TIMING MEASUREMENT OF MEMORIES USING LOW AREA, PROCESS IMMUNE TDCs

A DISSERTATION

Submitted in the partial fulfillment of the
requirements for the award of the degree

of

MASTER OF TECHNOLOGY
in
Electronics and Communication Engineering

(With specialization in Microelectronics and VLSI)

Submitted by

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May-2016

CANDIDATE'S DECLARATION

I hereby declare that the work which is being presented by me in this dissertation report entitled "**Timing Measurement of Memories Using Low Area, Process Immune TDCs**", submitted in partial fulfillment of the requirement for the award of the degree of, "**Master of Technology in Electronics and Communication Engineering**" with specialization in "**Microelectronics and VLSI**", and submitted to the Department of Electronics and Communication Engineering, Indian Institute of Technology, Roorkee, is an authentic record of the work carried out by me during the period June 2015 to May 2016, under the guidance of **Pratap Narayan Singh**, Principal Member of Technical Staff, STMicroelectronics, Noida, **Balwant Singh**, Group Manager, STMicroelectronics, Noida and **Dr. B. P. Das,** Professor, Electronics and Communication Engineering Department, Indian institute of Technology, Roorkee.

Date:
Place: IIT, Roorkee

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CERTIFICATE

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

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ABSTRACT

The access time of a memory which is one of the important performance parameters of memory design, is generally measured using time to digital converters (TDCs). This dissertation proposes a new analog type TDC architecture by exploiting a parasitic insensitive differential switched capacitor integrator which converts a time interval to be measured to voltage. The output voltage of the integrator is independent of the parasitic capacitances of the interconnects present between the two signal paths. The output voltage is then digitized using a 10-Bit Successive Approximation Register (SAR) type analog to digital converter (ADC). ADC employs a charge distribution type digital to analog converter (DAC). Various current and capacitor modes are provided to vary the measurement range and resolution of time measurement according to the accuracy required. The differential current given as input to the integrator is generated using a bandgap reference voltage source.

The major advantage of the proposed design is that it can measure time interval ranging from 1ps to 10ns for a power supply of 1V, 0.9V and 0.8V which shows the efficacy of the technique across supply voltage. The bandgap reference source used to generate current always operates at a power supply of 1.8V. The minimum time resolution that can be achieved is 3ps for a measurement range of 200ps. It is dependent on the LSB of the ADC used. The maximum operating frequency at which the design can measure the time interval accurately at a power supply of 1V is 20MHz. It decreases with the reduction in power supply. The proposed design is simulated and verified in using the 28nm UTBB-FDSOI Technology of STMicroelectronics.

KEYWORDS: Time to Digital Converter (TDC), Successive Approximation Register (SAR), Analog to Digital Converter (ADC), Digital to Analog Converter (DAC), Comparator, Switched Capacitor Integrator, Resolution.

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NOMENCLATURE

ABBEREVIATIONS

TDC Time to Digital Converter

TAC Time to Amplitude Converter

ADC Analog to Digital Converter

PVT Process Voltage Temperature

SAR Successive Approximation Register

DAC Digital to Analog Converter

1. Introduction

1.1 Access Time of Memories:

Access time is one of the most important performance parameters of a memory that decides the speed at which data can be read from a memory. It is defined as the time difference between the availability of output at the output pins while reading from a memory and the first clock rising transition that occurs after READ signal goes HIGH as explained in fig.1:

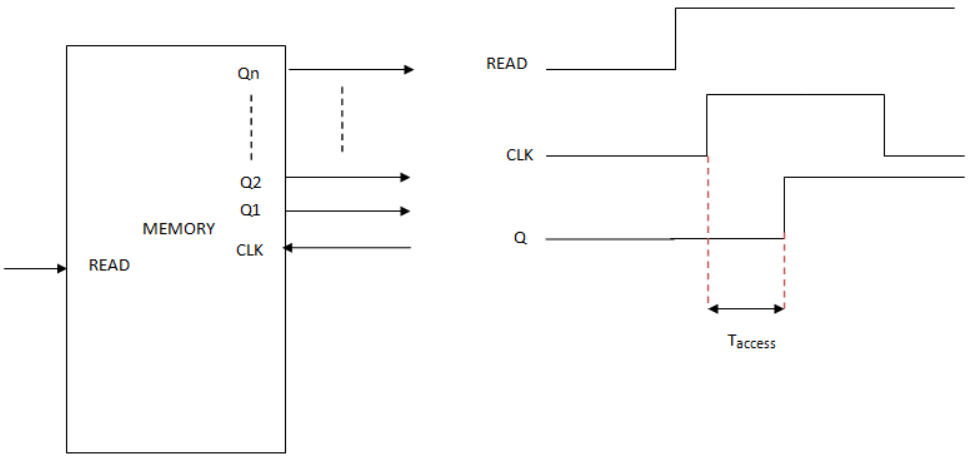

Fig.1 Access time of a memory.

In fig.1, T_{access} is the access time of the memory. It is generally measured using Time to Digital Converters (TDCs).

1.2 Time to Digital Converters:

Time to Digital Converters (TDCs) are basic building blocks of many applications such as high-precision on-chip time interval measurement, laser range finder, high-energy physics experiments, and 2D/3D imaging systems [23]. TDCs are typically used to measure time interval between two signals (generally referred to as START and STOP signals). Different TDC architectures including analog and digital type have been introduced in the literature having different resolution and measurement range. Some of these architectures are discussed below:

1.2.1 Analog TDCs:

It is a traditional approach to measure time interval. Analog type TDCs are also called as Time to Amplitude Converters (TACs).

(a) Current Integration Method: In this method, a pulse is generated using START and STOP signals whose pulse width is equal to the time difference between occurrences of these two signals. The pulse is then converted into voltage using an integrator. After that output voltage of the integrator is digitized using an Analog to Digital Converter (ADC) [5] as shown in fig.2. The dynamic range (DR) i.e. the maximum time interval that can be measured using an ADC with N bits is given by:

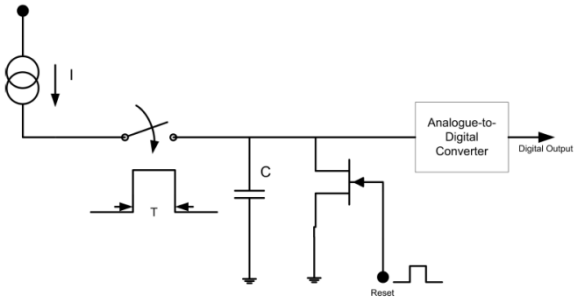

Fig 2: A simplified circuit for time interval measurement using dual-conversion [Ref. 5]

$$DR=2^{N}T_{LSB}$$

Where T_{LSB} is the minimum resolution that can be achieved.

The main problem with this circuit is that the resolution of the TDC depends on the resolution of the ADC.

(b) Dual Slope TDC: In this architecture of TDC, time stretching approach is used [3]. As shown in fig.3, current I_1 is integrated on capacitor C_1 for time period equal to the difference in occurrences of the START and STOP signals. As soon as STOP signal is arrived, I_1 is disconnected and current I_2 is used to charge another capacitor C_2. The voltage developed across C_1 during time interval T is given by:

$$V_{C1} = (I_1/C_1)T$$

After occurrence of STOP signal, let us say C_2 is charged for time T_2, then voltage developed across C_2 during T_2 is given by: $V_{C2} = (I_2/C_2)T_2$

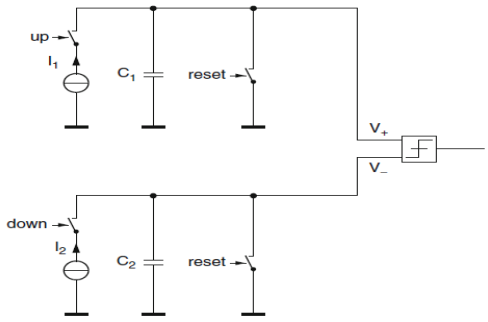

Fig 3: Schematic circuit diagram of a basic dual-slope TDC [Ref. 3]

Now V_{C1} will be equal to V_{C2} when:

$$T+T_2 = (1+(C_2/C_1)(I_1/I_2))T$$

So the time interval T is stretched by a factor of (1+M.N), where M is the capacitance ratio=C_2/C_1 and N is the current ratio=I_1/I_2.

Since M and N are dependent on ratios of capacitance and current values and not on the absolute values of capacitance and current, this circuit is more robust against process variations.

1.2.2 Digital TDCs:

(a) Counter based TDC: In this architecture of TDC, a reference clock frequency is used to count the number of clock periods fitting into the time interval to be measured [3]. A counter is used to count the number of clock edges as shown in fig.4:

$$\Delta T = NT_{CP} - (T_{CP} - \Delta T_{start}) + (T_{CP} - \Delta T_{stop})$$

$$\Delta T = NT_{CP} + \Delta T_{start} - \Delta T_{stop}$$

The overall resolution can be increased by increasing the frequency of the reference clock but that will lead to increase in power consumption.

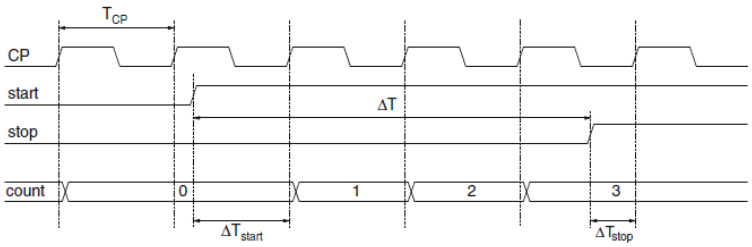

Fig 4: Principle of counter based TDC [Ref. 3]

(b) Digital Delay Line Based TDC: In this TDC architecture, START signal is delayed using a delay element chain [3]. The output of each delay element is given as input to a flip flop. At the arrival of STOP signal, sampled data is available at the output of the flip flops which generates a thermometric code.

If buffers are used in the delay chain, then the resolution is equal to the delay of two inverters. HIGH-LOW transition will give us a measure of the time interval as shown in fig.5. Let N be the number of HIGH outputs, then

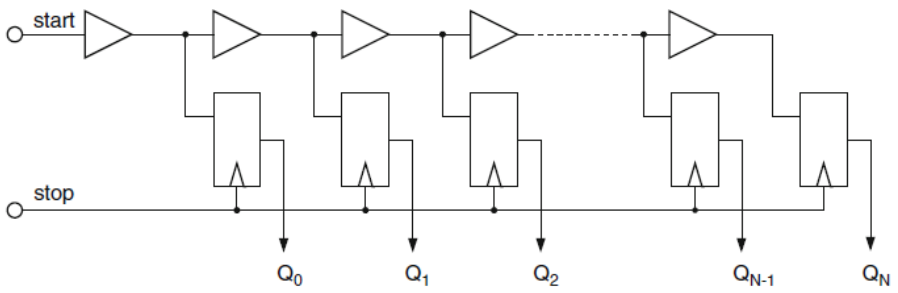

Fig 5: Implementation of a basic delay-line based time-to-digital converter [Ref. 3]

$\Delta T = NT_{LSB} + e$ where T_{LSB} is the delay of one element and e is the quantization error.

If inverters are used as delay elements then the resolution is doubled. But in case of inverters the output of the flip flops will be in the form of a series of alternating 0's and 1's.

111111111111111 ⌋⌈ 000000000000000 buffer TDC

010101010101010 ⌋⌈ 010101010101010 inverter TDC

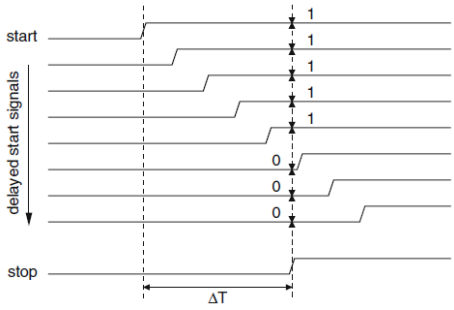

Fig 6: Operating principle of a delay line (including buffers) based TDC [Ref. 3]

In this case, the arrival of STOP signal is indicated by the phase change in the HIGH-LOW sequence instead of HIGH to LOW transition as in the case of buffers.

(**c) Vernier Delay Line Based TDC**: To reduce the resolution, both START and STOP signals are delayed using two delay lines having different delays [4]. Let START signal is delayed by the delay line in which each element provides a delay equal to t_1 and STOP signal is delayed by the delay line in which each element has a delay of t_2 such that t_2 is slightly less than t_1 as shown in fig.7. Let us assume that N stages have passed before the STOP signal catches up with START signal, then $T=N(t_1-t_2)$ and the resolution is (t_1-t_2).

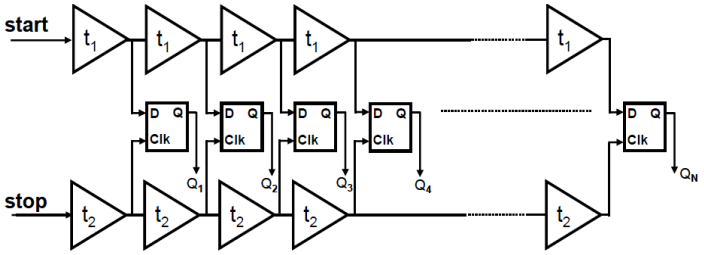

Fig 7: Vernier delay line TDC [Ref. 4]

If the resolution is very small then delay line should be long which leads to increase in INL.

1.2.3 Hybrid Type TDCs:

These TDCs are used when large measurement range is required with very high resolution. This can't be achieved by using above discussed architectures alone. So for large range, counter is used as coarse quantizer and for high resolution, one of the methods discussed above can be used as fine quantizer. Few of these are discussed below:

(a) Dual Slope Type Analog Interpolator: It is based on the Dual Slope TDC architecture. In this architecture, T1 or T2 are first stretched using the dual slope technique [1]. After that the stretched interval is measured using a counter as shown in fig.8.

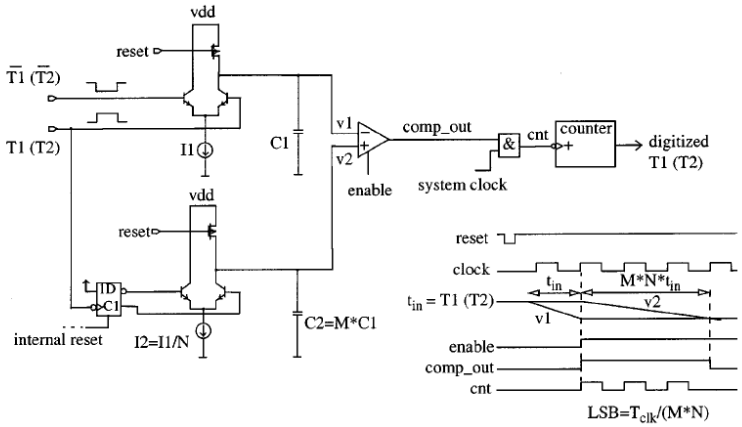

Fig 8: Principle of the interpolator based on time-to-voltage conversion [Ref. 1]

(b) Sub-gate Delay Line Interpolator: It uses a flash ADC type architecture [2]. The delay line consists of parallel elements. Let us assume that the delay of each element is τ_e originally and the time difference between each successive stage is τ_2 as shown in fig.9.

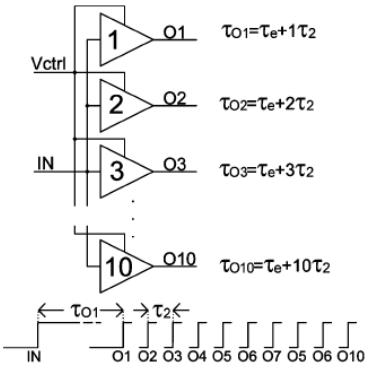

Fig 9: Parallel scaled delay line with its timing diagram [Ref. 2]

So the resolution of this architecture is τ_2 which can be varied by varying load capacitance of the delay elements. Hence in this case the resolution achieved is much smaller than that of cascaded delay line architecture which is limited by the technology.

Some other architectures are also available in the literature. An architecture based on pulse stretching [6] incorporates two parallel analog dual slope interpolators. Duty cycle of discharging clock along with capacitor and current ratios is used as stretching factor. The obtained resolution is around 50ps. In [7],[22], a TDC based on the pulse shrinking method is proposed. In this method, the pulse to be measured is given to a chain of inverters in which inverters have different aspect ratios which lead to reduction in pulse width of the signal. The number of inverters after which the pulse vanishes gives a measure of the width of the pulse. In [9], a TDC based on vernier delay lines is described. Vernier delay line is used for both coarse and fine quantization. To make the delay lines PVT insensitive, PLLs are used. [10] uses a time amplifier based on the varying delay of an SR Latch to amplify the time. A TDC based on differential delay line is proposed in [11] where the resolution is improved using a resistor divider interpolation technique which quantizes the delay of an element in the delay chain. [12] employs a TDC with successive approximation technique (used in ADCs). To increase the

measurement range, vernier delay line in the form of a ring is employed in [13]. [15] employs a counter as coarse quantizer and a miller integrator (discrete realization) as fine quantizer. In [16], analog type TDC with G_m-C integrator and SAR-ADC is employed. [17] is based on the dual slope conversion technique in which flash type architecture is employed to increase the conversion rate. [18] employs a flash TDC type architecture in which a capacitor bank is used to vary the delay of an inverter. [19],[20] use further modifications in vernier architecture to increase the measurement range and to reduce the non linearity in interpolation respectively. In [21], three dimensional vernier delay line is used to increase the measurement range further. [14] discusses the basic architectures of TDCs along with their performance analysis.

1.2.4. Comparison of various TDC architectures:

Table 1: Comparison of various TDC Architectures[8].

Technique	**Resolution**	**Variation Robustness**	**Comments**
Time to Amplitude Converters	~few ps	--	Resolution is limited by ADC resolution.
Time Stretching	~few ps	--	Robust against process variations.
Counter Based	~ns	-	Higher clock frequency required for higher resolution.
Delay Line	~ten's of ps	++	Affected by PVT variations.
Vernier	~ten's of ps	+	Affected by PVT variations.
Parallel Delay Elements	~few ps	--	More area requirements.

From table 1, it is clear that a few picosecond time resolution can be obtained using time to amplitude converters, time stretching approach or parallel delay elements technique. But the area requirement of the last two approaches is more than time to amplitude converters. Also time to amplitude converters are robust against process variations. So this technique is chosen for implementation.

2. Integrator Architectures for Time-Interval Measurement

In this chapter, Various integrator architectures with their limitations are discussed. In the end, a parasitic insensitive integrator architecture is chosen for implementation.

In analog type TDCs, time interval is converted into voltage using an integrator. So these are also known as time to amplitude converters (TACs). Different architectures of TACs were tried which are explained as follows with the help of simulation results:

2.1. Switched Capacitor Integrator with Voltage as Input:

It consists of a switched capacitor integrator circuit in which CLK and Q are START and STOP signals respectively as shown in fig.10. Voltage source is given as input and is used to charge the capacitor. Here differential architecture is used. VINN and VINP have equal and opposite variation. After Q signal goes LOW, the voltage source is disconnected and the charge stored on the holding capacitor is transferred to the feedback capacitor. Hence the output voltage of the integrator becomes a function of the time interval to be measured.

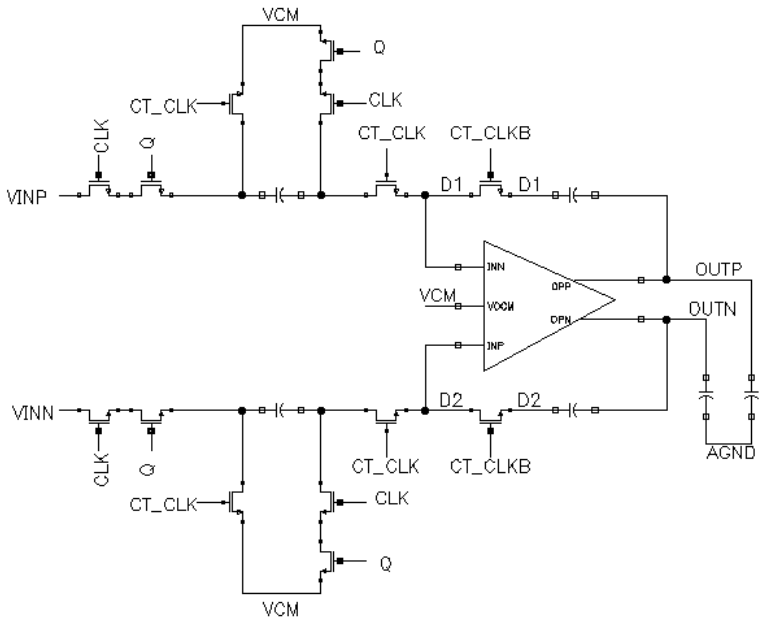

Fig 10: Schematic of Switched Capacitor Integrator with Voltage as Input.

Simulation conditions and results in 14nm UTBB-FDSOI technology of STMicroelectronics:

Input voltages VINN and VINP vary as: 0.5V±25mV. CLK transitions from LOW to HIGH and Q transitions from HIGH to LOW. Delay between CLK and Q is varying from 100ps to 1ns in steps of 100ps and then from 1ns to 10ns in steps of 1ns. CT_CLK is used to transfer the charge from holding capacitor to feedback capacitor and CT_CLKB is inverted signal of CT_CLK.

Fig.11 shows the variation of output voltage with transient time as a function of varying delay between CLK and Q signals.

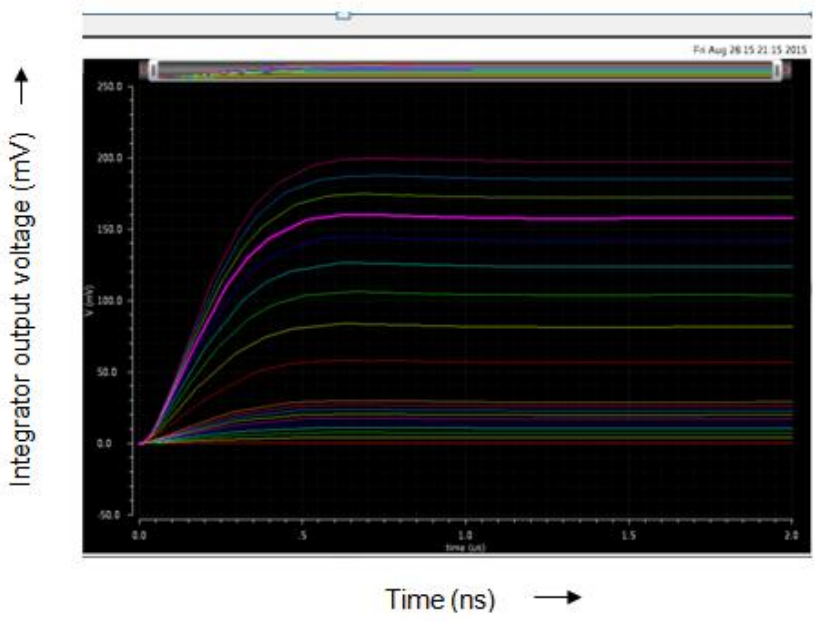

Fig 11: Output voltage of the integrator (y-axis) with transient time (x-axis) for different delay values for Switched Capacitor Integrator with Voltage as Input.

Now the output voltages are measured at t=1.99us. The change of this output voltage with the change in delay (time to be measured) is shown in fig.12. The time to be measured is varied from 100ps to 10ns and the output voltage (present at t=1.99us) is plotted. The characteristic exhibits exponential behavior.

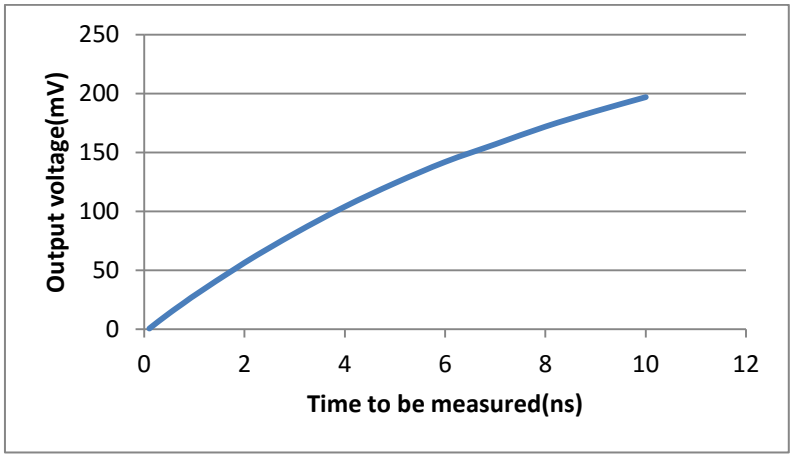

Fig 12: Variation of output voltage (present at t=1.99us) with time to be measured for Switched Capacitor Integrator with Voltage as Input.

This is because during charging, capacitor voltage at any time is given by:

$$V_c=V_o(1-\exp(-t/RC))$$

Here the time constant (RC) is dependent on the ON resistance of the switches present in the charging path of the capacitor. So it is not possible to estimate the time constant accurately and hence the output voltage. This circuit cannot be used for estimation of time interval with a good resolution.

2.2. Switched Capacitor Integrator with Current as Input:

To avoid the dependency of capacitor voltage on the ON-Resistance of the switch, voltage source is replaced by a current source. In this case, charge stored on the capacitor during the time interval T is given by:

$$Q=I.T$$

Where I is the value of the input current. Here the charge stored has a linear dependency on the time interval to be measured.

The circuit is shown in the fig.13. Differential current is generated by giving differential voltage as V_{gs} to the MOSFETs. PULSE is a signal whose pulse width is equal to the delay between START and STOP signals. Using this differential current source, capacitor is charged. After that the current source is disconnected and the charge stored on the holding capacitor is transferred to the feedback capacitor.

The main problem with this circuit is that it is sensitive to the effect of parasitic capacitances. Due to this non linearity in the output appears which cannot be measured.

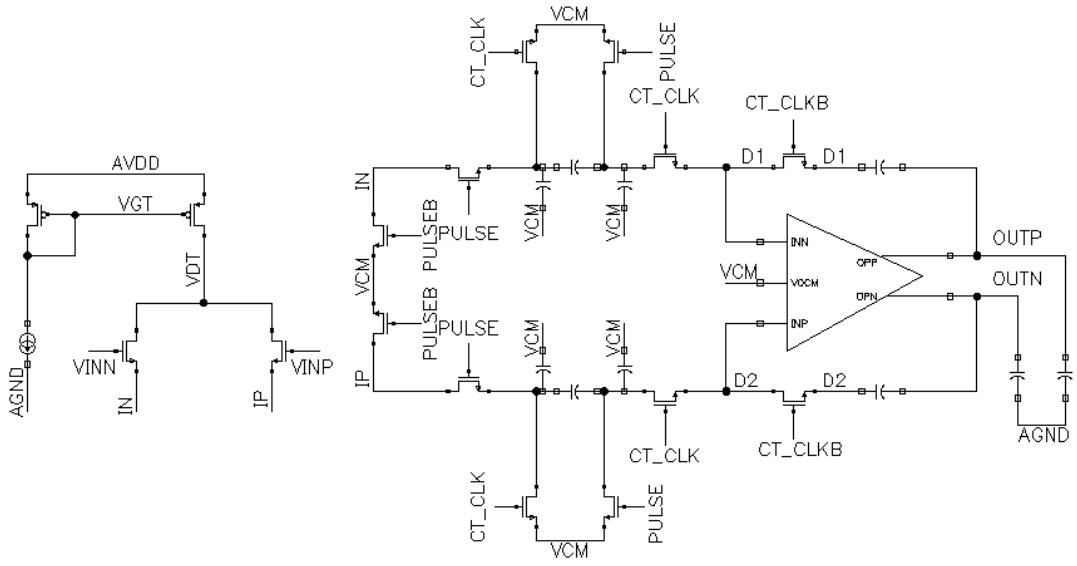

Fig 13: Schematic of Switched Capacitor Integrator with Current as input.

Simulation conditions and results in 28nm UTBB-FDSOI technology of STMicroelectronics:

PULSE is a signal whose pulse width is varying from 100ps to 1ns in steps of 100ps and then from 1ns to 10ns in steps of 1ns. PULSEB is inverted signal of PULSE. These two are non overlapping signals. Input signals for generating differential current i.e. VINN and VINP are varying as: 1V±5mV. CT_CLK is a signal which transitions from LOW to HIGH after 20ns for charge transfer.

The capacitors connected at both ends of the holding capacitor are 15% of their value for taking into account the effect of parasitic capacitances.

Now the output voltage present at t=49us is measured. The change of this voltage with the change in pulse width of signal PULSE (time to be measured) is shown in fig.14.

As seen from the fig.14, the output voltage is a non linear function of the time to be measured. This happens because of the parasitic capacitances. Due to the effect of parasitics, the current gets divided and hence the non linearity arises. Since this non linearity cannot be estimated so this circuit also cannot be used for measurement of time interval with a good resolution.

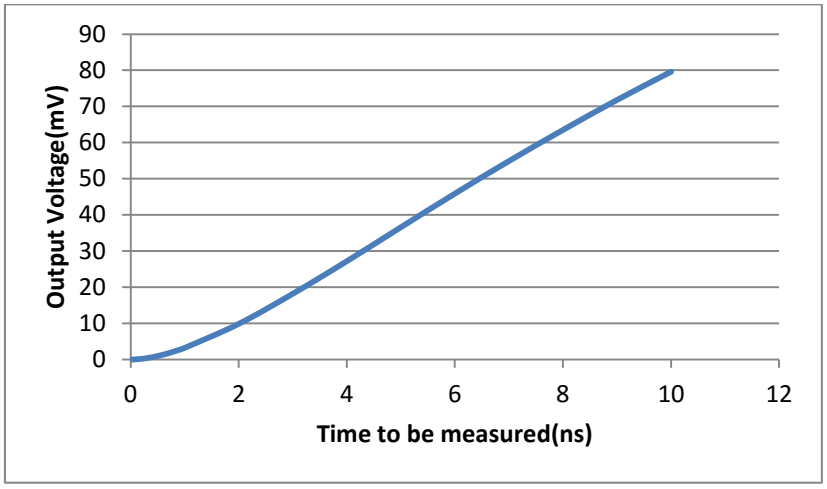

Fig 14: Variation of output voltage (present at t=49us) with time to be measured for Switched Capacitor Integrator with Current as Input.

2.3. Continuous Time Integrator with Current as Input:

This architecture is used to remove the effect of parasitic capacitances. Instead of integrating the current on the holding capacitor first and then transferring the charge onto the feedback capacitor, the current is directly integrated on the feedback capacitor. So here instead of switched capacitor integrator, a continuous time integrator is used. In this case bandwidth and gain of the op amp come into picture. To measure a time interval as small as 1ps, the GBW requirement of the op amp is quite large.

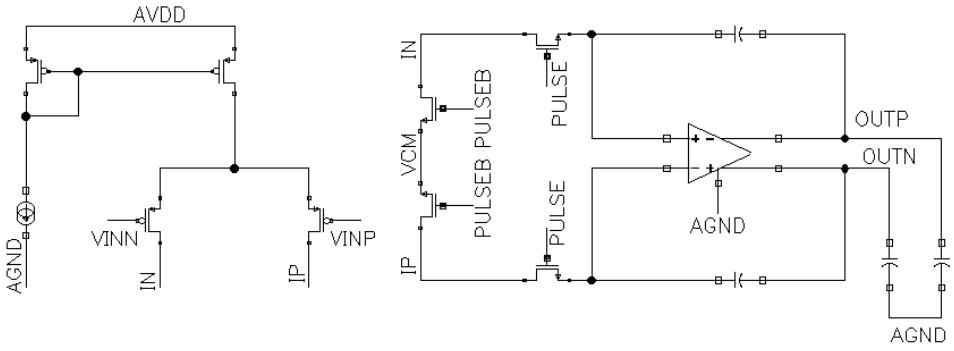

Fig 15: Schematic of Continuous Time Integrator with Current as Input.

To find the required dominant pole frequency and gain of the op amp for measuring time period varying from 1ps to 10ns, an ideal op amp is used and its gain and pole frequency are varied so that we get a linear output voltage vs. time delay curve as shown in fig.15. The required specifications are:

Gain=70dB and Pole frequency=50MHz .

which lead to a gain bandwidth product of the order of 150GHz.

Simulation conditions and results in 28nm UTBB-FDSOI technology of STMicroelectronics:

Input signals for generating differential current i.e. VINN and VINP are varying from 550mV±10mV. PULSE is a signal whose pulse width is to be measured. It is varying from 100ps to 1ns in steps of 100ps and then from 1ns to 10ns in steps of 1ns.

The output voltage is measured at t=49us. It is linearly varying with the pulse width of signal PULSE (time to be measured) as shown in fig.16.

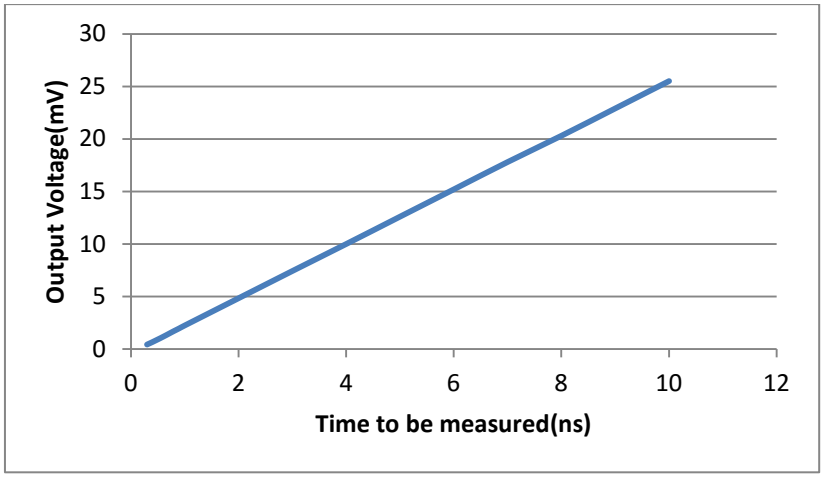

Fig 16: Variation of output voltage (present at t=49us) with time to be measured for Continuous Time Integrator with Current as Input.

Now the maximum f_T attainable with a single transistor in 28nm UTBB-FDSOI technology of STMicroelectronics is 300GHz. So a GBW of 150GHz for an op amp utilizing so many transistors is not attainable using this technology. Hence this design is not theoretically possible.

2.4. Parasitic Insensitive Switched Capacitor Integrator:

Fig.17 shows the schematic of the parasitic insensitive switched capacitor integrator. Here the current is given as input to the integrator. The differential current is generated using different PMOS and NMOS circuits. PMOS circuit act as current source while NMOS circuit act as current sink. So when these circuits are combined, the complete circuit acts as a differential current source.

This current is then integrated on the holding capacitor for a time interval equal to pulse width of signal PULSE (time to be measured). After this, the current source is disconnected and the charge stored on the holding capacitor is transferred to the feedback capacitor when CT_CLK goes from LOW to HIGH.

RESET switch is used to discharge the feedback capacitor after each measurement. Virtual ground nodes of the op amp are also precharged to a voltage equal to DC output voltage of the op amp by keeping RESET signal HIGH for some time.

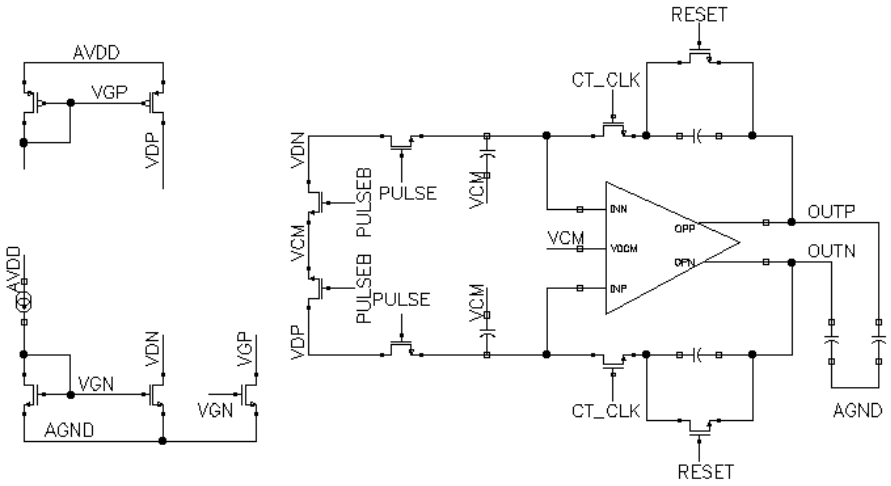

Fig 17: Schematic of Parasitic Insensitive Switched Capacitor Integrator.

Simulation conditions and results in 28nm UTBB-FDSOI technology of STMicroelectronics:

PULSE is a signal whose pulse width is to be measured. It is varying from 1ps to 10ns. PULSE and PULSEB are non overlapping signals. CT_CLK and RESET signals are initially HIGH for some time for discharging the feedback capacitor and precharging the virtual ground nodes.

The output voltage is measured at t=49us and is plotted as a function of pulse width of signal PULSE (time interval to be measured) as shown in fig.18. As seen from the fig.18, the output is linearly dependent on the time interval to be measured. Hence this Integrator architecture is not affected by the parasitic capacitances and can be used for time measurement with good resolution.

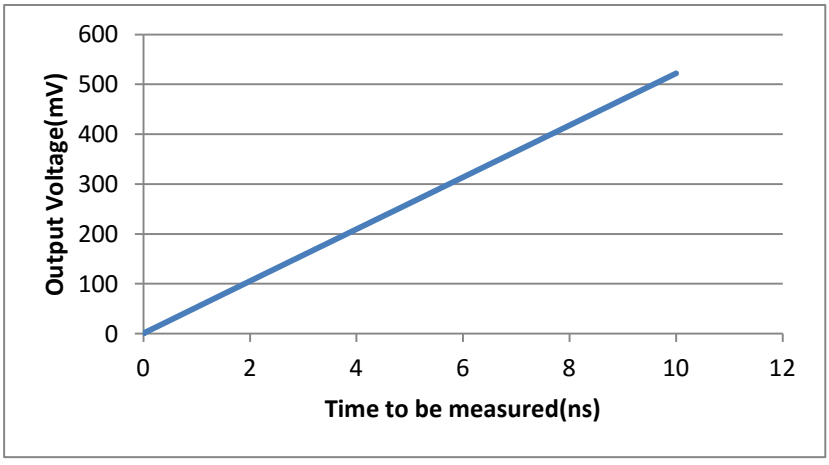

Fig 18: Variation of output voltage (present at t=49us) with time to be measured for Parasitic Insensitive Switched Capacitor Integrator.

Also the output voltage of this integrator can be expressed as:

$$V_{out}=I.T/C +Offset$$

Here C is the feedback capacitor and I is the input current. So the slope of the V_{out} vs T characteristic is independent of any parasitic capacitances. Hence this integrator design is parasitic independent.

3. Parasitic Independent and Wide Range Time-to-Digital Converter

In this chapter, the proposed TDC design is discussed in detail. The main objective of this work is to measure the access time of the memory. Two major contributions of this work are as follows:

1. The time internal to be measured is independent of the parasitic capacitances offered by two signal paths as the output voltage does not depend on the parasitic capacitances of the interconnects.
2. It can measure wide range of time intervals starting from 3 ps to 10 ns.

The top level block diagram of the proposed design is shown in fig.19. The design cosnsists of switched capacitor integrator, differential current generator, 10-bit SAR ADC along with bandgap voltage source and reference generator circuit. A differential current generated from a bandgap reference source is integrated using a switched capacitor integrator circuit for the time duration that is to be measured. A corresponding differential output voltage is generated at the output of the integrator, which is then converted into digital count using a 10-Bit SAR ADC. The reference voltages required for the ADC are generated from the bandgap reference voltage source. Different modes are provided for calibration of the circuit which will be explained in section 3.6.

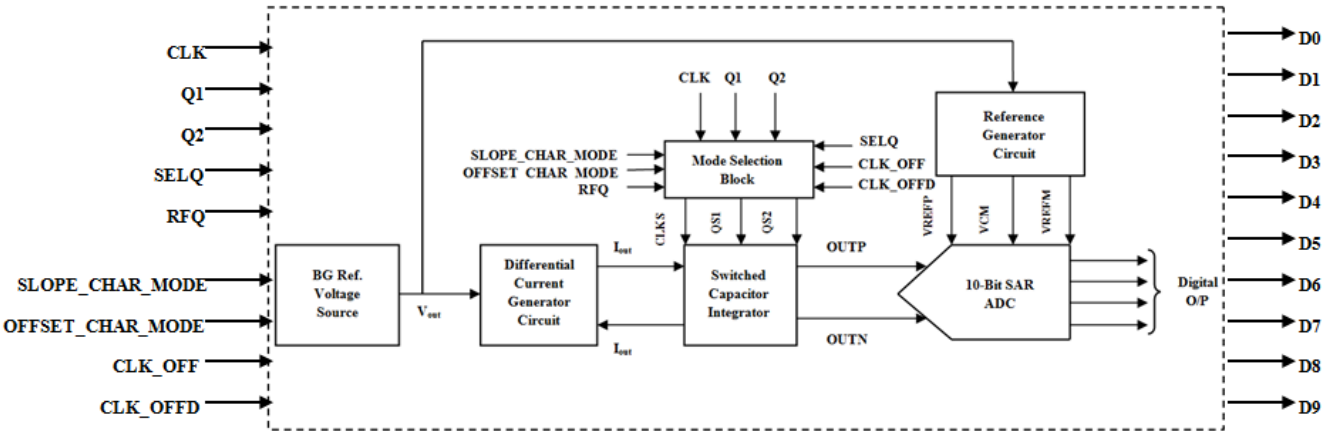

Fig 19: Top level block diagram of the proposed design.

3.1. Switched Capacitor Integrator:

In the proposed design, parasitic insensitive switched capacitor integrator is employed with some modifications. Instead of giving signal PULSE whose pulse width is equal to the time interval to be measured, two signals CLK and Q (equivalent to START and STOP signal) are used as shown in fig.20.

Access time of memory is measured with respect to two outputs from the memory: one which is closest to clock pin (Q1) and the one which is farthest from the clock pin (Q2). So a select pin SELQ is provided to select the Q pin with respect to which we want to measure the access time. Now the output of a memory i.e. Q can transition from HIGH to LOW or from LOW to HIGH but irrespective of that the input to the switch in the integrator (QS1 or QS2) should always transition from HIGH to LOW for proper operation of the circuit. This is ensured using a digital logic block shown in fig.21. As shown in

fig.21, a signal RFQ is used for differentiating between two transitions of Q i.e. from LOW to HIGH or from HIGH to LOW. When RFQ is LOW, Q transitions from LOW to HIGH and in this case Q is inverted and then its non overlapping counterpart is generated. When RFQ is HIGH, Q transitions from

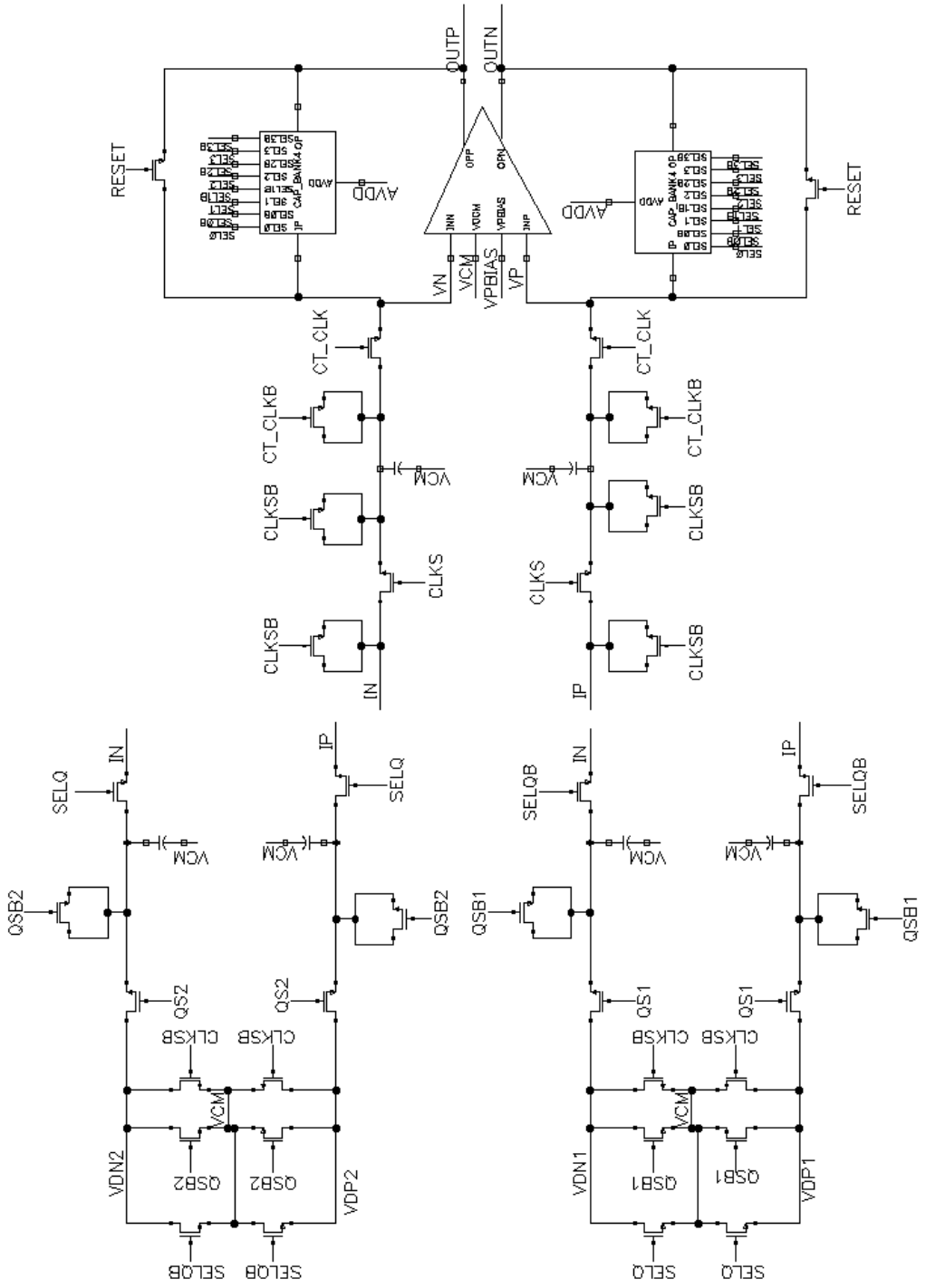

Fig 20: Integrator Design.

HIGH to LOW and in this case Q is directly given to the non overlapping clock generator circuit. RFQ signal ensures that QS always transitions from HIGH to LOW and QSB always transitions from LOW to HIGH. So QSB is non overlapping counterparts of Q signal.

CLK signal always transitions from LOW to HIGH. To balance the paths of both CLK and Q signals, CLK signal is also given to another digital logic block shown in fig.22 to generate CLKS signal which always goes from LOW to HIGH. CLKS (always rising) and QS (always falling) are given as input to the switches used in the integrator. CLKSB is non overlapping counterparts of CLK signal.

When both CLKS and QS signals are HIGH, only then the differential current will charge the holding capacitors. If any of these signals or both are LOW then the current will be steered away by the

switches controlled by CLKSB and QSB.

When SELQ=LOW, then the system will measure access time with respect to Q1 and the current of the Q2 path will be steered away by the switches controlled by SELQB signal (Inverted counterpart of

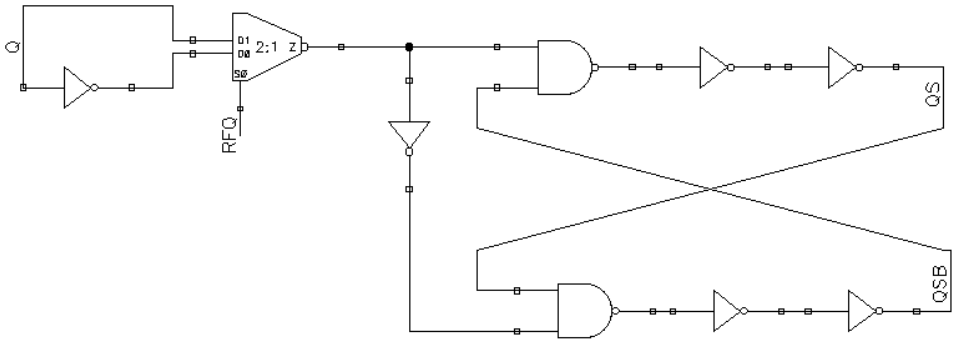

Fig 21: Q_DETECT Block to select transition of Q.

SELQ signal). When SELQ=HIGH, then the system will measure access time with respect to Q2 and the current of the Q1 path will be steered away by the switches controlled by SELQ signal.

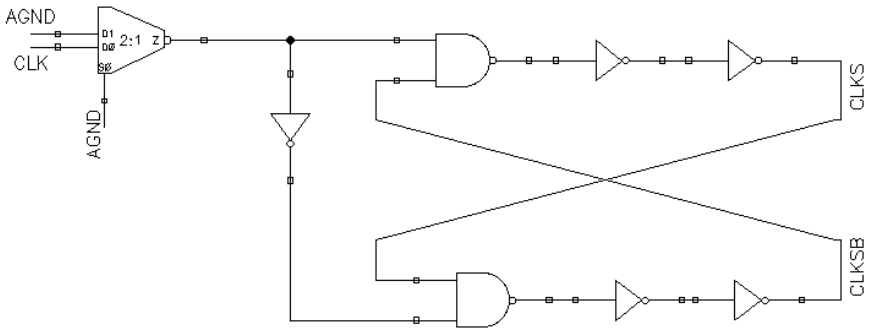

Fig 22: CLK_BAL block to balance the paths of CLK and Q.

Also, some dummy switches are used to cancel the effect of channel charge injection. The capacitances present between the input switches controlled by CLKS and QS are to take into account the effect of the parasitic capacitances of the metal line that will be used to connect these two switches. The circuit is insensitive to these parasitic capacitances.

After charging of holding capacitor, the charge is transferred to the feedback capacitor when CT_CLK goes HIGH.CT_CLK is generated using the digital logic shown in fig.23.

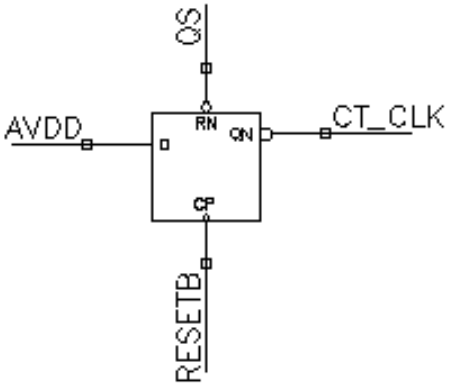

Fig 23: CT_CLK_GEN block to generate CT_CLK.

Feedback capacitor is present in the form of a capacitor bank consisting of 4 capacitors: 5fF, 25fF, 45fF, 65fF. One of these can be selected using signals CS0 and CS1 with the help of a 2:4 decoder circuit as shown in fig.24.
The feedback capacitor can be selected as shown in table:

Table 2: Feedback Capacitor Modes.

CS1	CS0	Feedback Capacitor
LOW	LOW	5fF
LOW	HIGH	25fF
HIGH	LOW	45fF
HIGH	HIGH	65fF

As the value of feedback capacitor increases, the time resolution of the system decreases and measurement range increases as explained in section 3.6.

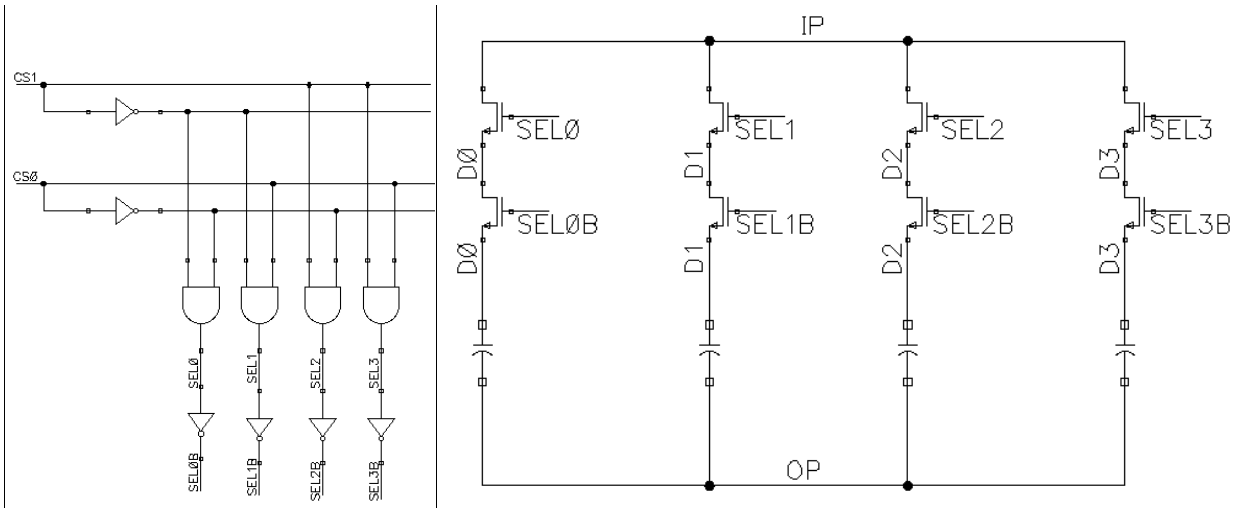

Fig 24: Capacitor bank and 2:4 Decoder to select feedback capacitor.

RESETB is the inverted signal of RESET signal (used to discharge the feedback capacitor before each measurement).

The op amp used in the integrator circuit is a two stage differential op amp as shown in fig.25. The first stage consists of diode connected transistor and cross coupled PMOS stage in parallel so that the overall output impedance is very high and gain is quite large. Second stage is CLASS A push pull stage with PMOS common source amplifier and NMOS as its load. The biasing to this NMOS load is provided by the common mode feedback circuit which sets the output common mode voltage to the voltage provided as input to it.

The common mode feedback circuit is shown in fig.26. The output of the 2nd stage of op amp is given as input to the common mode feedback circuit. The circuit compares the 2nd stage outputs with output

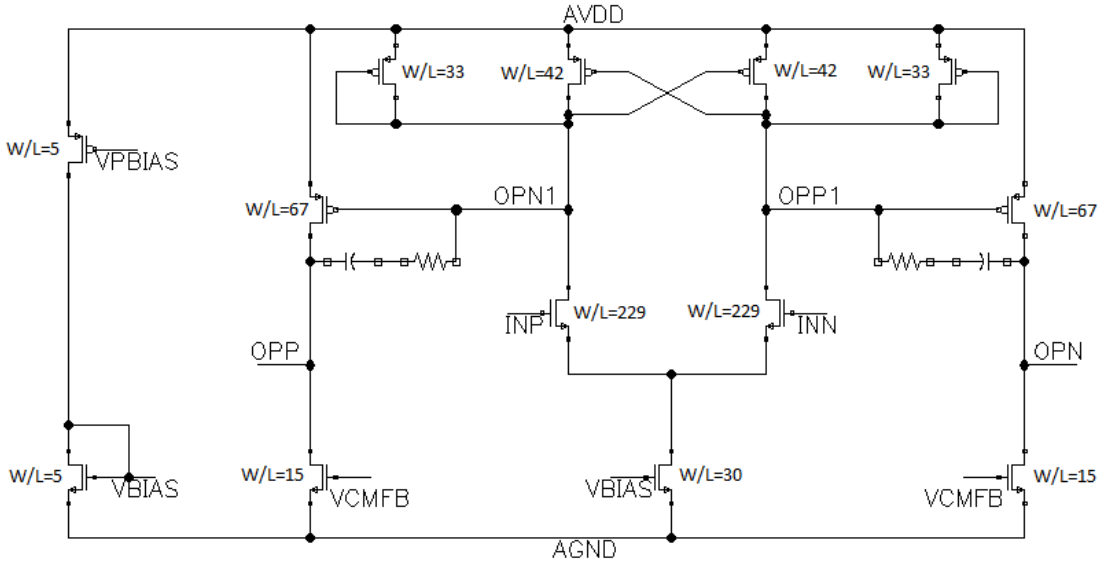

Fig 25: Schematic of Differential Ended Op Amp used in Integrator.

common mode voltage given as input and sets them equal. The output of this circuit is used for biasing of the NMOS load transistors present in the 2nd stage of the op amp. It sets their biasing voltage such that the common mode output voltage of the 2nd stage is equal to the voltage given as input (common mode voltage).

The specifications of the op amp at V_{dd}=1V and nominal corner when VOCM=300mV in 28nm UTBB-FDSOI technology of STMicroelectronics are:

DC Gain=81.1dB
GBW=586.6MHz
Phase Margin=66.71˚

The gain and GBW requirements of this op amp are quite large. The reason for this will be explained in section 3.6.

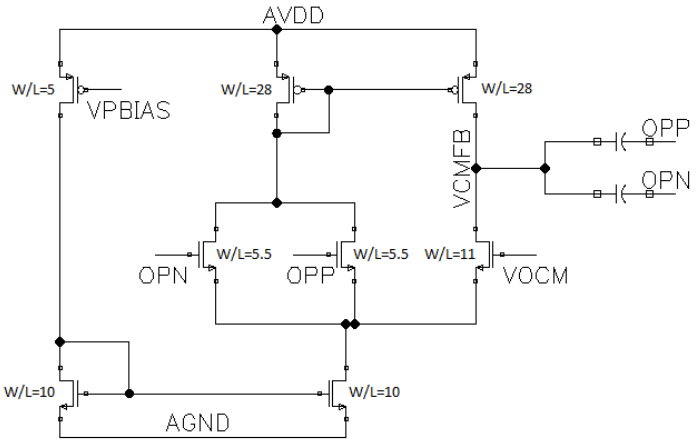

Fig 26: Common Mode Feedback Circuit.

3.2. Differential Current Generator:

The differential current given as input to the integrator is generated using a bandgap source. This bandgap source always operates at V_{dd}=1.8V.

A bandgap reference source is a circuit that generates a constant voltage or current independent of temperature changes [25]. Two quantities having positive and negative temperature coefficients are used to make a temperature independent source. Generally used quantities for this purpose are:

(i) The base emitter voltage of a BJT has a negative temperature coefficient.

(ii) The difference in base emitter voltages of two BJTs having unequal currents flowing through them has a positive temperature coefficient.

When these two quantities are proportionately added, a temperature independent quantity is obtained.

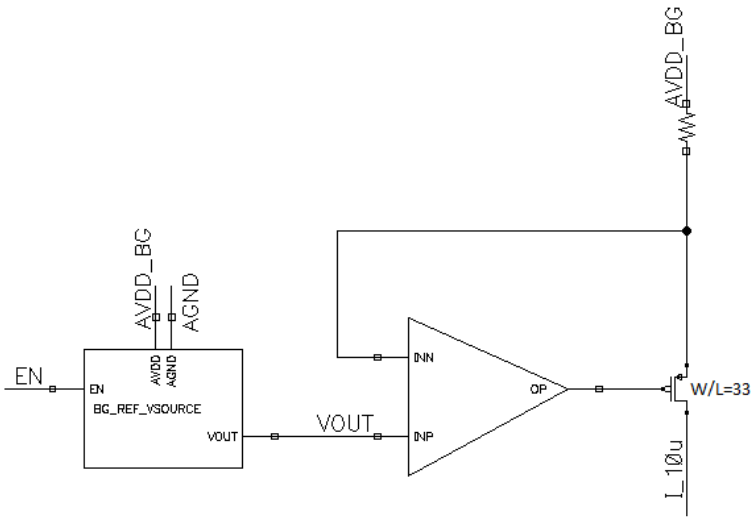

Fig 27: Circuit to generate a constant current of 10uA.

First of all, a bandgap source is used to generate a constant voltage. This constant voltage is then converted into constant current using the circuit shown in fig.27. A constant current of 10uA is generated using this circuit.

The op amp used here operates at V_{dd}=1.8V. The internal architecture of this single ended op amp is shown in fig.28.
Two current modes are introduced in the circuit to vary range and resolution of the circuit as explained in section 3.6. IMODE signal is used to vary the input current. When IMODE=LOW, 1uA current will be generated. But when IMODE=HIGH, 3uA current will be generated as shown in fig.29.

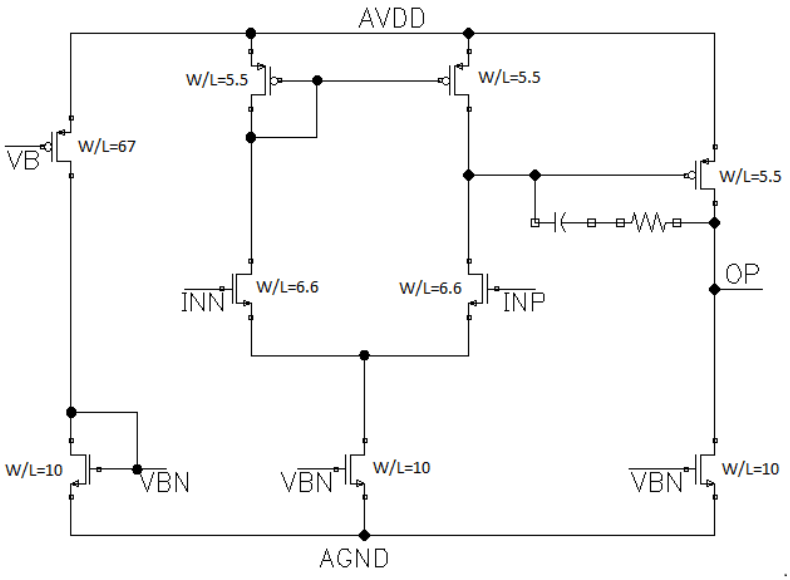

Fig 28: Schematic of Single Ended Op Amp to generate constant current (Operating at 1.8V).

After selecting input current mode, differential current is generated using current mirroring technique as shown in fig.30. PMOS acts as current source and NMOS acts as current sink. These are then fed to the integrator.

Same method is used for generation of differential current for both the outputs.

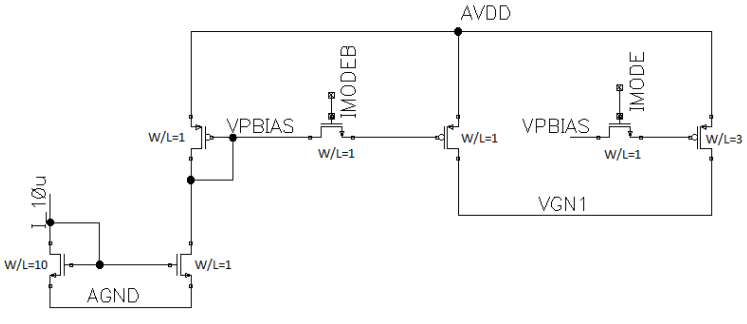

Fig 29: Circuit to introduce two current modes.

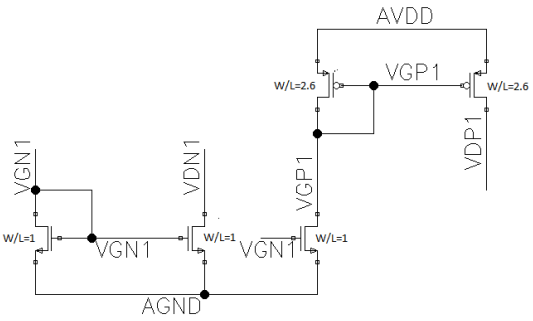

Fig 30: Circuit to generate Differential Current.

3.3. 10-Bit SAR ADC:

Differential output of the integrator is fed to a 10-bit differential SAR (Successive Approximation Register) type ADC. The block diagram of the ADC is shown in fig.31.

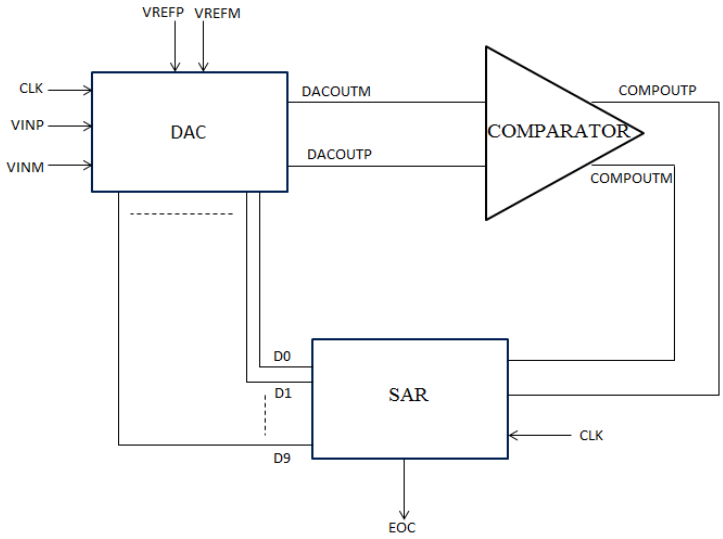

Fig 31: Block Diagram of SAR ADC

The ADC consists of a differential switched capacitor type DAC as shown in fig.32. Binary weighted capacitor array is used to convert digital signal to analog signal. Initially both the plates of the capacitors are connected to VCM (common mode input voltage). After that in the sampling mode, one plate of the capacitor is connected to input voltage (VINP in case of positive capacitor array and VINM in case of negative capacitor array) and the other to VCM so that the charge stored on the capacitor plates after this mode is proportional to (VCM-VIN). Now the SAR logic sets the MSB to logic '1' so that largest capacitor is connected to VREFP and the rest to VREFM in positive capacitor array (largest capacitor to VREFM and rest to VREFP in case of negative capacitor array). Now the DAC converts it into analog voltage which is then given as input to comparator. The comparator compares the two

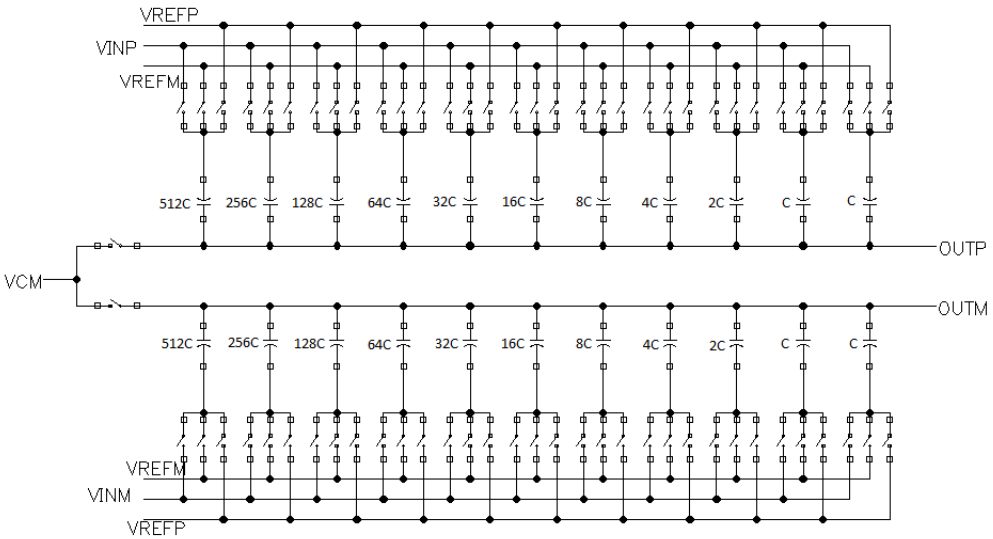

Fig 32: Switched Capacitor DAC

voltages and sends its output to SAR logic which again sets and resets the bits according to the output of the comparator. It will set the bit to 1 if input voltage is larger than the reference voltage otherwise 0 successively. Hence the analog input voltage is converted into digital count by successive approximation technique [24].

3.4. Reference Generator Circuit:

The reference voltages and common mode voltage for the ADC are generated using the bandgap voltage source. The constant voltage obtained from the bandgap source is 1.2V. This is given to resistive network through a buffer. The voltages obtained from the resistive divider network are 0.6V (VREFP), 0.3V (VCM) and GND (VREFM). These are given to ADC through buffers. Decoupling capacitors of 1uF are also used to reduce the effect of switching.

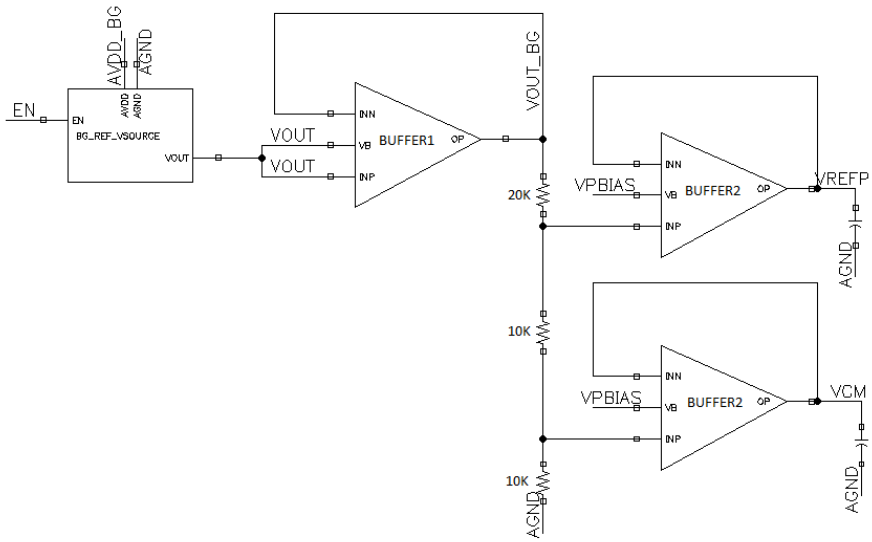

Fig 33: Reference Voltage Generation Circuit for ADC.

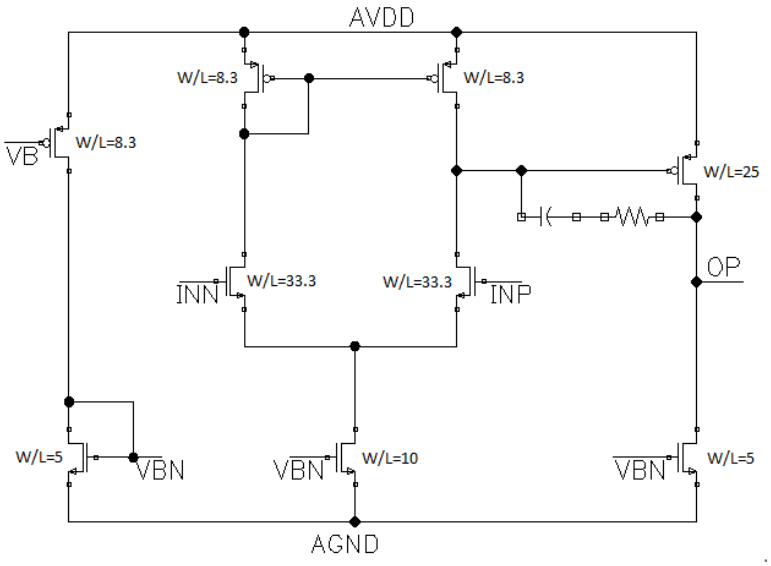

Fig 34: Schematic of BUFFER1 (Operating at V_{dd}=1.8V).

BUFFER1 used in the reference generation circuit is shown in fig.34. It operates at bandgap power supply i.e. V_{dd}=1.8V.

BUFFER2 is shown in fig.35.

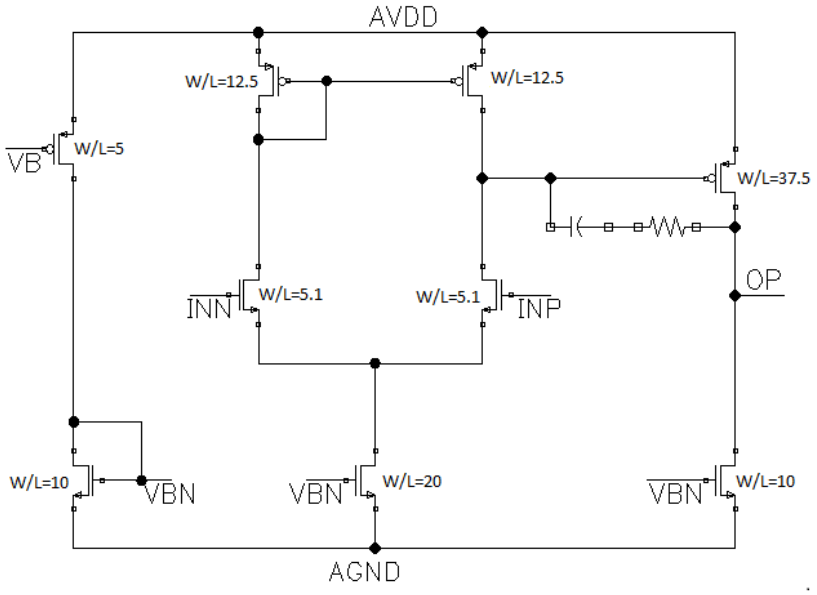

Fig 35: Schematic of BUFFER2.

3.5. Mode Selection Block:

As explained in section 3.6, the time can be calculated as follows:

$$T= (V_{out}\text{-Offset})/\text{Slope}$$

So, two parameters: *Offset* and *Slope* are needed for calculation of time.

So two modes are provided as shown in fig.36.

(i) **Offset characterization mode:** This mode is used to calculate offset of the system. In this mode, OFFSET_CHAR_MODE signal is kept HIGH. Then same signal CLK_OFF is applied to both Q and CLK switches such that the time interval to be measured is 0. This will calculate the overall offset of the system.

(ii) **Slope characterization mode:** This mode is used to calculate the slope of the V_{out} vs. T characteristics. In this mode, SLOPE_CHAR_MODE signal is kept HIGH. CLK_OFF signal is applied instead of CLK signal and CLK_OFFD signal instead of Q signal such that the delay between occurrences of CLK_OFF and CLK_OFFD signal is already known to us. Let the delay between CLK_OFF and CLK_OFFD signals is T_{known} and the output voltage corresponding to this delay is V_{known} then slope of the characteristics can be calculated as follows:

$$\textit{Slope}=(V_{known}\text{-Offset})/T_{known.}$$

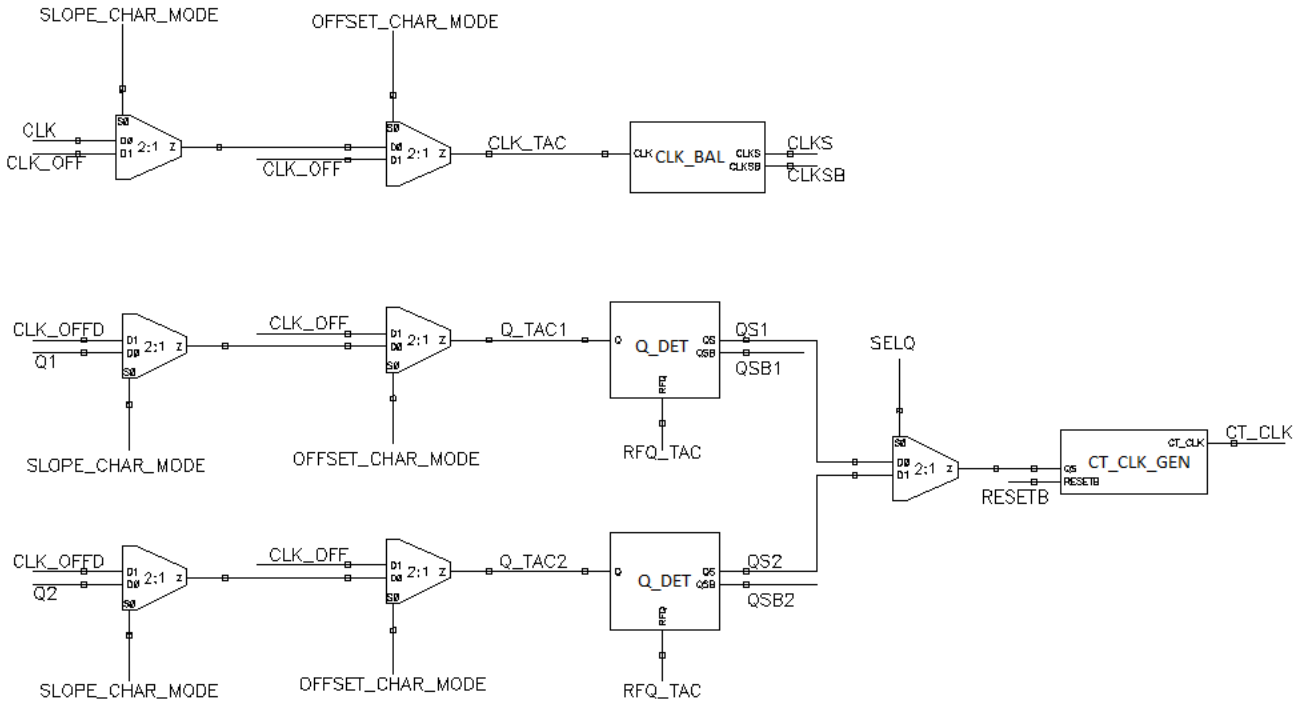

Fig 36: Block to select characterization modes.

3.6. Time Calculation:

Let I be the input differential current to the integrator, C_H be the holding capacitor, C be the feedback capacitor, T be the time period to be measured i.e. the time difference between CLK and Q signals. Then charge stored on C_H during time interval T is given by:

$$Q=I.T$$

This charge is then transferred to feedback capacitor C when CT_CLK goes from LOW to HIGH.

So the voltage across C is given by:

$$V_C = Q/C = I.T/C$$

This voltage appears as differential output of the integrator. So output of the integrator is given by:

$$V_{out} = I.T/C + Offset$$

Slope of V_{out} vs. T characteristics is directly proportional to I/C.

As I increases and C decreases, *Slope* of the characteristic increases i.e. change in Vout for the same change in T increases. Hence the resolution of the system increases but now the output of the integrator will saturate for smaller values of T , hence range of measurement decreases.

$$T = (V_{out} - Offset)/Slope$$

If slope for one current and capacitor mode is calculated then the slope for the rest will be proportional. So, only one slope value is needed for slope calculation of all the current and capacitor modes.

The resolution and range corresponding to all capacitor and current modes in 28nm UTBB-FDSOI technology of STMicroelectronics are specified in table 3:

Table 3: Measurement range and resolution for Input Current and Capacitor modes.

IMODE	INPUT CURRENT	CS1	CS0	FEEDBACK CAPACITOR	RESOLUTION	MEASUREMENT RANGE
1	3uA	0	0	5fF	2-3ps	200ps
1	3uA	0	1	25fF	6ps	1.25ns
1	3uA	1	0	45fF	12ps	2.25ns
1	3uA	1	1	65fF	17ps	3.5ns
0	1uA	0	0	5fF	6ps	600ps
0	1uA	0	1	25fF	20ps	3.5ns
0	1uA	1	0	45fF	35ps	7ns
0	1uA	1	1	65fF	50ps	10ns

The gain of the integrator op amp should be high so that A/1+AB factor does not affect the proportionality of slopes. If gain is less then the slopes will be lesser than the ideal values and hence the slope ratios will change.

The GBW of the op amp should also be higher so that the output of the integrator settles in lesser time and the maximum operating frequency of the system increases.

4. Analytical Modeling of Integrator Circuit

In this chapter, an analytical model for the switched capacitor integrator is devised and an expression for the output voltage is obtained including the non linearities of the op amp. The circuit can be modeled as explained below:

The circuit diagram of the integrator circuit is shown in fig.37. Three different phases are defined according to the input signals applied as shown in fig.38. The operation of the circuit in these phases

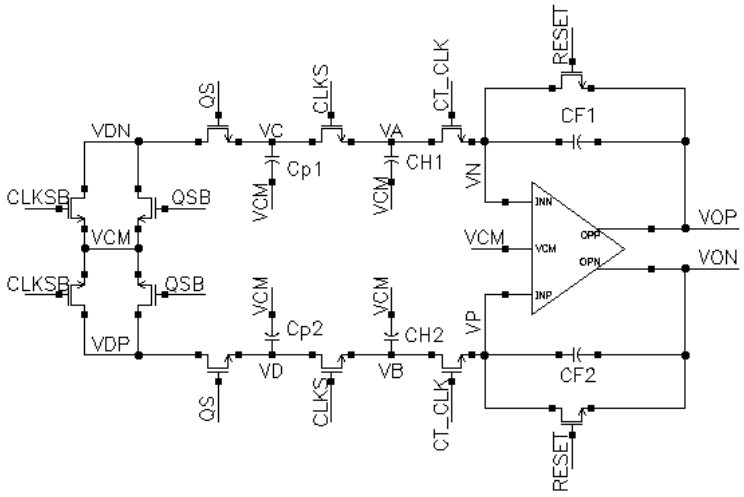

Fig 37: Basic Integrator Circuit with capacitance mismatches.

can be understood as follows:

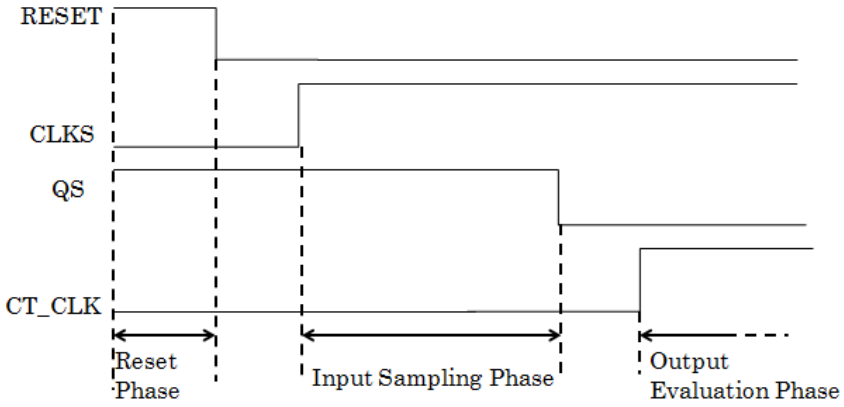

Fig 38: Three phases of operation of the integrator circuit.

(i) **Reset Phase:** This phase is used to discharge the feedback capacitor before each measurement. The circuit diagram for this phase is shown in fig.39.

Let V_{os1} is the total offset present due to current flowing between nodes C and D. Since current,I is flowing from node C to D, node C is at higher potential than node D. The voltages at these nodes can be written as:

$$V_c = V_{CM} + \frac{V_{os1}}{2} \text{ and } V_D = V_{CM} - \frac{V_{os1}}{2}$$

C_{p1} and C_{p2} correspond to the parasitic capacitances of interconnects present between switches controlled by CLKS and QS. C_{H1} and C_{H2} are the holding capacitors. C_{F1} and C_{F2} are the feedback

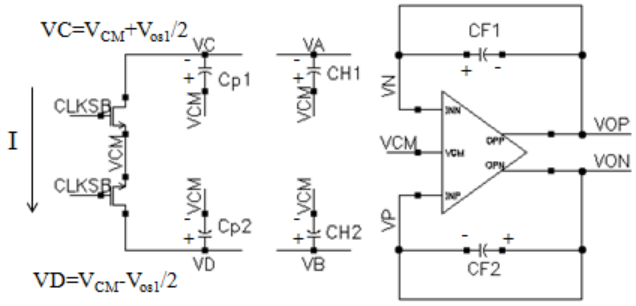

Fig 39: Circuit Configuration in Reset Phase.

capacitors present in the negative feedback path of the op amp. Charge across all of these capacitors is given by the following equations:

$$Q_{cp1} = C_{p1}\left[V_{CM} - V_{CM} - \frac{V_{os1}}{2}\right] = -C_{p1}\frac{V_{os1}}{2} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(1)$$

$$\text{And } Q_{cp2} = C_{p2}\left[V_{CM} - \frac{V_{os1}}{2} - V_{CM}\right] = -C_{p2}\frac{V_{os1}}{2} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(2)$$

Because $V_A \approx V_B \approx V_{CM}$, hence $Q_{C_{H1}} = 0$ and $Q_{C_{H2}} = 0$ ……..…..(3)

And $V_N = V_{OP}, V_P = V_{ON}$, hence $Q_{C_{F1}} \approx 0, Q_{C_{F2}} \approx 0$ ……..(4)

(ii) Input Sampling Phase: In this phase, both CLKS and QS go HIGH and charge the holding capacitor for a time period that is to be measured. Let us denote this phase by φ_1. The circuit configuration is shown in fig.40.

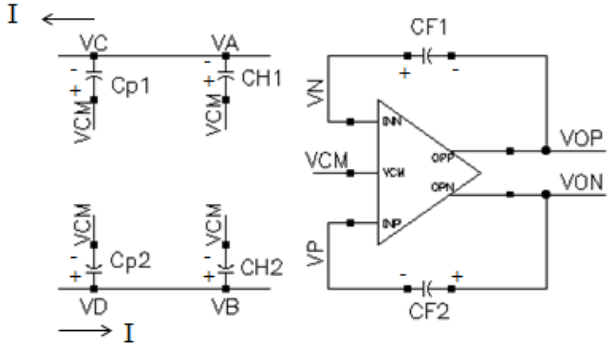

Fig 40: Circuit Configuration in Input Sampling Phase.

As shown in fig.40, C_{p1} and C_{H1} come into parallel. Similarly C_{p2} and C_{H2} come into parallel. The total charge at the end of this phase is given by:

$$Q_{C_{p1}+C_{H1}}(\Phi_1) = IT - C_{p1}\frac{V_{os1}}{2} = (C_{p1}+C_{H1})\left[V_{CM} - V_A(\Phi_1)\right] \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(5)$$

$$Q_{C_{p2}+C_{H2}}(\Phi_1) = IT - C_{p2}\frac{V_{os1}}{2} = (C_{p2}+C_{H2})\left[V_B(\Phi_1) - V_{CM}\right] \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots...(6)$$

From equation (5) and (6),

$$V_A(\Phi_1) = \frac{-IT + C_{p1}\dfrac{V_{os1}}{2}}{C_{p1}+C_{H1}} + V_{CM} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(7)$$

$$V_B(\Phi_1) = \frac{IT - C_{p2}\dfrac{V_{os1}}{2}}{C_{p2}+C_{H2}} + V_{CM} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots...(8)$$

Also, $V_N(\Phi_1) = V_{OP}(\Phi_1), V_P(\Phi_1) = V_{ON}(\Phi_1)$ and $V_{OP}(\Phi_1) \approx V_{ON}(\Phi_1) \approx V_{CM}$

$$Q_{CF1}(\Phi_1) = 0, Q_{CF2}(\Phi_2) = 0 \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots..(9)$$

(iii) Output Evaluation Phase: In this phase, the charge stored on the holding capacitor is transferred to the feedback capacitor. Let us denote this phase by φ_2. The circuit configuration is shown in fig.41.

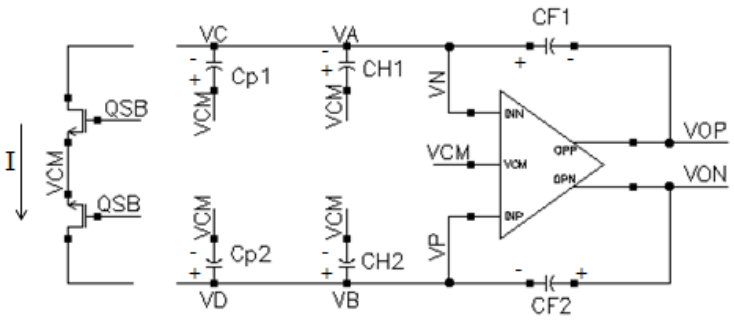

Fig 41: Circuit configuration in Output Evaluation Phase.

The total charge on all the capacitors can be expressed as:

$$Q_{C_{p1}+C_{H1}}(\Phi_2) = (C_{p1}+C_{H1})\left[V_{CM} - V_A(\Phi_2)\right] \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots..(10)$$

$$Q_{C_{p2}+C_{H2}}(\Phi_2) = (C_{p2}+C_{H2})\left[V_B(\Phi_2) - V_{CM}\right] \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(11)$$

$$Q_{C_{F1}}(\Phi_2) = C_{F1}\left[V_A(\Phi_2) - V_{OP}(\Phi_2)\right] \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(12)$$

$$Q_{C_{F2}}(\Phi_2) = C_{F2}\left[V_{ON}(\Phi_2) - V_B(\Phi_2)\right] \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(13)$$

Expression for output voltage of the integrator:

According to principle of conservation of charge:

$$\Delta Q_{C_{p1}+C_{H1}} = \Delta Q_{C_{F1}} \quad \text{.....(14)}$$

$$\Delta Q_{C_{p2}+C_{H2}} = \Delta Q_{C_{F2}} \quad \text{.....(15)}$$

which lead to

$$Q_{C_{p1}+C_{H1}}(\Phi_1) - Q_{C_{p1}+C_{H1}}(\Phi_2) = Q_{C_{F1}}(\Phi_1) - Q_{C_{F1}}(\Phi 2) \quad \text{.....(16)}$$

$$Q_{C_{p2}+C_{H2}}(\Phi_1) - Q_{C_{p2}+C_{H2}}(\Phi_2) = Q_{C_{F2}}(\Phi_1) - Q_{C_{F2}}(\Phi 2) \quad \text{.....(17)}$$

Substituting equations (5), (6), (9), (10), (11), (12) and (13) in equations (16) and (17), we get:

$$V_{OP}(\Phi_2) = \frac{IT}{C_{F1}} - \frac{C_{p1}}{C_{F1}}\frac{V_{os1}}{2} - \frac{(C_{p1}+C_{H1})}{C_{F1}}V_{CM} + V_A(\Phi_2)\left[\frac{C_{p1}+C_{H1}+C_{F1}}{C_{F1}}\right] \quad \text{.....(18)}$$

$$-V_{ON}(\Phi_2) = \frac{IT}{C_{F2}} - \frac{C_{p2}}{C_{F2}}\frac{V_{os1}}{2} + \frac{(C_{p2}+C_{H2})}{C_{F2}}V_{CM} - V_B(\Phi_2)\left[\frac{C_{p2}+C_{H2}+C_{F2}}{C_{F2}}\right] \quad \text{.....(19)}$$

Adding equation (18) and (19), we get:

$$V_{OP}(\Phi_2) - V_{ON}(\Phi_2) = IT\left(\frac{1}{C_{F1}}+\frac{1}{C_{F2}}\right) - \frac{V_{os1}}{2}\left(\frac{C_{p1}}{C_{F1}}+\frac{C_{p2}}{C_{F2}}\right) + V_{CM}\left(\frac{C_{p2}+C_{H2}}{C_{F2}} - \frac{C_{p1}+C_{H1}}{C_{F1}}\right) + V_A(\Phi_2)\left(1+\frac{C_{p1}+C_{H1}}{C_{F1}}\right) - V_B(\Phi_2)\left(1+\frac{C_{p2}+C_{H2}}{C_{F2}}\right)$$

.....(20)

Now if $C_{p1} = C_{p2} = C_p$, $C_{F1} = C_{F2} = C_F$ and $C_{H1} = C_{H2} = C_H$, then equation (20) can be written as:

$$V_{OP}(\Phi_2) - V_{ON}(\Phi_2) = 2\frac{IT}{C_F} - \frac{C_p}{C_F}V_{os1} + \left(V_A(\Phi_2) - V_B(\Phi_2)\right)\left(1+\frac{C_p+C_H}{C_F}\right) \quad \text{.....(21)}$$

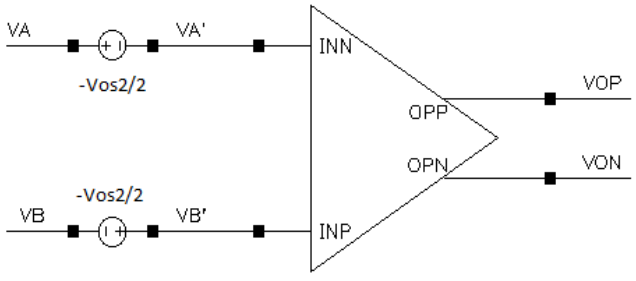

Fig 42: Non Idealities of the Op Amp.

For an op amp, as shown in fig.42, the output voltage can be modeled as:

$$V_{OP}(\Phi_2) - V_{ON}(\Phi_2) = A_v\left[V_B(\Phi_2) - V_A(\Phi_2) - V_{os2}\right] \quad \text{.....(22)}$$

where V_{os2} is the input offset voltage of the op amp and A_v is its open loop gain. From equation (22),

$$V_B(\Phi_2) - V_A(\Phi_2) = \frac{V_{OP}(\Phi_2) - V_{ON}(\Phi_1)}{A_v} + V_{os2} \quad \text{.....(23)}$$

Substituting this value in equation (21), we get

$$V_{OP}(\Phi_2) - V_{ON}(\Phi_2) = \frac{2\frac{IT}{C_F} - \left(\frac{C_p}{C_F}V_{os1} + \left(1 + \frac{C_p + C_H}{C_F}\right)V_{os2}\right)}{\left[1 + \frac{\left(1 + \frac{C_p + C_H}{C_F}\right)}{A_v}\right]} \quad \text{.....(24)}$$

Equation (24) takes into account the non idealities of the op amp i.e. Offset and Gain.The linear relationship between output voltage of the integrator and the time to be measured is not affected by the parasitic capacitances. C_p only affects the offset and the gain error of the system. This offset and gain error are constant for each input delay value. Hence offset and gain error can be calibrated accurately.

So by using proper calibration techniques, the system becomes independent of the parasitic capcaitances of the interconnects between the paths of the two signals.

5. Simulation and Results

The design is simulated in 28nm UTBB-FDSOI technology of STMicroelectronics using ELDO. Simulations are performed at V_{dd}=1V, 0.9V, 0.8V. The design is simulated for all the process corners: FF, FS, SF, SS, TT and at three temperature corners: -40^0C, 25^0C, 125^0C.

The transition time for both CLK and Q1 is 50ps. The delay between occurrences of CLK and Q1 is varied from 300ps to 8ns. The corresponding output count is obtained.

Offset is calculated by setting OFFSET_CHAR_MODE pin to logic '1'. A signal is applied to CLK_OFF pin which goes from LOW to HIGH after an initial delay of 1ns. *Offset* is calculated for all current and capacitor modes. After that *Slope* is calculated by setting SLOPE_CHAR_MODE pin to logic '1'. A known delay of 6ns is applied between CLK_OFF and CLK_OFFD signals (IMODE=0 and CS1=1. CS0=1) and output count is obtained. Using this count value and corresponding offset value, *Slope* is calculated for all current and capacitor modes (using proportionality of all current and capacitor modes) as explained below:

Let us denote the slope for a current and capacitor value as: $SLOPE_{(IMODE,CS1,CS0)}$ and offset as: $OFFSET_{(IMODE,CS1,CS0)}$.

Table 4: Slope Calculation for all Current and Capacitor Modes.

IMODE	CS1	CS0	SLOPE	Multiplication Factor (Fn)
0	0	0	$SLOPE_{(0,1,1)}$*F1	65/5
0	0	1	$SLOPE_{(0,1,1)}$*F2	65/25
0	1	0	$SLOPE_{(0,1,1)}$*F3	65/45
0	1	1	$(COUNT_{known}-OFFSET_{(0,1,1)})/6e^{-9}$	1
1	0	0	$SLOPE_{(0,1,1)}$*F5	3*65/5
1	0	1	$SLOPE_{(0,1,1)}$*F6	3*65/25
1	1	0	$SLOPE_{(0,1,1)}$*F7	3*65/45
1	1	1	$SLOPE_{(0,1,1)}$*F8	3

Let the count obtained for 6ns delay is $COUNT_{known}$, then

$$SLOPE_{(0,1,1)} = (COUNT_{known} - OFFSET_{(0,1,1)})/6e^{-9}$$

Multiplication Factor is calculated as follows:

As explained in section 3.6, slope is given by: I/C.

When capacitor changes from value C1 to C2, then slope will be multiplied by a factor of (C1/C2) and when IMODE changes from 0 to 1, current increases from 1uA to 3uA. So slope will be multiplied by a factor of 3.

Using the slope and offset values obtained, delay between CLK and Q1 is calculated as:

$$\text{Time(Calculated)}=(\text{Output Count}-\textit{Offset})/\textit{Slope}$$

Error in measurement is plotted for all voltage, process and temperature corners with respect to time to be measured (in 28nm UTBB-FDSOI technology of STMicroelectronics) as shown below:

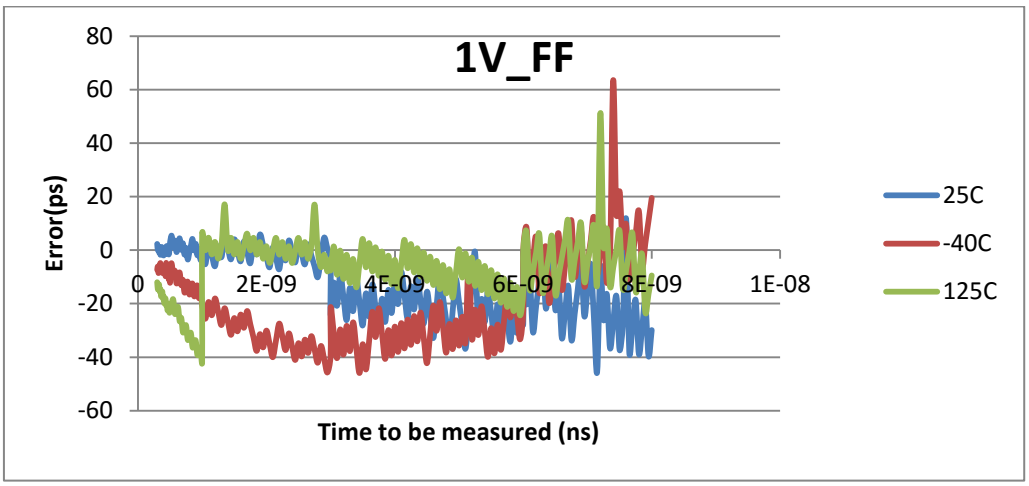

Fig 43: Error vs. Time to be measured for FF Process Corner at V_{dd}=1V.

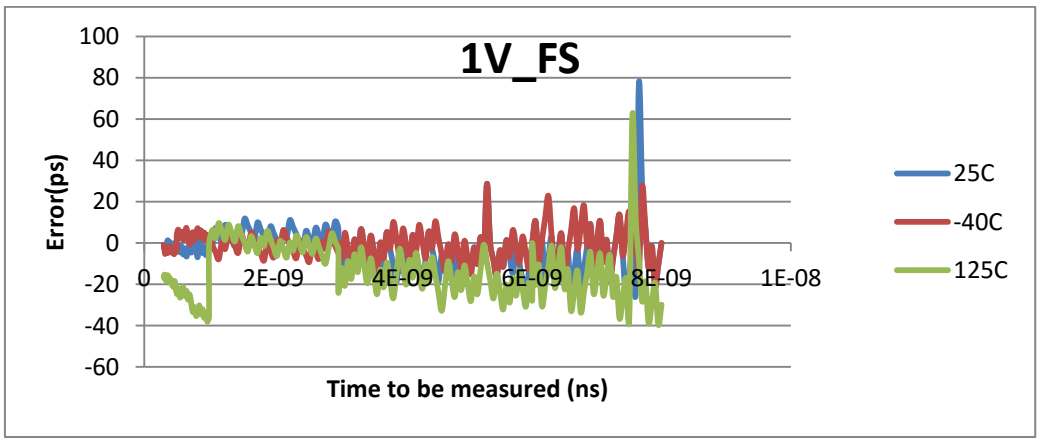

Fig 44: Error vs. Time to be measured for FS Process Corner at V_{dd}=1V.

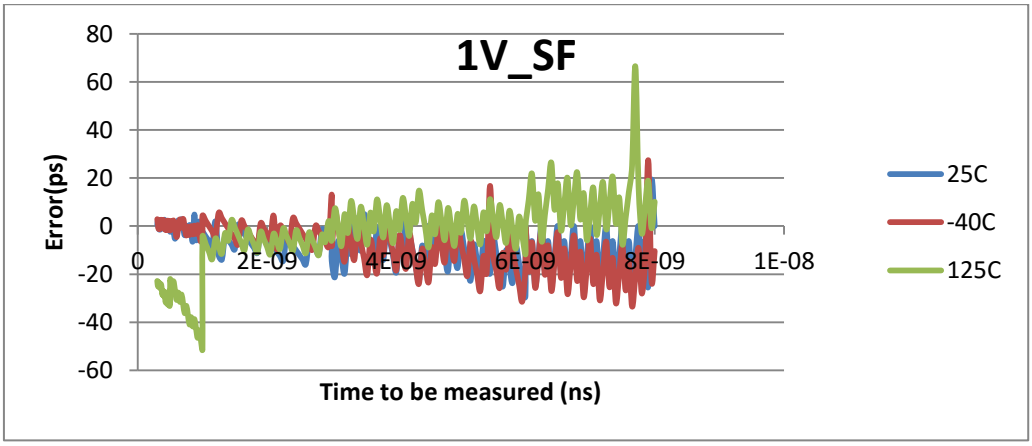

Fig 45: Error vs. Time to be measured for SF Process Corner at V_{dd}=1V.

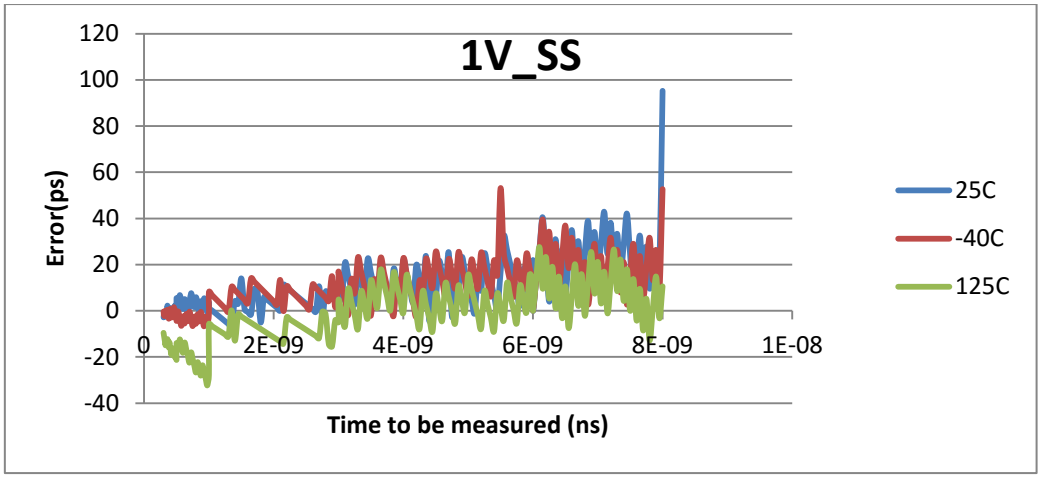

Fig 46: Error vs. Time to be measured for SS Process Corner at V_{dd}=1V.

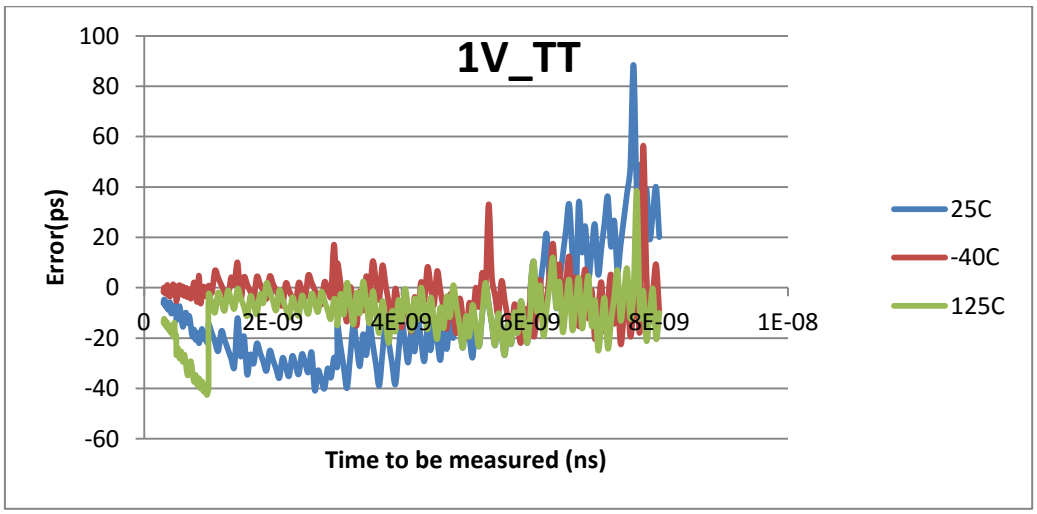

Fig 47: Error vs. Time to be measured for TT Process Corner at V_{dd}=1V.

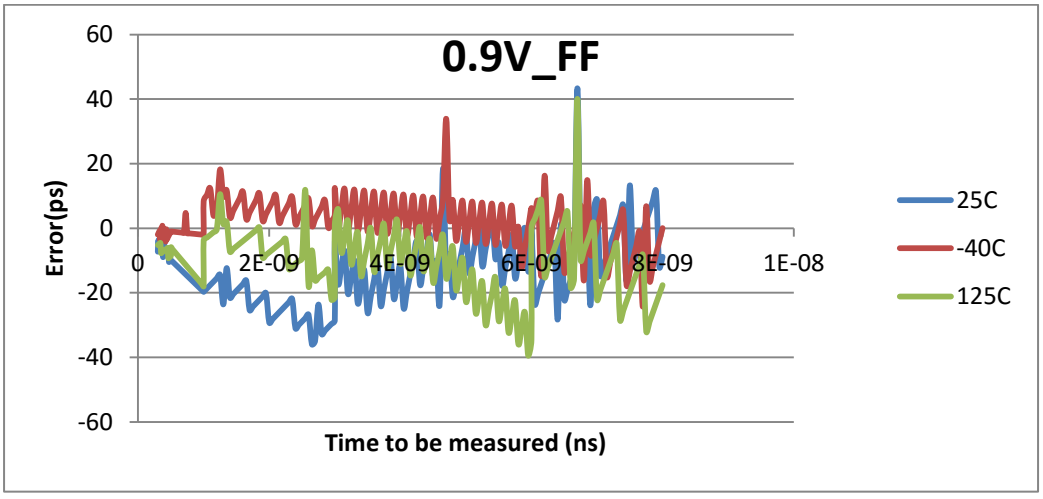

Fig 48: Error vs. Time to be measured for FF Process Corner at V_{dd}=0.9V.

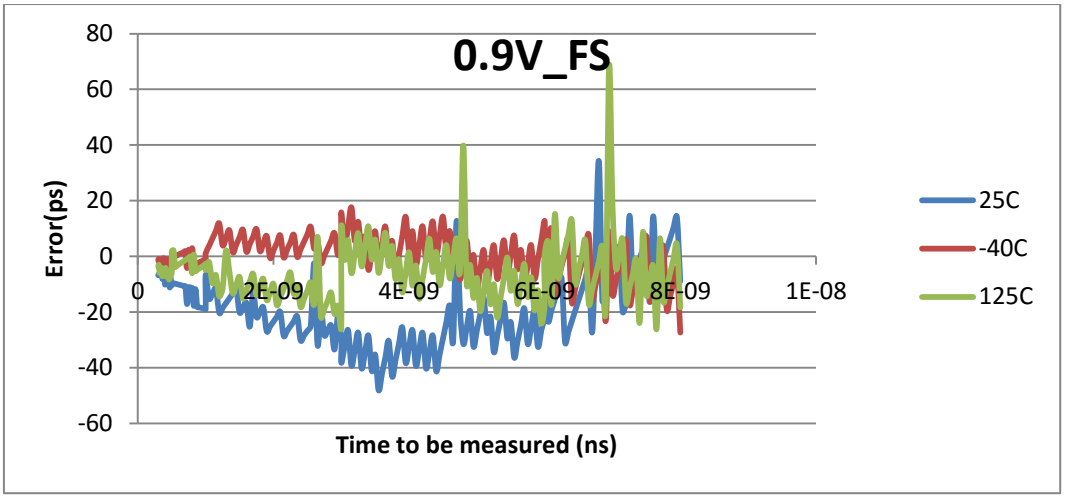

Fig 49: Error vs. Time to be measured for FS Process Corner at V_{dd}=0.9V.

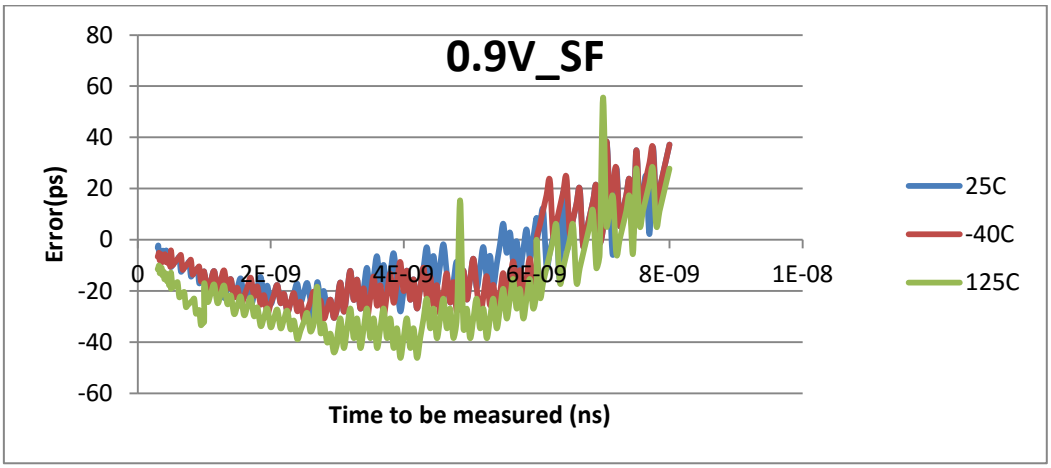

Fig 50: Error vs. Time to be measured for SF Process Corner at V_{dd}=0.9V.

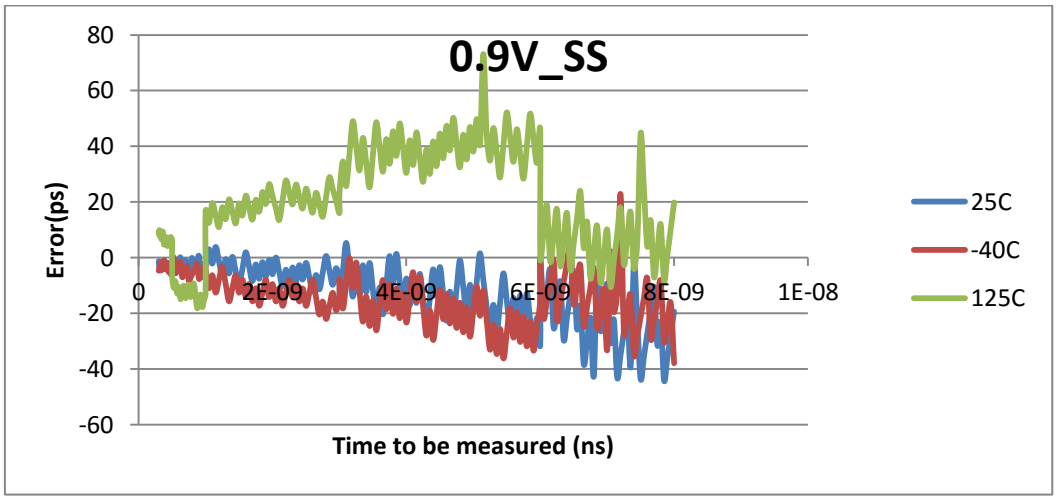

Fig 51: Error vs. Time to be measured for SS Process Corner at V_{dd}=0.9V.

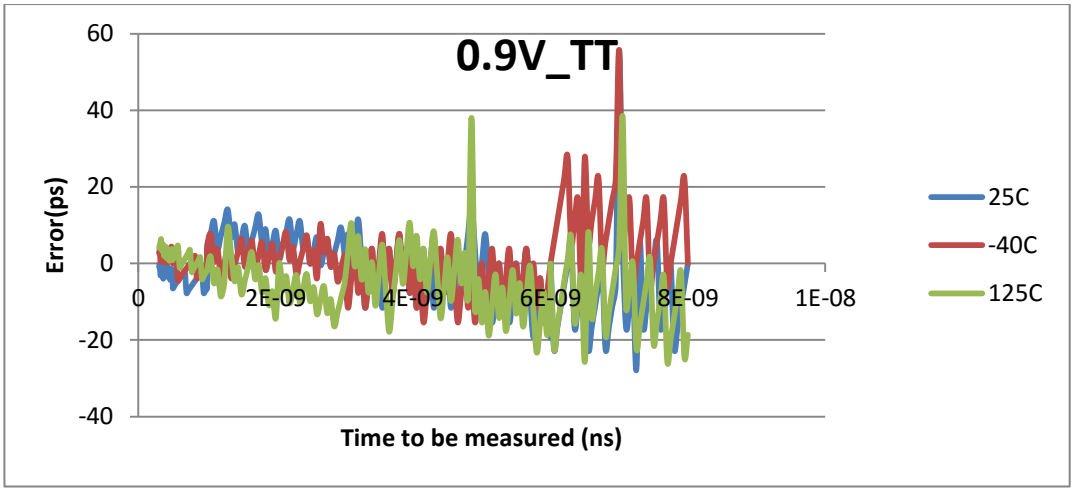

Fig 52: Error vs. Time to be measured for TT Process Corner at V_{dd}=0.9V.

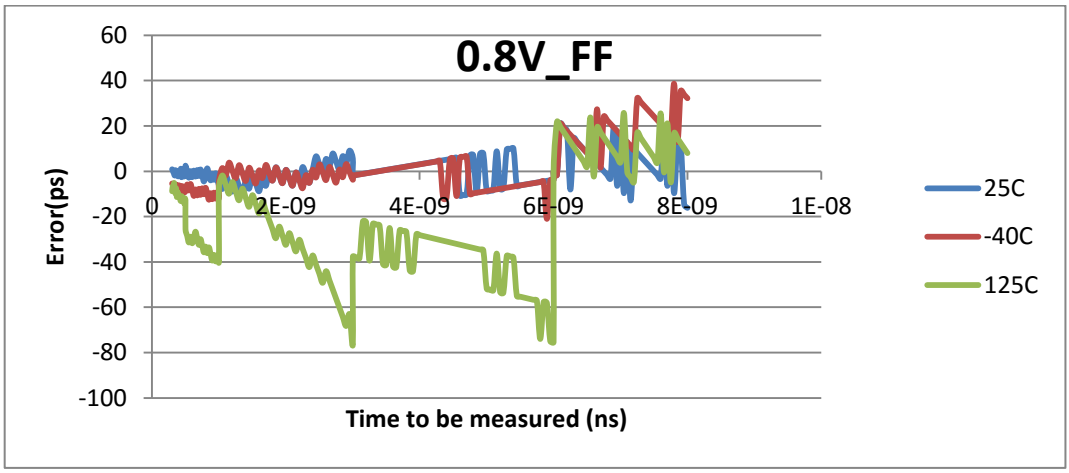

Fig 53: Error vs. Time to be measured for FF Process Corner at V_{dd}=0.8V.

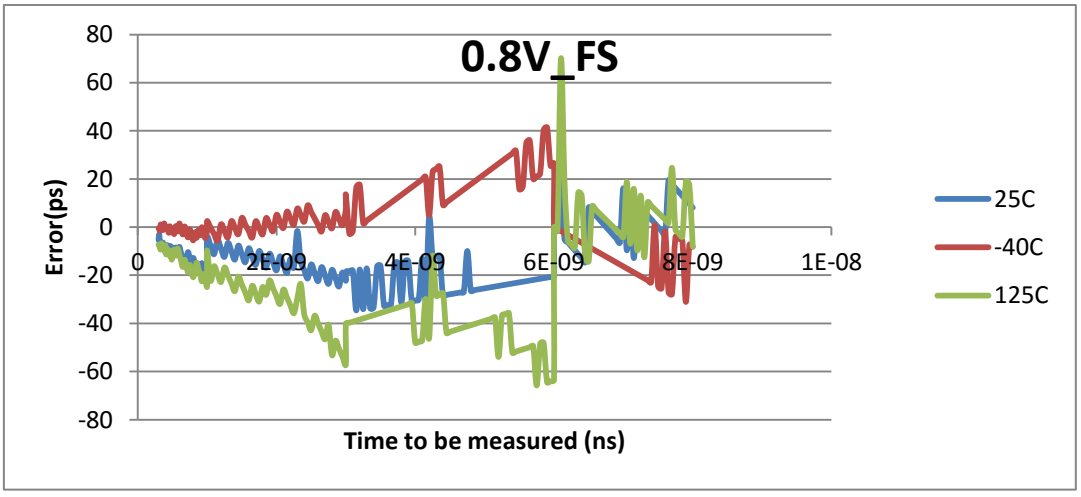

Fig 54: Error vs. Time to be measured for FS Process Corner at V_{dd}=0.8V.

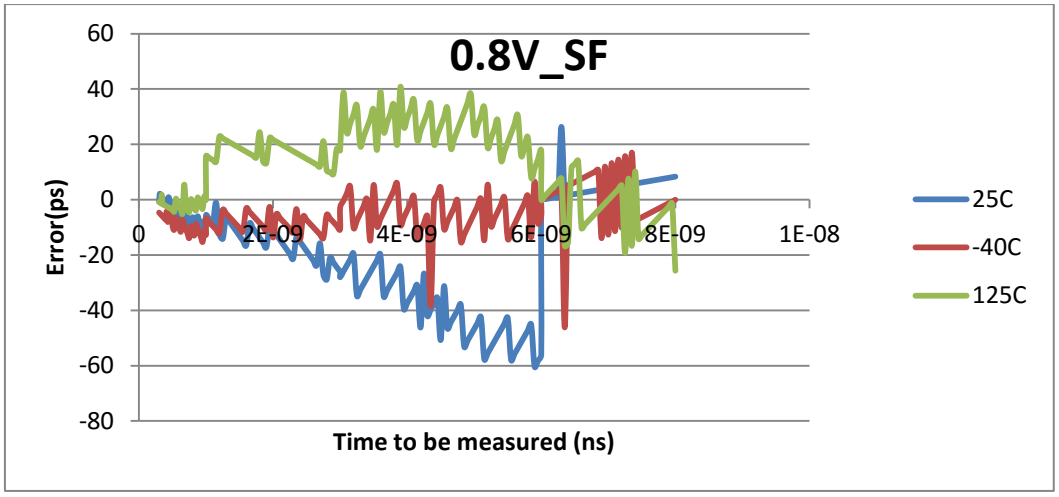

Fig 55: Error vs. Time to be measured for SF Process Corner at V_{dd}=0.8V

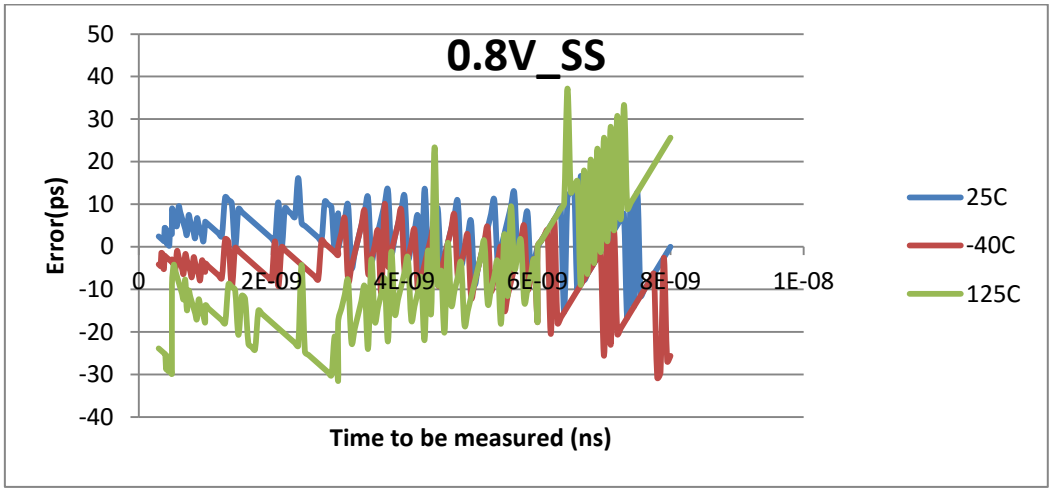

Fig 56: Error vs. Time to be measured for SS Process Corner at V_{dd}=0.8V

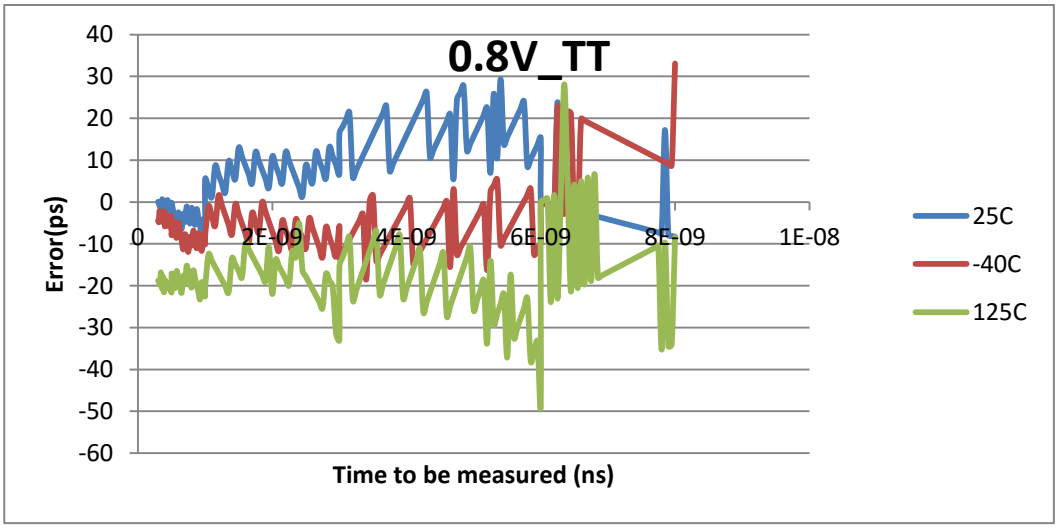

Fig 51: Error vs. Time to be measured for TT Process Corner at V_{dd}=0.8V

From the results it is clear that:

- As the measurement range increases, the resolution of ADC decreases and hence the error increases.
- As V_{dd} decreases, the GBW of the op amp decreases and the settling time of the integrator output increases.
  - At V_{dd}=1V, The integrator output settles within 50ns. So it is able to work at a maximum frequency of 20MHz.
  - At V_{dd}=0.9V, integrator output settles within 100ns. So the system is able to work at a maximum frequency of 10MHz.
  - At V_{dd}=0.8V, the integrator output settles within 200ns. So the system is able to work at a maximum frequency of 5MHz.
- As V_{dd} decreases, the gain of the op amp decreases as well and due to the feedback factor of the integrator circuit, Slope ratios deviate from the ideal values and hence overall error increases.

Table 5 shows the maximum percentage error at V_{dd}=1V for all process and temperature corners.

Table 5: Maximum percentage error at V_{dd}=1V for all process and temperature corners.

Process Corner	**Maximum Percentage Error(at temp=-40^{0}C)**	**Maximum Percentage Error(at temp=25^{0}C)**	**Maximum Percentage Error(at temp=125^{0}C)**
FF	2.67	1.03	4.89
FS	1.66	1.11	5.6
SF	0.969	1.07	8.05
SS	1.144	1.232	4.52
TT	1.098	2.59	5.37

From table 5, it is clear that maximum percentage error obtained is 8.05% at SF corner at 125^{0}C. This happens due to the fact that as temperature increases, threshold voltage of the MOSFET and mobility of the carriers reduce[26]. Both of these effects lead to reduction in gain of the op amp. Due to this, error is more at 125^{0}C as compared to -40^{0}C and 25^{0}C.

This error can be reduced if the *Slope* and *Offset* values are calculated separately for each feedback capacitor and input current mode instead of using one slope value for calculation of the rest of the modes. The maximum percentage error at SF corner and 125^{0}C reduces from 8.05% to 1.88% if the slope values are calculated separately for all current and capacitor modes.

Comparison of previous architectures with the proposed architecture:

Table 6: Comparison of existing architectures with the proposed architecture.

Technique Used	Technology	Minimum Resolution Attainable	Measurement Range
Analog Dual Slope Conversion [1]	0.8µm Bi-CMOS	32ps	2.5µs
Sub Gate Delay Line Quantization [2]	0.35um CMOS	12.2ps	202µs
Pulse Stretching [6]	0.35µm CMOS	50ps	250ns
Time Domain Cyclic Successive Approximation [12]	0.35µm CMOS	1.2ps	327µs
Vernier Ring [13]	0.13µm CMOS	8ps	32.7ns
G_m-C Integrator with SAR ADC [16]	90nm CMOS	11.74ps	6ns
2-D Vernier Delay Line [19]	65nm CMOS	4.8ps	600ps
3-D Vernier Delay Line [21]	0.13µm CMOS	6.98ps	14.2ns
Pulse Shrinking [22]	0.35µm CMOS	40ps	NA
Switched Capacitor Integrator with SAR ADC (this work)	28nm UTBB-FDSOI Technology of STMicroelectronics	3ps	10ns

From table 6, time domain cyclic successive approximation technique achieves a resolution of 1.2ps for a measurement range of 327µs . The design is implemented in 0.35µm CMOS technology.This work achieves a minimum resolution of 3ps with a measurement range of 10ns. The design is simulated in 28nm UTBB-FDSOI Technology of STMicroelectronics.

6. Conclusion

In this dissertation, a new analog type TDC architecture with a switched capacitor integrator is exploited for measuring the access time of memory in which the output voltage of the integrator is independent of the parasitic capacitances of the interconnects in the signal paths. The proposed TDC design has a measurement range upto 10ns. To avoid the dependency of the capacitor voltage on the resistance of the switches, current is given as input instead of voltage. Current given as input to the integrator is generated using a bandgap source. The proposed parasitic insensitive integrator architecture can avoid the non linearity due to parasitic capacitance and improves the resolution of measurement.

Various current and feedback capacitor modes are used for different range of time interval measurement to improve the accuracy of measurement.

The output of the integrator is digitized using a 10-Bit differential SAR ADC. The DAC (Digital to Analog Converter) used in ADC employs a binary weighted switched capacitor array. The reference voltages for the ADC are generated internally from the bandgap reference source using a resistive divider network and decoupling capacitors.

Two modes such as Offset characterization mode and Slope characterization mode are provided for calculation of offset and slope in which two signals with known delay between them are applied externally.

The design is simulated in 28nm UTBB-FDSOI technology of STMicroelectronics for all process (FF, FS, SF, SS, TT) and temperature (-40^0C, 25^0C, 125^0C) corners at V_{dd}=1V, 0.9V, 0.8V and overall error of the system is calculated with respect to the time to be measured. The overall error in measurement depends on the range of time interval to be measured. The error for a measurement range varying from 300ps to 8ns does not exceed 50ps at V_{dd}=1V and 0.9V for all process and temperature corners. But at V_{dd}=0.8V and temperature=125^0C, the error reaches upto 80ps because the gain reduces from 91.82dB (at V_{dd}=0.8V, FFA corner, -40^0C) to 68.64dB (at V_{dd}=0.8V, FFA corner, 125^0C). At V_{dd}=1V, the maximum percentage error obtained is 8.05% at SF corner at 125^0C. So, the error in measurement increases with decrease in V_{dd} and increase in temperature due to reduction in gain of the op amp.

The maximum frequency at which the circuit can operate also decreases with decrease in V_{dd} because of reduction in GBW of the op amp. At V_{dd}=1V, maximum operating frequency of the system is 20MHz which reduces to 10MHz at V_{dd}=0.9V and 5MHz at V_{dd}=0.8V.

7. References

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