Systematic Variation Aware VCO Design

A DISSERTATION

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Submitted by

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CANDIDATE'S DECLARATION

I hereby declare that the work, which is being reported in this dissertation on, "**Systematic Variation Aware VCO Design"**, being submitted in the partial fulfilment of the requirements for the award of the degree of **Master of Technology** in **Microelectronics & VLSI**, submitted in the Department of Electronics and Communication Engineering, Indian Institute of Technology Roorkee, Roorkee, India, is an authentic record of my own work carried out from May 2014 to May 2015 under the guidance and supervision of **Dr. Anand Bulusu,** Associate Professor, Department of Electronics and Communication Engineering, Indian Institute of Technology, Roorkee.

The matter embodied in the dissertation to the best of my knowledge has not been submitted for the award of any other degree elsewhere.

Dated:

Place: Roorkee (Ankush Gupta)

CERTIFICATE

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

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ABSTRACT

Scaling in CMOS technology has proved to be of great significance due to improved performance of design with low area and power requirement. But as we are moving towards lower technology nodes, many layout dependent effects come into picture which tends to impact performance of the design in unwanted manner. Thus it is becoming very important to avoid or reduce the impact of these effects on circuit performance parameters. It has become very necessary to predict these layout dependent effect in the earlier stages of circuit design cycle so that the overall number of iteration involved in circuit designing can be reduced. Many efforts has been done to tackle these problem by either compensating its impact or by modelling these effects. But all these efforts are still insufficient to make circuit systematic variation aware. Thus in this project work, optimisation of Voltage Controlled Oscillator (VCO) performance is done considering layout dependent effects like INWE, STI stress, etc. For the same, analysis of Current Starved VCO has been done and the impact of number of finger (nf) parameter of the MOSFET on device characteristics and thus on circuit performance parameters is analysed. Subsequently, a design methodology to optimize the nf in a multi-finger MOSFET to achieve optimum performance of the circuits has been proposed.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

LDE	Layout Dependent Effects
STI	Shallow Trench Isolation
INWE	Inverse Narrow Width Effect
WPE	Well Proximity Effect
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CSVCO	Current Starved Voltage Controlled Oscillator
TSPC	True Single Phase Clock
GND	Ground
CAD	Computer Added Design
DRC	Design Rule Check
LVS	Layout Versus Schematic
ERC	Electrical Rule Check
LOD	Length Of Diffusion
DIBL	Drain Induced Barrier Lowering
VCO	Voltage Controlled Oscillator

CHAPTER – 1

INTRODUCTION

From the very beginning of semiconductor industry, it has been observed that there comes a large change between the performance predicted during the designing process of any circuit and the performance obtained after physically realising that circuit on semiconductor. This change in performance has always brought a degradation in the value of performance parameters [1]. The cause behind this difference is inability to predict the physical effects of semiconductor accurately while designing the circuit.

It has always been a significant challenge for circuit designers to design a circuit whose performance will not degrade due to physical effects which arises on later stages. This limitation of a circuit design cycle has caused serious disadvantages to semiconductor industries such as less reliable circuits due to change in performance parameters, large time in designing a circuit due to multiple design cycles involved to reduce layout dependant effects, decreased lifetime of circuit due to failure resulting of unpredicted physical effects.

Thus in order to minimise this disadvantages and for improving the efficiency of circuit design cycle it is must to predict layout dependant effects (LDE) on circuit performance parameters beforehand and give some method to compensate for the degradation that will be caused by that layout dependant effects at later stage. Many research work has been done [2], [3], [4], [5] on this issue but yet no proper solution to this problem has been suggested.

Due to various processing effects circuit performance (both power and speed) is dependent on specific layout parameters and can vary by large amount from instance to instance. The accumulated effects can be severe to the point that it may cause the circuit to fail. The fundamental problem is that a device characteristics vary depending on the context, placement, and density of neighbouring devices. The variabilities in devices arises due to two sources of process non – uniformity: local stochastic component and global systematic component. The former is a white noise caused by a stochastic nature of fabrication process. It has no spatial dependence and causes a parameter mismatch for a pair of closely arranged devices. The latter represent a systematic parameter value distribution over the whole wafer which can be caused by either a non-uniform thermal distribution in a fabrication process or

the lens aberration in a photolithographic process. It consist of very low spatial frequency and thus can be regarded as a smooth variation over the wafer. It is very difficult to predict and study local stochastic component but effect of global systematic variations can be studied and predicted with a reasonable level of accuracy.

1.1 Layout dependant effect (LDE):-

There are many post layout effects which vary the performance parameters significantly and thus needs to be predicted beforehand while designing a circuit at pre layout level. Some of them are:-

1. Stress effect: - Unintentional stress as one caused due to Shallow trench isolation (STI) causes change in carrier mobility and thus changes device current.

2. Inverse narrow width effect (INWE): - On decreasing the width of a MOSFET beyond a certain limit results into a gradual decrease in the threshold voltage of the device.

3. Parasitic effect: - There is generation of parasitic capacitors, resistors, inductors, etc. between devices of circuit due to electrical interaction of different layers of layout.

4. Well proximity effect (WPE): - Due to scattering of implant ions from photo-resist defining well edge there is an increase in the threshold voltage and carrier mobility of the MOSFET which is in close proximity of well edge.

There are few other layout dependant effects (LDE) which may also affect circuit performance but their impact is somewhat less than above effects.

1.2 Problem statement:-

It has been seen that changing the number of fingers (nf) of MOSFET in layout while keeping overall width to be constant results in significant shift in the performance parameters. This shift in performance parameters is caused due to some layout dependant effects which arises due to change in number of fingers (nf) of MOSFET. Some of these effects are inverse narrow width effect (INWE), Stress effect and parasitic effect.

Circuit designer vary the nf in a random fashion without any knowledge of what effect it may cause at later stage. If they find any degradation in performance at later stage then they repeat the circuit design cycle with a new value of nf. This results in significant loss of time and

resources. Reason of this limitation in circuit design cycle is that circuit designers currently have no idea of how to vary nf to attain best performance.

Therefore, this dissertation work focuses on predicting effect of changing nf on circuit performance and thus giving an optimum value of nf for each MOSFET which will lead to best performance of circuit. The design under consideration for the purpose of this analysis is Current Starved Voltage Controlled Oscillator (CSVCO) which is an important part of most of the analog and digital circuits. This circuit has been designed in Cadence Virtuoso Tool and analysed using ADE-L, ELDO and HSPICE simulators.

1.3 Organization of report:-

This report has been organised in five chapters including this one which focuses on introduction to layout dependant effects (LDE), their influence on circuit performance parameters and problem statement. Second chapter includes basics of layout design technique which are necessary to understand the problem statement. It also contains analysis performed on the layout of TSPC frequency divide by 2 circuit. Third chapter is dedicated to analysis of Current starved voltage controlled oscillator to understand the effect of varying number of fingers of MOSFET on circuit performance parameters. Fourth chapter includes the proposed design technique for designing of Current Starved Voltage Controlled Oscillator (CSVCO) circuit and improvement in circuit performance parameters obtained by proposed technique. Last chapter contains conclusion and future scope.

CHAPTER – 2

LAYOUT DESIGN TECHNIQUES

Area of layout designing has been one of the most dynamic area of microelectronics industry due to ever reducing technology nodes. Also many new physical effects arises as we go down on technology nodes. Designing on advanced IC technologies are also affected with new problems such as large process variations and the dependency of the circuit performance on the physical layout parameters such as well proximity effects and stress effects. Due to this high market demand and effects of the new technologies, more and more challenges are coming in front of the layout design engineers because of which the amount of 'first-time-right' designs has dropped at every new technology node.

Analog designs often includes devices which should be ideally matched for correct operation of the circuit (such as transistors in differential pair). Layout dependant effects can vary their performance characteristics and thus can cause mismatch. To avoid this mismatch we need to adopt some techniques. On the other hand, in digital circuits operating at very high frequency, timing parameters becomes critical and has to be taken care at the layout design level.

2.1 Fundamentals of layout designing: -

To completely understand the concept of layout designing, one has to know about basic components that are used in layout designing. Knowledge of these fundamental points is must before starting to make layout of any circuit. This fundamental blocks includes different materials used in semiconductor industries, different layers used in layout and their order in a layout, different rules followed while drawing layouts, etc.

2.1.1 Different types of layers used in layout: -

1. Conductors: These layers are conducting layers which simply means that they are capable of carrying signal from one place to another. Metal, polysilicon layers, diffusion areas and well layers fall into this type of layers.

2. Isolation layers: These layers are the insulating layers that are used to isolate different conductor layer from each other in horizontal and vertical directions. This isolation is must in both the horizontal and vertical directions to avoid “short-circuits” between different electrical nodes.

3. Contacts or vias: This name is given to the layers which are cuts in the insulation layer that separates conductor layers and allow the lower layer to contact up through the cut or by the contact hole made in insulator layers. Metal vias or contacts are examples of these. Openings made in the passivation layer for bonding pads is also an example of a contact layer.

4. Implant layer: These layers do not itself define a new layer or contact, but change or customize existing conductor properties. For example, active or diffusion areas for NMOS and PMOS transistors are defined simultaneously. An N+ mask is used to create N+ implant areas that define certain diffusion areas to N-type by the use of an N-type implant and similarly for P-type implant as well.

2.1.2 Layout design rules: -

Depending upon the maximum and minimum physical dimension limit of any technology node each technology has its own set of design rules which must be followed while designing layout in that technology node so that it can be physically realised on semiconductor chips. In a general sense, these layout design rules can be divided into following categories: -

1. Width rules: - The minimum width of any polygon is a critical dimension as it defines the limit of the manufacturing process. For example the minimum gate length of a transistor follows this rule. Any violation in a minimum width rule will potentially results in an open-circuit in the offending layer. In that case the manufacturing process will not reliably produce a wire or continuous connection below a specific value, and breaks in the path will arise at the point at which the width rule was not followed.

In addition to single polygons, width rules can also be applied to structures such as transistors, simple devices or to single polygons with electrical or other special characteristics. An example of a structure with special electrical characteristics is a conductor layer that is connected to a power supply. The more current that pass through these conductor necessitate that they have a width greater than the minimum design rule, and in that case the correct value will depend on the size of the current rather than being a fixed value. Heavy currents passing through a narrow metal track may cause the track to act like a fuse, and over

time or during a large current peak the conductor polygon will break under the effect of over current.

2. Length rule: - The length of a path is usually unlimited, but in some processes there are rules defining minimum area requirements of a layer due to which there exist an implicit limit on minimum length of the layer if there is no scope to increase its width.

3. Space rule: - Another critical rule in layout designing is the space rule, which defines the minimum distance between two polygons of layouts. Generally, the space rules are applied to avoid any unwanted short-circuit between the two polygons.

When combined with the width rule on a single layer the space rules define a layer pitch. The pitch of a layer is of much importance while considering interconnect and routing. The routing area consumed by metal lines is conveniently calculated by multiplying the number of lines by the layer pitch.

4. Overlap rule: - As it is obvious from the name itself, the overlap rule defines the minimum overlap or surround of one polygon by another polygon. For example, the overlap of a metal layer with via or contact comes under this rule. These rules always involves polygons existing on different layers of layout, and this fact is the key reason behind the requirement of this type of rule. Whenever structures are manufactured using polygons on different layers, there is significant chance that there may be a misalignment between the actual and desired relative placements of the two polygons. Misalignment between polygons may result in both undesired short and open circuit connections, depending on the involved layers. Basically, overlap rules are used to reduce the impact of a small misalignment between different layers in the manufacturing process by making sure that the desired connectivity is maintained.

2.2 Layout design flow: -

In order to make a good quality layout, proper planning of complete design cycle is must. While designing layout for any given circuit, a designer must analyse input requirements for specification of circuit and output requirements to make sure that layout requirements match with it.

In a general sense, we can divide a layout design cycle into four steps: Define floorplan, Implement the design, Layout verification, Final steps as shown in fig. 2.1.

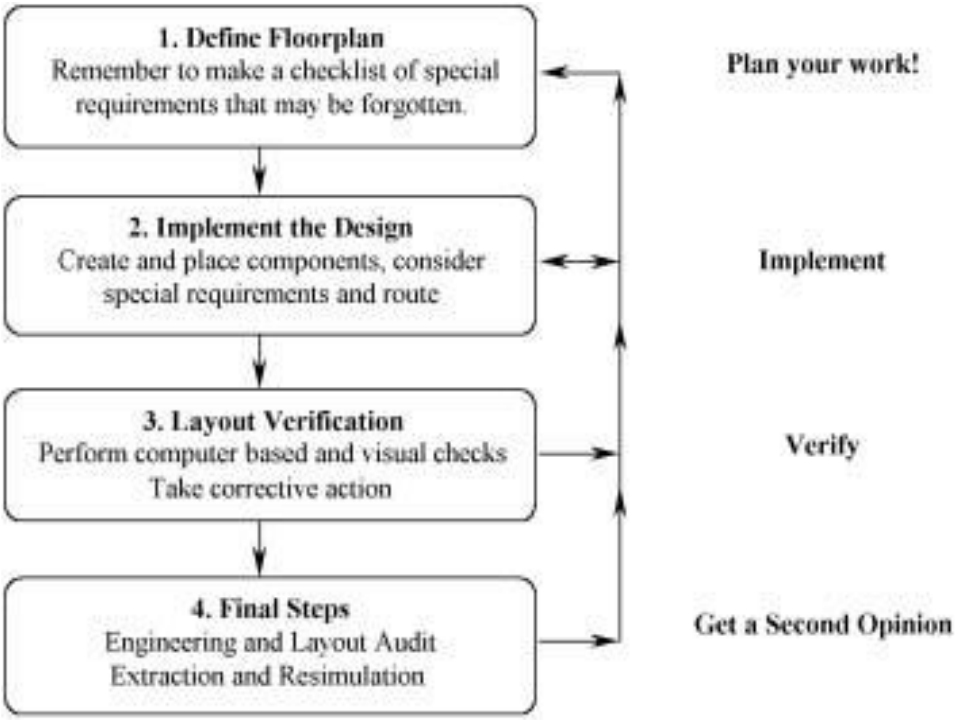

Fig 2.1 Layout design flow.

(Ref.: Dan Clein, "CMOS IC layout: Concepts, Methodologies and Tools", Edition 1999, Butterworth Heinemann prints.)

Step 1. Define floorplan: -

First step of layout designing is defining floorplan depending upon the number of signals involved in the circuit and their routing requirement. Floor-planning is basically an interface between layout designer and circuit designer. Primary concern is to minimize area requirement and congestion while maintaining physical design limitations. It can be further sub-divided into following four steps:-

1.1 Firstly we focus on position and routing of power supply and ground (GND) line. We also decide width of power and ground lines depending upon amount of current they will be carrying at most. In this step we also focus on number and position of well and substrate contacts that will be made to power and ground lines.

1.2 Second steps involves positioning of signals on layout depending upon their interface to external world. This also involves routing of these signals and defining their width depending upon current strength that they will be carrying. Special attention is required to be given to some signals like Clock signal, shielded signals, buffers of multiple bits which needs to be matched, etc.

1.3 This step involves special specifications of layout like symmetricity of layout, or making a portion noise immune, shielding a section from effects of other section, providing protection against latch-up issues, etc.

1.4 This is one of the most important part of layout designing and consist of most of the effort involved in layout designing. It involves major issues like deciding size of blocks of circuit, their placement depending upon signal routing involved, checking whether size requirement is meeting or not, deciding hierarchy of layout design, deciding number and types of layers needed to make layout of given design, etc.

1.5 Last step is a cross check to see if all the given specifications are met or not and checking the sanity of design.

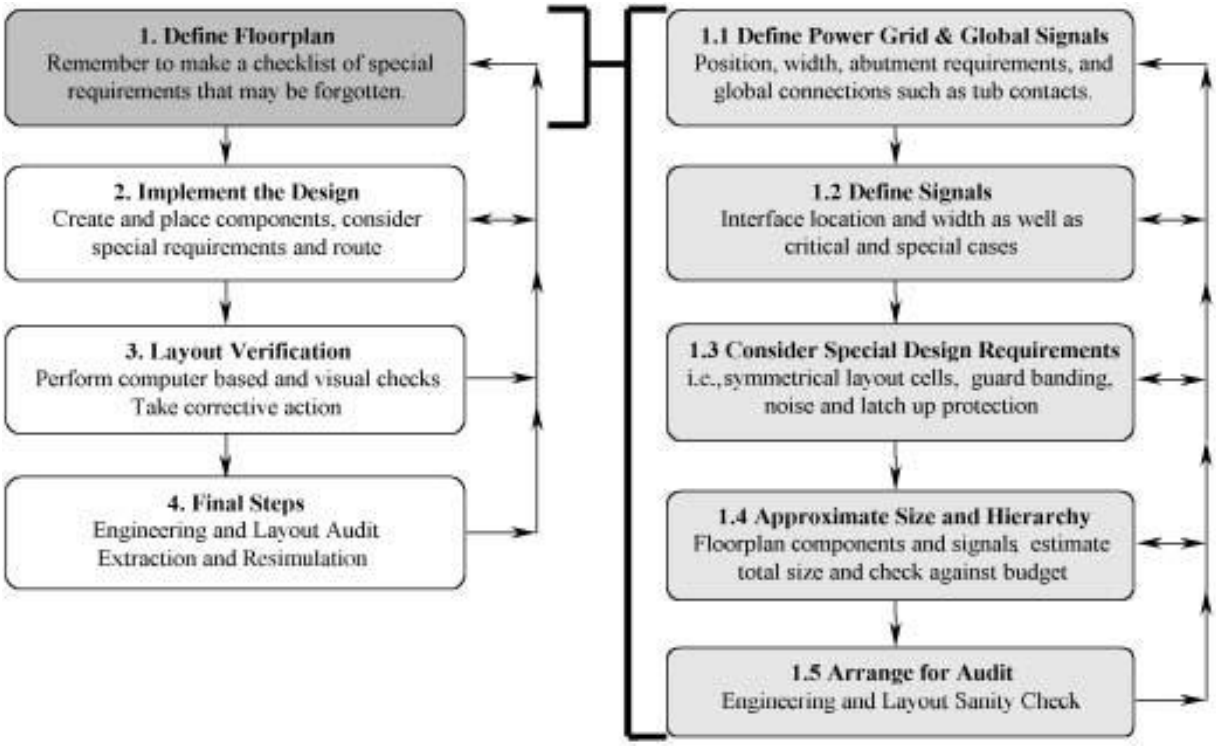

Fig 2.2 First step of layout design flow.

(Ref.: Dan Clein, "CMOS IC layout: Concepts, Methodologies and Tools", Edition 1999, Butterworth Heinemann prints.)

Step 2. Implement the design: -

After planning the layout of given circuit in first stage, the next step is to implement that design based on the planning done. While starting with the second step it is necessary to keep in mind all the layout techniques as this step involves efficient use of all those techniques. This step can be further sub-divided into four steps as follows: -

2.1 In this step we create all the components required in our design and place them according to the floorplan decided in first step.

2.2 In second step we move towards finer details of layout drawing such as placement of critical path signals, achieving layout symmetry, precise placement of components, latch-up and noise protection, substrate contact, etc.

2.3 Last step is to connect all nets using interconnects while giving special attention to critical nets.

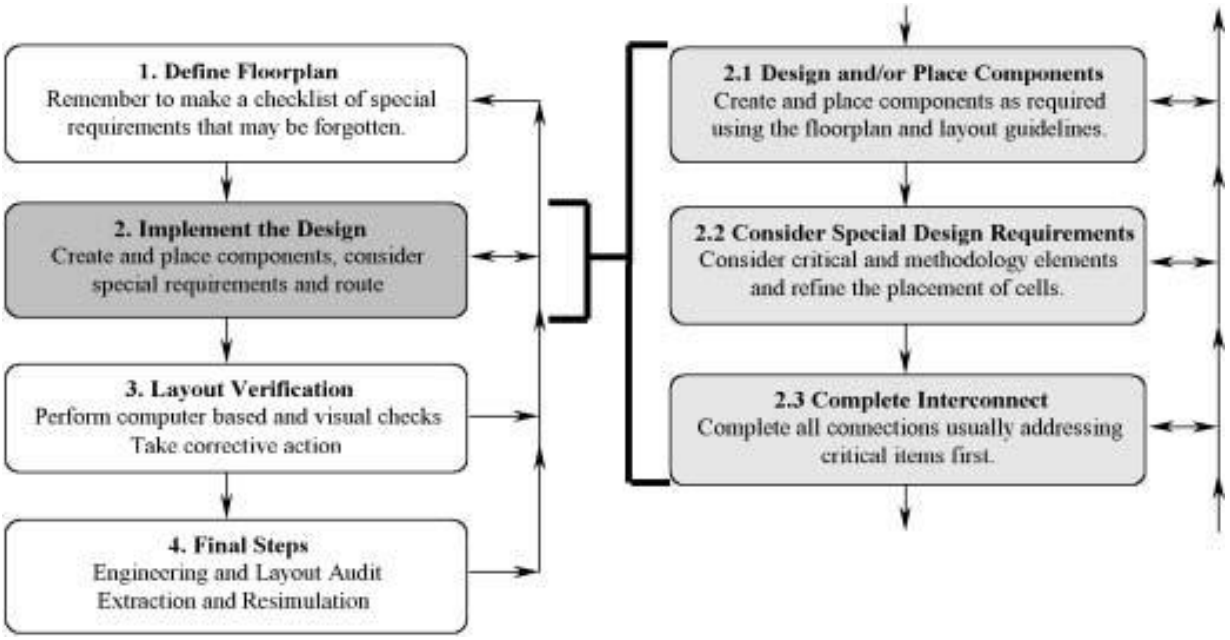

Fig 2.3 Second step of layout design flow.

(Ref.: Dan Clein, "CMOS IC layout: Concepts, Methodologies and Tools", Edition 1999, Butterworth Heinemann prints.)

Step 3. Layout verification: -

Once drawing of layout is completed in second step, next step is to verify the design. This is a very important step as many mechanism tends to fail the realisation of circuit on chip. It is an automated check step done mostly with the help of CAD tools. This step can be further sub-divided into four steps where each step involves a particular type of check that is to be applied on layout to avoid any failure mechanism that may arise due to any error in layout design: -

3.1 First step is Design Rule Check (DRC). In this step we check that whether all layers and polygons drawn in our layout follows manufacturing process rules or not. This rule ensures that the design is under the manufactural limit.

3.2 Second step is Layout Versus Schematic (LVS) check. In this step we verify that all the connections of our design is made correctly or not. Connections of layout is checked against the connections made in schematic considering it as the reference. This step also checks the number and size of the devices made against their number and size in schematic.

3.3 Third step is Electrical Rules Check (ERC). This steps involves checking of any short circuit, redundant device, partly or unconnected device, floating nodes, etc. This step is becoming less important as most of this checks falls under LVS check as well.

3.4 Last step is to make a visual inspection of the layout. This is done to ensure that the design follows required geometry, size requirement, etc.

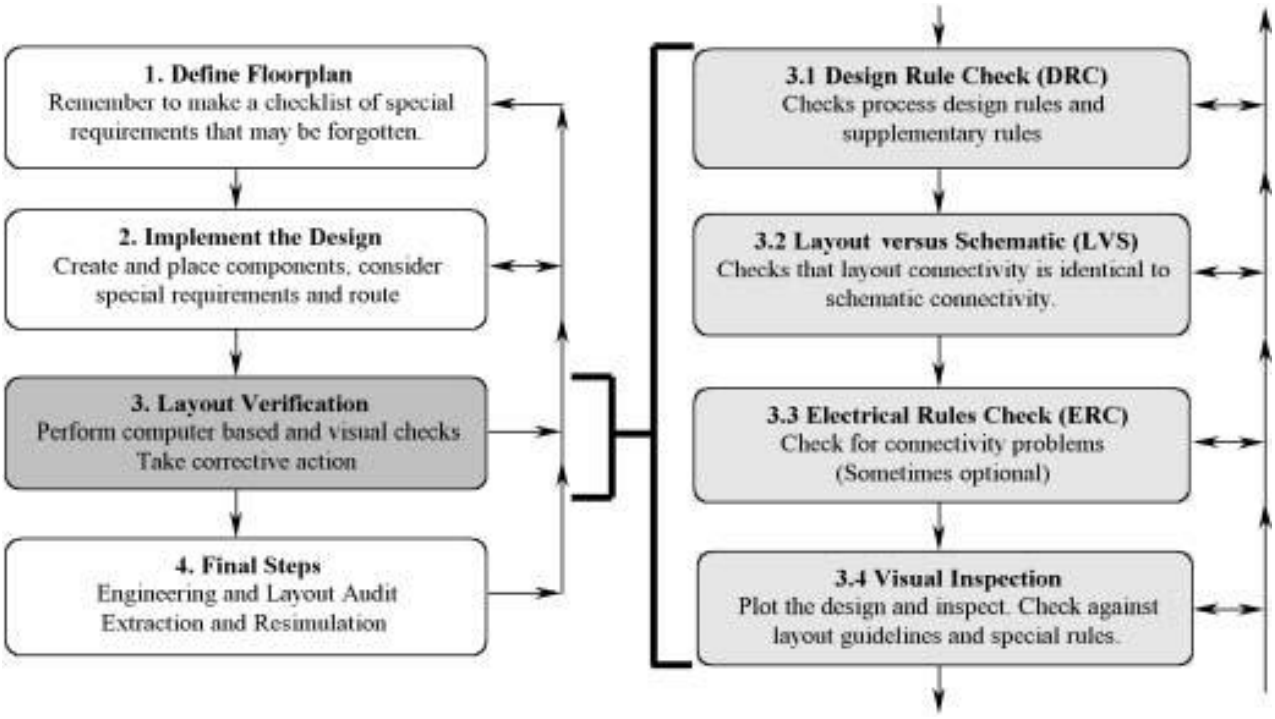

Fig 2.4 Third step of layout design flow.

(Ref.: Dan Clein, “CMOS IC layout: Concepts, Methodologies and Tools”, Edition 1999, Butterworth Heinemann prints.)

Step 4. Final Steps: -

Due to ever reducing technology nodes and increasing physical effects coming into picture, layout designs are becoming more and more complex with time. As the complexity of designs increases there is lot of scope involved for the improvement of design. Even after considering all rules and techniques while designing there may be some changes remaining to make design better. For this purpose there must a checking of layout done by some experts. This check also ensures that the automated checking involved in third step is done properly by CAD tools.

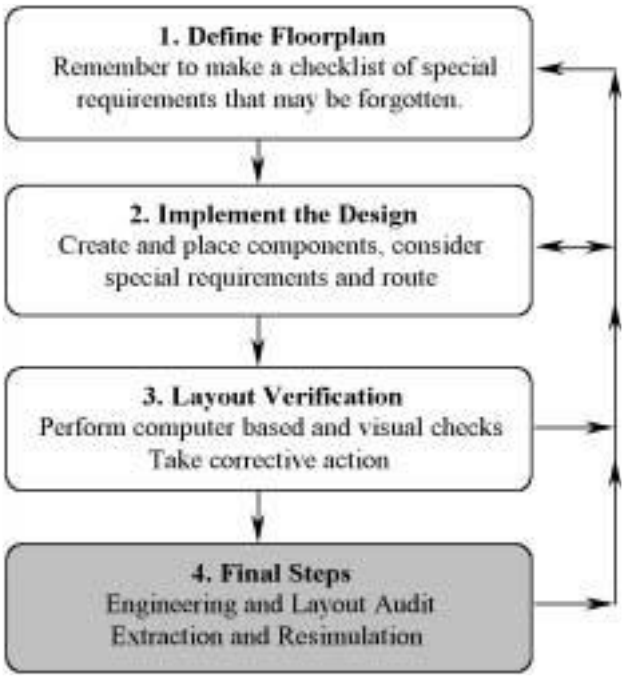

Fig 2.5 Last step of layout design flow.

(Ref.: Dan Clein, “CMOS IC layout: Concepts, Methodologies and Tools”, Edition 1999, Butterworth Heinemann prints.)

2.3 Issues of layout designing: -

It has been seen that as we move towards lower technology nodes, many physical effects starts to come into picture. While drawing layout for any circuit these effects must be taken into consideration else they may result into variation in circuit performance parameters, unwanted operation or in severe case complete failure of the design. This section deals with such types of issues involved in layout designing.

2.3.1 STI stress effect: -

As we are moving towards the lower technology nodes the mechanical stress, which was used a secondary concern of the circuit design, has now become one of the major factors determining the circuit performance. As compared to other intentional mechanical stresses, STI stress, which arises due to STI wells on active region of the device, is formed inevitably and has increasingly important impact on the device behaviour, especially in aggressively scaled-down CMOS technology. STI stress arises due to thermal mismatch between Si-SiO2. It depends on STI well size and device diffusion and gate length and is compressive in nature.

Major effects of STI stress on device characteristics are change in Mobility which directly affects device current, change in the leakage current of the device. To model stress in layout mostly Sa and Sb parameters are used and which defines LOD parameter for a device and thus helps in calculation of stress as shown in fig. 2.6.

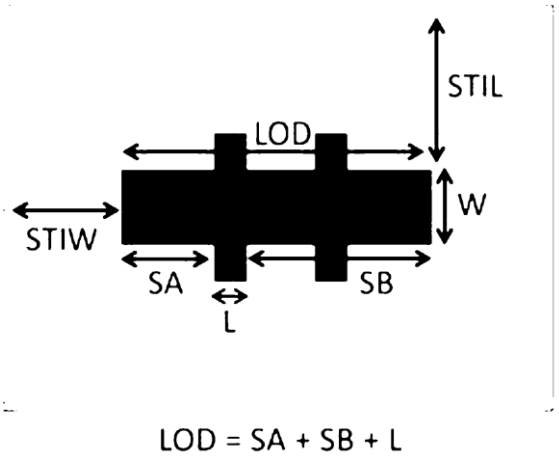

Fig 2.6 Figure showing parameters which defines LOD parameters and stress.

On varying the number of fingers (nf) of MOSFET, it has been seen that the effect of stress is reduced on the fingers located inside due to shielding from fingers at the edge, as a result of which the device current tends to increase. Following fig 2.7 shows this increase in current versus number of fingers for NMOS and PMOS (Vdd = 0.5 V, W = 1 μm, L = 0.06 μm): -

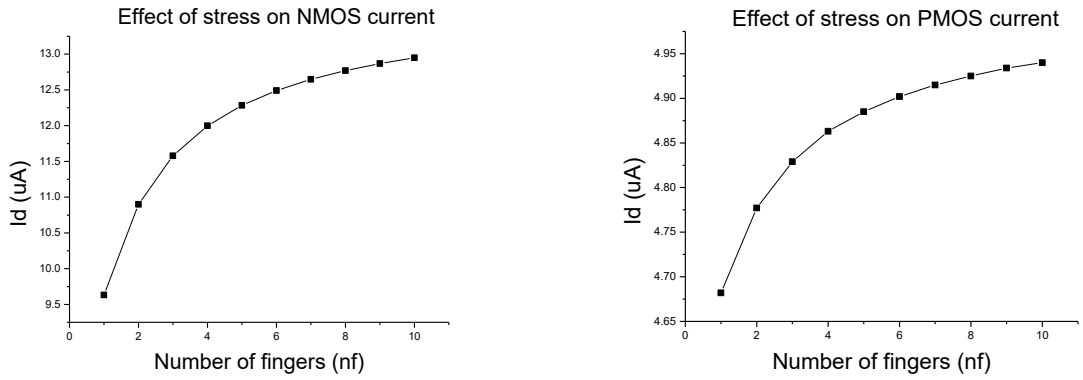

Fig 2.7 Figure showing effect of stress on NMOS and PMOS current.

2.3.2 Inverse narrow width effect (INWE): -

Inverse narrow width effect (INWE) arises due to the parasitic transistor formed at the sharp corner of shallow-trench isolation (STI) process. The geometrical effect of the corners in STI process results in the turning ON of the parasitic transistor at lower voltages compared to main channel. When the width of the transistor decreases, the contribution of parasitic corner transistor increases to the whole transistor performance. Due to which the threshold voltage becomes lesser for transistor with narrow width.

Usually the inverse narrow width effect (INWE) is studied in the super-threshold region and it was seen that the INWE is less critical compared to the DIBL. But in the near/sub-threshold region operation, the effect of DIBL is not strong compared to its effect in the super-threshold region because the drain-to-source voltage is low while the inverse narrow width effect is significant. Moreover, the current becomes exponentially dependent on the threshold voltage in the near/sub-threshold region, which amplifies the impact of the inverse narrow width effect on the current.

One of the most important parameter of layout designing is number of fingers (nf) of MOSFET. In a general sense, varying the number of fingers of MOSFET doesn't change its width so it is expected that the current through the device should remain constant but on examining closely it is seen that if by increasing the number of finger, the width of each finger enters in the range where INWE starts to affect significantly then it results in decrease in threshold voltage resulting in increase in device current (even with width of device kept constant) as shown in fig. 2.8: -

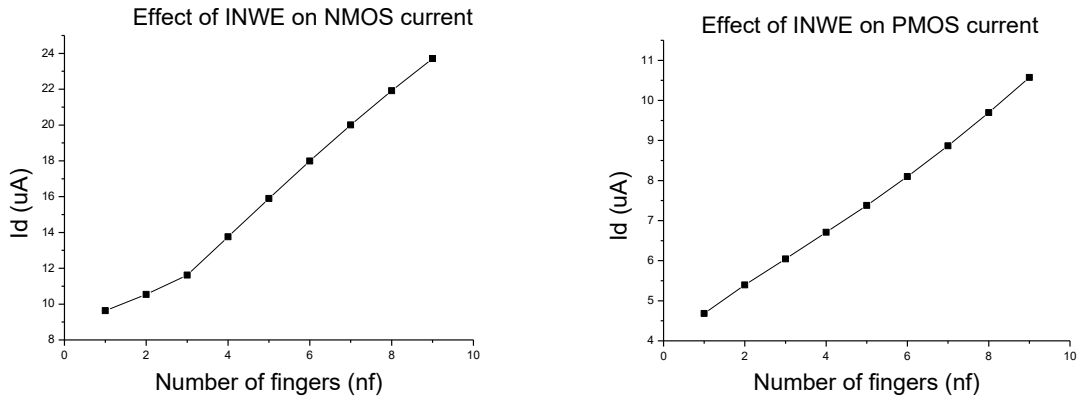

Fig 2.8 Figure showing effect of INWE on NMOS and PMOS current.

2.3.3 Well proximity effect (WPE): -

Well proximity effect (WPE) is used to define the parameter which deals with the scattering of the doping ions in the process of deep well implants, scattered from the edge of the photo-resist used to define the boundary of well. It mainly affects devices which are kept close to the well edge and has no significant effect on devices away from well edge.

Major results of this effect is to raise the threshold voltage of the devices kept closer to well edge. This effect of scattering from the edge of well falls off rapidly as we move device channel region away from the edge. Usually three parameters are used to quantify this effect: SCA, SCB and SCC. This effect can be avoided by setting design rules for minimum distance between active devices and well edge.

2.3.4 Antenna effect: -

The plasma based process involved in the fabrication of any chip tries to charge the conducting parts of the fabricated structure which in turn may result into the degradation of the quality of SIO2 used as thin gate oxide. Charges collected from the plasma based process results into current in gate oxide which is higher near gate oxide defects. As a result of this current more traps sites may generate and thus these traps will amplify current in gate oxide. It its most severe form above phenomenon may result into an early breakdown of gate oxide or affect the threshold voltage of the transistor.

This phenomenon occurs only when metal or poly layers, which are not covered by an oxide shielding layer, is exposed to plasma and also that it is not connected by a previously formed

P-N junction to the substrate. It is generally seen that charge formation due to plasma process appears to be critical only at the point of manufacturing when each conducting connections do not form an equipotential layer at the end of etching.

An antenna can be understand as an interconnect (like metal or polysilicon) which is not connected to silicon electrically (not grounded) during manufacturing steps of the chip. Normally an electrical path is provided to silicon in order to discharge any accumulated charge. But if it is not the case then there may be a build-up of charges on the interconnect to the limit when fast discharge will take place and leads to permanent physical damage to gate oxide. This phenomenon of destruction of gate oxide is referred as Antenna effect.

To quantify the chances of occurring of antenna effect in any design a parameter called as Antenna Ratio is used. It is the ratio of the physical area of conductor in the antenna and the total area of gate oxide which is connected to antenna electrically. A higher value of antenna ratio shows a higher probability of design failure due to antenna effect. It is either due to relatively greater area for charge accumulation or due to lesser area of gate oxide on which accumulated charge is concentrated.

It is generally seen that metal layers creates more antenna problem than poly layers. The breakdown of gate oxide in antenna effect is mainly due to the tunnelling current.

There are many techniques proposed to avoid antenna effect while designing a layout. Some of these techniques are use of jumper between different layers of metals, use of dummy transistors, connection of protection diode (R.B. diode) at the gate of MOSFET, etc.

2.3.5 Latch up

Latch up is defined as the condition when any semiconductor device operates in a high current state due to interaction of a NPN and a PNP bipolar transistor. These NPN and PNP bipolar transistors can be formed due to natural behaviour of technology or as a parasitic device. In case of a CMOS technology, these transistors are formed as parasitic devices.

In CMOS technology, for each PMOS formed there is generation of a PNP bipolar transistor between P- channel diffusion, N-well and P type substrate. Similarly, for each NMOS formed there is a NPN bipolar transistor between N-channel diffusion, P type substrate and N-well used in PMOS.

Whenever there is an interaction between these NPN and PNP bipolar transistors, there is formation of a regenerative feedback between the two transistors which leads to electrical instability. This interaction of three region PNP and three region NPN which are having common collector and base regions can also be viewed as four region PNPN device. As a result of this feedback, there exist a stable and an unstable region in the I-V characteristics of the device. The resultant I-V characteristics has an S- type shape with two conditions: High voltage low current and Low voltage high current. This PNPN device gets turned ON in a high current state in which it flows high current at very low voltage resulting in a low impedance shunt.

Whenever this parasitic PNPN device operates in high current state, it can lead to thermal runaway which can be destructive. This can cause harm to a circuit, chip, system or package.

Thus in order to reduce problem of Latch-up, main idea is to reduce the resistance between power grid (Power supply and ground lines) and substrate or well. But the magnitude of these resistance depends directly on the distance of P-tap (or N-tap) from P-substrate (or N-well). Thus in order to avoid the issue of latch up each design technology defines a design rule that P-tap (or N-tap) should be kept within a defined maximum distance to limit this resistance within permissible limits.

2.3.6 Electro-migration: -

It can be defines as the physical dislodging of ions in a conductor as a result of continuous flow of current which may lead to open circuits in the path. This phenomenon is more observed where wires operates under heavy current densities. It can be seen as an ageing issue and is more seen in case of continuous DC current flow as opposed to AC current flow as in case of AC current keeps on changing its direction after each cycle and thus ions more or less remains at their position.

2.4 Analysis of TSPC frequency divider circuit: -

In order to gain a better understanding of impact of layout dependant effects (LDE) on device characteristics and circuit performance parameter analysis of TSPC frequency divider circuit is done. It is very basic component and gives fairly good idea about layout dependent effect on other larger blocks. . It is basically a D flip-flop with its inverted output connected back to

its D input while feeding signal whose frequency has to be divided to the clock (clk) input of d flip-flop, where D flip flop is realized using TSPC design technique, as shown in fig. 2.9: -

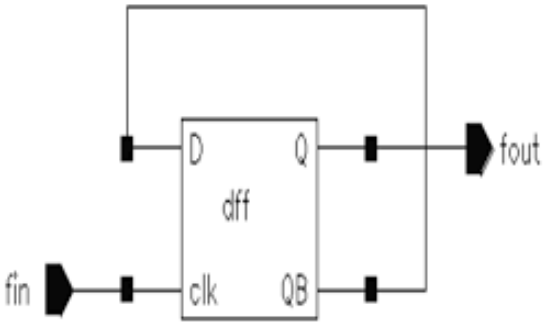

Fig.2.9 Frequency divide by 2 circuit using D flip flop.

Following fig 2.10 shows the schematic of the frequency divider circuit used which involves some modification to the basic block like adding clocked keeper cells at critical nodes to improve low frequency operation, using buffers to reduce loading effect on clock signal line, etc. in order to improve the performance:

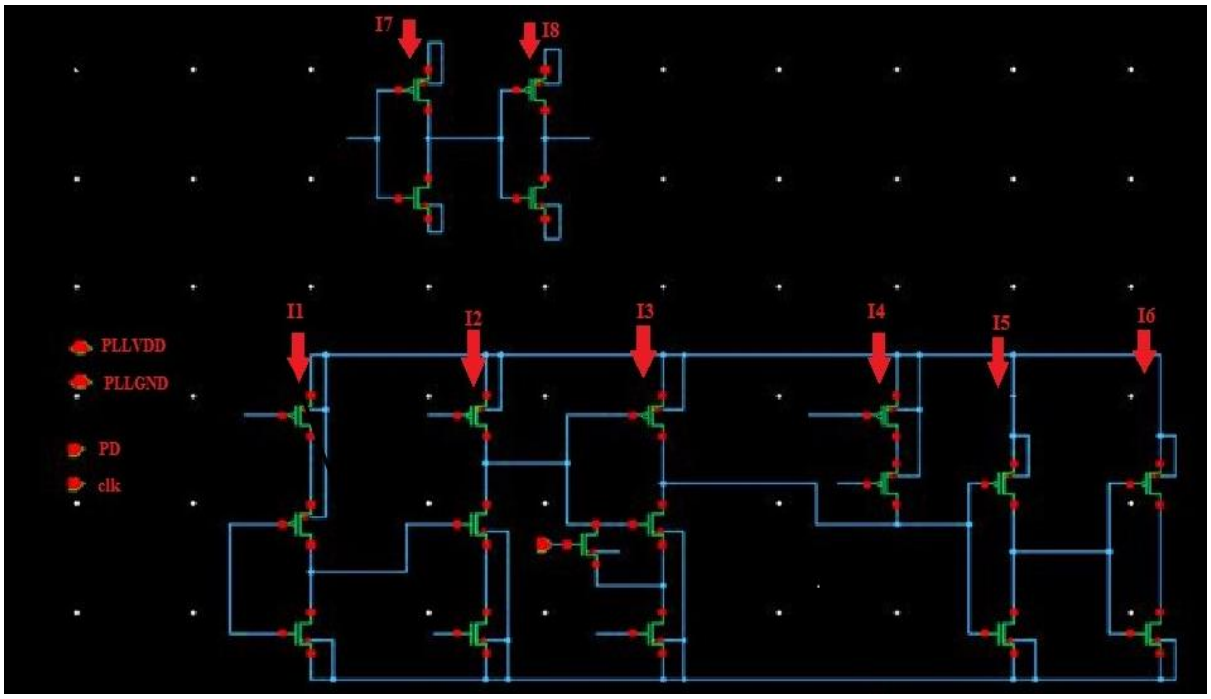

Fig.2.10 Schematic of TSPC Frequency Divide by 2 circuit used in our analysis.

2.4.1 Simulation setup: -

Here Cadence Virtuoso Tool is used for design generation and Eldo Simulator is used for performing parametric analysis. Other parameters of analysis is as follows: -

Technology Node = STMicroelectronics 65 nm

VDD (min) = 1.1 V

VDD (max) = 1.3 V

Temp. (Min) = -40 deg. C.

Temp. (Max) = 125 deg. C.

All the simulations are done for 6 different cases including Pre- layout analysis, Pre- layout analysis with lumped capacitors to predict parasitic effect beforehand, parasitic capacitance included extracted netlist of 2 different layouts and, parasitic capacitance and resistance included extracted netlist of 2 different layouts.

2.4.2 Performance parameters of TSPC frequency divider circuit: -

This block being a digital component has critical parameters related to timing and power dissipation of the circuit. Also, maintaining correct logic state and holding correct output plays dominant role in defining circuit performance. On the basis of such criterions, following are the dominant parameter of this circuit which defines the quality of performance: -

1. Clock – Q delay (T_{clk-q}):- It is defined as the time elapsed between the clock edge at the input of the circuit and the corresponding change in the output. It is measured at slow-slow corner, maximum temperature and minimum supply voltage.

2. Setup time (T_{setup}):- It is defined as the time interval before clock edge when data edge should come at the D input of the circuit for the proper operation of the circuit. It is measured at slow-slow corner, minimum temperature, minimum supply voltage and with high to low transition of data signal.

3. Hold time (T_{hold}):- It is defined as the minimum time after the clock edge for which data should be maintained at the input of circuit for proper logical switching at further

stages. It is measured at slow-slow corner, maximum temperature, minimum supply voltage and with low to high transition of data signal.

4. Maximum frequency of operation (f max):- It is the maximum frequency of input signal which can be correctly divided without creating any timing violation. It is usually preferred to be measured at slow-slow corner and minimum supply voltage.

5. Maximum current through supply (IVDD):- It is the maximum current consumed by the circuit from the supply. Generally preferred to be measured at fast-fast corner, maximum temperature, maximum frequency of operation and maximum supply voltage.

6. Maximum power dissipation: - It is one of the most important parameter defining figure of merit of the circuit and thus has to be focused more. Maximum power dissipation occurs under the case of maximum current consumed by the circuit from the supply.

7. Leakage current and leakage power: - Maximum current flowing through the supply under power down mode represents the leakages that arise in our design. It has to be measured under two cases: clock kept low and clock kept high. Leakage power dissipation can be calculated by multiplying supply voltage to leakage current. It is measured at fast-fast corner, maximum temperature and maximum supply voltage.

2.4.3 Simulation results: -

Following table shows obtained results for analysis of TSPC frequency divider circuit: -

1. Primary parameters:-

Table 2.1 Table showing values of primary parameters for all sets of simulation. (% deviation from Pre- layout analysis).

Parameters	Pre (approx.)	Pre with cap.	post_cc_1	post_rc_1	post_cc_2	post_rc_2
Clk-Q delay (psec)	60-100	7.14285	-11.904	21.428	-25	-22.619
Worst case setup time (psec)	10-30	26.0869	21.739	30.434	17.391	17.391
Theoretical maximum frequency of operation (Ghz)	1-20	-9.6774	5.376	-18.279	19.354	16.129
Practical maximum frequency of operation (Ghz)	1-20	-5.8823	11.764	-11.764	11.764	11.764
Maximum current consumed IVDD (uA) at respective fmax	500-900	23.6534	51.923	12.118	18.690	19.372
Power dissipation (uwatt) at respective fmax	600-1200	23.6436	51.915	12.110	18.690	19.372
Maximum current consumed IVDD (uA) at fmax= 7.5 Ghz	400-1000	17.8525	26.217	26.462	9.214	9.441
Power dissipation (uwatt) at fmax= 7.5 Ghz	550-1150	18.0086	26.383	26.620	9.244	9.553

2. Leakage parameters: - Measured at Fast-Fast corner, VDD= 1.3V, Temp= 125 deg. C.

Table 2.2 Table showing values of Leakage parameters for all sets of simulation. (% deviation from Pre- layout analysis).

	Pre (approx.)	Pre with cap	post_cc_1	post_rc_1	post_cc_2	post_rc_2
Leakage current :-						
For clock kept high (uA)	1-4	2.244695	27.88631	53.5815521	25.542021	28.29234
For clock kept low (uA)	1-5	1.929189	31.51748	66.9968216	22.762214	24.83184
Leakage power :-						
For clock kept high (uW)	2-5	2.918103	36.2522	69.6560177	33.204627	36.78005
For clock kept low (uW)	1.5-5.5	2.507946	40.97273	87.0958681	29.590878	32.28139

3. Setup time: - Measured at Slow-Slow corner, Rise time = 40 psec., Fall time = 40 psec., High to low transition.

Table 2.3 Table showing values of setup time for all sets of simulation under various operating conditions. (% deviation from Pre- layout analysis).

Setup time (psec)	Pre (approx.)	Pre with cap	post_cc_1	post_rc_1	post_cc_2	post_rc_2
Vdd= 1.3v, T= -40 deg. c.	8-14	33.3333	25	58.33333	41.66667	41.66667
Vdd= 1.3v, T= 125 deg. c.	6-12	33.3333	22.22222	33.33333	11.11111	11.11111
Vdd= 1.1v, T= -40 deg. c.	10-30	26.0869	21.73913	39.13043	17.3913	17.3913
Vdd= 1.1v, T= 125 deg. c.	5-25	40	33.33333	60	26.66667	26.66667

4. Hold time: - Measured at Slow-Slow corner, Rise time = 40 psec., Fall time = 40 psec., Low to high transition.

Table 2.4 Table showing values of hold time for all sets of simulation under various operating conditions. (% deviation from Pre- layout analysis).

Hold Time (psec)	Pre (approx.)	Pre with cap	post_cc_1	post_rc_1	post_cc_2	post_rc_2
Vdd= 1.3v, T= -40 deg. c.	1-20	0	-9.09091	-9.09091	-18.1818	-18.1818
Vdd= 1.3v, T= 125 deg. c.	2-22	0	-15.3846	-15.3846	-30.7692	-23.0769
Vdd= 1.1v, T= -40 deg. c.	5-25	0	0	0	-14.2857	-14.2857
Vdd= 1.1v, T= 125 deg. c.	5-29	0	-6.25	-6.25	-18.75	-18.75

2.4.4 Analysis of obtained data: -

From the experimental data that we have obtained, we can see following layout dependent effects on performance parameters:-

1. The order of parasitic effect (capacitance and resistance) is in the following order for different set of analysis:-

   $$\text{Pre (without cap)} \leq \text{Pre (with cap)} \leq \text{Post (CCmax)} \leq \text{Post (RCmax)}$$

2. Circuit becomes slow (all timing increases) as compared to Pre layout analysis without cap.

   This change can be up to 30% under worst case analysis.

3. One unique effect as opposite to general view is observed. Since the parasitic capacitance increases from Pre- layout analysis to Post- layout analysis it is expected that circuit should slow down (i.e. timing parameters should increase) but on the contrary circuit timing parameters decreases.

4. Increase in leakage current follows the same trend as that of parasitic capacitance which is a very obvious phenomenon as parasitic capacitances are responsible for leakages. Thus we can say leakage increases due to parasitic effect. Increase in leakage can be as large as 87% in a good layout as compared to Pre- layout analysis without cap.

CHAPTER – 3

ANALYSIS OF CSVCO

Voltage controlled oscillator is a circuit which generates variable frequency output depending upon the value of its input control voltage (Vc). As we know that most of the digital circuits depends on clock signals for their operation which makes a VCO an inevitable component of digital circuits. Also many analog and mixed signal circuits like trans-receiver and PLL consist VCO as an important component which shows that VCO is a widely used circuit and analysis of such circuit can give us a good insight the behaviour of all circuits under layout dependant effects (LDE).

Here the analysis of the effect of varying the number of fingers (nf) of each MOSFET on VCO operation has been done so that results obtained from it can be used in improving the current VCO designing techniques.

3.1 Design under study: -

It has been seen that on comparing with other voltage-controlled oscillators (VCOs) such as source-coupled oscillators and LC-tank oscillators, current-starved (CS) VCOs gives the widest tuning range and at the same time can have a practical balance among power, area, and phase noise. Thus we chose following design shown in fig. 3.1 which is a current starved voltage controlled oscillator of 3 stages: -

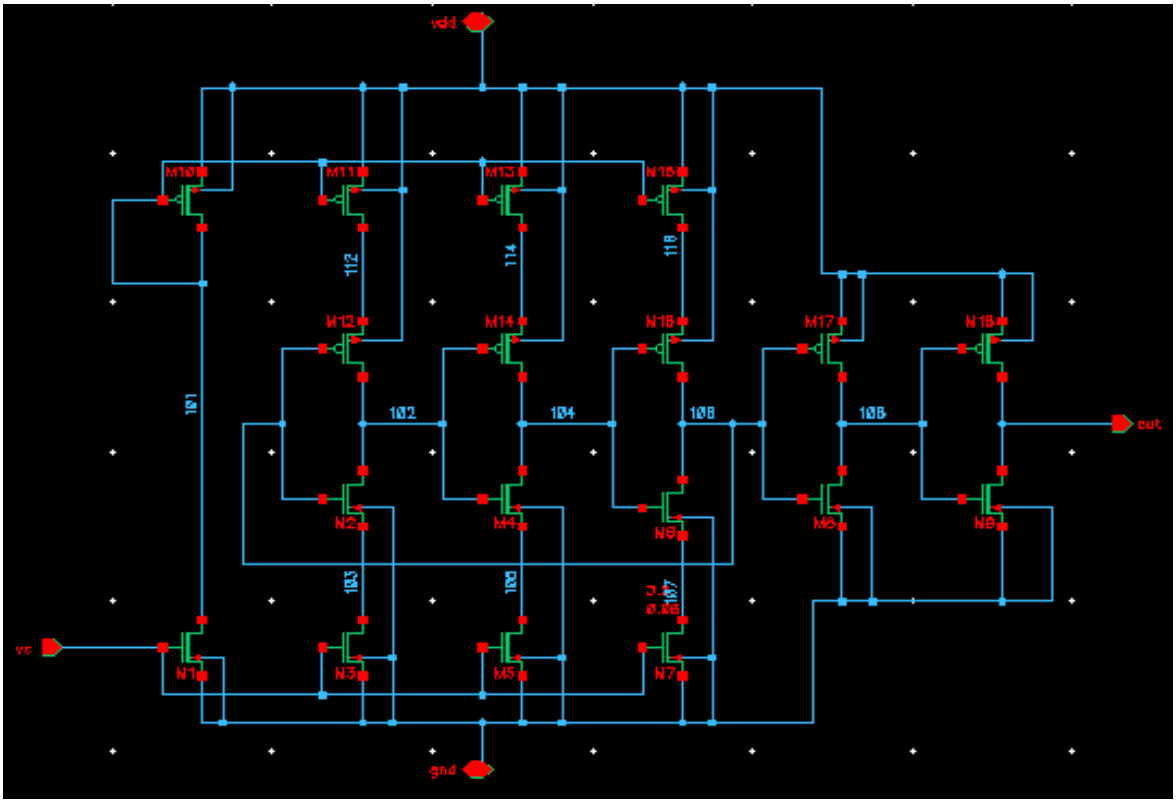

Fig 3.1 Schematic of Current Starved Voltage Controlled Oscillator (CSVCO) used in our analysis.

The circuit has three different parts, the inverter stages, current starving circuitry and the buffers. It consist of 3 inverter stages connected in feedback like a ring oscillator which is responsible for sustaining oscillations. Current starved circuitry includes MOSFETs which control the maximum amount of current that has to be fed to MOSFETs of inverter stages which in turn affects the frequency of oscillation of these stages. Last is the buffer stage consisting of two inverters in series to improve the output of CSVCO. As during the complete operation of CSVCO, the MOSFETs of inverter stages are made to starve for current by MOSFETs of current starving circuitry thus this circuit is called as Current Starved Voltage Controlled Oscillator.

3.2 Circuit performance parameters: -

Any voltage controlled oscillator circuit is characterised by same set of parameters which act as figure of merit for choosing any design. These performance parameters are Power consumption, Area, Operating frequency range, Linearity (and gain), Phase Noise and Power-delay product.

1. Power consumption: -

   Power consumption is defined as the product of supply voltage to the average current drawn by the VCO in one cycle of oscillation over its entire frequency range, i.e.

   Power dissipation (P) = Supply Voltage (Vdd) * Average current (Iavg.)

   It is a well-known fact that the power dissipation increases as the frequency of operation increases thus the maximum value of power dissipation is obtained for the maximum value of control voltage (Vc) at which the frequency of operation is highest. Thus we use this value to define the maximum power dissipation of the VCO. It is usually focussed to reduce the power dissipation of the circuit to reduce the operating cost of the design by either bringing down the supply voltage or by reducing the current required to operate the circuit. Reducing the leakage currents also help in cutting down the power dissipation of the circuit.

2. Area: -

   Area of the voltage controlled oscillator is defined as the area of chip required to fabricate the design under consideration which can be calculated by multiplying the width and height of the layout of design. It is a dynamic parameter in the sense that it purely depends upon the skills of layout designer and varies from designer to designer. As the area of any circuit directly affects the cost of production, it becomes an important factor thus putting layout designers in a tight constraint of reducing it to as low as possible.

3. Operating frequency range: -

   Operating frequency range of a voltage controlled oscillator is defined as the range of frequency at the output that the circuit can generate. It is usually desired to have a large operating range for the improved performance of other dependant circuits.

4. Linearity and gain: -

   For the better control of operating frequency of voltage controlled oscillator circuit, it is required that the output frequency should be linearly dependent upon the value of input control voltage for the entire range of operation, i.e.

   Frequency of oscillation f (osc) α Control voltage (Vc)

   ⇨ Frequency of oscillation f (osc) = K * Control voltage (Vc) + f0

Where K is linearity constant also called as gain or sensitivity of VCO whose value depends upon the circuit design parameters and f0 is VCO free running frequency.

This gain parameter K defines the sensitivity of the VCO circuit and a higher value of gain gives an increased operating frequency range. Thus it is always focussed to increase the gain K of the VCO circuit.

5. Phase Noise: -

   Phase noise defines the shift of the output frequency from its desired value over a period of time. It is related to frequency instability and Jitter in the output. Usually frequency instability is of two types:

   a. Long term: - A shift in the frequency over a period of hours, days, months, etc.

   b. Short term: - A shift in the frequency over a period of few seconds, millisecond, microseconds, etc.

   Phase is related to short term instability in the operating frequency. Phase noise is a frequency domain parameter which can be defined using single side band (SSB) phase noise denoted by £(f). This parameter £(f) is calculated as the area of 1 Hz bandwidth in Power spectral density curve at some offset frequency to the area of 1 Hz bandwidth at the centre frequency:

$$£(f) = \frac{Area\ under\ 1\ Hz\ bandwidth\ at\ offset\ frequency}{Area\ under\ 1\ Hz\ bandwidth\ at\ centre\ frequency}$$

   Unit of phase noise is dBc / Hz.

   Since this parameter defines the amount of disturbances in the output frequency thus it is tried to keep it as low as possible.

6. Power delay product: -

   Power delay product is defined as the product of power dissipation and the path delay in the circuit. It act as the figure of merit for a voltage controlled oscillator circuit and gives a fair comparison between two different architectures of VCO circuit.

3.3 Pre layout analysis of CSVCO: -

Pre layout analysis of current starved voltage controlled oscillator was done in order to understand the dependency of circuit performance parameters on number of fingers of

MOSFET as it is one of the main layout dependent parameter which results in many layout dependent effects such as Inverse narrow width effect, Stress, etc. As a result of this varying number of fingers (nf) results in change in many device characteristics such as threshold voltage, mobility, etc. which affects VCO circuit performance parameters such as operating frequency range, power dissipation, linearity, power delay product, etc. which is studied in this section.

3.3.1 Simulation setup: -

Here Cadence Virtuoso Tool is used for design generation and its ADE-L Simulator is used for performing parametric analysis. Other parameters of analysis is as follows: -

Technology Node	=	STMicroelectronics 65 nm
VDD	=	0.5 V
Temp.	=	27 deg. C.
Min. control voltage (Vc)	=	0.3 V
Max. control voltage (Vc)	=	0.5 V

3.3.2 Simulation results: -

By varying number of fingers of each MOSFET by same amount, we have measured control voltage (Vc) versus operating frequency range, power dissipation, linearity and power delay product and the results obtained are as follows: -

1. Frequency of oscillation versus control voltage (Vc) for different number of fingers : -

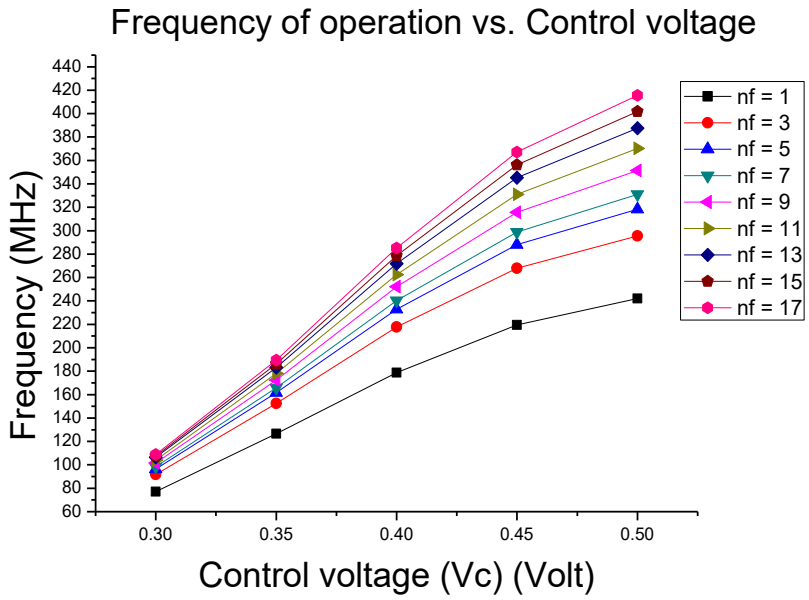

Fig 3.2 Figure showing variation of operating frequency vs. control voltage for different number of fingers.

2. Power dissipation versus control voltage (Vc) for different number of fingers : -

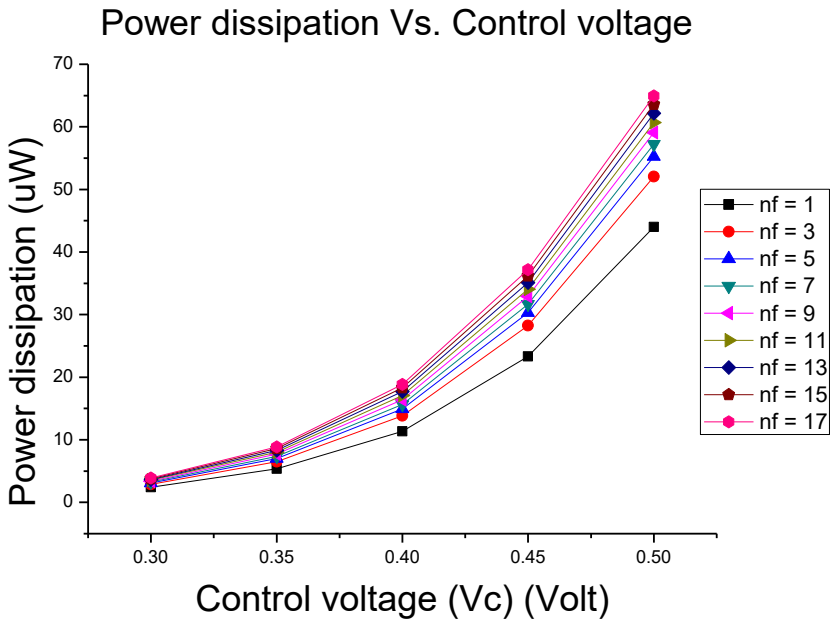

Fig 3.3 Figure showing variation of power dissipation vs. control voltage for different number of fingers.

3. Power- delay product vs. control voltage (Vc) for different number of fingers : -

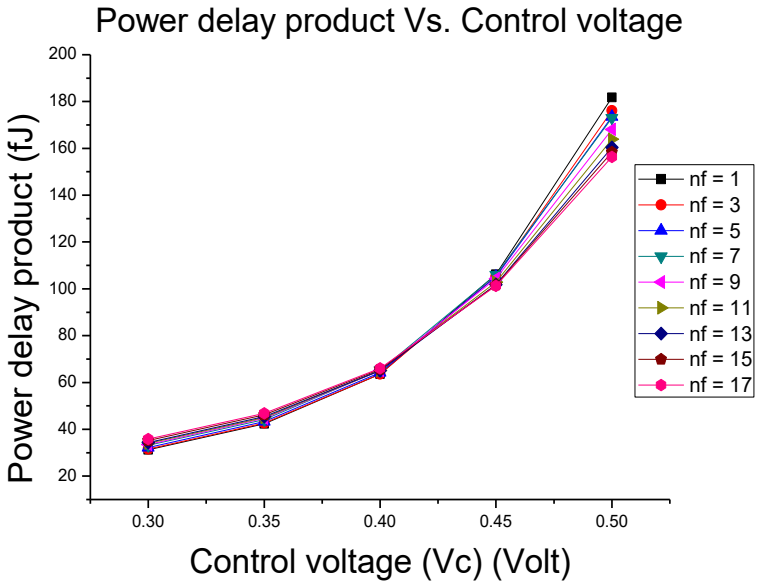

Fig 3.4 Figure showing variation of power delay product vs. control voltage for different number of fingers.

4. Range of frequency for which VCO follows linearity: -

Table 3.1 Table showing range of frequency for linearity of VCO.

Number of fingers	Range of frequency (MHz)
1	77 – 178
3	91 – 220
5	96 – 235
7	98 – 260
9	101 – 270
11	104 – 310
13	106 – 345
15	108 - 370
17	109 - 390

3.3.3 Analysis of obtained results: -

Following conclusion can be derived from the data obtained in the above experiments: -

1. On increasing the number of fingers of MOSFETs, the operating frequency range shifts towards higher values i.e. frequency for each value of control voltage increases.
2. On increasing the number of fingers of MOSFETs, the power dissipation increases because of the increase in operating frequency (which is caused due to increase in current due to decrease in threshold voltage).
3. On increasing the number of fingers of MOSFETs, it is seen that power delay product increases for lower value of control voltage (Vc) but decreases for higher value of control voltage (Vc).
4. On increasing the number of fingers of MOSFETs, it is clearly seen that the range of frequency for which VCO output follows linearity increases.

CHAPTER – 4

OPTIMIZATION OF CSVCO CIRCUIT CONSIDERING LAYOUT DEPENDENT SYSTEMATIC EFFECTS

After analysing dependency of performance parameters of Current Starved Voltage Controlled Oscillator (CSVCO) on number of fingers, we can conclude that it is an important layout dependent parameter which affects performance of CSVCO by significant amount. In other words we can say that if proper value of number of fingers of each MOSFET is not chosen carefully then it can lead to severe degradation in performance. Thus it becomes more important to formulate a proper technique to decide what value of number of fingers of MOSFETs should be chosen to improve circuit performance and match the given specifications.

4.1 Variability due to Number of fingers parameter: -

On closely examining the data obtained in Pre – layout analysis of CSVCO circuit, we can make following conclusions about the impact of number of fingers on circuit components:-

1. First of all, it can be seen that on increasing the number of fingers of MOSFET, the width of each finger moves towards lower values as a result of which Inverse Narrow Width Effect (INWE) comes into picture and as a result of it the threshold voltage of the MOSFETs decreases. This further results in increase in current of MOSFETs. Increase in current du to INWE effect can be seen as more current to charge internal nodes thus lesser time required in their charging and thus higher frequency of operation.

   Also it can be concluded that the increase in current will definitely lead to increase in power dissipation of the circuit.
2. Next layout dependent effect that arises on changing number of fingers of the MOSFETs is STI stress effect. When we increase the number of finger then due to shielding from outer fingers, the effect of STI stress on inner fingers decreases as a result of which stress does not affect whole width of the MOSFET which results in increased current value. But as we know that these increase in current tends to

saturates after a value above which any further increase in number of fingers will not lead to much change in the current of the MOSFETs.

Increase in current due to STI stress effect comes at higher value of width where inverse narrow width effect is not present. After current increase due to stress nearly saturates, the effect of INWE comes into picture on further increasing number of fingers.

Effect of increase in current due to stress on device characteristics is same as the effect of increase in current due to inverse narrow width effect.

3. Decrease in threshold voltage because of increase in the number of fingers due to INWE will result in larger leakage current through the MOSFETs and thus more power dissipation but these effect can be ignored because of very small change in the power dissipation as compared to the change due to increased ON current of the devices.

4.2 Proposed methodology to optimize CSVCO design: -

It is usually observed that circuit designers tends to vary number of fingers of all MOSFETs in same fashion (either increase or decrease) to achieve less layout area. By this analysis of Current Starved Voltage Controlled Oscillator (CSVCO), it has been found that a significant improvement in performance parameters can be achieved if we use unequal number of fingers for different set of MOSFETs depending upon their role in circuit operation.

The concept behind the unequal number of fingers depends upon optimising current value in different MOSFETs depending upon their position and role in the circuit. This concept can be better understood by considering each set of MOSFETs independently and observing effect of varying number of fingers on its characteristics. Following Pre- layout observations are made in this analysis of CSVCO circuit which act as the basis of proposed methodology for optimising CSVCO performance by varying number of fingers of MOSFETs:

1. If we fix the number of fingers of driving MOS (M2, M4, M6, M12, M14, M16) equals to 7 and vary the number of fingers of controlling MOS (M1, M3, M5, M7, M10, M11, M13, M15) then following results are obtained: -

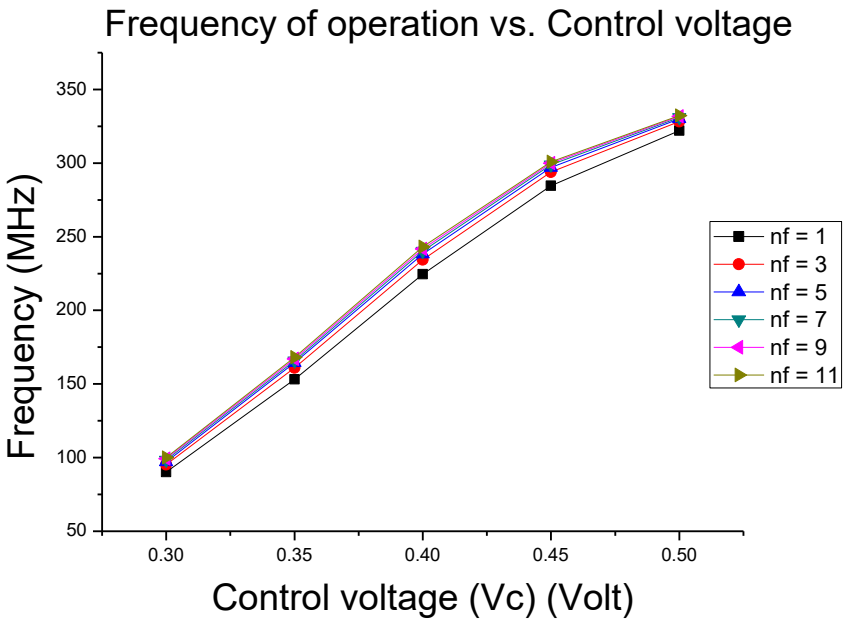

Fig. 4.1 Figure showing variation of operating frequency vs. control voltage for different number of fingers (for number of fingers of driving MOS (M2, M4, M6, M12, M14, M16) = 7).

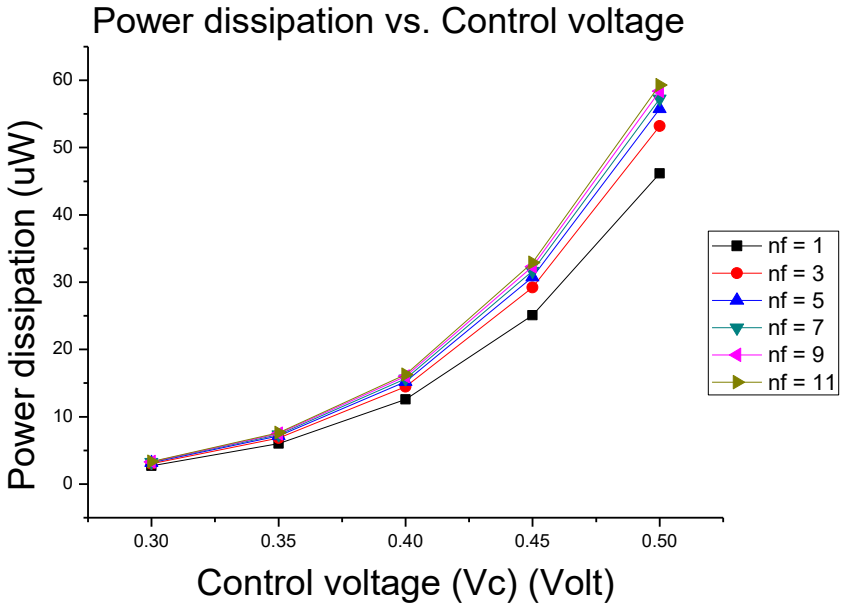

Fig. 4.2 Figure showing variation of power dissipation vs. control voltage for different number of fingers (for number of fingers of driving MOS (M2, M4, M6, M12, M14, M16) = 7).

Thus we can conclude that if we increase the number of finger of controlling MOS (M1, M3, M5, M7, M10, M11, M13, M15) beyond a certain limit then due to Inverse narrow width effect, it's threshold voltage decreases which leads to decrease in sensitivity (gain) of VCO and increased power dissipation. Thus it is advised to keep number of fingers of controlling MOSFET as low as possible. Although this

technique has a disadvantage that overall operating frequency range shifts to lower values.

2. On the other hand if we fix the number of fingers of controlling MOS (M1, M3, M5, M7, M10, M11, M13, M15) equals to 7 and vary the number of fingers of driving MOS (M2, M4, M6, M12, M14, M16) then following results are obtained: -

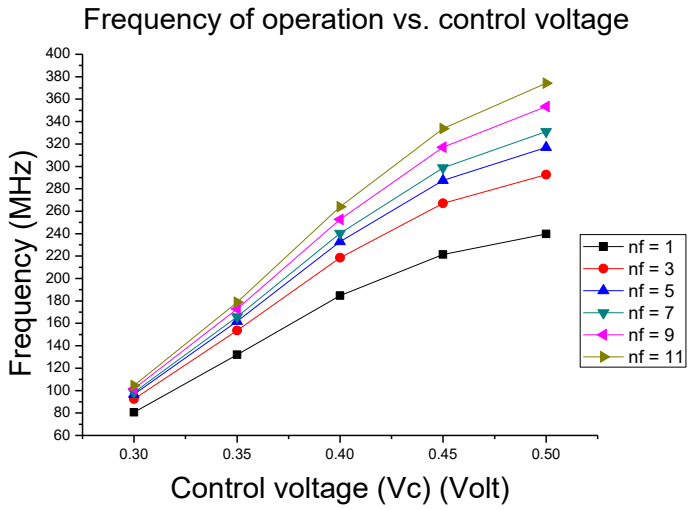

Fig. 4.3 Figure showing variation of operating frequency vs. control voltage for different number of fingers (for number of fingers of controlling MOS (M1, M3, M5, M7, M10, M11, M13, M15) = 7).

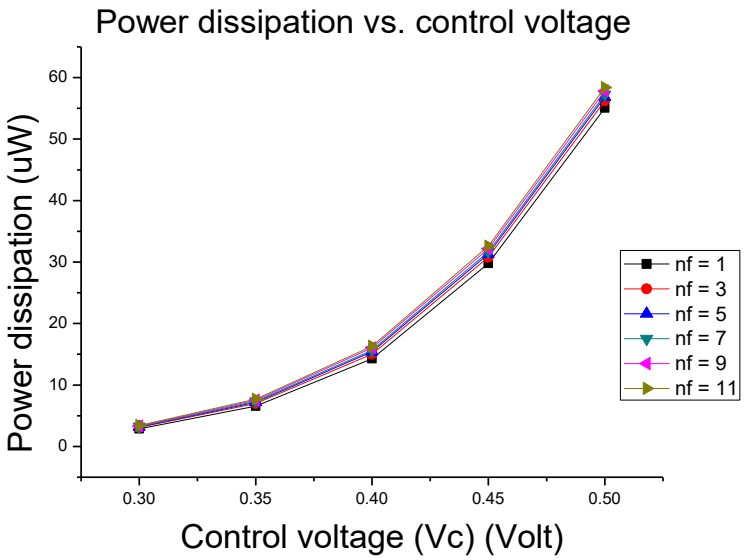

Fig. 4.4 Figure showing variation of power dissipation vs. control voltage for different number of fingers (for number of fingers of controlling MOS (M1, M3, M5, M7, M10, M11, M13, M15) = 7).

Thus we can say that the limitation of reduced frequency range in first case can be overcome by increasing the number of fingers of driving MOS (M2, M4, M6, M12, M14, M16) because increase in number of fingers of driving MOS results in increase in operating frequency range.

As a conclusion it is suggested to keep number of fingers of controlling MOS as low as possible while increase the value of number of fingers of driving MOS as much as possible. Pre-layout simulation has shown considerable improvement in operating frequency range and power dissipation of the CSVCO circuit under study using this technique. In the following results comparison of design with uniform number of fingers (as followed earlier) and design with non- uniform number of fingers (as following our proposed techniques) has been made: -

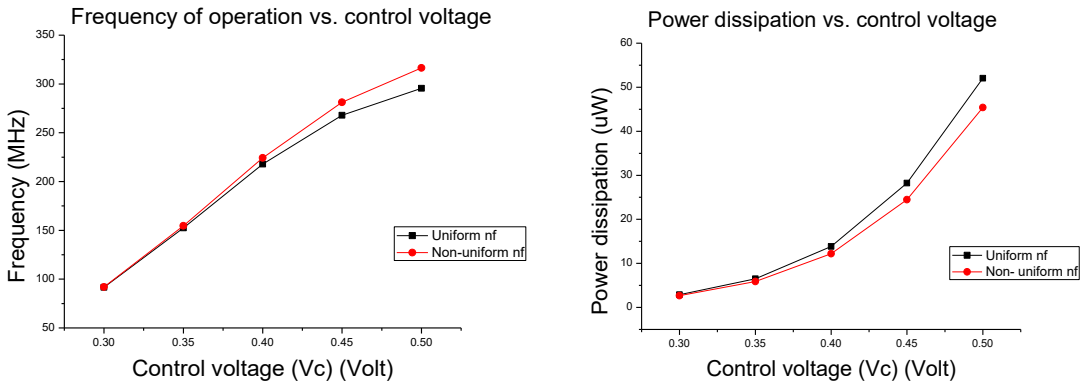

Fig. 4.5 For nf (uniform) = 3 / nf (non-uniform) = 1 (controlling MOS) and 5 (driving MOS).

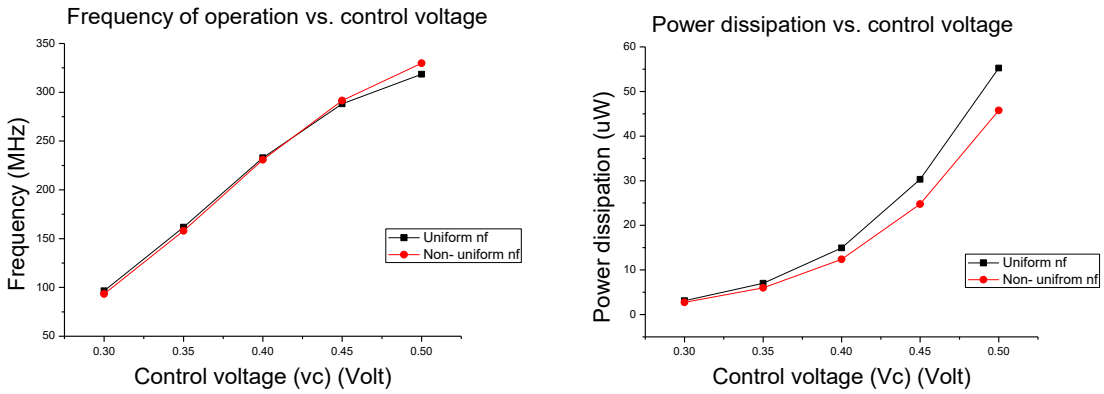

Fig. 4.6 For nf (uniform) = 5 / nf (non-uniform) = 1 (controlling MOS) and 7 (driving MOS).

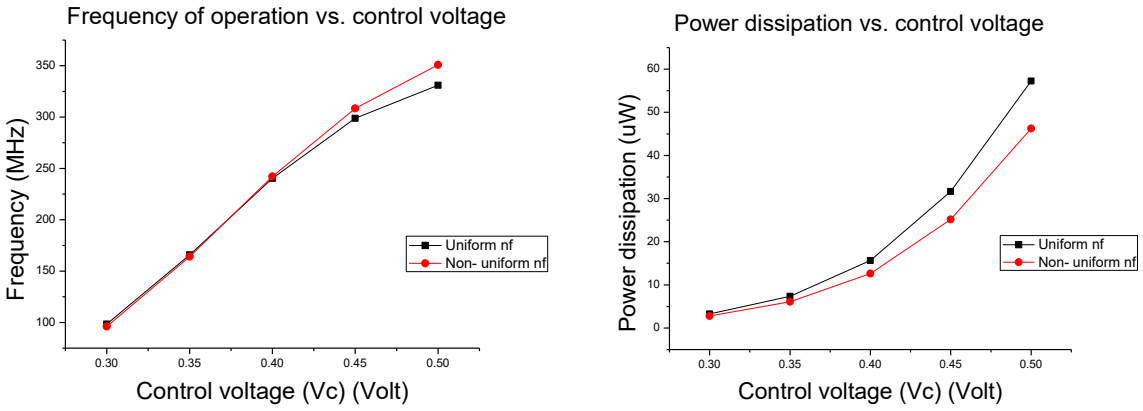

Fig. 4.7 For nf (uniform) = 7 / nf (non-uniform) = 1 (controlling MOS) and 9 (driving MOS).

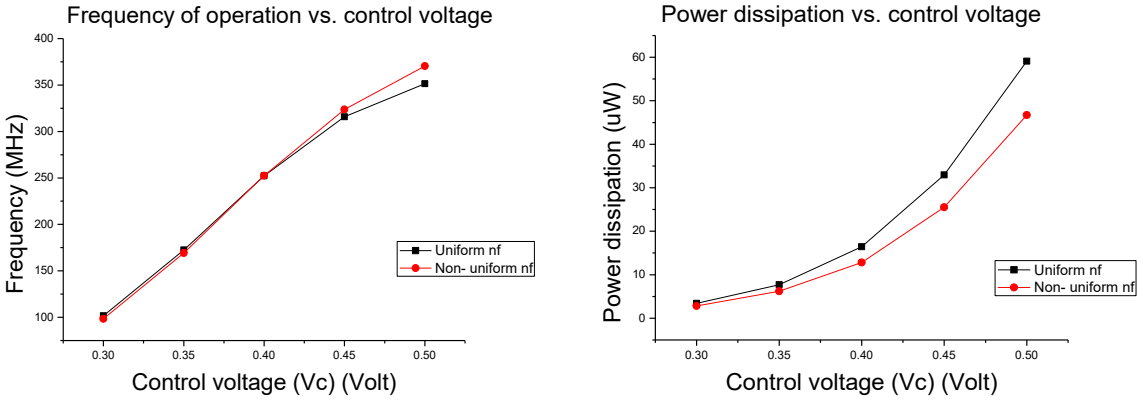

Fig. 4.8 For nf (uniform) = 9 / nf (non-uniform) = 1 (controlling MOS) and 11 (driving MOS).

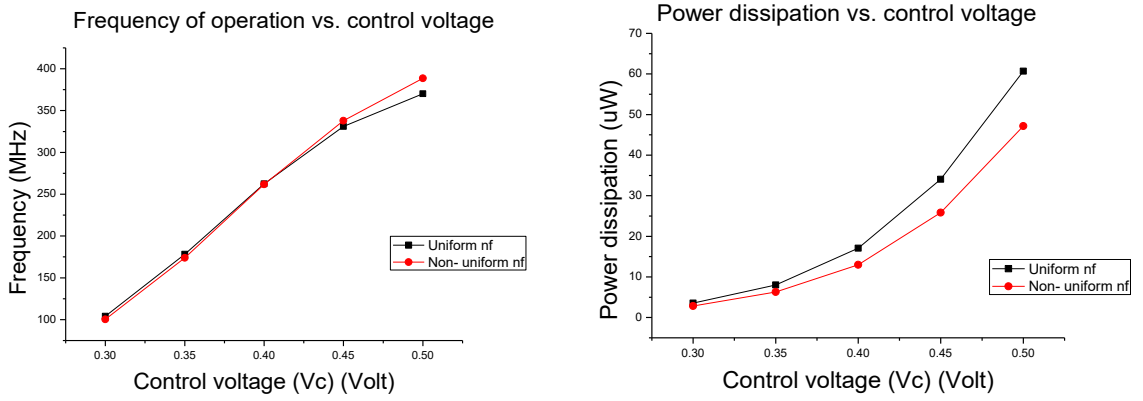

Fig. 4.9 For nf (uniform) = 11 / nf (non-uniform) = 1 (controlling MOS) and 13 (driving MOS).

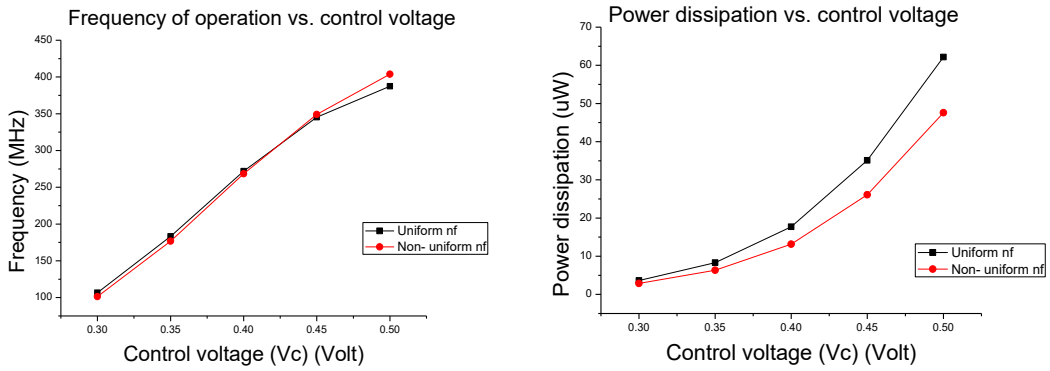

Fig. 4.10 For nf (uniform) = 13 / nf (non-uniform) = 1 (controlling MOS) and 15 (driving MOS).

4.3 Validation of proposed methodology on Post- layout design: -

As it has been seen that proposed technique of reducing the number of fingers of controlling MOSFETs and increasing the number of fingers of driving MOSFETs gives fairly good enough improved value of performance parameters of CSVCO circuit, thus Post- layout analysis has been done for some particular set of number of fingers of old and new design technique.

Following figures shows layout drawn for different values of uniform and non- uniform number of fingers: -

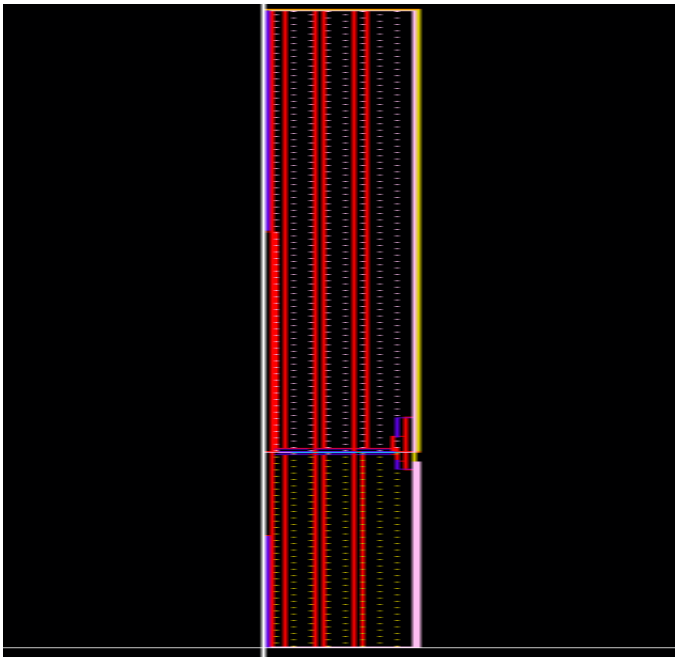

Fig. 4.11 Layout for nf (uniform) = 3.

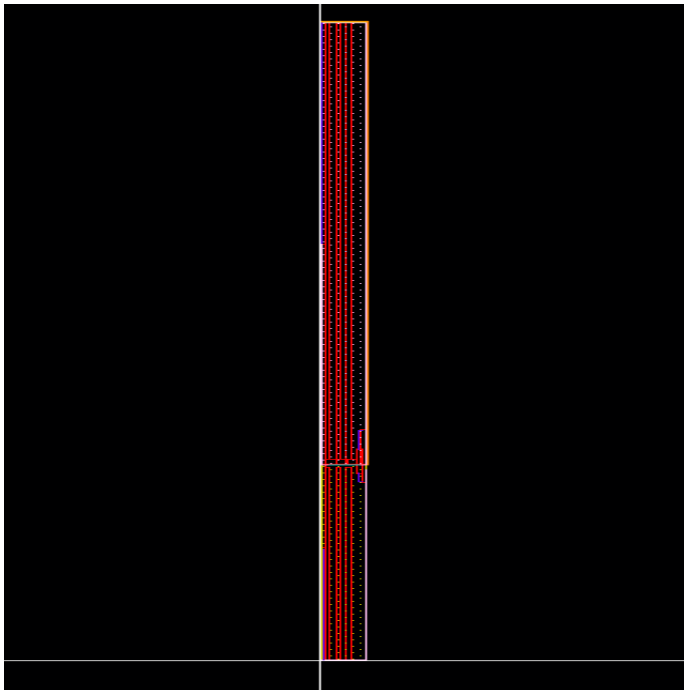

Fig. 4.12 Layout for nf (non-uniform) = 1 (controlling MOS) and 5 (driving MOS).

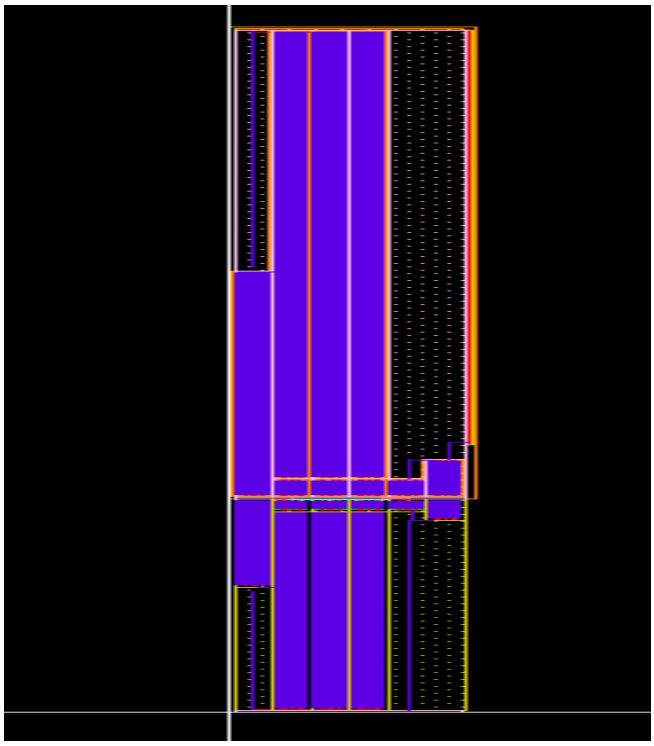

Fig. 4.13 Layout for nf (uniform) = 7.

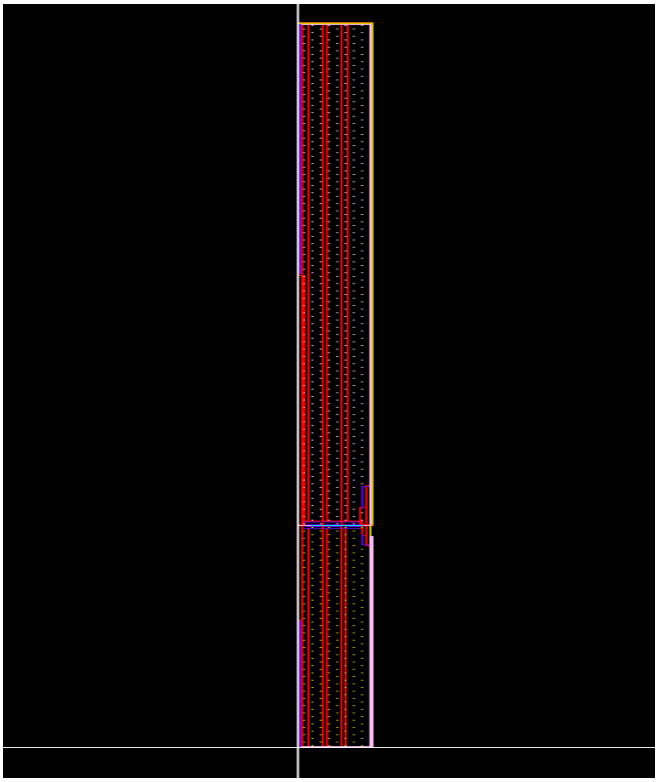

Fig. 4.14 Layout for nf (non-uniform) = 1 (controlling MOS) and 9 (driving MOS).

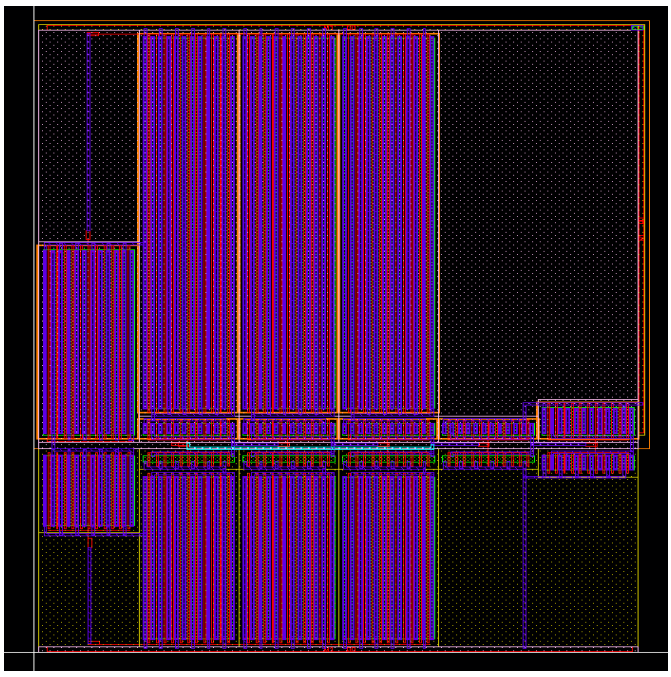

Fig. 4.15 Layout for nf (uniform) = 7.

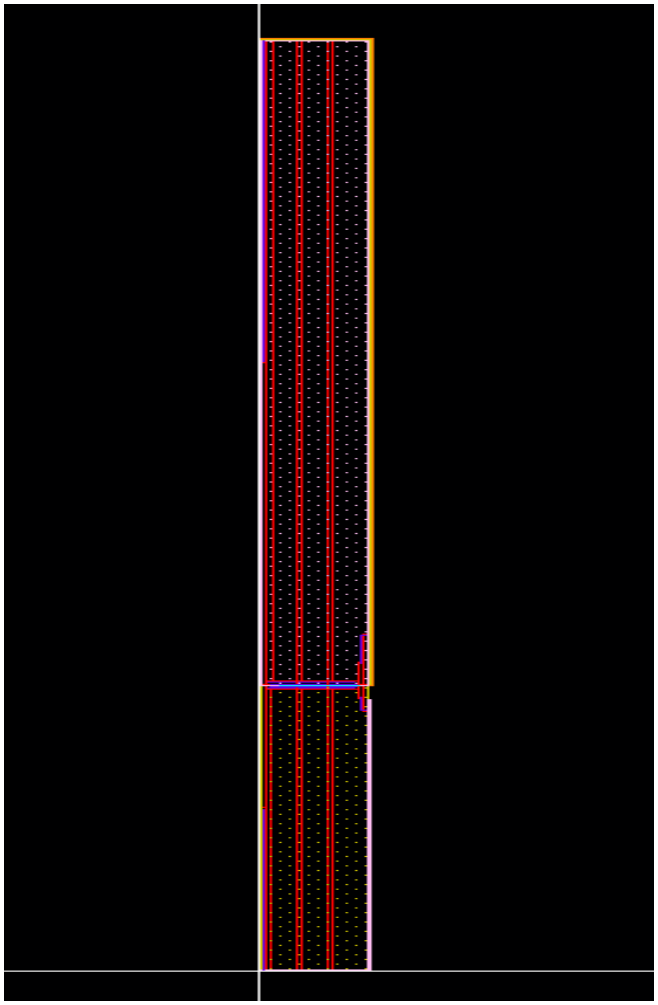

Fig. 4.16 Layout for nf (non-uniform) = 1 (controlling MOS) and 13 (driving MOS).

Following results are obtained in post- layout analysis: -

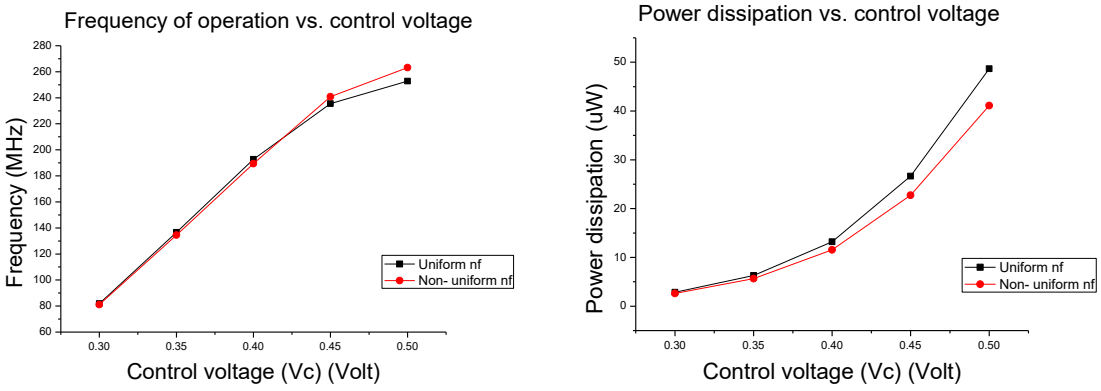

Fig. 4.17 For nf (uniform) = 3 / nf (non-uniform) = 1 (controlling MOS) and 5 (driving MOS).

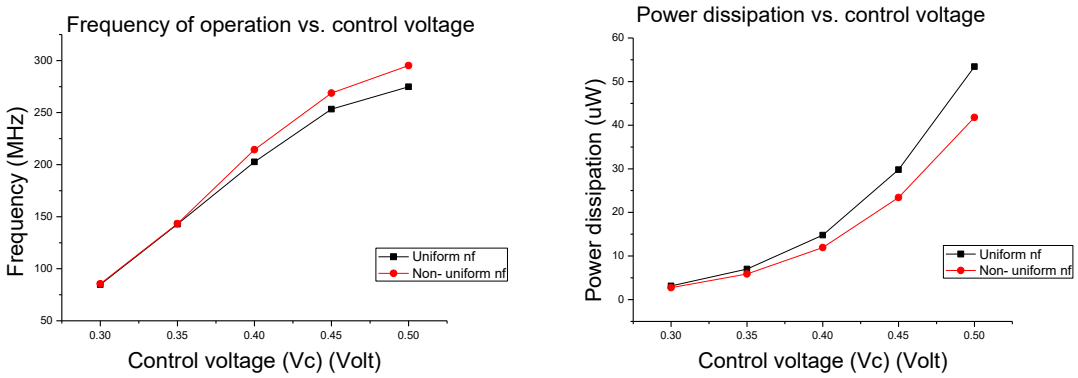

Fig. 4.18 For nf (uniform) = 7 / nf (non-uniform) = 1 (controlling MOS) and 9 (driving MOS).

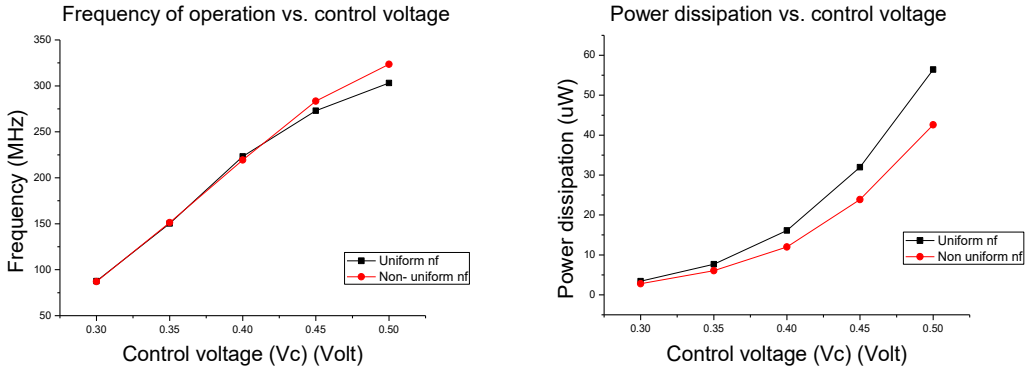

Fig. 4.19 For nf (uniform) = 11 / nf (non-uniform) = 1 (controlling MOS) and 13 (driving MOS).

Post- layout analysis has also shown considerable improvement in performance parameters of Current Starved VCO circuit which validates that proposed design technique gives better VCO circuit considering layout dependent effects.

CHAPTER – 5

CONCLUSION

From the observations made in project work, it can be said that circuit performance parameters are highly dependent upon layout dependent effects and if not taken care of this effects can lead to complete circuit failure under severe case. Thus, it is very necessary to know the impact that layout dependent effects can create on circuit performance beforehand at the schematic level.

Effects of increasing number of fingers of MOSFET are: Firstly its threshold voltage decreases due to inverse narrow width effect when width of each fingers becomes very small, secondly ON current of MOSFET increases due to shielding of inner fingers from STI stress effect and lastly its leakage current increases as a result of decrease in threshold voltage. Thus, predicting the optimum value of number of fingers of each MOSFET in design can help in avoiding degradation in circuit performance parameters due to layout dependent effects.

From the analysis performed on Current Starved Voltage Controlled Oscillator (CSVCO) circuit, it has been found that to achieve optimum performance of the circuit the number of fingers of controlling MOSFETs should be kept as low as possible and the number of fingers of driving MOSFETs should be kept as high as possible. Results obtained in pre layout and post layout analysis shows considerable improvement in CSVCO performance parameters. Also, by using this technique, much better results than nominal value of performance parameters such as range of operating frequency, power dissipation, linearity, area, etc. can be achieved on compromise of remaining performance parameters i.e. tuning of these performance parameters is also possible.

Thus using proposed methodology for circuit designing helps to predict layout dependent effects beforehand and reduce its impact on circuit performance parameters. As a result of which the overall number of iterations involved in circuit design cycle is reduced. This helps in reducing cost of production, improving reliability of circuit and meeting time to market.

CHAPTER – 6

FUTURE SCOPE

The methodology proposed in this project work is for the optimisation of Current Starved Voltage Controlled Oscillator (CSVCO) circuit performance parameter. This technique can now be further tested on other analog and mixed signal circuits and required modifications can be made to validate use of this technique on other circuits. Also automation of this technique can be done which can predict the exact number of fingers of each MOSFETs depending upon the specification of output given.

A similar technique can also be formulated for finding other parameters of layout such as Pitch of device, number of gate contacts, number of devices (m), etc. to obtain the optimum results of circuit performance parameters.

Impact of number of fingers of MOSFETs on layout dependent effects like inverse narrow width effect and STI stress has been studied in this work. Effect of number of fingers on other layout dependent effects can also be studied in future to improvise proposed technique.

All the observation made in this work is based on simulated data, finding results of this technique on fabricated circuit can also be done to make this technique silicon tested.

REFERENCES

[1] K. L. Yeh and J. C. Guo, "The impact of layout-dependent STI stress and effective width on low-frequency noise and high-frequency performance in nanoscale nMOSFETs", *IEEE Transactions on Electron Devices,* vol. 57, no. 11, pp. 3092-3100, Nov. 2010.

[2] A. B. Kahng, P. Sharma and R. O. Topaloglu, "Chip optimization through STI-stress-aware placement perturbations and fill insertion," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 27, no. 7, pp. 1241–1252, Jul. 2008.

[3] N. Alam, A. Bulusu, and S. Dasgupta, "Gate-Pitch optimization for circuit design using strain-engineered multi-finger gate structures", *IEEE Transactions on Electron Devices,* vol. 59, no. 11, pp. 3120-3123, Nov 2012.

[4] K. W. Su *et al.*, "A scalable model for STI mechanical stress effect on layout dependence of MOS electrical characteristics," in *IEEE Custom Integr. Circuits Conf.*, Sep. 2003, pp. 245–248.

[5] W. Rhett Davis and Harun Demircioglu, "Modelling Layout-Dependent Stress Effects: Opportunities for Open DFM", NC state university.

[6] B. Razavi, "Design of analog CMOS integrated circuit", Ch. 14-15, Edition 2001, McGraw Hill companies.

[7] Dan Clein, "CMOS IC layout: Concepts, Methodologies and Tools", Ch. 1-4, Edition 1999, Butterworth Heinemann prints.

[8] Neil H. E. Weste, David Money Harris, "CMOS VLSI Design: A circuits and systems perspective", Ch. 3-4, Fourth Edition, Pearson publications.

[9] Virtuoso Schematic Composer User Guide, October 2002.

[10] C.C. Wang *et al.*, "Modelling of layout-dependent stress effect in CMOS design," in *IEEE International Conference on Computer-Aided Design,* ACM, Nov. 2009, pp. 513-520.

[11] J. Xue *et al.*, "Layout-dependent STI stress analysis and stress-aware RF/Analog circuit design optimization", in *IEEE International Conference on Computer-Aided Design,* ACM, Nov. 2009, pp. 521-528.

[12] K. Okada, H. Onodera and K. Tamaru, "Layout dependent matching analysis of CMOS circuits", *IEICE trans. Fundamentals,* vol. e82–a, no.2, pp. 348-355, Feb. 1999.

[13] J. Zhou, S. Jayapal, B. Busze, L. Huang and J. Stuyt, “A 40 nm inverse narrow-width-effect-aware sub-threshold standard cell library”, in *DAC*, Jun. 2011, pp. 441-446.

[14] K. K. L. Hsueh, J. J. Sanchez, T. A. Demassa and L. A. Akers, “Inverse narrow width effects and small geometry MOSFET threshold voltage model”, *IEEE transactions on electron devices*, vol. 35, no. 3, pp. 325-338, Mar. 1988.

[15] K. Ohe, T. Yabu, S. Kugo, H. Umimoto and S. Odanaka, “The inverse-narrow-width effect of LOCOS isolated n-MOSFET in a high-concentration p-Well”, *IEEE Electron Device letters*, vol. 13, no. 12, pp. 636-638, Dec. 1992.

[16] T. Nishihara, K. Tokunaga, and K. Kobayashi, “A 0.5 pm isolation technology using advanced poly silicon pad LOCOS (APPL),” *IEDM Tech. Dig.*, 1988, pp. 100-103.

[17] H. H. Tsai, C. L. Yu, and C. Y. Wu, “A bird’s beak reduction technique for LOCOS in VLSI fabrication,” *IEEE Electron Deike Letl.*, vol. EDL-7, no. 2, pp. 122-123, Feb. 1986.

[18] C. MazurC, A. Lill, and C. Zeller, “Width-independent narrow nMOSFET reliability by split-well drive-in,” *IEEE Electron Device Lett.*, vol. 11, no. 5, pp. 224-226, May 1990.

[19] S. Odanaka *et al.*, “SMART three-dimensional process/device simulator integrated on a super-computer,” in *ISCAS Proc.*, vol. 2, 1987, pp. 534-537.

[20] S. Odanaka, H. Umimoto, M. Wakabayashi, and H. Esaki, “SMART-P: Rigorous three-dimensional process simulator on a supercomputer,” *IEEE Trans. Computer-Aided Design*, vol. 7, no. 6, pp. 675-683, June 1988.

[21] H. Umimoto, S. Odanaka, I. Nakao, and H. Esaki, “Numerical modelling of nonplanar oxidation coupled with stress effects,” *IEEE Trans. Computer-Aided Design*, vol. 8, no. 6, pp. 599-606, Jun. 1989.

[22] N. Shigyo and R. L. M. Dang, “Analysis of an anomalous subthreshold current in **a** fully recessed oxide MOSFET using a three-dimensional device simulator,” *IEEE Trans. Electron Devices*, vol. ED-32, no. 2, pp. 441-445, Feb. 1985.

[23] K. Ohe, **S.** Odanaka, K. Moriyama, T. Hori, and **G.** Fuse, “Narrow-width effects of shallow trench-isolated CMOS with n+-polysilicon gate,” *IEEE Trans. Electron Devices*, vol. 36, no. 6, pp. 224-226, June 1989.

[24] X. Li, Z. Ye, Y. Tan and Y. Wang, “A two-dimensional analysis method on STI-aware layout-dependent stress effect”, *IEEE transactions on electron devices*, vol. 59, no. 11, pp. 2964-2972, Nov. 2012.

[25] V. Moroz, G. Eneman, P. Verheyen, F. Nouri, L. Washington, L. Smith, M. Jurczakl, D. Pramanik, and X. Xu, “The impact of layout on stress-enhanced transistor performance,” in *SISPAD*, 2005, pp. 143–146.

[26] H. Tsuno *et al.*, “Advanced analysis and modeling of MOSFET characteristic fluctuation caused by layout variation,” in *VLSI Symp. Tech. Dig.*, 2007, pp. 204–205.

[27] M. Saitoh, N. Yasutake, Y. Nakabayashi, T. Numata, and K. Uchida, “Comprehensive performance assessment of scaled (110) CMOSFETs based on understanding of STI stress effects and velocity saturation,” in *IEDM Tech. Dig.*, 2008, pp. 1–4.

[28] P. K. Rout, D. P. Acharya and G. Panda, “A multi-objective optimization based fast and robust design methodology for low power and low phase noise current starved VCO”, *IEEE Transactions on Semiconductor Manufacturing*, vol. 27, no. 1, pp. 43-50, Feb. 2014.

[29] S. K. Saw and V. Nath, “A low power low noise current starved CMOS VCO for PLL”, in *IEEE International Conference on Computing, Communication and Automation*, May 2015, pp. 1252-1255.

[30] A. Sharma, N. Alam, S. Dasgupta and A. Bulusu, “Multi-finger MOSFETs’ optimization considering stress and INWE in static CMOS circuits”, *IEEE Transactions on Electron Devices*, vol. 63, no. 6, Jun. 2016.

PUBLICATION

[1] A. Gupta, A. Sharma, R. Singh and A. Bulusu, " Design consideration for near threshold current starved voltage controlled oscillator considering layout dependent effects", in IEEE 22nd ASPDAC (communicated).