FinFET Device-Circuit Interaction Issues

A DISSERTATION

Submitted in partial fulfilment of the

requirements for the award of the degree

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MASTER OF TECHNOLOGY

in

ELECTRONICS AND COMMUNICATION ENGINEERING

(With Specialization in Microelectronics and VLSI)

by

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CANDIDATE'S DECLARATION

I hereby declare that the work, which is being reported in this dissertation on, "**FinFET Device-Circuit Interaction Issues"**, being submitted in the partial fulfilment of the requirements for the award of the degree of **Master of Technology** in **Microelectronics & VLSI**, submitted in the Department of Electronics and Communication Engineering, Indian Institute of Technology Roorkee, Roorkee, India, is an authentic record of my own work carried out from May 2015 to May 2016 under the guidance and supervision of **Dr. Anand Bulusu**, Associate Professor, Department of Electronics and Communication Engineering, Indian Institute of Technology Roorkee, Roorkee.

The matter embodied in the dissertation to the best of my knowledge has not been submitted for the award of any other degree elsewhere.

Dated:

Place: Roorkee (Shobhit Tyagi)

CERTIFICATE

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

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ABSTRACT

Supply voltage scaling is most effective method for reducing the energy consumption in digital circuits. Lot of work has been done in past to determine the fundamental limit of supply voltage for CMOS logic circuits. It has been shown that minimum supply voltage for MOSFET based ideal CMOS inverter is 36mV. Owing to their near ideal subthreshold characteristic FinFET device are more suitable for ultra-low voltage application hence an analysis has been done to find a similar fundamental limit for FinFETs. This fundamental limit is purely theoretical. The significance of such limit is in predicting a practical limit for circuit operation by considering variability and noise into consideration.

After establishing the minimum supply voltage for FinFET inverters, sizing issues for circuit operating near this fundamental limit have been discussed. Thus it has been shown that, if proper sizing is not done, the fundamental limit as established above is insufficient. For such cases we need to look at problem from circuit point of view. A problem for pass transistor followed by latch has been solved analytically using a modified expression for subthreshold current of FinFET device. Finally, temperature variability have been considered. For this purpose temperature dependence of subthreshold current equation has been established and validated. Minimum supply voltage limit is found to increase with temperature.

All simulation level work have been carried out using a table-based Verilog-A model data for which have been extracted using TCAD. In later part of report behavioral modelling for analog blocks of high speed serial IOs has been discussed.

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CHAPTER 1

INTRODUCTION

There has been significant advances toward ultra-low voltage circuit design, aimed at applications that rely solely on small batteries. Example of such application are wearable computing, biomedical systems, handheld devices and sensor networks [1], [2]. Such application demands energy saving while providing intelligence and better performance for costly infrastructure support in places with difficult access, such as inside the human body. Scaling of supply voltage is by far the best way to reduce the total energy consumption.

The fundamental limit for supply voltage in the CMOS digital circuit has been reported to be 36mV at 300K in [3], [6]. Analysis of same has been done in [5] using sub-threshold current equation of bulk MOS. Since FinFET device shows close to ideal sub-threshold slope it can be an ideal candidate for low voltage operations. TCAD simulation results show that the minimum supply voltage for FinFETs, based on the criteria given in [5], is less than what is predicted for the bulk MOS device (less than 36mV). So an investigation is needed to explain and comment on the validity of results obtained.

For the above purpose sub-threshold current equation has been modified to characterize the behavior of the FinFET device in ultra-low voltage regime (< 100mV). A new equation for predicting minimum supply voltage for FinFET inverter is then derived using this new sub-threshold current equation (chapter 3), as has been done for bulk MOS in [5]. Adding to what has already been done for bulk MOS, an issue with sizing of SRAM and clocked latches at such low voltage has also been addressed. Finally issue of variability of min supply voltage with temperature has been dealt with in chapter 4 along with suggestions of architectures at such low supply voltages.

Another issue targeted was coming up with an alternative to long TCAD simulation for circuits with higher transistor counts. The existing technique of table based Verilog-A modelling was used for FinFET circuit simulation. The process of data extraction for the model was automated using the Perl scripting language. Verilog-A model has been described in chapter 2 along with methods of data extraction. Later part of chapter compares Sentarus TCAD result with those of H-Spice.

The organization of this thesis is as follows:

Chapter 1: Introduction and thesis organization.

Chapter 2: Fundamental limit of supply voltage for FinFETs have been discussed

Chapter 3: This chapter explains a table based Verilog-A model for FinFETs.

Chapter 4: Conclusion and Future work have been discussed in this chapter.

CHAPTER 2

Fundamental limit of supply voltage for FinFET circuits

2.1 Minimum supply voltage for MOSFET circuits

The fundamental limit of supply voltage for MOSFET circuit can be obtained by considering already established limits on binary switching energy and heuristic given in [9].

2.1.1 The Fundamental Limit on Binary Switching Energy

A lot of work has been done in the past to establish the fundamental limit on signal energy transfer during a binary switching transition. As reported in [6], the first statement of this limit was given by Jhon von Neumann who computed thermo dynamical minimum of energy per elementary act of information using:

$$kTlog_eN$$

Where N=2 for a binary act [7]. But no justification was provided for this assertion in [7]. Later Landuer calculated energy dissipation involved in restoring particle to one state from other in a hypothetical binary device, consisting of a particle in bistable potential well [8]. His work shows that if lowering of potential barrier of one side is carried out very slowly, the energy dissipation will be

$$kT(log_e2)$$

Which is equal to 0.0179 eV at 300^0K.

2.1.2 Minimum switching energy of a MOSFET

A convincing heuristic argument has been provided in [9] by A. W. Lo, for establishing minimum switching energy needed for a MOSFET. As argued by Lo, in order to meet the quintessential requirement of discrimination of binary signal the slope of static transfer curve of a (CMOS) binary logic gate must be greater than one in absolute value at transition point, where input voltage is equal to output voltage.

Using this requirement Swanson and Meindl derived minimum allowable supply voltage of the circuit [10] as

$$V_{dd}(min) \cong 2\left(\frac{kT}{q}\right)\left[1+\frac{C_{fs}}{C_{ox}+C_d}\right] log_e\left(2+\frac{C_d}{C_{ox}}\right) \quad (1)$$

Where C_{fs} is the fast surface state capacitance per unit area, C_{ox} is the gate-oxide capacitance per unit area, and C_d is the depletion region capacitance per unit area.

For an ideal MOSFET (i.e. one with subthreshold slope of 60 mV/decade at 300^0K) C_{fs} << C_{ox} and C_d << C_{ox}, so

$$V_{dd}(min) \cong 2(log_e 2)\frac{kT}{q} = 1.38\frac{kT}{2} = 0.036\ eV\ at\ 300^oK \quad (2)$$

Using this, minimum signal energy transfer during a binary switching transition can now be evaluated [10]. Energy stored on gate capacitance C_g of a single MOSFET in a CMOS inverter circuit is given by (assuming minimum possible gate charge of single electron Q = q and minimum supply voltage given by equation 2).

$$E_s(min) = \frac{1}{2}Q_g V_{dd}(min) = kT(log_e 2) \quad (3)$$

Which is the expression for fundamental limit on energy transfer during binary switching. The energy transfer of the circuit is triple of value obtained by 3, because inverter switching involves simultaneous switching of two MOSFETs (assuming PMOS width is kept twice to compensate for electron hole mobility difference). Thus it can be easily said that 36mV is the minimum supply voltage for circuits at 300^oK.

2.1.3 Minimum Supply voltage for MOSFET based CMOS circuits

Above work has been further expanded in [10], [11] to find minimum supply voltage of more complex circuits like NAND gate and SRAM cell. The basic heuristic for defining minimum supply voltage remains the same i.e. static voltage transfer curve must exhibit slope greater than one in absolute terms when input and output voltage levels are equal.

Work done in [11] shows that minimum supply voltage degrades for more complex logic gates. The reason being difficulty in balancing relative strength of NMOS and PMOS in case of stacked transistors.

Adding to this dependence on number of input switching simultaneously is important too, worst case have to be considered while deciding minimum supply voltage. Usually simultaneous switching of all inputs of a logic gate define minimum supply voltage for it.

For SRAM minimum supply voltage is defined to be the voltage below which two stable points in butterfly diagram of SRAM becomes indistinguishable. Which is actually the V_{DD} at which V_{IH} and V_{IL} of an inverter become equal, which is limiting condition of heuristic given in [9], i.e. obtaining absolute value of slope equal to one when input and output voltage level are equal.

Figure 2.1 shows the butterfly plots of SRAM for three different supply voltages.

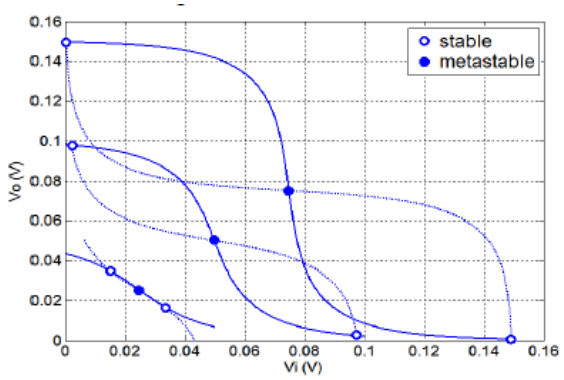


Figure 2.1 SRAM latch butterfly plot - n = 1.5 [5]

2.2 FinFET under 100mV current equation

For obtaining current equation in ultra-low voltage regime certain assumptions are needed as described below:

- Inversion charge is negligible as compared to depletion charge in voltage range of interest (i.e. less than 100mV).
- Fin potential rises by same amount as gate voltage (i.e. sub-threshold slope is closed to ideal).

Simulation results confirm these assumptions. There are some important observation regarding sub-threshold operation of FinFET device. These are described below:

- Depletion region from drain and source side extend into fin. This is like punch through in Bipolar Junction Transistors.
- Even without any gate potential fin is fully depleted due to work function difference between gate metal and Si.
- There is volume inversion in device i.e. electron concentration is not maximum at surface but at the centre of Fin (at lower gate voltages, below threshold voltage).

Taking above conditions into consideration sub-threshold current equation for FinFET can now be derived.

Case 1: No drain bias, $V_{DS} = 0$ and $V_{GS} \neq 0$ (< 100mV)

Net current through device is zero in this case. Since equal number of carrier will be able to cross barrier from both side net current through device will become zero. Barrier height will be controlled by applied gate voltage, V_{GS} and will depend on flat band voltage V_{FB} ($V_{FB} = \phi_{MS}$ if trapped charges are assumed zero) and built-in potential of junction between source/drain and channel.

Barrier as seen by electron in drain/source is given by:

$$V_o = V_{bi} - \phi_{MS} - \frac{V_{GS}}{\eta} \tag{4}$$

An important point here is

$$V_{bi} \neq \frac{KT}{q} log_e \left(\frac{N_A N_D}{{n_i}^2}\right)$$

The reason for this assertion is channel length is way too short than the required depletion region length i.e. depletion region charge required to balance the positive charge in fin extension region, for alignment of Fermi levels, is insufficient. Due to this, some carriers continue to flow into fin region to the point where fin become sufficiently negatively charged, so as to balance the positive charge in fin extension region.

Current density due to carriers reaching the source side, $J_{SD,}$ by crossing barrier V_o is directly proportional to concentration of carriers having energy greater than $E_{f\_D} + qV_o$, where E_{f_D} is the electron Fermi level in Drain.

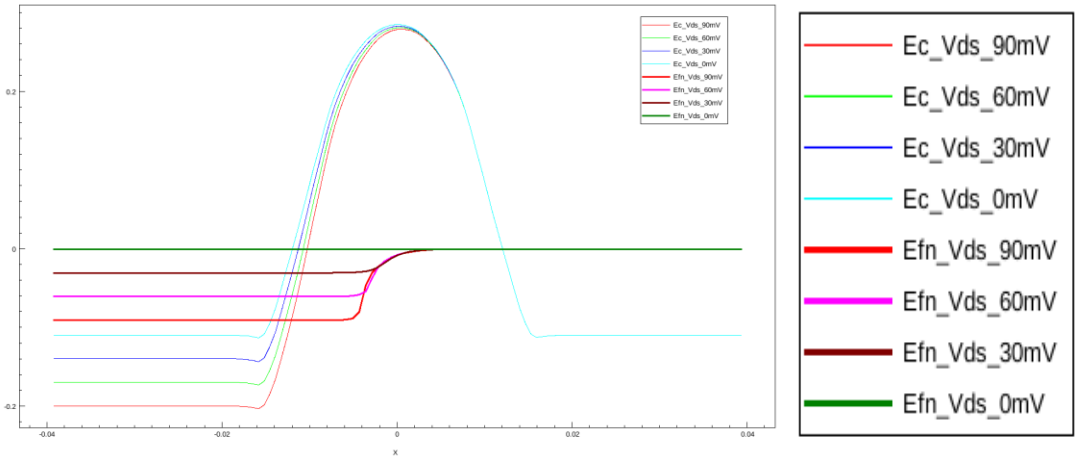


Figure 2.2 Variation of Energy levels with Drain Voltage

Similarly current density due to carriers from Source to Drain, J_{DS}, will be proportional to concentration of carriers having energy greater than $E_{f\_S} + qV_o$, E_{f_S} is the electron Fermi level in Source.

$$J_{SD}, J_{DS} \; \alpha \; N_c \exp\left(-\frac{E_c + qV_o - E_f}{KT}\right)$$

Which can be written as

$$J_{SD}, J_{DS} = C * N_c \exp\left(-\frac{E_c - E_f}{KT}\right) * \exp\left(-\frac{qV_o}{KT}\right)$$

Or,

$$J_{SD}, J_{DS} = C * n_n * \exp\left(-\frac{qV_o}{KT}\right)$$

n_n is electron concentration in Source/Drain region respectively i.e. N_D.

$$J_{SD}, J_{DS} = C * n_n * \exp\left(-\frac{qV_o}{KT}\right) \quad (5)$$

$$J_{net} = J_{SD} - J_{DS} = 0 \quad (6)$$

Case 2: A drain bias, $V_{DS} \neq 0$ is applied and $V_{GS} \neq 0$ (< 100mV)

When a drain voltage, V_{DS}, is applied barrier on drain side increases and can now be given by

$$V_o' = V_{bi} - \phi_{MS} - \frac{V_{GS} - \beta V_{DS}}{\eta} + V_{DS} \tag{7}$$

While on source side,

$$V_o'' = V_{bi} - \phi_{MS} - \frac{V_{GS} - \beta V_{DS}}{\eta} \tag{8}$$

Source to drain current density, J_{SD}, can now be given as:

$$J_{SD} = C * n_n * \exp\left(-\frac{qV_o'}{KT}\right) * \exp\left(-\frac{\lambda * qV_{DS}}{KT}\right) \tag{9}$$

The component $\exp(-\frac{\lambda * qV_{DS}}{KT})$ in equation (9) account for change in current due to charge imbalance created by applied drain voltage. After drain voltage is applied the symmetry in potential well is disturbed. Slope of energy level is greater on one side, also zero field point is shifted toward opposite (Source) terminal as clear from figure (2). Due to which there is net change in charge, ΔQ, due to applied V_{DS}. This charge drift into the drain terminal thus reducing the current density J_{SD} further. This charge imbalance increase with V_{DS} and hence the factor added with J_{SD} in equation 8 is justified.

Net current density can now be given by

$$J_{net} = J_{SD} - J_{DS}$$

Using (5), (7), (8) and (9)

$$J_{net} = C * n_n * \exp\left(-\frac{qV_o''}{KT}\right)\left(1 - \exp\left(-\frac{\Upsilon * qV_{DS}}{KT}\right)\right)$$

We can write,

$$J_{net} = J_o * \exp\left(\frac{q(V_{GS} - \beta V_{DS})}{\eta * KT}\right)\left(1 - \exp\left(-\frac{\Upsilon * qV_{DS}}{KT}\right)\right) \tag{9}$$

Where, $\Upsilon = 1 + \lambda$. Current can now be written as

$$I = I_o * \exp\left(\frac{q(V_{GS} - \beta V_{DS})}{\eta * KT}\right)\left(1 - \exp\left(-\frac{\Upsilon * qV_{DS}}{KT}\right)\right) \tag{10}$$

Value of I_o, η and Υ can be evaluated if we know value of current I, for two points, one of which should be at higher drain voltage. For our device (i.e. 16nm FinFET described in chapter 3) (at 300^oK), $I_o = 0.59$ nA, $\Upsilon = 2.9$, $\eta = 1.175$, $\beta = 0.04$.

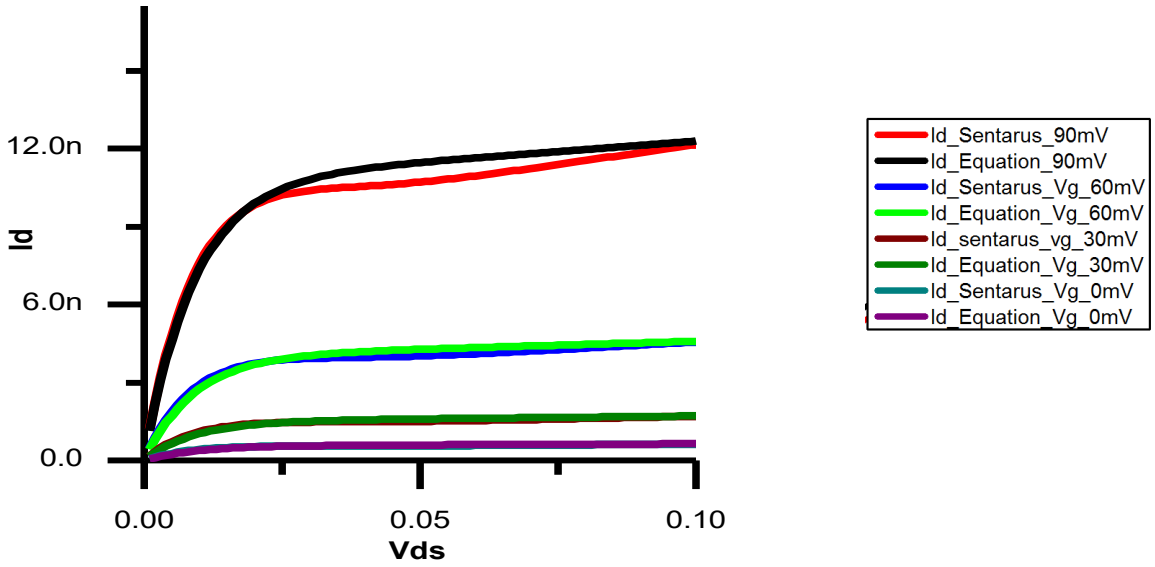


Figure 2.3 Sub-threshold Current comparison: Equation vs. TCAD

2.3 Minimum supply voltage for FinFET inverter

Repeating the work done in [5] for a FinFET inverter, using equation 10, expression for minimum supply voltage can be derived. Derivation of the same can be seen in Appendix-B at the end of report.

The final expression obtained is

$$V_{DD}(min) = \frac{2V_t}{\Upsilon} log_e(1 + \eta\Upsilon) \quad (11)$$

Using the values of η, Υ, from previous section (for 16nm FinFET device) $V_{DD}(min)$ is 26mV at 300^oK which is lower than that for ideal MOSFET.

At first this result seems wrong. The reason behind this is fundamental limit for energy transfer in binary transition. According to equation 3, for Q_g of single electron charge, minimum possible supply voltage comes out to be 36mV. The catch here his single electron charge is not possible for FinFETs. Since it's a double gate device, it's possible to reduce the minimum

supply voltage limit to 18mV (i.e. exactly half of 36mV). Thus result from expression 11 are actually acceptable.

2.4 Temperature Dependence of Sub-threshold current equation

Beside thermal voltage $V_t = \frac{KT}{q}$, I_o include several temperature dependent terms. We need to visit all contributing factors to come up with temperature dependence of current.

- Since current conduction is due to diffusion of carrier, I_o is directly proportional to diffusion constant and hence proportional to product, $\mu * V_t$ (mobility * thermal voltage).
- Barrier height given by equation 4 is again dependent on temperature. V_{bi} will not change with temperature but amount of charge trapped in potential well will change and hence Υ will change.
- With increase in temperature charge trapped should reduce and so does the Υ
- V_{FB} contain ϕ_{MS}, which is temperature dependent because ϕ_S will vary with temperature according to

$$\Phi_S = \left(\frac{KT}{q}\right) log_e\left(\frac{N_A}{n_i}\right) \text{ and, } n_i \; \alpha \; T^{\frac{3}{2}} * \exp\left(-\frac{E_g}{2KT}\right)$$

- Also constants, β and Υ are temperature dependent. Especially Υ decreases with increase in temperature.

Using dependencies explained above,

$$I_o = 0.56 * 10^{-9} * \left(\frac{T}{300}\right)^{K_1} * \exp\left(-\frac{E_g K_2}{2K}\left(\frac{1}{T} - \frac{1}{300}\right)\right) \quad (12)$$

K_1 and K_2 are fitting parameter, for our device $K_1 = 2.5$ and $K_2 = 0.49$.

$$\beta = \beta(300^oK) - 2.5 * 10^{-4} * abs\,(T - 300), \beta(300^oK) = 0.04$$

$$\Upsilon = \Upsilon(300^oK)\left(\frac{300}{T}\right)^{0.5}, \Upsilon(300^oK) = 2.9$$

Υ and β are empirically fitted for temperature dependence.

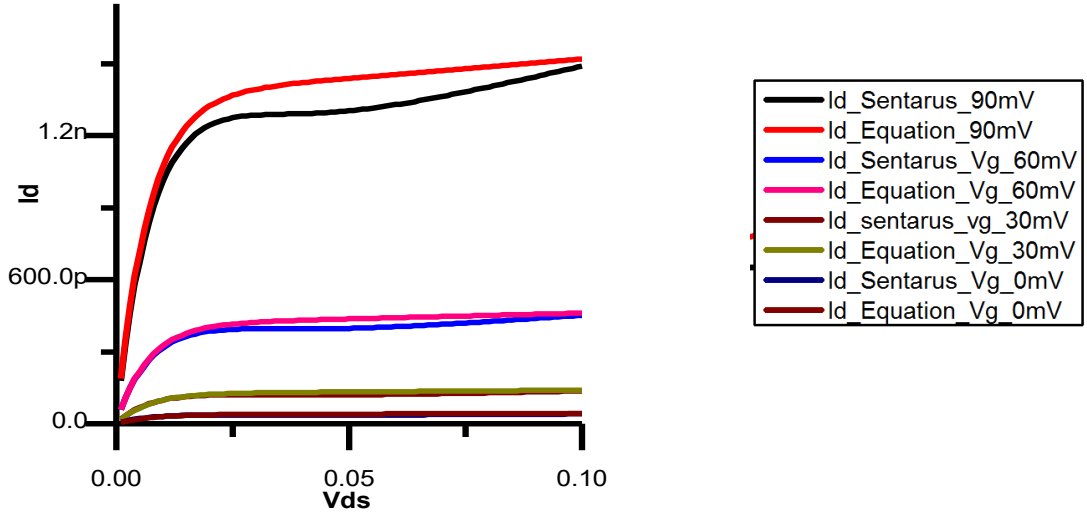


Figure 2.4 Sub-threshold Current Comparison at 248K

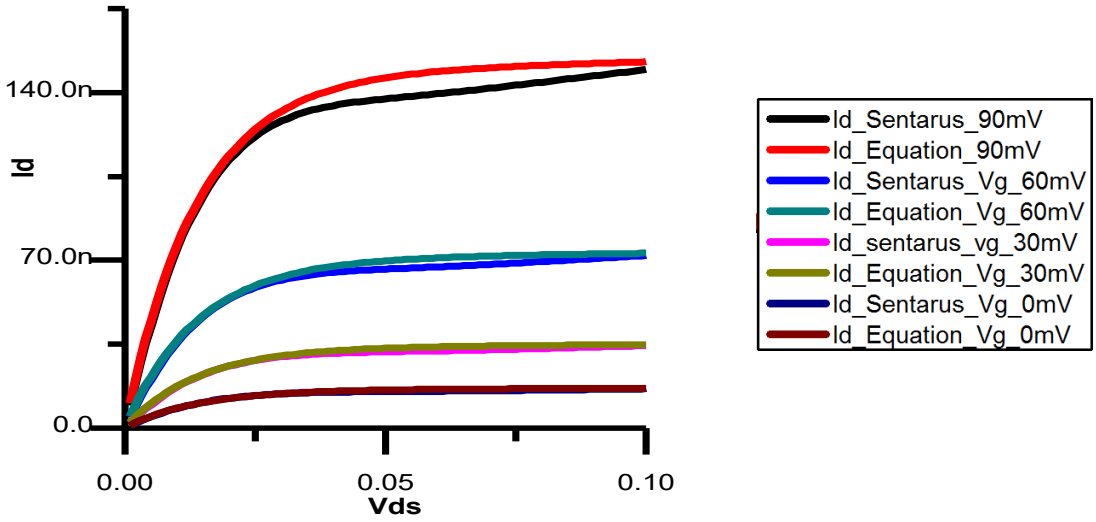


Figure 2.5 Sub-threshold Current Comparison at 400K

Figure 4 and 5 shows the comparison of current value for TCAD and equation 10, using equation 12 for I_o.

2.5 Minimum Supply voltage criteria: Revisited

The heuristic used by [9] is necessary but not sufficient condition to find out minimum supply voltage for circuits such as clocked latches and SRAM. Sizing of pass transistor is an important design consideration. Results shows that if sizing of pass transistor is not done properly, data continues to be written even when SRAM cell is not selected. So we can face a situation where write operation on some cell in a memory array cause data flipping on some other cell.

Simulation results shows that pass transistor size should be kept smaller than pull down transistor of feedback path in such circuits. If this sizing condition is satisfied, minimum supply voltage can be given by equation 11. Minimum sizing satisfying the required criteria is 123 (Pull up Transistor, Pass Transistor and Pull down Transistor). However if above sizing criteria is not used, as done in [12], the minimum supply voltage will be higher than the value obtained by 11. One such case in shown in figure 6 for 111 sizing. To obtain minimum supply voltage for such case we need to look this problem from circuit point of view.

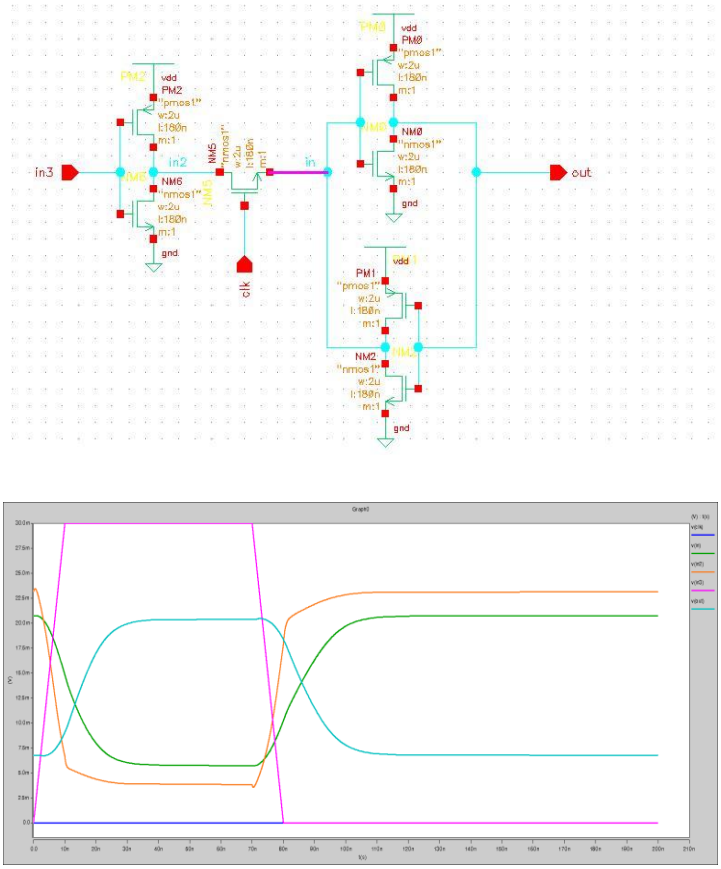


Figure 2.6 Waveforms for pass transistor (off state) followed by latch

2.6 Minimum Supply voltage for SRAM

As shown in figure 2.7 maximum supply voltage should be such that voltage at node Vx, should be either above V_{IH} (for V_{in} = logic 0 and V_X at Logic 1) or Below V_{IL} (for V_{in} = logic 1 and V_X at Logic 0). The reason for above assertion is, if voltage at node X rise above V_{IL} starting from GND (or Below V_{IH} starting from V_{DD}) loop gain of latch will become greater than unity and hence output voltage will toggle.

Using equation 10 we can solve for voltage V_{in} required at input to pull node V_X up or down to V_{IL} or V_{IH}. Steps of analysis are as follows:

- Expressions for V_{IH} and V_{IL} are needed first. These can be obtained by equating NMOS and PMOS current and solving for V_{out} along with condition, $\frac{dV_{out}}{dV_{in}} = -1$. By using values of V_{out} obtained we can figure out expressions for V_{IH} and V_{IL}.
- Once we have V_{IH}, V_{IL}, V_{out} at V_{IH} and V_{IL}, we can solve for V_{in} required for both cases i.e. by keeping V_X at V_{IH} and V_{out} at corresponding output one time while keeping V_X at V_{IL} with V_{out} at corresponding output other time.
- Now V_{DD} can be increased in steps. For V_X at V_{IH} case, if V_{in} comes out to be more than supply voltage for particular value of V_{DD}, we can consider that V_{DD} as limiting value. Similarly if V_{in} goes below zero for any value of V_{DD}, that will be limit. Maximum value of both case is the minimum supply voltage of operation for this arrangement.

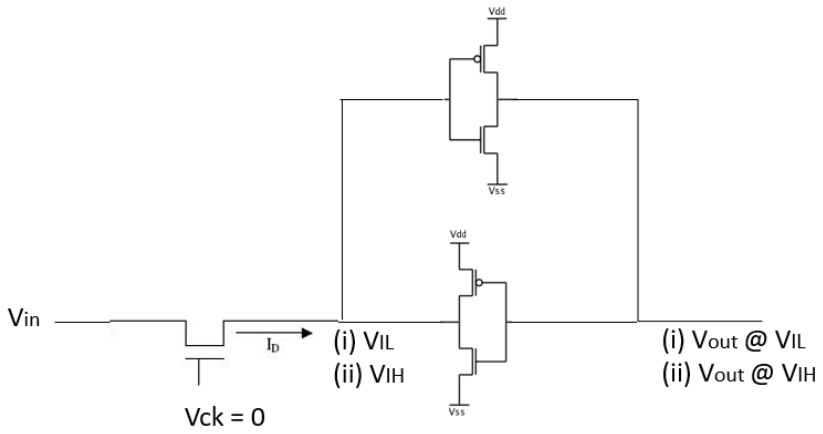


Figure 2.7 Condition for determining minimum supply voltage

Expressions obtained in solving problem from above steps are given below:

- $V_{out}\ at\ V_{in} = V_{IL},\ V_{oil} =>$

$$\frac{Vt}{\Upsilon}\log\left[\frac{2+4.\exp\left(-\Upsilon.\frac{Vdd}{Vt}\right)+sqrt\left(\left(2+4.\exp\left(-\Upsilon.\frac{Vdd}{Vt}\right)\right)^2-4.\left(1+\frac{2}{\Upsilon\eta}\right)^2\exp\left(-\Upsilon.\frac{Vdd}{Vt}\right)\right)}{2(2+\Upsilon.\eta).\exp\left(-\Upsilon.\frac{Vdd}{Vt}\right)}\right] \quad (13)$$

- $V_{out}\ at\ V_{in} = V_{IH},\ V_{oih} =>$

$$\frac{Vt}{\Upsilon}\log\left[\frac{2+4.\exp\left(-\Upsilon.\frac{Vdd}{Vt}\right)-sqrt\left(\left(2+4.\exp\left(-\Upsilon.\frac{Vdd}{Vt}\right)\right)^2-4.\left(1+\frac{2}{\Upsilon\eta}\right)^2\exp\left(-\Upsilon.\frac{Vdd}{Vt}\right)\right)}{2(2+\Upsilon.\eta).\exp\left(-\Upsilon.\frac{Vdd}{Vt}\right)}\right] \quad (14)$$

- $V_{IH}, V_{IL} can\ be\ obtained\ by\ using\ corresponding\ V_{out} from\ above\ in, V_{in} =>$

$$\frac{1}{2}\left(Vdd-\eta.Vt.\log\left[\beta.\left(\frac{1-\exp\left(-\Upsilon.\frac{Vout}{Vt}\right)}{1-\exp\left(-\Upsilon.\frac{Vdd-Vout}{Vt}\right)}\right)\right]\right) \quad (15)$$

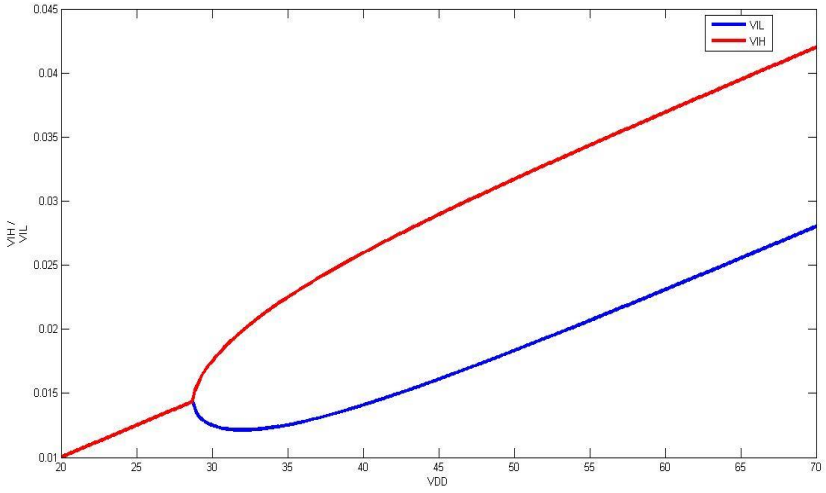


Figure 2.8: VIH and VIL vs. VDD

Figure 8 shows the variation of V_{IH} and V_{IL} with supply voltage. As expected V_{IH} and V_{IL} merge into one point after V_{DD} is scaled below a particular value given by equation 11.

- $V_{in}\ required\ for\ V_X = V_{IL} =>$

$$Vil\ -\frac{Vt}{\Upsilon}\left[1-\exp\left(\frac{Vil}{\eta.Vt}\right)\left\{\exp\left(\frac{Voil}{\eta.Vt}\right).\left(1-\exp\left(-\Upsilon.\left(\frac{Vil}{Vt}\right)\right)-\right.\right.\right.$$

$$\left.\left.\left.\frac{1}{\beta}.\exp\left(\frac{Vdd-Voil}{\eta.Vt}\right).\left(1-\exp\left(-\Upsilon.\frac{Vdd-Vil}{Vt}\right)\right)\right)\right\}\right] \quad (16)$$

- $V_{in}\ required\ for\ V_X = V_{IH} =>$

$$Vih+\frac{Vt}{\Upsilon}\left[1+\left\{\exp\left(\frac{Voih}{\eta.Vt}\right).\left(1-\exp\left(-\Upsilon.\left(\frac{Vih}{Vt}\right)\right)-\frac{1}{\beta}.\exp\left(\frac{Vdd-Voih}{\eta.Vt}\right).\left(1-\right.\right.\right.\right.$$

$$\left.\left.\left.\left.\exp\left(-\Upsilon.\frac{Vdd-Vih}{Vt}\right)\right)\right)\right\}\right] \quad (17)$$

β is ratio of I_{ON} and I_{OP}. The 'β' in current equation was neglected i.e. taken zero for these calculations

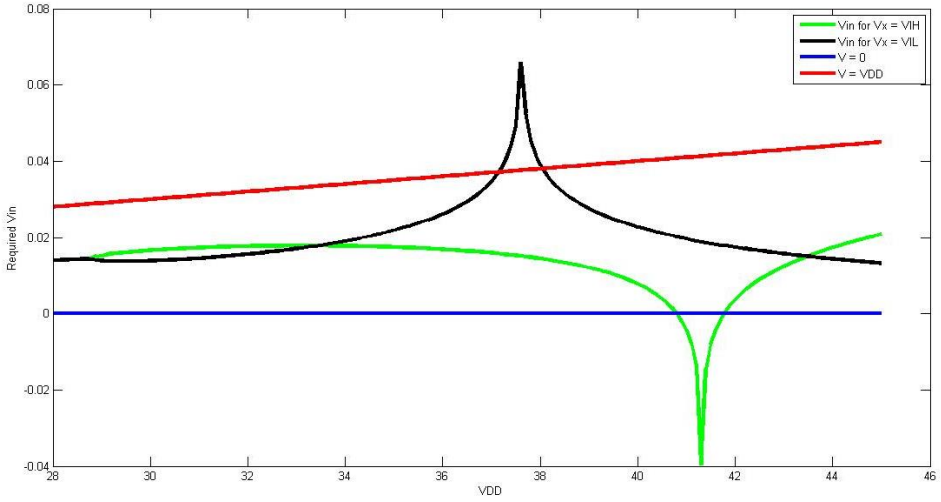


Figure 2.9 Curves for Vin required for Vx = VIH or VIL

From figure 9, it can be seen that minimum supply voltage need to be 42mV to avoid flipping of data in case of a zero write operation on some cell.

Results obtained from simulation were equal to what has been predicted by this analysis. Simulation shows 38mV minimum supply for avoiding flipping when V_{DD} is applied at V_{in} whereas 42mV in case 0 is applied to V_{in}. Hence minimum supply voltage of 42mV is needed for single pass transistor.

This analysis is considering single pass transistor, but actually it will be driven by two sides, so minimum supply voltage will be even higher. Simulation shows minimum supply voltage of 72mV is required to avoid data flipping. So for making a conservative guess for minimum

V_{DD} we can add the minimum V_{DD} needed in previous cases. So from our analysis it comes out to be 80mV which is quite close to simulation results.

2.7 Effect of temperature on minimum V_{DD}

Variation of minimum supply voltage with temperature for three category of circuit studied so far is summarized in table below:

Table 2.1 Variation of Vdd(min) for different circuits

Circuit	**T = 248K (-25°C)**	**T = 300K (27°C)**	**T = 400K (127°C)**
Inverter	20.9 mV	26.5 mV	37.8 mV
Pass transistor followed by latch	33 mV	42mV	57 mV
SRAM	63 mV	80mV	110 mV

.

CHAPTER 3

Look-up Table based Verilog-A models

3.1 Need of Verilog – A models

TCAD simulators take great amount of time to complete the simulation depending on device structure, meshing and various other factors. It can take days to complete a single 3D device simulation. The reason for such great simulation time is TCAD models are based on first principle, fundamental physics, and are too computationally complex. For analysis of circuits having transistor count greater than four analysis using device simulators may take several hours, hence is not feasible (in case of 2D simulations, in 3D even two device circuit simulation might not be feasible).

One of the solution to above problem is using Verilog-A model of device in circuit simulators such as Hspice. This helps in reducing simulation time greatly (a circuit with 100 transistors takes a few minutes, depending on the analysis, in SPICE) without the losing much of accuracy.

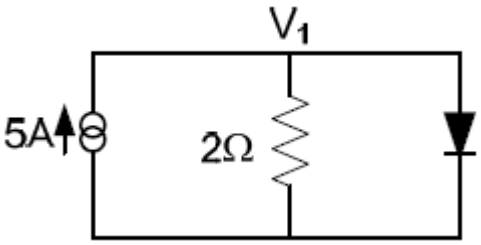
3.2 Basic idea for making a Verilog-A model

To understand how to create a Verilog-A model for a device we need to know how SPICE solve circuit level problems. SPICE constructs nodal equations for the circuit needed to be solved. This is done using net list. The equations are then rearranged in matrix form and solved using various matrix operations. It then solves for nodal voltages, satisfying KCL, by equation of the form given below:

$$[G] * [V] = [I]$$

The current matrix in above equation is usually known. For nonlinear elements, it forms equation which is transcendental i.e. it can only be solved numerically. For example, for a single diode circuit described below, we can write:

$$[0.5] * [V_1] = [5 - Is \exp\left(\frac{V_1}{V_t}\right)]$$



Which can be solved using the Newton - Raphson method. So for any model we must provide simulator value of terminal current as a function of terminal voltage. This can be done in one of following ways:

- By writing closed form empirical, device physics based, relation of terminal current in terms of terminal voltage i.e. a Compact Model
- By providing value of current directly for steps of possible voltage range, i.e. a table-based approach.

Compact Modeling is done using physics based constitutive equations. Bug fixing and improvement is a slow process in compact models. The advantage of table based models is that they are relatively simple and do not require device physics understanding for implementation. Beside this table-based models can be created in relatively less time, providing a faster alternative for circuit simulations with a high transistor count.

There are several disadvantages of the table based model, some of major disadvantages are:

- Table based models are can be derived for a particular set of conditions (for example for particular temperature), any change in condition would require extraction of data all over again.
- These are usually non-customizable, any change in device specification needs extraction of data all over again.
- Table based approach requires large run-time memory.

In the following sections a Verilog-A model for FinFETs is described.

3.3 A Look-up Table-based Verilog-A model for FinFET

In this section a Verilog-A model for FinFET device will be explained. This section is further divided as:

1. Device and Simulation Description
2. Extraction of I-V characteristics
3. Extraction of C-V characteristics
4. Table function in Verilog-A
5. Perl script for automation of task
6. Verilog-A model: Equations and Conventions.

3.3.1 Device and Simulation Description

Verilog-A model was extracted for a 16nm FinFETs whose parameters are explained in table below:

Table 3.1 Device Parameters

Parameter	**Value**	**Parameter**	**Value**
Gate Length L_G	16nm	Extension Length L_{ext}	16-20nm
Fin Width W_{fin}	≥ 8nm	S/D pad length L_{SD}	40nm
Fin Height H_{fin}	25nm	Channel Doping (N/P)	$1x10^{16}/1x10^{15}cm^{-3}$(As/B)
Oxide thickness t_{ox}	1.1nm	Pad Doping (N/P)	$1x10^{20}$ cm^{-3}(As/B)

For device simulations Sentaurus Technology TCAD is used. The technology parameters are in accordance with ITRS and drive current matches' roadmap targeted values. To match the device threshold with ITRS predicted value work function of Gate was tuned.

Appropriate physical models were used to account the scattering effects (ionized impurity scattering, carrier-carrier scattering) and mobility dependence on perpendicular and lateral field. Density-gradient transport model is used to include the carrier quantization effect. Figure 3.1 below shows the Device structure for NFET:

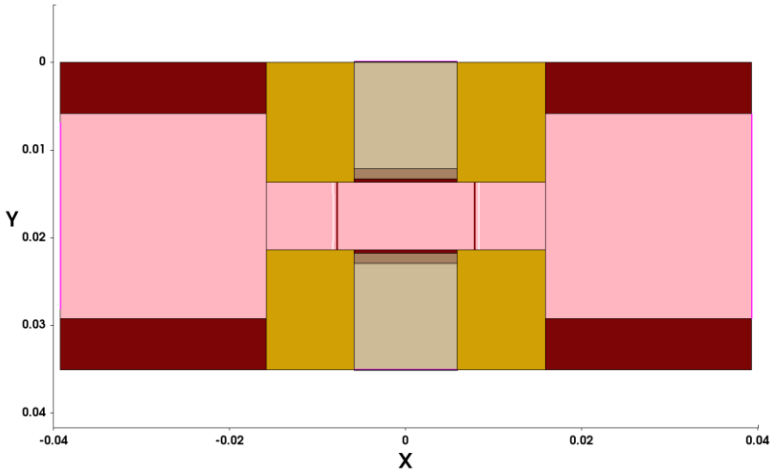


Figure 3.1: 16nm N-Type FinFET

Doping in Drain and Source extension regions is assumed to be Gaussian, while Constant for Drain/Source pad. Pad doping rolls off from the spacer, edge to Source/Drain extension region with gradient σ_L. 2D simulations are used for device parameter extraction without losing accuracy as referred in reference [13].

3.3.2 Extraction of I-V Characteristics

For our model we need to find drain current of FinFET as a function of terminal voltages for complete range of possible voltages. So we can basically say we need:

$$I = F (V_{GS} , V_{DS})$$

Where V_{GS} range from some negative value to +VDD for every discrete value of V_{DS} in range [- V_{DD} : V_{DD}] for NFET (for PFET V_{GS} will be swept from some positive value to -V_{DD}). Number of points in the range can be decided based on required accuracy level. For example we need to simulate for low voltage range o say 300mv, a step size of 10mv will give us only 30 points in range while 3mv step size will give us 100 points and hence better accuracy.

The negative value range of V_{GS} is not $-V_{DD}$ because of two reasons. Firstly, not all simulations will converge in TCAD simulation and other reasons for that is, it is a hypothetical case. (V_{GS} will not go below say 100mv in negative range) in real circuit operations.

To be on the safe side, it was swept from -0.4V to 1.1V (0.4V to -1.1V for PFET) in our model.

The final form of tables for I-V characteristics is as shown below:

# Vdrain = -1.10		
#Vds	**Vgs**	**Id**
-1.10	-0.40	-2.09870390000787E-05
-1.10	-0.39	-2.14580753204421E-05
-1.10	-0.38	-2.19291977448188E-05
……	……	……
……	……	……
……	……	……
……	……	……
-1.10	1.09	-7.67179917073861E-05
-1.10	1.10	-7.69859427380126E-05
# Vdrain = -1.09		
-1.09	-0.40	-2.05126687330198E-05
-1.09	-0.39	-2.09835212155468E-05
-1.09	-0.38	-2.14545095975271E-05
-1.09	-0.37	-2.19255843642856E-05
……	……	……
……	……	……

The '#' act as comment in table. While creating this table few things must be taken care off like significant digits in the value of a field should not change, for example, if the step size is 10mv then 1V should be written as 1.00V in the table. Also, values must be evenly spaced.

3.3.3 Extraction of C-V characteristics

Similar to I-V we need terminal capacitances of device as a function of terminal voltage. So we need C_{GD}, C_{GS}, $C_{DS,}$ as a function of V_{GS} and V_{DS} for the same range as in I-V characteristics. So we need a different table for each capacitance. The value of C_{DS} was very small compared to C_{GS} and C_{GD}, (smaller by an order of 10^5) therefore its contribution was neglected. The C_{GS} used over here is actually C_{SG} according to Sentarus TCAD conventions.

For capacitance extraction small signal AC simulation has to be performed on the device. Sentarus Devices computes **Y**-matrix for given device which describe change in current '**δi**' if terminal voltages face a small perturbation of '**δv**'. So $\mathbf{Y}_{12}$ represents change in current '**δi**' on terminal 1 for '**δv**' change in voltage at terminal 2.

From imaginary part of the **Y**-matrix capacitance values are extracted. AC small signal simulation can be performed in mixed-mode only.

Table format for capacitances is same as required for I-V. The only important thing is we need a different table for each capacitance.

3.3.4 Table Function in Verilog-A

'**$table_model()**' function in Verilog-A enables module in approximating system behavior by interpolating between user supplied data points. Sample data points can be provided either by an array or by file. Data file must be in text format with each sample separated by new line. Number in sequence can take real and integer value only. Also sequences should be separated by spaces or tab.

Syntax:

$table_model (table_inputs, table_data_source, table_control);

table_inputs are independent numerical expressions used as table input

table_data_source indicates the name of the file (table data file) or the name of an array.

table_control_is a string with two parts. The first part is integer which indicates the degrees of the spline interpolation (1-Linear spline, 2-Quadratic spline, 3-Cubic spline). The second part can have one or two characters (C-Clamp extrapolation, L-Linear extrapolation, E-Error condition). It is used to indicate extrapolation mode outside the data range i.e at the beginning and end of the data.

Example : "2CE,1EL" indicates "2nd dimension quadratic interpolation, clamp on extrapolation to left, error on extrapolation to right, 1st dimension linear interpolation, error on extrapolation to left, linear extrapolation on right"

3.3.5 Perl script for automation of data extraction

Process of data extraction for table based model is time consuming and really difficult to carry out accurately manually. The problem was tackled by automating the process using PERL scripting. Script.

3.3.6 Verilog-A Model: Equations and Conventions

Current equations becomes quite simple for table based models since there is no physics involved. Another factor contributing to simplicity of equation in our model is range over which data is extracted. Since we have values of current from $-V_{DD}$ to V_{DD} for practical range of V_{GS} we need not to worry about Drain/Source terminal exchange and thus we need not to write different equations in case of terminal exchange.

Drain current equation for the model can simply be written as:

$$I(d) <+ N_{fin} * (I_D + C_{GD} * \mathbf{ddt}(V(d,g)));$$

Where for particular terminal voltages

N_{fin} is number of fins in device,

I_D is Drain current from extracted I-V characteristics or 'DC' current value,

C_{GD} is extracted capacitance between Gate and Drain terminal (For Source terminal C_{GS} should replace it),

V(d,g) is voltage between Gate and Drain terminals of module

Complete Verilog-A model can be found in appendix at the end of report. Current equation has two parts to it, first part (I_D) simply represent dc value of current based on terminal voltages while second part capture contribution of C_{GD} in total current for change in V_{GD} using derivative function '**ddt**'.

Special care need to be taken while choosing signs as these must follow SPICE current conventions to avoid convergence issues and weird terminal voltages. Current going out of a terminal is negative while current into a terminal is positive.

N_{fin} in the model just multiply the current values by number of fins and do not take into account any other effect. So although it can be varied for circuit purpose but results might not be very accurate. A study needs to be done to compare difference between model results and actual Sentarus results.

3.4 Comparison between SPICE and TCAD results

For comparison between SPICE and TCAD we performed dc and transient simulations. First we compared VTC for an inverter. Results shows less than 2mV error in threshold voltage of inverter. Figure below shows inverter VTC as predicted by TCAD and SPICE.

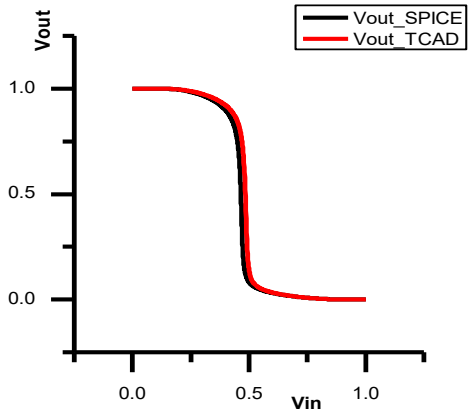


Figure 3.2: Inverter VTC: TCAD vs. SPICE

Apart from DC simulation transient results were also compared. The fact that output waveform matches to a great extent in case of transient response justifies our assumption of neglecting C_{DS}.

For further comparison, results of a three stage buffer chain were compared between SPICE and TCAD. Simulation setup of same is described in figure 3.2, load has been kept so as to avoid any drag effect at V_{OUT2}. Output waveforms for the same are shown in figure 3.3.

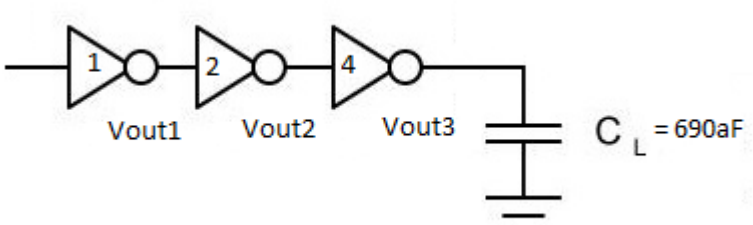


Figure 3.3: Three stage buffer with 124 loading

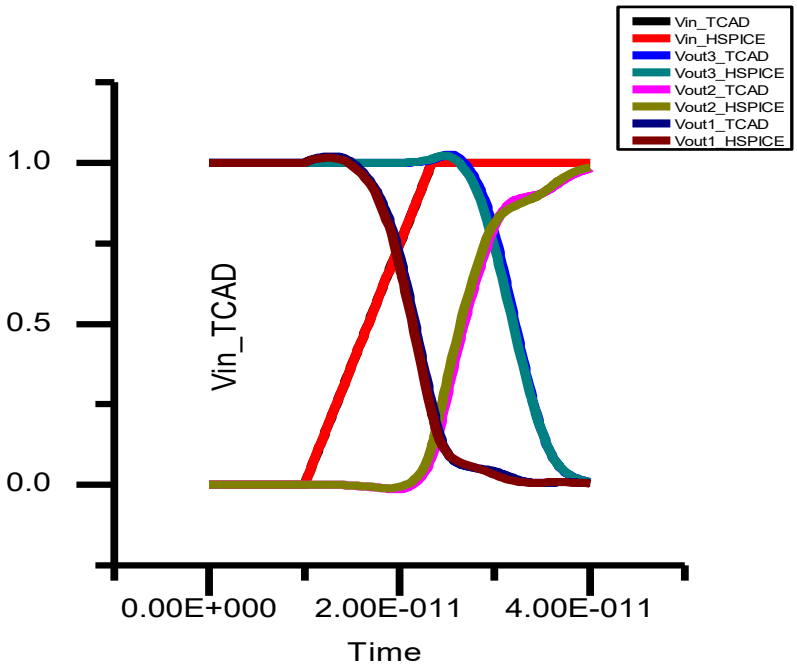


Figure 3.4: Output Comparison: 3 Stage inverter

Further simulations were carried out to see if such table based model is reliable for studying various device based effect. For this purpose, Sentarus TCAD and SPICE results were compared for three inverter chain to study drag phenomena as mentioned in [14]. Results for the same are described in following section.

Table 3.1: Delay Comparisons

Voltage Node	HSPICE	TCAD
Vout1	4.6787p	4.907p
Vout2	9.7057p	10.093p
Vout3	15.233p	15.458p

Table 3.2: Transition time comparison

Voltage Node	HSPICE	TCAD
Vout1	4.6728p	4.6486p
Vout2	5.6676p	5.539p
Vout3	5.1389p	4.782p

3.4.1 A comparative study between SPICE and TCAD results for a five inverter chain

It has been reported in [14], that a region of drag is observed in transition of input node voltage of an inverter in a FinFET buffer chain if loading on this inverter is less than what it provide to previous stages.

Simulation setup:

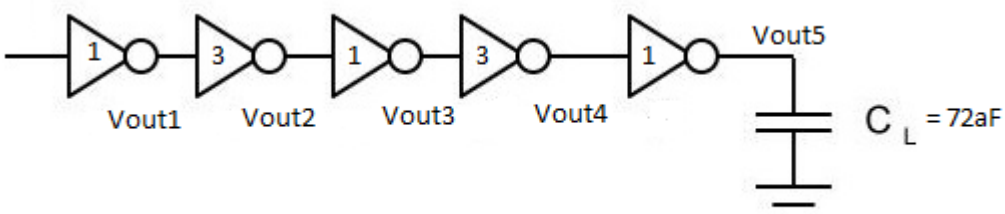


Figure 3.5: Simulation setup for 5 inverter buffer chain

A chain of 5 inverter was setup with loading as shown in figure. As explained in [14] such loading should cause a different kind of voltage transition i.e a period of slow transition should be observed at input nodes of inverters with 3 Fins (this effect has been called Drag).

Comparison of SPICE and TCAD results for 5 inverter chain:

- We can see drag effect clearly in the output waveforms for loadings reported in reference.
- The drag effect begins to appear at Vout of 0.3999 V in spice and at 0.372 V in sentarus, i.e. it's observed early in SPICE.
- Although at time = 19.995 ps value of both simulators was very close. Vout was 0.37016 V in sentarus and 0.3999 V in SPICE.
- This is also visible in curves plotted above. Onset of drag is almost at same time for all curves. Voltage magnitude differs after onset only.
- Simulation time for Sentarus TCAD was 3 hours while spice simulations were completed in few seconds.

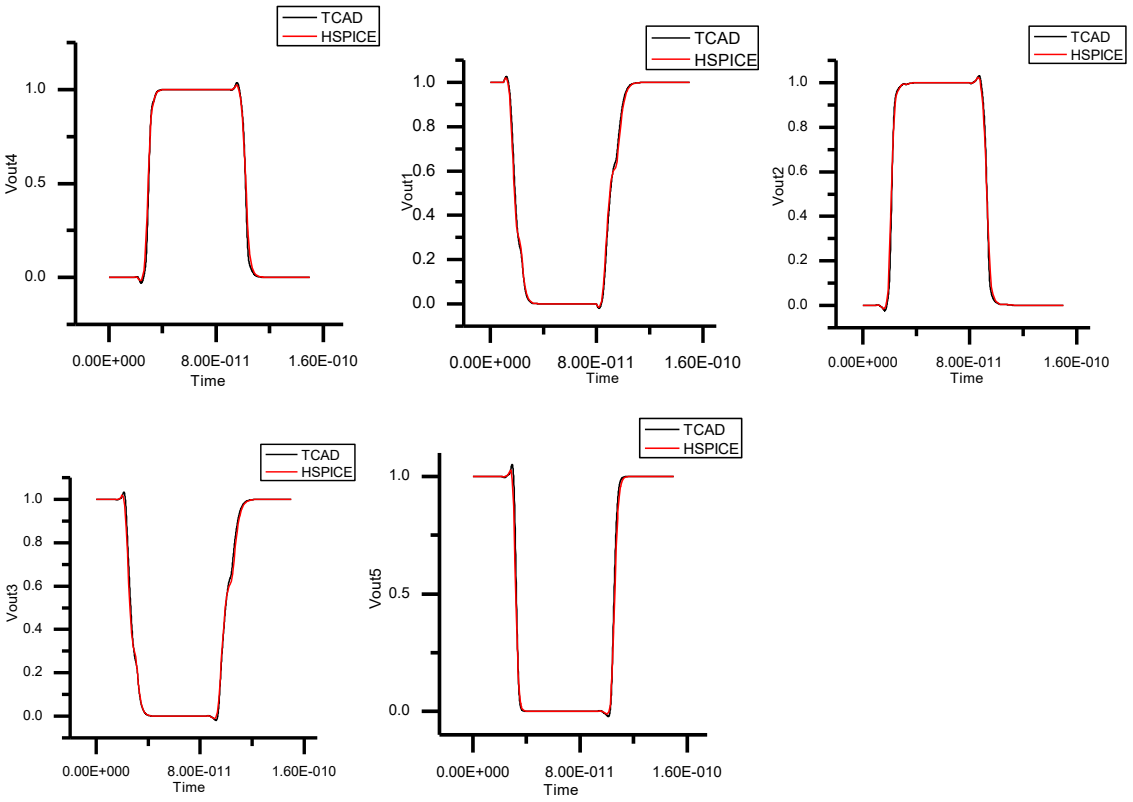


Figure 3.6: Output Waveform Comparision between SPICE and TCAD

For confirmation purpose a simulation for 13631 type of loading was done. As expected drag wasn't observed at Vout1 while we can clearly see drag effect at Vout2. These results confirms that such type of table based models capture various device level effects i.e. they can be used for such purposes without much loss of accuracy.

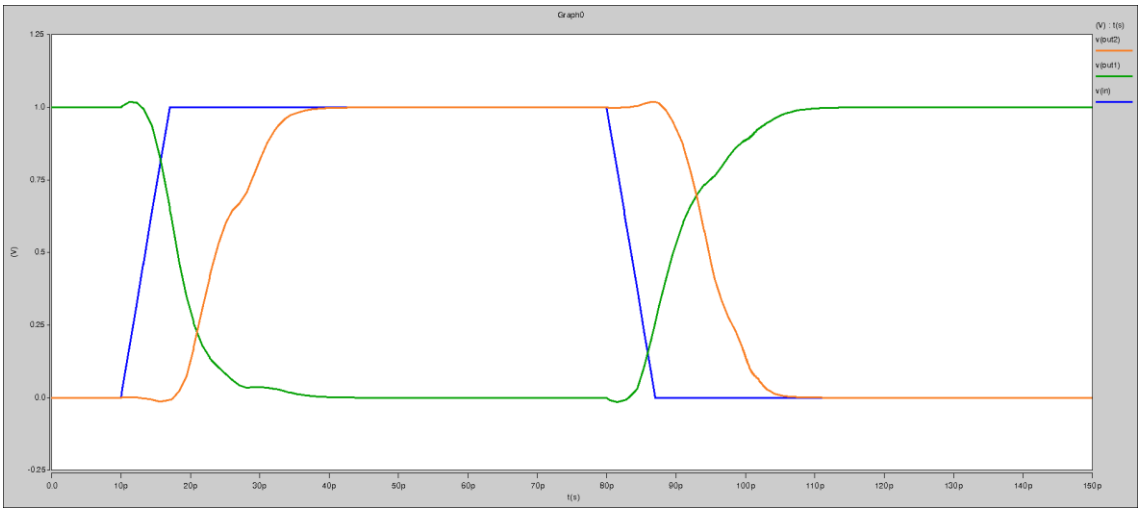


Figure 3.7: Output waveforms for Buffer with 13631 sizing

CHAPTER 4

CONCLUSION AND FUTURE WORK

4.1 CONCLUSION

Previous work on fundamental limits for supply voltage for MOSFETs is not sufficient to capture such limits for FinFET circuits. Owing to double gate structure, a potential well is formed in the channel at very low drain voltages. Adding to it, the channel length is smaller than depletion region required for balancing Fermi level of drain and channel. These cause trapped charge in the channel. To include contribution of this trapped charge sub-threshold current equation for FinFET is different from that for MOSFET.

In this work a foundation has been laid for further research into fundamental limit of FinFET circuits. A current equation for sub-threshold conduction has been derived semi-empirically and it's comparison with TCAD results prove its accuracy in predicting various trends and for solving circuit level problems analytically. Using this modified equation for sub-threshold current fundamental limit for minimum supply voltage has been derived for FinFET inverter. The fundamental supply voltage limit for FinFETs has been found lower than that for MOSFET, making FinFETs an ideal candidate for ultra-low voltage applications.

Adding to this, problem of sizing pass transistors in clocked circuit at such low voltage has been addressed. It has been shown that pass transistor size should be kept greater than pull down device of inverter otherwise minimum supply voltage will be higher than that predicted by fundamental limit equation. Same sizing requirements are valid for SRAM. Sizing becomes critical at such low voltage of operation. For example if SRAM circuit is not sized properly, as explained in this work, we may end up writing data in some cells unintentionally.

A methodology for predicting minimum V_{DD} has been formulated. Finally variability of minimum supply voltage with temperature, has been addressed for different circuit. Results shows this fundamental limit is higher at higher temperature.

Another issue of simulating circuits with large transistor count is solved using existing technique of table based Verilog-A model. Device simulators like TCAD are not suitable for simulating large circuits. A faster approach is using a Verilog-A model for device in circuit

simulators like H-SPICE. A table-based Verilog-A model for such purpose has been created along with automation of the process involved in extraction of required data for the same. This has been done using Perl scripting language.

4.2 FUTURE SCOPE

This work is theoretical at the moment. Performance at supply voltage close to fundamental limit will be very poor. So it need to be extended further to consider other variability issues, like Fin width and channel doping. Taking variability and noise into consideration, a practical limit for supply voltage can be determined. Next an analysis can be done between supply voltage and performance, this will help in selecting optimum supply voltage for a given application. Next, an analysis for performance improvement using architecture level changes can be done and better architecture for basic circuit can be suggested.

References

[1] M. M. Alioto, “Ultra-low power VLSI circuit design demystified and explained: A Tutorial”, IEEE Transactions on Circuits and Systems I – Regular Papers, vol. 59, no.1, Jan 2012.

[2] A. Cardoso, L. de Carli, C. Galup-Montoro, M.C.Schneider, “Analysis of the rectifier circuit valid down to its low-voltage limit”, IEEE Transactions on Circuits and Systems I – Regular Papers, vol. 59, no.1, Jan 2012.

[3] J.Rabaey, “The swarm: what it means to Microsystems education”, IEEE Microelectronic systems Education (MSE), San Diego, Jun 2011, http://www.mseconference.org/ SwarmKeynoteMSE11.pdf.

[4] Robert W. Keyes, “Fundamental Limits in Digital Information Processing”, Proceedings of the IEEE, vol. 69, NO. 2, February 1981.

[5] Luiz A.P.Melek, Marcio C.Schneider, and Carlos Galup-Montoro, “Ultra-Low Voltage CMOS Logic Circuits”, 2014 Argentine School of Micro-Nanoelectronics, Technology and Applications.

[6] J. D. Meindl and J. A. Davis, “The fundamental limit on binary switching energy for terascale integration (TSI),” IEEE Journal of Solid-State Circuits, vol. 35, no. 11, pp. 1515-1516, Oct 2000.

[7] J. von Neumann, Theory of Self-Reproducing Auotomata Urbana, IL. Univ. Illinios Press, 1966, p. 66

[8] R. W. Landauer, “Irreversibility and heat generation in the computing process,” IBM J. Res. Develop., pp. 183-191, 1961

[9] A. W. Lo, “Physical realization of digital logic circuits”, in Micropower Electronics, E. Keonjian, Ed. New York, NY: Macmilan, 1964, pp. 19-39

[10] R. M. Swanson and J. D. Meindl, “Ion-implanted complementary MOS transistor in low-voltage circuits”, IEEE J. Solid-State Circuits, vol. SC-7, pp. 1146-1152, Apr. 1972

[11] S. Hanson, B. Zhai, K. Bernstein, D. Blaauw, A. Bryant, L. Chang, K. K. Das, W. Haensch, E. J. Nowak, D. M. Sylvester, “Ultralow-voltage, minimum-energy CMOS”, IBM J. RES. & DEV. vol. 50 No. 4/5 July/September 2006.

[12] Rajiv Joshi, Sudesh Saroop, Rouwaida Kanj, Yang Liu, Weik Wang, Carl Radens, Yue Tan, and Karthik yogendra, “ A Universal Hardware-Driven PVT and Layout-Aware Predictive Failure Analytics for SRAM”, IEEE Transections on Very Large Scale Integration (VLSI) SYSTEMS, vol. 24, No. 3, March 2016

[13] Archana Pandey, Swati Raycha, Satish Maheshwaram, Sanjeev K. Manhas, Sudeb Dasgupta, Ashok K. Saxena, and Bulusu Anand, "Effect of Load Capacitance and Input Transition Time on FinFET Inverter Capacitances", IEEE Transection on Electron Devices, vol. 61, No. 1, January 2014.

[14] Archana Pandey, Harsh Kumar, S. K. Manhas, S. Dasgupta and Bulusu Anand, "A typical Voltage transitions in FinFET Multi-Stage Circuits: Origin and Significance", IEEE Transection on Electron Devices, vol. 63, No. 3, March 2016

[15] I. E. Sutherland, R. F. Sproull, and D. Harris, *Logical Effort: Designing Fast CMOS Circuits.* San Mateo, CA, USA: Morgan Kaufmann, 1998.

[16] Sentaurus TCAD Manuals, Synopsys Inc., Mountain View, CA, USA, 2009.

[17] A. Pandey, S. Raycha, S. Maheshwaram, S. K. Manhas, S. Dasgupta, A. K. Saxena, et al., " FinFET device capacitances: Impact of input transition time and output load", in Proc. IEEE 5th INEC, Jan. 2013, pp. 393-395.

[18] L. Lemaitre, G. Coram, C. McAndrew, K. Kundert, "Extensions to Verilog-A to Support Compact Device Modeling", Behavioral Modeling and Simulation, 2003. BMAS 2003. Proceedings of the 2003 International Workshop on 7-8 Oct. 2003, pp. 134-138

[19] James D. Meindl, "Low Power Microelectronics: Retrospect and Prospect", Proceedings of the IEEE, vol -83, No. 4, April 1995.

[20] Richard M. Swanson and James D. Meindl, "Ion-Implanted Complementary MOS Transistors in Low-Voltage Circuits", IEEE Journal of solid-state circuits, vol. sc-7, No. 2, April 1972.

[21] Chia-Hsiang Chen, Keith Bowman, Charles Augustine, Zhengya Zhang, and Jim Tschanz, "Minimum Supply Voltage for Sequential Logic Circuits in a 22nm Technology", Symposium on Low Power Electronics and Design, 4-6 Sept 2013, pp. 181-186.

[22] Open Verilog International, "Verilog-A Language Reference Manual", Version 1.0, August 1, 1996.

[23] S. M. SZE, *Semiconductor devices Physics and Technology Second Edition,* Jhon Wiley & Sons, 2002.

[24] Jean-Pierre Colinge, *FinFETs and Other Multi-Gate Transistors*, Springer Science+Business Media, LLC, 2008.

[25] International Roadmap Committee, Denver, CO, USA, (2010). *Process Integration, Devices and Structures* [Online]. Available: ttp://www.itrs.net/

[26] Xiaoxia Wu, Feng Wang, Yuan Xie, "Analysis of Subthreshold FinFET Circuits for Ultra-Low Power Design", IEEE International SOC Conference, 2006, pp. 91-92.

[27] Xue Lin, Yanzhi Wang, Massoud Pedram, "Stack Sizing Analysis and Optimization for FinFET Logic Cells and Circuits Operating in the Sub/Near-Threshold Regime", 15th International Symposium on Quality Electronic Design, 2014, pp. 341-348.

[28] Azzedin Es-Sakhi, Masud H Chowdhury, “Analytical model to estimate the subthreshold swing of SOI FinFET”, Electronics, Circuits, and Systems (ICECS), IEEE 20th International Conference, 2013, pp. 52-55.

[29] Qing Xie, Xue Lin, Yanzhi Wang, Mohammad Javad Dousti, Alireza Shafaei, Majid Ghasemi-Gol, Massoud Pedram, “5nm FinFET Standard Cell Library Optimization and Circuit Synthesis in Near- and Super-Threshold Voltage Regimes”, 2014 IEEE Computer Society Annual Symposium on VLSI, 2014, pp. 424-429.

[30] Kaushik Roy, Saibal Mukopadhyay, and Hamid Mahmoodi-Meimand, “Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicrometer CMOS Circuits”, Proceedings of the IEEE, vol. 91, No. 2, February 2003, pp. 305-327.

[31] S. Ohbayashi, et al., “A 65nm SoC embedded 6T-SRAM designed for manufacturability with read and write operation stabilizing circuits,” JSSC, pp. 820-829, April 2007.

[32] E. Karl, et al., “A 4.6GHz 162Mb SRAM design in 22nm tri-gate CMOS technology with integrated active V_{MIN}-enhancing assist circuitry,” in ISSCC, 2012, pp.230-231.

[33] X. Du, et al. “A Most probable point based method for uncertainty analysis,” J. Design and Manufacturing Automation, pp. 47-65, Feb. 2001.

[34] HSPICE® User Guide: Simulation and Analysis, Synopsis Inc., Version E-2010.12, December 2010.

PUBLICATIONS

[1]. A. Pandey, P. Garg, **S. Tyagi,** and B. Anand "A Modified Method of Logical Effort for FinFET Circuits Considering Impact of Transition Times on Fin-Extension Effects" [To be Communicated in IEEE journal]

APPENDIX – A: Table based Verilog – A Model for FinFET

Verilog-A Model for NFET is given below. This model is independent of device type (i.e. NFET or PFET it remains same). Only thing that need to be taken care of is sign conventions for different current components which ultimately depend on data extraction.

```
`include "disciplines.vams"
`include "constants.vams"

module N_FINFET (d,g,s,b); //Module definition for NFET

inout d,g,s,b;     // drain, gate, source, dummy bulk are in-out port of module
electrical d,g,s,b;

//Parameters
parameter real Nfin = 1 from (0:inf); // Parameter to change Number of Fins
parameter real dVth = 0 from (-inf:inf);
parameter real dVth0 = 0 from (-inf:inf);

// Variables used in code
real Vgs,Vds;
real Id;
real Cgs,Cgd;
real Id_tmp,Cgs_tmp,Cgd_tmp;
real Hfin, tsin;

// Table control parameter for $table_model() function
parameter string ecsId = "1L,1L";
parameter string ecsC = "1C,1C";
// Linear extrapolation of data outside range for I_D and Clamp for Capacitance
// First Degree interpolation for intermediate values
```

analog begin : finfet_module *// Beginning of FinFET module*

```
tsin = 8e-3;   // in um, not used in code for anything
Hfin = 1;
 // Height is already considered by Area factor in TCAD simulation hence kept unity.
Vds = V(d,s);
Vgs = V(g,s)-dVth-dVth0;

// Assigning values to temporary current and voltage variable from table
Id_tmp    =  $table_model(Vds,Vgs,"IdVg-NFET-Lg-11pt7nm.tbl",ecsId);
Cgs_tmp = -$table_model(Vds,Vgs,"CGS-NFET-Lg-11pt7nm.tbl",ecsC);
Cgd_tmp = -$table_model(Vds,Vgs,"CGD-NFET-Lg-11pt7nm.tbl",ecsC);
Id=Id_tmp;
Cgs=Cgd_tmp;
Cgd=Cgs_tmp;

I(d)<+Nfin*Hfin*(Id+Cgd*ddt(V(d,g)));
I(s)<+Nfin*Hfin*(-Id+Cgs*ddt(V(s,g)));
I(g)<+Nfin*Hfin*(+Cgd*ddt(V(g,d))+Cgs*ddt(V(g,s)));
//Verilog-A uses <+ to indicate a contribution to the voltage or current of a branch

end
endmodule
```

APPENDIX-B: Minimum Supply Voltage for an FinFET Inverter

Static transfer function of inverter is given by:

$$I_{DN} = I_{DP}$$

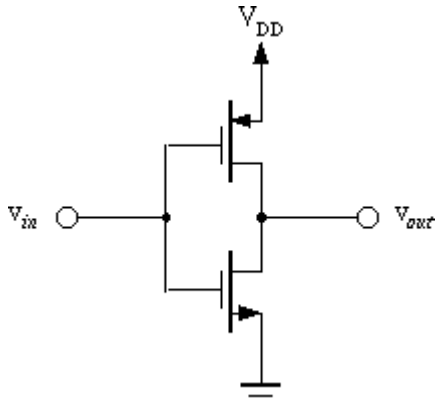


Figure B.1: CMOS Inverter

Using equation (10), for drain current of FinFET device we can write,

$$I_{oN} \exp\left(\frac{V_{in}}{\eta V_t}\right)\left[1 - \exp\left(-\frac{\Upsilon V_{out}}{V_t}\right)\right] = I_{oP} \exp\left(\frac{V_{DD} - V_{in}}{\eta V_t}\right)\left[1 - \exp\left(-\frac{\Upsilon (V_{DD} - V_{in})}{V_t}\right)\right]$$

The term β, in equation 10 has been neglected for making calculation easier. This assumption is justified later. By rearranging the terms in above expression we get:

$$\frac{V_{DD} - 2V_{in}}{\eta V_t} = log_e\left(\frac{I_{oN}}{I_{oP}}\right) + log_e\left(\frac{\left(1 - \exp\left(-\frac{\Upsilon V_{out}}{V_t}\right)\right)}{1 - \exp\left(-\frac{\Upsilon (V_{DD} - V_{out})}{V_t}\right)}\right) \qquad (B.1)$$

At minimum supply voltage, gain of FinFET inverter must be at least unity, at inversion point i.e. at $V_{in} = V_{out}$. Differentiating equation B.1 with respect to V_{in} we get:

$$-\frac{2}{\eta V_t} = A\left(-\frac{\Upsilon}{V_t}\right)\left[\frac{\left(\exp\left(-\frac{\Upsilon V_{out}}{V_t}\right) - \exp\left(-\frac{\Upsilon V_{DD}}{V_t}\right) + \exp\left(-\Upsilon\left(\frac{V_{DD} - V_{out}}{V_t}\right)\right) - \exp\left(-\frac{\Upsilon V_{DD}}{V_t}\right)\right)}{1 - \exp\left(-\frac{\Upsilon V_{out}}{V_t}\right) - \exp\left(-\frac{\Upsilon (V_{DD} - V_{out})}{V_t}\right) + \exp\left(-\frac{\Upsilon V_{DD}}{V_t}\right)}\right] \qquad (B.2)$$

Where, $A = \frac{dV_{out}}{dV_{in}}$

Assuming $I_{oN} = I_{oP}$, i.e. symmetric voltage transfer curve for inverter, we can take

$$V_{in} = V_{out} = \frac{V_{DD}}{2} \tag{B.3}$$

Now using B.3 in B.2 along with condition for minimum voltage, i.e. $A = -1$, we have,

$$\frac{2}{\eta V_t} = \frac{\Upsilon}{V_t}\left[\frac{2\exp\left(-\frac{\Upsilon V_{DD}}{2V_t}\right) - 2\exp\left(-\frac{\Upsilon V_{DD}}{V_t}\right)}{\left(1-\exp\left(-\frac{\Upsilon V_{DD}}{2V_t}\right)\right)^2}\right] \tag{B.4}$$

Solving B.4 for V_{DD},

$$V_{DD}(min) = \frac{2V_t}{\Upsilon} log_e(1 + \eta\Upsilon) \tag{B.5}$$

At 300^oK, $V_{DD}(min) = 26mV$, while minimum supply voltage comes out to be 28-29 mV from TCAD simulation which justifies our initial assumptions too.

APPENDIX C: Equations for Analysis of Pass Transistor followed by Latch

For equation 13 and 14 in chapter 2 we can use equation B.2 from appendix B, i.e.

$$-\frac{2}{\eta V_t} = A\left(-\frac{\Upsilon}{V_t}\right)\left[\frac{\left(\exp\left(-\frac{\Upsilon V_{out}}{V_t}\right)-\exp\left(-\frac{\Upsilon V_{DD}}{V_t}\right)+\exp\left(-\Upsilon\left(\frac{V_{DD}-V_{out}}{V_t}\right)\right)-\exp\left(-\frac{\Upsilon V_{DD}}{V_t}\right)\right)}{1-\exp\left(-\frac{\Upsilon V_{out}}{V_t}\right)-\exp\left(-\frac{\Upsilon(V_{DD}-V_{out})}{V_t}\right)+\exp\left(-\frac{\Upsilon V_{DD}}{V_t}\right)}\right]$$

Using $A = -1$, we will get a quadratic in $\exp\left(\frac{\Upsilon V_{out}}{V_t}\right)$,

$$\left(1+\frac{2}{\eta\Upsilon}\right)\exp\left(-\frac{\Upsilon V_{DD}}{V_t}\right)\left(\exp\left(\frac{\Upsilon V_{out}}{V_t}\right)\right)^2-\left(\frac{2}{\eta\Upsilon}+\frac{4}{\eta\Upsilon}\exp\left(-\frac{\Upsilon V_{DD}}{V_t}\right)\right)\exp\left(\frac{\Upsilon V_{out}}{V_t}\right)+\left(1+\frac{2}{\eta\Upsilon}\right)=0 \quad \text{(C.1)}$$

By solving equation C.1, values of V_{oil} and V_{oih} can be given as:

$$V_{out}\ at\ V_{in} = V_{IL},\ V_{oil} =>$$

$$\frac{Vt}{\Upsilon}\log\left[\frac{2+4.\exp\left(-\Upsilon.\frac{Vdd}{Vt}\right)+sqrt\left(\left(2+4.\exp\left(-\Upsilon.\frac{Vdd}{Vt}\right)\right)^2-4.\left(1+\frac{2}{\Upsilon\eta}\right)^2\exp\left(-\Upsilon.\frac{Vdd}{Vt}\right)\right)}{2(2+\Upsilon.\eta).\exp\left(-\Upsilon.\frac{Vdd}{Vt}\right)}\right] \quad \text{(C.2)}$$

And,

$$V_{out}\ at\ V_{in} = V_{IH},\ V_{oih} =>$$

$$\frac{Vt}{\Upsilon}\log\left[\frac{2+4.\exp\left(-\Upsilon.\frac{Vdd}{Vt}\right)-sqrt\left(\left(2+4.\exp\left(-\Upsilon.\frac{Vdd}{Vt}\right)\right)^2-4.\left(1+\frac{2}{\Upsilon\eta}\right)^2\exp\left(-\Upsilon.\frac{Vdd}{Vt}\right)\right)}{2(2+\Upsilon.\eta).\exp\left(-\Upsilon.\frac{Vdd}{Vt}\right)}\right] \quad \text{(C.3)}$$

As given in chapter 2. We can differentiate between V_{oil} and V_{oih} from the solutions of C.1 because at V_{IL}, V_{OUT} will be higher than V_{OUT} when input is V_{IH}.

Next, equation 15 can be obtained from equation B.2 as,

$$\frac{V_{DD}-2V_{in}}{\eta V_t} = log_e\left(\frac{I_{oN}}{I_{oP}}\right)+\ log_e\left(\frac{\left(1-\exp\left(-\frac{\Upsilon V_{out}}{V_t}\right)\right)}{1-\exp\left(-\frac{\Upsilon(V_{DD}-V_{out})}{V_t}\right)}\right)$$

Rearranging terms and solving for V_{in},

$$V_{in} = \frac{1}{2}\left(Vdd - \eta.Vt.\log\left[\beta.\left(\frac{1-\exp\left(-\Upsilon.\frac{Vout}{Vt}\right)}{1-\exp\left(-\Upsilon.\frac{Vdd-Vout}{Vt}\right)}\right)\right]\right) \quad \text{(C.4)}$$

Where $\beta = \left(\frac{I_{oN}}{I_{oP}}\right)$,

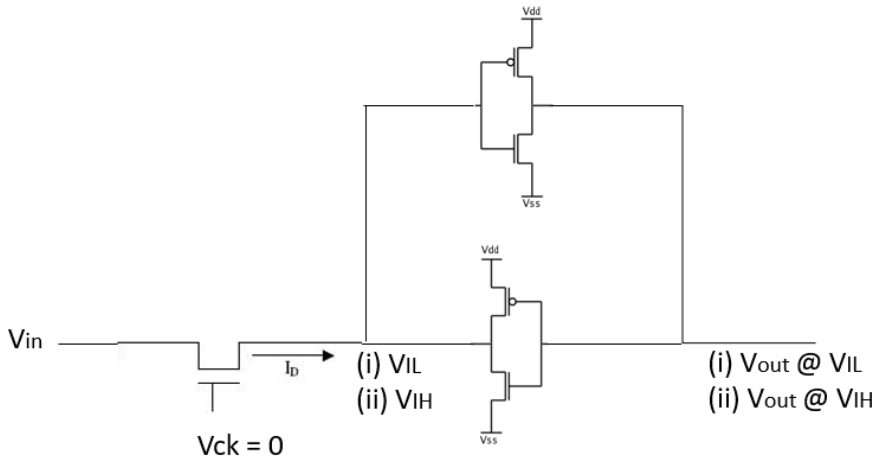


Figure C.1: Pass Transistor followed by Latch

For equation 16 and 17 we need to solve for V_{in} for two cases given in figure C.1.

Case (i):

$$I_{oN}\exp\left(-\frac{V_{IL}}{\eta V_t}\right)\left(1-\exp\left(-\frac{\Upsilon(V_{in}-V_{IL})}{V_t}\right)\right) + I_{oP}\exp\left(\frac{V_{DD}-V_{oil}}{\eta V_t}\right)\left(1-\exp\left(-\frac{\Upsilon(V_{DD}-V_{IL})}{V_t}\right)\right) =$$
$$I_{oN}\exp\left(\frac{V_{oil}}{\eta V_t}\right)\left(1-\exp\left(-\frac{\Upsilon V_{IL}}{V_t}\right)\right) \quad \text{(C.5)}$$

Solving C.5 for V_{in},

$$V_{in} => Vil - \frac{Vt}{\Upsilon}\left[1-\exp\left(\frac{Vil}{\eta.Vt}\right)\left\{\exp\left(\frac{Voil}{\eta.Vt}\right).\left(1-\exp\left(-\Upsilon.\left(\frac{Vil}{Vt}\right)\right) - \right.\right.\right.$$
$$\left.\left.\left.\frac{1}{\beta}.\exp\left(\frac{Vdd-Voil}{\eta.Vt}\right).\left(1-\exp\left(-\Upsilon.\frac{Vdd-Vil}{Vt}\right)\right)\right)\right\}\right] \quad \text{(C.6)}$$

Case (ii):

$$I_{oN}\exp\left(-\frac{V_{in}}{\eta V_t}\right)\left(1-\exp\left(-\frac{\Upsilon(V_{IH}-V_{in})}{V_t}\right)\right)+\ I_{oN}\exp\left(\frac{V_{oih}}{\eta V_t}\right)\left(1-\exp\left(-\frac{\Upsilon V_{IH}}{V_t}\right)\right)=$$
$$I_{oP}\exp\left(\frac{V_{DD}-V_{oih}}{\eta V_t}\right)\left(1-\exp\left(-\frac{\Upsilon(V_{DD}-V_{IH})}{V_t}\right)\right) \quad \text{(C.7)}$$

The term, $\exp\left(-\frac{V_{in}}{\eta V_t}\right)$ makes the expression difficult to solve, in practical circuits gate of pass transistor will se a voltage V_{OL} rather than ground and V_{in} itself will be close to ground at minimum permissible supply voltage. With these observation we assume V_{GS} for pass transistor to be zero. Now equation C.7 can be written as

$$I_{oN}\left(1-\exp\left(-\frac{\Upsilon(V_{IH}-V_{in})}{V_t}\right)\right)+\ I_{oN}\exp\left(\frac{V_{oih}}{\eta V_t}\right)\left(1-\exp\left(-\frac{\Upsilon V_{IH}}{V_t}\right)\right)=$$
$$I_{oP}\exp\left(\frac{V_{DD}-V_{oih}}{\eta V_t}\right)\left(1-\exp\left(-\frac{\Upsilon(V_{DD}-V_{IH})}{V_t}\right)\right) \quad \text{(C.8)}$$

Solving equation C.8 for V_{in},

$$V_{in}\ \Rightarrow Vih+\frac{Vt}{\Upsilon}\left[1+\left\{\exp\left(\frac{Voih}{\eta.Vt}\right).\left(1-\exp\left(-\Upsilon.\left(\frac{Vih}{Vt}\right)\right)-\frac{1}{\beta}.\exp\left(\frac{Vdd-Voih}{\eta.Vt}\right).\left(1-\right.\right.\right.\right.$$
$$\left.\left.\left.\left.\exp\left(-\Upsilon.\frac{Vdd-Vih}{Vt}\right)\right)\right)\right\}\right] \quad \text{(C.9)}$$