Radiation Induced Soft Errors in CMOS Circuits

A Seminar Report in partial fulfillment of the requirements for the degree of

MASTER OF TECHNOLOGY

In

Electronics and Communication Engineering

(With specialization in Microelectronics and VLSI)

Submitted by

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May, 2016

Candidates' Declaration

I hereby declare that the work which is being presented in the project report entitled "***Radiation Induced Soft Errors in CMOS Circuits***" in the partial fulfillment of the requirement of the degree of Master of Technology in Electronics & Communication Engineering is an authentic record of my own work carried out under the precise guidance of Mr. Abhishek Jain, Department of TrND, ST Microelectronics, Noida and Dr. Sanjeev Manhas & Dr. Sudeb Dasgupta, Department of Electronics and Communication, IIT Roorkee.

Date: Akash Gupta

Place: Roorkee (14534001)

Certificate

This is to certify that the information given by the candidate in this report is correct in best to my knowledge.

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Acknowledgement

With due respect, I express my deep sense of gratitude to my supervisors, Mr. Abhishek Jain, Department of TrND, ST Microelectronics, Noida and Dr. Sanjeev Manhas & Dr. Sudeb Dasgupta, Department of Electronics and Communication Engineering at Indian Institute of Technology, Roorkee for their valuable guidance and continuous support. I am very thankful to them for the encouragement they have given me to carry on with my research work.

I am extremely grateful to all the faculty members of Microelectronics & VLSI Department, who have provided me with the valuable conceptual knowledge during my course work. I would like to thank VLSI lab staff, PHD researchers and all my friends to provide with the support to carry on with my research work.

Abstract

Due to rapid development in semiconductor industry, high package density in Integrated Circuits is required. Scaling trend in CMOS technology dropped down to submicron levels. Also due to small node capacitances, fewer amount of charge required for switching logical states, means submicron devices are more prone to Single Event Effects (SEEs) due to radiations. This report contain analysis of radiation induced SEEs in CMOS circuits, different radiation hardening design techniques, proposed new radiation hardened design

Spice simulation environment created using Double exponential current pulse as glitch induced due to radiations. Critical nodes are found out by applying radiation pulse on the CMOS circuits. Effects of radiations are studied on the critical nodes, by varying peak current values, fall time using Monte Carlo simulations.

Analysis of Radiation of Heavy Ion, Single Event Effect on 3D TCAD LATCH, to find out the charge generated at different points along the length and angular radiation on the drain terminal of the off device.

Keywords: SEEs, SER, SEU, Double exponential current, Critical charge.

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Acronyms & Definitions

Critical Charge: Minimum amount of charge required to flip the logical state of sensitive node due to radiation particle strike.

Failure in time: FIT, measures as one failure in 1 billion of device hours.

Funneling: Charge generated on the track due to particle strike will distorts local electrical field, such that charge is pulled up the track towards the surface. This effect in known as funneling

Hard Error: It's a destructive phenomenon of permanent device or circuit failure, along with the loss of data.

Linear Energy Transfer: LET, Amount of energy deposited per unit path length in silicon is defined as LET.

Single Event Transient: SET, It is a voltage glitch in the circuit due to particle strike.

Single Event Upset: SEU, An event of change of logical state of digital circuits, ("0" to "1", or vice versa).

Soft Error: It is an error in the logical state of digital circuit, which can be restored.

Soft Error Rate: SER, Rate of occurrence of soft errors in a circuit.

CHAPTER 1

INTRODUCTION

1.1 Overview of thesis

In this work, we have discussed impact of radiation beam Single event effect on the CMOS circuits. Introduction to the basic single event effect, mechanism of charge generation and flow, different sources for the radiation beam in the devices. In next section we have discussed already existing radiation hardened techniques to reduce failure rate. In next section we have calibrated NMOS and PMOS devices using TCAD tool on 180nm technology with the fabricated data provided by ST Microelectronics. We have developed a 3D TCAD device to study the impact of radiation on the CMOS devices. On the 3D TCAD device heavy ion radiation model is implemented.

With the 3D TCAD device by implementing different energy radiation, Threshold Linear energy transfer (LET) is find out for both NMOS and PMOS device. From the data collected for different energy simulations, we have proposed a new Monte Carlo simulation algorithm environment to compare different circuit design for radiation beam. In next section we have proposed a simulation algorithm to find out the most sensitive node to radiation for the radiation strike. We have also proposed a new more robust radiation hardened design logic circuit.

For the 3D Latch developed using TCAD tool, we have studied the impact of radiation fall at different location along the length of the device in the channel and drain region of the OFF NMOS and PMOS device. In next section we have studied the impact of angular radiation strike for both NMOS and PMOS OFF devices.

1.2 Basic of CMOS radiations

Energetic particles due to radiation striking a circuit may cause damage due to many effects like Displacement Damage, Total ionizing dose (TID) and Single Event Effects (SEEs). **Displacement damage** is the process of creating vacancy by high energy radiation particle, in

which radiation atom will collide with the silicon atom and displaces the silicon atom in the interstitial space.

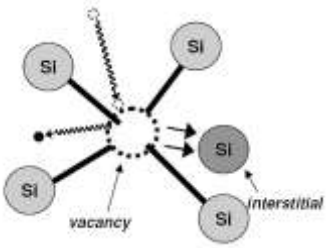

Figure 1, Displacement Damage effect, Ref [3]

Impact on majority carrier devices like MOSFET is almost negligible due to displacement damage. **Total Ionizing Dose** is another effect of radiation strike; it will lead to generation of electron hole pairs, due to heavy electric field electrons with their high saturation velocity will escape through gate oxide and will transport to the positive gate electrode.

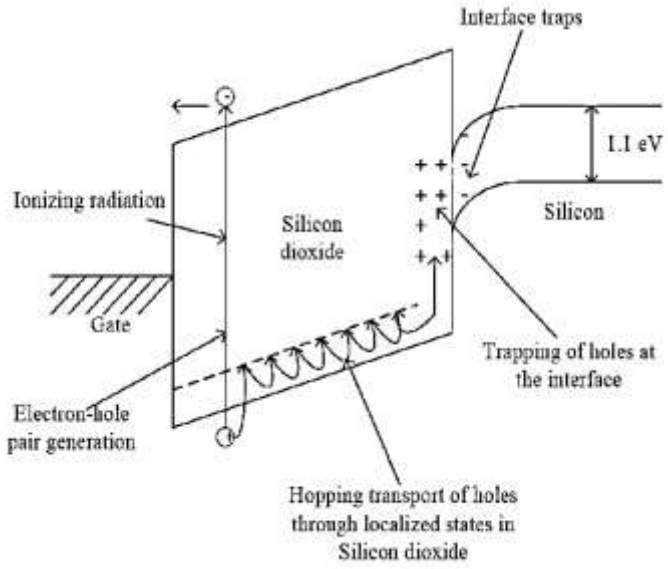

Figure 2, Total Ionizing Dose charge flow, Ref [3]

Holes which are not recombined will try to move towards si-sio2 interface. Some of the holes will escape/ tunnel out lead to current in silicon substrate, while some will be trapped in sio2. These trapped holes will lead to threshold voltage variation for the MOSFET. This work focused on Single Event Effects due to ration strike.

1.3 Single Event Effect basics

SEEs are the glitches due to radiation ion strikes at a circuit node, which will lead to Single Event Upsets and Single Event Transient in the CMOS circuits. Main causes of SEEs are different type of energetic particles striking the sensitive regions. Such radiation particles are alpha particles, heavy ions, cosmic rays, protons, neutrons etc.

Scaling trends in CMOS technology will lead to submicron technology, which is more prone to radiation. Due to smaller node capacitances in submicron devices, less amount of charge required for switching logical state. High package density means smaller separations in circuit nodes, which will enhance probability of more nodes of circuit affected for a single radiation event strike.

This sharing of charge between nearby nodes will impact circuit level radiation hardening techniques like stack separation etc., which work on the principle that an ion strike will affect a single node.

1.4 Impact induced with CMOS Scaling

- At submicron level reduction in gate oxide thickness and nodal capacitance, it will be easier to cause an upset at the output.
- With Reduced gate length there will be enhancement in the parasitic bipolar effect.
- And decrease in the nodal separation and desire for higher packing density will lead to increase in the probability of charge sharing between nearby nodes during an ion-strike.

1.5 Sources of Radiation

Three primary sources for the induction of soft errors in semiconductor devices:

1. Alpha particles
2. Neutrons
3. High energy Cosmic rays

1.5.1 Alpha Particles

It is a double-ionized helium atom ($^4He^{2+}$), composed of two protons and two neutrons.

Source of alpha particles in semiconductor devices:

- Wafer
- Packaging material, (Dominant source Th-232 and U-238 isotopes)
- Solder bumps, (Decay of Po-210 and Pb-210 impurities)

Interaction of alpha particles with silicon will generate electron-hole pairs; average 3.6eV of K.E. of alpha particles is lost for generation of each pair of EH. So an alpha can generate approximately a million EHP. As moving particle loses its KE, so it will increase time available to generate more EHP. So as particles traverse through device generation rate will keep on increasing, and maximum at the end of trajectory. 1MeVof alpha particles generate approximately 42fC of charge.

Fully processed wafers have an emission rate of 0.0003 alpha particles/cm2-hr. Natural alpha emission rates of process and package materials:

Material	Emission rate [$\alpha/(cm^2\ hr)$]
Cu metal	0.0019
Al metal	0.0014
Fully processed wafer	< 0.001
Mold compound	0.024 – < 0.002
Flip-chip underfill	0.002 – 0.0009
Pb-based solders	7.200 – < 0.002
Package	0.01 – 0.001

Table 1, Source of alpha particles & their emission rate, Ref [8]

1.5.2 Neutron induced Boron fission

Boron ^{10}B isotope is highly unstable towards neutrons. When ^{10}B isotope strike with the neutron fission takes places and it will split in two parts ^7Li and alpha particles. Energy possessed by the lithium nucleus is 0,840 MeV, while alpha particles with energy 1.47 MeV. These particles will generate EHP which will lead to soft errors.

Probability for the fission will reduce as the energy of neutron is high. As compare to alpha particles, lithium nucleus will generate more charges, means soft error probability is more with lithium. Charge generation rate for lithium is 25fC/um.

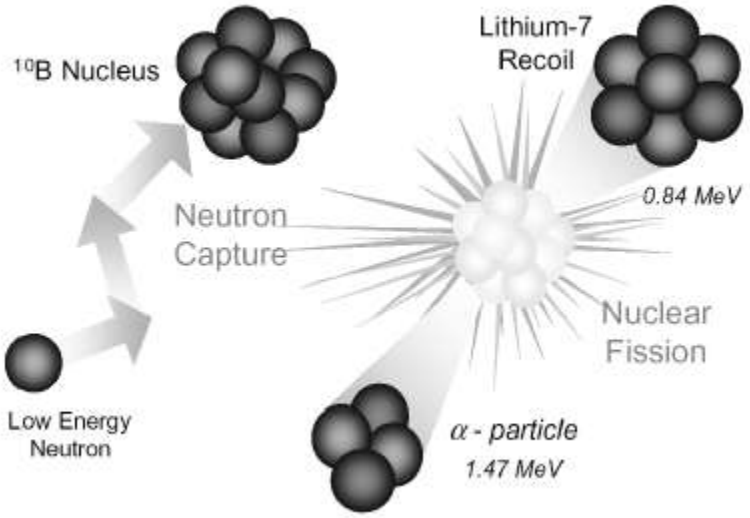

Figure 3, Neutron induced boron fission, Ref [8]

1.5.3 High energy Cosmic rays

Cosmic particles include alpha particles, heavier nuclei & protons. Cosmic rays with strong nuclear interactions reacts earth's atmosphere produces neutrons. Neutrons with energy higher than 4.5 MeV will lead to soft errors in devices.

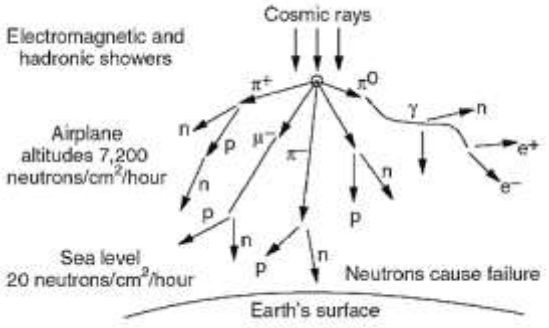

Figure 4, Neutrons generation from cosmic rays, Ref [8]

Neutrons do not generate charges directly, by colliding with silicon nucleus it will eject nucleus out of lattice and nucleus will reach higher energy state. Resulting silicon will emit gamma particles and generate charges. Neutron may also absorb during collision and then will breaks into secondary particles. Secondary particles generated will create charges, and will follow arbitrary track in the device, i.e. as compare to other particles neutron will have more sensitive regions in the device.

1.6 Mechanism of Single Event Effects

Radiation particle striking a device causes charge generation. Magnitude of charge generated depends on the linear energy transferred to the device and LET depends on the energy of the ion and mass of the particle and the material in which it is travelling. For silicon 3.6 eV of energy is required to generate 1 electron hole pair. Soft errors in the device occur due to collection and transport of this generated charge. Reversed biased junctions are most sensitive region for this charge collection and generation, which lead to soft errors. Generally charge collection takes place very few microns from the reverse biased junction. Charge collected generally from few fC to hundreds of fC.

1.6.1 Generation of Charge

Charge generation with radiation strike on device can be take place in following two ways:

1. Direct Ionization
2. Indirect Ionization

Direct Ionization: In this process energetic particle strike with the semiconductor and generate EHP in the track. Energetic particles in this case refer to heavy ions.

Indirect Ionization: Energetic particle struck the device and generate secondary particle, followed by ionization by secondary particle. Lighter particles like protons, neutrons etc. are considered as energetic particles in this case.

As the particle travel through device energy loss along the length (energy loss per unit length in Mev/cm) is measured as LET. When normalized with the density of target material LET

measured in Mev.cm^2 /mg. LET for silicon is 3.6eV to generate EHP (97 Mev.cm^2 /mg energy required to generate 1pC/um of charge in silicon).

As the ion strike the device it will form a track into the device with some beam radius in micron units, shown in Fig. 5 (a). A very high concentration of charge is generated around the ion beam track. Due to presence of high electric field near to depletion region these charges are collected in the form of funnel of charge, lead to high field depletion region deeper into the substrate region as shown in Fig. 5 (b). this formation of funnel due to electric field of depletion region will create a large drift current transient at that node. This process of drift of carries takes place in very small time duration few Pico seconds. This funnel formation inside the substrate depends on the doping concentration of the substrate.

1.6.2 Collection of Charge

Collection of charge can be accomplished with following three ways:

1. Diffusion
2. Drift
3. Recombination

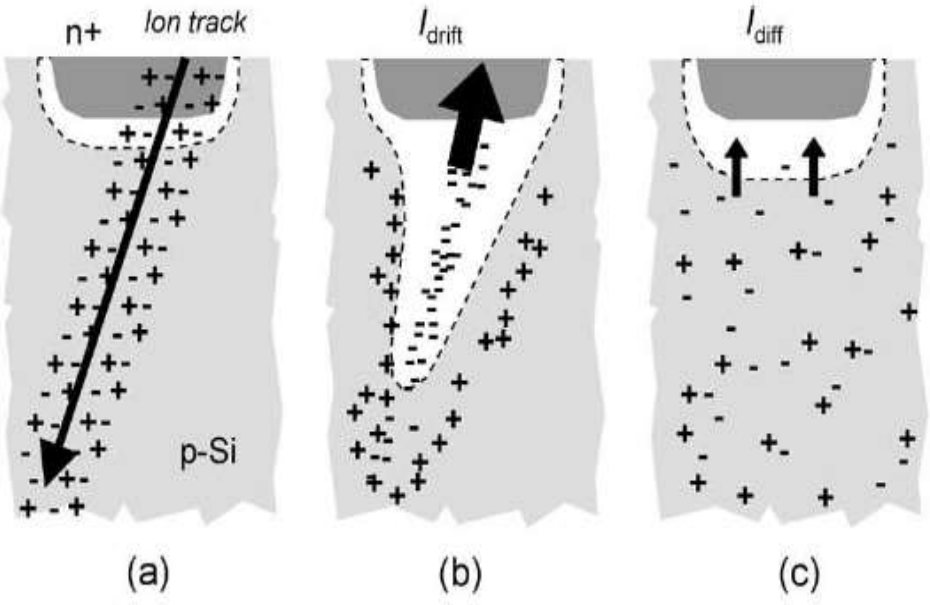

Figure 5, Mechanism of charge generation and flow Ref [7]

Drift of carriers take place in the depletion region due to presence of high electric field at the reverse biased junction. That's why most sensitive region for the ion-strike is reverse-biased junction. Transient current is observed at the junction due to this drift process for very small time duration. Two opposite charge carriers can disappear after recombination with each other.

Diffusion of carrier can take place due to gradient in concentration formed as EHPs are generated. Value of the collection of charge due to diffusion depends on the diffusion length. As compare to drift charge collection process, diffusion collection process is much slower; means will take place in longer time interval. Figure above will show drift, diffusion, recombination, and field funneling collection processes. Further charge collection takes place as the electrons diffuses into the depletion region.

1.6.3 Radiation-Induced current

Due to charge generation & collection process, current will start flowing through the device. As the drift charge collection process is much faster and maximum charge collection takes place through this process. Nature of the current pulse will be like as shown in Fig. 7, initial fast spike of current due to drift collection, followed by a slower decay due to diffusion collection.

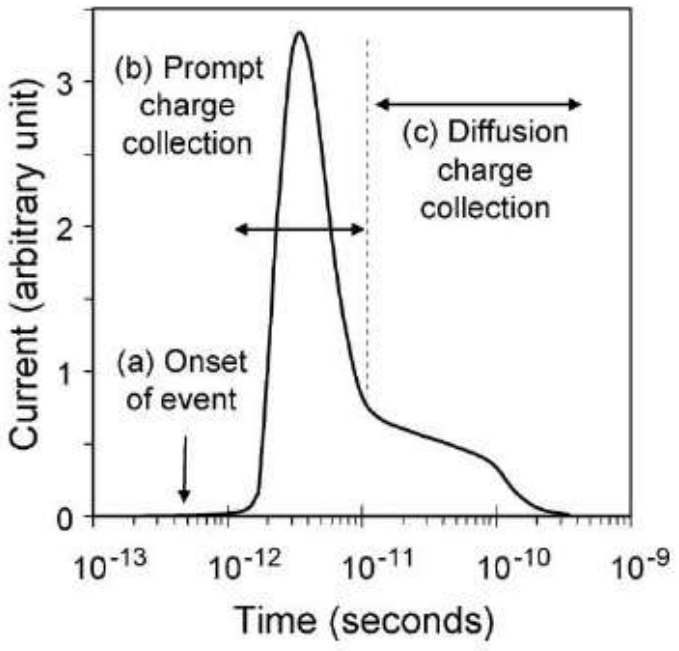

Figure 6, Radiation induced double exponential current, Ref [7]

This current pulse can be modeled as double exponential current pulse, with some peak current (I_o), rise time (t_r) and fall time (t_f),

$$I(t) = I_o\left(e^{-t/t_f} - e^{-t/t_r}\right)$$

Critical charge for the node under test can be calculated by integrating the current pulse for the pulse period.

$$Q_{crit} = \int_0^{T_{period}} I(t)\, dt$$

1.7 Radiation Induced Errors

Errors due to radiations may be permanent (Hard Errors) or temporary (Soft Errors).

1.7.1 Permanent Errors

Single Event Burnout (SEB) – Generated current will turn on parasitic bipolar device, which in turn provide feedback path, which will finally lead to burnout. Such effects mainly take place in power bipolar or MOSFET transistors.

Single Event Gate Rupture (SEGR) – This effect occur mainly in insulating gate oxide, due to accumulation of charge particles in the gate oxide. This will effectively increase the electric field inside the dielectric, finally lead to dielectric failure.

Single Event Latch up: This effect mainly occurs in CMOS devices, due to presence of p-n junctions. Radiation causes the flow of current in the substrate region of device, which will create a voltage drop in vertical device. Voltage drop will switch on the lateral device, and a heavy current start to flow, initiating a positive feedback loop. Heavy current will damage the device permanently.

1.7.2 Temporary Errors

Single Event Transient and Single Event Upset are some common temporary errors due to ion strike in semiconductor devices. SETs are in the form of voltage glitches, while SEUs are the temporal flip of logical state in the device.

CHAPTER 2

2D TCAD DEVICE CALIBRATION

2.1 NMOS - PMOS device calibration using Sentaurus TCAD tool

In this work we have designed NMOS & PMOS device (2 Dimensional) on 180nm technology using Sentaurus TCAD, Structure Editor Tool. Using Sentaurus Device Tool, devices are calibrated with the fabricated data.

2.1.1 Dimensions and details for the NMOS device structures:

For both NMOS device doping of the P- well is Gaussian in nature with peak concentration just below the surface. Shallow trench isolation is 0.39 micron deep and N type Source-Drain implants are 0.13 micron deep. Lightly doped drain extensions are 0.06 micron deep.

Device	NMOS		
Dimensions	Length = 2	Depth =1.2	
Substrate	Boron	Const. Conc. = 1e15	
Channel	Indium	Analytical Peak Conc. = 1e17	
S/D	Arsenic	Analytical Peak Conc. = 1e20	Depth= 0.2
S/D LDD	Arsenic	Analytical Peak Conc. = 1e18	Depth= 0.05
Poly Gate	Arsenic	Const. Conc. = 1e20	Height = 0.2
Gate Oxide	Thickness = 0.004		
Spacer	SiO2	Thickness = 0.15	
STI	SiO2	Depth = 0.5	
Gate Length	0.18		

*All dimension values in micro meter units

Table 2, NMOS 2D device dimension details

2.1.2 Dimensions and details for the PMOS device structures:

For both PMOS device doping of the N- well is Gaussian in nature with peak concentration just below the surface. Shallow trench isolation is 0.39 micron deep and P type Source-Drain implants are 0.13 micron deep. Lightly doped drain extensions are 0.06 micron deep.

Device	PMOS		
Dimensions	Length = 2	Depth =1.2	
Substrate	Phosphorus	Const. Conc. = 1e15	
Channel	Arsenic	Analytical Peak Conc. = 1e17	
S/D	Boron	Analytical Peak Conc. = 1e20	Depth= 0.2
S/D LDD	Boron	Analytical Peak Conc. = 1e18	Depth= 0.05
Poly Gate	Boron	Const. Conc. = 1e20	Height = 0.2
Gate Oxide	Thickness = 0.004		
Spacer	SiO2	Thickness = 0.15	
STI	SiO2	Depth = 0.5	
Gate Length	0.18		

*All dimension values in micro meter units

Table 3, PMOS 2D device dimension details

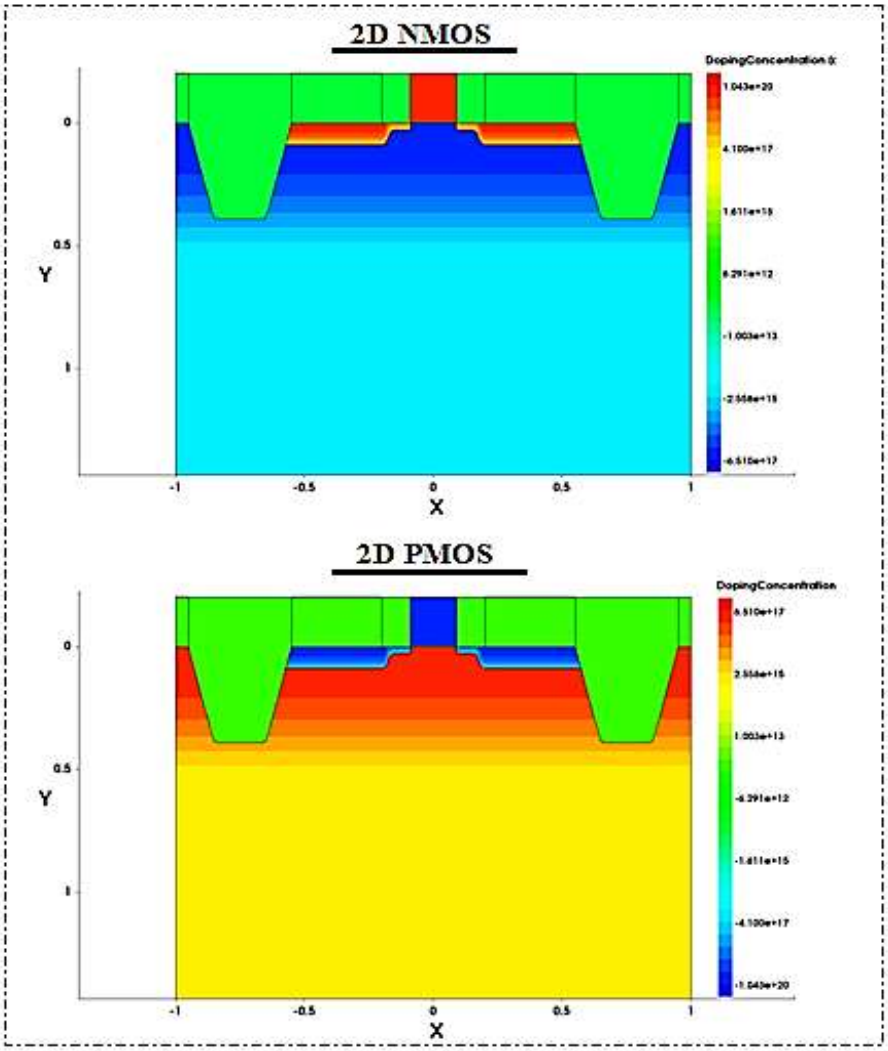

Figure 7, 2D NMOS PMOS devices Sentaurus Structure Editor Tool

2.2 I-V Characteristics for the TCAD device

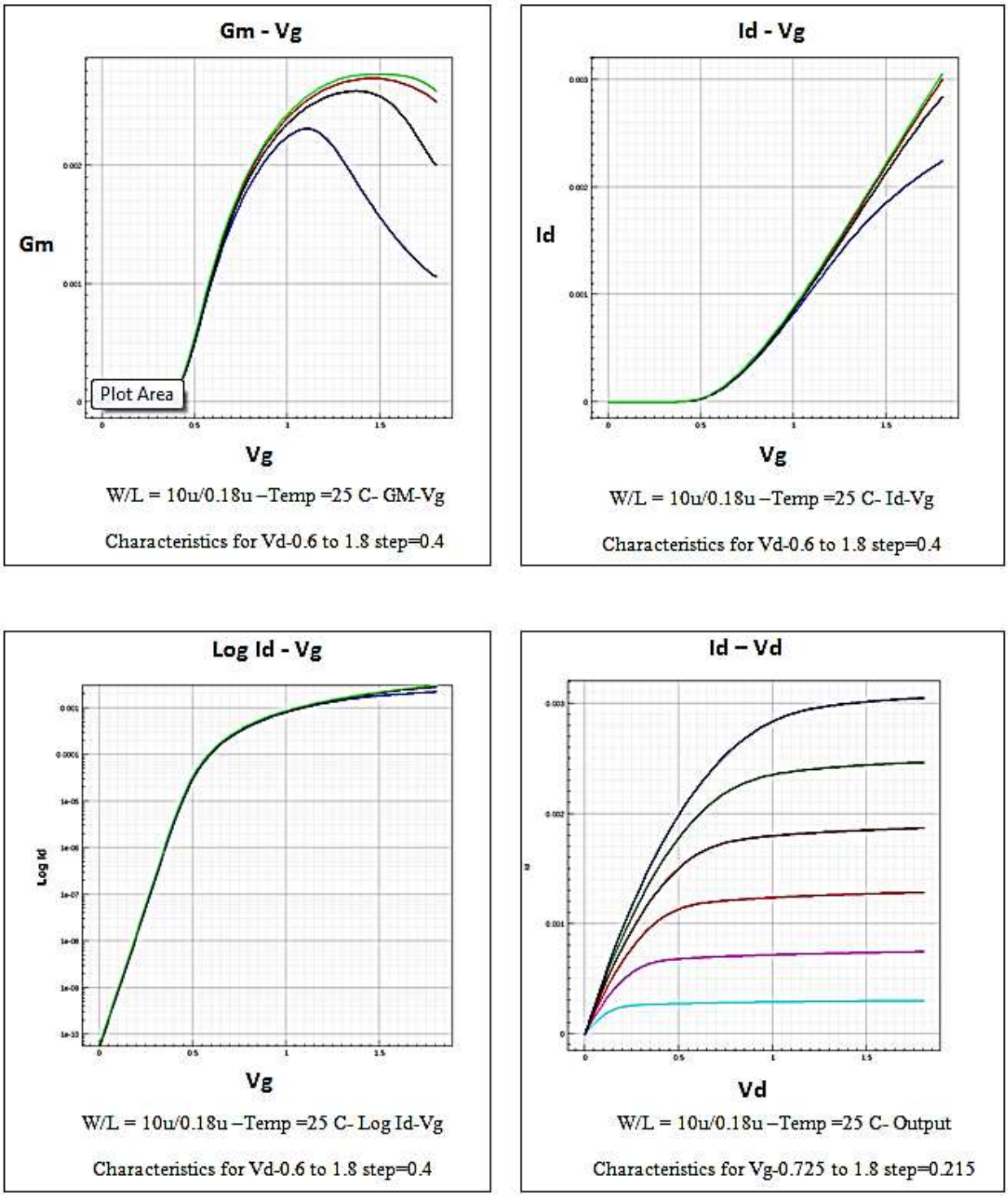

Figure 8, I-V Characteristics for the calibrated device

2.3 Device calibration Fabricated data and TCAD data

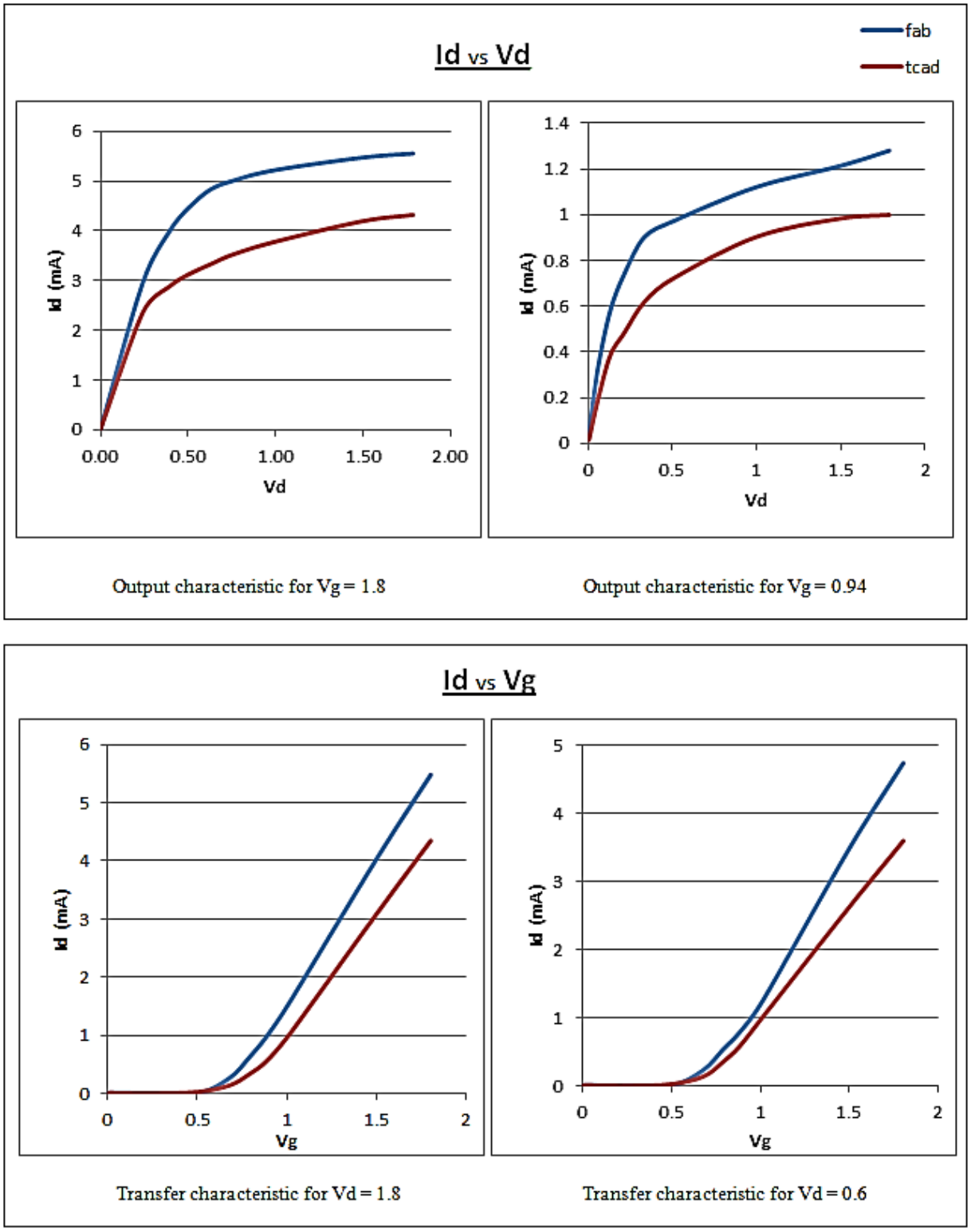

Figure 9, I-V Characteristics comparison fab and TCAD device

2.4 Comparison table Fabricate device data and TCAD device data:

	Fab_Data	**TCAD_Data**	
Parameters	NMOS	NMOS	PMOS
Dimensions	W/L = 10u/0.18u	W/L = 10u/0.18u	W/L = 10u/0.18u
Vth (Vds =Vdd)	*ST confidential	0.41	-0.378
ID sat (mA) (Vgs =Vds =Vdd)	*ST confidential	4.48	4.2
Ioff (pA) (Vds = Vdd)	*ST confidential	66.6	204

Table 4, Data comparison Fab and TCAD device

Finally, these calibrated NMOS and PMOS two dimensional structure with all the parameters set are transformed to three dimensional structures. These devise will be used to form 3D Latch structure discussed in next section.

CHAPTER 3

3D TCAD LATCH DEVICE

3.1 Introduction

In this work we have designed 3D LATCH on 180nm technology using Sentaurus TCAD, Structure Editor Tool. Using Sentaurus Device Tool, impact of radiations on the off device PMOS or NMOS is studied for different value of Radiation Energy.

3D Latch structure so formed utilizes triple well process flow, steps for the same as mentioned below:

- A layer of silicon with defined dimensions is taken as substrate, which utilizes constant P type doping profile.
- In this first substrate layer, analytical profile of N type is done up to a defined depth, this N type layer is called Epitaxial layer
- In the epitaxial layer two wells, N type and P type with analytical doping profile with defined depth is generated. These wells have higher doping concentration then the epitaxial layer doping concentration.
- Gate-oxide layer is grown on Nwell and Pwell to grow NMOS and PMOS structure.
- Polysilicon gate are grown.
- PMOS and NMOS, source & drain are implanted in the respective Nwell and Pwell.
- Metal contacts are defined in such a way to form two inverters.
- Finally a layer of sio2 is grown on top for the isolation.
- These two back to back inverters are electrically connected during simulation to form the Latch.

3.2 Latch Specifications:

Dimensions			
Region	**Length**	**Width**	**Height/Depth**
Device	9.371	10.21	1.8
Epitaxial	7.371	8.21	Y
N-P Well	4.881	5.72	Y/2
S/D	-	-	Y/10
STI	-	0.4	0.3 * Y
Poly silicon	0.18	-	0.2
Gate oxide	-	-	0.0035
Channel Length	0.18	-	-
PMOS	-	Y	-
NMOS	-	Y/2	-
Separation between active regions	-	1.77	-

***All dimensions is micro meter units**

Table 5, Device dimensions for the 3D TCAD Latch

Concentrations				
Region	**Dopant**	**Concentration (/cm3)**	**Type**	**Depth**
Substrate	Boron	1e15	Constant	1.8
Epitaxial layer	Phosphorus	X	Analytical	Y
Nwell	Phosphorus	2X	Analytical	Y/2
P well	Boron	2X	Analytical	Y/2
S/D NMOS	Arsenic	1e20	Analytical	Y/10
S/D PMOS	Boron	1e20	Analytical	Y/10
Poly NMOS	Arsenic	1e20	Constant	0.2
Poly PMOS	Boron	1e20	Constant	0.2

***All dimensions is micro meter units**

Table 6, Device concentration for different regions 3D TCAD Latch

3.3 Different views for the 3D device

3.3.1 2D cut along the width of the device

Figure 10, below shows the 2D cut along the device width, it specifies the Nwell for the PMOS devices, Pwell for NMOS devices; N type doped epitaxial layer and P type substrate.

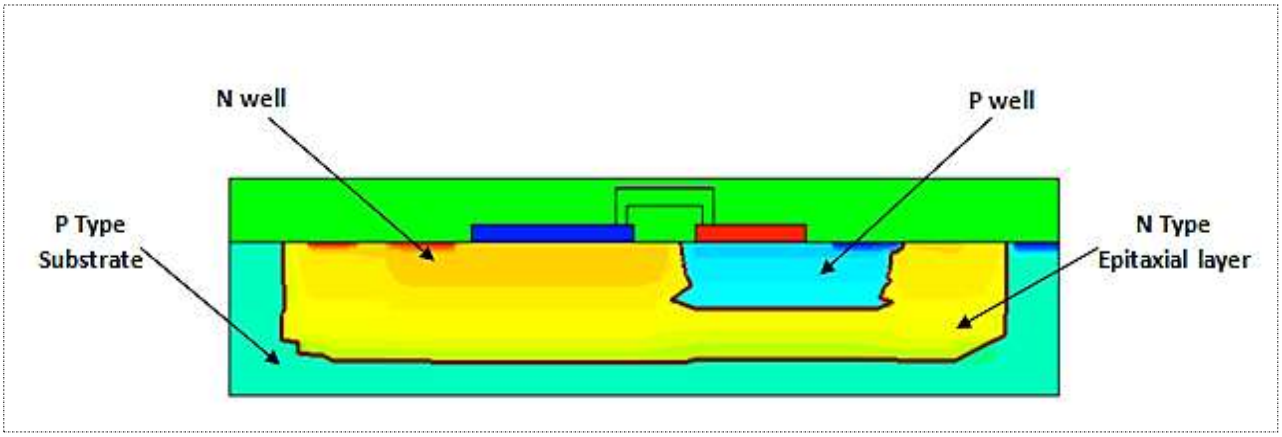

Figure 10, 2D cut along the width of the device

3.3.2 2D cut along the Length of the device, NMOS – PMOS

Figure 11, below shows the 2D cuts along the length of the 3D Latch, these specify the NMOSs in Pwell region and PMOSs in Nwell region. Metal contact connections for latch formation are not specified in this picture.

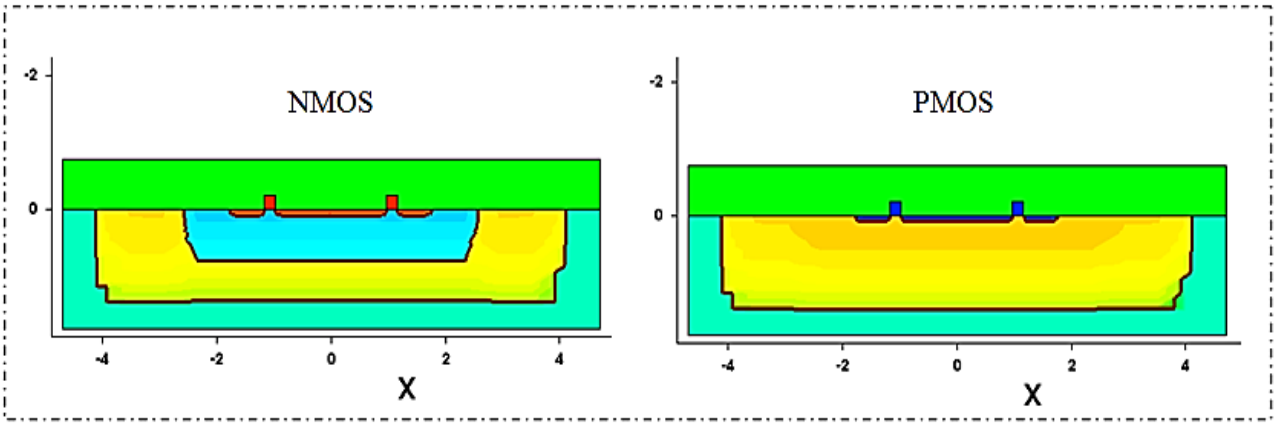

Figure 11, 2D cut along the Length of the device, NMOS – PMOS

3.3.3 Top View of 3D Latch

Figure 12, below shows the top view of the 3D latch formed using TCAD Tool, this clearly specify the different wells and their doping concentrations. It also specifies active regions for NMOS and PMOS devices and the high doped regions for metal contact and all the metal contacts to form latch device.

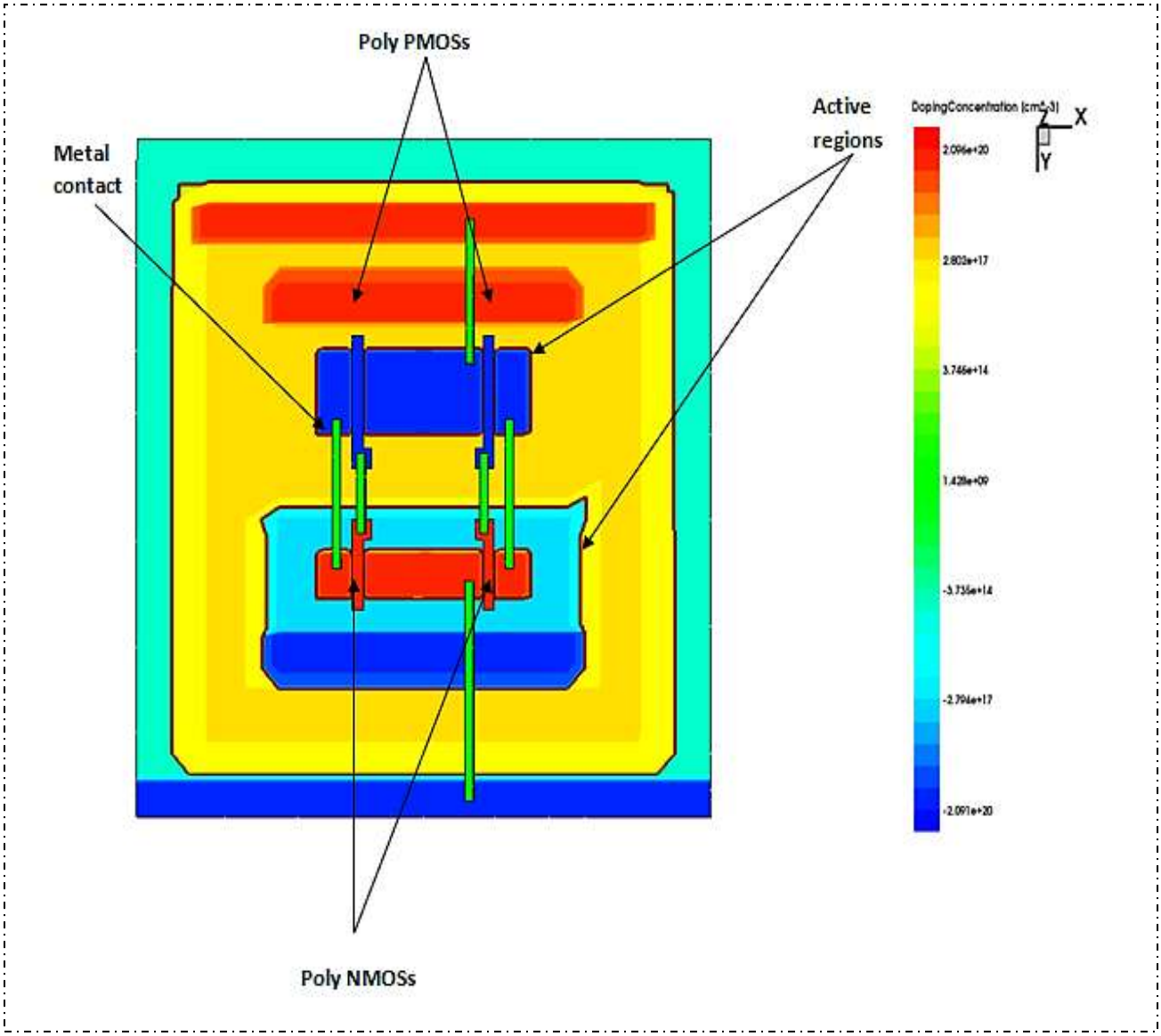

Figure 12, Top view of 3D Latch device

3.3.4 Side View of 3D latch and device meshing

Figure 13, below shows the side view of the 3D latch device so formed; it also specifies the meshing for different regions. As can be seen meshing is highly dense at the channel and junction region to have more number of points for the calculations, while for other regions it is not that much dense.

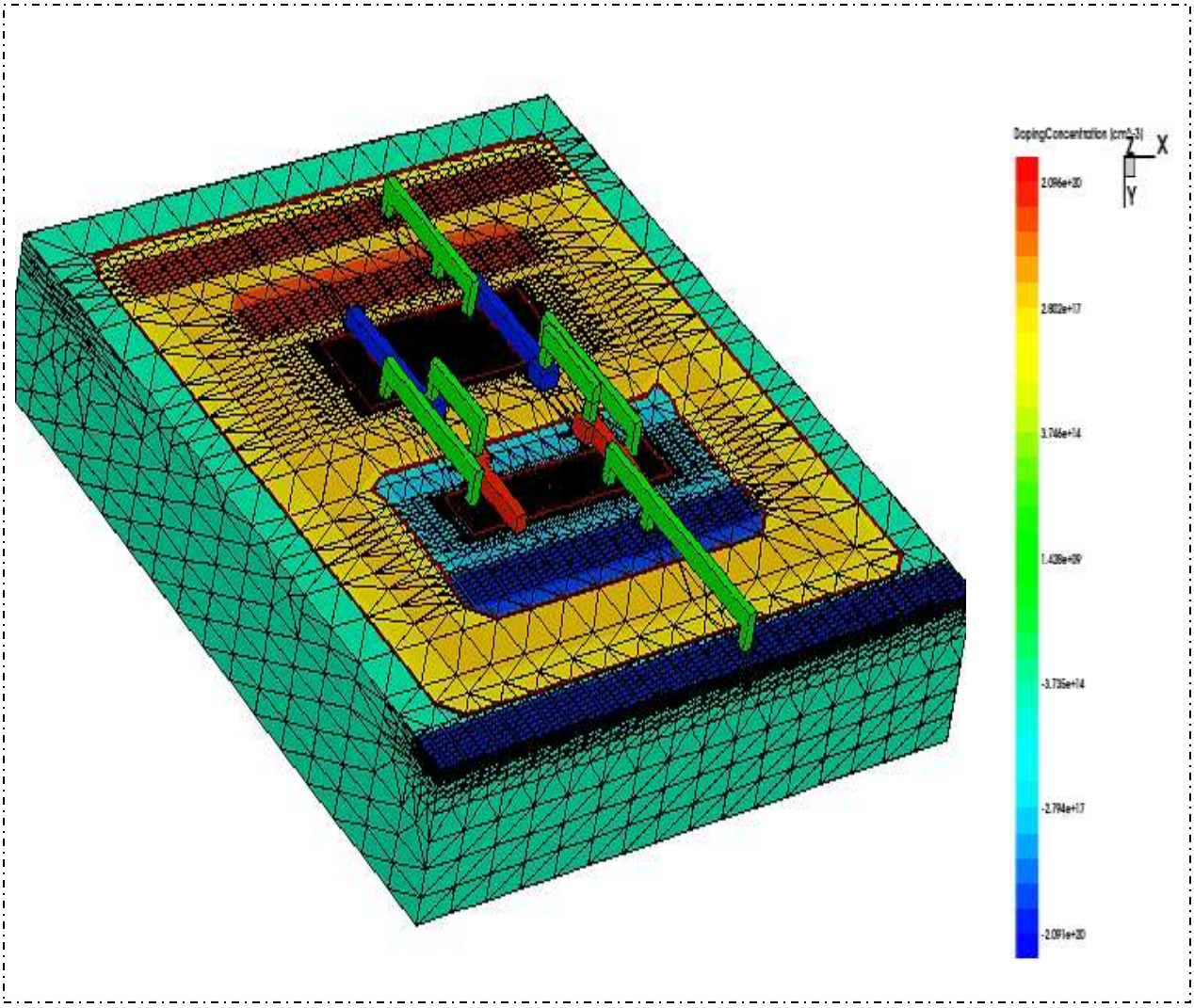

Figure 13, Side view of 3D Latch device and meshing at different regions

CHAPTER 4

HEAVY ION RADIATION ON 3D LATCH

4.1 Introduction

In this chapter we will discuss the impact of heavy ion radiation on the 3D Latch device formed using TCAD Sentaurus tool mentioned in last section. Heavy Ion environment is modeled using Sentaurus device tool in the physics section.

For the heavy ions parameters to be used in Sentaurus device tool are as follows:

a) **LET- Linear Energy transfer**

   It is the energy of the ions used to hit the device, and its value represents how much it can penetrate deep inside the surface. It can be either in electron volt unit or Pico coulomb per micro meter unit depends on whether Pico coulomb is selected in the physics sections.

b) **Location**

   It is the start point of the radiation beam on the device surface; Coordinates of the point on the surface.

c) **Direction**

   It is the direction of motion of ions of radiation beam; can be normal to the surface or can be varied to any angle depends on the coordinate mentioned.

d) **Beam radius**

   It is the lateral distribution of radiation beam perpendicular to length.

e) **Length**

   It is the length up to which radiation ions will penetrate.

f) **Spatial distribution**

   It represent the distribution of ions, can be Gaussian or exponential in nature.

g) **Time**

   As the Heavy ion radiation can be applied to the transient simulations, so it represents the time at which radiation ion beam fall on the device surface.

In this experiment, we had applied heavy ion radiation beam on the 3D Latch so formed. Circuit level diagram of the latch structure, nodes Q & Q bar are maintained at complementary initial conditions, one at level low and another at level high as shown in Fig. 14. So NMOS1 is the off device which is more prone to radiations is considered.

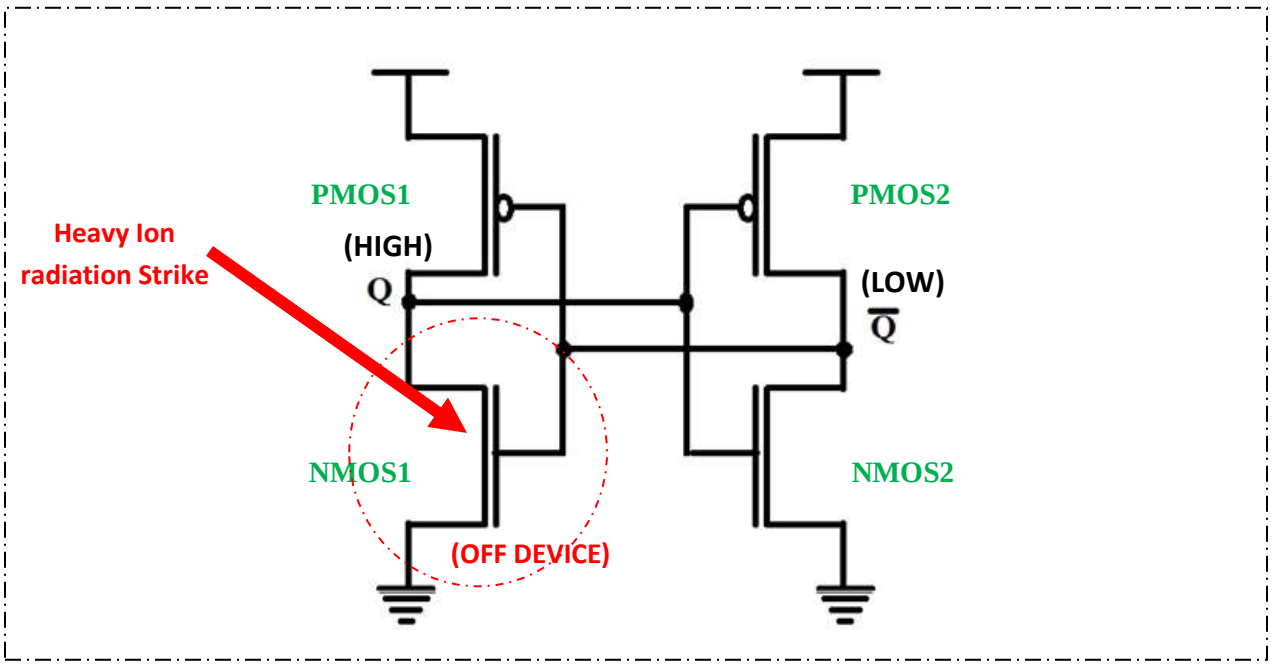

Figure 14, Circuit digram for the latch so formed (Cross coupled Invereters)

Heavy ion radiation is applied at the drain terminal of the NMOS1. Result of the transient simulation is shown in Fig. 15. As we can see, at the instant the radiation ion current beam strike the drain of OFF NMOS1 device, the data at both the nodes get flipped permanently. Even after the current pulse transient ends data at the nodes remain at the erroneous value, lead to soft error due to single particle strike at the sensitive node. Nature of the Heavy ion radiation beam current pulse is Double exponential current pulse with a very small rise time of few Pico second and a fall time of hundreds of Pico second. By integrating this radiation current pulse for the pulse width one can calculate the charge stored due to radiation strike at that particular sensitive node of the device.

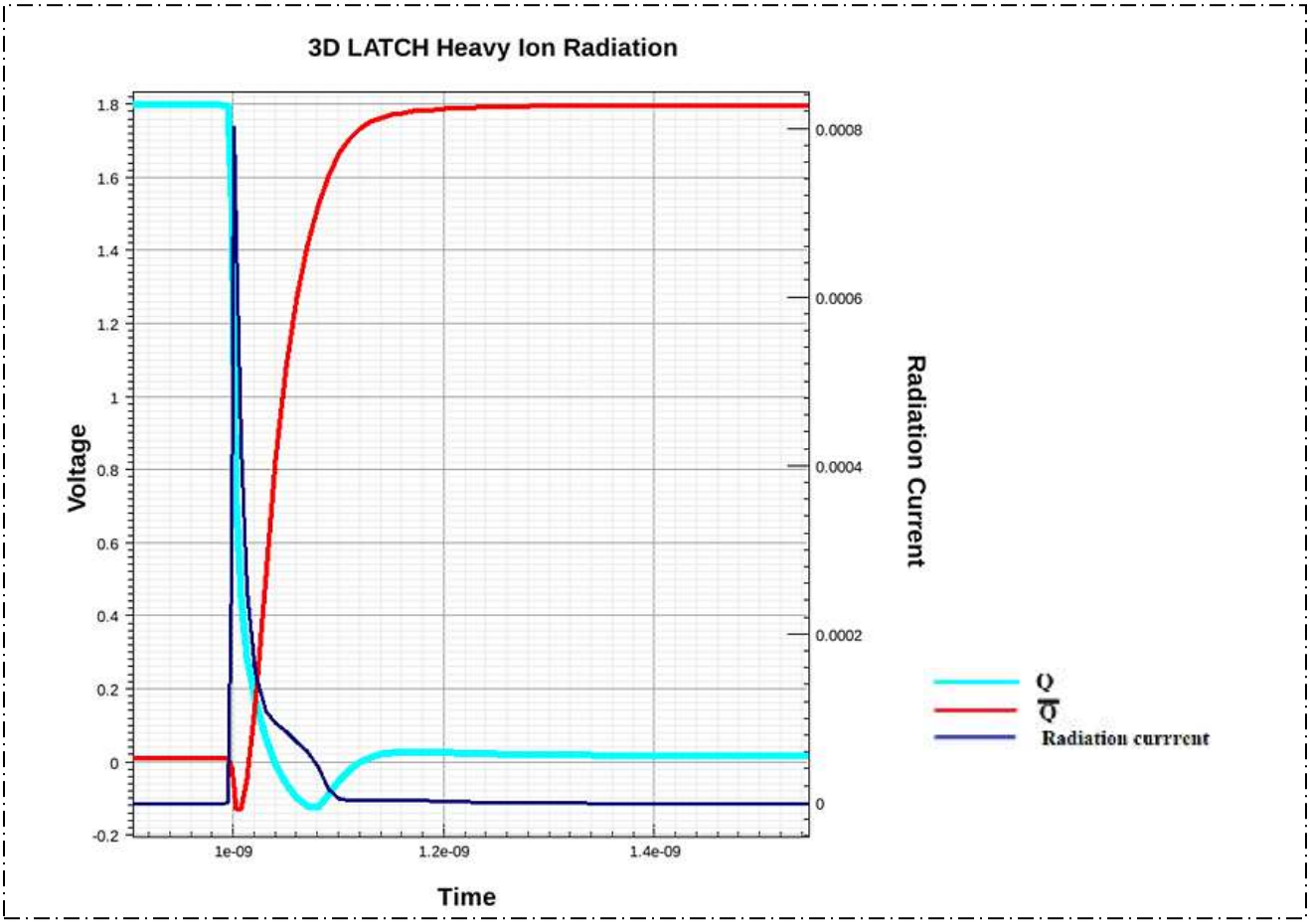

Figure 15, Impact of heavy ion radiation NMOS device

4.2 Sensitivity of Heavy Ion radiation at different location along the device length

In this chapter we have discussed the impact of heavy ion radiation along the device length at different location from channel to drain . On the 3D Latch formed, using sentaurus device tool varying the location parameter and keeping LET, direction, time and all other parameters constant Heavy ion radiation model is applied. For the Latch keeping one node at low voltage level and other at high voltage level, heavy ion radiation applied for the OFF NMOS device. And in the same way radiation puls eis applied to OFF PMOS device.

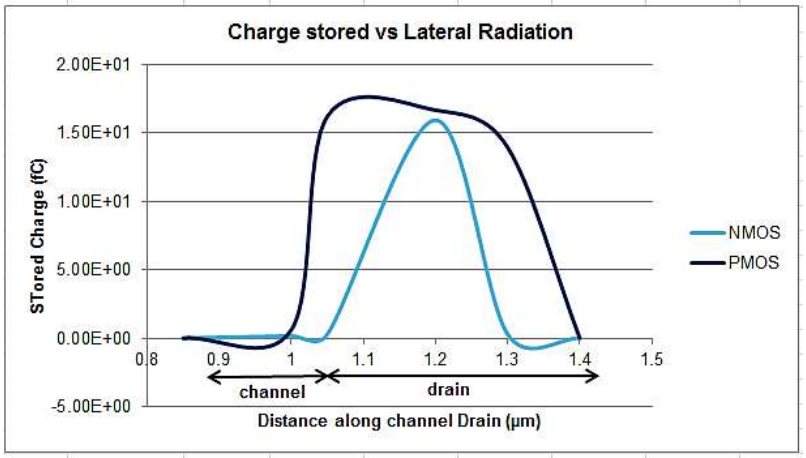

Figure 16, Charge stored for heavy ion at different location

Variation of heavy ion charge collected at different location for NMOS and PMOS as shown in Fig. 16. As can be seen that heavy ion charge accumulated for the off device is maximum at the drain channel junction region. And as we move away from the junction on either side charge accumulation keep on decreasing and became almost zero if the radiation fall away from the junction.

4.3 Sensitivity of OFF device to angular radiation strike

In this experiment we will discuss the impact of Heavy ion radiation at different angle for the OFF device . Heavy Ion radiation beam is applied at the off device drain region at different angles, heavy ion charge density for different angles as shown in Fig. 17. Charge collected for the ion strike is plotted vs angle of incidence as shown in Fig. 18.

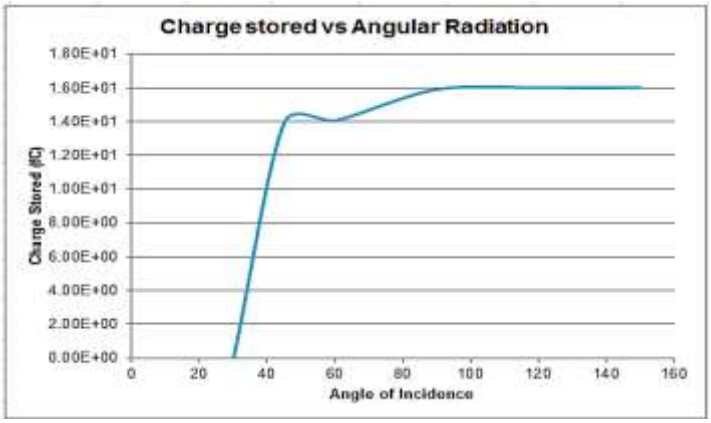

Figure 17, Charge stored for heavy ion at different angle

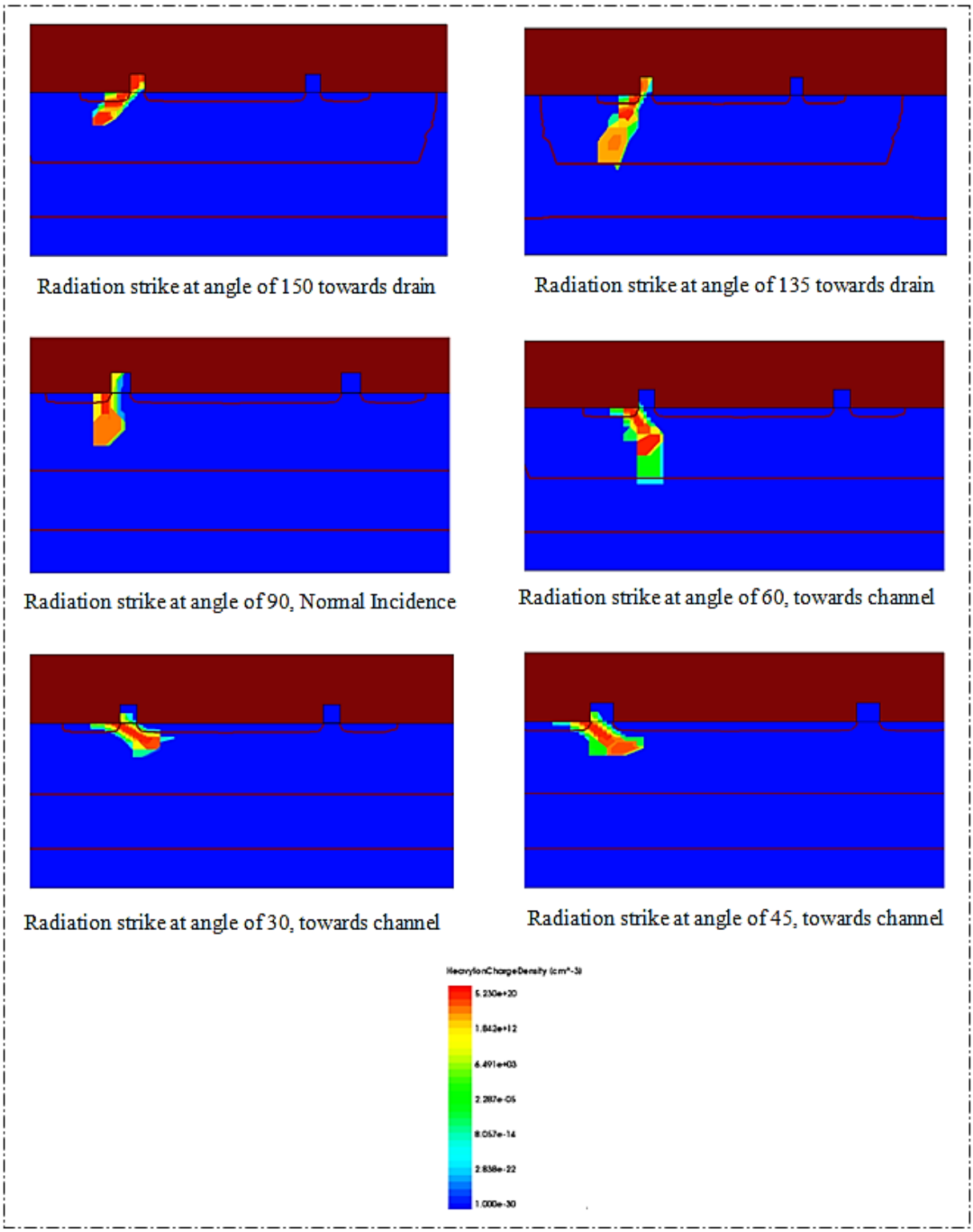

Figure 18, Heavy Ion charge density for the radiation strike at different angle

CHAPTER 5

FLIP FLOP RADIATION HARDENED TECHNIQUES

5.1 DICE - Dual Interlocked Cell

DICE, is a transistor level approach, shown in Fig. 19, which add redundant elements and feedback in conventional latch. Redundancy will help to recover the data lost at the node due to radiation strike. Feedback path will help to recover the data lost. M1 - M2 and M1N - M2N are the redundant complementary pairs. If either of the redundant pair nodes gets corrupted due to radiation pulse strike, it will be corrected by the feedback path provided by the redundant node.

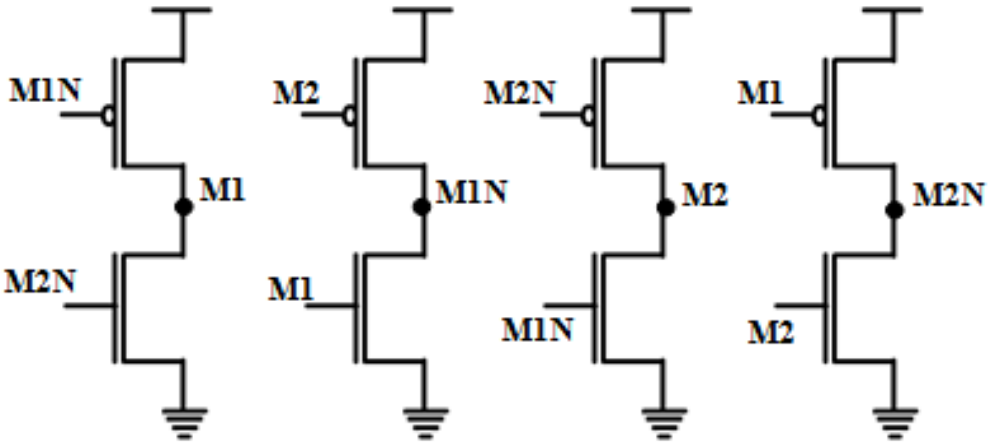

Figure 19, DICE design

With this technique error at the output of the logic is reduced to some extent, but introduced propagation delay of twice as with the conventional flip flop. This technique utilizes more number of transistors as compare to conventional flip flop. Power consumption is also worst with this technique around 3.5 times higher.

So the DICE radiation hardening design has issues of delay and high power dissipation, other design technique named Triple Modular Redundancy (TMR) is described in next section.

5.2 TMR - Triple Modular Redundancy

TMR latch as shown in Fig. 20, which utilizes three different systems to perform a process, whose result is processed by a majority-voting system to produce a single output. If any one of the three systems fails, the other two systems can correct and mask the fault. As it utilizes three redundant systems running parallel so impact due to a particle strike at any one node will be detected and corrected. It's a highly robust to radiation design. It works with the principle of error detection & correction up to some extent.

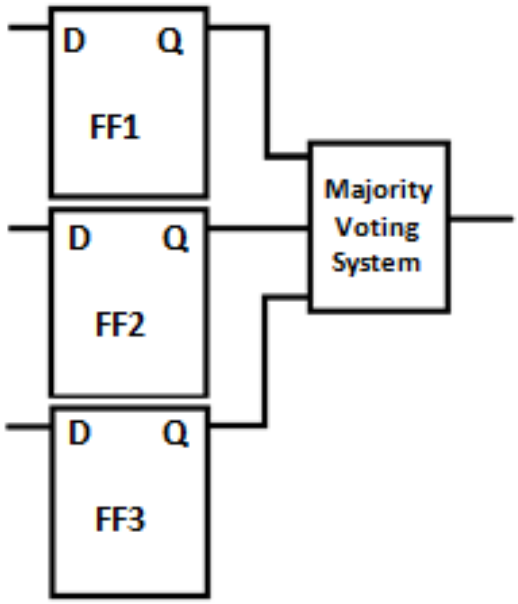

Figure 20, TMR Design

As three different systems running parallel, this design technique introduces more complexity of thrice the area requirement. More number of transistors as compare to conventional flip flop design.

So, the existing radiation hardened design DICE, TMR etc. has issues as mentioned above. To overcome the issues to some extent, a more robust to radiation and low power radiation hardened design technique is introduced in next section.

5.3 LPFFD Design

5.3.1 Principle of Operation

Basic architecture of the proposed design is as shown in Fig. 21. Proposed design utilizes following techniques:

- Redundancy for both master and slave blocks.
- Both the master and slave work on the single clock phase pulse.
- Transistor stacking for both master and slave stage blocks.
- Slave stage blocks cross coupled to master stage blocks output.

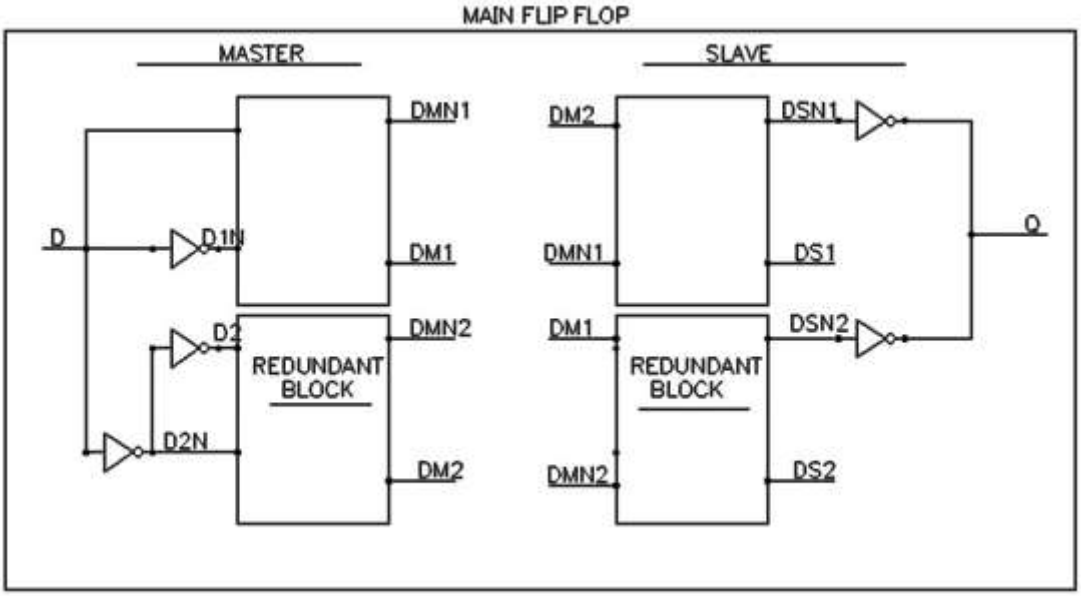

Figure 21, LPFFD design

In conventional flip flop design master and slave works on opposite phase clock pulse, while in case of LPFD design, master and slave stage blocks work with single phase clock pulse, which will reduce the chances of error due to glitches or any slew present at the clock input. This proposed design works with Inverted data input fed to both master and slave stage, so more robust to any erroneous input data.

With added redundant blocks to the master and slave stages, in case of radiation strike at any node of the master or slave block, data will be retrieved back through feedback path. Cross

coupling of the data at the input of slave stage will enhances the robustness of the design. As compare to previous techniques of radiation hardening (like DICE TMR etc.), in this design transistor stacking technique is used, which in turn reduces the leakage current of the transistor. Lead to reduce the power losses. Also due to transistor stacking equivalent resistance seen by a radiation particle is higher, so a larger amount of radiation current is required to flip the state as compare to previous techniques. So due to stacking of transistors, power losses will be less and robustness of the design increases.

Data and its inverted data are fed to master block and redundant block. These outputs of master stage are cross coupled to input of slave stage, which will provide more robustness for the error at any one of the input. Output of the slave stage is inverted to provide the final output of the Flop.

Master block along with the redundant block, D and inverted input driving the master block, at the positive phase clock, D input will be translated to output Q. If radiation strike any of the sensitive nodes (drain of the off NMOS or PMOS device) then state of the node will be affected, in that case redundant node will restore the state for the node under radiation impact.

CHAPTER 6

MODELING & SIMULATION

Radiation simulations for different radiation hardened designed is carried out with the Double exponential current pulse model as the radiation current pulse. This model is realized by applying a current source either as source/sink according to the logic state of the node.

6.1 Double exponential current pulse model

This model is realized as the exponential rise and exponential fall pulse, with rise time of few Pico seconds and fall time of hundreds of Pico seconds and with a peak current value in mAs.

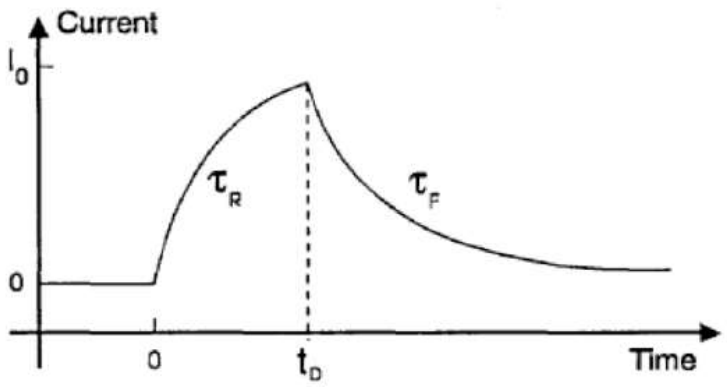

Figure 22, Double exponential current models Ref [2]

As the current source is applied to the node of the circuit to be considered, it will either accumulate charge or remove charge from the node. In this way logic state of the node will be flipped at the particular value of the peak current of the model.

6.2 Application of double exponential radiation model on basic D Flip Flop

To study the impact of radiation on different radiation hardened designs of D flip flop. Double exponential current pulse model is applied at one of the node of the master side of the flip flop. For the current pulse rise time and fall time are maintained at constant value and the peak current is varied. In this way threshold value of the peak current is find out for the conventional Master – Slave D flip flop design. For the same value of rise time, fall time and threshold peak current,

radiation simulations are carried out on different radiation hardened designed D flip flop. Result of the same as shown in Fig. 23. From the figure, we can see that as for the same radiation current pulse applied, error for the DICE structure is only delayed as compare to conventional design, while LPFD design retrieve back its value. So from the result of the radiation current model applied we can conclude that LPFD design is more robust to radiation as compare to previous design techniques.

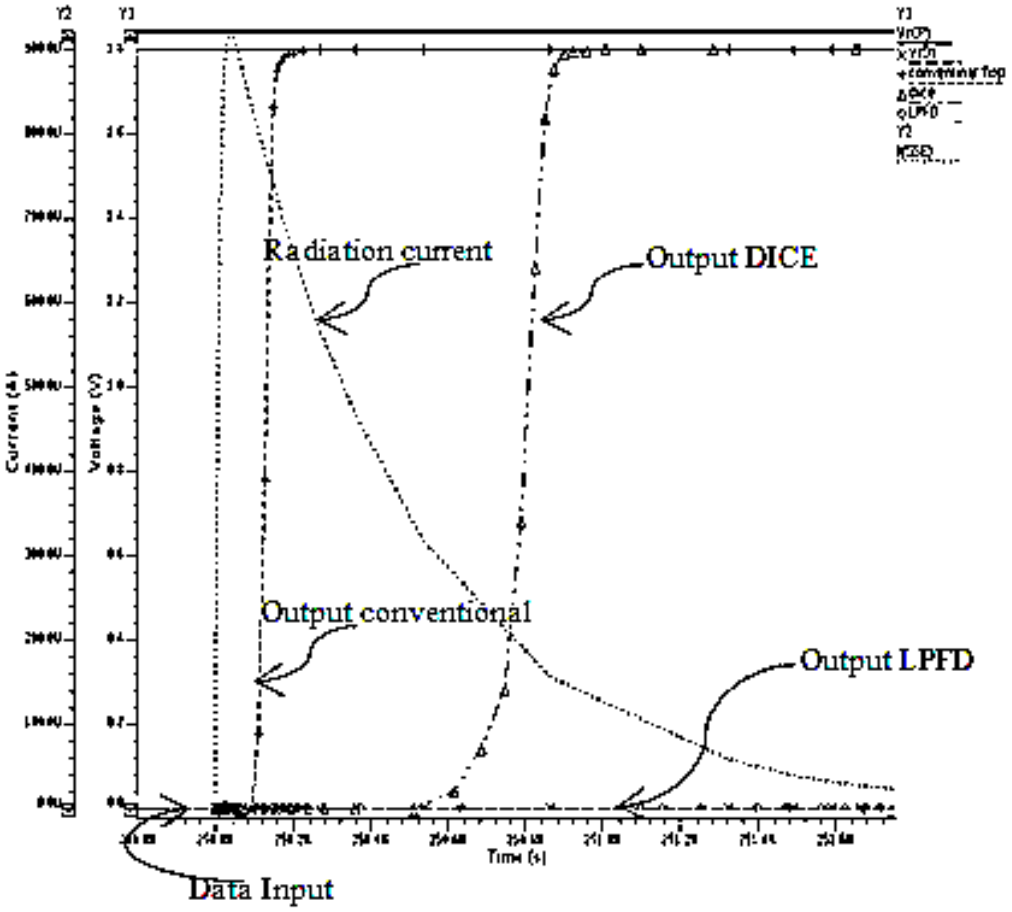

Figure 23, Impact of radiation on D flip flop (different RADHARD designs)

6.3 Monte Carlo Iteration technique to compare different RADHARD designs

In this section a comparison analysis of different radiation hardened design is carried out using Monte Carlo Iterative technique. Radiation current model used is same double exponential model, considering peak current as the only variable and keeping all other parameters at a constant value. Peak current of the model is varied with the user defined distribution functions as

shown in Fig. 24. To make the simulation environment more realistic, the variation of peak current is done using user defined probability distribution functions. Using these PDFs peak current is varied in such a way so that in 90% of the iterations, peak current will have its value closer to 0 (i.e. below threshold value of current), and for the remaining 10% ,its value will be closer to 1.

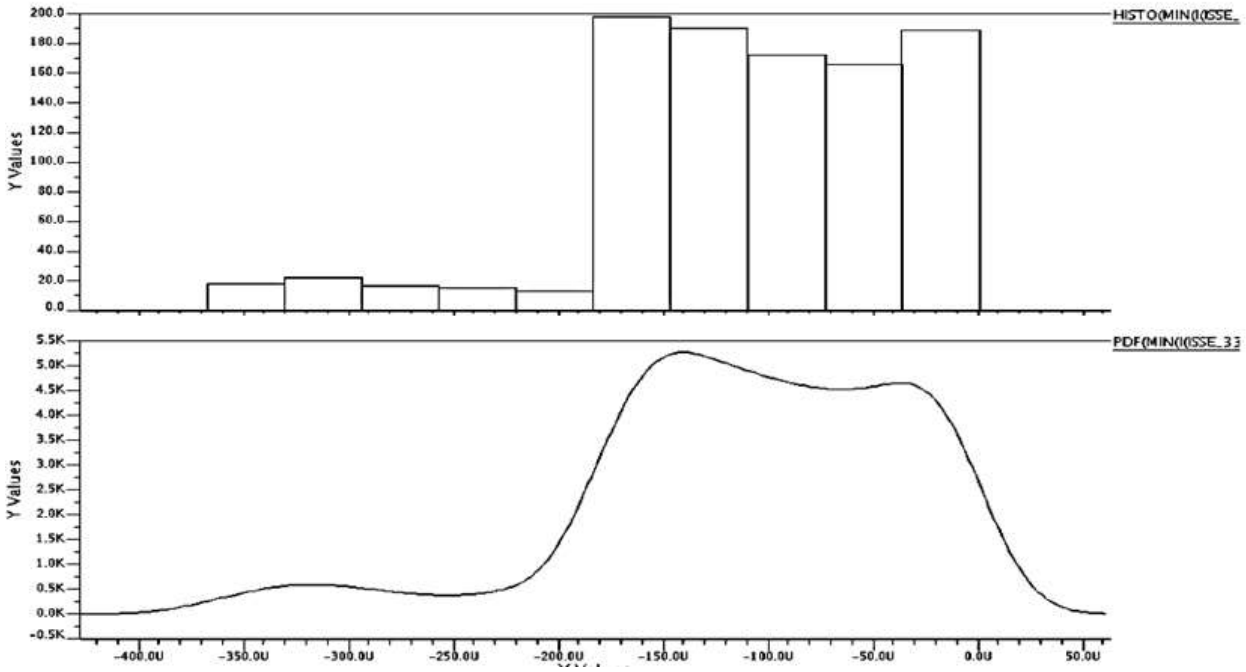

Figure 24, User define probability distribution function for current

Iterative simulation techniques were carried out on different RADHARD designs, by following the variation of peak current as shown in distribution function. Results of the Monte Carlo simulations carried on different designs as shown in table 7, below.

Flip Flop	Total Iterations	Output Flipped	Output not affected
Conventional	1001	845	156
DICE	1001	699	302
LPFFD	1001	70	931
TMR	1001	0	1001

Table 7, Result comparison for different RADHARD flip flop designs

From the results of the Monte Carlo iterative techniques, we can see that TMR is most robust design with 100% error free, but area and power requirements for this design are very high. As compare to high percentage error of 70% and 84% for DICE and conventional designs respectively, proposed LPFFD design is more close to the results of TMR for the radiation strike, with only 7% chances of failure.

6.4 Simulation Algorithm to find out the most sensitive node to radiation for a logic circuit

In this section we have proposed a new simulation algorithm to find out the most sensitive node to radiation for a given logic circuit. Sensitivity for the radiation beam is correlated to the charge accumulated for the radiation beam strike at different nodes.

Simulation algorithm flow as follows:

- For the given circuit, a script is generated to find out the operation mode of all the transistors present in the circuit netlist.
- From the output of the first simulation list of all the devices operating in off state is extracted.
- Again a script is generated to apply the double exponential radiation current model with some initial peak current value, fall time & rise time, at the drain node of the extracted off device.
- Output of the second simulation is compared with the applied data input, if the difference in two values is lower than the threshold value then value of the peak current is increased by a constant factor already defined.
- Loops of iterations carried out at drain of MOS devices till the difference exceeds the threshold already defined.
- Integration of the value of the peak current at which output is flipped from the desired value, taken for the pulse width.
- This is the desired critical charge at that particular node to flip the overall output of the circuit.
- Critical charge can be calculated by integration of the current for the pulse period.

So finally the value of the peak current for which the difference exceeds the threshold already defined, integration of the applied radiation current pulse for the pulse width will give the critical charge of that particular node. Simulation algorithm flow will be carried out as shown in Fig. 25.

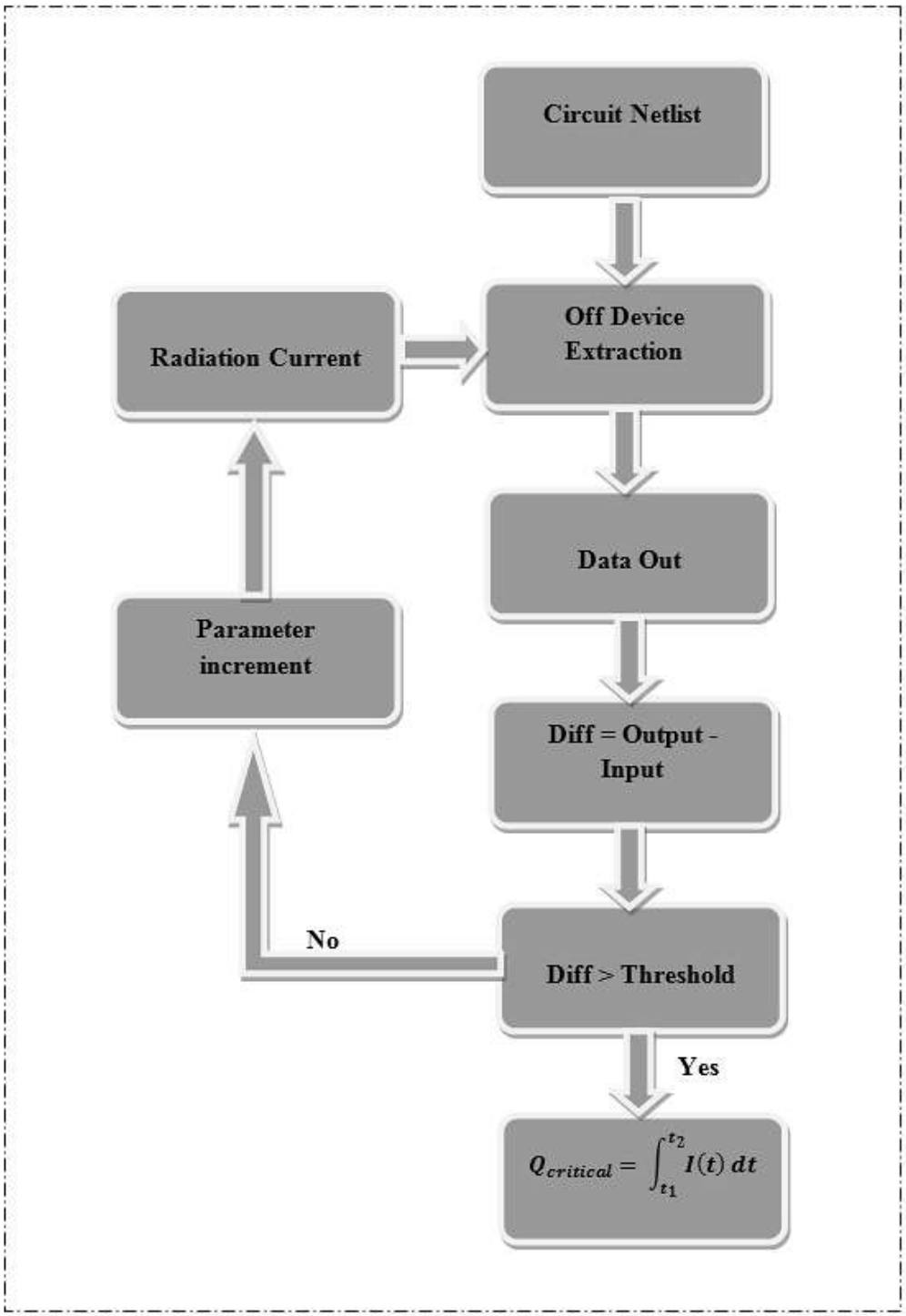

Figure 25, Simulation flow to find out most sensitive nodes

CONCLUSION

We studied impact of radiation on 110nm technology node. We calibrated 2D devices using TCAD tool and matched them with the ST microelectronics fabricated data up to some extent. We calibrated 3D Latch and studied impact of heavy ion radiation on the device. We have studied impact of radiation on different angle and different lateral locations, for the angular ion hit charge accumulated is max for the angle of incidence towards the channel region. And for the lateral variation it is found that the impact of radiation is max at the channel drain junction region.

In next section we have proposed a new radiation hardened design for the flip flop, which is more robust to radiation strike and also power efficient. This has been shown by comparing results with the other existing designs. We have also proposed a new simulation algorithm to find out the most sensitive node to radiation for a given logic circuit.

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