INVESTIGATIONS ON DIRECT TORQUE CONTROL OF INDUCTION MOTOR DRIVE

Ph.D. THESIS

by

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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled **'INVESTIGATIONS ON DIRECT TORQUE CONTROL OF INDUCTION MOTOR DRIVE'** in partial fulfilment of the requirements for the award of the degree of Doctor of Philosophy and submitted in the Department of Electrical Engineering of the Indian Institute of Technology Roorkee, Roorkee is an authentic record of my own work carried out during a period from July 2010 to July 2014 under the supervision of **Dr. S. P. Singh**, Professor, Department of Electrical Engineering, Indian Institute of Technology Roorkee, Roorkee.

The matter presented in the thesis has not been submitted by me for the award of any other degree of this or any other Institute.

(VENKATA RAMANA NAIK N)

This is to certify that the above statement made by the candidate is correct to the best of our knowledge.

(**S. P. Singh**)
Supervisor

Date: _____

The Ph.D. Viva-Voce Examination of ***Mr. Venkata Ramana Naik N***, Research Scholar, has been held on …….

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ABSTRACT

IMs are used worldwide as the workhorse in industrial applications. These motors are more robust and capable of operation in hazardous as well as extreme environmental conditions. But the major drawback of an induction motor (IM) is the difficulty in its speed control, which had been the main reason for the use as a DC motor in variable speed applications. The most convenient way of speed control of IM is by varying the supply frequency. This method requires simultaneous control of the magnitude and frequency of the voltage applied to IM using Scalar control. This method of speed control of IM is simple, but suffers from the poor dynamic response of the IM. Therefore, the vector control or field oriented control (FOC) is used for IM drives requiring high dynamic performance. In this method, the stator current is resolved into two components, namely direct-axis and quadrature-axis currents, the former controls the flux in the motor and later controls the electromagnetic torque produced. The vector control has several advantages such as wide speed range, precise speed regulation, and improved dynamic response. The vector controller with voltage decoupler is used to provide the reference signals for the modulation scheme, which drives the inverter. In order to get quick dynamic performance, direct torque controlled (DTC) IM drive is used. The DTC is achieved by direct and independent control of the flux linkages and electromagnetic torque through the selection of optimal inverter switching which gives fast torque response without requiring more number of transformations and modulation blocks. Many industries have marketed various forms of IM drives using direct torque control since 1980.

Voltage Source Inverter generates three-phase voltages of varying magnitude and frequency to drive the stator of IM. To achieve control of the magnitude and frequency of the inverter output voltage, three control techniques, namely sinusoidal pulse width modulation (SPWM), third harmonic injected pulse width modulation (THIPWM), and space vector modulation (SVM) are commonly used. The optimum utilization of the available DC bus voltage and the wide range of linear operation are extremely important in order to achieve the maximum output torque under all operating conditions. In this respect SVM results in higher utilization of DC bus voltage and reduced harmonic content of the output voltage as compared with SPWM method for the voltage source inverter (VSI).

The proportional integral direct torque control (PIDTC) along with SVM technique is used to operate the IM drive in various operating modes. The PIDTC suffers from the following problems: The stator flux ripple under steady state is more while operating at and above modulation index 0.5, thereby, causing the deterioration of the harmonic spectrum of output waveforms. The conventional PI controllers are tuned for specific operating point and do not operate satisfactorily when the operating point changes. Also, the PI-controllers cannot tune well, especially for the non-linear control system, which results in the inferior dynamic performance while operating in a wide range of speed and load applications.

Therefore, the improvement of the IM drive can be mainly classified into two parts such as ripple performance (voltage, current, flux, and torque) and dynamic performance (transient time during the sudden disturbance of either reference or load). The ripple performance of the IM mainly depends on the PWM technique, whereas the dynamic performance depends on the type of the controllers. The dynamic performance of IM can be improved when PI-controllers are replaced by type-1 fuzzy control (T1FC) or type-2 fuzzy control (T2FC). The ripples can be significantly reduced by hybrid space vector modulation (HSVM) with T1FC or T2FC along with duty ratio control (DRC). The HSVM with T1FC or T2FC consists of three sequences or PWMs in which two are the clamping sequences and one is the continuous sequence (conventional SVM). However, the clamping sequences such as bus-clamped space vector modulation 1 (BCSVM1) and bus-clamped space vector modulation 0 (BCSVM0) are developed based on SVM principle and they are clamped to any phase or leg of the inverter i.e., either positive or negative of the DC-link voltage, respectively. These three sequences are employed in different amplitudes of root mean square (RMS) flux ripples at each and every instant of the reference vector movement. Hence, the average/overall RMS flux ripples be maintained less by operating an appropriate PWM as compared to conventional SVM. Moreover, the DRC along with T1FC or T2FC is employed with the switching times/pulses independent of sampling time to improve the firing strength of the inverter, which will improve the voltage and current THD performance of the IM than conventional PIDTC.

In general, the type-1 fuzzy logic control (T1FLC) is known as the fuzzy logic control. Here, a Mamdani type method is used to frame the rules for both input and output, which consists of a single membership function and easy to understand because of linguistic terms and the structure of simple logical rules such as IF, THEN, AND, OR and

NOT rules etc. Moreover, a centroid method is used in the defuzzification process to find the crisp output of the corresponding controller. The advantages of T1FLC or FLC are simple, easy to implementation, performs well when the system has uncertainty, and effectively deals with the non-linear control system without requiring very big complex equations using simple logical rules, which are decided by the expert. Hence, the controller gives the good performance as compared to conventional PI-control. To further improve the controllers' performance, a large footprint of uncertainty is considered and controls the output in three-dimensional control with the help of type reduction technique in the T2FC, which is used in the defuzzification process as compared to T1FLC. Moreover, the T2FC is represented as a two membership function and provides much improved decision making from a large footprint of uncertainty using type-2 reduced fuzzy set and improves the controller performance in spite of being more complex and requiring additional time for tuning of the controllers as compared to conventional or type-1 fuzzy control.

The model of type-2 fuzzy based direct torque control (T2FDTC) for a two-level voltage source inverter fed IM drive is simulated to analyse the performance of the IM. The performance of T2FDTC of IM drive is compared with the PIDTC and the type-1 fuzzy based DTC (T1FDTC). The training data for type-1 and type-2 fuzzy is selected based on the conventional PIDTC scheme. The performance of simulated T2FDTC fed IM drive is also verified by the experimental setup using dSPACE kit (*DS1104*). The performance of two-level inverter fed IM is simulated for T2FDTC with HSVM, T2FDTC with DRC, T1FDTC with HSVM, T1FDTC with DRC, and PIDTC. The simulated performance of IM for T2FDCT with HSVM is tested under different operating regions such as starting, step change in the speed, speed reversal in both forward and backward direction, load perturbation. The current and voltage total harmonic distortion (THD) during no-load and full-load at various switching frequency, flux and torque ripples, and overall efficiency are calculated and the performance is compared with the above four control schemes (T2FDTC with DRC, T1FDTC with HSVM, T2FDTC with DRC, and PIDTC). Finally, the T2FDTC of IM with HSVM provides better performance for aforesaid operating conditions with improved overall efficiency of the IM drive as compared to the other four control schemes (T2FDTC with DRC, T1FDTC with HSVM, T1FDTC with DRC, and PIDTC). The simulated performance of T2FDTC with HSVM is also verified with the experimental waveforms to show the betterment in voltage and current THD at various switching frequency during no-load and full load, flux and torque

distortion, speed fluctuation during load perturbation, and better overall efficiency under different loading condition as compared to other four control schemes.

Multilevel inverter technology is receiving wider attention for the use in high power applications. This is mainly due to its improved output waveforms over the conventional two-level inverter technologies i.e., better output voltage with reduced THD, reduction of voltage ratings of the power semiconductor switching devices and also the reduced electro-magnetic interference. The general function of the multilevel inverter is to get a desired voltage from several levels of DC voltages. For this reason, multilevel inverters can easily provide the high power required for a large electric drive. As the number of levels increases, the output line voltage wave form adds more steps, producing a staircase wave which approaches the sinusoidal wave with minimum THD. Therefore, the filter size is also reduced significantly.

The space vector diagram of multilevel inverter is divided into different forms of sub-diagrams, in such a manner that the SVM becomes more simple and easy to implement. But, these works do not reach a generalization of the two-level SVM to the multilevel inverters because; they divide the diagram into interfered geometrical forms which increases the computational burden. To overcome this, a simple and fast method is implemented wherein the space vector diagram of three-level inverter is converted into smaller or inner hexagons and bigger or outer hexagon being space vector diagram. When the reference vector is in the inner /outer hexagon, the corresponding switching states of the inverter are operated to produce the voltage levels of two/three. Thus the SVM of three-level inverter becomes very simple and similar to that of conventional two-level inverter SVM. Similarly, the SVM pulses are developed for five-level inverter also.

Each simplification process comprises of two steps. Firstly, from the location of a given reference voltage, one hexagon is selected among the hexagons. Secondly, the origin of the reference voltage vector is transformed towards the center of the selected hexagon. The same two-level SVM can be placed in three-level SVM method after correcting the reference voltage vector. The two-level inverter switching pulses are converted to three level. In addition, the DC-link capacitor voltages for three-level diode clamped voltage source inverter (TLDCVSI) for PIDTC, T1FDTC and T2FDTC are balanced well or maintained constant by selecting/operating an appropriate space vector without the need of an extra PI-controller. As similar to the two-level inverter, the performance and characteristics of T2FDTC is compared with T1FDTC and PIDTC for TLDCVSI. The simulated three-level inverter fed T2FDTC IM drive performance under

different operating conditions is compared with PIDTC and T1FDTC. The dynamic performance of three-level inverter fed IM drive with T2FDTC is improved in all operating regions such as less voltage and current THD, less flux and torque distortion, and high full load efficiency with significant improved dynamic response of the IM drive. The performance of the simulated T2FDTC of IM drive for three-level DCMLI is also verified on the experimental setup using dSPACE kit (*DS1104*) and compared its performance with T1FDTC and PIDTC.

The five-level diode clamped voltage source inverter (FLDCVSI) along with T2FDTC is also simulated in the Matlab environment under similar operating conditions as that of the two-level VSI. The simulated response of FLDCVSI with T2FDTC of IM is compared with T1FDTC and PIDTC. To validate the simulation results, an experiment is conducted with the same rating of the machine parameters as used in the simulation and experimental setup for two and three level inverters is fabricated. Moreover, the FLDCVSI for T2FDTC scheme shows the best improvement on voltage and current THD during no-load and full-load at any switching frequency with less flux and torque ripples, less speed change during load perturbation, less peaks/dips in DC-link capacitor voltages during different modes of operation, and better efficiency at any load with fast dynamic response of the IM drive as compared to PIDTC and T1FDTC.

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V_{abcs}	Stator voltage of phases a,b and c respectively
V_{abcr}	Rotor voltage of phases a,b and c respectively
i_{abcs}	Stator currents of phases a,b and c respectively
i_{abcr}	Rotor currents of phases a,b and c respectively
λ_{abcs}	Stator flux linkages of phases a,b and c respectively
λ_{abcr}	Rotor flux linkages of phases a,b and c respectively
ω	Angular velocity of arbitrary reference frame
v_{ds}	d- axis stator voltages
v_{qs}	q- axis stator voltages,
i_{ds}	d-axis stator currents
i_{qs}	q- axis stator currents
R_s	Stator Resistance per Phase
λ_{qs}	d-axis stator flux linkages
λ_{ds}	q-axis stator flux linkages
λ_{qr}	d-axis rotor flux linkages
λ_{dr}	q-axis rotor flux linkages
ω_r	Rotor Angular Speed
L_S	Self Inductances of stator
L_r	Self Inductances of rotor
L_m	Mutual Inductance
T_e	Electromagnetic Torque
η	Overall efficiency
μ_M	Membership functions
θ	Phase angle
ω_e	Angular Velocity of synchronously rotating reference frame
ω_{sl}	Slip speed
θ_e	Rotor angle
i_{ds}	Reference d-axis Stator Current
i_{qs}	Reference q-axis Stator Current
f	Supply frequency
p	Crisp value/position

k_{pf}	Proportional constant of flux PI-control
k_{if}	Integral constant of flux PI-control
Z_0	Crisp value of the centre of area value of type-1 fuzzy
$\vee$	Maximum operator
$\wedge$	Minimum operator
x	Crisp value of the corresponding fuzzy set
$\cup$	Union
$\cap$	Intersection
$^-$	Negation or complement
μ	Fuzzy set for the corresponding membership function
p_1	Crisp position at particular value
F^i	Type-2 fuzzy logic control for ith rule
$\overline{\Pi(\overline{A})}$	Upper MF is associated with upper bound
$\underline{\Pi(\overline{A})}$	Lower MF is associated with lower bound
E_s	Speed controller error
CE_s	Change of the error for the speed controller
E_T	Torque controller error
CE_T	Change of the error for the torque controller
y_l	Singleton left side of the THEN-ingredient for type-2 fuzzy
y_r	Singleton right side of the THEN-ingredient for T2FLC
δ_{T_l}	left side of the final crisp value for T2FLC
δ_{T_r}	rightt side of the final crisp value for T2FLC
$\delta_{\cos}$	Centre of sets of the crisp value for T2FLC
$\delta_{T_{ce}}$	Defuzzified value for speed control using T2FLC
$\delta_{T_{ce}}$	Defuzzified value for speed control using T2FLC
$\delta_{\omega_{slc}}$	Defuzzified value for torque control using T2FLC

LIST OF ABBREVIATIONS

A	Ampere
ADC	Analog to Digital Converter
AC	Alternating Current
AI	Artificial Intelligence
ANN	Artificial Neural Network
CSI	Current-Source Inverter
d-axis	Direct Axis
DC	Direct Current
DAC	Digital to Analog Converter
DCI	Diode Clamped Inverter
DRC	Duty Ratio Control
DSP	Digital Signal Processor
DTC	Direct Torque Control
EMI	Electro Magnetic Interference
FLDCI	Five Level Diode Clamped Inverter
FFT	Fast Fourier Transform
FIS	Fuzzy Inference System
FLC	Fuzzy Logic Controller
FOC	Field Oriented Control
GTO	Gate Turn off Thyristor
Hz	Hertz
HSVM	Hybrid Space Vector Modulation
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
IM	Induction Motor
kHz	Kilo Hertz
LSE	Least-Squares Estimation
N-m	Newton Meter
NPC	Neutral point Clamped
PI	Proportional Integral
PIDTC	Proportional Integral Direct Torque Control
PWM	Pulse width Modulation

q-axis	Quadrature Axis
R	Subscript Implies Stator Coordinates
RMSE	Root-Mean-Square
RPM	Revolutions per Minute
S	Subscript Implies Stator Coordinates
SPWM	Sinusoidal Pulse Width Modulation
SVM	Space Vector Modulation
THD	Total Harmonic Distortion
T1FDTC	Type-1 Fuzzy Direct Torque Control
T2FDTC	Type-2 Fuzzy Direct Torque Control
T1FC	Type-1 Fuzzy Control
T2FC	Type-2 Fuzzy Control
TLIDCI	Three Level Diode Clamped Inverter
TG	Tacho-generator
V	Volts
VSI	Voltage-Source Inverter

CHAPTER-1
INTRODUCTION

1.1 General

Conventionally, the earlier stages of the development variable speed drives were only separately excited DC motor due to its simplicity in control of flux and torque by the inherent decoupled field and armature currents, respectively. But recent technological advancements are making AC drives (particularly induction motor drives) more popular because they are generally cheaper, smaller, rugged and reliable with the absence of commutators and brushes. Overall, AC drives are much superior to DC drives, and it appears that eventually DC drives will be totally obsolete. Therefore, in the last three decades the DC motor drives are progressively being replaced by AC drives. The main reason behind this development is modern semiconductor devices specially insulated gate bi-polar junction transistor(IGBT) and Digital Signal Processor (DSP) technologies.

Inverter circuit is used to generate three-phase voltages of varying magnitude and frequency to drive the stator of induction motor (IM). In general, two basic types of inverters exist: voltage-source inverter (VSI) employing a DC-link capacitor and providing a switched voltage waveform and current-source inverter (CSI), employing a DC link inductance and providing a switched current waveform at the motor terminals. VSI is more common compared to CSI since the use of pulse width modulation (PWM) allows efficient and smooth operation. Furthermore, the frequency range of VSI is higher and they are less expensive when compared to CSI drives of the same rating.

The control of this inverter plays an important role in deciding the output of inverter and hence the response of IM. To achieve control of the magnitude and frequency of the inverter output voltage, two main control techniques, namely- sinusoidal pulse width modulation (SPWM) and space vector modulation (SVM) are commonly used. Optimum utilization of the available DC bus voltage is extremely important in order to achieve the maximum output torque under all operating conditions. In this respect, a space vectors modulation result in higher utilization of DC bus voltage compared to SPWM method for the VSI.

But the disadvantage of conventional SVM is that it requires complex online computation that limits the switching frequency of the inverter and practically DSP based conventional SVM algorithm is constrained as the switching frequency increases. In order to utilize the high switching frequency power semiconductor devices (MOSFETs) effectively, the operating frequency of SVM has to be increased. The soft computing based techniques like type-1 fuzzy control, type-2 fuzzy control can be used to improve the firing strength of the inverter using duty ratio control or hybrid PWM control [107-109].

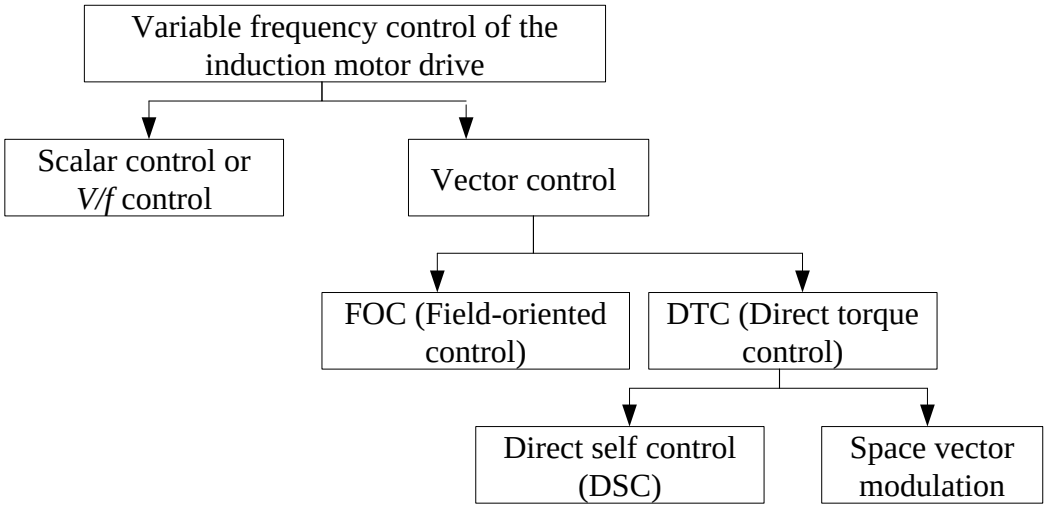


Fig. 1.1 Classifications of variable frequency drives

Together, with inverter control techniques and using the improved closed loop control method the dynamic performance of IM can be enhanced. The simplest methodin speed control of IM is variable frequency of the IM drive (VFIMD). The VFIMD are mainly classified into two types such as a scalar control (*V/f* control) and vector control as shown in Fig. 1.1. The scalar control requires simultaneous control of the magnitude and frequency of the voltage applied to IM. This method of speed control of IM is although simple, suffers from the poor dynamic response. Whereas, the vector control is used for IM drives for high dynamic performance as compared to scalar control. The vector control is again divided by two types: field oriented control (FOC) and direct torque control (DTC). In FOC, the torque and flux are indirectly controlled by controlling the d-q axes of currents to improve the dynamic performance of the IM like a separately excited DC-motor. However, FOC requires many controllers, co-ordinate transformations, rotor position sensor, etc. To improve further the fast dynamic performance of IM drive, DTC is used, in which the electromagnetic torque and flux of the IM are directly controlled with less number of transformations and sensors required.

The DTC is classified into two types such as direct self control (DSC) and space vector modulation. In DSC, the torque and flux are controlled using the hysteresis control with help of switching table. However, DSC provides variable switching frequency with more torque and flux ripples of the IM due to hysteresis control. Hence, it's very difficult to design the filter to reduce the torque and flux ripples of the IM. Whereas in DTC, along with space vector modulation (SVM) the switching frequency is maintained constant with significant improvement in flux and torque distortion as compared DSC. In DTC, determination of instantaneous magnitude and position of stator flux space vector must be known at every instant of time with precision to control the torque and flux components directly. In addition, the accurate speed information is necessary to realize the high performance. A speed transducers such as shaft mounted tacho-generator, resolvers or digital shaft encoders are generally used to obtain the speed information.

The conventional PI controllers are used in DTC based on the mathematical model of the system. Conventional PI controllers tuned for specific operation point, does not operate satisfactorily when the operating point changes for a wide range of speed control. To overcome this problem conventional PI controller can be replaced by intelligent controllers in order to obtain the best performance.

1.2 Literature Review

The comprehensive literature survey is carried out during the course of study and research on Investigations on Inverter fed IM drive is presented as discussed by classifying the literature into the following categories.

- Direct torque controlled IM drive.
- Pulse width modulation techniques.
- Soft computing techniques.
- Multilevel inverter (MLI)

1.2.1 Direct Torque Controlled Induction Motor

The speed of an IM is controlled using various control techniques that are used and explained in this literature. Alfredo Munoz-Garcıa, et. al [1] has investigated a novel open-loop speed control method for IMs that provides high output torque and nearly zero steady-state speed error at any frequency. The control scheme is based on the popular constant volts per hertz (*V/f*) method using low-cost current sensors. Only stator current measurements are needed to compensate for both stator resistance drop and slip

frequency. The proposed scheme fully compensates for the current resistance (IR) voltage drop by vectorially modifying the stator voltage and keeping the magnitude of the stator flux constant, regardless of changes in frequency or load. Allan B. Plunkett, et. al [2] has described a method of motor flux and torque sensing, that reduces the waveform harmonics and motor parameter variations with less motor torque oscillations. Marian Pet, et. al [8] has developed the DTC without requiring any co-ordinate transformation using the single current control as compared to the FOC. However, the problems occur at zero speed region that can be overcome by an additional carrier signal was given to the torque control input. The robust start and improved operation at low speed operation can be achieved with DTC than FOC. The DTC of the IM drive in which torque and flux are estimated using hysteresis controller along with the switching table without requiring many controllers and co-ordinate transformations, etc. Hence, the DTC has very fast and quick dynamic response than FOC, but it gives more torque and flux ripples. These ripples are difficult to eliminate due to the variable switching frequency produced by the hysteresis control [3-5]. C. L. Toh, et.al [6] has presented the DTC using FPGA and DSP and maintained constant switching frequency with reduced torque ripples using duty ratio control. Hao Yun, et.al[7] has shown that the torque and flux can be controlled separately by using the microcomputer, by selecting zero and nonzero space vectors respectively. Therefore, flux and torque control can be achieved separately. O. Barambones, et. al [9] has shown a sliding-mode controller with an integrated switching surface. The closed-loop stability of the proposed controller is proved under parameter uncertainties and load disturbances, using the Lyapunov stability theory. Simulated results show that the proposed controller, jointly with the proposed observer, provides high-performance dynamic characteristics and this scheme is robust with respect to plant parameter variations and external load disturbances. Finally, the feasibility of the proposed control scheme is proved by means of experimental results on a real IM.

Masood, et. al [10] has investigated on DTC with sliding mode observer for simultaneously detecting the rotor flux, motor speed and time constant. Moreover, a fast and search based method has been introduced to maximize the motor efficiency. Joon, et. al [11] has worked on the unified flux control algorithm to reduce the stator flux and torque ripple of the IM. The proposed algorithm compensates rotational back emf and made the stator voltage with the dead beat control directly from the flux and torque estimators. Nik Rumzi, et. al [12] has investigated on DTC with low pass filter (LPF) and compensates the control scheme to improve the torque and flux performance under steady

state condition. Abdelhakim, et. al [13] has investigated on a loss-minimization of DTC scheme for electric vehicles to minimize the IM losses and to evaluate the optimal magnetizing flux. Jef Beerten, et. al [14] has minimized the torque and flux ripples by maintaining the computation time as constant even an increasing the sampling frequency. Domenico, et. al [15] has investigated the matrix converter for DTC in which a high dynamic performance of the IM drive during regenerative braking was obtained with unity power factor. Anthony Purcell, et. al [16] has introduced a new switching strategy for reduced torque ripples and increased dynamic response as compared to conventional DTC. Purcell, et. al [17] has Presented on DTC to improve torque performance by increasing the switching frequency of the inverter with optimized switching's. Ahmad, et. al [18] has investigated the choice of the sliding mode theory, such as the switching between direct and indirect VSI control. The switching from one algorithm to another is achieved in smoother manner, shorter the execution time, and better torque performance under steady state. Cristian, et. al [19] has investigated the better torque and flux strategies with FLC as compared to conventional methods. Manuele, et. al[20] has presented on DTC of an IM using a single current sensor. This scheme has low cost with fast dynamic performance and the algorithm operates in two stages: 1) to predict stator currents from the model of the IM, and 2) to adjust the prediction on the basis of the sensed DC link current. Radu, et. al [21] has shown that the inverter has a constant inverter switching frequency, good transient performance and low distortion of the machine currents with respect to DSC and DTC scheme for variable frequency. A. Purcell, et. al [22] has developed a method for reducing torque pulsation in direct torque controlled IMs, based on a switching update rate, which is higher than the rated power device switching rate. Udayar Senthil, et. al [23] has investigated on to effectively minimize the stator currents and toque ripples even at high speeds by using different types of switching states of the DTC as compared to conventional DTC. G. Escobar, et. al [24] had developed a control vector (switching position), which is selected directly without the requirement of an auxiliary space vector. In addition, it has considered on the basis of quadratic and absolute functions. Finally the absolute and quadratic control has given better speed and torque performance as compare to classical DTC. Yen-Shin Lai, et. al [27] has investigated on SVM-DTC and shown that the torque and flux ripples are drastically reduced as compare to existing DTC approach with constant inverter switching frequency. Thomas G, et. al [28] has investigated on DTC in which the voltage space vectors are calculated to control the flux torque on dead beat fashion and SVM duty

cycle are used to improve the inverter performance. Zhifeng Zhang, et. al [29] has investigated on DTC, the torque performance and flux ripples were reduced significantly by using the SVM technique with improved dynamic response of IM than conventional DTC. J. Rodri, et. al [30] has investigated the torque ripple that can be partially compensated, by the new DTC scheme using discrete space vector modulation (DSVM). Domenico, et. al [31] has developed the discrete space vector direct torque control toget lower ripples in torque, flux, and stator currents as compared to conventional DTC. Cristian, et. al [32] has developed the control strategy that combines VSI and DTC principles with a simple, robust, and high performance drive. Moreover, the low torque, current, and flux ripples were mainly due to SVM. Cristian, et. al [33] has introduced a new direct torque and flux control based on space vector modulation(DTC-SVM) for IM sensor-less drive. It is able to reduce the acoustic noise, torque flux, current, and speed pulsations during the steady state as compared to classical DTC.

1.2.2 Pulse Width Modulation (PWM) Techniques

Usually, the pulse width modulation (PWM) techniques for VSI are used to control the frequency of the inverter by varying the modulating frequency and output voltage by controlling the amplitude of either modulating or carrier wave, and to reduce the total harmonic distortion by increasing the carrier frequency. The performance of an IM drive largely depends on inverter control techniques. The PWM strategies are required for switching the devices in a VSI, which produce the power with variable voltage and variable frequency. The number of pulse width modulation strategies has been developed and studied [24, 70, 104, 125]. The most commonly used pulse width modulation techniques are

- Sinusoidal PWM (SPWM)
- Third harmonic injection PWM (THIPWM)
- Space vector modulation(SVM)

In SPWM, a carrier wave is compared with the three sinusoidal reference waves by shifting an angle of 120^{o} to generate the firing pulses for the three phase inverter. However, the main disadvantage of SPWM is the attenuation of the fundamental voltage of the inverter because the linear modulation index (MI) for the SPWM is limited to 0.786, its' voltage and current THD of the inverter is high at above MI 0.786.Hence, the IM drive may not operate at rated values because of less MI. Also, the switching losses,

stress on switching devices are more at higher switching frequency operation. Because, there is no proper procedure to operate the switching devices from one state other state. In the [19], the reference/modulating waveform for THIPWM is generated by adding the actual sine wave to the third harmonic component. The THIPWM technique provides the more fundamental voltage of the inverter i.e., 15.57% and it increases the liner modulation index range from 0 to 0.907 as compared to the SPWM technique as shown in Fig. 1.2. The THIPWM increases the fundamental voltage with significant reduction of current ripple of the IM at above modulation index 0.786 as compared to SPWM. The disadvantage of THIPWM technique is that there is no defined procedure for determining the proper amount of the added third harmonic component. The SVM is also used for better utilization spectral performance and also reduced the THD at and above the MI 0.7866. In addition, SVM not only increases the linear modulation index range (0.907) but also operates a single switching transition for every change in space vector movement, which implies to reduce the stress on switching device and switching losses as compared to SPWM and THIPWM[74, 84-85] [25, 27].

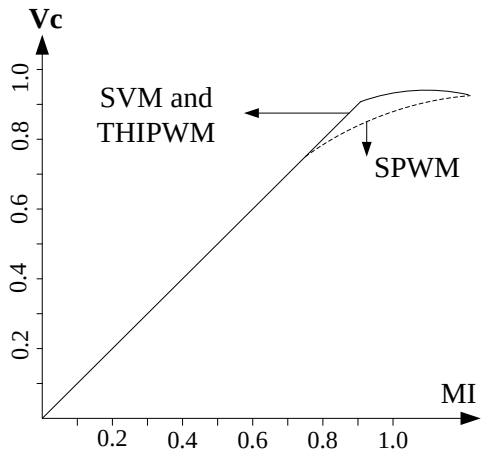


Fig. 1.2 MI vs. per unit control voltage (V_c) of the inverter

Cristian, et. al [33] has investigated on the control strategy that combines the advantages of VSI and DTC using space vector approach. Tushar Bhavsar, et.al [34] has studied the spectral properties of the waveforms produced by the PWM techniques for open loop *V/f* control IM using a two-level inverter. Further, an analytical closed-form expression is derived for the total harmonic distortion due to the PWM techniques. It is shown that the advance bus-clamped PWM (ABCPWM) techniques leads to reduce the flux and current ripples at above MI 0.7 than the conventional SVM. Joachim Holtz, et. al [35] has investigated on feed forward and feedback PWM schemes having relevance for industrial application and described their respective merits and shortcomings. The

secondary effects such as the influence of load current dependent switching time delay and transients in synchronized PWM techniques are discussed, and adequate compensation methods are presented. A recorded oscillograms illustrates the performance of the respective PWM principles. G. Narayanan, et. al [36] has introduced seven types of the PWM techniques based on principle of conventional SVM to reduce the current and flux ripple of the IM for two level VSI.. Here, each sector is divided by three-zone, five-zone, and seven-zone and the number of PWMs are used for the corresponding zones are three, five, and seven, respectively. Moreover the IM current ripple with seven-zone PWM was improved by 40% over a conventional SVM and also proved the seven-zone PWM has improved ripple performance at any modulation indices (up to the 0.866) as compared to the five-zone, three-zone HPWM and conventional SVM.

1.2.3 Soft Computing Techniques

Normally, the soft computing techniques are mostly used to improve the dynamic performance of the IM drive. The soft computing techniques are mainly classified as

- Neural network control (NNC)
- Neuro-fuzzy control (NFC)
- Type-1 fuzzy logic control (T1FLC) or fuzzy logic control (FLC)
- Type-2 fuzzy logic control (T2FLC)

Telford et. al [26] has shown the torque and flux ripples can be reduced at low speed by using duty cycle control. This scheme also effectively controls the mean of the output torque, and limits the switching frequency variation. Yongchang, et. al [37] has shown that the speed can be controlled over a wide range by using adaptive FLC even in case of sensor-less control of IM drive. The torque and flux performance can be improved with FLC compared to conventional DTC. Luis, et. al [39] has developed the training algorithms, the back propagation, adaptive neuron model, extended filter, and parallel recursive prediction error. The results of the extended Kalman filter, and the parallel recursive prediction error gives the best performance on torque of IM. This can be the optimum algorithm since it combines the gradient descent method with the Newton algorithm. Luis, et. al [45] has used artificial neural network and tuned the stator resistance in the controller to track actual resistance of the machine. The simulation and experimental results show that the neural network configuration gives more accurate results than the conventional control scheme. M. Godoy, et. al[40] has developed the neural network estimator, which provides the advantages of faster execution speed,

harmonic ripple immunity, and fault tolerance characteristics compared to DSP-based estimator.

L. Arias, et. al[41] has investigated on the FLC for DTC of IM drive. The DTC along with FLC has provided a major reduction in the undesirable torque ripple over classical DTC drive systems. Also, the reduction in reactive power drawn from the main supply resulting from the inclusion of the novel optimum stator flux controller is an additional benefit for the new drive system. G. Bird, et. al [42] has shown that the torque ripples are drastically reduced with fuzzy logic DTC (FLDTC) especially at low speed and high speed applications compared to conventional DTC. Sayeed et. al [43] has applied the direct self control using FLC, which provides better dynamic response of IM drive at rated speed control. At low speed operation also, the performance was improved with fuzzy stator resistance estimation. Pawel et. al [44] has shown the adaptive Neuro fuzzy inference system is applied to achieve high dynamic performance of decoupled flux and torque control. The DTC method was proposed to achieve both torque ripple reduction with constant switching frequency. The novel fuzzy logic DTC (FL-DTC) introduces a two-state modulation between the selected active and zero states. This modulation is controlled by an adaptive FLC, which calculates the optimum duty cycle with a low execution time for each sampling period[45]. Yen, et. al[46] has shown the combining all the advantages of P, PD, PI, and PID with FL-DTC has low steady state error compare to the PI-type FL-DTC.

The type-1 fuzzy control (T1FC) has a single membership function (MF) with two-dimensional control and simple logic rules such as IF, THEN, AND, OR and NOT [20]-[25],[29]. The F1C deals with the small foot-print of uncertainty (FOU) only, whereas the type-2 fuzzy control (T2FC) effectively deals the large footprint of uncertainty (FOU) with type-reduction in three-dimensional control, which is represented as two MF [20]-[25], [25]-[31]. S. Barkati, et. al [47] has investigated on the performance comparison between the T2FC and conventional FOC methods in which the T2FC was provided better simulation results in terms of overshoot, steady-state error, torque disturbance, and variable-speed tracking than conventional FOC. The T2FC has given good performance, because it estimates the control variable as close to the actual values than T1FC. Also, the fluctuations of the capacitor voltages are compensated well by drawing a sinusoidal current with nearly unity power factor, and ensure a smooth speed control action as compared to conventional control scheme.

1.2.4 Multilevel Inverter (MLI)

Generally the two level inverters are not suitable for high power applications, because the stresses on each device are more, which implies higher dv/dt, di/dt, switching losses, and the Thyristor's will not withstand due to high temperature(high voltage and current). By using MLI the above disadvantages are eliminated, and the harmonic spectrum is substantially improved as compared to the two-level inverter.

MLI technology has emerged as an important alternative in the area of high-power medium-voltage energy control. MLI concept is mainly suggested for reducing the harmonic content of the inverter output at a low switching frequency for high power applications [15, 21].The MLI has mainly classified as

- Diode-clamped multilevel inverter (DCMLI)
- Flying capacitor multilevel inverter (FCMLI)
- Cascaded multilevel inverter (CMLI)

The development in multi level inverter began in the early eighties when Nabae, et.al [93] presented a DCMLI or neutral point clamped MLI in 1981. Thereafter, different topologies in MLIs emerged: DCMLI, capacitor-clamped inverter or flying capacitor, and cascaded inverter and their control. Their control, modulation techniques, advantages and disadvantages of different topologies are discussed in [71,104, 105]. In order to improve the performance of MLI, the combination of basic MLI topologies are developed [11, 20, 115, 116]. A multilevel diode clamped back to back inverter for use in large electric drive with control strategy has been presented in [120]. The main disadvantage of this topology is that the required blocking voltage of the clamping diodes is proportional to the level for which they are used to employ clamping action and the clamping diodes can be subject to severe reverse-recovery stress, which limits the use of this topology. The recent advances and industrial applications of MLIs and their contributions is presented in [106]. Out of the different topologies, a DCMLI has found an important market for motor drives applications like conveyors, pumps, fans and mills, because the control method is simpler with less cost and space required [71].

Kyo-Beum, et. al [48] has shown that the DTC with three level-inverter reduces the torque ripples significantly at different loads/speed as compared to the two-level inverter. Alain Sapin, et. al [49] has investigated on the LC-filter connected between three level inverter and IM, which results in considerably reduced the torque, current, and flux ripples of the IM as compared to the conventional method. Kyo-Beum, et. al [50] has

investigated on the low speed performance of DTC along with the three level inverter fed IM drive. Because of the stator resistance estimation along with effective control of active state voltage vectors, the proposed method shows the improved dynamic performance of the IM over a conventional control method. Farid Khoucha, et. al [51] has investigated on fuel cells fed cascaded MLI in which the line voltage, currents are near to sinusoidal, which implies that the torque and flux ripple performance can be effectively improved in the MLI than two level inverter. Miguel, et. al [52] has investigated on the H-Bridge MLI fed IM drive in which the quality of flux and torque are improved with less stress and dv/dt on the switching devices compared to the two-level inverter. José Rodríguez, et. al [53] has proposed a DTC with 11-Level CMLI using imposition algorithm, which improved the quality of voltage and current with less torque ripple magnitudes than conventional method. Because, the use of the frequency imposition algorithm helped to minimize the variation of the switching frequency for typical standard DTC applications due to hysteresis comparator. This improvement produces a narrow torque spectrum even for high band frequencies. Samir, et. al [54] has shown that the torque, speed, and flux ripples are reduced with cascaded H-bridge multi-level inverter without required an extra filter. Also, the switching losses are found to be less with asymmetrical MLI.

Haoran Zhang, et. al [55] has investigated on the common-mode voltage, which is generated by the conventional PWM inverters. The major cause of motor bearing failures is due to the resulting leakage currents through the bearings. Similarly, the resulting current through the parasitic capacitance between the motor windings and frame adds to the total leakage current through the ground conductor resulting in increased EMI and false tripping of relays. It has been proven experimentally that cancellation of the common-mode voltage will eliminate the bearing currents and reduce the conducted EMI significantly. The simulation and experimental results show that MLI (three-level)with modified modulation schemes are not generating any common-mode voltages. Both SVM and sinusoidal SPWM are analyzed based on three-level inverters. This concept is also applied to both medium and low-voltage multilevel inverter applications to eliminate the common-mode voltage and improve the reliability of the IM drive.

1.3 Scope of Work and Author Contribution

The literature review carried out in the field of inverter fed IM drive has revealed that the most developments are in the direction of reducing THD, control hardware, and improving the quality of the drive output. Many schemes described in the literature deal with problem of switching of the inverter and the improved speed control schemes so that the dynamic performance of IM can be enhanced. It is found that extensive efforts are being made to improve the performance of inverter with the help of modifications in topological and control methodologies.

A proportional integral direct torque control (PIDTC) with SVM technique and PI-control of speed, torque, and flux control has been found probably the fair scheme for two-level inverter fed IM drive. The closed loop stability performance for PIDTC of IM is also checked with the bode plot after finding the overall transfer function with the corresponding gains of the PI-controllers. However, PIDTC provides considerable current, flux, and torque ripples with poor dynamic response. Because, the SVM doesn't provide root mean square (RMS) flux ripples and current ripples at and above the MI 0.5. In addition, the PI-controllers cannot work properly especially for the non-linear control system, which decays the dynamic behaviour of the system for a wide range of speed/load control. In order to improve further the dynamic response of the IM drive the type-1 fuzzy direct torque control (T1FDTC) method is developed in which the PI-controllers are replaced by type-1 fuzzy control (T1FC) to get quick control response. To improve the current and flux ripple performance in T1FDTC, the duty ratio control (DRC) and hybrid space vector modulation (HSVM) is used with the help of T1FC and compared their performance with PIDTC. To improve further dynamic behaviour and the steady state flux and current ripple performance of the IM drive in comparison to PIDTC and T1FDTC, the type-2 fuzzy DTC (T2FDTC) is used in which the PI-controllers are replaced by type-2 fuzzy control (T2FC) along with DRC and HSVM with the help of T2FC. Because, the T2FCeffectively handle the large footprint of the uncertainty with three-dimensional control and also it has the advantage of type reduction in the defuzzification process to select the appropriate control variable, which is close to the actual value as compared to T1FC.Therefore, in the present work, an attempt is made in the direction of developing a type-2 fuzzy based DTC (T2FDTC) for getting better performance of the two-level inverter fed IM drive than PIDTC and T1FDTC.

On the other hand MLIs are gaining wide popularity in industrial applications because of better performance and improved power quality as compared to the two-level inverter. Among the topologies of multi level inverter, a diode clamped multi-level inverters is widely used because of the low cost and simplicity. However, developing the space vector modulation technique is a complex issue. Hence, an attempt is made in such a manner that the developed two-level space vector modulation technique can be used in three-level space vector modulation. In addition, DC-link capacitor voltages for three-level inverter are balanced without the need of an extra controller.

Another issue observed from the literature is that performance of controllers used in the direct torque controlled IM drive is not precise when the operating point changes. An Intelligent controller such as, T1FLC and T2FLCis used to improve the performance of IM drive.

In view of the scope of work revealed by the literature survey made on IM drive an attempt has been made to establish the following contribution in the present investigation:

- Modelling and development of the controller using T1FLCand T2FLC:

A mathematical model for T1FC and T2FLCis developed. In this, the premise (non-linear) and consequent (linear) parameters of the fuzzy inference system (FIS)are tuned with the help of experts, which optimally represents the logical/mathematical relationship between the input and output space. In the first step, an approximate fuzzy model is initiated by the system and then improved through an iterative adaptive learning process.

- Development of type-2fuzzy DTC (T2FDTC) method for two-level inverter:

An algorithm for T2FDTC method is developed for generating switching pulses to the inverter. For the performance and comparison sake, the PIDTC and T1FDTC are also developed and simulated. The generated data is used for tuning of T1FLC and T2FLCto improve the dynamic performance of the IM. To improve the ripple performance (current, flux, and torque) of the IM, the HSVM and DRC are used in both the control schemes (T2FDTC and T1FDTC).

Simulation results obtained with the T2FDTC are compared with PIDTC and T1FDTC. The simulation results obtained are verified experimentally using a dSPACE kit (DS-1104).The performance measured in-terms of the total harmonic distortion (*THD*) of inverter voltage and current, speed, flux and torque distortion, and overall efficiency have been evaluated with T2FDTC, T1FDTC, and PIDTC.

- A design and implementation of T2FDTCfor three-level SVM inverter fed IM drive:

In order to use PIDTC, T1FDTC,and T2FDTCschemes in three-level inverter a simplified SVM algorithm is used and implemented. In this technique, a three-level inverter space vector diagram is decomposed into two-level space vector diagrams. The performance of T2FDTC along with three-level inverter fed IM drive is compared with PIDTC and T1FDTC. The voltage and current THDs of the inverter, flux and torque distortion, and overall efficiency are obtained from the simulation and is verified experimentally using dSPACE (DS-1104).

- Performance and evaluation of T2FDTC for five-level SVM inverter in closed loop control of IM drive:

The simulated performance of T2FDTC along with five-level inverter fed IM drive is evaluated using dSPACE (DS-1104) and its performance is compared with PIDTC and T2FDTC as similar to a three-level inverter mentioned earlier.

The PIDTC model is developed for closed loop control and to analyze the stability behaviour with the help of bode-plot after finding closed loop transfer function of the entire system. The performance of the two-level, three-level, and five-level inverter fed IM drive under various operating conditions is compared with conventional PIDTC and T1FDTCschemes.

1.4 Thesis Organization

The text of the thesis is distributed in seven chapters. An outline of each chapter is presented below:

In **Chapter 1**,a brief overview of space vector modulation, need of soft computing based space vector modulation, and direct torque control of IM drives is mentioned. An exhaustive survey of the literature on variable speed AC motor drive and the scope of the present work are followed by the contribution of the author and the format of the thesis

In **Chapter 2**,the type-1 and type-2 fuzzy control schemes are analyzed conceptually and mathematically and the motivation for using type-2 fuzzy is presented.

In **Chapter 3**,the design procedure for PIDTC, type-1 and type-2 fuzzy based DTC for the two-level inverter control is presented. The performance of the inverter and an IM are compared by using conventional, type-1 and type-2 fuzzy based DTC methods. The simulation results are verified experimentally using dSPACEDS-1104 kit.

In **Chapter 4**, theconventional,type-1 fuzzy, and type-2 fuzzy based DTC methods of chapter-3 are used in three-level SVM inverter. In order to use two-level SVM methods in

three-level SVM, a simplified space vector modulation is used. The obtained simulation results are verified experimentally.

In **Chapter 5**, the performance of five-level inverter fed direct torque controlled IM with type-2 fuzzy control is simulated, evaluated, and compared with conventional (PIDTC), and type-1 fuzzy control.

In **Chapter 6**, the system and developments for the hardware-setup in real time application is explained in detail.

In **Chapter 7**, the main conclusion along with salient features of inverter fed IM drive based on simulation and experimental results are listed. Applications along with the scope for future work are also indicated.

Sincere attempts have been made to refer the original source of references, which are appended at the end.

Based on the research work the list of research work publications as given below

1) One paper is published in Electric Power Components and System.
2) Two papers are accepted and published for the publication in IEEE Transactions on Industrial Electronics.
3) One paper is accepted and published for the publication in IETE Technical Review.
4) One paper accepted with minor change in Electric Power Components and System.
5) One paper is under minor revision in IEEE Transactions on Industrial Electronics.
6) One paper is under minor revision in International Journal Electronics.
7) The seven IEEE international conference papers have been presented and published.

CHAPTER -2

DESIGN AND DEVELOPMENT OF TYPE-1 AND TYPE-2 FUZZY LOGIC CONTROL

2.1 Introduction

A self learning control algorithm for the direct torque control of an IM drive can be improved with the help of artificial intelligence, such as expert systems, fuzzy logic control (type-1 fuzzy logic control or (T1FLC)), and type-2 fuzzy logic control (T2FLC). The T1FLC has been proved to be efficient in a wide range of engineering applications [40-44, 70, 82, 107, 108, 143-151]. Till now, the T1FLC is already used for drive applications to get better performance. The scope of the research is further extended for the application of direct torque control of IM drive using T2FLC. In this chapter, the design procedure for both artificial intelligent controllers (T1FLC and T2FLC) is discussed in detail. The T2FLC has three-dimensional control, handles effectively with large foot print of uncertainty, and also provides type-2 reduced fuzzy set in defuzzification process [143-151]. Whereas T1FLC consists of a single membership function (MF) and two-dimensional control without requiring any type reduction. An expertise is also required to select the MFs and to frame the rules as per the personal experience in both T1FLC and T2FLC [107-108]. The success is mostly due to the fact that the fuzzy controllers are suited well for capturing the imprecise nature of the human knowledge and reasoning processes. Mamdani type and centroid method are used in both the artificial intelligent schemes, because of simplicity with simple logic rules (such as IF, THEN, AND, OR, NOT etc), which is easy to implement without requiring any complex equations. Moreover, it effectively handles the huge ambiguous data in both linear and nonlinear control systems and provides robust performance.

2.2 Type-1 Fuzzy Logic Control

The T1FLC is a class of artificial intelligence (AI), but its history and applications are more recent than those of the expert systems (ES). According to George Boole, human thinking and decisions are based on "yes"/"no" reasoning, or "1"/"0" logic [40-44, 107-108]. The expert system (ES) principles were formulated based on Boolean logic. It has been argued that human thinking does not always follow crisp "yes"/"no" logic, but is

often vague, qualitative, uncertain, imprecise, or fuzzy in nature [70-82]. Based on the nature of fuzzy human thinking, Lotfi Zadeh, a computer scientist at the University of California, Berkeley, originated the "fuzzy logic," or fuzzy set theory, in 1965. In the beginning, he was highly criticized by the professional community, but gradually, fuzzy Logic (FL) captured the imagination of the professional community and eventually emerged as an entirely new discipline of AI [70, 82]. The general methodology of reasoning in FL and ES by "IF... THEN ..." statements or rules is the same; therefore, it is often called "fuzzy expert system." FL can help to supplement an ES, and it is sometimes hybrided with the latter to solve complex problems. FL has been successfully applied in process control, modeling, estimation, identification, diagnostics, military science, stock market prediction, etc.

2.2.1 Type-1 Fuzzy Sets

T1FLC unlike Boolean logic deals with problems that have fuzziness or vagueness. The classical set theory is based on Boolean logic, where a particular object or variable is either a member of a given set (logic 1), or it is not (logic 0). On the other hand, in fuzzy set theory based on FL, a particular object has a degree of membership in a given set that may be anywhere in the range of 0 (completely not in the set) to 1 (completely in the set). For this reason, FL is often defined as multi-valued logic (0 to 1), compared to bi-valued Boolean logic. It may be mentioned that although FL deals with imprecise information, the information is processed in sound mathematical theory, which has been advanced in recent years [43-46].

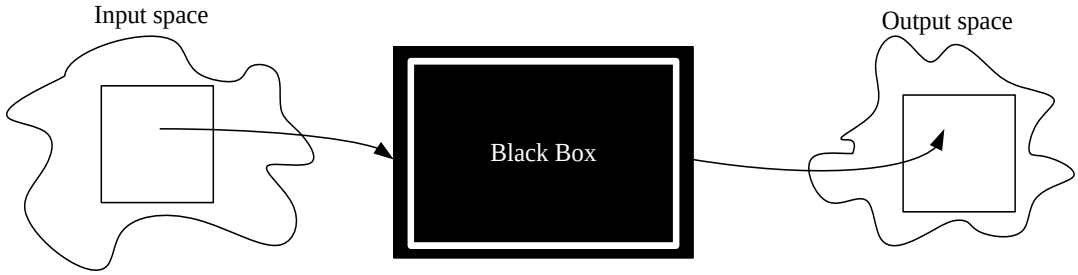


Fig. 2.1: Input/output mapping problems

Before discussing the FL theory, it should be emphasized here that basically, a FL problem can be defined as an input/output, static, nonlinear mapping problem through a "black box" as shown in Fig. 2.1. All the input information is defined in the input space, it is processed in the black box, and the solution appears in the output space. In general, mapping can be static or dynamic, and the mapping characteristics are determined by the black box's characteristics [65-72]. The black box can not only be a

type-1 fuzzy system, but also an ES, neural network, general mathematical system, such as differential equations, algebraic equations, etc., or anything else [41-45].

2.2.2 Type-1 Membership Functions

A membership function (MF) can have different shapes, as shown in Fig. 2.2. The simplest and most commonly used MF is the triangular-type, which can be symmetrical or asymmetrical in shape. A trapezoidal MF (symmetrical or unsymmetrical) has the shape of a truncated triangle [38-44]. Two MFs are built on the Gaussian distribution curve: a simple Gaussian curve and a two-sided composite of two different Gaussian curves [143-150].

The bell MF with a flat top is somewhat different from a Gaussian function. Both the Gaussian and bell functions are smooth and non-zero at all points. A sigmoidal-type MF can be open to the right or left. Asymmetrical and closed (not open to the right or left) MFs can be synthesized using two sigmoidal functions, such as difference sigmoidal (difference between two sigmoidal functions) and product sigmoidal (product of two segments). Polynomial-based curves can have several functions, including asymmetrical polynomial curve open to the left (Polynomial-Z) and its mirror image, open to the right (Polynomial-S), and one that is zero at both ends but has a rise in the middle (Polynomial-Pi). In addition to these types, any arbitrary MF can be generated by the user. In practice, one or two types of MFs (such as triangular and Gaussian) are more than enough to solve most problems [42-48].

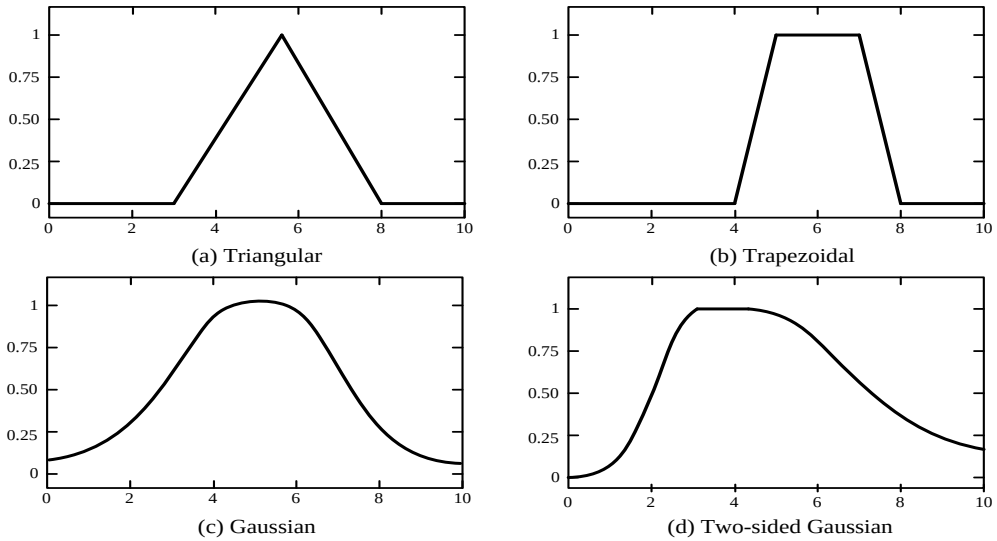


Fig. 2.2 (a): Different types of MFs for T1FLC (a) Triangular, (b) Trapezoidal, (c) Gaussian, (d) Two-sided Gaussian

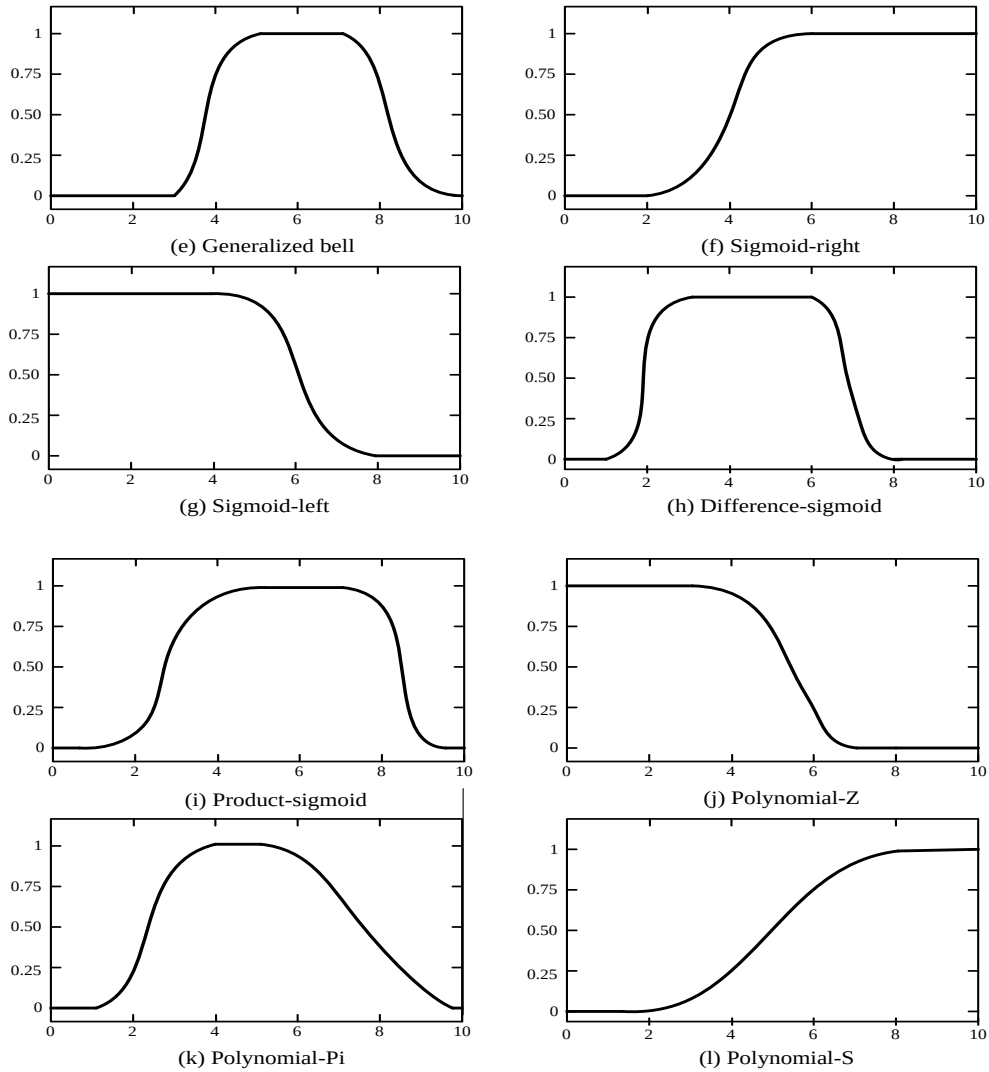


Fig. 2.2 (b): Different types of MFs for T1FLC (e) generalized bell, (f) sigmoid right, (g), sigmoid left, (h) Difference sigmoid, (i) Product-sigmoid, (j) Polynomial-Z, (k) Polynomial-Pi, (l) Polynomial-S

A singleton is a special type of MF that has a value of 1 at one point in the universe of discourse and zero elsewhere (a vertical spike). MFs can be represented by mathematical functions, segmented straight lines (for triangular and trapezoidal shapes), and look-up tables [41-45, 65-75].

2.2.3 Operations of Type-1 Fuzzy Sets

The basic properties of Boolean logic are also valid for FL. Fig. 2.3 shows the logical operations OR, AND, and NOT on fuzzy sets *A* and *B* using triangular MFs and compares them with the corresponding Boolean operations on the right. Let $\mu_A(x)$, $\mu_B(x)$ denote the degree of membership of a given element x in the universe of discourse X (denoted by $x \in X$).

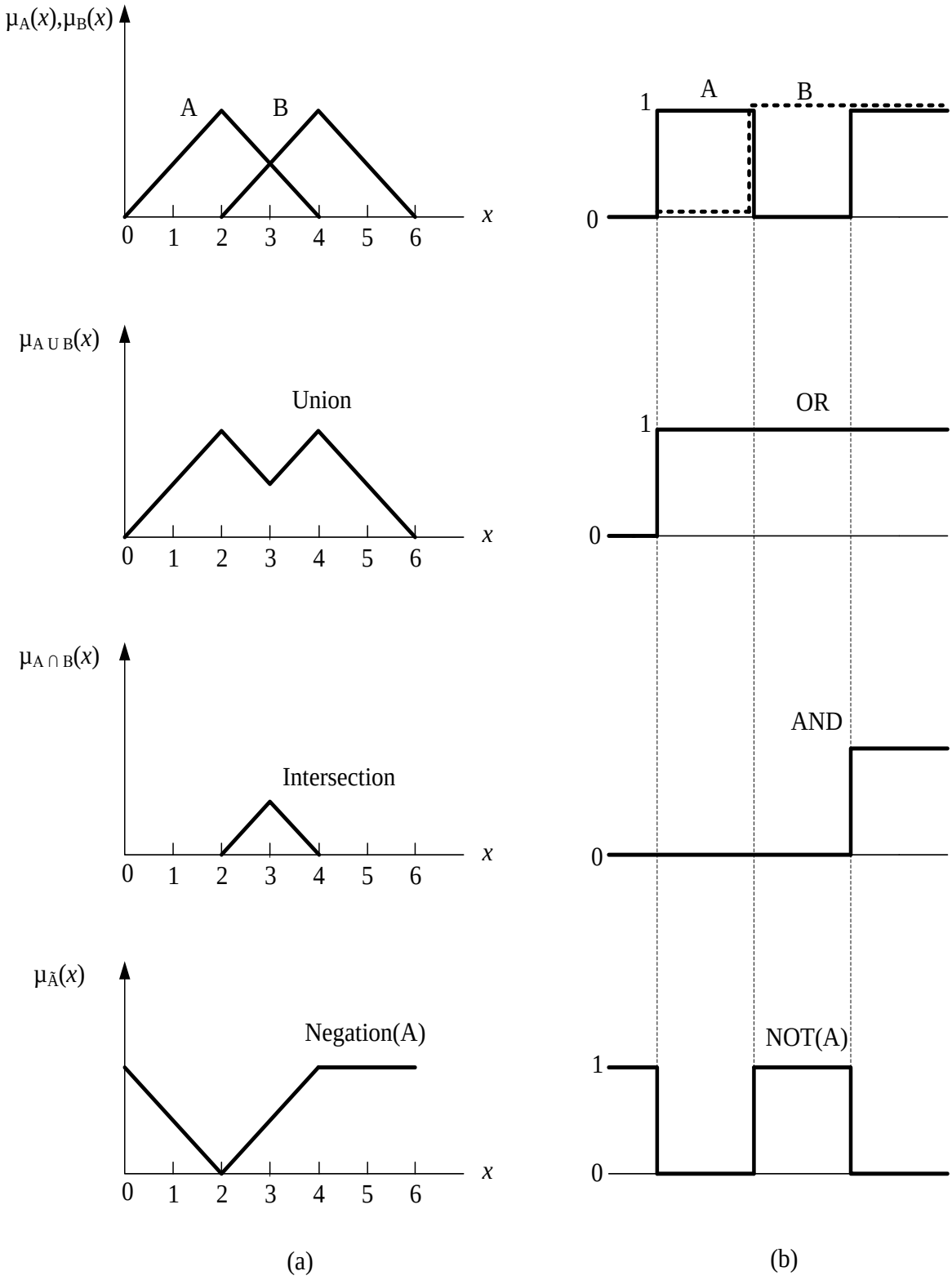


Fig. 2.3: Logical operation of (a) fuzzy sets, (b) Crisp sets

Union: Given two fuzzy sets A and B defined in the universe of discourse X, the union ($A \cup B$) is also a fuzzy set of X, with the MF given as [70]

$$\mu_{A\cup B}(x) = max\left[\mu_A(x), \mu_B(x)\right] = \mu_A(x) \vee \mu_B(x) \quad (2.1)$$

where the symbol "$\vee$" is a maximum operator. This is equivalent to Boolean OR logic.

Intersection: The intersection of two fuzzy sets A and B in the universe of discourse X denoted by $A \cap B$, has the MF given by [81- 82]

$$\mu_{A\cap B}(x) = min\left[\mu_A(x), \mu_B(x)\right] = \mu_A(x) \wedge \mu_B(x) \quad (2.2)$$

where "$\wedge$" is a minimum operator. This is equivalent to Boolean AND logic.

Complement or Negation: The complement of a given set A in the universe of discourse X is denoted by $\overline{A}$ and has the MF [40-44]

$$\mu_{\overline{A}}(x) = 1 - \mu_A(x) \quad (2.3)$$

This is equivalent to the NOT operation in Boolean logic. In FL, we can also define the following operations:

Product of two fuzzy sets: The product of two fuzzy sets A and B defined in the same universe of discourse X is a new fuzzy set, $A.B$, with an MF that equals the algebraic product of the MFs of A and B [70]

$$\mu_{A.B}(x) = \mu_A(x).\mu_B(x) \quad (2.4)$$

which can be generalized to any number of fuzzy sets in the same universe of discourse.

Multiplying Fuzzy Set by a Crisp Number: The MF of fuzzy set A can be multiplied by a crisp number k to obtain a new fuzzy set called product $k.A$. Its MF is [44]

$$\mu_{kA}(x) = k.\mu_A(x) \quad (2.5)$$

Power of a Fuzzy Set: We can raise fuzzy set A to a power m (positive real number) by raising its MF topower m. The m^{th} power of A is a new fuzzy set A^m, with MF [70]

$$\mu_{A^m}(x) = \left[\mu_{A^n}(x)\right]^m \quad (2.6)$$

Fuzzy set properties, as discussed above, are useful in performing additional operations using fuzzy sets. Consider the fuzzy sets A, B, and C defined over a common universe of discourse X. The following properties are valid for crisp and fuzzy sets. But some are more specific to fuzzy sets [71-85].

Double Negation [68-70]**:**

$$\overline{(\overline{A})} = A \tag{2.7}$$

Idempotency [44]**:**

$$A \cap A = A \tag{2.8}$$

$$A \cup A = A$$

Commutativity [40]**:**

$$A \cap B = B \cap A \tag{2.9}$$

$$A \cup B = B \cup A$$

Associative Property [70]:

$$A \cup (B \cup C) = (A \cup B) \cup C \tag{2.10}$$

$$A \cap (B \cap C) = (A \cap B) \cap C$$

Distributive Property [70]**:**

$$A \cup (B \cap C) = (A \cup B) \cap (A \cup C) \tag{2.11}$$

$$A \cap (B \cup C) = (A \cap B) \cup (A \cap C)$$

Absorption [70]**:**

$$A \cap (A \cap B) = A \tag{2.12}$$

$$A \cup (A \cap B) = A$$

De Morgan's Theorems [69-70]**:**

$$\overline{A \cup B} = \overline{A} \cap \overline{B} \tag{2.13}$$

$$\overline{A \cap B} = \overline{A} \cup \overline{B}$$

In fuzzy sets, all these properties can be expressed using the MF of the sets involved and the basic definition of union, intersection, and complement. For example, the distributive property in Eqn. (2.11) can be written as [44-60]

$$\begin{aligned} \mu_A(x) \vee \left(\mu_B(x) \wedge \mu_C(x)\right) &= \left(\mu_A(x) \vee \mu_B(x)\right) \wedge \left(\mu_A(x) \vee \mu_C(x)\right) \\ \mu_A(x) \wedge \left(\mu_B(x) \vee \mu_C(x)\right) &= \left(\mu_A(x) \wedge \mu_B(x)\right) \vee \left(\mu_A(x) \wedge \mu_C(x)\right) \end{aligned} \tag{2.14}$$

Similarly, the De Morgan's theorems in (2.13) can be written in the form [70]

$$\overline{\mu_A(x) \vee \mu_B(x)} = \overline{\mu_A}(x) \wedge \overline{\mu_B}(x)$$
$$\overline{\mu_A(x) \wedge \mu_B(x)} = \overline{\mu_A}(x) \vee \overline{\mu_B}(x) \quad (2.15)$$

The inference systems are mainly classified into three types such as Mamdani, Sugeno, and Tsukamoto. However, the Mamdani type is most preferred due to its simplicity and easier implementation than Sugeno and Tsukamanto [48-60].

2.2.4 Mamdani type-1 Fuzzy Logic Inference System

A Mamdani type of T1FLC consists of four main parts as shown in Fig. 2.4, which are:

- Fuzzifier
- Knowledge Base
- Inference Engine
- Defuzzifier

A Fuzzifier performs measurement of the input variables, scale mapping, and fuzzification. After measuring all input variables, the crisp input quantities are transformed into fuzzy quantities, which are also known as linguistic variables. This transformation is studied with the MFs. In T1FLC, the number of MFs and shape of the MFs are determined by the user's/expertise [40, 44, 70, 82, 107].

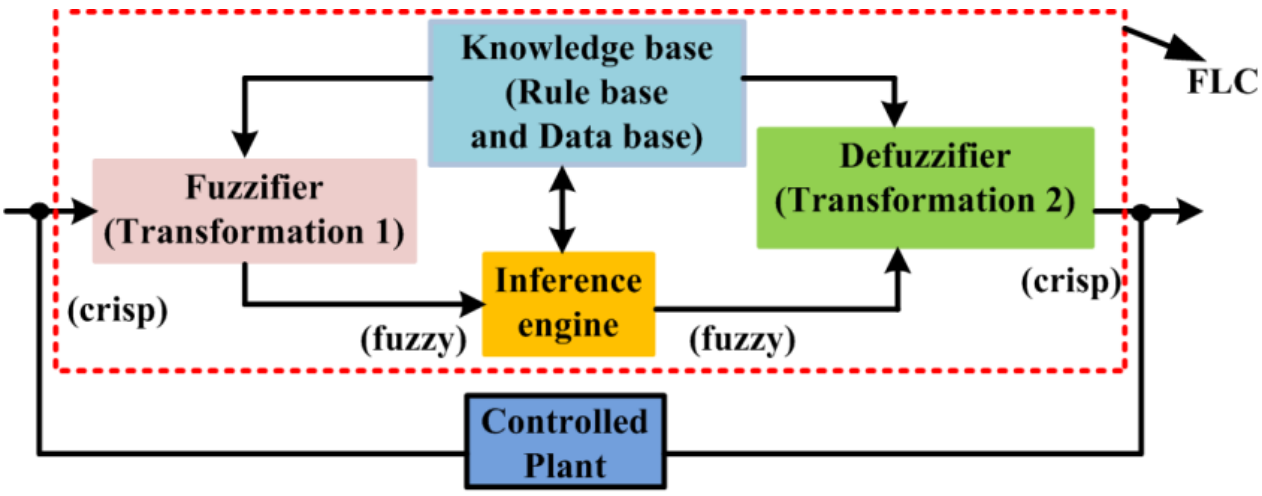


Fig. 2.4: Block diagram for T1FLC

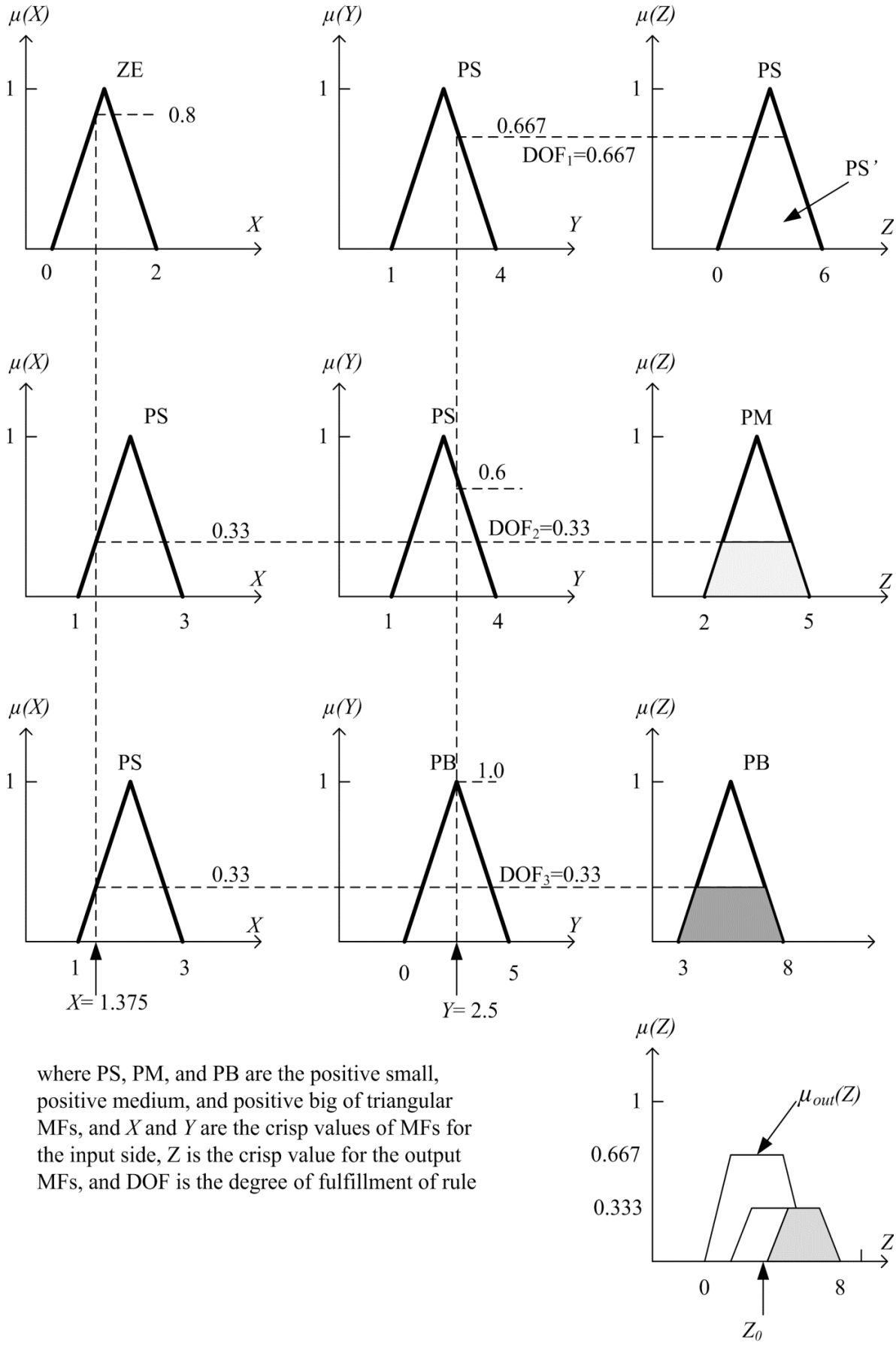


Fig. 2.5: Three-rules for Mamdani type-1 fuzzy system

The knowledge base consists of the database and the linguistic control rule base. The database provides the information that is used to define the linguistic control rules and fuzzy data manipulation in the T1FLC. The rule base (expert rules) specifies the control goal action by means of a set of linguistic control rules. The T1FLC has input and output signals. However, an appropriate output signals are determined by using the expert rules [14] -[17]. Moreover, the main schemes of developing the rule base are [40, 82, 107-110]:

- Using the experience and knowledge of an expert for the application and the control goals
- Modeling the control action of the operator
- Modeling the process using a self organized fuzzy controller
- Removal of any significant errors in the process output by suitable adjustment of control output
- Ensuring a smooth control action near the reference value
- Preventing the process output exceeding user specified values

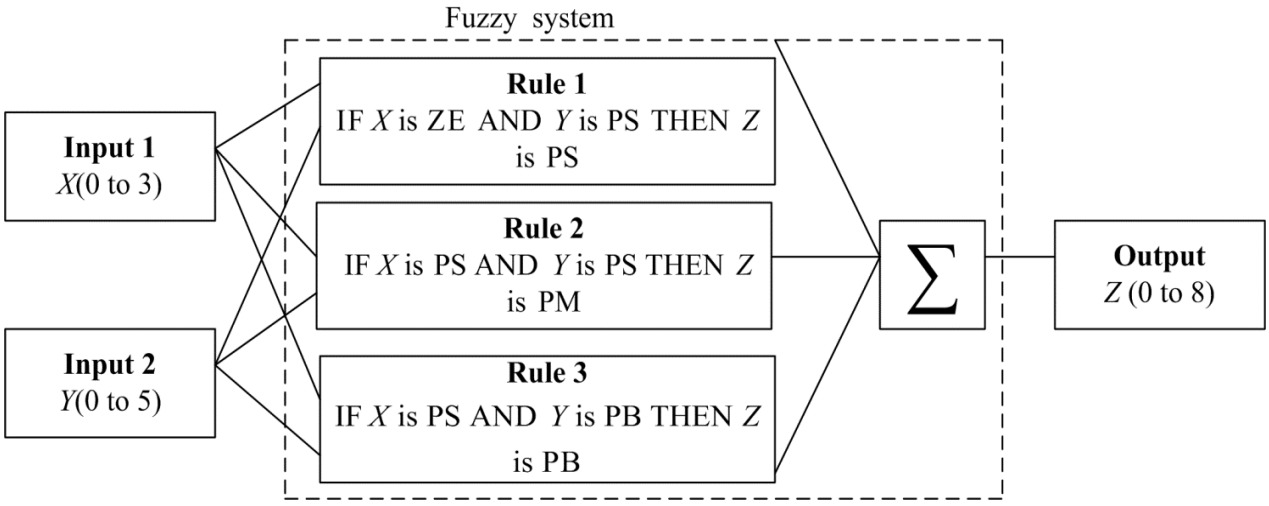


Fig. 2.6: Fuzzy inference system for Mamdani T1FLC

The inference engine (reasoning mechanism) is the kernel of T1FLC and it has the capability of both simulating human decision making based on fuzzy concepts and inferring fuzzy control actions using fuzzy implication and fuzzy logic rules of inference. In other words, once all the monitored input variables are transferred into their respective linguistic variables, the inference engine evaluates the set of IF-THEN rules (given in the rule base), which is aged a linguistic value for the linguistic variable. The linguistic result

is transformed into a crisp output value of FLC and that is why there is a second transformation (defuzzifier) [70-75, 140].

Let consider the three rules in a fuzzy system, which are in general form as given in Fig. 2.5 and the input and output ranges along with IF-THEN rules are given in Fig. 2.6. The fuzzy inference system with the Mamdani method for inputs $X = 1.375$ and $Y = 2.5$. Note that all the rules have an AND operator. From the Fig. 2.5, the degree of fulfillment (DOF) for Rule 1 can be given as

$$DOF_1 = \mu_{ZE}(X) \wedge \mu_{PS}(Y) = 0.8 \wedge 0.667 = 0.667 \tag{2.16}$$

Where /\ is minimum operator and μ_{ZE} *(X)* and μ_{PS} *(Y)* are the MFs of *X* and *Y*, respectively. The rule output is given by the truncated MF PS' as shown in the Fig. 2.5. Similarly, for Rules 2 and 3 can be written as

$$DOF_3 = \mu_{PS}(X) \wedge \mu_{PS}(Y) = 0.333 \wedge 0.6 = 0.333 \tag{2.17}$$

$$DOF_3 = \mu_{PS}(X) \wedge \mu_{PB}(Y) = 0.333 \wedge 1.0 = 0.333 \tag{2.18}$$

The corresponding fuzzy output MFs are PM and PB, respectively, as indicated in Fig. 2.5. The total fuzzy output is the union (OR) of the entire component MFs.

$$\mu_{out}(Z) = \mu_{PS}(Z) \vee \mu_{PM}(Z) \vee \mu_{PB}(Z) \tag{2.19}$$

which is shown in the lower right part of the Fig. 2.5. The defuzzification to convert the fuzzy output to crisp output will be discussed later.

The defuzzifier performs scaling and mapping as well as defuzzification, and it yields a non-fuzzy, crisp control action from the inferred fuzzy control action and consequent MFs of the rules. There are many defuzzification techniques such as maximum, minimum, and centroid etc.; among these methods the centroid method is used in the present work to find the crisp value [40, 44-45, 80-82].

2.2.5 Center of Area or Centroid Method for T1FLC

The Center of Area (COA) method is often called as the center of gravity method, which is used in defuzzification process. The crisp output Z_0 is taken to be the geometric center of the output fuzzy value $\mu_{out}(Z)$ area, where $\mu_{out}(Z)$ is formed by taking the union of all the contributions of rules whose DOF> 0 (for example, the lower right part of Fig. 2.5).

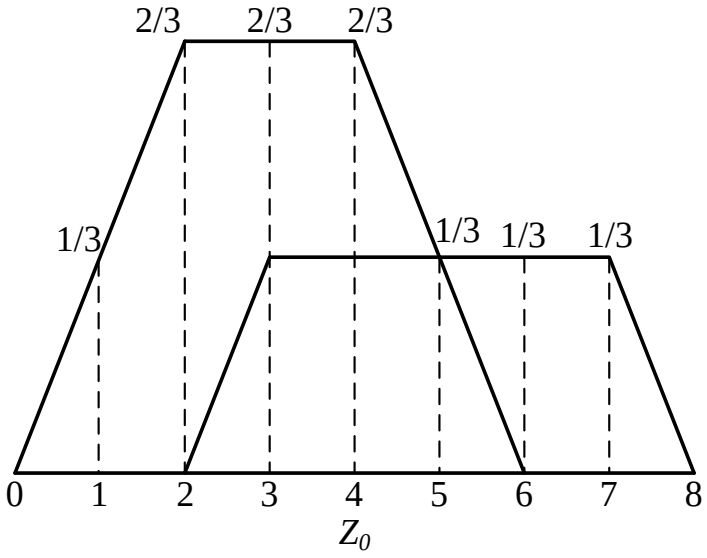


Fig. 2.7: Defuzzification of output for overall MF

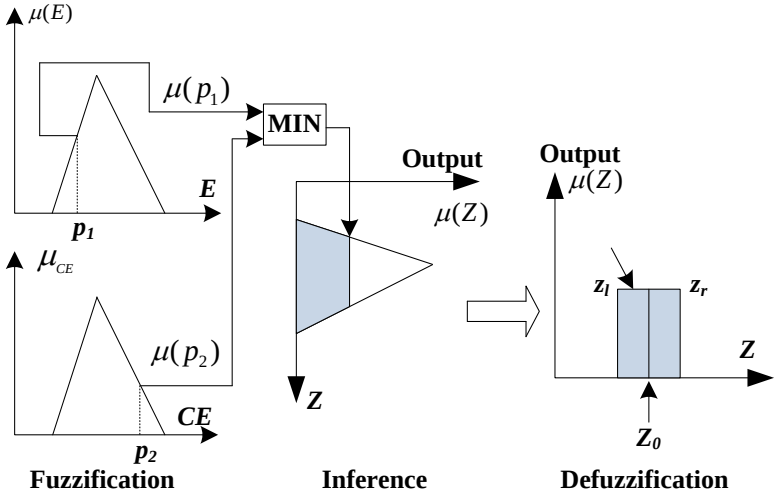


Fig. 2.8: T1FLC process for two inputs and single output MF

The general expression for COA defuzzification is [70-80]

$$Z_0 = \frac{\int Z.\mu_{out}(Z)}{\int \mu_{out}(Z)dZ} \tag{2.20}$$

With a discretized universe of discourse, the expression is [70, 82]

$$Z_0 = \frac{\sum_{i=1}^{n} Z_i.\mu_{out}(Z_i)}{\sum_{i=1}^{n} \mu_{out}(Z_i)} \tag{2.21}$$

where $\mu_{out}(Z)$ and n are the aggregated output MF and the number of samples, respectively. From Fig. 2.5, the overall MF can be found for three rule system in which the overall MF can be sampled by eight times as shown in Fig. 2.7 and hence the COA can be found from overall MF as

$$Z_0 = \frac{1.\frac{1}{3} + 2.\frac{2}{3} + 3.\frac{2}{3} + 4.\frac{2}{3} + 5.\frac{1}{3} + 6.\frac{1}{3} + 7.\frac{1}{3}}{\frac{1}{3} + \frac{2}{3} + \frac{2}{3} + \frac{1}{3} + \frac{1}{3} + \frac{1}{3} + \frac{1}{3}} = 3.7 \tag{2.22}$$

COA is a well known method and it is often used in spite of any amount of complexity in the calculation. Note that if the area of two or more contributing rules overlap, the overlapping area is counted once, which should be evident from Fig. 2.7. The overall operation of T1FLC for two inputs of E and CE and single output as shown in Fig. 2.8 in which the output at corresponding position p_1 and p_2 is selected for minimum product along with defuzzification process [70, 82].

The T1FLC has been widely applied in power electronic systems, applications include speed control of DC and AC drives, feedback control of the converter, off-line P-I and P-I-D tuning, nonlinearity compensation, on-line and off-line diagnostics, modeling, parameter estimation, performance optimization of drive systems based on on-line search, estimation for distorted waves, and so on [65-80].

2.3 Motivation of Type-2 Fuzzy System

A type-1 fuzzy system can utilize the human expertise by sorting its essential components in rule base and data base to perform fuzzy reasoning to infer the overall output value. The derivation of fuzzy rules and the corresponding MFs depends heavily on the prior knowledge about the system under consideration. There are two basic issues concerning the preparation and manipulation of knowledge. Firstly, there exists a systematic way to transform experiences or knowledge of human experts in to the knowledge base of a type-1 fuzzy inference system with two dimensional control only. Secondly, there is still a need of adaptability or learning algorithms to tune the MFs so as to minimize the large footprint of the uncertainty of controller and hence the discrepancy between the model (calculated) output and desired output can be reduced [61, 70, 107, 108]. These two problems greatly

restrict the application of fuzzy systems, either a controller or an expert system. Also, the transition from ordinary sets to fuzzy sets where it cannot determine the membership of an element is either set at zero or one using type-1 fuzzy sets. Similarly, when the circumstances are too fuzzified and it is troublesome to determine the membership grade even as the crisp value between zero and one [108].

To a large extent, the drawbacks of pertaining to this scheme seem to be complementary. Therefore, it seems natural to consider building an integrated system combining the concepts of T1FLC modeling and reduced type-2 fuzzy set. In other words, the integrated approach, or type-2 fuzzy modeling should incorporate the three most important features [143-152]:

1. Meaningful and concise representation of structured knowledge.
2. The efficient learning capability to identify parameters from the large footprint of uncertainty.
3. Clear mapping between parameters and structured knowledge with the 3-dimensional control.

2.3.1 Type-2 Fuzzy Control (T2FLC)

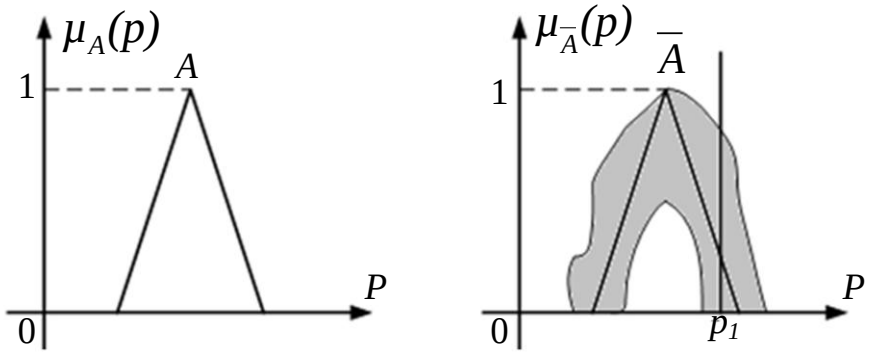
A type-2 MF is actually a 3-dimensional MF that describes a type-2 fuzzy set. Fig. 2.9 (a) and Fig. 2.9 (b) show the type-1 MF and shaded type-1 MF, which is obtained by shifting the points to left or right, but not necessarily by the same amount of the type-1 MF, in which 'p' is the crisp value of torque (speed) and p_1 is the particular position of torque (speed). However, the MF is not a crisp value anymore, instead it chooses many values wherever the vertical line crosses the shade. The type-2 fuzzy set denoted $\bar{A}$ is described by a type-2 MF $\mu_{\bar{A}}(p,u)$ where $p \epsilon P$ and $u \epsilon J_p \subseteq [0,1]$ that is [143]

$$\bar{A} = \{(p,u), \mu_{\bar{A}}(p,u)\} \tag{2.23}$$

In which $0 \leq \mu_{\bar{A}}(p,u) \leq 1$. The $\bar{A}$ can also be expressed as

$$\bar{A} = \int_{p \in P} \int_{u \in J_p} \frac{\mu_{\bar{A}}(p,u)}{(p,u)} \tag{2.24}$$

where $\iint$ denotes union over all admissible p and u



(a) (b)

Fig. 2.9: Development of type-2 MF (a) Type-1 MF (b) Shaded type-2 MF

At each value of p, let $p=p_1$ the 2-dimensional plane whose axes u and $\mu_{\bar{A}}(p_1,u)$ are called as vertical slice of $\mu_{\bar{A}}(p,u)$. It is $\mu_{\bar{A}}(p=p_1,u)$ for $p_1 \in P$ and $\forall u \in J_p \subseteq [0,1]$ that is

$$\mu_{\bar{A}}(p=p_1,u) \equiv \mu_{\bar{A}}(p_1) = \int_{u \in J_{p1}} \frac{f_{p_1}(u)}{u} \tag{2.25}$$

In which $0 \leq f_{p_1}(u) \leq 1$, because $p_1 \in P$, 1 is dropped on $\mu_{\bar{A}}(p_1)$ and it is referred to $\mu_{\bar{A}}(p)$ as a secondary MF is a type-1 fuzzy set, which is also mentioned to secondary set. The type-2 fuzzy set can be expressed as the union of all secondary set that is used in Eq. (2.25). Hence, the $\bar{A}$ in a vertical-slice manner can be re-expressed as [107-108]

$$\bar{A} = \{p, \mu_{\bar{A}}(p)\} \tag{2.26}$$

or

$$\bar{A} \equiv \int_{p \in P} \frac{\mu_{\bar{A}}(p)}{p} = \int_{p \in P} \frac{\int_{u \in J_p} f_p(u)/u}{p} \tag{2.27}$$

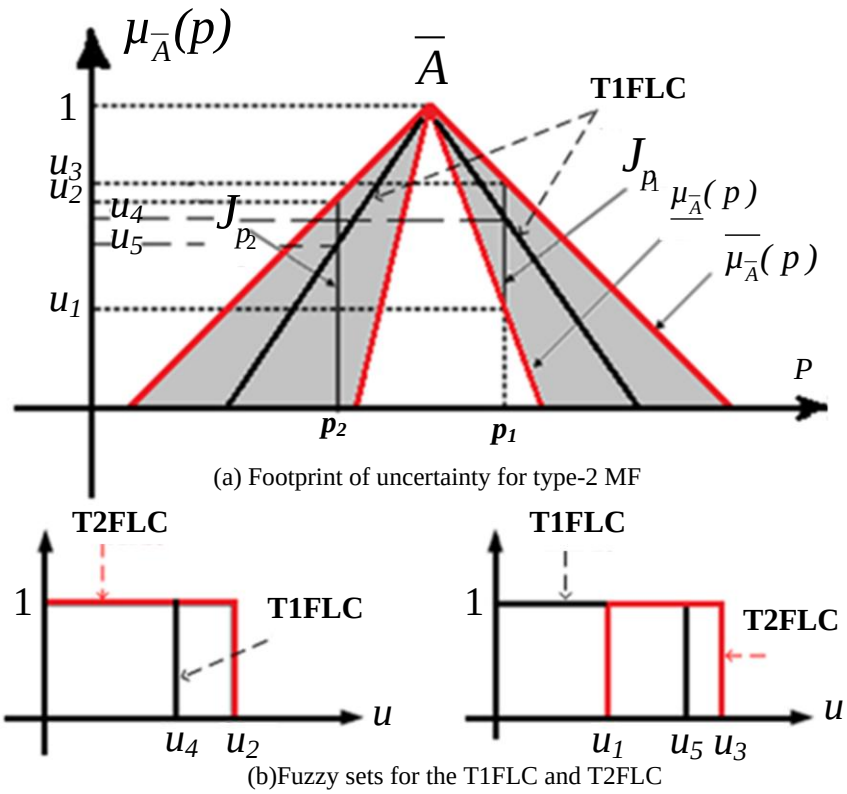
When $f_p(u)=1, \forall u \in J_p \subseteq [0,1]$ then the secondary MFs are interval sets. Hence, if this is true $\forall p \in P$ an interval type-2 MF is obtained. The interval secondary MF reflects a uniform uncertainty at the primary memberships of p. The uncertainty in the primary memberships of a type-2 fuzzy set $\bar{A}$ consists of a bounded region that is known as the footprint of uncertainty (II). It is as the union of all primary memberships, that is

$$\Pi(\bar{A}) = \bigcup_{p \in P} J_p \tag{2.28}$$

The upper and the lower MFs are two type-1 MFs that are bound for the footprint of uncertainty of a type-2 fuzzy set $\bar{A}$ [107-110]. The upper MF is associated with upper bound by $\overline{\Pi(\bar{A})}$, and it is denoted as $\overline{\mu_{\bar{A}}(p)}, \forall p \in P$. The lower MF is associated with lower bound off $\underline{\Pi(\bar{A})}$, and it is denoted as $\underline{\mu_{\bar{A}}}(p), \forall p \in P$, that is

$$\overline{\mu_{\bar{A}}}(p) = \overline{\Pi(\bar{A})} \tag{2.29}$$

$$\underline{\mu_{\bar{A}}}(p) = \underline{\Pi(\bar{A})} \tag{2.30}$$



(a) Footprint of uncertainty for type-2 MF

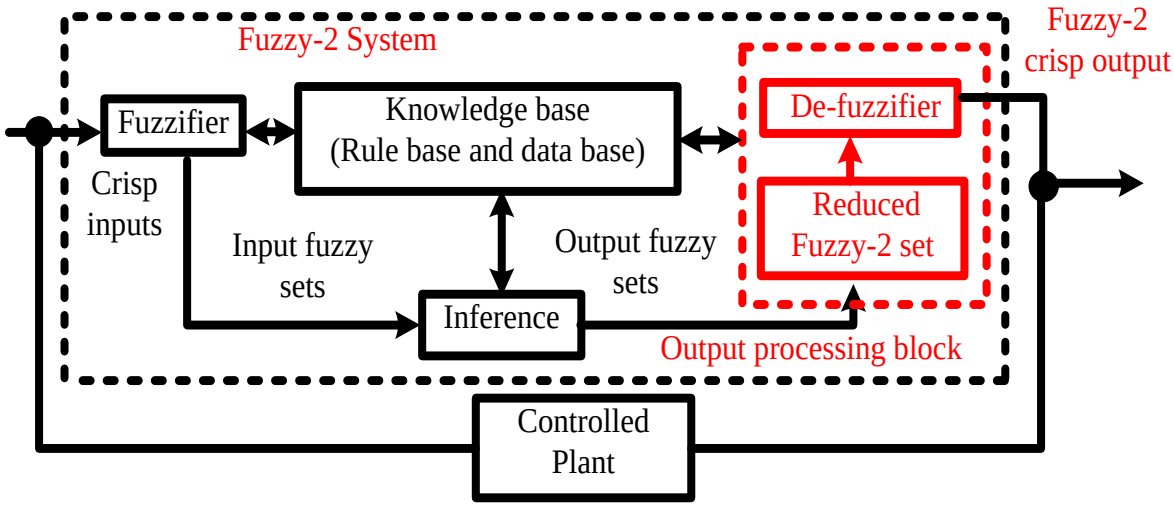
(b)Fuzzy sets for the T1FLC and T2FLC

Fig. 2.10: Type-2 fuzzy sets for the corresponding positions p_1 and p_2 for T1FLC and T2FLC

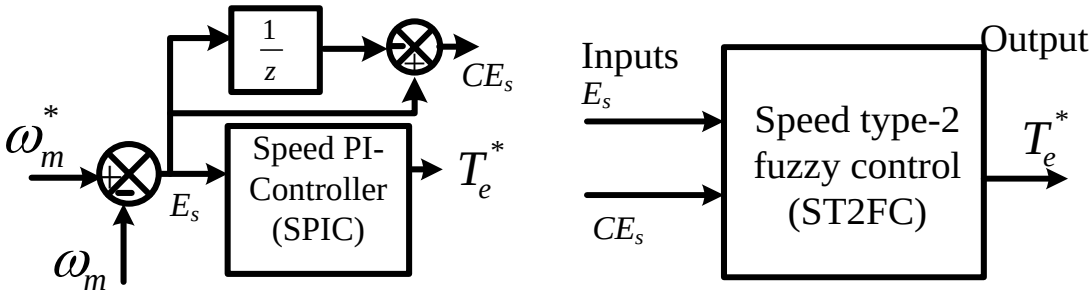
The secondary MF with Eq. (2.23) is carried out by existing lower and upper MFs, which is varied from zero to one. The blurred area of the footprint of uncertainty for a type-2 fuzzy set is shown in Fig. 2.10. The primary memberships J_{p1} and J_{p2}, and their associated secondary MFs are $\mu_{\bar{A}}(p_1)$ and $\mu_{\bar{A}}(p_2)$ as shown in Fig. 2.10 (a) at points p_1 and p_2. The upper and lower MFs are $\overline{\mu_{\bar{A}}}(p)$ and $\underline{\mu_{\bar{A}}}(p)$, respectively. The secondary MFs have the interval sets as shown in Fig. 2.10 (b). The different types of MFs and operating principles for T2FLC remain same as the T1FLC which is explained in Chapter 2.2.2 and

Chapter 2.2.3, respectively. However, the MF for T2FLC is represented as two MF instead of single MF as compared to T1FLC [140-165].

The block diagram for type-2 fuzzy logic system (T2FLS) is shown in Fig. 2.11(a) in which it is clearly mentioned that the control algorithm for T2FLC has both fuzzification and defuzzification process, which is similar to T1FLC. The main difference with the T2FLS is the output processing block as compared to T1FLS in which it includes the type reduction followed by defuzzification [140, 150-160]. Consequently, the output crisp value is generated by type-2 reduced fuzzy set or type-1 fuzzy set during the defuzzification process. While developing the control system, all consequent and antecedent parameters are assumed to be a type-2 fuzzy set. Moreover, the Mamdani type fuzzy and Centroid method are used to control the crisp output of overall MF using simple logical rules such as IF, THEN, AND, OR, and NOT etc. The design procedure for T2FLC using speed PI-controller (SPIC) by two inputs with a single output controller is followed as shown in Fig. 2.11(b).



(a) Block diagram for T2FLC



(b) E_S and CE_S are found from SPIC (c) Input and output of ST2FC

Fig. 2.11: Design procedure for T2FLC

From the speed PI-control (SPIC), the output of the SPIC is given as [27]:

$$T_e^* = k_{ps} e_s^*(t) + k_{is} \int e_s^*(t) dt \tag{2.31}$$

where k_{ps} and k_{is} are the proportional and integral gains of the SPIC, $e_s^*(t)$ is the error of SPIC. Differentiating on both sides of (2.31) gives

$$\frac{dT_e^*}{dt} = K_{ps} \frac{de_s^*(t)}{dt} + K_{is} e_s^*(t) \tag{2.32}$$

From (2.32), it is clear that the change of the torque is directly proportional to the inputs of the SPIC, *i.e.*, error (E_s *(k)*) and change of the error (CE_s *(k)*) [24]-[27] as shown in Fig. 2.11(c), and they have expressed as

$$E_s(k) = \omega_m^*(k) - \omega_m(k) \tag{2.33}$$

$$CE_s(k) = E_s(k) - E_s(k-1) \tag{2.34}$$

where, ω_r^**(k)* and ω_r *(k)* are the reference and the actual rotor speed of the motor, and E_s *(k)* and E_s *(k-1)* are the present and previous speed errors, respectively.

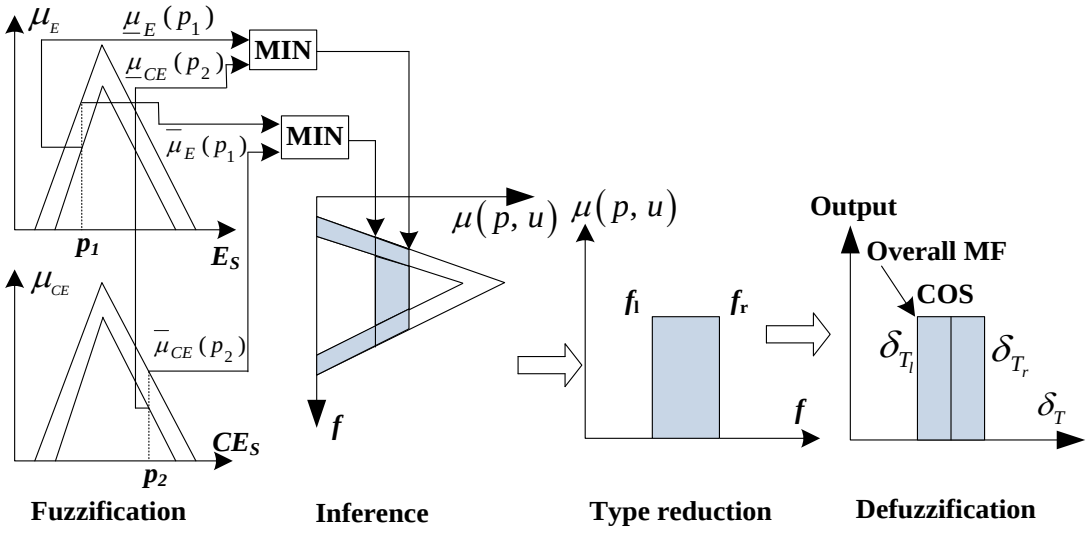


Fig. 2.12: T2FLC process for the corresponding input (E_S and CE_S) and output MFs

When a change of torque $\Delta T_e^*(k)$ is obtained, then the output of SPIC is [106-112]

$$T_e^*(k) = T_e^*(k-1) + \Delta T_e^*(k) \tag{2.35}$$

Where $T_e^*(k-1)$ is the previous value of estimated torque value of the speed type-2 fuzzy control (ST2FC). The ST2FC has input and output as shown in Fig. 2.11(c), where the input MFs (E_s*(k)* and CE_s*(k)*) have *'M'* number of MFs and the output MFs have *'N'* number of MFs and hence the total number of rules required will be ($M \times N$). Moreover, Fig. 2.12 shows the overall operation of T2FLC in which COS is the center of sets for the

output of overall MF during the defuzzification process in which each rule has the following form as

IF E_s is $\tilde{G}^{i}_{E_s}$ and CE_s is $\tilde{G}^{i}_{CE_s}$ THEN δ_T is (y^{i}_{l}, y^{i}_{r}) (2.36)

where i=1, 2…,M rules, $\tilde{G}^{i}_{E_s}$ and $\tilde{G}^{i}_{CE_s}$ are the fuzzy sets of the IF-ingredients, y^{i}_{l} and y^{i}_{r} are the singleton left and right side of THEN-ingredients. The MFs of IF and THEN parts are the input and output side of the ST2FC, respectively.

2.3.2 Type-Reduction and Defuzzification

When the antecedent and consequent MFs of T2FLS have continuous domains, the number of embedded sets is un-countable as shown in Fig. 2.13 in which x is the input and the y is the aggregated crisp output. Fig. 2.13 has been drawn assuming that the MFs have discrete domains to n number of values [105-112]. The memberships in the type-reduced set $\mu_Y(y_n)$ represent the level of uncertainty associated with each embedded T1FLS. A crisp output can be obtained by aggregating the outputs of all the embedded T1FLS after finding the centroids of the type-reduced set.

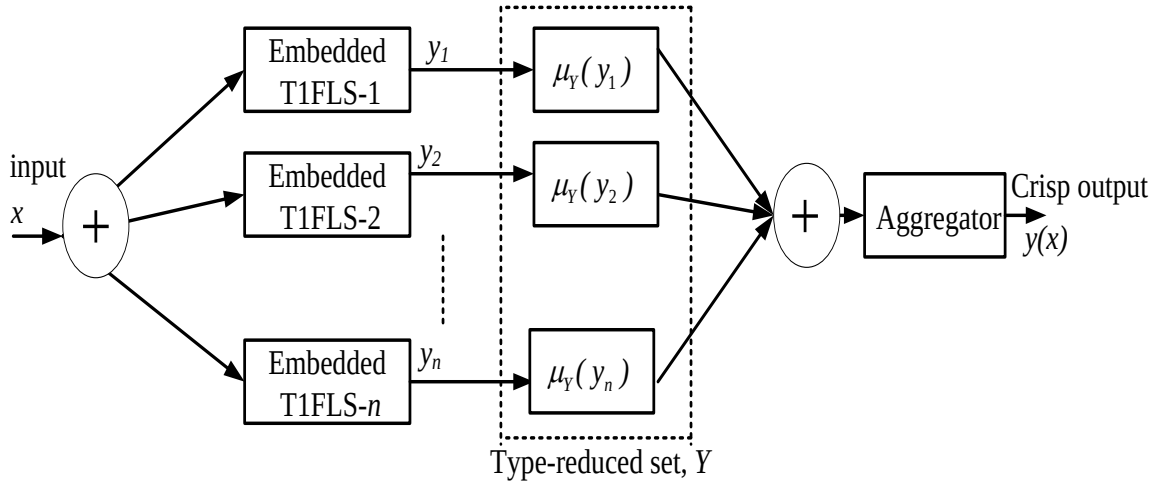


Fig. 2.13: T2FLS can be thought of as collection of a large number of embedded T1FLSs

From Fig. 2.11(a) and Fig. 2.12, it is observed that a singleton T2FLS is a mapping. After fuzzification, fuzzy inference, type reduction and defuzzification, a crisp output isobtained. The T2FLC values of the i^{th} rule can be obtained as:

$$F^{i} = \left(\underline{f}^{i}, \overline{f}^{i}\right) \tag{2.37}$$

where

$$\underline{f}^{i} = \underline{\mu}_{\tilde{G}^{i}_{E_s}}(E_s, u) * \underline{\mu}_{\tilde{G}^{i}_{CE_s}}(CE_s, u) \tag{2.38}$$

$$\overline{f}^{i} = \overline{\mu}_{\tilde{G}^{i}_{E_s}}(E_s, u) * \overline{\mu}_{\tilde{G}^{i}_{CE_s}}(CE_s, u)$$

(2.39)

where $\underline{\mu}_{\tilde{G}^{i}_{E_s}}$ and $\overline{\mu}_{\tilde{G}^{i}_{CE_s}}$ are grades of the lower and the upper MFs, respectively.

The interval singleton T2FLS uses either minimum or product t-norm, the result of input and antecedent operations is an interval type-1 set and the firing interval, which is determined by its left and right most points f_l^i and f_r^i, respectively [107]. A singleton fuzzification with a minimum t-norm is used and later, the output can be expressed as:

$$\delta_{T_{\cos}} = \left[\delta_{T_l}, \delta_{T_r} \right] \tag{2.40}$$

where $\delta_{T_{\cos}}$ is an interval of type-2 fuzzy set determined by the left and right end points ($\delta_{T_l}, \delta_{T_r}$), which can be derived from the consequent centroid set (y_l^i, y_r^i) [150-151]. The torque strength $\underline{f}^i \in F^i = \left(\underline{f}^i, \overline{f}^i \right)$ must be computed or set first before the computation of $\delta_{T_{\cos}}$. The leftmost point δ_{T_l} and the rightmost point δ_{T_r} can be expressed as [150-153]:

$$\delta_{T_l} = y_l = \sum_{i=1}^{M} \left[f_l^i y_l^i \right] \Big/ \sum_{i=1}^{M} f_l^i \tag{2.41}$$

$$\delta_{T_r} = y_r = \sum_{i=1}^{M} \left[f_r^i y_r^i \right] \Big/ \sum_{i=1}^{M} f_r^i \tag{2.42}$$

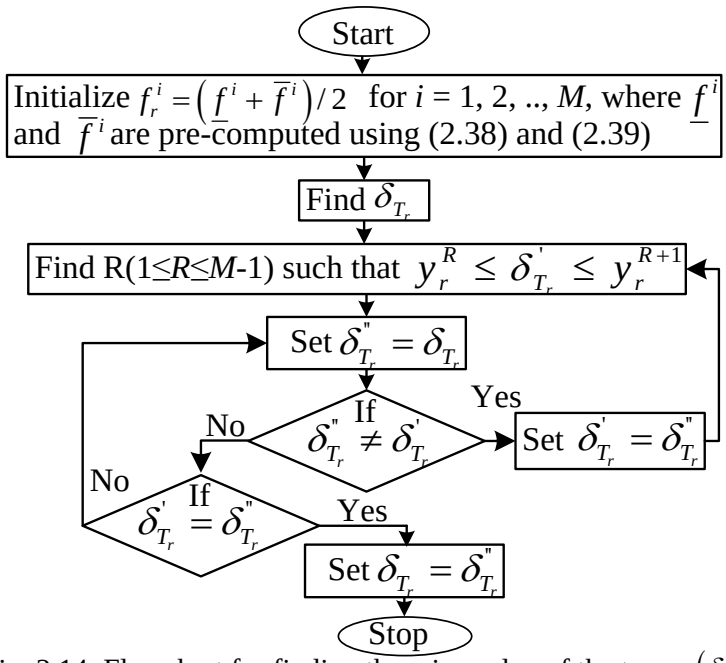


Fig. 2.14: Flowchart for finding the crisp value of the torque $\left(\delta_{T_r} \right)$

The procedure to compute δ_{T_l} and δ_{T_r} is that let first compute the rightmost point δ_{T_r} without loss of generality; assume that y_r^i is arranged in ascending order, *i.e.*, $y_r^1 \le y_r^2 \le \ldots \le y_r^M$. The algorithm for finding crisp output on the right side of T2FLC is shown in Fig. 2.14. Hence, δ_{T_r} in (2.42) can be re-expressed as [106-126, 151]:

$$\begin{aligned}\delta_{T_r} &= \delta_{T_r}\left(\underline{f}^1,\ldots,\underline{f}^R,\overline{f}^{R+1},\ldots,\overline{f}^M,y_r^1,\ldots,y_r^M\right)\\ &= \left[\sum_{i=1}^{R}\underline{f}^i y_r^i+\sum_{i=R+1}^{M}\overline{f}^i y_r^i\right]\Big/\left[\sum_{i=1}^{R}\underline{f}^i+\sum_{i=R+1}^{M}\overline{f}^i\right]\end{aligned} \tag{2.43}$$

The procedure to compute δ_{T_l} is similar to that of δ_{T_r} (as shown in Fig. 2.14) with slight modifications. In 3rd step of the Fig. 2.14, find L ($1 \le L \le M-1$) such that $y_l^L \le \delta_{T_l}^{'} \le y_l^{L+1}$, and allow $f_l^i = \overline{f}^i$ for $i \le L$ and $f_r^i = \underline{f}^i$ for $i > L$. Therefore δ_{T_l} can be expressed using (2.43) as [32]-[35]:

$$\begin{aligned}\delta_{T_l} &= \delta_{T_l}\left(\overline{f}^1,\ldots,\overline{f}^L,\underline{f}^{L+1},\ldots,\underline{f}^M,y_l^1,\ldots,y_l^M\right)\\ &= \left[\sum_{i=1}^{L}\overline{f}^i y_l^i+\sum_{i=L+1}^{M}\underline{f}^i y_l^i\right]\Big/\left[\sum_{i=1}^{L}\overline{f}^i+\sum_{i=L+1}^{M}\underline{f}^i\right]\end{aligned} \tag{2.44}$$

The defuzzified crisp output from an interval type-2 fuzzy system is the average or centre of sets of δ_{T_r} and δ_{T_l} as

$$\delta_{T_{ec}} = \left(\delta_{T_r}+\delta_{T_l}\right)\Big/2 \tag{2.45}$$

The T2FLS provides different values of input fuzzy sets and crisp values for the corresponding MFs, which are closed to actual values from the large uncertainty data over a T1FLCS [40, 107, 151]. Therefore, the output performance of the controller (ST2FC) should be improved due to the actual crisp value in the output side, which implies that the dynamic performance of the controller will be improved for the huge ambiguous data than T1FLC and conventional PIC (SPIC). The detail comparative performance of an IM for the direct torque control can be studied later.

2.4 Summary

Artificial intelligent controllers such as type-1 and type-2 fuzzy logic control (T2FLC) are reviewed. The design procedure for both T1FLC and T2FLC are explained and compared with examples in detail. An expertise is also required to select the MFs and to frame the rules as per the personal experience in both T1FLC and T2FLC. A Mamdani type and centroid method is used in both the artificial intelligent schemes, because of the simplicity, and easy to implement without required complex equations, and provides a robust performance for both linear and nonlinear control systems. However, the T1FLC cannot effectively handle with the large footprint of uncertainty than T2FLC. The success is mostly due to the fact that the type-2 fuzzy controllers are suited well for capturing the imprecise nature of the human knowledge and reasoning processes. Also, the T2FLC has three-dimensional control and provides type-2 reduced fuzzy set during the defuzzification process. Whereas in T1FLC consists of a single membership function (MF) and two-dimensional control and there is no type reduction.

CHAPTER - 3
DIRECT TORQUE CONTROL FOR TWO-LEVEL VSI FED IM DRIVE

3.1 Introduction

The conventional direct torque control (CDTC) was developed for getting quick dynamic response of the IM using switching table and without requiring any transformation [4-6]. Here, the torque and flux are controlled independently using hysteresis control. However, the hysteresis control gives considerable flux and torque ripples with variable switching frequency and hence it is difficult to design the filter to reduce the torque ripples of the IM [6-8, 9, 10-25]. The hysteresis control was replaced by type-1fuzzy control (T1FC) or fuzzy control. The duty cycle of the converter is controlled by the fuzzy rule base in such a way that the total time period is held constant, which leads to constant switching frequency operation. Even though the complexity of the constant switching frequency control is higher than the hysteresis control, it provides constant switching losses, is easy to design the filter to reduce the torque and flux ripples, and reduced switching frequency band-width for selection of switching devices [1-2,10-22]. This chapter presents proportional integral direct torque control (PIDTC), type-1 fuzzy direct torque control (T1FDTC), and type-2 fuzzy direct torque control (T2FDTC) of IM drive using space vector modulation (SVM). The PIDTC gives considerable flux and torque ripples with the poor dynamic performance of the IM drive. In order to improve the dynamic performance of IM drive, the T1FDTC and T2FDTC are proposed. In both T1FDTC and T2FDTC, the PI-controllers are replaced by type-2 fuzzy controllers (T2FCs) to improve the dynamic performance of the IM drive than PIDTC. The steady state ripples of flux, current, and torque of the IM drive with T1FDTC and T2FDTC can be improved using duty ratio control (DRC) and hybrid space vector modulation control (HSVM). The DRC of SVM is independent of the sampling period to improve the firing strength of the inverter, whereas HSVM uses multiple sequences in each sector to reduce RMS flux ripple of the IM. Consequently, the current and torque ripples of IM drive can be improved significantly than PIDTC. The T2FDTC provides significant improvement in the dynamic response with less current THD than T1FDTC and PIDTC. Because, the T2FC has three-

dimensional control with type reduction in defuzzification process to effectively deal with the huge ambiguous data (larger footprint of data) than T1FC. Moreover, Mamdani and Centroid method with simple IF and THEN rules are used in both control schemes (T1FDTC and T2FDTC). A prototype controller is developed in the laboratory and the control signals for PIDTC, T1FDTC and T2FDTC are generated by the dSPACE DS-1104 controller. The T2FDTC provides fewer ripples in flux and torque and less current total harmonic distortion (THD) with fast dynamic performance of the IM drive than T1FDTC and PIDTC.

3.2 Mathematical model for the PIDTC of IM

The simplified per-phase equivalent circuit model of the motor gives good performance under steady state operation only. Hence, an accurate dynamic model of the IM is necessary to study the dynamic behavior of the machine under both transient and steady state conditions.

However, the following assumptions are considered to model the IM such as uniform air gap, balanced rotor and stator windings with sinusoidal distributed magneto motive force (MMF), inductance vs. rotor position is sinusoidal effectively, and saturation and parameter changes are neglected. From the law of induction the part of the applied voltage which is not lost as heat in the winding resistance will build up a flux wave in the stator windings. Thus the voltage for the induction machine can be expressed as [31]

$$V_{abcs} = R_s I_{abcs} + \frac{d\psi_{abcs}}{dt} \tag{3.1}$$

$$V_{abcr} = R_r I_{abcr} + \frac{d\psi_{abcr}}{dt} \tag{3.2}$$

where V_{abcs} and V_{abcr} stator and rotor voltage vectors, I_{abcs} and I_{abcr} are stator and rotor currents, ψ_{abcs} and ψ_{abcr} are the stator and rotor flux linkages, and subscript *s* and *r* imply stator and rotor coordinates, respectively.

A change of variables is often used to reduce the complexity of the differential equations describing the induction machine [2-6,97]. Thus the induction machine stator variables can be transformed directly from the abc reference frame to the arbitrary frame using the Parks transformation as [6-11]

$$[f_{qdos}] = K_s[f_{abcs}] \tag{3.3}$$

Similarly the arbitrary frame variables can be transformed into abc stator reference frame using the inverse Parks transformation as [6, 4, 8, 25]

$$[f_{abcs}] = K_s^{-1}[f_{qdos}] \tag{3.4}$$

where

$$K_s = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin\theta & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{3.5}$$

$$(K_s)^{-1} = \begin{bmatrix} \cos\theta & -\sin\theta & 1 \\ \cos\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta - \frac{2\pi}{3}\right) & 1 \\ \cos\left(\theta + \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) & 1 \end{bmatrix} \tag{3.6}$$

Transforming the stator voltage Eq. (3.1) from abc frame to arbitrary reference frame

$$V_{qd0s} = R_s K_s K_s^{-1}[i_{qdos}] + K_s p\left\{K_s^{-1}\left[\psi_{qdos}\right]\right\} \tag{3.7}$$

where p is the operator d/dt

The time derivative term of the above Eq. (3.7) can be expressed as

$$p\left\{K_s^{-1}\left[\psi_{qdos}\right]\right\} = \begin{bmatrix} -\sin\theta & \cos\theta & 0 \\ -\sin\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta - \frac{2\pi}{3}\right) & 0 \\ -\sin\left(\theta + \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) & 0 \end{bmatrix} \frac{d\theta}{dt}\left[\psi_{qdos}\right] + K_s^{-1}\left[p\psi_{qdos}\right] \tag{3.8}$$

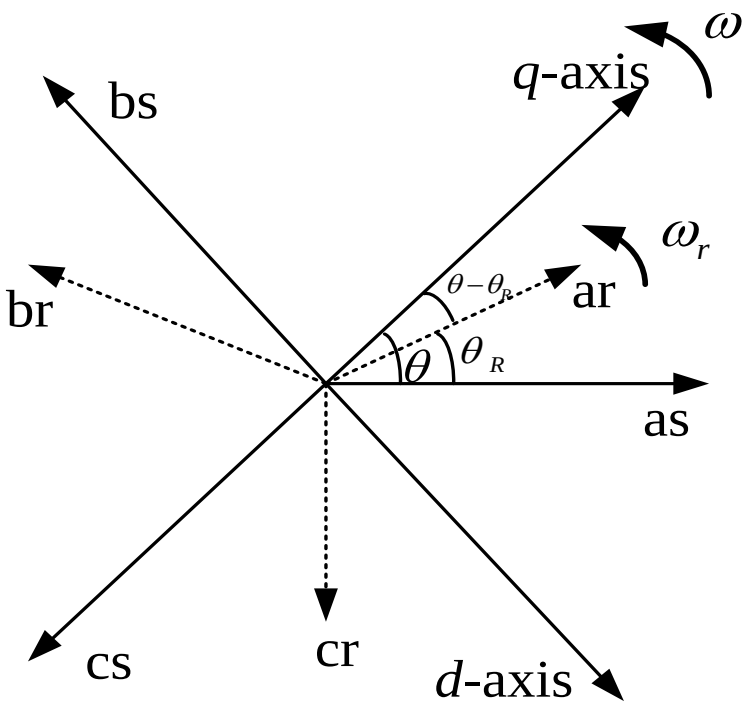


Fig. 3.1: Relationship between a-b-c and arbitrary rotating *q-d* axis

Substituting Eq. (3.5) and (3.6) in (3.7), the *d-q* voltage of the stator winding can be obtained as

$$V_{qd0s} = R_s \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \left[i_{qdos} \right] + \omega \begin{bmatrix} 0 & 1 & 0 \\ -1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \left[\lambda_{qdos} \right] + p \left[\lambda_{qdos} \right] \quad (3.9)$$

where $K_s K_s^{-1}$ is identity matrix and $\omega = \frac{d\theta}{dt}$ (Angular velocity of arbitrary reference frame). Due to the balanced operation the zero sequence voltages and currents are absent. This helps in representing the three phase machine by an equivalent two phase machine, with its phase in quadrature (*d-q* model). Thus the stator voltages can be expressed as [23]

$$v_{qs} = R_s i_{qs} + \omega \psi_{ds} + p \psi_{qs} \quad (3.10)$$

$$v_{ds} = R_r i_{ds} - \omega \psi_{qs} + p \psi_{ds} \quad (3.11)$$

where v_{ds} and v_{qs} are *d-q* axes stator voltages, i_{ds} and i_{qs} are d-q axes stator currents R_s is the stator resistance per phase, ψ_{qs} and ψ_{ds} are *d* and *q* axes stator flux linkages [36-38].

Similar to the stator, the rotor voltage Eq. (3.2) can also transform into *d-q* reference frame, but the transformation angle for the rotor quantities is (θ-θ_r) as shown in Fig 3.1. The rotor voltage can be expressed as

$$v_{qd0R} = R_r \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \left[i_{qdor} \right] + (\omega - \omega_r) \begin{bmatrix} 0 & 1 & 0 \\ -1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \left[\psi_{qdor} \right] + p \left[\psi_{qdor} \right] \quad (3.12)$$

Then the rotor voltages can be expressed after removing the zero quantity as

$$v_{qr} = R_r i_{qr} + (\omega - \omega_r) \psi_{dr} + p \psi_{qr} \quad (3.13)$$

$$v_{dr} = R_r i_{dr} - (\omega - \omega_r) \psi_{qr} + p \psi_{dr} \quad (3.14)$$

where v_{dr} and v_{qr} are *d-q* axis rotor voltages, i_{dr} and i_{qr} are d-q axis rotor currents respectively; R_r is rotor resistances per phase ψ_{qr} and ψ_{dr} are rotor flux linkages ω_r is rotor angular speed. In the squirrel cage IM the rotor bars are short circuited, so the voltages v_{qr} and v_{dr} are zero. The voltages can be expressed as

$$0 = R_r i_{qr} + (\omega - \omega_r) \psi_{dr} + p \psi_{qr} \quad (3.15)$$

$$0 = R_r i_{dr} - (\omega - \omega_r) \psi_{qr} + p \psi_{dr} \quad (3.16)$$

The stator and rotor flux linkages can be expressed as in-terms of inductances as [38]

$$\psi_{qs} = L_s i_{qs} + L_m i_{qr} \quad (3.17)$$

$$\psi_{ds} = L_s i_{ds} + L_m i_{dr} \quad (3.18)$$

$$\psi_{qr} = L_r i_{qr} + L_m i_{qs} \quad (3.19)$$

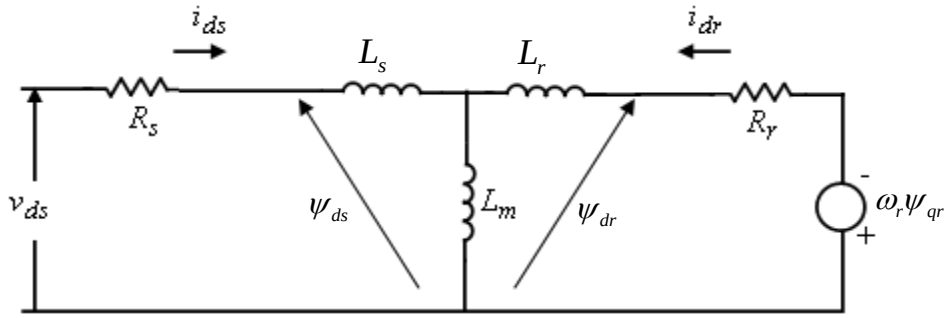
$$\psi_{dr} = L_r i_{dr} + L_m i_{ds} \quad (3.20)$$

where L_s and L_r are self inductances of the stator and rotor and L_m is mutual inductance. From the Eq. (3.12) to (3.13) and Eq. (3.14) to (3.19), the squirrel-cage IM can be expressed in matrix form as [15-21]

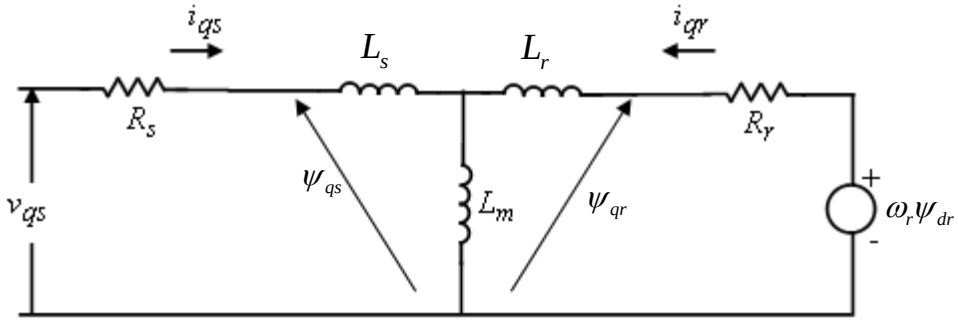
$$\begin{bmatrix} v_{qs} \\ v_{ds} \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} R_S + pL_s & \omega L_s & pL_m & \omega L_m \\ \omega L_s & R_s + pL_s & -\omega L_m & pL_m \\ pL_m & (\omega - \omega_r)L_m & R_r + pL_r & (\omega - \omega_r)L_r \\ -(\omega - \omega_r)L_m & pL_m & -(\omega - \omega_r)L_r & R_r + pL_r \end{bmatrix} \begin{bmatrix} i_{qs} \\ i_{ds} \\ i_{qr} \\ i_{dr} \end{bmatrix} \tag{3.21}$$

The IM model can be developed in three reference frames and these are:

- Stationary or stator reference frame
- Rotor reference frame
- Synchronously rotating reference frame



(a) *d*–axis equivalent circuit for IM



(a) q–axis equivalent circuit for IM

Fig. 3.2: Equivalent circuit of the IM in d-q axes

Among the various reference frames, DTC uses the stationary reference frame. Hence, in this work, the IM model is developed in the stationary reference frame, which is also known as a Stanley reference frame. For the stator reference frame, substituting ω=0, the above matrix form can be expressed as

$$\begin{bmatrix} v_{qs} \\ v_{ds} \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} R_s + pL_s & 0 & pL_m & 0 \\ 0 & R_s + pL_s & 0 & pL_m \\ pL_m & -\omega_r L_m & R_r + pL_r & -\omega_r L_r \\ \omega_r L_m & pL_m & \omega_r L_r & R_r + pL_r \end{bmatrix} \begin{bmatrix} i_{qs} \\ i_{ds} \\ i_{qr} \\ i_{dr} \end{bmatrix} \tag{3.22}$$

The equivalent circuit for the IM in d-q axes is given in Fig. 3.2, which looks like the transformer equivalent circuit. The stator and rotor currents in d-q axes are expressed using (3.22) as

$$i_{ds} = \frac{1}{\sigma L_s}\int (v_{qs} - R_s i_{qs} - \frac{L_m{}^2}{L_r}\omega_r i_{ds} - L_m \omega_r i_{dr} + \frac{L_m}{\tau_r} i_{qr})\, dt \tag{3.23}$$

$$i_{qs} = \frac{1}{\sigma L_s}\int (v_{ds} - R_s i_{ds} + \frac{L_m{}^2}{L_r}\omega_r i_{qs} + L_m \omega_2 i_{qr} + \frac{L_m}{\tau_r} i_{dr})\, dt \tag{3.24}$$

$$i_{dr} = \frac{1}{\sigma L_s L_r}\int (-v_{qs} + R_s i_{q1} - L_s \omega_r i_{ds} - \frac{L_s}{L_m} R_r i_{qr} + \frac{L_s L_r}{L_m}\omega_r i_{dr})\, dt \tag{3.25}$$

$$i_{qr} = \frac{1}{\sigma L_s L_r}\int (-v_{ds} + R_s i_{ds} - L_s \omega_r i_{qs} - \frac{L_s}{L_m} R_s i_{ds} + \frac{L_s L_r}{L_m}\omega_r i_{qr})\, dt \tag{3.26}$$

where, σ is magnetizing leakage coefficient$\left(1 - \frac{L_m{}^2}{L_s L_r}\right)$. The electromagnetic torque (T_e) can be expressed in terms of flux linkages and currents as [4-12]

$$T_e = \frac{3}{2}\frac{P}{2}\left(\psi_{ds} i_{qs} - \psi_{qs} i_{ds}\right) \tag{3.27}$$

where, P is the number of poles of the IM. From Eq. (3.17) to Eq. (3.18) and Eq. (3.22) the T_e can be expressed as [6, 9, 26]

$$T_e = \frac{3}{2}\frac{P}{2} L_m \left(i_{dr} i_{qs} - i_{qr} i_{ds}\right) \tag{3.28}$$

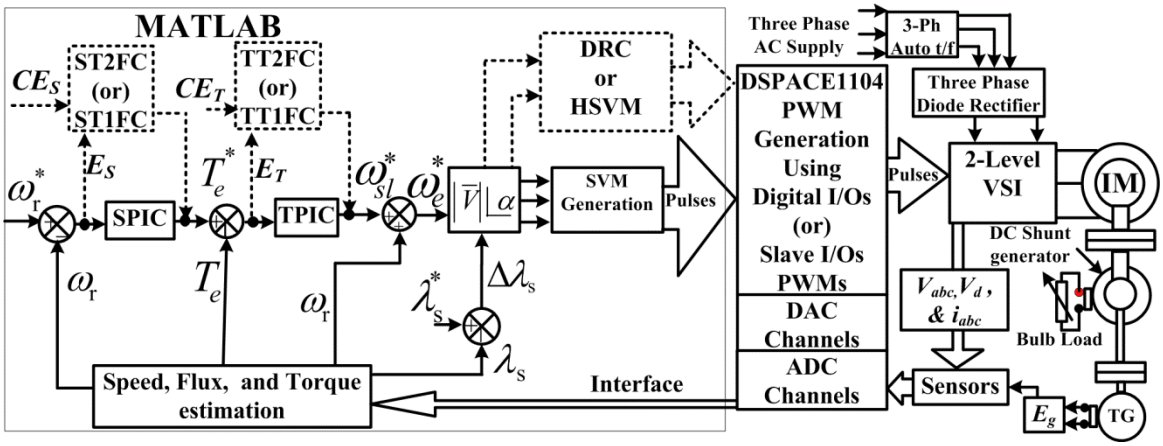


Fig. 3.3: Block diagram for PIDTC (thick line), type-1 and type-2 fuzzy DTC (dotted lines)

From the above Eq. (3.28), the torque produced by an IM depends solely on rotor current, which in turn is proportional to the air gap flux. Hence, if the flux of the motor is kept constant, then the motor is capable of delivering full load torque even at very low percentages of base speed. The electro-mechanical torque of the IM drive is given by

$$T_e = T_L + J\frac{d\omega_m}{dt} = T_L + \frac{2}{P}J\frac{d\omega_r}{dt} \tag{3.29}$$

where ω_m, ω_r, and J are mechanical speed, electrical speed, and moment of inertia of the IM, respectively. Fig. 3.3 shows the block diagram for proportional integral direct torque control (PIDTC) in thick line. Here, the speed of the induction motor is sensed by using DC-Tachogenerator that is coupled to the rotor shaft of the IM. The three-stator voltages and three-stator currents, DC-link voltage, and the speed of the IM are taken and fed back to the DSPACE board via the input ADC and Mux-ADC channels that are available in connector panel. The torque is estimated using Eq. (3.27) and the stator flux in d-q axes is estimated as [3-6]

$$\psi_{qs} = \int (v_{qs} - R_s i_{qs})dt \tag{3.30}$$

$$\psi_{ds} = \int (v_{ds} - R_s i_{ds})dt \tag{3.31}$$

Therefore the estimated stator flux is [13]

$$\psi = \sqrt{\psi_{ds}^2 + \psi_{qs}^2} \tag{3.32}$$

The angle θ is estimated from the torque PI-control (TPIC) as [1,19]:

$$\theta = \int \left(\omega_{sl}^* + \omega_r\right) dt \tag{3.33}$$

where $\omega_e^*, \omega_{sl}^*$, and ω_r are synchronous, slip, and rotor speed in rad/s, respectively. The reference flux is estimated as

$$\psi^* = \left|\psi^*\right| \cos\theta + j\left|\psi^*\right| \sin\theta \tag{3.34}$$

From the flux controller, the changes in d-q axes of stator flux linkages are given as:

$$\Delta\psi_{ds} = \left|\psi^*\right| \cos\theta - \psi_{ds} \tag{3.35}$$

$$\Delta\psi_{qs} = \left|\psi^*\right| \sin\theta - \psi_{qs} \tag{3.36}$$

The reference voltages in $\alpha - \beta$ axes are given as:

$$v_\beta^{\cdot} = \left(\Delta\psi_{qs} / \Delta t\right) + R_s i_{qs} \tag{3.37}$$

$$v_\alpha^{\cdot} = \left(\Delta\psi_{ds} / \Delta t\right) + R_s i_{ds} \tag{3.38}$$

where Δt is the change in time. The magnitude and the angle of the reference voltage vector are estimated as [10-17, 25-37]:

$$\overline{V} = \left| \sqrt{v_\alpha^{*2} + v_\beta^{*2}} \right| \angle \alpha \tag{3.39}$$

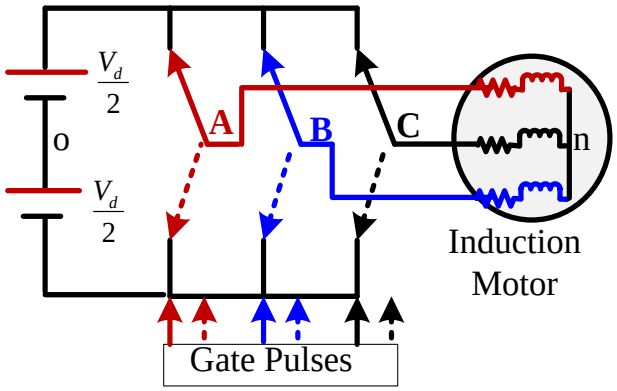
Where α is the angle between the reference vector and A-phase vector as

$$\alpha = \tan^{-1}\left(v_\beta^{*} / v_\alpha^{*} \right) \text{ and magnitude= } \sqrt{v_\alpha^{*2} + v_\beta^{*2}} \tag{3.40}$$

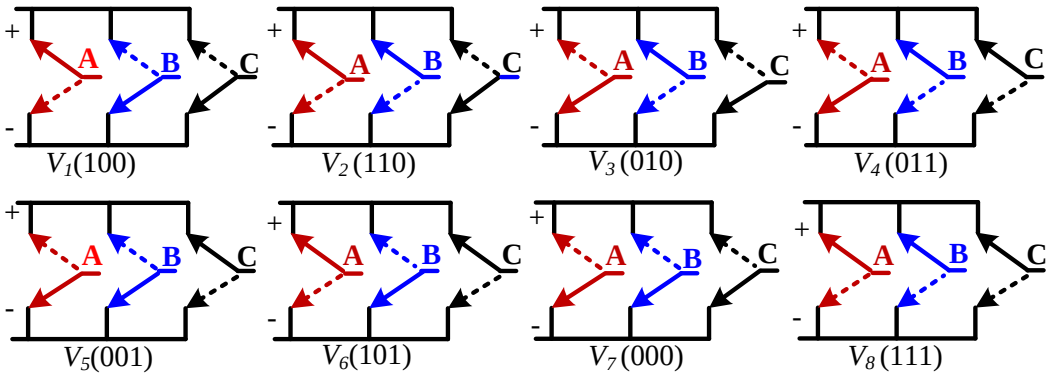
Now, the SVM pulses are developed after estimating reference vector and angle, which is explained later.

3.2.1 Voltage Source Inverter

Voltage source inverter (VSI) is a standard configuration for the PWM inverter drives due to the availability of fast power semiconductor devices, high dynamic response and good spectral performance compared to current source inverter (CSI) [23, 65]. Furthermore, the frequency range of VSI is higher when compared to CSI drives



(a) Three-phase two-level VSI fed IM



(b) Switching states for two-level VSI fed IM

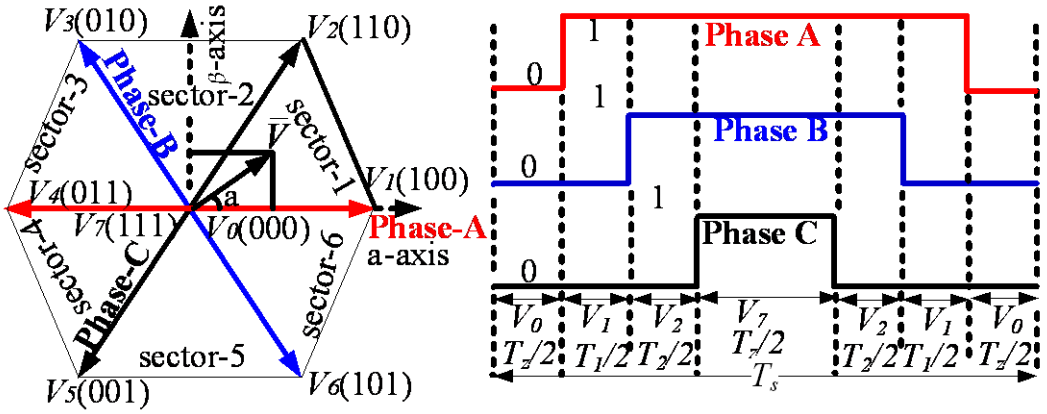
Fig. 3.4: VSI fed IM drive and its corresponding switching states

. In Fig 3.4 (a), the typical power stage of three phase two-level inverters and the equivalent circuit of the machine are presented. Fig. 3.4(a) provides the pole-voltages (V_{ao}, V_{bo}, V_{co}) for the inverter and phase-voltages applied to the induction machine are defined as V_{an}, V_{bn}, and V_{cn}. The available eight different switching states of three phase

inverter are depicted in the Fig 3.4 (b). Six out of these eight states (V_1 to V_6) produce a nonzero output voltage and are known as active switching states and the remaining two states (V_0 and V_7) produce zero output voltage and are known as zero switching states.

3.2.2 Space Vector Modulation (SVM)

A 3-ϕ 2-level inverter is shown in Fig. 3.4 (a), which consists of eight switching states as shown in Fig. 3.34 (b). Out of which, two are null states (000 and 111) that produce a zero inverter output voltage (line/phase voltages for the corresponding switching states) as shown in Fig. 3.4 (b). The other six states (V_1 toV_6) produces a vigorous voltage vector of the same magnitude $0.667V_d$ and have been divided by a constant phase displacement of 60° in a space vector plane as shown in Fig. 3.5 (a). The tips of these vectors form a regular hexagon. The defined area enclosed by two adjacent vectors, within the hexagon is known as a sector. Thus there are six sectors numbered 1 to 6 as shown in Fig. 3.5(a). The vectors have zero magnitude are referred to as zero-switching state vectors. They assume a position at the origin in the α-β reference plane.



(a): Space vector diagram (b) Pulse pattern at sector-1 region for two-level inverter

Fig. 3.5: Vector rpresentation for two-level VSI and corresponding pulse pattern for the sector-1

Table 2.1: Selection of switching sequences for SVM in all sectors

Sector No's	1st half-Sequence	2nd half-Sequence
1	$V_0V_1V_2V_7$	$V_7V_2V_1V_0$
2	$V_0V_3V_2V_7$	$V_7V_2V_3V_0$
3	$V_0V_3V_4V_7$	$V_7V_4V_3V_0$
4	$V_0V_5V_4V_7$	$V_7V_4V_5V_0$
5	$V_0V_5V_6V_7$	$V_7V_6V_5V_0$
6	$V_0V_1V_6V_7$	$V_7V_6V_1V_0$

The selection of switching states in all the sectors is given in Table-2.1 [14-20]. The switching times (T_1, T_2, and T_Z) are calculated for two-level SVM as

Appling the volt-second principle along α-axis

$$T_s \left|\overline{V}\right| \cos\alpha = T_1 V_1 + V_2 T_2 \cos 60° + 0 T_Z \tag{3.42}$$

Appling the volt-second principle along β-axis

$$T_s \left|\overline{V}\right| \sin\alpha = 0 T_1 + V_2 T_2 \sin 60° + 0 T_Z \tag{3.43}$$

The active vector time (T_2) for the corresponding voltage vector V_2 is [35]

$$T_2 = M T_s \frac{\sin(\alpha)}{\sin(60°)} \tag{3.44}$$

Substitute T_2 in Eq. (3.42), the active vector time (T_1) for the corresponding voltage vector V_1 is

$$T_1 = M T_s \frac{\sin(60° - \alpha)}{\sin(60°)} \tag{3.45}$$

Zero vector time (T_Z) for zero voltage vectors V_0 or V_7 is [31-38]

$$T_z = T_s - T_1 - T_2 \tag{3.46}$$

where, M , T_s, and V_d is the modulation index (MI), switching period, and DC-link voltage, respectively. The three pulses are generated in sector-1 region using Eq. (3.44) to Eq. (3.46) and Table 2.1 as shown in Fig. 3.5(b). Therefore, the process remains the same in other five sectors to develop the switching pulses for full cycle [5-10]. The three pole voltages (v_{ao}, v_{bo}, v_{co}) of the inverter are given as:

$$\begin{bmatrix} v_{ao} \\ v_{bo} \\ v_{co} \end{bmatrix} = \frac{V_d}{2} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} s_a \\ s_b \\ s_c \end{bmatrix} \tag{3.47}$$

$$s_a = \begin{cases} +1, \ if \ S_a = 1, \ then \ \text{switch is connected to +ve side of DC-link voltage} \\ -1, \ if \ S_a = 0, then \ \text{switch is connected to -ve side of DC-link voltage} \end{cases}$$

where $s_b = \begin{cases} +1, \ if \ S_b = 1, then \ \text{switch is connected to +ve side of DC-link voltage} \\ -1, \ if \ S_b = 0, then \ \text{switch is connected to -ve side of DC-link voltage} \end{cases}$

$$s_c = \begin{cases} +1, \ if \ S_c = 1, then \ \text{switch is connected to +ve side of DC-link voltage} \\ -1, \ if \ S_c = 0, then \ \text{switch is connected to -ve side of DC-link voltage} \end{cases}$$

The common mode voltage is given as:

$$v_{no} = \frac{v_{ao} + v_{bo} + v_{co}}{3} \tag{3.48}$$

The line voltages of the inverter can be found in the corresponding switching states (S_a, S_b, and S_c) as

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = V_d \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} = V_d \begin{bmatrix} S_a - S_b \\ S_b - S_c \\ S_c - S_a \end{bmatrix} \tag{3.49}$$

Table 2.2: Possible voltage vectors for the corresponding switching states

Switching states	V_{ao}	V_{bo}	V_{co}	V_{no}	V_{ab}	V_{bc}	V_{ca}	V_{an}	V_{bn}	V_{cn}	V_{Lk}	V_{Pk}
V_0(0 0 0)	$-\frac{V_d}{2}$	$-\frac{V_d}{2}$	$-\frac{V_d}{2}$	$-\frac{V_d}{2}$	0	0	0	0	0	0	0	0
V_1 (1 0 0)	$\frac{V_d}{2}$	$-\frac{V_d}{2}$	$-\frac{V_d}{2}$	$-\frac{V_d}{6}$	V_d	0	$-V_d$	$-\frac{2V_d}{3}$	$-\frac{V_d}{3}$	$-\frac{V_d}{3}$	$\frac{2V_d\angle 30°}{\sqrt{3}}$	$\frac{2V_d\angle 0°}{3}$
V_2 (1 1 0)	$\frac{V_d}{2}$	$\frac{V_d}{2}$	$-\frac{V_d}{2}$	$-\frac{V_d}{6}$	0	V_d	$-V_d$	$\frac{V_d}{3}$	$\frac{V_d}{3}$	$-\frac{2V_d}{3}$	$\frac{2V_d\angle 90°}{\sqrt{3}}$	$\frac{2V_d\angle 60°}{3}$
V_3 (0 1 0)	$-\frac{V_d}{2}$	$\frac{V_d}{2}$	$-\frac{V_d}{2}$	$-\frac{V_d}{6}$	$-V_d$	V_d	0	$-\frac{V_d}{3}$	$\frac{2V_d}{3}$	$-\frac{V_d}{3}$	$\frac{2V_d\angle 150°}{\sqrt{3}}$	$\frac{2V_d\angle 120°}{3}$
V_4 (0 1 1)	$-\frac{V_d}{2}$	$\frac{V_d}{2}$	$\frac{V_d}{2}$	$-\frac{V_d}{6}$	$-V_d$	0	V_d	$-\frac{2V_d}{3}$	$\frac{V_d}{3}$	$\frac{V_d}{3}$	$\frac{2V_d\angle 210°}{\sqrt{3}}$	$\frac{2V_d\angle 180°}{3}$
V_5 (0 0 1)	$\frac{V_d}{2}$	$\frac{V_d}{2}$	$\frac{V_d}{2}$	$-\frac{V_d}{6}$	0	$-V_d$	V_d	$-\frac{V_d}{3}$	$-\frac{V_d}{3}$	$\frac{2V_d}{3}$	$\frac{2V_d\angle 270°}{\sqrt{3}}$	$\frac{2V_d\angle 240°}{3}$
V_6 (1 0 1)	$\frac{V_d}{2}$	$-\frac{V_d}{2}$	$\frac{V_d}{2}$	$-\frac{V_d}{6}$	V_d	$-V_d$	0	$\frac{V_d}{3}$	$\frac{2V_d}{3}$	$\frac{V_d}{3}$	$\frac{2V_d\angle 330°}{\sqrt{3}}$	$\frac{2V_d\angle 300°}{3}$
V_7 (1 1 1)	$\frac{V_d}{2}$	$\frac{V_d}{2}$	$\frac{V_d}{2}$	$\frac{V_d}{2}$	0	0	0	0	0	0	0	0

The phase voltages of the inverter are found for the corresponding switching states as

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = \frac{V_d}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} = \frac{V_d}{3} \begin{bmatrix} 2S_a - S_b - S_c \\ 2S_b - S_c - S_a \\ 2S_c - S_a - S_b \end{bmatrix} \tag{3.50}$$

where the switching states $\left.\begin{matrix} S_a \\ S_b \\ S_c \end{matrix}\right\} = 0 \; or \; 1$

The sum of line voltage vectors for the corresponding switching states is

$$V_{SL} = V_{kL} = \frac{2}{3}\left(V_{ab}e^{j0} + V_{bc}e^{j\frac{2\pi}{3}} + V_{ca}e^{j\frac{4\pi}{3}} \right) \tag{3.51}$$

where k = 0, 1, 2, 3, 4, 5, 6, and 7 for corresponding voltage vectors.

Similarly, the resultant phase voltage vectors are found using Eq. (3.51) in which the line voltages are replaced by phase voltages for the corresponding switching states as given in Table 2.2. Table-2.2 shows pole voltages (V_{ao}, V_{bo}, and V_{co}), common mode voltages (V_{no}), line voltages (V_{ab}, V_{bc}, and V_{ca}**)**, phase voltages (V_{an}, V_{bn}, and V_{cn}), sum of line voltages (V_{Lk}) and sum of phase voltages (V_{Pk}) of the inverter are found for the corresponding switching states [12-21].

3.2.3 Transfer Function of the PIDTC of IM

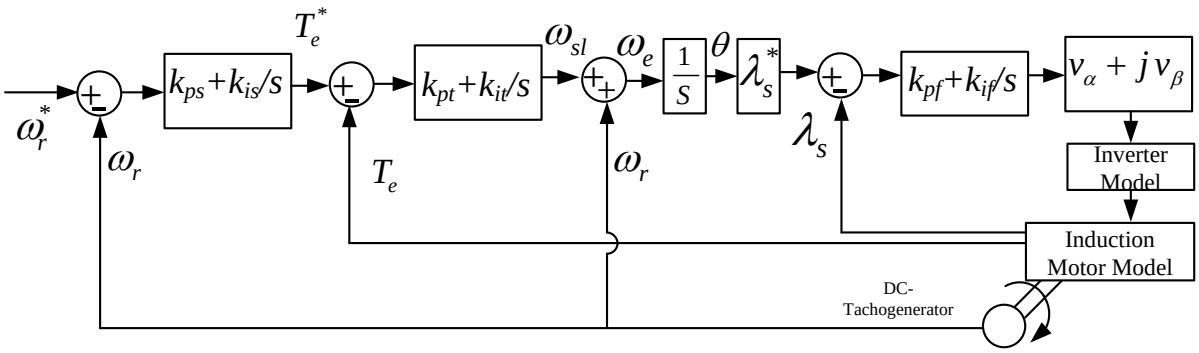
Fig. 3.6 (a) shows the closed loop block diagram for PIDTC. The G(s) is the open loop transfer function (TF) which consists of speed, torque, and flux controllers along with the plant and IM modeling as shown in Fig. 3.6 (a) in which H(s) is the unity feedback gain of overall speed/outer loop control and G(s) can be found from Eq. (3.52) after substituting k_p and k_i gains of the respective controllers (speed, torque, and flux) that are mentioned in Appendix-1. The overall open loop TF G(s) of the speed control (overall TF of PIDTC) can be found as

$$G(s) = \frac{2.948e^{6}s^{4} + 2.037e^{8}s^{3} + 2.436e^{9}s^{2} + 1.015e^{4}s + 0.1015}{s^{7} + 1246s^{6} + 3.982e^{5}s^{5} + 6.4e^{6}s^{4} + 2.64e^{8}s^{3}} \tag{3.52}$$

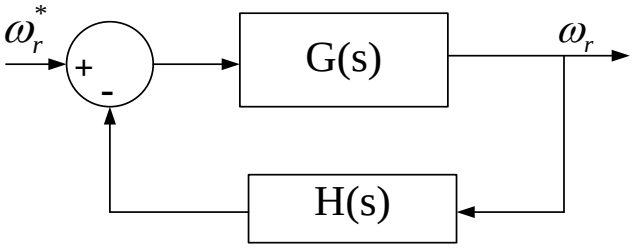
With the help of Eq. (3.52), the overall closed loop transfer function (CLTF) for the speed control of PIDTC can be found as

$$TF_{PIDTC} = \frac{\omega_r(s)}{\omega_r^*(s)} = \frac{G(s)}{1 + G(s)H(s)} \tag{3.53}$$

$$= \frac{2.948e^{6}s^{4} + 2.03e^{8}s^{3} + 2.43e^{9}s^{2} + 4.669e^{4}s + 0.1015}{s^{7} + 1246s^{6} + 3.982e^{5}s^{5} + 9.348e^{6}s^{4} + 2.301e^{8}s^{3} + 2.436e^{9}s^{2} + 4.669e^{4}s + 0.1015} \tag{3.54}$$



(a) Overall block diagram for PIDTC of IM



(b) Closed loop block diagram for the speed control of PIDTC

Fig. 3.6 Block diagram reduction for the speed PI-control of the IM drive with PIDTC

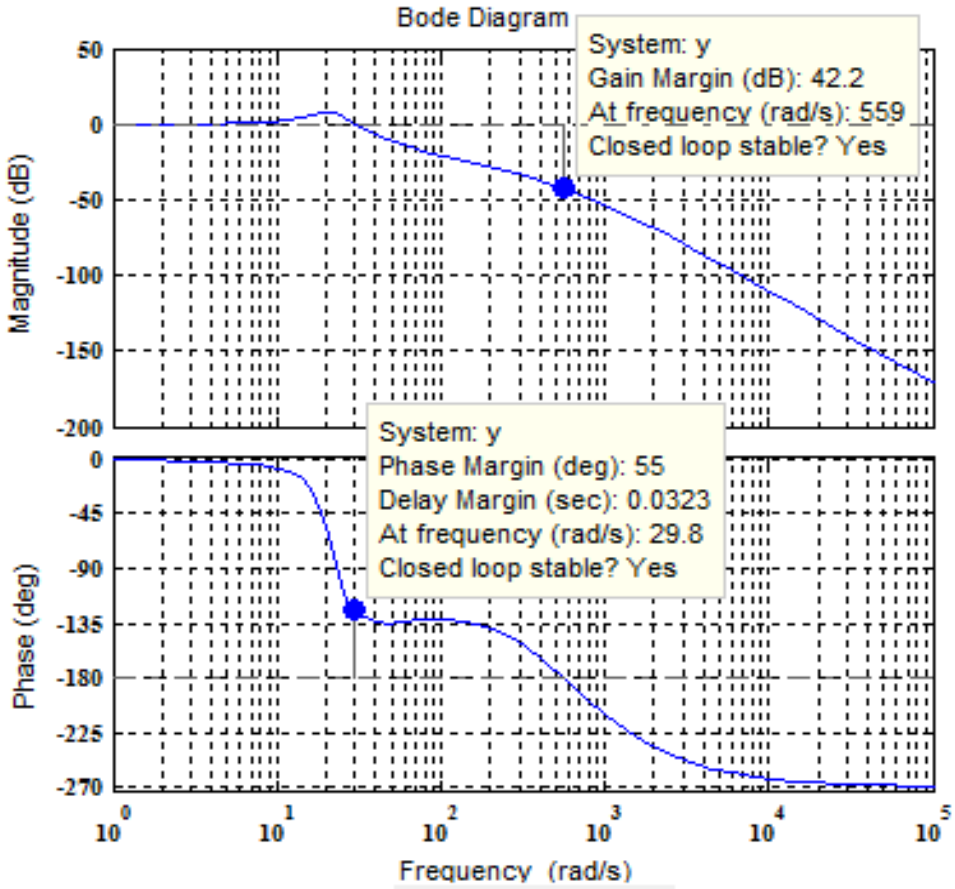


Fig. 3.7: Bode plots for CLTF for PIDTC of IM

Using (3.54), the closed loop stability performance is analyzed and it is verified with the bode plot (magnitude and phase plots) as shown in Fig. 3.7. The corresponding gain and phase margin for the bode plot are 42.2 and 55, respectively as shown in the Fig. 3.7.

3.3 Type-1 Fuzzy Direct Torque Control (T1FDTC)

The procedure and way of approach are already explained in the previous chapter (Chapter-2). However, a little brief explanation is given in this section. Fig. 3.3 shows the block diagram for T1FDTC (shown by dotted line) in which the PI-controllers (speed and torque) of PIDTC are replaced with T1FLC. From the SPIC, the output of the controller can be expressed as [16-21]

$$T_e^* = k_{ps} e_s^*(t) + k_{is} \int e_s^*(t) dt \tag{3.55}$$

where k_{ps} and k_{is} are proportional and integral gains of SPIC, and $e_s^*(t)$ is the error of SPIC, respectively. Applying differentiation on both sides of (3.55)

$$\frac{dT_e^*}{dt} = k_{ps} \frac{de_s^*(t)}{dt} + k_{is} e_s^*(t) \tag{3.56}$$

From (3.56), it is clear that the change of the torque is directly proportional to inputs of speed control, i.e., error (E_s) and change of error (CE_s) as shown in Fig. 3.3, and they are [19] -[22]

$$E_S(k) = \omega_r^*(k) - \omega_r(k) \tag{3.57}$$

$$CE_S(k) = E_S(k) - E_S(k-1) \tag{3.58}$$

where, $\omega_r^*(k)$ and $\omega_r(k)$ are reference and actual rotor speed, respectively. $E_s(k)$ and $E_s(k-1)$ are present and previous speed errors, respectively. When a change of torque $\Delta T_e^*(k)$ is obtained, then the output of the speed controller is [26-32]

$$T_e^*(k) = T_e^*(k-1) + \Delta T_e^*(k) \tag{3.59}$$

where $T_e^*(k-1)$ is the previous value of the estimated torque value from the speed T1FC (ST1FC). The ST1FC has input (E_s and CE_s) and output (T_{Ce}) MFs as shown in Fig. 3.8(a), 3.8(b), and 3.8(c), respectively. Where the inputs (E_s and CE_s) have 7 triangular MFs and the output side also has 7 triangular MFs and therefore the number of possible rules (M) should be 49 as given in Table 3.3 in which, each rule has the following form as [27-28]

IF E_s is $G_{E_s}^i$ and CE_s is $G_{CE_s}^i$ THEN δ_T is (T_l^i, T_r^i) (3.60)

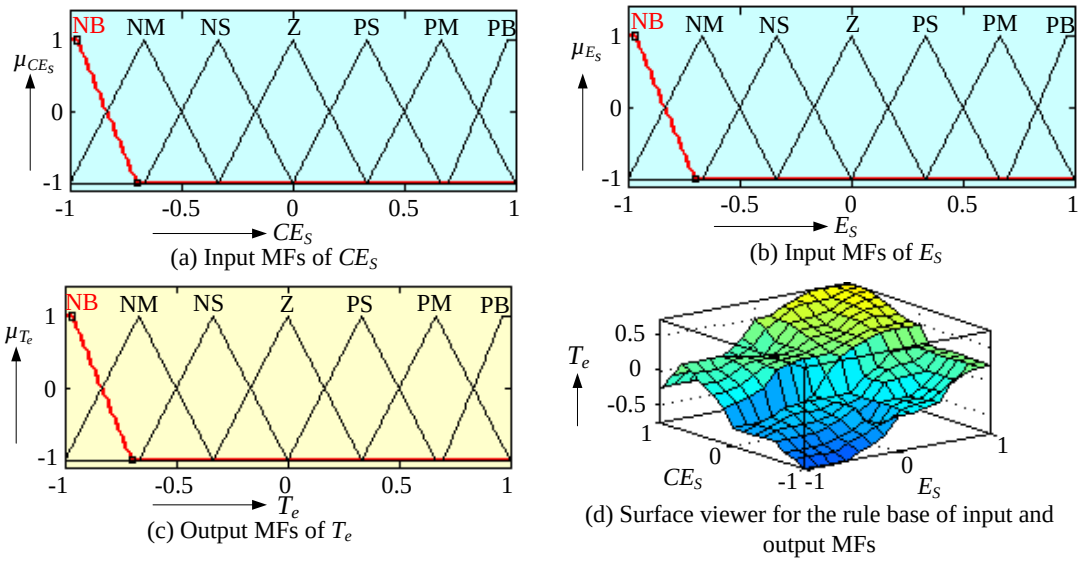
Where i is1, 2… M rules, $G_{E_s}^{i}$ and $G_{CE_s}^{i}$ are fuzzy sets of the IF-ingredient, and T_l^i and T_r^i are singleton left and right control actions of THEN-ingredient, respectively. The triangular MFs of IF and THEN parts are input ($E_s(k)$ and $CE_s(k)$) and output side ($T_e(k)$) of ST2FC respectively. The names of the triangular MFs for ST1FC in both input and output side are negative big (NB), negative medium (NM), negative small (NS), zero (Z), positive small (PS), positive medium (PM), and positive big (PB) as shown in Fig. 3.8 (a), Fig. 3.8 (b), and Fig. 3.8 (c). Fig. 3.8 (d) shows the surface viewer for the ST1FC, which clearly gives the input and the output relation of the rules with respect to the MFs [32-39].

3.3.1 Centroid Method T1FLC

The centroid of reference electromagnetic torque T_{Ce}^{*} (found from the crisp output of ST1FC) is estimated for the overall MF [20-26] and is given as [110-116, 129-141]:

$$T_{Ce}^{*} = \frac{\sum_{k=0}^{n} T_{Ck}^{*}\,\mu(T_{Ck}^{*})}{\sum_{k=1}^{n} \mu(T_{Ck}^{*})} \tag{3.61}$$

where, $\mu(T_{Ck}^{*})$ and T_{Ck}^{*} are overall output MF and crisp output quantity of speed controller, respectively, and k = 1, 2, ……,n number of samples of the aggregated output MF.



(a) Input MFs of CE_S

(b) Input MFs of E_S

(c) Output MFs of T_e

(d) Surface viewer for the rule base of input and output MFs

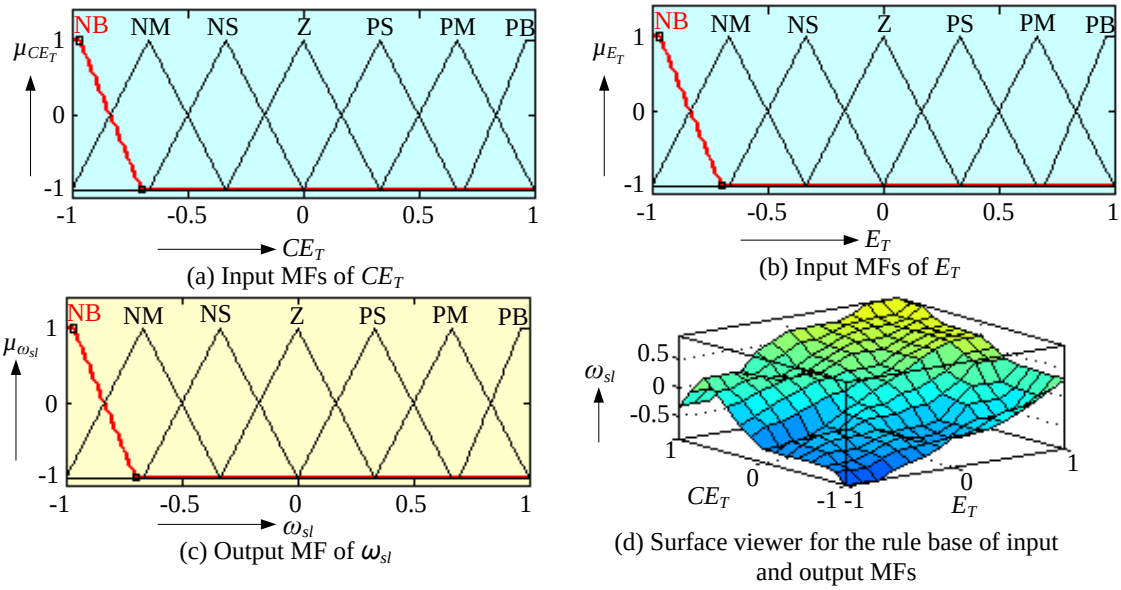
Fig. 3.8: Speed type-1 fuzzy control (ST1FC)

As similar to ST1FC, the torque PI-controller (TPIC) is replaced by torque type-1 fuzzy control (TT1FC) in which it has the same number of triangular MFs (7) in both input (E_T and CE_T) and output (ω_{sl}) side with the same number of rules M (49) as given at Table 3.4 and names of the MFs (NB, NM, NS, Z, PS, PM, and PB) as shown in Fig. 3.9 (a), Fig.

3.9 (b), and Fig. 3.9 (c). Fig. 3.9 (d) shows the surface viewer for the TT1FC, which clearly gives the input and the output relation of the rules with respect to the MFs. The corresponding crisp value of centroid reference slip speed ($\omega^*_{sl_{Ce}}$) for the TT1FC is estimated from overall MF as [110-115, 148]:

$$\omega^*_{sl_C} = \frac{\sum_{k=0}^{n} \omega^*_{sl_{Ck}} \mu(\omega^*_{sl_{Ck}})}{\sum_{k=1}^{n} \mu(\omega^*_{sl_{Ck}})} \tag{3.62}$$

where, $\mu(\omega^*_{sl_{Ck}})$ and $\omega^*_{sl_{Ck}}$ are overall output MF and crisp output quantity of slip speed, respectively and k=1, 2, ……n number of samples of the aggregated output MF.



(a) Input MFs of CE_T

(b) Input MFs of E_T

(c) Output MF of ω_{sl}

(d) Surface viewer for the rule base of input and output MFs

Fig. 3.9: Torque type-1 fuzzy control (TT1FC)

3.4 Type-2 fuzzy Based DTC

The type-2 fuzzy DTC block diagram is shown in Fig. 3.3, which is mentioned on the dotted line. The speed and torque PI-controllers are replaced by TP2FLC to further improve the dynamic performance of the IM drive. In addition, the duty ratios are controlled and hybrid space vector modulation (HSVM) using T2FLC to improve the flux and the torque performance of an IM, which is explained later in detail [107-121]. The input and output triangular MFs of ST2FC have found in Fig. 3.8 and Fig. 3.9 (a) respectively. Moreover, the rules are framed in Table 3.3 using IF and THEN. Here, the number of inputs (E_T and CE_T) and output (T_e) MFs remain same as that of ST1FC,which

is shown in Fig. 3.10(a), Fig. 3.10(b), and Fig. 3.10(c). Moreover, the corresponding numbers of rules for ST2FC are also same as that of ST1FC, which is given in same Table 3.3. The names of the triangular MFs for both input and output side are NB, NM, NS, Z, PS, PM, and PB as shown in Fig. 3.10 (a), Fig. 3.10 (b), and Fig. 3.10 (c). Fig. 3.10 (d) shows the surface viewer for the ST2FC, which clearly gives the input and the output relation of the rules with respect to their MFs of T2FLC [45-55, 99-107].

Table 3.3: Rule frame for ST1FC and ST2FC

E_S \ CE_S	**NB**	**NM**	**NS**	**Z**	**PS**	**PM**	**PB**
NB	NB	NB	NS	Z	PS	PM	PB
NM	NB	NB	NS	PS	PS	PS	PS
NS	NM	NS	NS	NS	PS	PS	PS
Z	NB	NB	NS	Z	PS	PM	PB
PS	NS	PS	PS	PM	PM	PB	PB
PM	NS	NS	PS	PM	PM	PB	PB
PB	NS	NS	PS	PM	PM	PB	PB

Table 3.4: Rule frame for TT1FC and TT2FC

E_T \ CE_T	**NB**	**NM**	**NS**	**Z**	**PS**	**PM**	**PB**
NB	NB	NB	NS	NS	NS	Z	PS
NM	NB	NB	NS	NS	Z	PS	PS
NS	NB	NM	NS	NS	Z	PS	PS
Z	NB	NB	NM	Z	PS	PM	PB
PS	PS	NM	NS	PS	PS	PM	PB
PM	PB	PM	PS	PM	PS	PM	PS
PB	PB	PB	PB	PB	PB	PB	PB

The design procedure from Eq. (3.55) to Eq. (3.60) for speed type-2 fuzzy control (ST2FC) remains same as the ST1FC.

3.4.1 Type Reduction of T2FLC

The type-2 fuzzy values of i^{th} rule can be obtained as [102-109, 121-125]:

$$F^i = \left(\underline{f}^i, \overline{f}^i \right) \tag{3.63}$$

where

$$\underline{f}^i = \underline{\mu}_{\underline{G}^i_{E_s}}(E_s, u) * \underline{\mu}_{\underline{G}^i_{CE_s}}(CE_s, u) \tag{3.64}$$

$$\overline{f}^{i} = \overline{\mu}_{\tilde{G}^{i}_{E_s}}(E_s, u) * \overline{\mu}_{\tilde{G}^{i}_{CE_s}}(CE_s, u) \tag{3.65}$$

where $\underline{\mu}_{\tilde{G}^{i}_{E_s}}$ and $\overline{\mu}_{\tilde{G}^{i}_{CE_s}}$ are grades of lower and upper MFs, respectively. A singleton fuzzification with a minimum t-norm is used and the output can be expressed as [26]:

$$\delta_{T_{\cos}} = \left[\delta_{T_l}, \delta_{T_r} \right] \tag{3.66}$$

where $\delta_{T_{\cos}}$ is an interval of type-2 fuzzy set determined by the left and right end points (δ_{T_l}, δ_{T_r}), which can be derived from the consequent centroid set (T_l^i, T_r^i) and torque strength $\underline{f}^i \in F^i = \left(\underline{f}^i, \overline{f}^i \right)$ must be computed or set first before the computation of $\delta_{T_{\cos}}$.

The left and rightmost points (δ_{T_l}, δ_{T_r}) are expressed as [108-121]:

$$\delta_{T_l} = T_l = \sum_{i=1}^{M} \left[f_l^i T_l^i \right] \Big/ \sum_{i=1}^{M} f_l^i \tag{3.67}$$

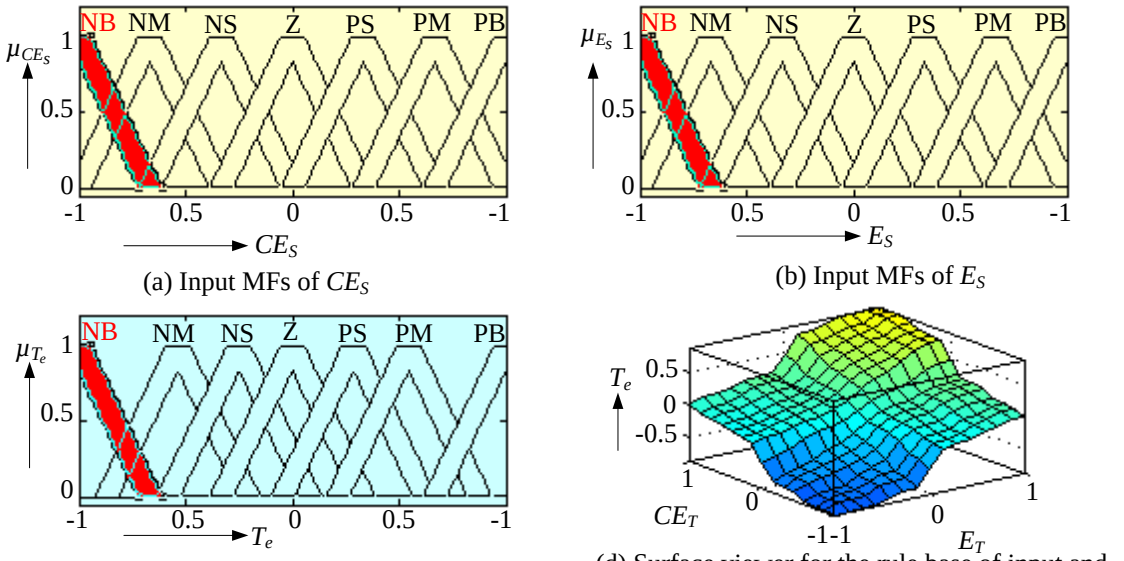
$$\delta_{T_r} = T_r = \sum_{i=1}^{M} \left[f_r^i T_r^i \right] \Big/ \sum_{i=1}^{M} f_r^i \tag{3.68}$$

It briefly states the procedure to compute δ_{T_l} and δ_{T_r}. First compute the rightmost point δ_{T_r} without loss of generality; assume that T_r^i is arranged in ascending order, i.e., $T_r^1 \le T_r^2 \le \ldots \le T_r^M$. The algorithm for finding crisp output on the right side of T2FC is shown in Fig. 6. Hence, δ_{T_r} in (32) can be re-expressed as [103-127, 129-138, 149-155]:

$$\begin{aligned} \delta_{T_r} &= \delta_{T_r}\left(\underline{f}^1, \ldots, \underline{f}^R, \overline{f}^{R+1}, \ldots, \overline{f}^M, T_r^1, \ldots, T_r^M \right) \\ &= \left[\sum_{i=1}^{R} \underline{f}^i T_r^i + \sum_{i=R+1}^{M} \overline{f}^i T_r^i \right] \Big/ \left[\sum_{i=1}^{R} \underline{f}^i + \sum_{i=R+1}^{M} \overline{f}^i \right] \end{aligned} \tag{3.69}$$

The procedure to compute δ_{T_l} is similar to that of δ_{T_r} (as shown in Fig. 3.12) with slight modifications. In 3rd step of the Fig. 3.12, find L ($1 \le L \le M-1$) such that $T_l^L \le \delta_{T_l}' \le T_l^{L+1}$, and allow $f_l^i = \overline{f}^i$ for $i \le L$ and $f_r^i = \underline{f}^i$ for $i > L$. Therefore δ_{T_l} can be expressed using (3.69) as [108-125, 145]:

$$\delta_{T_l} = \delta_{T_l}\left(\overline{f}^1,\ldots,\overline{f}^L,\underline{f}^{L+1},\ldots,\underline{f}^M,T_l^1,\ldots,T_l^M\right) = \left[\sum_{i=1}^{L}\overline{f}^i T_l^i + \sum_{i=L+1}^{M}\underline{f}^i T_l^i\right] \Big/ \left[\sum_{i=1}^{L}\overline{f}^i + \sum_{i=L+1}^{M}\underline{f}^i\right] \tag{3.70}$$



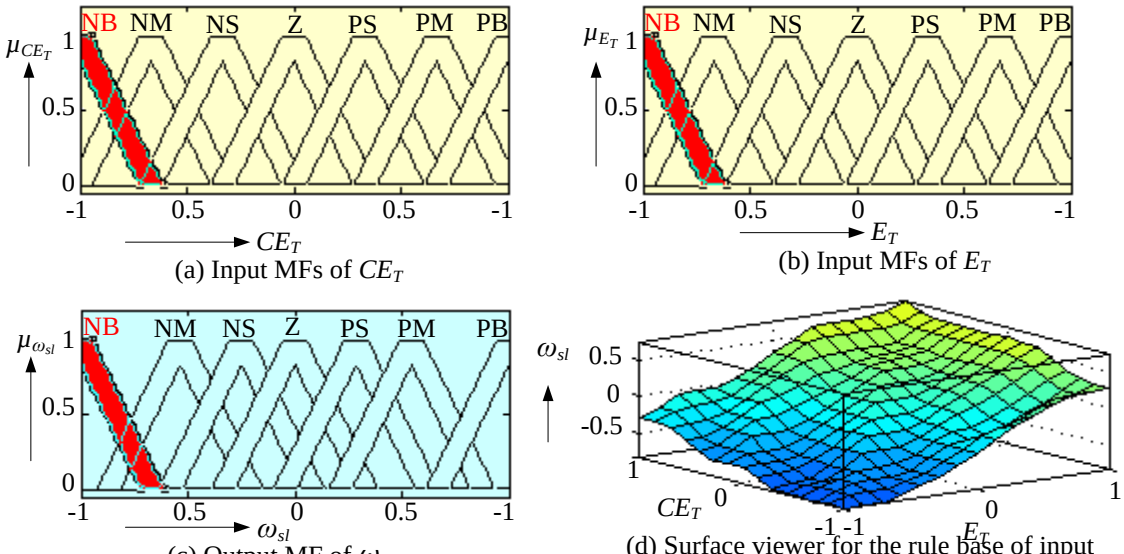
(a) Input MFs of CE_S

(b) Input MFs of E_S

(c) Output MFs of T_e

(d) Surface viewer for the rule base of input and output MFs

Fig. 3.10: Speed type-2 fuzzy control (ST2FC)



(a) Input MFs of CE_T

(b) Input MFs of E_T

(c) Output MF of ω_{sl}

(d) Surface viewer for the rule base of input and output MFs

Fig. 3.11: Torque type-2 fuzzy control (TT2FC)

3.4.2 Centroid of T2FLC

The defuzzified crisp output from an interval fuzzy-2 system is the average of δ_{T_r} and δ_{T_l} as [107]

$$\delta_{T_{ec}} = \left(\delta_{T_r} + \delta_{T_l} \right) \Big/ 2 \tag{3.71}$$

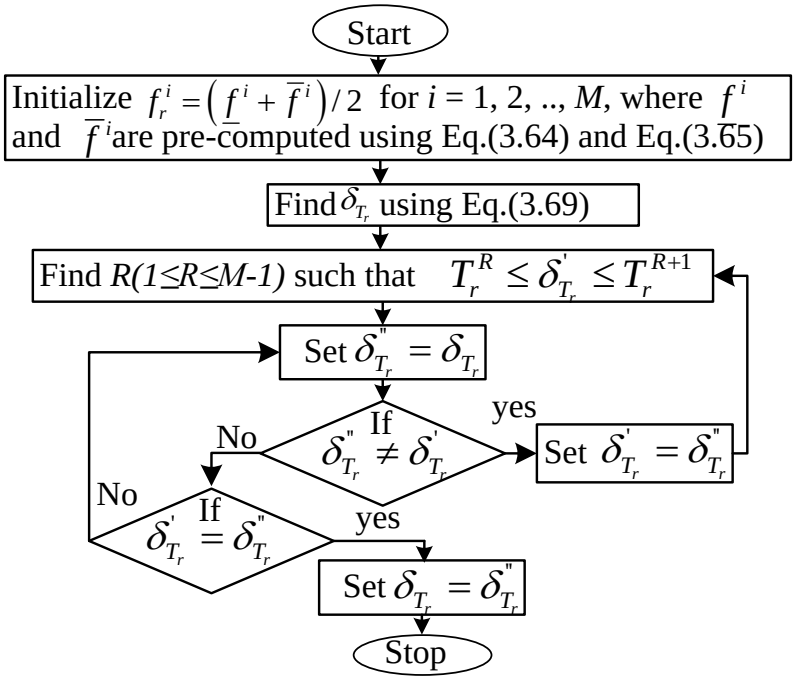


Fig. 3.12: Flowchart for finding the crisp value of the torque $\left(\delta_{T_r} \right)$

Similarly, the way of approach for torque TT2FC (TT2FC) is same as the ST2FC. Moreover, TT2FC has the same number of input and output MFs, and hence the number of rules (*M*) also be the same i.e., 49 as shown in Table-3.4. However, it has different crisp and fuzzy values in both the input and output side of TT2FC with the names of MFs i.e., NB, NM, NS, Z, PS, PM, and PB as shown in Fig. 3.11(a), Fig. 3.11(b), and Fig. 3.11(c). The crisp output of TT2FC is estimated like ST2FC using (35) as [45-53, 107-111]:

$$\delta_{\omega_{slc}} = \left(\delta_{\omega_{slcr}} + \delta_{\omega_{slcl}} \right) \Big/ 2 \tag{3.72}$$

Fig. 3.11(d) shows the surface viewer for the TT2FC, which clearly gives the input and the output relation of the rules with respect to their MFs of T2FLC. The surface viewer is improved with the TT2FC and the ST2FC as compared to TT1FC and the ST1FC. Therefore from huge ambigious data, the T2FLC estimates the control variable as close to

the actual value than T1FLC and PIC, which leads to improve the dynamic response of the IM drive with T2FDTC as compared T1FLC and PIDTC. The details of information will be studied in results and discussion.

3.5 Improvement of the current and flux ripples

The flux and current ripple performance during steady state of the IM in both T1FDTC and T2FDTC can be improved by

- Duty ratio control
- Hybrid Space Vector Modulation

3.5.1 Duty ratio control (DRC)

Fig. 3.13 shows the DRC for SVM in which the corresponding duty ratios are developed with the help of either T1FLC or T2FLC and the switching pulses are developed to the inverter with the help of repetitive counter [136]-[139]. The duty ratios are found from Eq. (3.73) to Eq. (3.75), which is independent of sampling time T_s as given below [138].

$$d_2 = \frac{t_2}{t_s} = M\,\frac{\sin\left(60^\circ - \alpha\right)}{\sin\left(60^\circ\right)} \tag{3.73}$$

$$d_1 = \frac{t_1}{t_s} = M\,\frac{\sin\left(\alpha\right)}{\sin\left(60^\circ\right)} \tag{3.74}$$

$$d_0 = 1 - d_1 - d_2 = \frac{t_Z}{t_s} \tag{3.75}$$

where d_1 is the duty ratio of switching vector that lags $\overline{V}$

d_2 is the duty ratio of switching vector that leads $\overline{V}$

d_0 is the duty cycle of zero switching vector

Sector-I:
$$\begin{bmatrix} Sa \\ Sb \\ Sc \end{bmatrix} = \begin{bmatrix} 0.5 & 1 & 1 \\ 0.5 & 1 & 0 \\ 0.5 & 0 & 0 \end{bmatrix} \begin{bmatrix} d_0 \\ d_2 \\ d_1 \end{bmatrix} = \begin{bmatrix} 0.5d_0 + d_2 + d_1 \\ 0.5d_0 + d_2 \\ 0.5d_0 \end{bmatrix} \tag{3.76}$$

Sector-II:
$$\begin{bmatrix} Sa \\ Sb \\ Sc \end{bmatrix} = \begin{bmatrix} 0.5 & 1 & 0 \\ 0.5 & 1 & 1 \\ 0.5 & 0 & 0 \end{bmatrix} \begin{bmatrix} d_0 \\ d_2 \\ d_1 \end{bmatrix} = \begin{bmatrix} 0.5d_0 + d_2 \\ 0.5d_0 + d_2 + d_1 \\ 0.5d_0 \end{bmatrix} \quad (3.77)$$

Sector-III:
$$\begin{bmatrix} Sa \\ Sb \\ Sc \end{bmatrix} = \begin{bmatrix} 0.5 & 0 & 0 \\ 0.5 & 1 & 1 \\ 0.5 & 1 & 0 \end{bmatrix} \begin{bmatrix} d_0 \\ d_2 \\ d_1 \end{bmatrix} = \begin{bmatrix} 0.5d_0 \\ 0.5d_0 + d_2 + d_1 \\ 0.5d_0 + d_2 \end{bmatrix} \quad (3.78)$$

Sector-IV:
$$\begin{bmatrix} Sa \\ Sb \\ Sc \end{bmatrix} = \begin{bmatrix} 0.5 & 0 & 0 \\ 0.5 & 1 & 0 \\ 0.5 & 1 & 1 \end{bmatrix} \begin{bmatrix} d_0 \\ d_2 \\ d_1 \end{bmatrix} = \begin{bmatrix} 0.5d_0 \\ 0.5d_0 + d_2 \\ 0.5d_0 + d_2 + d_1 \end{bmatrix} \quad (3.79)$$

Sector-V:
$$\begin{bmatrix} Sa \\ Sb \\ Sc \end{bmatrix} = \begin{bmatrix} 0.5 & 1 & 0 \\ 0.5 & 0 & 0 \\ 0.5 & 1 & 1 \end{bmatrix} \begin{bmatrix} d_0 \\ d_2 \\ d_1 \end{bmatrix} = \begin{bmatrix} 0.5d_0 + d_2 \\ 0.5d_0 \\ 0.5d_0 + d_2 + d_1 \end{bmatrix} \quad (3.80)$$

Sector-VI:
$$\begin{bmatrix} Sa \\ Sb \\ Sc \end{bmatrix} = \begin{bmatrix} 0.5 & 1 & 1 \\ 0.5 & 0 & 0 \\ 0.5 & 1 & 0 \end{bmatrix} \begin{bmatrix} d_0 \\ d_2 \\ d_1 \end{bmatrix} = \begin{bmatrix} 0.5d_0 + d_2 + d_1 \\ 0.5d_0 \\ 0.5d_0 + d_2 \end{bmatrix} \quad (3.81)$$

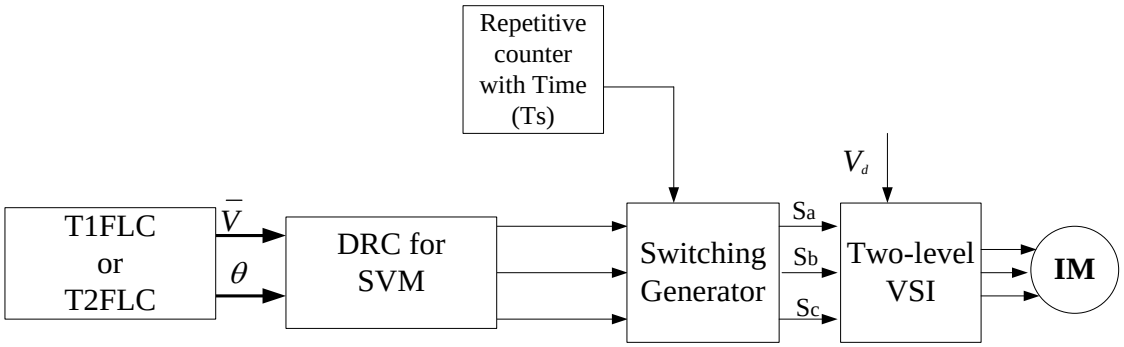


Fig. 3.13: DRC with T1FDTC or T2FDTC

Here, the duty ratios of T1FLC and T2FLC are independent of the sampling time and it can improve the quality of voltage or current waveforms under steady state by improving firing pulse of the inverter, which leads to improve the flux and torque performance of the IM drive rather than PIDTC [138]. By using Eq. (3.73) to Eq. (3.75), the SVPWM duty ratios are developed in a first sector using Eq. (3.76) for three phases. Similarly, this process will continue for the rest of five sectors to develop the duty ratios for the complete reference cycle (2π) as found from Eq. (3.77) to Eq. (3.81).

3.5.2 Hybrid Space Vector Modulation (HSVM)

The block diagram for HSVM using either T1FLC or T2FLC for DTC is shown in Fig. 3.14 in which the root mean square (RMS) value of flux ripples for three different types of switching sequences or PWMs are studied based on reference vector movement and later the corresponding pulse pattern is developed in both T1FDTC and T2FDTC using HSVM with less RMS flux ripple than the conventional PIDTC. The detail procedure is as explained below.

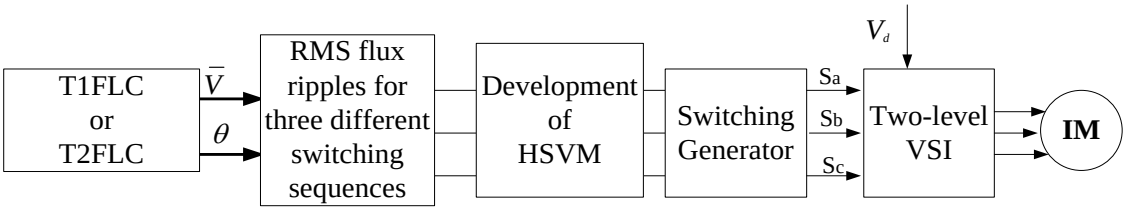


Fig. 3.14: HSVM with T1FLC or T2FLC

In the space vector approach, the applied voltage vector equals the reference voltage vector only in an average sense over the given sampling period, and not in an instantaneous fashion. The zero voltage vectors and active voltage vectors forming the boundary in the sector are used to generate this reference voltage vector, and at any instant one of the eight possible states of the inverter is always used. The difference between the reference voltage vector and the instantaneous applied voltage vector is the instantaneous voltage ripple vector. The instantaneous voltage ripple vectors for a sample positioned in the sector-I corresponding to the four possible applied vectors are as shown in Fig. 3.15. When there is a switching, the applied voltage vector is changed instantaneously and hence the voltage ripple vector is changed. Between any two consecutive switching instants, the applied voltage vector remains the same. As the reference voltage vector keeps revolving, the voltage ripple vector also keeps changing continuously with time, both in magnitude as well as angle. The voltage ripple vectors can be represented in a synchronously revolving d-q axis reference as shown in Fig. 3.15. The q-axis is in the direction of the reference voltage vector while the d-axis is 90^0 behind the q-axis. The instantaneous voltage ripple vectors in the synchronously revolving d-q reference frame corresponding to the active voltage vector V_1, active voltage vector V_2 and the zero voltage vectors are given in Eq. (3.82), Eq. (3.83) and Eq. (3.84), respectively [10],[36].

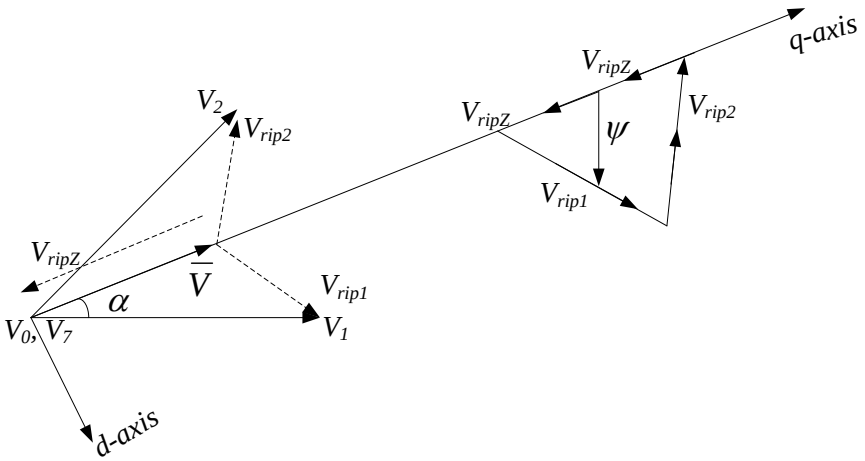


Fig 3.15: Instantaneous voltage ripple vectors along with d-q axes

$$V_{rip1} = \frac{2}{3} V_d \sin\alpha + j\left(\frac{2}{3}V_d \cos\alpha - \left|\overline{V}\right|\right) \tag{3.82}$$

$$V_{rip2} = -\frac{2}{3}V_d \sin(60-\alpha) + j\left(\frac{2}{3}V_d \cos(60-\alpha) - \left|\overline{V}\right|\right) \tag{3.83}$$

$$V_{ripz} = -j\left|\overline{V}\right| \tag{3.84}$$

The time integral of the voltage ripple vector, is referred as the ‘stator flux ripple vector’, and is a measure of ripple in the line current. At any instant within a subcycle, one of the two active voltage vectors or the zero voltage vectors is applied. When the zero voltage vector is applied, the error voltage vector is equal to the negative of the reference voltage vector to be generated. When an active voltage vector is applied, the voltage ripple vector is the vector originating from the tip of the reference voltage vector and ending at the tip of the active voltage vector applied. As the voltage ripple vector remains constant when any given vector is applied, the ripple flux vector changes at a uniform rate. The application of a zero voltage vector results in a variation of the q-axis component of the flux ripple. However, the application of any active voltage results in variation of the both the d-axis and q-axis components. The ripple/error volt-second corresponding to Eq. (3.82), Eq. (3.83), and Eq. (3.84) are given by

$$\begin{aligned} V_{rip1}T_1 &= \frac{2}{3} V_d T_1 \sin\alpha + j\left(\frac{2}{3}V_d \cos\alpha - \overline{V}\right)T_1 \\ &= D_1 + jQ_1 \end{aligned} \tag{3.85}$$

$$V_{rip2}T_2 = \left(-\frac{2}{3}V_d \sin(60° - \alpha)\right)T_2 + j\left(\frac{2}{3}V_d \cos(60° - \alpha) - \overline{V}\right)T_2 \quad (3.86)$$
$$= D_2 + jQ_2$$

$$V_{ripz} = -j\overline{V} * T_z \quad (3.87)$$
$$= jQ_z$$

where $D_1 = \left(\frac{2}{3}V_d \sin\alpha\right)T_1$, $D_2 = \left(\frac{2}{3}V_d \sin(60° - \alpha)\right)T_2$ (3.88)

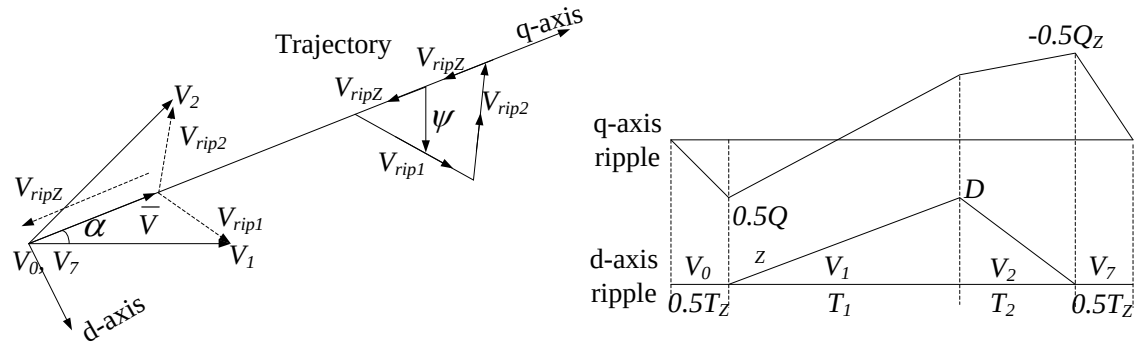
By substituting T_1 and T_2 in Eq. (3.88), we get $D_1=D_2$ and therefore $D_1=D_2=D$

$$Q_1 = \left(\frac{2}{3}V_d \cos\alpha - \overline{V}\right)T_1 \quad (3.89)$$

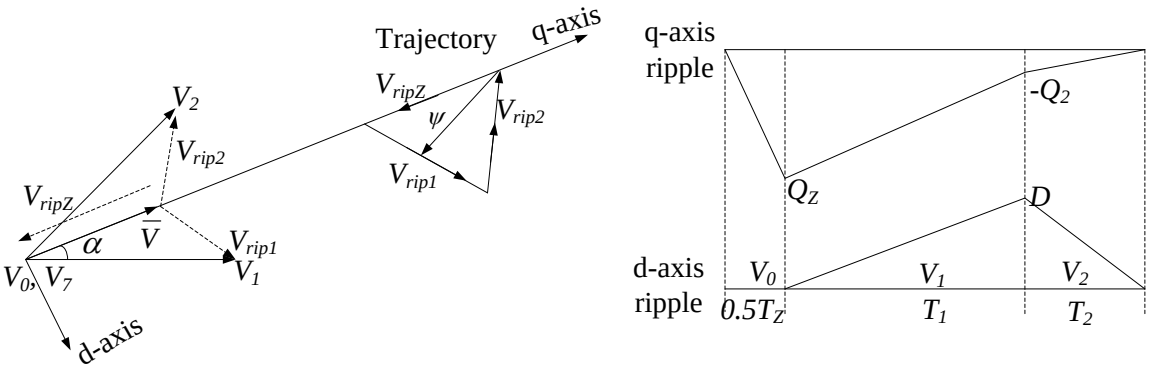
$$Q_2 = \left(\frac{2}{3}V_d \cos(60 - \alpha) - \overline{V}\right)T_2 \quad (3.90)$$

$$Qz = -\overline{V}\ T_z \quad (3.91)$$

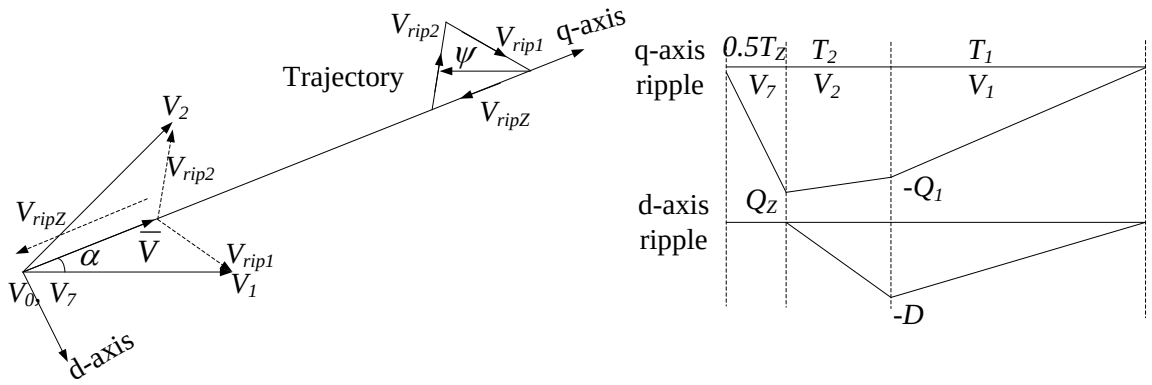
The sum expression from Eq. (3.85) to Eq. (3.87) is equated to zero, indicating the balance between applied volt-seconds and reference volt-seconds over a subcycle [34]-[36]. Volt-second balance ensures that the stator flux ripple vector starts and ends with zero magnitude in every subcycle. The variation in between these zero instants is a measure of the harmonic distortion in the 3-phase currents. This variation depends on the reference voltage generated and the switching sequence used. The mean square stator flux ripple over a subcycle corresponding to sequences (SVM, BCSVM0, and BCSVM1) is denoted by F_{seq}. The expression for mean square stator flux ripple can be derived in terms of D, Q_1, Q_2, and Q_z, which are defined in Eq. (3.88) to Eq. (3.91). The stator flux ripple has its components along the d-axis and q-axis. The d-axis ripple ($\Psi_{d(\mathrm{SVM})}$) and q-axis ripple ($\Psi_{q(\mathrm{SVM})}$) for SVM switching sequences are given in Eq. (3.92) to Eq. (3.93) as



(a) Stator flux ripple over a subcycle for SVM

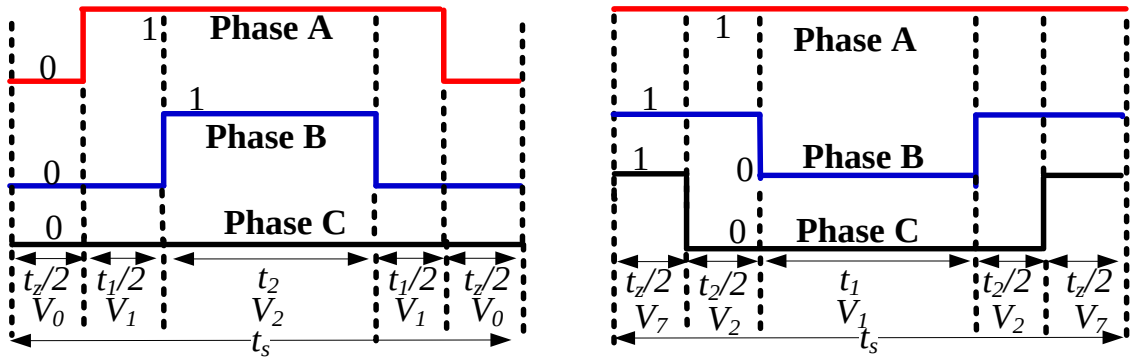


(b) Stator flux ripple over a subcycle for BCSVM0



(c) Stator flux ripple over a subcycle for BCSVM1

Fig 3.16: Stator flux ripple over a subcycle for alternative PWM techniques



(a) Pulse pattern for BCSVM0, (b) Pulse pattern for BCSVM1

Fig. 3.17: Pulse pattern for BCSVM0 and BCSVM1 techniques

$$\Psi_{q(SVM)} = \frac{Q_z t}{T_z}, \qquad \text{if } 0 \le t \le 0.5T_z$$

$$= 0.5Q_z + \frac{Q_1 t_1}{T_1}, \qquad \text{if } 0.5T_z \le t \le (0.5T_z + T_1)$$

$$= 0.5Q_z + Q_1 + \frac{Q_2 t_2}{T_2}, \quad \text{if } (0.5T_z + T_1) \le t \le (T_s - 0.5T_z)$$

$$= 0.5Q_z + \frac{Q_z t_3}{T_z}, \qquad \text{if } (T_s - 0.5T_z) \le t \le T_s \tag{3.92}$$

$$\Psi_{d(SVM)} = 0, \qquad \text{if } 0 \le t \le 0.5T_z$$

$$= \frac{Dt_1}{T_1}, \qquad \text{if } 0.5T_z \le t \le (0.5T_z + T_1)$$

$$= D - \frac{Dt_2}{T_2}, \quad \text{if } (0.5T_z + T_1) \le t \le (T_s - 0.5T_z)$$

$$= 0, \qquad \text{if } (T_s - 0.5T_z) \le t \le T_s \tag{3.93}$$

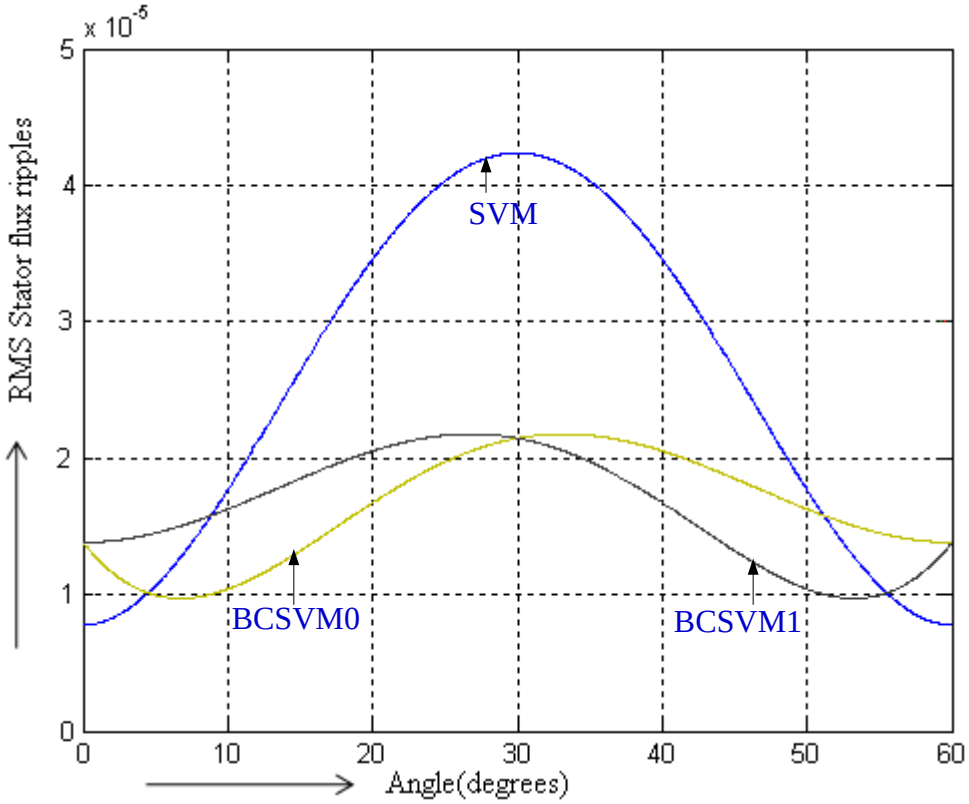
where $t_1 = t - 0.5T_z$; $t_2 = t - 0.5T_z - T_1$; $t_3 = t - 0.5T_z - T_1 - T_2$;

From Fig. 3.16(a), the mean square stator flux ripple over a subcycle for SVM sequence can be calculated as [36]-[38]

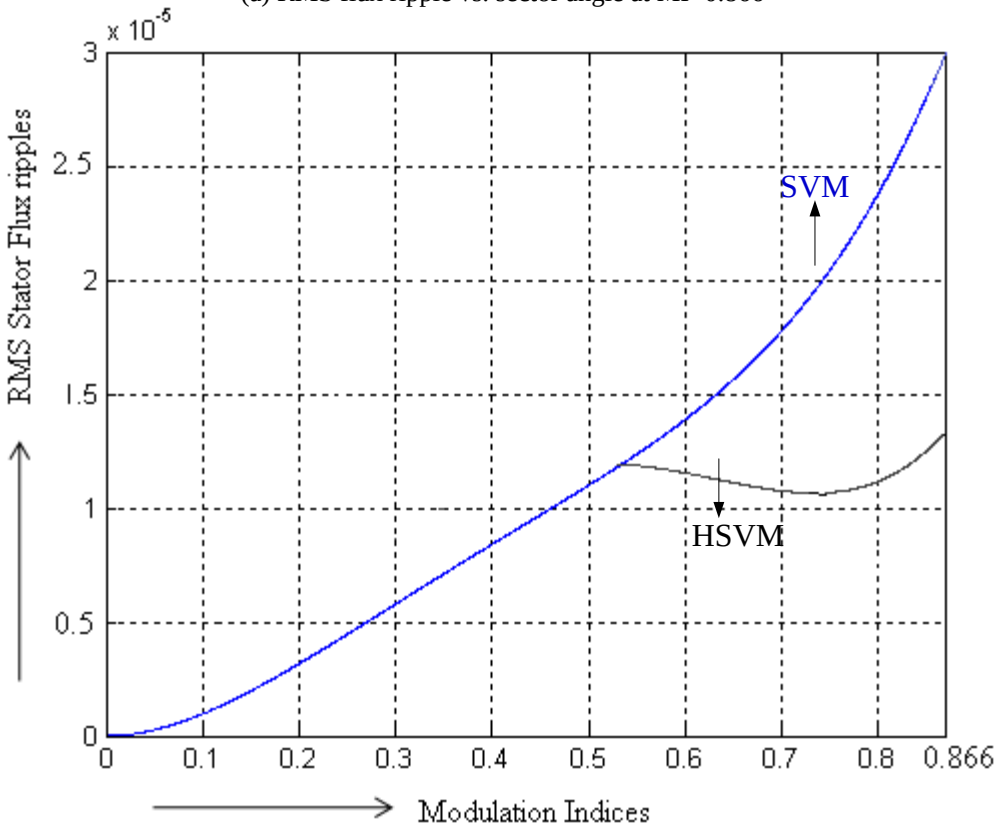
$$F_{SVM}^2 = \frac{1}{T_s}\int_0^{T_s} \psi_{q(SVM)}^2 dt + \frac{1}{T_s}\int_0^{T_s} \psi_{d(SVM)}^2 dt \tag{3.94}$$

$$\begin{aligned} F_{SVM}^2 = {} & \frac{1}{T_s}\int_{t=0}^{0.5T_z}\left(\frac{Q_z t}{T_z}\right)^2 dt + \frac{1}{T_s}\int_{t_1=0}^{T_1}\left(0.5Q_z + \frac{Q_1 t_1}{T_1}\right)^2 dt_1 \\ & + \frac{1}{T_s}\int_{t_2=0}^{T_2}\left(0.5Q_z + Q_1 + \frac{Q_2 t_2}{T_2}\right)^2 dt_2 \\ & + \frac{1}{T_s}\int_{t_3=0}^{0.5T_z}\left(-0.5Q_z + \frac{Q_z t_3}{T_z}\right)^2 dt_3 \\ & + \frac{1}{T_s}\int_{t_1=0}^{T_1}\left(\frac{Dt_1}{T_1}\right)^2 dt_1 + \frac{1}{T_s}\int_{t_2=0}^{T_2}\left(D - \frac{Dt_2}{T_2}\right)^2 dt_2 \end{aligned} \tag{3.95}$$

By simplifying the Eq. (3.95), the mean square stator flux ripple for the conventional SVM over a subcycle can be obtained as



(a) RMS flux ripple vs. sector angle at MI=0.866



(b) RMS stator flux ripple vs. MI

Fig. 3.18: RMS flux ripple performance of the IM drive

$$F_{SVM}^{2} = \frac{1}{3}\left(0.5Q_z\right)^2 \frac{T_z}{2T_s} + \frac{1}{3}\left[\left(0.5Q_z\right)^2 + 0.5Q_z\left(0.5Q_z + Q_1\right) + \left(0.5Q_z + Q_1\right)^2\right]\frac{T_1}{T_s} +$$
$$\frac{1}{3}\left[\left(0.5Q_z + Q_1\right)^2 - \left(0.5Q_z + Q_1\right)\left(0.5Q_z\right) + \left(-0.5Q_z\right)^2\right]\frac{T_2}{T_s} + \quad (3.96)$$
$$\frac{1}{3}\left(-0.5Q_z\right)^2 \frac{T_z}{2T_s} + \frac{1}{3}D^2\frac{\left(T_1 + T_2\right)}{T_s}$$

In general, with the bus clamped space vector modulation (BCSVM), only one zero voltage vector (either V_0 (000) or V_7 (111)) is considered instead of two zero vectors. As a result, there is no change in the switching state of one of the switches in a particular phase over a switching period and it remains clamped to either positive (with the zero voltage V_7 (111) only) or negative DC bus (with the zero voltage V_0 (000) only) [39],[34]. Hence, this is known as BCSVM. Because of the manipulation of zero voltage vectors in a switching period, one phase of the inverter remains un-modulated for the duration of one switching period. Therefore, the number of switchings is condensed to two third as compared to the conventional SVM. The Table-3.5 shows the sequences in all the sectors for BCSVM0 and BCSVM1. The pulse pattern for both BCSVM0 and BCSVM1 for 3-phase inverter is developed in a sector-1 region using Eq. (3.43) to Eq. (3.46) and Table 3.5 as shown in Fig. 3.17 (a) and Fig. 3.17 (b), respectively.

Table 3.5: Selection of switching sequences for BCSVM0 and BCSVM1 in all sectors

Sector No's	**BCSVM0 Sequence**		**BCSVM1 Sequence**	
	1st half	**2nd half**	**1st half**	**2nd half**
1	$V_0V_1V_2$	$V_2V_1V_0$	$V_7V_2V_1$	$V_1V_2V_7$
2	$V_0V_3V_2$	$V_2V_3V_0$	$V_7V_2V_3$	$V_3V_2V_7$
3	$V_0V_3V_4$	$V_4V_3V_0$	$V_7V_4V_3$	$V_3V_4V_7$
4	$V_0V_5V_4$	$V_4V_5V_0$	$V_7V_4V_5$	$V_5V_4V_7$
5	$V_0V_5V_6$	$V_6V_5V_0$	$V_7V_6V_5$	$V_5V_6V_7$
6	$V_0V_1V_6$	$V_6V_1V_0$	$V_7V_6V_1$	$V_1V_6V_7$

As similar to SVM, the mean square stator flux ripples can be calculated for BCSVM0 and BCSVM1 with the help of Fig. 3.16 (b) and Fig. 3. 16(c), respectively as given below

$$F_{BCSVM0}^{2} = \frac{4}{27}Q_z^2\frac{T_z}{T_s} + \frac{4}{27}\left[Q_z^2 + Q_z\left(Q_z + Q_1\right) + \left(Q_z + Q_1\right)^2\right]\frac{T_1}{T_s}$$
$$+ \frac{4}{27}\left(Q_z + Q_1\right)^2\frac{T_2}{T_s} + \frac{4}{27}D^2\frac{\left(T_1 + T_2\right)}{T_s} \quad (3.97)$$

$$F_{BCSVM1}^2 = \frac{4}{27}Q_z^2\frac{T_z}{T_s} + \frac{4}{27}\left[Q_z^2 + Q_z\left(Q_z + Q_2\right) + \left(Q_z + Q_2\right)^2\right]\frac{T_2}{T_s} + \frac{4}{27}\left(Q_z + Q_2\right)^2\frac{T_1}{T_s} + \frac{4}{27}D^2\frac{\left(T_1 + T_2\right)}{T_s} \quad (3.98)$$

The RMS stator flux ripple over a subcycle corresponding to SVM, BCSVM0, and BCSVM1 are given in Eq. (3.96) Eq. (3.97) and, Eq. (3.98), respectively. The sector angle vs. RMS flux ripple of the IM drive for three sequences at MI of 0.866 is shown in Fig. 3.18 (a) in which the three sequences are employed for different flux ripple at different instants. Hence, HSVM provides less average RMS flux ripples by operating the lowest flux ripple of the PWMs at each and every instant of the sector angle. Also, Fig. 3.18 (b) shows the MI vs. RMS flux ripple in which the HSVM provides less RMS flux ripple than SVM when the MI is more than 0.55. Moreover, the HSVM also improves the voltage, current, and torque ripples of the IM as compared to SVM, which is explained detail in results and discussion.

3.5.3 Total Harmonic Distortion (THD)

Let *X* be the waveform of either voltage or current. The total harmonic distortion (*THD*) is defined as the ratio of the sum of the RMS amplitude of the harmonic contents in *X* (X_h) to the RMS amplitude of fundamental (X_1) value such as [41]

$$\%\,(THD_x) = \left\lceil \sqrt{\sum_{n=1}^{n}\left(X_n^2\right) - X_1^2} \Big/ X_1 \right\rceil \times 100 \quad (3.99)$$

$$\%\,X_{THD} = \left(X_h / X_1\right) \times 100 \quad (3.100)$$

From (3.99) to (3.100), the *THD* is directly proportional to the sum of harmonic content (X_h) and it is inversely proportional to the fundamental value of voltage or current waveform (X_1) of the IM. Hence, as the harmonic content in the waveform increases then the *THD* also increases [40].

3.6 Overall efficiency of the IM drive

The ratio of the mechanical power to the actual input power fed by the inverter is known as the overall efficiency of the IM drive, which can be expressed as

$$\eta = \frac{P_m}{P_{inv}} = \frac{T_e\omega_m}{I_{inv}V_d} \quad (3.101)$$

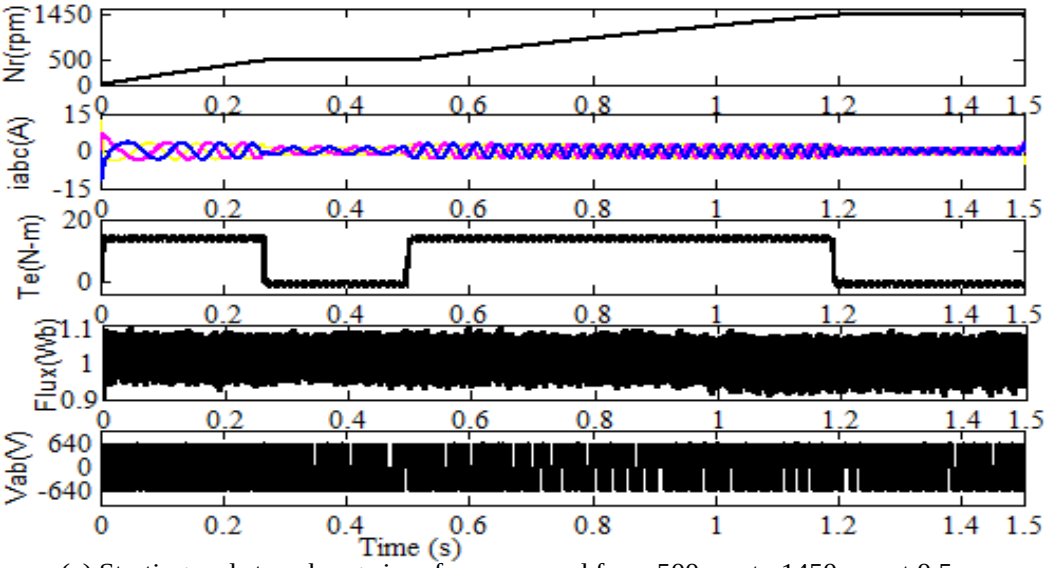
where P_m and P_{in} are the mechanical output power provided by the IM and the input power of the inverter, and I_{inv} and V_d are the average values of input current and voltage of the inverter, respectively.

3.7 Results and Discussion

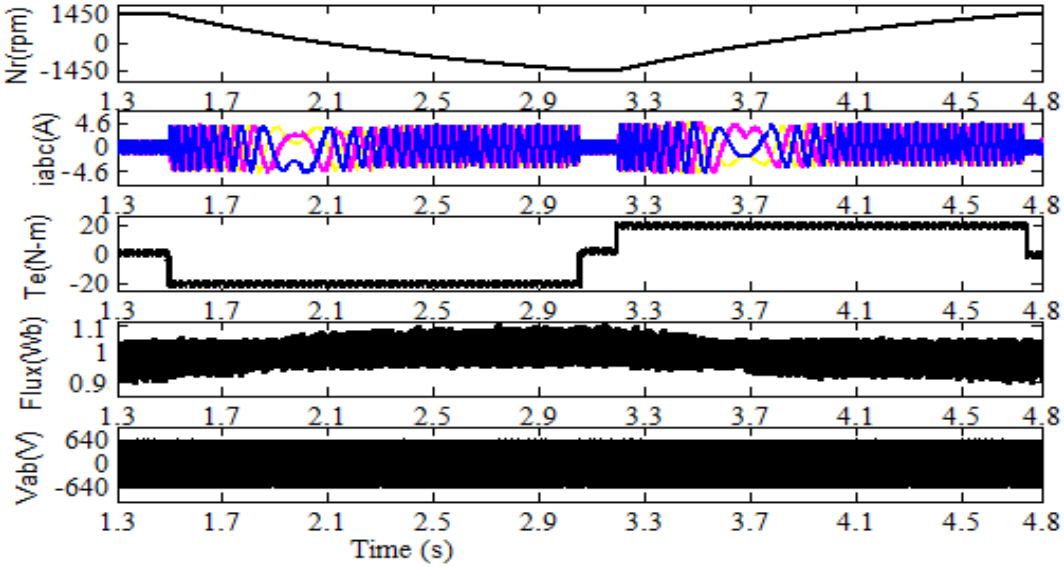
3.7.1 Simulation Results

The PIDTC is simulated in MATLAB using a two-level SVM inverter with the switching frequency of 5 kHz, and the sampling time of 40μs for 2HP IM. The reference speed during starting is taken as 500rpm, and subsequently a step change in reference speed from 500 rpm to 1450 rpm is initiated at 0.5s with the applied DC-link voltage of 640V as shown in Fig. 3.19 (a) and the rest of the parameters are mentioned at Appendix A1. Initially, a rotating flux is developed in stator because of the supply provided by the inverter. Consequently, the high starting torque and currents are developed and later speed is built up by the motor to run up to a required speed. The IM is settled at 0.25s when applied a reference speed of 500rpm at starting and the corresponding performance of the IM such as speed, three phase current, electromagnetic torque developed by the motor, stator flux, and line voltage of the inverter are shown in Fig. 3.19 (a). However, the line voltage and flux are almost the same from starting to the steady state. Moreover, the flux distortion is varied from 0.9Wb to 1.1Wb, i.e., ±0.1Wb. When a reference speed of IM drive changes from 500rpm to 1450rpm at 0.5s, the IM is settled at 1.2s and the corresponding IM current, torque, speed, line voltage, and flux are shown in Fig. 3.19 (a).

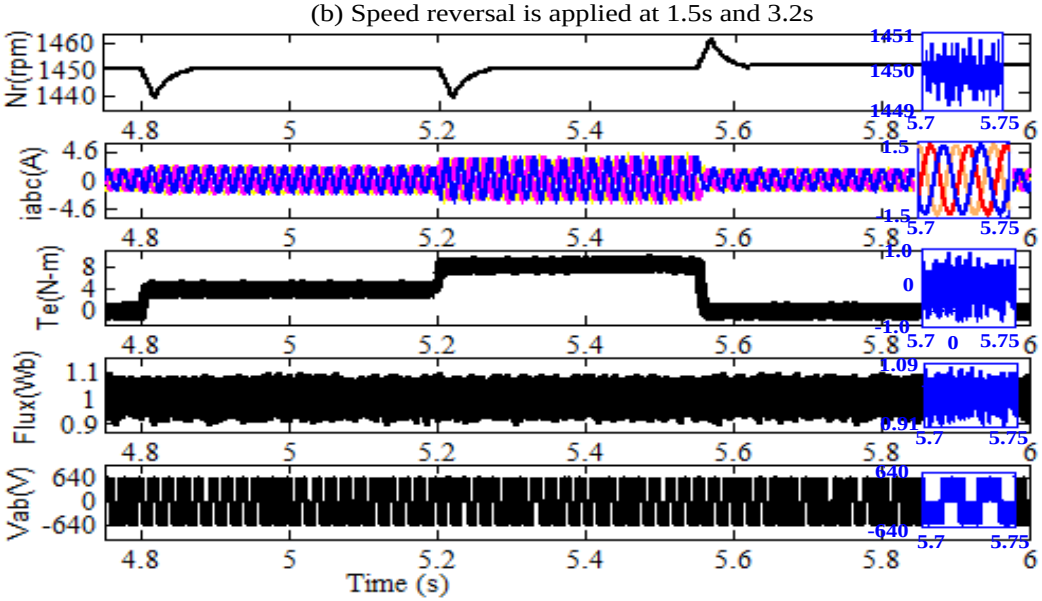
When the speed reversal is initiated at 1.5s, then the IM behavior is shown in Fig. 3.19 (b). To get required speed of -1450rpm, a larger amplitude of the current (5A) and high torque of -20Nm are developed during speed reversal. Moreover, the current directions also get reversed when the speed crosses to zero value and the IM is settled to -1450rpm at approximately 3.13s as shown in Fig. 3.19 (b). Now, the speed reversal is initiated again for PIDTC of IM at 3.2s then the corresponding operation of the IM is shown in Fig. 3.19 (b), which clearly shows a mirror image to the previous case (for the duration of 1.5s to 3.1s) of the IM drive. Consequently, the steady state of the IM is reached by 4.746s.



(a) Starting and step change in reference speed from 500rpm to 1450rpm at 0.5s

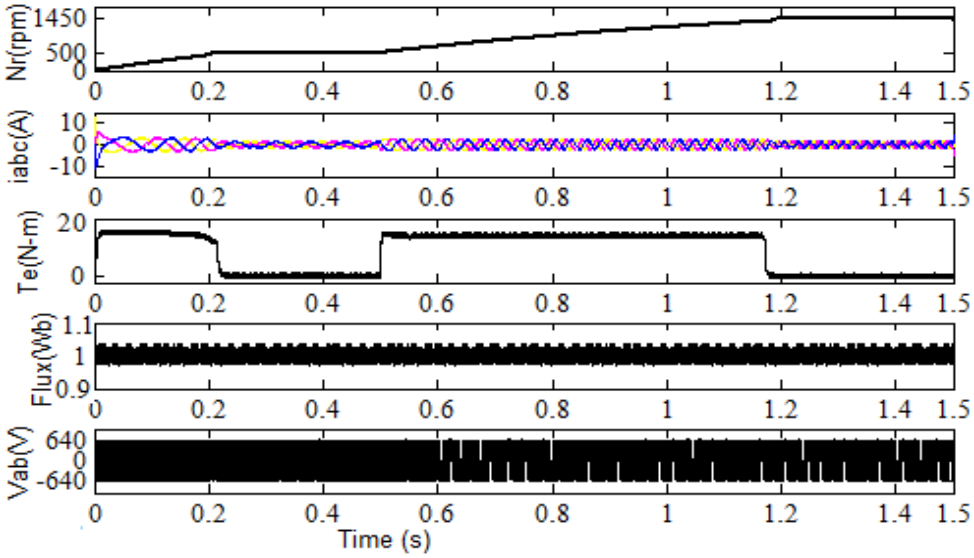


(b) Speed reversal is applied at 1.5s and 3.2s

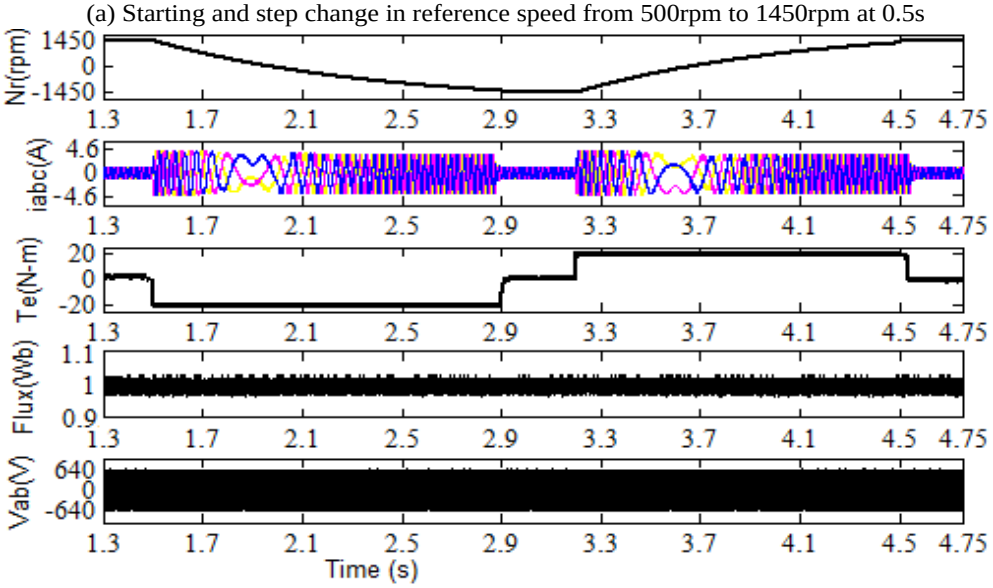


(c) Load of 4N-m, 8N-m, and 0N-m is applied at 4.8s 5.2s and 5.55s

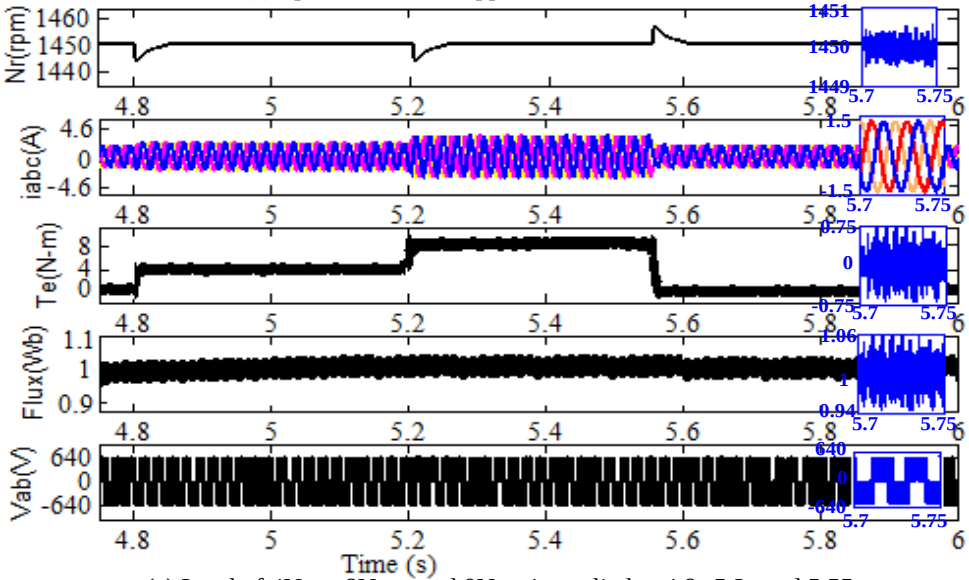
Fig. 3.19: PIDTC of IM drive under different operating modes



(a) Starting and step change in reference speed from 500rpm to 1450rpm at 0.5s

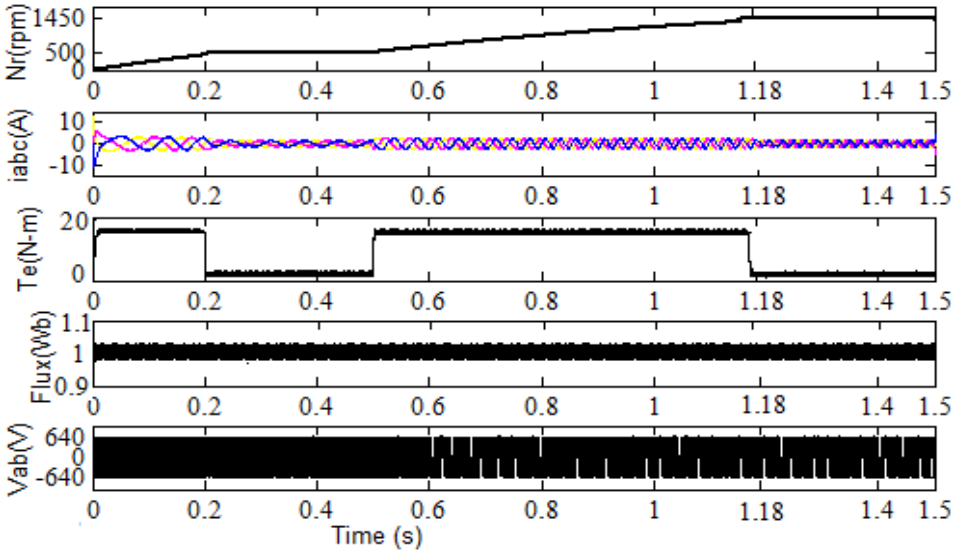


(b) Speed reversal is applied at 1.5s and 3.2s

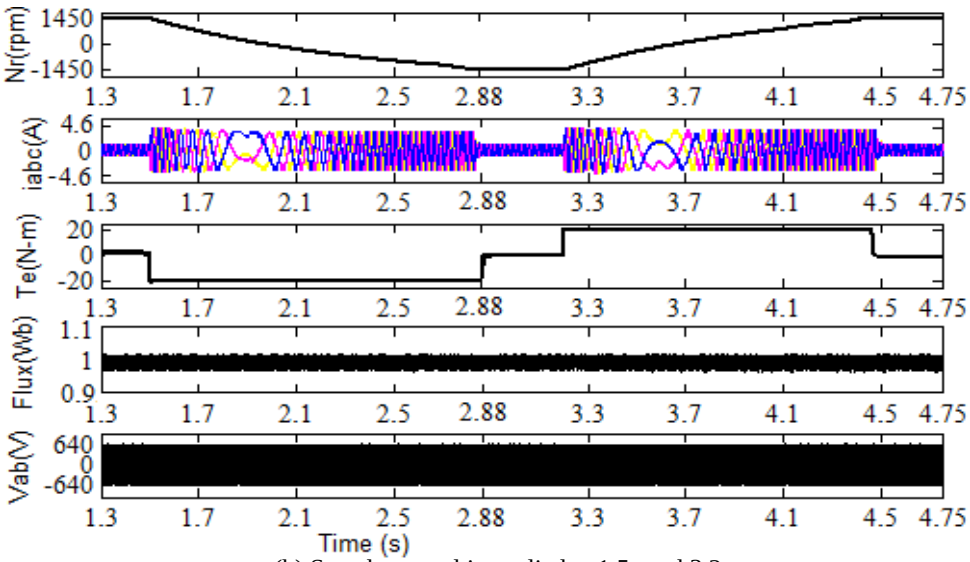


(c) Load of 4N-m, 8N-m, and 0N-m is applied at 4.8s 5.2s and 5.55s

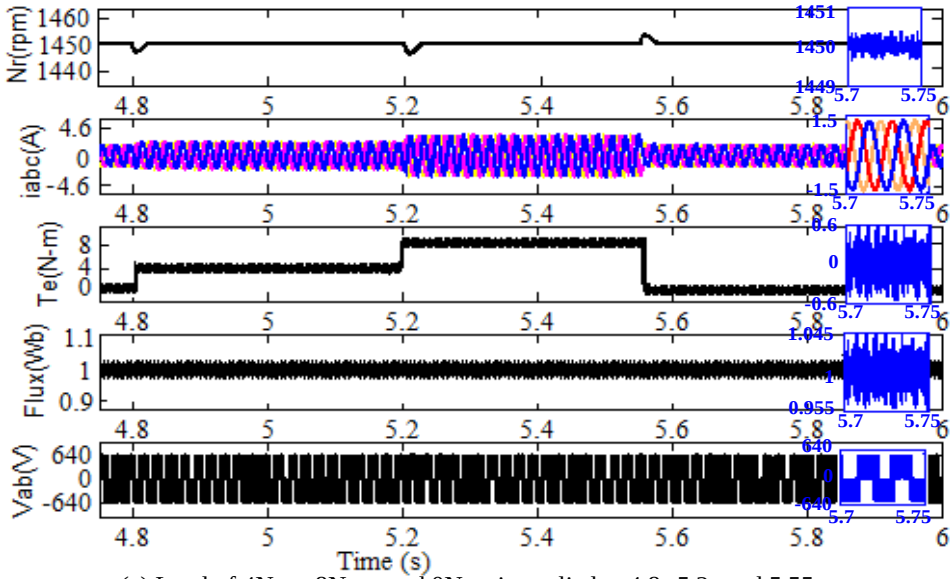
Fig. 3.20: T1FDTC along with DRC of IM drive under different operating modes



(a) Starting and step change in reference speed from 500rpm to 1450rpm at 0.5s

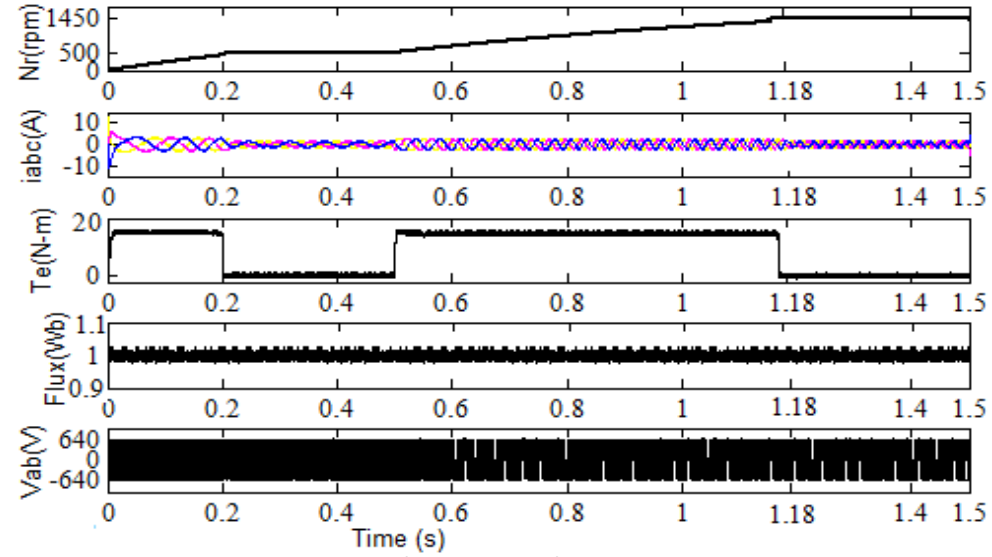


(b) Speed reversal is applied at 1.5s and 3.2s

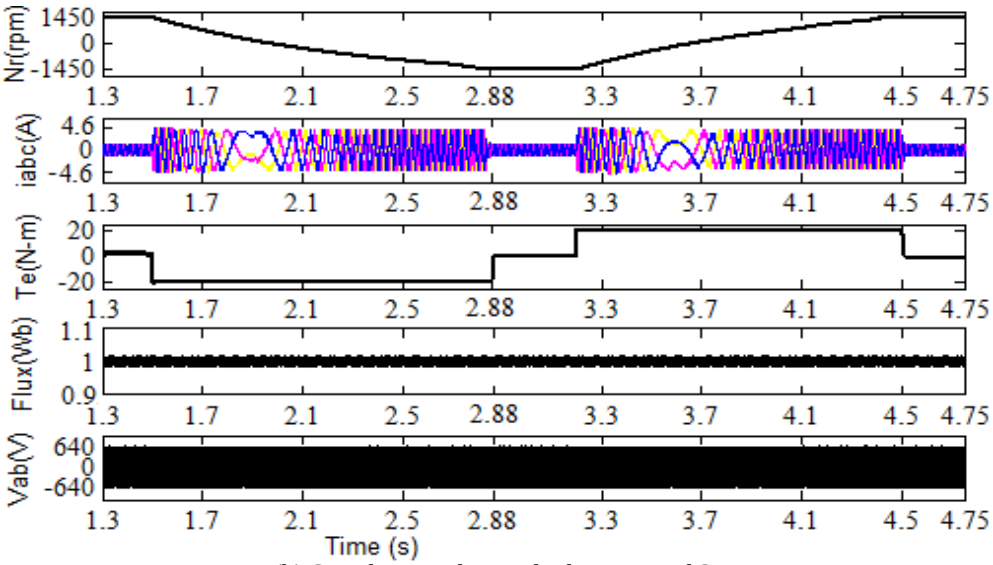


(c) Load of 4N-m, 8N-m, and 0N-m is applied at 4.8s 5.2s and 5.55s

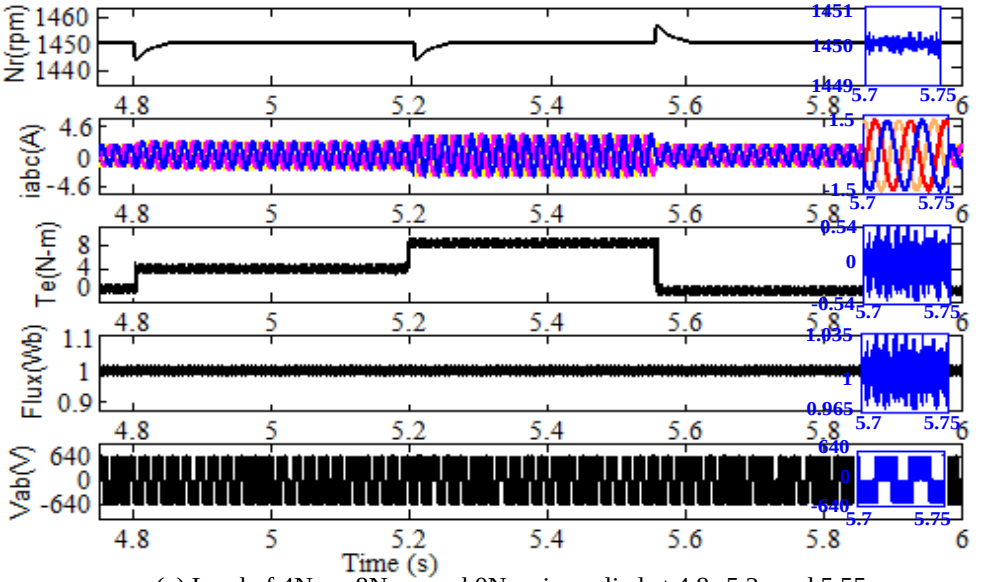
Fig. 3.21: T1FDTC along with HSVM of IM drive under different operating modes



(a) Starting and step change in reference speed from 500rpm to 1450rpm at 0.5s

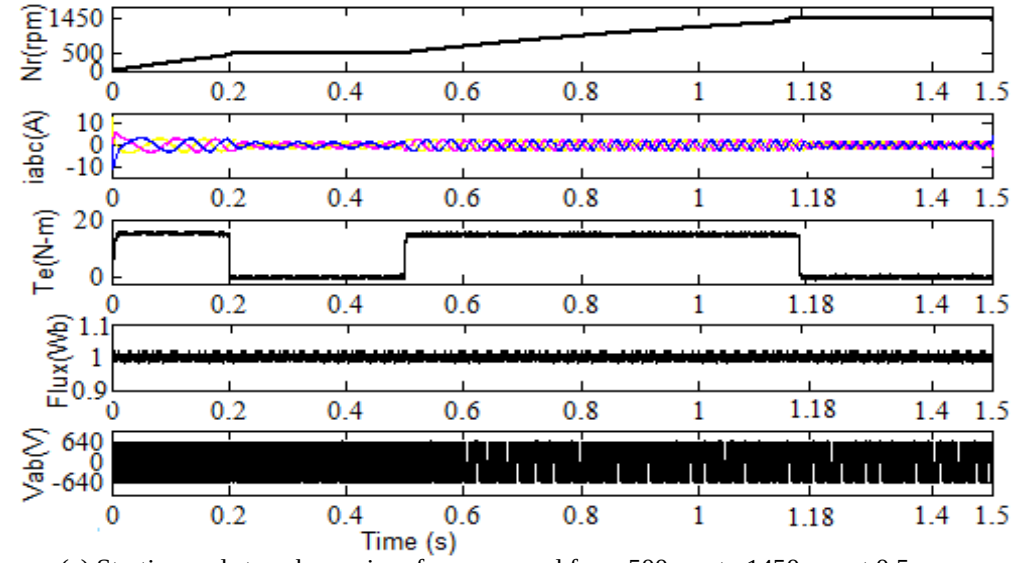


(b) Speed reversal is applied at 1.5s and 3.2s

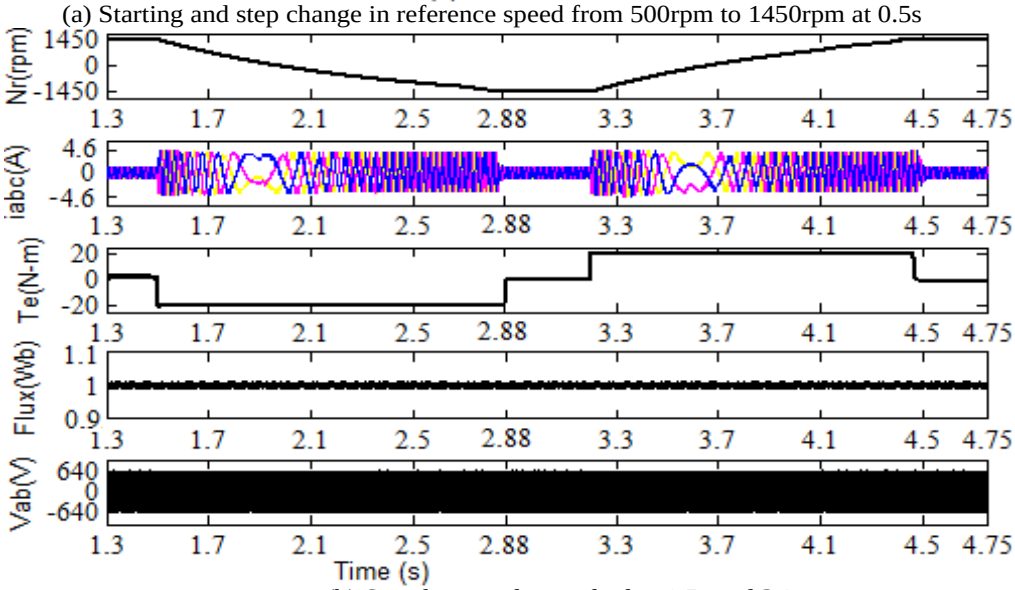


(c) Load of 4N-m, 8N-m, and 0N-m is applied at 4.8s 5.2s and 5.55s

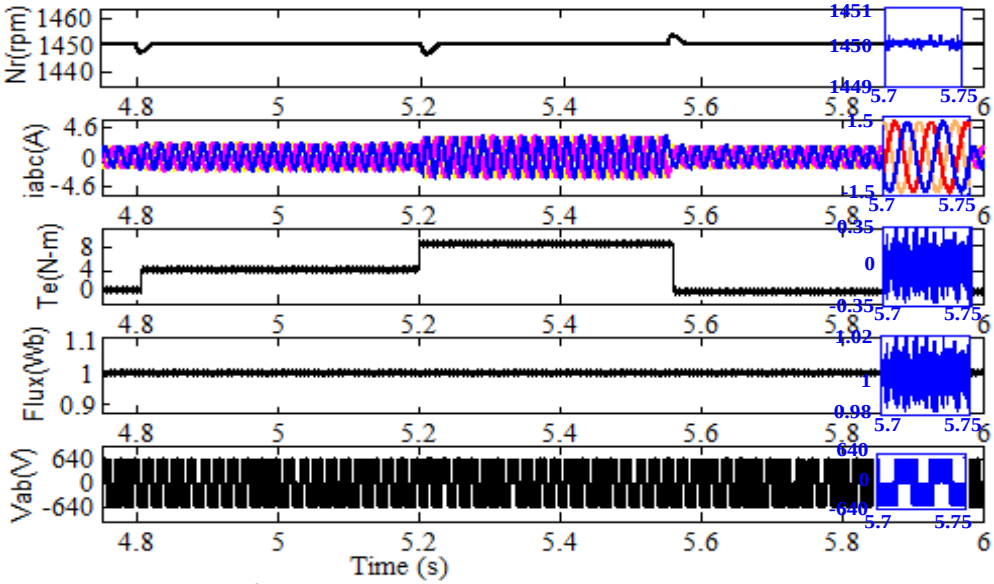
Fig. 3.22: T2FDTC along with DRC of IM drive under different operating modes



(a) Starting and step change in reference speed from 500rpm to 1450rpm at 0.5s



(b) Speed reversal is applied at 1.5s and 3.2s



(c) Load of 4N-m, 8N-m, and 0N-m is applied at 4.8s 5.2s and 5.55s

Fig. 3.23: T2FDTC along with HSVM of IM drive under different operating modes

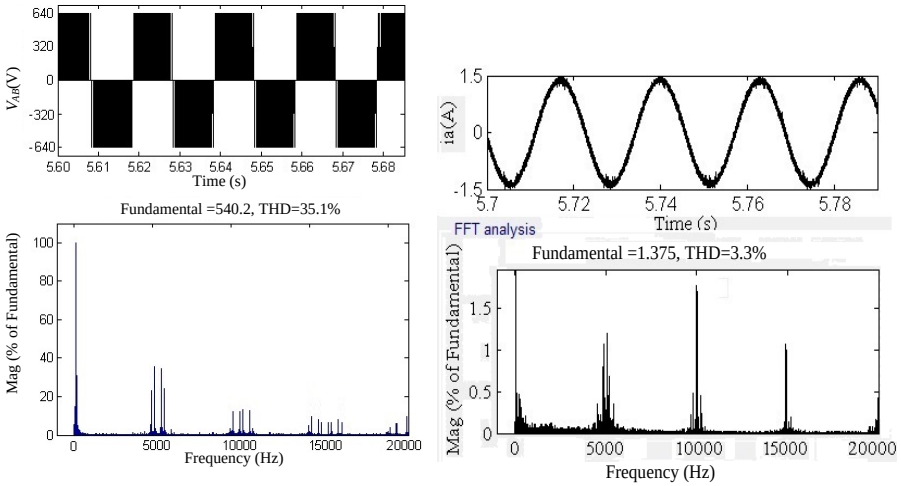
The load of 4 N-m, 8 N-m, and 0 N-m is applied to the IM at 4.75s, 5.2s and 5.55s, respectively as shown in Fig. 3.19 (c). The peak currents at above-mentioned instants are 2.2A, 2.9A, and 1.5A, respectively. As a result, there is a sudden change in speed approximately ±10rpm for every change in load torque. However, the electromagnetic torque and flux distortion of an IM drive under no-load condition vary by approximately of ±1.0Nm and ±0.1Wb, respectively as shown in Fig. 3.19 (c).

T1FDTC with DRC: With the similar operating conditions of PIDTC, the performance of the IM drive is also simulated for T1FDTC with DRC as shown in Fig. 3.20. Fig. 3.20 (a) shows the performance of the IM during starting while applying reference speed of 500rpm and step change in reference speed from 500rpm to 1450rpm at 0.5s. The IM provides reduced amplitude of starting current of 10A using T1FDTC with DRC than PIDTC. The T1FDTC of IM along with DRC settles at 0.21s and 1.18s during starting and step change in speed, respectively and hence the steady state of the IM is quickly reached before 2-3 cycles as compared to PIDTC. When the speed reversal is initiated at the same instants as that of PIDTC using T1FDTC with DRC then; the corresponding waveforms (speed, currents, torque, flux, and line voltage) of the IM are shown in Fig. 3.20 (b). The TIFDTC of IM with DRC is quickly reached to the steady state at 2.9s and 4.51s during the speed reversal as compared to PIDTC, respectively. The same loads (4Nm, 8Nm, and 0Nm) as applied with PIDTC are also applied to T1FDTC with DRC of IM at the same instants (4.5s, 5s, and 5.5s) as shown in Fig. 3.20 (c). The no-load flux ripples, the torque distortion, and speed fluctuation at load perturbation are reduced to 0.06Wb, 0.75N-m, and 5rpm, respectively as compared to PIDTC. Also, T1FDTC along with DRC provides faster dynamic response than PIDTC during starting, step changes in speed, speed reversal, and load perturbation.

T1FDTC with HSVM: The performance of the IM drive using T1FDTC along with HSVM is also simulated and corresponding waveforms are shown in Fig. 3.21 under the similar operating conditions of PIDTC. Fig. 3.21 (a) shows the performance of the IM during starting when applied the reference speed of 500rpm and a step change in the reference speed from 500rpm to 1450rpm at 0.5s. The IM provides a less amplitude of starting current of 10A using T1FDTC with HSVM than PIDTC. It settles at 0.2s and 1.173s during starting and step change in speed, respectively. Hence, the steady state of the IM is quickly reached before 2-3 cycles as compared to PIDTC. In addition, the speed

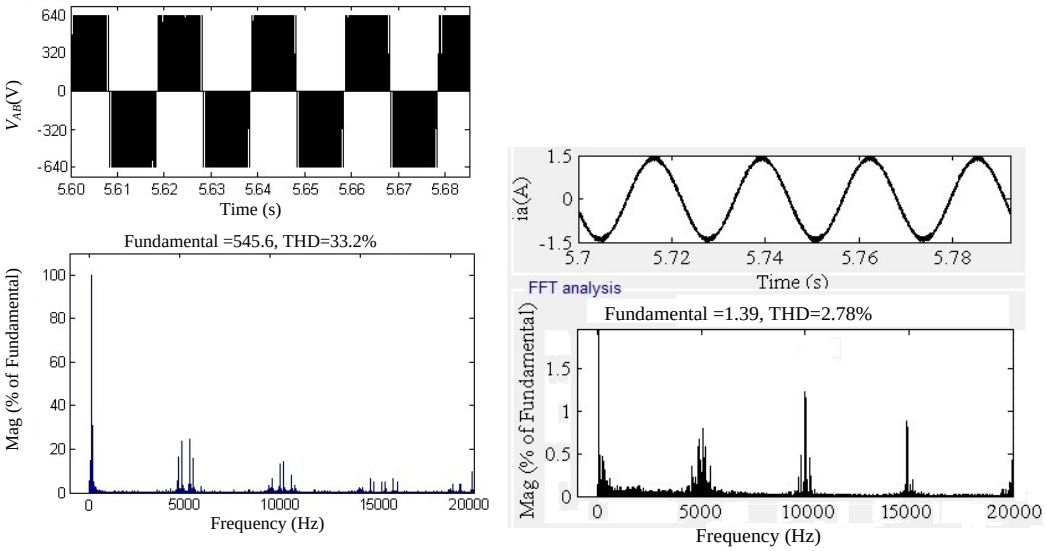
reversal is initiated at the same instants as that of PIDTC then; the corresponding waveforms (speed, currents, torque, flux, and line voltage) of the IM are shown in Fig. 3.21 (b). The TIFDTC of IM with HSVM is quickly reached to the steady state at 2.88s and 4.5s during the speed reversal as compared to PIDTC, respectively. The same loads (4Nm, 8Nm, and 0Nm) as applied with PIDTC are also applied to T1FDTC with HSVM of IM at the same instants (4.5s, 5s, and 5.5s) as shown in Fig. 3.21 (c). The no-load flux ripples and the torque distortion, and speed fluctuation at load perturbation are reduced to 0.045Wb, 0.6N-m, and 4.5rpm, respectively as compared to PIDTC and T1FDTC with DRC. Also, T1FDTC along with HSVM provides the fast dynamic response than PIDTC during starting, step changes in speed, speed reversal, and load perturbation.

T2FDTC with DRC: The performance of the IM drive using T2FDTC along with DRC is simulated and the corresponding waveforms are shown in Fig. 3.22 under the similar operating conditions of PIDTC. When the reference speed of 500rpm is applied at starting then the IM is settled at 0.2s as shown in Fig. 3.22 (a). Later, a step change in the reference speed of 1450rpm is applied to T2FDTC with DRC at 0.5s, the IM settles at 1.172s as shown in Fig. 3.22 (a). The IM draws less amplitude of starting current of 10A using T2FDTC with DRC than PIDTC. In addition, the speed reversal is initiated the same instants of PIDTC using T2FDTC with DRC then; the corresponding waveforms (speed, currents, torque, flux, and line voltage) of the IM are shown in Fig. 3.22 (b). The T2FDTC of IM with DRC is quickly reached to the steady state at 2.87s and 4.48s during the speed reversal as compared to PIDTC, respectively. The same loads (4Nm, 8Nm, and 0Nm) as applied with PIDTC are also applied to T2FDTC with DRC of IM at the same instants (4.5s, 5s, and 5.5s) as shown in Fig. 3.22 (c). The no-load flux ripples and the torque distortion, and speed fluctuation at load perturbation are reduced to 0.035Wb, 0.54N-m, and 4rpm, respectively as compared to PIDTC and T1FDTC with DRC. Also, T2FDTC along with DRC provides the fast dynamic response than PIDTC during starting, step changes in speed, speed reversal, and load perturbation.



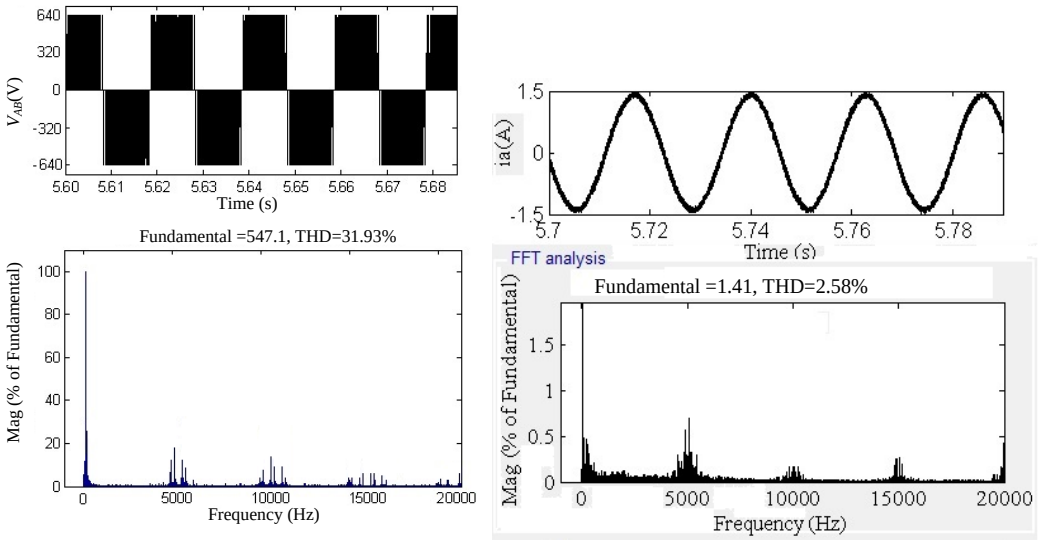
(a) Voltage THD (b) Current THD

Fig. 3.24: THD performance for the PIDTC of IM during No-load



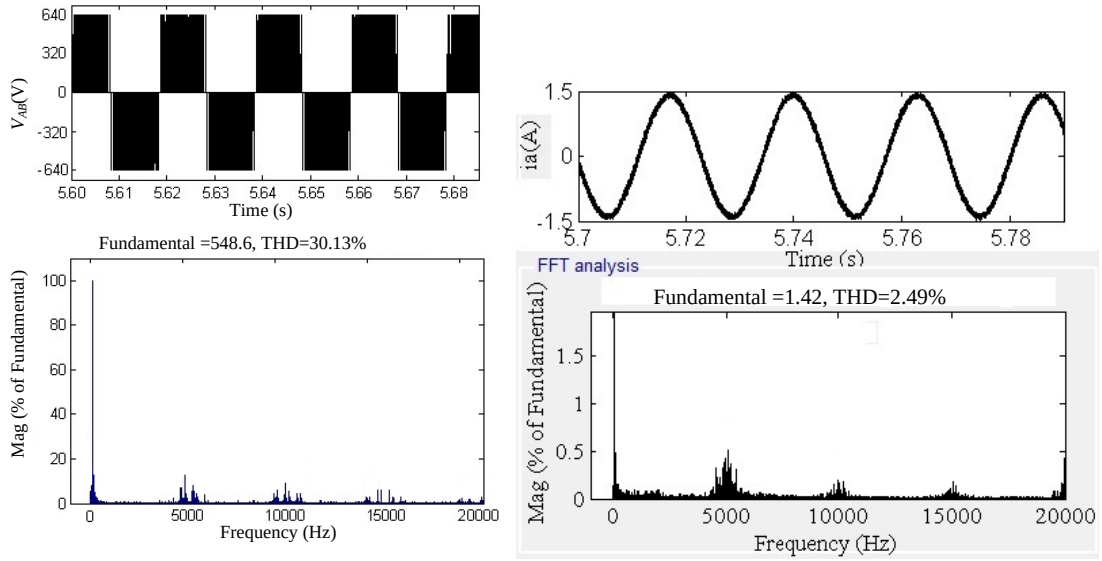
(a) Voltage THD (b) Current THD

Fig. 3.25: THD performance for the T1FDTC with DRC of IM during No-load



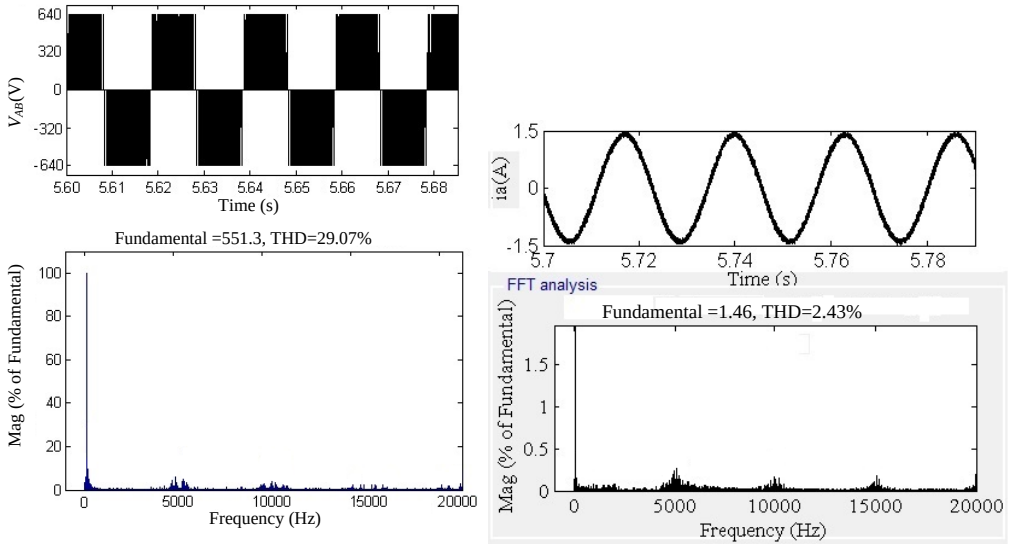
(a) Voltage THD (b) Current THD

Fig. 3.26: THD performance for the T1FDTC with HSVM of IM during No-load



(a) Voltage THD (b) Current THD

Fig. 3.27: THD performance for the T2FDTC with DRC of IM during No-load



(a) Voltage THD (b) Current THD

Fig. 3.28: THD performance for the T2FDTC with HSVM of IM during No-load

T2FDTC with HSVM: The performance of the IM drive using T2FDTC along with HSVM is also simulated and corresponding waveforms are shown in Fig. 3.23 under the similar operating condition. Fig. 3.23 (a) shows the performance of the IM during starting when applied the reference speed of 500rpm then the IM settles to 500rpm at 0.2s. Afterward, a step change in the reference speed of 1450rpm is applied to T2FDTC of IM at 0.5s. As a result, the IM quickly settles to 1450rpm at 1.173s as compared to PIDTC. In addition, IM draws reduced amplitude of starting current of 10A than PIDTC. Hence, the steady state of the IM is quickly reached before 2-3 cycles as compared to PIDTC. Now, a speed reversal is initiated at the same instants of PIDTC using T2FDTC with HSVM then, the corresponding waveforms (speed, currents, torque, flux, and line voltage) of the

IM are shown in Fig. 3.23 (b). The TIFDTC of IM with HSVM is quickly reached to the steady state at 2.868s and 4.478s during the speed reversal as compared to PIDTC, respectively. The same loads (4Nm, 8Nm, and 0Nm) as applied with PIDTC are also applied to T2FDTC with HSVM of IM at the same instants (4.5s, 5s, and 5.5s) as shown in Fig. 3.23 (c). The no-load flux ripples and the torque distortion, and speed fluctuation at load perturbation are reduced to 0.02Wb, 0.35N-m, and 4rpm, respectively as compared to PIDTC and T1FDTC with DRC. In addition, T2FDTC along with HSVM provides the fast dynamic response than PIDTC during starting, step changes in speed, speed reversal, and load perturbation.

Table 3.6: Simulated THD comparison for different control schemes

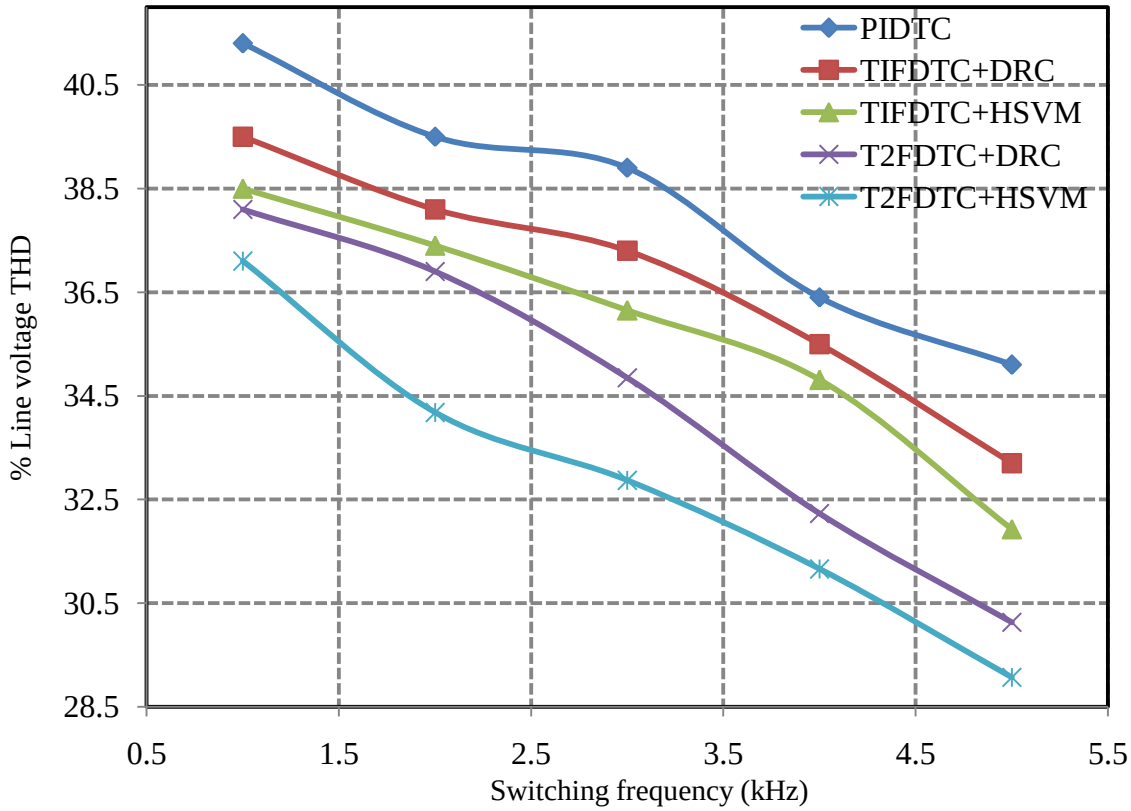
S.No.	f_{sw} (kHz)	$\%V_{THD}$					$\%i_{THD}$				
		PIDTC	TIFDTC		T2FDTC		PIDTC	TIFDTC		T2FDTC	
			DRC	HSVM	DRC	HSVM		DRC	HSVM	DRC	HSVM
No-Load											
1	1	41.3	39.5	38.5	38.1	37.1	5.2	4.72	4.52	4.2	4.12
2	2	39.5	38.1	37.4	36.9	34.18	4.9	4.45	4.15	3.95	3.75
3	3	38.9	37.3	36.15	34.85	32.87	4.1	3.78	3.41	3.35	3.24
4	4	36.4	35.5	34.81	32.23	31.16	3.7	3.53	3.36	3.18	2.95
5	5	35.1	33.2	31.93	30.13	29.07	3.3	2.78	2.58	2.49	2.43
Full-Load											
1	1	37.2	36.1	34.25	33.21	32.03	4.3	3.5	3.26	3.18	2.9
2	2	36.3	34.55	33.41	32.14	30.98	4.1	3.13	2.95	2.81	2.7
3	3	35.4	33.19	32.42	31.71	29.39	3.4	2.97	2.8	2.65	2.55
4	4	32.24	31.79	29.79	28.15	27.32	3.1	2.7	2.61	2.54	2.33
5	5	31.19	29.25	28.93	27.53	25.91	2.45	2.12	2	1.95	1.85

Fig. 3.24 (a) and Fig.3.24 (b) show the percentage of line voltage and current THD for PIDTC of the IM during no-load operation and the corresponding values are 35.1 and 3.3, respectively. The percentage of line voltage and current THDs during no-load for T1FDTC with DRC has 33.2 and 2.78 as shown in Fig. 3.25 (a) and Fig. 3.25 (b), respectively. Fig. 3.26 (a) and Fig.3.26 (b) give the percentage of line voltage and current THDs for T1FDTC with HSVM of the IM during no-load operation and the corresponding values are 31.93 and 2.58, respectively. The T2FDTC of the IM along with DRC provides the no-load line voltage and current THDs of 30.13 and 2.49 as shown in Fig. 3.27 (a) and Fig. 3.27 (b), respectively. Fig. 3.28 (a) and Fig. 3.28 (b) have the

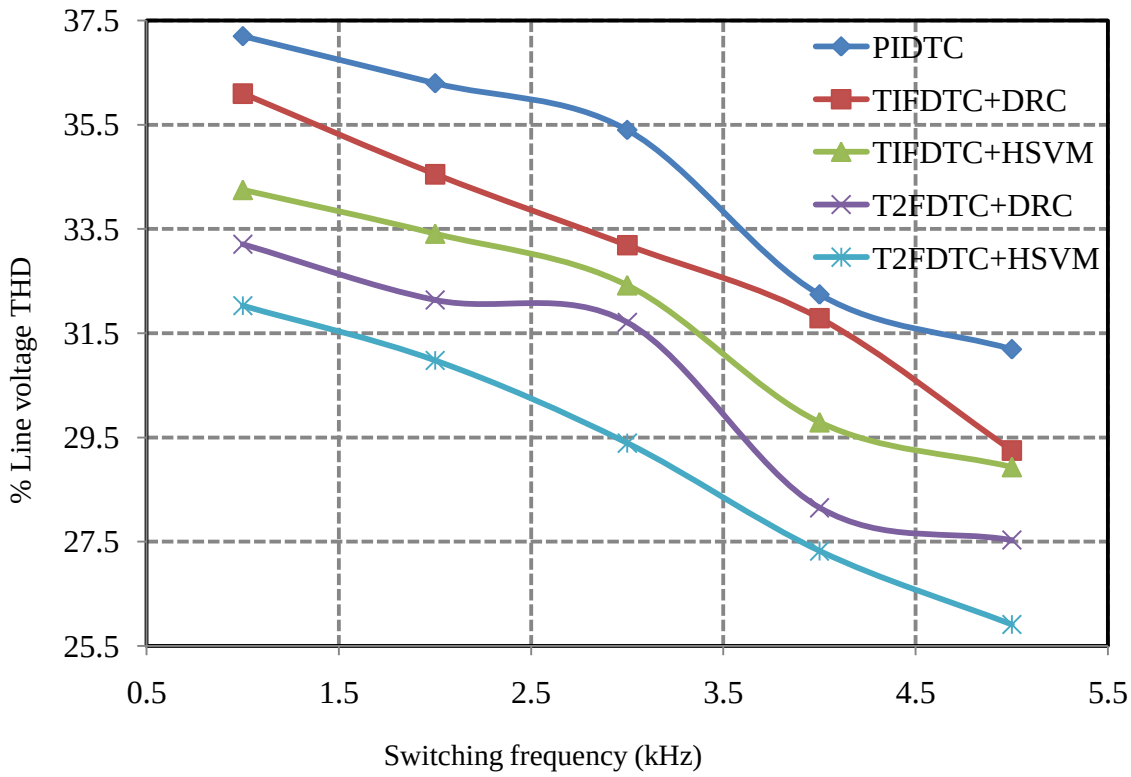
percentage of line voltage and current THDs for T2FDTC with HSVM of the IM during no-load operation and the corresponding values are 29.07 and 2.43, respectively. Therefore, it is observed from Fig. 3.24 to Fig. 3.28 that the T2FDTC with HSVM has provided less voltage and current THDs of 29.07% and 2.43% than other four control schemes control schemes (PIDTC, T1FDTC with DRC, T1FDTC with HSVM, and T2FDTC with DRC). This is due to the fact that the HSVM provided the less RMS flux ripple using T2FLC, the T2FLC effectively deals with the huge ambiguous data using the type reducer, and estimate the control variable very close to actual value.

Table 3.7: Overall efficiency of alternative techniques during simulation

% Load	V_d**(V)**	I_{inv}=I_d**(A)**	P_{inv}**(W)**	ω_m **(rad/s)**	T_e**(N-m)**	P_m**(W)**	$\%\eta = 100*(P_{inv}/P_m)$
PIDTC							
25	640	1.5	**960**	152.8	2.02	**308.656**	32.15
50	640	1.8	**1152**	152.8	3.9	**595.92**	51.72
75	640	2.55	**1632**	152.8	6.75	**1031.4**	63.19
100	640	2.8	**1792**	152.8	8.5	**1298.8**	72.47
T1FDTC with DRC							
25	640	1.5	**960**	152.8	2.09	**319.352**	33.26
50	640	1.8	**1152**	152.8	4.02	**614.256**	53.32
75	640	2.55	**1632**	152.8	6.9	**1054.32**	64.60
100	640	2.8	**1792**	152.8	8.62	**1317.14**	73.50
T2FDTC with DRC							
25	640	1.5	**960**	152.8	2.11	**322.408**	33.58
50	640	1.8	**1152**	152.8	4.15	**634.12**	55.04
75	640	2.55	**1632**	152.8	7.1	**1084.88**	66.47
100	640	2.8	**1792**	152.8	8.75	**1337**	74.60
T1FDTC with HSVM							
25	640	1.5	**960**	152.8	2.14	**326.992**	34.06
50	640	1.8	**1152**	152.8	4.2	**641.76**	55.70
75	640	2.55	**1632**	152.8	7.13	**1089.46**	66.75
100	640	2.8	**1792**	152.8	8.72	**1332.42**	74.35
T2FDTC with HSVM							
25	640	1.5	**960**	152.8	2.18	**333.104**	34.69
50	640	1.8	**1152**	152.8	4.3	**657.04**	57.03
75	640	2.55	**1632**	152.8	7.195	**1099.4**	67.36
100	640	2.8	**1792**	152.8	8.8	**1344.64**	75.03

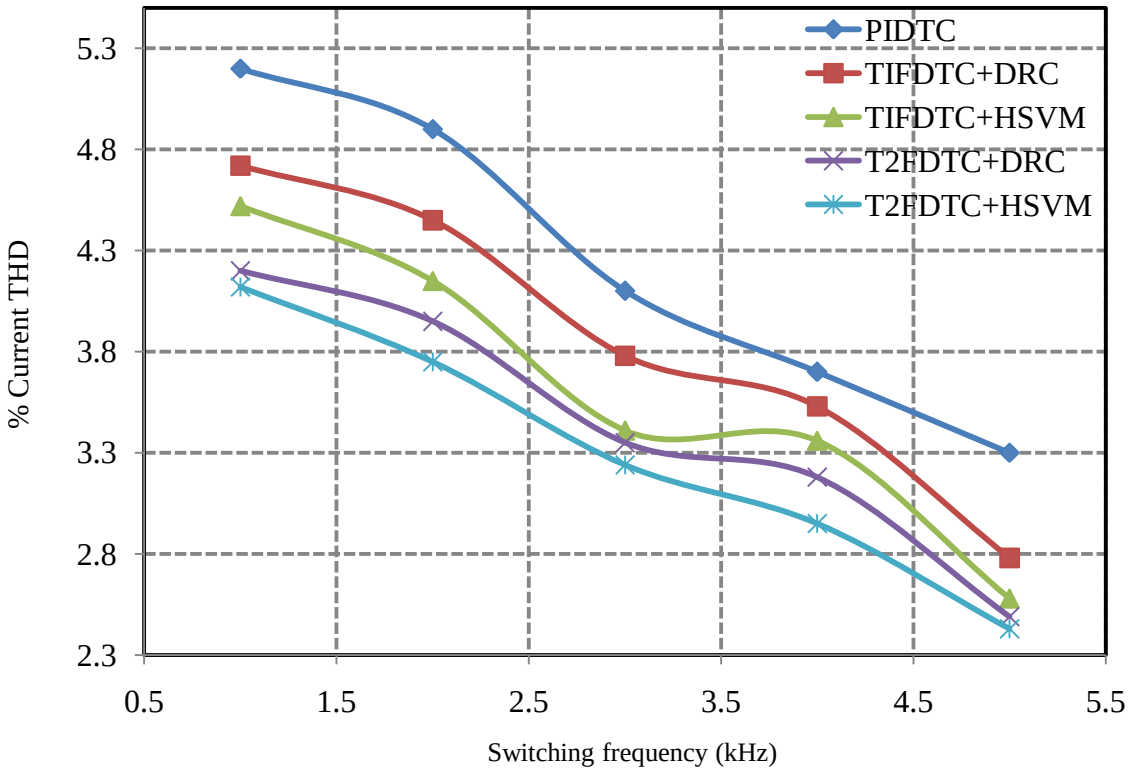


(a) No-load voltage THD vs. switching frequency

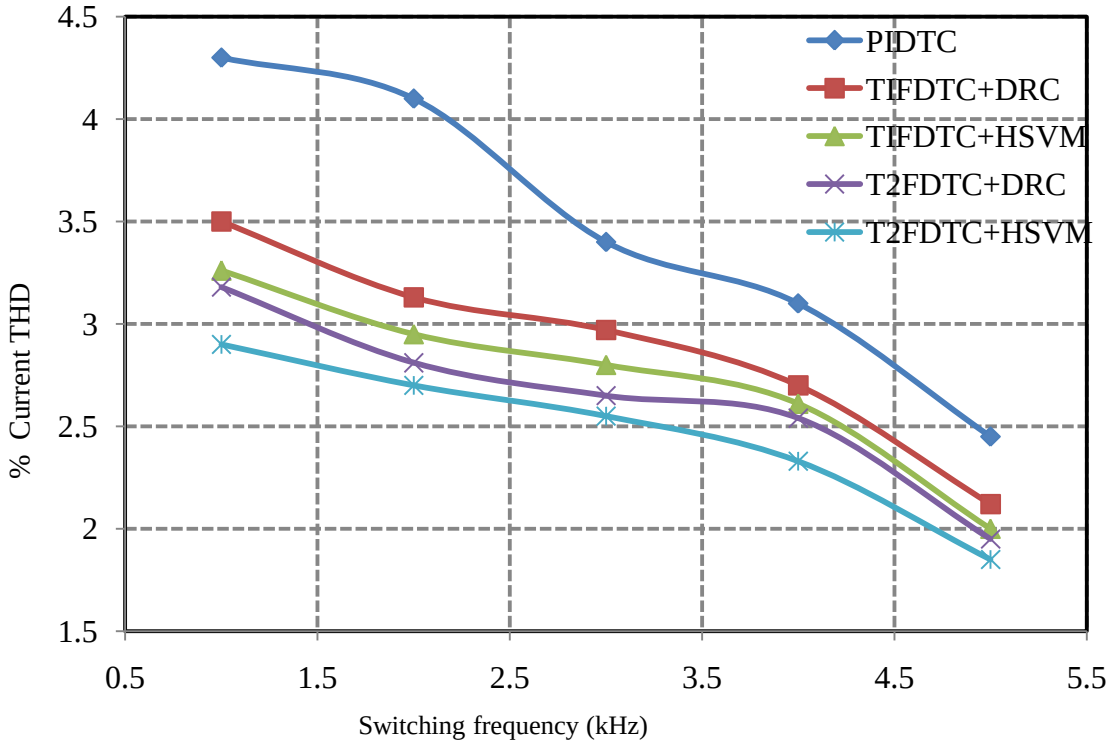


(b) Full-load voltage THD vs. switching frequency

Fig. 3.29: No-load and full-load voltage THD of the IM for different control schemes

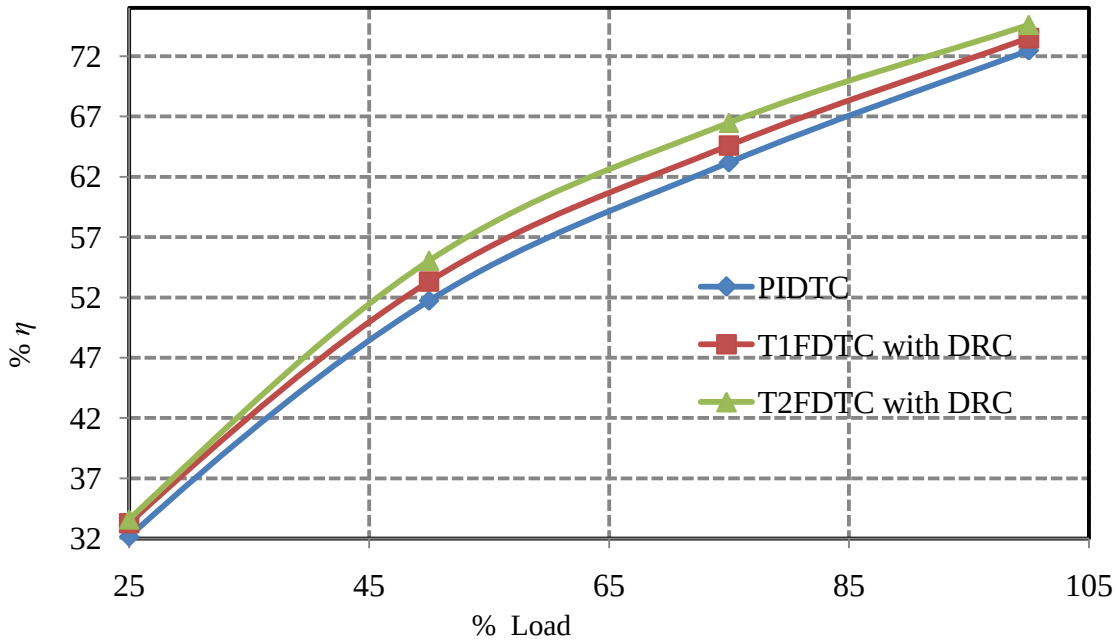


(a) No-load Current THD vs. switching frequency

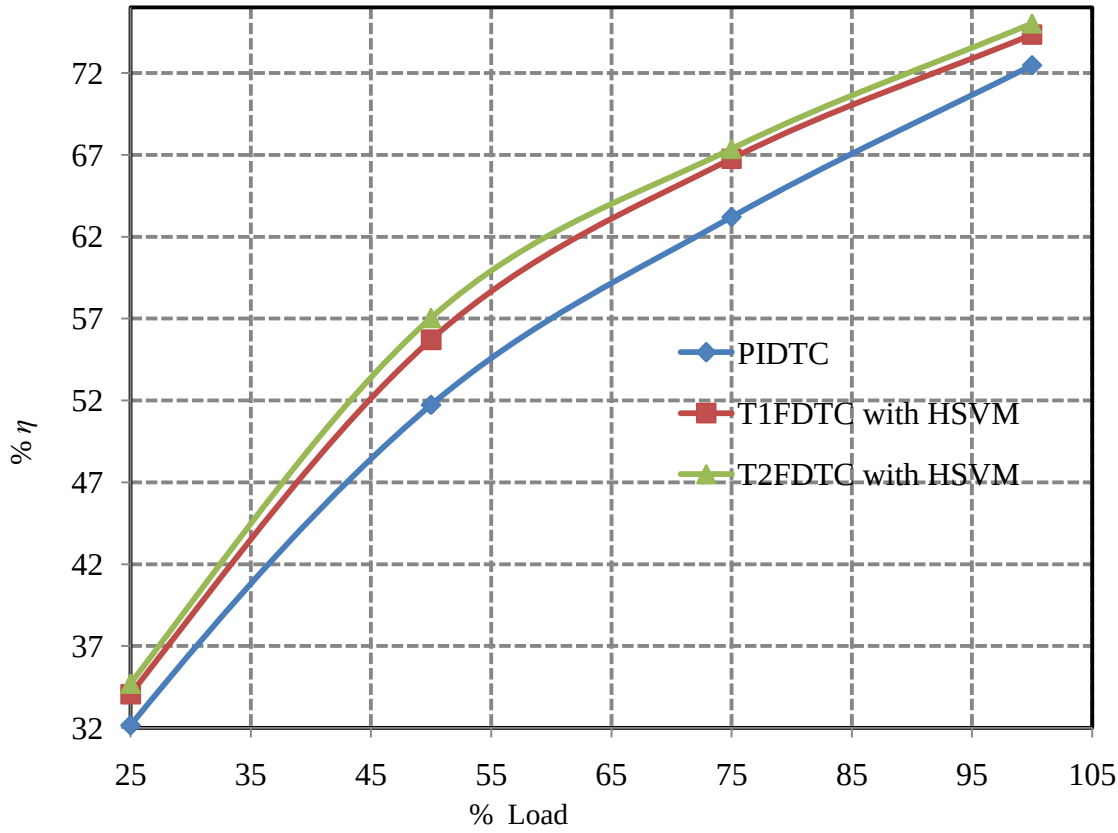


(a) full-load current THD vs. switching frequency

Fig. 3.30: No-load and full-load current THD of the IM for different control schemes



(a) PIDTC and DRC for T1FDTC and T2FDTC



(b) PIDTC, HSVM for T1FDTC and T2FDTC

Fig. 3.31: %Overall efficiency vs. load of the IM drive for different control techniques

Table 3.6 shows the simulated %THD comparison for both line voltage and current under no-load and full-load operaion by changing the switching frequency from 1kHz to

5kHz using different control schemes. Consequenty, a comparative performance is studied and plotted for the corresponding line voltage THD during the no-load and full-load as shown in Fig. 3.29 (a) and Fig. 3.29 (b), respectively. Furthermore, the percentage of current THD vs. switching frequency is plotted for both no-load and full-load operation as shown in Fig. 3.30 (a) and Fig. 3.30 (b), respectively. From Fig. 3.29 and Fig. 3.30, it is observed that the T2FDTC with HSVM provided less voltage and current THD value than PIDTC, T1FDTC with DRC, T1FDTC with HSVM, and T2FDTC with DRC. Morover, the efficiency also calculated under different loading condition with fixed switching frequency of 5kHz as given in Table 3.7. A graph is plotted between percentage of the efficiency and percentage of the load for PIDTC, T1FDTC with DRC and T2FDTC with DRC as shown in Fig. 3.31(a). Here, T2FDTC with DRC of the IM has more efficiency than T1FDTC with DRC and PIDTC. The reason is that the T2FDTC with DRC provides less harmonics/ripples of voltage, current, and torque which implies the losses should be less and hence the efficiency of the IM drive significantly improved as compared to T1FDTC with DRC and PIDTC. Fig. 3.31 (b) shows the percentage of the efficiency and percentage of the load for PIDTC, T1FDTC with HSVM and T2FDTC with HSVM in which the T2FDTC with HSVM provides the higher efficiency at each and every instant of the load as compared to other two control schemes (PDTC and T1FDTC with HSVM). It is concluded that the T2FDTC with HSVM provides the improved efficiency at all loading conditions as compared to the other four control schemes (PIDTC, T1FDTC with DRC, T1FDTC with HSVM, and T2FDTC with DRC). In addition, the percentage of full load efficiency of the IM using T2FDTC with HSVM is 75.03, which is the highest value among the four control schemes as mentioned above.

The comparative performance, such as starting, step change in speed, speed reversal, operation during the load, voltage and current THDs, flux and torque distortion, change in the speed during the load and efficiency at full load of the IM drive with the above control schemes are mentioned in Table 3.10 in detail. Where, Ψ_{NLdst}, T_{NLdist}, Nc_{DL}, $\%V_{NLTHD}$, $\%I_{NLTHD}$, $\%V_{FLTHD}$, $\%I_{FLTHD}$, $\%\eta_{FL}$, t_{st},t_{scs},t_{srf}, t_{srb}, and t_{DL}, are the no-load torque distortion (N-m), change in speed during the load (rpm), percentage of no-load voltage THD, percentage of no-load current THD, percentage of full-load voltage THD, percentage of full-load current THD, percentage of full-load efficiency, settling time (s) during starting, settling time (s) during step change in speed, settling time (s) during the speed reversal, and settling time (s) during the load, respectively.

3.7.2 Experimental Results

The above control schemes as mentioned in the simulation results are also experimentally implemented for the same rating of induction machine by using DSPACE-1104 control. Fig. 3.3 shows the schematic diagram for the IM drive using PIDTC, T1PFDTC with DRC, T1FDTC with HSVM, T2FDTC with DRC, and T2FDTC with HSVM. The experimental performance of the IM drive for the above mentioned control schemes is also implemented in real time and validated under similar operating conditions as used in the simulation results. The PIDTC of IM drive is also verified with the experimental setup using a DSPACE DS1104 controller. The operated switching frequency of the inverter and the sampling time (40μs), DC-link voltage, and parameters of the induction machine in real time applications remain same as the simulation with a dead band of 10μs for complementary switching devices and they are available in Appendix A1. At starting, the reference speed 500 rpm is initiated and controlling signals are generated through a DSPACE kit and set a required DC-voltage (640V) to the inverter by adjusting three-phase auto-transformer as shown in Fig. 3.32(a) in which the initial torque and flux are low values due to low supply voltage provided by the inverter and later picks up their values with supply voltage. Consequently, the IM picks of the speed and settled to 500rpm at 1.02s and the torque and current also settled at the same time. However, the flux is also maintained constant after reaching a required speed of the IM. Fig. 3.32 (b) shows the step change in speed from 500rpm to 1450rpm at 0.25s then the IM develops a torque of 18N-m with large amplitude of the current (4.6A) to get required speed (1450rpm). Therefore, the IM settled to 1450rpm at 1.19s with less torque and current. Fig. 3.32(c) shows the IM drive performance when the speed reversal (+1450rpm to -1450rpm) is initiated at 0.25s. Consequently, the IM develops the high negative electromagnetic torque of 18N-m with large current amplitudes of 4.6A to reach required speed-1450rpm. The IM speed is going to decrease until the zero speed is reached and it picks up in the reverse direction. Also observed that the current direction gets reversed when the speed crossed to zero and both (currents and torque) are settled at 2.28s with less current and torque. The speed reversal (-1450rpm to +1450rpm) is applied again to the IM drive at 0.25s, the corresponding waveforms look like a mirror image to the previous case. In addition, the IM is settled within 2.28s, which remains the same as in case of the speed reversal.

The load of 4N-m is applied and removed at 0.2s and 0.7s, the IM is decelerated and accelerated to 1440rpm and 1460rpm, respectively as shown in Fig. 3.32(e). However, the IM is settled to 1450rpm at 0.4s and 0.9s during decelerating and accelerating modes of operation, respectively. Therefore, the IM settled within 0.22s during both decelerating and accelerating modes of operation. Fig. 3.32(f) shows the IM performance for PIDTC in which a step changes in the load from 4N-m to 8N-m and 8N-m to 4N-m at 0.2s and 0.7s, respectively. The IM draws a large amplitude of the current (3.2A) and torque (8N-m) to get the required speed (1450rpm). Moreover, the settling time and drop in speed of the IM are 0.22s and 10rpm during decelerating and accelerating modes of the operation that remains the same as discussed above in Fig. 3.32(e).

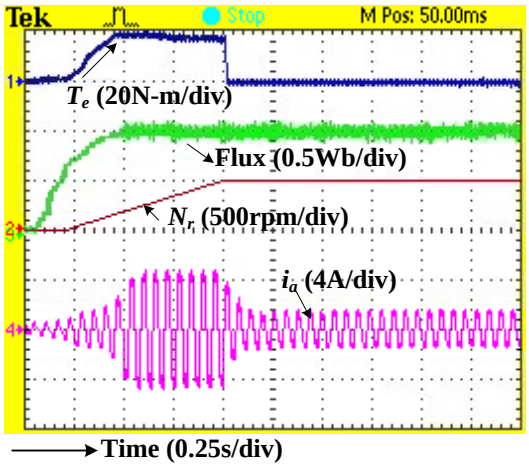
Similarly, the experimental performance of the IM drive is also checked under the same operating modes using T1FDTC with DRC. Fig. 3.33(a) shows the starting performance of the IM in which the large torque and current are developed as similar to PIDTC of IM and it is settled to 500rpm at 0.95s. Therefore, the settling time of the IM drive using T1FDTC with DRC is faster by 0.07s as compared to PIDTC. Fig. 3.33(b) shows a step change in the speed from 500rpm to 1450rpm at 0.25s for T1FDTC with DRC. Thus, the IM develops a high torque with large current to get required speed of 1450rpm and is settled to 1450rpm at 1.15s whereas in T1FDTC is settled at 1.19s as shown in Fig. 3.32(b). Hence, the settling time of IM for T1FDTC with DRC is faster by 0.04s than PIDTC. The speed reversal (from 1450rpm to -1450rpm) is initiated at 0.25s as shown in Fig. 3.33(c). The T1FDTC with DRC of IM is settled to -1450rpm at 2.125s because of high negative torque and current, whereas in PIDTC of IM was settled at 2.28s as shown in Fig. 3.32(c). The settling time during the speed reversal is faster approximately by 0.155s using T1FDTC with DRC than PIDTC. For a second time, the speed reversal (-1450rpm to +1450rpm) is initiated at 0.25s then the steady state of the IM is achieved by 2.15s as shown in Fig. 3.33(d) in which the settling time is almost same as the previous case. Fig. 3.33(e) shows a step change in the load (load perturbation) from 0N-m to 4N-m and 4N-m to 0N-m at 0.2s and 0.7s, respectively while running the IM at 1450rpm. The IM decelerates and accelerates to 1445rpm and 1455rpm settled to 1450rpm at 0.32s and 0.92s, respectively. Therefore, the fast dynamic performance of the IM using T1FDTC with DRC is obtained approximately by 0.08s at load perturbation than PIDTC. The no-load flux and torque distortions T1FDTC with DRC are ±0.095Wb and ±0.92N-m, whereas in PIDTC has ±0.123Wb and ±1.2N-m as shown in Fig. 3.32(e). Hence, the flux and torque distortions for T1FDTC with DRC improved by 22.7% and

28.12% than PIDTC. In addition, the change in speed during the load perturbation for T1FDTC with DRC of IM is 5rpm only, which is less than the PIDTC of IM drive. Fig. 3.33(f) shows the IM performance for T1FDTC with DRC in which a step change in the load from 4N-m to 8N-m and 8N-m to 4N-m at 0.2s and 0.7s, respectively. The settling time and the change in speed of the IM are 0.12s and 5rpm during decelerating and accelerating modes of operation, which remains the same as discussed above in Fig. 3.33(e).

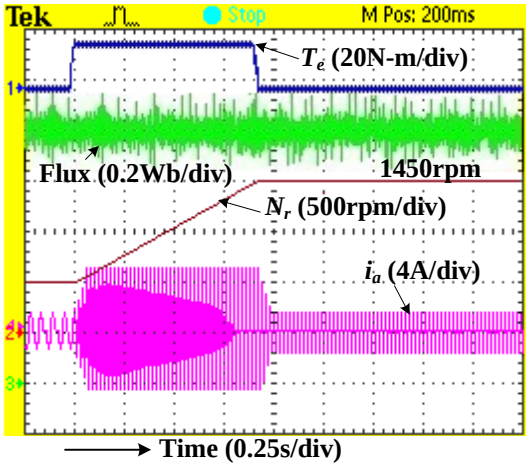
The experimental performance of the IM drive is also verified under the same operating conditions using T1FDTC with HSVM. Fig. 3.34(a) provides the starting performance of the IM in which the large torque and current are developed as similar to PIDTC of IM and consequently settled to 500rpm at 0.95s. Therefore, the IM drive using T1FDTC with HSVM is settled faster by 0.07s than PIDTC. Fig. 3.34(b) shows a step change in the speed from 500rpm to 1450rpm at 0.25s for T1FDTC with HSVM. Consequently, the IM develops a high torque with large current for getting the required speed of 1450rpm and is settled to 1450rpm at 1.149s, whereas in PIDTC was settled at 1.17s as shown in Fig. 3.32(b). The faster settling time of the IM for T1FDTC with HSVM is obtained by 0.41s than PIDTC. The speed reversal (from 1450rpm to -1450rpm) is commenced at 0.25s as shown in Fig. 3.34(c). The IM is inhabited to -1450rpm at 2.125s whereas in PIDTC is settled at 2.25s. The settling time is faster approximately by 0.125s during the speed reversal using T1FDTC with HSVM than PIDTC. Moreover, the speed reversal (-1450rpm to +1450rpm) is initiated again at 0.25s then the steady state of the IM is achieved by 2.125s as shown in Fig. 3.34(d) in which the settling time is almost same as that of the previous case. Fig. 3.34(e) provides a step change in the load (load perturbation) from 0N-m to 4N-m and 4N-m to 0N-m at 0.2s and 0.7s, respectively after settling the IM to 1450rpm. The IM speed reduces and increases to 1445rpm and 1455rpm and settled to 1450rpm at 0.32s and 0.82s, respectively. Therefore, the fast dynamic performance of the IM is obtained approximately by 0.08s during the load perturbation using T1FDTC with HSVM than PIDTC. In addition, the flux and torque distortion at no load are obtained as ±0.075Wb and ±0.84N-m, respectively. The percentage of improved the torque and flux distortions using T1FDTC with HSVM are 39% and 34.3% over PIDTC. Also, the change in speed for T1FDTC with HSVM of IM is 5rpm only that is very less as compared to PIDTC. Fig. 3.34(f) shows the IM performance for T1FDTC with HSVM in which a step change in the load from 4N-m to 8N-m and 8N-m to 4N-m at 0.2s and 0.7s, respectively. The total settling time and the

change in speed of the IM are 0.07s and 4rpm during decelerating and accelerating modes of operation, which remains the same as discussed above in Fig. 3.34(e).

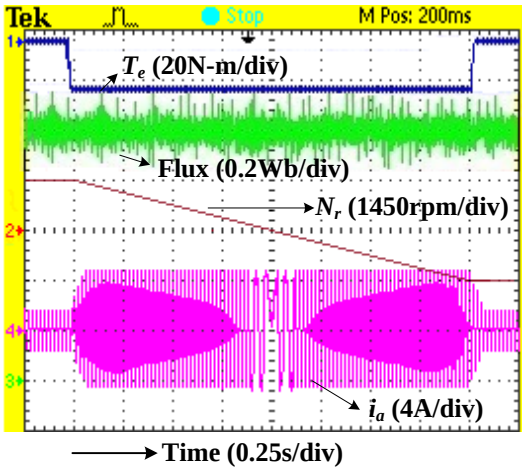
The experimental performance of the IM drive is also verified under the same operating conditions for T2FDTC with DRC. Fig. 3.35(a) consists of the starting performance of the IM in which the IM is settled to 500rpm at 0.875s. Therefore, the IM drive using T2FDTC with DRC is settled faster by 0.145s than PIDTC. Fig. 3.35(b) shows a step change in the speed from 500rpm to 1450rpm at 0.25s for T2FDTC with DRC. Consequently, the IM is settled to 1450rpm at 1.075s, whereas in PIDTC was settled at 1.19s as shown in Fig. 3.32(b). The faster settling time of the IM for T2FDTC with DRC is obtained by 0.115s than PIDTC. The speed reversal (from 1450rpm to -1450rpm) is commenced at 0.25s as shown in Fig. 3.35(c). The IM is inhabited to -1450rpm at 2s, whereas in PIDTC of IM is settled to -1450rpm at 2.28s. The settling time is faster approximately by 0.28s during the speed reversal using T2FDTC with DRC than PIDTC. Moreover, the speed reversal (-1450rpm to +1450rpm) is initiated again at 0.25s then the steady state of the IM is achieved by 2s as shown in Fig. 3.35(d) in which the settling time is same as discussed in the previous case. Fig. 3.35(e) provides a step change in the load (load perturbation) from 0N-m to 4N-m and 4N-m to 0N-m at 0.2s and 0.7s, respectively after settling the IM to 1450rpm. The IM speed reduces and increases to 1447rpm and 1453rpm and settled to 1450rpm at 0.26s and 0.76s, respectively. Therefore, the fast dynamic performance of the IM is obtained approximately by 0.14s during the load perturbation using T2FDTC with DRC than PIDTC. In addition, the flux and torque distortion for T2FDTC with DRC of IM at no load are ±0.06 and ±0.75. Thus, the improvement of flux and torque distortion than PIDTC is 52.3% and 41.46%, respectively. Moreover, the fluctuation in speed of the IM during the load perturbation is 3rpm that is very smaller than PIDTC. Fig. 3.35(f) shows the IM performance for T2FDTC with DRC in which a step change in the load from 4N-m to 8N-m and 8N-m to 4N-m at 0.2s and 0.7s, respectively. The total settling time and the change in speed of the IM are 0.08s and 3rpm during decelerating and accelerating modes of operation, which remains the same as discussed above in Fig. 3.35(e).



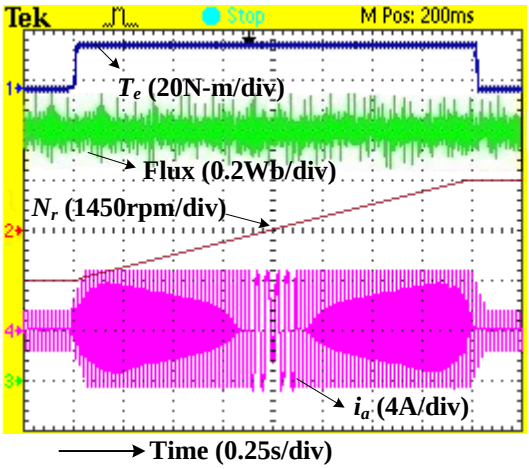
(a) Starting when applied a reference speed of 500rpm



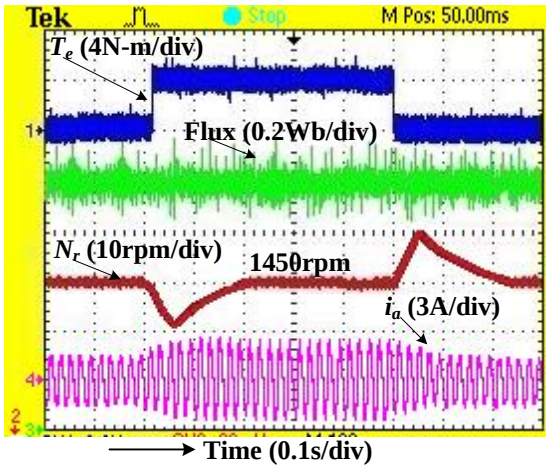
(b) Step change in speed at 0.25s



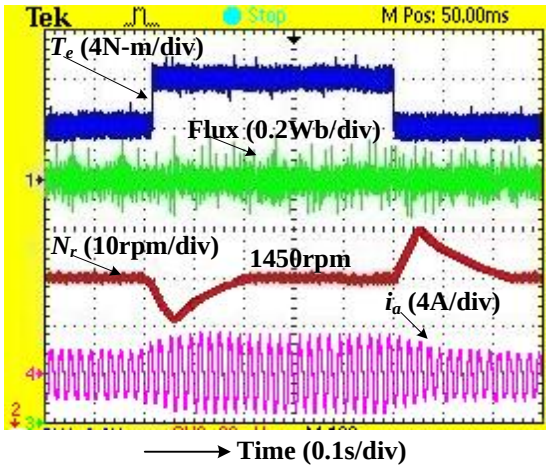
(c) Application speed reversal at 0.25s



(d) Application of speed reversal at 0.25s

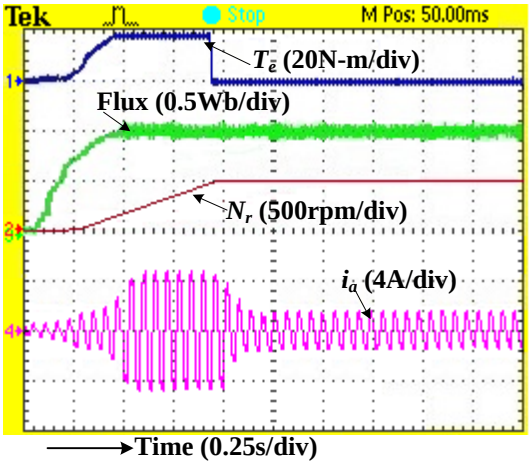


(e) During the load of 4N-m at 0.2s

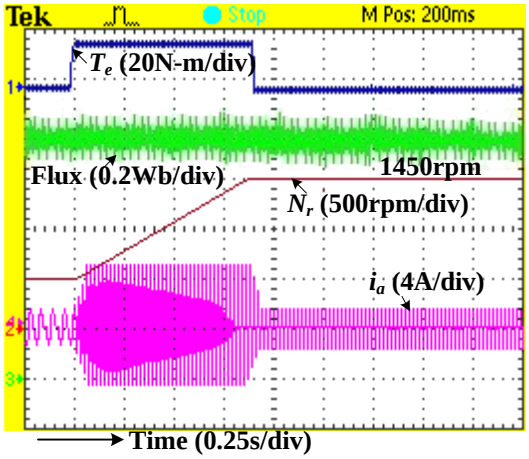


(f) During the load of 8N-m at 0.2s

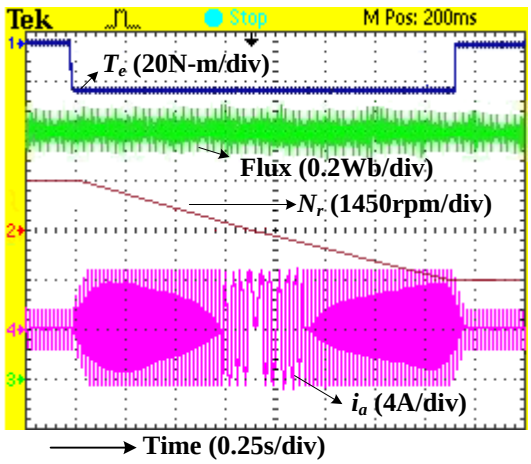
Fig. 3.32: Performance of the IM under different modes of operation using PIDTC



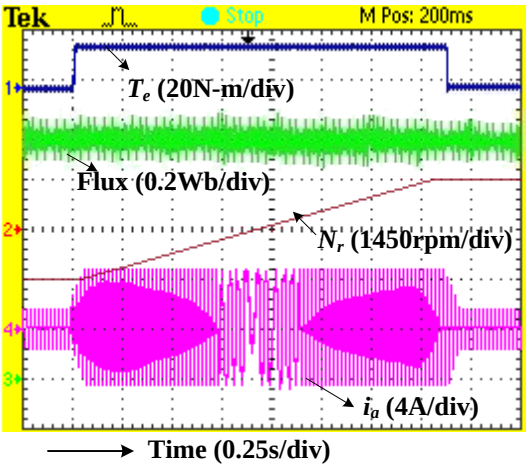
(a) Starting when applied a reference speed of 500rpm



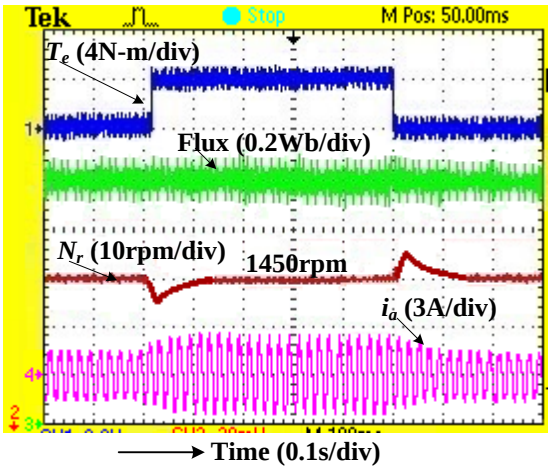
(b) Step change in speed at 0.25s



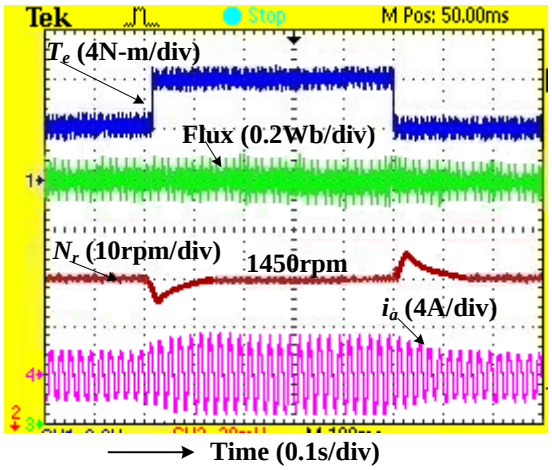
(c) Application of speed reversal at 0.25s



(d) Application of speed reversal at 0.25s

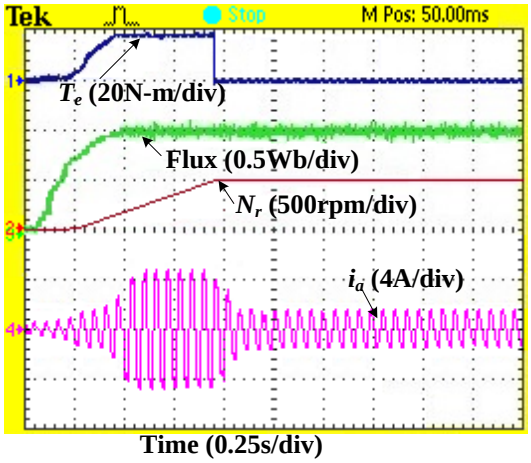


(e) During the load of 4N-m at 0.2s

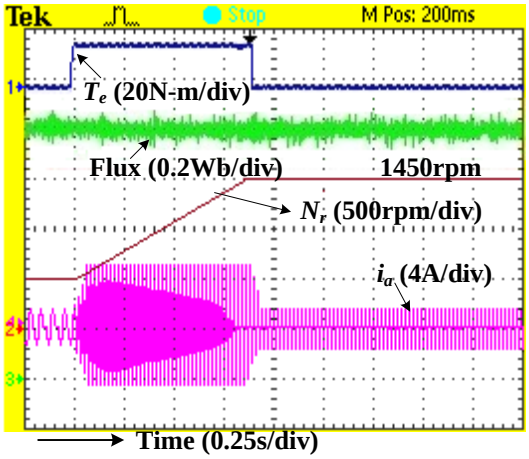


(f) During the load of 8N-m at 0.2s

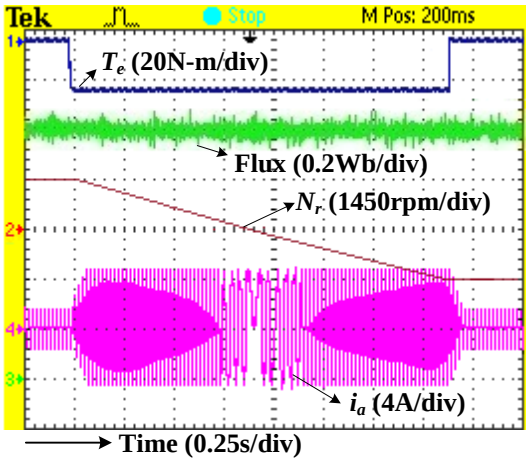
Fig. 3.33: Performance of the IM under different modes of operation using T1FDTC with DRC



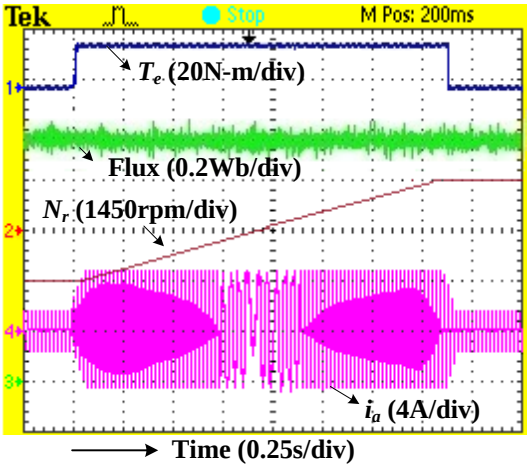
(a) Starting when applied a reference speed of 500rpm



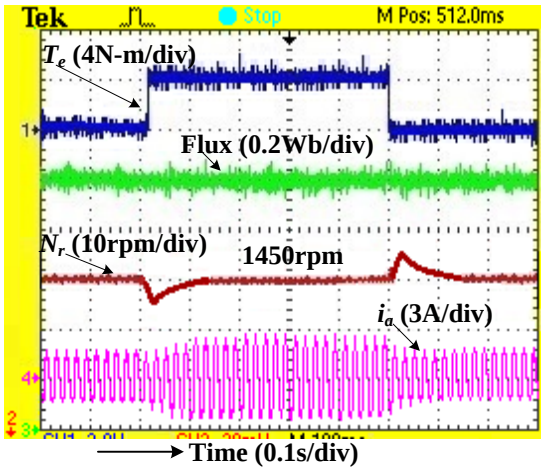
(b) Step change in speed at 0.25s



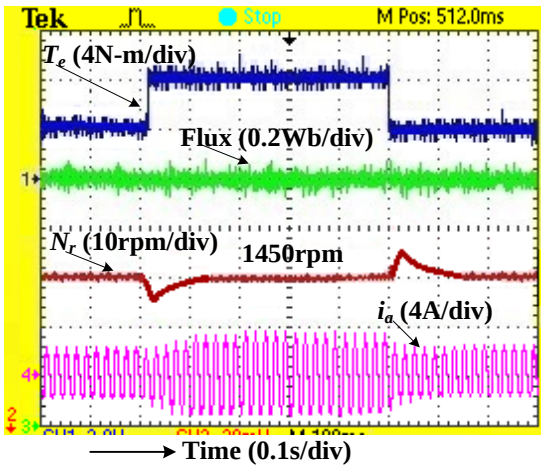
(c) Application of speed reversal at 0.25s



(d) Application of speed reversal at 0.25s

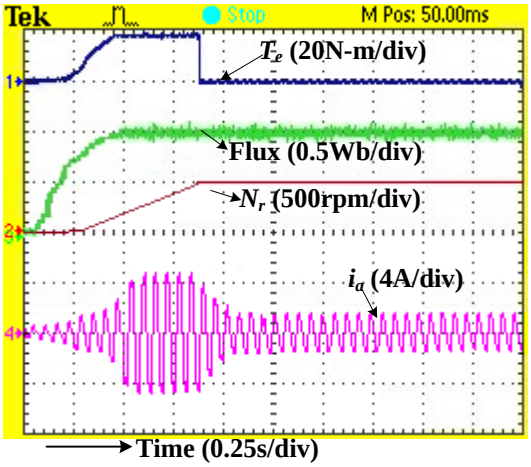


(e) During the load of 4N-m at 0.2s

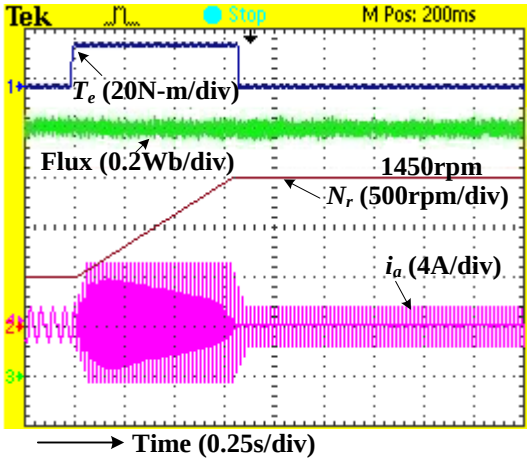


(f) During the load of 8N-m at 0.2s

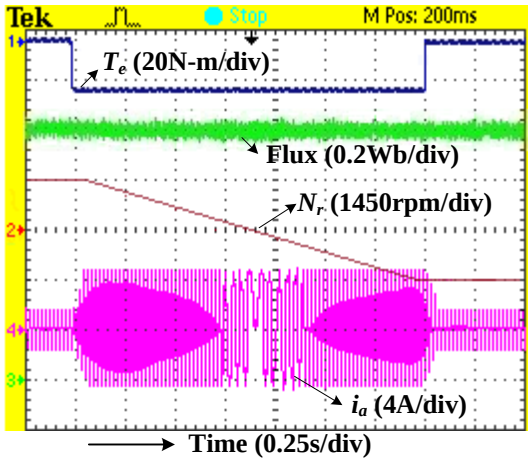
Fig. 3.34: Performance of the IM under different modes of operation using T1FDTC with HSVM



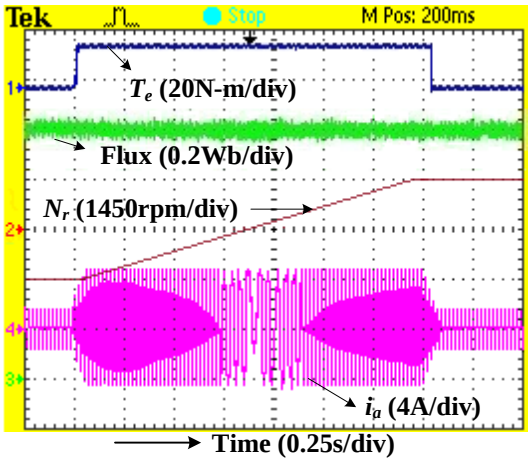
(a) Starting when applied a reference speed of 500rpm



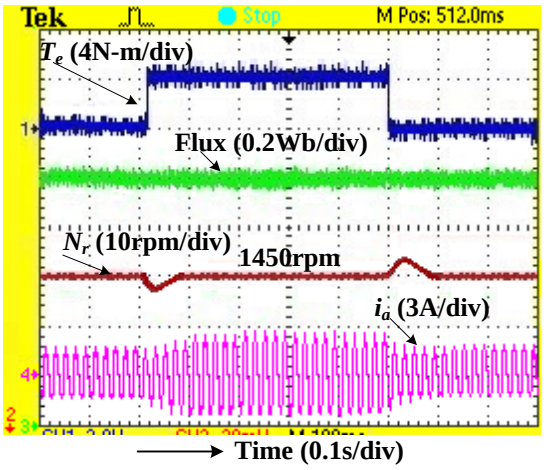
(b) Step change in speed at 0.25s



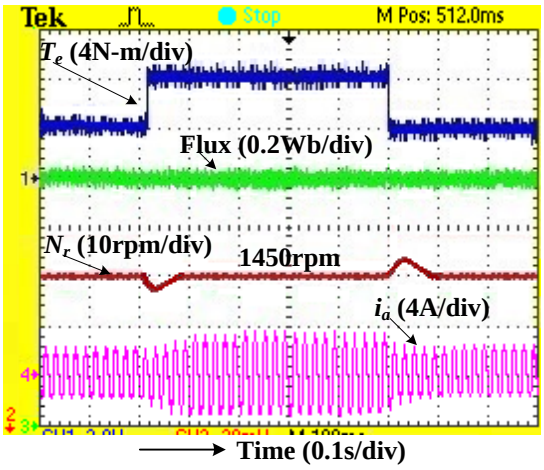
(c) Application of speed reversal at 0.25s



(d) Application of speed reversal at 0.25s

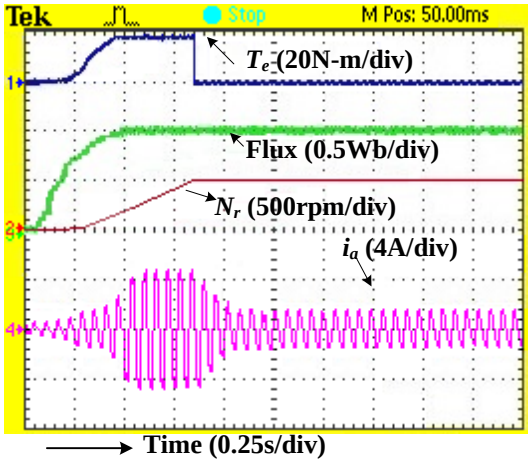


(e) During the load of 4N-m at 0.2s

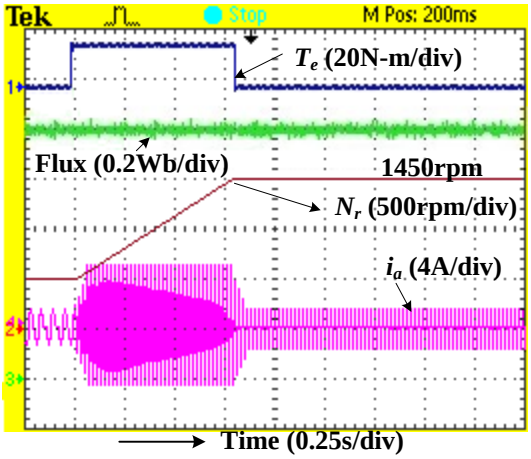


(f) During the load of 8N-m at 0.2s

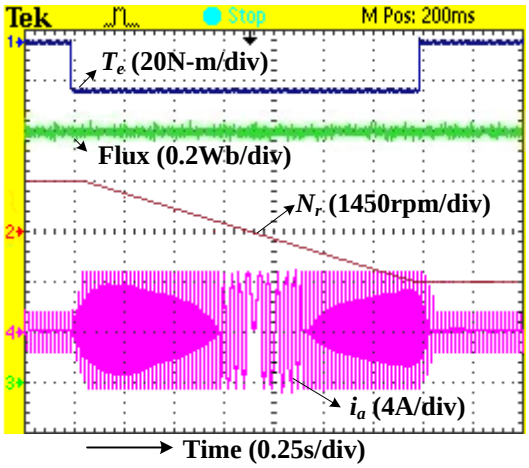
Fig. 3.35: Performance of the IM under different modes of operation using T2FDTC with DRC



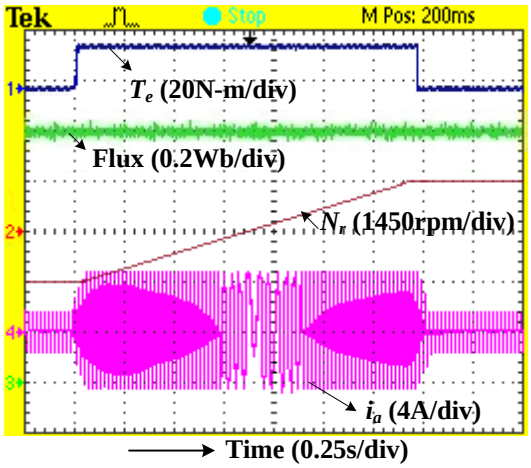
(a) Starting when applied a reference speed of 500rpm



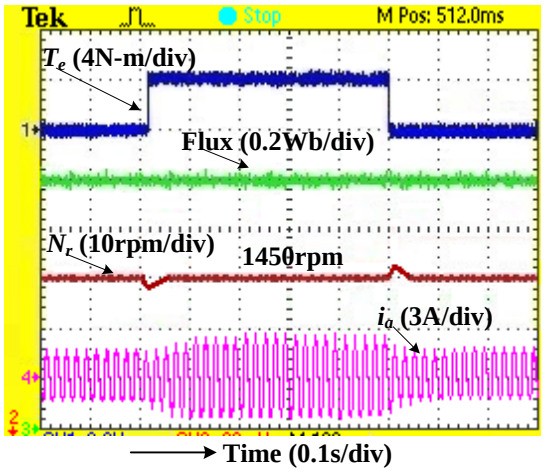
(b) Step change in speed at 0.25s



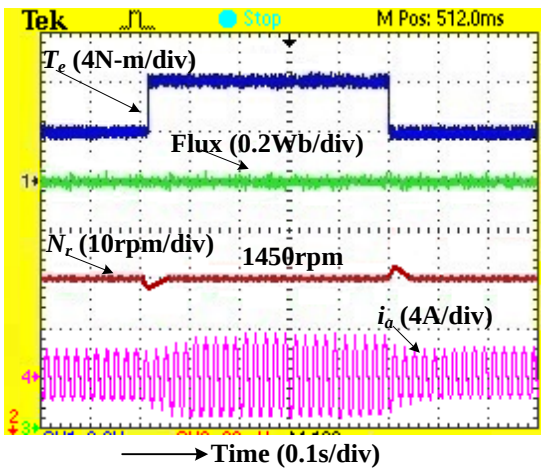
(c) Application of speed reversal at 0.25s



(d) Application of speed reversal at 0.25s

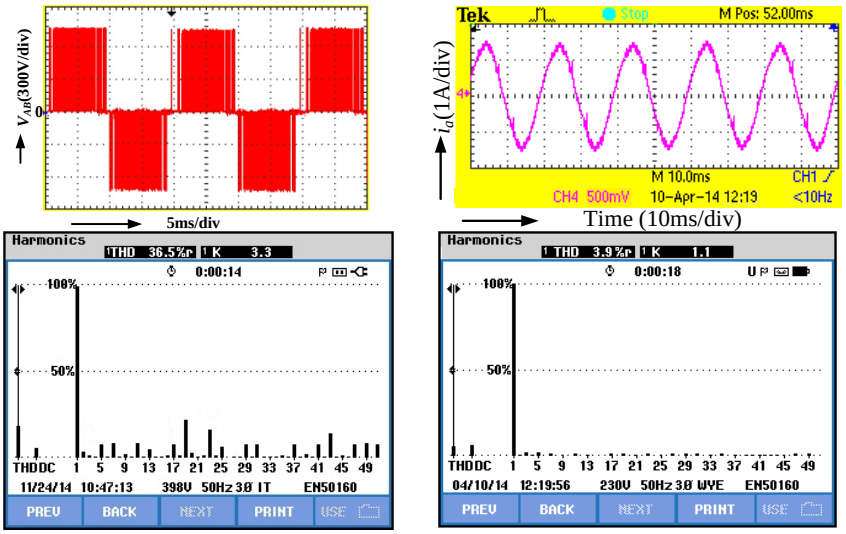


(e) During the load of 4N-m at 0.2s



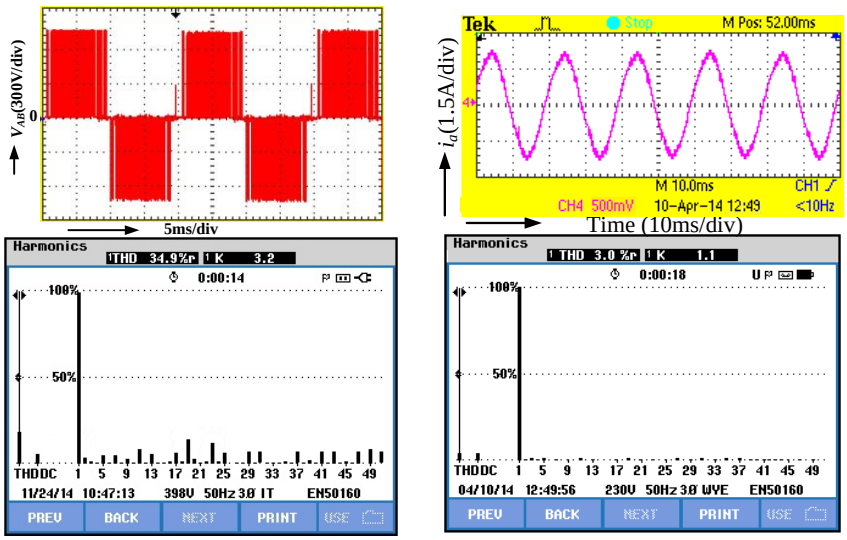
(f) During the load of 8N-m at 0.2s

Fig. 3.36: Performance of the IM under different modes of operation using T2FDTC with HSVM



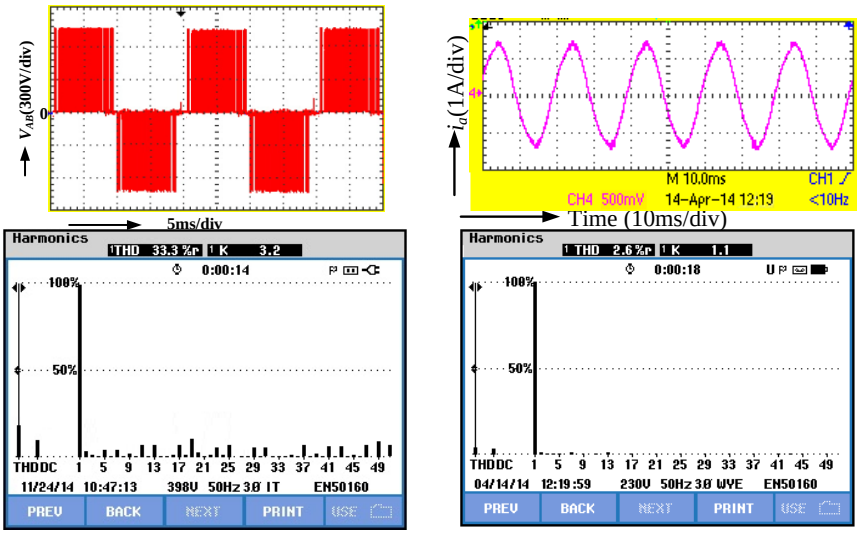
(a) Voltage THD (b) Current THD

Fig. 3.37: THD performance for the PIDTC of IM during no-load



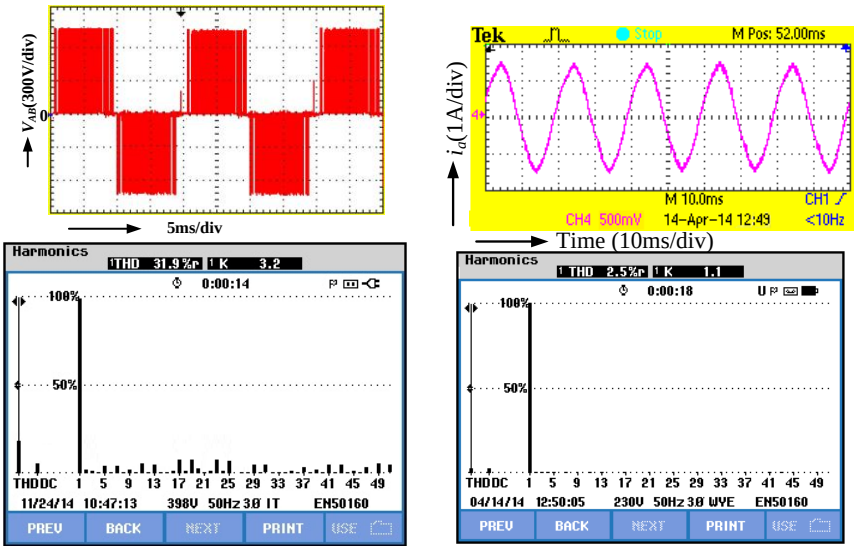
(a) Voltage THD (b) Current THD

Fig. 3.38: THD performance for the T1FDTC with DRC of IM during no-load



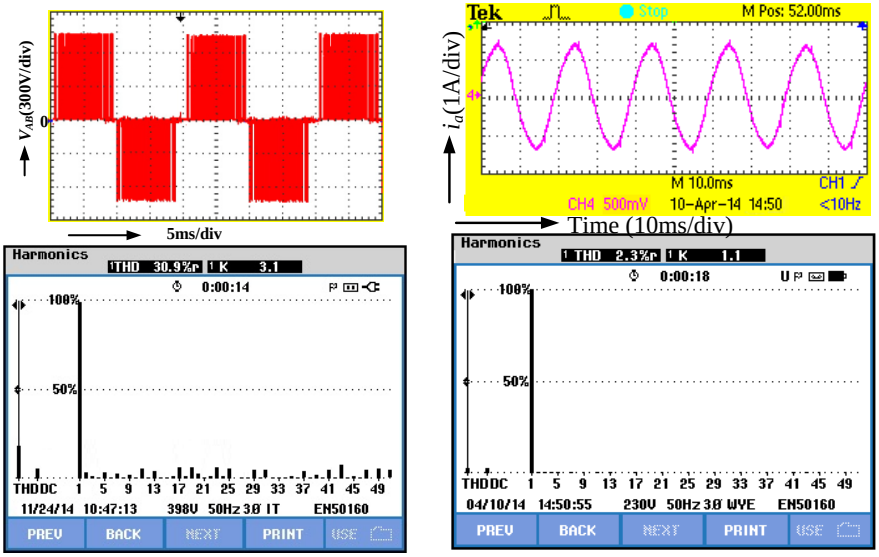
(a) Voltage THD (b) Current THD

Fig. 3.39: THD performance for the T1FDTC with HSVM of IM during no-load



(a) Voltage THD (b) Current THD

Fig. 3.40: THD performance for the T2FDTC with DRC of IM during no-load



(a) Voltage THD (b) Current THD

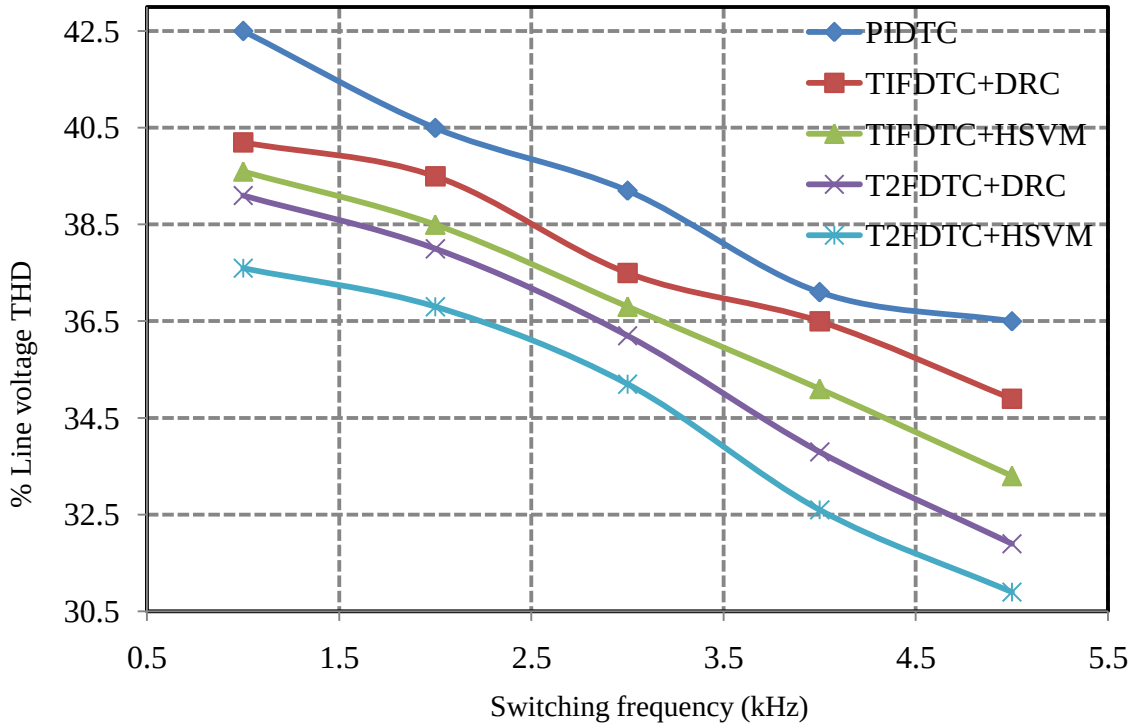
Fig. 3.41: THD performance for the T2FDTC with HSVM of IM during no-load

The simulated performance of the IM drive for T2FDTC with HSVM is also verified with the experimental setup as used under the similar operating conditions. Fig. 3.36(a) has the starting performance of the IM in which the IM is settled to 500rpm at 0.85s. Therefore, the IM drive using T2FDTC with HSVM is settled faster by 0.17s than PIDTC. Fig. 3.36(b) provides a step change in the speed from 500rpm to 1450rpm at 0.25s for T2FDTC with HSVM. As a result, the IM is settled to 1450rpm at 1.05s, whereas in PIDTC is settled at 1.19s as shown in Fig. 3.32(b). The faster settling time of the IM for T2FDTC with HSVM is obtained by 0.14s than PIDTC. The speed reversal (from 1450rpm to -1450rpm) is initiated at 0.25s as shown in Fig. 3.36(c). The IM is

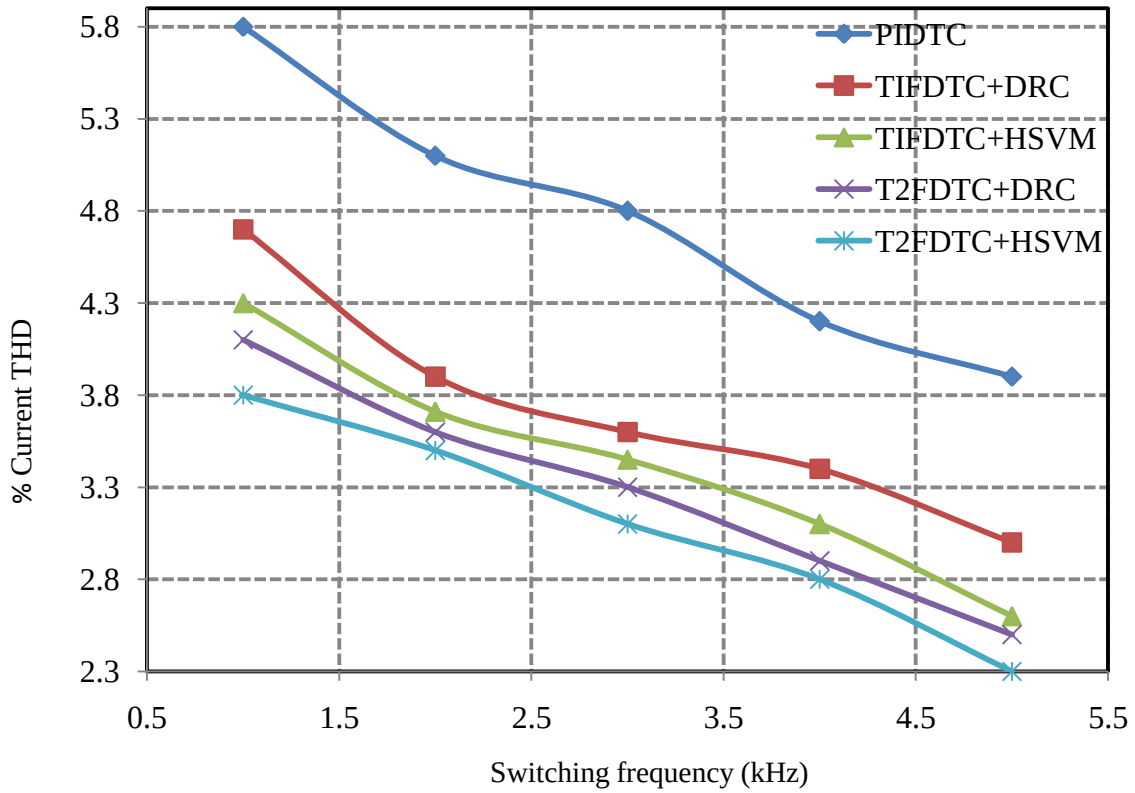
inhabited to -1450rpm at 1.97s, whereas in PIDTC of IM is settled to -1450rpm at 2.28s. The settling time is faster approximately by 0.28s during the speed reversal using T2FDTC with HSVM than PIDTC. Again, the speed reversal (-1450rpm to +1450rpm) is initiated at 0.25s then the IM is stable at 1.97s as shown in Fig. 3.36(d). However, the settling time remains the same as discussed in the previous case. Fig. 3.36(e) provides a step change in the load (load perturbation) from 0N-m to 4N-m and 4N-m to 0N-m at 0.2s and 0.7s, respectively while running a speed of 1450rpm. The IM speed reduces and increases to 1447rpm and 1453rpm and settled to 1450rpm at 0.245s and 0.745s, respectively. Therefore, the fast dynamic performance of the IM for T2FDTC with HSVM during the load perturbation is obtained approximately by 0.155s than PIDTC. In addition, the flux and torque distortion for T2FDTC with HSVM of IM at no load are ±0.045 and ±0.64. Consequently, the improvement in flux and torque distortion for T2FDTC with HSVM than PIDTC is 63.4% and 50%, respectively. Moreover, the fluctuation in speed of the IM during the load perturbation is 3rpm that is very smaller than PIDTC. Fig. 3.36(f) shows the IM performance for T2FDTC with HSVM in which a step change in the load from 4N-m to 8N-m and 8N-m to 4N-m at 0.2s and 0.7s, respectively. The total settling time and the change in speed of the IM are 0.155s and 3rpm during decelerating and accelerating modes of operation, which also remains the same as discussed above in Fig. 3.36(e).

Table 3.8: Exprimental THD comparison for different control schemes

S.No.	f_{sw} (kHz)	$\%V_{THD}$					$\%i_{THD}$				
		PIDTC	TIFDTC		T2FDTC		PIDTC	TIFDTC		T2FDTC	
			DRC	HSVM	DRC	HSVM		DRC	HSVM	DRC	HSVM
No-Load											
1	1	42.5	40.2	39.6	39.1	37.6	5.8	4.7	4.3	4.1	3.8
2	2	40.5	39.5	38.5	38	36.8	5.1	3.9	3.71	3.6	3.5
3	3	39.2	37.5	36.8	36.2	35.2	4.8	3.6	3.45	3.3	3.1
4	4	37.1	36.5	35.1	33.8	32.6	4.2	3.4	3.1	2.9	2.8
5	5	36.5	34.9	33.3	31.9	30.9	3.9	3.0	2.6	2.5	2.3
Full-Load											
1	1	38.5	35.8	34.8	34	33.6	4.9	3.9	3.7	3.5	3.2
2	2	36.2	35.4	34.7	34.4	32.3	4.5	3.2	3.1	2.9	2.7
3	3	34.4	33.2	33.1	32.1	31.2	3.9	3	2.9	2.7	2.5
4	4	33.3	32.3	31.4	30	29.5	3.5	2.9	2.7	2.6	2.3
5	5	31.5	30.2	29.6	28.5	27.8	3.1	2.1	2	1.9	1.8

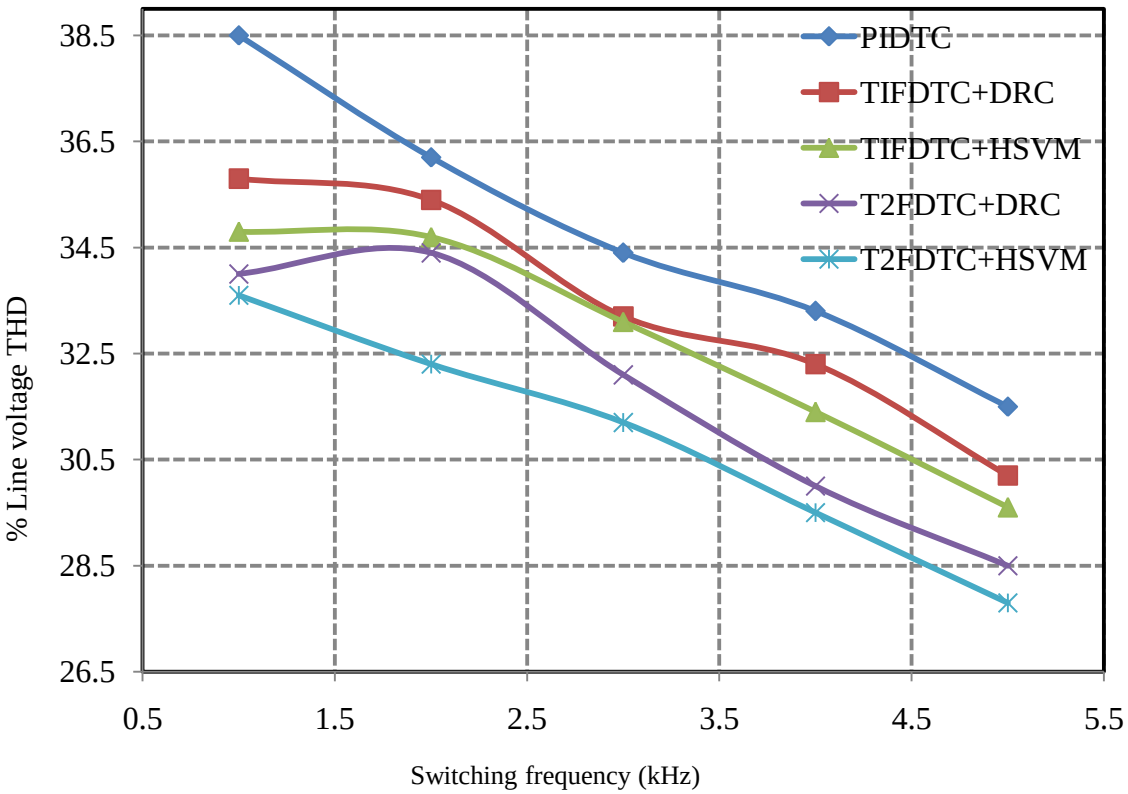


(a) Voltage THD vs. Switching frequency

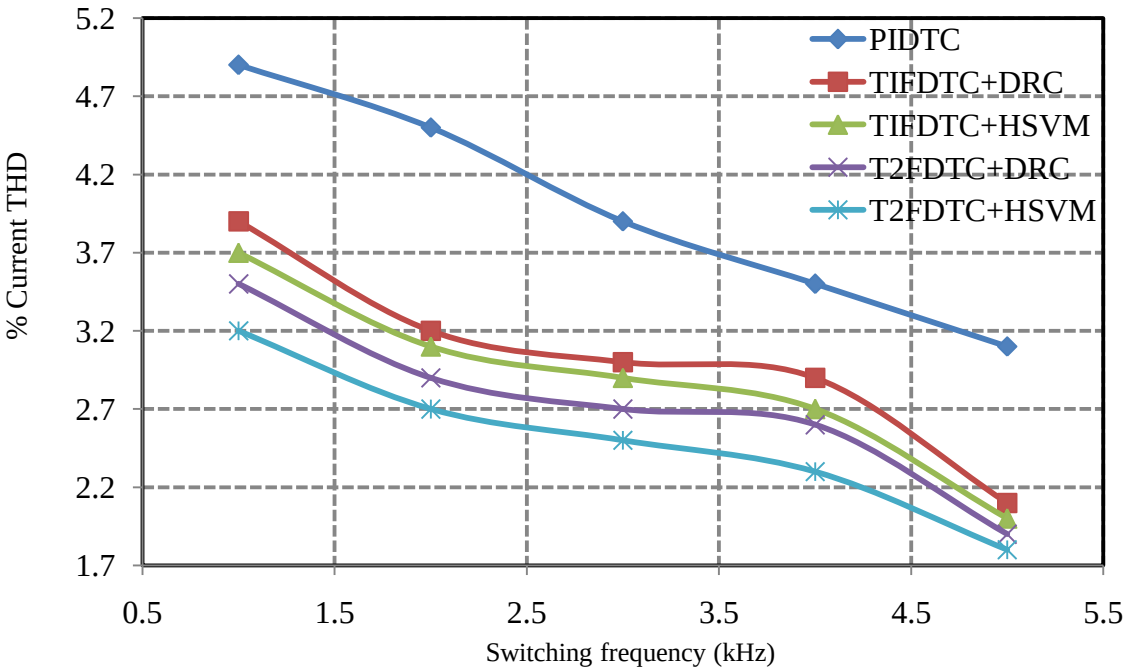


(b) Current THD vs. Switching frequency

Fig. 3.42: No-load THD performance of the IM drive for different control schemes



(a) Voltage THD vs. Switching frequency



(b) Current THD vs. Switching frequency

Fig. 3.43: Full-load THD performance of the IM drive for different control schemes

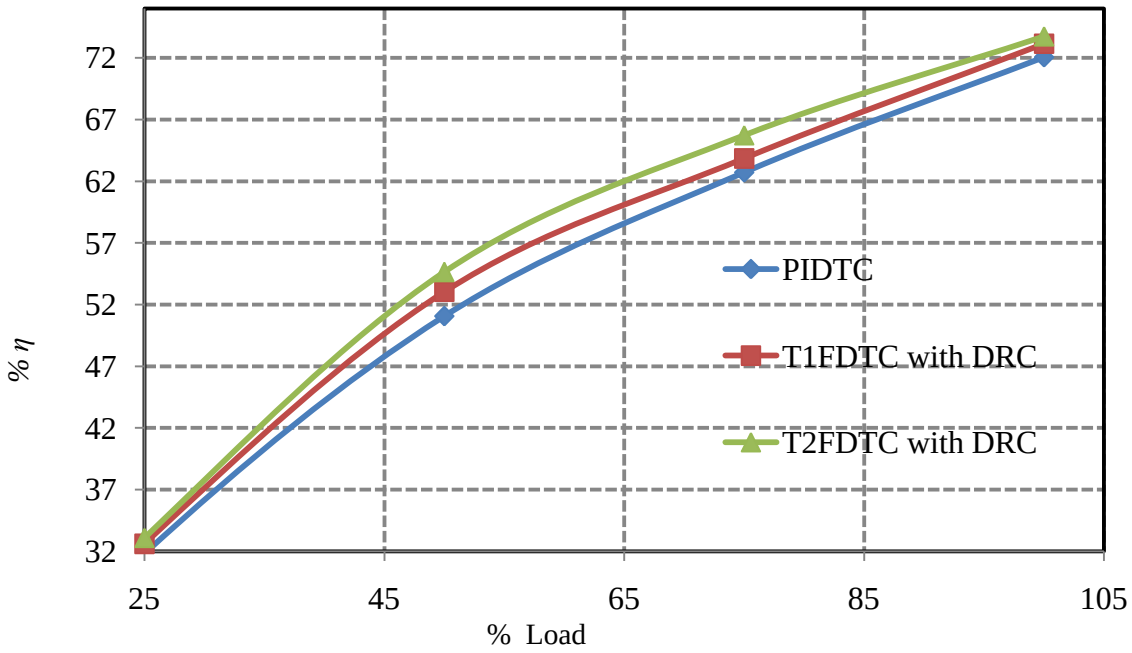
Table 3.9: Overall efficiency of alternative techniques

% Load	V_d(V)	$I_{inv}=I_d$(A)	P_{inv}(W)	ω_m(rad/s)	T_e(N-m)	P_m(W)	$\%\eta = 100*(P_{inv}/P_m)$
PIDTC							
25	640	1.5	**960**	152.8	2	**305.6**	31.83
50	640	1.8	**1152**	152.8	3.85	**588.28**	51.06
75	640	2.55	**1632**	152.8	6.7	**1023.76**	62.73
100	640	2.8	**1792**	152.8	8.45	**1291.16**	72.05
T1FDTC with DRC							
25	640	1.5	**960**	152.8	2.05	**313.24**	32.62
50	640	1.8	**1152**	152.8	4	**611.2**	53.05
75	640	2.55	**1632**	152.8	6.82	**1042.1**	63.85
100	640	2.8	**1792**	152.8	8.58	**1311.02**	73.15
T2FDTC with DRC							
25	640	1.5	**960**	152.8	2.08	**317.824**	33.10
50	640	1.8	**1152**	152.8	4.12	**629.536**	54.64
75	640	2.55	**1632**	152.8	7.02	**1072.66**	65.72
100	640	2.8	**1792**	152.8	8.65	**1321.72**	73.75
T1FDTC with HSVM							
25	640	1.5	**960**	152.8	2.12	**323.936**	33.74
50	640	1.8	**1152**	152.8	4.14	**632.592**	54.91
75	640	2.55	**1632**	152.8	7.09	**1083.35**	66.38
100	640	2.8	**1792**	152.8	8.72	**1332.42**	74.35
T2FDTC with HSVM							
25	640	1.5	**960**	152.8	2.14	**326.992**	34.06
50	640	1.8	**1152**	152.8	4.2	**641.76**	55.71
75	640	2.55	**1632**	152.8	7.1	**1084.88**	66.47
100	640	2.8	**1792**	152.8	8.75	**1337**	74.72

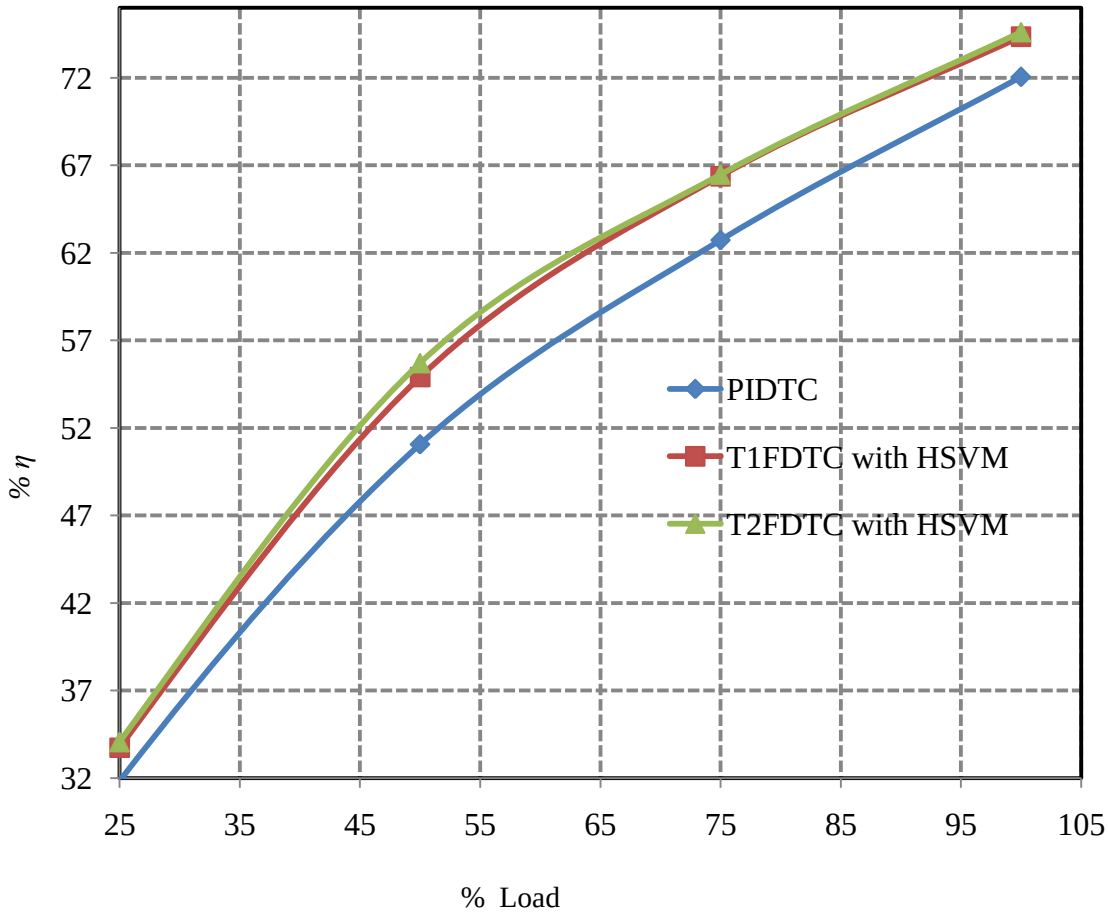
Fig. 3.37 (a) and Fig.3.37 (b) show the percentage of line voltage and current THD for PIDTC of the IM during no-load operation and the corresponding values are 36.5 and 3.9, respectively. The percentage of line voltage and current THDs during no-load for T1FDTC with DRC has 34.9 and 3.0 as shown in Fig. 3.38 (a) and Fig. 3.38 (b), respectively. Fig. 3.39 (a) and Fig.3.39 (b) give the percentage of line voltage and current THDs for T1FDTC with HSVM of the IM during no-load operation and the corresponding values are 33.3 and 2.6, respectively. The T2FDTC of the IM along with DRC provides the no-load line voltage and current THDs of 31.9 and 2.5 as shown in Fig. 3.40 (a) and Fig. 3.40 (b), respectively. Fig. 3.41 (a) and Fig. 3.41 (b) have the percentage

of line voltage and current THDs for T2FDTC with HSVM of the IM during no-load operation and the corresponding values are 30.9 and 2.3, respectively. Therefore, it is observed from Fig. 3.37 to Fig. 3.41 that the T2FDTC with HSVM has provided less voltage and current THDs of 30.9% and 2.3% than other four control schemes control schemes (PIDTC, T1FDTC with DRC, T1FDTC with HSVM, and T2FDTC with DRC). This is due to the fact that the HSVM provided the less RMS flux ripple using T2FLC, the T2FLC effectively deals with the huge ambiguous data using the type reducer, and estimate the control variable very close to the actual value.

Table 3.8 shows the experimental %THD comparison for both line voltage and current under no-load and full-load operaion by changing the switching frequency from 1kHz to 5kHz using different control schemes. Consequenty, a comparative performance is studied and plotted for the corresponding line voltage THD during the no-load and full-load as shown in Fig. 3.42 (a) and Fig. 3.42 (b), respectively. Furthermore, the percentage of current THD vs. switching frequency is plotted for both no-load and full-load operation as shown in Fig. 3.43 (a) and Fig. 3.43 (b), respectively. From Fig. 3.42 and Fig. 3.43, it is observed that the T2FDTC with HSVM provided less voltage and current THD value than PIDTC, T1FDTC with DRC, T1FDTC with HSVM, and T2FDTC with DRC. Moreover, the efficiency also calculated under different loading condition with a fixed switching frequency of 5kHz as given in Table 3.9. A graph is plotted between the percentage of the efficiency and percentage of the load for PIDTC, T1FDTC with DRC and T2FDTC with DRC as shown in Fig. 3.44(a). Here, T2FDTC with DRC of the IM has more efficiency than T1FDTC with DRC and PIDTC. The reason is that the T2FDTC with DRC provides less harmonics/ripples of voltage, current, and torque, which implies the losses should be less and hence the efficiency of the IM drive significantly improved as compared to T1FDTC with DRC and PIDTC. Fig. 3.44 (b) shows the percentage of the efficiency and percentage of the load for PIDTC, T1FDTC with HSVM and T2FDTC with HSVM in which the T2FDTC with HSVM provides higher efficiency at each and every instant of the load as compared to other two control schemes (PDTC and T1FDTC with HSVM). It is concluded that the T2FDTC with HSVM provides the improved efficiency at all loading conditions as compared to the other four control schemes (PIDTC, T1FDTC with DRC, T1FDTC with HSVM, and T2FDTC with DRC). In addition, the percentage of full load efficiency of the IM using T2FDTC with HSVM is 74.72, which is the highest value among the four control schemes as mentioned above.



(a) PIDTC and DRC for T1FDTC and T2FDTC



(b) PIDTC and HSVM for T1FDTC and T2FDTC

Fig. 3.44: Overall efficiency of the IM drive for different control schemes

Table 3.10: Prospectus of different control schemes of the IM drive

Measured parameters	Simulation results					Experimental results				
	PIDTC	T1FDTC		T2FDTC		PIDTC	T1FDTC		T2FDTC	
		DRC	HSVM	DRC	HSVM		DRC	HSVM	DRC	HSVM
$\pm\Psi_{dist}$ (Wb)	0.1	0.085	0.075	0.065	0.52	0.123	0.095	0.085	0.07	0.06
$\pm T_{dNL}$ (Nm)	1	0.86	0.78	0.65	0.55	1.2	0.95	0.85	0.78	0.65
$\pm N_{cDL}$ (rpm)	10	5	4.5	4	4	10	6	6	3	3
$\%V_{NLTHD}$	31.19	29.25	28.93	27.53	25.91	36.5	34.9	33.3	31.9	30.9
$\%I_{NLTHD}$	2.45	2.12	2	1.95	1.85	3.9	3.0	2.6	2.5	2.3
$\%V_{FLTHD}$	31.19	29.25	28.93	27.53	25.91	31.5	30.2	29.6	28.5	27.8
$\%I_{FLTHD}$	2.45	2.12	2	1.95	1.85	3.1	2.1	2.0	1.9	1.8
$\%\eta_{FL}$	72.47	73.50	74.35	74.60	75.03	72.05	73.15	73.75	74.35	74.72
t_{st}(s)	0.27	0.22	0.2	0.2	0.2	1.02	0.95	0.95	0.875	0.85
t_{scs}(s)	1.2	1.175	1.173	1.172	1.172	1.19	1.15	1.149	1.075	105
t_{sr}(s)	3.13	2.9	2.88	2.87	2.868	2.28	2.125	2.125	2	1.97
t_{sr}(s)	4.746	4.51	4.5	4.48	4.487	2.28	2.125	2.125	2	1.97
t_{dl} (s)	4.87	4.85	4.835	4.825	4.823	0.22	0.12	0.12	0.06	0.045

The percentage of improvement of flux distortion, torque distortion, voltage THD, and current THD for T2FDTC along with HSVM of the IM drive during the no-load is 51.21, 45.83, 15.2, and 41 as compared to PIDTC. Moreover, the full-load efficiency of the IM drive for T2FDTC is 74.72%, which is improved by 3.5% over a conventional PIDTC. The comparative performance, such as starting, step change in speed, speed reversal, operation during the load, voltage and current THDs, flux and torque distortion, change in the speed during the load and efficiency at full load of the IM drive with the above control schemes are mentioned in Table 3.10 in detail. Where, Ψ_{NLdst}, T_{NLdist}, Nc_{DL}, $\%V_{NLTHD}$, $\%I_{NLTHD}$, $\%V_{FLTHD}$, $\%I_{FLTHD}$, $\%\eta_{FL}$, t_{st},t_{scs},t_{sr}, and t_{DL}, are the no-load torque distortion (N-m), change in speed during the load (rpm), percentage of no-load voltage THD, percentage of no-load current THD, percentage of full-load voltage THD, percentage of full-load current THD, percentage of full-load efficiency, settling time (s) during starting, settling time (s) during step change in speed, settling time (s) during the speed reversal, and settling time (s) during the load, respectively.

3.8 Conclusion

A two-level inverter fed direct torque and controlled IM drive is simulated in the Matlab environment for two-level voltage source inverter using PIDTC, T1FDTC and T2FDTC.

The PIDTC provides considerable flux and torque ripples at above half of the modulation index as SVM provides more RMS flux ripples. Moreover, it has poor dynamic performance of the IM drive due to poor performance of the PI-controllers. In order to improve the dynamic performance of IM drive, the T1FDTC and T2FDTC are proposed. In both T1FDTC and T2FDTC, the PI-controllers are replaced either type-1 or type-2 fuzzy controllers (T2FCs) to get quick dynamic performance of the IM drive than PIDTC. Because, the T2FC has three-dimensional control with type reduction in defuzzification process to effectively deal with the huge ambiguous data (larger footprint of data) than T1FC. Moreover, Mamdani and centroid method with simple IF and THEN rules are used in both control schemes (T1FDTC and T2FDTC). The steady state ripples in flux, current, and torque of the IM drive with T1FDTC and T2FDTC are improved using either duty ratio control (DRC) or hybrid space vector modulation control (HSVM). The DRC of SVM is independent of the sampling time to improve the firing strength of the inverter, whereas HSVM uses two complementary bus-clamped sequences along with SVM in each sector to reduce RMS flux ripple of the IM. Consequently, the current and torque ripples of IM drive can be improved significantly than PIDTC. A comparative simulated performance of the IM drive during startup, the step change in speed, and load perturbation is presented. However, the T2FDTC with HSVM provides significant improvement in the overall efficiency with less voltage and current THD of the IM drive than T1FDTC and PIDTC. In addition, the dynamic response of the IM drive using T2FDTC with HSVM is improved significantly under any mode of operation. A prototype controller is developed in the laboratory and the control signals for PIDTC, T1FDTC and T2FDTC are generated by the dSPACE DS-1104 controller. In addition to the simulated results, the above control schemes are validated with the experimental results under the same operating conditions. It is concluded that the T2FDTC along with HSVM provides fewer flux ripples, less torque distortion, less voltage and current THD, and more overall efficiency of the IM drive with fast dynamic performance than T2FDTC with DRC, T1FDTC with HSVM, T1FDTC with DRC and PIDTC. The percentage of improvement of flux distortion, torque distortion, voltage THD, and current THD for T2FDTC along with HSVM of the IM drive during the no-load is 51.21, 45.83, 15.2, and 41 as compared to PIDTC. Moreover, the full-load efficiency of the IM drive for T2FDTC is 74.72%, which is improved by 3.5% over a conventional PIDTC.

CHAPTER -4

DIRECT TORQUE CONTROL FOR THREE-LEVEL DIODE CLAMPED INVERTER FED IM DRIVE

4.1 Introduction

In general, the two-level inverter fed IM drives are suitable for low voltage (LV) applications, but not medium voltage (MV) [181-192]. The two-level inverter has few limitations such as high switching frequency, more voltage/current stresses on devices, switching losses, overall device cost of the inverter, etc [192-193]. To overcome the above drawbacks, the multi-level inverter (MLI) is used for medium voltage (MV) applications. To further improve the voltage, current, torque, and flux of the IM drive the two-level voltage source inverter is replaced by three-level diode clamped inverter (TLDCI) [193]. This chapter presents PIDTC, T1FDTC, and T2FDTC of the IM drive using an SVM technique for three-level diode clamped inverter (TLDCI). The above control schemes have been implemented in the laboratory on a 2HP IM through DSPACE DS-1104 controller. In all three control schemes, the voltage across the DC-link capacitors of the TLDCI remains constant without using an extra controller by selecting an appropriate voltage space vector. However, the PIDTC along with TLDCI of the IM provides poor transient performance during startup, a step change in the speed, speed reversal, and step load with considerable current and voltage THD. In addition, it takes more time to reach the steady state with large spikes on capacitor voltages during load or speed variation which is due to poor performance of the PI-controllers (speed and torque). In T2FDTC, the conventional PI-controllers (speed and torque) are replaced by Mamdani type-2 fuzzy controllers using a Centroid method with simple logical rules such as IF and THEN rules. Moreover, the duty ratios are controlled with T2FLC to improve the voltage and current THDs than conventional PIDTC and T1FDTC. The simulated and experimental performance shows that T2FDTC for the three-level inverter fed IM drive provides a fast dynamic response, less current and voltage THDs, considerably less distortion in flux and torque, and fewer spikes on capacitor voltages as compared to PIDTC and T1FDTC.

4.2 Multilevel Inverter

Multilevel inverter (MLI) concept utilizes a higher number of active semiconductor switches to perform the power conversion in small voltage steps. This approach offers several advantages when compared with traditional two-level inverter, such as the smaller voltage steps leads to the production of high quality output waveforms, reduction of the dv/dt stresses and reduction in the electromagnetic interference. Another important feature of MLI is that the semiconductor switches are connected in series, which eliminates over voltage concerns [37, 48-50, 104, 118, 192-193].

Advancement in power semiconductor technology has led to production of switching devices capable of switching at high speeds and at high power levels. The PWM VSIs are being used extensively instead of CSIs in industrial applications owing to their control, flexibility and acceptable harmonic spectrum[23]. As the power rating of the device goes up, the switching frequency has to be reduced to limit the switching power loss. In such situation, MLI configuration is being suggested for reducing the harmonic content of the inverter output at a low switching frequency for high power applications [37-50, 193].

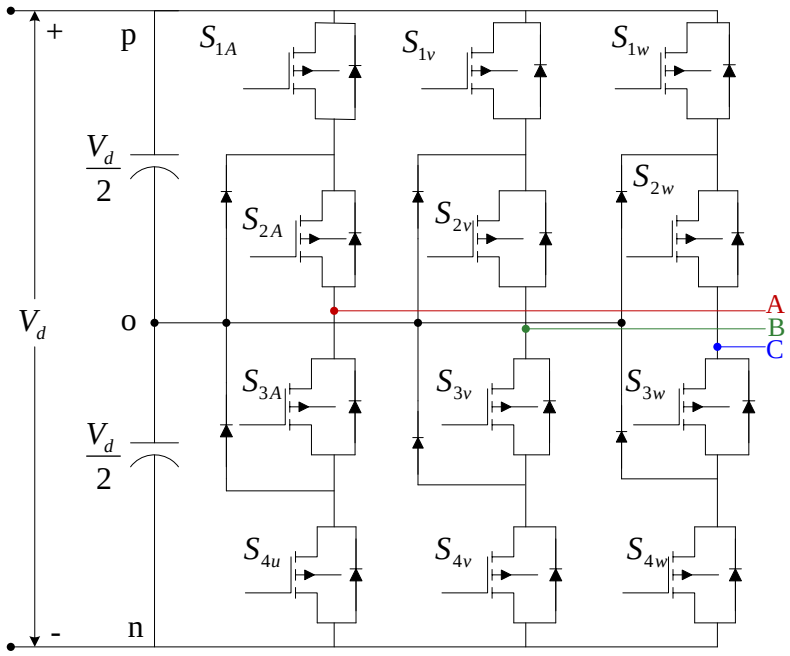


Fig. 4.1: DCMLI structure of the three-level

The three main types of MLIs in use are diode-clamped multilevel inverter (DCMLI), flying-capacitor multilevel inverter (FCMLI) and cascaded H-bridges

multilevel inverter (CHBMLI). The circuit diagrams of these MLIs are shown in Fig. 4.1, 4.2 and 4.3, respectively [103].

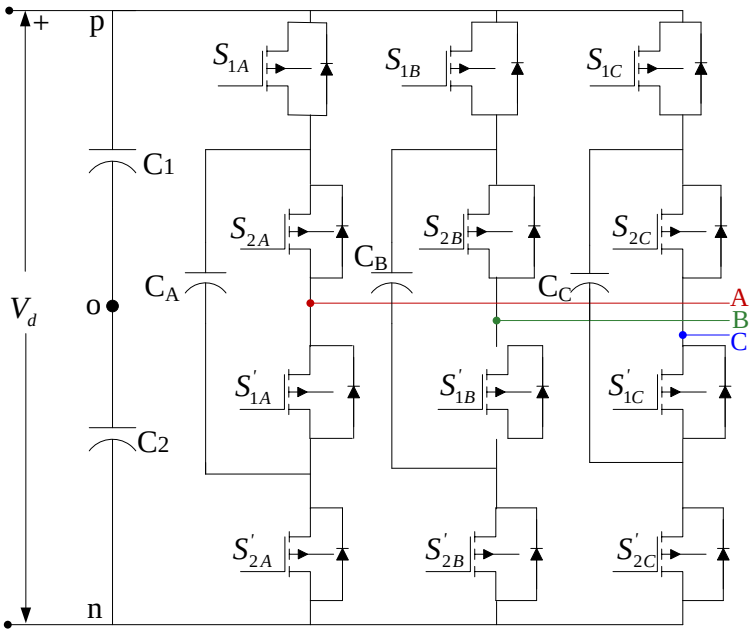


Fig. 4.2: FCMLI structure of the three-level

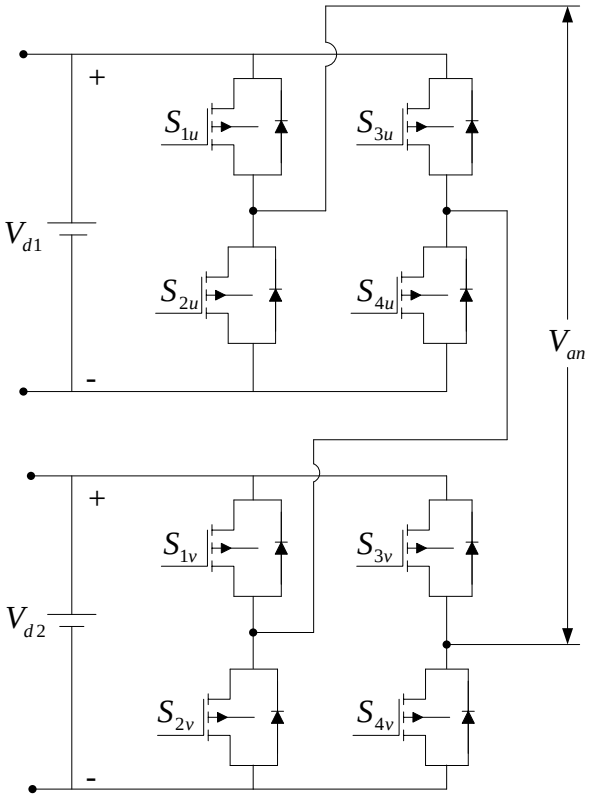


Fig. 4.3: Single phase of CHBMLI structure with two DC sources

The general concept behind this FCMLI is that the added capacitor is charged to one half of the DC link voltage and may be inserted in series with the DC link voltage to form an additional voltage level [104-121]. The capacitor voltage may be either

added to the converter ground or subtracted from the DC link voltage. The main drawbacks are: The number of capacitors required is high compared to other topologies, which is important due to the cost of the reactive devices and the inverter control can be very complicated and the switching losses are high for real power transmission. The CHBMLI is simply a series connection of multiple H-bridge inverters. The CHBMLI introduces the idea of using separate DC sources to produce an AC voltage waveform. The major drawback is that, it needs separate DC sources for real power conversion. Out of the three basic MLI structures, much attention and widely used is the DCMLI because of simplicity of its control [50, 104, 192-193].

4.2.1 Diode-Clamped Multilevel Inverter (DCMLI)

A DCMLI with m-level typically consists of (m-1) capacitors on DC bus and produces m-voltage levels in the phase voltage output. Fig. 4.1 shows a three-level diode clamped inverter (TLDCI). Comparing this topology with that of a standard two-level inverter shows that there is twice as many power electronics switches as well as added diodes. However, it should be noted that the voltage rating of power electronic switches is half of that of the power electronic switches in the two-level inverter. In three-level inverter, the voltage across each capacitor is $0.5V_d$, and each device voltage stress is limited to capacitor voltage level $0.5V_d$ through clamping diodes. A generalized m-level inverter leg requires (m-1) capacitors, 2(m-1) switching devices and (m-1)*(m-2) clamping diodes. For the operation of TLDCI, there are three switching states for each inverter leg; p, o and n. Where p means that the upper two switches in a leg 'A' are 'on' and the inverter terminal voltage is $+0.5V_d$;n means that the lower two switches are 'on' with a terminal voltage of $-0.5V_d$;o signifies that the inner two switches are 'on' with a terminal voltage of zero. The corresponding switching states of three-level inverter in one of the phase (A) are given in Table 4.1 [118, 192-193].

Table 4.1:Three level diode clamped inverter per phase switching states

Switching symbol	**Switching states**				**Pole voltages**	**Line voltages**
	S_{1A}	**S_{2A}**	**S_{1A}'**	**S_{2A}'**		
p	1	1	0	0	$0.5V_d$	V_d
o	0	1	1	0	0	$0.5\ V_d$
n	0	0	1	1	$-0.5V_d$	0

4.2.2 SVM Technique for Three-Level Inverter

In MLIs, the SVM methodologies have the advantage of increased inverter output voltage. In this modulation technique as used in other works [38, 83], the space vector diagram of MLI is divided into different forms of sub-diagrams, in such a manner that the implementation becomes simpler. However, these works do not reach a generalization of the two-level SVM because either they divide the diagram into triangles or interfere geometrical forms. In this work, a simple and fast method that divides the space vector diagram of three-level inverter into several small sectors, each sector again divided into four sub-sectors as shown in Fig. 4. is implemented [159-169]. In this manner, the developed two-level conventional, type-1 and type-2 fuzzy based DTC methods can be utilized in this three-level SVM method [160-163].

4.2.3 Basic Principle of SVM Method

The design of three-level SVM is difficult to understand as compared to two-level inverter. However, the pulses are generated to the inverter as similar to the two-level SVM. The three-level diode clamped inverter (TLDCI) is shown in Fig. 4.1. It has twenty seven switching state vectors in which there are three null state vectors and twenty four active state vectors as represented in Fig. 4.4 [160-169].

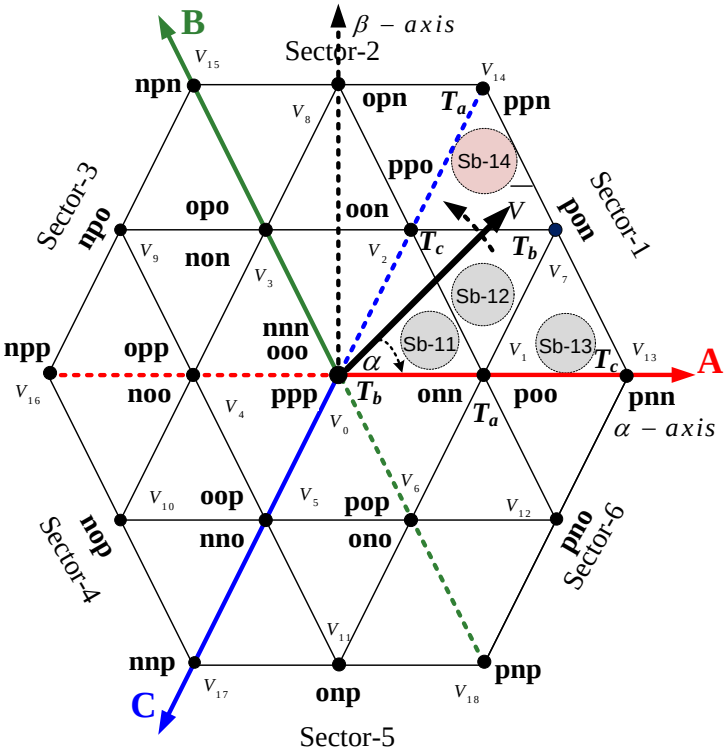


Fig. 4.4:Space vector diagram for three-level inverter

Table 4.2: Voltage Vectors and Switching States

Space vector		**Switching states**		**Vector classification**	**Vector magnitude**
V_0		[ooo, ppp, nnn]		Zero vector	0
V_1		**p-type**	**n-type**	Small voltage vector	$0.333V_d$
	V_{1p}	[poo]			
	V_{1n}		[onn]		
V_2	V_{2p}	[ppo]			
	V_{2n}		[oon]		
V_3	V_{3p}	[opo]			
	V_{3n}		[non]		
V_4	V_{4p}	[opp]			
	V_{4n}		[noo]		
V_5	V_{5p}	[oop]			
	V_{5n}		[nno]		
V_6	V_{6p}	[pop]			
	V_{6n}		[ono]		
V_7		[pon]		Medium vector	$0.5773V_d$
V_8		[opn]			
V_9		[npo]			
V_{10}		[nop]			
V_{11}		[onp]			
V_{12}		[pno]			
V_{13}		[pnn]		Large vector	$0.667V_d$
V_{14}		[ppn]			
V_{15}		[npn]			
V_{16}		[npp]			
V_{17}		[nnp]			
V_{18}		[pnp]			

Moreover, these twenty seven switching state vectors again divided into zero voltage vectors, small voltage vectors, medium voltage vectors, and large voltage vectors as given in Table-4.2 and they have [165-170]

The magnitude of three zero voltage vectors are

$$V_0 = 0 \tag{4.1}$$

The magnitudes of twelve small voltage vectors are

$$V_1 = V_2 = V_3 = V_4 = V_4 = V_5 = V_6 = 0.33V_d \tag{4.2}$$

The magnitudes of six medium voltage vectors are

$$V_7 = V_8 = V_9 = V_{10} = V_{11} = V_{12} = 0.5773V_d \tag{4.3}$$

The magnitudes of six large voltage vectors are

$$V_{13} = V_{14} = V_{15} = V_{16} = V_{17} = V_{18} = 0.667V_d \tag{4.4}$$

Three-level inverter has 27 switching state vectors in which three are the zero voltage vectors (V_0) and twenty-four are active state vectors as represented in Fig. 2(b). Twenty-four active vectors again divided into, small voltage vectors (V_0, V_1, V_2, V_4, V_5, and V_6), medium voltage vectors (V_7, V_8, V_9, V_{10}, V_{11}, and V_{12}), and large voltage vectors (V_{13}, V_{14}, V_{15}, V_{16}, V_{17}, and V_{18}), and their magnitudes are $0.33V_d$, $0.5773V_d$, and $0.667V_d$, respectively [49-50]. Moreover, the active voltage vectors are phase displaced by the same angle, i.e., 60° with respect to their group (small/medium/high) of voltage vectors only as shown in Fig. 4.4 [164-170]. To generalize the three-level SVM into two-level SVM then the three-level SVM has been divided into six sectors i.e. sector-1, sector-2, sector-3, sector-4, sector-5, and sector-6. However, each sector again divided into four sub-sectors. The sector-1 is shown in Fig. 4.4, which is divided into four sub-sectors Sb-11, Sb-12, Sb-13, and Sb-14. A 3-phase TLDCI is shown in Fig. 4.1 in which the nodes p, o, and n indicate the +ve, neutral, and negative positions of the inverter and the corresponding voltages are found when top, middle, and bottom two switches per phase are on, respectively. The corresponding three pole voltages per phase ($V_{Ao}/V_{Bo}/V_{Co}$) are given as $+0.5V_d$, 0, and $-0.5V_d$ when A, B, and C phases are connected to p, o, and n, respectively [104,167-169].

4.2.4 Capacitor Voltage Balance for TLDCI

In general, the TLDCI faces voltage balance problem on capacitors (C_1 and C_2) that can be improved using SVM algorithm without the need of an extra controller in which, the appropriate switching vector is selected based on the reference vector position without

using an extra controller [36-39]. Fig. 4.5 shows the performance of capacitor voltages for different switching vectors involved at sector-1 region.

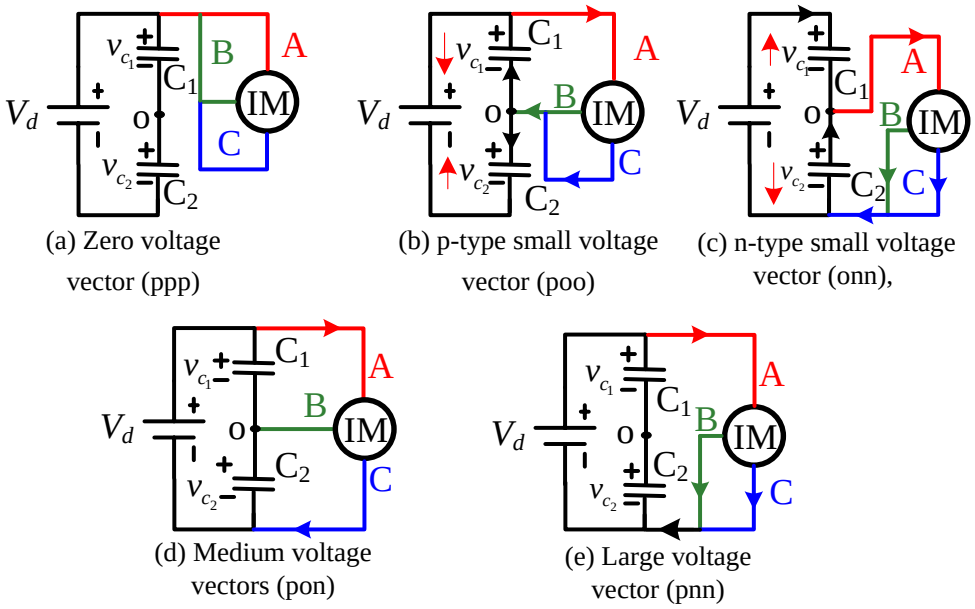


Fig. 4.5: Effect of capacitor voltages for the corresponding switching states

Zero and large voltage vectors: The zero and large voltage vectors are shown in Fig. 4.5(a) and (e) in which there is no chance of current flow in capacitors and hence the constant voltage will be maintained in both capacitors [167-169].

Small voltage vectors: Fig. 4.5(b) and (c) belong to the p and n type small voltage vectors. The corresponding voltage across dc-link capacitor C_2(v_{c_2})increases/decreases based on current flow direction. However, the voltage across the dc-link capacitor C_1 (v_{c_1}) is quite opposite to v_{c_2} as shown in Fig. 4.5(b) and (c) [128, 132-137, 167-170]. Hence, the average value of v_{c_1} and v_{c_2} is maintained constant when p and n-type small voltage vectors are operated once at half of the switching period.

Medium voltage vector: The dc-link voltages v_{c_1} and v_{c_2} are kept constant value, while operating medium voltage vector because there is no chance of current flow through the capacitors (C_1 and C_2) and phase B as shown in Fig. 4.5(d) [36-38, 168-169, 192-194].

Therefore, the capacitor voltages are well balanced and maintained constant for a given switching period by using zero, medium and large voltage vectors. They can be activated once per half of the switching period. Moreover, the small voltage vectors are operated twice per half of the switching period to maintain the constant voltages across

the DC-link capacitors. Similarly, the process remains the same to keep the constant voltage across the DC-link capacitors in another sector region also.

4.2.5 Volt-second Balance Principle for three-level SVM

The design of three-level SVM is a little difficult to understand as compared to two-level. As similar to the two-level inverter, the pole voltages of three-level SVM inverter are easily developed by selecting a single switching transition from one state to another. In addition, the capacitor voltage balance problem can also be improved by selecting the optimum switching states without using an extra controller (as stated above). To generalize the three-level SVM into two-level SVM, the three-level SVM has been divided into six sectors, i.e., sector-1, sector-2, sector-3, sector-4, sector-5, and sector-6 as shown in Fig. 4.4. However, each sector is again divided into four sub-sectors. Let us consider the sector-1 that is divided into four sub-sectors, i.e., Sb-11, Sb-12, Sb-13, and Sb-14 as shown in Fig. 4.6.

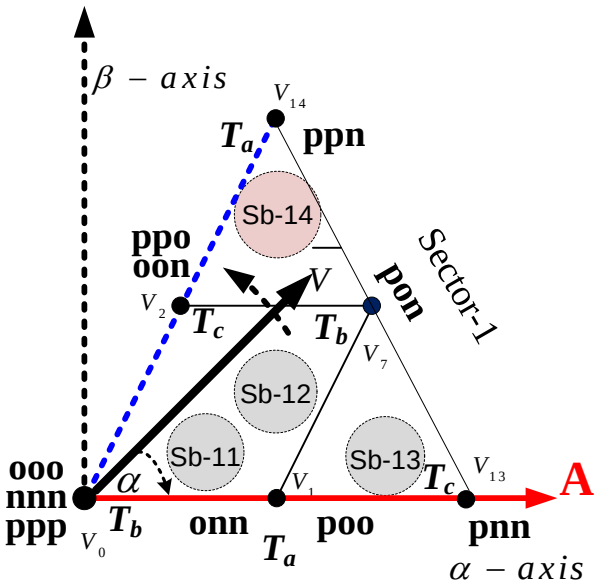


Fig. 4.6:Sector-1 diagram for three-level SVM

The volts-second balance principle is applied when the reference vector is in sub-sector region-4 (Sb-14) [136, 138, 144, 104, 169] as

$$\left|\overline{V}\right| \angle \alpha^{\circ} T_s = V_2 \angle 60^{\circ} T_a + V_7 \angle 30^{\circ} T_b + V_{14} \angle 60^{\circ} T_c \quad (4.5)$$

where $\overline{V}$ and T_s are reference vector and sampling time ($T_s = T_a + T_b + T_c$). By separating real and imaginary part from the (4.5), T_a, T_b, and T_c are calculated as

$$T_a / 2T_s = (M \sin\alpha - 0.5) \tag{4.6}$$

$$T_b / 2T_s = M \sin(60° - \alpha) \tag{4.7}$$

$$T_c / 2T_s = 1 - M \sin(60° + \alpha) \tag{4.8}$$

Where M is the modulation index ($\sqrt{3}\left|\overline{V}\right| / V_d$).

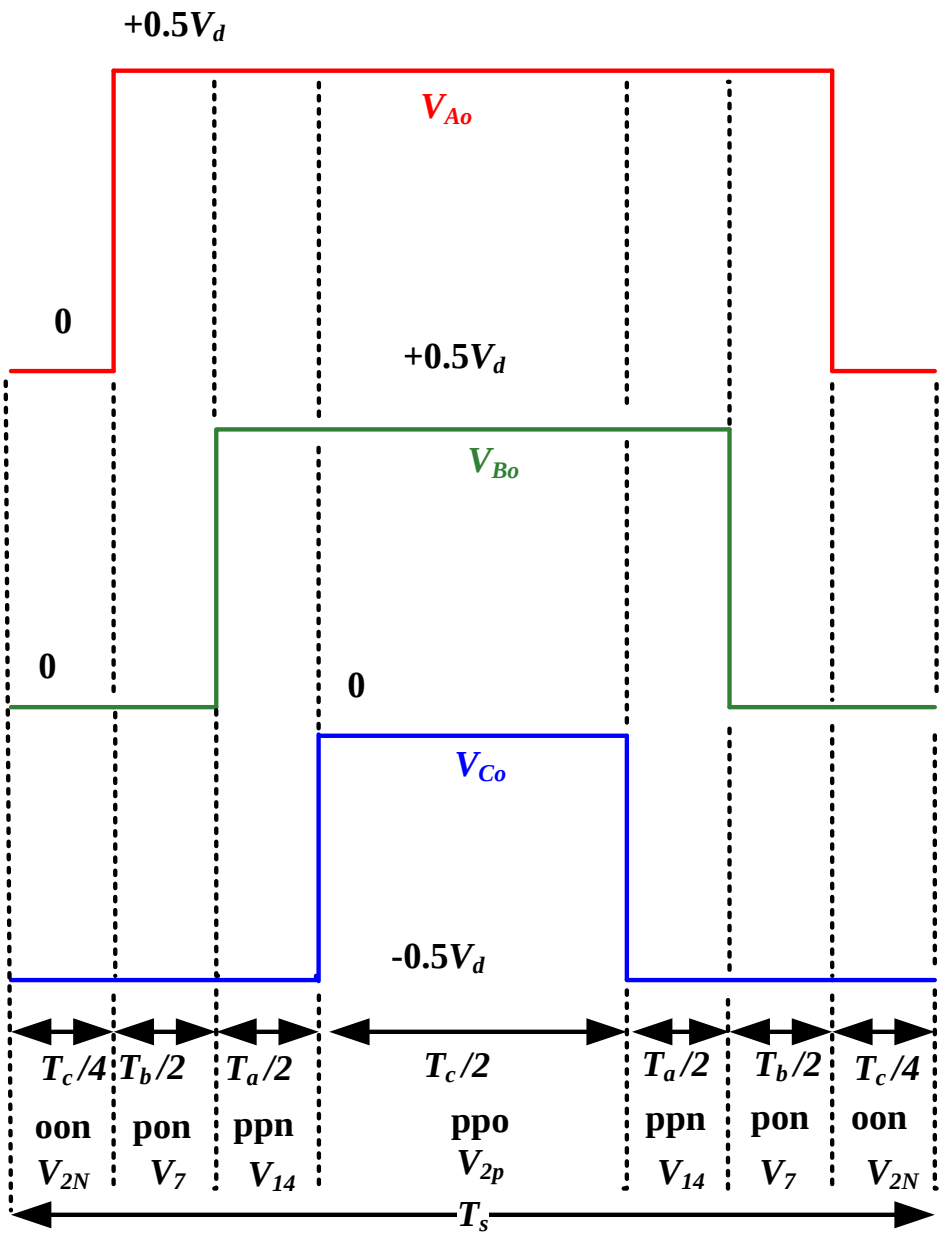


Fig. 4.7:Pole voltages of space vector modulation

The corresponding pole voltages for three phases are found using (4.6) to (4.8) as shown in Fig. 4.7 when the reference vector is at Sb-14 region. Similarly, the above process

remains same to find the switching time and develop the pole voltages of the inverter in other sub-sector regions also [145]-[170].

Table-4.3: Switching time calculation at sector-1 region

Switching times	**Sub-sectors in the sector-1 region**			
	Sb-11	**Sb-12**	**Sb-13**	**Sb-14**
$T_a/2T_s$	0.5-*Msin(60-α)*	0.5-*Msinα*	1-*Msin(60+α)*	*Msinα*-0.5
$T_b/2T_s$	0.5 *-Msin(60-α)*	*Msin(60-α)* -0.5	*Msinα*	*Msin(60-α)*
$T_c/2T_s$	*Msinα*	*0.5- Msin(60-α)*	*Msin(60-α)-0.5*	*1-Msin(60+α)*

The switching time periods are calculated for remaining three sub-sectors in a sector-1 (Sb-11, Sb-12, Sb-13, and Sb-14) as shown in Table-4.3. The equations in Table-3 are also used to find the switching times when the reference vector is in other sectors (like Sector-2, Sector-3, Sector-4, Sector-5, and Sector-6) then the equation for switching times in each sector are updated by 60° or multiple of 60° subtracted from the angle α such that the modified angle falls into the range is from 0° to 60° for easy calculations. Therefore, the switching time periods for the other sectors, sector-2, sector-3, sector-4, sector-5, and sector-6 can be updated by incrementing α by 60°, 120°, 180°, 240° and 300°, respectively [45-50, 165, 192-193]. Similarly, the PWM pulses are developed for a full cycle.

4.3 Type-1 Fuzzy Direct Torque Control

By transforming the three-level space vector plane into two-level space vector plane and redefining the reference voltage vector as explained in the previous sections, the developed two-level T1FDTC in the previous chapter is utilized for generating equivalent two-level switching pulses in this three-level SVM [58-65, 79-89, 169]. The obtained equivalent two-level switching states are compared with three-level space vector diagram to generate the three level switching pulses for the three-level inverter as explained in Section 4.2. The block diagram of three-level SVM with the proposed T1FDTC is shown by dotted lines in Fig. 4.8 in which the speed and torque PI-controllers are replaced by T1FLC and also the duty ratios are controlled independent of the sampling time using T1FLC [40-52, 80-107].

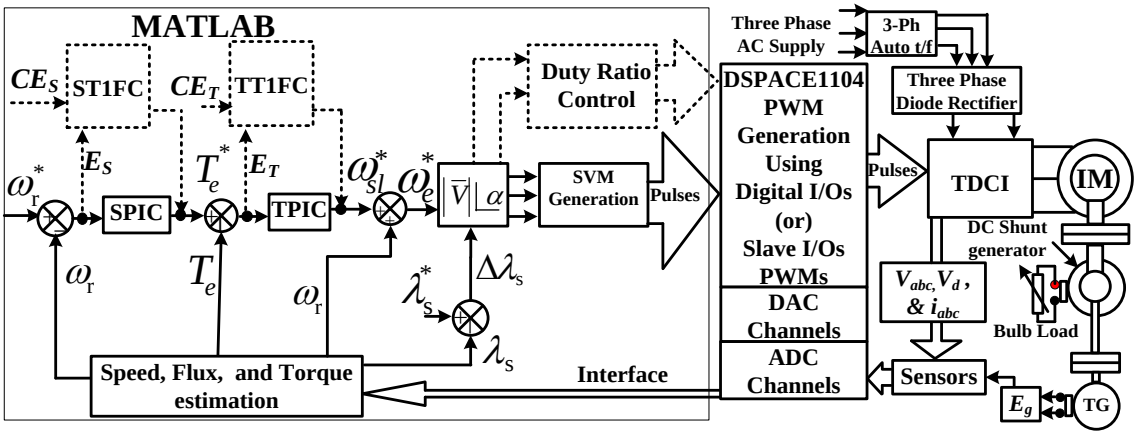


Fig. 4.8: T1FDTC for three-level inverter

The fuzzy rules are constructed for the scenario with fast rise time and less overshoot. Usually, these rules are determined by human experts via pre-learned algorithm, i.e., the person practically experienced while studying the IM behavior in each and every mode of operation and set the MFs and rules accordingly [30]-[33]. The sub-sector duty ratios for all sectors is explained previously Chapter-3.2, which are independent of the switching time period to improve the firing strength of the inverter as compared to the PIDTC. This is because torque and flux are directly proportional to voltage. Moreover, PI-controllers are controlled using the Mamdani type FLC as it sets the gains appropriately for all modes of the IM drive using simple rules (IF, THEN, AND, OR, and NOT) to improve the dynamic performance of the IM drive for TLDCI as compared to PIDTC [99-105].

4.4 Type-2 fuzzy Direct Torque Control

To further improve the dynamic performance of the IM drive from the huge ambiguous data, the T1FLCs are replaced by T2FLCs in which speed and torque PI-controllers are replaced by T2FLCs and controls the duty ratios like T1FLC [106-139].

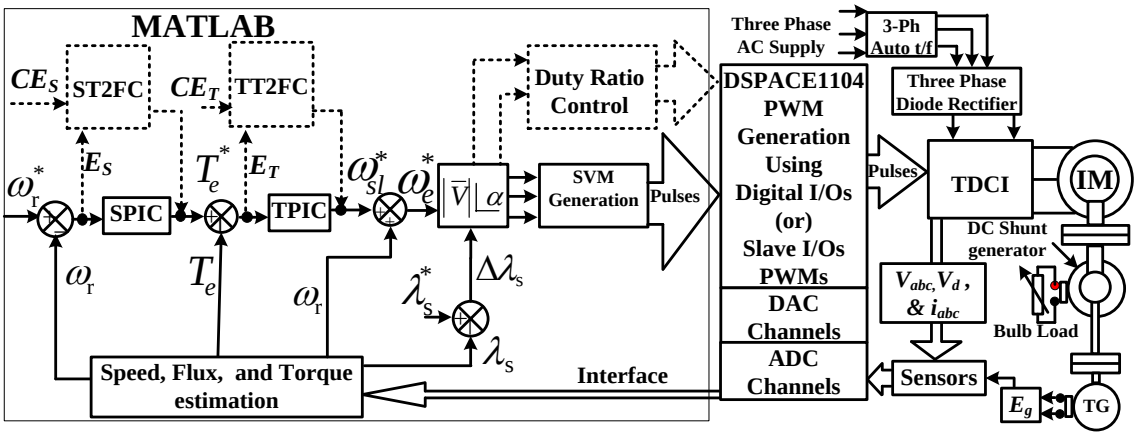


Fig. 4.9: Structure of T2FDTC for three-level inverter

In this, after obtaining the corrected two-level reference voltage vector and angle θ, a two-level T2FDTC with duty ratio control which is implemented in the previous chapter is used in the place of conventional SVM to generate equivalent two-level switching pulses. The two-level switching pulses are converted into three-level switching pulses, which is described in Section 4.3. The block diagram of the proposed T2FDTC for three-level SVM is shown by dotted lines in Fig. 4.9. Moreover, the design procedure for T2FDTC along with duty ratio control remains the same, which is explained in detail in the previous Chapter-3 [100-115, 121, 145-460].

4.5 Duty Ratio Control for T1FDTC and T2FDTC

Fig. 4.10 shows the duty ratio control (DRC) for SVM in which the corresponding duty ratios are developed with the help of either T1FLC or T2FLC and the switching pulses are developed to the inverter with the help of repetitive counter and DRC, which is independent of sampling time T_s like two-level inverter which is discussed in previous Chapter-3 [138].

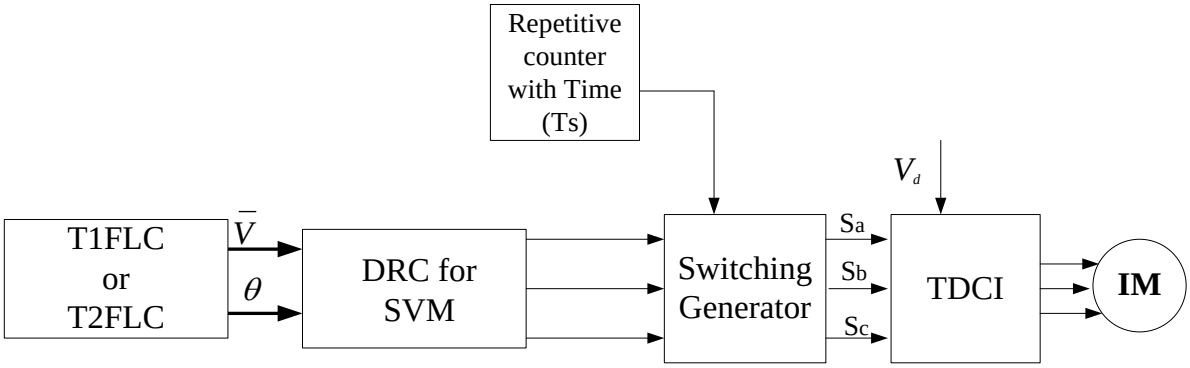


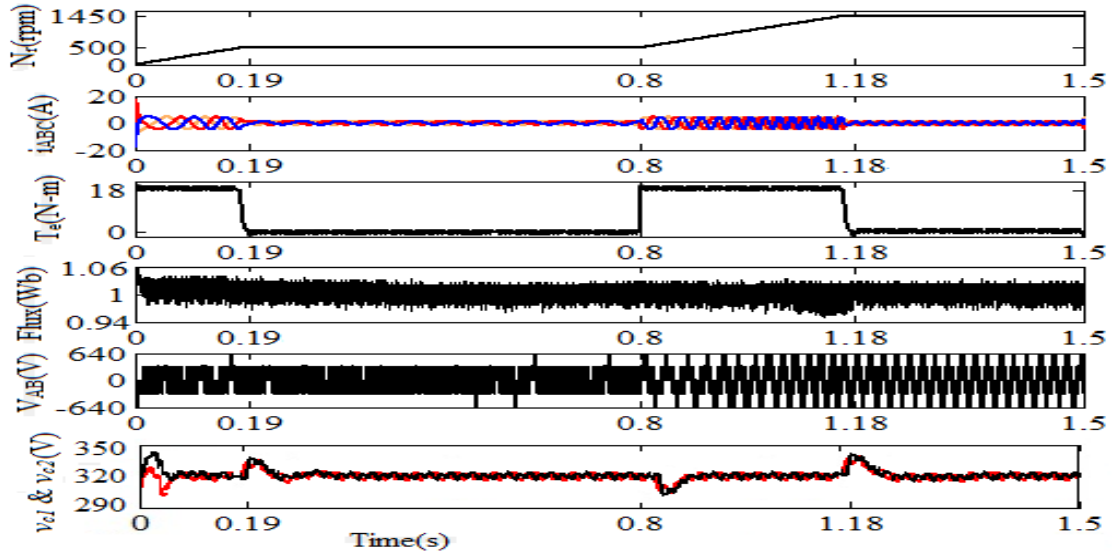
Fig. 4.10: DRC with T1FDTC or T2FDTC

The duty ratios of T1FLC and T2FLC are independent of the sampling time and it can improve the quality of voltage or current waveforms under steady state by improving firing pulse of the inverter, which leads to improve the flux and torque performance of the IM drive rather than PIDTC [137]-[138].

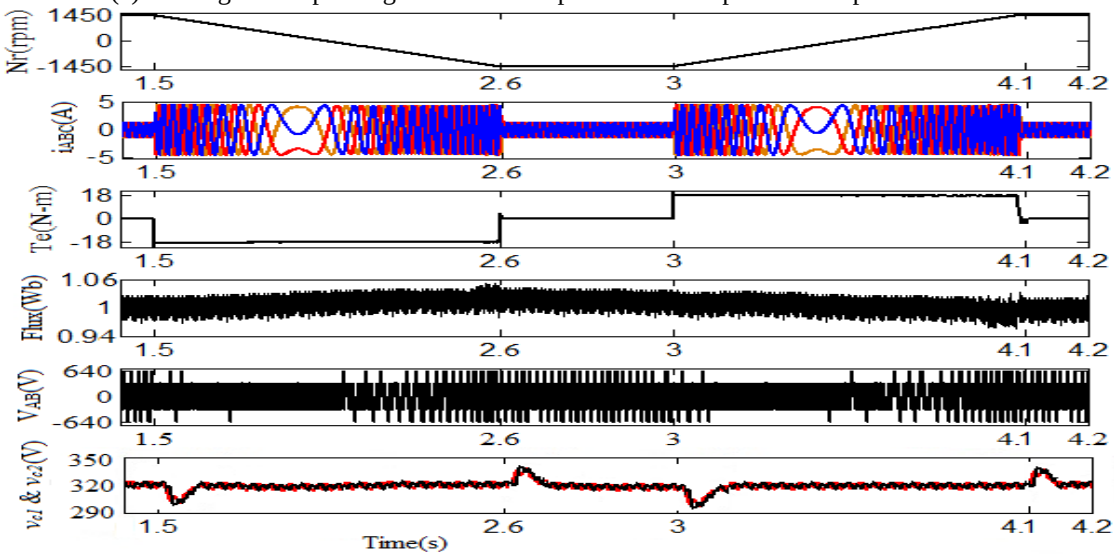
4.5 Results and Discussion

4.5.1 Simulation Results

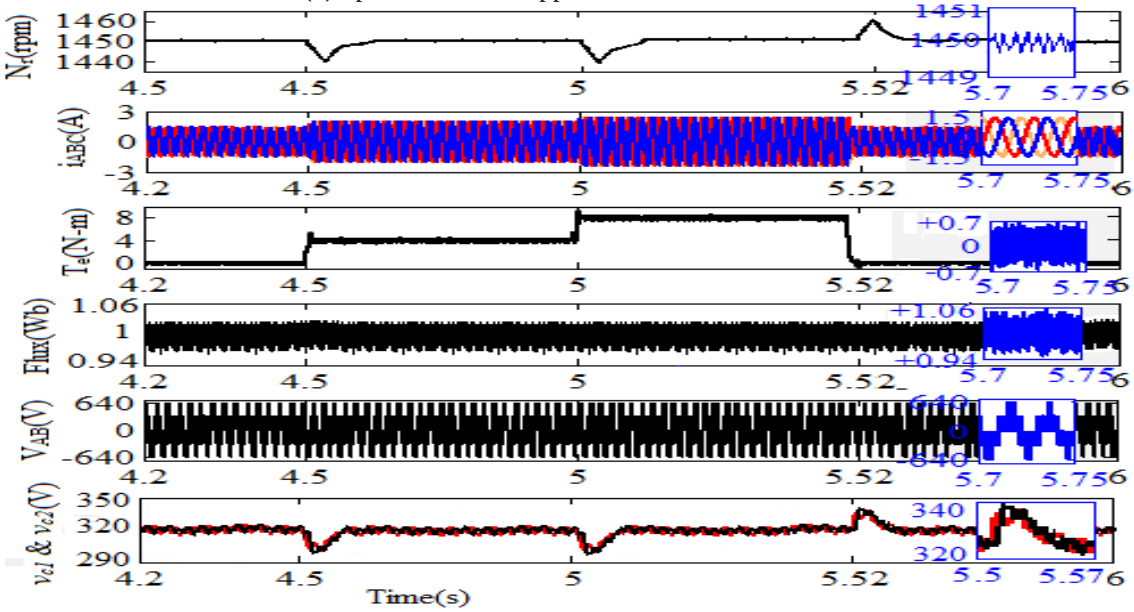
The PIDTC is simulated in MATLAB using a three-level SVM inverter with the switching frequency of 5 kHz, and the sampling time of 40μs for 2HP IM. The reference speed during starting is taken as 500rpm, and subsequently a step change in reference speed from 500 rpm to 1450 rpm is initiated at 0.8s with the applied DC-link voltage of 640V as shown in Fig. 4.11 (a). Initially, a rotating flux is developed in stator because of the supply provided by the inverter. Consequently, the high starting torque and currents are developed and later speed is built up by the motor to run upto the required speed. The IM is settled at 0.19s when applied a reference speed of 500rpm at starting and the corresponding performance of the IM such as speed, three phase current, electromagnetic torque developed by the motor, stator flux, line voltage of the inverter and capacitor voltages (v_{c1} and v_{c2}) are shown in Fig. 4.11 (a). At starting, half of line voltage is enough to reach the required speed (500rpm) of IM, and hence the reference vector should be within the inner hexagon of the space vector region. The line voltage and flux are almost the same from starting to the steady state. However, there is a sudden increase in capacitor voltages (v_{c1} and v_{c2}) at starting as well as just before getting the steady state. This is because of the capacitors act like charging and later it settles down within 2 to 3 cycles by selecting appropriate switching vector. Moreover, the flux distortion is varied from 0.94Wb to 1.06Wb, i.e., ±0.06Wb. When a reference speed of IM drive changes from 500rpm to 1450rpm at 0.8s as shown in Fig. 4.11 (a) then the IM develops a large electromagnetic torque and currents to get required speed (reference speed of 1450rpm) of the IM. After reaching the reference speed at 1.18s the IM settles at 1450rpm as shown in Fig. 4.11(a). However, the three levels appeared on line voltage, which implies that the reference vector now crosses to the outer hexagon region and utilized full of DC-link voltage (640V).Moreover, the capacitor voltages reduced and increased significantly during sudden increase and decrease of the IM currents at 0.8s and 1.18s, respectively, because the capacitors are discharging and charging the energy when the IM draws large or small currents through the capacitors and later settles down after 2 to 3 cycles like a buffer.



(a) Starting and step change in reference speed from 500rpm to 1450rpm at 0.5s

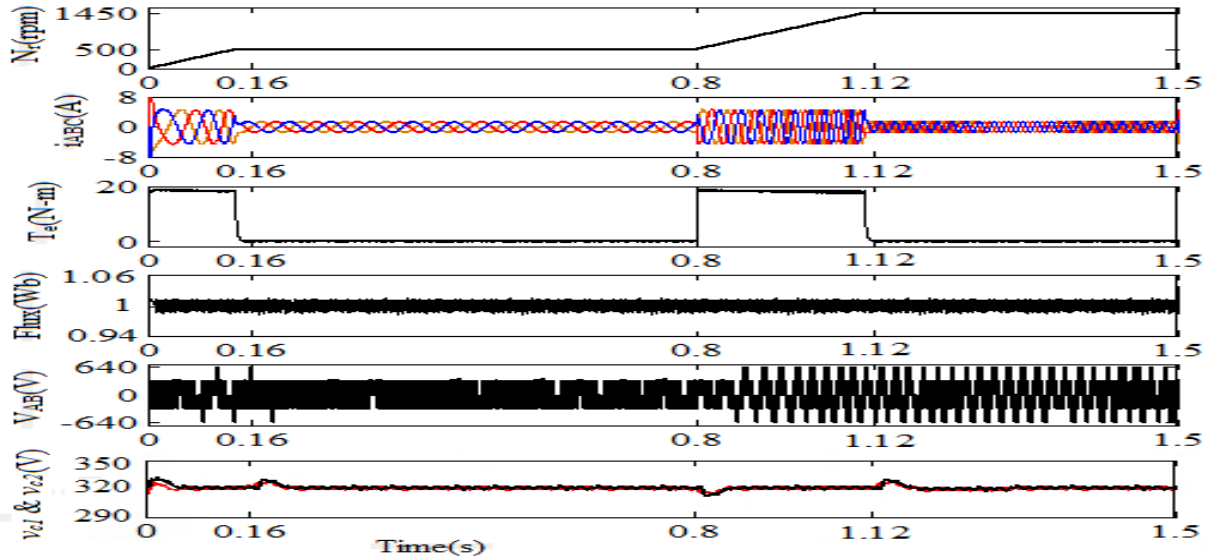


(b) Speed reversal is applied at 1.5s and 3.2s

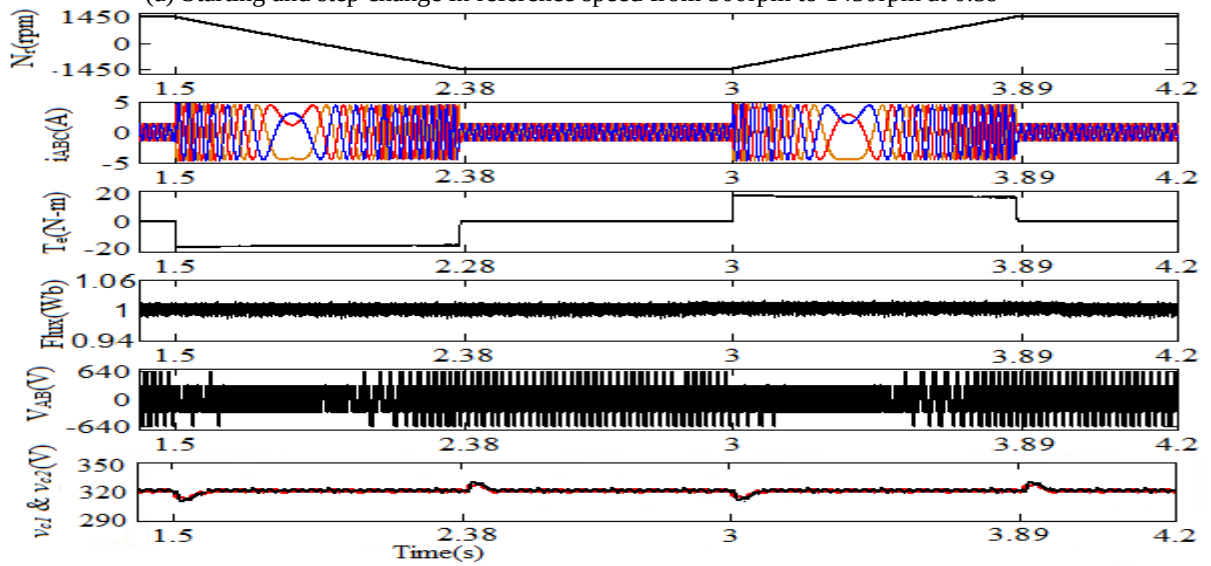


(c) Load of 4N-m, 8N-m, and 0N-m is applied at 4.8s 5.2s and 5.55s

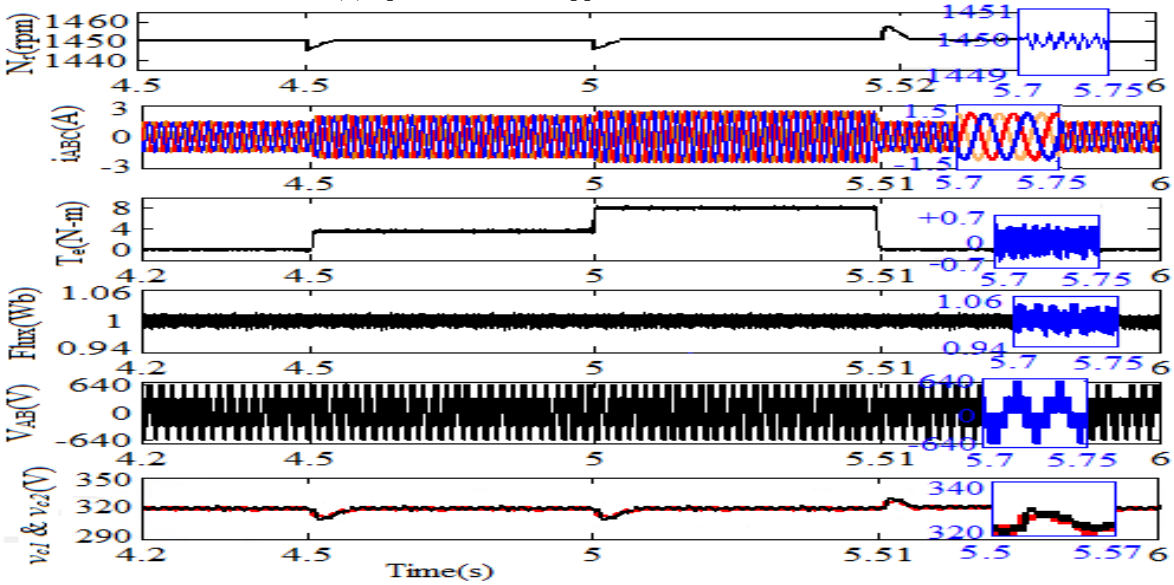
Fig. 4.11: PIDTC of IM drive under different operating modes



(a) Starting and step change in reference speed from 500rpm to 1450rpm at 0.5s

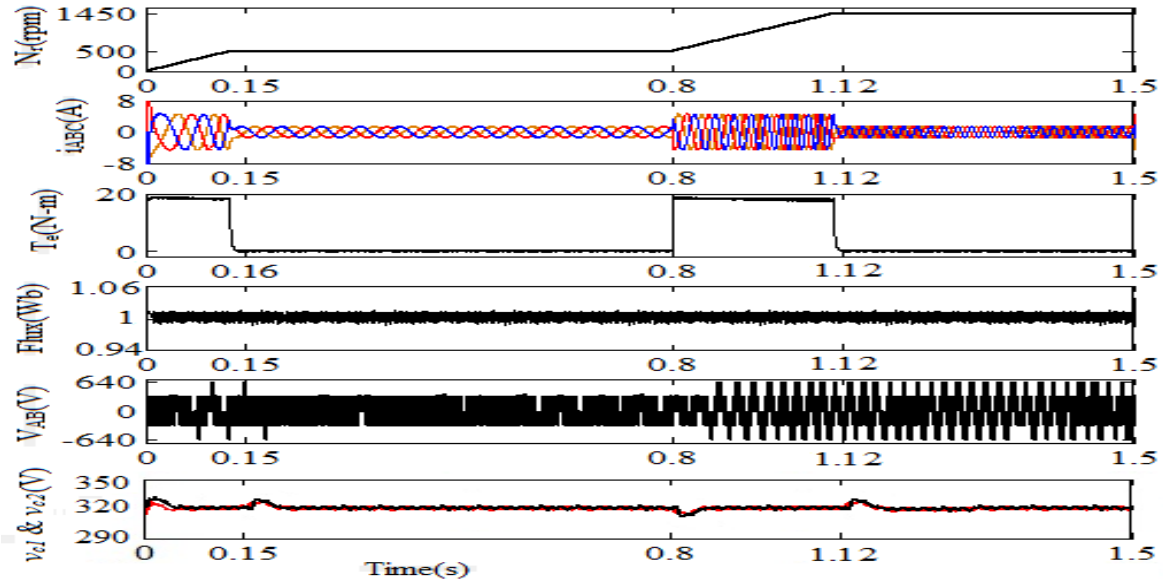


(b) Speed reversal is applied at 1.5s and 3.2s

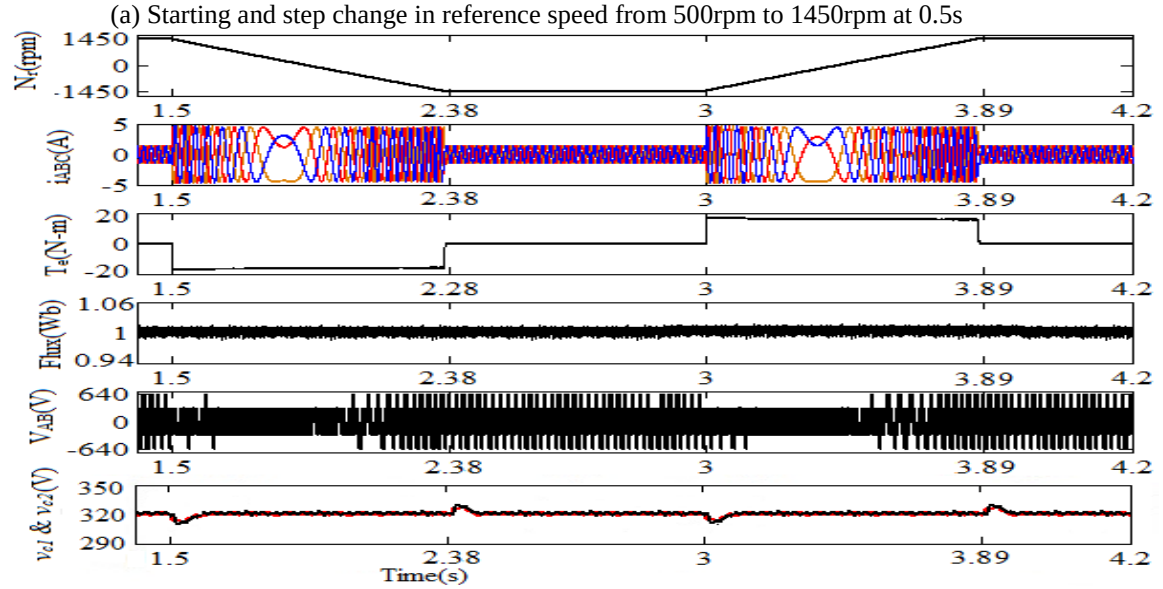


(c) Load of 4N-m, 8N-m, and 0N-m is applied at 4.8s 5.2s and 5.55s

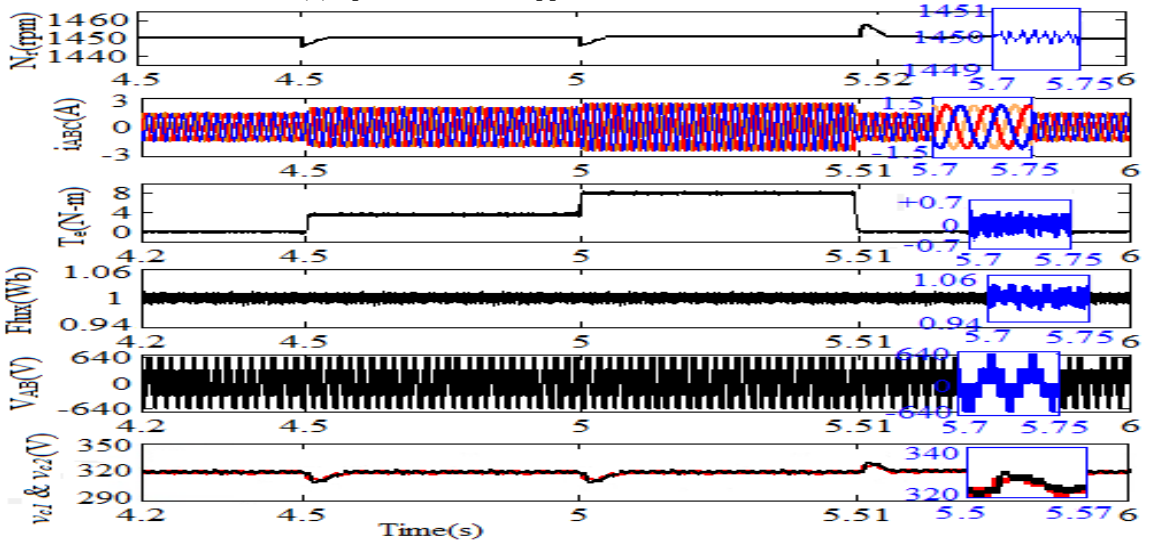
Fig. 4.12: T1FDTC of IM drive under different operating modes



(a) Starting and step change in reference speed from 500rpm to 1450rpm at 0.5s



(b) Speed reversal is applied at 1.5s and 3.2s



(c) Load of 4N-m, 8N-m, and 0N-m is applied at 4.8s 5.2s and 5.55s

Fig. 4.13: T2FDTC of IM drive under different operating modes

When the speed reversal is initiated at 1.5s, then the IM behavior is shown in Fig. 4.11 (b).To get the required speed of -1450rpm, a larger amplitude of the current (5A) and high torque of -20Nm are developed during speed reversal. The current directions also get reversed when the speed crosses to zero value and the IM is settled to -1450rpm at approximately 2.6s as shown in Fig. 4.11 (b). Moreover, the capacitor voltages are reduced and increased significantly during the sudden increasing and decreasing of the IM currents at 1.5s and 2.6s, respectively.

Now, the speed reversal is initiated again for PIDTC of IM at 3.2s then the corresponding operation of the IM is shown in Fig. 4.11 (b), which clearly shows a mirror image in the previous case (for the duration of 1.5s to 2.6s) of the IM drive. Consequently, the steady state of the IM is reached by 4.1s.

The load of 4 N-m, 8 N-m, and 0 N-m is applied to the IM at 4.5s, 5s and 5.5s, respectively, as shown in Fig. 4.11 (c). The peak currents at above-mentioned instants are 2.2A, 2.9A, and 1.5A, respectively. Moreover, the capacitors behave like discharging, discharging, and charging during those instants of applied load. Nevertheless, the flux is maintained almost constant throughout the operation. A sudden drop in the speed of the IM is approximately ±10rpm for every change in load torque. However, the electromagnetic torque and flux distortion of an IM drive under no-load condition varies approximately ±0.7Nm and ±0.0.06Wb, respectively as shown in Fig. 4.11 (c).

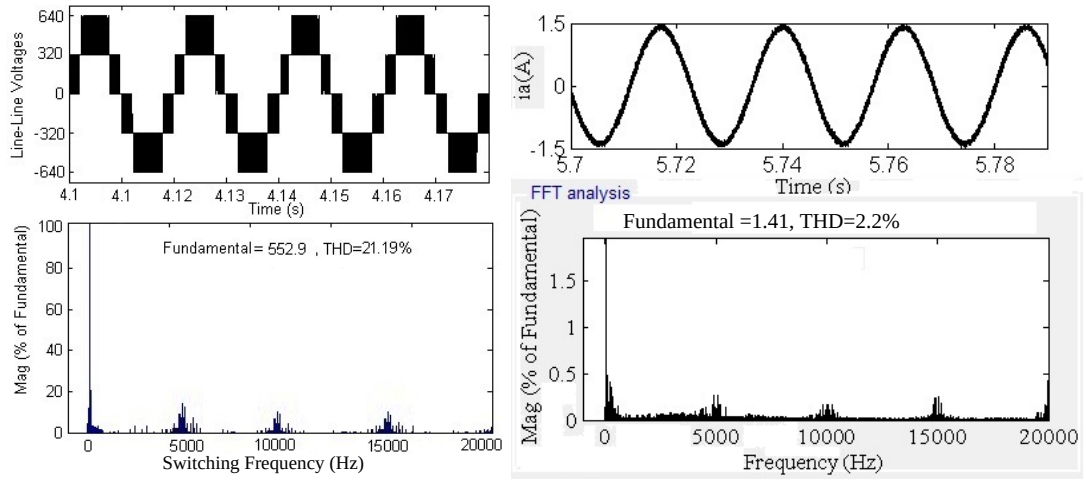
T1FDTC: With the similar operating conditions of PIDTC, the performance of the IM drive is also simulated for T1FDTC as shown in Fig. 4.12. Fig. 4.12 (a) shows the performance of the IM during starting while applying reference speed of 500rpm and step change in reference speed from 500rpm to 1450rpm at 0.8s. The T1FDTC of IM provides reduced amplitude of starting current of 8A with less peaks/dips in capacitor voltages and less flux distortion than PIDTC. The T1FDTC of IM settles at 0.16s and 1.12s during starting and step change in speed, respectively, and hence the steady state of the IM is quickly reached before 1-2 cycles as compared to PIDTC.

When the speed reversal is initiated at the same instants as that of PIDTC using T1FDTC then the corresponding waveforms (speed, currents, torque, flux, and line voltage) of the IM are shown in Fig. 4.11 (b). The TIFDTC of IM results in faster steady state characteristics at 2.38s and 3.89s during the speed reversal when compared to PIDTC, respectively. Moreover, TIFDTC of IM has less peaks/dips in capacitor voltages with less flux distortion than PIDTC. The same loads (4Nm, 8Nm, and 0Nm) of PIDTC

are also applied to T1FDTC of IM at the same instants (4.5s, 5s, and 5.5s) as shown in Fig. 4.12 (c). The no-load flux ripples, the torque distortion, and speed fluctuation at load perturbation are reduced to 0.05Wb, 0.7N-m, and 5rpm, respectively as compared to PIDTC. Also, T1FDTC provides faster dynamic response with less peaks/dips of the capacitor voltages than PIDTC during starting, step changes in speed, speed reversal, and load perturbation.

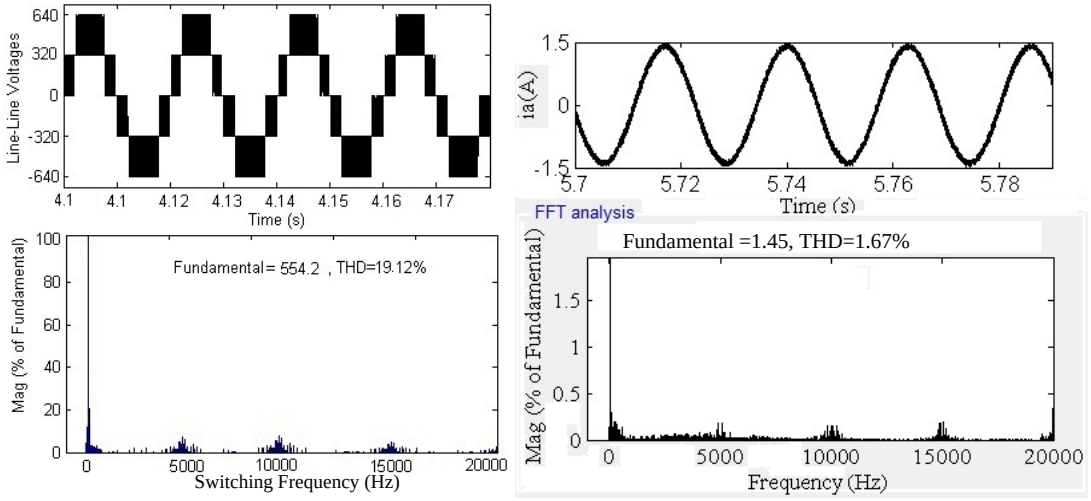
T2FDTC: The performance of the IM drive using T2FDTC is also simulated and corresponding waveforms are shown in Fig. 4.13 under the similar operating conditions of PIDTC. Fig. 4.13 (a) shows the performance of the IM during starting when the reference speed of 500rpm is applied and then a step change in the reference speed from 500rpm to 1450rpm at 0.8s. The T2FDTC of IM provides a less amplitude of starting current of 8A with less peaks/dips on capacitor voltages than PIDTC. It settles at 0.16s and 1.1s during starting and step change in the speed, respectively. Hence, the steady state of the IM is quickly reached before 0.08s with less peaks/dips on capacitor voltages than PIDTC during a step change in the speed.

The speed reversal is initiated at the same instants as that of PIDTC then; the corresponding waveforms (speed, currents, torque, flux, and line voltage) of the IM are shown in Fig. 4.13 (b). The T2FDTC of IM is quickly reached to the steady state at 2.34s and 3.85s during the speed reversal as compared to PIDTC, respectively. Moreover, the change in the capacitor voltages is less with T2FDTC control schemes during speed reversal as compared to PIDTC and T1FDTC. The same loads (4Nm, 8Nm, and 0Nm) as applied with PIDTC are also applied to T2FDTC of IM at the same instants (4.5s, 5s, and 5.5s) as shown in Fig. 4.13 (c). The no-load flux ripples, the torque distortion, and speed fluctuation at load perturbation are reduced to 0.045Wb, 0.45N-m, and 3rpm, respectively, which are significantly less than the PIDTC and T1FDTC. Also, T2FDTC provides faster dynamic response with less peaks/dips in the capacitor voltages than PIDTC during starting, step changes in speed, speed reversal, and load perturbation.



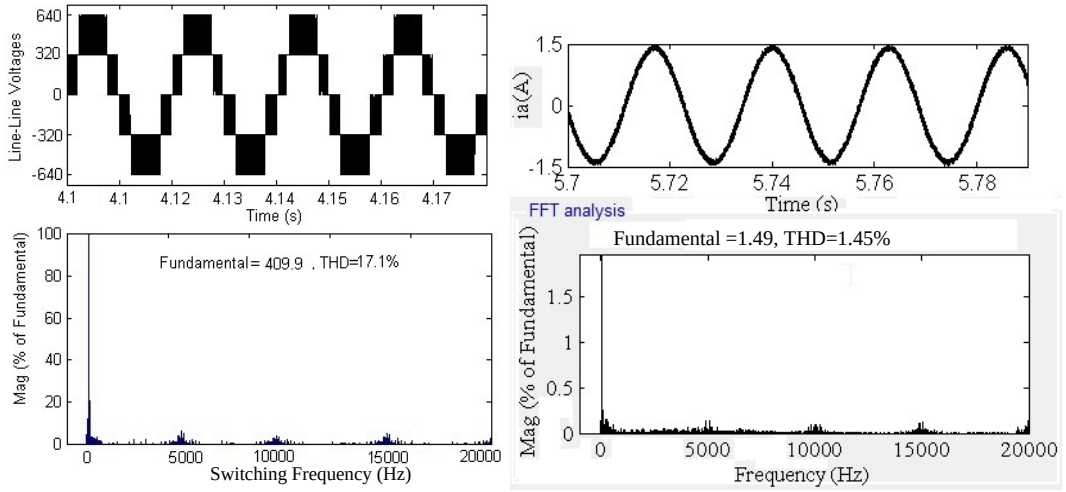
(a) Voltage THD (b) Current THD

Fig. 4.14: THD performance for the PIDTC of IM during No-load



(a) Voltage THD (b) Current THD

Fig. 4.15: THD performance for the T1FDTC of IM during No-load



(a) Voltage THD (b) Current THD

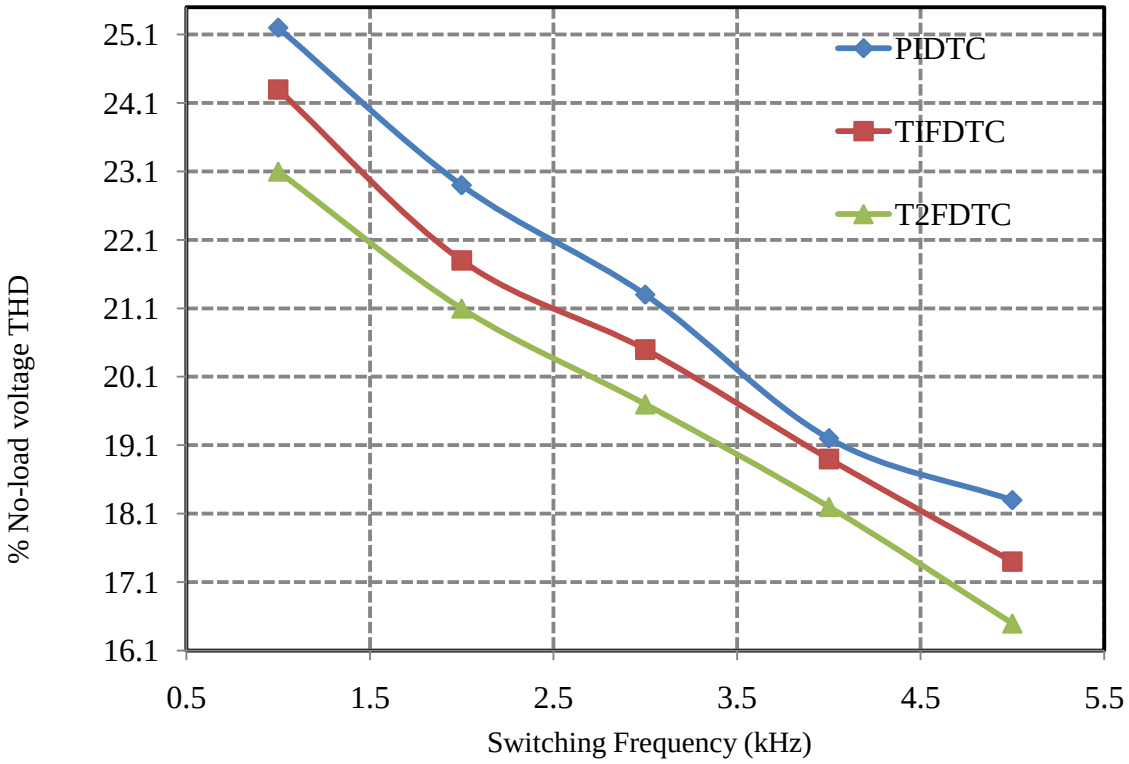
Fig. 4.16: THD performance for the T2FDTC of IM during No-load

Table 4.4: Simulated THD comparison for different control schemes

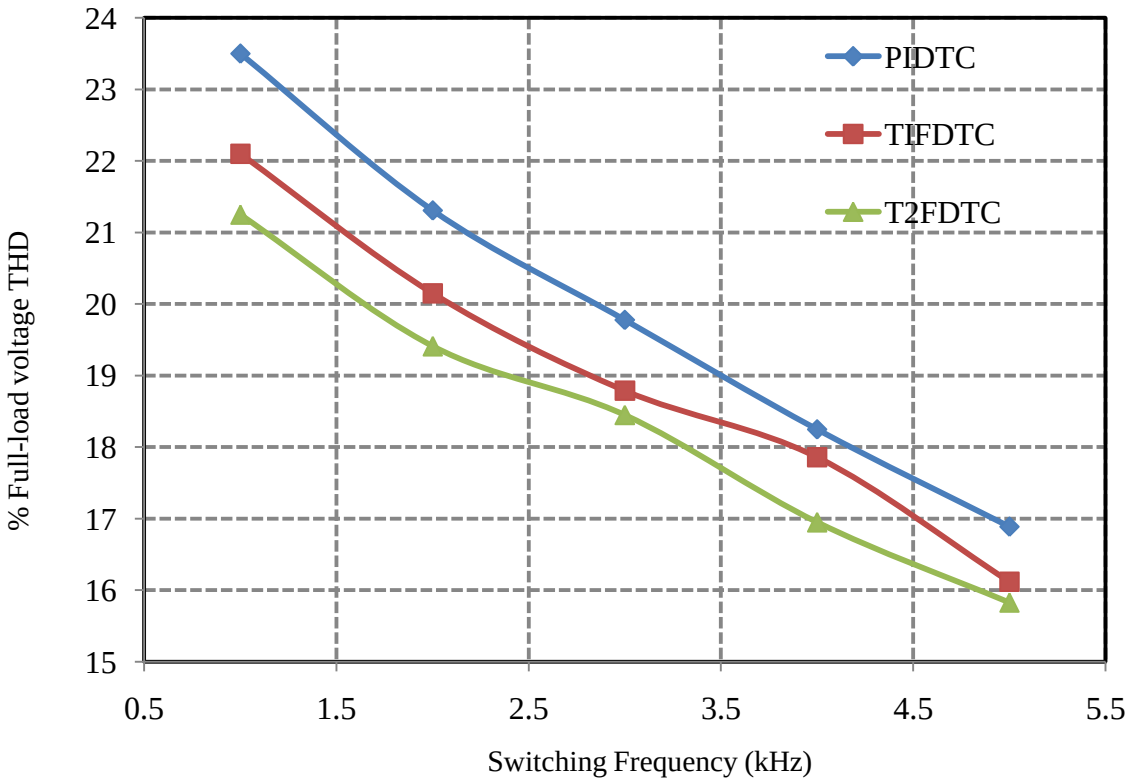
S.No.	f_{sw} (kHz)	$\%V_{THD}$			$\%i_{THD}$		
		PIDTC	**TIFDTC**	**T2FDTC**	**PIDTC**	**TIFDTC**	**T2FDTC**
No-Load							
1	1	25.2	24.3	23.1	4.15	3.95	3.81
2	2	22.9	21.8	21.1	3.75	3.65	3.48
3	3	21.3	20.5	19.7	3.45	3.25	3.1
4	4	19.2	18.9	18.2	3.12	2.92	2.85
5	5	18.3	17.4	16.5	2.55	2.45	2.21
Full-Load							
1	1	23.5	22.1	21.25	3.95	3.73	3.35
2	2	21.31	20.15	19.41	3.45	3.31	3.25
3	3	19.78	18.79	18.45	3.15	2.93	2.84
4	4	18.25	17.86	16.95	2.68	2.56	2.35
5	5	16.89	16.12	15.83	2.29	2.18	1.98

Table 4.5: Overall efficiency of alternative techniques during simulation

% Load	V_d**(V)**	$I_{inv}=I_d$**(A)**	P_{inv}**(W)**	ω_m**(rad/s)**	T_e**(N-m)**	P_m**(W)**	$\%\eta = 100*(P_{inv}/P_m)$
PIDTC							
25	640	1.5	**960**	152.8	2.18	**333.104**	34.69
50	640	1.8	**1152**	152.8	4.28	**653.984**	56.76
75	640	2.55	**1632**	152.8	7.19	**1098.63**	67.31
100	640	2.8	**1792**	152.8	8.9	**1359.92**	75.89
T1FDTC							
25	640	1.5	**960**	152.8	2.22	**339.216**	35.335
50	640	1.8	**1152**	152.8	4.34	**663.152**	57.56
75	640	2.55	**1632**	152.8	7.26	**1109.33**	67.97
100	640	2.8	**1792**	152.8	8.99	**1373.67**	76.65
T2FDTC							
25	640	1.5	**960**	152.8	2.28	**348.384**	36.29
50	640	1.8	**1152**	152.8	4.38	**669.264**	58.09
75	640	2.55	**1632**	152.8	7.31	**1116.97**	68.44
100	640	2.8	**1792**	152.8	9.1	**1390.48**	77.59

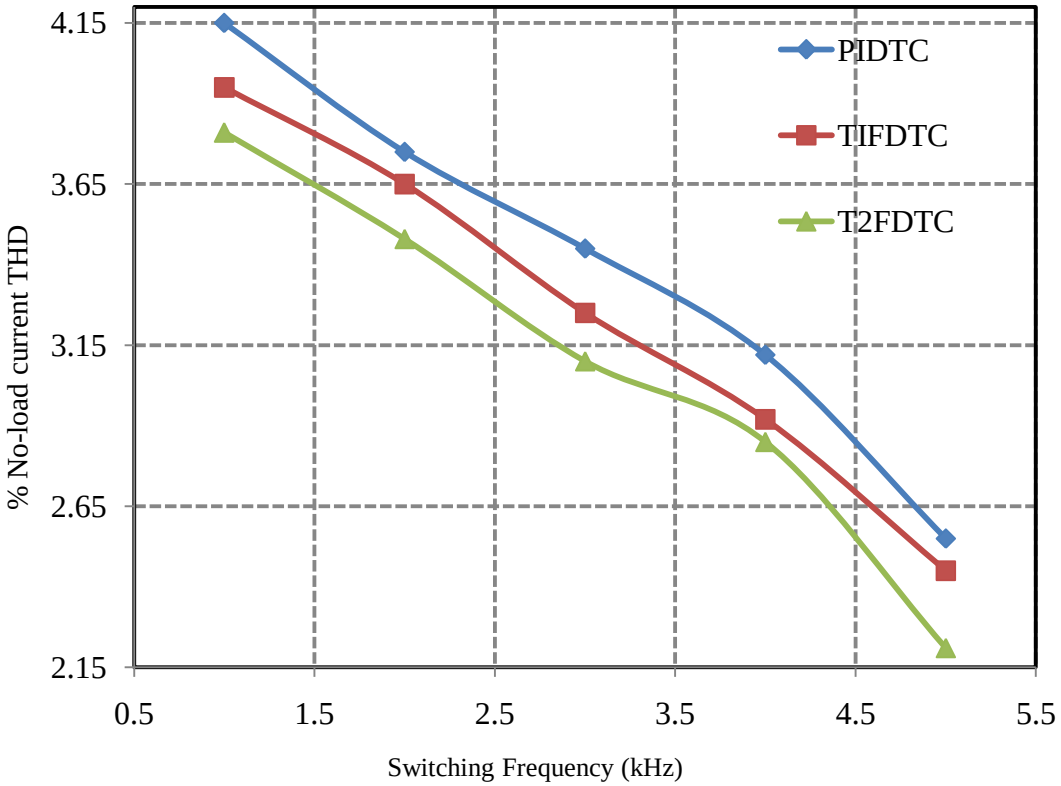


(a) No-load voltage THD vs. switching frequency

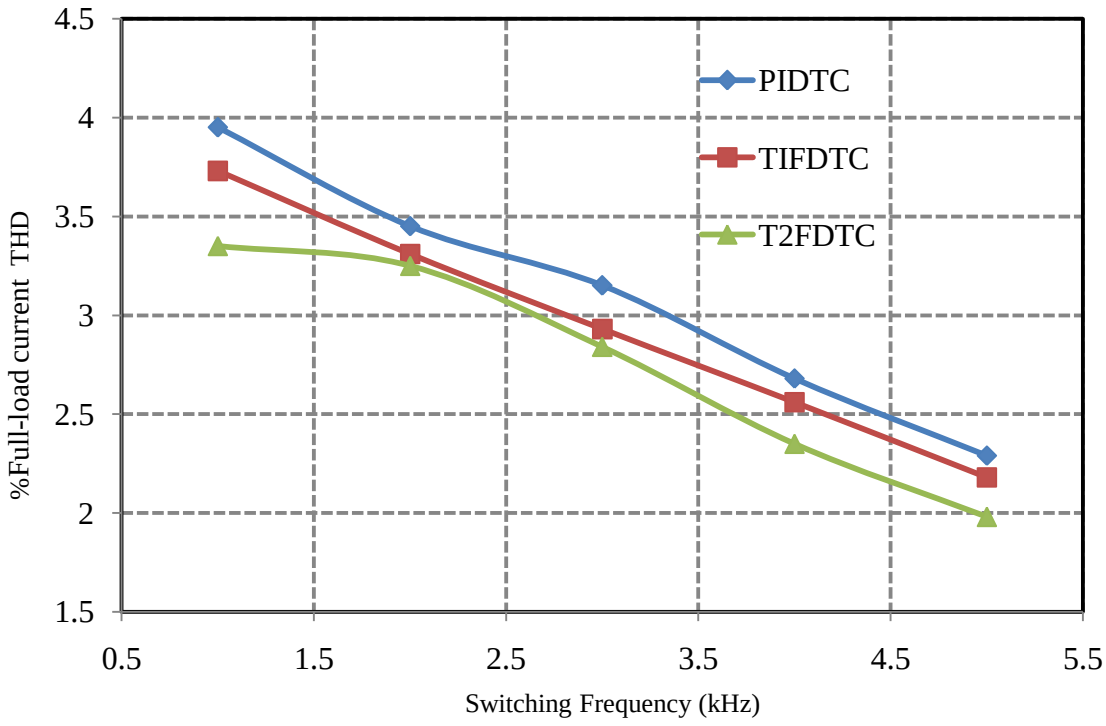


(b) Full-load voltage THD vs. switching frequency

Fig. 4.17: No-load and full-load line voltage THD performance of the IM drive



(a) No-load current THD vs. switching frequency



(b) Full-load current THD vs. switching frequency

Fig. 4.18: No-load and Full-load current THD of the IM drive for different control schemes

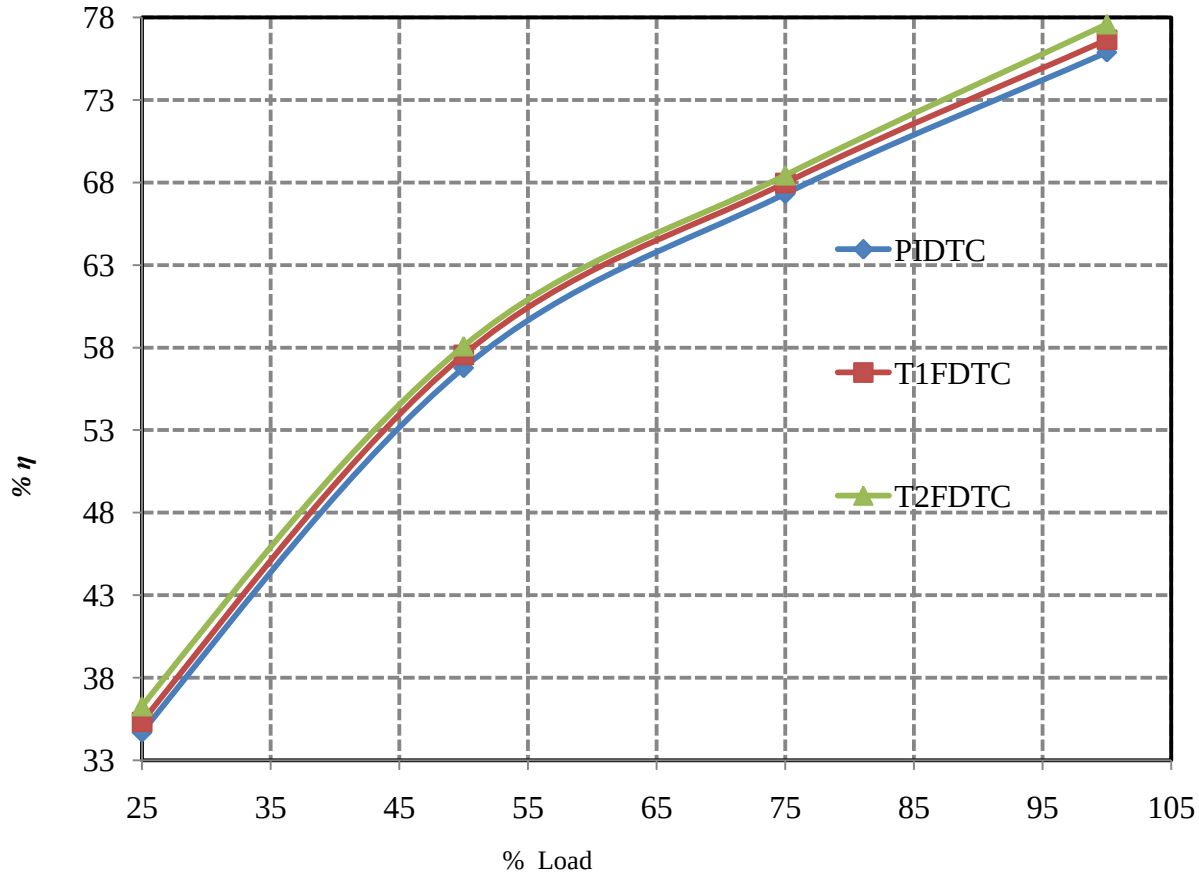


Fig. 4.19: Overall efficiency of three alternative techniques

Table 4.6: Prospectus of different control schemes of the IM drive

Measured parameters	**PIDTC**	**T1FDTC**	**Improvement of T1FDTC over PIDTC**	**T2FDTC**	**Improvement of T1FDTC over PIDTC**
$\pm\Psi_{dist}$ (Wb)	0.06	0.05	0.01	0.045	0.015
$\pm T_{dNL}$ (Nm)	0.7	0.6	0.1	0. 54	0.16
$\pm N_{cDL}$ (rpm)	10	4.5	5.5	3.5	6.5
$\%V_{NLTHD}$	21.19	19.12	2.07	17.1	4.09
$\%I_{NLTHD}$	2.2	1.67	0.53	1.45	0.75
$\%V_{FLTHD}$	16.89	16.12	0.77	15.83	1.06
$\%I_{FLTHD}$	2.29	2.18	0.11	1.98	0.31
$\%\eta_{FL}$	75.8	76.65	0.85	77.59	1.79
t_{st}(s)	0.16	0.15	0.07	0.15	0.07
t_{scs}(s)	1.18	1.12	0.06	1.1	0.08
t_{sr}(s)	2.6	2.38	0.22	2.34	0.26
t_{sr}(s)	4.1	3.89	0.21	3.85	0.25
t_{dl} (s)	0.15	0.1	0.05	0.08	0.07

Fig. 4.14 (a) and Fig.4.14 (b) show the percentage of line voltage and current THD for PIDTC of the IM during no-load operation and the corresponding values are 21.19 and 2.2, respectively. The percentage of line voltage and current THDs during no-load for T1FDTC has 19.12 and 1.67 as shown in Fig. 4.15 (a) and Fig. 4.15 (b), respectively. Fig. 4.16 (a) and Fig. 4.16 (b) give the percentage of line voltage and current THDs for T2FDTC of the IM during no-load operation and the corresponding values are 17.1 and 1.45, respectively. Therefore, it is observed from Fig. 4.14 to Fig. 4.16 that the T2FDTC has provided the least voltage and current THD, i.e., 17.1% and 1.45% than the other two control schemes (PIDTC and T1FDTC). This is due to the fact that the duty ratio are effectively controlled using T2FLC to improve the firing strength of the inverter than PIDTC and T1FDTC.Also the T2FLC effectively deals with the huge ambiguous data using type reducer and estimate the control variable as very close to the actual value.

Table 4.4 shows the simulated %THD comparison for both line voltage and current under no-load and full-load operaion by changing the switching frequency from 1kHz to 5kHz using different control schemes. Consequently, a comparative performance is studied and plotted for the corresponding line voltage THD during the no-load and full-load as shown in Fig. 4.17 (a) and Fig. 4.17 (b), respectively. Furthermore, the percentage of current THD vs. switching frequency is plotted for both no-load and full-load operation as shown in Fig. 4.18 (a) and Fig. 4.18 (b), respectively. From Fig. 4.17 and Fig. 4.18, it is observed that the T2FDTC provides less voltage and current THD value than PIDTC and T1FDTC. Moreover, the efficiency is calculated under different loading condition with a fixed switching frequency of 5kHz as given in Table 4.5.

A graph is plotted between the percentage of the efficiency and percentage of the load for PIDTC, T1FDTC and T2FDTC as shown in Fig. 4.19. Here, T2FDTC of the IM has more efficiency than T1FDTC and PIDTC. The reason is that the T2FDTC provides less harmonics/ripples of voltage, current, flux, torque and speed, which implies that the losses should also be reduced significantly and hence the efficiency of the IM drive is significantly improved as compared to T1FDTC and PIDTC. In addition, the percentage of full load efficiency of the IM using T2FDTC is 77.59, which is the highest value than the T1FDTC and PIDTC.

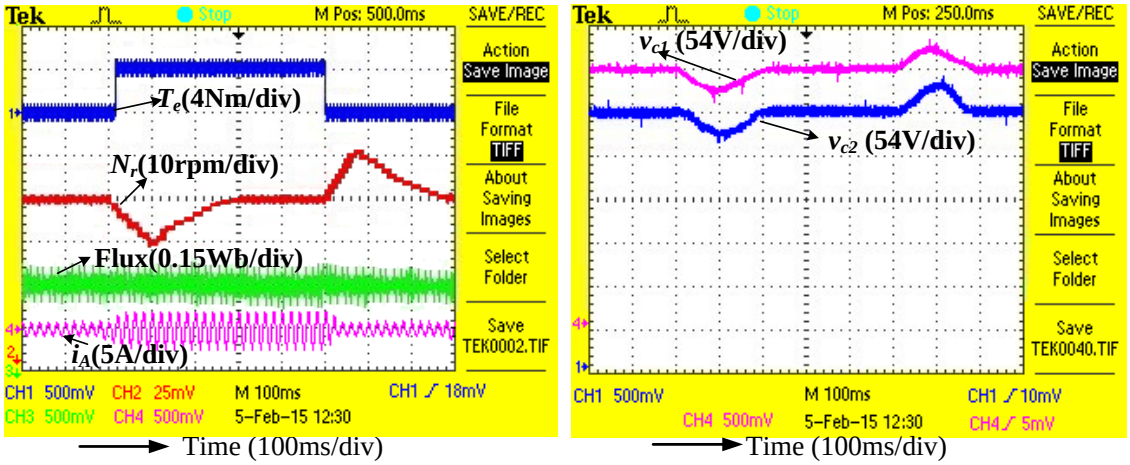
The comparative performance, such as starting, step change in speed, speed reversal, operation during the load, voltage and current THDs, flux and torque distortion, change in the speed during the load and efficiency at full load of the IM drive with the above

control schemes are mentioned in Table 4.6 in detail. Where, Ψ_{NLdst}, T_{NLdist}, Nc_{DL}, $\%V_{NLTHD}$, $\%I_{NLTHD}$,$\%V_{FLTHD}$, $\%I_{FLTHD}$,$\%\eta_{FL}$, t_{st}, t_{scs}, t_{sr}, and t_{dl} are the no-load torque distortion in N-m, change in speed during the load, percentage of no-load voltage THD, percentage of no-load current THD, percentage of full-load voltage THD, percentage of full-load current THD, percentage of full-load efficiency, settling time in sec during starting, settling time in sec during step change in speed, settling time in sec during the speed reversal, and settling time in sec during the load, respectively.

4.5.2 Experimental Results

The three-level PIDTC and F2DTC are also verified with the experimental setup using a DSPACE DS1104 controller. The operated switching frequency of the inverter and the sampling time (50µs), DC-link voltage, and parameters of the induction machine in real time applications remain same as the simulation with a dead band of 10µs for complementary switching devices and they are mentioned in Appendix A2.

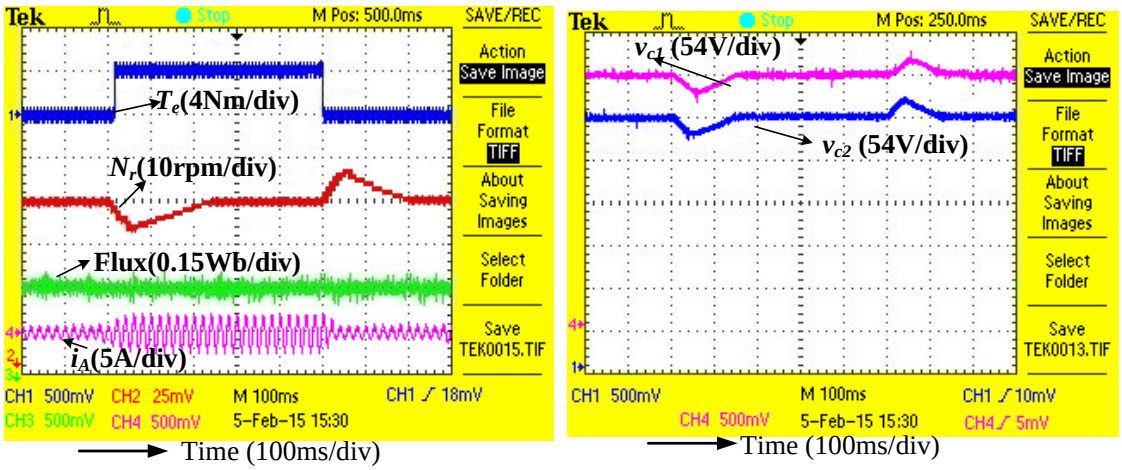
At starting, the reference speed 1450 rpm is initiated and controlling signals are generated through a DSPACE kit and set required DC-voltage (640V) by adjusting three-phase auto-transformer. After reaching the steady-state of the IM, the step load 4N-m applied and removed at 0.2s and 0.7s, respectively as shown in Fig. 4.20(a). Consequently, the electromagnetic torque (T_e) rises to 4N-m and falls down to 0N-m because of the load application. The IM decelerates and accelerates to 1440rpm and 1460rpm at the above mentioned instants and it settles at 0.5s and 1s, respectively. Moreover, the settling time and drop in speed of the IM are 0.3s and 10rpm during both decelerating and accelerating modes of the operation. Moreover, the current suddenly rises to 2.2A at 0.23s and again drops down to 1.5A at 0.73s due to increase and decrease in the load, respectively. However, the flux is maintained constant throughout the operation. The torque and flux distortion for PIDTC are ±0.75N-m and ±0.065Wb, respectively. The performance of DC-link capacitor voltages (v_{c1} and v_{c2}) for the PIDTC scheme during the load perturbation at the instants of 0.2s and 0.7s is shown in Fig. 4.20(b). The capacitor voltages settle at 0.4s and 0.9s after the load perturbation. The peaks and dips of capacitor voltages are varied approximately of ±30V. In addition, the settling time of the capacitors is approximately of 0.2s, whereas the IM speed takes approximately 0.3s to settle during the load and no-load operation.



(a) Torque, speed, flux, and current performance (b) DC-link voltages (v_{C1} and v_{C2}) across C_1 and C_2

Fig. 4.20: Performance of the PIDTC IM during the load perturbation at 0.2s and 0.7s

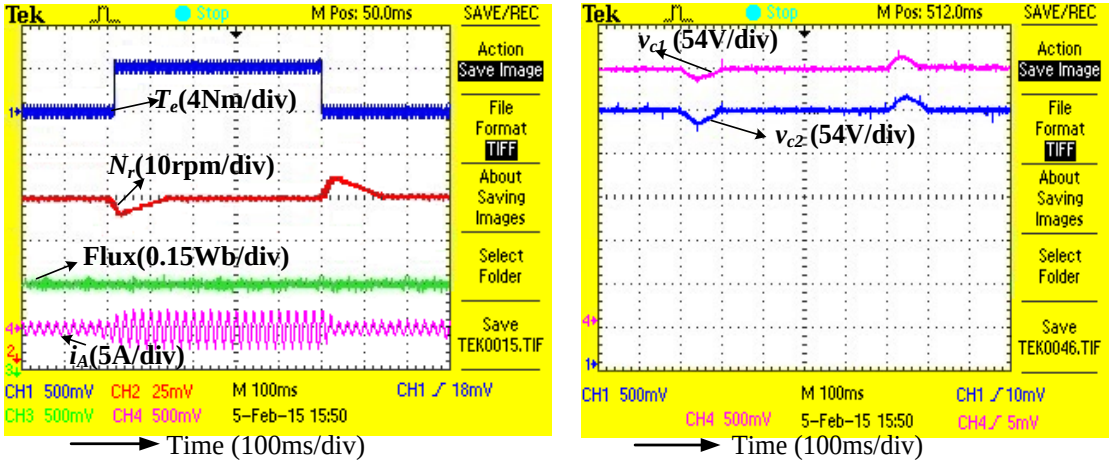
Similarly, the experimental performance for T1FDTC of the IM drive is also performed under the same operating modes. Fig. 4.21(a) shows a step change in the load (load perturbation) from 0N-m to 4N-m and 4N-m to 0N-m at 0.2s and 0.7s, respectively while running the IM at 1450rpm. The IM decelerates and accelerates to 1445rpm and 1455rpm settled to 1450rpm at 0.4s and 0.9s, respectively. Therefore, the fast dynamic performance of the IM using T1FDTC is obtained approximately by 0.1s at load perturbation than PIDTC. The no-load flux and torque distortions T1FDTC are ±0.05Wb and ±0.65N-m, whereas in PIDTC has ±0.065Wb and ±0.75N-m as shown in Fig. 4.20(a). Hence, the flux and torque distortions for T1FDTC have improved by 23.07% and 13.3% than that of PIDTC. In addition, the change in speed during the load perturbation for T1FDTC of IM is 5rpm only, which is reduced to half of the PIDTC of IM drive.



(a) Torque, speed, flux, and current performance (b) DC-link voltages (v_{C1} and v_{C2}) across C_1 and C_2

Fig. 4.21: Performance of the T1FDTC IM during the load perturbation at 0.2s and 0.7s

Fig. 4.21(b) shows the performance of DC-link capacitor voltages (v_{c1} and v_{c2}) for the T1FDTC scheme during the load perturbation at the instants of 0.2s and 0.7s. The capacitor voltages settle approximately at 0.34s and 0.74s after the load perturbation. The peaks and dips of capacitor voltages vary approximately by ±21V. In addition, the settling time of the capacitors for T1FDTC is approximately of 0.14s, whereas the PIDTC takes approximately 0.2s to settle during the load and no-load operation. Therefore, in T1FDTC the settling time of the capacitor voltages is faster by 0.08s with fewer peaks and swells in the capacitor voltages than PIDTC.

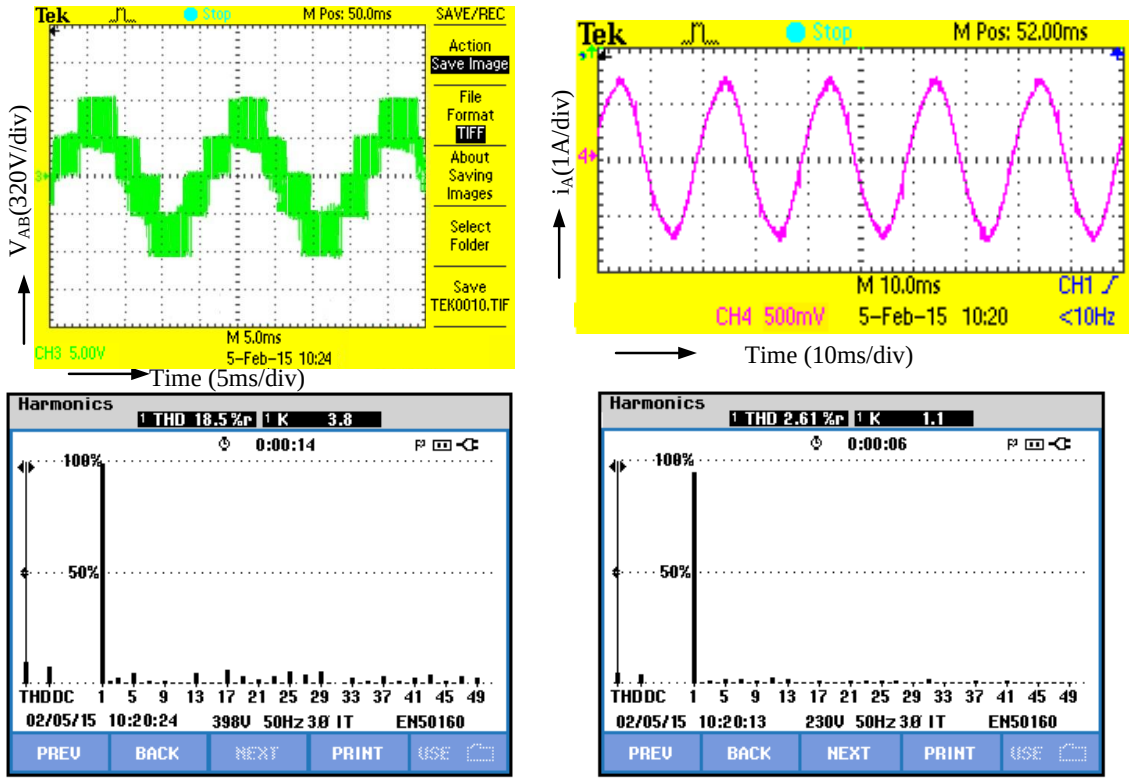


(a) Torque, speed, flux, and current performance (b) DC-link voltages (v_{C1} and v_{C2}) across C_1 and C_2

Fig. 4.22: Performance of the T2FDTC IM during the load perturbation at 0.2s and 0.7s

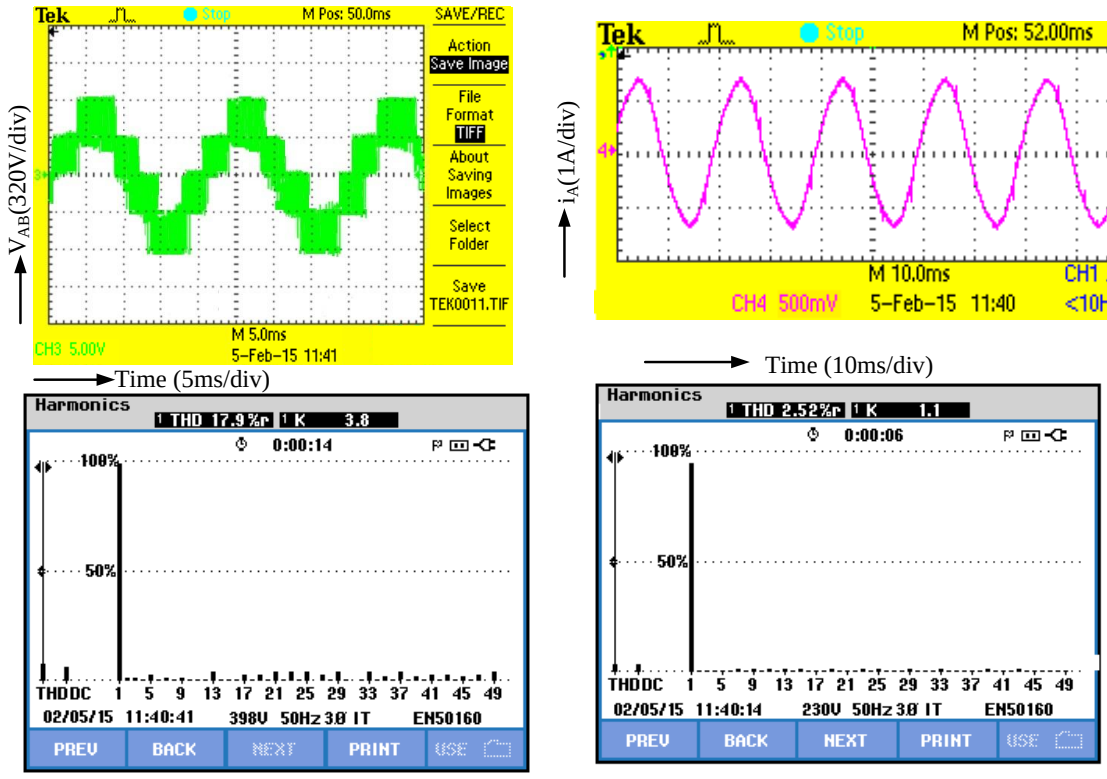
Similarly, the experimental performance for T2FDTC of the IM drive is also executed under the same operating mode. Fig. 4.22(a) shows a step change in the load (load perturbation) from 0N-m to 4N-m and 4N-m to 0N-m at 0.2s and 0.7s, respectively while running the IM at 1450rpm. Consequently, the IM develops a high torque of 4N-m with large current for getting the required speed of 1450rpm and is settled to 1450rpm at 0.34s during the application of the load, whereas PIDTC settled at 0.5s as shown in Fig. 4.20(a). Therefore, the speed of the IM with T2FDTC quickly settles by a margin of 0.16s than PIDTC. The IM speed accelerates from 1450rpm to 1455rpm and settles to 1450rpm at 0.84s during the load removal at 0.7s. Hence, the IM speed for T2FDTC settles again faster within 0.16s during the load removal case also. In addition, the flux and torque distortion at no load are obtained as ±0.04Wb and ±0.5N-m, respectively as shown in Fig. 4.22(a).Whereas the flux and torque distortion in PIDTC are ±0.065Wb and ±0.75N-m, respectively as shown in Fig. 4.20(a). The percentage of improvement in the flux and

torque distortions using T2FDTC is 38.4% and 33.3% over PIDTC. Also, the change in speed for T2FDTC of IM is 4rpm only, which is very less as compared to PIDTC.



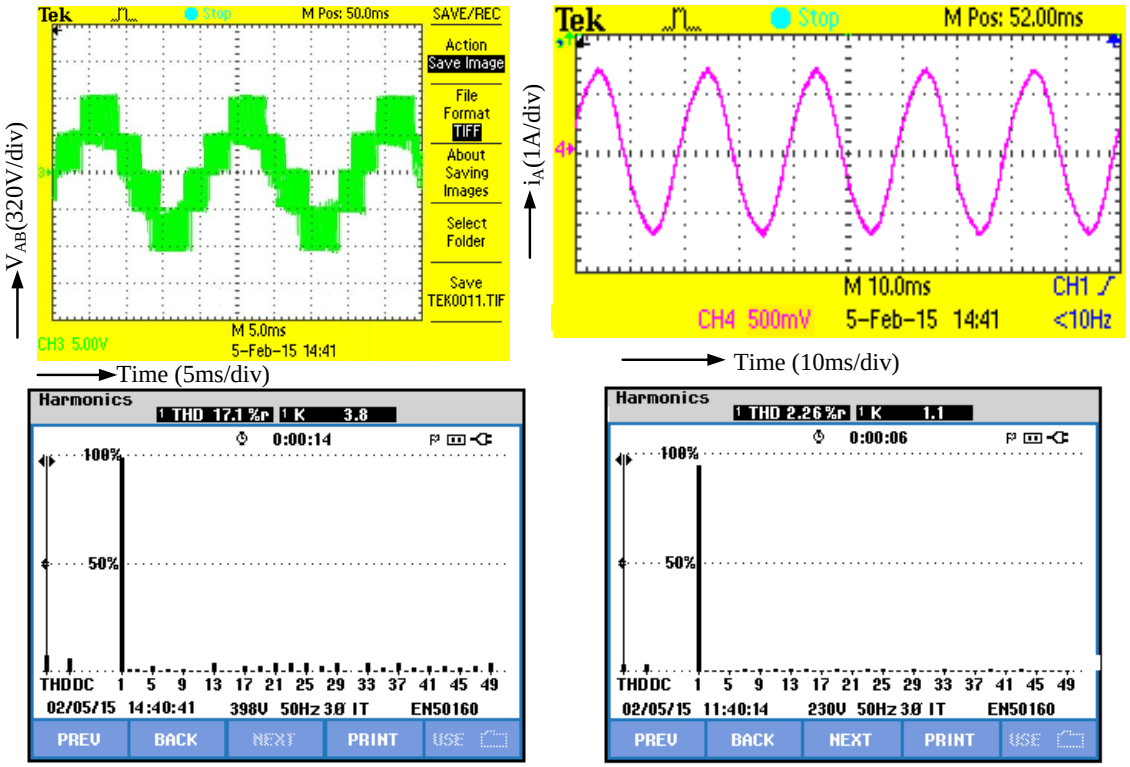
(a) Voltage THD (b) Current THD

Fig. 4.23: THD performance for the PIDTC of IM during No-load



(a) Voltage THD (b) Current THD

Fig. 4.24: THD performance for the T1FDTC of IM during No-load

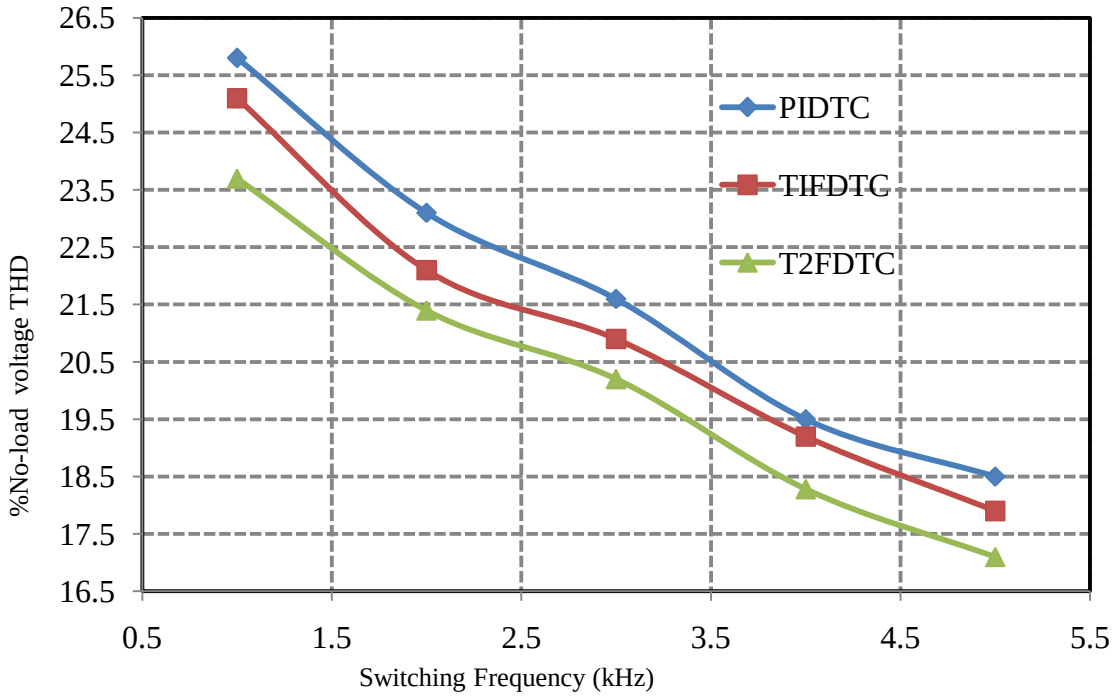


(a) Voltage THD (b) Current THD

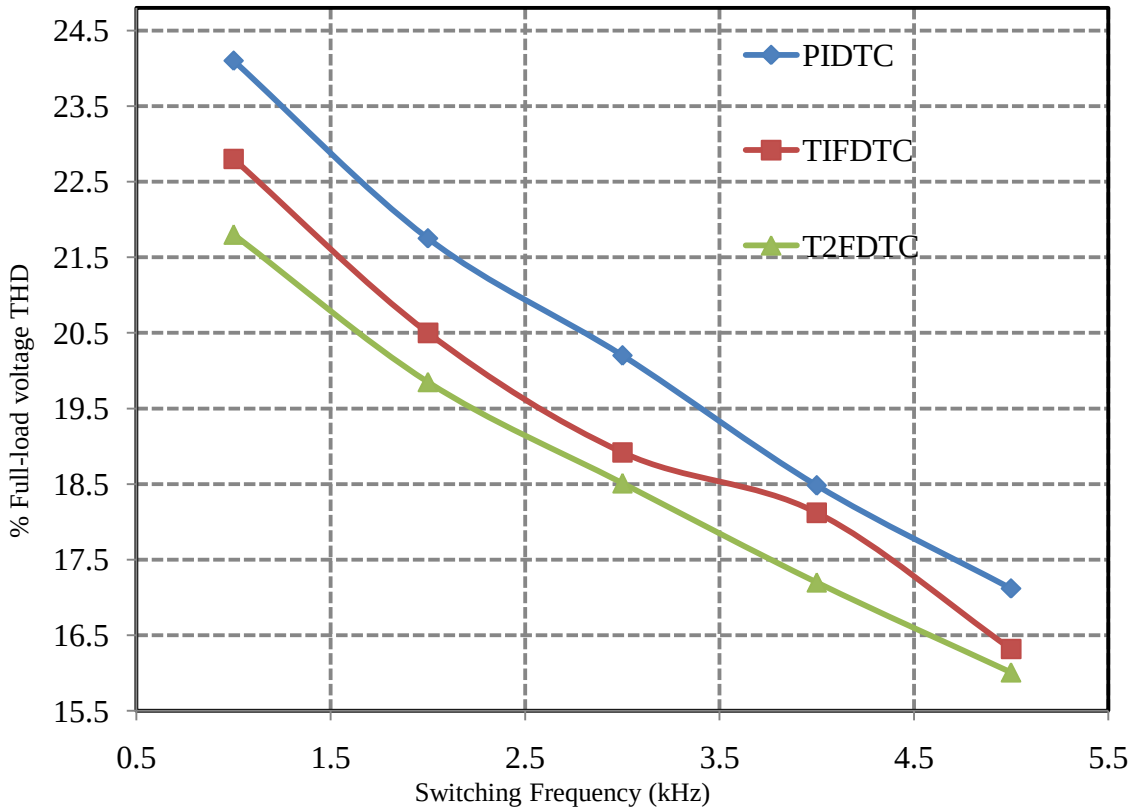
Fig. 4.25: THD performance for the T2FDTC of IM during No-load

Table 4.7: Exprimental THD comparison for different control schemes

S.No.	f_{sw} (kHz)	$\%V_{THD}$			$\%i_{THD}$		
		PIDTC	TIFDTC	T2FDTC	PIDTC	T1FDTC	T2FDTC
No-Load							
1	1	25.8	25.1	23.7	4.2	3.98	3.91
2	2	23.1	22.1	21.4	3.92	3.71	3.5
3	3	21.6	20.9	20.2	3.49	3.21	3.12
4	4	19.5	19.2	18.28	3.15	2.95	2.89
5	5	18.5	17.9	17.1	2.61	2.52	2.26
Full-Load							
1	1	24.1	22.8	21.8	4.1	3.79	3.41
2	2	21.75	20.5	19.85	3.49	3.4	3.25
3	3	20.2	18.92	18.51	3.19	3.02	2.85
4	4	18.48	18.12	17.2	2.72	2.6	2.38
5	5	17.12	16.32	16.01	2.3	2.19	1.99

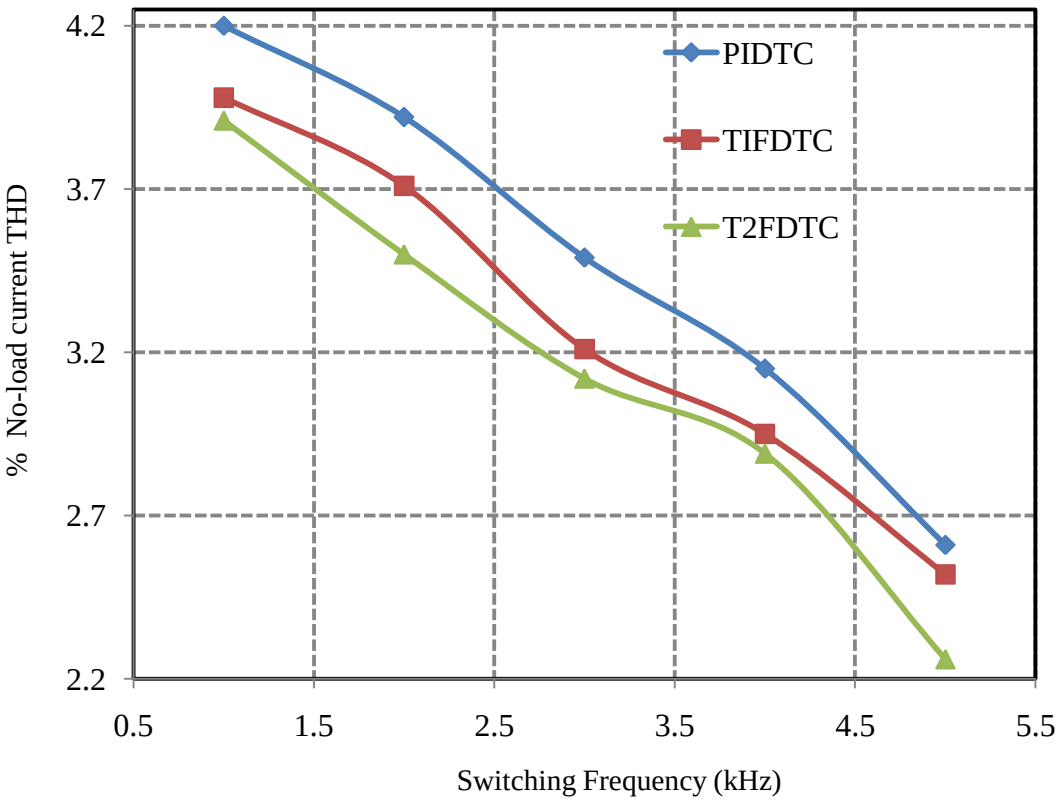


(a) No-load voltage THD vs. switching frequency

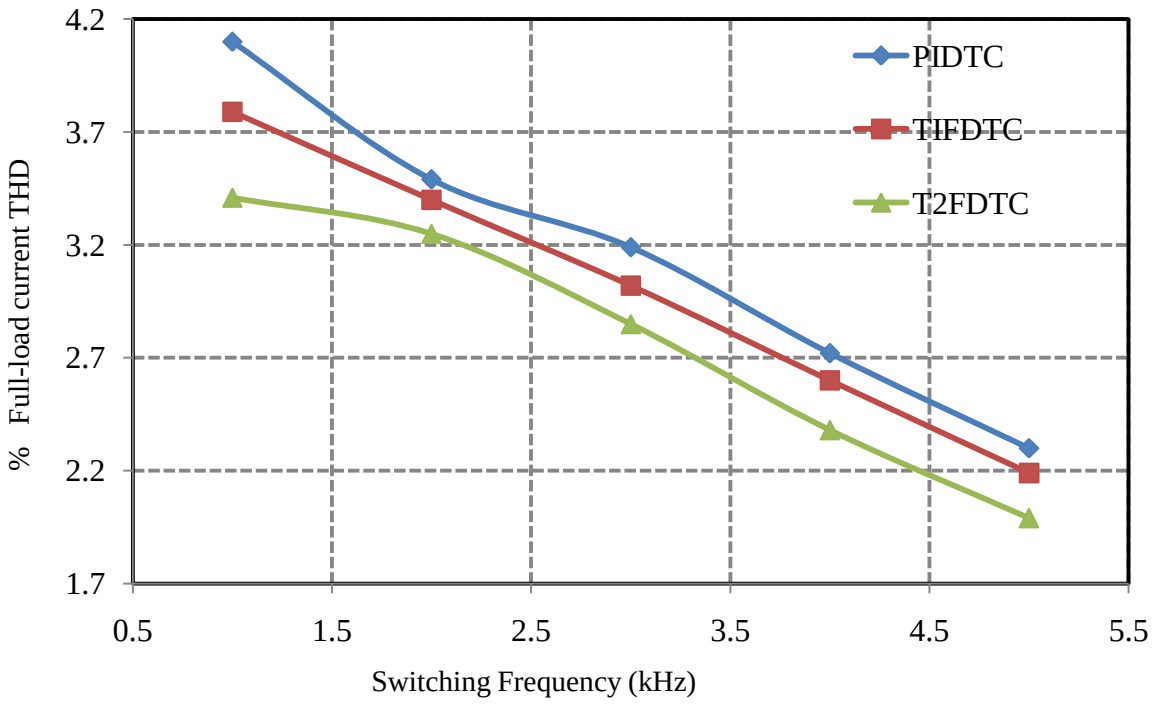


(b) Full-load voltage THD vs. switching frequency

Fig. 4.26: No-load and full-load voltage THD of the IM drive for different control schemes



(a) No-load Current THD vs. switching frequency for different control schemes



(b) Full-load current THD vs. switching frequency

Fig. 4.27: Current THD performance of the IM drive for different control schemes

Table 4.8: Overall efficiency of alternative techniques

% Load	V_d(V)	I_{inv}=I_d(A)	P_{inv}(W)	ω_m(rad/s)	T_e(N-m)	P_m(W)	$\%\eta = 100*(P_{inv}/P_m)$
PIDTC							
25	640	1.5	**960**	152.8	2.14	**326.992**	34.06
50	640	1.8	**1152**	152.8	4.22	**644.816**	55.97
75	640	2.55	**1632**	152.8	7.12	**1087.94**	66.66
100	640	2.8	**1792**	152.8	8.79	**1343.11**	74.95
T1FDTC							
25	640	1.5	**960**	152.8	2.19	**334.632**	34.86
50	640	1.8	**1152**	152.8	4.299	**656.887**	57.02
75	640	2.55	**1632**	152.8	7.21	**1101.69**	67.50
100	640	2.8	**1792**	152.8	8.89	**1358.39**	75.20
T2FDTC							
25	640	1.5	**960**	152.8	2.21	**337.688**	35.18
50	640	1.8	**1152**	152.8	4.31	**658.568**	57.16
75	640	2.55	**1632**	152.8	7.27	**1110.86**	68.07
100	640	2.8	**1792**	152.8	8.87	**1355.34**	75.65

Table 4.9: Prospectus of T2FDTC, T1FDTC and PIDTC of IM drive

Measured parameters	**PIDTC**	**T1FDTC**	**T1FDTC improvement over PIDTC**	**T2FDTC**	**T1FDTC improvement over PIDTC**
$\pm\Psi_{dist}$ (Wb)	0.065	0.05	**0.005**	0.04	**0.025**
$\pm T_{dNL}$ (Nm)	0.75	0.65	**0.15**	0. 5	**0.25**
$\pm N_{cDL}$ (rpm)	10	5	**5**	4	**6**
$\%V_{NLTHD}$	18.5	17.9	**0.6**	17.1	**1.4**
$\%I_{NLTHD}$	2.61	2.52	**0.08**	2.26	**0.35**
$\%V_{FLTHD}$	17.12	16.32	**0.8**	16.01	**1.11**
$\%I_{FLTHD}$	2.3	2.19	**0.11**	1.99	**0.31**
$\%\eta_{FL}$	74.9	75.2	**0.3**	75.65	**0.7**
t_C (s)	0.2	0.14	**0.06**	0.1	**0.1**
t_{dl} (s)	0.3	0.2	**0.1**	0.16	**0.14**
v_{cd}(V)	±30	±21	**±9**	±15	**±15**

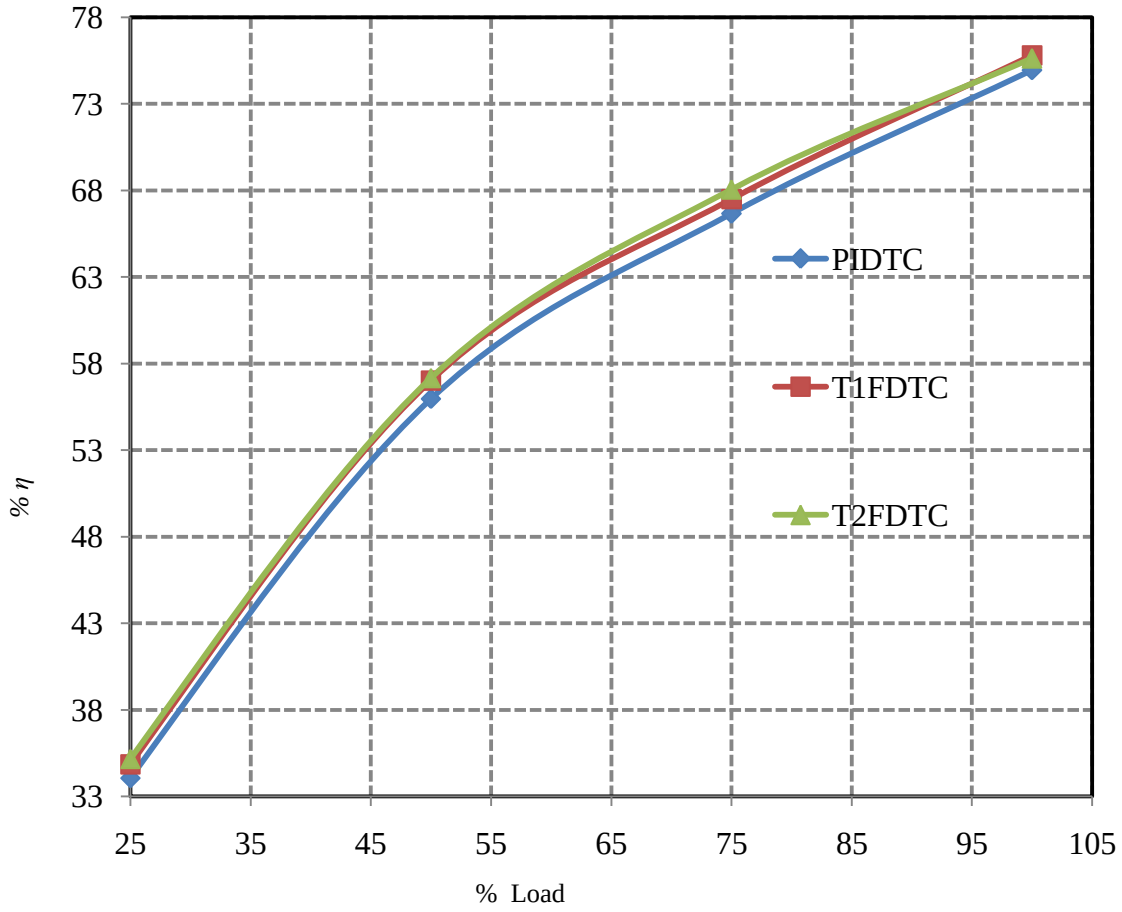


Fig. 4.28: Efficiensy vs. load for PIDTC, T1FDTC and T2FDTC

Fig. 4.22(b) shows the performance of DC-link capacitor voltages (v_{c1} and v_{c2}) for the T2FDTC scheme during the load perturbation at the instants of 0.2s and 0.7s. The capacitor voltages settle approximately at 0.3s and 0.7s after the load perturbation. The peaks and dips of capacitor voltages vary approximately by ±15V. In addition, the settling time of the capacitors for T1FDTC during both on-load and no-load is approximately of 0.1s, whereas the PIDTC takes approximately 0.2s to settle during the load and no-load operation. Therefore, the settling time of the capacitor voltages is faster by 0.1s with fewer peaks and swells in the capacitor voltages than PIDTC.

Fig. 4.23 (a) and Fig. 4.23 (b) show the percentage of line voltage and current THD for TLDCI using PIDTC of the IM during no-load operation and the corresponding values are 18.5 and 2.61, respectively. The percentage of line voltage and current THDs during no-load for T1FDTC has 17.9 and 2.52 as shown in Fig. 4.24 (a) and Fig. 4.24 (b), respectively. Fig. 4.25 (a) and Fig.4.25 (b) give the percentage of line voltage and current THDs for T2FDTC of the IM during no-load operation and the corresponding values are 17.1 and 2.26, respectively. Therefore, it is observed from Fig. 4.23 to Fig. 4.25 that the

T2FDTC has provided the least voltage and current THDs of 17.1% and 2.25% when compared to other two control schemes (PIDTC and T1FDTC).

Table 4.7 shows the experimental %THD comparison for both line voltage and current under no-load and full-load operation by changing the switching frequency from 1kHz to 5kHz using different control schemes. Consequenty, a comparative performance is studied and plotted for the corresponding line voltage THD during the no-load and full-load as shown in Fig. 4.26 (a) and Fig. 4.26 (b), respectively. Furthermore, the percentage of current THD vs. switching frequency is plotted for both no-load and full-load operation as shown in Fig. 4.27 (a) and Fig. 4.27 (b), respectively. From Fig. 4.26 and Fig. 4.27, it is observed that the T2FDTC provided less voltage and current THD value than PIDTC, and T1FDTC. Moreover, the efficiency is also calculated under different loading conditions with a fixed switching frequency of 5kHz as given in Table 4.8. A graph is plotted between the percentage of the efficiency and percentage of the load for PIDTC, T1FDTC and T2FDTC as shown in Fig. 4.28. Here, T2FDTC of the IM drive for TLDCI provides more efficiency than T1FDTC and PIDTC at any of the load condtions. The reason is that the T2FDTC provides less harmonics/ripples of voltage, current, and torque, which implies the losses should be less and hence the efficiency of the IM drive significantly improved as compared to T1FDTC and PIDTC. In addition, the percentage of full load efficiency of the IM using T2FDTC is 75.63, which is the highest value among the two control schemes as mentioned above. The percentage of improvement of flux distortion, torque distortion, voltage THD, and current THD for T2FDTC of the IM drive during the no-load is 38.4, 33.33, 18.2, and 20.34 when compared to PIDTC. The comparative performance for TLDCI using T2FDTC, T1FDTC, and PIDTC, such as starting, step change in speed, speed reversal, IM operation during the load, voltage and current THDs, flux and torque distortion, change in the speed during the load and efficiency at full load of the IM drive with the above control schemes are mentioned in Table 4.9 in detail. Where, Ψ_{NLdst}, T_{NLdist},Nc_{DL}, $\%V_{NLTHD}$, $\%I_{NLTHD}$,$\%V_{FLTHD}$, $\%I_{FLTHD}$,$\%\eta_{FL}$, t_C, t_{DL},and$v_{cd}$are the no-load torque distortion (N-m), change in speed during the load (rpm), percentage of no-load voltage THD, percentage of no-load current THD, percentage of full-load voltage THD, percentage of full-load current THD, percentage of full-load efficiency, settling time (s) during starting, settling time (s) for the capacitors, speed settling time (s) during the load and voltage drop across the capacitors, respectively.

4.6 Conclusion

A three-level inverter fed direct torque controlled IM drive is simulated in the Matlab environment for TLDCI using PIDTC, T1FDTC and T2FDTC. In addition, the voltages across the DC-link capacitors provide constant by operating or selecting an appropriate switching vector in all three control schemes without need of any extra controllers. The PIDTC provides considerable flux and torque ripples. Moreover, it has poor dynamic performance of the IM. In order to improve the dynamic performance of IM drive, the T1FDTC and the T2FDTC are proposed. In both T1FDTC and T2FDTC, the torque and speed PI-controllers are replaced by type-1 or type-2 fuzzy controllers (T2FCs) to get quick dynamic performance of the IM drive than PIDTC, because the T2FC has three-dimensional control with type reduction in defuzzification process to effectively deal with the huge ambiguous data (larger footprint of data) than T1FC. Moreover, Mamdani type and Centroid method with simple IF and THEN rules are used in both control schemes (T1FDTC and T2FDTC). The duty ratio control with T1FLC and T2FLC of SVM improves the firing strength of the inverter. Consequently, the current and torque ripples of IM drive can be improved significantly than PIDTC. A comparative simulated performance of the IM drive during startup, the step change in speed, and load perturbation is presented. The T2FDTC provides significant improvement in the overall efficiency with less voltage and current THD of the IM drive than T1FDTC and PIDTC. In addition, the dynamic response of the IM drive using T2FDTC is improved significantly at any mode of operation. A prototype controller is developed in the laboratory and the control signals for PIDTC, T1FDTC and T2FDTC are generated by the DSPACE DS-1104 controller. In addition, the simulated results of the above control schemes are validated with the experimental results under the various operating conditions. It is concluded that the T2FDTC provides fewer flux ripples, less torque distortion, less voltage and current THD, and more overall efficiency of the IM drive with fast dynamic performance T1FDTC and PIDTC. The percentage of improvement of flux distortion, torque distortion, voltage THD, and current THD for T2FDTC of the IM drive during the no-load is 38.4, 33.33, 18.2, and 20.34 when compared to PIDTC. Moreover, the full-load efficiency of the IM drive for T2FDTC is 75.65%, which is higher value over a conventional PIDTC and T1FDCT.

CHAPTER -5

DIRECT TORQUE CONTROL FOR FIVE-LEVEL DIODE CLAMPED INVERTER FED IM DRIVE

5.1 Introduction

A five-level diode clamped inverter (FLDCI) is used instead of a three-level diode clamped inverter for further improvement in the IM drive performance like reduced ripples in voltage, current, torque, and flux. The conventional DTC along with FLDCI reduces the torque and flux distortion of the IM than the two-level and three-level inverter [169, 195-196]. The type-1 fuzzy DTC along with FLDCI improves the dynamic performance of the IM than conventional DTC as the flux and torque controllers are replaced by type-1 fuzzy logic control [195]. In Chapter-4, the simulated performance of three-level inverter fed IM drive with PIDTC, T1FDTC and T2FDTC were presented and the performance of T2FDTC was validated with the experimental setup to improve the performance of the IM than PIDTC and T1FDTC. However, there is a still a scope to improve the performance of the IM drive with the similar controllers as used in the Chapter-3 and 4. In the present Chapter, a FLDCI fed IM drive is presented to further improve the ripple performance in voltage, current, flux, torque, and speed than two and three level inverter using the same control schemes. The above control schemes have been simulated and implemented in the laboratory on a 2HP IM through dSPACE DS-1104 controller. In all three control schemes, the voltage across the DC-link capacitors for FLDCI is balanced based on minimum energy property. However, the PIDTC along with FLDCI of the IM provides poor transient performance during startup, step change in the speed, speed reversal, and step load with considerable current and voltage THD. In addition, it takes more time to reach the steady state with large spikes on capacitor voltages during load or speed variation, which is due to poor performance of the PI-controllers (speed and torque). To improve the IM drive performance, the type-1 fuzzy logic control is used instead of PI-controllers (speed and torque) and as it controls the duty ratios independent of the sampling to improve the firing strength of the inverter. The type-1 fuzzy direct torque control (T1FDTC) provides considerable reduction in flux and torque distortion, and less voltage and current THD with improved dynamic response of

the IM drive. To further improve the dynamic response with less voltage and current THD of the IM drive, the T2FDTC is used in which T1FLC is replaced by T2FLC. The T2FLC effectively deals with the large FOU with five-dimensional control and reduced type-2 fuzzy set to improve the performance of the controller. The simulated and the experimental performance show that the F2DTC for the FLDCI fed IM drive provides the fast dynamic response, less current and voltage THDs, minimized distortion in flux and torque, and fewer spikes on capacitor voltages with improved overall efficiency than PIDTC and T1FDTC.

5.2 Proportional Integral Direct Torque Control

The block diagram for the PIDTC along with FLDCI for both simulation and real time implementation using SVPWM technique is shown by thick lines in Fig. 5.1 in which the rotor speed of the IM is estimated from Tacho-generator (TG) along with a voltage sensor through ADC channels on the dSPACE controller. Similarly, the DC-link voltages across the four capacitors (v_{C1}, v_{C2}, v_{C3}, and v_{C4}), three phase currents (i_{abc}), and voltages (v_{abc}) are sensed from voltage and current sensors and fed back through the ADC channels of the dSPACE controller. The stator flux and electromagnetic torque of the IM are estimated from the three phase voltages and currents using the formulae that are explained in Chapter-3. However, these three phase voltages and currents are estimated from the single voltage and current sensors using a phased locked loop control (PLLC), which converts the per phase voltage to three phase voltages by providing the transport delay as used in the experiment.

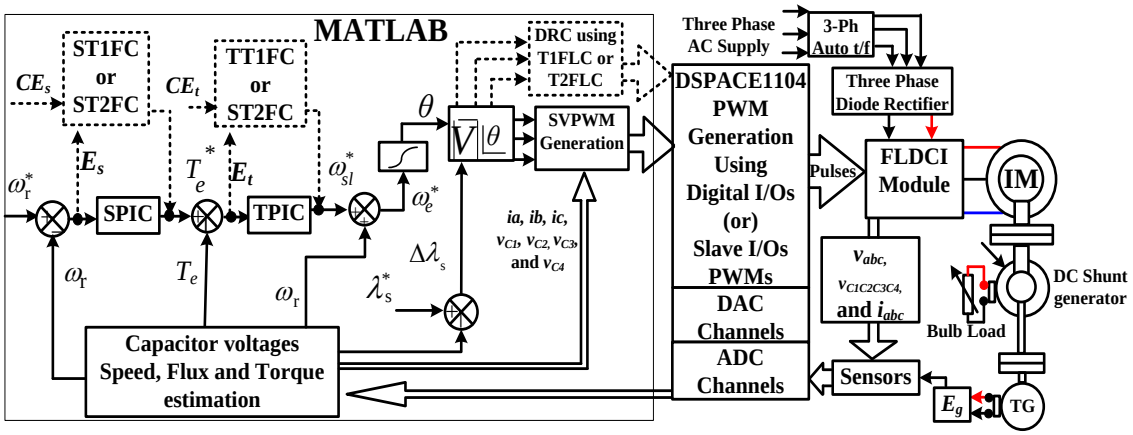


Fig. 5.1: Block diagram for PIDTC (shown by thick-line) / T1FDTC (shown by dotted lines) / T2FDTC (shown by dotted line) of IM using FLDCI

Moreover, the IM speed is estimated with the help of a DC-Tacho-generator and a voltage sensor and fed back by ADC channels of the dSPACE controller. After estimating

the speed, flux, and torque of the IM and comparing with the reference values, the error is given to the respective PI-controllers. Consequently, the reference vector and angle are estimated like PIDTC of the IM for two-level inverter, which is already described in the Chapter-3. Here, PI-controllers are tuned using Ziegler–Nichols method [11]. However, the best values of k_p and k_i are chosen for PI-controllers to get the overall better dynamic performance of the IM drive for a wide range of speed/torque control.

5.2.1 SVM for Five-level Diode Clamped Inverter

The SVM for FLDCI is easily developed after finding the reference vector and angle. The procedure to generate a reference vector and angle was explained in chapter-3 in detail. A 3-phase FLDCI is shown in Fig. 5.2 in which the pole nodes p, n, o, –n and -p, indicate the different positions of the DC-link capacitors. The pole voltages ($V_{Ao}/V_{Bo}/V_{Co}$) and line voltages ($V_{AB}/V_{BC}/V_{CA}$) for the corresponding switching states are given in Table 5.1, where 1 and 0 indicate the on and off state of the corresponding switching devices, respectively [169, 191-195].

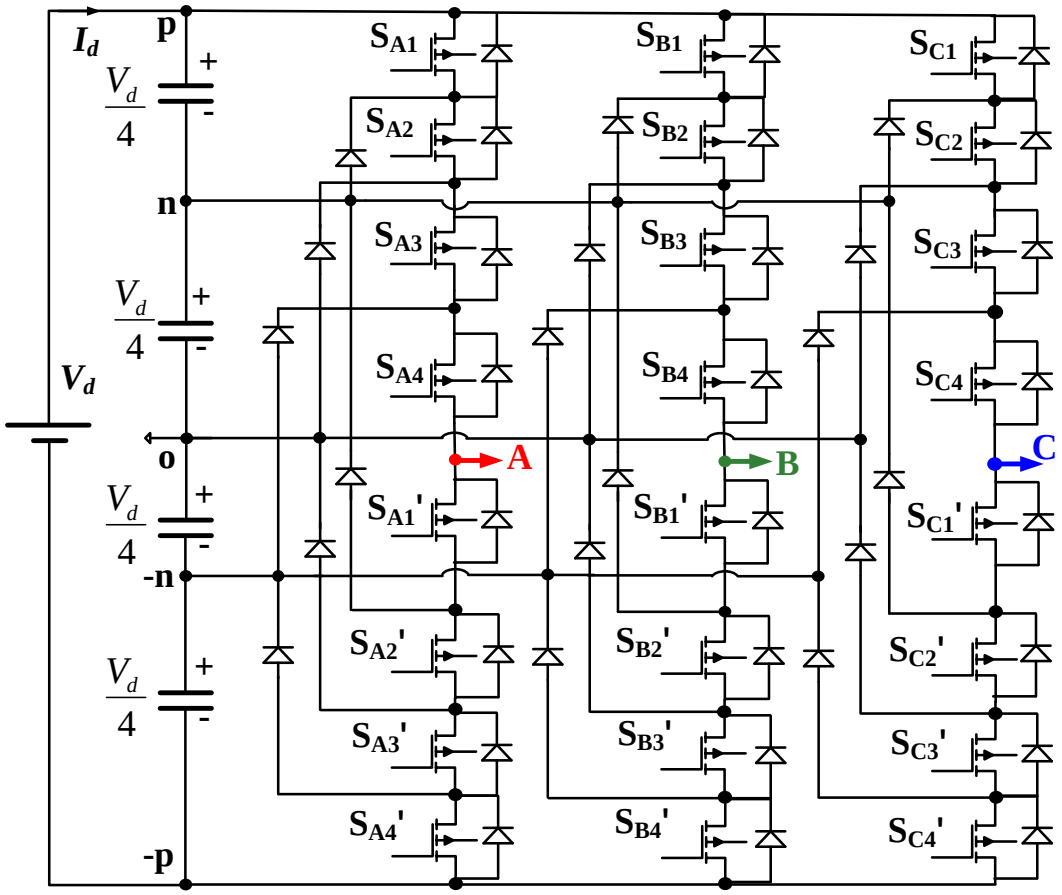


Fig. 5.2: Five-level diode clamped voltage source inverter

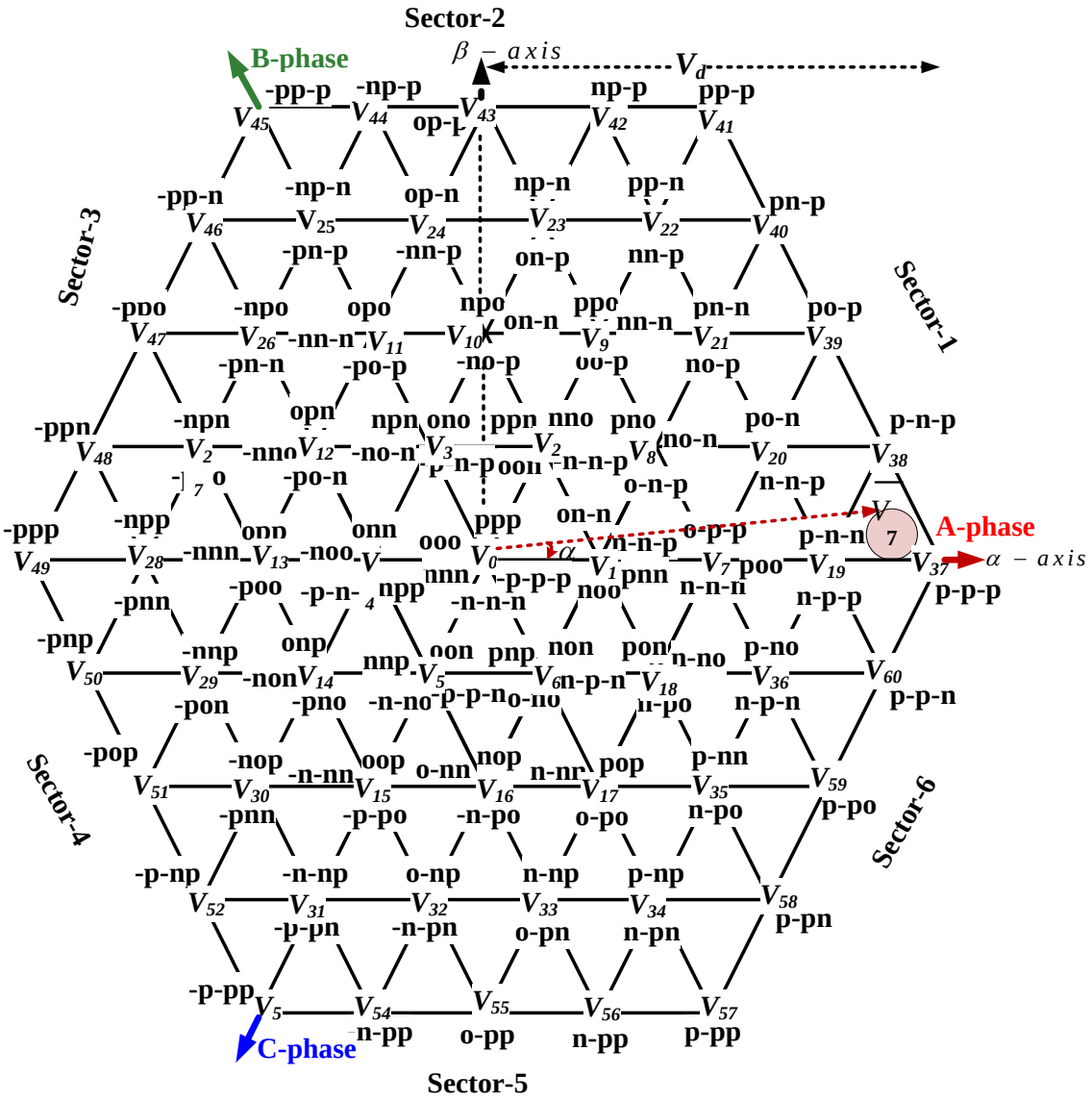


Fig. 5.3: Space vector diagram for five-level inverter

Table 5.1: Pole and line voltages for the corresponding switching states

Pole State	Pole voltages	Line voltages	S_{A1}	S_{A2}	S_{A3}	S_{A4}	S_{A1}'	S_{A2}'	S_{A3}'	S_{A4}'
p	$0.5V_d$	V_d	1	1	1	1	0	0	0	0
n	$0.25V_d$	$0.75V_d$	0	1	1	1	1	0	0	0
o	0	0.5	0	0	1	1	1	1	0	0
-n	$-0.25V_d$	$0.25V_d$	0	0	0	1	1	1	1	0
-p	$-0.5V_d$	0	0	0	0	0	1	1	1	1

In general, the five-phase five-level-inverter has 5^3=125 switching state vectors in which five are the zero voltage vectors (v_0) that are represented at the origin of the space vector plane and 120 are the active state vectors that are represented in Fig. 5.3. The 120 active vectors are again divided into inner hexagon-1 (IH1), inner hexagon-2 (IH2), inner hexagon-1 (IH3), and outer hexagon (OH) voltage vectors and they have 24, 36, 36, and 24 active vectors, respectively as shown in Fig. 5.3 [32,45, 103, 109, 111, 169]. To generalize the five-level SVM into two-level SVM, the five-level SVM has been divided into six sectors i.e., sector-1, sector-2, sector-3, sector-4, sector-5, and sector-6. However, each sector is again divided into 16 sub-sectors as shown in Fig. 5.3 in which the nodes p, n, o, -n, and -p indicate the positions of the FLDCI as shown in Fig. 5.2. The corresponding five pole and phase voltages per phase ($V_{Ao}/V_{Bo}/V_{Co}$) are given in Table-5.1 [109],[180]-[193].

5.2.2 Volt-Second Balance Principle for Five-level SVM

Considering the sector-1, the corresponding switching vectors are shown in Fig. 5.4(a). The volts-second balance principle is applied when the reference vector is in the subsector region-7 as shown in Fig. 5.4(a) then

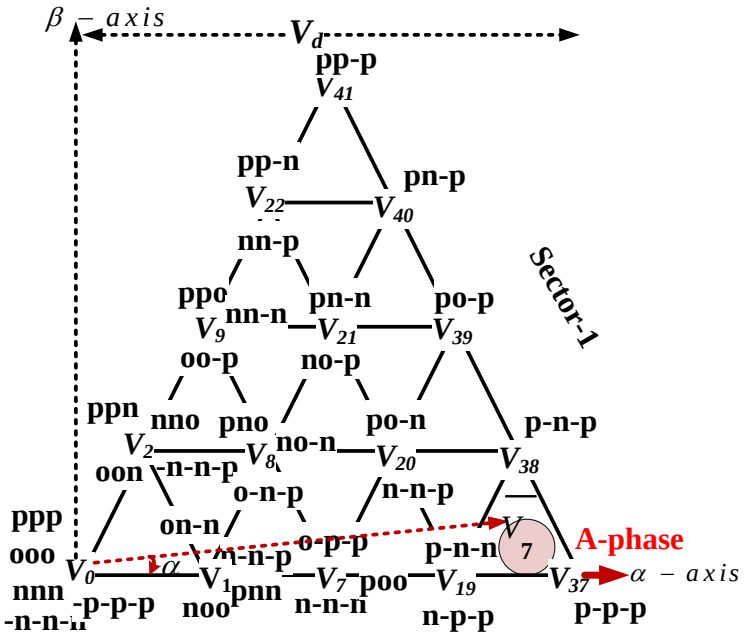
$$\left|\overline{V}\right| \angle \alpha^\circ t_s = V_{19} \angle 0^\circ t_a + V_{37} \angle 0^\circ t_b + V_{38} \angle 15^\circ t_c \tag{5.1}$$

where $\overline{v}$ and T_s are reference vector and sampling time ($T_s = T_a + T_b + T_c$). By separating the real and imaginary part from Eq. (5.1) then the switching times T_a, T_b, and T_c for the corresponding voltage are calculated as

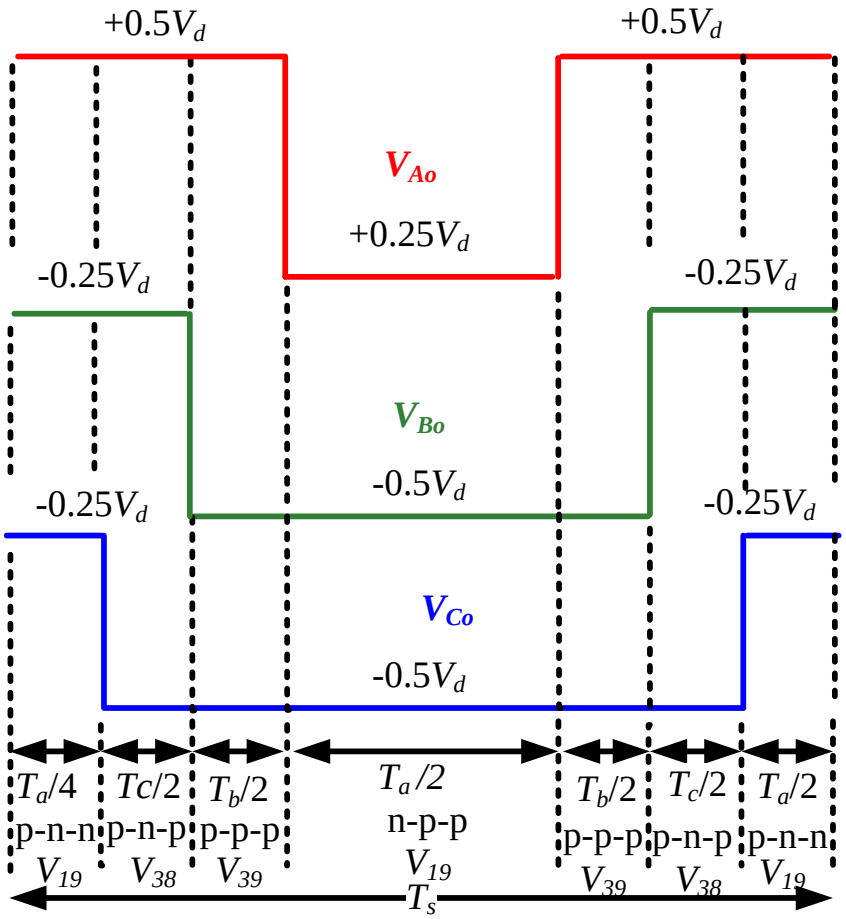
$$T_a = \frac{M T_s}{0.966} \frac{\sin \alpha}{\sin 15} \tag{5.2}$$

$$T_b = 4T_s \left[1 - \frac{2M \left(\sin(15 - \alpha) \cos 15 + \sin \alpha \right)}{\sin 30} \right] \tag{5.3}$$

$$T_c = T_s - (T_a + T_b) \tag{5.4}$$



(a) Space vector diagram at sector-1 region



(b) Pole voltages of space vector modulation at subsector region-7

Fig. 5.4: five-level SVM performance at subsector region-7

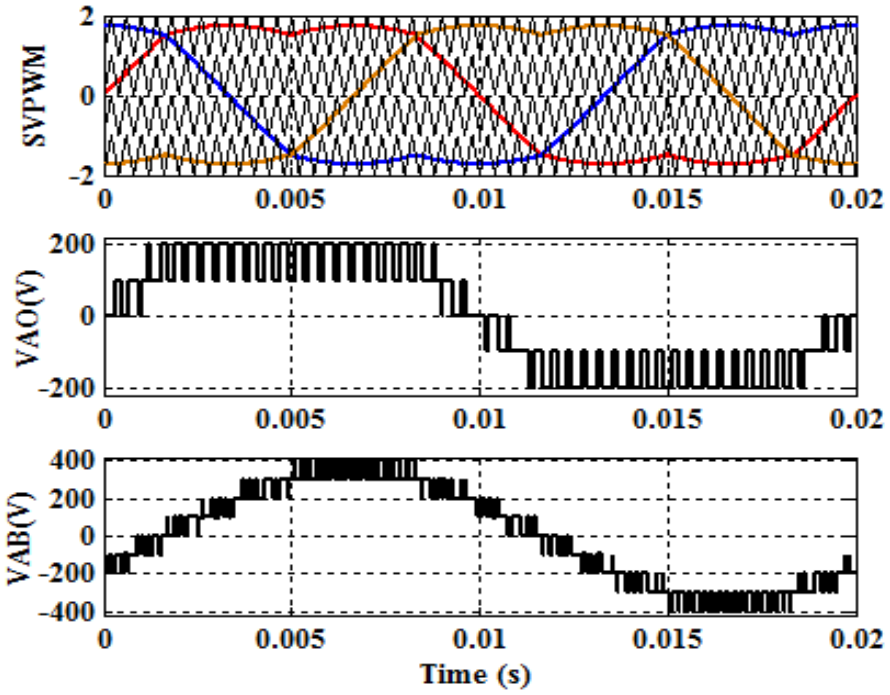


Fig. 5.5: Five modulating waves of SVPWM are compared with triangular wave, corresponding pole-voltage (V_{AO}), and Line-voltage (V_{AB})

where M is the modulation index of the space vector modulation, i.e., $M=(|\bar{V}|/V_d)$. The pole voltages for five phases are found using Eq. (5.2) to (5.4) as shown in Fig. 5.4 (b) when the reference vector is at the subsector region 7 [103, 169, 187, 196]. Similarly, the above process remains the same for finding the switching time and developing the pole voltages of the inverter in other sub-sector regions also [169, 193-196]. Moreover, the detail information of the five-level SVPWM technique is shown in Fig. 5.5 in which the pole and line voltages per phase are given for a full cycle. The voltage across the DC-link capacitors become un-balanced in a five-level diode clamped inverter. Therefore, to maintain this voltage constant, minimum energy principle is used that is explained later in detail [103, 109, 167-169].

5.2.3 DC-Capacitor-Voltage Balancing Based on Minimum Energy Principle

The FLDCI is shown in Fig. 5.2 in which the analysis of the inverter is explained with reference to Fig. 5.6. Each AC phase is interfaced to the DC terminals through a fictitious five-pole switch [196]. Based on the switching patterns of a FLDCI, the switching functions of the five-pole switches of Fig. 5.3, i.e., p_j, n_j, o_j, $-n_j$, and $-p_j$, j= A, B, and C are defined with reference to switching states of Fig. 5.2 and Table 5.1.

The switching functions determine the relationship between the AC- and DC-side variables for phase-A of the inverter as [160-169, 183, 195]

$$\left.\begin{aligned} p_A &= S_{A1}S_{A2}S_{A3}S_{A4} \\ n_A &= S_{A2}S_{A3}S_{A4}S'_{A1} \\ o_A &= S_{A3}S_{A4}S'_{A1}S'_{A2} \\ -n_A &= S_{A4}S'_{A1}S'_{A2}S'_{A3} \\ -p_A &= S'_{A1}S'_{A2}S'_{A3}S'_{A4} \end{aligned}\right\} \qquad (5.5)$$

The exact switching functions of Fig. 5.6, which is deduced from the multiplication of waveforms of Fig. 5.2, is given by Eq. (5.5).

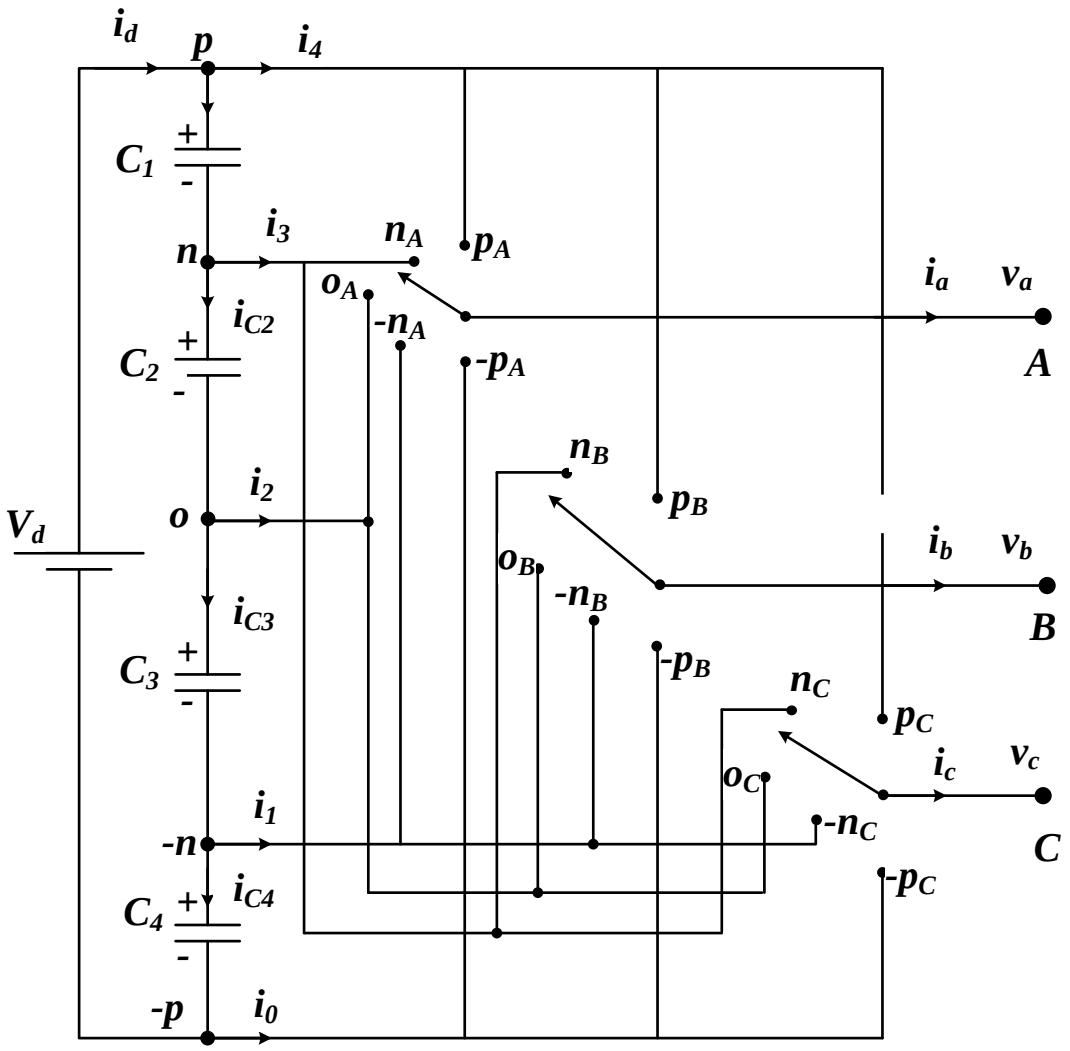


Fig. 5.6: Equivalent schematic of the FLDCI of Fig. 5.2 based on five-fictitious switches.

From Fig. 5.6, the capacitor currents can be expressed as

$$i_{C4} = i_3 + i_{C3} \qquad (5.6)$$

$$i_{C3} = i_2 + i_{C2} \qquad (5.7)$$

$$i_{C2} = i_1 + i_{C1}. \tag{5.8}$$

Considering that

$$i_{C_k} = C \frac{dv_{C_k}}{dt} \tag{5.9}$$

and

$$\sum_{k=1}^{4} \frac{dv_{C_k}}{dt} = 0 \tag{5.10}$$

The sum of capacitor currents can be realized as [195-196]

$$\sum_{k=1}^{4} i_{C_k} = 0 \tag{5.11}$$

The common current through all capacitors is not considered since it does not contribute to voltage drifts of the capacitors. Solving Eq. (5.6) to (5.8) and (5.11), it can be expressed as [187, 196]

$$i_{C_1} = \frac{1}{4}(i_1 + 2i_2 + 3i_3) - (i_1 + i_2 + i_3) \tag{5.12}$$

$$i_{C_2} = \frac{1}{4}(i_1 + 2i_2 + 3i_3) - (i_2 + i_3) \tag{5.13}$$

$$i_{C_3} = \frac{1}{4}(i_1 + 2i_2 + 3i_3) - i_3 \tag{5.14}$$

$$i_{C_4} = \frac{1}{4}(i_1 + 2i_2 + 3i_3) \tag{5.15}$$

In an FLDCI, the total energy E of 4 capacitors is

$$E = \frac{1}{2}\sum_{k=1}^{4} C_k v_{C_k}^2 \tag{5.16}$$

where

$$E = \sum_{k=1}^{4} v_{C_k} - V_d = 0 \tag{5.17}$$

Assuming that all capacitors are identical, i.e., $C_4 = \ldots C_1 = C$, the total energy E has its minimum of $(1/2)*C*(v_d^2/4)$ when all capacitor voltages are equal [169, 194-196]. This

condition is called the minimum energy property of a balanced FLDCI, which can be used as a basis for the DC-capacitor-voltage balancing and control. A control method should minimize Eq. (5.16) to achieve voltage balancing. By a change of variable from v_{Ck} to (v_{Ck} − V_d/(*m-1)*) in Eq. (5.16), the positive-definite cost function for m-level inverter can be expressed as

$$J = \frac{1}{2} C \sum_{k=1}^{m-1} \left(v_{C_k} - \frac{V_d}{m-1} \right)^2 \tag{5.18}$$

The proposed SVM DC-capacitor-voltage balancing strategy uses Eq. (5.18) for the selection of redundant switching states of a FLDCI reaches zero as its global minimum. [103, 160, 191, 196] The proposed SVM-based DC-capacitor-voltage balancing strategy uses Eq. (5.18) for the selection of redundant switching states of a FLDCI over a switching period. For a FLDCI, *J* can be expressed as

$$J = \frac{1}{2} C \sum_{k=1}^{4} \left(\Delta v_{C_k} \right)^2 \tag{5.19}$$

where Δv_{Cj} is a voltage deviation of capacitor C_k , i.e., $v_{Ck} = v_{Ck} - (V_d/4)$. Based on proper selection of redundant vectors, *J* can be minimized (ideally reduced to zero) if the capacitor voltages are maintained at voltage reference values of (V_d /4). The mathematical condition to minimize *J* is

$$\frac{dJ}{dt} = C \sum_{k=1}^{4} \left(\Delta v_{C_k} \frac{dv_{C_k}}{dt} \right) = \sum_{k=1}^{4} \left(\Delta v_{C_k} i_{C_k} \right) \leq 0 \tag{5.20}$$

where i_{Ck} is the current through capacitor C_k. $i_{Ck}, k = 1,2,3,4$ in Eq. (5.20) are affected by the DC-side intermediate branch currents i_3, i_2, and i_1 (Fig. 5.6). Currents i_3, i_2, and i_1 can be calculated if the switching states used in the switching pattern are known. Thus, it is advantageous to express Eq. (5.20) in terms of i_3, i_2, and i_1. The DC-capacitor currents are expressed as

$$i_{C_k} = \frac{1}{4} \sum_{y=1}^{3} \left(y i_y \right) - \sum_{y=k}^{3} i_y \;=,\; k = 1,2,3,4. \tag{5.21}$$

The procedures to deduce Eq. (5.21) are given in Eq. (5.6) through (5.15). Substituting for i_{Ck} from Eq. (5.21) in (5.20), the condition to achieve voltage balancing, i.e., Eq. (5.20) is deduced as

$$\sum_{k=1}^{4} \Delta v_{C_k} \left(\frac{1}{4} \sum_{y=1}^{3} y i_y - \sum_{y=k}^{3} i_y \right) \leq 0 \qquad (5.22)$$

Table 5.2: DC-side intermediate branch currents in terms of AC-Side currents for different switching states in a Sector-1

S.No.	Switching states	i_3	i_2	i_1
1	p-p-p	0	0	0
2	p-n-p	0	0	i_b
3	po-p	0	i_b	0
4	pn-p	i_b	0	0
5	pp-p	0	0	0
6	p-n-n	0	0	$-i_a$
7	n-p-p	i_a	0	0
8	po-n	*0*	i_b	i_c
9	n-n-p	i_a	*0*	i_b
10	pn-n	i_b	*0*	i_c
11	no-p	i_a	i_b	*0*
12	pp-n	*0*	*0*	i_c
13	nn-p	$-i_c$	*0*	*0*
14	poo	*0*	$-i_a$	*0*
15	n-n-n	i_a	*0*	$-i_a$
16	o-p-p	*0*	i_a	*0*
17	pno	i_b	i_c	*0*
18	no-n	i_a	i_b	i_c
19	o-n-p	*0*	i_a	i_b
20	ppo	*0*	i_c	*0*
21	nn-n	$-i_c$	*0*	i_c
22	oo-p	*0*	$-i_c$	*0*
23	pnn	$-i_a$	*0*	*0*
24	noo	i_a	$-i_a$	*0*
25	o-n-n	*0*	i_a	$-i_a$
26	-n-p-p	*0*	*0*	i_a
27	ppn	i_c	*0*	*0*
28	nno	$-i_c$	i_c	*0*
29	oo-n	*0*	$-i_c$	i_c
30	-n-n-p	*0*	*0*	i_c

Table 5.3: Interchanging phase currents in Sectors 1–6

S.No	Sector 1	Sector 2	Sector 3	Sector 4	Sector 5	Sector 6
1	i_a	$i_a \longrightarrow i_b$	$i_a \longrightarrow i_b$	$i_a \longrightarrow i_c$	$i_a \longrightarrow i_c$	i_a
2	i_b	$i_b \longrightarrow i_a$	$i_b \longrightarrow i_c$	i_b	$i_b \longrightarrow i_a$	$i_b \longrightarrow i_c$
3	i_c	i_c	$i_c \longrightarrow i_a$	$i_c \longrightarrow i_a$	$i_c \longrightarrow i_b$	$i_c \longrightarrow i_b$

Since the net DC-link voltage is regulated at V_d

$$\sum_{k=1}^{4} \Delta v_{C_k} = 0 \tag{5.23}$$

Substituting for Δv_{C4} in Eq. (5.22) from Eq. (5.23), yields

$$\sum_{k=1}^{3} \Delta v_{C_k} \left(\sum_{x=k}^{3} i_x \right) \geq 0 \tag{5.24}$$

Applying the averaging operator, over one sampling period, to Eq. (5.24) results in

$$\frac{1}{T} \int_{lT}^{(l+1)T} \sum_{k=1}^{3} \Delta v_{C_k} \left(\sum_{y=k}^{3} i_y \right) dt \geq 0 \tag{5.25}$$

Assuming that sampling period T_s, as compared to the time interval associate with the dynamics of capacitor voltages, is adequately small, the capacitor voltages can be assumed to remain constant over one sampling period and, consequently, Eq. (5.25) is simplified to

$$\sum_{k=1}^{3} \Delta v_{C_k}(l) \left(\sum_{y=k}^{3} \frac{1}{T} \int_{lT}^{(l+1)T} i_y \right) \geq 0 \tag{5.26}$$

or

$$\sum_{k=1}^{3} \Delta v_{C_k}(l) \left(\sum_{y=k}^{3} i_y(l) \right) \geq 0 \tag{5.27}$$

where $\Delta v_{C_k}(l)$ is the voltage drift of C_k at sampling period l, and $i_k(l)$ is the averaged value of the k^{th} DC-side intermediate branch current. To calculate i_k, $k = 1, 2, 3$, contributions of switching states to the DC-side intermediate branch currents and relationship between the DC- and AC-side currents, i.e., i_a, i_b, and i_c, are required. Effects of switching states on a DC-side intermediate branch current and its relationship with phase currents, corresponding to sector-1, are shown in Table 5.2. Based on Table 5.2, when the tip of reference voltage vector $\bar{v}$ is located in sector-1, the average values of the DC-side intermediate branch currents are [169, 195-196]

$$[i_3\ i_2\ i_1]^T = A[i_a\ i_b\ i_c]^T \tag{5.28}$$

where A is

$$A = \begin{bmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{bmatrix} \tag{5.29}$$

Elements of matrix A are

$$a_{11} = T_{\text{n-p-p}} + T_{\text{n-n-p}} + T_{\text{no-p}} + T_{\text{n-n-n}} + T_{\text{no-n}} - T_{\text{pnn}} + T_{\text{noo}} \tag{5.30}$$

$$a_{12} = T_{\text{pn-p}} + T_{\text{pn-n}} + T_{\text{pno}} \tag{5.31}$$

$$a_{13} = T_{\text{ppn}} - T_{\text{nn-p}} - T_{\text{nno}} - T_{\text{nn-n}} \tag{5.32}$$

$$a_{21} = -T_{\text{poo}} + T_{\text{o-p-p}} + T_{\text{o-n-p}} - T_{\text{noo}} + T_{\text{o-n-n}} \tag{5.33}$$

$$a_{22} = T_{\text{no-n}} + T_{\text{po-p}} + T_{\text{po-n}} + T_{\text{no-p}} \tag{5.34}$$

$$a_{23} = T_{\text{pno}} + T_{\text{ppo}} - T_{\text{oo-p}} + T_{\text{nno}} - T_{\text{oo-n}} \tag{5.35}$$

$$a_{31} = -T_{\text{p-n-n}} + T_{\text{-n-p-p}} - T_{\text{o-n-n}} - T_{\text{n-n-n}} \tag{5.36}$$

$$a_{32} = T_{\text{p-n-p}} + T_{\text{n-n-p}} + T_{\text{o-n-p}} \tag{5.37}$$

$$a_{33} = T_{\text{po-n}} + T_{\text{pn-n}} + T_{\text{pp-n}} + T_{\text{no-n}} + T_{\text{nn-n}} - T_{\text{-n-n-p}} + T_{\text{oo-n}} \tag{5.38}$$

where T_{ijk} , $i, j, k \in \{0, \ldots, 4\}$ denote the duty cycles of its corresponding switching vector, as calculated based on Eq. (5.1) to (5.4). The Eq. (5.28) is only valid for the calculation of i_1, i_2, and i_3 in sector-1. To calculate i_1, i_2, and i_3 in all sectors of Fig. 5.3, Eq. (5.28) is modified as

$$[i_3\ i_2\ i_1]^{\text{T}} = DS[i_a\ i_b\ i_c]^{\text{T}} \tag{5.39}$$

where

$$S = \begin{bmatrix} s_1 + s_6 & s_2 + s_3 & s_4 + s_5 \\ s_2 + s_5 & s_1 + s_4 & s_3 + s_6 \\ s_3 + s_4 & s_5 + s_6 & s_1 + s_2 \end{bmatrix} \tag{5.40}$$

and s_i, $i = 1, \ldots, 6$ denotes the sector in which the tip of the reference vector is located within. If the reference vector is in sector i, $s_i = 1$; otherwise, $s_i = 0$.

Matrix S is deduced based on the relationship between the DC-side intermediate branch currents and AC-side currents of sectors 2 to 6 with sector-1, as given by Table-5.3. When currents i_1, i_2, and i_3 are calculated by Eq. (5.39) for each set of switching combinations, they are replaced in Eq. (5.27), and the best set that maximizes

the left side of Eq. (5.27) is selected. The process outlined in this section determines the desired redundant switching states in the whole α-β plane to carry out the voltage-balancing task. The procedure to implement the proposed SVM-based balancing strategy is summarized in the diagram of Fig. 5.7 and includes the following steps [194-196]:

- Synthesis of reference voltage vector including a) identification of the sector in which the tip of $\bar{v}$ is located within, b) determination of adjacent switching voltage vectors, and c) calculation of on-duration time intervals of switching voltage vectors based on the SVM algorithm of Section-5.2 [195-196];

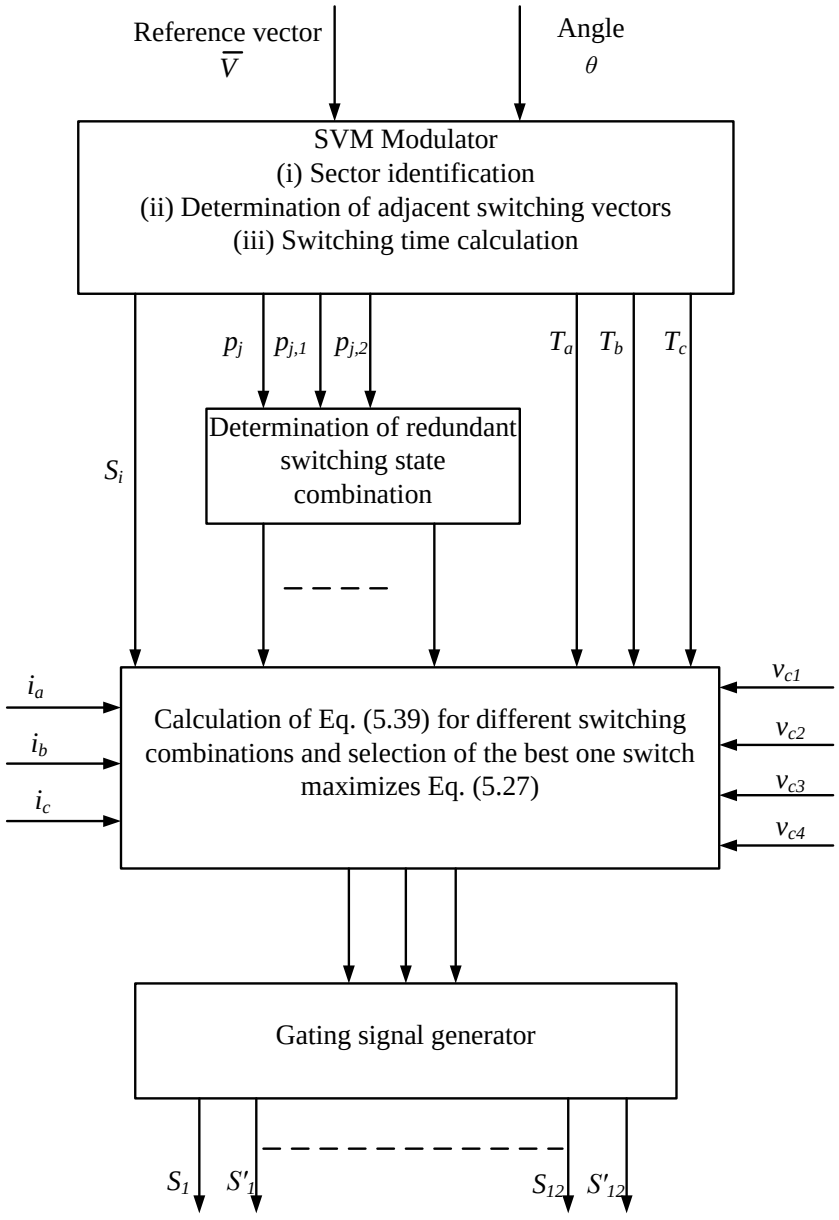


Fig. 5.7 Block diagram for the implementation of proposed SVM based capacitor voltage balancing strategy

- Determination of the switching states, including the redundant states that correspond to the adjacent switching vectors [28];
- Calculation of average values of i_3, i_2, and i_1 for each combination of redundant switching states based on Eq. (5.39);
- Replacement of the average values of i_3, i_2, and i_1 in Eq. (5.27) and the evaluation of the left side of Eq. (5.27). Among different combinations, the one that maximizes the left side of Eq. (5.27) and, consequently, minimizes Eq. (5.19) is selected to generate gating signals of the FLDCI [109, 111, 169, 196].

5.3 Type-1 Fuzzy Based Direct Torque Control for FLDCI

By transforming the five-level space vector plane into two-level space vector plane and redefining the reference voltage vector as explained in the previous sections, the developed two-level T1FDTC in the previous chapters is utilized for generating equivalent two-level switching pulses in this five-level SVM.

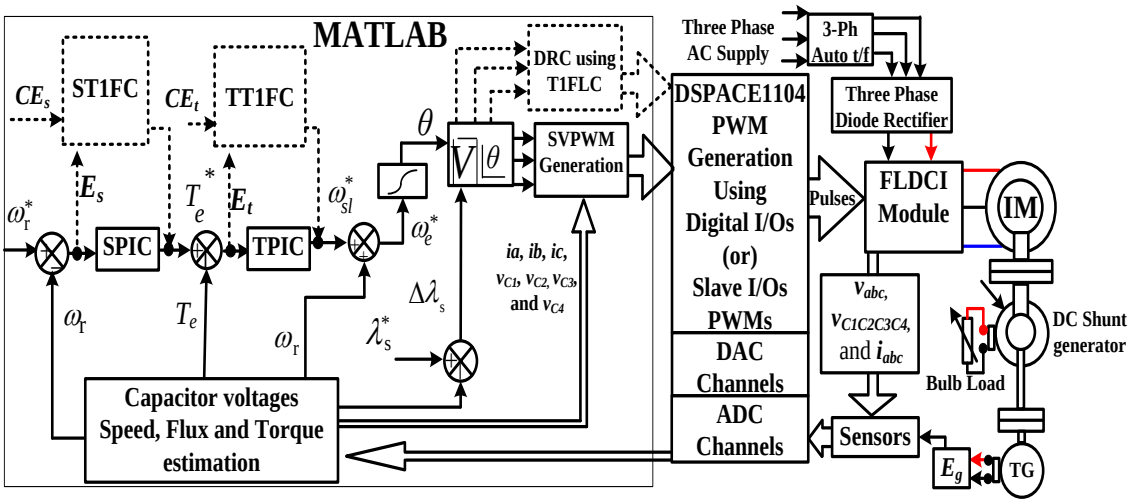


Fig. 5.8: Type-1 fuzzy based direct torque control using five-level diode clamped inverter

The obtained equivalent two-level switching states are compared with five-level space vector diagram to generate the three level switching pulses for the five-level inverter as explained in Section 5.2. The block diagram of five-level SVM with the proposed T1FDTC is shown by dotted lines in Fig. 5.8 in which the speed and torque PI-controllers are replaced by T1FLC and also the duty ratios are controlled independent of the sampling time using T1FLC.

The fuzzy rules are constructed for the scenario with fast rise time and less overshoot. Usually, these rules are determined by human experts via pre-learned algorithm, i.e., the person practically experienced while studying the IM behavior in each and every mode of operation and set the MFs and rules accordingly [30]-[33]. The sub-sector duty ratios using T1FLC for all sectors is explained earlier in chapter-3 From Eq. (3.73) to Eq. (3.81), which are independent of the switching time period and sampling time. In addition, the firing strength of the inverter is improved using T1FLC as compared to the PIDTC. This is because torque and flux are directly proportional to voltage. Moreover, PI-controllers are controlled using Mamdani-type FLC as it sets the gains appropriately for all modes of the IM drive using simple rules (IF, THEN, AND, OR, and NOT) to improve the dynamic performance of the IM drive for T1FDCI as compared to PIDTC.

5.3.1 Duty Ratio Control using T1FLC

Fig. 5.9 shows the duty ratio control (DRC) for SVM in which the corresponding duty ratios are developed with the help of T1FLC and the switching pulses are developed to the inverter using repetitive counter and DRC, which is independent of sampling time T_s like two-level inverter which is discussed in previous Chapter-3 [137]-[138].

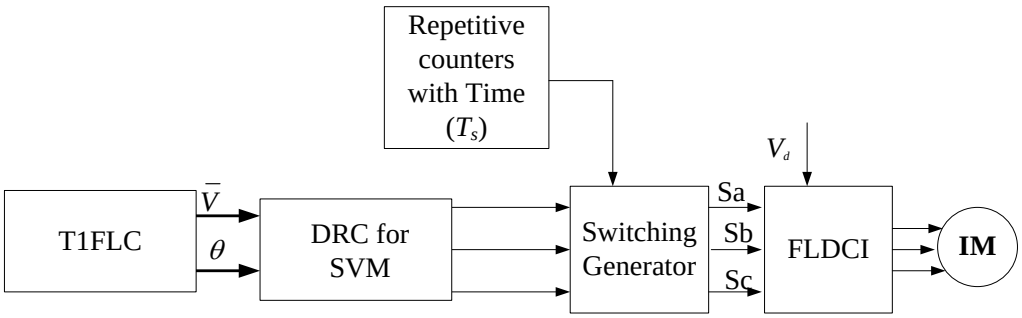


Fig. 5.9: DRC for T1FDTC using FLDCI

In addition, it can improve the quality of voltage or current waveforms under steady state by improving firing pulse of the inverter, which leads to improved flux and torque performance of the IM drive rather than PIDTC.

5.4 Type-2 fuzzy Based DTC using FLDCI

To further improve the dynamic performance of the IM drive from the huge ambiguous data, the T1FLCs are replaced by T2FLCs in which speed and torque PI-controllers are replaced by T2FLCs and the duty ratio is controlled like T1FLC.

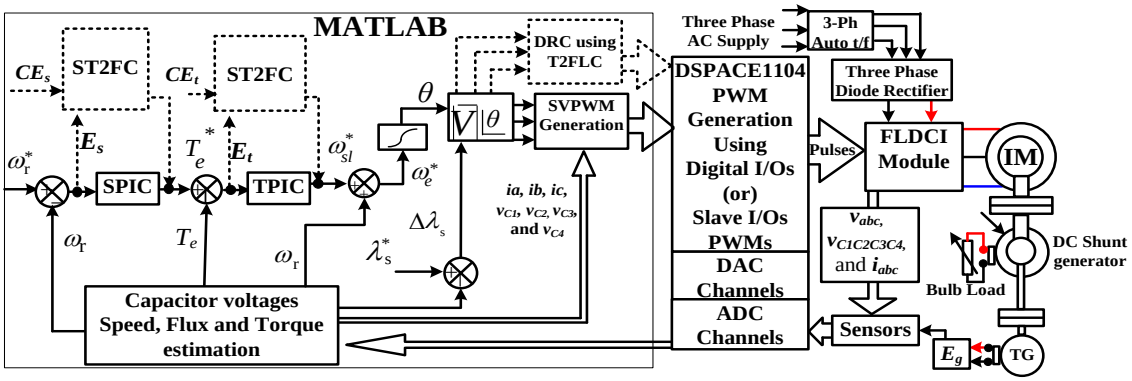


Fig. 5.10: Type-2 fuzzy based direct torque control using FLDCI

In this, after obtaining the reference voltage vector and angle θ, a two-level T2FDTC with duty ratio control which is implemented in the previous chapter is used in the place of conventional SVM to generate equivalent two-level switching pulses. The two-level switching pulses are converted into five-level switching pulses, which is described in section 5.3. The block diagram of the proposed T2FDTC for five-level SVM is as shown in Fig. 5.10. Moreover, the design procedure for T2FDTC along with duty ratio control remains the same, which is explained in detail in the previous Chapter-3.

5.4.1 Duty Ratio Control using T2FLC

Fig. 5.11 shows the duty ratio control (DRC) for SVM in which the corresponding duty ratios are developed using T2FLC and the switching pulses are developed for the inverter with the help of repetitive counter and DRC.

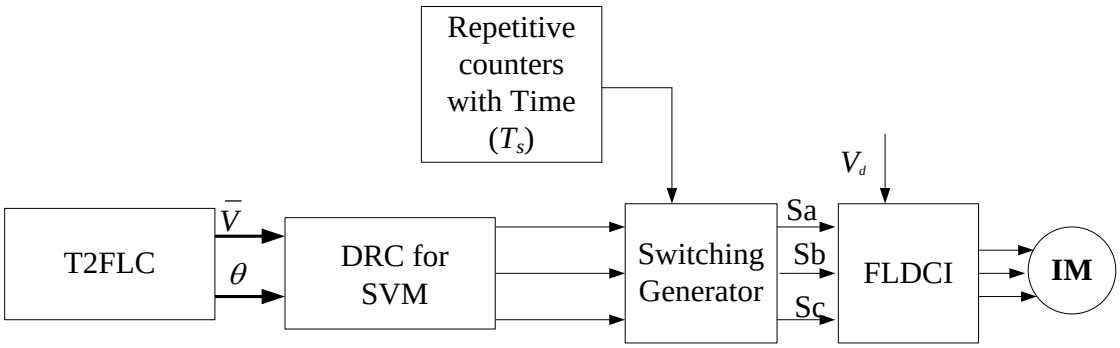


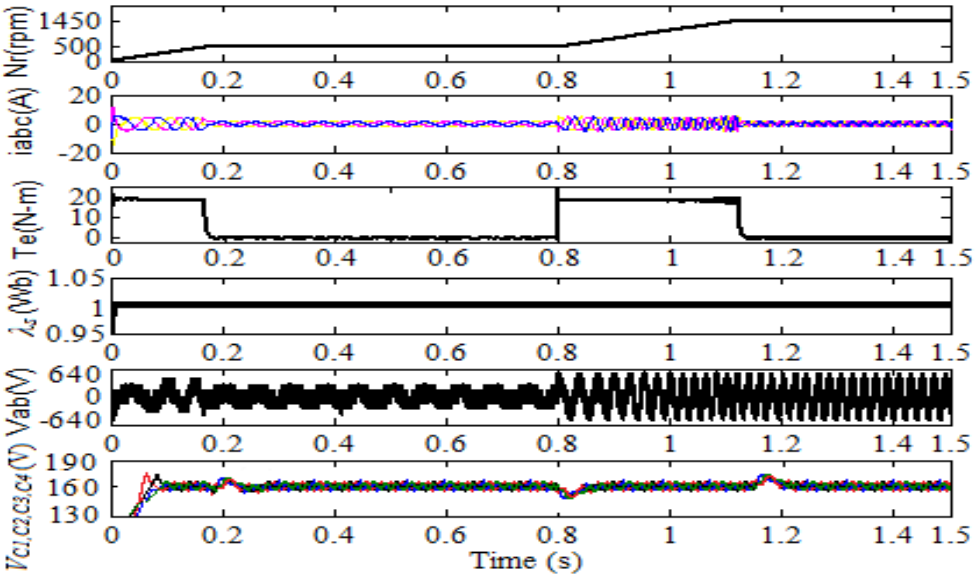
Fig. 5.11: DRC for T2FDTC using FLDCI

In addition, it can improve the quality of voltage or current waveforms under steady state by improving firing pulse of the inverter, which leads to improved flux and torque performance of the IM drive rather than PIDTC [138].

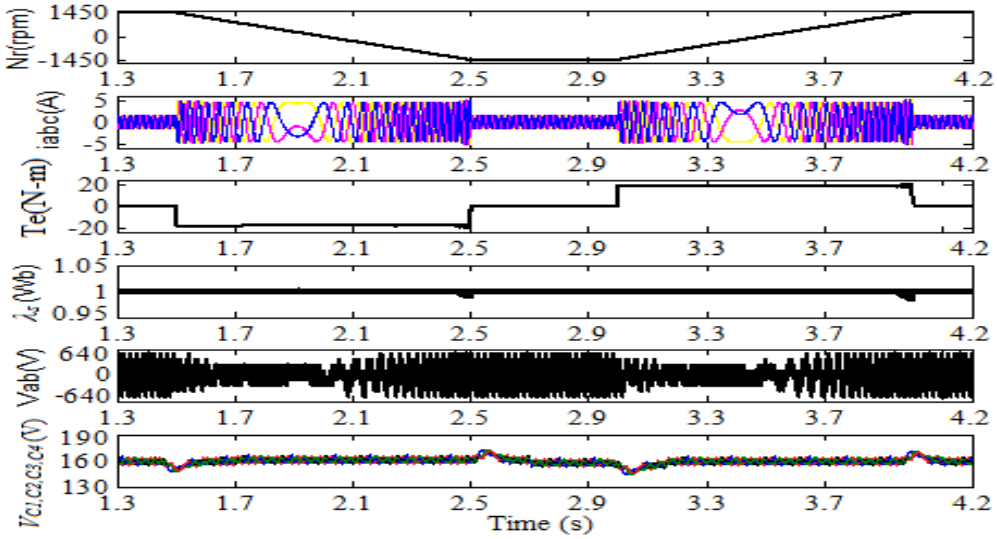
5.5 Results and Discussion

5.5.1 Simulation Results

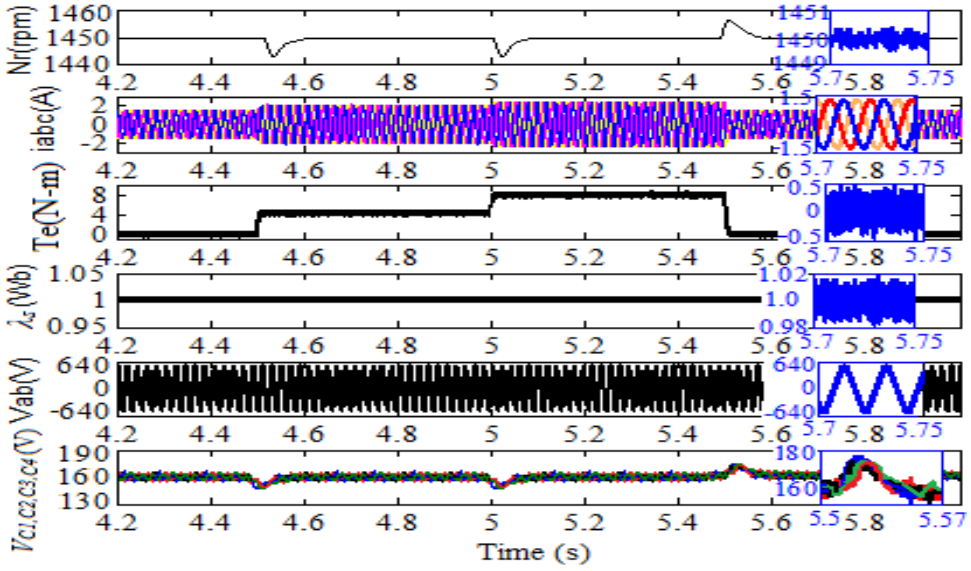
The PIDTC along with FLDCI is simulated in MATLAB using a SVM with the switching frequency of 5 kHz, and the sampling time of 45μs for 2HP IM. The reference speed during starting is taken as 500rpm, and subsequently a step change in reference speed from 500 rpm to 1450 rpm is initiated at 0.8s with the applied DC-link voltage of 640V as shown in Fig. 5.12(a) and the rest of the parameters are mentioned at Appendix A3. Initially, a rotating flux is developed in stator because of the three phase supply provided by the inverter. Consequently, the high starting torque and currents are developed and later speed is built up by the motor to run up to the required speed. The IM is settled at 0.19s when applied a reference speed of 500rpm at starting and the corresponding performance of the IM such as speed, currents, electromagnetic torque developed by the motor, stator flux, line voltage of the inverter and capacitor voltages (v_{c1} v_{c2}, v_{c3}, and v_{c4}) are shown in Fig. 5.12(a). At starting, half of line voltage is enough to reach the required speed (500rpm) of IM, and hence the reference vector should be within the inner hexagon of the space vector region. The line voltage and flux are almost the same from starting to the steady state. However, there is a sudden increase in capacitor voltages (v_{c1} v_{c2}, v_{c3}, and v_{c4}) at starting as well as just before getting the steady state. This is because of the capacitors act like charging and later it settles down within 2 to 3 cycles by selecting appropriate switching vector. Moreover, the flux distortion varies from 0.97Wb to 1.03Wb, i.e., ±0.03Wb. When a reference speed of IM drive changes from 500rpm to 1450rpm at 0.8s as shown in Fig. 5.12(a) then the IM develops a large electromagnetic torque and currents to get required speed (reference speed of 1450rpm) of the IM. After reaching the reference speed at 1.18s, the IM settles at 1450rpm as shown in Fig. 5.12(a). However, the five levels appear on line voltage, which implies that the reference vector now crosses to the outer hexagon region and utilizes full of DC-link voltage (640V). Moreover, the capacitor voltages gets reduced and increased significantly during sudden increase and decrease of the IM currents at 0.8s and 1.18s, respectively, because the capacitors are discharging and charging the energy when the IM draws large or small currents through the capacitors and later settles down after 2 to 3 cycles like a buffer.



(a) Starting and step change in reference speed from 500rpm to 1450rpm at 0.8s

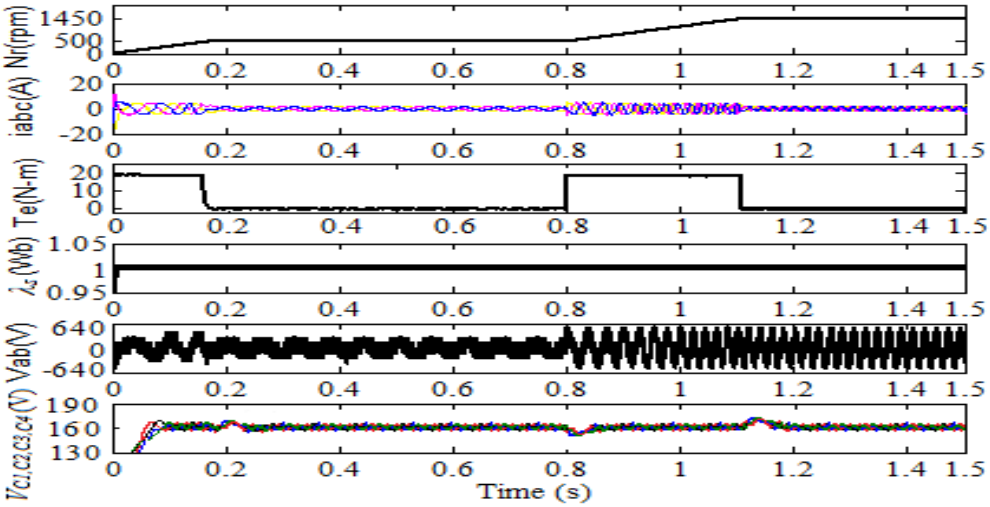


(b) Speed reversal is applied at 1.5s and 3s

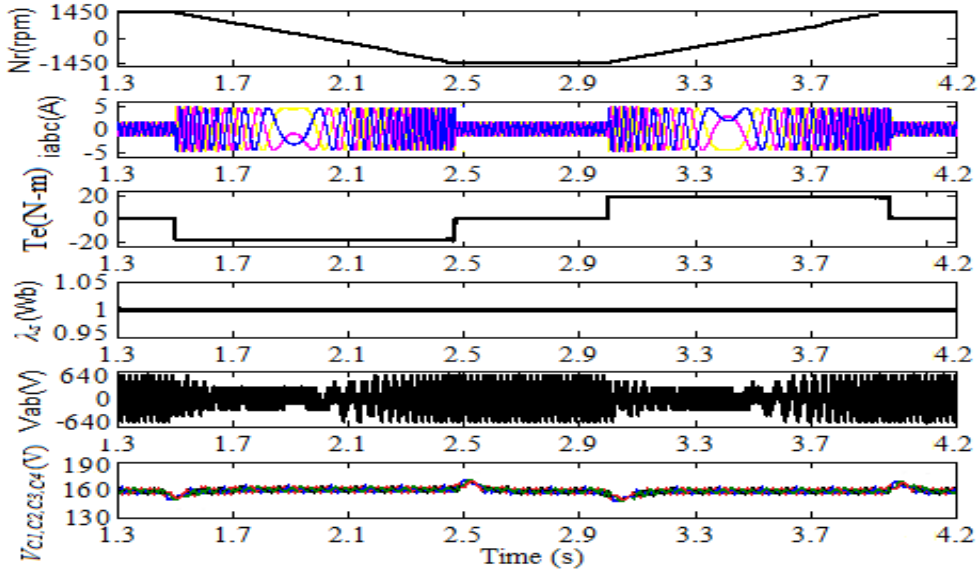


(c) Load of 4N-m, 8N-m, and 0N-m is applied at 4.5s, 5s, and 5.5s

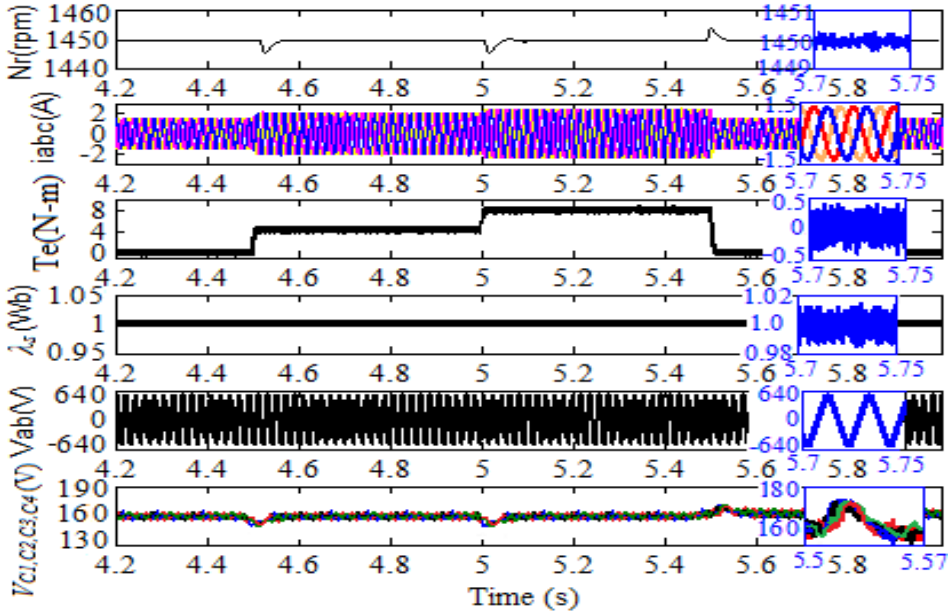
Fig. 5.12: PIDTC of IM drive for FLDCI under different operating modes



(a) Starting and step change in reference speed from 500rpm to 1450rpm at 0.8s

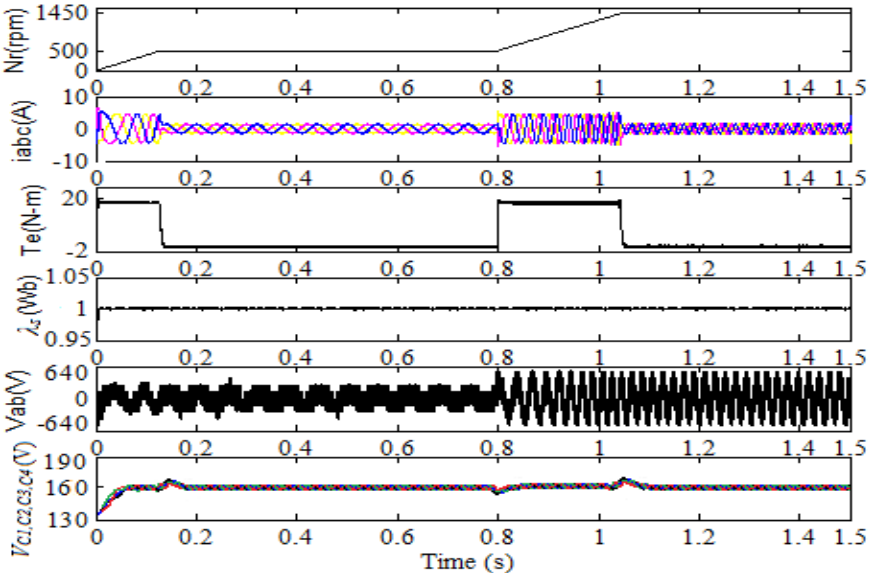


(b) Speed reversal is applied at 1.5s and 3s

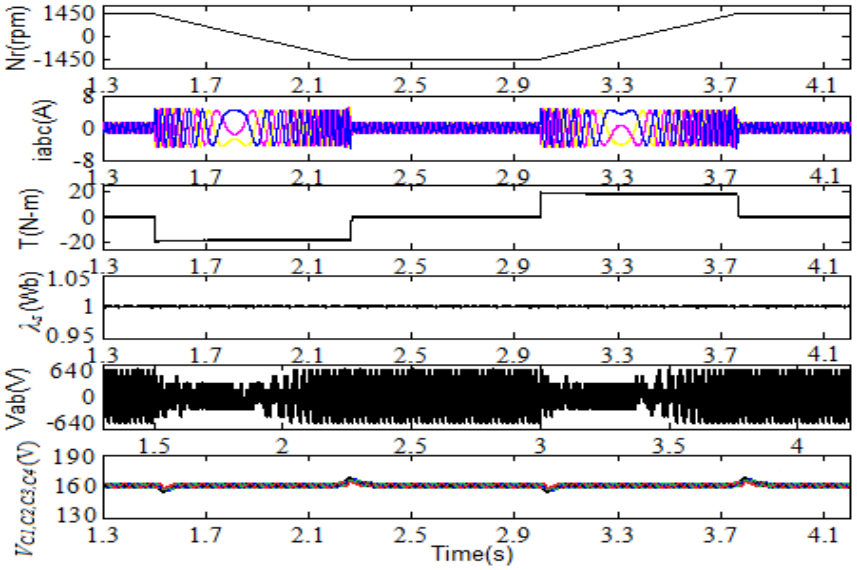


(c) Load of 4N-m, 8N-m, and 0N-m is applied at 4.5s, 5s, and 5.5s

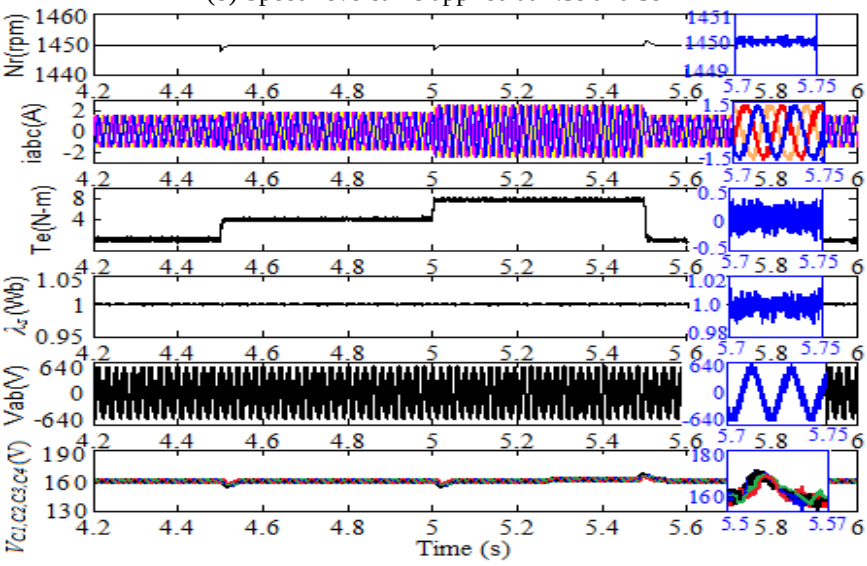
Fig. 5.13: T1FDTC of IM drive for FLDCI under different operating modes



(a) Starting and step change in reference speed from 500rpm to 1450rpm at 0.8s



(b) Speed reversal is applied at 1.5s and 3s



(c) Load of 4N-m, 8N-m, and 0N-m is applied at 4.5s, 5s, and 5.5s

Fig. 5.14: T2FDTC of IM drive for FLDCI under different operating modes

When the speed reversal is initiated at 1.5s, then the IM behavior is shown in Fig. 5.12(b). To get the required speed of -1450rpm, a larger amplitude of the current (5A) and high torque of -20Nm are developed during speed reversal. The current directions also get reversed when the speed crosses to zero value and the IM is settled to -1450rpm at approximately 2.6s as shown in Fig. 5.12(b). Moreover, the capacitor voltages are reduced and increased significantly during the sudden increasing and decreasing of the IM currents at 1.5s and 2.6s, respectively. Now, the speed reversal is initiated for PIDTC of IM at 3.2s then the corresponding operation of the IM is shown in Fig. 5.12 (b), which clearly shows a mirror image to the previous case (for the duration of 1.5s to 2.6s) of the IM drive. Consequently, the steady state of the IM is reached by 4.1s.

The load of 4 N-m, 8 N-m, and 0 N-m is applied to the IM at 4.5s, 5s and 5.5s, respectively, as shown in Fig. 5.12 (c). The peak currents at above-mentioned instants are 2.2A, 2.9A, and 1.5A, respectively. Moreover, the capacitors behave like discharging, discharging, and charging during those instants of the applied load. Nevertheless, the flux is maintained almost constant throughout the operation. A sudden drop in the speed of the IM is approximately ±10rpm for every change in load torque. However, the electromagnetic torque and flux distortion of an IM drive under no-load condition varies by approximately ±0.4Nm and ±0.03Wb, respectively as shown in Fig. 5.12(c).

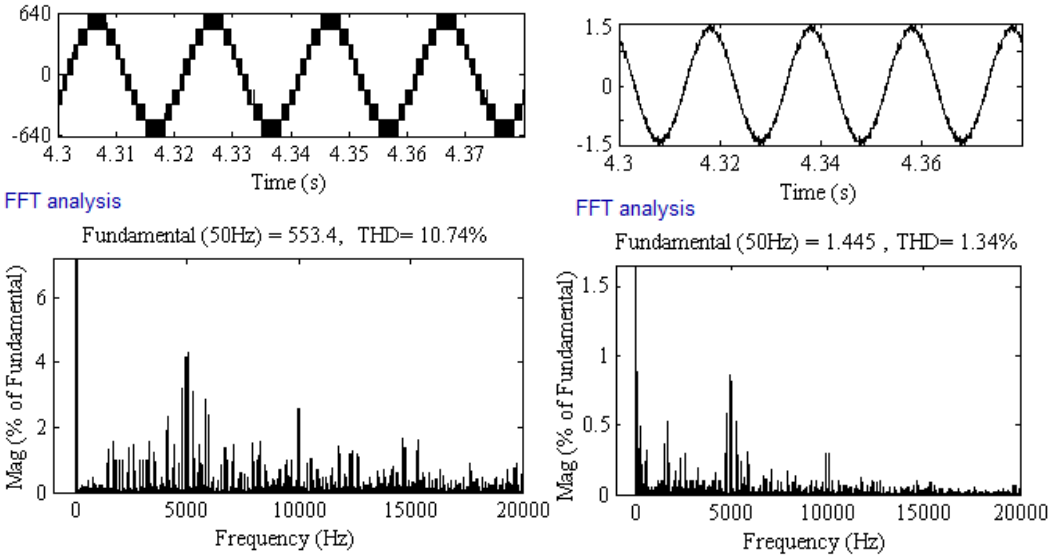
T1FDTC: With the similar operating conditions of PIDTC, the performance of the IM drive is also simulated for T1FDTC using FLDCI as shown in Fig. 5.13. Fig. 5.13 (a) shows the performance of the IM during starting while applying reference speed of 500rpm and step change in the reference speed from 500rpm to 1450rpm at 0.8s. The T1FDTC of IM provides reduced amplitude of starting current of 10A with less peaks/dips in capacitor voltages and less flux distortion than PIDTC. The T1FDTC of IM settles at 0.17s and 1.16s during starting and step change in speed, respectively, and hence the steady state of the IM is quickly reached before 1-2 cycles as compared to PIDTC.

When the speed reversal is initiated for T1FDTC at the same instants as that of PIDTC then the corresponding waveforms (speed, currents, torque, flux, line voltage and capacitor voltages) of the IM are shown in Fig. 5.13 (b). The T1FDTC of IM results in faster steady state characteristics at 2.45s and 3.95s during the speed reversal when compared to PIDTC, respectively. Moreover, TIFDTC of IM has less peaks/dips in capacitor voltages with less flux distortion than PIDTC. The same loads (4Nm, 8Nm, and 0Nm) of PIDTC are also applied to T1FDTC of IM at the same instants (4.5s, 5s, and

5.5s) as shown in Fig. 5.13 (c). The no-load flux ripples, the torque distortion, and speed fluctuation at load perturbation are reduced to 0.02Wb, 0.3N-m, and 5rpm, respectively when compared to PIDTC. Also, T1FDTC provides faster dynamic response with less peaks/dips of the capacitor voltages than PIDTC during starting, step changes in speed, speed reversal, and load perturbation.

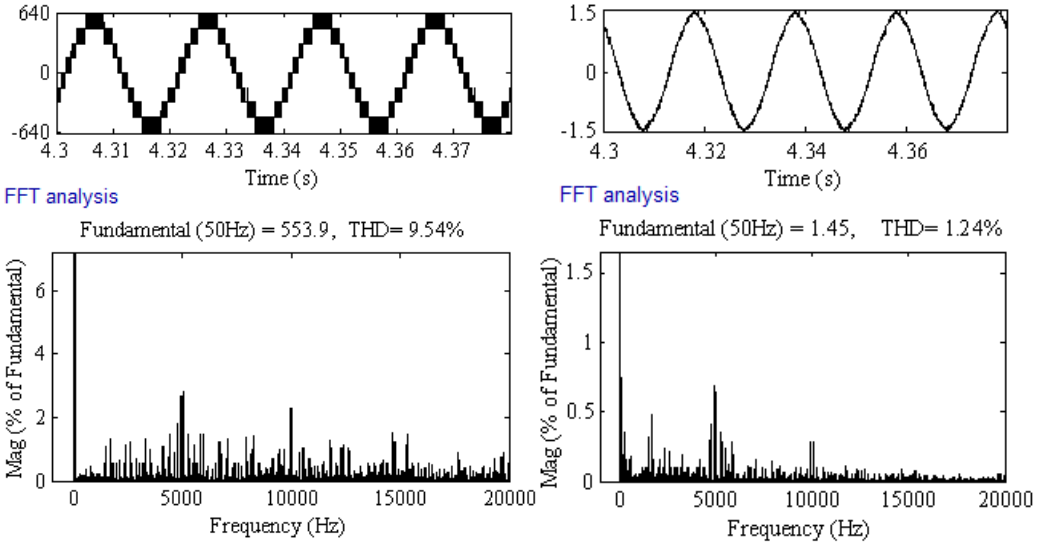
T2FDTC: The performance of the IM drive using T2FDTC is also simulated and the corresponding waveforms are shown in Fig. 5.14 under the similar operating conditions of PIDTC. Fig. 5.14 (a) shows the performance of the IM during starting when the reference speed of 500rpm is applied and then a step change in the reference speed from 500rpm to 1450rpm at 0.8s. The T2FDTC of IM provides a less amplitude of starting current of 8A with less peaks/dips on capacitor voltages than PIDTC. As a result, the IM settles at 0.16s and 1.15s during starting and step change in the speed, respectively. Hence, the steady state of the IM is quickly reached before 0.06s with less peaks/dips on capacitor voltages than PIDTC during a step change in the speed.

The speed reversal is initiated at the same instants as that of PIDTC then; the corresponding waveforms (speed, currents, torque, flux, and line voltage) of the IM are shown in Fig. 5.14(b). The T2FDTC of IM quickly reaches to the steady state at 2.34s and 3.85s during the speed reversal as compared to PIDTC, respectively. Moreover, the change in the capacitor voltages is less with T2FDTC control schemes speed reversal as compared to PIDTC and T1FDTC. The same loads (4Nm, 8Nm, and 0Nm) as applied with PIDTC are also applied to T2FDTC of IM at the same instants (4.5s, 5s, and 5.5s) as shown in Fig. 5.14 (c). The no-load flux ripples, the torque distortion, and speed fluctuation at load perturbation are reduced to 0.015Wb, 0.25N-m, and 3rpm, respectively, which are significantly less than the PIDTC and T1FDTC. Also, T2FDTC provides faster dynamic response with less peaks/dips in the four capacitor voltages than PIDTC during starting, step changes in speed, speed reversal and load perturbation.



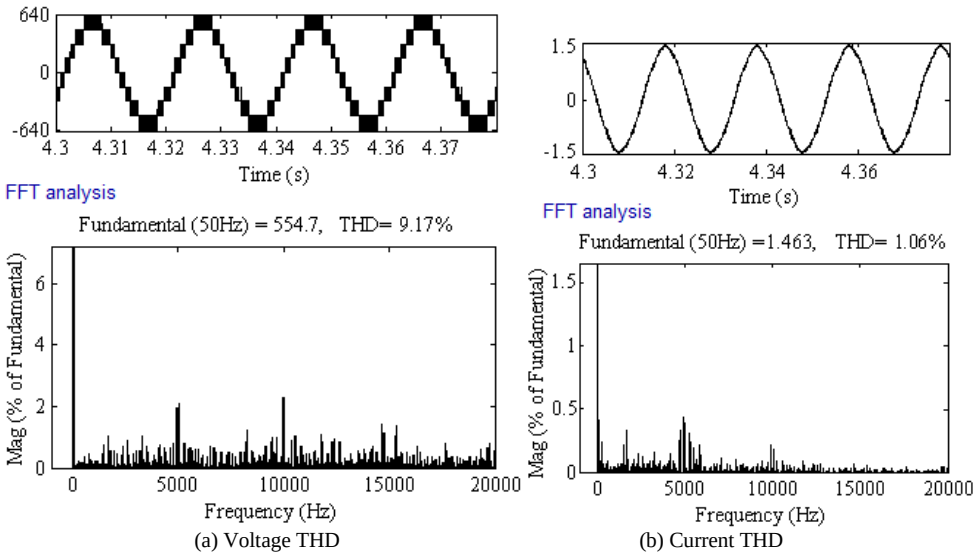
(a) Voltage THD (b) Current THD

Fig. 5.15: THD performance for the PIDTC of IM during No-load



(a) Voltage THD (b) Current THD

Fig. 5.16: THD performance for the T1FDTC of IM during No-load



(a) Voltage THD (b) Current THD

Fig. 5.17: THD performance for the T2FDTC of IM during No-load

Fig. 5.15 (a) and (b) show the percentage of line voltage and current THD for PIDTC using FLDCI of the IM during no-load operation and the corresponding values are 10.74 and 1.34, respectively. The percentage of line voltage and current THDs during no-load for T1FDTC has 9.54 and 1.24 as shown in Fig. 5.15 (a) and Fig. 5.15 (b), respectively. Fig. 5.16 (a) and Fig. 5.16 (b) give the percentage of line voltage and current THDs for T2FDTC of the IM during no-load operation and the corresponding values are 9.17 and 1.06, respectively. Therefore, it is observed from Fig. 5.14 to Fig. 5.16 that the T2FDTC has provided the least voltage and current THD, i.e., 9.17% and 1.06% than the other two control schemes (PIDTC and T1FDTC). This is due to the fact that the duty ratio are effectively controlled using T2FLC to improve the firing strength of the inverter than PIDTC and T1FDTC. Also, the T2FLC effectively deals with the huge ambiguous data using type reducer and estimates the control variable very close to the actual value.

Table 5.4 shows the simulated %THD comparison for both line voltage and current under no-load and full-load operaion by changing the switching frequency from 1kHz to 5kHz using different control schemes. Consequently, a comparative performance is studied and plotted for the corresponding line voltage THD during the no-load and full-load as shown in Fig. 5.18 (a) and Fig. 5.18 (b), respectively. Furthermore, the percentage of current THD vs. switching frequency is plotted for both no-load and full-load operation as shown in Fig. 5.19 (a) and Fig. 5.19 (b), respectively. From Fig. 5.18 and Fig. 5.19, it is observed that the T2FDTC provides less voltage and current THD value than PIDTC and T1FDTC.

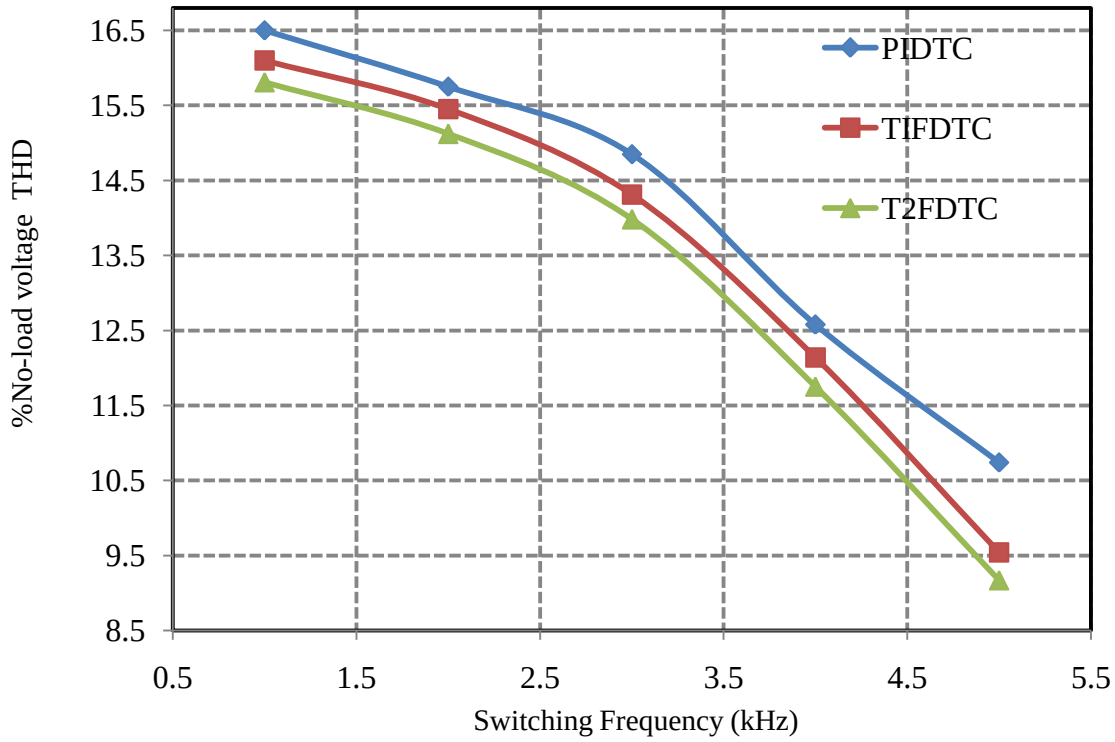
The efficiency is calculated under different loading condition with a fixed switching frequency of 5kHz as given in Table 5.5. Moreover, a graph is plotted between the percentage of the efficiency and percentage of the load for PIDTC, T1FDTC and T2FDTC as shown in Fig. 5.20. Here, T2FDTC of the IM has more efficiency than T1FDTC and PIDTC. The reason is that the T2FDTC provides less harmonics/ripples of voltage, current, flux, torque and speed, which implies that the losses should also be reduced significantly and hence the efficiency of the IM drive is significantly improved as compared to T1FDTC and PIDTC. In addition, the percentage of full load efficiency of the IM using T2FDTC is 80.15, which is the highest value than the T1FDTC and PIDTC.

Table 5.4: Simulated THD comparison for different control schemes

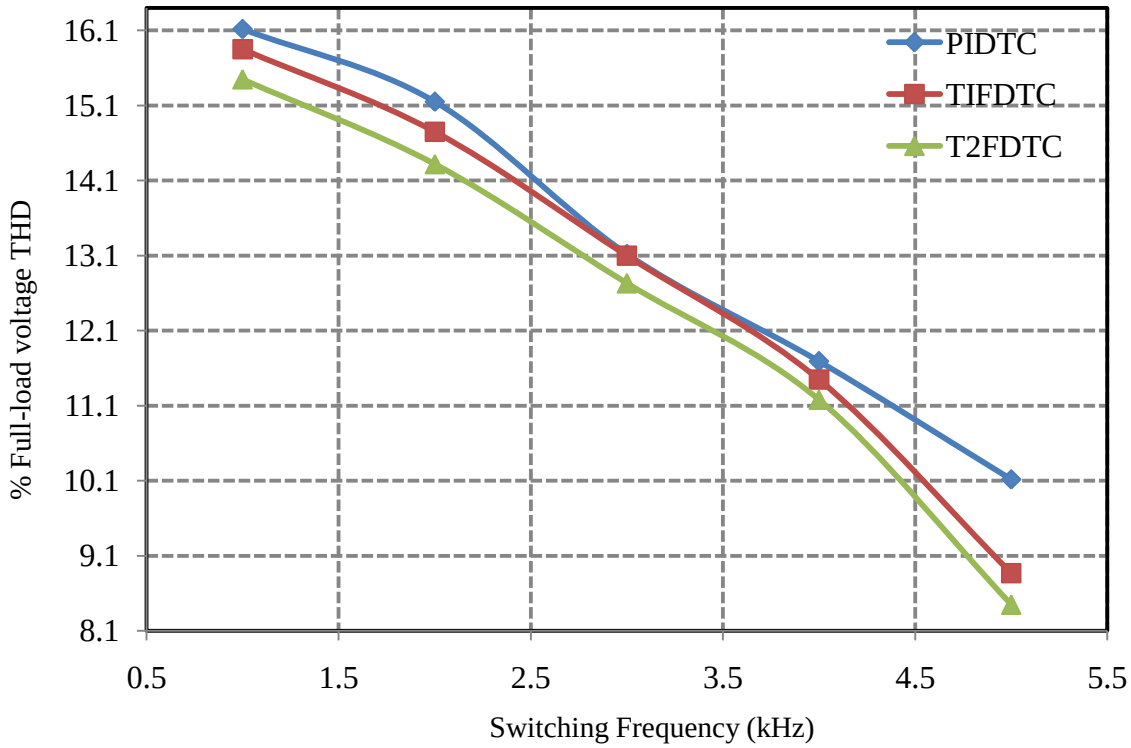
S.No.	f_{sw} (kHz)	$\%V_{THD}$			$\%i_{THD}$		
		PIDTC	TIFDTC		PIDTC	TIFDTC	
			TIFDTC	T2FDTC		TIFDTC	T2FDTC
No-Load							
1	1	16.5	16.1	15.81	3.5	3.41	3.32
2	2	15.75	15.45	15.12	2.98	2.75	2.63
3	3	14.85	14.31	13.98	2.45	2.25	2.12
4	4	12.58	12.14	11.75	1.97	1.75	1.65
5	5	10.74	9.54	9.17	1.34	1.24	1.06
Full-Load							
1	1	16.12	15.85	15.45	3.31	3.22	3.12
2	2	15.15	14.75	14.32	2.65	2.61	2.45
3	3	13.12	13.1	12.73	2.21	2.12	2.07
4	4	11.69	11.45	11.18	1.75	1.68	1.55
5	5	10.12	8.87	8.45	1.25	1.1	0.95

Table 5.5: Overall efficiency of alternative techniques during simulation

% Load	V_d(V)	I_{inv}=I_d(A)	P_{inv}(W)	ω_m(rad/s)	T_e(N-m)	P_m(W)	$\%\eta = 100*(P_{inv}/P_m)$
PIDTC							
25	640	1.5	**960**	152.8	2.26	**345.328**	35.97
50	640	1.8	**1152**	152.8	4.3	**657.04**	57.03
75	640	2.55	**1632**	152.8	7.29	**1113.91**	68.25
100	640	2.8	**1792**	152.8	9.25	**1413.4**	78.87
T1FDTC							
25	640	1.5	**960**	152.8	2.29	**349.912**	36.45
50	640	1.8	**1152**	152.8	4.34	**663.152**	57.56
75	640	2.55	**1632**	152.8	7.34	**1121.55**	68.72
100	640	2.8	**1792**	152.8	9.3	**1421.04**	79.29
T2FDTC							
25	640	1.5	**960**	152.8	2.41	**368.248**	38.35
50	640	1.8	**1152**	152.8	4.46	**681.488**	59.15
75	640	2.55	**1632**	152.8	7.4	**1130.72**	69.28
100	640	2.8	**1792**	152.8	9.4	**1436.32**	80.15

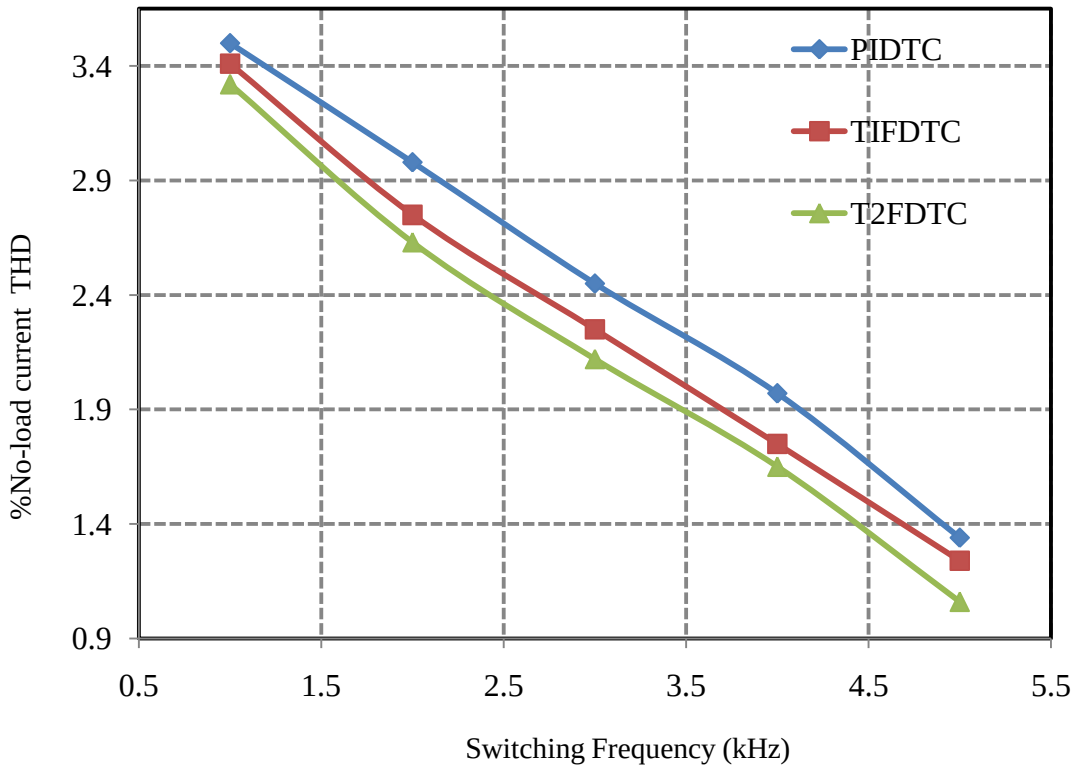


(a) No-load voltage THD vs. switching frequencyat

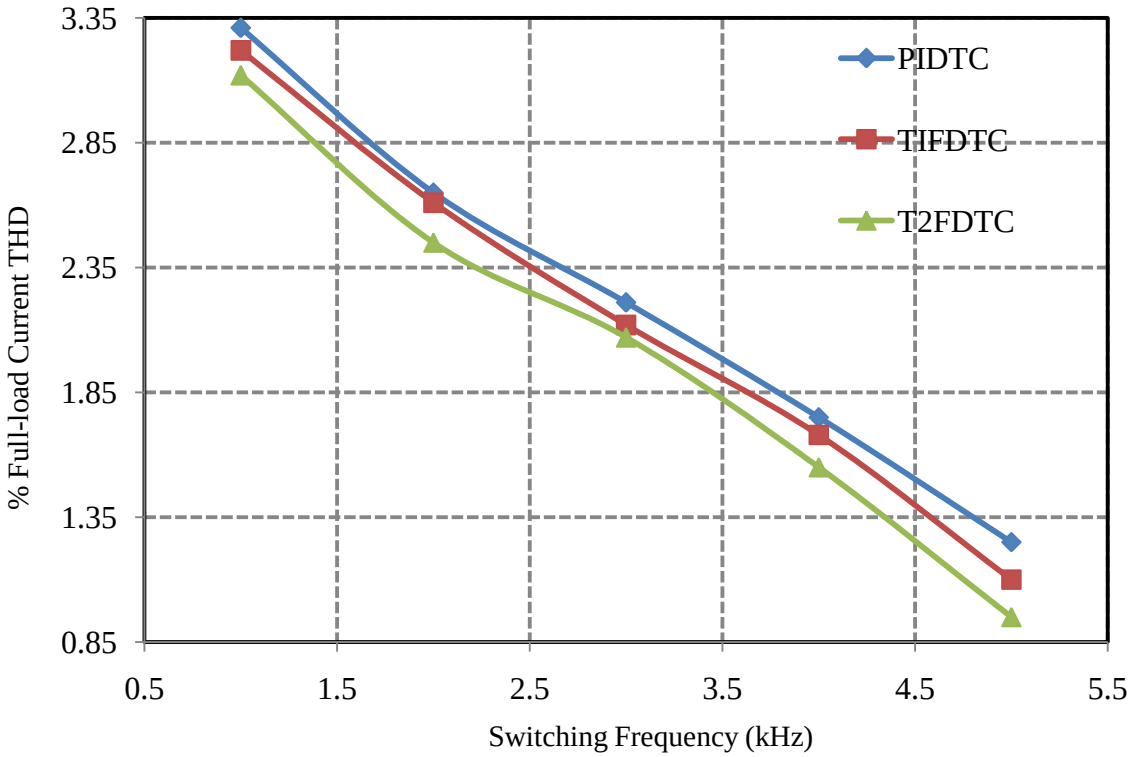


(b) Full-load voltage THD vs. switching frequency

Fig. 5.18: No-load and full-load line voltage THD of the IM drive for different control schemes



(a) No-load current THD vs. switching frequency



(b) Full-load Current THD vs. switching frequency

Fig. 5.19: No-load and full-load current THD of the IM drive for different control schemes

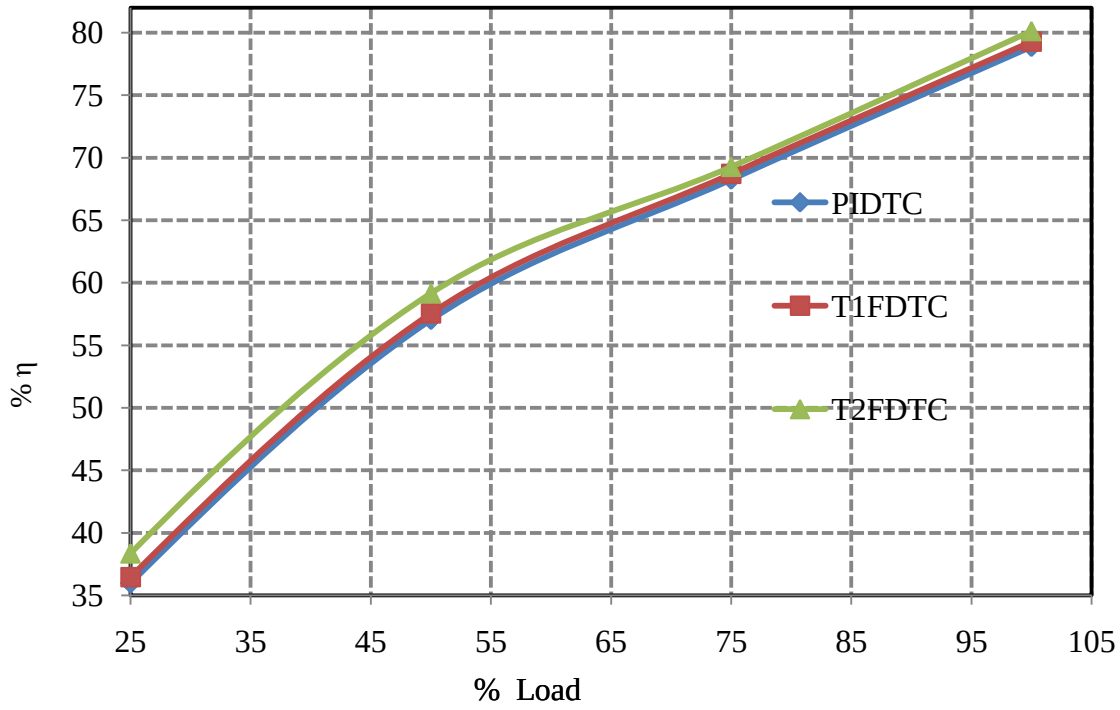


Fig. 5.20: % Overall efficiency vs. load of three alternative techniques

Table 5.6: Prospectus of different control schemes of the IM drive

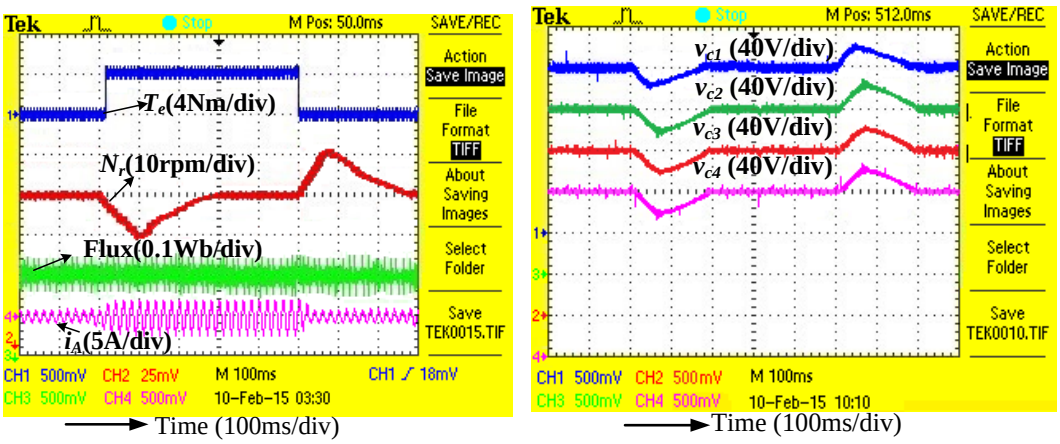
Measured parameters	**PIDTC**	**T1FDTC**	**Improvement of T1FDTC over PIDTC**	**T2FDTC**	**Improvement of T1FDTC over PIDTC**
$\pm\Psi_{dist}$ (Wb)	0.03	0.02	0.01	0.013	0.015
$\pm T_{dNL}$ (Nm)	0.4	0.3	0. 1	0.25	0.15
$\pm N_{cDL}$ (rpm)	10	4.5	5.5	3.5	6.5
$\%V_{NLTHD}$	10.74	9.54	1.2	9.17	1.57
$\%I_{NLTHD}$	1.34	1.24	0.1	1.06	0.28
$\%V_{FLTHD}$	10.12	8.87	1.25	8.45	1.67
$\%I_{FLTHD}$	1.25	1.1	0.15	0.95	0.3
$\%\eta_{FL}$	78.87	79.29	0.42	80.15	1.28
t_{st}(s)	0.19	0.17	0.02	0.16	0.03
t_{scs}(s)	1.18	1.12	0.06	1.05	0.13
t_{srf}(s)	2.6	2.45	0.15	2.34	0.26
t_{srb}(s)	4.1	3.95	0.15	3.85	0.25
t_{dl} (s)	0.1	0.05	0.05	0.02	0.08

The comparative performance, such as starting, step change in speed, speed reversal, operation during the load, voltage and current THDs, flux and torque distortion,

change in the speed during the load and efficiency at full load of the IM drive with the above control schemes are mentioned in Table 5.6 in detail.Where, T_{NLdist}, Nc_{DL}, $\%V_{NLTHD}$, $\%I_{NLTHD}$,$\%V_{FLTHD}$, $\%I_{FLTHD}$, $\%\eta_{FL}$, t_{st},t_{scs},t_{sr}, and t_{DL} are the no-load torque distortion in N-m, change in speed during the load, percentage of no-load voltage THD, percentage of no-load current THD, percentage of full-load voltage THD, percentage of full-load current THD, percentage of full-load efficiency, settling time in sec during starting, settling time in sec during step change in speed, settling time in sec during the speed reversal, and settling time in sec during the load, respectively.

5.5.2 Experimental Results

The PIDTC along with FLDCI is also verified with the experimental setup using a DSPACE DS1104 controller. The operated switching frequency of the inverter and the sampling time (50µs), DC-link voltage, and parameters of the induction machine in real time applications remain same as the simulation with a dead band of 10µs for complementary switching devices and they are mentioned in Appendix. A3. At starting, the reference speed of 1450 rpm is initiated and controlling signals are generated through a dSPACE kit and set required DC-voltage (640V) by adjusting three-phase auto-transformer. After reaching the steady-state of the IM, the step load of 4N-m is applied and removed at 0.2s and 0.7s, respectively as shown in Fig. 5.21(a). Consequently, the electromagnetic torque (T_e) rises to 4N-m and falls down to 0N-m because of the load application. The IM decelerates and accelerates to 1440rpm and 1460rpm at the above mentioned instants and it settles at 0.5s and 1s, respectively. Moreover, the settling time and drop in speed of the IM are 0.3s and 10rpm during both decelerating and accelerating modes of the operation. Moreover, the current suddenly rises to 2.2A at 0.23s and again falls down to 1.5A at 0.73s due to increase and decrease in the load, respectively. However, the flux is maintained constant throughout the operation. The torque and flux distortion for PIDTC are ±0.5N-m and ±0.04Wb, respectively. The performance of DC-link capacitor voltages (v_{c1}, $v_{c2,}$ v_{c3} and v_{c4}) for the PIDTC scheme during the load application and removal at the instants of 0.2s and 0.7s is shown in Fig. 5.21(b), respectively. The capacitor voltages settle at 0.4s and 0.9s during the application and removal of the load. The peaks and dips of capacitor voltages are varied approximately by ±30V. In addition, the settling time of the capacitors is approximately 0.2s, whereas the IM speed takes approximately 0.3s to settle during the load perturbation.

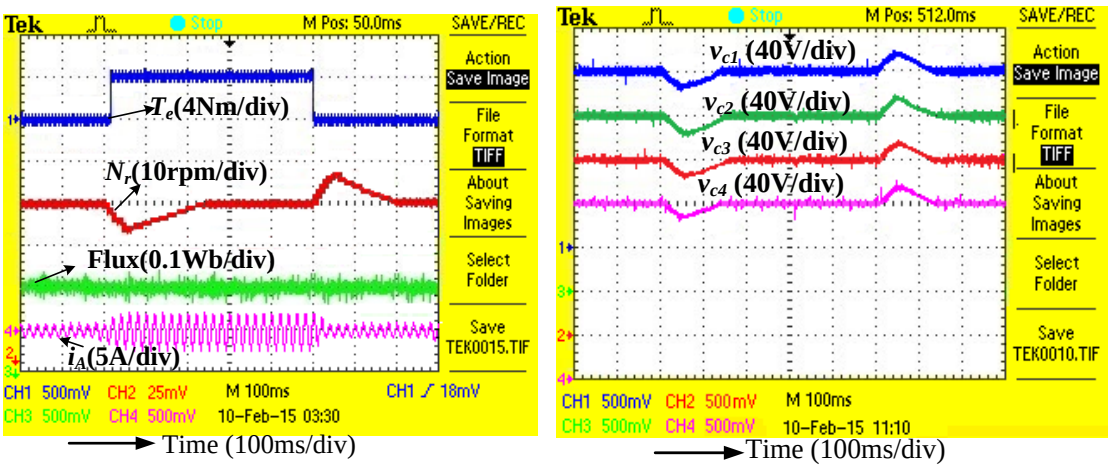


(a) Torque, speed, flux, and current performance (b) DC-link voltages across the capacitors

Fig. 5.21: Performance of the PIDTC IM during the load perturbation at 0.2s and 0.7s

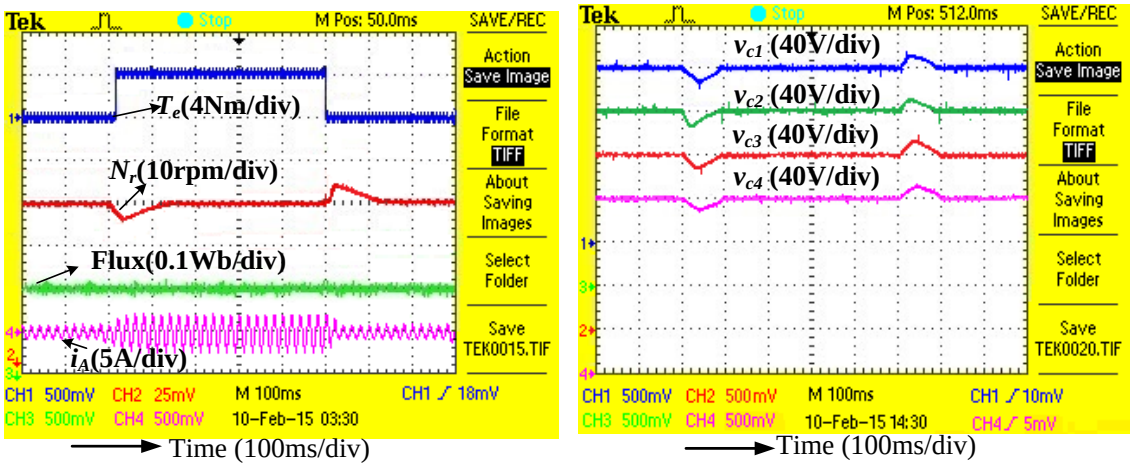
Similarly, the experimental performance for T1FDTC of the IM drive is also performed under the same operating modes. Fig. 5.22(a) shows a step change in the load (load perturbation) from 0N-m to 4N-m and 4N-m to 0N-m at 0.2s and 0.7s, respectively while running the IM at 1450rpm. The IM suddenly decelerates and accelerates to 1445rpm and 1455rpm, and later settled to 1450rpm at 0.4s and 0.9s, respectively. Therefore, the fast dynamic performance of the IM using T1FDTC is obtained approximately by 0.1s at load perturbation than PIDTC. The no-load flux and torque distortions T1FDTC are ±0.03Wb and ±0.4N-m, whereas in PIDTC has ±0.04Wb and ±0.5N-m as shown in Fig. 5.21(a). Hence, the flux and torque distortions for T1FDTC have improved by 33.33% and 20% respectively, than that of PIDTC. In addition, the change in speed during the load perturbation for T1FDTC of IM is 5rpm only, which is reduced to half of the PIDTC of IM drive.

Fig. 5.22(b) shows the performance of DC-link capacitor voltages (v_{c1}, v_{c2}, v_{c3} and v_{c4}) for the T1FDTC scheme during the load perturbation at the instants of 0.2s and 0.7s. The capacitor voltages settle approximately at 0.34s and 0.74s after the load perturbation. The peaks and dips of capacitor voltages vary approximately by ±21V. In addition, the settling time of the capacitors for T1FDTC is approximately of 0.14s, whereas the PIDTC takes approximately 0.2s to settle during the load and no-load operation. Therefore, the settling time of the capacitor voltages is faster with T1FDTC by 0.08s with fewer peaks and swells in the capacitor voltages than PIDTC.



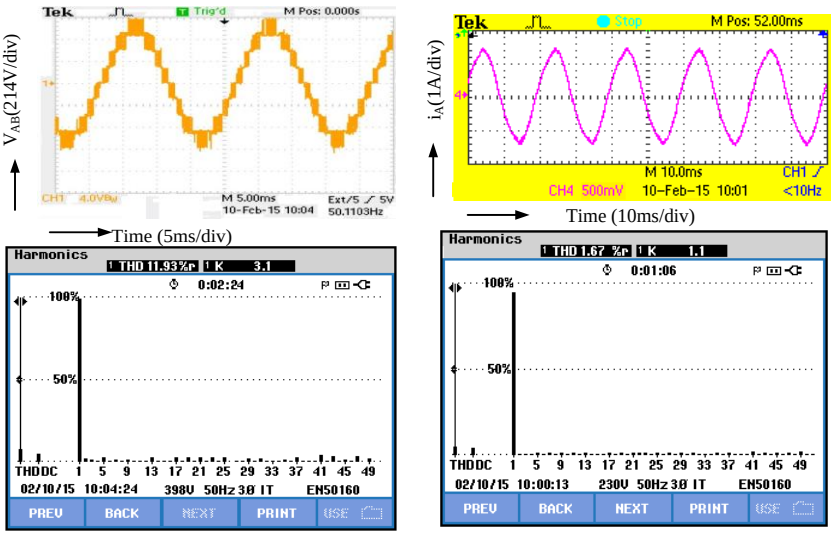
(a) Torque, speed, flux, and current performance (b) DC-link voltages across the capacitors

Fig. 5.22: Performance of the T1FDTC IM during the load perturbation at 0.2s and 0.7s



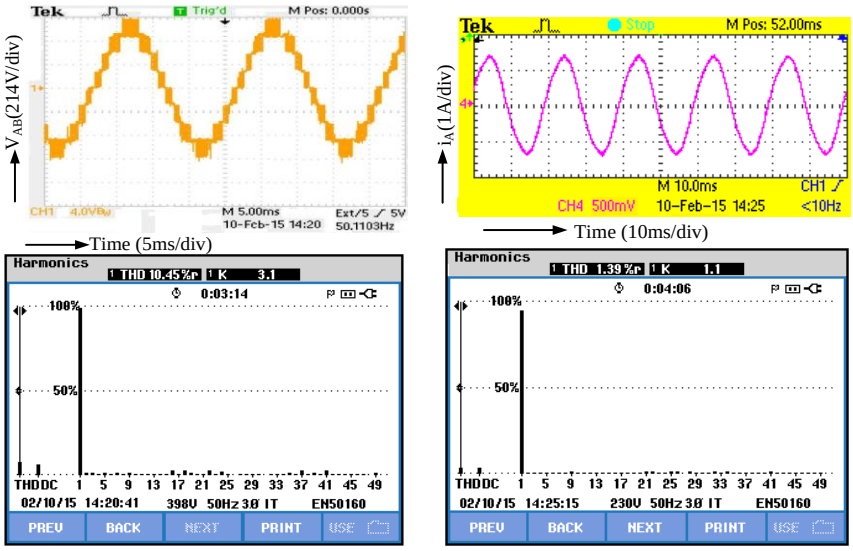
(a) Torque, speed, flux, and current performance (b) DC-link voltages across the capacitors

Fig. 5.23: Performance of the T2FDTC IM during the load perturbation at 0.2s and 0.7s



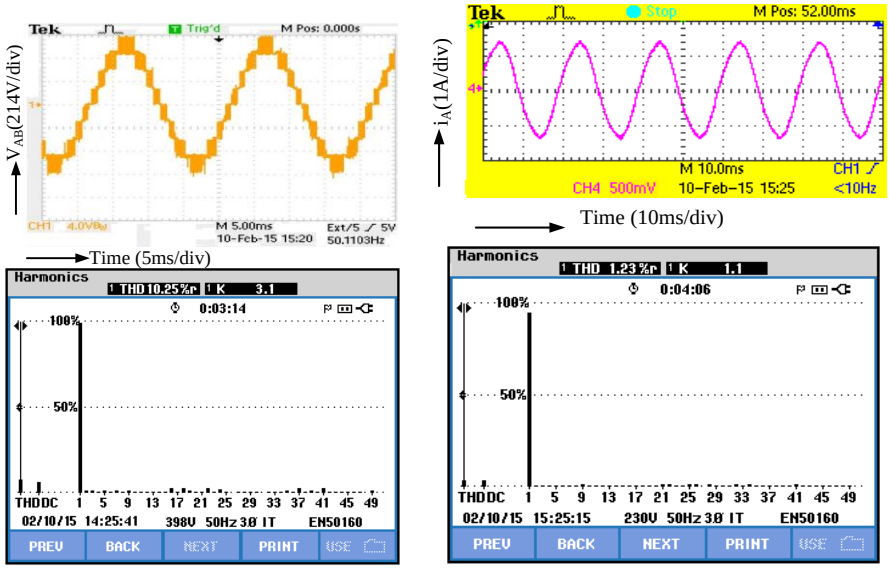
(a) Voltage THD (b) Current THD

Fig. 5.24: THD performance for the PIDTC of IM during No-load



(a) Voltage THD (b) Current THD

Fig. 5.25: THD performance for the T1FDTC of IM during No-load



(a) Voltage THD (b) Current THD

Fig. 5.26: THD performance for the T2FDTC of IM during No-load

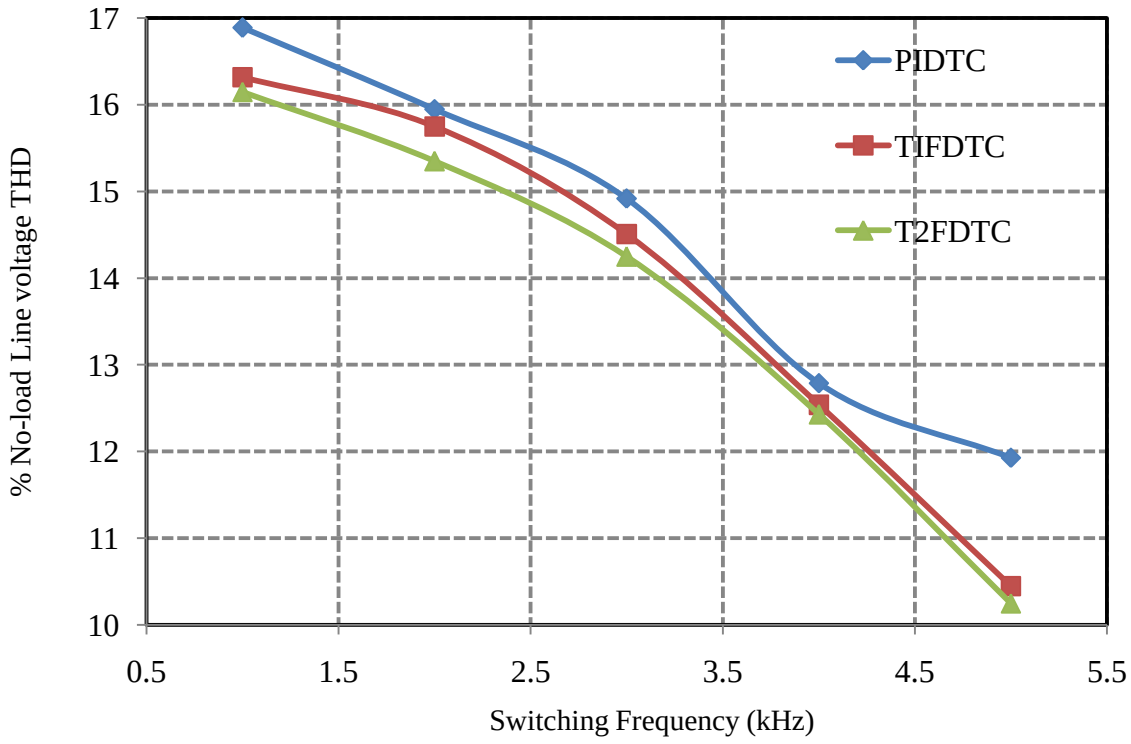
Similarly, the experimental performance for T2FDTC of the IM drive is also executed under the same operating mode. Fig. 5.23(a) shows a step change in the load (load perturbation) from 0N-m to 4N-m and 4N-m to 0N-m at 0.2s and 0.7s, respectively while running the IM at 1450rpm. Consequently, the IM develops a high torque of 4N-m with large current for getting the required speed of 1450rpm and is settled to 1450rpm at 0.34s during the application of the load, whereas PIDTC settled at 0.5s as shown in Fig. 5.21(a). Therefore, the speed of the IM with T2FDTC quickly settles by a margin of 0.16s than PIDTC. The IM speed accelerates from 1450rpm to 1454rpm and settles to 1450rpm at 0.84s during the load removal at 0.7s. Hence, the IM speed for T2FDTC settles again

faster within 0.16s during the load removal case also. In addition, the flux and torque distortion at no load are obtained as ±0.025Wb and ±0.35N-m, respectively as shown in Fig. 5.23(a). Whereas the flux and torque distortion in PIDTC are ±0.04Wb and ±0.5N-m, respectively as shown in Fig. 5.21(a). The percentage of improvement in the flux and torque distortions using T2FDTC is 37.5% and 30% over PIDTC. Also, the change in speed for T2FDTC of IM is 4rpm only, which is very less as compared to PIDTC.

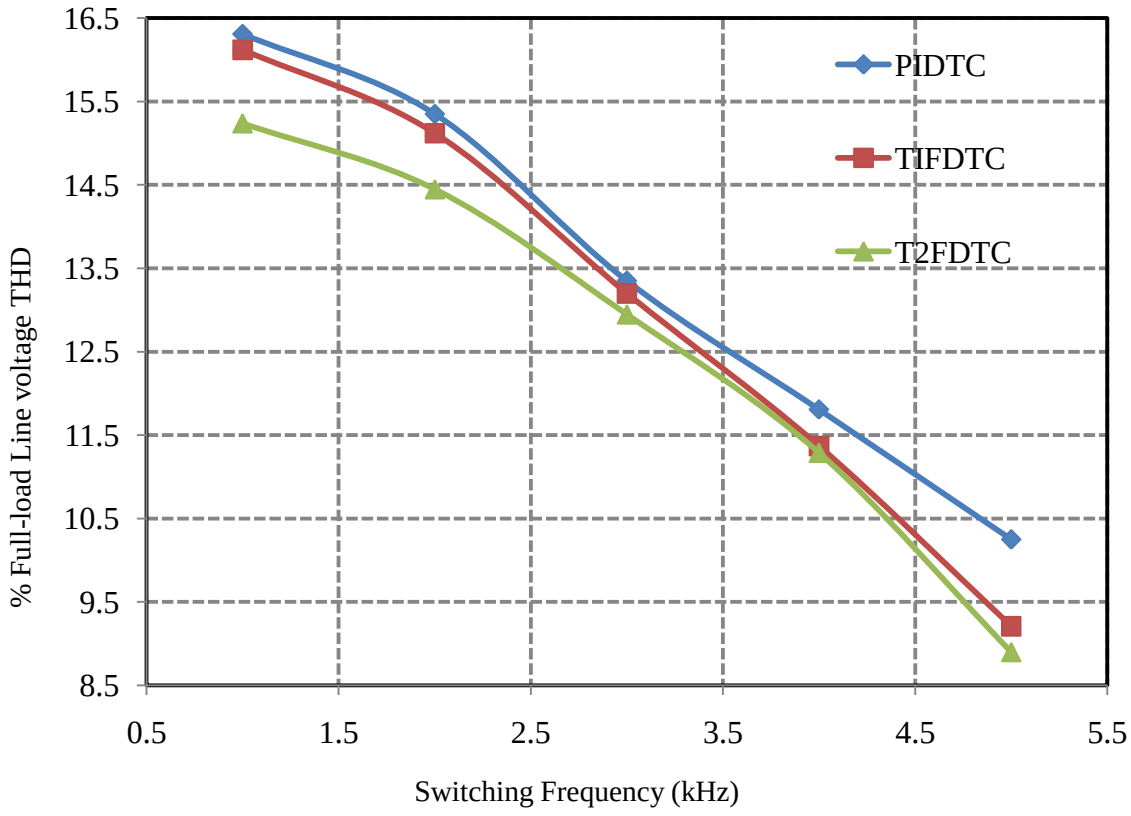
Table 5.7: Exprimental THD comparison for different control schemes

S.No.	f_{sw} (kHz)	$\%V_{THD}$			$\%i_{THD}$		
		PIDTC	TIFDTC	T2FDTC	PIDTC	T1FDTC	T2FDTC
No-Load							
1	1	16.89	16.32	16.15	3.65	3.57	3.45
2	2	15.95	15.75	15.35	3.12	2.87	2.75
3	3	14.92	14.51	14.25	2.69	2.45	2.37
4	4	12.79	12.54	12.43	2.05	1.9	1.75
5	5	11.93	10.45	10.25	1.67	1.39	1.23
Full-Load							
1	1	16.31	16.12	15.24	3.51	3.37	3.22
2	2	15.35	15.12	14.45	2.81	2.65	2.47
3	3	13.35	13.2	12.95	2.35	2.27	2.15
4	4	11.81	11.37	11.29	1.95	1.82	1.75
5	5	10.25	9.21	8.9	1.35	1.23	1.15

Fig. 5.23(b) shows the performance of DC-link capacitor voltages (v_{c1}, $v_{c2,}$ v_{c3} and v_{c4}) for the T2DTC scheme during the load perturbation at the instants of 0.2s and 0.7s. The capacitor voltages settle approximately at 0.3s and 0.7s after the load perturbation. The peaks and dips of capacitor voltages vary approximately by ±15V. In addition, the settling time of the capacitors for T1FDTC during both on-load and no-load is approximately of 0.1s, whereas the PIDTC takes approximately 0.2s to settle during the load and no-load operation. Therefore, the settling time of the capacitor voltages is faster by 0.1s with fewer peaks and swells in the capacitor voltages than PIDTC. Fig. 5.24 (a) and Fig. 5.24 (b) show the percentage of line voltage and current THD for FLDCI using PIDTC of the IM during no-load operation and the corresponding values are 11.93 and 1.67, respectively. The percentage of line voltage and current THDs during no-load for T1FDTC has 10.45 and 1.39 as shown in Fig. 5.25 (a) and Fig. 5.25 (b), respectively.

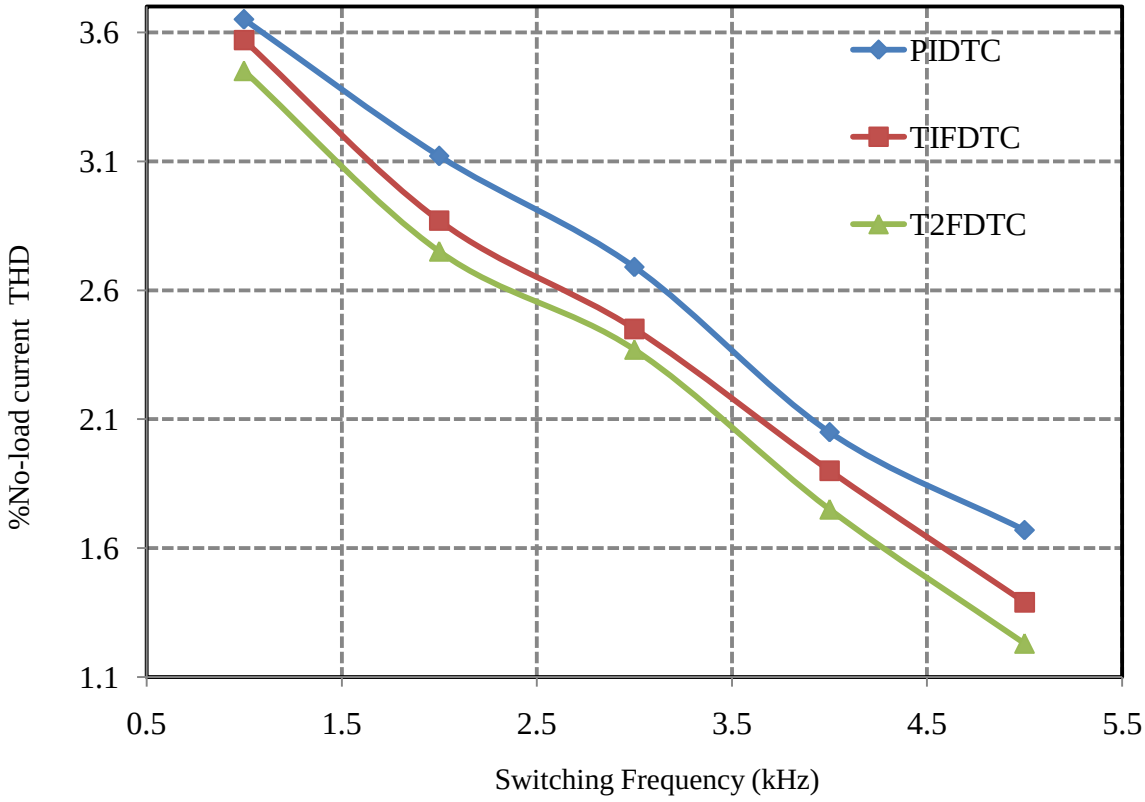


(a) No-load Line voltage THD vs. switching frequency

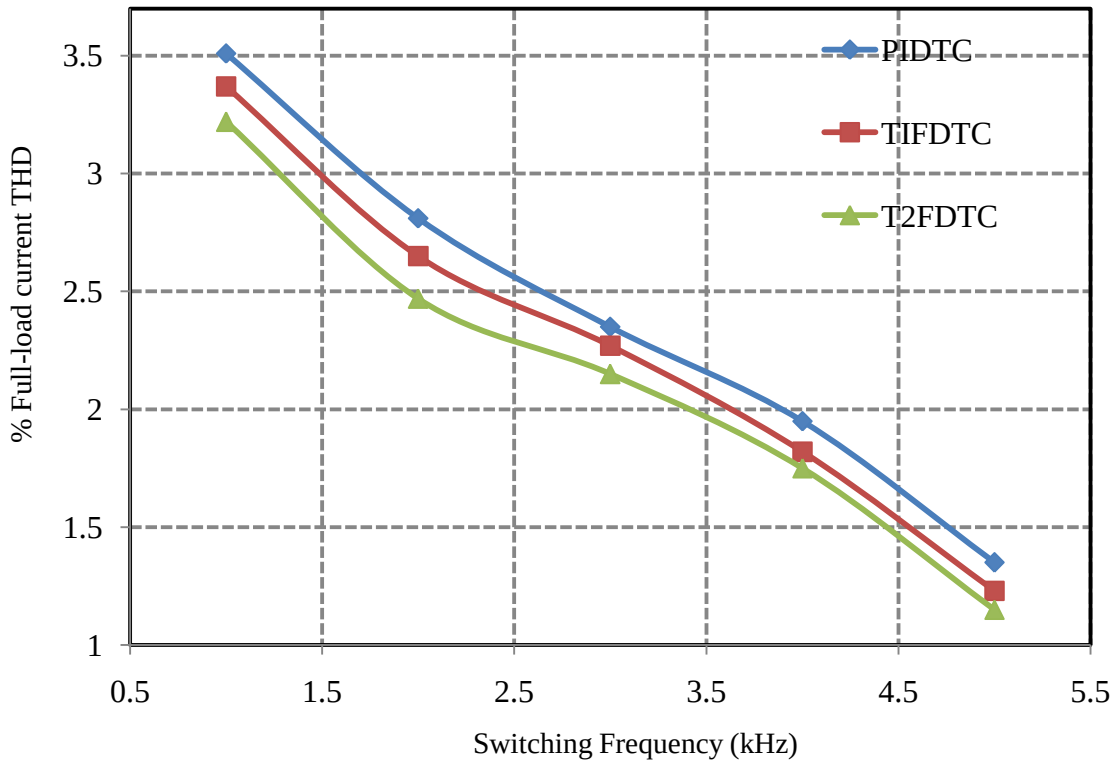


(b) Full-load Line voltage THD vs. switching frequency

Fig. 5.27: No-load and full-load line voltage THD of the IM drive for different control schemes



(a) No-load current THD vs. switching frequency



(b) Full-load current THD vs. switching frequency

Fig. 5.28: No-load and full-load current THD of the IM for different control schemes

Table 5.8 Overall efficiency of the alternative techniques

% Load	V_d(V)	I_{inv}=I_d(A)	P_{inv}(W)	ω_m(rad/s)	T_e(N-m)	P_m(W)	$\%\eta = 100*(P_{inv}/P_m)$
PIDTC							
25	640	1.5	**960**	152.8	2.22	**339.216**	35.335
50	640	1.8	**1152**	152.8	4.25	**649.4**	56.37
75	640	2.55	**1632**	152.8	7.23	**1104.74**	67.69
100	640	2.8	**1792**	152.8	9.05	**1382.84**	77.16
T1FDTC							
25	640	1.5	**960**	152.8	2.29	**349.912**	36.44
50	640	1.8	**1152**	152.8	4.34	**663.152**	57.56
75	640	2.55	**1632**	152.8	7.34	**1121.55**	68.72
100	640	2.8	**1792**	152.8	9.15	**1398.12**	78.02
T2FDTC							
25	640	1.5	**960**	152.8	2.34	**357.552**	37.25
50	640	1.8	**1152**	152.8	4.4	**672.32**	58.36
75	640	2.55	**1632**	152.8	7.39	**1129.19**	69.19
100	640	2.8	**1792**	152.8	9.35	**1428.68**	79.73

Table 5.9: Prospectus of T2FDTC, T1FDTC and PIDTC of IM drive

Measured parameters	**PIDTC**	**T1FDTC**	**T1FDTC improvement over PIDTC**	**T2FDTC**	**T1FDTC improvement over PIDTC**
$\pm\Psi_{dist}$ (Wb)	0.04	0.03	**0.01**	0.025	**0.015**
$\pm T_{dNL}$ (Nm)	0.5	0.4	**0.1**	0. 35	**0.15**
$\pm N_{cDL}$ (rpm)	10	5	**5**	4	**6**
$\%V_{NLTHD}$	11.93	10.45	**1.48**	10.25	**1.68**
$\%I_{NLTHD}$	1.67	1.39	**0.28**	1.23	**0.44**
$\%V_{FLTHD}$	10.25	9.21	**1.04**	8.9	**1.35**
$\%I_{FLTHD}$	1.35	1.23	**0.12**	1.15	**0.2**
$\%\eta_{FL}$	77.16	78.02	**0.853**	79.73	**2.558**
t_C (s)	0.2	0.14	**0.06**	0.1	**0.1**
t_{dl} (s)	0.3	0.2	**0.1**	0.16	**0.14**
v_{cd}(V)	±30	±21	**±9**	±15	**±15**

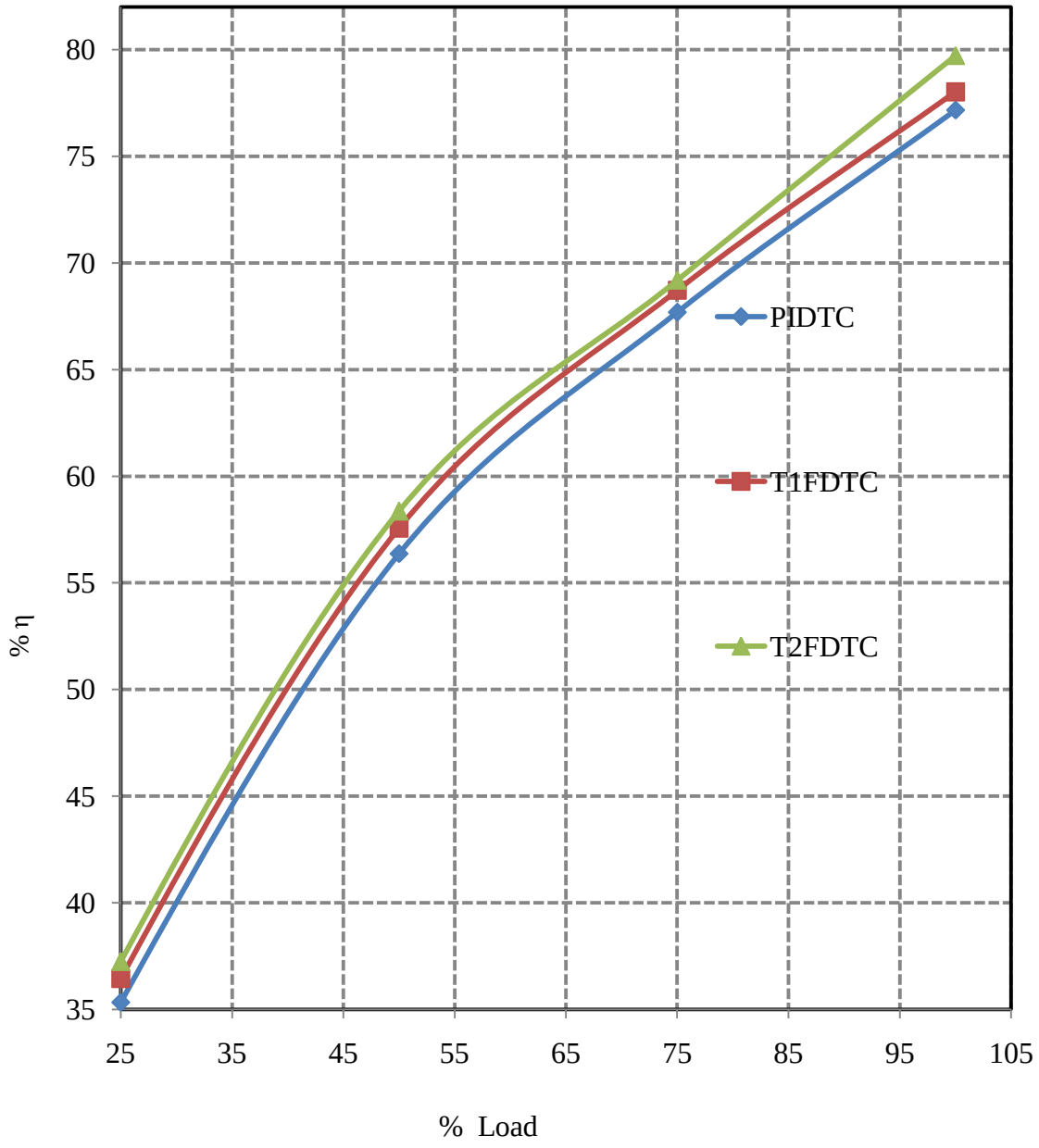


Fig. 5.29: %Overall efficiency vs. load of the IM drive for PIDTC, T1FDTC and T2FDTC

Fig. 5.26 (a) and Fig. 5.26 (b) give the percentage of line voltage and current THDs for T2FDTC of the IM during no-load operation and the corresponding values are 10.25 and 1.23, respectively. Therefore, it is observed from Fig. 5.24 to Fig. 5.26 that the T2FDTC has provided the least voltage and current THDs of 10.25% and 1.23% when compared to other two control schemes (PIDTC and T1FDTC).

Table 5.7 shows the experimental %THD comparison for both line voltage and current under no-load and full-load operation by changing the switching frequency from 1 kHz to

5kHz using different control schemes. Consequently, a comparative performance is studied and plotted for the corresponding line voltage THD during the no-load and full-load as shown in Fig. 5.27 (a) and Fig. 5.27 (b), respectively. Furthermore, the percentage of current THD vs. switching frequency is plotted for both no-load and full-load operation as shown in Fig. 5.28 (a) and Fig. 5.28 (b), respectively. From Fig. 5.27 and Fig. 5.28, it is observed that the T2FDTC provided less voltage and current THD value than PIDTC, and T1FDTC. Moreover, the efficiency is also calculated under different loading conditions with a fixed switching frequency of 5kHz as given in Table 5.8. A graph is plotted between the percentage of the efficiency and percentage of the load for PIDTC, T1FDTC and T2FDTC as shown in Fig. 5.29. Here, T2FDTC of the IM drive for FLDCI provides more efficiency than T1FDTC and PIDTC at any of the load conditions. The reason is that the T2FDTC provides less harmonics/ripples of voltage, current, and torque, which implies, the losses should be less and hence the efficiency of the IM drive significantly improved as compared to T1FDTC and PIDTC. In addition, the percentage of full load efficiency of the IM using T2FDTC is 79.73, which is the highest value among the two control schemes as mentioned above. The percentage of improvement of flux distortion, torque distortion, voltage THD, and current THD for T2FDTC of the IM drive during the no-load is 37.5, 30, 14.2, and 26.34 when compared to PIDTC. Moreover, the full-load efficiency of the IM drive for T2FDTC is improved by 3.31% over a conventional PIDTC.

The comparative performance for FLDCI using T2FDTC, T1FDTC, and PIDTC, such as starting, step change in speed, speed reversal, operation during the load, voltage and current THDs, flux and torque distortion, change in the speed during the load and efficiency at full load of the IM drive with the above control schemes are mentioned in Table 5.9 in detail, where, T_{NLdist}, Nc_{DL}, $\%V_{NLTHD}$, $\%I_{NLTHD}$,$\%V_{FLTHD}$, $\%I_{FLTHD}$,$\%\eta_{FL}$, t_C, t_{DL}, and v_{cd} are the no-load torque distortion (N-m), change in speed during the load (rpm), percentage of no-load voltage THD, percentage of no-load current THD, percentage of full-load voltage THD, percentage of full-load current THD, percentage of full-load efficiency, settling time (s) during starting, settling time (s) for the capacitors, speed settling time (s) during the load and voltage drop across the capacitors, respectively.

5.6 Conclusion

The five-level diode clamped inverter fed IM drive is simulated in the Matlab environment using PIDTC, T1FDTC and T2FDTC. The PIDTC results in considerable flux and torque ripples. However, PIDTC provide poor dynamic performance of the IM. In order to improve the dynamic performance of IM drive, the T2FDTC and T1FDTC are proposed. In both T1FDTC and T2FDTC, the torque and speed PI-controllers are replaced by type-1 or type-2 fuzzy controllers (T2FCs) to get quick dynamic performance of the IM drive than PIDTC, because the T2FC has three-dimensional control with type reduction in defuzzification process to effectively deal with the huge ambiguous data (larger footprint of data) than T1FC. Moreover, Mamdani and centroid method with simple IF and THEN rules are used in both control schemes (T1FDTC and T2FDTC). The DRC using T1FLC and T2FLC of SVM improves the firing strength of the inverter. Consequently, the current and torque ripples of IM drive can be improved significantly than PIDTC. A comparative simulated performance of the IM drive during startup, step change in speed, and load perturbation is presented. The T2FDTC provides significant improvement in the overall efficiency with less voltage and current THD of the IM drive than T1FDTC and PIDTC. In addition, the dynamic response of the IM drive using T2FDTC is improved significantly throughout any mode of operation. A prototype controller is developed in the laboratory and the control signals for PIDTC, T1FDTC and T2FDTC are generated by the dSPACE DS-1104 controller. In addition, the simulated results of the above control schemes are validated with the experimental results under the loaded operating condition. It is concluded that the T2FDTC provides fewer flux ripples, less torque distortion, less voltage and current THD, and more overall efficiency of the IM drive with fast dynamic performance thanT1FDTC and PIDTC. The percentage of improvement of flux distortion, torque distortion, voltage THD, and current THD for T2FDTC of the IM drive during the no-load is 37.5, 30, 14.2, and 26.34 when compared to PIDTC. Moreover, the full-load efficiency of the IM drive for T2FDTC is 79.73%, which is improved by 3.31% over a conventional PIDTC.

CHAPTER - 6

SYSTEM DEVELOPMENT AND EXPERIMENT

6.1 Introduction

Prototype hardware system comprising of PIDTC, T1FDTC, and T2FDTC along with dSPACE–DS1104 interfacing and related control circuits has been developed for two-level voltage source inverter (VSI), three-level diode clamped inverter (TLDCI), and five-level diode clamped inverter (FLDCI). The simulation results of the above control schemes are presented and are validated through the experimental system in the previous chapters, i.e., Chapter-3, Chapter-4 and Chapter-5. This Chapter provides the detail information about the experimental setup, which is used to execute in the real time applications. A DSP-DS1104 of dSPACE controller is used for the real time simulation and implementation of control algorithm. The control algorithm is first designed in Matlab/Simulink software and then the real time workshop of Matlab is used to generate the optimized C code for real time implementation. The interface between Matlab/Simulink and DSP (DS1104 of dSPACE) allows the control algorithm to run the hardware setup. The PIDTC, T1FDTC, and T2FDTC of IM drive is simulated and verified with the experimental setup using dSPACE DS-1104. Moreover, the following prototypes have been developed for direct torque control (DTC) in the laboratory to implement the above control schemes as

1. Enhanced two-level voltage source inverter (VSI) fed IM drive
2. Enhanced three-level diode clamped inverter (TLDCI) fed IM drive
3. Enhanced five-level diode clamped inverter (FLDCI) fed IM drive

6.1.1 Enhanced Two-level VSI fed IM drive for DTC

The two-level VSI fed IM drive has been designed and constructed to implement the T2FDTC, T1FDTC, and PIDTC control schemes as shown in Fig. 6.1 in which the DC-link voltage is provided to the inverter using the uncontrolled rectifier along with three-phase auto transformer. The power circuit of three-phase, two-level VSI generally requires six power semiconductor devices as shown in Fig. 6.1 in which the inverter module is connected to the IM and then coupled to the DC-shunt generator and DC-tacho-generator. The DC-tacho-generator is used to measure the speed of the IM in terms of generated voltage 'E_g', and is fed back by ADC-channels of the dSPACE controller through a

voltage sensor as shown in Fig. 6.1. The generated voltage is again converted to rpm by multiplying an appropriate gain of the system. The DC-shunt generator is used to check the behaviour of the IM drive during sudden load perturbation for proposed control schemes (T2FDTC and T1FDTC). In addition, the DC-link voltage and three phase voltages are measured by voltage sensors, whereas three-phase currents are measured by current sensors and they are fed back to the ADC-channels of the dSPACE controller. It should be made sure for the dSPACE controller that the ADC channels voltage and current value should not cross 5V and 400mA. However, the alternative gains can be multiplied after taking the signal from ADC channels.

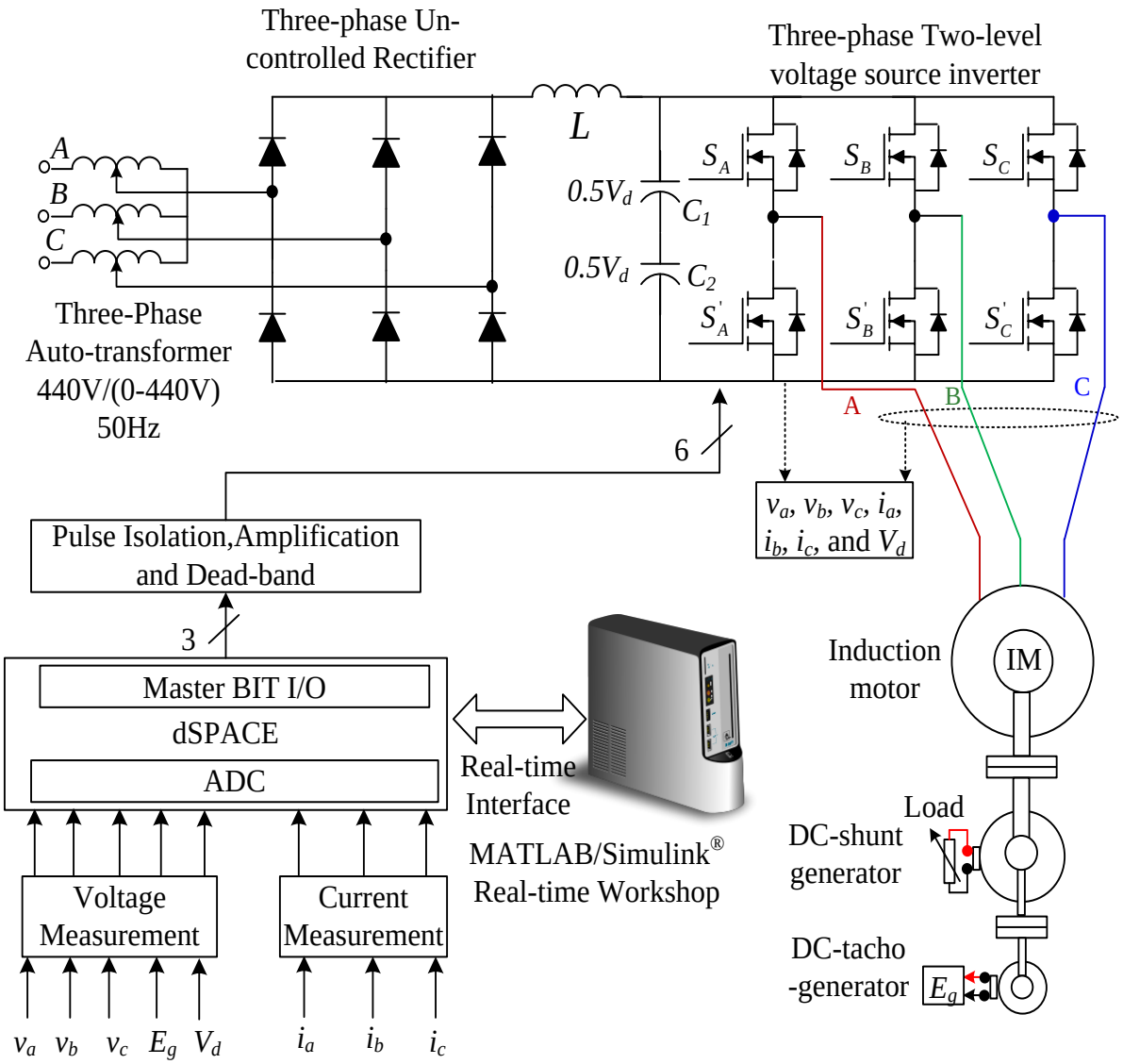


Fig. 6.1: Schematic diagram for hardware implementation of DTC using two-level VSI

6.1.2 Enhanced TLDCI fed IM drive for DTC

For the development of the DTC using TLDCI topology for the above mentioned control schemes (PIDTC, T1FDTC, and T2FDTC), 2 DC-link capacitors, 12 switching devices and 6 clamping diodes are required as shown in Fig. 6.2. More number of switching devices are connected in such a fashion that the stress on switching devices, ratings (voltage and current), voltage and current THDs are reduced significantly than the two-level VSI.

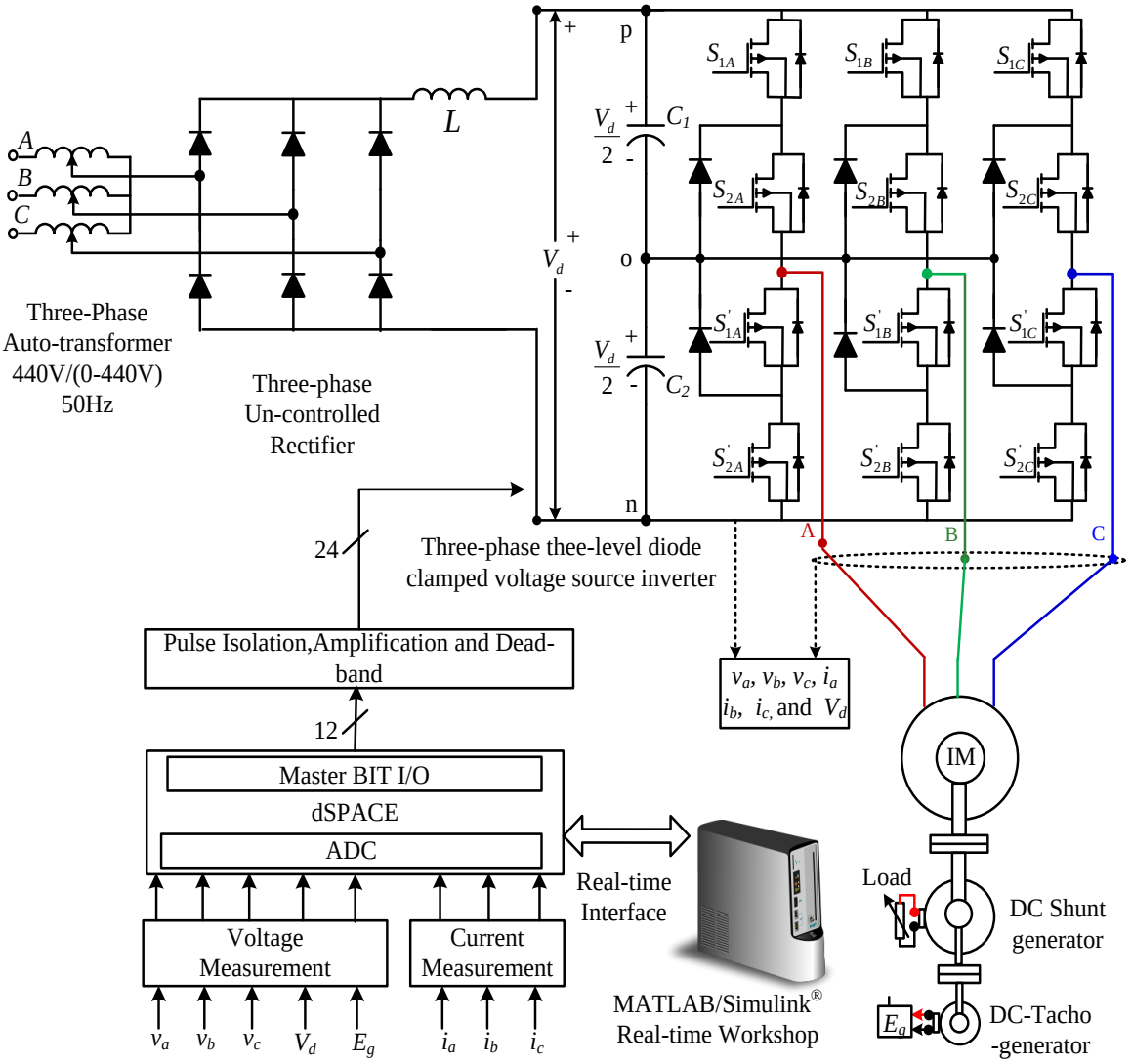


Fig. 6.2: Schematic diagram for hardware implementation of DTC using TLDCI

As a result, it produces three-level output voltage waveform with less THD under balanced input DC-link voltage condition. Here, three phase currents, three phase voltages, DC-link voltages, and generated voltage E_g, are enough to sense through the respective sensors and then connected ADC-channels of the dSPACE control.

6.1.3 Enhanced FLDCI fed IM drive for DTC

To further improve the voltage and current THD performance of the IM drive the FLDCI is used instead of two-level VSI and FLVSI as shown in Fig. 6.3 in which the number of power switching devices, clamping diodes, DC-link capacitors are 24, 18, and 4, respectively.

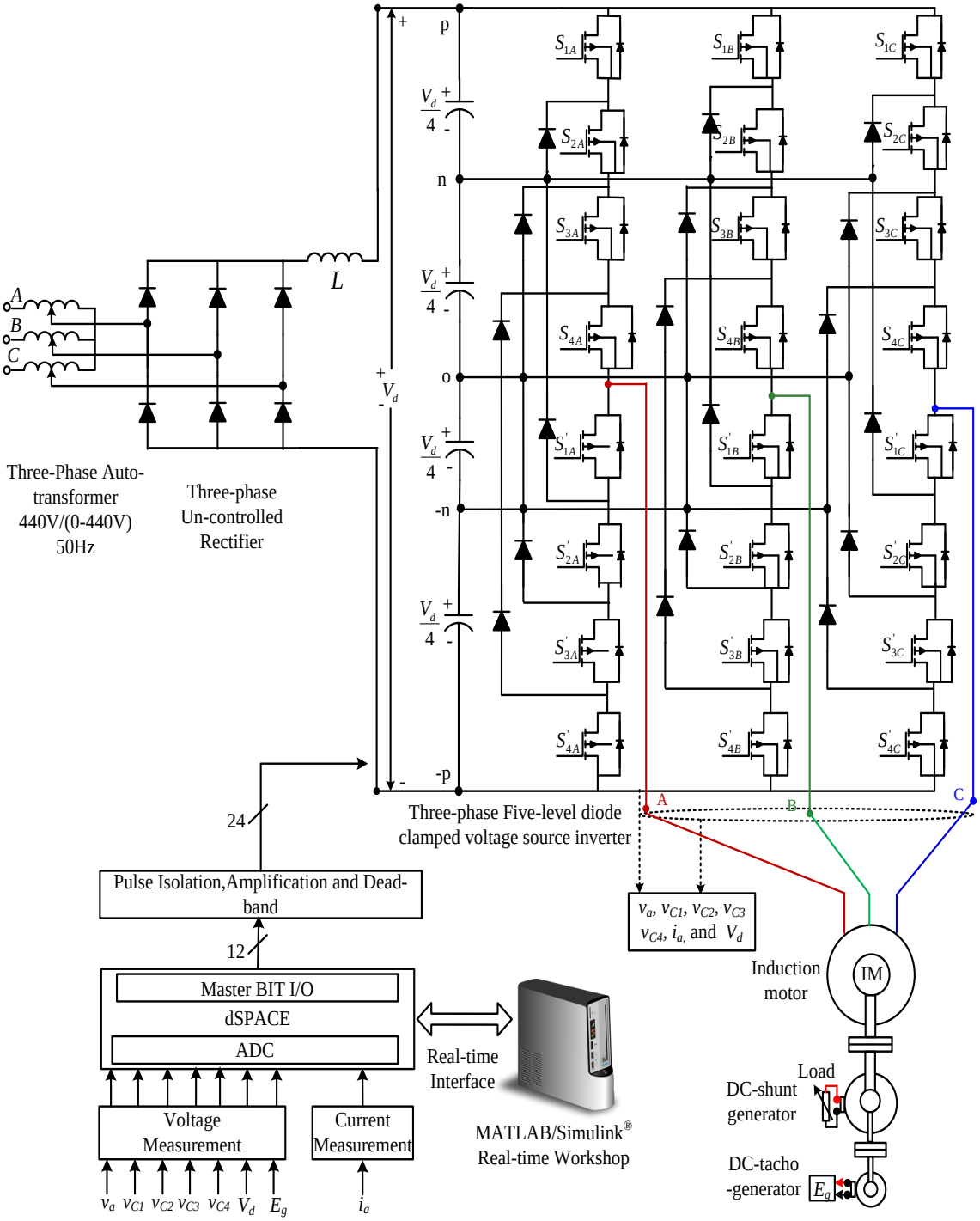


Fig. 6.3: Schematic diagram for hardware implementation of DTC using FLDCI

Here, phase currents and phase voltages, DC-link voltages (v_{c1}, v_{c2}, v_{c3}, and v_{c4}), and total DC-tacho-generator voltage E_g, are enough to implement FLDCI and are sensed through the respective sensors and then connected to the ADC-channels of the dSPACE controller.The complete schematic diagram for the realization of two-level VSI, TLDCI and FLDCI are shown in Fig. 6.1, Fig. 6.2 and Fig. 6.3, respectively.

For the development of the power circuit, the power MOSFETs (SPW47N60C3) of rating 650V/47A has been used as the switching devices for realizing the two-level VSI, TLDCI and FLDCI. The other hardware components required for the operation of the experimental set-up such as pulse amplification circuit, isolation circuit, dead-band circuit, voltage and current sensor circuits, non-linear/reactive loads have been designed and developed in the laboratory. A Digital Signal Processor (DSP) DS1104 of dSPACE has been used for the real-time implementation of control algorithms. By using the Real-Time Workshop (RTW) of MATLAB and Real-Time Interface (RTI) feature of dSPACE–DS1104, the simulink models of the various controllers of the prototypes have been implemented. The control algorithm is first designed in the MATLAB/Simulink software. The RTW of MATLAB generates the optimized C-code for real-time implementation. The interface between MATLAB/Simulink and Digital Signal Processor (DSP, DS1104 of dSPACE) allows the control algorithm to be executed on the hardware. The master bit I/O is used to generate the required gate pulses and Analog to Digital Converters (ADCs) are used to interface the sensed inverter modules, voltage and current, inverter current, load current, grid voltage and DC-bus capacitor voltages. The development of different hardware components as required for the operation of the hardware prototypes are discussed in the next section.

6.2 Development of System Hardware

The developed experimental prototype is comprised of the following parts:

1. Power circuit for two-level, three-level, and five- level inverter for DTC
2. Measurement circuits
   - IM phase currents
   - DC link voltages of the inverter and phase voltages of the IM
   - IM speed measurement using DC-tacho-generator
3. Development of System software
4. Control hardware

- MOSFET driver circuit for Isolation and Amplification
- Dead-band circuit

6.2.1 Development of Power Circuit

A three-phase two-level VSI, TLDCI and FLDCI with suitably designed filter inductor (L) on its DC side have been developed in the laboratory and are discussed in the previous Section 6.1 in detail. The self-commutated power semiconductor switches required for the development of the inverter are realized by the MOSFETs (SPW47N60C3). To protect each switching device, a suitably designed snubber circuit is connected across it. The snubber comprises of a parallel combination of a resistor and a capacitor connected across a Metal-Oxide Varistor (MOV). The devices are mounted on heat sinks to ensure proper heat dissipation. Various parameters used in different control strategies are mentioned in Appendix. A4 along with their ratings.

6.2.2 Measurement Circuits

For the precise and reliable operation of a system in closed loop, measurement of various system parameters and their conditioning is required. The measurement system must fulfil the following requirements:

- High accuracy
- Galvanic isolation with power circuit
- Linearity and fast response
- Ease of installation and operation

With the availability of Hall-effect current sensors and isolation amplifiers, these requirements are fulfilled to a large extent. In order to implement the control algorithm of the IM drive system in closed loop, following signals have been sensed.

1. IM phase currents
2. DC link voltages of the inverter and phase voltages of the IM
3. IM speed measurement using DC-tacho-generator

6.2.2.1 Sensing of AC Current

The inverter module output current and AC source currents have been sensed using the PCB-mounted Hall-effect current sensors (TELCON HTP50). The HTP50 is a closed loop

Hall effect current transformer suitable for measuring currents up to 50 A. This device provides an output current into an external load resistance. These current sensors provide the galvanic isolation between the high voltage power circuit and the low voltage control circuit and require a nominal supply voltage of the range ±12V to ±15V. It has a transformation ratio of 1000:1 and thus, its output is scaled properly to obtain the desired value of measurement. The circuit diagram of the current sensing scheme is shown in Fig.6.4.

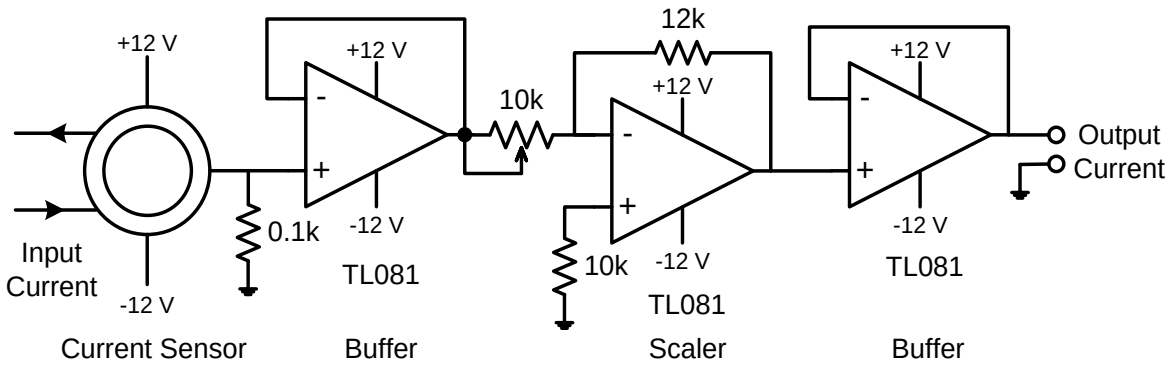


Fig. 6.4: AC current sensing circuit.

6.2.2.2 Sensing of AC/DC Voltage

The voltages are normally sensed using isolation amplifiers and among them, AD202 is a general purpose, two-port, transformer-coupled isolation amplifier that can be used for measuring both AC and DC voltages. The other main features of the AD202 isolation amplifier are:

1. Small physical size
2. High accuracy
3. Low power consumption
4. Wide bandwidth
5. Excellent common-mode performance

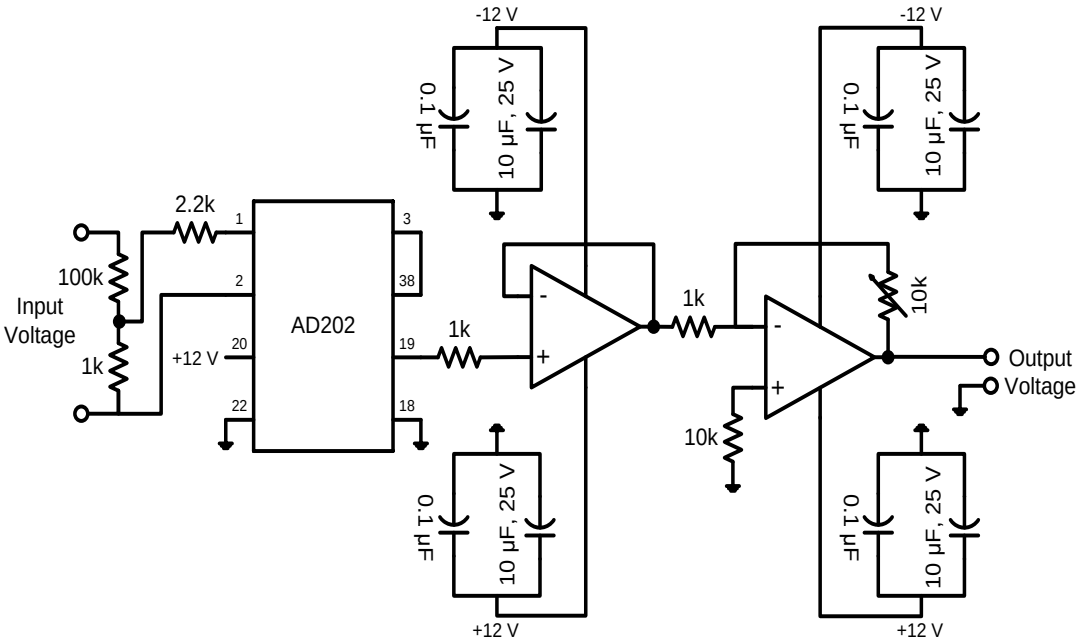


Fig. 6.5: AC/DC voltage sensing circuit.

This voltage sensor can sense voltages in the range of ±1 kV (peak) and it requires a nominal supply voltage range of ±12V to ±15V. Fig. 6. shows the circuit diagram for the voltage sensing scheme, which uses AD202 isolation amplifier. The voltage (AC or DC) to be sensed is applied between the terminals 1 and 2 (across a voltage divider comprising of 100 kΩ and 1 kΩ) and the voltage input to the sensor is available at the pins 1 and 2 of AD202 via a resistance of 2.2 kΩ. The isolated sensed voltage is available at the output terminal 19 of AD202. The output of voltage sensor is scaled properly to meet the requirement of the control circuit and is fed to the dSPACE via its ADC channel for further processing.

6.2.2.3 Sensing speed of the IM

Here, the speed of the IM is sensed with the help of DC-Tacho-generator, which is coupled to the rotor shaft of the IM. Here, the DC-Tacho-generator behaves like a DC-shunt generator. Therefore, the speed of the IM is directly proportional to the generated DC-voltage (E_g) of the DC-Tacho-generator. This DC-voltage is again sensed with the voltage sensor and is fed to the dSPACE via its ADC channel for further processing.

6.2.3 Development of System Software

Historically, control software was developed using assembly language. In recent years, industry began to adopt MATLAB/Simulink and Real-Time Workshop (RTW) platform

based method, which provides a more systematic way to develop control software. Fig.6.6 shows the Total Development Environment (TDE) of dSPACE and its major component blocks are explained as below:

- MATLAB is widely used as an interactive tool for modeling, analysis and visualization of systems, which itself contains more than 600 mathematical functions and supports additional toolboxes to make it more comprehensive.
- Simulink is a MATLAB add-on software that enables block diagram based modelling and analysis of linear, nonlinear, discrete, continuous, and hybrid systems.
- RTW is Simulink add-on software that enables automatic C-code generation from the Simulink model. The generated optimized code can be executed on PC, microcontrollers, and signal processors.

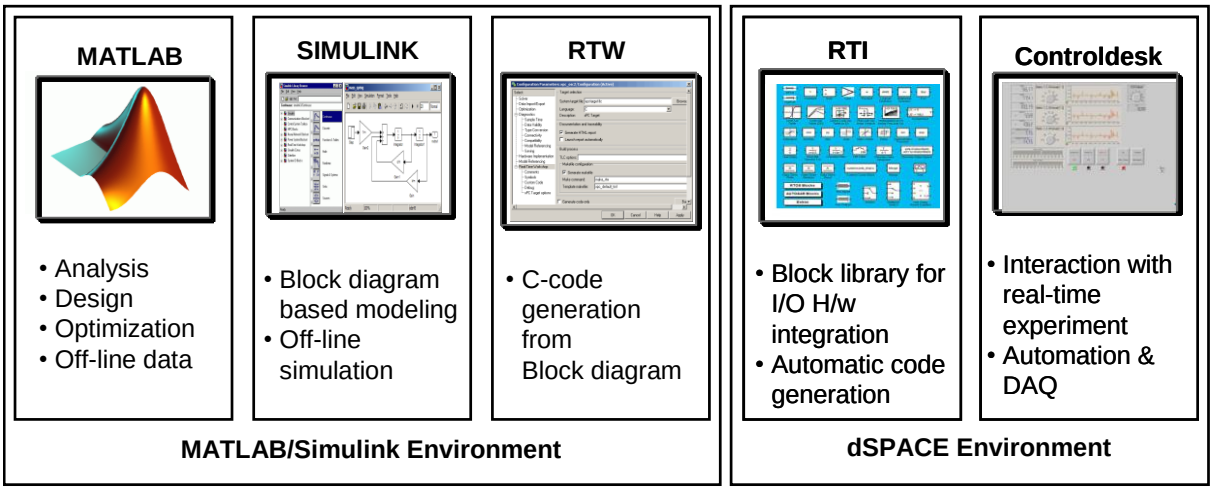


Fig.6.6: Total Development Environment of dSPACE with MATLAB.

- Real Time Interface (RTI) is add-on software of dSPACE which provides block libraries for I/O hardware integration of DS1104 R&D controller and generates optimized code for master and slave processors of the board.
- dSPACE's control desk is a software tool interfacing with real-time experimental setup and provides easy and flexible analysis, visualization, data acquisition and automation of the experimental setup. The major feature of real-time simulation is that the simulation is carried out as quickly as the real system would actually run, thus allowing to combine the simulation and the inverter (real plant).

The DSP DS1104 R&D controller board of dSPACE is a standard board that can be plugged into Peripheral Component Interconnect (PCI) slot of a desktop computer. The

DS1104 is specially designed for the development of high-speed multivariable digital controllers and real-time simulations for various applications. It is a complete real-time control system based on an AMD Opteron™ processor running at 2.6 GHz. It has 256 MB DDR-400 SDRAM local memory for the application and dynamic application data and 128 MB SDR SDRAM global memory for host data exchange. DS1104 R&D controller is a very good platform for the development of dSPACE prototype system for cost-sensitive RCP applications. It is used for the real-time simulation and implementation of the control algorithm in real-time.

Table 6.1: Number of I/Os and ADCs required for two, three, and five-level inverter

Topology	**No. of Master bit I/Os**		**No. of ADCs**	
Two level VSI fed DTC of IM drive	3	**3:** For giving gate pulses to **two level VSI**	8	Currents of the IM (3), Phase voltage of the IM (3), Speed measurement (1), DC-link voltage(1)
TLDCI fed DTC of IM drive	6	**6:** For giving gate pulses to **TLDCI**	8	Currents of the IM (3), Phase voltage of the IM (3), Speed measurement (1), DC-link voltage(1)
FLDCI fed DTC of IM drive	12	**12**: For giving gate pulses to FLDCI	8	Currents of the IM (1), Phase voltage of the IM (1), Speed measurement (1), DC-link voltages(4)

The sensed AC and DC voltages are fed to the dSPACE Multi-I/O Board (DS2201) of DS1104 via the available ADC channels on its connector panel. In order to add an I/O block (such as ADCs and master bit I/Os in this case) to the Simulink model, the required block is dragged from the dSPACE I/O library and dropped into the Simulink model of DTC. In fact, adding a dSPACE I/O block to a Simulink model is almost like adding any Simulink block to the model. The master bit I/Os configured in the output mode are connected to the model for providing a gate pulse signal to the switching devices of the MOSFETs. In addition to that, ADCs are connected to the model for giving different sensed parameter as input to the DSP hardware. The number of master bit I/Os and ADCs required for the three abovementioned topologies of DTC system are given in Table.6.1

The sensed signals of each topology are used for processing in the designed control algorithm. The vital aspect for real-time implementation is the generation of real-time code of the controller to link the host computer with the hardware. For dSPACE systems, Real-Time Interface (RTI) carries out this linking function. Together with RTW from the Mathworks®, it automatically generates the real-time code from Simulink models and implements this code on the dSPACE real-time hardware. This saves the time and effort considerably as there is no need to manually convert the Simulink model into another language such as 'C'. RTI carries out the necessary steps needing only addition of the required dSPACE blocks (I/O interfaces) to the Simulink model. In other words, RTI is the interface between Simulink and various dSPACE platforms. It is basically the implementation software for single-board hardware and connects the Simulink control models to the I/O of the board. In the present case, the optimized C-code of the Simulink model of the control algorithm is automatically generated by the RTW of MATLAB in conjunction with RTI of dSPACE.

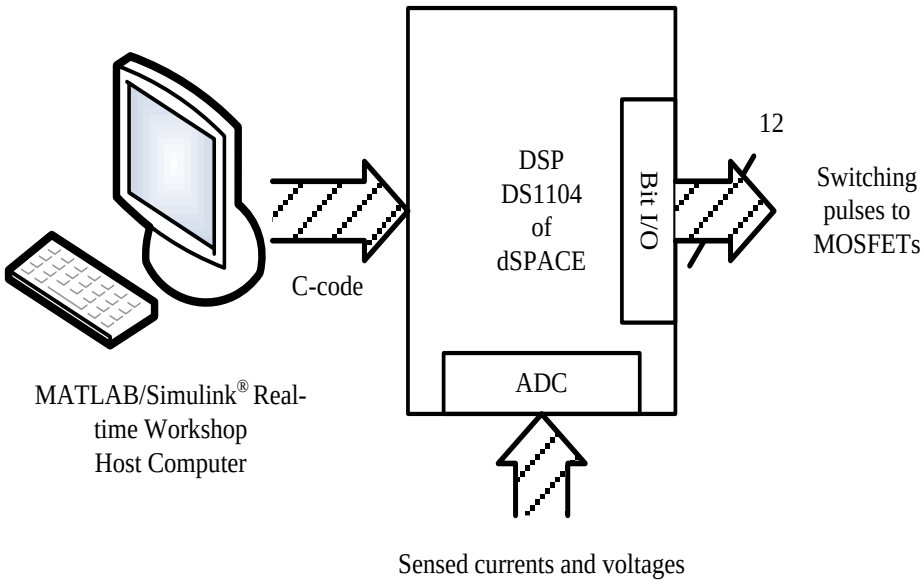


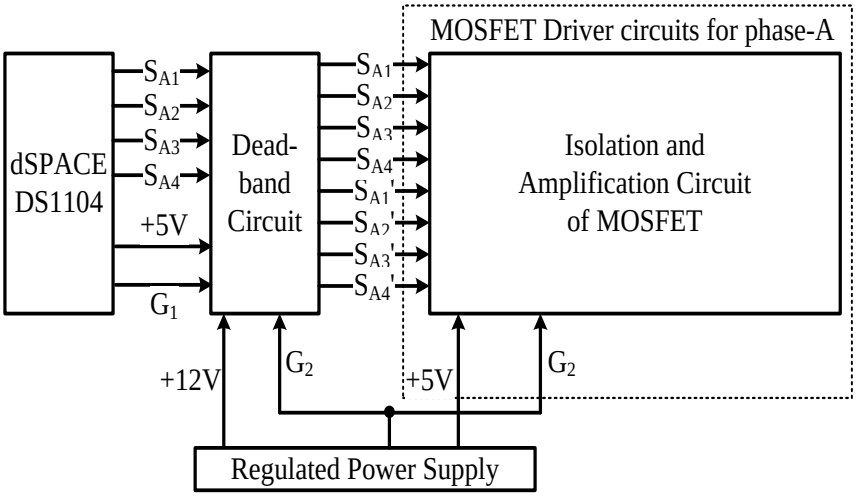
Fig. 6.7: DSP (dSPACE-DS1104) circuit board interfacing.

The generated code is then automatically downloaded into the dSPACE hardware where it is implemented in real-time and the gating signals are generated. The gating pulses for the power switches of the converter are issued via the Master-bit I/Os available on the dSPACE board. The DS2201 Connector/LED combo panel provides easy-to-use connections between DS1104 board and the devices to be connected to it. The panel also provides an array of LEDs indicating the states of digital signals (gating pulses). The

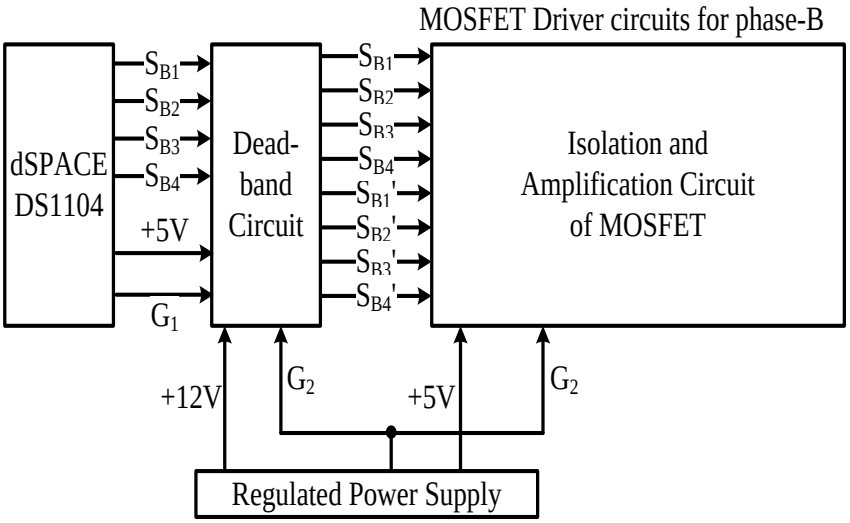
gating pulses are fed to various power devices driver circuits via dead-band and isolation circuits. Fig. 6.7 shows the schematic diagram of dSPACE-DS1104 board interfaced with the host computer and the real-world plant (power circuit of the DTC). Sensed signals are fed to the ADCs and generated gating pulses are given at Master bit I/Os.

6.2.4 Development of Control Hardware

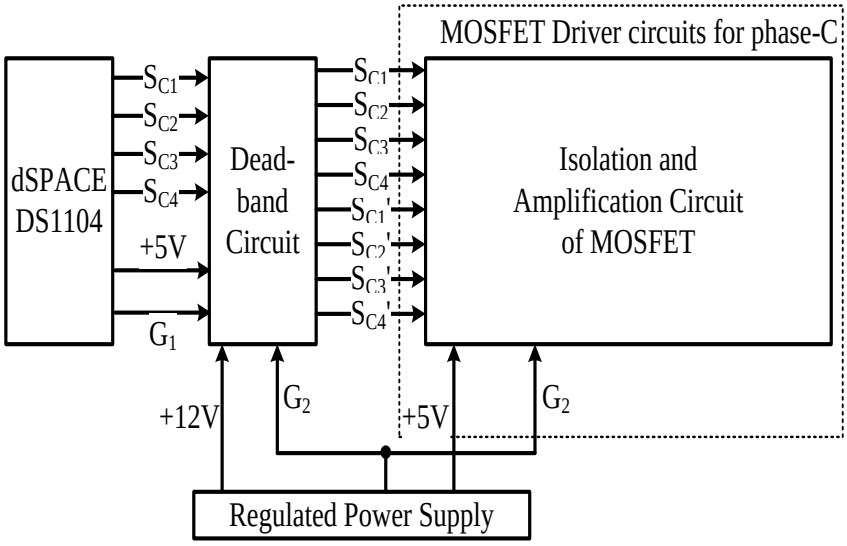
The control algorithm is designed and built into the MATLAB/Simulink software and the control pulses for the power switches of two-level VSI, TLDCI and FLDCI are generated by real-time simulation using the dSPACE control.



(a) Phase-A driver circuit



(b) Phase-B driver circuit



(c) Phase-C driver circuit

Fig. 6.8: Schematic diagram for providing firing pulses from dSPACE controller board to switching devices

The optimized C-code of the Simulink model of control algorithm is generated with the help of Real-Time Workshop (RTW) of MATLAB. The RTW of MATLAB and the Real-Time Interface (RTI) of dSPACE result in the real-time simulation of the model. The control pulses are generated at the various Master-bit I/Os of the dSPACE which are interfaced with the MOSFET driver circuits through isolation and dead-band circuits. This ensures the necessary isolation of the dSPACE hardware from the power circuit that is required for its protection. Fig. 6.8 shows the basic schematic diagram of interfacing firing pulses from the dSPACE board to switching devices of the three phases of the inverter. From Fig.. 6.8, it can be observed that the following hardware circuits are required for interfacing of FLDCI with dSPACE board.

1. Dead-band circuit
2. MOSFET driver circuits for isolation and amplification
3. Regulated Power Supplies

6.2.4.1 Dead-band Circuit

A dead-band (dead-time or delay) circuit is employed to provide a delay time (of about 1 μs) between the switching pulses to two complementary devices connected in the same leg of an inverter.

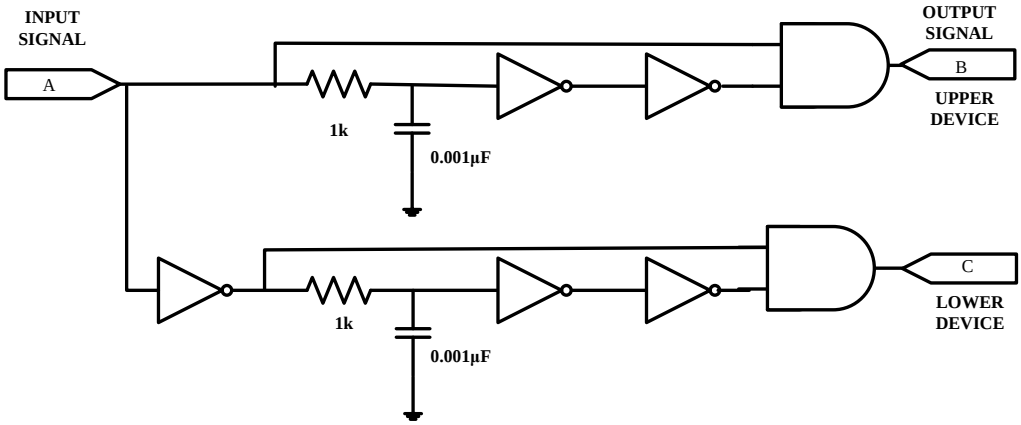
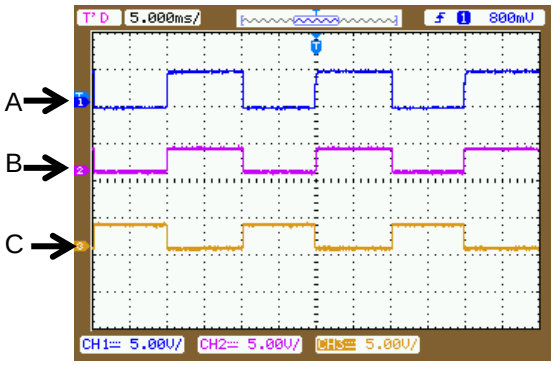
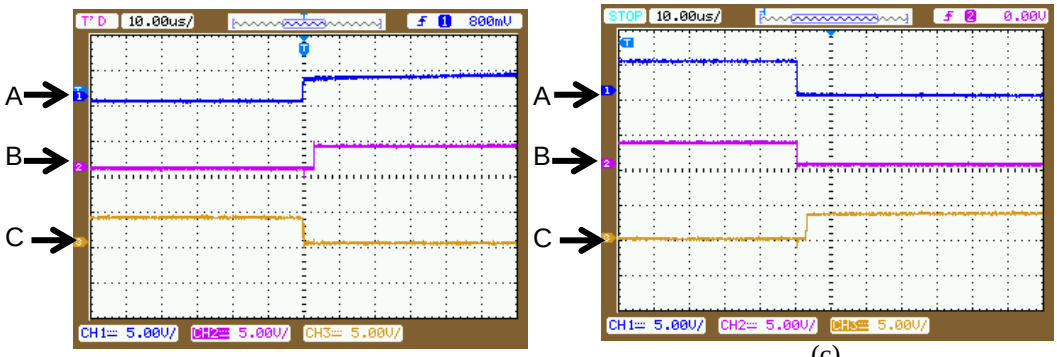


Fig.6.9: Dead-band circuit for single-leg of an inverter.



(a)



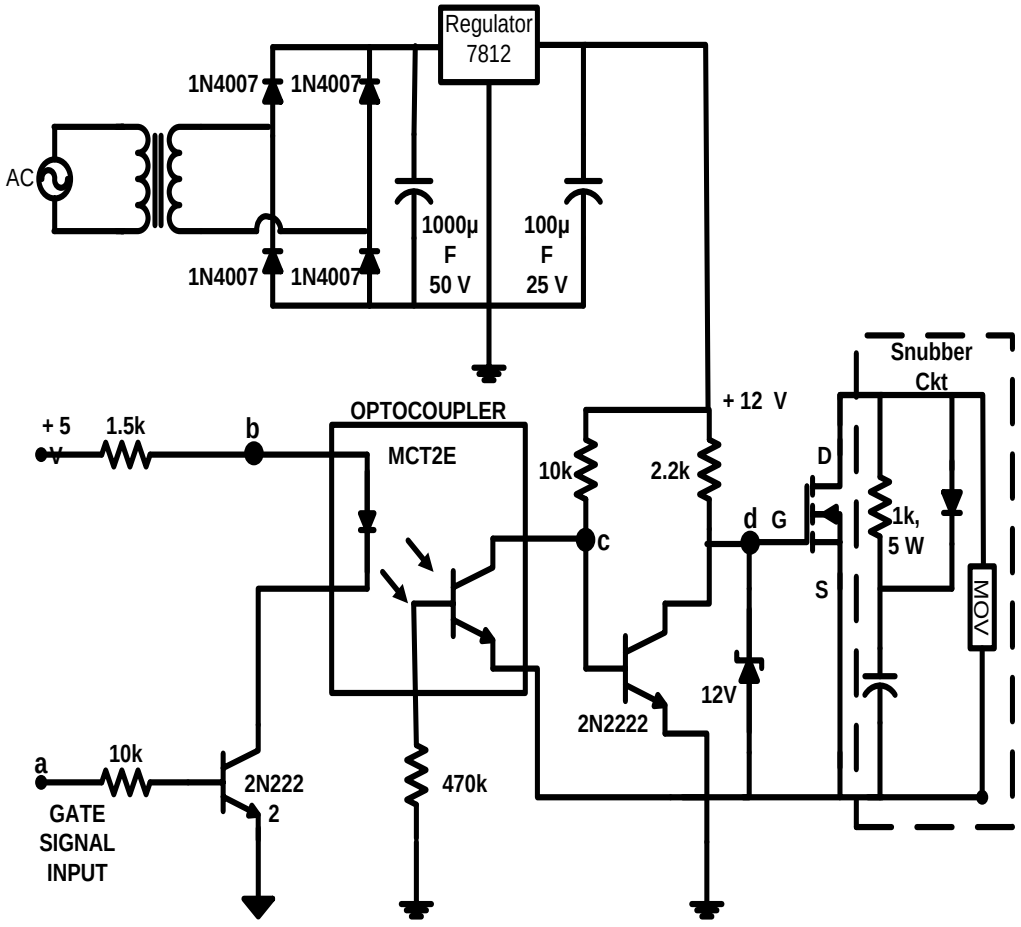
(b) (c)

Fig. 6.10: Firing signals for the switches S_{11} and S_{12} with dead-band circuit.

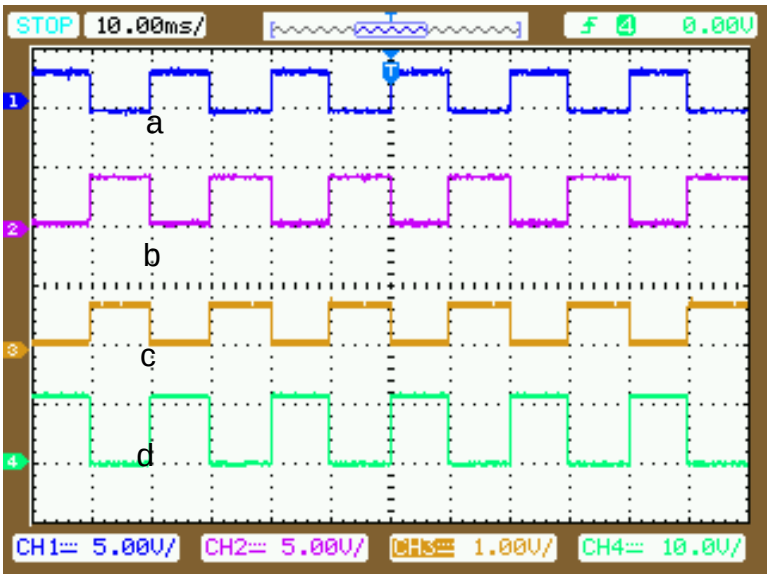
This is required to avoid the short circuit of devices in the same leg due to simultaneous conduction. The delay time between switches of the same leg of the inverter is introduced by an *RC* integrator circuit as shown in Fig.6.. An identical dead-band circuit has been used for each leg of the complementary switching devices. The different switching signals obtained experimentally for semiconductor devices in the same leg of an inverter are shown in Fig. 6.10(a) with a 1 µs delay. The switching delays for the upper and lower switches in same leg are shown in a clearer way in Fig. 6.10 (b) and Fig. 6.10 (c) respectively.

6.2.4.2 MOSFET Driver Circuits

The MOSFET driver circuits are used for pulse amplification and isolation purposes. The control pulses generated from dSPACE unit are not efficient to drive the switching devices. Thus, these signals are further amplified by using proper amplifier circuit. Fig. 6.11(a) shows a circuit diagram of pulse isolation and amplifier circuit for MOSFET driver circuit. For isolation between power circuit and a control circuit, an opto-coupler (MCT2E) is used. Although common + 5V, regulated DC power supply is used at the input side of the optocoupler, but individual regulated DC power supplies of +12V are used to connect the output side of optocoupler. In order to test the MOSFET driver, a PWM signal is applied at point 'a' of Fig. 6.11(a) and waveforms at different points (a, b, c and d) are recorded as shown in Fig. 6.11(b). It is observed that the waveform at point 'd' is similar to the PWM signal applied at point 'a', but its amplitude is increased to 12V which is used to drive the MOSFET.



(a) MOSFET driver circuit for isolation and amplification

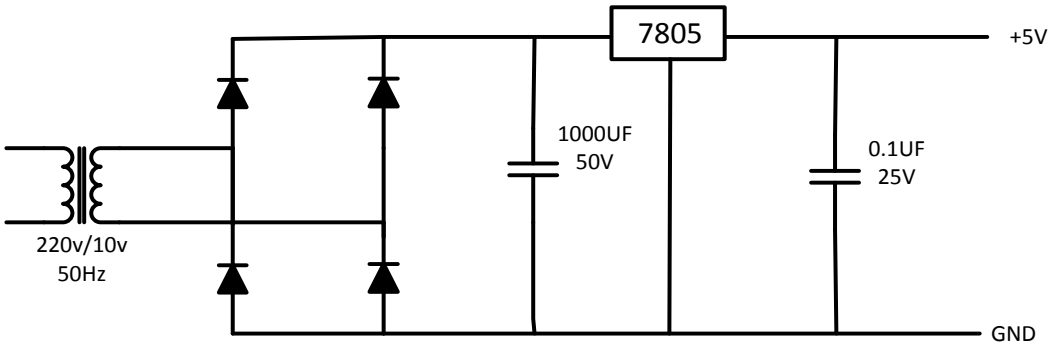


(b) Waveform at different points

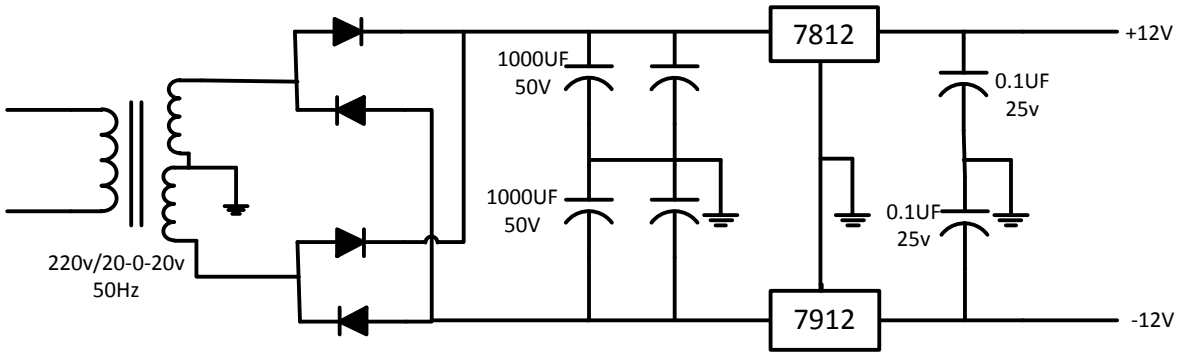
Fig. 6.11: MOSFET driver circuit and respective wave forms at different positions

6.2.4.3 Regulated Power Supplies

DC regulated supplies (+12v gnd -12v, +5v) are required for providing biasing to various circuits like pulse amplification and isolation circuits, hysteresis controller and voltage detectors etc. using IC's 7812 for +12v, IC 7912 for -12v and 7805 for +5 v. The circuit diagram of the power supplies is as shown in following Fig. 6.12 (a) and (b).



(a) Connection diagram for +5V power supply



(b) Connection diagram for -12 and+12v power supply

Fig. 6.12 Connection diagram for power supplies

Instead of using individual transformers a single multi-winding transformer (220V/20-0-20V-1A, 10V-1A, 10V-1A) is used for the power supplies. Here two 10V secondaries are used to give two +5v supplies separately; one for the switches and other for the control circuit.

6.5 Conclusion

In this chapter, the various components developed for the hradware implementation of DTC using two-level VSI, TLDCI, and FLDCI are discussed. An assortment of circuits for power, measurement and control circuitry are shown and explained as well. Moreover, the interfacing of the dSPACE DS-1104 between real time and Matalb is discussed in detail. Also, the control desk features are explained well for conducting the experiment.

CHAPTER - 7
CONCLUSIONS

7.1 General

The first part of this thesis refers to the review of soft computing based techniques, PWM techniques, and multilevel inverters. In addition, the development of type-1 and type-2 fuzzy controllers is discussed. Subsequently, the modeling and simulation of direct torque controlled induction motor drive using proportional integral, type-1 fuzzy, and type-2 fuzzy controllers are also discussed. Further, the modeling and simulation for direct torque control of IM drive is extended for the different topologies of the inverter such as two-level, three-level and five-level inverters. The simulated performance of the IM drive for the various combinations of control schemes and inverter topologies has been validated on prototype with the dSPACE DS-1104 controller. The performance of the IM drive is simulated, compared, and verified with the experimental setup using the dSPACE DS1104 for a two-level, three-level and five-level voltage source inverter fed IM drive in which it consists of the proportional integral DTC, type-1 fuzzy DTC and type-2 fuzzy DTC schemes.

7.2 Concluding Remarks

Due to the development of improved inverter topologies, semiconductor technologies and control methods for adjustable speed drives have become the preferred choice in industrial applications. Out of the various adjustable speed drives, IM drives are most widely used. Voltage source inverters are proven as standard configuration for PWM inverter drives compared to current source inverters. In order to control the VSI various PWM techniques are proposed. Out of the various techniques, space vector modulation (SVM) has grown as popular pulse width modulation method for voltage fed inverter AC drives because it not only reduces the harmonic content and also offers significant flexibility to optimize switching waveforms as compared to other modulation techniques.

Two-level inverter: The IM drive is simulated in the Matlab environment for two-level voltage source inverter using proportional integral direct torque control, type-1 fuzzy DTC and type-2 fuzzy DTC. The proportional integral direct torque control provides considerable flux and torque ripples at and above 0.5 modulation index as SVM provides more RMS flux ripples. Moreover, it has the poor dynamic performance of the IM drive due to the poor performance of PI-controllers. The performance of proportional integral DTC of IM drive is largely influenced by the type of speed and torque controllers in use. Usually, proportional-integral controllers are used due to its simplicity. But the tuning of electric drive controller is a complex problem due to the non-linearity of the machines, power converter and controller. Due to this, the conventional PI controller does not operate satisfactorily when the operating point changes. Therefore, it is felt that control techniques should be intelligent to increase the effectiveness of control strategies. An intelligent control system is expected to possess inbuilt adaptation or learning and decision making capability and hence it is able to meet desired performance over a very wide range of speed and uncertainty in the operating parameters.

The ripples in flux, current, and torque of the IM drive with type-1 fuzzy DTC are improved using either duty ratio control or hybrid space vector modulation control. The duty ratio control of SVM is independent of the sampling time and with type-1 fuzzy control improves the firing strength of the inverter. However, hybrid space vector modulation uses two complementary bus-clamped sequences along with the SVM sequence in each sector to reduce RMS flux ripple of the IM. Consequently, the current and torque ripples of IM drive is improved significantly than proportional integral DTC. In order to improve the dynamic performance of the IM drive than proportional integral DTC, the T1FDTC is used in which the speed and torque PI-controllers are replaced by type-1 fuzzy controllers (T1FCs). The T1FC uses Mamdani type and Centroid method with simple IF and THEN rules without need of very big complex equations. Moreover, the T1FLC effectively handles the non-linear system based on decision taken by the expertise via pre-learned algorithm than the PI-controllers. To further improve the ripple as well as the dynamic performance of the IM drive than the type-1 fuzzy DTC, the type-2 fuzzy DTC is also used. As the T2FC has three-dimensional control with type reduction in defuzzification process to effectively deal with the huge ambiguous data (larger footprint of uncertainty) than T1FC. To a large extent, the drawbacks of pertaining to this scheme seem to be complementary. Therefore, it seems natural to consider building an

integrated system combining the concepts of T1FC modeling and reduced type-2 fuzzy set.

A comparative simulated performance of the direct torque control of IM drive during startup, a step change in the speed, and load perturbation is presented for proportional integral DTC, type-1 fuzzy DTC with duty ratio control, type-1 fuzzy DTC with hybrid space vector modulation, type-2 fuzzy DTC with duty ratio control, and type-2 fuzzy DTC with hybrid space vector modulation. However, the type-2 fuzzy DTC along with hybrid space vector modulation provides less voltage THD, current THD, flux and torque distortion, and significant improvement in the overall efficiency of the IM drive than the other control schemes (proportional integral DTC, type-1 fuzzy DTC with duty ratio control, type-2 fuzzy DTC with hybrid space vector modulation, and type-2 fuzzy DTC with duty ratio control). In addition, the dynamic response of the IM drive for type-2 fuzzy DTC with hybrid space vector modulation is further improved significantly at all modes of the operation.

A prototype controller is developed in the laboratory using the same rating and parameters of the machine as used in the simulation. The control signals for the above control schemes are generated by the dSPACE DS-1104 controller. The simulated results of the above control schemes are validated with the experimental results under the same operating conditions. It is concluded for two-level VSI fed direct torque control of IM drive that the type-2 fuzzy DTC along with hybrid space vector modulation provides fewer flux ripples, less torque distortion, less voltage and current THD, and significant improvement in overall efficiency with fast dynamic performance of the IM drive than type-2 fuzzy DTC with duty ratio control, type-1 fuzzy DTC with hybrid space vector modulation, type-1 fuzzy DTC with duty ratio control and proportional integral DTC.

Three-level inverter: To further improve the voltage and current profile, torque and flux ripples, and dynamic performance of the IM drive the three-level inverters are used instead of two-level voltage source inverter. Here, the three-level diode clamped topology is chosen for investigation because increasing popularity in industrial application due to its simple control than the other topologies. A simplified SVM method that divides the space vector diagram of three-level inverter into space vector diagram of two-level inverter is used. The developed two-level VSI for conventional PI, type-1 and type-2 fuzzy based DTC are used in this three-level SVM. The IM drive is simulated in the Matlab environment for three-level diode clamped VSI using proportional integral DTC, type-1 fuzzy DTC and type-2 fuzzy DTC. In addition, the voltages across the DC-link

capacitors for different switching states such as zero, small, medium and large voltage vectors are analyzed. Moreover, in particular for three-level inverter the constant voltage across the DC-link capacitors is provided by operating or selecting an appropriate switching vector in all three control schemes without need of any extra PI-controller. The simulated response for three-level inverter of the IM drive is also validated with the dSPACE DS-1104 controller using same machine parameters as used in the simulation. It is concluded for three-level diode clamped VSI that the type-2 fuzzy DTC provides fewer flux ripples, less torque distortion, less voltage and current THD, and more overall efficiency of the IM drive with fast dynamic performance than type-1 fuzzy DTC and proportional integral DTC.

Five-level: Finally, the five-level diode clamped VSI fed IM drive is used to further improve the ripple and overall efficiency of the IM drive than two-level and three-level VSI. The control schemes such as PI, type-1 fuzzy and type-2 fuzzy remains the same as used in two and three-level VSI fed direct torque control of IM. In all three control schemes, the voltage across the DC-link capacitors is balanced on the basis of minimum energy principle in which the sum of the energy provided by all capacitors is minimum or zero as compared to the other switching state of the vector. Hence, the voltages across the DC-link capacitors maintained constant by operating or selecting an appropriate switching vector in all three control schemes without need of any extra PI-controllers. The simulated results of the IM drive for five-level diode clamped inverter using above control schemes are compared and validated with the experimental setup for the same parameters as used in the simulation. It is concluded that the type-2 fuzzy DTC along with five-level inverter provides fewer flux ripples, less torque distortion, less voltage and current THD, and highest overall efficiency with fast dynamic performance of the IM drive than two-level and three-level inverter.

7.3 Scope for future work

The important conclusions listed in this chapter have also given rise to the following aspects, which may be taken up for further exploration of the potential of inverter fed IM drive

1. The proposed type-2 fuzzy based DTC using SVM can be extended to over modulation region and higher inverter levels as well.
2. The speed of the IM can also be controlled and implemented for proportional integral DTC using single voltage and current sensors without requiring any speed sensor, i.e., Tacho-generator, encoder, etc. Therefore the total cost of the IM drive is reduced significantly.
3. The magnetic saturation effect is significant at motor startup and near rated operating conditions. Under saturated operation, the voltage and current harmonics generated by the IM become appreciable. These can alter the static and dynamic performance of the IM drives. In this thesis, the saturation effect has not been considered in the analytical model. The saturation effect may also be included in the analytical model.
4. Control and estimation strategies for IM drives are based on the equivalent circuit model of the motor. The frequency dependence of the rotor electrical circuit, non linearity of the magnetic circuit and temperature dependency of the stator and rotor electrical circuits have an impact on the accuracy of the motor model. Therefore, the effect of parameter sensitivity can also be included in the vector control scheme with the proposed SVM method.
5. Practical implementation of multilevel inverters for high power application is still an issue because it involves complexity in control. Intensive research needs to be done on developing the multilevel inverters with reduced number of components.
6. The type-2 Neuro-fuzzy control can be used instead of type-2 fuzzy control to improve the controller performance. To further improve dynamic response, DTC in both two-level and multi-level inverters can be done.
7. As similar to the two-level inverter, a Hybrid PWM can also be developed, simulated and implemented for proportional integral DTC in both three and five level inverter to further improve the torque and flux ripple performance of the IM drive.

PUBLICATIONS FROM THE WORK

Published or Accepted or Revised:

International Journals:

1. N. Venkataramana Naik and S. P. Singh, "Improved Torque and Flux performance of Type-2 Fuzzy Based DTC IM Using Space Vector Pulse-width Modulation," *Electric Power Components and System,* vol. 42, pp. 658-669, Mar. 2014.
2. N. Venkataramana Naik and S. P. Singh, "A Comparative Analytical Performance of Fuzzy-2 DTC and proportional integral DTC of IM Using DSPACE DS-1104," *IEEE Transactions on Industrial Electronics,* vol. pp. Aug. 2015.
3. N. Venkataramana Naik and S. P. Singh, "A Three-Level Fuzzy-2 DTC of IM Drive Using SVPWM," **Accepted** for the publication in *IEEE Transactions on Industrial Electronics*, Nov. 2015.
4. N. Venkataramana Naik and S. P. Singh, "A Fuzzy Direct Torque Control of IM Drive Using Bus-Clamped Space Vector Modulation," **Accepted** for the publication in *International Journal of IETE Technical Review*.
5. N. Venkataramana Naik and S. P. Singh, "Improved Torque and Flux Performance of PI DTC IM Drive using Three-Level SVPWM over a Two-level," **Accept with change** in *International Journal Electronics,* Aug. 2015.
6. N. Venkataramana Naik and S. P. Singh, "A Closed Loop Stability Analysis for F2DTC of Induction Motor Using Three-Level SVPWM," **Minor revision in** *ISA Transactions, Elsevier,* July. 2015.
7. N. Venkataramana Naik and S. P. Singh, "A Two-Level Fuzzy Based DTC Using PLL Control to Improve the IM Performance," **Major revision in** *Electric Power Components and System,* Jan. 2015.
8. N. Venkataramana Naik and S. P. Singh, "A Five-Level Fuzzy-2 DTC of IM Drive Using SVPWM," **Major revision** in *IEEE Transactions on Industrial Electronics*, Aug. 2015.

List of IEEE International Conferences

9. N. Venkataramana Naik and S. P. Singh, "Improved Dynamic Performance of Direct Torque Control at low speed over a scalar control," *IEEE Conf .Proc. INDICON-14 at IIT Bombay*, pp. 1-5, Dec. 2014.
10. N. Venkataramana Naik and S. P. Singh, "Improved Dynamic Performance of Fuzzy Based DTC IM Using Bus-Clamped SVM," *IEEE Conf. Proc. IICPE-12 at Delhi University*, pp. 1-6, Dec. 2013.
11. N. Venkataramana Naik and S. P. Singh, "A Novel Type-2 fuzzy Logic Control of IM Drive Using Scalar Control," *IEEE Conf. Proc. in IICPE-12 at* Delhi University, Dec. 2013.
12. N. Venkataramana Naik and S. P. Singh, "A Novel Type-2 fuzzy Logic Control of IM Drive using Space Vector PWM," *IEEE Conf. Proc. INDICON-12*, Kochi, pp. 1142-1147, Dec. 2013.
13. N. Venkataramana Naik and S. P. Singh, "Improved Dynamic Performance of Type-2 Fuzzy Based DTC IM Using SVPWM," *IEEE Conf. Proc. PEDES-12 at IISc Banglore*, pp. 1-5, Dec. 2013.
14. N. Venkataramana Naik and S. P. Singh, "A Comparative Study of *V/f* Controlled IM Using Two and Three Level Bus Clamped SVM," *International IEEE Conf, IICPE -14 at NIT Kurukshetra*, pp. 1-5, Dec. 2014.
15. N. Venkataramana Naik and S. P. Singh, "A NF Based Direct Torque Control of IM Drive Using BCSVM," *International IEEE Conf, IICPE -14, NIT Kurukshetra*, Dec. 2014.

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APPENDIX-1

This appendix consists of the induction motor drive parameters and the screenshots of the MATLAB/Simulink models for the DTC using two-level inverter.

PARAMETERS OF IM DRIVE FOR TWO-LEVEL INVERTER

S. No.	Parameters	2HP rating
1	Rated supply voltage (V_{L-L})	440V (L-L)
2	Power rating (P_o)	2HP
3	Rated speed (N_r)	1460 rpm
4	Number of poles	4
5	Stator resistance (R_s)	7.83Ω
6	Rotor resistance (R_r)	7.55 Ω
7	Stator leakage inductance (L_s)	0.4751H
8	Rotor leakage inductance (L_r)	0.4751H
9	Mutual inductance (L_m)	0.4535H
10	Moment of inertia (J)	0.06Kg-m^2
11	Diodes	1000V/40A
12	Four DC-Link capacitors ($C_1 = C_2$)	2200μF/450V
13	MOSFETs (SPW47N60C3)	650V/45A
14	Speed PI-control (k_{ps} and k_i)	20 and 150
15	Torque PI-control (k_{pt} and k_{it})	30 and 2
16	Flux control (k_{pf} and k_{if})	10 and 5
16	Voltage sensors (AD2OKY)	1000V
17	Current sensors (Telcon-HTP50)	50A
18	DC-Tacho-generator (RADIO ENGINE)	90V/3000rpm
19	Dead Band for two schemes	10μs
20	Sampling Time	40μs

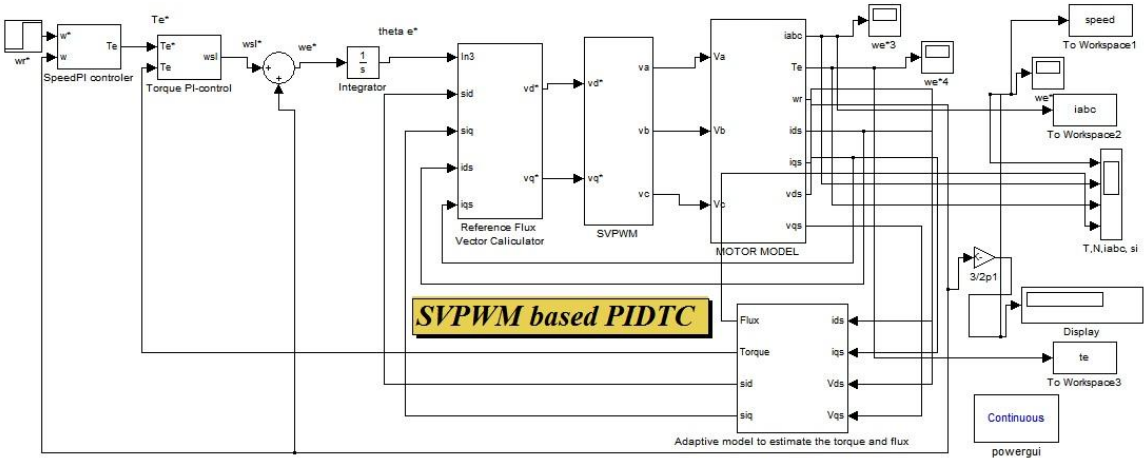

Fig. A. 1.1: PIDTC of induction motor for two-level inverter

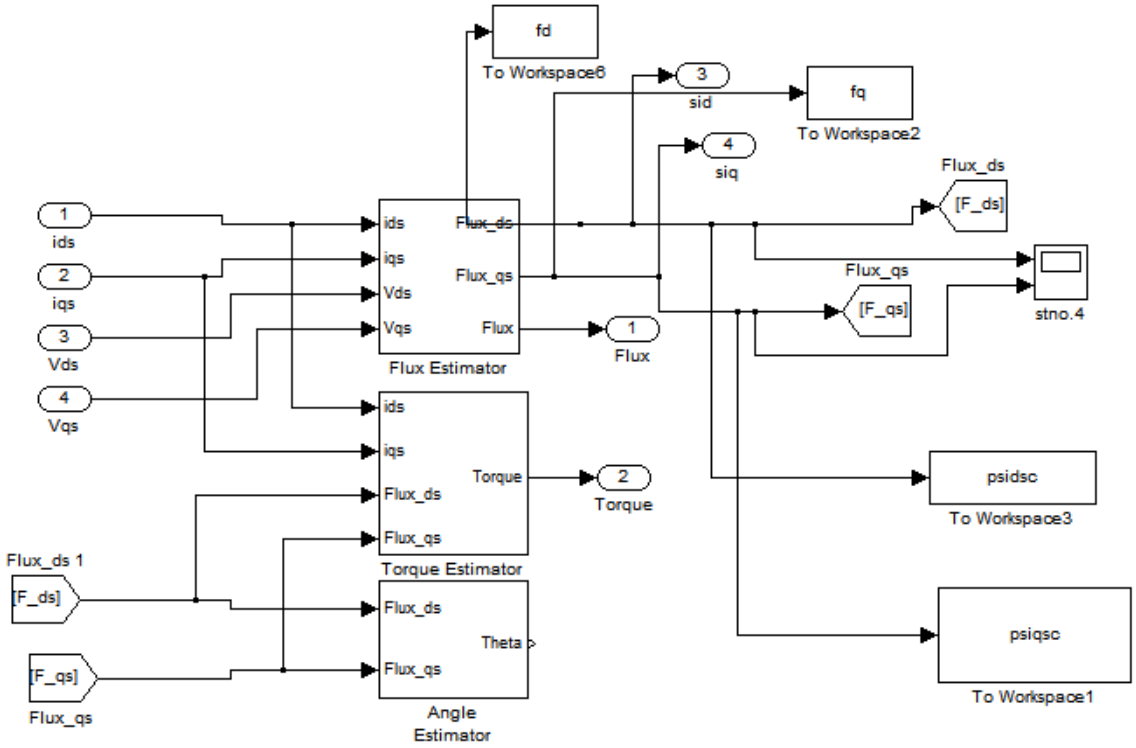

Fig. A. 1.2: Estimation of torque and flux of the induction motor

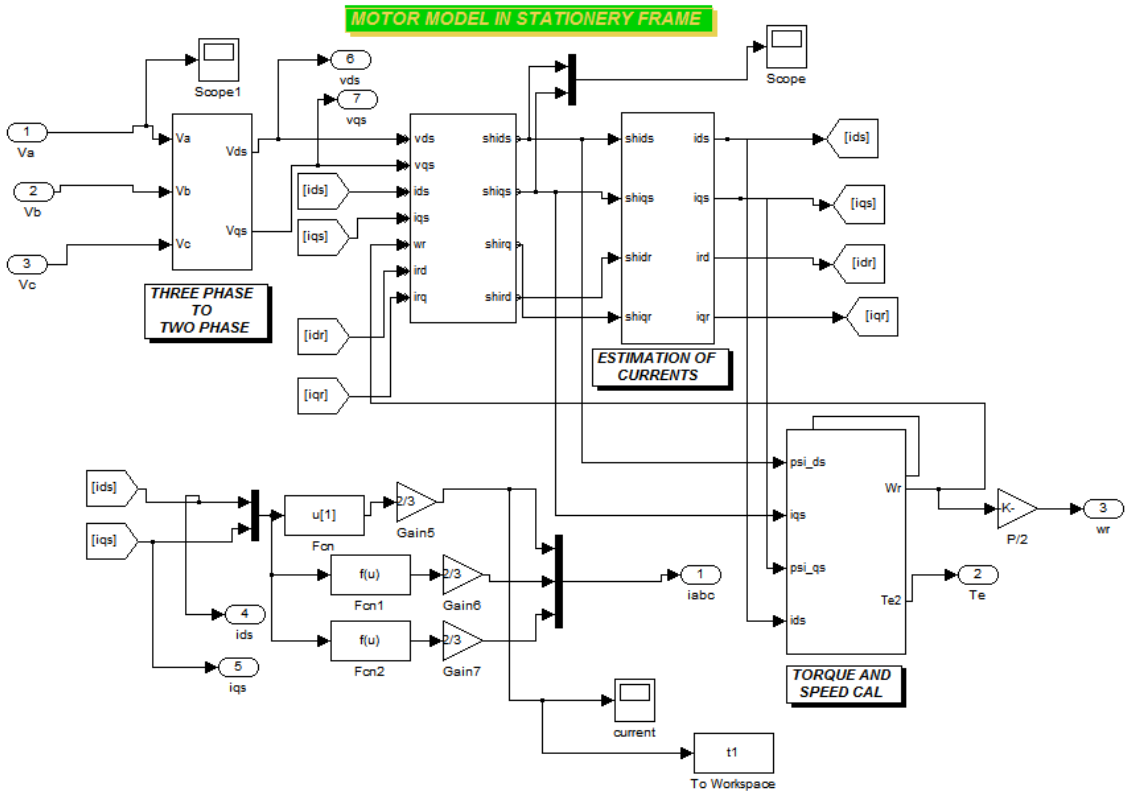

Fig. A. 1.3: Design of induction motor model

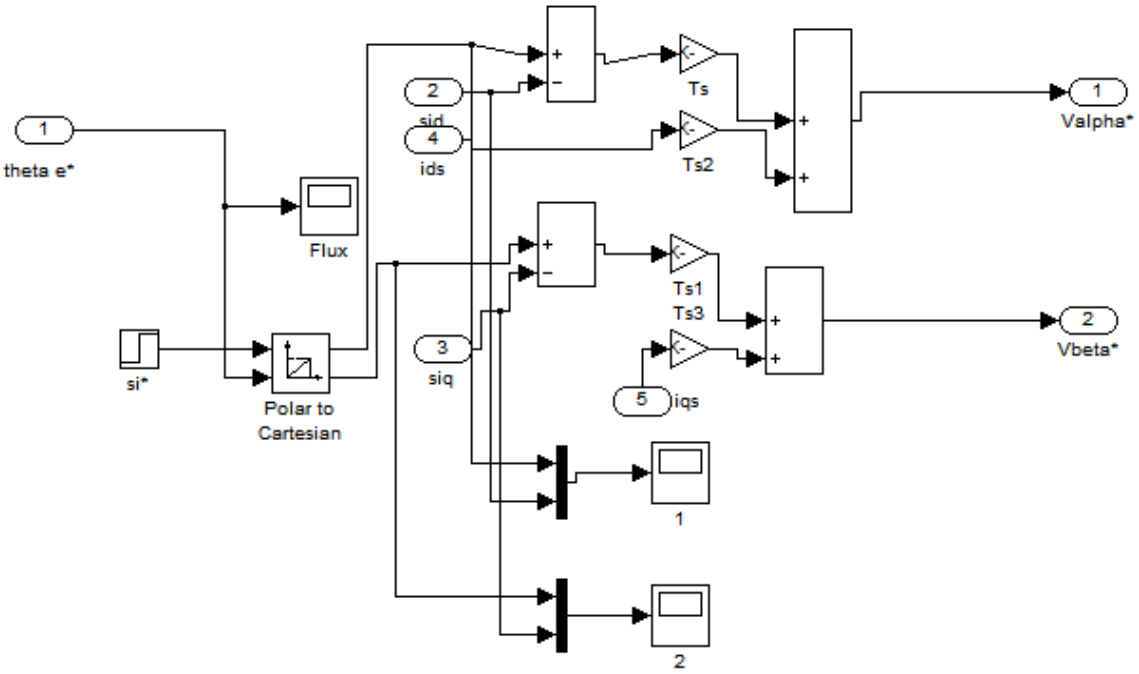

Fig. A. 1.4: V_α and V_β Calculation

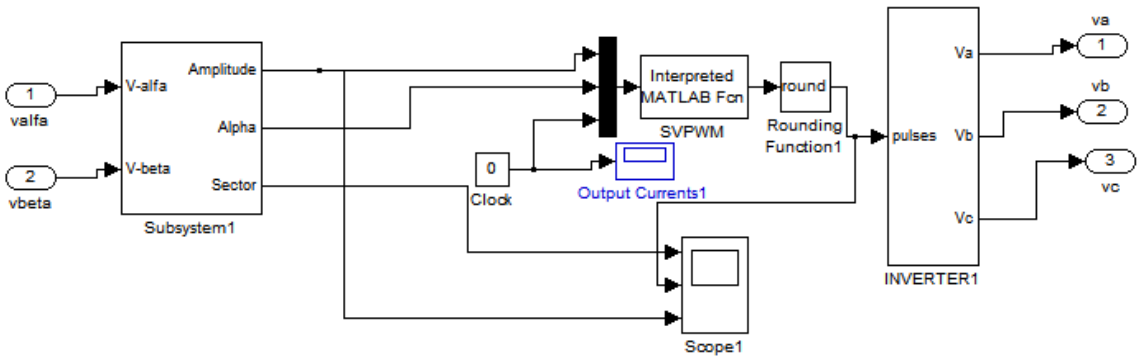

Fig. A. 1.5: SVPWM pulses developed with the help of reference vector

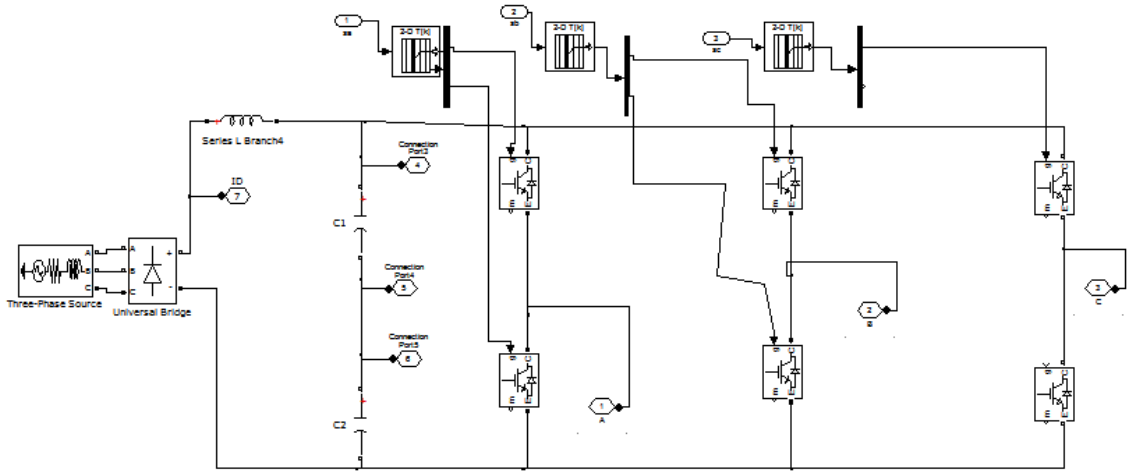

Fig. A. 1.6: Two-level inverter

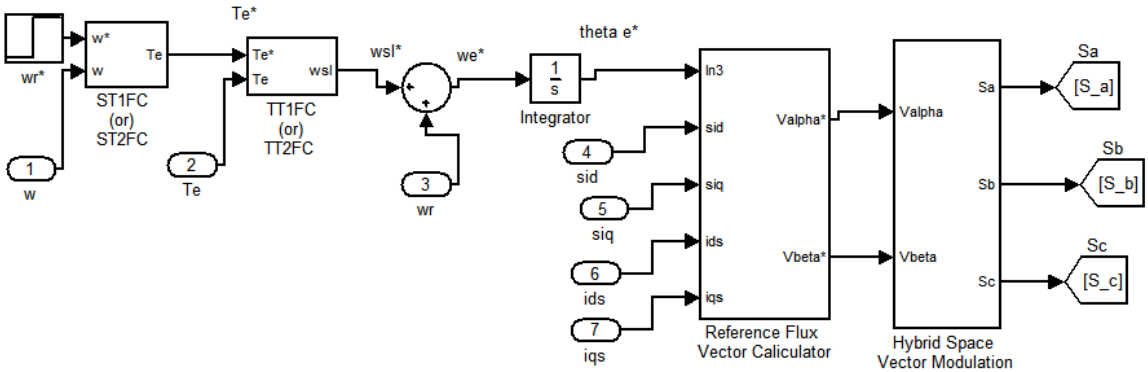

Fig. A. 1.7: Duty ratio control using type-1 and type-2 fuzzy control

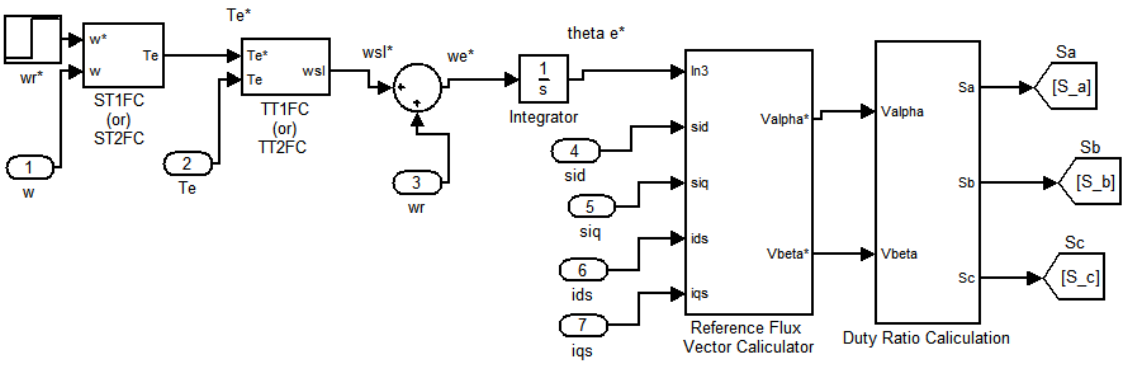

Fig. A. 1.8: Hybrid space vector modulation using type-1 and type-2 fuzzy control

APPENDIX-2

This appendix consists of the induction motor drive parameters and the screenshots of the MATLAB/Simulink models for the DTC using three-level inverter.

PARAMETERS OF IM DRIVE FOR THREE-LEVEL INVERTER

S. No.	**Parameters**	**2HP rating**
1	Rated supply voltage (VL-L)	440V (L-L)
2	Power rating (Po)	2HP
3	Rated speed (Nr)	1460 rpm
4	Number of poles	4
5	Stator resistance (Rs)	7.83Ω
6	Rotor resistance (Rr)	7.55 Ω
7	Stator leakage inductance (Ls)	0.4751H
8	Rotor leakage inductance (Lr)	0.4751H
9	Mutual inductance (Lm)	0.4535H
10	Moment of inertia (J)	0.06Kg-m2
11	Diodes	1000V/40A
12	Four DC-Link capacitors (C1 = C2)	2200μF/450V
13	MOSFETs (SPW47N60C3)	650V/45A
14	Voltage sensors (AD2OKY)	1000V
15	Current sensors (Telcon-HTP50)	50A
16	DC-Tacho-generator (RADIO ENGINE)	90V/3000rpm
17	Dead Band for two schemes	10μs
18	Sampling Time	45μs

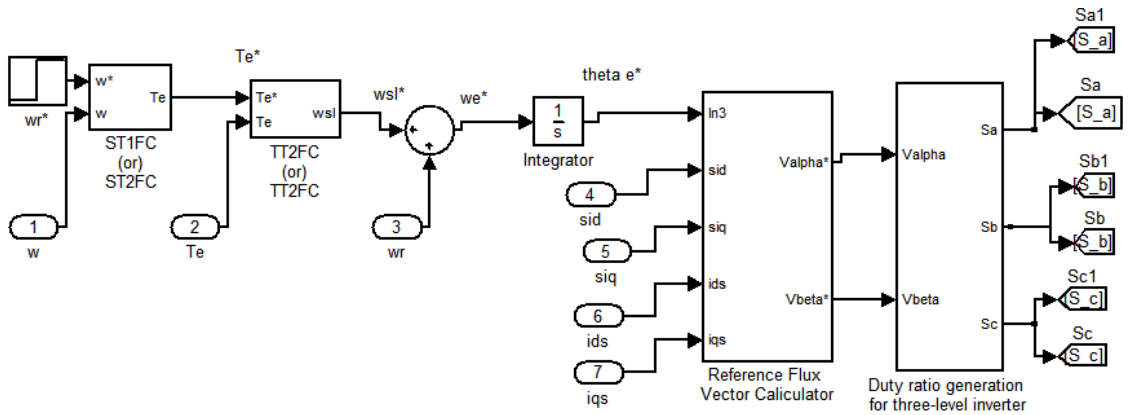

Fig. A. 2.1 Duty ratio control for three-level inverter fed induction motor using type-1 or type-2 fuzzy logic control

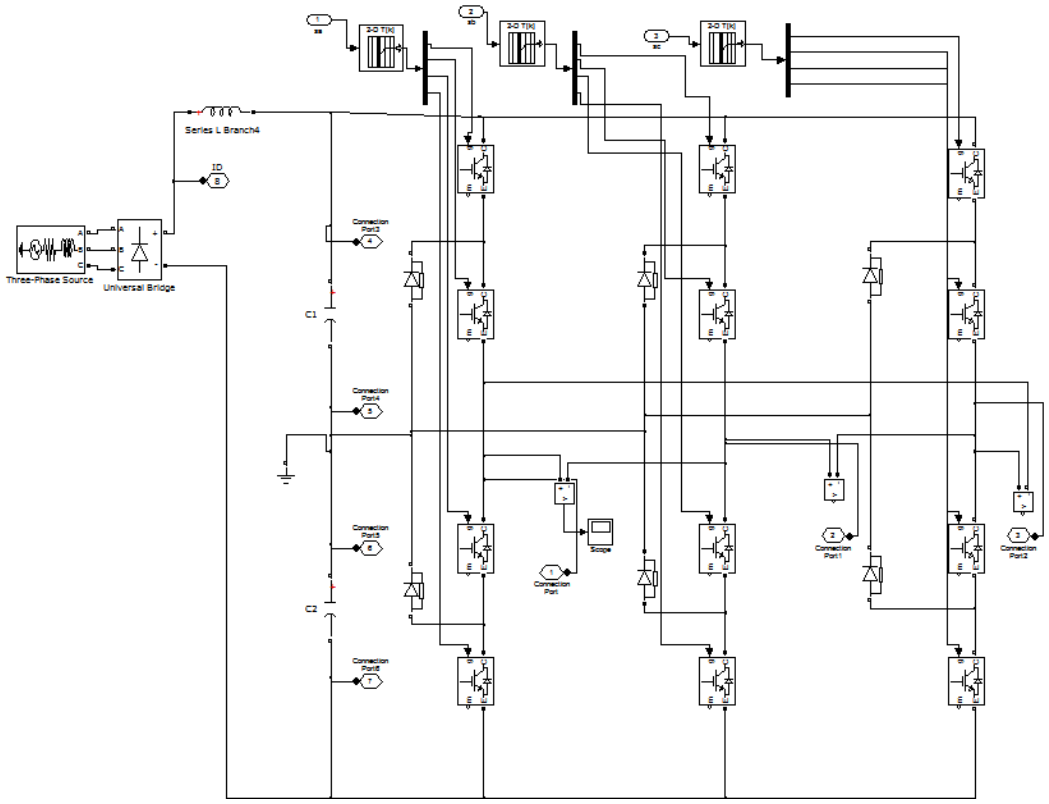

Fig. A. 2.2: Three-level inverter

APPENDIX-3

PARAMETERS OF IM DRIVE FOR FIVE-LEVEL INVERTER

S. No.	Parameters	2HP rating
1	Rated supply voltage (V_{L-L})	440V (L-L)
2	Power rating (P_o)	2HP
3	Rated speed (N_r)	1460 rpm
4	Number of poles	4
5	Stator resistance (R_s)	7.83Ω
6	Rotor resistance (R_r)	7.55 Ω
7	Stator leakage inductance (L_s)	0.4751H
8	Rotor leakage inductance (L_r)	0.4751H
9	Mutual inductance (L_m)	0.4535H
10	Moment of inertia (J)	0.06Kg-m^2
11	Diodes	1000V/40A
12	Four DC-Link capacitors ($C_1 = C_2$)	2200μF/450V
13	MOSFETs (SPW47N60C3)	650V/45A
16	Voltage sensors (AD2OKY)	1000V
17	Current sensors (Telcon-HTP50)	50A
18	DC-Tacho-generator (RADIO ENGINE)	90V/3000rpm
19	Dead Band for two schemes	10μs
20	Sampling Time	50μs

This appendix consists of the induction motor drive parameters, screenshots of the MATLAB/Simulink models for the DTC using five-level inverter and experimental setup.

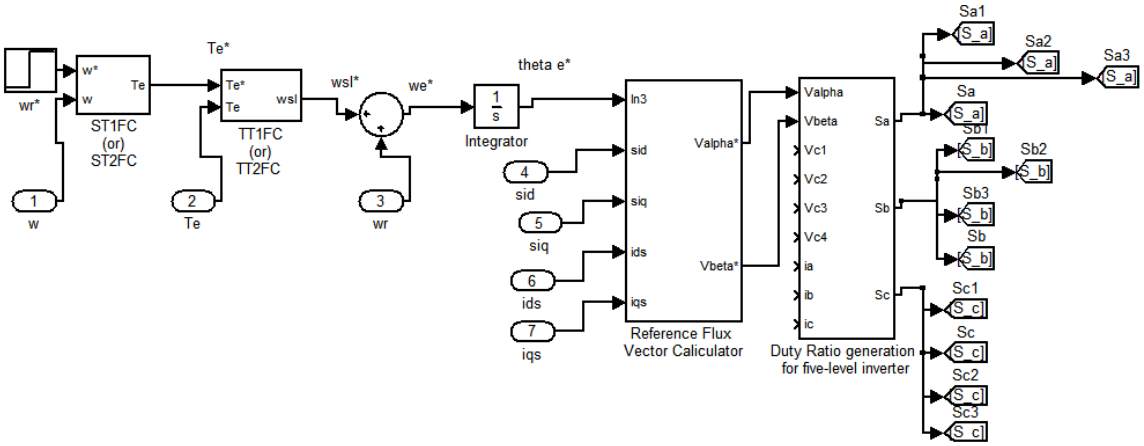

Fig. A. 2.1 Duty ratio control for five-level inverter fed induction motor using type-1 or type-2 fuzzy logic control

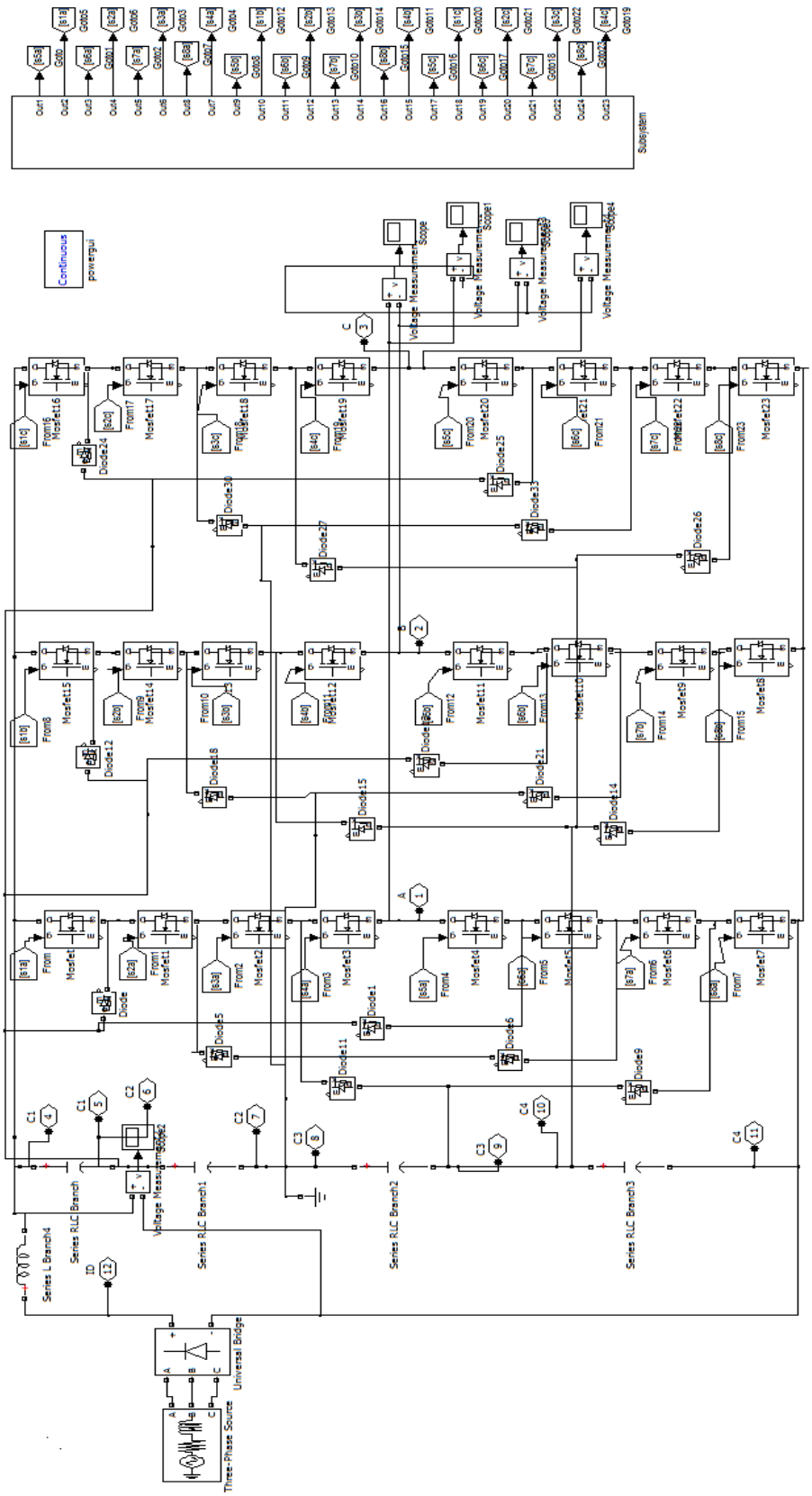

Fig. A. 3.2: Five-level inverter

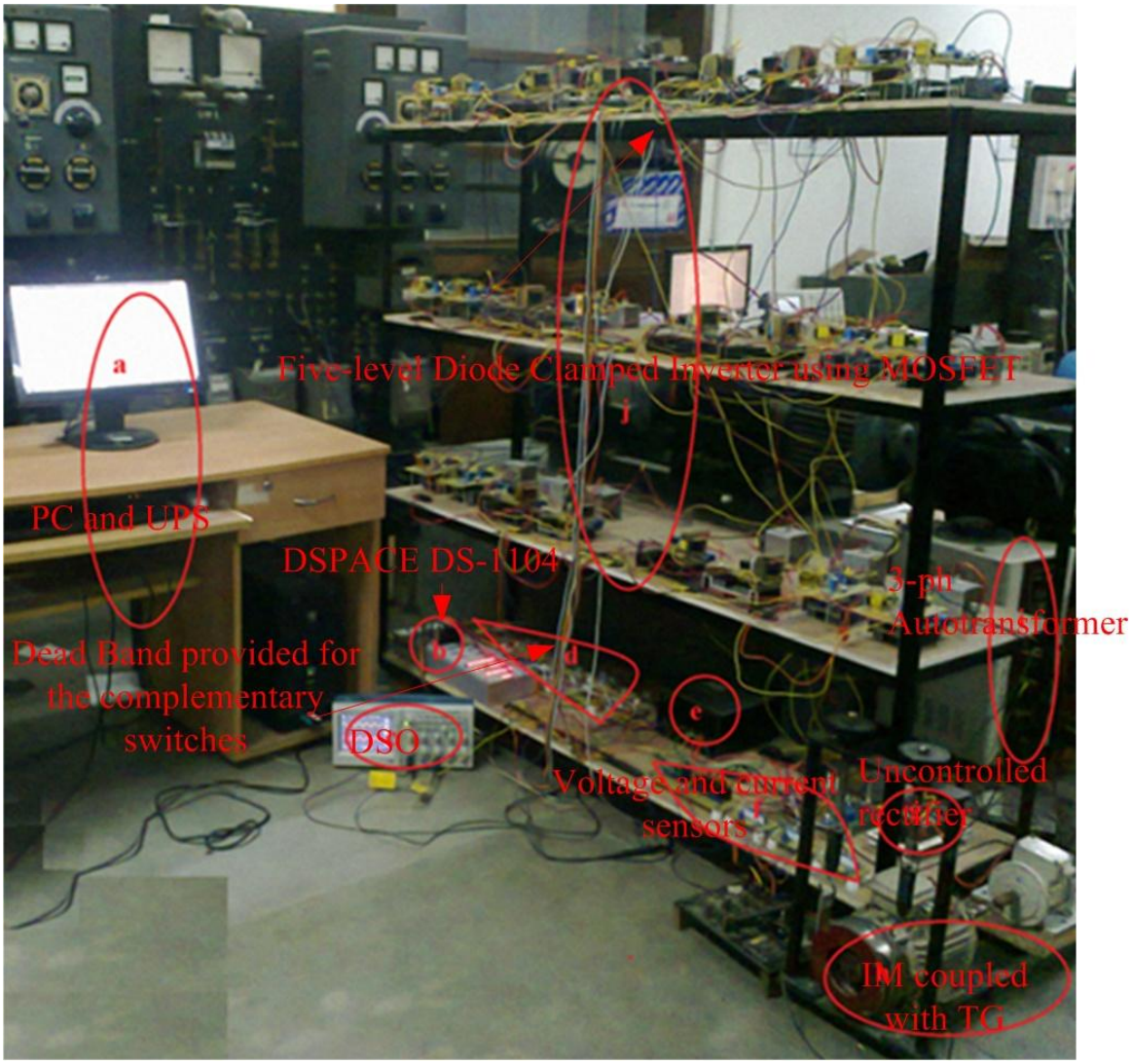

Fig. A 3.3 Experimental setup for five-level inverter

Fig. A 3.4 Sensors, Rectifier and RPS

Fig. A 3.5 Induction Motor Coupled with DC-Shunt generator and Tacho-generator

Fig. A 3.6 dSPACE control panel along with dead band circuits