MODELING AND CONTROL OF DC-DC CONVERTERS

Ph.D. THESIS

by

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A THESIS

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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in this thesis entitled **"MODELING AND CONTROL OF DC-DC CONVERTERS"** in partial fulfilment of the requirements for the award of the Degree of Doctor of Philosophy and submitted in the Department of Electrical Engineering of the Indian Institute of Technology Roorkee, Roorkee is an authentic record of my own work carried out during a period from July 2011 to January 2016 under the supervision of Dr. Yogesh Vijay Hote, Assistant Professor and Dr. Mukesh Kumar Pathak, Associate Professor, Department of Electrical Engineering, Indian Institute of Technology Roorkee, Roorkee, India.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other Institute.

(**MAN MOHAN GARG**)

This is to certify that the above statement made by the candidate is correct to the best of our knowledge.

(Yogesh Vijay Hote)
Supervisor

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Supervisor

Date: _____

ABSTRACT

The switch mode DC-DC converters are widely used in modern electronic systems as power supply because of their merits in terms of efficiency, compactness, light-weight, and reliability. They have many applications such as computer power supplies, aerospace instruments, medical instruments, telecommunication equipment, *etc*. The main feature of any DC-DC converter is to provide the stable desired DC output voltage irrespective of variations in the operating conditions such as input voltage, load current and reference output voltage (set point voltage). Normally, the input voltage to DC-DC converters is unregulated and the load current or set point voltage may also vary depending upon application requirements. Therefore, an accurate and reliable operation of DC-DC converters is essential under these circumstances. This has motivated to carry out this research work on the design, analysis, modeling, and control of the DC-DC converters.

This thesis moves around the three important aspects of the DC-DC converters namely design, modeling and control. The DC-DC converters have many non-isolated topologies like buck converter, boost converter, buck-boost converter, Cuk converter, Zeta converter, SEPIC converter, *etc*. In this thesis, two DC-DC converters, namely buck converter and Cuk converter have been considered for the research on above-mentioned aspects. The non-idealities of these converter elements are taken into consideration. These non-idealities are present in form of equivalent series resistances (ESRs) of the inductors and capacitors, the diode forward voltage drop and the on-resistances of the switch and diode.

In the first part of the thesis, the different design issues of the non-ideal DC-DC buck and Cuk converters are considered. The expressions of duty cycle, inductors, and capacitors are improved involving the non-ideal parameters of the converters. A detailed analysis of the output voltage ripple is carried out and importance of capacitor equivalent series resistance (ESR) is analyzed. A formula for maximum permissible ESR for specified output voltage ripple is proposed. The theoretical studies are validated via simulation and experimental results.

The second main aim of this thesis is to develop a mathematical model including all non-ideal elements, such that the developed model will be a close-replica of the practical converter in terms of dynamic and steady-state behaviour. The state-space averaging technique, averaged switch model technique and energy factor approach are used to develop the more accurate models of the non-ideal buck and Cuk converter. Further, the mathematical models in ideal and non-ideal case are compared. It is found that the models with non-idealities have much improved closeness to the practical converter as compared to the ideal counterpart.

In the final part, the performance of DC-DC buck and Cuk converters are improved using various controllers, namely the PI controller based on the stability boundary locus approach, PI-lead controller, two-loop controller, sliding mode controller. The algorithms for tuning the parameters of these controllers are proposed. The PI controller is also designed based on the reduced-order model of Cuk converter. The model-order reduction technique is used to obtain the reduced second-order model of the fourth-order Cuk converter. The hardware prototypes of DC-DC buck converters are developed and these control techniques are implemented on the prototypes. Extensive experimental and simulation studies are carried out for both types of converters. The comparative analysis of these control techniques is presented.

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(Man Mohan Garg)

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LIST OF ACRONYMS

dc, DC	Direct Current
ac, AC	Alternating Current
DSO	Digital Storage Oscilloscope
DSP	Digital Signal Processor
MOSFET	Metal Oxide Semiconductor Field-effect Transistor
pf, PF	Power Factor
PI	Proportional and Integral
PID	Proportional-Derivative-Integral
rms, RMS	Root Mean Square
SMPS	Switch Mode Power Supply
SSA	State-Space Averaging
SSE	Steady-State Error
PWM	Pulse Width Modulation
GM	Gain Margin
GCF	Gain Crossover Frequency
PM	Phase Margin
ESR	Equivalent Series Resistance
OVR	Output Voltage Ripple
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode

LIST OF SYMBOLS

$v_g(t)$	instantaneous input voltage
$v_L(t)$, $v_{L1}(t)$, $v_{L2}(t)$	instantaneous inductor voltage
$v_c(t)$, $v_{c1}(t)$, $v_{c2}(t)$	instantaneous capacitor voltage
$v_o(t)$	instantaneous output voltage
$I_g(t)$	instantaneous input current
$i_{sw}(t)$	instantaneous switch current
$i_D(t)$	instantaneous diode current
$i_L(t)$, $i_{L1}(t)$, $i_{L2}(t)$,	instantaneous inductor current
$i_c(t)$, $i_{c1}(t)$, $i_{c2}(t)$	instantaneous capacitor current
$i_o(t)$	instantaneous output current
K_p, K_i	Proportional and integral gains
L, L_1, L_2	Inductor
C, C_1, C_2	Capacitor
R	Load resistance
D	Duty cycle
D'	1-D
r_d	Diode forward resistance
r_{sw}	Switch on-resistance
r_x	$Dr_{sw}+ D'r_d$
r_L, r_{L1}, r_{L2}	ESR of Inductor
r_c, r_{c1}, r_{c2}	ESR of capacitor
V_F	Diode forward voltage drop

CHAPTER 1: INTRODUCTION

[This chapter describes the introduction of the thesis. The basic overview of power electronic converter and classifications of DC-DC converters are presented. The motivation of the work and thesis outlines is discussed.]

1.1 Overview

In the modern world, electric power has become a necessity for domestic appliances as well for industrial applications. There are various applications, which require the electric power in different forms like AC (Alternative current) or DC (direct current), constant or variable voltage, fixed or variable frequency, *etc*. Generally, at the consumer end, the electrical power is supplied in AC form with fixed voltage magnitude and fixed frequency (50 or 60 Hz). Therefore, to meet the demands of the different consumers, various types of power electronic converters have been developed. They convert one form of electrical power into another required form. Broadly, the power electronic converters can be classified into four types [1]–[3]:

1. AC-DC converters: These power electronic circuits convert AC voltage into a fixed or variable DC voltage. For example, diode rectifiers convert AC voltage into fixed DC voltage, whereas phase controlled rectifiers convert AC voltage into variable DC voltage.

2. DC-AC converters: They are also known as inverters. The input voltage to this converter is DC, which is converted into AC voltage of desired magnitude and frequency by varying the conduction period of the switches.

3. AC-AC converters: They convert fixed frequency and fixed magnitude AC voltage into variable magnitude AC voltage with same or variable frequency. For example, AC voltage regulators convert fixed AC voltage into variable AC voltage with the same frequency, whereas cyclo-converters give variable AC output voltage with variable frequency.

4. DC-DC converters: These converters transform electrical power of fixed DC voltage into variable DC voltage by controlling the conduction time of the switching devices.

In this thesis, the research work related to DC-DC converters have been carried out and discussed in the subsequent sections and chapters.

1.2 Introduction to DC-DC Converters

Modern electronic systems require high quality, compact, light-weight, reliable and efficient power supplies. For conventional low-power applications, the linear voltage regulators have generally been used. These linear regulators work on the principle of voltage divider circuit. The linear regulator can provide the output voltage only lower than the input voltage. Moreover, their energy conversion efficiency and power density are also low [1], [2], [4]. This makes them unsuitable for high power applications. For higher power applications, switching mode DC-DC converters are used. The switching mode DC-DC converters use the

power semiconductor switches, which either operate in saturation or cut off region [1]. Since the power loss is very small in these switches during the operation, the switching mode DC-DC converters can achieve higher energy conversion efficiency. Further, the modern semiconductor devices can operate at high frequencies leading to overall compact size due to reduction in the inductor and capacitor values [5], [6]. The switching mode DC-DC converters are now extensively used in the variety of industrial as well domestic applications owing to the advantages of controllable output voltage, compact size, light-weight and higher conversion efficiency [7]. Some of these applications include computer power supplies, aerospace instruments, fuel cells, medical instruments, power factor correction schemes, battery chargers, variable speed dc motor drives, telecommunication equipments, electrical vehicles, military instruments, chemical refineries, *etc* [8]–[21].

It is desirable to have minimum losses in the DC-DC converters while converting one level of DC voltage to another level. Therefore, to reduce the power losses, only inductors and capacitors are used in DC-DC converters (because ideally they have no losses). These passive components along with the semiconductor switches are assembled in different ways to obtain various topologies, each one having different properties [3], [22], [23]. In the literature, there are several classifications of DC-DC converter topologies based on the different criterion. However, the important DC-DC converters can be classified as follows:

Non-isolated DC-DC converters: In these converters, the load and input voltage source are not isolated electrically. There are several such topologies available in literature. The important topologies are: Buck converter, Boost converter, Buck-boost converter, Cuk converter, Zeta converter, SEPIC converter, *etc*.

Isolated DC-DC converters: In these DC-DC converters, the electrical isolation is provided between the input voltage source and load by means of a high frequency isolation transformer. The basic configurations are forward converter, flyback converter, push-pull converter, half bridge converter, full bridge converter, *etc*.

Further, several classifications are possible based on numbers of output (single output or multiple output), inductor current flow (continuous conduction mode (CCM) or discontinuous conduction mode (DCM)), magnitude of output voltage (buck, boost, buck-boost), *etc*. In continuous conduction mode (CCM), the inductor current is always positive during the entire switching period, whereas in discontinuous conduction mode (DCM), the inductor current becomes zero for a certain portion of switching period.

Based on the output voltage magnitude, a DC-DC switching converter can broadly be classified into the three categories: buck, boost and buck-boost. The basic topologies are shown in Fig. 1.1.

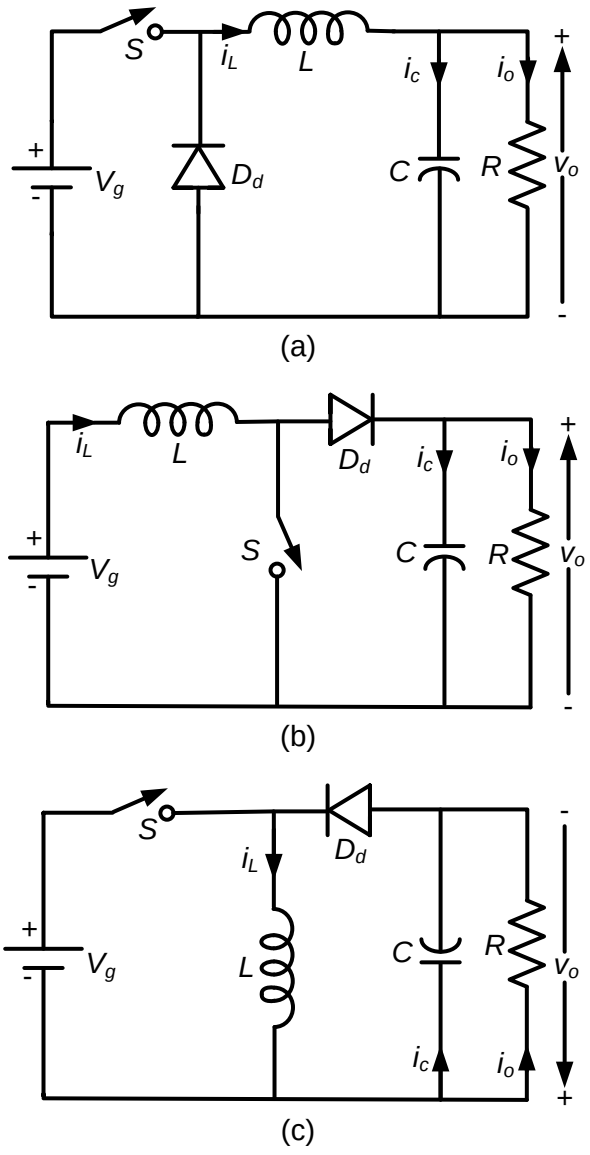


Fig. 1.1. Basic DC-DC converter topologies (a) Buck (b) Boost (c) Buck-boost

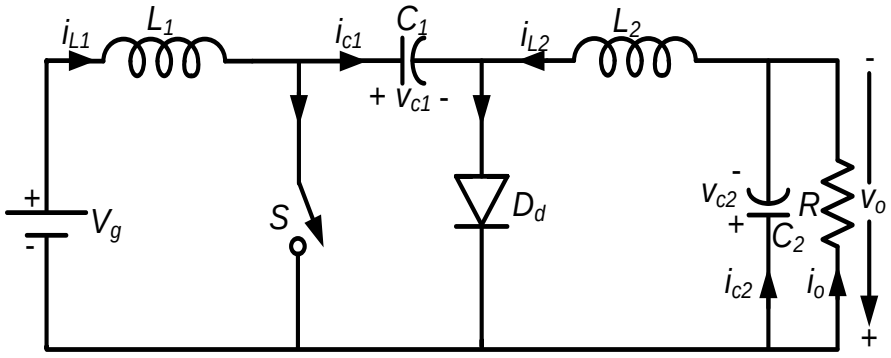


Fig. 1.2. DC-DC Cuk converter topology

The buck converter has an output voltage lower than the input voltage. It gives a continuous output current and lesser output voltage ripple requiring low value of capacitance. However, the input current is discontinuous (pulsed) in this topology, which requires the input filter. The boost converter provides an output voltage greater than the input voltage. The

input current is continuous, which eliminates the need of input filter. However, the output current is discontinuous (pulsed) in this topology and therefore, requires high value capacitance to reduce the output voltage ripple. The buck-boost converter gives an output voltage, which can be lower, equal or higher than the input voltage. The input current and output current both are discontinuous. The polarity of output voltage is opposite of the input voltage. These three basic topologies of DC-DC converters have simple configurations involving only one semiconductor switch, one diode, one inductor and one filter capacitor. These converters are second-order systems.

The advantages of these three converters can be combined in a single DC-DC converter arising a new topology named as Cuk converter [24],[25]. The circuit configuration of Cuk converter is shown in Fig. 1.2. This DC-DC converter provides continuous inductor current and continuous output current. The output voltage can be lower, equal or higher than the input voltage. Similar to buck-boost converter, the output voltage polarity is reverse of the input voltage. This converter involves two inductors and two capacitors. Therefore, it is a fourth-order system.

However, there are two other topologies similar to Cuk converter, which provides the output voltage with the same polarity as the input voltage. The topologies are DC-DC Zeta and SEPIC converters [26]–[28]. However, the Zeta converter suffers from discontinuous (pulsed) input current similar to buck converter and SEPIC converter suffers from discontinuous (pulsed) output current similar to boost converter. The Zeta and SEPIC converters are also fourth-order systems.

1.3 Motivation to the Research Work

In the previous section, it was discussed that there are several DC-DC converter topologies utilized in various applications. To meet the user requirements, it is necessary to decide the proper ratings of the different components of the particular DC-DC converter topology [29]–[40]. There are several factors, which decide the rating of the various passive elements and semiconductor devices used in the design of DC-DC converters [41], [42]. These factors are DC input voltage, DC output voltage, input current ripple, output voltage ripple, output power and switching frequency, *etc*. For an ideal DC-DC converter, the inductor value depends upon the desired ripple current and operating frequency. For small inductor current ripple, the high value of inductance is required [43]. However, the inductance value can be reduced by increasing the converter switching frequency. In practice, an inductance has small resistance, which causes some power losses in DC-DC converters. Therefore, inductor with low resistance is always preferred. The ferrite core inductors are normally used in the DC-DC converters operating at high switching frequencies. However, in the research papers and textbooks, the design equations of the inductors and capacitors do not involve the effect of all the non-idealities present in the elements. Similarly, the design of

capacitor is also an important issue for DC-DC converters. The capacitor value depends on the specified voltage ripple and switching frequency. However, the equivalent series resistance (ESR) of capacitor directly affects the output voltage ripple. The voltage ripple increases with the ESR. The various techniques has been reported in literature for output voltage ripple estimation and reduction [44]–[52]. Therefore, a proper analysis of ESR effect on the output voltage ripple on DC-DC converter is necessary, which is carried out in this thesis.

In addition to the design issues, the modeling of the switching converters has always been a topic of wide interest for power electronics engineers [1], [2], [25], [53]–[61]. In order to achieve the desired performance of a controller for DC-DC converters, an accurate model of DC-DC converter is required. In the last few decades, several techniques have been developed in literature to obtain the mathematical model of DC-DC converters such as state space averaging (SSA) method [58], [62]–[65], averaged switch model [66]–[68], energy factor approach [69], [70], transformer equivalent modeling method [3],[71], current injected equivalent circuit (CIEC) approach [72], [73], switching flow graph (SFG) technique [74], [75], bond graph technique [76], *etc*. These techniques are useful for modeling of DC-DC converter dynamics. It is observed in the literature that the converter models are generally obtained by neglecting the converter non-idealities. However, incorporation of non-idealities is an important aspect for getting more accurate mathematical models.

Further, the development of simple and efficient control algorithms for these converters is an interesting aspect for control engineers and researchers devoted in this area. A suitable controller is required to achieve the output voltage regulation of DC-DC converters in the presence of input voltage disturbances, load variations or set point (reference output voltage) variations and parameter variations. Especially, the controller design requires special attention as the order of DC-DC converters increases (due to increase in energy storage elements such as inductors and capacitors). The main objective of the controller design for DC-DC converters is to generate the switching pulses for the semiconductor devices with a duty cycle such that the DC output voltage is equal to the reference voltage. This output voltage regulation should be maintained despite variations in any operating conditions (such as load current, input voltage). This can be achieved by varying the duty cycle of the semiconductor switching device (hence the switch-on time) keeping the switching frequency constant. For this purpose, pulse-width modulation (PWM) technique is generally used. Therefore, the control problem is to monitor this duty cycle continuously so that the proper switching pulses are generated. The voltage mode control and current mode control are generally used for DC-DC converters in conjunction with suitable controller. In literature, many control design techniques are discussed, *e.g.* PI/PID controller, lag compensator, lead compensator, lag-lead compensator, pole-placement technique, fuzzy controller, genetic

algorithm based controller, sliding mode controller, H-infinity controller, *etc* [77]–[105]. All these control techniques have their own advantages and disadvantages depending upon the applications. However, there is always a scope to improve these techniques for better performance of the DC-DC converters. Further, the Cuk converter is a fourth-order system and therefore, the several model-order reduction techniques available in the literature can be used to obtain its reduced-order model [106]–[109]. The reduced-order model can be used to design the controller for the original system with less computational efforts.

In summary, for any DC-DC converter, one first needs to design its parameters for specified user requirements. Then, carry out its mathematical modeling and finally, design a suitable controller to regulate the output voltage under various working conditions. Therefore, in this thesis, the research work is carried out on these three aspects of DC-DC converters, which are as follows:

1. Design of DC-DC converters
2. Mathematical modeling of DC-DC converters
3. Control design techniques for DC-DC converters

As discussed earlier, there are several DC-DC converter topologies, but in this thesis, these three aspects are discussed detail for non-ideal DC-DC buck converter and Cuk converter.

1.4 Contribution of the Author and Thesis Organization

Although lot of research work have been carried out in the field of design, modeling and control of DC-DC converters. In this thesis an attempt has been made to contribute further in these three aspects of the DC-DC converters. In the literature, it is found that the effect of all the non-idealities has not been considered while designing the converter parameters and modeling the DC-DC converters. These non-idealities are present in the form of equivalent series resistances (ESRs) of inductors and capacitors, parasitic resistances of the diode and MOSFET during conduction and the forward voltage drop of the diode. In this thesis, the effect of all the non-idealities has been incorporated. The detailed contribution of the author has been reported in the subsequent chapters of the thesis. This thesis has five more chapters in addition to this introduction chapter. The brief descriptions of the author's contribution in each chapter are outlined as follows:

In Chapter 2, the improved expressions of the duty cycle are derived for the non-ideal DC-DC buck converter and Cuk converter. The effect of the non-idealities is included. Based on the improved expression, the design equations for inductor and capacitor calculations are also modified for these two converters. The improved expressions show that the duty cycle also depends on load resistances and non-idealities along with the input voltage. Further, with the detailed analysis of the capacitor voltage ripple, a formula for the maximum

allowable value of the capacitor ESR is developed for non-ideal buck converter and Cuk converter. This expression gives the maximum value of ESR for specified output voltage ripple and inductor current ripple at a particular frequency. For the Cuk converter, the design formula for input capacitor is also modified to incorporate the effect of its ESR. The theoretical studies are then validated by both simulation and experimental results.

Chapter 3 presents a detailed mathematical modeling of non-ideal DC-DC buck and Cuk converter based on state-space averaging technique, averaged switch model technique and energy factor approach. The parasitic resistances and diode voltage drop are included in the improved mathematical model of these converters. In the state-space averaging technique, the Leverrier's algorithm is used to derive the various transfer functions of the non-ideal converter. The comparisons of mathematical models in the case of ideal converter and non-ideal converter are presented, which shows that the mathematical modeling of the non-ideal converter gives more information of the physical converter, which are not revealed if the converter is assumed ideal.

In Chapter 4, the different classical control techniques are discussed which are based on the transfer function model of non-ideal DC-DC buck and Cuk converter. In this chapter, a PI controller has been designed for the buck and Cuk converter using the stability boundary locus approach based on the specified phase margin. It is seen that the PI controller is useful to eliminate the steady-state error in output voltage, but the transient response is not very good. Therefore, a PI-lead control technique has been presented. An algorithm has been proposed to tune the parameters of this PI-lead controller based on desired phase margin and gain crossover frequency. This algorithm provides the analytical formulae, which give the phase margin and gain crossover frequency exactly as specified. The PI-lead controller results in improved transient response. However, this controller contributes noise in output voltage for higher bandwidth. To improve the output voltage response of DC-DC converters further, a two-loop control scheme has been reported in this chapter. This control scheme has one inner current PI controller and one outer voltage PI controller. An algorithm is proposed for tuning the parameters of these two PI controllers based upon the desired phase margin and gain crossover frequency specifications. The beauty of the proposed algorithm is that the designed controller simultaneously satisfies the desired phase margin and crossover frequency requirements. As the Cuk converter is a fourth-order system, therefore, its reduced second-order model has also been obtained by means of model-order reduction techniques. Then, the PI controller is design based on reduced second-order model. It requires less computational effort for controller design in comparison to original fourth-order model. The controller thus obtained is implemented on actual fourth-order Cuk converter and shows good performance almost similar to the PI controller designed with original model.

All the control techniques are validated on the hardware prototypes of DC-DC buck and Cuk converters under various operating conditions and show the close agreement with MATLAB simulation results.

Chapter 5 describes the sliding mode control of DC-DC Cuk converter. The various transfer functions are obtained to analyse the closed-loop dynamics of sliding mode controlled Cuk converter. A simplified technique is suggested to tune the parameters of the controller. The simulation and experimental results are presented to validate the performance of the designed controller.

Finally, the conclusion of this complete work and possible future scope are summarized in chapter 6.

The appendixes and important references used in this entire work are given at the end of this thesis.

[In this chapter, various design issues related to non-ideal DC-DC Buck and Cuk converters have been covered in detail. The effects of all the non-idealities present in the converter elements are included.]

2.1 Introduction

DC-DC converters are widely used as power supply in various applications. Some applications like aerospace, military, chemical refineries and mines require tightly regulated, optimally designed and compact power supplies. For such applications, the optimum design of inductance and capacitance for DC-DC converters is required [110]–[113]. In most of the research papers and text-books, the analysis and design have been carried out by assuming the converter's elements to be ideal [1]–[3], [48], [114]. However, the elements of the DC-DC converters are not ideal in practice and have many non-idealities [115]–[117]. These non-idealities are present in the form of equivalent series resistances (ESRs) of inductors and capacitors, parasitic resistances of the MOSFET and diode during conduction and the forward voltage drop of diode. These non-idealities affect the performance and parameter design of DC-DC converter, which is not acceptable for an accurate and well-designed power supply. For example, the expressions of duty cycle for an ideal buck and Cuk converter operating in continuous conduction mode (CCM) are given as:

For buck converter,
$$D_{ideal} = \frac{V_o}{V_g} \tag{2.1}$$

For Cuk converter,
$$D_{ideal} = \frac{V_o}{V_o + V_g} \tag{2.2}$$

Where, V_g is the input voltage and V_o is the output voltage.

The above expressions are derived by assuming that all the elements in buck and Cuk converter are ideal [2], [3]. Therefore, in practical (lossy) buck and Cuk converter, these ideal duty cycle expressions do not provide the desired output voltage V_o for given input voltage V_g. This is because of the voltage drops (or power losses) occurring across the non-ideal components. To compensate these voltage drops or power losses, the actual duty cycle should be greater than the ideal duty cycle given by (2.1) and (2.2). Similarly, the proper design of the converter parameters is essential for achieving the desired performance. This requires in-depth analysis of converter circuit and its operation. In this chapter, a detailed analysis of non-ideal DC-DC buck converter and Cuk converter are carried out to obtain the improved design equations for inductor and capacitors.

Similarly, the capacitor design and correct estimation of output voltage ripple (OVR) are important issues for DC-DC converters, especially in high performance applications [49], [118], [119]. The equivalent series resistance (ESR) of the output capacitor plays an

important role in the design of capacitor for specified output voltage ripple. The low ESR capacitor results in lesser output voltage ripple. On the other hand, large ESR increases the output voltage ripple, hence requiring the higher value of capacitance. Moreover, ESR may also affect the stability and increase the power loss in converters [46], [120]–[122]. Therefore, the arbitrary value of ESR is not advisable for a precisely designed DC-DC converter. The ESR of a capacitor is a parasitic parameter that cannot be avoided by a capacitor manufacturer. However, from a power supply designer's point of view, a capacitance with low ESR is always preferable [50]. In literature, no analytical solution is available to determine the upper limit of ESR, which can be used without exceeding the specified output voltage ripple at a particular switching frequency. In this chapter, with detailed analysis of capacitor voltage ripple, a formula for the maximum allowable value of the capacitor ESR is developed for non-ideal buck converter and Cuk converter.

In the following sections, all these design issues are investigated for non-ideal DC-DC buck and Cuk converters.

2.2 Analysis of Non-ideal DC-DC Buck Converter

The basic circuit of a non-ideal DC-DC buck converter is shown in Fig. 2.1(a). It consists of a power MOSFET switch *S*, diode D_d, inductor *L*, capacitor *C* and load resistance *R* [1], [3]. For accurate analysis and design of the converter parameters, the non-idealities have been included in this circuit. These non-ideal elements are represented as equivalent series resistance (ESR) of inductor r_L, ESR of capacitor r_c, switch on-resistance r_{sw}, diode forward resistance r_d and diode forward voltage drop V_F. The values of these parasitic resistances are very small in comparison to load resistance *R*. The buck converter can operate in continuous conduction mode (CCM) and discontinuous conduction mode (DCM). However, in this thesis, the converter is assumed to operate in a continuous current conduction mode (CCM) with static duty cycle *D* and switching frequency f_s (or switching period *T*). The duty cycle *D* is the ratio of time duration for which switch is on (t_{on}) to the total switching period (*T*). Mathematically,

$$D = \frac{t_{on}}{t_{on} + t_{off}} = \frac{t_{on}}{T} = t_{on} f_s \tag{2.3}$$

Where, t_{on} is the time interval for which the switch is on and t_{off} is the time interval for which the switch is off.

From (2.3), we get

Switch-on time $t_{on} = DT$ (2.4)

Switch-off time $t_{off} = (1-D)T = D'T$ (2.5)

Where *D'=1-D*

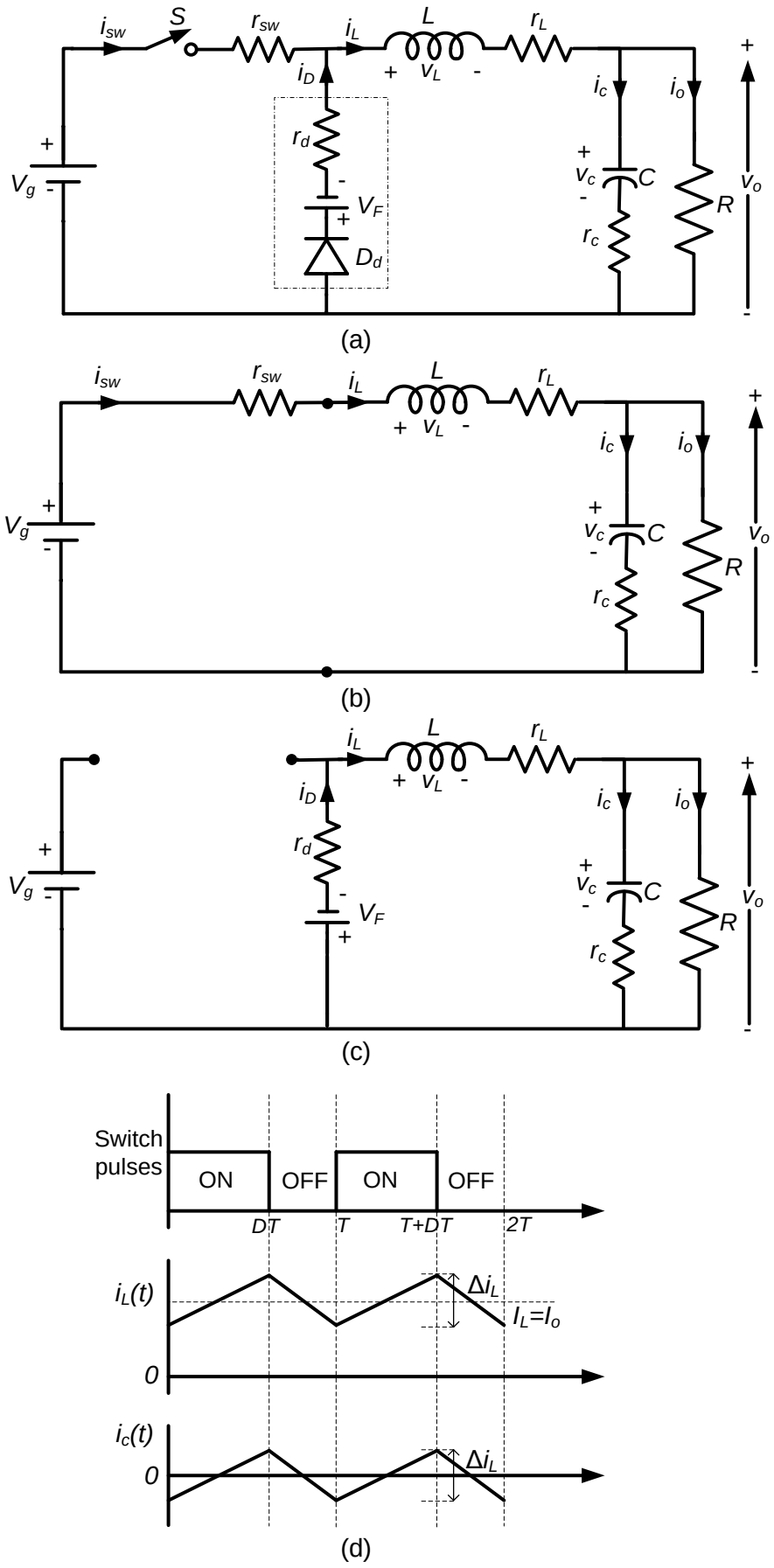


Fig. 2.1.(a) Basic circuit of a non-ideal DC-DC buck converter (b) equivalent circuit when the switch is on (c) equivalent circuit when the switch is off (d) associated waveforms

In continuous current conduction mode, the buck converter has two circuit states (a) when MOSFET switch conducts and diode remains off (b) when MOSFET switch remains off and diode conducts. The analysis of non-ideal buck converter in these two states is discussed in detail as follows:

2.2.1 When the switch is on (time interval $0 < t \leq DT$)

The corresponding equivalent circuit of a non-ideal DC-DC buck converter is shown in Fig. 2.1(b) for the time interval $0<t\leq DT$. In this duration, the MOSFET switch *S* is conducting and diode D_d is off. The switch is represented by its on-resistance r_{sw} and diode is represented as an open circuit. The switch current (i_{sw}) is equal to inductor current (i_L) and the diode current (i_D) is zero. The input power source supplies the power for inductor energy storage and load resistance. In this mode, the capacitor is discharged initially by the load resistance and then charged by the input current. The corresponding important waveforms are given in Fig. 2.1(d).

Using the Kirchhoff's voltage and current law (KVL and KCL), the voltage across inductor *L*, the current through capacitor *C* and the output voltage are given as:

$$v_{L,on}(t) = L\frac{di_L(t)}{dt} = v_g(t) - (r_L + r_{sw})i_L(t) - v_o(t) \tag{2.6}$$

$$i_{c,on}(t) = i_L(t) - \frac{v_o(t)}{R} \tag{2.7}$$

$$v_{o,on}(t) = v_c(t) + r_c i_c(t) \tag{2.8}$$

2.2.2 When the switch is off (time interval $DT < t \leq T$)

The corresponding equivalent circuit of a non-ideal DC-DC buck converter is shown in Fig. 2.1(c) for time interval $DT< t \leq T$. In this duration, the MOSFET switch *S* is off and diode D_d is conducting. The diode is represented by its on-resistance r_d and switch is represented as an open circuit. The diode current (i_D) is equal to inductor current (i_L) and the switch current (i_{sw}) is zero. In this mode, the load is disconnected from the input power source. The energy stored in the inductor is used to feed the power to load resistance. The capacitor is charged initially by inductor energy and then discharged by load current. The corresponding important waveforms are given in Fig. 2.1 (d).

Using the Kirchhoff's voltage and current law (KVL and KCL), the voltage across inductor *L*, the current through capacitor *C* and the output voltage are given as:

$$v_{L,off}(t) = L\frac{di_L(t)}{dt} = -(r_L + r_d)i_L(t) - V_F - v_o(t) \tag{2.9}$$

$$i_{c,off}(t) = i_L(t) - \frac{v_o(t)}{R} \tag{2.10}$$

$$v_{o,off}(t) = v_c(t) + r_c i_c(t) \tag{2.11}$$

2.2.3 Steady-state analysis

For steady-state analysis, the average value Z of a current and voltage variable $z(t)$ can be given as [3]:

$$Z = \frac{1}{T}\int_0^T z(t)dt = \frac{1}{T}\int_0^{DT} z_{on}(t)dt + \frac{1}{T}\int_{DT}^{T} z_{off}(t)dt \tag{2.12}$$

Where, $z_{on}(t)$ and $z_{off}(t)$ represent the variable $z(t)$ during switch on and switch off, respectively.

According to the principle of inductor volt-second balance, in steady-state, the average inductor voltage must be equal to zero *i.e.,*

$$V_L = \frac{1}{T}\int_0^T v_L(t)dt = \frac{1}{T}\int_0^{DT} v_{L,on}(t)dt + \frac{1}{T}\int_{DT}^{T} v_{L,off}(t)dt = 0 \tag{2.13}$$

Similarly, according to the principle of capacitor charge-balance, in steady-state, the average capacitor current must be equal to zero *i.e.,*

$$I_c = \frac{1}{T}\int_0^T i_c(t)dt = \frac{1}{T}\int_0^{DT} i_{c,on}(t)dt + \frac{1}{T}\int_{DT}^{T} i_{c,off}(t)dt = 0 \tag{2.14}$$

The average output voltage of the buck converter is

$$V_o = \frac{1}{T}\int_0^T v_o(t)dt = \frac{1}{T}\int_0^{DT} v_{o,on}(t)dt + \frac{1}{T}\int_{DT}^{T} v_{o,off}(t)dt \tag{2.15}$$

Substituting (2.6) and (2.9) in (2.13) and simplifying, we get

$$V_L = D\left[V_g - (r_L + r_{sw})I_L - V_o\right] + (1-D)\left[-(r_L + r_d)I_L - V_F - V_o\right] = 0$$
$$\Rightarrow DV_g = D'V_F + V_o + (r_L + Dr_{sw} + D'r_d)I_L \tag{2.16}$$

Substituting (2.7) and (2.10) in (2.14) and simplifying, we get

$$I_c = D\left[I_L - \frac{V_o}{R}\right] + (1-D)\left[I_L - \frac{V_o}{R}\right] = 0 \Rightarrow I_L = \frac{V_o}{R} = I_o \tag{2.17}$$

Here, I_o is the steady-state value of the load current.

Substituting (2.8) and (2.11) in (2.15) and simplifying, we get

$$V_o = D\left[V_c + r_c I_c\right] + (1-D)\left[V_c + r_c I_c\right] \Rightarrow V_o = V_c + r_c I_c \tag{2.18}$$

Since, in steady-state, the average value of capacitor current $I_c=0$, Therefore, from (2.18),

$$V_o = V_c \tag{2.19}$$

2.2.3.1 Expression for output voltage

Substituting values of I_L from (2.17) into (2.16), we get

$$DV_g = D'V_F + V_o + (r_L + Dr_{sw} + D'r_d)\frac{V_o}{R} \tag{2.20}$$

Simplifying (2.20) gives the average output voltage of the buck converter as:

$$V_o = \frac{DV_g - D'V_F}{1 + \dfrac{(r_L + Dr_{sw} + D'r_d)}{R}} \tag{2.21}$$

Equation (2.21) shows that the average output voltage of the non-ideal buck converter depends on input voltage, parasitic resistances of converter elements, diode forward voltage drop, and load resistance as well. The larger the value of these non-idealities, the lesser will be the output voltage. However, for ideal buck converter, the output voltage does not depend on non-idealities and load resistances. In the ideal case, it is equal to duty cycle multiplied by input voltage. Mathematically,

$$V_o = DV_g \tag{2.22}$$

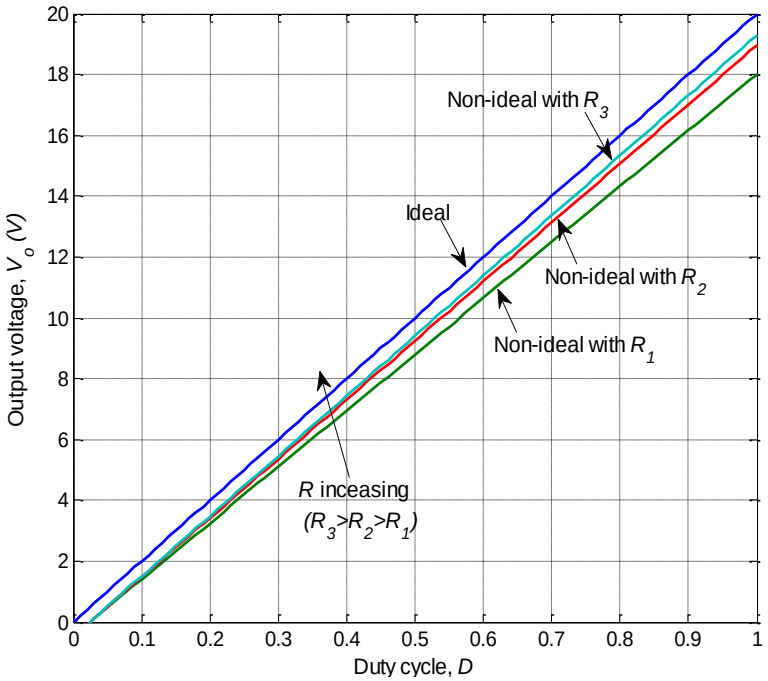


Fig. 2.2. Output voltage variation with duty cycle at various R and constant V_g (R_1=5 Ω, R_2=10 Ω, R_3=15 Ω and V_g =20 V)

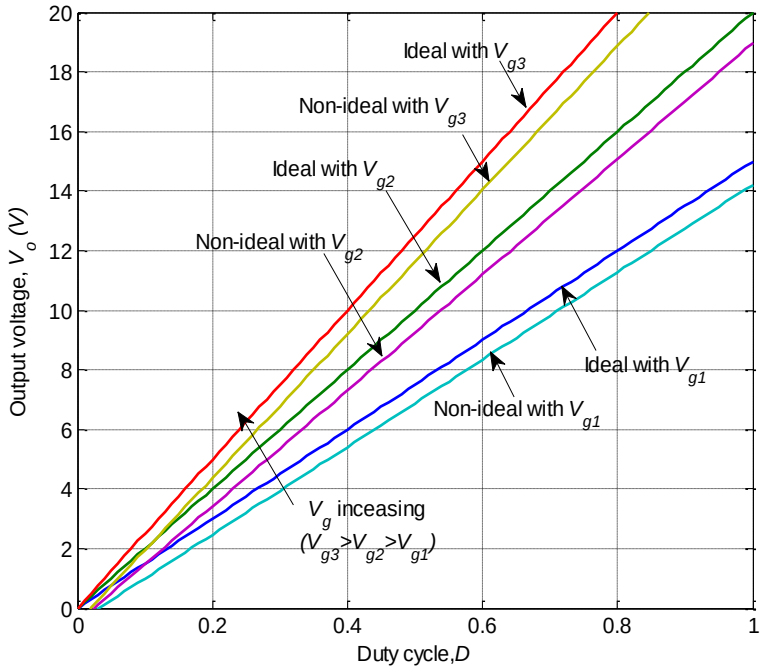


Fig. 2.3. Output voltage variation with duty cycle at various V_g and constant R (V_{g1}=15 V, V_{g2}=20 V, V_{g3}=25 V and R=10 Ω)

Table 2.1. Non-ideal DC-DC buck converter specifications

Parameters	**Value**
Input voltage, V_g	20 V
Output voltage, V_o	12 V
Load resistance, R	10 Ω
Inductance, L/r_L	490 μH/0.5 Ω
Capacitance, C/r_c	50 μF/0.1 Ω
Diode forward voltage, V_F	0.5 V
Resistance switch/diode (r_{sw}/r_d),	0.05 Ω/0.03 Ω
Switching frequency, f	20 kHz
Desired inductor current ripple, $\Delta i_L/I_L$	0.4
Desired output voltage ripple, $\Delta v_{om}/V_o$	0.01

The output voltage variation versus duty cycle plot is shown in Fig. 2.2 at constant input voltage V_g and different load resistances. The input voltage is kept constant 20 V, whereas the three different values of load resistance 5 Ω, 10 Ω and 20 Ω are taken. The values of parasitic resistances and diode forward voltage drop are considered constant and these values are same as given in Table 2.1. Fig. 2.2 clearly indicates that for a particular duty cycle, the non-ideal buck converter produces DC output voltage less than the ideal buck converter. The output voltage further decreases as the load resistance is decreased (or load current is increased). Because, as the load current increases, the voltage drops across the parasitic resistances would increase, resulting in lesser DC output voltage. The output voltage variation for different values of input voltage at constant load resistance R is shown in Fig. 2.3. The load resistance is kept constant at 10 Ω, whereas the values of input voltage are varied to three different values 15 V, 20 V and 25 V. For a particular value of duty cycle, the difference between the output voltage of ideal and non-ideal buck converter is clearly observed. This difference becomes larger as the input voltage increases. The reason for this large difference is that for the increased value of input voltage, the current drawn from input supply would be more, which causes more voltage drop across the non-idealities.

Therefore, by this analysis, it is verified that the output voltage of practical (non-ideal) buck converter is always less than the ideal buck converter. In order to achieve the desired output voltage in the presence of the non-idealities, the MOSFET switch should be kept ON for some extra time. In other words, the actual duty cycle must be greater than the ideal duty cycle given by (2.1).

2.2.3.2 Improved expression of duty cycle

As discussed previously, in order to obtain the desired output voltage in the presence of the non-idealities, the actual duty cycle must be increased. The improved expression of this actual duty cycle in terms of non-idealities is obtained analytically in this subsection.

Rearranging (2.21),

$$V_o\left(1+\frac{\left(r_L+Dr_{sw}+D'r_d\right)}{R}\right)=DV_g-D'V_F \tag{2.23}$$

Substituting *D'=1-D* in the above equation and simplifying,

$$V_o+V_o\frac{r_L}{R}+DV_o\frac{r_{sw}}{R}+(1-D)V_o\frac{r_d}{R}=DV_g-(1-D)V_F$$

$$\Rightarrow D\left(V_g+V_F+V_o\frac{\left(r_d-r_{sw}\right)}{R}\right)=V_o\left(1+\frac{r_L+r_d}{R}\right)+V_F$$

$$\Rightarrow D=\frac{V_o\left(1+\frac{r_L+r_d}{R}\right)+V_F}{V_g+V_F+V_o\frac{\left(r_d-r_{sw}\right)}{R}} \tag{2.24}$$

This expression can further be rewritten as follows:

$$D=\frac{V_o}{V_g}\frac{1+\frac{r_L+r_d}{R}+\frac{V_F}{V_o}}{1+\frac{V_F}{V_g}+\frac{V_o}{V_g}\frac{\left(r_d-r_{sw}\right)}{R}}\Rightarrow D=D_{ideal}\frac{1+\frac{r_L+r_d}{R}+\frac{V_F}{V_o}}{1+\frac{V_F}{V_g}+\frac{V_o}{V_g}\frac{\left(r_d-r_{sw}\right)}{R}} \tag{2.25}$$

Where, $D_{ideal}=V_o/V_g$ is duty cycle for an ideal buck converter.

For a DC-DC buck converter, the input voltage is less than the output voltage, thus the following inequality holds true.

$$1+\frac{r_L+r_d}{R}+\frac{V_F}{V_o}>1+\frac{V_F}{V_g}+\frac{V_o}{V_g}\frac{\left(r_d-r_{sw}\right)}{R} \tag{2.26}$$

Therefore, the actual duty cycle *D* given by the expression in (2.25) will always be greater than the D_{ideal}.

By putting all non-idealities to zero, the duty cycle *D* becomes same as ideal duty cycle D_{ideal}.

$$D=D_{ideal}=\frac{V_o}{V_g} \tag{2.27}$$

The improved duty cycle *D* in (2.25) and ideal duty cycle D_{ideal} in (2.27) is plotted with respect to the desired output voltage (V_o) as shown in Fig. 2.4. It can clearly be observed that to obtain the desired output voltage, the actual duty cycle *D* should be greater than the ideal duty cycle (D_{ideal}). For example, to obtain desired output voltage 12 V with input voltage 20 V and load resistance 10 Ω, the duty cycle required for ideal buck converter is 0.6 whereas for the practical converter under consideration, the actual duty cycle should be 0.6415.

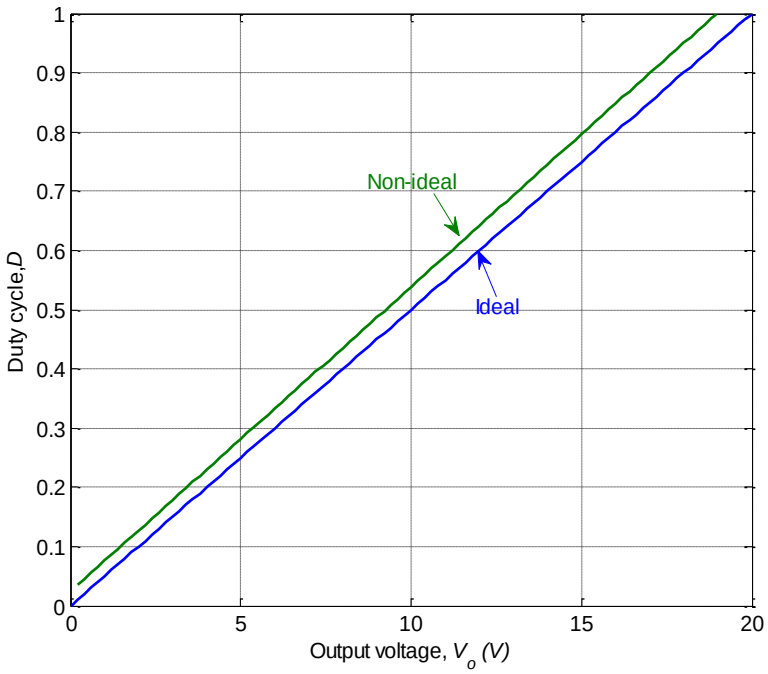


Fig. 2.4. Variation in duty cycle with desired output voltage

2.2.4 Inductor current ripple and inductor design

For any DC-DC converter, the inductor design is an important issue. The value of inductance basically depends upon the operating switching frequency and desired inductor current ripple. Let Δi_L be the desired inductor current ripper (ICR) and x_L be the desired inductor current ripple factor (ICRF) such that

$$x_L = \frac{\Delta i_L}{I_L} \tag{2.28}$$

Here, I_L is the average inductor current.

In steady-state, during switch-off, (2.9) can be written as:

$$L\frac{\Delta i_L}{\Delta t} = -\left(r_L + r_d\right)I_L - V_F - V_o \tag{2.29}$$

By substituting switch-off duration $\Delta t = D'T$, the magnitude of the inductor current ripple in steady-state will be

$$\Delta i_L = \frac{\left(r_d + r_L\right)I_L + V_F + V_o}{L} D'T \tag{2.30}$$

Further, substituting $T = \frac{1}{f}$ and $I_L = \frac{V_o}{R}$ from (2.17) into (2.30), we get

$$\Delta i_L = \frac{D'V_o}{Lf}\left(1 + \frac{r_L + r_d}{R} + \frac{V_F}{V_o}\right) \tag{2.31}$$

This is the expression for inductor current ripple for non-ideal buck converter.

Replacing $\Delta i_L = x_L I_L = x_L \frac{V_o}{R}$ in the above equation and simplifying, gives

$$\frac{x_L V_o}{R} = \frac{D'V_o}{Lf}\left(1+\frac{r_L+r_d}{R}+\frac{V_F}{V_o}\right) \Rightarrow L = \frac{D'R}{x_L f}\left(1+\frac{r_L+r_d}{R}+\frac{V_F}{V_o}\right) \tag{2.32}$$

Equation (2.32) gives the expression to design the inductance for desired inductor current ripple in terms of converter parameters and non-ideal elements. By substituting all non-idealities to zero and keeping $x_L=2$ gives the minimum value of inductance required for boundary conditions (between CCM and DCM) as below:

$$L = L_{ideal} = \frac{D'R}{2f} \tag{2.33}$$

This expression is same as available in literature [2], [3], [123].

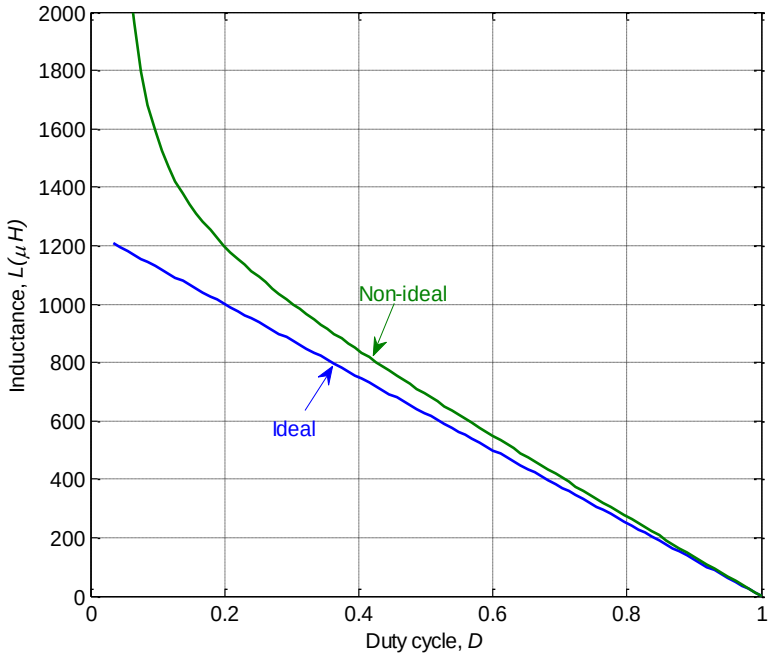


Fig. 2.5. Inductance variation with duty cycle for ideal and non-ideal buck converter

The value of inductance at different duty cycle is calculated for the two cases, *i.e.,* ideal and non-ideal buck converter and is plotted with respect to duty cycle as shown in Fig. 2.5. This figure clearly depicts that in the non-ideal case, the more inductance is required than the ideal case.

2.2.5 Output voltage ripple and capacitor design

Similar to inductor design, capacitor design is also an important aspect in designing the parameter of any DC-DC converter. In the buck converter, the voltage across the output capacitor is taken as the output voltage. Therefore, the design value of capacitance depends upon the desired output voltage ripple (OVR) and converter switching frequency. However, for a non-ideal DC-DC converter, the equivalent series resistance (ESR) of the capacitor also plays an important role in determining the capacitor design value. To determine the required capacitance value, the analysis of capacitor voltage ripple is necessary.

2.2.5.1 Analysis of output voltage ripple

In a non-ideal DC-DC buck converter, the effect of ESR of the capacitor is considered; therefore the output voltage ripple (Δv_o) consists of two parts [124]:

(a) Voltage ripple caused by the presence of ESR (Δv_{rc})

(b) Voltage ripple caused by the capacitor itself (Δv_c)

In steady-state, the capacitor current and corresponding voltage ripple waveforms are shown in Fig. 2.6. With the assumption that the load current (I_o) is ripple-free, the instantaneous capacitor current is equal to ($i_L(t)$- I_o).

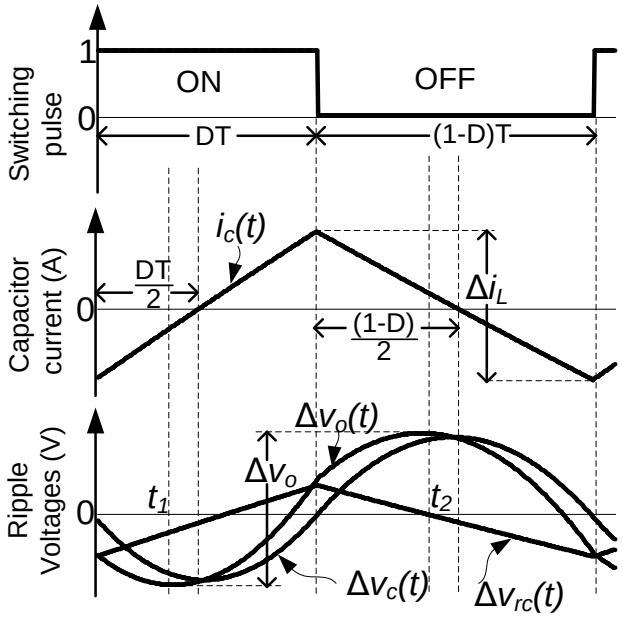


Fig. 2.6. Capacitor current and voltage ripple waveforms

***Analysis during switch-on* (*0 < t ≤ DT*):** When switch *S* is on, the capacitor current dynamics is given as [124]:

$$i_c(t) = \frac{\Delta i_L t}{DT} - \frac{\Delta i_L}{2} \tag{2.34}$$

The voltage drop across the ESR of capacitor is equal to ESR multiplied by capacitor current. Mathematically,

$$\Delta v_{rc}(t) = r_c i_c(t) \tag{2.35}$$

Substituting value of $i_c(t)$ from (2.34),we get

$$\Delta v_{rc}(t) = r_c\left(\frac{\Delta i_L t}{DT} - \frac{\Delta i_L}{2}\right) \tag{2.36}$$

The voltage ripple contribution due to capacitor itself is

$$\Delta v_c(t) = \frac{1}{C}\int_0^t i_c(t)\,dt + \Delta v_c(0) \tag{2.37}$$

Where, $\Delta v_c(0)$ is the initial ripple voltage across capacitor at t=0.

Substituting values of $i_c(t)$ from (2.34),

$$\Delta v_c(t) = \frac{1}{C}\int_0^t \left(\frac{\Delta i_L t}{DT} - \frac{\Delta i_L}{2}\right) dt + \Delta v_c(0) \tag{2.38}$$

Simplifying,

$$\Delta v_c(t) = \frac{\Delta i_L t}{2C}\left(\frac{t}{DT} - 1\right) + \Delta v_c(0) \tag{2.39}$$

Therefore, total output voltage ripple during switch-on period is the sum of voltage ripple due to ESR and voltage ripple due to capacitor itself *i.e.,*

$$\Delta v_o(t) = \Delta v_{rc}(t) + \Delta v_c(t) \tag{2.40}$$

Putting values from (2.36) and (2.39) gives

$$\Delta v_o(t) = r_c\left(\frac{\Delta i_L t}{DT} - \frac{\Delta i_L}{2}\right) + \frac{\Delta i_L t}{2C}\left(\frac{t}{DT} - 1\right) + \Delta v_c(0) \tag{2.41}$$

It can be seen from Fig. 2.6 that the minimum value of $\Delta v_o(t)$ during switch-on occurs at time t_1. To find out the minimum value of Δv_o during switch-on, (2.41) is differentiated with respect to time '*t*' and set equal to zero *i.e.,* [124]

$$\frac{d\Delta v_o(t)}{dt} = 0 \tag{2.42}$$

It gives,

$$t_1 = \frac{DT}{2} - r_c C \tag{2.43}$$

Substituting the value of t_1 from (2.43) into (2.36),(2.39) and (2.41) , we get

$$\Delta v_{rc}(t_1) = -\Delta i_L \frac{r_c^2 C}{DT} \tag{2.44}$$

$$\Delta v_c(t_1) = \Delta i_L\left(-\frac{DT}{8C} + \frac{r_c^2 C}{2DT}\right) + \Delta v_c(0) \tag{2.45}$$

$$\Delta v_o(t_1) = -\Delta i_L\left(\frac{DT}{8C} + \frac{r_c^2 C}{2DT}\right) + \Delta v_c(0) \tag{2.46}$$

***Analysis during switch-off* (*DT* < *t* ≤ *T*):** When switch *S* is off, the capacitor current dynamics is given as [124] :

$$i_c(t) = \frac{-\Delta i_L(t - DT)}{D'T} + \frac{\Delta i_L}{2} \tag{2.47}$$

The voltage ripple contribution due to ESR of the capacitor during switch-off is

$$\Delta v_{rc}(t) = r_c i_c(t) = r_c\left(\frac{-\Delta i_L(t - DT)}{D'T} + \frac{\Delta i_L}{2}\right) \tag{2.48}$$

The voltage ripple contribution due to capacitor itself is

$$\Delta v_c(t) = \frac{1}{C}\int_{DT}^t i_c(t) dt + \Delta v_c(DT) \tag{2.49}$$

Where, $\Delta v_c(DT)$ is the initial ripple voltage across capacitor at *t*=DT.

Substituting values of $i_c(t)$ from (2.47),

$$\Delta v_c(t) = \frac{1}{C}\int_{DT}^{t}\left(\frac{-\Delta i_L(t-DT)}{D'T} + \frac{\Delta i_L}{2}\right)dt + \Delta v_c(DT) \tag{2.50}$$

On simplifying,

$$\Delta v_c(t) = \frac{\Delta i_L(t-DT)}{2C}\left(\frac{-(t-DT)}{D'T} + 1\right) + \Delta v_c(DT) \tag{2.51}$$

Therefore, total output voltage ripple during switch-off period is the sum of voltage ripple due to ESR and voltage ripple due to capacitor itself *i.e.,*

$$\Delta v_o(t) = \Delta v_{rc}(t) + \Delta v_c(t) \tag{2.52}$$

Putting values from (2.48) and (2.51) gives

$$\Delta v_o(t) = r_c\left(\frac{-(t-DT)\Delta i_L}{D'T} + \frac{\Delta i_L}{2}\right) + \frac{\Delta i_L(t-DT)}{2C}\left(\frac{-(t-DT)}{D'T} + 1\right) + \Delta v_c(DT) \tag{2.53}$$

It is seen from Fig. 2.6 that the maximum value of $\Delta v_o(t)$ during switch-off occurs at time t_2. To find out this maximum value, (2.53) is differentiated with respect to time '*t*' and is made equal to zero *i.e.,* [124]

$$\frac{d\Delta v_o(t)}{dt} = 0 \tag{2.54}$$

This gives,

$$t_2 = \frac{(1+D)T}{2} - r_c C \tag{2.55}$$

Substituting the value of t_2 from (2.55) into (2.48),(2.51) and (2.53) , we get

$$\Delta v_{rc}(t_2) = \Delta i_L \frac{r_c^2 C}{(1-D)T}, \tag{2.56}$$

$$\Delta v_c(t_2) = \Delta i_L\left(\frac{D'T}{8C} - \frac{r_c^2 C}{2D'T}\right) + \Delta v_c(DT) \tag{2.57}$$

$$\Delta v_o(t_2) = \Delta i_L\left(\frac{D'T}{8C} + \frac{r_c^2 C}{2D'T}\right) + \Delta v_c(DT) \tag{2.58}$$

Therefore, the peak-to-peak value of output ripple voltages will be

$$\Delta v_o = \Delta v_o(t_2) - \Delta v_o(t_1) \tag{2.59}$$

Substituting values from (2.46) and (2.58), we get

$$\Delta v_o = \left[\Delta i_L\left(\frac{D'T}{8C} + \frac{r_c^2 C}{2D'T}\right) + \Delta v_c(DT)\right] - \left[-\Delta i_L\left(\frac{DT}{8C} + \frac{r_c^2 C}{2DT}\right) + \Delta v_c(0)\right] \tag{2.60}$$

In steady-state, the capacitor voltage ripple, $\Delta v_c(DT) = \Delta v_c(0)$.

Simplifying (2.60) gives

$$\Delta v_o = \Delta i_L \left(\frac{1}{8fC} + \frac{r_c^2 Cf}{2DD'} \right) \tag{2.61}$$

If $r_c=0$ is substituted in (2.61), the output voltage ripple is same as obtained in the ideal case (without considering the effect of capacitor ESR) [3], [123].

The contribution of ESR voltage ripple and capacitor voltage ripple in peak-to-peak output voltage ripple can also be found as follows:

The ripple voltage contribution due to ESR is

$$\Delta v_{rc} = \Delta v_{rc}(t_2) - \Delta v_{rc}(t_1) \tag{2.62}$$

Substituting values from (2.44) and (2.56),

$$\Delta v_{rc} = \Delta i_L \frac{r_c^2 Cf}{DD'} \tag{2.63}$$

Similarly, the ripple voltage contribution due to the capacitor is

$$\Delta v_c = \Delta v_c(t_2) - \Delta v_c(t_1) \tag{2.64}$$

Substituting values from (2.45) and (2.57),

$$\Delta v_c = \Delta i_L \left(\frac{1}{8fC} - \frac{r_c^2 Cf}{2DD'} \right) \tag{2.65}$$

It can be observed that the total peak-peak output voltage ripple is the sum of two individual voltage ripple given in (2.63) and (2.65).

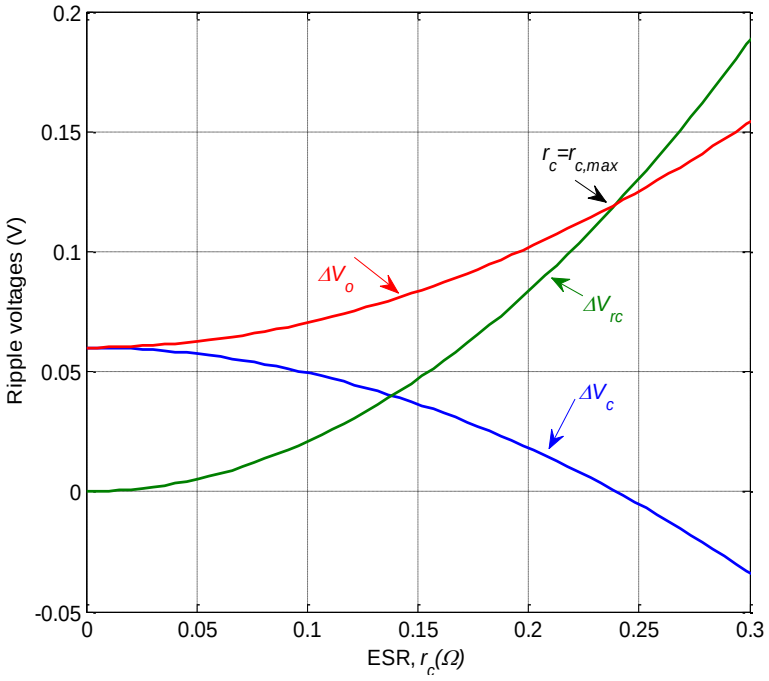


Fig. 2.7. Variations in different voltage ripple with capacitor ESR

These three ripple voltage variations defined in (2.61),(2.63) and (2.65) are plotted with respect to ESR as shown in Fig. 2.7. From this figure, it is observed that with an increase in ESR, Δv_{rc} increases at a faster rate than Δv_c decreases, thereby net increase in Δv_o.

However, as value of r_c increases beyond $r_{c,max}$, the voltage ripple Δv_{rc} becomes higher than Δv_o, which is practically impossible. It implies that the capacitor is no longer able to keep output voltage ripple within specified limit for $r_c > r_{c,max}$. This figure shows that as long as the capacitor ESR value is less than $r_{c,max}$, the output voltage ripple is less than 0.12 V as desired (within 1% of output voltage). The analytical relationship for this $r_{c,max}$ is derived in the forthcoming section.

2.2.5.2 Output capacitor design

Let the specified maximum output voltage ripple is Δv_{om}. The capacitor should be designed such that the following condition must satisfy:

$$\Delta v_o \le \Delta v_{om} \tag{2.66}$$

By substituting value of Δv_o from (2.61),

$$\Delta i_L \left(\frac{1}{8fC} + \frac{r_c^2 Cf}{2DD'} \right) \le \Delta v_{om} \tag{2.67}$$

Upon simplifying, we get

$$r_c^2 C^2 - \frac{2DD'}{f} \left(\frac{\Delta v_{om}}{\Delta i_L} \right) C + \frac{DD'}{4f^2} \le 0 \tag{2.68}$$

This is a quadratic constraint in C. Its solution is obtained to get the minimum value of capacitor C as:

$$C_{\min} = \frac{\frac{2DD'}{f}\left(\frac{\Delta v_{om}}{\Delta i_L} \right) - \sqrt{\left(\frac{2DD'}{f}\left(\frac{\Delta v_{om}}{\Delta i_L} \right) \right)^2 - 4r_c^2 \frac{DD'}{4f^2}}}{2r_c^2} \tag{2.69}$$

This expression gives the required minimum value of capacitance C with $r_c \le r_{c,max}$.

2.2.5.3 Derivation of maximum permissible ESR ($r_{c,max}$)

As discussed previously, the value of ESR affects the capacitor design to meet the desired output voltage ripple requirements. In (2.61), the additional term $\frac{r_c^2 Cf \Delta i_L}{2DD'}$ appears due to the presence of ESR. It suggests that as ESR increases, the output voltage ripple also increases and if ESR of the capacitor is not chosen properly, it may increase the output voltage ripple beyond the desired value. Therefore, it becomes necessary to evaluate the maximum permissible value of this ESR for desired output voltage ripple at given converter switching frequency. In this section, this maximum value is derived analytically.

In (2.69), C_{min} to be a real quantity the following condition must satisfy:

$$\left(\frac{2DD'}{f}\left(\frac{\Delta v_{om}}{\Delta i_L} \right) \right)^2 - 4r_c^2 \frac{DD'}{4f^2} \ge 0 \tag{2.70}$$

The simplification of the above inequality gives

$$r_c \le 2\sqrt{DD'}\,\frac{\Delta v_{om}}{\Delta i_L} \tag{2.71}$$

Therefore, the maximum permissible value of ESR ($r_{c,max}$) for the desired output voltage ripple (Δv_{om}) and inductor current ripple (Δi_L) will be

$$r_{c,\max} = 2\sqrt{DD'}\,\frac{\Delta v_{om}}{\Delta i_L} \tag{2.72}$$

This expression gives the maximum permissible value of capacitor ESR which will result output voltage ripple within the desired limit. If ESR value is greater than $r_{c,max}$ in (2.72), then the capacitor will not be able to keep the steady-state output voltage ripple in specified limit. This is also verified by experimental results in the next section.

Substituting (2.72) into (2.69) gives the minimum (worst) value of capacitor C with r_c=$r_{c,max}$ as

$$C_{\min}\big|_{r_c=r_{c,\max}} = \frac{1}{4f}\,\frac{\Delta i_L}{\Delta v_{om}} \tag{2.73}$$

By letting r_c=0 in (2.61), the minimum value of ideal capacitance should be

$$C_{\min}\big|_{r_c=0} = \frac{1}{8f}\,\frac{\Delta i_L}{\Delta v_{om}} \tag{2.74}$$

Equation (2.73) gives the minimum value of capacitance required for worst case ESR ($r_{c,max}$), whereas (2.74) gives the minimum value of the capacitor for an ideal case (r_c=0) [123], [125]. It is observed that the capacitor value required in the worst case is double of ideal case. The variation in minimum value of capacitance as a function of ESR is drawn in Fig. 2.8 using (2.69). From this figure, it is evident that the required capacitor value increases with increase in ESR and at r_c = $r_{c,max}$, it becomes double of capacitance value with r_c=0. For r_c > $r_{c,max}$, the capacitance value is a complex number. However, only the real part is plotted by MATLAB simulation as shown in this figure.

Substituting the values of Δi_L from (2.31) into (2.72),

$$r_{c,\max} = 2\sqrt{DD'}\,\frac{\Delta v_{om}}{\dfrac{D'V_o}{Lf}\left(1+\dfrac{r_L+r_d}{R}+\dfrac{V_F}{V_o}\right)} \tag{2.75}$$

Rearranging,

$$r_{c,\max} = 2\sqrt{\frac{D}{D'}}\,\frac{\left(\Delta v_{om}/V_o\right)Lf}{\left(1+\dfrac{V_F}{V_o}+\dfrac{r_L+r_d}{R}\right)} \tag{2.76}$$

This relation depicts that for specified output voltage ripple, the maximum permissible value of ESR ($r_{c,max}$) is proportional to switching frequency. Therefore, as the switching frequency of converter increases, the power supply designer is allowed to use the high ESR capacitor without violating the output voltage ripple constraint. Fig. 2.9 shows the variation in $r_{c,max}$ with frequency. It is observed that if switching frequency is 50 kHz, the designer may

use capacitor with ESR of 0.6 Ω whereas with 20 kHz switching frequency, this value is limited to 0.24 Ω. It is also to note that as frequency increases, required capacitor value also decreases.

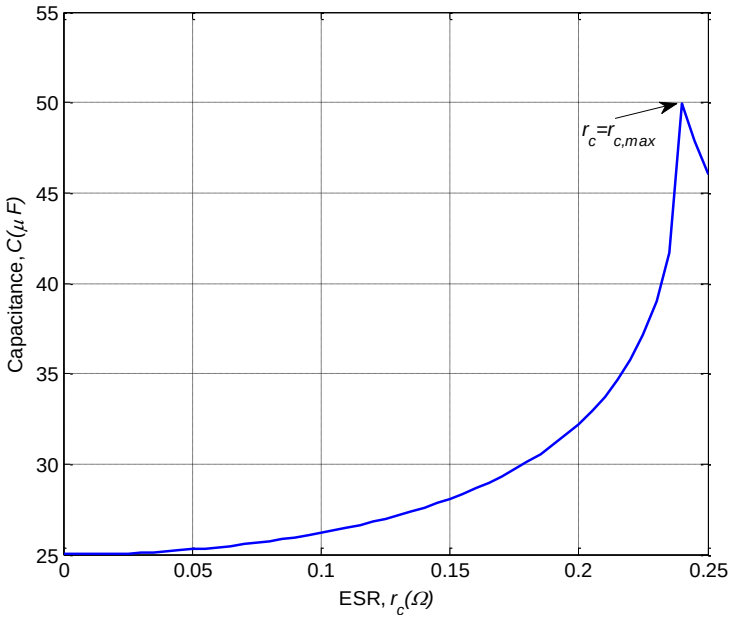


Fig. 2.8. Variation in minimum capacitance value versus ESR

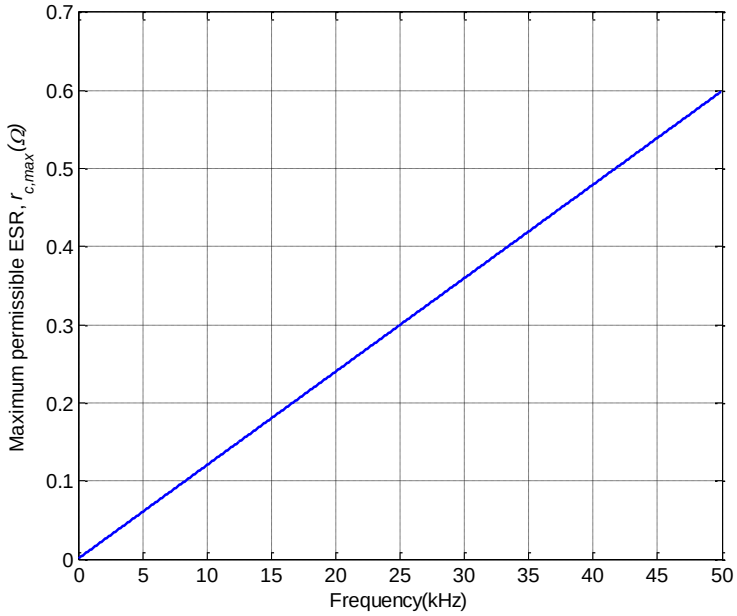


Fig. 2.9. Maximum permissible ESR ($r_{c,max}$) versus frequency

2.2.6 Results and discussion

The aforementioned theoretical studies are simulated using MATLAB/Simulink and are validated on an experimental prototype of DC-DC buck converter. For this purpose, the DC-DC buck converter parameters are used same as specified in Table 2.1. For these specifications, the duty cycle calculated using (2.25) is 0.6415, which is greater than the ideal duty cycle (=0.6). For this actual duty cycle, inductance value is calculated as 490 μH using (2.32), whereas using the ideal relation it is 448 μH. The maximum value of ESR ($r_{c,max}$) is

calculated 0.2398 Ω using (2.72) for desired output voltage ripple and output voltage ripple at switching frequency as specified in Table 2.1. The minimum (worst) value of capacitance (C_{min}) is computed 50 µF using (2.73), which is 25 µF in case of ideal capacitor.

The simulated result for output voltage with ideal and actual duty cycle is shown in Fig. 2.10. These simulation results show that for ideal duty cycle D=0.6, the output voltage is 11.2 V and for actual duty cycle D=0.6415, the output voltage is settled to 12 V (as desired).

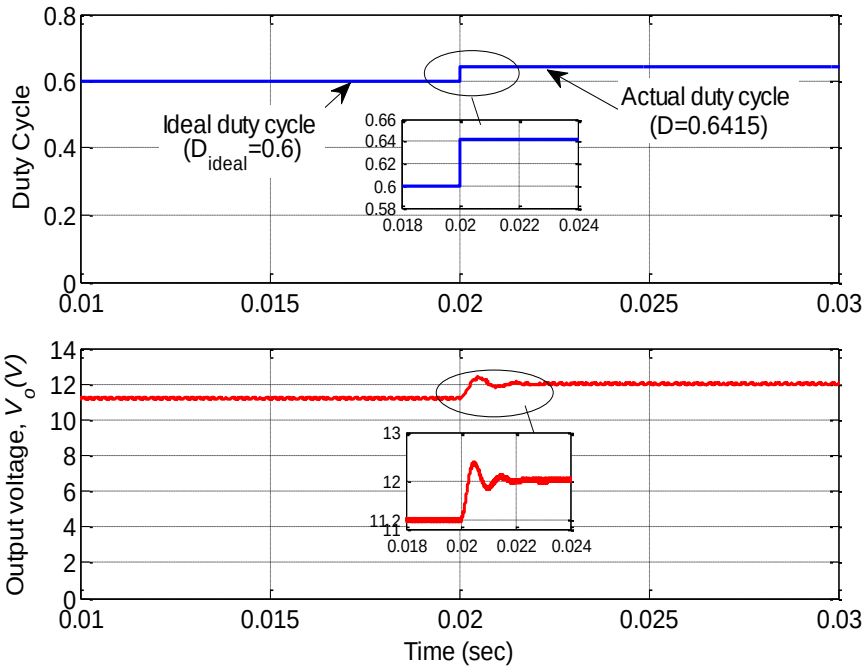


Fig. 2.10. Simulated output voltage response with ideal and improved duty cycles

Further, to investigate the effect of ESR variation on output voltage ripple, the four cases are discussed for different values of ESR. In each case, total output voltage ripple Δv_o, ripple voltage due to capacitor Δv_c and ripple voltage due to ESR Δv_{rc} are evaluated and plotted for a duration of two switching periods as discussed below:

***Case 1* (r_c = 0):** In this case, the capacitor is considered to be ideal with no ESR. However, it is very difficult to have such capacitor in practice. The ripple voltage contribution due to ESR is zero in this case. Therefore, the output voltage ripple Δv_o is same as Δv_c. These voltage ripple are shown in Fig. 2.11 (a). The peak-to-peak output voltage ripple is 0.06 V, which is half of the maximum allowed output voltage ripple (0.12 V).

***Case 2* (r_c = 0.1Ω < $r_{c,max}$):** For this case, the ESR is taken less than the maximum permissible value. The three simulated voltage ripple are displayed in Fig. 2.11 (b). Due to the presence of ESR, the peak-to-peak output voltage ripple is increased to 0.07 V. However, it is smaller than the maximum allowed output voltage ripple (0.12 V).

***Case 3* (r_c = $r_{c,max}$ = 0.2398 Ω):** If the capacitor ESR becomes equal to maximum permissible ESR, the corresponding simulated voltage ripple would be as shown in Fig. 2.11 (c). The ripple voltage contribution due to ESR increases, resulting in increased output voltage ripple.

The peak-to-peak output voltage ripple reaches to 0.12 V, which is equal to the maximum allowed value.

***Case 4* (r_c = 0.4 Ω > $r_{c,max}$):** This case studies the effect of ESR on output voltage ripple, if ESR is selected greater than the maximum permissible value. As shown in Fig. 2.11 (d), the voltage ripple due to ESR further increases such that the total peak-to-peak output voltage ripple becomes 0.19 V. However, this value of output voltage ripple is greater than the maximum allowed value (0.12 V) and therefore, does not meet the user specified output voltage ripple limit.

In order to verify these theoretical and simulation results, an experimental prototype of DC-DC buck converter has been developed. The measured parasitic resistances have already been specified in Table 2.1. The detailed description of prototype development is described in Appendix *B*.

The experimental results of output voltage response with the ideal duty cycle D=0.6 and actual (improved) duty cycle D=0.642 is shown in Fig. 2.12. These results indicate that the output voltage is 11.2 V with ideal duty cycle, not 12 V as desired. This is because of voltage drop across the converter non-idealities. However, with improved duty cycle the output voltage reaches to 12 V because the increased duty cycle forces the MOSFET switch to remain on for some extra time.

Fig. 2.13 shows the experimental results for output voltage ripple of DC-DC buck converter for different cases of ESR. Experimentally, the output voltage ripple has been validated for two cases of capacitor ESR: $r_c<r_{c,max}$ (r_c= 0.1 Ω) and $r_c>r_{c,max}$ (r_c= 0.4 Ω). As shown in Fig. 2.13 (a), the output voltage ripple for r_c= 0.1 Ω is 0.075 V, which is within desired output voltage ripple limit. The output voltage ripple for r_c= 0.4 Ω is 0.19 V as shown in Fig. 2.13 (b), which is beyond the maximum specified limit. It is to be observed that the experimental results match the simulation results closely.

Further, the variation of output voltage ripple with switching frequency at different ESR is also experimentally validated. The purpose to show these results is that a high ESR value can be used to limit the output voltage ripple within desired limit, if the converter switching frequency is increased. Fig. 2.14 (a)-(c) shows the output voltage ripple variation with switching frequency with ESR 0.1 Ω, 0.35 Ω and 0.5 Ω respectively. These results show that at 20 kHz the output voltage ripple is within 0.12 V limit for r_c= 0.1 Ω, but not for r_c= 0.35 Ω and r_c= 0.5 Ω. However, if switching frequency is greater than 30 kHz for r_c= 0.35 Ω and greater than 50 kHz for r_c= 0.5 Ω, the output voltage ripple is obtained within specified limit (0.12 V). It verifies that if the converter operates at a higher frequency, the output voltage will still remain within specified limit even with the higher ESR value. From these results, it can also be observed that for a fixed ESR, as the switching frequency is increasing, the output voltage

ripple is decreasing. Similarly, at a fixed switching frequency, the output voltage ripple decreases with decrease in ESR.

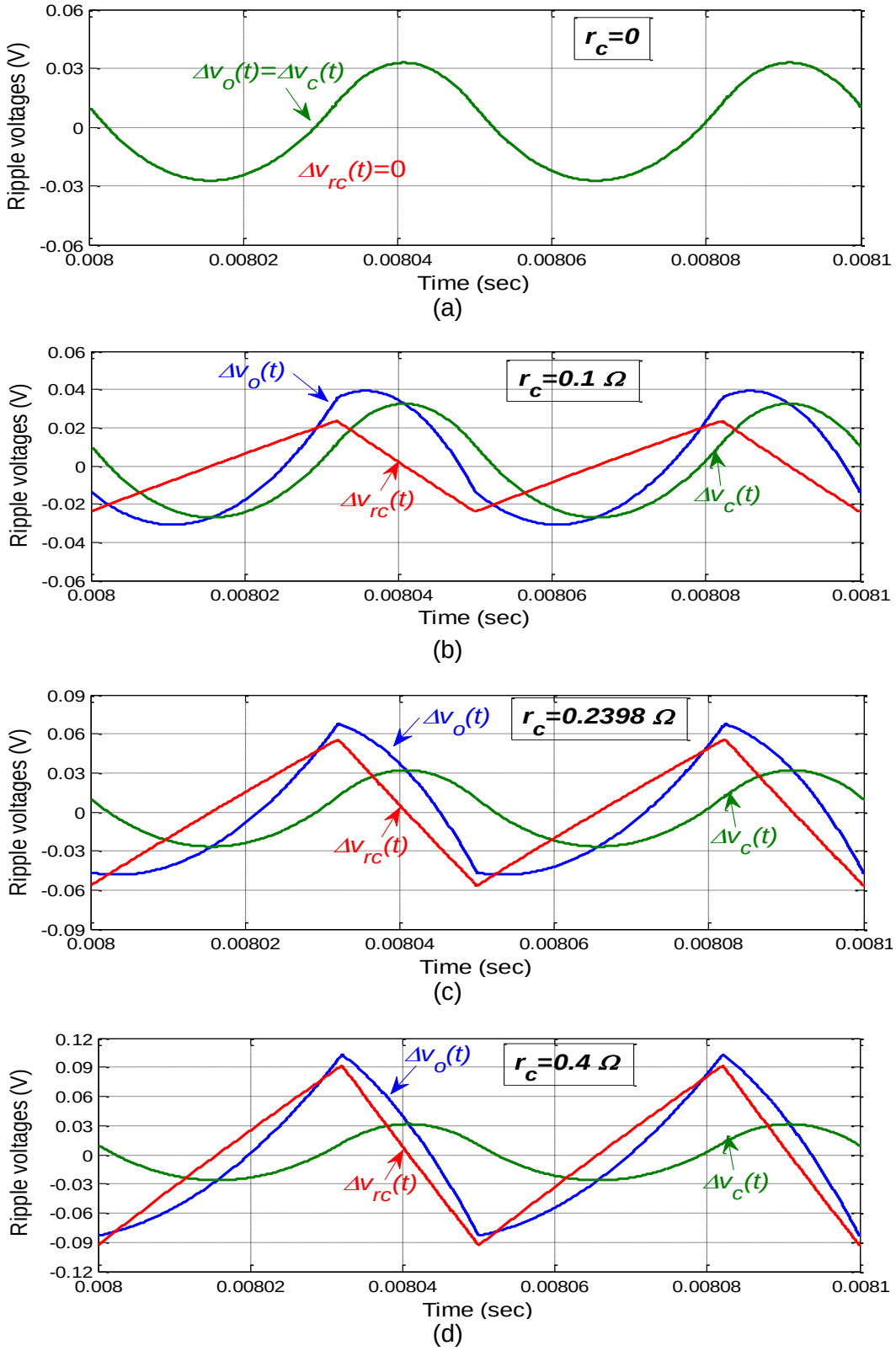


Fig. 2.11. Simulated voltage ripple waveforms for different ESR values (a) r_c=0 (b) r_c=0.1 Ω (r_c<$r_{c,max}$) (c) r_c=0.2398 Ω (r_c=$r_{c,max}$) (d) r_c=0.4 Ω (r_c>$r_{c,max}$)

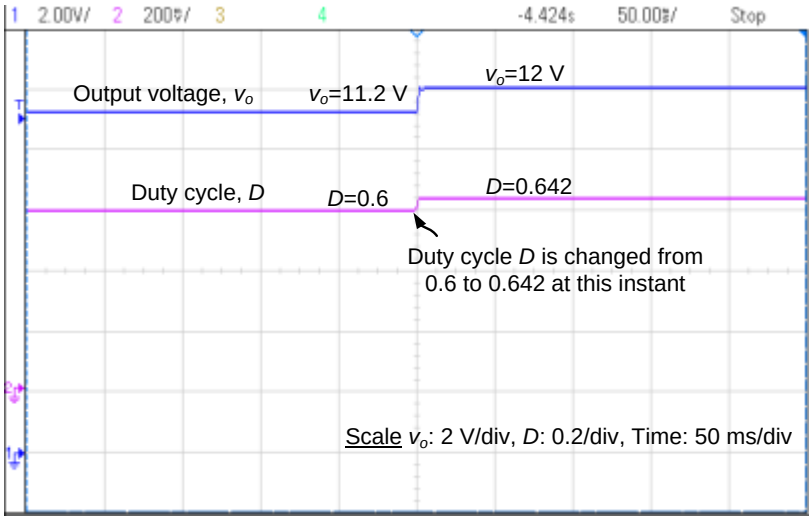
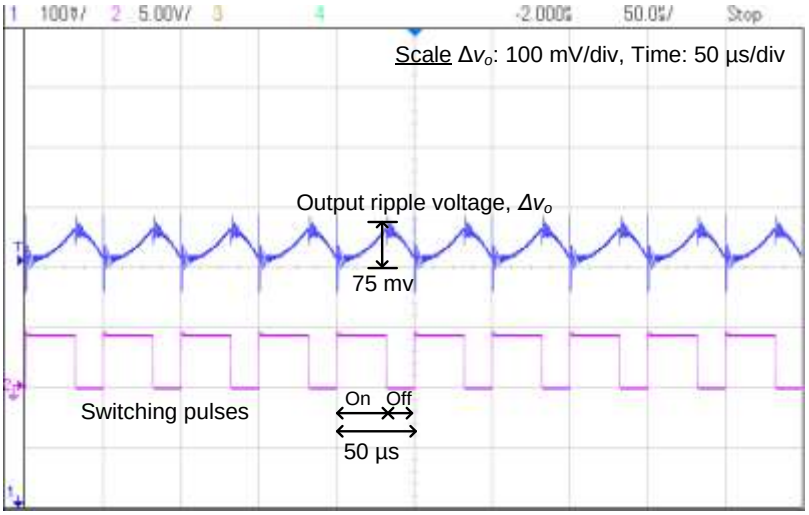
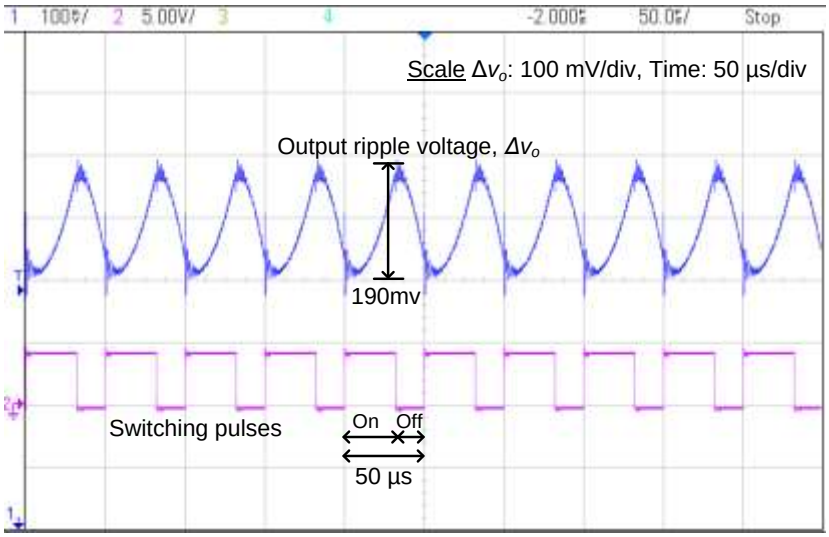


Fig. 2.12. Experimental results of output voltage response with ideal duty cycle (0.6)and improved duty cycle (0.642)

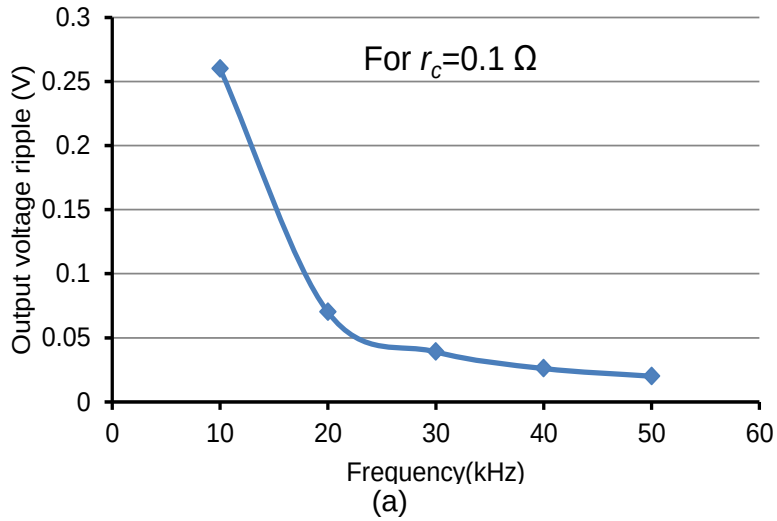


(a)

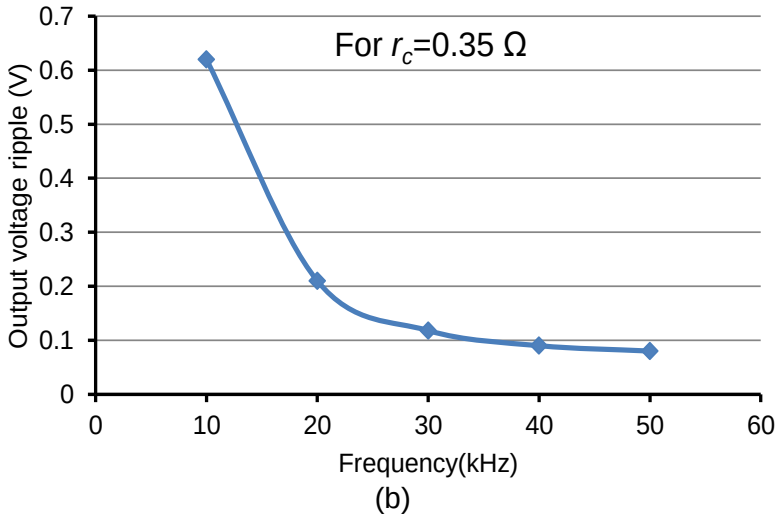


(b)

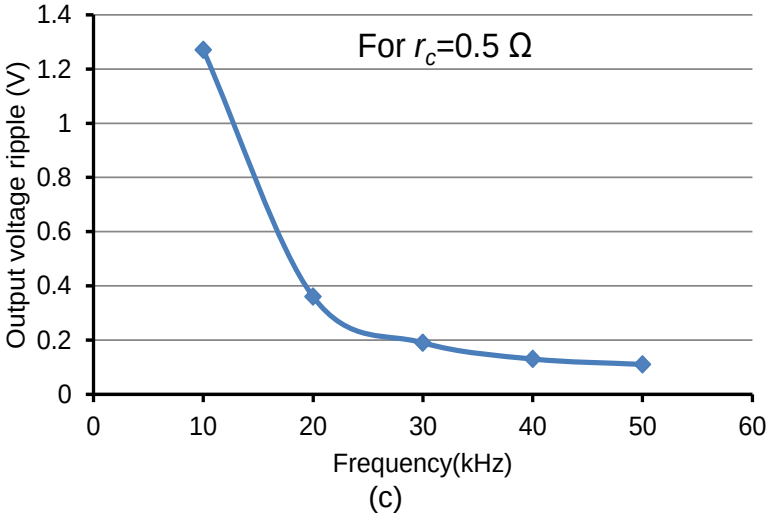
Fig. 2.13. Experimental results for output voltage ripple with (a) r_c=0.1 Ω (r_c<$r_{c,max}$) and (b) r_c=0.4 Ω (r_c>$r_{c,max}$)



(a)



(b)



(c)

Fig. 2.14. Experimental results of output voltage ripple variation with frequency with (a) r_c=0.1 Ω (b) r_c=0.35 Ω (c) r_c=0.5 Ω

2.3 Analysis of Non-ideal DC-DC Cuk Converter

The basic circuit of a non-ideal DC-DC Cuk converter is depicted in Fig. 2.15(a). For DC-DC Cuk converter, the magnitude of DC output voltage can be lower, equal or higher than the DC input voltage depending upon the duty cycle but polarity will always be opposite to the input voltage. It comprises of a MOSFET switch *S*, diode D_d, two inductors L_1 , L_2, two capacitors C_1 , C_2 and load resistor *R*. For the precise analysis and design of the converter parameters, the elements responsible for power loss have been considered. These elements are switch on-resistance (r_{sw}), diode forward resistance (r_d), diode forward voltage drop (V_F), equivalent series resistance (ESR) of inductors (r_{L1} and r_{L2} for L_1 and L_2, respectively) and ESR of capacitors (r_{c1} and r_{c2} for capacitors C_1 and C_2, respectively). In ideal Cuk converter, the values of these elements are zero [123], [126]. Similar to DC-DC buck converter, the DC-DC Cuk converter can also operate in two modes: continuous conduction mode (CCM) and discontinuous conduction mode (DCM). However, in subsequent discussion, the converter is assumed to be operating in CCM. In CCM, DC-DC Cuk converter has two circuit modes: (a) when switch is on for the duration *DT* and (b) when the switch is off for the duration *(1-D)T*. Here, *D* is duty cycle and *T* is period of one switching cycle (=1/f_s, f_s is switching frequency).

When the switch is on during *DT* period, voltage v_{c1} reverse biases diode D_d and capacitor C_1 is discharged through the capacitor C_2 and load *R*. The inductor L_2 also stores energy from capacitor C_1 .The inductor L_1 stores energy from input source V_g. In this mode, the capacitor C_2 is discharged initially by the load resistance and then charged by energy stored in capacitor C_1. When the switch is off during *(1-D) T* period, diode D_d is forward biased and conducts. The capacitor C_1 is charged through input current and inductor L_2 dissipates its energy to load and capacitor C_2. The capacitor C_2 is charged initially by the energy stored in inductor L_2 and then discharged by load current. The important waveforms for DC-DC Cuk converter are given in Fig. 2.15(d). The mathematical analysis of these two modes is given below:

2.3.1 When the switch is on (time interval $0 < t \leq DT$)

For time interval $0<t\leq DT$, the equivalent circuit diagram is shown in Fig. 2.15(b). As shown, in this mode, the MOSFET switch *S* is on and the diode D_d is reverse biased. The switch is characterized by its on-resistance r_{sw} and diode as an open circuit. The switch current (i_{sw}) is sum of both the inductor currents (i_{L1} and i_{L2}). The diode current (i_D) is zero. Using Kirchhoff's voltage law (KVL), the voltage across inductors L_1 and L_2 are given as:

$$v_{L1,on}(t) = L_1 \frac{di_{L1}(t)}{dt} = -(r_{L1} + r_{sw}) i_{L1}(t) - r_{sw} i_{L2}(t) + V_g \tag{2.77}$$

$$v_{L2,on}(t) = L_2 \frac{di_{L2}(t)}{dt} = -r_{sw} i_{L1}(t) - (r_{L2} + r_{c1} + r_{sw}) i_{L2}(t) + v_{c1}(t) - v_o(t) \tag{2.78}$$

Using Kirchhoff's current law (KCL), the current through capacitors C_1 and C_2 are given as:

$$i_{c1,on}(t) = C_1 \frac{dv_{c1}(t)}{dt} = -i_{L2}(t) \tag{2.79}$$

$$i_{c2,on}(t) = i_{L2}(t) - \frac{v_o(t)}{R} \tag{2.80}$$

The output voltage is

$$v_{o,on}(t) = v_{c2}(t) + r_{c2} i_{c2}(t) \tag{2.81}$$

2.3.2 When the switch is off (time interval $DT < t \leq T$)

During the time interval $DT < t \leq T$, the MOSFET switch S is off and diode D_d is forward biased. The corresponding equivalent circuit is shown in Fig. 2.15(c). In this duration, the diode is modeled by resistance r_d and forward voltage V_F . The MOSFET switch is open circuit. The diode current (i_D) is sum of both the inductor currents (i_{L1} and i_{L2}). The switch current (i_{sw}) is zero.

Using Kirchhoff's voltage law (KVL), the voltage across inductors L_1 and L_2 are given as:

$$v_{L1,off}(t) = L_1 \frac{di_{L1}(t)}{dt} = -(r_{L1} + r_{c1} + r_d) i_{L1}(t) - r_d i_{L2}(t) - v_{c1}(t) + V_g - V_F \tag{2.82}$$

$$v_{L2,off}(t) = L_2 \frac{di_{L2}(t)}{dt} = -r_d i_{L1}(t) - (r_{L2} + r_d) i_{L2}(t) - v_o(t) - V_F \tag{2.83}$$

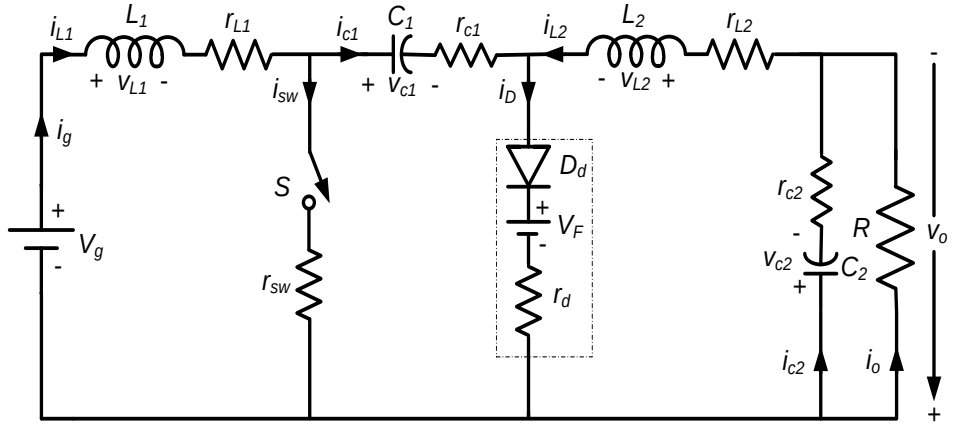
Using Kirchhoff's current law (KCL), the current through capacitors C_1 and C_2 are given as:

$$i_{c1,off}(t) = C_1 \frac{dv_{c1}(t)}{dt} = i_{L1}(t) \tag{2.84}$$

$$i_{c2,off}(t) = i_{L2}(t) - \frac{v_o(t)}{R} \tag{2.85}$$

The output voltage is

$$v_{o,off}(t) = v_{c2}(t) + r_{c2} i_{c2}(t) \tag{2.86}$$



(a)

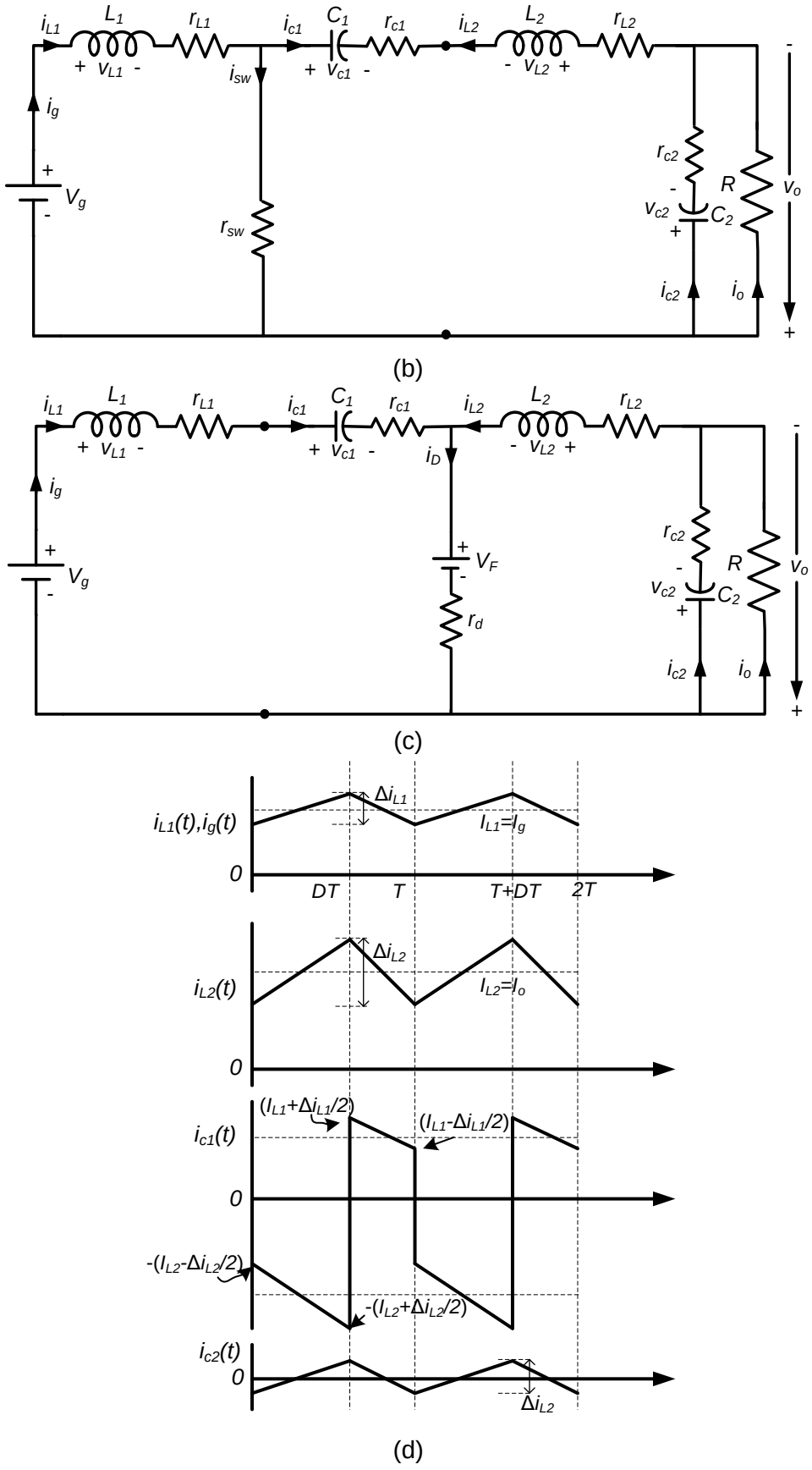


Fig. 2.15. (a) Basic circuit of a non-ideal DC-DC Cuk converter (b) equivalent circuit when the switch is on (c) equivalent circuit when the switch is off (d) associated waveforms

2.3.3 Steady-state analysis

For steady-state analysis, the average value Z of a current and voltage variable $z(t)$ can be given as [3]:

$$Z = \frac{1}{T}\int_0^T z(t)dt = \frac{1}{T}\int_0^{DT} z_{on}(t)dt + \frac{1}{T}\int_{DT}^{T} z_{off}(t)dt \tag{2.87}$$

Where, $z_{on}(t)$ and $z_{off}(t)$ are the variable $z(t)$ during switch ON and switch OFF, respectively.

In steady-state, according to the principle of inductor volt-second balance, the average inductor voltage must be equal to zero. Therefore,

For inductor L_1,

$$V_{L1} = \frac{1}{T}\int_0^T v_{L1}(t)dt = \frac{1}{T}\int_0^{DT} v_{L1,on}(t)dt + \frac{1}{T}\int_{DT}^{T} v_{L1,off}(t)dt = 0 \tag{2.88}$$

Substituting values from (2.77),(2.82) and simplifying, we get

$$V_{L1} = D\left[-(r_{L1}+r_{sw})I_{L1} - r_{sw}I_{L2} + V_g\right] + (1-D)\left[-(r_{L1}+r_{c1}+r_d)I_{L1} - r_dI_{L2} - V_{c1} + V_g - V_F\right] = 0$$

$$\Rightarrow V_{c1} = \frac{V_g}{D'} - V_F - \frac{(r_{L1}+D'r_{c1}+r_x)I_{L1}}{D'} - \frac{r_xI_{L2}}{D'} \tag{2.89}$$

For inductor L_2,

$$V_{L2} = \frac{1}{T}\int_0^T v_{L2}(t)dt = \frac{1}{T}\int_0^{DT} v_{L2,on}(t)dt + \frac{1}{T}\int_{DT}^{T} v_{L2,off}(t)dt = 0 \tag{2.90}$$

Substituting values from (2.78),(2.83) and simplifying, we get

$$V_{L2} = D\left[-r_{sw}I_{L1} - (r_{L2}+r_{c1}+r_{sw})I_{L2} + V_{c1} - V_o\right] + (1-D)\left[-r_dI_{L1} - (r_{L2}+r_d)I_{L2} - V_o - V_F\right] = 0$$

$$\Rightarrow V_o = DV_{c1} - D'V_F - r_xI_{L1} - (r_{L2}+Dr_{c1}+r_x)I_{L2} \tag{2.91}$$

Similarly, in the steady-state, according to the principle of capacitor charge-balance the average capacitor current must be equal to zero. Therefore,

For capacitor C_1,

$$I_{c1} = \frac{1}{T}\int_0^T i_{c1}(t)dt = \frac{1}{T}\int_0^{DT} i_{c1,on}(t)dt + \frac{1}{T}\int_{DT}^{T} i_{c1,off}(t)dt = 0 \tag{2.92}$$

Substituting values from (2.79),(2.84) and simplifying, we write

$$I_{c1} = D(-I_{L2}) + (1-D)(I_{L1}) = 0 \Rightarrow I_{L1} = \frac{D}{D'}I_{L2} \tag{2.93}$$

For capacitor C_2,

$$I_{c2} = \frac{1}{T}\int_0^T i_{c2}(t)dt = \frac{1}{T}\int_0^{DT} i_{c2,on}(t)dt + \frac{1}{T}\int_{DT}^{T} i_{c2,off}(t)dt = 0 \tag{2.94}$$

Substituting values from (2.80),(2.85) and simplifying gives,

$$I_{c2} = D\left(I_{L2} - \frac{V_o}{R}\right) + (1-D)\left(I_{L2} - \frac{V_o}{R}\right) = 0 \Rightarrow I_{L2} = \frac{V_o}{R} \tag{2.95}$$

The average output voltage of DC-DC Cuk converter will be

$$V_o = \frac{1}{T}\int_0^T v_o(t)dt = \frac{1}{T}\int_0^{DT} v_{o,on}(t)dt + \frac{1}{T}\int_{DT}^{T} v_{o,off}(t)dt \tag{2.96}$$

Substituting values from (2.81),(2.86) and simplifying, we get

$$V_o = D\left(V_{c2} + r_{c2}I_{c2}\right) + \left(1-D\right)\left(V_{c2} + r_{c2}I_{c2}\right) \Rightarrow V_o = V_{c2} \tag{2.97}$$

2.3.3.1 Expression for output voltage

Replacing the values of I_{L2} from (2.95) into (2.89), we have

$$V_{c1} = \frac{V_g}{D'} - V_F - \frac{\left(Dr_{L1} + DD'r_{c1} + r_x\right)I_{L2}}{D'^2} \tag{2.98}$$

Now substituting values of I_{L1}, I_{L2} and V_{c1} from (2.93), (2.95) and (2.98), respectively into (2.91) , we have

$$V_o = D\left[\frac{V_g}{D'} - V_F - \frac{\left(Dr_{L1} + DD'r_{c1} + r_x\right)}{D'^2}\frac{V_o}{R}\right] - D'V_F - r_x\frac{D}{D'}\frac{V_o}{R} - \left(r_{L2} + Dr_{c1} + r_x\right)\frac{V_o}{R}$$

$$\Rightarrow V_o = \frac{D}{D'}V_g - V_F - \frac{V_o}{R}\left(\left(\frac{D}{D'}\right)^2 r_{L1} + r_{L2} + \frac{Dr_{c1}}{D'} + \frac{r_x}{D'^2}\right)$$

$$\Rightarrow V_o = \frac{\frac{D}{D'}V_g - V_F}{1 + \frac{1}{R}\left(\left(\frac{D}{D'}\right)^2 r_{L1} + r_{L2} + \frac{Dr_{c1}}{D'} + \frac{r_x}{D'^2}\right)} \tag{2.99}$$

or

$$\Rightarrow V_o = \frac{\frac{D}{D'}V_g}{1 + \frac{V_F}{V_o} + \frac{1}{R}\left(\left(\frac{D}{D'}\right)^2 r_{L1} + r_{L2} + \frac{Dr_{c1}}{D'} + \frac{r_x}{D'^2}\right)} \tag{2.100}$$

Here, $r_x = Dr_{sw} + D'r_d$

The output voltage of ideal DC-DC Cuk converter is [125]

$$V_o = \frac{D}{D'}V_g \tag{2.101}$$

Similar to ideal DC-DC buck converter, the output voltage of ideal DC-DC Cuk converter is also a function of duty cycle and input voltage only. However, (2.101) clearly states that the output voltage V_o of non-ideal DC-DC Cuk converter is dependent not only on duty cycle D and input voltage V_g but also depends on load resistance R and other non-ideal elements. The output voltage V_o as a function of duty cycle D is shown in Fig. 2.16 for ideal and non-ideal cases at different load resistances. The input voltage is kept constant 20 V and the load resistance is varied over three different values 2 Ω, 10 Ω and 20 Ω. The values of parasitic resistances and diode forward voltage drop are assumed constant and these values are given in Table 2.2. It is observed from Fig. 2.16 that in the ideal case, the converter output voltage increases with duty cycle. On the other hand, for the non-ideal case, the output voltage first increases with duty cycle, reaches its maximum value, and then decreases to zero at duty cycle close to unity. The output voltage is dependent on load

resistance. At a particular value of duty cycle, as the load resistance decreases the output voltage also drops significantly. For any fixed duty cycle, the difference between ideal DC output voltage and non-ideal DC output voltage increases with decrease in load resistance. This is because of the increased power losses in non-ideal Cuk converter at lower load resistance (or higher load current).

Table 2.2. Non-ideal DC-DC Cuk converter specifications

Parameters	**Value**
Input voltage, V_g	20 V
Output voltage, V_o	12 V
Load resistance, R	10 Ω
Inductance, L_1/r_{L1}	3 mH/0.5 Ω
Inductance, L_2/r_{L2}	1.9 mH/0.3 Ω
Capacitance, C_1/r_{c1}	50 μF/0.3 Ω
Capacitance, C_2/r_{c2}	85 μF/0.2 Ω
Diode forward voltage, V_F	0.7 V
Resistance switch/diode (r_{sw}/r_d),	0.044 Ω/0.024 Ω
Switching frequency, f	10 kHz
Desired inductor current ripple, $\Delta i_{L1}/I_{L1}$	0.32
Desired inductor current ripple, $\Delta i_{L2}/I_{L2}$	0.34
Desired voltage ripple, $\Delta v_1/V_o$	0.05
Desired output voltage ripple, $\Delta v_{om}/V_o$	0.01

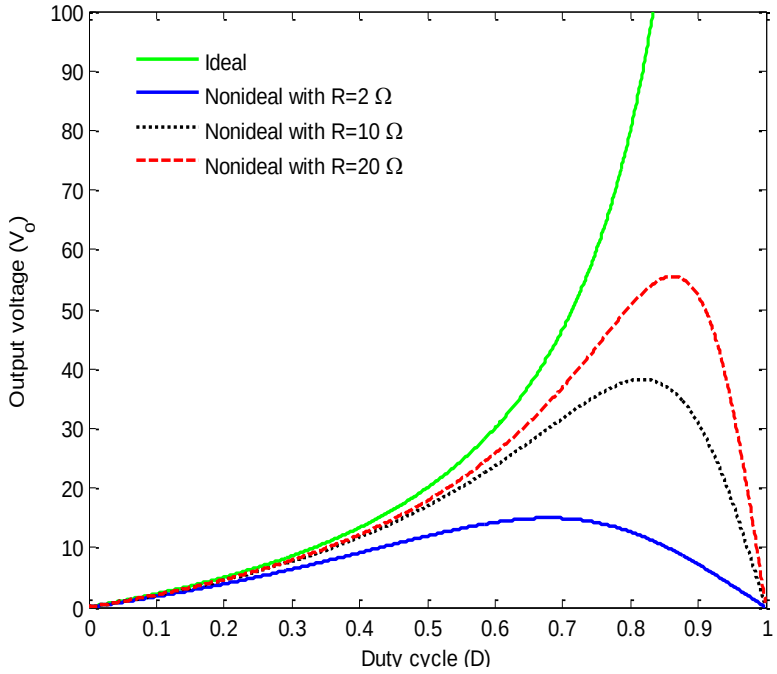


Fig. 2.16. Output voltage of DC-DC Cuk converter as a function of duty cycle

Therefore, it is clear that the output voltage of a practical Cuk converter is always less than the ideal Cuk converter, if the MOSFET switch of the practical Cuk converter is operated at a duty cycle which satisfies the relation in (2.101). The reason is that this relation is derived for the ideal Cuk converter. Therefore, to achieve the desired output voltage for practical Cuk converter, the duty cycle should be obtained by satisfying the input-output voltage relationship in (2.100). In the following section, this improved expression of duty cycle is derived.

2.3.3.2 Improved expression of duty cycle

As discussed in the previous section, the output voltage of a practical Cuk converter depends on load resistance and other parameters of a non-ideal converter. Therefore, to maintain the output voltage to the desired value despite of the voltage drops across the non-idealities, the actual duty cycle must be increased. The improved relationship for this duty cycle is developed in this section as follows:

Rewriting (2.100) in following form

$$V_o + V_F + \frac{V_o}{R}\left(\left(\frac{D}{D'}\right)^2 r_{L1} + r_{L2} + \frac{Dr_{c1}}{D'} + \frac{Dr_{sw} + D'r_d}{D'^2}\right) = \frac{D}{D'}V_g$$

$$\Rightarrow \frac{V_o}{R}D^2 r_{L1} + D'^2\left(V_o + \frac{V_o}{R}r_{L2} + V_F\right) + DD'\left(\frac{V_o}{R}r_{c1} - V_g\right) + Dr_{sw}\frac{V_o}{R} + D'r_d\frac{V_o}{R} = 0 \qquad (2.102)$$

Substituting $D' = 1 - D$ in the above equation and on simplifying, a quadratic equation in D is obtained as given below:

$$aD^2 + bD + c = 0 \qquad (2.103)$$

Where,

$$a = \left(1 + \frac{r_{L1} + r_{L2} - r_{c1}}{R} + \frac{V_g + V_F}{V_o}\right), b = -\left(2 + \frac{2r_{L2} - r_{c1} - r_{sw} + r_d}{R} + \frac{V_g + 2V_F}{V_o}\right), c = \left(1 + \frac{r_{L2} + r_d}{R} + \frac{V_F}{V_o}\right) \qquad (2.104)$$

The solution of quadratic equation in (2.103) is

$$D = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \qquad (2.105)$$

The feasible solution occurs with minus sign. Therefore, the actual duty cycle formula for non-ideal Cuk converter is:

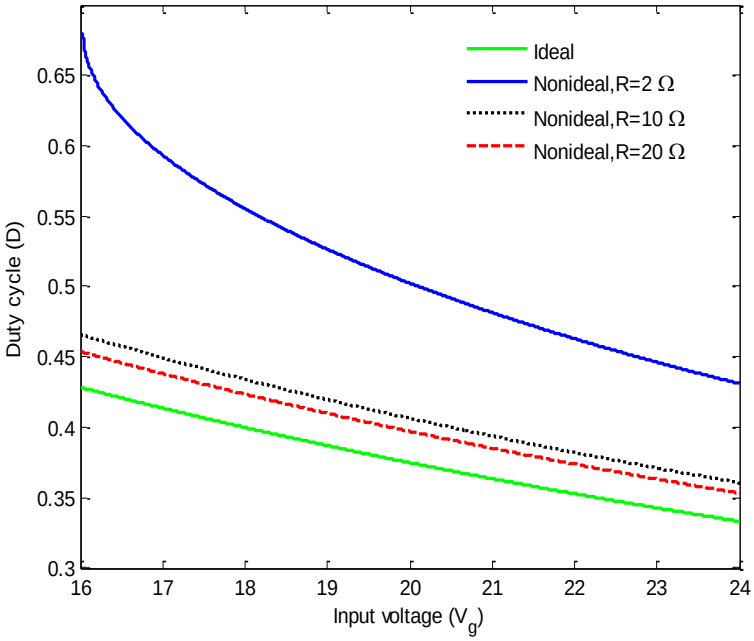
$$D = \frac{-b - \sqrt{b^2 - 4ac}}{2a} \qquad (2.106)$$

By substituting the values of the coefficients a, b and c, we get

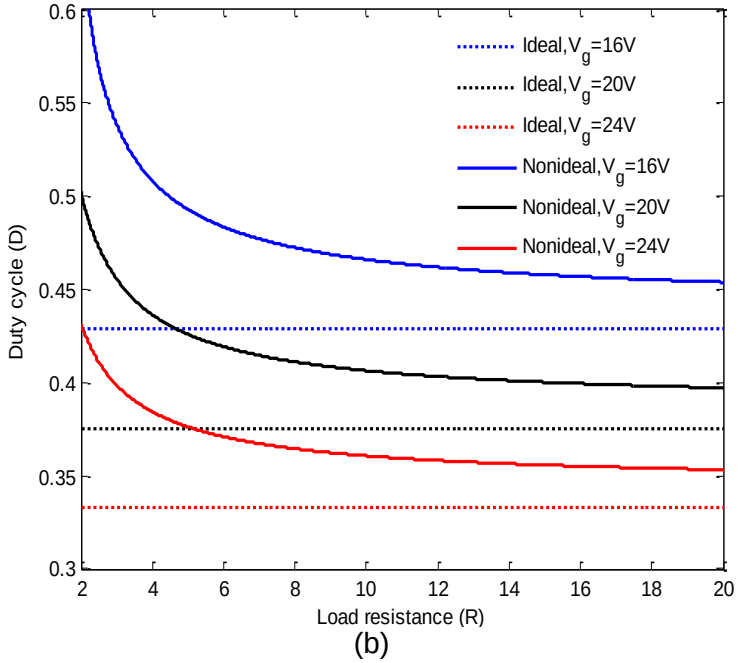
$$D = \frac{\left(2 + \frac{2r_{L2} - r_{c1} - r_{sw} + r_d}{R} + \frac{V_g + 2V_F}{V_o}\right) - \sqrt{\left(2 + \frac{2r_{L2} - r_{C1} - r_{sw} + r_d}{R} + \frac{V_g + 2V_F}{V_o}\right)^2 - 4\left(1 + \frac{r_{L1} + r_{L2} - r_{c1}}{R} + \frac{V_g + V_F}{V_o}\right)\left(1 + \frac{r_{L2} + r_d}{R} + \frac{V_F}{V_o}\right)}}{2\left(1 + \frac{r_{L1} + r_{L2} - r_{c1}}{R} + \frac{V_g + V_F}{V_o}\right)} \qquad (2.107)$$

Whereas, from (2.101), the duty cycle for ideal DC-DC Cuk converter is

$$D_{ideal} = \frac{V_o}{V_o + V_g} \tag{2.108}$$



(a)



(b)

Fig. 2.17. Duty cycle variation as a function of (a) input voltage (b) load resistance

This expression in (2.107) confirms that the actual duty cycle is not only dependent on output voltage and input voltage as in the ideal case, but also depends on load resistance and other non-ideal elements of the Cuk converter. The duty cycle calculated using this relation results in the desired value of the output voltage V_o. The variation in duty cycle D to obtain a particular output voltage is plotted as a function of input voltage and load resistance

in Fig. 2.17. The values of parasitic resistances and diode forward voltage drop are assumed constant as given in Table 2.2 and the desired DC output voltage is 12 V. In Fig. 2.17(a), the duty cycle variation is shown as a function of input voltage V_g at three different values of load resistance 2 Ω, 10 Ω and 20 Ω. It shows that the actual duty cycle is dependent on load resistance and at a particular value of input voltage, as the load resistance decreases, the required duty cycle increases. Similarly, at a particular value of load resistance, the difference between ideal and non-ideal duty cycle becomes narrower as the input voltage increases. Fig. 2.17(b) shows the duty cycle D plotted as a function of load resistance R at different values of input voltage (16 V, 20 V and 24 V). The difference between the duty cycle in ideal and non-ideal case is noticeable for a particular value of input voltage. Further, at the low value of load resistances, this difference is more. The reason for this is that at low load resistance, the power losses would be high. Therefore, to accommodate these power losses the duty cycle should be increased substantially.

2.3.4 Inductor current ripple and inductor design

In this section, the improved relationship for inductor current ripple and inductor design is developed for DC-DC Cuk converter currents including the effect of non-idealities. Let x_{L1} and x_{L2} be inductor current ripple factor (ICRF) for inductors L_1 and L_2 respectively, such that

$$x_{L1} = \frac{\Delta i_{L1}}{I_{L1}} \text{ and } x_{L2} = \frac{\Delta i_{L2}}{I_{L2}} \tag{2.109}$$

Here, I_{L1} and I_{L2} are the average currents through inductors L_1 and L_2, respectively.

2.3.4.1 Inductor L_1

From (2.77), in steady-state, the rate of change of inductor current i_{L1} can be assumed constant for one switching cycle *i.e.,*

$$\frac{\Delta i_{L1}}{\Delta t} = \frac{-\left(r_{L1} + r_{sw}\right) I_{L1} - r_{sw} I_{L2} + V_g}{L_1} \tag{2.110}$$

For on period $\Delta t = DT$, therefore, the magnitude of ripple current Δi_{L1} can be written as

$$\Delta i_{L1} = \frac{V_g - \left(r_{L1} + r_{sw}\right) I_{L1} - r_{sw} I_{L2}}{L_1} DT \tag{2.111}$$

Substituting values of I_{L1} and I_{L2} from (2.93) and (2.95),

$$\Delta i_{L1} = \frac{1}{L_1}\left(V_g - \left(r_{L1} + r_{sw}\right)\frac{DV_o}{D'R} - r_{sw}\frac{V_o}{R}\right)DT \tag{2.112}$$

Simplifying the above equation, we get

$$\Delta i_{L1} = \frac{DV_o}{L_1 f}\left(\frac{V_g}{V_o} - \frac{1}{RD'}\left(Dr_{L1} + r_{sw}\right)\right) \tag{2.113}$$

Here $f = 1/T$ is the switching frequency of Cuk converter.

Equation (2.100) can be written as

$$\frac{V_g}{V_o}=\frac{D'}{D}\left[1+\frac{V_F}{V_o}+\frac{1}{R}\left(\left(\frac{D}{D'}\right)^2 r_{L1}+r_{L2}+\frac{Dr_{c1}}{D'}+\frac{Dr_{sw}+D'r_d}{D'^2}\right)\right] \tag{2.114}$$

Substituting this expression in (2.113), we get

$$\Delta i_{L1}=\frac{DV_o}{L_1 f}\cdot\frac{D'}{D}\left[1+\frac{V_F}{V_o}+\frac{1}{R}\left(\left(\frac{D}{D'}\right)^2 r_{L1}+r_{L2}+\frac{Dr_{c1}}{D'}+\frac{Dr_{sw}+D'r_d}{D'^2}\right)-\frac{D}{RD'^2}\left(r_{sw}+Dr_{L1}\right)\right]$$

$$\Rightarrow \Delta i_{L1}=\frac{D'V_o}{L_1 f}\left[1+\frac{V_F}{V_o}+\frac{1}{R}\left(r_{L2}+\frac{Dr_{c1}}{D'}+\frac{r_d}{D'}\right)\right] \tag{2.115}$$

This is the expression for inductor current ripple Δi_{L1} for non-ideal Cuk converter.

Substituting $\Delta i_{L1}=x_{L1}I_{L1}=x_{L1}\frac{DV_o}{D'R}$ into (2.115), we get

$$x_{L1}\frac{DV_o}{D'R}=\frac{D'V_o}{L_1 f}\left[1+\frac{V_F}{V_o}+\frac{1}{R}\left(r_{L2}+\frac{Dr_{c1}}{D'}+\frac{r_d}{D'}\right)\right]\Rightarrow L_1=\frac{D'^2R}{x_{L1}fD}\left[1+\frac{V_F}{V_o}+\frac{1}{R}\left(r_{L2}+\frac{Dr_{c1}}{D'}+\frac{r_d}{D'}\right)\right] \tag{2.116}$$

This is the relationship to design inductance L_1 for non-ideal DC-DC Cuk converter.

2.3.4.2 Inductor L_2

From (2.83), in steady-state, the rate of change of inductor current i_{L2} can written as

$$\frac{\Delta i_{L2}}{\Delta t}=\frac{-r_d I_{L1}-\left(r_{L2}+r_d\right)I_{L2}-V_o-V_F}{L_2} \tag{2.117}$$

For off period $\Delta t=D'T$, the magnitude of ripple current Δi_{L2} can be written as

$$\Delta i_{L2}=\frac{V_o+V_F+r_d I_{L1}+\left(r_{L2}+r_d\right)I_{L2}}{L_2}D'T \tag{2.118}$$

Substituting values of I_{L1} and I_{L2} from (2.93),(2.95), we get

$$\Delta i_{L2}=\frac{1}{L_2}\cdot\left[V_o+V_F+r_d\frac{DV_o}{D'R}+\left(r_{L2}+r_d\right)I_{L2}\right]D'T \tag{2.119}$$

Simplifying the above equation,

$$\Delta i_{L2}=\frac{D'V_o}{fL_2}\left[1+\frac{V_F}{V_o}+\frac{1}{R}\left(r_{L2}+\frac{r_d}{D'}\right)\right] \tag{2.120}$$

This expression gives the inductor current ripple Δi_{L2} for non-ideal DC-DC Cuk converter.

Substituting $\Delta i_{L2}=x_{L2}I_{L2}=x_{L2}\frac{V_o}{R}$ in (2.120), the expression for inductor L_2 is obtained as

$$L_2=\frac{D'R}{x_{L2}f}\left[1+\frac{V_F}{V_o}+\frac{1}{R}\left(r_{L2}+\frac{r_d}{D'}\right)\right] \tag{2.121}$$

Putting the values of all non-ideal elements to zero in (2.115), (2.116), (2.120) and (2.121), these expressions become,

$$\Delta i_{L1}=\frac{D'V_o}{L_1 f} \tag{2.122}$$

$$L_1=\frac{D'^2R}{x_{L1}fD} \tag{2.123}$$

$$\Delta i_{L2} = \frac{D'V_o}{L_2 f} \tag{2.124}$$

$$L_2 = \frac{D'R}{x_{L2} f} \tag{2.125}$$

Equations (2.122)-(2.125) are same as given in the various textbooks to calculate the inductor current ripple and inductance value for an ideal Cuk converter [123], [125]. However, (2.116) and (2.121) provide the improved value of inductance L_1 and L_2 to limit the current ripple within a specified range for practical DC-DC Cuk converter.

2.3.5 Capacitor design

The equivalent series resistance (ESR) of a capacitor plays an important role in the design. A capacitor is modeled by its capacitance value and ESR value. The total voltage ripple of a capacitor is sum of the voltage ripple due to its own capacitance and the voltage ripple due to its ESR. Therefore, for proper capacitor design, it becomes necessary to consider the effect of ESR. The Cuk converter circuit has two capacitors C_1 and C_2. Capacitor C_1 is used to transfer the energy from input supply to the load. Capacitor C_2 is used at the output stage across the load resistance to minimize the output voltage ripple. In this section, the voltage ripple analysis and capacitor design is carried out for both capacitors C_1 and C_2.

2.3.5.1 Capacitor C_1

For capacitor C_1, the capacitor current $i_{c1}(t)$ and associated voltage ripple waveforms are shown in Fig. 2.18. Let the maximum allowable voltage ripple across capacitor C_1 be Δv_1. It is sum of the ripple voltage due to capacitor itself (Δv_{c1}) and the ripple voltage due to capacitor ESR (Δv_{rc1}) *i.e.,*

$$\Delta v_1 \simeq \Delta v_{c1} + \Delta v_{rc1} \tag{2.126}$$

Let r_{c1} be ESR of capacitor C_1. Therefore, the ripple voltage due to the ESR (r_{c1}) is

$$\Delta v_{rc1} = r_{c1} \Delta i_{c1} \tag{2.127}$$

As shown in Fig. 2.18, the ripple current Δi_{c1} at which maximum voltage drop across ESR (r_{c1}) occurs, is given by

$$\Delta i_{c1} = \left(I_{L2} + \frac{\Delta i_{L2}}{2} \right) + \left(I_{L1} - \frac{\Delta i_{L1}}{2} \right) = I_{L1} + I_{L2} + \frac{1}{2}\left(\Delta i_{L2} - \Delta i_{L1} \right) \tag{2.128}$$

Substituting values from (2.93), (2.95), (2.115) and (2.120) into above equation,

$$\Delta i_{c1} = \frac{V_o}{RD'} + \frac{D'V_o}{2f}\left(1 + \frac{V_F}{V_o} + \frac{1}{R}\left(r_{L2} + \frac{r_d}{D'} \right) \right)\left(\frac{1}{L_2} - \frac{1}{L_1} \right) - \frac{r_{c1} D V_o}{2 f L_1} \tag{2.129}$$

On substitution of (2.129) into (2.127) , we get

$$\Delta v_{rc1} = r_{c1}\left[\frac{V_o}{RD'} + \frac{D'V_o}{2f}\left(1 + \frac{V_F}{V_o} + \frac{1}{R}\left(r_{L2} + \frac{r_d}{D'}\right)\right)\left(\frac{1}{L_2} - \frac{1}{L_1}\right) - \frac{r_{c1}DV_o}{2fL_1}\right] \tag{2.130}$$

From (2.126),

$$\Delta v_{c1} \simeq \Delta v_1 - \Delta v_{rc1} \tag{2.131}$$

The capacitor voltage ripple (Δv_{c1}) is defined as

$$\Delta v_{c1} = \frac{1}{C_1}\int_0^{DT} i_{c1}dt \tag{2.132}$$

This integration of i_{c1} is equal to the area enclosed by capacitor current waveform in duration DT. Therefore, from Fig. 2.18, we can write

$$\int_0^{DT} i_{c1}dt = \frac{1}{2}\cdot\left(\left(I_{L2} - \frac{\Delta i_{L2}}{2}\right) + \left(I_{L2} + \frac{\Delta i_{L2}}{2}\right)\right)\cdot DT \Rightarrow \int_0^{DT} i_{c1}dt = I_{L2}\cdot DT \tag{2.133}$$

Substituting this value in (2.132) gives,

$$\Delta v_{c1} = \frac{1}{C_1}\left(I_{L2}\cdot DT\right) = \frac{DI_{L2}}{C_1 f} \tag{2.134}$$

Substituting value of $I_{L2} = \frac{V_o}{R}$ into the above equation, we get

$$\frac{\Delta v_{c1}}{V_o} = \frac{D}{RC_1 f} \tag{2.135}$$

Rearranging the above equation,

$$C_1 = \frac{D}{Rf\frac{\Delta v_{c1}}{V_o}} = \frac{D}{Rf\left(\frac{\Delta v_1 - \Delta v_{rc1}}{V_o}\right)} \tag{2.136}$$

This is the minimum required value of capacitor C_1 to limit the voltage ripple across it within desired range.

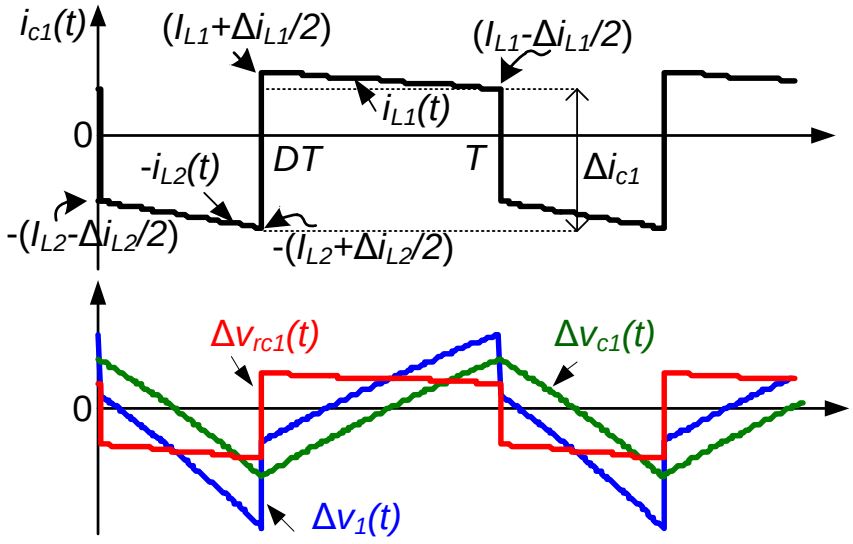


Fig. 2.18. Current and ripple voltage waveforms associated with capacitor C_1

2.3.5.2 Capacitor C_2

The capacitor C_2 is used as a filter capacitor at the output stage. The voltage ripple across this capacitor directly affects the quality of output voltage. Therefore, its design is carried out more carefully to limit the output voltage ripple within permissible range.

The capacitor current and different components of voltage ripple in steady-state are shown in Fig. 2.19. The output voltage ripple $\Delta v_o(t)$ is made up of two components:

a) Voltage ripple due to ESR, Δv_{rc2}

b) Voltage ripple due to capacitor itself, Δv_{c2}

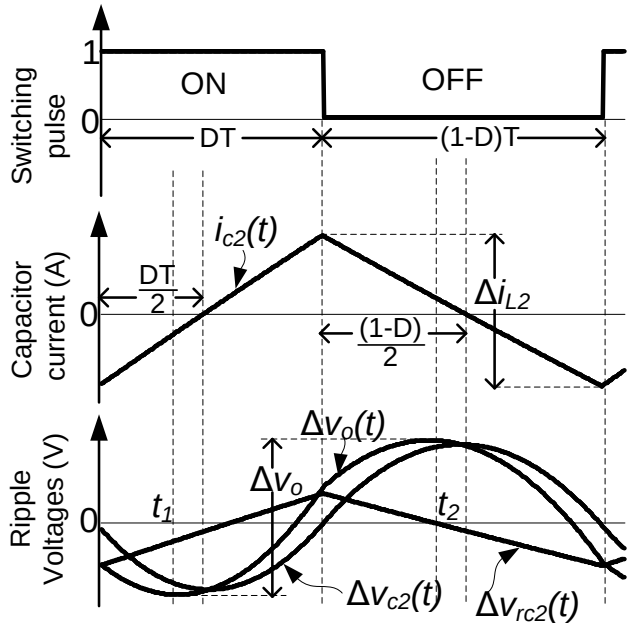


Fig. 2.19. Current and ripple voltage waveforms associated with capacitor C_2

The detailed analysis is carried out as follows:

Analysis when switch is on (0 < t ≤ DT): In this duration, the current through capacitor C_2 is given as:

$$i_{c2}(t) = \frac{\Delta i_{L2} t}{DT} - \frac{\Delta i_{L2}}{2} \tag{2.137}$$

Therefore, the voltage ripple contribution due to capacitor ESR is

$$\Delta v_{rc2}(t) = r_{c2} i_{c2}(t) = r_{c2} \Delta i_{L2} \left(\frac{t}{DT} - \frac{1}{2} \right) \tag{2.138}$$

The voltage ripple contribution due to capacitor itself is

$$\Delta v_{c2}(t) = \frac{1}{C_2} \int_0^t i_{c2}(t) dt + \Delta v_{c2}(0) = \frac{\Delta i_{L2}}{2C_2} \left(\frac{t^2}{DT} - t \right) + \Delta v_{c2}(0) \tag{2.139}$$

$\Delta v_{c2}(0)$ is the initial voltage across capacitor at t=0.

Therefore, the total output voltage ripple during switch-on is

$$\Delta v_o(t) = \Delta v_{c2}(t) + \Delta v_{rc2}(t) = \Delta i_{L2} \left[\frac{t^2}{2C_2 DT} + \left(\frac{r_{c2}}{DT} - \frac{1}{2C_2} \right) t - \frac{r_{c2}}{2} \right] + \Delta v_{c2}(0) \tag{2.140}$$

To find out the time t_1 at which $\Delta v_o(t)$ is minimum during switch-on, the above equation is differentiated with respect to time 't' and equate to zero. The expression for time t_1 is obtained as:

$$t_1 = \frac{DT}{2} - r_{c2}C_2 \tag{2.141}$$

Substituting this value of t_1 into (2.138)-(2.140), the different ripple voltages are

$$\Delta v_{rc2}(t_1) = -\Delta i_{L2}\frac{r_{c2}^2 C_2}{DT} \tag{2.142}$$

$$\Delta v_{c2}(t_1) = \Delta i_{L2}\left(-\frac{DT}{8C_2} + \frac{r_{c2}^2 C_2}{2DT}\right) + \Delta v_{c2}(0) \tag{2.143}$$

$$\Delta v_{o,\min} = \Delta v_o(t_1) = -\Delta i_{L2}\left(\frac{DT}{8C_2} + \frac{r_{c2}^2 C_2}{2DT}\right) + \Delta v_{c2}(0) \tag{2.144}$$

Analysis when switch is off (DT < t ≤ T): In this duration, the current through capacitor C_2 is:

$$i_{c2}(t) = \frac{-\Delta i_{L2}(t - DT)}{D'T} + \frac{\Delta i_{L2}}{2} \tag{2.145}$$

Therefore, the voltage ripple contribution due to capacitor ESR is

$$\Delta v_{rc2}(t) = r_{c2} i_{c2}(t) = r_{c2}\Delta i_{L2}\left(\frac{-(t - DT)}{D'T} + \frac{1}{2}\right) \tag{2.146}$$

The voltage ripple contribution due to capacitor itself is

$$\Delta v_{c2}(t) = \frac{1}{C_2}\int_{DT}^{t} i_{c2}(t)dt + \Delta v_{c2}(DT) = \frac{\Delta i_{L2}}{2C_2}\left(\frac{-(t - DT)^2}{D'T} + (t - DT)\right) + \Delta v_{c2}(DT) \tag{2.147}$$

$\Delta v_{c2}(DT)$ is the initial voltage across capacitor at $t=DT$.

Therefore, total output voltage ripple during the switch-off period is

$$\begin{aligned}\Delta v_o(t) &= \Delta v_{c2}(t) + \Delta v_{rc2}(t) \\ &= \Delta i_{L2}\left[\frac{-(t - DT)^2}{2C_2 D'T} + \left(\frac{-r_{c2}}{D'T} + \frac{1}{2C_2}\right)(t - DT) + \frac{r_{c2}}{2}\right] + \Delta v_{c2}(DT)\end{aligned} \tag{2.148}$$

The time 't_2' at which value of $\Delta v_o(t)$ occurs maximum during switch-off is obtained by differentiating the above equation with respect to time 't' and equating to zero as

$$t_2 = \frac{(1+D)T}{2} - r_{c2}C_2 \tag{2.149}$$

Substituting this value of t_2 into (2.146)-(2.148), the three ripple voltages are

$$\Delta v_{rc2}(t_2) = \Delta i_{L2}\frac{r_{c2}^2 C_2}{(1-D)T}, \tag{2.150}$$

$$\Delta v_{c2}(t_2) = \Delta i_{L2}\left(\frac{D'T}{8C_2} - \frac{r_{c2}^2 C_2}{2D'T}\right) + \Delta v_{c2}(DT) \tag{2.151}$$

$$\Delta v_{o,\max} = \Delta v_o\left(t_2\right) = \Delta i_{L2}\left(\frac{D'T}{8C_2} + \frac{r_{c2}^2 C_2}{2D'T}\right) + \Delta v_{c2}\left(DT\right) \tag{2.152}$$

In the steady-state,

$$\Delta v_{c2}\left(DT\right) = \Delta v_{c2}\left(0\right) \tag{2.153}$$

Therefore, total peak-to-peak output voltage ripple will be

$$\Delta v_o = \Delta v_o\left(t_2\right) - \Delta v_o\left(t_1\right) = \Delta i_{L2}\left(\frac{1}{8C_2 f} + \frac{r_{c2}^2 C_2 f}{2DD'}\right) \tag{2.154}$$

The contribution of ESR voltage ripple and capacitor voltage ripple in peak-to-peak output voltage ripple can also be found as follows:

$$\Delta v_{rc2} = \Delta v_{rc2}\left(t_2\right) - \Delta v_{rc2}\left(t_1\right) = \Delta i_{L2}\frac{r_{c2}^2 C_2 f}{DD'} \tag{2.155}$$

$$\Delta v_{c2} = \Delta v_{c2}\left(t_2\right) - \Delta v_{c2}\left(t_1\right) = \Delta i_{L2}\left(\frac{1}{8fC_2} - \frac{r_{c2}^2 C_2 f}{2DD'}\right) \tag{2.156}$$

Equations (2.154)-(2.156) depicts that these three ripple voltages are functions of capacitor ESR. The ripple voltage variation with respect to ESR is plotted in Fig. 2.20. This figure shows that with an increase in ESR, Δv_{rc} increases, whereas Δv_c decreases such that there is a net increase in Δv_o. However, after a particular value of ESR, output voltage ripple becomes greater than the specified limit. This value of ESR $r_{c2,max}$, is termed as critical value or maximum permissible value of ESR. As shown in figure, for the Cuk converter under consideration, the output voltage ripple is less than 0.12 V as desired (within 1% of output voltage) for $r_{c2}<r_{c2,max}$. The derivation of this $r_{c2,max}$ is carried out later.

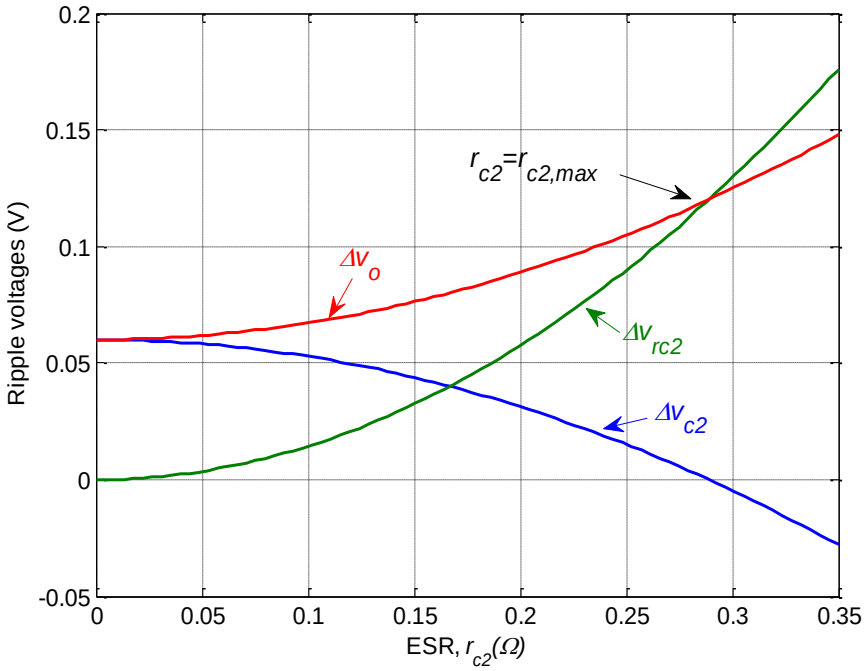


Fig. 2.20. Ripple voltage variations with ESR for DC-DC Cuk converter

Output capacitor design:

Let the maximum specified output voltage ripple be Δv_{om}. Therefore, the value of capacitor C_2 should be chosen such that

$$\Delta v_o \le \Delta v_{om} \tag{2.157}$$

Substituting the values from (2.154) into above equation,

$$\Delta i_{L2}\left(\frac{1}{8C_2 f}+\frac{r_{c2}^2 C_2 f}{2DD'}\right)\le \Delta v_{om} \tag{2.158}$$

Above inequality can be simplified as

$$r_{c2}^2 C_2^2-\frac{2DD'}{f}\left(\frac{\Delta v_{om}}{\Delta i_{L2}}\right)C_2+\frac{DD'}{4f^2}\le 0 \tag{2.159}$$

This is a quadratic inequality in C_2, which is solved to find the minimum value of output capacitor C_2 as

$$C_2=\frac{\frac{2DD'}{f}\left(\frac{\Delta v_{om}}{\Delta i_{L2}}\right)-\sqrt{\left(\frac{2DD'}{f}\left(\frac{\Delta v_{om}}{\Delta i_{L2}}\right)\right)^2-4r_{c2}^2\frac{DD'}{4f^2}}}{2r_{c2}^2} \tag{2.160}$$

This expression gives the minimum value of filter capacitor C_2 (with $r_{c2}\le r_{c2,max}$) for desired output voltage ripple and inductor current ripple at given switching frequency.

Maximum Permissible ESR for Output Capacitor:

As discussed in the previous section, the ESR of output capacitor C_2 plays an important role in the output voltage ripple of Cuk converter. As the value of ESR increases, the more ripple appears in output voltage, degrading the output voltage quality. Therefore, it is essential to derive an analytical relation for the maximum permissible value of ESR ($r_{c2,max}$) for specified output voltage ripple and switching frequency.

In (2.160), Capacitor C_2 will have a real value (practically feasible) only if the terms inside the root is greater than or equal to zero, *i.e.,*

$$\left(\frac{2DD'}{f}\left(\frac{\Delta v_{om}}{\Delta i_{L2}}\right)\right)^2-4r_{c2}^2\frac{DD'}{4f^2}\ge 0 \tag{2.161}$$

On simplification,

$$r_{c2}\le 2\sqrt{DD'}\,\frac{\Delta v_{om}}{\Delta i_{L2}} \tag{2.162}$$

Therefore, the maximum permissible value of ESR ($r_{c2,max}$) for the specified output voltage ripple (Δv_{om}) and inductor current ripple (Δi_{L2}) can be defined as

$$r_{c2,\max}=2\sqrt{DD'}\,\frac{\Delta v_{om}}{\Delta i_{L2}} \tag{2.163}$$

This is the expression for the critical value or the maximum permissible value of ESR for Cuk converter. If the ESR value of the output capacitor is greater than the $r_{c2,max}$, then the

output voltage ripple will exceed the maximum defined limit. It is proved later by simulation and experimental results.

Substituting value of $r_{c2,max}$ into (2.160), the minimum value of the output capacitor in the worst case is

$$C_{2,\min} = \frac{\Delta i_{L2}}{4f\Delta v_{om}} \tag{2.164}$$

Replacing value of Δi_{L2} from (2.120), we get

$$C_{2,\min} = \frac{D'V_o}{4L_2f^2\Delta v_{om}}\left[1+\frac{V_F}{V_o}+\frac{1}{R}\left(r_{L2}+\frac{r_d}{D'}\right)\right] \tag{2.165}$$

Replacing r_{c2}=0 (for ideal case) in (2.154), the minimum value of capacitance is

$$C_{2,\min,ideal} = \frac{\Delta i_{L2}}{8f\Delta v_{om}} = \frac{D'V_o}{8L_2f^2\Delta v_{om}} \tag{2.166}$$

Equations (2.164) and (2.166) provides the minimum value of output capacitance in non-ideal and ideal case, respectively. The minimum value of capacitor in ideal case is half of non- ideal case. To observe the variation in minimum value of capacitor C_2 as a function of ESR, the equation (2.160) is plotted in Fig. 2.21. It can be seen that the required capacitor value increases with increase in ESR and at $r_{c2} = r_{c2,max}$, it becomes two times of capacitance value with r_{c2}=0. For $r_{c2} > r_{c2,max}$, capacitance value is a complex number, therefore, MATLAB plots only real part as shown in figure.

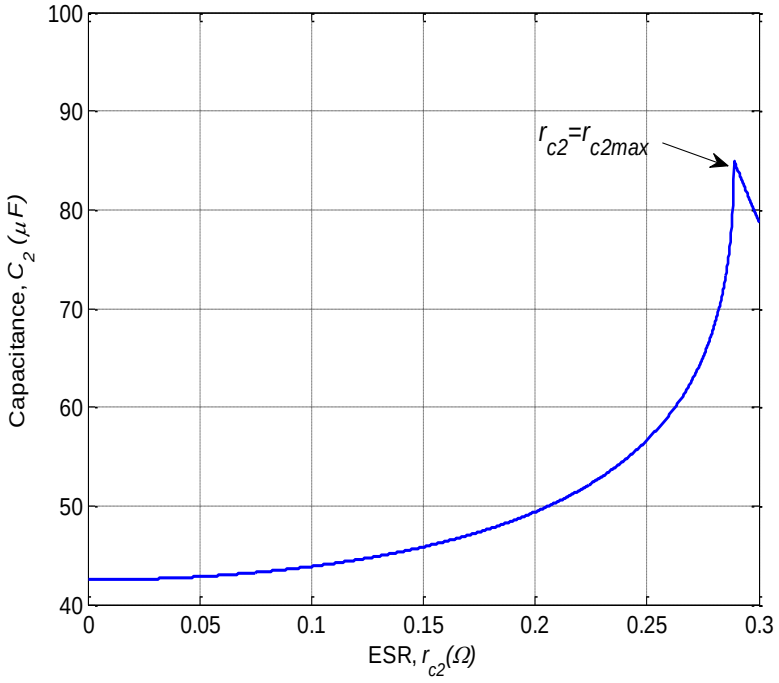


Fig. 2.21. Variations in minimum required value of capacitor C_2 with ESR

2.3.6 Results and discussion

The simulation and experimental results are obtained to verify the analytical studies. The simulations are carried out in MATLAB/Simulink software package, whereas for the

experimental results, a hardware prototype is developed. The detailed description of prototype development is described in Appendix *B*. The values of various parameters used for simulation and experiment are same as given in Table 2.2.

For these specifications, using (2.108), the ideal duty cycle is calculated 0.375, whereas the improved duty cycle in the presence of non-idealities is calculated as 0.406 using the proposed relationship in (2.107). This increased duty cycle is necessary to compensate the voltage drop occurring due to non-idealities. The value of inductor L_1 using ideal formula is 2.70 mH whereas it is 3 mH using the proposed formula in (2.116). Similarly, the value of inductor L_2 using ideal relationship is 1.74 mH whereas it is 1.91 mH using the proposed formula in (2.121). Therefore, the more inductance is required in the presence of non-idealities. The minimum value of capacitor C_1 is computed 50 µF using (2.136) to limit the total voltage ripple to 5%, while in ideal case it is 30 µF. The minimum value of capacitor C_2 is 42.5 µF in the ideal case, whereas 85 µF in non-ideal case as calculated by (2.165). The maximum permissible value of output capacitor ESR ($r_{c2,max}$) is calculated as 0.29 Ω using (2.163) to confine the output voltage ripple within 1% of output voltage.

The simulation and experimental inductor current and capacitor current waveforms of Cuk converter are shown in Fig. 2.22. The average inductor current values I_{L1} and I_{L2} are 0.82 A and 1.2 A, respectively, and the inductor current ripple Δi_{L1} and Δi_{L2} are 0.26 A and 0.41 A, respectively. The peak-to-peak capacitor currents are 2.1 A (for capacitor C_1) and 0.41 A (for capacitor C_2), respectively.

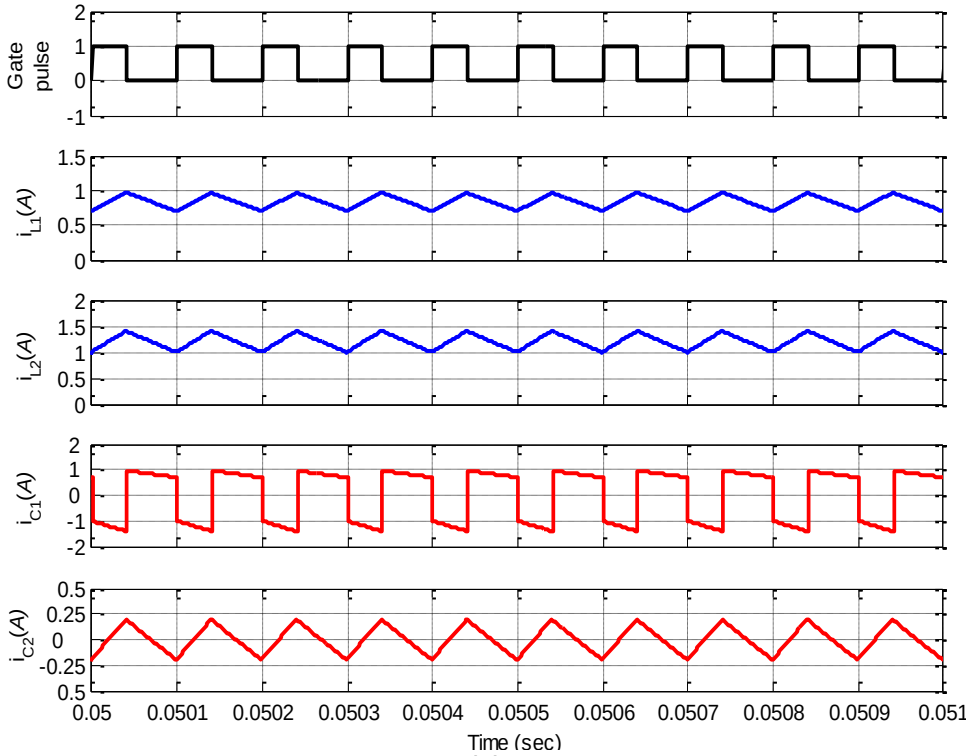
The simulated and experimental output voltage responses of the Cuk converter with ideal duty cycle D=0.375 are obtained as shown in Fig. 2.23. In steady-state, the output voltage magnitude reaches to 10.5 V (not 12 V as desired). On the other hand, it is observed that if the duty cycle is 0.406 as calculated by proposed relationship, the output voltage is 12 V in steady-state. The corresponding simulation and experimental results are shown in Fig. 2.24.

The effect of output capacitor ESR (r_{c2}) on the output voltage ripple of Cuk converter is also studied. By this study, the importance of determining the maximum permissible ESR ($r_{c2,max}$) is justified. For this purpose, two different cases ($r_{c2}<r_{c2,max}$ and $r_{c2}>r_{c2,max}$) are considered as discussed below-

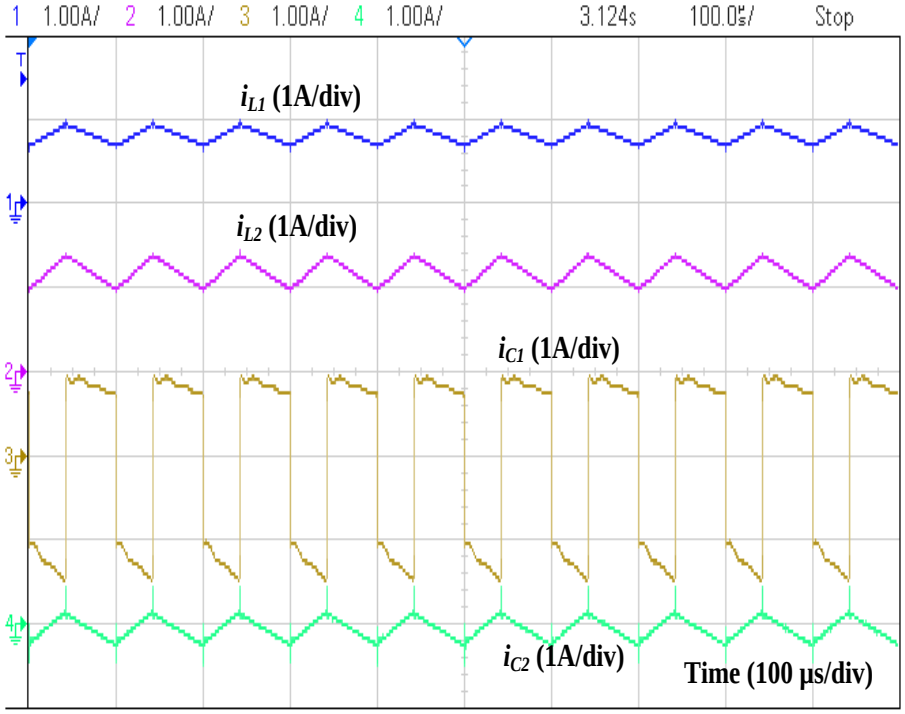
***Case 1 ($r_{c2} < r_{c2,max}$)*:** In this case, the ESR of the output capacitor (r_{c2}) is taken 0.2 Ω which is less than the value of maximum permissible ESR (0.29 Ω). The simulated and experimental waveforms of output voltage ripple are shown in Fig. 2.25. These results show that the magnitude of the output voltage ripple is nearly 100 mV, which is within specified limit (120 mv).

Case 2 ($r_{c2} > r_{c2,max}$): This case evaluates that what happens to output voltage ripple if capacitor ESR (r_{c2}) is greater than the maximum permissible ESR. Therefore, the value of r_{c2}

is kept 0.5 Ω in simulation as well as in experimental prototype. As shown in Fig. 2.26, the output voltage ripple is obtained nearly 200 mV, which is beyond the desired limit (120 mV). Therefore, this value of output capacitor ESR is not suitable to have output voltage ripple within 1% range as desired.

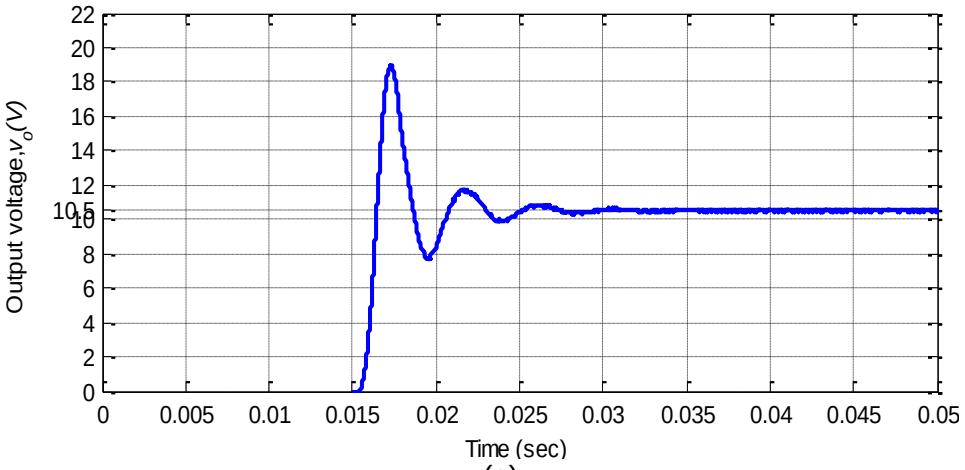


(a)

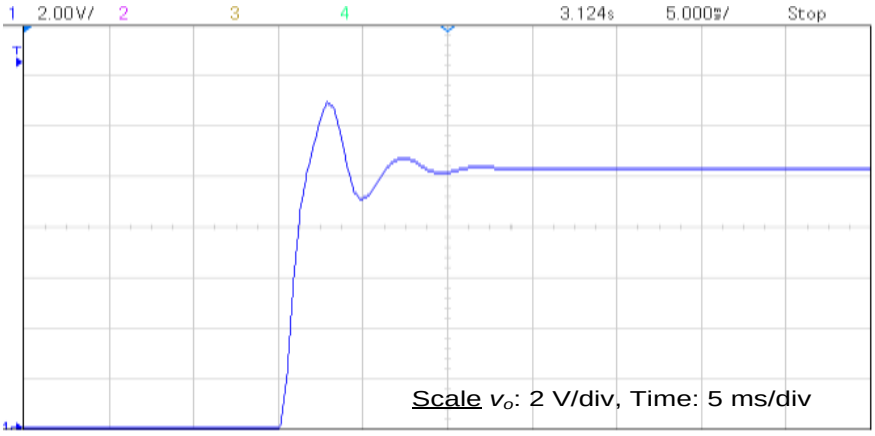


(b)

Fig. 2.22. Inductor current and capacitor current waveforms of Cuk converter (a) Simulation (b) Experimental

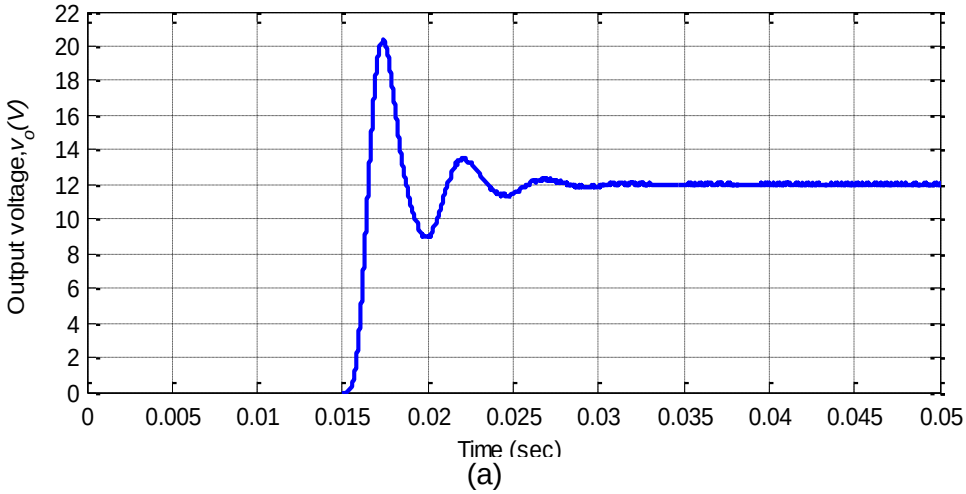


(a)

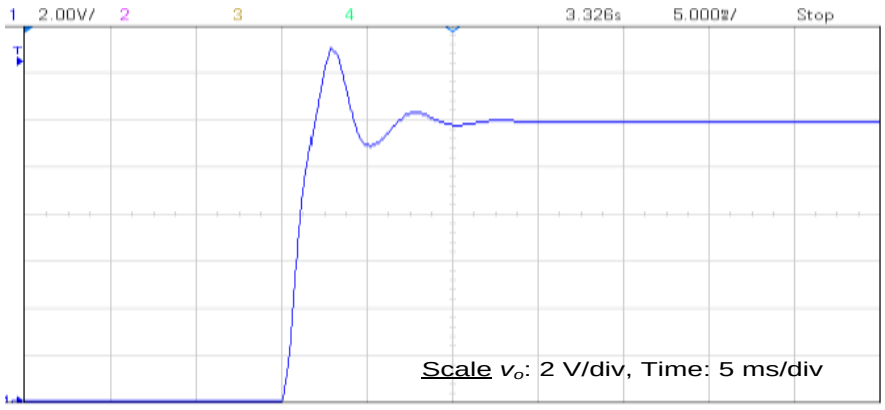


(b)

Fig. 2.23. Output voltage response of Cuk converter with ideal duty cycle D=0.375 (a) Simulation (b) Experimental

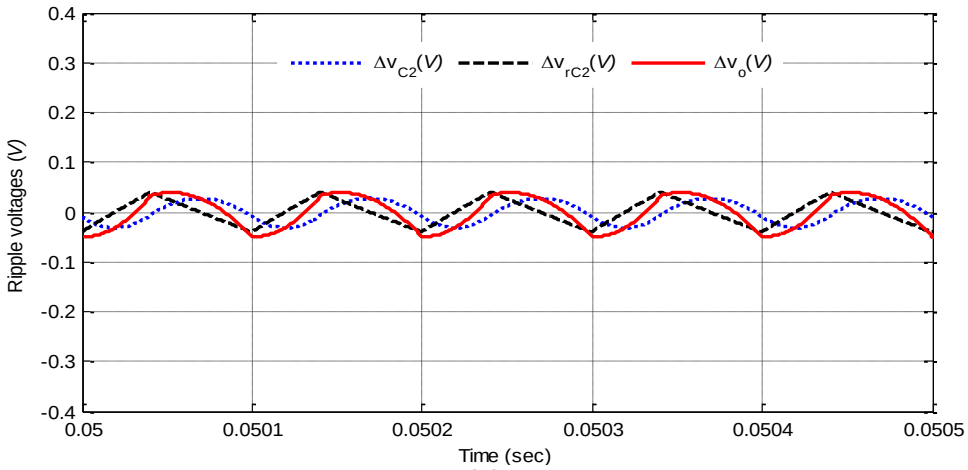


(a)

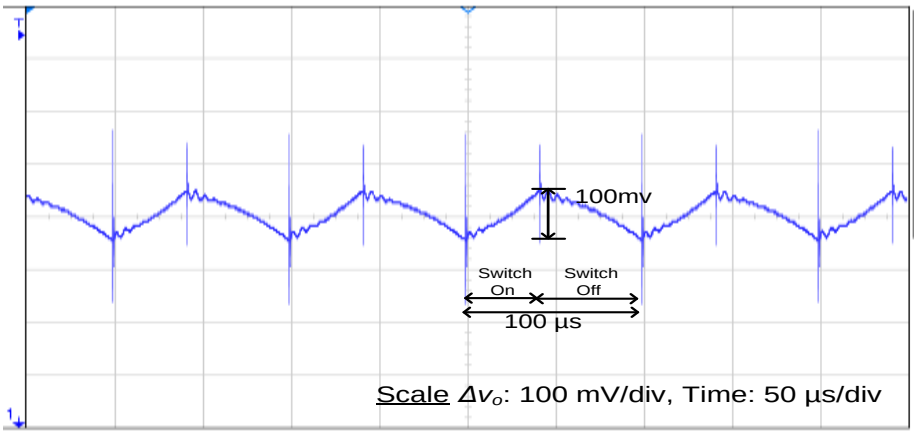


(b)

Fig. 2.24. Output voltage response of Cuk converter with improved duty cycle D=0.406 (a) Simulation (b) Experimental

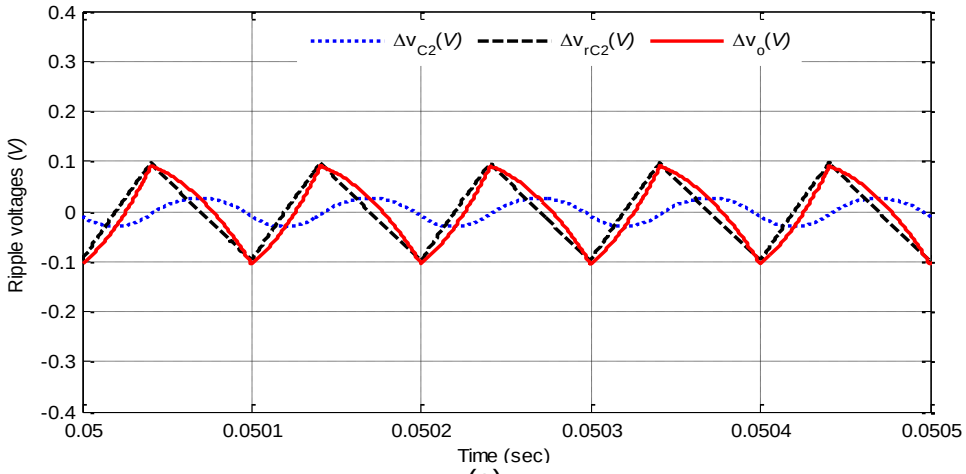


(a)

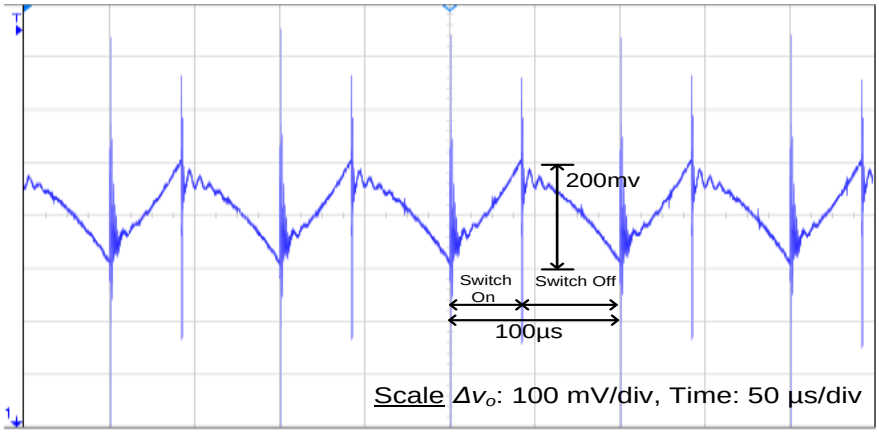


(b)

Fig. 2.25. Output voltage ripple with ESR 0.2 Ω ($r_{c2} < r_{c2,max}$) (a) Simulation (b) Experimental



(a)



(b)

Fig. 2.26. Output voltage ripple with ESR 0.5 Ω ($r_{c2} > r_{c2,max}$) (a) Simulation (b) Experimental

2.4 Conclusion

The performance of the DC-DC buck converter and Cuk converter has been analysed in the presence of the non-idealities. It has been proven by the experimental results that the ideal relationship for duty cycle produces the lesser output voltage than the desired output voltage. Therefore, by in-depth analysis, the improved expressions for duty cycle have been obtained, which results in the desired output voltage. Moreover, the modified equations for inductor and capacitor design have been obtained. Further, the effect of capacitor equivalent series resistance (ESR) on output voltage ripple (OVR) has been analysed in detail. With the help of simulation and experimental results, it was observed that for the ESR greater than a particular value ($r_{c,max}$), the output voltage ripple crosses the desired ripple limit. The expression for the maximum permissible value of ESR ($r_{c,max}$) was derived in terms of specified OVR.

[This chapter presents the different techniques used for mathematical modeling of non-ideal DC-DC buck and Cuk converter. The various transfer functions have been derived which includes the effect of non-ideal elements present in these converters.]

3.1 Introduction

The DC-DC switch mode converters are variable structure system and therefore, they are considered as non-linear time variant systems. The mathematical modeling of any DC-DC converter is essential in order to investigate the dynamic and steady-state behaviour. Mathematical modeling provides the information about how the variations in duty cycle, input voltage and load current affect the output voltage. Moreover, modeling also plays a key role in controller design of DC-DC converters to regulate the output voltage. For proper control design, it is mandatory to have an accurate and precise dynamic model of the converter. The significant work has been done for modeling of DC-DC converters. Several techniques are available in the literature for mathematical modeling of converters such as state-space averaging (SSA) method [25], [58], [63], averaged switch model technique [67], [127], transformer equivalent modeling method [3], current injected equivalent circuit (CIEC) approach [72], [73], switching flow graph (SFG) technique [74], [128], bond graph method [76], energy factor approach [69], [70], *etc*. These methods have its own advantages and limitations. They have certain ways to derive and express the mathematical model in specific form. However, it is observed in the literature that the mathematical models of the converters are obtained either by considering them ideal or considering only few non-ideal elements. In order to achieve the accurate model of DC-DC converter, the inclusion of all non-idealities is important. In this chapter, the various transfer functions are obtained for non-ideal DC-DC buck converter and Cuk converter including all non-ideal elements. As discussed earlier, though there are various methods available, but in this chapter, the mathematical models are derived using following approaches:

- State-space averaging (SSA) technique
- Averaged switch model technique
- Energy factor approach

3.2 State-space Averaging (SSA) Modeling Technique

The state-space averaging technique is described in this section. As discussed earlier, the DC-DC converters are variable structure time-varying system *i.e.,* they are switched between two or more time-invariant systems. In SSA technique, the state-space descriptions of these individual systems are first obtained. To obtain a unified state-space model, they are averaged and then linearized to get the small-signal model of the converter. This technique is

very popular and widely used for modeling the DC-DC converters. In this chapter, the SSA method will be discussed in a more generalized form. An additional constant vector has been added to include the effect of diode forward voltage drop. The SSA method can be used to obtain the small-signal model of DC-DC converters in both CCM and DCM mode. However, in this thesis, only CCM mode is discussed.

3.2.1 Generalized state-space averaging modeling technique

For CCM, DC-DC converters operate in two different circuit states in one switching period, (a) when switch is on for a time interval *dT* and (b) when switch is off for a time interval (*1-d)T*, where *d* is duty cycle and *T* is switching period. For each state, the equivalent circuit behaves like a linear circuit assuming that the circuit parameters *R*, *L* and *C* are linear [1], [3], [62]. The generalized state-space averaging modeling technique is presented in following steps:

Step 1: Obtaining the individual state equations model for each state of circuit operation

In any DC-DC converter, the inductor current and capacitor voltages are generally chosen as state variables. Therefore, the total numbers of state variables are equal to the total number of inductors and capacitors. In general, these state variables are represented by a state variable vector *x(t).* For CCM operation, the state equations model for the two circuit states are given by following equation:

(a) When the switch is on during time interval *dT*, the state equations model of converter is

$$\frac{dx(t)}{dt} = A_1 x(t) + B_1 u(t) + J_1 \tag{3.1}$$

$$y(t) = C_1 x(t) + E_1 u(t) + F_1 \tag{3.2}$$

(b) When the switch is off during time interval *(1-d)T*, state equations model of converter is

$$\frac{dx(t)}{dt} = A_2 x(t) + B_2 u(t) + J_2 \tag{3.3}$$

$$y(t) = C_2 x(t) + E_2 u(t) + F_2 \tag{3.4}$$

These individual state equations models are linear. Note that here *x(t)* is a state variable vector, *u(t)* is an input variable vector ,*y(t)* is an output variable vector. The different matrices associated with the state equations model in (3.1)-(3.4) are constant and are named as follows [77], [78] - A_i: system matrix, B_i: input coupling matrix, C_i: output coupling matrix, E_i: input-output coupling matrix, J_i and F_i: constant vectors, which are used here to involve the diode forward voltage drop in the modeling of DC-DC converter; Where *i=1,2.*

Step 2: Finding the averaged state-space model

To investigate the unified behaviour of the DC-DC converter, these two different state equations models are averaged over one switching period using corresponding conduction period as weights [1]. It yields,

$$\frac{d\bar{x}(t)}{dt} = A'(t)\bar{x}(t) + B'(t)\bar{u}(t) + J'(t) \tag{3.5}$$

$$\bar{y}(t) = C'(t)\bar{x}(t) + E'(t)\bar{u}(t) + F'(t) \tag{3.6}$$

Where,

$$\begin{aligned} &A'(t) = A_1 d(t) + A_2\left(1-d(t)\right), B'(t) = B_1 d(t) + B_2\left(1-d(t)\right), C'(t) = C_1 d(t) + C_2\left(1-d(t)\right) \\ &E'(t) = E_1 d(t) + E_2\left(1-d(t)\right), J'(t) = J_1 d(t) + J_2\left(1-d(t)\right), F'(t) = F_1 d(t) + F_2\left(1-d(t)\right) \end{aligned} \tag{3.7}$$

The bar (-) symbol represents the averaged value of a particular variable over one switching period. The averaged state-space model in (3.5)-(3.6) is non-linear because they have the multiplication of time-varying terms.

Step 3: Linearization by introducing small ac perturbation around a DC operating point

In order to obtain the small-signal model of DC-DC converter, the above non-linear averaged state-space model is linearized around a steady-state (DC) operating point. For this purpose, small ac perturbations are introduced around steady-state (DC) values of different variables as follows:

$$\begin{aligned} &\bar{x}(t) = X + \tilde{x}(t) \qquad ,\bar{y}(t) = Y + \tilde{y}(t), \bar{u}(t) = U + \tilde{u}(t) \\ &d(t) = D + \tilde{d}(t), d'(t) = 1 - d(t) = 1 - D - \tilde{d}(t) = D' - \tilde{d}(t) \end{aligned} \tag{3.8}$$

Here $X >> \tilde{x}(t), Y >> \tilde{y}(t), U >> \tilde{u}(t)$ and $D >> \tilde{d}(t)$.

The variables with '~' denotes the small ac perturbed signal, whereas variables in capital letter represent a steady-state (DC) value.

By substituting these values from (3.8) into non-linear averaged model in (3.5)-(3.6), we get

$$\begin{aligned} \dot{X} + \dot{\tilde{x}}(t) = &\left[A_1\left(D + \tilde{d}(t)\right) + A_2\left(1 - D - \tilde{d}(t)\right)\right]\left(X + \tilde{x}(t)\right) + \left[B_1\left(D + \tilde{d}(t)\right) + B_2\left(1 - D - \tilde{d}(t)\right)\right] \cdot \\ &\left(U + \tilde{u}(t)\right) + \left[J_1\left(D + \tilde{d}(t)\right) + J_2\left(1 - D - \tilde{d}(t)\right)\right] \\ \Rightarrow \dot{X} + \dot{\tilde{x}}(t) = &\left(A_1 D + A_2(1-D)\right)X + \left(A_1 D + A_2(1-D)\right)\tilde{x}(t) + \left(A_1 - A_2\right)X\tilde{d}(t) + \left(A_1 - A_2\right)\tilde{d}(t)\tilde{x}(t) + \\ &\left(B_1 D + B_2(1-D)\right)U + \left(B_1 D + B_2(1-D)\right)\tilde{u}(t) + \left(B_1 - B_2\right)U\tilde{d}(t) + \left(B_1 - B_2\right)\tilde{d}(t)\tilde{u}(t) + \\ &\left(J_1 D + J_2(1-D)\right) + \left(J_1 - J_2\right)\tilde{d}(t) \end{aligned} \tag{3.9}$$

Similarly,

$$\begin{aligned} Y + \tilde{y}(t) = &\left[C_1\left(D + \tilde{d}(t)\right) + C_2\left(1 - D - \tilde{d}(t)\right)\right]\left(X + \tilde{x}(t)\right) + \left[E_1\left(D + \tilde{d}(t)\right) + E_2\left(1 - D - \tilde{d}(t)\right)\right] \cdot \\ &\left(U + \tilde{u}(t)\right) + \left[F_1\left(D + \tilde{d}(t)\right) + F_2\left(1 - D - \tilde{d}(t)\right)\right] \\ \Rightarrow Y + \tilde{y}(t) = &\left(C_1 D + C_2(1-D)\right)X + \left(C_1 D + C_2(1-D)\right)\tilde{x}(t) + \left(C_1 - C_2\right)X\tilde{d}(t) + \left(C_1 - C_2\right)\tilde{d}(t)\tilde{x}(t) + \\ &\left(E_1 D + E_2(1-D)\right)U + \left(E_1 D + E_2(1-D)\right)\tilde{u}(t) + \left(E_1 - E_2\right)U\tilde{d}(t) + \left(E_1 - E_2\right)\tilde{d}(t)\tilde{u}(t) + \\ &\left(F_1 D + F_2(1-D)\right) + \left(F_1 - F_2\right)\tilde{d}(t) \end{aligned} \tag{3.10}$$

To obtain the linear model, the second-order non-linear terms (terms having multiplication of two small ac perturbed signals) in (3.9)-(3.10) are neglected and therefore, we get

$$\begin{aligned}\dot{X}+\dot{\tilde{x}}(t)=&\left(A_1D+A_2(1-D)\right)X+\left(A_1D+A_2(1-D)\right)\tilde{x}(t)+\left(A_1-A_2\right)X\tilde{d}(t)+\\&\left(B_1D+B_2(1-D)\right)U+\left(B_1D+B_2(1-D)\right)\tilde{u}(t)+\left(B_1-B_2\right)U\tilde{d}(t)+\\&\left(J_1D+J_2(1-D)\right)+\left(J_1-J_2\right)\tilde{d}(t)\end{aligned}\tag{3.11}$$

$$\begin{aligned}Y+\tilde{y}(t)=&\left(C_1D+C_2(1-D)\right)X+\left(C_1D+C_2(1-D)\right)\tilde{x}(t)+\left(C_1-C_2\right)X\tilde{d}(t)+\\&\left(E_1D+E_2(1-D)\right)U+\left(E_1D+E_2(1-D)\right)\tilde{u}(t)+\left(E_1-E_2\right)U\tilde{d}(t)+\\&\left(F_1D+F_2(1-D)\right)+\left(F_1-F_2\right)\tilde{d}(t)\end{aligned}\tag{3.12}$$

These two equations can be further rewritten as

$$\dot{X}+\dot{\tilde{x}}(t)=\underbrace{AX+BU+J}_{\text{steady-state term}}+\underbrace{A\tilde{x}(t)+B\tilde{u}(t)+B_d\tilde{d}(t)}_{\text{small signal term}}\tag{3.13}$$

$$Y+\tilde{y}(t)=\underbrace{CX+EU+F}_{\text{steady-state term}}+\underbrace{C\tilde{x}(t)+E\tilde{u}(t)+E_d\tilde{d}(t)}_{\text{small signal term}}\tag{3.14}$$

Where,

$$\begin{aligned}&A=A_1D+A_2(1-D),B=B_1D+B_2(1-D),\\&J=J_1D+J_2(1-D),B_d=\left(A_1-A_2\right)X+\left(B_1-B_2\right)U+\left(J_1-J_2\right)\end{aligned}\tag{3.15}$$

and

$$\begin{aligned}&C=C_1D+C_2(1-D),E=E_1D+E_2(1-D),\\&F=F_1D+F_2(1-D),E_d=\left(C_1-C_2\right)X+\left(E_1-E_2\right)U+\left(F_1-F_2\right)\end{aligned}\tag{3.16}$$

Equations (3.13)-(3.14) represent the generalized large-signal linear averaged state-space model of a DC-DC converter. It can be separated to obtain steady-state (dc) and small-signal (ac) model as follows:

Steady-state (dc) model

In (3.13)-(3.14), replacing the small-signal terms by zero, we get the steady-state (DC) model as below:

$$\dot{X}=0=AX+BU+J\tag{3.17}$$

$$Y=CX+EU+F\tag{3.18}$$

On simplifying (3.17),

$$X=-A^{-1}\left(BU+J\right)\tag{3.19}$$

Substituting this value of X into (3.17)

$$Y=-CA^{-1}\left(BU+J\right)+EU+F\ \Rightarrow Y=\left(-CA^{-1}B+E\right)U+\left(-CA^{-1}J+F\right)\tag{3.20}$$

Equations (3.19) and (3.20) can be used to obtain the steady-state value of any state variable (inductor current and capacitor voltage) and output variable (output voltage) of DC-DC converter.

Small-signal (ac) model

By replacing the steady-state (DC) terms in (3.13)-(3.14) to zero, we get

$$\dot{\tilde{x}}(t) = A\tilde{x}(t) + B\tilde{u}(t) + B_d\tilde{d}(t) \tag{3.21}$$

$$\tilde{y}(t) = C\tilde{x}(t) + E\tilde{u}(t) + E_d\tilde{d}(t) \tag{3.22}$$

Step 4: Determination of various transfer functions from small-signal model

Equations (3.21)-(3.22) represent the small-signal state-space averaged model of DC-DC converter. However, to obtain the various transfer functions, the Laplace transform of above state-space model is taken as:

$$s\tilde{x}(s) = A\tilde{x}(s) + B\tilde{u}(s) + B_d\tilde{d}(s) \tag{3.23}$$

$$\tilde{y}(s) = C\tilde{x}(s) + E\tilde{u}(s) + E_d\tilde{d}(s) \tag{3.24}$$

Simplifying (3.23),

$$\tilde{x}(s) = (sI - A)^{-1}B\tilde{u}(s) + (sI - A)^{-1}B_d\tilde{d}(s) \tag{3.25}$$

'*I*' is unit matrix and '*s*' is Laplace operator.

Inserting this value in (3.24),

$$\tilde{y}(s) = C(sI - A)^{-1}\left(B\tilde{u}(s) + B_d\tilde{d}(s)\right) + E\tilde{u}(s) + E_d\tilde{d}(s)$$

$$\Rightarrow \tilde{y}(s) = \left[C(sI - A)^{-1}B + E\right]\tilde{u}(s) + \left[C(sI - A)^{-1}B_d + E_d\right]\tilde{d}(s) \tag{3.26}$$

The equations (3.25) and (3.26) can be used to obtain various transfer functions of DC-DC converter. For a DC-DC converter, $\tilde{x}$ represents inductor current and capacitor voltage perturbations, $\tilde{u}$ represents input voltage and load current perturbations, $\tilde{d}$ represents duty cycle perturbation and $\tilde{y}$ represents output voltage perturbation. The various transfer functions relating these perturbations can be obtained from (3.25)-(3.26) as follows:

Transfer functions relating duty cycle ($\tilde{d}$) and input variable ($\tilde{u}$) to state variable ($\tilde{x}$) are

$$\begin{aligned} \frac{\tilde{x}(s)}{\tilde{u}(s)} &= (sI - A)^{-1}B \\ \frac{\tilde{x}(s)}{\tilde{d}(s)} &= (sI - A)^{-1}B_d \end{aligned} \tag{3.27}$$

Transfer functions relating duty cycle ($\tilde{d}$) and input variable ($\tilde{u}$) to output variable ($\tilde{y}$) are

$$\begin{aligned} \frac{\tilde{y}(s)}{\tilde{u}(s)} &= C(sI - A)^{-1}B + E \\ \frac{\tilde{y}(s)}{\tilde{d}(s)} &= C(sI - A)^{-1}B_d + E_d \end{aligned} \tag{3.28}$$

For a second-order DC-DC converter,

$$\tilde{x}(t) = \begin{bmatrix} \tilde{i}_L(t) \\ \tilde{v}_c(t) \end{bmatrix}, u(t) = \begin{bmatrix} \tilde{v}_g(t) \\ \tilde{i}_z(t) \end{bmatrix}, y = \tilde{v}_o(t) \tag{3.29}$$

$\tilde{i}_L(t)$ is inductor current perturbation, $\tilde{v}_c(t)$ is capacitor voltage perturbation, $\tilde{v}_g(t)$ is input voltage perturbation, $\tilde{i}_z(t)$ is load current perturbation, and $\tilde{v}_o(t)$ is output voltage perturbation.

For a fourth-order DC-DC converter,

$$\tilde{x}(t)=\begin{bmatrix}\tilde{i}_{L1}(t)\\ \tilde{i}_{L2}(t)\\ \tilde{v}_{c1}(t)\\ \tilde{v}_{c2}(t)\end{bmatrix},u(t)=\begin{bmatrix}\tilde{v}_g(t)\\ \tilde{i}_z(t)\end{bmatrix},y=\tilde{v}_o(t) \tag{3.30}$$

$\tilde{i}_{L1}(t)$ and $\tilde{i}_{L2}(t)$ are inductor current perturbations, $\tilde{v}_{c1}(t)$ and $\tilde{v}_{c2}(t)$ are capacitor voltage perturbations, $\tilde{v}_g(t)$ is input voltage perturbation, $\tilde{i}_z(t)$ is load current perturbation, and $\tilde{v}_o(t)$ is output voltage perturbation.

It is observed that to determine the various transfer functions, the calculation of resolvent matrix $(sI-A)^{-1}$ is necessary. The computation of this matrix $(sI-A)^{-1}$ is discussed below.

3.2.1.1 Computation of resolvent matrix $(sI-A)^{-1}$

Generally, for a given system matrix *A,* the resolvent matrix is calculated using conventional matrix inversion formula, which is given as [129]

$$(sI-A)^{-1}=\frac{Adj(sI-A)}{|sI-A|} \tag{3.31}$$

$Adj(sI-A)$ is called adjoint matrix, which is the transpose of the cofactor matrix of *(sI-A)* and $|sI-A|$ is determinant of *(sI-A)*.

However, the calculation of resolvent matrix for a DC-DC converter using this formula has some disadvantages-

- For higher-order converters, the order of system matrix is very high. For example, Cuk, Zeta and SEPIC converters are of fourth-order. For such converters, the evaluation of resolvent matrix using the conventional formula is cumbersome.
- Further, if all the parasitic resistances of inductors, capacitors, diode and MOSFET are also included to obtain the more accurate model, the calculation becomes more complex.
- Moreover, it is difficult to calculate this resolvent matrix using computers due to the presence of Laplace variable '*s*' [130].

Therefore, in this chapter, the Leverrier's algorithm [130] has been used to obtain the transfer functions of non-ideal DC-DC buck and Cuk converter. This algorithm overcomes all the difficulties stated above. Though this algorithm is available in control system literature, but to the best of author's knowledge, it has never been used to obtain the transfer functions of DC-DC converters. This algorithm helps a lot in obtaining various transfer functions of higher-order DC-DC converters including all the non-idealities. This algorithm is explained in following section.

3.2.1.2 Generalized Leverrier's Algorithm

For n^{th} order DC-DC converter, having system matrix A of order nxn, the resolvent matrix using Leverrier's algorithm is given by [130]

$$(sI - A)^{-1} = \frac{Adj(sI - A)}{|sI - A|} = \frac{Q_{n-1}s^{n-1} + Q_{n-2}s^{n-2} + ... + Q_1 s + Q_0}{s^n + a_{n-1}s^{n-1} + ... + a_1 s + a_0} \quad (3.32)$$

Here, Q_i are nxn matrices and a_i are constant coefficients, which are computed in following n steps [130]:

Step 1: In this step, define the matrix Q_{n-1} as an identity matrix I_n of order n, and then calculate coefficient a_{n-1}

$$Q_{n-1} = I_n \quad (3.33)$$

$$a_{n-1} = -trace(Q_{n-1}A) \quad (3.34)$$

Where, I_n is n^{th} order identity matrix.

Step 2: Compute the next matrix Q_{n-2} and coefficient a_{n-2}

$$Q_{n-2} = Q_{n-1}A + a_{n-1}I_n \quad (3.35)$$

$$a_{n-2} = -\frac{1}{2}trace(Q_{n-2}A) \quad (3.36)$$

Step j: In the same way, j^{th} matrix Q_{n-j} and coefficient a_{n-j} are calculated as

$$Q_{n-j} = Q_{n-j+1}A + a_{n-j+1}I_n \quad (3.37)$$

$$a_{n-j} = -\frac{1}{j}trace(Q_{n-j}A) \quad (3.38)$$

Step n: Finally, calculate

$$Q_0 = Q_1 A + a_1 I_n \quad (3.39)$$

$$a_0 = -\frac{1}{n}trace(Q_0 A) \quad (3.40)$$

The beauty of this algorithm is that it can be checked whether all the calculated matrices and coefficients are correct by verifying

$$Q_0 A + a_0 I_n = 0 \quad (3.41)$$

In the subsequent sub-sections, the various transfer functions of non-ideal buck and Cuk converter are derived involving all the non-idealities. These non-idealities include the equivalent series resistances (ESR) of inductors and capacitors, the parasitic resistances of the diode and MOSFET during conduction state and the forward voltage drop of the diode.

3.2.2 Modeling of non-ideal DC-DC buck converter

The circuit diagram of non-ideal DC-DC buck converter is shown in Fig. 3.1(a). As shown in the figure, the buck converter consists of power MOSFET switch S, diode D_d, inductor L, capacitor C and load resistance R [1]. For obtaining the accurate and precise model of the converter, all the major non-idealities which may affect the dynamic and steady-

state response of converter are considered. These non-idealities are equivalent series resistances (ESR) of inductor r_L, ESR of capacitor r_c, switch on-resistance r_{sw}, diode forward resistance r_d and diode forward voltage drop V_F. The values of these parasitic resistances are very small in comparison to load resistance R. The circuit description and operation remain same as discussed in the previous chapter. In this figure, all the currents and voltages are instantaneous and they are functions of time. At the output stage, an additional current source $i_z(t)$ has been added to determine the dynamic effect of load current variation on output voltage response.

In this section, the modeling of non-ideal DC-DC buck converter is carried out by considering it to be operated in CCM. In CCM operation, a DC-DC buck converter has two circuit states (a) when MOSFET switch conducts and diode remains off (b) when MOSFET switch remains off and diode conducts. The state-space equations in these two circuit states are obtained as follows:

Step 1: Obtaining the state equations for each circuit state

Switch on (time interval $0 < t \leq DT$)

For time interval $0<t\leq DT$, the MOSFET switch S is conducting and diode D_d is off. The respective equivalent circuit of non-ideal buck converter is shown in Fig. 3.1(b). The switch is modelled by its on-resistance r_{sw} and the diode is open circuited. By applying Kirchhoff's voltage law and current law (KVL and KCL), the corresponding inductor voltage, capacitor current and output voltage equations are given as:

$$v_L(t) = L\frac{di_L(t)}{dt} = v_g(t) - (r_{sw} + r_L)i_L(t) - v_o(t) \tag{3.42}$$

$$i_c(t) = C\frac{dv_c(t)}{dt} = i_L(t) - \frac{v_o(t)}{R} - i_z(t) \tag{3.43}$$

$$v_o(t) = v_c(t) + r_c i_c(t) \tag{3.44}$$

Substituting (3.43) into (3.44),

$$v_o(t) = v_c(t) + r_c\left(i_L(t) - \frac{v_o(t)}{R} - i_z(t)\right) \Rightarrow \quad v_o(t) = \frac{r_c R}{R + r_c}i_L(t) + \frac{R}{R + r_c}v_c(t) - \frac{r_c R}{R + r_c}i_z(t) \tag{3.45}$$

Substituting (3.45) into (3.42),

$$L\frac{di_L(t)}{dt} = -\left(r_{sw} + r_L + \frac{r_c R}{R + r_c}\right)i_L(t) - \frac{R}{R + r_c}v_c(t) + v_g(t) + \frac{r_c R}{R + r_c}i_z(t) \tag{3.46}$$

Substituting (3.45) into (3.43),

$$C\frac{dv_c(t)}{dt} = \frac{R}{R + r_c}i_L(t) - \frac{1}{R + r_c}v_c(t) - \frac{R}{R + r_c}i_z(t) \tag{3.47}$$

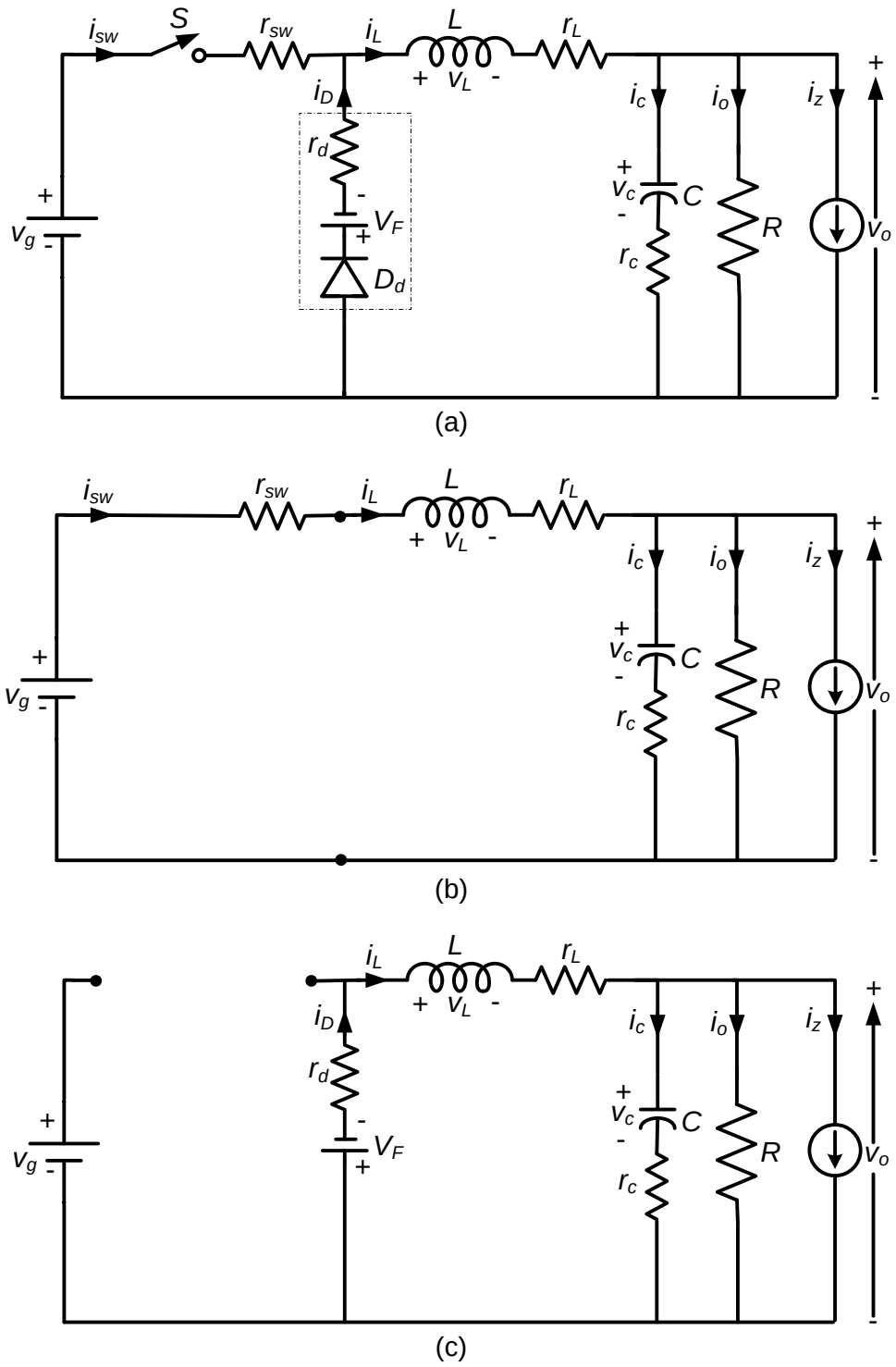


Fig. 3.1. (a) Circuit diagram of non-ideal DC-DC buck converter (b) equivalent circuit during switch-on (c) equivalent circuit during switch off

Equations (3.46), (3.47) and (3.45) can be written in the state-space representation form as follows:

$$\begin{bmatrix} \dfrac{di_L(t)}{dt} \\ \dfrac{dv_c(t)}{dt} \end{bmatrix} = A_1 \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} + B_1 \begin{bmatrix} v_g(t) \\ i_z(t) \end{bmatrix} + J_1 \tag{3.48}$$

$$v_o(t) = C_1 \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} + E_1 \begin{bmatrix} v_g(t) \\ i_z(t) \end{bmatrix} + F_1 \tag{3.49}$$

Where,

$$A_1 = \begin{bmatrix} -\frac{1}{L}\left(r_{sw} + r_L + \frac{r_c R}{R + r_c}\right) & -\frac{1}{L}\left(\frac{R}{R + r_c}\right) \\ \frac{1}{C}\left(\frac{R}{R + r_c}\right) & -\frac{1}{C}\left(\frac{1}{R + r_c}\right) \end{bmatrix}, B_1 = \begin{bmatrix} \frac{1}{L} & \frac{1}{L}\left(\frac{r_c R}{R + r_c}\right) \\ 0 & -\frac{1}{C}\left(\frac{R}{R + r_c}\right) \end{bmatrix}, J_1 = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{3.50}$$

$$C_1 = \begin{bmatrix} \frac{r_c R}{R + r_c} & \frac{R}{R + r_c} \end{bmatrix}, E_1 = \begin{bmatrix} 0 & -\frac{r_c R}{R + r_c} \end{bmatrix}, F_1 = [0]$$

Switch off (time interval $DT < t \leq T$)

For time interval $DT<t\leq T$, the MOSFET switch S is off and diode D_d is conducting. The respective equivalent circuit of non-ideal buck converter is shown in Fig. 3.1(c). The diode is modelled by its on-resistance r_d and forward voltage drop V_F and switch is open circuited. By applying Kirchhoff's voltage law and current law (KVL and KCL), the corresponding inductor voltage, capacitor current and output voltage equations are given as:

$$v_L(t) = L\frac{di_L(t)}{dt} = -V_F - (r_d + r_L) i_L(t) - v_o(t) \tag{3.51}$$

$$i_c(t) = C\frac{dv_c(t)}{dt} = i_L(t) - \frac{v_o(t)}{R} - i_z(t) \tag{3.52}$$

$$v_o(t) = v_c(t) + r_c i_c(t) \tag{3.53}$$

Substituting (3.52) into (3.53),

$$v_o(t) = v_c(t) + r_c\left(i_L(t) - \frac{v_o(t)}{R} - i_z(t)\right) \Rightarrow \; v_o(t) = \frac{r_c R}{R + r_c} i_L(t) + \frac{R}{R + r_c} v_c(t) - \frac{r_c R}{R + r_c} i_z(t) \tag{3.54}$$

Substituting (3.54) into (3.51),

$$L\frac{di_L(t)}{dt} = -\left(r_d + r_L + \frac{r_c R}{R + r_c}\right) i_L(t) - \frac{R}{R + r_c} v_c(t) + \frac{r_c R}{R + r_c} i_z(t) - V_F \tag{3.55}$$

Substituting (3.54) into (3.52),

$$C\frac{dv_c(t)}{dt} = \frac{R}{R + r_c} i_L(t) - \frac{1}{R + r_c} v_c(t) - \frac{R}{R + r_c} i_z(t) \tag{3.56}$$

Equations (3.55), (3.56) and (3.54) can be written in the state-space representation form as follows:

$$\begin{bmatrix} \frac{di_L(t)}{dt} \\ \frac{dv_c(t)}{dt} \end{bmatrix} = A_2 \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} + B_2 \begin{bmatrix} v_g(t) \\ i_z(t) \end{bmatrix} + J_2 \tag{3.57}$$

$$v_o(t) = C_2 \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} + E_2 \begin{bmatrix} v_g(t) \\ i_z(t) \end{bmatrix} + F_2 \tag{3.58}$$

Where,

$$A_2=\begin{bmatrix}-\frac{1}{L}\left(r_d+r_L+\frac{r_cR}{R+r_c}\right) & -\frac{1}{L}\left(\frac{R}{R+r_c}\right)\\ \frac{1}{C}\left(\frac{R}{R+r_c}\right) & -\frac{1}{C}\left(\frac{1}{R+r_c}\right)\end{bmatrix},B_2=\begin{bmatrix}0 & \frac{1}{L}\left(\frac{r_cR}{R+r_c}\right)\\ 0 & -\frac{1}{C}\left(\frac{R}{R+r_c}\right)\end{bmatrix},J_2=\begin{bmatrix}-\frac{V_F}{L}\\ 0\end{bmatrix} \quad (3.59)$$

$$C_2=\begin{bmatrix}\frac{r_cR}{R+r_c} & \frac{R}{R+r_c}\end{bmatrix},E_2=\begin{bmatrix}0 & -\frac{r_cR}{R+r_c}\end{bmatrix},F_2=\begin{bmatrix}0\end{bmatrix}$$

Step 2: Finding the averaged state-space model

As discussed in section 3.2.1, the large-signal non-linear averaged state-space model of non-ideal buck converter can be given as

$$\begin{bmatrix}\frac{d\bar{i}_L(t)}{dt}\\ \frac{d\bar{v}_c(t)}{dt}\end{bmatrix}=A'(t)\begin{bmatrix}\bar{i}_L(t)\\ \bar{v}_c(t)\end{bmatrix}+B'(t)\begin{bmatrix}\bar{v}_g(t)\\ \bar{i}_z(t)\end{bmatrix}+J'(t) \quad (3.60)$$

$$\bar{v}_o(t)=C'(t)\begin{bmatrix}\bar{i}_L(t)\\ \bar{v}_c(t)\end{bmatrix}+E'(t)\begin{bmatrix}\bar{v}_g(t)\\ \bar{i}_z(t)\end{bmatrix}+F'(t) \quad (3.61)$$

Where,

$$\begin{aligned}&A'(t)=A_1d(t)+A_2\left(1-d(t)\right),B'(t)=B_1d(t)+B_2\left(1-d(t)\right),\\ &C'(t)=C_1d(t)+C_2\left(1-d(t)\right),E'(t)=E_1d(t)+E_2\left(1-d(t)\right),\\ &J'(t)=J_1d(t)+J_2\left(1-d(t)\right),F'(t)=F_1d(t)+F_2\left(1-d(t)\right)\end{aligned} \quad (3.62)$$

Step 3: Linearization by introducing small ac perturbation around a DC operating point

The following perturbations in variables are introduced around their respective steady-state (DC) values-

$$\begin{aligned}&\bar{i}_L(t)=I_L+\tilde{i}_L(t),\bar{i}_o(t)=I_o+\tilde{i}_o(t),\bar{i}_z=I_z+\tilde{i}_z(t),d(t)=D+\tilde{d}(t),\\ &\bar{v}_g(t)=V_g+\tilde{v}_g(t),\bar{v}_c(t)=V_c+\tilde{v}_c(t),\bar{v}_o(t)=V_o+\tilde{v}_o(t)\end{aligned}$$

By introducing these values into (3.60)-(3.62), we get the steady-state (dc) and small- signal (ac) model of non-ideal buck converter as follows:

Steady-state (dc) model:

$$\begin{bmatrix}I_L\\ V_c\end{bmatrix}=-A^{-1}\left(B\begin{bmatrix}V_g\\ I_z\end{bmatrix}+J\right) \quad (3.63)$$

$$V_o=C\begin{bmatrix}I_L\\ V_c\end{bmatrix}+E\begin{bmatrix}V_g\\ I_z\end{bmatrix}+F \quad (3.64)$$

Small-signal (ac) model:

$$\begin{bmatrix}\frac{d\tilde{i}_L(t)}{dt}\\ \frac{d\tilde{v}_c(t)}{dt}\end{bmatrix}=A\begin{bmatrix}\tilde{i}_L(t)\\ \tilde{v}_c(t)\end{bmatrix}+B\begin{bmatrix}\tilde{v}_g(t)\\ \tilde{i}_z(t)\end{bmatrix}+B_d\tilde{d}(t) \quad (3.65)$$

$$\tilde{v}_o(t) = C\begin{bmatrix}\tilde{i}_L(t)\\ \tilde{v}_c(t)\end{bmatrix} + E\begin{bmatrix}\tilde{v}_g(t)\\ \tilde{i}_z(t)\end{bmatrix} + E_d\tilde{d}(t) \tag{3.66}$$

Where, the corresponding averaged matrices and vectors are calculated by substituting (3.50) and (3.59) into (3.15)-(3.16) as follows:

$$A = \begin{bmatrix} -\frac{1}{L}\left(r_x + r_L + \frac{r_c R}{R+r_c}\right) & -\frac{1}{L}\left(\frac{R}{R+r_c}\right) \\ \frac{1}{C}\left(\frac{R}{R+r_c}\right) & -\frac{1}{C}\left(\frac{1}{R+r_c}\right)\end{bmatrix}, B = \begin{bmatrix} \frac{D}{L} & \frac{1}{L}\left(\frac{r_c R}{R+r_c}\right) \\ 0 & -\frac{1}{C}\left(\frac{R}{R+r_c}\right)\end{bmatrix}, J = \begin{bmatrix} -\frac{D'V_F}{L} \\ 0\end{bmatrix}, r_x = Dr_{sw} + D'r_d$$

$$C = \begin{bmatrix}\frac{r_c R}{R+r_c} & \frac{R}{R+r_c}\end{bmatrix}, E = \begin{bmatrix}0 & -\frac{r_c R}{R+r_c}\end{bmatrix}, F = [0], B_d = \begin{bmatrix}\frac{V_g + V_F - (r_{sw} - r_d)I_L}{L} \\ 0\end{bmatrix}, E_d = 0 \tag{3.67}$$

By substituting these matrices and vector values in (3.63)-(3.64), the steady-state values are obtained as:

$$I_L = I_o + I_z = \frac{V_o}{R} + I_z \tag{3.68}$$

$$V_o = V_c = \frac{DV_g - D'V_F - I_z(r_L + r_x)}{1 + \frac{1}{R}(r_L + r_x)} \tag{3.69}$$

Step 4: Determination of various transfer functions from small-signal model

For buck converter, there are nine possible transfer functions relating the state variables (i_L, v_c) and output voltage (v_o) with input voltage (v_g), load current (i_o) and duty cycle (d). However, only important transfer functions are derived here. First, the matrix $(sI - A)^{-1}$ is evaluated for buck converter using Leverrier's algorithm as discussed in section 3.2.1.2.

Application of Leverrier's algorithm for buck converter

Buck converter is a second-order system. Therefore, for n=2, the resolvent matrix according to Leverrier's algorithm is given as:

$$(sI - A)^{-1} = \frac{Adj(sI - A)}{|sI - A|} = \frac{Q_1 s + Q_0}{s^2 + a_1 s + a_0} \tag{3.70}$$

The coefficients a_1, a_0 and matrices Q_1, Q_0 are obtained stepwise as follows:

Step 1: Matrix Q_1 and coefficient a_1 are computed in this step.

$$Q_1 = I_2 = \begin{bmatrix}1 & 0\\ 0 & 1\end{bmatrix} \tag{3.71}$$

$$\begin{aligned} a_1 &= -trace(Q_1 A) = -trace(A) \\ &= \frac{1}{L}\left(r_x + r_L + \frac{r_c R}{R+r_c}\right) + \frac{1}{C}\left(\frac{1}{R+r_c}\right) \end{aligned} \tag{3.72}$$

Step 2: Matrix Q_0 and coefficient a_0 are computed in this step.

$$Q_0 = Q_1 A + a_1 I_2 = \begin{bmatrix} \frac{1}{C}\left(\frac{1}{R+r_c}\right) & -\frac{1}{L}\left(\frac{R}{R+r_c}\right) \\ \frac{1}{C}\left(\frac{R}{R+r_c}\right) & \frac{1}{L}\left(r_x + r_L + \frac{r_c R}{R+r_c}\right) \end{bmatrix} \tag{3.73}$$

$$a_o = -\frac{1}{2} trace\left(Q_0 A\right) = \frac{r_x + r_L + R}{LC\left(R+r_c\right)} \tag{3.74}$$

Verification:

$$\begin{aligned} Q_0 A + a_0 I_2 = & \begin{bmatrix} \frac{1}{C}\left(\frac{1}{R+r_c}\right) & -\frac{1}{L}\left(\frac{R}{R+r_c}\right) \\ \frac{1}{C}\left(\frac{R}{R+r_c}\right) & \frac{1}{L}\left(r_x + r_L + \frac{r_c R}{R+r_c}\right) \end{bmatrix} \begin{bmatrix} -\frac{1}{L}\left(r_x + r_L + \frac{r_c R}{R+r_c}\right) & -\frac{1}{L}\left(\frac{R}{R+r_c}\right) \\ \frac{1}{C}\left(\frac{R}{R+r_c}\right) & -\frac{1}{C}\left(\frac{1}{R+r_c}\right) \end{bmatrix} + \\ & \frac{r_x + r_L + R}{LC\left(R+r_c\right)} \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \\ = & \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \end{aligned} \tag{3.75}$$

Therefore, the resolvent matrix is

$$\left(sI - A\right)^{-1} = \frac{Adj(sI - A)}{\left|sI - A\right|} = \frac{\begin{bmatrix} s + \frac{1}{C}\left(\frac{1}{R+r_c}\right) & -\frac{1}{L}\left(\frac{R}{R+r_c}\right) \\ \frac{1}{C}\left(\frac{R}{R+r_c}\right) & s + \frac{1}{L}\left(r_x + r_L + \frac{r_c R}{R+r_c}\right) \end{bmatrix}}{s^2 + \left(\frac{1}{L}\left(r_x + r_L + \frac{r_c R}{R+r_c}\right) + \frac{1}{C}\left(\frac{1}{R+r_c}\right)\right)s + \frac{r_x + r_L + R}{LC\left(R+r_c\right)}} \tag{3.76}$$

Derivations of various transfer functions

Now, the important transfer functions of non-ideal buck converter are derived, which are useful for analysis and controller design.

(i) Input voltage to output voltage transfer function: This transfer function describes that how the variations or disturbances in input voltage affect the output voltage. This transfer function is obtained by considering the effect of disturbances in the duty cycle and output current to be zero. Thus, using (3.28), the input voltage to output voltage transfer function is

$$\frac{\tilde{v}_o(s)}{\tilde{v}_g(s)} = C\left(sI - A\right)^{-1}\left[B\right]_{first\ column} + \left[E\right]_{first\ column} \tag{3.77}$$

Here $[B]_{first\ column}$ and $[E]_{first\ column}$ are the column vectors containing the elements of first column of the matrices B and E, respectively. The corresponding values are substituted from (3.67) and (3.76) into (3.77).

$$\frac{\tilde{v}_o(s)}{\tilde{v}_g(s)}=\begin{bmatrix}\frac{r_cR}{R+r_c} & \frac{R}{R+r_c}\end{bmatrix}\frac{\begin{bmatrix}s+\frac{1}{C}\left(\frac{1}{R+r_c}\right) & -\frac{1}{L}\left(\frac{R}{R+r_c}\right)\\ \frac{1}{C}\left(\frac{R}{R+r_c}\right) & s+\frac{1}{L}\left(r_x+r_L+\frac{r_cR}{R+r_c}\right)\end{bmatrix}}{s^2+\left(\frac{1}{L}\left(r_x+r_L+\frac{r_cR}{R+r_c}\right)+\frac{1}{C}\left(\frac{1}{R+r_c}\right)\right)s+\frac{r_x+r_L+R}{LC(R+r_c)}}\begin{bmatrix}\frac{D}{L}\\ 0\end{bmatrix}+0$$

$$=\frac{\frac{RD}{LC(R+r_c)}(r_cCs+1)}{s^2+\left(\frac{1}{L}\left(r_x+r_L+\frac{r_cR}{R+r_c}\right)+\frac{1}{C}\left(\frac{1}{R+r_c}\right)\right)s+\frac{r_x+r_L+R}{LC(R+r_c)}} \tag{3.78}$$

(ii) Load current to output voltage transfer function: This transfer function describes that how the variations or disturbances in load current appear on the output voltage. This transfer function is obtained by considering the effect of disturbances in input voltage and duty cycle to be zero. Thus, using (3.28) and substituting corresponding values from (3.67) and (3.76) , the load current to output voltage transfer function is

$$\frac{\tilde{v}_o(s)}{\tilde{i}_z(s)}=C(sI-A)^{-1}[B]_{\text{sec ond column}}+[E]_{\text{sec ond column}}$$

$$=\begin{bmatrix}\frac{r_cR}{R+r_c} & \frac{R}{R+r_c}\end{bmatrix}\frac{\begin{bmatrix}s+\frac{1}{C}\left(\frac{1}{R+r_c}\right) & -\frac{1}{L}\left(\frac{R}{R+r_c}\right)\\ \frac{1}{C}\left(\frac{R}{R+r_c}\right) & s+\frac{1}{L}\left(r_x+r_L+\frac{r_cR}{R+r_c}\right)\end{bmatrix}}{s^2+\left(\frac{1}{L}\left(r_x+r_L+\frac{r_cR}{R+r_c}\right)+\frac{1}{C}\left(\frac{1}{R+r_c}\right)\right)s+\frac{r_x+r_L+R}{LC(R+r_c)}}\cdot\begin{bmatrix}\frac{1}{L}\left(\frac{r_cR}{R+r_c}\right)\\ -\frac{1}{C}\left(\frac{R}{R+r_c}\right)\end{bmatrix}+\begin{bmatrix}-\frac{r_cR}{R+r_c}\end{bmatrix}$$

$$=\frac{\frac{-R}{LC(R+r_c)}(r_cCs+1)(Ls+(r_L+r_x))}{s^2+\left(\frac{1}{L}\left(r_x+r_L+\frac{r_cR}{R+r_c}\right)+\frac{1}{C}\left(\frac{1}{R+r_c}\right)\right)s+\frac{r_x+r_L+R}{LC(R+r_c)}} \tag{3.79}$$

(iii) Duty cycle to output voltage transfer function: It describes that how the variations in duty cycle reflect on the output voltage. For this, the effect of disturbances in input voltage and output current are considered zero. This transfer function, which is used for the control design. Therefore, using (3.28) and substituting respective values from (3.67) and (3.76), the duty cycle to output voltage transfer function is

$$\frac{\tilde{v}_o(s)}{\tilde{d}(s)}=C(sI-A)^{-1}B_d+E_d$$

$$=\begin{bmatrix}\frac{r_cR}{R+r_c} & \frac{R}{R+r_c}\end{bmatrix}\frac{\begin{bmatrix}s+\frac{1}{C}\left(\frac{1}{R+r_c}\right) & -\frac{1}{L}\left(\frac{R}{R+r_c}\right)\\ \frac{1}{C}\left(\frac{R}{R+r_c}\right) & s+\frac{1}{L}\left(r_x+r_L+\frac{r_cR}{R+r_c}\right)\end{bmatrix}}{s^2+\left(\frac{1}{L}\left(r_x+r_L+\frac{r_cR}{R+r_c}\right)+\frac{1}{C}\left(\frac{1}{R+r_c}\right)\right)s+\frac{r_x+r_L+R}{LC(R+r_c)}}\cdot\begin{bmatrix}\frac{V_g+V_F-(r_{sw}-r_d)I_L}{L}\\ 0\end{bmatrix}+0$$

$$= \frac{\frac{R\left(V_g + V_F - \left(r_{sw} - r_d\right)I_L\right)}{LC\left(R + r_c\right)}\left(r_c Cs + 1\right)}{s^2 + \left(\frac{1}{L}\left(r_x + r_L + \frac{r_c R}{R + r_c}\right) + \frac{1}{C}\left(\frac{1}{R + r_c}\right)\right)s + \frac{r_x + r_L + R}{LC\left(R + r_c\right)}} \tag{3.80}$$

These transfer functions of non-ideal buck converter have different time domain and frequency domain behavior in comparison to ideal buck converter. The comparison will be carried out later in this chapter. In the following section, the SSA technique is used to obtain the different transfer function of non-ideal Cuk converter.

3.2.3 Modeling of non-ideal DC-DC Cuk converter

Fig. 3.2(a) shows the circuit diagram of non-ideal DC-DC Cuk converter. It comprises of two inductors L_1 , L_2, two capacitors C_1, C_2, MOSFET switch S, diode D_d and load resistor R. The parasitic elements have been considered to get the mathematical model as realistic as possible. These elements are equivalent series resistances (ESR) of inductors r_{L1}, r_{L2}, ESR of capacitors $r_{c1,}$ r_{c2}, switch on-resistance r_{sw}, diode forward resistance r_d and diode forward voltage drop V_F. The values of these parasitic resistances are very small in comparison to load resistance R. The circuit description and operation remain same as discussed in the previous chapter. At the output stage, an additional current source $i_z(t)$ has been added to determine the effect of the load current variation on output voltage response. In the figure, all the currents and voltages are instantaneous and they are functions of time.

The state-space averaging modeling of non-ideal DC-DC Cuk converter is carried out in this section. The converter is considered to be operating in continuous conduction mode (CCM). In CCM operation, it has two circuit states (a) when MOSFET switch is on and diode is off (b) when MOSFET switch S is off and diode is on. The state-space equations in these two circuit states are obtained as follows:

Step 1: Obtaining the state equations for each circuit state

Switch on (time interval $0 < t \leq DT$)

For time interval $0<t\leq DT$, the MOSFET switch S is conducting and diode D_d is off. The respective equivalent circuit of non-ideal Cuk converter is shown in Fig. 3.2(b). The switch is modelled by its on-resistance r_{sw} and the diode is open circuited. By applying Kirchhoff's voltage law and current law (KVL and KCL), the corresponding inductor voltages, capacitor currents and output voltage equations are given as:

$$v_{L1}(t) = L_1 \frac{di_{L1}(t)}{dt} = -\left(r_{sw} + r_{L1}\right)i_{L1}(t) - r_{sw}i_{L2}(t) + v_g(t) \tag{3.81}$$

$$v_{L2}(t) = L_2 \frac{di_{L2}(t)}{dt} = -r_{sw}i_{L1}(t) - \left(r_{sw} + r_{L2} + r_{c1}\right)i_{L2}(t) + v_{c1}(t) - v_o(t) \tag{3.82}$$

$$i_{c1}(t) = C_1 \frac{dv_{c1}(t)}{dt} = -i_{L2}(t) \tag{3.83}$$

$$i_{c2}(t) = C_2 \frac{dv_{c2}(t)}{dt} = i_{L2}(t) - \frac{v_o(t)}{R} - i_z(t) \tag{3.84}$$

$$v_o(t) = v_{c2}(t) + r_{c2} i_{c2}(t) \tag{3.85}$$

Substituting (3.84) into (3.85),

$$v_o(t) = v_{c2}(t) + r_{c2}\left(i_{L2}(t) - \frac{v_o(t)}{R} - i_z(t)\right) \Rightarrow v_o(t) = \frac{r_{c2}R}{R + r_{c2}} i_{L2}(t) + \frac{R}{R + r_{c2}} v_{c2}(t) - \frac{r_{c2}R}{R + r_{c2}} i_z(t) \tag{3.86}$$

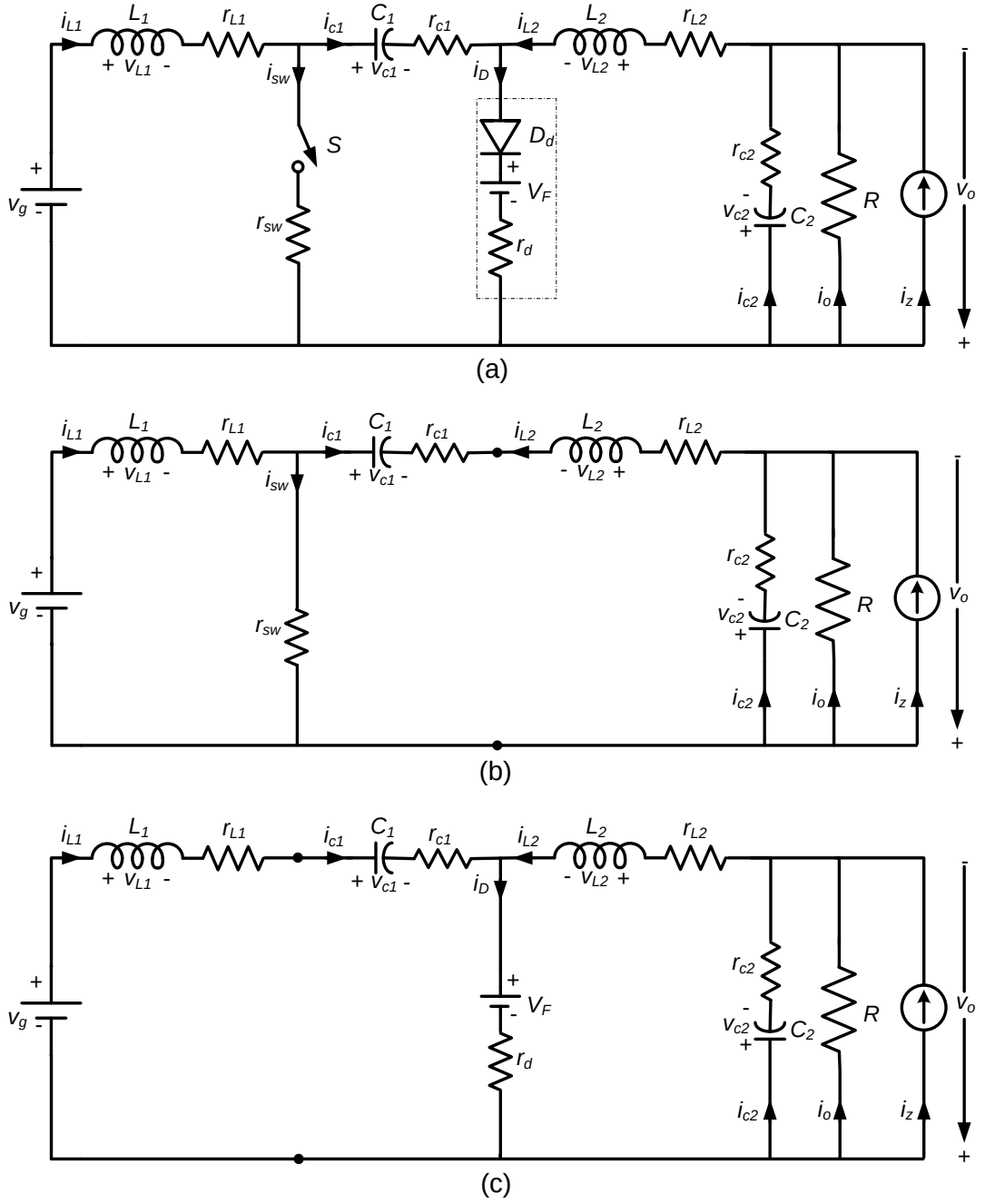


Fig. 3.2.(a) Circuit diagram of non-ideal DC-DC Cuk converter (b) equivalent circuit during switch-on (c) equivalent circuit during switch off

Inserting (3.86) into (3.82) and (3.84), we get respectively

$$L_2\frac{di_{L2}(t)}{dt}=-r_{sw}i_{L1}(t)-\left(r_{sw}+r_{L2}+r_{c1}+\frac{Rr_{c2}}{R+r_{c2}}\right)i_{L2}(t)+v_{c1}(t)-\frac{R}{R+r_{c2}}v_{c2}(t)+\frac{Rr_{c2}}{R+r_{c2}}i_z(t) \quad (3.87)$$

$$C_2\frac{dv_{c2}(t)}{dt}=\frac{R}{R+r_{c2}}i_{L2}(t)-\frac{1}{R+r_{c2}}v_{c2}(t)-\frac{R}{R+r_{c2}}i_z(t) \quad (3.88)$$

Equations (3.81), (3.87), (3.83), (3.88) and (3.86) can be written in the state-space representation form as follows:

$$\begin{bmatrix}\frac{di_{L1}(t)}{dt}\\ \frac{di_{L2}(t)}{dt}\\ \frac{dv_{c1}(t)}{dt}\\ \frac{dv_{c2}(t)}{dt}\end{bmatrix}=A_1\begin{bmatrix}i_{L1}(t)\\ i_{L2}(t)\\ v_{c1}(t)\\ v_{c2}(t)\end{bmatrix}+B_1\begin{bmatrix}v_g(t)\\ i_z(t)\end{bmatrix}+J_1 \quad (3.89)$$

$$v_o(t)=C_1\begin{bmatrix}i_{L1}(t)\\ i_{L2}(t)\\ v_{c1}(t)\\ v_{c2}(t)\end{bmatrix}+E_1\begin{bmatrix}v_g(t)\\ i_z(t)\end{bmatrix}+F_1 \quad (3.90)$$

Where,

$$A_1=\begin{bmatrix}-\frac{(r_{sw}+r_{L1})}{L_1} & -\frac{r_{sw}}{L_1} & 0 & 0\\ -\frac{r_{sw}}{L_2} & -\frac{1}{L_2}\left(r_{sw}+r_{L2}+r_{c1}+\frac{r_{c2}R}{R+r_{c2}}\right) & \frac{1}{L_2} & -\frac{1}{L_2}\left(\frac{R}{R+r_{c2}}\right)\\ 0 & -\frac{1}{C_1} & 0 & 0\\ 0 & \frac{1}{C_2}\left(\frac{R}{R+r_{c2}}\right) & 0 & -\frac{1}{C_2}\left(\frac{1}{R+r_{c2}}\right)\end{bmatrix},B_1=\begin{bmatrix}\frac{1}{L_1} & 0\\ 0 & \frac{1}{L_2}\left(\frac{r_{c2}R}{R+r_{c2}}\right)\\ 0 & 0\\ 0 & -\frac{1}{C_2}\left(\frac{R}{R+r_{c2}}\right)\end{bmatrix},$$

$$J_1=\begin{bmatrix}0\\0\\0\\0\end{bmatrix},C_1=\begin{bmatrix}0 & \frac{r_{c2}R}{R+r_{c2}} & 0 & \frac{R}{R+r_{c2}}\end{bmatrix},E_1=\begin{bmatrix}0 & -\frac{r_{c2}R}{R+r_{c2}}\end{bmatrix},F_1=\begin{bmatrix}0\end{bmatrix} \quad (3.91)$$

Switch off (time interval *DT<t≤T*)

For time interval *DT<t≤ T,* the MOSFET switch *S* is off and diode D_d is conducting. The respective equivalent circuit of non-ideal Cuk converter is shown in Fig. 3.2(c). The diode is modelled by on-resistance r_d and forward voltage drop V_F and the switch is open circuited. By applying Kirchhoff's voltage law and current law (KVL and KCL), the corresponding inductor voltages, capacitor currents and output voltage equations are given as:

$$v_{L1}(t) = L_1 \frac{di_{L1}(t)}{dt} = -(r_d + r_{L1} + r_{c1}) i_{L1}(t) - r_d i_{L2}(t) - v_{c1}(t) + v_g(t) - V_F \quad (3.92)$$

$$v_{L2}(t) = L_2 \frac{di_{L2}(t)}{dt} = -r_d i_{L1}(t) - (r_d + r_{L2}) i_{L2}(t) - v_o(t) - V_F \quad (3.93)$$

$$i_{c1}(t) = C_1 \frac{dv_{c1}(t)}{dt} = i_{L1}(t) \quad (3.94)$$

$$i_{c2}(t) = C_2 \frac{dv_{c2}(t)}{dt} = i_{L2}(t) - \frac{v_o(t)}{R} - i_z(t) \quad (3.95)$$

$$v_o(t) = v_{c2}(t) + r_{c2} i_{c2}(t) \quad (3.96)$$

Substituting (3.95) into (3.96), we get

$$v_o(t) = \frac{r_{c2}R}{R + r_{c2}} i_{L2}(t) + \frac{R}{R + r_{c2}} v_{c2}(t) - \frac{r_{c2}R}{R + r_{c2}} i_z(t) \quad (3.97)$$

Putting (3.97) into (3.93) and (3.95), we get respectively

$$v_{L2}(t) = L_2 \frac{di_{L2}(t)}{dt} = -r_d i_{L1}(t) - \left(r_d + r_{L2} + \frac{r_{c2}R}{R + r_{c2}}\right) i_{L2}(t) - \frac{R}{R + r_{c2}} v_{c2}(t) + \frac{r_{c2}R}{R + r_{c2}} i_z(t) - V_F \quad (3.98)$$

$$C_2 \frac{dv_{c2}(t)}{dt} = \frac{R}{R + r_{c2}} i_{L2}(t) - \frac{1}{R + r_{c2}} v_{c2}(t) - \frac{R}{R + r_{c2}} i_z(t) \quad (3.99)$$

Equations (3.92), (3.98), (3.94), (3.99) and (3.97) can be written in the state-space representation form as follows:

$$\begin{bmatrix} \frac{di_{L1}(t)}{dt} \\ \frac{di_{L2}(t)}{dt} \\ \frac{dv_{c1}(t)}{dt} \\ \frac{dv_{c2}(t)}{dt} \end{bmatrix} = A_2 \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{c1}(t) \\ v_{c2}(t) \end{bmatrix} + B_2 \begin{bmatrix} v_g(t) \\ i_z(t) \end{bmatrix} + J_2 \quad (3.100)$$

$$v_o(t) = C_2 \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{c1}(t) \\ v_{c2}(t) \end{bmatrix} + E_2 \begin{bmatrix} v_g(t) \\ i_z(t) \end{bmatrix} + F_2 \quad (3.101)$$

Where,

$$A_2 = \begin{bmatrix} -\frac{(r_d + r_{L1} + r_{c1})}{L_1} & -\frac{r_d}{L_1} & -\frac{1}{L_1} & 0 \\ -\frac{r_d}{L_2} & -\frac{1}{L_2}\left(r_d + r_{L2} + \frac{r_{c2}R}{R + r_{c2}}\right) & 0 & -\frac{1}{L_2}\left(\frac{R}{R + r_{c2}}\right) \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{1}{C_2}\left(\frac{R}{R + r_{c2}}\right) & 0 & -\frac{1}{C_2}\left(\frac{1}{R + r_{c2}}\right) \end{bmatrix}, B_2 = \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & \frac{1}{L_2}\left(\frac{r_{c2}R}{R + r_{c2}}\right) \\ 0 & 0 \\ 0 & -\frac{1}{C_2}\left(\frac{R}{R + r_{c2}}\right) \end{bmatrix},$$

$$J_2=\begin{bmatrix}-\frac{V_F}{L_1}\\-\frac{V_F}{L_2}\\0\\0\end{bmatrix},C_2=\begin{bmatrix}0 & \frac{r_{c2}R}{R+r_{c2}} & 0 & \frac{R}{R+r_{c2}}\end{bmatrix},E_2=\begin{bmatrix}0 & -\frac{r_{c2}R}{R+r_{c2}}\end{bmatrix},F_2=\begin{bmatrix}0\end{bmatrix} \quad (3.102)$$

Step 2: Finding the averaged state-space model

According to the discussion in section 3.2.1, the large-signal non-linear averaged state-space model of non-ideal Cuk converter can be given as

$$\begin{bmatrix}\frac{d\bar{i}_{L1}(t)}{dt}\\\frac{d\bar{i}_{L2}(t)}{dt}\\\frac{d\bar{v}_{c1}(t)}{dt}\\\frac{d\bar{v}_{c2}(t)}{dt}\end{bmatrix}=A'(t)\begin{bmatrix}\bar{i}_{L1}(t)\\\bar{i}_{L2}(t)\\\bar{v}_{c1}(t)\\\bar{v}_{c2}(t)\end{bmatrix}+B'(t)\begin{bmatrix}\bar{v}_g(t)\\\bar{i}_z(t)\end{bmatrix}+J'(t) \quad (3.103)$$

$$\bar{v}_o(t)=C'(t)\begin{bmatrix}\bar{i}_{L1}(t)\\\bar{i}_{L2}(t)\\\bar{v}_{c1}(t)\\\bar{v}_{c2}(t)\end{bmatrix}+E'(t)\begin{bmatrix}\bar{v}_g(t)\\\bar{i}_z(t)\end{bmatrix}+F'(t) \quad (3.104)$$

Where,

$$\begin{aligned}&A'(t)=A_1d(t)+A_2\left(1-d(t)\right),B'(t)=B_1d(t)+B_2\left(1-d(t)\right),\\&C'(t)=C_1d(t)+C_2\left(1-d(t)\right),E'(t)=E_1d(t)+E_2\left(1-d(t)\right),\\&J'(t)=J_1d(t)+J_2\left(1-d(t)\right),F'(t)=F_1d(t)+F_2\left(1-d(t)\right)\end{aligned} \quad (3.105)$$

Step 3: Linearization by introducing small ac perturbation around a DC operating point

The following perturbations in variables are introduced around their respective steady-state (DC) values-

$$\begin{aligned}&\bar{i}_{L1}(t)=I_{L1}+\tilde{i}_{L1}(t),\bar{i}_{L2}(t)=I_{L2}+\tilde{i}_{L2}(t),\bar{i}_o(t)=I_o+\tilde{i}_o(t),\\&\bar{v}_g(t)=V_g+\tilde{v}_g(t),\bar{i}_z=I_z+\tilde{i}_z(t),d(t)=D+\tilde{d}(t),\\&\bar{v}_{c1}(t)=V_{c1}+\tilde{v}_{c1}(t),\bar{v}_{c2}(t)=V_{c2}+\tilde{v}_{c2}(t),\bar{v}_o(t)=V_o+\tilde{v}_o(t)\end{aligned} \quad (3.106)$$

By introducing these values into (3.103)-(3.105), we get the steady-state (dc) and small-signal (ac) model of non-ideal Cuk converter as follows:

Steady-state (dc) model:

$$\begin{bmatrix}I_{L1}\\I_{L2}\\V_{c1}\\V_{c2}\end{bmatrix}=-A^{-1}\left(B\begin{bmatrix}V_g\\I_z\end{bmatrix}+J\right) \quad (3.107)$$

$$V_o = C\begin{bmatrix} I_{L1} \\ I_{L1} \\ V_{c1} \\ V_{c2} \end{bmatrix} + E\begin{bmatrix} V_g \\ I_z \end{bmatrix} + F \tag{3.108}$$

Small-signal (ac) model:

$$\begin{bmatrix} \frac{d\tilde{i}_{L1}(t)}{dt} \\ \frac{d\tilde{i}_{L2}(t)}{dt} \\ \frac{d\tilde{v}_{c1}(t)}{dt} \\ \frac{d\tilde{v}_{c2}(t)}{dt} \end{bmatrix} = A\begin{bmatrix} \tilde{i}_{L1}(t) \\ \tilde{i}_{L2}(t) \\ \tilde{v}_{c1}(t) \\ \tilde{v}_{c2}(t) \end{bmatrix} + B\begin{bmatrix} \tilde{v}_g(t) \\ \tilde{i}_z(t) \end{bmatrix} + B_d\tilde{d}(t) \tag{3.109}$$

$$\tilde{v}_o(t) = C\begin{bmatrix} \tilde{i}_{L1}(t) \\ \tilde{i}_{L2}(t) \\ \tilde{v}_{c1}(t) \\ \tilde{v}_{c2}(t) \end{bmatrix} + E\begin{bmatrix} \tilde{v}_g(t) \\ \tilde{i}_z(t) \end{bmatrix} + E_d\tilde{d}(t) \tag{3.110}$$

Where, the corresponding averaged matrices and vectors are calculated by substituting (3.91) and (3.102) into (3.15)-(3.16)

$$A = \begin{bmatrix} -\frac{(r_x + r_{L1} + D'r_{c1})}{L_1} & -\frac{r_x}{L_1} & -\frac{D'}{L_1} & 0 \\ -\frac{r_x}{L_2} & -\frac{1}{L_2}\left(r_x + r_{L2} + Dr_{c1} + \frac{r_{c2}R}{R + r_{c2}}\right) & \frac{D}{L_2} & -\frac{1}{L_2}\left(\frac{R}{R + r_{c2}}\right) \\ \frac{D'}{C_1} & -\frac{D}{C_1} & 0 & 0 \\ 0 & \frac{1}{C_2}\left(\frac{R}{R + r_{c2}}\right) & 0 & -\frac{1}{C_2}\left(\frac{1}{R + r_{c2}}\right) \end{bmatrix}, J = \begin{bmatrix} -\frac{D'V_F}{L_1} \\ -\frac{D'V_F}{L_2} \\ 0 \\ 0 \end{bmatrix},$$

$$B = \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & \frac{1}{L_2}\left(\frac{r_{c2}R}{R + r_{c2}}\right) \\ 0 & 0 \\ 0 & -\frac{1}{C_2}\left(\frac{R}{R + r_{c2}}\right) \end{bmatrix}, C = \begin{bmatrix} 0 & \frac{r_{c2}R}{R + r_{c2}} & 0 & \frac{R}{R + r_{c2}} \end{bmatrix}, E = \begin{bmatrix} 0 & -\frac{r_{c2}R}{R + r_{c2}} \end{bmatrix}, F = [0], r_x = Dr_{sw} + D'r_d,$$

$$B_d = \begin{bmatrix} \frac{V_{c1} + V_F + (r_d - r_{sw} + r_{c1})I_{L1} + (r_d - r_{sw})I_{L2}}{L_1} \\ \frac{V_{c1} + V_F + (r_d - r_{sw})I_{L1} + (r_d - r_{sw} - r_{c1})I_{L2}}{L_2} \\ -\frac{(I_{L1} + I_{L2})}{C_1} \\ 0 \end{bmatrix} = \begin{bmatrix} \frac{V_{c1} + V_F + \frac{(r_d - r_{sw} + Dr_{c1})}{D'}I_{L2}}{L_1} \\ \frac{V_{c1} + V_F - \left(r_{c1} + \frac{r_{sw} - r_d}{D'}\right)I_{L2}}{L_2} \\ \frac{-I_{L2}}{D'C_1} \\ 0 \end{bmatrix}, E_d = 0 \tag{3.111}$$

By substituting these matrices and vector values in (3.107)-(3.108), the steady-state values are obtained as:

$$I_{L1} = \frac{D}{D'} I_{L2} \tag{3.112}$$

$$I_{L2} = I_o + I_z = \frac{V_o}{R} + I_z \tag{3.113}$$

$$V_{c1} = \frac{V_g}{D'} - V_F - \frac{\left(Dr_{L1} + DD'r_{c1} + r_x\right)}{D'^2} I_{L2} \tag{3.114}$$

$$V_o = V_{c2} = \frac{\frac{D}{D'}V_g - V_F - I_z\left(\left(\frac{D}{D'}\right)^2 r_{L1} + r_{L2} + \frac{D}{D'}r_{c1} + \frac{r_x}{D'^2}\right)}{1 + \frac{1}{R}\left(\left(\frac{D}{D'}\right)^2 r_{L1} + r_{L2} + \frac{D}{D'}r_{c1} + \frac{r_x}{D'^2}\right)} \tag{3.115}$$

Step 4: Determination of various transfer functions from small-signal model

For the Cuk converter, fifteen transfer functions are possible relating the four state variables (i_{L1}, i_{L2}, v_{c1}, v_{c2}) and output voltage (v_o) with input voltage (v_g), load current (i_o) and duty cycle (d). However, only important transfer functions are derived here. First, the matrix $\left(sI - A\right)^{-1}$ is evaluated for Cuk converter using Leverrier's algorithm as discussed in section 3.2.1.2.

Application of Leverrier's algorithm for Cuk converter

Cuk converter is a fourth-order system. Therefore, for n=4, the resolvent matrix according to Leverrier's algorithm is given as:

$$\left(sI - A\right)^{-1} = \frac{Adj(sI - A)}{\left|sI - A\right|} = \frac{Q_3 s^3 + Q_2 s^2 + Q_1 s + Q_0}{s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \tag{3.116}$$

The coefficients a_3, a_2 a_1, a_0 and matrices Q_3, Q_2, Q_1, Q_0 are obtained stepwise as follows:

Step 1: Matrix Q_3 and coefficient a_3 are determined in this step.

$$Q_3 = I_4 = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \tag{3.117}$$

$$\begin{aligned} a_3 &= -trace\left(Q_3 A\right) = -trace\left(A\right) \\ &= \frac{\left(r_x + r_{L1} + D'r_{c1}\right)}{L_1} + \frac{1}{L_2}\left(r_x + r_{L2} + Dr_{c1} + \frac{r_{c2}R}{R + r_{c2}}\right) + \frac{1}{C_2}\left(\frac{1}{R + r_{c2}}\right) \end{aligned} \tag{3.118}$$

Step 2: Matrix Q_2 and coefficient a_2 are computed in this step.

$$Q_2 = Q_3 A + a_3 I_4 = \begin{bmatrix} a_3 - \frac{\left(r_x + r_{L1} + D'r_{c1}\right)}{L_1} & -\frac{r_x}{L_1} & -\frac{D'}{L_1} & 0 \\ -\frac{r_x}{L_2} & \frac{\left(r_x + r_{L1} + D'r_{c1}\right)}{L_1} + \frac{1}{C_2}\left(\frac{1}{R + r_{c2}}\right) & \frac{D}{L_2} & -\frac{1}{L_2}\left(\frac{R}{R + r_{c2}}\right) \\ \frac{D'}{C_1} & -\frac{D}{C_1} & a_3 & 0 \\ 0 & \frac{1}{C_2}\left(\frac{R}{R + r_{c2}}\right) & 0 & a_3 - \frac{1}{C_2}\left(\frac{1}{R + r_{c2}}\right) \end{bmatrix} \tag{3.119}$$

$$a_2 = -\frac{1}{2}trace(Q_2 A)$$
$$= \frac{1}{L_1 L_2}\left(\left(r_x + r_{L1} + D'r_{c1}\right)\left(r_{L2} + Dr_{c1} + \frac{r_{c2}R}{R + r_{c2}}\right) + r_x\left(r_{L1} + D'r_{c1}\right)\right) + \quad (3.120)$$
$$\frac{D'^2}{L_1 C_1} + \frac{\left(r_x + r_{L1} + D'r_{c1}\right)}{L_1 C_2\left(R + r_{c2}\right)} + \frac{D^2}{L_2 C_1} + \frac{\left(R + r_x + r_{L2} + Dr_{c1}\right)}{L_2 C_2\left(R + r_{c2}\right)}$$

Step 3: Matrix Q_1 and coefficient a_1 are calculated in this step.

$$Q_1 = Q_2 A + a_2 I_4 = \begin{bmatrix} q_1^{11} & q_1^{12} & q_1^{13} & q_1^{14} \\ q_1^{21} & q_1^{22} & q_1^{23} & q_1^{24} \\ q_1^{31} & q_1^{32} & q_1^{33} & q_1^{34} \\ q_1^{41} & q_1^{42} & q_1^{43} & q_1^{44} \end{bmatrix} \quad (3.121)$$

Where,

$$q_1^{11} = \frac{D^2}{L_2 C_1} + \frac{\left(R + r_x + r_{L2} + Dr_{c1}\right)}{L_2 C_2\left(R + r_{c2}\right)}, q_1^{12} = \frac{-r_x}{L_1 C_2\left(R + r_{c2}\right)} + \frac{DD'}{L_1 C_1},$$

$$q_1^{13} = \frac{-1}{L_1 L_2}\left(r_x + D'r_{L2} + DD'r_{c1} + \frac{D'r_{c2}R}{R + r_{c2}}\right) - \frac{D'}{L_1 C_2\left(R + r_{c2}\right)},$$

$$q_1^{14} = \frac{Rr_x}{L_1 L_2\left(R + r_{c2}\right)}, q_1^{21} = \frac{-r_x}{L_2 C_2\left(R + r_{c2}\right)} + \frac{DD'}{L_2 C_1}, q_1^{22} = \frac{\left(r_x + r_{L1} + D'r_{c1}\right)}{L_1 C_2\left(R + r_{c2}\right)} + \frac{D'^2}{L_1 C_1},$$

$$q_1^{23} = \frac{\left(r_x + Dr_{L1} + DD'r_{c1}\right)}{L_1 L_2} + \frac{D}{L_2 C_2\left(R + r_{c2}\right)}, q_1^{24} = \frac{-R\left(r_x + r_{L1} + D'r_{c1}\right)}{L_1 L_2\left(R + r_{c2}\right)},$$

$$q_1^{31} = \frac{1}{L_2 C_1}\left(r_x + D'r_{L2} + DD'r_{c1} + \frac{D'r_{c2}R}{R + r_{c2}}\right) + \frac{D'}{C_1 C_2\left(R + r_{c2}\right)}, q_1^{32} = \frac{-\left(r_x + Dr_{L1} + DD'r_{c1}\right)}{L_1 C_1} - \frac{D}{C_1 C_2\left(R + r_{c2}\right)},$$

$$q_1^{33} = \frac{1}{L_1 L_2}\left(\left(r_x + r_{L1} + D'r_{c1}\right)\left(r_{L2} + Dr_{c1} + \frac{r_{c2}R}{R + r_{c2}}\right) + r_x\left(r_{L1} + D'r_{c1}\right)\right) + \frac{\left(r_x + r_{L1} + D'r_{c1}\right)}{L_1 C_2\left(R + r_{c2}\right)} + \frac{\left(R + r_x + r_{L2} + Dr_{c1}\right)}{L_2 C_2\left(R + r_{c2}\right)},$$

$$q_1^{34} = \frac{DR}{L_2 C_1\left(R + r_{c2}\right)}, q_1^{41} = \frac{-Rr_x}{L_2 C_2\left(R + r_{c2}\right)}, q_1^{42} = \frac{R\left(r_x + r_{L1} + D'r_{c1}\right)}{L_1 C_2\left(R + r_{c2}\right)},$$

$$q_1^{43} = \frac{DR}{L_2 C_2\left(R + r_{c2}\right)}, q_1^{44} = \frac{1}{L_1 L_2}\left(\left(r_x + r_{L1} + D'r_{c1}\right)\left(r_{L2} + Dr_{c1} + \frac{r_{c2}R}{R + r_{c2}}\right) + r_x\left(r_{L1} + D'r_{c1}\right)\right) + \frac{D'^2}{L_1 C_1} + \frac{D^2}{L_2 C_1}$$

$$a_1 = -\frac{1}{3}trace(Q_1 A) = \frac{1}{L_1 L_2 C_1}\left(r_x + D^2 r_{L1} + D'^2 r_{L2} + DD'r_{c1} + D'^2\left(\frac{r_{c2}R}{R + r_{c2}}\right)\right) + \quad (3.122)$$
$$\frac{\left(\left(r_x + r_{L1} + D'r_{c1}\right)\left(R + r_{L2} + Dr_{c1}\right) + r_x\left(r_{L1} + D'r_{c1}\right)\right)}{L_1 L_2 C_2\left(R + r_{c2}\right)} + \frac{D^2 L_1 + D'^2 L_2}{L_1 L_2 C_1 C_2\left(R + r_{c2}\right)}$$

Step 4: Matrix Q_0 and coefficient a_0 are computed in this step.

$$Q_0 = Q_1 A + a_1 I_4 = \begin{bmatrix} q_0^{11} & q_0^{12} & q_0^{13} & q_0^{14} \\ q_0^{21} & q_0^{22} & q_0^{23} & q_0^{24} \\ q_0^{31} & q_0^{32} & q_0^{33} & q_0^{34} \\ q_0^{41} & q_0^{42} & q_0^{43} & q_0^{44} \end{bmatrix} \quad (3.123)$$

Where,

$$q_0^{11}=\frac{D^2}{L_2C_1C_2\left(R+r_{c2}\right)},q_0^{12}=\frac{DD'}{L_1C_1C_2\left(R+r_{c2}\right)},q_0^{13}=-\frac{D'R+r_x+D'r_{L2}+DD'r_{c1}}{L_1L_2C_2\left(R+r_{c2}\right)},$$

$$q_0^{14}=\frac{-DD'R}{L_1L_2C_1\left(R+r_{c2}\right)},q_0^{21}=\frac{DD'}{L_2C_1C_2\left(R+r_{c2}\right)},q_0^{22}=\frac{D'^2}{L_1C_1C_2\left(R+r_{c2}\right)},$$

$$q_0^{23}=\frac{r_x+Dr_{L1}+DD'r_{c1}}{L_1L_2C_2\left(R+r_{c2}\right)},q_0^{24}=\frac{-D'^2R}{L_1L_2C_1\left(R+r_{c2}\right)},q_0^{31}=\frac{D'R+r_x+D'r_{L2}+DD'r_{c1}}{L_2C_1C_2\left(R+r_{c2}\right)},$$

$$q_0^{32}=-\frac{r_x+Dr_{L1}+DD'r_{c1}}{L_1C_1C_2\left(R+r_{c2}\right)},q_0^{33}=\frac{\left(\left(r_x+r_{L1}+D'r_{c1}\right)\left(R+r_{L2}+Dr_{c1}\right)+r_x\left(r_{L1}+D'r_{c1}\right)\right)}{L_1L_2C_2\left(R+r_{c2}\right)},$$

$$q_0^{34}=\frac{R\left(r_x+Dr_{L1}+DD'r_{c1}\right)}{L_1L_2C_1\left(R+r_{c2}\right)},q_0^{41}=\frac{RDD'}{L_2C_1C_2\left(R+r_{c2}\right)},q_0^{42}=\frac{D'^2R}{L_1C_1C_2\left(R+r_{c2}\right)},$$

$$q_0^{43}=\frac{R\left(r_x+Dr_{L1}+DD'r_{c1}\right)}{L_1L_2C_2\left(R+r_{c2}\right)},q_0^{44}=\frac{1}{L_1L_2C_1}\left(r_x+D^2r_{L1}+D'^2r_{L2}+DD'r_{c1}+D'^2\left(\frac{r_{c2}R}{R+r_{c2}}\right)\right)$$

$$a_0=-\frac{1}{4}trace\left(Q_0A\right)=\frac{D'^2R+D^2r_{L1}+D'^2r_{L2}+DD'r_{c1}+r_x}{L_1L_2C_1C_2\left(R+r_{c2}\right)} \tag{3.124}$$

Verification:

$$Q_0A+a_0I_4=\begin{bmatrix}0&0&0&0\\0&0&0&0\\0&0&0&0\\0&0&0&0\end{bmatrix} \tag{3.125}$$

Derivations of various transfer functions

Now, the important transfer functions of non-ideal Cuk converter are derived, which are useful for analysis and controller design.

(i) Input voltage to output voltage transfer function: This transfer function describes that how the variations or disturbances in input voltage affect the output voltage. This transfer function is obtained by considering the effect of disturbances in the duty cycle and output current to be zero. Thus, using (3.28), the input voltage to output voltage transfer function is

$$\frac{\tilde{v}_o\left(s\right)}{\tilde{v}_g\left(s\right)}=C\left(sI-A\right)^{-1}\left[B\right]_{first\ column}+\left[E\right]_{first\ column} \tag{3.126}$$

Here, $[B]_{first\ column}$ and $[E]_{first\ column}$ are the column vectors containing elements of the first column of the matrix B and E, respectively. Substituting values from (3.111) and (3.116) into (3.126), we get

$$\frac{\tilde{v}_o\left(s\right)}{\tilde{v}_g\left(s\right)}=\begin{bmatrix}0&\frac{r_{c2}R}{R+r_{c2}}&0&\frac{R}{R+r_{c2}}\end{bmatrix}\frac{Q_3s^3+Q_2s^2+Q_1s+Q_0}{s^4+a_3s^3+a_2s^2+a_1s+a_0}\begin{bmatrix}\frac{1}{L_1}\\0\\0\\0\end{bmatrix}+0 \tag{3.127}$$

Substituting the matrices Q_i and coefficients a_i from (3.117)-(3.124) into (3.127) and simplifying, we get

$$\frac{\tilde{v}_o(s)}{\tilde{v}_g(s)} = \frac{K_{og}(ps+1)(p_{g1}s + p_{g0})}{s^4 + a_3 s^3 + a_2 s^2 + a_1 s^1 + a_0} \tag{3.128}$$

Where, $K_{og} = \dfrac{R}{L_1 L_2 C_1 C_2 (R + r_{c2})}, p = r_{c2} C_2, p_{g1} = -r_x C_1, p_{g0} = DD',$

(ii) Load current to output voltage transfer function: This transfer function describes that how the variations or disturbances in load current affects the output voltage. This transfer function is obtained by considering the effect of disturbances in input voltage and duty cycle to be zero. Thus, using (3.28), the load current to output voltage transfer function is

$$\frac{\tilde{v}_o(s)}{\tilde{i}_z(s)} = C(sI - A)^{-1}[B]_{\text{sec ond column}} + [E]_{\text{sec ond column}} \tag{3.129}$$

Substituting values from (3.111) and (3.116), we get

$$\frac{\tilde{v}_o(s)}{\tilde{i}_z(s)} = \begin{bmatrix} 0 & \dfrac{r_{c2}R}{R + r_{c2}} & 0 & \dfrac{R}{R + r_{c2}} \end{bmatrix} \frac{Q_3 s^3 + Q_2 s^2 + Q_1 s + Q_0}{s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \begin{bmatrix} 0 \\ \dfrac{1}{L_2}\left(\dfrac{r_{c2}R}{R + r_{c2}}\right) \\ 0 \\ -\dfrac{1}{C_2}\left(\dfrac{R}{R + r_{c2}}\right) \end{bmatrix} + \begin{bmatrix} -\dfrac{r_{c2}R}{R + r_{c2}} \end{bmatrix} \tag{3.130}$$

Substituting the matrices Q_i and coefficients a_i from (3.117)-(3.124) into (3.130) and simplifying, we get

$$\frac{\tilde{v}_o(s)}{\tilde{i}_z(s)} = \frac{K_{oz}(ps+1)(p_{z3}s^3 + p_{z2}s^2 + p_{z1}s + p_{z0})}{s^4 + a_3 s^3 + a_2 s^2 + a_1 s^1 + a_0} \tag{3.131}$$

Where,

$$K_{oz} = \frac{-R}{L_1 L_2 C_1 C_2 (R + r_{c2})}, p = r_{c2} C_2, p_{z3} = L_1 L_2 C_2, p_{z2} = L_1 C_1 (r_x + r_{L2} + D r_{c1}) + L_2 C_1 (r_x + r_{L1} + D' r_{c1}),$$

$$p_{z1} = D^2 L_1 + D'^2 L_2 + C_1\left((r_x + r_{L1} + D' r_{c1})(r_{L2} + D r_{c1}) + r_x (r_{L1} + D' r_{c1})\right), p_{z0} = D^2 r_{L1} + D'^2 r_{L2} + DD' r_{c1} + r_x$$

(iii) Duty cycle to output voltage transfer function: This transfer function describes that how the variations in duty cycle reflect on the output voltage. This transfer function is obtained by considering the effect of disturbances in input voltage and output current to be zero. Therefore, using (3.28), the duty cycle to output voltage transfer function is

$$\frac{\tilde{v}_o(s)}{\tilde{d}(s)} = C(sI - A)^{-1} B_d + E_d \tag{3.132}$$

Substituting values from (3.111) and (3.116),

$$\frac{\tilde{v}_o(s)}{\tilde{d}(s)}=\begin{bmatrix}0 & \dfrac{r_{c2}R}{R+r_{c2}} & 0 & \dfrac{R}{R+r_{c2}}\end{bmatrix}\frac{Q_3s^3+Q_2s^2+Q_1s+Q_0}{s^4+a_3s^3+a_2s^2+a_1s+a_0}\begin{bmatrix}\dfrac{V_{c1}+V_F+\frac{(r_d-r_{sw}+Dr_{c1})}{D'}I_{L2}}{L_1}\\ \dfrac{V_{c1}+V_F-\left(r_{c1}+\frac{r_{sw}-r_d}{D'}\right)I_{L2}}{L_2}\\ \dfrac{-I_{L2}}{D'C_1}\\ 0\end{bmatrix}+0 \quad (3.133)$$

Substituting the matrices Q_i and coefficients a_i from (3.117)-(3.124) into (3.133) and simplifying, we get

$$\frac{\tilde{v}_o(s)}{\tilde{d}(s)}=\frac{K_{od}\left(ps+1\right)\left(ps+1\right)\left(p_{d2}s^2+p_{d1}s+p_{d0}\right)}{s^4+a_3s^3+a_2s^2+a_1s^1+a_0} \quad (3.134)$$

Where,

$$K_{od}=\frac{R}{L_1L_2C_1C_2\left(R+r_{c2}\right)},p=r_{c2}C_2,p_{d1}=\left(r_{L1}+D'r_{c1}\right)C_1\left(V_{c1}+V_F\right)-L_1I_{L1}-\left(\left(r_{L1}+D'r_{c1}\right)\left(r_{c1}+\frac{r_{sw}}{D'^2}\right)-\frac{r_{L1}r_X}{D'^2}\right)C_1I_{L2}$$

$$p_{d2}=L_1C_1\left[V_{c1}+V_F-I_{L2}\left(r_{c1}+\frac{r_{sw}-r_D}{D'}\right)\right],p_{d0}=D'\left(V_{c1}+V_F\right)-\left(\frac{D}{D'}r_{L1}+D'r_{c1}+\frac{r_{sw}}{D'}\right)I_{L2}$$

3.3 Averaged Switch Model Technique

The DC-DC converters have semiconductor devices (MOSFET and diodes) for switching action. These semiconductor devices are non-linear in nature and therefore, cause non-linearity in the model of DC-DC converter. The key step in the mathematical modeling of DC-DC converters is to get the linearized model. As discussed earlier, many techniques have been developed for modeling of the switched-mode power converters. Among them, SSA technique has been used in the previous section to obtain the mathematical model of non-ideal DC-DC buck and Cuk converter. In SSA technique, the state equations for switch-on and switch-off period were first averaged to get the large-signal non-linear averaged model of DC-DC converter. Then, this non-linear averaged model was linearized by introducing the small-signal perturbations around an equilibrium point. The resultant large-signal linear model was separated to obtain the steady-state and small-signal model of the DC-DC converters. Finally, the various transfer functions were obtained from the small-signal model. Though this technique is a pure analytical based on matrix algebra, it requires lot of calculations to obtain the transfer function models of DC-DC converter. Another well-known technique for modeling of DC-DC converters has been reported in literature called averaged switch model technique [3], [67].

In averaged switch model technique, the converter switch and diode are replaced by their large-signal averaged models. The voltage across and current through these devices during switch-on and switch-off are averaged. This large-signal model is characterized by a combination of controlled voltage and current sources. In research paper [66], the averaged

switch model technique has been presented in which the switch and diode are considered to form a three-terminal network (called the PWM-switch or switch network). It suggests a generalized averaged circuit model which can be used to replace the PWM-switch (switch and diode) in any DC-DC converter. However, it is difficult to solve the resultant circuit to obtain the various transfer functions of the higher-order converters such as Cuk, Zeta and SEPIC converters.

The aim of this section is to obtain the mathematical model of non-ideal DC-DC buck converter and Cuk converter using averaged switch model approach. The model of non-ideal buck converter using PWM- switch model approach has been obtained in [131]. They have taken the averaged effect of parasitic elements. The reflection rules based on the principle of energy conversion were used to obtain the averaged value of parasitic components. However, it requires additional computational efforts. In this chapter, the effects of parasitics are considered in their original branch avoiding the unnecessary calculations for averaging the effect of parasitic elements to a particular branch. For this purpose, the averaged model for MOSFET and diode are substituted individually. In the same manner, this technique has also been used for modeling of non-ideal DC-DC Cuk converter. The various transfer function models thus obtained can be used for analysis and controller design implementing different control strategies.

3.3.1 Modeling of non-ideal DC-DC buck converter

The basic circuit diagram of non-ideal buck converter is given in Fig. 3.3. The inductor, capacitor, switch and diode have been represented in their non-ideal form. The instantaneous voltage across the ideal switch and ideal diode are denoted by v_{sw} and v_D respectively, whereas the instantaneous current through switch and diode are denoted by i_{sw} and i_D, respectively. The converter is considered to be operating in continuous conduction mode (CCM).

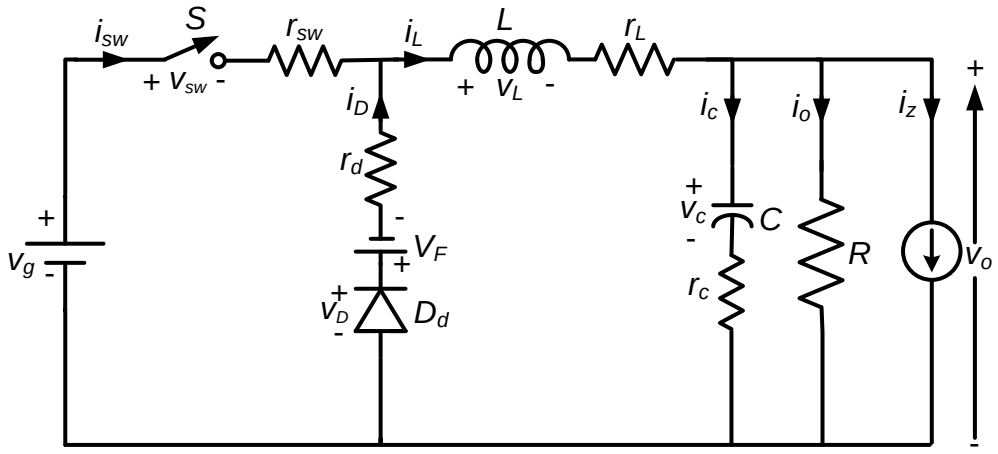


Fig. 3.3. Basic circuit of non-ideal DC-DC buck converter

In CCM operation, it has two circuit states (a) when MOSFET switch is on and diode is off (b) when MOSFET switch is off and diode is on. The step-wise procedure to obtain the steady-state and small-signal model of buck converter using averaged switch model technique is given as follows:

Step 1: Obtain the averaged model of switch and diode

The equivalent circuit diagram of buck converter during switch-on period ($0<t\leq DT$) and switch-off period ($DT<t\leq T$) are given in Fig. 3.4. From these figure, the voltage and current relationships for switch S and diode D_d can easily be obtained.

The instantaneous switch voltage (v_{sw}) and switch current (i_{sw}) are given as

$$v_{sw}(t)=\begin{cases}0 & \text{for } 0<t\leq dT\\ v_g(t)+V_F+r_d i_L(t) & \text{for } dT<t\leq T\end{cases} \tag{3.135}$$

$$i_{sw}(t)=\begin{cases}i_L(t) & \text{for } 0<t\leq dT\\ 0 & \text{for } dT<t\leq T\end{cases} \tag{3.136}$$

The instantaneous diode voltage (v_D) and diode current (i_D) are given as

$$v_D(t)=\begin{cases}v_g(t)-r_{sw}i_L(t) & \text{for } 0<t\leq dT\\ 0 & \text{for } dT<t\leq T\end{cases} \tag{3.137}$$

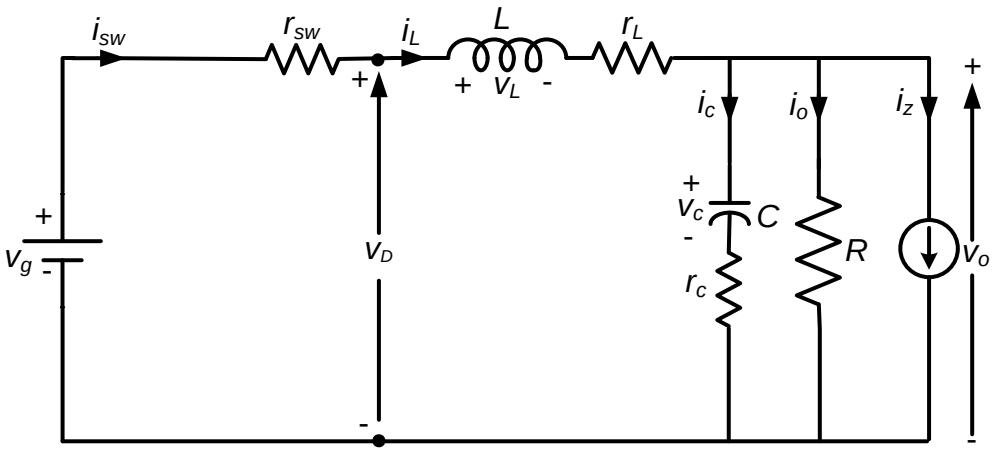
$$i_D(t)=\begin{cases}0 & \text{for } 0<t\leq dT\\ i_L(t) & \text{for } dT<t\leq T\end{cases} \tag{3.138}$$

These instantaneous voltages and currents are time averaged over one switching cycle to obtain the averaged switch and diode model.

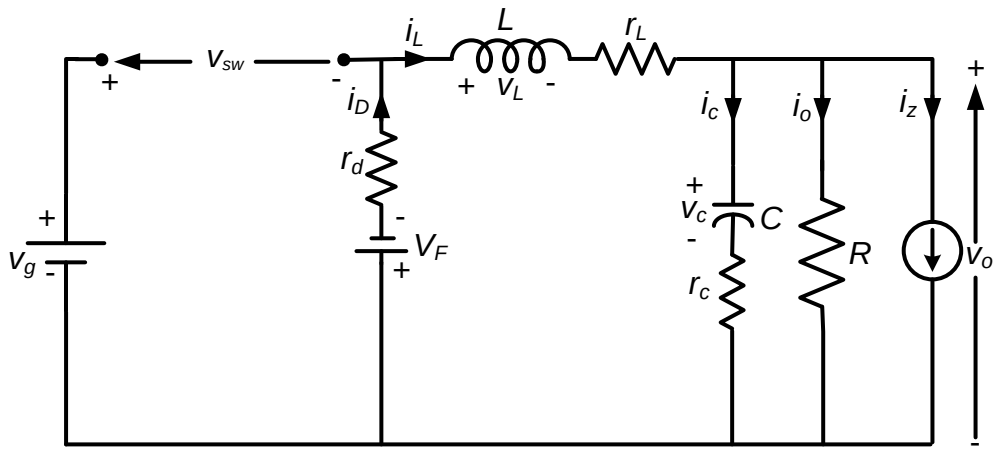
The averaged switch voltage and switch current are obtained as

$$\bar{v}_{sw}(t)=d'(t)\left[\bar{v}_g(t)+V_F+r_d\bar{i}_L(t)\right] \tag{3.139}$$

$$\bar{i}_{sw}(t)=d(t)\bar{i}_L(t) \tag{3.140}$$



(a)



(b)

Fig. 3.4. Equivalent circuit diagram of non-ideal buck converter during (a) switch-on (b) switch-off

The averaged diode voltage and current are obtained as

$$\bar{v}_D(t) = d(t)\left[\bar{v}_g(t) - r_{sw}\bar{i}_L(t)\right] \tag{3.141}$$

$$\bar{i}_D(t) = d'(t)\bar{i}_L(t) \tag{3.142}$$

Where, $d'(t) = 1 - d(t)$

The averaged equations of switch and diode in (3.139)-(3.142) are non-linear because they have multiplication of two time-varying quantities. This is large-signal non-linear averaged switch model of DC-DC buck converter.

Step 2: Linearization of the averaged switch model by introducing small perturbations

In order to obtain the small-signal (ac) model of buck converter, the above non-linear averaged switch model is linearized around a steady-state (DC) operating point. For this purpose, small ac perturbations are introduced around the steady-state (DC) operating point as follows:

$$\begin{aligned}
&\bar{v}_{sw}(t) = V_{sw} + \tilde{v}_{sw}(t), \bar{i}_{sw}(t) = I_{sw} + \tilde{i}_{sw}(t), \bar{v}_D(t) = V_D + \tilde{v}_D(t), \bar{i}_D(t) = I_D + \tilde{i}_D(t), \\
&\bar{v}_g(t) = V_g + \tilde{v}_g(t), \bar{i}_L(t) = I_L + \tilde{i}_L(t), d(t) = D + \tilde{d}(t), d'(t) = D' - \tilde{d}(t), \\
&\bar{i}_o(t) = I_o + \tilde{i}_o(t), \bar{i}_z = I_z + \tilde{i}_z(t), \bar{v}_c(t) = V_c + \tilde{v}_c(t), \bar{v}_o(t) = V_o + \tilde{v}_o(t)
\end{aligned} \tag{3.143}$$

The variables having symbol '~' represent small-signal perturbation and variables in capital letter represent the steady-state value.

By applying these perturbations into the non-linear averaged switch model in (3.139)-(3.142), we get

$$V_{sw} + \tilde{v}_{sw}(t) = \left(D' - \tilde{d}(t)\right)\left[V_g + \tilde{v}_g(t) + V_F + r_d\left(I_L + \tilde{i}_L(t)\right)\right] \tag{3.144}$$

$$I_{sw} + \tilde{i}_{sw}(t) = \left(D + \tilde{d}(t)\right)\left(I_L + \tilde{i}_L(t)\right) \tag{3.145}$$

$$V_D + \tilde{v}_D(t) = \left(D + \tilde{d}(t)\right)\left[V_g + \tilde{v}_g(t) - r_{sw}\left(I_L + \tilde{i}_L(t)\right)\right] \tag{3.146}$$

$$I_D + \tilde{i}_D(t) = \left(D' - \tilde{d}(t)\right)\left(I_L + \tilde{i}_L(t)\right) \tag{3.147}$$

Equations (3.144)-(3.147) are further simplified by neglecting the products of perturbation terms, which results in following set of linear equations,

$$V_{sw}+\tilde{v}_{sw}(t)=D'\left(V_g+V_F+r_dI_L\right)+D'\left(\tilde{v}_g(t)+r_d\tilde{i}_L(t)\right)-\tilde{d}(t)\left(V_g+V_F+r_dI_L\right) \tag{3.148}$$

$$I_{sw}+\tilde{i}_{sw}(t)=DI_L+D\tilde{i}_L(t)+\tilde{d}(t)I_L \tag{3.149}$$

$$V_D+\tilde{v}_D(t)=D\left(V_g-r_{sw}I_L\right)+D\left(\tilde{v}_g(t)-r_{sw}\tilde{i}_L(t)\right)+\tilde{d}(t)\left(V_g-r_{sw}I_L\right) \tag{3.150}$$

$$I_D+\tilde{i}_D(t)=D'I_L+D'\tilde{i}_L(t)-\tilde{d}(t)I_L \tag{3.151}$$

Equations (3.148)-(3.151) provide the large-signal linear averaged switch model of the non-ideal buck converter, which can further be used to study the steady-state and dynamic behaviour. The equations (3.148)-(3.151) can be realized using combinations of controlled voltage and/or current sources. The switch and diode in original circuit (Fig. 3.3) are replaced by these controlled voltage and/or current sources. The pair of controlled voltage source and current source should be selected *i.e.*, if the switch is replaced by controlled voltage source then the diode should be replaced by controlled current source and if the switch is replaced by controlled current source then the diode should be replaced by the controlled voltage source [66]. The first case is discussed in detail here. It gives the steady-state and small-signal model same as obtained from SSA technique.

The large-signal linear averaged switch model of complete non-ideal buck converter is shown in Fig. 3.5. This model is obtained by inserting the averaged model of the switch and diode into the original circuit model. The switch is replaced by voltage sources and the diode is replaced by controlled current sources.

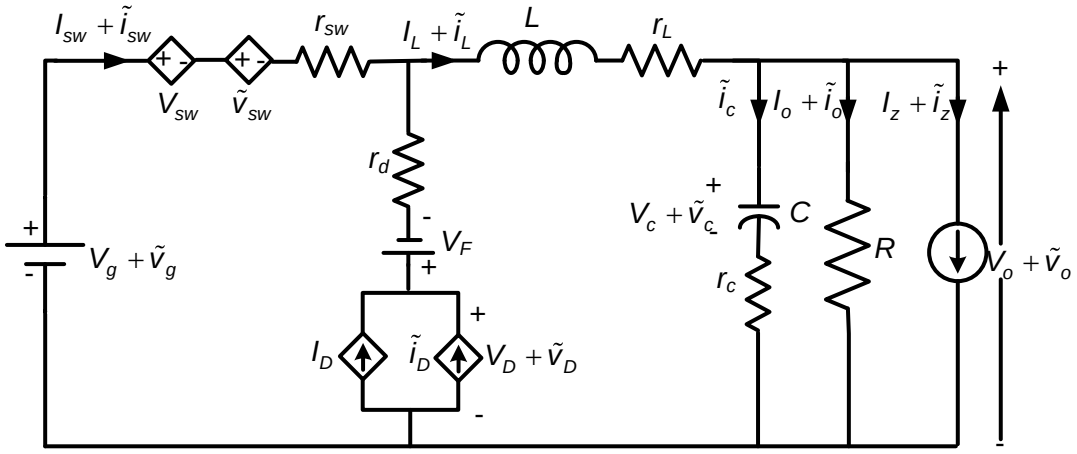


Fig. 3.5. Linearized large-signal averaged switch model of non-ideal buck converter

The expressions for controlled voltage and current sources can be obtained from (3.148) and (3.151) as follows:

$$V_{sw}=D'\left(V_g+V_F+r_dI_L\right) \tag{3.152}$$

$$\tilde{v}_{sw}=D'\left(\tilde{v}_g+r_d\tilde{i}_L\right)-\tilde{d}\left(V_g+V_F+r_dI_L\right) \tag{3.153}$$

$$I_D = D' I_L \tag{3.154}$$

$$\tilde{i}_D = D' \tilde{i}_L - \tilde{d} I_L \tag{3.155}$$

It is to be clearly noted that each of these controlled voltage and current sources are dependent on more than one variable. These variables are current, voltage and duty cycle. For example, voltage source $\tilde{v}_{sw}$ is dependent on input voltage $\tilde{v}_g$, inductor current $\tilde{i}_L$ and duty cycle $\tilde{d}$. Although for clarity purpose, the controlled sources have been shown as a single source in figures.

Step 3: Obtaining steady-state (dc) and small-signal (ac) model

To study the steady-state (dc) behaviour and dynamic (ac) behaviour of non-ideal buck converter operating in CCM, the circuit in Fig. 3.5 is segregated into two parts. Consequently, the steady-state (dc) circuit model and linear small-signal (ac) circuit model of non-ideal buck converter are obtained as shown in Fig. 3.6 and Fig. 3.7, respectively.

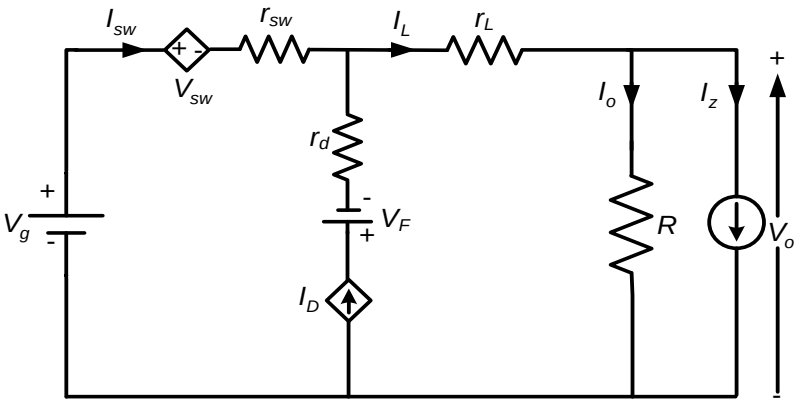


Fig. 3.6. Steady-state model of non-ideal DC-DC buck converter

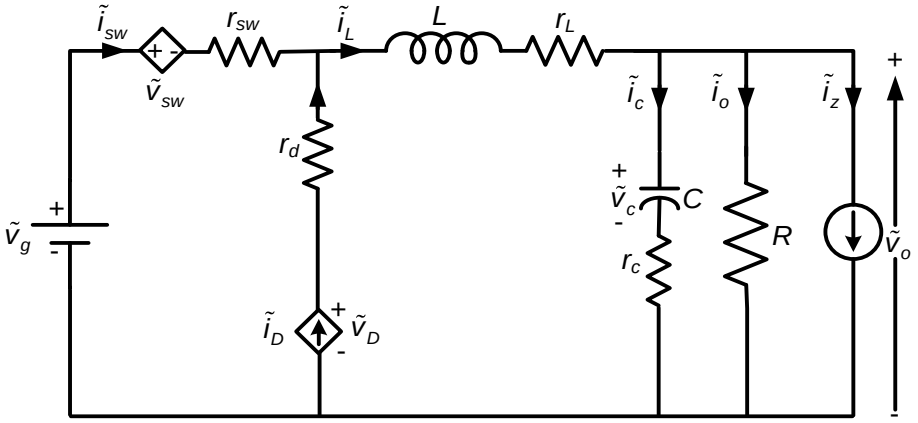


Fig. 3.7. Linearized small-signal model of non-ideal DC-DC buck converter

Steady-state (dc) model:

In circuit of Fig. 3.6, applying Kirchhoff's voltage law (KVL), we have

$$V_g - V_{sw} - r_{sw} I_{sw} - r_L I_L - V_o = 0 \tag{3.156}$$

Applying Kirchhoff's current law (KCL),

$$I_{sw} = I_L - I_D = DI_L \tag{3.157}$$

$$I_L = \left(\frac{V_o}{R} + I_z\right) \tag{3.158}$$

Substituting values from (3.152) and (3.157) into (3.156),

$$\begin{aligned} &V_g - D'\left(V_g + V_F + r_d I_L\right) - r_{sw}\left(DI_L\right) - r_L I_L - V_o = 0 \\ &\Rightarrow DV_g - D'V_F - \left(Dr_{sw} + D'r_d + r_L\right)I_L - V_o = 0 \end{aligned} \tag{3.159}$$

Substituting value of I_L from (3.158) in the above equation and simplifying for V_o gives

$$V_o = \frac{DV_g - D'V_F - \left(r_L + Dr_{sw} + D'r_d\right)I_z}{1 + \frac{1}{R}\left(r_L + Dr_{sw} + D'r_d\right)} \tag{3.160}$$

Small-signal (ac) model:

In the circuit of Fig. 3.7, applying Kirchhoff's voltage law (KVL), we have

$$\tilde{v}_g - \tilde{v}_{sw} - r_{sw}\tilde{i}_{sw} - \left(r_L + Z_L\right)\tilde{i}_L - \tilde{v}_o = 0 \tag{3.161}$$

Where, $Z_L = sL$ is the impedance of the inductor.

Applying Kirchhoff's current law (KCL),

$$\tilde{i}_{sw} = \tilde{i}_L - \tilde{i}_D \tag{3.162}$$

$$\tilde{i}_L = \tilde{i}_c + \tilde{i}_o + \tilde{i}_z \tag{3.163}$$

Replacing value from (3.155) into (3.162), we get

$$\tilde{i}_{sw} = D\tilde{i}_L + \tilde{d}I_L \tag{3.164}$$

Substituting values from (3.153) and (3.164) into (3.161), we get

$$\begin{aligned} &\tilde{v}_g - D'\left(\tilde{v}_g + r_d\tilde{i}_L\right) + \tilde{d}\left(V_g + V_F + r_d I_L\right) - r_{sw}\left(D\tilde{i}_L + \tilde{d}I_L\right) - \left(r_L + Z_L\right)\tilde{i}_L - \tilde{v}_o = 0 \\ &\Rightarrow D\tilde{v}_g + \left(V_g + V_F + \left(r_d - r_{sw}\right)I_L\right)\tilde{d} - \left(Dr_{sw} + D'r_d + r_L + Z_L\right)\tilde{i}_L - \tilde{v}_o = 0 \end{aligned} \tag{3.165}$$

The load current is $\tilde{i}_o = \frac{\tilde{v}_o}{R}$ and capacitor current is $\tilde{i}_c = \frac{\tilde{v}_o}{r_c + Z_c}$. Where, $Z_c = \frac{1}{sC}$

Inserting these values in (3.163),

$$\tilde{i}_L = \frac{\tilde{v}_o}{r_c + Z_c} + \frac{\tilde{v}_o}{R} + \tilde{i}_z \Rightarrow \tilde{i}_L = Y_o\tilde{v}_o + \tilde{i}_z \tag{3.166}$$

Where, $$Y_o = \frac{1}{r_c + Z_c} + \frac{1}{R} = \frac{1 + sC\left(R + r_c\right)}{R\left(1 + sr_cC\right)}$$

Upon simplification of (3.165) by inserting values from (3.166), we get

$$D\tilde{v}_g + \left(V_g + V_F + \left(r_d - r_{sw}\right)I_L\right)\tilde{d} - \left(Dr_{sw} + D'r_d + r_L + Z_L\right)\left(Y_o\tilde{v}_o + \tilde{i}_z\right) - \tilde{v}_o = 0$$

$$\Rightarrow \left(1 + \left(Dr_{sw} + D'r_d + r_L + Z_L\right)Y_o\right)\tilde{v}_o = D\tilde{v}_g + \left(V_g + V_F + \left(r_d - r_{sw}\right)I_L\right)\tilde{d} - \left(Dr_{sw} + D'r_d + r_L + Z_L\right)\tilde{i}_z \tag{3.167}$$

This is the simplified small-signal model of non-ideal buck converter, which is used to get different transfer functions in the following steps.

Step 4: Derivation of different transfer functions

In this section, the important transfer functions of non-ideal buck converter are derived from its simplified small-signal model.

(i) Input voltage to output voltage transfer function:

The input voltage to output voltage transfer function can be found by substituting the perturbation in duty signal ($\tilde{d}$) and perturbation in load current ($\tilde{i}_z$) to be zero.

Substituting $\tilde{d}=0$ and $\tilde{i}_z=0$ in (3.167) gives,

$$\left(1+\left(Dr_{sw}+D'r_d+r_L+Z_L\right)Y_o\right)\tilde{v}_o=D\tilde{v}_g \tag{3.168}$$

The term $\left(1+\left(Dr_{sw}+D'r_d+r_L+Z_L\right)Y_o\right)$ can be simplified by substituting respective values as follows:

$$\begin{aligned}
&\left(1+\left(Dr_{sw}+D'r_d+r_L+Z_L\right)Y_o\right)\\
&\quad=1+\left(Dr_{sw}+D'r_d+r_L+sL\right)\frac{1+sC\left(R+r_c\right)}{R\left(1+sr_cC\right)}\\
&\quad=\frac{R\left(1+sr_cC\right)+\left(Dr_{sw}+D'r_d+r_L\right)+s\left(L+C\left(R+r_c\right)\left(Dr_{sw}+D'r_d+r_L\right)\right)+s^2LC\left(R+r_c\right)}{R\left(1+sr_cC\right)}\\
&\quad=\frac{s^2LC\left(R+r_c\right)+s\left(L+C\left(R+r_c\right)\left(Dr_{sw}+D'r_d+r_L\right)+r_cRC\right)+\left(R+Dr_{sw}+D'r_d+r_L\right)}{R\left(1+sr_cC\right)}\\
&\quad=\frac{LC\left(R+r_c\right)}{R\left(1+sr_cC\right)}\left[s^2+s\left\{\frac{\left(Dr_{sw}+D'r_d+r_L\right)}{L}+\frac{r_cR}{L\left(R+r_c\right)}+\frac{1}{C\left(R+r_c\right)}\right\}+\frac{\left(R+Dr_{sw}+D'r_d+r_L\right)}{LC\left(R+r_c\right)}\right]
\end{aligned} \tag{3.169}$$

Substituting this value into (3.168) , the input voltage to output voltage transfer function is

$$\frac{\tilde{v}_o\left(s\right)}{\tilde{v}_g\left(s\right)}=\frac{\frac{DR}{LC\left(R+r_c\right)}\left(1+sr_cC\right)}{s^2+s\left\{\frac{\left(Dr_{sw}+D'r_d+r_L\right)}{L}+\frac{r_cR}{L\left(R+r_c\right)}+\frac{1}{C\left(R+r_c\right)}\right\}+\frac{\left(R+Dr_{sw}+D'r_d+r_L\right)}{LC\left(R+r_c\right)}} \tag{3.170}$$

(ii) Load current to output voltage transfer function:

The load current to output voltage transfer function (output impedance) can be found by substituting the perturbation of duty signal ($\tilde{d}$) and perturbation of input voltage ($\tilde{v}_g$) to zero.

Substituting $\tilde{d}=0$ and $\tilde{v}_g=0$ in (3.167) gives,

$$\left(1+\left(Dr_{sw}+D'r_d+r_L+Z_L\right)Y_o\right)\tilde{v}_o=-\left(Dr_{sw}+D'r_d+r_L+Z_L\right)\tilde{i}_z \tag{3.171}$$

Substituting the term $\left(1+\left(Dr_{sw}+D'r_d+r_L+Z_L\right)Y_o\right)$ from (3.169), the load current to output voltage transfer function is obtained as:

$$\frac{\tilde{v}_o(s)}{\tilde{i}_z(s)} = \frac{-\dfrac{R}{LC(R+r_c)}(1+sr_cC)(Dr_{sw}+D'r_d+r_L+sL)}{s^2+s\left\{\dfrac{(Dr_{sw}+D'r_d+r_L)}{L}+\dfrac{r_cR}{L(R+r_c)}+\dfrac{1}{C(R+r_c)}\right\}+\dfrac{(R+Dr_{sw}+D'r_d+r_L)}{LC(R+r_c)}} \quad (3.172)$$

(iii) Duty cycle to output voltage transfer function:

The duty cycle to output voltage transfer function can be found by substituting the perturbation in input voltage ($\tilde{v}_g$) and perturbation in load current ($\tilde{i}_z$) to be zero.

Substituting $\tilde{v}_g = 0$ and $\tilde{i}_z = 0$ in (3.167) gives,

$$\left(1+\left(Dr_{sw}+D'r_d+r_L+Z_L\right)Y_o\right)\tilde{v}_o = \left(V_g+V_F+\left(r_d-r_{sw}\right)I_L\right)\tilde{d} \quad (3.173)$$

Substituting the term $\left(1+\left(Dr_{sw}+D'r_d+r_L+Z_L\right)Y_o\right)$ from (3.169), the duty cycle to the output voltage transfer function is obtained as:

$$\frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{\dfrac{R\left(V_g+V_F+\left(r_d-r_{sw}\right)I_L\right)}{LC(R+r_c)}(1+sr_cC)}{s^2+s\left\{\dfrac{(Dr_{sw}+D'r_d+r_L)}{L}+\dfrac{r_cR}{L(R+r_c)}+\dfrac{1}{C(R+r_c)}\right\}+\dfrac{(R+Dr_{sw}+D'r_d+r_L)}{LC(R+r_c)}} \quad (3.174)$$

In following section, this technique is used for modeling of non-ideal DC-DC Cuk converter.

3.3.2 Modeling of non-ideal DC-DC Cuk converter

The circuit configuration of non-ideal Cuk converter is given in Fig. 3.8. The inductors, capacitors, switch, and diode have been shown with their non-ideal representation. The instantaneous voltage across the ideal switch and the ideal diode are denoted by v_{sw} and v_D, respectively, whereas the instantaneous current through the switch and the diode are denoted by i_{sw} and i_D, respectively. The converter is considered to be operating in continuous conduction mode (CCM). In CCM operation, it has two circuit states (a) when MOSFET switch is on and diode is off (b) when MOSFET switch is off and diode is on. The step-wise procedure to obtain the steady-state and small-signal model of Cuk converter using averaged-switch model technique is given as follows:

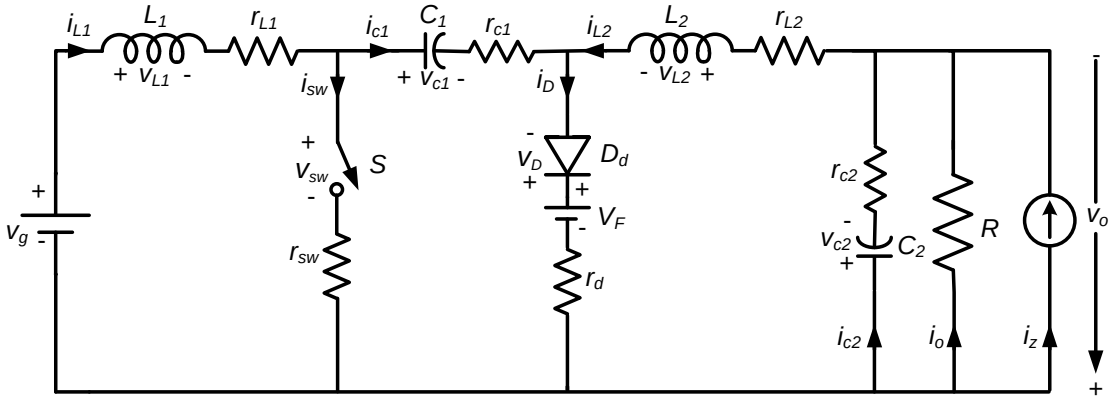


Fig. 3.8. Circuit diagram of non-ideal DC-DC Cuk converter

Step 1: Obtain the averaged model of switch and diode

The equivalent circuit diagram of the Cuk converter during switch-on period ($0<t\leq DT$) and switch-off period ($DT<t\leq T$) are given in Fig. 3.9. From these figures, the voltage and current relationships for switch S and diode D_d can easily be obtained.

The instantaneous switch voltage (v_{sw}) and switch current (i_{sw}) are given as

$$v_{sw}(t)=\begin{cases}0 & \text{for } 0<t\leq dT\\ v_{c1}(t)+V_F+r_{c1}i_{L1}(t)+r_d\left(i_{L1}(t)+i_{L2}(t)\right) & \text{for } dT<t\leq T\end{cases} \tag{3.175}$$

$$i_{sw}(t)=\begin{cases}i_{L1}(t)+i_{L2}(t) & \text{for } 0<t\leq dT\\ 0 & \text{for } dT<t\leq T\end{cases} \tag{3.176}$$

The instantaneous diode voltage (v_D) and diode current (i_D) are given as

$$v_D(t)=\begin{cases}v_{c1}(t)-r_{c1}i_{L2}(t)-r_{sw}\left(i_{L1}(t)+i_{L2}(t)\right) & \text{for } 0<t\leq dT\\ 0 & \text{for } dT<t\leq T\end{cases} \tag{3.177}$$

$$i_D(t)=\begin{cases}0 & \text{for } 0<t\leq dT\\ i_{L1}(t)+i_{L2}(t) & \text{for } dT<t\leq T\end{cases} \tag{3.178}$$

These instantaneous current and voltage relationships are time averaged over one switching cycle to obtain the averaged PWM switch model.

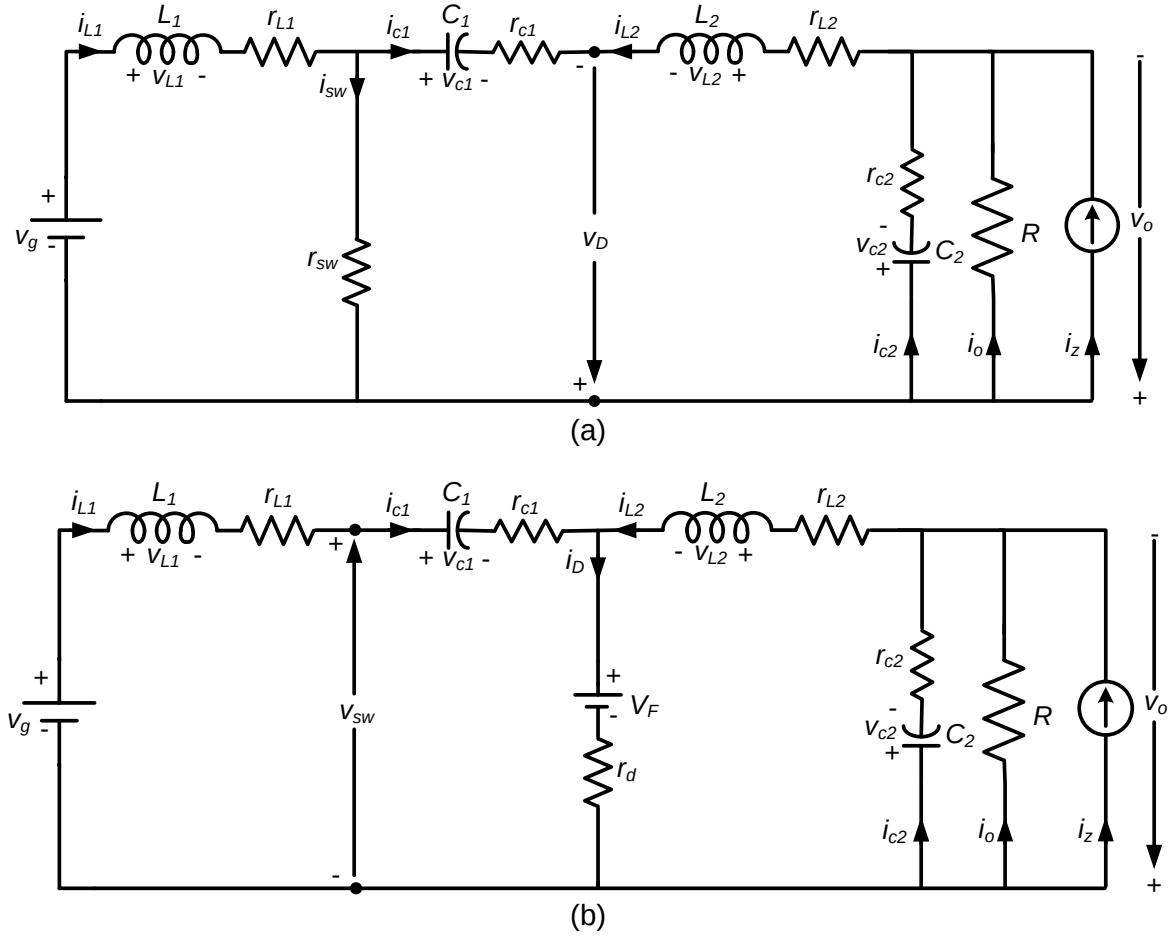


Fig. 3.9. Equivalent circuit diagram of non-ideal Cuk converter during (a) switch-on (b) switch-off

The averaged switch voltage and current are obtained as

$$\bar{v}_{sw}(t) = d'(t)\left[\bar{v}_{c1}(t) + V_F + r_{c1}\bar{i}_{L1}(t) + r_d\left(\bar{i}_{L1}(t) + \bar{i}_{L2}(t)\right)\right] \tag{3.179}$$

$$\bar{i}_{sw}(t) = d(t)\left(\bar{i}_{L1}(t) + \bar{i}_{L2}(t)\right) \tag{3.180}$$

The averaged diode voltage and current are obtained as

$$\bar{v}_D(t) = d(t)\left[\bar{v}_{c1}(t) - r_{c1}\bar{i}_{L2}(t) - r_{sw}\left(\bar{i}_{L1}(t) + \bar{i}_{L2}(t)\right)\right] \tag{3.181}$$

$$\bar{i}_D(t) = d'(t)\left(\bar{i}_{L1}(t) + \bar{i}_{L2}(t)\right) \tag{3.182}$$

Equations (3.179)-(3.182) represent the large-signal non-linear averaged switch model of Cuk converter. These averaged equations of the switch and diode are non-linear because they are product of the two time-varying terms.

Step 2: Linearization of the averaged switch model by introducing small perturbations

The linearized switch model of Cuk converter can be obtained by introducing the small-signal (ac) perturbations around an equilibrium (steady-state) point. The small-signal perturbations for Cuk converter are defined as:

$$\begin{aligned}
&\bar{v}_{sw}(t) = V_{sw} + \tilde{v}_{sw}(t), \bar{i}_{sw}(t) = I_{sw} + \tilde{i}_{sw}(t), \bar{v}_D(t) = V_D + \tilde{v}_D(t), \bar{i}_D(t) = I_D + \tilde{i}_D(t),\\
&\bar{v}_g(t) = V_g + \tilde{v}_g(t), \bar{v}_o(t) = V_o + \tilde{v}_o(t), d(t) = D + \tilde{d}(t), d'(t) = D' - \tilde{d}(t),\\
&\bar{i}_o(t) = I_o + \tilde{i}_o(t), \bar{i}_z = I_z + \tilde{i}_z(t), \bar{i}_{L1}(t) = I_{L1} + \tilde{i}_{L1}(t), \bar{i}_{L2}(t) = I_{L2} + \tilde{i}_{L2}(t),\\
&\bar{v}_{c1}(t) = V_{c1} + \tilde{v}_{c1}(t), \bar{v}_{c2}(t) = V_{c2} + \tilde{v}_{c2}(t)
\end{aligned} \tag{3.183}$$

The variables having symbol '~' represent small-signal perturbation and variables in capital letter represent the steady-state value.

The small-signal perturbations are time varying quantities. Here onwards, the time *'t'* in bracket with small-signal perturbation is dropped for the sake of simplicity of equations.

Applying these perturbations in (3.179)-(3.182),

$$V_{sw} + \tilde{v}_{sw} = \left(D' - \tilde{d}\right)\left[V_{c1} + \tilde{v}_{c1} + V_F + r_{c1}\left(I_{L1} + \tilde{i}_{L1}\right) + r_d\left(I_{L1} + \tilde{i}_{L1} + I_{L2} + \tilde{i}_{L2}\right)\right] \tag{3.184}$$

$$I_{sw} + \tilde{i}_{sw} = \left(D + \tilde{d}\right)\left(I_{L1} + \tilde{i}_{L1} + I_{L2} + \tilde{i}_{L2}\right) \tag{3.185}$$

$$V_D + \tilde{v}_D = \left(D + \tilde{d}\right)\left[V_{c1} + \tilde{v}_{c1} - r_{c1}\left(I_{L2} + \tilde{i}_{L2}\right) - r_{sw}\left(I_{L1} + \tilde{i}_{L1} + I_{L2} + \tilde{i}_{L2}\right)\right] \tag{3.186}$$

$$I_D + \tilde{i}_d = \left(D' - \tilde{d}\right)\left(I_{L1} + \tilde{i}_{L1} + I_{L2} + \tilde{i}_{L2}\right) \tag{3.187}$$

The second-order (the product of perturbations) terms can be neglected to get the linear model. Therefore, equations (3.184)-(3.187) become

$$\begin{aligned}
V_{sw} + \tilde{v}_{sw} \;= {} & D'\left[V_{c1} + V_F + r_{c1}I_{L1} + r_d\left(I_{L1} + I_{L2}\right)\right] + D'\left[\tilde{v}_{c1} + r_{c1}\tilde{i}_{L1} + r_d\left(\tilde{i}_{L1} + \tilde{i}_{L2}\right)\right]\\
& - \tilde{d}\left[V_{c1} + V_F + r_{c1}I_{L1} + r_d\left(I_{L1} + I_{L2}\right)\right]
\end{aligned} \tag{3.188}$$

$$I_{sw} + \tilde{i}_{sw} = D\left(I_{L1} + I_{L2}\right) + D\left(\tilde{i}_{L1} + \tilde{i}_{L2}\right) + \tilde{d}\left(I_{L1} + I_{L2}\right) \tag{3.189}$$

$$V_D + \tilde{v}_D = D\left[V_{c1} - r_{c1}I_{L2} - r_{sw}\left(I_{L1} + I_{L2}\right)\right] + D\left[\tilde{v}_{c1} - r_{c1}\tilde{i}_{L2} - r_{sw}\left(\tilde{i}_{L1} + \tilde{i}_{L2}\right)\right] + \tilde{d}\left[V_{c1} - r_{c1}I_{L2} - r_{sw}\left(I_{L1} + I_{L2}\right)\right] \quad (3.190)$$

$$I_D + \tilde{i}_d = D'\left(I_{L1} + I_{L2}\right) + D'\left(\tilde{i}_{L1} + \tilde{i}_{L2}\right) - \tilde{d}\left(I_{L1} + I_{L2}\right) \quad (3.191)$$

Equations (3.188)-(3.191) provide the large-signal linear averaged switch model, which is further used to study the steady-state and dynamic behaviour of the non-ideal Cuk converter operating in CCM. These equations can be realized using combinations of controlled voltage and/or current sources. The switch and diode in original circuit (Fig. 3.8) are replaced by these controlled voltage and/or current sources. The pair of controlled voltage source and current source should be selected [66]. Therefore, two cases are possible: (i) the switch is replaced by controlled voltage source and the diode is replaced by controlled current source and (ii) the switch is replaced by the controlled current source and the diode is replaced by the controlled voltage source.

Case 1: In this case, the switch is replaced by controlled voltage source and the diode is replaced by controlled current source. The respective equivalent circuit is shown as in Fig. 3.10 (a). The expressions for the controlled voltage and current sources can be obtained from (3.188) and (3.191) as follows:

$$V_{sw} = D'\left[V_{c1} + V_F + r_{c1}I_{L1} + r_d\left(I_{L1} + I_{L2}\right)\right] \quad (3.192)$$

$$\tilde{v}_{sw} = D'\left[\tilde{v}_{c1} + r_{c1}\tilde{i}_{L1} + r_d\left(\tilde{i}_{L1} + \tilde{i}_{L2}\right)\right] - \left[V_{c1} + V_F + r_{c1}I_{L1} + r_d\left(I_{L1} + I_{L2}\right)\right]\tilde{d} \quad (3.193)$$

$$I_D = D'\left(I_{L1} + I_{L2}\right) \quad (3.194)$$

$$\tilde{i}_D = D'\left(\tilde{i}_{L1} + \tilde{i}_{L2}\right) - \left(I_{L1} + I_{L2}\right)\tilde{d} \quad (3.195)$$

Case 2: In this case, the switch is replaced by the controlled current source and the diode is replaced by the controlled voltage source. The respective equivalent circuit is shown as in Fig. 3.10 (b). The expressions for the controlled current and voltage sources can be obtained from (3.189) and (3.190) as follows:

$$I_{sw} = D\left(I_{L1} + I_{L2}\right) \quad (3.196)$$

$$\tilde{i}_{sw} = D\left(\tilde{i}_{L1} + \tilde{i}_{L2}\right) + \left(I_{L1} + I_{L2}\right)\tilde{d} \quad (3.197)$$

$$V_D = D\left[V_{c1} - r_{c1}I_{L2} + r_{sw}\left(I_{L1} + I_{L2}\right)\right] \quad (3.198)$$

$$\tilde{v}_D = D\left[\tilde{v}_{c1} - r_{c1}\tilde{i}_{L2} - r_{sw}\left(\tilde{i}_{L1} + \tilde{i}_{L2}\right)\right] + \left[V_{c1} - r_{c1}I_{L2} - r_{sw}\left(I_{L1} + I_{L2}\right)\right]\tilde{d} \quad (3.199)$$

It is to be clearly noted that each controlled voltage and current source realized using (3.192) -(3.199) are dependent on more than one variable. These sources are a combination of current, voltage and duty cycle variables. Although to have clarity in figures, they have been shown as a single source. In the both cases, the steady-state and dynamic analysis follow the same steps and results in same expressions. Therefore, only one case (first case) is discussed here. It gives the steady-state and small-signal models identical to SSA technique.

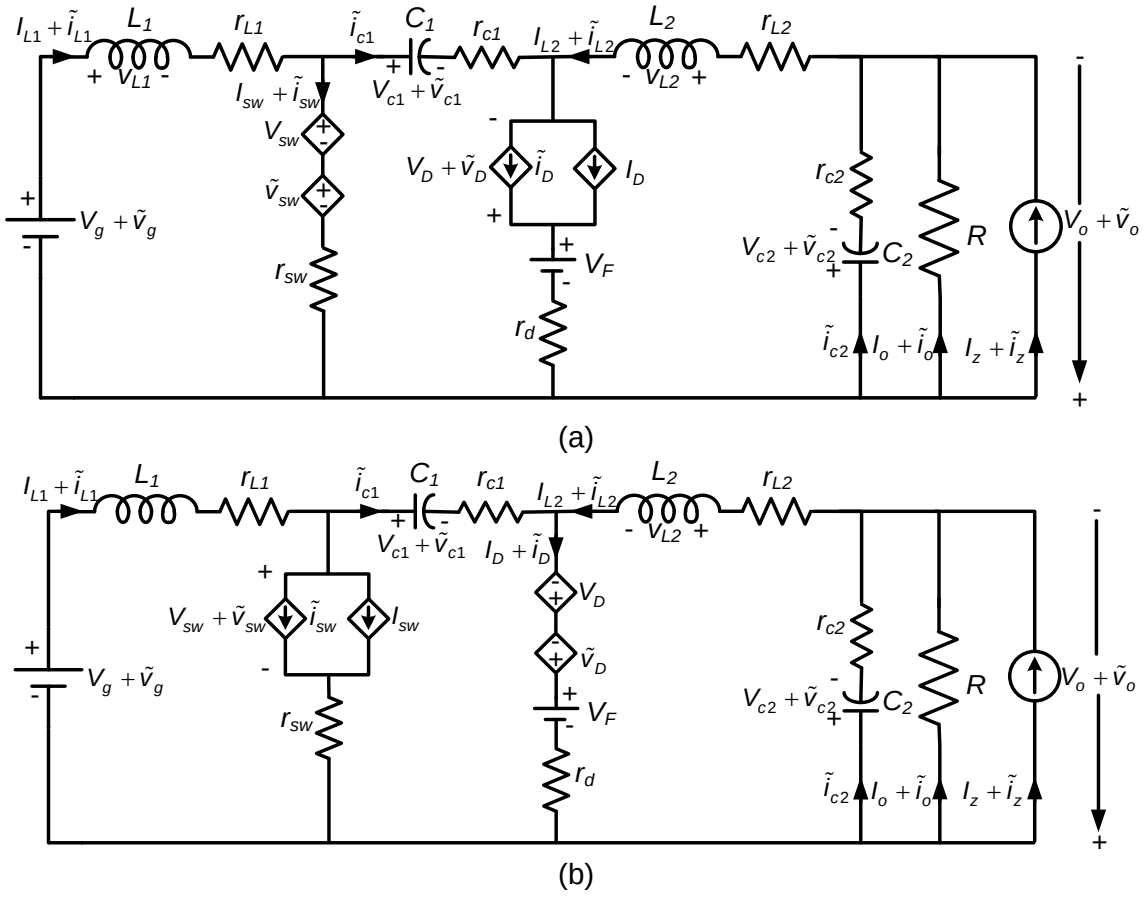


Fig. 3.10. Linearized large-signal averaged switch model of non-ideal Cuk converter
(a) Case 1 (b) Case 2

Step 3: Obtaining steady-state (dc) and small-signal (ac) model

To obtain the steady-state (dc) and small-signal (ac) model of non-ideal Cuk converter, the large-signal model in Fig. 3.10 is segregated into two parts. Consequently, the steady-state (dc) circuit model and linear small-signal (ac) circuit model of non-ideal Cuk converter are obtained as shown in Fig. 3.11 and Fig. 3.12, respectively.

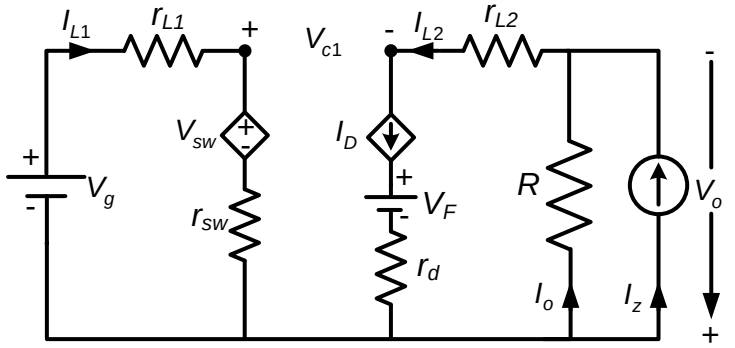


Fig. 3.11. Steady-state model of non-ideal DC-DC Cuk converter

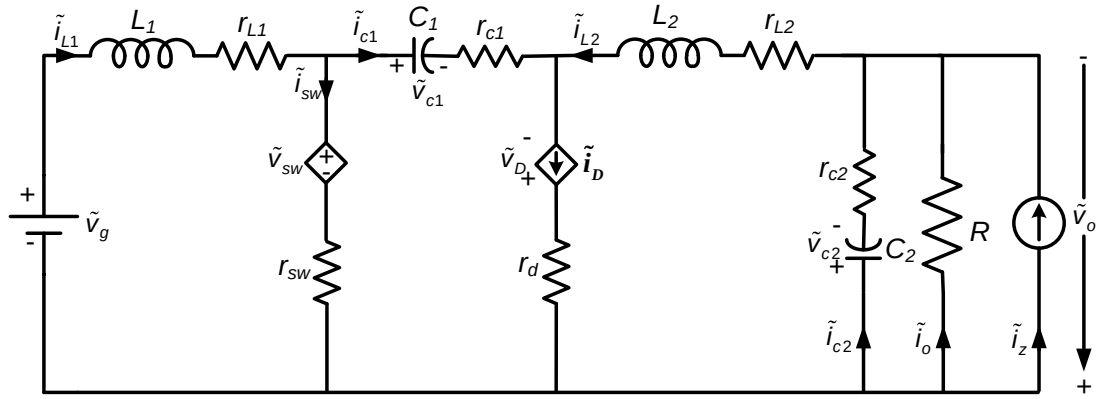


Fig. 3.12. Linearized small-signal model of non-ideal DC-DC Cuk converter

Steady-state (dc) model:

Applying Kirchhoff's voltage law (KVL) in the circuit of Fig. 3.11, we have

$$V_g - (r_{L1} + r_{sw}) I_{L1} - V_{sw} = 0 \tag{3.200}$$

$$V_g - r_{L1} I_{L1} - V_{c1} + r_{L2} I_{L2} + V_o = 0 \tag{3.201}$$

Applying Kirchhoff's current law (KCL) in Fig. 3.11,

$$I_D = I_{L2} \tag{3.202}$$

$$I_{L2} = \left(\frac{V_o}{R} + I_z \right) \tag{3.203}$$

Equating (3.194) and (3.202), we get

$$I_{L1} = \frac{D}{D'} I_{L2} \tag{3.204}$$

Substituting values of I_{L2} and I_{L1} from (3.203)-(3.204) into (3.201), we get

$$V_{c1} = V_g + \left(1 + \frac{1}{R} \left(r_{L2} - \frac{D}{D'} r_{L1} \right) \right) V_o + \left(r_{L2} - \frac{D}{D'} r_{L1} \right) I_z \tag{3.205}$$

Replacing the values of I_{L1} and V_{c1} into (3.192), the simplified expression for V_{sw} becomes

$$V_{sw} = D' V_g + D' V_o + D' V_F + \left(-D r_{L1} + D' r_{L2} + D r_{c1} + r_d \right) I_{L2} \tag{3.206}$$

Substitution of the respective values from (3.203),(3.204) and (3.206) into (3.200) and upon simplification, we get

$$V_o = V_{c2} = \frac{\frac{D}{D'} V_g - V_F - I_z \left(\frac{D^2 r_{L1} + D'^2 r_{L2} + D D' r_{c1} + r_x}{D'^2} \right)}{1 + \frac{1}{R} \left(\frac{D^2 r_{L1} + D'^2 r_{L2} + D D' r_{c1} + r_x}{D'^2} \right)} \tag{3.207}$$

Small-signal (ac) model:

Applying Kirchhoff's voltage law (KVL) in Fig. 3.12, we have

$$\tilde{v}_g - (r_{L1} + Z_{L1} + r_{sw}) \tilde{i}_{L1} + r_{sw} \tilde{i}_{c1} - \tilde{v}_{sw} = 0 \tag{3.208}$$

$$\tilde{v}_{sw} + r_{sw} \left(\tilde{i}_{L1} - \tilde{i}_{c1} \right) - \left(\tilde{v}_{c1} + r_{c1} \tilde{i}_{c1} \right) + (r_{L2} + Z_{L2}) \tilde{i}_{L2} + \tilde{v}_o = 0 \tag{3.209}$$

Where, $Z_{L1} = sL_1$ and $Z_{L1} = sL_2$ are impedances of inductors.

Applying Kirchhoff's current law (KCL) in Fig. 3.12, we get

$$\tilde{i}_D = \tilde{i}_{L2} + \tilde{i}_{c1} \tag{3.210}$$

$$\tilde{i}_{L2} = \tilde{i}_{c2} + \tilde{i}_o + \tilde{i}_z \tag{3.211}$$

Substituting $\tilde{i}_{c1} = Y_{c1}\tilde{v}_{c1}, \text{where} Y_{c1} = \frac{1}{sC_1}$ and $\tilde{v}_{sw}$ from (3.193) into (3.208)-(3.209) gives

$$\begin{aligned}
&\tilde{v}_g - \left(r_{L1} + Z_{L1} + r_{sw}\right)\tilde{i}_{L1} + r_{sw}Y_{c1}\tilde{v}_{c1} - D'\left[\tilde{v}_{c1} + r_{c1}\tilde{i}_{L1} + r_d\left(\tilde{i}_{L1} + \tilde{i}_{L2}\right)\right] + \left[V_{c1} + V_F + r_{c1}I_{L1} + r_d\left(I_{L1} + I_{L2}\right)\right]\tilde{d} = 0 \\
&\Rightarrow -\left(r_{L1} + Z_{L1} + D'r_{c1} + r_{sw} + D'r_d\right)\tilde{i}_{L1} - D'r_d\tilde{i}_{L2} - \left(D' - r_{sw}Y_{c1}\right)\tilde{v}_{c1} + \tilde{v}_g + \left[V_{c1} + V_F + r_{c1}I_{L1} + r_d\left(I_{L1} + I_{L2}\right)\right]\tilde{d} = 0
\end{aligned} \tag{3.212}$$

$$\begin{aligned}
&D'\left[\tilde{v}_{c1} + r_{c1}\tilde{i}_{L1} + r_d\left(\tilde{i}_{L1} + \tilde{i}_{L2}\right)\right] - \tilde{d}\left[V_{c1} + V_F + r_{c1}I_{L1} + r_d\left(I_{L1} + I_{L2}\right)\right] + \\
&\qquad r_{sw}\left(\tilde{i}_{L1} - Y_{c1}\tilde{v}_{c1}\right) - \left(\tilde{v}_{c1} + r_{c1}Y_{c1}\tilde{v}_{c1}\right) + \left(r_{L2} + Z_{L2}\right)\tilde{i}_{L2} + \tilde{v}_o = 0 \\
&\Rightarrow \left(D'r_{c1} + r_{sw} + D'r_d\right)\tilde{i}_{L1} + \left(r_{L2} + Z_{L2} + D'r_d\right)\tilde{i}_{L2} - \left(D + \left(r_{c1} + r_{sw}\right)Y_{c1}\right)\tilde{v}_{c1} \\
&\qquad -\left[V_{c1} + V_F + r_{c1}I_{L1} + r_d\left(I_{L1} + I_{L2}\right)\right]\tilde{d} + \tilde{v}_o = 0
\end{aligned} \tag{3.213}$$

Replacing the values from (3.195) into (3.210), we get

$$D'\left(\tilde{i}_{L1} + \tilde{i}_{L2}\right) - \left(I_{L1} + I_{L2}\right)\tilde{d} = \tilde{i}_{L2} + \tilde{i}_{c1} \Rightarrow \tilde{i}_{L1} = \frac{D\tilde{i}_{L2} + Y_{c1}\tilde{v}_{c1} + \left(I_{L1} + I_{L2}\right)\tilde{d}}{D'} \tag{3.214}$$

Similar to (3.166) of buck converter, for Cuk converter also we can write

$$\tilde{i}_{L2} = Y_o\tilde{v}_o + \tilde{i}_z \tag{3.215}$$

Where,

$$Y_o = \frac{1}{R \parallel \left(r_{c2} + \frac{1}{sC_2}\right)} = \frac{1 + sC_2\left(R + r_{c2}\right)}{R\left(1 + sr_{c2}C_2\right)} \tag{3.216}$$

Equations (3.212)-(3.215) are generalized small-signal model of non-ideal DC-DC Cuk converter, which can be used to derive the different transfer functions of Cuk converter in the next section.

Step 4: Derivation of different transfer functions

In this section, the important transfer functions of non-ideal Cuk converter are derived from its simplified small-signal model.

(i) Input voltage to output voltage transfer function:

The input voltage to output voltage transfer function can be found by substituting the perturbation in duty signal ($\tilde{d}$) and perturbation in load current ($\tilde{i}_z$) to be zero.

Substituting $\tilde{d} = 0$ and $\tilde{i}_z = 0$ in (3.212)-(3.215) gives

$$-\left(r_{L1} + Z_{L1} + D'r_{c1} + r_{sw} + D'r_d\right)\tilde{i}_{L1} - D'r_d\tilde{i}_{L2} - \left(D' - r_{sw}Y_{c1}\right)\tilde{v}_{c1} + \tilde{v}_g = 0 \tag{3.217}$$

$$\left(D'r_{c1} + r_{sw} + D'r_d\right)\tilde{i}_{L1} + \left(r_{L2} + Z_{L2} + D'r_d\right)\tilde{i}_{L2} - \left(D + \left(r_{c1} + r_{sw}\right)Y_{c1}\right)\tilde{v}_{c1} + \tilde{v}_o = 0 \tag{3.218}$$

$$\tilde{i}_{L1} = \frac{D\tilde{i}_{L2} + Y_{c1}\tilde{v}_{c1}}{D'} \tag{3.219}$$

$$\tilde{i}_{L2} = Y_o \tilde{v}_o \tag{3.220}$$

Substituting values from (3.219)-(3.220) into (3.218), we get

$$\tilde{v}_{c1} = \frac{D' + \left(D' r_{L2} + D' Z_{L2} + DD' r_{c1} + r_x\right) Y_o}{DD' - r_x Y_{c1}} \tilde{v}_o, r_x = D r_{sw} + D' r_d \tag{3.221}$$

Substituting values from (3.219),(3.220) and (3.221) into (3.217), we get

$$\text{den} \cdot \tilde{v}_o = \left(DD' - r_x Y_{c1}\right) \tilde{v}_g \tag{3.222}$$

$$\text{den} = \left(D'^2 + \left(r_{L1} + Z_{L1} + D' r_{c1} + r_x\right) Y_{c1}\right) \cdot \left(1 + \left(r_{L2} + Z_{L2} + D r_{c1} + \frac{r_x}{D'}\right) Y_o\right) + \left(D r_{L1} + D Z_{L1} + DD' r_{c1} + r_x\right) \left(D - \frac{r_x Y_{c1}}{D'}\right) Y_o$$

The coefficient '*den*' can be simplified by inserting the respective values as follows:

$$\text{den} = \left(D'^2 + \left(r_{L1} + sL_1 + D' r_{c1} + r_x\right) sC_1\right) \cdot \left(1 + \left(r_{L2} + sL_2 + D r_{c1} + \frac{r_x}{D'}\right) \frac{1 + sC_2\left(R + r_{c2}\right)}{R\left(1 + s r_{c2} C_2\right)}\right) +$$

$$\left(D r_{L1} + D s L_1 + DD' r_{c1} + r_x\right) \left(D - \frac{r_x}{D'} sC_1\right) \frac{1 + sC_2\left(R + r_{c2}\right)}{R\left(1 + s r_{c2} C_2\right)}$$

$$\Rightarrow \text{den} = \frac{q_4 s^4 + q_3 s^3 + q_2 s^2 + q_1 s + q_0}{R\left(1 + s r_{c2} C_2\right)} \tag{3.223}$$

Where,

$$q_4 = L_1 L_2 C_1 C_2 r_E, q_3 = L_1 L_2 C_1 + L_1 C_1 C_2 \left(r_{c2} R + r_E r_{E2}\right) + L_2 C_1 C_2 r_E r_{E1}, q_0 = D'^2 R + D^2 r_{L1} + D'^2 r_{L2} + DD' r_{c1} + r_x$$

$$q_2 = L_1 C_1 \left(R + r_{E2}\right) + D^2 L_1 C_2 r_E + L_2 C_1 r_{E1} + D'^2 L_2 C_2 r_E + C_1 C_2 \left[r_{c2} R r_{E1} + r_E r_{E1} \left(r_{L2} + D r_{c1}\right) + r_E r_x \left(r_{L1} + D' r_{c1}\right)\right]$$

$$q_1 = D^2 L_1 + D'^2 L_2 + C_1 \left[r_{E1} \left(R + r_{L2} + D r_{c1}\right) + r_x \left(r_{L1} + D' r_{c1}\right)\right] + C_2 \left[D'^2 r_{c2} R + r_E \left(D^2 r_{L1} + D'^2 r_{L2} + DD' r_{c1} + r_x\right)\right]$$

$$r_E = R + r_{c2}, r_{E1} = r_{L1} + D' r_{c1} + r_x, r_{E2} = r_{L2} + D r_{c1} + r_x$$

Substituting this value of '*den*' into (3.222), the input voltage to output voltage transfer function is given as:

$$\frac{\tilde{v}_o(s)}{\tilde{v}_g(s)} = \frac{R\left(ps + 1\right)\left(p_{g1} s + p_{g0}\right)}{q_4 s^4 + q_3 s^3 + q_2 s^2 + q_1 s + q_0} \tag{3.224}$$

Where, $p = r_{c2} C_2, p_{g1} = -r_x C_1, p_{g0} = DD'$

(ii) Load current to output voltage transfer function:

The load current to output voltage transfer function can be found by substituting the perturbation of duty signal ($\tilde{d}$) and perturbation of input voltage ($\tilde{v}_g$) to zero.

Substituting $\tilde{d} = 0$ and $\tilde{v}_g = 0$ in (3.212)-(3.215) gives

$$-\left(r_{L1} + Z_{L1} + D' r_{c1} + r_{sw} + D' r_d\right) \tilde{i}_{L1} - D' r_d \tilde{i}_{L2} - \left(D' - r_{sw} Y_{c1}\right) \tilde{v}_{c1} = 0 \tag{3.225}$$

$$\left(D' r_{c1} + r_{sw} + D' r_d\right) \tilde{i}_{L1} + \left(r_{L2} + Z_{L2} + D' r_d\right) \tilde{i}_{L2} - \left(D + \left(r_{c1} + r_{sw}\right) Y_{c1}\right) \tilde{v}_{c1} + \tilde{v}_o = 0 \tag{3.226}$$

$$\tilde{i}_{L1} = \frac{D \tilde{i}_{L2} + Y_{c1} \tilde{v}_{c1}}{D'} \tag{3.227}$$

$$\tilde{i}_{L2} = Y_o \tilde{v}_o + \tilde{i}_z \tag{3.228}$$

Substituting values from (3.227)-(3.228) into (3.226), we get

$$\tilde{v}_{c1}=\frac{\left(D'+\left(D'r_{L2}+D'Z_{L2}+DD'r_{c1}+r_x\right)Y_o\right)\tilde{v}_o+\left(D'r_{L2}+D'Z_{L2}+DD'r_{c1}+r_x\right)\tilde{i}_z}{DD'-r_xY_{c1}} \quad (3.229)$$

Substituting values from (3.227), (3.228) and (3.229) into (3.225), we get

$$\text{den}\cdot\tilde{v}_o=$$
$$\left[\left(D'^2+\left(r_{L1}+Z_{L1}+D'r_{c1}+r_x\right)Y_{c1}\right)\left(r_{L2}+Z_{L2}+Dr_{c1}+\frac{r_x}{D'}\right)+\left(Dr_{L1}+DZ_{L1}+DD'r_{c1}+r_x\right)\left(D-\frac{r_xY_{c1}}{D'}\right)\right]\left(-\tilde{i}_z\right) \quad (3.230)$$

Substituting the corresponding values in the above equation and simplifying, the load current to the output voltage transfer function is obtained as:

$$\frac{\tilde{v}_o(s)}{\tilde{i}_z(s)}=\frac{-R(ps+1)\left(p_{z3}s^3+p_{z2}s^2+p_{z1}s+p_{z0}\right)}{q_4s^4+q_3s^3+q_2s^2+q_1s+q_0} \quad (3.231)$$

Where,

$$p_{z3}=L_1L_2C_2,\ p_{z2}=L_1C_1r_{E2}+L_2C_1r_{E1},\ p_{z0}=D^2r_{L1}+D'^2r_{L2}+DD'r_{c1}+r_x,$$
$$p_{z1}=D^2L_1+D'^2L_2+C_1\left[r_{E1}\left(r_{L2}+Dr_{c1}\right)+r_x\left(r_{L1}+D'r_{c1}\right)\right],p=r_{c2}C_2$$

The remaining coefficients in (3.231) remain same as in (3.223).

(iii) Duty cycle to output voltage transfer function:

The duty cycle to output voltage transfer function can be found by substituting the perturbation in input voltage ($\tilde{v}_g$) and perturbation in load current ($\tilde{i}_z$) to be zero.

Substituting $\tilde{v}_g=0$ and $\tilde{i}_z=0$ in (3.212)-(3.215) gives

$$-\left(r_{L1}+Z_{L1}+D'r_{c1}+r_{sw}+D'r_d\right)\tilde{i}_{L1}-D'r_d\tilde{i}_{L2}-\left(D'-r_{sw}Y_{c1}\right)\tilde{v}_{c1}+\left[V_{c1}+V_F+r_{c1}I_{L1}+r_d\left(I_{L1}+I_{L2}\right)\right]\tilde{d}=0 \quad (3.232)$$

$$\left(D'r_{c1}+r_{sw}+D'r_d\right)\tilde{i}_{L1}+\left(r_{L2}+Z_{L2}+D'r_d\right)\tilde{i}_{L2}-\left(D+\left(r_{c1}+r_{sw}\right)Y_{c1}\right)\tilde{v}_{c1}$$
$$-\left[V_{c1}+V_F+r_{c1}I_{L1}+r_d\left(I_{L1}+I_{L2}\right)\right]\tilde{d}+\tilde{v}_o=0 \quad (3.233)$$

$$\tilde{i}_{L1}=\frac{D\tilde{i}_{L2}+Y_{c1}\tilde{v}_{c1}+\left(I_{L1}+I_{L2}\right)\tilde{d}}{D'} \quad (3.234)$$

$$\tilde{i}_{L2}=Y_o\tilde{v}_o \quad (3.235)$$

Substituting the values from (3.234)-(3.235) into (3.233), we get

$$\tilde{v}_{c1}=\frac{\left(D'+\left(D'r_{L2}+D'Z_{L2}+DD'r_{c1}+r_x\right)Y_o\right)\tilde{v}_o-\left(D'V_{c1}+D'V_F-D'r_{c1}I_{L2}-r_{sw}\left(I_{L1}+I_{L2}\right)\right)\tilde{d}}{DD'-r_xY_{c1}} \quad (3.236)$$

Substituting values from (3.234),(3.235) and (3.236) into (3.232), we get

$$\text{den}\cdot\tilde{v}_o=\left[\begin{array}{l}\left(D'^2+\left(r_{L1}+Z_{L1}+D'r_{c1}+r_x\right)Y_{c1}\right)\left(V_{c1}+V_F-r_{c1}I_{L2}-\frac{r_{sw}}{D'}\left(I_{L1}+I_{L2}\right)\right)\\ \quad+\left(D'V_{c1}+D'V_F-D'r_{c1}I_{L2}-\left(r_{L1}+Z_{L1}+r_{sw}\right)\left(I_{L1}+I_{L2}\right)\right)\left(D-\frac{r_xY_{c1}}{D'}\right)\end{array}\right]\tilde{d} \quad (3.237)$$

Substituting the corresponding values in above equation and then simplifying, we get the duty cycle to output voltage transfer function as:

$$\frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{R(ps+1)\left(p_{d2}s^2 + p_{d1}s + p_{d0}\right)}{q_4 s^4 + q_3 s^3 + q_2 s^2 + q_1 s + q_0} \tag{3.238}$$

Where,

$$p_{d2} = L_1 C_1 \left[V_{c1} + V_F - I_{L2}\left(r_{c1} + \frac{r_{sw} - r_D}{D'} \right) \right], p_{d0} = D'\left(V_{c1} + V_F\right) - \left(\frac{D}{D'} r_{L1} + D' r_{c1} + \frac{r_{sw}}{D'} \right) I_{L2},$$

$$p_{d1} = \left(r_{L1} + D' r_{c1}\right) C_1 \left(V_{c1} + V_F\right) - L_1 I_{L1} - \left[\left(r_{L1} + D' r_{c1}\right)\left(r_{c1} + \frac{r_{sw}}{D'^2} \right) - \frac{r_{L1} r_x}{D'^2} \right] C_1 I_{L2},$$

The remaining coefficients in (3.238) remain same as in (3.223).

3.4 Comparison of Ideal and Non-ideal DC-DC Buck and Cuk Converter Models

It is observed that the steady-state and transfer function models obtained using state-space averaging method and averaged switch model method are identical for non-ideal buck converter as well for non-ideal Cuk converter. By replacing the non-ideal elements to zero in these models, one can obtain the mathematical model for ideal buck and Cuk converters. In the following sections, the Bode plots and step responses of these converter transfer functions are compared for ideal and non-ideal case.

3.4.1 Buck converter

In order to summarize, the steady-state and transfer function models of non-ideal DC-DC buck converter are rewritten as follows. It is to note that the state-space averaging method and averaged switch model technique gives identical transfer functions and steady-state formulae.

Steady-state model: Rewriting (3.68)-(3.69) or (3.158)-(3.160)

$$I_L = \frac{V_o}{R} + I_z \tag{3.239}$$

$$V_o = V_c = \frac{DV_g - D'V_F - \left(r_L + r_x\right) I_z}{1 + \frac{1}{R}\left(r_L + r_x\right)} \tag{3.240}$$

Input voltage to output voltage transfer function: Rewriting (3.78) or (3.170),

$$G_{vg,nonideal}(s) = \frac{\tilde{v}_o(s)}{\tilde{v}_g(s)} = \frac{\frac{RD}{LC\left(R + r_c\right)}\left(r_c C s + 1\right)}{s^2 + \left(\frac{1}{L}\left(r_x + r_L + \frac{r_c R}{R + r_c} \right) + \frac{1}{C}\left(\frac{1}{R + r_c} \right) \right) s + \frac{r_x + r_L + R}{LC\left(R + r_c\right)}} \tag{3.241}$$

Load current to output voltage transfer function: Rewriting (3.79) or (3.172),

$$G_{vz,nonideal}(s) = \frac{\tilde{v}_o(s)}{\tilde{i}_z(s)} = \frac{\frac{-R}{LC\left(R + r_c\right)}\left(r_c C s + 1\right)\left(Ls + \left(r_L + r_x\right)\right)}{s^2 + \left(\frac{1}{L}\left(r_x + r_L + \frac{r_c R}{R + r_c} \right) + \frac{1}{C}\left(\frac{1}{R + r_c} \right) \right) s + \frac{r_x + r_L + R}{LC\left(R + r_c\right)}} \tag{3.242}$$

Duty cycle to output voltage transfer function: Rewriting (3.80) or (3.174),

$$G_{vd,nonideal}(s)=\frac{\tilde{v}_o(s)}{\tilde{d}(s)}=\frac{\dfrac{R\left(V_g+V_F-\left(r_{sw}-r_d\right)I_L\right)}{LC\left(R+r_c\right)}\left(r_cCs+1\right)}{s^2+\left(\dfrac{1}{L}\left(r_x+r_L+\dfrac{r_cR}{R+r_c}\right)+\dfrac{1}{C}\left(\dfrac{1}{R+r_c}\right)\right)s+\dfrac{r_x+r_L+R}{LC\left(R+r_c\right)}} \tag{3.243}$$

By substituting the parasitic elements to zero in the above equations, we get

Steady-state model:

$$I_L=\frac{V_o}{R}+I_z \tag{3.244}$$

$$V_o=DV_g \tag{3.245}$$

Input voltage to output voltage transfer function:

$$G_{vg,ideal}(s)=\frac{\tilde{v}_o(s)}{\tilde{v}_g(s)}=\frac{\dfrac{D}{LC}}{s^2+\dfrac{1}{RC}s+\dfrac{1}{LC}} \tag{3.246}$$

Load current to output voltage transfer function:

$$G_{vz,ideal}(s)=\frac{\tilde{v}_o(s)}{\tilde{i}_z(s)}=\frac{\dfrac{-s}{C}}{s^2+\dfrac{1}{RC}s+\dfrac{1}{LC}} \tag{3.247}$$

Duty cycle to output voltage transfer function:

$$G_{vd,ideal}(s)=\frac{\tilde{v}_o(s)}{\tilde{d}(s)}=\frac{\dfrac{V_g}{LC}}{s^2+\dfrac{1}{RC}s+\dfrac{1}{LC}} \tag{3.248}$$

The steady-state relationships and transfer functions in (3.244)-(3.248) are same as available in the literature. The comparison shows that the steady-state values of inductor current and output voltages are lesser in non-ideal case than the ideal case. Similarly, the location of poles and zeros are different in both cases. In non-ideal case, there is a zero due to capacitor ESR, which is absent in the ideal case. The effect of the non-idealities on the locations of poles and zeros will be discussed with the help of simulation results. The steady-state values, step response and Bode plots for the transfer functions of buck converter are compared for both the cases.

To obtain the MATLAB simulation results, the parameters of buck converter are considered as given in Table 3.1. The non-zero values of parasitic resistances of inductor, and capacitor and forward voltage drop of diode are also given in the table. For ideal DC-DC buck converter, these parasitic parameters are taken as zero. The steady-state value of load current variation (I_z) is assumed zero for the simulation results.

Table 3.1. Parameter values of non-ideal buck converter

Parameters	Value
Input voltage, V_g	16 V
Output voltage, V_o	12 V
Load resistance, R	11 Ω
Inductance, L/r_L	1.1 mH/0.18 Ω
Capacitance, C/r_c	84 μF/0.3 Ω
Diode forward voltage, V_F	0.7 V
Resistance switch/diode (r_{sw}/r_d),	0.044 Ω/0.024 Ω

3.4.1.1 Steady-state model

The values from Table 3.1 is substituted in steady-state model for ideal and non-ideal case given in (3.244)-(3.245) and (3.239)-(3.240), respectively. With these specifications, the values of steady-state parameters are shown in Table 3.2. According to these steady-state results, the value of steady-state inductor current and output voltage for non-ideal case is always less than the ideal case. This is due to the voltage drop across the non-ideal elements. The higher the values of these non-ideal elements, the more will be the difference in the steady-state values of both cases. This aspect has been discussed in detail in previous chapter.

Table 3.2. Comparison of steady-state parameters of ideal and non-ideal buck converter

Steady-state parameters	Ideal case	Non-ideal case
Inductor current, I_L	1.09 A	1.05 A
Output voltage, V_o (=V_c)	12 V	11.59 V
DC voltage gain factor (V_o/V_g)	0.75	0.725

3.4.1.2 Input voltage to output voltage transfer function

By plugging the values of different parameters in (3.246) and (3.241) respectively, we get

$$G_{vg,ideal}(s)=\frac{\tilde{v}_o(s)}{\tilde{v}_g(s)}=\frac{8.117\times10^6}{s^2+1082s+1.082\times10^7} \tag{3.249}$$

$$G_{vg,nonideal}(s)=\frac{\tilde{v}_o(s)}{\tilde{v}_g(s)}=\frac{199.1s+7.901\times10^6}{s^2+1518s+1.074\times10^7} \tag{3.250}$$

It is computed that the ideal buck converter is having two complex conjugate poles (at -541.12± *j* 3244.9) and no zero, whereas non-ideal buck converter is having two complex conjugate poles (at -759± *j* 3188.8) and one real zero (at -3.968 x 10^4). This real zero in non-ideal buck converter does exist due to ESR of the output capacitor.

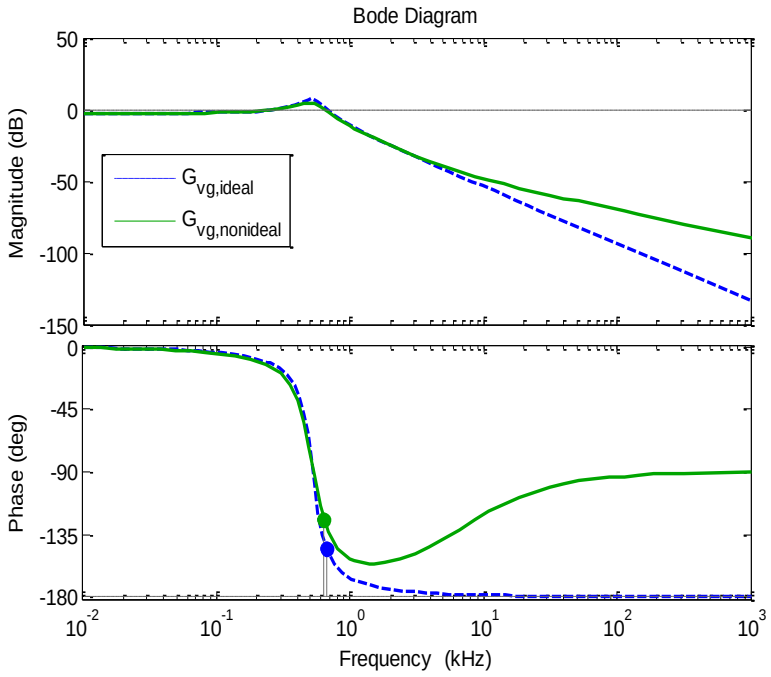


Fig. 3.13. Comparison of Bode plots of $G_{vg}(s)$ for ideal and non-ideal buck converter

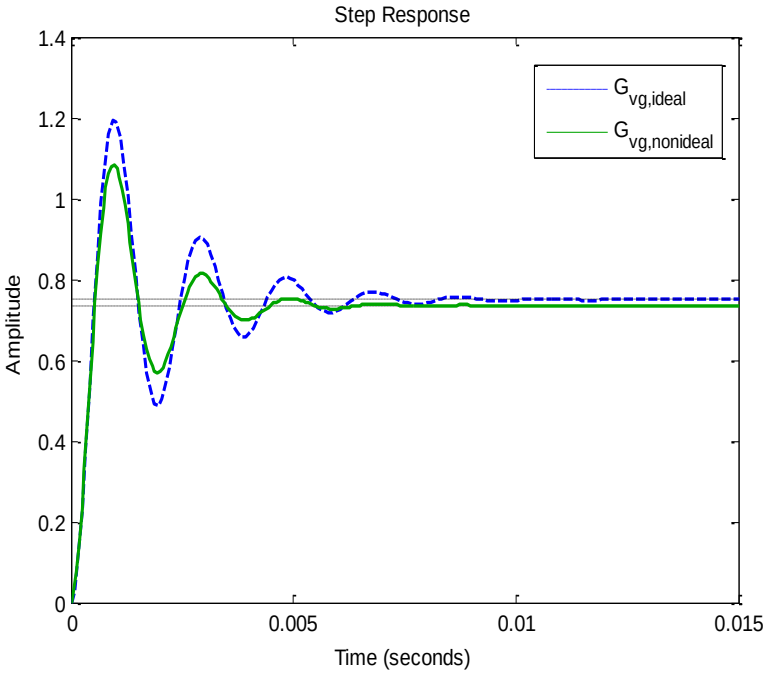


Fig. 3.14. Comparison of step responses of $G_{vg}(s)$ for ideal and non-ideal buck converter

Fig. 3.13 and Fig. 3.14 respectively show the Bode plots and step responses of transfer functions of ideal and non-ideal buck converter. In both the cases, the system is stable. For both the case, gain margin is infinite. The phase margin for the ideal case is 34° at gain crossover frequency 667 Hz, whereas for non-ideal case, it is 55.4° at gain crossover frequency 634 Hz. Thus, non-idealities increase the damping of buck converter and make it more stable and less oscillatory as also seen in the step response.

3.4.1.3 Load current to output voltage transfer function

By substituting the values of different parameters in (3.247) and (3.242) respectively, we get

$$G_{vz,ideal}(s) = \frac{\tilde{v}_o(s)}{\tilde{i}_z(s)} = \frac{-1.19\times10^4 s}{s^2 + 1082s + 1.082\times10^7} \tag{3.251}$$

$$G_{vz,nonideal}(s) = \frac{\tilde{v}_o(s)}{\tilde{i}_z(s)} = \frac{-0.292s^2 - 1.165\times10^4 s - 2.307\times10^6}{s^2 + 1518s + 1.074\times10^7} \tag{3.252}$$

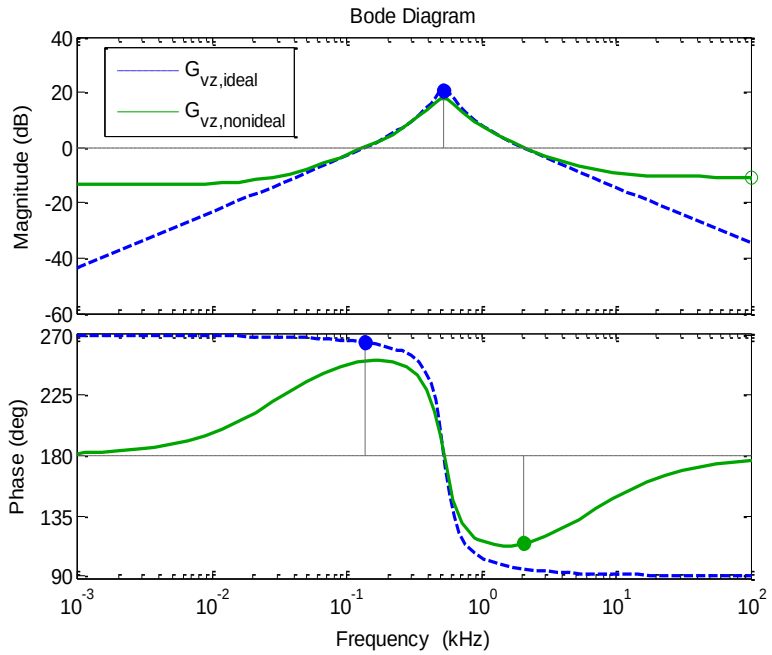


Fig. 3.15. Comparison of Bode plots of $G_{vz}(s)$ for ideal and non-ideal buck converter

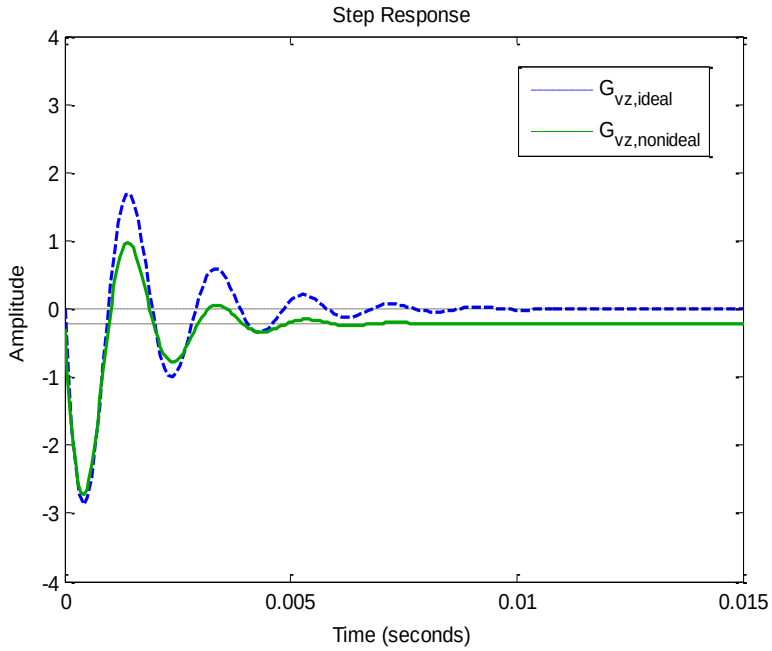


Fig. 3.16. Comparison of step responses of $G_{vz}(s)$ for ideal and non-ideal buck converter

It is found that the ideal buck converter is having two complex conjugate poles (at -541.12± *j* 3244.9) and one zero (at 0), whereas the transfer function of non-ideal buck converter is

having two complex conjugate poles (at -759± *j* 3188.8) and two real zeros (at -3.96 x 10^4 and -199). These real zeros in non-ideal buck converter do exist due to parasitic resistances.

The Bode plots and step responses of ideal and non-ideal transfer function are shown in Fig. 3.15 and Fig. 3.16, respectively. The gain margin for ideal case is -20.8 dB (at 524 Hz) and for non-ideal case, it is -17.6 dB (at 533 Hz). The phase margin in ideal case and non-ideal case is 84.8° (at 135 Hz) and 70° (at 136 Hz), respectively. It indicates that the closed-loop uncompensated buck converter will be unstable for the load variations in both the cases. The time response shows that for non-ideal case, there will be a steady-state error in output voltage for load current disturbances whereas for ideal buck converter it is zero.

3.4.1.4 Duty cycle to output voltage transfer function

By replacing the values of different parameters in (3.248) and (3.243) respectively, we get

$$G_{vd,ideal}(s)=\frac{\tilde{v}_o(s)}{\tilde{d}(s)}=\frac{1.732\times10^8}{s^2+1082s+1.082\times10^7} \tag{3.253}$$

$$G_{vd,nonideal}(s)=\frac{\tilde{v}_o(s)}{\tilde{d}(s)}=\frac{4428s+1.757\times10^8}{s^2+1518s+1.074\times10^7} \tag{3.254}$$

It is observed that the ideal buck converter is having two complex conjugate poles (at -541.12± *j* 3244.9) and no zero, whereas non-ideal buck converter is having two complex conjugate poles (at -759± *j* 3188.8) and one real zero (at -3.96 x 10^4). This real zero in non-ideal converter appears due to capacitor ESR.

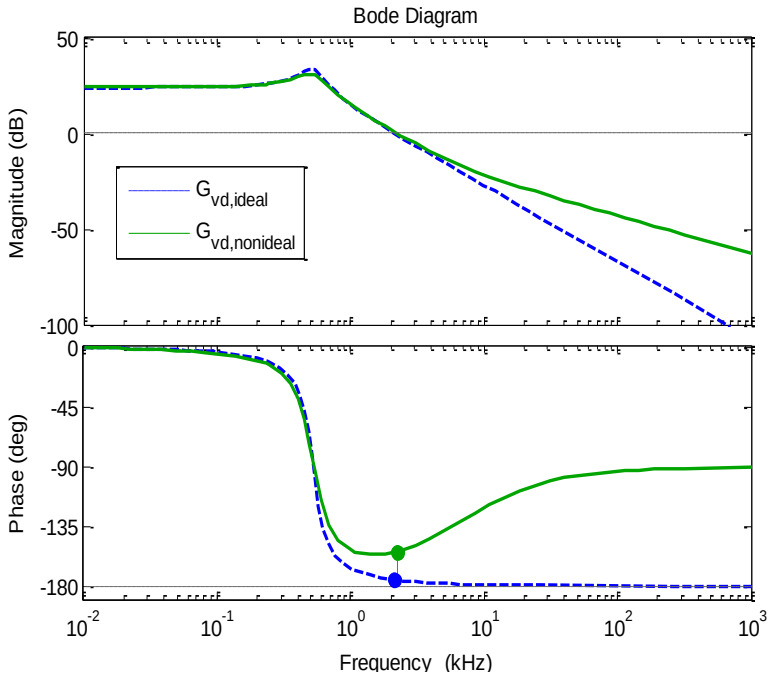


Fig. 3.17. Comparison of Bode plots of $G_{vd}(s)$ for ideal and non-ideal buck converter

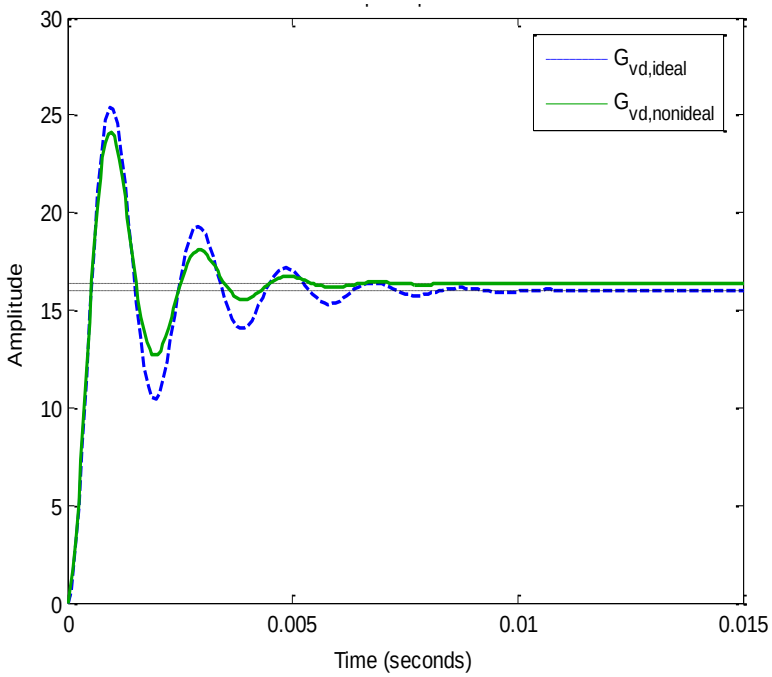


Fig. 3.18. Comparison of step responses of $G_{vd}(s)$ for ideal and non-ideal buck converter

The Bode plots and step responses of ideal and non-ideal buck converter are shown in Fig. 3.17 and Fig. 3.18, respectively. As the buck converter is a second-order system, therefore, the gain margin in both cases is infinite. The phase margin in ideal case and non-ideal case is 4.85° (at 2.16 kHz) and 26° (at 2.23 kHz), respectively. It indicates that the closed-loop system will be more stable in non-ideal case. The time response also shows that in the non-ideal case the step response is having less overshoot and oscillations. This is because of the damping provided by the parasitic resistances.

3.4.2 Cuk converter

It has been observed in the previous sections that the state-space averaging method and averaged switch model technique give identical steady-state formulae and transfer functions. In order to summarize, the steady-state and transfer function models of non-ideal DC-DC Cuk converter are rewritten as follows:

Steady-state model: Rewriting (3.112)-(3.115) or (3.203)-(3.207),

$$I_{L1} = \frac{D}{D'} I_{L2} \tag{3.255}$$

$$I_{L2} = \frac{V_o}{R} + I_z \tag{3.256}$$

$$V_{c1} = \frac{V_g}{D'} - V_F - \frac{\left(Dr_{L1} + DD'r_{c1} + r_x\right)}{D'^2} I_{L2} \tag{3.257}$$

$$V_o = V_{c2} = \frac{\frac{D}{D'}V_g - V_F - \left(\left(\frac{D}{D'}\right)^2 r_{L1} + r_{L2} + \frac{D}{D'}r_{c1} + \frac{r_x}{D'^2}\right)I_z}{1 + \frac{1}{R}\left(\left(\frac{D}{D'}\right)^2 r_{L1} + r_{L2} + \frac{D}{D'}r_{c1} + \frac{r_x}{D'^2}\right)} \tag{3.258}$$

Input voltage to output voltage transfer function: Rewriting (3.128) or (3.224),

$$G_{vg,nonideal}(s) = \frac{\tilde{v}_o(s)}{\tilde{v}_g(s)} = \frac{K_{og}(ps+1)\left(p_{g1}s + p_{g0}\right)}{s^4 + a_3 s^3 + a_2 s^2 + a_1 s^1 + a_0} \tag{3.259}$$

Where, $$K_{og} = \frac{R}{L_1 L_2 C_1 C_2 (R + r_{c2})}, p = r_{c2}C_2, p_{g1} = -r_x C_1, p_{g0} = DD', \tag{3.260}$$

$$a_3 = \frac{(r_x + r_{L1} + D'r_{c1})}{L_1} + \frac{1}{L_2}\left(r_x + r_{L2} + Dr_{c1} + \frac{r_{c2}R}{R + r_{c2}}\right) + \frac{1}{C_2}\left(\frac{1}{R + r_{c2}}\right) \tag{3.261}$$

$$a_2 = \frac{1}{L_1 L_2}\left((r_x + r_{L1} + D'r_{c1})\left(r_{L2} + Dr_{c1} + \frac{r_{c2}R}{R + r_{c2}}\right) + r_x(r_{L1} + D'r_{c1})\right) + \frac{D'^2}{L_1 C_1} + \frac{(r_x + r_{L1} + D'r_{c1})}{L_1 C_2 (R + r_{c2})} + \frac{D^2}{L_2 C_1} + \frac{(R + r_x + r_{L2} + Dr_{c1})}{L_2 C_2 (R + r_{c2})} \tag{3.262}$$

$$a_1 = \frac{1}{L_1 L_2 C_1}\left(r_x + D^2 r_{L1} + D'^2 r_{L2} + DD'r_{c1} + D'^2\left(\frac{r_{c2}R}{R + r_{c2}}\right)\right) + \frac{\left((r_x + r_{L1} + D'r_{c1})(R + r_{L2} + Dr_{c1}) + r_x(r_{L1} + D'r_{c1})\right)}{L_1 L_2 C_2 (R + r_{c2})} + \frac{D^2 L_1 + D'^2 L_2}{L_1 L_2 C_1 C_2 (R + r_{c2})} \tag{3.263}$$

$$a_0 = \frac{D'^2 R + D^2 r_{L1} + D'^2 r_{L2} + DD'r_{c1} + r_x}{L_1 L_2 C_1 C_2 (R + r_{c2})} \tag{3.264}$$

Load current to output voltage transfer function: Rewriting (3.131) or (3.231),

$$G_{vz,nonideal}(s) = \frac{\tilde{v}_o(s)}{\tilde{i}_z(s)} = \frac{K_{oz}(ps+1)\left(p_{z3}s^3 + p_{z2}s^2 + p_{z1}s + p_{z0}\right)}{s^4 + a_3 s^3 + a_2 s^2 + a_1 s^1 + a_0} \tag{3.265}$$

$$K_{oz} = \frac{-R}{L_1 L_2 C_1 C_2 (R + r_{c2})}, p = r_{c2}C_2, p_{z3} = L_1 L_2 C_2, p_{z2} = L_1 C_1 (r_x + r_{L2} + Dr_{c1}) + L_2 C_1 (r_x + r_{L1} + D'r_{c1}),$$
$$p_{z1} = D^2 L_1 + D'^2 L_2 + C_1\left((r_x + r_{L1} + D'r_{c1})(r_{L2} + Dr_{c1}) + r_x(r_{L1} + D'r_{c1})\right), p_{z0} = D^2 r_{L1} + D'^2 r_{L2} + DD'r_{c1} + r_x \tag{3.266}$$

The coefficients a_3, a_2, a_1 and a_0 are same as in (3.261)-(3.264).

Duty cycle to output voltage transfer function: Rewriting (3.134) or (3.238),

$$G_{vd,nonideal}(s) = \frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{K_{od}(ps+1)\left(p_{d2}s^2 + p_{d1}s + p_{d0}\right)}{s^4 + a_3 s^3 + a_2 s^2 + a_1 s^1 + a_0} \tag{3.267}$$

$$K_{od} = \frac{R}{L_1 L_2 C_1 C_2 (R + r_{c2})}, p = r_{c2}C_2, p_{d1} = (r_{L1} + D'r_{c1})C_1(V_{c1} + V_F) - L_1 I_{L1} - \left((r_{L1} + D'r_{c1})\left(r_{c1} + \frac{r_{sw}}{D'^2}\right) - \frac{r_{L1}r_x}{D'^2}\right)C_1 I_{L2}$$
$$p_{d2} = L_1 C_1\left[V_{c1} + V_F - \left(r_{c1} + \frac{r_{sw} - r_D}{D'}\right)I_{L2}\right], p_{d0} = D'(V_{c1} + V_F) - \left(\frac{D}{D'}r_{L1} + D'r_{c1} + \frac{r_{sw}}{D'}\right)I_{L2} \tag{3.268}$$

The coefficients a_3, a_2, a_1 and a_0 are same as in (3.261)-(3.264).

In order to get the steady-state and transfer function models of ideal Cuk converter, by replacing the parasitics to zero in the above relations, we get

Steady-state model:

$$I_{L1} = \frac{D}{D'} I_{L2} \tag{3.269}$$

$$I_{L2} = I_o + I_z = \frac{V_o}{R} + I_z \tag{3.270}$$

$$V_{c1} = \frac{V_g}{D'} \tag{3.271}$$

$$V_o = V_{c2} = \frac{D}{D'} V_g \tag{3.272}$$

Input voltage to output voltage transfer function:

$$G_{vg,ideal}(s) = \frac{\tilde{v}_o(s)}{\tilde{v}_g(s)} = \frac{\dfrac{DD'}{L_1L_2C_1C_2}}{s^4 + \dfrac{1}{RC_2}s^3 + \left(\dfrac{D'^2}{L_1C_1} + \dfrac{D^2}{L_2C_1} + \dfrac{1}{L_2C_2}\right)s^2 + \dfrac{D^2L_1 + D'^2L_2}{RL_1L_2C_1C_2}s + \dfrac{D'^2}{L_1L_2C_1C_2}} \tag{3.273}$$

Load current to output voltage transfer function:

$$G_{vz,ideal}(s) = \frac{\tilde{v}_o(s)}{\tilde{i}_z(s)} = \frac{\dfrac{-1}{L_1L_2C_1C_2}\left(L_1L_2C_2s^3 + \left(D^2L_1 + D'^2L_2\right)s\right)}{s^4 + \dfrac{1}{RC_2}s^3 + \left(\dfrac{D'^2}{L_1C_1} + \dfrac{D^2}{L_2C_1} + \dfrac{1}{L_2C_2}\right)s^2 + \dfrac{D^2L_1 + D'^2L_2}{RL_1L_2C_1C_2}s + \dfrac{D'^2}{L_1L_2C_1C_2}} \tag{3.274}$$

Duty cycle to output voltage transfer function:

$$G_{vd,ideal}(s) = \frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{\dfrac{1}{L_1L_2C_1C_2}\left(L_1C_1V_{c1}s^2 - L_1I_{L1}s + D'V_{c1}\right)}{s^4 + \dfrac{1}{RC_2}s^3 + \left(\dfrac{D'^2}{L_1C_1} + \dfrac{D^2}{L_2C_1} + \dfrac{1}{L_2C_2}\right)s^2 + \dfrac{D^2L_1 + D'^2L_2}{RL_1L_2C_1C_2}s + \dfrac{D'^2}{L_1L_2C_1C_2}} \tag{3.275}$$

The steady-state relationships and transfer functions in (3.269)-(3.275) are same as given in existing literature. The comparison shows that the steady-state values of all the variables are less if the non-idealities are present. Similarly, the non-idealities also affect the location of poles and zeros. The total number of zeros present in the transfer function of the ideal Cuk converter is also less than the non-ideal Cuk converter. The effect of non-idealities on poles and zeros will be discussed with the help of simulation results.

In order to compare the steady-state values, step response and Bode plots of the ideal and non-ideal Cuk converter transfer functions, the MATLAB simulation results are obtained for both the cases. The parameters of the non-ideal Cuk converter considered for the simulation is shown in Table 3.3. For the ideal Cuk converter, all the parameters remain same except the non-idealities replaced to zero. The steady-state value of load current variation (I_z) is assumed zero in simulation results.

Table 3.3. Parameter values of non-ideal Cuk converter

Parameters	Value
Input voltage, V_g	20 V
Output voltage, V_o	16 V
Load resistance, R	11 Ω
Inductance, L_1/r_{L1}	3 mH/0.35 Ω
Inductance, L_2/r_{L2}	1.9 mH/0.25 Ω
Capacitance, C_1/r_{c1}	420 μF/0.11 Ω
Capacitance, C_2/r_{c2}	420 μF/0.11 Ω
Diode forward voltage, V_F	0.7 V
Resistance switch/diode (r_{sw}/r_d),	0.044 Ω/0.024 Ω

3.4.2.1 Steady-state model

In the steady-state model of ideal and non-ideal Cuk converter respectively given by (3.269)-(3.272) and (3.255)-(3.258), the values of various parameters are substituted from Table 3.3. With these substitutions, the values of steady-state parameters of Cuk converter are obtained as given in Table 3.4. These steady-state results show that the value of steady-state currents and voltages for non-ideal case are always less than the ideal case. This is due to the power loss in the non-ideal elements. It has been discussed widely in the previous chapter.

Table 3.4. Comparison of steady-state parameters of ideal and non-ideal Cuk converter

Steady-state parameters	Ideal case	Non-ideal case
Inductor current, I_{L1}	1.16 A	1.05 A
Inductor current, I_{L2}	1.45 A	1.31 A
Capacitor voltage, V_{c1}	36 V	34.38 V
Output voltage, V_o (=V_{c2})	16 V	14.42 V
DC voltage gain factor (V_o/V_g)	0.8	0.721

3.4.2.2 Input voltage to output voltage transfer function

By putting the values of the converter parameters in (3.273) and (3.259), respectively, we get

$$G_{vg,ideal}(s) = \frac{\tilde{v}_o(s)}{\tilde{v}_g(s)} = \frac{2.456\times10^{11}}{s^4 + 216.5s^3 + 1.746\times10^6 s^2 + 1.06\times10^8 s + 3.07\times10^{11}} \quad (3.276)$$

$$G_{vg,nonideal}(s) = \frac{\tilde{v}_o(s)}{\tilde{v}_g(s)} = \frac{-628.4s^2 - 2.369\times10^6 s + 2.431\times10^{11}}{s^4 + 594.2s^3 + 1.836\times10^6 s^2 + 3.949\times10^8 s + 3.224\times10^{11}} \quad (3.277)$$

The ideal Cuk converter is having four complex conjugate poles (at -84.5± *j* 1237.3 and -23.6± *j* 446.1) and no zero. On the other hand, non-ideal Cuk converter is having four complex conjugate poles (at -196± *j* 1229 and -101± *j* 444.8) and two real zeros (at -2.16 x 10^4 and 1.78 x 10^4).

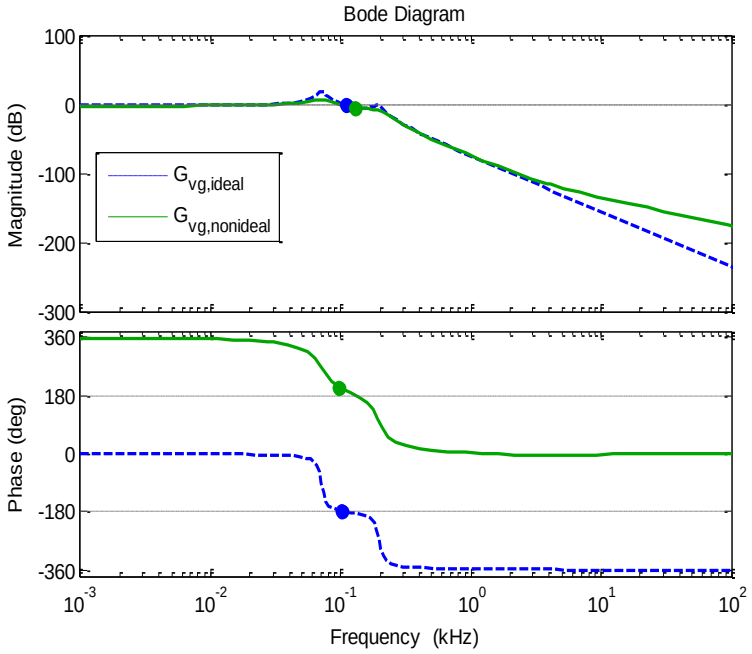


Fig. 3.19. Comparison of Bode plots of $G_{vg}(s)$ for ideal and non-ideal Cuk converter

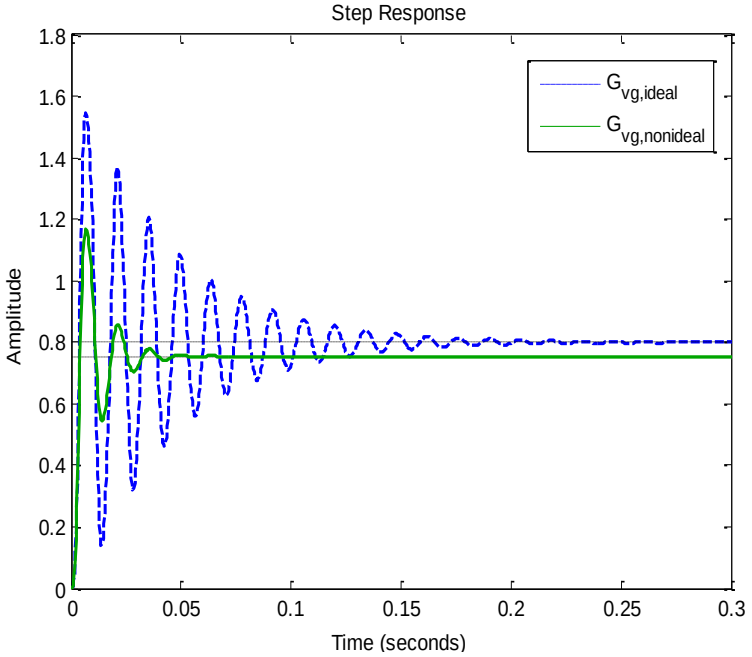


Fig. 3.20. Comparison of step responses of $G_{vg}(s)$ for ideal and non-ideal Cuk converter

Fig. 3.19 and Fig. 3.20 show the Bode plots and step responses of these ideal and non-ideal Cuk converter transfer functions. In both the cases, the system is stable. For ideal case, gain margin is 2.03 dB (at 112 Hz) and phase margin is 2.52° (at 103 Hz). For non-ideal case, gain margin is 5.38 dB (at 129 Hz) and phase margin is 25.7° (at 96.6 Hz). Therefore, the non-idealities make the Cuk converter output voltage more stable in the presence of input voltage disturbances. As also observed from step response, the non-ideal Cuk converter is having a less oscillatory response.

3.4.2.3 Load current to output voltage transfer function

By inserting the respective values of parameters in (3.274) and (3.265) respectively, we get

$$G_{vz,ideal}(s)=\frac{\tilde{v}_o(s)}{\tilde{i}_z(s)}=\frac{-2381s^3-1.173\times10^9 s}{s^4+216.5s^3+1.746\times10^6 s^2+1.066\times10^8 s+3.07\times10^{11}} \quad (3.278)$$

$$G_{vz,nonideal}(s)=\frac{\tilde{v}_o(s)}{\tilde{i}_z(s)}=\frac{-0.1089s^4-2393s^3-8.17\times10^5 s^2-1.231\times10^9 s-2.032\times10^{11}}{s^4+594.2s^3+1.836\times10^6 s^2+3.949\times10^8 s+3.224\times10^{11}} \quad (3.279)$$

The ideal Cuk converter is having four complex conjugate poles (at -84.5± *j* 1237.3 and -23.6± *j* 446.1) and three zeros (at 0, ± *j* 701.77), whereas non-ideal buck converter have four complex conjugate poles (at -196± *j* 1229 and -101± *j* 444.8) and four zeros (at -2.16 x 10^4, -175.07 and -73.77± *j* 697.75).

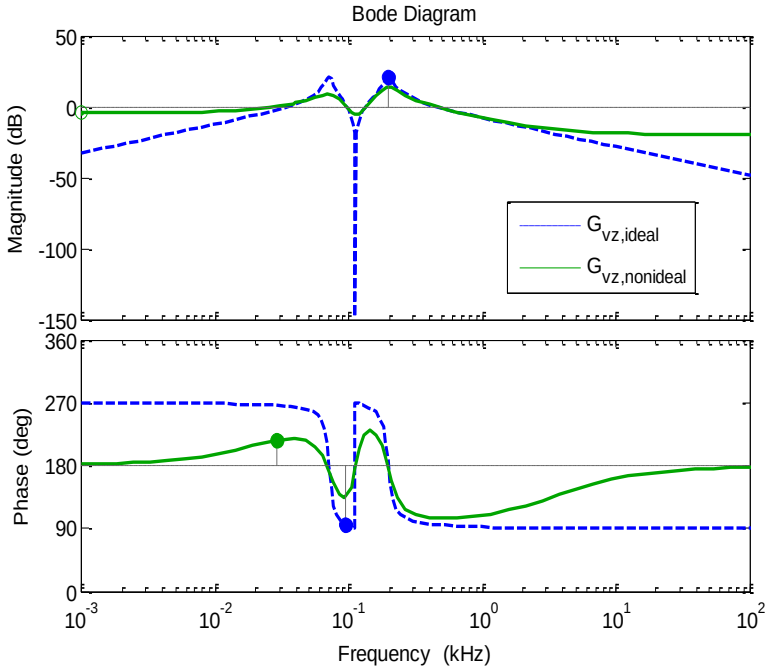


Fig. 3.21. Comparison of Bode plots of $G_{vz}(s)$ for ideal and non-ideal Cuk converter

Fig. 3.21 and Fig. 3.22 show the Bode plots and step responses of ideal and non-ideal Cuk converter. For ideal case, gain margin is -20.8 dB (at 71 Hz) and phase margin is 84.8° (at 34 Hz). For non-ideal case, gain margin is -8.6 dB (at 67.9 Hz) and phase margin is 35.2° (at 28.6 Hz). It indicates that the closed-loop uncompensated Cuk converter will be unstable for the load variations in both the ideal and non-ideal cases. It may be observed from time response that the steady-state error is zero in the ideal case, whereas it is non-zero for the non-ideal case in the presence of load current disturbances.

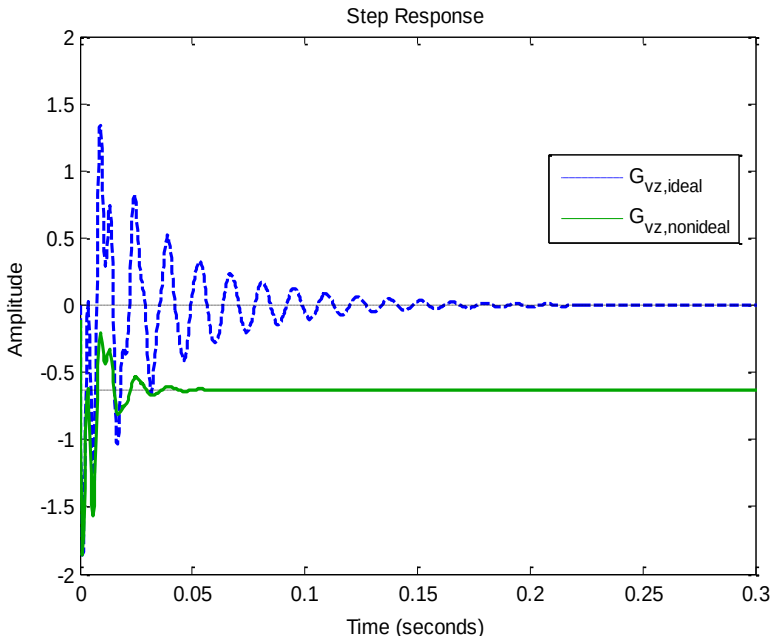


Fig. 3.22. Comparison of step responses of $G_{vz}(s)$ for ideal and non-ideal Cuk converter

3.4.2.4 Duty cycle to output voltage transfer function

By replacing the values of different parameters in (3.275) and (3.267) respectively, we get

$$G_{vd,ideal}(s)=\frac{\tilde{v}_o(s)}{\tilde{d}(s)}=\frac{4.511\times10^7 s^2-3.472\times10^9 s+1.989\times10^{13}}{s^4+216.5s^3+1.746\times10^6 s^2+1.066\times10^8 s+3.07\times10^{11}} \quad (3.280)$$

$$G_{vd,nonideal}(s)=\frac{\tilde{v}_o(s)}{\tilde{d}(s)}=\frac{2000s^3+4.342\times10^7 s^2+3.692\times10^9 s+1.865\times10^{13}}{s^4+594.2s^3+1.836\times10^6 s^2+3.949\times10^8 s+3.224\times10^{11}} \quad (3.281)$$

It is observed that the ideal Cuk converter is having four complex conjugate poles (at -84.5± *j* 1237.3 and -23.6± *j* 446.1) and two right half plane zeros (at 38.48± *j* 662.9) whereas non-ideal Cuk converter is having four complex conjugate poles (at -196± *j* 1229 and -101± *j* 444.8) and three zeros (at -2.16 x 10^4, -32.68± *j* 655.55). It indicates that ideal converter behavior is non-minimum phase system, whereas actual (non-ideal) Cuk converter is minimum phase system.

The frequency responses (Bode plots) and step time responses of ideal and non-ideal Cuk converter are shown in Fig. 3.23 and Fig. 3.24, respectively. For the ideal Cuk converter, gain margin is -37.8 dB (at 83.7 Hz) and phase margin is 2.52° (at 1.08 kHz). For non-ideal Cuk converter, gain margin is infinite and phase margin is 22.1° (at 1.09 kHz). Therefore, the closed-loop uncompensated ideal Cuk converter in an unstable system and closed-loop non-ideal Cuk converter gives stable output voltage for duty cycle variations. From the open loop step response, it is observed that parasitic resistances in non-ideal converter provides damping and therefore improves the system transient response.

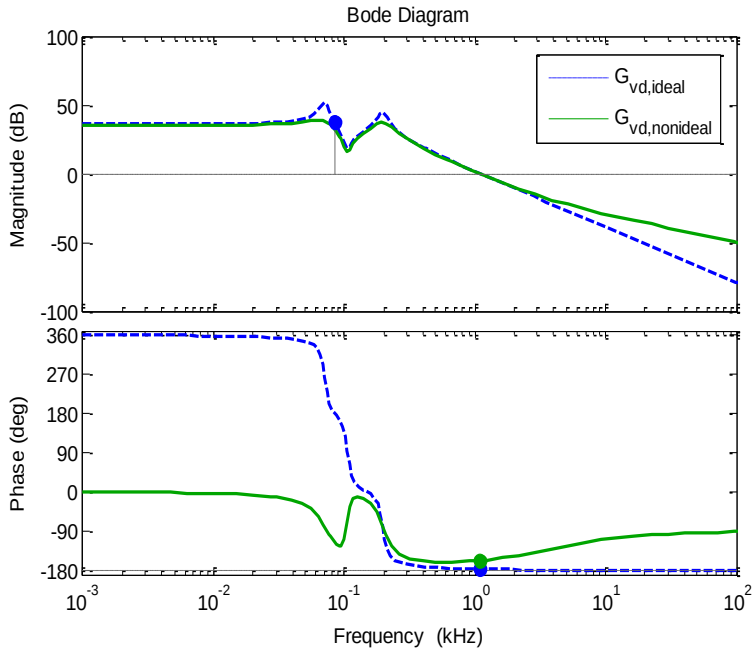


Fig. 3.23. Comparison of Bode plots of $G_{vd}(s)$ for ideal and non-ideal Cuk converter

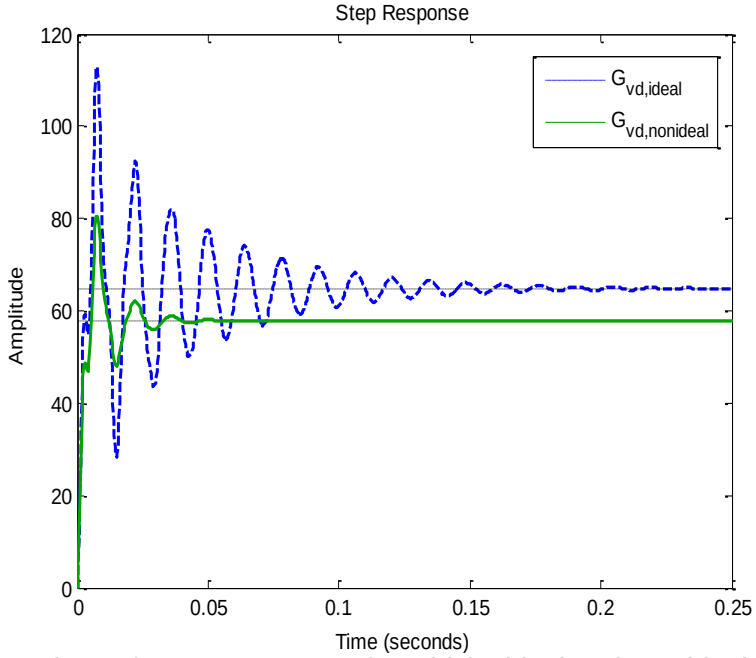


Fig. 3.24. Comparison of step responses of $G_{vd}(s)$ for ideal and non-ideal Cuk converter

From these discussions about buck and Cuk converters, it is concluded that negligence of non-idealities gives a less accurate converter model, which may lead to selection of inefficient compensator design. A special attention is required while deriving model of Cuk converter because depending upon the parasitic values, it may or may not be a non-minimum phase system.

3.5 Modeling using Energy Factor Approach

The mathematical modeling of the complex and higher-order converters using the conventional techniques needs lot of computations because of the involvement of higher-order differential equations. Therefore, in the literature, the mathematical modeling of DC-DC

converters have also been carried out using the concept of energy factor [69], [70]. This concept makes use of the energy storage capability of DC-DC converters. A DC-DC converter is considered as an energy container, which has some energy storage elements such as inductors and capacitors. These elements store the energy during operation of DC-DC converters. The stored energy varies if the working conditions changes. In other word, when converter changes from one steady-state to other steady-state, the corresponding stored energy also changes. Therefore, there will be a transient phenomenon between one steady-state to other. Based on this concept, the term energy factor and other related terms are defined in [70], which reveal the relationship between stored energy and the characteristics of DC-DC converters. The energy factor and its associated parameters such as pumping energy (PE), stored energy (SE), capacitor/inductor stored energy ratio (CIR) and energy loss (EL) are used to describe the large-signal and small-signal behaviour of DC-DC converters. Using these parameters, two terms, namely time constant and damping time constant is described. The beauty of this proposed method [70] is that any DC-DC power converter can be characterized by a second-order transfer function in terms of time constant (τ) and damping time constant (τ_d). The transient phenomenon of a DC-DC converter can be analysed by the pole-zero location of this second-order transfer function. The detailed description of all these parameters and transfer function are described in the following section.

3.5.1 Energy factor and its associated parameters

All DC-DC converters have an input DC power supply source, energy storage elements, filter circuit and load. Let the switching period is denoted by T. The following terms in respect to DC-DC converter are defined for time period T as [70]:

The input energy or pumping energy is

$$PE = P_{in} \cdot T = V_g I_g T \tag{3.282}$$

V_g is the input voltage, I_g is the average input current and P_{in} is input power.

The total energy stored in inductors (for m number of inductors) is

$$W_L = \frac{1}{2}\sum_{i=1}^{m} L_i I_{Li}^2 \tag{3.283}$$

L_i is the value of the inductor and I_{Li} is the average value of current in i^{th} inductor.

The total energy stored in capacitors (for n number of capacitors) is

$$W_C = \frac{1}{2}\sum_{i=1}^{n} C_i V_{ci}^2 \tag{3.284}$$

C_i is the value of the capacitor and V_{ci} is the average value of voltage across i^{th} capacitor.

Therefore, the total stored energy is

$$SE = W_L + W_C = \frac{1}{2}\left(\sum_{i=1}^{m} L_i I_{Li}^2 + \sum_{i=1}^{n} C_i V_{ci}^2\right) \tag{3.285}$$

The capacitor to inductor stored energy ratio is

$$CIR = \frac{W_C}{W_L} \tag{3.286}$$

The energy factor is defined as the ratio of total stored energy and pumping energy.

$$EF = \frac{SE}{PE} = \frac{W_L + W_C}{V_g I_g T} \tag{3.287}$$

The efficiency of DC-DC converter is

$$\eta = \frac{P_o}{P_o + P_L} \tag{3.288}$$

P_o is the power delivered to the load and P_L is the total power loss in the DC-DC converter.

3.5.1.1 Time constant (τ)

The time constant τ for a DC-DC converter is defined as [70]

$$\tau = \frac{2T \times EF}{1 + CIR}\left(1 + CIR\frac{1-\eta}{\eta}\right) \tag{3.289}$$

This parameter is used to estimate the transient operation of DC-DC converter. It is proportional to settling time. According to [70], it is independent of the converter duty cycle and switching frequency.

3.5.1.2 Damping time constant (τ_d)

The time constant τ for a DC-DC converter is defined as [70]

$$\tau_d = \frac{2T \times EF}{1 + CIR}\left(\frac{CIR}{\eta + CIR(1-\eta)}\right) \tag{3.290}$$

The damping time constant is used to estimate the oscillation in the transient response of DC-DC converter. According to [70] , it is also independent of the converter duty cycle and switching frequency.

3.5.1.3 Transfer function of DC-DC converter

The generalized transfer function of DC-DC converter is defined as [69], [70]

$$G(s) = \frac{M_v}{\tau\tau_d s^2 + \tau s + 1} = \frac{\frac{M_v}{\tau\tau_d}}{s^2 + \frac{1}{\tau_d}s + \frac{1}{\tau\tau_d}} \tag{3.291}$$

$M_v = V_o/V_g$ is DC voltage gain of DC-DC converter.

Equation (3.291) gives the generalized mathematical model for any DC-DC converter as a second-order transfer function. However, this transfer function provides the relationship between input voltage and output voltage only. For controller design, the duty-cycle to the output voltage transfer function is required, which is not obtained by the method proposed in [70]. Moreover, the original research in [69], [70] states that the time constant (τ) and damping time constant (τ_d) are independent of the converter duty cycle and switching frequency. In the research work of this thesis, it is found that these time constants do depend on duty cycle and switching frequency. It has been proven with a detail analysis of non-ideal DC-DC buck converter and Cuk converter. The following analysis simplifies the calculation of time constant (τ) and damping time constant (τ_d).

3.5.2 Simplified analysis

Let r_{loss} is the equivalent resistance as referred to load side, which is responsible for the power loss in the DC-DC converter. Then, the power loss in converter can be defined as:

$$P_L = I_o^2 r_{loss} \tag{3.292}$$

Therefore, power input

$$P_{in} = P_o + P_L = I_o^2 \left(R + r_{loss}\right) \tag{3.293}$$

and Efficiency

$$\eta = \frac{P_o}{P_{in}} = \frac{P_o}{P_o + P_L} = \frac{I_o^2 R}{I_o^2 R + I_o^2 r_{loss}} = \frac{R}{R + r_{loss}} \tag{3.294}$$

The DC current gain of DC-DC converter is

$$M_i = \frac{I_o}{I_g} \tag{3.295}$$

The DC voltage gain of DC-DC converter is

$$M_v = \frac{V_o}{V_g} \tag{3.296}$$

It can be written in following form

$$M_v = \frac{V_o}{V_g} = \frac{V_o I_o}{V_g I_g} \cdot \frac{1}{M_i} = \frac{R}{R + r_{loss}} \cdot \frac{1}{M_i} = \frac{\cancel{1}/M_i}{1 + \frac{r_{loss}}{R}} \tag{3.297}$$

The factor $\frac{2T \times EF}{1 + CIR}$ appears in expression of τ and τ_d in (3.289)-(3.290). It is simplified as follows

$$\frac{2T \times EF}{1 + CIR} = \frac{2T \times \frac{W_L + W_C}{P_{in} \cdot T}}{1 + \frac{W_C}{W_L}} = \frac{2W_L}{P_{in}} = \frac{2W_L}{I_o^2 \left(R + r_{loss}\right)} \tag{3.298}$$

Substituting this value into (3.289)-(3.290), the simplified expression for the time constant (τ) and damping time constant (τ_d) are obtained as

$$\tau = \frac{2W_L}{I_o^2 \left(R + r_{loss}\right)} \left(1 + CIR \frac{r_{loss}}{R}\right) \tag{3.299}$$

$$\tau_d = \frac{2W_L \cdot CIR}{I_o^2 \left(R + r_{loss} CIR\right)} \tag{3.300}$$

Now, these simplified expressions are applied to obtain the mathematical model of DC-DC buck converter and Cuk converter. In [69], [70], the mathematical models for buck converter and super-lift Luo converter were obtained using this approach, but only resistance of the inductor (r_L) was added as lossy component. However, in following analysis, all the non-idealities have been considered to get the accurate model.

3.5.3 Non-ideal buck converter

Fig. 3.25 shows the schematic of DC-DC buck converter including all the major non-idealities. The operation of converter remains same as discussed previously. The buck converter is considered operating in continuous conduction mode with switching period *T* (switching frequency *f*) and static duty cycle *D*. In the following discussion, the mathematical model for buck converter is evaluated using energy factor approach.

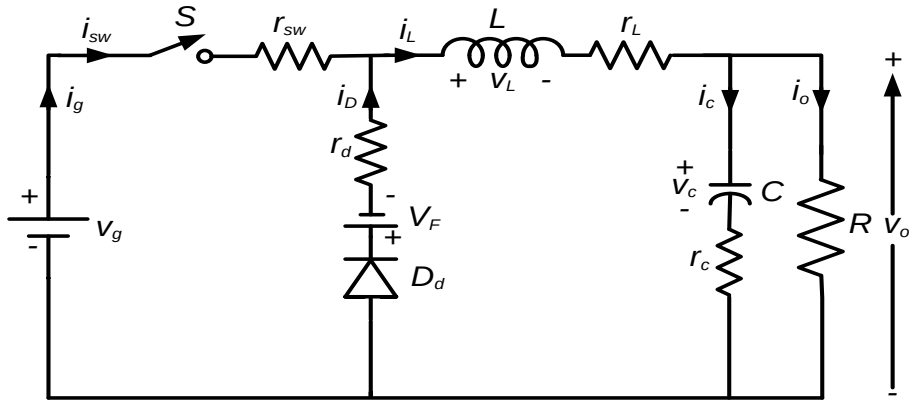


Fig. 3.25. Non-ideal DC-DC buck converter

By the steady-state analysis of buck converter, the following useful relations are derived in Appendix *A*.

The average values of input current (I_g), output current (I_o) and diode current (I_D) are

$$I_o = I_L,\ I_g = DI_L,\ I_D = D'I_L, \tag{3.301}$$

The rms values of inductor current, capacitor current, switch current and diode current are

$$i_{L,rms} = \sqrt{I_L^2 + \frac{\Delta i_L^2}{12}}, i_{c,rms} = \frac{\Delta i_L}{\sqrt{12}}, i_{sw,rms} = \sqrt{D\left(I_L^2 + \frac{\Delta i_L^2}{12}\right)}, i_{D,rms} = \sqrt{D'\left(I_L^2 + \frac{\Delta i_L^2}{12}\right)}, \tag{3.302}$$

Where, $\Delta i_L = D' \dfrac{(r_d + r_L)I_L + V_F + V_o}{Lf}$

The power loss in different elements of non-ideal buck converter will be

$$P_L = P_{rL} + P_{rC} + P_{rSw} + P_{rD} + P_{VD} = r_{loss} I_o^2 \tag{3.303}$$

Where, $$r_{loss} = \left(r_L + Dr_{sw} + D'r_D + \frac{RD'V_F}{V_o}\right) + \left(r_L + r_c + Dr_{sw} + D'r_D\right)\frac{\Delta i_L^2}{12I_L^2} \tag{3.304}$$

Since the inductor current ripple is function of the switching frequency and therefore, r_{loss} is also function of switching frequency and duty cycle as well.

The energy stored in the inductor is

$$W_L = \frac{1}{2}LI_L^2 = \frac{1}{2}LI_o^2 \tag{3.305}$$

The energy stored in the capacitor is

$$W_C = \frac{1}{2}CV_o^2 = \frac{1}{2}CR^2I_o^2 \tag{3.306}$$

The capacitor-inductor stored energy ratio is

$$CIR = \frac{W_C}{W_L} = \frac{CR^2}{L} \tag{3.307}$$

The DC current gain is

$$M_i = \frac{I_o}{I_g} = \frac{1}{D} \tag{3.308}$$

Calculation of voltage gain (M_v):

Substituting values from (3.308) into (3.297),

$$M_v = \frac{D}{1+\frac{r_{loss}}{R}} \tag{3.309}$$

Calculation of time constant (τ):

Substituting values from (3.305) and (3.307) into (3.299), we get

$$\tau = \frac{2\left(\frac{1}{2}LI_o^2\right)}{I_o^2\left(R+r_{loss}\right)}\left(1+\frac{CR^2}{L}\frac{r_{loss}}{R}\right) = \frac{L+CRr_{loss}}{R+r_{loss}} \tag{3.310}$$

Calculation of damping time constant (τ_d):

Substituting values from (3.305) and (3.307) into (3.300), we get

$$\tau_d = \frac{2\left(\frac{1}{2}LI_o^2\right)}{I_o^2}\left(\frac{\frac{CR^2}{L}}{R+r_{loss}\frac{CR^2}{L}}\right) = \frac{CRL}{L+CRr_{loss}} \tag{3.311}$$

From (3.310) and (3.311), it is clear that τ and τ_d are function of loss component r_{loss}. As observed from (3.304), this loss component r_{loss} is function of duty cycle *D* and switching frequency *f*. Therefore, τ and τ_d will also be the function of duty cycle *D* and switching frequency *f*. Thus, the fundamental statement of [69], [70] becomes incorrect, which states that τ and τ_d remain unchanged with variation in *D* and *f*. This is also verified by the simulation results later.

3.5.4 Non-ideal Cuk converter

Fig. 3.26 shows the circuit diagram of DC-DC Cuk converter that includes all the non-idealities. The operation of the Cuk converter has already been explained earlier. The Cuk converter is considered operating in continuous conduction mode with switching period *T* (switching frequency *f*) and static duty cycle *D*. In the following discussion, the mathematical model for the Cuk converter is evaluated using energy factor approach. By the steady-state analysis of Cuk converter, the following useful relations are found in Appendix *A*.

The average values of input current (I_g), output current (I_o) and diode current (I_D) are

$$I_o = I_{L2}, I_g = I_{L1} = \frac{D}{D'}I_{L2} = \frac{D}{D'}I_o, I_D = D'\left(I_{L1}+I_{L2}\right) = I_o, \tag{3.312}$$

The rms values of inductor currents, capacitor currents, switch current and diode current are

$$i_{L1,rms} = I_o\sqrt{\frac{D^2}{D'^2}+\frac{\Delta i_{L1}^2}{12I_o^2}}, i_{L2,rms} = I_o\sqrt{1+\frac{\Delta i_{L2}^2}{12I_o^2}}, i_{c1,rms} = I_o\sqrt{\frac{D}{D'}+\frac{1}{12I_o^2}\left(D\Delta i_{L2}^2+D'\Delta i_{L1}^2\right)},$$

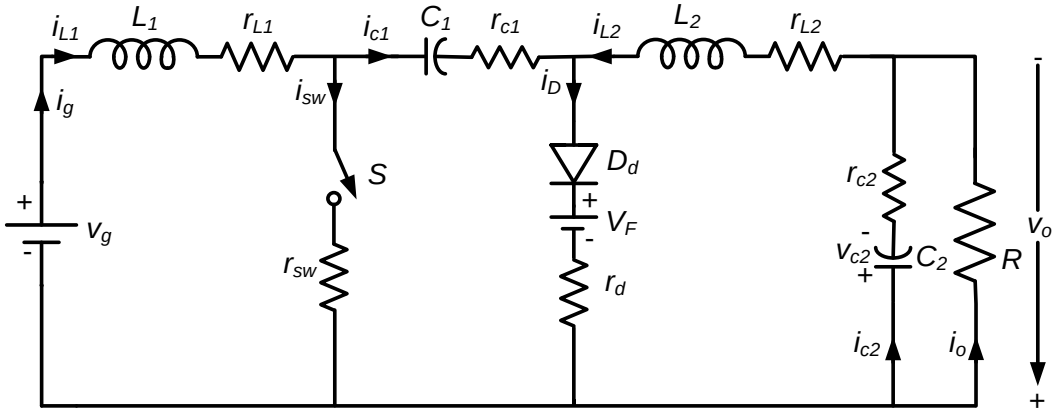


Fig. 3.26. Non-ideal DC-DC Cuk converter

$$i_{c2,rms}=\frac{\Delta i_{L2}}{\sqrt{12}}, i_{sw,rms}=I_o\sqrt{\frac{D}{D'^2}+\frac{D\left(\Delta i_{L1}+\Delta i_{L2}\right)^2}{12I_o^2}}, i_{D,rms}=I_o\sqrt{\frac{1}{D'}+\frac{D'\left(\Delta i_{L1}+\Delta i_{L2}\right)^2}{12I_o^2}} \quad (3.313)$$

Where, $$\Delta i_{L1}=\frac{D'V_o}{L_1 f}\left(1+\frac{V_F}{V_o}+\frac{1}{R}\left(r_{L2}+\frac{D}{D'}r_{c1}+\frac{r_d}{D'}\right)\right), \Delta i_{L2}=\frac{D'V_o}{L_2 f}\left(1+\frac{V_F}{V_o}+\frac{1}{R}\left(r_{L2}+\frac{r_d}{D'}\right)\right)$$

The power loss in different elements of the Cuk converter will be

$$P_L=P_{rL1}+P_{rL2}+P_{rC1}+P_{rC2}+P_{rSw}+P_{rD}+P_{VD}=r_{loss}I_o^2 \quad (3.314)$$

Where,

$$r_{loss}=\left(\frac{D^2r_{L1}}{D'^2}+r_{L2}+\frac{Dr_{c1}}{D'}+\frac{Dr_{sw}+D'r_D}{D'^2}+\frac{RV_F}{V_o}\right)+\left(r_{L1}+D'r_{c1}\right)\frac{\Delta i_{L1}^2}{12I_o^2}+ \left(r_{L2}+Dr_{c1}+r_{c2}\right)\frac{\Delta i_{L2}^2}{12I_o^2}+\left(Dr_{sw}+D'r_D\right)\frac{\left(\Delta i_{L1}+\Delta i_{L2}\right)^2}{12I_o^2} \quad (3.315)$$

r_{loss} is function of duty cycle and switching frequency as well because it depends on the inductor current ripple which is function of the switching frequency.

The energy stored in inductors is

$$W_{L1}=\frac{1}{2}L_1I_{L1}^2=\frac{1}{2}L_1\frac{D^2}{D'^2}I_o^2, \quad W_{L2}=\frac{1}{2}L_2I_{L2}^2=\frac{1}{2}L_2I_o^2$$

$$W_L=W_{L1}+W_{L2}=\frac{1}{2}\left(\frac{L_1D^2}{D'^2}+L_2\right)I_o^2=\frac{1}{2}L_{eq}I_o^2 \text{ , Where } L_{eq}=\left(\frac{L_1D^2}{D'^2}+L_2\right) \quad (3.316)$$

The energy stored in the capacitor is

$$W_{C1}=\frac{1}{2}C_1V_1^2=\frac{1}{2}C_1\left(V_g+V_o\right)^2=\frac{1}{2}C_1\left(\frac{V_o}{M_v}+V_o\right)^2=\frac{1}{2}C_1R^2\left(\frac{M_v+1}{M_v}\right)^2I_o^2$$

$$W_{C2}=\frac{1}{2}C_2V_2^2=\frac{1}{2}C_2V_o^2=\frac{1}{2}C_2R^2I_o^2$$

$$W_C=W_{C1}+W_{C2}=\frac{1}{2}R^2\left[C_1\left(\frac{M_v+1}{M_v}\right)^2+C_2\right]I_o^2=\frac{1}{2}R^2C_{eq}I_o^2 \quad (3.317)$$

Where, $C_{eq}=C_1\left(\frac{M_v+1}{M_v}\right)^2+C_2$

The capacitor-inductor stored energy ratio is

$$CIR = \frac{W_C}{W_L} = \frac{C_{eq}R^2}{L_{eq}} \tag{3.318}$$

The DC current gain is

$$M_i = \frac{I_o}{I_g} = \frac{I_{L2}}{I_{L1}} = \frac{D'}{D} \tag{3.319}$$

Calculation of voltage gain (M_v):

Substituting values from (3.319) into (3.297),

$$M_v = \frac{D/D'}{1+\frac{r_{loss}}{R}} \tag{3.320}$$

***Calculation of time constant (τ)*:**

Substituting values from (3.316) and (3.318) into (3.299), we get

$$\tau = \frac{2\left(\frac{1}{2}L_{eq}I_o^2\right)}{I_o^2\left(R+r_{loss}\right)}\left(1+\frac{C_{eq}R^2}{L_{eq}}\frac{r_{loss}}{R}\right) = \frac{L_{eq}+C_{eq}Rr_{loss}}{R+r_{loss}} \tag{3.321}$$

Calculation of damping time constant (τ_d):

Substituting values from (3.316) and (3.318) into (3.300), we get

$$\tau_d = \frac{2\left(\frac{1}{2}L_{eq}I_o^2\right)}{I_o^2}\left(\frac{\frac{C_{eq}R^2}{L_{eq}}}{R+r_{loss}\frac{C_{eq}R^2}{L_{eq}}}\right) = \frac{C_{eq}RL_{eq}}{L_{eq}+C_{eq}Rr_{loss}} \tag{3.322}$$

From (3.321) and (3.322), it is clear that τ and τ_d are function of loss component r_{loss}, C_{eq} and L_{eq}. As observed from (3.315)-(3.317), r_{loss} is function of duty cycle D and switching frequency f and C_{eq}, L_{eq} are functions of the duty cycle. Consequently, τ and τ_d will also be the function of duty cycle D and switching frequency f. Thus, the statement of [70] is incorrect in case of Cuk converter also, which states that τ and τ_d remain constant with variation in D and f. It is also proved by the simulation results later.

3.5.5 Simulation results

In order to verify the second-order model of non-ideal buck and Cuk converter obtained from energy factor approach, MATLAB simulation is carried out. The step responses of these second-order transfer functions are compared with the step responses of models obtained from state-space averaging technique.

3.5.5.1 Buck converter

For simulation purpose, the buck converter specifications are kept same as shown in Table 3.1. The switching frequency is 10 kHz and duty cycle is 0.75. By substituting these values, the different parameters are calculated as follows-

V_o=11.594 V, I_L=1.054 A, Δi_L=0.284 A, r_{loss}=0.3882 Ω, M_i=1.333, M_v=0.7244, **τ=128.08 µs**, **τ_d=696.79 µs**.

Therefore, from (3.291), the transfer function of buck converter using the energy factor approach is

$$G_{EF}(s)=\frac{8.117\times10^{6}}{s^{2}+1435s+1.12\times10^{7}} \tag{3.323}$$

Rewriting (3.250), the transfer function of buck converter using SSA technique is

$$G_{SSA}(s)=\frac{199.1s+7.901\times10^{6}}{s^{2}+1518s+1.074\times10^{7}} \tag{3.324}$$

For input voltage V_g=16 V, the output voltage step response of buck converter is compared for both the techniques as shown in Fig. 3.27. This comparison shows the transient response and steady-state response is matched closely.

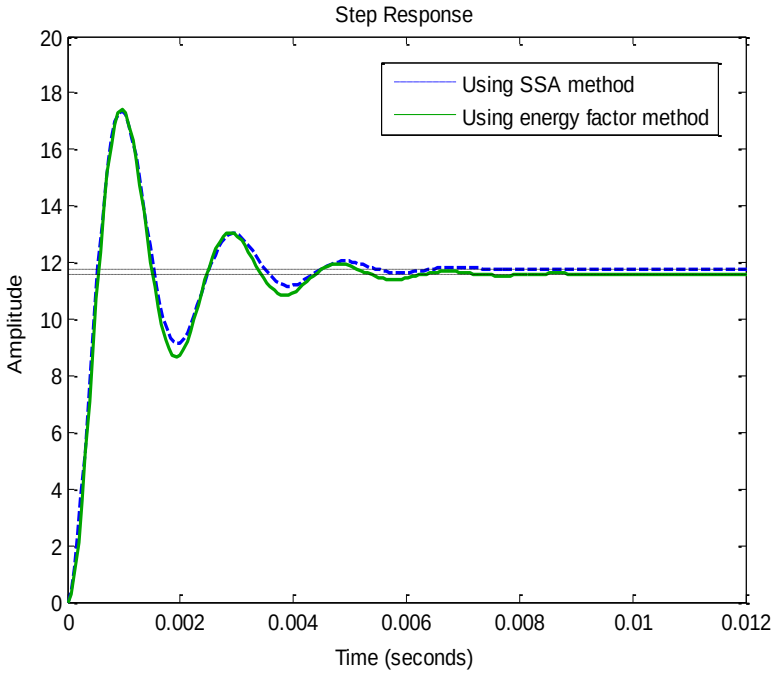


Fig. 3.27. Comparison of output voltage step responses of non-ideal buck converter

Now it is verified that the values of τ and τ_d is not independent of duty cycle and switching frequency. For this purpose, two cases are considered in which these parameters are varied one by one, while keeping other parameters constant.

Case 1: *D is varied from 0.75 to 0.85 keeping other parameters constant*

In this case, the following parameters are obtained:

V_o=13.23 V, I_L=1.202 A, Δi_L=0.193 A, r_{loss}=0.309 Ω, M_i=1.176, M_v=0.8267, **τ=122.54 µs**, **τ_d=733.38 µs**.

Case 2: *f is varied from 10 kHz to 20 kHz keeping other parameters constant*

In this case, the following parameters are obtained:

V_o=11.594 V, I_L=1.054 A, Δi_L=0.1421 A, r_{loss}=0.386 Ω, M_i=1.133, M_v=0.724, **τ=127.92 µs**, **τ_d=697.83** µs.

The values of time constants τ and τ_d for different combinations of duty cycle and switching frequency are compared in Table 3.5. From this table, it is clear that time constants τ and damping time constant τ_d are different for different values of duty cycle and switching frequency. This is because of the power loss variation with duty cycle and frequency as discussed earlier. It is observed that with the increase in duty cycle or switching frequency τ decreases whereas τ_d increases.

Table 3.5. Comparison of time constants τ and damping time constant τ_d for buck converter

Duty cycle (*D*)	Switching frequency (*f*)	Time constant (τ)	Damping time constant (τ_d)
0.75	10 kHz	128.08 µs	696.79 µs
0.85	10 kHz	122.54 µs	733.38 µs
0.75	20 kHz	127.92 µs	697.83 µs

3.5.5.2 Cuk converter

For simulation of Cuk converter, the parameter value is kept same as shown in Table 3.3. The switching frequency is 10 kHz and duty cycle is 0.444. By substituting these values, the different parameters are computed as follows-

V_o=14.42 V, I_{L1}=1.0489 A, I_{L2}=1.3112 A, Δi_{L1}=0.289 A, Δi_{L2}=0.453 A, r_{loss}=1.209 Ω, M_i=1.25, M_v=0.721, **τ=3.378 ms**, **τ_d=2.867 ms**.

Therefore, from (3.291), the transfer function of the Cuk converter using the energy factor approach is

$$G_{EF}(s)=\frac{7.443\times10^4}{s^2+348.8s+1.033\times10^5} \tag{3.325}$$

Rewriting (3.250), the transfer function of buck converter using SSA technique is

$$G_{SSA}(s)=\frac{-628.4s^2-2.369\times10^6 s+2.431\times10^{11}}{s^4+594.2s^3+1.836\times10^6 s^2+3.949\times10^8 s+3.224\times10^{11}} \tag{3.326}$$

For input voltage V_g=20 V, the output voltage step responses from both the transfer functions are compared as shown in Fig. 3.28. This comparison shows the transient response and steady-state responses are almost similar. Therefore, the second-order transfer function obtained from the energy factor approach approximates the characteristics of fourth-order Cuk converter. However, the energy factor approach does not reflect the effect of zeros of Cuk converter, which causes the difference in dynamic response.

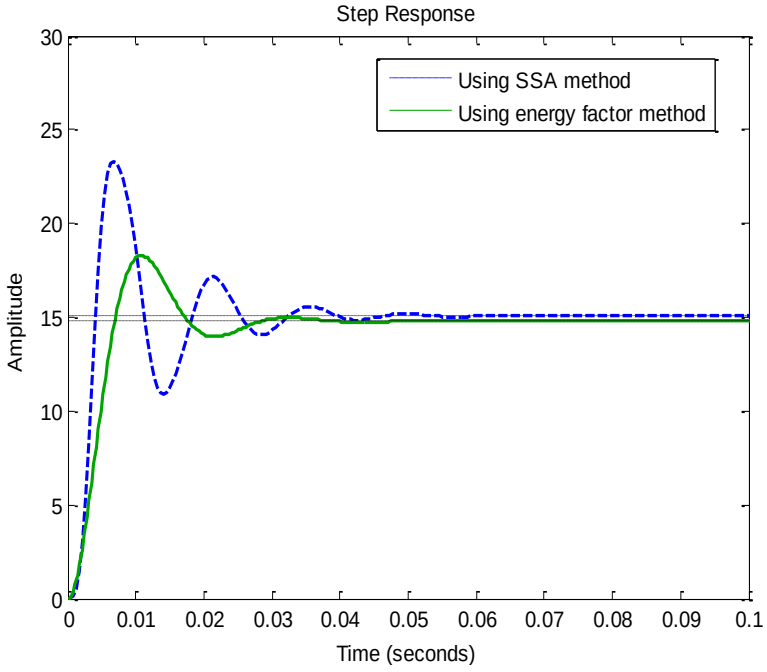


Fig. 3.28. Comparison of output voltage step responses of non-ideal Cuk converter

Further, to validate that the values of τ and τ_d is dependent of duty cycle and switching frequency; two cases are considered in which one by one these parameters are varied while keeping other parameters constant.

Case 1: *D is varied from 0.444 to 0.55 keeping other parameters constant*
In this case, the following parameters are obtained:
V_o=21.62 V, I_{L1}=2.42 A, I_{L2}=1.96 A, Δi_{L1}=0.347 A, Δi_{L2}=0.542 A, r_{loss}=1.44 Ω, M_i=0.81, M_v=1.08, **τ=3.031 ms**, **τ_d=3.378 ms**.

Case 2: *f is varied from 10 kHz to 20 kHz keeping other parameters constant*
In this case, the following parameters are obtained:
V_o=14.42 V, I_{L1}=1.0489 A, I_{L2}=1.3112 A, Δi_{L1}=0.145 A, Δi_{L2}=0.226 A, r_{loss}=1.204 Ω, M_i=1.25, M_v=0.721, **τ=3.365 ms**, **τ_d=2.873 ms**.

The values of time constants τ and τ_d for different combinations of duty cycle and switching frequency are compared in Table 3.6. From this table, it may be observed that time constants τ and damping time constant τ_d are different for different values of duty cycle and switching frequency. This is because of the different value of power loss due to variation in duty cycle and frequency. Similar to buck converter, for Cuk converter also, it is seen that with the increase in duty cycle or switching frequency τ decreases, whereas τ_d increases.

Table 3.6. Comparison of time constants τ and damping time constant τ_d for Cuk converter

Duty cycle (*D*)	Switching frequency (*f*)	Time constant (τ)	Damping time constant (τ_d)
0.44	10 kHz	3.378 ms	2.867 ms
0.55	10 kHz	3.031 ms	3.378 ms
0.44	20 kHz	3.365 ms	2.873 ms

3.6 Conclusion

In this chapter, the mathematical modeling of non-ideal DC-DC buck and Cuk converter have been carried out. First, the generalized state-space averaging technique was discussed involving the additional constant vector to involve the effect of diode forward voltage drop. This SSA technique was used to obtain the improved model of the non-ideal DC-DC buck and Cuk converters. Then, the averaged switch model technique was discussed. The improved transfer functions for the non-ideal buck and Cuk converters have been obtained including all the non-idealities using these two methods. The transfer functions obtained by both the methods are identical. The improved transfer functions give more accurate steady-state and transient behaviour of the converters. The results show that with the ideal assumptions, duty cycle to output voltage transfer functions of Cuk converter is non-minimum phase system, whereas it is found to be a minimum phase system with the substitution of all non-idealities. However, depending upon the values of non-ideal elements, it may be minimum phase or non-minimum phase but in ideal case, it is always non-minimum phase. Therefore, the obtained improved transfer functions are very useful from controller design point of view. Further, the concept of the energy factor approach has also been discussed in detail. The transfer functions of the non-ideal buck and Cuk converter were obtained. It was proven that if the non-idealities are included, the transfer functions depend upon switching frequency and duty cycle in contrast to the theory given by the original author.

CHAPTER 4: CONTROL OF DC-DC CONVERTERS

[In this chapter, the design of the various control techniques for DC-DC buck and Cuk converter are discussed. The experimental and simulation results are presented to validate the performance of these controller techniques.]

4.1 Introduction

In the previous chapter, the mathematical modeling of non-ideal DC-DC buck and Cuk converter has been discussed. Now the next step is to design a suitable controller to regulate the output voltage of these converters in various operating conditions. In DC-DC converter applications, the DC input voltage supply and load current may vary due to various reasons. However, it is always desirable to maintain a constant output voltage despite of these input and load variations. When there are any unusual variations in input voltage or in load current requirements, the output voltage of the DC-DC converter deviates from its desired value. Therefore, it is mandatory to introduce an additional component, which can bring the output voltage back to the desired value as quickly as possible. It arises a need of suitable closed-loop control of DC-DC converter, which automatically adjusts the duty cycle to regulate the output voltage in the presence of such variations.

Therefore, in general, a control design for DC-DC converter should meet the following requirements [1], [3], [132]:

- Better line and load regulation *i.e.*, the output voltage should remain constant in the presence of input voltage and load current variations.
- Good voltage regulation in case of set point (reference output voltage) change.
- Better transient and steady-state performance.
- Should remain stable in all operating conditions.

In the literature, to improve the dynamic and steady-state response of DC-DC converters, several linear and non-linear control methods have been reported such as PI/PID controller, lag compensator, lead compensator, lag-lead compensator, pole-placement technique, fuzzy controller, genetic algorithm based controller, sliding mode controller, H-infinity controller, *etc* [82], [83], [133]–[140]. These control techniques have its own advantages and disadvantages [90], [141], [142]. For example, a nonlinear hysteretic PWM controller is designed for DC-DC buck converter [143]. It responds faster to sudden load changes, but is subjected to variable switching frequency and unpredictable noise spectrum. On the other hand, PI controllers are simple in structure but they are unable to regulate the output voltage in case of large variations in operating conditions [144]. Therefore, to further improve the performance of the DC-DC converters under large variations in input and load conditions, two-loop control schemes have been suggested [91], [97], [145]–[149]. In research paper [148], a cascaded control of DC-DC buck converter using PI controller has

been presented. It shows the effectiveness of two-loop control against line and load disturbances. However, they have not considered the equivalent series resistance (ESR) of inductor and capacitor in controller design, which affects the transient response of compensated system [150]. A fixed-frequency hysteretic current (FFHC) has been proposed to improve stability and dynamic behaviour of a DC-DC buck converter [149], however, it involves the complex mathematics.

The PI/PID controllers are extensively used for industrial applications. The many methods have been suggested to tune the parameters of these controllers [78], [151]–[156]. Since the converter switching frequency plays an important role in operation of DC-DC converters, the controller design in the frequency domain is much better than the time domain design. For DC-DC converters phase margin (PM) and bandwidth (or gain crossover frequency, GCF) are the important frequency domain measures ,which are used to indicate the performance and robustness against disturbances [3], [157]. Therefore, it is better to design a controller based on the frequency domain measures. In DC-DC converter applications, larger phase margin and higher bandwidth are desirable to ensure better stability and fast transient response against disturbances, respectively. The larger phase margin results in smaller overshoots but longer rise time and settling time, while higher bandwidth speeds up the response of system but also increases noise susceptibility [158]. Therefore, a compromise has to be made while selecting phase margin and bandwidth. For DC-DC converters, phase margin greater than 60º and bandwidth up to one-fourth of the switching frequency are considered good for line and load disturbances rejection [3], [159], [160]. Several analytical methods have been proposed in control literature for PI/PID controller design satisfying the specified gain and phase margin constraints [161]–[168].

The Cuk converter is a fourth-order system. Therefore, in order to simplify the control design problem, a lower-order model of the Cuk converter can be obtained. In the literature, several model-order reduction techniques have been reported to obtain the lower-order or reduced-order model of a higher-order system. The popular model-order reduction methods are truncation method, Pade approximation method, Routh stability criteria, Routh stability equation method, differentiation method, *etc* [106]–[109], [169]–[177]. These methods have its own advantages and disadvantages when applied to a higher-order system. The reduced-order model approximates the original characteristics of the full order system. The model-order reduction techniques have been used to obtain the second-order model of the DC-DC Cuk converter in [178] and a controller has been designed for the Cuk converter using its reduced-order model in [179]. However, these papers have not reported the experimental results to validate the converter performance. Therefore, in this chapter, the reduced-order model of DC-DC Cuk converter is obtained to design a suitable PI controller based on stability boundary locus. The performance of the Cuk converter is validated experimentally.

Pulse width modulator

In order to monitor the duty cycle of the switch, the pulse width modulator (PWM modulator) block will frequently be used in this chapter. Therefore, in this section, the basic function of this block is discussed [1], [3]. The PWM modulator is shown in Fig. 4.1(a). The input to this block is control signal $v_c(t)$, which is generated by the a suitable controller designed for the DC-DC converter. This control signal is compared in a comparator with a sawtooth waveform $v_{sw}(t)$. The sawtooth waveform has fixed switching frequency f_s and peak-to-peak magnitude V_{sw}. The sawtooth waveform frequency is set equal to the converter switching frequency. When the magnitude of the control signal is higher than the magnitude of sawtooth waveform, the comparator output is high; otherwise, the comparator output is low. The typical waveforms are shown in Fig. 4.1(b). The comparator output is periodic switching pulses of duty cycle $d(t)$. The duty cycle of the switching pulses is defined as:

$$d(t) = \frac{v_c(t)}{V_{sw}} \tag{4.1}$$

Therefore, the mathematical model of the pulse width modulator can be described as:

$$\frac{d(t)}{v_c(t)} = \frac{1}{V_{sw}} \tag{4.2}$$

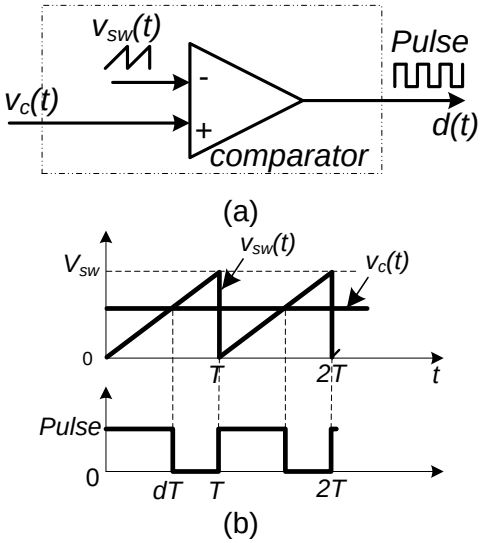


Fig. 4.1. (a) Pulse width modulator circuit (b) corresponding waveforms

In this chapter, first the algorithm for designing PI, PI-lead and two-loop PI controllers are discussed and then these algorithms are implemented on the DC-DC buck and Cuk converters. The performances of the control techniques are investigated using simulation and experimental results. This chapter is divided into two major sections as follows:

- Control of buck converter
- Control of Cuk converter

4.2 Control of DC-DC Buck Converter

In this section, three different control techniques are presented to regulate the DC output voltage of buck converter. The simulation and experimental results are obtained under different working conditions. This section is divided into following subsections.

4.2.1 PI controller design

4.2.2 PI-lead controller design

4.2.3 Two-loop PI controller design

4.2.4 Performance comparison of different control techniques for buck converter

4.2.1 PI controller design

The design and mathematical modeling of DC-DC buck converter has been discussed in detail in the previous chapters. In this section, the closed-loop control of DC-DC buck converter using a PI controller is carried out in order to regulate the DC output voltage of the converter. There are many techniques available in the literature to tune the parameters of the PI controller based on the desired performance. However, in this thesis, the stability boundary locus approach [161] is used to tune the parameter of the PI controller for DC-DC buck and Cuk converter. This approach is very helpful in tuning of PI controller parameters based on desired gain margin and phase margin. As the gain margin of the DC-DC buck converter and Cuk converter under consideration is infinite (very large), therefore, the improvement of phase margin is more important. In view of this, first the generalized algorithm is discussed for obtaining the PI controller parameters for desired gain margin and phase margin using stability boundary locus approach.

Stability boundary locus method

The stability boundary locus method was proposed by N. Tan *et.al.* in 2006 [161] for the computation of PI controller parameters K_p and K_i. This method gives a family of all stabilizing PI controllers. In this method, a global stability region is obtained in K_P-K_i plane by the intersection of the real root boundary (RRB) and the complex root boundary (CRB) [180]. The real root boundary (RRB) is the boundary line at which a real root of the closed-loop characteristic equation crosses the imaginary axis at s=0. The complex root boundary is the boundary line at which complex roots of the closed-loop characteristic equation crosses over the imaginary axis at $s=j\omega$. The RRB and CRB divide the entire parameter plane (K_P-K_i plane) into stable and unstable regions. The stable boundary region can be found by choosing a test point within each region. Any pair of K_P-K_i value within this stable region would stabilize the closed-loop system. Further, this method was also extended to compute the PI parameters based on desired gain margin and phase margin. The stability region obtained based on the desired phase margin and gain margin is a subset of the global

stability region. In [181], this method has been used for PI controller design of PWM DC-DC buck converter, however, experimental validation has not been reported. In this chapter, this method has been used for designing PI controller parameters for both DC-DC buck and Cuk converters and further hardware implementation has been given.

4.2.1.1 Algorithm for tuning PI controller using stability boundary locus approach

The DC-DC buck converter is a second-order system and Cuk converter is a fourth-order system. In this chapter, a PI controller is designed for closed-loop control of both the converter. Therefore, the PI control algorithm is discussed in general for a fourth-order converter system. It is used later for buck converter and Cuk converter both. Fig 4.2 shows the block diagram of closed-loop control of a DC-DC converter using PI controller.

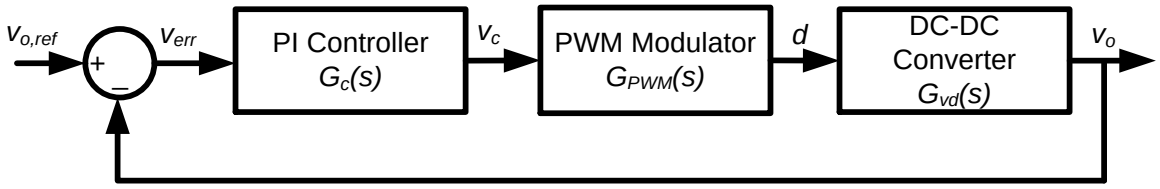


Fig. 4.2. Block diagram of closed-loop PI control of DC-DC converter

Step 1: Let the duty cycle to output voltage transfer functions of DC-DC converter and PWM Modulator are

$$G_{vd}(s)=\frac{\tilde{v}_o(s)}{\tilde{d}(s)}=\frac{b_3s^3+b_2s^2+b_1s+b_0}{a_4s^4+a_3s^3+a_2s^2+a_1s+a_0} \tag{4.3}$$

$$G_{PWM}(s)=\frac{1}{V_{sw}} \tag{4.4}$$

In this design, sawtooth peak voltage $V_{sw}=1$ is taken.

Therefore, the loop transfer function of uncompensated system will be

$$G(s)=G_{PWM}(s)G_{vd}(s)=\frac{b_3s^3+b_2s^2+b_1s+b_0}{a_4s^4+a_3s^3+a_2s^2+a_1s+a_0} \tag{4.5}$$

Now to improve the phase margin and steady-state performance of this converter, a PI controller is designed whose transfer function is

$$G_c(s)=\left(K_p+\frac{K_i}{s}\right) \tag{4.6}$$

Where, K_p and K_i are parameters of PI controller.

Step 2: Specify the desired phase margin φ (in degree) and gain margin A.

In order to satisfy these frequency domain specifications, the characteristic equation of closed-loop DC-DC converter system is given as

$$1+Ae^{-j\varphi}G(s)G_c(s)=0 \tag{4.7}$$

Step 3: Substituting (4.5) and (4.6) into (4.7) and replacing $s=j\omega$, we get

$$1+A(\cos\varphi - j\sin\varphi)\left(\frac{-b_3 j\omega^3 - b_2\omega^2 + b_1 j\omega + b_0}{a_4\omega^4 - a_3 j\omega^3 - a_2\omega^2 + a_1 j\omega + a_0}\right)\left(\frac{K_p j\omega + K_i}{j\omega}\right) = 0$$

$$\Rightarrow \left(K_p \cdot \mathrm{Re}_1 + K_i \cdot \mathrm{Re}_2 + \mathrm{Re}_3\right) + j\left(K_p \cdot \mathrm{Im}_1 + K_i \cdot \mathrm{Im}_2 + \mathrm{Im}_3\right) = 0 \tag{4.8}$$

Where,

$$\begin{aligned}
&\mathrm{Re}_1 = A\left[-\omega^2\left(-b_3\omega^2 + b_1\right)\cos\varphi + \omega\left(-b_2\omega^2 + b_0\right)\sin\varphi\right] \\
&\mathrm{Re}_2 = A\left[\left(-b_2\omega^2 + b_0\right)\cos\varphi + \omega\left(-b_3\omega^2 + b_1\right)\sin\varphi\right], \mathrm{Re}_3 = -\omega^2\left(-a_3\omega^2 + a_1\right) \\
&\mathrm{Im}_1 = A\left[\omega^2\left(-b_3\omega^2 + b_1\right)\sin\varphi + \omega\left(-b_2\omega^2 + b_0\right)\cos\varphi\right] \\
&\mathrm{Im}_2 = A\left[-\left(-b_2\omega^2 + b_0\right)\sin\varphi + \omega\left(-b_3\omega^2 + b_1\right)\cos\varphi\right], \mathrm{Im}_3 = \omega\left(a_4\omega^4 - a_2\omega^2 + a_0\right)
\end{aligned} \tag{4.9}$$

Separating real and imaginary parts, we get two equations

$$K_p \cdot \mathrm{Re}_1 + K_i \cdot \mathrm{Re}_2 + \mathrm{Re}_3 = 0 \tag{4.10}$$

$$K_p \cdot \mathrm{Im}_1 + K_i \cdot \mathrm{Im}_2 + \mathrm{Im}_3 = 0 \tag{4.11}$$

Simplifying these equations for K_p and K_i gives

$$K_p(\omega, A, \varphi) = \frac{\left(q_7 \sin\varphi\omega^7 + q_6\cos\varphi\omega^6 + q_5\sin\varphi\omega^5 + q_4\cos\varphi\omega^4 + q_3\sin\varphi\omega^3 + q_2\cos\varphi\omega^2 + q_1\sin\varphi\omega + q_0\cos\varphi\right)}{-A\left(p_6\omega^6 + p_4\omega^4 + p_2\omega^2 + p_0\right)} \tag{4.12}$$

$$K_i(\omega, A, \varphi) = \frac{\omega\left(q_7\cos\varphi\omega^7 - q_6\sin\varphi\omega^6 + q_5\cos\varphi\omega^5 - q_4\sin\varphi\omega^4 + q_3\cos\varphi\omega^3 - q_2\sin\varphi\omega^2 + q_1\cos\varphi\omega - q_0\sin\varphi\right)}{-A\left(p_6\omega^6 + p_4\omega^4 + p_2\omega^2 + p_0\right)} \tag{4.13}$$

Where,

$$\begin{aligned}
&q_7 = -a_4 b_3, q_6 = -a_4 b_2 + a_3 b_3, q_5 = a_4 b_1 - a_3 b_2 + a_2 b_3, q_4 = a_4 b_0 - a_3 b_1 + a_2 b_2 - a_1 b_3, \\
&q_3 = a_3 b_0 - a_2 b_1 + a_1 b_2 - a_0 b_3, q_2 = -a_2 b_0 + a_1 b_1 - a_0 b_2, q_1 = -a_1 b_0 + a_0 b_1, q_0 = a_0 b_0 \\
&p_6 = b_3^2, p_4 = b_2^2 - 2b_1 b_3, p_2 = b_1^2 - 2b_0 b_2, p_0 = b_0^2
\end{aligned}$$

Step 4: Now by solving these two equations simultaneously at different value of 'ω', the stability boundary locus in K_p-K_i plane is obtained.

To obtain the stability boundary locus for desired gain margin A, we substitute $\varphi=0$ in (4.12) and (4.13). Thus, we get

$$K_p(\omega, A) = \frac{\left(q_6\omega^6 + q_4\omega^4 + q_2\omega^2 + q_0\right)}{-A\left(p_6\omega^6 + p_4\omega^4 + p_2\omega^2 + p_0\right)} \tag{4.14}$$

$$K_i(\omega, A) = \frac{\omega\left(q_7\omega^7 + q_5\omega^5 q_3\omega^3 + q_1\omega\right)}{-A\left(p_6\omega^6 + p_4\omega^4 + p_2\omega^2 + p_0\right)} \tag{4.15}$$

By solving these equations, we get the stability boundary locus for desired gain margin.

Similarly, to obtain the stability boundary locus for desire phase margin φ, we substitute $A=1$ in (4.12)-(4.13). Thus, we get

$$K_p(\omega, \varphi) = \frac{\begin{pmatrix} q_7\sin\varphi\omega^7 + q_6\cos\varphi\omega^6 + q_5\sin\varphi\omega^5 + q_4\cos\varphi\omega^4 + q_3\sin\varphi\omega^3 \\ +q_2\cos\varphi\omega^2 + q_1\sin\varphi\omega + q_0\cos\varphi \end{pmatrix}}{-\left(p_6\omega^6 + p_4\omega^4 + p_2\omega^2 + p_0\right)} \tag{4.16}$$

$$K_i(\omega,\varphi)=\frac{\omega\begin{pmatrix} q_7\cos\varphi\omega^7-q_6\sin\varphi\omega^6+q_5\cos\varphi\omega^5-q_4\sin\varphi\omega^4+q_3\cos\varphi\omega^3 \\ -q_2\sin\varphi\omega^2+q_1\cos\varphi\omega-q_0\sin\varphi \end{pmatrix}}{-\left(p_6\omega^6+p_4\omega^4+p_2\omega^2+p_0\right)} \tag{4.17}$$

By solving these two equations, the stability boundary locus for desired phase margin is obtained. The interaction of these two boundaries locus gives the desired stability region in K_p-K_i plane, which guarantees the specified phase margin and gain margin. Any combination of K_p and K_i selected within this stability region guarantees the gain margin and phase margin which is greater than or equal to the specified margins. For the DC-DC converters, normally gain margin is high or infinite. Therefore, only one stability boundary locus may be sufficient to ensure the desired phase margin.

4.2.1.2 PI controller design for DC-DC buck converter

The block diagram of closed-loop PI control of a DC-DC buck converter is shown in Fig. 4.3. The actual output voltage (v_o) is compared with the reference output voltage ($v_{o,ref}$) and then, the resultant voltage error is processed via PI controller $G_c(s)$. The output of the PI controller is control voltage v_c, which is compared with a sawtooth signal of fixed peak and frequency. The output of this comparison is obtained in the form of the switching pulses of desired duty cycle d in order to regulate the output voltage of the buck converter. The detailed schematic of this control scheme for buck converter is shown in Fig. 4.4.

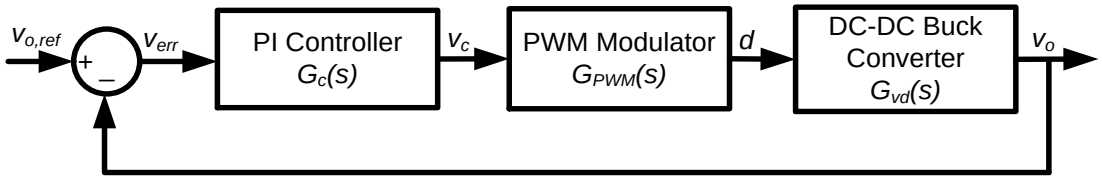


Fig. 4.3. Block diagram of closed-loop control of buck converter using PI controller

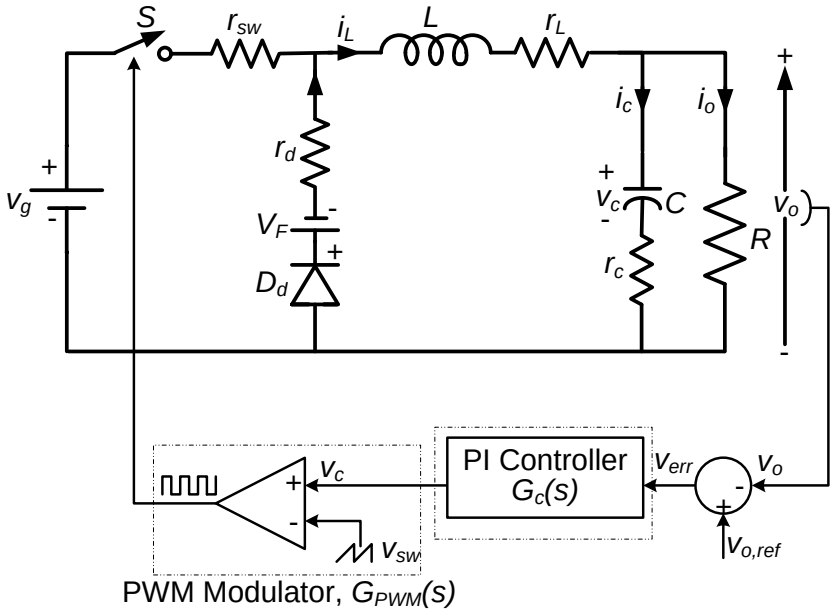


Fig. 4.4. Detailed schematic of PI controlled DC-DC buck converter

Table 4.1. DC-DC buck converter specifications

Parameters	**Value**
Input voltage, V_g	16-24 V
Output voltage, V_o	12 V
Load resistance, R	11-22 Ω
Inductance, L/r_L	1.1 mH/0.18 Ω
Capacitance, C/r_c	84 μF/0.3 Ω
Switch-on resistance, r_{sw}	0.044 Ω
Diode forward resistance, r_{dw}	0.024 Ω
Diode forward voltage, V_F	0.7 V
Switching frequency, f	20 kHz
Sawtooth peak, V_{sw}	1

The parameters of the buck converter under consideration are given in Table 4.1. These parameters are same as used for its modeling in chapter 3. The input voltage and load resistance are considered to vary in the given range. In this chapter, the mathematical model used for controller design is derived by assuming that the buck converter is operating at minimum input voltage and maximum load current.

The derivation of duty-cycle to output-voltage transfer function has been carried out in (3.254) of the previous chapter. Thus, substituting V_g=16 V and R=11 Ω and other buck converter parameters, we get

$$G_{vd}(s)=\frac{\tilde{v}_o(s)}{\tilde{d}(s)}=\frac{4428s+1.757\times10^8}{s^2+1518s+1.074\times10^7} \tag{4.18}$$

The uncompensated loop transfer function of buck converter will be

$$T(s)=G_{PWM}(s)G_{vd}(s)=\frac{1}{V_{sw}}G_{vd}(s)=\frac{4428s+1.757\times10^8}{s^2+1518s+1.074\times10^7} \tag{4.19}$$

The frequency response of the uncompensated buck converter is shown in Fig. 4.5. It shows that the gain margin is infinite and phase margin is 26° at a gain crossover frequency of 2.23 kHz. This phase margin is not sufficient as it results in poor transient response with larger overshoots. Moreover, the gain of the uncompensated converter at low frequencies is constant, which gives steady-state error for any step disturbance in the system. The steady-state error for step disturbance occurs because uncompensated system is a type-0 system.

To improve the phase margin of the system, the gain crossover frequency can be shifted to a low value and to eliminate the steady-state error, a single pole at the origin can be added. To accomplish both these tasks, a PI controller is designed. The PI controller is designed using the stability boundary locus approach discussed in the previous section.

By comparing (4.19) with (4.5), we get

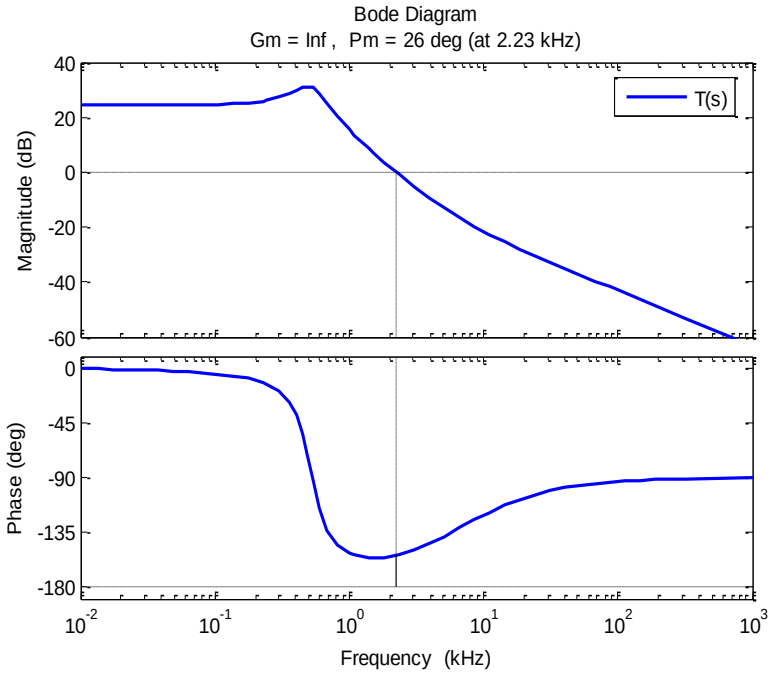


Fig. 4.5. Frequency response of uncompensated DC-DC buck converter

$$b_3 = 0, b_2 = 0, b_1 = 4428, b_0 = 1.757 \times 10^8, a_4 = 0, a_3 = 0, a_2 = 1, a_1 = 1518, a_0 = 1.074 \times 10^7 \quad (4.20)$$

Substituting these coefficients in (4.12) and (4.13), we get

$$K_p(\omega, \varphi) = \frac{\left(-4428 \sin\varphi\omega^3 - 1.69 \times 10^8 \cos\varphi\omega^2 - 2.19 \times 10^{11} \sin\varphi\omega + 1.88 \times 10^{15} \cos\varphi\right)}{-A\left(1.96 \times 10^7 \omega^2 + 3.08 \times 10^{16}\right)} \quad (4.21)$$

$$K_i(\omega, \varphi) = \frac{\omega\left(-4428 \cos\varphi\omega^3 + 1.69 \times 10^8 \sin\varphi\omega^2 - 2.19 \times 10^{11} \cos\varphi\omega - 1.88 \times 10^{15} \sin\varphi\right)}{-A\left(1.96 \times 10^7 \omega^2 + 3.08 \times 10^{16}\right)} \quad (4.22)$$

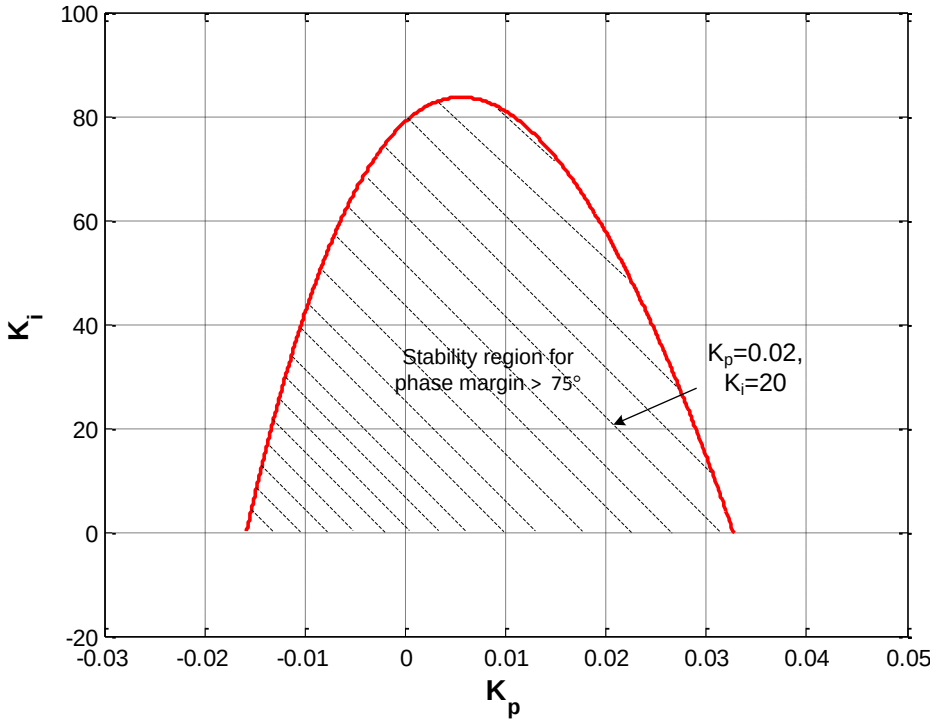


Fig. 4.6. Stability boundary locus for DC-DC buck converter

As the gain margin of the system is infinite, therefore, the PI controller parameters are designed to improve the phase margin of the closed-loop system. Let the desired phase margin of the compensated system is 75°. Therefore, by substituting A=1 and φ=75° in (4.21) -(4.22) and then varying ω, the stability boundary locus in K_p-K_i plane is obtained as shown in Fig. 4.6. The any combination of K_p and K_i within this stability region will give the phase margin greater than or equal to 75°. We select K_p=0.02 and K_i=20. With these values, the PI controller transfer function is

$$G_c(s) = \frac{0.02s + 20}{s} \tag{4.23}$$

Therefore, the loop transfer function of compensated buck converter is

$$G_c(s)T(s) = \left(\frac{0.02s + 20}{s}\right) \cdot \left(\frac{4428s + 1.757 \times 10^8}{s^2 + 1518s + 1.074 \times 10^7}\right) \tag{4.24}$$

The frequency response of the compensated buck converter is shown in Fig. 4.7. As seen from the figure, the phase margin of the closed-loop buck converter has been increased to 107° but gain crossover frequency is decreased to 55.8 Hz. The increased phase margin reduces the overshoot, but the decreased crossover frequency makes the speed of response sluggish. The gain at low frequencies is now having -20 dB/decade slope which will help in eliminating the steady-state error.

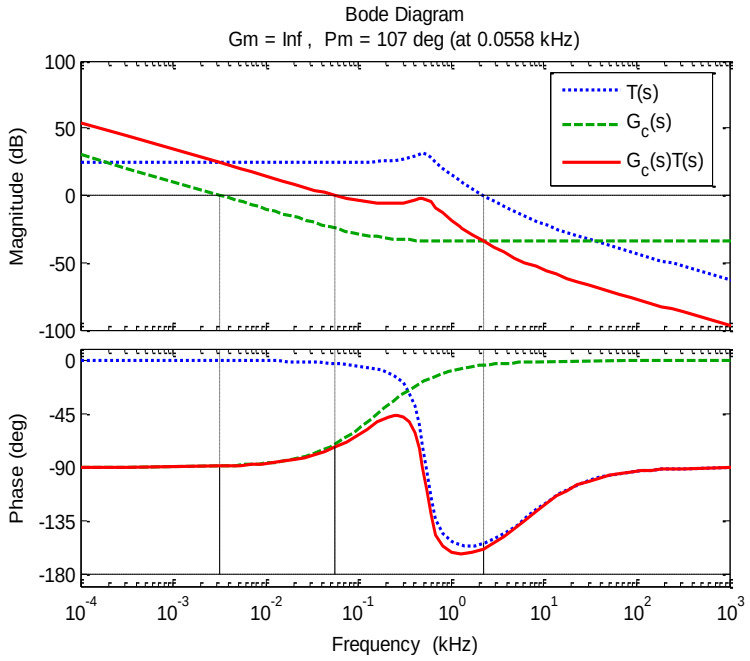


Fig. 4.7. Frequency response of PI controlled DC-DC buck converter

4.2.1.3 Results and discussion

In order to verify the performance of the PI controller designed in (4.23), the simulation and experimental results have been obtained for closed-loop DC-DC buck converter. The buck converter parameters for simulation and experimental results are same as given in Table 4.1. The simulation results are obtained using MATLAB/Simulink software. The PI controller is implemented on buck converter prototype using dSPACE controller. The detailed

description for the development of experimental setup has been given separately in Appendix *B*. The simulation and experimental results are compared and analysed for three different conditions:

(a) Variation in reference output voltage

(b) Variation in input voltage

(c) Variation in load current

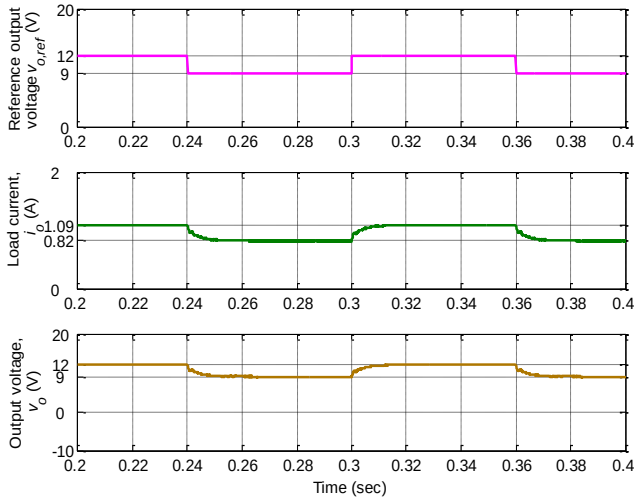
(a) Variation in reference output voltage

The performance of the PI controller designed for buck converter is observed for step change in reference output voltage ($V_{o,ref}$). The input voltage (V_g) and load resistance (R) are kept constant to 16 V and 11 Ω, respectively. For reference voltage variation from 12 V to 9 V and vice-versa, the simulation and experimental results are shown in Fig. 4.8 (a), whereas for reference voltage variation from 12 V to 15 V and vice-versa, the corresponding simulation and experimental results are shown in Fig. 4.8 (b). It is observed that in both the cases, the output voltage reaches to the new desired value within 15-20 ms without any overshoot and oscillations. The load current also varies according to new desired output voltage because load resistance is kept constant (11 Ω). The load current is 0.82 A, 1.09 A and 1.36 A for desired output voltage 9 V, 12 V and 15 V, respectively. It is verified that the simulation and experimental results match well.

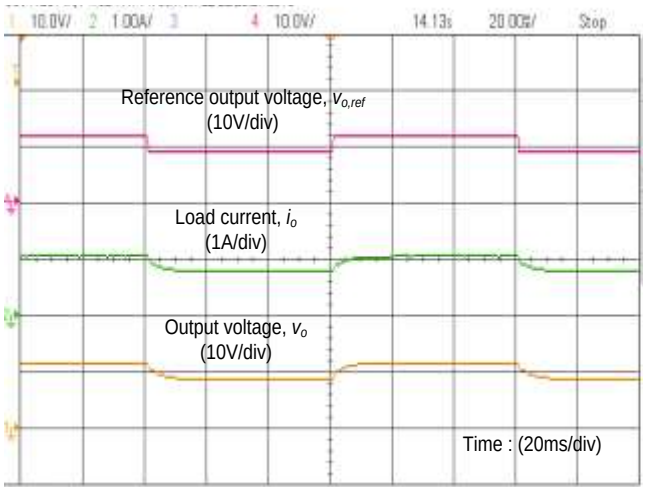
(b) Variation in input voltage

The simulation and experimental results are obtained for step variation in input voltage while keeping the load conditions constant. The variation in input voltage (V_g) is considered from minimum (16 V) to maximum (24 V) and vice-versa for two extreme load conditions R=11 Ω (*i.e.,* maximum load current, 1.09 A) and R=22 Ω (*i.e.,* minimum load current, 0.54 A). The desired output voltage is 12 V.

In the first case, the load is fixed at 11 Ω and the input voltage varies from 16 V to 24 V (Fig. 4.9 (a)) and 24 V to 16 V (Fig. 4.9 (b)). In the second case, the load is fixed at 22 Ω and the input voltage varies from 16 V to 24 V (Fig. 4.10(a)) and 24 V to 16 V (Fig. 4.10(b)). These results indicate that when the input voltage is increased from 16 V to 24 V, the output voltage settles back to steady-state (12 V) within 15 ms. However, during transients, the output voltage faces large oscillations and overshoot of 6 V. Similarly, when the input voltage is decreased from 24 V to 16 V, the output voltage sets within 20 ms. It has large oscillations and undershoot of 3.5 V - 4.5 V. The experimental results also validate the simulation results. In the experimental results, the step change in input voltage was realized using a manual switch. So, during the initial part of the transition period, there is a dip in the input voltage before reaching to new input voltage. Therefore, the initial part of transients in the experimental output voltage is ignored while comparing with the simulation.

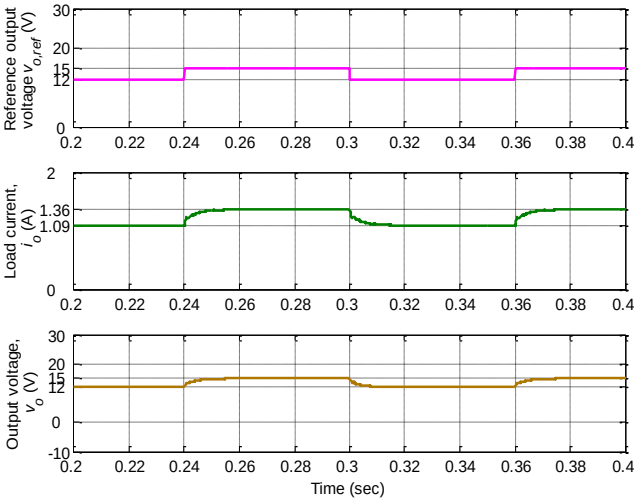


Simulation

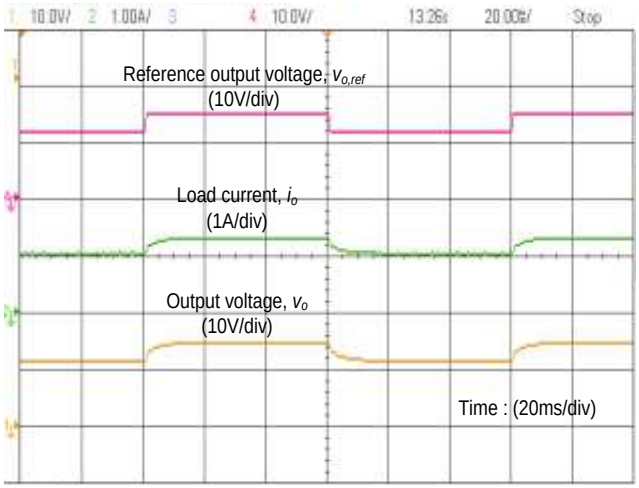


Experimental

(a)



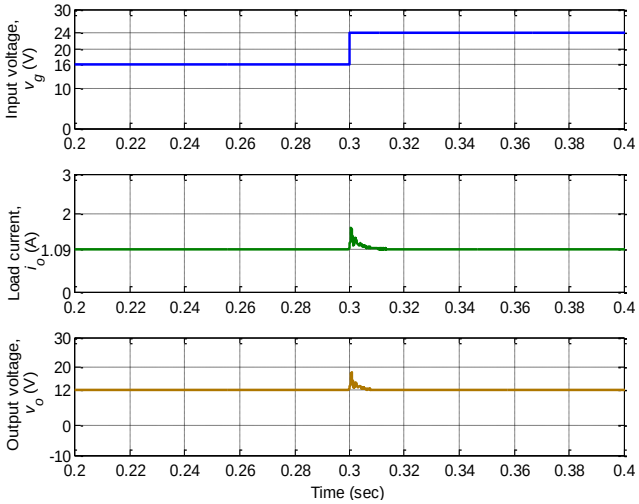
Simulation



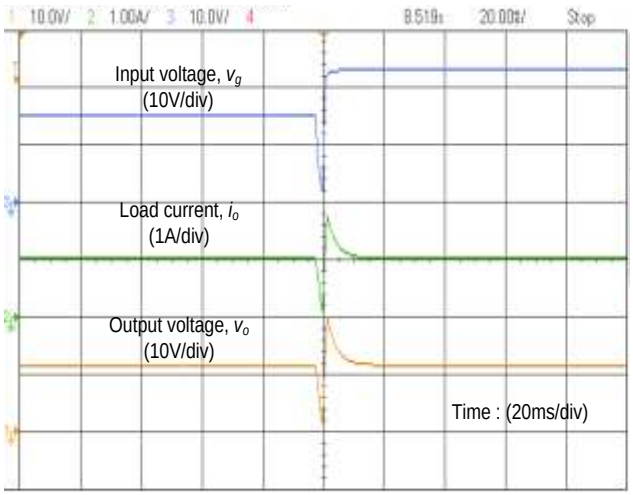
Experimental

(b)

Fig. 4.8. Simulation and experimental results for reference output voltage variation from (a) 12 V to 9 V and vice-versa (b) 12 V to 15 V and vice-versa

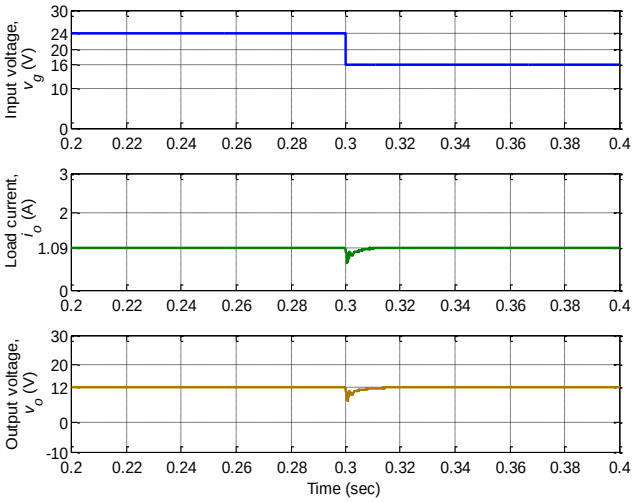


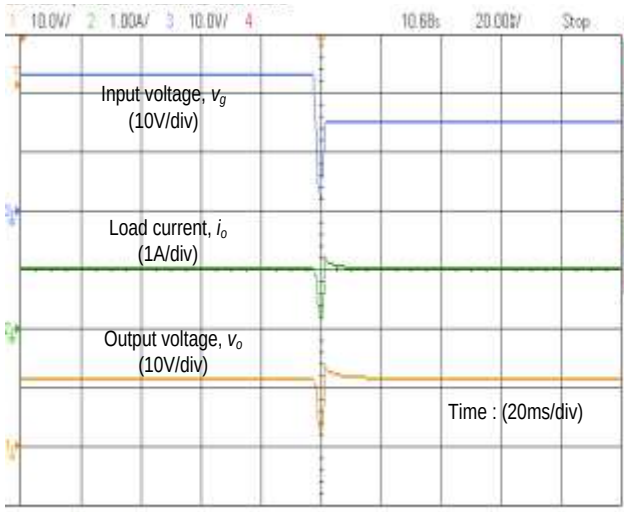
Simulation



Experimental

(a)

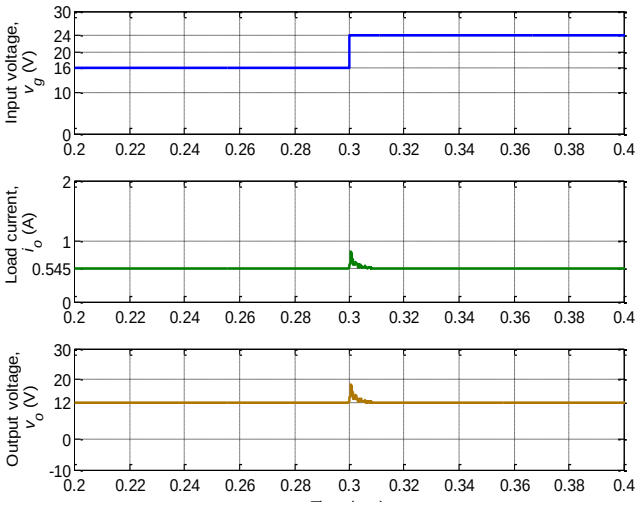


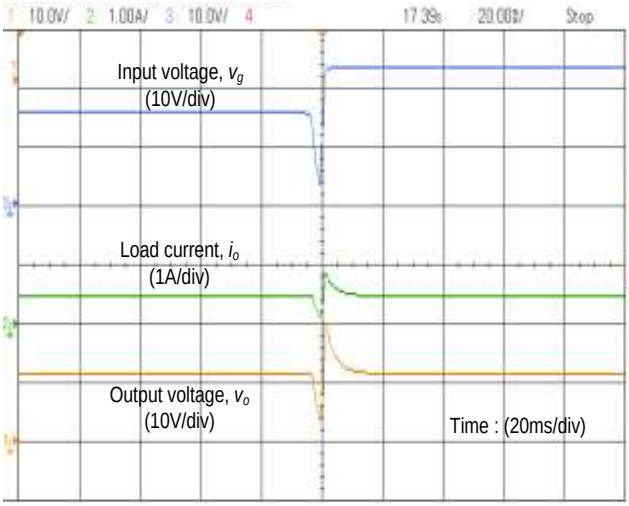


Simulation Experimental

(b)

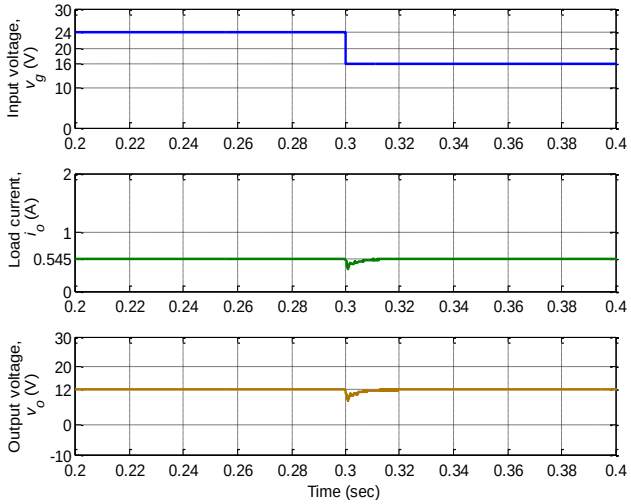
Fig. 4.9. Simulation and experimental results with R=11 Ω for input voltage variation from (a) 16 V to 24 V (b) 24 V to 16 V

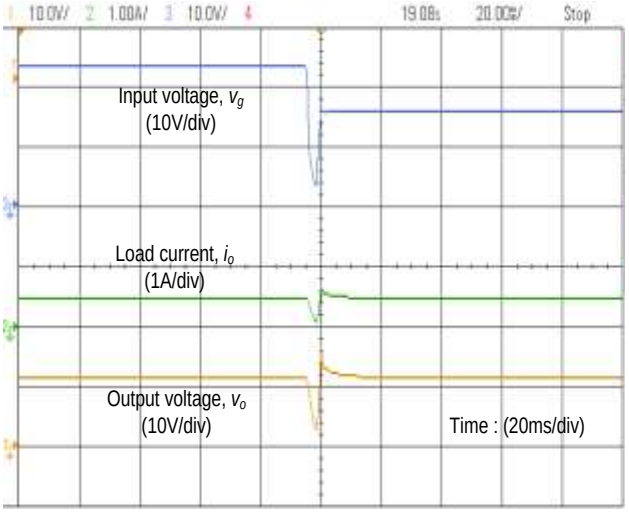




Simulation Experimental

(a)





Simulation Experimental

(b)

Fig. 4.10. Simulation and experimental results with R=22 Ω for input voltage variation from (a) 16 V to 24 V (b) 24 V to 16 V

(c) Variation in load resistance or load current

The performance of the closed-loop buck converter is also observed for variations in load conditions while keeping the input voltage constant. The load resistance (R) is varied from 22 Ω (*i.e.,* minimum load current, 0.54 A) to 11 Ω (*i.e.,* maximum load current, 1.09 A) and vice-versa for two extreme input voltages V_g=16 V (minimum) and V_g=24 V (maximum). The desired output voltage is 12 V. Fig. 4.11(a) shows the simulation and experimental results for step variation in load resistance from 22 Ω to 11 Ω and vice-versa at fixed input voltage 16 V. Similarly, in Fig. 4.11 (b), the simulation and experimental results are shown for same load variation, but at fixed input voltage 24 V. These results demonstrate that when the load is switched from 22 Ω to 11 Ω, the output voltage experiences the undershoot of 4 V and settles to 12 V within 15 ms. Similarly, when the load is shifted from 11 Ω to 22 Ω, the output voltage settles within 25 ms and with overshoot of 4 V- 6 V and undershoot of around 2 V. The experimental results are similar to the simulation results validating the performance of PI controller on buck converter prototype.

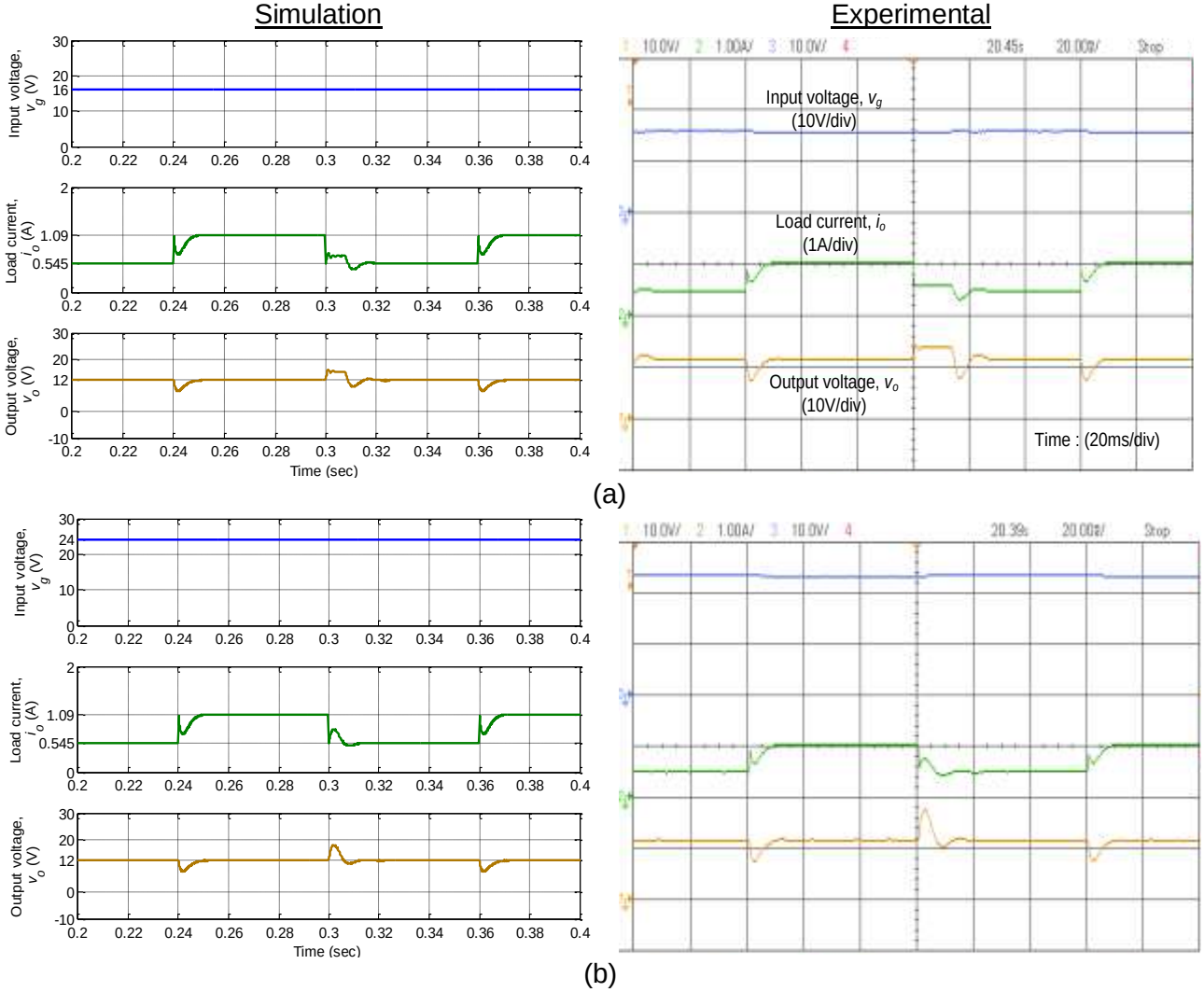


Fig. 4.11. Simulation and experimental results for variation in load resistance from 22 Ω to 11 Ω and vice-versa at input voltage (a) V_g=16 V (b) V_g=24 V

4.2.2 PI-lead controller design

As seen in the previous section, the phase margin of the uncompensated buck converter is poor and it is also having a constant gain in the low-frequency region which results in steady-state error. To improve these performance specifications, a PI controller was designed. The designed PI controller improves the phase margin and low-frequency gain. However, with PI controller, the improved phase margin occurs at a smaller gain crossover frequency. Due to smaller gain crossover frequency, the settling time of the output voltage is larger which was also validated from obtained simulation and experimental results.

However, for a stable and well-regulated DC-DC converter system, the frequency response should meet the following requirements [1], [3], [132]:

i) The gain in low-frequency region should be high to reduce/eliminate SSE in output voltage. Preferably, frequency response should have slope of -20dB/decade at low frequencies.

ii) The PM of the compensated system should be greater than 60° to ensure better closed-loop stability. Higher PM improves the transient response and therefore reducing the overshoots occurring due to the input voltage and/or load current fluctuations.

iii) The bandwidth (or GCF) of the compensated system should be between one-tenth to one-fourth of the converter switching frequency.

Now the role of different existing compensators are discussed in brief to meet the above requirements as follows [77], [78]:

a) PI controller: It is used to eliminate steady-state error (SSE). The transfer function of PI controller is given as

$$G_{PI}(s) = \frac{K_p s + K_i}{s} \tag{4.25}$$

K_p and K_i are the parameters of PI controller.

As discussed earlier, the PI controller adds a pole at the origin. Therefore, the closed-loop SSE for step input becomes zero. However, PI controller also contributes negative phase and thus reduces the overall phase margin (PM) of the compensated system. This results in excessive oscillations in output voltage response, which is not desirable. However, the phase margin of the compensated system can be improved at the cost of reduced gain crossover frequency resulting in slower speed of response. Therefore, PI controller is not a suitable choice to compensate the DC-DC converter system with poor PM.

b) PID controller: The transfer function of PID controller is

$$G_{PID}(s) = \frac{K_d s^2 + K_p s + K_i}{s} \tag{4.26}$$

K_p, K_i and K_d are the parameters of PID controller.

Due to the presence of a pole at the origin, it also eliminates the closed-loop SSE for the step input disturbances to DC-DC converter systems. It also helps in improving the phase margin. However, it introduces +20 dB/decade slope in the high frequency region and

therefore making the compensated DC-DC converter more susceptible to high frequency noise and output voltage ripple.

c) Lag compensator: The transfer function of lag compensator is

$$G_{lag}(s) = \frac{K_{lag}(s+\alpha)}{(s+\beta)}, \beta < \alpha \tag{4.27}$$

K_{lag}, α and β are the parameters of lag compensator.

The lag compensator is used to improve the steady-state performance. However, similar to PI controller, this compensator also introduces phase lag and therefore, is not a suitable choice as a compensator for DC-DC converters with poor PM.

d) Lead compensator: The transfer function of lead compensator is

$$G_{lead}(s) = \frac{K_{lead}(s+\alpha)}{(s+\beta)}, \beta > \alpha \tag{4.28}$$

K_{lead}, α and β are the parameters of lead compensator.

Lead compensator is used to add positive phase at desired GCF and thus improves PM. However, it does not help in improving steady-state performance of DC-DC converters.

e) Lag-lead compensator: The transfer function of lag-lead compensator is

$$G_{lag-lead}(s) = \frac{K_{lag-lead}(s+\alpha_1)(s+\alpha_2)}{(s+\beta_1)(s+\beta_2)}, \beta_1 < \alpha_1 \text{ and} \beta_2 > \alpha_2 \tag{4.29}$$

K_{lead}, α_1, β_1, α_2 and β_2 are the parameters of lag-lead compensator.

This compensator combines the properties of lag and lead compensators. The lag section improves the steady-state performance while lead section improves the transient performance. However, this compensator does not eliminate SSE arising from step input disturbances to DC-DC converter systems.

From the above discussion, it is observed that to eliminate SSE in output voltage, the controller (compensator) should have a pole at origin. In order to improve PM, the controller should also provide sufficient positive phase in the vicinity of GCF. None of the above-discussed controllers is meeting these requirements simultaneously. Therefore, to achieve both of these characteristics in a single controller, the PI and lead compensators are combined to form a PI-lead controller [182],[183]. In this PI-lead controller, the PI section is responsible to increase the gain at low frequencies and thus improving steady-state performance. The lead section is responsible to provide the specified PM at desired GCF and thus improving transient performance. In this section, an algorithm is proposed to determine the parameters of this PI-lead controller.

The PI-lead controller is a cascade combination of PI and lead compensators. Therefore, the transfer function of the PI-lead controller is defined as

$$G_{PI-lead}(s) = \frac{K_p s + K_i}{s} \cdot \frac{K_{lead}(s+\alpha)}{(s+\beta)}, \alpha < \beta$$

$$= \frac{K_i K_{lead}\left(\frac{s}{K_i/K_P}+1\right)(s+\alpha)}{s(s+\beta)}, \alpha < \beta \tag{4.30}$$

By introducing the new variable $K=K_i K_{lead}$ and $\omega_z=K_i/K_p$, the above equation can be rewritten in following form

$$G_{PI-lead}(s) = \frac{K\left(\frac{s}{\omega_z}+1\right)(s+\alpha)}{s(s+\beta)}, \alpha < \beta \tag{4.31}$$

Here K, ω_z, α and β are the parameters of PI-lead controller, which are tuned using the following algorithm.

4.2.2.1 Algorithm for tuning of PI-lead controller parameters

In this section, an analytical algorithm is proposed to determine the parameters of PI-lead controller. The simple analytical formulae are derived in terms of desired frequency domain specifications (*i.e.,* phase margin and gain crossover frequency). In this chapter, the PI-lead controller will be used to regulate the output voltage of both DC-DC buck converter and Cuk converter. Therefore, this algorithm is presented in general for a fourth-order DC-DC converter as below:

Step 1: Consider loop transfer function of an uncompensated fourth-order DC-DC converter as

$$G(s) = \frac{b_3 s^3 + b_2 s^2 + b_1 s + b_0}{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \tag{4.32}$$

This is a type-0 system, which has constant gain in the low-frequency region and poor phase margin (PM) in vicinity of gain crossover frequency (GCF).

For this system, the PI-lead controller is designed by dividing it in two parts (a) PI control design and (b) lead compensator design

Step 2: To increase the low-frequency gain, a PI controller $G_{PI}(s)$ is designed, which is having transfer function in the following form:

$$G_{PI}(s) = \frac{\left(\frac{s}{\omega_z}+1\right)}{s} \tag{4.33}$$

Here, ω_z is the corner frequency of the PI controller, which is selected sufficiently below than the GCF in order to increase the low-frequency gain.

With the PI controller design, the system in (4.32) becomes

$$G_1(s) = G(s)G_{PI}(s) = \frac{\frac{b_3}{\omega_z}s^4 + \left(b_3 + \frac{b_2}{\omega_z}\right)s^3 + \left(b_2 + \frac{b_1}{\omega_z}\right)s^2 + \left(b_1 + \frac{b_0}{\omega_z}\right)s + b_0}{a_4 s^5 + a_3 s^4 + a_2 s^3 + a_1 s^2 + a_0 s} \tag{4.34}$$

As the PI compensated system in (4.34) is type-1 system, the closed-loop will have zero steady-state error for step input disturbances. Now, the next step is to design the lead section for improving the transient performance.

Step 3: Specify the desired phase margin φ_{margin} (in degree) and gain crossover frequency ω_{gc} (rad/sec) of overall compensated DC-DC converter system.

Let the magnitude and phase of $G_1(s)$ at gain crossover frequency ω_{gc} are denoted by K_1 and φ_1, respectively *i.e.,*

$$K_1 = \left|G_1\left(j\omega_{gc}\right)\right|, \varphi_1 = \angle G_1\left(j\omega_{gc}\right) \tag{4.35}$$

To fulfil the specified PM and GCF requirements exactly, the lead section parameters should be designed to contribute magnitude K_{req} and phase angle φ_{req} at frequency ω_{gc}. Mathematically,

$$K_{req} = 1/K_1 \tag{4.36}$$

$$\varphi_{req} = -180^{\circ} - \varphi_1 + \varphi_{margin} \tag{4.37}$$

Step 4: The function of the lead section is to provide the desired phase lead at frequency ω_{gc}. In this step, the parameters of lead section are designed in such a way that the desired phase boost at ω_{gc} is met exactly. There is no need to add any additional phase angle as done in the conventional lead compensator design [77], [78].

The transfer function of the lead section (compensator) is

$$G_{lead}\left(s\right) = K\frac{s+\alpha}{s+\beta}, \alpha < \beta \tag{4.38}$$

Magnitude and phase angle of the above transfer function at any frequency 'ω' will be

$$\left|G_{lead}\left(j\omega\right)\right| = K\frac{\sqrt{\omega^2+\alpha^2}}{\sqrt{\omega^2+\beta^2}} \tag{4.39}$$

$$\varphi_{lead} = \angle G_{lead}\left(j\omega\right) = \tan^{-1}\left(\frac{\omega}{\alpha}\right) - \tan^{-1}\left(\frac{\omega}{\beta}\right) = \tan^{-1}\frac{\omega\left(\beta-\alpha\right)}{\omega^2+\alpha\beta} \tag{4.40}$$

As $\beta > \alpha$, therefore angle φ_{lead} is always positive as expected.

To find out the frequency (ω_m) at which lead compensator contributes maximum phase angle, differentiating (4.40) with respect to 'ω' [77], [78], we get

$$\omega_m = \sqrt{\alpha\beta} \tag{4.41}$$

By substituting (4.41) into (4.39) and (4.40), magnitude (K_m) and phase angle (φ_m) of lead compensator at frequency $\omega=\omega_m$ are

$$K_m = K\sqrt{\frac{\alpha}{\beta}} \tag{4.42}$$

$$\varphi_m = \tan^{-1}\frac{\beta-\alpha}{2\sqrt{\alpha\beta}} = \sin^{-1}\frac{\beta-\alpha}{\beta+\alpha} \tag{4.43}$$

This frequency ω_m is chosen as desired gain crossover frequency, ω_{gc} .Therefore, in order to have the desired phase margin at this frequency, the parameters K_m and φ_m must be equal to parameters K_{req} and φ_{req} respectively. Therefore,

$$\omega_{gc}\left(=\omega_m\right)=\sqrt{\alpha\beta} \tag{4.44}$$

$$\varphi_{req}\left(=\varphi_m\right)=\sin^{-1}\frac{\beta-\alpha}{\beta+\alpha} \tag{4.45}$$

$$K_{req}\left(=K_m\right)=K\sqrt{\frac{\alpha}{\beta}} \tag{4.46}$$

Equations (4.44)-(4.46) are simplified to get the lead compensator parameters (K, α and β) in terms of desired parameters, thus we get

$$K=K_{req}\sqrt{\frac{1+\sin\varphi_{req}}{1-\sin\varphi_{req}}} \tag{4.47}$$

$$\alpha=\omega_{gc}\sqrt{\frac{1-\sin\varphi_{req}}{1+\sin\varphi_{req}}} \tag{4.48}$$

$$\beta=\omega_{gc}\sqrt{\frac{1+\sin\varphi_{req}}{1-\sin\varphi_{req}}} \tag{4.49}$$

The above steps can be summarized as in following steps:

1. Obtain the duty-cycle-to-output-voltage transfer function $G_{vd}(s)$ of the DC-DC converter and thus uncompensated loop transfer function $G(s)$.
2. Design the PI section of PI-lead controller by placing zero (ω_z) at lower frequency sufficiently below than gain crossover frequency ω_{gc}.
3. Define the desired phase margin (φ_{margin}) and gain crossover frequency (ω_{gc} in rad/sec).
4. Calculate the required gain (K_{req}) and phase boost (φ_{req}) to be obtained from the lead section using (4.36) and (4.37).
5. Finally, obtain the lead section parameters using (4.47)-(4.49).

4.2.2.2 PI-lead controller design for buck converter

Fig. 4.12 shows the block diagram of PI-lead controlled DC-DC buck converter. As shown in figure, The actual output voltage (v_o) is compared with reference output voltage ($v_{o,ref}$). In this scheme, the voltage error (v_{err}) is passed though PI-lead controller, which gives control voltage, v_c. This control voltage signal is compared with fixed frequency and fixed magnitude sawtooth waveform to generate the gate pulses for the switch. The detailed schematic of this control scheme remains same as shown in Fig. 4.4 except the PI controller is replaced by PI-lead controller.

In the previous section, the design algorithm to determine the parameters of PI-lead controller based on frequency domain measures has been developed. The performance of PI section depends on selected corner frequency (ω_z or f_z) and the performance of the lead section depends upon chosen PM (φ_{margin}) and GCF (ω_{gc} or f_{gc}). Normally, these performance

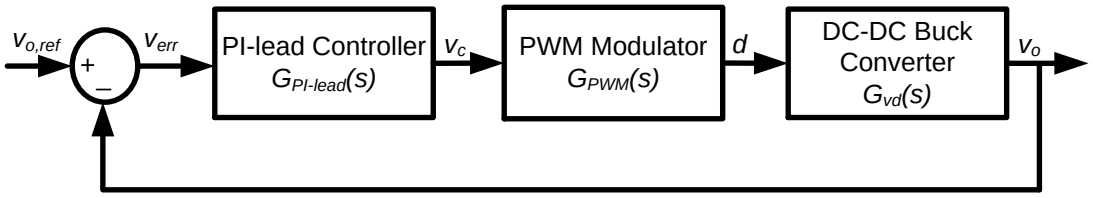


Fig. 4.12. Block diagram of closed-loop control of buck converter using PI-lead controller

parameters are specified based on some thumb rules. There is no quantitative solution in the literature for specifying these parameters to the best of the author's knowledge. Therefore, in this section, the performance of the buck converter with PI-lead controller is evaluated for different combinations of f_z, f_{gc} and φ_{margin} by fixing two parameters at a time and varying the other. The parameters of buck converter are same as given in Table 4.1. Based on this analysis, the PI-lead controller giving the best performance is chosen.

(a) Performance analysis with variation of φ_{margin} at fixed f_z and f_{gc}

In this subsection, the performance of the compensated buck converter is analysed for different values of φ_{margin} at fixed gain crossover frequency f_{gc} (=$\omega_{gc}/2\pi$), in Hz. For this analysis, the different values of φ_{margin} are taken as 30°, 45°, 60°, 75° and 90°. The different values of f_{gc} are chosen as 0.5 kHz, 1 kHz, 2 kHz, 3 kHz and 5 kHz. The corner frequency f_z (=$\omega_z/2\pi$) of PI section is kept constant at 40 Hz.

The uncompensated loop transfer function of buck converter remains same as in (4.19). For the sake of understanding, it is rewritten below:

$$T(s) = G_{PWM}(s)G_{vd}(s) = \frac{1}{V_{sw}}G_{vd}(s) = \frac{4428s + 1.757\times10^8}{s^2 + 1518s + 1.074\times10^7} \tag{4.50}$$

The PI-lead controller is designed for this transfer function of the buck converter using the design algorithm given in the previous section. The design procedure is illustrated for one combination of desired PM and GCF *i.e.,* φ_{margin}=30° at f_{gc}=0.5 kHz. It will remain same for another set of specifications.

Substituting ω_z =2π×40 into (4.33), the transfer function of PI section is obtained as

$$G_{PI}(s)\big|_{f_z=40Hz} = \frac{0.003979s + 1}{s} \tag{4.51}$$

and the parameters of lead section are obtained using (4.47)-(4.49) as K=1.246, α=1.81×10^4, β=544. Therefore, the complete PI-lead controller transfer function is

$$G_{PI-lead}(s)\Big|_{\substack{f_z=40\,Hz\\ f_{gc}=0.5\,kHz\\ \varphi_{margin}=30^\circ,}} = \frac{1.246\times(0.003979s+1)\left(s+1.81\times10^4\right)}{s(s+544)} \tag{4.52}$$

Similarly, the PI-lead controller transfer function is determined for PM of 45°,60°,75° and 90° at GCF 0.5 kHz. All the transfer functions and corresponding frequency domain and time domain performance indices of the compensated buck converter are given in Table 4.2. The important time domain performance specifications such as rise time (t_r), settling time (t_s) within 2% tolerance band and overshoot (M_p) are determined. The respective frequency

responses and step time responses of the compensated buck converter are shown in Fig. 4.13. The frequency responses indicate that the gain margin increases with phase margin and becomes infinite for PM 75° and 90°. The time response indicates that as PM is increased, the overshoot is decreased, but rise time and settling time are increased. Similarly, the PI-lead controller is designed for different values of GCF. The corresponding performance indices, frequency responses, and step time responses are obtained. These are shown in Table 4.3 and Fig. 4.14 for f_{gc}=1 kHz; in Table 4.4 and Fig. 4.15 for f_{gc}=2 kHz; in Table 4.5 and Fig. 4.16 for f_{gc}=3 kHz; in Table 4.6 and Fig. 4.17 for f_{gc}=5 kHz.

The following observations are made from the above performance analysis:

(i) Gain margin of the compensated system is infinite in all cases except for φ_{margin}=30°, 45° and 60° at f_{gc}=0.5 kHz.

(ii) At a particular specified GCF, if PM is increased, then the peak overshoot decreases, but rise time and settling time is increased. Therefore, a compromise has to be made while specifying PM.

(iii) At f_{gc}=0.5 kHz and 1 kHz, for PM greater than or equal to 60°, there is no overshoot. However, at higher gain crossover frequencies, overshoot increases. The overshoot is reduced for the comparatively larger value of PM.

(iv) The studies show that the PM of 75° is the best choice for this buck converter. Because if a lower value is chosen, the overshoot is more and if higher value is chosen, the rise time and settling time is more. For φ_{margin}=75°, the parameters are moderate.

Table 4.2. Performance indices of compensated buck converter for f_z=40 Hz and f_{gc}=0.5 kHz

Performance indices						PI-lead controller transfer function
Frequency domain			Time domain			
PM(°)	GM(dB)	f_{pc}(kHz)	t_r(ms)	t_s(ms)	M_p(%)	
30	2.66	0.57	0.66	18.7	9.17	$\frac{1.25(0.003979s+1)(s+1.81\times10^4)}{s(s+544)}$
45	5.26	0.62	4.3	19.6	0	$\frac{2.24(0.003979s+1)(s+1.01\times10^4)}{s(s+980)}$
60	9.83	0.72	12.3	25.0	0	$\frac{3.33(0.003979s+1)(s+6792)}{s(s+1453)}$
75	Inf	inf	16.4	31.6	0	$\frac{4.55(0.003979s+1)(s+4965)}{s(s+1988)}$
90	Inf	inf	20.9	39.2	0	$\frac{5.99(0.003979s+1)(s+3767)}{s(s+2620)}$

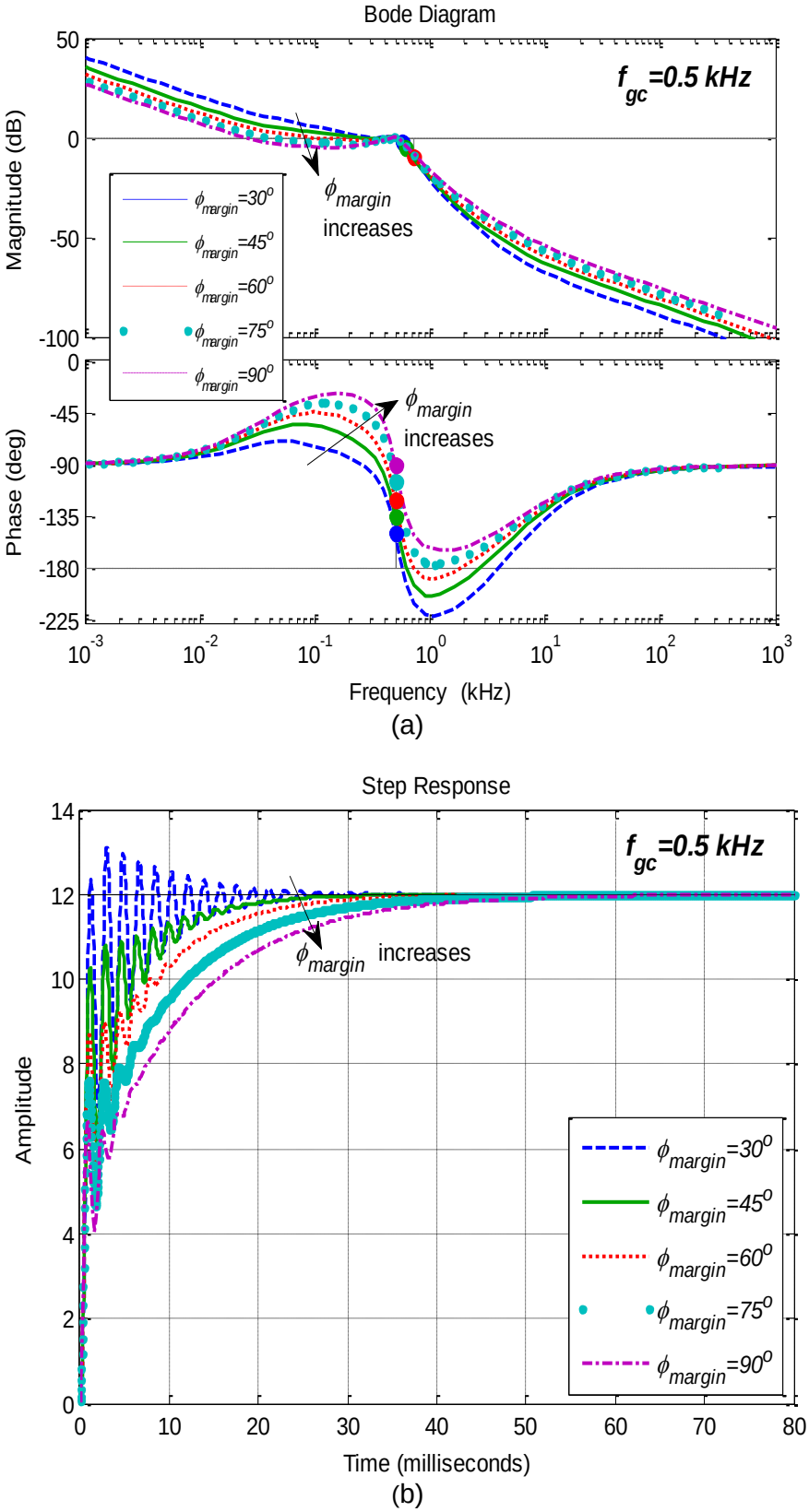


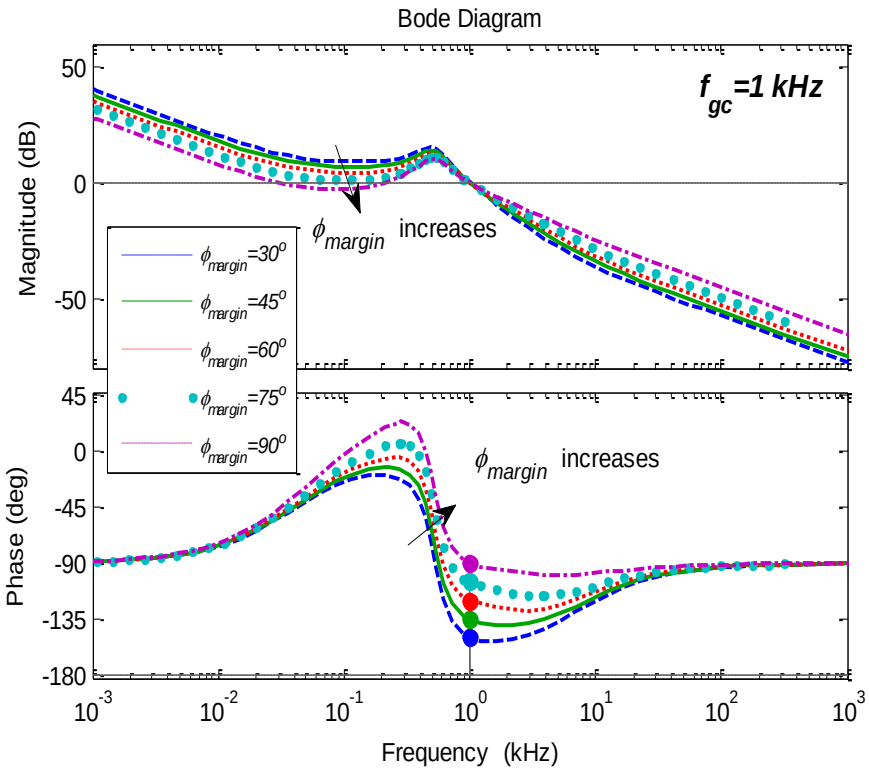
Fig. 4.13. Compensated DC-DC buck converter responses with different phase margin at f_{gc}= 0.5 kHz and f_z=40 Hz (a) frequency response (b) step response

Table 4.3. Performance indices of compensated buck converter for f_z=40 Hz and f_{gc}=1 kHz

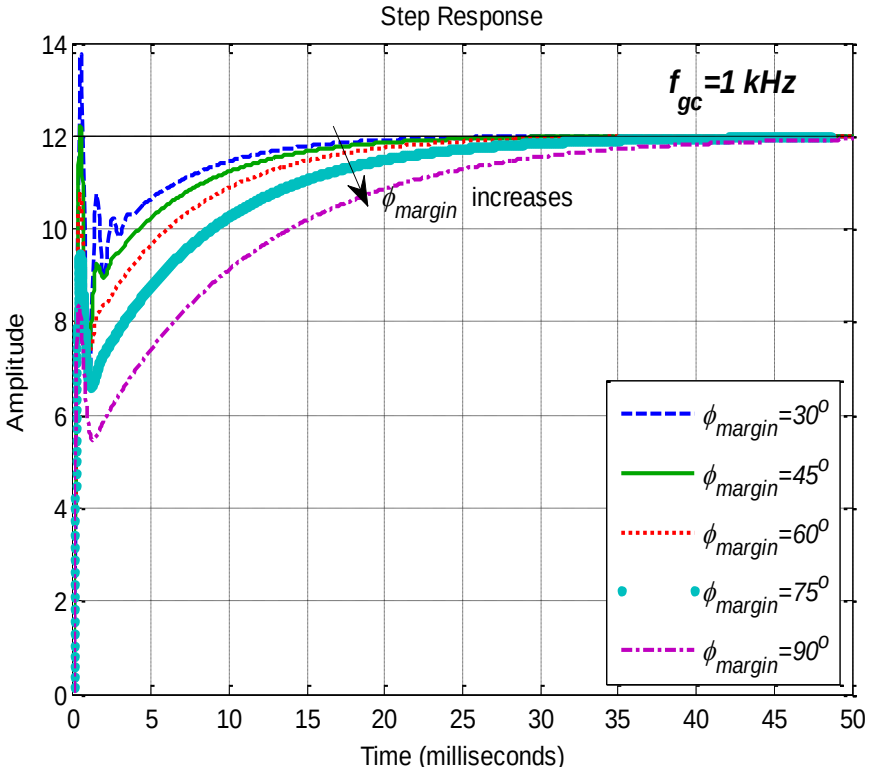
Performance indices						PI-lead controller transfer function
Frequency domain			Time domain			
PM(°)	GM(dB)	f_{pc}(kHz)	t_r(ms)	t_s(ms)	M_p(%)	
30	inf	inf	0.25	14.6	14.7	$\frac{48.63(0.003979s+1)(s+5765)}{s(s+6848)}$
45	inf	inf	0.27	17.1	1.74	$\frac{63.62(0.003979s+1)(s+4405)}{s(s+8961)}$
60	inf	inf	9.5	20.4	0	$\frac{85.6(0.003979s+1)(s+3276)}{s(s+1.2\times10^4)}$
75	inf	inf	12.8	25.8	0	$\frac{122.3(0.003979s+1)(s+2291)}{s(s+1.7\times10^4)}$
90	inf	inf	19.4	36.8	0	$\frac{200.6(0.003979s+1)(s+1397)}{s(s+2.8\times10^4)}$

Table 4.4. Performance indices of compensated buck converter for f_z=40 Hz and f_{gc}=2 kHz

Performance indices						PI-lead controller transfer function
Frequency domain			Time domain			
PM(°)	GM(dB)	f_{pc}(kHz)	t_r(ms)	t_s(ms)	M_p(%)	
30	inf	inf	0.09	5.8	38.7	$\frac{235.3(0.003979s+1)(s+1.12\times10^4)}{s(s+1.4\times10^4)}$
45	inf	inf	0.10	7.1	24.0	$\frac{308.3(0.003979s+1)(s+8606)}{s(s+1.83\times10^4)}$
60	inf	inf	0.11	8.6	11.7	$\frac{416.1(0.003979s+1)(s+6377)}{s(s+2.47\times10^4)}$
75	inf	inf	0.13	10.7	1.6	$\frac{599.5(0.003979s+1)(s+4427)}{s(s+3.56\times10^4)}$
90	inf	inf	0.19	14.3	0	$\frac{1001.6(0.003979s+1)(s+2649)}{s(s+5.96\times10^4)}$

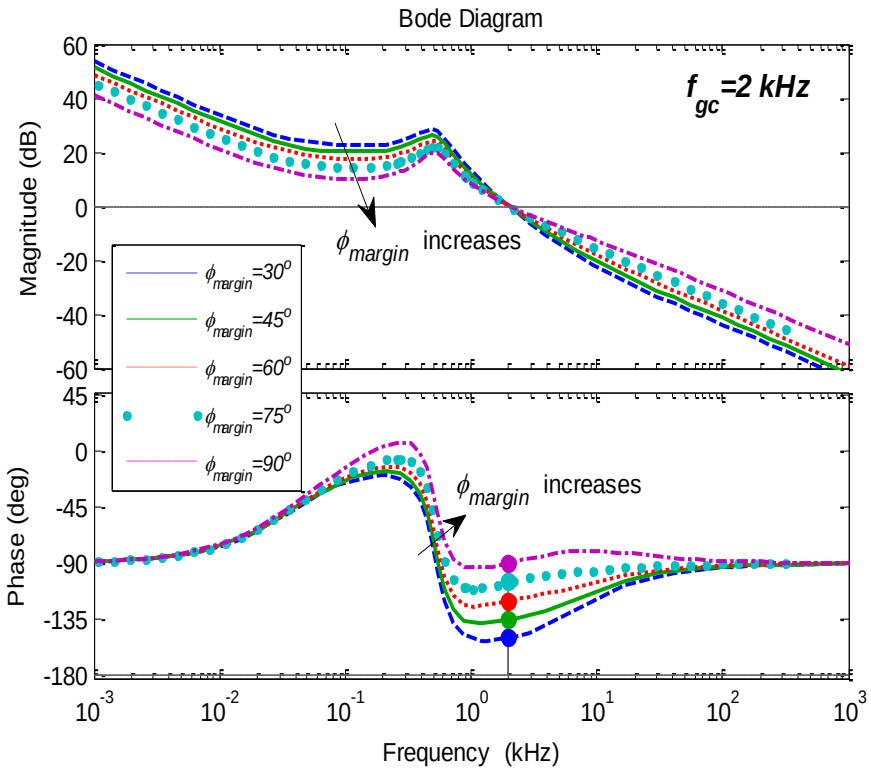


(a)

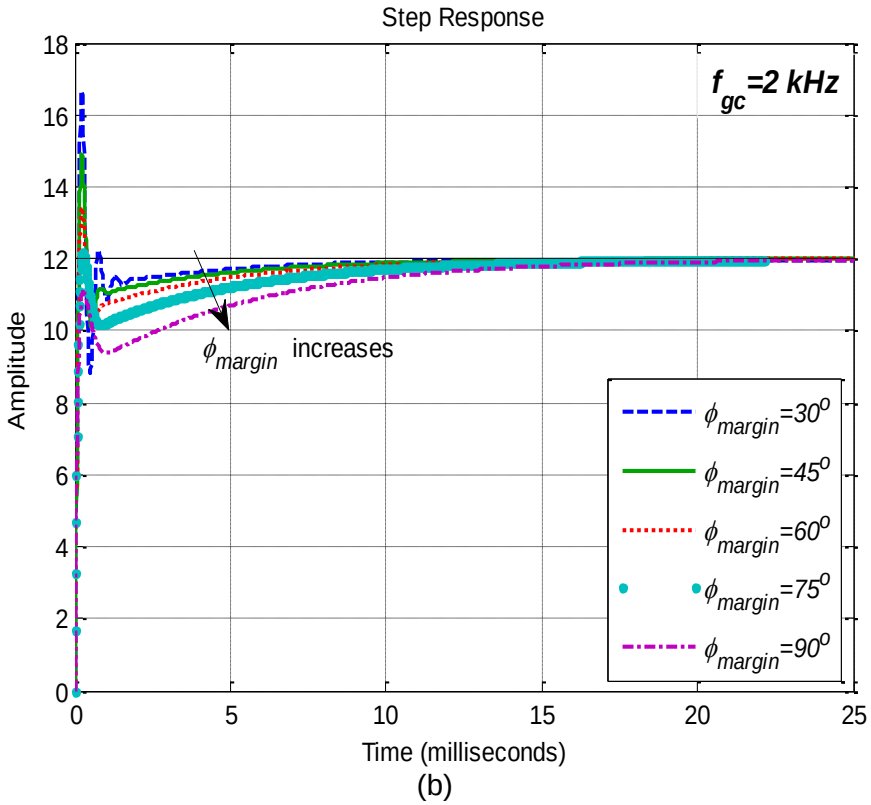


(b)

Fig. 4.14. Compensated DC-DC buck converter responses with different phase margin at f_{gc}= 1 kHz and f_z=40 Hz (a) frequency response (b) step response



(a)



(b)

Fig. 4.15. Compensated DC-DC buck converter responses with different phase margin at f_{gc}= 2 kHz and f_z=40 Hz (a) frequency response (b) step response

Table 4.5. Performance indices of compensated buck converter for f_z=40 Hz and f_{gc}=3 kHz

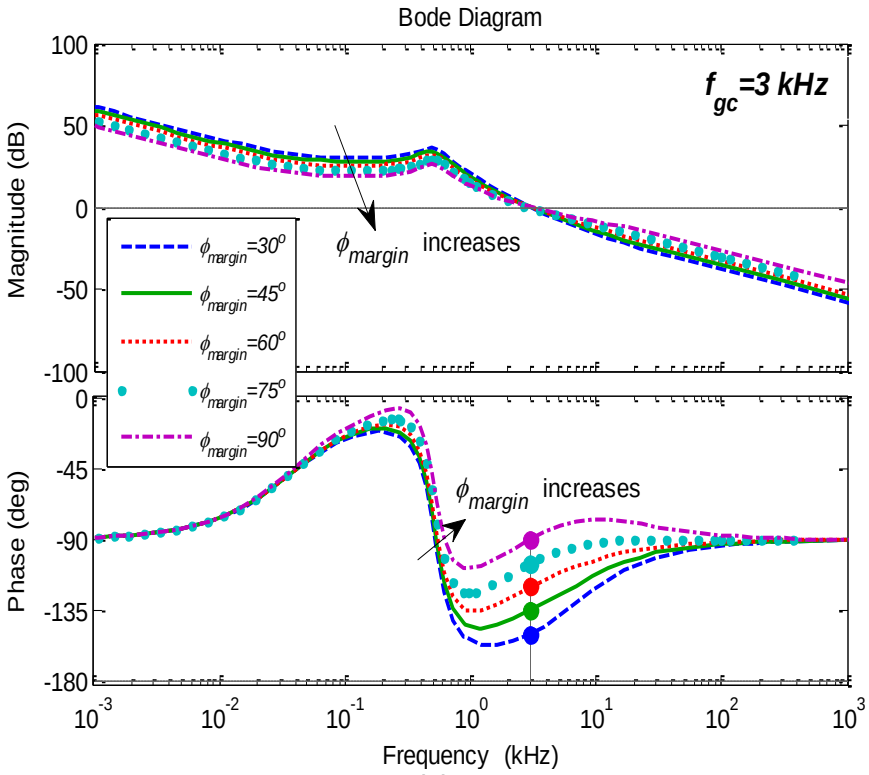
Performance indices						PI-lead controller transfer function
Frequency domain			Time domain			
PM(°)	GM(dB)	f_{pc}(kHz)	t_r(ms)	t_s(ms)	M_p(%)	
30	inf	inf	0.062	2.0	43.3	$\frac{471.2(0.003979s+1)(s+1.86\times10^4)}{s(s+1.91\times10^4)}$
45	inf	inf	0.066	3.2	29.3	$\frac{614.3(0.003979s+1)(s+1.43\times10^4)}{s(s+2.48\times10^4)}$
60	inf	inf	0.071	4.4	17.9	$\frac{817.5(0.003979s+1)(s+1.07\times10^4)}{s(s+3.31\times10^4)}$
75	inf	inf	0.08	5.9	9.3	$\frac{1142.7(0.003979s+1)(s+7691)}{s(s+4.62\times10^4)}$
90	inf	inf	0.10	#	2.3	$\frac{1777.7(0.003979s+1)(s+4944)}{s(s+7.18\times10^4)}$

the steady-state value of output voltage does not settle within 2% tolerance band.

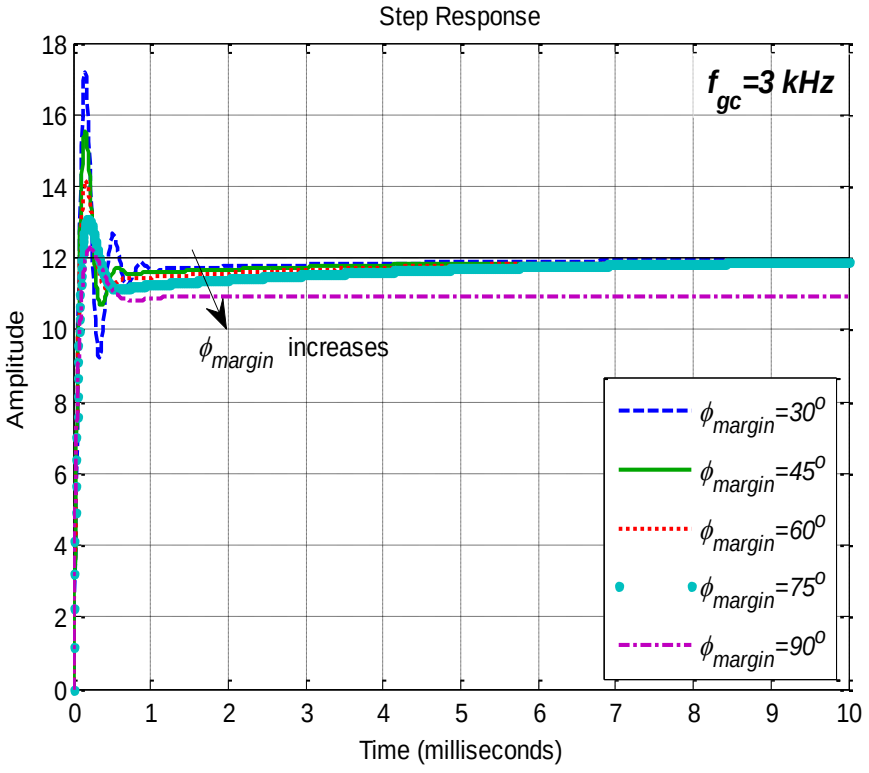
Table 4.6. Performance indices of compensated buck converter for f_z=40 Hz and f_{gc}=5 kHz

Performance indices						PI-lead controller transfer function
Frequency domain			Time domain			
PM(°)	GM(dB)	f_{pc}(kHz)	t_r(ms)	t_s(ms)	M_p(%)	
30	inf	inf	0.036	0.47	45.8	$\frac{948(0.003979s+1)(s+3.79\times10^4)}{s(s+2.6\times10^4)}$
45	inf	inf	0.038	0.30	32.3	$\frac{1233.2(0.003979s+1)(s+2.91\times10^4)}{s(s+3.38\times10^4)}$
60	inf	inf	0.041	0.36	21.9	$\frac{1612.6(0.003979s+1)(s+2.23\times10^4)}{s(s+4.43\times10^4)}$
75	inf	inf	0.046	0.99	14.7	$\frac{2165(0.003979s+1)(s+1.66\times10^4)}{s(s+5.95\times10^4)}$
90	inf	inf	0.056	#	9.7	$\frac{3084(0.003979s+1)(s+1.16\times10^4)}{s(s+8.47\times10^4)}$

the steady-state value of output voltage does not settle within 2% tolerance band.

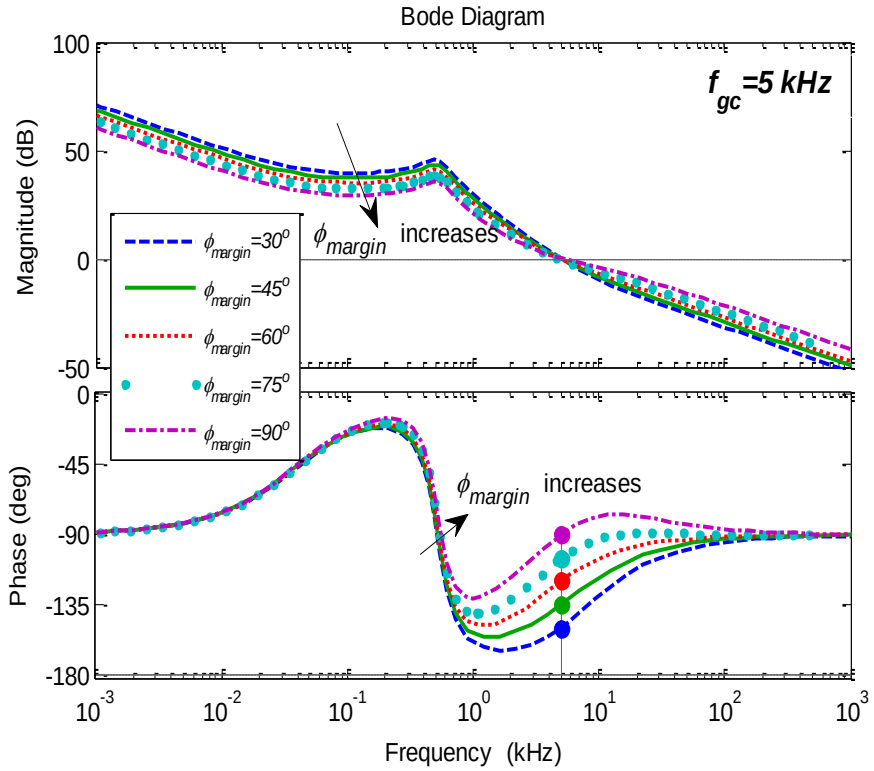


(a)

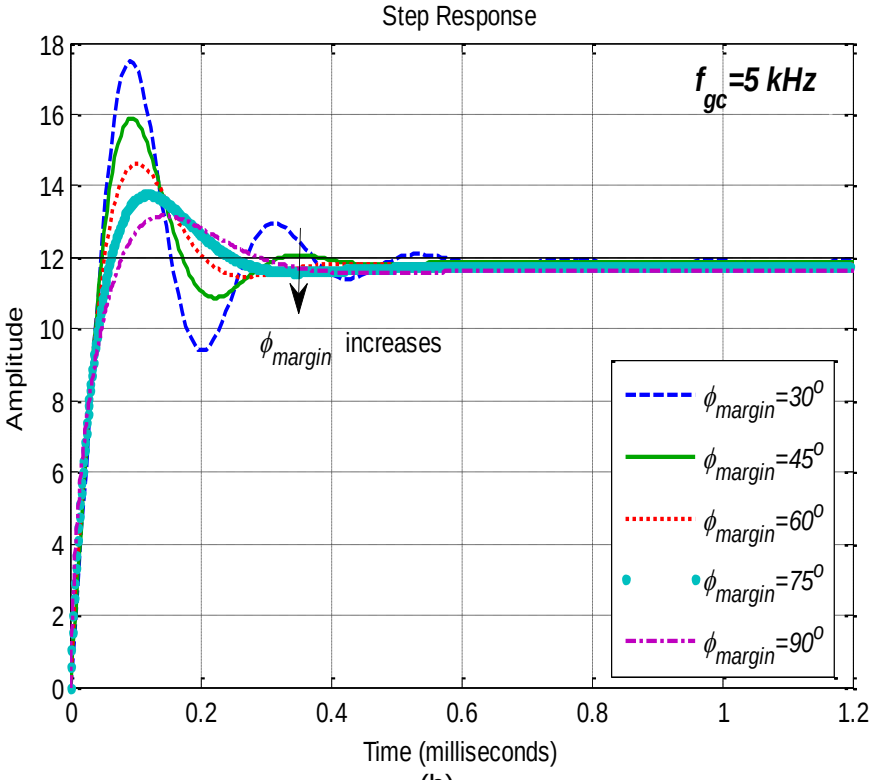


(b)

Fig. 4.16. Compensated DC-DC buck converter responses with different phase margin at f_{gc}= 3 kHz and f_z=40 Hz (a) frequency response (b) step response



(a)



(b)

Fig. 4.17. Compensated DC-DC buck converter responses with different phase margin at f_{gc}= 5 kHz and f_z=40 Hz (a) frequency response (b) step response

(b) Performance analysis with variation of f_{gc} at fixed φ_{margin} and f_z

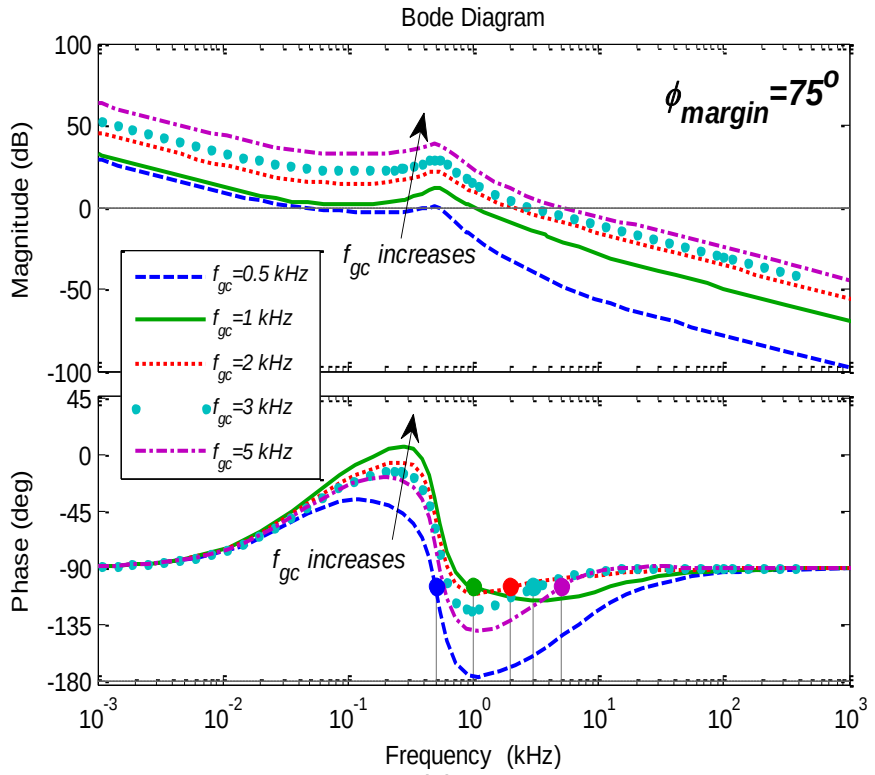
In this section, the analysis is performed at different values of GCF for fixed φ_{margin}=75° and f_z=40 Hz. The corresponding PI-lead controller transfer functions and performance indices are reported in Table 4.7. The frequency responses and step time responses are shown in Fig. 4.18. The gain margin is infinite at all values of f_{gc}. The step time responses indicate that for f_{gc}=0.5 kHz, peak overshoot is 0%, but rise time is 16.4 ms and settling time is 31.6 ms; for f_{gc}=1 kHz, peak overshoot is 0%, but rise time is 12.8 ms and settling time is 25.8 ms; for f_{gc}=2 kHz, peak overshoot is 1.6%, but rise time is 0.13 ms and settling time is 10.7 ms. For f_{gc}=3 kHz and 5 kHz, rise time and settling time are very small, but peak overshoot is high. Therefore, the compensated system will respond better for f_{gc} =2 kHz with moderate overshoot (less than 2%).

(c) Performance analysis with variation of f_z at constant φ_{margin} and f_{gc}

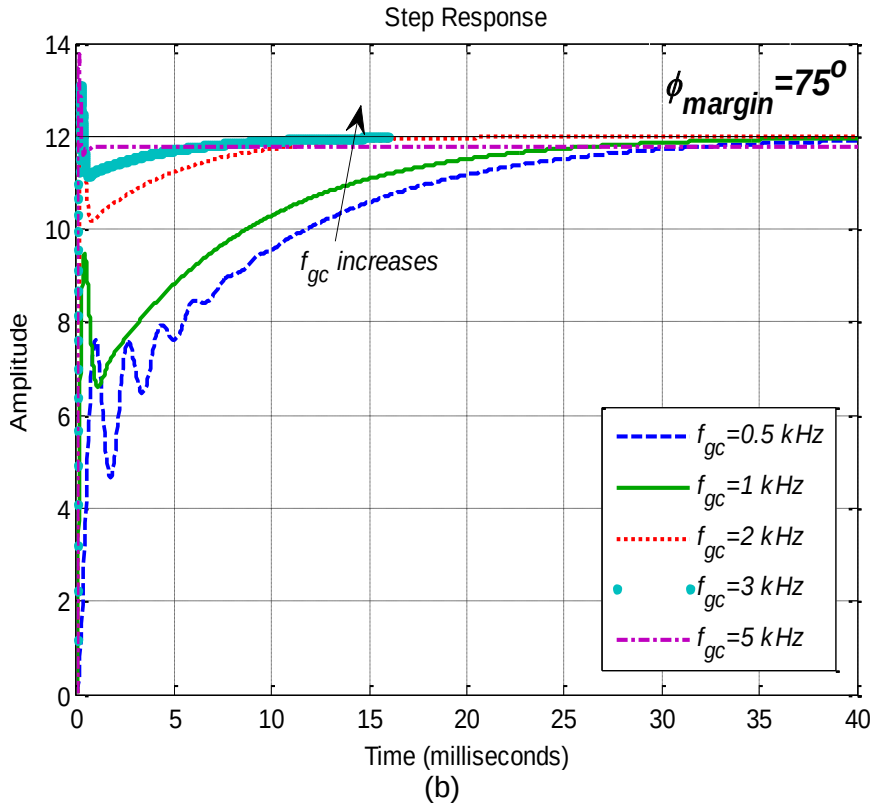
In the previous sections, the PI-lead controller has been designed for various combinations of PM and GCF. The performance analysis shows that the PM of 75° at GCF of 2 kHz is suitable choice for the controller design. However, all these performance analysis were carried out at fixed f_z=40 Hz. In this section, the PI-lead controller is designed by varying the corner frequency (f_z) of PI section and the performance of the resultant compensated system is evaluated. The corresponding PI-lead controller transfer functions and performance indices are given in Table 4.8. The frequency response and step time response are shown in Fig. 4.19. The results show that gain margin is infinite for each f_z. As f_z is increased, the rise time and settling time decrease, but peak overshoot increases. Therefore, depending upon the requirement, f_z can be chosen. In this paper, f_z=40 Hz is chosen, which results in 0.135 ms rise time, 10.7 ms settling time and 1.6% peak overshoot.

Table 4.7. Performance indices of compensated buck converter for f_z=40 Hz and PM=75°

Performance indices						PI-lead controller transfer function
Frequency domain			Time domain			
PM(°)	GM(dB)	f_{pc}(kHz)	t_r(ms)	t_s(ms)	M_p(%)	
0.5	inf	inf	16.4	31.6	0	$\frac{4.55(0.003979s+1)(s+4965)}{s(s+1988)}$
1	inf	inf	12.8	25.8	0	$\frac{122.3(0.003979s+1)(s+2291)}{s(s+1.7\times10^4)}$
2	inf	inf	0.13	10.7	1.6	$\frac{599.5(0.003979s+1)(s+4427)}{s(s+3.56\times10^4)}$
3	inf	inf	0.08	5.9	9.3	$\frac{1142.7(0.003979s+1)(s+7691)}{s(s+4.62\times10^4)}$
5	inf	inf	0.046	0.99	14.7	$\frac{2165(0.003979s+1)(s+1.66\times10^4)}{s(s+5.95\times10^4)}$

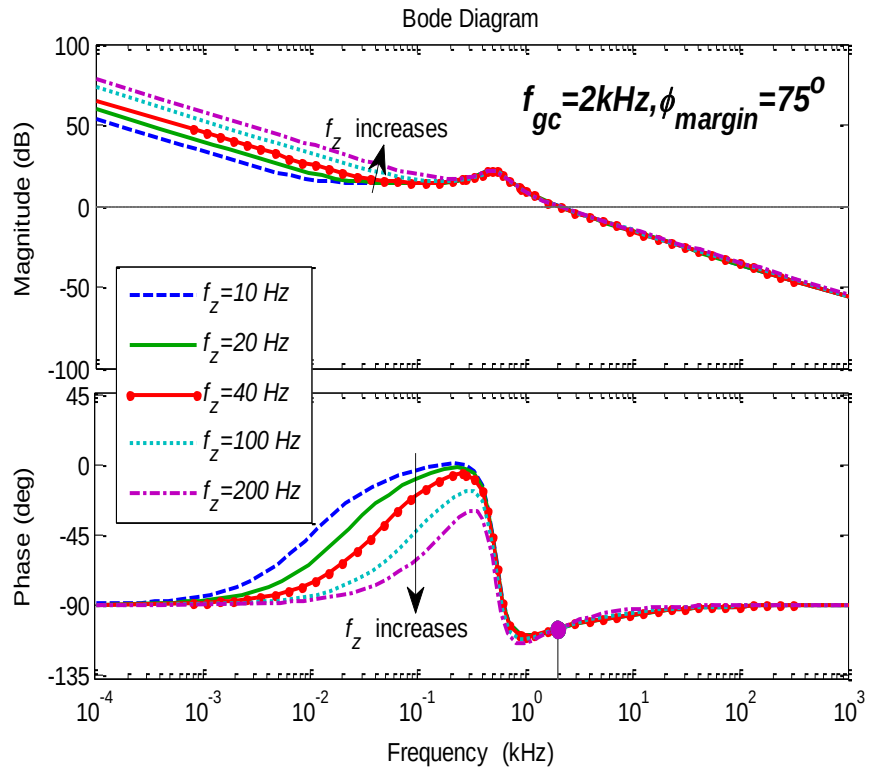


(a)

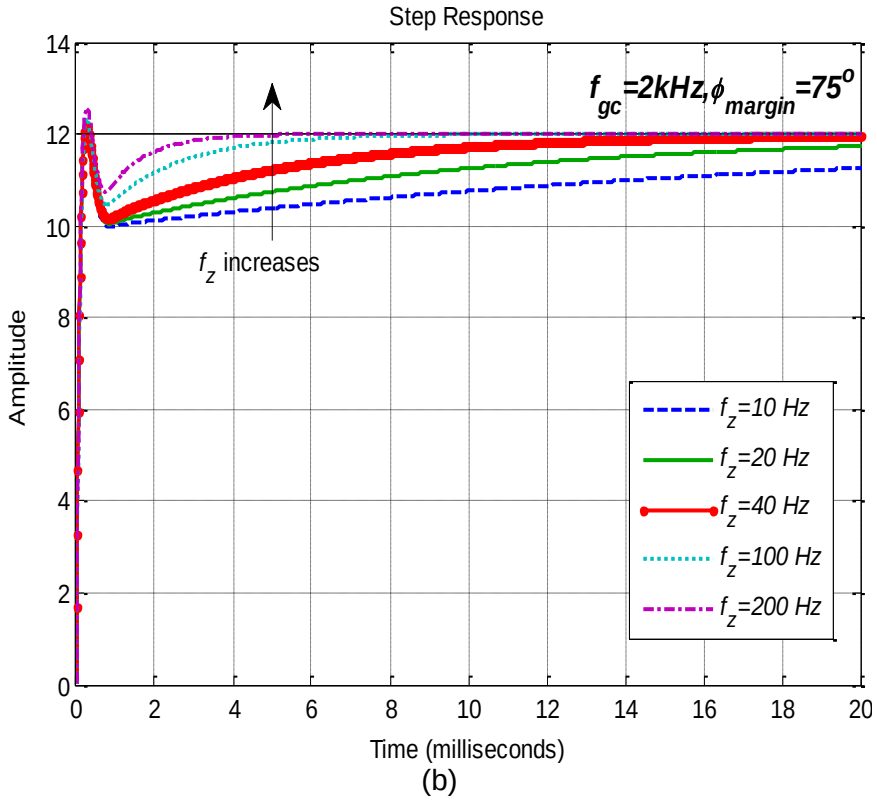


(b)

Fig. 4.18. Compensated DC-DC buck converter responses with φ_{margin}=75° at different gain crossover frequencies and f_z=40 Hz (a) frequency response (b) step response



(a)



(b)

Fig. 4.19. Compensated DC-DC buck converter responses at different values of f_z with constant φ_{margin}=75° and f_{gc}=2 kHz (a) frequency response (b) step response

Table 4.8. Performance indices of compensated buck converter for PM=75° and f_{gc}=2 kHz

Performance indices						PI-lead controller transfer function
Frequency domain			Time domain			
PM(°)	GM(dB)	f_{pc}(kHz)	t_r(ms)	t_s(ms)	M_p(%)	
10	inf	inf	0.137	41.8	0.9	$\frac{146.4(0.0159s+1)(s+4533)}{s(s+3.48\times10^4)}$
20	inf	inf	0.136	21.0	1.13	$\frac{295.1(0.00796s+1)(s+4497)}{s(s+3.51\times10^4)}$
40	inf	inf	0.135	10.7	1.6	$\frac{599.5(0.003979s+1)(s+4427)}{s(s+3.567\times10^4)}$
100	inf	inf	0.133	4.5	2.9	$\frac{1571.9(0.001592s+1)(s+4216)}{s(s+3.745\times10^4)}$
200	inf	inf	0.13	2.5	4.8	$\frac{3411(0.000796s+1)(s+3872)}{s(s+4.079\times10^4)}$

From the above analysis, it is concluded that for the buck converter under consideration, the PI-lead controller designed with f_z=40 Hz, φ_{margin}=75°, f_{gc}=2 kHz will result in better transient and steady-state performance. The transfer function of corresponding PI-lead controller is

$$G_{PI-lead}(s)=\frac{599.5\times(0.003979s+1)(s+4427)}{s(s+3.567\times10^4)} \tag{4.53}$$

Therefore, loop transfer function of PI-lead controlled system is

$$G_{PI-lead}(s)T(s)=\frac{599.5\times(0.003979s+1)(s+4427)}{s(s+3.567\times10^4)}\cdot\left(\frac{4428s+1.757\times10^8}{s^2+1518s+1.074\times10^7}\right) \tag{4.54}$$

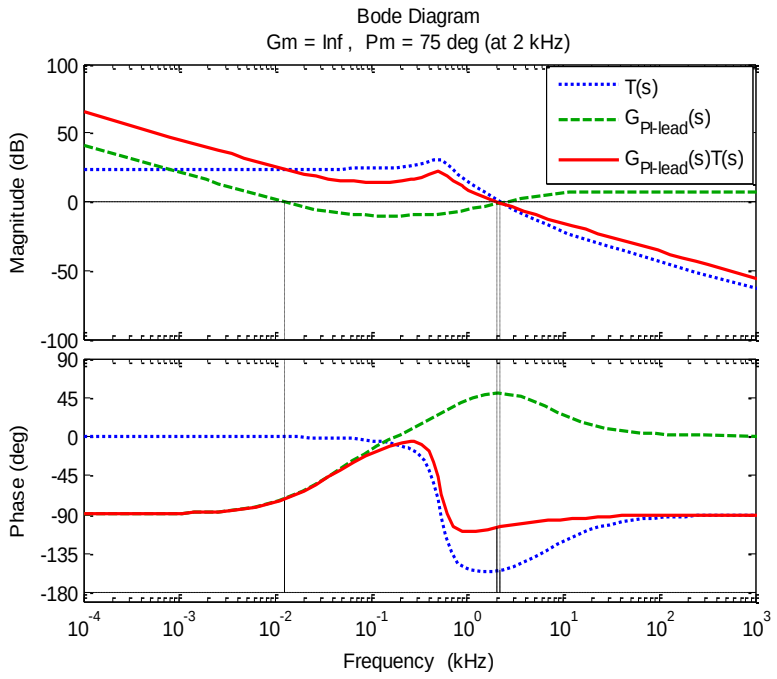


Fig. 4.20. Frequency response of PI-lead controlled DC-DC buck converter

The frequency response of the buck converter with PI-lead control design is shown in Fig. 4.20. As observed from this figure, the phase margin of the compensated system is 75° at a gain crossover frequency of 2 kHz, which was the objective of this controller design. These performance specifications are met exactly as specified. The slope of the magnitude plot is -20 dB/decade in the low-frequency region, which reduces the steady-state error for any step disturbance. The increased gain crossover frequency helps in faster speed of response.

4.2.2.3 Results and discussion

To observe the performance of the proposed PI-lead controller for DC-DC buck converter, the simulation and experimental studies are performed. The PI-lead controller in (4.53) (designed for phase margin 75° at a gain crossover frequency of 2 kHz) is used for this purpose. The simulation is carried out using MATLAB/Simulink software and experimental results are obtained implementing the PI-lead controller based on dSPACE system. The experimental setup remains same as used for PI controller, except replacing the PI controller transfer function by PI-lead controller transfer function.

The simulation and experimental results are obtained for three different conditions:

(a) Variation in reference output voltage

(b) Variation in input voltage

(c) Variation in load current

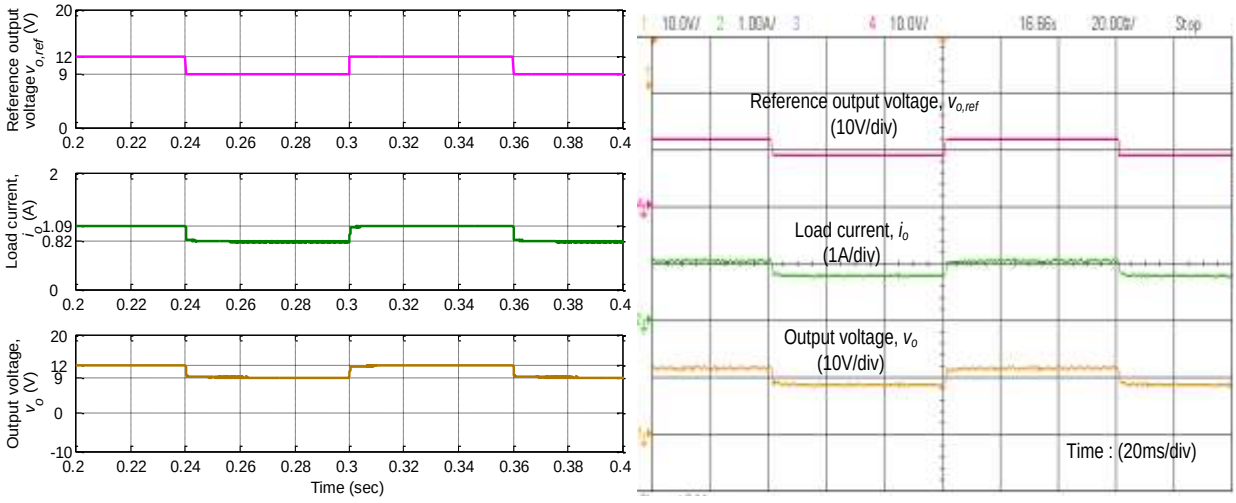
(a) Variation in reference output voltage

The performance of PI-lead controller for buck converter is observed for step variation in reference output voltage ($V_{o,ref}$). The input voltage (V_g) and load resistance (R) are kept fixed to 16 V and 11 Ω, respectively. When the reference voltage varies from 12 V to 9 V and vice-versa, the simulation and experimental results are shown in Fig. 4.21 (a) and when it varies from 12 V to 15 V and vice-versa, the respective simulation and experimental results are shown in Fig. 4.21 (b). It is seen that the output voltage is settled within 10 ms without any oscillations or overshoot/undershoot. The load current is 0.82 A, 1.09 A and 1.36 A for desired output voltage 9 V, 12 V and 15 V, respectively. The simulation and experimental results are also almost same.

(b) Variation in input voltage

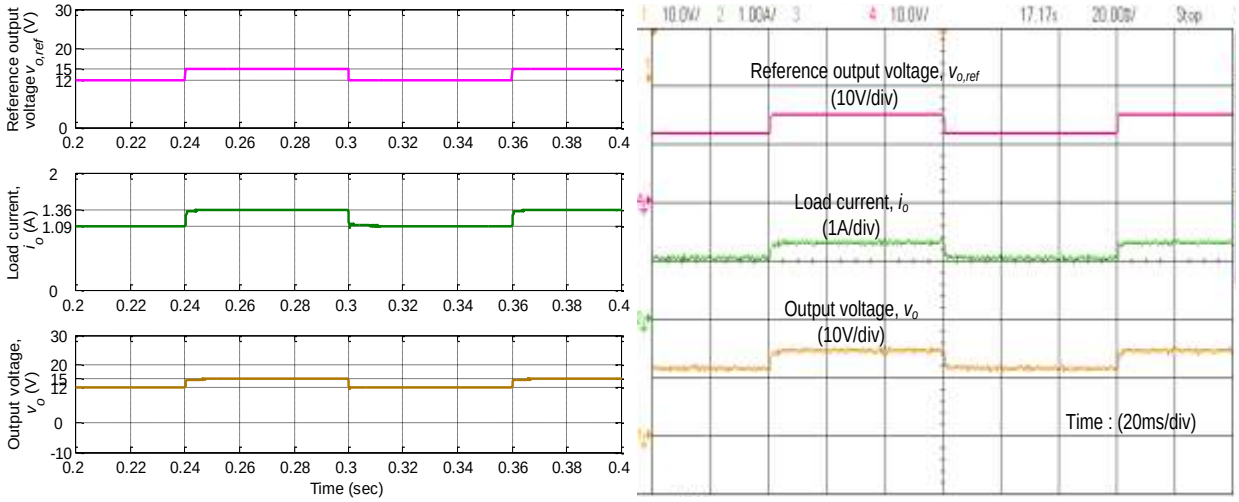
The simulation and experimental results are obtained for step variation in input voltage at fixed load resistance. The variation in input voltage (V_g) is considered from minimum (16 V) to maximum (24 V) and vice-versa for two extreme load conditions R=11 Ω (*i.e.,* maximum load current, 1.09 A) and R=22 Ω (*i.e.,* minimum load current, 0.54 A). The desired output voltage is 12 V.

For the fixed load of 11 Ω, when the input voltage is varied from 16 V to 24 V and vice-versa, the results are shown in Fig. 4.22(a) and Fig. 4.22(b), respectively. Similarly, for the fixed load of 22 Ω, when the input voltage is varied from 16 V to 24 V and vice-versa, the results are shown in Fig. 4.23 (a) and Fig. 4.23 (b), respectively. The results demonstrate that when the input voltage increases from 16 V to 24 V, the output voltage settles within 10 ms with overshoot of 1 V and when the input voltage decreases from 24 V to 16 V, the output voltage settles within 10 ms with undershoot of 1 V. In the experimental results, the step change in input voltage was realized using a manual. So, during the initial part of the transition period, there is a dip in the input voltage before reaching to new input voltage. Therefore, the initial part of transients in the experimental output voltage is ignored while comparing with the simulation.



Simulation Experimental

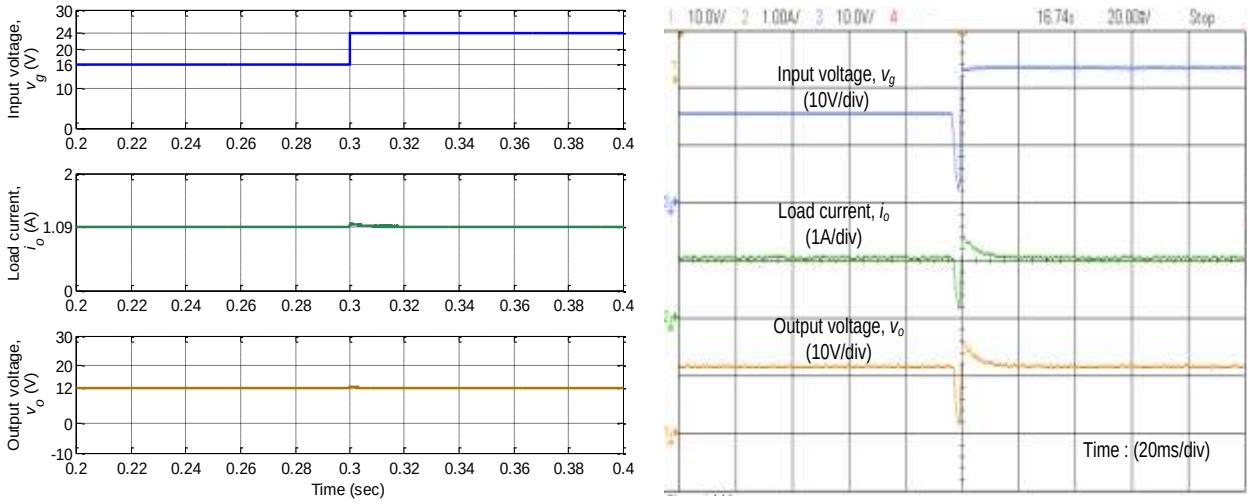
(a)



Simulation Experimental

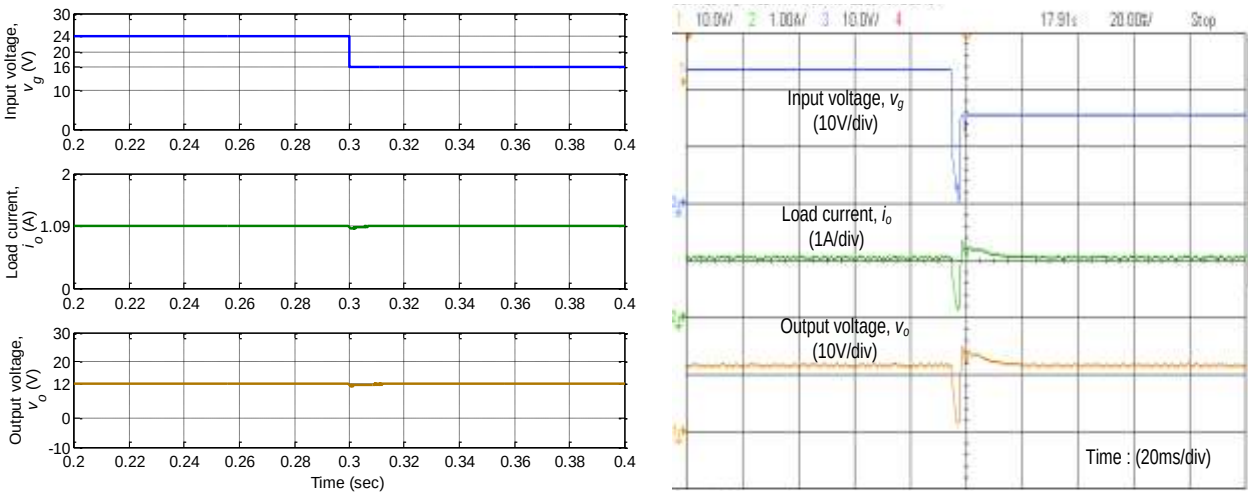
(b)

Fig. 4.21. Simulation and experimental results for reference output voltage variation from (a) 12 V to 9 V and vice-versa (b) 12 V to 15 V and vice-versa



Simulation Experimental

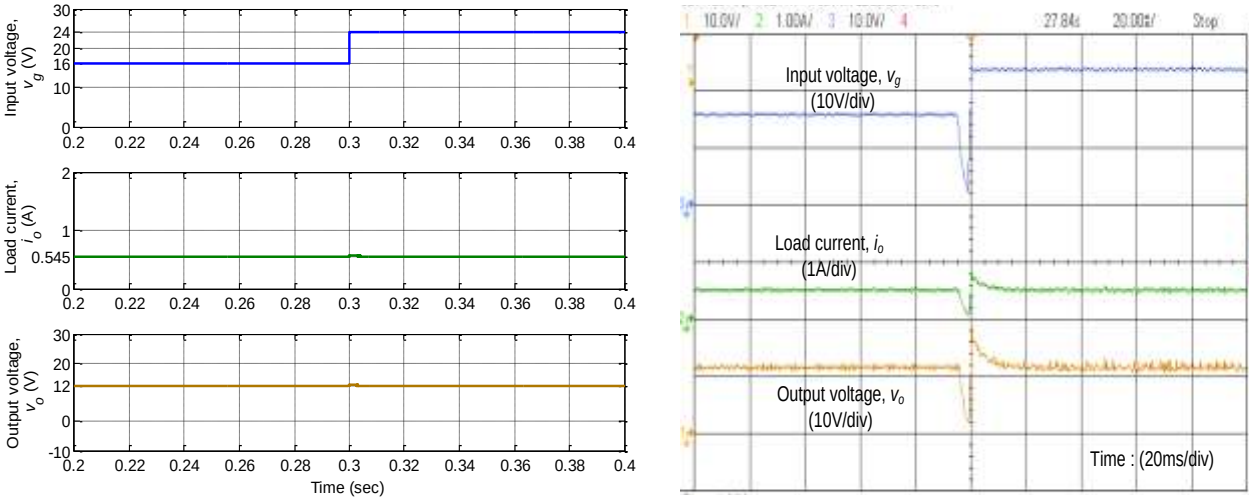
(a)



Simulation Experimental

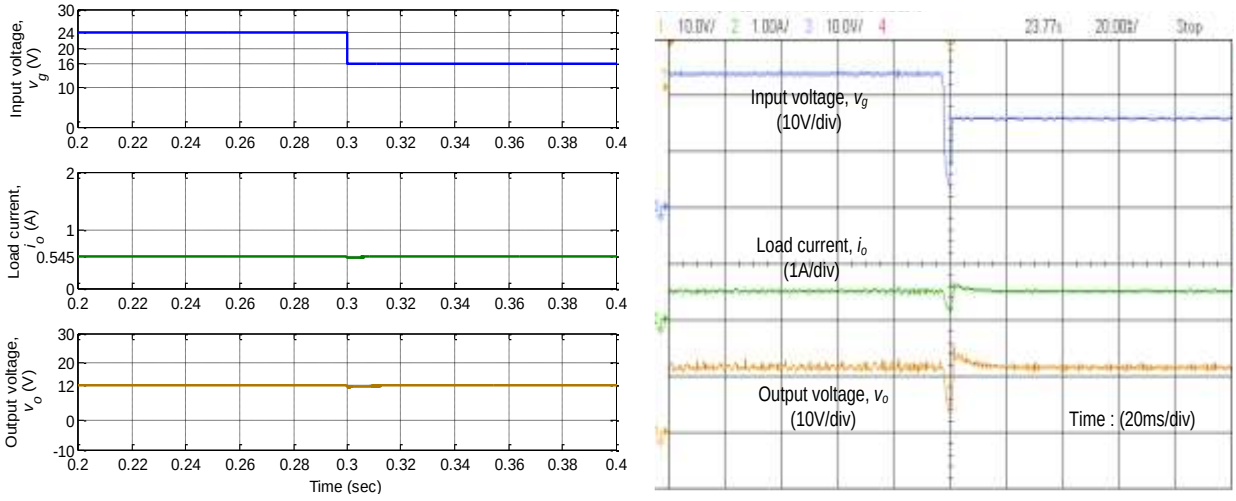
(b)

Fig. 4.22. Simulation and experimental results with R=11 Ω for input voltage variation from (a) 16 V to 24 V (b) 24 V to 16 V



Simulation Experimental

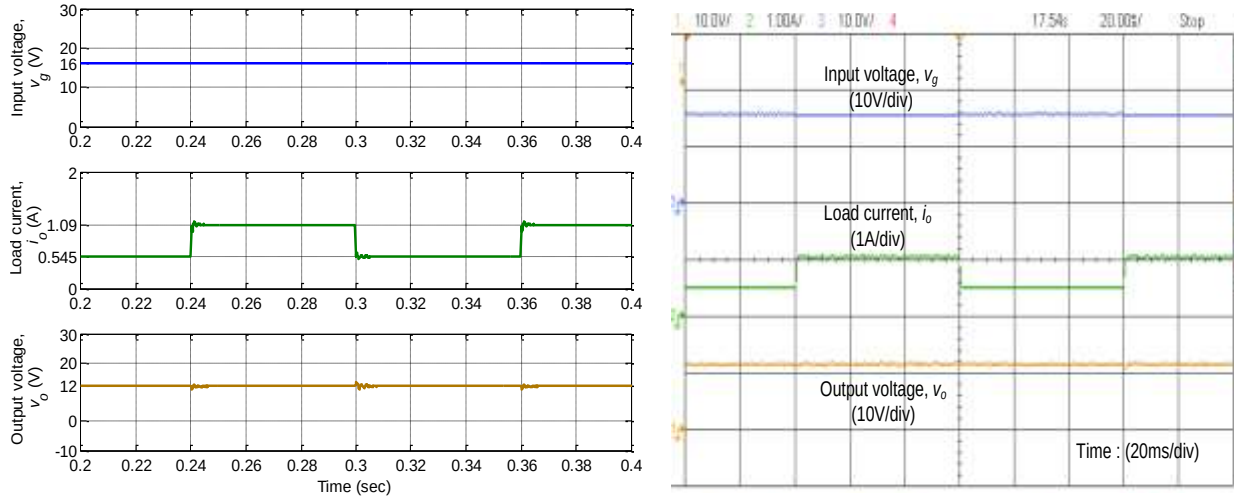
(a)



Simulation Experimental

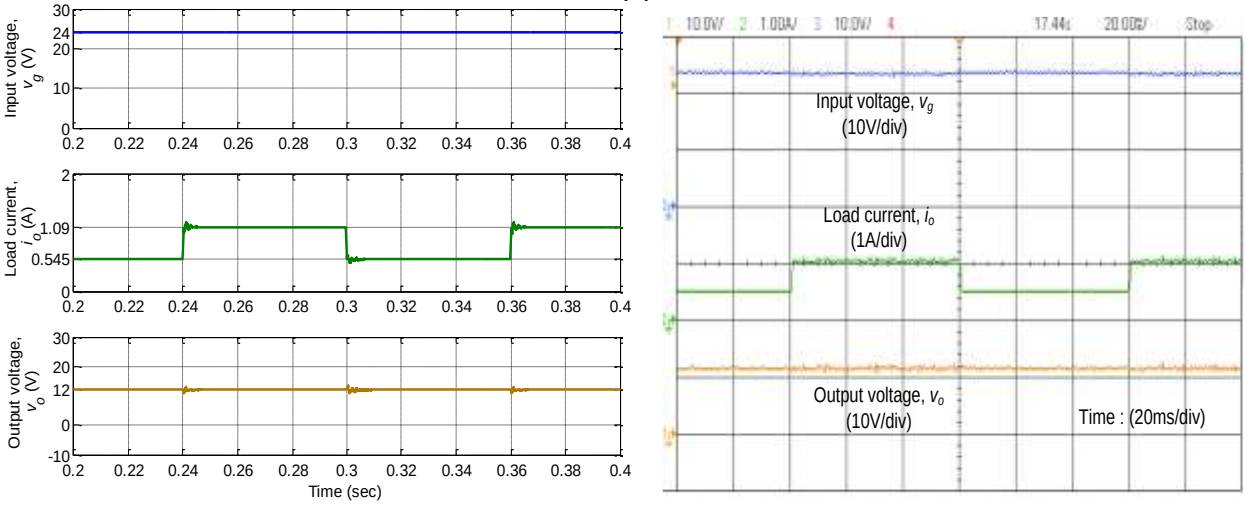
(b)

Fig. 4.23. Simulation and experimental results with R=22 Ω for input voltage variation from (a) 16 V to 24 V (b) 24 V to 16 V



Simulation Experimental

(a)



Simulation Experimental

(b)

Fig. 4.24. Simulation and experimental results for variation in load resistance from 22 Ω to 11 Ω and vice-versa at input voltage (a) V_g=16 V (b) V_g=24 V

(c) Variation in load resistance or load current

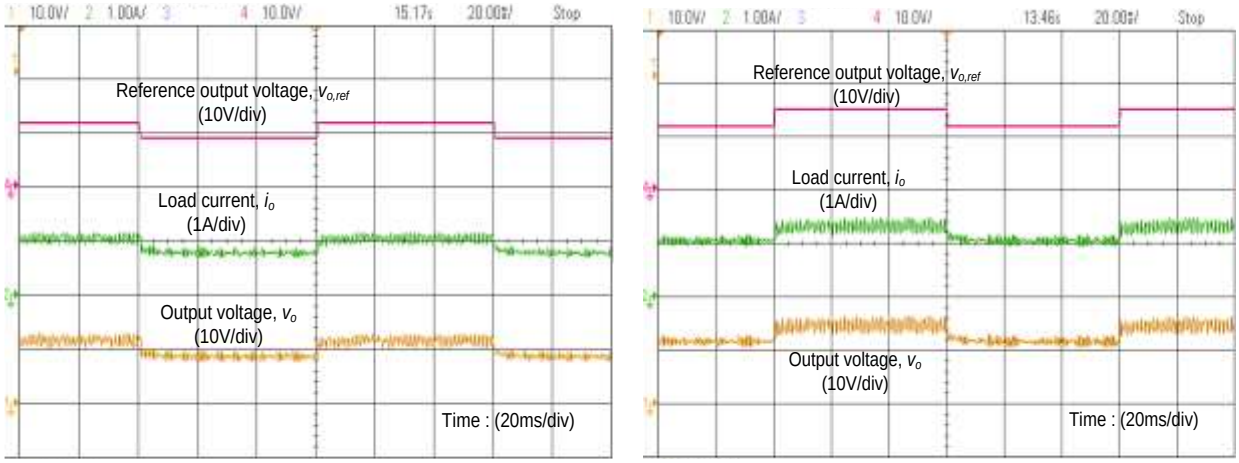
In this section, the performance of PI-lead controller is observed for variations in load resistance while keeping the input voltage constant. The load resistance (R) is varied from 22 Ω (*i.e.*, minimum load current, 0.54 A) to 11 Ω (*i.e.,* maximum load current, 1.09 A) and vice-versa for two extreme input voltages V_g=16 V (minimum) and V_g=24 V (maximum). The desired output voltage is 12 V. The simulation and experimental results for step variation in load resistance from 22 Ω to 11 Ω and vice-versa at constant input voltage 16 V are displayed in Fig. 4.24(a) and at constant input voltage 24 V are displayed in Fig. 4.24(b). As seen, when the load is switched from 22 Ω to 11 Ω and vice-versa, the output voltage experiences the overshoots and undershoots with oscillations and settles to 12 V within 10 ms. The maximum value of overshoots or undershoots is 2 V. The experimental results verify the MATLAB simulation results.

The PI-lead controller designed in (4.53) results in phase margin of 75° and 2 kHz for compensated buck converter. With the simulation and experimental results, it was observed that the output voltage settles within 10 ms under different working conditions. With PI controller, the settling time was observed 15-20 ms. Therefore, the settling time has been improved with PI-lead controller. This improvement appears because the gain crossover frequency of compensated buck converter was 2 kHz with PI-lead controller in comparison to low crossover frequency with PI controller.

In order to verify the performance of PI-lead controller at 4 kHz gain crossover frequency, the experimental results are obtained. The transfer function of the PI-lead controller 4 kHz gain crossover frequency is derived using the algorithm proposed in section 4.2.2.1, keeping f_z=40 Hz and φ_{margin}=75°. The transfer function is

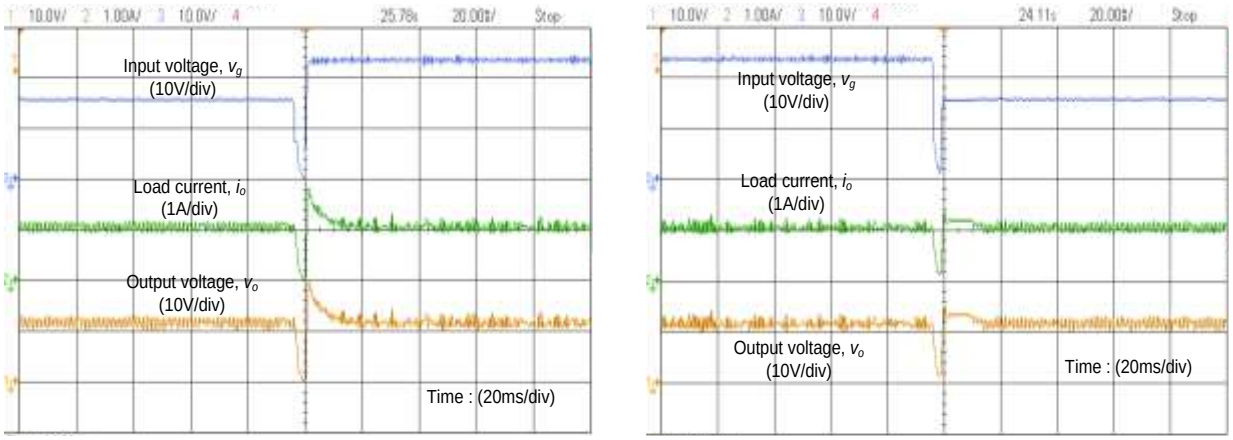
$$G_{PI-lead}(s)=\frac{1671.5\times(0.003979s+1)\left(s+1.18\times10^{4}\right)}{s\left(s+5.354\times10^{4}\right)} \tag{4.55}$$

The experimental results are obtained under different working conditions by implementing the PI-lead controller in (4.55) on the buck converter prototype using dSPACE system. These results are shown in Fig. 4.25 to Fig. 4.28 for variations in reference output voltage, input voltage and load current. All these results demonstrate that the output voltage contains large noise. Therefore, it can be concluded that the PI-lead controller designed at higher gain crossover frequency is not a suitable choice for buck converter compensation.



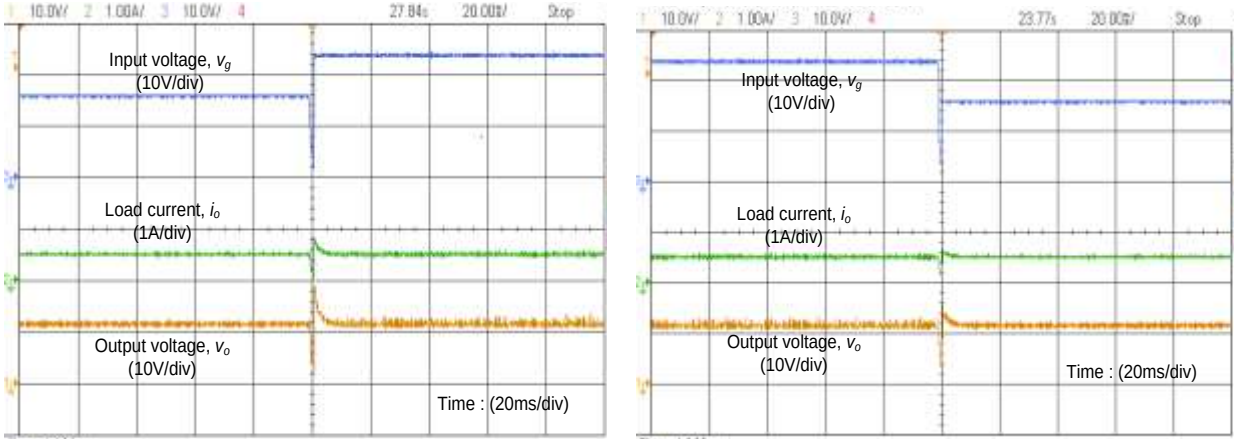
(a) (b)

Fig. 4.25. Experimental results of PI-lead controlled buck converter (at 4 kHz GCF) for reference output voltage variation from (a) 12 V to 9 V and vice-versa (b) 12 V to 15 V and vice-versa



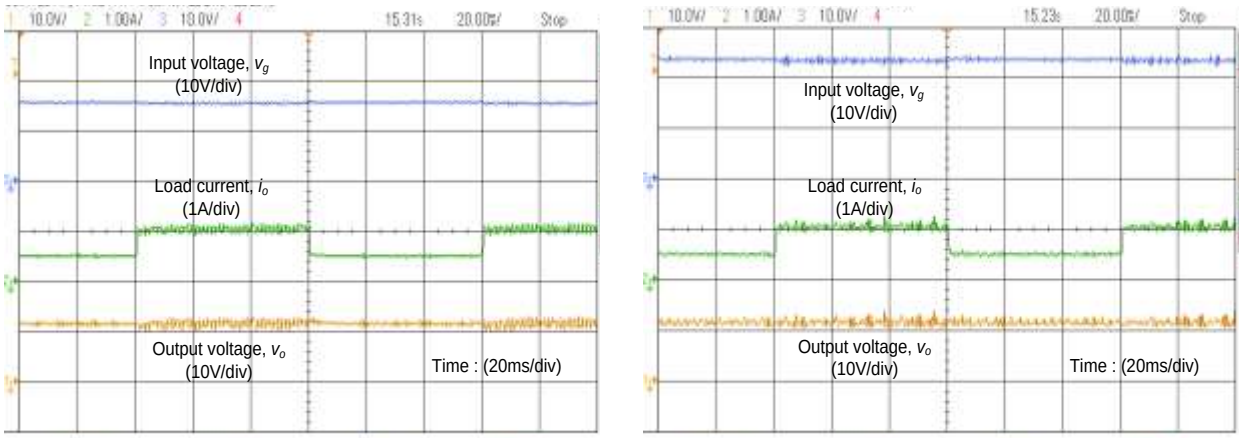
(a) (b)

Fig. 4.26. Experimental results of PI-lead controlled buck converter (at 4 kHz GCF) for load resistance 11 Ω and input voltage variation from (a) 16 V to 24 V (b) 24 V to 16 V



(a) (b)

Fig. 4.27. Experimental results of PI-lead controlled buck converter (at 4 kHz GCF) for load resistance 22 Ω and Input voltage variation from (a) 16 V to 24 V (b) 24 V to 16 V



(a) (b)

Fig. 4.28. Experimental results of PI-lead controlled buck converter (at 4 kHz GCF) for load resistance variation from 22 Ω to 11 Ω and vice-versa at input voltage (a) V_g=16 V (b) V_g=24 V

4.2.3 Two-loop PI controller design

In the previous sections, the output voltage of DC-DC buck converter has been regulated using the PI controller and PI-lead controller. As seen from the results of these two controllers, it was observed that the PI controller eliminates the steady-state error but gives large settling time. Using the PI controller, the phase margin of the compensated system has improved at the cost of reduced gain crossover frequency resulting in slower speed of response. Therefore, to improve the phase margin at desired high crossover frequency, PI-lead controller was suggested. The PI-lead controller provided the improved phase margin at a reasonably good gain crossover frequency. However, as the value of desired gain crossover frequency is increased, there was noise in the regulated output voltage. Thus, the PI-lead controller is good for gain crossover frequency up to 10% of switching frequency. It can be concluded that it is difficult to obtain the large phase margin at high gain crossover frequencies (upto 20-25% of the switching frequency) using a single loop control. Therefore, in this section, two-loop control of DC-DC converters is discussed. In [148], the two-loop control of buck converter was designed using the time domain measures neglecting the effect of converter non-idealities. Moreover the performance was not tested on all possible variations in the operating conditions. In this chapter, the two-loop control for both the DC-DC buck converter and Cuk converter is designed using frequency domain measures and performance is validated experimentally under various operating conditions.

The block diagram of a two-loop control scheme for any DC-DC converter is shown in Fig. 4.29.

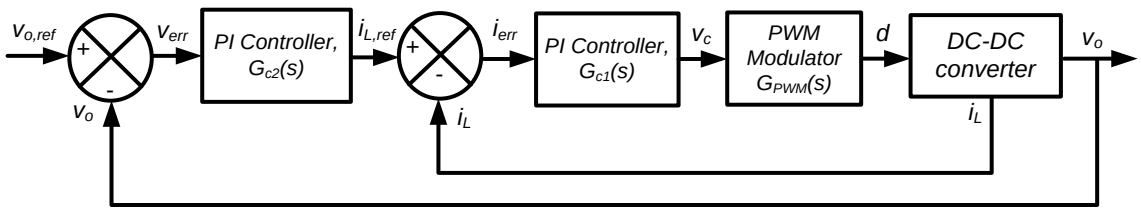


Fig. 4.29. Block diagram of closed two-loop PI control scheme for a DC-DC converter

The two-loop control for a DC-DC converter is composed of one inner current control loop (ICCL) and one outer voltage control loop (OVCL). In each loop, one PI controller is used for loop-shaping. The PI controllers are tuned in such a way that the dynamics of the current control loop is faster than the voltage control loop. As shown in block diagram, in the outer voltage loop, the actual output voltage (v_o) is compared with the reference output voltage ($v_{o,ref}$) and the resultant voltage error is processed through voltage PI controller $G_{c2}(s)$. The function of this PI controller is to set the reference inductor current $i_{L,ref}$. Now the actual inductor current i_L is compared with this reference inductor current $i_{L,ref}$, which gives the current error i_{err}. This current error is fed to PI controller $G_{c1}(s)$, which generates control signal v_c. This control signal is now compared with a fixed frequency, fixed magnitude sawtooth waveform to produce the switching pulses for the switch of DC-DC converter. The duty cycle of switching pulses is continuously monitored to regulate the output voltage in case of any disturbance in the input voltage, load current or reference voltage.

In this scheme, the parameters of the two PI controllers are tuned based on specified phase margin and gain crossover frequency. An algorithm is proposed to derive the analytical formulae for these parameters in terms of specified phase margin and gain crossover frequency. In this chapter, this two-loop control scheme will be used for both DC-DC buck converter and Cuk converter. Therefore, the proposed algorithm is discussed for a generalized fourth-order converter, which can be applied to either of the converter.

4.2.3.1 Proposed PI controller algorithm for specified phase margin and gain crossover frequency

In the two-loop control scheme, two PI controllers are used each for outer voltage control loop and inner current control loop. In this section, for loop shaping of these control loops based on the desired frequency domain specifications, the analytical formulae for PI controller parameters are derived as follows:

Step 1: Consider a generalized linear time-invariant fourth-order system $G(s)$ to be compensated as

$$G(s) = \frac{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0}{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \tag{4.56}$$

The transfer function of a PI controller $G_c(s)$ to compensate this system is

$$G_c(s) = \frac{K_p s + K_i}{s} \tag{4.57}$$

Where, K_p and K_i are proportional and integral gain constants of PI controller.

Step 2: In this step, define the desired phase margin (φ) and corresponding gain crossover frequency (ω_c). Therefore, the PI controller should be tuned in such a way that the compensated system would have a phase margin of φ at crossover frequency ω_c. It is possible only if following two equations are satisfied simultaneously.

$$\left|G(j\omega_c)G_c(j\omega_c)\right| = 1 \tag{4.58}$$

and

$$\angle G(j\omega_c)G_c(j\omega_c) = -180^\circ + \varphi \tag{4.59}$$

Equations (4.58) and (4.59) can be combined as

$$1 + e^{-j\varphi}G(j\omega_c)G_c(j\omega_c) = 0 \tag{4.60}$$

Using Euler's identity function, one can write

$$e^{-j\varphi} = \cos\varphi - j\sin\varphi \tag{4.61}$$

Step 3: Derivation of formulae for K_p and K_i

On substituting (4.56)-(4.57) replaced with $s=j\omega$ and (4.61) into (4.60), we get

$$1 + (\cos\varphi - j\sin\varphi)\frac{b_4\omega_c^4 - b_3 j\omega_c^3 - b_2\omega_c^2 + b_1 j\omega_c + b_0}{a_4\omega_c^4 - a_3 j\omega_c^3 - a_2\omega_c^2 + a_1 j\omega_c + a_0}\left(\frac{K_p j\omega_c + K_i}{j\omega_c}\right) = 0 \tag{4.62}$$

$$\begin{aligned}\Rightarrow\ & j\omega_c\left(a_4\omega_c^4 - a_3 j\omega_c^3 - a_2\omega_c^2 + a_1 j\omega_c + a_0\right) + (\cos\varphi - j\sin\varphi)\cdot \\ & \left(b_4\omega_c^4 - b_3 j\omega_c^3 - b_2\omega_c^2 + b_1 j\omega_c + b_0\right)\left(K_p j\omega_c + K_i\right) = 0\end{aligned} \tag{4.63}$$

On simplifying above equation, we get

$$\begin{aligned}& K_p\left[-\omega_c^2\left(-b_3\omega_c^2 + b_1\right)\cos\varphi + \omega_c\left(b_4\omega_c^4 - b_2\omega_c^2 + b_0\right)\sin\varphi\right] + \\ & K_i\left[\left(b_4\omega_c^4 - b_2\omega_c^2 + b_0\right)\cos\varphi + \omega_c\left(-b_3\omega_c^2 + b_1\right)\sin\varphi\right] - \omega_c^2\left(-a_3\omega_c^2 + a_1\right) + \\ & jK_p\left[\omega_c^2\left(-b_3\omega_c^2 + b_1\right)\sin\varphi + \omega_c\left(b_4\omega_c^4 - b_2\omega_c^2 + b_0\right)\cos\varphi\right] + \\ & jK_i\left[-\left(b_4\omega_c^4 - b_2\omega_c^2 + b_0\right)\sin\varphi + \omega_c\left(-b_3\omega_c^2 + b_1\right)\cos\varphi\right] + j\omega_c\left(a_4\omega_c^4 - a_2\omega_c^2 + a_0\right) = 0\end{aligned} \tag{4.64}$$

Equating real and imaginary parts of (4.64) and then simplifying yields

$$K_p(\omega_c,\varphi) = \frac{\left(q_8\cos\varphi\omega_c^8 + q_7\sin\varphi\omega_c^7 + q_6\cos\varphi\omega_c^6 + q_5\sin\varphi\omega_c^5 + q_4\cos\varphi\omega_c^4 + q_3\sin\varphi\omega_c^3 + q_2\cos\varphi\omega_c^2 + q_1\sin\varphi\omega_c + q_0\cos\varphi\right)}{-\left(p_8\omega_c^8 + p_6\omega_c^6 + p_4\omega_c^4 + p_2\omega_c^2 + p_0\right)} \tag{4.65}$$

$$K_i(\omega_c,\varphi) = \frac{\omega_c\left(-q_8\sin\varphi\omega_c^8 + q_7\cos\varphi\omega_c^7 - q_6\sin\varphi\omega_c^6 + q_5\cos\varphi\omega_c^5 - q_4\sin\varphi\omega_c^4 + q_3\cos\varphi\omega_c^3 - q_2\sin\varphi\omega_c^2 + q_1\cos\varphi\omega_c - q_0\sin\varphi\right)}{-\left(p_8\omega_c^8 + p_6\omega_c^6 + p_4\omega_c^4 + p_2\omega_c^2 + p_0\right)} \tag{4.66}$$

Where,

$$\begin{aligned}& q_8 = a_4b_4, q_7 = -a_4b_3 + a_3b_4, q_6 = -a_4b_2 + a_3b_3 - a_2b_4, q_5 = a_4b_1 - a_3b_2 + a_2b_3 - a_1b_4, \\ & q_4 = a_4b_0 - a_3b_1 + a_2b_2 - a_1b_3 + a_0b_4, q_3 = a_3b_0 - a_2b_1 + a_1b_2 - a_0b_3, \\ & q_2 = -a_2b_0 + a_1b_1 - a_0b_2, q_1 = -a_1b_0 + a_0b_1, q_0 = a_0b_0 \\ & p_8 = b_4^2, p_6 = b_3^2 - 2b_2b_4, p_4 = b_2^2 + 2(b_0b_4 - b_1b_3), p_2 = b_1^2 - 2b_0b_2, p_0 = b_0^2\end{aligned}$$

Equations (4.65) and (4.66) give the generalized formulae for tuning parameter K_p and K_i in terms of system parameters and desired frequency domain specifications (Phase

margin and gain crossover frequency). These formulae will be used in subsequent sections to design current control loop and voltage control loop for DC-DC buck and Cuk converter. However, these formulae may also be applied to other types of DC-DC converters.

4.2.3.2 Two-loop control scheme for DC-DC buck converter

In this section, the implementation of two-loop PI control scheme for DC-DC buck converter is carried out. The parameters for the two PI controllers are tuned using the proposed tuning formulae. The block diagram of the control scheme for buck converter is shown in Fig. 4.30. As shown in the block diagram, the PI current controller $G_{c1}(s)$ is designed based on duty cycle to inductor current transfer function $G_{id}(s)$ and PI voltage controller $G_{c2}(s)$ is tuned based on inductor current to output voltage transfer function $G_{vi}(s)$. The detailed schematic of this two-loop control scheme for buck converter is shown in Fig. 4.31.

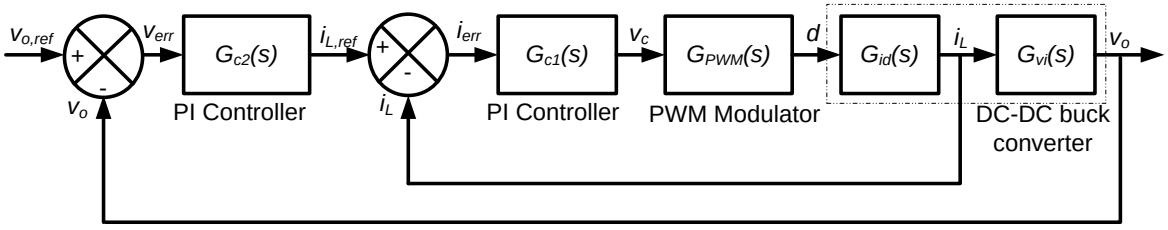


Fig. 4.30. Complete block diagram of closed two-loop controlled DC-DC buck converter

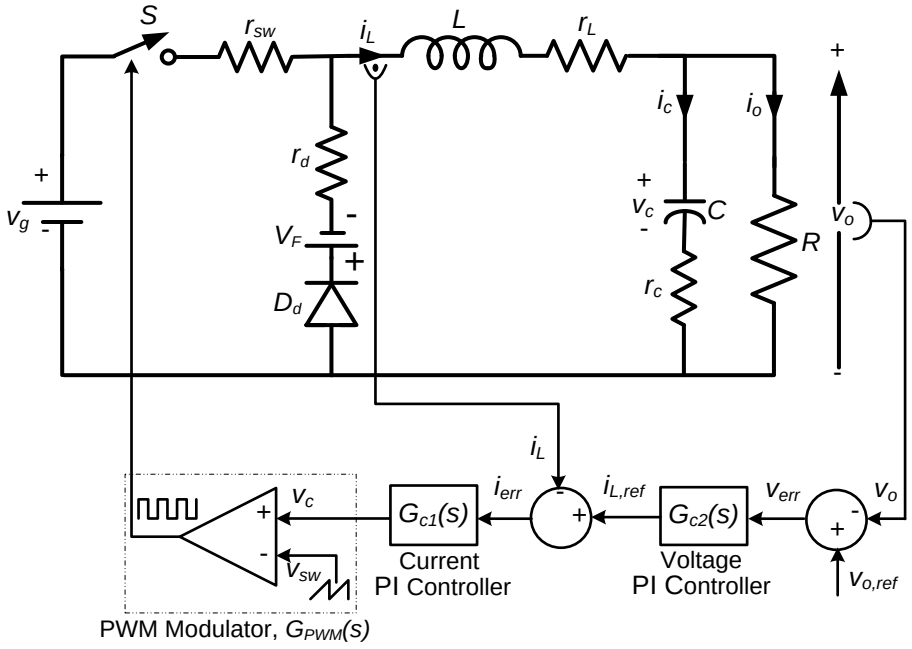


Fig. 4.31. Detailed schematic for closed two-loop PI control of DC-DC buck converter

The buck converter specifications are kept same as given in Table 4.1. The different transfer functions of buck converter required for this control scheme are obtained using the derivations carried out in chapter 3. Therefore, substituting V_g=16 V and R=11 Ω and other buck converter parameters, we get

Duty cycle to output voltage transfer function

$$G_{vd}(s)=\frac{\tilde{v}_o(s)}{\tilde{d}(s)}=\frac{4428s+1.757\times10^8}{s^2+1518s+1.074\times10^7} \tag{4.67}$$

Duty cycle to inductor current transfer function

$$G_{id}(s)=\frac{\tilde{i}_L(s)}{\tilde{d}(s)}=\frac{1.516\times10^4 s+1.597\times10^7}{s^2+1518s+1.074\times10^7} \tag{4.68}$$

Inductor current to output voltage transfer function

$$G_{vi}(s)=\frac{\tilde{v}_o(s)}{\tilde{i}_L(s)}=\frac{4428s+1.757\times10^8}{1.516\times10^4 s+1.597\times10^7} \tag{4.69}$$

(a) Inner current control loop (ICCL) design

The block diagram of inner current control loop is shown in Fig. 4.32. In this control loop, the actual inductor current i_L is compared with the reference inductor current $i_{L,ref}$. The resultant inductor current error is passed through PI controller $G_{c1}(s)$. The output of PI controller is compared (in PWM modulator block) with the sawtooth waveform of fixed magnitude and frequency to generate the switching pulses of desired duty cycle.

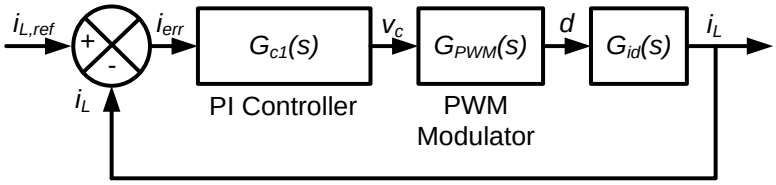


Fig. 4.32. Block diagram of inner current control loop for DC-DC buck converter

In this case, the loop transfer function of uncompensated system is

$$T_1(s)=G_{PWM}(s)G_{id}(s) \tag{4.70}$$

Here, $G_{PWM}(s)=1/V_{sw}$ is the transfer function of PWM modulator, V_{sw} is peak value of the sawtooth waveform. V_{sw} =1 is taken in this design.

Therefore, for the buck converter under consideration, the loop transfer function without compensation is

$$T_1(s)=G_{id}(s)=\frac{1.516\times10^4 s+1.597\times10^7}{s^2+1518s+1.074\times10^7} \tag{4.71}$$

The frequency response of $T_1(s)$ is shown in Fig. 4.33. It has phase margin of 91.9° at 2.52 kHz gain crossover frequency and constant low-frequency gain. The phase margin is good but due to constant low-frequency gain, it will have steady-state error in inductor current. Therefore, a PI controller $G_{c1}(s)$ is designed to increase the low-frequency gain and thus, to reduce the steady-state error between actual inductor current and reference inductor current. Let the transfer function of $G_{c1}(s)$ be

$$G_{c1}(s)=\frac{K_{p1}s+K_{i1}}{s} \tag{4.72}$$

Comparing (4.71) with (4.56), we get

$$b_4=0, b_3=0, b_2=0, b_1=1.516\times10^4, b_0=1.597\times10^7, a_4=0, a_3=0, a_2=1, a_1=1518, a_0=1.074\times10^7 \quad (4.73)$$

The PI controller parameters are tuned using the proposed formulae in terms of specified frequency domain measures. Therefore, substituting values of coefficients from (4.73) into (4.65)-(4.66), we get

$$K_{p1}(\omega_c,\varphi)=\frac{\left(-1.52\times10^4\sin\varphi\omega_c^3+7.04\times10^6\cos\varphi\omega_c^2+1.38\times10^{11}\sin\varphi\omega_c+1.71\times10^{14}\cos\varphi\right)}{-\left(2.298\times10^8\omega_c^2+2.55\times10^{14}\right)} \quad (4.74)$$

$$K_{i1}(\omega_c,\varphi)=\frac{\omega_c\left(-1.52\times10^4\sin\varphi\omega_c^3-7.04\times10^6\cos\varphi\omega_c^2+1.38\times10^{11}\sin\varphi\omega_c-1.71\times10^{14}\cos\varphi\right)}{-\left(2.298\times10^8\omega_c^2+2.55\times10^{14}\right)} \quad (4.75)$$

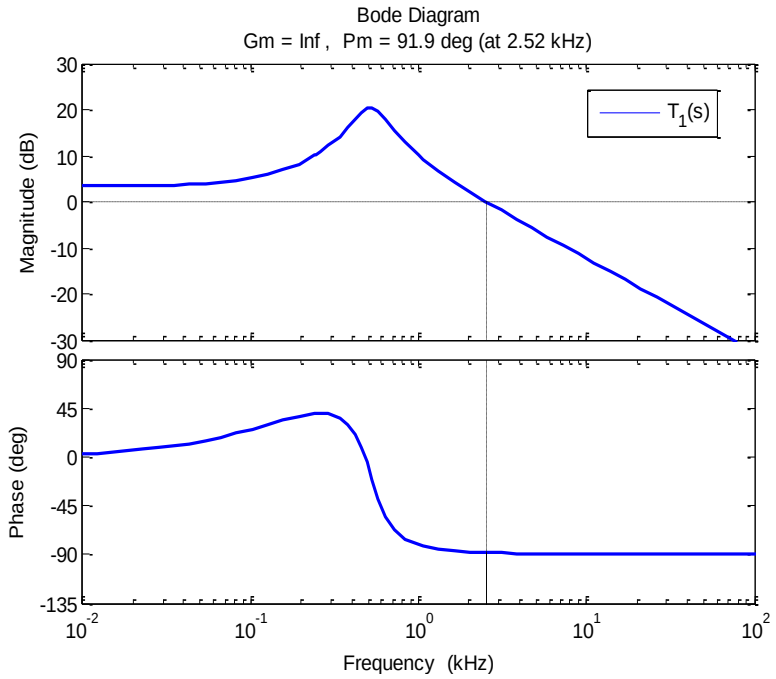


Fig. 4.33. Frequency response of uncompensated current control loop of buck converter

For inner current control loop, PI controller parameters are tuned to achieve phase margin of 75° at 4 kHz gain crossover frequency. Therefore, substituting $\omega_c=2\pi.4\text{x}10^3 = 8000\pi$ and $\varphi=75°$ in (4.74) and (4.75), we get $K_{p1}=1.567$ and $K_{i1}=1.138\text{x}10^4$.

The frequency response of compensated current control loop is shown in Fig. 4.34. It shows that the desired phase margin and gain crossover frequency is obtained and gain in low-frequency region has been improved.

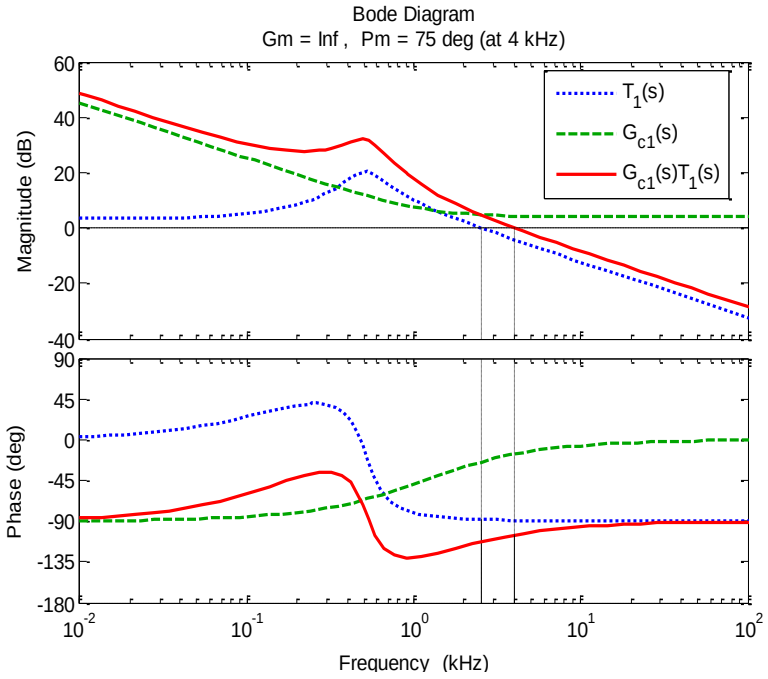


Fig. 4.34. Frequency response of compensated current control loop of buck converter

(b) Outer voltage control loop (OVCL) design

The block diagram of the outer voltage control loop of buck converter is shown in Fig. 4.35. The function of outer voltage control loop (OVCL) is to generate the reference inductor current $i_{L,ref}$. In this control loop, the actual output voltage v_o is compared with the reference output voltage $v_{o,ref}$. The resultant voltage error is passed through PI controller $G_{c21}(s)$. The output of the PI controller serves as reference inductor current for the inner current control loop.

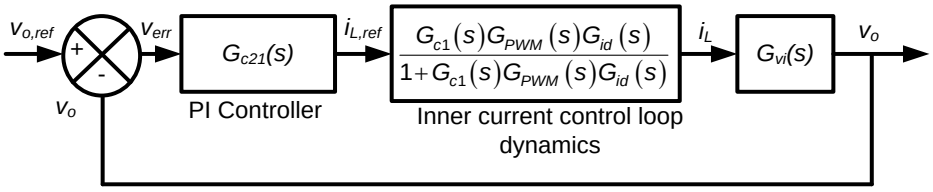


Fig. 4.35. Block diagram of outer voltage control loop of DC-DC buck converter

The closed-loop dynamics of compensated current control loop can be collectively written as

$$\frac{T_1(s)G_{c1}(s)}{1+T_1(s)G_{c1}(s)} = \frac{G_{c1}(s)G_{PWM}(s)G_{id}(s)}{1+G_{c1}(s)G_{PWM}(s)G_{id}(s)} \tag{4.76}$$

Therefore, the loop transfer function of uncompensated voltage control loop will be

$$T_2(s) = \frac{G_{c1}(s)G_{PWM}(s)G_{id}(s)}{1+G_{c1}(s)G_{PWM}(s)G_{id}(s)} \cdot G_{vi}(s) \tag{4.77}$$

Substituting the corresponding transfer functions from (4.71) and (4.72) into above equation, we get

$$T_2(s) = \frac{1.052\times10^8 s^3 + 5.049\times10^{12} s^2 + 3.552\times10^{16} s + 3.194\times10^{19}}{1.52\times10^4 s^4 + 3.99\times10^8 s^3 + 3.56\times10^{12} s^2 + 6.08\times10^{15} s + 2.9\times10^{18}} \tag{4.78}$$

The frequency response of $T_2(s)$ is shown in Fig. 4.36. It has phase margin of 85° at 2.16 kHz gain crossover frequency and constant low-frequency gain. The phase margin is good but due to constant low-frequency gain, it will have steady-state error in output voltage. Moreover, in two-loop control, the gain crossover frequency of outer voltage loop is kept relatively lower than the inner current control loop. Therefore, a PI controller $G_{c21}(s)$ is designed to increase the low-frequency gain and to adjust the desired phase margin at lower gain crossover frequency. Let the transfer function of $G_{c21}(s)$ be

$$G_{c21}(s)=\frac{K_{p21}s+K_{i21}}{s} \tag{4.79}$$

Comparing (4.78) with (4.56), we get

$$\begin{aligned} &b_4=0, b_3=1.052\times10^8, b_2=5.049\times10^{12}, b_1=3.552\times10^{16}, b_0=3.194\times10^{19},\\ &a_4=1.52\times10^4, a_3=3.99\times10^8, a_2=3.56\times10^{12}, a_1=6.08\times10^{15}, a_0=2.9\times10^{18} \end{aligned} \tag{4.80}$$

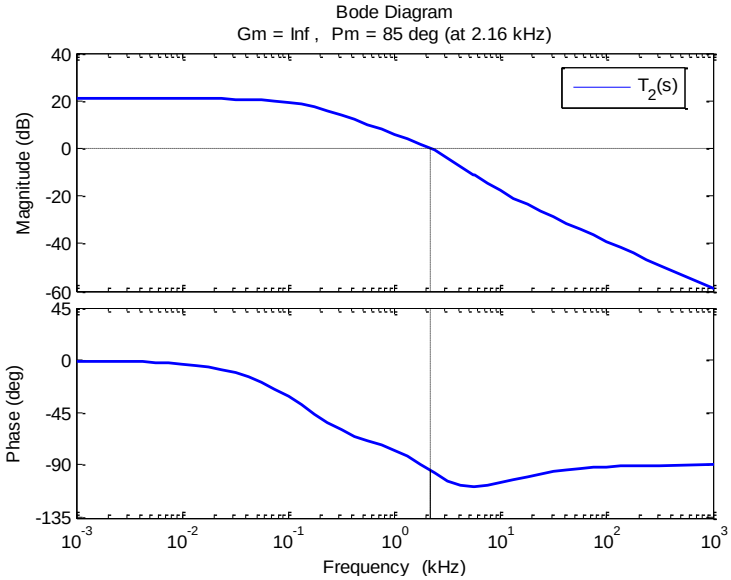


Fig. 4.36. Frequency response of uncompensated voltage control loop of buck converter

This PI controller parameters are tuned using the proposed formulae in terms of specified frequency domain measures. Therefore, substituting values of coefficients from (4.80) into (4.65)-(4.66), we get

$$K_{p21}(\omega_c,\varphi)=\frac{\left(\begin{array}{c}-1.59\times10^{12}\sin\varphi\omega_c^7-3.45\times10^{16}\cos\varphi\omega_c^6-1.1\times10^{21}\sin\varphi\omega_c^5+3.65\times10^{24}\cos\phi\omega_c^4-\\ 8.33\times10^{28}\sin\varphi\omega_c^3+8.76\times10^{31}\cos\varphi\omega_c^2-9.12\times10^{34}\sin\varphi\omega_c+9.27\times10^{37}\cos\varphi\end{array}\right)}{-\left(1.017\times10^{16}\omega_c^6+1.8\times10^{25}\omega_c^4+9.39\times10^{32}\omega_c^2+1.02\times10^{39}\right)} \tag{4.81}$$

$$K_{i21}(\omega_c,\varphi)=\frac{\omega_c\left(\begin{array}{c}-1.59\times10^{12}\sin\varphi\omega_c^7+3.45\times10^{16}\cos\varphi\omega_c^6-1.1\times10^{21}\sin\varphi\omega_c^5-3.65\times10^{24}\cos\phi\omega_c^4-\\ 8.33\times10^{28}\sin\varphi\omega_c^3-8.76\times10^{31}\cos\varphi\omega_c^2-9.12\times10^{34}\sin\varphi\omega_c-9.27\times10^{37}\cos\varphi\end{array}\right)}{-\left(1.017\times10^{16}\omega_c^6+1.8\times10^{25}\omega_c^4+9.39\times10^{32}\omega_c^2+1.02\times10^{39}\right)} \tag{4.82}$$

The PI controller for voltage control loop is designed to have phase margin of 75° at 50 Hz gain crossover frequency, which is much lower than 4 kHz, the gain crossover frequency of current control loop. Therefore, substituting ω_c=100π and φ=75° in (4.81) and (4.82), we get K_{p21}=0.0035 and K_{i21}=29.92.

The frequency response of compensated voltage control loop is shown in Fig. 4.37. It can be observed that the compensated voltage control loop has achieved the specified phase margin at desired gain crossover frequency and high gain with -20 dB/decade slope in low-frequency region.

Since, in Fig. 4.35, the inner current loop dynamics is always faster than the outer voltage loop dynamics, therefore, it can be neglected in comparison to voltage control loop to simplify the voltage control loop design. Therefore, the corresponding block diagram in this case is shown in Fig. 4.38. The loop transfer function of uncompensated voltage control loop in this case is same as the inductor current to output voltage transfer function $G_{vi}(s)$ given in (4.69).

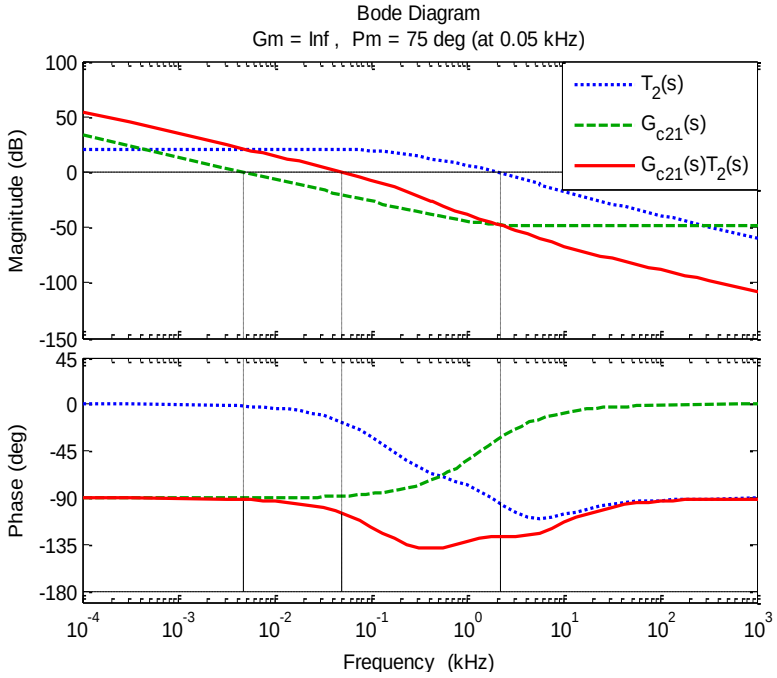


Fig. 4.37. Frequency response of compensated voltage control loop of buck converter

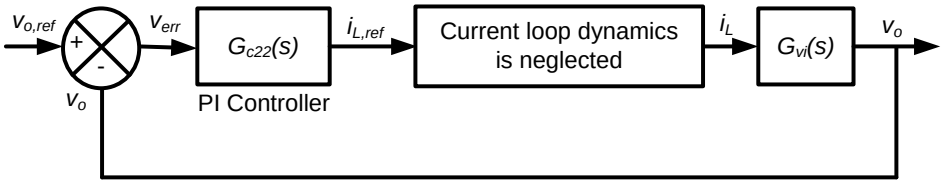


Fig. 4.38. Block diagram of outer voltage control loop of DC-DC buck converter when inner current loop dynamics is neglected

The frequency response of $G_{vi}(s)$ is shown in Fig. 4.39. It has phase margin of 112° at 1.92 kHz gain crossover frequency and constant low-frequency gain. Similar to previous case (where current dynamics was not neglected), to increase the gain in low-frequency region a PI controller $G_{c22}(s)$ is designed. Let the transfer function of $G_{c22}(s)$ be

$$G_{c22}(s) = \frac{K_{p22}s + K_{i22}}{s} \tag{4.83}$$

Comparing (4.69) with (4.56),

$$b_4 = 0, b_3 = 0, b_2 = 0, b_1 = 4428, b_0 = 1.757 \times 10^8,$$
$$a_4 = 0, a_3 = 0, a_2 = 0, a_1 = 1.516 \times 10^4, a_0 = 1.597 \times 10^7 \quad (4.84)$$

Replacing these values of coefficients from (4.84) into (4.65)-(4.66), we get

$$K_{p22}(\omega_c, \varphi) = \frac{\left(6.44 \times 10^7 \cos\varphi\omega_c^2 - 2.59 \times 10^{12} \sin\varphi\omega_c + 2.81 \times 10^{15} \cos\varphi\right)}{-\left(1.804 \times 10^7 \omega_c^2 + 3.087 \times 10^{16}\right)} \quad (4.85)$$

$$K_{i22}(\omega_c, \varphi) = \frac{\omega_c\left(-6.44 \times 10^7 \sin\varphi\omega_c^2 - 2.59 \times 10^{12} \cos\varphi\omega_c - 2.81 \times 10^{15} \sin\varphi\right)}{-\left(1.804 \times 10^7 \omega_c^2 + 3.087 \times 10^{16}\right)} \quad (4.86)$$

To achieve the desired phase margin of 75° at 50 Hz gain crossover frequency, we substitute ω_c=100π and φ=75° in (4.85) and (4.86). It gives K_{p22}=0.0019 and K_{i22}=29.79.

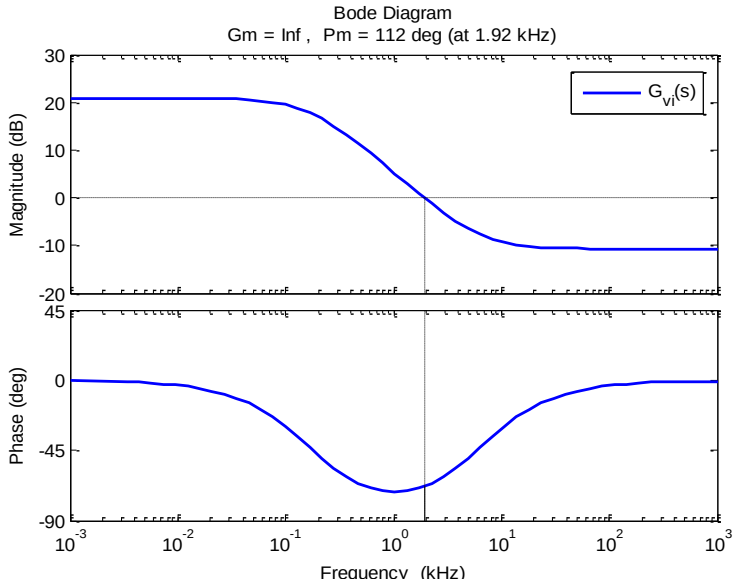


Fig. 4.39. Frequency response of uncompensated voltage control loop of buck converter when inner current loop dynamics is neglected

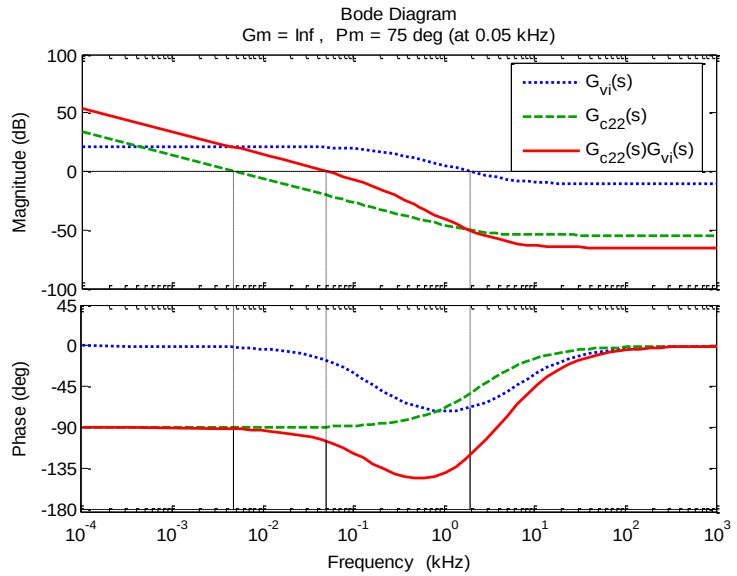


Fig. 4.40. Frequency response of compensated voltage control loop of buck converter when inner current loop dynamics is neglected

The frequency response of compensated outer voltage control loop with neglected current loop dynamics is shown in Fig. 4.40. The required phase margin, gain crossover frequency are achieved and low-frequency gain has been increased with -20 dB/decade slope.

The frequency response of the compensated voltage control loop with PI controllers $G_{c21}(s)$ and $G_{c22}(s)$ is compared in Fig. 4.41. As shown in the figure, if the PI controller $G_{c22}(s)$ is applied to voltage control loop $T_2(s)$, in which the inner current loop dynamics is not neglected, the phase margin is 74.1° and gain crossover frequency is 49.8 Hz. These frequency domain specifications are very close to desired specification (phase margin 75° and gain crossover frequency is 50 Hz). It validates that the dynamics of current control loop is faster than the voltage control loop and therefore, can be neglected to simplify the analysis and design of PI controller for outer voltage control loop.

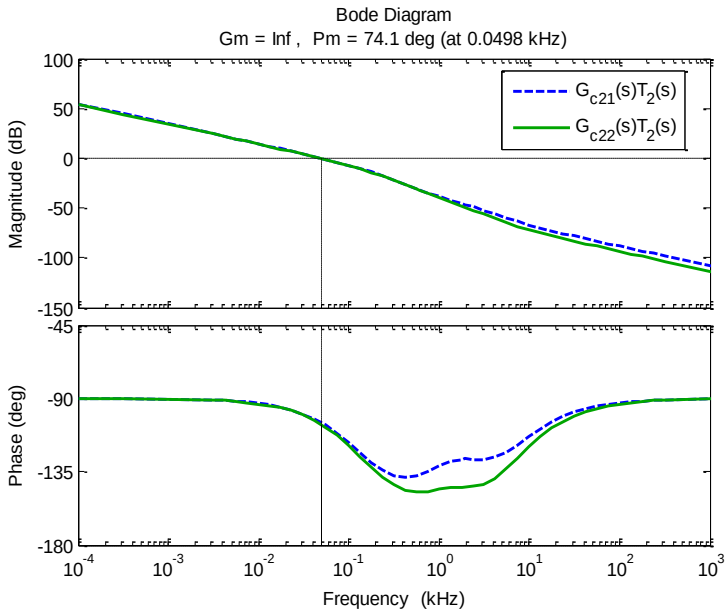


Fig. 4.41. Comparison of frequency responses of compensated voltage control loop of buck converter with PI controllers $G_{c21}(s)$ and $G_{c22}(s)$

4.2.3.3 Results and discussion

In this section, the performance of two-loop PI control of buck converter is tested under different operating conditions. The simulation and experimental result are obtained and discussed. The simulation is carried out using MATLAB/Simulink software. The voltage loop and current loop PI controllers are implemented on buck converter prototype using dSPACE system. The inductor current and output voltage are sensed using current and voltage sensors and fed to dSPACE controller via ADC channels. The detailed discussions on the hardware implementation are given in Appendix *B*.

The simulation and experimental results are attained for three different conditions:

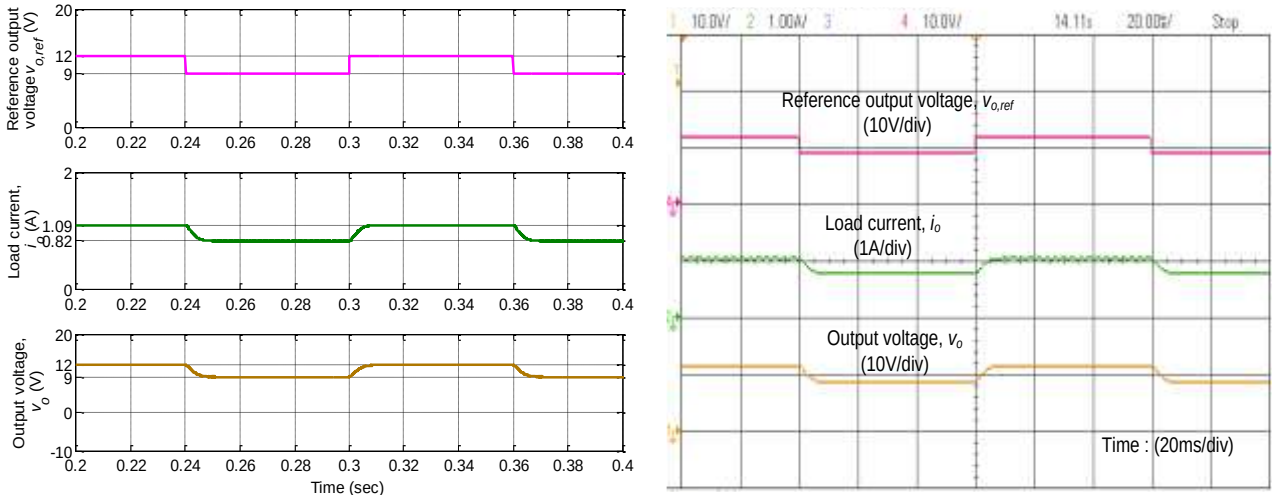
(a) Variation in reference output voltage

(b) Variation in input voltage

(c) Variation in load current

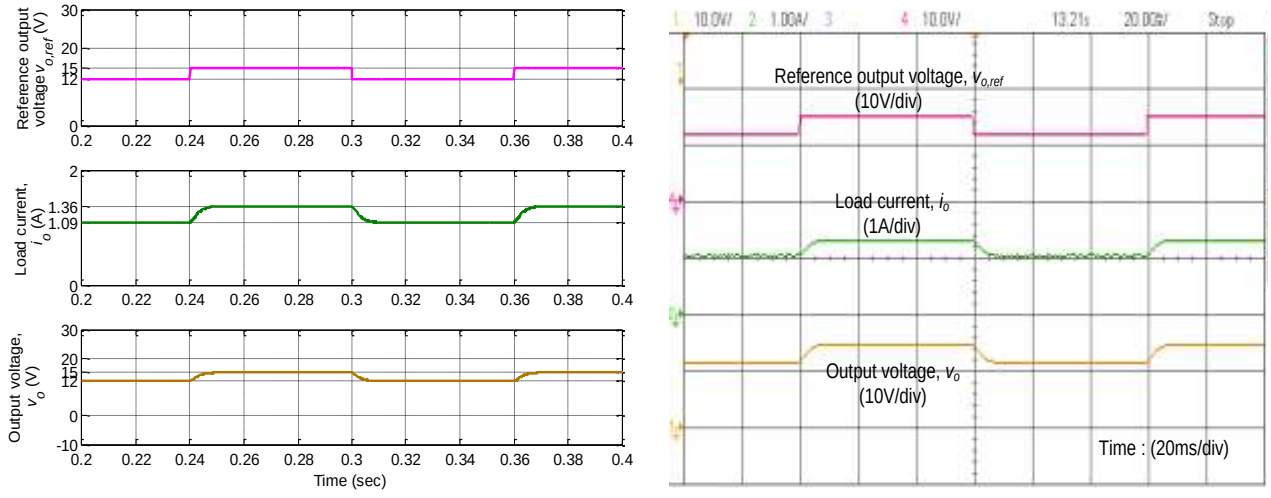
(a) Variation in reference output voltage

In this case, the reference output voltage is varied while keeping the input voltage (V_g) and load resistance (R) constant to 16 V and 11 Ω, respectively. For reference voltage variation from 12 V to 9 V and vice-versa, the simulation and experimental results are shown in Fig. 4.42(a). Similarly, for reference voltage variation from 12 V to 15 V and vice-versa, the corresponding simulation and experimental results are shown in Fig. 4.42 (b). It is observed that the output voltage smoothly settles to steady-state (12 V) within 5-7 ms without any oscillation and undershoot/overshoot. The load current is 0.82 A, 1.09 A and 1.36 A for desired output voltage 9 V, 12 V and 15 V, respectively. The simulation and experimental results match very closely.



Simulation Experimental

(a)



Simulation Experimental

(b)

Fig. 4.42. Simulation and experimental results for reference output voltage variation from (a) 12 V to 9 V and vice-versa (b) 12 V to 15 V and vice-versa

(b) Variation in input voltage

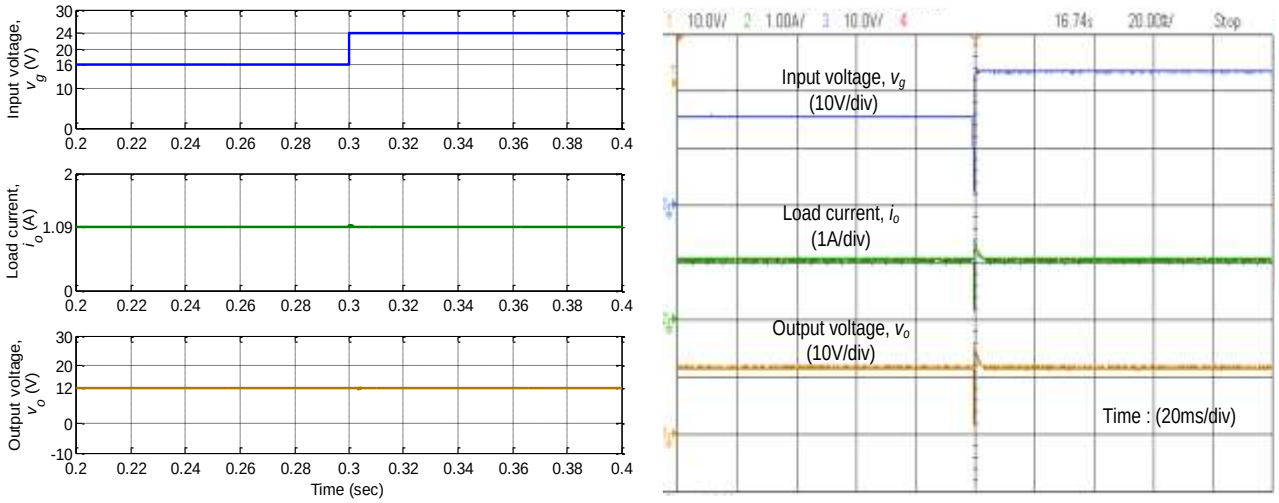
In this case, the variation in input voltage (V_g) is considered from minimum (16 V) to maximum (24 V) and vice-versa for two extreme load conditions R=11 Ω (*i.e.,* maximum load current, 1.09 A) and R=22 Ω (*i.e.*, minimum load current, 0.54 A). The desired output voltage is 12 V.

When at fixed load of 11 Ω, the input voltage is varied from 16 V to 24 V and vice-versa; the results are shown in Fig. 4.43 (a) and Fig. 4.43 (b), respectively. Similarly, when at fixed load of 22 Ω, the input voltage is varied from 16 V to 24 V and vice-versa; the results are shown in Fig. 4.44 (a) and Fig. 4.44 (b), respectively. These results illustrate that the output voltage settles quickly within 5 ms. The output voltage has small overshoot of 0.3 V with increase in the input voltage from 16 V to 24 V, whereas undershoot of 0.3 V with decrease in the input voltage from 24 V to 16 V. The experimental results vary slightly from simulation results in transient condition. The reason is that the step change in input voltage was realized using a manual switch. Therefore, during the initial part of the transition period, there is a dip in the input voltage before reaching to new input voltage. Therefore, in this particular case, the initial part of transients in the experimental output voltage is ignored while comparing with the simulation.

(c) Variation in load resistance or load current

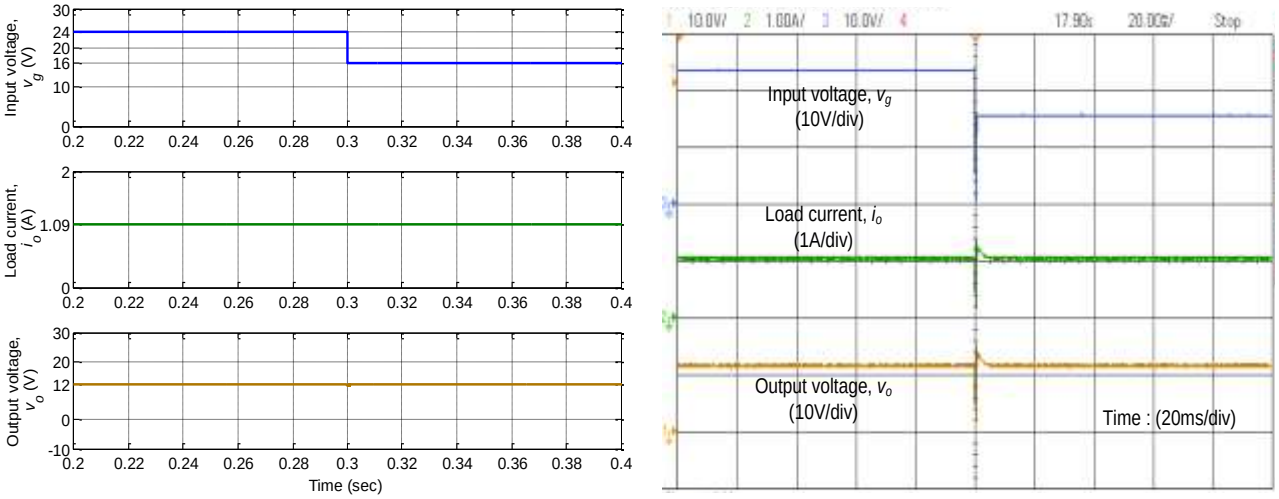
In this case, the load resistance (R) is varied from 22 Ω (*i.e.,* minimum load current, 0.54 A) to 11 Ω (*i.e.,* maximum load current, 1.09 A) and vice-versa for two extreme input voltages V_g=16 V (minimum) and V_g=24 V (maximum). The desired output voltage is 12 V.

At constant input voltage 16 V, the simulation and experimental results for step variation in load resistance from 22 Ω to 11 Ω and vice-versa are shown in Fig. 4.45 (a). Similarly, for same load variation but at constant input voltage 24 V, the results are displayed in Fig. 4.45 (b). These results exhibit that the output voltage reaches steady-state very quickly within 3-5 ms. The output voltage has small undershoot of 0.2 V when the load is switched from 22 Ω to 11 Ω, whereas overshoot of 0.2 V when the load is switched from 11 Ω to 22 Ω. The experimental results validate the MATLAB simulation results.



Simulation Experimental

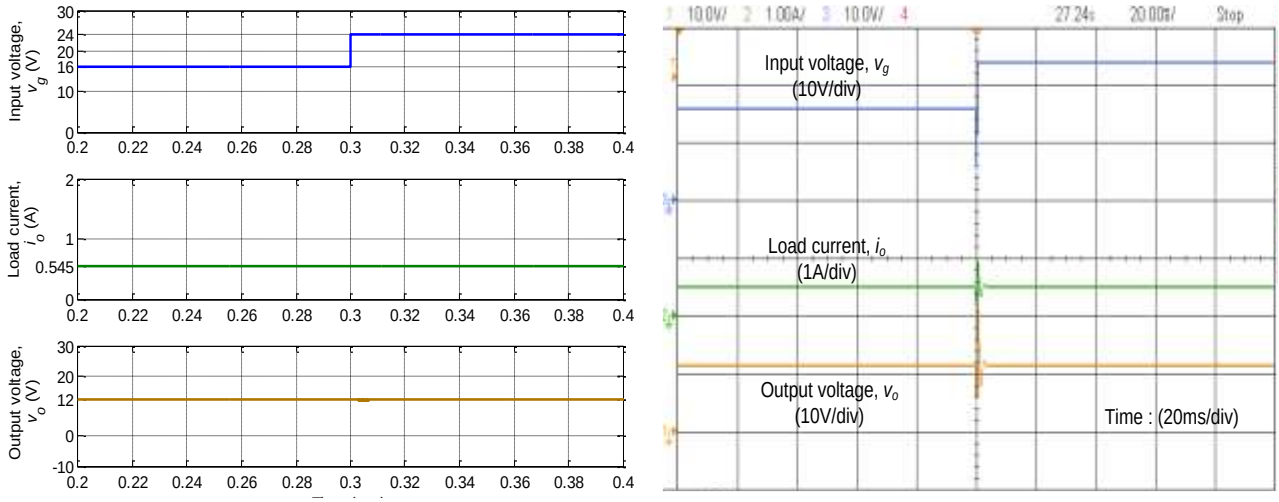
(a)



Simulation Experimental

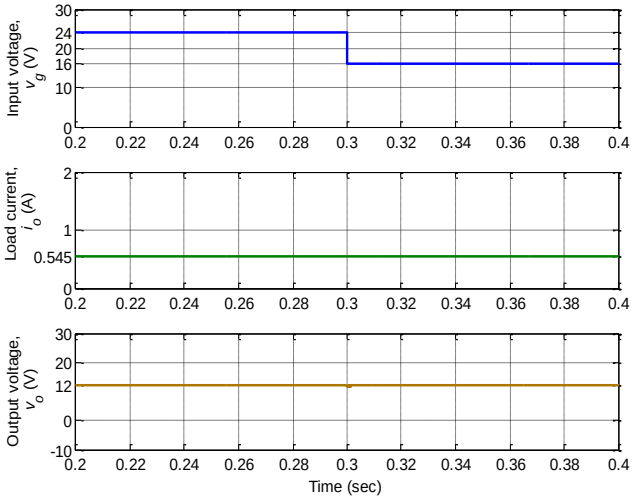
(b)

Fig. 4.43. Simulation and experimental results with R=11 Ω for input voltage variation from (a) 16 V to 24 V (b) 24 V to 16 V

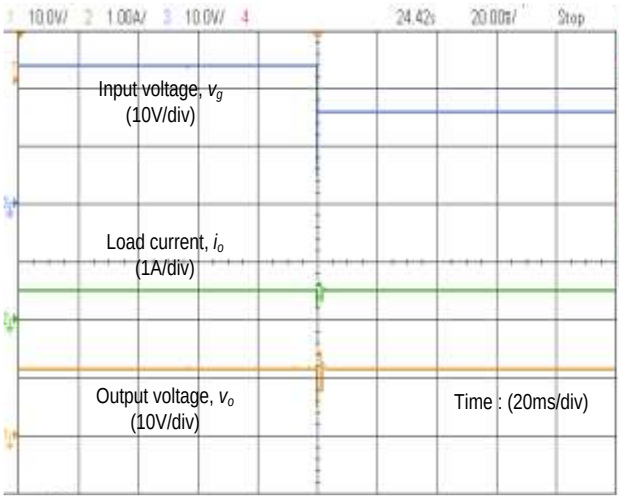


Simulation Experimental

(a)



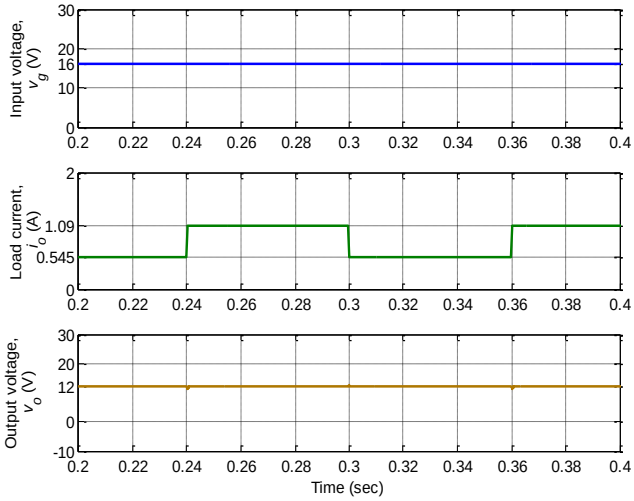
Simulation



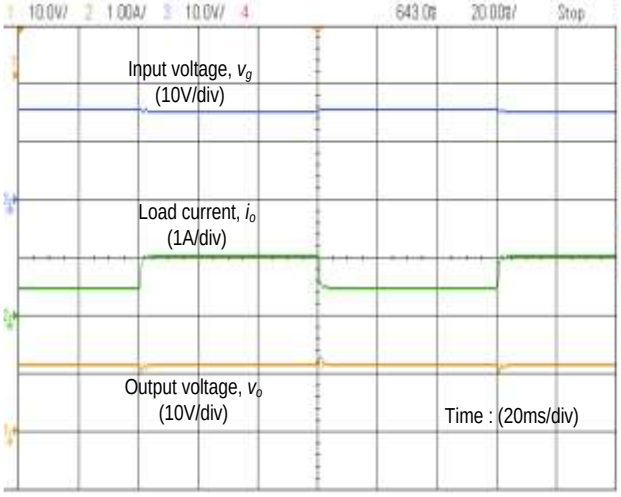
Experimental

(b)

Fig. 4.44. Simulation and experimental results with R=22 Ω for input voltage variation from (a) 16 V to 24 V (b) 24 V to 16 V

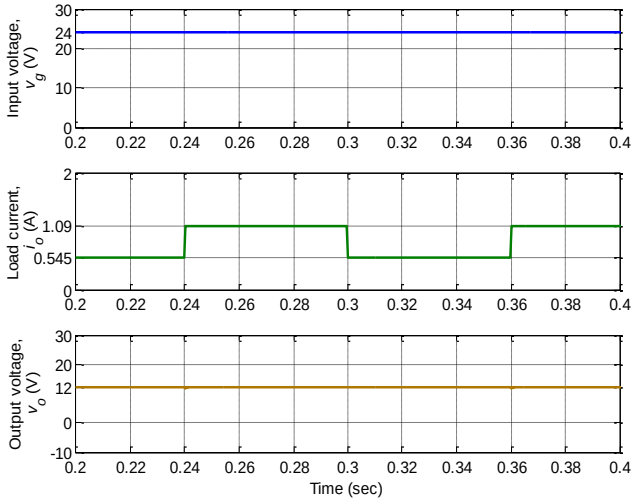


Simulation

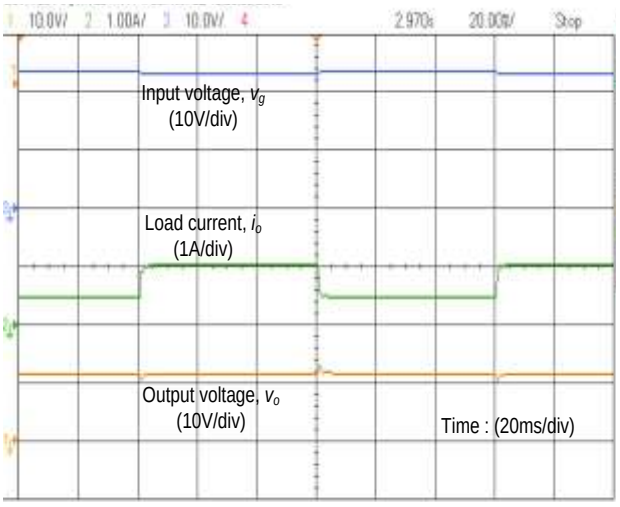


Experimental

(a)



Simulation



Experimental

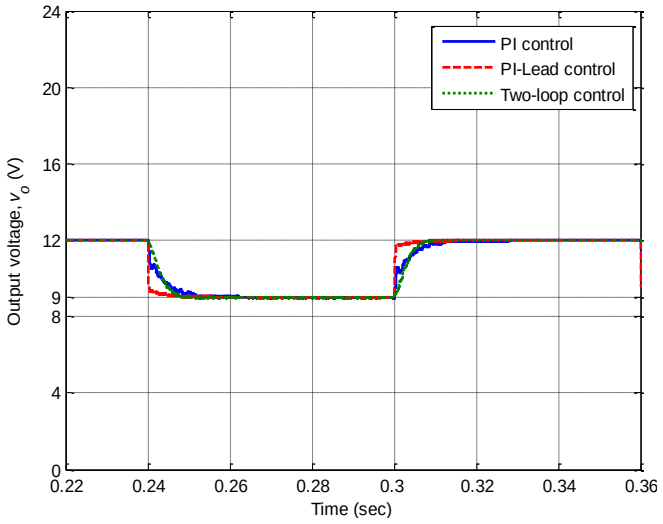
(b)

Fig. 4.45. Simulation and experimental results for variation in load resistance from 22 Ω to 11 Ω and vice-versa at input voltage (a) V_g=16 V (b) V_g=24 V

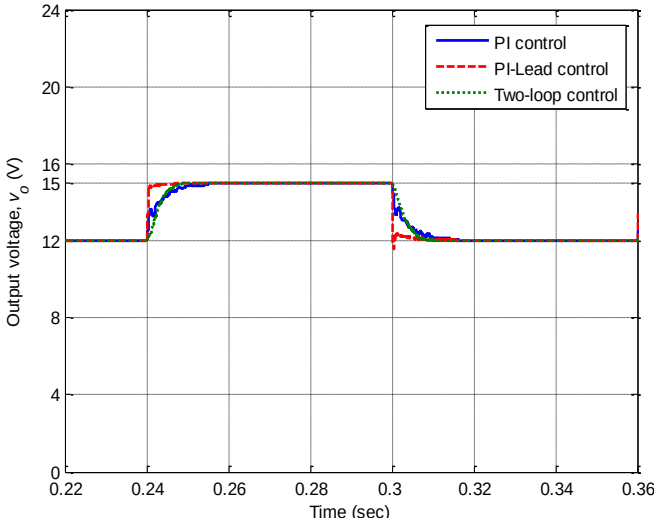
4.2.4 Performance comparison of different control techniques for buck converter

The aim of this section is to compare the performance of the three different control techniques used to regulate the output voltage of buck converter. These control techniques are PI control using stability boundary locus, PI-lead control and two-loop PI control. The individual performance has already been discussed using the simulation and experimental results. In this section, only the simulated output voltages with different control techniques are compared for various working conditions as shown in Fig. 4.46. The output voltage under reference voltage variation reaches to the new desired value within 15 to 20 ms, 10 ms and 5-7 ms for PI control, PI-lead control and two-loop PI control, respectively. For variation in input voltage, the output voltage settles to steady-state within 15 ms, 10 ms and 5 ms with PI controller, PI-lead controller and two-loop PI controller, respectively. However, the output voltage bears maximum overshoot of 6 V and maximum undershoot of 4.5 V with PI controller; whereas maximum overshoot and undershoot of 1 V with PI-lead controller and, maximum overshoot and undershoot of 0.3 V with two-loop PI controller. For load resistance variation, the output voltage settles to steady-state within 15-25 ms, 10 ms and 3-5 ms with PI controller, PI-lead controller and two-loop PI controller, respectively. The output voltage has maximum undershoot of 4 V and maximum overshoot of 6 V with PI controller; whereas maximum undershoot and overshoot of 2 V with PI-lead controller and maximum undershoot and overshoot of 0.2 V with two-loop PI controller.

From this comparison, it is concluded that the PI controller regulates the output voltage under all three cases, but takes larger time to settle to the steady-state value in comparison with PI-lead and two-loop controller. Further, PI controller has more overshoot/undershoot with oscillations. The PI-lead controller has less settling time in comparison to PI controller, but more in comparison to two-loop PI control. The PI-lead controller was designed with 4 kHz frequency in order to improve the settling time, but it introduces more noise in output voltage as shown by experimental result in section 4.2.2.3. In conclusion, the two-loop PI control gives better dynamic and steady-state performance over PI and PI-lead controller.

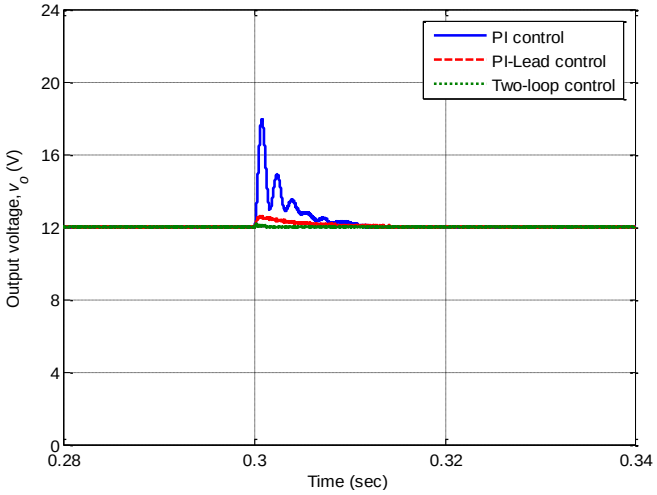


V_{ref}=12 V to 9 V and vice-versa

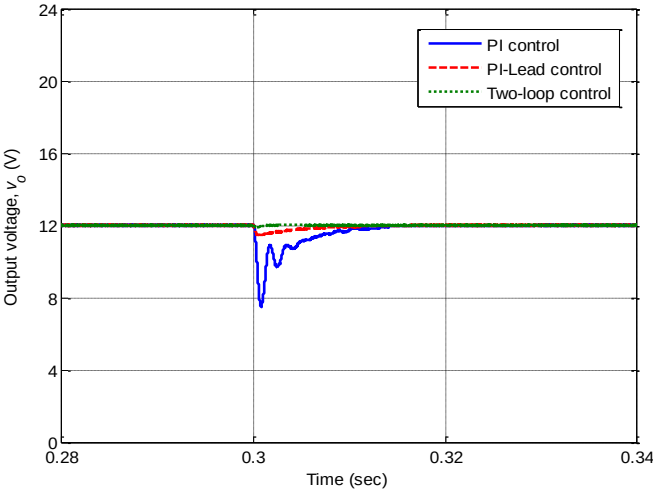


V_{ref}=12 V to 15 V and vice-versa

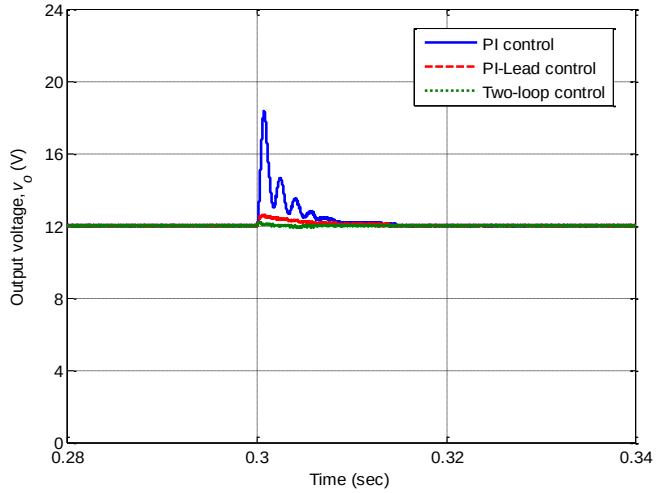
(a)



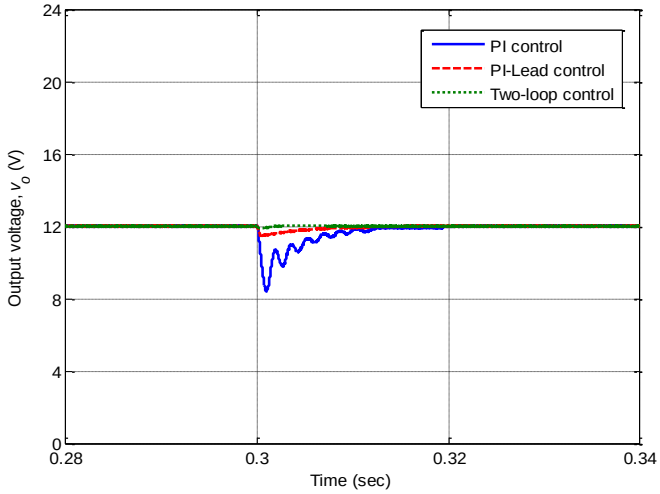
V_g=16 V to 24 V with R=11 Ω



V_g=24 V to 16 V with R=11 Ω

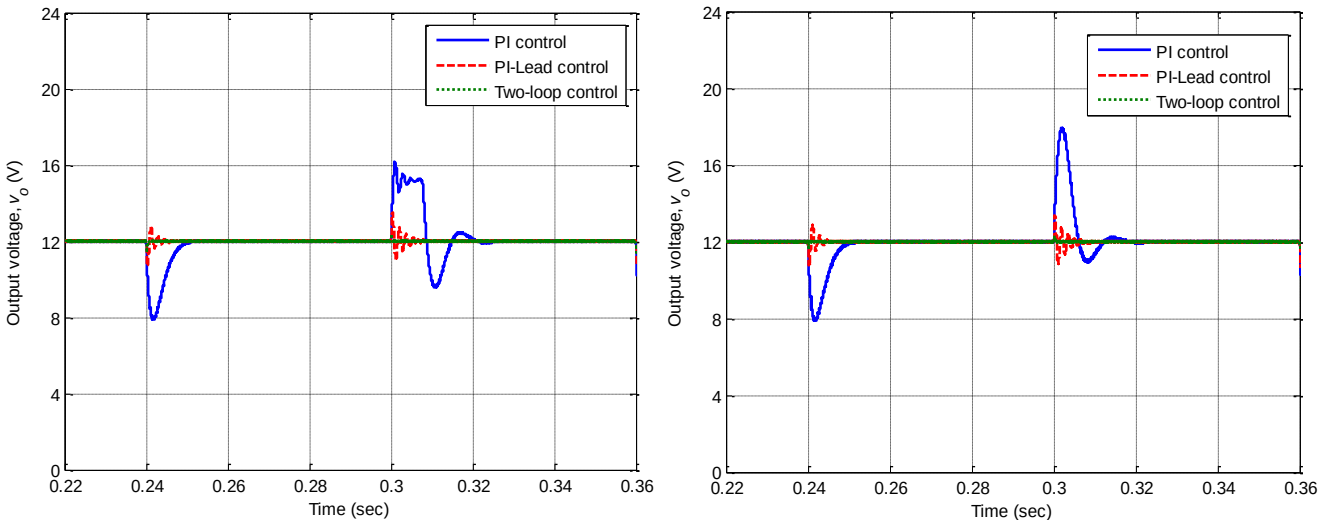


V_g=16 V to 24 V with R=22 Ω



V_g=24 V to 16 V with R=22 Ω

(b)



R=22 Ω to 11 Ω and vice-versa with V_g=16 V

R=22 Ω to 11 Ω and vice-versa with V_g=24 V

(c)

Fig. 4.46. Comparison of different control techniques for DC-DC buck converter Output voltage for variation in (a) reference output voltage (b) input voltage (c) load current

4.3 Control of DC-DC Cuk Converter

In this section, the different control techniques used for the buck converter have also been implemented to regulate the DC output voltage of the Cuk converter. The simulation and experimental results are presented under different working conditions. The Cuk converter is a fourth-order system. Therefore, PI controller using its reduced second-order model has also been designed. This section is divided into following subsections.

4.3.1 PI controller design

4.3.2 PI controller design using reduced second-order model

4.3.3 PI-lead controller design

4.3.4 Two-loop PI controller design

4.3.5 Performance comparison of different control techniques for Cuk converter

4.3.1 PI controller design

In this section, the PI control design for DC-DC Cuk converter is discussed. The simulation and experimental results are obtained to show the performance of the PI controller.

4.3.1.1 Description of the control scheme

The block diagram of closed-loop PI control of a DC-DC Cuk converter is shown in Fig. 4.47. The detailed schematic of this control scheme for Cuk converter is given in Fig. 4.48. Similar to buck converter PI control design, the actual output voltage (v_o) is compared with the reference output voltage ($v_{o,ref}$). The resultant voltage error (v_{err}) is fed via PI controller $G_c(s)$ to generate control voltage v_c, which is compared with a sawtooth signal of fixed peak

and frequency. The output of the comparator provides the switching pulses of desired duty cycle *d* to regulate the dc output voltage of the Cuk converter.

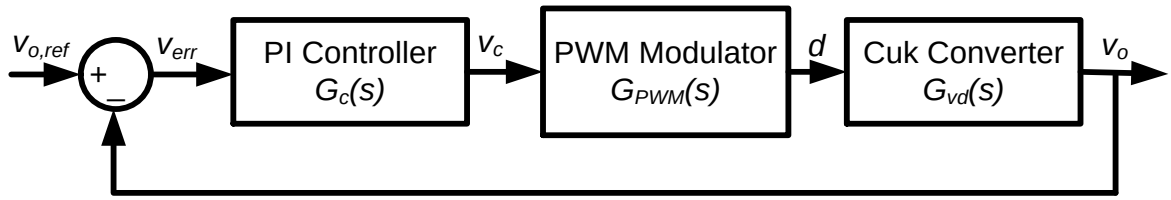


Fig. 4.47. Block diagram of closed-loop PI control of DC-DC Cuk converter

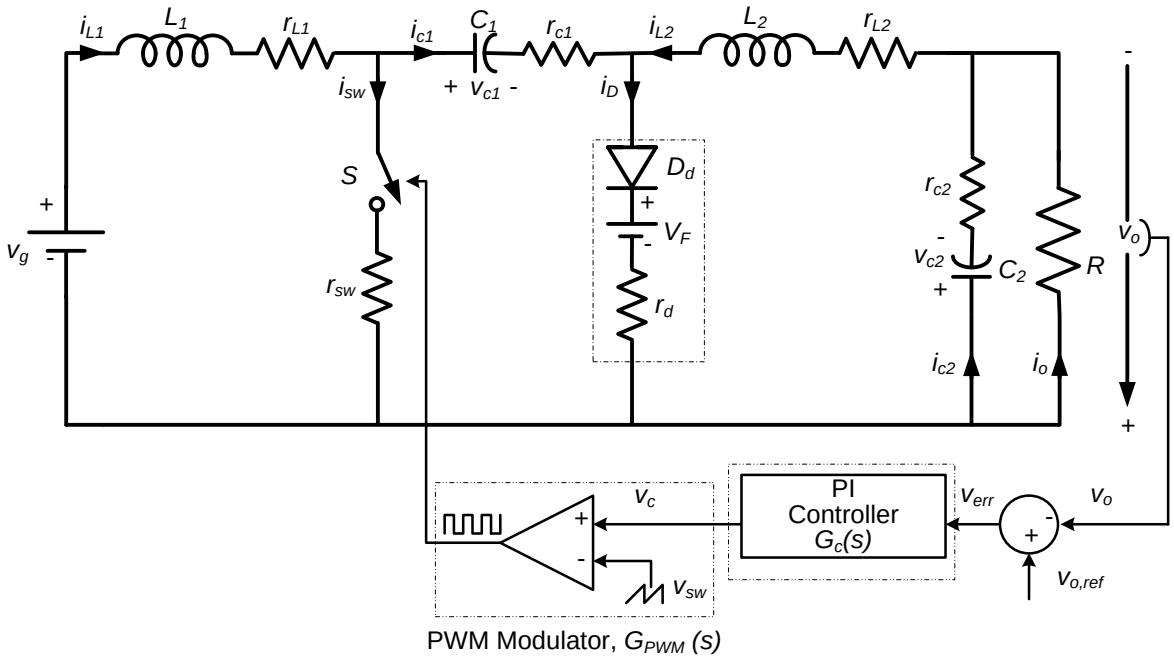


Fig. 4.48. Detailed schematic of PI controlled DC-DC Cuk converter

Table 4.9. DC-DC Cuk converter specifications

Parameters	**Value**
Input voltage, V_g	20-28 V
Output voltage, V_o	16 V
Load resistance, R	11-22 Ω
Inductance, L_1/r_{L1}	3 mH/0.35 Ω
Inductance, L_2/r_{L2}	1.9 mH/0.25 Ω
Capacitance, C_1/r_{c1}	420 μF/0.11 Ω
Capacitance, C_2/r_{c2}	420 μF/0.11 Ω
Diode forward voltage, V_F	0.7 V
Resistance switch/diode (r_{sw}/r_d),	0.044 Ω/0.024 Ω
Switching frequency, f	20 kHz
Sawtooth Peak Voltage, V_{sw}	1

The parameters of Cuk converter under consideration are given in Table 4.9. These parameters are same as used for Cuk converter modeling in chapter 3. The input voltage and load resistance is considered variable in a range given in Table 4.9. In this chapter, the mathematical model of Cuk converter used for controller design is derived by assuming that the converter is operating with minimum input voltage (V_g=20 V) and maximum load current (or minimum load resistance R=11 Ω).

The duty-cycle to output-voltage transfer function of the Cuk converter has already been derived in (3.281) of the previous chapter. Therefore, substituting these Cuk converter parameters, we get

$$G_{vd}(s)=\frac{\tilde{v}_o(s)}{\tilde{d}(s)}=\frac{2000s^3+4.342\times10^7s^2+3.692\times10^9s+1.865\times10^{13}}{s^4+594.2s^3+1.836\times10^6s^2+3.949\times10^8s+3.224\times10^{11}} \tag{4.87}$$

The uncompensated loop transfer function of Cuk converter will be

$$T(s)=G_{PWM}(s)G_{vd}(s)=\frac{2000s^3+4.342\times10^7s^2+3.692\times10^9s+1.865\times10^{13}}{s^4+594.2s^3+1.836\times10^6s^2+3.949\times10^8s+3.224\times10^{11}} \tag{4.88}$$

Where, $G_{PWM}(s)=1/V_{sw}$ is the transfer function of PWM modulator and V_{sw}=1 for this modulator design.

The bode plot of uncompensated DC-DC Cuk converter is shown in Fig. 4.49, which suggests that the phase margin of the uncompensated system is 22.1° at a gain crossover frequency of 1.09 kHz. This phase margin is low and gives poor transient response with larger overshoots. Moreover, the gain of the uncompensated Cuk converter is constant in the low-frequency region that results in steady-state error for a step disturbance.

To improve the steady-state error and the phase margin of this Cuk converter, a PI controller is designed. The parameters of this PI controller are tuned using the stability boundary locus approach discussed in section 4.2.1.1.

By comparing (4.88) with (4.5), we get

$$\begin{aligned} &b_3=2000, b_2=4.342\times10^7, b_1=3.692\times10^9, b_0=1.865\times10^{13},\\ &a_4=1, a_3=594.2, a_2=1.836\times10^6, a_1=3.949\times10^8, a_0=3.224\times10^{11}\end{aligned} \tag{4.89}$$

Substituting these coefficients in (4.16) and (4.17), we get

$$K_p(\omega,\varphi)=\frac{\left(\begin{array}{l}-2000\sin\varphi\omega^7-4.22\times10^7\cos\varphi\omega^6-1.84\times10^{10}\sin\varphi\omega^5+9.53\times10^{13}\cos\varphi\omega^4+\\ 2.08\times10^{16}\sin\varphi\omega^3-4.68\times10^{19}\cos\varphi\omega^2-6.17\times10^{21}\sin\varphi\omega+6.01\times10^{24}\cos\varphi\end{array}\right)}{-\left(4\times10^6\omega^6+1.87\times10^{15}\omega^4-1.60\times10^{21}\omega^2+3.47\times10^{26}\right)} \tag{4.90}$$

$$K_i(\omega,\varphi)=\frac{\omega\left(\begin{array}{l}-2000\cos\varphi\omega^7+4.22\times10^7\sin\varphi\omega^6-1.84\times10^{10}\cos\varphi\omega^5-9.53\times10^{13}\sin\varphi\omega^4+\\ 2.08\times10^{16}\cos\varphi\omega^3+4.68\times10^{19}\sin\varphi\omega^2-6.17\times10^{21}\cos\varphi\omega-6.01\times10^{24}\sin\varphi\end{array}\right)}{-\left(4\times10^6\omega^6+1.87\times10^{15}\omega^4-1.60\times10^{21}\omega^2+3.47\times10^{26}\right)} \tag{4.91}$$

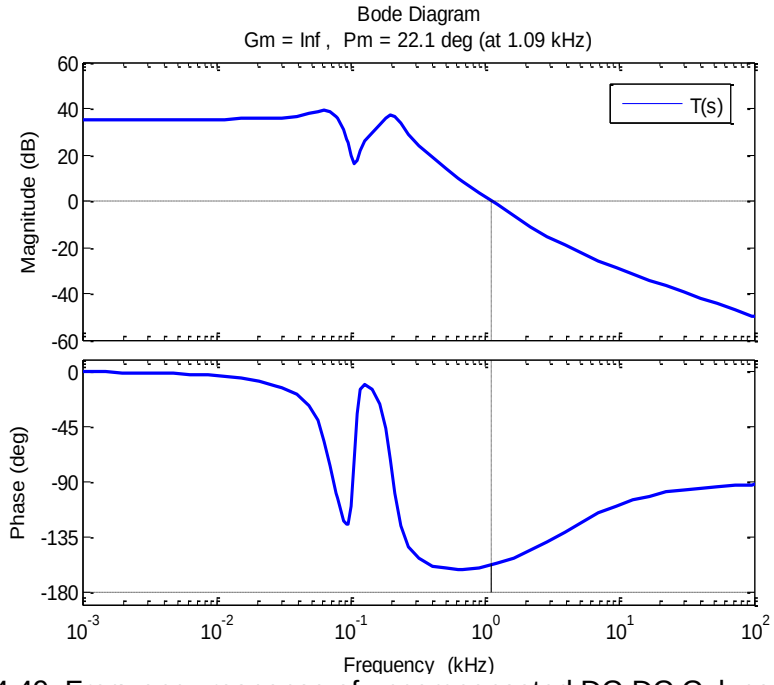


Fig. 4.49. Frequency response of uncompensated DC-DC Cuk converter

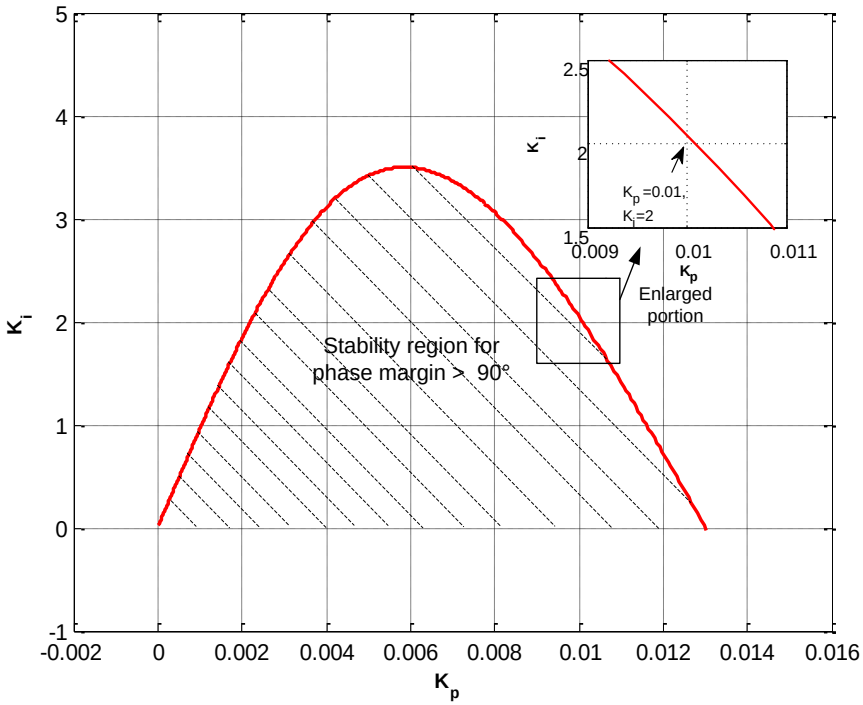


Fig. 4.50. Stability boundary locus for DC-DC Cuk converter

The PI controller is designed to achieve the phase margin of atleast 90°. Therefore, substituting φ=90° in (4.90)-(4.91) and then by varying ω, the stability boundary locus for Cuk converter in K_p-K_i plane is obtained as shown in Fig. 4.50. The any pair of K_p and K_i within this stability region assures phase margin of 90° or more. The K_p=0.01 and K_i=2 are selected within this stable region. With these values of K_p and K_i, the PI controller transfer function is

$$G_c(s) = \frac{0.01s + 2}{s} \tag{4.92}$$

The bode plot of the PI compensated Cuk converter is shown in Fig. 4.51. As seen from the figure, the phase margin of the closed-loop Cuk converter is increased to 93.6° but gain crossover frequency is decreased to 63.9 Hz. The increased phase margin helps in reducing the overshoot, but decreased crossover frequency makes the speed of response sluggish. The low-frequency gain is now having -20 dB/decade slope which helps to eliminate the steady-state error.

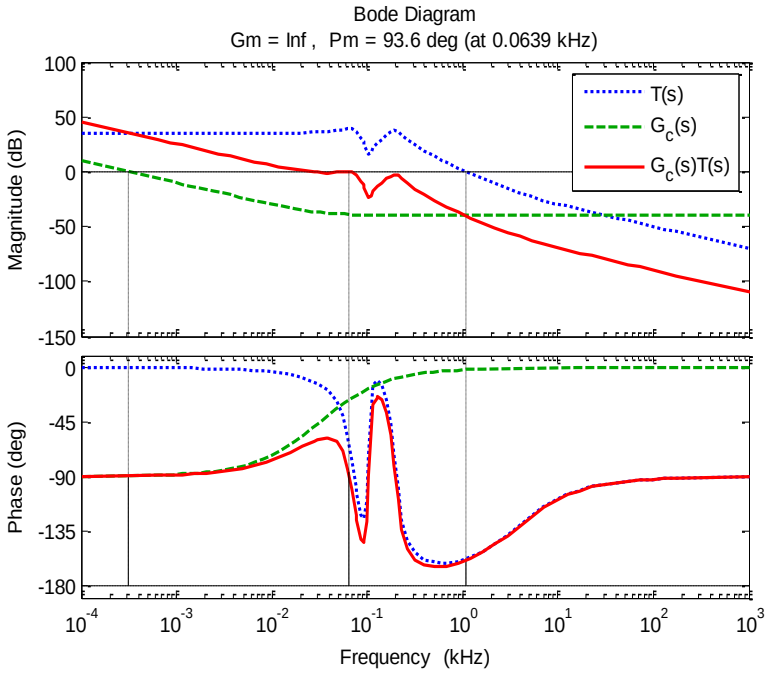


Fig. 4.51. Frequency response of PI compensated DC-DC Cuk converter

4.3.1.2 Results and discussion

In this section, the performance of this PI control design of the Cuk converter is tested under different conditions. The Cuk converter parameters for simulation and experimental results remain same as given in Table 4.9. The transfer function of PI controller is given in (4.92). The simulation results are obtained using MATLAB/Simulink software, whereas the experimental results are obtained by implementing the PI controller on the Cuk converter prototype using dSPACE controller. The experimental part has been discussed elaborately in Appendix *B*.

The simulation and experimental results are analysed for three different working conditions:

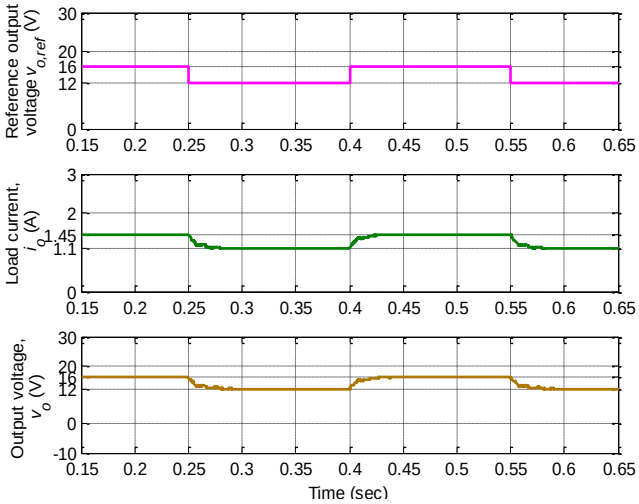
(a) Variation in reference output voltage

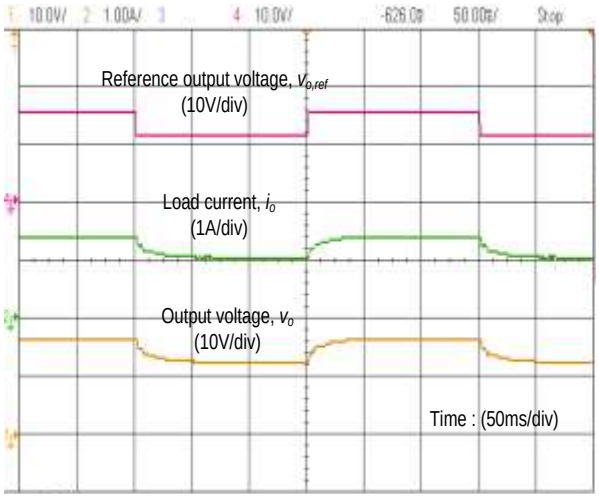
(b) Variation in input voltage

(c) Variation in load current

(a) Variation in reference output voltage

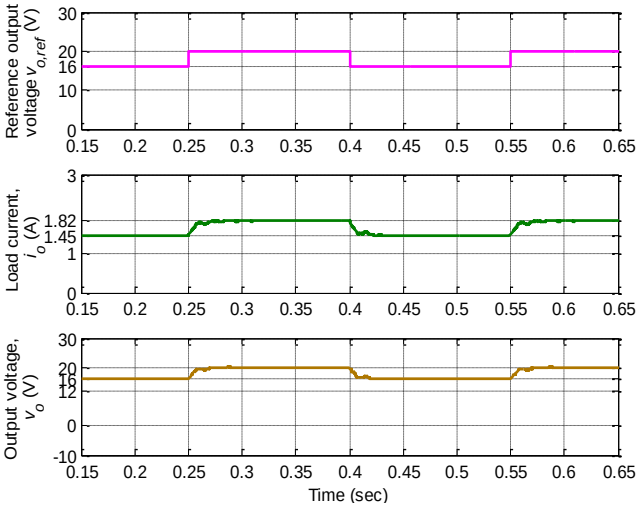
In this case, the performance of PI controller is observed for step change in reference output voltage ($V_{o,ref}$). The input voltage (V_g) and load resistance (R) are kept constant to 20 V and 11 Ω, respectively. For the reference voltage variation from 16 V to 12 V and vice-versa, the simulation and experimental results are shown in Fig. 4.52 (a). Similarly, for reference voltage variation from 16 V to 20 V and vice-versa, the corresponding simulation and experimental results are shown in Fig. 4.52 (b). It is observed that the output voltage reaches to the new desired value within 50-60 ms without any overshoot/undershoot and oscillations. The load current also varies according to new desired output voltage because load resistance is kept constant (11 Ω). The load current is 1.09 A, 1.45 A and 1.81 A for desired output voltage 12 V, 16 V and 20 V, respectively. It is demonstrated that the simulation and experimental results are closely matched.

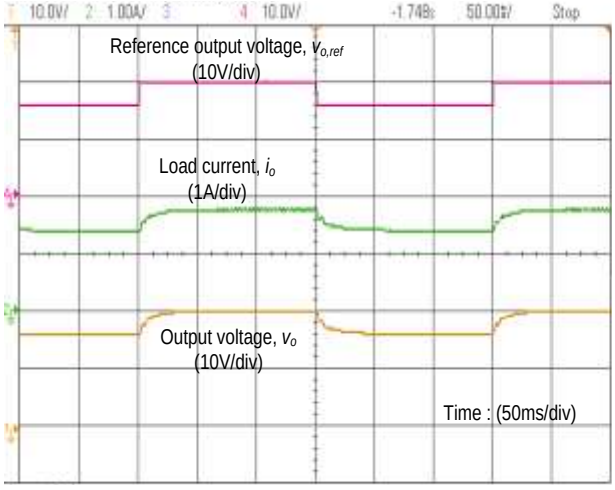




Simulation Experimental

(a)





Simulation Experimental

(b)

Fig. 4.52. Simulation and experimental results for reference output voltage variation from (a) 16 V to 12 V and vice-versa (b) 16 V to 20 V and vice-versa

(b) Variation in input voltage

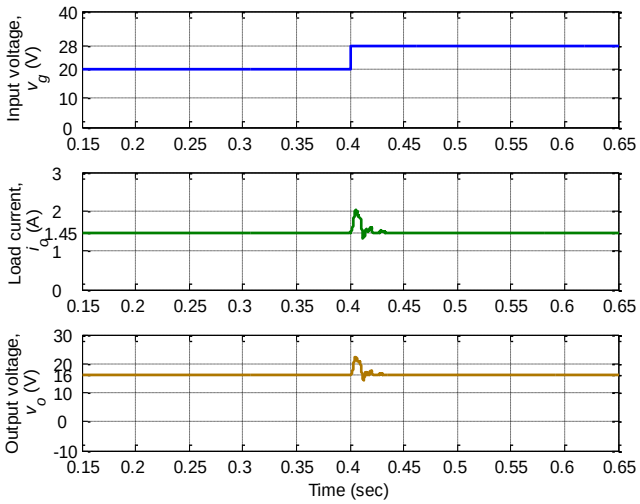
The simulation and experimental results are obtained for step variation in input voltage while keeping the load conditions constant. The variation in input voltage (V_g) is considered from minimum (20 V) to maximum (28 V) and vice-versa for two extreme load conditions R=11 Ω (*i.e.,* maximum load current, 1.45 A) and R=22 Ω (*i.e.,* minimum load current, 0.73 A). The desired output voltage is 16 V.

In the first case, the load is fixed at 11 Ω and the input voltage varies from 20 V to 28 V (Fig. 4.53 (a)) and 28 V to 20 V (Fig. 4.53 (b)). In the second case, the load is fixed at 22 Ω and the input voltage varies from 20 V to 28 V (Fig. 4.54 (a)) and 28 V to 20 V (Fig. 4.54 (b)). From these results, it is demonstrated that when the input voltage is increased from 20 V to 28 V, the output voltage reaches back to steady-state (16 V) within 45-50 ms. However, during transients, the output voltage faces overshoot of 6-7 V and undershoot of 1.8-2.2 V. Similarly, when the input voltage is decreased from 28 V to 20 V, the output voltage settles in 55-70 ms. It has undershoot of 4-6 V and overshoot of 1.6-4 V. The experimental results also validate the simulation results. The experimental results slightly vary from simulation results during transients because the step change in input voltage was realized using a manual switch.

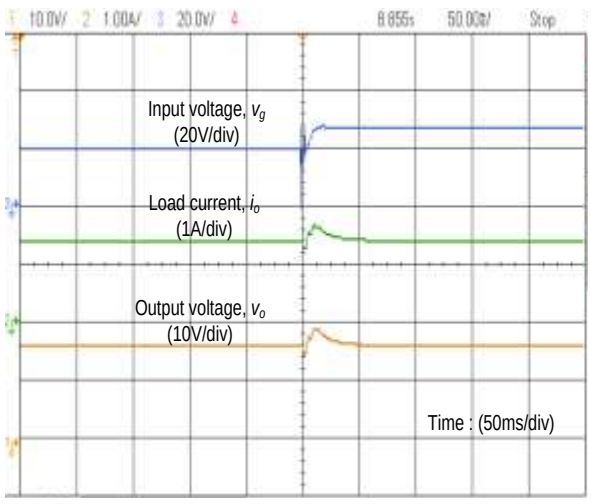
(c) Variation in load resistance or load current

In this case, the performance of the PI controlled Cuk converter is tested for variations in load conditions while keeping the input voltage constant. The load resistance (R) is varied from 22 Ω (*i.e.,* minimum load current, 0.73 A) to 11 Ω (*i.e.,* maximum load current, 1.45 A) and vice-versa for two extreme input voltages V_g=20 V (minimum) and V_g=28 V (maximum). The desired output voltage is 16 V.

Fig. 4.55 (a) shows the simulation and experimental results for step variation in load resistance from 22 Ω to 11 Ω and vice-versa at fixed input voltage 20 V. Similarly, in Fig. 4.55 (b), the simulation and experimental results are shown for the same load variation, but at fixed input voltage 28 V. These results display that the output voltage settles within 40-50 ms. For load variation from 22 Ω to 11 Ω, the output voltage has slight oscillations with the undershoot of 1.2 V and overshoot of 0.4 V. On the other hand, when the load is shifted from 11 Ω to 22 Ω, the output voltage has overshoot of 1.6 V and undershoot of 0.4 V. The experimental results are in close agreement with the simulation results validating the performance of PI controller for Cuk converter prototype.

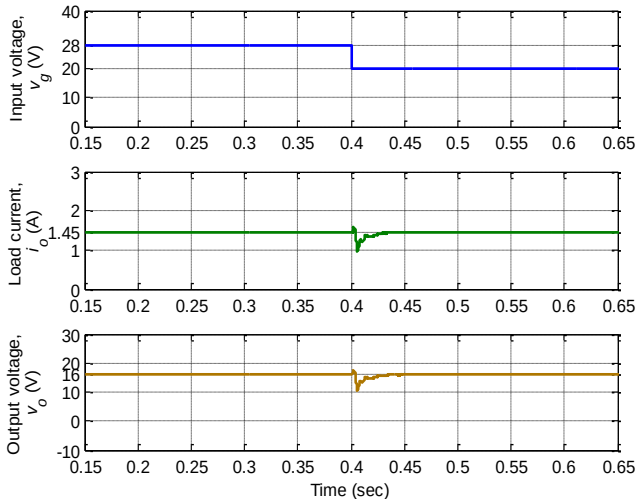


Simulation

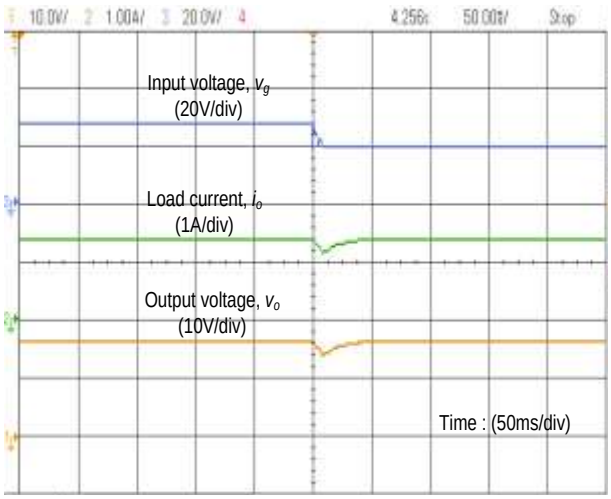


Experimental

(a)



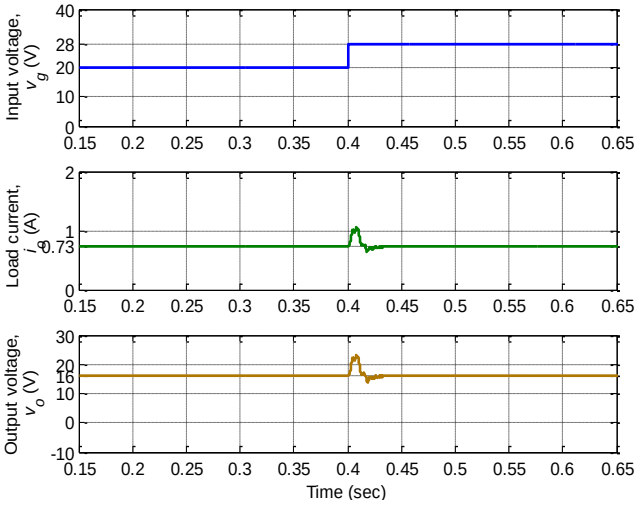
Simulation



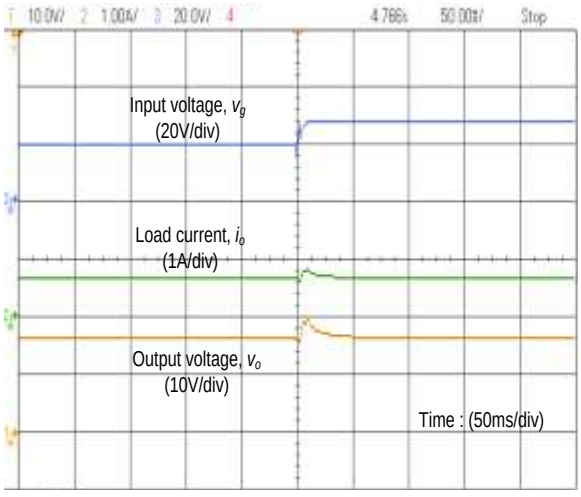
Experimental

(b)

Fig. 4.53. Simulation and experimental results with R=11 Ω for input voltage variation from (a) 20 V to 28 V (b) 28 V to 20 V

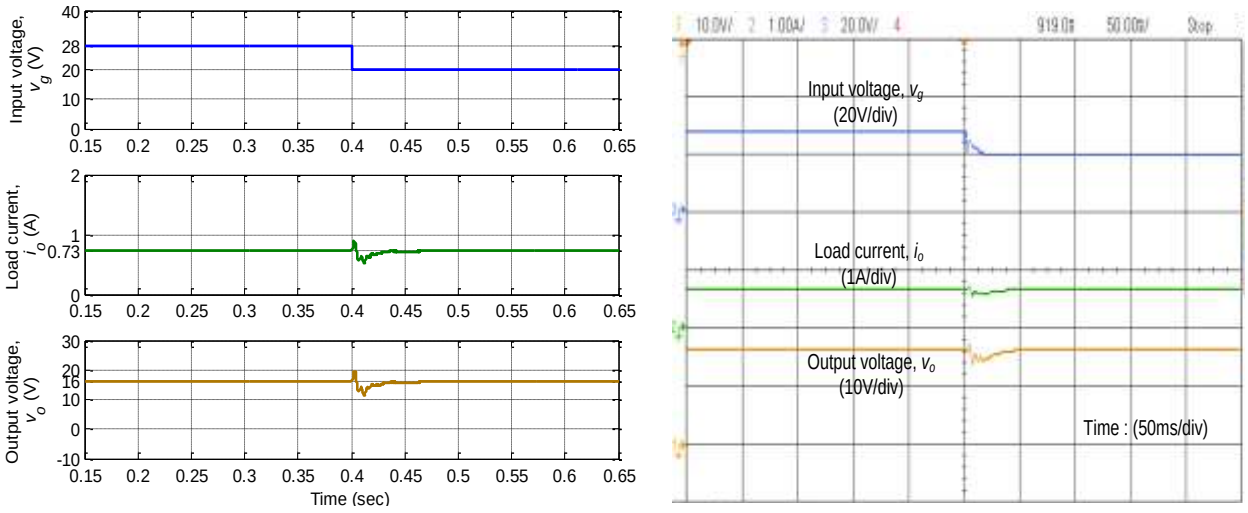


Simulation



Experimental

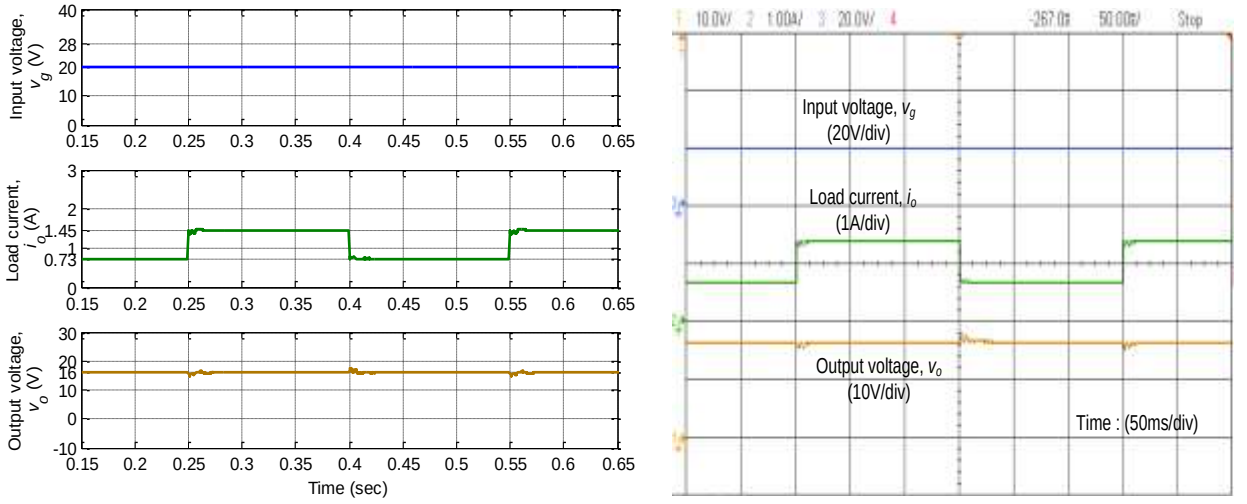
(a)



Simulation Experimental

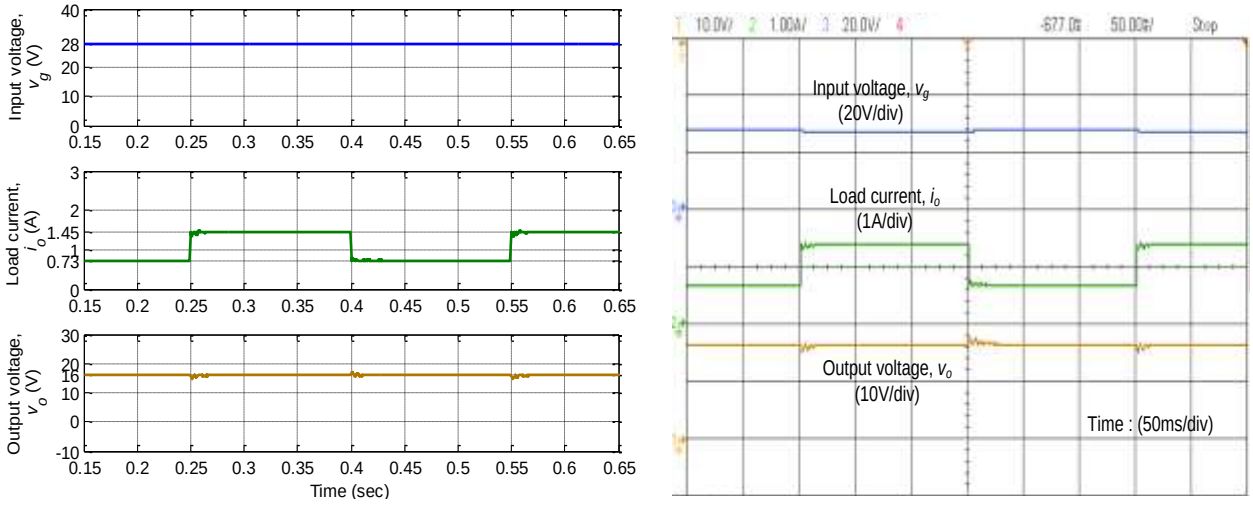
(b)

Fig. 4.54. Simulation and experimental results with R=22 Ω for input voltage variation from (a) 20 V to 28 V (b) 28 V to 20 V



Simulation Experimental

(a)



Simulation Experimental

(b)

Fig. 4.55. Simulation and experimental results for variation in load resistance from 22 Ω to 11 Ω and vice-versa at input voltage (a) V_g=20 V (b) V_g=28 V

4.3.2 PI controller design using reduced second-order model

The DC-DC Cuk converter is a fourth-order system. In the previous section, a PI controller was designed for DC-DC Cuk converter using its fourth-order transfer function. As discussed in the introduction of this chapter, there are several model-order reduction techniques in the literature. However, in this section, only the truncation method is used to get the second-order reduced model of the Cuk converter. The aim of the author is to design a PI controller based on the obtained reduced-order model and then implementing this PI controller on the hardware prototype to validate the performance.

Therefore, in this section, first, the truncation method for model-order reduction of higher-order system is discussed in brief. Then, this method is applied to get second-order reduced model of Cuk converter. Finally, the PI controller for the Cuk converter is designed using the reduced second-order model. The simulation and experimental results are obtained to show the performance of the designed PI controller based on reduced-order model.

4.3.2.1 Truncation method for model-order reduction

The truncation method is the simplest method for obtaining reduced-order model of higher-order systems [171]. This method does not require any mathematical commutation to obtain the reduced-order model. In this method, the higher-order terms in the numerator and denominator of the original system are truncated to obtain the low-order model.

Consider the transfer function of a n^{th}-order higher-order system $G(s)$ as

$$G(s) = \frac{\sum_{i=0}^{n-1} b_i s^i}{\sum_{i=0}^{n} a_i s^i} \tag{4.93}$$

Where, b_i and a_i are coefficients of the numerator and denominator polynomials, respectively.

Then, the r^{th}-order ($r<n$) reduced model of $G(s)$ are obtained by truncating the higher-order terms in (4.93). The r^{th}-order reduced model is given as

$$R(s) = \frac{\sum_{i=0}^{r-1} b_i s^i}{\sum_{i=0}^{r} a_i s^i} \tag{4.94}$$

This method is used to obtain the second-order reduced model of original fourth-order transfer function of DC-DC Cuk converter. The fourth-order duty-cycle to output-voltage transfer function of Cuk converter has been obtained in (4.87) and is rewritten as

$$G_{vd}(s) = \frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{2000s^3 + 4.342\times10^7 s^2 + 3.692\times10^9 s + 1.865\times10^{13}}{s^4 + 594.2s^3 + 1.836\times10^6 s^2 + 3.949\times10^8 s + 3.224\times10^{11}} \tag{4.95}$$

The second-order reduced model of this Cuk converter using truncation method is

$$R(s) = \frac{3.692\times10^9 s + 1.865\times10^{13}}{1.836\times10^6 s^2 + 3.949\times10^8 s + 3.224\times10^{11}} = \frac{2010s + 1.016\times10^7}{s^2 + 215s + 1.755\times10^5} \tag{4.96}$$

4.3.2.2 Description of control scheme

The block diagram of the closed-loop scheme for the PI controller design of Cuk converter using its reduced second-order model is shown in Fig. 4.56. The detailed explanation of this block diagram remains same as given in section 4.3.1.1. The only difference is that in the present case, the reduced second-order transfer function model of Cuk converter is used for PI controller design instead of original fourth-order transfer function model used in section 4.3.1.1.

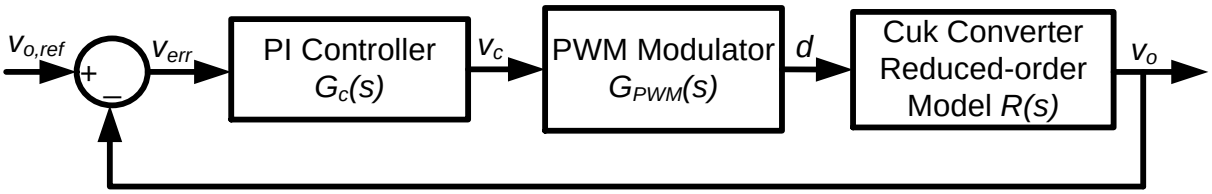


Fig. 4.56. Block diagram of closed-loop PI control of DC-DC Cuk converter using reduced second-order model

From this block diagram, the loop transfer function of uncompensated system will be

$$T_R(s) = G_{PWM}(s)R(s) = \frac{2010s + 1.016\times10^7}{s^2 + 215s + 1.755\times10^5} \tag{4.97}$$

Where, $G_{PWM}(s)=1/V_{sw}$ is transfer function of PWM modulator and V_{sw}=1 for this modulator design.

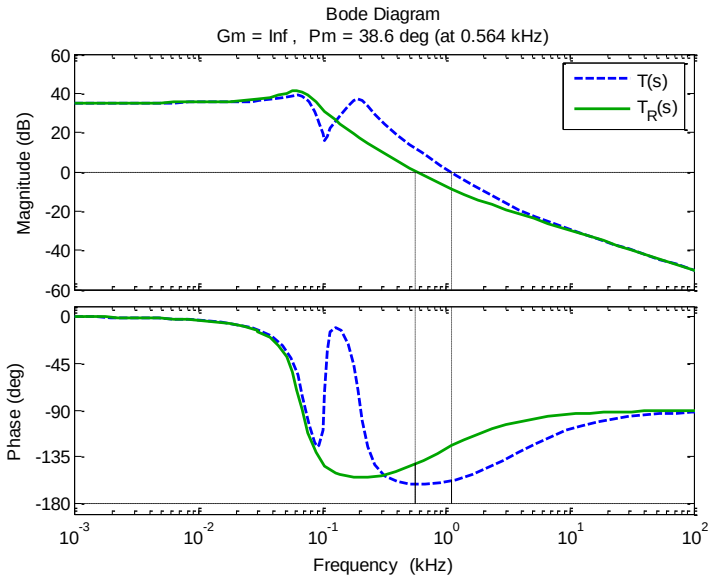


Fig. 4.57. Frequency responses of uncompensated DC-DC Cuk converter with original and reduced second-order model

Table 4.10. Comparison of frequency domain parameters for uncompensated DC-DC Cuk converter with original and reduced second-order model

Uncompensated system	Gain Margin	Phase Margin	Gain crossover frequency
With original model	inf	22.1°	1.09 kHz
With reduced second-order model	inf	38.6°	0.564 kHz

The bode plot of uncompensated DC-DC Cuk converter with original model (*T(s)*) and with reduced second-order model ($T_R(s)$) is compared in Fig. 4.57. The frequency domain parameters in both cases are given in Table 4.10. As seen from the responses, the reduced second-order model approximates the characteristics of the original fourth-order system. Therefore, this second-order model can be used for controller design. In order to improve the phase margin and low-region frequency gain, a PI controller is designed using the stability boundary locus approach discussed in section 4.2.1.1. For this purpose, the reduced second-order model is used instead of original fourth-order transfer function.

By comparing (4.97) with (4.5), we get

$$b_3=0, b_2=0, b_1=2010, b_0=1.016\times10^7, a_4=0, a_3=0, a_2=1, a_1=215, a_0=1.755\times10^5 \quad (4.98)$$

The PI controller is designed to achieve the phase margin of atleast 90°. Therefore, first, we substitute φ=90° and the coefficients from (4.98) into (4.16)-(4.17). Then by varying ω, the stability boundary locus in K_p-K_i plane is obtained as shown in Fig. 4.58. Any pair of K_p and K_i within this stability region assures phase margin of 90° or more. The PI controller parameters K_p=0.006 and K_i=2 are selected. With these values of K_p and K_i, the PI controller transfer function is

$$G_c(s)=\frac{0.006s+2}{s} \quad (4.99)$$

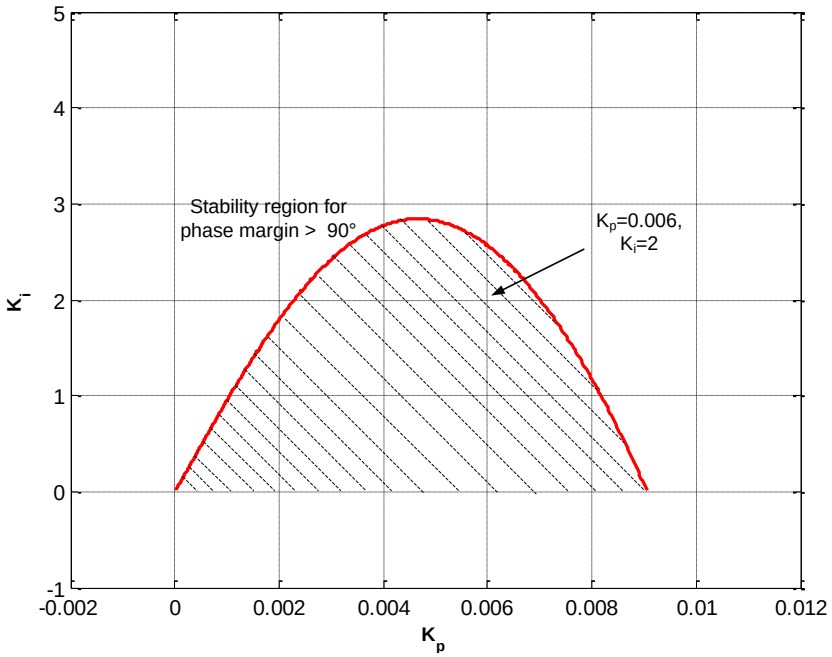


Fig. 4.58. Stability boundary locus for reduced second-order model of Cuk converter

The bode plots of the PI compensated Cuk converter with reduced second-order model are shown in Fig. 4.59. The phase margin of the closed-loop compensated system is increased to 103° at gain crossover frequency of 22 Hz. The increased phase margin reduces the overshoot. However, the decreased crossover frequency makes the system slower. The low-frequency gain is now having -20 dB/decade slope which helps to eliminate

the steady-state error. The comparison of bode plots of PI compensated Cuk converter with original fourth-order and reduced second-order transfer function is shown in Fig. 4.60. The corresponding frequency domain parameters are compared in Table 4.11. From these responses, it is clear that the PI controller $G_c(s)$ designed from the reduced second-order model of Cuk converter gives almost similar performance with the original fourth-order transfer function also.

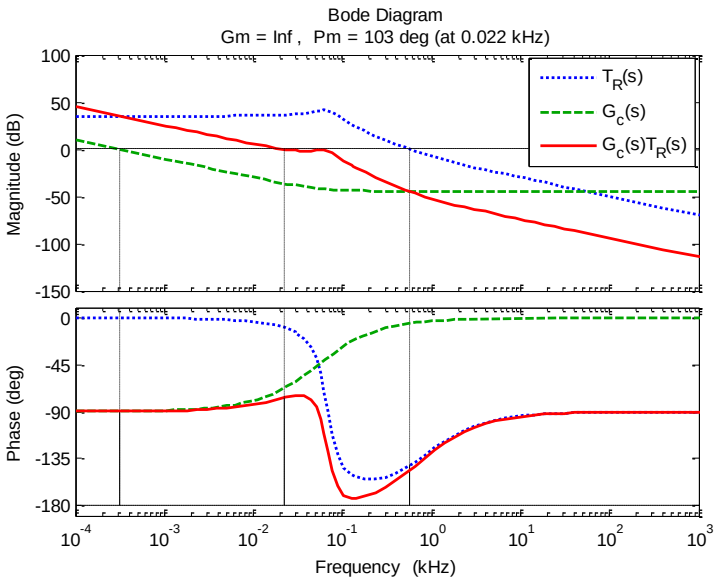


Fig. 4.59. Frequency response of PI controlled Cuk converter with reduced-order model

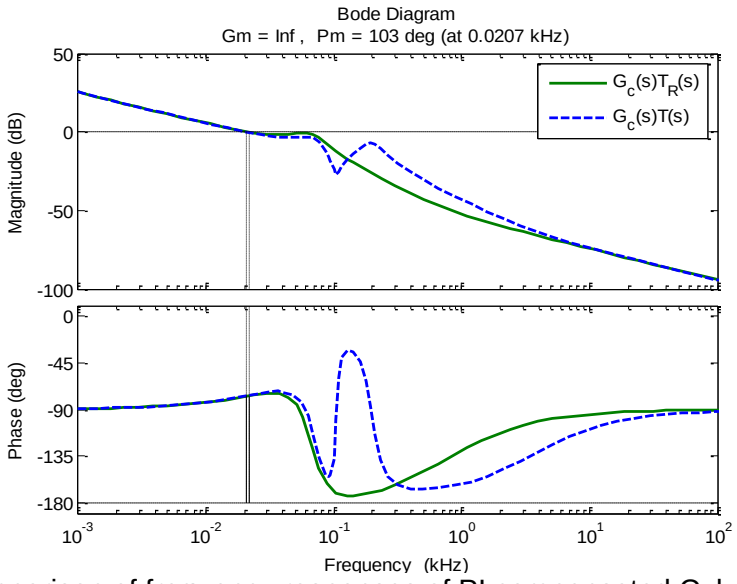


Fig. 4.60. Comparison of frequency responses of PI compensated Cuk converter with reduced second-order model and original fourth-order model

Table 4.11. Comparison of frequency domain parameters for PI compensated DC-DC Cuk converter with original and reduced second-order model

Compensated system	**Gain Margin**	**Phase Margin**	**Gain crossover frequency**
With original model	inf	103°	20.7 Hz
With reduced second-order model	inf	103°	22 Hz

4.3.2.3 Results and discussion

In this section, the PI controller transfer function derived from the reduced second-order model of Cuk converter is implemented for obtaining the simulation and experimental results of actual fourth-order Cuk converter. The transfer function of PI controller used for these results are given in (4.99). This transfer function is implemented on Cuk converter prototype using dSPACE controller for obtaining the experimental results. The simulation and experimental results are obtained for three different operating conditions.

(a) Variation in reference output voltage

(b) Variation in input voltage

(c) Variation in load current

(a) Variation in reference output voltage

In this case, the reference output voltage ($V_{o,ref}$) is varied while keeping the input voltage (V_g) and load resistance (R) constant to 20 V and 11 Ω, respectively. For the reference voltage variation from 16 V to 12 V and vice-versa, the simulation and experimental results are shown in Fig. 4.61 (a). Similarly, for the reference voltage variation from 16 V to 20 V and vice-versa, the corresponding simulation and experimental results are shown in Fig. 4.61 (b). It is observed that the output voltage reaches to the new desired value within 50-60 ms without any overshoot/undershoot and oscillations. The simulation and experimental results are in close agreement.

(b) Variation in input voltage

The simulation and experimental results are obtained for step variation in input voltage while keeping the load conditions constant. The variation in input voltage (V_g) is considered from minimum (20 V) to maximum (28 V) and vice-versa for two extreme load conditions R=11 Ω (*i.e.,* maximum load current, 1.45 A) and R=22 Ω (*i.e.,* minimum load current, 0.73 A). The desired output voltage is 16 V. For the fixed load resistance of 11 Ω, when the input voltage varies from 20 V to 28 V and vice-versa, the results are shown in Fig. 4.62 (a) and Fig. 4.62 (b). Similarly, for the fixed load of 22 Ω, when the input voltage varies from 20 V to 28 V, the respective results are shown in Fig. 4.63 (a) and Fig. 4.63 (b). These results indicate that when the input voltage is increased from 20 V to 28 V, the output voltage settles to steady-state (16 V) within 50-60 ms. However, during transients, the output voltage faces overshoot of 5.6-6.6 V and undershoot of 1.6 V. Similarly, when the input voltage is decreased from 28 V to 20 V, the output voltage settles in 60-75 ms. It has undershoot of 4-5.4 V and overshoot of 1.6-4 V. The experimental results match with the simulation results. The experimental results slightly vary from simulation results during transients because the step change in input voltage was realized using a manual switch.

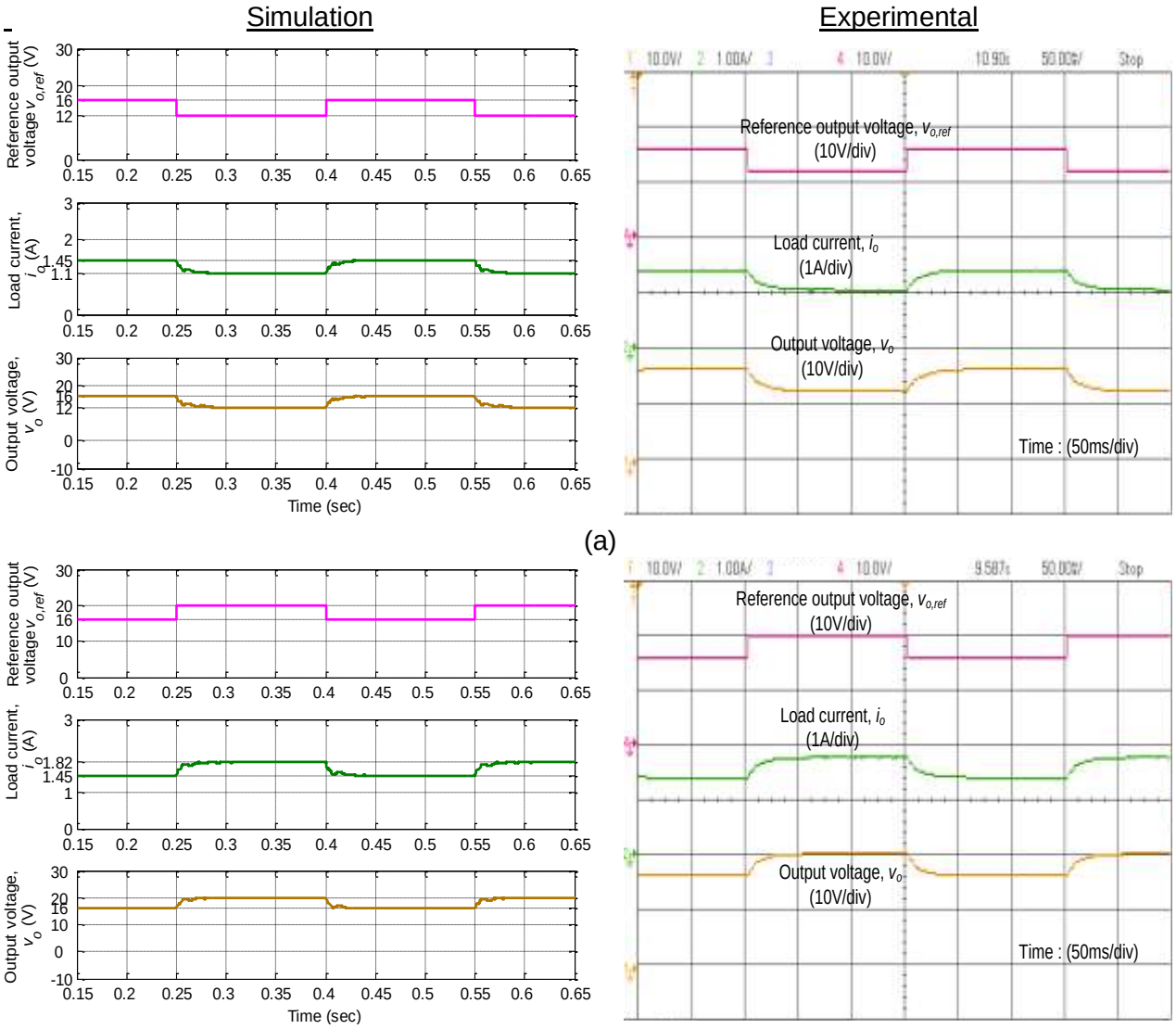
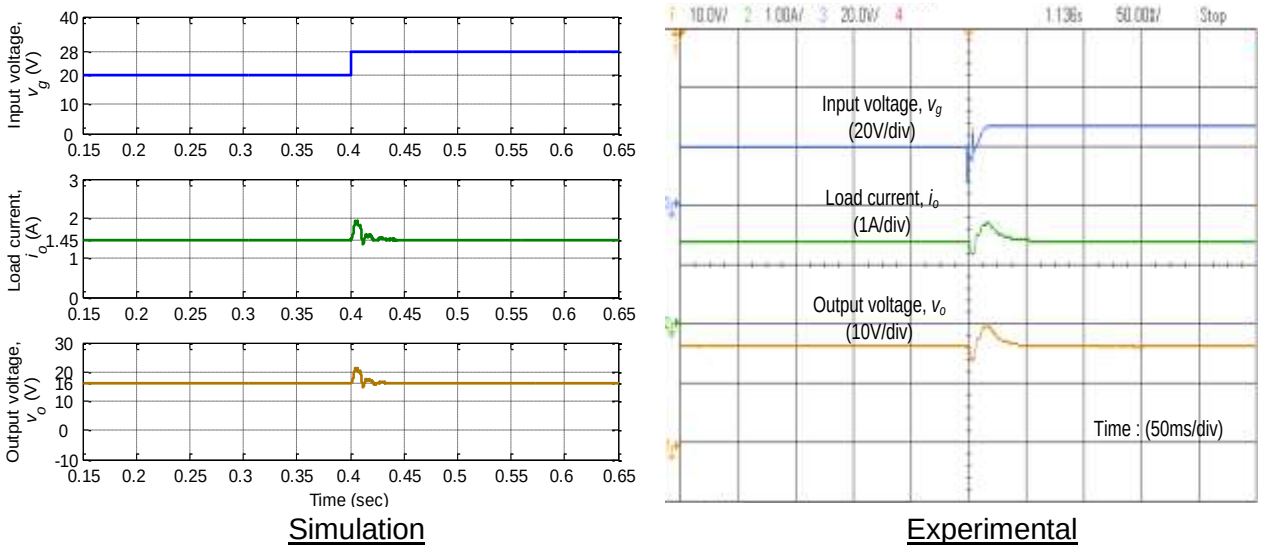
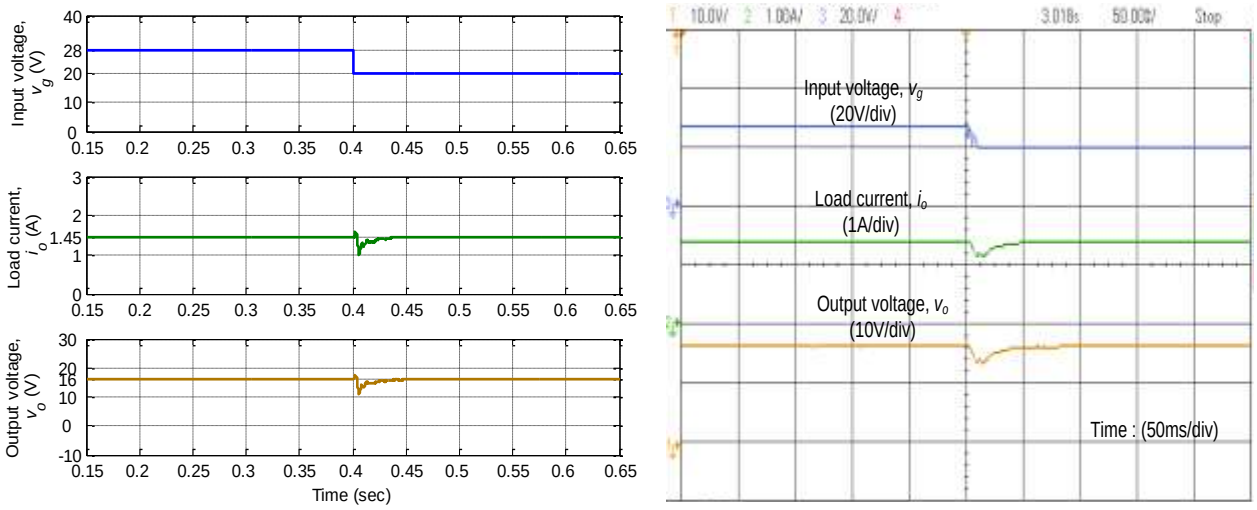


Fig. 4.61. Simulation and experimental results for reference output voltage variation from (a) 16 V to 12 V and vice-versa (b) 16 V to 20 V and vice-versa

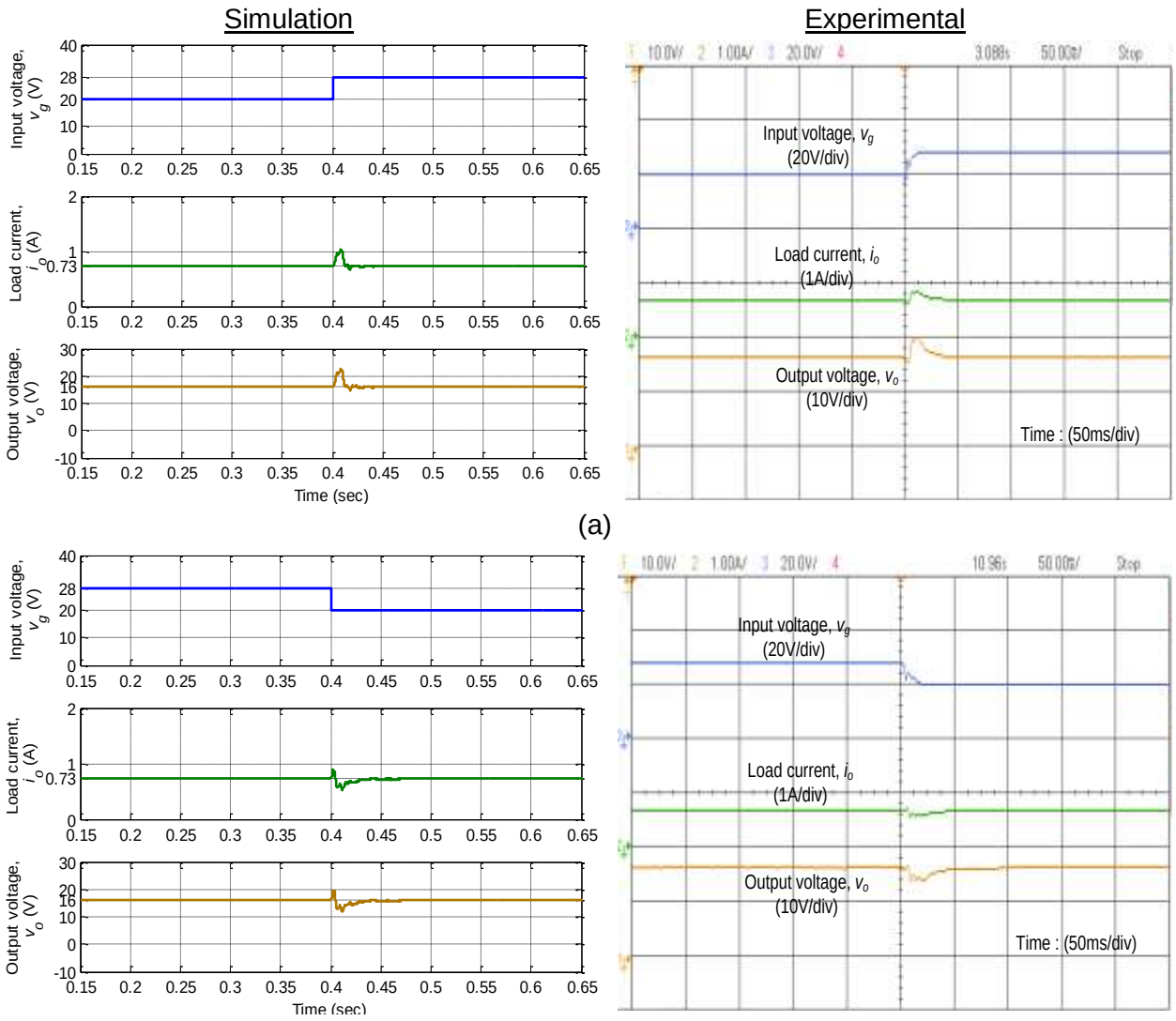




Simulation Experimental

(b)

Fig. 4.62. Simulation and experimental results with R=11 Ω for input voltage variation from (a) 20 V to 28 V (b) 28 V to 20 V



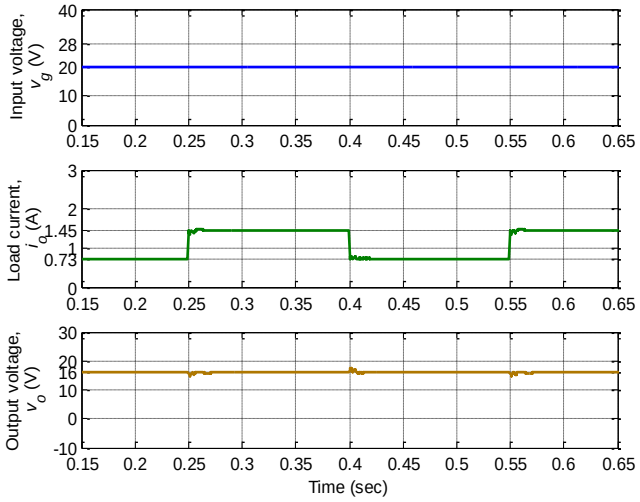
(a)

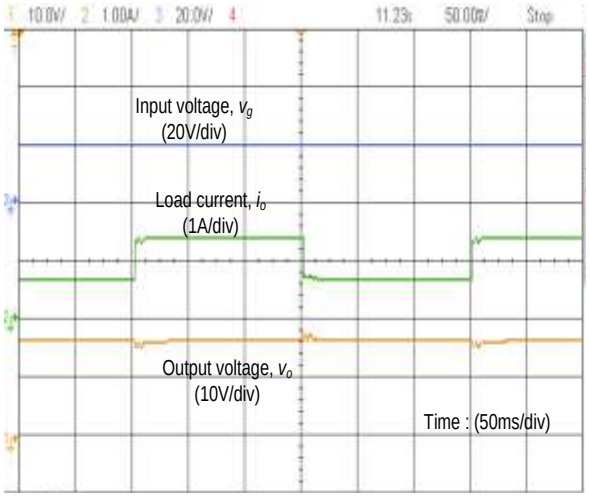
(b)

Fig. 4.63. Simulation and experimental results with R=22 Ω for input voltage variation from (a) 20 V to 28 V (b) 28 V to 20 V

(c) Variation in load resistance or load current

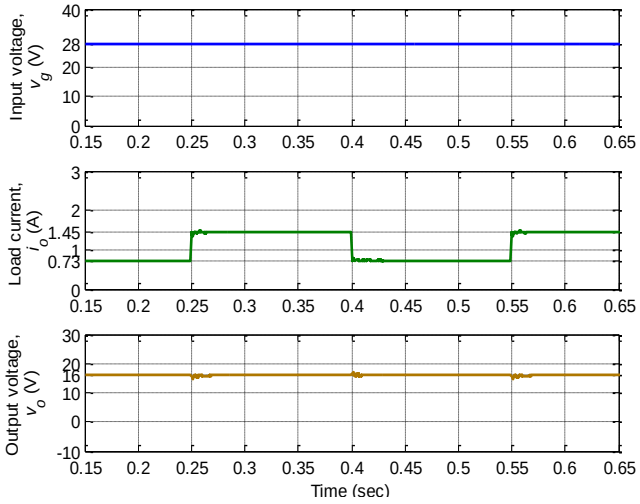
In this case, the performance is observed for variations in load conditions while keeping the input voltage constant. The load resistance (R) is varied from 22 Ω (*i.e.,* minimum load current, 0.73 A) to 11 Ω (*i.e.,* maximum load current, 1.45 A) and vice-versa for two extreme input voltages V_g=20 V (minimum) and V_g=28 V (maximum). The desired output voltage is 16 V. In Fig. 4.64 (a), the simulation and experimental results have been shown for step variation in load resistance from 22 Ω to 11 Ω and vice-versa at fixed input voltage 20 V. Similarly, Fig. 4.64 (b) shows the results for same load variation, but at fixed input voltage 28 V. These results indicate that the output voltage settles within 50 ms. For load variation from 22 Ω to 11 Ω, the output voltage has slight oscillations with the undershoot of 1.2 V and overshoot of 0.4 V. On the other hand, when the load is shifted from 11 Ω to 22 Ω, the output voltage has overshoot of 1.6 V and undershoot of 0.4 V. The experimental results are in close agreement with the simulation results.

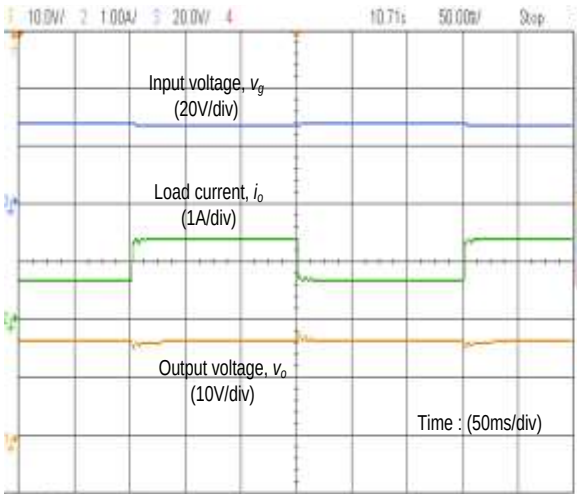




Simulation Experimental

(a)





Simulation Experimental

(b)

Fig. 4.64. Simulation and experimental results for variation in load resistance from 22 Ω to 11 Ω and vice-versa at input voltage (a) V_g=20 V (b) V_g=28 V

4.3.3 PI-lead controller design

In this section, the PI-lead controller is designed for DC-DC Cuk converter. The performance of this PI-lead controller is evaluated through simulation and experimental results.

4.3.3.1 Description of control scheme

The block diagram of the PI-lead controlled DC-DC Cuk converter is shown in Fig. 4.65. The explanation of this block diagram is same as given for block diagram in Fig. 4.47. The only difference lies in the control scheme implemented. In this scheme, PI-lead controller is used instead of PI controller.

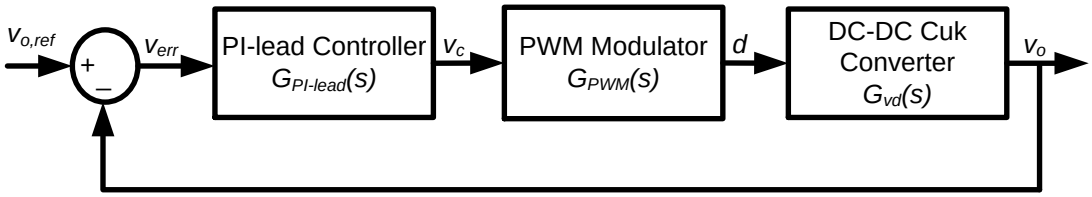


Fig. 4.65. Block diagram of closed-loop PI-lead control of DC-DC Cuk converter

The loop transfer function of the uncompensated Cuk converter remains same as obtain in (4.88) and its Bode plot has earlier been plotted in Fig. 4.49. The phase margin of uncompensated Cuk converter is 22.1° at gain crossover frequency of 1.09 kHz. A PI controller was designed in section 4.3.1.1 to improve the phase margin of this Cuk converter. The desired phase margin was successfully achieved by the designed PI controller, but the gain crossover frequency was decreased to very low value, which results in sluggish response of the compensated system. Therefore, in order to maintain the desired gain crossover frequency at desired phase margin, PI-lead controller is designed for Cuk converter also similar to buck converter. The more details about PI-lead controller have already been discussed in section 4.2.2.

Let consider the PI-lead controller for DC-DC Cuk converter under consideration is designed to obtain phase margin 90° at gain crossover frequency of 2 kHz. Also consider that the corner frequency of PI section of PI-lead controller is selected 100 Hz. The algorithm to design PI-lead controller parameters has already been given in section 4.2.2.1. Therefore, by substituting f_z=100 Hz, φ_{margin}=90°, f_{gc}=2 kHz into (4.47)-(4.49), we get the lead section parameters as K=7406.6, α=3332 and β=4.739×10^4. The complete PI-lead controller transfer function is

$$G_{PI-lead}(s)=\frac{7406.6\times(0.001592s+1)(s+3332)}{s(s+4.739\times10^4)} \tag{4.100}$$

Therefore, loop transfer function of PI-lead controlled system is

$$G_{PI-lead}(s)T(s) = \frac{7406.6\times(0.001592s+1)(s+3332)}{s(s+4.739\times10^4)}\cdot\frac{2000s^3+4.342\times10^7s^2+3.692\times10^9s+1.865\times10^{13}}{s^4+594.2s^3+1.836\times10^6s^2+3.949\times10^8s+3.224\times10^{11}} \quad (4.101)$$

The frequency responses of PI-lead controlled DC-DC Cuk converter is shown in Fig. 4.66. The desired phase margin of 90° is attained at gain crossover frequency of 2 kHz, which was the objective of this controller design. These performance specifications are met exactly as specified. The gain in low-frequency region has been increased with slope of -20 dB/decade. It eliminates the steady-state error for any step disturbance. The increased gain crossover frequency helps in faster speed of response.

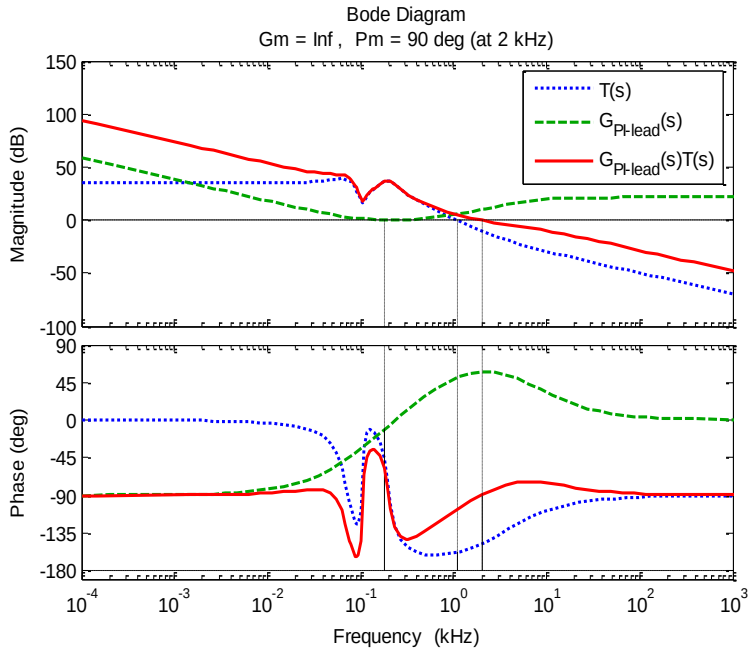


Fig. 4.66. Frequency response of PI-lead compensated DC-DC Cuk converter

4.3.3.2 Results and discussion

The proposed PI-lead controller for the DC-DC Cuk converter is verified through simulation and experimental results. The PI-lead controller transfer function have been derived in (4.100). This PI-lead controller is implemented using dSAPCE system on the Cuk converter hardware prototype. The experimental setup remains same as used for PI controller, except replacing the PI controller transfer function by PI-lead controller transfer function.

The simulation and experimental results are obtained for three different conditions:

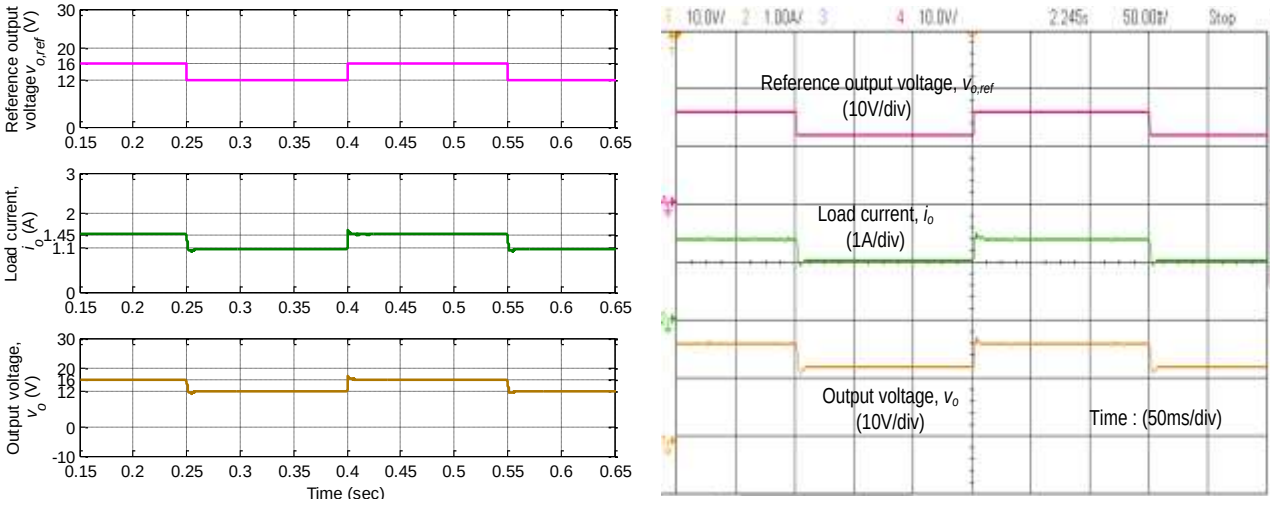
(a) Variation in reference output voltage

(b) Variation in input voltage

(c) Variation in load current

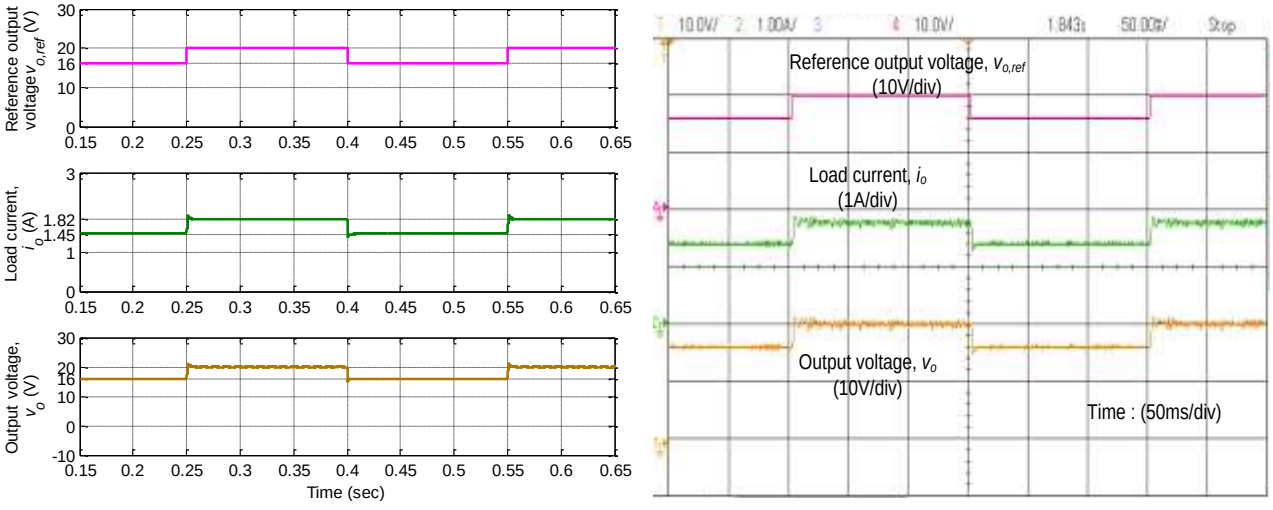
(a) Variation in reference output voltage

The performance of PI-lead controller for Cuk converter is observed for step variation in reference output voltage ($V_{o,ref}$). The input voltage (V_g) and load resistance (R) are kept fixed to 20 V and 11 Ω, respectively. When the reference voltage decreases from 16 V to 12 V and vice-versa, the simulation and experimental results are shown in Fig. 4.67 (a) and when it increases from 16 V to 20 V and vice-versa, the respective simulation and experimental results are shown in Fig. 4.67 (b). It is observed that the output voltage smoothly reaches to the new desired value within 30-40 ms. The simulation and experimental results are in close agreement. The steady-state load current is 1.09 A, 1.45 A and 1.81 A for desired output voltage 12 V, 16 V and 20 V, respectively. The simulation and experimental results are almost same.



Simulation Experimental

(a)



Simulation Experimental

(b)

Fig. 4.67. Simulation and experimental results for reference output voltage variation from (a) 16 V to 12 V and vice-versa (b) 16 V to 20 V and vice-versa

(b) Variation in input voltage

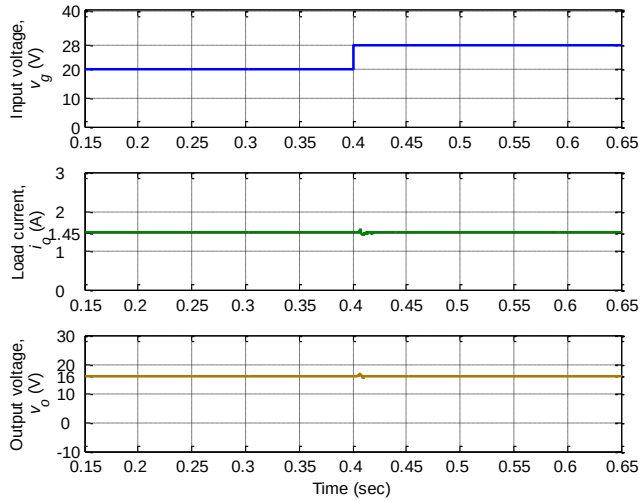
In this case, the simulation and experimental results are obtained for step variation in input voltage at fixed load resistance. The variation in input voltage (V_g) is considered from minimum (20 V) to maximum (28 V) and vice-versa for two extreme load conditions R=11 Ω (*i.e.,* maximum load current, 1.45 A) and R=22 Ω (*i.e.,* minimum load current, 0.73 A). The desired output voltage is 16 V.

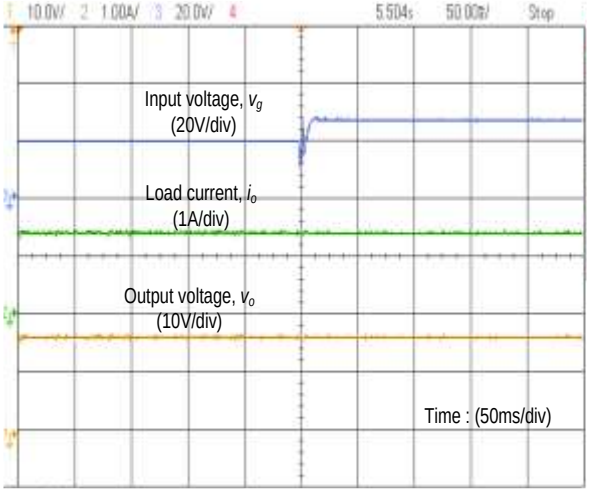
For the fixed load of 11 Ω, when the input voltage is varied from 20 V to 28 V and vice-versa, the results are shown in Fig. 4.68 (a) and Fig. 4.68 (b), respectively. Similarly, for the fixed load of 22 Ω, when the input voltage is varied from 20 V to 28 V and vice-versa, the results are shown in Fig. 4.69 (a) and Fig. 4.69 (b), respectively. These results demonstrate that when the input voltage increases from 20 V to 28 V, the output voltage settles within 25-30 ms. It has overshoot of 1-3.6 V and undershoot of 0.7-1.6 V. When the input voltage decreases from 28 V to 20 V, the output voltage settles within 40 ms with undershoot of 1.2-2.2 V and overshoot of 1.6-4 V. The slight differences in the experimental and simulations results are observed during transient, because for the experimental results, the step change in input voltage was realized using a manual switch.

(c) Variation in load resistance or load current

In this case, the performance of PI-lead controller is observed for variations in load resistance while keeping the input voltage constant. The load resistance (R) is varied from 22 Ω (*i.e.,* minimum load current, 0.73 A) to 11 Ω (*i.e.,* maximum load current, 1.45 A) and vice-versa for two extreme input voltages V_g=20 V (minimum) and V_g=28 V (maximum). The desired output voltage is 16 V.

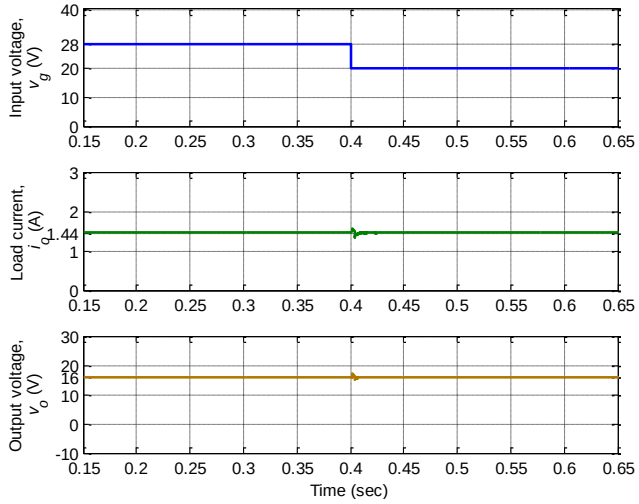
The simulation and experimental results for step variation in load resistance from 22 Ω to 11 Ω and vice-versa at constant input voltage 20 V are shown in Fig. 4.70 (a) and at constant input voltage 28 V, the results are displayed in Fig. 4.70 (b). The results present that the output voltage reaches to steady-state value within 30 ms. When the load is switched 22 Ω to 11 Ω and vice-versa, the output voltage experiences the oscillations with maximum overshoots and undershoots of 0.2-0.4 V. The experimental results validate the MATLAB simulation results.

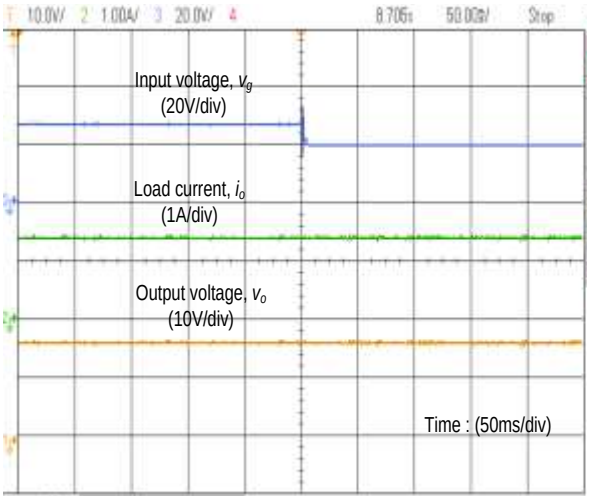




Simulation Experimental

(a)

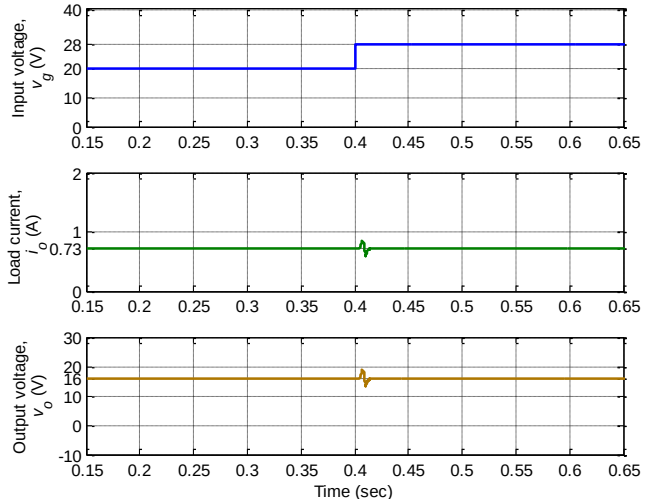


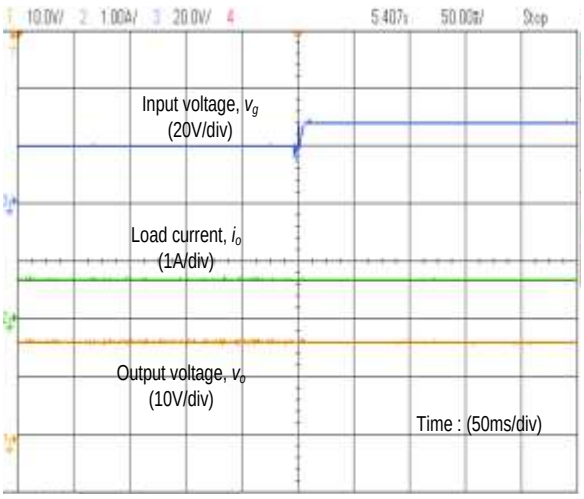


Simulation Experimental

(b)

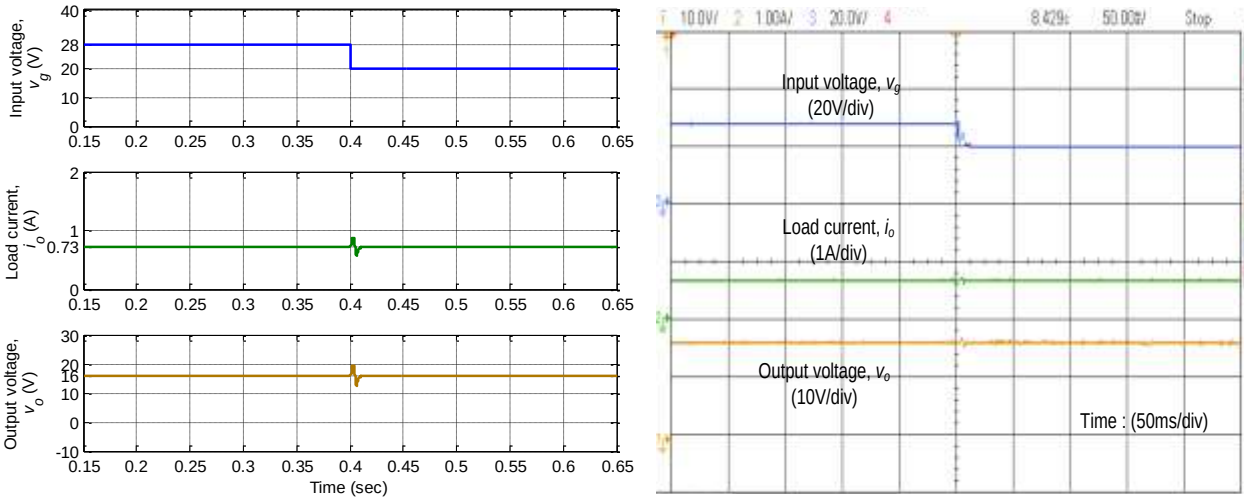
Fig. 4.68. Simulation and experimental results with R=11 Ω for input voltage variation from (a) 20 V to 28 V (b) 28 V to 20 V





Simulation Experimental

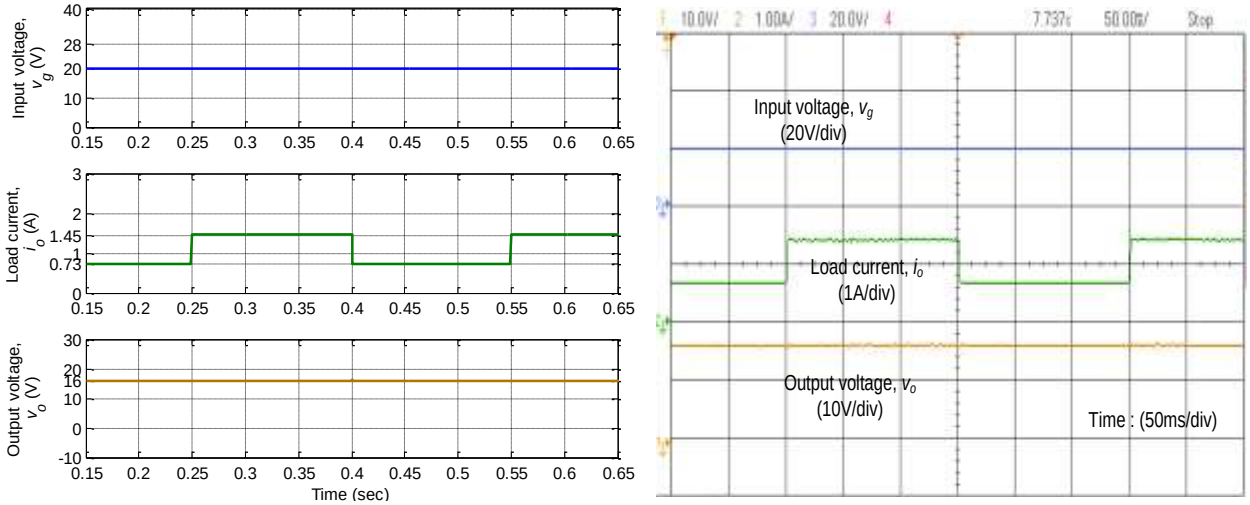
(a)



Simulation Experimental

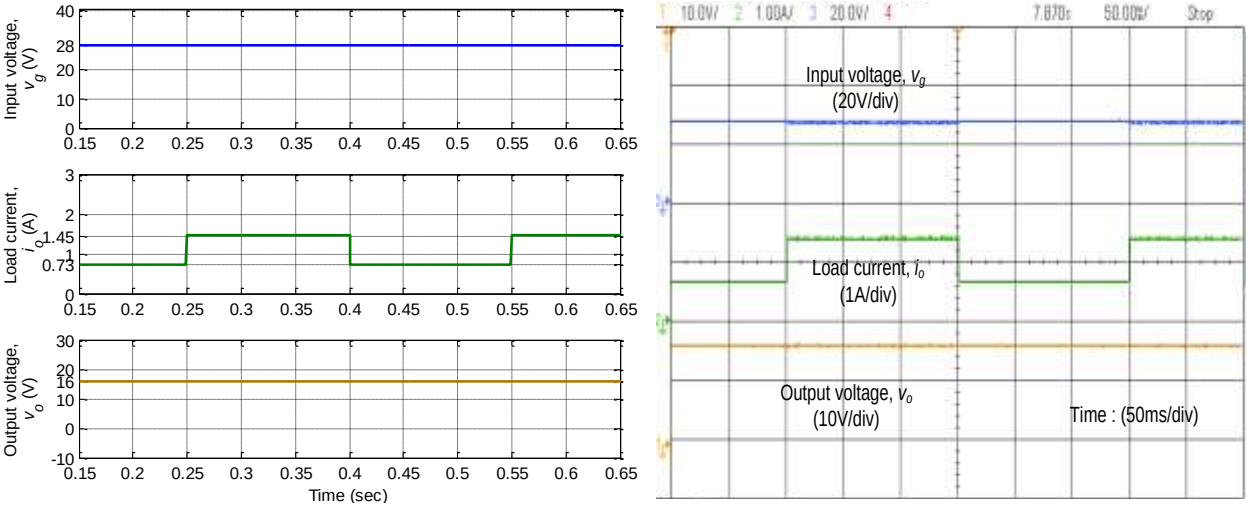
(b)

Fig. 4.69. Simulation and experimental results with R=22 Ω for input voltage variation from (a) 20 V to 28 V (b) 28 V to 20 V



Simulation Experimental

(a)



Simulation Experimental

(b)

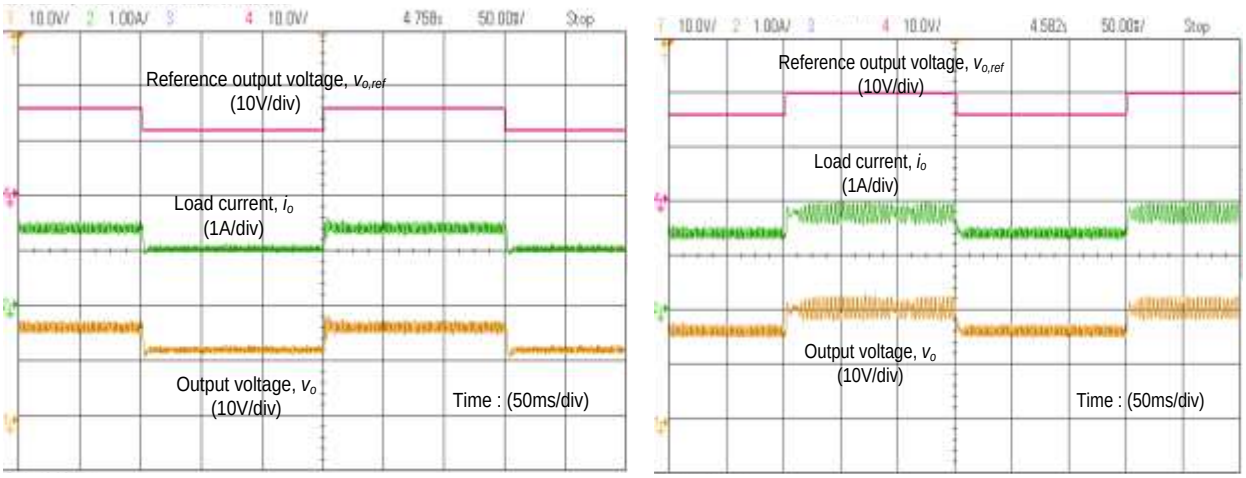
Fig. 4.70. Simulation and experimental results for variation in load resistance from 22 Ω to 11 Ω and vice-versa at input voltage (a) V_g=20 V (b) V_g=28 V

The PI-lead controller in (4.100) was derived for Cuk converter based on specified frequency domain specifications (phase margin 90° at 2 kHz). From the simulation and experimental results, it was observed that the output voltage settles within 25-40 ms under different working conditions. With PI controller, the settling time was noted 45-75 ms. Thus, the settling time has been improved with the use of PI-lead controller. This is because of the higher gain crossover frequency of PI-lead controlled Cuk converter in comparison to PI controller.

In order to verify the performance of PI-lead controller at 4 kHz gain crossover frequency, the experimental results are obtained. The transfer function of the PI-lead controller at 4 kHz gain crossover frequency is derived using the algorithm proposed in section 4.2.2.1, keeping f_z=100 Hz and φ_{margin}=90°. The transfer function is

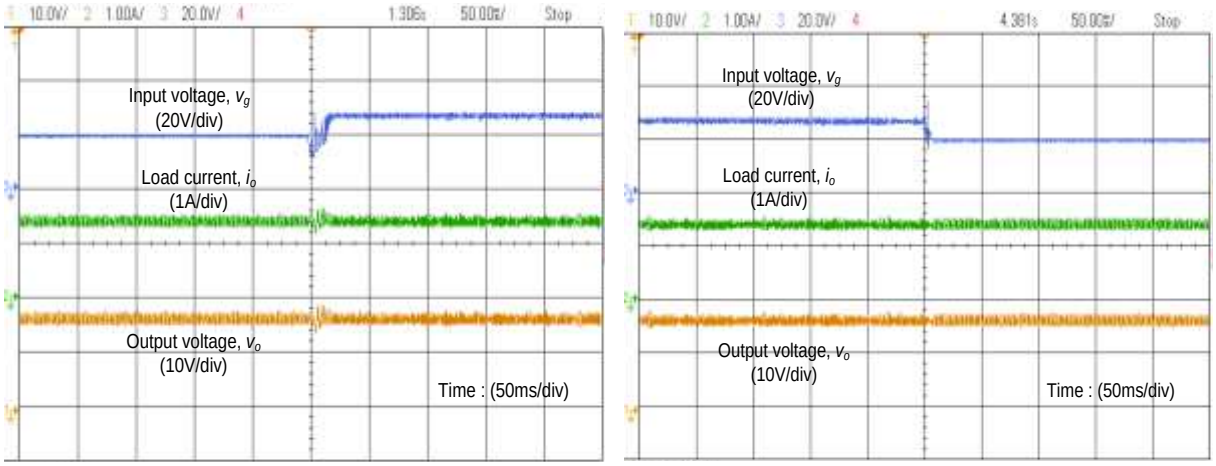
$$G_{PI-lead}(s) = \frac{13086 \times (0.001592s + 1)(s + 1.146 \times 10^4)}{s(s + 5.51 \times 10^4)} \tag{4.102}$$

The experimental results are obtained under different conditions by implementing the PI-lead controller in (4.102) on the Cuk converter prototype using dSPACE. These experimental results are shown in Fig. 4.71 to Fig. 4.74 for variations in reference output voltage, input voltage and load current. All these results demonstrate that the output voltage contains noise signal with this PI-lead controller. Therefore, it is not advisable to use this PI-lead controller designed at 4 kHz crossover frequency for the output voltage regulation of Cuk converter.



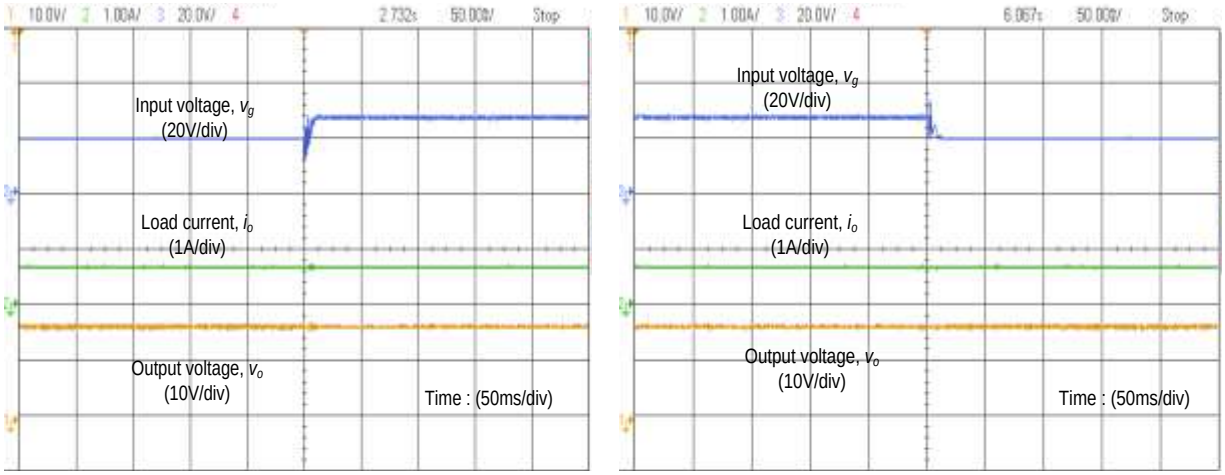
(a) (b)

Fig. 4.71. Experimental results of PI-lead controlled Cuk converter (at 4 kHz GCF) for reference output voltage variation from (a) 16 V to 12 V and vice-versa (b) 16 V to 20 V and vice-versa



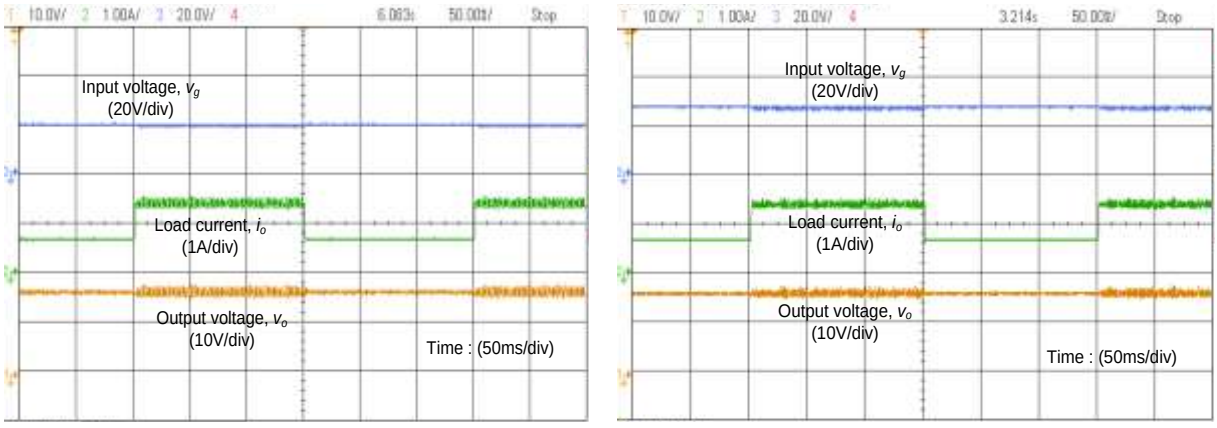
(a) (b)

Fig. 4.72. Experimental results of PI-lead controlled Cuk converter (at 4 kHz GCF) for load resistance 11 Ω and input voltage variation from (a) 20 V to 28 V (b) 28 V to 20 V



(a) (b)

Fig. 4.73. Experimental results of PI-lead controlled Cuk converter (at 4 kHz GCF) for load resistance 22 Ω and Input voltage variation from (a) 20 V to 28 V (b) 28 V to 20 V



(a) (b)

Fig. 4.74. Experimental results of PI-lead controlled Cuk converter (at 4 kHz GCF) for load resistance variation from 22 Ω to 11 Ω and vice-versa at input voltage (a) V_g=20 V (b) V_g=28 V

4.3.4 Two-loop PI controller design

The two-loop PI controller design for DC-DC buck converter has already been implemented. In this section, this scheme is used to regulate the output voltage of DC-DC Cuk converter. The block diagram of two-loop PI control of Cuk converter is shown in Fig. 4.75. As shown in the figure, there is two control loops, namely inner current control loop and outer voltage control loop. These two PI controllers $G_{c1}(s)$ and $G_{c2}(s)$ are designed to regulate the dc output voltage of Cuk converter. The Cuk converter model is represented by duty cycle to inductor current (i_{L1}) transfer function $G_{id}(s)$ and inductor current to output voltage transfer function $G_{vi}(s)$. The detailed schematic of this control scheme for Cuk converter is shown in Fig. 4.76.

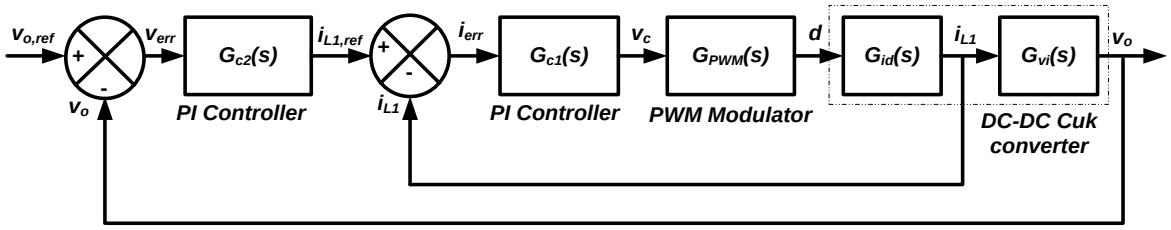


Fig. 4.75. Complete block diagram for closed two-loop PI control of DC-DC Cuk converter

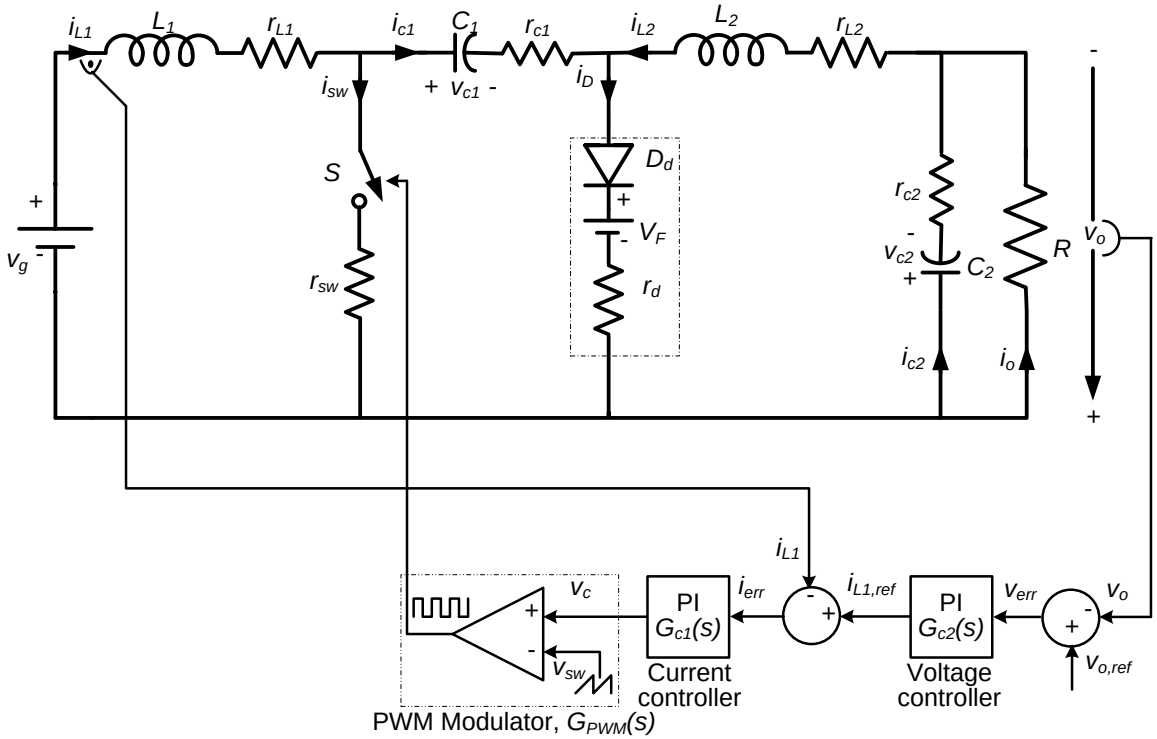


Fig. 4.76. Detailed schematic for closed two-loop PI control of DC-DC Cuk converter

The specifications of Cuk converter are same as taken in previous controller design schemes and are given in Table 4.9. The various transfer functions required for two-loop PI control scheme are obtained using the derivations carried out in chapter 3. Therefore, by substituting these converter parameters values, for input voltage V_g=20 V and R=11 Ω, we obtain:

Duty cycle to output voltage transfer function

$$G_{vd}(s)=\frac{\tilde{v}_o(s)}{\tilde{d}(s)}=\frac{2000s^3+4.342\times10^7s^2+3.692\times10^9s+1.865\times10^{13}}{s^4+594.2s^3+1.836\times10^6s^2+3.949\times10^8s+3.224\times10^{11}} \quad (4.103)$$

Duty cycle to inductor current transfer function

$$G_{id}(s)=\frac{\tilde{i}_{L1}(s)}{\tilde{d}(s)}=\frac{1.172\times10^4s^3+6.068\times10^6s^2+2.191\times10^{10}s+2.726\times10^{12}}{s^4+594.2s^3+1.836\times10^6s^2+3.949\times10^8s+3.224\times10^{11}} \quad (4.104)$$

Inductor current to output voltage transfer function

$$G_{vi}(s)=\frac{\tilde{v}_o(s)}{\tilde{i}_{L1}(s)}=\frac{2000s^3+4.342\times10^7s^2+3.692\times10^9s+1.865\times10^{13}}{1.172\times10^4s^3+6.068\times10^6s^2+2.191\times10^{10}s+2.726\times10^{12}} \quad (4.105)$$

4.3.4.1 Inner current control loop (ICCL) design

The block diagram for inner current control loop for DC-DC Cuk converter is shown in Fig. 4.77. The actual inductor current i_{L1} is compared with the reference inductor current $i_{L1,ref}$. The resultant inductor current error i_{err} is then passed through PI controller $G_{c1}(s)$. The output of PI controller is modulating signal or control voltage v_c, which is compared (in PWM modulator block) with the sawtooth signal of fixed magnitude and frequency to continuously monitor the duty cycle of the switching pulses.

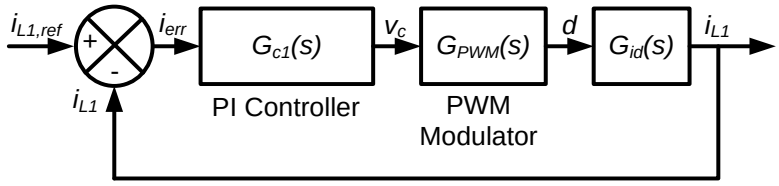


Fig. 4.77. Block diagram of inner current control loop for Cuk converter

In this case, the loop transfer function of uncompensated system is

$$T_1(s)=G_{PWM}(s)G_{id}(s)=\frac{1.172\times10^4s^3+6.068\times10^6s^2+2.191\times10^{10}s+2.726\times10^{12}}{s^4+594.2s^3+1.836\times10^6s^2+3.949\times10^8s+3.224\times10^{11}} \quad (4.106)$$

Here, $G_{PWM}(s)=1/V_{sw}$ is the transfer function of PWM modulator, V_{sw} is peak voltage of sawtooth waveform. $V_{sw}=1$ is taken for this design.

The frequency response of uncompensated system $T_1(s)$ is shown in Fig. 4.78. It has constant gain in low-frequency region. The gain margin is infinite and phase margin is 90.4° at 1.86 kHz gain crossover frequency. The phase margin is good but due to constant low-frequency gain, it will have steady-state error in inductor current. Therefore, a PI controller $G_{c1}(s)$ is designed to increase the low-frequency gain and thus, to reduce the steady-state error between actual inductor current and reference inductor current. Let the transfer function of $G_{c1}(s)$ be

$$G_{c1}(s)=\frac{K_{p1}s+K_{i1}}{s} \quad (4.107)$$

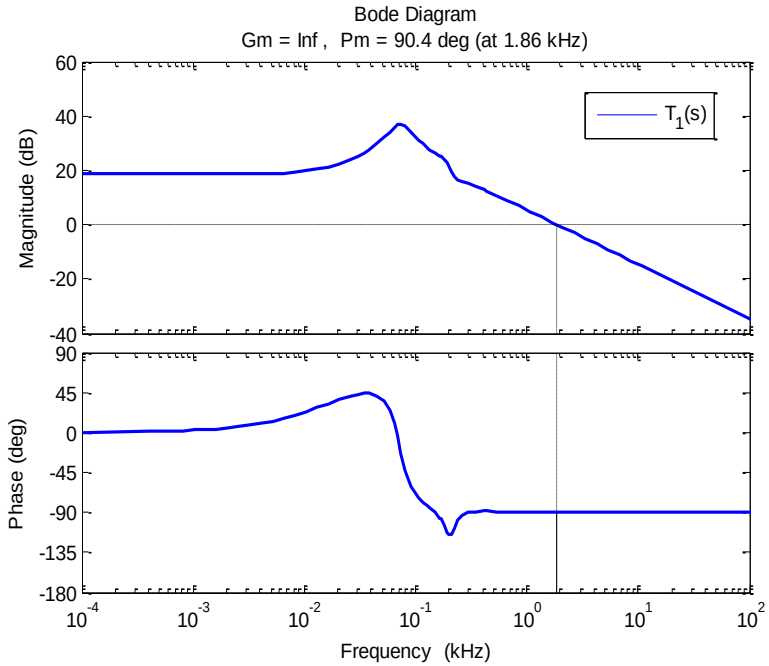


Fig. 4.78. Frequency response of uncompensated current control loop of Cuk converter

Comparing (4.106) with (4.56),

$$b_4=0, b_3=1.172\times10^4, b_2=6.068\times10^6, b_1=2.191\times10^{10}, b_0=2.7267\times10^{12},$$
$$a_4=1, a_3=594.2, a_2=1.836\times10^6, a_1=3.949\times10^8, a_0=3.224\times10^{11} \quad (4.108)$$

The controller parameters K_{p1} and K_{c1} are tuned in terms of specified phase margin and gain crossover frequency using the proposed formulae in section 4.2.3.1. Therefore, substituting values of coefficients from (4.108) into (4.65)-(4.66), we get

$$K_{p1}(\omega_c,\varphi)=\frac{\left(\begin{array}{c}-1.17\times10^4\sin\varphi\omega_c^7+8.95\times10^5\cos\varphi\omega_c^6+3.98\times10^{10}\sin\varphi\omega_c^5-3.78\times10^{12}\cos\phi\omega_c^4-\\ 4\times10^{16}\sin\varphi\omega_c^3+1.69\times10^{18}\cos\varphi\omega_c^2+5.99\times10^{21}\sin\varphi\omega_c+8.79\times10^{23}\cos\varphi\end{array}\right)}{-\left(1.373\times10^8\omega_c^6-4.77\times10^{14}\omega_c^4+4.47\times10^{20}\omega_c^2+7.43\times10^{24}\right)} \quad (4.109)$$

$$K_{i1}(\omega_c,\varphi)=\frac{\omega_c\left(\begin{array}{c}-1.17\times10^4\sin\varphi\omega_c^7-8.95\times10^5\cos\varphi\omega_c^6+3.98\times10^{10}\sin\varphi\omega_c^5+3.78\times10^{12}\cos\phi\omega_c^4-\\ 4\times10^{16}\sin\varphi\omega_c^3-1.69\times10^{18}\cos\varphi\omega_c^2+5.99\times10^{21}\sin\varphi\omega_c-8.79\times10^{23}\cos\varphi\end{array}\right)}{-\left(1.373\times10^8\omega_c^6-4.77\times10^{14}\omega_c^4+4.47\times10^{20}\omega_c^2+7.43\times10^{24}\right)} \quad (4.110)$$

For inner current control loop, the PI controller parameters are tuned to give phase margin of 90° at 4 kHz gain crossover frequency. Therefore, substituting $\omega_c=2\pi.4\text{x}10^3=8000\pi$ and $\varphi=90°$ in (4.109) and (4.110), we get $K_{p1}=2.145$ and $K_{i1}=163.6$.

The frequency response of the compensated current control loop is shown in Fig. 4.79. It can be observed that the desired phase margin 90° and gain crossover frequency 4 kHz are obtained and gain of compensated system in low-frequency region has been improved with this PI controller.

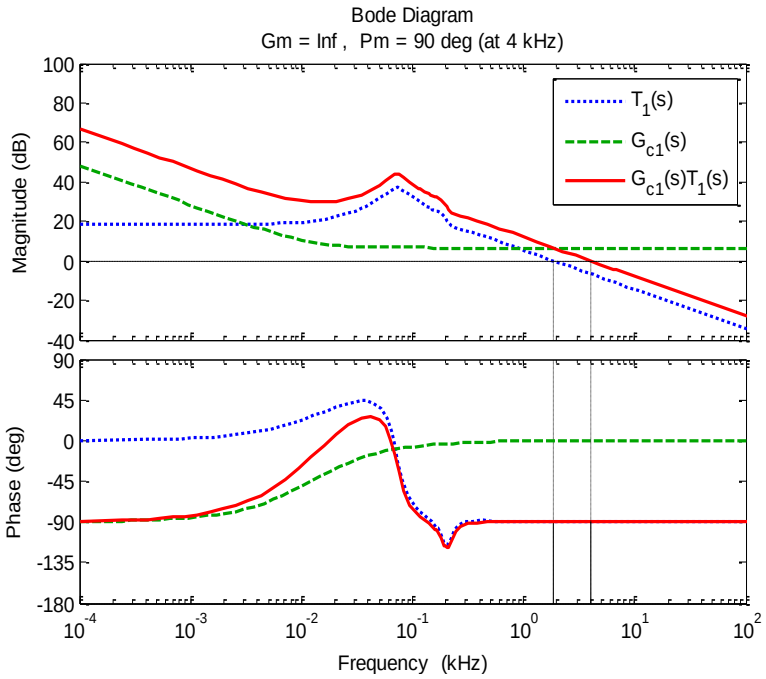


Fig. 4.79. Frequency response of compensated current control loop of Cuk converter

4.3.4.2 Outer voltage control loop (OVCL) design

The block diagram of the outer voltage control loop of Cuk converter is shown in Fig. 4.80 (a). As shown in the figure, the current loop dynamics has been collectively represented a separate block. However, as the inner current control loop is must faster than the outer voltage control loop and therefore, in order to simplify the controller design for outer loop, this current loop dynamics can also be neglected. It was proved earlier in this chapter for two-loop control of DC-DC buck converter that the outer voltage controller design is not much affected by the inner current control loop dynamics. The block diagram in Fig. 4.80 (b) shows the outer voltage control loop of Cuk converter when the current control loop dynamics is neglected.

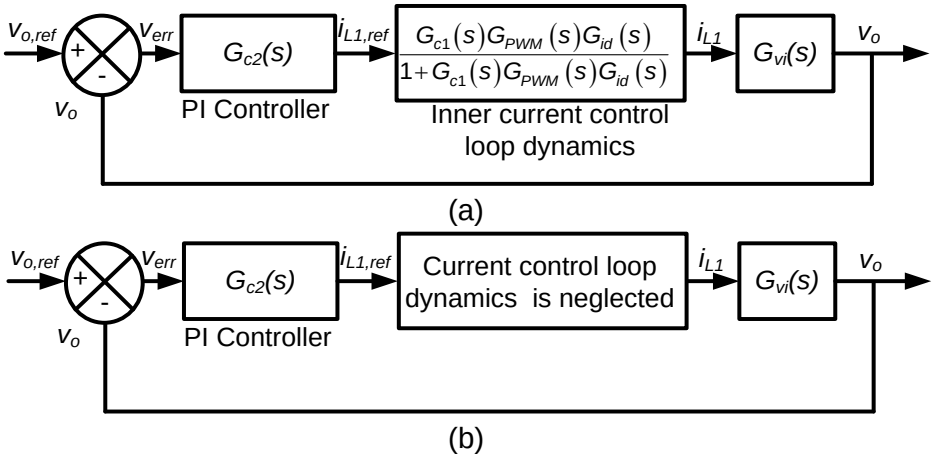


Fig. 4.80. Block diagram of outer voltage control loop of Cuk converter (a) with current control loop dynamics (b) without current control loop dynamics

The purpose of outer voltage control loop (OVCL) is to generate the reference inductor current $i_{L1,ref}$. In this control loop, the actual output voltage v_o is compared with the reference output voltage $v_{o,ref}$. The resultant voltage error is passed through PI controller $G_{c2}(s)$ to produce the reference inductor current $i_{L1,ref}$ for the inner current control loop.

The loop transfer function of uncompensated voltage control loop with current loop dynamics will be

$$T_2(s) = \frac{G_{c1}(s)G_{PWM}(s)G_{id}(s)}{1+G_{c1}(s)G_{PWM}(s)G_{id}(s)} \cdot G_{vi}(s) \tag{4.111}$$

Substituting respective values,

$$T_2(s) = \frac{\begin{array}{c}5.03\times10^{7}s^{7}+1.21\times10^{12}s^{6}+8.37\times10^{14}s^{5}+2.63\times10^{18}s^{4}\\ +8.66\times10^{20}s^{3}+9.49\times10^{23}s^{2}+1.78\times10^{26}s+8.32\times10^{27}\end{array}}{\begin{array}{c}1.17\times10^{4}s^{8}+3.08\times10^{8}s^{7}+3.75\times10^{11}s^{6}+1.23\times10^{15}s^{5}+8.46\times10^{17}s^{4}\\ +1.17\times10^{21}s^{3}+3.48\times10^{23}s^{2}+3.64\times10^{25}s+1.22\times10^{27}\end{array}} \tag{4.112}$$

If the inner current control loop dynamics is neglected, the loop transfer function of uncompensated voltage control loop is same as the inductor current to output voltage transfer function, $G_{vi}(s)$. It is rewritten below:

$$G_{vi}(s) = \frac{2000s^{3}+4.342\times10^{7}s^{2}+3.692\times10^{9}s+1.865\times10^{13}}{1.172\times10^{4}s^{3}+6.068\times10^{6}s^{2}+2.191\times10^{10}s+2.726\times10^{12}} \tag{4.113}$$

Here, the PI controller for voltage control loop will be designed by considering the inner current control loop dynamics neglected becuase the inner current loop dynamics is always faster than the outer voltage loop dynamics. Let the transfer function of PI controller $G_{c2}(s)$ be

$$G_{c2}(s) = \frac{K_{p2}s + K_{i2}}{s} \tag{4.114}$$

Comparing (4.113) with (4.56),

$$\begin{array}{l}b_4=0, b_3=2000, b_2=4.34\times10^{7}, b_1=3.69\times10^{9}, b_0=1.865\times10^{13},\\ a_4=0, a_3=1.172\times10^{4}, a_2=6.07\times10^{6}, a_1=2.19\times10^{10}, a_0=2.726\times10^{12}\end{array} \tag{4.115}$$

The PI controller parameters K_{p2} and K_{c2} are tuned to have phase margin of 90° at 50 Hz gain crossover frequency using the proposed formulae in section 4.2.3.1. The gain crossover frequency of voltage control loop is specified much lower than the crossover frequency of inner current loop to ensure the faster operation of the current loop.

Substituting values of coefficients from (4.115) into (4.65)-(4.66), we get

$$K_{p2}(\omega_c,\varphi) = \frac{\left(\begin{array}{c}2.34\times10^{7}\cos\varphi\omega_c^{6}-4.97\times10^{11}\sin\varphi\omega_c^{5}+1.76\times10^{14}\cos\phi\omega_c^{4}+\\ 1.14\times10^{18}\sin\varphi\omega_c^{3}-1.51\times10^{20}\cos\varphi\omega_c^{2}-3.98\times10^{23}\sin\varphi\omega_c+5.08\times10^{25}\cos\varphi\end{array}\right)}{-\left(4\times10^{6}\omega_c^{6}+1.87\times10^{15}\omega_c^{4}-1.61\times10^{21}\omega_c^{2}+3.48\times10^{26}\right)} \tag{4.116}$$

$$K_{i2}(\omega_c,\varphi) = \frac{\omega_c\left(\begin{array}{c}-2.34\times10^{7}\cos\varphi\omega_c^{6}-4.97\times10^{11}\sin\varphi\omega_c^{5}-1.76\times10^{14}\cos\phi\omega_c^{4}+1.14\times10^{18}\\ \sin\varphi\omega_c^{3}+1.51\times10^{20}\cos\varphi\omega_c^{2}-3.98\times10^{23}\sin\varphi\omega_c-5.08\times10^{25}\cos\varphi\end{array}\right)}{-\left(4\times10^{6}\omega_c^{6}+1.87\times10^{15}\omega_c^{4}-1.61\times10^{21}\omega_c^{2}+3.48\times10^{26}\right)} \tag{4.117}$$

Replacing specified frequency domain measures ω_c=2π.50=100π and φ=90° in above equations, we get K_{p2}=0.44 and K_{i2}=57.08. The frequency response of compensated outer

voltage control loop with neglected current loop dynamics is shown in Fig. 4.81. The specified phase margin, gain crossover frequency is achieved and gain in low-frequency region has been increased having -20 dB/decade slope.

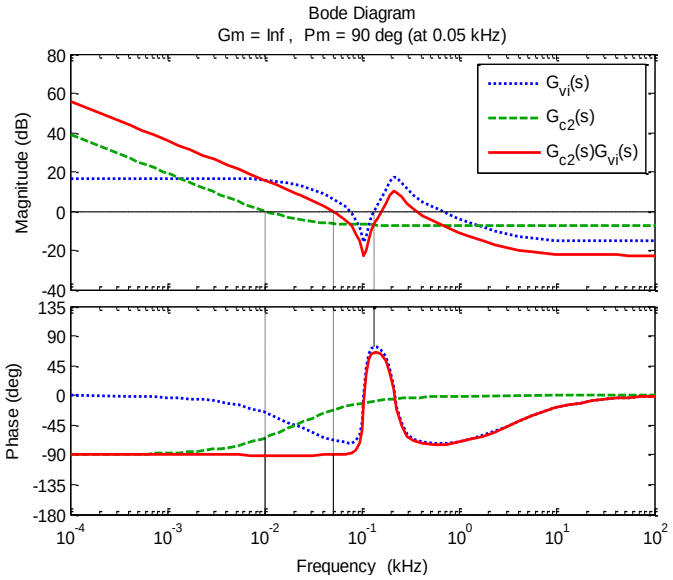


Fig. 4.81. Frequency response of compensated voltage control loop of Cuk converter without inner current loop dynamics

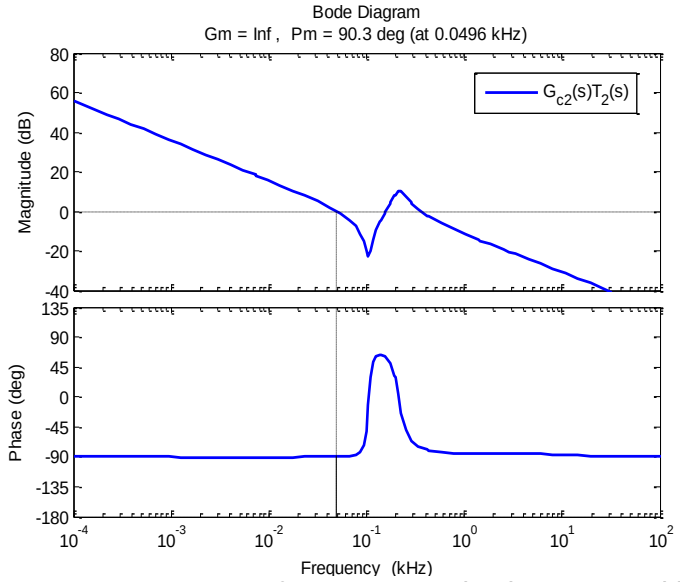


Fig. 4.82. Frequency response of compensated voltage control loop of Cuk converter with inner current loop dynamics and PI controller $G_{c2}(s)$

These PI controller value K_{p2}=0.44 and K_{i2}=57.08 are used with $T_2(s)$, the loop transfer function of uncompensated voltage control loop with current loop dynamics. The frequency response of the compensated voltage control loop in this case is shown in Fig. 4.82. As shown in figure, the phase margin is 90.3° and gain crossover frequency is 49.6 Hz, which are almost same as desired (phase margin 90° and gain crossover frequency is 50 Hz). The negligence of inner current control loop dynamics does not much affect the voltage controller design. Therefore, these PI parameters can be used for the control of practical Cuk converter without much degrading the desired performance measures.

4.3.4.3 Results and discussion

This section aims to observe the performance of two-loop PI control of Cuk converter under different operating conditions. The simulation results are obtained using MATLAB/Simulink software. The experimental results are also obtained to verify the simulation results. The voltage loop and current loop PI controllers designed in (4.107) and (4.114) are implemented on Cuk converter prototype using dSPACE system. The inductor current and output voltage are sensed using current and voltage sensors and fed to dSPACE controller via ADC channels. Detailed discussion on experimental work is given in Appendix *B*.

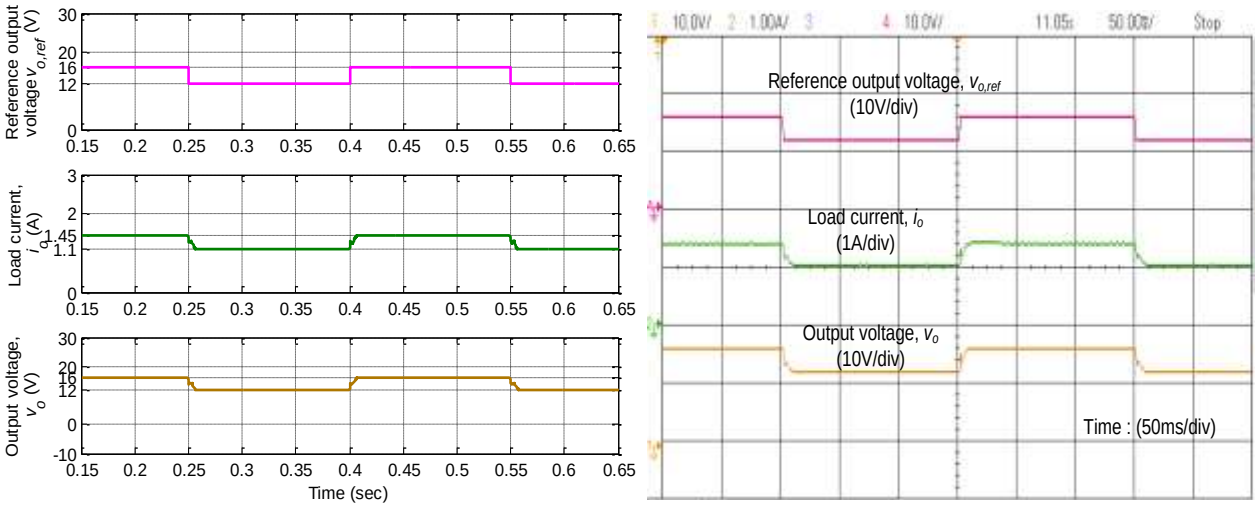
(a) Variation in reference output voltage

In this case, the reference output voltage is varied while keeping the input voltage (V_g) and load resistance (R) constant to 20 V and 11 Ω, respectively. For reference voltage variation from 16 V to 12 V and vice-versa, the simulation and experimental results are shown in Fig. 4.83(a). Similarly, for reference voltage variation from 16 V to 20 V and vice-versa, the corresponding simulation and experimental results are shown in Fig. 4.83 (b). It is observed that the output voltage smoothly settles to steady-state (16 V) within 10-15 ms without any oscillation and undershoot/overshoot. The load current is 1.09 A, 1.45 A and 1.81 A for desired output voltage 12 V, 16 V and 20 V, respectively. It can be observed that the simulation and experimental results are closely matched.

(b) Variation in input voltage

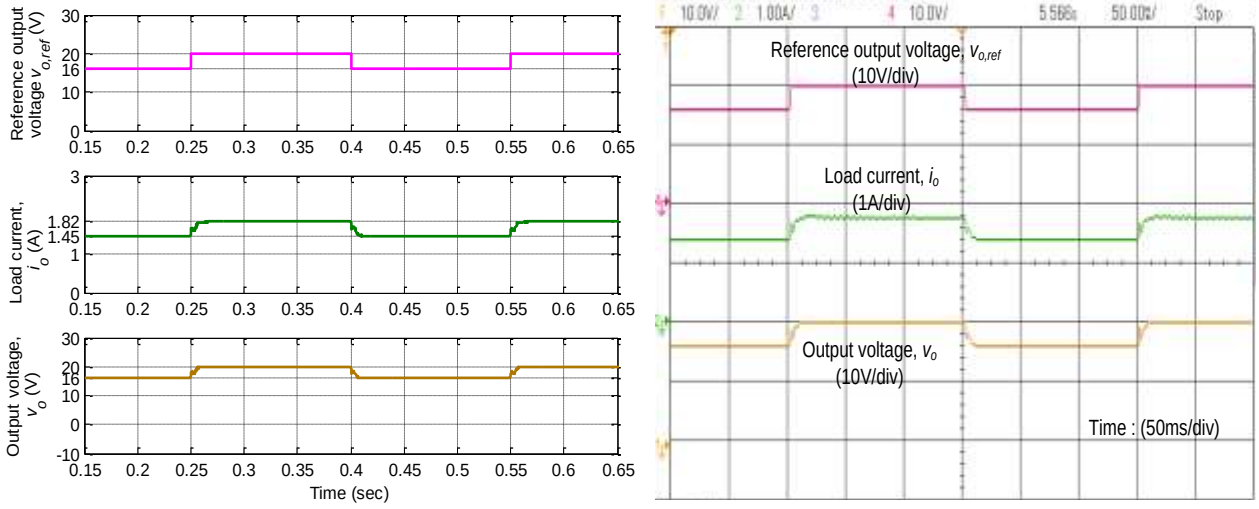
In this case, the variation in input voltage (V_g) is considered from minimum (20 V) to maximum (28 V) and vice-versa for two extreme load conditions R=11 Ω (*i.e.,* maximum load current, 1.45 A) and R=22 Ω (*i.e.,* minimum load current, 0.73 A). The desired output voltage is 16 V.

When at fixed load of 11 Ω, the input voltage is varied from 20 V to 28 V and vice-versa; the results are shown in Fig. 4.84 (a) and Fig. 4.84 (b), respectively. Similarly, when at fixed load of 22 Ω, the input voltage is varied from 20 V to 28 V and vice-versa; the results are shown in Fig. 4.85 (a) and Fig. 4.85 (b), respectively. These results indicate that the output voltage settles to steady-state back within 25-30 ms. The output voltage has overshoot of 1.6 V and undershoot of 3.6-4 V when the input voltage is increased from 20 V to 28 V. Similarly, the output voltage has undershoot of 1.6-2 V and overshoot of 3.6-4 V when the input voltage is decreased from 28 V to 20 V. The experimental results vary slightly from simulation results in transient condition. The reason is that the step change in input voltage was realized using a manual. Therefore, in this particular case, the initial part of transients in the experimental output voltage is ignored while comparing with the simulation results.



Simulation Experimental

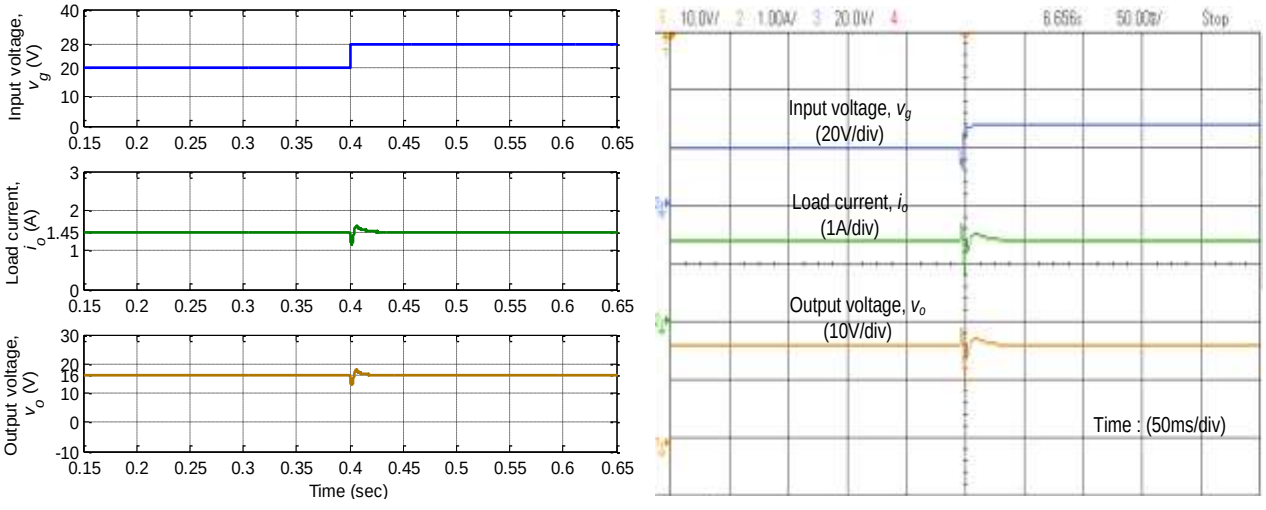
(a)



Simulation Experimental

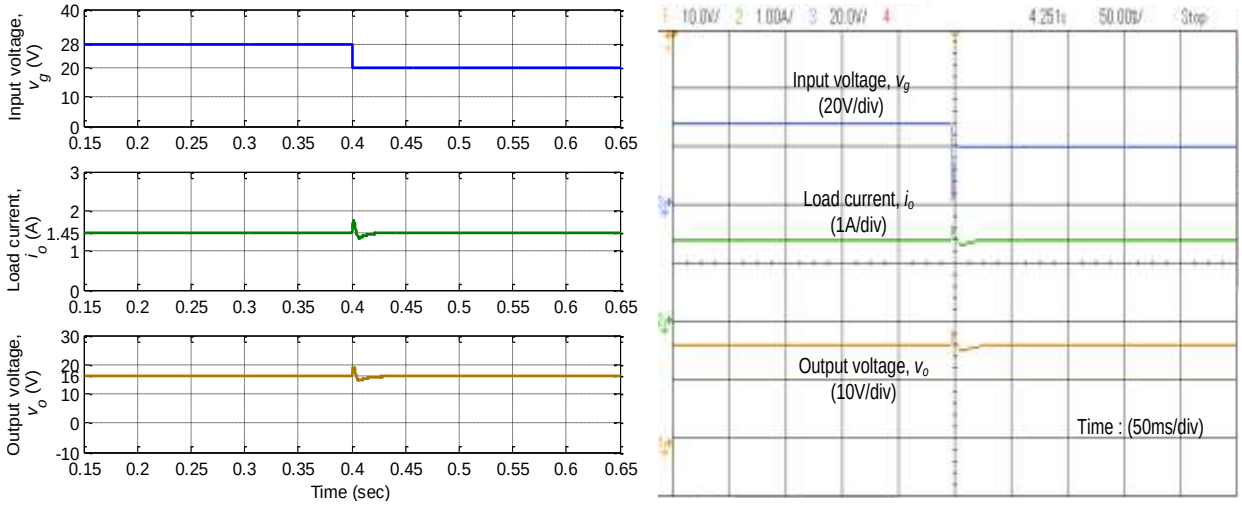
(b)

Fig. 4.83. Simulation and experimental results for reference output voltage variation from (a) 16 V to 12 V and vice-versa (b) 16 V to 20 V and vice-versa



Simulation Experimental

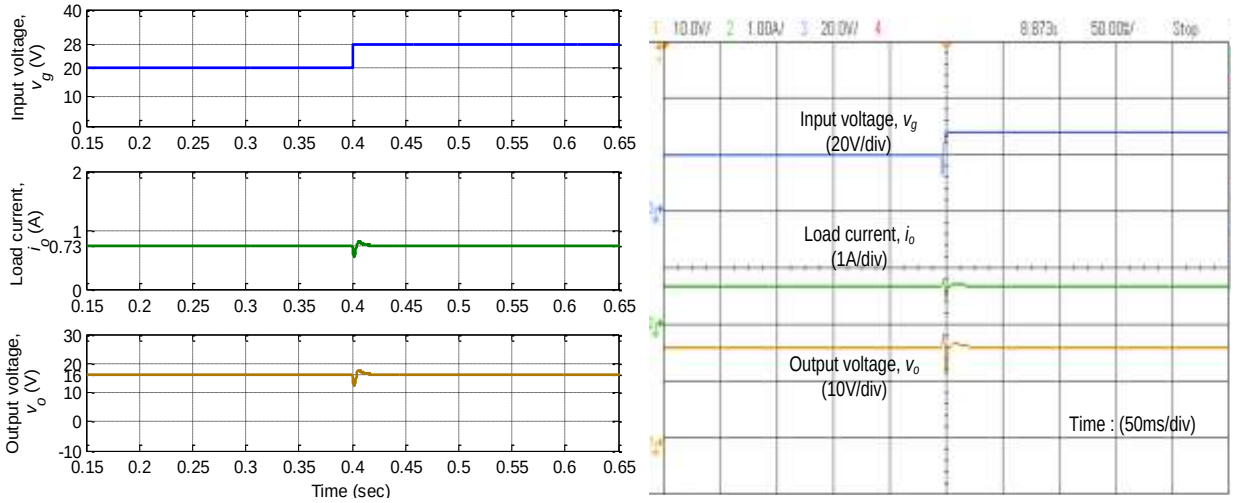
(a)



Simulation Experimental

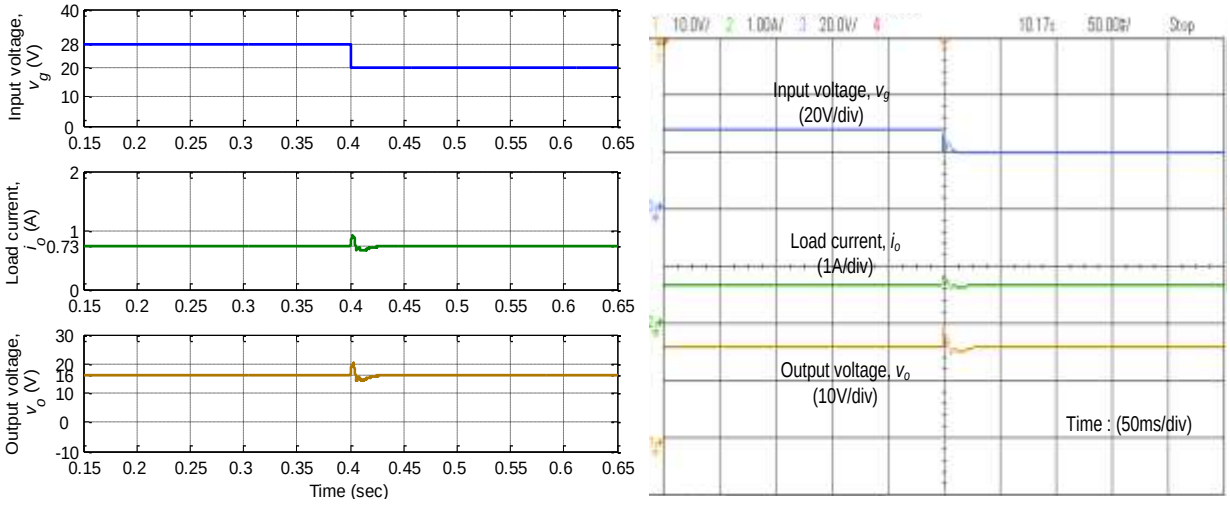
(b)

Fig. 4.84. Simulation and experimental results with R=11 Ω for input voltage variation from (a) 20 V to 28 V (b) 28 V to 20 V



Simulation Experimental

(a)



Simulation Experimental

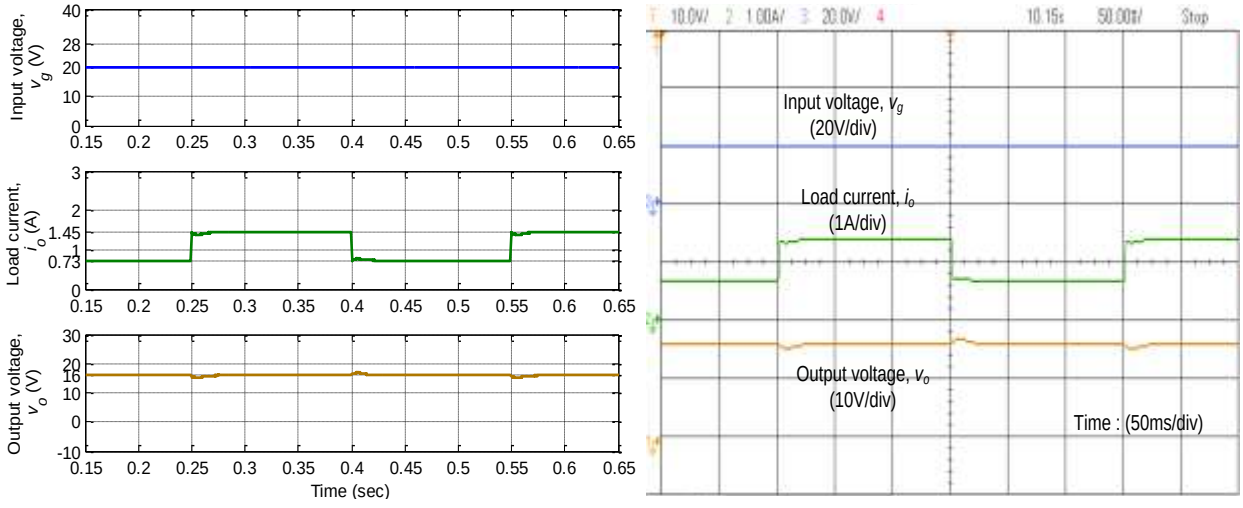
(b)

Fig. 4.85. Simulation and experimental results with R=22 Ω for input voltage variation from (a) 20 V to 28 V (b) 28 V to 20 V

(c) Variation in load resistance or load current

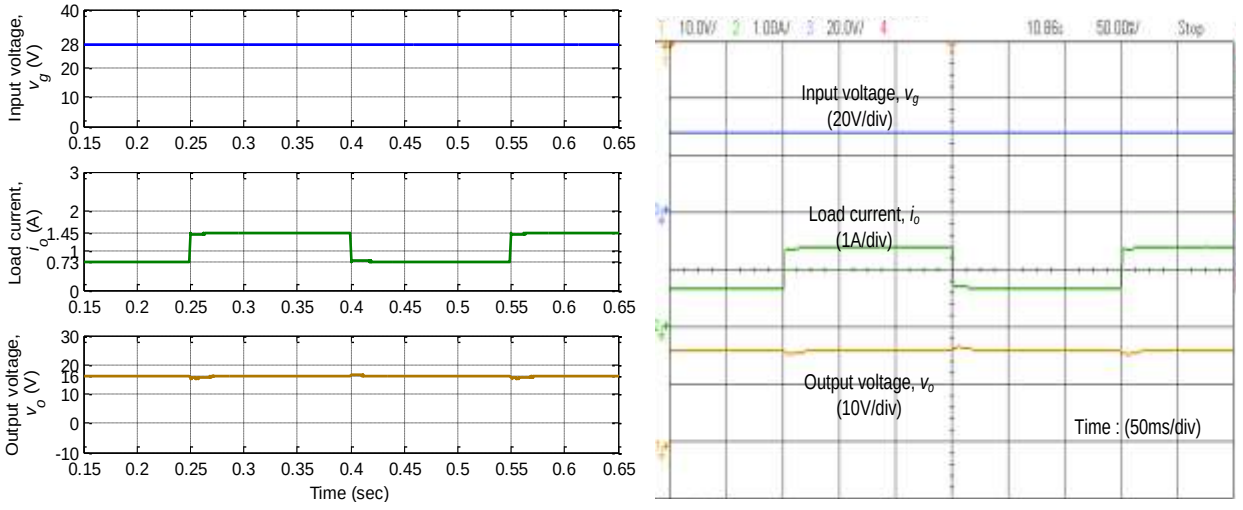
In this case, the load resistance (R) is varied from 22 Ω (*i.e.,* minimum load current, 0.73 A) to 11 Ω (*i.e.,* maximum load current, 1.45 A) and vice-versa for two extreme input voltages V_g=20 V (minimum) and V_g=28 V (maximum). The desired output voltage is 16 V.

At fixed input voltage 20 V, the simulation and experimental results are shown in Fig. 4.86(a) for step variation in load resistance from 22 Ω to 11 Ω and vice-versa. Similarly, for same load variation, but at constant input voltage 28 V; the results are shown in Fig. 4.86 (b). These results inform that the output voltage reaches steady-state very quickly within 20 ms. The output voltage has small undershoot of 0.8 V when the load is switched from 22 Ω to 11 Ω, whereas overshoot of 1 V when the load is switched from 11 Ω to 22 Ω. The experimental results validate the MATLAB simulation results.



Simulation Experimental

(a)



Simulation Experimental

(b)

Fig. 4.86. Simulation and experimental results for variation in load resistance from 22 Ω to 11 Ω and vice-versa at input voltage (a) V_g=20 V (b) V_g=28 V

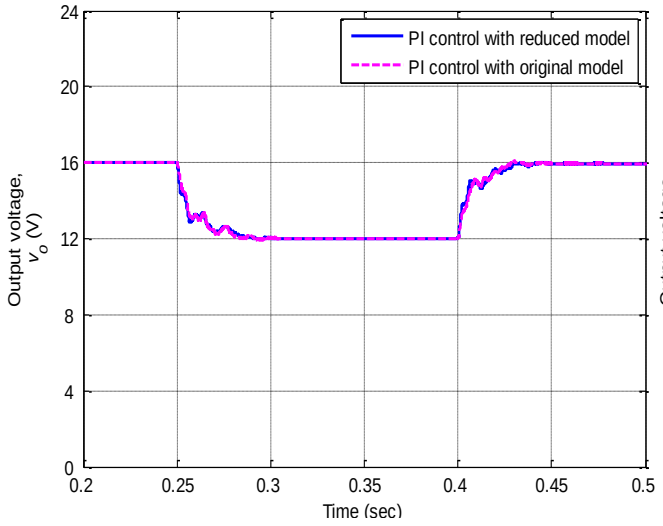
4.3.5 Performance comparison of different control techniques for Cuk converter

In the previous sections, the different controllers have been designed to regulate the output voltage of the Cuk converter under various working conditions. The simulation and experimental results have been discussed individually for each control technique. The purpose of this section is to compare the performance of these control techniques. For this purpose, the simulated output voltage for different control techniques has been compared under various conditions. In order to make the clarity in the figures, the two performance comparisons have been considered as follows:

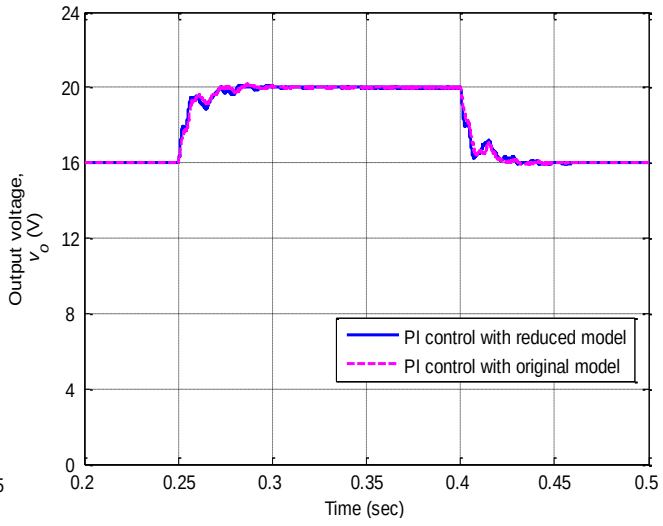
1. Performance comparison of reduced and original model based PI controllers for DC-DC Cuk converter
2. Performance comparison of PI, PI-lead and two-loop PI controllers for DC-DC Cuk converter

4.3.5.1 Performance comparison of reduced model and original model based PI controllers for DC-DC Cuk converter

In previous sections, it was discussed that Cuk converter is a fourth-order Cuk converter and therefore, it is possible to get its lower-order model using model-order reduction techniques. In section 4.3.2, a second-order model of Cuk converter was obtained using the truncation method and then a PI controller was designed based on the stability boundary locus method. In section 4.3.1, the PI controller was designed using its fourth-order model. Under different working conditions, the output voltage of the Cuk converter has been compared with both these PI controllers and is shown in Fig. 4.87. From these results, it can be observed that the performance of Cuk converter is almost similar using both the PI controllers. The PI controller with original model results in little faster settling time, whereas the PI controller with the reduced model gives slightly less overshoot. The reason is that the compensated Cuk converter has 93.6° phase margin at 63.9 Hz gain crossover frequency with original model based PI controller, whereas 103° phase margin at 20.7 Hz gain crossover frequency with original model based PI controller. The high gain crossover frequency results in faster settling time and high phase margin results in lower overshoot.

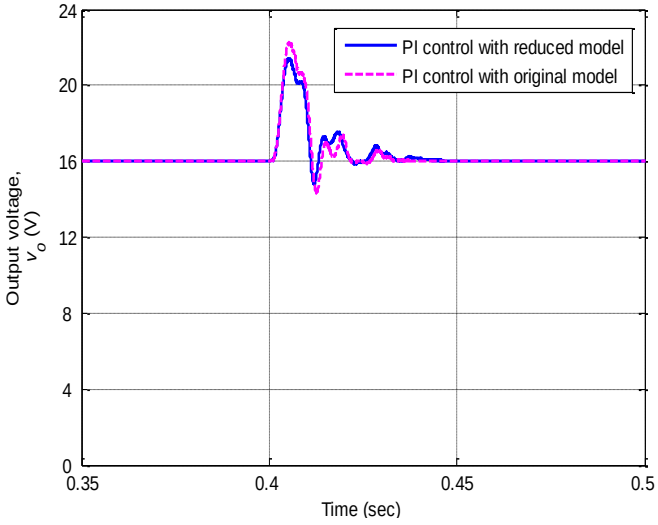


V_{ref}=16 V to 12 V and vice-versa

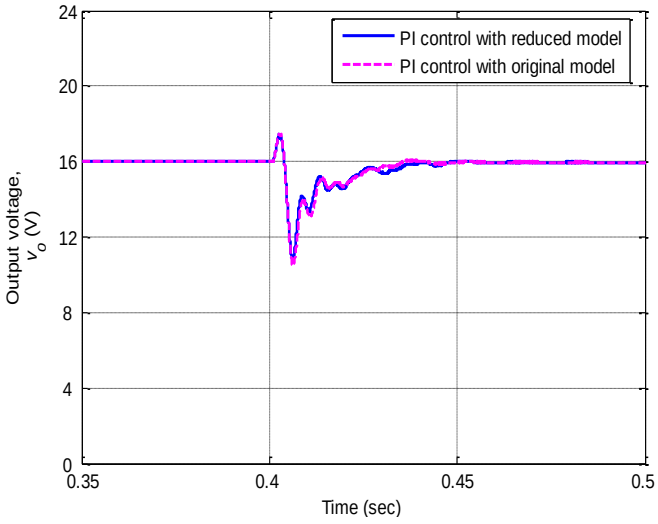


V_{ref}=16 V to 20 V and vice-versa

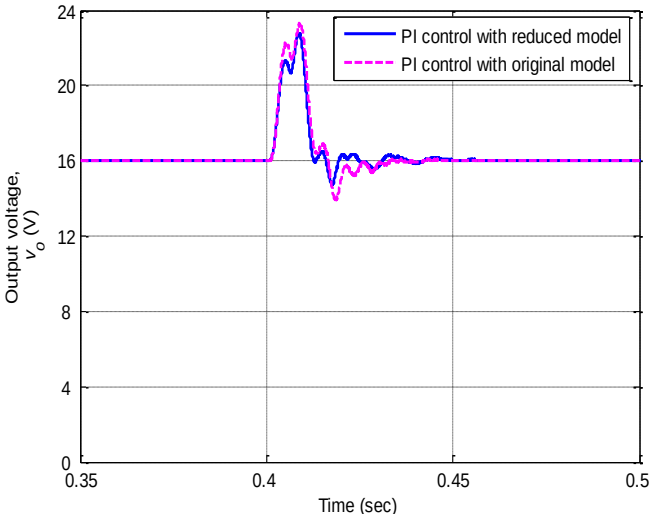
(a)



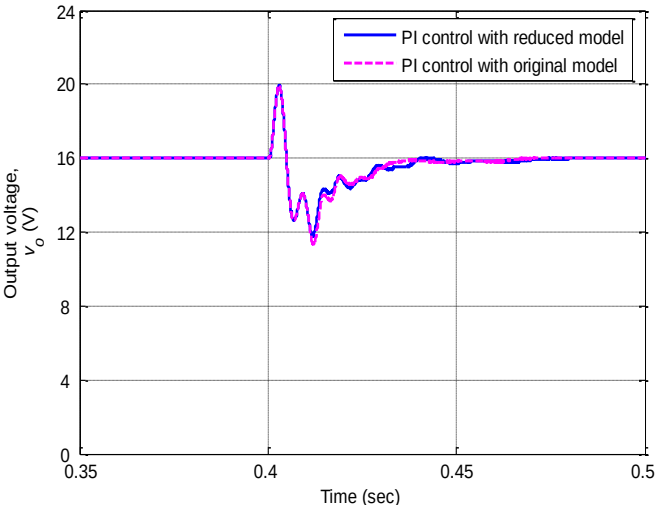
V_g=20 V to 28 V with R=11 Ω



V_g=28 V to 20 V with R=11 Ω

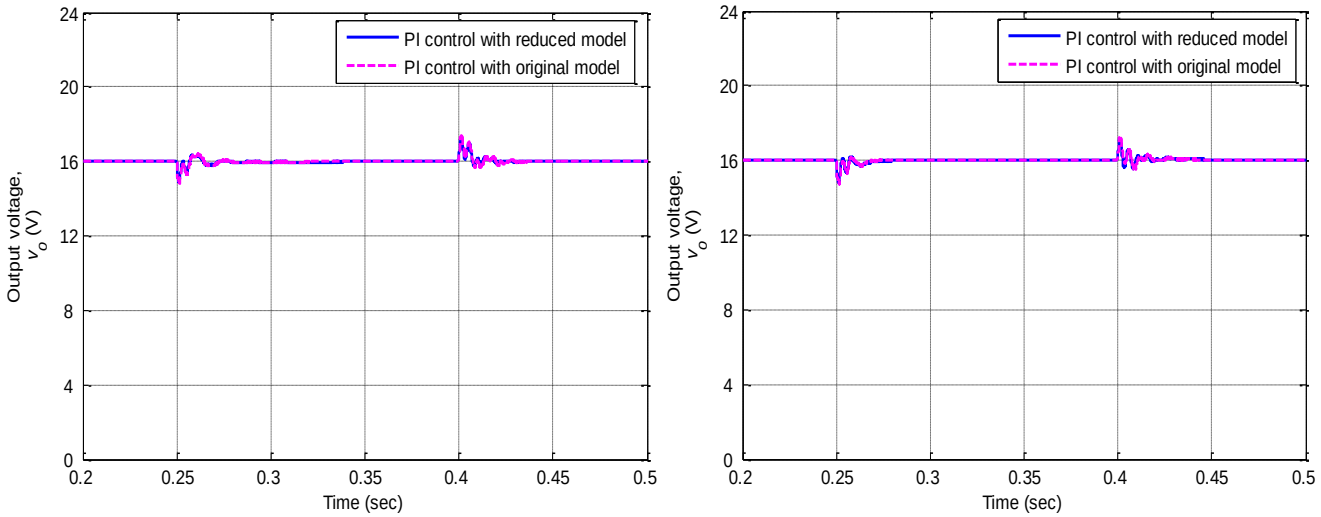


V_g=20 V to 28 V with R=22 Ω



V_g=28 V to 20 V with R=22 Ω

(b)



R=22 Ω to 11 Ω and vice-versa with V_g=20 V

R=22 Ω to 11 Ω and vice-versa with V_g=28 V

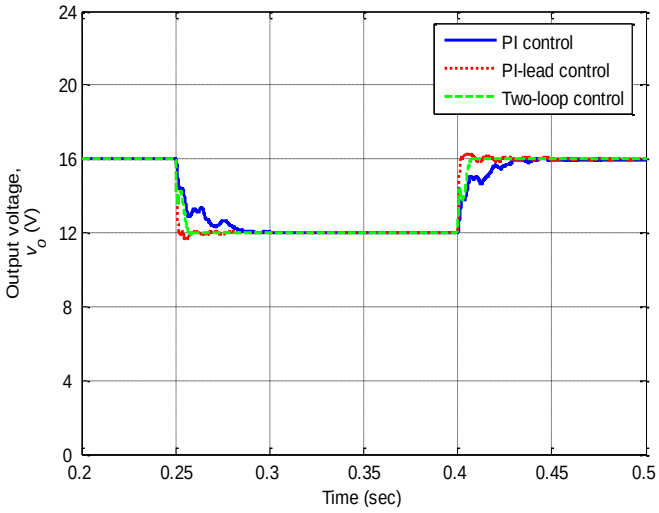
(c)

Fig. 4.87. Perfpremance comparison of reduced and original model based PI controllers for Cuk converter Output voltage for variation in (a) reference output voltage (b) input voltage (c) load current

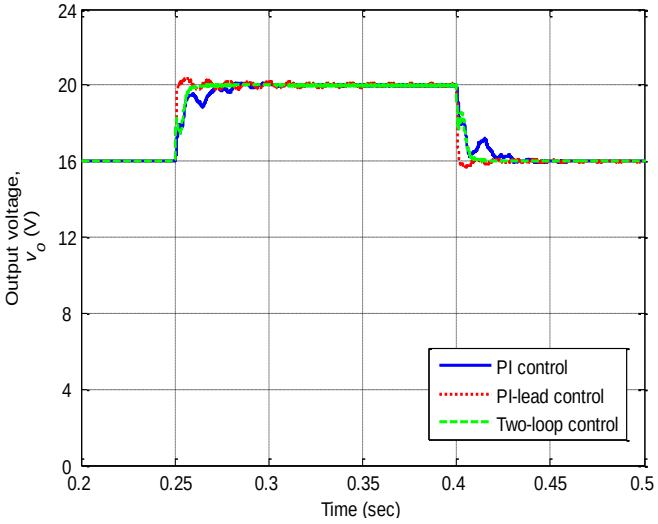
4.3.5.2 Performance comparison of PI, PI-lead and two-loop PI controllers for DC-DC Cuk converter

In order to study the performance comparison of PI, PI-lead and two-loop controllers, the output voltage of Cuk converter under various operating conditions is shown in Fig. 4.88. For variation in reference voltage, the settling time is 50-60 ms, 30-40 ms and 10-15 ms for PI control, PI-lead control and two-loop PI control, respectively. Under input voltage variation condition, the output voltage reaches to steady-state within 45-75 ms with PI controller, within 25-40 ms with PI-lead controller and within 25-30 ms with two-loop PI controller. For input voltage variation, the output voltage has maximum overshoot of 7 V and maximum undershoot of 6 V with PI controller; whereas maximum overshoot of 4 V and maximum undershoot of 2.2 V with PI-lead controller and, maximum overshoot and undershoot of 4 V with two-loop PI controller. For load resistance variation, the output voltage settles to steady-state within 40-50 ms, 30 ms and 20 ms with PI controller, PI-lead controller and two-loop PI controller, respectively. The output voltage has maximum undershoot of 1.2 V and maximum overshoot of 1.6 V with PI controller; whereas maximum undershoot and overshoot of 0.4 V with PI-lead controller and maximum undershoot and overshoot of 1 V with two-loop PI controller.

From these results, it is observed that PI controller regulates the output voltage under various conditions, but on the cost of larger overshoot/undershoot, oscillations and more settling time. On the other hand, PI-lead controller results in better dynamic and steady-state performance, but introduces the high frequency ripple in DC output voltage when designed at high gain crossover frequency. However, the two-loop PI controller gives satisfactory dynamic and steady-state performance, which is better in comparison to PI and PI-lead controller.

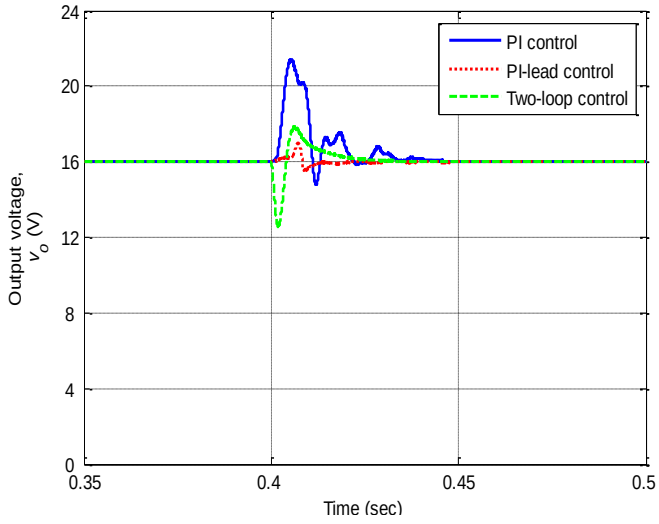


V_{ref}=16 V to 12 V and vice-versa

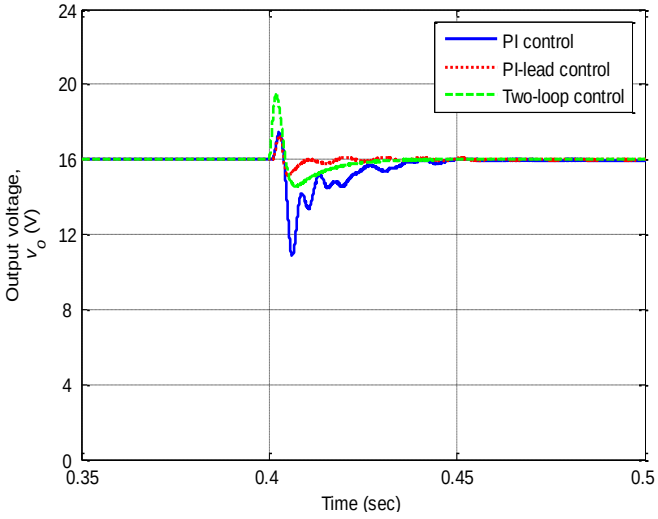


V_{ref}=16 V to 20 V and vice-versa

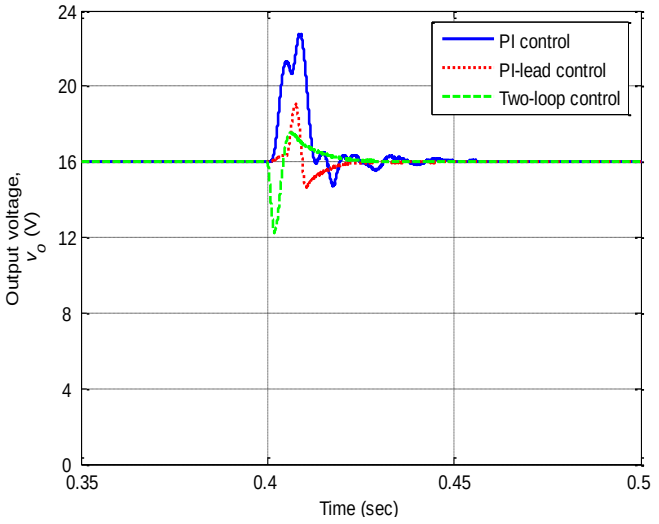
(a)



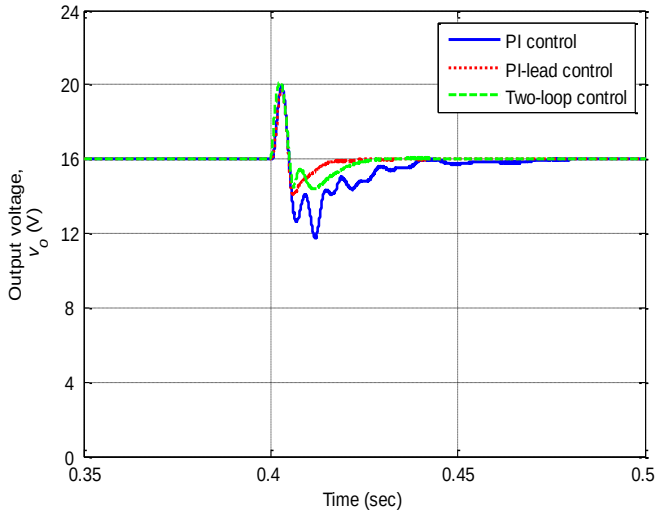
V_g=20 V to 28 V with R=11 Ω



V_g=28 V to 20 V with R=11 Ω

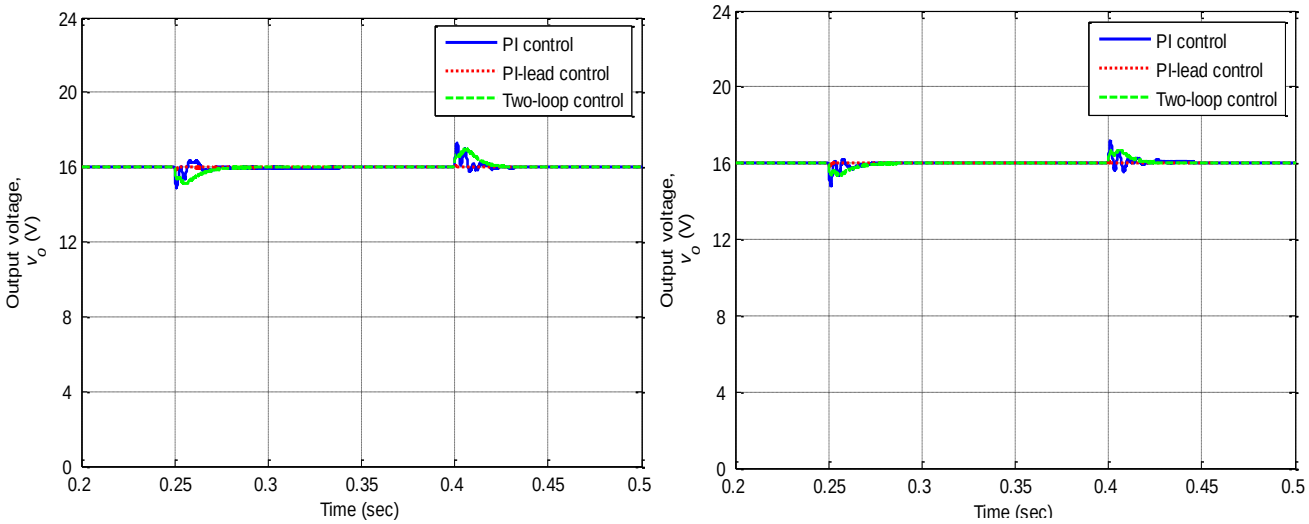


V_g=20 V to 28 V with R=22 Ω



V_g=28 V to 20 V with R=22 Ω

(b)



R=22 Ω to 11 Ω and vice-versa with V_g=20 V R=22 Ω to 11 Ω and vice-versa with V_g=28 V

(c)

Fig. 4.88. Performance comparison of PI, PI-lead and two-loop PI controllers for Cuk converter Output voltage for variation in (a) reference output voltage (b) input voltage (c) load current

4.4 Conclusion

In this chapter, the different control techniques were discussed to regulate the output voltage of non-ideal DC-DC buck and Cuk converters. The improved transfer functions (obtained in the previous chapter) were used for the controller design. First, a PI controller was designed using the stability boundary locus approach. This approach tunes the PI controller parameters based on the desired phase margin. The PI controller was designed for buck and Cuk converter. The experimental results show that the compensated system regulates the output voltage, but with larger overshoots and setting time. With the help of experimental results, it was found that the PI controller designed based on the reduced-order model of the Cuk converter also shows the almost similar performance. Then, a PI-lead controller was designed to improve the performance. An algorithm for tuning the parameters of the PI-lead controller was proposed, which gives the desired phase margin and gain crossover frequency exactly. The PI-lead controller improves the settling time and overshoots. However, for the higher gain crossover frequency, PI-lead controller introduces the noise in the output voltage as observed from the experimental results. In order to improve the performance of the converters further, a two-loop PI controller was discussed. This scheme consists of two PI controllers; outer voltage PI controller and inner current PI controller. An algorithm has been proposed to tune the parameters of these PI controllers based on desired phase margin and gain crossover frequency. This scheme has been implemented for buck and Cuk converters. The experimental results show that the settling time and overshoots has been improved significantly under different working conditions.

[In this chapter, sliding mode control technique is discussed to regulate the output voltage of the DC-DC Cuk converter. The MATLAB simulation and experimental results are provided to verify the performance of the designed sliding mode controller.]

5.1 Introduction

In the previous chapter, various classical control techniques were designed for DC-DC buck and Cuk converters. These techniques were designed based on transfer functions of the DC-DC converter. The DC-DC converters are non-linear systems. Therefore, from an averaged model, a small-signal model was derived by introducing perturbations and then linearizing the converter dynamics around a DC operating point. Finally, this small-signal model was used to derive the different transfer function models of the DC-DC converters. Therefore, the controller design based on these transfer functions may not be suitable to achieve better output voltage regulation, dynamic and static performance, and stability in the presence of parametric uncertainty or large variations in input and/or load conditions. Moreover, as the order of DC-DC converters increases, the design of high-performance controller becomes a difficult and challenging task.

On the other hand, sliding mode control is a well-known non-linear control technique. This technique has been used extensively for the control of variable structure systems (VSS) [184]–[186]. The DC-DC converters are variable structure systems as they have more than one circuit structures depending upon the position of the switch. Therefore, the DC-DC converters are good candidate for the application of sliding mode control theory [187]. The sliding mode control technique has been used for the different DC-DC converters [79], [91], [97], [149], [188]–[191]. In sliding mode control, a switching surface is defined as a function of the state variables. The control signal is driven in such a way that the instantaneous values of the state variables forces the system trajectory to stay on the selected sliding surface. The sliding mode control technique offers many advantages such as: stable output voltage in the presence of large input voltage or load disturbances, good dynamic and steady-state response, robustness to parameter variations. The sliding mode control is very useful especially for the output voltage regulation of higher-order DC-DC converters such as Cuk, Zeta, SEPIC converters, *etc*.

In this chapter, the research work done in [192] is extended. In this original paper [192], a sliding mode control is designed for the DC-DC Cuk converter. The superiority of the sliding mode control over the other control techniques has been reported. However, the various transfer functions obtained in this paper are incorrect. Some of these transfer functions have been corrected in [193], [194]. However, in this chapter, the entire analysis is revised and all the derivations are carried out correctly. Further, a simplified approach based

on stability boundary locus is developed to design the parameters of the controller parameter. Moreover, despite doing good research work on sliding mode control of DC-DC Cuk converter, the experimental validation of this control methodology has not been performed in [192]. In [193], the author has given only steady-state experimental results under few operating conditions. The steady-state and transient performance have not been reported under all operating condition. However, in this chapter, the steady-state and transient performance of the proposed control approach have been experimentally validated for DC-DC Cuk converter under various operating conditions using dSPACE DS1104 digital signal processor.

5.2 Cuk converter

The basic system configuration of DC-DC Cuk converter is shown in Fig. 5.1. It has two inductors L_1 and L_2, two capacitors C_1 and C_2, switch S_w, one diode D_d and load resistance R. The operating principle of the Cuk converter has been discussed in previous chapters and therefore, will not be discussed again here. In brief, this converter can transfer electrical energy from an input power source to output load at different output voltage levels. The output voltage (v_o) can be lesser, equal or greater than the input voltage with opposite polarity. The switch is operated with the duty cycle d at switching frequency f_s (or switching period T).

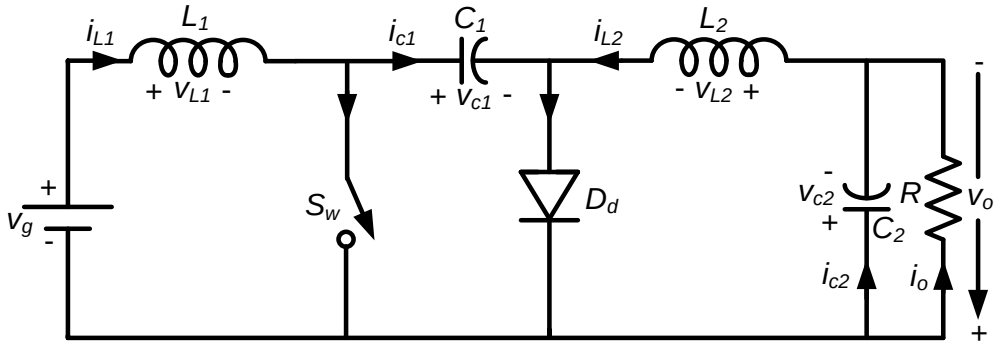


Fig. 5.1. Basic configuration of DC-DC Cuk converter

5.2.1 Dynamic equations of DC-DC Cuk converter

Considering the operation of the Cuk converter in continuous conduction mode (CCM), there are two switching states.

(a) Switch is on: In this state, the switch is on and the diode is reverse biased. The equivalent circuit is shown in Fig. 5.2(a). The dynamic equations of the Cuk converter can be written as:

$$
\begin{aligned}
v_{L1}(t) &= L_1 \frac{di_{L1}(t)}{dt} = v_g(t) \\
v_{L2}(t) &= L_2 \frac{di_{L2}(t)}{dt} = v_{c1}(t) - v_{c2}(t) \\
i_{c1}(t) &= C_1 \frac{dv_{c1}(t)}{dt} = -i_{L2}(t) \\
i_{c2}(t) &= C_2 \frac{dv_{c2}(t)}{dt} = i_{L2}(t) - \frac{v_{c2}(t)}{R} \\
v_o(t) &= v_{c2}(t)
\end{aligned}
\tag{5.1}
$$

(b) *Switch is off*: In this state, the switch is off and the diode is forward biased. The equivalent circuit is shown in Fig. 5.2(b). The dynamic equations of the Cuk converter can be written as:

$$
\begin{aligned}
v_{L1}(t) &= L_1 \frac{di_{L1}(t)}{dt} = v_g(t) - v_{c1}(t) \\
v_{L2}(t) &= L_2 \frac{di_{L2}(t)}{dt} = -v_{c2}(t) \\
i_{c1}(t) &= C_1 \frac{dv_{c1}(t)}{dt} = i_{L1}(t) \\
i_{c2}(t) &= C_2 \frac{dv_{c2}(t)}{dt} = i_{L2}(t) - \frac{v_{c2}(t)}{R} \\
v_o(t) &= v_{c2}(t)
\end{aligned}
\tag{5.2}
$$

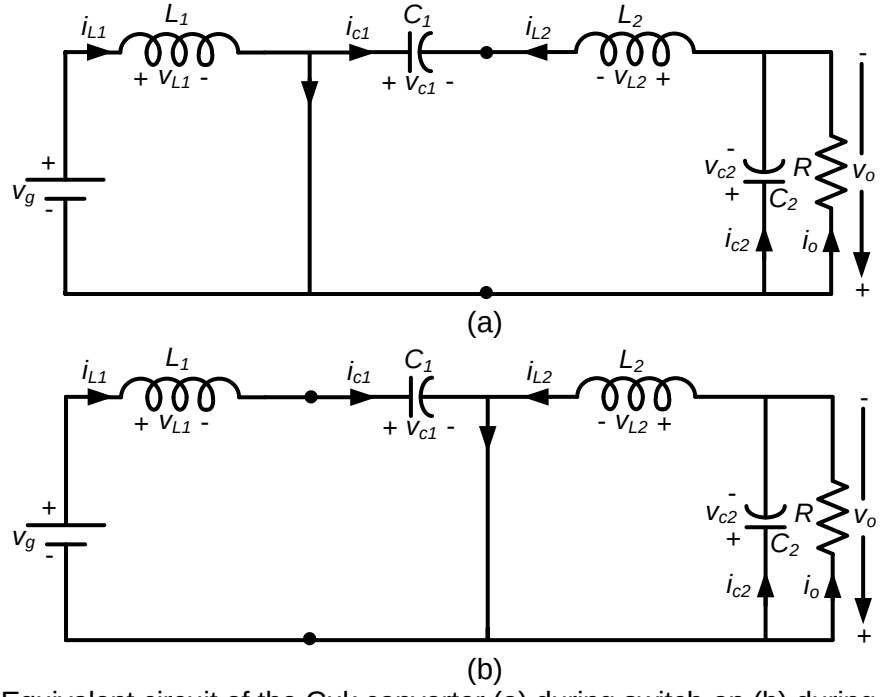


Fig. 5.2. Equivalent circuit of the Cuk converter (a) during switch-on (b) during switch-off

These dynamic equations during switch on and switch off can be combined as follows [192]:

$$\begin{aligned}
\frac{di_{L1}(t)}{dt} &= \frac{1}{L_1}\left[v_g(t) - \bar{u}v_{c1}(t)\right] = \frac{1}{L_1}\left[v_g(t) - v_{c1}(t) + uv_{c1}(t)\right] \\
\frac{di_{L2}(t)}{dt} &= \frac{1}{L_2}\left[uv_{c1}(t) - v_o(t)\right] = \frac{1}{L_2}\left[-v_o(t) + uv_{c1}(t)\right] \\
\frac{dv_{c1}(t)}{dt} &= \frac{1}{C_1}\left[\bar{u}i_{L1}(t) - ui_{L2}(t)\right] = \frac{1}{C_1}\left[i_{L1}(t) - u\left(i_{L1}(t) + i_{L2}(t)\right)\right] \\
\frac{dv_o(t)}{dt} &= \frac{1}{C_2}\left[i_{L2}(t) - \frac{v_o(t)}{R}\right]
\end{aligned} \tag{5.3}$$

Where, $\bar{u} = 1 - u$ and u is a binary switching signal which has value 1 if switch S_w is on and 0 if switch S_w is off.

5.2.2 State-space representation

The open-loop dynamics equations of DC-DC Cuk converter in (5.3) can be represented in state-space form as follows:

$$X'(t) = \frac{dX(t)}{dt} = A(t) + B(t)u(t) \tag{5.4}$$

Where,

$$X(t) = \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{c1}(t) \\ v_o(t) \end{bmatrix}, A = \begin{bmatrix} \frac{v_g(t) - v_{c1}(t)}{L_1} \\ \frac{-v_o(t)}{L_2} \\ \frac{i_{L1}(t)}{C_1} \\ \frac{i_{L2}(t)}{C_2} - \frac{v_o(t)}{RC_2} \end{bmatrix}, B = \begin{bmatrix} \frac{v_{c1}(t)}{L_1} \\ \frac{v_{c1}(t)}{L_2} \\ \frac{-i_{L1}(t) - i_{L2}(t)}{C_1} \\ 0 \end{bmatrix}, u(t) = \begin{cases} 1, & \text{for switch-on} \\ 0, & \text{for switch-off} \end{cases}$$

The inductor currents i_{L1}, i_{L2} and capacitor voltage v_{c1}, v_{c2} (=v_o) are selected as state variables. Here onward, the time t in brackets will be dropped for better appearance of the expressions.

5.3 Design of sliding mode control for Cuk converter

The block diagram of the proposed sliding mode control scheme is shown in Fig. 5.3. This control scheme involves two control loops: a) outer voltage control loop and inner current control loop [192]. The outer voltage control loop employs a PI controller and inner current loop controller employs a sliding mode controller. The primary inductor current (i_{L1}) and output voltage (v_o) are taken as controlled state variables. These two variables are sensed and feedback to regulate the output voltage of Cuk converter.

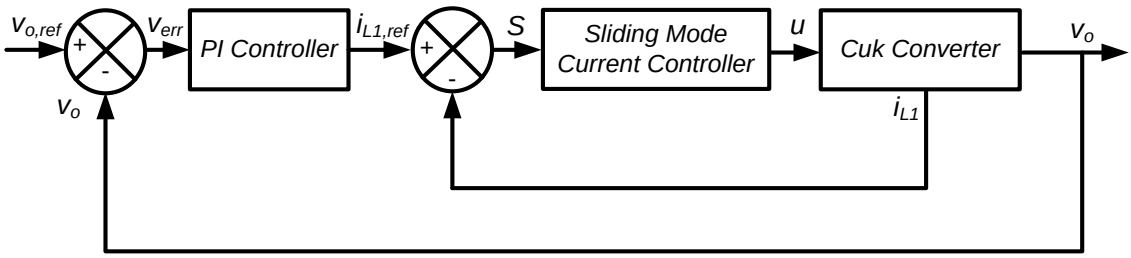


Fig. 5.3. Block diagram for sliding mode control of Cuk converter

a) Outer voltage loop controller: The function of the outer voltage loop is to eliminate the steady-state error in output voltage. For this purpose, a PI controller is used in the outer voltage control loop. The output of this PI controller is used as reference primary inductor current ($i_{L1,ref}$) for the inner sliding mode current control loop. This reference current $i_{L1,ref}$ is given as [192]:

$$i_{L1,ref}(t) = K_p e(t) + K_i \int e(t)dt \tag{5.5}$$

Where, the output voltage error $e(t) = v_{o,ref}(t) - v_o(t)$ is the difference between the instantaneous output voltage reference ($v_{o,ref}$) and actual output voltage (v_o). The coefficients K_p and K_i are the parameters of PI controller, which are tuned based on sliding surface dynamics of sliding mode control. The determination of these parameters will be discussed later in this chapter.

b) Inner current loop controller: In this loop, the actual inductor current (i_{L1}) is compared with the reference inductor current ($i_{L1,ref}$). Based on the chosen sliding surface, the switching signal is generated for the semiconductor devices.

5.3.1 Sliding surface

The ultimate goal of the sliding mode controller is to regulate the DC output voltage of Cuk converter. However, the sliding surface can be designed by selecting the appropriate combination of converter's state variables. The number of state variables should be as minimum as possible to avoid the large number of tuning parameters.

For the control scheme under consideration, the sliding surface is chosen as the difference between reference primary inductor current and actual primary inductor current as [192]:

$$S = i_{L1,ref} - i_{L1} \tag{5.6}$$

The switching signal u is defined as $u = \dfrac{1 + sign(s)}{2}$. It means

$$u = \begin{cases} 1, & for\ S \geq 0\ \ or\ \ i_{L1,ref} \geq i_{L1} \\ 0, & for\ S < 0\ \ or\ \ i_{L1,ref} < i_{L1} \end{cases} \tag{5.7}$$

The reference inductor current $i_{L1,ref}$ is generated by the outer voltage loop control and has been given in (5.5).

This sliding surface can be written in terms of the state vector *X* (defined in (5.4)) as below:

$$S = GX + \psi \tag{5.8}$$

Where, $G = \begin{bmatrix} -1 & 0 & 0 & 0 \end{bmatrix}, \psi = i_{L1,ref}$

5.3.2 Equivalent control

The analysis of closed-loop sliding mode control system is carried out using the concept of equivalent control. The equivalent control converts the original discontinuous system into a continuous ideal sliding mode system [187]. The continuous equivalent control signal (u_{eq}) is derived by satisfying two following conditions on the sliding surface *S*.

$$S = 0 \tag{5.9}$$

$$\frac{dS}{dt} = 0 \tag{5.10}$$

In sliding mode control literature, it is also called invariance conditions.

From first condition, we get

$$S = i_{L1,ref} - i_{L1} = 0 \Rightarrow \quad i_{L1} = i_{L1,ref} \tag{5.11}$$

For the second condition, we substitute *S* from (5.8) and get

$$\frac{dS}{dt} = GX' + \psi' = 0 \tag{5.12}$$

Substituting $X' = A + Bu$ from (5.4) into (5.12),

$$G\left(A + Bu_{eq}\right) + \psi' = 0 \Rightarrow \qquad u_{eq} = -\left(GB\right)^{-1}\left(GA + \psi'\right) \tag{5.13}$$

Substituting corresponding values of vectors *A* and *B* from (5.4) and *G* and *ψ* from (5.8) into (5.13), we have

$$u_{eq} = -\left(-\frac{L_1}{v_{c1}}\right)\left(-\frac{v_g - v_{c1}}{L_1} + i'_{L1,ref}\right) \Rightarrow \; u_{eq} = \frac{-v_g + v_{c1} + L_1 i'_{L1,ref}}{v_{c1}} \tag{5.14}$$

u_{eq} is a continuous switching signal which takes value between 0 and 1, which will provide the ideal sliding motion on the sliding surface.

5.3.3 Hitting and existence conditions

In order to obtain the desired dynamic and steady-state performance, the closed-loop system must enter into SM operation. For the closed-loop system to be in SM operation, three necessary conditions must be satisfied [187]. These conditions are hitting condition, existence condition and stability condition. In this subsection, first two conditions are discussed. The stability conditions will be discussed in the next section.

Hitting condition:

The hitting condition ensures that the system state trajectory will always be directed towards the sliding surface irrespective of the initial conditions. The hitting condition for the Cuk

converter is satisfied by choosing the sliding surface such that the switching takes place as below:

$$u = \begin{cases} 1, & for\ S > 0 \\ 0, & for\ S < 0 \end{cases} \tag{5.15}$$

This condition has already been satisfied by defining the appropriate switching signal in (5.7).

Existence condition:

The existence condition guarantees that the system state trajectory in the vicinity of sliding surface will always be directed towards the sliding surface. To fulfil the existence condition following condition must be satisfied.

$$\lim_{S\to 0} SS' < 0 \Rightarrow \begin{cases} S' < 0, & for\ S > 0 \\ S' > 0, & for\ S < 0 \end{cases} \tag{5.16}$$

Differentiating (5.6) with respect to '*t*', we get

$$S' = i'_{L1,ref} - i'_{L1} \tag{5.17}$$

Substituting values from (5.3)

$$S' = i'_{L1,ref} - \frac{v_g - v_{c1} + uv_{c1}}{L_1} = \frac{L_1 i'_{L1,ref} - v_g + v_{c1} - uv_{c1}}{L_1} \tag{5.18}$$

Case 1: $S > 0, S' < 0$

From hitting conditions, for $S > 0$, u=1; Therefore, substituting in (5.18), we get

$$\begin{aligned} & S' = \frac{L_1 i'_{L1,ref} - v_g}{L_1} < 0 \\ \Rightarrow \quad & L_1 i'_{L1,ref} - v_g < 0 \\ \Rightarrow \quad & 0 < v_g - L_1 i'_{L1,ref} \end{aligned} \tag{5.19}$$

Case 2: $S < 0, S' > 0$

From hitting conditions, for $S < 0$, u=0; Therefore, substituting in (5.18), we get

$$\begin{aligned} & S' = \frac{L_1 i'_{L1,ref} - v_g + v_{c1}}{L_1} > 0 \\ \Rightarrow \quad & L_1 i'_{L1,ref} + v_{c1} - v_g > 0 \\ \Rightarrow \quad & v_g - L_1 i'_{L1,ref} < v_{c1} \end{aligned} \tag{5.20}$$

Combining (5.19) and (5.20) gives

$$0 < v_g - L_1 i'_{L1,ref} < v_{c1} \tag{5.21}$$

This is the existence condition for the defined sliding surface of DC-DC Cuk converter [192]. This condition will always be satisfied because v_{c1} (=v_g+v_o) is always greater than v_g for Cuk converter.

5.4 Stability analysis of closed-loop dynamics

The stability conditions for the closed-loop SM control of the Cuk converter can be derived by finding the ideal sliding dynamics first and then carrying out the small-signal analysis around its equilibrium point [192].

5.4.1 Ideal sliding dynamics

The ideal sliding mode dynamics is obtained by the replacement of the discontinuous switching signal u by continuous switching signal u_{eq} (obtained from equivalent control method) in the original dynamics of the Cuk converter.

Therefore, replacing $u = u_{eq}$ in (5.4), we get

$$\begin{bmatrix} i'_{L1} \\ i'_{L2} \\ v'_{c1} \\ v'_o \end{bmatrix} = \begin{bmatrix} \frac{v_g - v_{c1}}{L_1} \\ \frac{-v_o}{L_2} \\ \frac{i_{L1}}{C_1} \\ \frac{i_{L2}}{C_2} - \frac{v_o}{RC_2} \end{bmatrix} + \begin{bmatrix} \frac{v_{c1}}{L_1} \\ \frac{v_{c1}}{L_2} \\ \frac{-i_{L1} - i_{L2}}{C_1} \\ 0 \end{bmatrix} u_{eq} \tag{5.22}$$

Substituting value of u_{eq} from (5.14) into (5.22) and simplifying, we have

$$\frac{d}{dt}\begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{c1} \\ v_o \end{bmatrix} = \begin{bmatrix} i'_{L1,ref} \\ \frac{1}{L_2}\left(-v_o - v_g + v_{c1} + L_1 i'_{L1,ref}\right) \\ \frac{i_{L1}}{C_1} + \left(\frac{-i_{L1} - i_{L2}}{C_1}\right)\left(\frac{-v_g + v_{c1} + L_1 i'_{L1,ref}}{v_{c1}}\right) \\ \frac{i_{L2}}{C_2} - \frac{v_o}{RC_2} \end{bmatrix} \tag{5.23}$$

This is the ideal sliding mode dynamics of the closed-loop DC-DC Cuk converter.

5.4.2 Equilibrium point

The equilibrium point on the sliding surface is a stable steady-state point where the ideal sliding dynamics are finally settled. It can be obtained by equating (5.23) to zero *i.e.,*

$$\frac{d}{dt}\begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{c1} \\ v_o \end{bmatrix} = 0 \tag{5.24}$$

On simplification, it gives

$$V_{c1} = V_o + V_g, I_{L1} = I_{L1,ref} = \frac{V_o^2}{RV_g}, I_{L2} = \frac{V_o}{R} \tag{5.25}$$

Where, V_g, R, I_{L1}, I_{L2}, V_{c1} and V_o are steady-state values of the input voltage, load resistance, inductor currents, capacitor voltage and the output voltage at the equilibrium point.

5.4.3 Small-signal analysis

The ideal sliding dynamics in (5.23) is non-linear. It is linearized by introducing the perturbation terms around the equilibrium point obtained in (5.25). Before proceeding to linearization, the ideal sliding dynamics in (5.23) is simplified and the necessary expressions are obtained.

On simplifying (5.23), we get

$$i'_{L1} = i'_{L1,ref} \Rightarrow i_{L1} = i_{L1,ref} \tag{5.26}$$

$$i'_{L2} = \frac{1}{L_2}\left(-v_o - v_g + v_{c1} + L_1 i'_{L1,ref}\right) \Rightarrow v_{c1} = v_o + v_g + L_2 i'_{L2} - L_1 i'_{L1,ref} \tag{5.27}$$

$$\begin{aligned} v'_{c1} &= \frac{i_{L1}}{C_1} + \frac{-i_{L1} - i_{L2}}{C_1}\left(\frac{-v_g + v_{c1} + L_1 i'_{L1,ref}}{v_{c1}}\right) \\ \Rightarrow \quad C_1 v_{c1} v'_{c1} &= v_{c1} i_{L1} - \left(i_{L1} + i_{L2}\right)\left(-v_g + v_{c1} + L_1 i'_{L1,ref}\right) \end{aligned} \tag{5.28}$$

$$v'_o = \frac{i_{L2}}{C_2} - \frac{v_o}{RC_2} \Rightarrow i_{L2} = \frac{v_o}{R} + C_2 v'_o \tag{5.29}$$

Substituting $i_{L1}=i_{L1,ref}$ into (5.28) and simplifying for $i_{L1,ref}$, we get

$$\begin{aligned} C_1 v_{c1} v'_{c1} &= \left(v_g - L_1 i'_{L1,ref}\right) i_{L1,ref} - i_{L2}\left(-v_g + v_{c1} + L_1 i'_{L1,ref}\right) \\ \Rightarrow \quad i_{L1,ref} &= \frac{i_{L2}\left(-v_g + v_{c1} + L_1 i'_{L1,ref}\right) + C_1 v_{c1} v'_{c1}}{\left(v_g - L_1 i'_{L1,ref}\right)} \end{aligned} \tag{5.30}$$

Differentiating (5.30) with respect to time 't' [192]

$$i'_{L1,ref} = \frac{\left(v_g - L_1 i'_{L1,ref}\right).\frac{d}{dt}\left\{i_{L2}\left(-v_g + v_{c1} + L_1 i'_{L1,ref}\right) + C_1 v_{c1} v'_{c1}\right\} - \left\{i_{L2}\left(-v_g + v_{c1} + L_1 i'_{L1,ref}\right) + C_1 v_{c1} v'_{c1}\right\}.\frac{d}{dt}\left(v_g - L_1 i'_{L1,ref}\right)}{\left(v_g - L_1 i'_{L1,ref}\right)^2} \tag{5.31}$$

$$\begin{aligned} \Rightarrow \left(v_g - L_1 i'_{L1,ref}\right)^2 i'_{L1,ref} &= \left(v_g - L_1 i'_{L1,ref}\right)\left\{i'_{L2}\left(-v_g + v_{c1} + L_1 i'_{L1,ref}\right) + i_{L2}\left(-v'_g + v'_{c1} + L_1 i''_{L1,ref}\right) + C_1 v_{c1} v''_{c1} + C_1 v'^2_{c1}\right\} \\ &\quad - \left\{i_{L2}\left(-v_g + v_{c1} + L_1 i'_{L1,ref}\right) + C_1 v_{c1} v'_{c1}\right\}\left(v'_g - L_1 i''_{L1,ref}\right) \end{aligned}$$

$$\begin{aligned} \Rightarrow \underbrace{\left(v_g - L_1 i'_{L1,ref}\right)^2 i'_{L1,ref}}_{I} &= \underbrace{\left(v_g - L_1 i'_{L1,ref}\right) i'_{L2}\left(-v_g + v_{c1} + L_1 i'_{L1,ref}\right)}_{II} + \underbrace{\left(v_g - L_1 i'_{L1,ref}\right) i_{L2}\left(-v'_g + v'_{c1} + L_1 i''_{L1,ref}\right)}_{III} \\ &\quad + \underbrace{\left(v_g - L_1 i'_{L1,ref}\right) C_1 v_{c1} v''_{c1}}_{IV} + \underbrace{\left(v_g - L_1 i'_{L1,ref}\right) C_1 v'^2_{c1}}_{V} + \underbrace{\left(-v'_g + L_1 i''_{L1,ref}\right) C_1 v_{c1} v'_{c1}}_{VI} + \underbrace{\left(-v'_g + L_1 i''_{L1,ref}\right) i_{L2}\left(-v_g + v_{c1} + L_1 i'_{L1,ref}\right)}_{VII} \end{aligned} \tag{5.32}$$

This is a multi-variable non-linear equation. It can be linearized by introducing perturbations in different variables around their respective equilibrium values.

$$v_g = V_g + \tilde{v}_g, v_o = V_o + \tilde{v}_o, v_{o,ref} = V_{o,ref} + \tilde{v}_{o,ref}, R = R_e + \tilde{R} \tag{5.33}$$

To linearize the closed-loop dynamics, the perturbation terms with order greater than one and the terms having the mutual product of perturbations have been neglected (For example, terms $\tilde{R}^2, \tilde{v}_o^2, \tilde{v}_o\tilde{R}, \tilde{v}_o\tilde{R}'$ are neglected for simplification purpose)

The multiple differentiations of these variables give

$$\begin{aligned} &v_g' = \tilde{v}_g', v_g'' = \tilde{v}_g'', \\ &v_o' = \tilde{v}_o', v_o'' = \tilde{v}_o'', v_o''' = \tilde{v}_o''', v_o^{(4)} = \tilde{v}_o^{(4)} \\ &v_{o,ref}' = \tilde{v}_{o,ref}', v_{o,ref}'' = \tilde{v}_{o,ref}'', v_{o,ref}''' = \tilde{v}_{o,ref}''', v_{o,ref}^{(4)} = \tilde{v}_{o,ref}^{(4)} \\ &R' = \tilde{R}', R'' = \tilde{R}'' \end{aligned} \tag{5.34}$$

Also $$\frac{1}{R} = \frac{1}{R_e + \tilde{R}} = \frac{1}{R_e}\left(1 + \frac{\tilde{R}}{R_e}\right)^{-1} = \frac{1}{R_e}\left(1 - \frac{\tilde{R}}{R_e} + \frac{\tilde{R}^2}{R_e^2} - \cdots\right) = \frac{1}{R_e} - \frac{\tilde{R}}{R_e^2} \tag{5.35}$$

Differentiating (5.5) thrice, we get

$$i_{L1,ref}' = K_p\left(\tilde{v}_{o,ref}' - \tilde{v}_o'\right) + K_i\left(\tilde{v}_{o,ref} - \tilde{v}_o\right) \tag{5.36}$$

$$i_{L1,ref}'' = K_p\left(\tilde{v}_{o,ref}'' - \tilde{v}_o''\right) + K_i\left(\tilde{v}_{o,ref}' - \tilde{v}_o'\right) \tag{5.37}$$

$$i_{L1,ref}''' = K_p\left(\tilde{v}_{o,ref}''' - \tilde{v}_o'''\right) + K_i\left(\tilde{v}_{o,ref}'' - \tilde{v}_o''\right) \tag{5.38}$$

Replacing value of 1/*R* from (5.35) into (5.29),

$$\begin{aligned} &i_{L2} = \frac{v_o}{R} + C_2 v_o' = \left(V_o + \tilde{v}_o\right)\left(\frac{1}{R_e} - \frac{\tilde{R}}{R_e^2}\right) + C_2\tilde{v}_o' \\ \Rightarrow \quad &i_{L2} = \frac{1}{R_e}\left(V_o + \tilde{v}_o\right) - \frac{V_o}{R_e^2}\tilde{R} + C_2\tilde{v}_o' \end{aligned} \tag{5.39}$$

Differentiating (5.39) twice, we get

$$i_{L2}' = \frac{\tilde{v}_o'}{R_e} - \frac{V_o}{R_e^2}\tilde{R}' + C_2\tilde{v}_o'' \tag{5.40}$$

$$i_{L2}'' = \frac{\tilde{v}_o''}{R_e} - \frac{V_o}{R_e^2}\tilde{R}'' + C_2\tilde{v}_o''' \tag{5.41}$$

Substituting values of $i_{L1,ref}'$ from (5.36) and i_{L2}' from (5.40) into (5.27), we get

$$v_{c1} = V_o + \tilde{v}_o + V_g + \tilde{v}_g + L_2\left(\frac{\tilde{v}_o'}{R_e} - \frac{V_o}{R_e^2}\tilde{R}' + C_2\tilde{v}_o''\right) - L_1\left\{K_p\left(\tilde{v}_{o,ref}' - \tilde{v}_o'\right) + K_i\left(\tilde{v}_{o,ref} - \tilde{v}_o\right)\right\} \tag{5.42}$$

Differentiating (5.42) twice, we get

$$v_{c1}' = \tilde{v}_o' + \tilde{v}_g' + L_2\left(\frac{\tilde{v}_o''}{R_e} - \frac{V_o}{R_e^2}\tilde{R}'' + C_2\tilde{v}_o'''\right) - L_1\left\{K_p\left(\tilde{v}_{o,ref}'' - \tilde{v}_o''\right) + K_i\left(\tilde{v}_{o,ref}' - \tilde{v}_o'\right)\right\} \tag{5.43}$$

$$v_{c1}'' = \tilde{v}_o'' + \tilde{v}_g'' + L_2\left(\frac{\tilde{v}_o'''}{R_e} - \frac{V_o}{R_e^2}\tilde{R}''' + C_2\tilde{v}_o^{(4)}\right) - L_1\left\{K_p\left(\tilde{v}_{o,ref}''' - \tilde{v}_o'''\right) + K_i\left(\tilde{v}_{o,ref}'' - \tilde{v}_o''\right)\right\} \tag{5.44}$$

Simplification of (5.32): This equation is simplified in different parts. Any higher-order perturbation term and their mutual products are neglected to get the linearize model.

Part 1:

$$I = \left(v_g - L_1 i'_{L1,ref}\right)^2 i'_{L1,ref} = v_g^2 i'_{L1,ref} - 2v_g L_1 i'^2_{L1,ref} + L_1^2 i'^3_{L1,ref} \tag{5.45}$$

Substituting $v_g = V_g + \tilde{v}_g$ and $i'_{L1,ref}$ from (5.36) into (5.45) and simplifying, we get

$$I = V_g^2 \left\{K_p \left(\tilde{v}'_{o,ref} - \tilde{v}'_o\right) + K_i \left(\tilde{v}_{o,ref} - \tilde{v}_o\right)\right\} \tag{5.46}$$

Part 2:

$$II = \left(v_g - L_1 i'_{L1,ref}\right) i'_{L2} \left(-v_g + v_{c1} + L_1 i'_{L1,ref}\right) \tag{5.47}$$

Substituting $v_g = V_g + \tilde{v}_g$, $i'_{L1,ref}$ from (5.36) and v_{c1} from (5.42) into (5.47) and simplifying, we get

$$II = V_g V_o \left(\frac{\tilde{v}'_o}{R_e} - \frac{V_o}{R_e^2}\tilde{R}' + C_2 \tilde{v}''_o\right) \tag{5.48}$$

Part 3:

$$III = \left(v_g - L_1 i'_{L1,ref}\right) i_{L2} \left(-v'_g + v'_{c1} + L_1 i''_{L1,ref}\right) \tag{5.49}$$

Substituting $v_g = V_g + \tilde{v}_g$, $i'_{L1,ref}$ and $i''_{L1,ref}$ from (5.36)-(5.37) and v'_{c1} from (5.43) into (5.49) and simplifying, we get

$$III = \frac{V_g V_o}{R_e}\left\{\tilde{v}'_o + L_2\left(\frac{\tilde{v}''_o}{R_e} - \frac{V_o}{R_e^2}\tilde{R}'' + C_2 \tilde{v}'''_o\right)\right\} \tag{5.50}$$

Part 4:

$$IV = \left(v_g - L_1 i'_{L1,ref}\right) C_1 v_{c1} v''_{c1} \tag{5.51}$$

Substituting $v_g = V_g + \tilde{v}_g$, v_{c1} and v''_{c1} from (5.42),(5.44) and $i'_{L1,ref}$ from (5.36) into (5.51) and then simplifying, we get

$$IV = C_1 V_g \left(V_o + V_g\right)\left[\tilde{v}''_o + \tilde{v}''_g + L_2\left(\frac{\tilde{v}'''_o}{R_e} - \frac{V_o}{R_e^2}\tilde{R}''' + C_2 \tilde{v}_o^{(4)}\right) - L_1\left\{K_p\left(\tilde{v}'''_{o,ref} - \tilde{v}'''_o\right) + K_i\left(\tilde{v}''_{o,ref} - \tilde{v}''_o\right)\right\}\right] \tag{5.52}$$

Part 5:

$$V = \left(v_g - L_1 i'_{L1,ref}\right) C_1 v'^2_{c1} \tag{5.53}$$

Substituting $v_g = V_g + \tilde{v}_g$, $i'_{L1,ref}$ from (5.36) and v'_{c1} from (5.43) and then simplifying, we have

$$V = 0 \tag{5.54}$$

Part 6:

$$VI = \left(-v'_g + L_1 i''_{L1,ref}\right) C_1 v_{c1} v'_{c1} \tag{5.55}$$

Substituting $i''_{L1,ref}$ from (5.37), v_{c1} and v'_{c1} from (5.42)-(5.43) and then simplifying, we have

$$VI = 0 \tag{5.56}$$

Part 7:

$$VII = \left(-v_g' + L_1 i_{L1,ref}''\right) i_{L2} \left(-v_g + v_{c1} + L_1 i_{L1,ref}'\right) \tag{5.57}$$

Substituting $i_{L1,ref}''$ from (5.37), v_{c1} and v_{c1}' from (5.42)-(5.43) and then simplifying, we get

$$VII = \frac{V_o^2}{R_e}\left\{-\tilde{v}_g' + L_1 K_p\left(\tilde{v}_{o,ref}'' - \tilde{v}_o''\right) + L_1 K_i\left(\tilde{v}_{o,ref}' - \tilde{v}_o'\right)\right\} \tag{5.58}$$

Collecting all these terms and substituting back into (5.32), we finally get

$$\begin{aligned}
&V_g^2\left\{K_p\left(\tilde{v}_{o,ref}' - \tilde{v}_o'\right) + K_i\left(\tilde{v}_{o,ref} - \tilde{v}_o\right)\right\} \\
&= V_g V_o\left(\frac{\tilde{v}_o'}{R_e} - \frac{V_o}{R_e^2}\tilde{R}' + C_2\tilde{v}_o''\right) + \frac{V_g V_o}{R_e}\left\{\tilde{v}_o' + L_2\left(\frac{\tilde{v}_o''}{R_e} - \frac{V_o}{R_e^2}\tilde{R}'' + C_2\tilde{v}_o'''\right)\right\} \\
&\quad + C_1 V_g\left(V_o + V_g\right)\left[\tilde{v}_o'' + \tilde{v}_g'' + L_2\left(\frac{\tilde{v}_o'''}{R_e} - \frac{V_o}{R_e^2}\tilde{R}''' + C_2\tilde{v}_o^{(4)}\right) - L_1\left\{K_p\left(\tilde{v}_{o,ref}''' - \tilde{v}_o'''\right) + K_i\left(\tilde{v}_{o,ref}'' - \tilde{v}_o''\right)\right\}\right] \\
&\quad + \frac{V_o^2}{R_e}\left\{-\tilde{v}_g' + L_1 K_p\left(\tilde{v}_{o,ref}'' - \tilde{v}_o''\right) + L_1 K_i\left(\tilde{v}_{o,ref}' - \tilde{v}_o'\right)\right\}
\end{aligned} \tag{5.59}$$

This expression gives the closed-loop dynamics of sliding mode controlled DC-DC Cuk converter. The different transfer function models relating the effect of variations in the different working conditions (reference voltage, input voltage, and load resistance) on the output voltage are evaluated in following subsections.

5.4.3.1 Transfer function for step variation in reference voltage

The transfer function relating the reference output voltage ($v_{o,ref}$) and actual output voltage (v_o) is obtained by setting perturbations in input voltage (v_g) and load resistance (R) and their derivatives to zero *i.e.,*

$$\tilde{v}_g = 0, \tilde{v}_g' = 0, \tilde{v}_g'' = 0, R_e = R, \tilde{R} = 0, \tilde{R}' = 0, \tilde{R}'' = 0, \tilde{R}''' = 0 \tag{5.60}$$

Substituting these values in (5.59), we get

$$\begin{aligned}
&V_g^2\left\{K_p\left(\tilde{v}_{o,ref}' - \tilde{v}_o'\right) + K_i\left(\tilde{v}_{o,ref} - \tilde{v}_o\right)\right\} \\
&= V_g V_o\left(\frac{\tilde{v}_o'}{R} + C_2\tilde{v}_o''\right) + \frac{V_g V_o}{R}\left\{\tilde{v}_o' + L_2\left(\frac{\tilde{v}_o''}{R} + C_2\tilde{v}_o'''\right)\right\} + \frac{V_o^2}{R}\left\{L_1 K_p\left(\tilde{v}_{o,ref}'' - \tilde{v}_o''\right) + L_1 K_i\left(\tilde{v}_{o,ref}' - \tilde{v}_o'\right)\right\} \\
&\quad + C_1 V_g\left(V_o + V_g\right)\left[\tilde{v}_o'' + L_2\left(\frac{\tilde{v}_o'''}{R} + C_2\tilde{v}_o^{(4)}\right) - L_1\left\{K_p\left(\tilde{v}_{o,ref}''' - \tilde{v}_o'''\right) + K_i\left(\tilde{v}_{o,ref}'' - \tilde{v}_o''\right)\right\}\right]
\end{aligned} \tag{5.61}$$

On simplification, we get

$$b_3\tilde{v}_{o,ref}''' + b_2\tilde{v}_{o,ref}'' + b_1\tilde{v}_{o,ref}' + b_0\tilde{v}_{o,ref} = a_4\tilde{v}_o^{(4)} + a_3\tilde{v}_o''' + a_2\tilde{v}_o'' + a_1\tilde{v}_o' + a_0\tilde{v}_o \tag{5.62}$$

Now taking the Laplace transform of (5.62), we get the reference voltage to output voltage transfer function as follows [194]:

$$\frac{\tilde{v}_o(s)}{\tilde{v}_{o,ref}(s)} = \frac{b_3 s^3 + b_2 s^2 + b_1 s + b_0}{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \tag{5.63}$$

Where,

$$b_3 = K_p L_1 C_1 V_g \left(V_o + V_g\right), b_2 = K_i L_1 C_1 V_g \left(V_o + V_g\right) - \frac{K_p L_1 V_o^2}{R}, b_1 = K_p V_g^2 - \frac{K_i L_1 V_o^2}{R}, b_0 = K_i V_g^2,$$

$$a_4 = L_2 C_1 C_2 V_g \left(V_o + V_g\right), a_3 = \frac{L_2 C_2 V_g V_o}{R} + \frac{L_2 C_1 V_g \left(V_o + V_g\right)}{R} + K_p L_1 C_1 V_g \left(V_o + V_g\right), a_0 = K_i V_g^2, \quad (5.64)$$

$$a_2 = C_2 V_g V_o + \frac{L_2 V_g V_o}{R^2} + C_1 V_g \left(V_o + V_g\right) + K_i L_1 C_1 V_g \left(V_o + V_g\right) - \frac{K_p L_1 V_o^2}{R}, a_1 = K_p V_g^2 + \frac{2V_g V_o - K_i L_1 V_o^2}{R},$$

This transfer function has four poles and three zeros. The location of poles and zeros depend on the Cuk converter parameters and PI controller parameters K_p and K_i. In original paper [192], the expressions for some of these coefficients (a_2, a_3, b_1) were wrong.

5.4.3.2 Transfer function for step variation in input voltage

The transfer function relating the input voltage (v_g) and output voltage (v_o) is obtained by setting the perturbations in reference output voltage ($v_{o,ref}$) and load resistance (R) and their derivatives to zero *i.e.,*

$$\tilde{v}_{o,ref} = 0, \tilde{v}'_{o,ref} = 0, \tilde{v}''_{o,ref} = 0, \tilde{v}'''_{o,ref} = 0, \tilde{v}^{(4)}_{o,ref} = 0, R_e = R, \tilde{R} = 0, \tilde{R}' = 0, \tilde{R}'' = 0, \tilde{R}''' = 0 \quad (5.65)$$

Substituting these values in (5.59), we get

$$\begin{aligned} & V_g^2 \left\{K_p \left(-\tilde{v}'_o\right) + K_i \left(-\tilde{v}_o\right)\right\} \\ & = V_g V_o \left(\frac{\tilde{v}'_o}{R} + C_2 \tilde{v}''_o\right) + \frac{V_g V_o}{R} \left\{\tilde{v}'_o + L_2 \left(\frac{\tilde{v}''_o}{R} + C_2 \tilde{v}'''_o\right)\right\} + \frac{V_o^2}{R} \left\{-\tilde{v}'_g + L_1 K_p \left(-\tilde{v}''_o\right) + L_1 K_i \left(-\tilde{v}'_o\right)\right\} \quad (5.66) \\ & + C_1 V_g \left(V_o + V_g\right) \left[\tilde{v}''_o + \tilde{v}''_g + L_2 \left(\frac{\tilde{v}'''_o}{R} + C_2 \tilde{v}^{(4)}_o\right) - L_1 \left\{K_p \left(-\tilde{v}'''_o\right) + K_i \left(-\tilde{v}''_o\right)\right\}\right] \end{aligned}$$

On simplification, we get

$$p_2 \tilde{v}''_g + p_1 \tilde{v}'_g = a_4 \tilde{v}^{(4)}_o + a_3 \tilde{v}'''_o + a_2 \tilde{v}''_o + a_1 \tilde{v}'_o + a_0 \tilde{v}_o \quad (5.67)$$

By taking the Laplace transform of (5.67), the input voltage to output voltage transfer function is obtained as [194]:

$$\frac{\tilde{v}_o(s)}{\tilde{v}_g(s)} = \frac{p_2 s^2 + p_1 s}{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \quad (5.68)$$

Where,

$$p_2 = -C_1 V_g \left(V_o + V_g\right), p_1 = \frac{V_o^2}{R} \quad (5.69)$$

The remaining coefficients of (5.68) is same as given in (5.64). This transfer function has four poles and two zeros. The locations of poles remain same as in previous transfer function. The one zero is situated at origin and other at $\frac{V_o^2}{RC_1 V_g \left(V_o + V_g\right)}$, which is always a positive value. However, original paper [192] incorrectly stated that this zero is always negative. A positive zero means that the closed-loop system for this particular case behaves as non-minimum phase system.

5.4.3.3 Transfer function for step variation in load resistance

The transfer function relating the load resistance (R) and output voltage (v_o) is obtained by setting the perturbations in reference output voltage ($v_{o,ref}$) and input voltage (v_g) and their derivatives to zero *i.e.,*

$$\tilde{v}_{o,ref}=0,\tilde{v}'_{o,ref}=0,\tilde{v}''_{o,ref}=0,\tilde{v}'''_{o,ref}=0,\tilde{v}^{(4)}_{o,ref}=0,\tilde{v}_g=0,\tilde{v}'_g=0,\tilde{v}''_g=0 \tag{5.70}$$

Substituting these values in (5.59), we get

$$\begin{aligned}
&V_g^2\left\{K_p\left(-\tilde{v}'_o\right)+K_i\left(-\tilde{v}_o\right)\right\}\\
&=V_gV_o\left(\frac{\tilde{v}'_o}{R_e}-\frac{V_o}{R_e^2}\tilde{R}'+C_2\tilde{v}''_o\right)+\frac{V_gV_o}{R_e}\left\{\tilde{v}'_o+L_2\left(\frac{\tilde{v}''_o}{R_e}-\frac{V_o}{R_e^2}\tilde{R}''+C_2\tilde{v}'''_o\right)\right\}+\frac{V_o^2}{R_e}\left\{L_1K_p\left(-\tilde{v}''_o\right)+L_1K_i\left(-\tilde{v}'_o\right)\right\}\\
&+C_1V_g\left(V_o+V_g\right)\left[\tilde{v}''_o+L_2\left(\frac{\tilde{v}'''_o}{R_e}-\frac{V_o}{R_e^2}\tilde{R}'''+C_2\tilde{v}^{(4)}_o\right)-L_1\left\{K_p\left(-\tilde{v}'''_o\right)+K_i\left(-\tilde{v}''_o\right)\right\}\right]
\end{aligned} \tag{5.71}$$

Upon simplification, we get

$$r_3\tilde{R}'''+r_2\tilde{R}''+r_1\tilde{R}'=a_4\tilde{v}^{(4)}_o+a_3\tilde{v}'''_o+a_2\tilde{v}''_o+a_1\tilde{v}'_o+a_0\tilde{v}_o \tag{5.72}$$

By taking the Laplace transform of (5.72), the load resistance to output voltage transfer function is

$$\frac{\tilde{v}_o(s)}{\tilde{R}(s)}=\frac{r_3s^3+r_2s^2+r_1s}{a_4s^4+a_3s^3+a_2s^2+a_1s+a_0} \tag{5.73}$$

Where,

$$r_3=\frac{L_2C_1V_gV_o\left(V_o+V_g\right)}{R_e^2},r_2=\frac{L_2V_gV_o^2}{R_e^3},r_1=\frac{V_gV_o^2}{R_e^2} \tag{5.74}$$

The remaining coefficients of (5.74) is same as given in (5.64). This transfer function has four poles and three zeros. The locations of poles remain same as in previous transfer function. The one zero is situated at the origin and the locations of other two zeros depend upon the Cuk converter parameters. In the original paper [192], this transfer function was derived incorrect, which stated that the transfer function has only two zeros.

5.4.4 Selection of parameters of SM based PI controller

In the previous section, the transfer functions describing the closed-loop dynamics of PI-SM controlled Cuk converter were derived. Therefore, from these transfer functions, the characteristic equation for this closed-loop system can be written as

$$a_4s^4+a_3s^3+a_2s^2+a_1s+a_0=0 \tag{5.75}$$

This characteristic equation is function of Cuk converter parameters and PI controller parameters K_p and K_i. For this closed-loop system to be stable, the value of K_p and K_i must be selected such that the all four poles lie in the left half of the s-plane. Here, two methods are discussed.

5.4.4.1 Existing method using Routh-Hurwitz stability criterion

In this method, the values of K_p and K_i were found with the application of Routh-Hurwitz stability criterion [192]. The following Routh array is constructed for the characteristic equation in (5.75).

$$\begin{array}{c|ccc} s^4 & a_4 & a_2 & a_0 \\ s^3 & a_3 & a_1 & \\ s^2 & h_1 & a_0 & \\ s^1 & h_2 & & \\ s^0 & a_0 & & \end{array} \tag{5.76}$$

Where, $h_1 = \dfrac{a_3 a_2 - a_4 a_1}{a_3}, h_2 = \dfrac{h_1 a_1 - a_3 a_0}{h_1}$

According to Routh-Hurwitz stability criterion, this closed-loop system will be stable only if the elements of the first column are positive *i.e.,*

$$a_4 > 0, a_3 > 0, h_1 > 0, h_2 > 0, a_0 > 0 \tag{5.77}$$

Referring the expressions of these coefficients in (5.64), it is observed that a_3 and a_4 is always positive, whereas a_0 is positive if the value of K_i is positive. However, the expressions for coefficient h_1 and h_2 are complex and it is very difficult to get the analytical solutions for K_p and K_i satisfying h_1>0 and h_2>0 together. It can be solved using either the trial and error method or numerical method. In the original paper, the values of K_p and K_i were determined using root locus approach. However, All these approaches are complex and time consuming. On the other hand, in this thesis, a simplified approach is used based on the stability boundary locus method [161].

5.4.4.2 Proposed method using the stability boundary locus method

The coefficients of characteristic equation in (5.75) are rearranged in following manner.

$$a_{43}s^4 + \left(a_{31}K_p + a_{33}\right)s^3 + \left(a_{21}K_p + a_{22}K_i + a_{23}\right)s^2 + \left(a_{11}K_p + a_{12}K_i + a_{13}\right)s + a_{02}K_i = 0 \tag{5.78}$$

Where,

$a_4 = a_{43}$, $a_{43} = L_2C_1C_2V_g\left(V_o + V_g\right)$,

$a_3 = \left(a_{31}K_p + a_{33}\right)$, $a_{31} = L_1C_1V_g\left(V_o + V_g\right), a_{33} = \dfrac{L_2C_2V_gV_o}{R} + \dfrac{L_2C_1V_g\left(V_o + V_g\right)}{R}$

$a_2 = \left(a_{21}K_p + a_{22}K_i + a_{23}\right)$, $a_{21} = -\dfrac{L_1V_o^2}{R}, a_{22} = L_1C_1V_g\left(V_o + V_g\right), a_{23} = C_2V_gV_o + \dfrac{L_2V_gV_o}{R^2} + C_1V_g\left(V_o + V_g\right)$,

$a_1 = \left(a_{11}K_p + a_{12}K_i + a_{13}\right)$, $a_{11} = V_g^2, a_{12} = -\dfrac{L_1V_o^2}{R}, a_{13} = \dfrac{2V_gV_o}{R}$,

$a_0 = a_{02}K_i$, $a_{02} = V_g^2$,

Equation (5.78) is further written in following form:

$$1 + G_{new}\left(s\right) = 0 \tag{5.79}$$

$$G_{new}(s)=\frac{\left(a_{31}s^3+a_{21}s^2+a_{11}s\right)K_p+\left(a_{22}s^2+a_{12}s+a_{02}\right)K_i}{a_{43}s^4+a_{33}s^3+a_{23}s^2+a_{13}s} \tag{5.80}$$

For characteristic equation in (5.79), $G_{new}(s)$ is a compensated loop transfer function.

Now, the stability boundary locus approach [161] is used to determine the values of parameters K_p and K_i, which would stabilize the closed-loop system. Moreover, these parameters are determined to satisfy the desired gain margin and phase margin. The stepwise procedure is given below.

Step 1: Specify the desired gain margin A and phase margin φ (in degree). To satisfy these stability margins, the characteristic equation becomes

$$1+Ae^{-j\varphi}G_{new}(s)=0 \tag{5.81}$$

Step 2: In the above equation, first substituting $s=j\omega$ and then separating the real and imaginary parts, two equations are obtained. These two equations are functions of ω, A, φ, K_p and K_i.

Then, these two equations are simplified to get the expressions for K_p and K_i as follows:

$$K_p=f_1(\omega,A,\varphi),K_i=f_2(\omega,A,\varphi) \tag{5.82}$$

Step 3: Now, for desired value of gain margin A and phase margin φ, two different stability boundary locus in K_p-K_i plane are plotted by varying ω. To obtain the stability boundary locus for desired gain margin A, we substitute $\varphi=0$ in (5.82) whereas to obtain the stability boundary locus for desired phase margin φ, we substitute $A=1$ in (5.82).

The intersection of these two boundary locus provides the stability region for desired gain margin and phase margin. Any pair of K_p and K_i selected within this region will stabilize the closed system with guaranteed desired stability margins.

5.5 Design example

The parameters of the Cuk converter used for simulation and experimental validation of the sliding mode control scheme are same as used in the previous chapter (Table 4.9). By substituting these values in (5.75), the characteristic equation is

$$\begin{aligned}&2.41\times10^{-7}s^4+\left(9.07\times10^{-4}K_p+7.54\times10^{-5}\right)s^3\\&+\left(-0.0698K_p+9.07\times10^{-4}K_i+0.44\right)s^2+\left(400K_p-0.0698K_i+58.2\right)s+400K_i=0\end{aligned} \tag{5.83}$$

Rearranging this characteristic equation,

$$1+\frac{\left(9.07\times10^{-4}s^3-0.0698s^2+400s\right)K_p+\left(9.07\times10^{-4}s^2-0.0698s+400\right)K_i}{2.41\times10^{-7}s^4+7.54\times10^{-5}s^3+0.44s^2+58.2s}=0 \tag{5.84}$$

For desired gain margin A and phase margin φ, the characteristic equation becomes

$$1+Ae^{-j\varphi}\frac{\left(9.07\times10^{-4}s^3-0.0698s^2+400s\right)K_p+\left(9.07\times10^{-4}s^2-0.0698s+400\right)K_i}{2.41\times10^{-7}s^4+7.54\times10^{-5}s^3+0.44s^2+58.2s}=0 \tag{5.85}$$

Substituting $s=j\omega$ in the above equation and separating real and imaginary parts, we get two equations as

$$AK_p\left[\left(-9.07\times10^{-4}\omega^3+400\omega\right)\sin\varphi+0.0698\omega^2\cos\varphi\right]+ AK_i\left[\left(-9.07\times10^{-4}\omega^2+400\right)\cos\varphi-0.0698\omega\sin\varphi\right]=0.44\omega^2-2.41\times10^{-7}\omega^4 \quad (5.86)$$

$$AK_p\left[\left(-9.07\times10^{-4}\omega^3+400\omega\right)\cos\varphi-0.0698\omega^2\sin\varphi\right]+ AK_i\left[\left(9.07\times10^{-4}\omega^2-400\right)\sin\varphi-0.0698\omega\cos\varphi\right]=-58.2\omega+7.54\times10^{-5}\omega^3 \quad (5.87)$$

Now these two equations are simplified for K_p and K_i and stability boundary locus are plotted for desired gain margin of 20 dB (corresponding to A=10) and phase margin of 90°. The two boundary locus in K_p-K_i plane are obtained by varying ω as shown in Fig. 5.4. The intersection portion is shown by the shaded area. Any combination of K_p and K_i selected within this area gives the stability margins greater than or equal to the specified margins (20 dB gain margin and 90° phase margin). Here, the parameters K_p= 0.4 and K_i=40 have been selected within this region. The bode plot of the compensated system with K_p= 0.4 and K_i=40 is shown in Fig. 5.5. It shows that the gain margin (21.6 dB) and phase margin (90.1°) of the compensated system are greater than the specified.

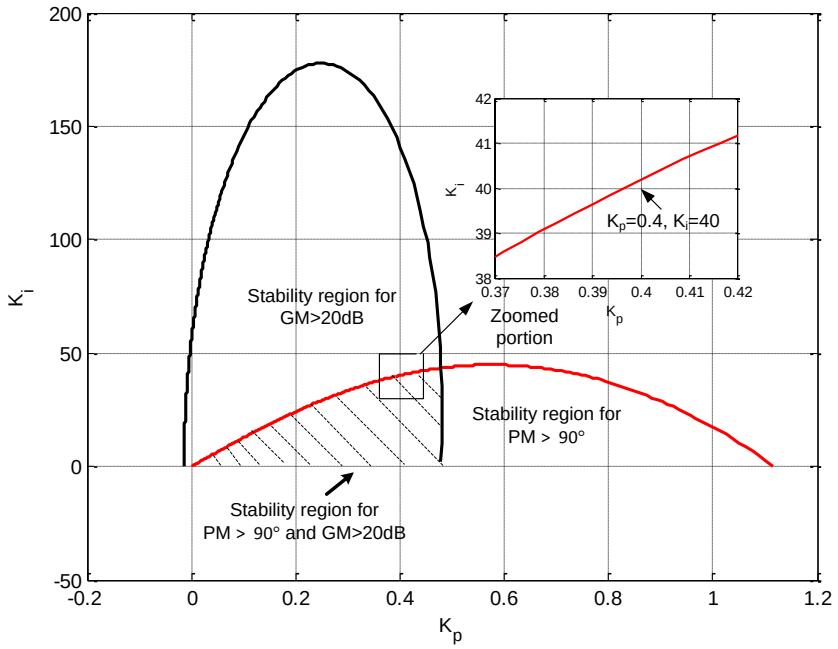


Fig. 5.4. Stability boundary locus for sliding mode control of DC-DC Cuk converter

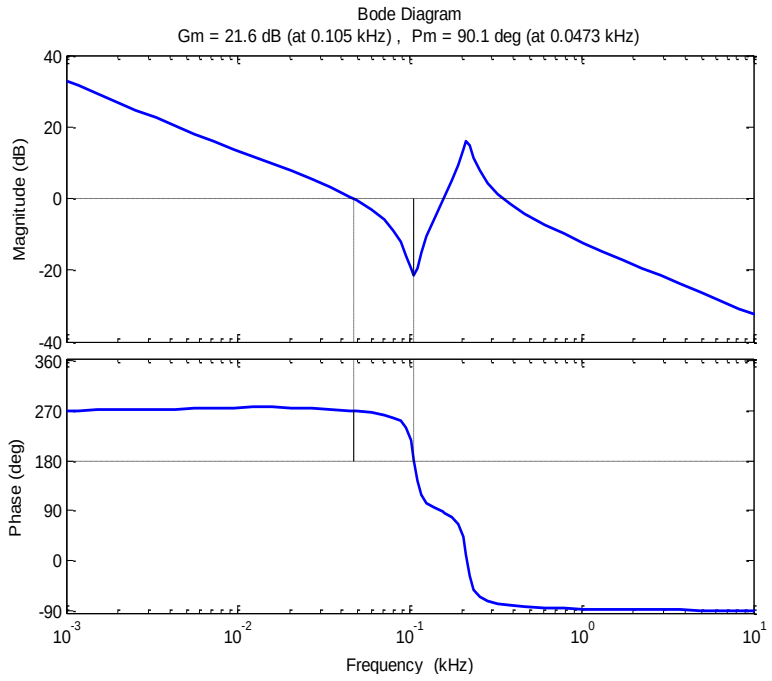


Fig. 5.5. Bode plot of sliding mode controlled Cuk converter with K_p= 0.4 and K_i=40

5.6 Results and discussion

The main purpose of this section is to analyse the performance of DC-DC Cuk converter with the designed sliding mode controller. For this purpose, the simulation and experimental results are obtained under different working conditions. The experimental results are obtained implementing sliding mode control using dSPACE system. The PI controller parameters used are K_p= 0.4 and K_i=40. The inductor current and output voltage are sensed using current and voltage sensors and fed to dSPACE controller via ADC channels. The desired switching pulse is generated and received at a Master I/O bit of the dSPACE connector panel. This switching pulse is connected to the MOSFET switch of the Cuk converter via driver circuit. The different components of experimental work are explained in Appendix *B*.

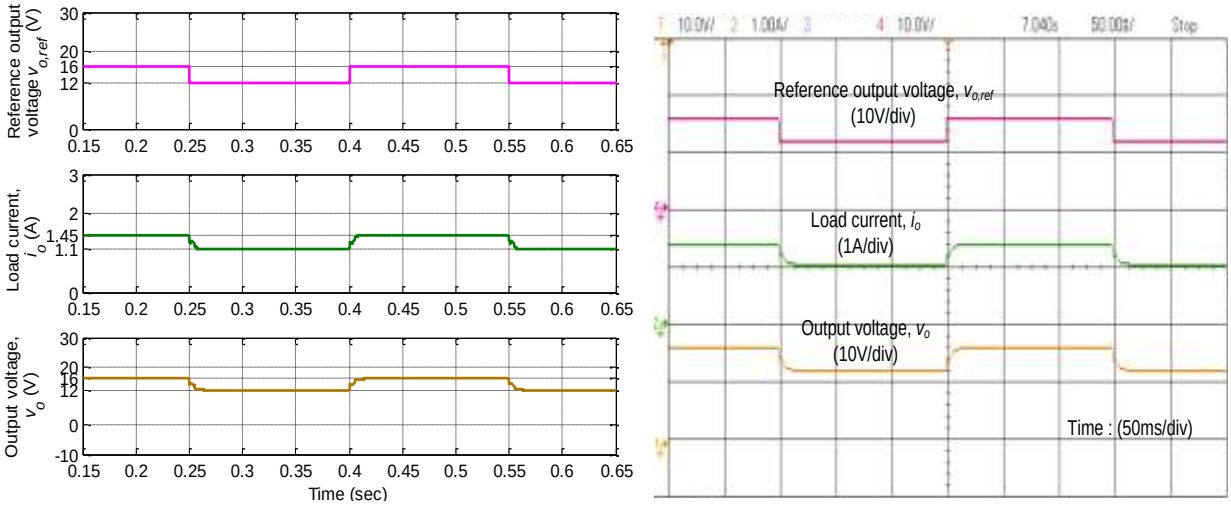
(a) Variation in reference output voltage

In this case, the input voltage (V_g) and load resistance (R) are kept constant to 20 V and 11 Ω, respectively while the reference output voltage is varied. For reference voltage variation from 16 V to 12 V and vice-versa, the simulation and experimental results are shown in Fig. 5.6 (a). Similarly, for reference voltage variation from 16 V to 20 V and vice-versa, the corresponding results are shown in Fig. 5.6 (b). The results demonstrate that the output voltage smoothly settles to steady-state (16 V) within 15 -20 ms without any oscillation and undershoot/overshoot. As the load resistance is fixed to 11 Ω; the load current is 1.09 A, 1.45 A and 1.81 A for different desired output voltage 12 V, 16 V and 20 V, respectively. The simulation and experimental results are closely matched verifying the performance of the designed sliding mode control.

(b) Variation in input voltage

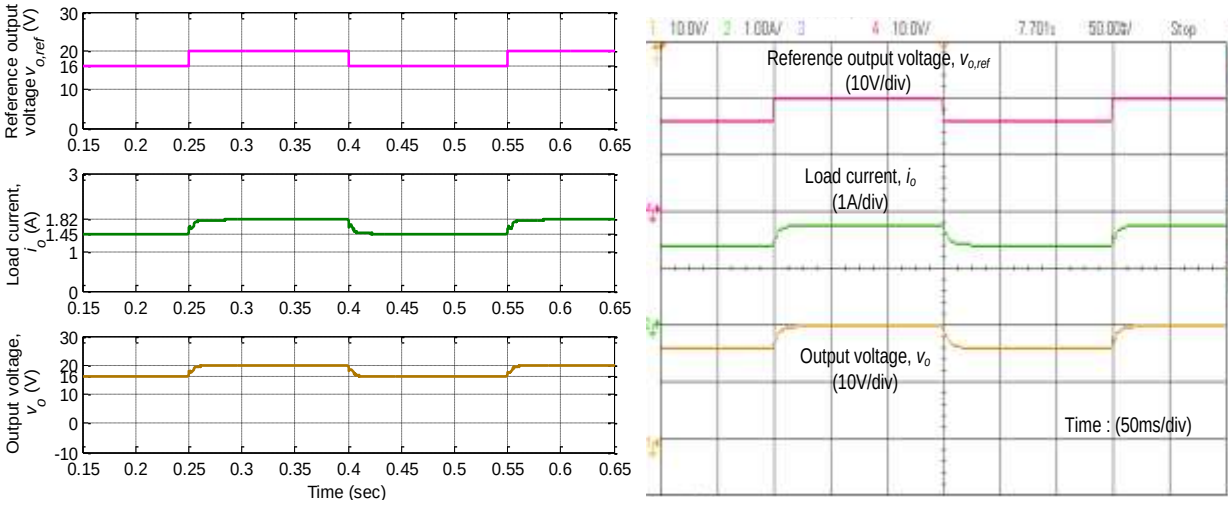
In this case, the input voltage (V_g) is varied from minimum (20 V) to maximum (28 V) and vice-versa for two extreme load conditions R=11 Ω (*i.e.,* maximum load current, 1.45 A) and R=22 Ω (*i.e.,* minimum load current, 0.73 A). The desired output voltage is 16 V.

For fixed load resistance of 11 Ω, when the input voltage is varied from 20 V to 28 V and vice-versa; the results are shown in Fig. 5.7 (a) and Fig. 5.7 (b), respectively. Similarly, when at a fixed load of 22 Ω, the input voltage is varied from 20 V to 28 V and vice-versa; the results are shown in Fig. 5.8 (a) and Fig. 5.8 (b), respectively. The output voltage reaches to steady-state (16 V) within 30-40 ms. The output voltage has overshoot of 1.6 V and undershoot of 3.6-4 V when the input voltage is increased from 20 V to 28 V. Similarly, when the input voltage is decreased from 28 V to 20 V, the output voltage has undershoot of 1.6-1.8 V and overshoot of 3.6-4 V. The experimental results vary slightly from simulation results in transient condition. The reason is that the step change in input voltage was realized using a manual switch. Therefore, in this particular case, the initial part of transients in the experimental output voltage is ignored while comparing with the simulation results.



Simulation Experimental

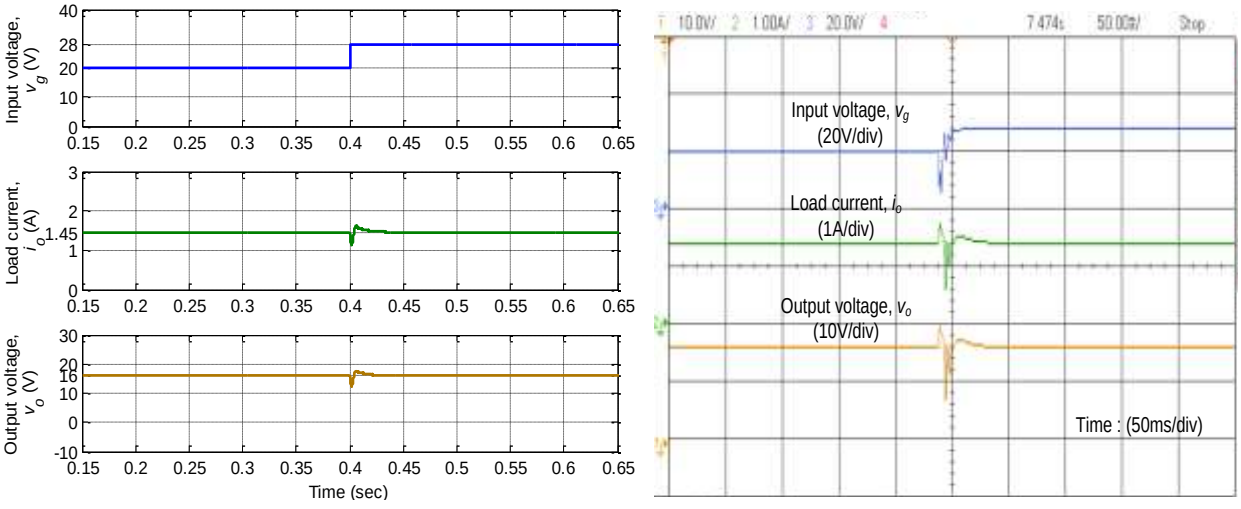
(a)



Simulation Experimental

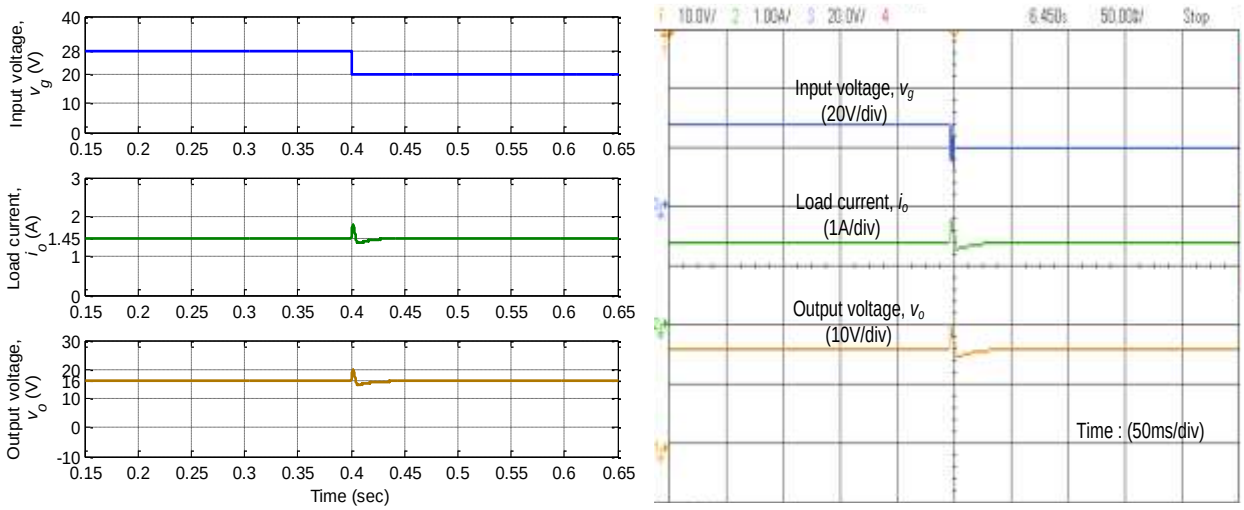
(b)

Fig. 5.6. Simulation and experimental results for reference output voltage variation from (a) 16 V to 12 V and vice-versa (b) 16 V to 20 V and vice-versa



Simulation Experimental

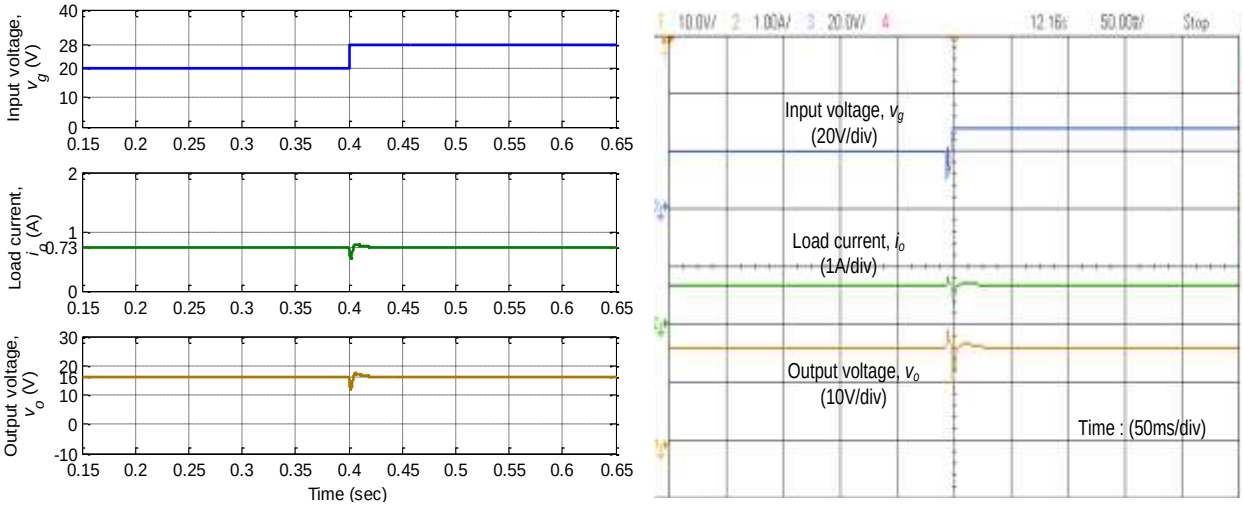
(a)



Simulation Experimental

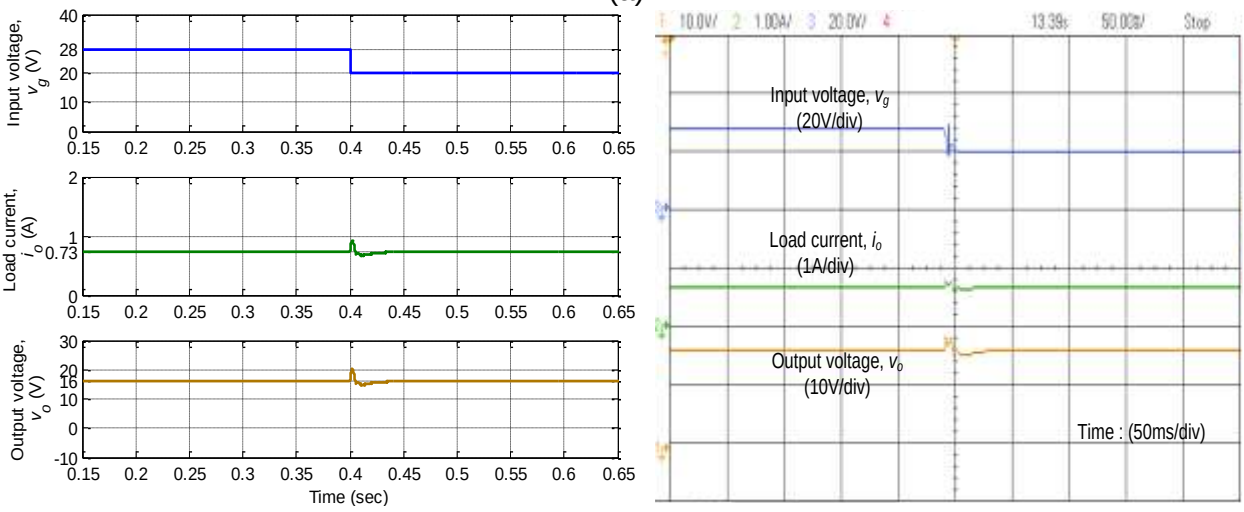
(b)

Fig. 5.7. Simulation and experimental results with R=11 Ω for input voltage variation from (a) 20 V to 28 V (b) 28 V to 20 V



Simulation Experimental

(a)



Simulation Experimental

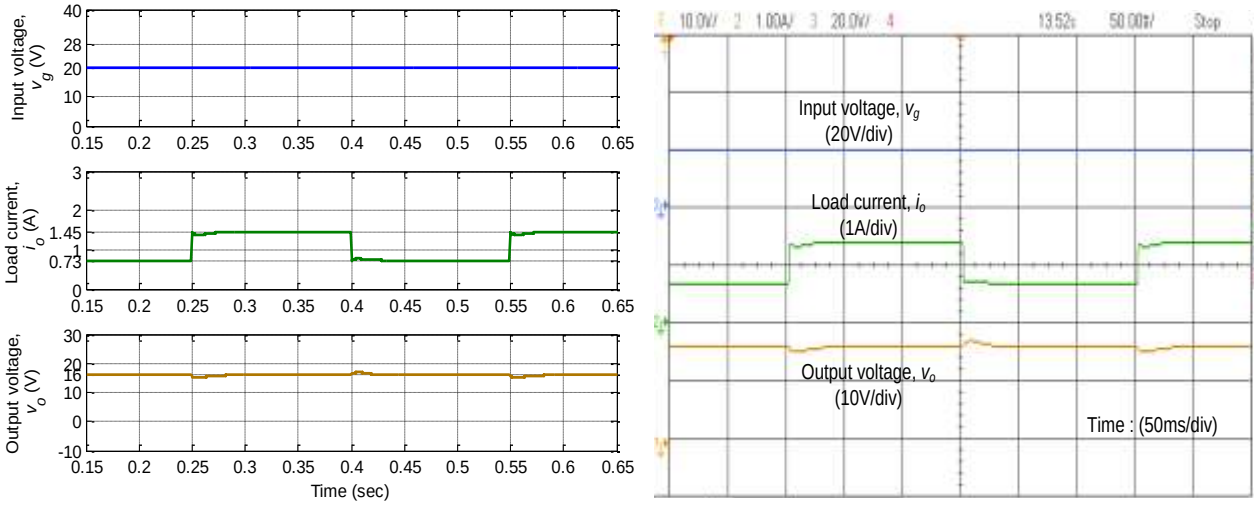
(b)

Fig. 5.8. Simulation and experimental results with R=22 Ω for input voltage variation from (a) 20 V to 28 V (b) 28 V to 20 V

(c) Variation in load resistance or load current

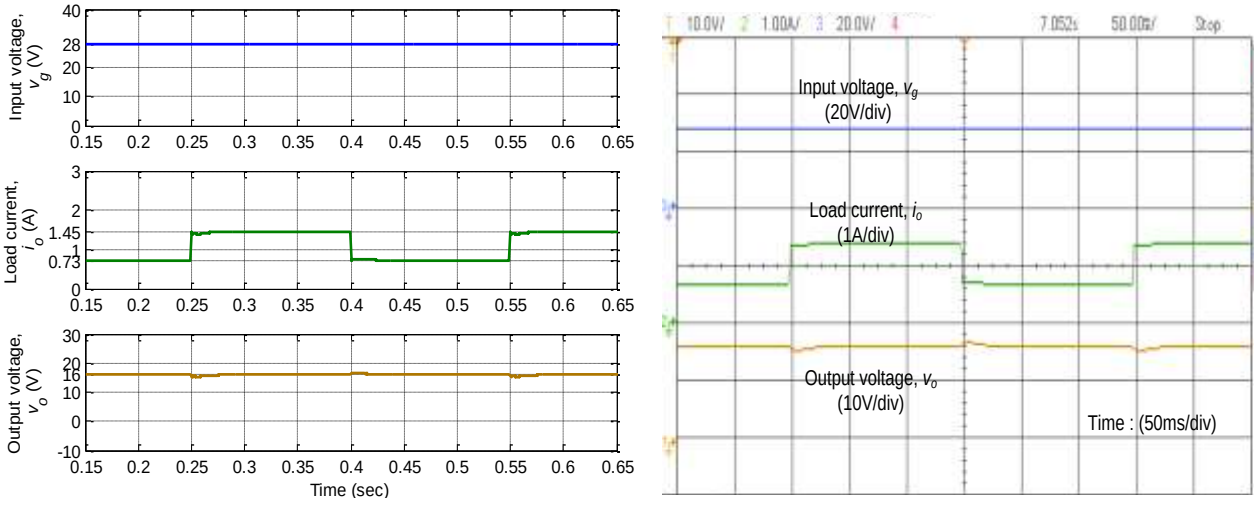
In this case, the load resistance (R) is varied from 22 Ω (*i.e.,* minimum load current, 0.73 A) to 11 Ω (*i.e.,* maximum load current, 1.45 A) and vice-versa for two extreme input voltages V_g=20 V (minimum) and V_g=28 V (maximum). The desired output voltage is 16 V.

The simulation and experimental results are shown in Fig. 5.9 (a) for step variation in load resistance from 22 Ω to 11 Ω and vice-versa at fixed input voltage 20 V. Similarly, for same load variation, but at constant input voltage 28 V; the results are shown in Fig. 5.9 (b). From these results, it is observed that the output voltage settles within 20 ms. The output voltage has small undershoot of 0.8 V and overshoot of 1 V when the load is switched from 22 Ω to 11 Ω and 11 Ω to 22 Ω, respectively. The experimental results are in close agreement with the simulation results validating the performance of the sliding mode controller.



Simulation Experimental

(a)



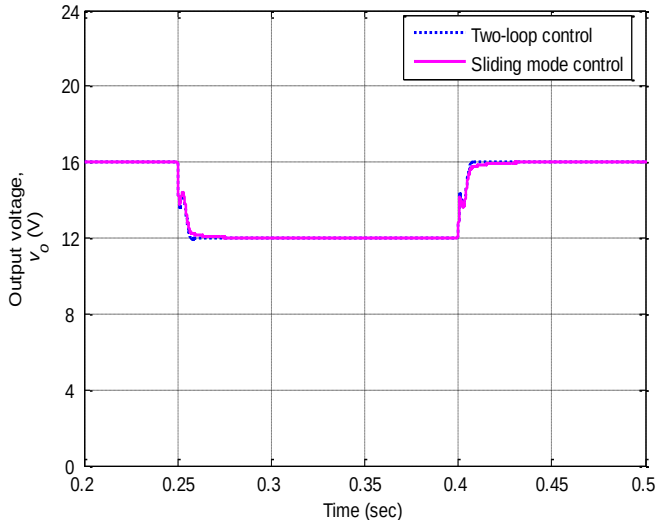
Simulation Experimental

(b)

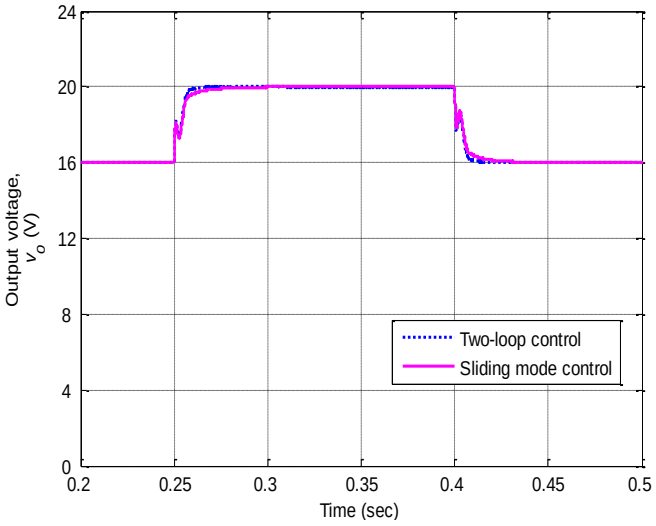
Fig. 5.9. Simulation and experimental results for variation in load resistance from 22 Ω to 11 Ω and vice-versa at input voltage (a) V_g=20 V (b) V_g=28 V

5.7 Performance comparison of two-loop PI control and sliding mode control of Cuk converter

In the previous chapter, it was concluded that the two-loop PI control of Cuk converter gives better performance in comparison to PI and PI-lead controllers. Now, in this section, the performance of two-loop PI controller is compared with the sliding mode controller. The output voltage of the Cuk converter under various operating conditions is shown in Fig. 5.10. This figure shows that the results in both the cases are almost similar. In the sliding mode control, the settling time is slightly more because the gain crossover frequency of the compensated system is less in comparison to two-loop PI controller. Though the dynamic and steady-state performances of both the controllers are almost same, but in sliding mode control, only one PI controller is required which is easier to tune than the two PI controllers in two-loop control. Moreover, in sliding mode control, there is no need of PWM modulator, as sliding mode control directly generates the gate pulses.

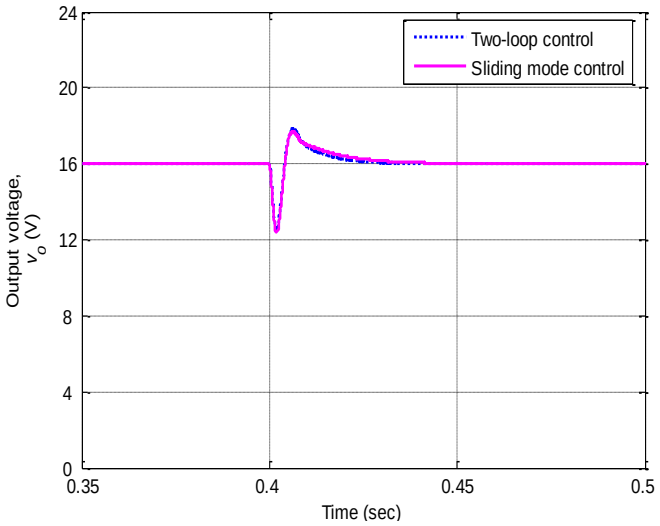


V_{ref}=16 V to 12 V and vice-versa

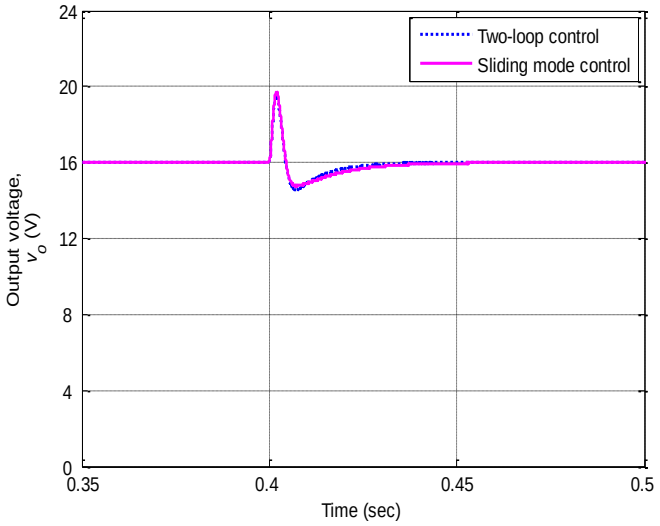


V_{ref}=16 V to 20 V and vice-versa

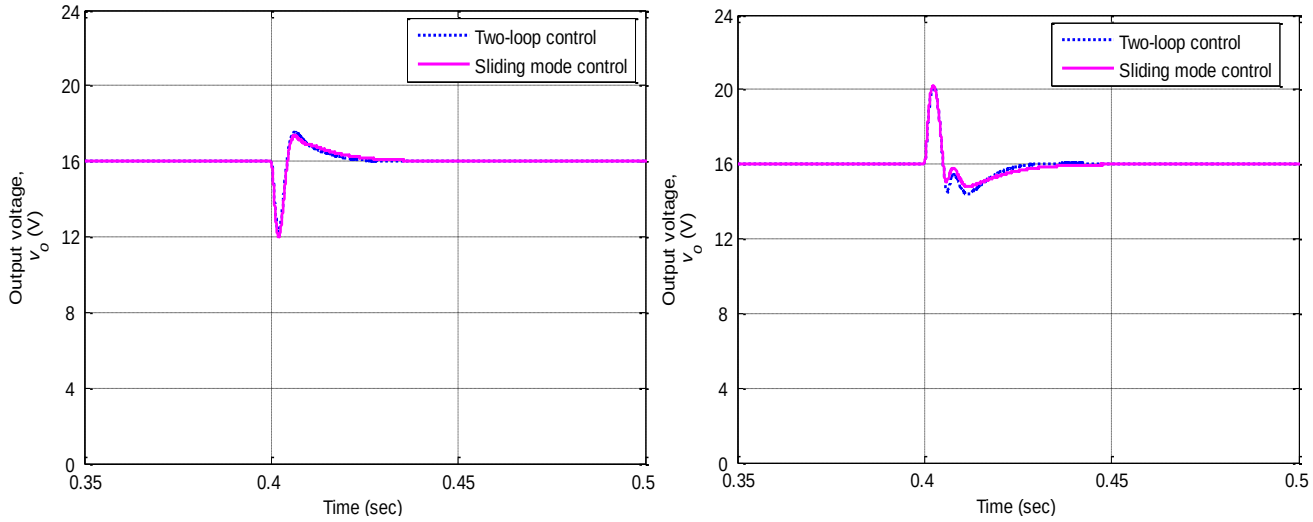
(a)



V_g=20 V to 28 V with R=11 Ω



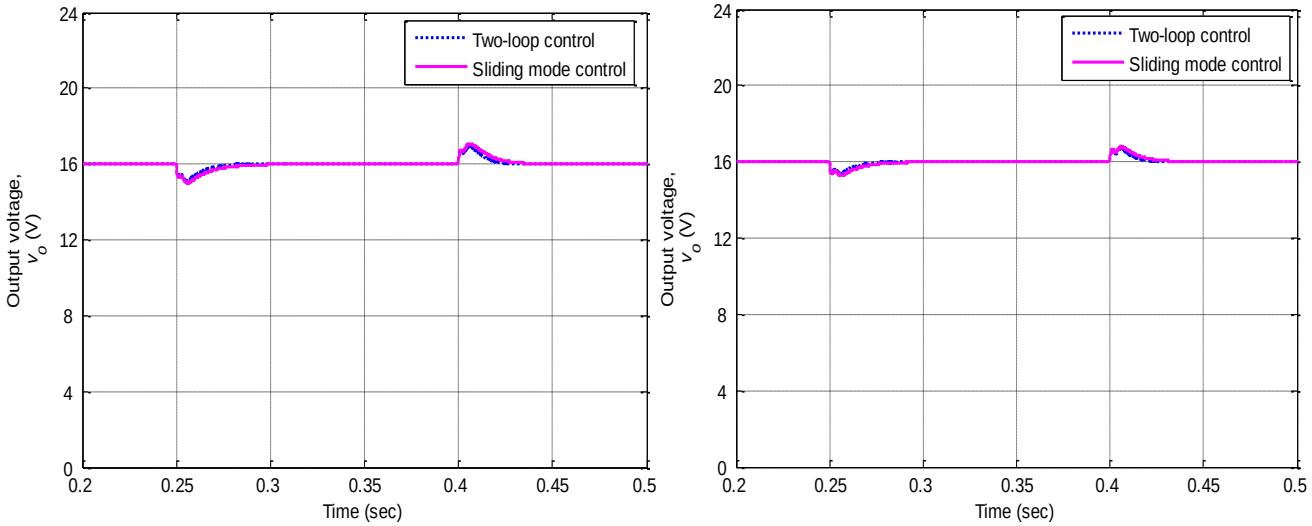
V_g=28 V to 20 V with R=11 Ω



V_g=20 V to 28 V with R=22 Ω

V_g=28 V to 20 V with R=22 Ω

(b)



R=22 Ω to 11 Ω and vice-versa with V_g=20 V

R=22 Ω to 11 Ω and vice-versa with V_g=28 V

(c)

Fig. 5.10. Performance comparison of two-loop control and sliding mode control for Cuk converter: Output voltage for variation in (a) reference output voltage (b) input voltage (c) load current

5.8 Conclusion

This chapter has presented the sliding mode control of DC-DC Cuk converter. The correct analysis and derivation of various transfer functions were carried out. A simple approach based on stability boundary locus was used to tune the parameters of sliding mode based PI controller. It is found from the simulation and experimental results that the performance of the designed sliding mode controller is almost similar to two-loop PI control. However, sliding mode control requires to design only one PI parameters and there is no need of the PWM modulator to generate the switching pulses.

[The main conclusion of the research work presented in this thesis and the possible future research in this area has been summarized in this chapter.]

6.1 Conclusion

In this thesis, the design, mathematical modeling and control issues of non-ideal DC-DC converters are discussed. These issues have been discussed for the two typical non-ideal DC-DC converter topologies namely buck converter (second-order system) and Cuk converter (fourth-order system). In this thesis, the DC-DC converters have been considered non-ideal while evaluating their design equations and mathematical models. The outcome of this research work on design, modeling and control issues can be summarized as follows:

1. In the research related to design issues, it was observed that the ideal duty cycle (calculated by considering the converter to be ideal) results in a lesser voltage than the desired. This voltage drop is due to the power loss occurring across the different resistive components of the converter elements. Therefore, the improved expressions for duty cycle of the buck and Cuk converter were derived incorporating the major non-idealities present in the converter elements. The design equation for inductors and capacitors were also improved considering buck and Cuk converters non-ideal. It is found that the required values of these elements are more in case of non-ideal consideration. Further, the output voltage ripple analysis has been carried out and a formula for maximum possible value of ESR was derived. The ESR of output capacitor less than this maximum value ensures that the output voltage ripple will be within specified limit. The theoretical analysis has been validated by simulation and experimental results.
2. The input voltage to output voltage, load current to output voltage and duty cycle to output voltage transfer functions of non-ideal DC-DC buck and Cuk converter were obtained using state-space averaging technique and averaged switch model technique. The ESRs of inductors and capacitors, resistances of switch and diode, and diode forward voltage drop were involved in order to improve the dynamic and steady-state model of the converters. The state-space averaging and averaged switch model techniques both results in identical transfer functions. It was found that the non-ideal transfer functions have different steady-state and transient characteristics from the ideal transfer functions. The duty cycle to output voltage transfer function is generally used for control design. It was observed that the duty cycle to output voltage transfer function of the DC-DC Cuk converter is minimum phase system for the parameter values considered in this thesis; however, it is non-minimum phase system with the ideal parameter assumptions. Therefore, it is concluded that depending upon the values of non-ideal elements, it may be minimum phase or non-minimum phase.

However, in ideal case, it is always non-minimum phase because it always has zeros in right half plane. These improved transfer functions were used for the controller design of buck and Cuk converters. In the later part of modeling, the energy factor approaches were used to obtain the second-order model of non-ideal buck and Cuk converter. It was observed that the transfer function models are dependent on duty cycle and converter switching frequency.

3. In order to regulate the output voltage of buck and Cuk converter in different operating conditions, the various controllers were designed. The transfer function models obtained incorporating non-ideal elements of buck and Cuk converters were used. The PI, PI-lead and two-loop PI controller were designed for both the buck and Cuk converters. The stability boundary locus approach was used to tune PI controller. The simulation and experimental studies has shown that the PI controller is able to regulate the output voltage in different conditions but has larger overshoot and settling time. As the Cuk converter is a fourth-order system, therefore, its reduced second-order model was obtained using truncation method and PI controller was designed based on this reduced model. This PI controller was implemented on original Cuk converter and the converter performance was found almost similar. Further, a PI-lead controller was designed to improve the performance of these converters. To tune the parameters of this PI-lead controller based on desired phase margin and gain crossover frequency, an algorithm was proposed. The tuned parameters meet the phase margin and gain crossover frequency exactly. The settling time and overshoots are improved. However, if the PI-lead controller is designed to achieve the higher gain crossover frequency further, the noise appears in the output voltage as observed from the experimental results. Therefore, in order to achieve the increased bandwidth of the compensated converter system, a two-loop PI control scheme was implemented for buck and Cuk converter. In this scheme, outer voltage PI controller and inner current PI controller were used to regulate the output voltage. The parameters of these two PI controllers were designed using the proposed approach to achieve the desired phase margin and gain crossover frequency simultaneously. The simulation and experimental results were obtained to show the improved settling time and overshoots under different working conditions in comparison to PI and PI-lead controllers. The experimental results also confirm that the output voltage has no noise.

4. In the last part of the thesis, the sliding mode control technique for DC-DC Cuk converter was discussed. The correct analysis and derivation of various transfer functions were carried out in contrast to previously reported work in the literature. The controller parameters were tuned using a simple approach based on stability boundary locus approach. The simulation and experimental results have shown that the performance of the designed sliding mode control is almost similar to two-loop PI control. However, in the sliding mode control design only one PI controller is required to tune instead of two PI controllers in two-loop control

design. In sliding mode control, the PWM modulator is not required to generate the switching pulses.

6.2 Future scope

The research work presented in the thesis can further be extended. The some points related to possible future scope of the work are given below:

1. Though these design, modeling and control issues have been applied for DC-DC buck and Cuk converters in this thesis, but in a similar way with suitable modification, they may be implemented on other DC-DC converters.

2. As the small-signal averaged model does not reveal the effect of converter switching frequency on its dynamics. Therefore, the mathematical models of the DC-DC converters can be developed to include the effect of converter switching frequency on its dynamics.

3. In this thesis, the control techniques has been designed by considering the converter parameters constant. In future, these control techniques can be further developed by considering parameter variations in the converter.

4. These control design techniques can implemented in different applications such as battery operated electrical vehicles, photovoltaic systems, dc microgrid, *etc*.

Buck Converter:

The circuit diagram of DC-DC buck converter is shown in Fig. 3.25. The various steady-state current waveforms for buck converter are shown in Fig. A.1.

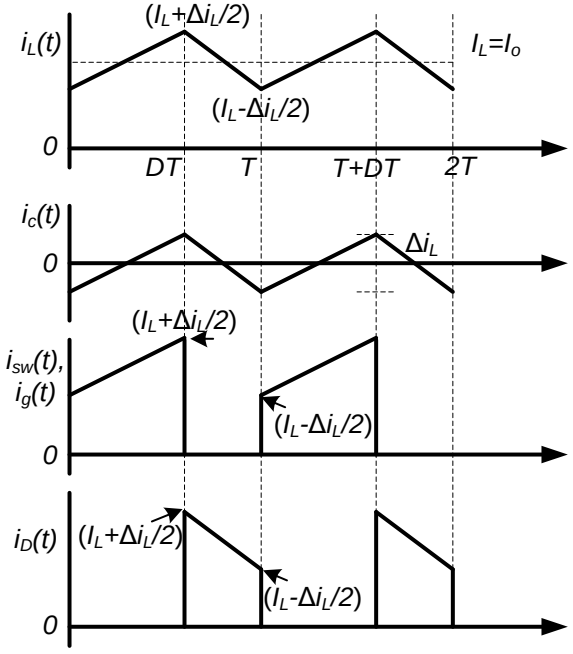


Fig. A.1. Various steady-state current waveforms for DC-DC buck converter (not to scale)

From these waveforms, the average and rms values of different current variables are calculated as follows [123], [124]:

The instantaneous value of inductor current is

$$i_L(t)=\begin{cases}\dfrac{\Delta i_L t}{DT}+\left(I_L-\dfrac{\Delta i_L}{2}\right) & \text{for } 0<t\le dT\\ -\dfrac{\Delta i_L\left(t-DT\right)}{D'T}+\left(I_L+\dfrac{\Delta i_L}{2}\right) & \text{for } dT<t\le T\end{cases} \tag{A.1}$$

The instantaneous value of the capacitor current is

$$i_c(t)=\begin{cases}\dfrac{\Delta i_L t}{DT}-\dfrac{\Delta i_L}{2} & \text{for } 0<t\le dT\\ -\dfrac{\Delta i_L\left(t-DT\right)}{D'T}+\dfrac{\Delta i_L}{2} & \text{for } dT<t\le T\end{cases} \tag{A.2}$$

The instantaneous value of switch current is

$$i_{sw}(t)=\begin{cases}\dfrac{\Delta i_L t}{DT}+\left(I_L-\dfrac{\Delta i_L}{2}\right) & \text{for } 0<t\le dT\\ 0 & \text{for } dT<t\le T\end{cases} \tag{A.3}$$

The instantaneous value of diode current is

$$i_D(t)=\begin{cases}0 & \text{for } 0<t\le dT\\ -\dfrac{\Delta i_L(t-DT)}{D'T}+\left(I_L+\dfrac{\Delta i_L}{2}\right) & \text{for } dT<t\le T\end{cases} \tag{A.4}$$

Where, $\Delta i_L = D'\dfrac{(r_d+r_L)I_L+V_F+V_o}{Lf}$ is peak-to-peak inductor current ripple.

The average input current or switch current is

$$I_g = I_{sw} = \frac{1}{T}\int_0^T i_{sw}(t)dt = \frac{1}{T}\int_0^{DT}\left[\frac{\Delta i_L t}{DT}+\left(I_L-\frac{\Delta i_L}{2}\right)\right]dt = DI_L \tag{A.5}$$

The average diode current is

$$I_D = \frac{1}{T}\int_0^T i_D(t)dt = \frac{1}{T}\int_0^{DT}\left[-\frac{\Delta i_L(t-DT)}{D'T}+\left(I_L+\frac{\Delta i_L}{2}\right)\right]dt = D'I_L \tag{A.6}$$

The average capacitor current is

$$I_c = \frac{1}{T}\int_0^T i_c(t)dt = \frac{1}{T}\int_0^{DT}\Delta i_L\left(\frac{t}{DT}-\frac{1}{2}\right)dt+\frac{1}{T}\int_{DT}^{T}\Delta i_L\left(-\frac{(t-DT)}{D'T}+\frac{1}{2}\right)dt = 0 \tag{A.7}$$

The rms value of switch current or input current will be

$$\begin{aligned} i_{g,rms} = i_{sw,rms} &= \sqrt{\frac{1}{T}\int_0^T i_{sw}^2(t)dt} = \sqrt{\frac{1}{T}\int_0^{DT}\left(\frac{\Delta i_L t}{DT}+\left(I_L-\frac{\Delta i_L}{2}\right)\right)^2 dt}\\ &= \sqrt{\frac{1}{T}\int_0^{DT}\left(\left(\frac{\Delta i_L}{DT}\right)^2 t^2+\frac{2\Delta i_L}{DT}\left(I_L-\frac{\Delta i_L}{2}\right)t+\left(I_L-\frac{\Delta i_L}{2}\right)^2\right)dt} = \sqrt{D\left(I_L^2+\frac{\Delta i_L^2}{12}\right)} \end{aligned} \tag{A.8}$$

The rms value of diode current will be

$$\begin{aligned} i_{D,rms} &= \sqrt{\frac{1}{T}\int_0^T i_D^2(t)dt} = \sqrt{\frac{1}{T}\int_{DT}^{T}\left(-\frac{\Delta i_L(t-DT)}{D'T}+\left(I_L+\frac{\Delta i_L}{2}\right)\right)^2 dt}\\ &= \sqrt{\frac{1}{T}\int_{DT}^{T}\left(\left(\frac{\Delta i_L}{D'T}\right)^2(t-DT)^2-\frac{2\Delta i_L}{D'T}\left(I_L+\frac{\Delta i_L}{2}\right)(t-DT)+\left(I_L+\frac{\Delta i_L}{2}\right)^2\right)dt} = \sqrt{D'\left(I_L^2+\frac{\Delta i_L^2}{12}\right)} \end{aligned} \tag{A.9}$$

Similarly, the rms value of capacitor current will be

$$i_{c,rms} = \sqrt{\frac{1}{T}\int_0^T i_c^2(t)dt} = \sqrt{\frac{1}{T}\int_0^{DT}\Delta i_L^2\left(\frac{t}{DT}-\frac{1}{2}\right)^2 dt+\frac{1}{T}\int_{DT}^{T}\Delta i_L^2\left(-\frac{(t-DT)}{D'T}+\frac{1}{2}\right)^2 dt} = \frac{\Delta i_L}{\sqrt{12}} \tag{A.10}$$

The rms value of inductor current will be

$$i_{L,rms} = \sqrt{\frac{1}{T}\int_0^T i_L^2(t)dt} = \sqrt{\frac{1}{T}\int_0^{DT}\left(\frac{\Delta i_L t}{DT}+\left(I_L-\frac{\Delta i_L}{2}\right)\right)^2 dt+\frac{1}{T}\int_{DT}^{T}\left(-\frac{\Delta i_L t}{D'T}+\left(I_L+\frac{\Delta i_L}{2}\right)\right)^2 dt} \tag{A.11}$$

The terms in this expression are similar to the expression of rms switch current and rms diode current, therefore, it is simplified directly as

$$i_{L,rms} = \sqrt{D\left(I_L^2 + \frac{\Delta i_L^2}{12}\right) + D'\left(I_L^2 + \frac{\Delta i_L^2}{12}\right)} = \sqrt{I_L^2 + \frac{\Delta i_L^2}{12}} \tag{A.12}$$

The power loss in different elements of non-ideal buck converter will be

$$P_L = P_{rL} + P_{rC} + P_{rSw} + P_{rD} + P_{VD} = r_L i_{L,rms}^2 + r_c i_{c,rms}^2 + r_{sw} i_{sw,rms}^2 + r_d i_{D,rms}^2 + V_F I_D \tag{A.13}$$

Substituting the respective values of currents, we get

$$\begin{aligned} P_L &= r_L\left(I_L^2 + \frac{\Delta i_L^2}{12}\right) + r_c\frac{\Delta i_L^2}{12} + r_{sw}D\left(I_L^2 + \frac{\Delta i_L^2}{12}\right) + r_D D'\left(I_L^2 + \frac{\Delta i_L^2}{12}\right) + V_F D' I_L \\ &= \left(r_L + Dr_{sw} + D'r_D + \frac{D'V_F}{I_L}\right) I_L^2 + \left(r_L + r_c + Dr_{sw} + D'r_D\right)\frac{\Delta i_L^2}{12} \\ &= \left[\left(r_L + Dr_{sw} + D'r_D + \frac{RD'V_F}{V_o}\right) + \left(r_L + r_c + Dr_{sw} + D'r_D\right)\frac{\Delta i_L^2}{12I_L^2}\right] I_L^2 = r_{loss} I_L^2 = r_{loss} I_o^2 \end{aligned} \tag{A.14}$$

Therefore,

$$r_{loss} = \left(r_L + Dr_{sw} + D'r_D + \frac{RD'V_F}{V_o}\right) + \left(r_L + r_c + Dr_{sw} + D'r_D\right)\frac{\Delta i_L^2}{12I_L^2} \tag{A.15}$$

Cuk Converter:

The circuit diagram of DC-DC Cuk converter is shown in Fig. 3.26. The various steady-state current waveforms for DC-DC Cuk converter is shown in Fig. A.2. From these waveforms, the average and rms values of different current variables are calculated as follows:

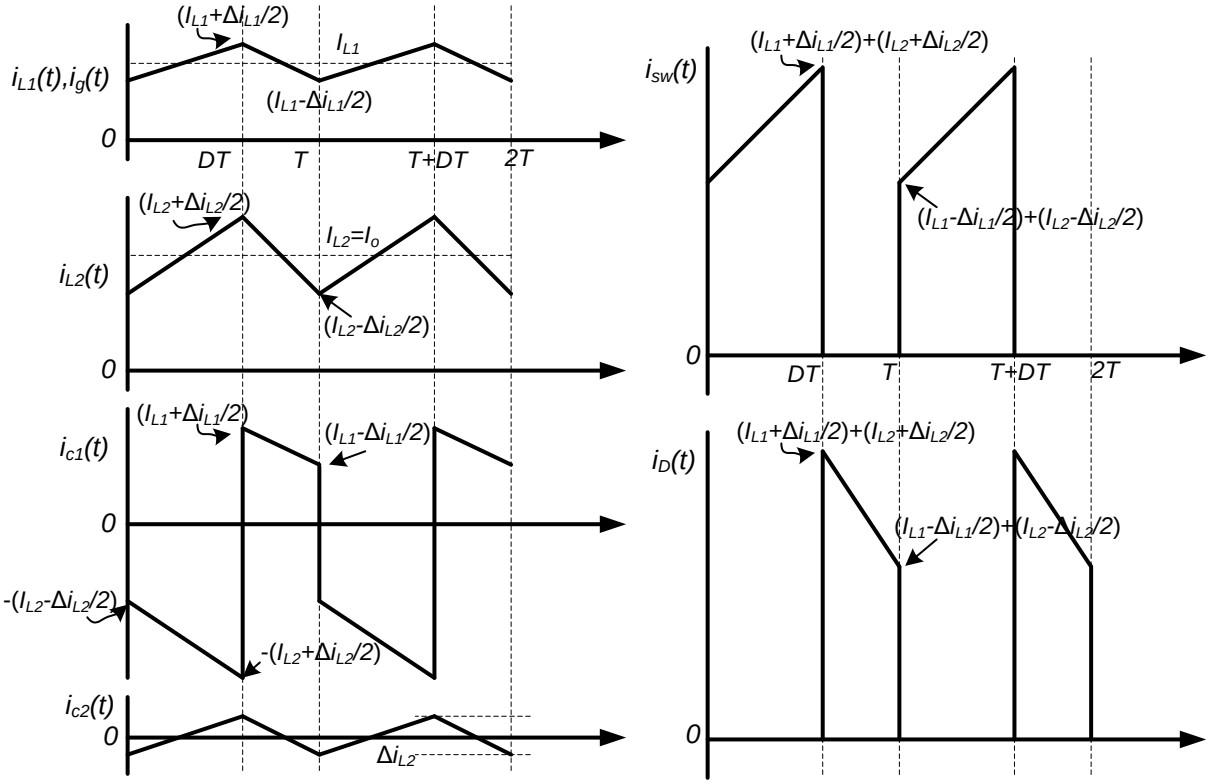


Fig. A.2. Various steady-state current waveforms for DC-DC Cuk converter (not to scale)

The instantaneous values of inductor currents are

$$i_g(t) = i_{L1}(t) = \begin{cases} \dfrac{\Delta i_{L1} t}{DT} + \left(I_{L1} - \dfrac{\Delta i_{L1}}{2} \right) & \text{for } 0 < t \le dT \\ -\dfrac{\Delta i_{L1}(t - DT)}{D'T} + \left(I_{L1} + \dfrac{\Delta i_{L1}}{2} \right) & \text{for } dT < t \le T \end{cases} \quad \text{(A.16)}$$

$$i_{L2}(t) = \begin{cases} \dfrac{\Delta i_{L2} t}{DT} + \left(I_{L2} - \dfrac{\Delta i_{L2}}{2} \right) & \text{for } 0 < t \le dT \\ -\dfrac{\Delta i_{L2}(t - DT)}{D'T} + \left(I_{L2} + \dfrac{\Delta i_{L2}}{2} \right) & \text{for } dT < t \le T \end{cases} \quad \text{(A.17)}$$

The instantaneous values of capacitor currents are

$$i_{c1}(t) = \begin{cases} -\dfrac{\Delta i_{L2} t}{DT} - \left(I_{L2} - \dfrac{\Delta i_{L2}}{2} \right) & \text{for } 0 < t \le dT \\ -\dfrac{\Delta i_{L1}(t - DT)}{D'T} + \left(I_{L1} + \dfrac{\Delta i_{L1}}{2} \right) & \text{for } dT < t \le T \end{cases} \quad \text{(A.18)}$$

$$i_{c2}(t) = \begin{cases} \dfrac{\Delta i_{L2} t}{DT} - \dfrac{\Delta i_{L2}}{2} & \text{for } 0 < t \le dT \\ -\dfrac{\Delta i_{L2}(t - DT)}{D'T} + \dfrac{\Delta i_{L2}}{2} & \text{for } dT < t \le T \end{cases} \quad \text{(A.19)}$$

The instantaneous value of switch current is

$$i_{sw}(t) = \begin{cases} \dfrac{(\Delta i_{L1} + \Delta i_{L2}) t}{DT} + \left(I_{L1} + I_{L2} - \dfrac{(\Delta i_{L1} + \Delta i_{L2})}{2} \right) & \text{for } 0 < t \le dT \\ 0 & \text{for } dT < t \le T \end{cases} \quad \text{(A.20)}$$

The instantaneous value of diode current is

$$i_D(t) = \begin{cases} 0 & \text{for } 0 < t \le dT \\ -\dfrac{(\Delta i_{L1} + \Delta i_{L2})(t - DT)}{D'T} + \left(I_{L1} + I_{L2} + \dfrac{(\Delta i_{L1} + \Delta i_{L2})}{2} \right) & \text{for } dT < t \le T \end{cases} \quad \text{(A.21)}$$

Where, $\Delta i_{L1} = \dfrac{D'V_o}{L_1 f}\left(1 + \dfrac{V_F}{V_o} + \dfrac{1}{R}\left(r_{L2} + \dfrac{D}{D'} r_{c1} + \dfrac{r_d}{D'}\right)\right)$ and $\Delta i_{L2} = \dfrac{D'V_o}{L_2 f}\left(1 + \dfrac{V_F}{V_o} + \dfrac{1}{R}\left(r_{L2} + \dfrac{r_d}{D'}\right)\right)$

are the peak-to-peak inductor current ripple for inductor L_1 and L_2 respectively.

It can be observed that these expressions are analogues to buck converter, therefore the average and rms values of different currents are computed in the similar fashion as below:

The average input current or inductor current (through L_1) is

$$I_g = I_{L1} = \frac{D}{D'} I_{L2} = \frac{D}{D'} I_o \quad \text{(A.22)}$$

Similarly, the average capacitor current (through C_1) is

$$I_{c1} = \frac{1}{T}\int_0^T i_{c1}(t)dt = \frac{1}{T}\int_0^{DT}\left[-\Delta i_{L2}\left(\frac{t}{DT} - \frac{1}{2}\right) - I_{L2}\right]dt + \frac{1}{T}\int_{DT}^{T}\Delta i_{L1}\left[\left(-\frac{(t - DT)}{D'T} + \frac{1}{2}\right) + I_{L1}\right]dt = 0 \quad \text{(A.23)}$$

The average capacitor current (through C_2) is

$$I_{c2} = \frac{1}{T}\int_0^T i_{c2}(t)dt = \frac{1}{T}\int_0^{DT} \Delta i_{L2}\left(\frac{t}{DT} - \frac{1}{2}\right)dt + \frac{1}{T}\int_{DT}^{T} \Delta i_{L2}\left(-\frac{(t-DT)}{D'T} + \frac{1}{2}\right)dt$$
$$= \frac{1}{T}\left[\Delta i_{L2}\left(\frac{1}{DT}\frac{(DT)^2}{2} - \frac{DT}{2}\right) + \Delta i_{L2}\left(-\frac{1}{D'T}\frac{(D'T)^2}{2} + \frac{D'T}{2}\right)\right] = 0 \quad \text{(A.24)}$$

The average switch current is

$$I_{sw} = \frac{1}{T}\int_0^T i_{sw}(t)dt = \frac{1}{T}\int_0^{DT}\left[\frac{(\Delta i_{L1} + \Delta i_{L2})t}{DT} + \left(I_{L1} + I_{L2} - \frac{(\Delta i_{L1} + \Delta i_{L2})}{2}\right)\right]dt$$
$$= \frac{1}{T}\left[\frac{(\Delta i_{L1} + \Delta i_{L2})}{DT}\frac{(DT)^2}{2} + \left(I_{L1} + I_{L2} - \frac{(\Delta i_{L1} + \Delta i_{L2})}{2}\right)DT\right] = D(I_{L1} + I_{L2}) = \frac{D}{D'}I_o \quad \text{(A.25)}$$

The average diode current is

$$I_D = \frac{1}{T}\int_0^T i_D(t)dt = \frac{1}{T}\int_0^{DT}\left[-\frac{(\Delta i_{L1} + \Delta i_{L2})(t-DT)}{D'T} + \left(I_{L1} + I_{L2} + \frac{(\Delta i_{L1} + \Delta i_{L2})}{2}\right)\right]dt$$
$$= \frac{1}{T}\left[-\frac{(\Delta i_{L1} + \Delta i_{L2})}{D'T}\frac{(D'T)^2}{2} + \left(I_{L1} + I_{L2} + \frac{(\Delta i_{L1} + \Delta i_{L2})}{2}\right)D'T\right] = D'(I_{L1} + I_{L2}) = I_o \quad \text{(A.26)}$$

The rms value of inductor current (through L_1) or input current will be

$$i_{g,rms} = i_{L1,rms} = \sqrt{\frac{1}{T}\int_0^T i_{L1}^2(t)dt} = \sqrt{\frac{1}{T}\int_0^{DT}\left[\frac{\Delta i_{L1}t}{DT} + \left(I_{L1} - \frac{\Delta i_{L1}}{2}\right)\right]^2 dt + \frac{1}{T}\int_{DT}^{T}\left[-\frac{\Delta i_{L1}(t-DT)}{D'T} + \left(I_{L1} + \frac{\Delta i_{L1}}{2}\right)\right]^2 dt}$$
$$= \sqrt{\frac{1}{T}\left(DT\left(I_{L1}^2 + \frac{\Delta i_{L1}^2}{12}\right)\right) + \frac{1}{T}\left(D'T\left(I_{L1}^2 + \frac{\Delta i_{L1}^2}{12}\right)\right)} = \sqrt{I_{L1}^2 + \frac{\Delta i_{L1}^2}{12}}$$

Substituting $I_{L1} = \frac{D}{D'}I_{L2} = \frac{D}{D'}I_o$ in the above equation

$$i_{g,rms} = i_{L1,rms} = I_o\sqrt{\frac{D^2}{D'^2} + \frac{\Delta i_{L1}^2}{12I_o^2}} \quad \text{(A.27)}$$

The rms value of inductor current (through L_2) will be

$$i_{L2,rms} = \sqrt{\frac{1}{T}\int_0^T i_{L2}^2(t)dt} = \sqrt{\frac{1}{T}\int_0^{DT}\left[\frac{\Delta i_{L2}t}{DT} + \left(I_{L2} - \frac{\Delta i_{L2}}{2}\right)\right]^2 dt + \frac{1}{T}\int_{DT}^{T}\left[-\frac{\Delta i_{L2}(t-DT)}{D'T} + \left(I_{L2} + \frac{\Delta i_{L2}}{2}\right)\right]^2 dt} \quad \text{(A.28)}$$
$$= \sqrt{I_{L2}^2 + \frac{\Delta i_{L2}^2}{12}} = \sqrt{I_o^2 + \frac{\Delta i_{L2}^2}{12}} = I_o\sqrt{1 + \frac{\Delta i_{L2}^2}{12I_o^2}}$$

The rms value of the capacitor current (through C_1) will be

$$i_{c1,rms} = \sqrt{\frac{1}{T}\int_0^T i_{c1}^2(t)dt} = \sqrt{\frac{1}{T}\int_0^{DT}\left[-\frac{\Delta i_{L2}t}{DT} - \left(I_{L2} - \frac{\Delta i_{L2}}{2}\right)\right]^2 dt + \frac{1}{T}\int_{DT}^{T}\left[-\frac{\Delta i_{L1}(t-DT)}{D'T} + \left(I_{L1} + \frac{\Delta i_{L1}}{2}\right)\right]^2 dt} \quad \text{(A.29)}$$
$$= \sqrt{D\left(I_{L2}^2 + \frac{\Delta i_{L2}^2}{12}\right) + D'\left(I_{L1}^2 + \frac{\Delta i_{L1}^2}{12}\right)} = \sqrt{\frac{D}{D'}I_o^2 + \frac{1}{12}\left(D\Delta i_{L2}^2 + D'\Delta i_{L1}^2\right)} = I_o\sqrt{\frac{D}{D'} + \frac{1}{12I_o^2}\left(D\Delta i_{L2}^2 + D'\Delta i_{L1}^2\right)}$$

The rms value of the capacitor current (through C_2) will be

$$i_{c2,rms} = \sqrt{\frac{1}{T}\int_0^T i_{c2}^2(t)dt} = \sqrt{\frac{1}{T}\int_0^{DT} \Delta i_{L2}^2\left(\frac{t}{DT}-\frac{1}{2}\right)^2 dt + \frac{1}{T}\int_{DT}^{T} \Delta i_{L2}^2\left(-\frac{(t-DT)}{D'T}+\frac{1}{2}\right)^2 dt}$$
$$= \sqrt{\frac{1}{T}\left[\Delta i_{L2}^2\left(\frac{DT}{3}-\frac{DT}{2}+\frac{DT}{4}\right)\right] + \frac{1}{T}\left[\Delta i_{L2}^2\left(\frac{D'T}{3}-\frac{D'T}{2}+\frac{D'T}{4}\right)\right]} = \frac{\Delta i_{L2}}{\sqrt{12}} \quad \text{(A.30)}$$

The rms value of the switch current will be

$$i_{sw,rms} = \sqrt{\frac{1}{T}\int_0^T i_{sw}^2(t)dt} = \sqrt{\frac{1}{T}\int_0^{DT}\left(\frac{(\Delta i_{L1}+\Delta i_{L2})t}{DT} + \left(I_{L1}+I_{L2}-\frac{(\Delta i_{L1}+\Delta i_{L2})}{2}\right)\right)^2 dt}$$
$$= \sqrt{D\left((I_{L1}+I_{L2})^2 + \frac{(\Delta i_{L1}+\Delta i_{L2})^2}{12}\right)} = I_o\sqrt{\frac{D}{D'^2}+\frac{D(\Delta i_{L1}+\Delta i_{L2})^2}{12I_o^2}} \quad \text{(A.31)}$$

The rms value of diode current will be

$$i_{D,rms} = \sqrt{\frac{1}{T}\int_0^T i_D^2(t)dt} = \sqrt{\frac{1}{T}\int_{DT}^{T}\left(-\frac{(\Delta i_{L1}+\Delta i_{L2})(t-DT)}{D'T} + \left(I_{L1}+I_{L2}+\frac{(\Delta i_{L1}+\Delta i_{L2})}{2}\right)\right)^2 dt}$$
$$= \sqrt{D'\left((I_{L1}+I_{L2})^2 + \frac{(\Delta i_{L1}+\Delta i_{L2})^2}{12}\right)} = I_o\sqrt{\frac{1}{D'}+\frac{D'(\Delta i_{L1}+\Delta i_{L2})^2}{12I_o^2}} \quad \text{(A.32)}$$

Therefore, the power loss in different elements of non-ideal Cuk converter will be

$$P_L = P_{rL1}+P_{rL2}+P_{rC1}+P_{rC2}+P_{rSw}+P_{rD}+P_{VD}$$
$$= r_{L1}i_{L1,rms}^2 + r_{L2}i_{L2,rms}^2 + r_{c1}i_{c1,rms}^2 + r_{c2}i_{c2,rms}^2 + r_{sw}i_{sw,rms}^2 + r_d i_{D,rms}^2 + V_F I_D \quad \text{(A.33)}$$

Substituting respective values of currents, we get

$$P_L = r_{L1}I_o^2\left(\frac{D^2}{D'^2}+\frac{\Delta i_{L1}^2}{12I_o^2}\right) + r_{L2}I_o^2\left(1+\frac{\Delta i_{L2}^2}{12I_o^2}\right) + r_{c1}I_o^2\left(\frac{D}{D'}+\frac{1}{12I_o^2}\left(D\Delta i_{L2}^2 + D'\Delta i_{L1}^2\right)\right)$$
$$+ r_{c2}\frac{\Delta i_{L2}^2}{12} + Dr_{sw}I_o^2\left(\frac{1}{D'^2}+\frac{(\Delta i_{L1}+\Delta i_{L2})^2}{12I_o^2}\right) + D'r_D I_o^2\left(\frac{1}{D'^2}+\frac{(\Delta i_{L1}+\Delta i_{L2})^2}{12I_o^2}\right) + V_F I_o \quad \text{(A.34)}$$
$$= I_o^2\left[\begin{array}{l}\left(\frac{D^2}{D'^2}r_{L1}+r_{L2}+\frac{D}{D'}r_{c1}+\frac{Dr_{sw}+D'r_D}{D'^2}+\frac{RV_F}{V_o}\right)+\left(r_{L1}+D'r_{c1}\right)\frac{\Delta i_{L1}^2}{12I_o^2}+ \\ \left(r_{L2}+Dr_{c1}+r_{c2}\right)\frac{\Delta i_{L2}^2}{12I_o^2}+\left(Dr_{sw}+D'r_D\right)\frac{(\Delta i_{L1}+\Delta i_{L2})^2}{12I_o^2}\end{array}\right] = r_{loss}I_o^2$$

Therefore,

$$r_{loss} = \left(\frac{D^2 r_{L1}}{D'^2}+r_{L2}+\frac{Dr_{c1}}{D'}+\frac{Dr_{sw}+D'r_D}{D'^2}+\frac{RV_F}{V_o}\right)+\left(r_{L1}+D'r_{c1}\right)\frac{\Delta i_{L1}^2}{12I_o^2}+$$
$$\left(r_{L2}+Dr_{c1}+r_{c2}\right)\frac{\Delta i_{L2}^2}{12I_o^2}+\left(Dr_{sw}+D'r_D\right)\frac{(\Delta i_{L1}+\Delta i_{L2})^2}{12I_o^2} \quad \text{(A.35)}$$

APPENDIX – B

[In this appendix, a brief documentation about the important building blocks of the experimental setup is presented.]

In this thesis, various controller design techniques have been discussed to regulate the output voltage of DC-DC buck and Cuk converter under different operating conditions. The simulation results of these converters with the designed control techniques are obtained using MATLAB/Simulink software. However, to validate these simulation results for a practical (or physical) DC-DC converter, an experimental setup is necessary. For this purpose, a prototype of DC-DC buck and Cuk converter is developed. The control algorithm can be implemented in various ways. One approach is to use analog controllers, which make use of different components such as operational amplifiers ICs, resistances, and capacitors. Although analog controllers have no constraints on sampling time or switching frequency, the practical development of these compensator circuits is not so easy [195]. It is comparatively difficult to set the exact values of the controller gains using the analog controllers. The other approach is to use digital controllers. In this thesis, the different control techniques are implemented using dSPACE DS1104 digital simulator interfaced with MATLAB/Simulink to observe the performance of DC-DC converters [196], [197].

A generalized block diagram of the experimental set-up for dSPACE based closed-loop controlled DC-DC converter is given in Fig. B.1. This block diagram shows the generalized way for real-time implementation of a control technique on DC-DC converter prototype using dSPACE DS1104 digital controller board [196]. The dSAPCE system includes a slave I/O subsystem based on TMS320F240 DSP processor. Depending upon the designed control technique, the output voltage and/or inductor current are sensed using voltage and/or current sensors. These sensed voltage and/or current signals are fed as input to analog-to digital converter (ADC) channels on dSPACE connector panel. The proposed controller is modeled in the MATLAB/Simulink environment and is converted into the optimized C-code using Real-Time Workshop (RTW) function of MATLAB. Then, this code is compiled by a compiler and finally dumped to DSP processor, which generates the required switching gate pulses by using the and Real-Time Interface (RTI) features of dSPACE DS1104. These desired gate pulses are obtained at I/O bits of dSPACE controller board and then, fed to MOSFET driver circuit for amplification and isolation purpose. The isolated and amplified gate pulses are connected to the MOSFET switch of DC-DC converter prototype. The any effect of variation in operating conditions on output voltage is sensed and the suitable gate pulses are generated in real-time.

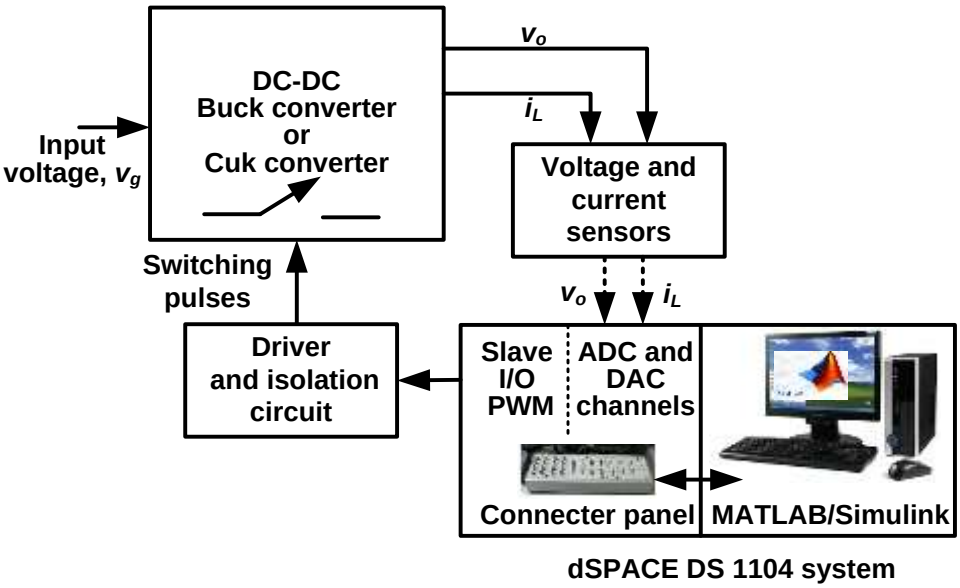


Fig. B.1. Generalized block diagram representation of experimental setup

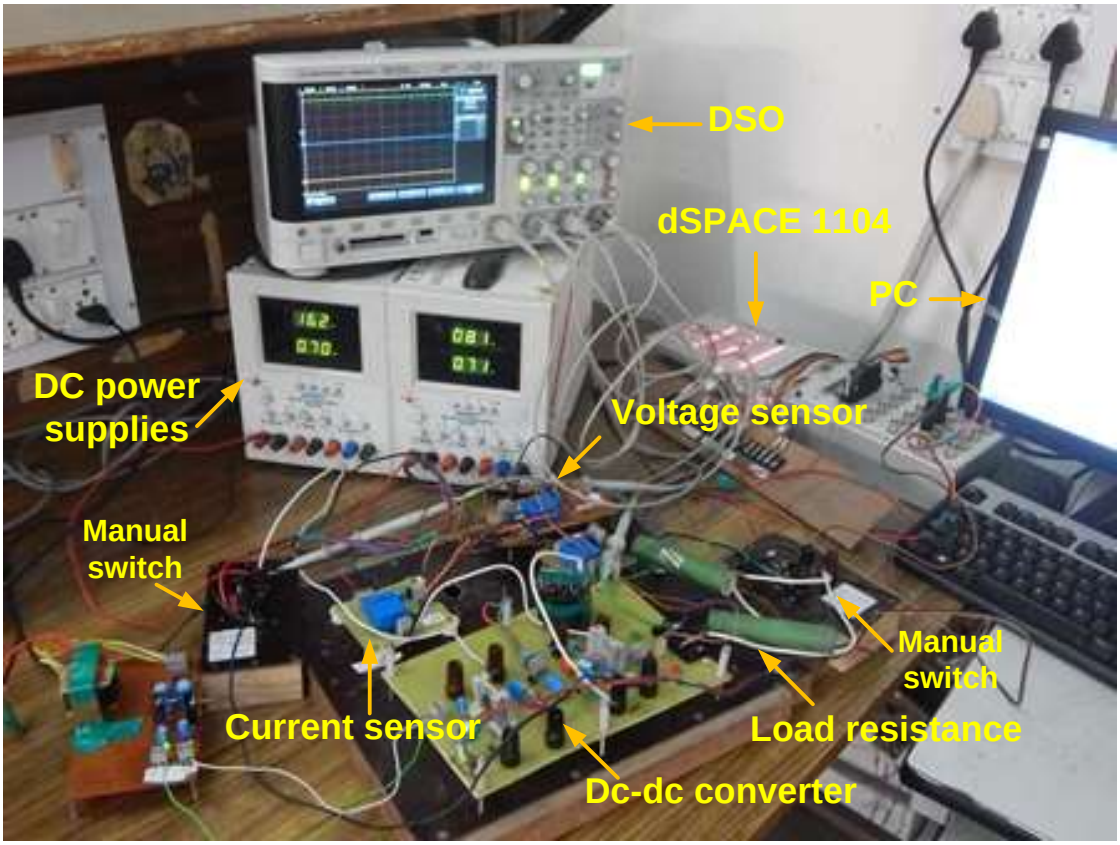


Fig. B.2. Laboratory experimental setup

The experimental setup developed in the laboratory is shown in Fig. B.2. This experimental setup consists of following components.

1. Prototypes of buck converter and Cuk converter

2. Signal measurement circuits (voltage sensor and current sensor)

3. Controller implementation using dSPACE system

4. Driver and isolation circuits

5. DC Power supplies: Scientific make power supplies with the rating (±15 V/1 A, 15 V/1 A) and (Dual output 30 V/3 A) are used. The power supply with the rating (±15 V/1 A, 15 V/1 A) is used for driver circuit, current sensor and voltage sensors. The power supply with rating (Dual output 30 V/3 A) is used as the main input power supply for DC-DC converters.

6. Digital storage oscilloscope (DSO): Agilent make DSO X-2014A (100 MHz) is used for capturing the different current and voltage waveforms of buck and Cuk converter.

1. Prototypes of buck converter and Cuk converter

A DC-DC buck and Cuk converter prototype have been developed in the laboratory. The circuit diagram for these converters is same as discussed in chapter 4. The practical values of different parameters of buck and Cuk converter are same as used for MATLAB/Simulink simulation in chapters 4 and 5. In fact, the measured values of physical inductor(s), capacitor(s) and their series resistances are used for simulation. The ferrite core inductors are designed to minimize the core loss at high switching frequencies. The electrolytic aluminium capacitors are used. The metal oxide semiconductor field effect transistor (MOSFET) switch IRF540 and Schottky diode MUR1560 are used as semiconductor devices. A suitable snubber circuit is designed to protect the switching device. The MOSFET and diode are placed on heat sinks to ensure proper heat dissipation.

The connection diagram to realize the step variation in input voltage and load resistance is shown in Fig. B.3. As shown in Fig. B.3(a), two DC input voltage supply is connected with the help of single pole double throw (SPDT) switch. When common terminal '*c*' is connected to terminal '*1*', the total DC input voltage applied to the converter is (V_{g1} + V_{g2}) and when connected to 2, the total DC input voltage applied to the converter is V_{g1}. For buck converter, the step variation in input voltage is considered 16 V to 24 V and vice-versa, thereby setting V_{g1}=16 V and V_{g2}=8 V. For the Cuk converter, the step variation in input voltage is taken 20 V to 28 V and vice-versa, thereby setting V_{g1}=20 V and V_{g2}=8 V. It is worthwhile to mention that during the transition from one input voltage to another, the manual switch takes some time (few milliseconds). During this transition, the terminal '*c'* will not be connected to any terminal either '1' or '2' and therefore, the net input voltage tries to fall. As soon as the contact is made between two terminals, the input voltage will set to respective value. Therefore, for experimental results, there is a possibility that the exact step change in input voltage may not be realized. There may be some dip before reaching to a new value. However, one may use programmable power supplies available in market to realize the exact step variation in input voltage.

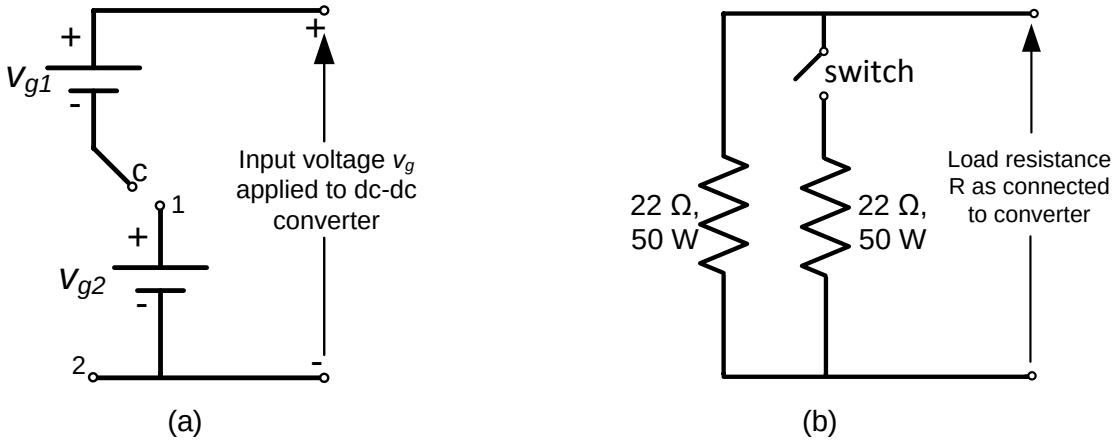


Fig. B.3. Connection diagram for step variation of (a) input voltage (b) load resistance

Similarly, to realize the step variation in the load resistance, the connection diagram is shown in Fig. B.3(b). In buck and Cuk converters, the step variation in load resistance is 22 Ω to 11 Ω and vice-versa. For this purpose, two 22 Ω resistances are connected in parallel via a manual switch. When this switch is off, the net load resistance is 22 Ω and when this switch is on, the net load resistance connected to converter is 11 Ω.

2. Signal measurement circuits (voltage sensor and current sensor)

For precise and reliable closed-loop control, the actual output voltage and inductor current are required to sense in implementation of different control techniques for DC-DC buck converter and Cuk converter. The Hall-effect voltage and current transducers are used for this purpose. These Hall-effect transducers also provide galvanic isolation between power circuit (primary circuit) and control circuit (secondary circuit). Any hall-effect voltage and current sensors can be used for this purpose. However, in the experimental work of this thesis, LEM make LV 20-P voltage transducers and LA 25-NP current transducers are used. These transducers convert high-level analog signals into low-level analog signals.

Voltage sensor circuit

The actual output voltage of buck and Cuk converter is compared with the reference output voltage to generate output voltage error. The voltage level of the actual output voltage is scaled down to be within the specified range before connecting to ADC channels of dSPACE. The analog signal connected to these ADC channels should be within ±10V range. The connection diagram of a Hall-effect voltage sensor circuit is shown in Fig. B.4.

According to the data sheet of this voltage transducer [198], the input side resistance R_1 should be selected such that the maximum value of input current be ±10 mA and output side resistance R_2 lies between 100 Ω- 350 Ω.

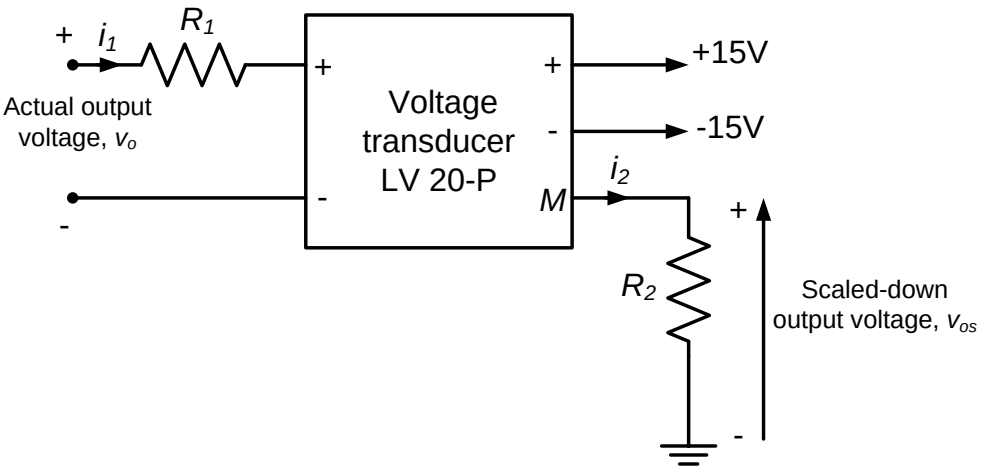


Fig. B.4. Connection diagram of voltage sensor circuit

Considering that the actual output voltage (v_o) of DC-DC buck and Cuk converter to be measured is 20 V and it is downscaled to 5 V. The value of input resistance R_1 is selected 2.2 kΩ Therefore, the input current i_1 is calculated as-

$$i_1 = \frac{v_o}{R_1} = \frac{20}{2.2\times10^3} = 9.09\,mA \tag{B.1}$$

The conversion ratio (K_v) of this voltage transducer is 2500:1000. Therefore, the output current i_2 will be-

$$i_2 = K_v i_1 = 2.5\times\frac{20}{2.2\times10^3} = \frac{1}{44}A = 22.72\,mA \tag{B.2}$$

The output resistance R_2 is chosen in such a way that the down scaled output voltage (v_{os}) is 5 V. So, we get

$$R_2 = \frac{v_{os}}{i_2} = 5\times44 = 220\,\Omega \tag{B.3}$$

Thus, the value of the R_1=2.2 kΩ and R_2=220 Ω is selected.
The down scale factor for these values is

$$K_{dsf} = \frac{v_{os}}{v_o} = \frac{1}{4} \tag{B.4}$$

This sensed output voltage (v_{os}) is fed to ADC channels of dSPACE. In the MATLAB/Simulink environment, the output of the corresponding ADC channel is multiplied by a factor of $1/K_{dsf}$ (=4 in this case) to get the actual output voltage for comparison with the reference voltage.

Current sensor circuit

The actual inductor current is compared with the reference inductor current in two-loop control and sliding mode control. The actual inductor current is sensed and scaled down before feeding to ADC channels of the dSPACE system. The analog signal connected to

these ADC channels should be within ±10 V range. The connection diagram of a Hall-effect current sensor circuit is shown in Fig. B.5.

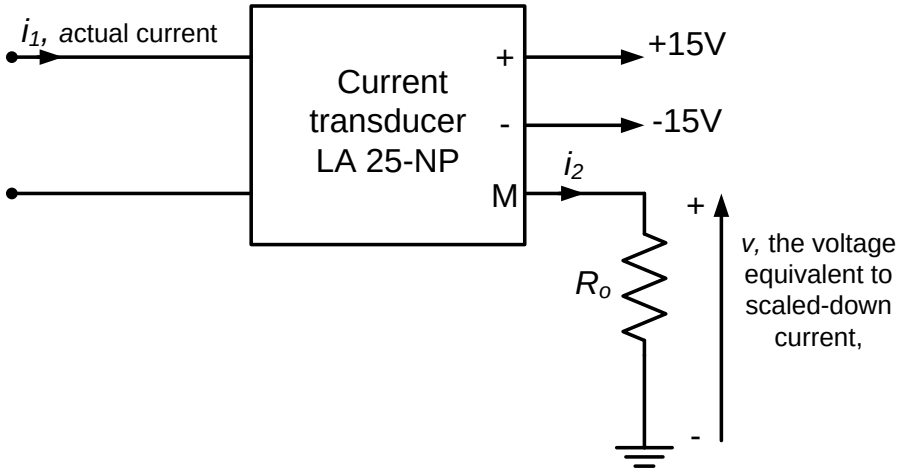


Fig. B.5. Connection diagram of current sensor circuit

According to the data sheet of this current transducer [199], the different number of primary turns can be selected depending upon the nominal value of measured primary current. The value of resistance R_o should lie between 100 Ω to 320 Ω.

Considering that the actual inductor current (i_1) of DC-DC buck and Cuk converter to be measured is 5 A. For this nominal value, the primary number of turns is 5 as specified in the data sheet. The corresponding conversion ratio (K_i) is 5/1000. Therefore, the downscaled secondary side current will be

$$i_2 = K_i i_1 = \frac{5}{1000} \times 5 = 25\,mA \tag{B.5}$$

The output resistance R_o is selected in such a way that the output of current transducer is 5 V equivalent to actual primary current of 5 A. Therefore,

$$R_o = \frac{v}{i_2} = \frac{5}{25 \times 10^{-3}} = 200\,\Omega \tag{B.6}$$

This resistance has been calculated such that the input current of 5 A is converted to an equivalent voltage of 5 V. Therefore, the current to voltage conversion factor will be unity. In the MATLAB/Simulink environment, the output of the corresponding ADC channel is directly used as the actual current to compare with the reference current.

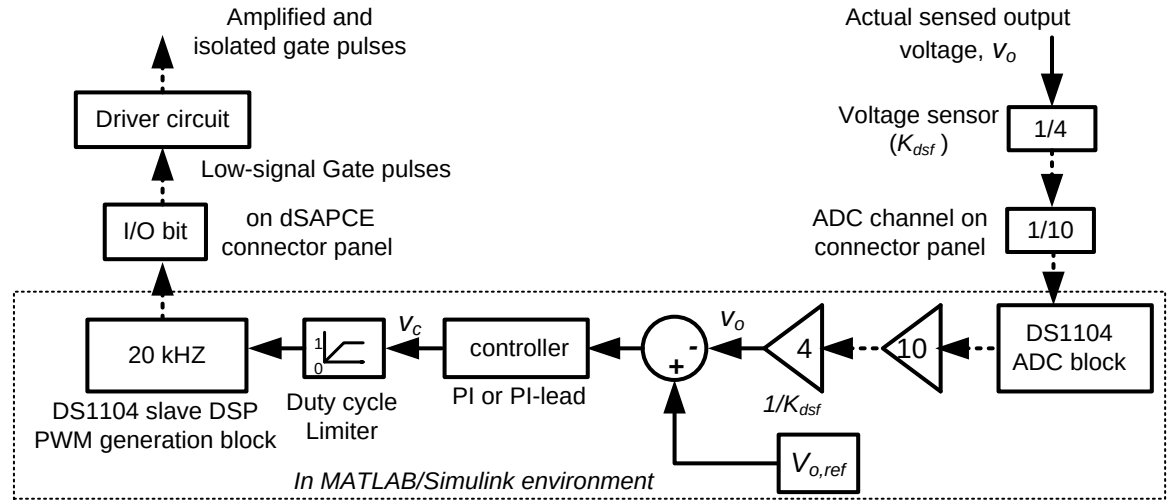
3. Controller implementation using dSPACE system

In this thesis, the different control techniques have been implemented using dSPACE DS1104 controller board. The DSP DS1104 R&D controller board of dSPACE is a standard board that can be plugged into Peripheral Component Interconnect (PCI) slot of a desktop computer [196]. The DS1104 is specially designed for the development of high-speed multivariable digital controllers and real-time simulations for various applications. It is a complete real-time control system based on 603 PowerPC floating-point processor running at

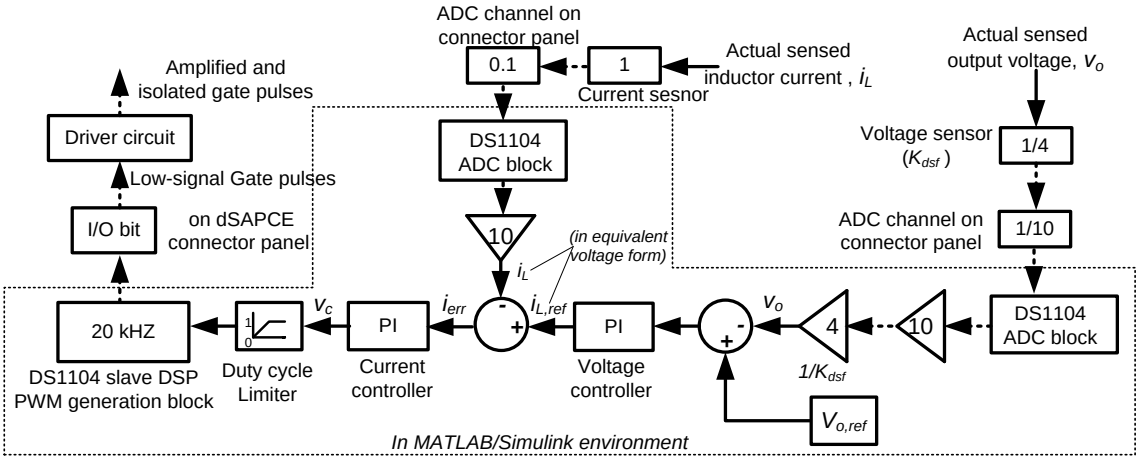
250 MHz. For advance I/O purposes, the board includes a slave-DSP subsystem based on the TMS320F240 DSP microcontroller. For purposes of rapid control prototyping (RCP), the specific interface connectors and connector panels are provided which gives easy access to all input and output signals of the board. Therefore, DS1104 R&D controller is a very good platform for the development of the dSPACE prototype system for cost-sensitive RCP applications. It is used for the real-time implementation of the control algorithm with hardware-in-loop.

The typical implementation of the different control techniques using the dSAPCE controller board is shown in Fig. B.6. The control techniques used in this thesis a: single loop control (PI controller and PI-lead controller), two-loop PI control and Sliding-mode control. The dSPACE implementation of these techniques remains same for DC-DC buck and Cuk converters. Therefore, only general explanation is given. Fig. B.6(a) shows the implementation of the PI or PI-lead control technique. The actual output voltage (v_o) of the converter prototype is sensed using voltage sensor. This actual output voltage (v_o) is scaled by a factor of ¼ by the voltage sensor gain. This scaled output voltage is connected to ADC channels at the connector panel. The output voltage is again divided by 10 automatically before connecting it to DS1104 ADC block in MATLAB environment. To get the actual sensed output voltage v_o in the MATLAB environment, the output of ADC block is multiplied by factors 10 and 4 (inverse of voltage sensor gain). Then, this voltage v_o is compared with the reference output voltage $v_{o,ref}$. The error is processed via designed controller (PI or PI-lead) which gives a control voltage v_c. A duty cycle limiter block is used to limit the duty cycle to 1. The output of the limiter is fed to a PWM generation block. The PWM block generates a sawtooth waveform of 20 kHz and compares it with the control voltage to produce the switching pulses of the required duty cycle. These switching pulses can be obtained on I/O pins at the dSPACE connector panel. The switching pulses generated by dSPACE are amplified and isolated using the MOSFET driver circuit and finally fed to MOSFET switch of the converter.

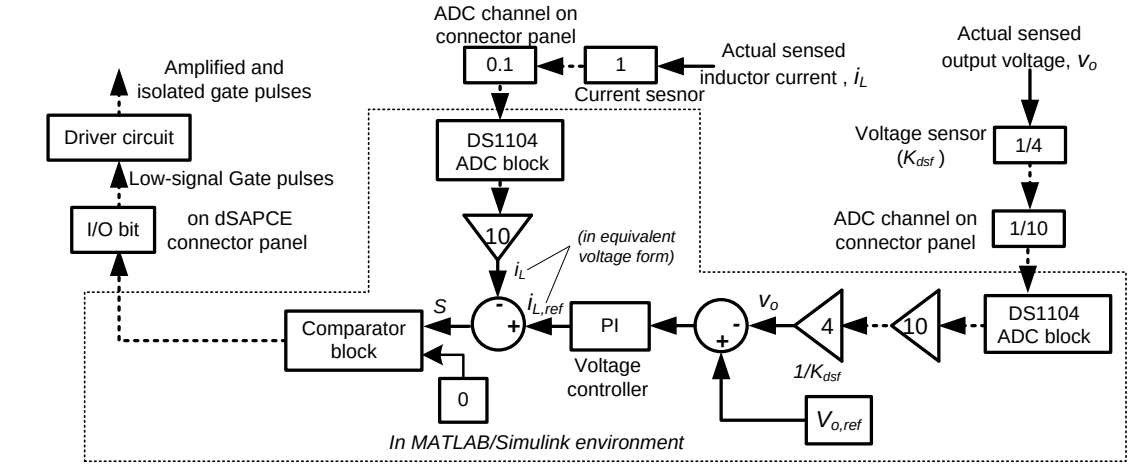
The dSAPCE implementation of the two-loop PI control scheme is shown in Fig. B.6(b) . In two-loop PI control, in addition to output voltage (v_o), the inductor current (i_L) is also sensed and feedback to dSPACE controller board. The gain of the current sensor set to be one, therefore, there is only one multiplier (10) is required in the MATLAB model. The outer voltage PI controller generates the reference inductor current ($i_{L,ref}$) for the inner current loop control. The actual current (i_L) is compared with the reference inductor current ($i_{L,ref}$) to generate the current error (i_{err}), which processed in the inner current PI controller to generate the control voltage v_c. The remaining process is similar to single loop control.



(a)



(b)



(c)

Fig. B.6. Implementation of the different control techniques using dSPACE DS1104 controller system (a) PI or PI-lead control (b) Two-loop PI control (c) Sliding mode control

The dSAPCE implementation of the sliding mode control scheme (Fig. B.6(c)) is similar to two-loop PI control. The only difference lies in the pulse generation in MATLAB

environment. In the sliding mode control, the current error was chosen as sliding surface. This current error is compared in a comparator with zero, which directly generates the desired switching pulses depending upon the current error. If current error is positive, the comparator output is high otherwise it is low. There is no need to use PWM generation block.

4. Driver and isolation circuits

The gate pulses for MOSFET switching device of DC-DC buck and Cuk converters are generated using the dSPACE system. The voltage magnitude of these gate pulses is not sufficient to drive the MOSFET switch. Moreover, these switching pulses cannot directly be applied to the MOSFET switch because the MOSFET switch is part of the power circuit, whereas the switching pulses are part of the control circuit. An electrical isolation is necessary between the power circuit and the control circuit in order to prevent any damage or malfunctioning of the system. Therefore, a high-speed optocoupler integrated circuit (IC) TLP250 is used as MOSFET gate driver and for isolation purpose. In TLP250, the input and output are optically isolated. The input stage has a light emitting diode (LED) and the output stage has an integrated photodetector [200]. The complete circuit of MOSFET driver circuit using TLP250 is shown in Fig. B.7.

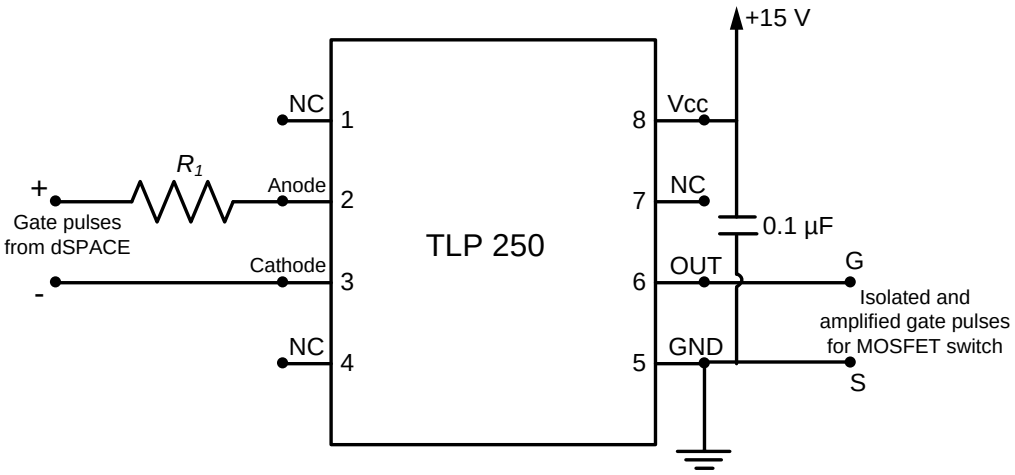


Fig. B.7. MOSFET driver circuit

As shown in the figure, the low amplitude gate pulses generated by the dSAPCE system are connected between pin number 2 and 3 of TLP250 by a resistance R_1. The isolated power supply (V_{cc}) of 15 V is connected between pin number 8 and 5. The pin number 1,4 and 7 are not connected (NC) anywhere. The isolated and amplified gate pulses of magnitude slighter less than V_{cc} are obtained between pin number 6 and 5, which is connected to the MOSFET switch of the power converter. A 0.1 µF bypass capacitor is connected between pin number 8 and 5. This capacitor should be placed as close to the TLP250 as possible [200]. The detailed schematic diagram and functioning of TLP250 is

given in its datasheet. The typical input and output switching gate pulses of the driver circuit (for 60% duty cycle and 20 kHz switching frequency) are shown in Fig. B.8.

Calculation of resistance R_1

The datasheet informs that a light emitting diode (LED) is connected between pin number 2 and 3. In order to limit the current through this LED, this resistance R_1 is used. The typical values of parameters are taken from IC datasheet as below:

Input forward current (I_F) = 10 mA

Input forward voltage (V_F) = 1.6 V

Amplitude of the switching pulses obtained from dSAPCE is 5 V. Therefore, the value of resistance R_1 is computed as

$$R_1 = \frac{5 - 1.6}{10 \times 10^{-3}} = 340\,\Omega \tag{B.7}$$

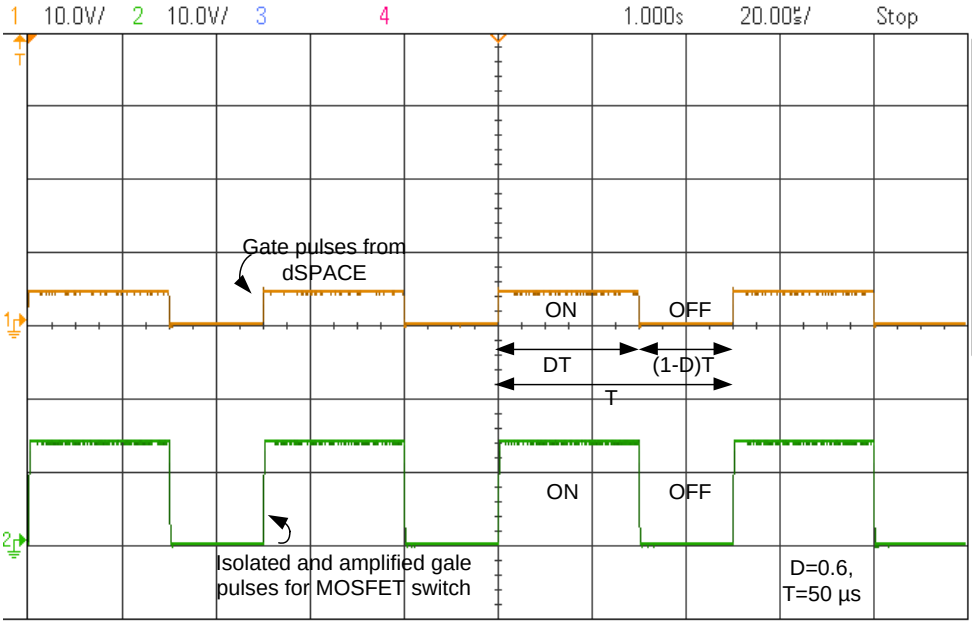


Fig. B.8. Input and output switching gate pulses from the MOSFET driver circuit

PUBLICATIONS FROM THE WORK

International Journals (SCI/SCIE)

1. **M.M. Garg,** Y.V. Hote, and M.K. Pathak, "Notes on Small Signal Analysis of Energy Factor and Mathematical Modeling for Power DC-DC Converters," **IEEE Trans. Power Electronics**, vol. 29, no. 7, pp. 3848, 2014.
2. **M.M. Garg**, M.K. Pathak and Y.V. Hote, "Impact of Non-idealities on Design and Performance of DC-DC Buck Converter," **Journal of Power Electronics**, 2015 (***In press***, **SCIE**)
3. **M.M. Garg**, Y.V. Hote and M.K. Pathak, "Design and Performance Analysis of a PWM DC-DC Buck Converter using PI-Lead Compensator," Arabian Journal of Science and Engineering, **Springer**, vol. 40, no. 12, pp. 3607-3626, 2015, (**SCIE**)
4. **M.M. Garg**, M.K. Pathak and Y.V. Hote, "Analysis and Design of Non-ideal DC-DC Cuk Converter," **IET Circuits, Devices and Systems**, 2016 (***Accepted,* SCI**)
5. **M.M. Garg** and Y.V. Hote, "Leverrier Algorithm based Reduced Order Modeling of DC-DC Converters," **IEEE Transactions on Industry Applications** (***Under submission process***) (*This research paper was recommended to submit for further review and possible publication in this journal by the committee of* IEEE *6th India International Conference on Power Electronics, IICPE-2014)*
6. **M.M. Garg**, Y.V. Hote and M.K. Pathak, "Design of two-loop PI controller for DC-DC buck converter," International Journal of Electronics, Taylor and Fransis (***Under submission process***)

International conferences

1. **M.M. Garg**, Y.V. Hote, and M.K. Pathak, "PI Controller Design of a DC-DC Zeta Converter for Specific Phase Margin and Cross-over Frequency," **IEEE** 10th Asian Control Conference (ASCC 2015) held in Malaysia, pp. 1-6, 2015
2. **M.M. Garg** and M.K. Pathak, "Matlab/Simulink based Model of Non-ideal Zeta Converter," 4th International Conference on Power and Energy Systems (ICPES- 2014) held in Singapore, pp. 1-5, 2014
3. **M.M. Garg** and Y.V. Hote, "Leverrier Algorithm based Reduced Order Modeling of DC-DC Converters," **IEEE** 6th India International Conference on Power Electronics (IICPE-2014) held at NIT Kurukshetra, India, pp. 1-6, 2014
4. **M.M. Garg**, Y.V. Hote, and M.K. Pathak, "Leverrier's Algorithm based Modeling of Higher-order DC-DC Converters," **IEEE** 5th India International Conference on Power Electronics (IICPE-2012) held at DTU Delhi, India, pp. 1-6, 2012

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