# PERFORMANCE ENHANCEMENT OF MULTILEVEL INVERTER FOR INDUCTION MOTOR DRIVE

**Ph.D. THESIS**

*by*

**SANJIV KUMAR**


**DEPARTMENT OF ELECTRICAL ENGINEERING**
**INDIAN INSTITUTE OF TECHNOLOGY ROORKEE**
**ROORKEE – 247667 (INDIA)**
**JULY, 2016**

# PERFORMANCE ENHANCEMENT OF MULTILEVEL INVERTER FOR INDUCTION MOTOR DRIVE

**A THESIS**

*Submitted in partial fulfilment of the requirements for the award of the degree*

*of*

**DOCTOR OF PHILOSOPHY**

*in*

**ELECTRICAL ENGINEERING**

*by*

**SANJIV KUMAR**


**DEPARTMENT OF ELECTRICAL ENGINEERING**
**INDIAN INSTITUTE OF TECHNOLOGY ROORKEE**
**ROORKEE – 247667 (INDIA)**
**JULY, 2016**

# INDIAN INSTITUTE OF TECHNOLOGY ROORKEE
# ROORKEE

## CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in this thesis entitled **"PERFORMANCE ENHANCEMENT OF MULTILEVEL INVERTER FOR INDUCTION MOTOR DRIVE ",** in partial fulfilment of the requirements for the award of the Degree of Doctor of Philosophy and submitted in the Department of Electrical Engineering of the Indian Institute of Technology Roorkee, Roorkee is an authentic record of my own work carried out during a period from July, 2012 to July, 2016 under the supervision of Dr. Pramod Agarwal, Professor, Department of Electrical Engineering, Indian Institute of Technology Roorkee, Roorkee.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other Institute.

(**Sanjiv Kumar**)

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

(Pramod Agarwal)
Supervisor

**Dated: _____**

## ABSTRACT

Conversion from electrical energy to mechanical energy is an important process in modern industrial civilization and it is done by means of electrical machines. About half of the electrical energy generated in a developed country is ultimately consumed by electric motors, of which 90% are induction motors as they are simple, rugged and cheap. The rapid development of power electronic devices and converter technologies in the last few decades has made possible to develop energy efficient adjustable speed induction motor drives. The conventional two-level voltage source inverters (VSIs) are widely used in induction motor drive applications due to the simple structure, control, reliability as well as cheaper parts. In recent years, industries have begun to use high power equipment, which now are at megawatt levels. In high power and high performance drive applications, two-level VSIs suffers from problems like high dv/dt, higher switching loss, poor power quality, higher common-mode voltages and electromagnetic interference (EMI). Adjustable speed drives in megawatt range are usually connected to medium-voltage network due to restriction on current rating at low-voltage, therefore to connect the conventional two-level VSI with medium-voltage network several switching devices are to be connected in series. All the series connected switching devices should have accurate static and dynamic voltage sharing circuit which is not practically possible.

Multilevel inverter (MLI) approach, on the other hand offers low dv/dt stress, good power quality, low switching loss, high voltage capability and good electro-magnetic compatibility (EMC) even at high power applications. Use of several levels of DC-voltage enables MLI to achieve better quality output voltages at low switching frequency. MLI topologies require more device count, but they are modular in structure and compact in size as they require reduced size output filter and transformer or none of them. Due to above features multilevel inverters emerge as an attractive solution for high power and high performance medium-voltage induction motor drives.

Induction motors used in electric drives are either delta or star connected with three terminals and the motors are fed using two-level VSIs. In open-end winding induction motor, this delta or star connection is opened and the motor now has six terminals. The performance equivalent to 3-level inverter can be obtained by feeding these six terminals of open-end winding induction motor from both sides using two three-phase two-level VSI. There are certain advantages of the open-end winding method, such as common-mode voltage reduction and increase in the voltage transfer ratio. The multilevel inverter topologies proposed in the thesis uses this dual inverter fed open-end winding configuration for the induction motor.

The present work is carried out to improve the performance of MLI for induction motor drive with simplified modelling, control and implementation. Problems associated with

conventional two-level voltage source PWM (Pulse Width Modulation) inverter fed induction motor drives are addressed first. Their possible solutions and recent trends are discussed. Different MLIs topologies along with their features, technical challenges, applications, historical developments and research gaps are discussed. A comprehensive literature survey on MLI including various MLI topologies, diverse modulation and control schemes for induction motor are given in detail. MLI for induction motor drive is designed, developed and investigated.

In the literature, it has been shown that an open-end winding induction motor drive fed with two-level VSI inverters produce phase voltage waveforms and voltage space vector locations similar to a conventional 3-level inverter. This dual two-level (D2L) configuration is taken as the first investigative object. A mathematical model of the squirrel cage open-end stator winding induction motor in stationary reference is developed along with switching function based D2L inverter model. The carrier based space vector pulse width modulation (SVPWM) scheme is used to generate the control pulses for switching devices. To investigate the performance of SVPWM based D2L inverter scheme for open-end induction motor drive under steady-state and dynamic conditions simulation study is carried out in MATLAB/Simulink environment. The developed motor model is operated in constant *V/f* mode under no-load condition covering the entire range of modulation. Various simulation results are obtained and analyzed for performance evaluation.

A 5-level inverter configuration based on conventional 2-level inverters is selected as a second investigative object. The open-end winding induction motor is fed by 3-level inverter from one end and the other end is fed by two-level inverter. The combined effect of these two inverters generates five levels as $-V_{DC}/4$, 0, $+V_{DC}/4$, $+V_{DC}/2$ and $+3V_{DC}/4$, where $V_{DC}$ is the equivalent DC link voltage of the conventional two-level inverter fed induction motor drive. The 3-level inverter is realized by cascading two conventional two-level inverters. All three conventional two-level inverters are powered by isolated DC sources. This scheme uses asymmetrical DC link voltages to generate five levels in phase voltage of induction motor. A total of 512 space vector combinations are possible with this configuration which are distributed over 61 space vector locations. It has been shown that the same 5-level inverter circuit can produce six levels as $-V_{DC}/5$, 0, $+V_{DC}/5$, $+2V_{DC}/5$, $+3V_{DC}/5$ and $+4V_{DC}/5$ by selecting a proper ratio of DC link voltages of individual two-level inverters. A switching function based mathematical model is developed and simulated with MATLAB/Simulink. The 5-level inverter performance is evaluated in MATLAB by running a 1.5 kW open-end winding induction motor model at no-load in *V/f* control mode. In the simulation results, it is found that the adopted scheme generates the voltage levels similar to conventional 5-level inverters.

To generate high resolution voltage space vectors with reduced number of components for an open-end winding induction motor, a 9-level inverter scheme is proposed. The 9-level inverter operation is realized by feeding both ends of the open-end winding by two 3-level inverters with asymmetrical DC link voltage. These 3-level inverters are realized by cascading two 2-level inverters. The total DC link voltage $V_{DC}$ is divided into two 3-level inverters in the ratio of $3V_{DC}/4$ and $V_{DC}/4$. The proposed topology completely eliminates the requirement of clamping diodes and DC-link capacitors which are needed in the neutral point clamped (NPC) inverter. It also eliminates eighty four capacitors of rating $V_{DC}/8$ which are required in case of 9-level FC inverter topology. Compared to the conventional cascade H-bridge topology, the proposed inverter requires less number of power supplies. The flow of triplen harmonic current through the switches and motor windings is not possible in the proposed scheme due to use of four isolated DC supply. A modified level shifted triangular carrier based SVPWM technique is used for the proposed drive system. The proposed PWM scheme is capable of ensuring a smooth changeover from the mode of two-level inversion to the 3-level, then 3-level to 4-level, then from 4-level to 5-level and so on up to 9-level inversion and vice versa. This feature reduces the switching losses at lower speed range. A switching function based mathematical model of the proposed drive system is developed and validated by detailed analytical results in MATLAB/Simulink environment.

A hybrid 9-level inverter is another configuration proposed in the thesis to reduce the requirement of four isolated DC sources of two different voltage rating into two isolated DC sources of the same voltage rating. The proposed topology is realized by feeding one end of the open-end winding induction motor by 5-level hybrid inverter and the other end by conventional two-level inverter. The three phase hybrid 5-level inverter is realized by cascading a 3-level flying capacitor (FC) inverter with capacitor fed H-bridge in each phase. The capacitor voltages are maintained at desired voltage level for the entire modulation range and also during transient operation by making use of redundant switching states available for generating different voltage levels. The proposed topology is capable of operating as 5-level inverter at full load in case of failure of H-bridge by simply bypass the faulty H-bridge; this feature enhances the reliability drive of the system. The proposed topology is compared with conventional topology in terms of the number of components used. The proposed inverter requires thirty IGBTs whereas the conventional topologies NPC, FC and CHB topology based 9-level inverters require forty eight IGBTs. As compared to asymmetrical cascade H-bridge (ACHB) topology which requires six isolated DC supply of two different voltages rating the proposed topology needs only two isolated DC supplies of the same rating. The proposed topology requires only six capacitors out of which three are of voltage rating $V_{DC}/4$ and three are of voltage rating $V_{DC}/8$ on the other hand, conventional 9-level FC inverter requires eighty four capacitors of voltage rating $V_{DC}/8$. The conventional

NPC 9-level inverter requires 168 clamping diodes and eight capacitors of voltage rating $V_{DC}/8$; this requirement is completely eliminated in the proposed hybrid 9-level inverter. In the proposed inverter semiconductor switching devices which operated at a higher DC voltage switch less, hence low switching frequency rating devices can be used. As both sides inverters are fed by isolated DC supply so zero sequence currents are inherently prevented because there is no path available to flow of these currents. In the proposed hybrid 9-level inverter switching devices which operate at higher voltage level switch less as compared to the switching devices which operate at lower voltage level in the entire range of linear modulation, this feature can lead to use of low switching frequency rating power semiconductor devices hence overall cost is reduced. A switching state based mathematical model is developed to realize 9-level inversion operation. The space vector location and available switching redundancy at different locations are discussed. The capacitors voltage balancing algorithm and performance of the drive is evaluated during steady state and transient state in MATLAB/Simulink environment by operating an open-end winding induction motor at no-load in constant *V/f* mode and results are presented.

The third topology proposed in the present work is an eighteen-level inverter topology for open-end winding induction motor drive. In the proposed topology one end of the open-end IM is fed by conventional two-level inverter, while the other end is connected to a nine-level asymmetrical cascade H-bridge (ACHB) inverter. The proposed topology is capable of generating eighteen levels as $-V_{DC}$, $-12V_{DC}/13$, $-11V_{DC}/13$ $-10V_{DC}/13$, $-9V_{DC}/13$, $-8V_{DC}/13$, $-7V_{DC}/13$, $-6V_{DC}/13$, $-5V_{DC}/13$, $-4V_{DC}/13$, $-3V_{DC}/13$, $-2V_{DC}/13$, $-V_{DC}/13$, 0, $+V_{DC}/13$, $+2V_{DC}/13$, $+3V_{DC}/13$ and $+4V_{DC}/13$. The proposed topology requires less number of components as compared to conventional multilevel inverter (MLI) topology. An interesting feature of the proposed topology is that, it can operate in nine-level mode by connecting the motor winding in star in case of failure of the two-level inverter. Similarly, if the fault occurs in ACHB inverter the proposed inverter can operate in two-level mode. Thus, the reliability of the system is improved. Exhaustive simulation study is carried out to evaluate the performance of proposed inverter for the entire modulation range and results are presented.

In this thesis extensive simulation study is carried out on D2L inverter, 5-level inverter, 9-level inverter, hybrid 9-level inverter and 18-level inverter for an induction motor with open-end windings. In order to validate the simulation results, downscaled prototypes of following topologies are developed in the laboratory and experimentation is carried out:

Topology-1: 5-Level Inverter for open-end IMD

Topology-2: 9-Level Inverter for open-end IMD

Topology-3: Hybrid 9-Level Inverter for open-end IMD

The system hardware of these prototypes is developed in three stages:

- Implementation of power circuit
- Implementation of control circuit
- Measurement of system parameters

The inverter circuits of all three topologies are developed using IGBTs (IRG4PH40KD). RT-Lab from Opal-RT Technologies is used as real-time hardware-in-loop controller to generate gate pulses for IGBTs in real-time. The different hardware circuits which are required for the proper operation of experimental setup such as driver circuit, isolation and dead-band circuits, voltage and current sensor circuits are designed, developed and interfaced with RT-Lab real time controller.

In simulation studies of aforementioned topologies, the total DC link voltage ($V_{DC}$) of 600V was selected, but due to the practical constraints total DC-link voltage of 200V is used for experimental investigations. An open-end winding induction motor of 1.5kW, 415V, 50Hz, 4pole is used as load and operated at no-load with constant *V/f* control. As the experimentation is carried out at reduced voltage, for validating the experimental results, the simulation study at reduced voltage is also carried out. The experimental and simulation results are matching to each other.

The multilevel inverter topologies presented in this thesis are particularly suitable for high power drive applications such as an electric vehicle, traction, etc. Although all the proposed schemes are experimentally tested and validated on downscaled laboratory prototypes, but the proposed topologies, SVPWM technique and *V/f* control scheme are general in nature and can be easily applied to high power applications induction motor drive.

## ACKNOWLEDGEMENTS

With GOD's grace I have got this opportunity to thanks all those who have supported me all through this course of work. First and foremost, I would like to express my sincere gratitude to my supervisor Dr. Pramod Agarwal, Professor, Department of Electrical Engineering, Indian Institute of Technology Roorkee, for his guidance, valuable suggestions, patience, continuous encouragement and constant source of inspiration throughout the course of this study. I am sincerely indebted to him for his pronounced individuality, humanistic and warm personal approach, and excellent facilities provided to me in the laboratory to carry out this research work smoothly.

I heartily extend my gratitude to Dr. S. P. Srivastava, Professor & Head, Department of Electrical Engineering, Indian Institute of Technology, Roorkee, for providing excellent laboratory and computing facilities of the Department for the research work.

I would like to acknowledge my research committee members Dr. B. Das (Professor EED & Chairman SRC), Dr. S. P. Gupta (Professor EED) and Dr. R. C. Mittal (Professor Mathematics Department), for their time to time critical examination of my research work and for their constructive recommendations.

My heartfelt thanks to Dr. K. Gopakumar (Professor, CEDT, IISc Bangalore), Dr. Bhim Singh (Professor, EED, IITD), Mr. Mooteri K. Vasantha (Emeritus Professor, EED, IITR), and Dr. Shailendra Jain (Professor, EED, NIT Bhopal), for their valuable suggestions during the work.

I acknowledge my sincere gratitude to All India Council for Technical Education, Government of India for providing financial support during my Ph.D. work. The research work has been carried out under Quality Improvement Programme (QIP) scheme of AICTE.

I will never forget my friends Dr. Aurobind Panda, Dr. Rakesh Maurya, Dr. Lal Bahadur Prasad, Dr. Vasundhara Mahajan, Mr. Sukant Haldar, and Mr. Anubhav Agarwal for kept me motivated by their caring words and wholehearted supports during the research work. I will always thankful to my good friends Mr. Pannala Sanjeev and Mr. Ravindra Kumar for their help and moral support.

I would also like to thank all the administrative & technical staff of the Department of Electrical Engineering, Indian Institute of Technology Roorkee, for their cooperation and necessary facilities provided to me to carry out this research work. My special thanks to Mr. Ameer Ahmad, Mr. Gautam Singh and Mr. Rakesh Kumar, who helped me to prepare experimental setup of my research work.

My sincere thanks are also due to Director Harcourt Butler Technological Institute (HBTI), Kanpur (India) and all faculty members of Electrical Engineering Department of HBTI, Kanpur (India), for the cooperation they have extended to me while working at IIT Roorkee.

“God could not be everywhere so he created mothers! With her blessing there’s always a good day after, one know everything will turn out fine”. With these words, I sincerely acknowledge the blessing of my mother Smt. Sheela Saxena for her encouragement and moral support rendered to me throughout my life.

No words can adequately express my deepest gratitude and love to my wife Smt. Jyoti Saxena for her unconditional support, encouragement, love and inspiration and always being there for me during good and bad times. I once again thanks to my wife and mother for shouldering all family responsibilities with a smiling face. I am thankful to my loving son Manas who always provided entertainment and a grand welcome to me at home with his big cheerful smile after long working hours in the lab. I am indebted to my son, as he has missed me lot during my work.

I sincerely acknowledge the ethical support from my Father-in-law Shri. Rakesh Prakesh Srivastava and Mother-in-law Smt. Suman Srivastava. I would like to thank whole in-law’s family for their constant love and encouragement.

Last but not the least I would like to thank to Almighty ‘GOD’ for giving me health, strength and perseverance to complete this study.

.

**(SANJIV KUMAR)**

## CONTENTS

**ABSTRACT** ..... **I**

**ACKNOWLEDGEMENTS** ..... **VII**

**CONTENTS** ..... **IX**

**LIST OF FIGURES** ..... **XIII**

**LIST OF TABLES** ..... **XXXI**

**LIST OF ACRONYMS** ..... **XXXIII**

**LIST OF SYMBOLS** ..... **XXXV**

**CHAPTER 1: INTRODUCTION AND LITERATURE REVIEW** ..... **1**

1.1 Overview ..... 1

1.2 Inverter Topologies for Induction Motor Drives ..... 2

1.2.1 Conventional Two-Level Inverter ..... 2

1.2.2 Multilevel Inverter ..... 4

1.3 Literature Review ..... 6

1.3.1 Multilevel Inverter Topologies ..... 6

1.3.1.1 Diode Clamped Multilevel Inverter (DCMLI) ..... 7

1.3.1.2 Flying Capacitor Multilevel Inverter (FCMLI) ..... 9

1.3.1.3 Cascade H-Bridge Multilevel Inverter (CHBMLI) ..... 10

1.3.1.4 Multilevel Inversion Using Split-phase Induction Motor ..... 11

1.3.1.5 Multilevel Inversion Using Open-end Winding Induction Motor ..... 12

1.3.2 Modulation Techniques for Multilevel Inverters ..... 14

1.3.2.1 Selective Harmonic Elimination PWM (SHE-PWM) ..... 15

1.3.2.2 Sinusoidal PWM (SPWM) ..... 15

1.3.2.3 Space Vector PWM (SVPWM) ..... 18

1.3.2.4 Sigma Delta Modulation (SDM) ..... 19

1.3.2.5 Hysteresis Current Control (HCC) Modulation ..... 20

1.3.3 Applications of Multilevel Inverters ..... 21

1.3.4 Induction Motor Speed Control Methods ..... 24

1.4 Scope of Work and Author's Contribution ..... 25

1.5 Organization of the Thesis ..... 28

**CHAPTER 2: DUAL TWO-LEVEL INVERTER FOR INDUCTION MOTOR DRIVE** ..... **31**

2.1 Introduction ..... 31

2.2 System Configuration and Switching Logic ..... 31

2.2.1 Power Circuit ..... 31

2.2.2 Switching Logic ..... 32
2.3 Control Scheme ..... 33
2.4 Mathematical Modelling of Dual Two-Level (D2L) Inverter fed IMD ..... 34
2.4.1 Model of D2L Inverter ..... 34
2.4.2 Mathematical Modelling of Open-end Stator Winding Induction Motor ..... 37
2.5 Simulation Studies ..... 40
2.5.1 Simulation Results and Discussion ..... 43
2.6 Conclusion ..... 52

**CHAPTER 3: FIVE-LEVEL INVERTER FOR INDUCTION MOTOR DRIVE .....53**

3.1 Introduction ..... 53
3.2 5-Level Inverter Scheme for Induction Motor Drive ..... 53
3.2.1 Power Circuit ..... 53
3.2.2 Switching Logic ..... 54
3.2.3 Analysis of Voltage Space Vectors ..... 55
3.2.4 Selection of DC Link Voltage Ratio ..... 58
3.3 Control Scheme ..... 59
3.4 Mathematical Modelling of 5-level Inverter Scheme ..... 61
3.5 Simulation Results and Discussion ..... 62
3.6 Performance Comparison ..... 73
3.7 Conclusion ..... 73

**CHAPTER 4: NINE-LEVEL INVERTER FOR INDUCTION MOTOR DRIVE .....75**

4.1 Introduction ..... 75
4.2 9-Level Inverter Scheme for Induction Motor Drive ..... 76
4.2.1 Power Circuit ..... 76
4.2.1.1 Comparison between Proposed Inverter and Conventional MLI ..... 77
4.2.2 Switching Logic ..... 77
4.2.3 Analysis of Voltage Space Vectors ..... 79
4.2.4 Effect of common-mode voltage ..... 81
4.2.5 Selection of DC Link Voltage Ratio ..... 81
4.3 Modified SVPWM technique for the proposed nine-level inverter ..... 82
4.4 Mathematical Modelling of Proposed 9-Level Inverter ..... 86
4.4.1 Mathematical Model of 9-Level Inverter ..... 87
4.5 Simulation Results and Discussion ..... 89
4.6 Performance Comparison ..... 110
4.7 Conclusion ..... 111

**CHAPTER 5: HYBRID NINE-LEVEL INVERTER FOR INDUCTION MOTOR DRIVE..113**
5.1 Introduction ..... 113
5.2 Hybrid 9-Level Inverter Scheme for Induction Motor Drive ..... 114
5.2.1 Power Circuit ..... 114
5.2.1.1 Salient Features of Proposed Inverter Topology ..... 115
5.2.2 Generation of Different Levels and Capacitor Voltage Balancing Logic ..... 116
5.2.3 Control Strategy and Capacitor Design ..... 127
5.2.4 Analysis of Voltage Space Vectors ..... 129
5.3 Mathematical Modelling of Hybrid 9-Level Inverter ..... 132
5.4 Simulation Results and Discussion ..... 133
5.5 Performance Comparison ..... 161
5.6 Conclusion ..... 163

**CHAPTER 6: EIGHTEEN-LEVEL INVERTER FOR INDUCTION MOTOR DRIVE..... 165**
6.1 Introduction ..... 165
6.2 18-Level Inverter Scheme for Induction Motor Drive ..... 166
6.2.1 Power Circuit ..... 166
6.2.2 Salient Features of Proposed Inverter Topology ..... 168
6.3 Control Strategy and PWM Generation ..... 169
6.4 Mathematical Modelling of Proposed 18-Level Inverter ..... 172
6.5 Simulation Results and Discussion ..... 173
6.6 Performance Comparison ..... 185
6.7 Conclusion ..... 186

**CHAPTER 7: SYSTEM DEVELOPMENT AND EXPERIMENTATION ..... 187**
7.1 Introduction ..... 187
7.2 Hardware Implementation ..... 188
7.2.1 Power Circuit Implementation ..... 188
7.2.1.1 Topology-1: 5-Level Inverter Scheme ..... 189
7.2.1.2 Topology-2: 9-Level Inverter Scheme ..... 190
7.2.1.3 Topology-3: Hybrid 9-Level Inverter Scheme ..... 190
7.2.2 Control Circuit Implementation ..... 190
7.2.2.1 Isolation Circuit ..... 191
7.2.2.2 Dead-Band Circuit ..... 191
7.2.2.3 IGBT Driver Circuit ..... 193
7.2.3 Measurement of System Parameter ..... 194
7.2.3.1 Measurement of Voltage ..... 194
7.2.3.2 Measurement of Current ..... 195

7.2.4 System Software ..... 196
7.3 Experimental Validation ..... 196
7.3.1 Experimental Validation of 5-level Inverter ..... 197
7.3.2 Experimental Validation of 9-level Inverter ..... 210
7.3.3 Experimental Validation of Hybrid 9-level Inverter ..... 230
7.4 Conclusion ..... 253

**CHAPTER 8: CONCLUSION AND FUTURE SCOPE OF RESEARCH ..... 255**
8.1 Conclusion ..... 255
8.2 Future Scope of Research ..... 258

**PUBLICATIONS FROM THE WORK ..... 259**
**PHOTOGRAPHS OF THE EXPERIMENTAL SET-UP ..... 261**
**BIBLIOGRAPHY ..... 267**
**APPENDIX – A ..... 283**
**APPENDIX – B ..... 285**

## LIST OF FIGURES

Fig. 1.1: Power circuit of conventional two-level MV VSI drive ..... 3
Fig. 1.2: One phase leg of an inverter with (a) two levels; (b) three levels; (c) n levels ..... 5
Fig. 1.3: Three-phase five-level diode clamped inverter ..... 8
Fig. 1.4: Three-phase five-level flying capacitor inverter ..... 9
Fig. 1.5: Three-phase five-level cascade H-bridge inverter ..... 10
Fig. 1.6: Split phase induction motor drive ..... 12
Fig. 1.7: Schematic of power circuit for open-end winding based three-level inverter ..... 13
Fig. 1.8: Classification of multilevel modulation techniques ..... 14
Fig. 1.9: Carrier arrangements for five-level inverter; (a) PD, (b) POD, (c) APOD, (d)PS ..... 17
Fig. 1.10: Block diagrams of delta modulation: (a) Simple delta modulator, (b) Sigma–delta modulator ..... 20
Fig. 1.11: Block diagram of sigma delta modulation control of a multilevel inverter ..... 20
Fig. 2.1 :Dual two-level (D2L) inverter scheme for open-end winding induction motor drive ... 32
Fig. 2.2: Switching signals for the devices of phase–A of three-level D2L inverter using LSPWM technique ..... 33
Fig. 2.3: Diagrammatic representation of switching functions and inverter pole voltages for D2L inverter ..... 35
Fig. 2.4: Equivalent circuit of an induction motor in stationary reference frame ..... 39
Fig. 2.5: Simulink model of D2L inverter scheme (a) Power circuit (b) Control circuit and monitoring ..... 41
Fig. 2.6: Graph between THD of motor phase-A voltage and switching frequency for different value of modulation index ..... 42
Fig. 2.7: (a) Motor phase-A, voltage ($V_{A1A2}$) and current ($i_{A1A2}$) at $m$=0.2; $f^*_m$ =10Hz for SVPWM based D2L inverter for open-end IM drive at no load (b) zoom view of waveforms shown in (a) ..... 44
Fig. 2.8: (a) Harmonic spectrum of phase-A voltage ($V_{A1A2}$) at $m$=0.2; $f^*_m$ =10Hz (b) Harmonic spectrum of phase-A current ($i_{A1A2}$) at $m$=0.2; $f^*_m$ =10Hz (c) Zoom view of harmonic spectrum shown in (b) ..... 45
Fig. 2.9: Top trace; Inverter-1 pole voltage ($V_{A1O}$), Middle trace; Inverter-2 pole voltage ..... 46
Fig. 2.10: Motor phase-A, voltage ($V_{A1A2}$) and current ($i_{A1A2}$) at $m$=0.8; $f^*_m$ =40Hz for SVPWM .. 46
Fig. 2.11: (a) Harmonic spectrum of phase-A voltage ($V_{A1A2}$) at $m$=0.8; $f^*_m$ =40Hz (b) Harmonic spectrum of phase-A current ($i_{A1A2}$) at $m$=0.8; $f^*_m$ =40Hz (c) Zoom view of harmonic spectrum shown in (b) ..... 47
Fig. 2.12: Top trace; Inverter-1 pole voltage ($V_{A1O}$), Middle trace; Inverter-2 pole voltage .... 48
Fig. 2.13 : Motor phase-A, voltage ($V_{A1A2}$) and current ($i_{A1A2}$) at $m$=1; $f^*_m$ =50Hz for SVPWM48

Fig. 2.14: (a) Harmonic spectrum of phase-A voltage ($V_{A1A2}$) at $m$=1.0; $f^*_m$ =50 Hz (b) Harmonic spectrum of phase-A current ($i_{A1A2}$) at $m$=1.0; $f^*_m$ =50Hz (c) Zoom view of harmonic spectrum shown in (b) ..... 49
Fig. 2.15: Top trace; Inverter-1 pole voltage ($V_{A1O}$), Middle trace; Inverter-2 pole voltage ..... 50
Fig. 2.16: (a) Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A1A2}$ (lower trace) waveforms under sudden change in modulation index from 0.2 to 0.8 (b) Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A1A2}$ (lower trace) waveforms under sudden change in modulation index from 0.8 to 0.2 ..... 51
Fig. 3.1: Power circuit of 5-level inverter scheme for open-end winding induction motor drive ..... 54
Fig. 3.2: Equivalent voltage space vector $V_s$ in $\alpha$-$\beta$ plane ..... 57
Fig. 3.3: Voltage space vectors distribution for 5-level inverter ..... 57
Fig. 3.4: Power circuit of 6-level inverter scheme for open-end winding induction motor drive ..... 59
Fig. 3.5: Switching signals for the devices of phase–A of 5-level inverter using LSPWM technique ..... 60
Fig. 3.6: Motor phase-A, voltage $V_{A2A3}$ (upper trace) and current $i_{A2A3}$ (lower trace) of 5-level inverter fed open-end IM drive at no load ($m$=0.2; $f^*_m$ =10Hz) ..... 64
Fig. 3.7: (a) Harmonic spectrum of phase-A voltage ($V_{A2A3}$) at $m$=0.2; $f^*_m$ =10Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 64
Fig. 3.8: (a) Harmonic spectrum of phase-A current ($i_{A2A3}$) at $m$=0.2; $f^*_m$ =10Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 65
Fig. 3.9: Top trace; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace; Two-level inverter-B pole voltage ($V_{A3O'}$), Bottom trace; Difference of 3-level inverter-A and two-level inverter-B pole voltages ($V_{A2O}$ - $V_{A3O'}$) at $m$=0.2; $f^*_m$ =10Hz ..... 65
Fig. 3.10: Motor phase-A, voltage $V_{A2A3}$ (upper trace) and current $i_{A2A3}$ (lower trace) of 5-level inverter fed open-end IM drive at no load ($m$=0.4; $f^*_m$ =20Hz) ..... 66
Fig. 3.11: (a) Harmonic spectrum of phase-A voltage ($V_{A2A3}$) at $m$=0.4; $f^*_m$ =20Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 66
Fig. 3.12: (a) Harmonic spectrum of phase-A current ($i_{A2A3}$) at $m$=0.4; $f^*_m$ =20Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 67
Fig. 3.13: Top trace; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace; Two-level inverter-B pole voltage ($V_{A3O'}$), Bottom trace; Difference of 3-level inverter-A and two-level inverter-B pole voltages ($V_{A2O}$ - $V_{A3O'}$) at $m$=0.4; $f^*_m$ =20Hz ..... 67
Fig. 3.14: Motor phase-A, voltage $V_{A2A3}$ (upper trace) and current $i_{A2A3}$ (lower trace) of 5-level inverter fed open-end IM drive at no load ($m$=0.6; $f^*_m$ =30Hz) ..... 68
Fig. 3.15: (a) Harmonic spectrum of phase-A voltage ($V_{A2A3}$) at $m$=0.6; $f^*_m$ =30Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 68

Fig. 3.16: (a) Harmonic spectrum of phase-A current ($i_{A2A3}$) at $m$=0.6; $f^*_m$ =30Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 69
Fig. 3.17: Top trace; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace; Two-level inverter-B pole voltage ($V_{A3O'}$), Bottom trace; Difference of 3-level inverter-A and two-level inverter-B pole voltages ($V_{A2O}$ - $V_{A3O'}$) at $m$=0.6; $f^*_m$ =30Hz..... 69
Fig. 3.18: Motor phase-A, voltage $V_{A2A3}$ (upper trace) and current $i_{A2A3}$ (lower trace) of 5-level inverter fed open-end IM drive at no load ($m$=0.8; $f^*_m$ =40Hz)..... 70
Fig. 3.19: (a) Harmonic spectrum of phase-A voltage ($V_{A2A3}$) at $m$=0.8; $f^*_m$ =40Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 70
Fig. 3.20: (a) Harmonic spectrum of phase-A current ($i_{A2A3}$) at $m$=0.8; $f^*_m$ =40Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 71
Fig. 3.21: Top trace; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace; Two-level inverter-B pole voltage ($V_{A3O'}$), Bottom trace; Difference of 3-level inverter-A and two-level inverter-B pole voltages ($V_{A2O}$ - $V_{A3O'}$) at $m$=0.8; $f^*_m$ =40Hz..... 71
Fig. 3.22: (a) Motor phase-A voltage $V_{A2A3}$ (upper trace) and current $i_{A2A3}$ (lower trace) waveforms under sudden change in operation from two-level to 5-level at no-load (b) Motor phase-A voltage $V_{A2A3}$ (upper trace) and current $i_{A2A3}$ (lower trace) waveforms under sudden change in operation from 5-level to two-level at no-load ..... 72
Fig. 4.1: Power circuit of 9-level inverter for open-end winding induction motor drive..... 76
Fig. 4.2: Locations of voltage space-phasors for 9-level inverter ..... 80
Fig. 4.3: (a) Reference waves during two-level operation in conventional SVPWM (b) Reference waves during two-level operation in modified SVPWM (c) Reference waves during 4-level operation in conventional SVPWM (d) Reference waves during 4-level operation in modified SVPWM (e) Reference waves during 6-level operation in conventional SVPWM (f) Reference waves during 6-level operation in modified SVPWM ..... 84
Fig. 4.4: Reference waves during 9-level operation in conventional and modified SVPWM . 85
Fig. 4.5: Motor phase-A, voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) of 9-level inverter fed open-end IM drive at no load ($m$=0.08; $f^*_m$ =4Hz; 2-level mode) ..... 90
Fig. 4.6: (a) Harmonic spectrum of phase-A voltage ($V_{A2A4}$) at $m$=0.08; $f^*_m$ =4Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 90
Fig. 4.7: (a) Harmonic spectrum of phase-A current ($i_{A2A4}$) at $m$=0.08; $f^*_m$ =4Hz (b) Zoom view of harmonic spectrum shown in (a)..... 91
Fig. 4.8 :Top trace; Inverter-A pole voltage ($V_{A2O}$), Middle trace; Inverter-B pole voltage ($V_{A4O'}$), Bottom trace; Difference of Inverter-A and Inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$) at $m$=0.08; $f^*_m$ =4Hz (2-level mode)..... 91
Fig. 4.9: Motor phase-A, voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) of 9-level inverter fed open-end IM drive at no load ($m$=0.16; $f^*_m$ =8Hz; 3-level mode) ..... 92

Fig. 4.10: (a) Harmonic spectrum of phase-A voltage ($V_{A2A4}$) at $m$=0.16; $f^*_m$ =8Hz (b) Zoom view of harmonic spectrum shown in (a)..... 93
Fig. 4.11: (a) Harmonic spectrum of phase-A current ($i_{A2A4}$) at $m$=0.16; $f^*_m$ =8Hz (b) Zoom view of harmonic spectrum shown in (a)..... 93
Fig. 4.12 :Top trace; Inverter-A pole voltage ($V_{A2O}$), Middle trace; Inverter-B pole voltage ($V_{A4O'}$), Bottom trace; Difference of Inverter-A and Inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$) at $m$=0.16; $f^*_m$ =8Hz (3-level mode)..... 94
Fig. 4.13: Motor phase-A, voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) of 9-level inverter fed open-end IM drive at no load ($m$=0.28; $f^*_m$ =14Hz; 4-level mode)..... 95
Fig. 4.14: (a) Harmonic spectrum of phase-A voltage ($V_{A2A4}$) at $m$=0.28; $f^*_m$ =14Hz (b) Zoom view of harmonic spectrum shown in (a)..... 95
Fig. 4.15: (a) Harmonic spectrum of phase-A current ($i_{A2A4}$) at $m$=0.28; $f^*_m$ =14Hz (b) Zoom view of harmonic spectrum shown in (a)..... 96
Fig. 4.16 :Top trace; Inverter-A pole voltage ($V_{A2O}$), Middle trace; Inverter-B pole voltage ($V_{A4O'}$), Bottom trace; Difference of Inverter-A and Inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$) at $m$=0.28; $f^*_m$ =14Hz (4-level mode)..... 96
Fig. 4.17: Motor phase-A, voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) of 9-level inverter fed open-end IM drive at no load ($m$=0.36; $f^*_m$ =18Hz; 5-level mode)..... 98
Fig. 4.18: (a) Harmonic spectrum of phase-A voltage ($V_{A2A4}$) at $m$=0.36; $f^*_m$ =18Hz (b) Zoom view of harmonic spectrum shown in (a)..... 98
Fig. 4.19: (a) Harmonic spectrum of phase-A current ($i_{A2A4}$) at $m$=0.36; $f^*_m$ =18Hz (b) Zoom view of harmonic spectrum shown in (a)..... 99
Fig. 4.20 :Top trace; Inverter-A pole voltage ($V_{A2O}$), Middle trace; Inverter-B pole voltage ($V_{A4O'}$), Bottom trace; Difference of Inverter-A and Inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$) at $m$=0.36; $f^*_m$ =18Hz (5-level mode)..... 99
Fig. 4.21: Motor phase-A, voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) of 9-level inverter fed open-end IM drive at no load ($m$=0.42; $f^*_m$ =21Hz; 6-level mode)..... 100
Fig. 4.22: (a) Harmonic spectrum of phase-A voltage ($V_{A2A4}$) at $m$=0.42; $f^*_m$ =21Hz (b) Zoom view of harmonic spectrum shown in (a)..... 100
Fig. 4.23: (a) Harmonic spectrum of phase-A current ($i_{A2A4}$) at $m$=0.42; $f^*_m$ =21Hz (b) Zoom view of harmonic spectrum shown in (a)..... 101
Fig. 4.24 :Top trace; Inverter-A pole voltage ($V_{A2O}$), Middle trace; Inverter-B pole voltage ($V_{A4O'}$), Bottom trace; Difference of Inverter-A and Inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$) at $m$=0.42; $f^*_m$ =21Hz (6-level mode)..... 101
Fig. 4.25: Motor phase-A, voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) of 9-level inverter fed open-end IM drive at no load ($m$=0.52; $f^*_m$ =26Hz; 7-level mode)..... 102

Fig. 4.26: (a) Harmonic spectrum of phase-A voltage ($V_{A2A4}$) at $m$=0.52; $f^*_m$ =26Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 102
Fig. 4.27: (a) Harmonic spectrum of phase-A current ($i_{A2A4}$) at $m$=0.52; $f^*_m$ =26Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 103
Fig. 4.28 :Top trace; Inverter-A pole voltage ($V_{A2O}$), Middle trace; Inverter-B pole voltage ($V_{A4O'}$), Bottom trace; Difference of Inverter-A and Inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$) at $m$=0.52; $f^*_m$ =26Hz (7-level mode)..... 103
Fig. 4.29: Motor phase-A, voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) of 9-level inverter fed open-end IM drive at no load ($m$=0.64; $f^*_m$ =32Hz; 8-level mode ) ..... 105
Fig. 4.30: (a) Harmonic spectrum of phase-A voltage ($V_{A2A4}$) at $m$=0.64; $f^*_m$ =32Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 105
Fig. 4.31: (a) Harmonic spectrum of phase-A current ($i_{A2A4}$) at $m$=0.64; $f^*_m$ =32Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 106
Fig. 4.32 :Top trace; Inverter-A pole voltage ($V_{A2O}$), Middle trace; Inverter-B pole voltage ($V_{A4O'}$), Bottom trace; Difference of Inverter-A and Inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$) at $m$=0.64; $f^*_m$ =32Hz (8-level mode)..... 106
Fig. 4.33: Motor phase-A, voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) of 9-level inverter fed open-end IM drive at no load ($m$=0.8; $f^*_m$ =40Hz; 9-level mode ) ..... 107
Fig. 4.34: (a) Harmonic spectrum of phase-A voltage ($V_{A2A4}$) at $m$=0.8; $f^*_m$ =40Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 107
Fig. 4.35: (a) Harmonic spectrum of phase-A current ($i_{A2A4}$) at $m$=0.8; $f^*_m$ =40Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 108
Fig. 4.36 :Top trace; Inverter-A pole voltage ($V_{A2O}$), Middle trace; Inverter-B pole voltage ($V_{A4O'}$), Bottom trace; Difference of Inverter-A and Inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$) at $m$=0.8; $f^*_m$ =40Hz (9-level mode)..... 108
Fig. 4.37: (a) Motor phase-A voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) waveforms under sudden change in operation from two-level to 9-level at no-load (b) Motor phase-A voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) waveforms under sudden change in operation from 9-level to two-level at no-load ..... 109
Fig. 5.1: Power circuit of hybrid 9-level inverter for induction motor drive ..... 114
Fig. 5.2: Methods of generating voltage level -$V_{DC}$/2 ($L_1$) in phase-A and current path (a) For switching state $S_{A1}$=0, $S_{A2}$=0, $S_{A3}$=0, $S_{A4}$=0, $S_{A5}$=1 (b) For switching state $S_{A1}$=0, $S_{A2}$=0, $S_{A3}$=1, $S_{A4}$=1, $S_{A5}$=1..... 119
Fig. 5.3: Methods of generating voltage level -3$V_{DC}$/8 ($L_2$) in phase-A and current path (a) For switching state $S_{A1}$=0, $S_{A2}$=0, $S_{A3}$=0, $S_{A4}$=1, $S_{A5}$=1 (b) For switching state $S_{A1}$=0, $S_{A2}$=1, $S_{A3}$=1, $S_{A4}$=0, $S_{A5}$=1 (c) For switching state $S_{A1}$=1, $S_{A2}$=0, $S_{A3}$=1, $S_{A4}$=0, $S_{A5}$=1 ..... 120

Fig. 5.4: Methods of generating voltage level $-V_{DC}/4$ ($L_3$) in phase-A and current path (a) For switching state $S_{A1}$=1, $S_{A2}$=0, $S_{A3}$=0, $S_{A4}$=0, $S_{A5}$=1 (b) For switching state $S_{A1}$=0, $S_{A2}$=1, $S_{A3}$=0, $S_{A4}$=0, $S_{A5}$=1 (c) For switching state $S_{A1}$=0, $S_{A2}$=1, $S_{A3}$=1, $S_{A4}$=1, $S_{A5}$=1 (d) For switching state $S_{A1}$=1, $S_{A2}$=0, $S_{A3}$=1, $S_{A4}$=1, $S_{A5}$=1 ..... 121
Fig. 5.5: Methods of generating voltage level $-V_{DC}/8$ (L4) in phase-A and current path (a) For switching state $S_{A1}$=0, $S_{A2}$=1, $S_{A3}$=0, $S_{A4}$=1, $S_{A5}$=1 (b) For switching state $S_{A1}$=1, $S_{A2}$=0, $S_{A3}$=0, $S_{A4}$=1, $S_{A5}$=1 (c) For switching state $S_{A1}$=1, $S_{A2}$=1, $S_{A3}$=1, $S_{A4}$=0, $S_{A5}$=1 ..... 122
Fig. 5.6: Methods of generating voltage level 0 ($L_5$) in phase-A and current path (a) For switching state $S_{A1}$=1, $S_{A2}$=1, $S_{A3}$=1, $S_{A4}$=1, $S_{A5}$=1 (b) For switching state $S_{A1}$=1, $S_{A2}$=1, $S_{A3}$=0, $S_{A4}$=0, $S_{A5}$=1 ..... 123
Fig. 5.7: Methods of generating voltage level $V_{DC}/8$ ($L_6$) in phase-A and current path (a) For switching state $S_{A1}$=0, $S_{A2}$=0, $S_{A3}$=0, $S_{A4}$=1, $S_{A5}$=0 (b) For switching state $S_{A1}$=0, $S_{A2}$=1, $S_{A3}$=1, $S_{A4}$=0, $S_{A5}$=0 (c) For switching state $S_{A1}$=1, $S_{A2}$=0, $S_{A3}$=1, $S_{A4}$=0, $S_{A5}$=0 ..... 124
Fig. 5.8: Methods of generating voltage level $V_{DC}/4$ ($L_7$) in phase-A and current path (a) For switching state $S_{A1}$=1, $S_{A2}$=0, $S_{A3}$=0, $S_{A4}$=0, $S_{A5}$=0 (b) For switching state $S_{A1}$=0, $S_{A2}$=1, $S_{A3}$=0, $S_{A4}$=0, $S_{A5}$=0 (c) For switching state $S_{A1}$=0, $S_{A2}$=1, $S_{A3}$=1, $S_{A4}$=1, $S_{A5}$=0 (d) For switching state $S_{A1}$=1, $S_{A2}$=0, $S_{A3}$=1, $S_{A4}$=1, $S_{A5}$=0 ..... 125
Fig. 5.9: Methods of generating voltage level $3V_{DC}/8$ (L8) in phase-A and current path (a) For switching state $S_{A1}$=0, $S_{A2}$=1, $S_{A3}$=0, $S_{A4}$=1, $S_{A5}$=0 (b) For switching state $S_{A1}$=1, $S_{A2}$=0, $S_{A3}$=0, $S_{A4}$=1, $S_{A5}$=0 (c) For switching state $S_{A1}$=1, $S_{A2}$=1, $S_{A3}$=1, $S_{A4}$=0, $S_{A5}$=0 ..... 126
Fig. 5.10: Methods of generating voltage level $V_{DC}/2$ ($L_9$) in phase-A and current path (a) For switching state $S_{A1}$=1, $S_{A2}$=1, $S_{A3}$=1, $S_{A4}$=1, $S_{A5}$=0 (b) For switching state $S_{A1}$=1, $S_{A2}$=1, $S_{A3}$=0, $S_{A4}$=0, $S_{A5}$=0 ..... 127
Fig. 5.11: Block diagram of control logic ..... 128
Fig. 5.12: Modulating signals with eight level shifted triangular carriers ..... 129
Fig. 5.13: Locations of voltage space-phasors for 9-level inverter ..... 130
Fig. 5.14: Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A1A2}$ (lower trace) of hybrid 9-level inverter fed open-end IM drive at no load ($m$=0.08; $f^*_m$ =4Hz; 2-level mode) ..... 135
Fig. 5.15: Capacitors voltages $V_{CA1}$ (upper trace) and $V_{CA2}$ (lower trace) in 2-level mode ... 135
Fig. 5.16: (a) Harmonic spectrum of phase-A voltage ($V_{A1A2}$) at $m$=0.08; $f^*_m$ =4Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 136
Fig. 5.17: (a) Harmonic spectrum of phase-A current ($i_{A1A2}$) at $m$=0.08; $f^*_m$ =4Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 136
Fig. 5.18: Top trace; Inverter-A pole voltage ($V_{A1O}$), Middle trace; Inverter-B pole voltage ($V_{A2O'}$), Bottom trace; Difference of Inverter-A and -B pole voltages ($V_{A1O}$ - $V_{A2O'}$) at $m$=0.08; $f^*_m$ =4Hz (2-level mode) ..... 137

Fig. 5.19: Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A1A2}$ (lower trace) of hybrid 9-level inverter fed open-end IM drive at no load ($m$=0.16; $f^*_m$ =8Hz; 3-level mode)..... 138
Fig. 5.20: Capacitors voltages $V_{CA1}$ (upper trace) and $V_{CA2}$ (lower trace) in 3-level mode... 139
Fig. 5.21: (a) Harmonic spectrum of phase-A voltage ($V_{A1A2}$) at $m$=0.16; $f^*_m$ =8Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 139
Fig. 5.22: (a) Harmonic spectrum of phase-A current ($i_{A1A2}$) at $m$=0.16; $f^*_m$ =8Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 140
Fig. 5.23: Top trace; Inverter-A pole voltage ($V_{A1O}$), Middle trace; Inverter-B pole voltage ($V_{A2O'}$), Bottom trace; Difference of Inverter-A and -B pole voltages ($V_{A1O}$ - $V_{A2O'}$) at $m$=0.16; $f^*_m$ =8Hz (3-level mode)..... 140
Fig. 5.24: Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A2A4}$ (lower trace) of hybrid 9-level inverter fed open-end IM drive at no load ($m$=0.28; $f^*_m$=14Hz; 4-level mode)..... 141
Fig. 5.25: Capacitors voltages $V_{CA1}$ (upper trace) and $V_{CA2}$ (lower trace) in 4-level mode... 142
Fig. 5.26: (a) Harmonic spectrum of phase-A voltage ($V_{A1A2}$) at $m$=0.28; $f^*_m$ =14Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 142
Fig. 5.27: (a) Harmonic spectrum of phase-A current ($i_{A1A2}$) at $m$=0.28; $f^*_m$ =14Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 143
Fig. 5.28 :Top trace; Inverter-A pole voltage ($V_{A2O}$), Middle trace; Inverter-B pole voltage ($V_{A4O'}$), Bottom trace; Difference of Inverter-A and -B pole voltages ($V_{A2O}$ - $V_{A4O'}$) at $m$=0.28; $f^*_m$ =14Hz (4-level mode)..... 143
Fig. 5.29: Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A2A2}$ (lower trace) of hybrid 9-level inverter fed open-end IM drive at no load ($m$=0.36; $f^*_m$ =18Hz; 5-level mode)..... 145
Fig. 5.30: Capacitors voltages $V_{CA1}$ (upper trace) and $V_{CA2}$ (lower trace) in 5-level mode... 145
Fig. 5.31: (a) Harmonic spectrum of phase-A voltage ($V_{A1A2}$) at $m$=0.36; $f^*_m$ =18Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 146
Fig. 5.32: (a) Harmonic spectrum of phase-A current ($i_{A1A2}$) at $m$=0.36; $f^*_m$ =18Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 146
Fig. 5.33 :Top trace; Inverter-A pole voltage ($V_{A1O}$), Middle trace; Inverter-B pole voltage ($V_{A2O'}$), Bottom trace; Difference of Inverter-A and -B pole voltages ($V_{A1O}$ - $V_{A2O'}$) at $m$=0.36; $f^*_m$ =18Hz (5-level mode)..... 147
Fig. 5.34: Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A1A2}$ (lower trace) of hybrid 9-level inverter fed open-end IM drive at no load ($m$=0.42; $f^*_m$ =21Hz; 6-level mode)..... 147
Fig. 5.35: Capacitors voltages $V_{CA1}$ (upper trace) and $V_{CA2}$ (lower trace) in 6-level mode... 148
Fig. 5.36: (a) Harmonic spectrum of phase-A voltage ($V_{A1A2}$) at $m$=0.42; $f^*_m$ =21Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 148
Fig. 5.37: (a) Harmonic spectrum of phase-A current ($i_{A1A2}$) at $m$=0.42; $f^*_m$ =21Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 149

Fig. 5.38 :Top trace; Inverter-A pole voltage ($V_{A1O}$), Middle trace; Inverter-B pole voltage ($V_{A2O'}$), Bottom trace; Difference of Inverter-A and -B pole voltages ($V_{A1O}$ - $V_{A2O'}$) at $m$=0.42; $f^*_m$ =21Hz (6-level mode) ..... 149
Fig. 5.39: Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A1A2}$ (lower trace) of hybrid 9-level inverter fed open-end IM drive at no load ($m$=0.52; $f^*_m$ =26Hz; 7-level mode) ..... 150
Fig. 5.40: Capacitors voltages $V_{CA1}$ (upper trace) and $V_{CA2}$ (lower trace) in 7-level mode... 150
Fig. 5.41: (a) Harmonic spectrum of phase-A voltage ($V_{A1A2}$) at $m$=0.52; $f^*_m$ =26Hz (b) Zoom view of harmonic spectrum shown in (a)..... 151
Fig. 5.42: (a) Harmonic spectrum of phase-A current ($i_{A1A2}$) at $m$=0.52; $f^*_m$ =26Hz (b) Zoom view of harmonic spectrum shown in (a)..... 151
Fig. 5.43 :Top trace; Inverter-A pole voltage ($V_{A1O}$), Middle trace; Inverter-B pole voltage ($V_{A4O'}$), Bottom trace; Difference of Inverter-A and -B pole voltages ($V_{A1O}$ - $V_{A2O'}$) at $m$=0.52; $f^*_m$ =26Hz (7-level mode) ..... 152
Fig. 5.44: Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A1A2}$ (lower trace) of hybrid 9-level inverter fed open-end IM drive at no load (m=0.64; $f^*_m$ =32Hz; 8-level mode)..... 153
Fig. 5.45: Capacitors voltages $V_{CA1}$ (upper trace) and $V_{CA2}$ (lower trace) in 8-level mode... 153
Fig. 5.46: (a) Harmonic spectrum of phase-A voltage ($V_{A1A2}$) at $m$=0.64; $f^*_m$ =32Hz (b) Zoom view of harmonic spectrum shown in (a)..... 154
Fig. 5.47: (a) Harmonic spectrum of phase-A current ($i_{A1A2}$) at $m$=0.64; $f^*_m$ =32Hz (b) Zoom view of harmonic spectrum shown in (a)..... 154
Fig. 5.48 :Top trace; Inverter-A pole voltage ($V_{A1O}$), Middle trace; Inverter-B pole voltage ($V_{A2O'}$), Bottom trace; Difference of Inverter-A and -B pole voltages ($V_{A1O}$ - $V_{A2O'}$) at $m$=0.64; $f^*_m$ =32Hz (8-level mode) ..... 155
Fig. 5.49: Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A1A2}$ (lower trace) of hybrid 9-level inverter fed open-end IM drive at no load ($m$=0.8; $f^*_m$ =40Hz; 9-level mode )..... 155
Fig. 5.50: Capacitors voltages $V_{CA1}$ (upper trace) and $V_{CA2}$ (lower trace) in 9-level mode... 156
Fig. 5.51: (a) Harmonic spectrum of phase-A voltage ($V_{A1A2}$) at $m$=0.8; $f^*_m$ =40Hz (b) Zoom view of harmonic spectrum shown in (a)..... 156
Fig. 5.52: (a) Harmonic spectrum of phase-A current ($i_{A1A2}$) at $m$=0.8; $f^*_m$ =40Hz (b) Zoom view of harmonic spectrum shown in (a)..... 157
Fig. 5.53 :Top trace; Inverter-A pole voltage ($V_{A1O}$), Middle trace; Inverter-B pole voltage ($V_{A2O'}$), Bottom trace; Difference of Inverter-A and -B pole voltages ($V_{A1O}$ - $V_{A2O'}$) at $m$=0.8; $f^*_m$ =40Hz (9-level mode) ..... 157
Fig. 5.54: Motor phase-A voltage $V_{A1A2}$, current $i_{A1A2}$, capacitors voltages $V_{CA1}$ and $V_{CA2}$ under sudden change in operation from two-level to 9-level at no-load..... 158
Fig. 5.55: Motor phase-A voltage $V_{A1A2}$, current $i_{A1A2}$, capacitors voltages $V_{CA1}$ and $V_{CA2}$ under sudden change in operation from 9-level to two-level at no-load..... 159

Fig. 5.56: Effect of disabling the capacitor voltage balancing algorithm ..... 160
Fig. 6.1: Power circuit of 18-level inverter for induction motor drive ..... 166
Fig. 6.2: Schematic block diagram of V/f control scheme ..... 170
Fig. 6.3: Modulating signals with eight level shifted triangular carriers ..... 171
Fig. 6.4: Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A2A2}$ (lower trace) of 18-level inverter fed open-end IM drive at no load ($m$=0.16; $f^*_m$ =8Hz; 5-level mode) ..... 175
Fig. 6.5: (a) Harmonic spectrum of phase-A voltage ($V_{A1A2}$) at $m$=0.16; $f^*_m$ =8Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 175
Fig. 6.6: (a) Harmonic spectrum of phase-A current ($i_{A1A2}$) at $m$=0.16; $f^*_m$ =8Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 176
Fig. 6.7 :Top trace; Inverter-A pole voltage ($V_{A1O}$), Middle trace; Inverter-B pole voltage ($V_{A2O'}$), Bottom trace; Difference of Inverter-A and -B pole voltages ($V_{A1O}$ - $V_{A2O'}$) at $m$=0.16; $f^*_m$ =8Hz (5-level mode) ..... 176
Fig. 6.8: Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A2A2}$ (lower trace) of 18-level inverter fed open-end IM drive at no load ($m$=0.36; $f^*_m$ =18Hz; 10-level mode) ..... 177
Fig. 6.9: (a) Harmonic spectrum of phase-A voltage ($V_{A1A2}$) at $m$=0.36; $f^*_m$ =18Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 177
Fig. 6.10: (a) Harmonic spectrum of phase-A current ($i_{A1A2}$) at $m$=0.36; $f^*_m$ =18Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 178
Fig. 6.11 :Top trace; Inverter-A pole voltage ($V_{A1O}$), Middle trace; Inverter-B pole voltage ($V_{A2O'}$), Bottom trace; Difference of Inverter-A and -B pole voltages ($V_{A1O}$ - $V_{A2O'}$) at $m$=0.36; $f^*_m$ =18Hz (10-level mode) ..... 178
Fig. 6.12: Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A2A2}$ (lower trace) of 18-level inverter fed open-end IM drive at no load ($m$=0.52; $f^*_m$ =26Hz; 13-level mode) ..... 180
Fig. 6.13: (a) Harmonic spectrum of phase-A voltage ($V_{A1A2}$) at $m$=0.52; $f^*_m$ =26Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 180
Fig. 6.14: (a) Harmonic spectrum of phase-A current ($i_{A1A2}$) at $m$=0.52; $f^*_m$ =26Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 181
Fig. 6.15 :Top trace; Inverter-A pole voltage ($V_{A1O}$), Middle trace; Inverter-B pole voltage ($V_{A2O'}$), Bottom trace; Difference of Inverter-A and -B pole voltages ($V_{A1O}$ - $V_{A2O'}$) at $m$=0.52; $f^*_m$ =26Hz (13-level mode) ..... 181
Fig. 6.16: Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A2A2}$ (lower trace) of 18-level inverter fed open-end IM drive at no load ($m$=0.8; $f^*_m$ =40Hz; 18-level mode) ..... 182
Fig. 6.17: (a) Harmonic spectrum of phase-A voltage ($V_{A1A2}$) at $m$=0.8; $f^*_m$ =40Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 182
Fig. 6.18: (a) Harmonic spectrum of phase-A current ($i_{A1A2}$) at $m$=0.8; $f^*_m$ =40Hz (b) Zoom view of harmonic spectrum shown in (a) ..... 183

Fig. 6.19 :Top trace; Inverter-A pole voltage ($V_{A1O}$), Middle trace; Inverter-B pole voltage ($V_{A2O'}$), Bottom trace; Difference of Inverter-A and -B pole voltages ($V_{A1O}$ - $V_{A2O'}$) at $m$=0.8; $f^*_m$ =40Hz (18-level mode) ..... 183
Fig. 6.20: (a) Motor phase-A voltage $V_{A1A2}$ (upper trace) and current $i_{A1A2}$ (lower trace) waveforms under sudden change in modulation index from 0.16 (5-level mode) to 0.8 (18-level mode) at no-load (b) Motor phase-A voltage $V_{A1A2}$ (upper trace) and current $i_{A1A2}$ (lower trace) waveforms under sudden change in modulation index from 0.8 (18-level mode) to 0.16 (5-level mode) to at no-load ..... 184
Fig. 7.1: General block diagram of power circuit ..... 188
Fig. 7.2: (a) Power circuit of 3-Level inverter-A; (b) Power circuit of two-level inverter-B .... 189
Fig. 7.3: Power circuit of single leg of hybrid 5-level inverter-A ..... 190
Fig. 7.4: Block diagram of open-end winding induction motor drive ..... 191
Fig. 7.5: Isolation circuit for four IGBTs ..... 192
Fig. 7.6: Dead band circuit (a) Circuit diagram; (b) Waveforms at different points ..... 192
Fig. 7.7: IGBT driver circuit ..... 193
Fig. 7.8: AC/DC voltage sensing circuit ..... 195
Fig. 7.9: Hall-effect sensor based AC current sensing circuit ..... 195
Fig. 7.10: Interfacing of RT-Lab with MATLAB and real-world plant (Inverter-A and B) ..... 196
Fig. 7.11: (a) Motor phase-A, voltage $V_{A2A3}$ (upper trace Y-axis: 20V/div) and current $i_{A2A3}$ (lower trace Y-axis: 1A/div) of 5-level inverter fed open-end IM drive at no load (b) Top trace Y-axis: 100V/div; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace Y-axis: 100V/div; Difference of 3-level inverter-A and two-level inverter-B pole voltages ($V_{A2O}$ - $V_{A3O'}$), Bottom trace Y-axis: 50V/div; Two-level inverter-B pole voltage ($V_{A3O'}$) (Experimental result: $m$=0.2; $f^*_m$ =10Hz) ..... 199
Fig. 7.12: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A2A3}$ (b) Current $i_{A2A3}$ (Experimental result: $m$=0.2; $f^*_m$ =10Hz) ..... 199
Fig. 7.13: (a) Motor phase-A, voltage $V_{A2A3}$ (upper trace) and current $i_{A2A3}$ (lower trace) of 5-level inverter fed open-end IM drive at no load (b) Top trace; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace; Difference of 3-level inverter-A and two-level inverter-B pole voltages ($V_{A2O}$ - $V_{A3O'}$), Bottom trace; Two-level inverter-B pole voltage ($V_{A3O'}$) (Simulation result: $m$=0.2; $f^*_m$ =10Hz) ..... 200
Fig. 7.14: (a) Motor phase-A, voltage $V_{A2A3}$ (upper trace Y-axis: 25V/div) and current $i_{A2A3}$ (lower trace Y-axis: 1A/div) of 5-level inverter fed open-end IM drive at no load (b) Top trace Y-axis: 100V/div; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace Y-axis: 100V/div; Difference of 3-level inverter-A and two-level inverter-B pole voltages ($V_{A2O}$ - $V_{A3O'}$), Bottom trace Y-axis: 50V/div; Two-level inverter-B pole voltage ($V_{A3O'}$) (Experimental result: $m$=0.4; $f^*_m$ =20Hz) ..... 201

Fig. 7.15: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A2A3}$ (b) Current $i_{A2A3}$ (Experimental result: $m$=0.4; $f^*_m$ =20Hz)..... 201
Fig. 7.16: (a) Motor phase-A, voltage $V_{A2A3}$ (upper trace) and current $i_{A2A3}$ (lower trace) of 5-level inverter fed open-end IM drive at no load (b) Top trace; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace; Difference of 3-level inverter-A and two-level inverter-B pole voltages ($V_{A2O}$ - $V_{A3O'}$), Bottom trace; Two-level inverter-B pole voltage ($V_{A3O'}$) (Simulation result: $m$=0.4; $f^*_m$ =20Hz)..... 202
Fig. 7.17: (a) Motor phase-A, voltage $V_{A2A3}$ (upper trace Y-axis: 40V/div) and current $i_{A2A3}$ (lower trace Y-axis: 1A/div) of 5-level inverter fed open-end IM drive at no load (b) Top trace Y-axis: 100V/div; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace Y-axis: 100V/div; Difference of 3-level inverter-A and two-level inverter-B pole voltages ($V_{A2O}$ - $V_{A3O'}$), Bottom trace Y-axis: 50V/div; Two-level inverter-B pole voltage ($V_{A3O'}$) (Experimental result: $m$=0.6; $f^*_m$ =30Hz)..... 204
Fig. 7.18: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A2A3}$ (b) Current $i_{A2A3}$ (Experimental result: $m$=0.6; $f^*_m$ =30Hz)..... 204
Fig. 7.19: (a) Motor phase-A, voltage $V_{A2A3}$ (upper trace) and current $i_{A2A3}$ (lower trace) of 5-level inverter fed open-end IM drive at no load (b) Top trace; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace; Difference of 3-level inverter-A and two-level inverter-B pole voltages ($V_{A2O}$ - $V_{A3O'}$), Bottom trace; Two-level inverter-B pole voltage ($V_{A3O'}$) (Simulation result: $m$=0.6; $f^*_m$ =30Hz)..... 205
Fig. 7.20: (a) Motor phase-A, voltage $V_{A2A3}$ (upper trace Y-axis: 50V/div) and current $i_{A2A3}$ (lower trace Y-axis: 1A/div) of 5-level inverter fed open-end IM drive at no load (b) Top trace Y-axis: 100V/div; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace Y-axis: 100V/div; Difference of 3-level inverter-A and two-level inverter-B pole voltages ($V_{A2O}$ - $V_{A3O'}$), Bottom trace Y-axis: 50V/div; Two-level inverter-B pole voltage ($V_{A3O'}$) (Experimental result: $m$=0.8; $f^*_m$ =40Hz)..... 206
Fig. 7.21: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A2A3}$ (b) Current $i_{A2A3}$ (Experimental result: $m$=0.8; $f^*_m$ =40Hz)..... 206
Fig. 7.22: (a) Motor phase-A, voltage $V_{A2A3}$ (upper trace) and current $i_{A2A3}$ (lower trace) of 5-level inverter fed open-end IM drive at no load (b) Top trace; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace; Difference of 3-level inverter-A and two-level inverter-B pole voltages ($V_{A2O}$ - $V_{A3O'}$), Bottom trace; Two-level inverter-B pole voltage ($V_{A3O'}$) (Simulation result: $m$=0.8; $f^*_m$ =40Hz)..... 207
Fig. 7.23: Motor phase-A voltage $V_{A2A3}$ (upper trace Y-axis: 80V/div) and current $i_{A2A3}$ (lower trace Y-axis: 3A/div) waveforms under sudden change in operation from (a) two-level to 5-level at no-load (b) 5-level to two-level at no-load (Experimental result)..... 208

Fig. 7.24: (a) Motor phase-A voltage $V_{A2A3}$ (upper trace) and current $i_{A2A3}$ (lower trace) waveforms under sudden change in operation from two-level to 5-level at no-load (b) Motor phase-A voltage $V_{A2A3}$ (upper trace) and current $i_{A2A3}$ (lower trace) waveforms under sudden change in operation from 5-level to two-level at no-load (Simulation result) ..... 209
Fig. 7.25: (a) Motor phase-A, voltage $V_{A2A4}$ (upper trace Y-axis: 20V/div) and current $i_{A2A4}$ (lower trace Y-axis: 1A/div) of 9-level inverter fed open-end IM drive at no load (b) Top trace Y-axis: 100V/div; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace Y-axis: 50V/div; Difference of 3-level inverter-A and inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$), Bottom trace Y-axis: 50V/div; 3-level inverter-B pole voltage ($V_{A4O'}$) (Experimental result: $m$=0.16; $f^*_m$ =8Hz; 3-level mode) ..... 212
Fig. 7.26: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A2A4}$ (b) Current $i_{A2A4}$ (Experimental result: $m$=0.16; $f^*_m$ =8Hz; 3-level mode) ..... 213
Fig. 7.27: (a) Motor phase-A, voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) of 9-level inverter fed open-end IM drive (b) Top trace; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace; Difference of 3-level inverter-A and inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$), Bottom trace; 3-level inverter-B pole voltage ($V_{A4O'}$) (Simulation result: $m$=0.16; $f^*_m$ =8Hz; 3-level mode) ..... 214
Fig. 7.28: (a) Motor phase-A, voltage $V_{A2A4}$ (upper trace Y-axis: 30V/div) and current $i_{A2A4}$ (lower trace Y-axis: 1A/div) of 9-level inverter fed open-end IM drive at no load (b) Top trace Y-axis: 100V/div; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace Y-axis: 50V/div; Difference of 3-level inverter-A and inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$), Bottom trace Y-axis: 50V/div; 3-level inverter-B pole voltage ($V_{A4O'}$) (Experimental result: $m$=0.28; $f^*_m$ =14Hz; 4-level mode) ..... 215
Fig. 7.29: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A2A4}$ (b) Current $i_{A2A4}$ (Experimental result: $m$=0.28; $f^*_m$ =14Hz; 4-level mode) ..... 215
Fig. 7.30: (a) Motor phase-A, voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) of 9-level inverter fed open-end IM drive at no load (b) Top trace; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace; Difference of 3-level inverter-A and inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$), Bottom trace; 3-level inverter-B pole voltage ($V_{A4O'}$) (Simulation result: $m$=0.28; $f^*_m$ =14Hz; 4-level mode) ..... 216
Fig. 7.31: (a) Motor phase-A, voltage $V_{A2A4}$ (upper trace Y-axis: 35V/div) and current $i_{A2A4}$ (lower trace Y-axis: 1A/div) of 9-level inverter fed open-end IM drive at no load (b) Top trace Y-axis: 100V/div; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace Y-axis: 50V/div; Difference of 3-level inverter-A and inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$), Bottom trace Y-axis: 50V/div; 3-level inverter-B pole voltage ($V_{A4O'}$) (Experimental result: $m$=0.36; $f^*_m$ =18Hz; 5-level mode) ..... 218

Fig. 7.32: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A2A4}$ (b) Current $i_{A2A4}$ (Experimental result: $m$=0.36; $f^*_m$ =18Hz; 5-level mode) ..... 218
Fig. 7.33: (a) Motor phase-A, voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) of 9-level inverter fed open-end IM drive at no load (b) Top trace; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace; Difference of 3-level inverter-A and inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$), Bottom trace; 3-level inverter-B pole voltage ($V_{A4O'}$) (Simulation result: $m$=0.36; $f^*_m$ =18Hz; 5-level mode) ..... 219
Fig. 7.34: (a) Motor phase-A, voltage $V_{A2A4}$ (upper trace Y-axis: 40V/div) and current $i_{A2A4}$ (lower trace Y-axis: 1A/div) of 9-level inverter fed open-end IM drive at no load (b) Top trace Y-axis: 100V/div; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace Y-axis: 50V/div; Difference of 3-level inverter-A and inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$), Bottom trace Y-axis: 50V/div; 3-level inverter-B pole voltage ($V_{A4O'}$) (Experimental result: $m$=0.42; $f^*_m$ =21Hz; 6-level mode) ..... 220
Fig. 7.35: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A2A4}$ (b) Current $i_{A2A4}$ (Experimental result: $m$=0.42; $f^*_m$ =21Hz; 6-level mode) ..... 220
Fig. 7.36: (a) Motor phase-A, voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) of 9-level inverter fed open-end IM drive at no load (b) Top trace; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace; Difference of 3-level inverter-A and inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$), Bottom trace; 3-level inverter-B pole voltage ($V_{A4O'}$) (Simulation result: $m$=0.42; $f^*_m$ =21Hz; 6-level mode) ..... 221
Fig. 7.37: (a) Motor phase-A, voltage $V_{A2A4}$ (upper trace Y-axis: 50V/div) and current $i_{A2A4}$ lower trace Y-axis: 1A/div) of 9-level inverter fed open-end IM drive at no load (b) Top trace Y-axis: 100V/div; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace Y-axis: 50V/div; Difference of 3-level inverter-A and inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$), Bottom trace Y-axis: 50V/div; 3-level inverter-B pole voltage ($V_{A4O'}$) (Experimental result: $m$=0.52; $f^*_m$ =26Hz; 7-level mode) ..... 223
Fig. 7.38: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A2A4}$ (b) Current $i_{A2A4}$ (Experimental result: $m$=0.52; $f^*_m$ =26Hz; 7-level mode) ..... 223
Fig. 7.39: (a) Motor phase-A, voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) of 9-level inverter fed open-end IM drive at no load (b) Top trace; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace; Difference of 3-level inverter-A and inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$), Bottom trace; 3-level inverter-B pole voltage ($V_{A4O'}$) (Simulation result: $m$=0.52; $f^*_m$ =26Hz; 7-level mode) ..... 224
Fig. 7.40: (a) Motor phase-A, voltage $V_{A2A4}$ (upper trace Y-axis: 20V/div) and current $i_{A2A4}$ (lower trace Y-axis: 1A/div) of 9-level inverter fed open-end IM drive at no load (b) Top trace Y-axis: 100V/div; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace Y-axis: 50V/div; Difference of 3-level inverter-A and inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$), Bottom

trace Y-axis: 50V/div; 3-level inverter-B pole voltage ($V_{A4O'}$) (Experimental result: $m$=0.8; $f^*_m$ =40Hz; 9-level mode)..... 225
Fig. 7.41: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A2A4}$ (b) Current $i_{A2A4}$ (Experimental result: $m$=0.8; $f^*_m$ =40Hz; 9-level mode) ..... 225
Fig. 7.42: (a) Motor phase-A, voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) of 9-level inverter fed open-end IM drive at no load (b) Top trace; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace; Difference of 3-level inverter-A and inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$), Bottom trace; 3-level inverter-B pole voltage ($V_{A4O'}$) (Simulation result: $m$=0.8; $f^*_m$ =40Hz; 9-level mode)..... 226
Fig. 7.43: Motor phase-A voltage $V_{A2A4}$ (upper trace Y-axis: 100V/div) and current $i_{A2A4}$ (lower trace Y-axis: 3A/div) waveforms under sudden change in operation from (a) 3-level to 9-level at no-load (b) 9-level to 3-level at no-load (Experimental result) ..... 227
Fig. 7.44: (a) Motor phase-A voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) waveforms under sudden change in operation from 3-level to 9-level at no-load (b) Motor phase-A voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) waveforms under sudden change in operation from 9-level to 3-level at no-load (Simulation result) .... 228
Fig. 7.45: (a) Trace-1: Y-axis= 25V/div; Motor phase-A voltage $V_{A1A2}$ , Trace-2: Y-axis= 1A/div; phase-A current $i_{A1A2}$, Trace-3: Y-axis=2V/div; Ripple in capacitor voltage $V_{CA1}$, Trace-4: Y-axis=2V/div; Ripple in capacitor voltage $V_{CA2}$ (b) Top trace Y-axis: 50V/div; 5-level inverter-A pole voltage ($V_{A1O}$), Middle trace Y-axis: 50V/div; Difference of inverter-A and inverter-B pole voltages ($V_{A1O}$ - $V_{A2O'}$), Bottom trace Y-axis: 100V/div; 2-level inverter-B pole voltage ($V_{A2O'}$) (Experimental result: $m$=0.16; $f^*_m$ =8Hz; 3-level mode) ..... 231
Fig. 7.46: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A1A2}$ (b) Current $i_{A1A2}$ (Experimental result: $m$=0.16; $f^*_m$ =8Hz; 3-level mode) ..... 231
Fig. 7.47: (a) Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A2A4}$ (lower trace) (b) Capacitors voltages $V_{CA1}$ (upper trace) and $V_{CA2}$ (lower trace) (Simulation result: $m$=0.16; $f^*_m$ =8Hz; 3-level mode) ..... 232
Fig. 7.48: Top trace; 5-level inverter-A pole voltage ($V_{A1O}$), Middle trace; Difference of inverter-A and inverter-B pole voltages ($V_{A1O}$ - $V_{A2O'}$), Bottom trace; 2-level inverter-B pole voltage ($V_{A2O'}$) (Simulation result: $m$=0.16; $f^*_m$ =8Hz; 3-level mode) ..... 233
Fig. 7.49: (a) Trace-1: Y-axis= 30V/div; Motor phase-A voltage $V_{A1A2}$, Trace-2: Y-axis= 1A/div; phase-A current $i_{A1A2}$, Trace-3: Y-axis=2V/div; Ripple in capacitor voltage $V_{CA1}$, Trace-4: Y-axis=2V/div; Ripple in capacitor voltage $V_{CA2}$ (b) Top trace Y-axis: 50V/div; 5-level inverter-A pole voltage ($V_{A1O}$), Middle trace Y-axis: 50V/div; Difference of inverter-A and inverter-B pole voltages ($V_{A1O}$ - $V_{A2O'}$), Bottom trace Y-axis: 100V/div; 2-level inverter-B pole voltage ($V_{A2O'}$) (Experimental result: $m$=0.28; $f^*_m$ =14Hz; 4-level mode)..... 234

Fig. 7.50: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A1A2}$ (b) Current $i_{A1A2}$ (Experimental result: $m$=0.28; $f^*_m$ =14Hz; 4-level mode) ..... 234
Fig. 7.51: (a) Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A2A4}$ (lower trace) (b) Capacitors voltages $V_{CA1}$ (upper trace) and $V_{CA2}$ (lower trace) (Simulation result: $m$=0.28; $f^*_m$ =14Hz; 4-level mode) ..... 235
Fig. 7.52: Top trace; 5-level inverter-A pole voltage ($V_{A1O}$), Middle trace; Difference of inverter-A and inverter-B pole voltages ($V_{A1O}$ - $V_{A2O'}$), Bottom trace; 2-level inverter-B pole voltage ($V_{A2O'}$) (Simulation result: $m$=0.28; $f^*_m$ =14Hz; 4-level mode)..... 236
Fig. 7.53: (a) Trace-1: Y-axis= 35V/div; Motor phase-A voltage $V_{A1A2}$, Trace-2: Y-axis= 1A/div; phase-A current $i_{A1A2}$, Trace-3: Y-axis=2V/div; Ripple in capacitor voltage $V_{CA1}$, Trace-4: Y-axis=2V/div; Ripple in capacitor voltage $V_{CA2}$ (b) Top trace Y-axis: 50V/div; 5-level inverter-A pole voltage ($V_{A1O}$), Middle trace Y-axis: 50V/div; Difference of inverter-A and inverter-B pole voltages ($V_{A1O}$ - $V_{A2O'}$), Bottom trace Y-axis: 100V/div; 2-level inverter-B pole voltage ($V_{A2O'}$) (Experimental result: $m$=0.36; $f^*_m$ =18Hz; 5-level mode)..... 237
Fig. 7.54: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A1A2}$ (b) Current $i_{A1A2}$ (Experimental result: $m$=0.36; $f^*_m$ =18Hz; 5-level mode) ..... 237
Fig. 7.55: (a) Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A2A4}$ (lower trace) (b) Capacitors voltages $V_{CA1}$ (upper trace) and $V_{CA2}$ (lower trace) (Simulation result: $m$=0.36; $f^*_m$ =18Hz; 5-level mode) ..... 238
Fig. 7.56: Top trace; 5-level inverter-A pole voltage ($V_{A1O}$), Middle trace; Difference of inverter-A and inverter-B pole voltages ($V_{A1O}$ - $V_{A2O'}$), Bottom trace; 2-level inverter-B pole voltage ($V_{A2O'}$) (Simulation result: $m$=0.36; $f^*_m$ =18Hz; 5-level mode)..... 239
Fig. 7.57: (a) Trace-1: Y-axis= 40V/div; Motor phase-A voltage $V_{A1A2}$, Trace-2: Y-axis= 1A/div; phase-A current $i_{A1A2}$, Trace-3: Y-axis=2V/div; Ripple in capacitor voltage $V_{CA1}$, Trace-4: Y-axis=2V/div; Ripple in capacitor voltage $V_{CA2}$ (b) Top trace Y-axis: 50V/div; 5-level inverter-A pole voltage ($V_{A1O}$), Middle trace Y-axis: 50V/div; Difference of inverter-A and inverter-B pole voltages ($V_{A1O}$ - $V_{A2O'}$), Bottom trace Y-axis: 100V/div; 2-level inverter-B pole voltage ($V_{A2O'}$) (Experimental result: $m$=0.42; $f^*_m$ =21Hz; 6-level mode)..... 240
Fig. 7.58: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A1A2}$ (b) Current $i_{A1A2}$ (Experimental result: $m$=0.42; $f^*_m$ =21Hz; 6-level mode) ..... 240
Fig. 7.59: (a) Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A2A4}$ (lower trace) (b) Capacitors voltages $V_{CA1}$ (upper trace) and $V_{CA2}$ (lower trace) (Simulation result: $m$=0.42; $f^*_m$ =21Hz; 6-level mode) ..... 241
Fig. 7.60: Top trace; 5-level inverter-A pole voltage ($V_{A1O}$), Middle trace; Difference of inverter-A and inverter-B pole voltages ($V_{A1O}$ - $V_{A2O'}$), Bottom trace; 2-level inverter-B pole voltage ($V_{A2O'}$) (Simulation result: $m$=0.42; $f^*_m$ =21Hz; 6-level mode)..... 242

Fig. 7.61: (a) Trace-1: Y-axis= 50V/div; Motor phase-A voltage $V_{A1A2}$, Trace-2: Y-axis= 1A/div; phase-A current $i_{A1A2}$, Trace-3: Y-axis=2V/div; Ripple in capacitor voltage $V_{CA1}$, Trace-4: Y-axis=2V/div; Ripple in capacitor voltage $V_{CA2}$ (b) Top trace Y-axis: 50V/div; 5-level inverter-A pole voltage ($V_{A1O}$), Middle trace Y-axis: 50V/div; Difference of inverter-A and inverter-B pole voltages ($V_{A1O}$ - $V_{A2O'}$), Bottom trace Y- axis: 50V/div; 2-level inverter-B pole voltage ($V_{A2O'}$) (Experimental result: $m$=0.52; $f^*_m$ =26Hz; 7-level mode) ..... 243
Fig. 7.62: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A1A2}$ (b) Current $i_{A1A2}$ (Experimental result: $m$=0.52; $f^*_m$ =26Hz; 7-level mode) ..... 243
Fig. 7.63: (a) Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A2A4}$ (lower trace) (b) Capacitors voltages $V_{CA1}$ (upper trace) and $V_{CA2}$ (lower trace) (Simulation result: $m$=0.52; $f^*_m$ =26Hz; 7-level mode) ..... 244
Fig. 7.64: Top trace; 5-level inverter-A pole voltage ($V_{A1O}$), Middle trace; Difference of inverter-A and inverter-B pole voltages ($V_{A1O}$ - $V_{A2O'}$), Bottom trace; 2-level inverter-B pole voltage ($V_{A2O'}$) (Simulation result: $m$=0.52; $f^*_m$ =26Hz; 7-level mode) ..... 245
Fig. 7.65: (a) Trace-1: Y-axis= 75V/div; Motor phase-A voltage $V_{A1A2}$ , Trace-2: Y-axis= 1A/div; phase-A current $i_{A1A2}$, Trace-3: Y-axis=2V/div; Ripple in capacitor voltage $V_{CA1}$, Trace-4: Y-axis=2V/div; Ripple in capacitor voltage $V_{CA2}$ (b) Top trace Y-axis: 50V/div; 5-level inverter-A pole voltage ($V_{A1O}$), Middle trace Y-axis: 50V/div; Difference of inverter-A and inverter-B pole voltages ($V_{A1O}$ - $V_{A2O'}$), Bottom trace Y-axis: 100V/div; 2-level inverter-B pole voltage ($V_{A2O'}$) (Experimental result $m$=0.8; $f^*_m$ =40Hz; 9-level mode) ..... 246
Fig. 7.66: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A1A2}$ (b) Current $i_{A1A2}$ (Experimental result $m$=0.8; $f^*_m$ =40Hz; 9-level mode) ..... 246
Fig. 7.67: (a) Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A2A4}$ (lower trace) (b) Capacitors voltages $V_{CA1}$ (upper trace) and $V_{CA2}$ (lower trace) (Simulation result $m$=0.8; $f^*_m$ =40Hz; 9-level mode) ..... 247
Fig. 7.68: Top trace; 5-level inverter-A pole voltage ($V_{A1O}$), Middle trace; Difference of inverter-A and inverter-B pole voltages ($V_{A1O}$ - $V_{A2O'}$), Bottom trace; 2-level inverter-B pole voltage (Simulation result $m$=0.8; $f^*_m$ =40Hz; 9-level mode) ..... 248
Fig. 7.69: Trace-1: Y-axis= 100V/div; Motor phase-A voltage $V_{A1A2}$ , Trace-2: Y-axis= 3A/div; phase-A current $i_{A1A2}$, Trace-3: Y-axis=50V/div; Capacitor voltage $V_{CA1}$, Trace-4: Y-axis=25V/div; Capacitor voltage $V_{CA2}$ (a) 3-level to 9-level at no-load (b) 9-level to 3-level at no-load (Experimental result) ..... 249
Fig. 7.70: Motor phase-A voltage $V_{A1A2}$, current $i_{A1A2}$, capacitors voltages $V_{CA1}$ and $V_{CA2}$ under sudden change in operation from 3-level to 9-level at no-load (Simulation result) ..... 249
Fig. 7.71: Motor phase-A voltage $V_{A1A2}$, current $i_{A1A2}$, capacitors voltages $V_{CA1}$ and $V_{CA2}$ under sudden change in operation from 9-level to 3-level at no-load (Simulation result) ..... 250

Fig. 7.72: Effect of disabling the capacitor voltage balancing algorithm on phase voltage and current (a) Experimental results ; Trace-1: Y-axis= 150V/div; Motor phase-A voltage $V_{A1A2}$ , Trace-2: Y-axis= 1A/div; phase-A current $i_{A1A2}$, Trace-3: Y-axis=100V/div; Capacitor voltage $V_{CA1}$, Trace-4: Y-axis=100V/div; Capacitor voltage $V_{CA2}$ (b) Simulation results ..... 251

## LIST OF TABLES

Table 1.1: Comparison of power components requirements in conventional MLIs ..... 11
Table 1.2: The most appropriate control scheme matching diagram according to topologies . 21
Table 1.3: Multilevel inverter application summary based on topology ..... 23
Table 2.1: Switching states of inverter-1 and inverter-2 to realised three-levels in phase- A 33
Table 2.2: Effect of switching frequency on THD of motor phase-A voltage ..... 42
Table 3.1: Five levels realised in phase- A for combinations of pole voltages of inverter-A and inverter-B ..... 55
Table 3.2: Switching states of phase-A related switches of all two-level inverters for 5-level operation ..... 55
Table 3.3: Switching states of phase-A related switches of all two-level inverters for 6-level operation ..... 59
Table 3.4: Performance comparison of 5-level inverter with D2L inverter ..... 73
Table 4.1: Comparison of nine-level inverter topologies ..... 77
Table 4.2: Nine levels realised in phase-A for combinations of pole voltages of inverter-A and inverter-B ..... 78
Table 4.3: Switching states of phase-A related switches of all the four inverters for nine-level operation ..... 79
Table 4.4: Maximum magnitude of reference phasor $V^*_s$ in different operating regions ..... 86
Table 4.5: Summary of simulation results of 9-level inverter obtained at different modulation indices ..... 110
Table 4.6: Performance comparison of 9-level inverter with 5-level inverter ..... 111
Table 5.1: Comparison of nine-level inverter topologies ..... 116
Table 5.2: Switching states to realize nine voltage levels in phase-A and effect on capacitors ... 117
Table 5.3: Switching states for space-vector sector of 60º interval ..... 131
Table 5.4: Summary of simulation results of hybrid 9-level inverter obtained at different modulation indices ..... 161
Table 5.5: Performance comparison of hybrid 9-level inverter with 9-level inverter ..... 162
Table 6.1: Switching states to realized eighteen–levels in phase-A ..... 167
Table 6.2: Comparison of 18-level inverter topologies ..... 169
Table 6.3: Determination of region and phase voltage level from modulating signal ..... 171
Table 6.4: Performance comparisons of 18-level inverter with hybrid 9-level inverter ..... 185
Table 7.1: Comparison of experimental and downscaled simulation results of 5-level inverter ... 210
Table 7.2: Comparison of experimental and downscaled simulation results of proposed 9-level inverter ..... 229
Table 7.3: Comparison of experimental and downscaled simulation results of proposed hybrid 9-level inverter ..... 252

## LIST OF ACRONYMS

| | |
|---|---|
| ACHB | Asymmetrical Cascade H-bridge |
| APOD | Alternative Phase Opposition Disposition |
| ASD | Adjustable Speed Drive |
| CHB | Cascade H-Bridge |
| D2L | Dual Two-Level |
| DAC | Digital to Aanalog Converters |
| DC | Direct Current |
| DCMLI | Diode Clamped Multilevel Inverter |
| DSTATCOM | Distribution Static Compensator |
| DTC | Direct Torque Control |
| EMC | Electro Magnetic Compatibility |
| EMI | Electro Magnetic Interference |
| FACTS | Flexible AC Transmission System |
| FCMLI | Flying Capacitor Multilevel Inverter |
| FLC | Feedback Linearization Control |
| FOC | Field Oriented Control |
| HCC | Hysteresis Current Control |
| HIL | Hardware In Loop |
| HVDC | High Voltage Direct Current |
| IM | Induction Motor |
| IMD | Induction Motor Drive |
| LSPWM | Level Shifted Pulse Width Modulation |
| MLI | Multilevel Inverter |
| MMF | Magneto Motive Force |
| MOV | Metal Oxide Varistor |
| MRAS | Model Reference Adaptive System |
| NPC | Neutral Point Clamped |
| OHSPWM | Optimized Harmonics Stepped Pulse Width Modulation |
| PD | Phase Disposition |
| POD | Phase Opposition Disposition |
| PS | Phase Shifted |
| SDPWM | Sigma Delta Pulse Width Modulation |
| SPWM | Sinusoidal Pulse Width Modulation |
| SHE | Selective Harmonic Elimination |
| SVPWM | Space Vector Pulse Width Modulation |

| | |
|---|---|
| UVLO | Under Voltage Lockout |
| VFD | Variable Frequency Drive |

## LIST OF SYMBOLS

| | |
|---|---|
| $\psi^s_{qs}$ , $\psi^s_{ds}$ | Stator q-axis and d-axis flux linkage per second |
| $\psi'^s_{qr}$ , $\psi'^s_{dr}$ | Rotor q-axis and d-axis flux linkage per second referred to stator side |
| $\psi^s_{md}$ , $\psi^s_{mq}$ | Motor q-axis and d-axis mutual flux linkage per second |
| $f_c$ | Switching frequency |
| $f^*_m$ | Frequency of reference phase voltage |
| $i_{A1A2}$ | Motor phase-A current |
| $i^s_{qr}$ , $i^s_{dr}$ | Rotor q-axis and d-axis current component in stationary reference frame |
| $i^s_{qs}$ , $i^s_{ds}$ | Stator q-axis and d-axis current component in stationary reference frame |
| $J$ | Motor moment of inertia |
| $m$ | Modulation index |
| $N_s$ , $N_r$ | Number of turns in stator and rotor windings |
| $P$ | Number of poles of induction motor |
| $PU$ | Per unit |
| $SF_X$ | Switching function applied to phase-X |
| $SF_a$, $SF_b$, $SF_c$ | Switching functions for phase- A, B, C |
| $T_{em}$ | Electromagnetic torque |
| $T_{load}$ | Load torque |
| $V^*_a$, $V^*_b$, $V^*_c$ | Three reference waves |
| $V_{A1A2}$, $V_{B1B2}$, $V_{C1C2}$ | Three-phase motor voltages |
| $V_{A1O}$, $V_{B1O}$, $V_{C1O}$ | Three phase Inverter-1 pole voltages |
| $V_{A2O}$, $V_{B2O}$, $V_{C2O}$ | Three phase Inverter-2 pole voltages |
| $V_{A3O'}$, $V_{B3O'}$, $V_{C3O'}$ | Three phase Inverter-3 pole voltages |
| $V_{A4O'}$, $V_{B4O'}$, $V_{C4O'}$ | Three phase Inverter-4 pole voltages |
| $V_{AB}$, $V_{BC}$, $V_{CA}$ | Three phase line voltages |
| $V_{CA1}$, $V_{CA2}$ | Phase-A capacitors voltages |
| $V_{CB1}$, $V_{CB2}$ | Phase-B capacitors voltages |
| $V_{CC1}$, $V_{CC2}$ | Phase-C capacitors voltages |
| $\Delta V_{CA1}$, $\Delta V_{CA2}$ | Ripples in phase-A capacitors voltages |
| $\Delta V_{CB1}$, $\Delta V_{CB2}$ | Ripples in phase-B capacitors voltages |
| $\Delta V_{CC1}$, $\Delta V_{CC2}$ | Ripples in phase-C capacitors voltages |
| $V_{DC}$ | DC Link Voltage |

| | |
|---|---|
| $V_r^*$ | Reference voltage space phasor |
| $V_{A1A2}$ , | Motor phase-A voltage |
| $V_{OO'}$ | Common mode voltage |
| $V_s$ | Voltage space vector |
| $v_{qs}^s$ , $v_{ds}^s$ | Stator q-axis and d-axis voltage component |
| $v'^s_{qr}$ , $v'^s_{dr}$ | Rotor q-axis and d-axis voltage component referred to stator side |
| $\omega_b$ | Rated angular frequency |
| $\omega_r$ | Rotor speed |

# CHAPTER 1: INTRODUCTION AND LITERATURE REVIEW

*[This chapter describes problems faced by conventional two-level inverter fed medium voltage IM drives, their possible solutions as well as the features and the technical challenges of MLIs. A comprehensive literature survey on MLIs is given in detail. Finally, scope of work, author's contribution and thesis outlines are presented.]*

## 1.1 Overview

Conversion from electrical energy to mechanical energy is an important process in modern industrial civilization and it is done by means of electrical machines. Typical applications of electrical machine drives are in industrial drives for motion control and in automotive control (electric vehicles).

Over a period of more than 40 years induction motor (IM) has become widely used motor in industry and replaced DC motor in most of the applications due to advantages as listed below:

- Robustness
- No commutator and brushes
- Simpler protection and maintenance free
- Lower rotor inertia
- Smaller size and weight,
- Lower price

A wide range of speed control of IM requires variable frequency and variable voltage supply which necessitates complex control of induction motor drives. However, the advantages of IM override the issue of complex control.

The development of high power converter and medium voltage (MV) drives started in the mid 1980's after commercialization of MV power semiconductor devices [1]. The effort in advancing the technology has led to significant acceptance of MV drives in recent years. The GTO was the standard for the MV drive until the IGBT and IGCT emerged as viable solutions in late 1990s [2, 3]. These power semiconductor devices have rapidly progressed into the main areas of high-power electronics due to the superior switching characteristics, reduced power losses, ease of gate control and snubber less operation [4]. The high-power MV drives have pervasive applications in the industries. The drives in MV range cover power ratings from fraction of MW to few tens of MW at the medium voltage level of 2.3 kV to 13.8 kV. However, the majority of the installed MV drives are in the 1-to 4-MW range with voltage rating from 3.3 kV to 6.6 kV [4]. It has been reported in literature that 97% of the installed MV induction motors operate at a fixed speed and only 3% are controlled by variable speed drives [5]. Large amount of energy saving can be obtained by employing ASD (Adjustable

Speed Drive) where variable speed is required. The use of MV drive can give payback time of the investment from 1 to 2.5 years [6].

Voltage source inverters (VSIs) are well proven as a standard configuration for the PWM inverter drives due to availability of fast power semiconductor devices, high dynamic response and good spectral performance [7]. Current Source Inverter (CSI) drives give limited dynamic performance. VSI drives require only a simple diode bridge as a front-end converter whereas, CSI drives require active frontend converter to supply controlled current source to drive. The DC-link chock required in CSI drive offers short-circuit protection, at the same time it increases size, volume and weight. The output capacitors required in CSI drive can lead to resonance with motor. On the other side minimum cost, compact size, high dynamic response, good spectral performance, high efficiency and high reliability for rectifying state in VSI drives elect them as standard configurations over CSI drives. It is shown in literature that the three level NPC VSI drive achieves higher efficiency as compared to CSI drive [8]. In two-level VSIs high frequency PWM (Pulse Width Modulation) techniques are used to improve the quality of output voltage waveform. The high frequency PWM suffers from problems like higher switching losses, high dv/dt, higher common-mode voltages, more EMI/EMC etc. The reduction of switching frequency usually causes an increase in the harmonic distortion of the line-side and motor-side waveforms of the drive. At the same time, industry has begun to demand higher power equipment, which now reached up to megawatt level. Controlled AC drives in the megawatt range are usually connected to the medium-voltage network. Currently, medium voltage drives cover voltages from 2.3 kV- 7.2 kV. The output power ranges from approximately 200 kW to as high as 12 MW, so it is difficult to connect a single power semiconductor switch directly to medium-voltage grids [1]. The problems associated to high frequency PWM inverter become more pronounced at high power levels. For these reasons, a new family of multilevel inverters has emerged as the solution for working at higher voltage levels with minimum waveform distortion at limited switching frequencies [1, 8].

## 1.2 Inverter Topologies for Induction Motor Drives

There are two possible solutions for the inverters operated in high power medium-voltage range; one is conventional two-level inverter with series connection of switching devices and the other is multilevel inverter (MLI). The first solution is complex even with fast switching devices due to requirement of accurate static and dynamic voltage sharing of the series devices and therefore, MLIs are preferred in such applications.

### 1.2.1 Conventional Two-Level Inverter

Two-level voltage source inverter is a well-known inverter topology for low-voltage (≤600 V) drives. This technology has been extended to the MV drives, which are

commercially available for the power rating up to a few megawatts [10]. The power circuit of conventional two-level MV VSI drive is shown in Fig. 1.1. The inverter consists of 12 IGBTs (Insulated Gate Bipolar Transistor) with four IGBTs per inverter leg and two IGBTs per inverter branch. In order to reduce voltage per switching device, series connections of the switches are used. The number of series connected switches (IGBTs) depends upon the terminal voltage level of drive. The DC-link voltage for inverter configuration can be obtained by 6, 12 or 24 pulse diode rectifier. In applications with more stringent harmonic requirements, the higher pulse number diode rectifiers can be used. Bhim Singh, et al. discussed the detailed analysis on the multi-pulse diode rectifier and active front-end converters [11]. The multi-pulse diode rectifier can be replaced by an active front-end for four-quadrant operation or regenerative braking. The DC-link capacitors are normally of oil-filled type instead of electrolytic types which are commonly used in the low-voltage VSI drives; due to limited voltage ratings of electrolytic type.

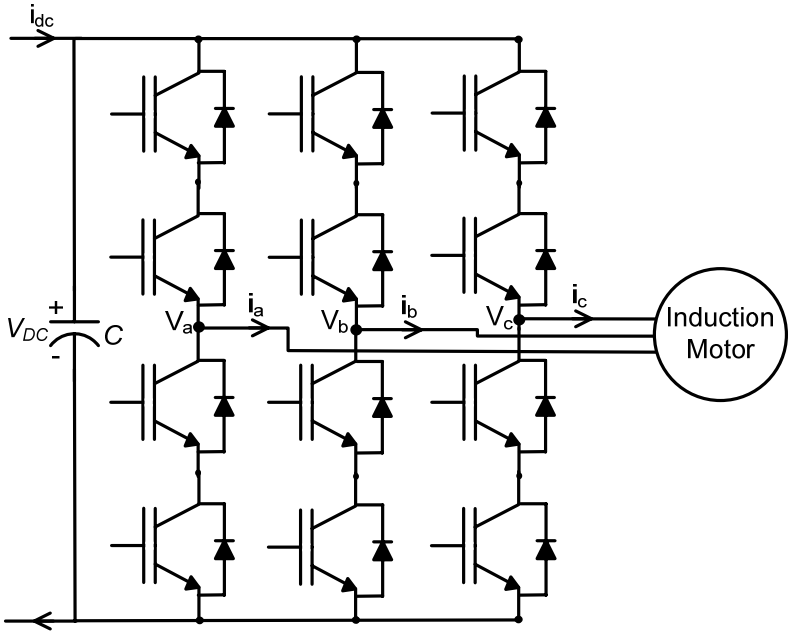



Fig. 1.1: Power circuit of conventional two-level MV VSI drive

The two-level inverter fed MV induction motor drive has number of advantages including simple converter topology, simple PWM scheme and ease of DC capacitor recharging. On contrary, it has several problems at high switching frequency, which are listed below [9, 11, 12]:

1. Fast switching speed of semiconductor devices generates high *dv/dt*. Therefore, waveform reflections at the rising and falling edges of the inverter output voltage results in premature failure of motor winding insulation due to partial discharges.

High switching also induces rotor shaft voltages and current flowing into shaft bearing leading to early bearing failure.

2. Current and voltage harmonics in the stator winding results into additional power losses in the motor winding and magnetic core. At higher power level these losses are significant. Thus, motor is derated and cannot operate at its full capacity.
3. The switching action of an inverter generates common-mode (CM) voltages, which appears on the neutral of the stator winding with respect to ground and superimposed to the phase voltage of the stator winding, resulting into premature failure of the motor winding insulation. Keeping in view the high replacement cost and loss of production in MV drives, special care should be taken to minimize common-mode voltages.
4. High EMI is associated with high switching frequency.
5. Device switching losses accounts for a significant amount of total power loss at high switching frequency and it will increase further in the MV drive. Its minimization leads to a reduction in operating and manufacturing cost as well as the cooling requirements for the switching devices.

As the two-level inverter produces high *dv*/*dt* and higher THD in its output voltage, therefore it often requires a large-size LC filter installed at its output terminals. The first two problems as listed above can be effectively taken care by adding properly designed LC filter at inverter output. The LC filter is normally installed inside the drive cabinet and connected to the inverter with short cables to avoid wave reflections. However, the use of large size LC filter causes an increase in the manufacturing cost, fundamental voltage drops and circulating current between filter and DC circuit. It may also cause LC resonances that can be excited by the harmonics in the inverter PWM output voltage.

### 1.2.2 Multilevel Inverter

Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms [9]. The commutation of the switches permits the addition of the capacitor voltages, which produces high voltage at the output, while the power semiconductors must withstand only reduced voltages. The term multilevel inverter (MLI) is specifically used for DC/AC multilevel power processing system to distinguish it from AC/DC multilevel power processing system. In some of the literature both of these power processing systems are uniquely named as multilevel converters [13, 14].

In general form of MLI different voltage levels are formed by employing several DC voltage sources through different configurations. Fig. 1.2 shows a schematic diagram of one phase leg of inverter with different numbers of levels, for which the action of the power semiconductors is represented by an ideal switch with several positions. A two-level inverter

generates an output voltage with two values (levels) with respect to the negative terminal of the DC source shown in Fig. 1.2(a), while the three-level inverter generates three voltages as shown in Fig. 1.2(b), and so on. Fig. 1.2(c) uses series-connected capacitors to generate different DC voltage level using single DC voltage source. If all capacitors are of same value then each capacitor has the same voltage $V_c$ as given by:

$$V_c = \frac{V_{dc}}{n-1} \tag{1.1}$$

Where $n$ is the number of levels in MLI. The term levels are referred to as the number of nodes to which an inverter can be accessible. An n-level inverter needs (n-1) capacitors. The output pole voltage can be defined as voltage across output terminals of the inverter and the negative terminal of the DC supply denoted as '0' as shown in Fig. 1.2. The number of levels in pole voltage is the same as that of in MLI. The number of the line-to-line voltage levels is given by k as:

$$k = 2n-1 \tag{1.2}$$

Considering a star connected load, the number of phase voltage level, p, is given by:

$$p = 2k-1 = 4n-3 \tag{1.3}$$

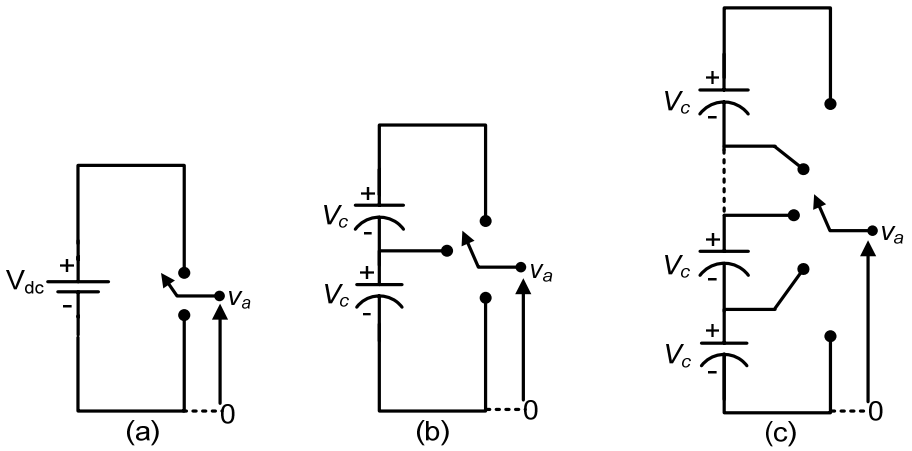



Fig. 1.2: One phase leg of an inverter with (a) two levels; (b) three levels; (c) n levels

In a 5-level inverter, it is possible to obtain pole voltage, line-to-line voltage and phase voltage levels of 5, 9 and 17 respectively. Higher the number of levels better is the quality of output voltage and a better approximation of a sinusoidal wave, but a more complex control system with respect to the two-level inverter. Some of the attractive features of MLI are as follows [4, 13, 15]:

1. They can operate with a lower switching frequency while giving same output waveform quality as compared to two-level inverter.

2. They draw input current with very low distortion.
3. MLI can generate output voltages with extremely low distortion, reduced voltage stress on switching devices and lower *dv/dt*. Hence, associated problems are substantially reduced.
4. They require more device count, but still they are compact in size because they require either reduced sized output filter or transformer or none of them.
5. Smaller common-mode (CM) voltages are generated, thus, reducing stress on motor bearings. Using sophisticated modulation methods, CM voltages can be eliminated.
6. Less EMI can be achieved in MLI due to lower switching frequency.

The various problems associated with two-level inverters, necessitate multilevel inverters as an attractive solution for high power as well as low power induction motor drives (IMDs). However, MLI has several technical challenges like large device count, DC-link voltage unbalancing, more complex circuit and control at higher level. Hence, there is a need to investigate MLIs, which have been a subject of intensive research recently. The use of multilevel inverter for installation of the MV drive can lead to a significant savings on energy cost [17]. Nowadays, there are numerous commercial MLI-ASDs are available for high power application [4]. In spite of several good features posses by MLIs for MV drives, yet they are not able to completely replace the two-level inverter due to technological problems such as reliability, efficiency, control complexity, design difficulties of easy and fast modulation methods [14].

## 1.3 Literature Review

Multilevel Inverters (MLIs) gaining popularity in many fields like power system, HVDC transmission, medium and high voltage induction motor drives, non-conventional energy sources etc. Many researchers have discussed MLIs, their control strategy, uses, advantages, disadvantages and how they can be effectively used in induction motor drive application. The significant contributions in these fields are discussed in this section.

### 1.3.1 Multilevel Inverter Topologies

The development in MLI began in the early eighties when Akira Nabae et al. [18] presented a neutral point clamped NPC PWM inverter in 1981. In this article, a new neutral-point-clamped pulse width modulation (PWM) inverter composed of main switching devices which operate as switches for PWM and auxiliary switching devices to clamp the output terminal potential to the neutral point potential has been discussed. This inverter output contains less harmonic content as compared with that of a conventional type. It was the milestone in the history of MLI. However, the concept of utilizing several levels for power conversion has been introduced in 1975 and it was based on cascaded H-bridge [19]. This

was followed by the diode clamped inverter [19, 20] which utilized a bank of series connected capacitors to generate different DC voltage level using single DC voltage source. A later invention of flying capacitor [22], the capacitors were floating instead of series-connection. Various MLI configurations are available in the literature that can be applied to replace the existing two-level inverters. The major multilevel inverter topologies are discussed in subsequent sub-sections.

#### 1.3.1.1 Diode Clamped Multilevel Inverter (DCMLI)

The diode clamped multilevel inverter (DCMLI) proposed by Nabae, Takahashi and Akagi in [18] can be considered the first real multilevel inverter. The DCMLI employs clamping diodes and series connected DC capacitors to produce AC voltage waveforms with multiple voltage levels [17, 22]. The inverter can be configured as a three, four, five or any higher-level topology, but for higher number of levels the control complexity increases exponentially [24]. Therefore, mainly three-level inverter, often known as neutral-point clamped (NPC) inverter, has found in the market [23].

Fig. 1.3 shows the circuit diagram of a three phase five-level DCMLI [4] . Each phase-leg of the inverter is composed of eight active switches (with anti-parallel diodes) from $S_1$ to $S'_4$. In practice, either IGBT or IGCT is used as a switching device. The upper and lower switches of each phase-leg form complementary pairs as ($S_1$, $S'_1$), ($S_2$, $S'_2$), ($S_3$, $S'_3$) and ($S_4$, $S'_4$). On the DC side of the inverter, four series connected capacitors are used to split the DC bus in to four parts, and provides a neutral point O. The voltage across each of the DC capacitor is $V_{dc}/4$, where $V_{dc}$ is the total DC link voltage. The diodes, connected to the DC bus capacitors are called 'clamping diodes', which limits the voltage stress across each device to $V_{dc}/4$. The voltage rating of diode $D'_1$ in Fig. 1.3 is three times the voltage rating of $D_1$ because it has to block three capacitor voltages ($3V_{dc}/4$) when all lower devices, $S'_1$ - $S'_4$ are turned ON. Similarly, $D_2$ and $D'_2$ need to block $2V_{dc}/4$, and $D_3$ needs to block $3V_{dc}/4$. Therefore, different voltage rating clamping diodes are required in DCMLI.

The DC bus capacitors in DCMLIs carry full load current, leading to DC-link capacitor voltage unbalancing and results in the neutral point fluctuation [25], . Several modulation schemes have been suggested in the literature to address the capacitor voltage unbalancing problem along with the control of the output voltage [24]-[34]. These schemes are either carrier based or space vector based control scheme.

R. Rojas, et al. [26] have reported a tight control of capacitor voltage by using a hysteresis controller that is capable of stabilizing the neutral point potential variations within fixed limits during steady and transient states. A switching frequency optimal PWM control method has been suggested in [27], which achieves the switching frequency two times the mean thyristor switching frequency permitted. A simple control circuit is proposed in [28], to address the capacitor voltage balancing for a diode-clamped multilevel inverter (DCMLI)

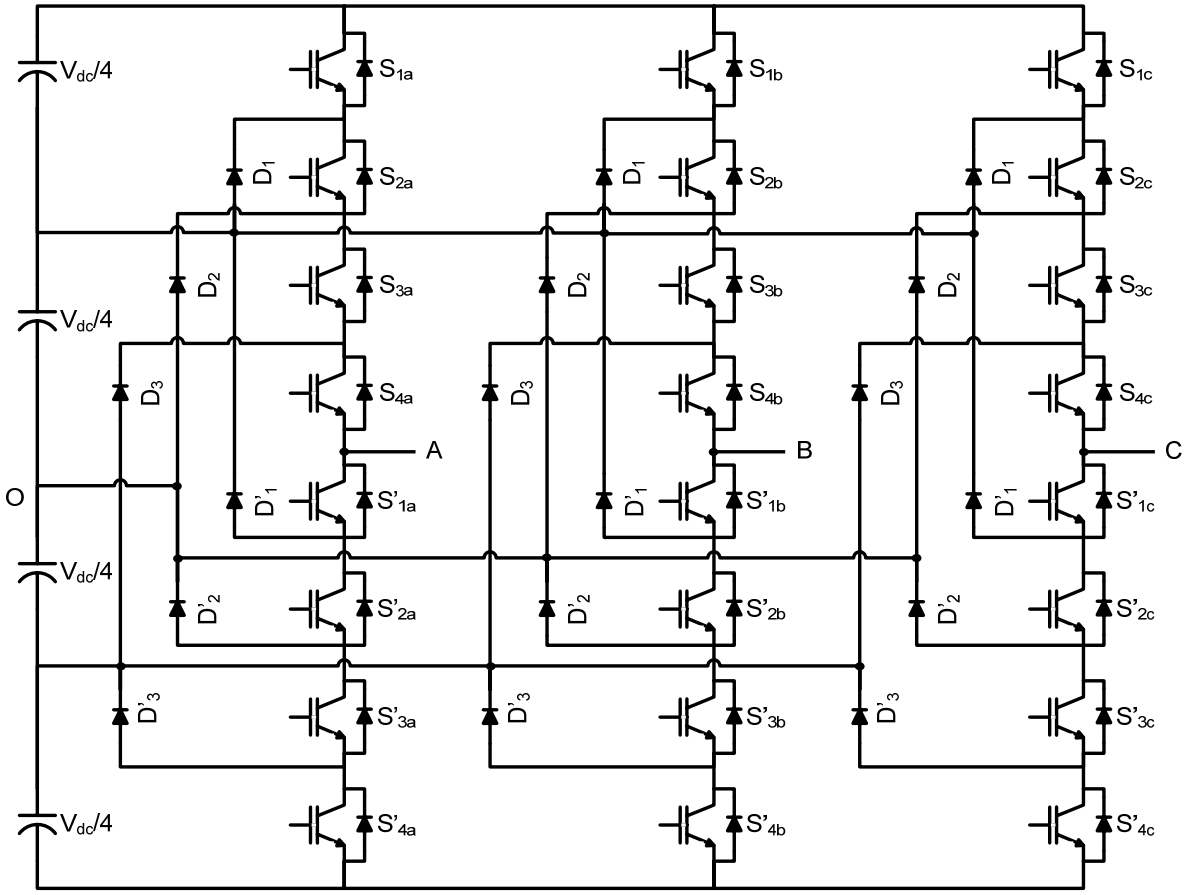



Fig. 1.3: Three-phase five-level diode clamped inverter

based distribution static compensator (DSTATCOM) connected to a three-phase, four-wire (3p4w) distribution system. A switched rectifier DC voltage source is proposed by K. Siva kumar et al. [29], for three-level neutral-point-clamped (NPC) inverter based drive system to alleviate the inverter from capacitor voltage balancing. The limiting conditions for which a four-level diode clamped inverter cannot achieve voltage balancing is explored in [30] and to avoid these limiting conditions proper redundant vectors are selected in the space-vector diagram so that a quadratic parameter related to the currents in the middle points is minimized. Some virtual space vector concept based modulation scheme are reported in literature [29, 30] which offers balancing of the neutral-point voltage over the full range of inverter output voltages and for all load power factors. A simple space vector PWM scheme for operating a three-level NPC inverter at higher modulation index, including overmodulation region, with neutral point balancing is presented in [33].

An optimal predictive control method for the NPC multilevel inverter, working as an active power filter for power quality applications is proposed in [34]. S.B. Monge, et al. [35] presented a PWM strategy for *n*-level three-phase diode clamped inverters in the overmodulation region, with dc-link capacitor voltage balance in every switching cycle. A sixth harmonic zero-sequence voltage injection based triangle carrier modulation scheme is

proposed in [36], for voltage balancing of a three-level diode-clamped converter in a transformer less hybrid active filter.

#### 1.3.1.2 Flying Capacitor Multilevel Inverter (FCMLI)

Another benchmark multilevel topology is flying capacitor multilevel inverter proposed by Meynard and Foch in 1992 [22]. This topology requires a series connection of pre-charged capacitor switching cells [8, 13]. The circuit configuration of a five-level FC inverter is depicted in Fig. 1.4. An *n*-level FC inverter requires a total of (*n*-1)×(*n*-2)/2 auxiliary capacitors per phase leg in addition to (*n*-1) main dc bus capacitors.This topology has several unique and attractive features when compared to the DCMLI. One feature is that clamping diodes as required in DCMLI are not needed. Furthermore, the FCMLI has a switching redundancy within a phase, which can be used to balance the voltages of the flying capacitors (FC) and equally distribute the switching and conduction losses of the semiconductor switches. The topology provide extra ride through capabilities during power outage. The requirement of several flying capacitors for higher level inverters makes the topology bulky, costly and less reliable. In the last few decades several modulation schemes have been reported in the literature to efficiently maintain the correct voltage across the

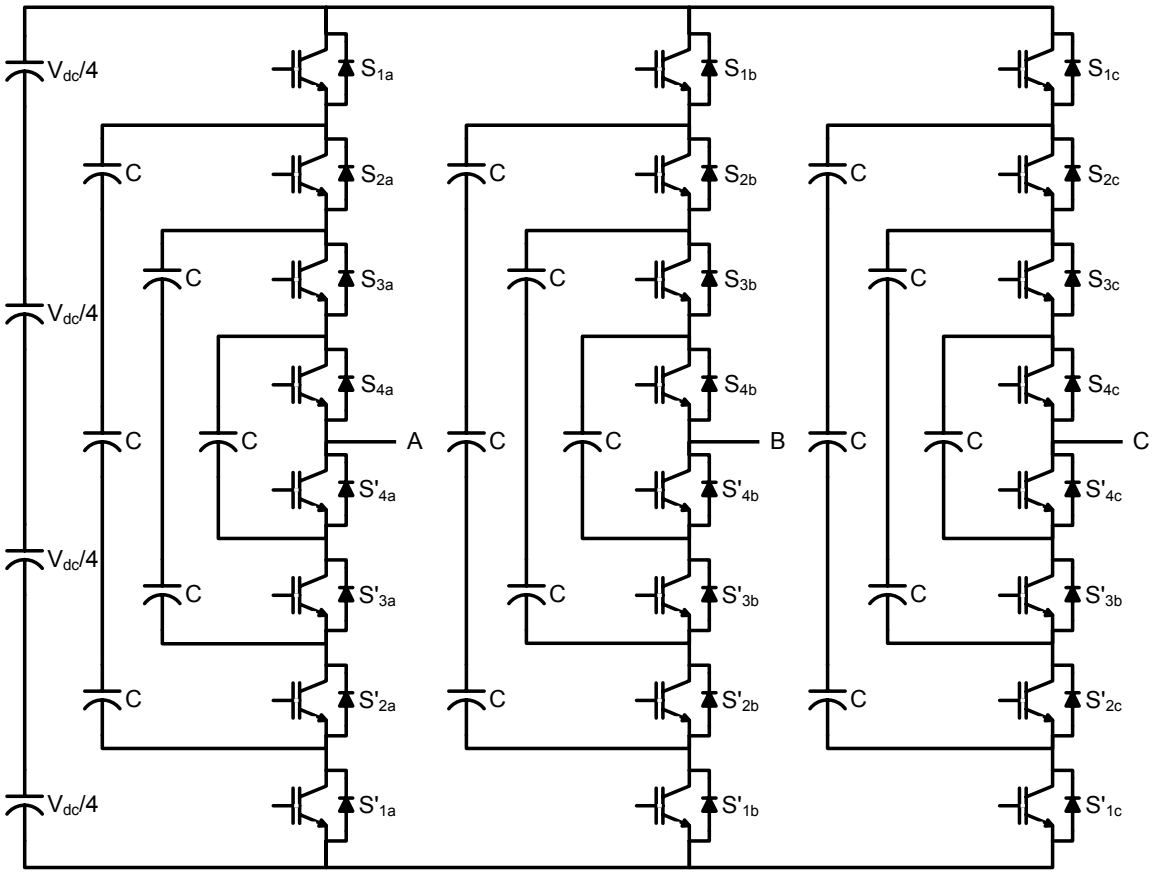



Fig. 1.4: Three-phase five-level flying capacitor inverter

floating or cell capacitor [37]–[45], out of which most of the schemes are based on carrier based PWM [35, 36, 38, 42]. A rule-based switching pattern scheme to maintain the capacitor voltage at desired level in FC inverter is proposed in [45]. A multilevel hysteresis current regulation strategy has been presented [39], to improve the dynamic response of FC MLIs. An analytic method is proposed by B. P. McGrath, et al. [41] for determining the natural capacitor voltage balancing dynamics of a three-phase flying capacitor converter supplying an induction motor load. Extended operation of a three-cell flying capacitor multilevel inverter has been studied by Keith A. Corzine and Jing Huang [42]. An interesting direct predictive control for a four-level FC inverter is proposed in [43]. In this scheme the gating patterns are generated without any modulation, just using sequence tables calculated offline.

#### 1.3.1.3 Cascade H-Bridge Multilevel Inverter (CHBMLI)

Cascade H-bridge (CHB) multilevel inverter is a new topology as compared to DCMLIs and FCMLIs [46]. This configuration has recently become popular in adjustable speed drive applications. The circuit diagram of three-phase five-level CHB inverter is shown in Fig. 1.5 ($V_{dc1}$=$V_{dc2}$). CHBMLIs consist of number of H-bridge power conversion cells, each supplied by an isolated source on DC side and series connected on AC side [47]–[49].

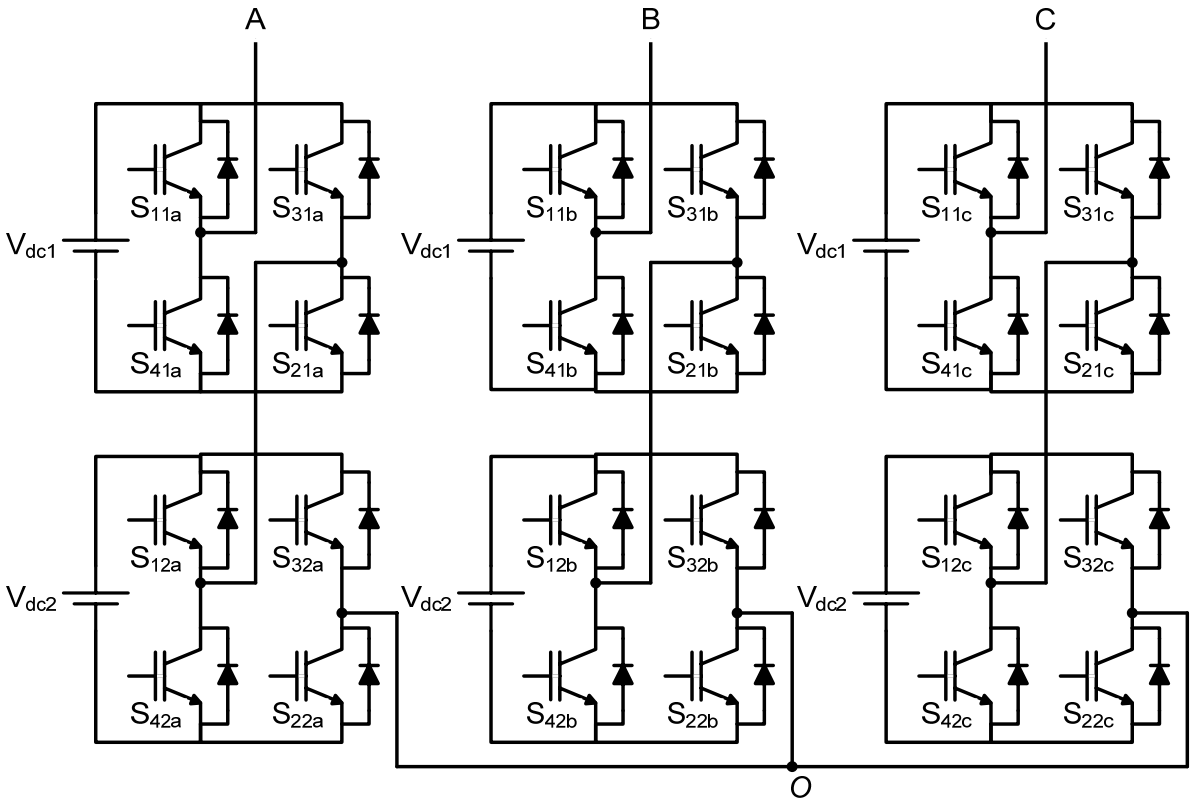



Fig. 1.5: Three-phase five-level cascade H-bridge inverter

However, the requirements of isolated DC sources make the topology bulky and very much costly. Regeneration is not possible in this topology, which restricts its application in regenerative motor drives. In the last few years researchers working in the field of MLIs have reported several variants of CHBMLIs and their control schemes [50]–[58].

Manjrekar has proposed an asymmetrical CHB topology [46]. Asymmetrical configurations of CHB ($V_{dc1} \neq V_{dc2}$) offer very high power improved quality waveform with less power semiconductors [49]. Lower switching losses can be obtained if high-power cells commutate at lower switching frequency. Contrarily, differences in power sharing of input transformers and complexity of input current harmonic compensation are the drawbacks of asymmetrical configuration of CHB.

A comparison of different types of three-phase MLIs, in terms of power components required to realize *n*-number of levels in each type of inverter is given in Table 1.1.

Table 1.1: Comparison of power components requirements in conventional MLIs

| Components Required | DCMLI | FCMLI | CHBMLI |
|---|---|---|---|
| Main switching devices (per phase) | 2(*n*-1) | 2(*n*-1) | 2(*n*-1) |
| Main diodes (per phase) | 2(*n*-1) | 2(*n*-1) | 2(*n*-1) |
| Clamping diodes (per phase) | (*n*-1)(*n*-2) | 0 | 0 |
| DC bus capacitors | (*n*-1) | (*n*-1) | (*n*-1)/2 |
| Balancing capacitors (per phase) | 0 | (*n*-1)(*n*-2)/2 | 0 |

#### 1.3.1.4 Multilevel Inversion Using Split-phase Induction Motor

It has been shown in literature that improved-quality multilevel output voltage waveform can be achieved by using split-phase induction motor [59]–[62]. The power circuit of split phase induction motor drive is shown in Fig. 1.6. K. Oguchi, et al. have suggested a six-phase inverter system to obtain a 60-step waveform for a six-phase induction motor [60]. The inverter system comprises two main three-phase inverters, an additional single-phase inverter and coupling reactors. The single-phase inverter injects ripple voltage, at a frequency six times higher than the fundamental frequency of the output voltage, into the DC-link. The main inverters operate at the same frequency as the output voltage. The coupling reactor is used to absorb harmonic components of the order $6m \pm 1$ ($m$=1,3,5…). This type of system is suited to applications where it is not possible to use high-frequency PWM and that require improved-quality voltage waveform.

K. Gopakumar, et al. proposed dual voltage source inverter fed six-phase induction motor drive system [59]. In this scheme 48 locations for the resultant voltage space vector are possible as compared with eight in the conventional three-phase configuration. The boundary of the voltage space phasor locations is a 12-sided polygon as compared with a hexagon for the three-phase system. Also, the DC-bus utilization in this system is higher by about 11.5% compared to the conventional system (i.e. a system in which a three-phase induction motor fed by two-level inverter).

In six-phase induction motor air gap flux produced by all the 6*m*±1 (*m*=1, 3, 5…) order harmonic voltages are mutually cancelled; these components are called zero sequence components and responsible for flow of large harmonic currents in the stator phases. Only the 12*m*±1 (*m*=0, 1, 2, 3…) order harmonic voltage components contribute toward the air gap flux and electromagnetic torque production in \

the motor. An interesting scheme is presented in [62] where two six-phase induction motors are connected in series with proper phase sequence so that the zero sequence component voltages of one machine act as torque and flux producing components for the other. Thus, the two six-phase induction motors can be independently controlled from a single six-phase inverter system.

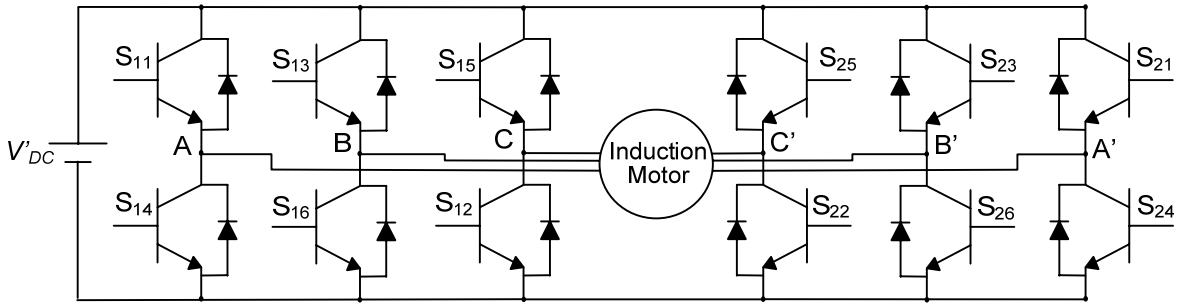



Fig. 1.6: Split phase induction motor drive

#### 1.3.1.5 Multilevel Inversion Using Open-end Winding Induction Motor

The concept of obtaining three-level inversion operation by feeding an open-end winding induction motor (IM) from either side with two two-level inverters is introduced by Stemmler and Guggenbach [63]. An open-end winding IM is obtained by opening the neutral point of the stator windings. Fig. 1.7 shows the power circuit schematic proposed in [63]. This scheme requires two isolated power supplies to prevent the triplen harmonic currents from flowing through the motor phases [64]. The magnitude of DC-link voltage of each inverter is $V_{DC}/2$, where $V_{DC}$ represents the DC-link voltage in an equivalent conventional scheme (i.e. a scheme in which a single two level inverter feeds a normal IM). It is well suited for automotive applications in which splitting the batteries bank is possible [65], [66].

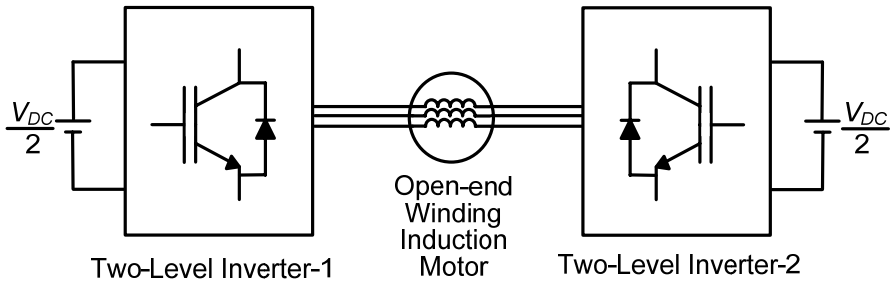



Fig. 1.7: Schematic of power circuit for open-end winding based three-level inverter

In recent years several MLI topologies based on this configuration have been reported in the literature [67]–[74]. M.R. Baiju, et al. presented a topology for voltage-space phasor generation equivalent to a five-level inverter for an open-end winding induction motor in [74]. In this scheme both ends of the IM are fed by three-level inverters. These three-level inverters are implemented by cascading two two-level inverters. In this scheme four isolated DC supplies are required. A six-level inverter is realized by feeding one end of the open-end winding IM motor by three-level inverter and other end by two-level inverter [72]. A hybrid seven-level inverter configuration for open-end winding IM is proposed in [68]. This inverter uses two numbers of two-level inverters and six capacitor-fed H-bridges to realize seven-level in the inverter output voltage. The number of levels in the topology proposed in [68] can be increased from seven to nine by changing the voltage across the capacitors of H-bridges [67], [75]. The advantage of capacitor fed H-bridge is that if any bridge fails, the inverter can still be operated at reduced power level that enhances the reliability of circuit. In addition to that more redundant states are available for capacitor balancing. A five-level inverter for an open-end winding induction motor is proposed by Figarado [70], this inverter uses only two DC-link rectifiers of voltage rating of $V_{DC}/4$, a neutral-point clamped (NPC) three-level inverter and a two-level inverter. Even though the two-level inverter is connected to the high-voltage side, it is always in square-wave operation. Since the two-level inverter is not switching in a pulse width modulation hence switching losses are reduced. K. Sivakumar, et al. presented a five-level inverter topology for open-end winding induction motor (IM) drive in [69]. The proposed topology is realized by feeding the phase winding of an open-end induction motor with two-level inverters in series with flying capacitors. The flying capacitor voltages are balanced using the switching state redundancy for full modulation range. The proposed inverter scheme is capable of producing two-level to five-level pulse width modulated voltage across the phase winding depending on the modulation range.

Somasekhar, et al. proposed a circuit configuration for the open-end winding induction motor drive to eliminate the requirement of isolated DC sources [76]. In this scheme the elimination of triplen harmonic currents is achieved by generation of switched neutral using bidirectional auxiliary switches.

### 1.3.2 Modulation Techniques for Multilevel Inverters

The efficiency parameters such as switching losses, harmonics, etc. of multilevel inverter are depend on the modulation strategies used to control the inverter. It is a technical challenge to extend traditional modulation methods to the multilevel case, due to the inherent additional complexity of having more power electronics devices to control, and the extra degrees of freedom provided by these topologies. As a consequence, a large number of modulation algorithms have been developed, each one with unique features and drawbacks, depending on the application. Abundant modulation techniques and control paradigms have been developed for multilevel inverters such as sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE-PWM), space vector modulation (SVM), and others. A classification of the modulation methods developed to control the multilevel inverters are presented in Fig. 1.8. Three main modulation techniques of multilevel inverters are SHE-PWM, PWM and optimized harmonics stepped pulse width modulation (OHS–PWM). The regular PWM modulation method can be classified as open loop and closed loop owing to its control strategy. The open loop PWM techniques are SPWM, space vector PWM, sigma–delta modulation, while closed loop current control methods are defined as hysteresis, linear, and optimized current control techniques [77].

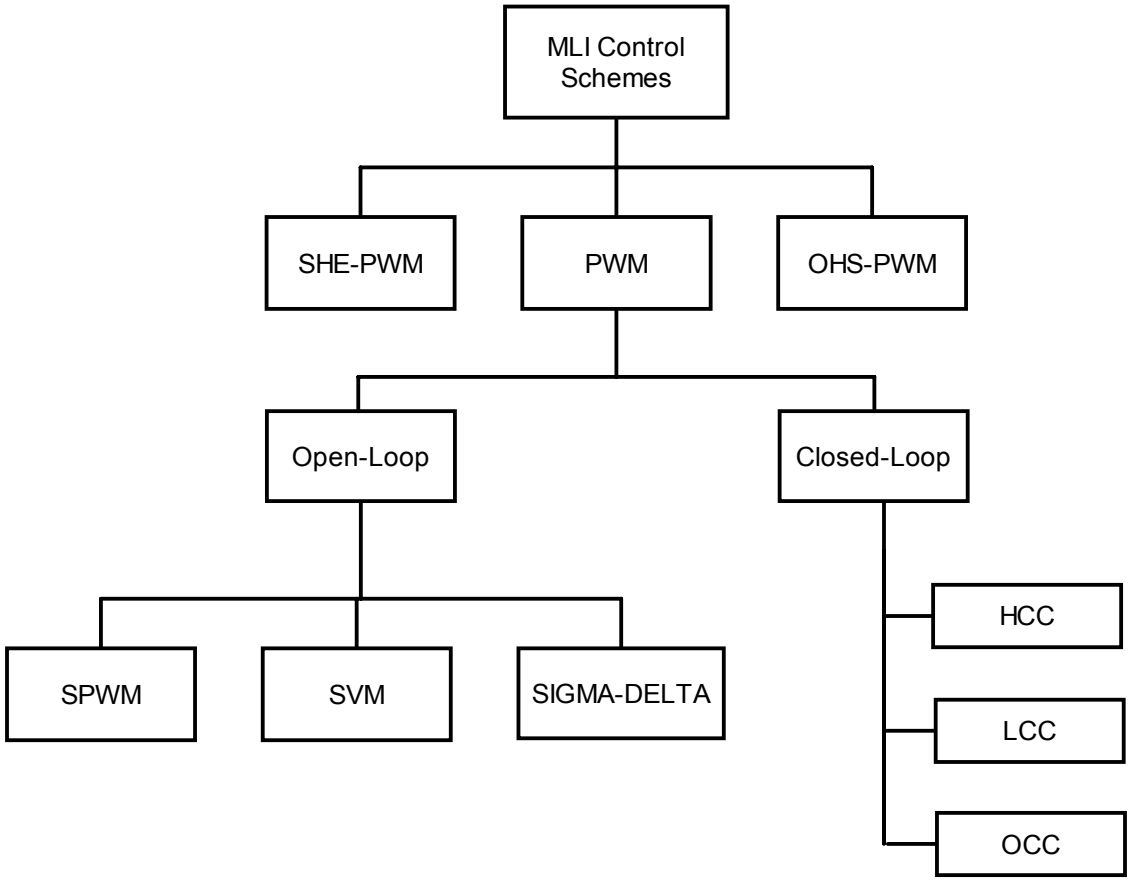



Fig. 1.8: Classification of multilevel modulation techniques

Different modulation methods and their technical features, limitation and applications are summarized in detail in [77], part of which is reproduced here for better insight. In general, low/medium switching frequency methods are preferred for high-power applications due to the reduction of switching losses, while the better output power quality and higher bandwidth of high switching frequency algorithms are more suitable for high dynamic range applications. Space Vector Modulation (SVM), Optimized Harmonic Stepped Wave (OHS) and Selective Harmonic Elimination (SHE) modulations are carried out at fundamental switching frequency, whereas Space Vector PWM and Sinusoidal PWM are high switching frequency modulation schemes.

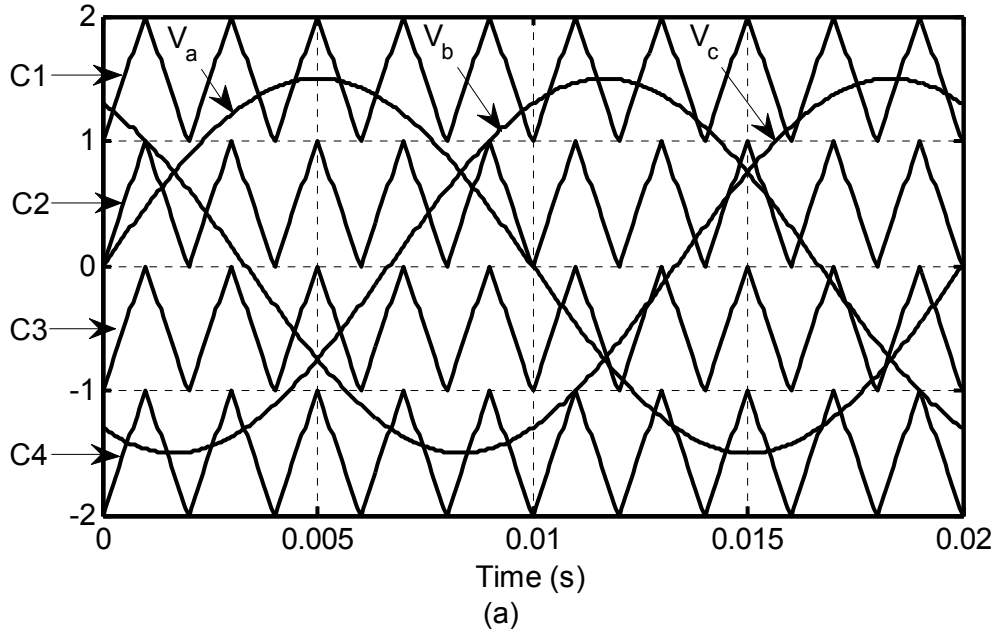
#### 1.3.2.1 Selective Harmonic Elimination PWM (SHE-PWM)

The selective harmonic elimination PWM (SHE-PWM) technique is based on fundamental frequency switching theory proposed by Patel in the year 1973 [78]. The main idea of this method is based on defining the switching angles of harmonic orders to be eliminated. Using SHE-PWM, it is possible to eliminate limited number of harmonics, but the non canceled harmonics are not considered in the algorithm and could reach very high amplitudes [79]. This leads to the fact that it is not possible to keep them below a desired value, having a great impact on the size and the cost of the filtering system. However, the flexibility of SHMPWM (Selective Harmonic Mitigation PWM) can be used to apply different criteria for low and high order harmonics. High-order harmonics can be reduced using SHM-PWM. SHM minimizes these harmonics, rather than eliminating them, according to some cost function (such as harmonic loss in an induction motor) to give a better overall result. A summary of harmonic elimination PWM techniques is presented by Enjeti et al. [80]. Selective harmonic elimination (SHE) has been extended to the multilevel case for high-power applications due to the strong reduction in the switching losses [81]–[83]. However, SHE algorithms are very limited to open loop or low-bandwidth applications since the switching angles are computed offline and stored in tables, which are then interpolated according to the operating conditions. In addition, SHE based methods become very complex to design and implement for converters with a high number of levels (above five), due to the increase of switching angles, hence equations that need to be solved. Chiasson, et al. suggested a complete solution to the harmonic elimination problem using the theory of resultants from elimination theory [84].

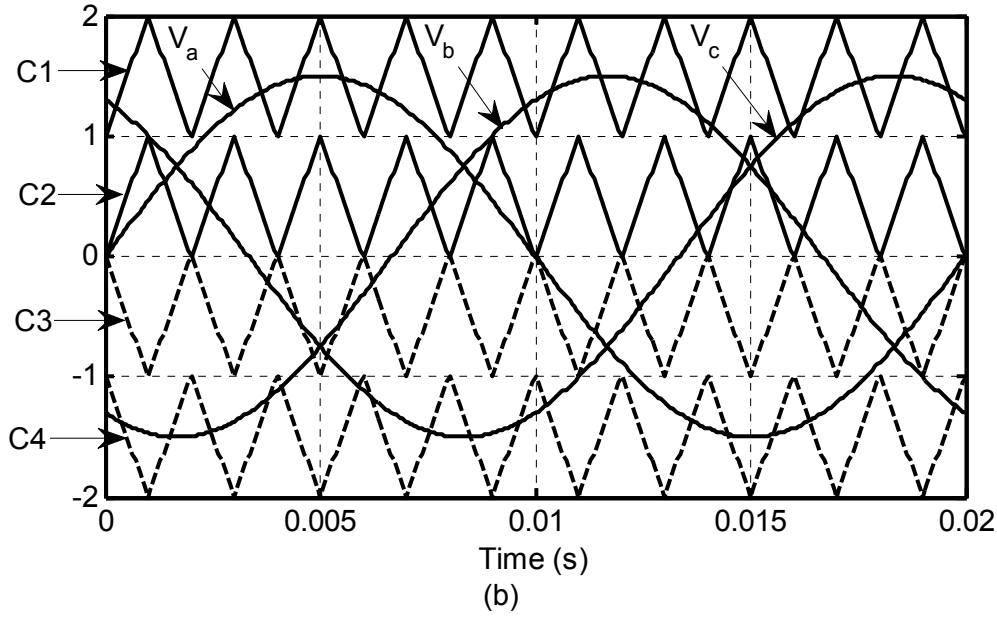
#### 1.3.2.2 Sinusoidal PWM (SPWM)

Traditional PWM techniques [85] have been successfully extended for multilevel inverters, by using multiple carriers to control each power switch of the inverter. Therefore, the traditional sinusoidal PWM techniques are also known as multicarrier PWM methods. For multi-cell topologies, like FC and CHB, each carrier can be associated with a particular

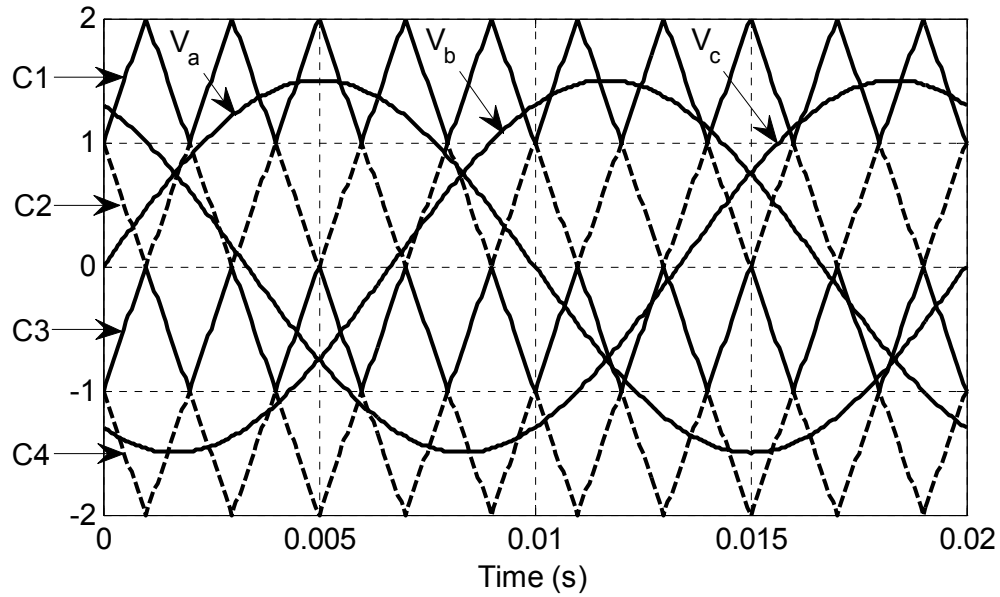
power cell to be modulated independently using sinusoidal bipolar and unipolar PWM, respectively, providing an even power distribution among the cells. The multi-carrier SPWM control methods have been classified according to vertical and horizontal arrangements of carrier signal. The vertical carrier distribution techniques are defined as phase disposition (PD), phase opposition disposition (POD), and alternative phase opposition disposition (APOD), while horizontal arrangement is known as phase shifted (PS) control technique. An example of these arrangements for a five-level inverter (thus four carriers) is given in Fig. 1.9 (a)–(d), respectively. In fact, PSPWM is only useful for cascaded H-bridges and flying capacitors MLI, while level shifted PWM (PD, POD and APOD) are more useful for NPC-MLI [86], [87]. An in-depth assessment between these PWM methods can be found in [88], [89].



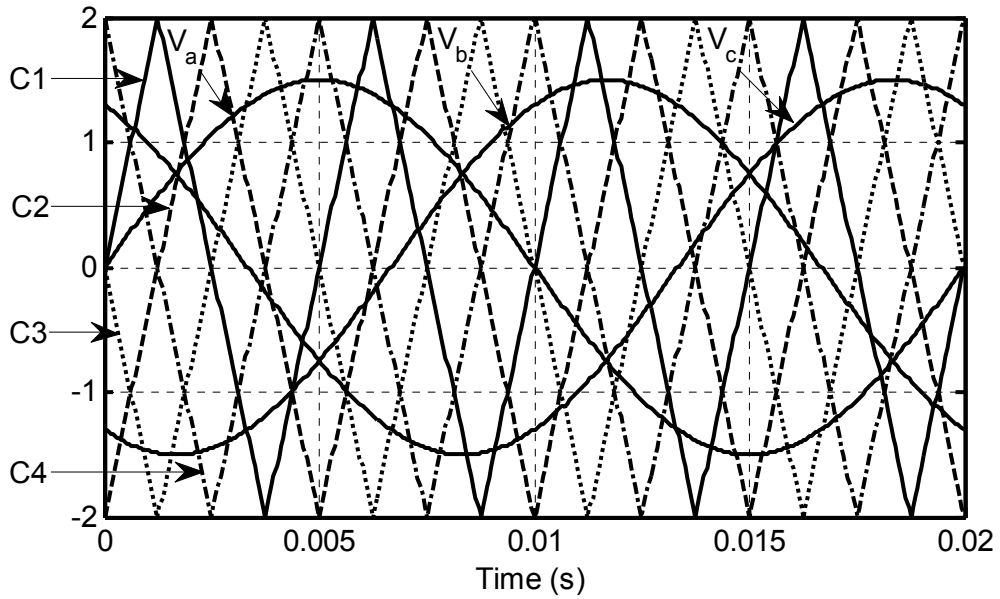
(a)



(b)




(c)




(d)

Fig. 1.9: Carrier arrangements for five-level inverter; (a) PD, (b) POD, (c) APOD, (d)PS

LS-PWM techniques can be implemented for any multilevel topology; however, they are more suited for the NPC-MLI since each carrier signal can be easily related to each power semiconductor. Particularly, LS-PWM methods are not very attractive for CHB inverters, since the vertical shifts relate each carrier and output level to a particular cell, producing an uneven power distribution among the cells. This power unbalance disables the input current harmonic mitigation that can be achieved with the multi-pulse input isolation transformer, reducing the power quality. Finally, the hybrid modulation is in part a PWM based method that is specially conceived for the CHB with unequal DC sources [90], [91]. The basic idea is to take advantage of the different power rates among the cells of the converters to reduce switching losses and improve the converter efficiency. This is achieved

by controlling the high-power cells at a fundamental switching frequency by turning ‘ON’ and ‘OFF’ each switch of each cell only one time per cycle, while the low-power cell is controlled using unipolar PWM.

#### 1.3.2.3 Space Vector PWM (SVPWM)

Space vector pulse width modulation (SVPWM) directly uses the reference voltage given by the control system as a reference space vector to be generated by the power converter. The harmonic elimination and fundamental voltage ratios in SVPWM schemes are obtained in better values compared to SPWM schemes. In addition to this, the maximum peak value of the output voltage is 15% greater than triangular carrier-based modulation techniques [77]. The requirement of sector identification and look-up table to determine the switching intervals in SVPWM make this method quite complicated. Although the difficulty of determining sectors and switching sequences according to increased *n*-level of inverter, DSP and microprocessor implementations provide proper solution while preparing the algorithms. The SVPWM technique generates the voltage reference vector as a linear combination of the state vectors obtaining an averaged output voltage equal to the reference over one switching period [92].

The proper placement of the zero space vectors can be achieved by addition of triplen offset voltage in all of the three reference waveforms in the carrier based PWM, which is equivalent to using space vector PWM [66], [93], [94]. McGrath, et al. find the similar equivalence between the phase disposition (PD) carrier and space vector modulation strategies applied to diode clamped, cascaded *n*-level or hybrid multilevel inverters [95].

Several space vector modulation (SVM) algorithms extended to multilevel converters have been proposed and reported in the literature. Most of them are particularly designed for a specific number of levels of the converter. The computational cost and the algorithm complexity are increased with the number of levels. This modulation technique for multilevel converters involves trigonometric function calculations, look-up tables, or coordinated system transformations, which increases the computational load. Researchers have made tremendous efforts to reduce the computational burden and the complexity of the algorithms compared with other conventional SVM and sinusoidal PWM modulation techniques [96]–[101]. These techniques provide the nearest state vectors to the reference vector forming the switching sequence and calculating the corresponding duty cycles using very simple calculations without involving trigonometric functions, look-up tables, or coordinate system transformations [102]. Therefore, these methods significantly reduce the computational load, permitting the online computation of the switching sequence and the on-state duration of the respective switching state vectors. In addition, the low computational cost of the proposed methods is always the same and it is independent of the number of levels of the inverter.

The general SVM scheme proposed by Gupta A.K., et al. in [100] for cascade MLI operated in overmodulation range is also applicable for NPC-MLI [33]. Wenxi Yao, et al. studied the relations of SVM and traditional carrier based PWM for multilevel inverter in their research articles [103], [104]. They proposed that the PWM generation of SVM can be achieved by carrier-based PWM scheme by addition of suitable offset in sine wave.

The common-mode voltage (CMV) generates leakage current and this leakage/discharge current is the main cause of bearing erosion because of the fluting or electro discharge machining (EDM) effect [105]. A number of techniques have been suggested to reduce or eliminate the common-mode voltages generated by the various configurations of multilevel inverters [106]–[111]. A comparative study of common mode voltage elimination scheme using SVM and SPWM for three-level NPC inverter is presented in [107] and It has been shown that SPWM gives almost the same performance as that of SVM.

Von Jouanne, et al. proposed a modulation scheme for eliminating the common-mode voltage in the conventional neutral-point clamped (NPC) three-level inverter [108]. M. R. Baiju, et al. presented a SVM based PWM to eliminate the common mode voltage using the open-end winding configuration for the induction motor [109]. A12-sided polygonal voltage space vector generation with common-mode voltage elimination is proposed for an open-end stator winding induction motor drive [110]. The proposed scheme gives a motor operation with zero common-mode voltage, which thus totally eliminates all the problems associated with common-mode voltage variation. A.K. Gupta. et al. proposed a space-vector modulation scheme to reduce common mode voltage for cascaded multilevel inverters. The proposed scheme not only reduces the CMV but also increase the voltage range of operation by about 17% with less total harmonic distortion [111].

#### 1.3.2.4 Sigma Delta Modulation (SDM)

The delta modulation (DM) technique was firstly proposed as a 1-bit coding method of pulse code modulation (PCM) by Jager in 1952 [77]. One-bit coding application was obtained using an integrator feedback block to pulse modulator that is a component of encoding process as seen in Fig. 1.10(a). The sigma-delta modulation (SDM) has been described with [112] in order to prevent the decreasing on power density of modulated signal according to increase sampling frequency. A SDM system was obtained adding a sample and hold block to a basic DM modulator as shown in Fig. 1.10(b). The SDM has adapted to power conversion processes using analog to digital (ADC) and digital to analog converters (DAC) [77]. The utilization of resonant DC-link inverters allows the soft switching applications instead of hard switching of conventional PWM. These kinds of inverters are mostly known with their zero switching losses obtained by switching at predetermined times of a sampler clock and this method can be appropriately adapted to SDM [113].

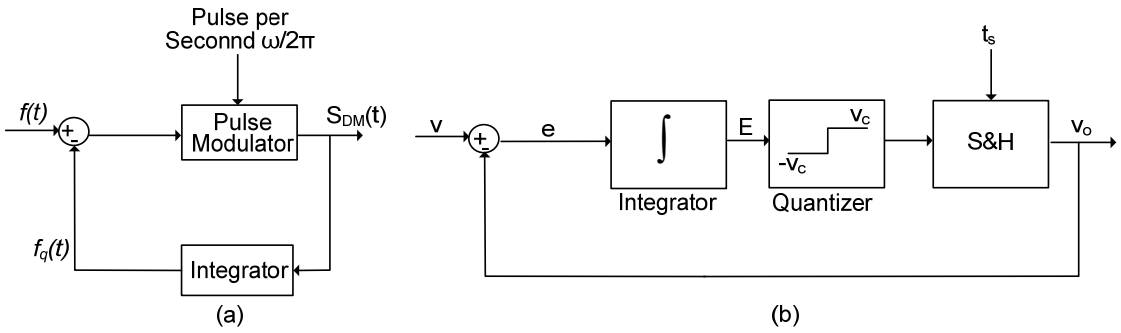



Fig. 1.10: Block diagrams of delta modulation: (a) Simple delta modulator, (b) Sigma–delta modulator

In the Fig. 1.10(b), the output of modulator changes to $+V_o$, 0, or $-V_o$ according to sampling period of $f_s$ and the output is compared with input amplitudes. The error (e) is integrated and the integrator (E) output is fed to quantizer. Quantizer determines the output sign opposite to (E). A multilevel SDM generates multi-bit data sequence and decoding the output yields several output states which can be used to control on/off states of the switches of multilevel inverter. The block diagram of SDM controlled multilevel inverter is shown in Fig. 1.11. The interaction of SDM modulator and inverter is managed using a multilevel decode logic block that adopts the quantized SDM signals and decodes to switching signals for inverter [114].

The research shows that although it has been developed to control DC-link inverters, the sigma-delta modulators can be developed to control multilevel inverters using logic interfaces [77], [115]. For a SDM controlled multilevel inverter, the output errors such as irregular voltage distribution and system nonlinearity can be reduced in high frequency switching up to 200 kHz.

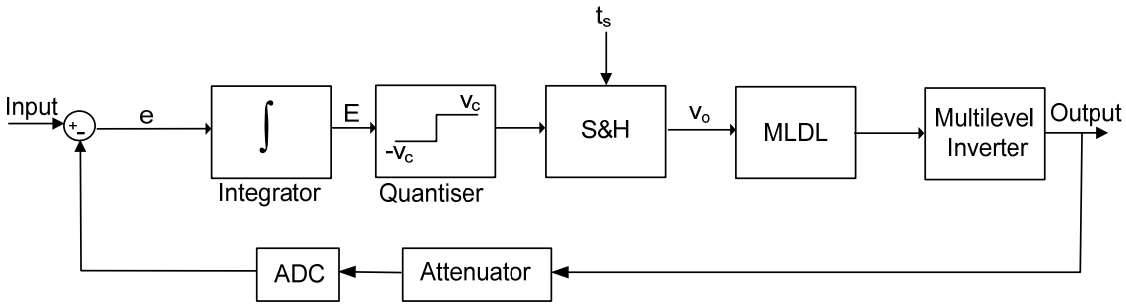



Fig. 1.11: Block diagram of sigma delta modulation control of a multilevel inverter

### 1.3.2.5 Hysteresis Current Control (HCC) Modulation

The hysteresis current control (HCC) modulation is a feedback current control method where the load current tracks the reference current within a hysteresis band in nonlinear load application of an MLI. Depending upon the hysteresis band, output waveform can be obtained from the set reference. The scheme is easy to implement. However, uncontrolled

switching frequency and higher switching losses in inverter limits its practical implementation [9]. A current-error space phasor based hysteresis controller with nearly constant switching frequency for generalized *n*-level voltage source inverter fed three-phase induction motor drive has been found in literature [116]–[118]. P.C. Loh, et al. suggested a double band hysteresis regulator for hybrid seven-level inverter [119]. The controller uses the slope of the current error to determine the appropriate steady state voltage level to keep this error within the inner hysteresis band, while still allowing switching to the extreme inverter states during transient conditions to reduce the current error as rapidly as possible. Roberto Rojas, et al. have been proposed hysteresis comparator based closed loop control of the line-to-line voltage vectors of NPC inverter [120]. A current-error space-vector-based hysteresis controller with online computation of boundary for two-level inverter-fed induction motor (IM) drives is proposed by R. Ramchand, et al. [121].

As mentioned above, all of the modulation schemes illustrated in Fig. 1.8 are not suitable for every topology; moreover, some of the algorithms are not applicable to some converters. The selected control scheme for any MLI determines the effectiveness on harmonic elimination, while generating the ideal output voltage. DC-MLIs, especially three-level structure, have a wide popularity in motor drive applications besides other multilevel topologies due to reducing THD with robust control of SHE-PWM control scheme. However, it would be a restriction of complexity and pre-defined switching angles when the levels exceed three. The SPWM and SVM modulation techniques succeed this limitation of DC-MLI for higher level topologies.

Table 1.2 illustrates the most appropriate control schemes according to selected multilevel inverter topology.

Table 1.2: The most appropriate control scheme matching diagram according to topologies

| Topology | Control scheme | | |
|---|---|---|---|
| | SHE-PWM | SPWM | SVPWM |
| DC-MLI | Most Appropriate | Applicable | Applicable |
| FC-MLI | Applicable | Applicable | Not Good |
| CHB-MLI | Not Good | Most Appropriate | Applicable |

### 1.3.3 Applications of Multilevel Inverters

In today's world multilevel voltage source converters have successfully been applied and emerged as an important alternative that competes with PWM-CSI in classic applications like compressors, pumps, fans, rolling mills, and conveyors, etc. [1]. It is worth noticing that these processes are the most common medium-voltage applications in the industry. The MLI

topologies discussed in section 1.3.1 posses different characteristics like the number of components, modularity, control complexity, efficiency, and fault tolerance. Particularly, the NPC topology has found an important market in high-power motor drive applications such as conveyors, pumps, fans and mills. Application of variable frequency drive (VFD) for high-power medium voltage (2.4 kV to 13.8 kV) motors is shown using NPC-MLI in [4, 8]. CHBs are suitable for renewable power conversion, battery operated vehicles, Magnetic Resonance Imaging (MRI) and transformer-less applications like active filters and STATCOMs [15]. G. Joos, et al. have been shown CHB and NPC application for STATCOM [122], [123]. S. Anand, et al. proposed a 4-level Open-Ended Transformer based STATCOM for high power applications [124].

Researchers all over the world are making great efforts to improve multilevel inverter performances such as the control simplification [125], implementation issues [126], [127], reducing the THD of the output signals [4], [125], reducing DC-link current ripples [109], the balancing of the DC-link capacitor voltage [24-34,111], extended operation in overmodulation [92], [100], reducing common-mode voltage [106]–[111], the development of new MLI topologies [91], [129]–[131] and new control strategies [85], [132]–[146]. In fact, the MLI idea is so much attractive that several major drive manufactures have obtained patents on MLI and associated switching techniques [147]–[149] and commercialized NPC, FC or CHB topologies with application oriented control [4]. Commercially available MV drive products offered by major drive manufactures are presented in [4].

Many MLI applications focus on industrial medium-voltage VFDs [150], automotive and traction systems [151], [152], flexible AC transmission system (FACTS) [153]–[156] and utility interface for renewable energy systems [157]. Multilevel inverters for high-power MV drives have found widespread applications in industry. They are used for pipeline pumps in the petrochemical industry [158] and water pumping stations [6], steel rolling mills in the metals industry [159] and traction applications in the transportation industry [147].

Researchers started to think about battery power electric vehicles since the 1960's; when the demand was revived due to air pollution and ecology. Technology advancement in last decade in the field of electric drives systems, new battery technologies, fuel cell, etc. lead to tremendous developments of HEVs. CHB and dual two level inverter scheme are prospective for HEV and other traction applications [151], [152].

Currently, one of the trends in development is to use synchronous generators with fully rated power converters. To reach the power levels of turbines several converters in parallel are required to handle full power since the current rating is generally high, considering that the output voltage of the conversion systems is usually about 690V. Nevertheless, operation in medium voltage now appears to be very attractive, considering that it would lead to lower currents and, hence cable width and cost reduction, which also has a positive impact on the

size and cost of line filters. It also reduces the voltage step-up requirement for connection at the PCC. Because of these reasons and considering that current turbines are in the megawatt range, multilevel converters emerge as a promising alternative as power converter interface for wind energy systems [157], [160]–[162].

The use of multilevel converters as power interface for photovoltaic grid-connected system seems, at a first glance, not very appropriate due to the low power level of current photovoltaic systems. However, grid-connected photovoltaic power plants are consistently increasing in power rating mainly due to the reduction in the cost of photovoltaic modules (among other factors); now, hundreds of large photovoltaic-based power plants over 10 MW [118] are operating, and even more are under development. For large photovoltaic power plants, centralized and multi string configurations are used with a central dc–ac converter that interfaces the power to the grid. Now that they reached the megawatt range, classic topologies such as the two-level voltage source converter will not be able to deliver the desired power quality, maximum allowed switching frequency, higher voltage operation, and reduction in filter size as that multilevel converters can provide. Multilevel converters can be used to interconnect the photovoltaic strings in a more intelligent way to reach higher voltages that are close to or even of the same value as the point of common coupling. As grid code requirements for photovoltaic systems will become more demanding, multilevel topologies will also become even more attractive [163]. Recent research shows that a three-phase four-level NPC-based converter and a five-level converter formed by a three-level H-bridge with a bidirectional switch arrangement that can clamp two additional levels to the output has been proposed as dc–ac converter stage in a multi string photovoltaic configuration [164], [165]. M. Saeedifard, et al. have been proposed a five-level diode clamped converter (DCC) based back-to-back high-voltage direct- current (HVDC) converter system [166].

Table 1.3: Multilevel inverter application summary based on topology

| Application | Topology | | |
|---|---|---|---|
| | DC-MLI | FC-MLI | CHB-MLI |
| Train Traction & Motor Drive | Good | Applicable | Most Appropriate |
| Active filters | Most Appropriate | Applicable | Applicable |
| Photovoltaic | Most Appropriate | Not Good | Applicable |
| Wind Power | Applicable | Most Appropriate | Applicable |
| HVDC | Applicable | Not Good | Most Appropriate |
| UPFC and UPQC | Applicable | Applicable | Most Appropriate |
| STATCOM | Applicable | Applicable | Most Appropriate |

Multilevel converters have matured from being an emerging technology to a well established and attractive solution for medium-voltage high-power drives. The recent developments in multilevel converter technologies together with the recent trends and challenges faced by energy applications such as, industrial drives, traction, renewable energy conversion [167], HVDC, FACTS and distributed generation systems are opening a wide area of applications where this technology has a lot to offer. Table 1.3 gives the idea about how active a particular topology is for a particular application.

### 1.3.4 Induction Motor Speed Control Methods

IM speed control methods can be divided into scalar and vector control. The general classification of IM control methods are given in [168]. Scalar control is based on relationship valid in steady state, only voltage magnitude and frequency of motor voltage, current and flux linkage space vectors are controlled. Thus, it does not act on space vector position during transients. *V/f* control of IMD gives adequate performance in steady state condition. Additionally, *V/f* control is simple, easy to implement and the control does not require any sensor and signal conditioning circuit. Application of *V/f* control is chosen where drive system may not require high dynamic performance. *V/f* control being simple in implementation widely used in majority of industrial applications. As being a scalar control technique, it gives sluggish dynamic response without decoupled control. Nearly, 85% of motors installed drives are used for pumps, fans, compressors and conveyors, where the drive system may not require high dynamic performance [1].

The vector control is based on relations valid for dynamic states, not only magnitude and frequency but also instantaneous positions of voltage, current and flux space vectors. Therefore, the vector control acts on the positions of space vectors and provides their correct orientations both in steady state as well as during transients. The most popular vector control methods Field Oriented Control (FOC) and Direct Torque Control (DTC) [169], have become industrial standard in advanced drive control. They are capable of introducing decoupled control between flux and torque in IMD [168]. Feedback Linearization Control (FLC) is another vector based control method in which input-output decoupling is obtained by nonlinear transformation of motor state variables in new coordinates [168]. DTC represents a viable alternative of FOC. It operates with closed loop torque and flux control without current controllers and insensitive to rotor parameters. Survey on DTC of PWM inverter-fed AC motors is given in [168]. Vector control methods give superior dynamic performance, but they have drawbacks like necessity and problems in number of sensors to be used, requirement of controller parameter tuning, complex control and higher cost. Several control scheme have been reported in the literature to eliminate or reduce the requirement of sensors [170]–[174].

V. Verma, et al. presented a single current sensor based vector controlled IM drive [170]. In this drive system, current estimation is based on the reference currents in

synchronously rotating reference frame and the vector rotator, the speed estimation exploits a different form of X-model reference adaptive system (X-MRAS). Both techniques MRAS and X-MRAS do not involve stator resistance. Hence, the proposed controller works very well at low speed.

C. Chakraborty, et al. proposed a model reference adaptive controller (MRAC) for the speed [171] and rotor resistance [173] estimation of the vector controlled induction motor drive. A. Choudhury and K. Chatterjee have also been reported a model reference adaptive scheme (MRAS) based clos6ed loop control scheme for direct torque control (DTC) IM drive [172]. The proposed scheme completely eliminates the requirement of speed sensor and offer constant switching frequency. An effort is made by A. Dey, et al. to minimize the torque ripples in DTC IM drive by using a three-level hysteresis torque controller [175].

The selection of the IM motor control is done based on the superior performance, implementation issues in real-time and cost effectiveness.

### 1.4 Scope of Work and Author's Contribution

MLI for medium and high voltage induction motor drive gaining more and more popularity day by day because of their inherent quality of reduced total harmonic distortion (THD), low *dv/dt* stress, low switching losses, high voltage capability and good Electro-Magnetic Compatibility (EMC). The quality of MLI output voltage is improved with the increase in number of levels, but at the same time the structure of MLI become very complex and less reliable, due to use of large number of switching devices.

Present work is carried out to investigate the possibility of obtaining multilevel inversion operation for induction motor drive with reduce number of components. Technical problems, possible solutions and attractive features are discussed for conventional two-level inverter and MLI topologies. The multilevel inverter topologies proposed in the thesis use dual inverter fed open-end winding configuration for the induction motor. A comprehensive literature survey on MLI with respect to various topologies, historical developments, PWM techniques, control methodologies and recent trends are given. The main contributions of the author are as follows:

**1) Investigations on dual two-level (D2L) inverter for IMD**

- A mathematical model of the squirrel cage open-end stator winding induction motor in stationary reference is developed.
- A switching function based mathematical model of D2L inverter is also developed.
- Simulation study is carried out in MATLAB/Simulink environment by operating the developed motor model with D2L inverter in constant *V/f* mode under no-load condition covering the entire range of modulation.

- Various simulation results are obtained and analyzed for performance evaluation.

**2) Investigations on 5-level inverter for IMD**

- A 5-level inverter configuration based on conventional 2-level inverters is realized.
- A switching function based mathematical model of 5-level inverter is developed and simulated with MATLAB/Simulink.
- It has been shown that the same 5-level inverter circuit can produce six levels by selecting a proper ratio of DC link voltages of individual two-level inverters.
- The level shifted triangular carrier based SVPWM scheme is adopted and implemented in MATLAB to generate the control pulses for switching devices.
- Performance of 5-level inverter is evaluated in MATLAB by running a 1.5 kW open-end winding induction motor model at no-load in *V/f* control mode.

**3) Investigations on 9-level inverter for IMD**

- With the aim to generate high resolution voltage space vectors with reduced number of components for an open-end winding induction motor, a 9-level inverter scheme is proposed.
- A modified level shifted triangular carrier based SVPWM technique is used for the proposed drive system.
- The proposed PWM scheme is capable of ensuring a smooth changeover from the mode of two-level inversion to the 3-level, then 3-level to 4-level, then from 4-level to 5-level and so on up to 9-level inversion and vice versa.
- A switching function based mathematical model of the proposed drive system is developed and validated by detailed analytical results in MATLAB/Simulink environment.
- Simulation study is carried out in MATLAB/Simulink environment to evaluate the performance of proposed 9-level inverter in steady state as well as in transient state.

**4) Investigations on hybrid 9-level inverter for IMD**

- A hybrid 9-level inverter is another configuration proposed in the thesis to reduced the requirement of four number of isolated DC sources of two different voltage rating in to two isolated DC sources of same voltage rating.
- The proposed topology is compared with conventional topology in terms of number of components used.
- A switching state based mathematical model is developed to realize 9-level inversion operation.

- The space vector location and available switching redundancy at different locations are analyzed.
- The capacitors voltage balancing algorithm and performance of the proposed inverter is evaluated under steady state as well as in transient state in MATLAB/Simulink environment.
- The scheme is computationally simple; therefore, it can be implemented using a commercially available DSP/microcontroller.

**5) Investigations on 18-level inverter for IMD**

- The third topology proposed in the present work is an 18-level inverter topology for open-end winding induction motor drive by using ACHB and conventional two-level inverter.
- The proposed topology requires less number of components as compared to conventional multilevel inverter (MLI) topology.
- The number of components used by proposed topology is same as that of use by hybrid 9-level inverter.
- An interesting feature of the proposed topology is that, it can operate in nine-level mode by connecting the motor winding in star in case of failure of two-level inverter. Similarly if the fault occurs in ACHB inverter the proposed inverter can operate in two-level mode. Thus, the reliability of the system is improved.
- A switching function based mathematical model of proposed inverter is developed and implemented using MATLAB/Simulink. The performance of inverter is investigated by running a 1.5kW open-end winding induction motor under no-load in *V/f* control mode for the entire range of modulation.

**6) Development of laboratory prototype for experimental validation**

- In this thesis extensive simulation study is carried out on D2L inverter, 5-level inverter, 9-level inverter, hybrid 9-level inverter and 18-level inverter for an induction motor with open-end windings. In order to validate the simulation results, downscaled prototypes of following topologies are developed in the laboratory and experimentation is carried out:
  (a) Topology-1: 5-Level Inverter for open-end IMD
  (b) Topology-2: 9-Level Inverter for open-end IMD
  (c) Topology-3: Hybrid 9-Level Inverter for open-end IMD
- The different hardware components as required for the proper operation of experimental setups such as driver circuit, isolation and dead-band circuits, voltage and current sensor circuits designed, developed and interfaced with RT-Lab real time controller.

- Rapid control prototyping of drives library is carried out by total development environment of RT-Lab real time digital simulator with Spartan-3 FPGA board for flexible control development using model-based control design with minimum hardware and small design cycle.
- A level shifted triangular carrier based SVPWM algorithm implemented on RT-Lab real time controller to generate gate pulses for the IGBTs of developed prototype inverter in real time.
- Implementation of *V/f* control scheme for IMD is carried out in RT-Lab real time digital simulator.
- Performances of all three prototype inverters are experimentally evaluated in steady state and dynamic speed changing conditions. Further, these experimental studies are validated with simulation results obtained using the experimental parameters.

## 1.5 Organization of the Thesis

The thesis is organized in eight chapters and the work included in each chapter is briefly outlined below:

**CHAPTER-1** starts with brief overview of the problems faced by conventional two-level inverter fed high power medium voltage IM drives, their possible solutions and then the features and the technical challenges of MLIs are discussed. A comprehensive literature survey on MLIs including various topologies, modulation strategies, control schemes, historical developments, and applications is given in detail. Finally, scope of work, author's contribution and thesis outlines are presented.

**CHAPTER-2** describes dual two-level (D2L) inverter, scheme for open-end IMD. A mathematical model of the squirrel cage open-end stator winding induction motor along with D2L inverter is presented. A carrier based space vector pulse width modulation (SVPWM) scheme is adopted for the D2L inverter scheme. The steady state and transient state performances of the SVPWM based D2L inverter scheme is investigated for open-end IMD in MATLAB/Simulink environment.

In **CHAPTER-3** a 5-level inverter scheme using three numbers of two-level inverters is presented for open-end IMD. A Switching function based inverter mathematical model is proposed. Procedure for determining the DC link ratio to achieve the maximum number of levels in output voltage is discussed. A simulation model of 5-level inverter scheme is developed using Simulink toolbox of MATLAB software and tested by operating a 1.5-kW open-end winding IM model at no-load in *V/f* control mode.

A 9-level inverter scheme for open-end IMD is proposed in **CHAPTER-4.** A switching function based mathematical model of the proposed scheme is developed and validated by detailed analytical results in MATLAB/Simulink environment. A modified level shifted

triangular carrier based space vector pulse width modulation (SVPWM) scheme is proposed to reduce the switching losses at lower speed operation. Simulation study is carried out to evaluate the steady state and transient state performance of the SVPWM based 9-level inverter scheme by operating an open-end winding IM at no-load in constant *V/f* mode for entire range of modulation.

**CHAPTER-5** investigates a hybrid 9-level inverter topology for open-end IMD. The proposed topology is compared with other 9-level inverter topologies in terms of number of component used. A switching function based mathematical model is developed to realize 9-level inversion operation. To validate the mathematical model simulation study is carried out in MATLAB/Simulink environment and detailed analytical results are presented. The space vector location and available switching redundancy at different locations are discussed. The capacitors balancing algorithm and performance of the drive is evaluated during steady state as well as in transient state by operating an open-end winding IM model at no-load in constant *V/f* mode covering the entire range of modulation.

**CHAPTER-6** proposes an 18-level inverter using the same number of switching devices used by hybrid 9-level inverter presented in chapter-5. A comparison is made between proposed 18-level inverter and other 18-level MLI topologies in terms of number of components use. A switching function based mathematical model is developed for proposed inverter. Exhaustive simulation study is carried out in MATLAB/Simulink environment to check the correctness of mathematical model. Steady state and dynamic performance of the proposed inverter fed open-end IMD system at different modulation indices at no-load in *V/f* control mode, based on simulation studies, is also presented.

**CHAPTER-7** is dedicated to experimental investigations on 5-Level Inverter, 9-Level Inverter and hybrid 9-Level Inverter topologies proposed in previous chapters for open-end IMD. This chapter deals with design of system hardware, RT-Lab Meta Controller interfacing and experimentation on the three laboratory prototype to validate the simulation results presented in previous chapters. To investigate the performance of the prototype inverters a 1.5kW open-end winding IM is operated at no-load in *V/f* control mode. Further, these experimental studies are validated with simulation results obtained using the experimental parameters.

The main conclusions of the presented work and possible future research are summarised in **CHAPTER-8**.

A list of important references and appendices are given at the end.

# CHAPTER 2: DUAL TWO-LEVEL INVERTER FOR INDUCTION MOTOR DRIVE

*[This chapter describes dual two-level (D2L) inverter, scheme for open-end induction motor drive. The mathematical model of the squirrel cage open-end stator winding induction motor along with D2L inverter is developed. A carrier based space vector pulse width modulation (SVPWM) scheme is presented for the D2L inverter scheme. The steady state and transient state performance of the SVPWM based D2L inverter scheme is investigated for open-end induction motor drive.]*

## 2.1 Introduction

The conventional two-level inverters are widely used in variable speed induction motor drive due to its simple circuit structure, reliable and cheaper parts as well as simple control. In high power and high performance drive applications, they suffer from problems like high dv/dt, higher switching loss, poor power quality and high Electromagnetic Interference (EMI). On the other hand, multilevel inverters (MLI) offer low dv/dt stress, good power quality, low switching loss, high voltage capability and better Electro-Magnetic Compatibility (EMC) even at high performance and high power applications. The quality of output voltage waveform improves with the increase of number of levels, but at the same time the conventional MLIs suffer from several problems like large device count, DC-link voltage unbalancing, more complex circuit and control specially at higher number of levels [9]. In order to adopt multilevel approach using conventional two-level inverter configurations [176]-[177], the dual two-level inverter (D2L) scheme is selected for analysis. This topology produces voltage levels equivalent to a three-phase three-level inverter. As compared to cascade H-bridge (CHB) three-phase three-level inverter topology [46] which requires three isolated DC sources, the D2L inverter scheme uses only two isolated DC sources. The voltage rating of the source and switching devices are receded by half in D2L configuration. Resultant space vector locations generated by D2L inverter scheme for open-end winding induction motor are similar to a three-level neutral point clamped (NPC) inverter [18]. The D2L scheme completely eliminates the requirement of clamping diodes and tapped DC-link capacitors. It offers reduced harmonic distortions with limited switching frequencies, lower dv/dt and higher voltage capability. Moreover, the inverter is composed of widely commercialized parts, which make its implementation cheaper and reliable. It is well suited for automotive applications in which splitting the batteries bank is convenient and reliable solution.

## 2.2 System Configuration and Switching Logic

### 2.2.1 Power Circuit

The power circuit of D2L inverter scheme for open-end winding induction motor (IM) is shown in Fig. 2.1. One end terminals of the open-end winding IM ($A_1$, $B_1$, $C_1$) are fed by two-level inverter-1 while the others end terminals of the machine ($A_2$, $B_2$, $C_2$) are fed by

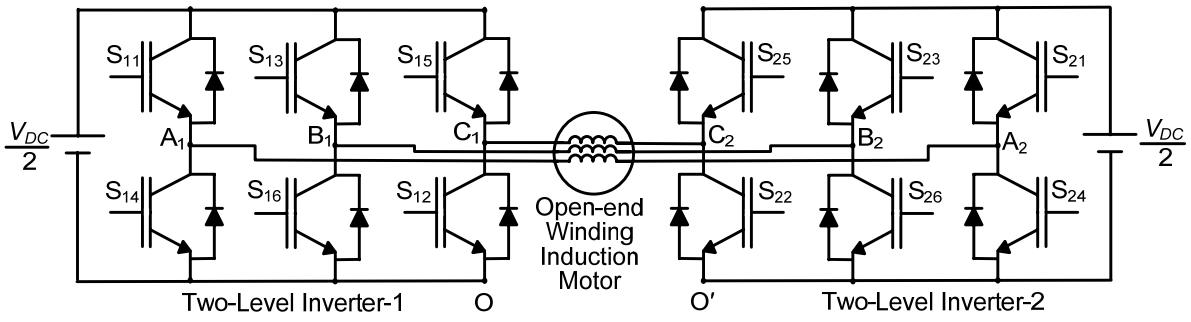



Fig. 2.1 :Dual two-level (D2L) inverter scheme for open-end winding induction motor drive

another similar type of two-level inverter-2. Both two-level inverters are powered by isolated DC source of magnitude $V_{DC}/2$. Any pole voltage $V_{A1O}$, $V_{B1O}$ or $V_{C1O}$ of two-level inverter-1, can have two levels 0 and $V_{DC}/2$ independently. Similarly inverter-2 pole voltages with respect to reference point O′ are $V_{A2O'}$, $V_{B2O'}$ and $V_{C2O'}$ can also have two levels 0 and $V_{DC}/2$ independently. The difference of these two pole voltages will have three-different levels as $-V_{DC}/2$, 0 and $+V_{DC}/2$.

### 2.2.2 Switching Logic

Inverter switching logic is developed to obtain three-level inversion operation. The pole voltage $V_{A1O}$ of two-level inverter-1 (Fig. 2.1) will be at level $+V_{DC}/2$ if the switch $S_{11}$ is made to turn 'ON', and at level zero if the switch $S_{14}$ is made to turn 'ON'. Any pole voltage of two-level inverter-1 $V_{A1O}$, $V_{B1O}$ or $V_{C1O}$ can have these two levels by proper selection of switches of two-level inverter-1, which are made to be turned 'ON'. Similarly the pole voltage $V_{A2O'}$ of inverter-2 (Fig. 2.1) can also have voltage level of $V_{DC}/2$ if the switch $S_{21}$ is made to turn 'ON', and at level of zero if the switch $S_{24}$ is made to turn 'ON'. Any pole voltage of two-level inverter-2 $V_{A2O'}$, $V_{B2O'}$ or $V_{C2O'}$ can have these two levels by proper selection of switches of two-level inverter-2, which are made to be turned 'ON'. The combine effect of both two-level inverters is generation of three distinct voltage levels in the phase voltage of open-end winding induction motor as shown in Table 2.1. It is clear from the Table 2.1 that the voltage levels of $-V_{DC}/2$ (Level-$L_1$) and 0 (Level-$L_2$) can be generated by clamping the inverter-1 at zero voltage level and switching the inverter-2 between $V_{DC}/2$ and zero. Similarly to get the voltage level of $V_{DC}/2$ (Level-$L_3$), inverter-1 is clamped at $V_{DC}/2$ and inverter-2 at zero. Switching states of corresponding switches of both two-level inverters to realize three-levels across the phase-A winding of open-end induction motor are shown in Table 2.1. Similar logic can also be implemented for others phases. Switches correspond to same leg of any two-level inverter operate in complementary fashion. The voltage rating of all the switches is $V_{DC}/2$ where $V_{DC}$ is the equivalent DC link voltage required to operate conventional two-level inverter fed induction motor drive.

Table 2.1: Switching states of inverter-1 and inverter-2 to realised three-levels in phase- A

| Level | Pole voltage of two-level inverter-1 ($V_{A1O}$) | Pole voltage of two-level inverter-2 ($V_{A2O'}$) | Motor phase-A voltage level ($V_{A1O}$ -$V_{A2O'}$) | Switch (state) Inverter-1 | Switch (state) Inverter-2 |
|---|---|---|---|---|---|
| $L_1$ | 0 | $V_{DC}/2$ | $-V_{DC}/2$ | $S_{14}$ (ON) | $S_{21}$ (ON) |
| $L_2$ | 0 | 0 | 0 | $S_{14}$ (ON) | $S_{24}$ (ON) |
| $L_3$ | $V_{DC}/2$ | 0 | $V_{DC}/2$ | $S_{11}$ (ON) | $S_{24}$ (ON) |

### 2.3 Control Scheme

The gating signals for the devices are generated using the multi-level carrier based space vector pulse width modulation (SVPWM) technique [178], [179]. The open-end winding induction motor is operated in constant *V/f* control mode. The magnitude of reference voltage space phasor ($V_r$*) is determined by *V/f* ratio and modulation index. Fig. 2.2 shows the principle of multi-level carrier based space vector pulse width modulation (SVPWM) scheme. In this figure only phase–A modulating procedure is shown for simplicity. Both the switches of same leg operate in complementary fashion. The entire range of operation is divided into three regions by two level-shifted triangular carrier waves (C1, C2). The region below the first triangular carrier C1 is define as level $L_1$, region between C1 and C2 is level $L_2$ and region above second triangular carrier C2 is level $L_3$.

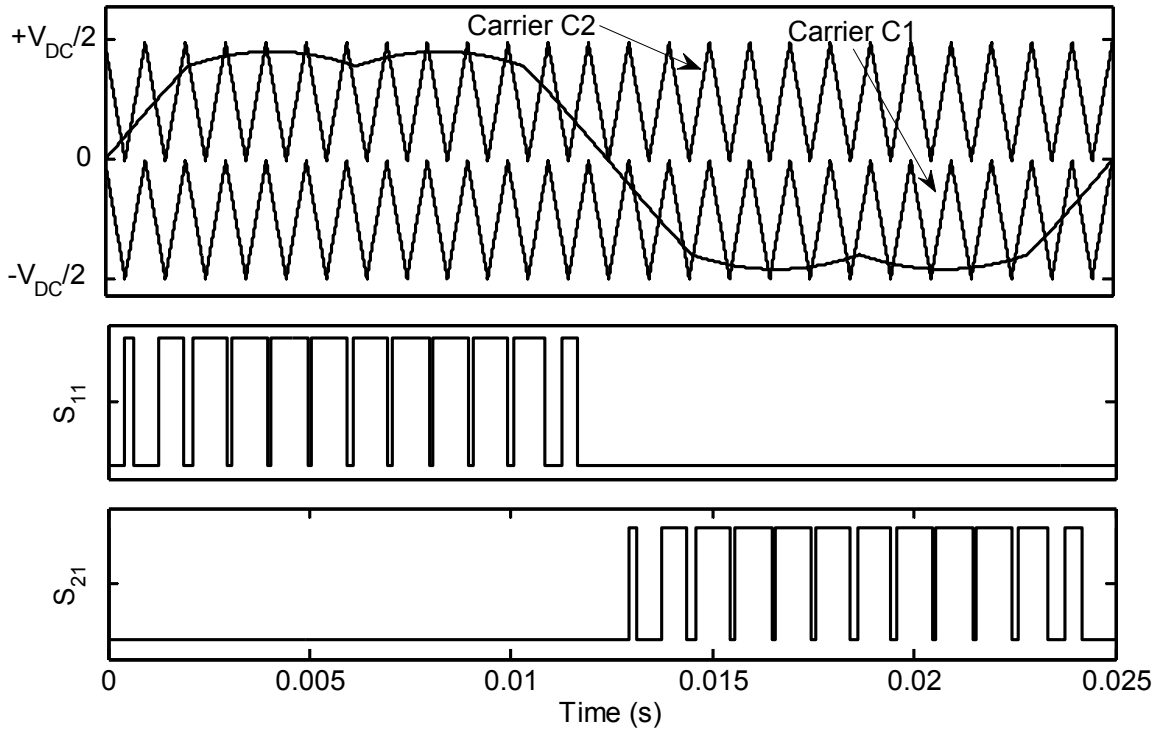



Fig. 2.2: Switching signals for the devices of phase–A of three-level D2L inverter using LSPWM technique

Three modulating signals are simultaneously compared with triangular carrier signals (C1, C2) in each sample period and depending upon their instantaneous position switching signals are generated according to Table 2.1. The three reference waves ($V^*_a$, $V^*_b$, $V^*_c$) corresponding to phase-A, B and C are generated by transferring the orthogonal components of reference voltage phasor ($V^*_r$) into the 3-phase quantity. An offset as given by equation (2.1) is added to these reference waves to generate three modulating signals which give the performance equivalent to conventional SVPWM [179]. The three modulating signals are expressed by equation (2.2).

$$V_{offset} = -[\max(V_a^*, V_b^*, V_c^*) + \min(V_a^*, V_b^*, V_c^*)] / 2 \tag{2.1}$$

$$\left.\begin{aligned} V_{A1A2}^* &= V_a^* + V_{offset} \\ V_{B1B2}^* &= V_b^* + V_{offset} \\ V_{C1C2}^* &= V_c^* + V_{offset} \end{aligned}\right\} \tag{2.2}$$

The modulation index ($m$) is define as the ratio of the magnitude of the actual reference voltage space phasor ($\left|V_r^*\right|$) to the maximum magnitude of the voltage space phasor ($V_{DC}$) as given by equation (2.3). The limit of modulation index ($m$) for linear modulation is 0.866 [179].

$$m = \frac{\left|V_r^*\right|}{V_{DC}} \tag{2.3}$$

## 2.4 Mathematical Modelling of Dual Two-Level (D2L) Inverter fed IMD

The mathematical modelling of dual two-level inverter fed open loop drive scheme includes model of D2L inverter and open-end winding induction motor. The assumptions made for the modelling of the drive scheme are as follows:

- The DC link voltages available at the input terminals of inverters are ripple free.
- The three-phase stator windings of the induction motor are balanced and produce sinusoidal Magneto Motive Force (MMF) in the space and harmonics are ignored.
- Switching transients in both inverters are ignored.
- Switching transition time of the switching devices are considered to be negligible.

### 2.4.1 Model of D2L Inverter

Mathematical modelling of D2L scheme is first obtained for switching functions based pole voltages of both two-level inverters thereafter motor phase-voltages are obtained in terms of inverters pole voltages and line voltages. Fig. 2.3 shows the applied switching function to each switch and inverters pole voltages with respect to their negative terminal. Both switches of the same leg operate in complementary fashion to avoid the short-circuit of DC source. Two switching functions $SF_X$ and $SF_{X'}$ (X=a, b, c) are defined for each phase

which can take discrete value either 0 or 1. In terms of switching function, Inverter-1 pole voltages ($V_{A1O}$, $V_{B1O}$, $V_{C1O}$) with respect to point-O are given by

$$\left.\begin{aligned} V_{A1O} &= \frac{V_{DC}}{2} SF_a \\ V_{B1O} &= \frac{V_{DC}}{2} SF_b \\ V_{C1O} &= \frac{V_{DC}}{2} SF_c \end{aligned}\right\} \tag{2.4}$$

Similarly Inverter-2 pole voltages ($V_{A2O'}$,$V_{B2O'}$,$V_{C2O'}$) with respect to point-O' in terms of DC link voltages and switching functions are given by:

$$\left.\begin{aligned} V_{A2O'} &= \frac{V_{DC}}{2} SF_{a'} \\ V_{B2O'} &= \frac{V_{DC}}{2} SF_{b'} \\ V_{C2O'} &= \frac{V_{DC}}{2} SF_{c'} \end{aligned}\right\} \tag{2.5}$$

The three-phase voltages can be expressed as:

$$V_{A1A2} = V_{A1O} + V_{OO'} - V_{A2O'} \tag{2.6}$$

$$V_{B1B2} = V_{B1O} + V_{OO'} - V_{B2O'} \tag{2.7}$$

$$V_{C1C2} = V_{C1O} + V_{OO'} - V_{C2O'} \tag{2.8}$$

Where $V_{A1A2}$,$V_{B1B2}$,$V_{C1C2}$ are the phase voltages of phase A, B and C respectively and $V_{OO'}$ is the common mode voltage. Since both the two-level inverters are supplied by isolated DC sources, hence they can be assumed to be two independent nodes. Thus for the balance three-phase load summation of the three-phase voltages will be zero.

$$V_{A1A2} + V_{B1B2} + V_{C1C2} = 0 \tag{2.9}$$

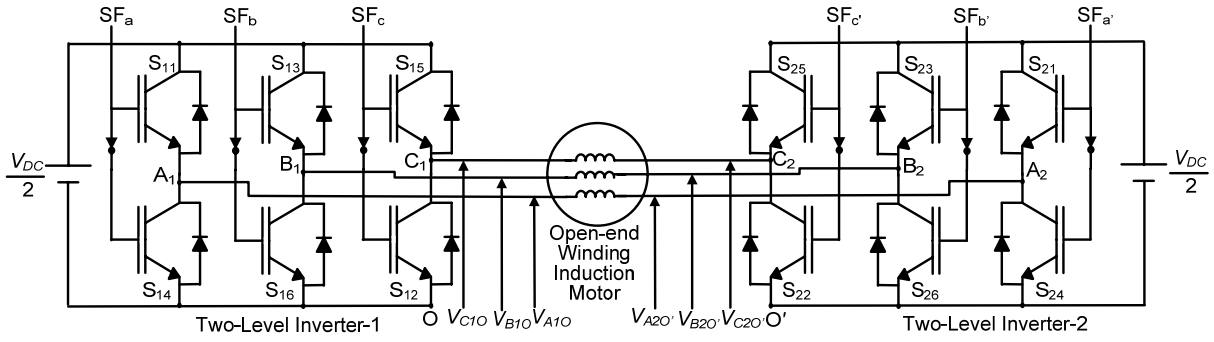



Fig. 2.3: Diagrammatic representation of switching functions and inverter pole voltages for D2L inverter

Using equations (2.6)-(2.9) common mode voltage can be expressed as:

$$V_{OO'} = \frac{(V_{A2O'} + V_{B2O'} + V_{C2O'}) - (V_{A1O} + V_{B1O} + V_{C1O})}{3} \tag{2.10}$$

Thus, the common mode voltage of the D2L inverter system is the difference between the common mode voltages of an individual inverter. The common mode voltage is not a problem if two sources are isolated; in single source topologies an arrangement has to be made to avoid common mode current flow.

On substituting the value of $V_{OO'}$ from equation (2.10) in to equation (2.6) phase-A voltage can be expressed as:

$$V_{A1A2} = \frac{2}{3}(V_{A1O} - V_{A2O'}) - \frac{1}{3}(V_{B1O} - V_{B2O'}) - \frac{1}{3}(V_{C1O} - V_{C2O'}) \tag{2.11}$$

Similarly substituting the value of $V_{OO'}$ from equation (2.10) in to equations (2.7) and (2.8) phase-B ($V_{B1B2}$) and phase-C ($V_{C1C2}$) voltages can be written as:

$$V_{B1B2} = -\frac{1}{3}(V_{A1O} - V_{A2O'}) + \frac{2}{3}(V_{B1O} - V_{B2O'}) - \frac{1}{3}(V_{C1O} - V_{C2O'}) \tag{2.12}$$

$$V_{C1C2} = -\frac{1}{3}(V_{A1O} - V_{A2O'}) - \frac{1}{3}(V_{B1O} - V_{B2O'}) + \frac{2}{3}(V_{C1O} - V_{C2O'}) \tag{2.13}$$

Equations (2.11)-(2.13) can be written in matrix form as:

$$\begin{bmatrix} V_{A1A2} \\ V_{B1B2} \\ V_{C1C2} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} V_{A1O} - V_{A2O'} \\ V_{B1O} - V_{B2O'} \\ V_{C1O} - V_{C2O'} \end{bmatrix} \tag{2.14}$$

Substituting the values of pole voltages in terms of switching functions from equations (2.4)-(2.5), motor phase voltages can be expressed as follows:

$$\begin{bmatrix} V_{A1A2} \\ V_{B1B2} \\ V_{C1C2} \end{bmatrix} = \frac{V_{DC}}{6}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} SF_a - SF_{a'} \\ SF_b - SF_{b'} \\ SF_c - SF_{c'} \end{bmatrix} \tag{2.15}$$

The combined effect of three-phase voltages $V_{A1A2}$, $V_{B1B2}$ and $V_{C1C2}$ on motor phase winding, at any instant will be given by $V_s$ as:

$$V_s = V_{A1A2} + V_{B1B2}.e^{j(2\pi/3)} + V_{C1C2}.e^{j(4\pi/3)} \tag{2.16}$$

The d-q component of space vector $V_s$ in terms of phase voltages is given by:

$$\begin{bmatrix} V_{qs} \\ V_{ds} \\ V_{os} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/2 & 1/2 & 1/2 \end{bmatrix}\begin{bmatrix} V_{A1A2} \\ V_{B1B2} \\ V_{C1C2} \end{bmatrix} \tag{2.17}$$

Motor phase voltages can also be expressed in terms of line-to-line voltages of inverter-1 and inverter-2. The line-to-line voltages of inverter-1 are labeled as $V_{A1B1}$, $V_{B1C1}$,

$V_{C1A1}$ whereas inverter-2 line-to-line voltages are labeled as $V_{A2B2}$, $V_{B2C2}$, $V_{C2A2}$. The motor phase voltages $V_{A1A2}$, $V_{B1B2}$ and $V_{C1C2}$ can be expressed in terms of line-to-line voltages as:

$$\left.\begin{aligned} V_{A1A2} - V_{B1B2} &= V_{A1B1} - V_{A2B2} \\ V_{B1B2} - V_{C1C2} &= V_{B1C1} - V_{B2C2} \\ V_{C1C2} - V_{A1A2} &= V_{C1A1} - V_{C2A2} \end{aligned}\right\} \tag{2.18}$$

Using equations (2.9) and (2.18), motor phase voltages can be written as:

$$\left.\begin{aligned} V_{A1A2} &= \frac{V_{A1B1} - V_{C1A1}}{3} - \frac{V_{A2B2} - V_{C2A2}}{3} \\ V_{B1B2} &= \frac{V_{B1C1} - V_{A1B1}}{3} - \frac{V_{B2C2} - V_{A2B2}}{3} \\ V_{C1C2} &= \frac{V_{C1A1} - V_{B1C1}}{3} - \frac{V_{C2A2} - V_{B2C2}}{3} \end{aligned}\right\} \tag{2.19}$$

### 2.4.2 Mathematical Modelling of Open-end Stator Winding Induction Motor

The open-end winding induction motor structure is obtained by opening the neutral point of the conventional squirrel cage induction motor (IM) and it does not require any design change in the motor. In the present work, an open-end stator winding induction motor is modeled using *d-q* theory in the stationary reference frame which needs fewer variables and hence analysis becomes easy. The parameters shown in Appendix-A are used to model IM and developed model is used throughout the thesis for simulation analysis.

The equivalent circuit model of an induction motor in stationary reference frame is shown in Fig. 2.4. The stator q-axis voltage component ($v_{qs}^{s}$) is given by

$$v_{qs}^{s} = \frac{p}{\omega_b}\psi_{qs}^{s} + r_s i_{qs}^{s} \tag{2.20}$$

The stator q-axis flux linkage per second can be written as follows:

$$\psi_{qs}^{s} = x_{ls} i_{qs}^{s} + \psi_{mq}^{s} \tag{2.21}$$

$$\psi_{mq}^{s} = x_m (i_{qs}^{s} + i_{qr}^{s}) \tag{2.22}$$

From equations (2.20)-(2.22) q-axis stator flux linkage can be given by

$$\psi_{qs}^{s} = \omega_b \int \{v_{qs}^{s} - \frac{r_s}{x_{ls}}(\psi_{qs}^{s} - \psi_{mq}^{s})\} dt \tag{2.23}$$

Similar analysis is carried out to evaluate stator d-axis flux linkage as given below:

$$v_{ds}^{s} = \frac{p}{\omega_b}\psi_{ds}^{s} + r_s i_{ds}^{s} \tag{2.24}$$

$$\psi_{ds}^{s} = x_{ls} i_{ds}^{s} + \psi_{md}^{s} \tag{2.25}$$

$$\psi_{md}^{s} = x_m (i_{ds}^{s} + i_{dr}^{s}) \tag{2.26}$$

$$\psi_{ds}^{s} = \omega_b \int \{v_{ds}^{s} - \frac{r_s}{x_{ls}}(\psi_{ds}^{s} - \psi_{md}^{s})\} dt \tag{2.27}$$

By rearranging equations (2.21) and (2.25), stator q-axis and d-axis currents can be expressed as:

$$i^s_{qs} = \frac{\psi^s_{mq} - \psi^s_{qs}}{x_{ls}} \tag{2.28}$$

$$i^s_{ds} = \frac{\psi^s_{ds} - \psi^s_{md}}{x_{ls}} \tag{2.29}$$

To evaluate rotor flux linkages all the quantity of rotor side are referred to the stator side and basic circuit equations are formed using equivalent circuit shown in Fig. 2.4. Equation (2.30) shows the rotor quantities referred to stator side. The rotor circuit analysis is carried out in the same way as it was carried out for stator circuit. As the rotor is short circuit therefore $v'^s_{qr}$ and $v'^s_{dr}$ are equated to zero in equations (2.31) and (2.34) . The rotor q-axis and d-axis flux linkages are expressed by equations (2.33) and (2.36) respectively.

$$\left.\begin{aligned}
\psi'^s_{qr} &= \frac{N_s}{N_r}\psi^s_{qr} = \omega_b \lambda'_{qr} = \omega_b \frac{N_s}{N_r}\lambda_{qr} \\
\psi'^s_{dr} &= \frac{N_s}{N_r}\psi^s_{dr} \\
i'^s_{qr} &= \frac{N_r}{N_s} i^s_{qr} \\
i'^s_{dr} &= \frac{N_r}{N_s} i^s_{dr} \\
L'^s_{lr} &= (\frac{N_s}{N_r})^2 L^s_{lr} \\
L_m &= \frac{3}{2}L_{ss} = \frac{3}{2}\frac{N_s}{N_r}L_{sr} = \frac{3}{2}\frac{N_s}{N_r}L_{rr}
\end{aligned}\right\} \tag{2.30}$$

Rotor q-axis analysis in stationary reference frame is as follows:

$$v'^s_{qr} = \frac{p}{\omega_b}\psi'^s_{qr} - \frac{\omega_r}{\omega_b}\psi'^s_{dr} + r'_r\,\psi'^s_{qr} = 0 \tag{2.31}$$

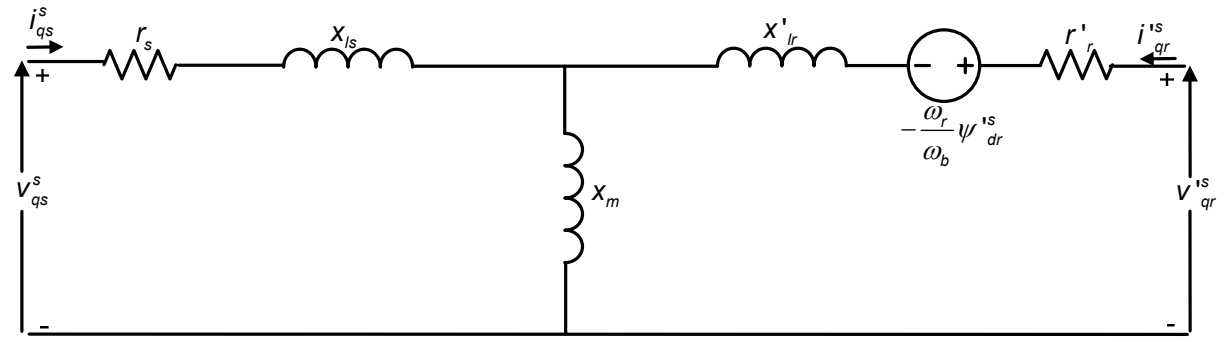
$$\psi'^s_{qr} = x'_{lr}\, i'^s_{qr} + \psi^s_{mq} \tag{2.32}$$

$$\psi'^s_{qr} = \omega_b \int \{\frac{\omega_r}{\omega_b}\psi'^s_{dr} + \frac{r'_r}{x'_{lr}}(\psi^s_{mq} - \psi'^s_{qr})\} dt \tag{2.33}$$

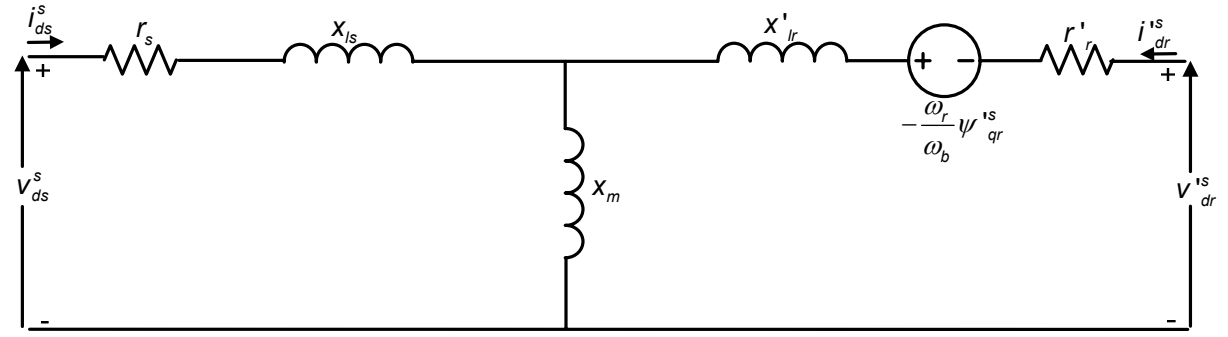
Similarly for rotor d-axis;

$$v'^s_{dr} = \frac{p}{\omega_b}\psi'^s_{dr} + \frac{\omega_r}{\omega_b}\psi'^s_{qr} + r'_r\,\psi'^s_{qr} = 0 \tag{2.34}$$

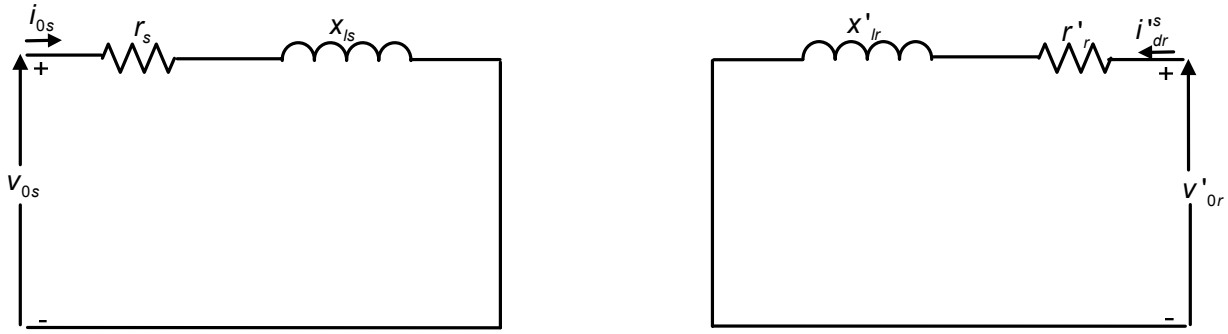
$$\psi'^s_{dr} = x'_{lr}\, i'^s_{dr} + \psi^s_{md} \tag{2.35}$$




(a) q-axis equivalent circuit




(b) d-axis equivalent circuit




(c) zero sequence equivalent circuit

Fig. 2.4: Equivalent circuit of an induction motor in stationary reference frame

$$\psi'^s_{dr} = \omega_b \int \{-\frac{\omega_r}{\omega_b}\psi'^s_{qr} + \frac{r'_r}{x'_{lr}}(\psi^s_{md} - \psi'^s_{dr})\}dt \tag{2.36}$$

The zero sequence stator and rotor currents can be computed using equations (2.37) and (2.38) respectively.

$$i_{os} = \frac{\omega_b}{x_{ls}} \int (v_{os} - i_{os} r_s)dt \tag{2.37}$$

$$i'_{or} = \frac{\omega_b}{x'_{lr}} \int (v'_{or} - i'_{or}\, r'_r)dt \tag{2.38}$$

Using equations (2.22),(2.28) and (2.32), $\psi^s_{mq}$ can be expressed as:

$$\psi^s_{mq} = x_M(\frac{\psi^s_{qs}}{x_{ls}} + \frac{\psi'^s_{qr}}{x_{lr}}) \tag{2.39}$$

Where $X_M$ is given as:

$$\frac{1}{x_M} = \frac{1}{x_m} + \frac{1}{x_{ls}} + \frac{1}{x'_{lr}} \tag{2.40}$$

Similarly using equations (2.26), (2.29) and (2.35), $\psi^s_{md}$ can be expressed as:

$$\psi^s_{md} = x_M\left(\frac{\psi^s_{ds}}{x_{ls}} + \frac{\psi'^s_{dr}}{x'_{lr}}\right) \tag{2.41}$$

The developed electromagnetic torque is given by

$$T_{em} = \frac{3}{2}\frac{P/2}{\omega_b}\left(\psi^s_{ds} i^s_{qs} - \psi^s_{qs} i^s_{ds}\right) \tag{2.42}$$

The equation of motion of the rotor is obtained by equating the inertia torque to the accelerating torque, that is

$$\frac{2J\omega_b}{P}\frac{d(\omega_r / \omega_b)}{dt} = T_{em} + T_{load} - T_{damp} \tag{2.43}$$

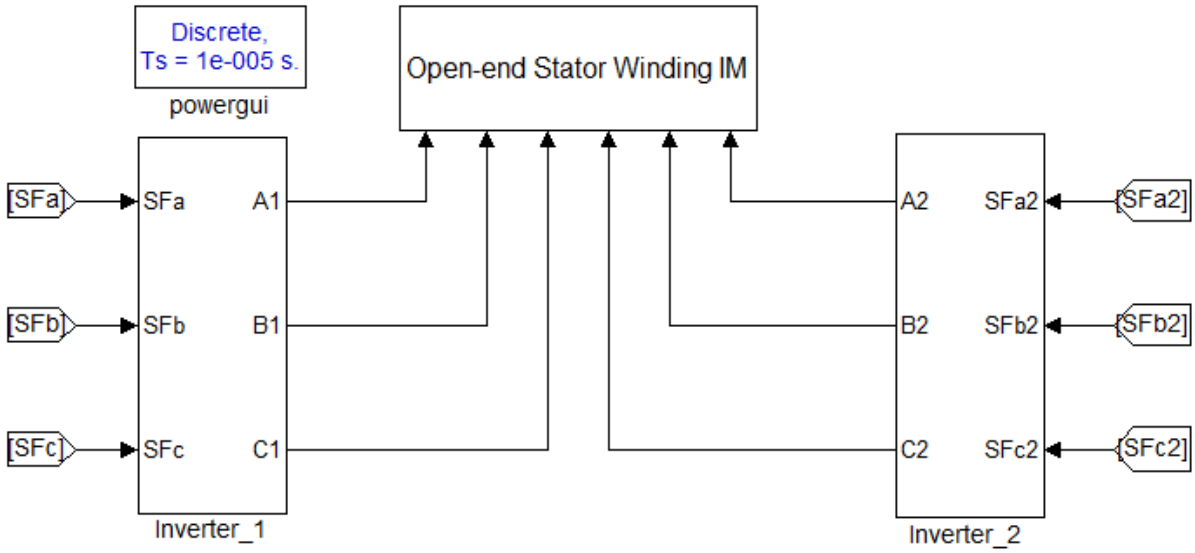
Here, P is the number of poles and $\omega_r / \omega_b$ is per unit rotor speed.

### 2.5 Simulation Studies

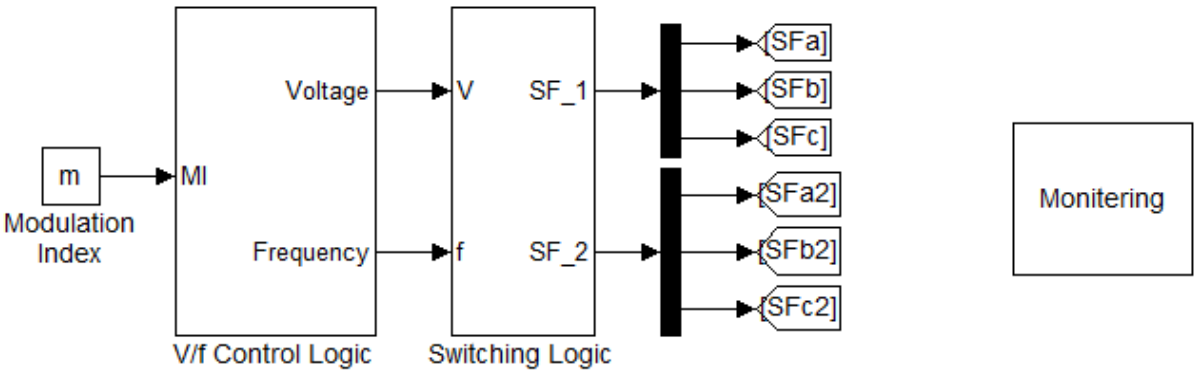
To evaluate the performance of D2L inverter scheme a MATLAB/Simulink model is developed and simulation study is carried out in fixed-point simulation mode at a sampling time of 10 µSec. S-Function concept is used to develop various blocks using mathematical equations in order to increase the simulation speed and improve the numerical stability. The developed simulink model consists of two parts, the first part is power circuit and the second part is control circuit and monitoring as shown in Fig. 2.5(a) and (b) respectively. The power circuit consists of open-end winding induction motor and D2L inverter. The parameters of the open-end winding IM used in simulation study are given in Appendix-A. The library of developed subsystems is applied to a switching function based D2L inverter scheme. Switching function based two-level inverters take switching pulses as an input signals and produced the pole voltages which are fed to the open-end winding IM. The control circuit generates the switching functions for both two-level inverters depending upon modulation index (*m*). The value of modulation index is given to *V/f* logic block which generates magnitude of reference voltage ($V^*_r$) and frequency ($f^*_m$) for switching logic block. The switching logic block uses a space vector pulse width modulation (SVPWM) technique to generate switching functions for the inverters. The monitoring block consist of several scopes and display block to measure various performance parameter of the system like voltage, current, THD, modulation index, etc. The motor is operated in constant *V/f* mode under no-load condition over the wide range of operation. The DC-link voltage needed to get a maximum phase voltage of 340V (√2*240V) for a 240 volts motor, operating under linear modulation range can be determined as:

$$\frac{2}{3}\times\frac{\sqrt{3}}{2}\times V_{DC}=340$$
$$\Rightarrow V_{DC}=588.88 \text{ Volts}$$

Therefore, for simulation study DC link voltage is taken as 600V throughout in the thesis. The simulated D2L inverter model is operated at various switching frequencies and results are tabulated in Table 2.2. It can be observed in Fig. 2.6 that with the increase in switching frequency THD decreases. Therefore, minimum switching frequency ($f_c$) 1kHz is selected to further improve the performance by increasing the number of levels. To cover the entire range of modulation three values of modulation indices ($m$) 0.2, 0.8 and 1 correspond to frequencies ($f^*_m$) of 10, 40 and 50Hz respectively are selected. The motor phase-A voltage ($V_{A1A2}$), phase-A current ($i_{A1A2}$), their harmonic spectrums, inverters pole-A voltages ($V_{A1O}$, $V_{A2O'}$) and difference of inverters pole-A voltages ($V_{A1O}$ - $V_{A2O'}$) are considered as evaluation criteria. The simulation results are presented for steady-state, as well as for transient-state condition.




(a)




(b)

Fig. 2.5: Simulink model of D2L inverter scheme (a) Power circuit (b) Control circuit and monitoring

Table 2.2: Effect of switching frequency on THD of motor phase-A voltage

| Modulation index(*m*) | Switching frequency | THD of phase-A voltage in % | Amplitude of dominant harmonic component in % |
|---|---|---|---|
| 0.2 | 1kHz | 132.53 | 72 |
| | 3kHz | 128.49 | 71.2 |
| | 5kHz | 121.94 | 66.52 |
| | 10kHz | 109.69 | 56.15 |
| 0.4 | 1kHz | 61.20 | 15.48 |
| | 3kHz | 62.24 | 15.08 |
| | 5kHz | 59.57 | 14.53 |
| | 10kHz | 50.73 | 14.13 |
| 0.8 | 1kHz | 32.18 | 12 |
| | 3kHz | 31.75 | 11.25 |
| | 5kHz | 31.44 | 10.85 |
| | 10kHz | 31.30 | 10.77 |

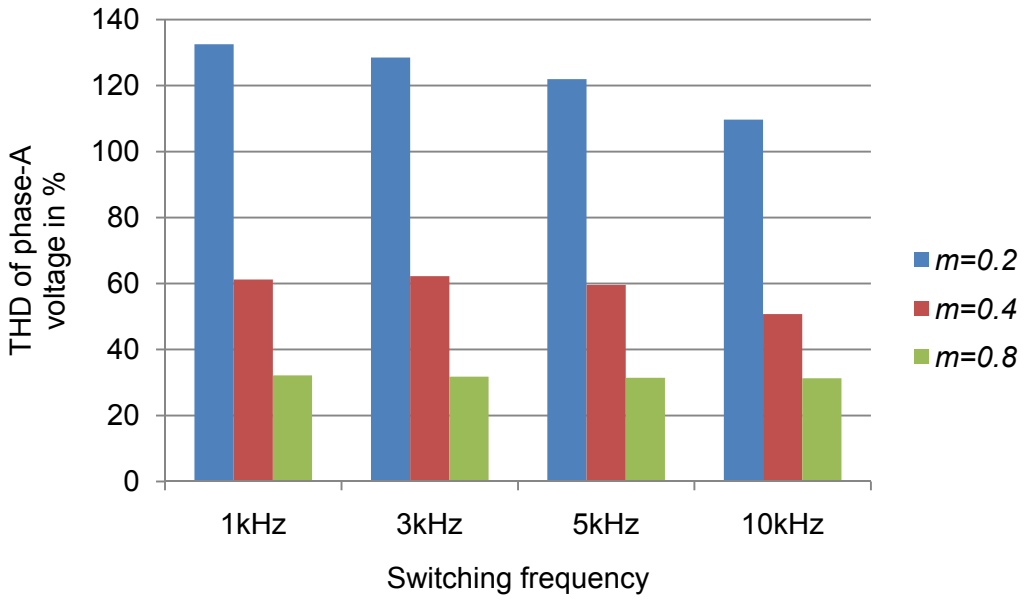
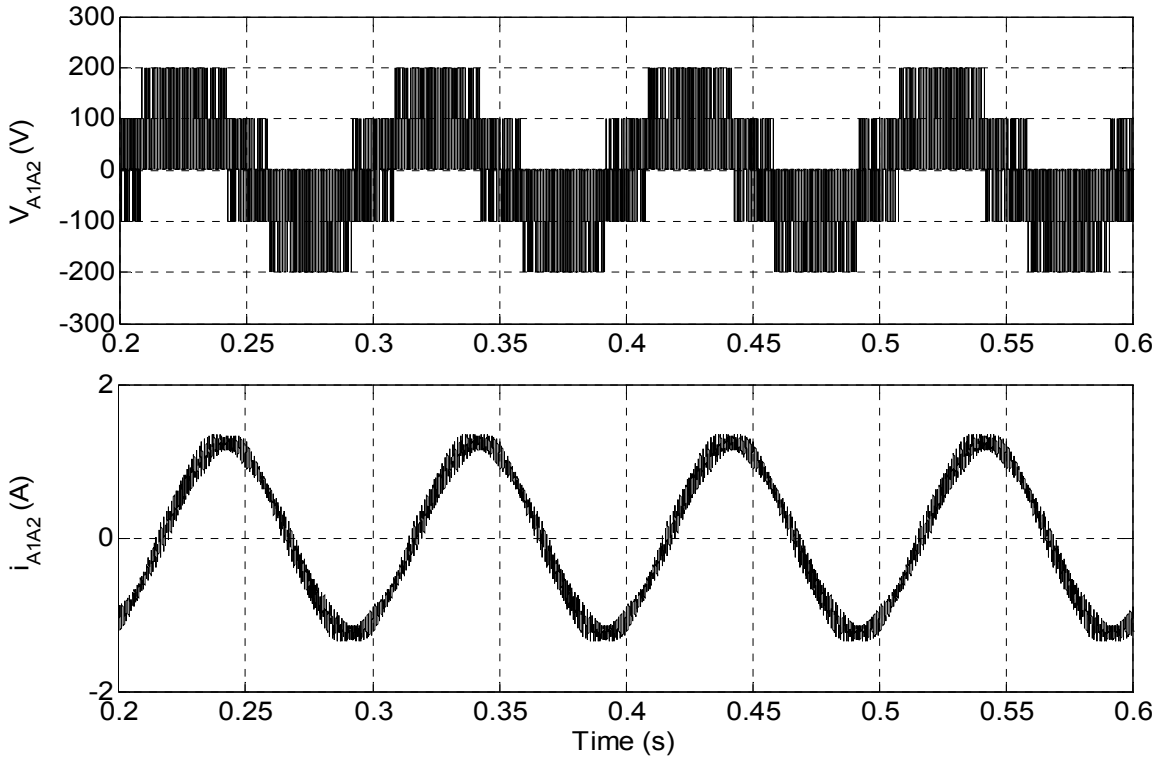


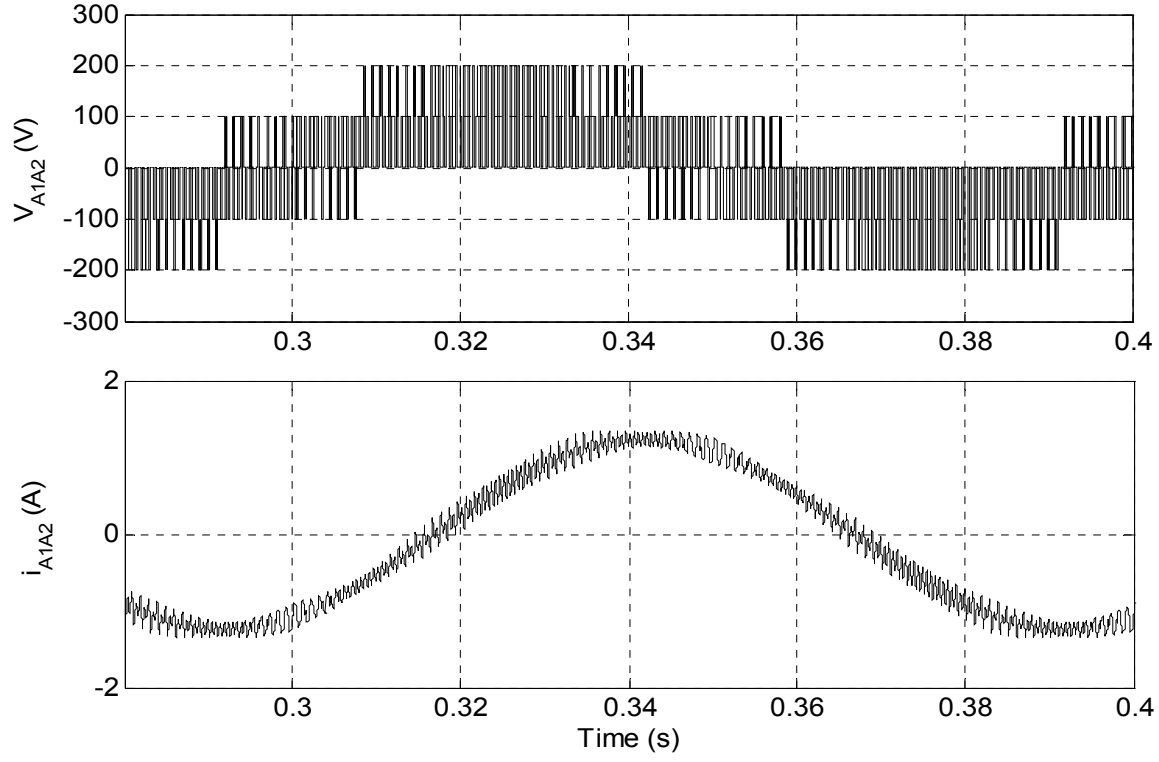

Fig. 2.6: Graph between THD of motor phase-A voltage and switching frequency for different value of modulation index

### 2.5.1 Simulation Results and Discussion

The steady-state performance of D2L inverter for open-end IM drive at no load is shown in Fig. 2.7 - Fig. 2.15. The motor phase-A voltage ($V_{A1A2}$) and current ($i_{A1A2}$) at modulation index $m$ =0.2 is shown in Fig. 2.7. At this modulation index motor operates at fundamental frequency ($f^*_m$) of 10Hz. The harmonic spectrum of phase-A voltage and current with respect to their fundamental component are shown in the Fig. 2.8(a) and Fig. 2.8(b) respectively. These spectrums show that the dominant harmonic component of phase voltage and current occur at the side band of order of 200 (2 $f_c/f^*_m$ =2x1000/10). The amplitude of dominate harmonic component of voltage and current are 72% and 5% of their fundamental. The lower order harmonics responsible for higher losses are significantly low. The pole voltages and difference in pole voltages of inverter-1 and inverter-2 are shown in Fig. 2.9. It can be noted from pole voltages waveform that both inverters operate in PWM mode only for half of the duration of fundamental cycle. This feature can lead to use of low switching frequency rating power semiconductor devices in dual two-level inverter scheme. Fig. 2.10 shows the performance of D2L inverter scheme when IM operated at modulation index $m$ =0.8 corresponds to fundamental frequency ($f^*_m$) of 40Hz at no load. The phase voltage waveform clearly shows the performance equivalent to three-level inverter. The harmonic spectrum of phase-A voltage and current with respect to their fundamental component are shown in the Fig. 2.11(a) and Fig. 2.11(b) respectively. These spectrums show that the dominant harmonic component of phase voltage occur at the side band of order of 50 (2 $f_c/f^*_m$ =2x1000/40) with the amplitude of 12% of the fundamental voltage. The overall THD of phase current is 10.58% of the fundamental. The lower order harmonics responsible for higher losses are little bit high as compared to the two-level mode of operation. The pole voltages and difference in pole voltages of inverter-1 and inverter-2 for three-level mode of operation are shown in Fig. 2.12. The performance of SVPWM based D2L inverter scheme is also evaluated in overmodulation region and result are shown in Fig. 2.13 - Fig. 2.15. The modulation index $m$ =1 and corresponding fundamental frequency $f^*_m$ is equal to 50 for this mode of operation. The motor phase-A voltage and current are shown in Fig. 2.13 and their harmonic spectrums, shown in Fig. 2.14. It can be observed from voltage and current harmonic spectrums that lower order harmonics are increased in overmodulation region. The pole voltages and difference in pole voltages of inverter-1 and inverter-2 for overmodulation mode are shown in Fig. 2.15. However, the limit of linear modulation ends at 0.866, even though motor is operated at $m$ =1 just to show the operation of inverter in over modulation region. In the subsequent chapters motor is operated under linear modulation range.

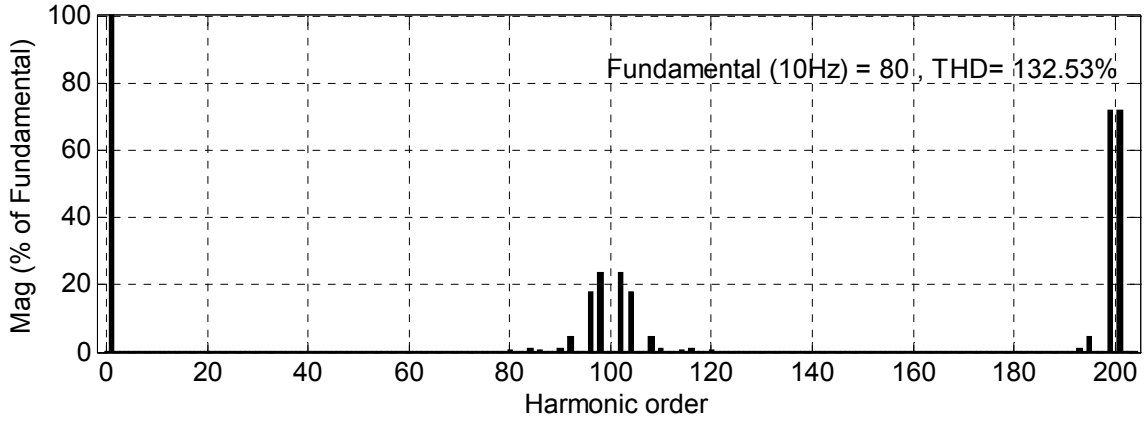



(a)

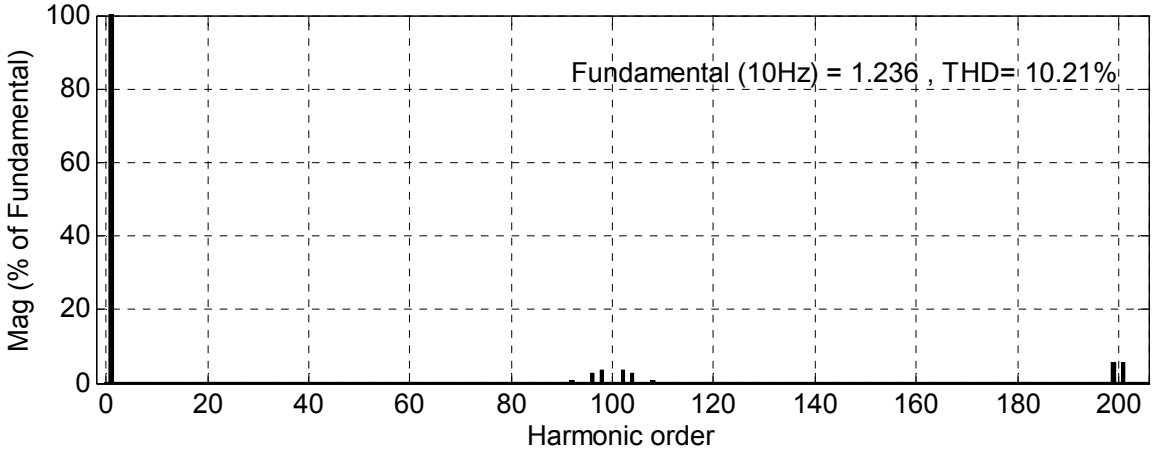



(b)

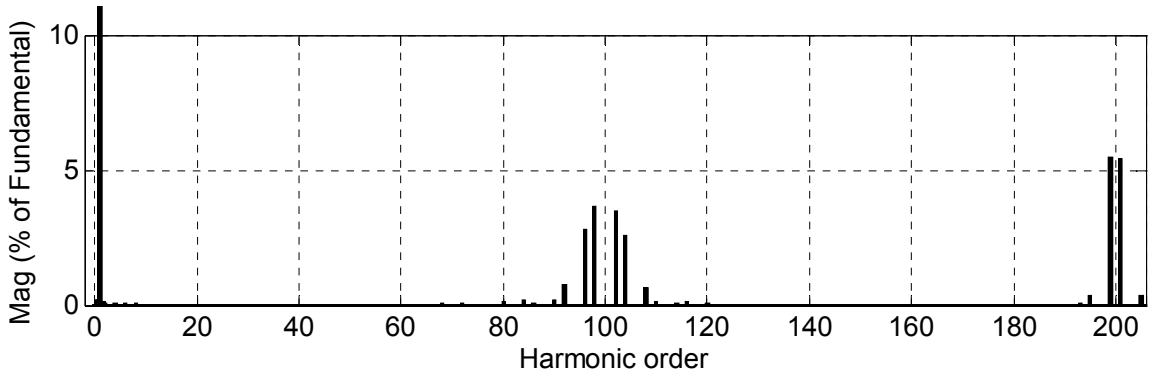
Fig. 2.7: (a) Motor phase-A, voltage ($V_{A1A2}$) and current ($i_{A1A2}$) at $m$=0.2; $f^*_m$ =10Hz for SVPWM based D2L inverter for open-end IM drive at no load (b) zoom view of waveforms shown in (a)




(a)




(b)




(c)

Fig. 2.8: (a) Harmonic spectrum of phase-A voltage ($V_{A1A2}$) at $m$=0.2; $f^*_m$ =10Hz
(b) Harmonic spectrum of phase-A current ($i_{A1A2}$) at $m$=0.2; $f^*_m$ =10Hz
(c) Zoom view of harmonic spectrum shown in (b)

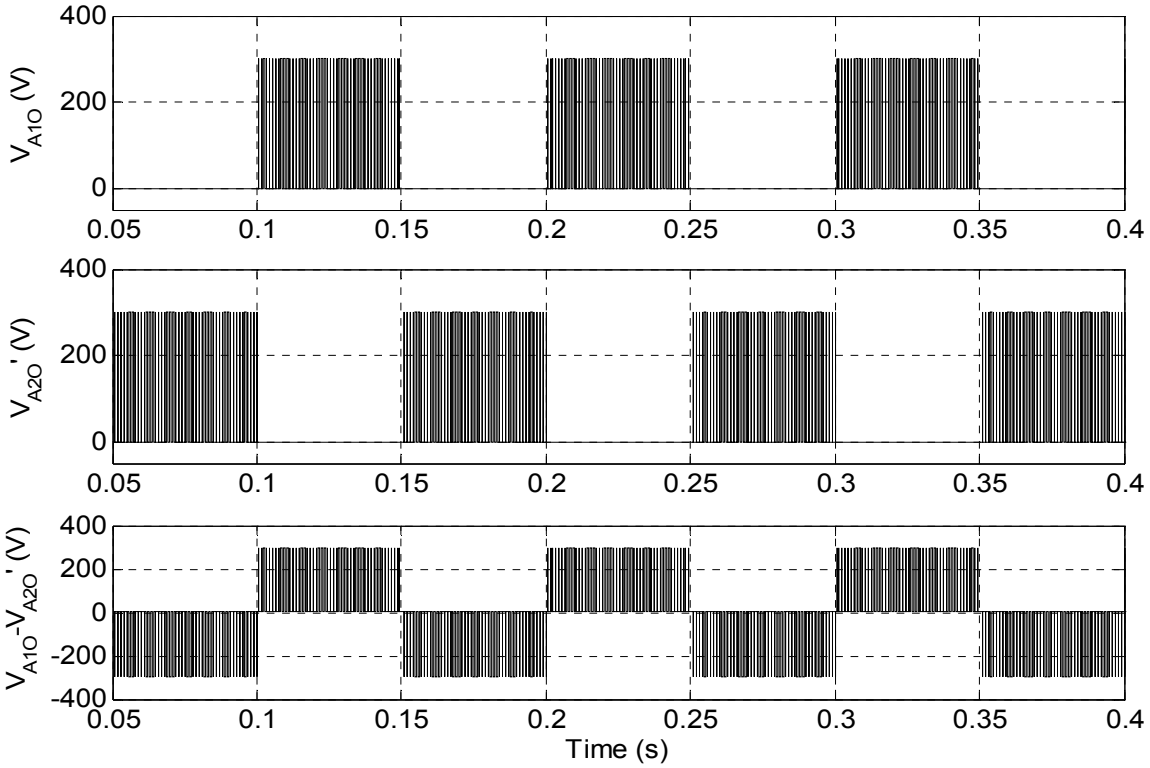



Fig. 2.9: Top trace; Inverter-1 pole voltage ($V_{A1O}$), Middle trace; Inverter-2 pole voltage ($V_{A2O'}$), Bottom trace; Difference of inverter-1and -2 pole voltages ($V_{A1O}$ - $V_{A2O'}$) at $m$=0.2; $f^*_m$ =10Hz

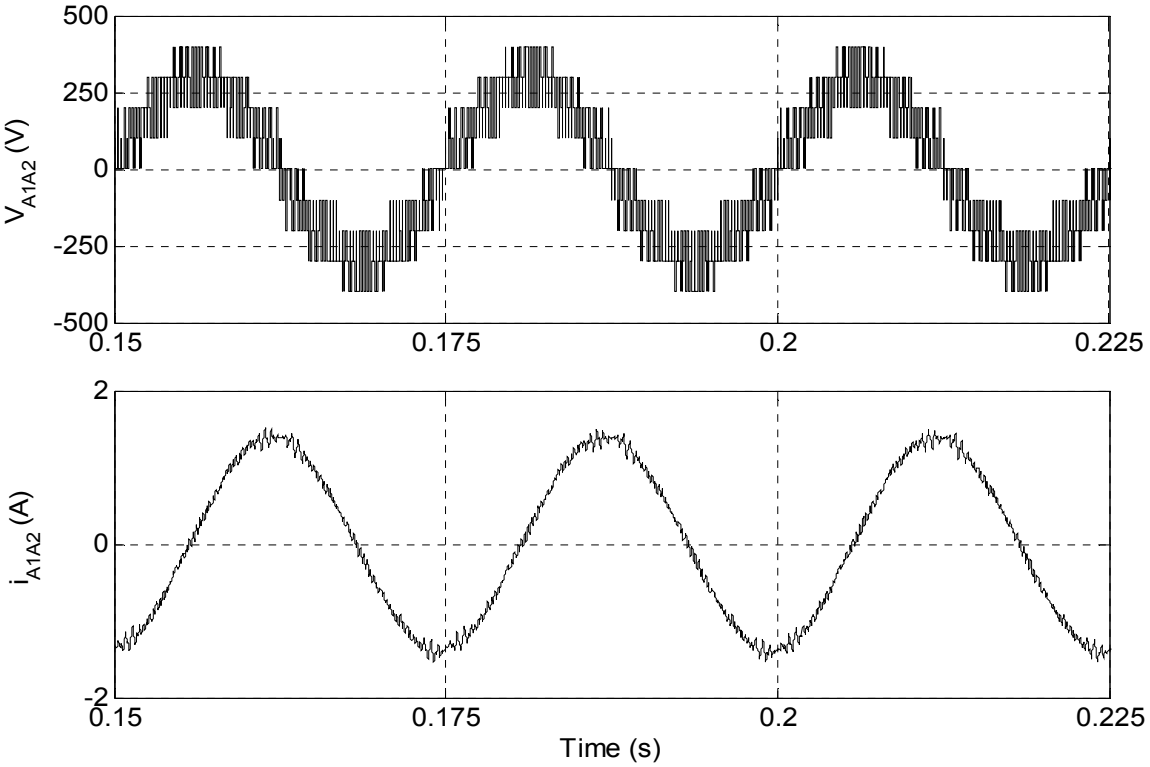
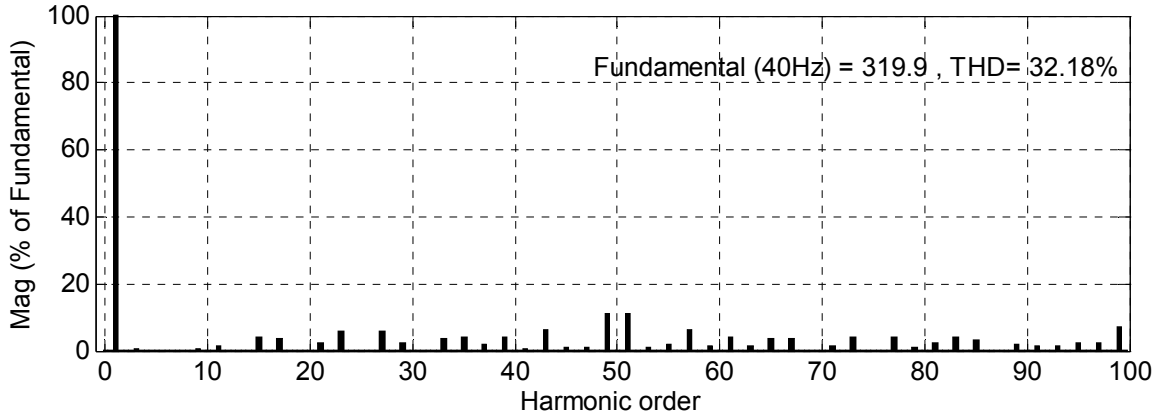
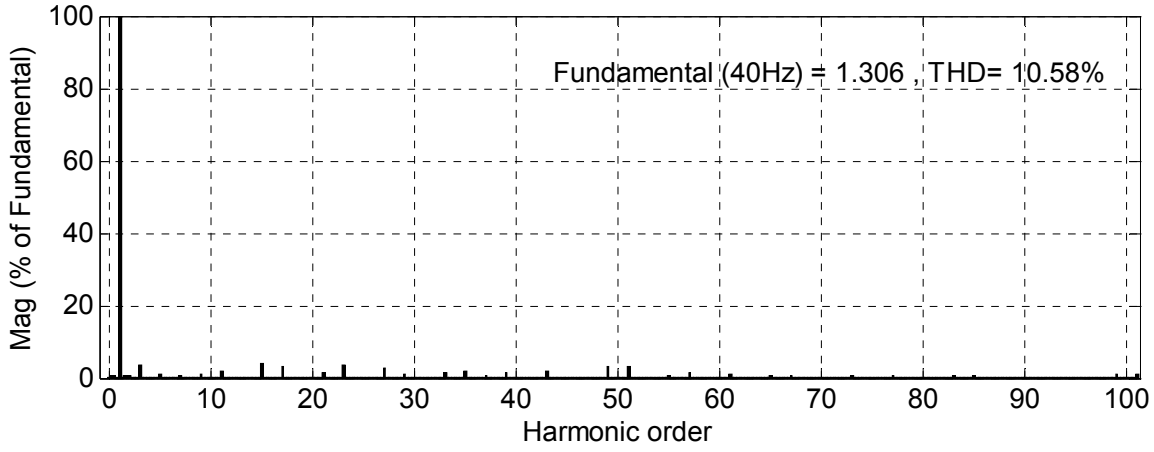


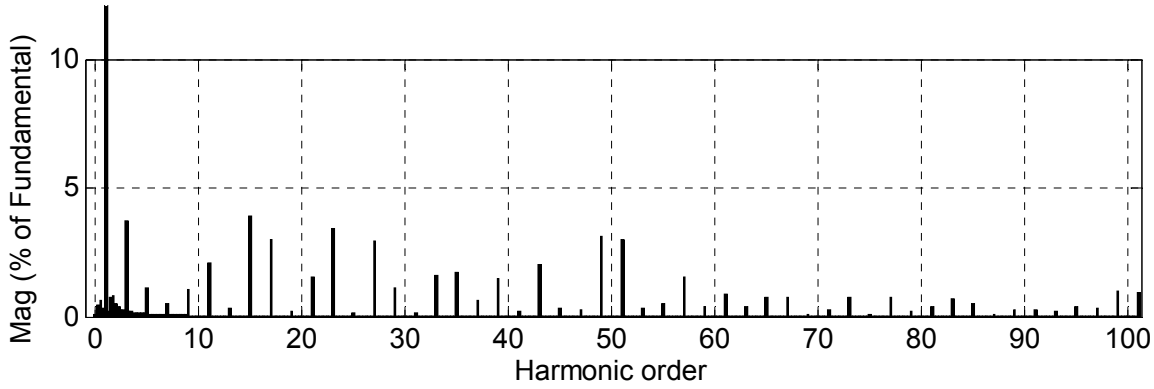

Fig. 2.10: Motor phase-A, voltage ($V_{A1A2}$) and current ($i_{A1A2}$) at $m$=0.8; $f^*_m$ =40Hz for SVPWM based D2L inverter for open-end IM drive at no load




(a)




(b)




(c)

Fig. 2.11: (a) Harmonic spectrum of phase-A voltage ($V_{A1A2}$) at $m$=0.8; $f^*_m$ =40Hz
(b) Harmonic spectrum of phase-A current ($i_{A1A2}$) at $m$=0.8; $f^*_m$ =40Hz
(c) Zoom view of harmonic spectrum shown in (b)

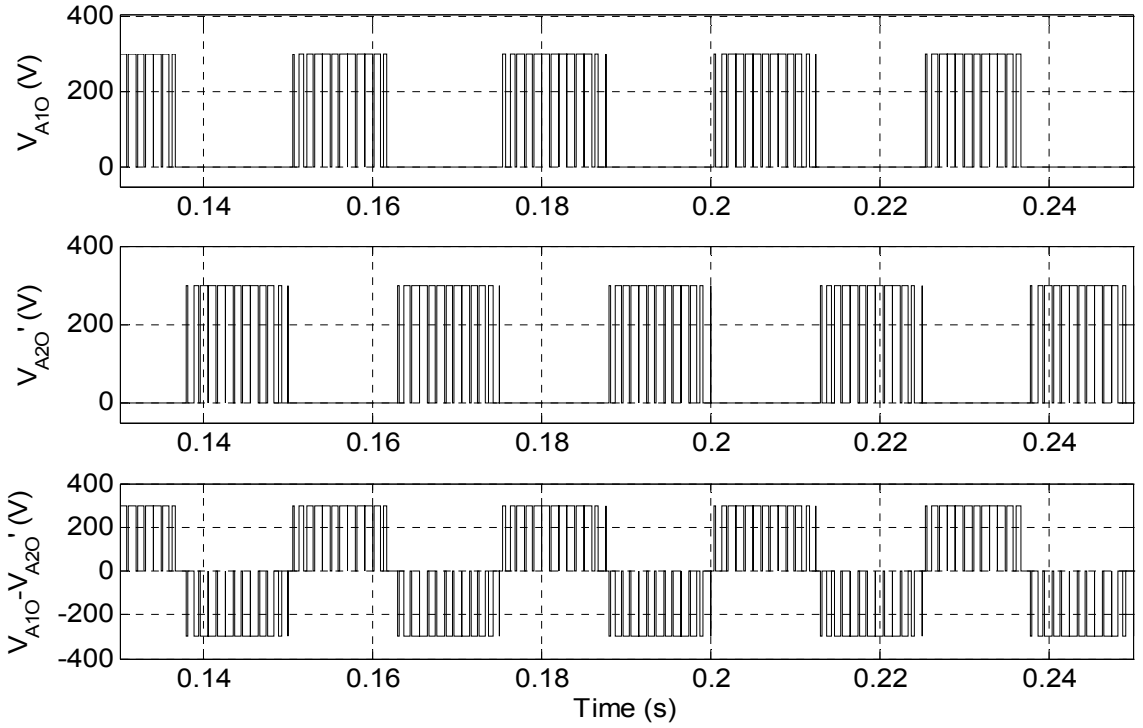



Fig. 2.12: Top trace; Inverter-1 pole voltage ($V_{A1O}$), Middle trace; Inverter-2 pole voltage ($V_{A2O'}$), Bottom trace; Difference of inverter-1and -2 pole voltages ($V_{A1O}$ - $V_{A2O'}$) at $m$=.08; $f^*_m$ =40Hz

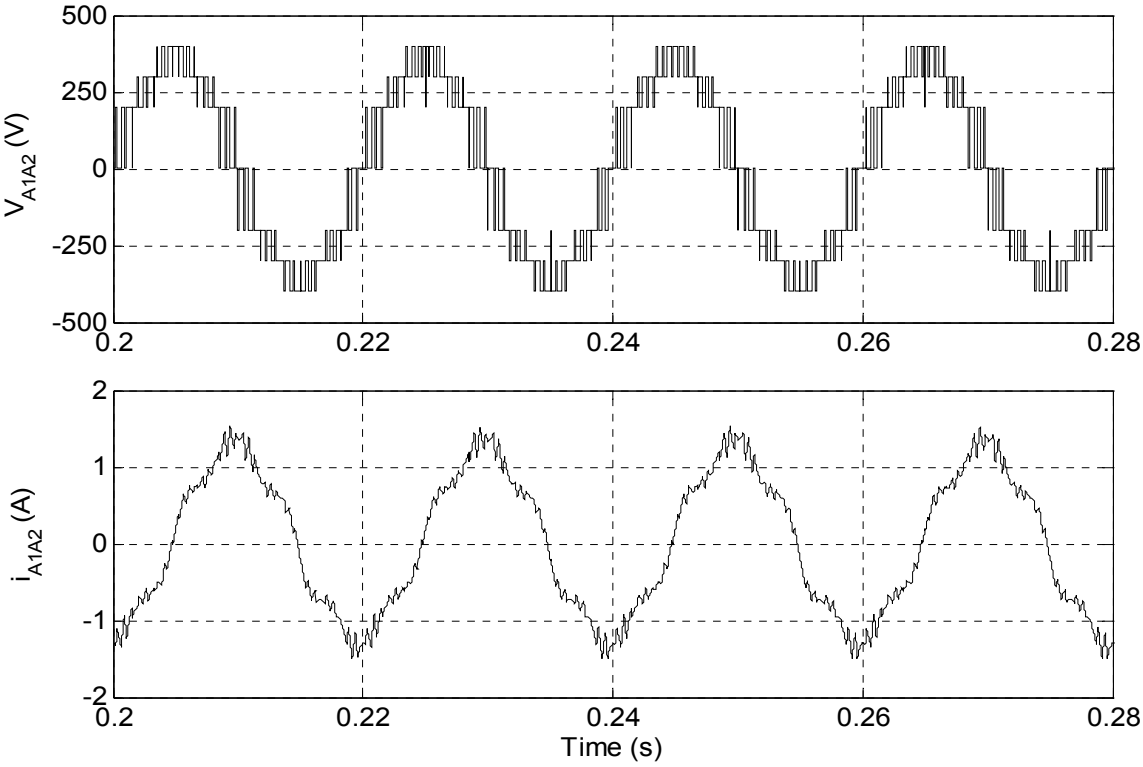
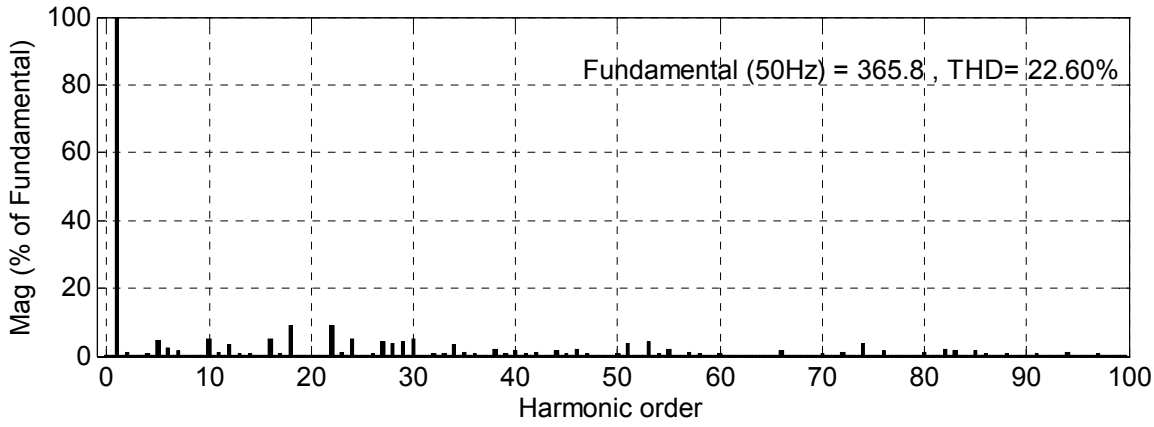
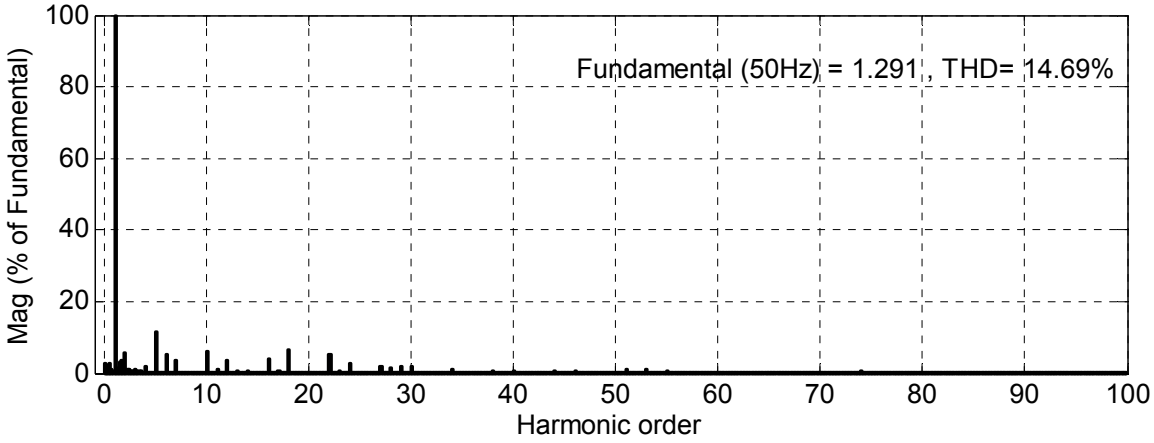


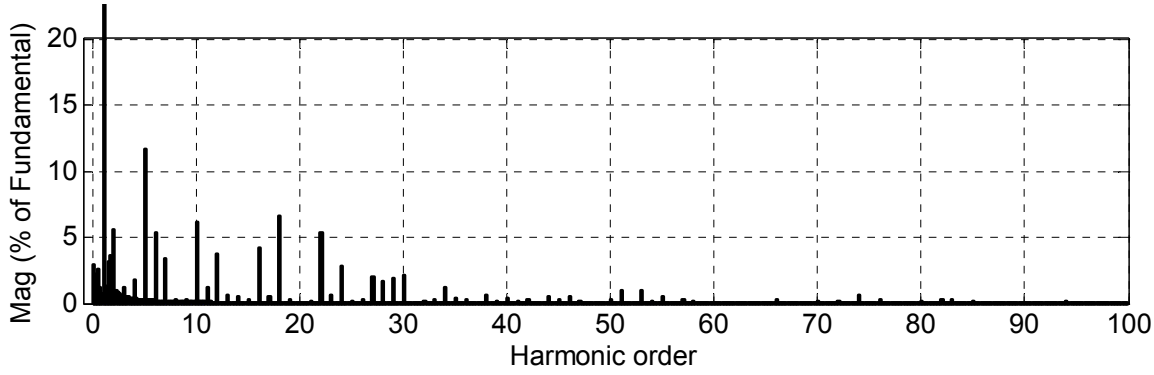

Fig. 2.13 : Motor phase-A, voltage ($V_{A1A2}$) and current ($i_{A1A2}$) at $m$=1; $f^*_m$ =50Hz for SVPWM based D2L inverter for open-end IM drive at no load




(a)




(b)




(c)

Fig. 2.14: (a) Harmonic spectrum of phase-A voltage ($V_{A1A2}$) at $m$=1.0; $f^*_m$ =50 H
(b) Harmonic spectrum of phase-A current ($i_{A1A2}$) at $m$=1.0; $f^*_m$ =50Hz
(c) Zoom view of harmonic spectrum shown in (b)

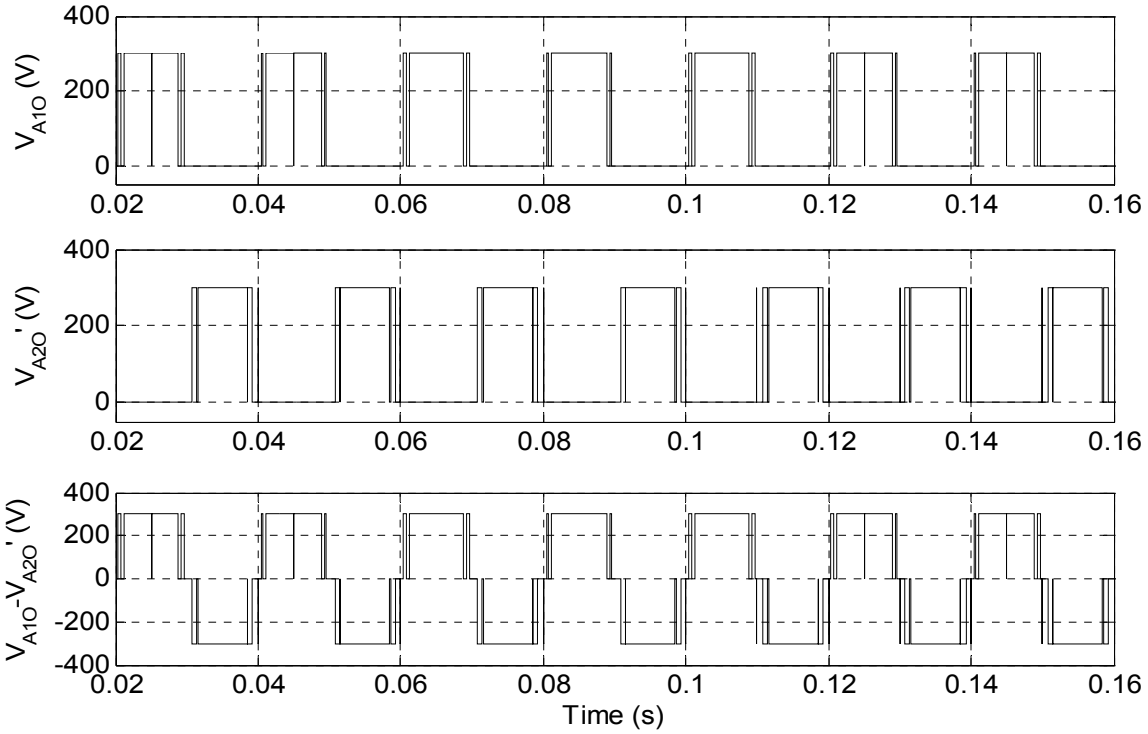
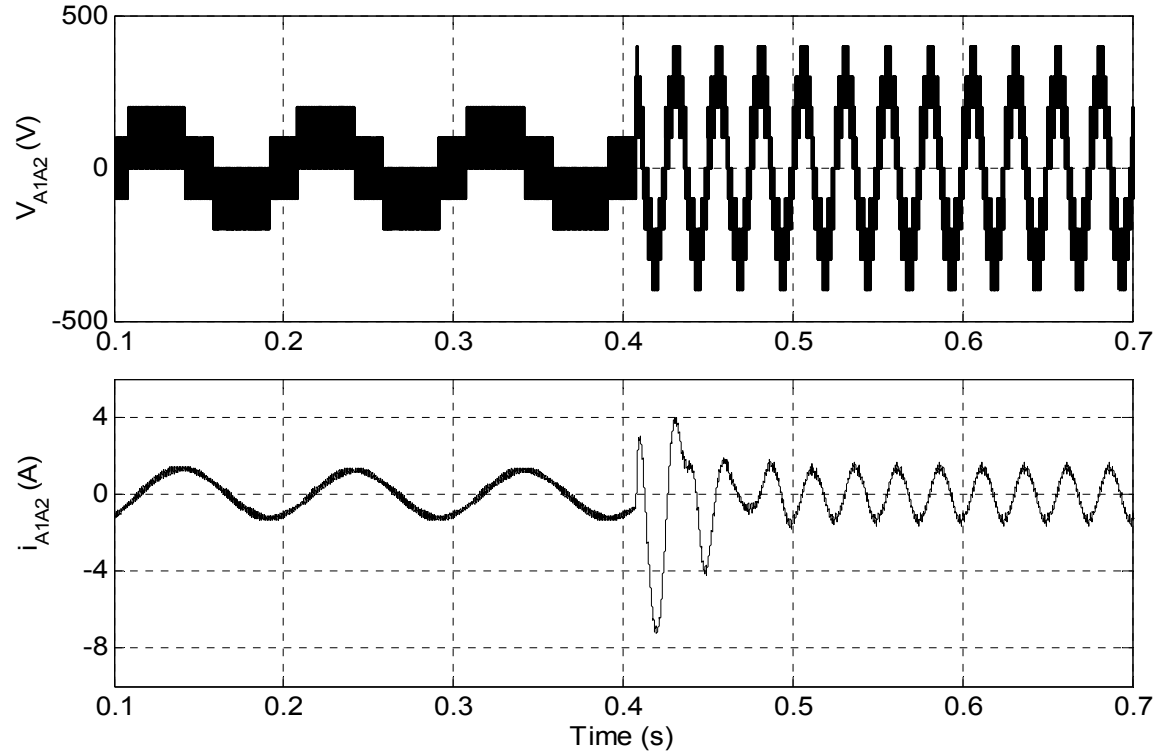
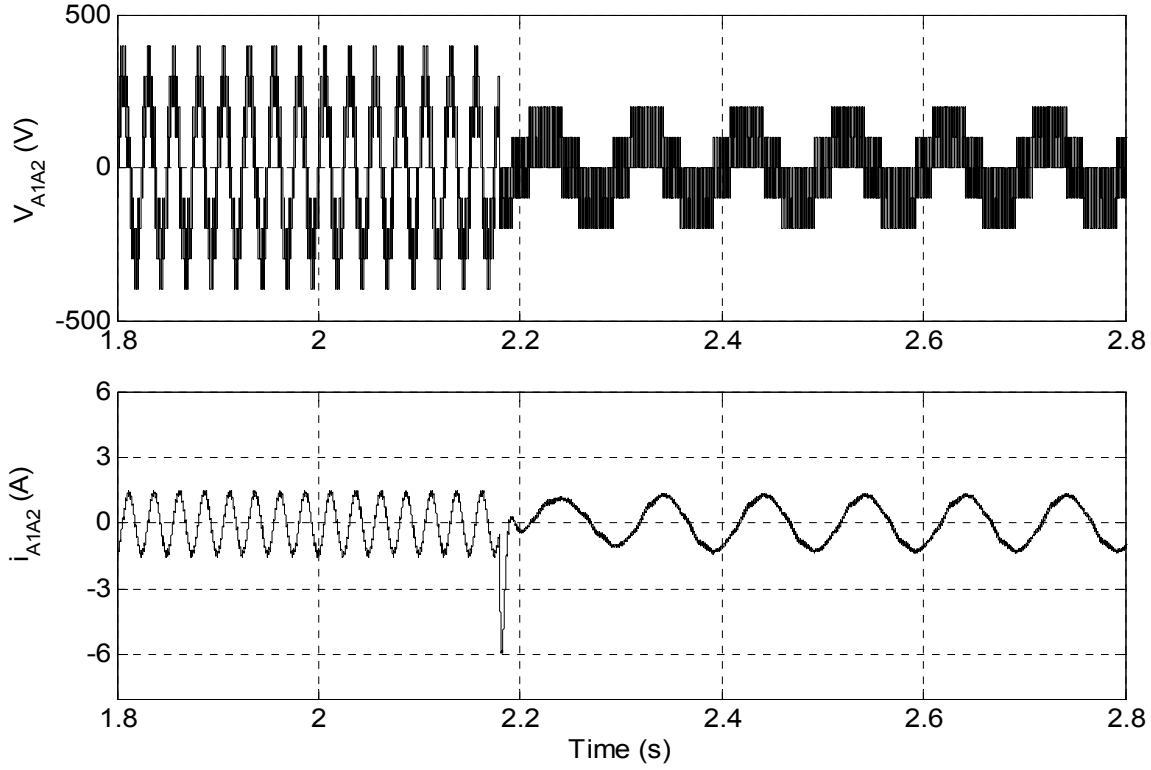



Fig. 2.15: Top trace; Inverter-1 pole voltage ($V_{A1O}$), Middle trace; Inverter-2 pole voltage ($V_{A2O'}$), Bottom trace; Difference of inverter-1and -2 pole voltages ($V_{A1O}$ - $V_{A2O'}$) at $m$=1; $f^*_m$ =50Hz




(a)




(b)

Fig. 2.16: (a) Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A1A2}$ (lower trace) waveforms under sudden change in modulation index from 0.2 to 0.8
(b) Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A1A2}$ (lower trace) waveforms under sudden change in modulation index from 0.8 to 0.2

The performance of D2L inverter fed open-end IM is also investigated against transient state stability by changing the modulation index from 0.2 to 0.8 and from 0.8 to 0.2. Fig. 2.16 (a) shows the motor phase voltage and current waveforms during the changeover of modulation index from 0.2 to 0.8. Similar types of waveforms for sudden change in modulation index from 0.8 to 0.2 are shown in Fig. 2.16 (b). It is depicted in phase voltage waveform that changeover of modulation index from lower to higher or from higher to lower take place instantaneously. The motor phase current and hence the motor speed attains its steady state in within few cycles.

## 2.6 Conclusion

The dual two-level (D2L) inverter produces the same voltage levels across the phase winding of induction motor as they are generated by three-level inverter. The D2L scheme completely eliminates the requirement of clamping diodes and DC-link capacitors which are required in neutral point clamped (NPC) inverter. Three-level cascade H-bridge (CHB) requires three isolated DC supply of rating $V_{DC}$, whereas the D2L inverter scheme uses only two isolated DC supplies of $V_{DC}/2$ rating and switching devices voltage rating is also reduced by half. In comparison to flying capacitor MLI topology the D2L inverter scheme does not need any flying capacitors. A switching function based mathematical model of dual two-level inverter is developed and the performance is evaluated under different operating conditions. The performance of the inverter under steady state and transient state is found satisfactory, but harmonics contents in the output voltage are quite high.

In the next chapter, a 5-level inverter is realized by using three numbers of conventional two-level inverters to improve the quality of output voltage.

# CHAPTER 3: FIVE-LEVEL INVERTER FOR INDUCTION MOTOR DRIVE

*[In this chapter a 5-level inverter scheme is presented for open-end induction motor drive. A Switching function based mathematical model of 5-level inverter is proposed. Procedure for determining the DC link ratio to achieve the maximum number of levels in output voltage is discussed. A simulation model of 5-level inverter scheme is developed using SimPowerSystems™ and Simulink toolbox of MATLAB software and tested on 1.5-kW open-end winding induction motor]*

## 3.1 Introduction

Multilevel inverter of 5-level and above for medium and high power applications is an area of extensive research though 3-level inverters are now being used for various applications [180]. The 3-level diode-clamped inverter topology is one of the well established topology among various multilevel configurations, presented in the literature. Number of papers and patents published in the area of 3-level NPC inverter shows the importance of research on this topology [23], [149]. This topology suffers a major problem of neutral point fluctuation due to unbalancing of DC link capacitors voltages [31], [36]. Further extension of this topology to 5-level is more complex and required several clamping diodes of different ratings. 5-level inversion can also be achieved by feeding an open-end winding IM from both ends by 3-level inverter with symmetrical DC link [74], [181], [182]. In this chapter, D2L scheme presented in previous chapter is further explored to achieve 5-level structure by using three numbers of conventional two-level inverters [72], [180]. In this configuration an open-end winding IM is fed by 3-level inverter from one end and other end is fed by two-level inverter [180]. This structure does not require any clamping diodes and there is no issue of voltage unbalancing. When compared with the series connected H-bridge, it uses three isolated DC sources and 18 switching devices whereas cascade H-bridge (CHB) topology needs six isolated DC sources and 24 switching devices. Resultant space vector locations generated by adopted 5-level inverter scheme for open-end winding IM are similar to a 5-level neutral point clamped (NPC) inverter. It offers reduced harmonic distortions with reduced switching frequency, lower dv/dt and higher voltage capability. Moreover, the modular approach of the inverter makes its implementation simple and reliable.

## 3.2 5-Level Inverter Scheme for Induction Motor Drive

### 3.2.1 Power Circuit

The power circuit of the 5-level inverter scheme for open-end induction motor drive is shown in Fig. 3.1. Five-level inversion operation is achieved by feeding one end of the open-end winding IM by 3-level inverter-A and other end by two-level inverter-B. 3-level inverter-A is realized by cascading two conventional two-level inverter-1 and inverter-2. The DC link voltage of two-level inverter-1 and inverter-B is $V_{DC}/4$ each, whereas two-level inverter-2 is of

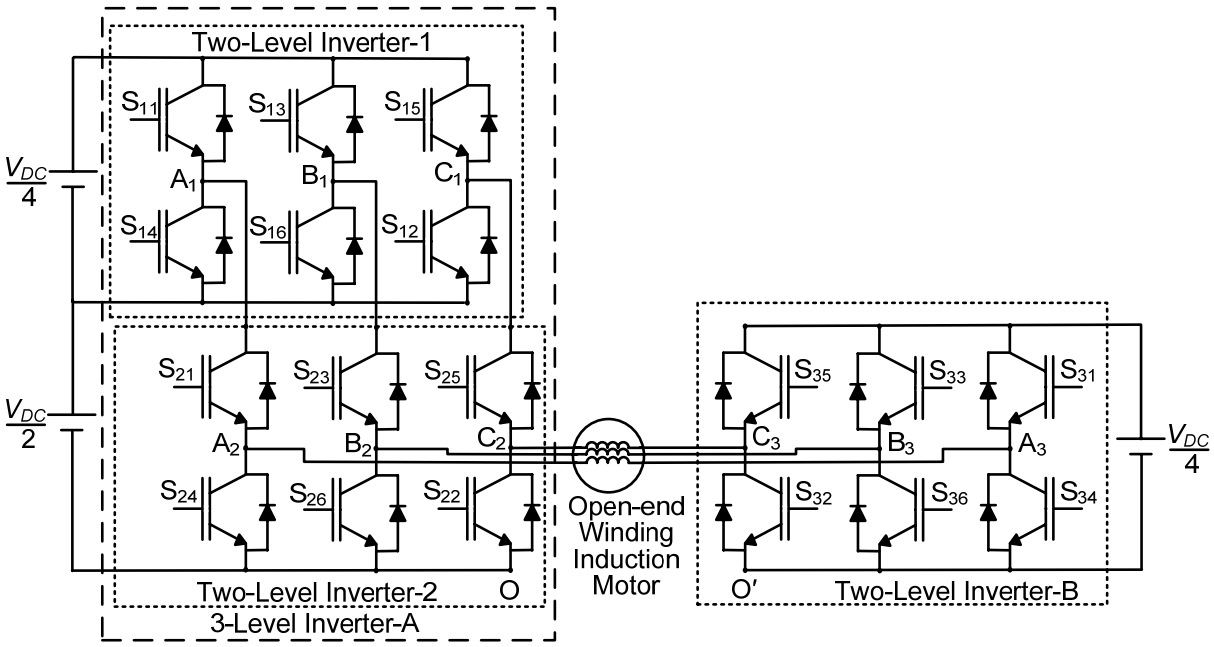



Fig. 3.1: Power circuit of 5-level inverter scheme for open-end winding induction motor drive

$V_{DC}/2$, where $V_{DC}$ is the equivalent DC-link voltage required to operate the conventional two-level inverter fed induction motor drive. All three conventional two-level inverters are powered by isolated DC sources. This scheme uses asymmetrical DC link voltages to generate five levels in phase voltage of induction motor. The 3-level inverter pole voltages $V_{A2O}$, $V_{B2O}$ or $V_{C2O}$ can have three levels 0, $V_{DC}/2$ and $3V_{DC}/4$ independently. The two-level inverter-B pole voltages with respect to its own reference point O′ are denoted as $V_{A3O'}$, $V_{B3O'}$ and $V_{C3O'}$. These pole voltages can have two levels 0 and $V_{DC}/4$ independently. The combined effect of these two inverters generates five levels as $-V_{DC}/4$, 0, $+V_{DC}/4$, $+V_{DC}/2$ and $+3V_{DC}/4$.

### 3.2.2 Switching Logic

The pole voltage $V_{A2O}$ of 3-level inverter-A (Fig. 3.1) will be at level of $+3V_{DC}/4$ if the switch $S_{11}$ and $S_{21}$ are made to turn 'ON', and at level of $+V_{DC}/2$ if the switch $S_{14}$ and $S_{21}$ are made to turn 'ON'. The pole voltage $V_{A2O}$ will be zero if the switch $S_{24}$ is made to turn 'ON'. Any pole voltage of 3-level inverter-A $V_{A2O}$, $V_{B2O}$ or $V_{C2O}$ can have these three levels by proper selection of switches of 3-level 'Inverter-A' which are made to be turned 'ON'. Similarly the pole voltage $V_{A3O'}$ of inverter-B (Fig. 3.1) can have voltage level of $+V_{DC}/4$ if the switch $S_{31}$ is made to turn 'ON', and at level of 0 if the switch $S_{34}$ is made to turn 'ON'. Any pole voltage of two-level inverter-B $V_{A3O'}$, $V_{B3O'}$ or $V_{C3O'}$ can have these two levels by proper selection of switches of two-level 'Inverter-B', which are made to be turned 'ON'. The combined effect of both two-level inverters is generation of five distinct voltage levels in the phase voltage of open-end winding induction motor as shown in Table 3.1. It is clear from the Table 3.1 that the voltage levels of $-V_{DC}/4$ (Level-$L_1$) and 0 (Level-$L_2$) can be generated by clamping the inverter-A at 'zero' voltage level and switching the inverter-B

Table 3.1: Five levels realised in phase- A for combinations of pole voltages of inverter-A and inverter-B

| Level | Pole voltage of 3-level Inverter-A ($V_{A2O}$) | Pole voltage of two-level Inverter-B ($V_{A3O'}$) | Motor phase-A voltage level ($V_{A2O}$ -$V_{A3O'}$) |
|---|---|---|---|
| $L_1$ | 0 | $V_{DC}/4$ | $-V_{DC}/4$ |
| $L_2$ | 0 | 0 | 0 |
| $L_3$ | $V_{DC}/2$ | $V_{DC}/4$ | $+V_{DC}/4$ |
| $L_4$ | $V_{DC}/2$ | 0 | $+V_{DC}/2$ |
| $L_5$ | $3V_{DC}/4$ | 0 | $+3V_{DC}/4$ |

Table 3.2: Switching states of phase-A related switches of all two-level inverters for 5-level operation

| Level | Motor phase-A voltage level | Switch (state) Inverter-1 | Switch (state) Inverter-2 | Switch (state) Inverter-B |
|---|---|---|---|---|
| $L_1$ | $-V_{DC}/4$ | $S_{14}$ (ON) | $S_{24}$ (ON) | $S_{31}$ (ON) |
| $L_2$ | 0 | $S_{14}$ (ON) | $S_{24}$ (ON) | $S_{34}$ (ON) |
| $L_3$ | $+V_{DC}/4$ | $S_{14}$ (ON) | $S_{21}$ (ON) | $S_{31}$ (ON) |
| $L_4$ | $+V_{DC}/2$ | $S_{14}$ (ON) | $S_{21}$ (ON) | $S_{34}$ (ON) |
| $L_5$ | $+3V_{DC}/4$ | $S_{11}$ (ON) | $S_{21}$ (ON) | $S_{34}$ (ON) |

between $V_{DC}/4$ and zero. Similarly to get the voltage level of $+V_{DC}/4$ (Level-$L_3$) and $+V_{DC}/2$ (Level-$L_4$), inverter-A is clamped at $V_{DC}/2$ and inverter-B switched between $V_{DC}/4$ and zero. Switching states of corresponding switches of all two-level inverters to realize five levels across the phase-A winding of open-end induction motor are shown in Table 3.2. Similar logic can also be implemented for others phases. Switches correspond to same leg of any two-level inverter operate in complementary fashion. The switches of 'Inverter-2' have to be rated for $3V_{DC}/4$ because they have to block voltage level of $3V_{DC}/4$ when the top switches of inverter-1 are 'ON'.

### 3.2.3 Analysis of Voltage Space Vectors

Assuming points O and O′ of the inverters shown in Fig. 3.1 are connected then the common mode voltage $V_{OO'}$ will be zero and the three phase voltages $V_{A2A3}$, $V_{B2B3}$ and $V_{C2C3}$ of open-end winding induction motor in terms of pole voltages will be given by

$$V_{A2A3} = V_{A2O} - V_{A3O'} \tag{3.1}$$

$$V_{B2B3} = V_{B2O} - V_{B3O'} \tag{3.2}$$

$$V_{C2C3} = V_{C2O} - V_{C3O'} \tag{3.3}$$

The net effect of these 3-phase voltages on 120º apart motor phase winding, at any instant is denoted by equivalent voltage space vector $V_s$ as:

$$V_s = V_{A2A3} + V_{B2B3}.e^{j(2\pi/3)} + V_{C2C3}.e^{j(4\pi/3)} \quad (3.4)$$

The voltage space vector $V_s$ in terms of pole voltage is given by equation (3.5).

$$V_s = (V_{A2O} - V_{A3O'}) + (V_{B2O} - V_{B3O'}).e^{j(2\pi/3)} + (V_{C2O} - V_{C3O'}).e^{j(4\pi/3)} \quad (3.5)$$

The voltage space vector $V_s$ can be resolved along α-β axis as shown in Fig. 3.2, where α-axis is along the phase-A axis and β-axis is 90 degree apart from α-axis. $V_s$ will be given by:

$$V_s = V_{s(\alpha)} + jV_{s(\beta)} \quad (3.6)$$

Where $V_{s(\alpha)}$ is the summation of all components of $V_{A2A3}$, $V_{B2B3}$ and $V_{C2C3}$ in the direction of α-axis and $V_{s(\beta)}$ is the addition of all the components of $V_{B2B3}$ and $V_{C2C3}$ along the β-axis.

$$V_{s(\alpha)} = V_{A2A3(\alpha)} + V_{B2B3(\alpha)} + V_{C2C3(\alpha)} \quad (3.7)$$

$$V_{s(\beta)} = V_{B2B3(\beta)} + V_{C2C3(\beta)} \quad (3.8)$$

$$\begin{bmatrix} V_{s(\alpha)} \\ V_{s(\beta)} \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{A2A3} \\ V_{B2B3} \\ V_{C2C3} \end{bmatrix} \quad (3.9)$$

Substituting the values of phase voltages from equations (3.1)-(3.3) in equation (3.9), the α-β axis voltages can be expressed as:

$$\begin{bmatrix} V_{s(\alpha)} \\ V_{s(\beta)} \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{A2O} - V_{A3O'} \\ V_{B2O} - V_{B3O'} \\ V_{C2O} - V_{C3O'} \end{bmatrix} \quad (3.10)$$

Depending upon the switching state phase voltages can be easily found and once the phase voltages are known $V_s$ can be calculated using equation (3.6) and equation (3.10). 3-level inverter-A can generate 64 switching state as it is having two, two-level inverter in cascade combination and each two-level inverter can generate eight switching states hence total of 64 (8x8) different combination of space vectors. Two-level inverter-B can generate eight switching states. Collectively inverter-A and inverter-B will generate total of 512 (64x8) space vectors distributed over 61 locations as shown in Fig. 3.3. The switching states 0,1,2,3 and 4 correspond to phase voltage levels of $-V_{DC}/4$, 0, $+V_{DC}/4$, $+V_{DC}/2$ and $+3V_{DC}/4$. The redundant switching states are not shown in the figure for simplicity. There are four co-centric hexagons forming four layers of operating region. If the reference space vector $V_s$ exist within the first layer, which is the region inside the innermost hexagon the inverter operates in two-level mode. If the reference vector is in between first and second hexagon, i.e. in layer-two the operation is shifted from two-level to 3-level. Similarly, when the

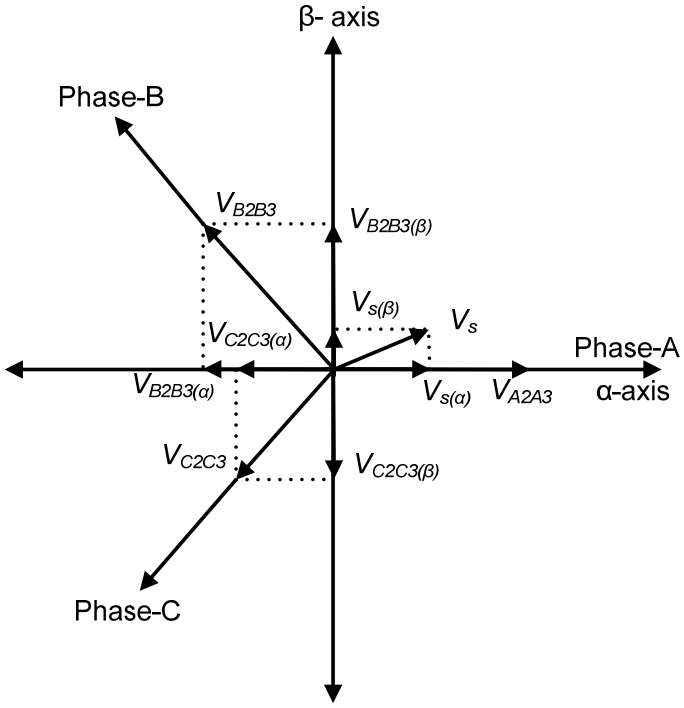



Fig. 3.2: Equivalent voltage space vector $V_s$ in *α-β* plane

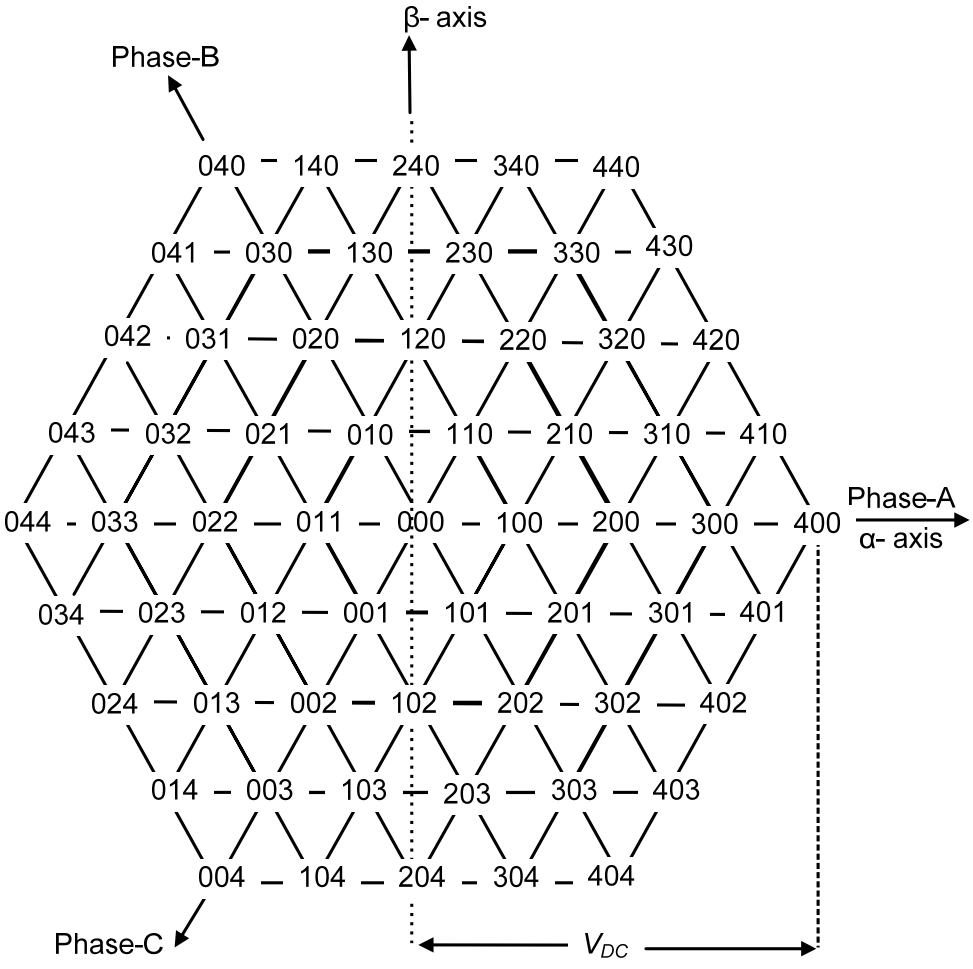



Fig. 3.3: Voltage space vectors distribution for 5-level inverter

reference vector is in layer-three mode of operation is 4-level and finally, when reference vector is in layer-four the operation reaches to its maximum level that is the 5-level mode of operation. In the above discussion it is assumed that the points O and O′ are connected, but in actual they are not connected hence common-mode voltage will exist between these two points. The effect of this voltage is only generation of multiplicity of space vectors in different locations, and the system with unconnected points O and O′ will generates the same voltage space vectors as generated by $V_s$ [74].

### 3.2.4 Selection of DC Link Voltage Ratio

The effective number of voltage levels in open-end winding induction motor configuration depends on the ratio of the DC link voltages of individual inverters. The maximum number of voltage levels achievable is the product of the voltage levels of the individual inverters [183]. To obtain the maximum number of effective voltage levels, the DC voltage ratio must be set as:

$$\frac{V_{DC2}}{V_{DC1}} = \frac{n_2 - 1}{n_2(n_1 - 1)} \tag{3.11}$$

Where $V_{DC1}$ is the DC link voltage of first inverter, which is having $n_1$ number of voltage levels and $V_{DC2}$ is the DC link voltage of second inverter having $n_2$ number of voltage levels.

The 5-level configuration shown in Fig. 3.1 can produce six different voltage levels by making proper selection of DC link voltages of 3-level inverter-A and two-level inverter-B. Taking $n_1$ =3 and $n_2$ =2 the ratio of DC link voltage of 3-level inverter-A to two-level inverter-B comes out to be 4 and if $V_{DC}$ is the equivalent DC link voltage, then DC link voltages of 3-level inverter-A and two-level inverter-B will be $4V_{DC}/5$ and $V_{DC}/5$ respectively. The modified power circuit to achieve 6-level inversion operation is shown in Fig. 3.4. The power circuit remains same as the power circuit of 5-level inverter the change is only in the DC link voltages of all two-level inverters. The 3-level inverter pole voltages $V_{A2O}$, $V_{B2O}$ or $V_{C2O}$ can have three levels 0, $2V_{DC}/5$ and $4V_{DC}/5$ independently. The two-level inverter-B pole voltages with respect to its own reference point O′ are denoted as $V_{A3O'}$, $V_{B3O'}$ and $V_{C3O'}$. These pole voltages can have two levels 0 and $V_{DC}/5$ independently. The combined effect of these two inverters generates six levels as $-V_{DC}/5$, 0, $+V_{DC}/5$, $+2V_{DC}/5$, $+3V_{DC}/5$ and $+4V_{DC}/5$. Switching states of corresponding switches of all two-level inverters to realize six levels across the phase-A winding of open-end induction motor are shown in Table 3.3. Similar logic can also be implemented for others phases. Switches correspond to same leg of any two-level inverter operate in complementary fashion.

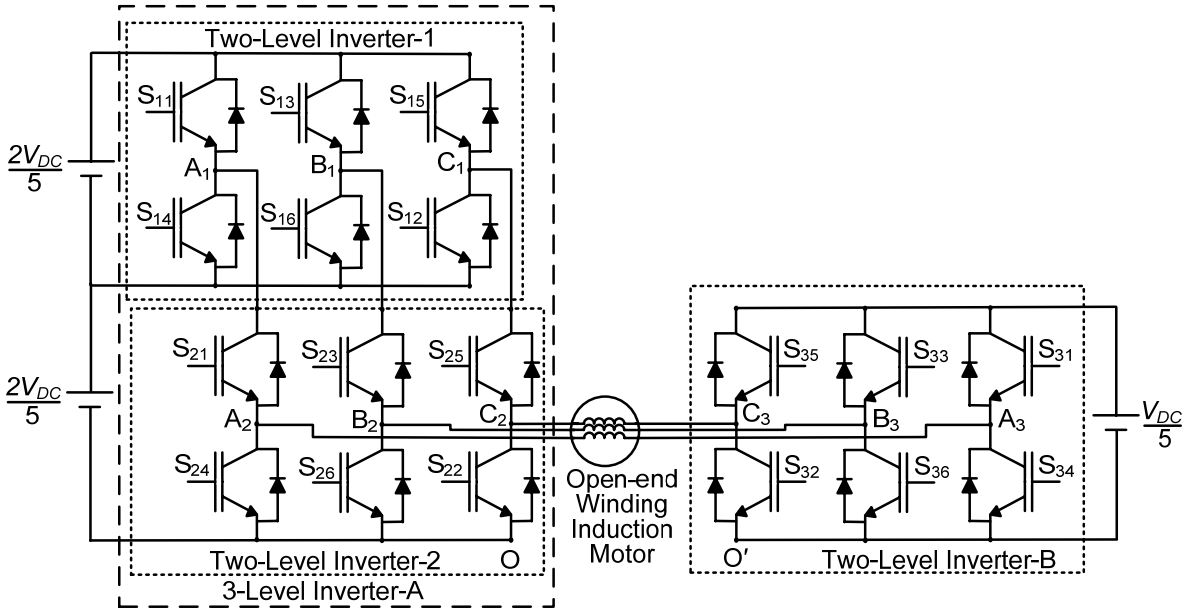



Fig. 3.4: Power circuit of 6-level inverter scheme for open-end winding induction motor drive

Table 3.3: Switching states of phase-A related switches of all two-level inverters for 6-level operation

| Level | Motor phase-A voltage level | Switch (state) Inverter-1 | Switch (state) Inverter-2 | Switch (state) Inverter-B |
|---|---|---|---|---|
| $L_1$ | $-V_{DC}/5$ | $S_{14}$ (ON) | $S_{24}$ (ON) | $S_{31}$ (ON) |
| $L_2$ | 0 | $S_{14}$ (ON) | $S_{24}$ (ON) | $S_{34}$ (ON) |
| $L_3$ | $+V_{DC}/5$ | $S_{14}$ (ON) | $S_{21}$ (ON) | $S_{31}$ (ON) |
| $L_4$ | $+2V_{DC}/5$ | $S_{14}$ (ON) | $S_{21}$ (ON) | $S_{34}$ (ON) |
| $L_5$ | $+3V_{DC}/5$ | $S_{11}$ (ON) | $S_{21}$ (ON) | $S_{31}$ (ON) |
| $L_6$ | $+4V_{DC}/5$ | $S_{11}$ (ON) | $S_{21}$ (ON) | $S_{34}$ (ON) |

### 3.3 Control Scheme

The level shifted carrier based space vector pulse width modulation (SVPWM) technique describe in Chapter-2, for D2L inverter is extended to 5-level inverter. The entire range of operation is divided into five regions by four level-shifted triangular carrier waves (C1, C2, C3, C4) as shown in Fig. 3.5. The region below the first triangular carrier C1 is define as level $L_1$, region between C1 and C2 is level $L_2$, region between C2 and C3 is level $L_3$, region between C3 and C4 is level $L_4$ and region above triangular carrier C4 is level $L_5$. Three modulating signals are simultaneously compared with all triangular carrier signals (C1, C2, C3, C4) in each sample period and depending upon their instantaneous position switching signals are generated according to Table 3.2. In Fig. 3.5 only phase–A modulating procedure is shown for simplicity for other phases switching signals are generated in similar fashion. The switches of same leg operate in complementary fashion. The open-end winding

IM drive is operated in constant *V/f* control mode at no-load. The magnitude of reference voltage space vector ($V^*_s$) is determined by constant *V/f* ratio and modulation index. The three reference waves ($V^*_a$, $V^*_b$ $V^*_c$) correspond to phase-A, B and C are determined by transferring the orthogonal components of reference voltage vector ($V^*_s$) into the three phase quantity as described in subsection 3.2.3. An offset as given by equation (3.12) is added to these reference voltages to generate three modulating signals which give the performance equivalent to conventional SVPWM. The three modulating signals correspond to three phases are given by equation (3.13).

$$V_{offset} = -[\max(V^*_a, V^*_b, V^*_c) + \min(V^*_a, V^*_b, V^*_c)]/2 \tag{3.12}$$

$$\left.\begin{aligned} V^*_{A2A3} &= V^*_a + V_{offset} \\ V^*_{B2B3} &= V^*_b + V_{offset} \\ V^*_{C2C3} &= V^*_c + V_{offset} \end{aligned}\right\} \tag{3.13}$$

The modulation index (*m*) is define as the ratio of the magnitude of the actual reference voltage space phasor ($|V^*_s|$) to the maximum magnitude of the voltage space phasor ($V_{DC}$) as $m = |V^*_s| / V_{DC}$ . The limit of modulation index (*m*) for linear modulation is 0.866.

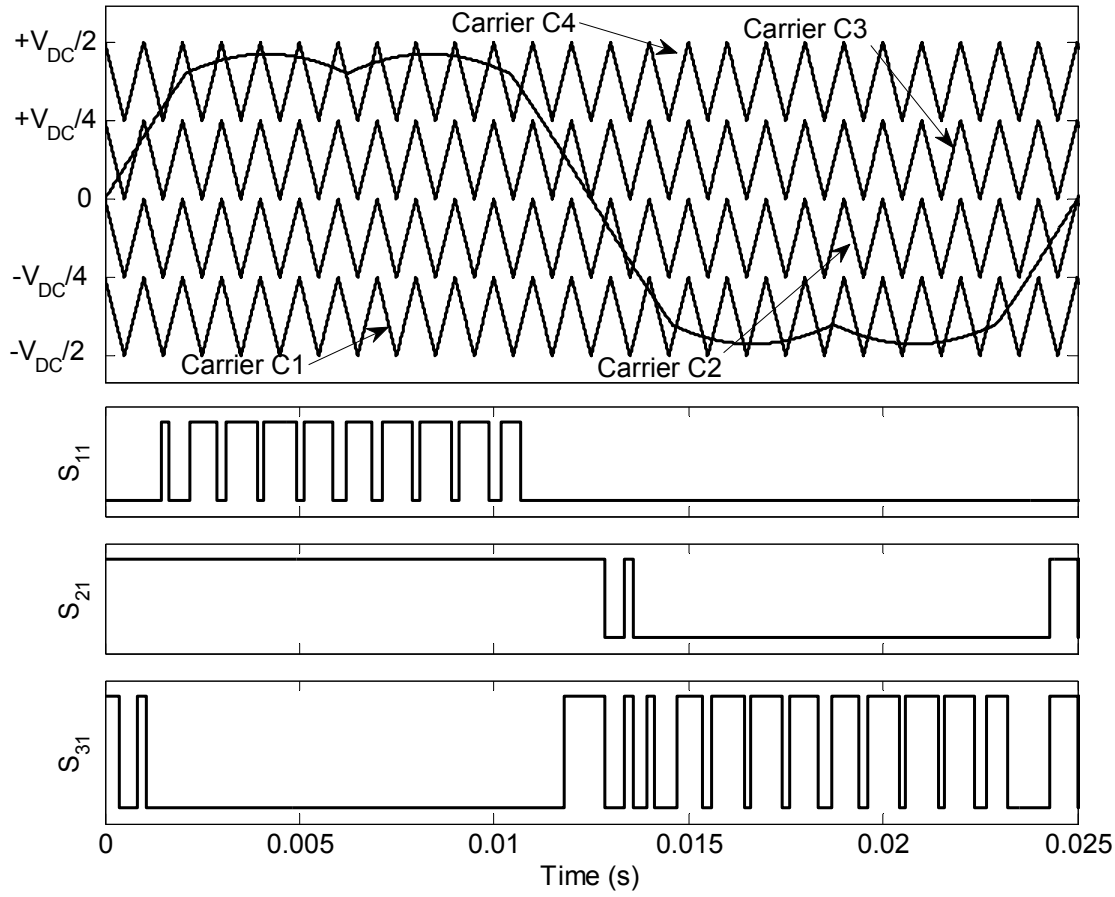



Fig. 3.5: Switching signals for the devices of phase–A of 5-level inverter using LSPWM technique

### 3.4 Mathematical Modelling of 5-level Inverter Scheme

A switching function based mathematical model developed in Chapter-2 for D2L inverter scheme, is modified to get the expression for output voltage of 5-level inverter scheme. The pole voltages of 3-level inverter-A can be expressed as:

$$\left.\begin{aligned} V_{A2O} &= \frac{V_{DC}}{4} SF_a \\ V_{B2O} &= \frac{V_{DC}}{4} SF_b \\ V_{C2O} &= \frac{V_{DC}}{4} SF_c \end{aligned}\right\} \tag{3.14}$$

The switching function $SF_X$ (X=a, b, c) can take three values 0, 2 and 3 depending upon the condition as described in equations (3.15) - (3.17)

$$SF_a = \begin{cases} 0 & \text{when } S_{14} = 1 \text{ and } S_{24} = 1 \\ 2 & \text{when } S_{14} = 1 \text{ and } S_{21} = 1 \\ 3 & \text{when } S_{11} = 1 \text{ and } S_{21} = 1 \end{cases} \tag{3.15}$$

$$SF_b = \begin{cases} 0 & \text{when } S_{16} = 1 \text{ and } S_{26} = 1 \\ 2 & \text{when } S_{16} = 1 \text{ and } S_{23} = 1 \\ 3 & \text{when } S_{13} = 1 \text{ and } S_{23} = 1 \end{cases} \tag{3.16}$$

$$SF_c = \begin{cases} 0 & \text{when } S_{12} = 1 \text{ and } S_{22} = 1 \\ 2 & \text{when } S_{12} = 1 \text{ and } S_{25} = 1 \\ 3 & \text{when } S_{15} = 1 \text{ and } S_{25} = 1 \end{cases} \tag{3.17}$$

Similarly, two-level inverter-B pole voltages ($V_{A3O'}$, $V_{B3O'}$, $V_{C3O'}$) with respect to point-O' in terms of DC link voltages and switching functions are given by

$$\left.\begin{aligned} V_{A3O'} &= \frac{V_{DC}}{4} SF_{a'} \\ V_{B3O'} &= \frac{V_{DC}}{4} SF_{b'} \\ V_{C3O'} &= \frac{V_{DC}}{4} SF_{c'} \end{aligned}\right\} \tag{3.18}$$

The switching function $SF_{X'}$ (X=a, b, c) can take two discreet values either 0 or 1 depending upon the condition as described below:

$$SF_{a'} = \begin{cases} 0 & \text{when } S_{34} = 1 \\ 1 & \text{when } S_{31} = 1 \end{cases} \tag{3.19}$$

$$SF_{b'} = \begin{cases} 0 & \text{when } S_{36} = 1 \\ 1 & \text{when } S_{33} = 1 \end{cases} \tag{3.20}$$

$$SF_{c'} = \begin{cases} 0 & \text{when } S_{32} = 1 \\ 1 & \text{when } S_{35} = 1 \end{cases} \tag{3.21}$$

The three-phase motor voltages can be derived in terms of pole voltages as described in Chapter-2

$$\begin{bmatrix} V_{A2A3} \\ V_{B2B3} \\ V_{C2C3} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} V_{A2O} - V_{A3O'} \\ V_{B2O} - V_{B3O'} \\ V_{C2O} - V_{C3O'} \end{bmatrix} \tag{3.22}$$

After putting the values of pole voltages in terms of switching functions from equations (3.14) and (3.18) the motor phase voltages can be expressed as

$$\begin{bmatrix} V_{A2A3} \\ V_{B2B3} \\ V_{C2C3} \end{bmatrix} = \frac{V_{DC}}{12}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} SF_a - SF_{a'} \\ SF_b - SF_{b'} \\ SF_c - SF_{c'} \end{bmatrix} \tag{3.23}$$

The combined effect of three-phase voltages $V_{A2A3}$, $V_{B2B3}$ and $V_{C2C3}$ on motor phase winding, at any instant will be given by $V_s$ as

$$V_s = V_{A2A3} + V_{B2B3}.e^{j(2\pi/3)} + V_{C2C3}.e^{j(4\pi/3)} \tag{3.24}$$

The d-q component of space vector $V_s$ in terms of phase voltages can be expressed as

$$\begin{bmatrix} V_{qs} \\ V_{ds} \\ V_{os} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/2 & 1/2 & 1/2 \end{bmatrix}\begin{bmatrix} V_{A2A3} \\ V_{B2B3} \\ V_{C2C3} \end{bmatrix} \tag{3.25}$$

### 3.5 Simulation Results and Discussion

MATLAB/Simulink based simulation study is carried out in fixed-point simulation mode at a sampling time of 10 μSec to evaluate the performance of 5-level inverter scheme for open-end induction motor drive. The mathematical model of open-end winding induction motor describe in subsection 2.4.2 is developed in MATLAB/Simulink environment using S-function concept. The induction motor is operated in constant *V/f* mode under no-load condition covering the entire range of linear modulation. The switching frequency ($f_c$) is kept constant at 1kHz and DC link voltage is taken as 600V for simulation analysis. The motor phase-A voltage ($V_{A2A3}$), phase-A current ($i_{A2A3}$), their harmonic spectrum, inverters pole-A voltages ($V_{A2O}$, $V_{A3O'}$) and difference of inverters pole-A voltages ($V_{A2O}$ - $V_{A3O'}$) are considered as evaluation criteria. To cover the entire range of linear modulation four values of modulation indices ($m$) 0.2, 0.4, 0.6 and 0.8 correspond to frequencies ($f^*_m$) of 10, 20, 30, and 40Hz respectively are selected. The performance of 5-level inverter scheme is evaluated under steady-state as well as transient-state conditions and results are presented in Fig. 3.6 - Fig. 3.22.

The motor phase-A voltage ($V_{A2A3}$) and current ($i_{A2A3}$) at modulation index $m$ =0.2 are shown in Fig. 3.6. At this modulation index motor operates at fundamental frequency ($f^*_m$) of 10Hz. The phase-A voltage ($V_{A2A3}$) and current ($i_{A2A3}$) waveforms are equivalent to conventional two-level inverter. The harmonic spectrum of phase-A voltage and current with

respect to their fundamental component for the modulation index $m$ =0.2 are shown in Fig. 3.7 and Fig. 3.8 respectively. These spectra show that the dominant harmonic component of phase voltage and current occur at the multiple of 100 ($f_c/f^*_m$ = 1000/10) i.e. near 100$^{th}$ and 200$^{th}$ order. Lower order harmonics responsible for higher losses are significantly low. The pole voltages and difference in pole voltages of 3-level inverter-A and two-level inverter-B are shown in Fig. 3.9. It can be noted from pole voltages waveform that 3-level inverter-A operates in two-level mode (0 and $V_{DC}$/2) only for half of the duration of fundamental cycle and for remaining half cycle it is clamped at voltage level of $V_{DC}$/2 so effective switching frequency is half of the actual switching frequency. This feature can lead to use of low switching frequency rating power semiconductor devices in the proposed 5-level inverter scheme. The two-level inverter-B operates in PWM mode throughout the cycle, but since its DC link voltage is only $V_{DC}$/4 hence switching losses are less.

Similar type of waveforms for motor phase-A voltage ($V_{A2A3}$), phase-A current ($i_{A2A3}$), their harmonic spectrums, inverters pole-A voltages ($V_{A2O}$, $V_{A3O'}$) and difference of inverters pole-A voltages ($V_{A2O}$ - $V_{A3O'}$) at modulation index $m$ =0.4 are shown in from Fig. 3.10 to Fig. 3.13. At this modulation index motor operates at fundamental frequency ($f^*_m$) of 20Hz.

The performance of the motor at modulation index $m$ =0.6 is depicted in from Fig. 3.14 to Fig. 3.17. It can be observed from harmonic spectrum of phase voltage shown in Fig. 3.15 for $m$ =0.6 that THD is reduced to 9.55% and dominant harmonic component occur at side band of 67$^{th}$ ($2f_c/f^*_m$ = 2*1000/30) order harmonic. The distortion in phase current is only 1.58% as shown in Fig. 3.16. The pole-A voltages and difference in pole voltages of 3-level inverter-A and two-level inverter-B are shown in Fig. 3.17. It can be noted from pole voltages waveform that 3-level inverter-A operates in 3-level mode of operation and takes the values 0, $V_{DC}$/2 and 3$V_{DC}$/4 only for half of the duration of fundamental cycle and for remaining half cycle it is clamped at zero voltage so effectively it is operated in PWM mode only for half of the duration of fundamental cycle hence switching losses are reduce. Similarly two-level inverter-B also operates in PWM mode only for half of the duration of fundamental cycle hence switching losses are also reduced in this inverter.

Performance of the motor at modulation index $m$ =0.8 correspond to 40Hz operation is presented in from Fig. 3.18 to Fig. 3.21. At this modulation index the distortion in phase voltage is reduced to 7.85%. However, THD of phase current is increased and reached up to 4.90% due to presence of lower order harmonics.

The proposed drive system is also investigated against transient state stability by sudden change its operation from two-level to 5-level and from 5-level to two-level operation; the results are shown in Fig. 3.22(a) and Fig. 3.22(b) respectively. It can be observed in Fig. 3.22 that changeover from lower to higher or higher to lower level of operation take place instantly and drive achieve its steady state within few cycles.

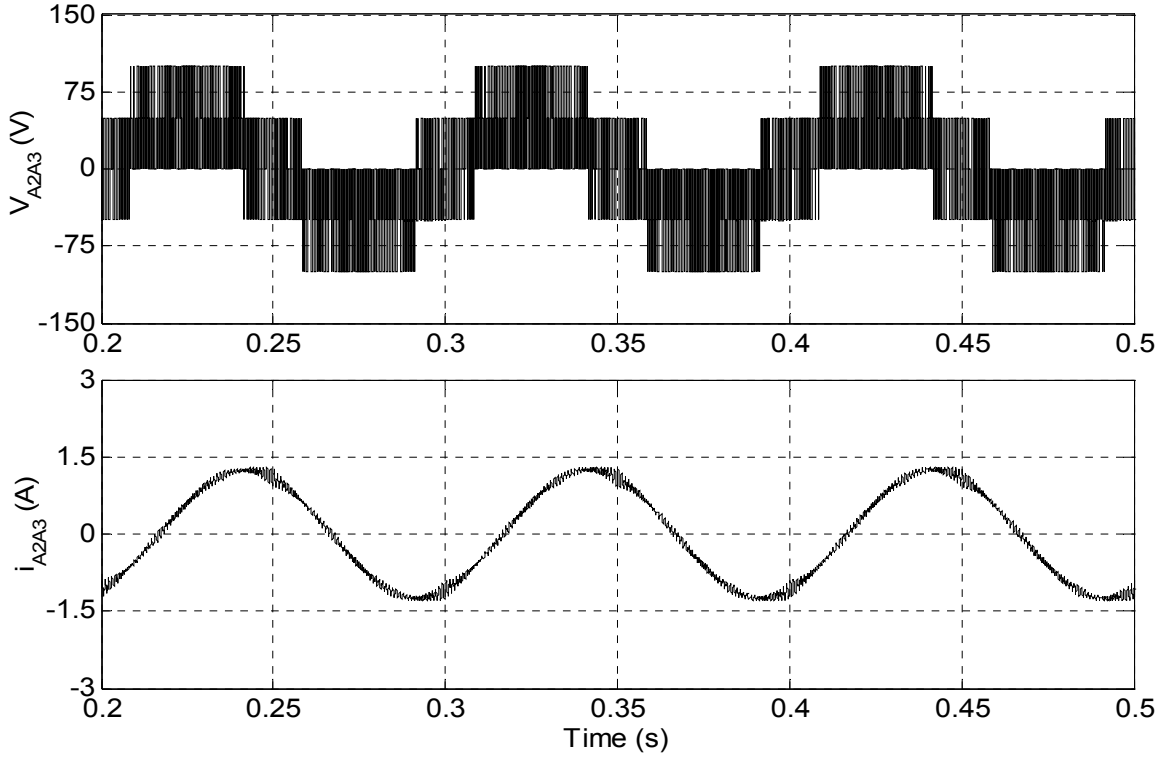



Fig. 3.6: Motor phase-A, voltage $V_{A2A3}$ (upper trace) and current $i_{A2A3}$ (lower trace) of 5-level inverter fed open-end IM drive at no load ($m$=0.2; $f^*_m$ =10Hz)

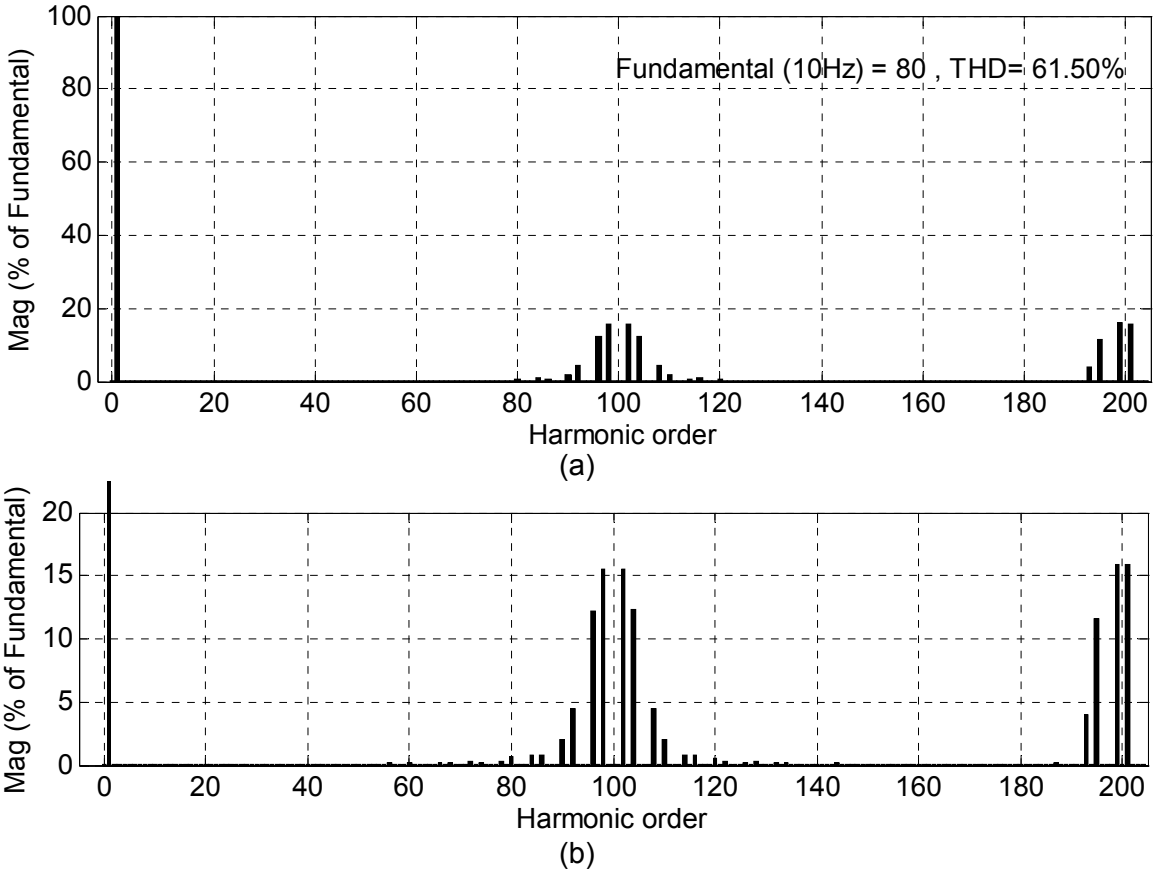



Fig. 3.7: (a) Harmonic spectrum of phase-A voltage ($V_{A2A3}$) at $m$=0.2; $f^*_m$ =10Hz
(b) Zoom view of harmonic spectrum shown in (a)

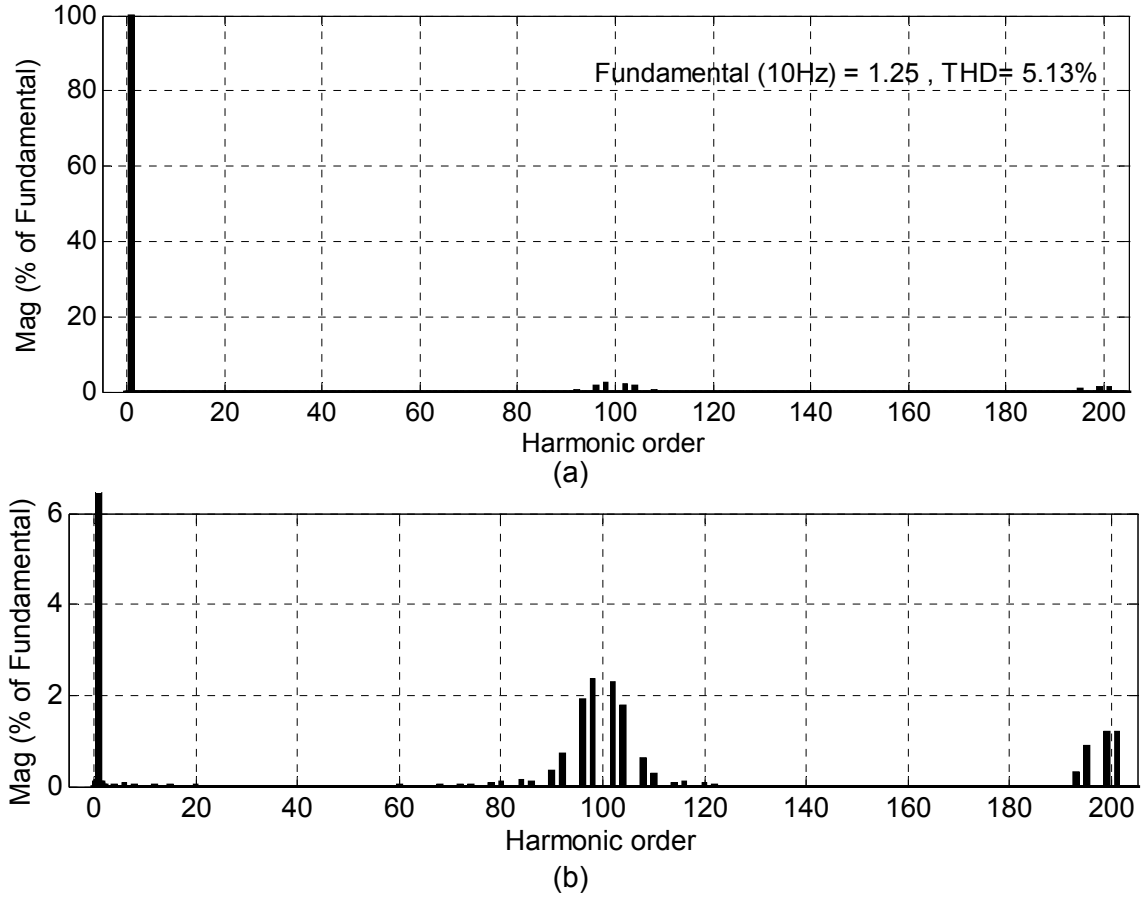



Fig. 3.8: (a) Harmonic spectrum of phase-A current ($i_{A2A3}$) at $m$=0.2; $f^*_m$ =10Hz
(b) Zoom view of harmonic spectrum shown in (a)

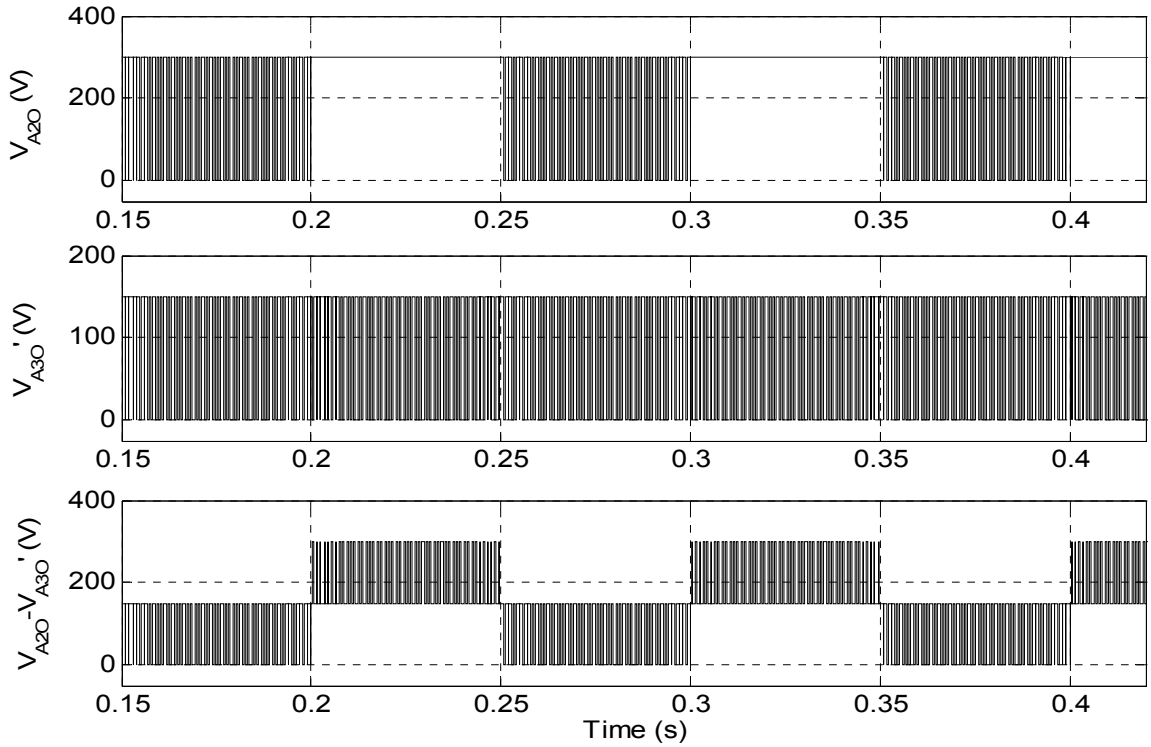



Fig. 3.9: Top trace; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace; Two-level inverter-B pole voltage ($V_{A3O'}$), Bottom trace; Difference of 3-level inverter-A and two-level inverter-B pole voltages ($V_{A2O}$ - $V_{A3O'}$) at $m$=0.2; $f^*_m$ =10Hz

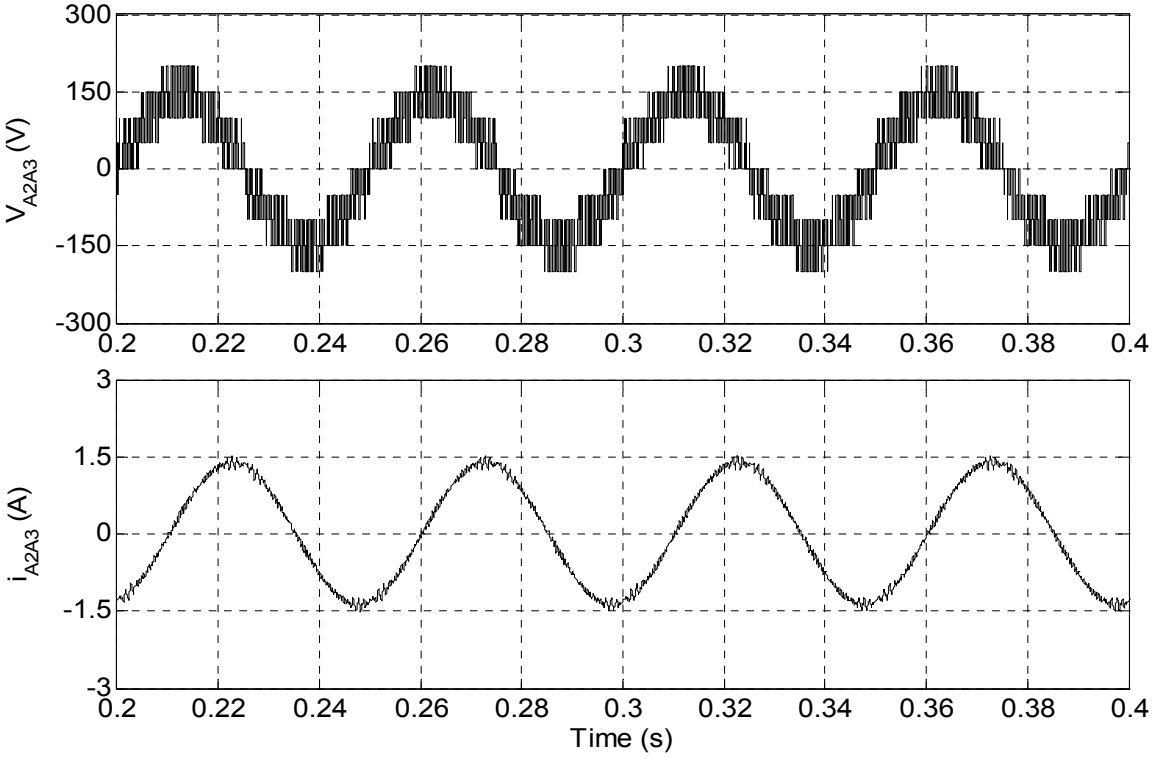



Fig. 3.10: Motor phase-A, voltage $V_{A2A3}$ (upper trace) and current $i_{A2A3}$ (lower trace) of 5-level inverter fed open-end IM drive at no load ($m$=0.4; $f^*_m$ =20Hz)

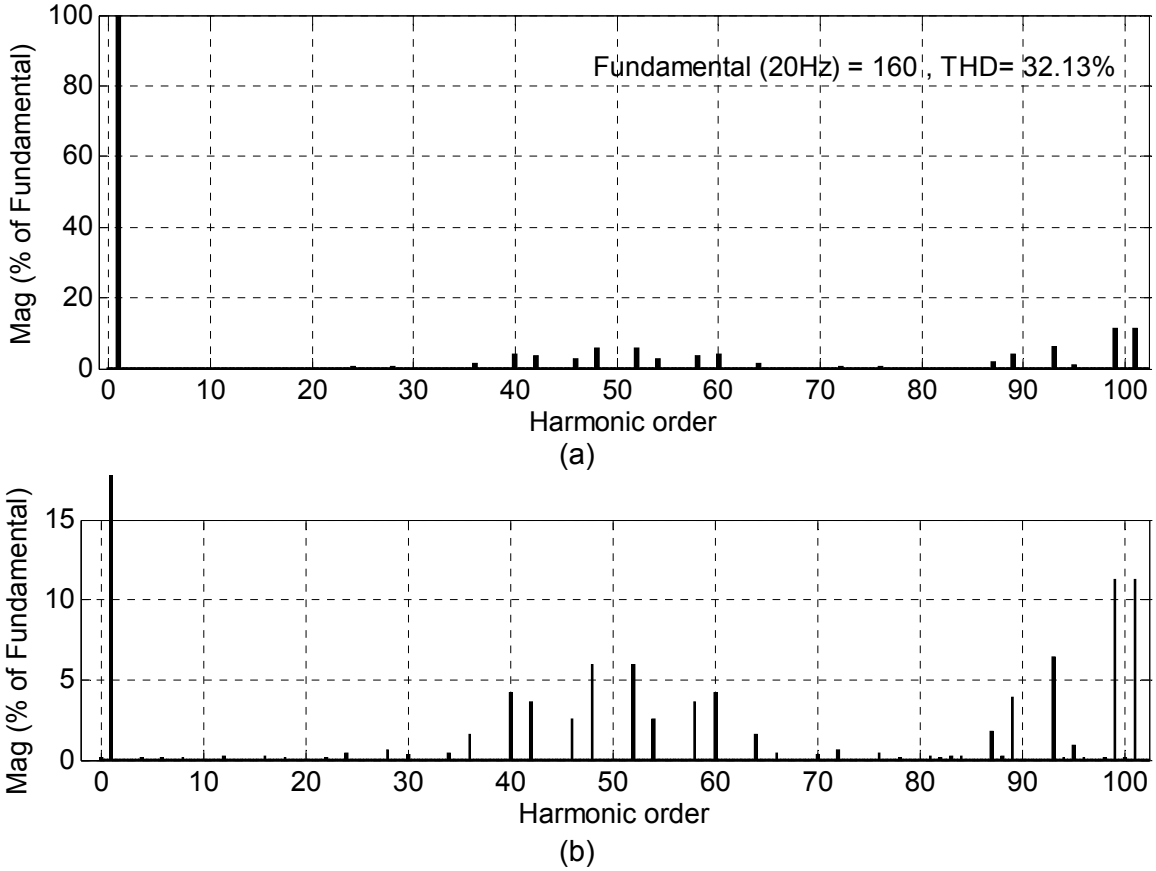



Fig. 3.11: (a) Harmonic spectrum of phase-A voltage ($V_{A2A3}$) at $m$=0.4; $f^*_m$ =20Hz
(b) Zoom view of harmonic spectrum shown in (a)

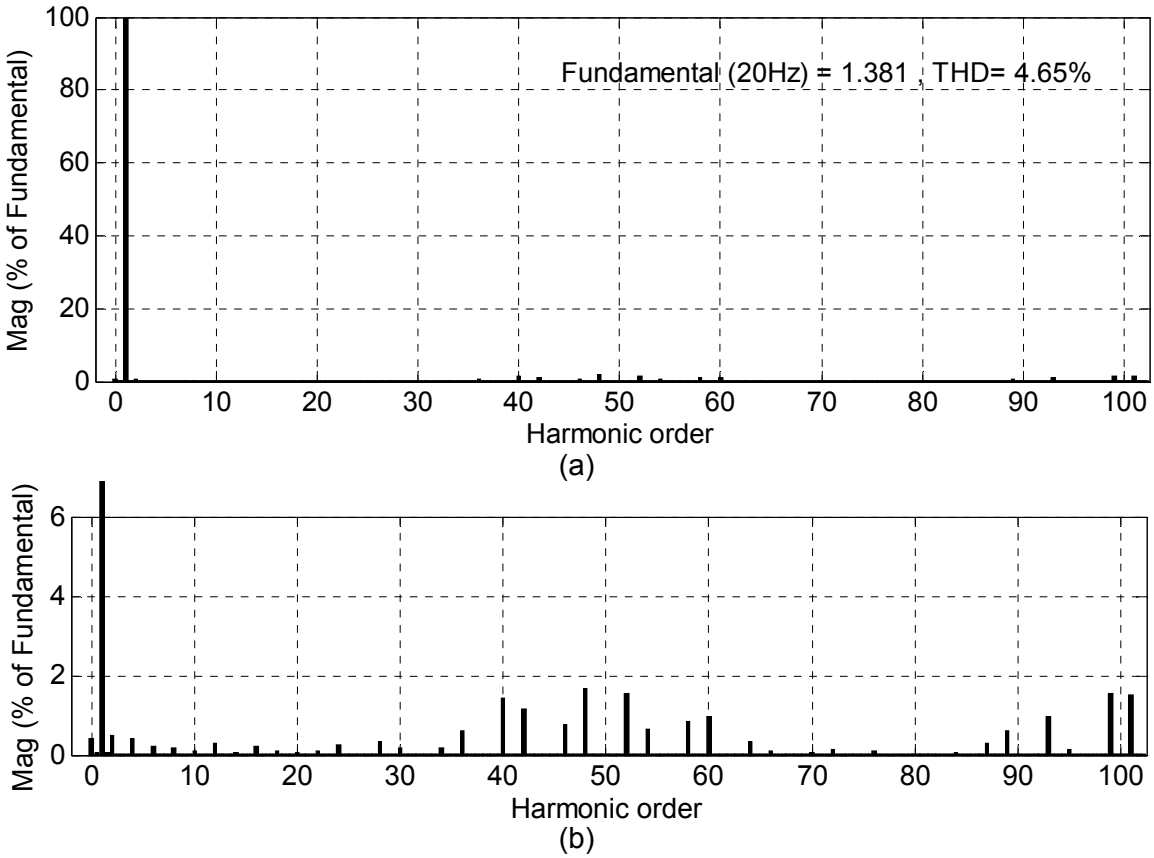



Fig. 3.12: (a) Harmonic spectrum of phase-A current ($i_{A2A3}$) at $m$=0.4; $f^*_m$ =20Hz
(b) Zoom view of harmonic spectrum shown in (a)

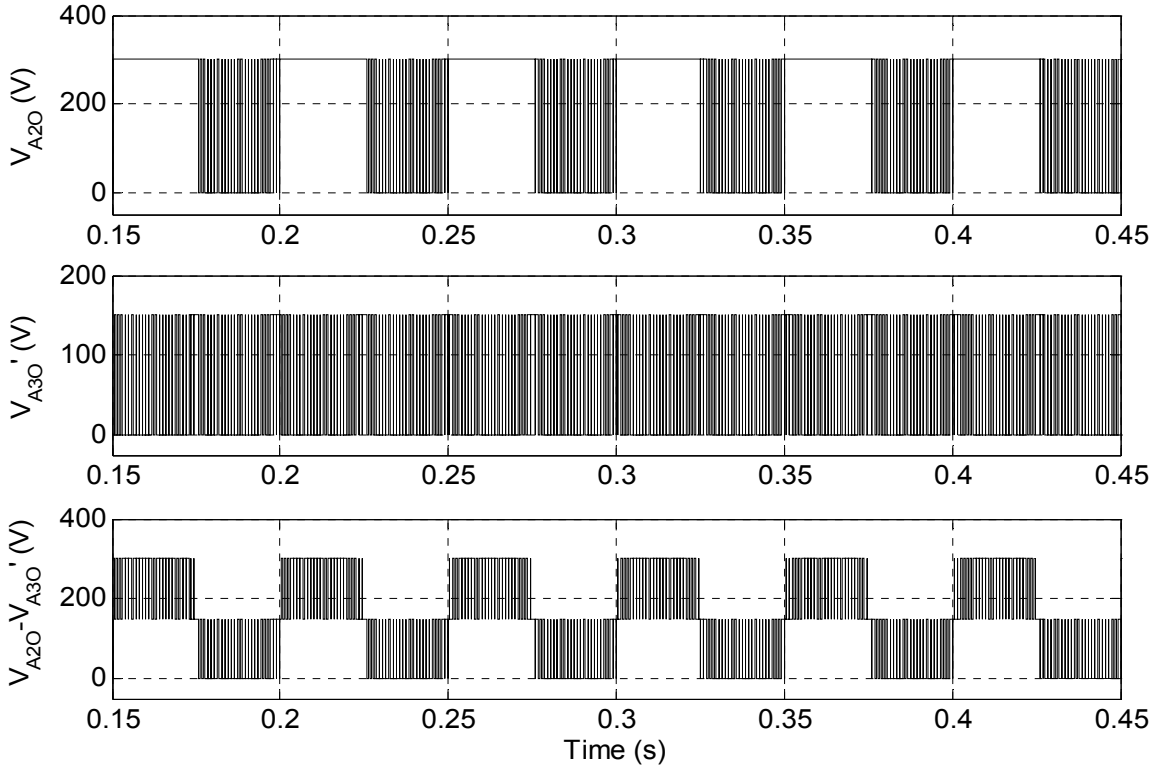



Fig. 3.13: Top trace; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace; Two-level inverter-B pole voltage ($V_{A3O'}$), Bottom trace; Difference of 3-level inverter-A and two-level inverter-B pole voltages ($V_{A2O}$ - $V_{A3O'}$) at $m$=0.4; $f^*_m$ =20Hz

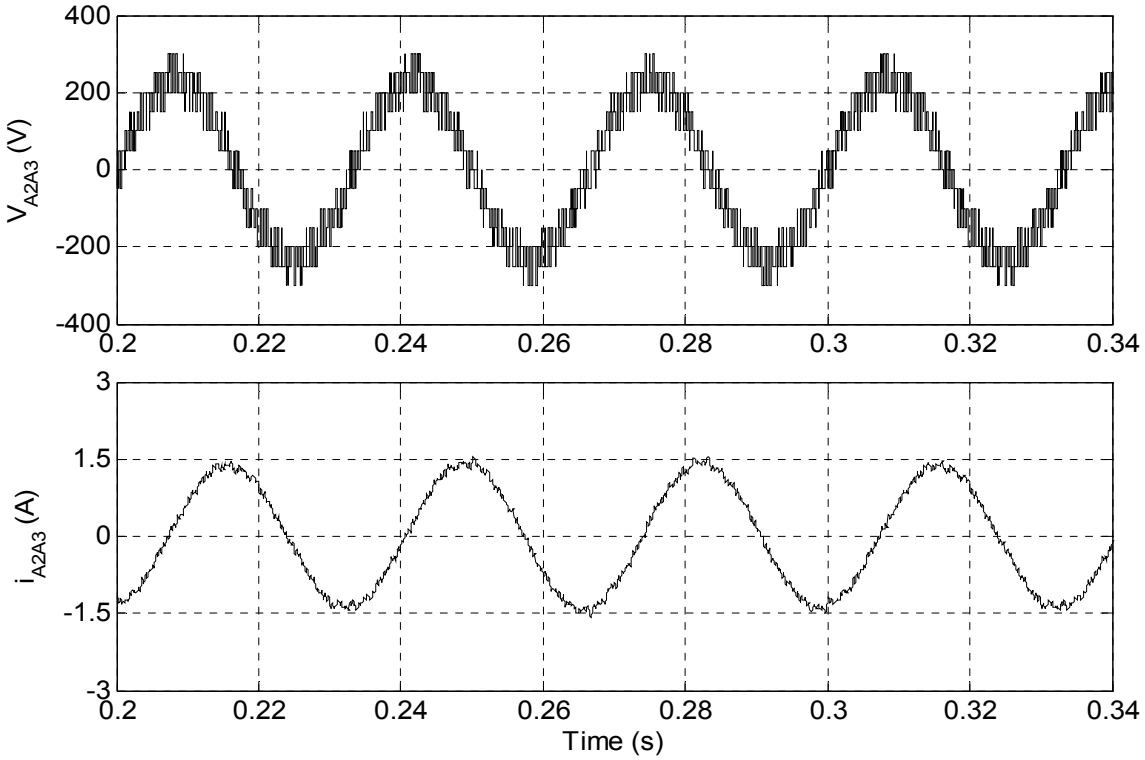



Fig. 3.14: Motor phase-A, voltage $V_{A2A3}$ (upper trace) and current $i_{A2A3}$ (lower trace) of 5-level inverter fed open-end IM drive at no load ($m$=0.6; $f^*_m$ =30Hz)

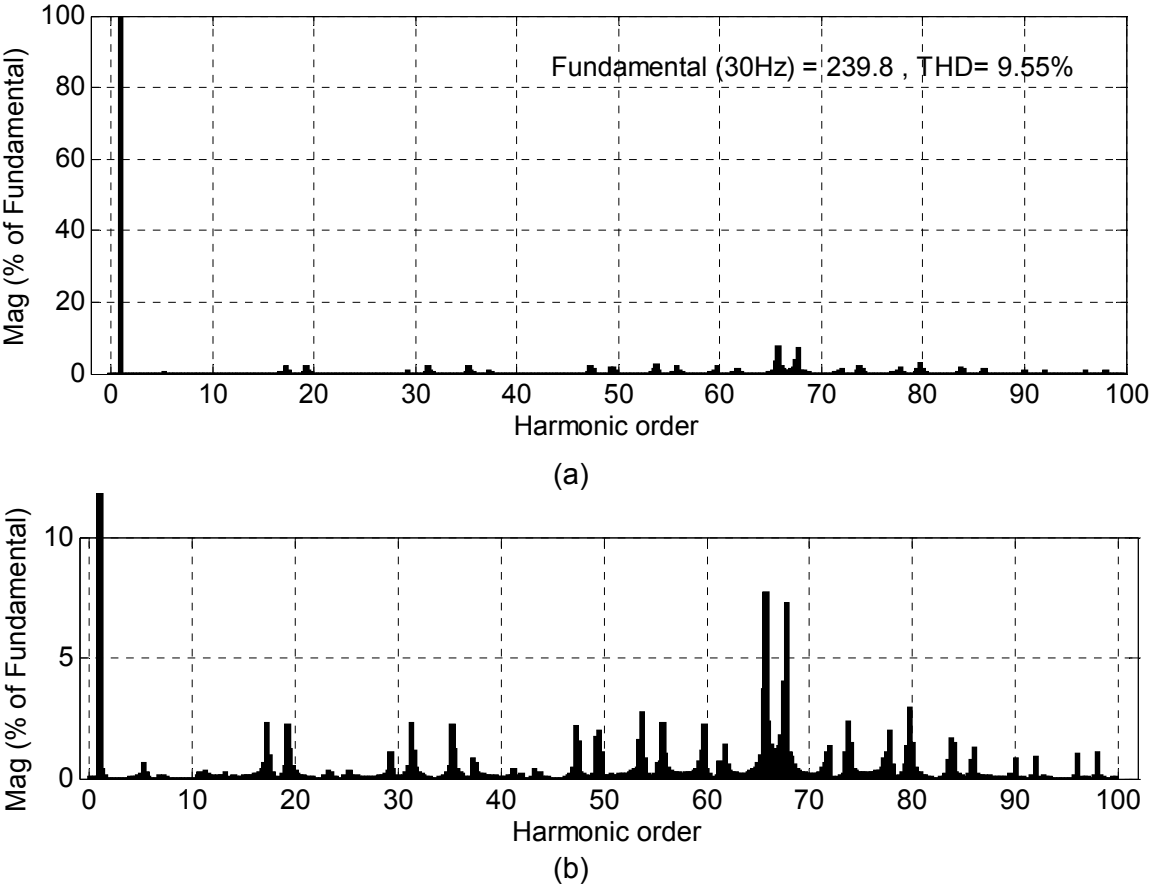



Fig. 3.15: (a) Harmonic spectrum of phase-A voltage ($V_{A2A3}$) at $m$=0.6; $f^*_m$ =30Hz
(b) Zoom view of harmonic spectrum shown in (a)

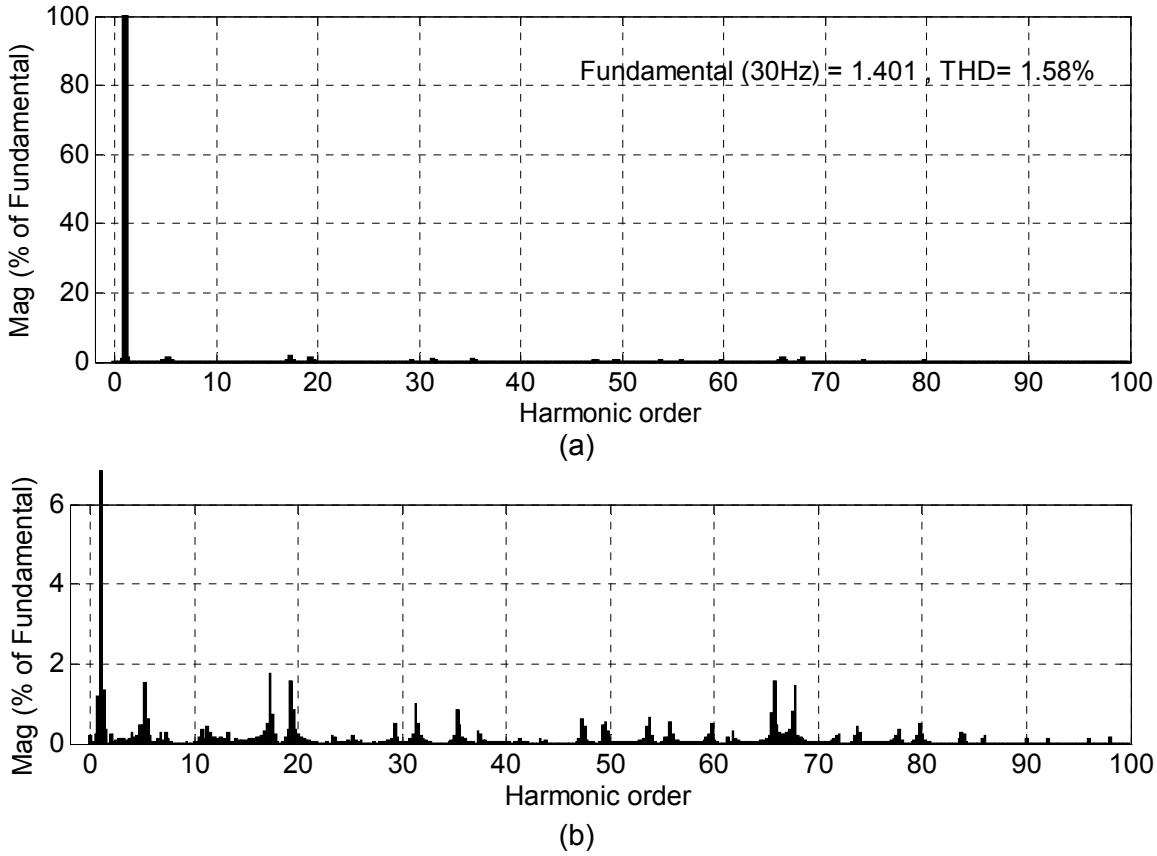



Fig. 3.16: (a) Harmonic spectrum of phase-A current ($i_{A2A3}$) at $m$=0.6; $f^*_m$ =30Hz (b) Zoom view of harmonic spectrum shown in (a)

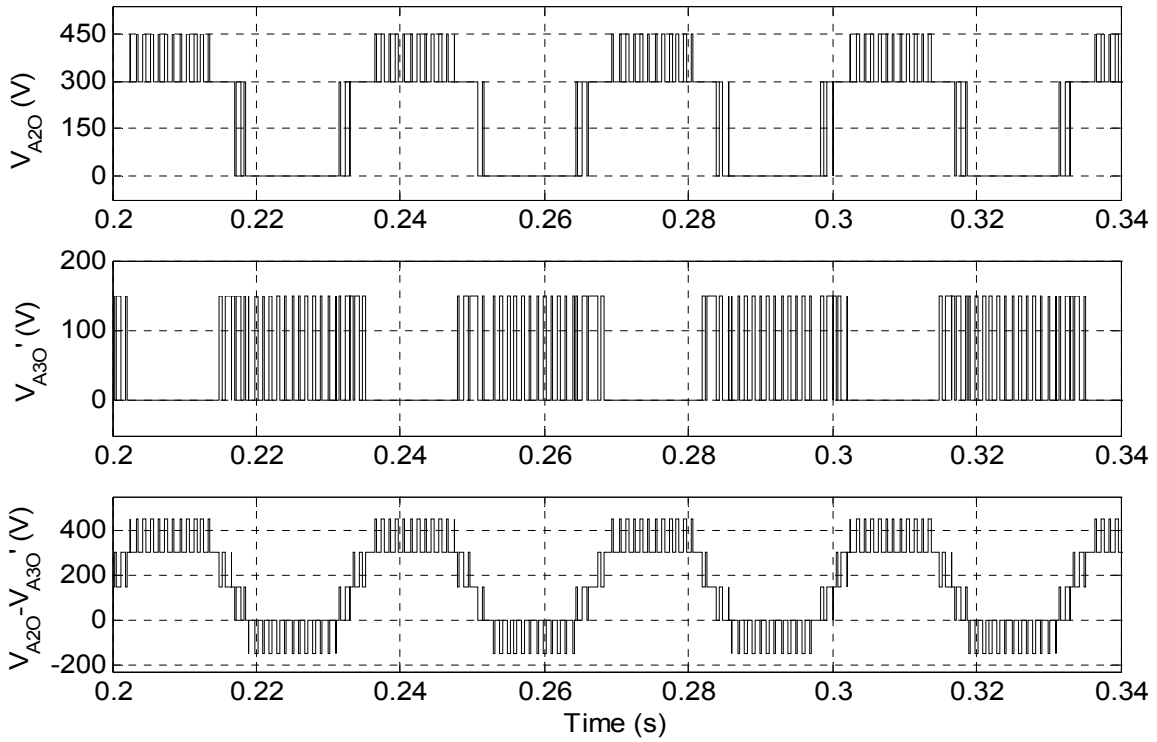



Fig. 3.17: Top trace; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace; Two-level inverter-B pole voltage ($V_{A3O'}$), Bottom trace; Difference of 3-level inverter-A and two-level inverter-B pole voltages ($V_{A2O}$ - $V_{A3O'}$) at $m$=0.6; $f^*_m$ =30Hz

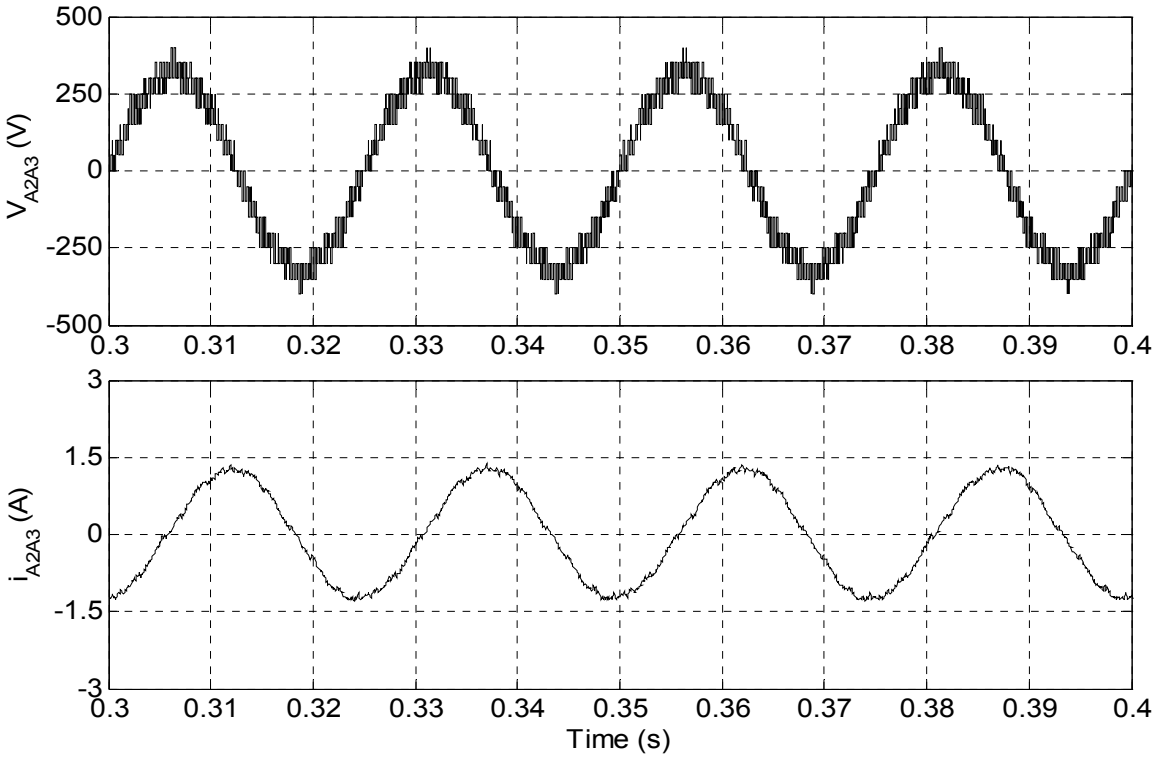



Fig. 3.18: Motor phase-A, voltage $V_{A2A3}$ (upper trace) and current $i_{A2A3}$ (lower trace) of 5-level inverter fed open-end IM drive at no load ($m$=0.8; $f^*_m$ =40Hz)

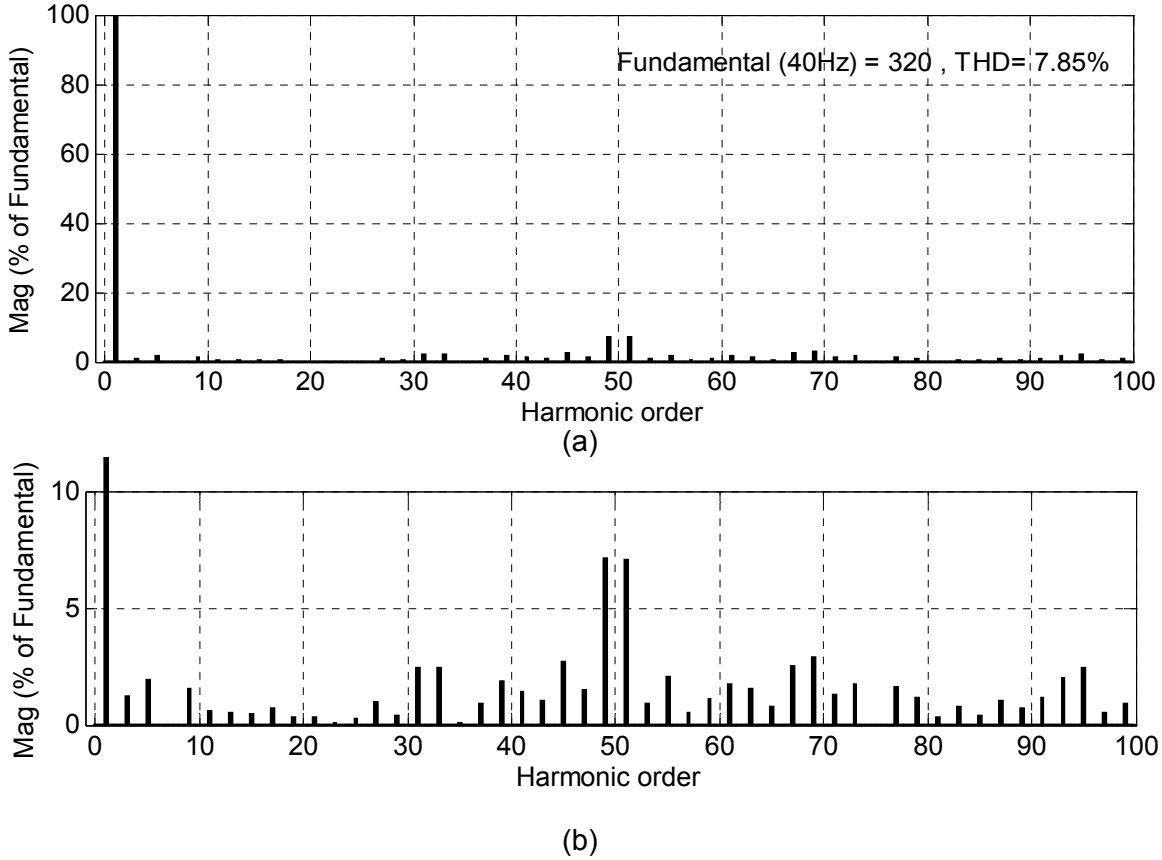



Fig. 3.19: (a) Harmonic spectrum of phase-A voltage ($V_{A2A3}$) at $m$=0.8; $f^*_m$ =40Hz
(b) Zoom view of harmonic spectrum shown in (a)

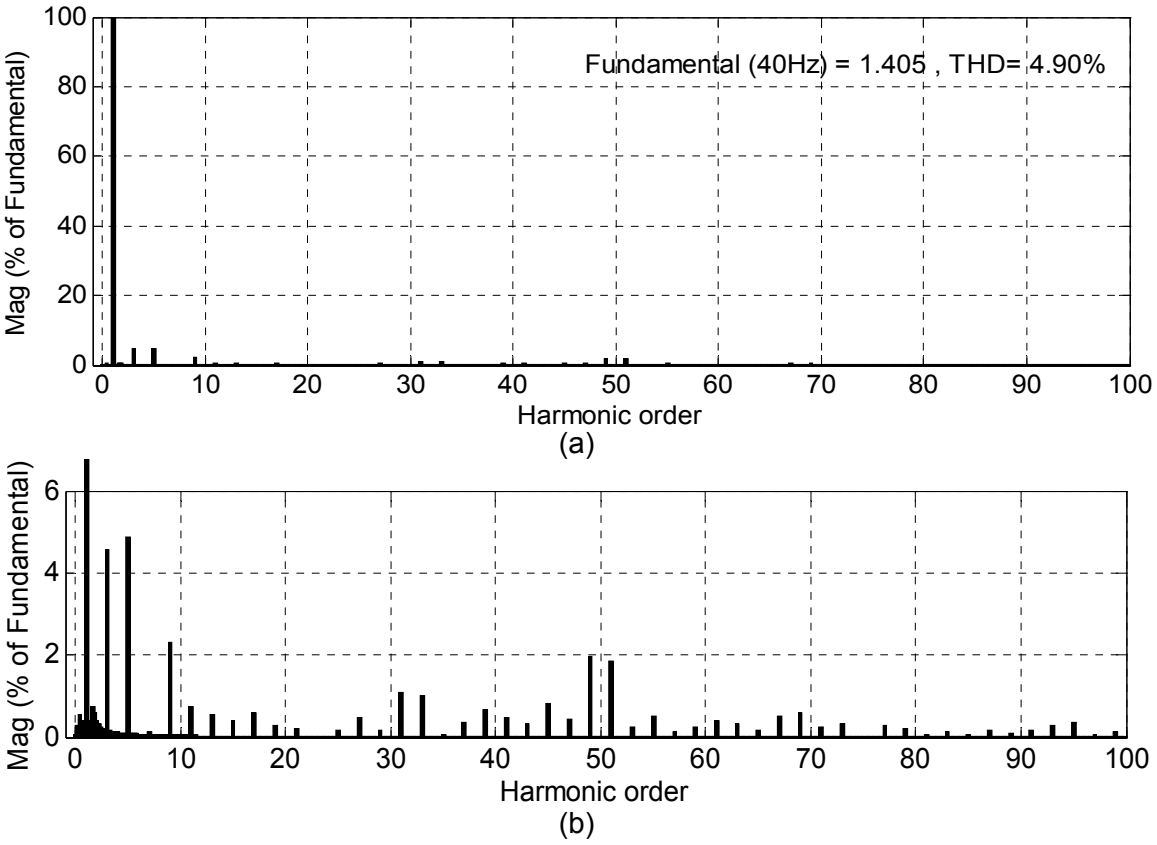



Fig. 3.20: (a) Harmonic spectrum of phase-A current ($i_{A2A3}$) at $m$=0.8; $f^*_m$ =40Hz
(b) Zoom view of harmonic spectrum shown in (a)

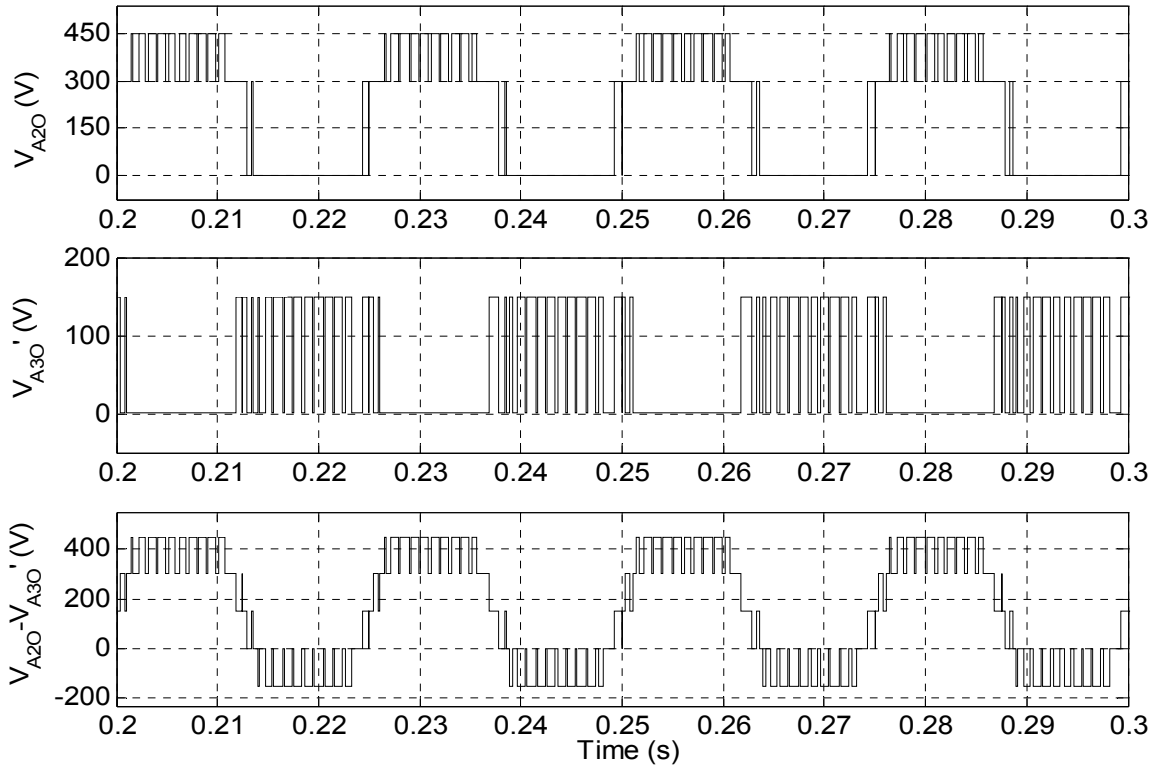
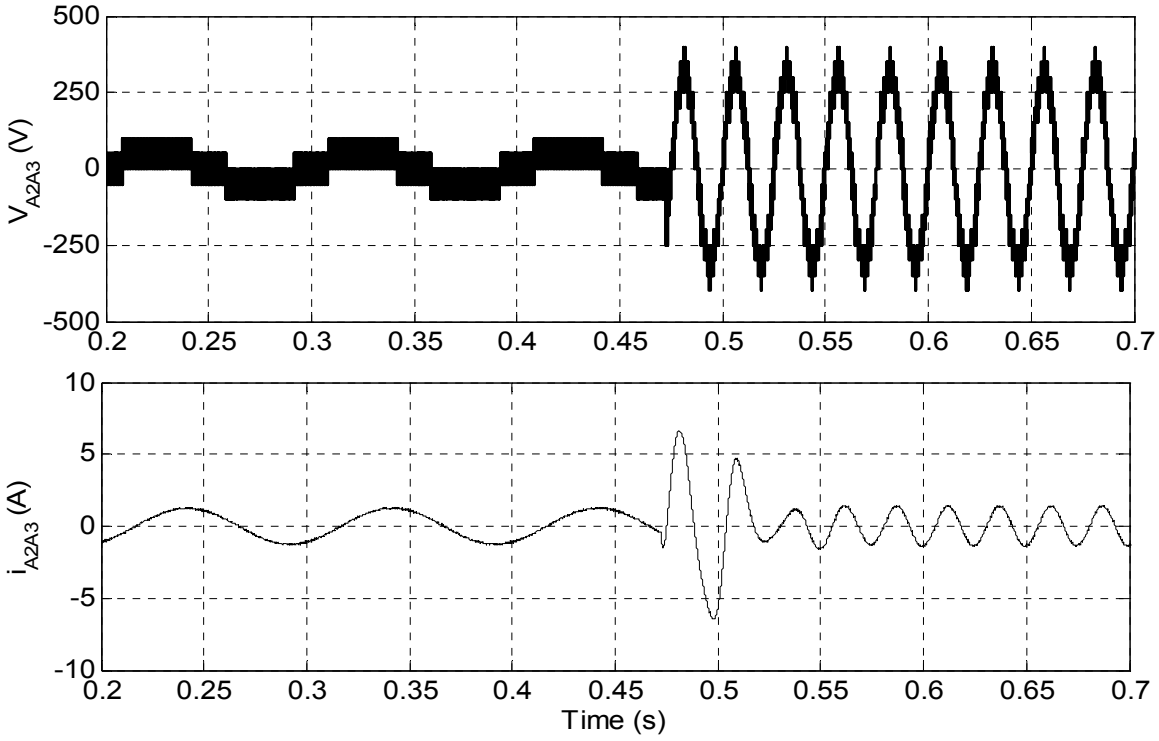
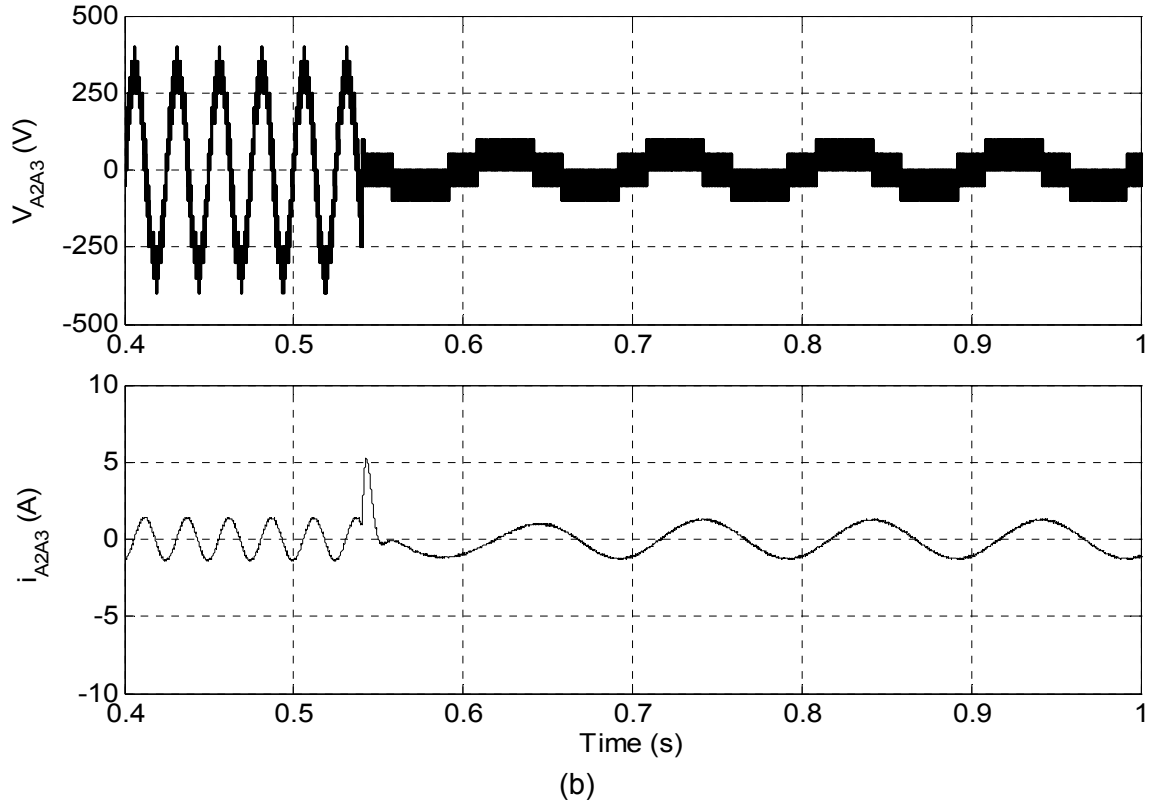



Fig. 3.21: Top trace; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace; Two-level inverter-B pole voltage ($V_{A3O'}$), Bottom trace; Difference of 3-level inverter-A and two-level inverter-B pole voltages ($V_{A2O}$ - $V_{A3O'}$) at $m$=0.8; $f^*_m$ =40Hz




(a)




(b)

Fig. 3.22: (a) Motor phase-A voltage $V_{A2A3}$ (upper trace) and current $i_{A2A3}$ (lower trace) waveforms under sudden change in operation from two-level to 5-level at no-load (b) Motor phase-A voltage $V_{A2A3}$ (upper trace) and current $i_{A2A3}$ (lower trace) waveforms under sudden change in operation from 5-level to two-level at no-load

### 3.6 Performance Comparison

In order to compare the performance of 5-level inverter with dual two-level (D2L) inverter simulation results obtained for different value of modulation index are tabulated in Table 3.4. It can be concluded from Table 3.4 that 5-level inverter gives better voltage and current harmonic spectrums as compared to D2L inverter. The order of dominant harmonic components in the phase voltage and current are the same in both inverters, but magnitude is less in case of 5-level inverter. At lower value of modulation index 5-level inverter operates in 3-level mode and for higher modulation index it operates in 5-level mode whereas D2L inverter operates in 3-level mode during the complete range of operation.

Table 3.4: Performance comparison of 5-level inverter with D2L inverter

| Performance parameter | Type of inverter | Modulation index(*m*) | | | |
|---|---|---|---|---|---|
| | | 0.2 | 0.4 | 0.6 | 0.8 |
| Level of operation | 5-level inverter | 3 | 3 | 5 | 5 |
| | D2L inverter | 3 | 3 | 3 | 3 |
| RMS of phase-A voltage (*V*) | 5-level inverter | 66.41 | 118.8 | 173.9 | 229.3 |
| | D2L inverter | 94.15 | 132.9 | 184 | 237.8 |
| RMS of phase-A current (*A*) | 5-level inverter | 0.886 | 0.977 | 0.995 | 0.998 |
| | D2L inverter | 0.893 | 0.976 | 0.998 | 0.968 |
| Frequency of phase voltage (*Hz)* | 5-level inverter | 10 | 20 | 30 | 40 |
| | D2L inverter | 10 | 20 | 30 | 40 |
| THD of phase-A voltage in % | 5-level inverter | 61.50 | 32.13 | 9.55 | 7.85 |
| | D2L inverter | 132.53 | 61.21 | 13.10 | 31.97 |
| Order of dominant voltage harmonic (amplitude in %) | 5-level inverter | 200±1 (15.91) | 100±1 (11.15) | 66±1 (7.48) | 50±1 (7.37) |
| | D2L inverter | 200±1 (71.76) | 100±1 (15.59) | 66±1 (17.32) | 50±1 (32.18) |
| THD of phase-A current in % | 5-level inverter | 5.13 | 4.65 | 1.58 | 4.90 |
| | D2L inverter | 10.21 | 9.48 | 1.26 | 10.58 |
| Order of dominant current harmonic (amplitude in %) | 5-level inverter | 100±2 (2.36) | 50±2 (1.65) | 17 (1.56) | 5 (4.70) |
| | D2L inverter | 200±1 (5.57) | 50±2 (4.43) | 66±1 (3.55) | 3 and 15 (3.92) |

### 3.7 Conclusion

A 5-level inverter using 3-level inverter and conventional two-level is realized for open-end winding induction motor drive. The describe scheme generates 512 voltage space vectors distributed over 61 locations. The presented 5-level inverter scheme completely

eliminates the requirement of clamping diodes and DC-link capacitors which are required in neutral point clamped (NPC) inverter. In comparison to 5-level cascade H-bridge (CHB) inverter which requires six isolated DC supply of rating $V_{DC}/4$, the adopted 5-level scheme requires only three isolated DC supplies. The adopted scheme does not need any flying capacitors as they are required in flying capacitor MLI topology. A switching function based mathematical model is developed and simulation study has been carried out using MATLAB/Simulink to evaluate the performance of inverter and results are presented. From the simulation results, it can be observed that the adopted scheme generates the voltages similar to conventional 5-level inverters. In simulation results it is found that the voltage and current harmonic spectrums of the presented 5-level inverter fed open-end winding induction motor drive are improved in comparison to dual two level (D2L) inverter fed open-end winding induction motor drive, but still it does not meet the IEEE-519 standards. The drive operation is found stable under steady state as well as transient conditions. The transition of drive operation from two-level to 5-level or from 5-level to two-level take place instantaneously and drive achieves its steady state within few cycles.

In the next chapter, a 9-level inverter is proposed to further improve the quality of inverter output voltage.

# CHAPTER 4: NINE-LEVEL INVERTER FOR INDUCTION MOTOR DRIVE

*[This chapter describes 9-level inverter scheme for open-end induction motor drive. A switching function based mathematical model of the proposed scheme is developed and validated by detailed analytical results in MATLAB/Simulink environment. A modified level shifted triangular carrier based space vector pulse width modulation (SVPWM) scheme is proposed to reduce the switching losses at lower speed operation and to get the even number of level operation. The steady state and transient state performance of the SVPWM based 9-level inverter scheme is evaluated by operating an open-end winding induction motor at no-load in constant V/f mode.]*

## 4.1 Introduction

In Chapter-3, five level inversion operation is achieved by feeding one end of the open-end winding IM by 3-level inverter and other end by conventional two-level inverter. The 5-level inverter generates 512 voltage space vectors distributed over 61 locations. The performance of inverter was good, but not meets out the IEEE-519 standards. In this chapter, a 9-level inverter topology is proposed to further improve the quality of output voltage. In the proposed topology open-end winding induction motor is fed from both ends by three-phase 3-level cascade inverter. The 3-level inverter is realized by connecting two, two-level inverter in cascade as discussed in previous chapter. Each 3-level inverter is powered by two isolated DC voltage sources of the same magnitude. As both the 3-level inverters are fed by isolated DC sources hence flow of zero sequence currents is not possible in proposed inverter. The proposed inverter needs only twenty four IGBTs whereas the conventional topologies NPC, FC and CHB based 9-level inverters require forty eight IGBTs. Although asymmetrical cascade H-bridge (ACHB) [49] 9-level inverter also uses twenty four IGBTs, but it requires six isolated DC supply whereas proposed topology needs only four isolated DC supplies. The 9-level FC inverter requires eighty four capacitors of rating $V_{DC}/8$ which are completely eliminated in the proposed inverter. The proposed topology does not require clamping diodes and capacitors whereas NPC 9-level inverter requires 168 clamping diodes and eight capacitors of rating $V_{DC}/8$. Though proposed topology uses four isolated DC supply in comparison with the NPC and FC topologies, but it inherently prevents the flow of triplen harmonic current through the switches and motor windings. The resultant space vector locations generated by proposed 9-level inverter for open-end winding induction motor are similar to the conventional (NPC, FC, CHB) 9-level inverters.

In this chapter, an alternative switching strategy has been also proposed. The proposed SVPWM based switching strategy is an improvisation over the one adopted in Chapter-3. The proposed PWM strategy ensures that the changeover of inverter operation from two level to 9-level mode including even number of level operation. An important advantage of proposed PWM scheme is that in lower speed range switching losses are reduced.

## 4.2 9-Level Inverter Scheme for Induction Motor Drive

### 4.2.1 Power Circuit

The power circuit of proposed 9-level inverter scheme for open-end winding induction motor is shown in Fig. 4.1. Both ends of the open-end winding ($A_2$, $B_2$, $C_2$) is connected with 3-level 'Inverter-A' and the other end ($A_4$, $B_4$, $C_4$) is connected with 3-level 'Inverter-B'. Inverter-A is having two conventional two-level inverters 'Inverter-1' and 'Inverter-2' and 'Inverter-B' is also consist of two two-level inverters 'Inverter-3' and 'Inverter-4'. The DC link voltage of 'Inverter-1' and 'Inverter-2' are (3/8)$V_{DC}$ , whereas 'Inverter-3' and 'Inverter-4' are of (1/8)$V_{DC}$ where $V_{DC}$ is the equivalent DC link voltage required to operate the conventional two-level inverter fed induction motor drive. The pole voltages $V_{A2O}$, $V_{B2O}$ or $V_{C2O}$ of 3-level 'Inverter-A' can have any of three levels 0, (3/8)$V_{DC}$ or (6/8)$V_{DC}$ independently. Inverter-B pole voltages with respect to its own reference point O′ are $V_{A4O'}$, $V_{B4O'}$ and $V_{C4O'}$. These pole voltages can also have any of three levels 0, (1/8)$V_{DC}$ or (2/8)$V_{DC}$ independently. The combine effect of these two, 3-level inverters is the generation of nine different levels in the phase winding of induction motor. These levels are -(2/8)$V_{DC}$, -(1/8)$V_{DC}$, 0, (1/8)$V_{DC}$, (2/8)$V_{DC}$, (3/8)$V_{DC}$, (4/8)$V_{DC}$, (5/8)$V_{DC}$ and (6/8)$V_{DC}$. The switches of 'Inverter-2' have to be rated for (6/8)$V_{DC}$ because they block (6/8)$V_{DC}$ when the top switches of 'Inverter-1' are 'ON'. Similarly switches in 'Inverter-4' are of (2/8)$V_{DC}$ rating as they have to block (2/8)$V_{DC}$ when the top switches of 'Inverter-3' will be 'ON'.

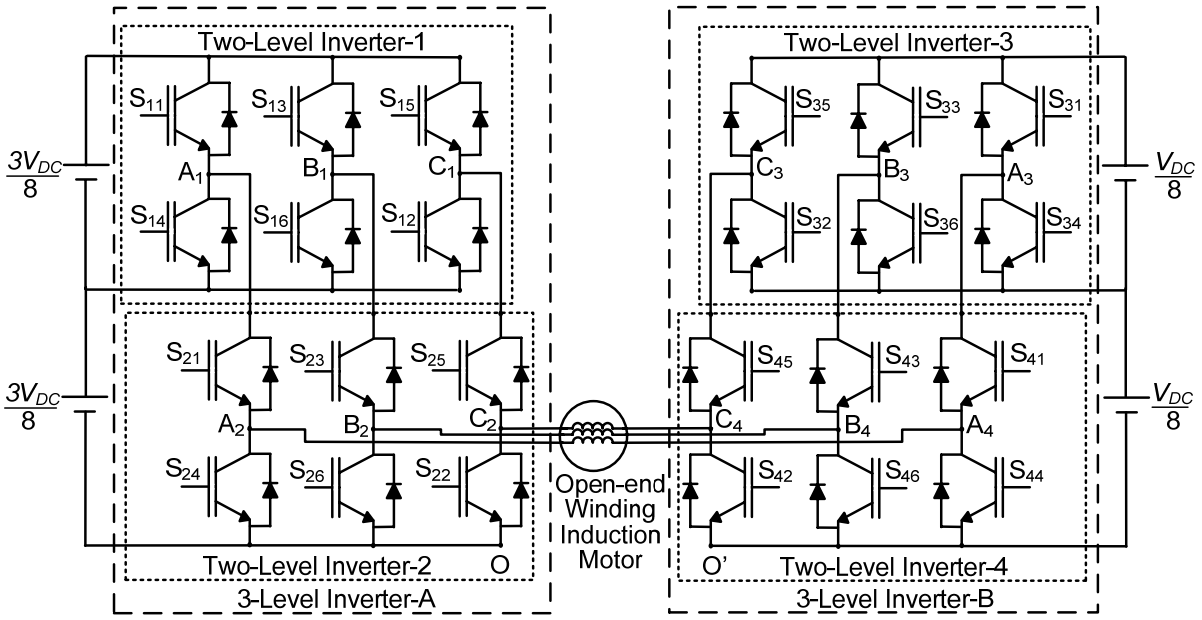



Fig. 4.1: Power circuit of 9-level inverter for open-end winding induction motor drive

#### 4.2.1.1 Comparison between Proposed Inverter and Conventional MLI

The proposed nine-level inverter topology is compared with the conventional nine-level inverter topologies, in terms of the components require and results are tabulated in Table 4.1. The proposed inverter needs only twenty four IGBTs whereas the conventional topologies NPC, FC and CHB based nine-level inverters require forty eight IGBTs. Although asymmetrical cascade H-bridge (ACHB) also uses twenty four IGBTs, but it requires six isolated DC supply whereas proposed topology needs only four isolated DC supplies. The nine-level FC inverter requires eighty four capacitors of rating $V_{DC}/8$ which are completely eliminated in the proposed inverter. The proposed topology does not require clamping diodes and capacitors whereas NPC nine-level inverter requires 168 clamping diodes and eight capacitors of rating $V_{DC}/8$. Though proposed topology uses four isolated DC supply in comparison with the NPC and FC topologies, but it prevents the flow of triplen harmonic current through the switches and motor windings.

Table 4.1: Comparison of nine-level inverter topologies

| Component (Rating) | NPC | FC | CHB | ACHB[1] | Proposed Inverter |
|---|---|---|---|---|---|
| DC source ($V_{DC}$) | 1 | 1 | 0 | 0 | 0 |
| DC source ($3V_{DC}/8$) | 0 | 0 | 0 | 3 | 2 |
| DC source ($V_{DC}/8$) | 0 | 0 | 12 | 3 | 2 |
| IGBT ($V_{DC}/8$) | 48 | 48 | 48 | 12 | 6 |
| IGBT ($V_{DC}/4$) | 0 | 0 | 0 | 0 | 6 |
| IGBT ($3V_{DC}/8$) | 0 | 0 | 0 | 12 | 6 |
| IGBT ($3V_{DC}/4$) | 0 | 0 | 0 | 0 | 6 |
| Clamping diode ($V_{DC}/8$) | 168 | 0 | 0 | 0 | 0 |
| Capacitor[2] ($V_{DC}/8$) | 8 | 84 | 0 | 0 | 0 |

Note: [1]ACHB is the asymmetrical cascade H-bridge with voltage source scaled in power of 3[49]
[2] Excluding rectifier capacitors

### 4.2.2 Switching Logic

Inverter-A pole voltage $V_{A2O}$ can have different voltage levels depending upon the status of corresponding switches. The pole voltage $V_{A2O}$ will be at level of $(6/8)V_{DC}$ if the switch $S_{21}$ and $S_{11}$ are made to turn 'ON', and at level of $(3/8)V_{DC}$ if the switch $S_{21}$ and $S_{14}$ are made to turn 'ON' and for zero level, switch $S_{24}$ has to be made turn 'ON'. Any pole voltage of 3-level 'Inverter-A' $V_{A2O}$, $V_{B2O}$ or $V_{C2O}$ can have these three levels by proper selection of

switches of two-level 'Inverter-1' and 'Inverter-2', which are made to be turned 'ON'. Similarly the 'Inverter-B' pole voltage $V_{A4O'}$ can have voltage level of $(2/8)V_{DC}$ if the switch $S_{41}$ and $S_{31}$ are made to turn 'ON', and at level of $(1/8)V_{DC}$ if the switch $S_{41}$ and $S_{34}$ are made to turn 'ON' and for zero level, switch $S_{44}$ has to be made turn 'ON'. Any pole voltage of three-level 'Inverter-B' $V_{A4O'}$, $V_{B4O'}$ or $V_{C4O'}$ can have these three levels by proper selection of switches of two-level 'Inverter-3' and 'Inverter-4', which are made to be turned 'ON'. When both 3-level inverters operate simultaneously nine distinct voltage levels generate in the phase voltage of open-end winding induction motor as shown in Table 4.2. It is clear from the Table 4.2 that the voltage levels $-(2/8)V_{DC}$ (Level-$L_1$), $-(1/8)V_{DC}$ (Level-$L_2$) and 0 (Level-$L_3$) can be generated by clamping the 'Inverter-A' at 'zero' voltage level and switching the 'Inverter-B' between $(2/8)V_{DC}$, $(1/8)V_{DC}$ and zero. Similarly voltage levels $+(1/8)V_{DC}$ (Level-$L_4$), $+(2/8)V_{DC}$ (Level-$L_5$) and $+(3/8)V_{DC}$ (Level-$L_6$) can be generated by clamping the 'Inverter-A' at $(3/8)V_{DC}$ and switching the 'Inverter-B' between $(2/8)V_{DC}$, $(1/8)V_{DC}$ and zero. The upper three voltage levels $+(4/8)V_{DC}$ (Level-$L_7$), $+(5/8)V_{DC}$ (Level-$L_8$) and $+(6/8)V_{DC}$ (Level-$L_9$) are generated by clamping the 'Inverter-A' at $(6/8)V_{DC}$ and switching the 'Inverter-B' between $(2/8)V_{DC}$, $(1/8)V_{DC}$ and zero. Switching states of corresponding switches of all four two-level inverters to realize nine-levels across the phase-A winding of open-end IM are shown in Table 4.3. Similar logic can also be implemented for others phases. Switches correspond to same leg of any two-level inverter operate in complementary fashion.

Table 4.2: Nine levels realised in phase-A for combinations of pole voltages of inverter-A and inverter-B

| Level | Pole voltage of 3-level Inverter-A ($V_{A2O}$) | Pole voltage of 3-level Inverter-B ($V_{A4O'}$) | Motor phase-A voltage level ($V_{A2O}$ -$V_{A4O'}$) |
|---|---|---|---|
| $L_1$ | 0 | $(2/8)V_{DC}$ | $-(2/8)V_{DC}$ |
| $L_2$ | 0 | $(1/8)V_{DC}$ | $-(1/8)V_{DC}$ |
| $L_3$ | 0 | 0 | 0 |
| $L_4$ | $(3/8)V_{DC}$ | $(2/8)V_{DC}$ | $+(1/8)V_{DC}$ |
| $L_5$ | $(3/8)V_{DC}$ | $(1/8)V_{DC}$ | $+(2/8)V_{DC}$ |
| $L_6$ | $(3/8)V_{DC}$ | 0 | $+(3/8)V_{DC}$ |
| $L_7$ | $(6/8)V_{DC}$ | $(2/8)V_{DC}$ | $+(4/8)V_{DC}$ |
| $L_8$ | $(6/8)V_{DC}$ | $(1/8)V_{DC}$ | $+(5/8)V_{DC}$ |
| $L_9$ | $(6/8)V_{DC}$ | 0 | $+(6/8)V_{DC}$ |

Table 4.3: Switching states of phase-A related switches of all the four inverters for nine-level operation

| Level | Motor Phase-A Voltage Level | Switch (State) Inverter-1 | Switch (State) Inverter-2 | Switch (State) Inverter-3 | Switch (State) Inverter-4 |
|---|---|---|---|---|---|
| $L_1$ | -(2/8)$V_{DC}$ | $S_{14}$ (ON) | $S_{24}$ (ON) | $S_{31}$ (ON) | $S_{41}$ (ON) |
| $L_2$ | -(1/8)$V_{DC}$ | $S_{14}$ (ON) | $S_{24}$ (ON) | $S_{34}$ (ON) | $S_{41}$ (ON) |
| $L_3$ | 0 | $S_{14}$ (ON) | $S_{24}$ (ON) | $S_{34}$ (ON) | $S_{44}$ (ON) |
| $L_4$ | +(1/8)$V_{DC}$ | $S_{14}$ (ON) | $S_{21}$ (ON) | $S_{31}$ (ON) | $S_{41}$ (ON) |
| $L_5$ | +(2/8)$V_{DC}$ | $S_{14}$ (ON) | $S_{21}$ (ON) | $S_{34}$ (ON) | $S_{41}$ (ON) |
| $L_6$ | +(3/8)$V_{DC}$ | $S_{14}$ (ON) | $S_{21}$ (ON) | $S_{34}$ (ON) | $S_{44}$ (ON) |
| $L_7$ | +(4/8)$V_{DC}$ | $S_{11}$ (ON) | $S_{21}$ (ON) | $S_{31}$ (ON) | $S_{41}$ (ON) |
| $L_8$ | +(5/8)$V_{DC}$ | $S_{11}$ (ON) | $S_{21}$ (ON) | $S_{34}$ (ON) | $S_{41}$ (ON) |
| $L_9$ | +(6/8)$V_{DC}$ | $S_{11}$ (ON) | $S_{21}$ (ON) | $S_{34}$ (ON) | $S_{44}$ (ON) |

### 4.2.3 Analysis of Voltage Space Vectors

The expression for equivalent voltage space vector $V_s$ can be derived in the same manner as of D2L inverter. The equivalent voltage space vector $V_s$ is given by

$$V_s = V_{A2A4} + V_{B2B4}.e^{j(2\pi/3)} + V_{C2C4}.e^{j(4\pi/3)} \tag{4.1}$$

In terms of pole voltage equation (4.1) can be written as:

$$V_s = (V_{A2O} - V_{A4O'}) + (V_{B2O} - V_{B4O'}).e^{j(2\pi/3)} + (V_{C2O} - V_{C4O'}).e^{j(4\pi/3)} \tag{4.2}$$

The voltage space vector $V_s$ can be resolve in terms of α-β axis components and given by:

$$V_s = V_{s(\alpha)} + jV_{s(\beta)} \tag{4.3}$$

Where $V_{s(\alpha)}$ is the summation of all components of $V_{A2A4}$, $V_{B2B4}$ and $V_{C2C4}$ in the direction of α-axis and $V_{s(\beta)}$ is the addition of all the components of $V_{B2B4}$ and $V_{C2C4}$ along the β-axis.

$$V_{s(\alpha)} = V_{A2A4(\alpha)} + V_{B2B4(\alpha)} + V_{C2C4(\alpha)} \tag{4.4}$$

$$V_{s(\beta)} = V_{B2B4(\beta)} + V_{C2C4(\beta)} \tag{4.5}$$

In matrix form $V_{s(\alpha)}$ and $V_{s(\beta)}$ combined can be written as follows:

$$\begin{bmatrix} V_{s(\alpha)} \\ V_{s(\beta)} \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{A2A4} \\ V_{B2B4} \\ V_{C2C4} \end{bmatrix} \tag{4.6}$$

In terms of pole voltages equation (4.6) can be written as:

$$\begin{bmatrix} V_{s(\alpha)} \\ V_{s(\beta)} \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{A2O} - V_{A4O'} \\ V_{B2O} - V_{B4O'} \\ V_{C2O} - V_{C4O'} \end{bmatrix} \quad (4.7)$$

Depending upon the switching state pole voltages can be obtained as described in section 4.2.2 and once pole voltages are known $V_s$ can be calculated using equations (4.3) and (4.7). Each 3-level inverter can generate 64 switching state as they are having two, two-level inverter in cascade combination and each two-level inverter can generate eight switching states hence total of 64 (8×8) different combination of space phasors. Together these two three-level 'Inverter-A' and 'Inverter-B', will generate total of 4096 (64×64) space phasors distributed over 217 locations as shown in Fig. 4.2. The redundant, switching states are used to minimize the switching losses.

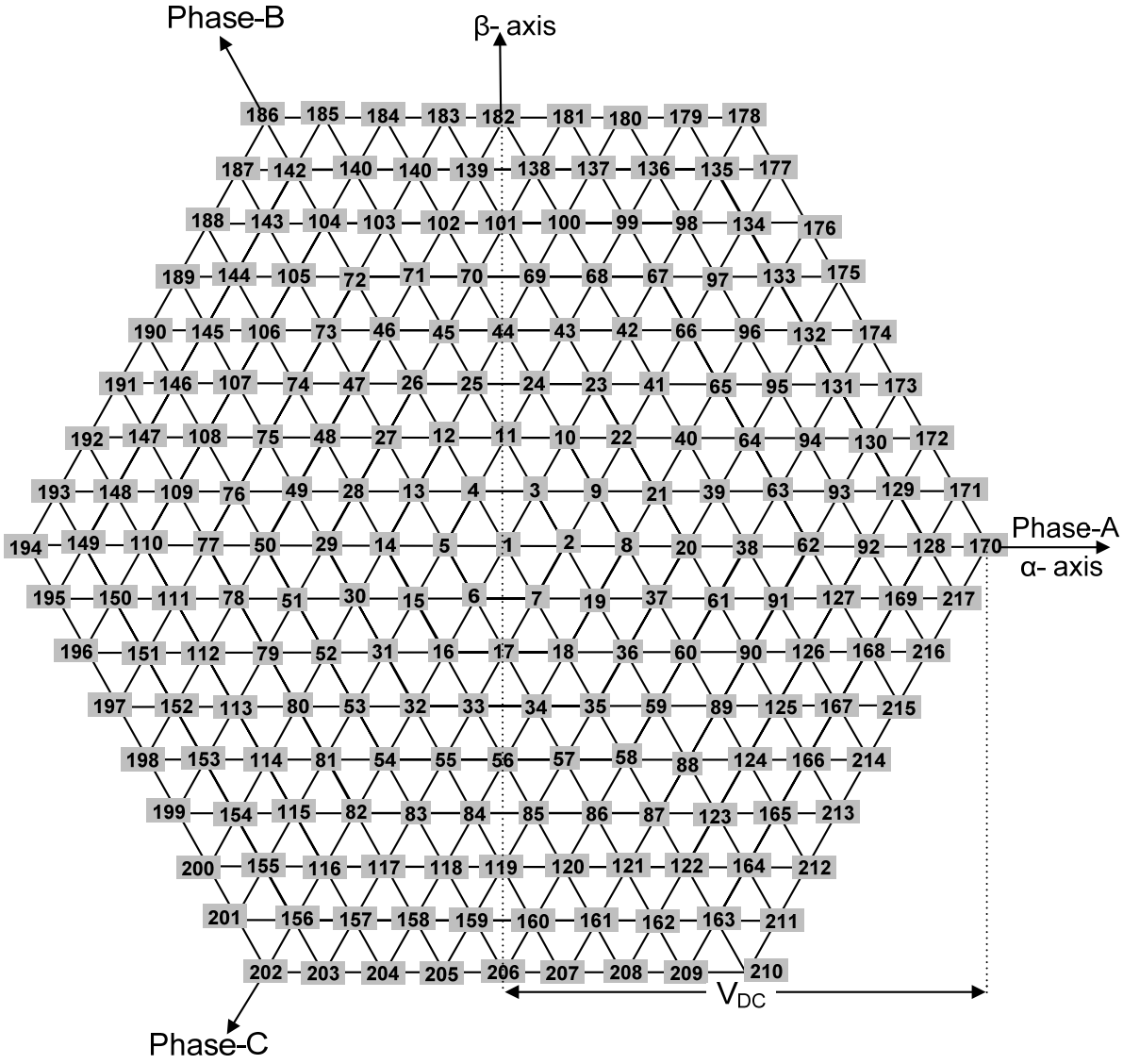



Fig. 4.2: Locations of voltage space-phasors for 9-level inverter

### 4.2.4 Effect of common-mode voltage

In the above discussion it is assumed that the points O and O′ are connected, but in actual they are isolated hence there will be voltage difference between these two points, this voltage is known as common-mode voltage [184]. The actual phase voltages are given by equations (4.8)-(4.10).

$$V_{A2A4} = V_{A2O} + V_{OO'} - V_{A4O'} \tag{4.8}$$

$$V_{B2B4} = V_{B2O} + V_{OO'} - V_{B4O'} \tag{4.9}$$

$$V_{C2C4} = V_{C2O} + V_{OO'} - V_{C4O'} \tag{4.10}$$

Where $V_{OO'}$ is the common mode voltage and given by:

$$V_{OO'} = \frac{(V_{A4O'} + V_{B4O'} + V_{C4O'}) - (V_{A2O} + V_{B2O} + V_{C2O})}{3} \tag{4.11}$$

After substituting the expression for phase voltages in equation (4.1), $V_s$ can be expressed as follows:

$$\begin{aligned} V_s &= (V_{A2O} + V_{OO'} - V_{A4O'}) + (V_{B2O} + V_{OO'} - V_{B4O'}).e^{j(2\pi/3)} \\ &\quad + (V_{C2O} + V_{OO'} - V_{C4O'}).e^{j(4\pi/3)} \\ &= (V_{A2O} - V_{A4O'}) + (V_{B2O} - V_{B4O'}).e^{j(2\pi/3)} + (V_{C2O} - V_{C4O'}).e^{j(4\pi/3)} \\ &\quad + (V_{OO'} + V_{OO'}.e^{j(2\pi/3)} + V_{OO'}.e^{j(4\pi/3)}) \end{aligned} \tag{4.12}$$

Since for balance system

$$V_{OO'} + V_{OO'}.e^{j(2\pi/3)} + V_{OO'}.e^{j(4\pi/3)} = V_{OO'} - \frac{1}{2}V_{OO'} - \frac{1}{2}V_{OO'} = 0$$

Therefore, equation (4.12) reduced to

$$V_s = (V_{A2O} - V_{A4O'}) + (V_{B2O} - V_{B4O'}).e^{j(2\pi/3)} + (V_{C2O} - V_{C4O'}).e^{j(4\pi/3)} \tag{4.13}$$

This equation is same as that derived in section 4.2.3 assuming that points O and O' are connected. Hence the effect of common mode voltage only generation of multiplicity of space vectors in different locations, and the system with unconnected points O and O′ will generates the same voltage space vectors as generated by $V_s$.

### 4.2.5 Selection of DC Link Voltage Ratio

In open-end winding configuration the maximum number of voltage levels achievable is the product of the voltage levels of the individual inverters. In the proposed topology both sides inverters are 3-level so the maximum 9-level we can achieve across the phase winding. To achieve the 9-level operation the DC link voltages of 3-level inverters are selected in the ration as given in equation (4.14). If DC link voltages of 3-level 'Inverter-A' and 'Inverter-B' are $V_{DC1}$ and $V_{DC2}$ then ratio $V_{DC2}/V_{DC1}$ will be given by

$$\frac{V_{DC2}}{V_{DC1}} = \frac{n_2 - 1}{n_2(n_1 - 1)} = \frac{3 - 1}{3(3 - 1)} = \frac{1}{3} \tag{4.14}$$

Where $n_1$ and $n_2$ are the number of levels in pole voltages of 'Inverter-A' and 'Inverter-B' respectively ($n_1 = n_2 = 3$).

The total DC link voltage required to operate conventional two-level inverter fed induction motor drive is $V_{DC}$, therefore

$$V_{DC1} + V_{DC2} = V_{DC} \tag{4.15}$$

From equation (4.14) and (4.15) the values of $V_{DC1}$ and $V_{DC2}$ are come out to be $3/4V_{DC}$ and $1/4V_{DC}$ respectively. The DC link voltage of 3-level inverters is equally distributed between their respective two-level inverters as shown in Fig. 4.1.

### 4.3 Modified SVPWM technique for the proposed nine-level inverter

The modulation scheme adopted in Chapter-3 to generate PWM pulses for 5-level inverter has a drawback that inverter operates either in 3-level or 5-level mode and even number of operation like two-level or 4-level was not possible in this scheme. Due to this drawback switching losses increase because at lower modulation index inverter operates in 3-level mode of operation whereas it is suppose to operate in two-level mode. Similarly when 4-level operation is required inverter operates in 5-level mode hence switching losses increase. To overcome this problem a modified space vector pulse width modulation (SVPWM) technique is proposed. The proposed scheme started with two-level operation and gradually goes up to 9-level operation as the modulation index increases. The proposed scheme required eight level shifted triangular carrier pulses (N-1, for N-level inverter) all having the same peak-to-peak amplitude $V_c$ equal to $V_{DC}/8$; in general $V_{DC}$/N-1. The frequency ($f_c$) of triangular carrier wave is selected as 1kHz this parameter decides the switching frequency of the inverter. The entire range of operation is divided into nine regions $R_1$-$R_9$ by eight level shifted triangular carrier waves C1 - C8. The region below the first triangular carrier C1 is define as $R_1$, region between C1 and C2 is $R_2$ similarly region between C2 and C3 is called $R_3$, in the same way $R_4$-$R_8$ are define and finally $R_9$ is the region above last triangular carrier C8. Regions $R_1$-$R_9$ corresponds to voltage levels $L_1$ to $L_9$ as shown in Table 4.2. The magnitude of reference phasor $V^*_s$ is calculated from the motor speed requirement by using constant *V/f* control. A factor of 2/3 is used to get the desired magnitude of reference phase voltage. The three phase voltages are generated as given by:

$$\left.\begin{aligned} V_a &= V_m^* Sin\omega t \\ V_b &= V_m^* Sin(\omega t - 2\pi/3) \\ V_c &= V_m^* Sin(\omega t + 2\pi/3) \end{aligned}\right\} \tag{4.16}$$

Now an offset voltage as given in equation (4.17) is added to these phase voltages to optimize the THD content in inverter output voltage and increase the utilization of DC link voltage.

$$V_{offset} = -[\max(V_a, V_b, V_c) + \min(V_a, V_b, V_c)]/2 \tag{4.17}$$

The new reference wave after addition of offset will be given as:

$$\left.\begin{aligned} V_a^* &= V_m^* Sin\omega t - [\max(V_a,V_b,V_c)+\min(V_a,V_b,V_c)]/2 \\ V_b^* &= V_m^* Sin(\omega t - 2\pi/3) - [\max(V_a,V_b,V_c)+\min(V_a,V_b,V_c)]/2 \\ V_c^* &= V_m^* Sin(\omega t + 2\pi/3) - [\max(V_a,V_b,V_c)+\min(V_a,V_b,V_c)]/2 \end{aligned}\right\} \quad (4.18)$$

In the conventional level shifted SVPWM scheme at lower speed such that $V_m^* \le V_c/2$ the three reference wave are situated at the centre of level shifted carrier set as shown in Fig. 4.3 (a). In this case inverter operates in 3-level mode of operation because the reference wave at different instants could be in $L_4$ (+$V_{DC}$/8), $L_5$ (+2$V_{DC}$/8) or $L_6$ (+3$V_{DC}$/8) and switching occur in both the two-level inverters constituting 3-level 'Inverter-B' (Fig. 4.1). In the proposed scheme for this range of speed reference waves are placed at the middle of the lower most carrier wave C1 as shown in Fig. 4.3 (b). In this case proposed 9-level inverter operates in two-level mode because reference wave resides only in $L_1$ (-2$V_{DC}$/8) and $L_2$ (-$V_{DC}$/8) hence switching losses are only due to two-level inverter-3. The proposed 9-level inverter operates in two-level mode of operation until $\left|V_s^*\right| \le \frac{\sqrt{3}}{16} V_{DC}$ and in this range of speed the tip of the space vector $V_s^*$ is situated within the innermost hexagon created by space vector locations 2-3-4-5-6-7 shown in Fig. 4.2. For the next speed range such that $V_c/2 < V_m^* \le V_c$ the reference wave will remain in $L_4$ (+$V_{DC}$/8), $L_5$ (+2$V_{DC}$/8) or $L_6$ (+3$V_{DC}$/8) at different instants in case of conventional level shifted SVPWM so the inverter operates in 3-level mode of operation.

In proposed modulation scheme an additional DC bias of magnitude $V_c/2$ is given to the reference waves so that they are placed at the middle of triangular carrier C1 and C2 and switching losses correspond to 3-level operation same as the conventional SVPWM scheme. In the same way when $V_c < V_m^* \le 3V_c/2$ the reference waves are positioned at the middle of three lower most carrier (C1, C2 and C3) in modified SVPWM scheme as shown in Fig. 4.3 (d). In this case switching losses correspond to 4-level operation as the reference waves lie in levels $L_1$-$L_4$ and switching occur in 'Inverter-2', 'Inverter-3' and 'Inverter-4' whereas in conventional SVPWM switching take place in all two-level inverters because reference waves reside in five levels $L_3$-$L_7$ as depicted in Fig. 4.3 (c). Similarly when reference voltage is such that $3V_c/2 < V_m^* \le 2V_c$ the reference waves in case of modified SVPWM are placed at the middle of four lower most carriers (C1-C4) and operating region is distributed from $L_1$ to $L_5$ whereas in conventional SVPWM scheme operating region lies between levels $L_3$-$L_7$ so in both the scheme switching losses correspond to 5-level operation. In the same way as the inverter operation shifted from 5-level to 6-level and so on up to 9-level a DC voltage of magnitude $V_c$/2 is added to reference wave in each step. The positions of reference waves

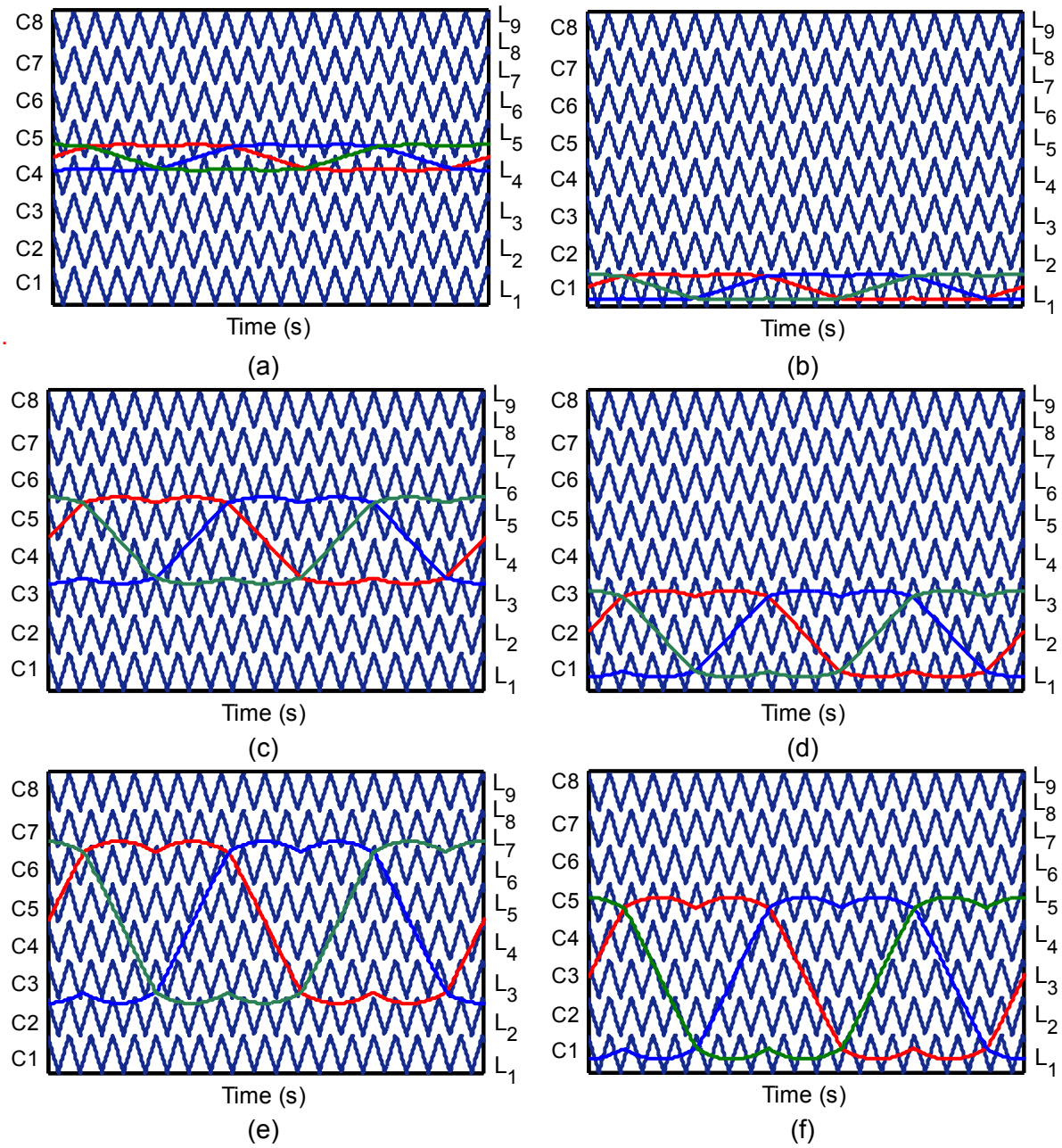



Fig. 4.3: (a) Reference waves during two-level operation in conventional SVPWM
(b) Reference waves during two-level operation in modified SVPWM
(c) Reference waves during 4-level operation in conventional SVPWM
(d) Reference waves during 4-level operation in modified SVPWM
(e) Reference waves during 6-level operation in conventional SVPWM
(f) Reference waves during 6-level operation in modified SVPWM

for 6-level operation in case of conventional and modified SVPWM are shown in Fig. 4.3 (e) and Fig. 4.3 (f) respectively. It is evident from Fig. 4.3 that for even number level operation (2, 4, 6, 8) the switching losses are comparatively less as compared to conventional level shifted SVPWM scheme. The higher speed range when $7V_c / 2 < V_m^*$ reference waves are placed at the middle of eight carriers (C1-C8) similar to conventional level shifted SVPWM scheme as depicted in Fig. 4.4. To get clear pictures to facilitate the

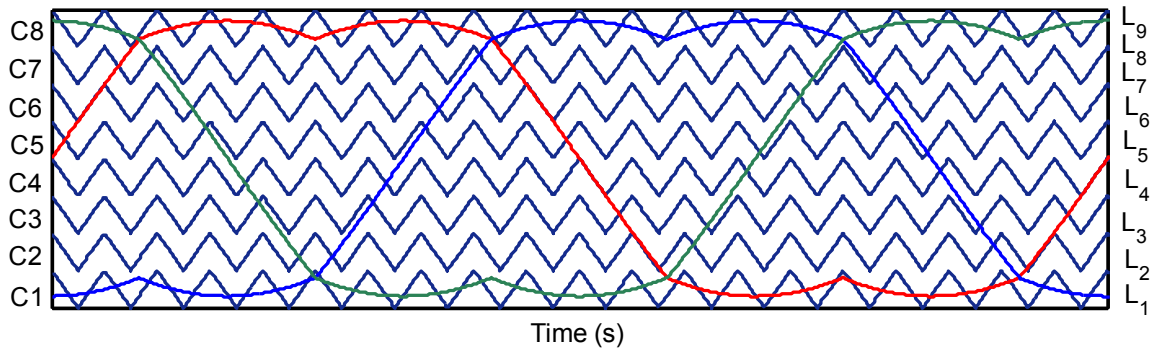



Fig. 4.4: Reference waves during 9-level operation in conventional and modified SVPWM

explanation of the proposed SVPWM strategy, it is assumed that the frequency of the modulating signals are constant; but in practice the frequency of the reference signal is varied by the control scheme employed to control the speed of the motor.

The modified modulating signals to implement the proposed scheme are generated by adding a progressive DC bias of magnitude $\frac{nV_c}{2}$ with respect to the bottom point of lower most carrier wave (C1) is added to the reference wave given by equation (4.18), where 'n' takes the value from 1 to 8 depending upon the region $R_2$ - $R_9$ in which peak of the modulating signals lie. So finally the modified modulating signals for three phases are expressed as:

$$\left.\begin{aligned} V_a^* &= V_m^* Sin\omega t - [\max(V_a,V_b,V_c)+\min(V_a,V_b,V_c)]/2 + nV_c/2 \\ V_b^* &= V_m^* Sin(\omega t - 2\pi/3) - [\max(V_a,V_b,V_c)+\min(V_a,V_b,V_c)]/2 + nV_c/2 \\ V_c^* &= V_m^* Sin(\omega t + 2\pi/3) - [\max(V_a,V_b,V_c)+\min(V_a,V_b,V_c)]/2 + nV_c/2 \end{aligned}\right\} \quad (4.19)$$

All the three modulating signals are simultaneously compared with eight triangular carriers in every sample period and depending upon the instantaneous position of modulating signal particular voltage level $L_1$ - $L_9$ is applied across the phase winding of motor. The proposed scheme generates equivalent voltage space vector $V_s^*$ as generated by conventional space vector modulation. The maximum magnitude of voltage space phasor in different level of operation is shown in Table 4.4. The modulation index ($m$) is define as the ratio of the magnitude of the required voltage space phasor ($|V_s^*|$) to the maximum magnitude of the voltage space phasor ($V_{DC}$) as given in equation (4.20). The maximum radius of the circle inscribed in the space vector diagram shown in Fig. 4.2 is $\sqrt{3}V_{DC}/2$ hence the limit of modulation index ($m$) for linear modulation is 0.866.

$$m = \frac{|V_s^*|}{V_{DC}} = \frac{3V_m^*/2}{V_{DC}} \quad (4.20)$$

The advantages of modified level shifted SVPWM over conventional level shifted SVPWM can be summarized as follows:

- In lower speed range inverter starts with two-level mode and gradually switches in to 3-level, 4-level, 5-level, 6-level, 7-level, 8-level and 9-level operation as reference speed increases.
- In lower speed range switching occur only in two-level 'Inverter-3' hence switching losses are reduced as compare to conventional level shifted SVPWM where switching occur in 'Inverter-3' and 'Inverter-4' both.
- Less switching occur in the two-level inverter which operates at higher DC link in case of modified scheme as compared to conventional scheme for middle speed range.

Table 4.4: Maximum magnitude of reference phasor $V^*_s$ in different operating regions

| Modulating Signal Lies Between | Mode of Operation | Maximum Magnitude of Reference Phasor $V^*_s$ | Voltage Levels Applied Across Phase |
|---|---|---|---|
| $R_1$ - $R_2$ | 2-Level | $(\sqrt{3}/16)V_{DC}$ | $L_1$ to $L_2$ |
| $R_1$ - $R_3$ | 3-Level | $(\sqrt{3}/8)V_{DC}$ | $L_1$ to $L_3$ |
| $R_1$ - $R_4$ | 4-Level | $(3\sqrt{3}/16)V_{DC}$ | $L_1$ to $L_4$ |
| $R_1$ - $R_5$ | 5-Level | $(\sqrt{3}/4)V_{DC}$ | $L_1$ to $L_5$ |
| $R_1$ - $R_6$ | 6-Level | $(5\sqrt{3}/16)V_{DC}$ | $L_1$ to $L_6$ |
| $R_1$ - $R_7$ | 7-Level | $(3\sqrt{3}/8)V_{DC}$ | $L_1$ to $L_7$ |
| $R_1$ - $R_8$ | 8-Level | $(7\sqrt{3}/16)V_{DC}$ | $L_1$ to $L_8$ |
| $R_1$ - $R_9$ | 9-Level | $(\sqrt{3}/2)V_{DC}$ | $L_1$ to $L_9$ |

### 4.4 Mathematical Modelling of Proposed 9-Level Inverter

A switching function based mathematical model of the proposed 9-level inverter is developed to derive the expression for three-phase voltages of open-end winding induction motor. First of all the pole voltages of 'Inverter-A' and 'Inverter-B' are derived in terms their respective switching functions then motor phase voltages are derived in terms of pole voltages. The following assumptions are made for the mathematical modelling:

- The DC link voltages available at the input terminals of all two-level inverters are ripple free.
- Switching transients in all two-level inverters are ignored.
- Switching transition times of the switching devices are considered to be negligible.

- The three-phase stator windings of the induction motor are balanced and produce sinusoidal magnetic field in the space.

### 4.4.1 Mathematical Model of 9-Level Inverter

The pole voltages of 3-level 'Inverter-A' in terms of switching function $SF_x$ (X=a, b, c) are given by:

$$\left.\begin{aligned} V_{A2O} &= \frac{V_{DC}}{8} SF_a \\ V_{B2O} &= \frac{V_{DC}}{8} SF_b \\ V_{C2O} &= \frac{V_{DC}}{8} SF_c \end{aligned}\right\} \tag{4.21}$$

The switching function $SF_X$ ($X$=a, b, c) can take three values 0, 3 and 6 depending upon the switching state (1=ON, 0=OFF) of the corresponding two-level inverter switch described as follows:

$$SF_a = \begin{cases} 0 & \text{when } S_{14}=1 \text{ and } S_{24}=1 \\ 3 & \text{when } S_{14}=1 \text{ and } S_{21}=1 \\ 6 & \text{when } S_{11}=1 \text{ and } S_{21}=1 \end{cases} \tag{4.22}$$

$$SF_b = \begin{cases} 0 & \text{when } S_{16}=1 \text{ and } S_{26}=1 \\ 3 & \text{when } S_{16}=1 \text{ and } S_{23}=1 \\ 6 & \text{when } S_{13}=1 \text{ and } S_{23}=1 \end{cases} \tag{4.23}$$

$$SF_c = \begin{cases} 0 & \text{when } S_{12}=1 \text{ and } S_{22}=1 \\ 3 & \text{when } S_{12}=1 \text{ and } S_{25}=1 \\ 6 & \text{when } S_{15}=1 \text{ and } S_{25}=1 \end{cases} \tag{4.24}$$

Similarly, other 3-level 'Inverter-B' pole voltages ($V_{A4O'}, V_{B4O'}, V_{C4O'}$) with respect to point-O' in terms of DC link voltages and switching functions are given by:

$$\left.\begin{aligned} V_{A4O'} &= \frac{V_{DC}}{8} SF_{a'} \\ V_{B4O'} &= \frac{V_{DC}}{8} SF_{b'} \\ V_{C4O'} &= \frac{V_{DC}}{8} SF_{c'} \end{aligned}\right\} \tag{4.25}$$

The switching function $SF_{X'}$ (X=a, b, c) can take three discreet values 0, 1 and 2 depending upon the condition described as follows:

$$SF_{a'} = \begin{cases} 0 & \text{when } S_{34}=1 \text{ and } S_{44}=1 \\ 1 & \text{when } S_{34}=1 \text{ and } S_{41}=1 \\ 2 & \text{when } S_{31}=1 \text{ and } S_{41}=1 \end{cases} \tag{4.26}$$

$$SF_{b'} = \begin{cases} 0 & \text{when } S_{36} = 1 \text{ and } S_{46} = 1 \\ 1 & \text{when } S_{36} = 1 \text{ and } S_{43} = 1 \\ 2 & \text{when } S_{33} = 1 \text{ and } S_{43} = 1 \end{cases} \quad (4.27)$$

$$SF_{c'} = \begin{cases} 0 & \text{when } S_{32} = 1 \text{ and } S_{42} = 1 \\ 1 & \text{when } S_{32} = 1 \text{ and } S_{45} = 1 \\ 2 & \text{when } S_{35} = 1 \text{ and } S_{45} = 1 \end{cases} \quad (4.28)$$

The three-phase motor voltages can be derived in terms of pole voltages by using equations (4.8)-(4.11) and expressed as:

$$\left.\begin{aligned} V_{A2A4} &= \frac{2}{3}(V_{A2O} - V_{A4O'}) - \frac{1}{3}(V_{B2O} - V_{B4O'}) - \frac{1}{3}(V_{C2O} - V_{C4O'}) \\ V_{B2B4} &= -\frac{1}{3}(V_{A2O} - V_{A4O'}) + \frac{2}{3}(V_{B2O} - V_{B4O'}) - \frac{1}{3}(V_{C2O} - V_{C4O'}) \\ V_{C2C4} &= -\frac{1}{3}(V_{A2O} - V_{A4O'}) - \frac{1}{3}(V_{B2O} - V_{B4O'}) + \frac{2}{3}(V_{C2O} - V_{C4O'}) \end{aligned}\right\} \quad (4.29)$$

Where $V_{A2A4}, V_{B2B4}, V_{C2C4}$ are the phase voltages of motor phase A, B and C respectively. Equation (4.29) can be written in matrix form as:

$$\begin{bmatrix} V_{A2A4} \\ V_{B2B4} \\ V_{C2C4} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} V_{A2O} - V_{A4O'} \\ V_{B2O} - V_{B4O'} \\ V_{C2O} - V_{C4O'} \end{bmatrix} \quad (4.30)$$

Now using equations (4.21), (4.25) and (4.30), the motor phase voltages can be expressed in terms of switching functions as:

$$\begin{bmatrix} V_{A2A4} \\ V_{B2B4} \\ V_{C2C4} \end{bmatrix} = \frac{V_{DC}}{24}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} SF_a - SF_{a'} \\ SF_b - SF_{b'} \\ SF_c - SF_{c'} \end{bmatrix} \quad (4.31)$$

The relationship between orthogonal components $V_{qs}$ and $V_{ds}$ of voltage space phasor in terms of phase voltages $V_{A2A4}$, $V_{B2B4}$, $V_{C2C4}$ is given by the transformation

$$\begin{bmatrix} V_{qs} \\ V_{ds} \\ V_{os} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/2 & 1/2 & 1/2 \end{bmatrix}\begin{bmatrix} V_{A2A4} \\ V_{B2B4} \\ V_{C2C4} \end{bmatrix} \quad (4.32)$$

These d-q components acts as inputs for the open-end winding induction motor model developed in section 2.4.2, to calculate the motor phase currents. The motor phase voltages can also be written in terms of line-to-line voltages of 'Inverter-A' and 'Inverter-B'. The line-to-line voltages of 'Inverter-A' are labeled as $V_{A2B2}$, $V_{B2C2}$, $V_{C2A2}$ whereas 'Inverter-B' line-to-line voltages are labeled as $V_{A4B4}$, $V_{B4C4}$, $V_{C4A4}$. The motor phase voltages $V_{A2A4}$, $V_{B2B4}$ and $V_{C2C4}$ can be related to line-to-line voltages of individual inverter as:

$$\left.\begin{aligned} V_{A2A4} - V_{B2B4} &= V_{A2B2} - V_{A4B4} \\ V_{B2B4} - V_{C2C4} &= V_{B2C2} - V_{B4C4} \\ V_{C2C4} - V_{A2A4} &= V_{C2A2} - V_{C4A4} \end{aligned}\right\} \quad (4.33)$$

For balance load $V_{A2A4} + V_{B2B4} + V_{C2C4} = 0$ so above equation can be rearranged and written as follows:

$$\left.\begin{aligned} V_{A2A4} &= \frac{V_{A2B2} - V_{C2A2}}{3} - \frac{V_{A4B4} - V_{C4A4}}{3} \\ V_{B2B4} &= \frac{V_{B2C2} - V_{A2B2}}{3} - \frac{V_{B4C4} - V_{A4B4}}{3} \\ V_{C2C4} &= \frac{V_{C2A2} - V_{B2C2}}{3} - \frac{V_{C4A4} - V_{B4C4}}{3} \end{aligned}\right\} \quad (4.34)$$

## 4.5 Simulation Results and Discussion

The performance of proposed 9-level inverter scheme for open-end winding IM drive is evaluated through simulation in MATLAB/Simulink environment. The simulation study is carried out in fixed-point simulation mode at a sampling time of 10 µSec. The mathematical model of 9-level inverter and open-end winding IM are developed in MATLAB/Simulink environment using S-function concept. The induction motor is operated in constant *V/f* mode under no-load condition covering the entire range of linear modulation. The switching frequency ($f_c$) is kept constant at 1kHz and DC link voltage ($V_{DC}$) is taken as 600V for simulation analysis. The motor phase-A voltage ($V_{A2A4}$), phase-A current ($i_{A2A4}$), their harmonic spectrums, inverters pole-A voltages ($V_{A2O}$, $V_{A4O'}$) and difference of inverters pole-A voltages ($V_{A2O}$ - $V_{A4O'}$) are considered as evaluation criteria. The performance of 9-level inverter scheme is evaluated under steady-state as well as transient-state conditions and results are presented in from Fig. 4.5 to Fig. 4.37.

The simulation results when inverter is operated in two-level mode of operation are presented in Fig. 4.5 through Fig. 4.8. The motor phase-A voltage ($V_{A2A4}$) and current ($i_{A2A4}$) at modulation index $m$ =0.08 are shown in Fig. 4.5. At this modulation index motor operates at fundamental frequency ($f^*_m$) of 4Hz and modulating signals are situated within the levels $L_1$ and $L_2$. The phase-A voltage ($V_{A2A4}$) and current ($i_{A2A4}$) waveforms are equivalent to conventional two-level inverter. The harmonic spectrum of phase-A voltage and current with respect to their fundamental component for the modulation index $m$ =0.08 are shown in Fig. 4.6 and Fig. 4.7 respectively. It is evident from these spectrums that the dominant harmonic component of phase voltage and current occur at the sideband of multiple of 250 ($f_c/f^*_m$ = 1000/4) i.e. $250^{th}$ and $500^{th}$ order. Lower order harmonics responsible for higher losses are significantly very low.

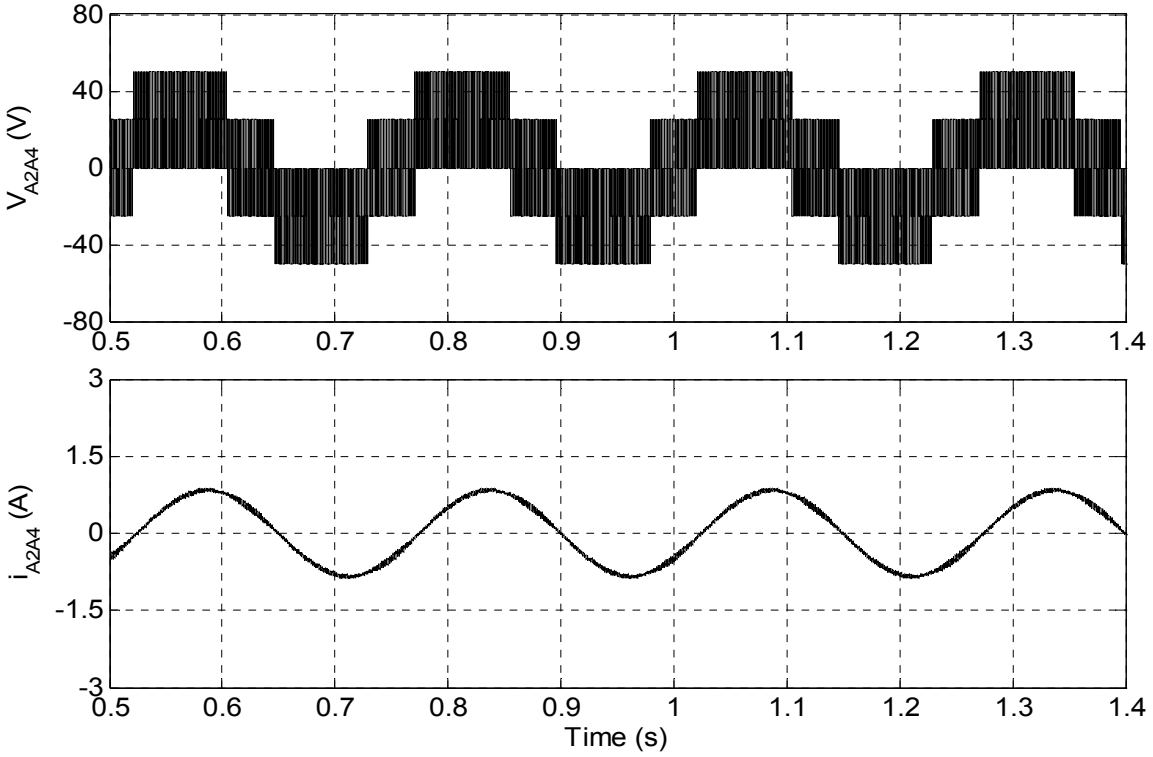



Fig. 4.5: Motor phase-A, voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) of 9-level inverter fed open-end IM drive at no load ($m$=0.08; $f^*_m$ =4Hz; 2-level mode)

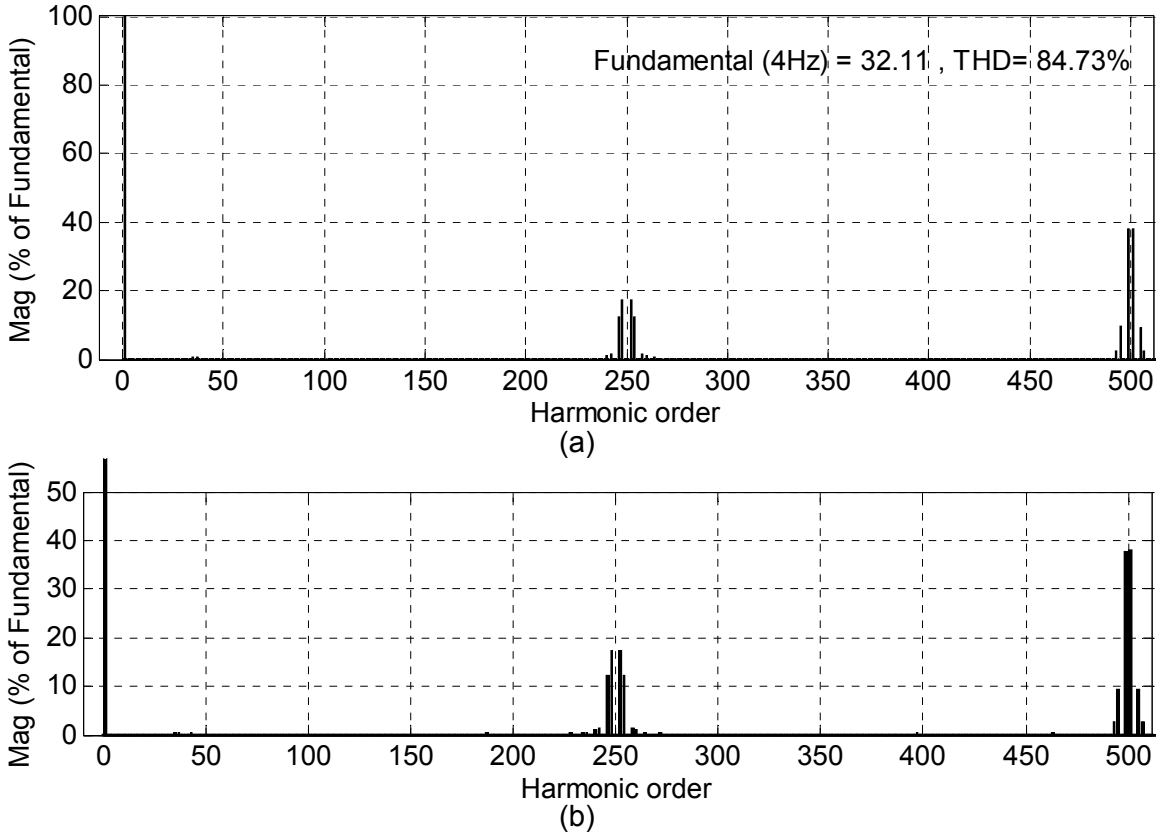



Fig. 4.6: (a) Harmonic spectrum of phase-A voltage ($V_{A2A4}$) at $m$=0.08; $f^*_m$ =4Hz
(b) Zoom view of harmonic spectrum shown in (a)

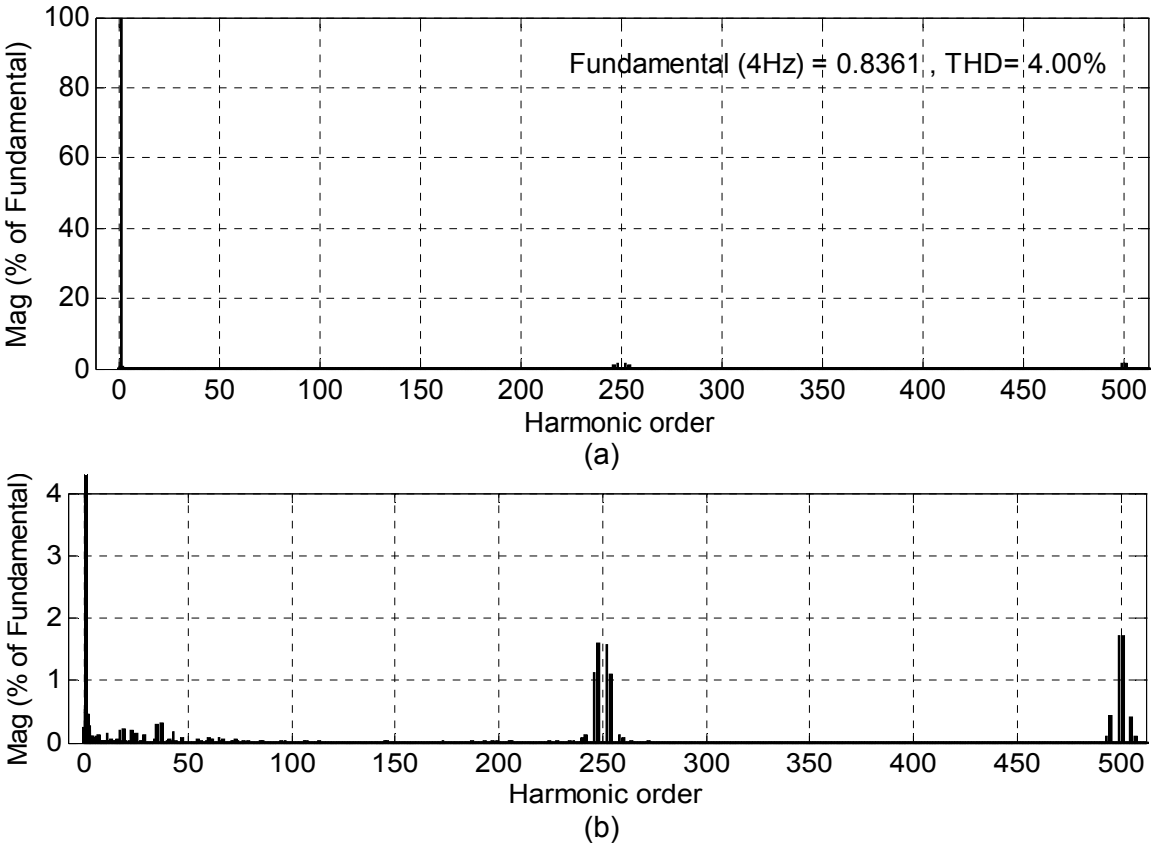



Fig. 4.7: (a) Harmonic spectrum of phase-A current ($i_{A2A4}$) at $m$=0.08; $f^*_m$ =4Hz
(b) Zoom view of harmonic spectrum shown in (a)

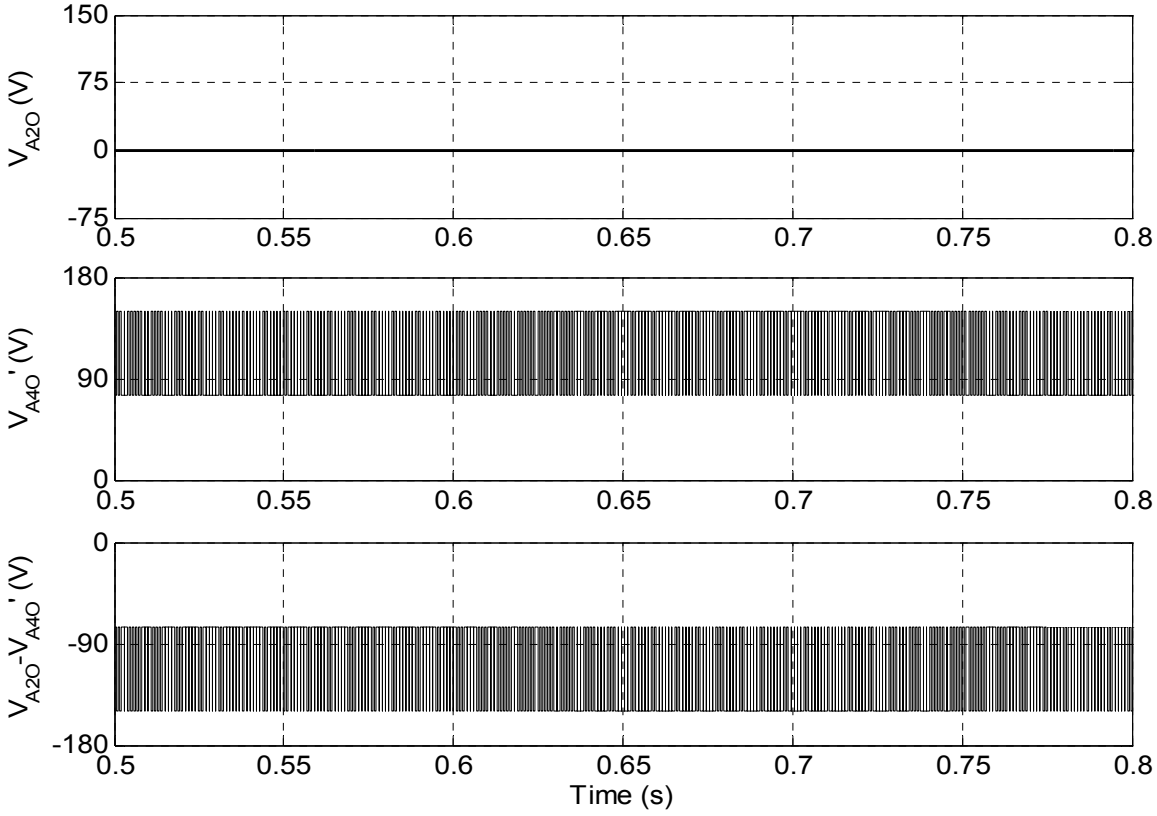



Fig. 4.8 :Top trace; Inverter-A pole voltage ($V_{A2O}$), Middle trace; Inverter-B pole voltage ($V_{A4O'}$), Bottom trace; Difference of Inverter-A and Inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$) at $m$=0.08; $f^*_m$ =4Hz (2-level mode)

The pole-A voltages ($V_{A2O}$, $V_{A4O'}$) and difference of these pole voltages ($V_{A2O}$ - $V_{A4O'}$) are shown in Fig. 4.8 for two-level mode of operation. It may be observed from pole voltages waveform that 3-level inverter-B operates in two-level mode ($2V_{DC}/8$ and $V_{DC}/8$) while the inverter-A is clamped at zero voltage level. The difference of pole voltages ($V_{A2O}$ - $V_{A4O'}$) switch between two voltage levels $-(2/8)V_{DC}$ and $-(1/8)V_{DC}$ which validate the logic of modified SVPWM scheme.

The waveforms for motor phase-A voltage ($V_{A2A4}$), phase-A current ($i_{A2A4}$), their harmonic spectrums, inverters pole-A voltages ($V_{A2O}$, $V_{A4O'}$) and difference of inverters pole-A voltages ($V_{A2O}$ - $V_{A4O'}$) at modulation index $m$ =0.16 are shown in Fig. 4.9 through Fig. 4.12. At this modulation index the modulating signals situated within the regions $R_1$ - $R_3$ and inverter operates in 3-level mode of operation. The fundamental frequency ($f^*_m$) of the motor for this modulation index is 8Hz. The motor phase-A voltage ($V_{A2A4}$) and current ($i_{A2A4}$) at modulation index $m$ =0.16 shown in Fig. 4.9 are equivalent to 3-level inverter waveforms. The THD of phase voltage is reduced to 40.79% from 84.73% as compared to two-level mode of operation; and dominant harmonic component occur at the side band of 250$^{th}$ ($2f_c/f^*_m$ = 2*1000/8) order as shown in Fig. 4.10. The total harmonic distortion (THD) in phase current is only 2.51% as shown in Fig. 4.11.

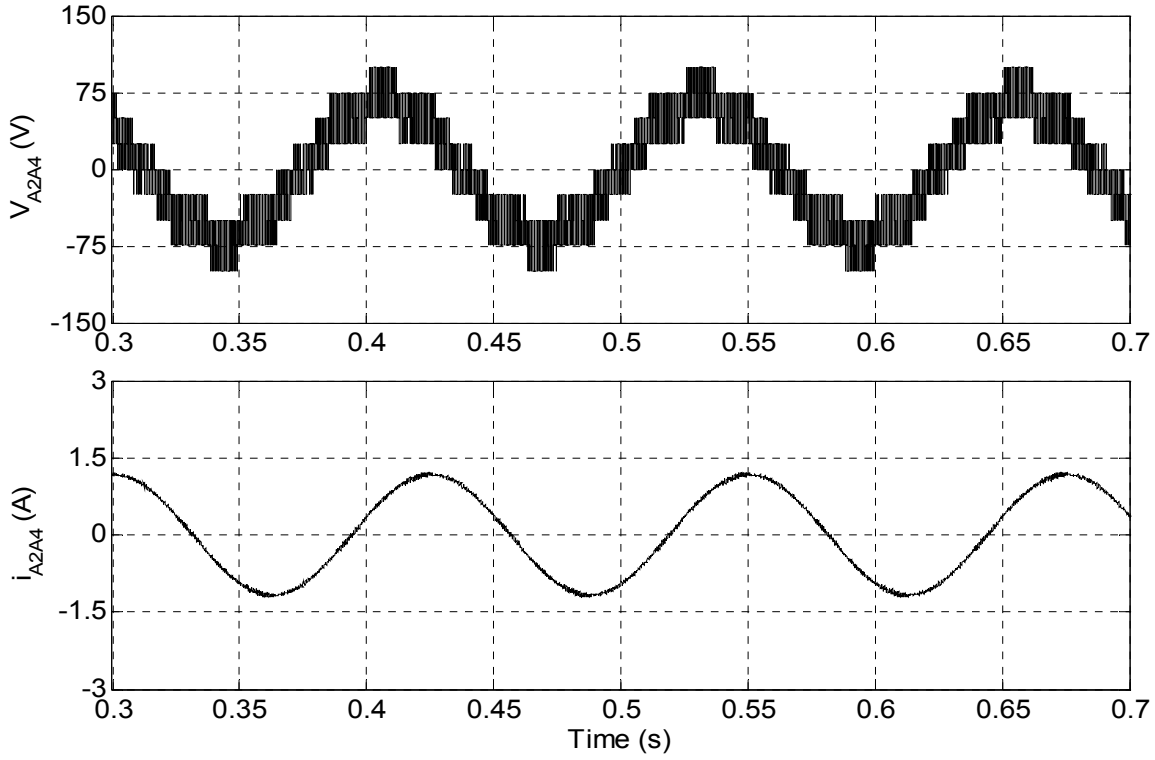



Fig. 4.9: Motor phase-A, voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) of 9-level inverter fed open-end IM drive at no load ($m$=0.16; $f^*_m$ =8Hz; 3-level mode)

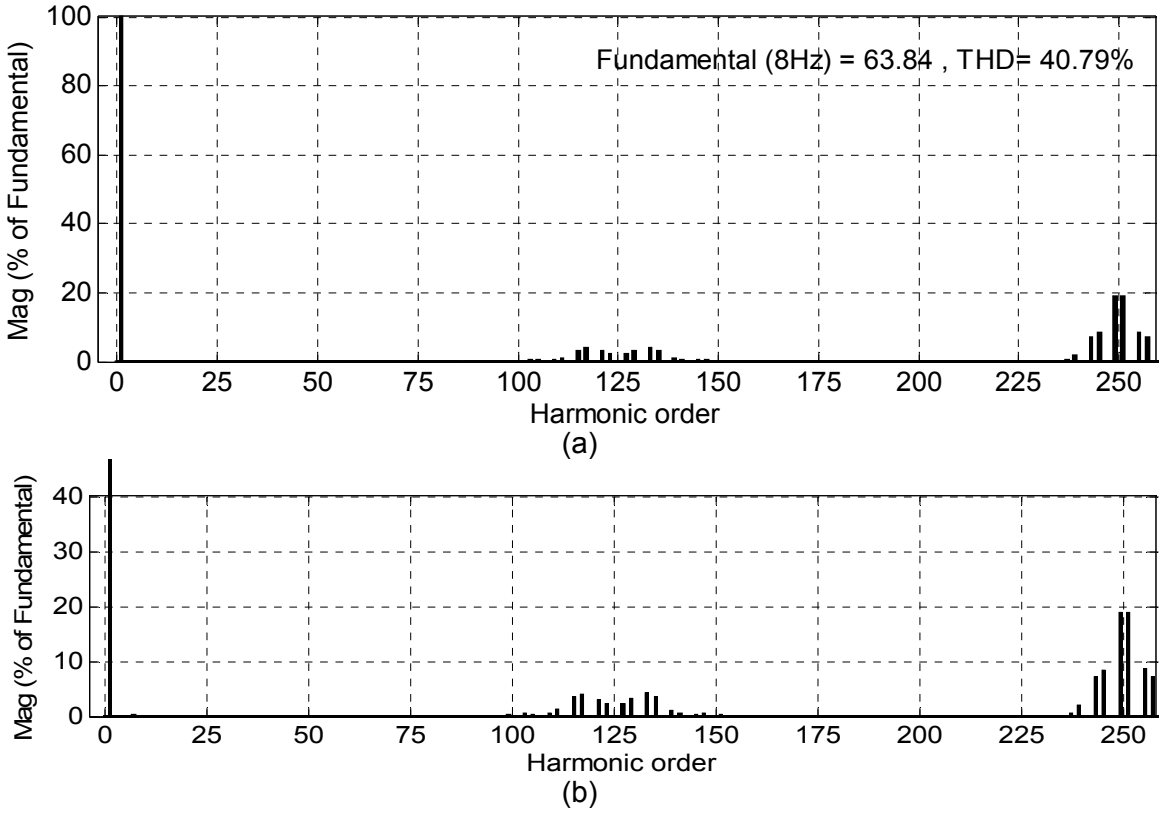



Fig. 4.10: (a) Harmonic spectrum of phase-A voltage ($V_{A2A4}$) at $m$=0.16; $f^*_m$ =8Hz
(b) Zoom view of harmonic spectrum shown in (a)

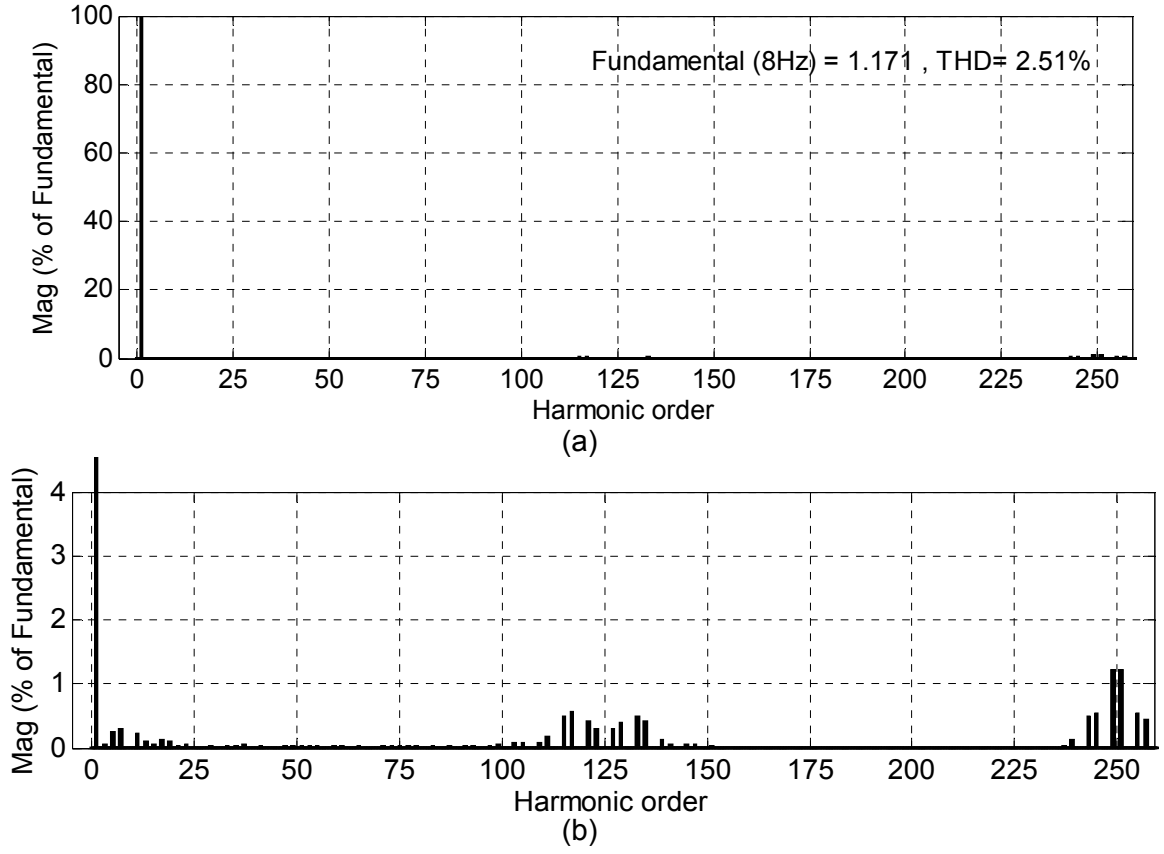



Fig. 4.11: (a) Harmonic spectrum of phase-A current ($i_{A2A4}$) at $m$=0.16; $f^*_m$ =8Hz
(b) Zoom view of harmonic spectrum shown in (a)

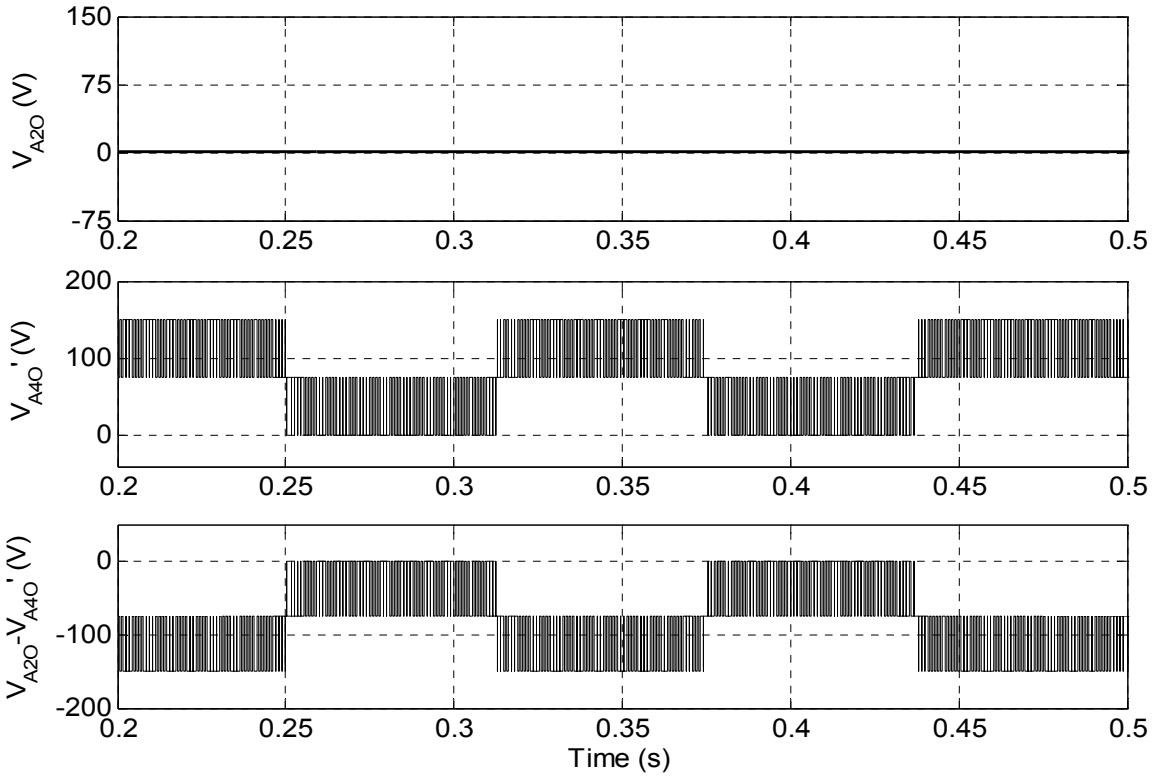



Fig. 4.12 :Top trace; Inverter-A pole voltage ($V_{A2O}$), Middle trace; Inverter-B pole voltage ($V_{A4O'}$), Bottom trace; Difference of Inverter-A and Inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$) at $m$=0.16; $f^*_m$ =8Hz (3-level mode)

The pole-A voltages ($V_{A2O}$ , $V_{A4O'}$) and difference of these pole voltages ($V_{A2O}$ - $V_{A4O'}$) are shown in Fig. 4.12 for 3-level mode of operation. It may be observed from pole voltages waveforms that 3-level inverter-B operates in 3-level mode (0, $V_{DC}$/8 and 2$V_{DC}$/8) while the inverter-A is still clamped at zero voltage level. The difference of pole voltages ($V_{A2O}$ - $V_{A4O'}$) having three distinct voltage levels -(2/8)$V_{DC}$ , -(1/8)$V_{DC}$ and zero confirming the correctness of modified SVPWM scheme.

The simulated motor phase voltage and current for 4-level operation is shown in Fig. 4.13. The value of modulation index $m$ =0.28 and fundamental frequency $f^*_m$ =14Hz. in this range the modulating signals varies in the regions $R_1$ - $R_4$ and inverter operates in 4-level mode of operation. The THD of phase voltage (Fig. 4.14.) and current (Fig. 4.15) are 8.38% and 0.68% respectively and dominant harmonic component occur at the side band of 143$^{rd}$ ($2f_c/f^*_m$ = 2*1000/14) order harmonic. It is depicted from Fig. 4.16 that the difference in pole voltage ($V_{A2O}$ - $V_{A4O'}$) waveform posses four distinct levels -(2/8)$V_{DC}$ , -(1/8)$V_{DC}$ ,0 and +(1/8)$V_{DC}$. It is also evident from pole voltages waveforms that in 4-level mode inverter-A is also started to operate in PWM mode, but only for half of the duration of fundamental cycle and for remaining half cycle it is clamped at zero voltage.

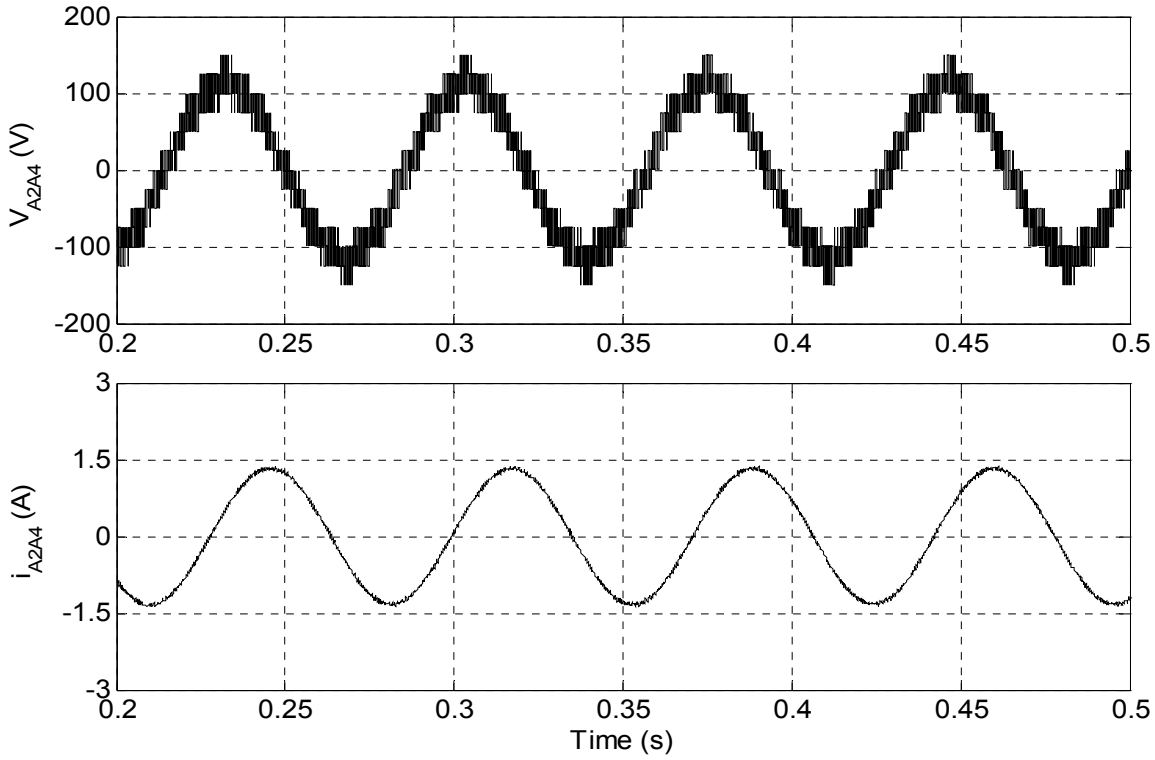



Fig. 4.13: Motor phase-A, voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) of 9-level inverter fed open-end IM drive at no load ($m$=0.28; $f^*_m$ =14Hz; 4-level mode)

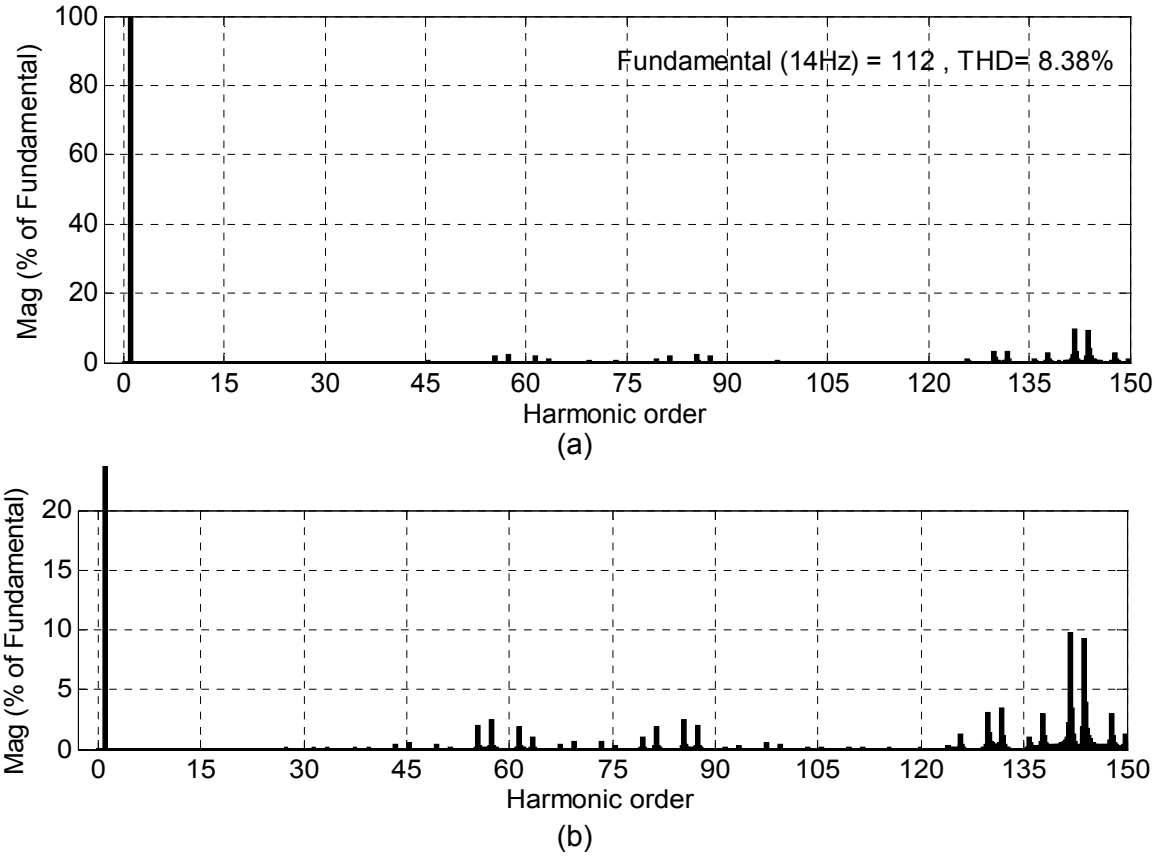



Fig. 4.14: (a) Harmonic spectrum of phase-A voltage ($V_{A2A4}$) at $m$=0.28; $f^*_m$ =14Hz
(b) Zoom view of harmonic spectrum shown in (a)

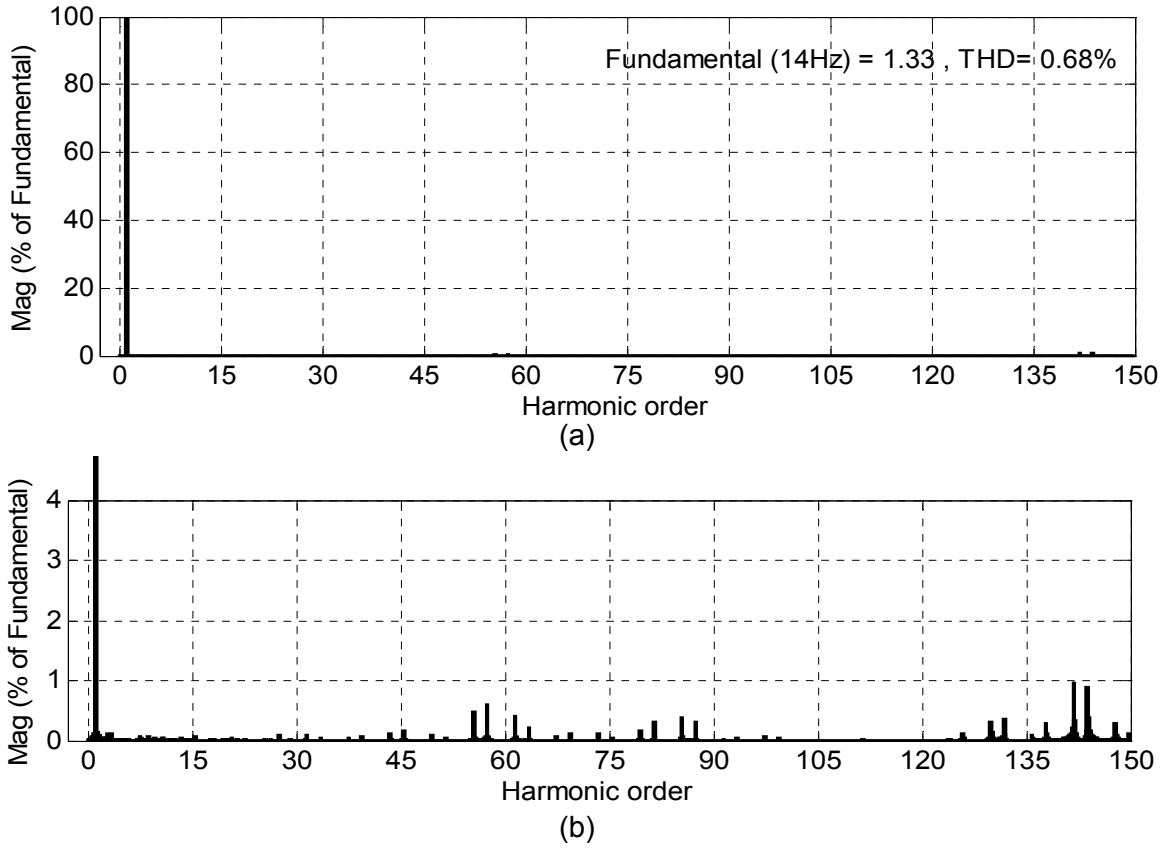



Fig. 4.15: (a) Harmonic spectrum of phase-A current ($i_{A2A4}$) at $m$=0.28; $f^*_m$ =14Hz
(b) Zoom view of harmonic spectrum shown in (a)

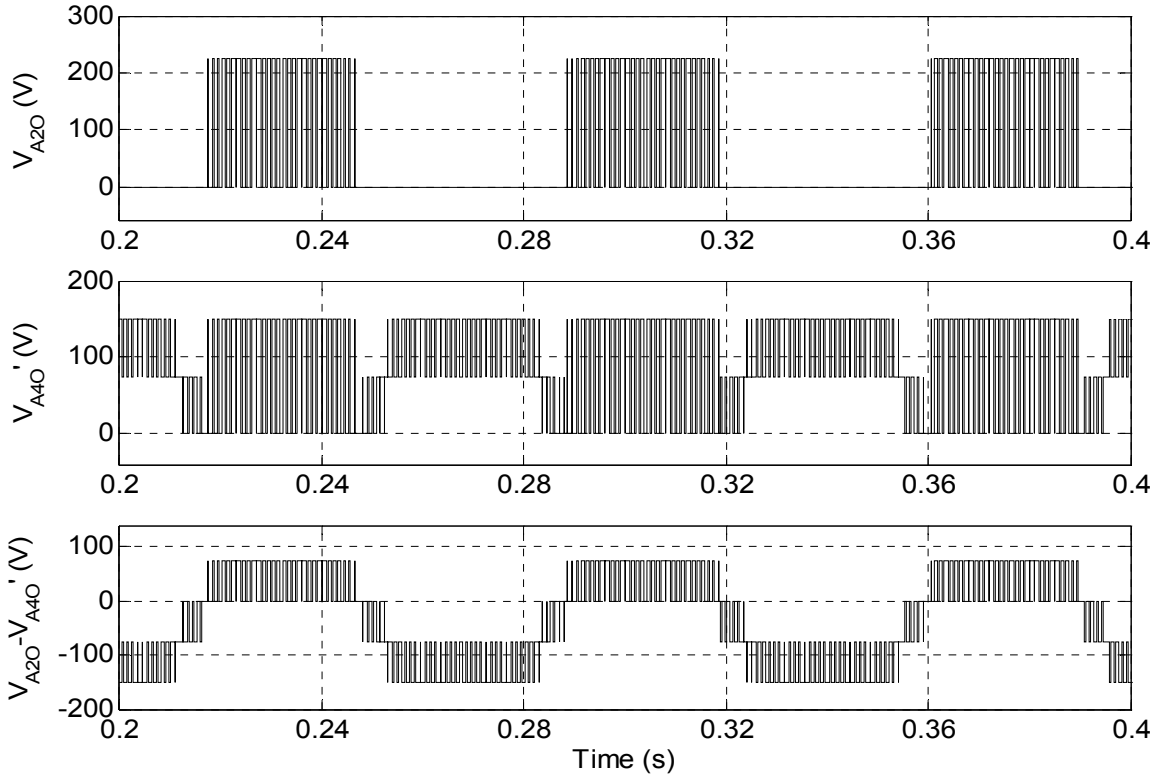



Fig. 4.16 :Top trace; Inverter-A pole voltage ($V_{A2O}$), Middle trace; Inverter-B pole voltage ($V_{A4O'}$), Bottom trace; Difference of Inverter-A and Inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$) at $m$=0.28; $f^*_m$ =14Hz (4-level mode)

Fig. 4.17 through Fig. 4.20 illustrate the simulation results obtain when inverter is operated at modulation index $m$=0.36. In this case the modulating signals lie in regions $R_1$ - $R_5$ and inverter operates in 5-level mode of operation which may be observed in difference of pole voltage ($V_{A2O}$ - $V_{A4O'}$) waveforms shown in Fig. 4.20. The five levels realised in this mode are -(2/8)$V_{DC}$, -(1/8)$V_{DC}$, 0, +(1/8)$V_{DC}$ and +(2/8)$V_{DC}$. In this range of operation 3-level inverter-A operates in two-level mode whereas inverter-B operates in 3-level which can be observed in pole voltage waveforms shown in Fig. 4.20. The phase-A voltage and current are shown in Fig. 4.17. The THD of phase voltage (Fig. 4.18) is further reduce to 6.89% whereas THD of phase current (Fig. 4.19) is only 0.66% of the fundamental frequency ($f^*_m$) which is 18Hz in this mode of operation. The dominant harmonic component occur at the side band of $111^{th}$ ($2f_c/f^*_m$ = 2*1000/18) order.

Simulation results for 6-level mode of operation are shown in Fig. 4.21 - Fig. 4.24. Inverter is operated at modulation index $m$=0.42 and fundamental frequency ($f^*_m$) of 21Hz. In this case the modulating signals cover six regions $R_1$ - $R_6$ results 6-level mode of operation. The phase-A voltage and current are shown in Fig. 4.21. The harmonic spectrum of phase voltage (Fig. 4.22) and current (Fig. 4.23) are further improved and position of occurrence of dominant harmonic is approximately at the side band of $96^{th}$ ($2f_c/f^*_m$ = 2*1000/21) order. It is depicted from pole voltages waveforms shown in Fig. 4.24 that 3-level inverter-A still operates in two-level mode whereas inverter-B attains all the three levels. The six levels realised in this mode are $\pm$(2/8)$V_{DC}$ , $\pm$(1/8)$V_{DC}$ ,0 and +(3/8)$V_{DC}$.

Inverter is operated in 7-level mode of operation at modulation index $m$=0.52 and fundamental frequency ($f^*_m$) of 26Hz. The modulating signals vary from region $R_1$ to $R_7$ and inverter operates in 7-level mode of operation. Motor phase voltage and current are shown in Fig. 4.25. It may be observed in pole voltages waveforms (Fig. 4.28) that in 7-level operation both 3-level inverters operate in 3-level mode and difference of their pole voltage contains seven distinct levels as $\pm$150, $\pm$75, 0, +225 and +300 as depicted in difference of pole voltage ($V_{A2O}$ - $V_{A4O'}$) waveform (Fig. 4.28). As the DC link voltage is 600V therefore these voltage levels correspond to $\pm$(2/8)$V_{DC}$, $\pm$(1/8)$V_{DC}$, 0, +(3/8)$V_{DC}$ and +(4/8)$V_{DC}$. Another important observation can be made from pole voltage waveform that switching occur in inverter-A only for half of the duration of fundamental cycle and for remaining half cycle it is clamped at zero voltage level so effective switching frequency is half of the actual switching frequency. This feature can lead to use of low switching frequency rating power semiconductor devices in the proposed 9-level inverter scheme. The harmonic spectrum of phase voltage is shown in Fig. 4.26. The dominant harmonic component in the spectrum of phase voltage occur approximately at the side band of $77^{th}$ ($2f_c/f^*_m$ = 2*1000/26) order. The harmonic spectrum of phase current shown in Fig. 4.27 and it is found that lower order harmonics are increased in phase current.

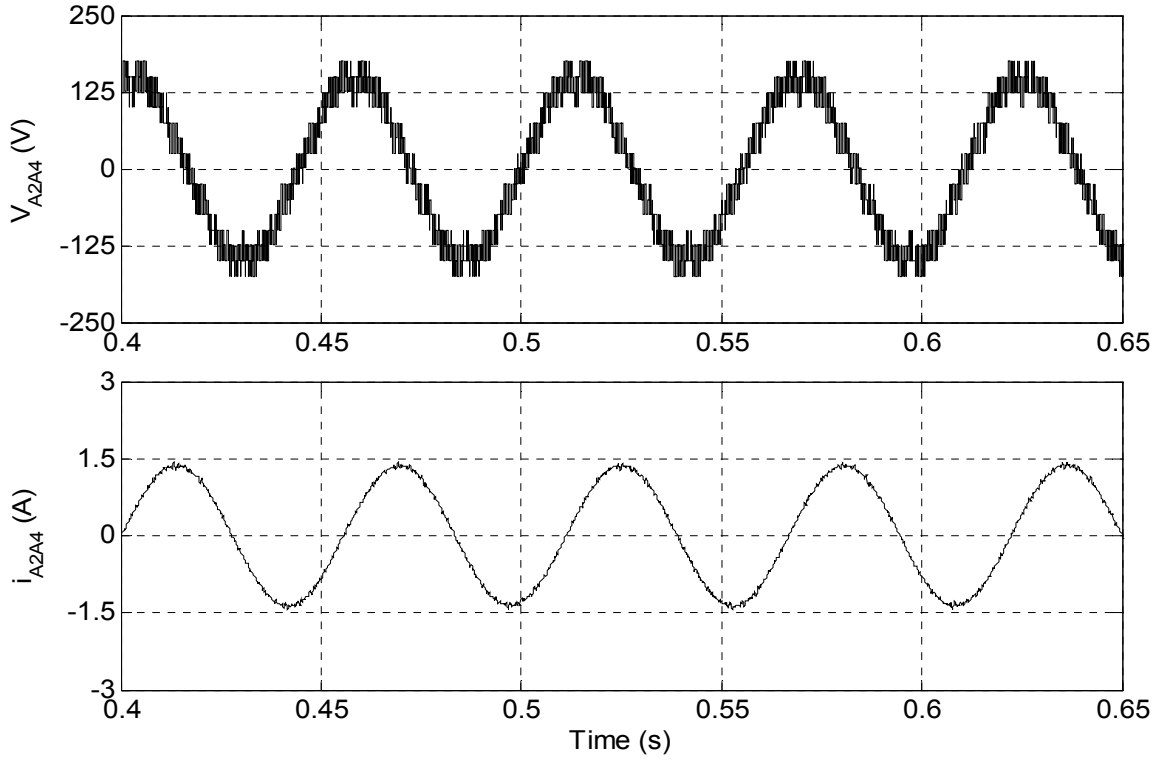



Fig. 4.17: Motor phase-A, voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) of 9-level inverter fed open-end IM drive at no load ($m$=0.36; $f^*_m$ =18Hz; 5-level mode)

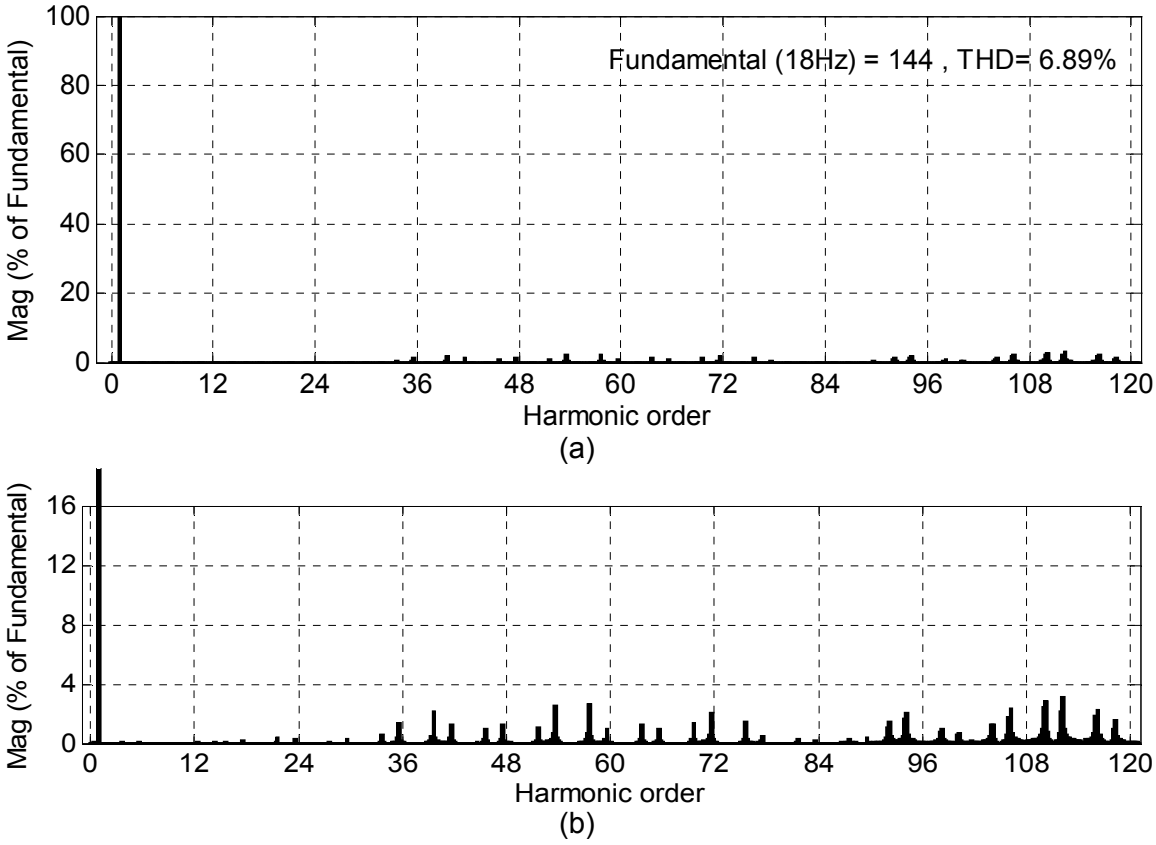



Fig. 4.18: (a) Harmonic spectrum of phase-A voltage ($V_{A2A4}$) at $m$=0.36; $f^*_m$ =18Hz
(b) Zoom view of harmonic spectrum shown in (a)

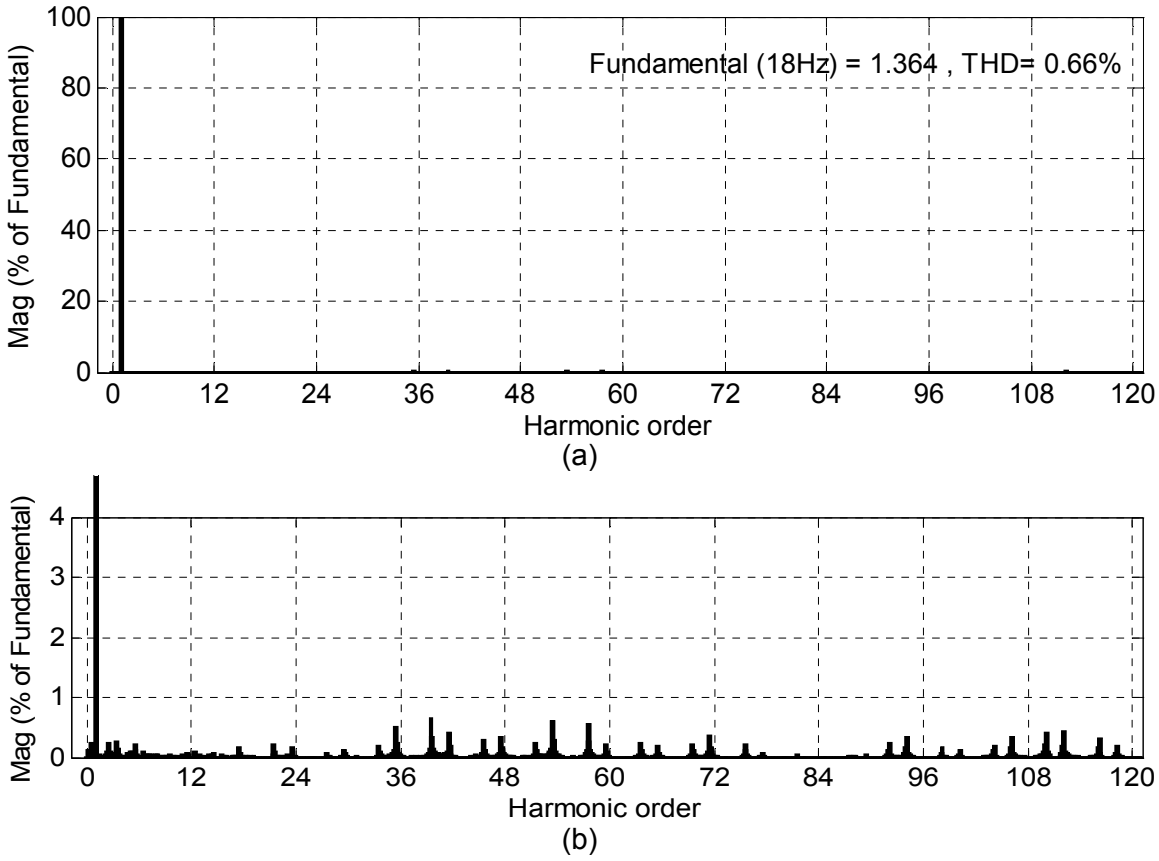



Fig. 4.19: (a) Harmonic spectrum of phase-A current ($i_{A2A4}$) at $m$=0.36; $f^*_m$ =18Hz
(b) Zoom view of harmonic spectrum shown in (a)

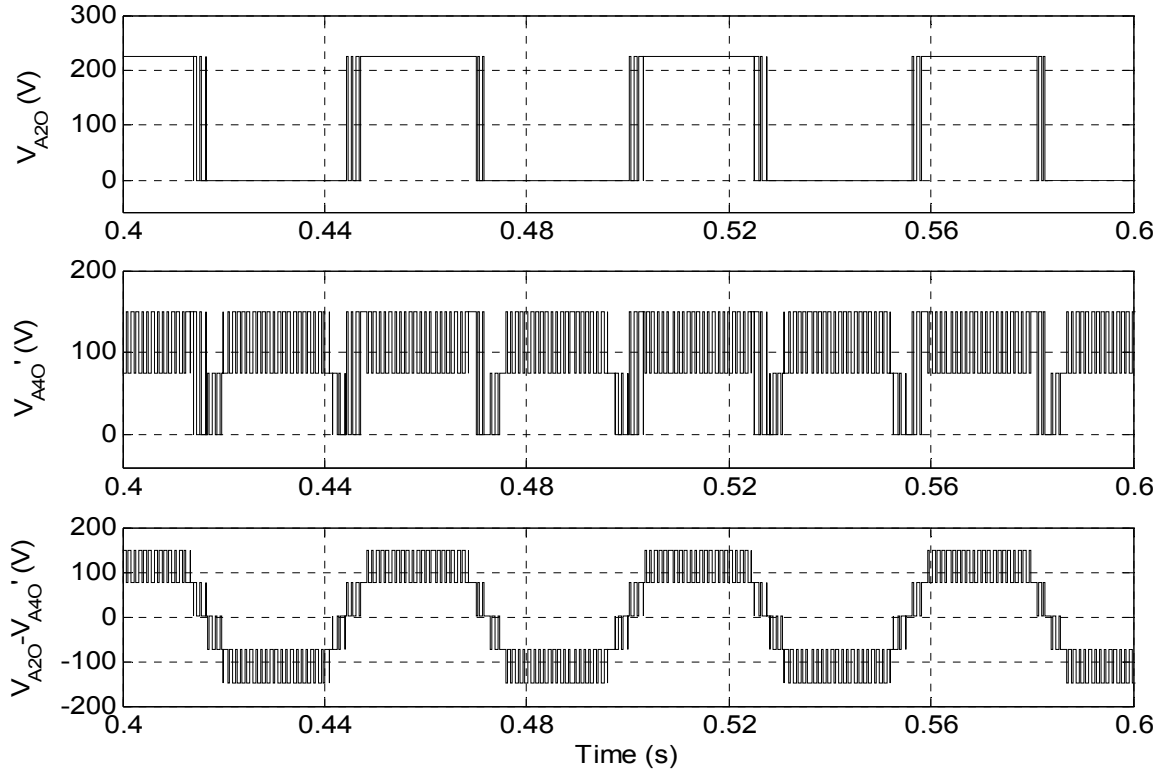



Fig. 4.20 :Top trace; Inverter-A pole voltage ($V_{A2O}$), Middle trace; Inverter-B pole voltage ($V_{A4O'}$), Bottom trace; Difference of Inverter-A and Inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$) at $m$=0.36; $f^*_m$ =18Hz (5-level mode)

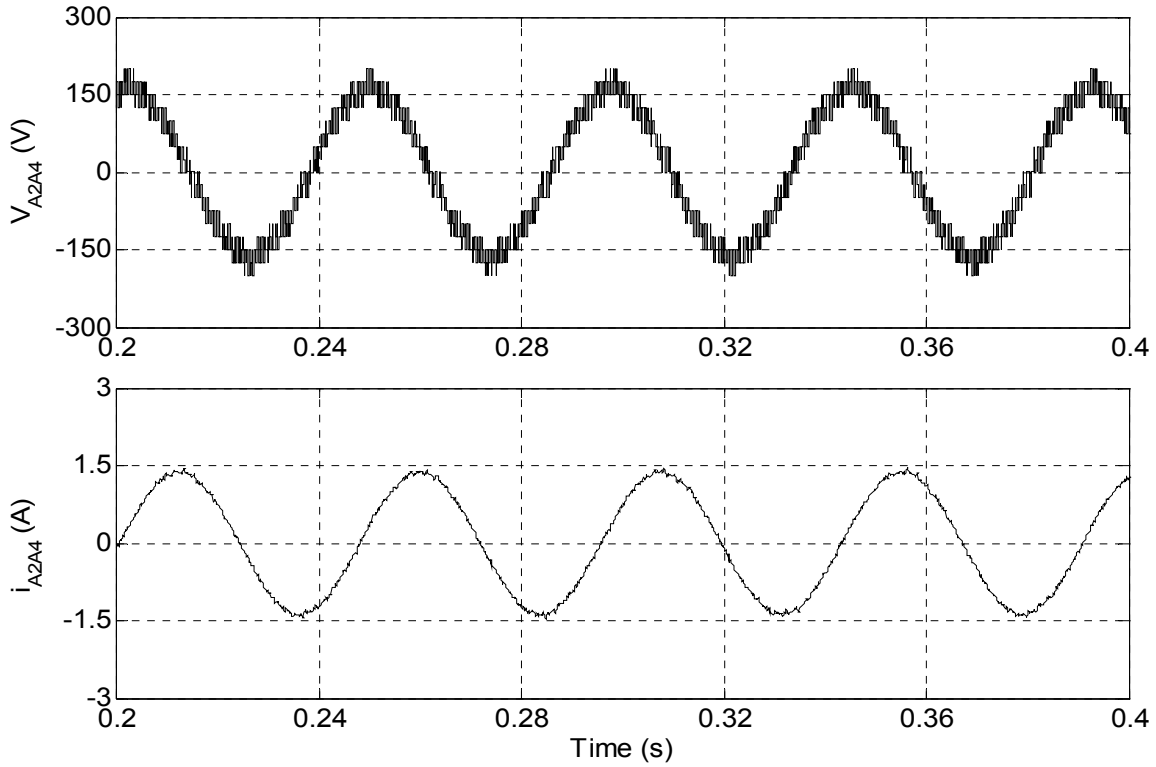



Fig. 4.21: Motor phase-A, voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) of 9-level inverter fed open-end IM drive at no load ($m$=0.42; $f^*_m$ =21Hz; 6-level mode)

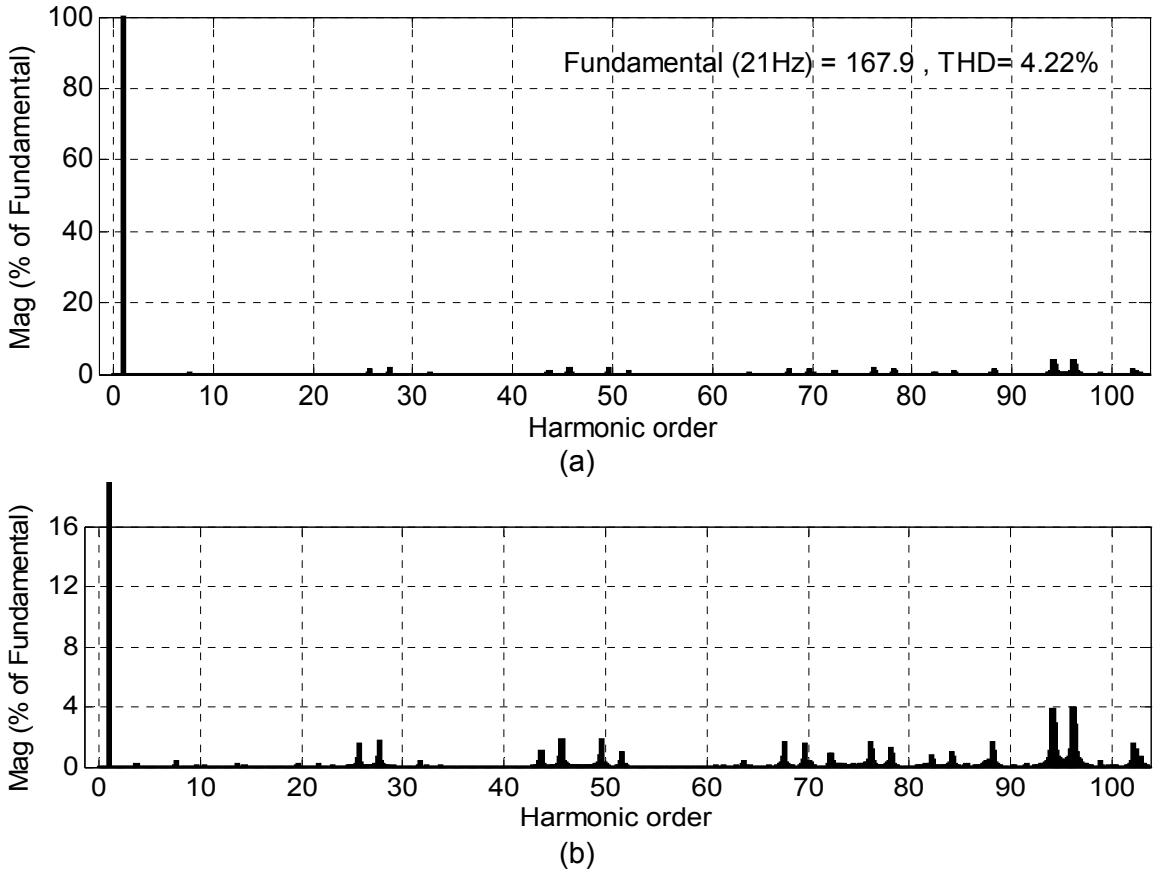



Fig. 4.22: (a) Harmonic spectrum of phase-A voltage ($V_{A2A4}$) at $m$=0.42; $f^*_m$ =21Hz
(b) Zoom view of harmonic spectrum shown in (a)

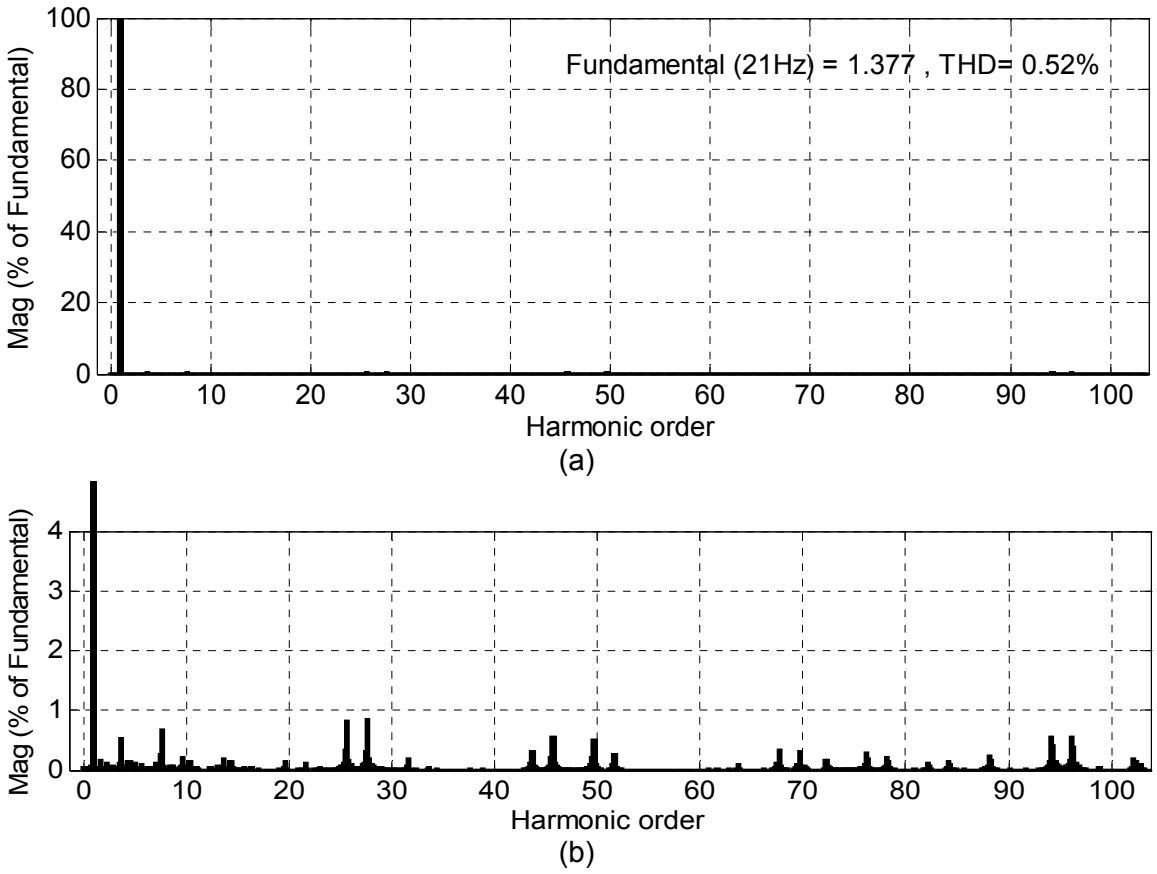



Fig. 4.23: (a) Harmonic spectrum of phase-A current ($i_{A2A4}$) at $m$=0.42; $f^*_m$ =21Hz
(b) Zoom view of harmonic spectrum shown in (a)

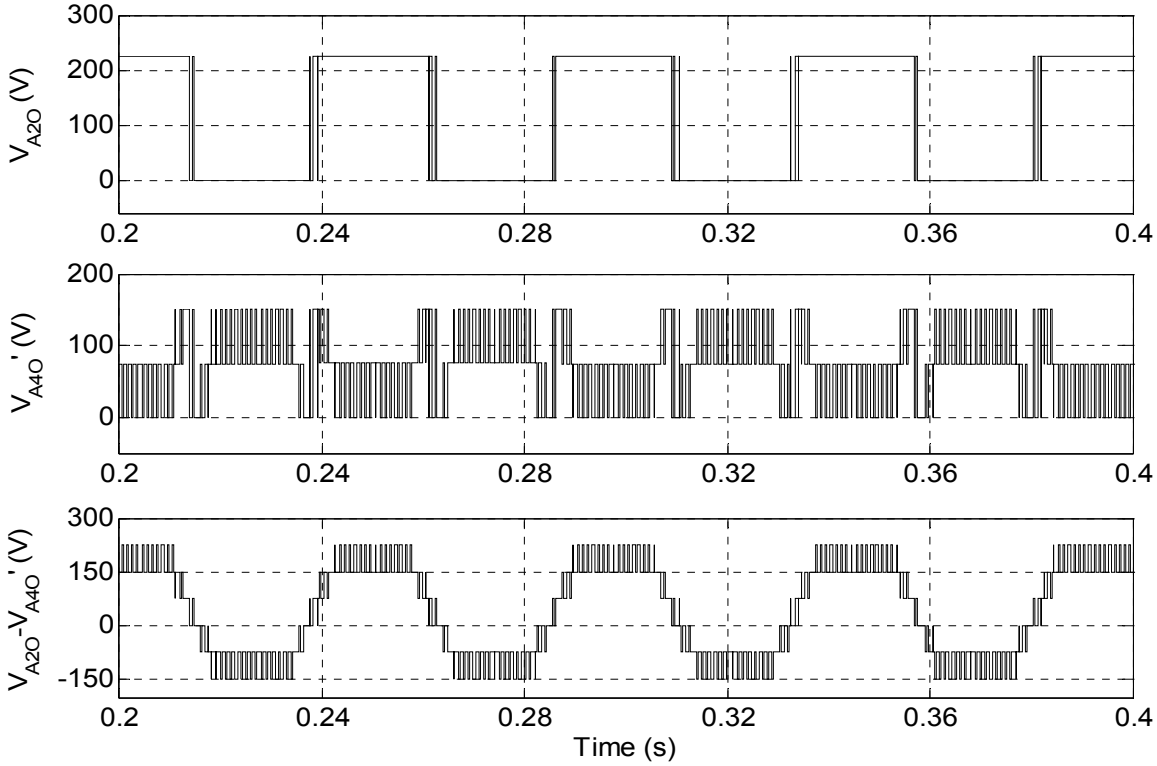



Fig. 4.24 :Top trace; Inverter-A pole voltage ($V_{A2O}$), Middle trace; Inverter-B pole voltage ($V_{A4O'}$), Bottom trace; Difference of Inverter-A and Inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$) at $m$=0.42; $f^*_m$ =21Hz (6-level mode)

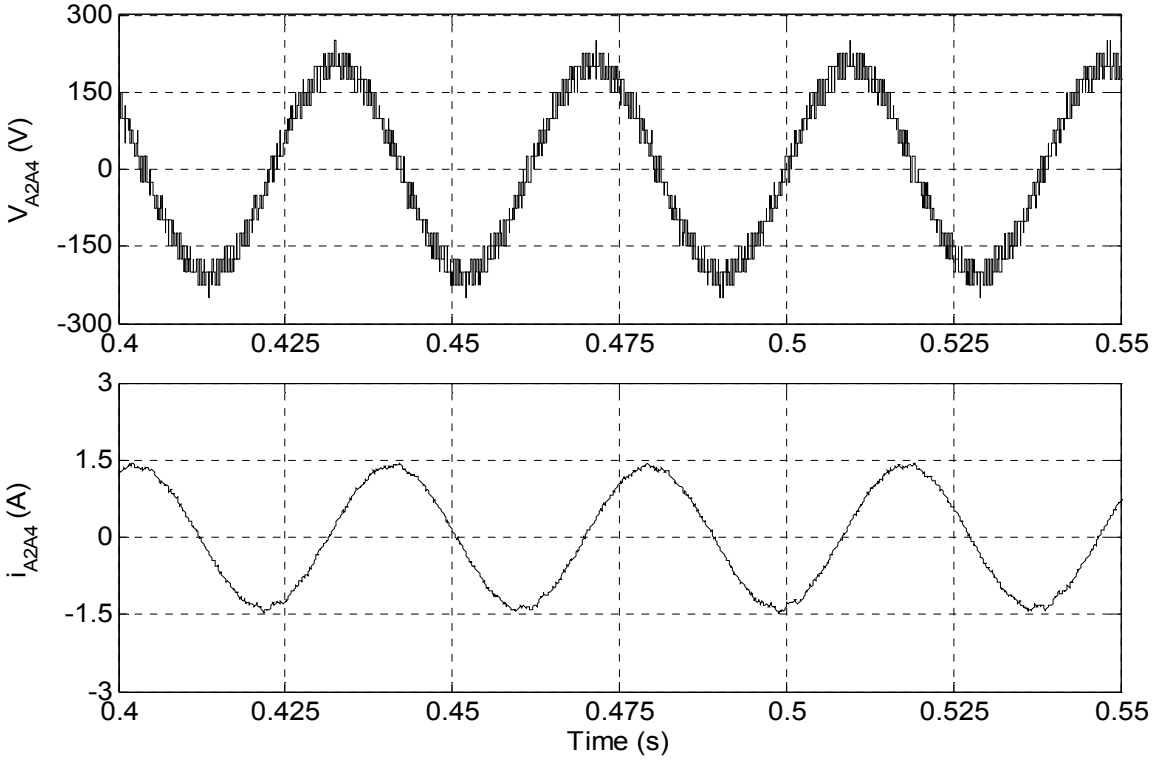



Fig. 4.25: Motor phase-A, voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) of 9-level inverter fed open-end IM drive at no load ($m$=0.52; $f^*_m$ =26Hz; 7-level mode)

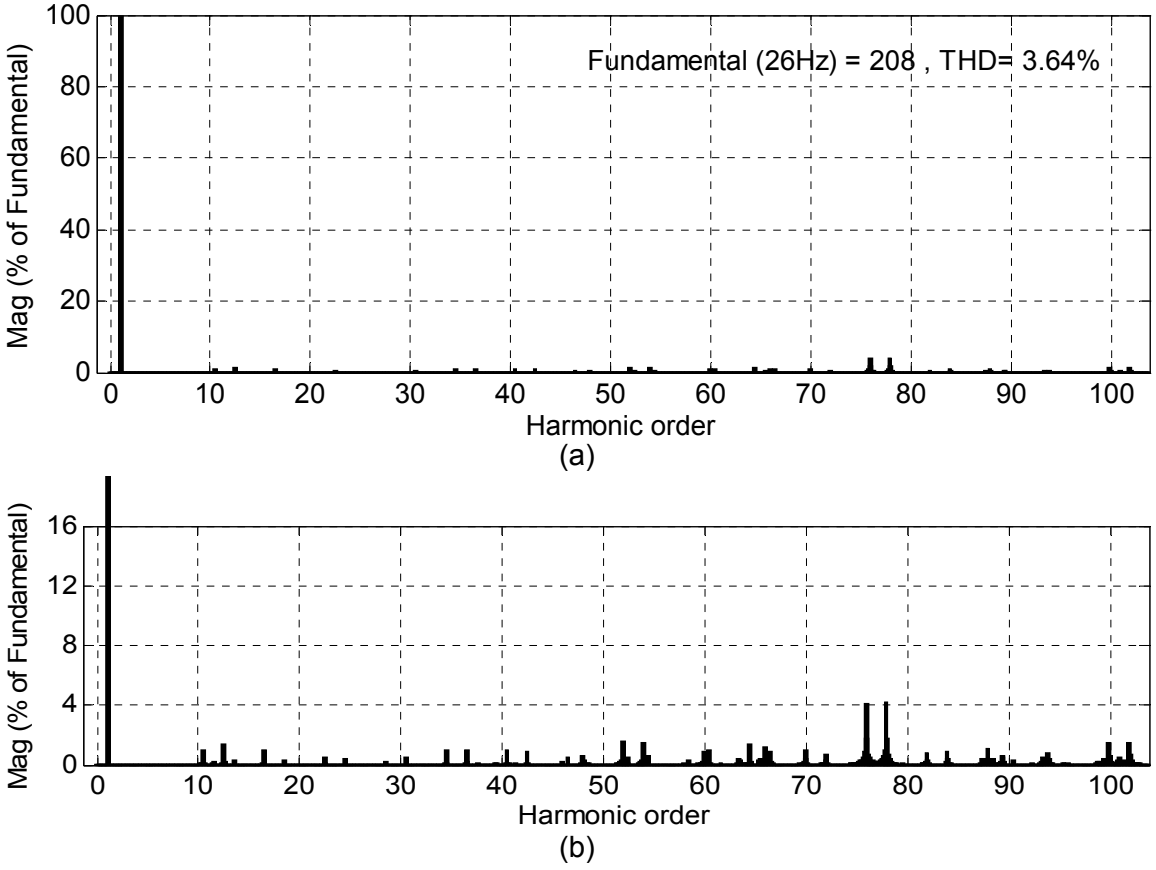



Fig. 4.26: (a) Harmonic spectrum of phase-A voltage ($V_{A2A4}$) at $m$=0.52; $f^*_m$ =26Hz
(b) Zoom view of harmonic spectrum shown in (a)

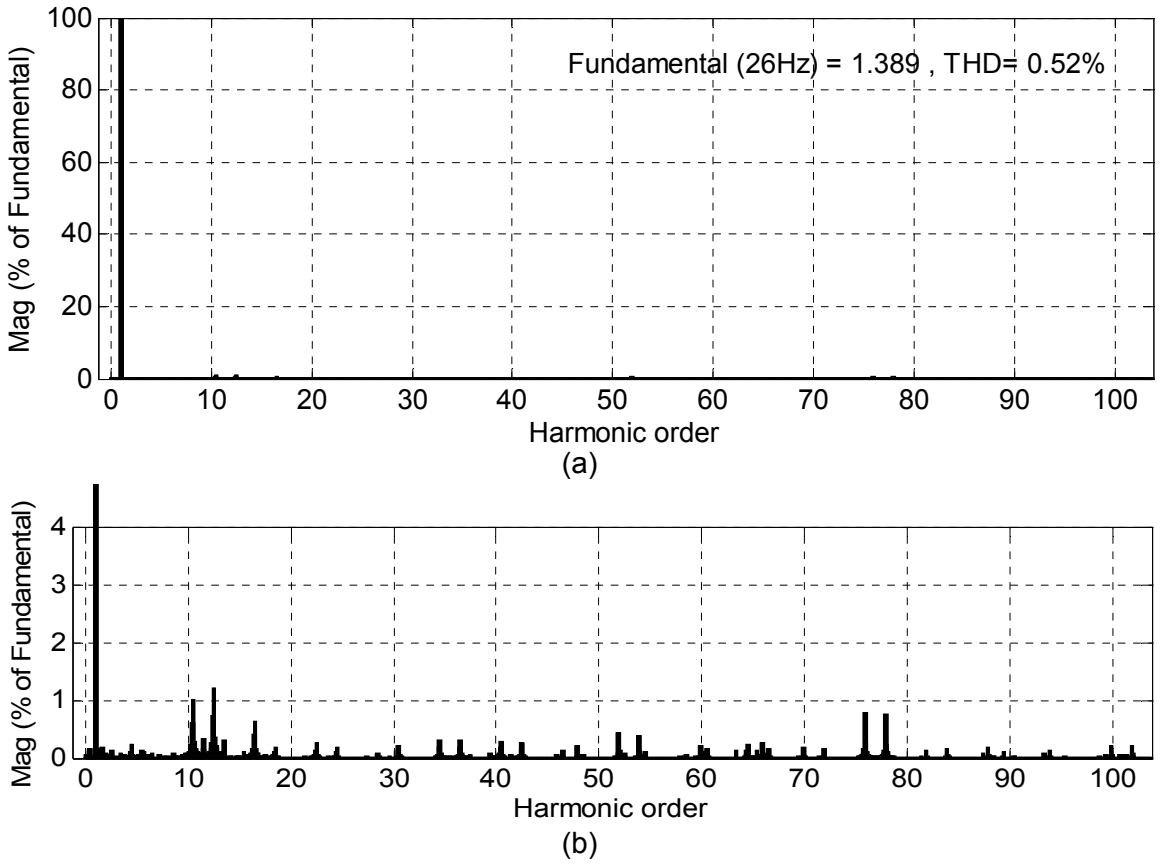



Fig. 4.27: (a) Harmonic spectrum of phase-A current ($i_{A2A4}$) at $m$=0.52; $f^*_m$ =26Hz
(b) Zoom view of harmonic spectrum shown in (a)

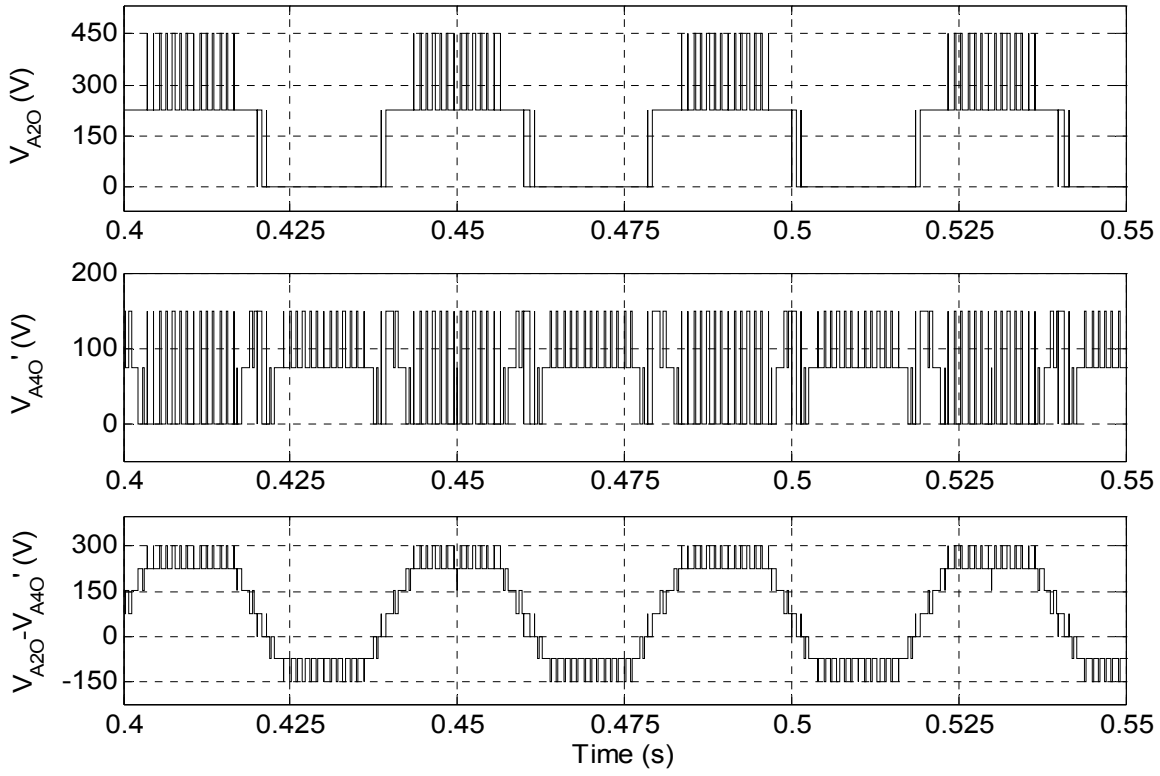



Fig. 4.28 :Top trace; Inverter-A pole voltage ($V_{A2O}$), Middle trace; Inverter-B pole voltage ($V_{A4O'}$), Bottom trace; Difference of Inverter-A and Inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$) at $m$=0.52; $f^*_m$ =26Hz (7-level mode)

Fig. 4.29 through Fig. 4.32 illustrate the simulated results obtained when inverter is operated at modulation index $m$=0.64. All the three modulating waves reside in regions $R_1$ - $R_8$ at this modulation index so inverter operates as 8-level inverter. The motor operates at fundamental frequency $f^*_m$=32Hz. The Motor phase voltage and current waveforms shown in Fig. 4.29 are further refine and approach towards sinusoidal. Inverter-A pole voltage switch between 3-levels 0, $3V_{DC}/8$ and 6 $V_{DC}/8$ (0, 225 and 450) as shown in pole voltage waveform (Fig. 4.32). Similarly Inverter-B also operates in 3-level mode (Fig. 4.32 middle trace) and give the pole voltage 0, 75 and 150 correspond to 0, $V_{DC}/8$ and $2V_{DC}/8$ ($V_{DC}$ =600V). The difference pole voltages (Fig. 4.32 bottom trace) contains eight distinct voltage levels as $\pm$150, $\pm$75, 0, +225, +300 and +375 corresponding to the levels $\pm(2/8)V_{DC,}$ $\pm(1/8)V_{DC}$, 0, $+(3/8)V_{DC}$, $+(4/8)V_{DC}$ and $+(5/8)V_{DC}$. The harmonic spectrum of phase voltage is further improved with the THD of 3.21% and dominant harmonic component is shifted towards the side band of 63$^{rd}$ ($2f_c/f^*_m$ = 2*1000/32) order as shown in Fig. 4.30. The harmonic spectrum of phase current is shown in Fig. 4.31; and it can be seen that at this modulation index lower order harmonics of current are increased.

Similar types of results are obtained for the modulation index $m$=0.8 correspond to 9-level mode of operation. Motor runs at fundamental frequency $f^*_m$=40Hz. The range of modulating signals vary from region $R_1$ - $R_9$ and nine levels are applied across the motor phase winding. The simulated phase voltage and current waveforms are shown in Fig. 4.33. Although the pole voltages waveforms (Fig. 4.36) having same voltage levels as they posses in the 8-level mode, but their difference (Fig. 4.36 bottom trace) is having one more level, which is +450 correspond to voltage level of $+(6/8)V_{DC}$, so total 9-levels are obtained. It is evident in this mode also that inverter-A which operate at higher DC link voltage switched only for half of the duration of fundamental cycle hence less switching losses occur in two-level inverter-1 and inverter-2. The harmonic spectrums of phase voltage and current are presented in Fig. 4.34 and Fig. 4.35 respectively.

The proposed drive system is also investigated against transient state stability by sudden changeover from two-level mode of operation to 9-level mode of operation and vice-versa. Fig. 4.37(a) shows the motor phase-A voltage ($V_{A2A4}$) and current ($i_{A2A4}$) during sudden change from two-level to 9-level mode of operation. The changeover from lower to higher level operation takes place smoothly and drive attains its steady state in 0.457 second. The similar observation can also be made from Fig. 4.37(b) which shows the motor phase-A voltage ($V_{A2A4}$) and current ($i_{A2A4}$) during sudden change in operation from 9-level to two-level mode. In this case also changeover takes place very smoothly and drive attains its steady state in 0.608 second.

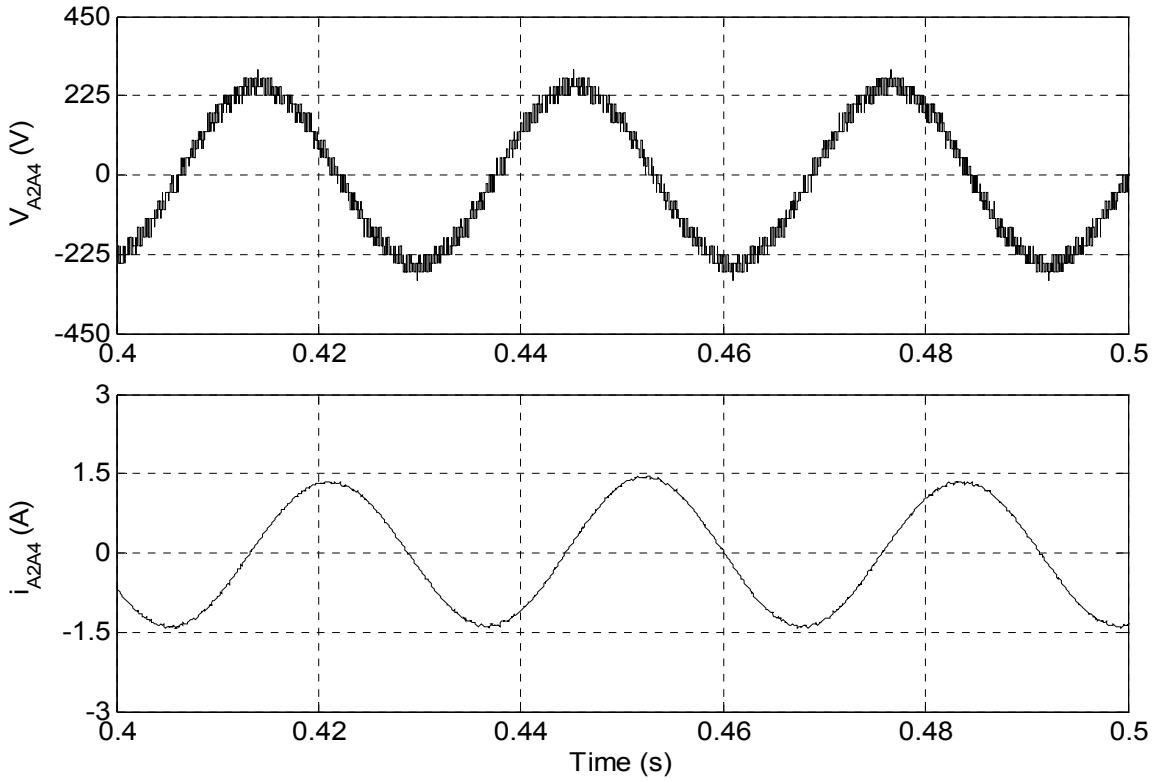



Fig. 4.29: Motor phase-A, voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) of 9-level inverter fed open-end IM drive at no load ($m$=0.64; $f^*_m$ =32Hz; 8-level mode )

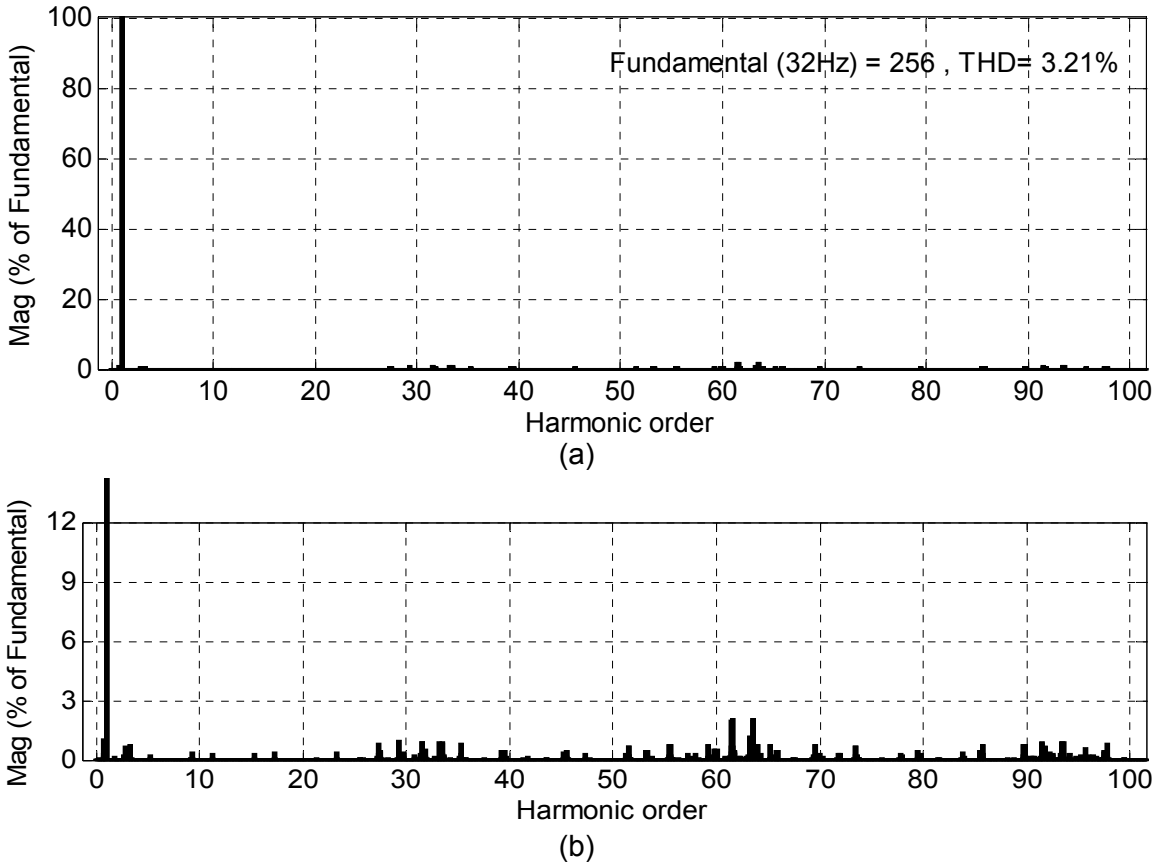



Fig. 4.30: (a) Harmonic spectrum of phase-A voltage ($V_{A2A4}$) at $m$=0.64; $f^*_m$ =32Hz
(b) Zoom view of harmonic spectrum shown in (a)

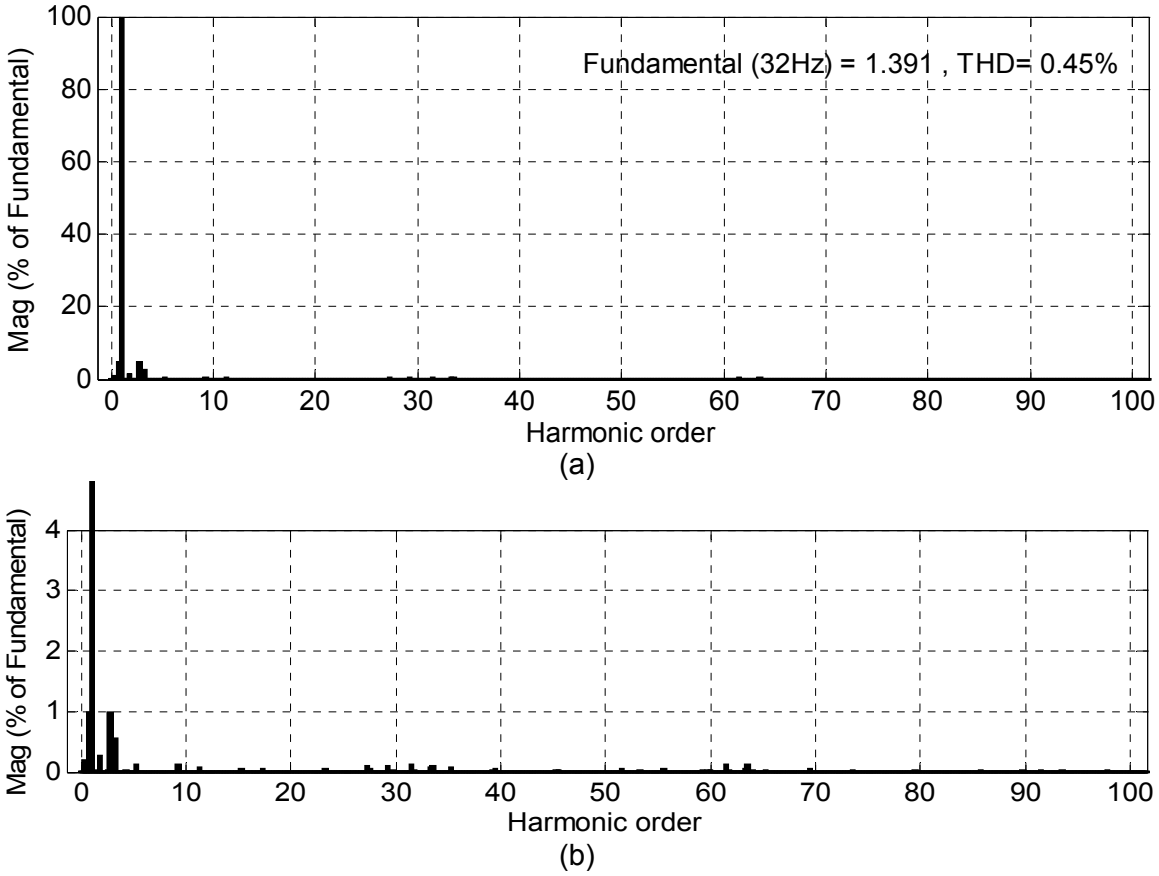



Fig. 4.31: (a) Harmonic spectrum of phase-A current ($i_{A2A4}$) at $m$=0.64; $f^*_m$ =32Hz
(b) Zoom view of harmonic spectrum shown in (a)

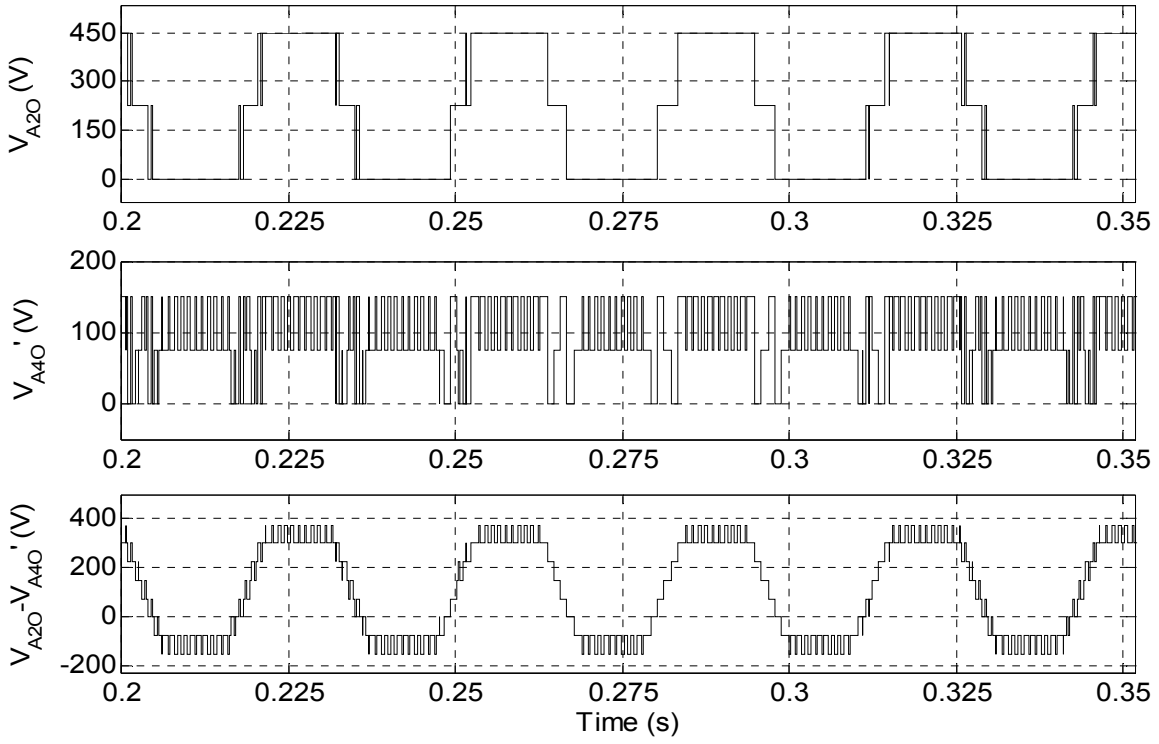



Fig. 4.32 :Top trace; Inverter-A pole voltage ($V_{A2O}$), Middle trace; Inverter-B pole voltage ($V_{A4O'}$), Bottom trace; Difference of Inverter-A and Inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$) at $m$=0.64; $f^*_m$ =32Hz (8-level mode)

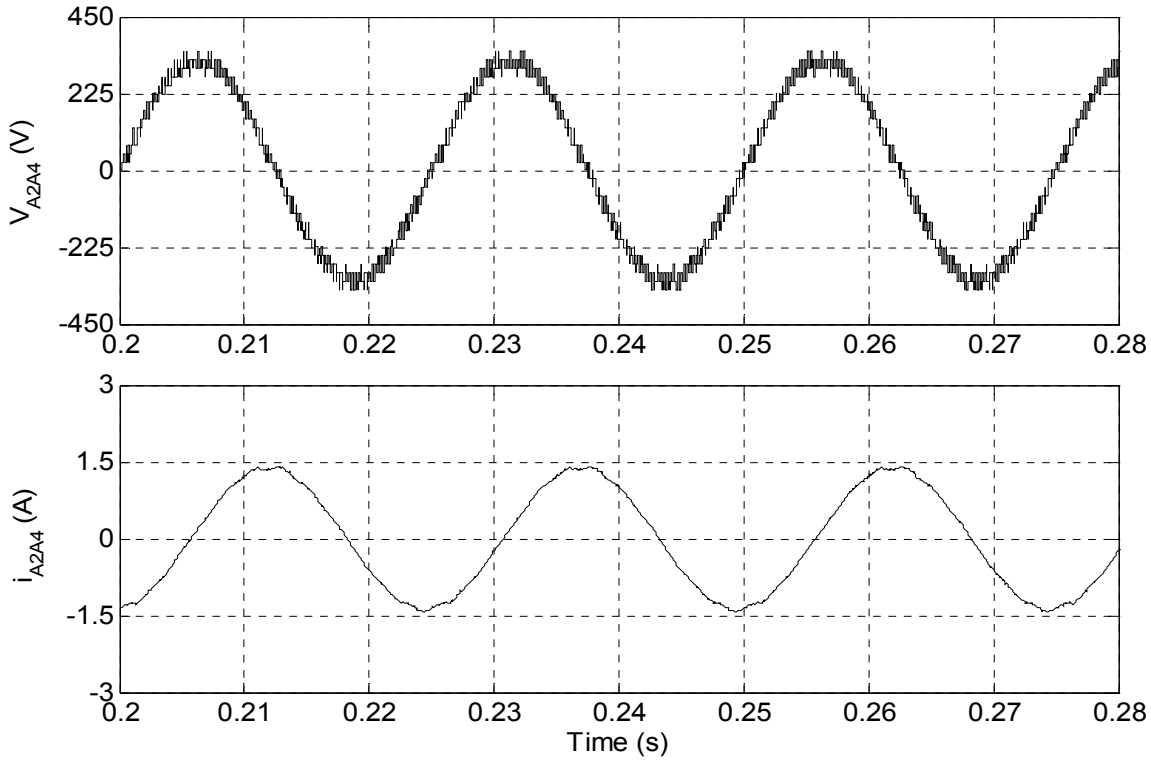



Fig. 4.33: Motor phase-A, voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) of 9-level inverter fed open-end IM drive at no load ($m$=0.8; $f^*_m$ =40Hz; 9-level mode )

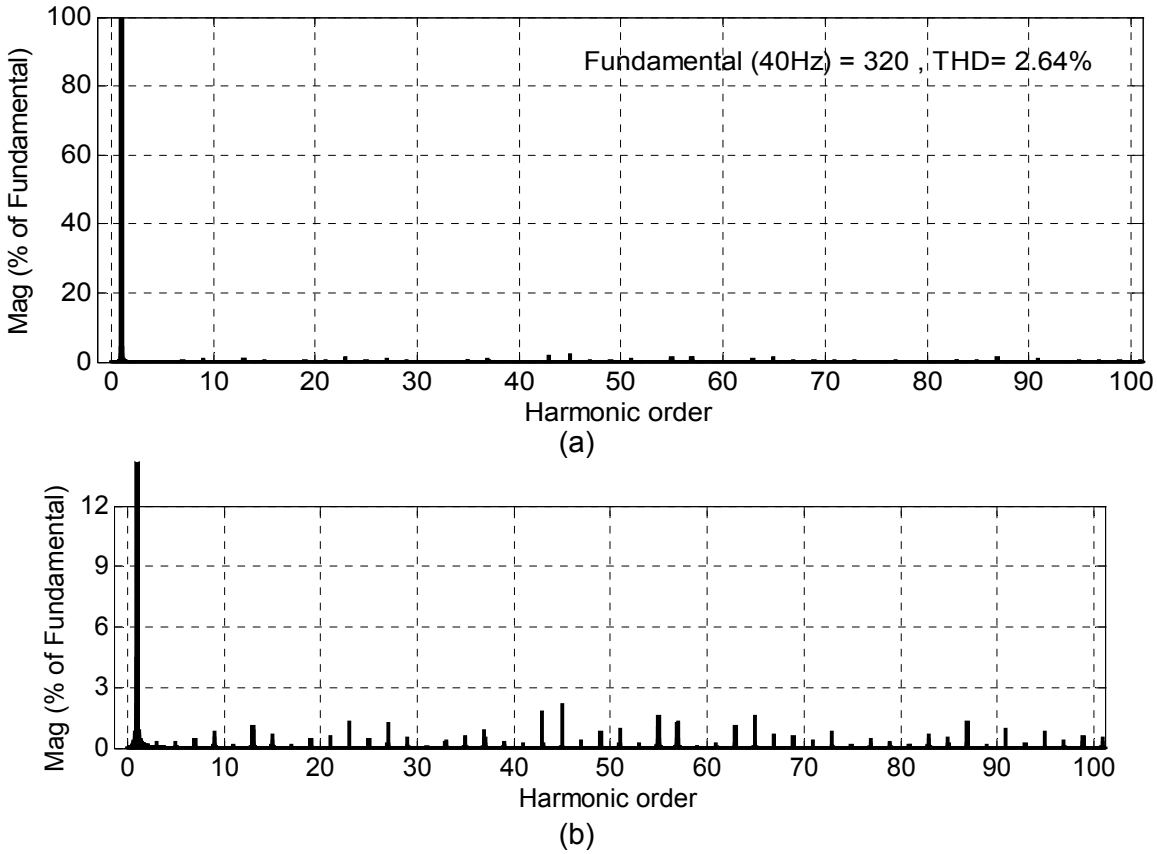



Fig. 4.34: (a) Harmonic spectrum of phase-A voltage ($V_{A2A4}$) at $m$=0.8; $f^*_m$ =40Hz
(b) Zoom view of harmonic spectrum shown in (a)

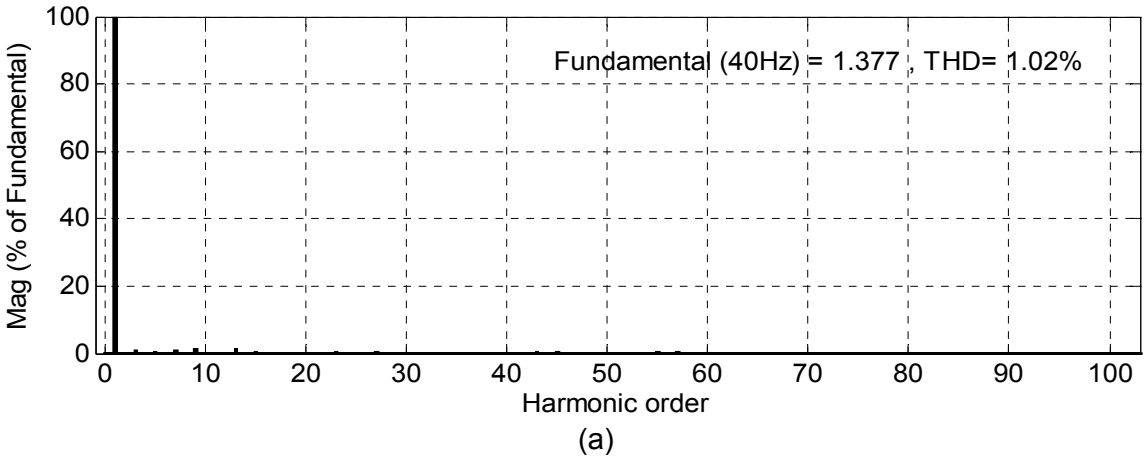



Fig. 4.35: (a) Harmonic spectrum of phase-A current ($i_{A2A4}$) at $m$=0.8; $f^*_m$ =40Hz
(b) Zoom view of harmonic spectrum shown in (a)

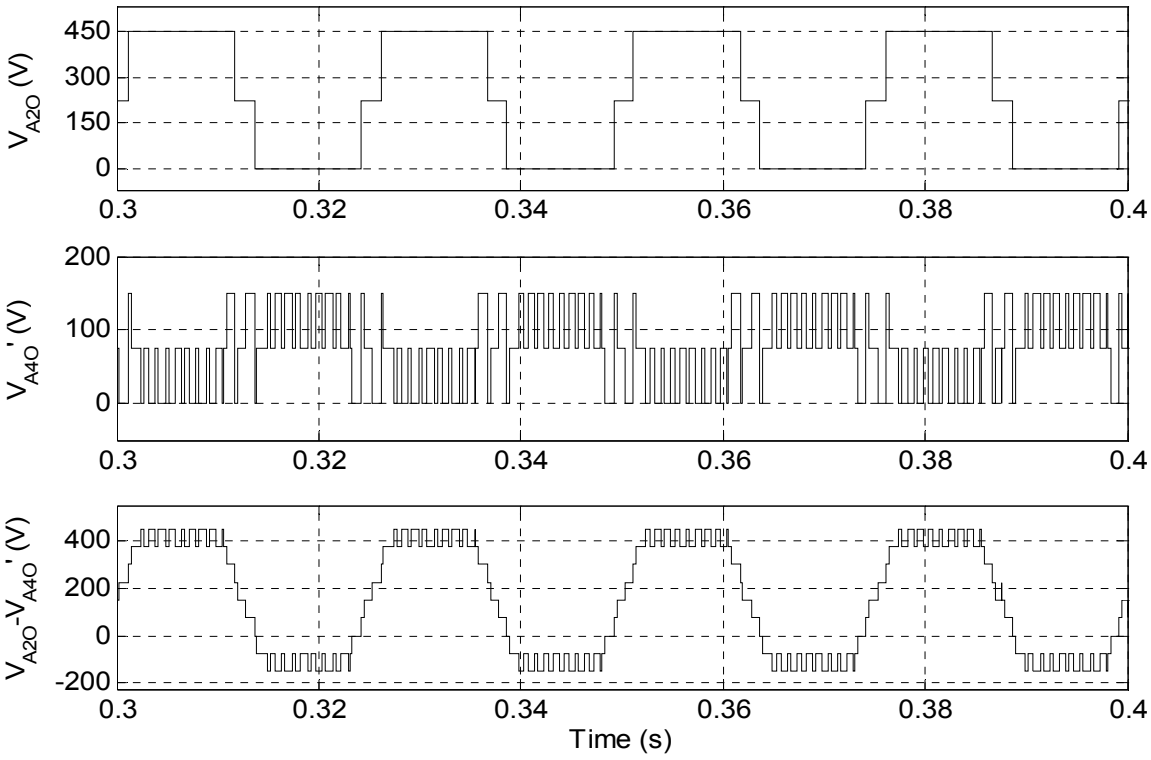
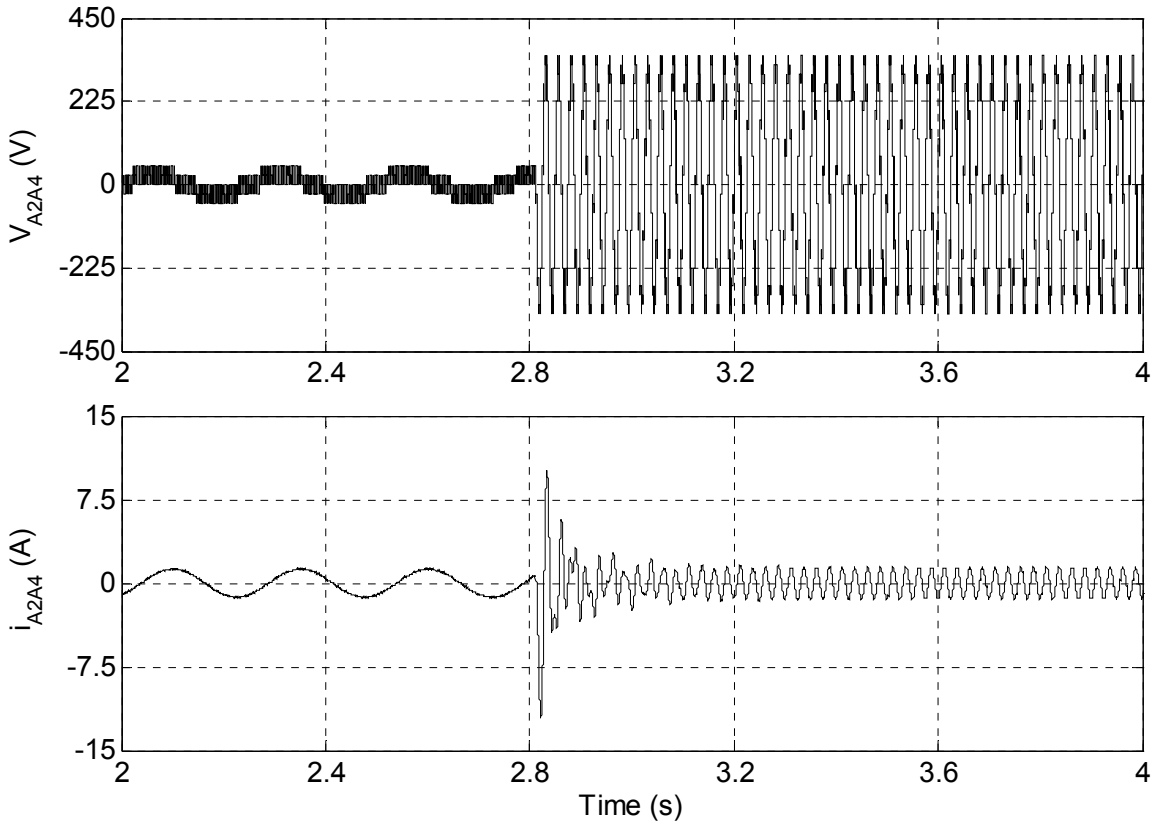
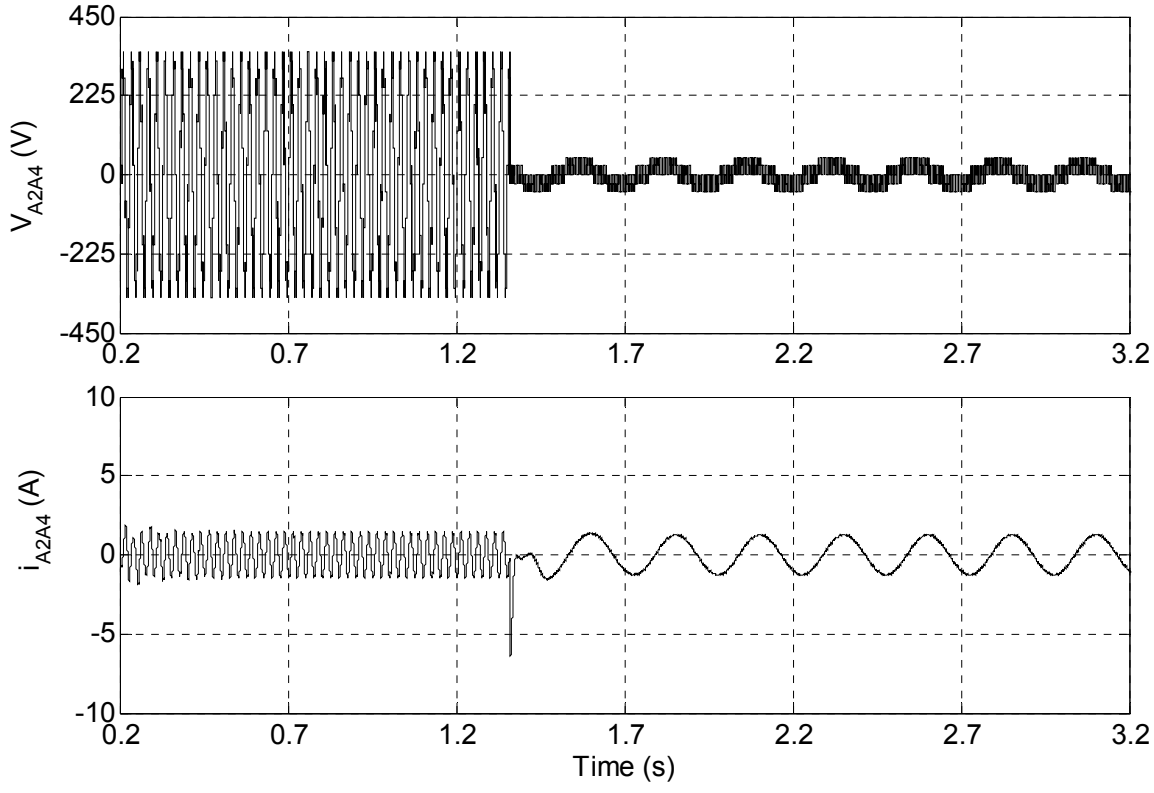



Fig. 4.36 :Top trace; Inverter-A pole voltage ($V_{A2O}$), Middle trace; Inverter-B pole voltage ($V_{A4O'}$), Bottom trace; Difference of Inverter-A and Inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$) at $m$=0.8; $f^*_m$ =40Hz (9-level mode)




(a)




(b)

Fig. 4.37: (a) Motor phase-A voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) waveforms under sudden change in operation from two-level to 9-level at no-load (b) Motor phase-A voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) waveforms under sudden change in operation from 9-level to two-level at no-load

Table 4.5 summarized the simulation results obtained at different modulation indices. From the analysis of simulation results, it may be concluded that the proposed 9-level inverter is capable of rendering a good performance with the modified SVPWM technique.

Table 4.5: Summary of simulation results of 9-level inverter obtained at different modulation indices

| Performance parameter | Modulation index(*m*) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 0.08 | 0.16 | 0.28 | 0.36 | 0.42 | 0.52 | 0.64 | 0.8 |
| Level of operation | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| RMS of phase-A voltage (*V*) | 29.76 | 48.75 | 81.34 | 103.4 | 120.1 | 148.2 | 183.3 | 227.3 |
| RMS of phase-A current (*A*) | 0.591 | 0.829 | 0.939 | 0.964 | 0.975 | 0.981 | 0.982 | 0.985 |
| Frequency of phase voltage (*Hz)* | 4 | 8 | 14 | 18 | 21 | 26 | 32 | 40 |
| THD of phase-A voltage in % | 84.73 | 40.79 | 8.38 | 6.89 | 4.22 | 3.64 | 3.21 | 2.64 |
| Order of dominant voltage harmonic (amplitude in %) | 500±1 (37.2) | 250±1 (18.1) | 142±2 (9.1) | 111±2 (3.6) | 95±2 (4.0) | 77±2 (4.1) | 63±2 (1.85) | 45 (2.1) |
| THD of phase-A Current in % | 4.0 | 2.51 | 0.68 | 0.66 | 0.52 | 0.52 | 0.45 | 1.02 |
| Order of dominant current harmonic (amplitude in %) | 500±1 (1.82) | 250±1 (1.19) | 142±2 (0.9) | 39 (0.64) | 27 (0.75) | 13 (1.18) | 3 (1.0) | 9 &13 (1.10) |
| Settling time for Changeover from 2-level to 9-level in sec. | 0.457 | | | | | | | |
| Settling time for Changeover from 9-level to 2-level in sec. | 0.608 | | | | | | | |
| Sampling time | 10 μSecond | | | | | | | |

### 4.6 Performance Comparison

The performance of proposed 9-level inverter is compared with 5-level inverter presented in Chapter-3, by operating an open-end winding induction motor at no-load under different modulation indices and simulation results are tabulated in Table 4.6. It can be concluded from the simulation results that proposed 9-level inverter gives better performance in terms of voltage and current harmonic spectra as compared to 5-level inverter.

Table 4.6: Performance comparison of 9-level inverter with 5-level inverter

| Performance parameter | Type of inverter | Modulation index(*m*) | | | | |
|---|---|---|---|---|---|---|
| | | 0.1 | 0.2 | 0.4 | 0.5 | 0.8 |
| Level of operation | 9-level inverter | 3 | 4 | 6 | 7 | 9 |
| | 5-level inverter | 2 | 3 | 4 | 4 | 5 |
| RMS of phase-A voltage (*V*) | 9-level inverter | 33.23 | 59.41 | 114.7 | 142.8 | 227.3 |
| | 5-level inverter | 49.97 | 66.41 | 118.8 | 145.6 | 229.3 |
| RMS of phase-A current (*A*) | 9-level inverter | 0.676 | 0.885 | 0.972 | 0.983 | 0.985 |
| | 5-level inverter | 0.677 | 0.886 | 0.977 | 0.991 | 0.998 |
| Frequency of phase voltage (*Hz)* | 9-level inverter | 5 | 10 | 20 | 25 | 40 |
| | 5-level inverter | 5 | 10 | 20 | 25 | 40 |
| THD of phase-A voltage in % | 9-level inverter | 61.45 | 32.01 | 16.28 | 13.02 | 2.64 |
| | 5-level inverter | 132.53 | 61.5 | 32.05 | 24.57 | 7.85 |
| Order of dominant voltage harmonic (amplitude in %) | 9-level inverter | 400±1 (15.81) | 200±1 (11.24) | 100±1 (7.16) | 80±1 (5.29) | 45 (2.1) |
| | 5-level inverter | 400±1 (71.95) | 200±1 (15.91) | 100±1 (11.26) | 80±1 (7.82) | 50±1 (7.37) |
| THD of phase-A current in % | 9-level inverter | 3.65 | 2.70 | 2.54 | 2.97 | 1.02 |
| | 5-level inverter | 5.70 | 5.13 | 4.88 | 4.62 | 4.90 |
| Order of dominant current harmonic (amplitude in %) | 9-level inverter | 400±1 (0.78) | 200±1 (0.85) | 100±1 (0.99) | 80±1 (0.91) | 9 &13 (1.10) |
| | 5-level inverter | 400±1 (3.56) | 100±2 (2.36) | 50±2 (1.65) | 80±1 (1.21) | 5 (4.70) |

## 4.7 Conclusion

The 5-level inverter scheme describe in Chapter-3 is modified to achieve 9-level inversion operation. This is done by feeding the open-end winding induction motor by 3-level inverter from both ends. The DC-link voltage of individual inverter is selected in asymmetrical manner to get the maximum number of levels in the output phase voltage. A switching function based mathematical model of proposed 9-level inverter is developed and the performance is evaluated under different operating conditions. Motor phase voltage, phase current, their harmonic spectrums, inverter pole voltages, difference in inverter pole voltages and sudden change in modulation index are considered as an evaluation criteria for performance evaluation.

The motor phase voltage waveform becomes more and more smoother as the modulation index (reference speed) increases and approaches towards sinusoidal. The THD

in motor phase voltage and current is considerably lesser than the one obtained with the circuit configuration described in Chapter-3. In the proposed 9-level inverter configuration, in the entire range of linear modulation, the inverter with higher DC-link voltage is switched less frequently than the inverter with lower DC-link voltage making it suitable for high power drives with reduced switching losses.

A modified level shifted triangular carrier based SVPWM technique also presented in this chapter. The proposed PWM scheme is capable of ensuring a smooth changeover from the mode of two-level inversion to the 3-level, then 3-level to 4-level, then from 4-level to 5-level and so on up to 9-level inversion and vice versa. This feature reduced the switching losses at lower speed range.

The proposed topology completely eliminates the requirement of clamping diodes and DC-link capacitors which are required in neutral point clamped (NPC) inverter. It also eliminates eighty four capacitors of rating $V_{DC}/8$ which are required in 9-level FC inverter topology. Hence one can conclude that the proposed topology requires less number of components as compared to conventional topologies. The flow of triplen harmonic current through the switches and motor windings is not possible in the proposed scheme due to use of four isolated DC supply.

The requirement of isolated DC sources is further reduced from four to two in the topology proposed in next chapter.

# CHAPTER 5: HYBRID NINE-LEVEL INVERTER FOR INDUCTION MOTOR DRIVE

*[A hybrid 9-level inverter topology for open-end winding induction motor (IM) drive is discussed in this chapter. A switching state based mathematical model is developed to realize 9-level inversion operation. To validate the mathematical model simulation study is carried out in MATLAB/Simulink environment and detailed analytical results are presented. The space vector location and available switching redundancy at different locations are discussed. A modified level shifted triangular carrier based space vector pulse width modulation (SVPWM) scheme describe in previous chapter is used to generate PWM pulses for the switching devices of the proposed inverter. The capacitors balancing algorithm and performance of the drive is evaluated during steady state as well as in transient state by operating an open-end winding induction motor at no-load in constant V/f mode.]*

## 5.1 Introduction

The 9-level inverter topology proposed in Chapter-4 for open-end winding induction motor drive requires four isolated DC sources of two different voltage rating. Although this topology gives very good performance, but providing four isolated DC sources of two different rating is difficult. In order to simplify this, it is proposed to achieve 9-level inversion operation using only two isolated DC sources of same voltage rating. The proposed topology is realized by feeding one end of the open-end winding IM by 5-level hybrid inverter and the other end by conventional two-level inverter. The three phase hybrid 5-level inverter is realized by cascading a 3-level flying capacitor (FC) inverter with capacitor fed H-bridge in each phase. The capacitors voltages are maintained at desired level for the entire modulation range as well as during transient operation by making use of redundant switching states available for generating different voltage levels. The proposed topology is capable of operating as 5-level inverter at full load in case of failure of H-bridge by simply bypass the faulty H-bridge, this feature enhance the reliability drive of system. The proposed inverter requires thirty IGBTs whereas the conventional topologies NPC, FC and CHB topology based 9-level inverters require forty eight IGBTs. As compared to asymmetrical cascade H-bridge (ACHB) [49] topology which requires six isolated DC supply of two different voltage ratings the proposed topology needs only two isolated DC supplies of same rating. The proposed topology requires only six capacitors out of which three are of voltage rating $V_{DC}/4$ and three are of voltage rating $V_{DC}/8$ on the other hand conventional 9-level FC inverter requires eighty four capacitors of voltage rating $V_{DC}/8$. The conventional NPC 9-level inverter requires 168 clamping diodes and eight capacitors of voltage rating $V_{DC}/8$ this requirement is completely eliminate in the proposed hybrid 9-level inverter. In the proposed inverter semiconductor switching devices which operated at higher DC voltage switch less hence low switching frequency rating devices can be used. Both inverters are fed by isolated DC supply

so zero sequence currents are inherently prevented because there is no path available to flow of these currents.

## 5.2 Hybrid 9-Level Inverter Scheme for Induction Motor Drive

### 5.2.1 Power Circuit

The power circuit of proposed hybrid 9-level inverter scheme for induction motor with open-end winding configuration is shown in Fig. 5.1. In this scheme one end of the stator winding ($A_1$, $B_1$, $C_1$) is connected to a hybrid five-level inverter-A and the other end ($A_2$, $B_2$, $C_2$) is connected to a conventional two-level inverter-B. Both inverters are fed by isolated DC sources of magnitude $V_{DC}/2$, where $V_{DC}$ is the equivalent DC link voltage required to operate the conventional two-level inverter fed induction motor drive. The isolated DC sources can be implemented using a 12-pulse diode rectifier system. The advantage of using 12-pulse rectifier is that harmonic spectrum of the input current is improved. The 3-phase hybrid 5-level inverter-A is realized by cascading a 3-level FC inverter with capacitor fed H-bridge in each phase [185]. The flying capacitors $C_{A1}$, $C_{B1}$ and $C_{C1}$ are kept at the voltage level of $V_{DC}/4$ whereas the voltages of CHB capacitors $C_{A2}$, $C_{B2}$ and $C_{C2}$ are maintained at voltage level of $V_{DC}/8$. The 3-level FC inverter can generate three levels 0, $V_{DC}/4$ and $V_{DC}/2$ with respect to reference point O. The cascade connection of 3-level FC inverter with CHB can produce five different levels in pole voltages of inverter-A. For example, phase-A pole voltage of inverter-A, $V_{A1O}$ can have five distinct voltage levels as 0, $V_{DC}/8$, $V_{DC}/4$, $3V_{DC}/8$ and $V_{DC}/2$.

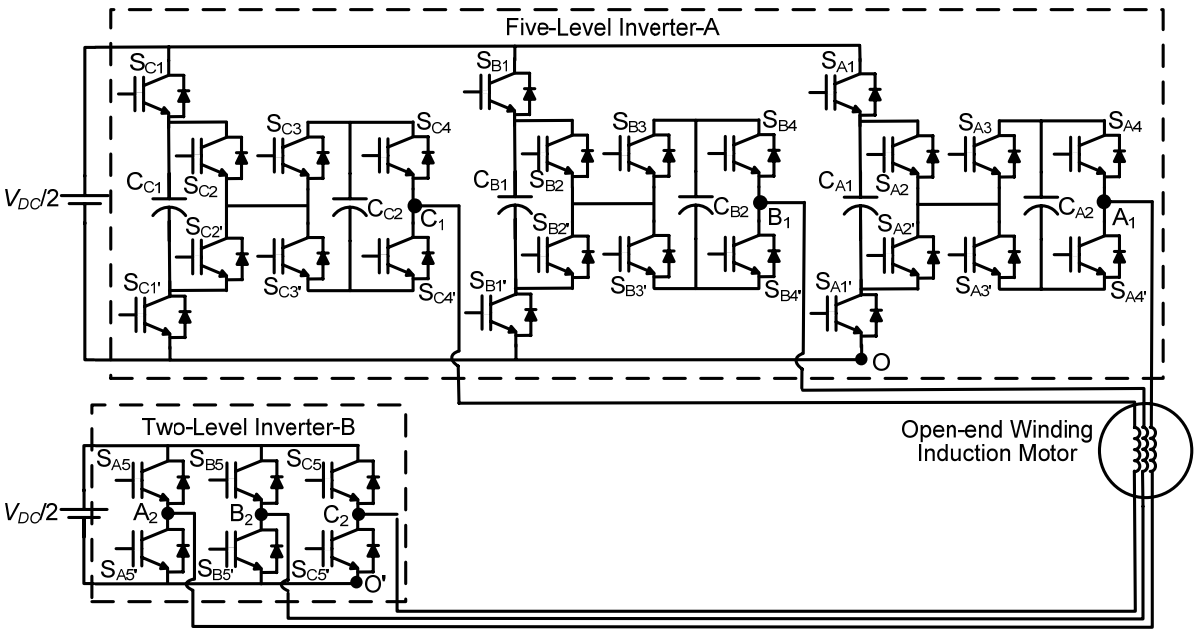



Fig. 5.1: Power circuit of hybrid 9-level inverter for induction motor drive

Similarly others pole voltages $V_{B1O}$ and $V_{C1O}$ can also have these voltage levels depending upon their corresponding switching states. Two-level inverter-B pole voltages $V_{A2O'}$, $V_{B2O'}$ and $V_{C2O'}$ can have voltage level of 0 and $V_{DC}/2$ with respect to its own reference point O'. When these two inverters simultaneously feed the power to the open-end winding IM, nine distinct levels are generated across the phase winding.

#### 5.2.1.1 Salient Features of Proposed Inverter Topology

As compared to 9-level inverter topology proposed in Chapter-4 which requires four isolated DC supplies of two different rating, the hybrid 9-level inverter presented in this chapter need only two isolated DC supplies of same rating. Another advantage of hybrid 9-level inverter is that the maximum voltage rating of the IGBT required in hybrid 9-level inverter is $V_{DC}/2$ as compared to the 9-level inverter topology reported in Chapter-4. The proposed 9-level inverter topology requires only thirty switches out of which six switches are of voltage rating $V_{DC}/2$, twelve switches are of voltage rating $V_{DC}/4$ and twelve switches are of voltage rating $V_{DC}/8$, whereas the conventional topologies (NPC, FC, CHB) based nine-level inverters require forty eight switches of voltage rating of $V_{DC}/8$. Although asymmetrical cascade H-bridge (ACHB) 9-level inverter uses only twenty four switches, but it requires six isolated DC supplies whereas proposed topology needs only two isolated DC supplies. A comparison of the proposed topology with the other 9-level inverter topologies, in terms of the number of components required, is given in Table 5.1. The proposed topology uses three capacitors $C_{A1}$, $C_{B1}$ and $C_{C1}$ of voltage rating $V_{DC}/4$ and three capacitors $C_{A2}$, $C_{B2}$ and $C_{C2}$ of voltage rating $V_{DC}/8$ whereas conventional 9-level FC inverter requires 84 capacitors of voltage rating $V_{DC}/8$ and 9-level NPC requires eight capacitors of voltage rating $V_{DC}/8$. The proposed topology completely eliminates the requirement of 168 clamping diodes which are required in NPC 9-level inverter. The cost, complexity of the control circuit and conduction losses are reduced with reduction in number of components hence proposed inverter could be a better choice for induction motor drive applications. The operation of proposed 9-level inverter is independent of the load power factor at any modulation index.

The hybrid 9-level inverter proposed in [67] requires six additional switches of voltage rating $V_{DC}/2$ as compared to the proposed 9-level inverter, apart from this the switching status of the switches operated at higher DC link voltage ($V_{DC}/2$) also changes with the change in direction of current in every level of operation this led to higher switching losses. In the proposed inverter the status of the switches operated at higher DC link voltage ($V_{DC}/2$) does not change with the change in direction of current in any level of operation that results the reduced switching losses and improved efficiency. Reliability of the system is an important issue of any industrial application. In the proposed configuration if any H-bridge fails, the inverter can be still operated as a 5-level inverter in the entire range of modulation

Table 5.1: Comparison of nine-level inverter topologies

| Component | NPC | FC | CHB | ACHB[1] | HMLI[2] | Proposed Inverter |
|---|---|---|---|---|---|---|
| DC source ($V_{DC}$) | 1 | 1 | 0 | 0 | 0 | 0 |
| DC source ($3V_{DC}/8$) | 0 | 0 | 0 | 3 | 0 | 0 |
| DC source ($V_{DC}/2$) | 0 | 0 | 0 | 0 | 2 | 2 |
| DC source ($V_{DC}/8$) | 0 | 0 | 12 | 3 | 0 | 0 |
| IGBT ($V_{DC}/8$) | 48 | 48 | 48 | 12 | 12 | 12 |
| IGBT ($V_{DC}/4$) | 0 | 0 | 0 | 0 | 12 | 12 |
| IGBT ($3V_{DC}/8$) | 0 | 0 | 0 | 12 | 0 | 0 |
| IGBT ($V_{DC}/2$) | 0 | 0 | 0 | 0 | 12 | 6 |
| Clamping diode ($V_{DC}/8$) | 168 | 0 | 0 | 0 | 0 | 0 |
| Capacitor[3] ($V_{DC}/8$) | 8 | 84 | 0 | 0 | 9 | 9 |

Note: [1] ACHB is the asymmetrical cascade H-bridge with voltage source scaled in power of 3 [49]
[2] HMLI is the hybrid multilevel inverter for open-end winding IM [67]
[3] Excluding rectifier capacitors.

even at full load by routing the current through the devices in the complementary path. For example, if $S_{A3}$ or $S_{A4}$ fails, then current can be routed through $S_{A3'}$ and $S_{A4'}$ by making them permanently ON and removing the gating signals to $S_{A3}$ and $S_{A4}$ or vice versa. This feature makes the inverter more reliable. Though proposed topology uses two isolated DC supply of same voltage rating in comparison with the NPC and FC topologies, but at the same time it also prevents the flow of triplen harmonic current through the switches and motor windings.

### 5.2.2 Generation of Different Levels and Capacitor Voltage Balancing Logic

The proposed topology is capable of generating eleven voltage levels: -(5/8)$V_{DC}$, -$V_{DC}$/2, -(3/8)$V_{DC}$, -$V_{DC}$/4, -$V_{DC}$/8, 0, +$V_{DC}$/8, +$V_{DC}$/4, +(3/8)$V_{DC}$, +$V_{DC}$/2 and +(5/8)$V_{DC}$ in phase voltage as shown in Table 5.2. Since, the voltage levels -(5/8)$V_{DC}$ and (5/8)$V_{DC}$ do not have redundant switching states to balance the capacitors voltages hence they are not used in the proposed topology. If constant DC sources are used at the place of capacitors then proposed topology can be used as 11-level inverter. The switching states to generate nine different levels ($L_1$ - $L_9$) in the phase-A voltage $V_{A1A2}$ along with the effect of these switching states on capacitors voltage based on direction of current is shown in Table 5.2. The switches $S_{xy}$ and $S_{xy'}$ (x=A, B, C and y=1, 2, 3, 4, 5) operate in complementary fashion. The voltage levels -$V_{DC}$/2, -(3/8)$V_{DC}$, -$V_{DC}$/4, -$V_{DC}$/8, 0, +$V_{DC}$/8, +$V_{DC}$/4, +(3/8)$V_{DC}$ and +$V_{DC}$/2 correspond to

levels $L_1$ to $L_9$. These voltage levels are generated by properly combining the pole voltages of five-level inverter-A ($V_{A1O}$, $V_{B1O}$, and $V_{C1O}$) with pole voltages of two-level inverter-B ($V_{A2O'}$, $V_{B2O'}$, and $V_{C2O'}$). To realize the first five levels ($L_1$-$L_5$) two-level inverter is clamped at $V_{DC}/2$ and for remaining four levels ($L_6$-$L_9$) it is kept at zero as depicted in Table 5.2.

Table 5.2: Switching states to realize nine voltage levels in phase-A and effect on capacitors

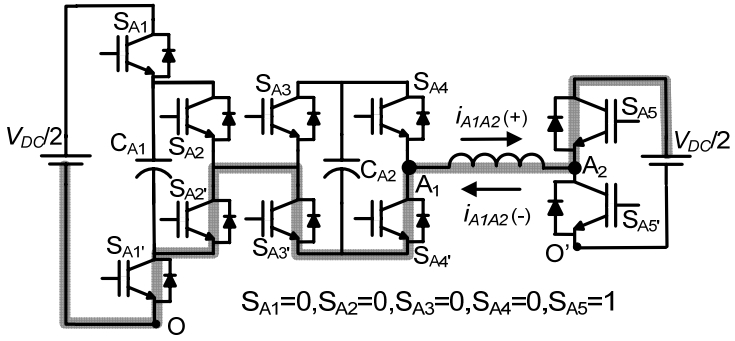
| Pole Voltage $V_{A1O}$ | Pole Voltage $V_{A2O'}$ | Motor phase-A voltage level ($V_{A1O}$ -$V_{A2O'}$) | Level Of Operation | Direction of Current $i_{A1A2}$# | Switching State* $S_{A1}$ $S_{A2}$ $S_{A3}$ $S_{A4}$ $S_{A5}$ | Effect on Capacitor $C_{A1}$ | Effect on Capacitor $C_{A2}$ |
|---|---|---|---|---|---|---|---|
| -$V_{DC}$/8 | $V_{DC}$/2 | -5$V_{DC}$/8 | Not Used | + | 00101 | No Effect | Charge |
| -$V_{DC}$/8 | $V_{DC}$/2 | -5$V_{DC}$/8 | Not Used | - | 00101 | No Effect | Discharge |
| 0 | $V_{DC}$/2 | -$V_{DC}$/2 | $L_1$ | + | 00001 | No Effect | No Effect |
| 0 | $V_{DC}$/2 | -$V_{DC}$/2 | $L_1$ | + | 00111 | No Effect | No Effect |
| 0 | $V_{DC}$/2 | -$V_{DC}$/2 | $L_1$ | - | 00001 | No Effect | No Effect |
| 0 | $V_{DC}$/2 | -$V_{DC}$/2 | $L_1$ | - | 00111 | No Effect | No Effect |
| $V_{DC}$/8 | $V_{DC}$/2 | -3$V_{DC}$/8 | $L_2$ | + | 00011 | No Effect | Discharge |
| $V_{DC}$/8 | $V_{DC}$/2 | -3$V_{DC}$/8 | $L_2$ | + | 01101 | Discharge | Charge |
| $V_{DC}$/8 | $V_{DC}$/2 | -3$V_{DC}$/8 | $L_2$ | + | 10101 | Charge | Charge |
| $V_{DC}$/8 | $V_{DC}$/2 | -3$V_{DC}$/8 | $L_2$ | - | 00011 | No Effect | Charge |
| $V_{DC}$/8 | $V_{DC}$/2 | -3$V_{DC}$/8 | $L_2$ | - | 01101 | Charge | Discharge |
| $V_{DC}$/8 | $V_{DC}$/2 | -3$V_{DC}$/8 | $L_2$ | - | 10101 | Discharge | Discharge |
| $V_{DC}$/4 | $V_{DC}$/2 | -$V_{DC}$/4 | $L_3$ | + | 10001 | Charge | No Effect |
| $V_{DC}$/4 | $V_{DC}$/2 | -$V_{DC}$/4 | $L_3$ | + | 01001 | Discharge | No Effect |
| $V_{DC}$/4 | $V_{DC}$/2 | -$V_{DC}$/4 | $L_3$ | + | 01111 | Discharge | No Effect |
| $V_{DC}$/4 | $V_{DC}$/2 | -$V_{DC}$/4 | $L_3$ | + | 10111 | Charge | No Effect |
| $V_{DC}$/4 | $V_{DC}$/2 | -$V_{DC}$/4 | $L_3$ | - | 10001 | Discharge | No Effect |
| $V_{DC}$/4 | $V_{DC}$/2 | -$V_{DC}$/4 | $L_3$ | - | 01001 | Charge | No Effect |
| $V_{DC}$/4 | $V_{DC}$/2 | -$V_{DC}$/4 | $L_3$ | - | 01111 | Charge | No Effect |
| $V_{DC}$/4 | $V_{DC}$/2 | -$V_{DC}$/4 | $L_3$ | - | 10111 | Discharge | No Effect |
| 3$V_{DC}$/8 | $V_{DC}$/2 | -$V_{DC}$/8 | $L_4$ | + | 01011 | Discharge | Discharge |
| 3$V_{DC}$/8 | $V_{DC}$/2 | -$V_{DC}$/8 | $L_4$ | + | 10011 | Charge | Discharge |
| 3$V_{DC}$/8 | $V_{DC}$/2 | -$V_{DC}$/8 | $L_4$ | + | 11101 | No Effect | Charge |
| 3$V_{DC}$/8 | $V_{DC}$/2 | -$V_{DC}$/8 | $L_4$ | - | 01011 | Charge | Charge |
| 3$V_{DC}$/8 | $V_{DC}$/2 | -$V_{DC}$/8 | $L_4$ | - | 10011 | Discharge | Charge |
| 3$V_{DC}$/8 | $V_{DC}$/2 | -$V_{DC}$/8 | $L_4$ | - | 11101 | No Effect | Discharge |
| $V_{DC}$/2 | $V_{DC}$/2 | 0 | $L_5$ | + | 11111 | No Effect | No Effect |

| Pole Voltage $V_{A1O}$ | Pole Voltage $V_{A2O'}$ | Motor phase-A voltage level ($V_{A1O}$ -$V_{A2O'}$) | Level Of Operation | Direction of Current $i_{A1A2}$# | Switching State* $S_{A1}$ $S_{A2}$ $S_{A3}$ $S_{A4}$ $S_{A5}$ | Effect on Capacitor $C_{A1}$ | Effect on Capacitor $C_{A2}$ |
|---|---|---|---|---|---|---|---|
| $V_{DC}/2$ | $V_{DC}/2$ | 0 | $L_5$ | + | 11001 | No Effect | No Effect |
| $V_{DC}/2$ | $V_{DC}/2$ | 0 | $L_5$ | - | 11111 | No Effect | No Effect |
| $V_{DC}/2$ | $V_{DC}/2$ | 0 | $L_5$ | - | 11001 | No Effect | No Effect |
| $V_{DC}/8$ | 0 | $+V_{DC}/8$ | $L_6$ | + | 00010 | No Effect | Discharge |
| $V_{DC}/8$ | 0 | $+V_{DC}/8$ | $L_6$ | + | 01100 | Discharge | Charge |
| $V_{DC}/8$ | 0 | $+V_{DC}/8$ | $L_6$ | + | 10100 | Charge | Charge |
| $V_{DC}/8$ | 0 | $+V_{DC}/8$ | $L_6$ | - | 00010 | No Effect | Charge |
| $V_{DC}/8$ | 0 | $+V_{DC}/8$ | $L_6$ | - | 01100 | Charge | Discharge |
| $V_{DC}/8$ | 0 | $+V_{DC}/8$ | $L_6$ | - | 10100 | Discharge | Discharge |
| $V_{DC}/4$ | 0 | $+V_{DC}/4$ | $L_7$ | + | 10000 | Charge | No Effect |
| $V_{DC}/4$ | 0 | $+V_{DC}/4$ | $L_7$ | + | 01000 | Discharge | No Effect |
| $V_{DC}/4$ | 0 | $+V_{DC}/4$ | $L_7$ | + | 01110 | Discharge | No Effect |
| $V_{DC}/4$ | 0 | $+V_{DC}/4$ | $L_7$ | + | 10110 | Charge | No Effect |
| $V_{DC}/4$ | 0 | $+V_{DC}/4$ | $L_7$ | - | 10000 | Discharge | No Effect |
| $V_{DC}/4$ | 0 | $+V_{DC}/4$ | $L_7$ | - | 01000 | Charge | No Effect |
| $V_{DC}/4$ | 0 | $+V_{DC}/4$ | $L_7$ | - | 01110 | Charge | No Effect |
| $V_{DC}/4$ | 0 | $+V_{DC}/4$ | $L_7$ | - | 10110 | Discharge | No Effect |
| $3V_{DC}/8$ | 0 | $+3V_{DC}/8$ | $L_8$ | + | 01010 | Discharge | Discharge |
| $3V_{DC}/8$ | 0 | $+3V_{DC}/8$ | $L_8$ | + | 10010 | Charge | Discharge |
| $3V_{DC}/8$ | 0 | $+3V_{DC}/8$ | $L_8$ | + | 11100 | No Effect | Charge |
| $3V_{DC}/8$ | 0 | $+3V_{DC}/8$ | $L_8$ | - | 01010 | Charge | Charge |
| $3V_{DC}/8$ | 0 | $+3V_{DC}/8$ | $L_8$ | - | 10010 | Discharge | Charge |
| $3V_{DC}/8$ | 0 | $+3V_{DC}/8$ | $L_8$ | - | 11100 | No Effect | Discharge |
| $V_{DC}/2$ | 0 | $+V_{DC}/2$ | $L_9$ | + | 11110 | No Effect | No Effect |
| $V_{DC}/2$ | 0 | $+V_{DC}/2$ | $L_9$ | + | 11000 | No Effect | No Effect |
| $V_{DC}/2$ | 0 | $+V_{DC}/2$ | $L_9$ | - | 11110 | No Effect | No Effect |
| $V_{DC}/2$ | 0 | $+V_{DC}/2$ | $L_9$ | - | 11000 | No Effect | No Effect |
| $5V_{DC}/8$ | 0 | $+5V_{DC}/8$ | Not used | + | 11010 | No Effect | Discharge |
| $5V_{DC}/8$ | 0 | $+5V_{DC}/8$ | Not used | - | 11010 | No Effect | Charge |

Note: # Direction of current in motor winding from terminal $A_1$ to $A_2$ is assumed to be positive (+) and from $A_2$ to $A_1$ is negative (-)

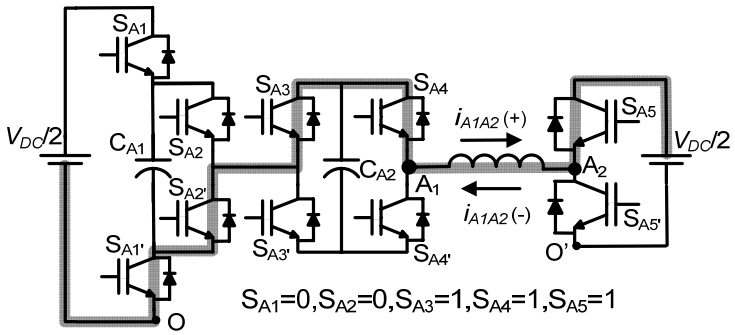
* Switching state '1' denotes switch is ON and '0' denotes switch is OFF

To generate voltage levels of $-V_{DC}/2$, 0 and $V_{DC}/2$, there are two redundant states for each level, for voltage levels of $-(3/8)V_{DC}$, $-V_{DC}/8$, $+V_{DC}/8$ and $(3/8)V_{DC}$ there are three redundant states for each level and to generate $-V_{DC}/4$ and $+V_{DC}/4$ there are four redundant states available for each level. Fig. 5.2 shows two possible circuit configuration to generate voltage level of $-V_{DC}/2$ in phase-A. Since current does not flow through the capacitors $C_{A1}$ and $C_{A2}$ during operation in level $L_1$ ($-V_{DC}/2$) hence capacitors voltages are unaffected.




$$V_{A1O} - V_{A2O'} = 0 - V_{DC}/2 = -V_{DC}/2$$

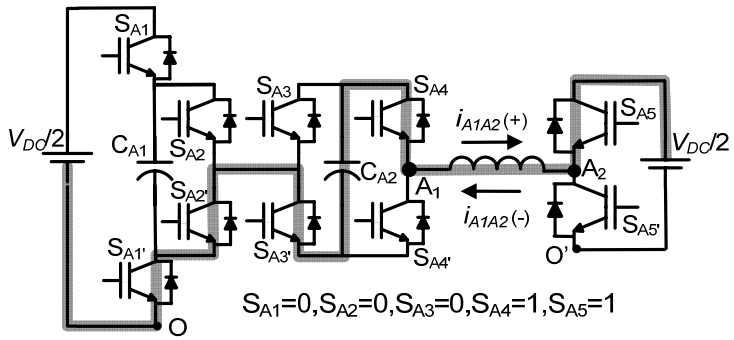
(a)




$$V_{A1O} - V_{A2O'} = 0 - V_{DC}/2 = -V_{DC}/2$$

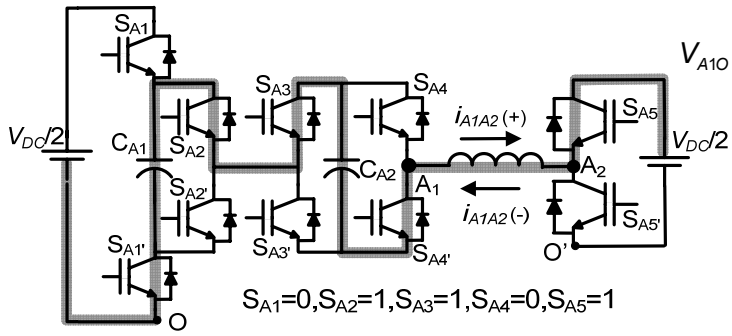
(b)

Fig. 5.2: Methods of generating voltage level $-V_{DC}/2$ ($L_1$) in phase-A and current path
(a) For switching state $S_{A1}=0$, $S_{A2}=0$, $S_{A3}=0$, $S_{A4}=0$, $S_{A5}=1$
(b) For switching state $S_{A1}=0$, $S_{A2}=0$, $S_{A3}=1$, $S_{A4}=1$, $S_{A5}=1$



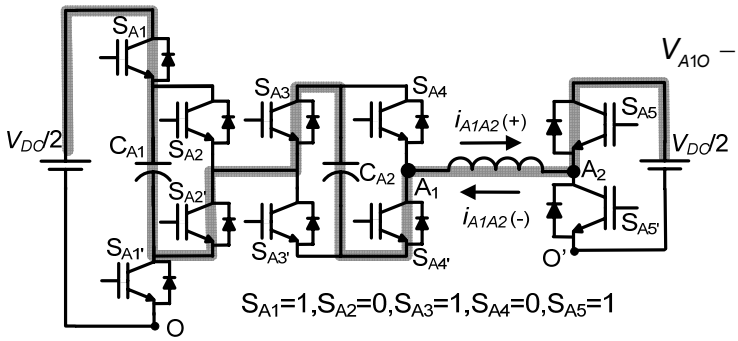

$$V_{A1O} - V_{A2O'} = V_{CA2} - V_{DC}/2$$
$$= V_{DC}/8 - V_{DC}/2$$
$$= -3V_{DC}/8$$

(a)




$$V_{A1O} - V_{A2O'} = -V_{CA2} + V_{CA1} - V_{DC}/2$$
$$= -V_{DC}/8 + V_{DC}/4 - V_{DC}/2$$
$$= -3V_{DC}/8$$

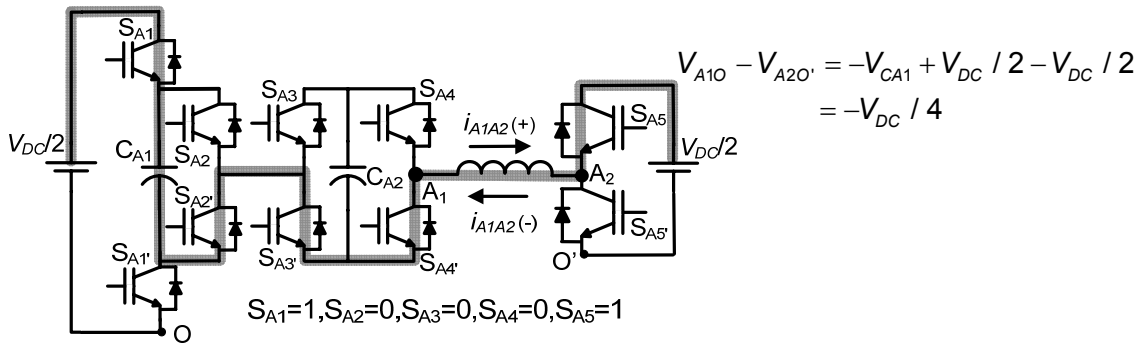
(b)



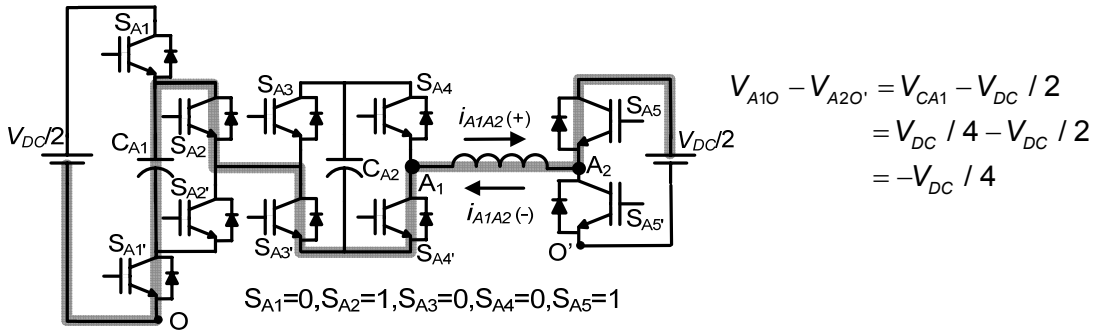

$$V_{A1O} - V_{A2O'} = -V_{CA2} - V_{CA1} + V_{DC}/2 - V_{DC}/2$$
$$= -V_{DC}/8 - V_{DC}/4$$
$$= -3V_{DC}/8$$

(c)

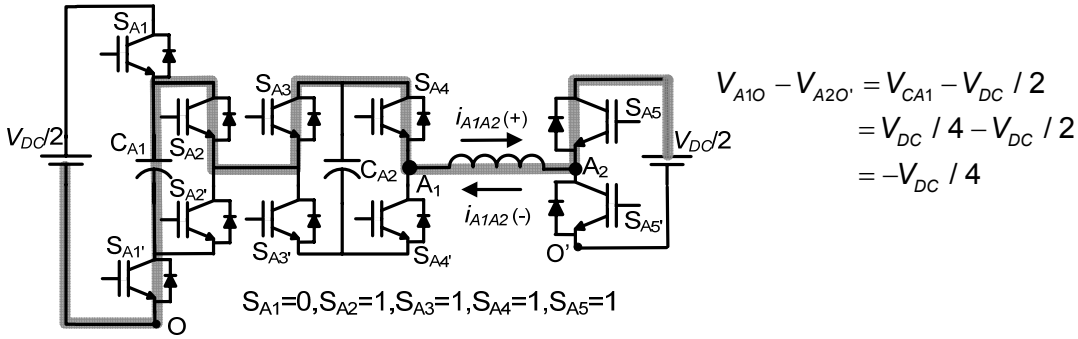
Fig. 5.3: Methods of generating voltage level -3$V_{DC}$/8 ($L_2$) in phase-A and current path
(a) For switching state $S_{A1}$=0, $S_{A2}$=0, $S_{A3}$=0, $S_{A4}$=1, $S_{A5}$=1
(b) For switching state $S_{A1}$=0, $S_{A2}$=1, $S_{A3}$=1, $S_{A4}$=0, $S_{A5}$=1
(c) For switching state $S_{A1}$=1, $S_{A2}$=0, $S_{A3}$=1, $S_{A4}$=0, $S_{A5}$=1



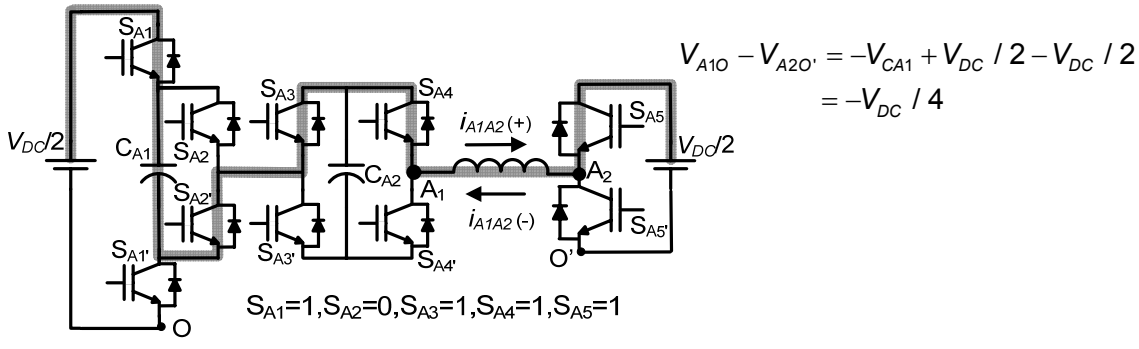

(a)




(b)

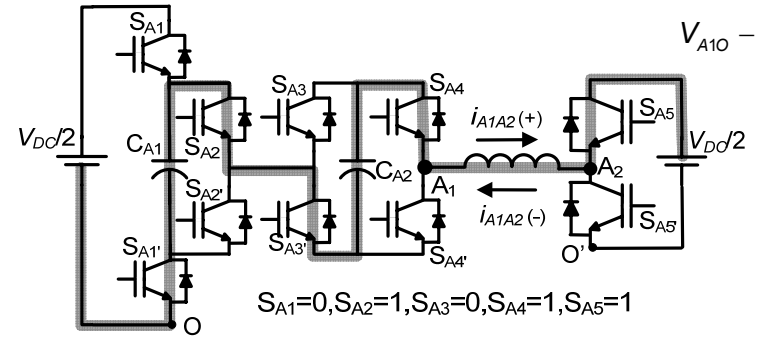



(c)



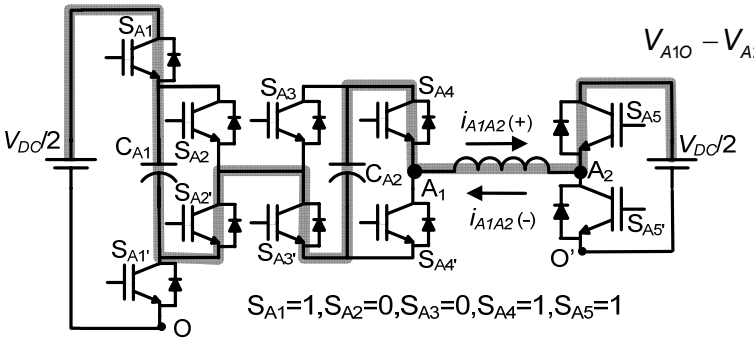

(d)

Fig. 5.4: Methods of generating voltage level -$V_{DC}$/4 ($L_3$) in phase-A and current path
(a) For switching state $S_{A1}$=1, $S_{A2}$=0, $S_{A3}$=0, $S_{A4}$=0, $S_{A5}$=1
(b) For switching state $S_{A1}$=0, $S_{A2}$=1, $S_{A3}$=0, $S_{A4}$=0, $S_{A5}$=1
(c) For switching state $S_{A1}$=0, $S_{A2}$=1, $S_{A3}$=1, $S_{A4}$=1, $S_{A5}$=1
(d) For switching state $S_{A1}$=1, $S_{A2}$=0, $S_{A3}$=1, $S_{A4}$=1, $S_{A5}$=1



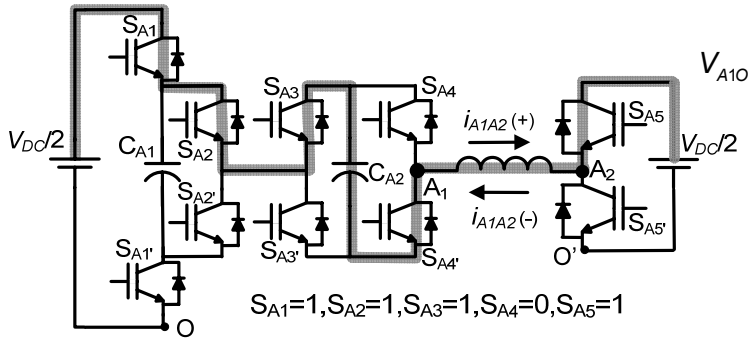

$$V_{A1O} - V_{A2O'} = V_{CA2} + V_{CA1} - V_{DC}/2$$
$$= V_{DC}/8 + V_{DC}/4 - V_{DC}/2$$
$$= -V_{DC}/8$$

(a)




$$V_{A1O} - V_{A2O'} = V_{CA2} - V_{CA1} + V_{DC}/2 - V_{DC}/2$$
$$= V_{DC}/8 - V_{DC}/4$$
$$= -V_{DC}/8$$

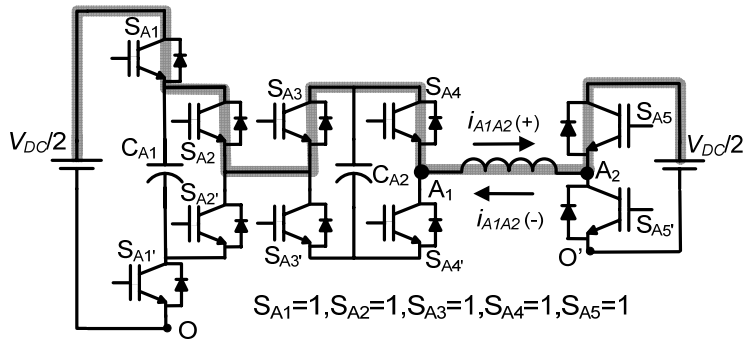
(b)




$$V_{A1O} - V_{A2O'} = -V_{CA2} + V_{DC}/2 - V_{DC}/2$$
$$= -V_{DC}/8$$

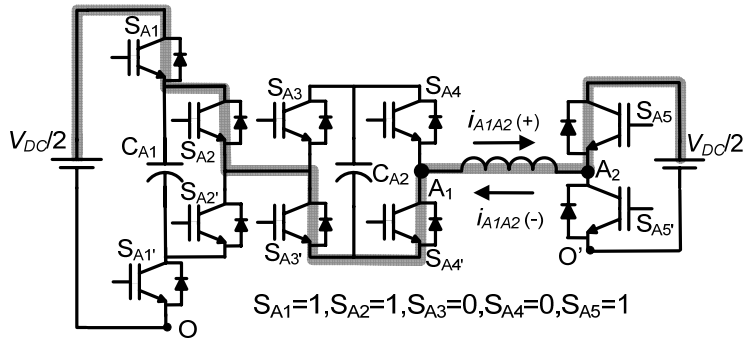
(c)

Fig. 5.5: Methods of generating voltage level -$V_{DC}/8$ (L4) in phase-A and current path
(a) For switching state $S_{A1}$=0, $S_{A2}$=1, $S_{A3}$=0, $S_{A4}$=1, $S_{A5}$=1
(b) For switching state $S_{A1}$=1, $S_{A2}$=0, $S_{A3}$=0, $S_{A4}$=1, $S_{A5}$=1
(c) For switching state $S_{A1}$=1, $S_{A2}$=1, $S_{A3}$=1, $S_{A4}$=0, $S_{A5}$=1




$$V_{A1O} - V_{A2O'} = V_{DC}/2 - V_{DC}/2 = 0$$

(a)




$$V_{A1O} - V_{A2O'} = V_{DC}/2 - V_{DC}/2 = 0$$

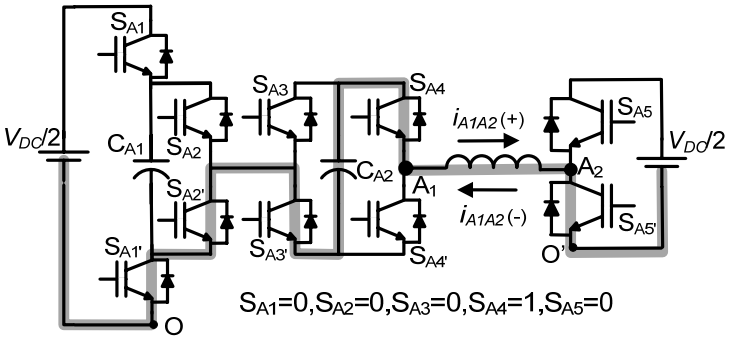
(b)

Fig. 5.6: Methods of generating voltage level 0 ($L_5$) in phase-A and current path
(a) For switching state $S_{A1}$=1, $S_{A2}$=1, $S_{A3}$=1, $S_{A4}$=1, $S_{A5}$=1
(b) For switching state $S_{A1}$=1, $S_{A2}$=1, $S_{A3}$=0, $S_{A4}$=0, $S_{A5}$=1

Different ways to generate -(3/8)$V_{DC}$ in phase-A using redundant switching states are shown in Fig. 5.3. Since the capacitors come in the path of current and depending upon the direction of current they get charge or discharge, hence the capacitors voltage balancing has to be ensure using the different switching combination as shown in Table 5.2. Various circuit configurations to realize voltage levels -$V_{DC}$/4 ($L_3$), -$V_{DC}$/8 ($L_4$), 0 ($L_5$), $V_{DC}$/8 ($L_6$), $V_{DC}$/4 ($L_7$), 3$V_{DC}$/8 ($L_8$) and $V_{DC}$/2 ($L_9$) in phase-A are shown in from Fig. 5.5 to Fig. 5.10. It can be noticed from these circuit configurations that to generate last four levels ($L_6$ – $L_9$), inverter-A uses same switching combination as it uses to generate levels $L_2$ – $L_5$ respectively, whereas two-level inverter-B is clamped at zero voltage. The flying capacitors can be either charged or discharged in any direction of current by using the redundant switching states in any level of operation. FCs voltages can be maintained at desired level by selecting the appropriate switching states as shown in Table 5.2 depending upon the direction of current $i_{A1A2}$ for all nine levels of phase-A. Similar logic can also be implemented for other two phases.

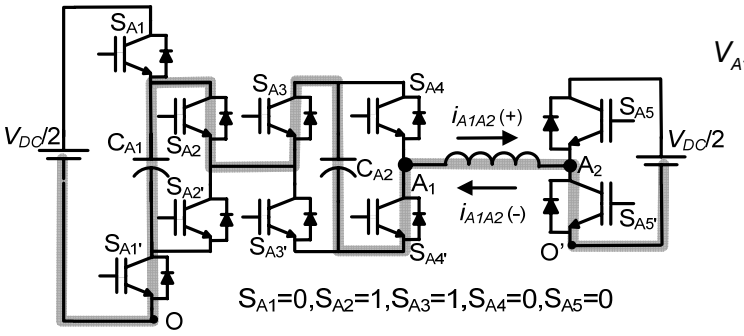
The capacitors voltages are sensed and compared with reference voltage ($V_{DC}$/4 for

$C_{A1}$, $C_{B1}$, $C_{C1}$ and $V_{DC}/8$ for $C_{A2}$, $C_{B2}$, $C_{C2}$) in every switching period and error is passed through hysteresis controller. The hysteresis controller selects the appropriate switching combination to minimize the error. The capacitors voltages are balanced quickly because the corrective action is taking place in every switching period. The capacitor-voltage balancing can be done independent of load power factor at any modulation index.



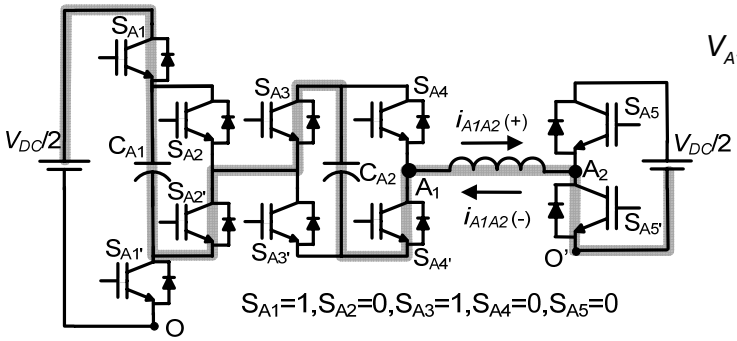

$$V_{A1O} - V_{A2O'} = V_{CA2} - 0$$
$$= V_{DC}/8 - 0$$
$$= V_{DC}/8$$

(a)




$$V_{A1O} - V_{A2O'} = -V_{CA2} + V_{CA1} - 0$$
$$= -V_{DC}/8 + V_{DC}/4 - 0$$
$$= V_{DC}/8$$

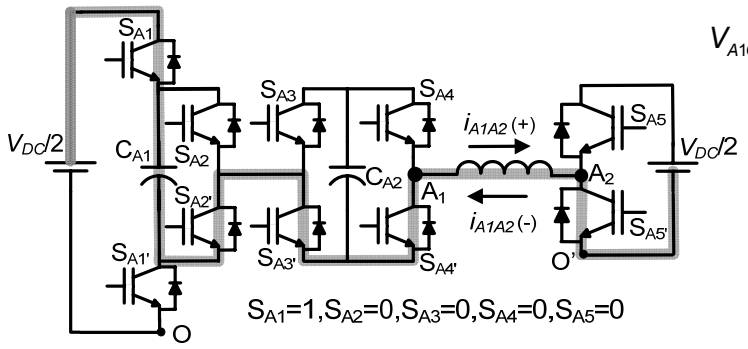
(b)




$$V_{A1O} - V_{A2O'} = -V_{CA2} - V_{CA1} + V_{DC}/2 - 0$$
$$= -V_{DC}/8 - V_{DC}/4 + V_{DC}/2$$
$$= V_{DC}/8$$

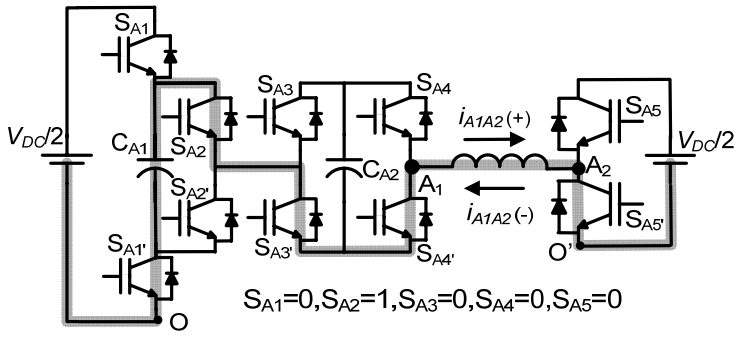
(c)

Fig. 5.7: Methods of generating voltage level $V_{DC}/8$ ($L_6$) in phase-A and current path
(a) For switching state $S_{A1}$=0, $S_{A2}$=0, $S_{A3}$=0, $S_{A4}$=1, $S_{A5}$=0
(b) For switching state $S_{A1}$=0, $S_{A2}$=1, $S_{A3}$=1, $S_{A4}$=0, $S_{A5}$=0
(c) For switching state $S_{A1}$=1, $S_{A2}$=0, $S_{A3}$=1, $S_{A4}$=0, $S_{A5}$=0



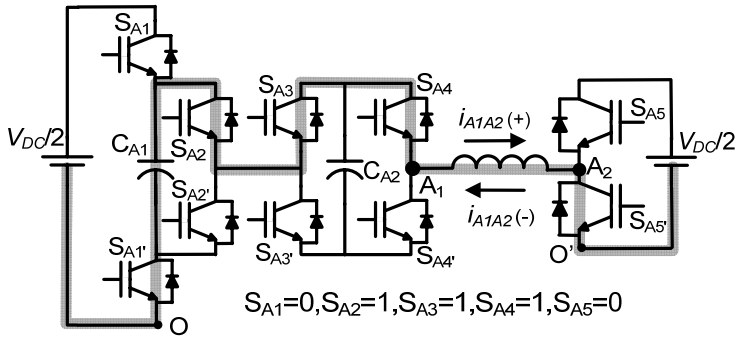

$$V_{A1O} - V_{A2O'} = -V_{CA1} + V_{DC}/2 - 0$$
$$= -V_{DC}/4 + V_{DC}/2$$
$$= V_{DC}/4$$

(a)



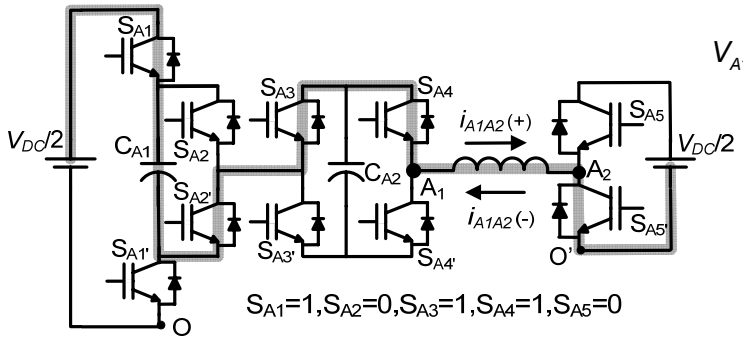

$$V_{A1O} - V_{A2O'} = V_{CA1} - 0$$
$$= V_{DC}/4$$

(b)




$$V_{A1O} - V_{A2O'} = V_{CA1} - 0$$
$$= V_{DC}/4$$

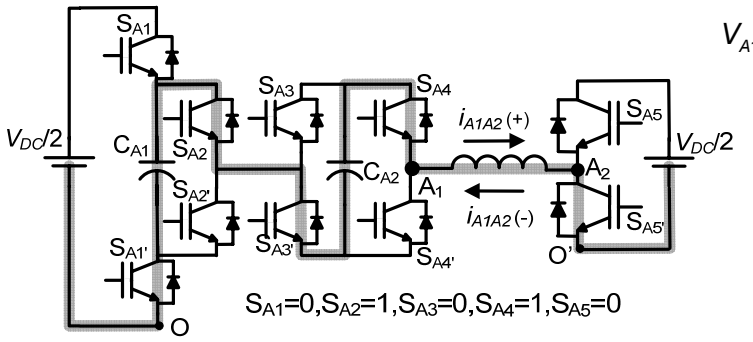
(c)




$$V_{A1O} - V_{A2O'} = -V_{CA1} + V_{DC}/2 - 0$$
$$= V_{DC}/4$$

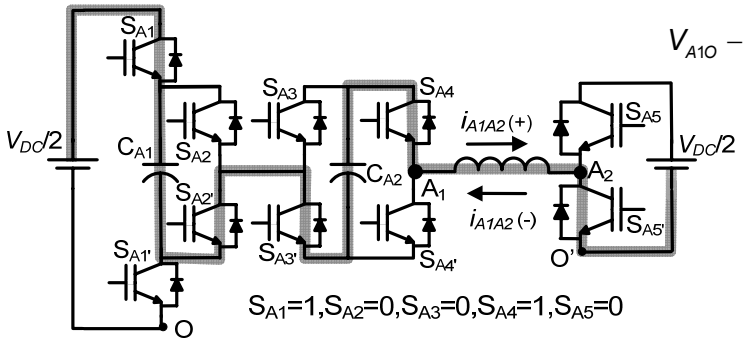
(d)

Fig. 5.8: Methods of generating voltage level $V_{DC}/4$ ($L_7$) in phase-A and current path
(a) For switching state $S_{A1}$=1, $S_{A2}$=0, $S_{A3}$=0, $S_{A4}$=0, $S_{A5}$=0
(b) For switching state $S_{A1}$=0, $S_{A2}$=1, $S_{A3}$=0, $S_{A4}$=0, $S_{A5}$=0
(c) For switching state $S_{A1}$=0, $S_{A2}$=1, $S_{A3}$=1, $S_{A4}$=1, $S_{A5}$=0
(d) For switching state $S_{A1}$=1, $S_{A2}$=0, $S_{A3}$=1, $S_{A4}$=1, $S_{A5}$=0



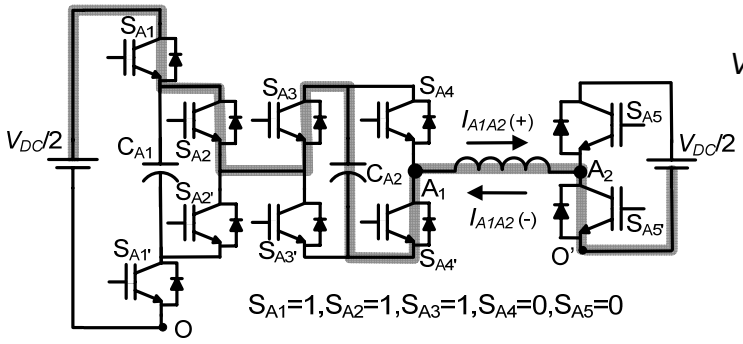

$$V_{A1O} - V_{A2O'} = V_{CA2} + V_{CA1} - 0$$
$$= V_{DC}/8 + V_{DC}/4$$
$$= 3V_{DC}/8$$

(a)




$$V_{A1O} - V_{A2O'} = V_{CA2} - V_{CA1} + V_{DC}/2 - 0$$
$$= V_{DC}/8 - V_{DC}/4 + V_{DC}/2$$
$$= 3V_{DC}/8$$

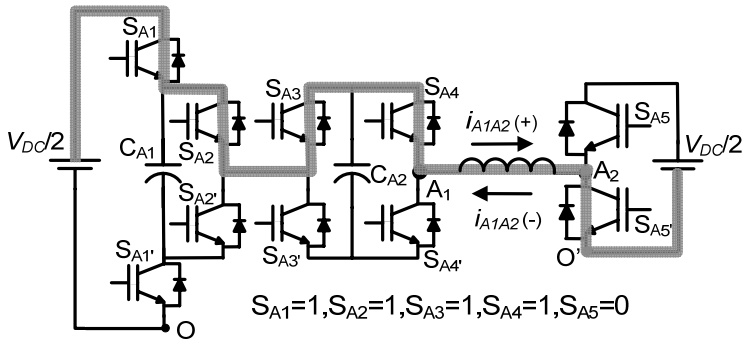
(b)




$$V_{A1O} - V_{A2O'} = -V_{CA2} + V_{DC}/2 - 0$$
$$= 3V_{DC}/8$$

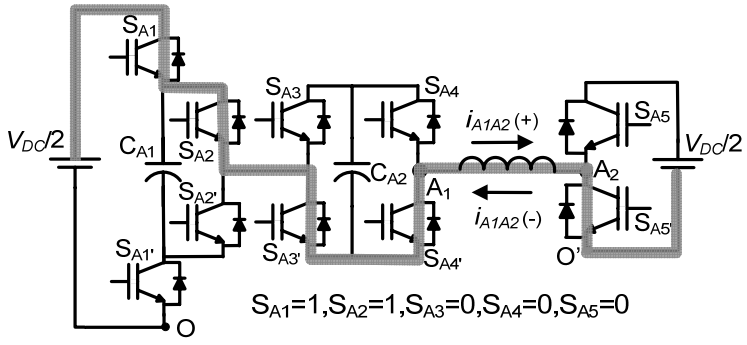
(c)

Fig. 5.9: Methods of generating voltage level $3V_{DC}/8$ (L8) in phase-A and current path
(a) For switching state $S_{A1}$=0, $S_{A2}$=1, $S_{A3}$=0, $S_{A4}$=1, $S_{A5}$=0
(b) For switching state $S_{A1}$=1, $S_{A2}$=0, $S_{A3}$=0, $S_{A4}$=1, $S_{A5}$=0
(c) For switching state $S_{A1}$=1, $S_{A2}$=1, $S_{A3}$=1, $S_{A4}$=0, $S_{A5}$=0




$$V_{A1O} - V_{A2O'} = V_{DC}/2 - 0$$
$$= V_{DC}/2$$

(a)




$$V_{A1O} - V_{A2O'} = V_{DC}/2 - 0$$
$$= V_{DC}/2$$

(b)

Fig. 5.10: Methods of generating voltage level $V_{DC}/2$ ($L_9$) in phase-A and current path
(a) For switching state $S_{A1}$=1, $S_{A2}$=1, $S_{A3}$=1, $S_{A4}$=1, $S_{A5}$=0
(b) For switching state $S_{A1}$=1, $S_{A2}$=1, $S_{A3}$=0, $S_{A4}$=0, $S_{A5}$=0

### 5.2.3 Control Strategy and Capacitor Design

The block diagram of control logic is shown in Fig. 5.11. A level shifted pulse width modulation (LSPWM) technique proposed in section 4.3 of Chapter-4 is used to generate PWM pulses for 9-level inverter. The switching frequency is kept constant during the entire range of operation and it is selected as 1kHz. The required reference phasor $V_r^*$ is calculated from the motor speed requirement by using constant *V/f* control. The three reference phase voltages ($V_{A1A2}^*, V_{B1B2}^*, V_{C1C2}^*$) are generated by transferring the orthogonal components of reference voltage phasor $V_r^*$ into the three phase quantity and expressed by:

$$\left.\begin{aligned} V_{A1A2}^* &= V_m^* Sin\omega t \\ V_{B1B2}^* &= V_m^* Sin(\omega t - 2\pi/3) \\ V_{C1C2}^* &= V_m^* Sin(\omega t + 2\pi/3) \end{aligned}\right\} \quad (5.1)$$

These reference waves are fed to SVPWM generation block which add a DC bias of magnitude $\frac{nV_c}{2}$ and an offset ($V_{offset}$) signal to generate three modulating signals. The three modulating signals correspond to phase-A, B and C, generated by SVPWM block are given by equation (5.2).

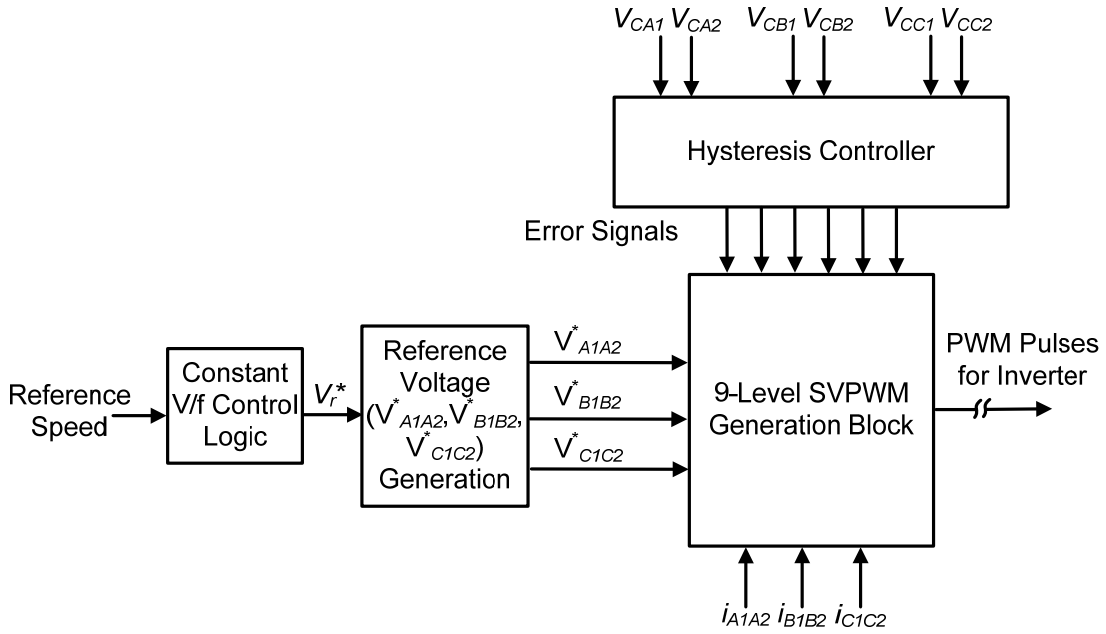



Fig. 5.11: Block diagram of control logic

$$\left.\begin{aligned} V_a^* &= V_m^* Sin\omega t + V_{offset} + nV_c/2 \\ V_b^* &= V_m^* Sin(\omega t - 2\pi/3) + V_{offset} + nV_c/2 \\ V_c^* &= V_m^* Sin(\omega t + 2\pi/3) + V_{offset} + nV_c/2 \end{aligned}\right\} \quad (5.2)$$

Where, $V_{offset} = -[\max(V^*_{A1A2}, V^*_{B1B2}, V^*_{C1C2}) + \min(V^*_{A1A2}, V^*_{B1B2}, V^*_{C1C2})]/2$ and $V_c$ is the amplitude of triangular carrier. The value of '*n*' changes from 1 to 8 for two-level to nine-level operation.

A hysteresis controller is used to maintain the capacitors voltage at desired level. All six capacitors voltages ($V_{CA1}$, $V_{CA2}$, $V_{CB1}$, $V_{CB2}$, $V_{CC1}$, $V_{CC2}$) are sensed and given to the hysteresis controller. The hysteresis controller compares the measured voltages with their respective reference voltages and generates error signals. If the instantaneous value of capacitor voltage is within the acceptable limit then the hysteresis controller generates zero value of error which means no action is required. If the value of capacitor voltage exceeds the upper boundary of the hysteresis controller, the controller generates the negative error signal and a switching combination is to be selected by SVPWM generation block which discharge the capacitor. Similarly if the value of capacitor voltage crosses the lower limit of the hysteresis controller, the controller generates the positive error signal and a switching combination is to be selected by SVPWM which charge the capacitor. The 9-level SVPWM generation block simultaneously compared the three modulating signals ($V_a^*, V_b^*, V_c^*$) with eight triangular carrier (C1-C8) as shown in Fig. 5.12 and identify the level of operation. The modulating signals for the value of modulation index *m*=0.8 along with eight triangular carriers as shown in Fig. 4.4, is redrawn in Fig. 5.12 to facilitate an easy reference. Once the level of operation is identify

PWM pulses are generated depending upon respective error signals for capacitors voltages ($V_{CA1}$, $V_{CA2}$, $V_{CB1}$, $V_{CB2}$, $V_{CC1}$, $V_{CC2}$) and direction of three phase currents ($i_{A1A2}$, $i_{B1B2}$, $i_{C1C2}$) according to the Table 5.2.

The ripples in capacitors voltages significantly affect the performance of proposed 9-level inverter. The capacitors are designed in such a way that ripple in voltage across the capacitors would not exceed the allowable limit in one switching cycle at full load current. Accordingly, the capacitance (C) is selected by the following equation

$$C = \frac{I_L \times T_s}{\Delta V} \tag{5.3}$$

Where $I_L$ is peak load current, $T_s$ is switching period and $\Delta V$ is allowable peak to peak ripple in capacitor voltage.

For the peak load current of 8A and allowable ripples in capacitor voltage of 4V all six capacitors are selected of rating 2200 μF.

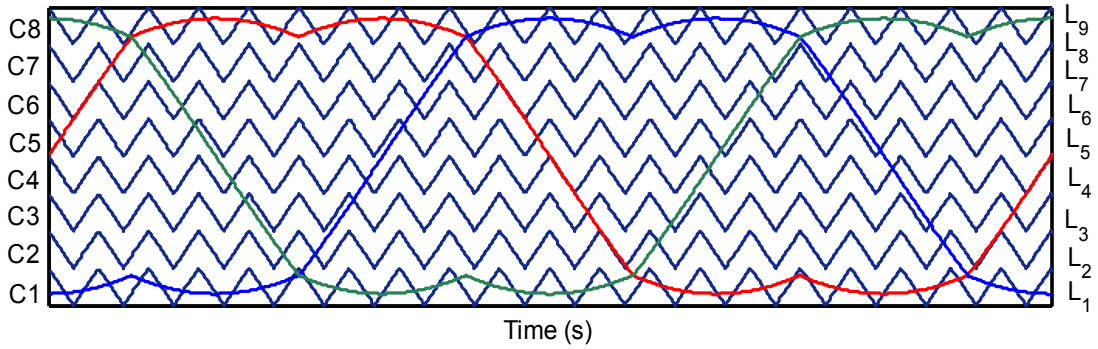



Fig. 5.12: Modulating signals with eight level shifted triangular carriers

### 5.2.4 Analysis of Voltage Space Vectors

The equation for equivalent voltage space vector $V_s$ can be written as:

$$V_s = V_{A1A2} + V_{B1B2}.e^{j(2\pi/3)} + V_{C1C2}.e^{j(4\pi/3)} \tag{5.4}$$

It is shown in Table 5.2 that there are 26 possible combination to generate nine different levels in phase-A. Therefore, a total of 17576 (26 × 26 × 26) switching states are possible for the proposed three-phase 9-level inverter. These switching combinations are distributed over 217 locations as shown in Fig. 5.13. The space-vector diagram for the proposed hybrid 9-level inverter consists of eight concentric hexagons. The switching state combinations for a space-vector sector of 60º interval (shaded locations in Fig. 5.13) are tabulated in Table 5.3. The outermost forty eight locations starting from 170 to 217 have only one combination of phases to generate these vectors. The space-vector locations from 128 to 169 have two combinations, locations from 92 to 127 have locations three combinations, locations from 62 to 91 have four combinations, locations from 38 to 61 have five redundant states, locations from 20 to 37 have six redundant states and locations from 8 to 19 have seven redundant states. The space-vector locations 2, 3, 4, 5, 6 and 7 are located on smallest

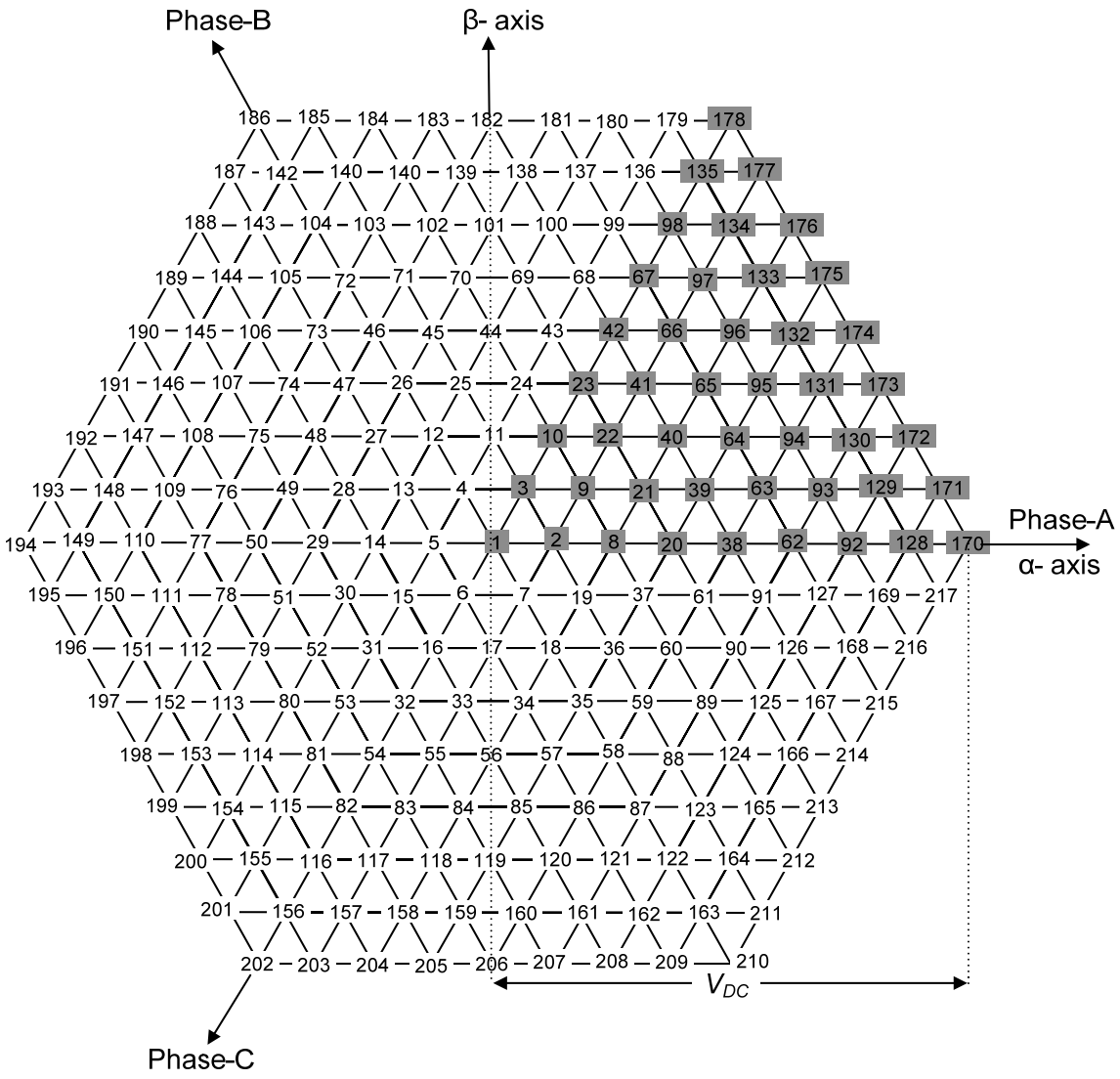



Fig. 5.13: Locations of voltage space-phasors for 9-level inverter

hexagon have eight redundant states. The zero vector location 1 located at the center of polygon has a total number of nine redundant states. The available redundancies at different locations can be used in space vector pulse width modulation (SVPWM) to minimize the switching losses by reducing inverter switching transition.

Table 5.3: Switching states for space-vector sector of 60º interval

| State No. | Combinations of three phases (a,b,c)# | Number of combinations |
|---|---|---|
| 1 | (0,0,0)(1,1,1)(2,2,2)(3,3,3)(4,4,4) (5,5,5)(6,6,6)(7,7,7) (8,8,8) | 9 |
| 2 | (1,0,0)(2,1,1)(3,2,2)(4,3,3) (5,4,4)(6,5,5)(7,6,6)(8,7,7) | 8 |
| 3 | (1,1,0)(2,2,1)(3,3,2)(4,4,3) (5,5,4)(6,6,5)(7,7,6)(8,8,7) | 8 |
| 8 | (2,0,0)(3,1,1)(4,2,2)(5,3,3) (6,4,4)(7,5,5)(8,6,6) | 7 |
| 9 | (2,1,0)(3,2,1)(4,3,2)(5,4,3) (6,5,4)(7,6,5)(8,7,6) | 7 |
| 10 | (2,2,0)(3,3,1)(4,4,2)(5,5,3) (6,6,4)(7,7,5)(8,8,6) | 7 |
| 20 | (3,0,0)(4,1,1)(5,2,2)(6,3,3)(7,4,4)(8,5,5) | 6 |
| 21 | (3,1,0)(4,2,1)(5,3,2)(6,4,3)(7,5,4)(8,6,5) | 6 |
| 22 | (3,2,0)(4,3,1)(5,4,2)(6,5,3)(7,6,4)(8,7,5) | 6 |
| 23 | (3,3,0)(4,4,1)(5,5,2)(6,6,3)(7,7,4)(8,8,5) | 6 |
| 38 | (4,0,0)(5,1,1)(6,2,2) (7,3,3)(8,4,4) | 5 |
| 39 | (4,1,0)(5,2,1)(6,3,2) (7,4,3)(8,5,4) | 5 |
| 40 | (4,2,0)(5,3,1)(6,4,2) (7,5,3)(8,6,4) | 5 |
| 41 | (4,3,0)(5,4,1)(6,5,2) (7,6,3)(8,7,4) | 5 |
| 42 | (4,4,0)(5,5,1)(6,6,2) (7,7,3)(8,8,4) | 5 |
| 62 | (5,0,0)(6,1,1)(7,2,2)(8,3,3) | 4 |
| 63 | (5,1,0)(6,2,1)(7,3,2)(8,4,3) | 4 |
| 64 | (5,2,0)(6,3,1)(7,4,2)(8,5,3) | 4 |
| 65 | (5,3,0)(6,4,1)(7,5,2)(8,6,3) | 4 |
| 66 | (5,4,0)(6,5,1)(7,6,2)(8,7,3) | 4 |
| 67 | (5,5,0)(6,6,1)(7,7,2)(8,8,3) | 4 |
| 92 | (6,0,0)(7,1,1)(8,2,2) | 3 |
| 93 | (6,1,0)(7,2,1)(8,3,2) | 3 |
| 94 | (6,2,0)(7,3,1) (8,4,2) | 3 |
| 95 | (6,3,0)(7,4,1) (8,5,2) | 3 |
| 96 | (6,4,0)(7,5,1) (8,6,2) | 3 |
| 97 | (6,5,0)(7,6,1) (8,7,2) | 3 |
| 98 | (6,6,0)(7,7,1) (8,8,2) | 3 |
| 128 | (7,0,0)(8,1,1) | 2 |
| 129 | (7,1,0)(8,2,1) | 2 |
| 130 | (7,2,0)(8,3,1) | 2 |
| 131 | (7,3,0)(8,4,1) | 2 |

| State No. | Combinations of three phases (a,b,c)# | Number of combinations |
|---|---|---|
| 132 | (7,4,0)(8,5,1) | 2 |
| 133 | (7,5,0)(8,6,1) | 2 |
| 134 | (7,6,0)(8,7,1) | 2 |
| 135 | (7,7,0)(8,8,1) | 2 |
| 170 | (8,0,0) | 1 |
| 171 | (8,1,0) | 1 |
| 172 | (8,2,0) | 1 |
| 173 | (8,3,0) | 1 |
| 174 | (8,4,0) | 1 |
| 175 | (8,5,0) | 1 |
| 176 | (8,6,0) | 1 |
| 177 | (8,7,0) | 1 |
| 178 | (8,8,0) | 1 |

Note: # a,b,c values 0,1,2,3,4,5,6,7 and 8 correspond to phase voltage levels of $-V_{DC}/2$, $-3V_{DC}/8$, $-V_{DC}/4$, $-V_{DC}/8$, 0, $+V_{DC}/8$, $+V_{DC}/4$, $+3V_{DC}/8$ and $+V_{DC}/2$.

### 5.3 Mathematical Modelling of Hybrid 9-Level Inverter

A mathematical model of the proposed hybrid 9-level inverter is developed based on switching states. The pole voltage $V_{A1O}$ of 5-level 'Inverter-A' in terms of switching states, capacitors voltage ($V_{CA1}$, $V_{CA2}$) and DC link voltage can be given as:

$$\begin{aligned} V_{A1O} &= \left\{\frac{V_{DC}}{2}S_{A1}S_{A2} + V_{CA1}S_{A2}(1-S_{A1}) + (\frac{V_{DC}}{2} - V_{CA1})S_{A1}(1-S_{A2})\right\}\times \\ &\quad \left\{S_{A3}S_{A4} + (1-S_{A3})(1-S_{A4}) + (1-S_{A3})S_{A4} + S_{A3}(1-S_{A4})\right\} + \\ &\quad V_{CA2}\left\{S_{A4}(1-S_{A3}) - S_{A3}(1-S_{A4})\right\} \\ &= \frac{V_{DC}}{2}S_{A1} + V_{CA1}(S_{A2} - S_{A1}) + V_{CA2}(S_{A4} - S_{A3}) \end{aligned} \tag{5.5}$$

Similarly the others pole voltages $V_{B1O}$ and $V_{C1O}$ can be written as:

$$\begin{aligned} V_{B1O} &= \left\{\frac{V_{DC}}{2}S_{B1}S_{B2} + V_{CB1}S_{B2}(1-S_{B1}) + (\frac{V_{DC}}{2} - V_{CB1})S_{B1}(1-S_{B2})\right\}\times \\ &\quad \left\{S_{B3}S_{B4} + (1-S_{B3})(1-S_{B4}) + (1-S_{B3})S_{B4} + S_{B3}(1-S_{B4})\right\} + \\ &\quad V_{CB2}\left\{S_{B4}(1-S_{B3}) - S_{B3}(1-S_{B4})\right\} \\ &= \frac{V_{DC}}{2}S_{B1} + V_{CB1}(S_{B2} - S_{B1}) + V_{CB2}(S_{B4} - S_{B3}) \end{aligned} \tag{5.6}$$

$$\begin{aligned} V_{C1O} &= \left\{\frac{V_{DC}}{2}S_{C1}S_{C2} + V_{CC1}S_{C2}(1-S_{C1}) + (\frac{V_{DC}}{2} - V_{CC1})S_{C1}(1-S_{C2})\right\}\times \\ &\quad \left\{S_{C3}S_{C4} + (1-S_{C3})(1-S_{C4}) + (1-S_{C3})S_{C4} + S_{C3}(1-S_{C4})\right\} + \\ &\quad V_{CC2}\left\{S_{C4}(1-S_{C3}) - S_{C3}(1-S_{C4})\right\} \\ &= \frac{V_{DC}}{2}S_{C1} + V_{CC1}(S_{C2} - S_{C1}) + V_{CC2}(S_{C4} - S_{C3}) \end{aligned} \tag{5.7}$$

The instantaneous value of capacitor voltage $V_{CXY}$ (X=A, B, C and Y =1,2) is given by equation (5.8).

$$V_{CXY} = \frac{1}{C_{XY}} \int i_{CXY} dt \tag{5.8}$$

Where, $i_{CXY}$ is the instantaneous current through the capacitor $C_{XY}$.

Similarly, two-level 'Inverter-B' pole voltages ($V_{A2O'}, V_{B2O'}, V_{C2O'}$) with respect to point-O' in terms of DC link voltages and switching states are given by equation (4.25).

$$\left.\begin{aligned} V_{A2O'} &= \frac{V_{DC}}{2} S_{A5} \\ V_{B2O'} &= \frac{V_{DC}}{2} S_{B5} \\ V_{C2O'} &= \frac{V_{DC}}{2} S_{C5} \end{aligned}\right\} \tag{5.9}$$

The three-phase motor voltages can be written in terms of pole as:

$$\begin{bmatrix} V_{A1A2} \\ V_{B1B2} \\ V_{C1C2} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} V_{A1O} - V_{A2O'} \\ V_{B1O} - V_{B2O'} \\ V_{C1O} - V_{C2O'} \end{bmatrix} \tag{5.10}$$

The relationship between orthogonal components $V_{qs}$, $V_{ds}$ of voltage space phasor in terms of phase voltages $V_{A2A4}$, $V_{B2B4}$, $V_{C2C4}$ is given by the transformation:

$$\begin{bmatrix} V_{qs} \\ V_{ds} \\ V_{os} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \begin{bmatrix} V_{A1A2} \\ V_{B1B2} \\ V_{C1C2} \end{bmatrix} \tag{5.11}$$

These d-q components acts as inputs for the open-end winding induction motor model developed in section 2.4.2, to calculate the motor phase currents.

### 5.4 Simulation Results and Discussion

The performance of proposed hybrid 9-level inverter scheme for open-end induction motor drive is evaluated in MATLAB/Simulink environment. The mathematical model of hybrid 9-level inverter is developed in MATLAB/Simulink environment using S-function and simulation study is carried out in fixed-point simulation mode at a sampling time of 10 µSec. The mathematical model of 1.5kW open-end winding induction motor describe in subsection 2.4.2 is developed in MATLAB/Simulink and used as load. The switching frequency ($f_c$) is kept constant at 1kHz and DC link voltage ($V_{DC}$) is taken as 600V for simulation analysis. The band of allowable ripple in capacitors voltage is selected as ±2 volt means the range of capacitor voltage $V_{CA1}$ varies from 148V to 152V and range of capacitor voltage $V_{CA2}$ is from 73V to 77V. The induction motor is operated in constant *V/f* mode under no-load condition covering the entire range of linear modulation. The modulation scheme and values of modulation index to obtain different levels of operation; are used same as they are in

Chapter-4 to compare the performance of both 9-level inverters. The limit of modulation index ($m$) for linear modulation is 0.866. The motor phase-A voltage ($V_{A1A2}$), phase-A current ($i_{A1A2}$), their harmonic spectrums, phase-A capacitors voltages ($V_{CA1}$, $V_{CA2}$), inverters pole-A voltages ($V_{A1O}$, $V_{A2O'}$) and difference of inverters pole-A voltages ($V_{A1O}$ - $V_{A2O'}$) are considered as evaluation criteria. The performance of hybrid 9-level inverter scheme and capacitors balancing are evaluated under steady-state as well as under transient-state conditions and results are presented in Fig. 5.14 - Fig. 5.56.

The motor phase-A voltage ($V_{A1A2}$), current ($i_{A1A2}$) and capacitors voltages ($V_{CA1}$, $V_{CA2}$) at modulation index $m$ =0.08 are shown in Fig. 5.14 and Fig. 5.15 respectively. At this modulation index motor operates at fundamental frequency ($f^*_m$) of 4Hz and capacitors voltages are balance at desired level within the allowable ripple of $\pm$2 volt. The phase-A voltage ($V_{A1A2}$) and current ($i_{A1A2}$) waveforms are equivalent to conventional two-level inverter (Fig. 5.14). The harmonic spectrum of phase-A voltage and current with respect to their fundamental component for the modulation index $m$ =0.08 are shown in Fig. 5.16 and Fig. 5.17 respectively. It is evident from these spectrums that the dominant harmonic component of phase voltage and current occur at the side band of 500 ($2f_c/f^*_m$ = 2*1000/4). Lower order harmonics responsible for higher losses are significantly very low.

The pole-A voltages ($V_{A1O}$, $V_{A2O'}$) and difference of these pole voltages ($V_{A1O}$ - $V_{A2O'}$) are shown in Fig. 5.18 for two-level mode of operation. It may be observed from pole voltages waveform that 5-level inverter-A operates in two-level mode (0 and $V_{DC}$/8) while the inverter-B is clamped at $V_{DC}$/2 (300V) voltage level. The difference of pole voltages ($V_{A1O}$ - $V_{A2O'}$) switch between two voltage levels -300V and -225V correspond to $-V_{DC}/2$ and $-(3/8)V_{DC}$.

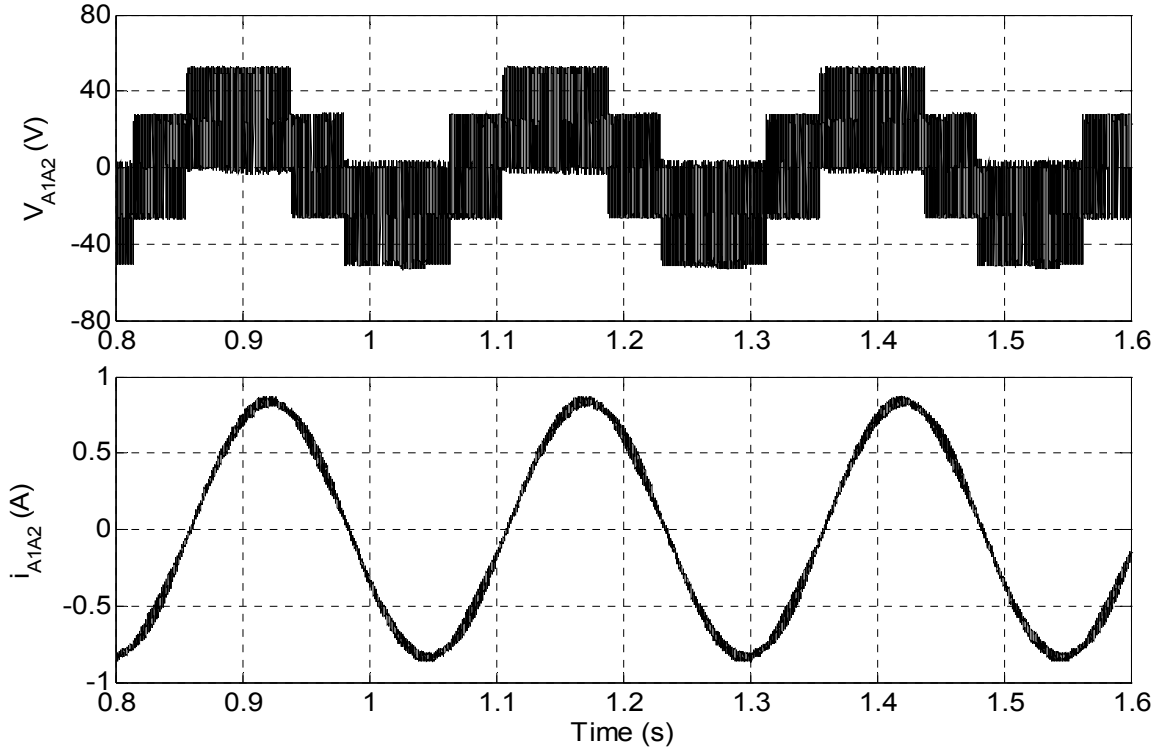



Fig. 5.14: Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A1A2}$ (lower trace) of hybrid 9-level inverter fed open-end IM drive at no load ($m$=0.08; $f^*_m$ =4Hz; 2-level mode)

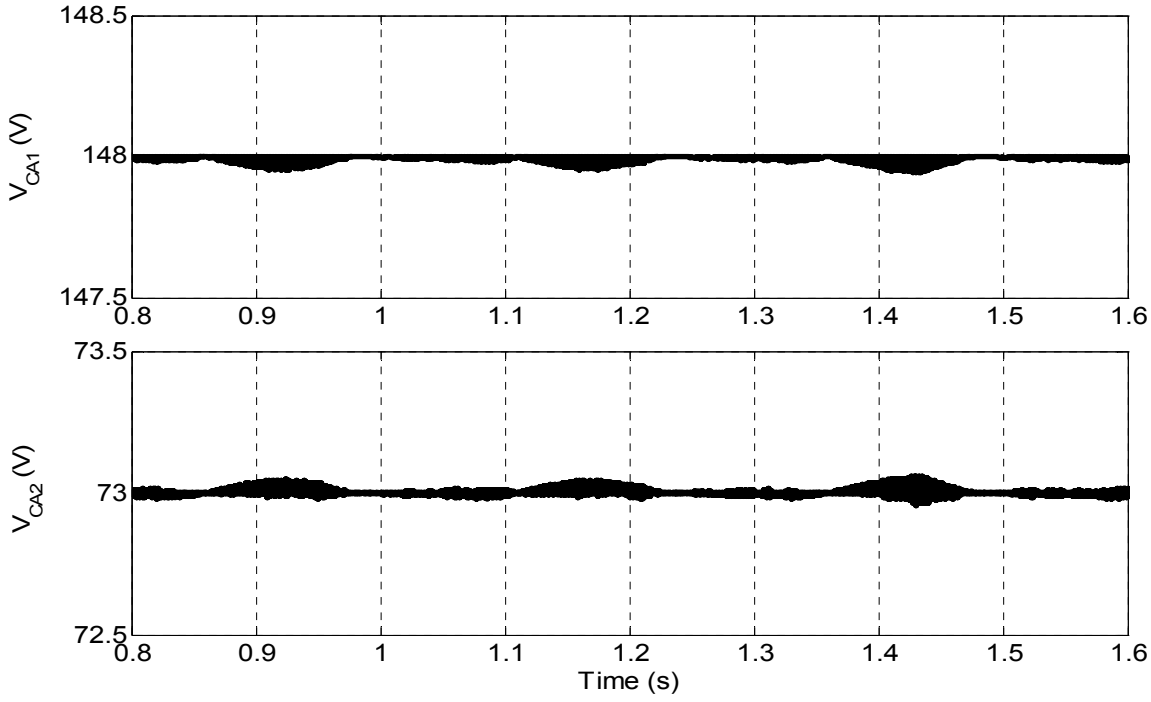



Fig. 5.15: Capacitors voltages $V_{CA1}$ (upper trace) and $V_{CA2}$ (lower trace) in 2-level mode

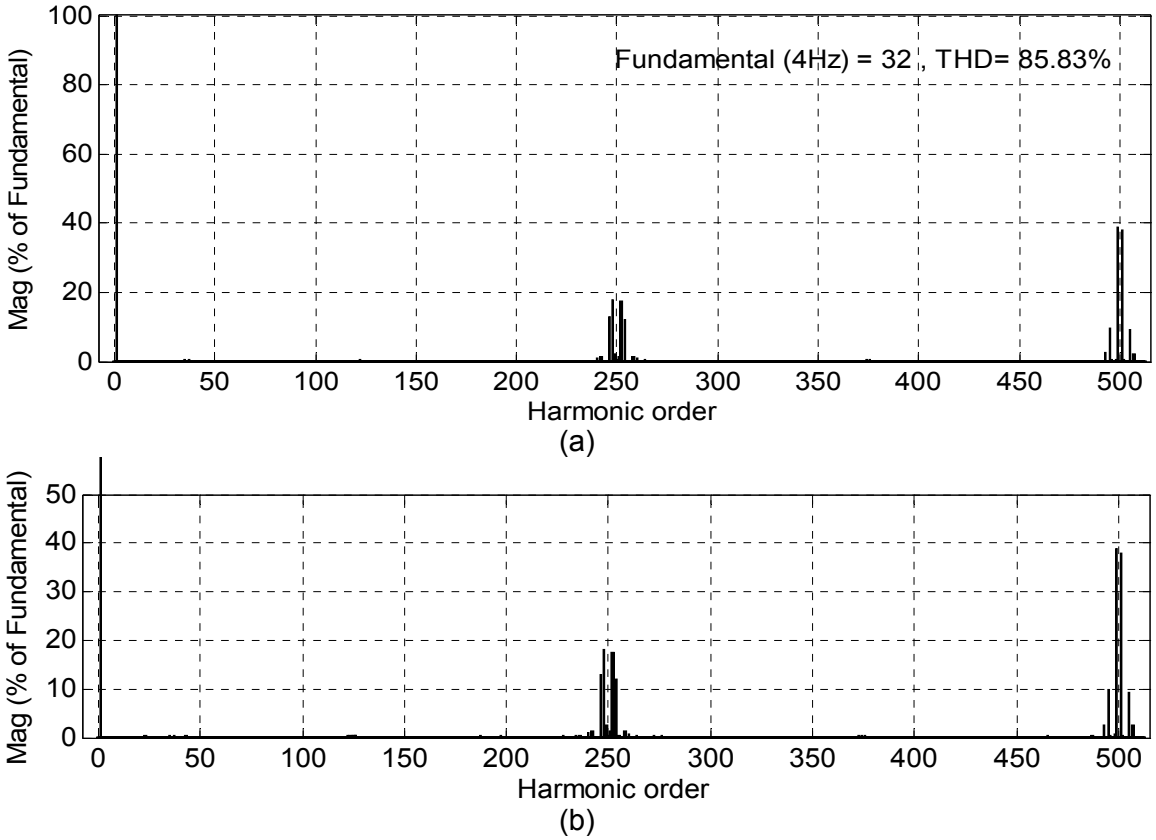



Fig. 5.16: (a) Harmonic spectrum of phase-A voltage ($V_{A1A2}$) at $m$=0.08; $f^*_m$ =4Hz
(b) Zoom view of harmonic spectrum shown in (a)

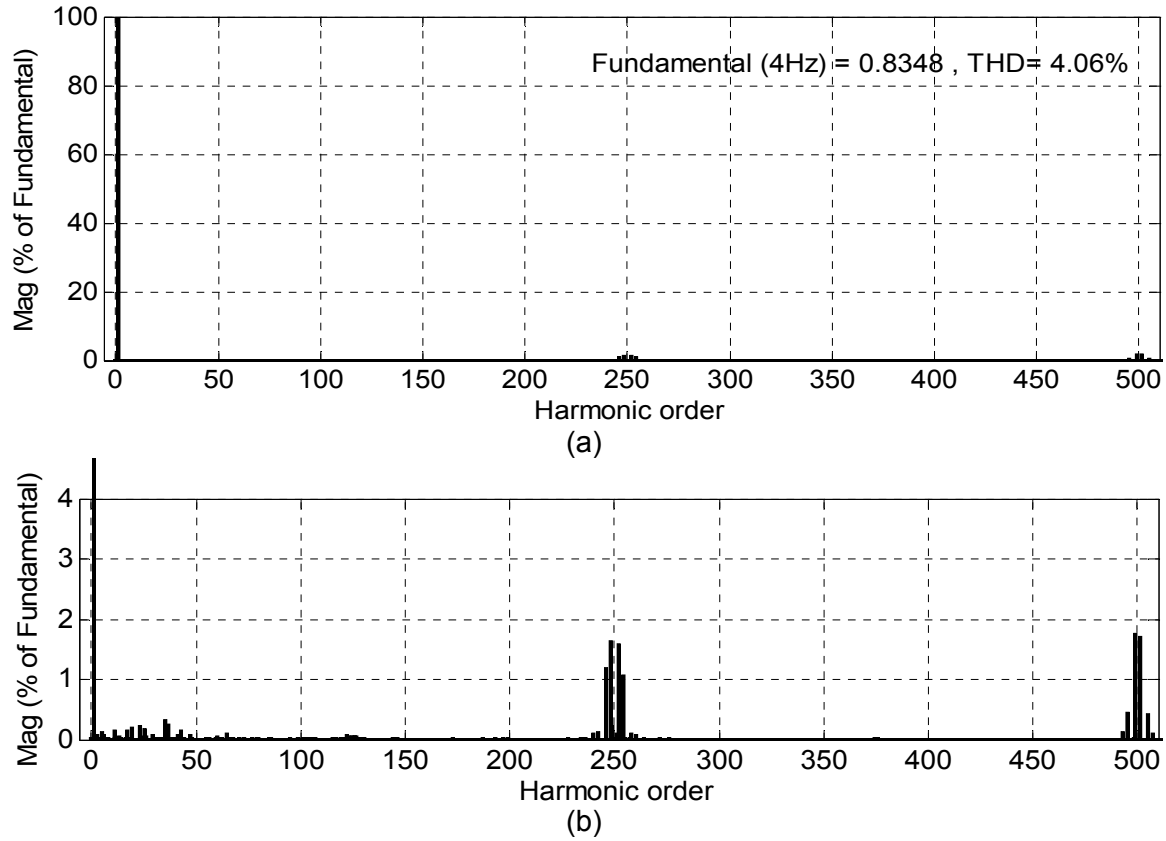



Fig. 5.17: (a) Harmonic spectrum of phase-A current ($i_{A1A2}$) at $m$=0.08; $f^*_m$ =4Hz
(b) Zoom view of harmonic spectrum shown in (a)

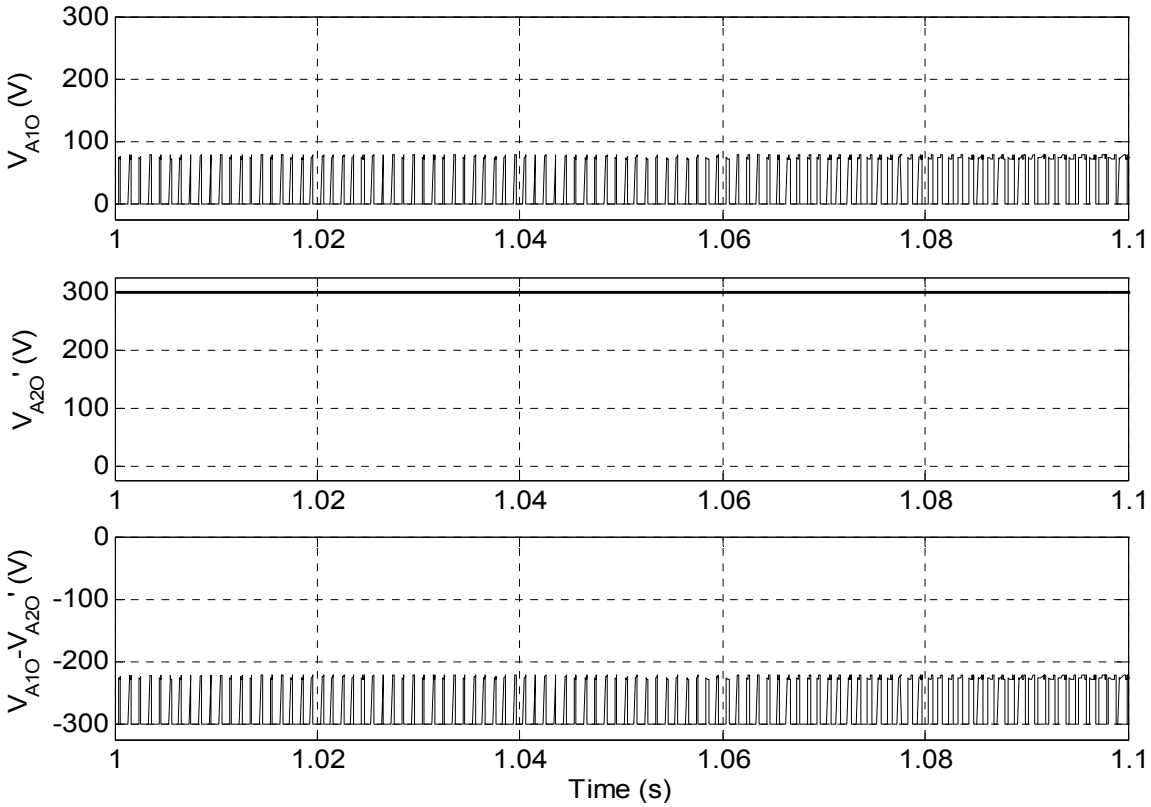



Fig. 5.18: Top trace; Inverter-A pole voltage ($V_{A1O}$), Middle trace; Inverter-B pole voltage ($V_{A2O'}$), Bottom trace; Difference of Inverter-A and -B pole voltages ($V_{A1O}$ - $V_{A2O'}$) at $m$=0.08; $f^*_m$ =4Hz (2-level mode)

The simulation results for motor phase-A voltage ($V_{A1A2}$), phase-A current ($i_{A1A2}$), capacitors voltages ($V_{CA1}$, $V_{CA2}$), harmonic spectrums of phase-A voltage and current, inverters pole-A voltages ($V_{A1O}$, $V_{A2O'}$) and difference of inverters pole-A voltages ($V_{A1O}$ - $V_{A2O'}$) at modulation index $m$ =0.16 are shown in Fig. 5.19-Fig. 5.23. At this modulation index the modulating signals situated within the levels $L_1$ - $L_3$ and inverter operates in 3-level mode of operation. The fundamental frequency ($f^*_m$) of the motor for this modulation index is 8Hz. The motor phase-A voltage ($V_{A1A2}$) and current ($i_{A1A2}$) at modulation index $m$ =0.16 shown in Fig. 5.19 are similar to the waveforms achieved for 9-level inverter proposed in Chapter-4. The capacitors voltages $V_{CA1}$ and $V_{CA2}$ are well balanced as depicted in Fig. 5.20. As compared to two-level mode of operation, the THD of phase voltage is reduced to 41.18% from 85.83% and dominant harmonic component occur at the side band of 250$^{th}$ ($2f_c/f^*_m$ = 2*1000/8) order as shown in Fig. 5.21. The distortion in phase current is only 2.77% as shown in Fig. 5.22.

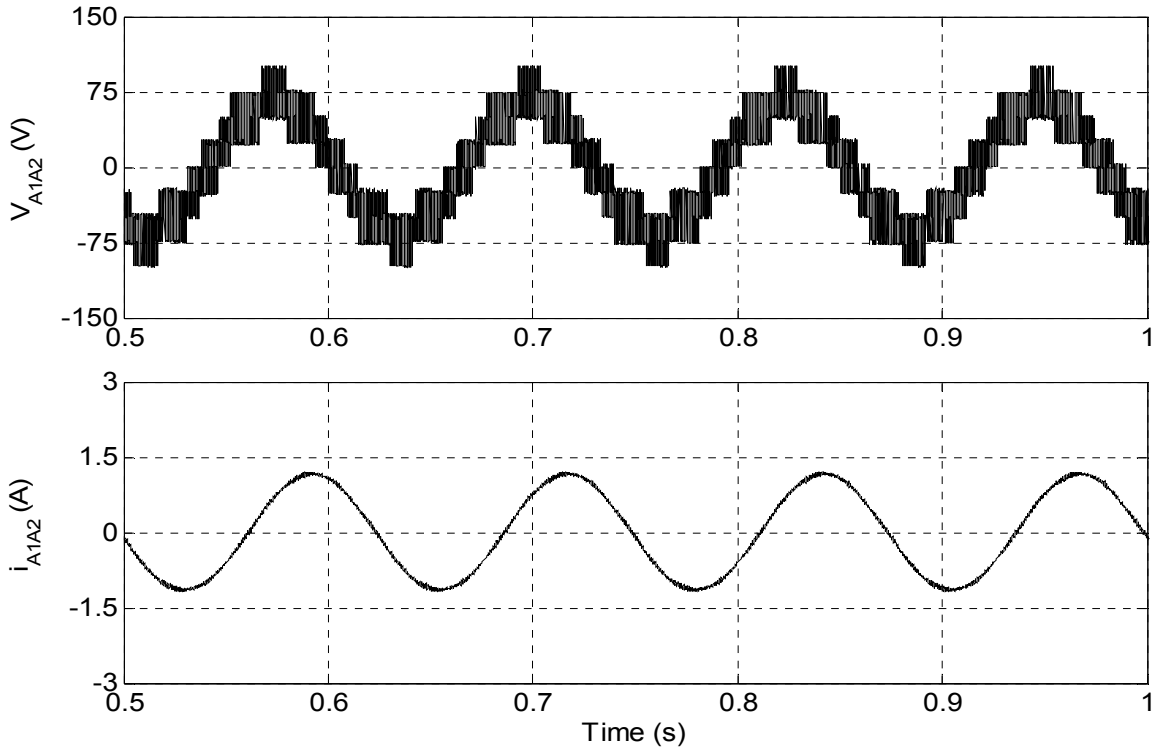



Fig. 5.19: Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A1A2}$ (lower trace) of hybrid 9-level inverter fed open-end IM drive at no load ($m$=0.16; $f^*_m$ =8Hz; 3-level mode)

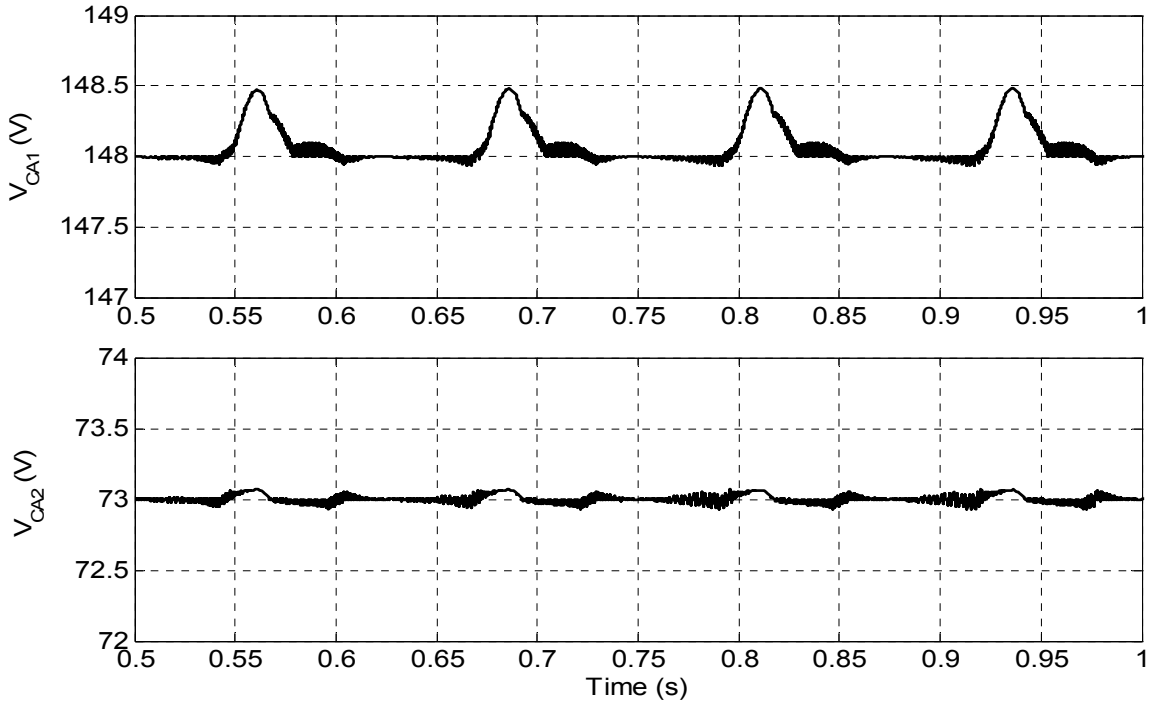



Fig. 5.20: Capacitors voltages $V_{CA1}$ (upper trace) and $V_{CA2}$ (lower trace) in 3-level mode

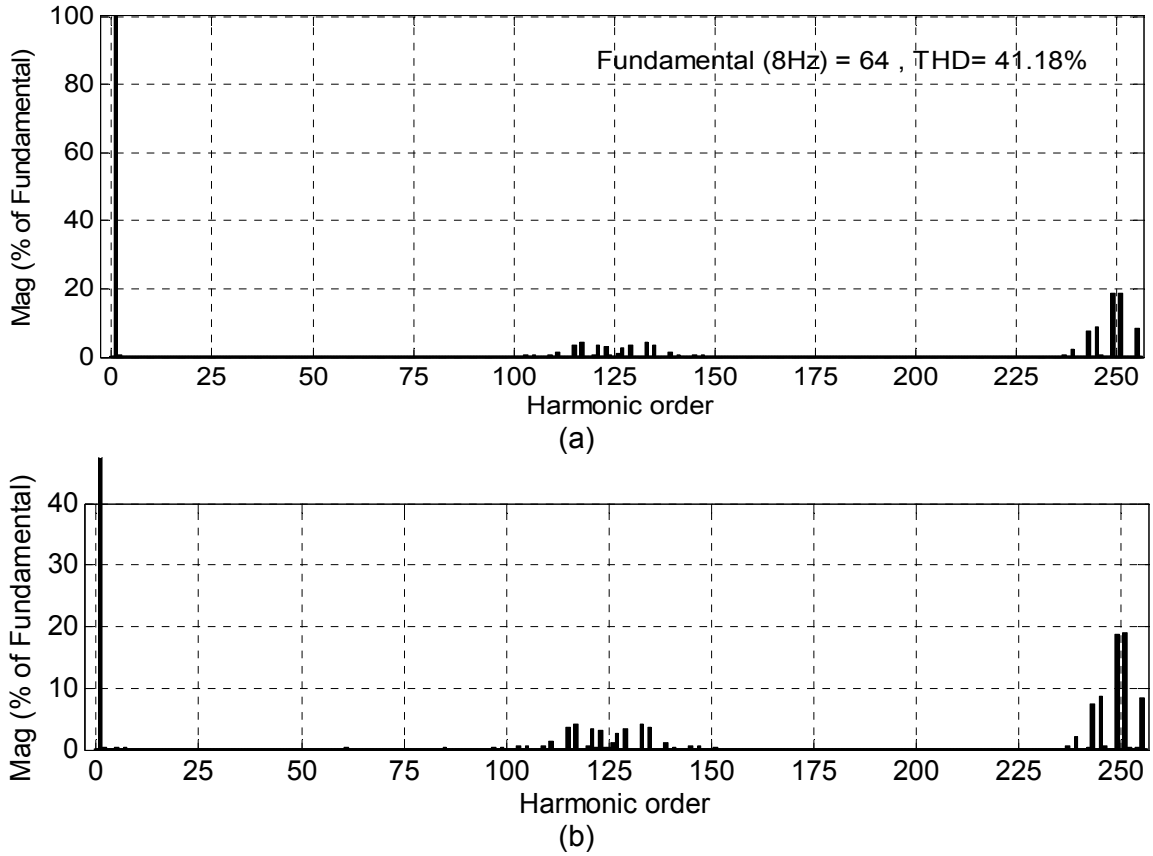



Fig. 5.21: (a) Harmonic spectrum of phase-A voltage ($V_{A1A2}$) at $m$=0.16; $f^*_m$ =8Hz
(b) Zoom view of harmonic spectrum shown in (a)

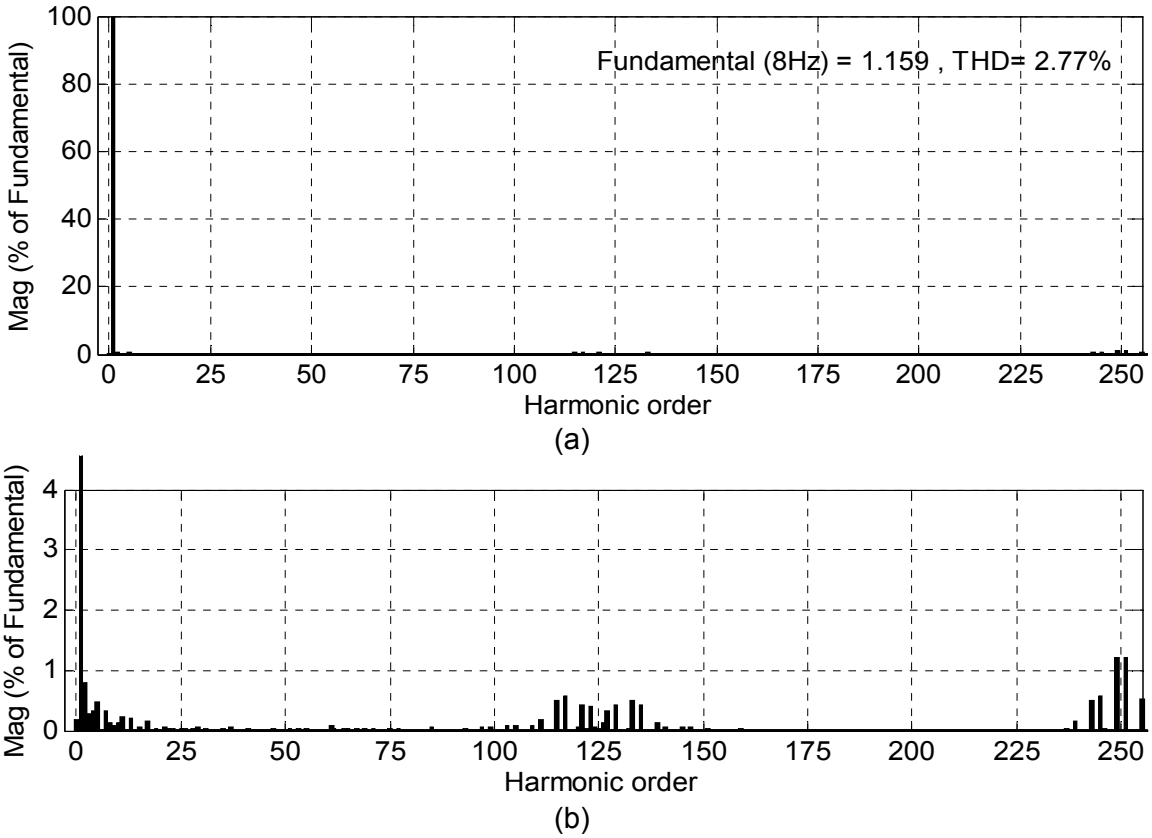



Fig. 5.22: (a) Harmonic spectrum of phase-A current ($i_{A1A2}$) at $m$=0.16; $f^*_m$ =8Hz
(b) Zoom view of harmonic spectrum shown in (a)

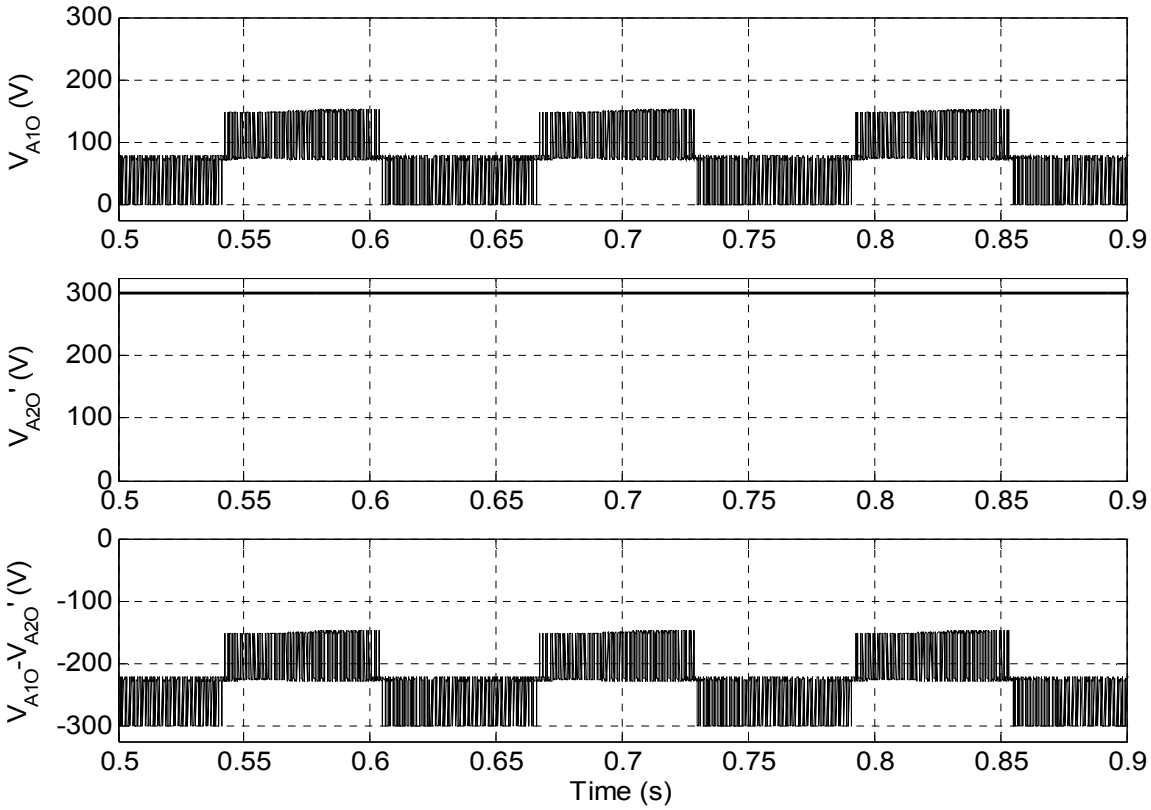



Fig. 5.23: Top trace; Inverter-A pole voltage ($V_{A1O}$), Middle trace; Inverter-B pole voltage ($V_{A2O'}$), Bottom trace; Difference of Inverter-A and -B pole voltages ($V_{A1O}$ - $V_{A2O'}$) at $m$=0.16; $f^*_m$ =8Hz (3-level mode)

The pole-A voltages ($V_{A1O}$, $V_{A2O'}$) and difference of these pole voltages ($V_{A1O}$ - $V_{A2O'}$) are shown in Fig. 5.23 for 3-level mode of operation. It may be observed from the pole voltages waveform that 5-level inverter-A operates in 3-level mode and gives the voltage level of 0, 75 and 150 correspond to 0, $V_{DC}/8$ and $2V_{DC}/8$ while the inverter-B is still clamped at 300V ($V_{DC}/2$). The difference of pole voltages ($V_{A1O}$ - $V_{A2O'}$) having three distinct voltage levels - $V_{DC}/2$, -(3/8)$V_{DC}$ and -(1/8)$V_{DC}$.

The simulation results correspond to modulation index $m$=0.28 and fundamental frequency $f^*_m$=14Hz are presented in Fig. 5.24-Fig. 5.28. In this range the modulating signals cover four levels $L_1$ - $L_4$ and inverter operates in 4-level mode of operation. It can be observed in Fig. 5.28 that the difference in pole voltage ($V_{A1O}$ - $V_{A2O'}$) possess four distinct levels -$V_{DC}/2$, -(3/8)$V_{DC}$, -(1/4)$V_{DC}$ and -(1/8)$V_{DC}$. It is also evident from Fig. 5.28 that in 4-level mode 5-level inverter-A operates in 4-level mode and gives the voltage level of 0, 75, 150 and 225 (0, $V_{DC}/8$, $V_{DC}/4$ and $3V_{DC}/8$) while the inverter-B is still clamped at 300V ($V_{DC}/2$). The THD of phase voltage (Fig. 5.26) and current (Fig. 5.27) are 8.52% and 1.16% respectively and dominant harmonic component occur approximately at the side band of 143$^{rd}$ ($2f_c/f^*_m$ = 2*1000/14). The ripple in capacitor voltage $V_{CA1}$ is little bit increase as compared to 3-level mode of operation, but within the allowable limit (Fig. 5.25). The motor phase-A voltage ($V_{A1A2}$) and current ($i_{A1A2}$) waveforms are shown in Fig. 5.24.

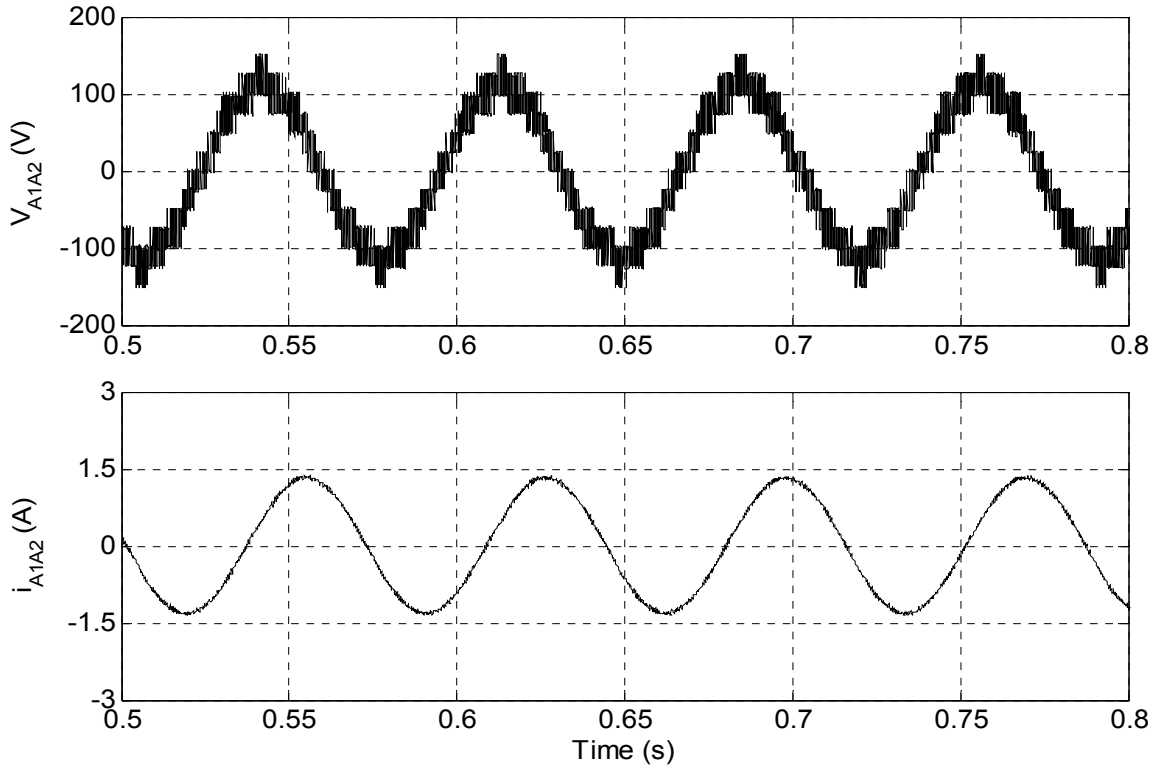



Fig. 5.24: Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A2A4}$ (lower trace) of hybrid 9-level inverter fed open-end IM drive at no load ($m$=0.28; $f^*_m$=14Hz; 4-level mode)

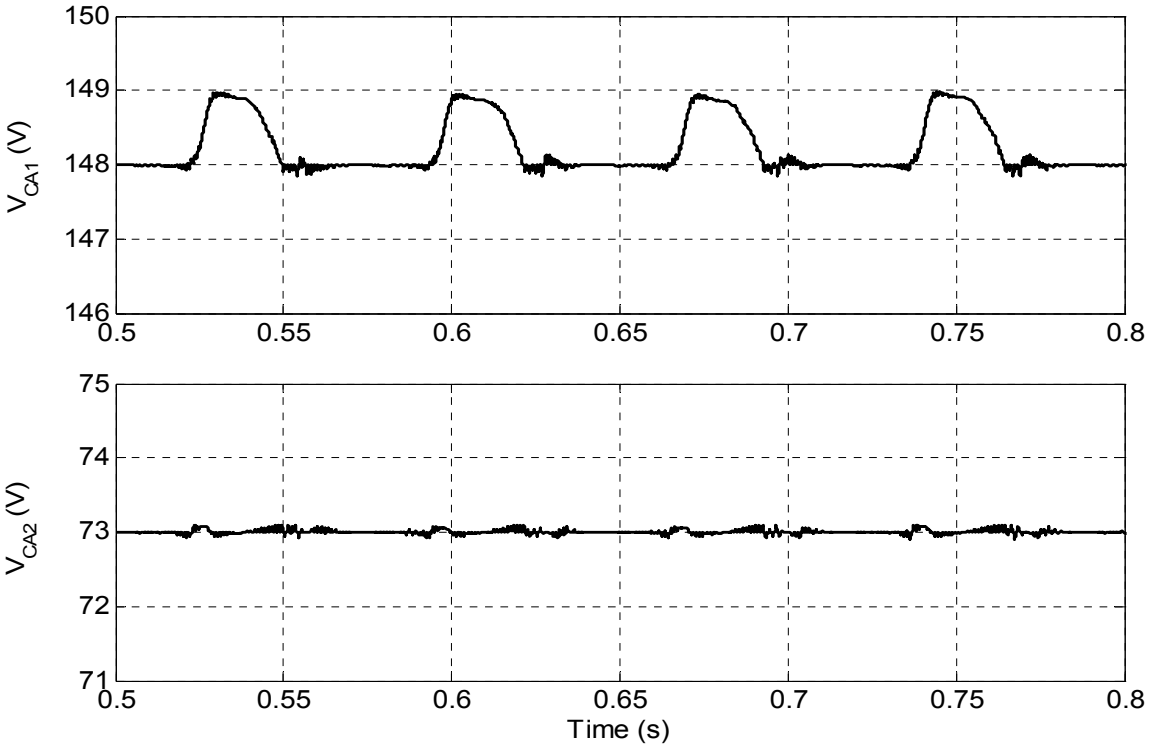



Fig. 5.25: Capacitors voltages $V_{CA1}$ (upper trace) and $V_{CA2}$ (lower trace) in 4-level mode

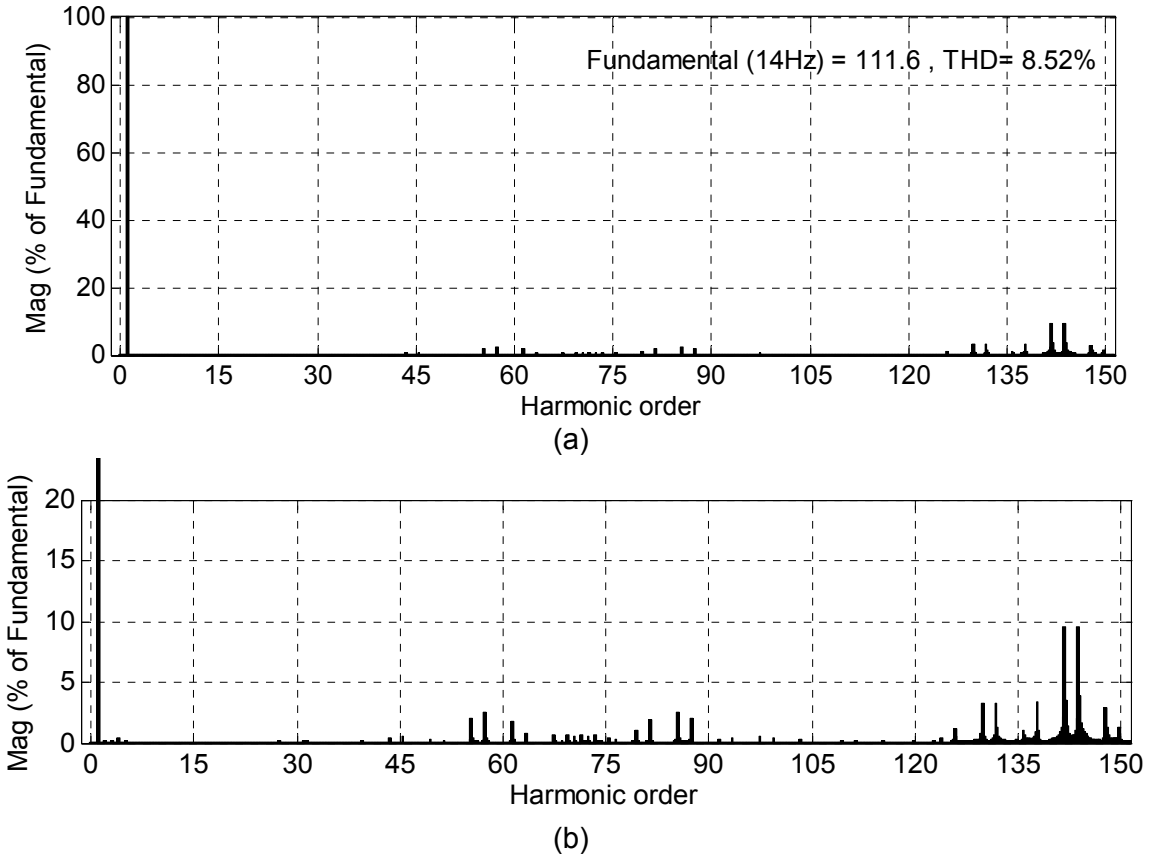
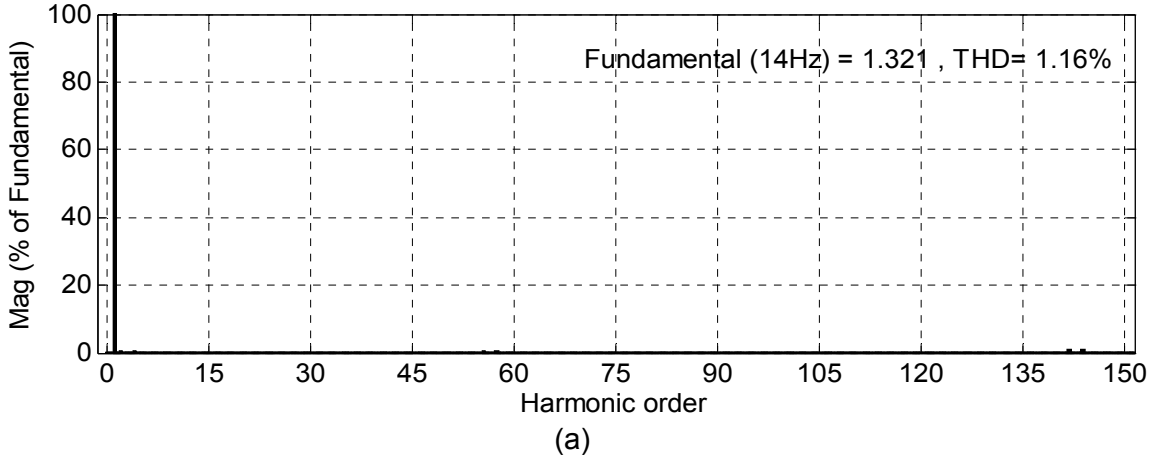
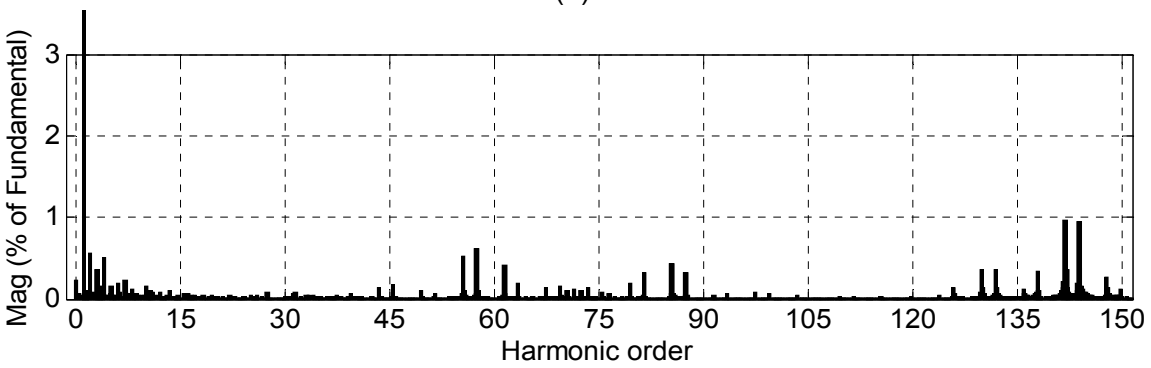



Fig. 5.26: (a) Harmonic spectrum of phase-A voltage ($V_{A1A2}$) at $m$=0.28; $f^*_m$ =14Hz
(b) Zoom view of harmonic spectrum shown in (a)




(a)




(b)

Fig. 5.27: (a) Harmonic spectrum of phase-A current ($i_{A1A2}$) at $m$=0.28; $f^*_m$ =14Hz
(b) Zoom view of harmonic spectrum shown in (a)

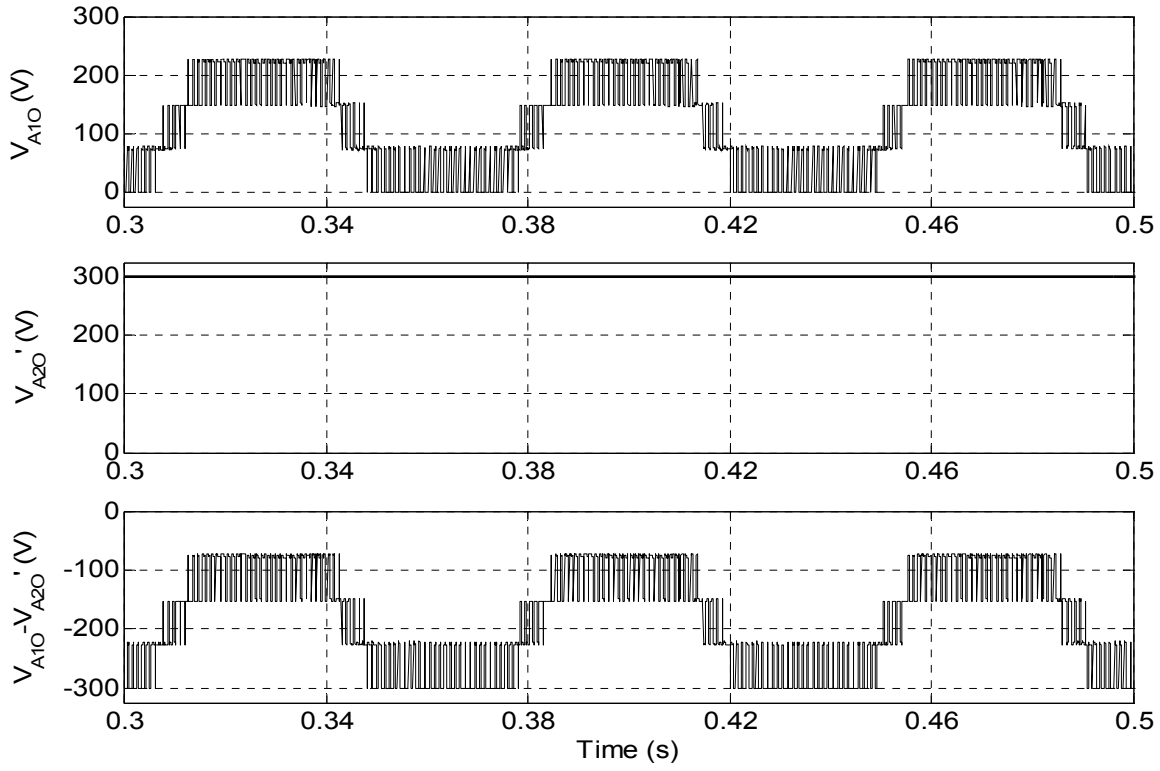



Fig. 5.28 :Top trace; Inverter-A pole voltage ($V_{A2O}$), Middle trace; Inverter-B pole voltage ($V_{A4O'}$), Bottom trace; Difference of Inverter-A and -B pole voltages ($V_{A2O}$ - $V_{A4O'}$) at $m$=0.28; $f^*_m$ =14Hz (4-level mode)

Fig. 5.29 through Fig. 5.33 illustrate the simulation results obtain when inverter is operated at modulation index $m$=0.36. In this case, inverter operates in 5-level mode and five levels realised in this mode are -300, -225, -150, -75 and 0 ($-V_{DC}/2$, $-3V_{DC}/8$, $-V_{DC}/4$, $-V_{DC}/8$ and 0) as shown in difference of pole voltage ($V_{A2O}$ - $V_{A4O'}$) waveform (Fig. 5.33 lower trace). It is depicted in Fig. 5.33 that in this mode, 5-level inverter-A switch between 5-levels whereas inverter-B is clamped at $V_{DC}/2$ (300V). The phase-A voltage, current and capacitors voltages ($V_{CA1}$, $V_{CA2}$) are shown in Fig. 5.29 and Fig. 5.30 respectively. The THD of phase voltage (Fig. 5.31) is reduced to 6.86% whereas THD of phase current (Fig. 5.32) is only 1.14% of the fundamental component ($f^*_m$=18Hz). The dominant harmonic component approximately occur at the side band of 111$^{th}$ ($2f_c/f^*_m$ = 2*1000/18) order.

Similar types of waveforms for 6-level mode of operation at modulation index $m$=0.42 are shown in Fig. 5.34 - Fig. 5.38. At this modulation index modulating signals cover levels $L_1$ - $L_6$ results 6-level mode of operation and motor is operated at fundamental frequency ($f^*_m$) of 21Hz. Motor phase-A voltage and current are shown in Fig. 5.34. The capacitors voltages are well balanced (Fig. 5.35). The harmonic spectrum of phase voltage (Fig. 5.36) and current (Fig. 5.37) are further improved and position of occurrence of dominant harmonic is approximately at the side band of 96$^{th}$ ($2f_c/f^*_m$ = 2*1000/21) order. It is depicted from pole voltages waveforms shown in Fig. 5.38 that 5-level inverter-A operates in 5-level mode and inverter-B started to operate in two-level mode. The six levels realised in this mode are -300, -225, -150, -75, 0 and +75 correspond to $-V_{DC}/2$, $-3V_{DC}/8$, $-V_{DC}/4$, $-V_{DC}/8$, 0 and $+V_{DC}/8$.

Another set of simulation results at modulation index $m$=0.52 in shown in Fig. 5.39 through Fig. 5.43 in same order as the previous set of results. Inverter operates in 7-level mode at fundamental frequency ($f^*_m$) of 26Hz at $m$=0.52. Motor phase voltage and current are shown in Fig. 5.39. The ripple in capacitors voltage ($V_{CA1}$, $V_{CA2}$) is less than 1V as shown in Fig. 5.40. It may be observed from pole voltages waveforms in Fig. 5.43 that the inverter which operates at higher DC link switch less hence low switching frequency rating power semiconductor devices can be used for two-level inverter-B. The seven distinct voltage levels obtain in this mode are -300, -225, -150, -75, 0, +75 and +150 correspond to $-V_{DC}/2$, $-3V_{DC}/8$, $-V_{DC}/4$, $-V_{DC}/8$, 0, $+V_{DC}/8$ and $+V_{DC}/4$ as depicted in difference of pole voltage ($V_{A1O}$ - $V_{A2O'}$) waveform (Fig. 5.43). The harmonic spectrum of phase voltage and current are shown in Fig. 5.41 and Fig. 5.42 respectively. The occurrence of dominant harmonic component in the spectrum of phase voltage is in same pattern as in the previous cases and it is found that lower order harmonics are increased in phase current.

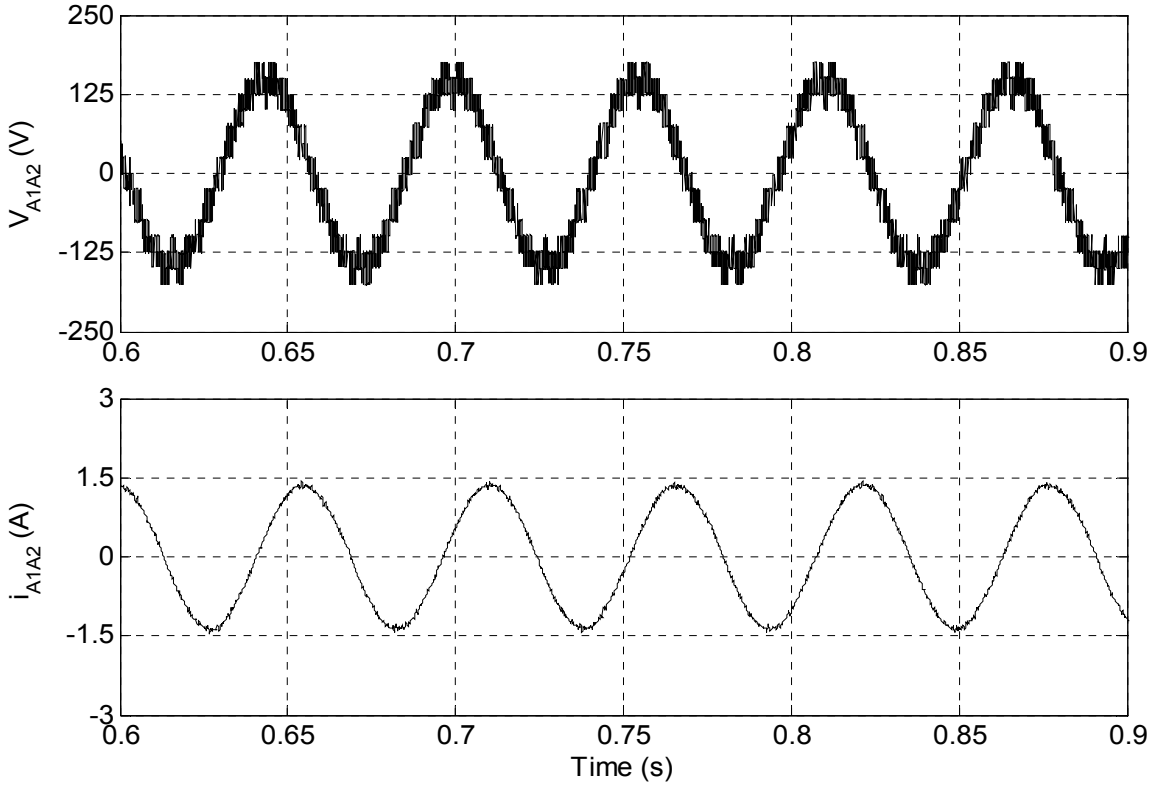



Fig. 5.29: Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A2A2}$ (lower trace) of hybrid 9-level inverter fed open-end IM drive at no load ($m$=0.36; $f^*_m$ =18Hz; 5-level mode)

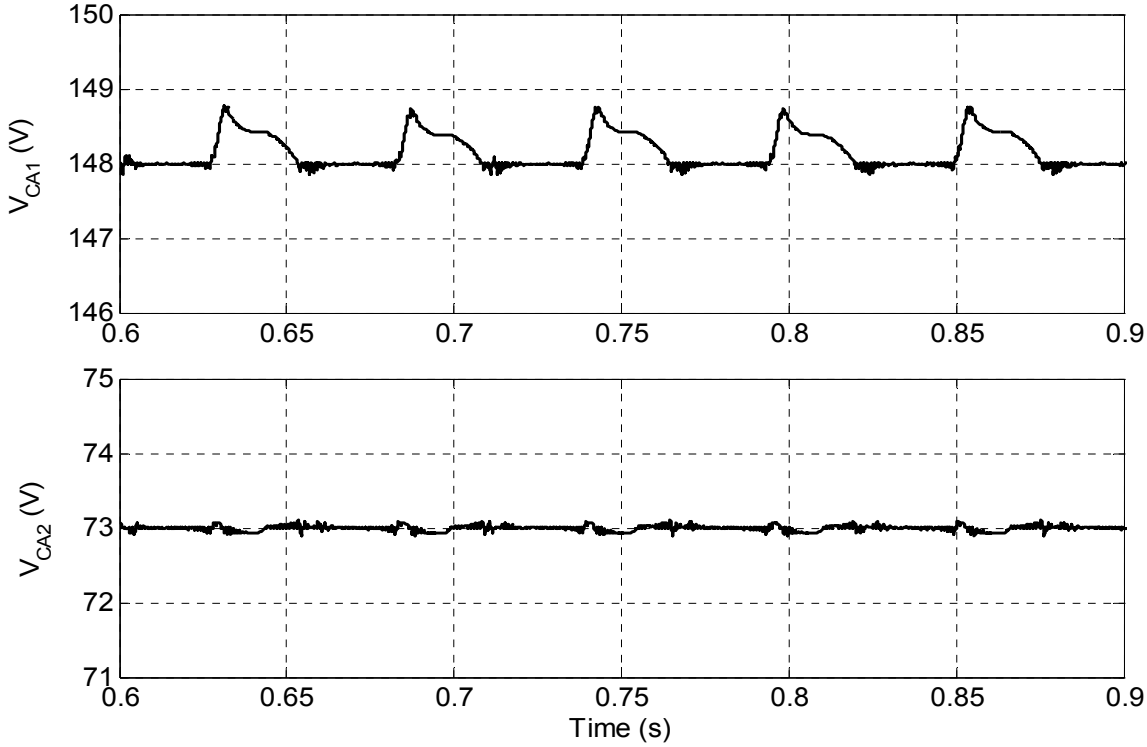



Fig. 5.30: Capacitors voltages $V_{CA1}$ (upper trace) and $V_{CA2}$ (lower trace) in 5-level mode

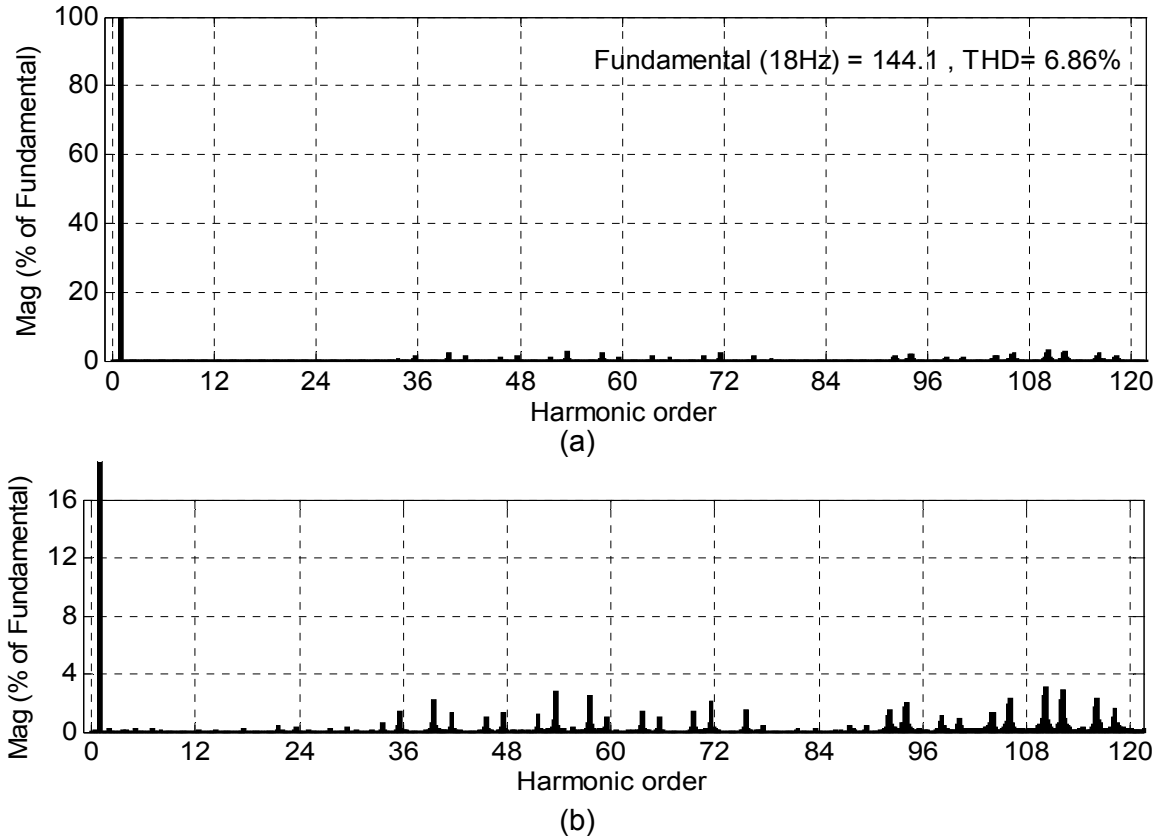



Fig. 5.31: (a) Harmonic spectrum of phase-A voltage ($V_{A1A2}$) at $m$=0.36; $f^*_m$ =18Hz
(b) Zoom view of harmonic spectrum shown in (a)

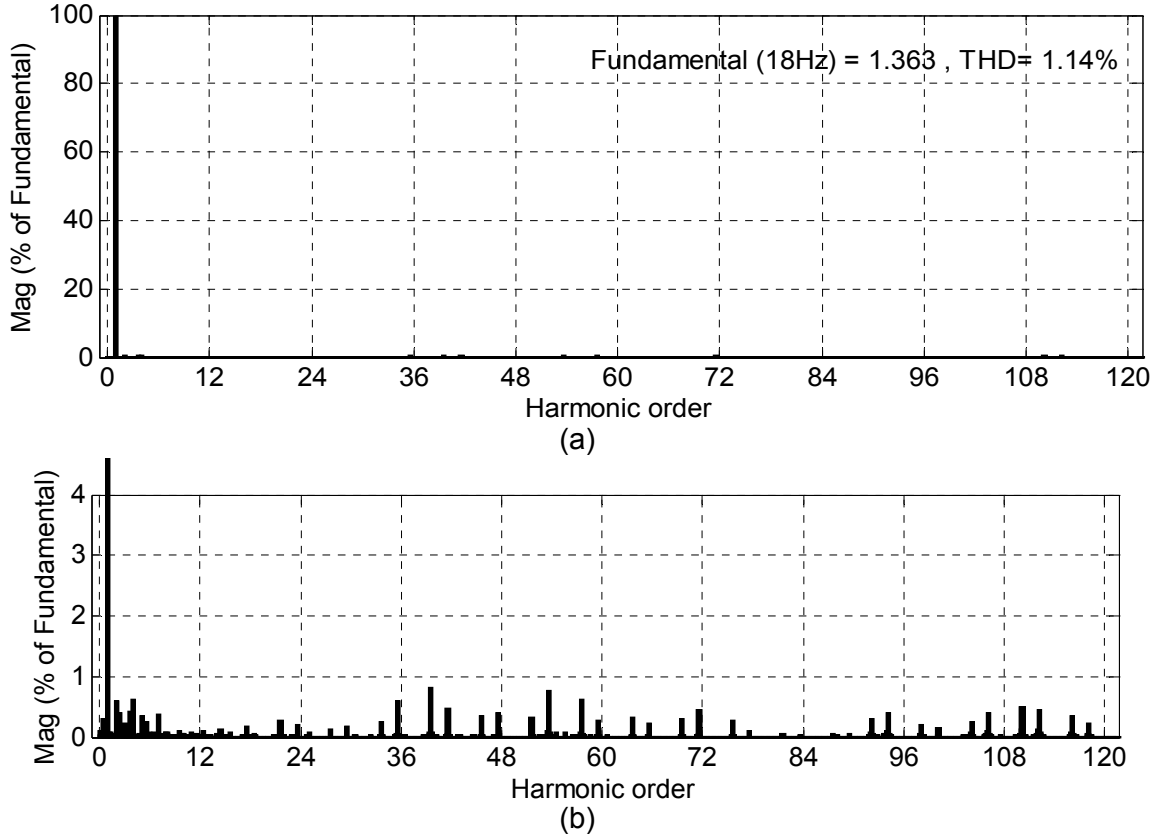



Fig. 5.32: (a) Harmonic spectrum of phase-A current ($i_{A1A2}$) at $m$=0.36; $f^*_m$ =18Hz
(b) Zoom view of harmonic spectrum shown in (a)

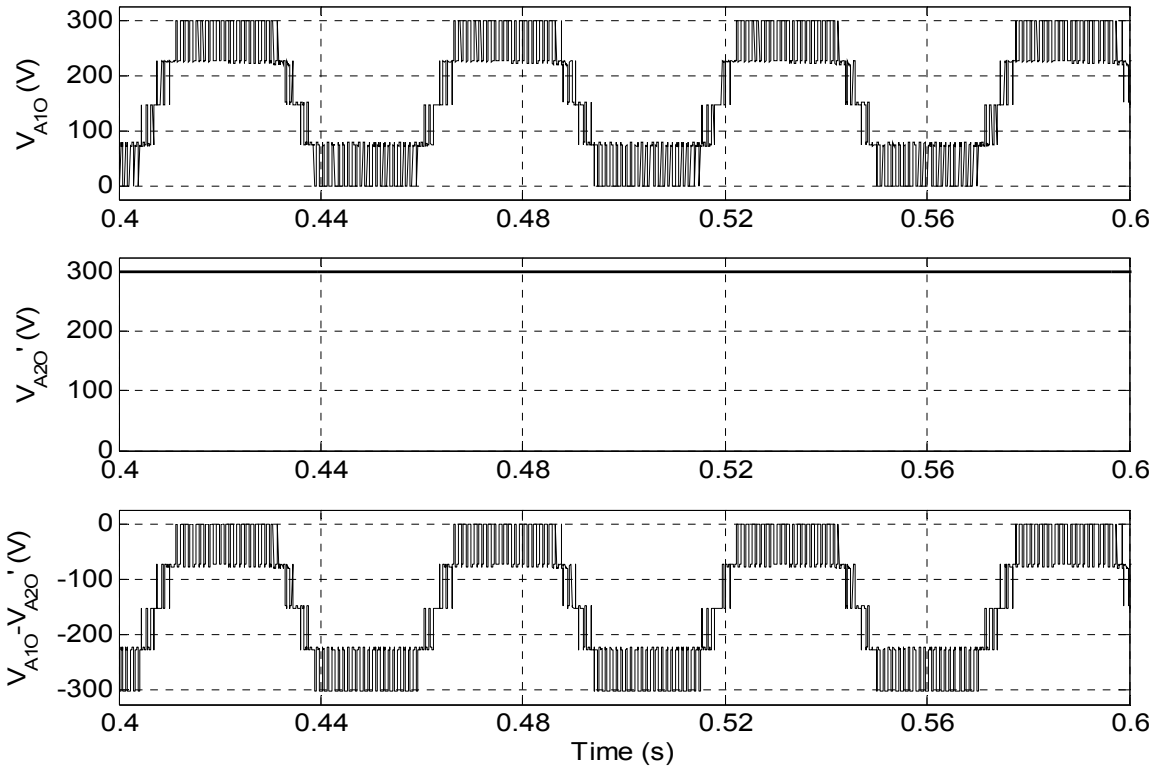



Fig. 5.33 :Top trace; Inverter-A pole voltage ($V_{A1O}$), Middle trace; Inverter-B pole voltage ($V_{A2O'}$), Bottom trace; Difference of Inverter-A and -B pole voltages ($V_{A1O}$ - $V_{A2O'}$) at $m$=0.36; $f^*_m$ =18Hz (5-level mode)

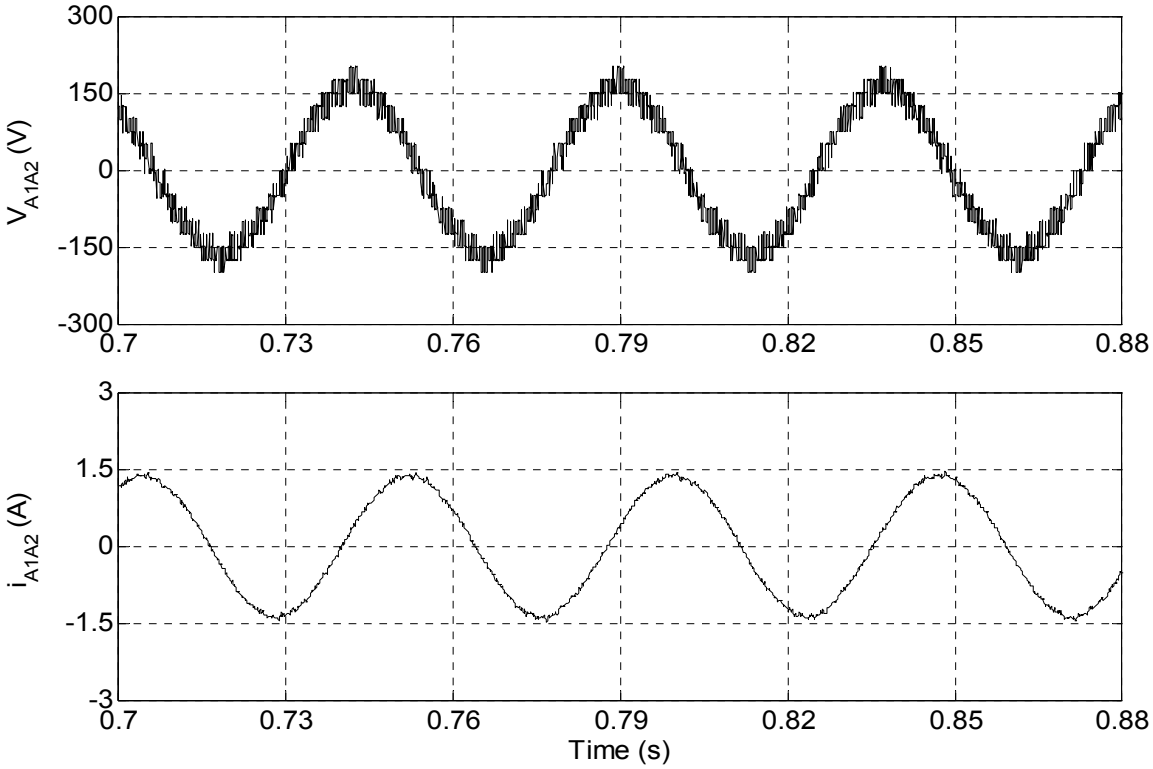



Fig. 5.34: Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A1A2}$ (lower trace) of hybrid 9-level inverter fed open-end IM drive at no load ($m$=0.42; $f^*_m$ =21Hz; 6-level mode)

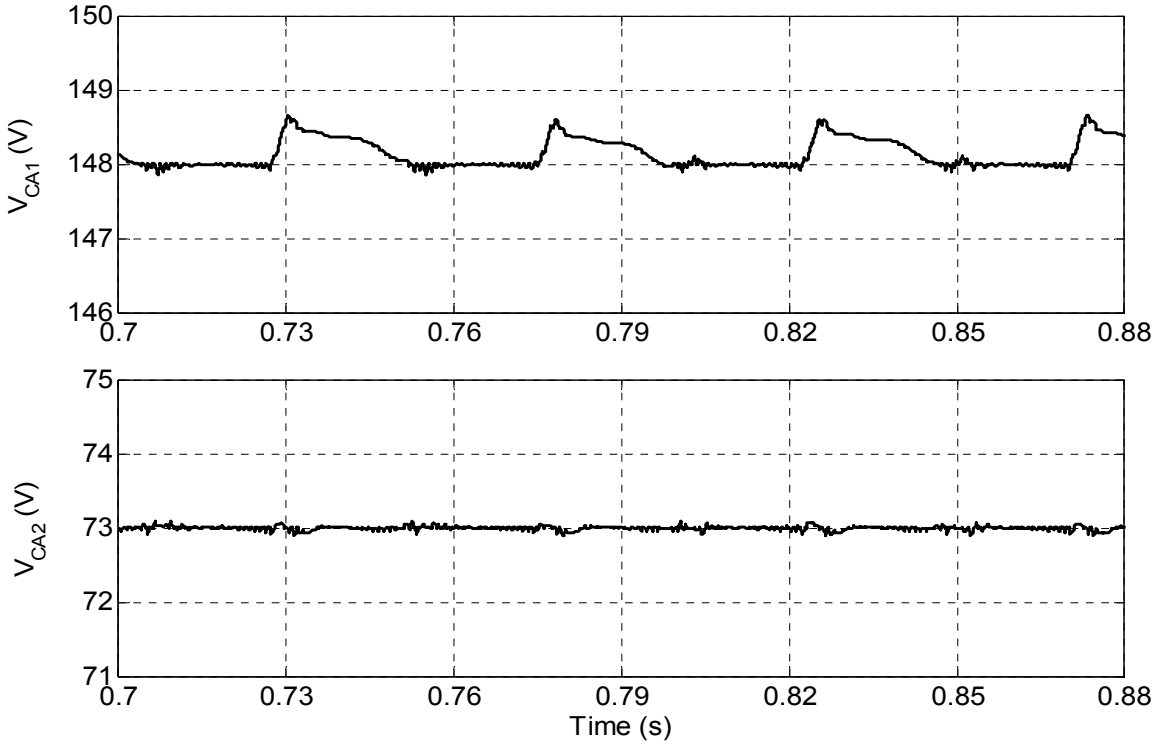



Fig. 5.35: Capacitors voltages $V_{CA1}$ (upper trace) and $V_{CA2}$ (lower trace) in 6-level mode

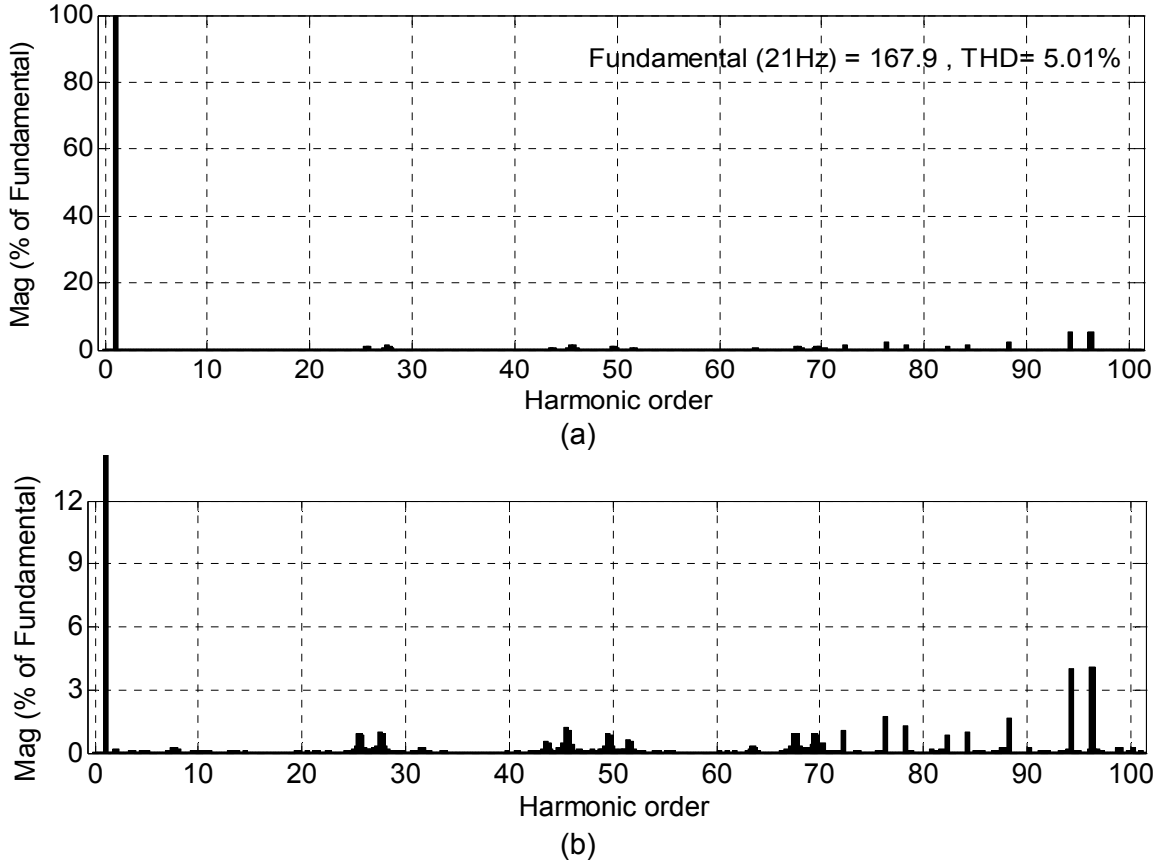



Fig. 5.36: (a) Harmonic spectrum of phase-A voltage ($V_{A1A2}$) at $m$=0.42; $f^*_m$ =21Hz
(b) Zoom view of harmonic spectrum shown in (a)

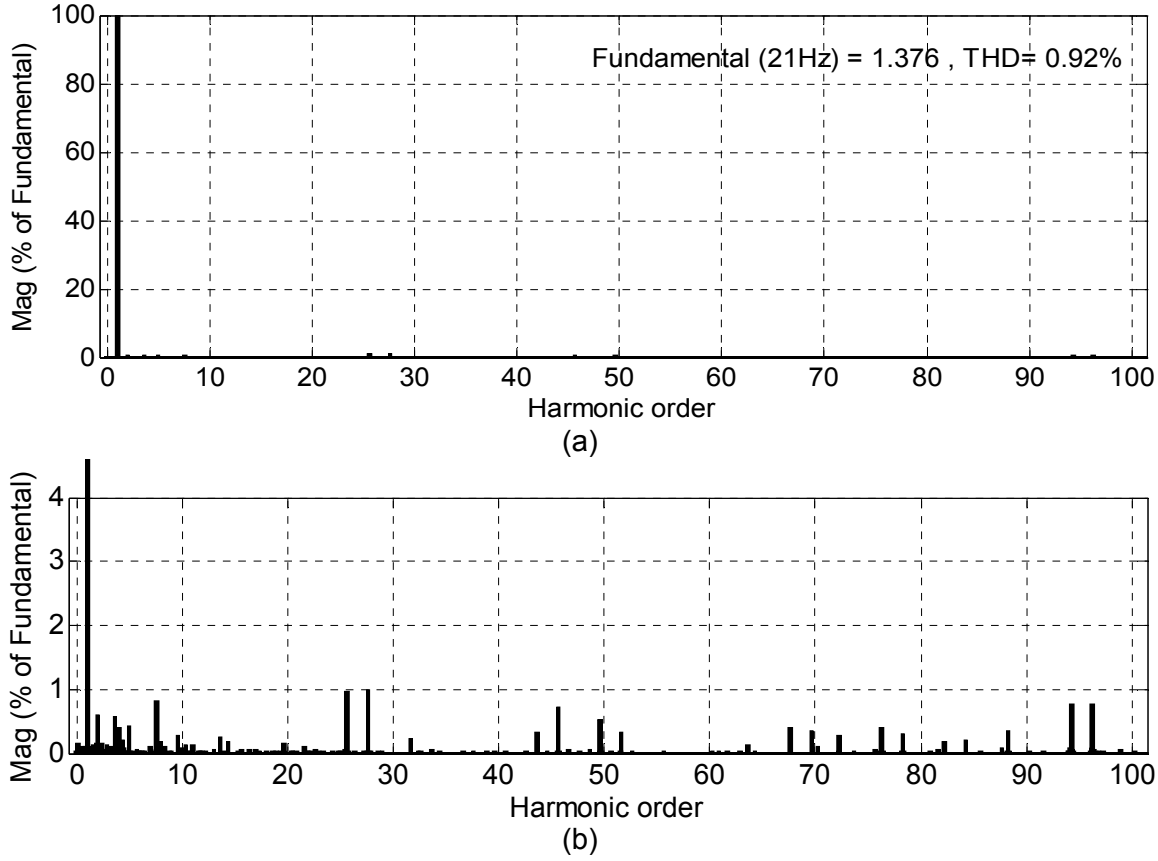



Fig. 5.37: (a) Harmonic spectrum of phase-A current ($i_{A1A2}$) at $m$=0.42; $f^*_m$ =21Hz
(b) Zoom view of harmonic spectrum shown in (a)

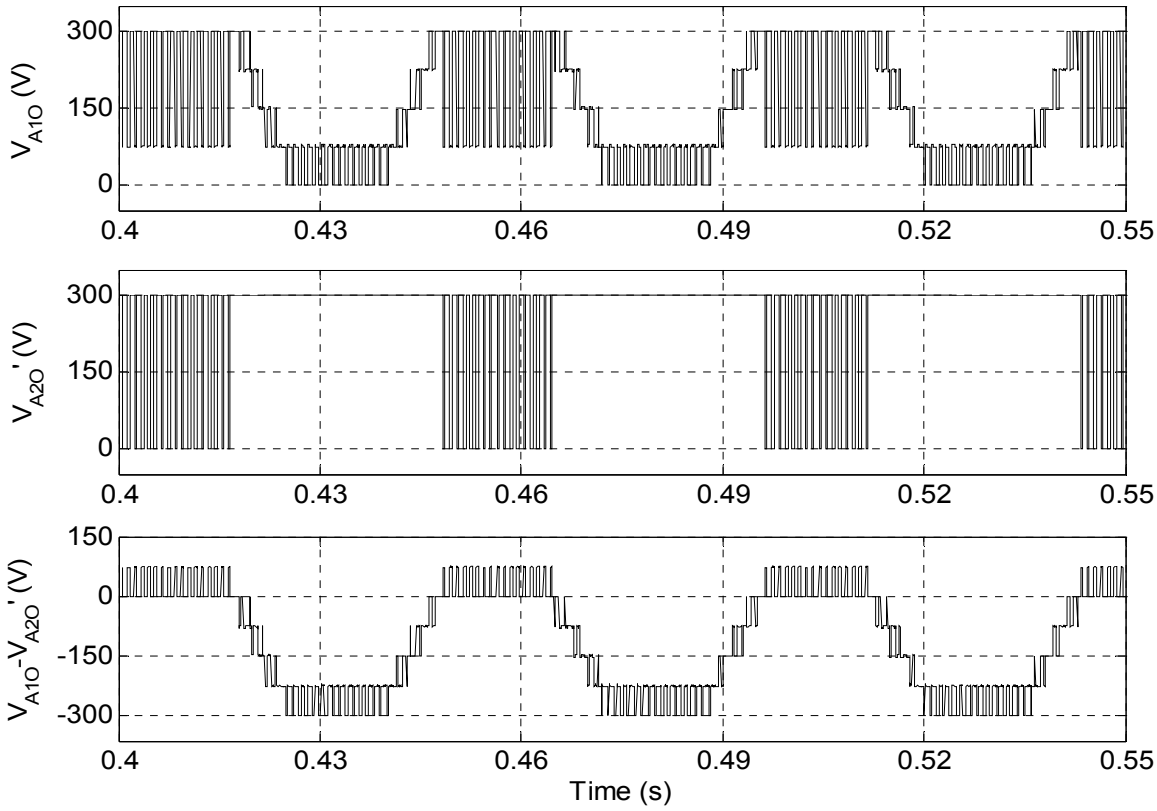



Fig. 5.38 :Top trace; Inverter-A pole voltage ($V_{A1O}$), Middle trace; Inverter-B pole voltage ($V_{A2O'}$), Bottom trace; Difference of Inverter-A and -B pole voltages ($V_{A1O}$ - $V_{A2O'}$) at $m$=0.42; $f^*_m$ =21Hz (6-level mode)

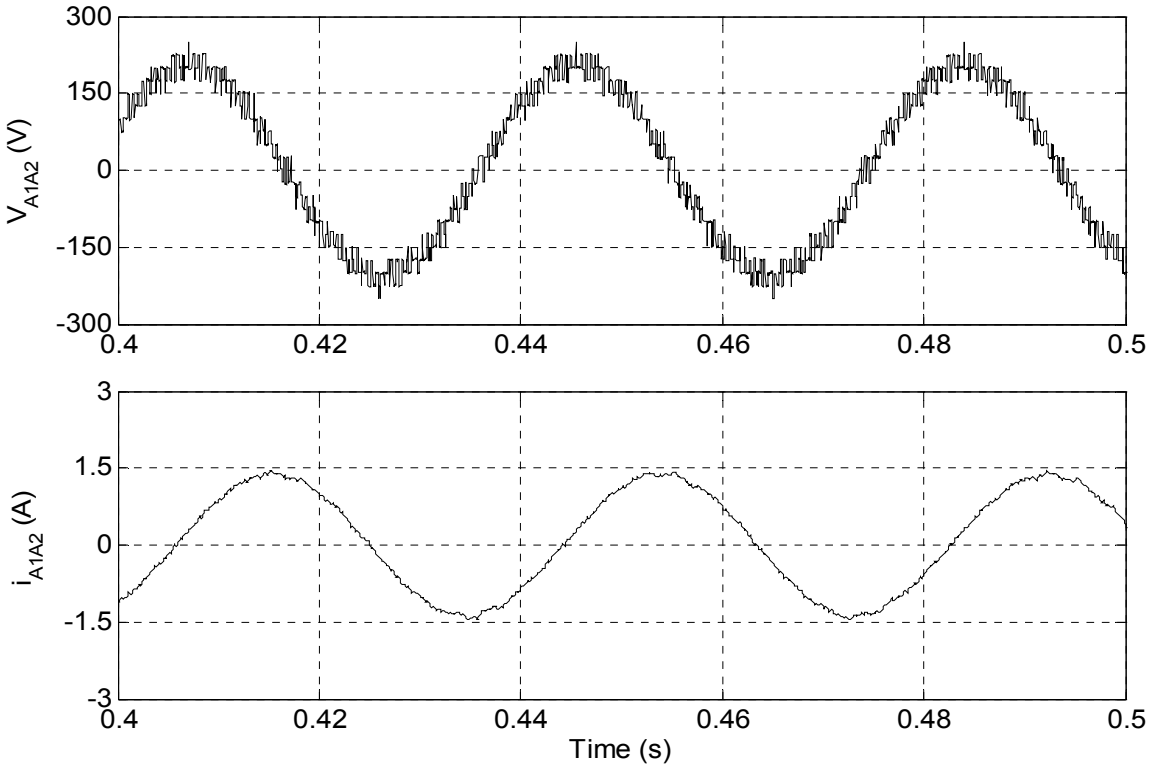



Fig. 5.39: Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A1A2}$ (lower trace) of hybrid 9-level inverter fed open-end IM drive at no load ($m$=0.52; $f^*_m$ =26Hz; 7-level mode)

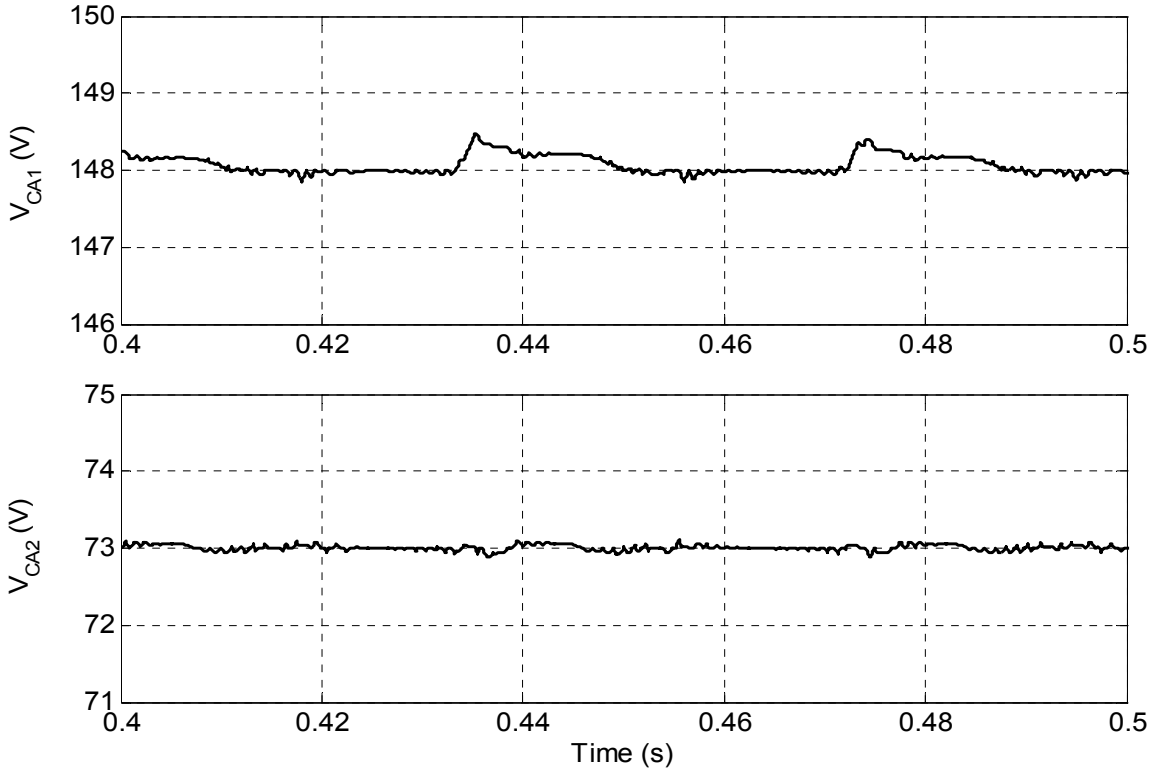



Fig. 5.40: Capacitors voltages $V_{CA1}$ (upper trace) and $V_{CA2}$ (lower trace) in 7-level mode

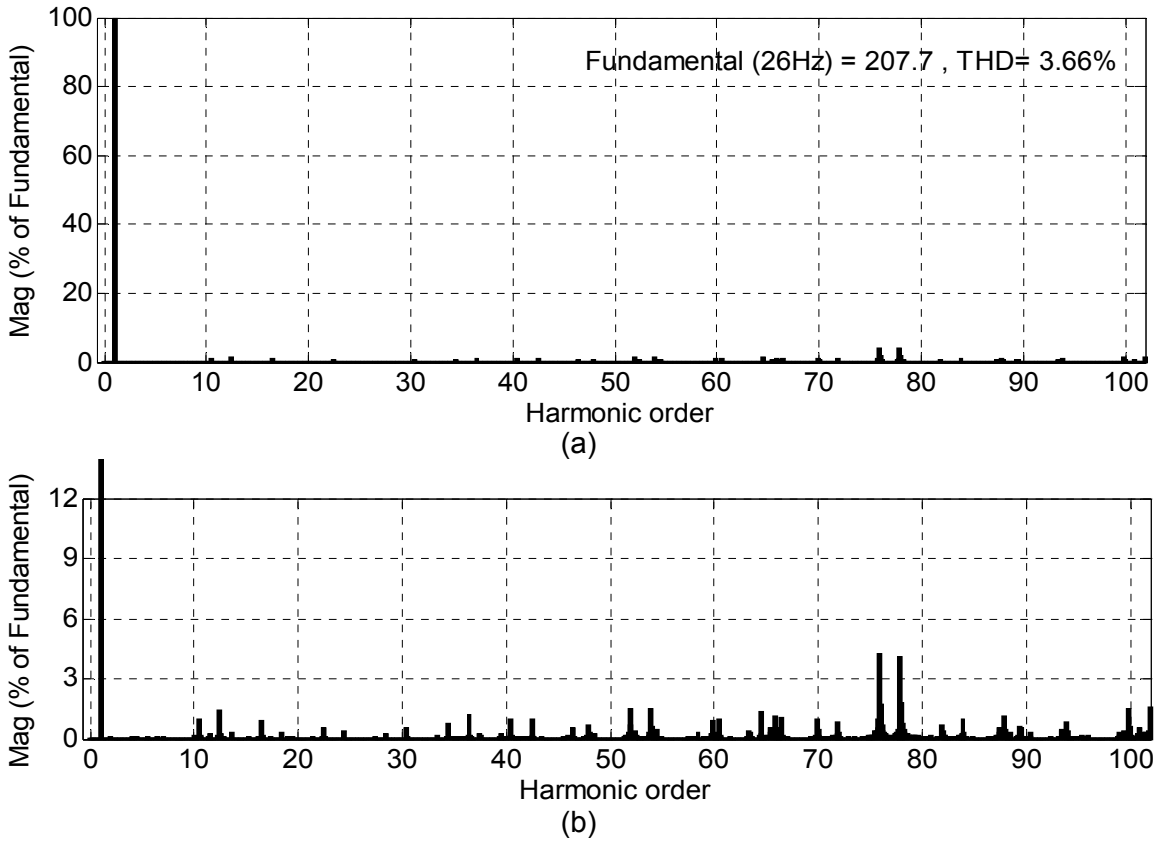



Fig. 5.41: (a) Harmonic spectrum of phase-A voltage ($V_{A1A2}$) at $m$=0.52; $f^*_m$ =26Hz
(b) Zoom view of harmonic spectrum shown in (a)

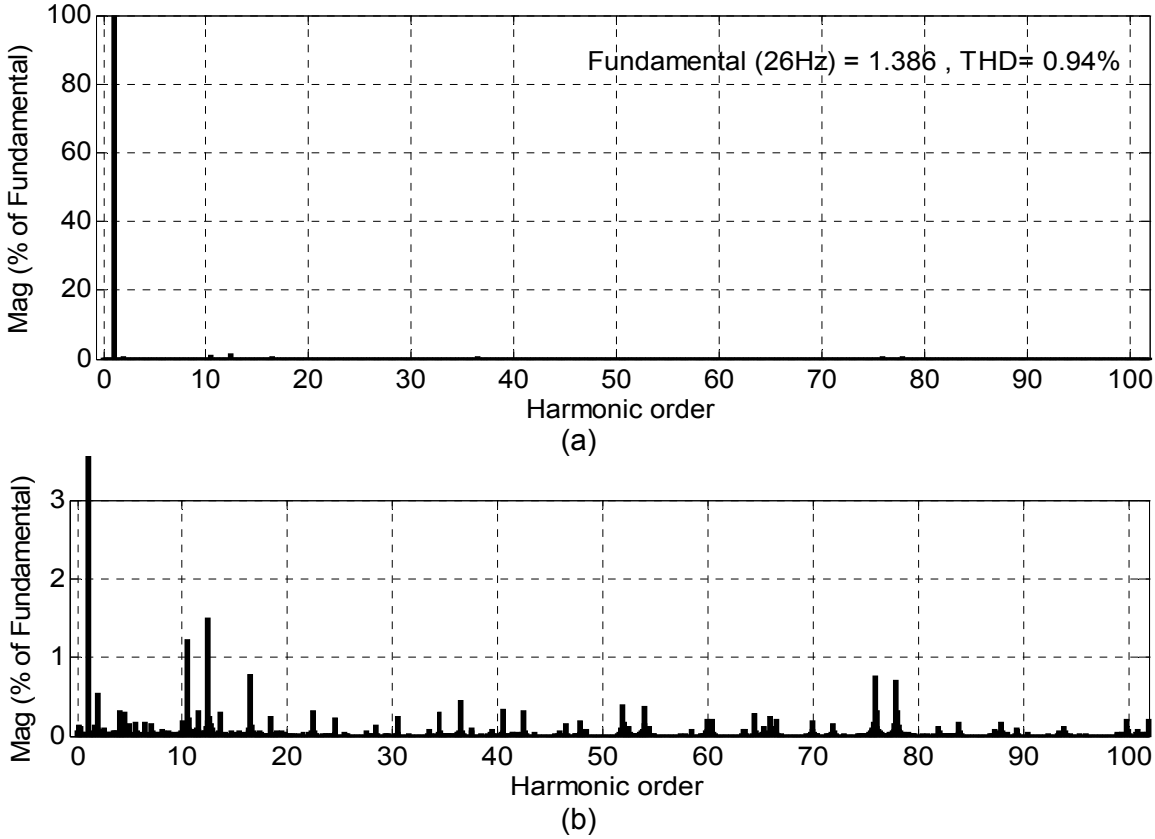



Fig. 5.42: (a) Harmonic spectrum of phase-A current ($i_{A1A2}$) at $m$=0.52; $f^*_m$ =26Hz
(b) Zoom view of harmonic spectrum shown in (a)

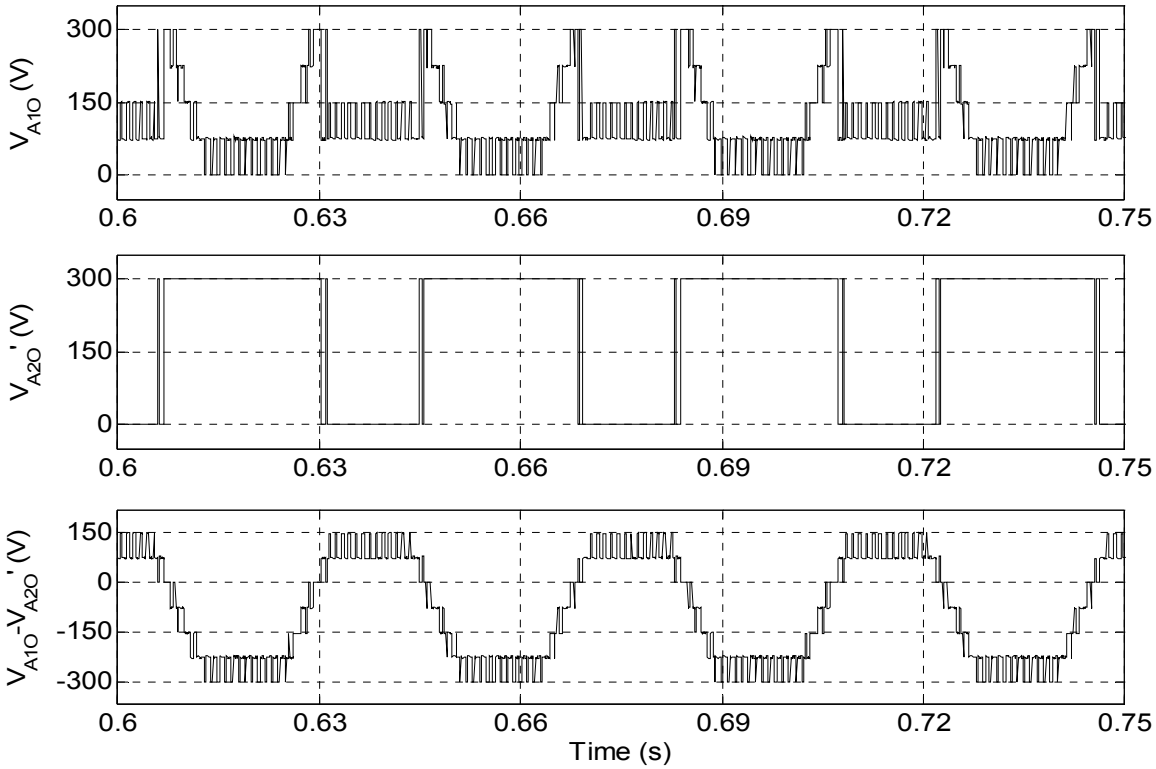



Fig. 5.43 :Top trace; Inverter-A pole voltage ($V_{A1O}$), Middle trace; Inverter-B pole voltage ($V_{A4O'}$), Bottom trace; Difference of Inverter-A and -B pole voltages ($V_{A1O}$ - $V_{A2O'}$) at $m$=0.52; $f^*_m$ =26Hz (7-level mode)

Motor phase-A voltage and current for 8-level mode of operation ($m$=0.64, $f^*_m$=32Hz) are shown in Fig. 5.44. In 8-level mode (Fig. 5.48) one additional level +225 (+3$V_{DC}$/8) is added in the levels obtain in 7-level mode of operation. Similarly in 9-level mode one more level of +300 (+$V_{DC}$/2) as compare to 8-level operation is observed in the pole voltage waveforms shown in Fig. 5.53. The ripple in capacitors voltage ($V_{CA1}$, $V_{CA2}$) is less than 1V in both the mode. The harmonic spectrum of phase voltage in 8-level mode is found little bit distorted and THD is 4.26%. The distortion is due to asymmetric nature of pole voltages of two-level inverter-B. As the switching frequency is only 1kHz so some switching pulses are missed and inverter-B operates in six-step mode which can be observed in inverter-B pole voltage ($V_{A2O'}$) waveform shown in Fig. 5.48. The harmonic spectrum of phase current for 8-level mode of operation is shown in Fig. 5.47. In this case, also the lower order harmonics are increased. It is evident from pole voltages waveforms that in both the mode inverter-B which operates at higher DC link voltage switched very less hence low switching losses occur in inverter-B which increased the overall drive efficiency. The Motor phase-A voltage and current waveforms obtained in 9-level mode of operation are presented in Fig. 5.49 both the waveforms approach towards sinusoidal. The harmonic spectra of phase voltage and current in 9-level mode are shown in Fig. 5.51 and Fig. 5.52 respectively.

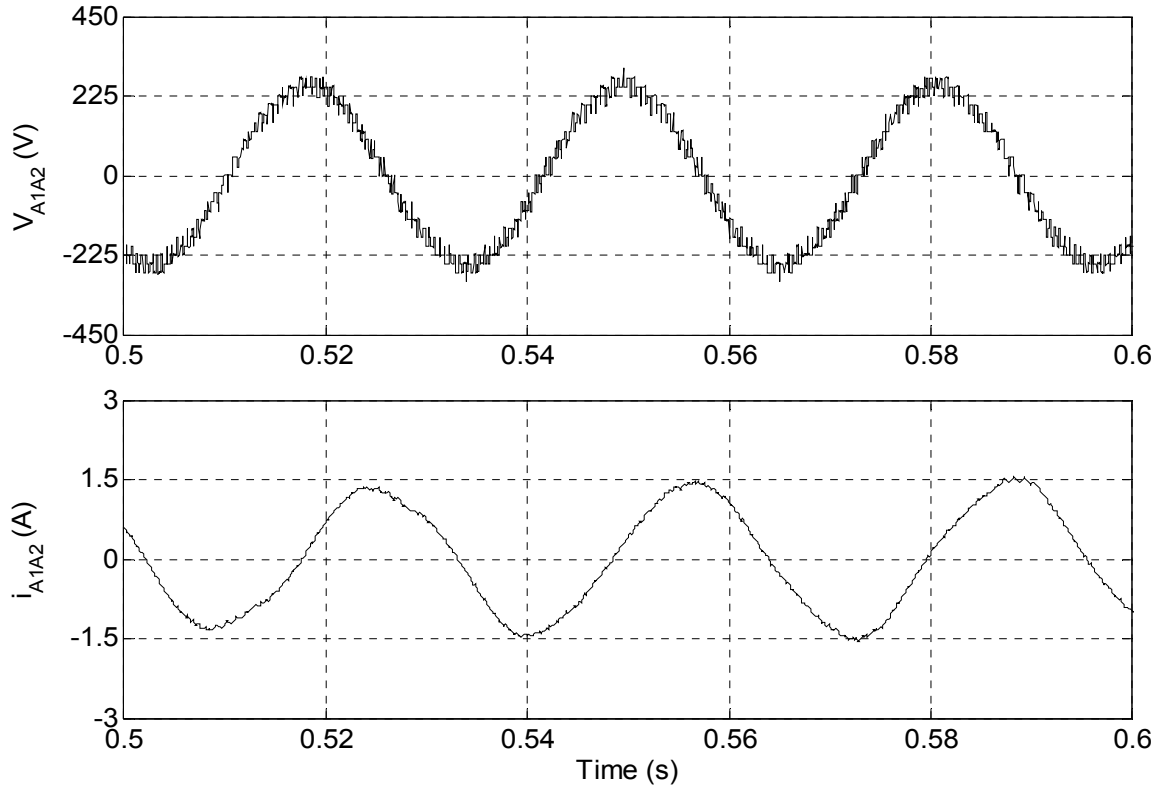



Fig. 5.44: Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A1A2}$ (lower trace) of hybrid 9-level inverter fed open-end IM drive at no load (m=0.64; $f^*_m$ =32Hz; 8-level mode)

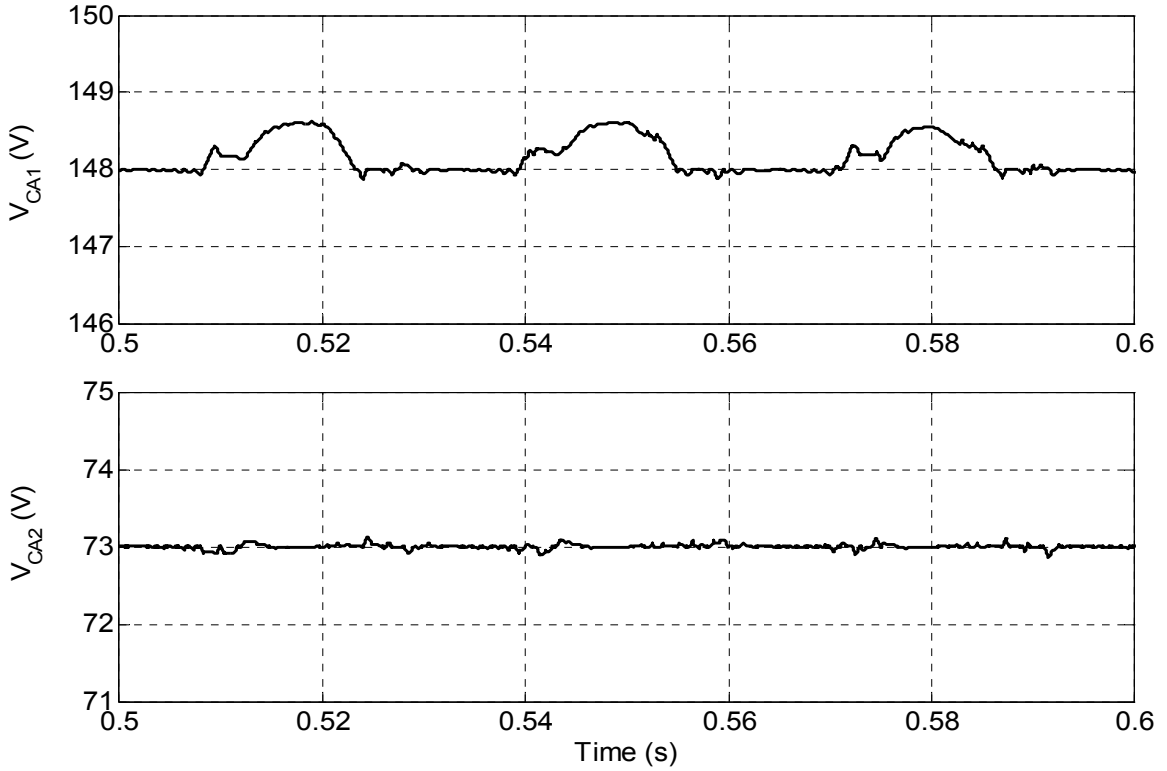



Fig. 5.45: Capacitors voltages $V_{CA1}$ (upper trace) and $V_{CA2}$ (lower trace) in 8-level mode

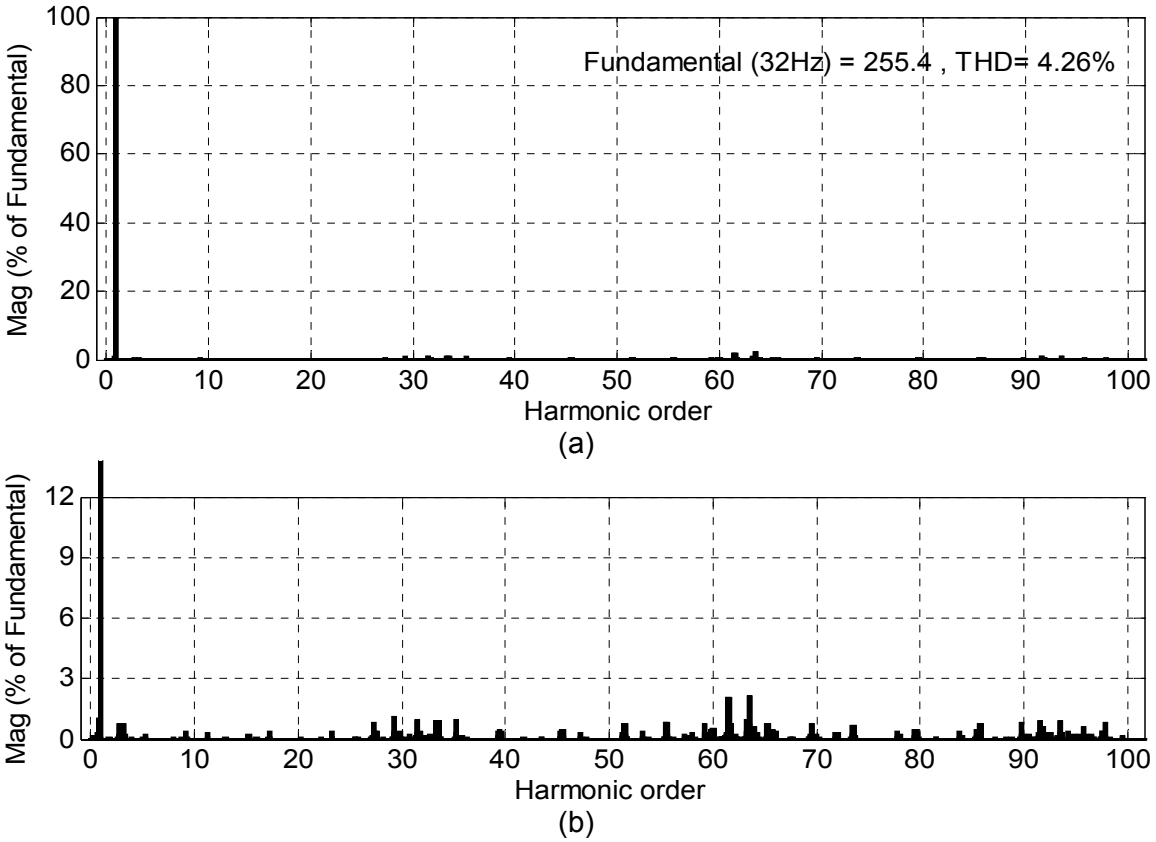



Fig. 5.46: (a) Harmonic spectrum of phase-A voltage ($V_{A1A2}$) at $m$=0.64; $f^*_m$ =32Hz
(b) Zoom view of harmonic spectrum shown in (a)

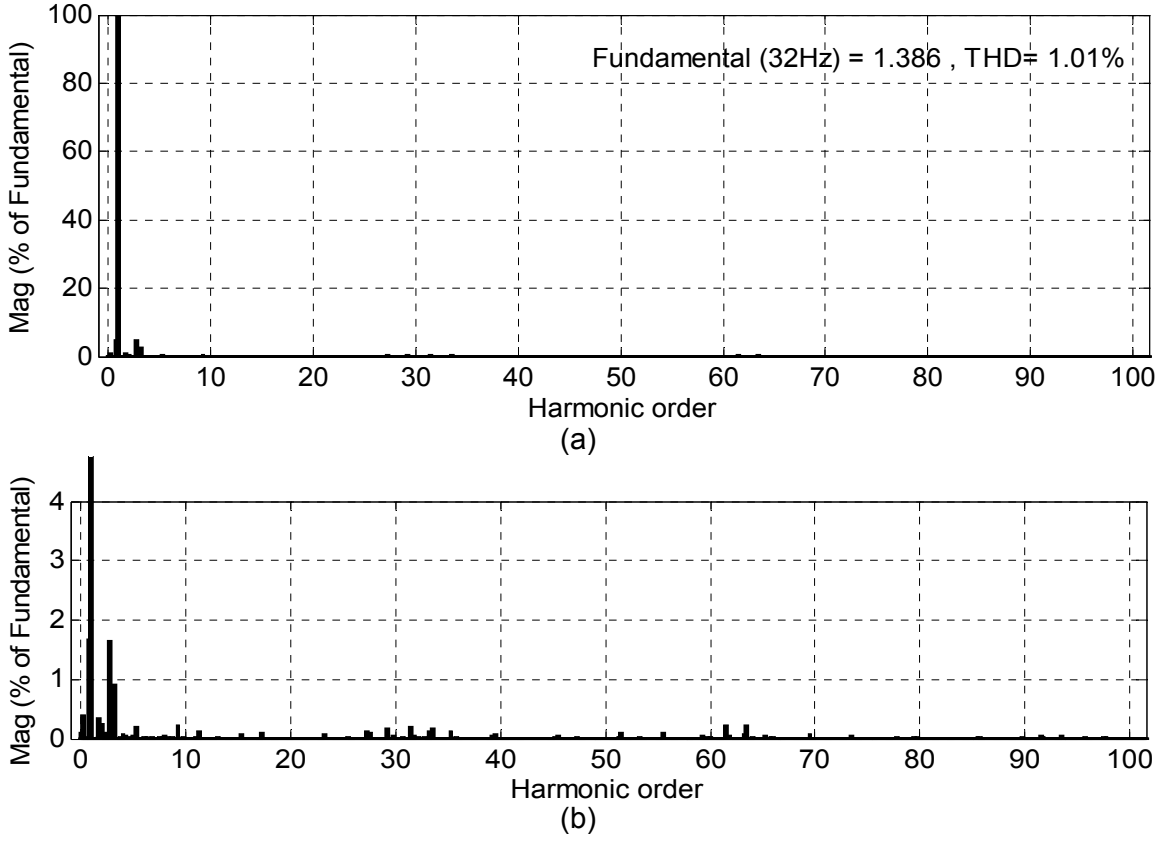



Fig. 5.47: (a) Harmonic spectrum of phase-A current ($i_{A1A2}$) at $m$=0.64; $f^*_m$ =32Hz
(b) Zoom view of harmonic spectrum shown in (a)

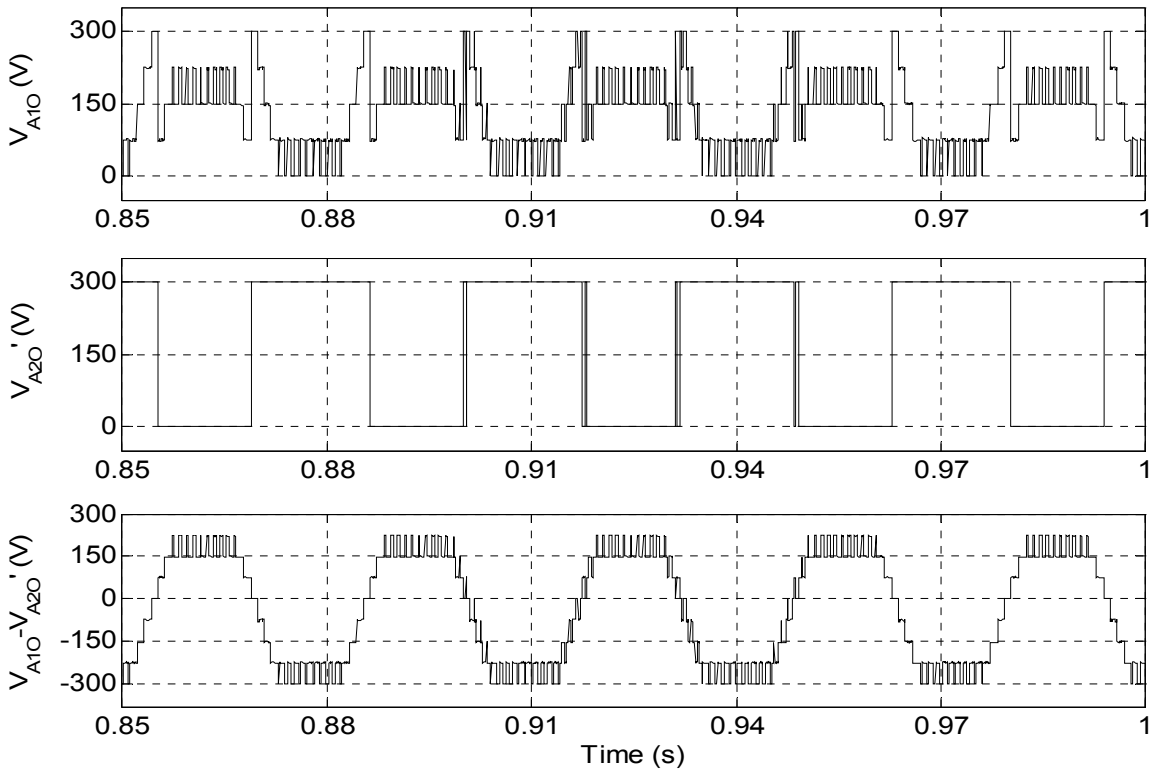



Fig. 5.48 :Top trace; Inverter-A pole voltage ($V_{A1O}$), Middle trace; Inverter-B pole voltage ($V_{A2O'}$), Bottom trace; Difference of Inverter-A and -B pole voltages ($V_{A1O}$ - $V_{A2O'}$) at $m$=0.64; $f^*_m$ =32Hz (8-level mode)

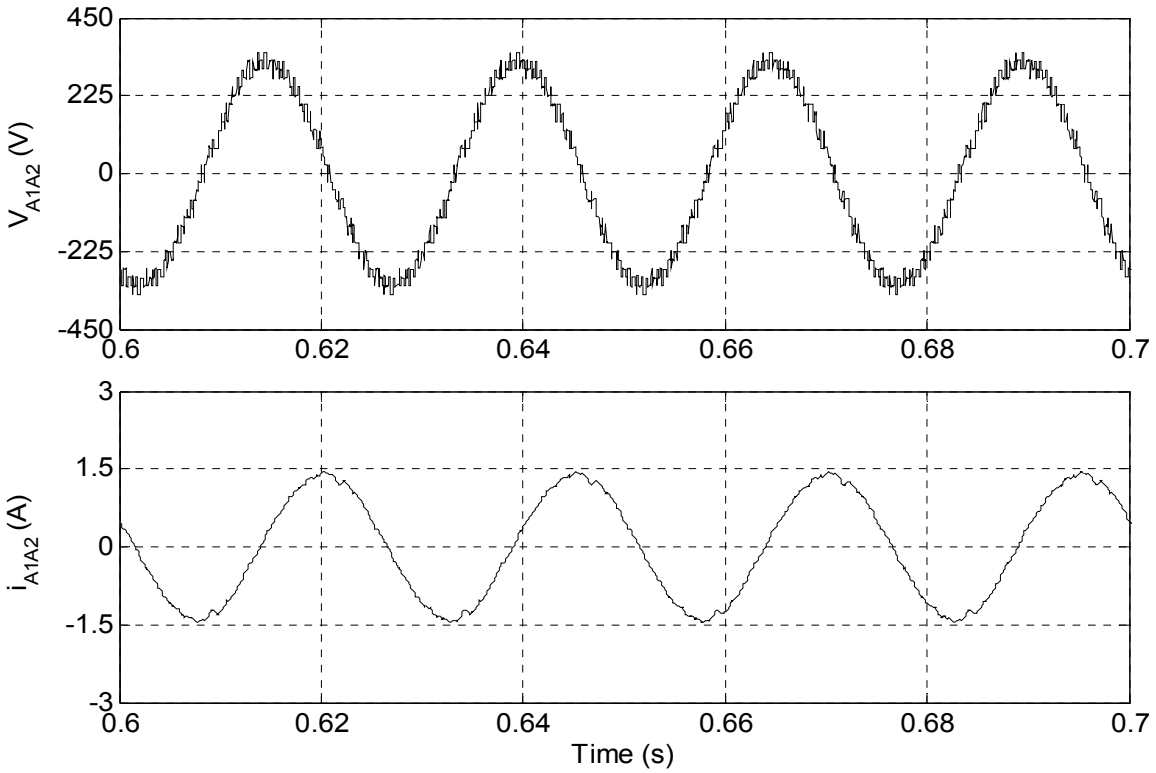



Fig. 5.49: Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A1A2}$ (lower trace) of hybrid 9-level inverter fed open-end IM drive at no load ($m$=0.8; $f^*_m$ =40Hz; 9-level mode )

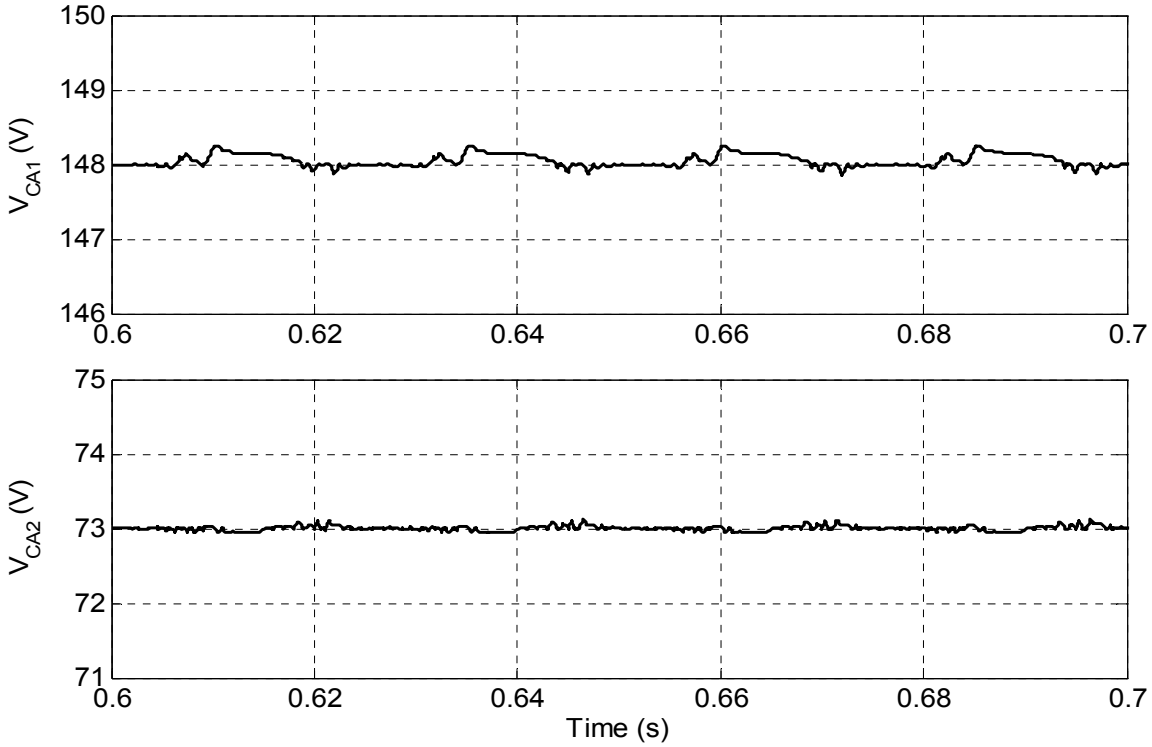



Fig. 5.50: Capacitors voltages $V_{CA1}$ (upper trace) and $V_{CA2}$ (lower trace) in 9-level mode

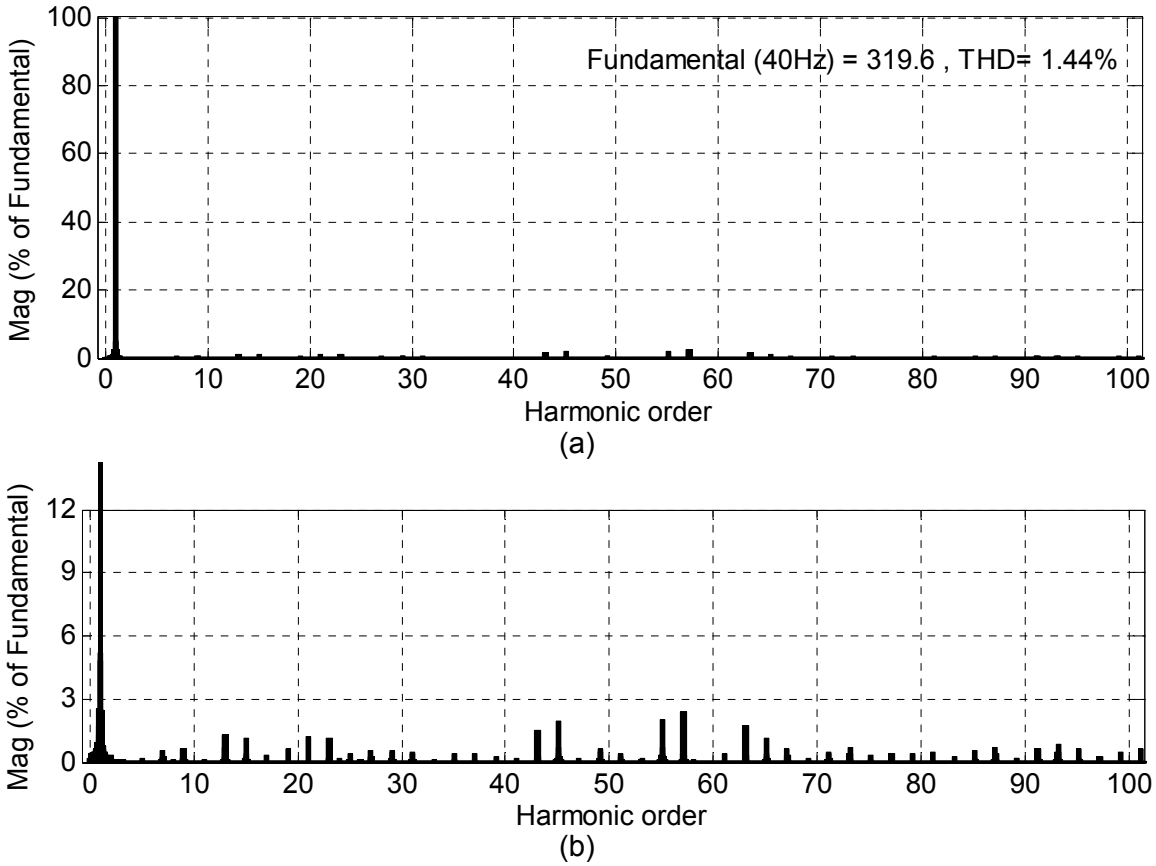



Fig. 5.51: (a) Harmonic spectrum of phase-A voltage ($V_{A1A2}$) at $m$=0.8; $f^*_m$ =40Hz
(b) Zoom view of harmonic spectrum shown in (a)

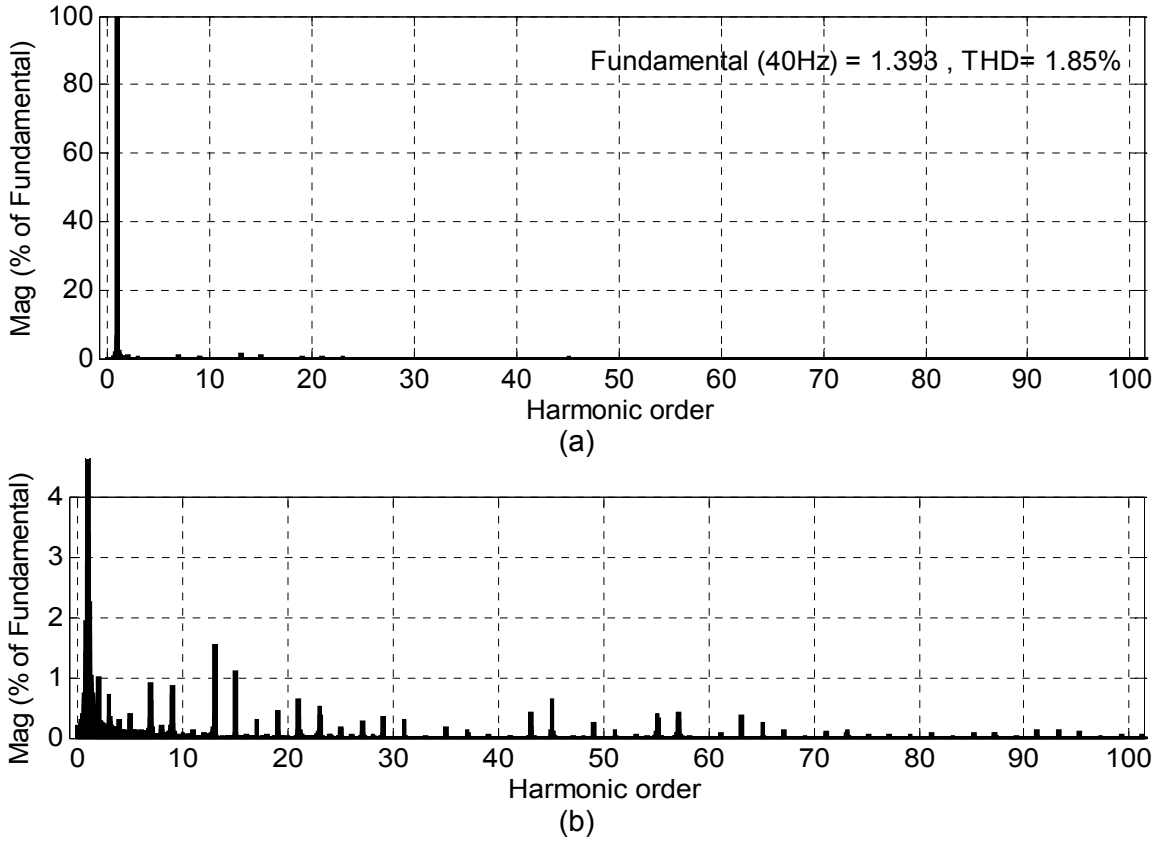



Fig. 5.52: (a) Harmonic spectrum of phase-A current ($i_{A1A2}$) at $m$=0.8; $f^*_m$ =40Hz
(b) Zoom view of harmonic spectrum shown in (a)

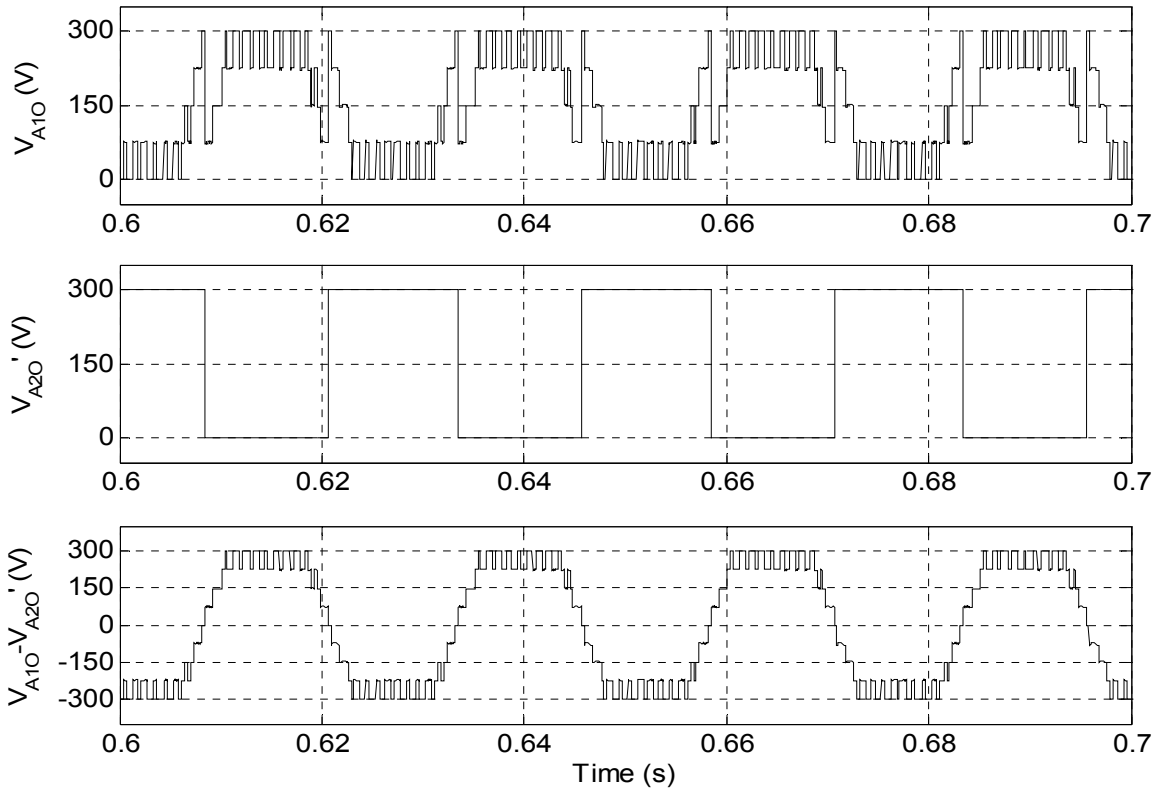



Fig. 5.53 :Top trace; Inverter-A pole voltage ($V_{A1O}$), Middle trace; Inverter-B pole voltage ($V_{A2O'}$), Bottom trace; Difference of Inverter-A and -B pole voltages ($V_{A1O}$ - $V_{A2O'}$) at $m$=0.8; $f^*_m$ =40Hz (9-level mode)

The performance of proposed hybrid 9-level inverter under transient state is investigated by sudden change its operation from two-level to 9-level mode and from 9-level to two-level mode by changing the value of modulation index from 0.08 to 0.8 and vice versa. Fig. 5.54 shows the motor phase-A voltage ($V_{A1A2}$), current ($i_{A1A2}$) and capacitors voltages $V_{CA1}$ and $V_{CA2}$ during sudden change from two-level to 9-level mode of operation. It can be observed from Fig. 5.54 that changeover of inverter operation from two-level to 9-level take place instantaneously and drive attains its steady state in 0.537 second. The capacitors voltages are well balance during acceleration even though the current is high.

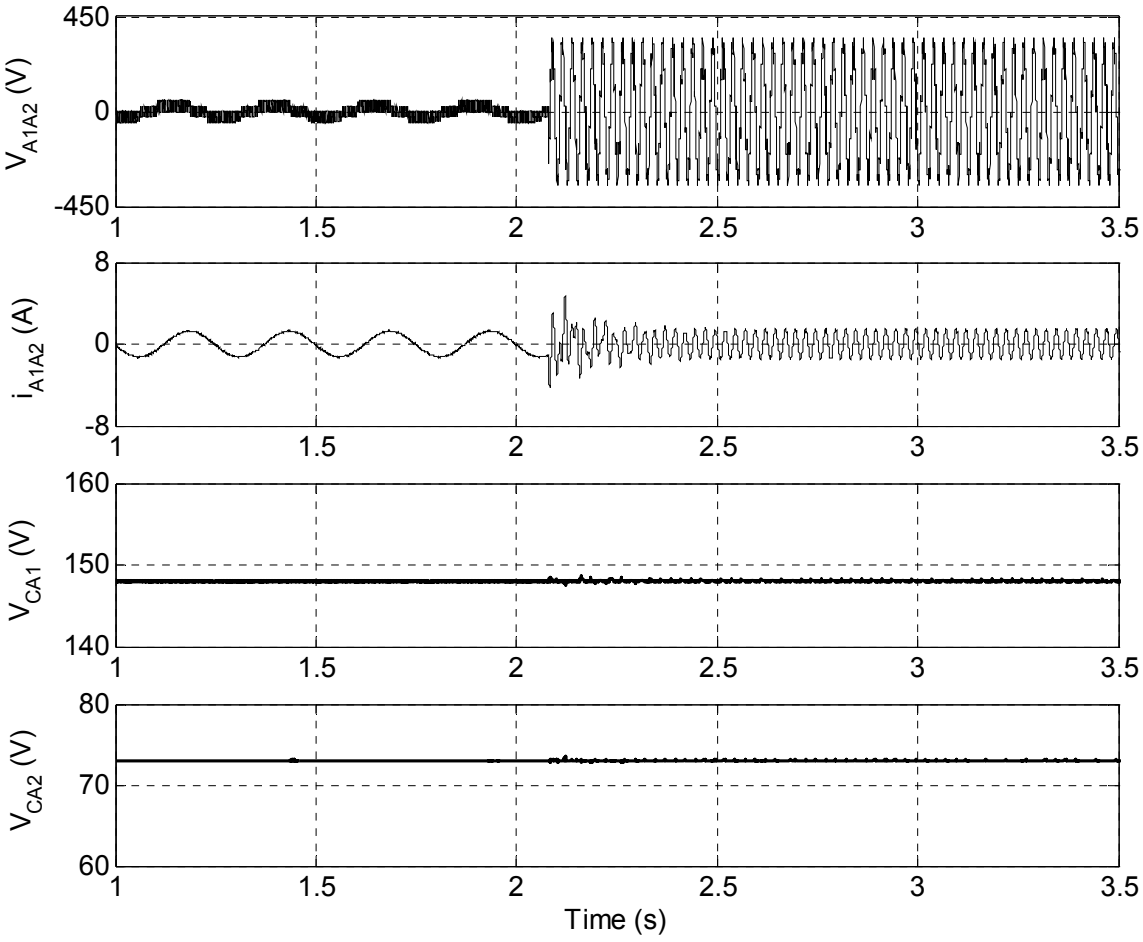



Fig. 5.54: Motor phase-A voltage $V_{A1A2}$, current $i_{A1A2}$, capacitors voltages $V_{CA1}$ and $V_{CA2}$ under sudden change in operation from two-level to 9-level at no-load

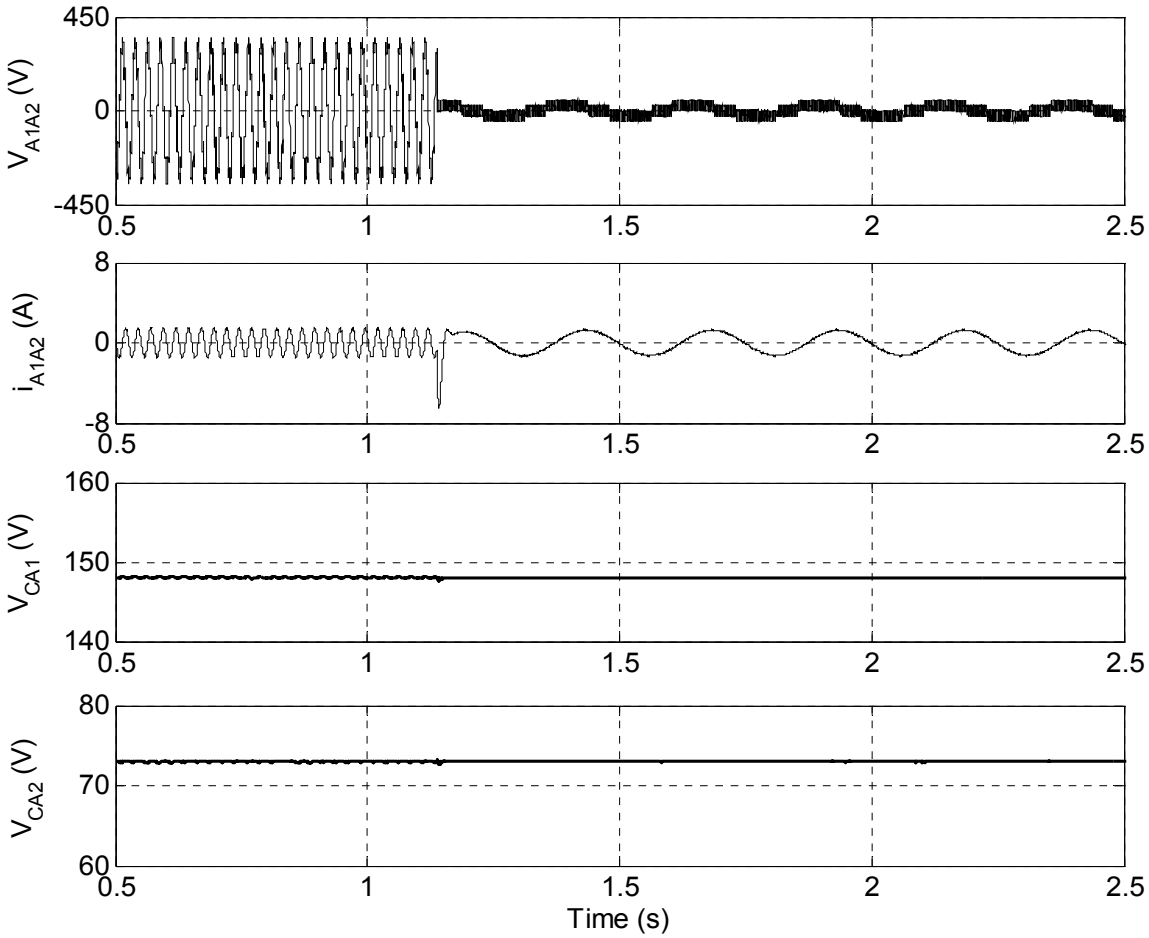



Fig. 5.55: Motor phase-A voltage $V_{A1A2}$, current $i_{A1A2}$, capacitors voltages $V_{CA1}$ and $V_{CA2}$ under sudden change in operation from 9-level to two-level at no-load

Fig. 5.55 shows the simulation results pertaining to changeover from 9-level to two-level operation. In this case also capacitors voltages are well balanced and drive attains its steady state in 0.774 second. It is evident from Fig. 5.54 and Fig. 5.55 that the capacitors voltages remain balanced even during the transient period which confirms the effectiveness of capacitor voltage balancing algorithm.

The effect of disabling the capacitor voltage balancing algorithm is shown in Fig. 5.56. The capacitor balancing logic is disabled at time t=1s for capacitor $C_{A1}$ and enable at t=3s and for $C_{A2}$ it is disabled at t=3s and enable at t=4.5s. It can be seen that the phase voltage, current and capacitors voltages regained their original values very quickly after enabling the capacitor voltage balancing algorithm.

Simulation results shown in Fig. 5.14 - Fig. 5.55 are summarized in Table 5.4. it can be concluded from above discussion that the proposed 9-level inverter start with two-level mode of operation at lower modulation index and as the modulation increases inverter operation is switch towards 3-level, 4-level, 5-level and up to 9-level mode of operation. The capacitors voltages are effectively balanced in all the modes of operation as well as during transient

state using switching state redundancy available in different levels. It is observed capacitors voltages are balanced at lower limit of their respective hysteresis band, it is because the value of no-load current is very low and it is not capable to overcharge the capacitors.

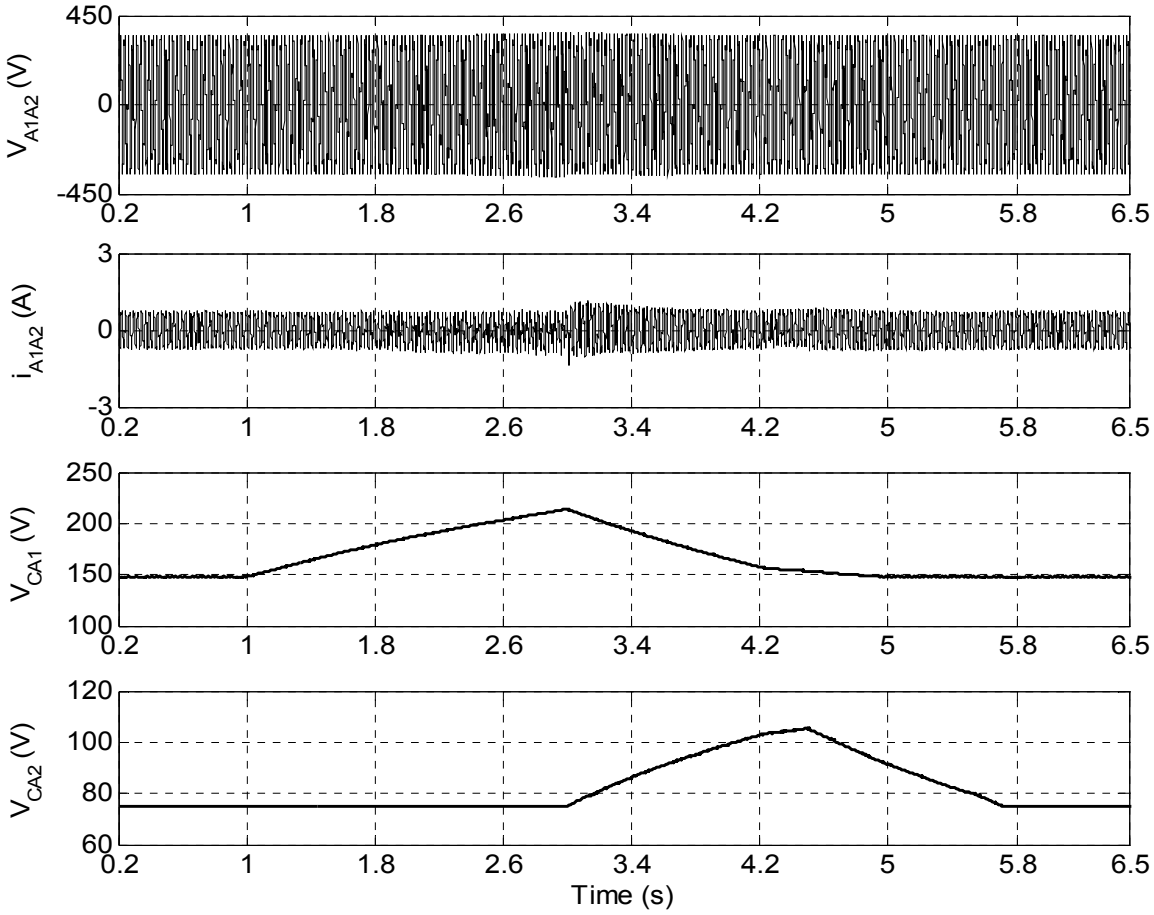



Fig. 5.56: Effect of disabling the capacitor voltage balancing algorithm

Table 5.4: Summary of simulation results of hybrid 9-level inverter obtained at different modulation indices

| Performance parameter | Modulation index($m$) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 0.08 | 0.16 | 0.28 | 0.36 | 0.42 | 0.52 | 0.64 | 0.8 |
| Level of operation | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| RMS of phase-A voltage ($V$) | 29.91 | 48.48 | 81.2 | 103.4 | 120.1 | 148 | 182.9 | 227.4 |
| RMS of phase-A current ($A$) | 0.592 | 0.823 | 0.937 | 0.966 | 0.973 | 0.983 | 0.990 | 0.993 |
| Frequency of phase voltage ($Hz$) | 4 | 8 | 14 | 18 | 21 | 26 | 32 | 40 |
| THD of phase-A voltage in % | 85.83 | 41.18 | 8.52 | 6.86 | 5.01 | 3.66 | 4.26 | 1.44 |
| Order of dominant voltage harmonic (amplitude in %) | 500±1 (38.4) | 250±1 (18.2) | 142±2 (9.2) | 111±2 (3.64) | 95±2 (4.1) | 77±2 (4.2) | 63±2 (1.88) | 57 (2.2) |
| THD of phase-A Current in % | 4.06 | 2.77 | 1.16 | 1.14 | 0.92 | 0.94 | 1.01 | 1.85 |
| Order of dominant current harmonic (amplitude in %) | 500±1 (1.80) | 250±1 (1.20) | 142±2 (0.92) | 39 (0.8) | 27 (1.0) | 13 (1.5) | 3 (1.52) | 13 (1.45) |
| $\Delta V_{CA1}(V)$ | Less than 1(V) | | | | | | | |
| $\Delta V_{CA2}(V)$ | Less than 1(V) | | | | | | | |
| Settling time for changeover from 2-level to 9-level in sec. | 0.537 | | | | | | | |
| Settling time for changeover from 9-level to 2-level in sec. | 0.774 | | | | | | | |
| Sampling time | 10 µSecond | | | | | | | |

## 5.5 Performance Comparison

The performance of proposed hybrid 9-level is compared with 9-level inverter presented in Chapter-4, by operating an open-end winding induction motor under no-load at different modulation indices. The simulated results are tabulated in Table 5.5. It is observed in Table 5.5 that the performance of hybrid 9-level inverter is almost equivalent to the 9-level inverter proposed in Chapter-4 under steady state as well as in transient state.

Table 5.5: Performance comparison of hybrid 9-level inverter with 9-level inverter

| Performance parameter | Type of inverter | Modulation index(*m*) | | | | |
|---|---|---|---|---|---|---|
| | | 0.1 | 0.2 | 0.4 | 0.5 | 0.8 |
| Level of operation | Hybrid 9-level inverter[a] | 3 | 4 | 6 | 7 | 9 |
| | 9-level inverter[b] | 3 | 4 | 6 | 7 | 9 |
| RMS of phase-A voltage (*V*) | Hybrid 9-level inverter[a] | 33.37 | 59.28 | 114.8 | 142.6 | 227.4 |
| | 9-level inverter[b] | 33.23 | 59.41 | 114.7 | 142.8 | 227.3 |
| RMS of phase-A current (*A*) | Hybrid 9-level inverter[a] | 0.675 | 0.881 | 0.972 | 0.981 | 0.993 |
| | 9-level inverter[b] | 0.676 | 0.885 | 0.972 | 0.983 | 0.985 |
| Frequency of phase voltage (*Hz)* | Hybrid 9-level inverter[a] | 5 | 10 | 20 | 25 | 40 |
| | 9-level inverter[b] | 5 | 10 | 20 | 25 | 40 |
| THD of phase-A voltage in % | Hybrid 9-level inverter[a] | 62.74 | 32.45 | 16.33 | 12.98 | 1.44 |
| | 9-level inverter[b] | 61.45 | 32.01 | 16.28 | 13.02 | 2.64 |
| Order of dominant voltage harmonic (amplitude in %) | Hybrid 9-level inverter[a] | 400±1 (16.64) | 200±1 (11.45) | 100±1 (7.14) | 80±1 (5.28) | 57 (2.2) |
| | 9-level inverter[b] | 400±1 (15.81) | 200±1 (11.24) | 100±1 (7.16) | 80±1 (5.29) | 45 (2.1) |
| THD of phase-A current in % | Hybrid 9-level inverter[a] | 4.28 | 2.70 | 2.68 | 3.07 | 1.85 |
| | 9-level inverter[b] | 3.65 | 2.70 | 2.54 | 2.97 | 1.02 |
| Order of dominant current harmonic (amplitude in %) | Hybrid 9-level inverter[a] | 400±1 (0.78) | 200±1 (0.85) | 100±1 (0.99) | 80±1 (0.91) | 13 (1.45) |
| | 9-level inverter[b] | 400±1 (0.78) | 200±1 (0.85) | 100±1 (0.99) | 80±1 (0.91) | 9&13 (1.10) |
| Settling time for changeover from 2-level to 9-level in sec. | Hybrid 9-level inverter[a] | 0.537 | | | | |
| | 9-level inverter[b] | 0.457 | | | | |
| Settling time for changeover from 9-level to 2-level in sec. | Hybrid 9-level inverter[a] | 0.762 | | | | |
| | 9-level inverter[b] | 0.608 | | | | |

Note: [a] Proposed hybrid 9-level inverter
[b] 9-level inverter proposed in Chapter-4

## 5.6 Conclusion

In this chapter a hybrid 9-level inverter topology is proposed for open-end winding induction motor drive. The proposed topology requires only two isolated DC sources of same magnitude as compared to the 9-level inverter topology proposed in Chapter-4 which requires four isolated DC sources. The DC source requirement can be further reduce to one by feeding both sides inverter by a single source of magnitude $V_{DC}/2$, but in that case a proper switching scheme to be adopted to eliminate the common mode (triplen) voltage in the phase winding. The maximum voltage rating of the switching device required in the proposed topology is $V_{DC}/2$ whereas the topology proposed in Chapter-4 requires switching device of voltage rating of $3V_{DC}/4$.

A switching state based mathematical model of hybrid 9-level inverter is developed and the performance of proposed topology is evaluated for entire range of linear modulation by operating a 1.5kW open-end winding induction motor at no-load in MATLAB/Simulink environment. Motor phase voltage, phase current, their harmonic spectrums, balancing of capacitor voltage, inverter pole voltages, difference in inverter pole voltages and sudden change in modulation index are considered as an evaluation criteria for performance evaluation. The effectiveness of capacitors balancing algorithm is tested under steady state as well as transient state conditions and it is found working satisfactory.

The motor phase voltage shows a 2-level or a 3-level or a 4-level waveform in the lowest speed range, a 5-level or a 6-level or a 7-level waveform in the medium speed range, a 8-level or a 9-level waveform in the higher speed range. The motor phase voltage waveform approaches towards sinusoidal as the number of levels in the waveform increases. The harmonic spectrum of motor phase voltage and current are similar to the harmonic spectra which are obtained with 9-level inverter proposed in Chapter-4. In the proposed hybrid 9-level inverter switching devices which operate at higher voltage level switch less as compared to the switching devices which operate at lower voltage level in the entire range of linear modulation, this feature can lead to use of low and switching frequency rating power semiconductor devices hence overall cost is reduced.

To reduce the switching frequency further and increase the number of levels in the output voltage using the same number of switching device an eighteen-level inverter is proposed in next chapter.

# CHAPTER 6: EIGHTEEN-LEVEL INVERTER FOR INDUCTION MOTOR DRIVE

*[An asymmetrical cascade H-bridge based 18-level inverter topology with reduced number of semiconductor switches and switching frequency for open-end induction motor drive is proposed in this chapter. A switching state based mathematical model is also developed for proposed 18-level inverter. Level shifted triangular carrier based space vector pulse width modulation (SVPWM) scheme describe in Chapter-4 is used to generate PWM pulses for the switching devices. To validate the mathematical model and viability of proposed 18-level inverter extensive simulation study is carried out in MATLAB/Simulink environment and simulation results are presented. The performance of proposed 18-level inverter fed open-end induction motor drive is evaluated during steady state and dynamic speed changing conditions at no-load in constant V/f mode.]*

## 6.1 Introduction

The cascade H-bridge [14], [186] and hybrid H-bridge [46], [90] MLI topologies significantly increase the number of levels in the output voltage waveforms for the same number of power electronics devices therefore, these topologies become one of the most attractive approaches. In fact, it become one of the research topics is to increase the level number for the H-bridge multilevel topologies, such that the harmonic contents can be reduced as much as possible, while keeping low switching frequency and switching losses.

A hybrid 9-level inverter topology proposed in chapter-5 for open-end winding induction motor drive uses thirty IGBTs. In this chapter an eighteen-level inversion operation is realized using the same number of IGBTs. The switching frequency is reduced to half as compared to the switching frequency used for hybrid 9-level inverter in Chapter-5. The proposed topology is realized by feeding one end of the open-end winding induction motor by three-phase ACHB 9-level inverter and the other end by conventional three-phase two-level inverter. The three-phase ACHB 9-level inverter [49], consists of two single phase H-bridge cells in each phase with the DC-link voltage ratio of 1:3. The zero sequence currents are completely eliminated in the proposed topology because both sides' inverters are fed by isolated DC supplies. The proposed inverter uses less number of components as compared to conventional MLI topologies. The proposed topology requires seven isolated DC sources out of which six sources are of lower voltage rating; these lower voltage rating isolated sources can be easily implemented using photovoltaic power cells [164], [165]. In the proposed inverter, semiconductor switching devices which operated at higher DC-link voltage switch less hence low switching frequency rating devices can be used. The proposed topology produces a voltage space phasor of maximum amplitude of $V_{DC}$ whereas the maximum DC link voltage used is (9/13)$V_{DC}$, this feature further reduces the size of inverter.

## 6.2 18-Level Inverter Scheme for Induction Motor Drive

### 6.2.1 Power Circuit

A schematic power circuit diagram of proposed 18-level inverter fed open-end IM drive system is shown in Fig. 6.1. One side terminals $A_1$, $B_1$ and $C_1$ of the open-end winding IM are fed by ACHB 9-level inverter-A while the others side terminals $A_2$, $B_2$ and $C_2$ are connected to two-level inverter-B. The three-phase ACHB 9-level inverter is realized by connecting two H-bridges (H-bridge A1 and A2 for phase-A, H-bridge B1 and B2 for phase-B, H-bridge C1 and C2 for phase-C) per phase in cascade. The DC-link voltages of H-bridge X1, H-bridge X2 (X=A, B or C) and two-level inverter-B are kept in ratio of 1:3:9 to achieve 18-level operation. The proposed topology requires thirty switches; and seven isolated DC supplies of magnitude as shown in Fig. 6.1, where $V_{DC}$ is the equivalent DC-link voltage required to operate conventional two-level inverter fed induction motor drive.

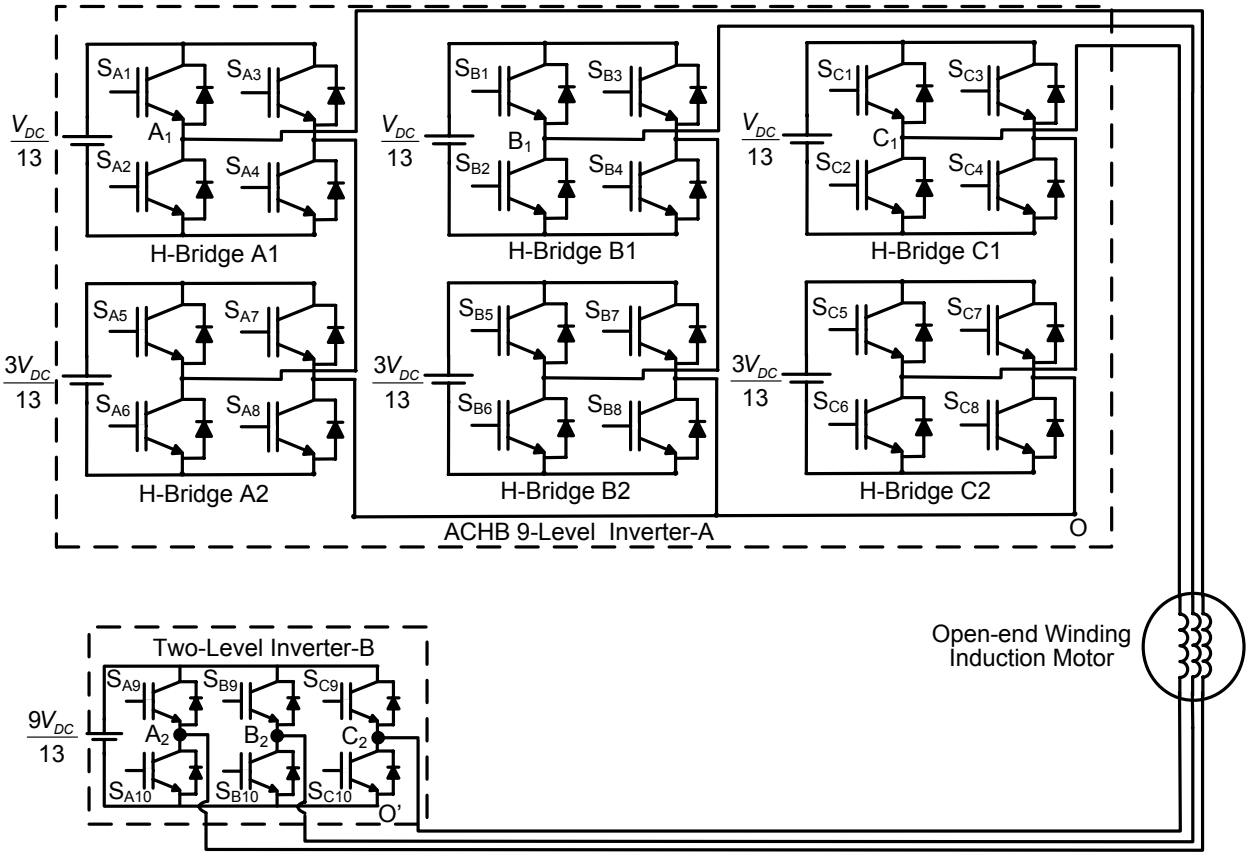



Fig. 6.1: Power circuit of 18-level inverter for induction motor drive

The symbols $V_{A1O}$, $V_{B1O}$ and $V_{C1O}$ denote the pole voltages of ACHB 9-level inverter-A. Similarly, the symbols $V_{A2O'}$, $V_{B2O'}$ and $V_{C2O'}$ denote the pole voltages of two-level inverter-B with respect to its own reference point O'. Any pole voltage $V_{A1O}$, $V_{B1O}$ or $V_{C1O}$ of inverter-A can have nine-different voltage levels viz. -(4/13)$V_{DC}$, -(3/13)$V_{DC}$, -(2/13)$V_{DC}$, -(1/13)$V_{DC}$, 0, +(1/13)$V_{DC}$, +(2/13)$V_{DC}$, +(3/13)$V_{DC}$ and +(4/13)$V_{DC}$ independently. For example, pole voltage $V_{A1O}$ becomes -(4/13)$V_{DC}$ if switches $S_{A2}$, $S_{A3}$, $S_{A6}$ and $S_{A7}$ are 'ON', or becomes -(3/13)$V_{DC}$ if

switches $S_{A1}$, $S_{A3}$, $S_{A6}$ and $S_{A7}$ are turned 'ON'. Similarly two-level inverter pole voltages $V_{A2O'}$, $V_{B2O'}$ and $V_{C2O'}$ can have voltage levels of 0 and +(9/13)$V_{DC}$. The combined effect of these two inverters on the motor phase winding is generation of eighteen distinct levels as: -$V_{DC}$, -(12/13)$V_{DC}$, -(11/13)$V_{DC}$, -(10/13)$V_{DC}$, -(9/13)$V_{DC}$, -(8/13)$V_{DC}$, -(7/13)$V_{DC}$, -(6/13)$V_{DC}$, -(5/13)$V_{DC}$, -(4/13)$V_{DC}$, -(3/13)$V_{DC}$, -(2/13)$V_{DC}$, -(1/13)$V_{DC}$, 0, +(1/13)$V_{DC}$, +(2/13)$V_{DC}$, +(3/13)$V_{DC}$ and +(4/13)$V_{DC}$.

Different voltage levels and corresponding switching states to generate eighteen-levels across the phase-A winding is shown in Table 6.1. Similar logic can also be developed for phase-B and C by simply replacing the switch '$S_{AX}$ ' by '$S_{BX}$ ' and '$S_{CX}$ ' (where $X$ =1 to 10) respectively. The switches of same legs operate in complementary fashion to avoid the short- circuit of DC-link.

Table 6.1: Switching states to realized eighteen–levels in phase-A

| Level of operation | Pole voltage $V_{A1O}$ | Pole voltage $V_{A2O'}$ | Motor phase-A voltage level ($V_{A1O}$ -$V_{A2O'}$) | Switching State[a] | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $S_{A1}$ | $S_{A2}$ | $S_{A3}$ | $S_{A4}$ | $S_{A5}$ | $S_{A6}$ | $S_{A7}$ | $S_{A8}$ | $S_{A9}$ | $S_{A10}$ |
| $L_1$ | -(4/13)$V_{DC}$ | +(9/13)$V_{DC}$ | -$V_{DC}$ | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| $L_2$ | -(3/13)$V_{DC}$ | +(9/13)$V_{DC}$ | -(12/13)$V_{DC}$ | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| $L_3$ | -(2/13)$V_{DC}$ | +(9/13)$V_{DC}$ | -(11/13)$V_{DC}$ | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| $L_4$ | -(1/13)$V_{DC}$ | +(9/13)$V_{DC}$ | -(10/13)$V_{DC}$ | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| $L_5$ | 0 | +(9/13)$V_{DC}$ | -(9/13)$V_{DC}$ | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| $L_6$ | +(1/13)$V_{DC}$ | +(9/13)$V_{DC}$ | -(8/13)$V_{DC}$ | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| $L_7$ | +(2/13)$V_{DC}$ | +(9/13)$V_{DC}$ | -(7/13)$V_{DC}$ | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| $L_8$ | +(3/13)$V_{DC}$ | +(9/13)$V_{DC}$ | -(6/13)$V_{DC}$ | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| $L_9$ | +(4/13)$V_{DC}$ | +(9/13)$V_{DC}$ | -(5/13)$V_{DC}$ | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| $L_{10}$ | -(4/13)$V_{DC}$ | 0 | -(4/13)$V_{DC}$ | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| $L_{11}$ | -(3/13)$V_{DC}$ | 0 | -(3/13)$V_{DC}$ | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| $L_{12}$ | -(2/13)$V_{DC}$ | 0 | -(2/13)$V_{DC}$ | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| $L_{13}$ | -(1/13)$V_{DC}$ | 0 | -(1/13)$V_{DC}$ | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| $L_{14}$ | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| $L_{15}$ | +(1/13)$V_{DC}$ | 0 | +(1/13)$V_{DC}$ | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| $L_{16}$ | +(2/13)$V_{DC}$ | 0 | +(2/13)$V_{DC}$ | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| $L_{17}$ | +(3/13)$V_{DC}$ | 0 | +(3/13)$V_{DC}$ | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| $L_{18}$ | +(4/13)$V_{DC}$ | 0 | +(4/13)$V_{DC}$ | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |

[a] Switching state '1' denotes switch is 'ON' and '0' denotes switch is 'OFF'

### 6.2.2 Salient Features of Proposed Inverter Topology

The proposed 18-level inverter uses same number of switches as that of require by hybrid 9-level inverter presented in Chapter-5. As the number of levels is quite high so the inverter can be operated at lower switching frequency, results the lower switching losses and improve overall efficiency. The 18-level NPC and FC use 102 IGBTs of voltage rating $V_{DC}/17$; and CHB uses 108 IGBTs of voltage rating $V_{DC}/18$ whereas the proposed inverter uses only thirty number of IGBTs out of which six are of voltage rating $9V_{DC}/13$, twelve are of voltage rating $3V_{DC}/13$ and remaining twelve IGBTs of voltage rating $V_{DC}/13$, where $V_{DC}$ is the equivalent DC-link voltage required to operate conventional two-level inverter fed induction motor drive. As the cost and complexity of control circuit increases with the increase in number of switches therefore proposed inverter offers low cost solution. The proposed topology does not require any balancing capacitor whereas 18-level NPC and FC required 17 and 408 capacitors respectively. The 18-level NPC requires 816 clamping diode this requirement is completely eliminated in the proposed topology. Asymmetrical cascade H-bridge (ACHB) 18-level inverter topology [49] requires nine isolated DC sources out of which three are of voltage rating $9V_{DC}/13$, three are of voltage rating $3V_{DC}/13$ and remaining three of voltage rating $V_{DC}/13$, whereas the proposed topology needs seven isolated DC sources out of which three are of voltage rating $3V_{DC}/13$, three are of voltage rating $V_{DC}/13$ and one DC source of voltage rating $9V_{DC}/13$. Although, ACHB with nine DC sources and 36 switches can generate 27-levels, but the requirement of three number of higher rating isolated DC sources of $9V_{DC}/13$ makes the system bulky and costly hence the proposed 18-level inverter could be a better compromise between cost and quality. An interesting feature of the proposed inverter is its ability to operate in two-level mode at reduced power level in case failure of any H-bridge of ACHB inverter. It can be done by disconnecting the motor terminals ($A_1$,$B_1$,$C_1$) from faulty ACHB inverter and connect them in star. Similarly the proposed inverter can operate in nine-level mode by disconnecting the motor terminals ($A_2$,$B_2$,$C_2$) from two-level inverter and connect them in star in case of fault in two-level inverter. This feature increases the reliability of the overall system. An important point can be observed from Table 6.1 that for the first nine levels ($L_1$-$L_9$) two-level inverter is clamped at $9V_{DC}/13$ and for remaining nine levels ($L_{10}$ - $L_{18}$) it is clamped at zero. Therefore, switching losses are reduced because two-level inverter which operates at higher DC link voltage switch less as compared to the inverter which operates at lower DC link voltage. The flow of triplen harmonic current through motor winding is inherently prevented in the proposed 18-level inverter as the both side terminals are fed by isolated DC supplies.

The comparison of proposed topology with other topologies in terms of number of components used is given in Table 6.2.

Table 6.2: Comparison of 18-level inverter topologies

| Component | NPC | FC | CHB | ACHB[a] | Proposed Inverter |
|---|---|---|---|---|---|
| DC source ($V_{DC}$) | 1 | 1 | 0 | 0 | 0 |
| DC source ($V_{DC}$/18) | 0 | 0 | 27 | 0 | 0 |
| DC source ($V_{DC}$/13) | 0 | 0 | 0 | 3 | 3 |
| DC source ($3V_{DC}$/13) | 0 | 0 | 12 | 3 | 3 |
| DC source ($9V_{DC}$/13) | 0 | 0 | 12 | 3 | 1 |
| IGBT ($V_{DC}$/18) | 0 | 0 | 108 | 0 | 0 |
| IGBT ($V_{DC}$/17) | 102 | 102 | 0 | 0 | 0 |
| IGBT ($V_{DC}$/13) | 0 | 0 | 0 | 12 | 12 |
| IGBT ($3V_{DC}$/13) | 0 | 0 | 0 | 12 | 12 |
| IGBT ($9V_{DC}$/13) | 0 | 0 | 0 | 12 | 6 |
| Clamping diode ($V_{DC}$/17) | 816 | 0 | 0 | 0 | 0 |
| Capacitor[b] ($V_{DC}$/17) | 17 | 408 | 0 | 0 | 0 |

Note: [a] ACHB is the asymmetrical cascade H-bridge with voltage source scaled in power of 3 [49]
[b] Excluding rectifier capacitors

### 6.3 Control Strategy and PWM Generation

The level shifted pulse width modulation (LSPWM) scheme presented in section 4.3 of Chapter-4 for 9-level inverter is extended to generate PWM pulses for proposed 18-level inverter. The schematic block diagram of *V/f* control scheme is shown in Fig. 6.2. The switching frequency is kept constant during the entire range of operation and it is selected as 500Hz. The required reference phasor $V_r^*$ is calculated from the motor speed requirement by using constant *V/f* control. The three reference phase voltages ($V_{A1A2}^*, V_{B1B2}^*, V_{C1C2}^*$) are generated by transferring the orthogonal components of reference voltage phasor $V_r^*$ into the three phase quantity and given by

$$\left.\begin{aligned} V_{A1A2}^* &= V_m^* Sin\omega t \\ V_{B1B2}^* &= V_m^* Sin(\omega t - 2\pi/3) \\ V_{C1C2}^* &= V_m^* Sin(\omega t + 2\pi/3) \end{aligned}\right\} \quad (6.1)$$

These reference waves are fed to SVPWM generation block which add a DC bias of magnitude $\frac{nV_c}{2}$ and an offset ($V_{offset}$) signal as discussed in section 4.3 of Chapter-4.

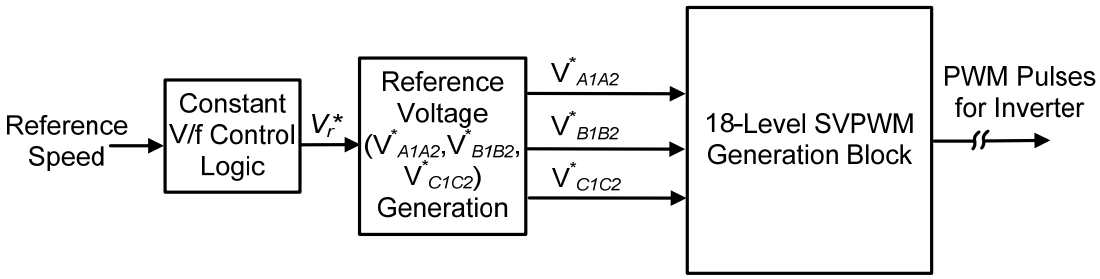



Fig. 6.2: Schematic block diagram of V/f control scheme

The three modulating signals correspond to phase-A, B and C, generated by SVPWM block are given by equation

$$\left.\begin{aligned} V_a^* &= V_m^* Sin\omega t + V_{offset} + nV_c/2 \\ V_b^* &= V_m^* Sin(\omega t - 2\pi/3) + V_{offset} + nV_c/2 \\ V_c^* &= V_m^* Sin(\omega t + 2\pi/3) + V_{offset} + nV_c/2 \end{aligned}\right\} \quad (6.2)$$

Where, $V_{offset} = -[\max(V^*_{A1A2}, V^*_{B1B2}, V^*_{C1C2}) + \min(V^*_{A1A2}, V^*_{B1B2}, V^*_{C1C2})]/2$ and $V_c$ is the amplitude of triangular carrier. The value of '*n*' changes from 1 to 17 for two-level to eighteen-level operation.

The adopted LSPWM scheme uses seventeen level shifted triangular carriers (C1-C17). These seventeen triangular carriers divide the entire range of modulation into eighteen different regions $R_1$-$R_{18}$ as shown in Fig. 6.3. The region below the first triangular carrier C1 is define as $R_1$, region between C1 and C2 is $R_2$ similarly region between C2 and C3 is called $R_3$, in the same way $R_4$-$R_{17}$ are defined and finally $R_{18}$ is the region above last triangular carrier C17. These eighteen regions $R_1$-$R_{18}$ correspond to eighteen levels $L_1$-$L_{18}$ as shown in Table 6.3. The 18-level SVPWM generation block simultaneously compared the three modulating signals ($V_a^*, V_b^*, V_c^*$) with seventeen triangular carrier (C1-C17) and identify the level of operation according to Table 6.3. Once the level of operation is found required voltage level is applied across the phase by turning 'ON' the switches correspond to that level using Table 6.1. One important point can be noticed here that in the adopted PWM scheme switching losses are less as compared to conventional LSPWM scheme because for lower modulation indices, switching occur only in ACHB inverter which operates at lower DC link voltage and two-level inverter is clamped at $+9V_{DC}/13$, whereas in case of conventional LSPWM two-level inverter is also operated in PWM mode hence more switching losses.

The proposed inverter starts to operate in two-level mode for lower speed range and as the speed increases operation is shifted from two-level to 18-level mode including even number of levels.

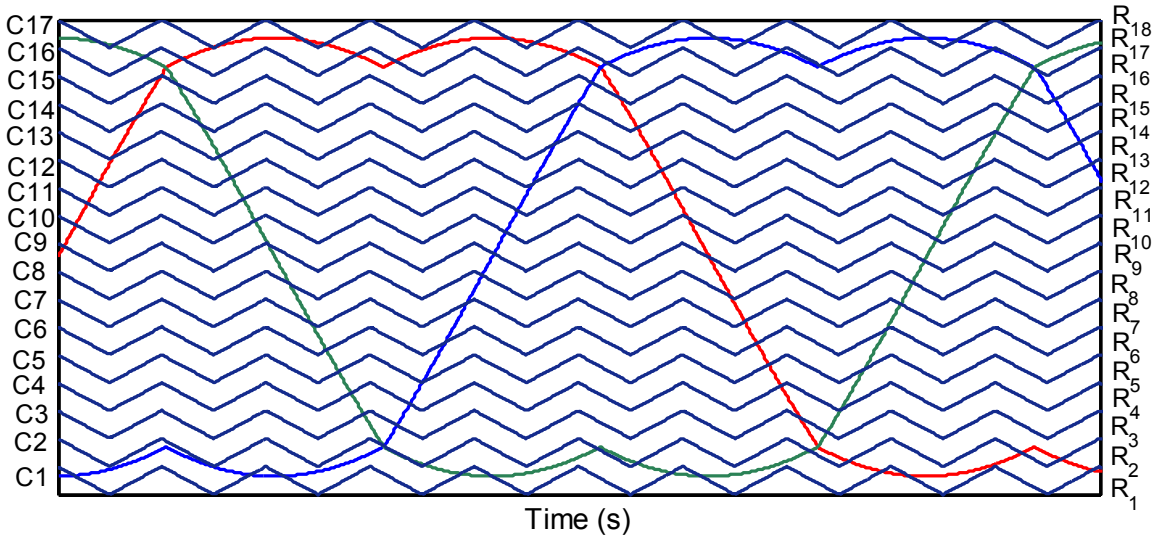



Fig. 6.3: Modulating signals with eight level shifted triangular carriers

Table 6.3: Determination of region and phase voltage level from modulating signal

| Level | Modulating signal amplitude | Region | Phase voltage level |
|---|---|---|---|
| $L_1$ | <C1 | $R_1$ | $-V_{DC}$ |
| $L_2$ | >C1 and <C2 | $R_2$ | $-12V_{DC}/13$ |
| $L_3$ | >C2 and <C3 | $R_3$ | $-11V_{DC}/13$ |
| $L_4$ | >C3 and <C4 | $R_4$ | $-10V_{DC}/13$ |
| $L_5$ | >C4 and <C5 | $R_5$ | $-9V_{DC}/13$ |
| $L_6$ | >C5 and <C6 | $R_6$ | $-8V_{DC}/13$ |
| $L_7$ | >C6 and <C7 | $R_7$ | $-7\ V_{DC}/13$ |
| $L_8$ | >C7 and <C8 | $R_8$ | $-6\ V_{DC}/13$ |
| $L_9$ | >C8 and <C9 | $R_9$ | $-5V_{DC}/13$ |
| $L_{10}$ | >C9 and <C10 | $R_{10}$ | $-4V_{DC}/13$ |
| $L_{11}$ | >C10 and <C11 | $R_{11}$ | $-3V_{DC}/13$ |
| $L_{12}$ | >C11 and <C12 | $R_{12}$ | $-2V_{DC}/13$ |
| $L_{13}$ | >C12 and <C13 | $R_{13}$ | $-V_{DC}/13$ |
| $L_{14}$ | >C13 and <C14 | $R_{14}$ | 0 |
| $L_{15}$ | >C14 and <C15 | $R_{15}$ | $+V_{DC}/13$ |
| $L_{16}$ | >C15 and <C16 | $R_{16}$ | $+2V_{DC}/13$ |
| $L_{17}$ | >C16 and <C17 | $R_{17}$ | $+3V_{DC}/13$ |
| $L_{18}$ | >C17 | $R_{18}$ | $+4V_{DC}/13$ |

## 6.4 Mathematical Modelling of Proposed 18-Level Inverter

A mathematical model of the proposed 18-level inverter is developed based on switching states. The pole voltage $V_{A1O}$ of 9-level 'Inverter-A' in terms of switching states and DC link voltage is given by:

$$\begin{aligned} V_{A1O} &= \frac{V_{DC}}{13}(S_{A1}S_{A4} - S_{A2}S_{A3}) + \frac{3V_{DC}}{13}(S_{A5}S_{A8} - S_{A6}S_{A7}) \\ &= \frac{V_{DC}}{13}\left[(S_{A1}S_{A4} - S_{A2}S_{A3}) + 3(S_{A5}S_{A8} - S_{A6}S_{A7})\right] \end{aligned} \tag{6.3}$$

Similarly the others pole voltages $V_{B1O}$ and $V_{C1O}$ can be written as

$$\begin{aligned} V_{B1O} &= \frac{V_{DC}}{13}(S_{B1}S_{B4} - S_{B2}S_{B3}) + \frac{3V_{DC}}{13}(S_{B5}S_{B8} - S_{B6}S_{B7}) \\ &= \frac{V_{DC}}{13}\left[(S_{B1}S_{B4} - S_{B2}S_{B3}) + 3(S_{B5}S_{B8} - S_{B6}S_{B7})\right] \end{aligned} \tag{6.4}$$

$$\begin{aligned} V_{C1O} &= \frac{V_{DC}}{13}(S_{C1}S_{C4} - S_{C2}S_{C3}) + \frac{3V_{DC}}{13}(S_{C5}S_{C8} - S_{C6}S_{C7}) \\ &= \frac{V_{DC}}{13}\left[(S_{C1}S_{C4} - S_{C2}S_{C3}) + 3(S_{C5}S_{C8} - S_{C6}S_{C7})\right] \end{aligned} \tag{6.5}$$

Similarly, two-level 'Inverter-B' pole voltages ($V_{A2O'}, V_{B2O'}, V_{C2O'}$) with respect to point-O' in terms of DC link voltages and switching states are given by

$$\left.\begin{aligned} V_{A2O'} &= \frac{9V_{DC}}{13}S_{A9} \\ V_{B2O'} &= \frac{9V_{DC}}{13}S_{B9} \\ V_{C2O'} &= \frac{9V_{DC}}{13}S_{C9} \end{aligned}\right\} \tag{6.6}$$

The actual phase voltages in terms of pole voltages can be expressed as:

$$\left.\begin{aligned} V_{A1A2} &= V_{A1O} + V_{OO'} - V_{A2O'} \\ V_{B1B2} &= V_{B1O} + V_{OO'} - V_{B2O'} \\ V_{C1C2} &= V_{C1O} + V_{OO'} - V_{C2O'} \end{aligned}\right\} \tag{6.7}$$

Where $V_{OO'}$ is the common mode voltage and given by

$$V_{OO'} = \frac{(V_{A2O'} + V_{B2O'} + V_{C2O'}) - (V_{A1O} + V_{B1O} + V_{C1O})}{3} \tag{6.8}$$

The three-phase motor voltages can be written in terms of pole voltages as:

$$\left.\begin{aligned} V_{A1A2} &= \frac{2}{3}(V_{A1O} - V_{A2O'}) - \frac{1}{3}(V_{B1O} - V_{B2O'}) - \frac{1}{3}(V_{C1O} - V_{C2O'}) \\ V_{B1B2} &= -\frac{1}{3}(V_{A1O} - V_{A2O'}) + \frac{2}{3}(V_{B1O} - V_{B2O'}) - \frac{1}{3}(V_{C1O} - V_{C2O'}) \\ V_{C1C2} &= -\frac{1}{3}(V_{A1O} - V_{A2O'}) - \frac{1}{3}(V_{B1O} - V_{B2O'}) + \frac{2}{3}(V_{C1O} - V_{C2O'}) \end{aligned}\right\} \tag{6.9}$$

Where $V_{A1A2}, V_{B1B2}, V_{C1C2}$ are the phase voltages of motor phase A, B and C respectively. Equation (6.9) can be written in matrix form as:

$$\begin{bmatrix} V_{A1A2} \\ V_{B1B2} \\ V_{C1C2} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} V_{A1O} - V_{A2O'} \\ V_{B1O} - V_{B2O'} \\ V_{C1O} - V_{C2O'} \end{bmatrix} \tag{6.10}$$

After putting the values of pole voltages from equations (6.3) - (4.25), phase voltages can be expressed as follows:

$$\begin{bmatrix} V_{A1A2} \\ V_{B1B2} \\ V_{C1C2} \end{bmatrix} = \frac{V_{DC}}{39}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} S_{A1}S_{A4} - S_{A2}S_{A3} + 3(S_{A5}S_{A8} - S_{A6}S_{A7}) - 9S_{A9} \\ S_{B1}S_{B4} - S_{B2}S_{B3} + 3(S_{B5}S_{B8} - S_{B6}S_{B7}) - 9S_{B9} \\ S_{C1}S_{C4} - S_{C2}S_{C3} + 3(S_{C5}S_{C8} - S_{C6}S_{C7}) - 9S_{C9} \end{bmatrix} \tag{6.11}$$

The relationship between orthogonal components $V_{qs}$, $V_{ds}$ of voltage space phasor in terms of phase voltages $V_{A1A2}$, $V_{B1B2}$, $V_{C1C2}$ is given by the transformation as:

$$\begin{bmatrix} V_{qs} \\ V_{ds} \\ V_{os} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/2 & 1/2 & 1/2 \end{bmatrix}\begin{bmatrix} V_{A1A2} \\ V_{B1B2} \\ V_{C1C2} \end{bmatrix} \tag{6.12}$$

These d-q components acts as inputs for the open-end winding induction motor model developed in section 2.4.2, to calculate the motor phase currents.

### 6.5 Simulation Results and Discussion

In order to verify the performance of proposed 18-level inverter scheme for open-end induction motor drive, extensive simulation studies are carried out. The mathematical model of 18-level inverter developed in section 6.4 is simulated in MATLAB/Simulink environment and simulation study is carried out in fixed-point simulation mode at a sampling time of 10 μSec. The mathematical model of 1.5kW open-end winding induction motor describe in subsection 2.4.2 is also developed in MATLAB/Simulink. The switching frequency ($f_c$) is kept constant at 500Hz for the entire range of modulation and DC link voltage ($V_{DC}$) is taken as 600V for simulation study. The open-end winding IM is operated in constant *V/f* mode under no-load condition covering the entire range of linear modulation. The modulation index ($m$) is defined as the ratio of the magnitude of the required voltage space phasor ($\left|V_r^*\right|$) to the maximum magnitude of the voltage space phasor ($V_{DC}$); the maximum value modulation index (m) in linear modulation region is 0.866. To cover the entire range of linear modulation four values of modulation indices ($m$) 0.16, 0.36, 0.52 and 0.8 correspond to frequencies ($f^*_m$) of 8, 18, 26 and 40Hz respectively are selected. The motor phase-A voltage ($V_{A1A2}$), phase-A current ($i_{A1A2}$), their harmonic spectra, inverters pole-A voltages ($V_{A1O}$, $V_{A2O'}$) and difference of inverters pole-A voltages ($V_{A1O}$ - $V_{A2O'}$) are considered as evaluation criteria. The simulation results are presented in Fig. 6.4 - Fig. 6.20 under steady-state as well as for transient-state conditions.

The waveforms for motor phase-A voltage ($V_{A1A2}$), phase-A current ($i_{A1A2}$), their harmonic spectrums, inverters pole-A voltages ($V_{A1O}$, $V_{A2O'}$) and difference of inverters pole-A voltages ($V_{A1O}$ - $V_{A2O'}$) at modulation index $m$ =0.16 are shown in Fig. 6.4 through Fig. 6.7. At this modulation index the modulating signals situated within the regions $R_1$ - $R_5$ and inverter operates in 5-level mode of operation. The fundamental frequency ($f^*_m$) of the motor for this modulation index is 8Hz. The motor phase-A voltage ($V_{A1A2}$) and current ($i_{A1A2}$) at modulation index $m$ =0.16 shown in Fig. 6.4 are equivalent to 5-level inverter waveforms. The harmonic spectrum of phase-A voltage and current with respect to their fundamental component for the modulation index $m$ =0.16 are shown in Fig. 6.5 and Fig. 6.6 respectively. It is evident from these spectrums that the THD of phase voltage and current are 12.31% and 1.14% respectively and lower order harmonics responsible for higher losses are significantly very low.

The pole-A voltages ($V_{A1O}$, $V_{A2O'}$) and difference of inverters pole-A voltages ($V_{A1O}$ - $V_{A2O'}$) are shown in Fig. 6.7 for 5-level mode of operation. It may be observed from pole voltages waveform that 9-level inverter-A operates in 5-level mode and attains the pole voltage values correspond to -(4/13)$V_{DC}$, -(3/13)$V_{DC}$, -(2/13)$V_{DC}$, -(1/13)$V_{DC}$ and 0; while the two-level inverter-B is clamped at (9/13)$V_{DC.}$ The difference of pole voltages ($V_{A1O}$ - $V_{A2O'}$) switch between five voltage levels -$V_{DC}$, -(12/13)$V_{DC}$, -(11/13)$V_{DC}$, -(10/13)$V_{DC}$ and -(9/13)$V_{DC}$ which confirm the 5-level mode of operation.

Fig. 6.8 through Fig. 6.11 illustrate the simulated results obtained when inverter operates in 10-level mode of operation. For the value of modulation index $m$=0.36 the three modulating waves reside in regions $R_1$ - $R_{10}$ so inverter operates in 10-level mode of operation. The motor operates at fundamental frequency $f^*_m$=18Hz. The motor phase voltage and current waveforms shown in Fig. 6.8 are further refine and approach towards sinusoidal. It can be observed from pole voltage waveform shown in Fig. 6.11 that ACHB Inverter-A pole voltage switch between all 9-levels ±(4/13)$V_{DC}$, ± (3/13)$V_{DC}$, ± (2/13)$V_{DC}$, ±(1/13)$V_{DC}$ and zero; whereas inverter-B operate in two-level mode only for half of the duration of fundamental cycle and for remaining half period it is still clamped at (9/13)$V_{DC}$. The difference of pole voltages (Fig. 6.11 bottom trace) contains ten distinct voltage levels corresponding to the levels -$V_{DC}$, -(12/13)$V_{DC}$, -(11/13)$V_{DC}$, -(10/13)$V_{DC}$, -(9/13)$V_{DC}$, -(8/13)$V_{DC}$, -(7/13)$V_{DC}$, -(6/13)$V_{DC}$, -(5/13)$V_{DC}$ and -(4/13)$V_{DC}$. The harmonic spectrums of phase-A voltage and current are presented in Fig. 6.9 and Fig. 6.10 respectively. The harmonic spectrum of phase voltage is further improved with the THD of 2.79% and the magnitude of dominant harmonic component is less than 1.5% (Fig. 6.9 b). The THD of phase current is slightly increased from 1.14% (in 5-level mode) to 1.43% (in 10-level mode) due to presence of lower order harmonics.

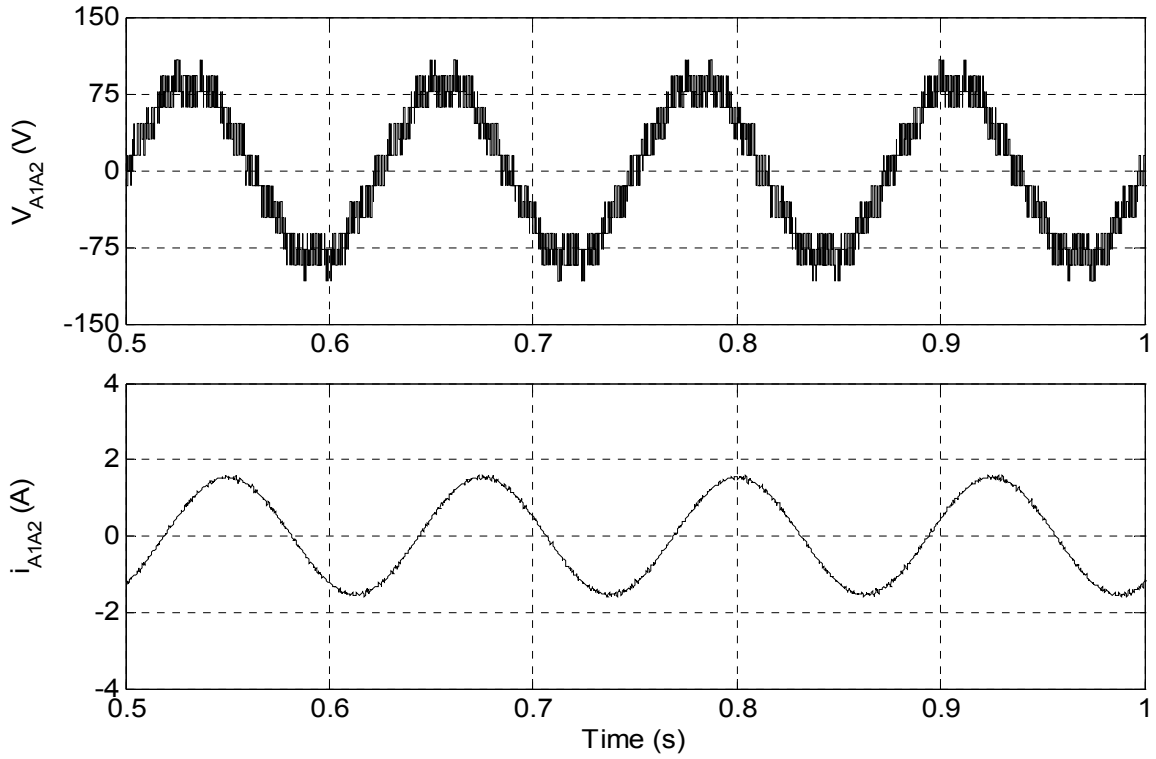



Fig. 6.4: Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A2A2}$ (lower trace) of 18-level inverter fed open-end IM drive at no load ($m$=0.16; $f^*_m$ =8Hz; 5-level mode)

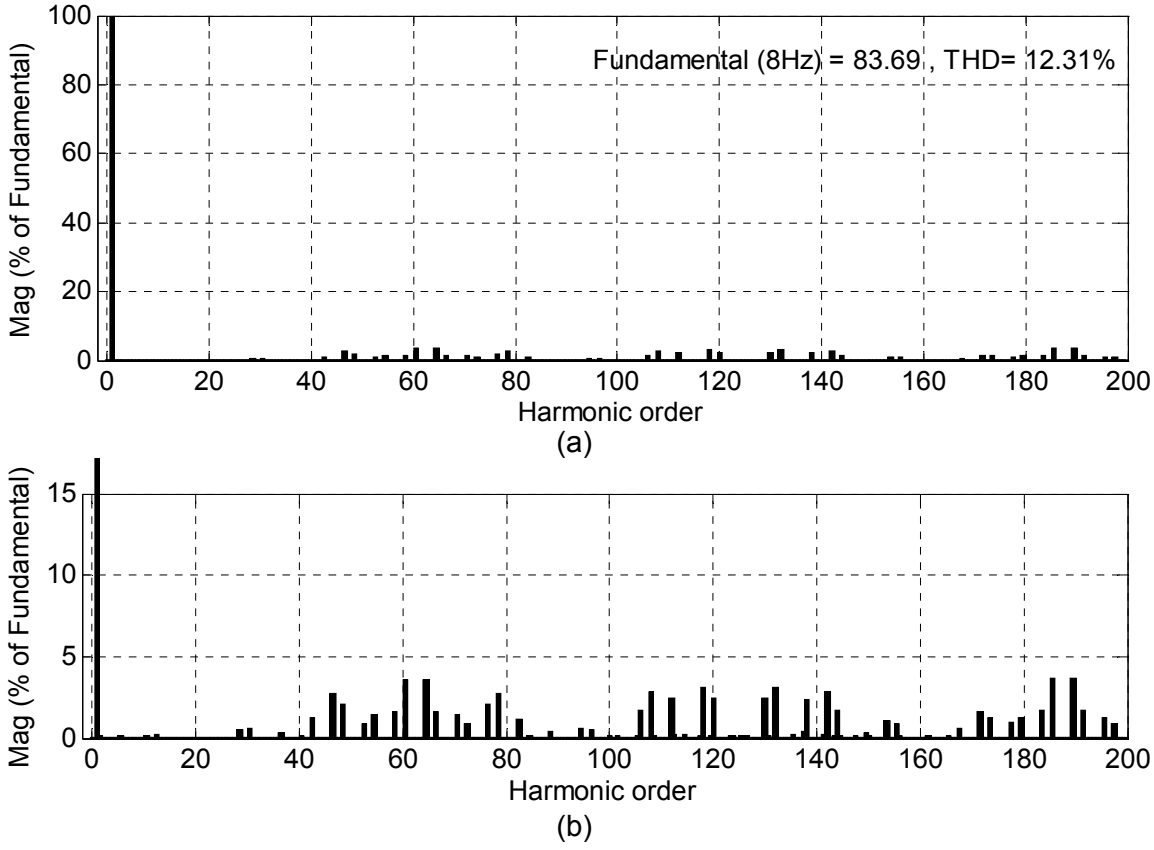



Fig. 6.5: (a) Harmonic spectrum of phase-A voltage ($V_{A1A2}$) at $m$=0.16; $f^*_m$ =8Hz
(b) Zoom view of harmonic spectrum shown in (a)

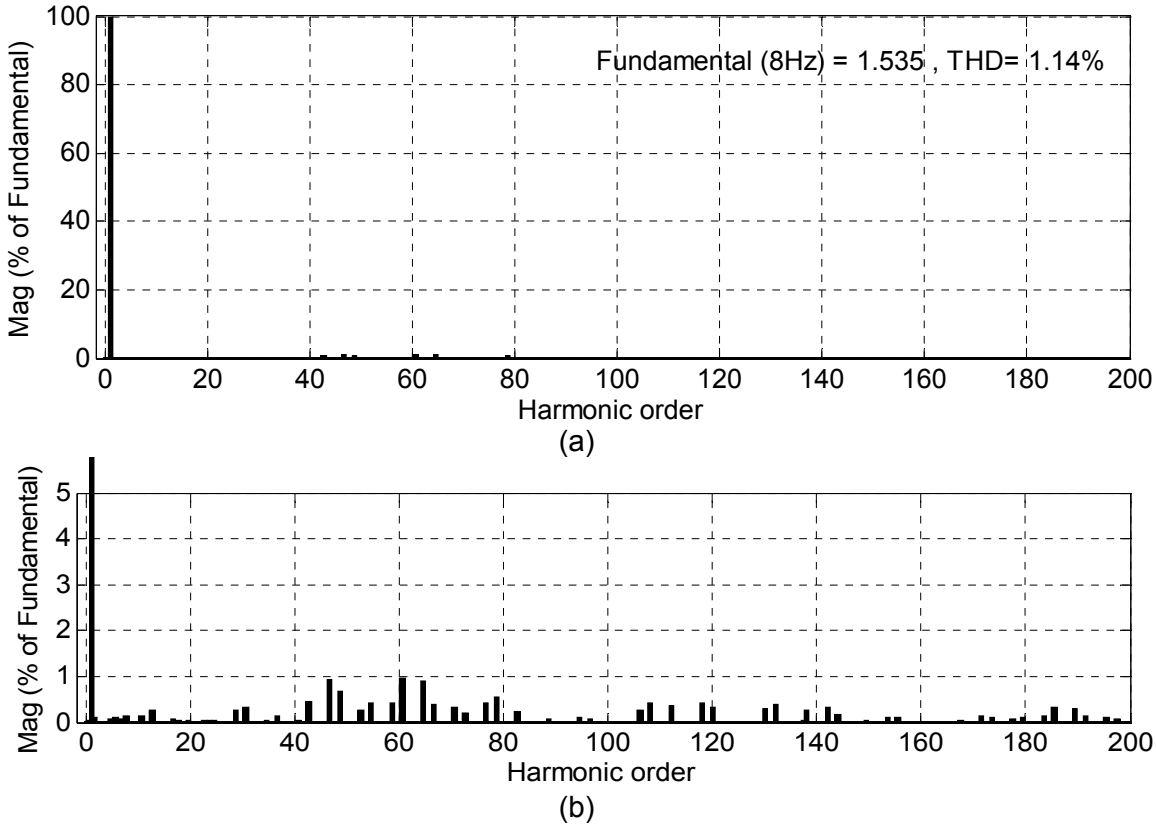



Fig. 6.6: (a) Harmonic spectrum of phase-A current ($i_{A1A2}$) at $m$=0.16; $f^*_m$ =8Hz
(b) Zoom view of harmonic spectrum shown in (a)

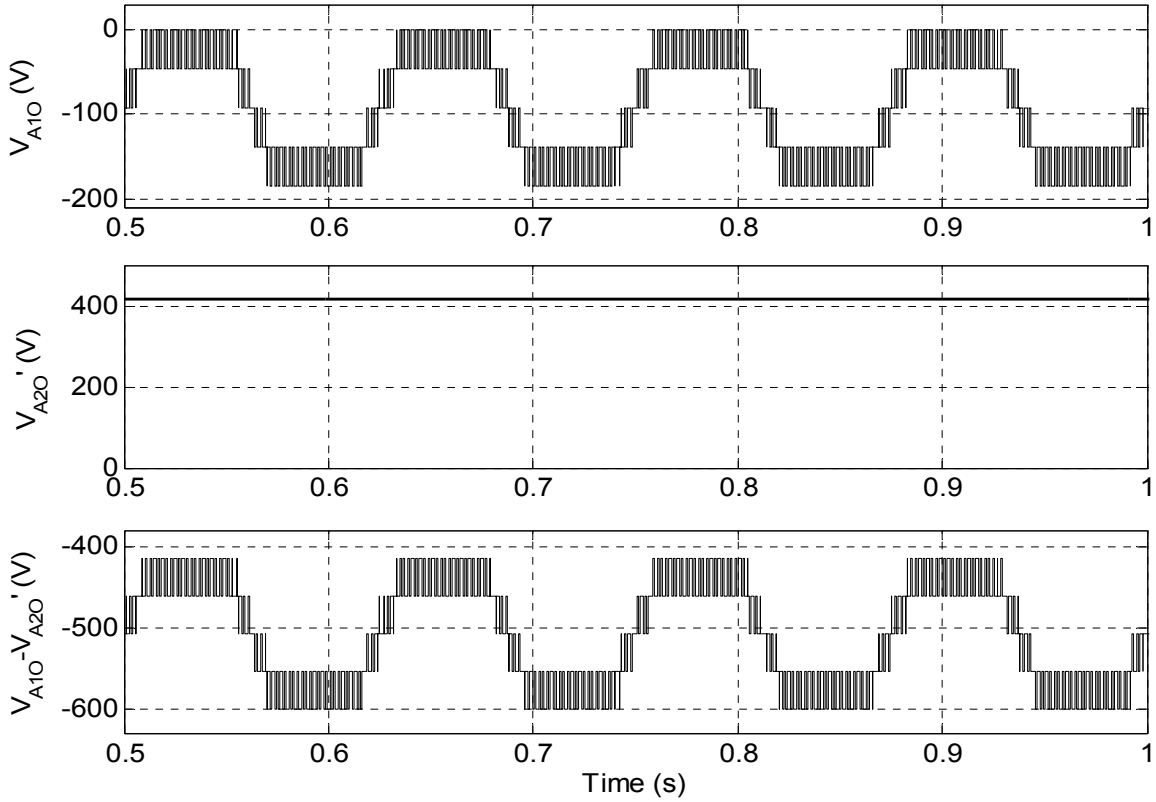



Fig. 6.7 :Top trace; Inverter-A pole voltage ($V_{A1O}$), Middle trace; Inverter-B pole voltage ($V_{A2O'}$), Bottom trace; Difference of Inverter-A and -B pole voltages ($V_{A1O}$ - $V_{A2O'}$) at $m$=0.16; $f^*_m$ =8Hz (5-level mode)

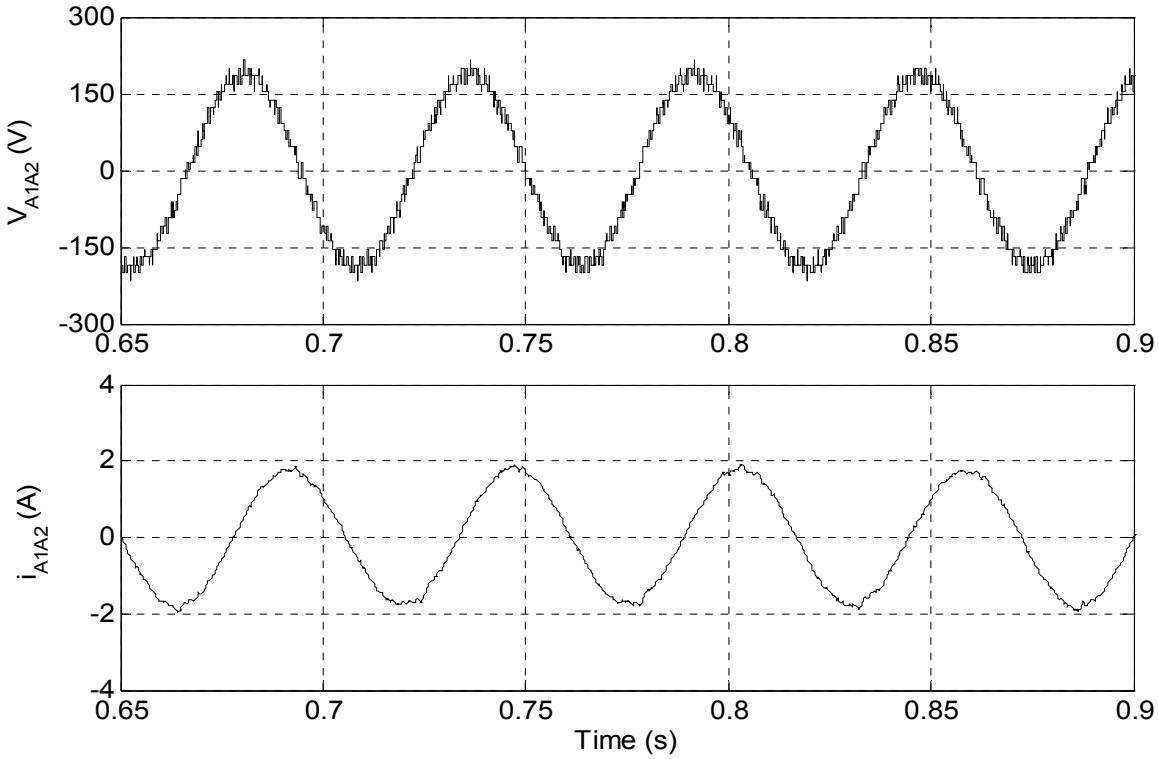



Fig. 6.8: Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A2A2}$ (lower trace) of 18-level inverter fed open-end IM drive at no load ($m$=0.36; $f^*_m$ =18Hz; 10-level mode)

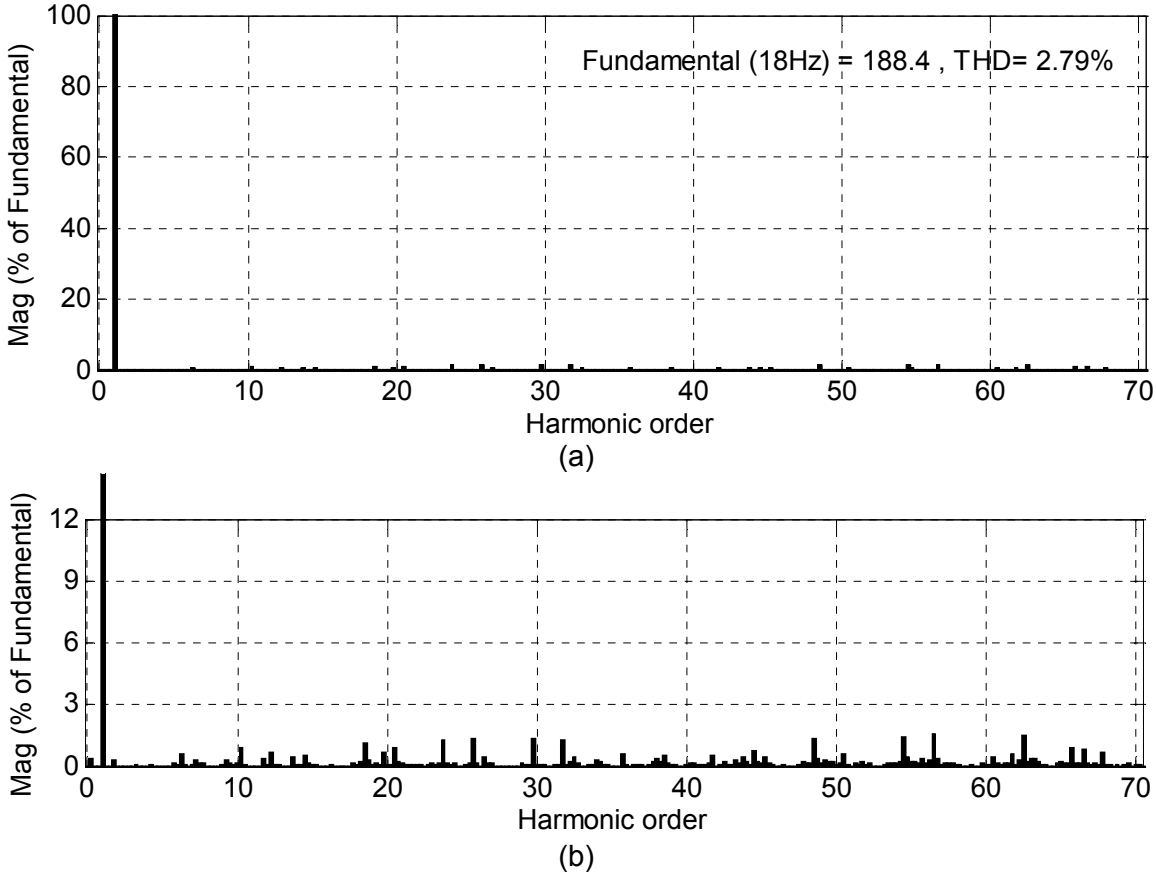



Fig. 6.9: (a) Harmonic spectrum of phase-A voltage ($V_{A1A2}$) at $m$=0.36; $f^*_m$ =18Hz
(b) Zoom view of harmonic spectrum shown in (a)

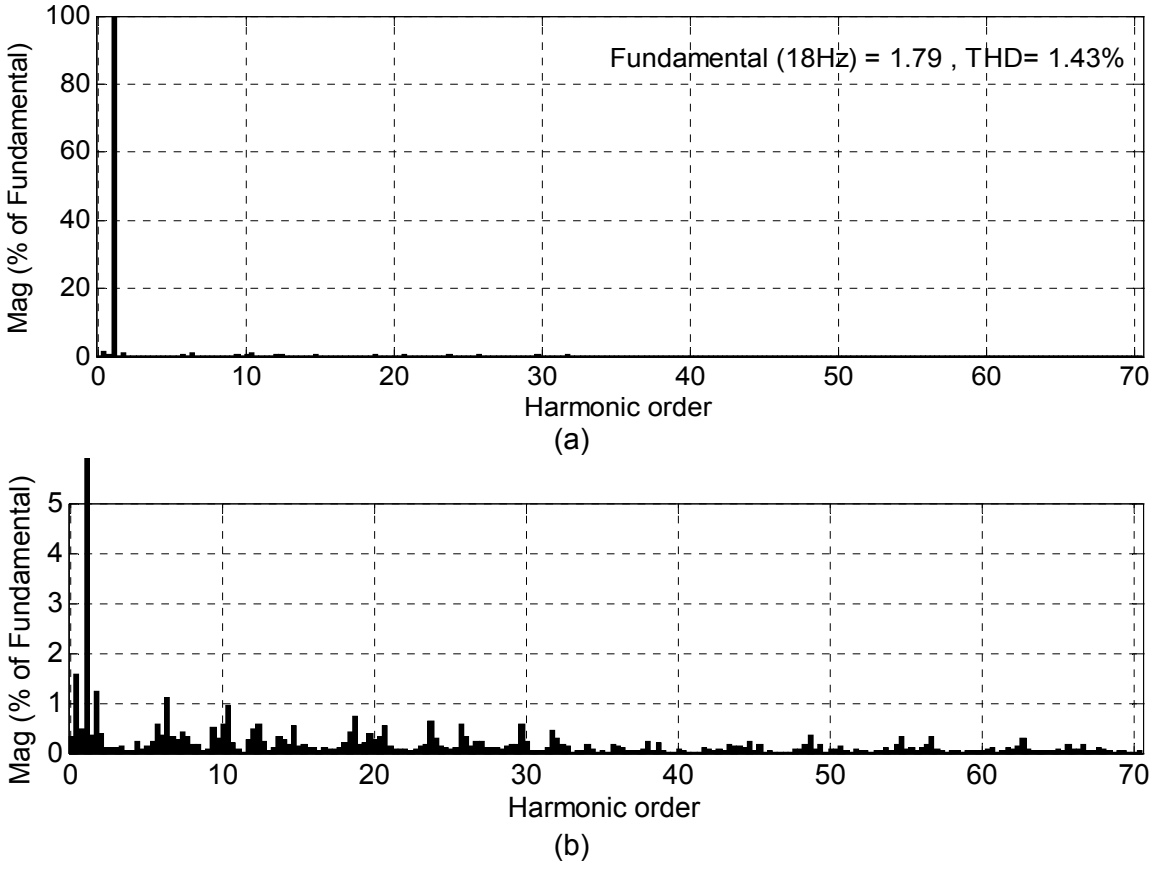



Fig. 6.10: (a) Harmonic spectrum of phase-A current ($i_{A1A2}$) at $m$=0.36; $f^*_m$ =18Hz
(b) Zoom view of harmonic spectrum shown in (a)

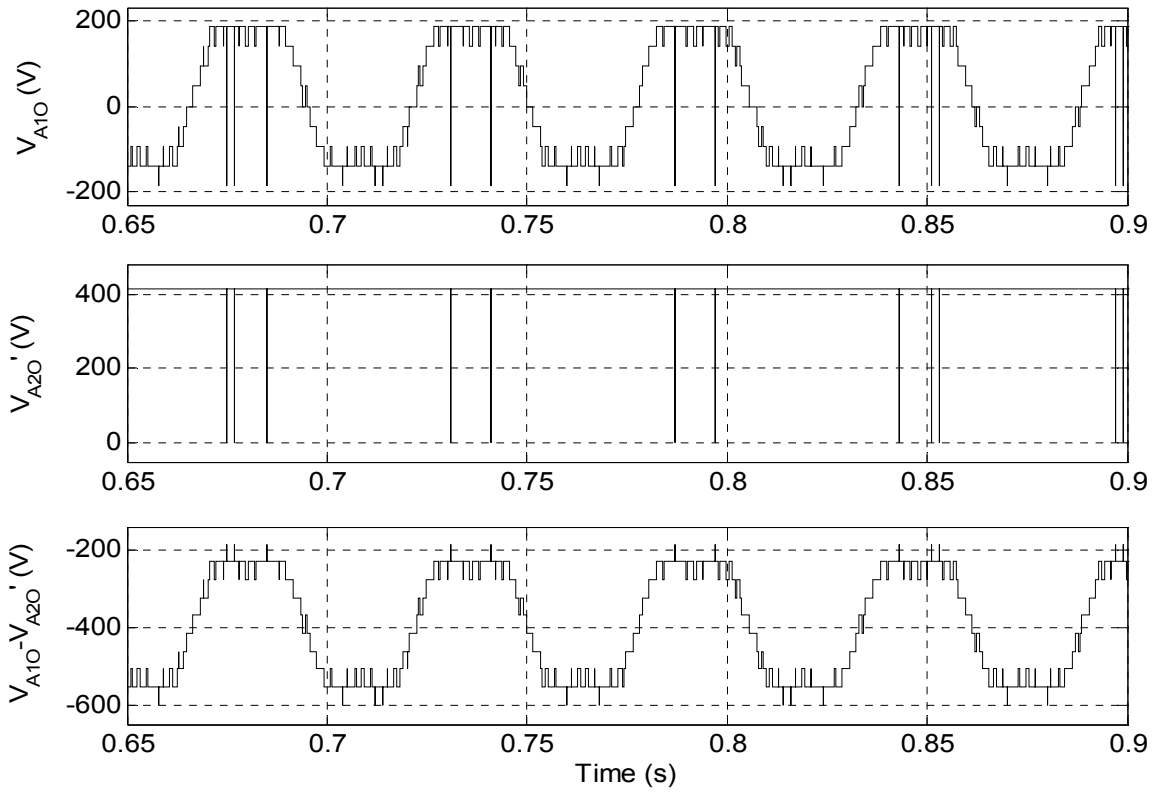



Fig. 6.11 :Top trace; Inverter-A pole voltage ($V_{A1O}$), Middle trace; Inverter-B pole voltage ($V_{A2O'}$), Bottom trace; Difference of Inverter-A and -B pole voltages ($V_{A1O}$ - $V_{A2O'}$) at $m$=0.36; $f^*_m$ =18Hz (10-level mode)

Similar types of results are obtained for the modulation index $m$=0.52 correspond to 13-level mode of operation. The motor is operated at fundamental frequency $f^*_m$=26Hz. The range of modulating signals varies from region $R_1$-$R_{13}$ and thirteen levels ($L_1$-$L_{13}$) are applied across the motor phase winding. The simulated phase voltage and current waveforms are shown in Fig. 6.12. It is evident from inverter-B pole-A voltage ($V_{A2O'}$) waveform shown in Fig. 6.15 (middle trace) that inverter-B which operates at higher DC link voltage change its state from (9/13)$V_{DC}$ to zero once in a cycle hence switching losses are reduced. Inverter-A operates in 9-level mode and takes all nine voltage levels correspond to ±(4/13)$V_{DC}$, ±(3/13)$V_{DC}$, ±(2/13)$V_{DC}$, ±(1/13)$V_{DC}$ and zero (upper trace of Fig. 6.15). The thirteen level realized for modulation index $m$=0.52 are -$V_{DC}$, -(12/13)$V_{DC}$, -(11/13)$V_{DC}$, -(10/13)$V_{DC}$, -(9/13)$V_{DC}$, -(8/13)$V_{DC}$, -(7/13)$V_{DC}$, -(6/13)$V_{DC}$, -(5/13)$V_{DC}$, -(4/13)$V_{DC}$, -(3/13)$V_{DC}$, -(2/13)$V_{DC}$ and -(1/13)$V_{DC}$ as depicted in pole voltage waveform shown in bottom trace of Fig. 6.15. The THD of phase-A voltage (Fig. 6.13) and current (Fig. 6.14) are 2.69% and 1.34% respectively. The magnitude of dominant harmonic component of voltage is 1% and current is less than 2%.

Another set of simulation results at modulation index $m$=0.8 is shown in Fig. 6.16 through Fig. 6.19 in same order as the previous set of results. Motor runs at fundamental frequency $f^*_m$=40Hz. The range of modulating signals varies from region $R_1$-$R_{18}$ and all eighteen levels are applied across the motor phase winding. The simulated waveforms of phase-A voltage and current shown in Fig. 6.16 are almost sinusoidal in nature. Although the pole voltages waveforms (Fig. 6.19) having the same voltage levels as they posses in 13-level mode of operation, but their difference (Fig. 6.19 bottom trace) is having eighteen voltage levels correspond to -$V_{DC}$, -(12/13)$V_{DC}$, -(11/13)$V_{DC}$, -(10/13)$V_{DC}$, -(9/13)$V_{DC}$, -(8/13)$V_{DC}$, -(7/13)$V_{DC}$, -(6/13)$V_{DC}$, -(5/13)$V_{DC}$, -(4/13)$V_{DC}$, -(3/13)$V_{DC}$, -(2/13)$V_{DC}$, -(1/13)$V_{DC}$, 0, +(1/13)$V_{DC}$, +(2/13)$V_{DC}$, +(3/13)$V_{DC}$ and +(4/13)$V_{DC}$. It is evident in this mode also that inverter-B which operate at higher DC link voltage switched its state from (9/13)$V_{DC}$ to zero once in a fundamental cycle hence less switching losses occur in two-level inverter-B. The harmonic spectra of phase voltage and current are presented in Fig. 6.17 and Fig. 6.18 respectively.

The performance of proposed inverter fed open-end winding IM drive system is also investigated during transient state. The inverter operation is suddenly change from 5-level mode to 18-level mode by changing the modulation index from 0.16 (5-level mode) to 0.8 (18-level mode) and vice versa at no-load. Fig. 6.20(a) shows the motor phase-A voltage ($V_{A1A2}$) and current ($i_{A1A2}$) during sudden change from 5-level to 18-level mode of operation. The changeover from lower to higher level mode of operation takes place instantaneously and drive attains its steady state within few cycles. Fig. 6.20(b) shows the motor phase-A voltage ($V_{A1A2}$) and current ($i_{A1A2}$) during sudden change from 18-level to 5-level mode of operation. The changeover from higher to lower level mode of operation also takes place instantaneously and drive attains its steady state very quickly.

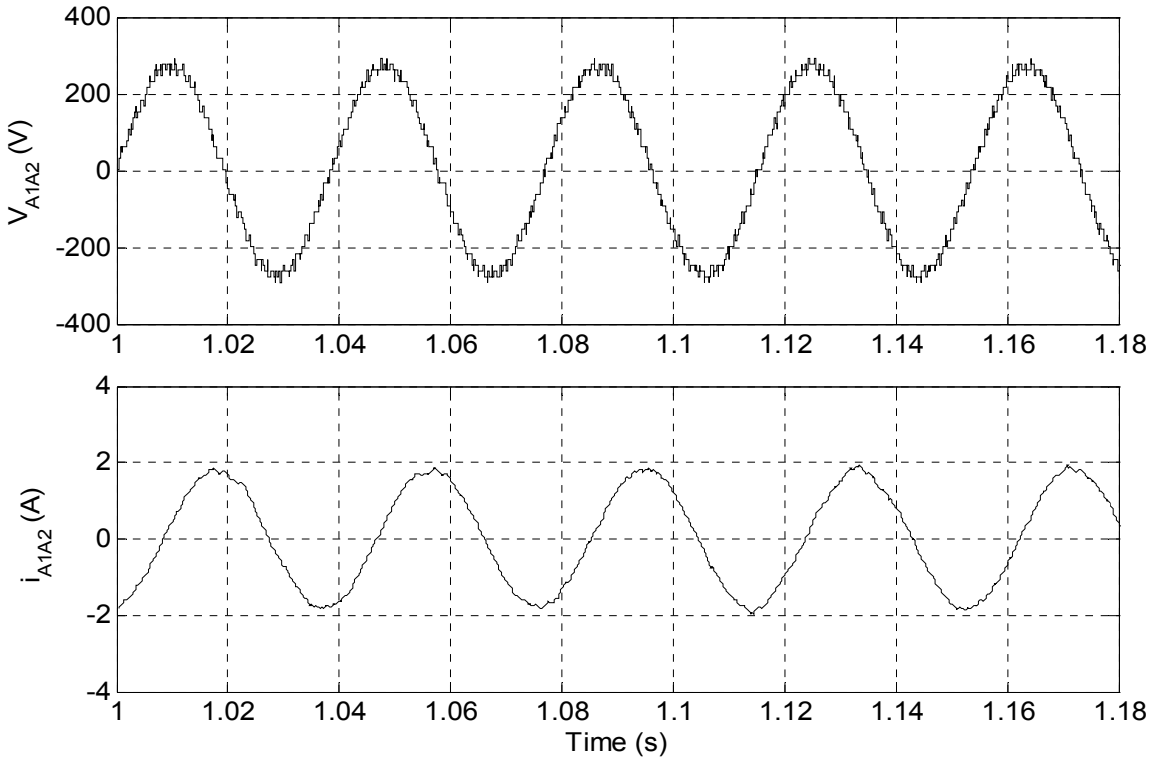



Fig. 6.12: Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A2A2}$ (lower trace) of 18-level inverter fed open-end IM drive at no load ($m$=0.52; $f^*_m$ =26Hz; 13-level mode)

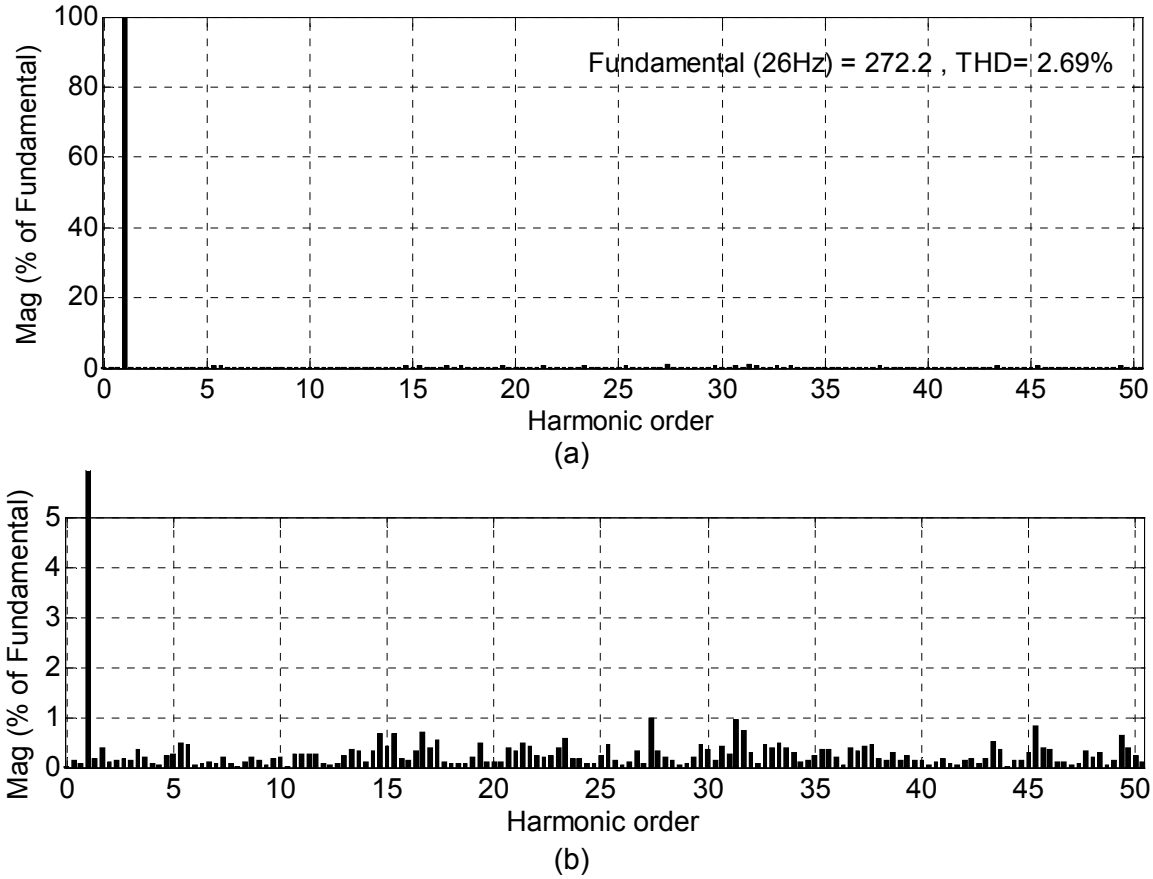



Fig. 6.13: (a) Harmonic spectrum of phase-A voltage ($V_{A1A2}$) at $m$=0.52; $f^*_m$ =26Hz
(b) Zoom view of harmonic spectrum shown in (a)

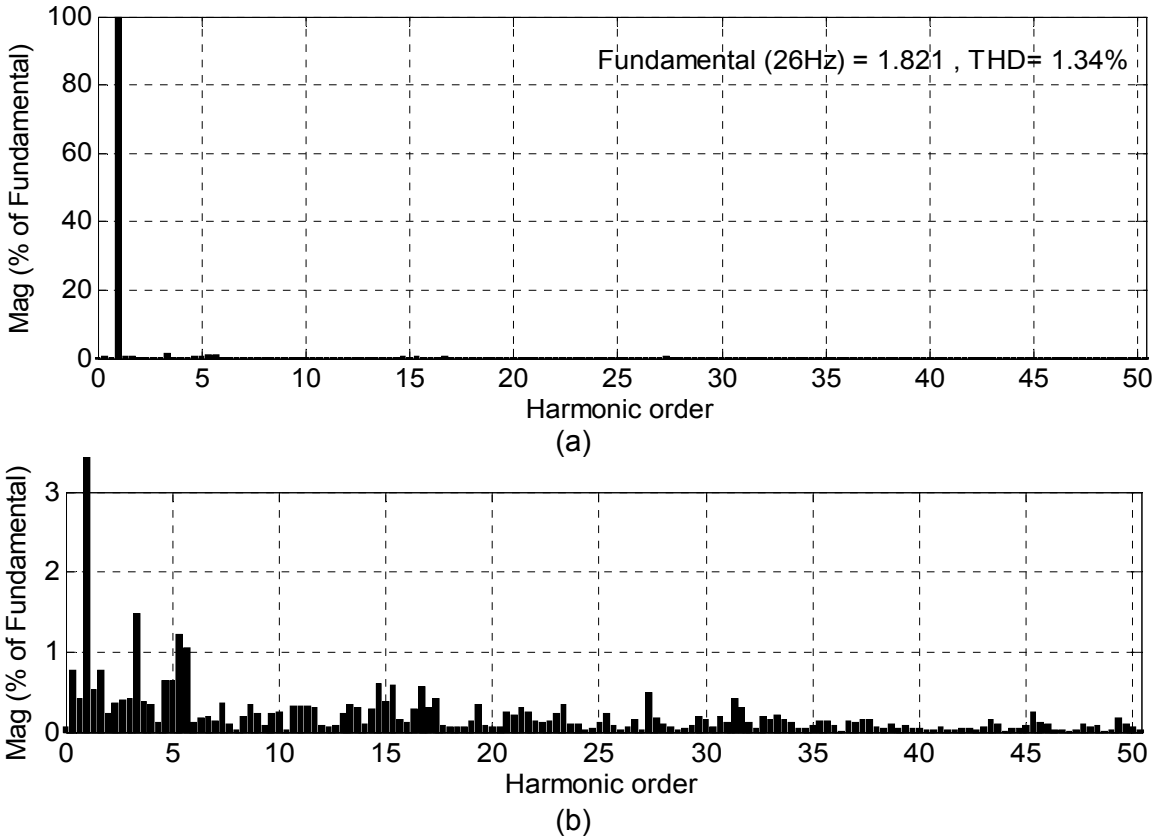



Fig. 6.14: (a) Harmonic spectrum of phase-A current ($i_{A1A2}$) at $m$=0.52; $f^*_m$ =26Hz
(b) Zoom view of harmonic spectrum shown in (a)

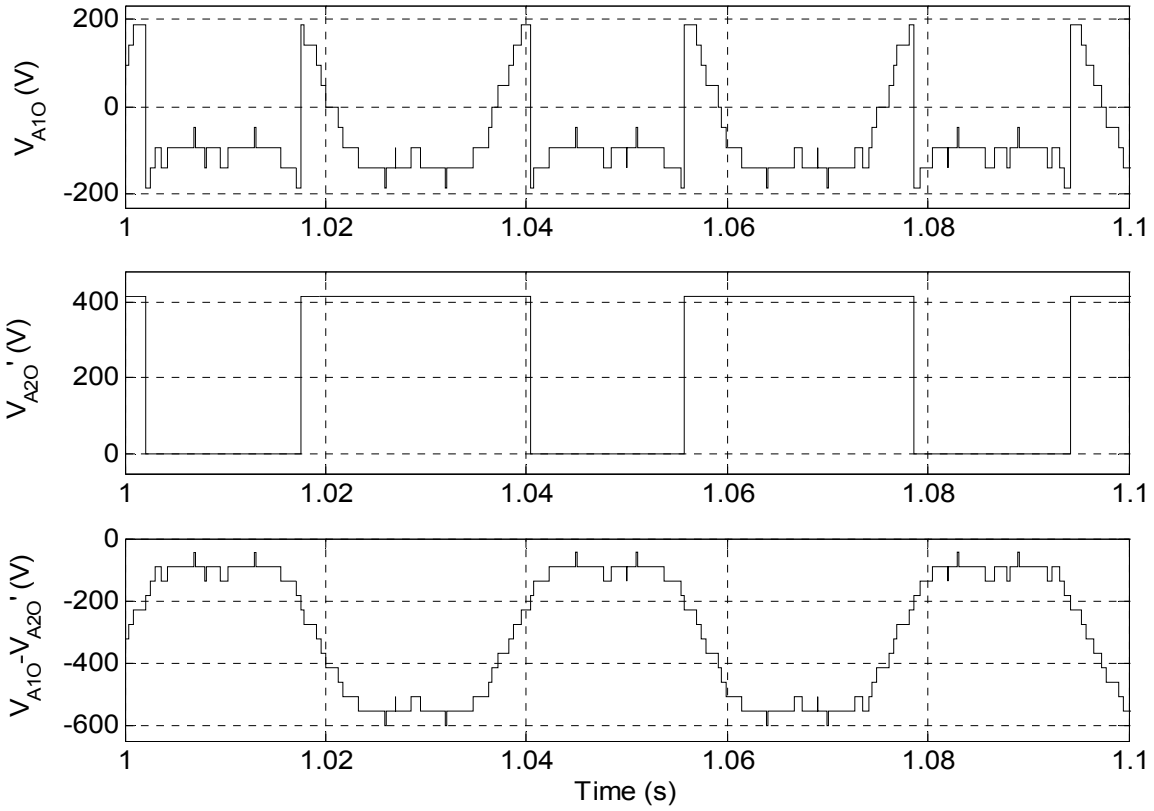



Fig. 6.15 :Top trace; Inverter-A pole voltage ($V_{A1O}$), Middle trace; Inverter-B pole voltage ($V_{A2O'}$), Bottom trace; Difference of Inverter-A and -B pole voltages ($V_{A1O}$ - $V_{A2O'}$) at $m$=0.52; $f^*_m$ =26Hz (13-level mode)

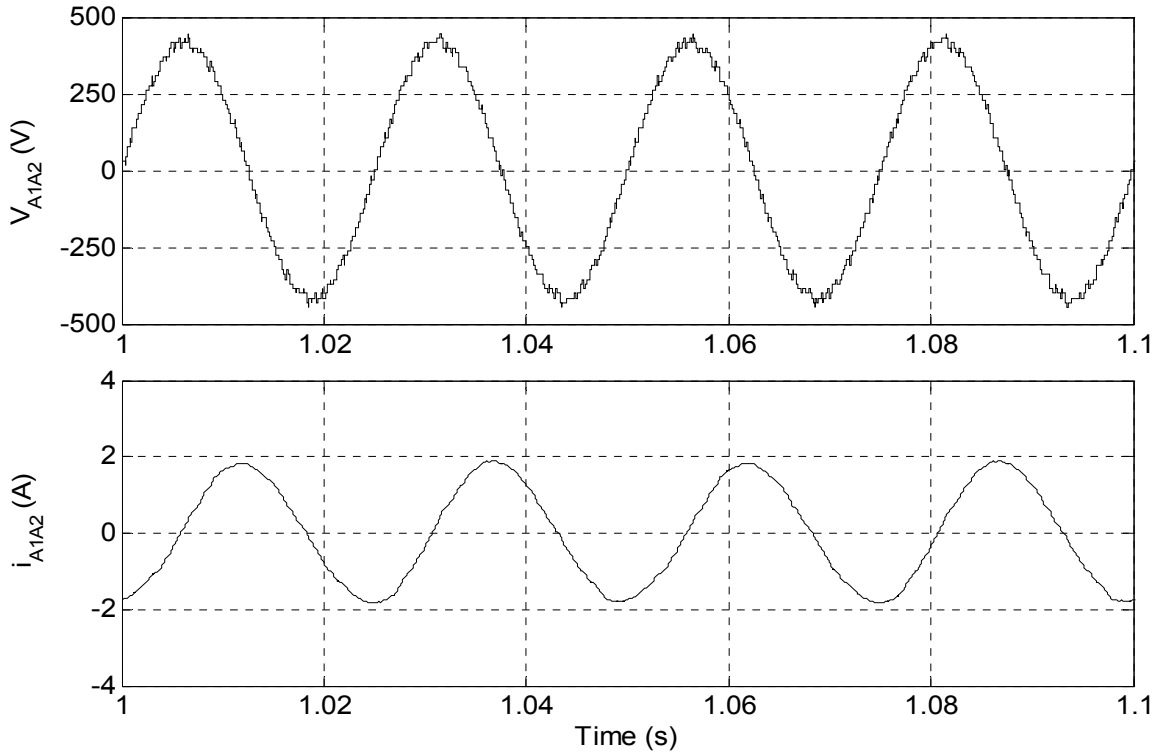



Fig. 6.16: Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A2A2}$ (lower trace) of 18-level inverter fed open-end IM drive at no load ($m$=0.8; $f^*_m$ =40Hz; 18-level mode)

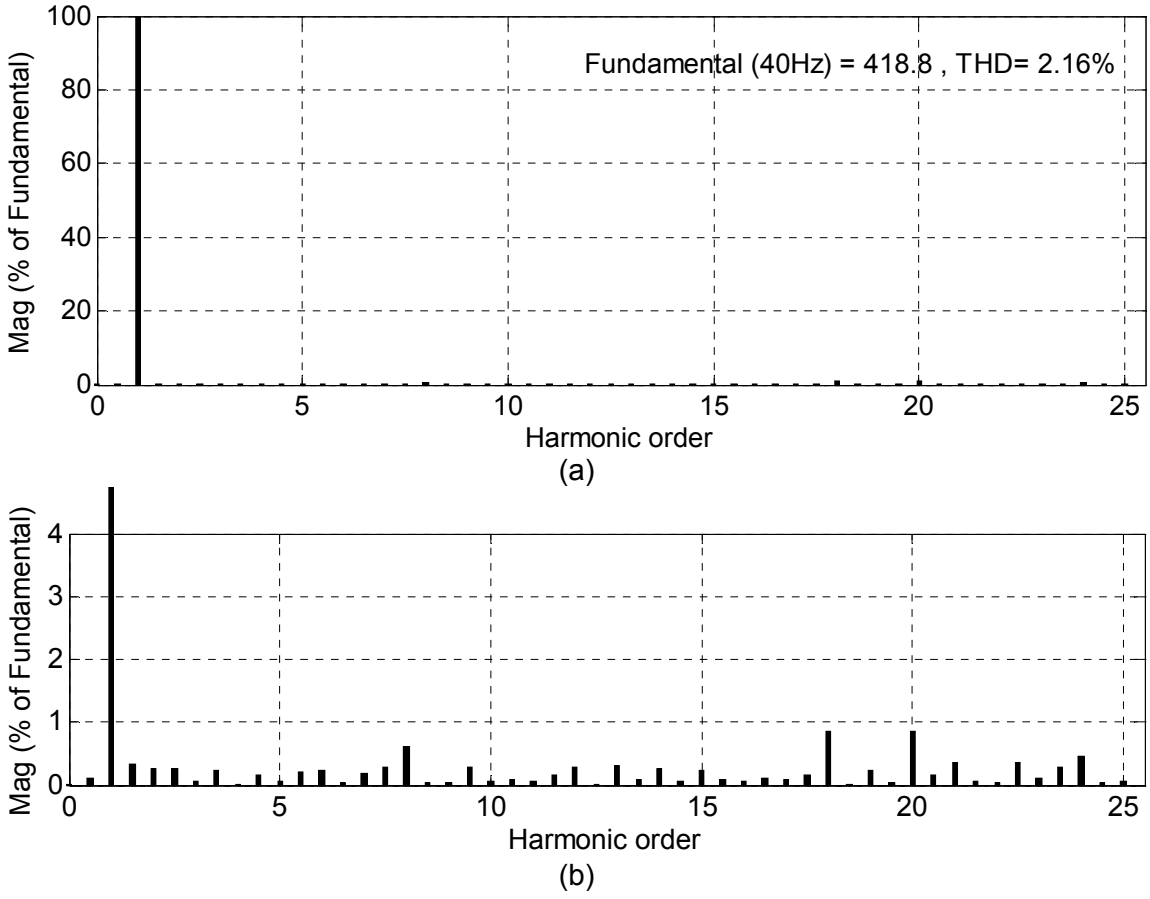



Fig. 6.17: (a) Harmonic spectrum of phase-A voltage ($V_{A1A2}$) at $m$=0.8; $f^*_m$ =40Hz
(b) Zoom view of harmonic spectrum shown in (a)

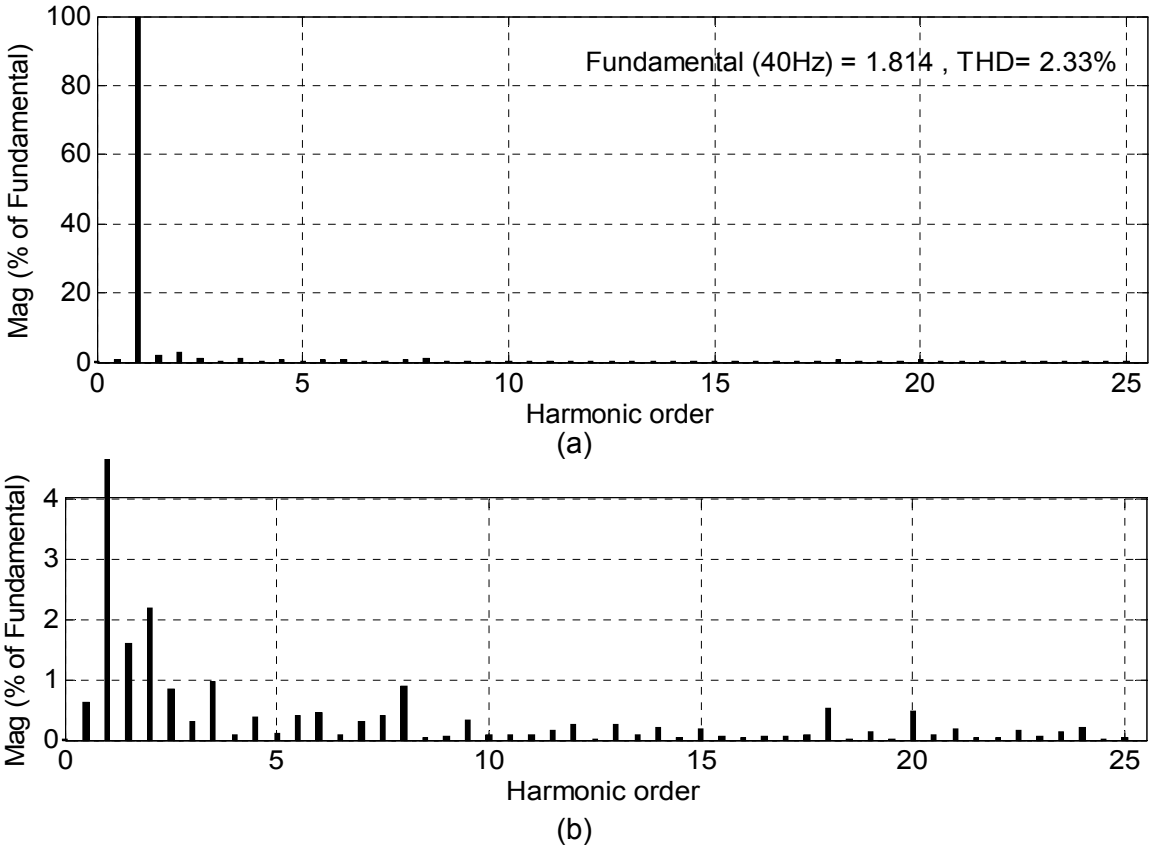



Fig. 6.18: (a) Harmonic spectrum of phase-A current ($i_{A1A2}$) at $m$=0.8; $f^*_m$ =40Hz
(b) Zoom view of harmonic spectrum shown in (a)

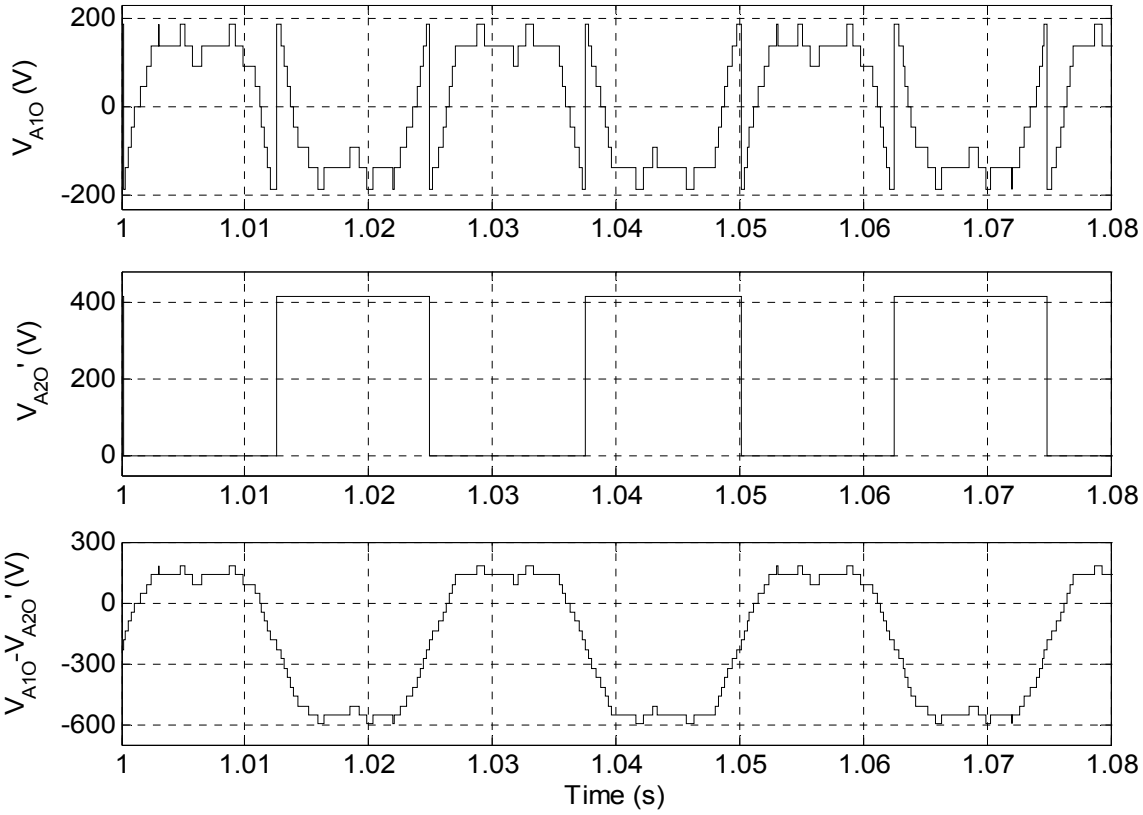
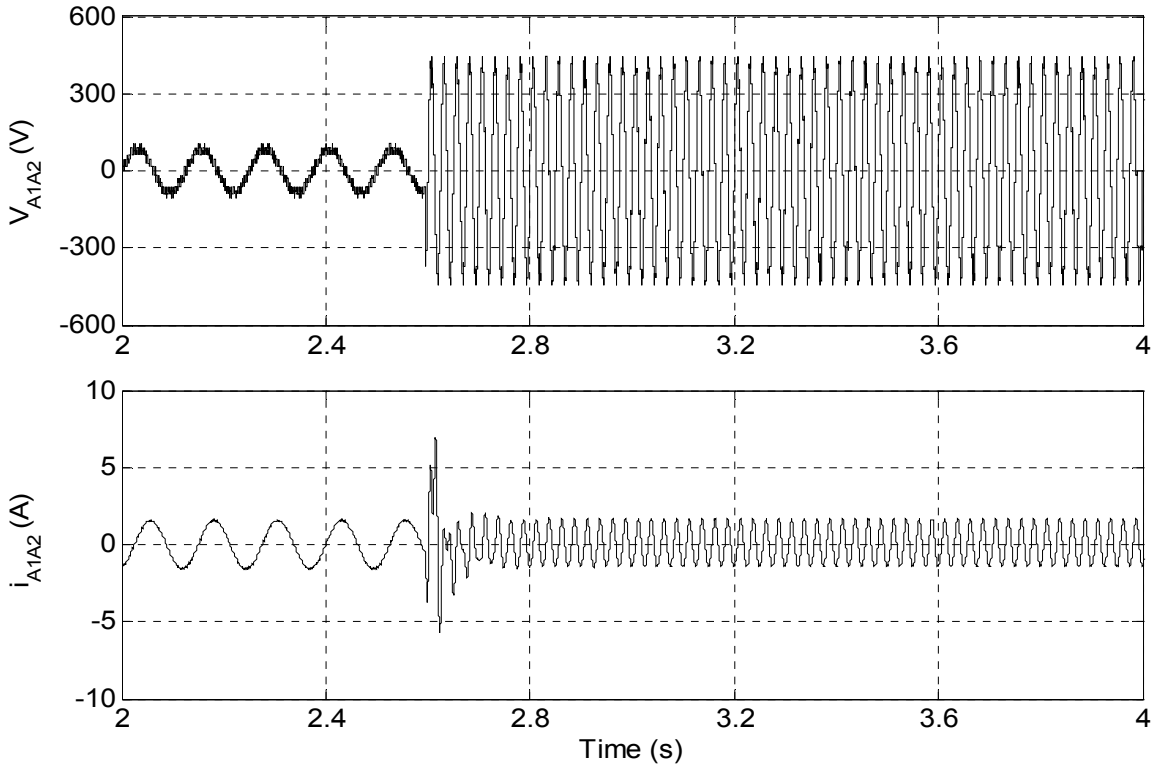
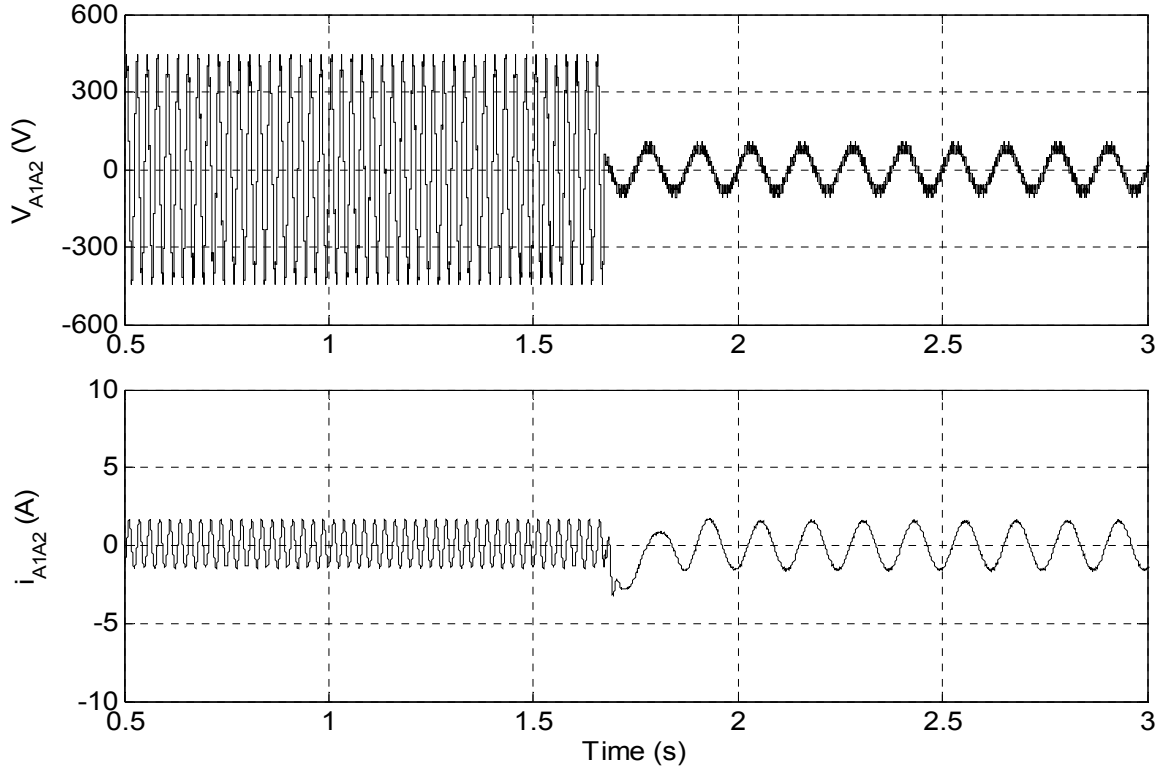



Fig. 6.19 :Top trace; Inverter-A pole voltage ($V_{A1O}$), Middle trace; Inverter-B pole voltage ($V_{A2O'}$), Bottom trace; Difference of Inverter-A and -B pole voltages ($V_{A1O}$ - $V_{A2O'}$) at $m$=0.8; $f^*_m$ =40Hz (18-level mode)




(a)




(b)

Fig. 6.20: (a) Motor phase-A voltage $V_{A1A2}$ (upper trace) and current $i_{A1A2}$ (lower trace) waveforms under sudden change in modulation index from 0.16 (5-level mode) to 0.8 (18-level mode) at no-load
(b) Motor phase-A voltage $V_{A1A2}$ (upper trace) and current $i_{A1A2}$ (lower trace) waveforms under sudden change in modulation index from 0.8 (18-level mode) to 0.16 (5-level mode) to at no-load

### 6.6 Performance Comparison

The performance of 18-level inverter is compared with hybrid 9-level inverter proposed in Chapter-5, in terms of level of operation, THD of phase-A voltage and dominant harmonic component of phase-A voltage under different modulation indices and results are tabulated in Table 6.4. It can be observed in Table 6.4 that 18-level inverter shows better performance over hybrid 9-level inverter throughout the modulation range even though the switching frequency of 18-level inverter is half of the switching frequency of hybrid 9-level inverter. The simulation results shown in Fig. 6.4 - Fig. 6.20 confirm the viability of proposed 18-level inverter scheme for open-end IM drive system.

Table 6.4: Performance comparisons of 18-level inverter with hybrid 9-level inverter

| Performance parameter | Type of inverter | Modulation index(*m)* | | | |
|---|---|---|---|---|---|
| | | 0.16 | 0.36 | 0.52 | 0.8 |
| Level of operation | 18-level inverter[a] | 5 | 10 | 13 | 18 |
| | Hybrid 9-level inverter[b] | 3 | 5 | 7 | 9 |
| RMS of phase-A voltage (*V*) | 18-level inverter[a] | 60.02 | 133.7 | 192.3 | 296.4 |
| | Hybrid 9-level inverter[b] | 48.48 | 103.4 | 148 | 227.4 |
| RMS of phase-A current (*A*) | 18-level inverter[a] | 1.086 | 1.249 | 1.276 | 1.281 |
| | Hybrid 9-level inverter[b] | 0.823 | 0.966 | 0.983 | 0.993 |
| Frequency of phase voltage (*Hz)* | 18-level inverter[a] | 8 | 18 | 26 | 40 |
| | Hybrid 9-level inverter[b] | 8 | 18 | 26 | 40 |
| THD of phase-A voltage in % | 18-level inverter[a] | 12.31 | 2.79 | 2.69 | 2.16 |
| | Hybrid 9-level inverter[b] | 41.18 | 6.86 | 3.66 | 1.44 |
| Order of dominant voltage harmonic (amplitude in %) | 18-level inverter[a] | 60 (4.0) | 57 (1.5) | 27 (1.0) | 20 (0.98) |
| | Hybrid 9-level inverter[b] | 250±1 (18.2) | 111±2 (3.64) | 77±2 (4.2) | 57 (2.2) |
| THD of phase-A current in % | 18-level inverter[a] | 1.14 | 1.43 | 1.34 | 2.33 |
| | Hybrid 9-level inverter[b] | 2.77 | 1.14 | 0.94 | 1.85 |
| Order of dominant current harmonic (amplitude in %) | 18-level inverter[a] | 60 (0.98) | 2 (1.2) | 3 (1.5) | 3 (2.2) |
| | Hybrid 9-level inverter[b] | 250±1 (1.20) | 39 (0.8) | 13 (1.5) | 13 (1.45) |

Note: [a] Switching frequency of 18-level inverter is 500Hz
[b] Switching frequency of hybrid 9-level inverter is 1kHz

## 6.7 Conclusion

In this chapter an 18-level inverter topology is proposed for open-end winding induction motor drive. The proposed topology is realized using the same numbers of IGBTs as those are required by hybrid 9-level inverter presented in Chapter-5. The proposed topology produces a voltage space phasor of maximum amplitude of $V_{DC}$ whereas the maximum DC link voltage used is (9/13)$V_{DC}$, this feature further reduces the size of inverter. In the proposed 18-level inverter configuration the two-level inverter which operates at higher DC-link voltage is switched less frequently than the inverter with lower DC-link voltage for the entire range of modulation hence switching losses are reduced. The proposed topology is compared with conventional topologies in terms of number of components used and it is found that the proposed 18-level inverter completely eliminates 816 clamping diodes and 17 capacitors which are required in 18-level NPC. It also eliminates 408 balancing capacitors which are required in 18-level FC inverter. The proposed topology uses only seven isolated DC sources as compared to conventional CHB topology which requires 27 isolated DC supplies. However, out of seven isolated DC sources six sources are of lower voltage rating; these lower voltage rating isolated sources can be easily implemented using photovoltaic power cells.

A switching function based mathematical model of the proposed 18-level inverter is developed and the performance is evaluated by running a 1.5kW open-end winding induction motor at no-load under same operating conditions as that of use to evaluate the performance of hybrid 9-level inverter proposed in Chapter-5. Motor phase voltage, phase current, their harmonic spectrums, inverter pole voltages, difference in inverter pole voltages and sudden change in modulation index are considered as an evaluation criteria for performance evaluation. The inverter switching frequency is kept half of the switching frequency of hybrid 9-level inverter proposed in Chapter-5. The MATLAB/Simulink based simulation studies have been carried out and results are presented. From the simulation results, it can be observed that the proposed 18-level inverter gives reduced harmonic distortion even at half of the switching frequency when compared with hybrid 9-level inverter fed open-end winding IM drive.

# CHAPTER 7: SYSTEM DEVELOPMENT AND EXPERIMENTATION

*[This chapter presents the design of system hardware, RT-Lab Meta Controller interfacing and experimentation for the prototype models of different topologies of MLIs to validate the simulation results presented in previous chapters. The development for laboratory prototype models of 5-Level Inverter (topology-1), 9-Level Inverter (topology-2) and Hybrid 9-Level Inverter (topology-3) for open-end IMD is carried out. RT-Lab real time digital simulator with Spartan-3 board is used for real time interface with MATLAB/Simulink environment. A level shifted triangular carrier based space vector pulse width modulation (SVPWM) algorithm as describe in previous chapter is implemented on RT-Lab real time controller to generate gate pulses for the IGBTs of developed prototype inverters. To evaluate the performance of the prototype inverters experimentation is carried out. Further, these experimental studies are validated with simulation results obtained using the experimental parameters.]*

## 7.1 Introduction

The multi-level voltage across the phase windings of open-end winding IM can be obtained by using different combination of inverter at both ends. In the previous chapters extensive simulation study is carried out on D2L inverter, 5-level inverter, 9-level inverter, hybrid 9-level inverter and 18-level inverter for induction motor drive. In order to validate the simulation results, downscaled prototypes of following topologies are developed in the laboratory and experimentation is carried out:

**Topology-1:** 5-Level Inverter for open-end IMD

**Topology-2:** 9-Level Inverter for open-end IMD

**Topology-3:** Hybrid 9-Level Inverter for open-end IMD

The system hardware of these prototypes is developed in three stages:

- Implementation of power circuit
- Implementation of control circuit
- Measurement of system parameters

The power circuit of IMD consists of rectifier system, intermediate DC circuit system and inverter system. The DC-link voltages are obtained through uncontrolled diode bridge (KBPC3510) and to make it ripple free suitable ratings of DC link capacitors are chosen. The inverter circuits of all three topologies are developed using IGBTs (IRG4PH40KD).

The control algorithm to generate gate pulses for IGBTs is developed in MATLAB/Simulink environment. The RT-Lab is used as a real time HIL (hardware in loop) controller to implement control algorithm in real time. The RT-Lab compiler converts the MATLAB/Simulink program into a code compatible to Spartan-3 FPGA (field programmable gate array) board. The FPGA board generates the control signals for the IGBTs in real time which are taken out from digital output port of the RT-Lab. The feedback signals required to generate gate pulses are taken into RT-Lab by using analog input port.

The measurement of various system parameters and their conditioning is required to generate the pulses for switching devices at desired instants. To measure various parameters like voltage, current measuring circuits are developed in the laboratory using voltage and current sensors.

## 7.2 Hardware Implementation

The development of different hardware components as required for the operation of the hardware prototypes are discussed in this section.

### 7.2.1 Power Circuit Implementation

The general block diagram of power circuit of above-mentioned topologies is shown in Fig. 7.1. It consists of isolation transformer, rectifier, inverter-A and inverter-B. The double wound isolation transformer of 1kVA rating having three windings of 230V/115V/115V, 50Hz is used to supply AC power to the rectifiers. Isolated DC sources are developed using single phase uncontrolled rectifiers diode bridge (KBPC3510) rectifier. A 2200μF capacitor is connected across the output terminal of rectifier to make the DC voltage ripple free. Inverter-A in case of topology-1 (5-level inverter) and topology-2 (9-level inverter) is a cascade three-phase 3-level inverter as shown in Fig. 7.2(a), whereas in case of topology-3 (Hybrid 9-level inverter) it is three-phase 5-level hybrid inverter whose one leg is shown in Fig. 7.3. Inverter-B for topology-1 and topology-3 is a conventional two-level inverter whereas for topology-2 it is the same as 3-level inverter-A used in this topology. All these inverters are fabricated using IGBTs (International Rectifier IRG4PH50KD). Excessive transient voltages can occur, if the leakage inductance in the power circuit and snubber is not minimized. With conventional bus, longer connections of power circuit can cause more parasitic inductance making snubber design more difficult. In order to obtain low bus inductance in the power circuit their layout arrangement is optimized, thick aluminum heat sinks are designed to ensure proper heat dissipation and snubber circuit is directly mounted on the IGBT terminals.

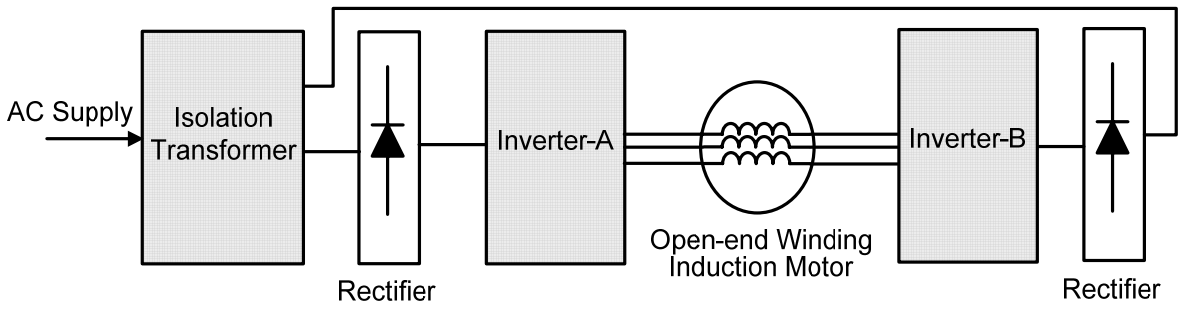



Fig. 7.1: General block diagram of power circuit

The snubber circuit comprises of a parallel combination of a resistor and a capacitor connected across a Metal-Oxide Varistor (MOV). The values of resistance and oil Impregnated capacitor of snubber circuit are selected as 50E±10%, 6W and KT-22 (1000V DC) respectively. The MOV selected for snubber is GE14 V320.

#### 7.2.1.1 Topology-1: 5-Level Inverter Scheme

The power circuit of 5-level inverter shown in sub section 3.2.1 is implemented in the laboratory using IGBTs. The circuit configuration of Inverter-A and Inverter-B are shown in Fig. 7.2(a) and Fig. 7.2(b) respectively. In this configuration two numbers of isolation transformers and three single phase rectifier bridges are required to develop three isolated DC sources.

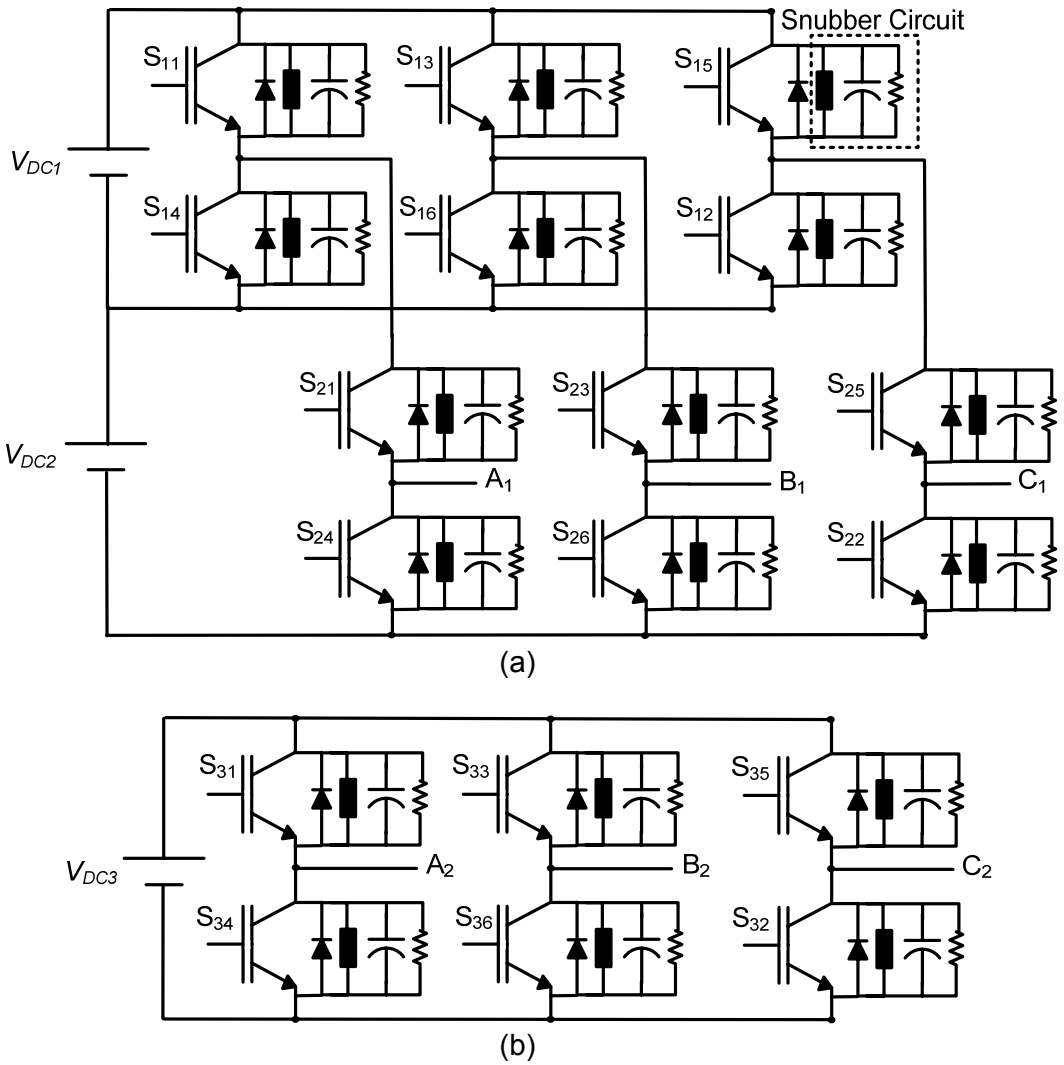



Fig. 7.2: (a) Power circuit of 3-Level inverter-A; (b) Power circuit of two-level inverter-B

### 7.2.1.2 Topology-2: 9-Level Inverter Scheme

The 9-level inverter scheme shown in sub section 4.2.1 is developed in the laboratory for experimentation using two numbers of 3-level inverter. The power circuit of 3-level inverter-A and inverter-B are same as shown in Fig. 7.2 (a); the difference is only in their DC link voltages. This topology requires four isolated DC sources so two numbers of isolation transformers and four rectifier bridges are used.

### 7.2.1.3 Topology-3: Hybrid 9-Level Inverter Scheme

The hybrid 9-level inverter topology proposed in sub section 5.2.1 is developed in the laboratory for hardware validation. A single leg of 5-level Inverter-A is shown in Fig. 7.3, the other side inverter-B is same as the two-level inverter used in topology-1 with DC link voltage of $V_{DC}/2$. This topology requires only one isolation transformer and two single phase rectifier bridges to develop two isolated DC link. As per design the value of capacitors $C_{A1}$ and $C_{A2}$ is selected as 2200μF.

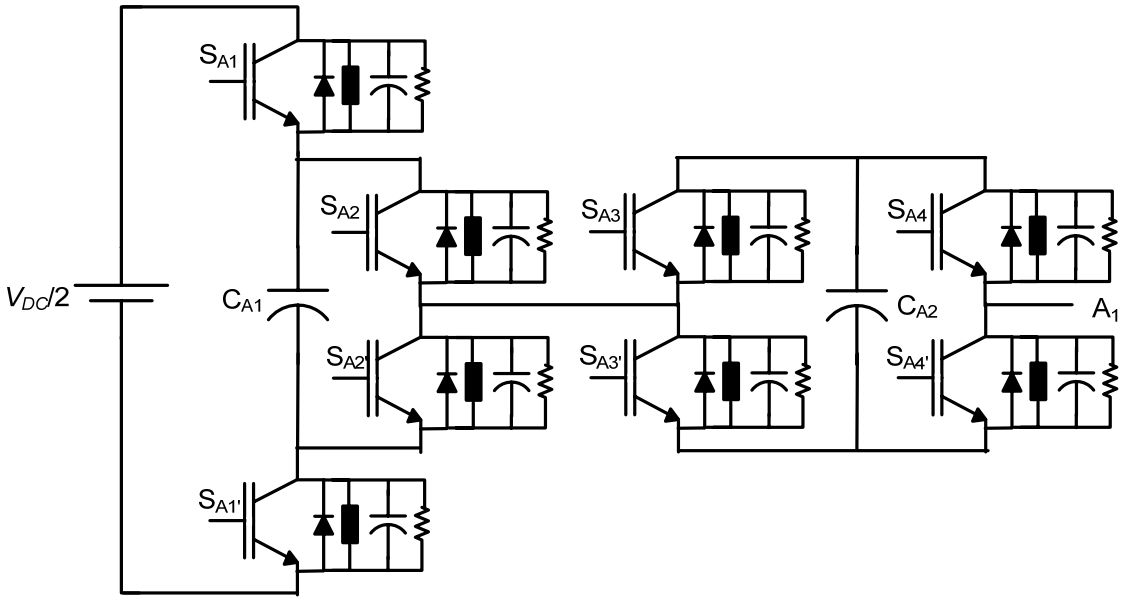



Fig. 7.3: Power circuit of single leg of hybrid 5-level inverter-A

### 7.2.2 Control Circuit Implementation

The block diagram of developed prototype of open-end winding induction motor drive is shown in Fig. 7.4. The gate pulses for IGBTs of inverter-A and inverter-B are generated by Opal-RT real time simulator using Spartan-3 FPGA board. In the block diagram only six pulses are shown for each inverter, but in actual the number of pulses depend upon the configuration of inverters. The control algorithm is developed using MATLAB /Simulink software and RT-Events block set of RT-Lab. The RT- Lab Meta controller compile the developed algorithm and generate optimized C-code for RT-lab real time digital simulator to generate gate pulses for IGBTs in real time simulation mode. The control pulses are available

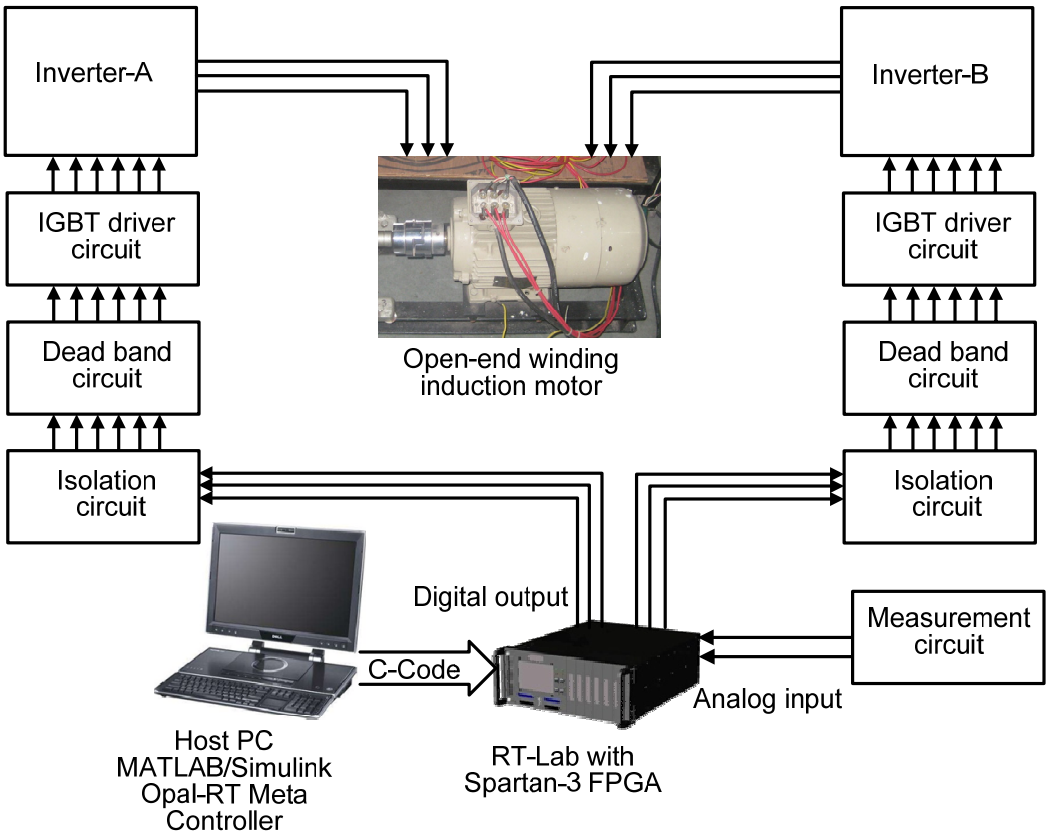



Fig. 7.4: Block diagram of open-end winding induction motor drive

at digital output card of RT-Lab simulator. These pulses are interfaced with the IGBTs driver circuits through isolation and dead-band circuits. This ensures the necessary isolation of the RT-Lab controller hardware from the power circuit, which is required for its protection. Fig. 7.4 shows the schematic diagram of interfacing firing pulses from RT-Lab controller to IGBTs of inverters. It can be observed that the isolation circuit, dead band circuit and IGBT driver circuit is required for interfacing the inverters with RT-Lab digital output card.

#### 7.2.2.1 Isolation Circuit

An isolation circuit is used to provide optical isolation between RT-Lab digital output card and power circuit of inverter. Fig. 7.5 shows the isolation circuit for four IGBTs. A non-inverting hex buffer HCF4050BE is used to prevent loading of RT-Lab digital output card. Optical isolation is achieved using Toshiba make opto-coupler 6N137 chip.

#### 7.2.2.2 Dead-Band Circuit

The IGBTs of same leg operate in complementary and to avoid short-circuit of IGBTs in the same leg due to simultaneous conduction a dead-band circuit is used. The time delay (of about 1 μs) between gate pulses of IGBTs of same leg is introduced by R-C circuit and logic

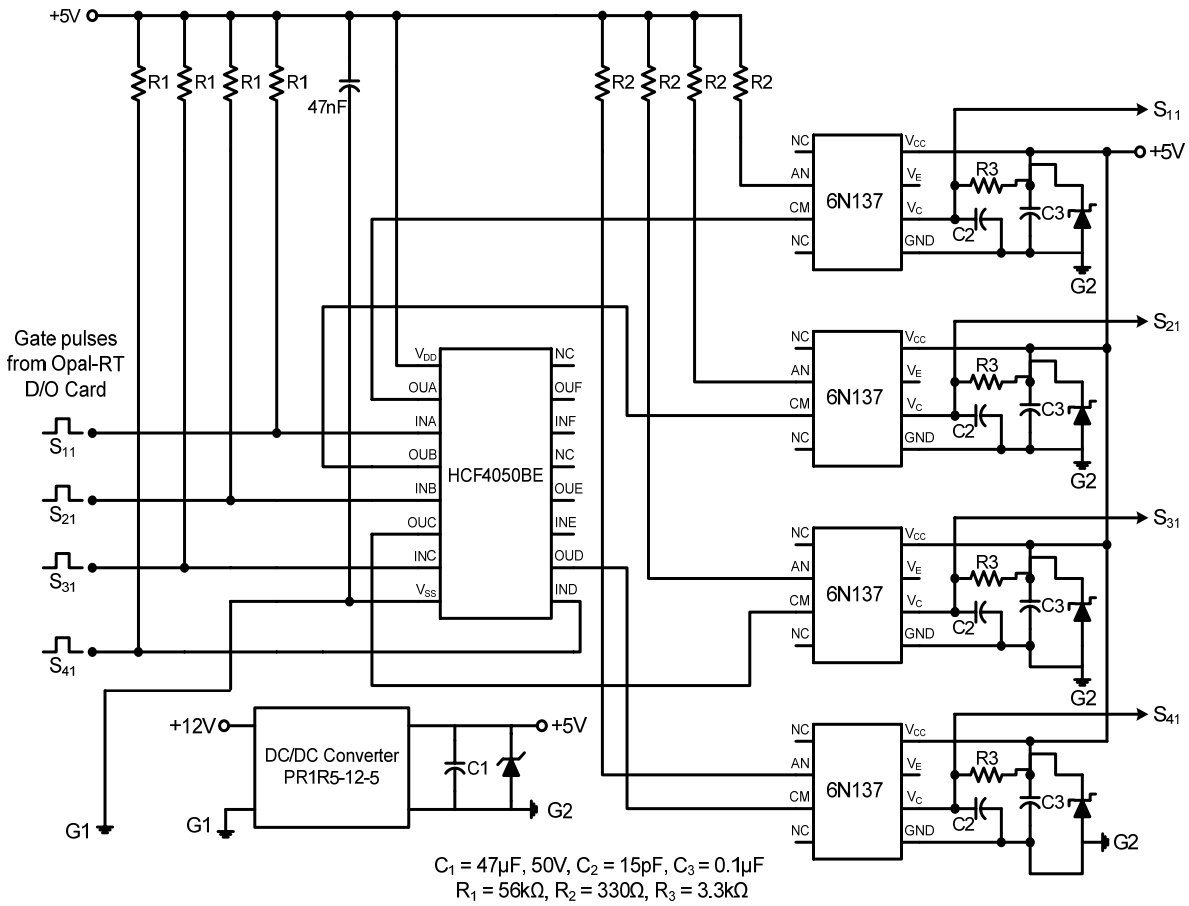
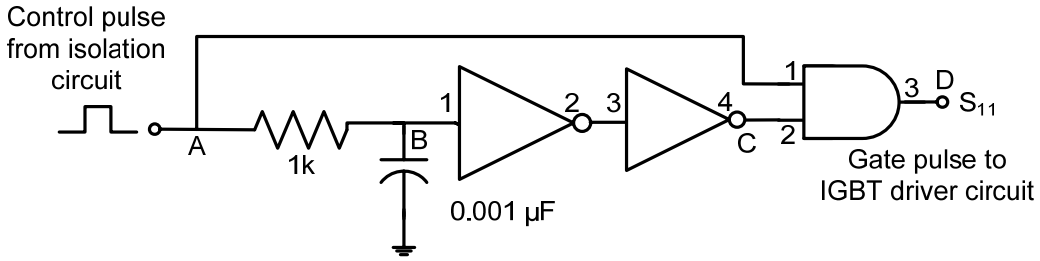
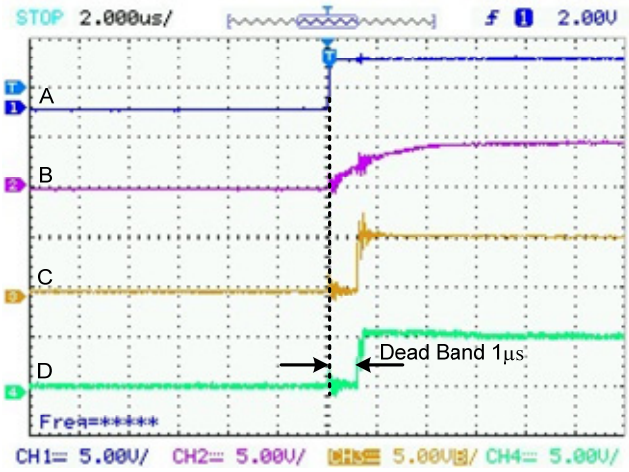



Fig. 7.5: Isolation circuit for four IGBTs




(a)




(b)

Fig. 7.6: Dead band circuit (a) Circuit diagram; (b) Waveforms at different points

gates as shown in Fig. 7.6. The output of the isolation circuit is passed through dead band circuit before given to IGBT.

#### 7.2.2.3 IGBT Driver Circuit

The IGBT driver circuit is used to amplify the amplitude of gate pulse and provide isolation between power circuit and control circuit. The driver circuit has inbuilt features like fault protection and protection against the under-voltage lockout. HCPL-316J chip from Agilent Technologies is used as an IGBT driver chip. It can drive IGBTs up to 150 A at an applied voltage up to 1200 V. The circuit diagram of the IGBT driver circuit is shown in Fig. 7.7. During normal operation, $V_{out}$ signal (Pin no. 11) of the HCPL-316J is controlled by either by VLN+ (Pin no. 1) or VLN- (Pin no. 2), with the IGBT collector-to-emitter voltage being monitored at $D_{SAT}$ (Pin no. 14). The FAULT and RESET are active low signals hence during normal operation FAULT output and RESET input should be held high. When the voltage on the $D_{SAT}$ pin (Pin no. 14) exceeds 7V, while IGBT is on, $V_{OUT}$ (Pin no. 11) is slowly brought low in order to “softly” turn-off the IGBT and prevent large induced voltages. Also, an internal feedback channel is activated which brings FAULT output (Pin no. 6) low for the purpose of notifying the RT-Lab controller of the fault condition. The FAULT output remains low until

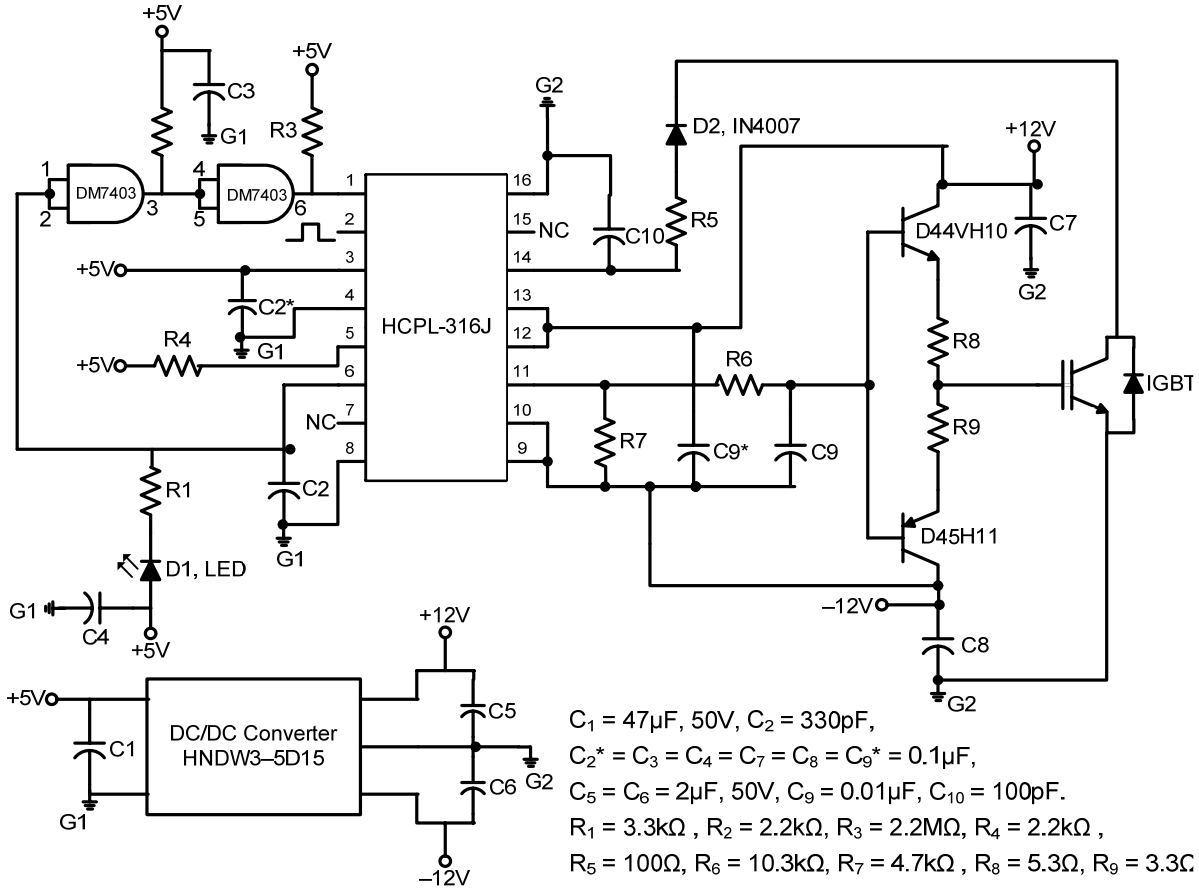



Fig. 7.7: IGBT driver circuit

RESET is brought low. An LED indication is provided in each driver circuit to indicate the occurrence of a fault, thus prompting a corrective action, either manually or through RT-Lab controller. The HCPL-316J Under Voltage Lockout (UVLO) feature is designed to prevent the application of insufficient gate voltage to IGBT by forcing the HCPL-316J output low during power-up. IGBTs typically require gate voltages of 15V to achieve their rated $V_{CE(ON)}$ voltage. At gate voltages below 12V typically, their on-voltage increases dramatically, especially at higher currents. At very low gate voltages (below 10V), the IGBT may operate in the linear region and quickly overheat. The UVLO feature causes the output to be clamped whenever insufficient operating supply voltage is applied.

### 7.2.3 Measurement of System Parameter

For accurate and reliable operation of the system, measurement of various system parameters and their conditioning is required. The measurement system must fulfil the following requirements:

- Galvanic isolation between power and control circuit
- High accuracy with ease of installation and operation
- Linearity and fast response

With the availability of Hall-effect current sensors and isolation amplifiers, these requirements are fulfilled to a large extent. In order to implement the control algorithm and monitoring purpose inverters pole voltages, phase voltages, capacitors voltages (Topology-3) and phase currents are sensed.

#### 7.2.3.1 Measurement of Voltage

The voltages are normally sensed using isolation amplifiers and among them, AD202 is a general purpose, two-port, transformer-coupled isolation amplifier that can be used for measuring both ac and dc voltages. It offers bipolar ±5V output range, an adjustable gain range from 1 V/V to 100 V/V, ±0.025% maximum nonlinearity, 130dB of CMR and lower power consumption. The other main features of the AD202 isolation amplifier are:

- Small physical size
- High accuracy
- Low power consumption
- Wide bandwidth
- Excellent common-mode performance

This voltage sensor can sense voltages in the range of ±1 kV (peak) and it requires a nominal supply voltage range of ±12V to ±15V. Fig. 7.8 shows the circuit diagram for the voltage sensing scheme, which uses AD202 isolation amplifier. The voltage (ac or dc) to be sensed is applied between the terminals 1 and 2 (across a voltage divider comprising of 100 kΩ and 1 kΩ) and the voltage input to the sensor is available at the pins 1 and 2 of AD202

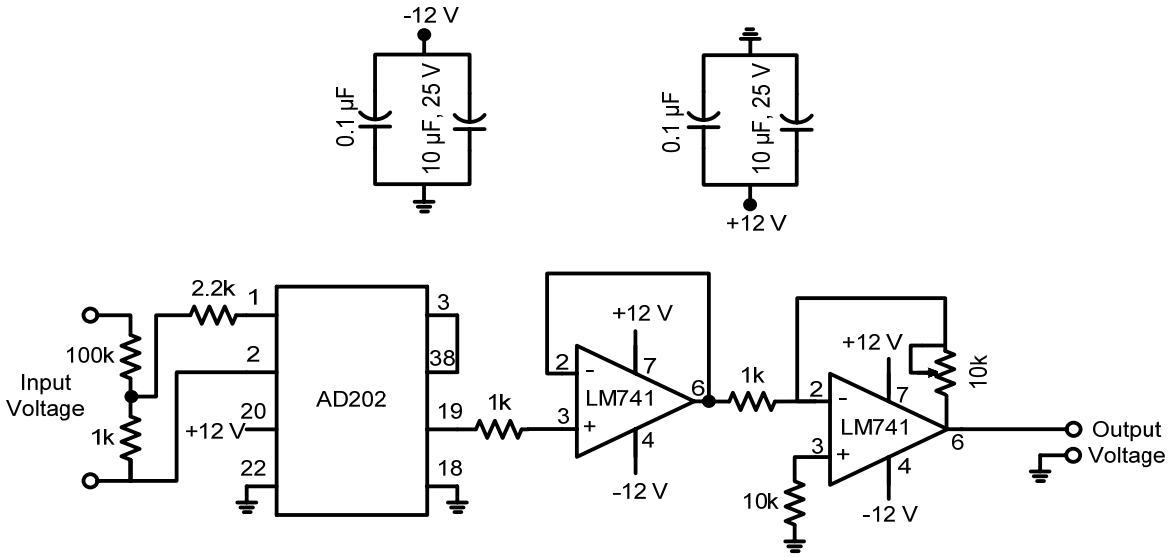



Fig. 7.8: AC/DC voltage sensing circuit

via a resistance of 2.2 kΩ. The isolated sensed voltage is available at the output terminal 19 of AD202. The output of voltage sensor is scaled properly to meet the requirement of the control circuit and is fed to the RT-Lab analog input card for further processing.

### 7.2.3.2 Measurement of Current

The motor phase currents are sensed using the PCB-mounted Hall-effect current sensors (TELCON HTP25). The HTP25 is a closed loop Hall-effect current transformer suitable for measuring currents up to 25A. This device provides an output current into an external load resistance. These current sensors provide the galvanic isolation between the high voltage power circuit and the low voltage control circuit and require a nominal supply voltage of the range ±12V to ±15V. It has a transformation ratio of 1000:1 and thus its output is scaled properly to obtain the desired value of measurement. The circuit diagram of the current sensing scheme is shown in Fig. 7.9.

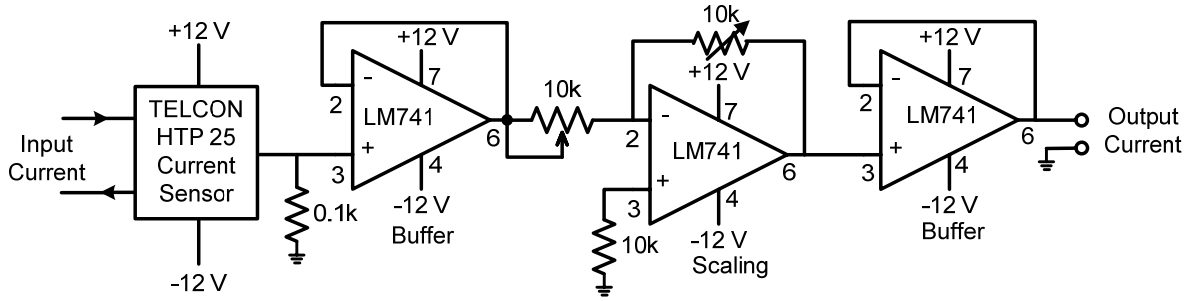



Fig. 7.9: Hall-effect sensor based AC current sensing circuit

### 7.2.4 System Software

Historically, control software was developed using assembly language. In recent years, industry began to adopt MATLAB/Simulink and Real-Time Workshop (RTW) platform based method, which provides a more systematic way to develop control software. RT-Lab, from Opal-RT Technologies, is used as real-time hardware-in-loop controller to generate gate pulses for IGBTs in real-time. It is a complete real-time control system based on Intel™ 2.6 GHz processor running at RedHat Linux operating system. The offline control algorithm developed in MATLAB/Simulink platform converted and transported to the Spartan-3 FPGA board of RT-Lab using Opal-RT's compiler RT-Lab version 10.6. This saves the time and effort twice as there is no need to manually convert the Simulink model into another language such as C and one need not to be concerned about a real-time program frame and I/O function calls, or about implementing and downloading the code onto the RT-Lab. The process is notably very efficient when applied to input/output because RT-Lab provides a set of simulink block that automatically configure common I/O functions like analog inputs (feedback signals) and time-stamped digital outputs, with a resolution of 10 nanoseconds. The generated digital output signals are taken out from digital output card and fed to various IGBTs driver circuits via isolation and dead-band circuits. Fig. 7.10 shows the schematic diagram of RT-Lab board interfaced with the host computer and the real-world plant (Inverter-A and B). The sensed signals from the real-world are fed to the analog input card to use these signals for controlling or monitoring purpose.

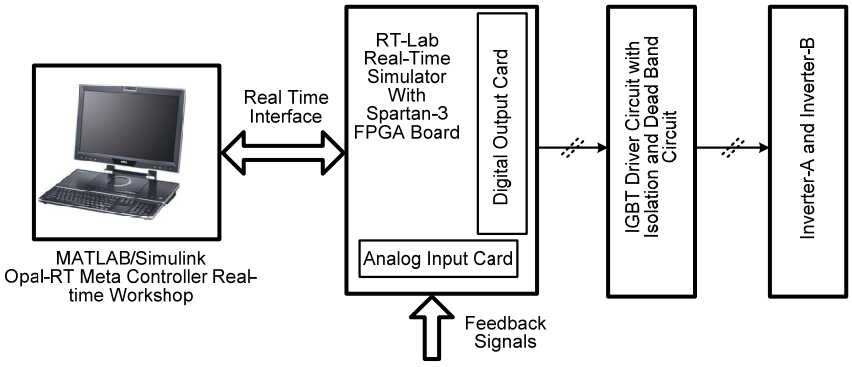



Fig. 7.10: Interfacing of RT-Lab with MATLAB and real-world plant (Inverter-A and B)

## 7.3 Experimental Validation

The prototype models of following MLI topologies are developed in the laboratory and experimentation is carried out:

**Topology-1:** 5-Level Inverter for open-end IMD

**Topology-2:** 9-Level Inverter for open-end IMD

**Topology-3:** Hybrid 9-Level Inverter for open-end IMD

In simulation studies of these topologies the total DC link voltage ($V_{DC}$) of 600V was selected, but due to the practical constraints total DC-link voltage of 200V is used. An open-end winding induction motor of 1.5kW, 415V, 50Hz, 4pole is used as load and operated at no-load with constant *V/f* control. As the experimentation is carried out at reduced voltage, for validating the experimental results, the simulation study at reduced voltage is also carried out. The complete system hardware consists of power circuit and control circuit and its schematic diagram is shown in Fig. 7.4. Experimental results for each prototype are obtained on Agilent DSO1014A oscilloscope and presented in the next sub-sections.

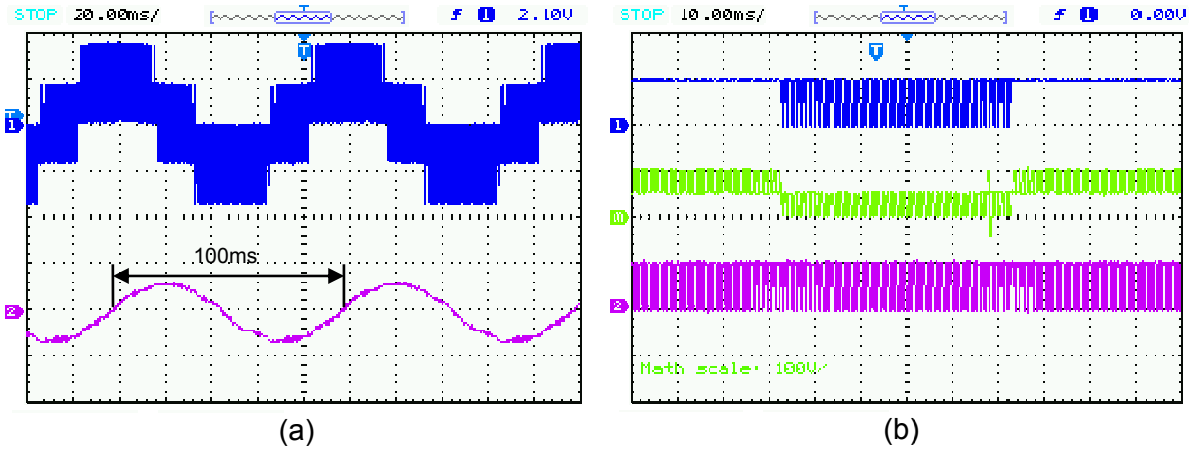
### 7.3.1 Experimental Validation of 5-level Inverter

The performance of 5-level inverter scheme discussed in Chapter-3 is evaluated experimentally for 1.5kW, 415V, 50Hz, 4pole open-end winding induction motor operated in constant *V/f* mode under no-load condition covering the entire range of linear modulation. The control algorithm describe in section-3.3 is developed on RT-Lab real-time simulator and firing pulses for IGBTs are generated using Spartan-3 FPGA board. The three isolated DC link are implemented using single phase rectifier bridges and a 2200μF capacitor is connected at the output of rectifier. The switching frequency ($f_c$) is kept constant at 1kHz and DC link voltage is taken as 200V for experimentation. The motor used for experimentation having the same parameters as the simulated motor model (Appendix-A). The motor phase-A voltage ($V_{A2A3}$), phase-A current ($i_{A2A3}$), their harmonic spectrums, inverters pole-A voltages ($V_{A2O}$, $V_{A3O'}$) and difference of inverters pole-A voltages ($V_{A2O}$ - $V_{A3O'}$) are considered as evaluation parameters. To cover the entire range of linear modulation four values of modulation indices ($m$) 0.2, 0.4, 0.6 and 0.8 correspond to frequencies ($f^*_m$) of 10, 20, 30, and 40Hz respectively are selected. The performance of 5-level inverter scheme is experimentally evaluated under steady-state as well as transient-state conditions and results are presented. In order to validate the experimental results, simulation results under same operating conditions are also given.

The experimentally obtained motor phase-A voltage ($V_{A2A3}$), current ($i_{A2A3}$) and pole voltages ($V_{A2O}$, $V_{A3O'}$) waveforms of individual inverters at modulation index $m$=0.2 are shown in Fig. 7.11(a) and Fig. 7.11(b) respectively. At this modulation index motor operates at fundamental frequency ($f^*_m$) of 10Hz. The simulated waveforms of motor phase-A voltage ($V_{A2A3}$), current ($i_{A2A3}$) and pole voltages ($V_{A2O}$, $V_{A3O'}$) of individual inverters at same operating conditions are presented in Fig. 7.13(a) and Fig. 7.13(b) respectively. It may be seen that the experimental results (Fig. 7.11) are in agreement with the simulation results (Fig. 7.13). In both cases (Experimental and Simulation) phase-A voltage ($V_{A2A3}$) and current ($i_{A2A3}$) waveforms are equivalent to the conventional two-level inverter voltage and current waveforms. The normalized harmonic spectrum of phase-A voltage $V_{A2A3}$ (Fig. 7.11a), and current $i_{A2A3}$ (Fig. 7.11b) obtained using FFT, are presented in Fig. 7.12(a) and Fig. 7.12(b)

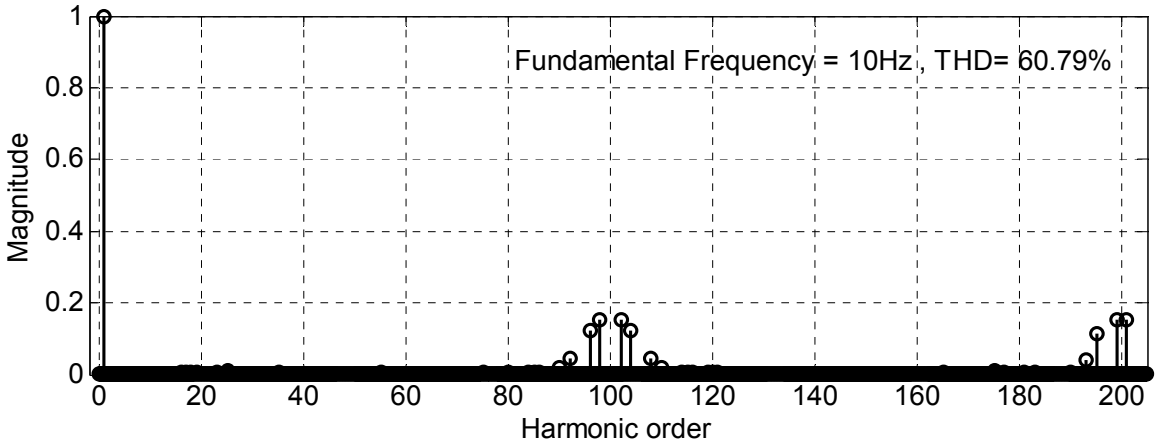
respectively. It can be observed from Fig. 7.12 that the dominant harmonic components of phase voltage and current occur at the side band of multiple of 100 ($f_c/f^*_m$ =2*1000/10) i.e. at $100^{th}$, $200^{th}$ order. It can be observed from pole voltages waveform that 3-level inverter-A operates in two-level mode (0 and 100V) only for half of the duration of fundamental cycle and for remaining half cycle it is clamped at voltage level of 100V ($V_{DC}$/2) so effective switching frequency is half of the actual switching frequency.

Another set of experimental and simulation results when modulation index $m$ =0.4 and fundamental frequency $f^*_m$=20Hz are shown in Fig. 7.14 - Fig. 7.16. The experimental results for motor phase-A voltage ($V_{A2A3}$) and current ($i_{A2A3}$) are presented in Fig. 7.14(a) and simulation results are shown in Fig. 7.16(a). The experimentally obtained pole voltages ($V_{A2O}$, $V_{A3O'}$) and difference of inverters pole-A voltages ($V_{A2O}$ - $V_{A3O'}$) are depicted in Fig. 7.14(b). The simulated waveforms of pole voltages and their difference are shown in Fig. 7.16(b). The pole voltages waveforms are similar to the pole voltages waveforms obtained in previous case. The normalized harmonic spectrum of phase-A voltage (Fig. 7.14a) is shown in Fig. 7.15(a) and THD is found 31.87% with dominant harmonic component at side band of $100^{th}$ ($2f_c/f^*_m$ = 2*1000/20) order. Normalized harmonic spectrum of phase-A current is presented in Fig. 7.15(b) and THD is found 3.57%. It can be noticed that the experimental results obtained in this case also similar to simulation results. The experimental harmonic spectra are obtained by saving the actual motor phase voltage and current in to the workspace of MATLAB using analog input card of RT-Lab and then analyzed using FFT in MATLAB.

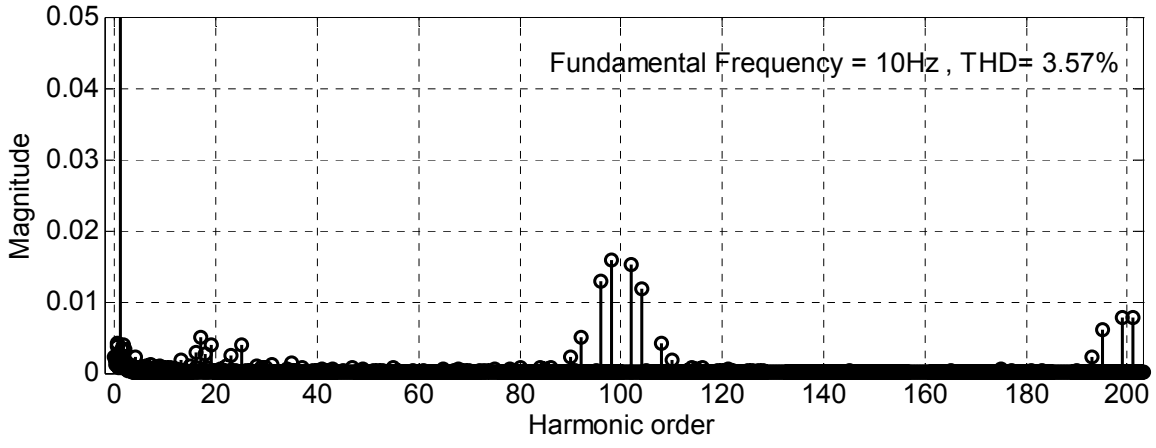



(a) (b)

Fig. 7.11: (a) Motor phase-A, voltage $V_{A2A3}$ (upper trace Y-axis: 20V/div) and current $i_{A2A3}$ (lower trace Y-axis: 1A/div) of 5-level inverter fed open-end IM drive at no load
(b) Top trace Y-axis: 100V/div; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace Y-axis: 100V/div; Difference of 3-level inverter-A and two-level inverter-B pole voltages ($V_{A2O}$ - $V_{A3O'}$), Bottom trace Y-axis: 50V/div; Two-level inverter-B pole voltage ($V_{A3O'}$)
(Experimental result: $m$=0.2; $f^*_m$ =10Hz)

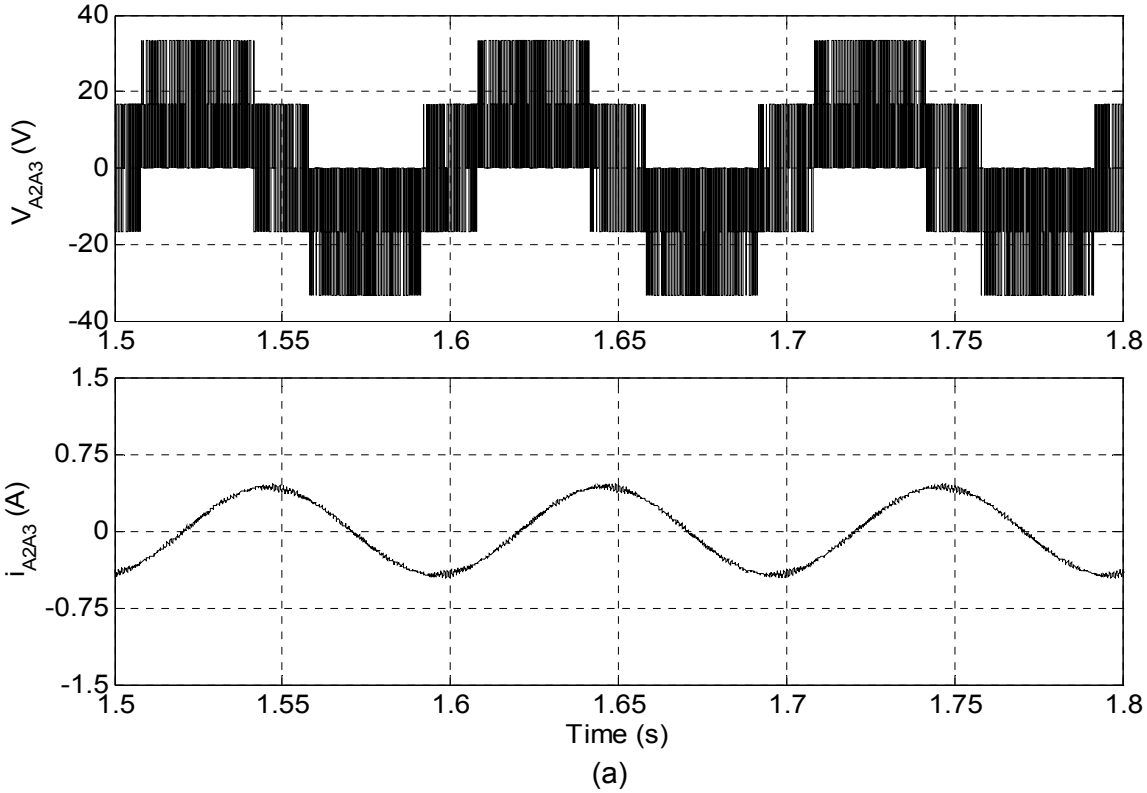



(a)

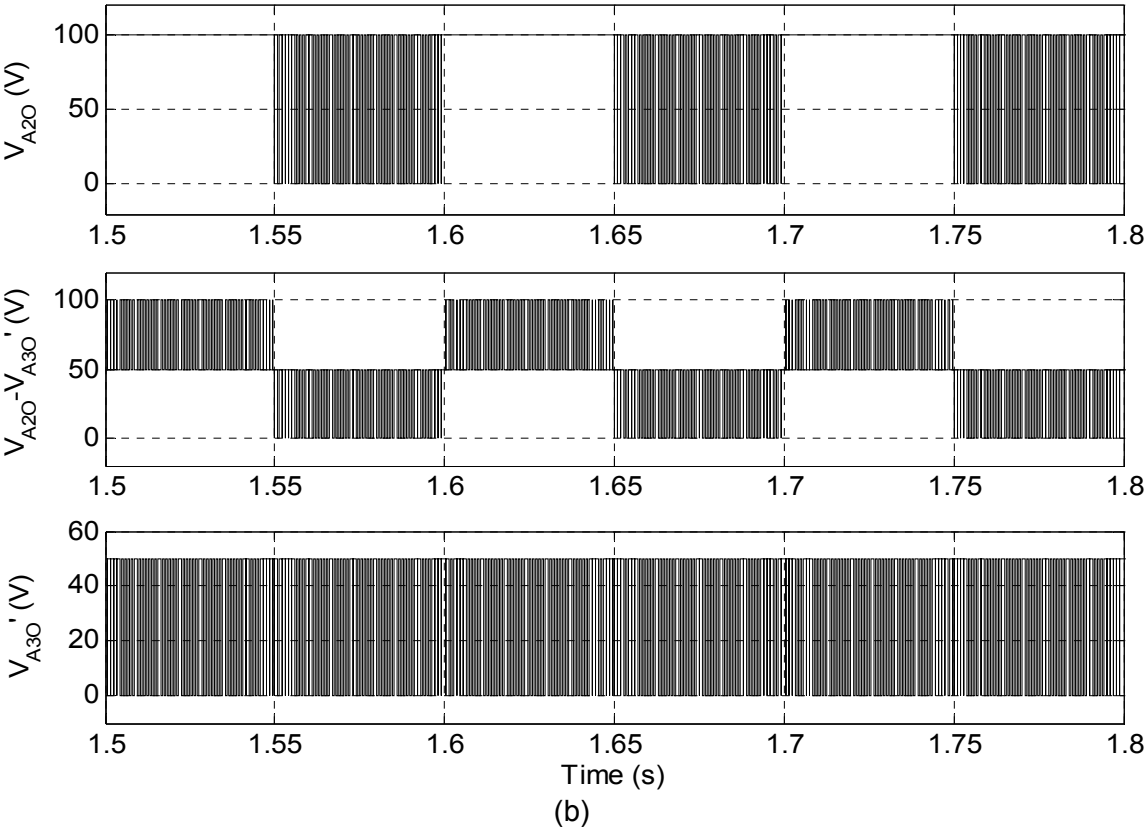



(b)

Fig. 7.12: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A2A3}$ (b) Current $i_{A2A3}$
(Experimental result: $m$=0.2; $f^*_m$ =10Hz)




(a)




(b)

Fig. 7.13: (a) Motor phase-A, voltage $V_{A2A3}$ (upper trace) and current $i_{A2A3}$ (lower trace) of 5-level inverter fed open-end IM drive at no load
(b) Top trace; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace; Difference of 3-level inverter-A and two-level inverter-B pole voltages ($V_{A2O}$ - $V_{A3O'}$), Bottom trace; Two-level inverter-B pole voltage ($V_{A3O'}$)
(Simulation result: $m$=0.2; $f^*_m$ =10Hz)

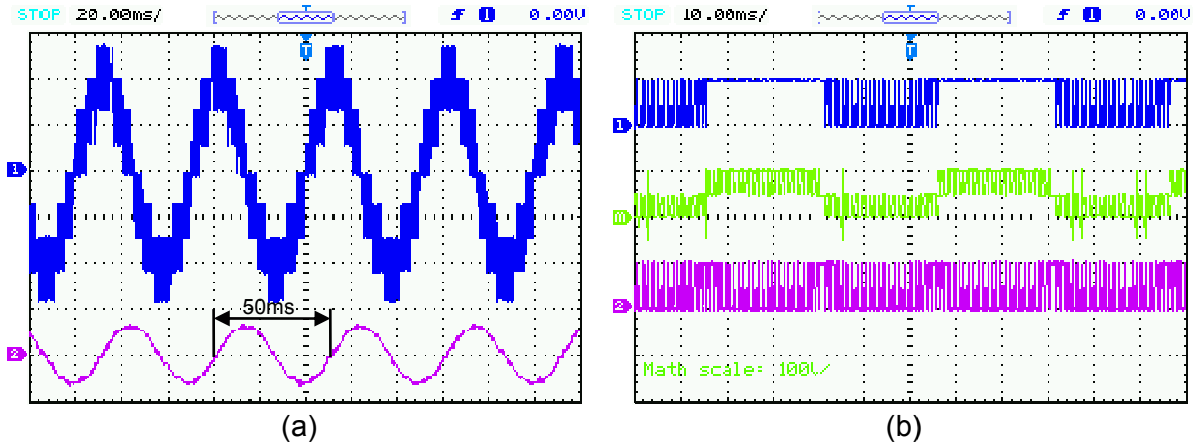



Fig. 7.14: (a) Motor phase-A, voltage $V_{A2A3}$ (upper trace Y-axis: 25V/div) and current $i_{A2A3}$ (lower trace Y-axis: 1A/div) of 5-level inverter fed open-end IM drive at no load
(b) Top trace Y-axis: 100V/div; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace Y-axis: 100V/div; Difference of 3-level inverter-A and two-level inverter-B pole voltages ($V_{A2O}$ - $V_{A3O'}$), Bottom trace Y-axis: 50V/div; Two-level inverter-B pole voltage ($V_{A3O'}$)
(Experimental result: $m$=0.4; $f^*_m$ =20Hz)

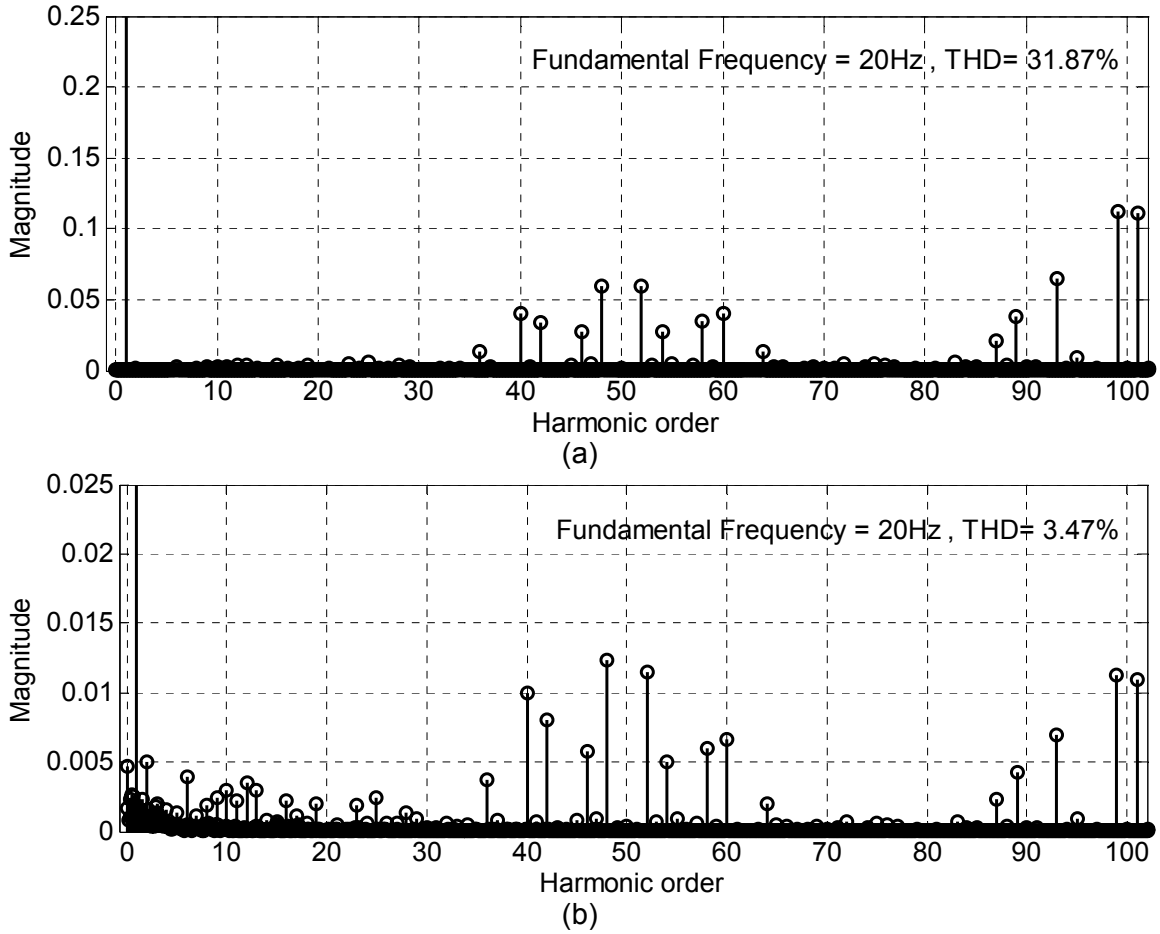
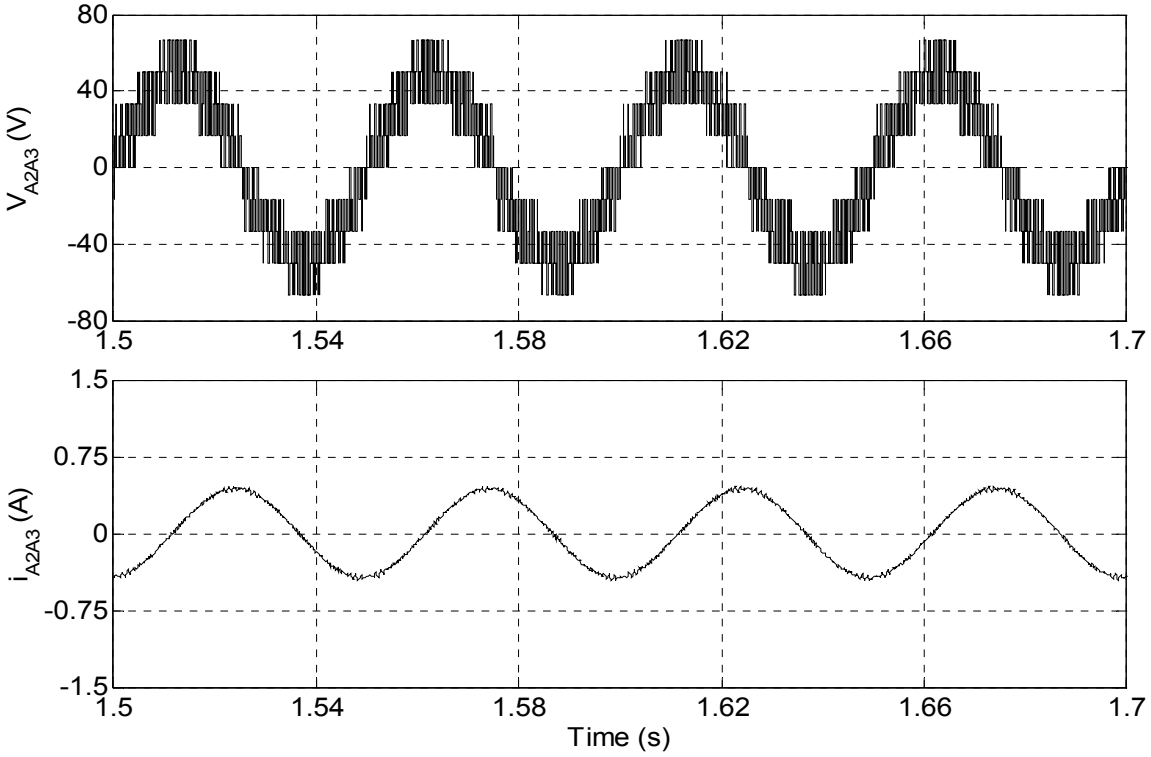
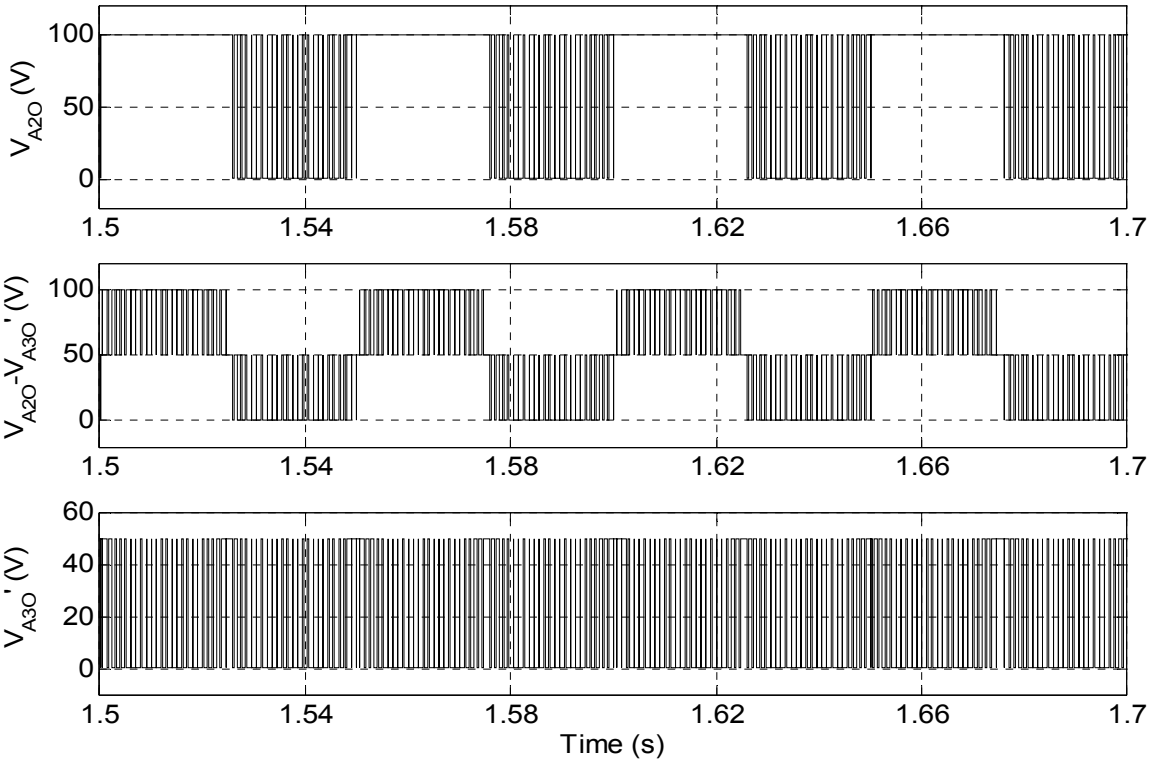



Fig. 7.15: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A2A3}$ (b) Current $i_{A2A3}$
(Experimental result: $m$=0.4; $f^*_m$ =20Hz)




(a)




(b)

Fig. 7.16: (a) Motor phase-A, voltage $V_{A2A3}$ (upper trace) and current $i_{A2A3}$ (lower trace) of 5-level inverter fed open-end IM drive at no load
(b) Top trace; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace; Difference of 3-level inverter-A and two-level inverter-B pole voltages ($V_{A2O}$ - $V_{A3O'}$), Bottom trace; Two-level inverter-B pole voltage ($V_{A3O'}$)
(Simulation result: $m$=0.4; $f^*_m$ =20Hz)

Fig. 7.17 through Fig. 7.19 present the experimental and simulation results obtained when motor is operated at modulation index $m$ =0.6 and fundamental frequency $f^*_m$=30Hz. Fig. 7.17(a) shows the experimental waveforms of phase-A voltage $V_{A2A3}$ (upper trace) and current $i_{A2A3}$ (lower trace). The simulated motor phase voltage and current is shown in Fig. 7.19(a). The experimentally obtained inverter-A and inverter-B pole voltages ($V_{A2O}$, $V_{A3O'}$), are presented in Fig. 7.17(b). The middle trace of Fig. 7.17(b) shows the difference of 3-level inverter-A and two-level inverter-B pole voltages ($V_{A2O}$ - $V_{A3O'}$). The simulated waveforms of $V_{A2O}$, $V_{A3O'}$ and their difference is shown in Fig. 7.19(b). It can be noted from pole voltages waveforms (Fig. 7.17b, Fig. 7.19b) that 3-level inverter-A operates in three level mode of operation and takes the values 0, 100 and 150 correspond to 0, $V_{DC}$/2 and 3$V_{DC}$/4 only for half of the duration of fundamental cycle and for remaining half cycle it is clamped at zero voltage so effectively it is operated in PWM mode only for half of the duration of fundamental cycle hence switching losses are reduced. The normalized harmonic spectrums of experimentally obtained phase-A voltage and current are shown in Fig. 7.18(a) and Fig. 7.18(b) respectively. It can be observed from harmonic spectrum of phase voltage that THD is reduced to 8.05% and dominant harmonic component occur at side band of 67$^{th}$ ($2f_c/f^*_m$ = 2*1000/30) order. It is depicted in harmonic spectrum (Fig. 7.18b) of phase current that the lower order harmonics are increased, but the THD is only 1.10%.

Similar experimental and simulation results correspond to the case when motor is operated at modulation index $m$ =0.8 with fundamental frequency $f^*_m$=40Hz are presented in Fig. 7.20 through Fig. 7.22. Motor phase-A voltage $V_{A2A3}$ (Fig. 7.20a; experimental, Fig. 7.22a simulated) become more refine and total harmonic distortion (Fig. 7.21a) is 7.11% of the fundamental. The distortion in motor phase current is increased due to presence of lower order 3$^{rd}$ and 5$^{th}$ harmonics (Fig. 7.21b) and THD is 5.71%. The pole voltages waveforms (Fig. 7.20b; experimental, Fig. 7.22b simulated) have the same level as in the previous case.

The proposed drive system is also investigated against transient state stability by sudden change its operation from two-level to 5-level operation and vice versa. Fig. 7.23(a) and Fig. 7.23(b) show the experimentally obtained phase-A voltage $V_{A2A3}$ and current $i_{A2A3}$ during sudden change in operation from two-level to 5-level and from 5-level to two-level respectively. The simulated waveforms during transient operation under same operating conditions are presented in Fig. 7.24. It can be observed from Fig. 7.23 and Fig. 7.24 that changeover from lower to higher or from higher to lower level of operation take place very smoothly and drive achieve its steady state within few cycles.

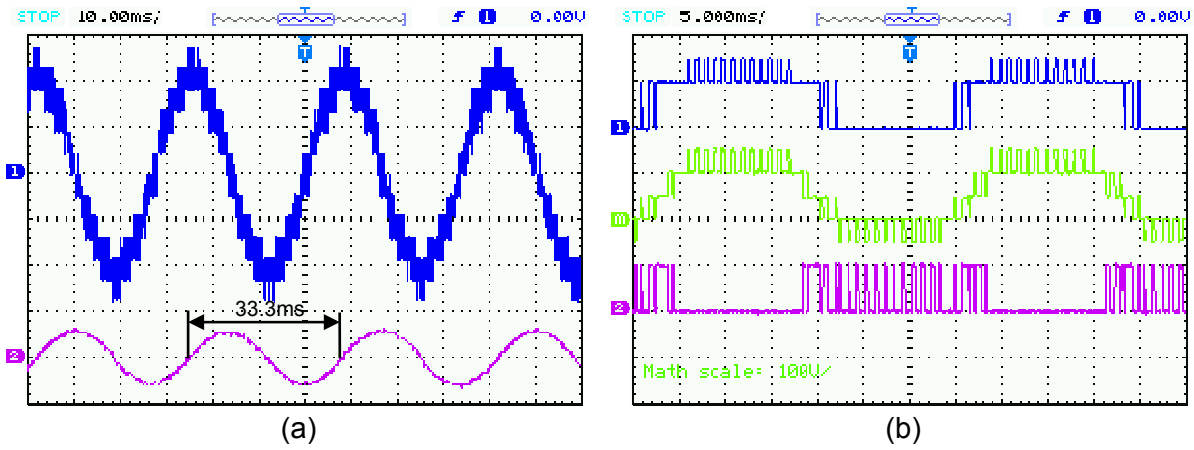



Fig. 7.17: (a) Motor phase-A, voltage $V_{A2A3}$ (upper trace Y-axis: 40V/div) and current $i_{A2A3}$ (lower trace Y-axis: 1A/div) of 5-level inverter fed open-end IM drive at no load
(b) Top trace Y-axis: 100V/div; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace Y-axis: 100V/div; Difference of 3-level inverter-A and two-level inverter-B pole voltages ($V_{A2O}$ - $V_{A3O'}$), Bottom trace Y-axis: 50V/div; Two-level inverter-B pole voltage ($V_{A3O'}$)
(Experimental result: $m$=0.6; $f^*_m$ =30Hz)

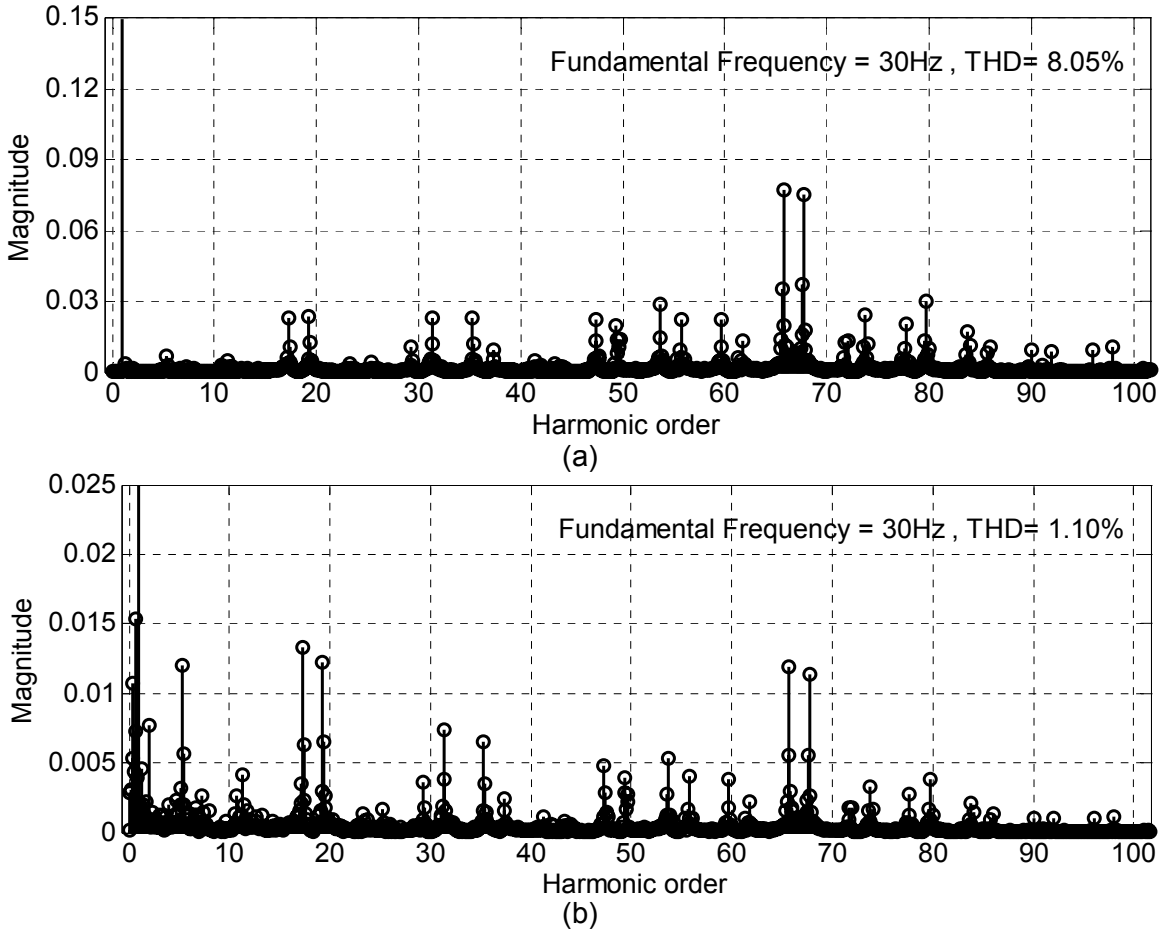
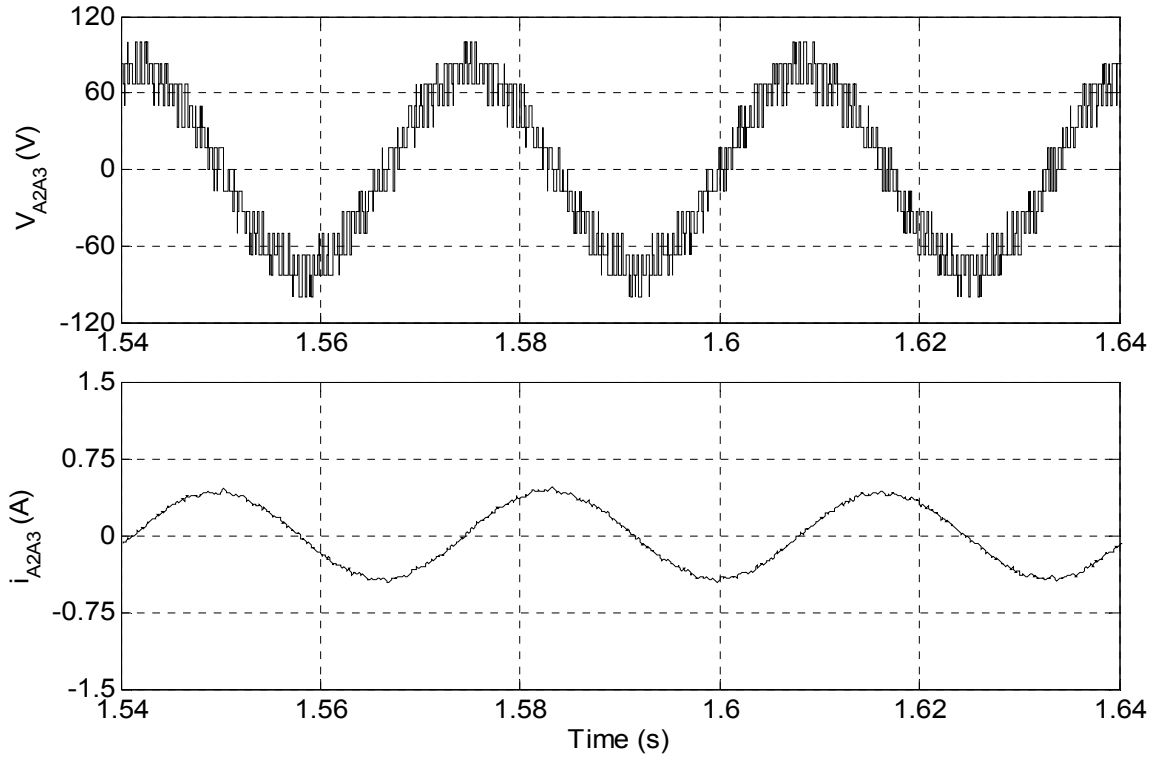
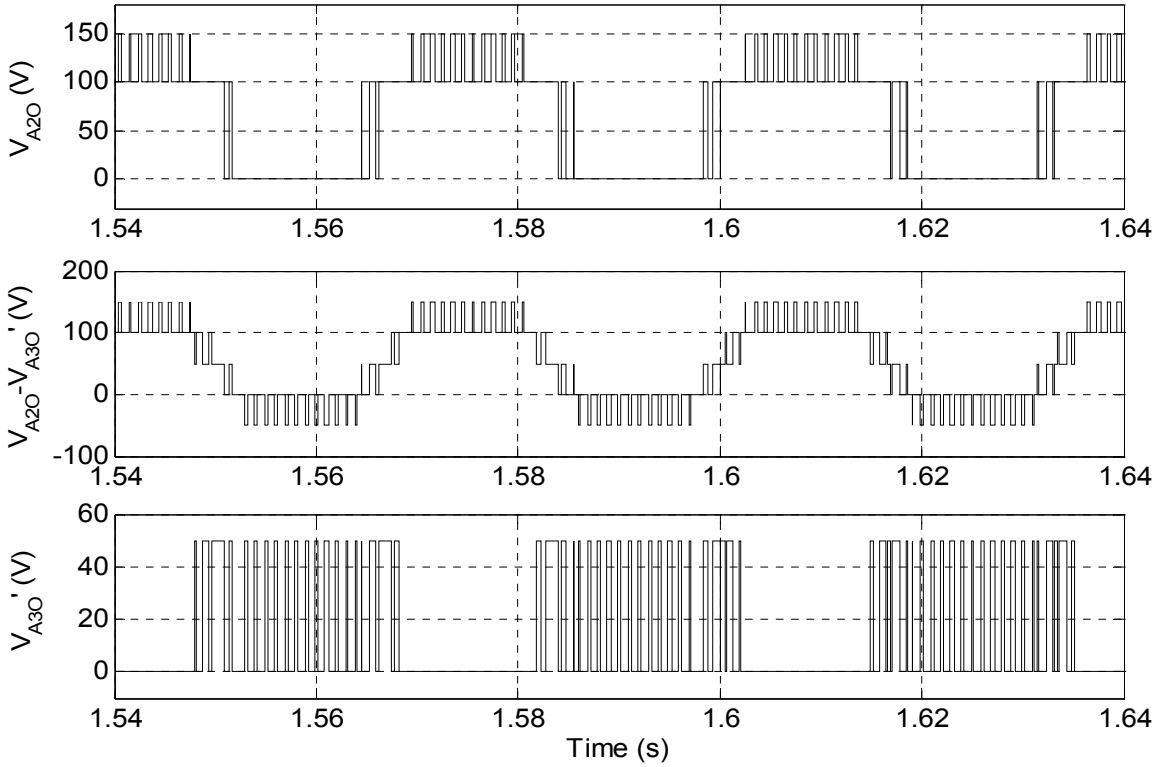



Fig. 7.18: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A2A3}$ (b) Current $i_{A2A3}$
(Experimental result: $m$=0.6; $f^*_m$ =30Hz)




(a)




(b)

Fig. 7.19: (a) Motor phase-A, voltage $V_{A2A3}$ (upper trace) and current $i_{A2A3}$ (lower trace) of 5-level inverter fed open-end IM drive at no load
(b) Top trace; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace; Difference of 3-level inverter-A and two-level inverter-B pole voltages ($V_{A2O}$ - $V_{A3O'}$), Bottom trace; Two-level inverter-B pole voltage ($V_{A3O'}$)
(Simulation result: $m$=0.6; $f^*_m$ =30Hz)

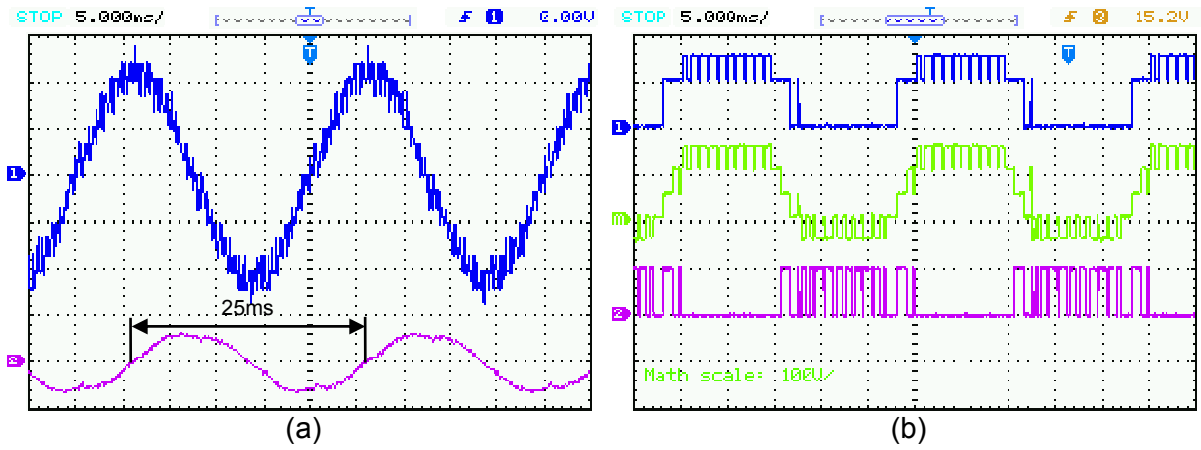



Fig. 7.20: (a) Motor phase-A, voltage $V_{A2A3}$ (upper trace Y-axis: 50V/div) and current $i_{A2A3}$ (lower trace Y-axis: 1A/div) of 5-level inverter fed open-end IM drive at no load
(b) Top trace Y-axis: 100V/div; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace Y-axis: 100V/div; Difference of 3-level inverter-A and two-level inverter-B pole voltages ($V_{A2O}$ - $V_{A3O'}$), Bottom trace Y-axis: 50V/div; Two-level inverter-B pole voltage ($V_{A3O'}$)
(Experimental result: $m$=0.8; $f^*_m$ =40Hz)

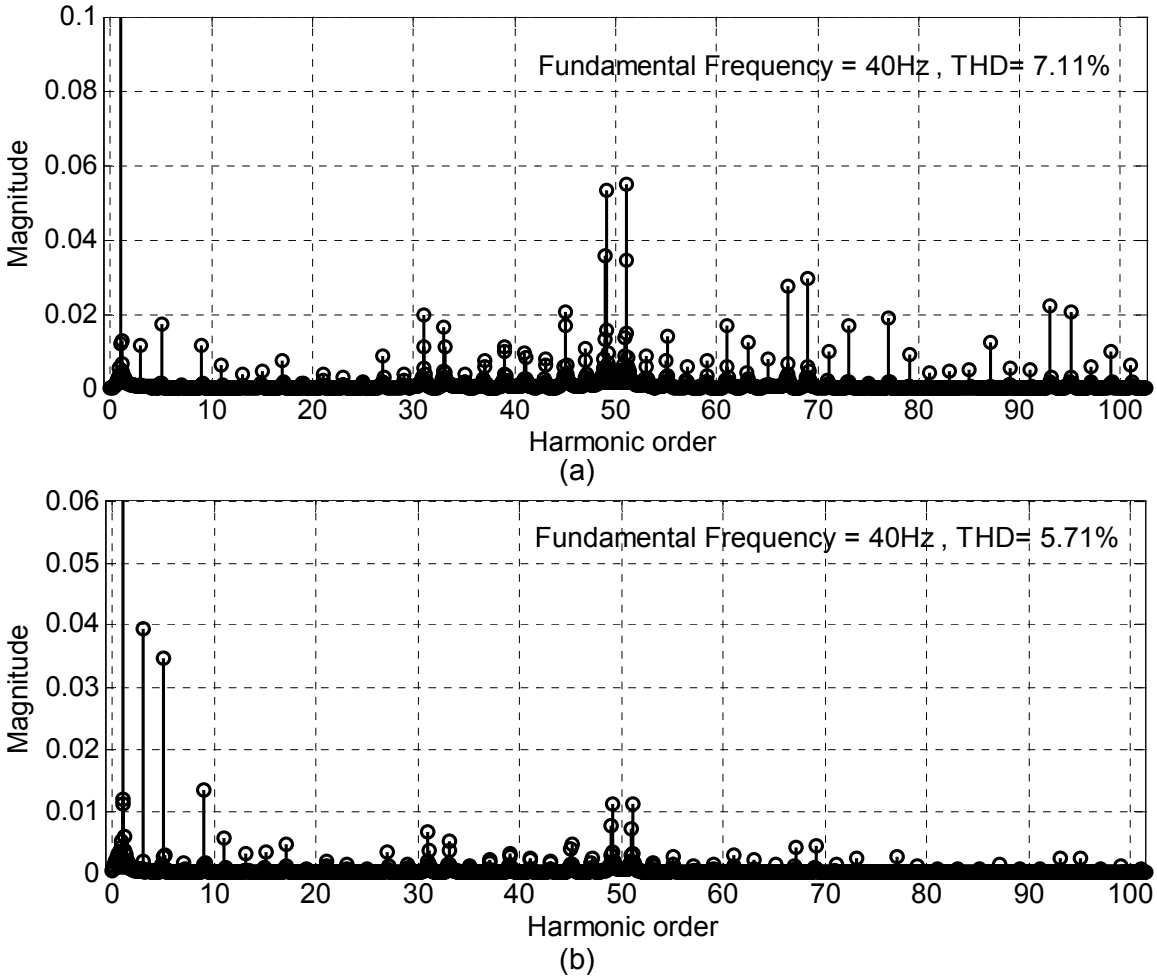
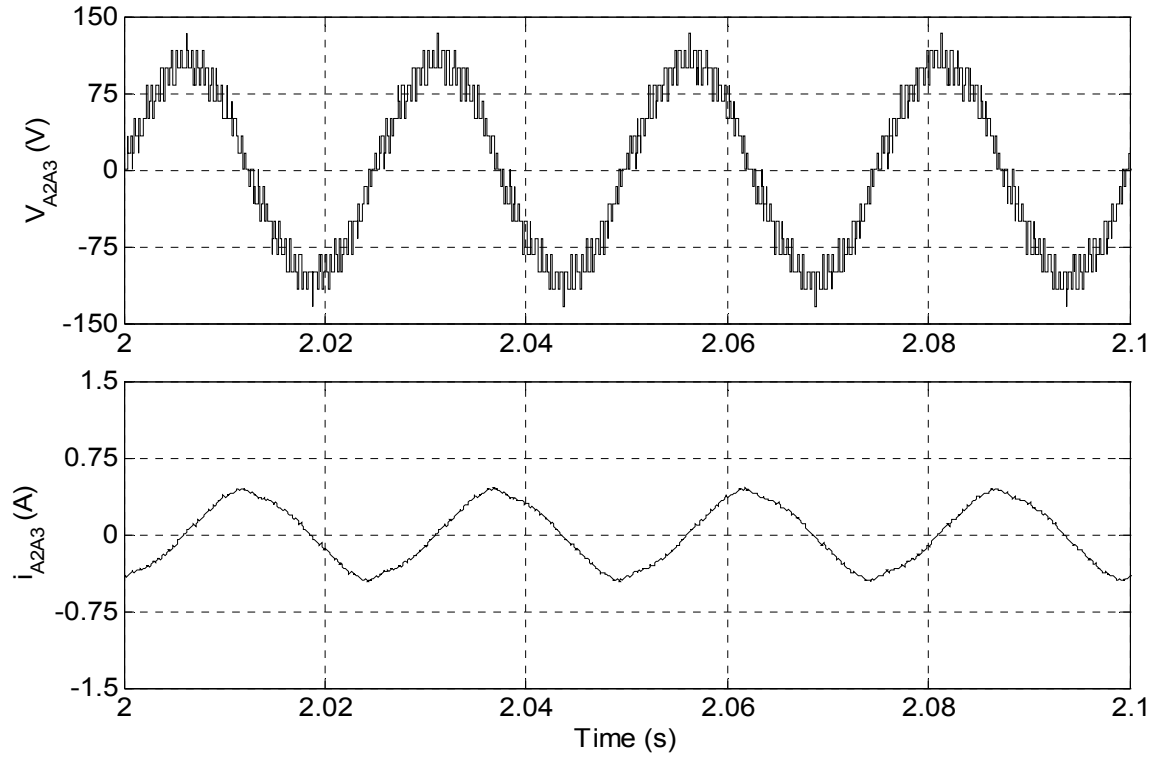
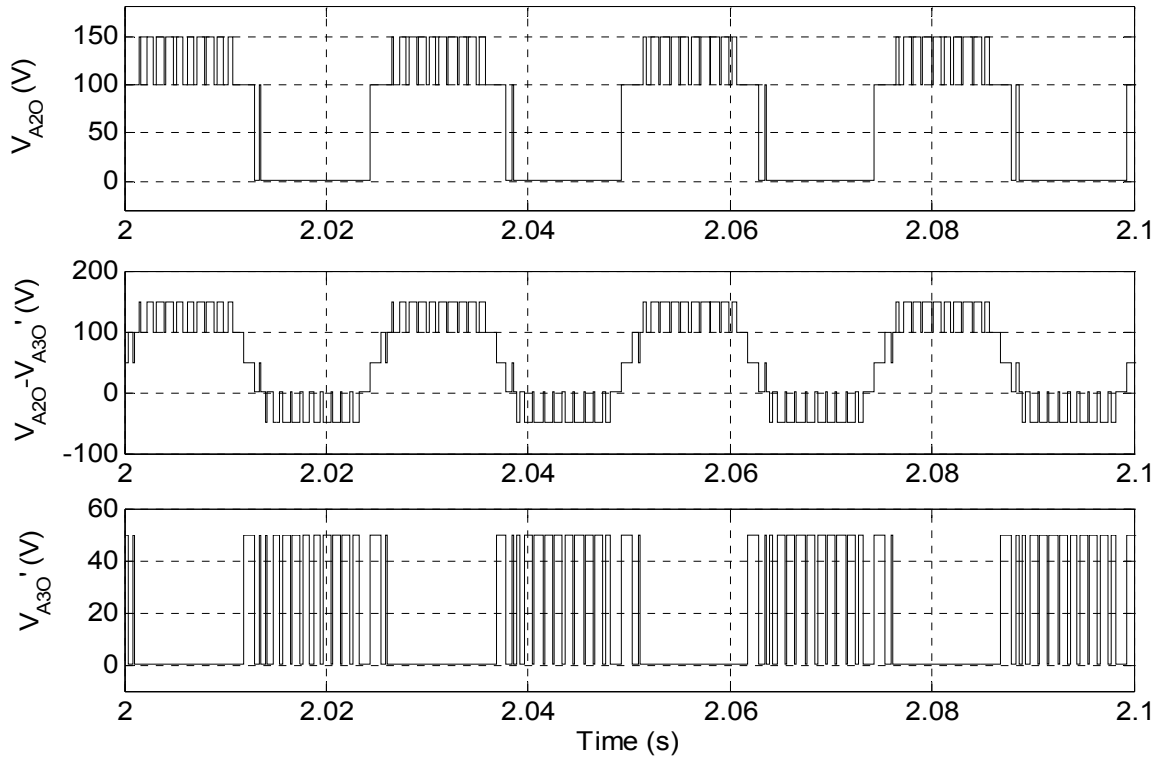



Fig. 7.21: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A2A3}$ (b) Current $i_{A2A3}$
(Experimental result: $m$=0.8; $f^*_m$ =40Hz)

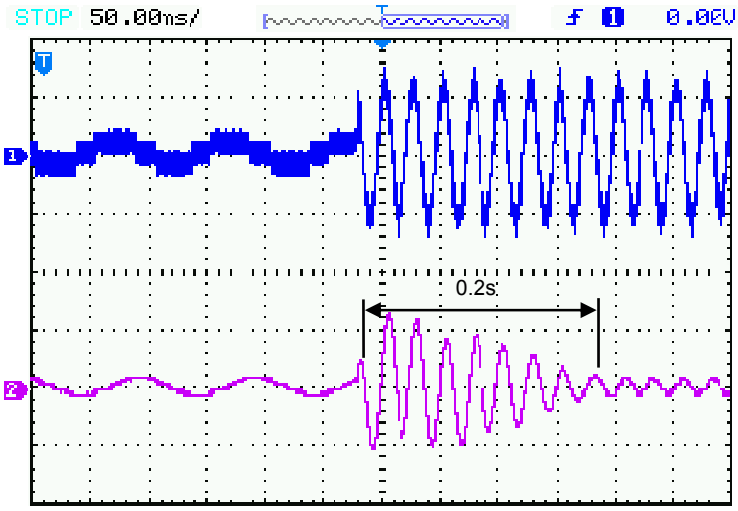



(a)

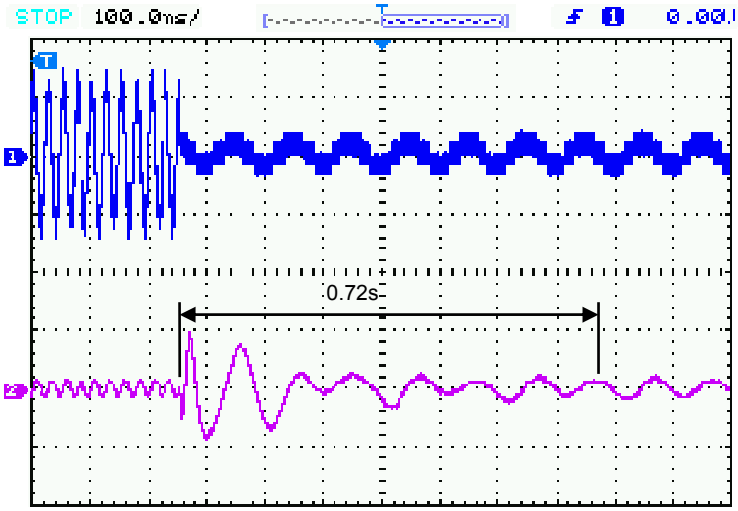



(b)

Fig. 7.22: (a) Motor phase-A, voltage $V_{A2A3}$ (upper trace) and current $i_{A2A3}$ (lower trace) of 5-level inverter fed open-end IM drive at no load
(b) Top trace; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace; Difference of 3-level inverter-A and two-level inverter-B pole voltages ($V_{A2O}$ - $V_{A3O'}$), Bottom trace; Two-level inverter-B pole voltage ($V_{A3O'}$)
(Simulation result: $m$=0.8; $f^*_m$ =40Hz)

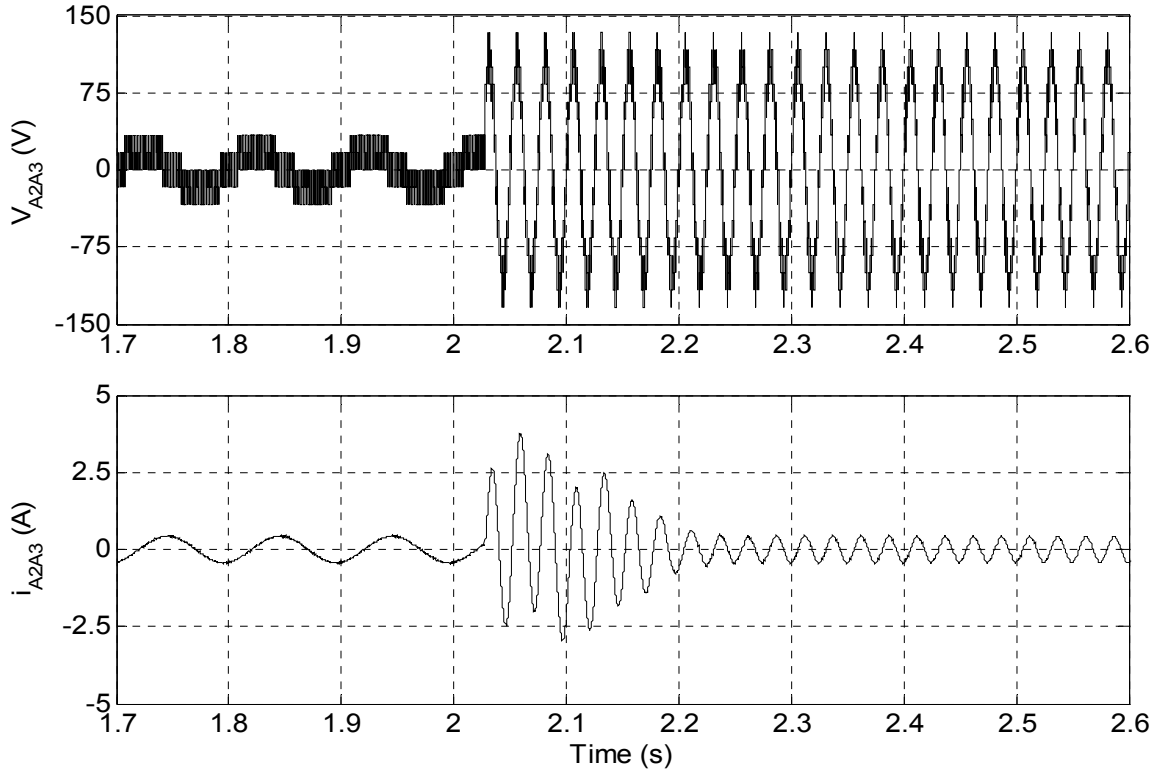



(a)

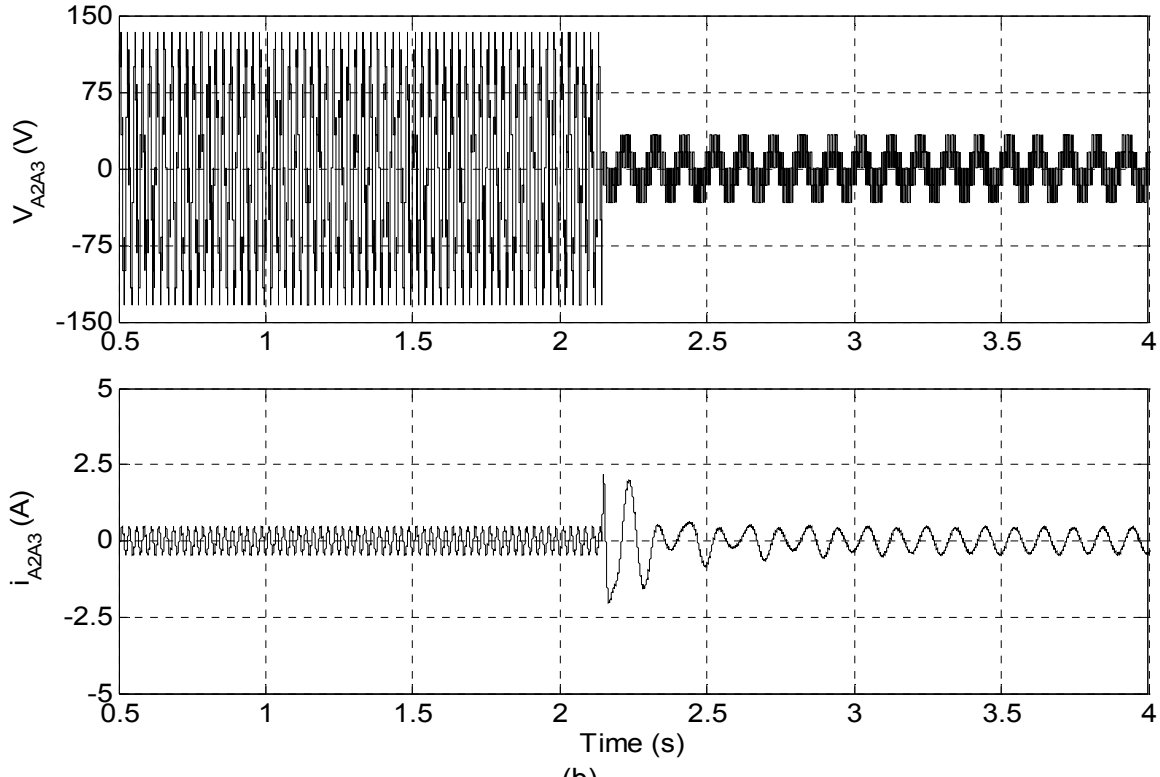



(b)

Fig. 7.23: Motor phase-A voltage $V_{A2A3}$ (upper trace Y-axis: 80V/div) and current $i_{A2A3}$ (lower trace Y-axis: 3A/div) waveforms under sudden change in operation from (a) two-level to 5-level at no-load (b) 5-level to two-level at no-load
(Experimental result)




(a)




(b)

Fig. 7.24: (a) Motor phase-A voltage $V_{A2A3}$ (upper trace) and current $i_{A2A3}$ (lower trace) waveforms under sudden change in operation from two-level to 5-level at no-load (b) Motor phase-A voltage $V_{A2A3}$ (upper trace) and current $i_{A2A3}$ (lower trace) waveforms under sudden change in operation from 5-level to two-level at no-load (Simulation result)

The comparison of experimental and downscaled simulation results obtained at different values of modulation index is given in Table 7.1. It can be observed from Table 7.1 that the experimental results are in good agreement with the simulation results under all operating conditions in steady state as well as in transient state.

Table 7.1: Comparison of experimental and downscaled simulation results of 5-level inverter

| Performance parameter | | Modulation index(*m*) | | | |
|---|---|---|---|---|---|
| | | 0.2 | 0.4 | 0.6 | 0.8 |
| Level of operation | Experimental | 3 | 3 | 5 | 5 |
| | Simulation | 3 | 3 | 5 | 5 |
| RMS of phase-A voltage (*V*) | Experimental | 21.9 | 39.63 | 58.04 | 76.44 |
| | Simulation | 22.2 | 39.65 | 58.03 | 76.46 |
| RMS of phase-A current (*A*) | Experimental | 0.302 | 0.305 | 0.354 | 0.392 |
| | Simulation | 0.306 | 0.306 | 0.353 | 0.397 |
| Frequency of phase voltage (*Hz)* | Experimental | 10 | 20 | 30 | 40 |
| | Simulation | 10 | 20 | 30 | 40 |
| THD of phase-A voltage in % | Experimental | 60.79 | 31.87 | 8.05 | 7.11 |
| | Simulation | 61.58 | 32.65 | 9.58 | 7.80 |
| Order of dominant voltage harmonic (amplitude in pu) | Experimental | 200±1 (0.160) | 100±1 (0.115) | 66±1 (0.075) | 50±1 (0.057) |
| | Simulation | 200±1 (0.162) | 100±1 (0.117) | 66±1 (0.077) | 50±1 (0.074) |
| THD of phase-A Current in % | Experimental | 3.57 | 3.47 | 1.10 | 5.71 |
| | Simulation | 5.15 | 4.68 | 1.82 | 5.82 |
| Order of dominant current harmonic (amplitude in pu) | Experimental | 100±2 (0.016) | 50±2 (0.013) | 17 (0.013) | 3 (0.04) |
| | Simulation | 100±2 (0.026) | 50±2 (0.017) | 17 (0.015) | 5 (0.048) |
| Settling time for 2-level to 5-level in sec | Experimental | 0.2 | | | |
| | Simulation | 0.275 | | | |
| Settling time for 5-level to 2-level in sec | Experimental | 0.72 | | | |
| | Simulation | 0.875 | | | |
| Sampling time | Experimental | 50 µSecond | | | |
| | Simulation | | | | |

### 7.3.2 Experimental Validation of 9-level Inverter

The performance of 9-level inverter topology proposed in Chapter-4 is investigated experimentally by operating a 1.5kW, 415V, 50Hz, 4pole open-end winding induction motor in constant *V/f* mode under no-load condition covering the entire range of linear modulation.

The gating signals for IGBTs are generated using Spartan-3 FPGA board of Opal RT-Lab real time digital simulator. The SVPWM algorithm proposed in section-4.3 is developed in MATLAB and converted in to C-code using RT-Lab Meta Controller (version 10.5) to configure the FPGA board. The four isolated DC link are implemented using single phase rectifier bridges and a 2200μF capacitor is connected at the output of rectifier. The switching frequency ($f_c$) is kept constant at 1kHz and DC link voltage is taken as 200V for experimentation. The motor used for experimentation having the same parameters as the simulated motor model (Appendix-A). The motor phase-A voltage ($V_{A2A4}$), phase-A current ($i_{A2A4}$), their harmonic spectrums, inverters pole-A voltages ($V_{A2O}$, $V_{A4O'}$) and difference of inverters pole-A voltages ($V_{A2O}$ - $V_{A4O'}$) are considered as evaluation criteria.

The motor is run at modulation indices ($m$) of 0.16, 0.28, 0.36, 0.42, 0.52 and 0.8 correspond to fundamental frequencies ($f^*_m$) of 8, 14, 18, 21, 26 and 40Hz respectively. The proposed 9-level inverter operates in 3-level, 4-level, 5-level, 6-level, 7-level and 9-level inversion mode correspond to these modulation indices. The performance of develop prototype of 9-level inverter scheme is experimentally investigated under steady-state as well as transient-state conditions and results are shown. As the experimentation is carried out at reduced voltage, for validating the experimental results, the simulation study at reduced DC link voltage is also carried out under same operating conditions and results are presented.

The experimental results obtained for motor phase-A voltage ($V_{A2A4}$), current ($i_{A2A4}$), pole-A voltages of individual inverters ($V_{A2O}$, $V_{A4O'}$) and their difference ($V_{A2O}$ - $V_{A4O'}$) at modulation index $m$ =0.16 are presented in Fig. 7.25. At this modulation index inverter operates in 3-level mode of operation and fundamental frequency ($f^*_m$) of the motor phase voltage is 8Hz. The motor phase-A voltage ($V_{A2A4}$) and current ($i_{A2A4}$) obtained in simulation (Fig. 7.27a) under same operating condition are similar to the experimentally obtained phase voltage and current waveforms (Fig. 7.25b). The normalized harmonic spectrum of experimentally obtained phase voltage and current are shown in Fig. 7.26(a) and Fig. 7.26(b) respectively. The THD of phase voltage is 40.65% with the occurrence of dominant harmonic component at the side band of 250$^{th}$ ($2f_c/f^*_m$ = 2*1000/8) order whereas THD of phase current is only 1.66% as shown in Fig. 7.26. The experimental results for pole-A voltages ($V_{A2O}$, $V_{A4O'}$) and their difference ($V_{A2O}$ - $V_{A4O'}$) are shown in Fig. 7.25(b). These waveforms are similar to the waveforms obtained in simulation (Fig. 7.27b) for 3-level mode of operation. It can be seen in pole voltages waveform that 3-level inverter-B operates in 3-level mode and take the values 0, 25 and 50 correspond to 0, $V_{DC}$/8 and 2$V_{DC}$/8 while the inverter-A is still clamped at zero voltage level. The difference of pole voltages ($V_{A2O}$ - $V_{A4O'}$) having three distinct voltage levels -(2/8)$V_{DC}$, -(1/8)$V_{DC}$ and zero confirming the correctness of modified SVPWM algorithm.

Experimental results for modulation index $m$ =0.28 (fundamental frequency $f^*_m$ =14Hz) are presented in Fig. 7.28 - Fig. 7.29. The simulated motor phase-A voltage ($V_{A2A4}$) and current ($i_{A2A4}$) waveforms shown in Fig. 7.30(a) are similar to the experimentally obtained phase voltage and current waveforms shown in Fig. 7.28(a). The actual and simulated pole voltages ($V_{A2O}$, $V_{A4O'}$) along with their difference ($V_{A2O}$ - $V_{A4O'}$) under same operating conditions are shown in Fig. 7.28(b) and Fig. 7.30(b) respectively. It is depicted in middle trace of Fig. 7.28(b) and Fig. 7.30(b) that the difference of pole voltages ($V_{A2O}$ - $V_{A4O'}$) posses four distinct levels -50, -25, 0 and 25 correspond to -(2/8)$V_{DC}$, -(1/8)$V_{DC}$, 0 and +(1/8)$V_{DC}$. It is also evident from pole voltage waveforms that in 4-level mode inverter-A is also started to operate in PWM mode but only for half of the duration of fundamental cycle and for remaining half cycle it is clamped at zero voltage. The normalized harmonic spectrums of phase voltage (upper trace Fig. 7.28a) and current (lower trace Fig. 7.28a) are shown in Fig. 7.29(a) and Fig. 7.29(b) respectively. The THD of phase voltage and current are 6.10% and 0.31% respectively and dominant harmonic component approximately occur at the side band of 143$^{rd}$ ($2f_c/f^*_m$ = 2*1000/14) as shown in Fig. 7.29.

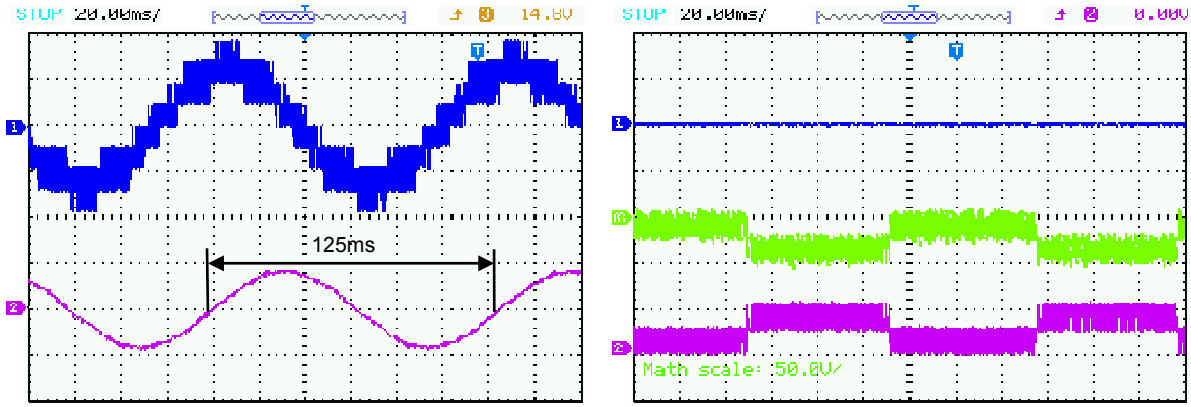



Fig. 7.25: (a) Motor phase-A, voltage $V_{A2A4}$ (upper trace Y-axis: 20V/div) and current $i_{A2A4}$ (lower trace Y-axis: 1A/div) of 9-level inverter fed open-end IM drive at no load
(b) Top trace Y-axis: 100V/div; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace Y-axis: 50V/div; Difference of 3-level inverter-A and inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$), Bottom trace Y-axis: 50V/div; 3-level inverter-B pole voltage ($V_{A4O'}$)
(Experimental result: $m$=0.16; $f^*_m$ =8Hz; 3-level mode)

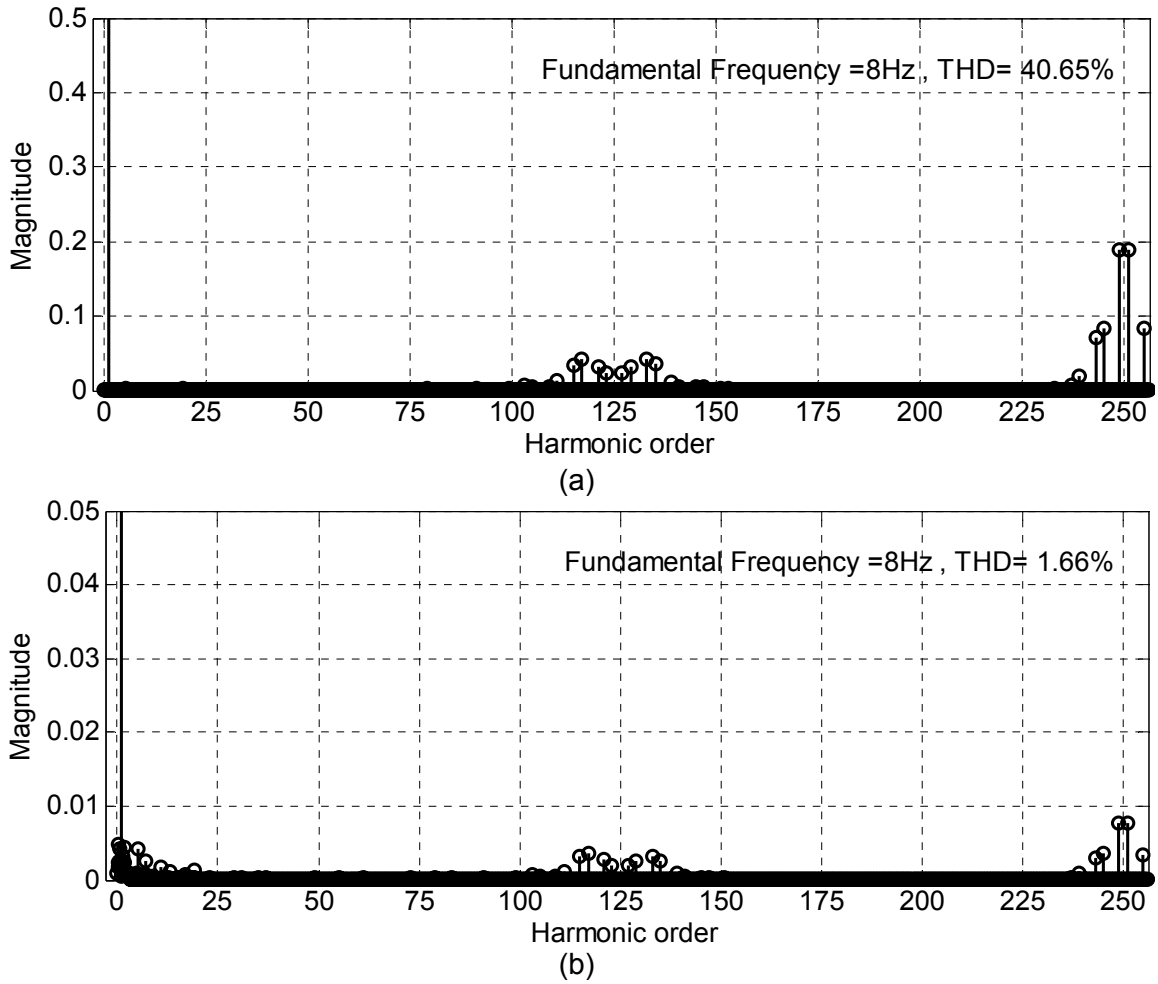
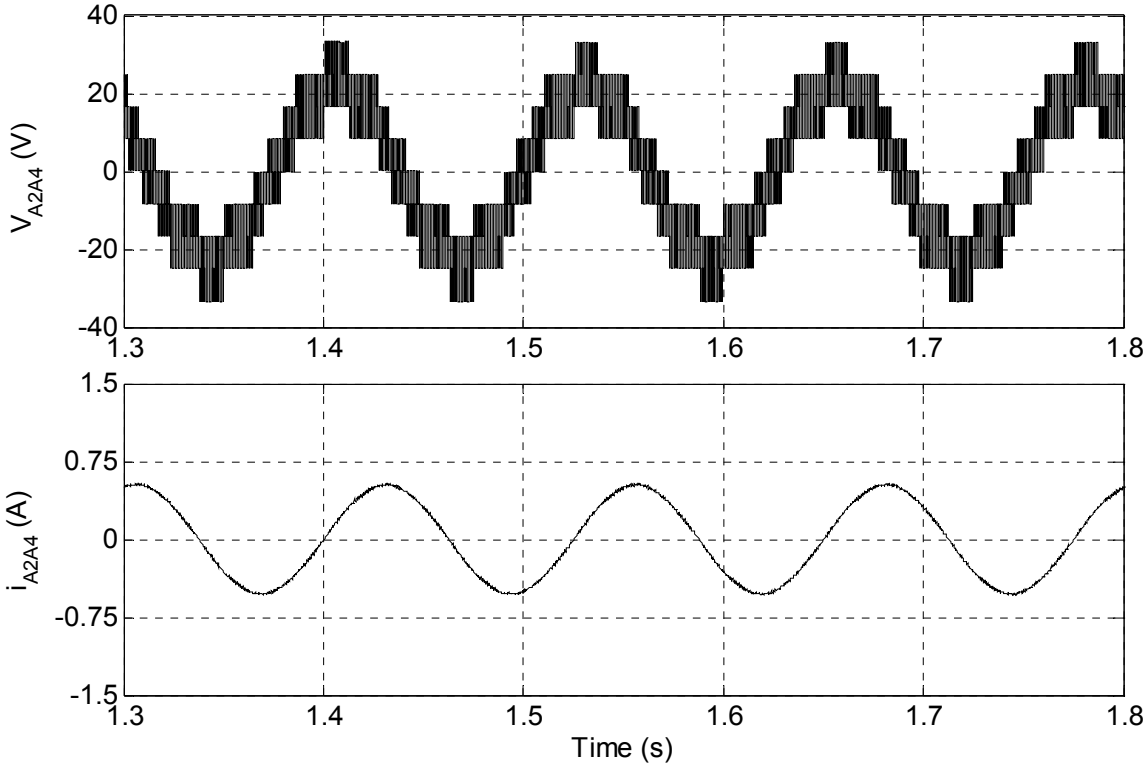
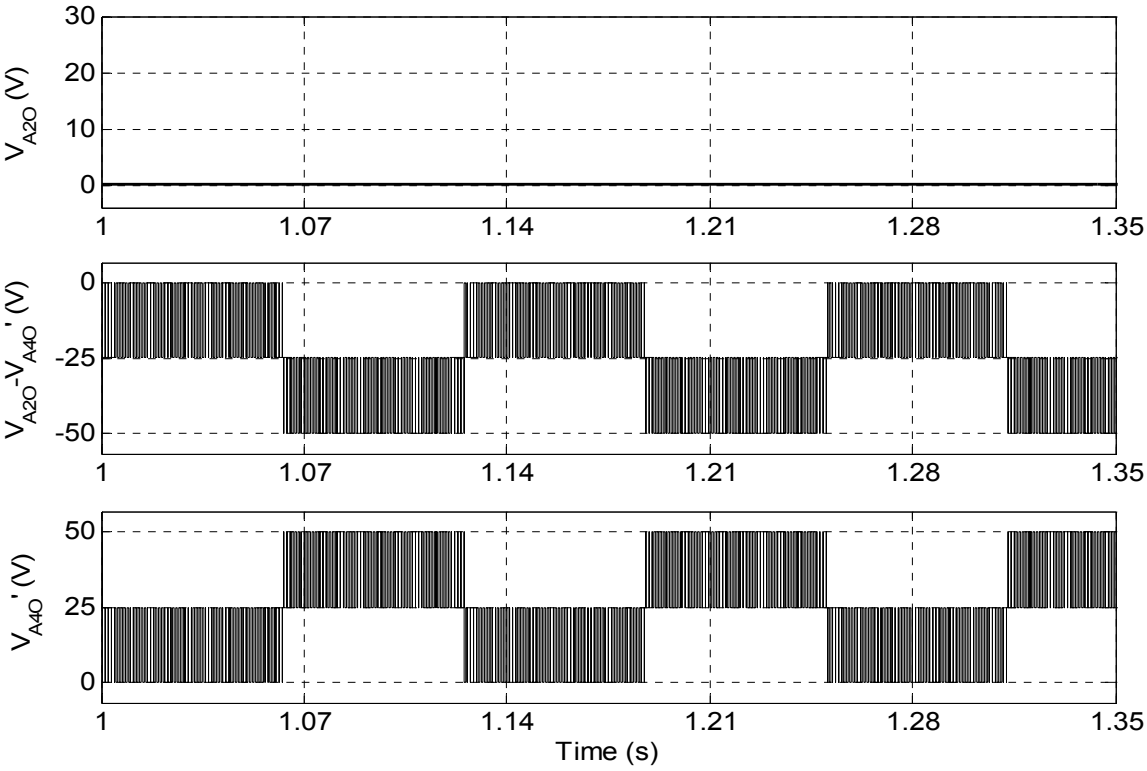



Fig. 7.26: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A2A4}$ (b) Current $i_{A2A4}$ (Experimental result: $m$=0.16; $f^*_m$ =8Hz; 3-level mode)




(a)




(b)

Fig. 7.27: (a) Motor phase-A, voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) of 9-level inverter fed open-end IM drive
(b) Top trace; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace; Difference of 3-level inverter-A and inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$), Bottom trace; 3-level inverter-B pole voltage ($V_{A4O'}$)
(Simulation result: $m$=0.16; $f^*_m$ =8Hz; 3-level mode)

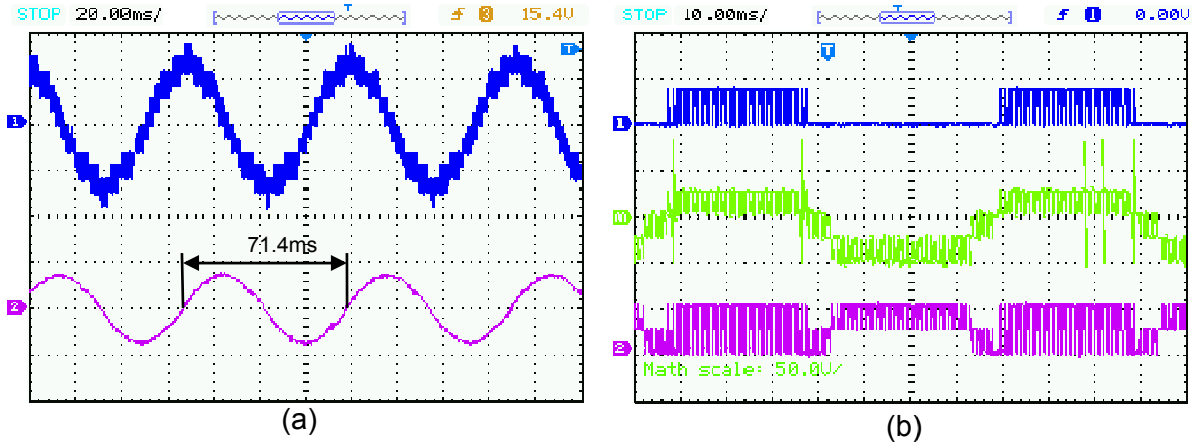



Fig. 7.28: (a) Motor phase-A, voltage $V_{A2A4}$ (upper trace Y-axis: 30V/div) and current $i_{A2A4}$ (lower trace Y-axis: 1A/div) of 9-level inverter fed open-end IM drive at no load
(b) Top trace Y-axis: 100V/div; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace Y-axis: 50V/div; Difference of 3-level inverter-A and inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$), Bottom trace Y-axis: 50V/div; 3-level inverter-B pole voltage ($V_{A4O'}$)
(Experimental result: $m$=0.28; $f^*_m$ =14Hz; 4-level mode)

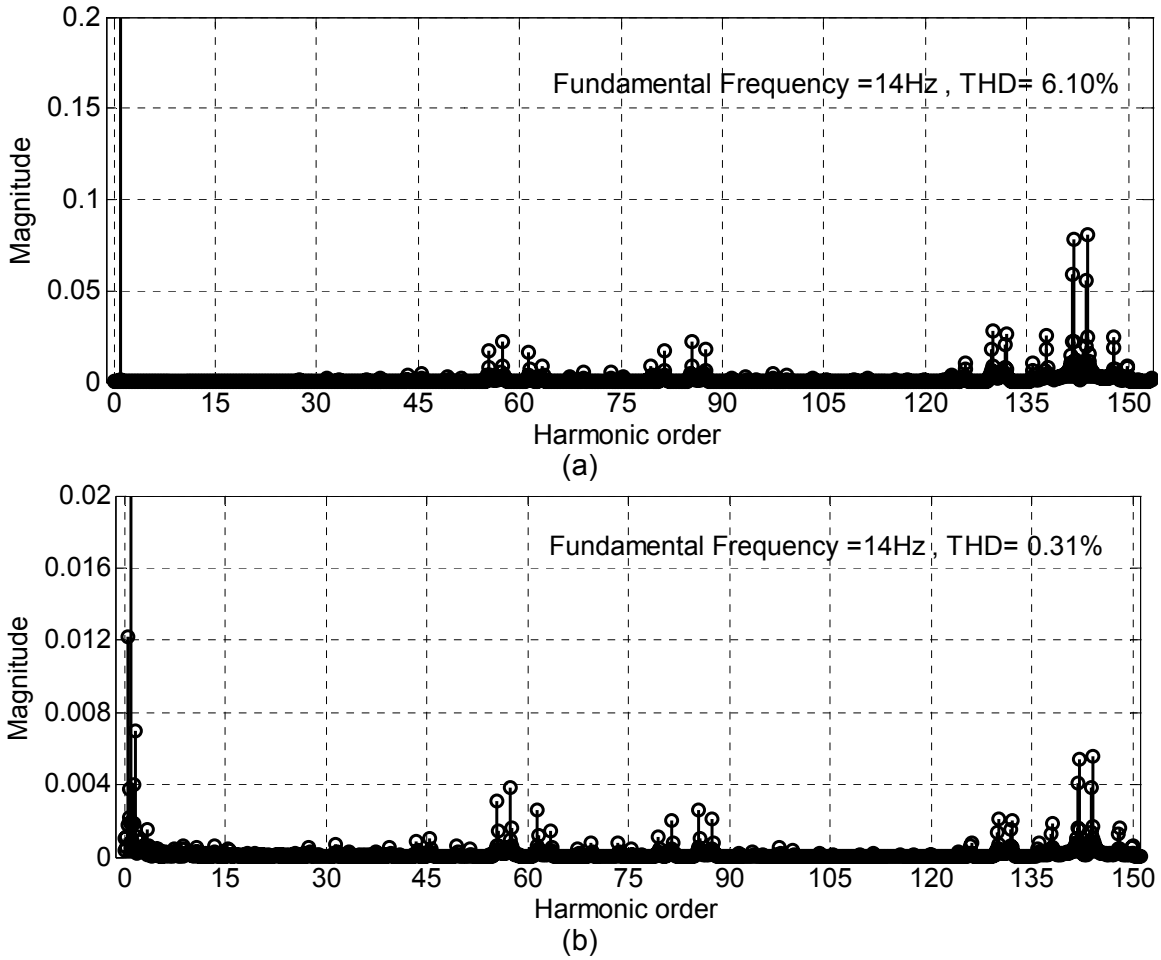
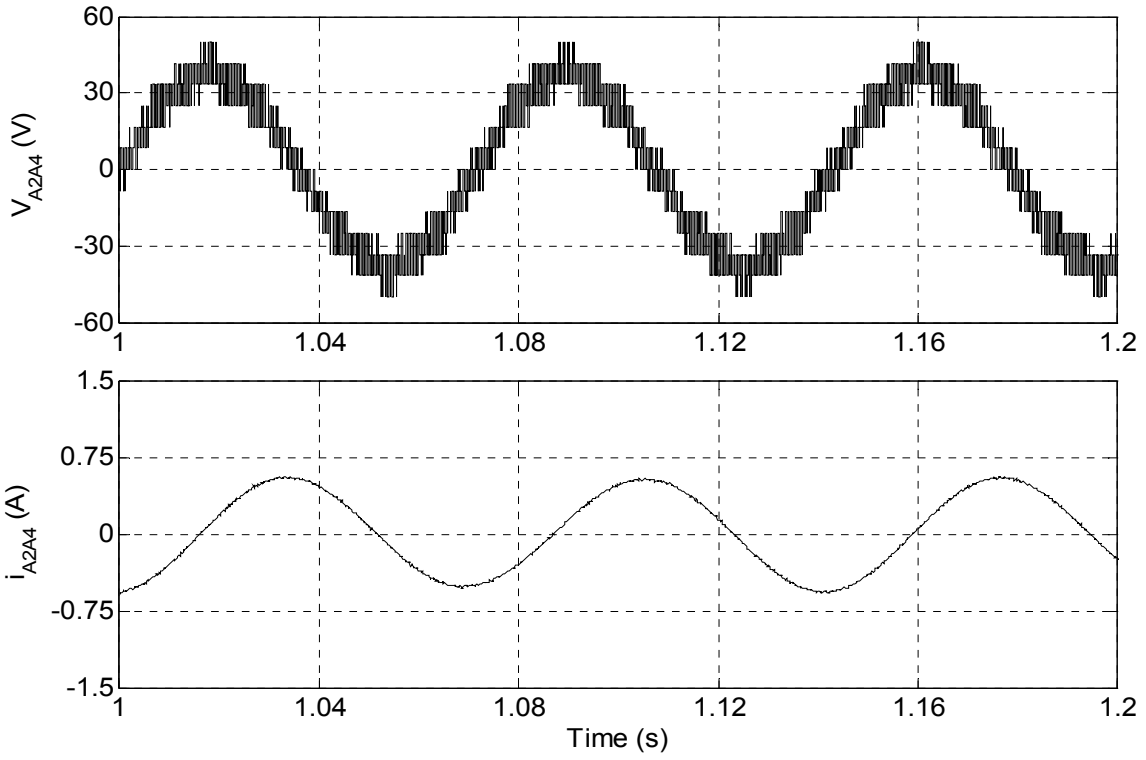
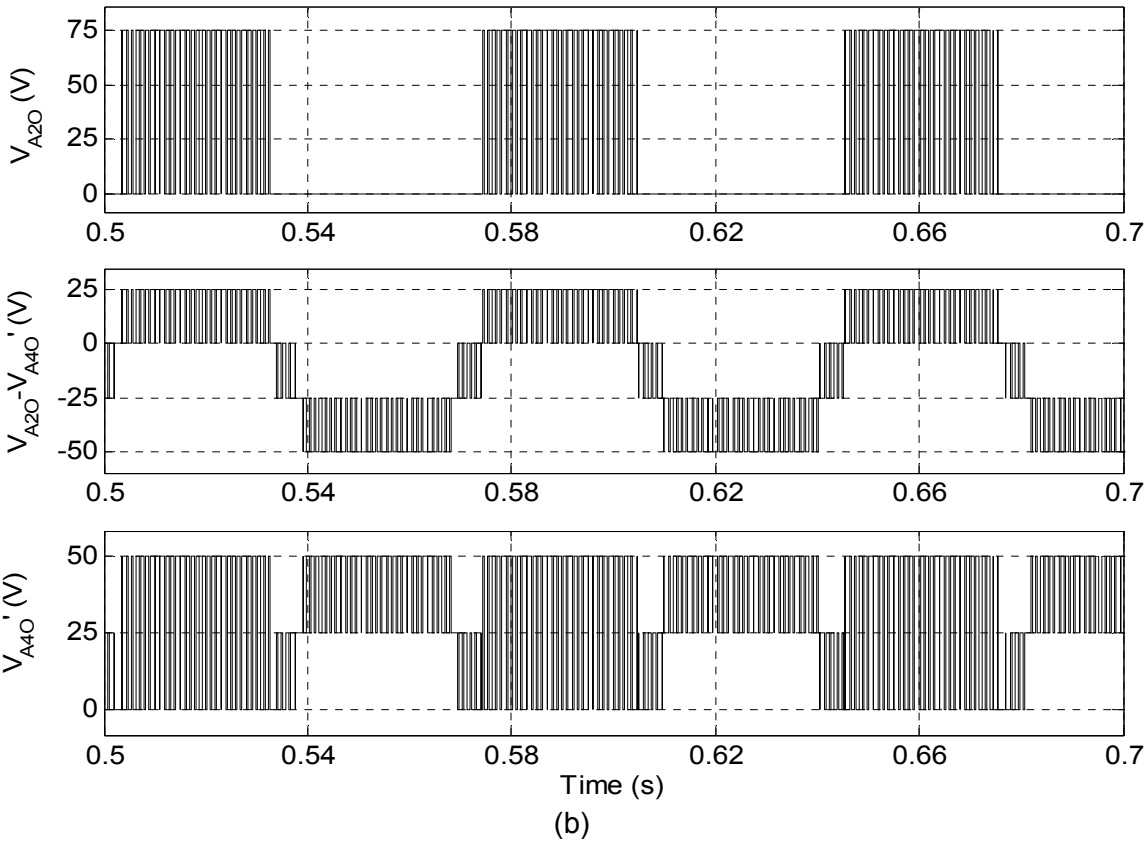



Fig. 7.29: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A2A4}$ (b) Current $i_{A2A4}$
(Experimental result: $m$=0.28; $f^*_m$ =14Hz; 4-level mode)




(a)




(b)

Fig. 7.30: (a) Motor phase-A, voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) of 9-level inverter fed open-end IM drive at no load
(b) Top trace; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace; Difference of 3-level inverter-A and inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$), Bottom trace; 3-level inverter-B pole voltage ($V_{A4O'}$)
(Simulation result: $m$=0.28; $f^*_m$ =14Hz; 4-level mode)

The waveforms given in Fig. 7.31 and Fig. 7.32 depict the performance under 5-level operation of the prototype inverter, at modulation index $m$=0.36 and fundamental frequency ($f^*_m$) of 18Hz. The experimentally obtained motor phase-A voltage ($V_{A2A4}$) and current ($i_{A2A4}$) are presented in Fig. 7.31(a). The simulated phase voltage and current are shown in Fig. 7.33(a). The experimental results are in conformity of simulation results. The normalized harmonic spectrum of actual phase-A voltage and current are presented in Fig. 7.32(a) and Fig. 7.32(b) respectively. The experimental results for pole-A voltage of individual inverters ($V_{A2O}$, $V_{A4O'}$) and difference of pole voltages ($V_{A2O}$ - $V_{A4O'}$) are depicted in Fig. 7.31(b) and simulated results are presented in Fig. 7.33(b). It can be observed in difference of pole voltage ($V_{A2O}$ - $V_{A4O'}$) waveform (middle trace of Fig. 7.31b and Fig. 7.33b) that the five levels realised in this mode are $\pm$50, $\pm$25 and 0 correspond to $\pm(2/8)V_{DC}$, $\pm(1/8)V_{DC}$ and 0. In this range of operation 3-level inverter-A operates in two-level mode whereas inverter-B operates in 3-level which can be observed in experimental (Fig. 7.31b) and simulated (Fig. 7.33b) pole voltage waveforms. The THD of phase voltage is 5.58% and dominant harmonic component occur approximately at the side band of $111^{th}$ ($2f_c/f^*_m$ = 2*1000/18) order. The THD of phase current (Fig. 7.32b) is only 0.47%.

Another set of experimental and simulation result obtained when motor is operated at modulation index $m$=0.42 and fundamental frequency ($f^*_m$) of 21Hz are shown in Fig. 7.34 - Fig. 7.36. The 9-level inverter operates in 6-level inversion mode at this modulation index. Experimentally obtained motor phase-A voltage and current are shown in Fig. 7.34(a) and individual inverters pole-A voltage and their difference are shown in Fig. 7.34(b). Fig. 7.36 (a) shows the simulated motor phase-A voltage and current waveforms. The pole voltages and difference in pole voltages obtained in simulation are presented in Fig. 7.36(b). It can be observed from pole voltages waveforms (Fig. 7.34b and Fig. 7.36b) that 3-level inverter-A still operates in two-level mode whereas inverter-B attains all three levels. The difference of pole voltage ($V_{A2O}$ - $V_{A4O'}$) waveforms (middle trace of Fig. 7.34b and Fig. 7.36b) posses six distinct levels which are $\pm$50, $\pm$25 ,0 and +75 correspond to $\pm(2/8)V_{DC}$, $\pm(1/8)V_{DC}$, 0 and $+(3/8)V_{DC}$. The normalized harmonic spectrum of experimentally obtained phase voltage is shown in Fig. 7.35(a). The total harmonic distortion (THD) in the harmonic spectrum of phase voltage is found 3.58% and position of occurrence of dominant harmonic is approximately at the side band of $96^{th}$ ($2f_c/f^*_m$ = 2*1000/21) order. Normalized harmonic spectrum of phase current (lower trace of Fig. 7.34a) is presented in Fig. 7.35(b). THD of phase current $i_{A2A4}$ is very less 0.34% and lower order harmonics are also present.

It may be seen that the actual phase voltage, current and pole voltages waveforms obtained experimentally (Fig. 7.34) are in agreement with the one obtained by simulation (Fig. 7.36) in 6-level inversion mode as well.

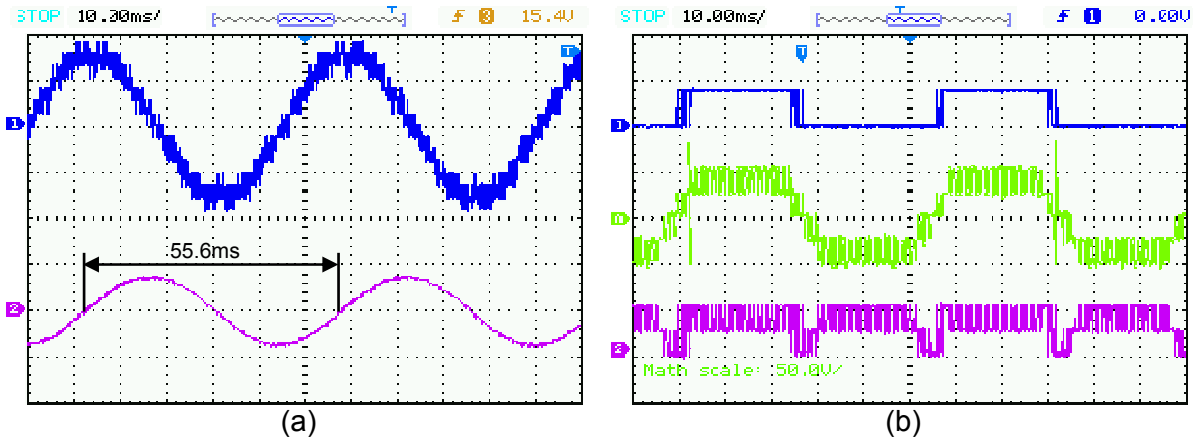



Fig. 7.31: (a) Motor phase-A, voltage $V_{A2A4}$ (upper trace Y-axis: 35V/div) and current $i_{A2A4}$ (lower trace Y-axis: 1A/div) of 9-level inverter fed open-end IM drive at no load (b) Top trace Y-axis: 100V/div; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace Y-axis: 50V/div; Difference of 3-level inverter-A and inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$), Bottom trace Y-axis: 50V/div; 3-level inverter-B pole voltage ($V_{A4O'}$) (Experimental result: $m$=0.36; $f^*_m$ =18Hz; 5-level mode)

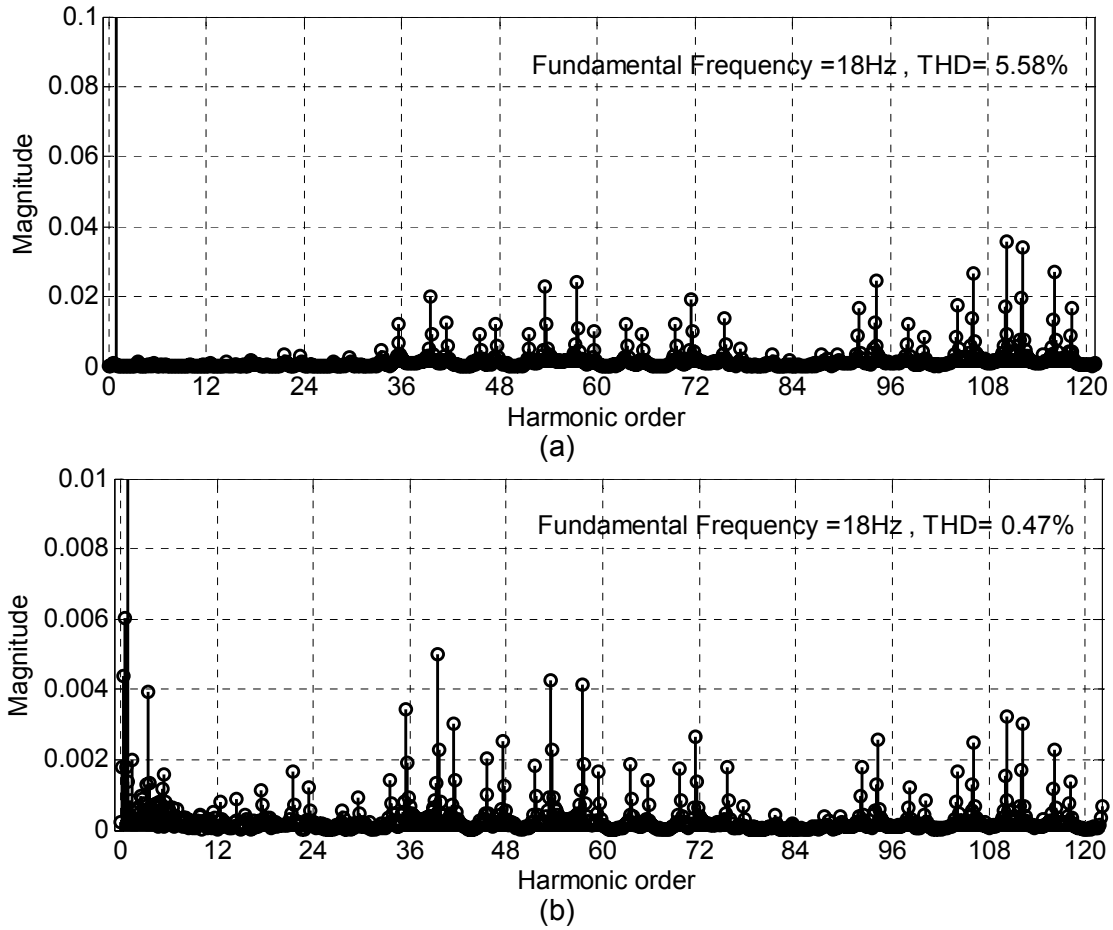
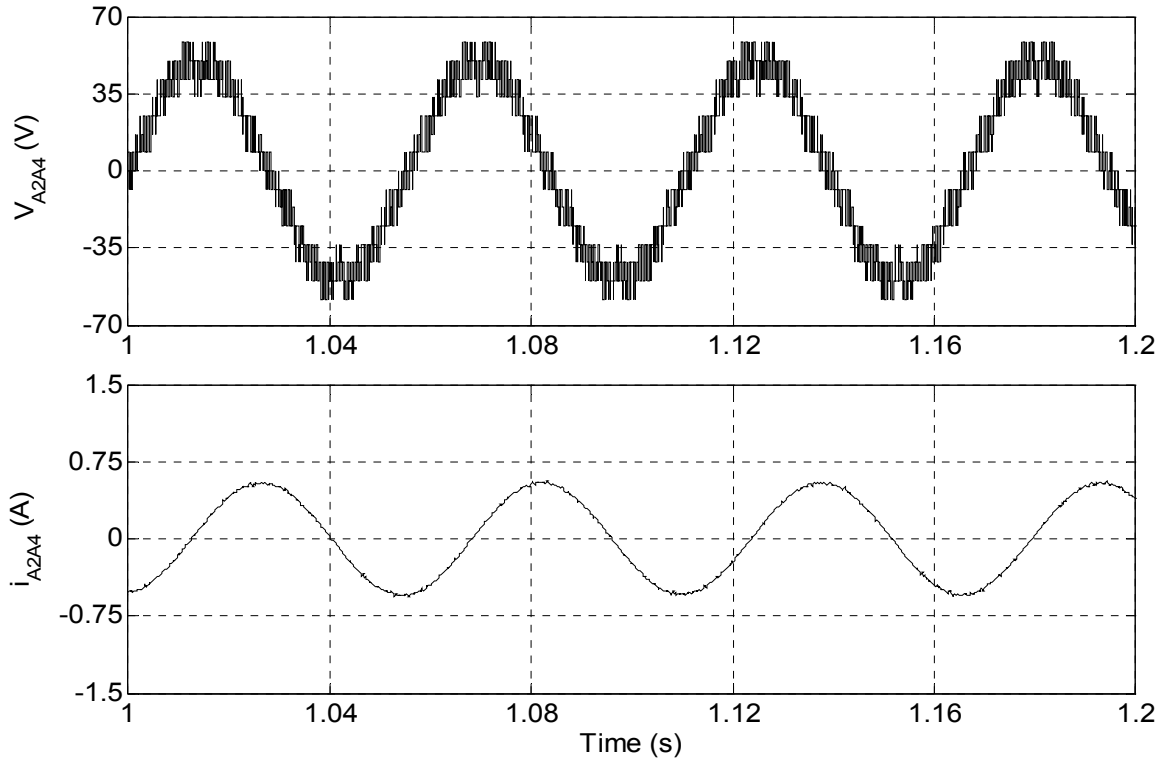
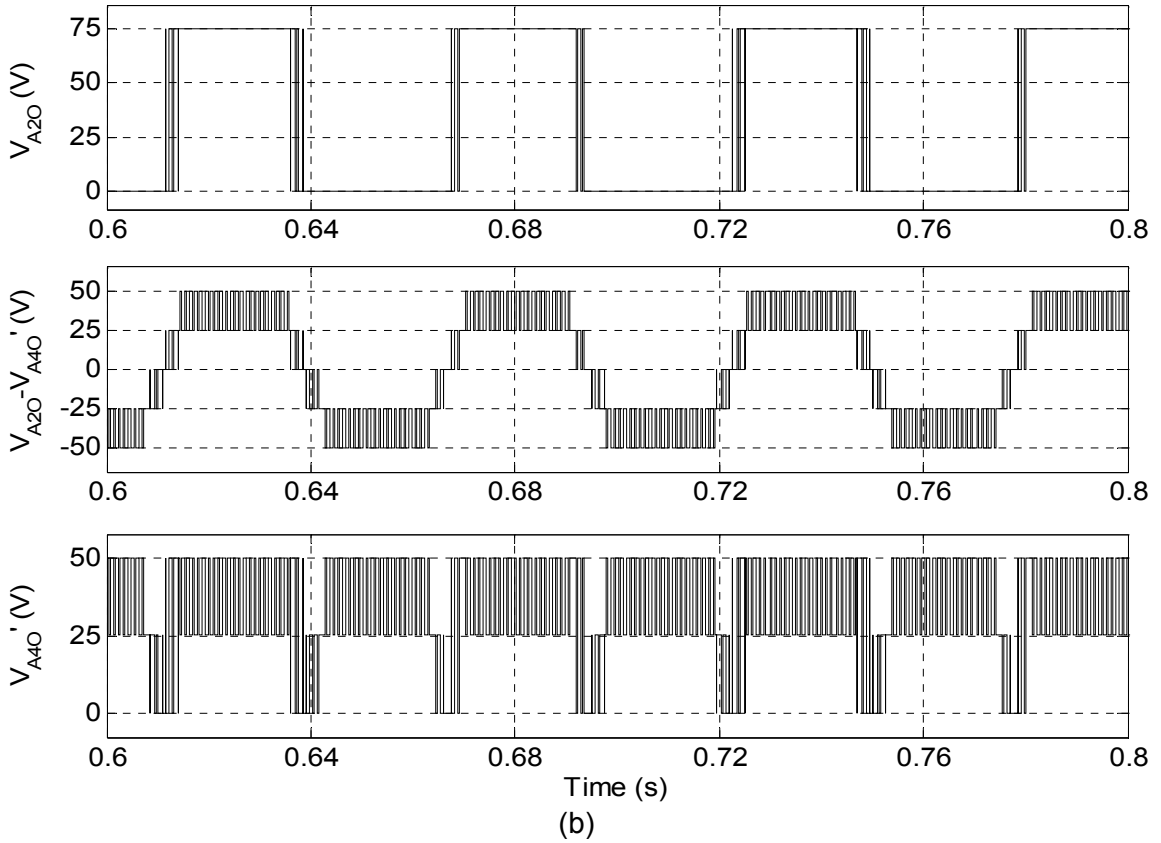



Fig. 7.32: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A2A4}$ (b) Current $i_{A2A4}$ (Experimental result: $m$=0.36; $f^*_m$ =18Hz; 5-level mode)




(a)




(b)

Fig. 7.33: (a) Motor phase-A, voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) of 9-level inverter fed open-end IM drive at no load
(b) Top trace; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace; Difference of 3-level inverter-A and inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$), Bottom trace; 3-level inverter-B pole voltage ($V_{A4O'}$)
(Simulation result: $m$=0.36; $f^*_m$ =18Hz; 5-level mode)

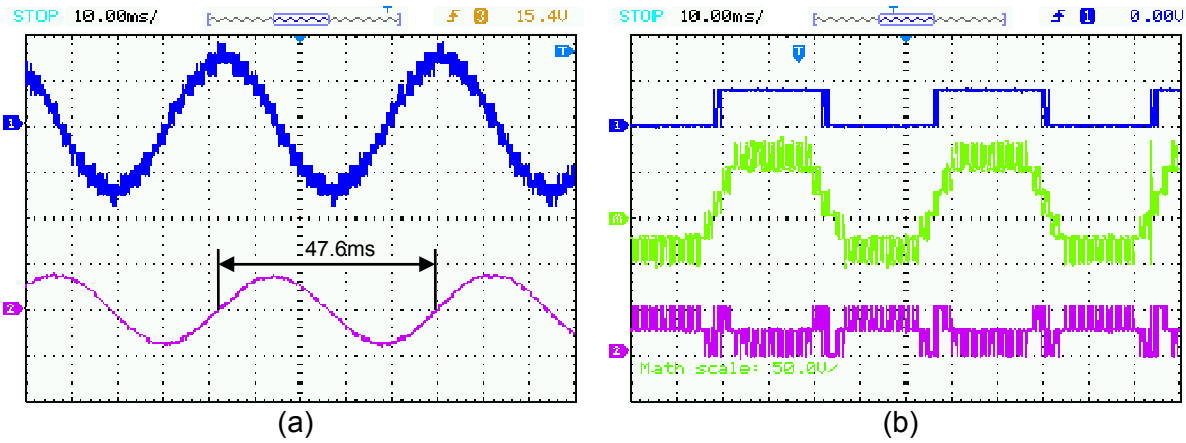



Fig. 7.34: (a) Motor phase-A, voltage $V_{A2A4}$ (upper trace Y-axis: 40V/div) and current $i_{A2A4}$ (lower trace Y-axis: 1A/div) of 9-level inverter fed open-end IM drive at no load
(b) Top trace Y-axis: 100V/div; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace Y-axis: 50V/div; Difference of 3-level inverter-A and inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$), Bottom trace Y-axis: 50V/div; 3-level inverter-B pole voltage ($V_{A4O'}$)
(Experimental result: $m$=0.42; $f^*_m$ =21Hz; 6-level mode)

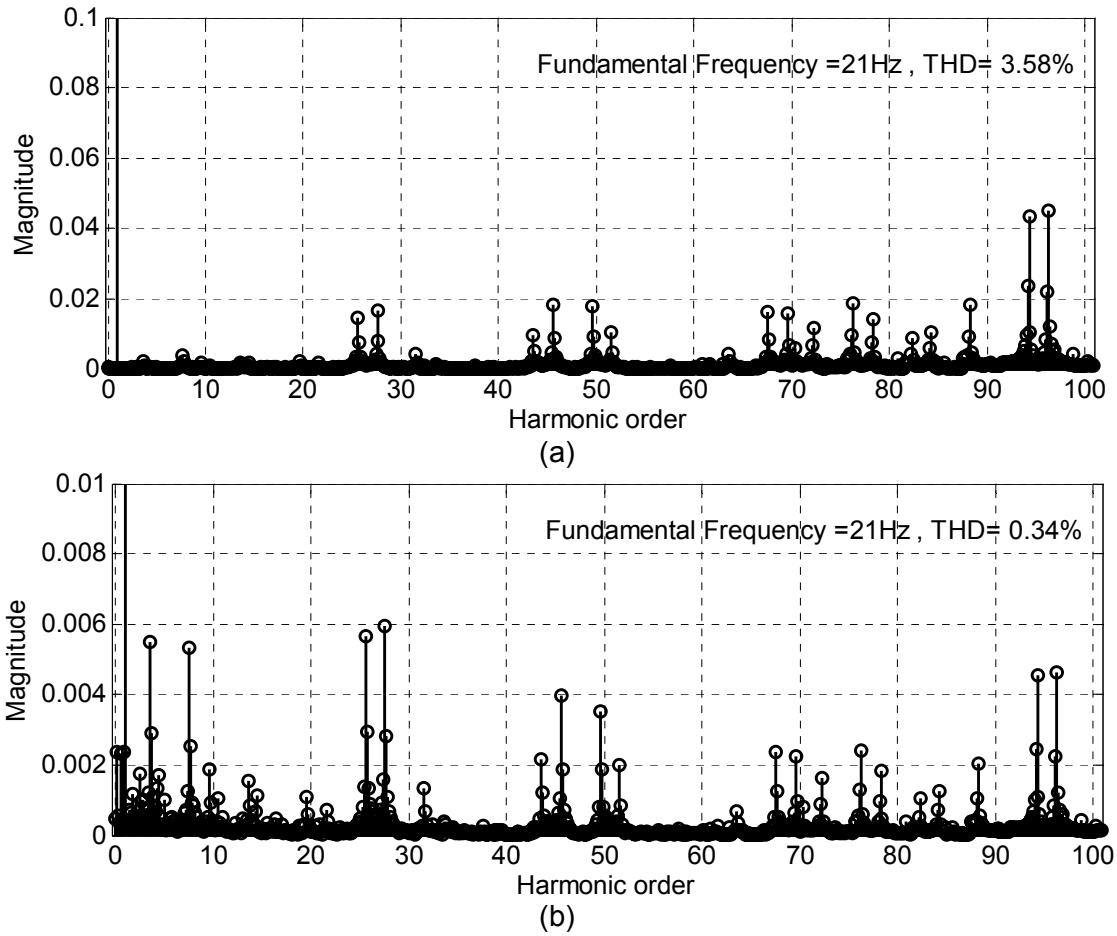
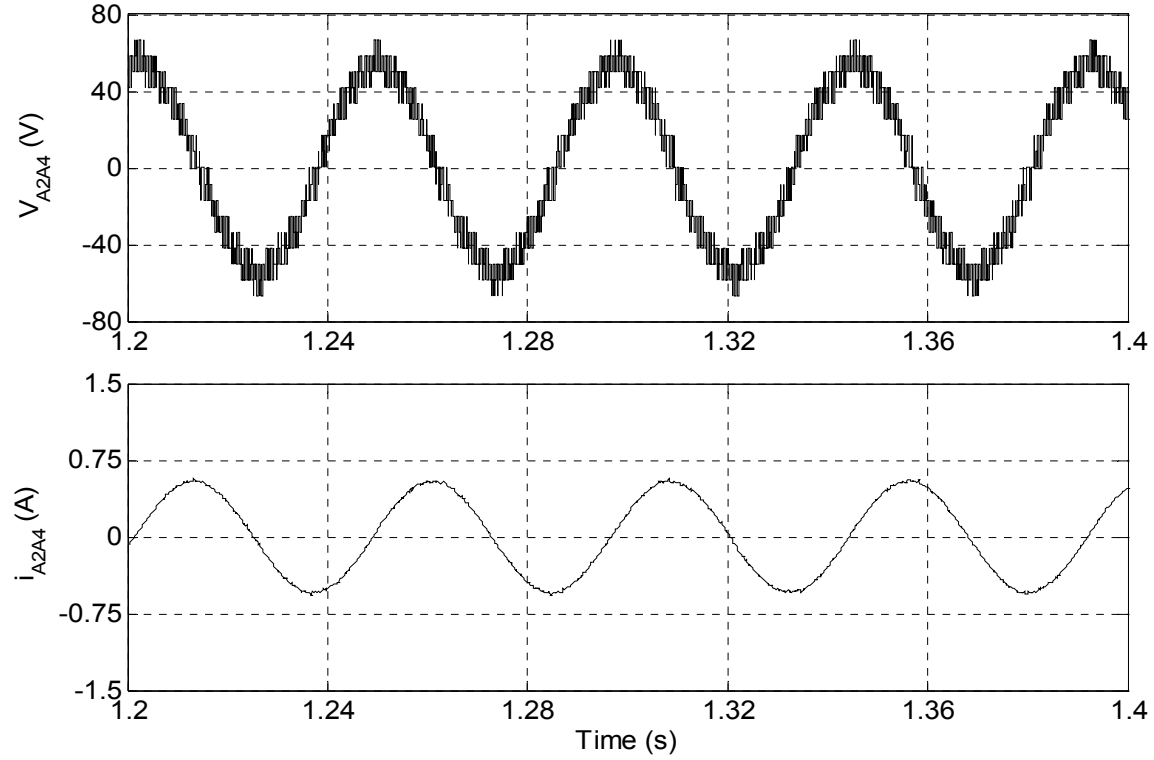
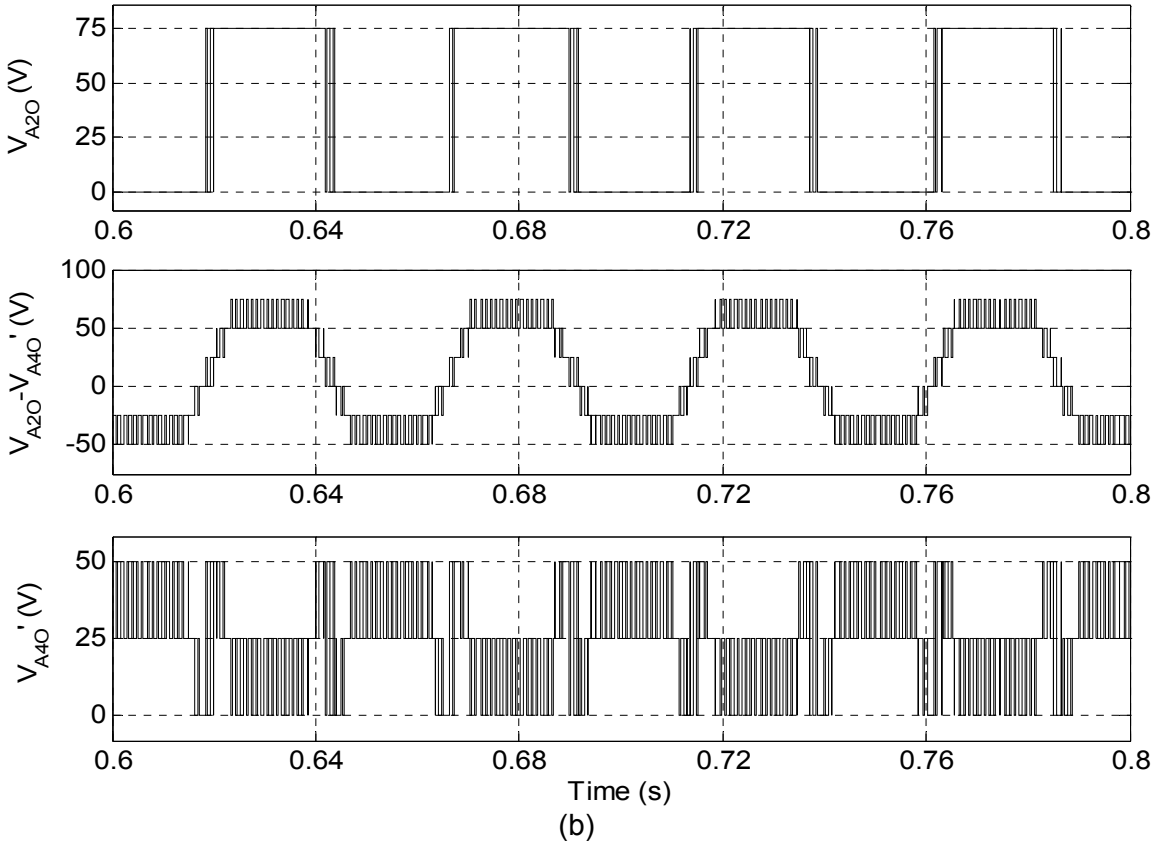



Fig. 7.35: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A2A4}$ (b) Current $i_{A2A4}$
(Experimental result: $m$=0.42; $f^*_m$ =21Hz; 6-level mode)




(a)




(b)

Fig. 7.36: (a) Motor phase-A, voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) of 9-level inverter fed open-end IM drive at no load
(b) Top trace; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace; Difference of 3-level inverter-A and inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$), Bottom trace; 3-level inverter-B pole voltage ($V_{A4O'}$)
(Simulation result: $m$=0.42; $f^*_m$ =21Hz; 6-level mode)

To investigate the performance of inverter under 7-level mode of operation motor is operated at modulation index $m$=0.52 and fundamental frequency ($f^*_m$) of 26Hz. Motor phase-A voltage and current are shown in Fig. 7.37(a) (experimental) and Fig. 7.39(a) (simulation). It can be observed in pole voltages waveforms presented in Fig. 7.37(b) (experimental) and Fig. 7.39(b) (simulated) that in 7-level operation both 3-level inverters operate in 3-level mode and difference of their pole voltage contains seven distinct levels as $\pm$50, $\pm$25, 0, +75 and +100 as depicted in difference of pole voltage ($V_{A2O}$ - $V_{A4O'}$) waveform (middle trace of Fig. 7.37b and Fig. 7.39b). As the DC link voltage is 200V therefore these voltage levels correspond to $\pm(2/8)V_{DC}$, $\pm(1/8)V_{DC}$, 0, $+(3/8)V_{DC}$ and $+(4/8)V_{DC}$. Another important observation can be made from pole voltage waveform that switching occur in inverter-A only for half of the duration of fundamental cycle and for remaining half cycle it is clamped at zero voltage level so effective switching frequency is half of the actual switching frequency. The normalized harmonic spectrum of experimentally obtained phase voltage is depicted in Fig. 7.38(a). The dominant harmonic component in the spectrum of phase voltage approximately occur at the side band of $77^{th}$ ($2f_c/f^*_m$ = 2*1000/26) order and THD is 3.20%. The normalized harmonic spectrum of phase current (lower trace of Fig. 7.37a) shown in Fig. 7.38(b) and it is found that lower order harmonics are increased in phase current.

Fig. 7.40 through Fig. 7.42 illustrates the performance of inverter under 9-level mode of operation at modulation index $m$=0.8. In this mode the modulating signals cover the entire regions so 9-level inversion operation is achieved. The fundamental frequency of applied voltage across the motor terminal is 40Hz. Simulated phase voltage and current waveforms (Fig. 7.42a) are similar to the one obtained by experimentation (Fig. 7.40a) in this case as well. The Motor phase voltage waveform is further improved and approach towards sinusoidal. Inverter-A pole voltage switch between 3-levels 0, 75 and 150 correspond to 0, $3V_{DC}/8$ and 6 $V_{DC}/8$ as shown in pole voltage waveforms (Fig. 7.40b; experimental, Fig. 7.42b; simulated). Similarly Inverter-B also operates in 3-level mode (bottom trace of Fig. 7.40b; experimental and Fig. 7.42b; simulated) and give the pole voltage 0, 25 and 50 correspond to 0, $V_{DC}/8$ and $2V_{DC}/8$. The difference of pole voltages (middle trace of Fig. 7.40b; experimental and Fig. 7.42b; simulated) contains nine distinct voltage levels as $\pm$50, $\pm$25, 0, +75, +100, +125 and +150 corresponding to the levels $\pm(2/8)V_{DC,}$ $\pm(1/8)V_{DC}$, 0, $+(3/8)V_{DC}$, $+(4/8)V_{DC}$, $+(5/8)V_{DC}$ and $+(6/8)V_{DC}$. The normalized harmonic spectrum of phase voltage and current (upper and lower trace of Fig. 7.40) are shown in Fig. 7.41(a) and Fig. 7.41(b) respectively. The lower order harmonics are increased in harmonic spectrum of phase current. The experimental and simulation results are almost matching to each other in 9-level inversion mode also.

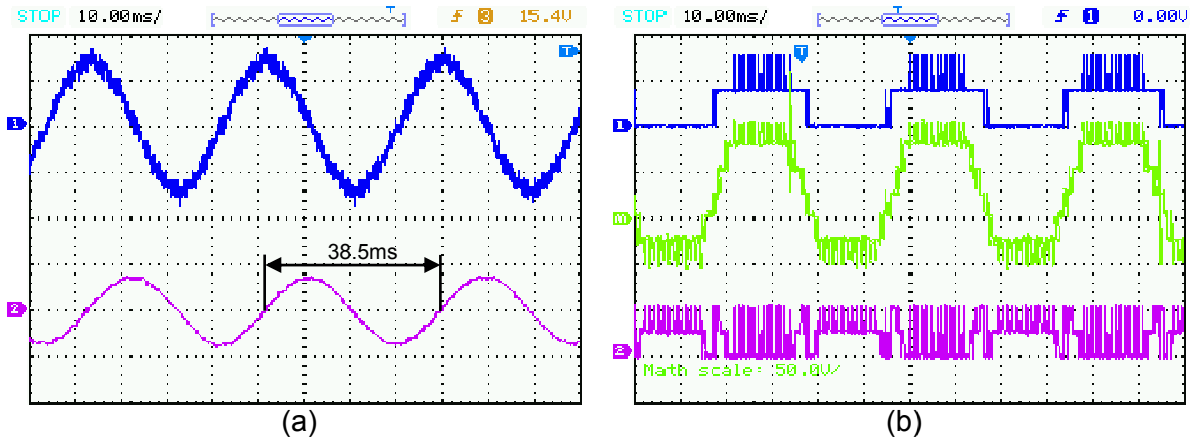



Fig. 7.37: (a) Motor phase-A, voltage $V_{A2A4}$ (upper trace Y-axis: 50V/div) and current $i_{A2A4}$ lower trace Y-axis: 1A/div) of 9-level inverter fed open-end IM drive at no load
(b) Top trace Y-axis: 100V/div; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace Y-axis: 50V/div; Difference of 3-level inverter-A and inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$), Bottom trace Y-axis: 50V/div; 3-level inverter-B pole voltage ($V_{A4O'}$)
(Experimental result: $m$=0.52; $f^*_m$ =26Hz; 7-level mode)

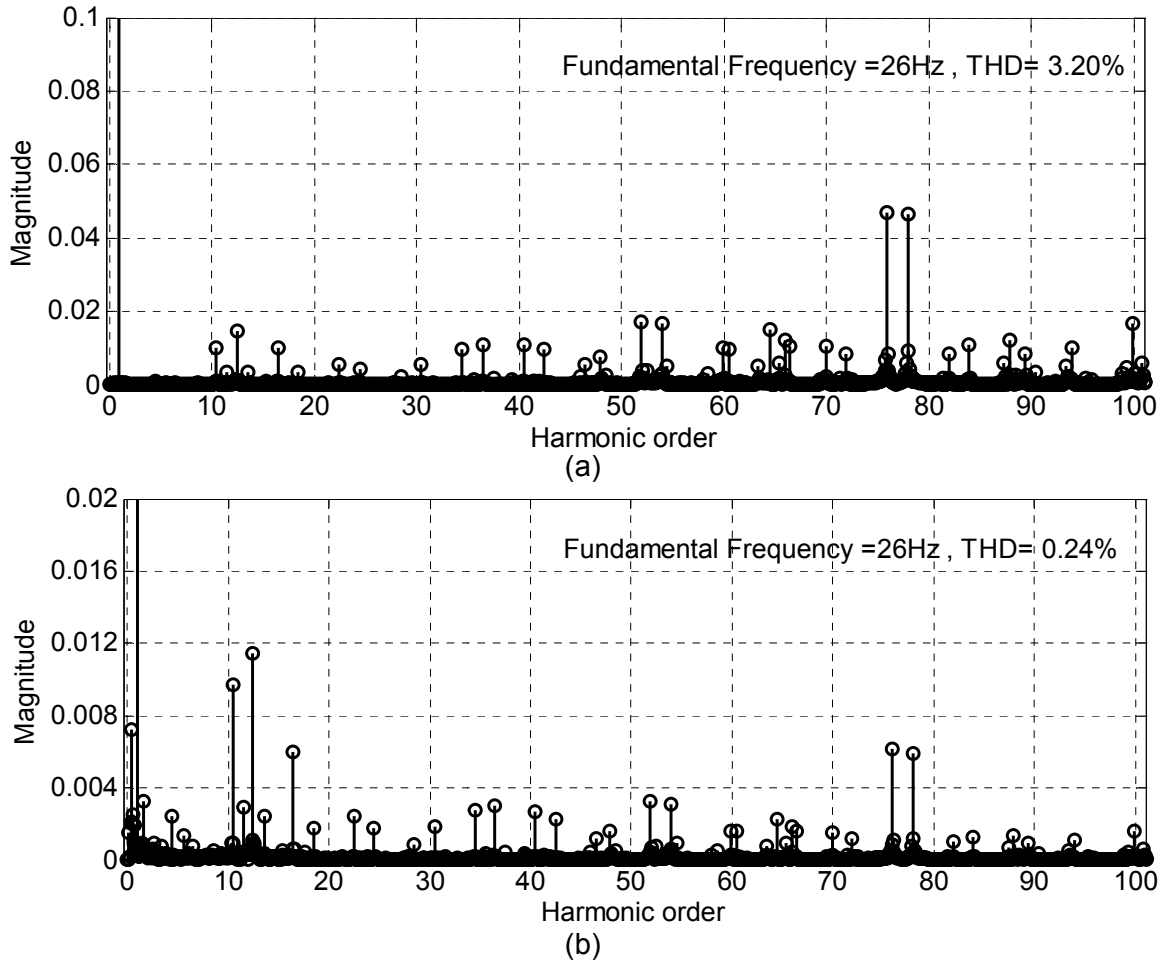
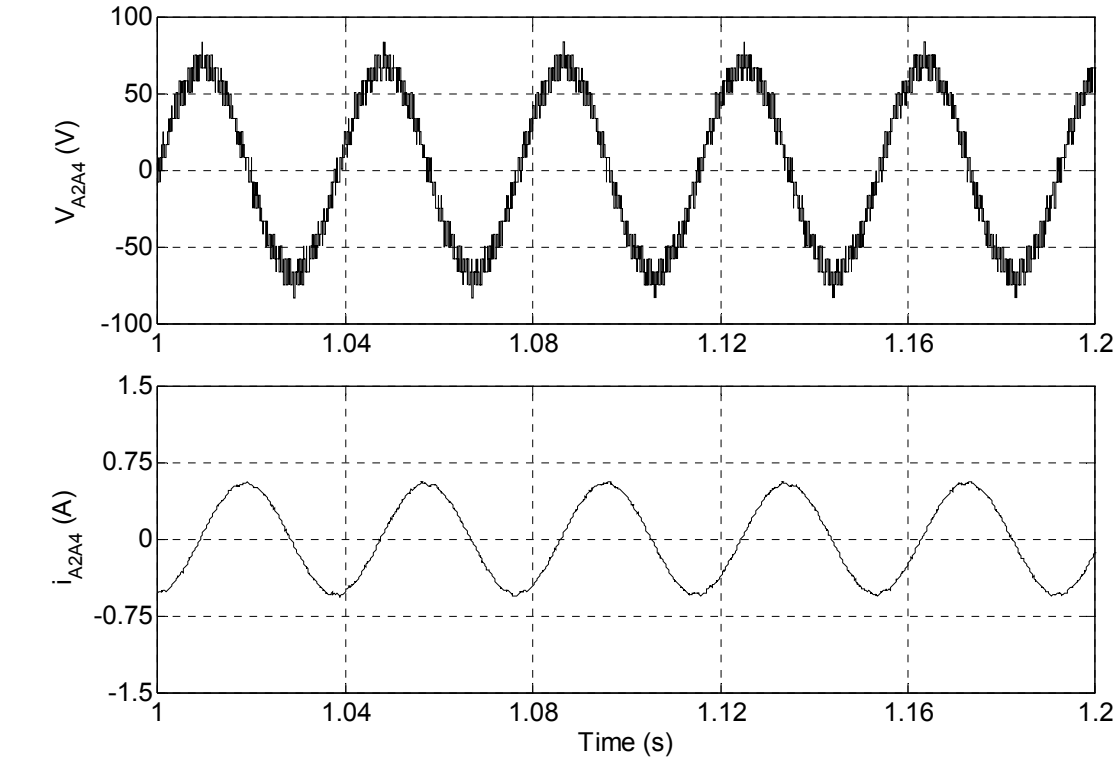
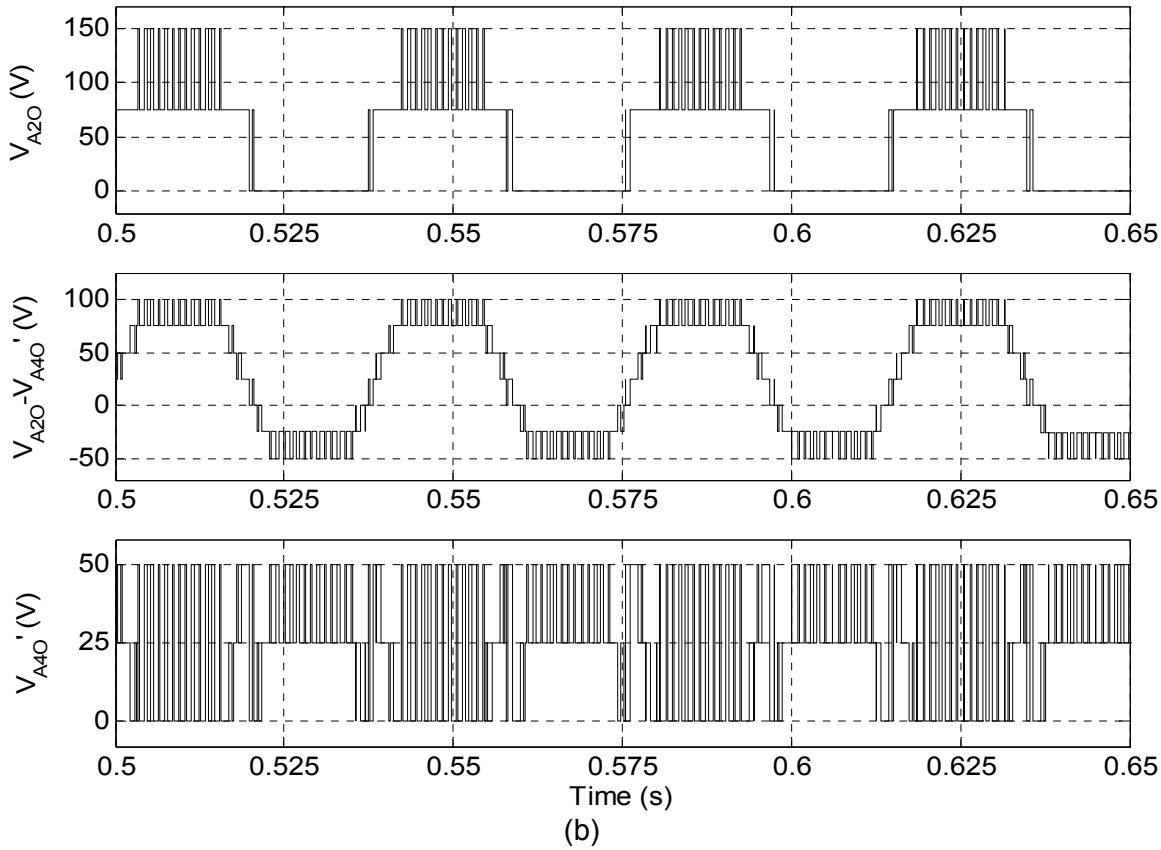



Fig. 7.38: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A2A4}$ (b) Current $i_{A2A4}$
(Experimental result: $m$=0.52; $f^*_m$ =26Hz; 7-level mode)




(a)




(b)

Fig. 7.39: (a) Motor phase-A, voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) of 9-level inverter fed open-end IM drive at no load
(b) Top trace; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace; Difference of 3-level inverter-A and inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$), Bottom trace; 3-level inverter-B pole voltage ($V_{A4O'}$)
(Simulation result: $m$=0.52; $f^*_m$ =26Hz; 7-level mode)

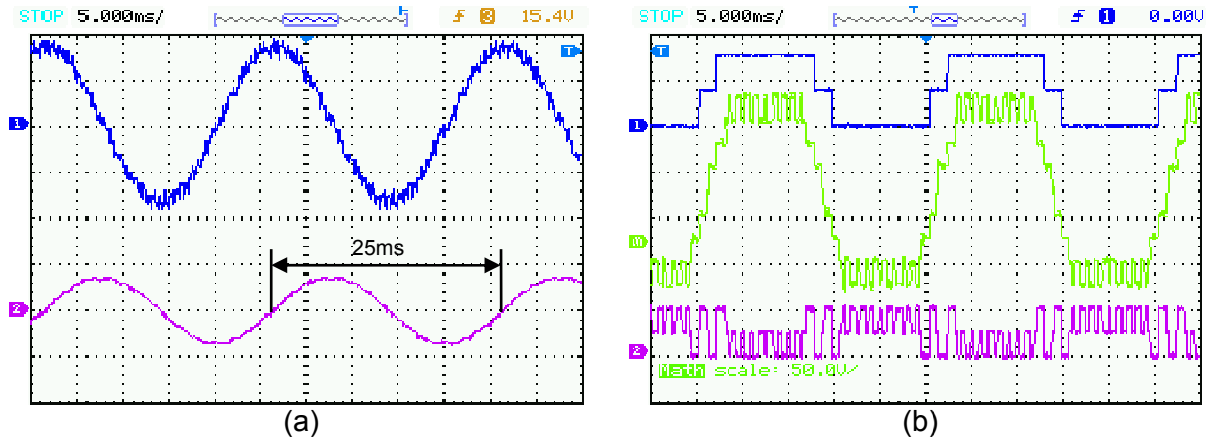



Fig. 7.40: (a) Motor phase-A, voltage $V_{A2A4}$ (upper trace Y-axis: 20V/div) and current $i_{A2A4}$ (lower trace Y-axis: 1A/div) of 9-level inverter fed open-end IM drive at no load
(b) Top trace Y-axis: 100V/div; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace Y-axis: 50V/div; Difference of 3-level inverter-A and inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$), Bottom trace Y-axis: 50V/div; 3-level inverter-B pole voltage ($V_{A4O'}$)
(Experimental result: $m$=0.8; $f^*_m$ =40Hz; 9-level mode)

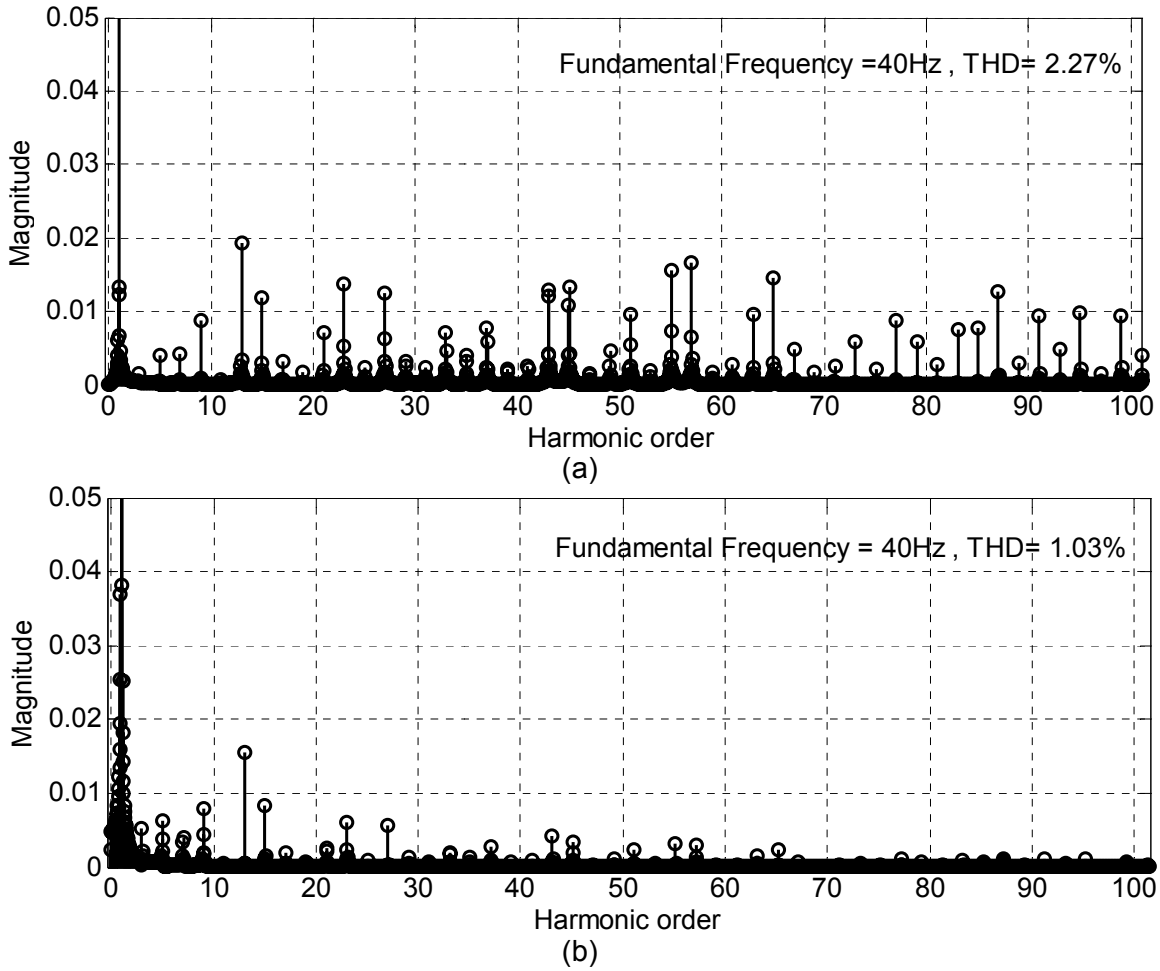
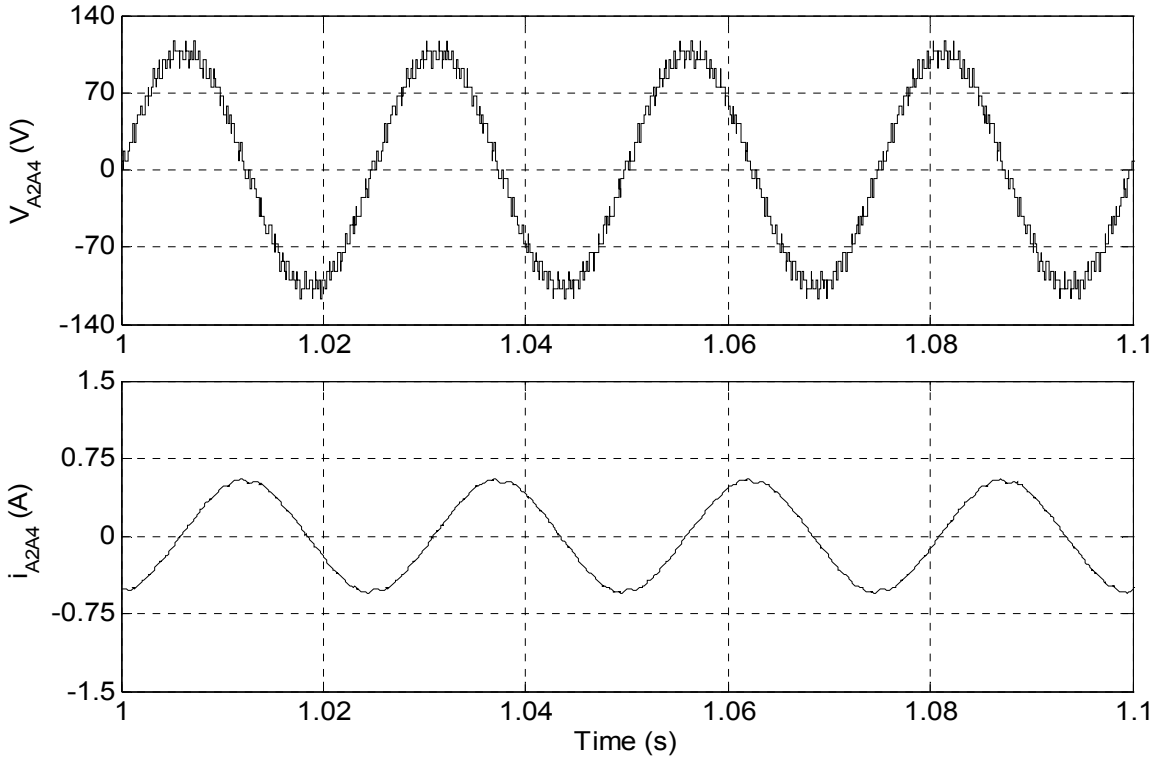
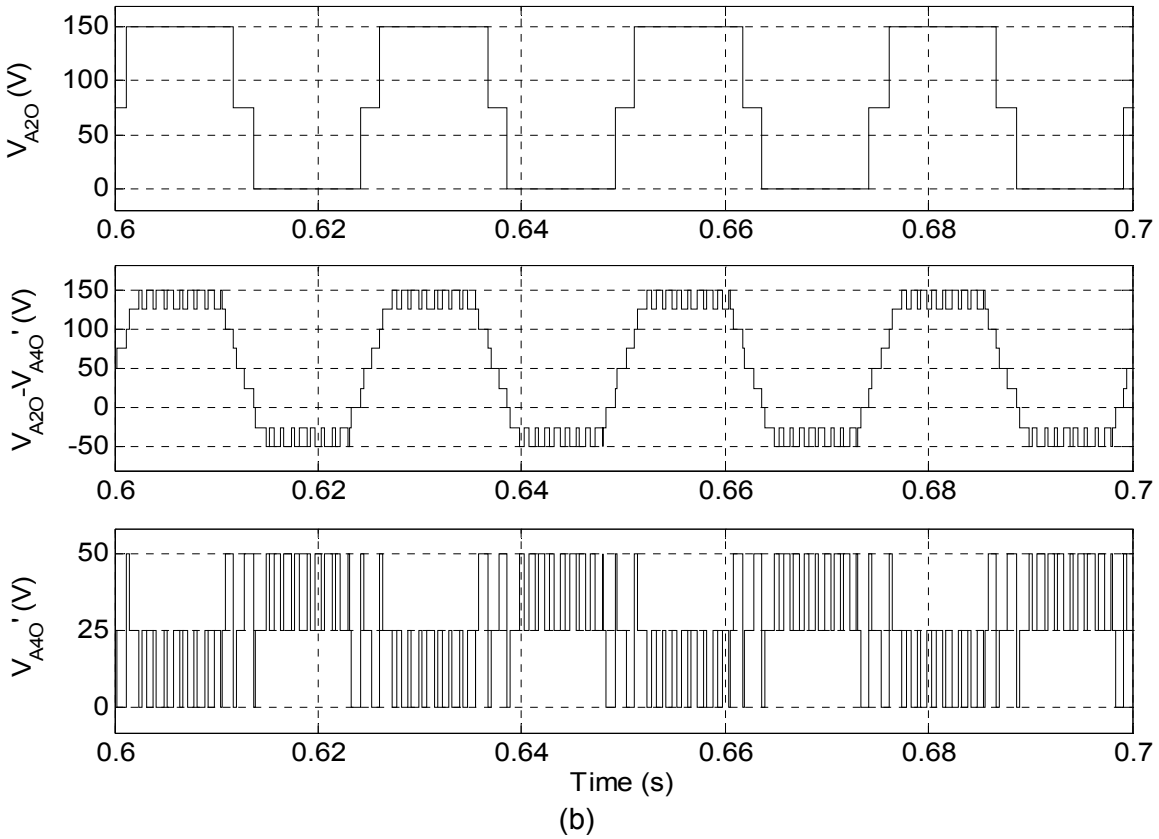



Fig. 7.41: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A2A4}$ (b) Current $i_{A2A4}$
(Experimental result: $m$=0.8; $f^*_m$ =40Hz; 9-level mode)




(a)

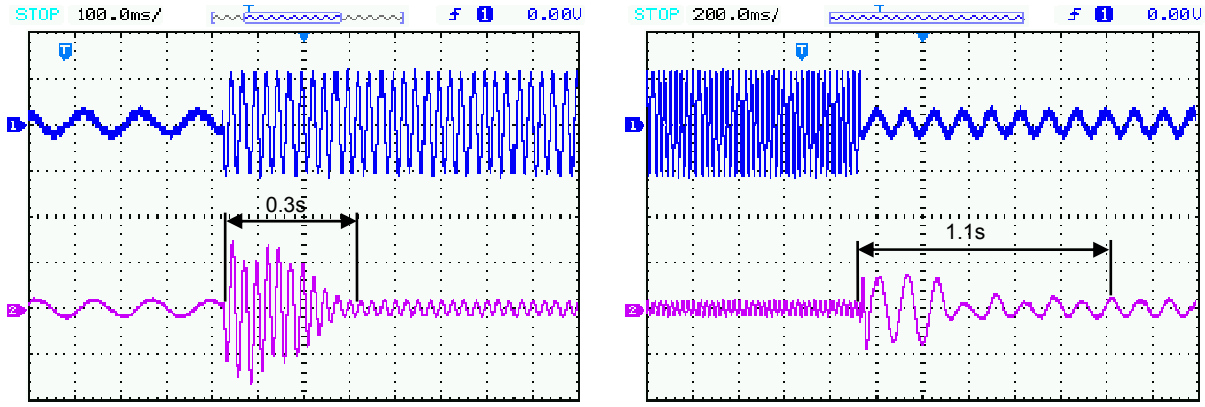



(b)

Fig. 7.42: (a) Motor phase-A, voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) of 9-level inverter fed open-end IM drive at no load
(b) Top trace; 3-level inverter-A pole voltage ($V_{A2O}$), Middle trace; Difference of 3-level inverter-A and inverter-B pole voltages ($V_{A2O}$ - $V_{A4O'}$), Bottom trace; 3-level inverter-B pole voltage ($V_{A4O'}$)
(Simulation result: $m$=0.8; $f^*_m$ =40Hz; 9-level mode)

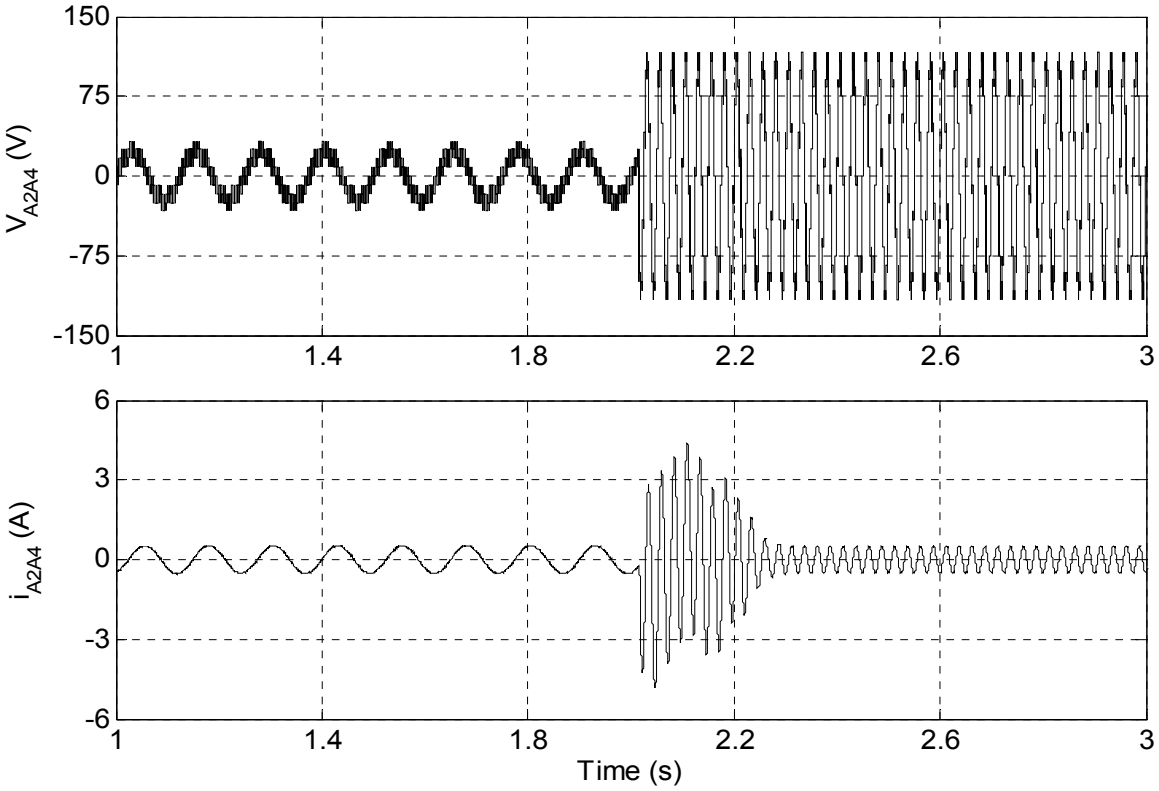
The developed prototype of proposed 9-level inverter is also investigated against transient state stability. The inverter is operated in 3-level mode and when steady state is achieved its mode of operation is sudden change from 3-level to 9-level mode of operation. The value of modulation index ($m$) is selected as 0.16 and 0.8 for 3-level and 9-level operation respectively. The experimentally obtained motor phase-A voltage $V_{A2A4}$ and current $i_{A2A4}$ are shown in Fig. 7.43(a). The simulated waveforms of motor phase-A voltage $V_{A2A4}$ and current $i_{A2A4}$ under same operating condition are presented in Fig. 7.44(a). It can be noticed from phase voltage and current waveforms that changeover from 3-level mode of operation to 9-level mode of operation takes place instantly and drive attains its steady state in 0.3 second in actual and 0.48 second in simulation. The drive is also investigated against changeover from higher to lower level operation i.e., from 9-level to 3-level operation. Fig. 7.43(b) depicts the experimentally obtained phase voltage (upper trace) and current (lower trace) during sudden change in operation from 9-level to 3-level. The simulated waveforms for higher to lower changeover operation are shown in Fig. 7.44(b). In this case also, it can be observed that the drive attains its steady state within few cycles.

The experimentally obtained results under different operating conditions (steady state as well as transient state) are in good agreement with the results obtained in simulations and therefore, the feasibility of proposed 9-level inverter scheme is confirmed.

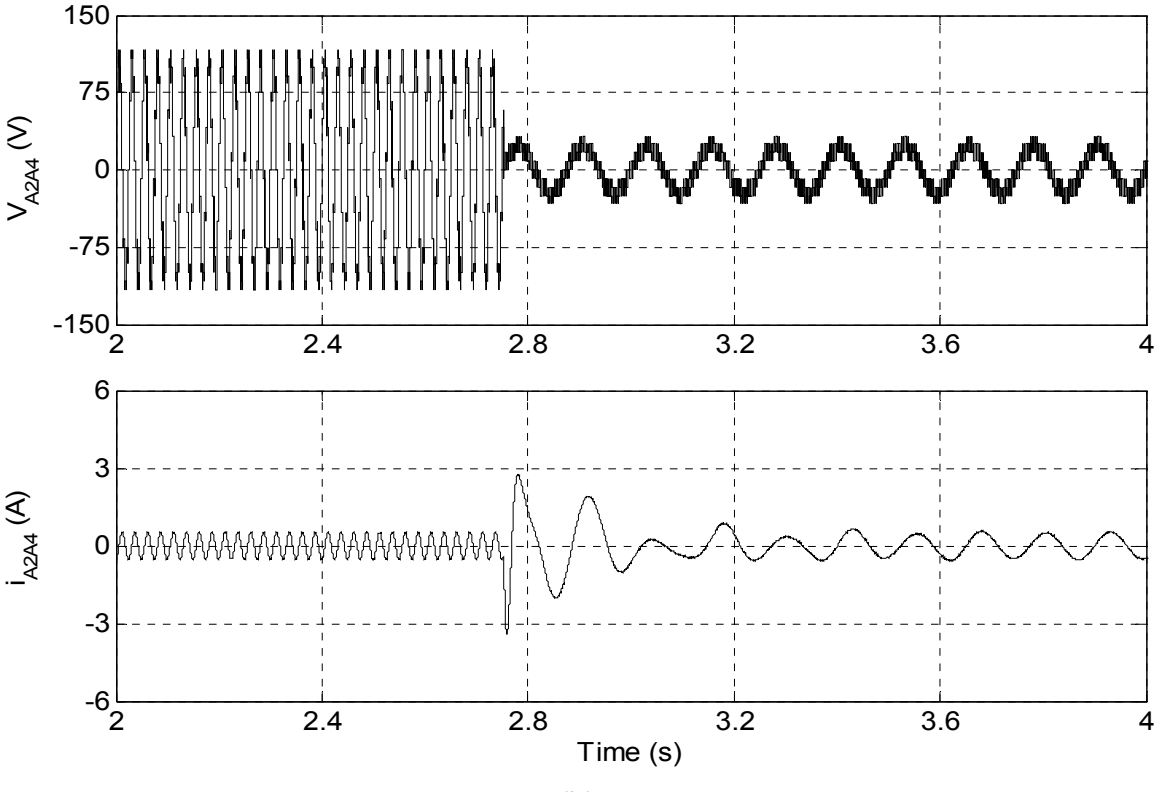



(a) (b)

Fig. 7.43: Motor phase-A voltage $V_{A2A4}$ (upper trace Y-axis: 100V/div) and current $i_{A2A4}$ (lower trace Y-axis: 3A/div) waveforms under sudden change in operation from (a) 3-level to 9-level at no-load (b) 9-level to 3-level at no-load
(Experimental result)




(a)




(b)

Fig. 7.44: (a) Motor phase-A voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) waveforms under sudden change in operation from 3-level to 9-level at no-load
(b) Motor phase-A voltage $V_{A2A4}$ (upper trace) and current $i_{A2A4}$ (lower trace) waveforms under sudden change in operation from 9-level to 3-level at no-load

Table 7.2: Comparison of experimental and downscaled simulation results of proposed 9-level inverter

| Performance parameter | | Modulation index(*m*) | | | | | |
|---|---|---|---|---|---|---|---|
| | | 0.16 | 0.28 | 0.36 | 0.42 | 0.52 | 0.8 |
| Level of operation | Experimental | 3 | 4 | 5 | 6 | 7 | 9 |
| | Simulation | 3 | 4 | 5 | 6 | 7 | 9 |
| RMS of phase-A voltage (*V*) | Experimental | 16.25 | 27.02 | 34.33 | 38.01 | 49.53 | 74.34 |
| | Simulation | 16.95 | 27.11 | 34.43 | 40.01 | 49.41 | 75.73 |
| RMS of phase-A current (*A*) | Experimental | 0.345 | 0.381 | 0.385 | 0.383 | 0.380 | 0.358 |
| | Simulation | 0.345 | 0.385 | 0.39 | 0.391 | 0.397 | 0.399 |
| Frequency of phase voltage (*Hz)* | Experimental | 8 | 14 | 18 | 21 | 26 | 40 |
| | Simulation | 8 | 14 | 18 | 21 | 26 | 40 |
| THD of phase-A voltage in % | Experimental | 40.65 | 6.10 | 5.58 | 3.58 | 3.20 | 2.27 |
| | Simulation | 40.79 | 8.40 | 7.02 | 4.62 | 3.88 | 2.88 |
| Order of dominant voltage harmonic (amplitude in pu) | Experimental | 250±1 (0.2) | 142±2 (0.083) | 111±2 (0.038) | 95±2 (0.045) | 77±2 (0.046) | 45 (0.02) |
| | Simulation | 250±1 (0.22) | 142±2 (0.091) | 111±2 (0.042) | 95±2 (0.046) | 77±2 (0.051) | 45 (0.025) |
| THD of phase-A Current in % | Experimental | 1.66 | 0.31 | 0.47 | 0.34 | 0.24 | 1.03 |
| | Simulation | 2.51 | 0.78 | 0.72 | 0.59 | 0.47 | 1.10 |
| Order of dominant current harmonic (amplitude in pu) | Experimental | 250±1 (0.008) | 142±2 (0.005) | 39 (0.005) | 27 (0.006) | 13 (0.012) | 13 (0.015) |
| | Simulation | 250±1 (0.023) | 142±2 (0.019) | 39 (0.007) | 27 (0.008) | 13 (0.015) | 9 &13 (0.019) |
| Settling time for 3-level to 9-level in sec | Experimental | 0.3 | | | | | |
| | Simulation | 0.48 | | | | | |
| Settling time for 9-level to 3-level in sec | Experimental | 1.1 | | | | | |
| | Simulation | 0.88 | | | | | |
| Sampling time | Experimental | 50 µSecond | | | | | |
| | Simulation | | | | | | |

### 7.3.3 Experimental Validation of Hybrid 9-level Inverter

The developed prototype of hybrid 9-level inverter topology proposed in Chapter-5 has been tested on 1.5kW, 415V, 50Hz, 4pole open-end winding induction motor drive with constant *V/f* control scheme under no-load condition. The switching frequency ($f_c$) is kept constant at 1kHz and DC link voltage ($V_{DC}$) is taken as 200V for experimentation. Two isolated DC link of magnitude 100V ($V_{DC}/2$) for individual inverters are implemented using single phase diode bridge (KBPC3510) rectifier and a 2200μF capacitor is connected at the output of rectifier. The motor used for experimentation having the same parameters as the simulated motor model (Appendix-A). The control strategy describe in sub-section 5.2.3 is implemented on RT-Lab Meta Controller. All the capacitors voltages and currents are sensed and send to RT-Lab Meta Controller via analog input card. The hysteresis band is selected as $\pm$2V means the range of capacitor voltage $V_{CA1}$ varies from 48V to 52V and range of capacitor voltage $V_{CA2}$ is from 23V to 27V. The switching signals for IGBTs are generated using Spartan-3 FPGA board of Opal RT-Lab real time digital simulator. The motor is run at different modulation indices and the value of modulation indices is selected same as the value selected in previous section, to compare the performance of both 9-level inverters. The motor phase-A voltage ($V_{A1A2}$), phase-A current ($i_{A1A2}$), their harmonic spectrums, phase-A capacitors voltages ($V_{CA1}$, $V_{CA2}$), inverters pole-A voltages ($V_{A1O}$, $V_{A2O'}$) and difference of inverters pole-A voltages ($V_{A1O}$ - $V_{A2O'}$) are considered as evaluation criteria. The performance of developed prototype of hybrid 9-level inverter scheme is experimentally investigated under steady-state as well as transient-state conditions. As the experimentation is carried out at reduced voltage, for validating the experimental results, the simulation study at reduced DC link voltage is also carried out under same operating conditions and results are presented.

Fig. 7.45(a) shows the experimentally obtained phase-A voltage (trace-1), current (trace-2), ripple in capacitors voltages $V_{CA1}$ and $V_{CA2}$ (trace-3 and 4) pertaining to 3-level mode of operation, at $m$ =0.16 and $f^*_m$=8Hz. The simulated waveforms are given in Fig. 7.47(a) and Fig. 7.47(b). The capacitors voltages are well balanced and peak to peak ripple is less than 1V. The experimentally obtained pole voltages waveforms shown in Fig. 7.45(b) are exactly same as the simulated pole voltages waveforms shown in Fig. 7.48. It can be seen in pole voltages waveform that 5-level inverter-A operates in 3-level mode and gives the voltage level of 0, 25 and 50 correspond to 0, $V_{DC}/8$ and $2V_{DC}/8$ while the inverter-B is clamped at 100V ($V_{DC}/2$). The difference of pole voltages ($V_{A1O}$ - $V_{A2O'}$) having three distinct voltage levels -100, -75 and -25 confirm the 3-level mode of operation. Normalized harmonic spectrum of phase voltage (trace-1 of Fig. 7.45a) and current (trace-2 of Fig. 7.45a) are shown in Fig. 7.46(a) and Fig. 7.46(b) respectively. The THD of phase voltage is 42.42% and dominant harmonic component occur at the side band of 250$^{th}$ ($2f_c/f^*_m$ = 2*1000/8) order.

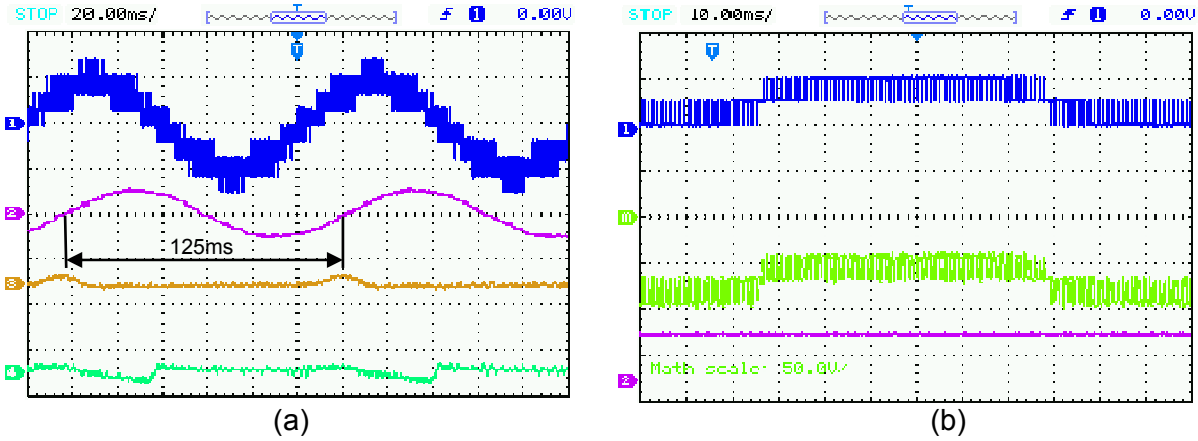



Fig. 7.45: (a) Trace-1: Y-axis= 25V/div; Motor phase-A voltage $V_{A1A2}$ , Trace-2: Y-axis= 1A/div; phase-A current $i_{A1A2}$, Trace-3: Y-axis=2V/div; Ripple in capacitor voltage $V_{CA1}$, Trace-4: Y-axis=2V/div; Ripple in capacitor voltage $V_{CA2}$
(b) Top trace Y-axis: 50V/div; 5-level inverter-A pole voltage ($V_{A1O}$), Middle trace Y-axis: 50V/div; Difference of inverter-A and inverter-B pole voltages ($V_{A1O}$ - $V_{A2O'}$), Bottom trace Y-axis: 100V/div; 2-level inverter-B pole voltage ($V_{A2O'}$)
(Experimental result: $m$=0.16; $f^*_m$ =8Hz; 3-level mode)

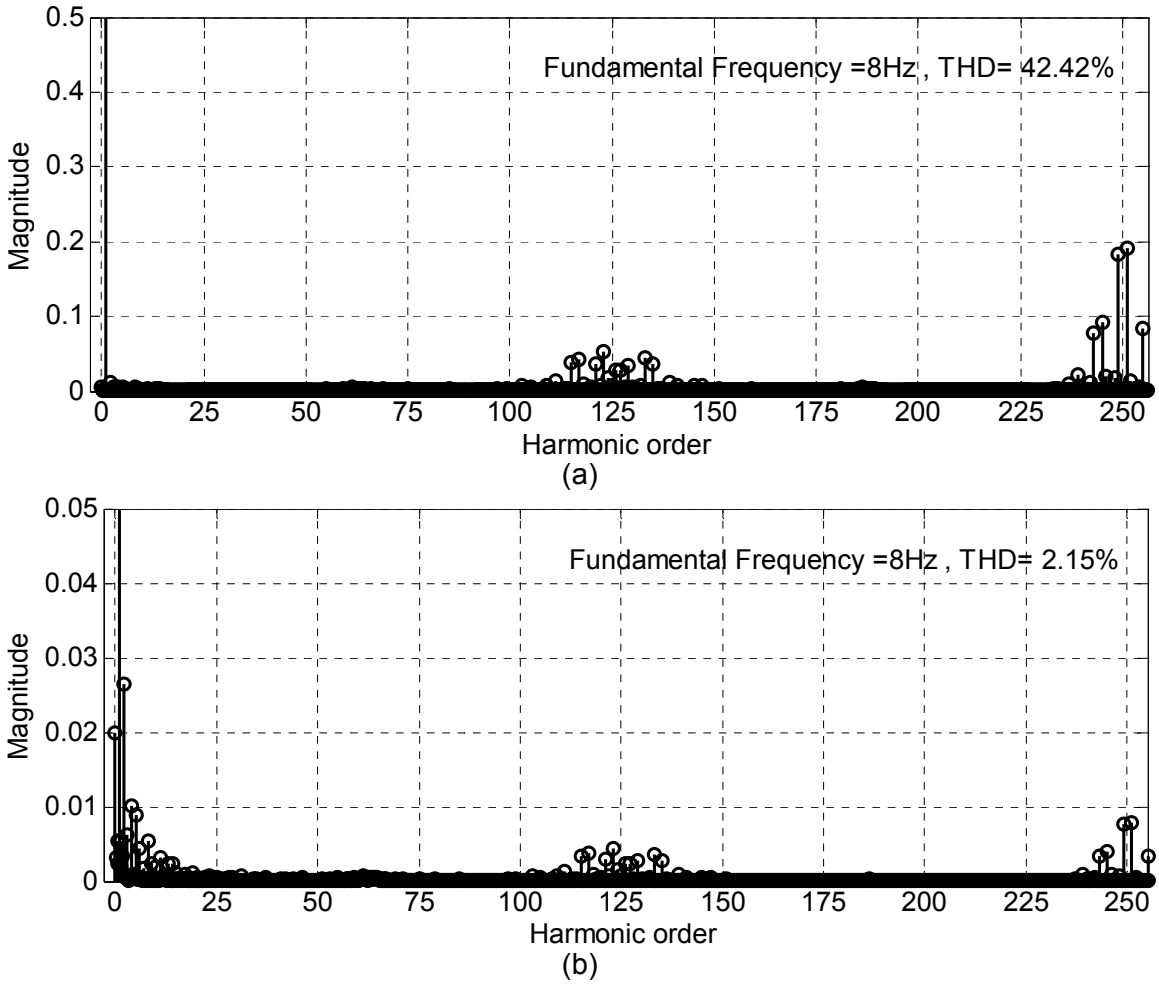
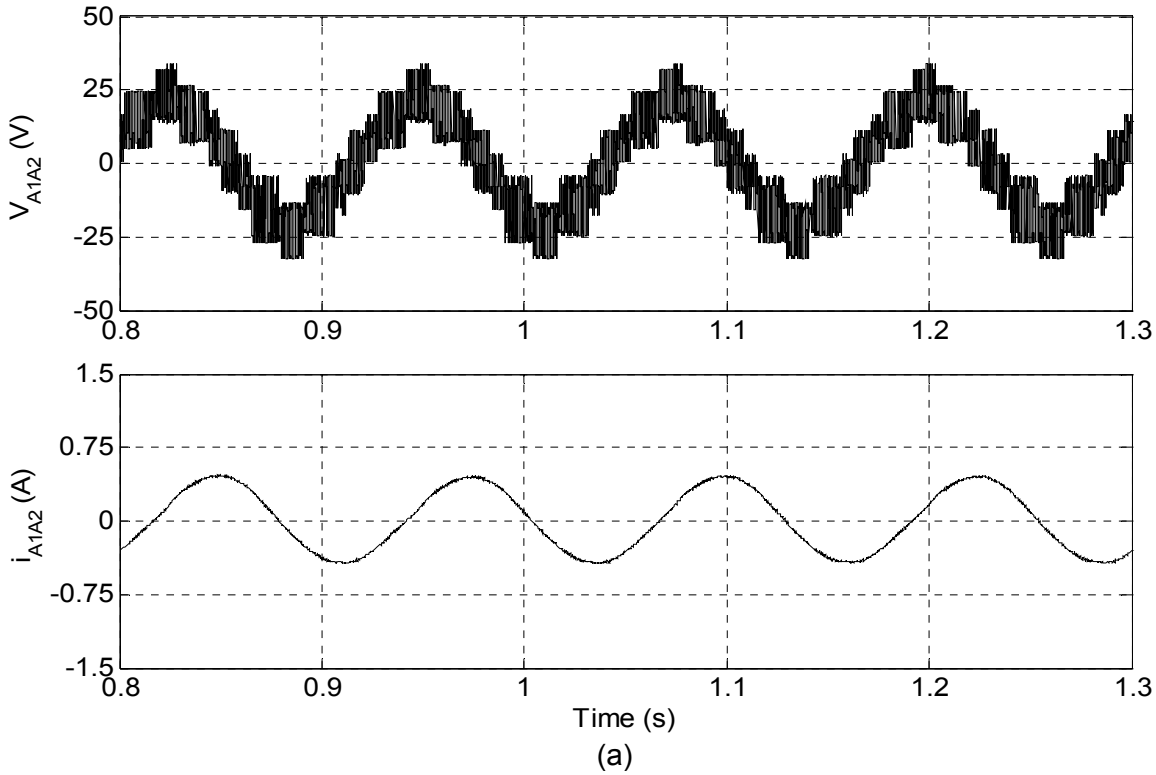
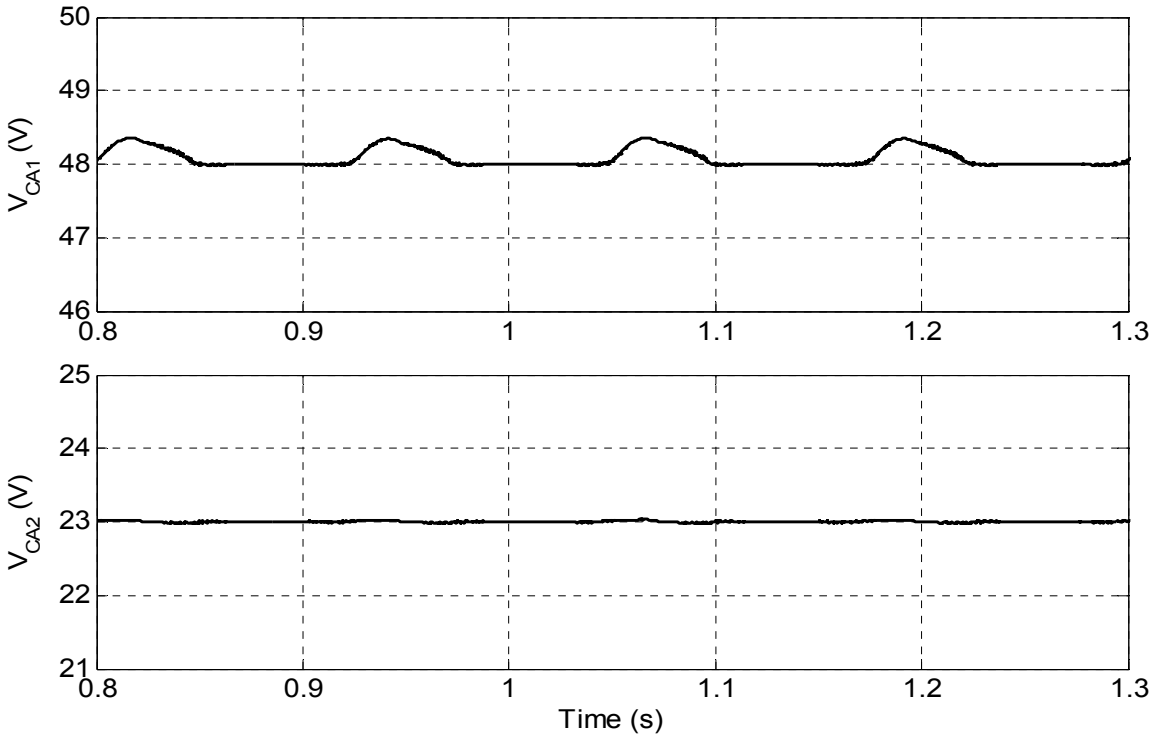



Fig. 7.46: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A1A2}$ (b) Current $i_{A1A2}$
(Experimental result: $m$=0.16; $f^*_m$ =8Hz; 3-level mode)




(a)




(b)

Fig. 7.47: (a) Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A2A4}$ (lower trace)
(b) Capacitors voltages $V_{CA1}$ (upper trace) and $V_{CA2}$ (lower trace)
(Simulation result: $m$=0.16; $f^*_m$ =8Hz; 3-level mode)

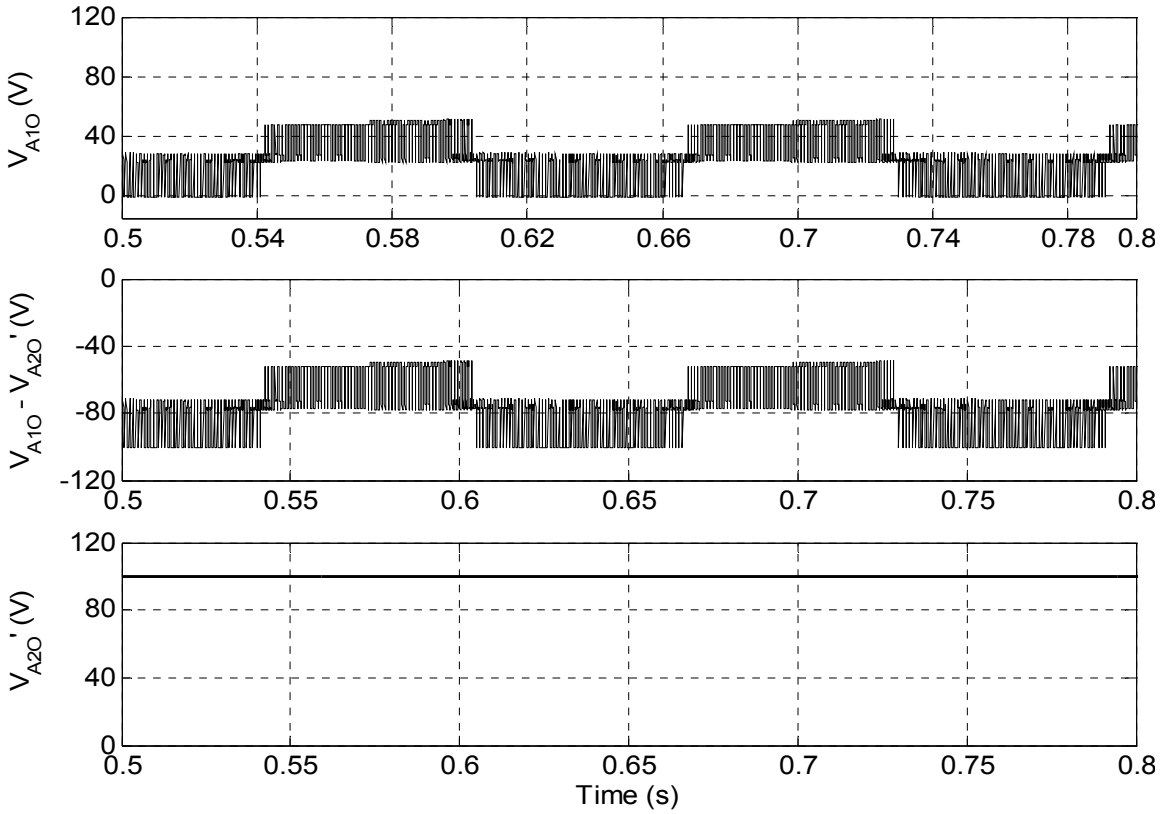



Fig. 7.48: Top trace; 5-level inverter-A pole voltage ($V_{A1O}$), Middle trace; Difference of inverter-A and inverter-B pole voltages ($V_{A1O}$ - $V_{A2O'}$), Bottom trace; 2-level inverter-B pole voltage ($V_{A2O'}$)
(Simulation result: $m$=0.16; $f^*_m$ =8Hz; 3-level mode)

Another set of experimental and simulation result obtained when motor is operated at modulation index $m$=0.28 and fundamental frequency ($f^*_m$) of 14Hz. At this modulation index inverter operates in 4-level inversion mode of operation. The experimentally obtained waveforms of phase-A voltage ($V_{A1A2}$), current ($i_{A1A2}$), ripple in capacitors voltages $V_{CA1}$ and $V_{CA2}$ are shown in Fig. 7.49(a). The waveforms are in the same order as they were in previous set of results. The simulated waveforms are shown in Fig. 7.51 and Fig. 7.52. It can be observed from pole voltages waveforms that difference of pole voltage ($V_{A1O}$ - $V_{A2O'}$) possess four distinct levels -100, -75, -50 and -25 correspond to -$V_{DC}$/2, -(3/8)$V_{DC}$, -(1/4)$V_{DC}$ and -(1/8)$V_{DC}$. It is also evident from pole voltages waveforms that in 4-level inversion mode 5-level inverter-A operates in 4-level mode and gives the voltage level of 0, 75, 150 and 225 (0, $V_{DC}$/8, $V_{DC}$/4 and 3$V_{DC}$/8) while the inverter-B is still clamped at 300V ($V_{DC}$/2). The THD of experimentally obtained phase voltage and current are 12.35% and 2.19% as depicted in their normalized harmonic spectrum shown in Fig. 7.50. The dominant harmonic component of phase voltage approximately occur at the side band of 143$^{rd}$ ($2f_c/f^*_m$ = 2*1000/14). The capacitors voltages $V_{CA1}$ and $V_{CA2}$ are well balanced and peak to peak ripple in capacitor voltage is less then 1V (Fig. 7.49a and Fig. 7.51b).

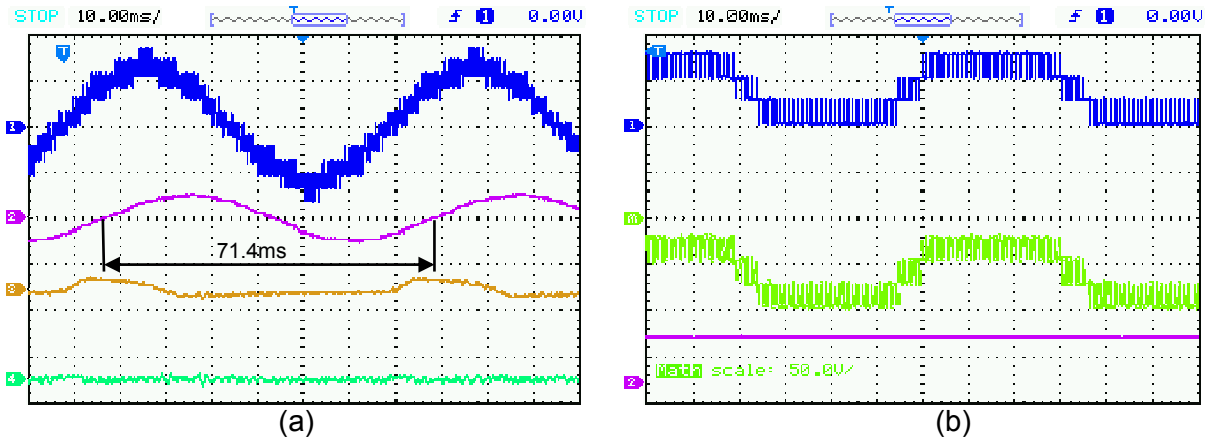



Fig. 7.49: (a) Trace-1: Y-axis= 30V/div; Motor phase-A voltage $V_{A1A2}$, Trace-2: Y-axis= 1A/div; phase-A current $i_{A1A2}$, Trace-3: Y-axis=2V/div; Ripple in capacitor voltage $V_{CA1}$, Trace-4: Y-axis=2V/div; Ripple in capacitor voltage $V_{CA2}$
(b) Top trace Y-axis: 50V/div; 5-level inverter-A pole voltage ($V_{A1O}$), Middle trace Y-axis: 50V/div; Difference of inverter-A and inverter-B pole voltages ($V_{A1O}$ - $V_{A2O'}$), Bottom trace Y-axis: 100V/div; 2-level inverter-B pole voltage ($V_{A2O'}$)
(Experimental result: $m$=0.28; $f^*_m$ =14Hz; 4-level mode)

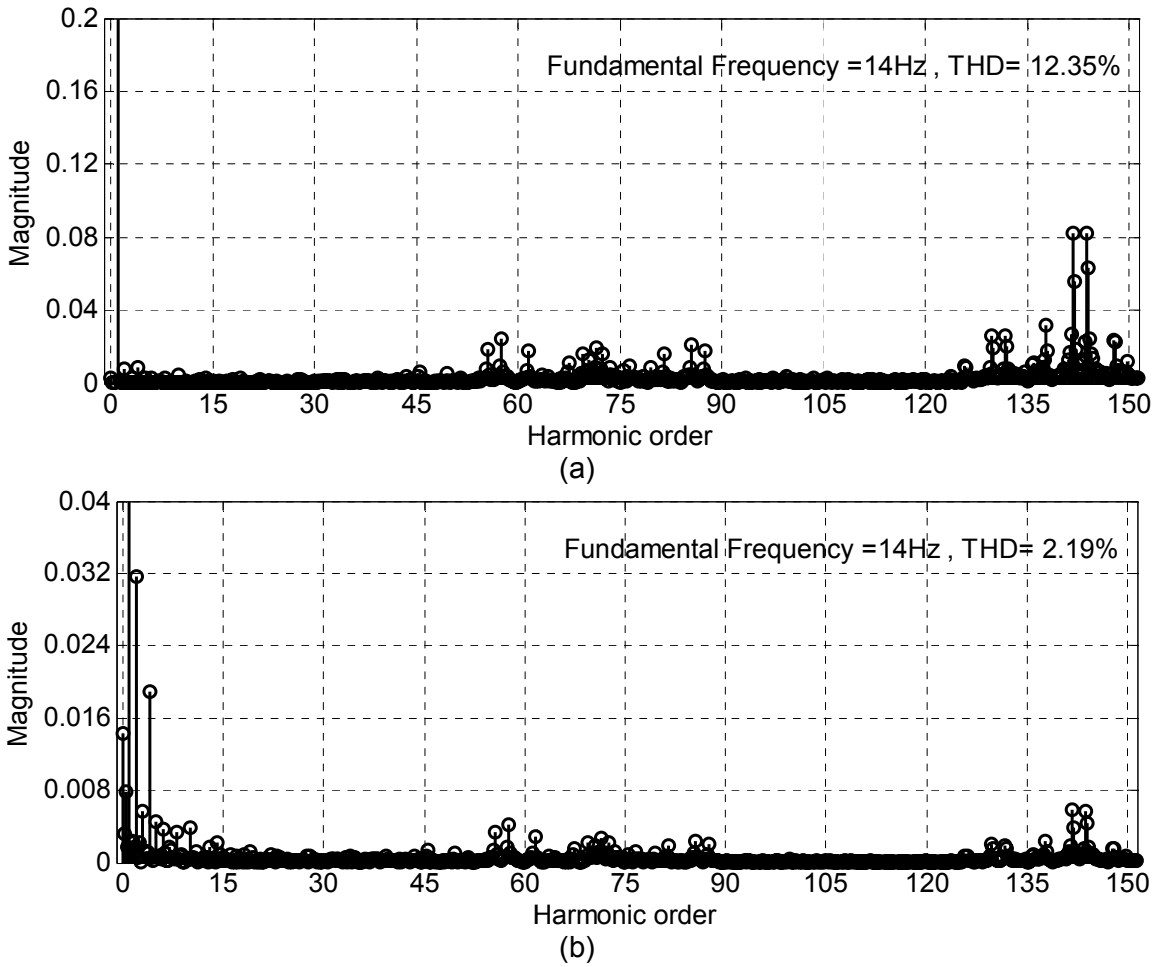
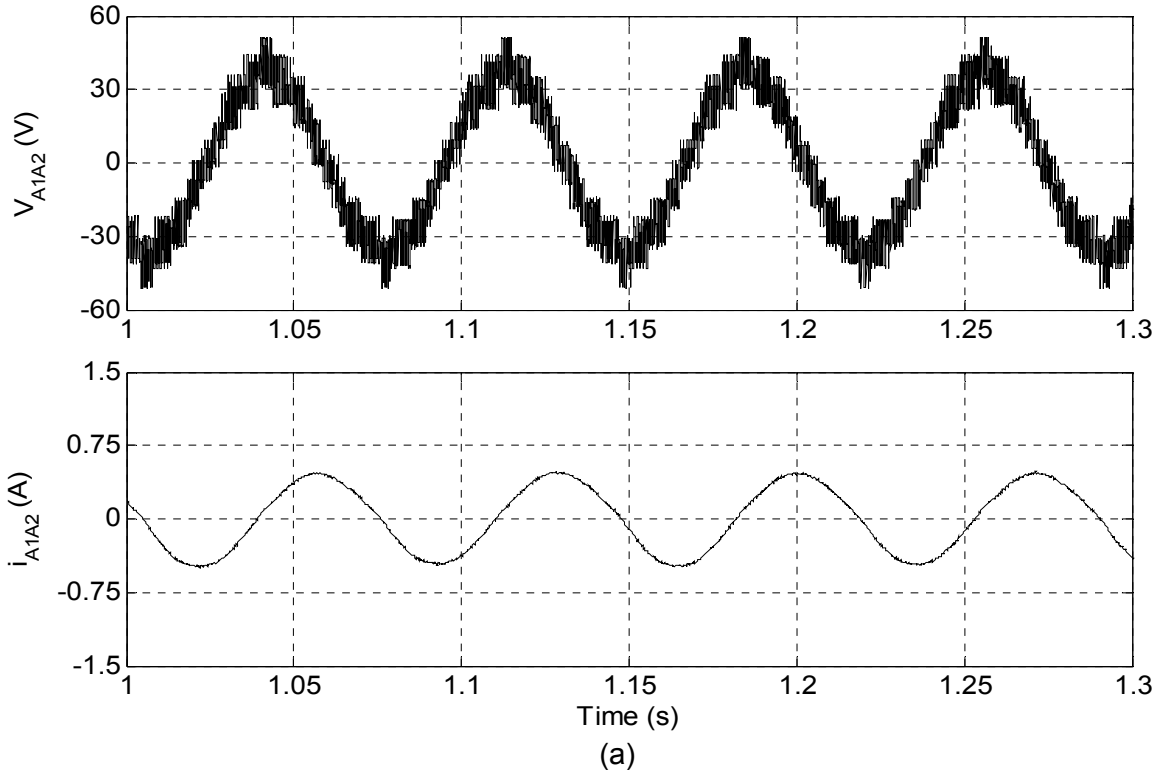
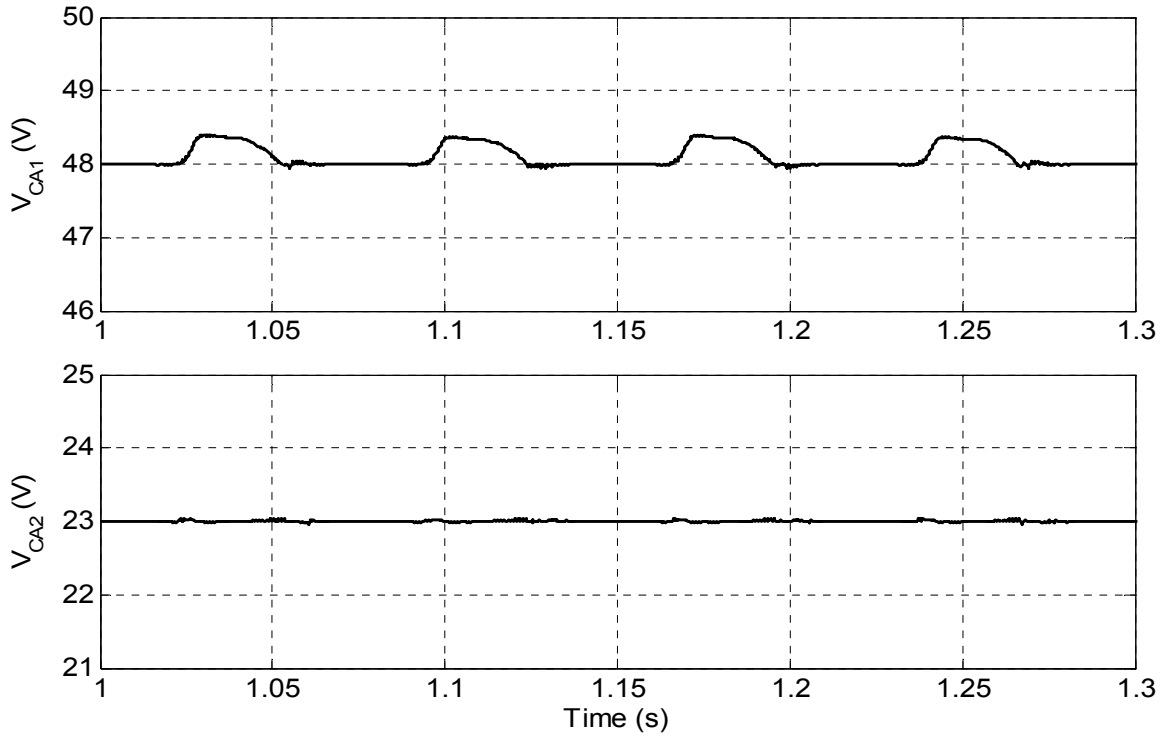



Fig. 7.50: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A1A2}$ (b) Current $i_{A1A2}$
(Experimental result: $m$=0.28; $f^*_m$ =14Hz; 4-level mode)




(a)




(b)

Fig. 7.51: (a) Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A2A4}$ (lower trace)
(b) Capacitors voltages $V_{CA1}$ (upper trace) and $V_{CA2}$ (lower trace)
(Simulation result: $m$=0.28; $f^*_m$ =14Hz; 4-level mode)

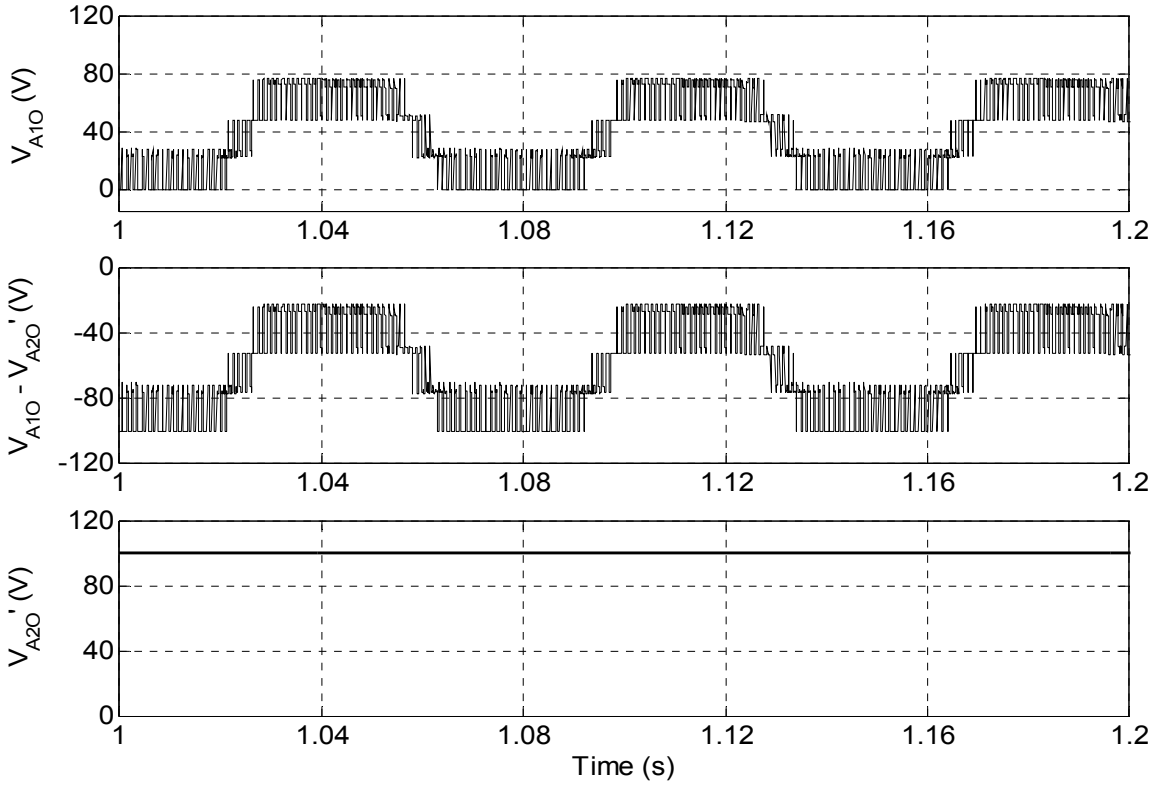



Fig. 7.52: Top trace; 5-level inverter-A pole voltage ($V_{A1O}$), Middle trace; Difference of inverter-A and inverter-B pole voltages ($V_{A1O}$ - $V_{A2O'}$), Bottom trace; 2-level inverter-B pole voltage ($V_{A2O'}$)
(Simulation result: $m$=0.28; $f^*_m$ =14Hz; 4-level mode)

The performance of the developed prototype inverter under 5-level mode of operation at modulation index of 0.36 is shown in Fig. 7.53 and Fig. 7.54. The fundamental frequency of inverter output voltage is 18Hz. The simulation results under same operating condition are shown in Fig. 7.55 and Fig. 7.56. The simulation and experimenter results are almost matching to each other. The capacitor voltages are effectively balanced with peak to peak ripple is less than 1V (Fig. 7.53a; experimental and Fig. 7.55b; simulated). It can be observed from pole voltages waveform (Fig. 7.53b; experimental and Fig. 7.56; simulated) that 5-level inverter-A operates in 5-level mode and pole voltage $V_{A1O}$ attains five distinct voltage levels whereas two-level inverter-B clamped at 100V ($V_{DC}$/2). The five levels realised in difference of pole voltages ($V_{A1O}$ - $V_{A2O'}$) are -100, -75, -50, -25 and 0 as shown in middle trace of Fig. 7.53(b) (experimental) and Fig. 7.56 (simulated). The normalized harmonic spectrum of motor phase voltage and current (trace-1 and trace-2 of Fig. 7.53a) are analyzed using FFT and presented in Fig. 7.54(a) and Fig. 7.54(b) respectively. It can be observed in the spectrum of phase voltage that lower order harmonics are absent. The THD of phase voltage is found 7.12% and dominant harmonic component occur at the side band of $111^{th}$ ($2f_c/f^*_m$ = 2*1000/18) order whereas THD of phase current is 2.11% with the presence of lower order harmonics.

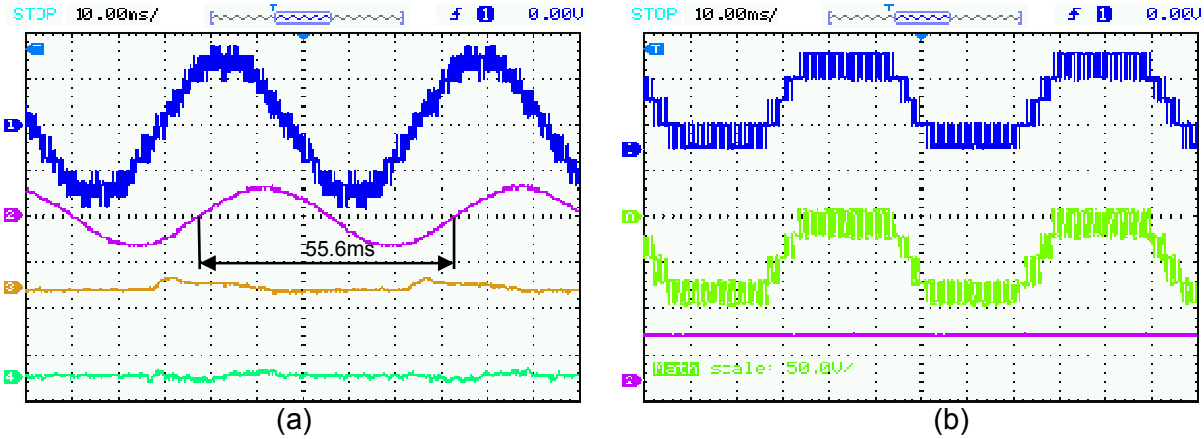



Fig. 7.53: (a) Trace-1: Y-axis= 35V/div; Motor phase-A voltage $V_{A1A2}$, Trace-2: Y-axis= 1A/div; phase-A current $i_{A1A2}$, Trace-3: Y-axis=2V/div; Ripple in capacitor voltage $V_{CA1}$, Trace-4: Y-axis=2V/div; Ripple in capacitor voltage $V_{CA2}$
(b) Top trace Y-axis: 50V/div; 5-level inverter-A pole voltage ($V_{A1O}$), Middle trace Y-axis: 50V/div; Difference of inverter-A and inverter-B pole voltages ($V_{A1O}$ - $V_{A2O'}$), Bottom trace Y-axis: 100V/div; 2-level inverter-B pole voltage ($V_{A2O'}$)
(Experimental result: $m$=0.36; $f^*_m$ =18Hz; 5-level mode)

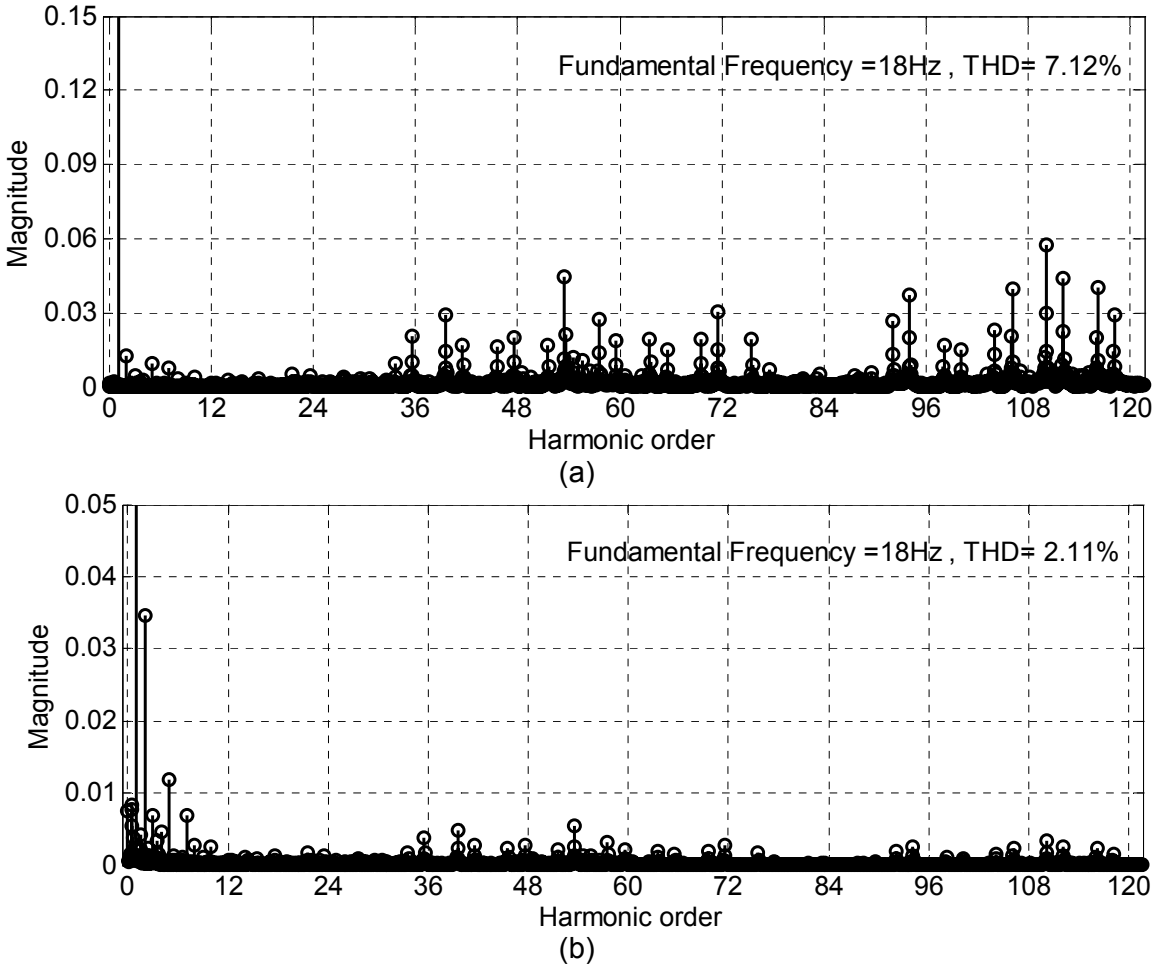
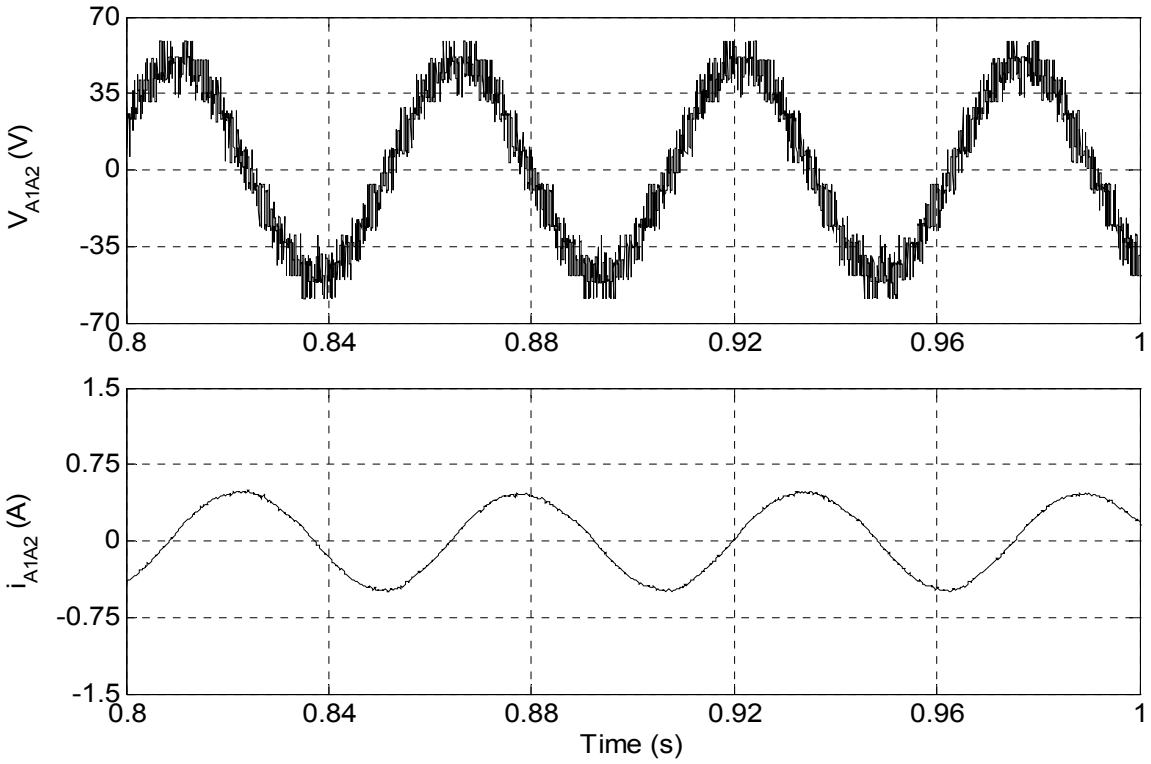
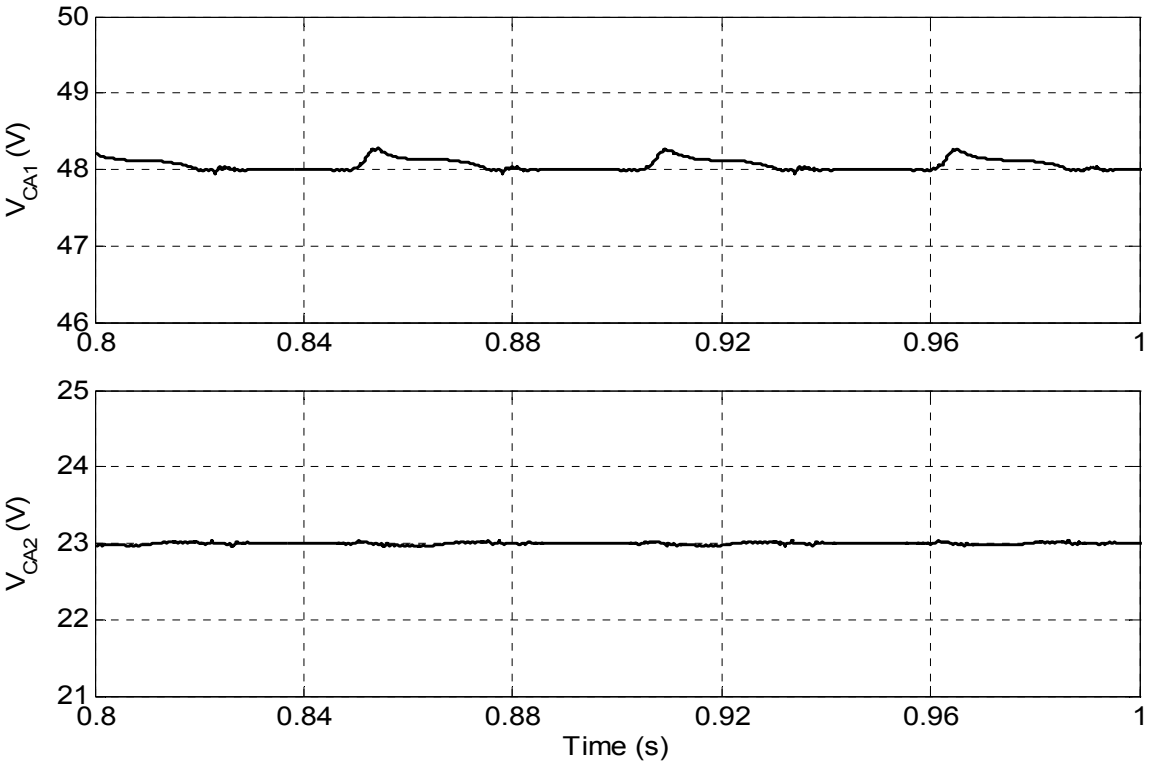



Fig. 7.54: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A1A2}$ (b) Current $i_{A1A2}$
(Experimental result: $m$=0.36; $f^*_m$ =18Hz; 5-level mode)




(a)




(b)

Fig. 7.55: (a) Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A2A4}$ (lower trace)
(b) Capacitors voltages $V_{CA1}$ (upper trace) and $V_{CA2}$ (lower trace)
(Simulation result: $m$=0.36; $f^*_m$ =18Hz; 5-level mode)

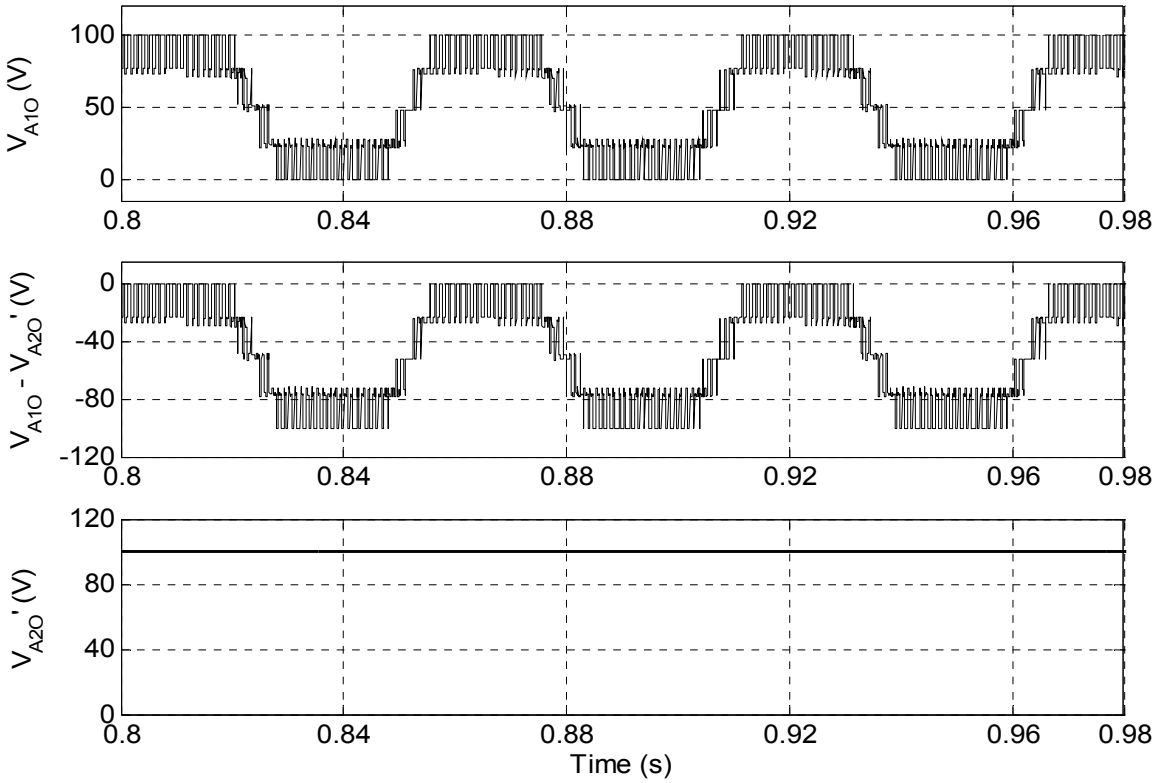



Fig. 7.56: Top trace; 5-level inverter-A pole voltage ($V_{A1O}$), Middle trace; Difference of inverter-A and inverter-B pole voltages ($V_{A1O}$ - $V_{A2O'}$), Bottom trace; 2-level inverter-B pole voltage ($V_{A2O'}$)
(Simulation result: $m$=0.36; $f^*_m$ =18Hz; 5-level mode)

Fig. 7.57 through Fig. 7.60 illustrates the performance of inverter under 6-level mode of operation at modulation index $m$=0.42 (fundamental frequency $f^*_m$=21). In this case also the experimentally obtained waveforms of phase-A voltage (trace-1), current (trace-2), ripple in capacitors voltages $V_{CA1}$ and $V_{CA2}$ (trace-3 and 4) shown in Fig. 7.57(a) are similar to the one obtained by simulation waveforms as shown in Fig. 7.59 and Fig. 7.60. It can be observed from experimental (Fig. 7.57b) and simulated (Fig. 7.60) pole voltage waveforms that inverter-A pole voltage ($V_{A1O}$) having five distinct voltage levels as 0, 25, 50, 75 and 100 correspond to 0, $V_{DC}$/8, $V_{DC}$/4, 3$V_{DC}$/8 and $V_{DC}$/2 whereas two-level inverter-B started to operate in two-level mode only for half of the duration of fundamental cycle and for remaining half cycle it is still clamped at 100V ($V_{DC}$/2). The six levels realised in this mode are -100, -75, -50, -25, 0 and +25 correspond to -$V_{DC}$/2, -3$V_{DC}$ /8, -$V_{DC}$/4, -$V_{DC}$/8, 0 and +$V_{DC}$/8 as depicted in difference of pole voltage waveform (middle trace of Fig. 7.57b; experimental and Fig. 7.60; simulated). The normalized harmonic spectrum of experimentally obtained phase voltage and current are further improved and position of occurrence of dominant harmonic component of phase voltage is at the side band of 96$^{th}$ ($2f_c/f^*_m$ = 2*1000/21) order. The THD of phase voltage (Fig. 7.58a) and current (Fig. 7.58b) are found 5.30% and 2.74% respectively.

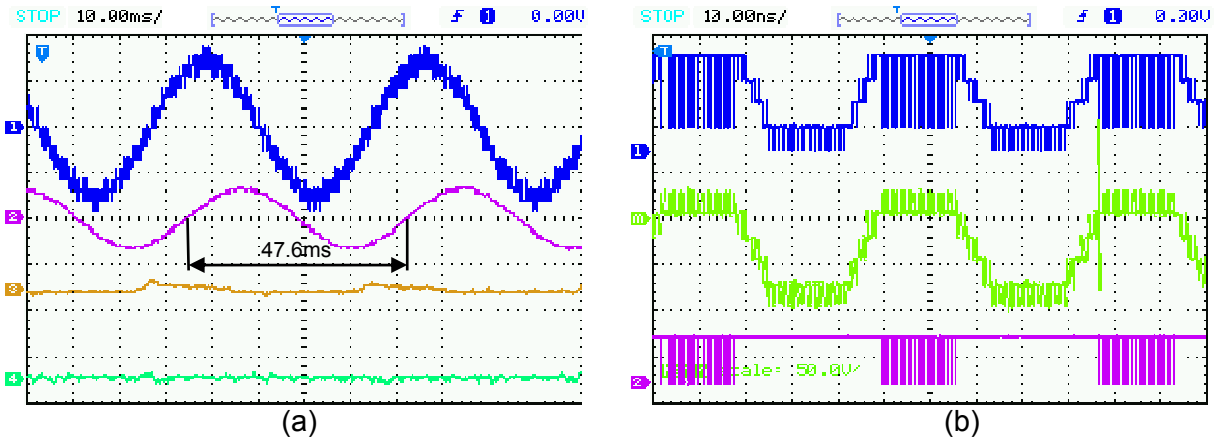



Fig. 7.57: (a) Trace-1: Y-axis= 40V/div; Motor phase-A voltage $V_{A1A2}$, Trace-2: Y-axis= 1A/div; phase-A current $i_{A1A2}$, Trace-3: Y-axis=2V/div; Ripple in capacitor voltage $V_{CA1}$, Trace-4: Y-axis=2V/div; Ripple in capacitor voltage $V_{CA2}$
(b) Top trace Y-axis: 50V/div; 5-level inverter-A pole voltage ($V_{A1O}$), Middle trace Y-axis: 50V/div; Difference of inverter-A and inverter-B pole voltages ($V_{A1O}$ - $V_{A2O'}$), Bottom trace Y-axis: 100V/div; 2-level inverter-B pole voltage ($V_{A2O'}$)
(Experimental result: $m$=0.42; $f^*_m$ =21Hz; 6-level mode)

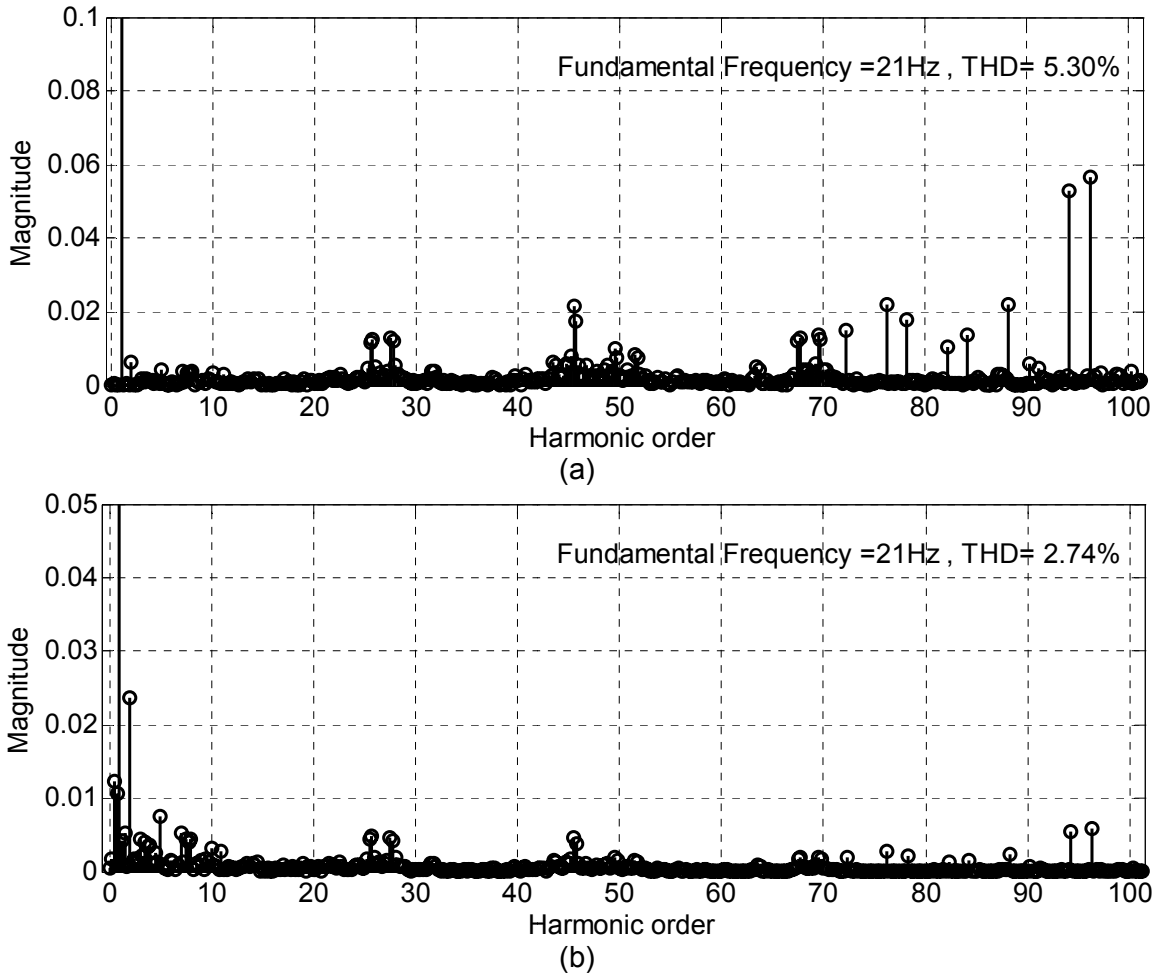



Fig. 7.58: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A1A2}$ (b) Current $i_{A1A2}$
(Experimental result: $m$=0.42; $f^*_m$ =21Hz; 6-level mode)

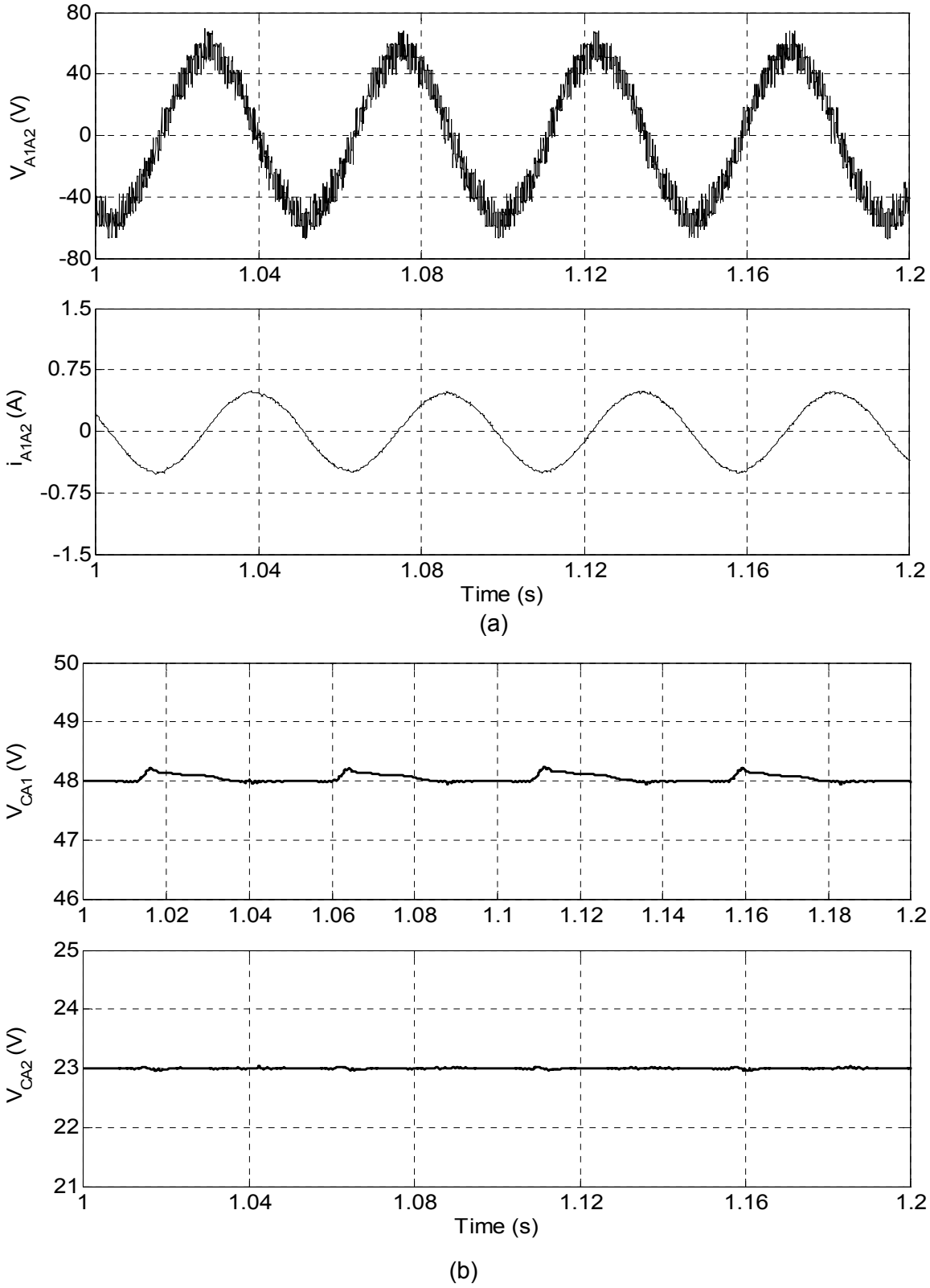



Fig. 7.59: (a) Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A2A4}$ (lower trace)
(b) Capacitors voltages $V_{CA1}$ (upper trace) and $V_{CA2}$ (lower trace)
(Simulation result: $m$=0.42; $f^*_m$ =21Hz; 6-level mode)

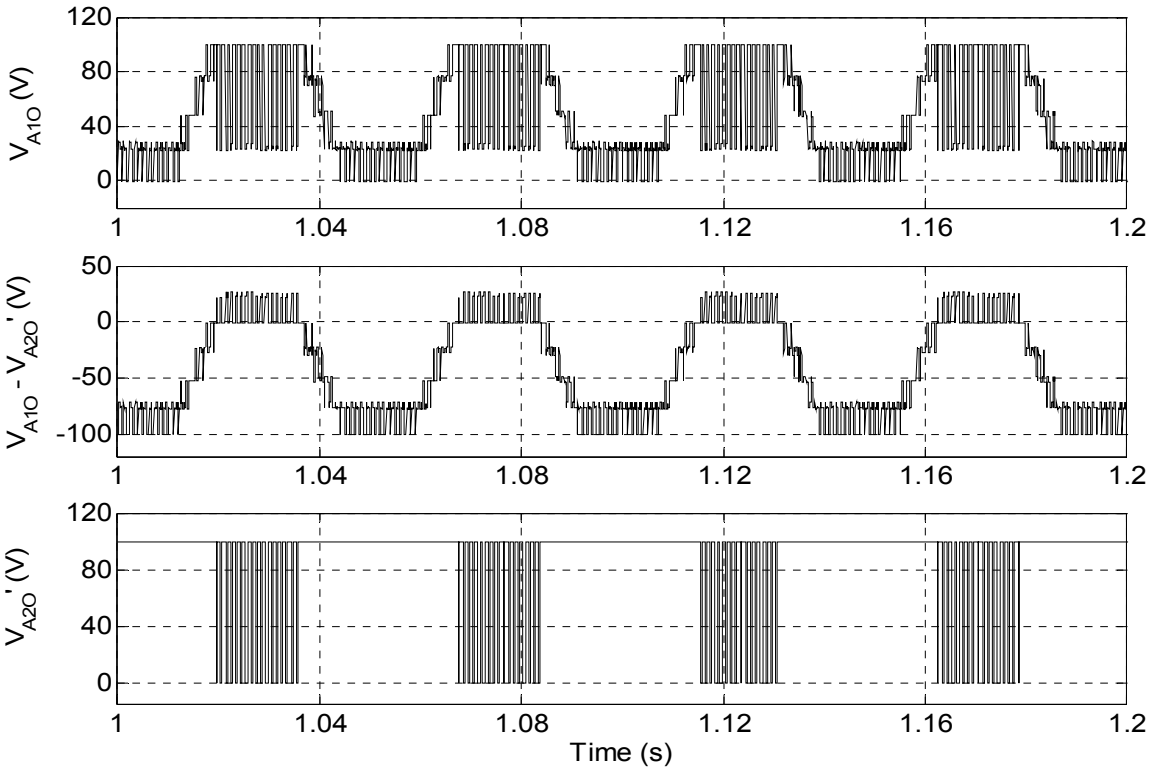



Fig. 7.60: Top trace; 5-level inverter-A pole voltage ($V_{A1O}$), Middle trace; Difference of inverter-A and inverter-B pole voltages ($V_{A1O}$ - $V_{A2O'}$), Bottom trace; 2-level inverter-B pole voltage ($V_{A2O'}$) (Simulation result: $m$=0.42; $f^*_m$ =21Hz; 6-level mode)

The waveforms given in Fig. 7.61 and Fig. 7.62 depict the performance under 7-level mode of operation of the prototype inverter, at modulation index $m$=0.52 and fundamental frequency ($f^*_m$) of 26Hz. The waveforms are in same order as the previous set of results. The simulated phase voltage and current are shown in Fig. 7.63(a). The capacitors voltages ($V_{CA1}$, $V_{CA2}$) and pole voltages ($V_{A1O,}$ $V_{A2O'}$) obtained in simulation are presented in Fig. 7.63(b) and Fig. 7.64 respectively. It may be observed from pole voltages waveforms (Fig. 7.61b; experimental and Fig. 7.64; simulated) that the inverter which operates at higher DC link voltage switch less hence low switching frequency rating power semiconductor devices can be used for two-level inverter-B. The seven distinct voltage levels obtain in this mode are -100, -75, -50, -25, 0, +25 and +50 correspond to -$V_{DC}$/2, -3$V_{DC}$ /8, -$V_{DC}$/4, -$V_{DC}$/8, 0, +$V_{DC}$/8 and +$V_{DC}$/4 as depicted in difference of pole voltage ($V_{A1O}$ - $V_{A2O'}$) waveform (middle trace of Fig. 7.61b; experimental and Fig. 7.64; simulated). The capacitors voltages $V_{CA1}$ and $V_{CA2}$ (trace-3, 4 of Fig. 7.61a; experimental and Fig. 7.63b; simulated) are maintained at desired level (50V for $C_{A1}$ and 25V for $C_{A2}$) with the allowable ripple of $\pm$2V. The normalized harmonic spectrum of phase voltage and current are shown in Fig. 7.62(a) and Fig. 7.62(b) respectively. The occurrence of dominant harmonic component in the spectrum of phase voltage is in same pattern as in the previous cases and it is found that lower order harmonics are increased in phase current. The experimentally obtained results are in good agreement with the results obtained in simulation in this case also.

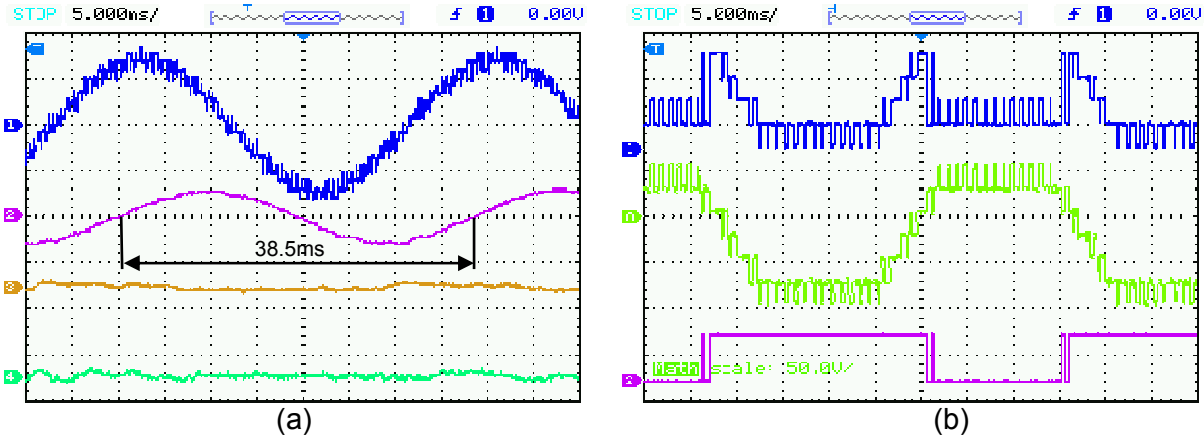



Fig. 7.61: (a) Trace-1: Y-axis= 50V/div; Motor phase-A voltage $V_{A1A2}$, Trace-2: Y-axis= 1A/div; phase-A current $i_{A1A2}$, Trace-3: Y-axis=2V/div; Ripple in capacitor voltage $V_{CA1}$, Trace-4: Y-axis=2V/div; Ripple in capacitor voltage $V_{CA2}$
(b) Top trace Y-axis: 50V/div; 5-level inverter-A pole voltage ($V_{A1O}$), Middle trace Y-axis: 50V/div; Difference of inverter-A and inverter-B pole voltages ($V_{A1O}$ - $V_{A2O'}$), Bottom trace Y-axis: 50V/div; 2-level inverter-B pole voltage ($V_{A2O'}$)
(Experimental result: $m$=0.52; $f^*_m$ =26Hz; 7-level mode)

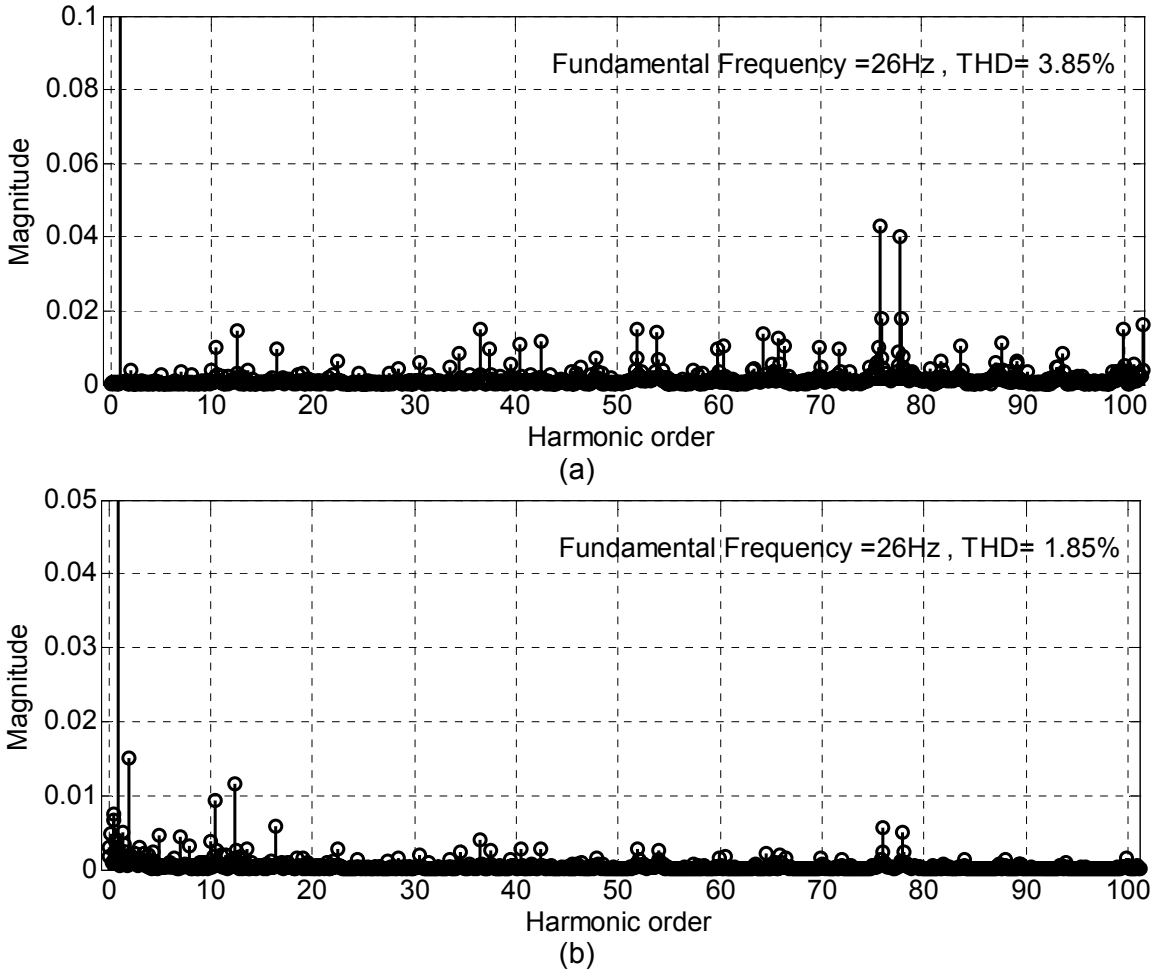
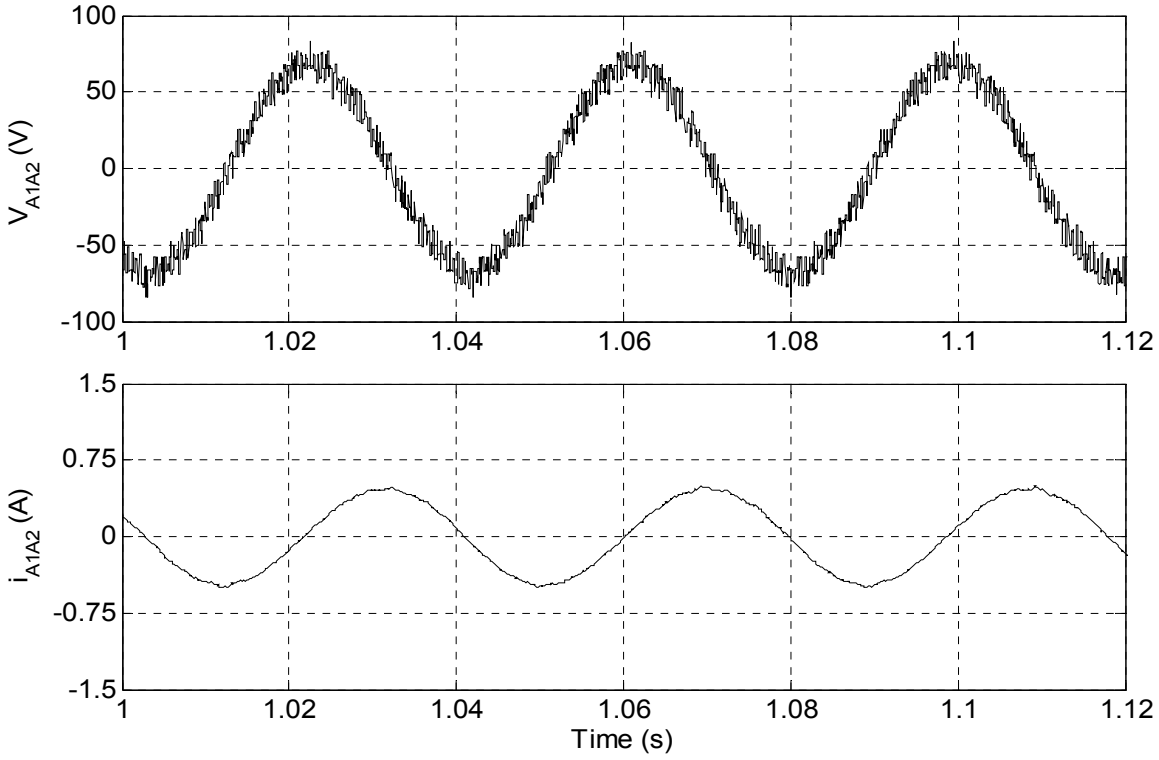
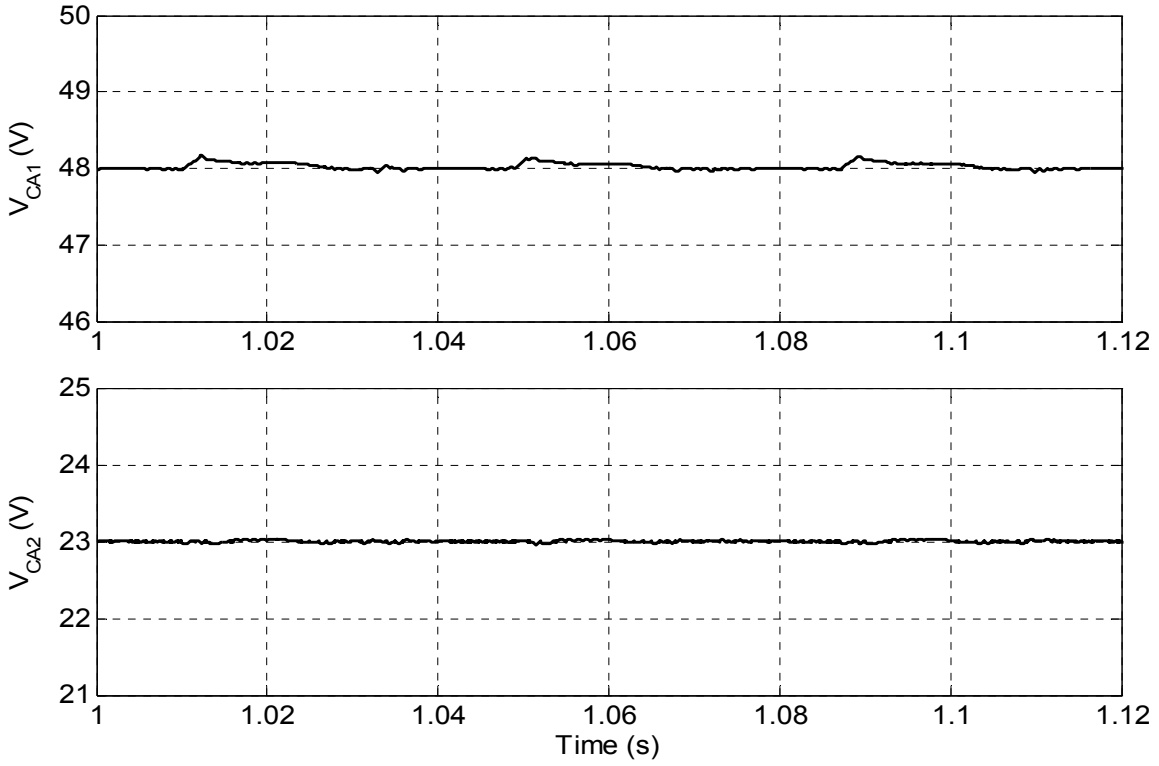



Fig. 7.62: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A1A2}$ (b) Current $i_{A1A2}$
(Experimental result: $m$=0.52; $f^*_m$ =26Hz; 7-level mode)




(a)




(b)

Fig. 7.63: (a) Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A2A4}$ (lower trace)
(b) Capacitors voltages $V_{CA1}$ (upper trace) and $V_{CA2}$ (lower trace)
(Simulation result: $m$=0.52; $f^*_m$ =26Hz; 7-level mode)

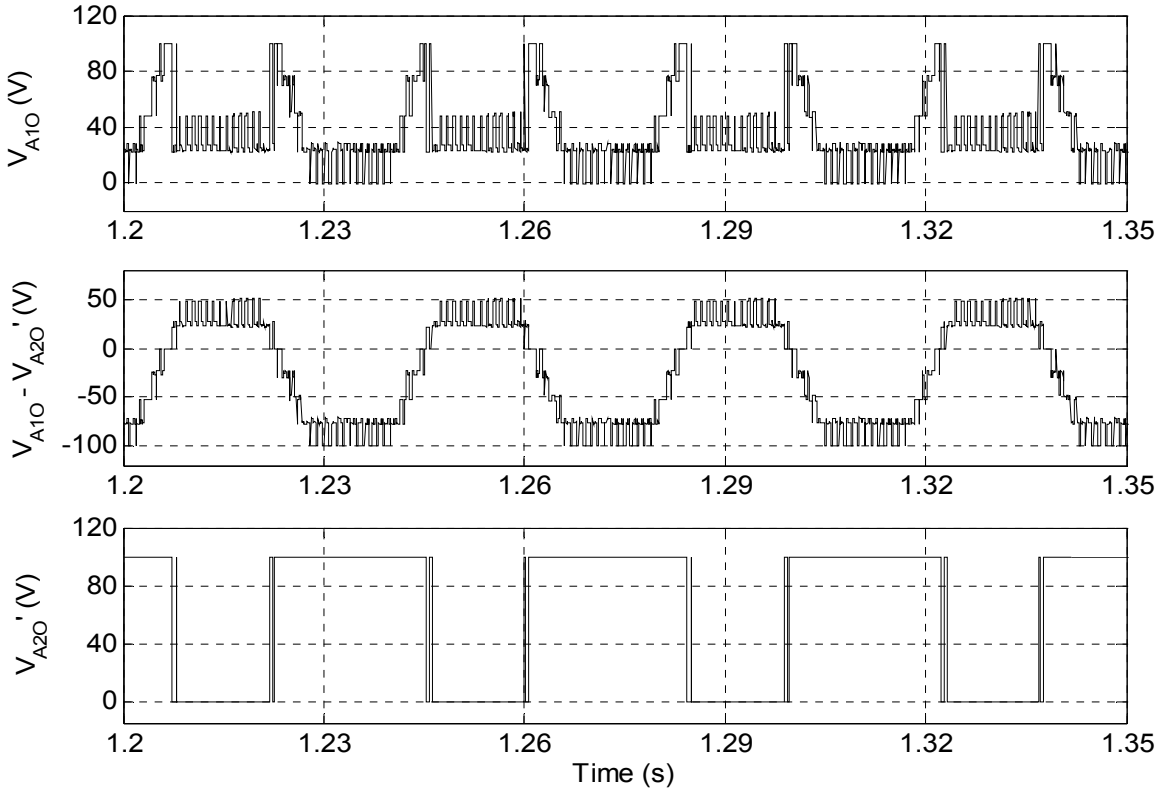



Fig. 7.64: Top trace; 5-level inverter-A pole voltage ($V_{A1O}$), Middle trace; Difference of inverter-A and inverter-B pole voltages ($V_{A1O}$ - $V_{A2O'}$), Bottom trace; 2-level inverter-B pole voltage ($V_{A2O'}$)
(Simulation result: $m$=0.52; $f^*_m$ =26Hz; 7-level mode)

To investigate the performance of inverter under 9-level mode of operation inverter is operated at modulation index $m$=0.8. At this modulation index motor operates at fundamental frequency ($f^*_m$) of 40Hz. Experimentally obtained waveforms of phase-A voltage (trace-1), current (trace-2) and ripple in capacitors voltages $V_{CA1}$ and $V_{CA2}$ (trace-3 and 4) are presented in Fig. 7.65(a). The simulation results under same operating conditions are shown in Fig. 7.67 and Fig. 7.68 in same order as the previous set of results. It can be noticed in simulated (Fig. 7.68) as well as in actual (Fig. 7.65b) pole voltages waveforms that the difference of pole voltage ($V_{A1O}$ - $V_{A2O'}$) contains nine distinct voltage levels as -100, -75, -50, -25, 0, +25, +50, +75 and +100 correspond to -$V_{DC}$/2, -3$V_{DC}$ /8, -$V_{DC}$/4, -$V_{DC}$/8, 0, +$V_{DC}$/8, +$V_{DC}$/4 , +3$V_{DC}$/8 and +$V_{DC}$/2 hence confirm the 9-level mode of operation. The two-level inverter which operates at higher voltage level switch less as compared to the switching devices which operate at lower voltage level results reduced switching losses. The ripple in capacitors voltages ($V_{CA1}$, $V_{CA2}$) is less than 1V in both cases; simulated (Fig. 7.67b) as well as experimental (Fig. 7.65a). This validates the capacitor balancing algorithm. The normalized harmonic spectrum of phase voltage waveform is further improved and THD is only 2.81% (Fig. 7.66a). However, lower order harmonic as well as THD of phase current is little bit increased as depicted in Fig. 7.66(b). Experimental and simulation results are almost matching to each other.

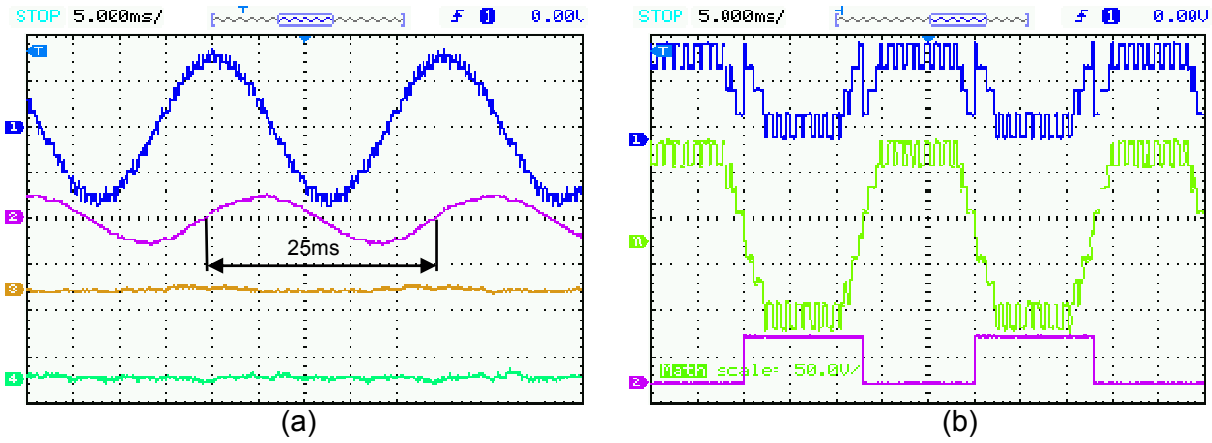



Fig. 7.65: (a) Trace-1: Y-axis= 75V/div; Motor phase-A voltage $V_{A1A2}$ , Trace-2: Y-axis= 1A/div; phase-A current $i_{A1A2}$, Trace-3: Y-axis=2V/div; Ripple in capacitor voltage $V_{CA1}$, Trace-4: Y-axis=2V/div; Ripple in capacitor voltage $V_{CA2}$
(b) Top trace Y-axis: 50V/div; 5-level inverter-A pole voltage ($V_{A1O}$), Middle trace Y-axis: 50V/div; Difference of inverter-A and inverter-B pole voltages ($V_{A1O}$ - $V_{A2O'}$), Bottom trace Y-axis: 100V/div; 2-level inverter-B pole voltage ($V_{A2O'}$)
(Experimental result $m$=0.8; $f^*_m$ =40Hz; 9-level mode)

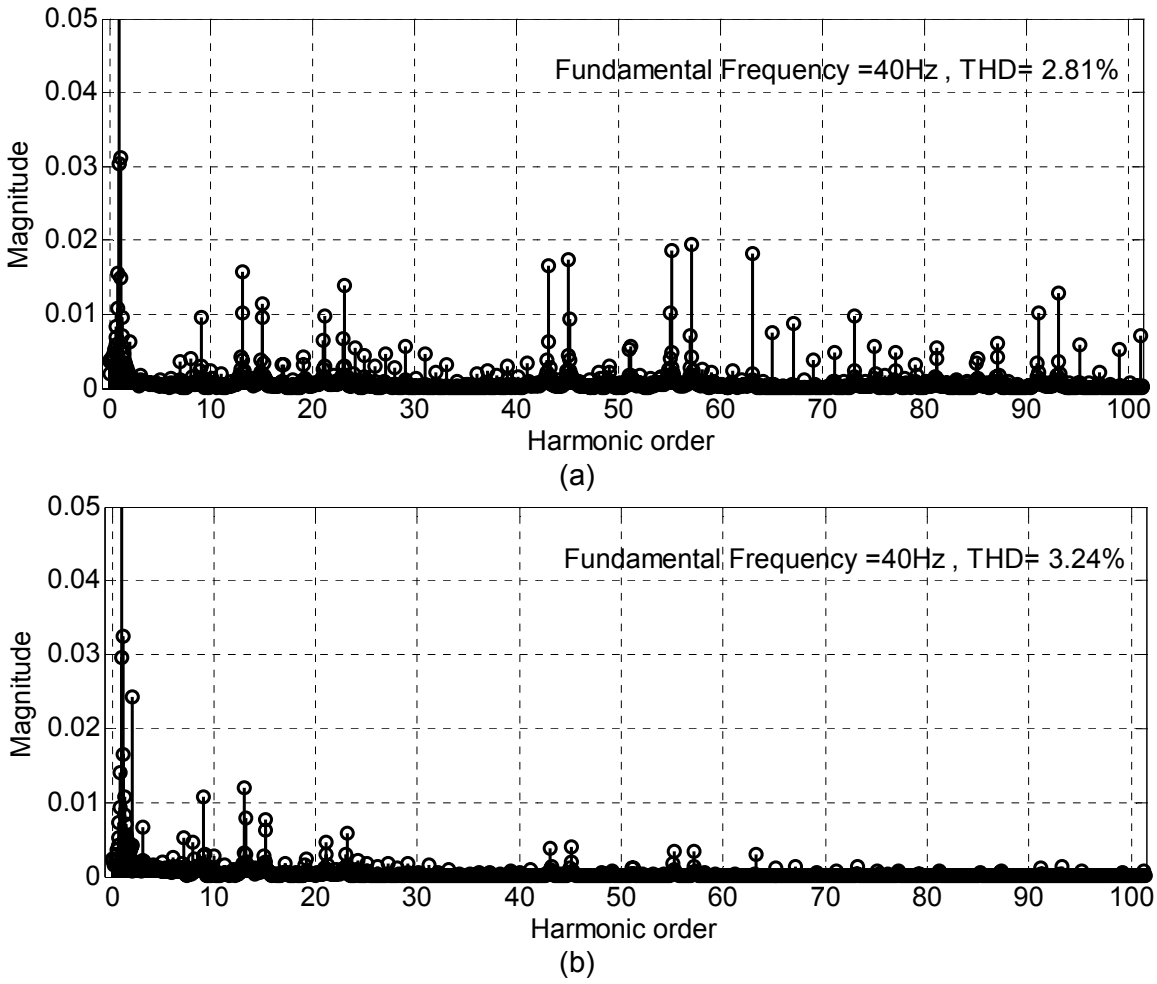



Fig. 7.66: Normalized harmonic spectrum of phase-A (a) Voltage $V_{A1A2}$ (b) Current $i_{A1A2}$
(Experimental result $m$=0.8; $f^*_m$ =40Hz; 9-level mode)

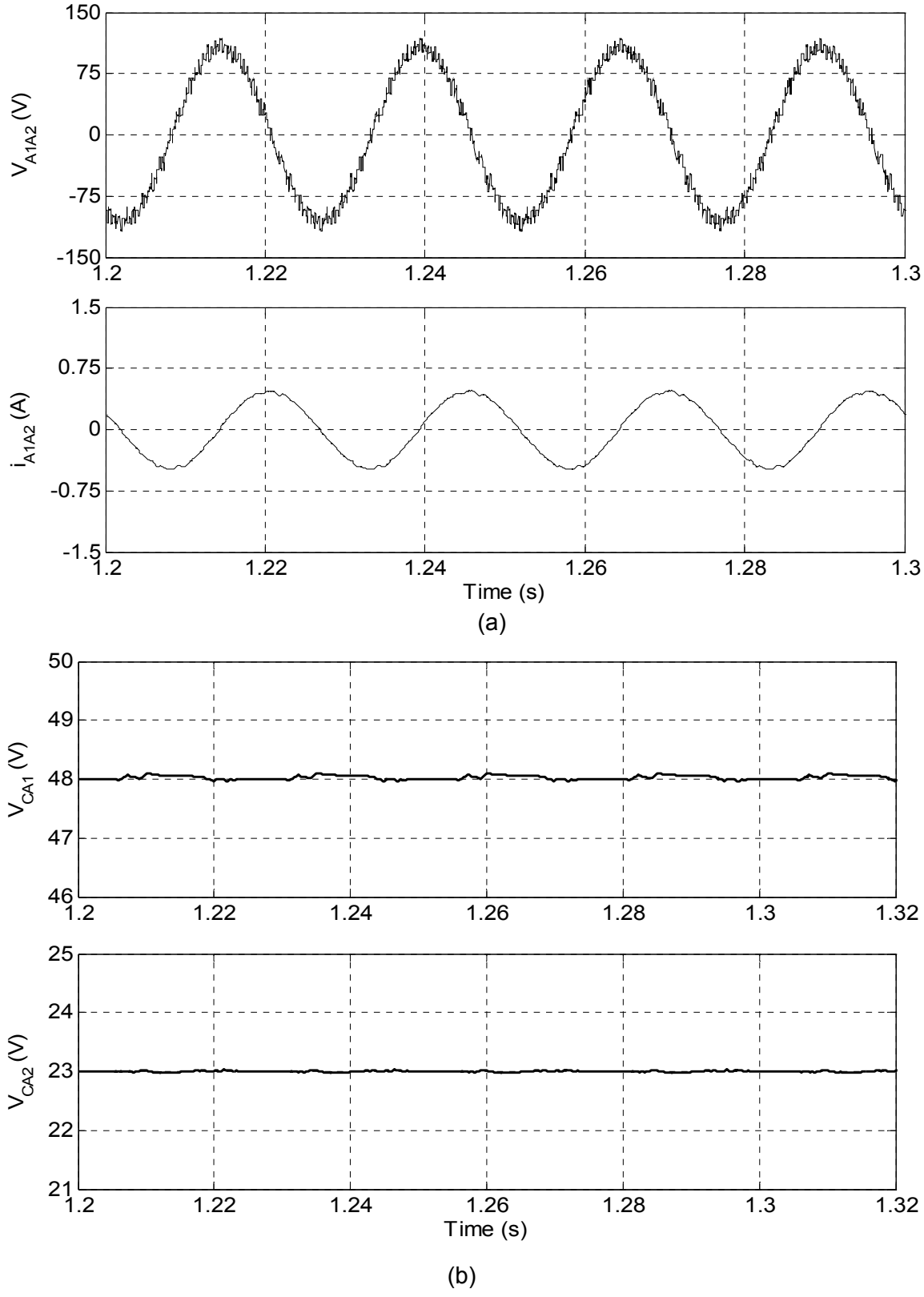



Fig. 7.67: (a) Motor phase-A, voltage $V_{A1A2}$ (upper trace) and current $i_{A2A4}$ (lower trace)
(b) Capacitors voltages $V_{CA1}$ (upper trace) and $V_{CA2}$ (lower trace)
(Simulation result $m$=0.8; $f^*_m$ =40Hz; 9-level mode)

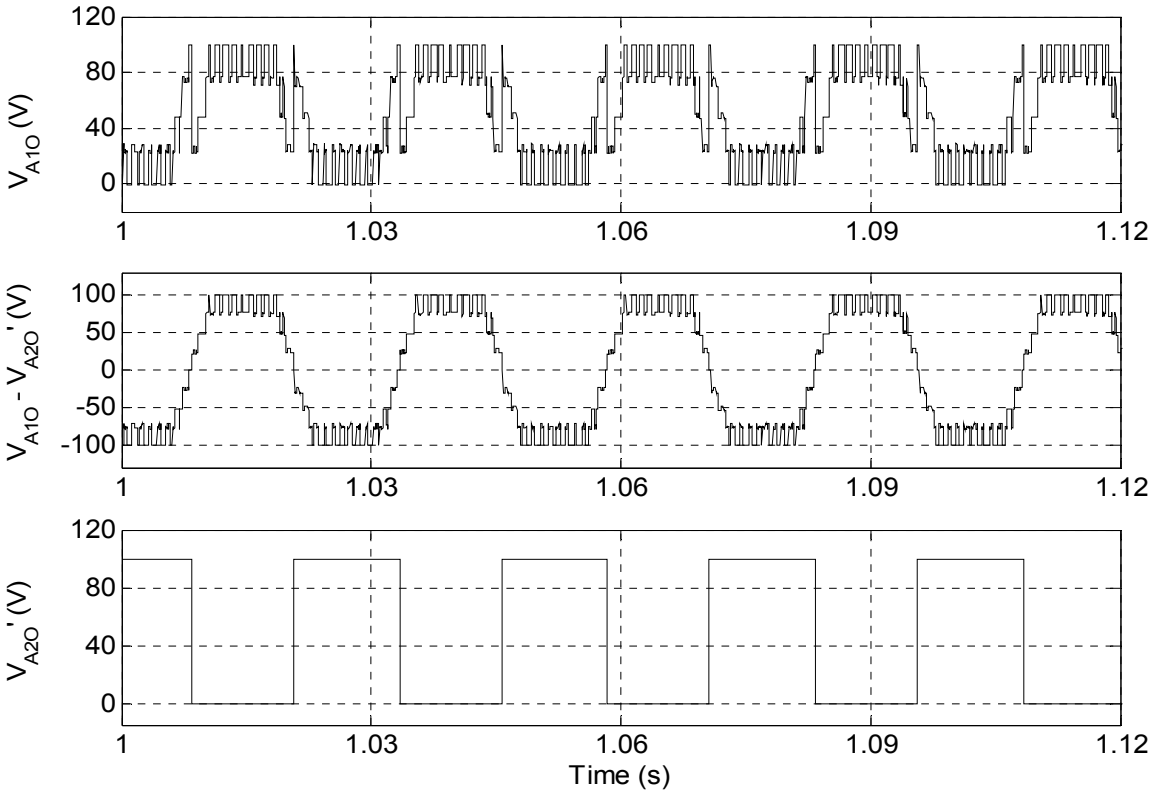
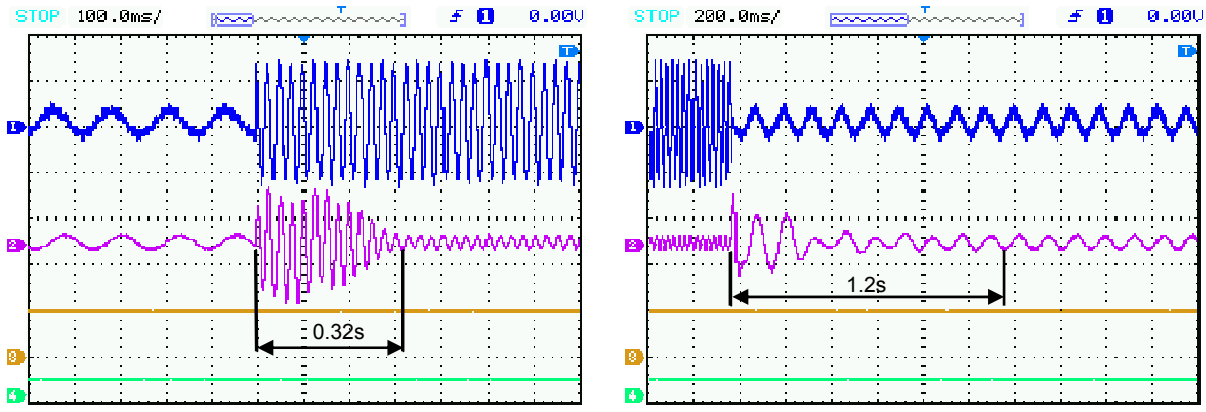



Fig. 7.68: Top trace; 5-level inverter-A pole voltage ($V_{A1O}$), Middle trace; Difference of inverter-A and inverter-B pole voltages ($V_{A1O}$ - $V_{A2O'}$), Bottom trace; 2-level inverter-B pole voltage ($V_{A2O'}$)
(Simulation result $m$=0.8; $f^*_m$ =40Hz; 9-level mode)

The performance of developed prototype hybrid 9-level inverter is also investigated against transient state stability by sudden change its operation from 3-level to 9-level mode and from 9-level to 3-level mode of operation by changing the value of modulation index from 0.16 to 0.8 and vice versa. Fig. 7.69(a) shows the experimentally obtained waveforms of motor phase-A voltage ($V_{A1A2}$), current ($i_{A1A2}$) and ripple in capacitors voltages $V_{CA1}$ and $V_{CA2}$ during sudden change from 3-level to 9-level mode of operation. The simulated waveforms correspond to changeover from 3-level to 9-level mode are shown in Fig. 7.70. It can be observed in simulated and actual waveforms that changeover of inverter operation from 3-level to 9-level take place instantaneously and drive attains its steady state within few cycles. The capacitors voltages are well balance during acceleration even though the current is quite high. The experimental and simulation results pertaining to changeover from 9-level to 3-level mode of operation are shown in Fig. 7.69(b) and Fig. 7.71. It can be observed in this case also capacitors voltages are well balanced and drive attains its steady state very quickly. It is evident from Fig. 7.69 to Fig. 7.71 that the capacitors voltages remain balanced even during the transient period which confirms the effectiveness of capacitor voltage balancing algorithm.




(a) (b)

Fig. 7.69: Trace-1: Y-axis= 100V/div; Motor phase-A voltage $V_{A1A2}$ , Trace-2: Y-axis= 3A/div; phase-A current $i_{A1A2}$, Trace-3: Y-axis=50V/div; Capacitor voltage $V_{CA1}$, Trace-4: Y-axis=25V/div; Capacitor voltage $V_{CA2}$ (a) 3-level to 9-level at no-load (b) 9-level to 3-level at no-load (Experimental result)

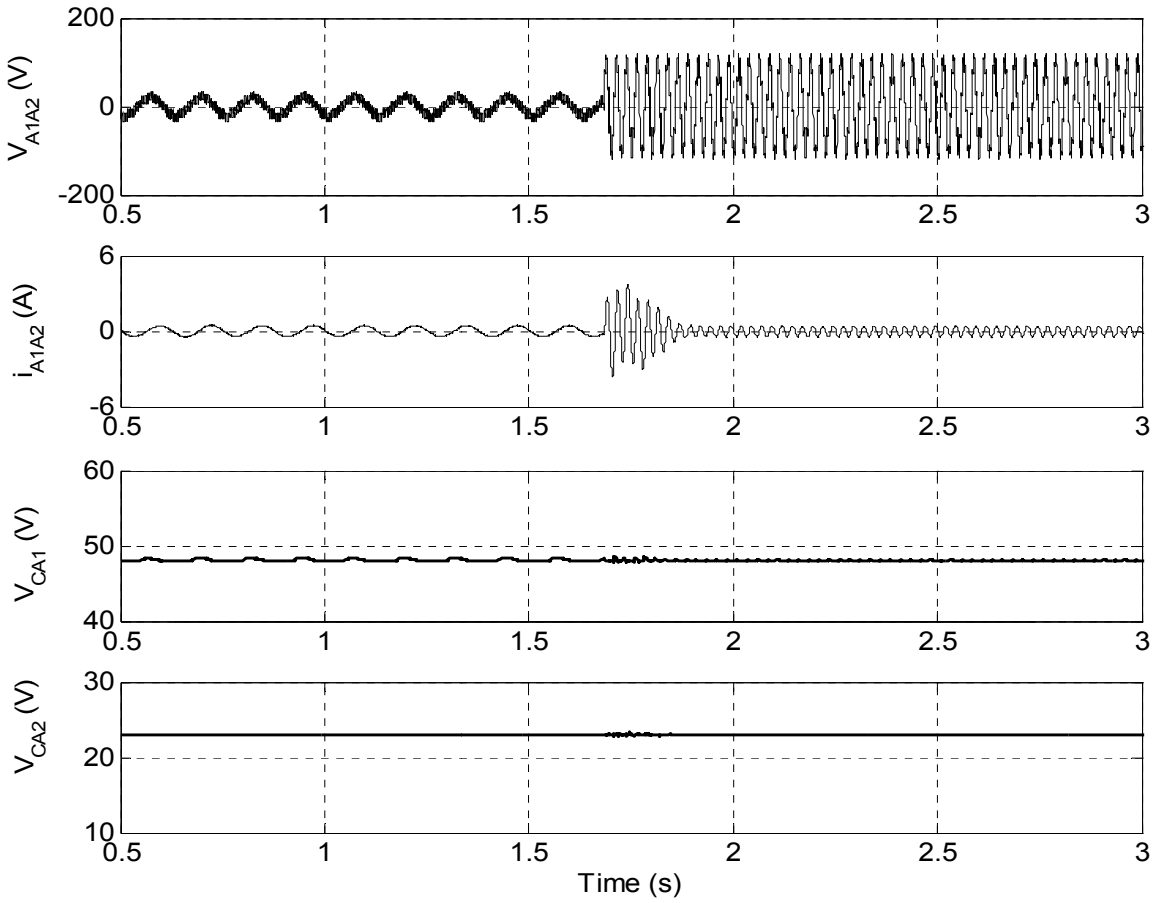



Fig. 7.70: Motor phase-A voltage $V_{A1A2}$, current $i_{A1A2}$, capacitors voltages $V_{CA1}$ and $V_{CA2}$ under sudden change in operation from 3-level to 9-level at no-load (Simulation result)

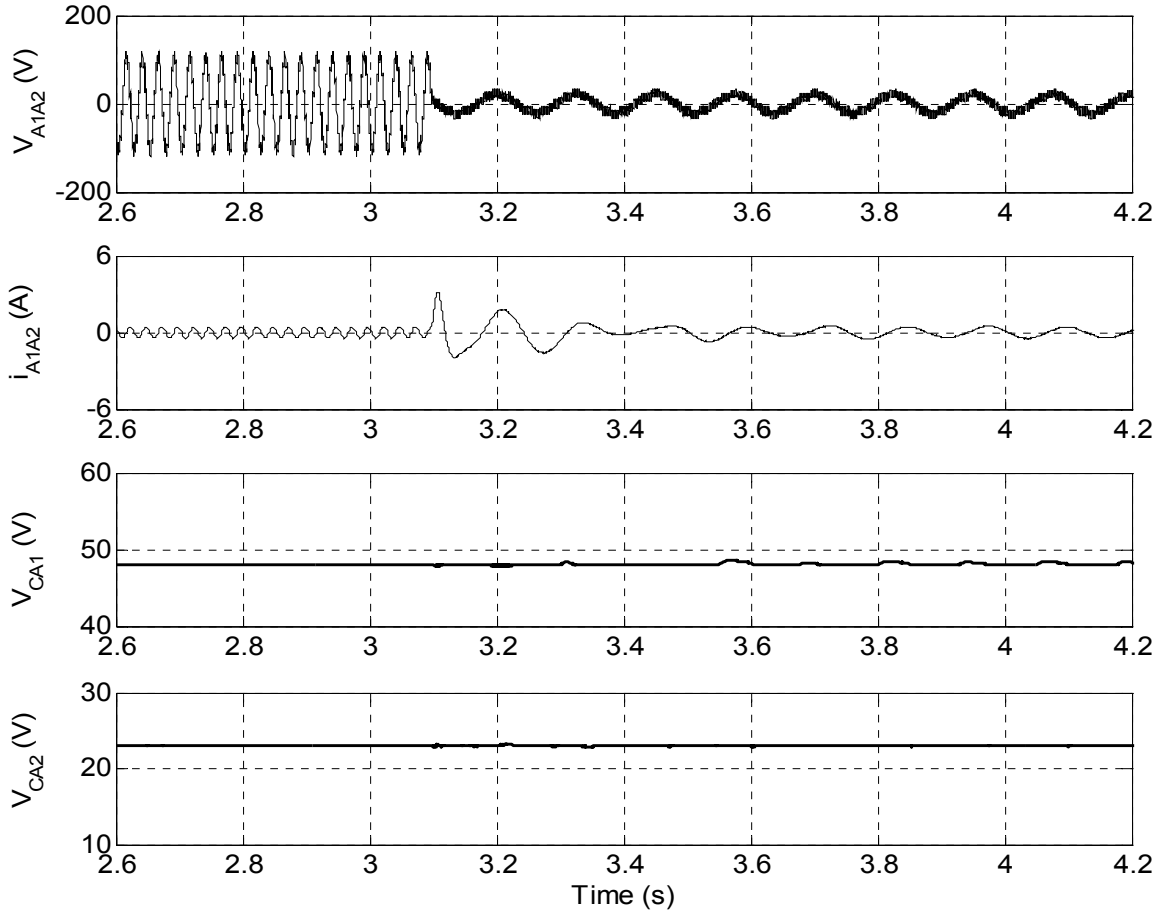



Fig. 7.71: Motor phase-A voltage $V_{A1A2}$, current $i_{A1A2}$, capacitors voltages $V_{CA1}$ and $V_{CA2}$ under sudden change in operation from 9-level to 3-level at no-load (Simulation result)

The effect of disabling the capacitor voltage balancing algorithm is shown in Fig. 7.72. In simulation the capacitor balancing logic is disabled at time t=1s for capacitor $C_{A1}$ and enable at t=3s and for $C_{A2}$ it is disabled at t=3s and enable at t=4.5s and results are shown in Fig. 7.72(b). To obtain experimental results the capacitor balancing logic is disabled at $T_1$ for capacitor $C_{A1}$ and enable at $T_2$ and for $C_{A2}$ it is disabled at $T_2$ and enable at $T_3$. It can be observed from experimental and simulation results shown in Fig. 7.72 (a) and (b) that the phase voltage, current and capacitors voltages regained their original values very quickly after enabling the capacitor voltage balancing algorithm. Some spikes are observed in phase voltage and current due to sudden unbalance in capacitors voltages. The results prove the effectiveness of capacitor voltage balancing logic.

Table 7.3 summarised the experimental and downscaled simulation results shown in Fig. 7.45 - Fig. 7.71. The experimental and simulation results discussed so far establish the fact that in the proposed hybrid 9-level inverter, it is possible to achieve the balancing of capacitors voltages in the entire range of liner modulation as well as during transient period using switching state redundancy available in different levels. It is observed voltages are balanced at lower limit of their respective hysteresis band because the value of

no-load current is very low and it is not capable to overcharge the capacitors. The experimental results verify the performance of the proposed nine-level inverter topology.

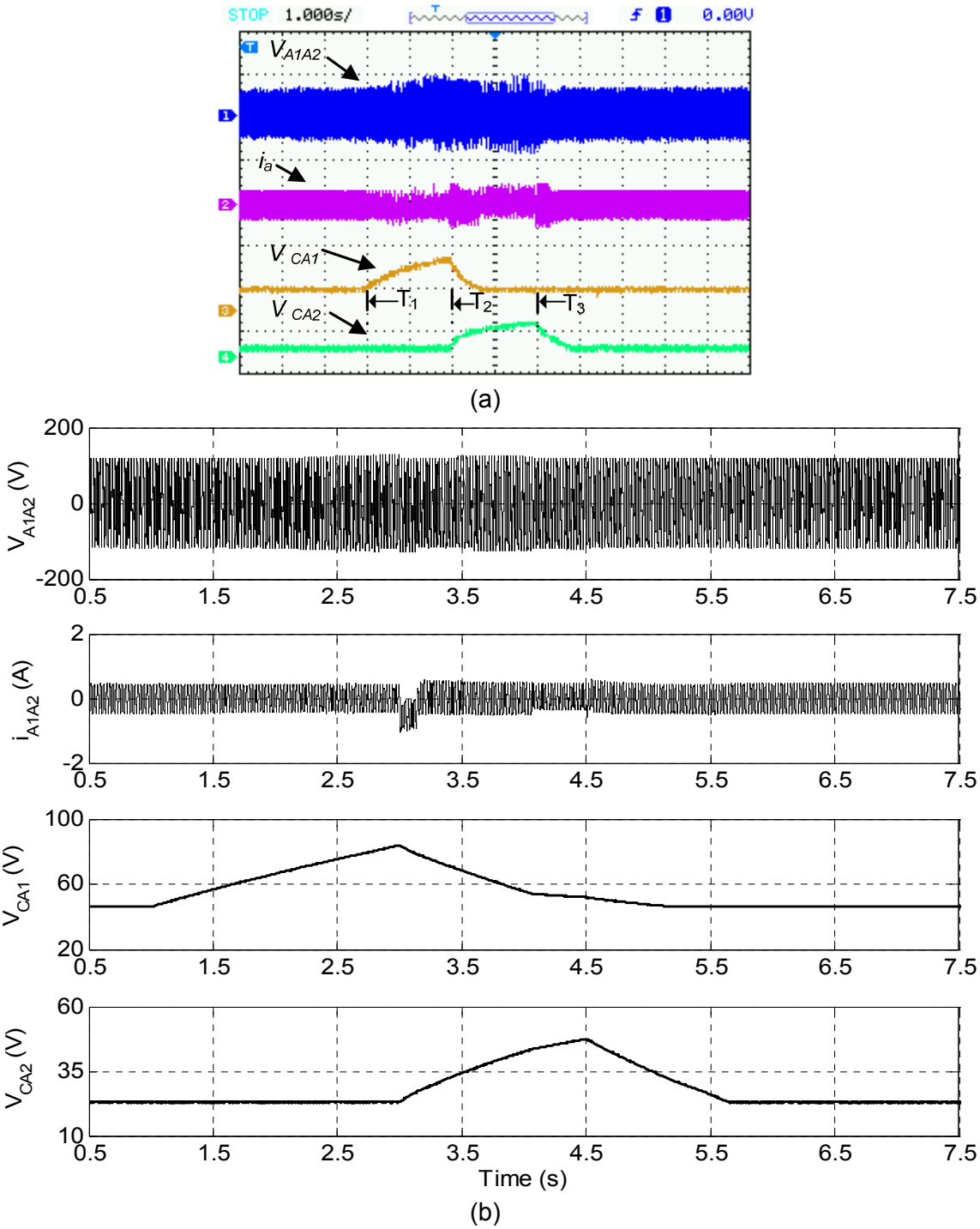



Fig. 7.72: Effect of disabling the capacitor voltage balancing algorithm on phase voltage and current (a) Experimental results ; Trace-1: Y-axis= 150V/div; Motor phase-A voltage $V_{A1A2}$ , Trace-2: Y-axis= 1A/div; phase-A current $i_{A1A2}$, Trace-3: Y-axis=100V/div; Capacitor voltage $V_{CA1}$, Trace-4: Y-axis=100V/div; Capacitor voltage $V_{CA2}$
(b) Simulation results

Table 7.3: Comparison of experimental and downscaled simulation results of proposed hybrid 9-level inverter

| Performance parameter | | Modulation index($m$) | | | | | |
|---|---|---|---|---|---|---|---|
| | | 0.16 | 0.28 | 0.36 | 0.42 | 0.52 | 0.8 |
| Level of operation | Experimental | 3 | 4 | 5 | 6 | 7 | 9 |
| | Simulation | 3 | 4 | 5 | 6 | 7 | 9 |
| RMS of phase-A voltage ($V$) | Experimental | 15.22 | 26.72 | 34.28 | 37.72 | 48.59 | 74.2 |
| | Simulation | 15.88 | 26.97 | 34.62 | 40.02 | 49.23 | 75.78 |
| RMS of phase-A current ($A$) | Experimental | 0.34 | 0.335 | 0.365 | 0.335 | 0.360 | 0.348 |
| | Simulation | 0.34 | 0.341 | 0.339 | 0.338 | 0.342 | 0.323 |
| Frequency of phase voltage ($Hz$) | Experimental | 8 | 14 | 18 | 21 | 26 | 40 |
| | Simulation | 8 | 14 | 18 | 21 | 26 | 40 |
| THD of phase-A voltage in % | Experimental | 42.42 | 12.35 | 7.12 | 5.30 | 3.85 | 2.81 |
| | Simulation | 41.4 | 12.82 | 7.45 | 6.01 | 4.22 | 2.92 |
| Order of dominant voltage harmonic (amplitude in pu) | Experimental | 250±1 (0.2) | 142±2 (0.089) | 111 (0.06) | 95±2 (0.058) | 77±2 (0.042) | 57 (0.02) |
| | Simulation | 250±1 (0.24) | 142±2 (0.097) | 111±2 (0.067) | 95±2 (0.061) | 77±2 (0.054) | 57 (0.031) |
| THD of phase-A Current in % | Experimental | 2.15 | 2.19 | 2.11 | 2.74 | 1.85 | 3.24 |
| | Simulation | 2.64 | 2.32 | 2.52 | 2.81 | 2.4 | 3.72 |
| Order of dominant current harmonic (amplitude in pu) | Experimental | 250±1 (0.008) | 142±2 (0.007) | 49 (0.005) | 95±2 (0.008) | 13 (0.013) | 13 (0.014) |
| | Simulation | 250±1 (0.015) | 142±2 (0.022) | 39 (0.017) | 27 (0.028) | 13 (0.032) | 13 (0.019) |
| $\Delta V_{CA1}(V)$ | Experimental | 0.8 | 0.8 | 0.6 | 0.6 | 0.4 | 0.4 |
| | Simulation | 0.4 | 0.4 | 0.3 | 0.2 | 0.15 | 0.1 |
| $\Delta V_{CA2}(V)$ | Experimental | 0.6 | 0.4 | 0.8 | 0.4 | 0.6 | 0.4 |
| | Simulation | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 |
| Settling time for 3-level to 9-level in sec | Experimental | 0.32 | | | | | |
| | Simulation | 0.29 | | | | | |
| Settling time for 9-level to 3-level in sec | Experimental | 1.2 | | | | | |
| | Simulation | 0.75 | | | | | |
| Sampling time | Experimental | 50 μSecond | | | | | |
| | Simulation | | | | | | |

## 7.4 Conclusion

In this chapter, the development of system hardware for prototype model of 5-Level Inverter, 9-Level Inverter and hybrid 9-Level Inverter for open-end IMD is presented. IGBTs are used as switching devices for implementation of prototype inverter. RT-Lab, from Opal-RT Technologies, is used as real-time hardware-in-loop controller to generate gate pulses for IGBTs in real-time. The different hardware components as required for the proper operation of experimental setups such as driver circuit, isolation and dead-band circuits, voltage and current sensor circuits designed, developed and interfaced with RT-Lab real time controller.

The performance of 5-level inverter (topology-1) based on level shifted triangular carrier SVPWM is evaluated experimentally for constant *V/f* controlled open-end winding IMD in the entire range of modulation. The drive operation is found satisfactory under steady state as well as transient conditions. The transition of drive operation from two-level to 5-level and from 5-level to two-level take place instantaneously and drive achieves its steady state within few cycles. Further, the simulation study is carried out under experimental operating conditions to validate the experimental results. It is found that simulation and experimental results are almost matching to each other.

In order to verify the simulation studies of the proposed 9-level inverter (topology-2), a prototype model of the inverter is developed in the laboratory and experimentation is carried out at reduced voltage. As the experimentation is carried out at reduced voltage, for validating the experimental results, the simulation study at reduced voltage is also carried out. Simulation results are found in good agreement with experimental results. The proposed modified level shifted triangular carrier based SVPWM scheme smoothly change the mode of operation from 3-level to 4-level, then from 4-level to 5-level and so on up to 9-level with increase in modulation index. This feature reduced the switching losses at lower speed range. Stability in voltage levels of the proposed inverter is also examined during sudden change its operation from 3-level to 9-level and from 9-level to 3-level and it is observed that drive attains its steady state very quickly. The motor phase voltage waveform becomes more and more refine as the modulation index increased and approaches towards sinusoidal. The THD in motor phase voltage and current is considerably lesser than the one obtained in 5-level inverter configuration.

The viability of hybrid 9-level inverter topology (topology-3) is examined by running a 1.5kW open-end winding induction motor at no-load in constant *V/f* control mode using developed prototype of inverter. The waveforms of motor phase voltage, phase current, capacitor voltage, inverter pole voltages, difference in inverter pole voltages are found almost the same as they were found in simulation studies. The operation of prototype inverter is found satisfactory in the entire range of linear modulation. The working of capacitors balancing algorithm is tested and verified under steady state as well as transient state

conditions. The capacitors voltages are found well balanced with peak to peak ripple is less than 1V under all operating conditions. The motor phase voltage shows a 3-level or a 4-level waveform for lower values of modulation index, a 5-level or a 6-level or a 7-level waveform for medium values of modulation index and 9-level waveform for higher value. The motor phase voltage waveform approaches towards sinusoidal as the number of level in the waveform increases. The harmonic spectrum of motor phase voltage and current are almost similar to the harmonic spectrums which are obtained with previous configuration of 9-level inverter (topology-2). Further, to validate the experimental results simulation study is carried out again at reduced voltage and it is found simulation and experimental results are almost matching each other except small practical discrepancies.

The experimental and simulation results confirm the practical implementation of all the three topologies.

# CHAPTER 8: CONCLUSION AND FUTURE SCOPE OF RESEARCH

*[The main conclusions of the presented work and possible research in future are summarized in this chapter.]*

## 8.1 Conclusion

This thesis presents the research carried out to improve the performance of multilevel inverter (MLI) for induction motor drive with simplified modelling, control and implementation. Conventional three-phase induction motors used in electric drives are either delta or star connected and the motor has three terminals which are fed using a two-level VSI. In open-end winding induction motor, this delta or star connection is opened and the motor now has six terminals. This motor is then fed from both the ends either with 2-level inverters or 3-level inverters or with a combination of the 2-level and 3-level inverters. Open-end winding induction motor drive configurations offer certain advantages in terms of increased voltage capability, common-mode voltage and current suppression. The multilevel inverter topologies proposed in the thesis uses dual inverter fed open-end winding configuration for the induction motor drive. The major conclusions derived from this research work are summarised as follows:

- An open-end induction motor fed by dual two-level (D2L) inverter investigated in Chapter-2, gives the performance equivalent to a single 3-level inverter fed conventional induction motor drive. In D2L inverter scheme, requirement of clamping diodes which are required in neutral point clamped (NPC) inverter is completely eliminated. In D2L inverter scheme the voltage rating of DC supply and switches are reduced to half as compared to voltage rating of DC supply and switches used in cascade H-bridge (CHB) inverter, this feature reduces the size and cost of the drive. In comparison to flying capacitor (FC) MLI topology the D2L inverter scheme does not requires any flying capacitors.
- A 5-level inversion operation is achieved by using 3-level inverter and conventional 2-level inverter for open-end winding induction motor drive in Chapter-3. The presented configuration generates 512 voltage space vectors distributed over 61 locations. The 2-level inverter is the basic building block of 5-level inverter scheme, the modular approach of the inverter makes its implementation simple and reliable. This structure does not require any clamping diodes and there is no issue of voltage unbalancing. When compared with the series connected H-bridge, it uses three isolated DC sources and 18 switching devices whereas CHB topology needs six isolated DC sources and 24 switching devices. It is observed in simulation results that the adopted 5-level inverter scheme generates the phase voltage profile similar to conventional 5-level inverter. In simulation results it is also found that the voltage and current harmonic spectra of the

presented 5-level inverter fed open-end winding induction motor drive are improved in comparison to dual two level (D2L) inverter fed open-end winding induction motor drive.

- A 2-level inverter based topology for high resolution voltage space phasor generation for an open-end winding induction motor drive is proposed in Chapter-4. The open-end winding induction motor is fed from both ends by two 3-level inverters with asymmetrical DC-links. The 3-level inverter is realized by connecting two 2-level inverters in cascade. The proposed topology generates voltage space phasor equivalent to a conventional 9-level inverter. The proposed configuration generates 4096 voltage space phasors distributed over 217 locations. The currents of the triplen harmonic order are inherently prevented in this scheme due to use of isolated DC supply. In the proposed 9-level inverter configuration the inverter with higher DC-link voltage is switched less frequently than the inverter with lower DC-link voltage making it suitable for high power drives with reduced switching losses. The proposed topology completely eliminates the requirement of 168 clamping diodes and 8 DC-link capacitors which are require in neutral point clamped (NPC) inverter. It also eliminates 84 capacitors of rating $V_{DC}/8$ which are required in 9-level FC inverter topology. This circuit configuration requires 4 isolated DC-power supplies instead of 12 isolated power supplies compared to the CHB topology.
- A modified level shifted triangular carrier based SVPWM technique proposed in Chapter-4, ensures smooth changeover from the mode of 2-level inversion to the 3-level, then 3-level to 4-level, then from 4-level to 5-level and so on up to 9-level inversion and vice versa. This feature reduces the switching losses at lower speed range.
- In Chapter-5, an another power circuit is proposed to realize 9-level inversion operation using only two isolated DC sources of magnitude $V_{DC}/2$ and 30 switching devices. The proposed topology is realized by feeding one end of the open-end winding induction motor by 5-level hybrid inverter and the other end by conventional two-level inverter. The three phase hybrid 5-level inverter is realized by cascading a 3-level flying capacitor (FC) inverter with capacitor fed H-bridge in each phase. A total of 17576 switching combinations are possible in proposed configuration. The proposed hybrid 9-level inverter topology can be operated by a single source of magnitude $V_{DC}/2$ by adopting an appropriate switching scheme to eliminate the common mode voltage in the phase winding. In the proposed circuit, the maximum voltage rating of the switching devices is reduced from $3V_{DC}/4$ to $V_{DC}/2$ as compared to the 9-level inverter topology presented in Chapter-4. A switching state based mathematical model of hybrid 9-level inverter is developed and the performance of proposed topology is evaluated for entire range of linear modulation by operating a 1.5kW open-end winding induction motor model at no-load in MATLAB/Simulink environment. The capacitors voltage balancing is effectively achieved in steady state as well as in transient state conditions. The simulated motor

phase voltage shows a 2-level or a 3-level or a 4-level waveform in the lowest speed range, a 5-level or a 6-level or a 7-level waveform in the medium speed range, a 8-level or a 9-level waveform in the higher speed range. The harmonic spectra of motor phase voltage and current are similar to the harmonic spectrums which are obtained with 9-level inverter proposed in Chapter-4. In the proposed hybrid 9-level inverter, switching devices which operate at higher voltage level switch less as compared to the switching devices which operate at lower voltage level in the entire range of modulation, this feature can lead to use of low switching frequency rated power semiconductor devices; in addition to that the number of components used by hybrid 9-level inverter is quite less as compared to conventional 9-level inverter topologies hence overall cost is reduced.

- An 18-level inverter circuit for open-end winding induction motor drive is proposed in Chapter-6. The proposed circuit uses same number of switching devices as that of used by hybrid 9-level inverter presented in Chapter-5. The maximum amplitude of voltage space phasor generated is $V_{DC}$ whereas the maximum DC link voltage used is $(9/13)V_{DC}$, this feature further reduces the size of inverter. The proposed 18-level inverter completely eliminates 816 clamping diodes and 17 capacitors which are required in 18-level NPC. It also eliminates 408 balancing capacitors which are required in 18-level FC inverter. The proposed topology uses seven isolated DC sources as compared to conventional CHB topology which requires 27 isolated DC supplies. The performance of proposed inverter is examined using MATLAB/Simulink simulation. In simulation results it is found that proposed 18-level inverter gives reduced harmonic distortion even at half of the switching frequency when compared with hybrid 9-level inverter fed open-end winding IM drive.
- In this thesis extensive simulation study is carried out on D2L inverter, 5-level inverter, 9-level inverter, hybrid 9-level inverter and 18-level inverter for open-end induction motor drive. In order to validate the simulations results, downscaled prototypes of 5-level inverter, 9-level inverter and hybrid 9-level inverter are developed in the laboratory and experimentation is carried out. RT-Lab from Opal-RT Technologies is used as real-time hardware-in-loop controller to generate gate pulses for IGBTs in real-time. The different hardware components required for the proper operation of experimental setups such as driver circuit, isolation and dead-band circuits, voltage and current sensor circuits designed, developed and interfaced with RT-Lab real time controller. Further, to validate the experimental results simulation study is carried out again at reduced voltage and it is found that experimental results are in good agreement with the simulation results and confirm the practical implementation of all the three topologies.

## 8.2 Future Scope of Research

All initial objectives for the thesis work have been fulfilled successfully. It is clear that this study is only the first step of future research works but it is presumed to be an important basis. In the future works, the acquired knowledge will be the most powerful tool to reach greater results and to continue making progress. In light of the work accomplished in this thesis, following aspects are identified for future research work:

1. The proposed schemes can be further explored for induction motors with open-end windings with a higher number of phases like 5-phase or 6-phase motors. In such cases, the inverters would have lower DC-link voltage requirements.
2. The proposed hybrid 9-level inverter can be operated using single DC link of magnitude $V_{DC}/2$. In this case, there will be triplen harmonic content in the phase voltages which cause a high triplen harmonic current to flow through the motor phases and power semiconductor devices. An effort can be made to design a harmonic filter or to develop a modulation scheme that should avoid the switching of those vectors which generates triplen harmonics.
3. The performance of proposed MLIs in overmodulation region can be explored further.
4. As the number of levels increases in MLI, device count and possibility of failure in power semiconductor devices rises exponentially. Hence, fault tolerant operation of MLI needs to be explored for reliable operation of MLI.
5. Effort can be made to modify SVPWM scheme to incorporate switching state redundancy to reduce switching losses.

## PUBLICATIONS FROM THE WORK

**International Journal**

**[1] Sanjiv Kumar and Pramod Agarwal**, "A Nine-Level Inverter with Reduced Number of Components for Open-End Winding Induction Motor," *Arabian Journal for Science and Engineering*, *Springer*, Volume 40, Issue 3, pp. 883-892, March 2015.

[2] **Sanjiv Kumar and Pramod Agarwal**, "A Hybrid Nine-Level Inverter Topology for an Open-end Stator Winding Induction Motor," *Electric Power Components and Systems*, *Taylor & Francis*, (**Accepted for publication**).

[3] **Sanjiv Kumar and Pramod Agarwal,** "An Experimental Investigation on Five-Level Inverter Fed Open-end Winding Induction Motor Drive," *Journal of The Institution of Engineers (India): Series B, Springer*, (Third revision submitted).

[4] **Sanjiv Kumar and Pramod Agarwal,** "Performance Evaluation of Eighteen-Level Inverter Fed Open-end Winding IM Drive," *IETE, Taylor & Francis,* (Under review).

**International conferences**

[5] **Sanjiv Kumar and Pramod Agarwal, "**A Nine-Level Inverter For Open-end Induction Motor" *in IEEE International Conference on Recent Advances in Engineering and Computational Sciences (RAECS)*, 2014, pp. 1-6, March 06 - 08, 2014 at UIET Panjab University Chandigarh, India.

[6] **Sanjiv Kumar and Pramod Agarwal,** "A Novel Eighteen-Level Inverter for an Open-end Winding Induction Motor," in *6$^{th}$ IEEE India International Conference on Power Electronics (IICPE)*, 2014, pp.1-6, Dec. 08-10, 2014 at National Institute of Technology Kurukshetra, India.

[7] **Sanjiv Kumar and Pramod Agarwal,** "Simulation of FLC Based Five-Level Inverter Fed Open-end Winding IM Drive," in *IEEE International Conference on Recent Advances in Engineering and Computational Sciences (RAECS)*, 2015, pp. 1-6, December 21 - 22, 2015 at UIET Panjab University Chandigarh, India.

Fig. P.1: Front view of the experimental set-up

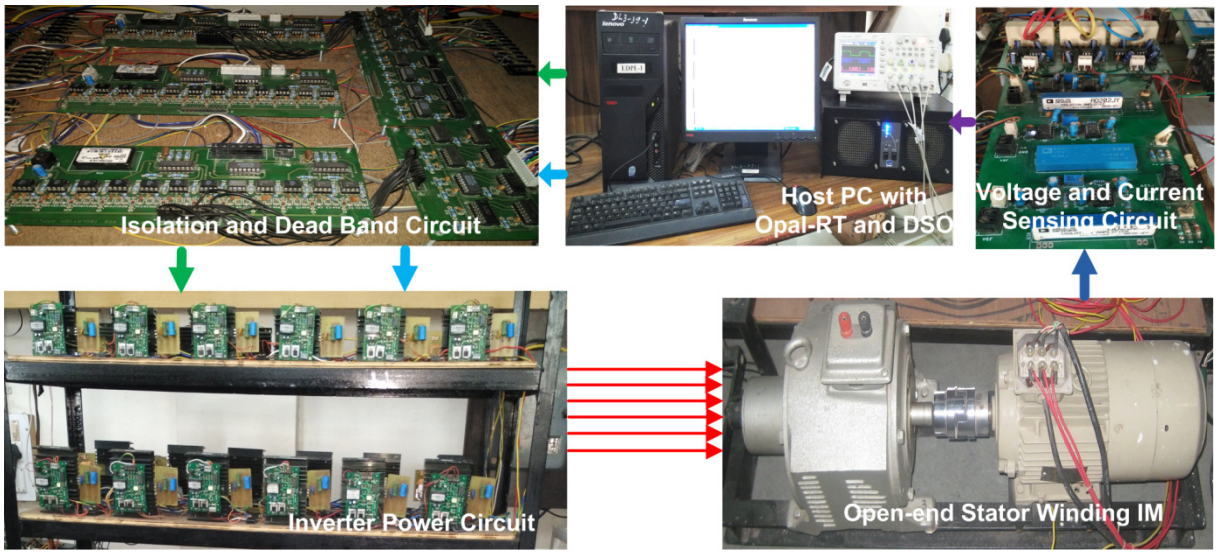



Fig. P.2: Block diagram of the experimental set-up


Fig. P.3: Host PC with Opal-RT and DSO

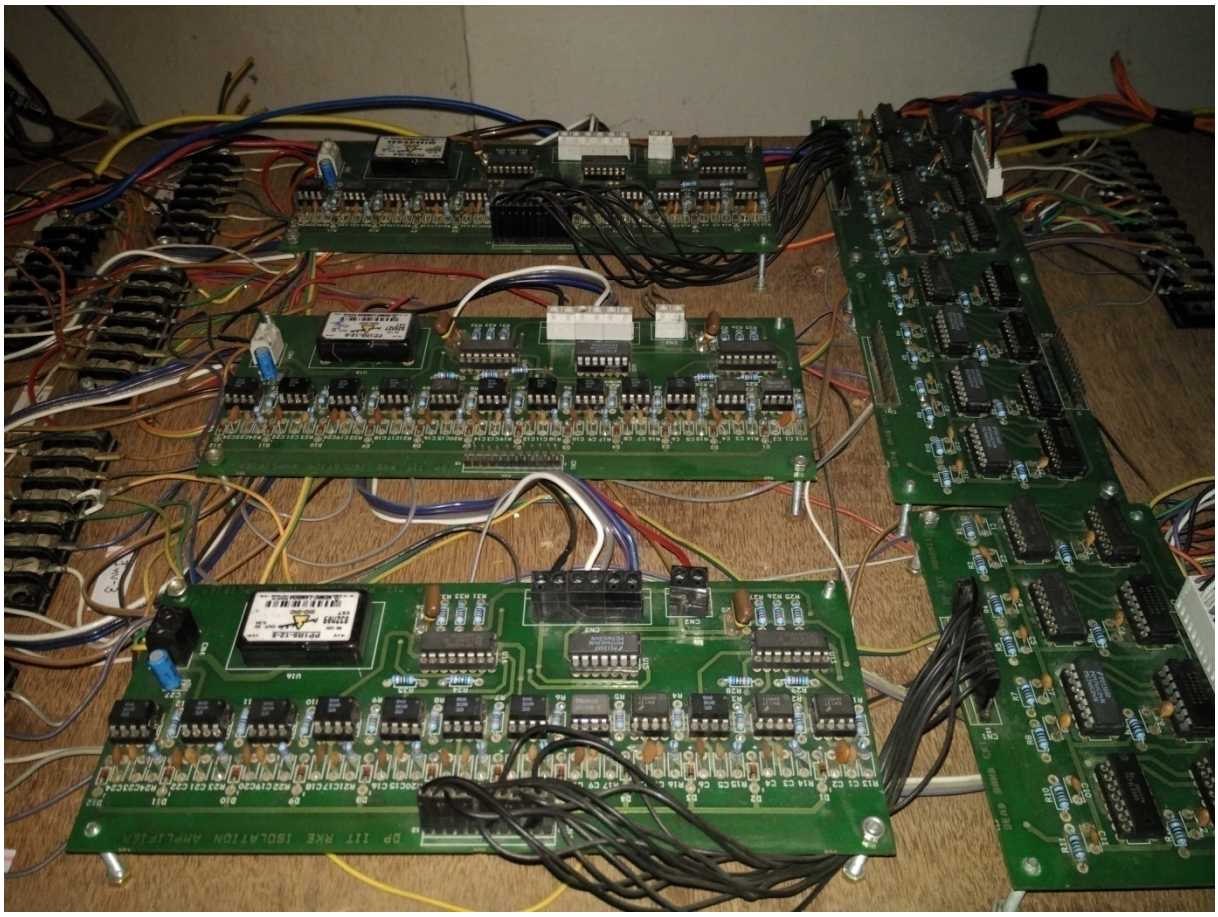


Fig. P.4: Isolation and Dead Band Circuit

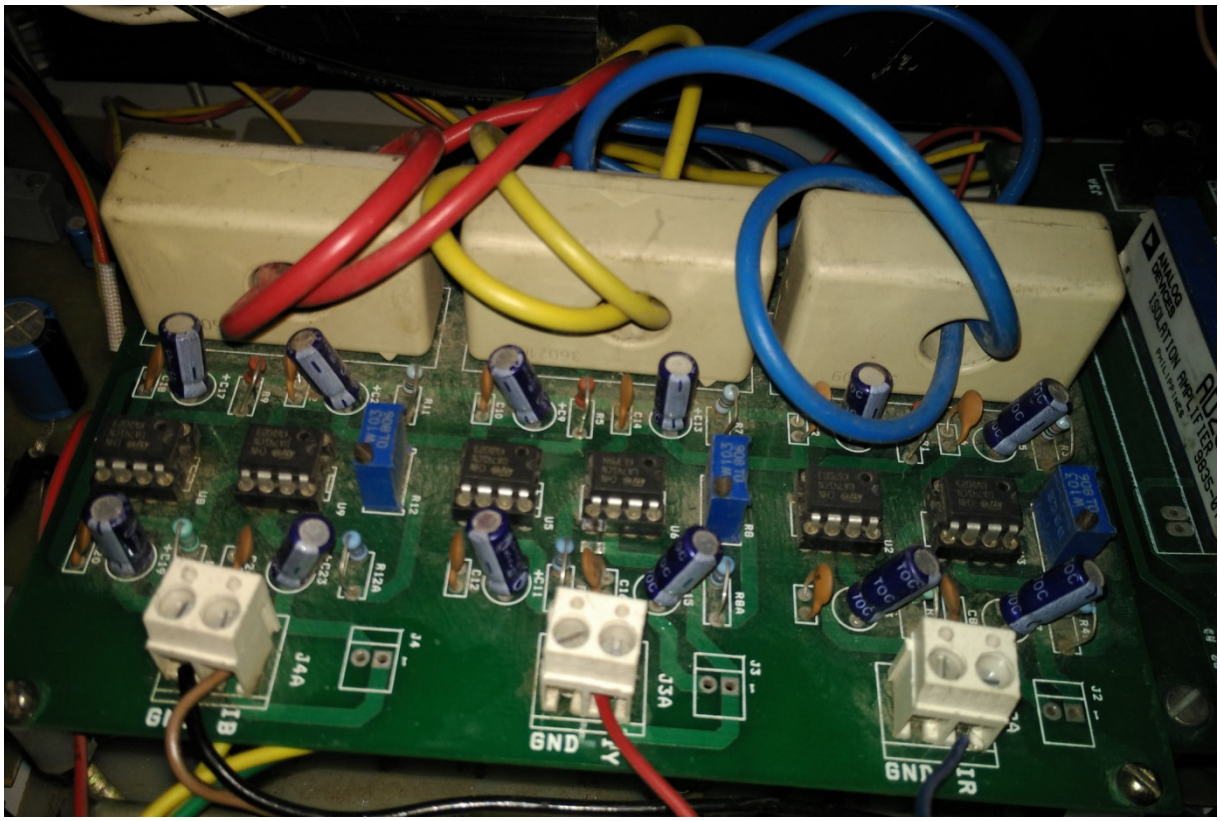



Fig. P.5: Current Sensing Circuit

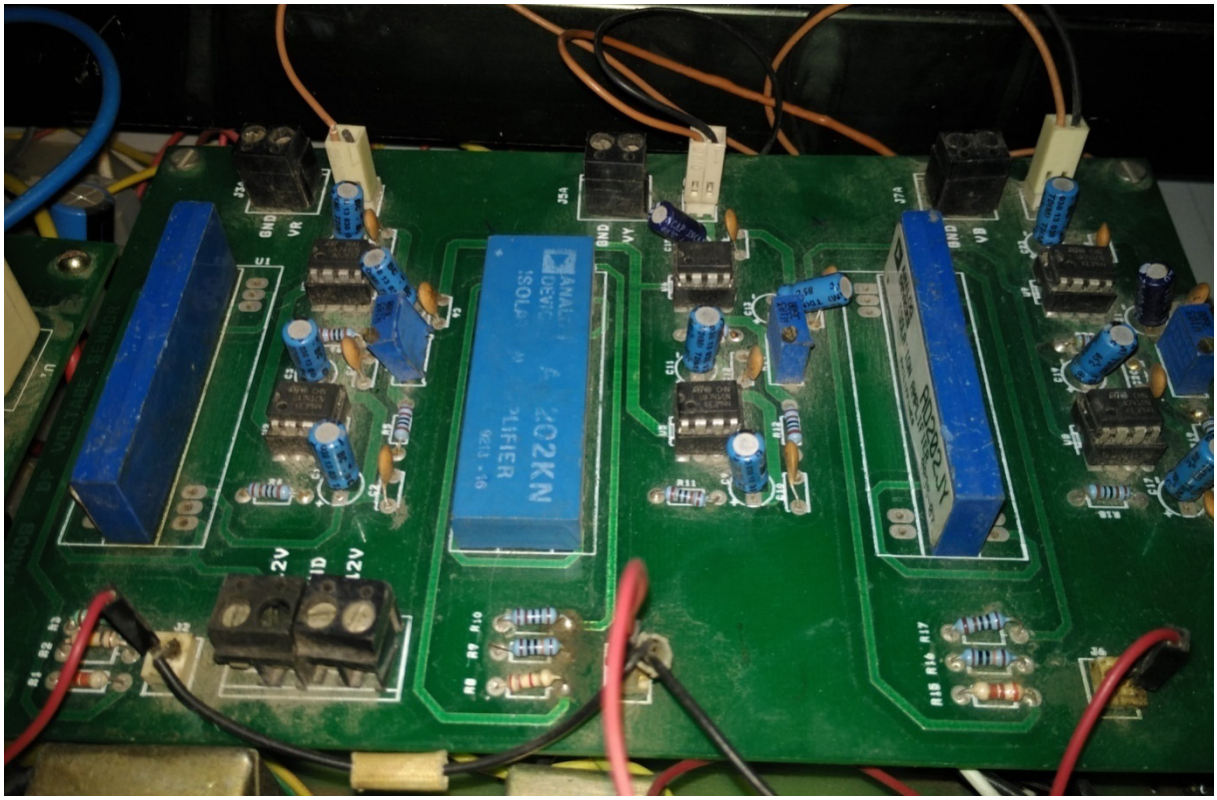



Fig. P.6: Voltage Sensing Circuit

## BIBLIOGRAPHY


[1] **S. Rizzo and N. Zargari**, "Medium Voltage Drives: What does the Future Hold?," in *4th International Power Electronics and Motional Control Conference (IPEMC)*, 2004, pp. 82–89.

[2] **P. K. Steimer, H. E. Gruning, J. Werninger, E. Carroll, S.Klaka, and S.Linder**, "IGCT-A New Emerging Technology for High Power, Low Cost Converters," *IEEE Industry Application Magazine*, pp. 12–18, 1999.

[3] **H. Brunner, M. Hierholzer, T. Laska, and A. Porst**, "Progress in Development of The 3.5 kV High Voltage IGBT/Diode Chipset and 1200A Module Applications," in *Proceedings of 9th International Symposium on Power Semiconductor Devices and IC's*, 1997, pp. 225–228.

[4] **B. Wu**, *High Power Converters and AC Drives*. IEEE press/Wiley A John Wiley & Sons, Inc., Hoboken, New Jersey, 2006.

[5] **S. Malik and D. Kluge**, "ACS 1000 - World 's First Standard AC Drive for Medium-Voltage Applications," *ABB Rev.*, vol. 2, pp. 4–11, 1998.

[6] **B. P. Schmitt and R. Sommer**, "Retrofit of Fixed Speed Induction Motor With Medium Voltage Drive Converters Using NPC Three-Level Inverter High- Voltage IGBT Based Topology," in *IEEE Internationl Symposium on Industrial Electronics*, 2001, vol. 709, pp. 746–751.

[7] **B. Singh, K. B. Naik, and A. K. Goel**, "Steady State Analysis of an Inverter-Fed Induction Motor Employing Natural Commutation," *IEEE Trans. Power Electron.*, vol. 5, no. 1, pp. 117–123, 1990.

[8] **E. P. Wiechmann, P. Aqueveque, R. Burgos, and J. Rodriguez**, "On The Efficiency of Voltage Source and Current Source Inverters for High-Power Drives," *IEEE Trans. Ind. Electron.*, vol. 55, no. 4, pp. 1771–1782, Apr. 2008.

[9] **J. Rodríguez, J. Lai, and F. Z. Peng**, "Multilevel Inverters: A Survey of Topologies , Controls And Applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[10] **Y. Shakweh and E. A. Lewis**, "Assessment of Medium Voltage PWM VSI Topologies for Multi-Megawatt Variable Speed Drive Applications," in *30th Annual IEEE Power Electronics Specialists Conference, South Carolina USA*, 1999, vol. 2, pp. 965–971.

[11] **B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P.Kothari**, "A Review of Three-Phase Improved Power Quality AC-DC Converters," *IEEE Trans. Ind. Electron.*, vol. 51, no. 3, pp. 641–660, Jun. 2004.

[12] **A. von Jouanne, P. Enjeti, and W. Gray**, "Application Issues for PWM Adjustable Speed AC Motor Drives," *IEEE Industry Application Magazine*, pp. 10–18, 1996.

[13] **S. Wei, N. Zargari, B. Wu, and S. Rizzo**, “Comparison and Mitigation of Common Mode Voltage in Power Converter Topologies,” in *Conference Record of the 2004 IEEE Industry Applications Conference, 2004. 39th IAS Annual Meeting.*, 2004, vol. 3, pp. 1852–1857.

[14] **J.S. Lai and F. Z. Peng**, “Multilevel Converters- A New Breed of Power Converters,” *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, 1996.

[15] **L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats**, “The Age of Multilevel Converters Arrives,” *IEEE Industrial Electronics Magazine*, vol. 2, no. 2, pp. 28–39, Jun-2008.

[16] **J. Rodríguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro**, “Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives,” *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[17] **R. Bhatia, H. U. Krattiger, A. Bonanini, J. T. Inge, and G. H. Sydnor**, “Adjustable Speed Drive With a Single 100-MW Synchronous Motor,” *ABB Rev.*, vol. 6, pp. 14–20, 1998.

[18] **A. Nabae, I. Takahashi, and H. Akagi**, “A New Neutral-Point-Clamped PWM Inverter,” *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, 1981.

[19] **R. H. Baker and L. H. Bannister**, “United States Patent Electric Power Converter,” 3,867,643, 1975.

[20] **S. Ogasawara and K. Akagi**, “A Vector Control System Using a Neutral-Point-Clamped Voltage Source PWM Inverter,” in *Conference Record of the 1991 IEEE Industry Applications Society Annual Meeting*, 1991, pp. 422–427.

[21] **H. L. Liu and G. H. Cho**, “Three-Level Space Vector PWM in Low Index Modulation Region Avoiding Narrow Pulse Problem,” *IEEE Trans. Power Electron.*, vol. 9, no. 5, pp. 481–486, Sep. 1994.

[22] **T. A. Meynard and H. Foch**, “Multi-Level Conversion: High Voltage Choppers and Voltage-Source Inverters,” in *PESC `92 Record. 23rd Annual IEEE Power Electronics Specialists Conference*, 1992, pp. 397–403.

[23] **J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama**, “A Survey on Neutral-Point-Clamped Inverters,” *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, Jul. 2010.

[24] **J. Zhao, Y. Han, X. He, C. Tan, J. Cheng, and R. Zhao**, “Multilevel Circuit Topologies Based on the Switched-Capacitor Converter and Diode-Clamped Converter,” *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2127–2136, Aug. 2011.

[25] **N. Celanovic and D. Borojevic**, “A Comprehensive Study of Neutral-Point Voltage Balancing Problem in Three- Level Neutral-Point-Clamped Voltage Source PWM Inverters,” *IEEE Trans. Power Electron.*, vol. 15, no. 2, pp. 242–249, Mar. 2000.

[26] **R. Rojas, T. Ohnishi, and T. Suzuki**, “Neutral-Point-Clamped Inverter with Improved Voltage Waveform and Control Range,” *IEEE Trans. Ind. Electron.*, vol. 42, no. 6, pp. 587–594, Dec. 1995.

[27] **J. K. Steinke**, “Switching Frequency Optimal PWM Control of a Three-Level Inverter,” *IEEE Trans. Power Electron.*, vol. 7, no. 3, pp. 487–496, Jul. 1992.

[28] **A. Shukla, A. Ghosh, and A. Joshi**, “Control Schemes for DC Capacitor Voltages Equalization in Diode-Clamped Multilevel Inverter-Based DSTATCOM,” *IEEE Trans. Power Deliv.*, vol. 23, no. 2, pp. 1139–1149, Apr. 2008.

[29] **K. Siva kumar, K. Gopakumar, G. Mondal, and K. Corzine**, “Neutral-Point Balancing of Neutral-Point-Clamped Three-Level Inverter with a Front End Switched Rectifier DC Source for the Full Modulation Range,” *IET Power Electron.*, vol. 2, no. 5, pp. 527–534, 2009.

[30] **J. Pou, R. Pindado, and D. Boroyevich**, “Voltage-Balance Limits in Four-Level Diode-Clamped Converters With Passive Front Ends,” *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 190–196, Feb. 2005.

[31] **S. Busquets Monge, S. Somavilla, J. Bordonau, and D. Boroyevich**, “Capacitor Voltage Balance for The Neutral-Point- Clamped Converter Using The Virtual Space Vector Concept With Optimized Spectral Performance,” *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1128–1135, Jul. 2007.

[32] **S. Busquets-Monge, S. Alepuz, J. Rocabert, and J. Bordonau**, “Pulsewidth Modulations for the Comprehensive Capacitor Voltage Balance of n-Level Three-Leg Diode-Clamped Converters,” *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1364–1375, May 2009.

[33] **A. K. Gupta and A. M. Khambadkone**, “A Simple Space Vector PWM Scheme to Operate a Three-Level NPC Inverter at High Modulation Index Including Overmodulation Region, With Neutral Point Balancing,” *IEEE Trans. Ind. Appl.*, vol. 43, no. 3, pp. 751–760, 2007.

[34] **J. D. Barros and J. F. Silva**, “Optimal Predictive Control of Three-Phase NPC Multilevel Converter for Power Quality Applications,” *IEEE Trans. Ind. Electron.*, vol. 55, no. 10, pp. 3670–3681, Oct. 2008.

[35] **S. Busquets-Monge, R. K. Maheshwari, and S. Munk-Nielsen**, “Overmodulation of n-Level Three-Leg DC-AC Diode-Clamped Converters With Comprehensive Capacitor Voltage Balance,” *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1872–1883, May 2013.

[36] **H. Akagi and T. Hatada**, “Voltage Balancing Control for a Three-Level Diode-Clamped Converter in a Medium-Voltage Transformerless Hybrid Active Filter,” *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 571–579, Mar. 2009.

[37] **A. Shukla, A. Ghosh, and A. Joshi**, “Natural Balancing of Flying Capacitor Voltages in Multicell Inverter Under PD Carrier-Based PWM,” *IEEE Trans. Power Electron.*, vol. 26, no. 6, pp. 1682–1693, Jun. 2011.

[38] **B. P. McGrath, T. Meynard, G. Gateau, and D. G. Holmes**, “Optimal Modulation of Flying Capacitor and Stacked Multicell Converters Using a State Machine Decoder,” *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 508–516, Mar. 2007.

[39] **A. Shukla, A. Ghosh, and A. Joshi**, “Improved Multilevel Hysteresis Current Regulation and Capacitor Voltage Balancing Schemes for Flying Capacitor Multilevel Inverter,” *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 518–529, Mar. 2008.

[40] **A. Shukla, A. Ghosh, and A. Joshi**, “Capacitor Voltage Balancing Schemes in Flying Capacitor Multilevel Inverters,” in *IEEE Power Electronics Specialists Conference PESC*, 2007, no. 1, pp. 2367–2372.

[41] **B. P. McGrath and D. G. Holmes**, “Natural Capacitor Voltage Balancing for a Flying Capacitor Converter Induction Motor Drive,” *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1554–1561, Jun. 2009.

[42] **H. Jing and K. A. Corzine**, “Extended Operation of Flying Capacitor Multilevel Inverters,” *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 140–147, Jan. 2006.

[43] **F. Defaÿ, A. Llor, and M. Fadel**, “Direct Control Strategy for a Four-Level Three-Phase Flying-capacitor Inverter,” *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2240–2248, Jul. 2010.

[44] **B. P. Mcgrath and D. G. Holmes**, “Enhanced Voltage Balancing of a Flying Capacitor Multilevel Converter Using Phase Disposition ( PD ) Modulation,” *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1933–1942, Jul. 2011.

[45] **L. Zhang and S. J. Watkins**, “Capacitor Voltage Balancing in Multilevel Flying Capacitor Inverters by Rule-Based Switching Pattern Selection,” *IET Electr. Power Appl.*, vol. 1, no. 3, pp. 339–347, 2007.

[46] **M. D. Manjrekar, P. K. Steimer, and T. A. Lipo**, “Hybrid Multilevel Power Conversion System: A Competitive Solution for High-Power Applications,” *IEEE Trans. Ind. Appl.*, vol. 36, no. 3, pp. 834–841, 2000.

[47] **K. Corzine and Y. Familiant**, “A New Cascaded Multilevel H-Bridge Drive,” *IEEE Trans. Power Electron.*, vol. 17, no. 1, pp. 125–131, Jan. 2002.

[48] **M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Pérez**, “A Survey on Cascaded Multilevel Inverters,” *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197–2206, Jul. 2010.

[49] **Y. S. Lai and F. S. Shyu**, “Topology for Hybrid Multilevel Inverter,” *IEE Proc. Electr. Power Appl.*, vol. Vol. 149, no. No. 6, pp. 494–458, 2002.

[50] **J. Ebrahimi, E. Babaei, and G. B. Gharehpetian**, “A New Multilevel Converter

Topology With Reduced Number of Power Electronic Components," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 655–667, Feb. 2012.

[51] **A. L. Batschauer, S. A. Mussa, and M. L. Heldwein**, "Three-Phase Hybrid Multilevel Inverter Based on Half-Bridge Modules," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 668–678, Feb. 2012.

[52] **Y. Li and B. Wu**, "A Novel DC Voltage Detection Technique in the CHB Inverter-Based STATCOM," *IEEE Trans. Power Deliv.*, vol. 23, no. 3, pp. 1613–1619, Jul. 2008.

[53] **N. P. Schibli, T. Nguyen, and A. C. Rufer**, "A Three-Phase Multilevel Converter for High-Power Induction Motors," *IEEE Trans. Power Electron.*, vol. 13, no. 5, pp. 978–986, Sep. 1998.

[54] **M. Veenstra and A. Rufer**, "Control of a Hybrid Asymmetric Multilevel Inverter for Competitive Medium-Voltage Industrial Drives," *IEEE Trans. Ind. Appl.*, vol. 41, no. 2, pp. 655–664, 2005.

[55] **E. Villanueva, P. Correa, J. Rodriguez, and M. Pacas**, "Control of a Single-Phase Cascaded H-Bridge Multilevel Inverter for Grid-Connected Photovoltaic Systems," *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4399–4406, Nov. 2009.

[56] **P. Lezana and G. Ortiz**, "Extended Operation of Cascade Multicell Converters Under Fault Condition," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2697–2703, Jul. 2009.

[57] **W. Song and A. Q. Huang**, "Fault-Tolerant Design and Control Strategy for Cascaded H-Bridge Multilevel Converter-Based STATCOM," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2700–2708, Aug. 2010.

[58] **Z. Du, L. M. Tolbert, B. Ozpineci, and J. N. Chiasson**, "Fundamental Frequency Switching Strategies of a Seven-Level Hybrid Cascaded H-Bridge Multilevel Inverter," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 25–33, Jan. 2009.

[59] **K. Gopakumar, V. T. Ranganathan, and S. R. Bhat**, "Split-Phase Induction Motor Operation from PWM Voltage Source Inverter," *IEEE Trans. Ind. Appl.*, vol. 29, no. 5, pp. 927–932, 1993.

[60] **K. Oguchi, A. Kawaguchi, T. Kubota, and N. Hoshi**, "A Novel Six-Phase Inverter System with 60-Step Output Voltages for High-Power Motor Drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 5, pp. 1141–1149, 1999.

[61] **K. K. Mohapatra, K. Gopakumar, V. T. Somasekhar, and L. Umanand**, "A Novel Modulation Scheme for a Six Phase Induction Motor with Open-end Windings," in *IEEE 28th Annual Conference of the Industrial Electronics Society. IECON 02*, 2002, vol. 1, pp. 810–815.

[62] **K. K. Mohapatra, R. S. Kanchan, M. R. Baiju, P. N. Tekwani, and K. Gopakumar**, "Independent Field-Oriented Control of Two Split-Phase Induction Motors From a Single Six-Phase Inverter," *IEEE Trans. Ind. Electron.*, vol. 52, no. 5, pp. 1372–1382, Oct. 2005.

[63] **H. Stemmler and P. Guggenbach**, "Configurations of High-Power Voltage Source Inverter Drives," in *Fifth European Conference*, 1993, pp. 7–14.

[64] **K. K. Mohapatra, K. Gopakumar, V. T. Somasekhar, and L. Umanand**, "A Harmonic Elimination and Suppression Scheme for an Open-End Winding Induction Motor Drive," *IEEE Trans. Ind. Electron.*, vol. 50, no. 6, pp. 1187–1198, Dec. 2003.

[65] **K. K. Mohapatra and N. Mohan**, "Open-End Winding Induction Motor Driven With Matrix Converter For Common-Mode Elimination," in *International Conference on Power Electronics, Drives and Energy Systems, 2006. PEDES '06*, 2006, pp. 1–6.

[66] **R. Baranwal, K. Basu, and N. Mohan**, "Carrier-Based Implementation of SVPWM for Dual Two-Level VSI and Dual Matrix Converter With Zero Common-Mode Voltage," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1471–1487, Mar. 2015.

[67] **P. P. Rajeevan, K. Sivakumar, K. Gopakumar, C. Patel, and H. Abu-rub**, "A Nine-Level Inverter Topology for Medium-Voltage Induction Motor Drive With Open-End Stator Winding," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3627–3636, Sep. 2013.

[68] **P. P. Rajeevan, K. Sivakumar, C. Patel, R. Ramchand, and K. Gopakumar**, "A Seven-Level Inverter Topology for Induction Motor Drive Using Two-Level Inverters and Floating Capacitor Fed H-Bridges," *IEEE Trans. Power Electron.*, vol. 26, no. 6, pp. 1733–1740, Jun. 2011.

[69] **K. Sivakumar, A. Das, K. Gopakumar, R. Ramchand, and C. Patel**, "A Hybrid Multilevel Inverter Topology for an Open-End Winding Induction-Motor Drive Using Two-Level Inverters in Series With a Capacitor-Fed H-Bridge Cell," *IEEE Trans. Ind. Electron.*, vol. 57, no. 11, pp. 3707–3714, Nov. 2010.

[70] **S. Figarado, K. Sivakumar, R. Ramchand, A. Das, C. Patel, and K. Gopakumar**, "Five-Level Inverter Scheme for an Open-end Winding Induction Machine With Less Number of Switches," *IET Power Electron.*, vol. 3, no. 4, pp. 637–647, 2010.

[71] **S. Figarado, K. Gopakumar, G. Mondal, K. Sivakumar, and N. S. Dinesh**, "Three-Level Inverter Fed Open- end Winding IM Drive with Common Mode Voltage Elimination and Reduced Power Device Count," in *33rd Annual Conference of the IEEE Industrial Electronics Society (IECON) , Nov. 5-8, 2007 Taipei, Taiwan*, 2007, pp. 1238–1243.

[72] **V. T. Somasekhar, K. Gopakumar, M. R. Baiju, K. K. Mohapatra, and L. Umanand**, "A Multilevel Inverter System for an Induction Motor With Open-End Windings," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 824–836, Jun. 2005.

[73] **V. T. Somasekhar, M. R. Baiju, and K. Gopakumar**, “Dual Two-level Inverter Scheme for an Open-end Winding Induction Motor Drive With a Single DC Power Supply and Improved DC Bus Utilisation,” *IEE Proceedings-Electric Power Appl.*, vol. 151, no. 2, pp. 230–238, Mar. 2004.

[74] **M. Baiju, K. Gopakumar, K. K. Mohapatra, V. T. Somasekhar, and L. Umanand**, “Five-Level Inverter Voltage-Space Phasor Generation for an Open-end Winding Induction Motor Drive,” *IEE Proceedings, Electr. Power Appl.*, vol. 150, no. 5, pp. 531–538, Sep. 2003.

[75] **P. P. Rajeevan, K. Sivakumar, C. Patel, K. Gopakumar, and A.-R. Haitham**, “A Hybrid Nine-Level Inverter for IM Drive,” in *2011 IEEE International Symposium on Industrial Electronics*, 2011, pp. 65–70.

[76] **V. T. Somasekhar, K. Gopakumar, A. Pittet, and V. T. Ranganathan**, “PWM Inverter Swiching Strategy for a Dual Two-Level Inverter Fed Open-End Winding Induction Motor Drive With a Swiched Neutral,” *IEE Proc. Electr. Power Appl.*, vol. 149, no. 2, pp. 152–160, Mar. 2002.

[77] **I. Colak, E. Kabalci, and R. Bayindir**, “Review of Multilevel Voltage Source Inverter Topologies and Control Schemes,” *Energy Convers. Manag.*, vol. 52, no. 2, pp. 1114–1128, Feb. 2011.

[78] **H. S. Patel and R. G. Hoft**, “Generalized Techniques of Harmonic Elimination and Voltage Control in Thyristor Inverters: Part I--Harmonic Elimination,” *IEEE Trans. Ind. Appl.*, vol. IA-9, no. 3, pp. 310–317, 1973.

[79] **J. Napoles, J. I. Leon, R. Portillo, L. G. Franquelo, and M. A. Aguirre**, “Selective Harmonic Mitigation Technique for High-Power Converters,” *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2315–2323, Jul. 2010.

[80] **P. N. Enjeti, P. D. Ziogas, and J. F. Lindsay**, “Programmed PWM techniques to eliminate harmonics: A critical evaluation,” *IEEE Trans. Ind. Appl.*, vol. 26, no. 2, pp. 302–316, 1990.

[81] **B. Ozpineci, L. M. Tolbert, and J. N. Chiasson**, “Harmonic Optimization of Multilevel Converters Using Genetic Algorithms,” *IEEE Power Electron. Lett.*, vol. 3, no. 3, pp. 92–95, Sep. 2005.

[82] **L. Li, D. Czarkowski, Y. Liu, and P. Pillay**, “Multilevel Selective Harmonic Elimination PWM Technique in Series-Connected Voltage Inverters,” *IEEE Trans. Ind. Appl.*, vol. 36, no. 1, pp. 160–170, 2000.

[83] **Z. Du, L. M. Tolbert, and J. N. Chiasson**, “Active Harmonic Elimination for Multilevel Converters,” *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 459–469, Mar. 2006.

[84] **J. N. Chiasson, L. M. Tolbert, K. J. Mckenzie, and Z. Du**, “A Complete Solution to the Harmonic Elimination Problem,” *IEEE Trans. Power Electron.*, vol. 19, no. 2, pp.

491–499, Mar. 2004.

[85] **J. Holtz**, “Pulse Width Modulation for Electronic Power Conversion,” in *IEEE Proceedings*, 1994, vol. 82, no. 8, pp. 1194–1214.

[86] **J. Rodriguez, S. Kouro, J. I. Leon, R. C. Portillo, and M. A. Pérez**, “Multilevel Converters□: An Enabling Technology for High-Power Applications,” *Proc. IEEE*, vol. 97, no. 11, pp. 1786–1817, Nov. 2009.

[87] **G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto**, “A New Multilevel PWM Method: A Theoretical Analysis,” *IEEE Trans. Power Electron.*, vol. 7, no. 3, pp. 497–505, Jul. 1992.

[88] **B. P. McGrath and D. G. Holmes**, “Multicarrier PWM Strategies for Multilevel Inverters,” *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 858–867, Aug. 2002.

[89] **J. H. Kim, S. K. Sul, and P. N. Enjeti**, “A carrier-based PWM method with optimal switching sequence for a multilevel four-leg voltage-source inverter,” *IEEE Trans. Ind. Appl.*, vol. 44, no. 4, pp. 1239–1248, 2008.

[90] **M. D. Manjrekar and T. A. Lipo**, “A Hybrid Multilevel Inverter Topology for Drive Applications,” in *APEC ’98 Thirteenth Annual Applied Power Electronics Conference and Exposition*, 1998, vol. 2, pp. 523–529.

[91] **C. Rech and J. R. Pinheiro**, “Hybrid Multilevel Converters: Unified Analysis and Design Considerations,” *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 1092–1104, Apr. 2007.

[92] **V. T. Ranganathan**, “Space Vector Pulsewidth Modulation — A Status Review,” *Sadhana*, vol. 22, no. 6, pp. 675–688, Dec. 1997.

[93] **D. G. Holmes**, “The Significance of Zero Space Vector Placement for Carrier-Based PWM Schemes,” *IEEE Trans. Ind. Appl.*, vol. 32, no. 5, pp. 1122–1129, 1996.

[94] **S. Halasz, G. Csonka, and A. A. M. Hassan**, “Sinusoidal PWM Techniques With Additional Zero-Sequence Harmonics,” in *20th International Conference on Industrial Electronics, Control, and Insrumentation*, 1994, pp. 85–90.

[95] **N. S. Choi, J. G. Cho, and G. H. Cho**, “A General Circuit Topology of Multilevel Inverter,” in *PESC ’91 Record 22nd Annual IEEE Power Electronics Specialists Conference*, 1991, pp. 96–103.

[96] **J. Pou, D. Boroyevich, and R. Pindado**, “New Feedforward Space-Vector PWM Method to Obtain Balanced AC Output Voltages in a Three-Level Neutral-Point-Clamped Converter,” *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 1026–1034, Oct. 2002.

[97] **M. M. Prats, L. G. Franquelo, R. Portillo, J. I. Leon, E. Galvan, and J. M. Carrasco**, “A 3-D Space Vector Modulation Generalized Algorithm for Multilevel Converters,” *IEEE Power Electron. Lett.*, vol. 99, no. 4, pp. 110–114, Dec. 2003.

[98] **A. K. Gupta and A. M. Khambadkone**, “A Space Vector PWM Scheme for Multilevel Inverters Based on Two-Level Space Vector PWM,” *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1631–1639, 2006.

[99] **L. G. Franquelo, M. Á. M. Prats, R. C. Portillo, J. I. L. Galvan, M. a. Perales, J. M. Carrasco, E. G. Díez, and J. L. M. Jiménez**, “Three-Dimensional Space-Vector Modulation Algorithm for Four-Leg Multilevel Converters Using abc Coordinates,” *IEEE Trans. Ind. Electron.*, vol. 53, no. 2, pp. 458–466, Apr. 2006.

[100] **A. K. Gupta and A. M. Khambadkone**, “A General Space Vector PWM Algorithm for Multilevel Inverters, Including Operation in Overmodulation Range,” *IEEE Trans. Power Electron.*, vol. 22, no. 2, Mar. 2007.

[101] **A. S. Aneesh Mohamed, A. Gopinath, and M. R. Baiju**, “A Simple Space Vector PWM Generation Scheme for Any General n-Level Inverter,” *IEEE Trans. Ind. Electron.*, vol. 56, no. 5, pp. 1649–1656, May 2009.

[102] **W. Song, X. Feng, and K. M. Smedley**, “A Carrier-Based PWM Strategy With the Offset Voltage Injection for Single-Phase Three-Level Neutral-Point-Clamped Converters,” *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1083–1095, Mar. 2013.

[103] **F. Wang**, “Sine-Triangle Versus Space-Vector Modulation for Three-Level PWM Voltage-Source Inverters,” *IEEE Trans. Ind. Appl.*, vol. 38, no. 2, pp. 500–506, 2002.

[104] **W. Yao, H. Hu, and Z. Lu**, “Comparisons of Space-Vector Modulation and Carrier-Based Modulation of Multilevel Inverter,” *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 45–51, Jan. 2008.

[105] **J. M. Erdman, R. J. Kerkman, D. W. Schlegel, and G. L. Skibinski**, “Effect of PWM Inverters on AC Motors Bearing Currents and Shaft Voltages,” *IEEE Trans. Ind. Appl.*, vol. 32, no. 2, pp. 250–259, 1996.

[106] **F. Wang**, “Motor Shaft Voltages and Bearing Currents and Their Reduction in Multilevel Medium-Voltage PWM Voltage-Source-Inverter Drive Applications,” *IEEE Trans. Ind. Appl.*, vol. 36, no. 5, pp. 1336–1341, 2000.

[107] **H. Zhang, A. Von Jouanne, S. Dai, A. K. Wallace, and F. Wang**, “Multilevel Inverter Modulation Schemes to Eliminate Common-Mode Voltages,” *IEEE Trans. Ind. Appl.*, vol. 36, no. 6, pp. 1645–1653, 2000.

[108] **A. Von Jouanne, S. Dai, and H. Zhang**, “A Multilevel Inverter Approach Providing DC-link Balancing, Ride-Through Enhancement, and Common-Mode Voltage Elimination,” *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 739–745, Aug. 2002.

[109] **M. R. Baiju, K. K. Mohapatra, R. S. Kanchan, and K. Gopakumar**, “A Dual Two-Level Inverter Scheme With Common Mode Voltage Elimination for an Induction Motor Drive,” *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 794–805, May 2004.

[110] **S. Lakshminarayanan, G. Mondal, P. N. Tekwani, K. K. Mohapatra, and K.**

**Gopakumar**, “Twelve-Sided Polygonal Voltage Space Vector Based Multilevel Inverter for an Induction Motor Drive With Common-Mode Voltage Elimination,” *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2761–2763, Oct. 2007.

[111] **A. K. Gupta and A. M. Khambadkone**, “A Space Vector Modulation Scheme to Reduce Common Mode Voltage for Cascaded Multilevel Inverters,” *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1672–1681, Sep. 2007.

[112] **H. Inose and Y. Yasuda**, “A Unity Bit Coding Method by Negative Feedback,” in *Proceedings of the IEEE*, 1963, vol. 51, no. 11, pp. 1524–1535.

[113] **M. H. Kheraluwala and D. M. Divan**, “Delta Modulation Strategies for Resonant Link Inverters,” *IEEE Trans. Power Electron.*, vol. 5, no. April, pp. 220–228, Apr. 1990.

[114] **S. S. Singh, F. Li, C. Garrett, and R. Thomas**, “A Study of Sigma-Delta Modulation Control Strategies for Multi-Level Voltage Source Inverters,” in *Power Electronics and Variable Speed Drives, 21-23 September 1998*, 1998, pp. 347–352.

[115] **C. S. Diaz, F. I. Escobar, G. C. Diotaiuti, and V. M. G. Arguis**, “Adaptive Sigma-Delta Modulator Applied to Control a Five Level Multilevel Inverter,” in *Proceedings of the Fifth IEEE International Caracas Conference on Devices, Circuits and Systems, Nov. 3-5, 2004.*, 2004, vol. 1, no. 1, pp. 219–224.

[116] **A. Dey, P. P. Rajeevan, R. Ramchand, K. Mathew, and K. Gopakumar**, “A Space-Vector-Based Hysteresis Current Controller for a General n-Level Inverter-Fed Drive With Nearly Constant Switching Frequency Control,” *Ind. Electron. IEEE Trans.*, vol. 60, no. 5, pp. 1989–1998, 2013.

[117] **A. Dey, R. Ramchand, P. P. Rajeevan, C. Patel, K. Mathew, and K. Gopakumar**, “Nearly Constant Switching Frequency Hysteresis Current Controller for General n-level Inverter Fed Induction Motor Drive,” in *IECON 2011-37th Annual Conference of the IEEE Industrial Electronics Society*, 2011, pp. 4451–4456.

[118] **A. Dey, N. A. Azeez, K. Mathew, N. K. Gopakumar, and M. P. Kazmierkowski**, “Hysteresis Current Controller for a General n-Level Inverter Fed Drive With Online Current Error Boundary Computation and Nearly Constant Switching Frequency,” *IET Power Electron.*, vol. 6, no. 8, pp. 1640–1649, 2013.

[119] **P. C. Loh, G. H. Bode, D. G. Holmes, and T. A. Lipo**, “A Time-Based Double-Band Hysteresis Current Regulation Strategy for Single-Phase Multilevel Inverters,” *IEEE Trans. Ind. Appl.*, vol. 39, no. 3, pp. 883–892, 2003.

[120] **R. Rojas, T. Ohnishi, and T. Suzuki**, “An Improved Voltage Vector Control Method for Neutral-Point-Clamped Inverters,” *IEEE Trans. Power Electron.*, vol. 10, no. 6, pp. 666–672, Nov. 1995.

[121] **R. Ramchand, K. Gopakumar, C. Patel, K. Sivakumar, A. Das, and H. Abu-Rub**, “Online Computation of Hysteresis Boundary for Constant Switching Frequency

Current-Error Space-Vector-Based Hysteresis Controller for VSI-Fed IM Drives," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1521–1529, Mar. 2012.

[122] **G. Joos, X. Huang, and B. T. Ooi**, "Direct-Coupled Multilevel Cascaded Series Var Compensators," *IEEE Trans. Ind. Appl.*, vol. 34, no. 5, pp. 1156–1163, 1998.

[123] **B. T. Ooi, G. Joos, and X. Huang**, "Operating Principles of Shunt STATCOM Based on 3-Level Diode-Clamped Converters," *IEEE Trans. Power Deliv.*, vol. 14, no. 4, pp. 1504–1510, Oct. 1999.

[124] **S. Anand, B. G. Fernandes, and K. Chatterjee**, "A New 4-Level Open-Ended Transformer Based STATCOM for High Power Applications," in *36th Annual Conference on IEEE Industrial Electronics Society IECON 2010*, 2010, pp. 1957–1962.

[125] **J. H. Seo, C. H. Choi, and D. S. Hyun**, "A New Simplified Space- Vector PWM Method for Three-Level Inverters," *IEEE Trans. Power Electron.*, vol. 16, no. 4, pp. 545–550, Jul. 2001.

[126] **C. Wang, B. K. Bose, V. Oleschuk, S. Mondal, and J. O. P. Pinto**, "Neural-Network-Based Space-Vector PWM of a Three-Level Inverter Covering Overmodulation Region and Performance Evaluation on Induction Motor Drive," in *IECON'03. 29th Annual Conference of the IEEE Industrial Electronics Society*, 2003, vol. 1, pp. 1–6.

[127] **S. Chen and G. Joos**, "Symmetrical SVPWM Pattern Generator Using Field Programmable Gate Array Implementation," in *APEC. Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition*, 2002, vol. 2, pp. 1004–1010.

[128] **K. Yamanaka, A. M. Hava, H. Kirino, Y. Tanaka, N. Koga, and T. Kume**, "A Novel Neutral Point Potential Stabilization Technique Using the Information of Output Current Polarities and Voltage Vector," *IEEE Trans. Ind. Appl.*, vol. 38, no. 6, pp. 1572–1580, 2002.

[129] **G. T. R. Das and K. C. Sekhar**, "A Novel Eight-level Inverter System for an Open-end Winding Induction Motor," in *IEEE Power Electronics Specialists Conference*, 2007, pp. 719–725.

[130] **K. C. Sekhar and G. T. R. Das**, "Multi-level inverter for Induction Motor Drive," in *International Conference on Power Electronics, Drives and Energy Systems, 2006. PEDES '06.*, 2006, pp. 1–6.

[131] **M. Saeedifard, P. M. Barbosa, and Peter K. Steimer**, "Operation and Control of a Hybrid Seven-Level Converter," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 652–660, Feb. 2012.

[132] **V. G. Agelidis and M. Calais**, "Application Specific Harmonic Performance Evaluation of Multicarrier PWM Techniques," in *PESC 98, 29th Annual IEEE Power Electronics Specialists Conference*, 1998, pp. 172–178.

[133] **S. G. Lee, D.-W. Kang, Y.-H. Lee, and D. S. H. Hyun**, "The Carrier-Based PWM Method for Voltage Balance of Flying Capacitor Multilevel Inverter," *2001 IEEE 32nd Annu. Power Electron. Spec. Conf.*, vol. 1, pp. 126–131, 2001.

[134] **M. Khazraei, H. Sepahvand, K. Corzine, and M. Ferdowsi**, "A Generalized Capacitor Voltage Balancing Scheme for Flying Capacitor Multilevel Converters," in *Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2010, pp. 58–62.

[135] **K. Ramachandrasekhar, S. Mohan, and S. Srinivas**, "An Improved PWM for a Dual Two-Level Inverter Fed Open-end Winding Induction Motor Drive," in *The XIX International Conference on Electrical Machines - ICEM*, 2010, pp. 1–6.

[136] **M. A. S. Mendes, Z. M. A. Peixoto, P. F. Seixas, and P. Donoso-Garcia**, "A Space Vector PWM Method for Three-Level Flying-Capacitor Inverters," in *2001 IEEE 32nd Annual Power Electronics Specialists Conference*, 2001, pp. 182–187.

[137] **J. Suh, C. Choi, and D. Hyun**, "A New Simplified Space-Vector PWM Method for Three-Level Inverters," in *APEC '99. Fourteenth Annual Applied Power Electronics Conference and Exposition*, 1999, pp. 515–520.

[138] **S. Halasz, G. Csonka, A. A. M. Hassan, and B. T. Huu**, "Analysis of the Unipolar PWM Techniques," in *Proceedings of 8th Mediterranean Electrotechnical Conference on Industrial Applications in Power Systems, Computer Science and Telecommunications (MELECON 96)*, 1996, vol. 1, pp. 353–356.

[139] **P. Palanivel and S. S. Dash**, "Control of Three Phase Cascaded Multilevel Inverter Using Various Novel Multicarrier Pulse Width Modulation Techniques," in *TENCON 2010 IEEE Region 10 Conference*, 2010, pp. 59–64.

[140] **R. Bojoi, M. Lazzari, F. Profumo, and A. Tenconi**, "Digital Field-Oriented Control for Dual Three-Phase Induction Motor Drives," *IEEE Trans. Ind. Appl.*, vol. 39, no. 3, pp. 752–760, 2003.

[141] **S. Alepuz, S. Busquets-Monge, J. Bordonau, J. A. Martinez-Velasco, C. A. Silva, J. Pontt, and J. Rodriguez**, "Control Strategies Based on Symmetrical Components for Grid-Connected Converters Under Voltage Dips," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 2162–2173, Jun. 2009.

[142] **A. Von Jouanne, S. D. S. Dai, and H. Z. H. Zhang**, "A Simple Method for Balancing The DC-link Voltage of Three-Level Inverters," *2001 IEEE 32nd Annu. Power Electron. Spec. Conf.*, pp. 1341–1345, 2001.

[143] **M. Botao, L. Congwei, Z. Yang, and L. Fahai**, "New SVPWM Control Scheme for Three-Phase Diode Clamping Multilevel Inverter With Balanced DC Voltages," in *IECON Proceedings, Industrial Electronics Conference*, 2002, pp. 903–907.

[144] **L. Lin, Y. Zou, Z. Wang, and H. Jin**, "A Simple Neutral-Point Voltage Balancing

Control Method for Three-Level NPC PWM VSI Inverters," *IEEE Int. Conf. Electr. Mach. Drives, 2005.*, pp. 828–833, 2005.

[145] **M. Koyama, T. Fujii, R. Uchida, and T. Kawabata**, "Space Voltage Vector-Based New PWM Method for Large Capacity Three-Level GTO Inverter," in *Proceedings of the 1992 International Conference on Industrial Electronics, Control, Instrumentation, and Automation*, 1992, pp. 271–276.

[146] **P. F. Seixas, M. A. Severo Mendes, P. Donoso-Garcia, and A. M. N. Lima**, "A Space Vector PWM Method for Three-Level Voltage Source Inverters," in *APEC 2000. Fifteenth Annual IEEE Applied Power Electronics Conference and Exposition*, 2000, vol. 1, pp. 549–555.

[147] **S. Bernet**, "Recent Developments of High Power Converters for Industry and Traction Applications," *IEEE Trans. Power Electron.*, vol. 15, no. 6, pp. 1102–1117, Nov. 2000.

[148] **P. W. Hammond**, "United States Patent Medium Voltage PWM Drive and Method," 5,625,545, 1997.

[149] **K. Yamanaka, K. K. Yamada, and T. Terada**, "United States Patent Three-Level Neutral Point Clamping Type Inverter Circuit," US 6,226,192 B1, 2001.

[150] **M. F. Aiello, P. W. Hammod, and M. Rastogi**, "United States Patent Modular Multi-Level Adjustable Supply With Parallel Connected Active Inputs," US 6,301,130 B1, 2001.

[151] **L. M. Tolbert, F. Z. Peng, and T. G. Habetler**, "Multilevel Inverters for Electric Vehicle Applications," in *IEEE Workshop on Power Electronics in Transportation*, 1998, pp. 79–84.

[152] **Z. Du, B. Ozpineci, L. M. Tolbert, and J. N. Chiasson**, "DC-AC Cascaded H-Bridge Multilevel Boost Inverter With No Inductors for Electric/Hybrid Electric Vehicle Applications," *IEEE Trans. Ind. Appl.*, vol. 45, no. 3, pp. 963–970, 2009.

[153] **S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Pérez, and J. I. Leon**, "Recent Advances and Industrial Applications of Multilevel Converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[154] **J. Dixon, L. Moran, J. Rodriguez, and R. Domke**, "Reactive power compensation technologies: State-of-the-art review," *Proc. IEEE*, vol. 93, no. 12, pp. 2144–2164, Dec. 2005.

[155] **F. Z. Peng, J. Lai, J. W. Mckeever, and J. Vancoevering**, "A Multilevel Voltage-Source Inverter with Separate DC Sources for Static Var Generation," *IEEE Trans. Ind. Appl.*, vol. 32, no. 5, pp. 1130–1138, 1996.

[156] **Y. Cheng, C. Qian, M. L. Crow, S. Pekarek, and S. Atcitty**, "A Comparison of Diode-Clamped and Cascaded Multilevel Converters for a STATCOM With Energy Storage,"

*IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1512–1521, Oct. 2006.

[157] **S. Alepuz, S. Busquets-Monge, J. Bordonau, J. Gago, D. González, and J. Balcells**, "Interfacing Renewable Energy Sources to the Utility Grid Using a Three-Level Inverter," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1504–1511, Oct. 2006.

[158] **W. C. Rossmann and R. G. Ellis**, "Retrofit of 22 Pipeline Pumping Stations with 3000 HP Motors and Variable-Frequency Drives," *IEEE Trans. Ind. Appl.*, vol. 34, no. 1, pp. 178–186, 1996.

[159] **H. Okayama, R. Uchida, M. Koyama, S. Mizoguchi, S. Tamai, H. Ogawa, T. Fujii, and Y. Shimomura**, "Large Capacity High Performance 3-Level GTO Inverter System for Steel Main Rolling Mill Drives," in *IAS '96. Conference Record of the 1996 IEEE Industry Applications Conference Thirty-First IAS Annual Meeting*, 1996, vol. 1, pp. 174–179.

[160] **M. Malinowski, S. Stynski, W. Kolomyjski, and M. P. Kazmierkowski**, "Control of Three-Level PWM Converter Applied to Variable-Speed-Type Turbines," *IEEE Trans. Ind. Electron.*, vol. 56, no. 1, pp. 69–77, Jan. 2009.

[161] **R. C. Portillo, M. M. Prats, J. I. Leon, J. A. Sánchez, J. M. Carrasco, E. Galván, and L. G. Franquelo**, "Modeling Strategy for Back-to-Back Three-Level Converters Applied to High-Power Wind Turbines," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1483–1491, Oct. 2006.

[162] **C. H. Ng, M. A. Parker, L. Ran, P. J. Tavner, J. R. Bumby, and E. Spooner**, "A Multilevel Modular Converter for a Large, Light Weight Wind Turbine Generator," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1062–1074, May 2008.

[163] **F. S. Kang, S. J. Park, S. E. Cho, C. U. Kim, and T. Ise**, "Multilevel PWM Inverters Suitable for the Use of Stand-Alone Photovoltaic Power Systems," *IEEE Trans. Energy Convers.*, vol. 20, no. 4, pp. 906–915, Dec. 2005.

[164] **S. Busquets-Monge, J. Rocabert, P. Rodríguez, S. Alepuz, and J. Bordonau**, "Multilevel Diode-Clamped Converter for Photovoltaic Generators With Independent Voltage Control of Each Solar Array," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2713–2723, Jul. 2008.

[165] **N. A. Rahim and J. Selvaraj**, "Multistring Five-Level Inverter With Novel PWM Control Scheme for PV Application," *IEEE Trans. Ind. Electron.*, vol. 57, no. 6, pp. 2111–2123, Jun. 2010.

[166] **M. Saeedifard, R. Iravani, and J. Pou**, "A Space Vector Modulation Strategy for a Back-to-Back Five-Level HVDC Converter System," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 452–466, Feb. 2009.

[167] **S. Guanchu, K. Lee, L. Xinchun, and L. Chongbo**, "New Neutral Point Balancing Strategy for Five-Level Diode Clamped Converters Used in STATCOM of Wind

Energy Conversion Systems," in *2009 IEEE 6th International Power Electronics and Motion Control Conference*, 2009, vol. 3, pp. 2354–2358.

[168] **G. S. Buja and M. P. Kazmierkowski**, "Direct Torque Control of PWM Inverter-Fed AC Motors-A Survey," *IEEE Trans. Ind. Electron.*, vol. 51, no. 4, pp. 744–757, Aug. 2004.

[169] **A. Kumar, B. G. Fernandas, and K. Chatterjee**, "Direct Torque Control of Open-end Winding Induction Motor Drive Using the Concept of Imaginary Switching Times for Marine Propulsion Systems," in *31st Annual Conference of IEEE Industrial Electronics Society, 2005. IECON 2005*, 2005, pp. 1504–1509.

[170] **V. Verma, C. Chakraborty, and S. Maiti**, "Speed Sensorless Vector Controlled Induction Motor Drive Using Single Current Sensor," *IEEE Trans. Energy Convers.*, vol. 28, no. 4, pp. 938–950, Dec. 2013.

[171] **A. V. R. Teja, C. Chakraborty, S. Maiti, and Y. Hori**, "A New Model Reference Adaptive Controller for Four Quadrant Vector Controlled Induction Motor Drives," *IEEE Trans. Ind. Electron.*, vol. 59, no. 10, pp. 3757–3767, Oct. 2012.

[172] **A. Choudhury and K. Chatterjee**, "Speed Sensor Less Direct Torque Controlled Induction Motor Drive With Constant Switching Frequency Operation," in *IEEE 2011 EnergyTech*, 2011, pp. 1–6.

[173] **S. Maiti, C. Chakraborty, Y. Hori, and M. C. Ta**, "Model Reference Adaptive Controller-Based Rotor Resistance and Speed Estimation Techniques for Vector Controlled Induction Motor Drive Utilizing Reactive Power," *IEEE Trans. Ind. Electron.*, vol. 55, no. 2, pp. 594–601, Feb. 2008.

[174] **C. Chakraborty, M. C. Ta, and Y. Hori**, "Speed Sensorless, Efficiency Optimized Control of Induction Motor Drives Suitable for EV Applications," in *The 29th Annual Conference of the IEEE Industrial Electronics Society, 2003. IECON '03.*, 2003, vol. 1, pp. 913–918.

[175] **A. Dey, B. Singh, D. Chandra, and B. Dwivedi**, "A Novel Approach to Minimize Torque Ripples in DTC Induction Motor Drive," in *International Conference on Power, Control and Embedded Systems (ICPCES), 2010*, 2010, pp. 1–6.

[176] **E. G. Shivakumar, K. Gopakumar, S. K. Sinha, A. Pittet, and V. T. Ranganathan**, "Space Vector PWM Control of Dual Inverter Fed Open-End Winding Induction Motor Drive," in *Applied Power Electronics Conference and Exposition, APEC*, 2001, vol. 1, pp. 399–405.

[177] **K. Sivakumar, A. Das, R. Ramchand, C. Patel, and K. Gopakumar**, "A Three Level Voltage Space Vector Generation for Open End Winding IM Using Single Voltage Source Driven Dual Two-Level Inverter," in *TENCON 2009 IEEE Region 10 Conference*, 2009, pp. 1–5.

[178] **B. P. McGrath, D. G. Holmes, and T. Lipo**, "Optimized Space Vector Switching Sequences for Multilevel Inverters," *IEEE Trans. Power Electron.*, vol. 18, no. 6, pp. 1293–1301, Nov. 2003.

[179] **R. S. Kanchan, M. R. Baiju, K. K. Mohapatra, P. P. Ouseph, and K. Gopakumar**, "Space Vector PWM Signal Generation for Multilevel Inverters Using Only the Sampled Amplitudes of Reference Phase Voltages," *IEE Proc. Electr. Power Appl.*, vol. 152, pp. 297–309, Mar. 2005.

[180] **V. T. Somasekhar, K. Chandrasekhar, and K. Gopakumar**, "A New Five-Level Inverter System for an Induction Motor With Open-end Windings," in *The Fifth International Conference on Power Electronics and Drive Systems, PEDS*, 2003, pp. 199–204.

[181] **M.R.Baiju, K.K.Mohapatra, V.T.Somasekhar, K.Gopakumar, and L.Umanand**, "A Five-Level Inverter Voltage Space Phasor Generation for an Open-end Winding Induction Motor Drive," in *Applied Power Electronics Conference and Exposition, 2003. APEC '03. Eighteenth Annual IEEE*, 2003, vol. 2, pp. 826–832.

[182] **K. Sivakumar, A. Das, R. Ramchand, C. Patel, and K. Gopakumar**, "A Simple Five-Level Inverter Topology for Induction Motor Drive Using Conventional Two-Level Inverters and Flying Capacitor Technique," in *35th Annual Conference of IEEE Industrial Electronics*, 2009, pp. 1009–1013.

[183] **J. D. Irwin**, *The Power Electronics Handbook*. CRC Press LLC, 2002.

[184] **A. Somani, R. K. Gupta, K. K. Mohapatra, and N. Mohan**, "On the Causes of Circulating Currents in PWM Drives With Open-End Winding AC Machines," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3670–3678, Sep. 2013.

[185] **P. Roshankumar, P. P. Rajeevan, K. Mathew, K. Gopakumar, J. I. Leon, and L. G. Franquelo**, "A Five-Level Inverter Topology with Single-DC Supply by Cascading a Flying Capacitor Inverter and an H-Bridge," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3505–3512, 2012.

[186] **P. W. Hammond**, "A New Approach to Enhance Power Quality for Medium Voltage AC Drives," *IEEE Trans. Ind. Appl.*, vol. 33, no. 1, pp. 202–208, 1997.

**Open-end Winding Induction Motor Rating and Parameters**

| | |
|---|---|
| Rated power: | 1.5 kW |
| Rated Voltage: | 415 V (+/- 10 %) 3-Ø star connection |
| Rated Current: | 3.3A |
| Nominal Speed: | 1415 rpm |
| Pole pairs: | 2 |
| Rated frequency: | 50 Hz (+/- 5 %) |
| Nominal efficiency: | 79.0 % |
| Stator resistance: | 6.325 Ω |
| Rotor resistance: | 3.476 Ω |
| Magnetizing inductance: | 0.363 H |
| Stator leakage inductance: | 0.0203 H |
| Rotor leakage inductance: | 0.0203 H |
| Moment of inertia: | 0.0033 kg-$m^2$ |

In this appendix, the screenshots of the controller of a 9-level Inverter developed using RT-Lab in HIL and MATLAB/Simulink are shown.

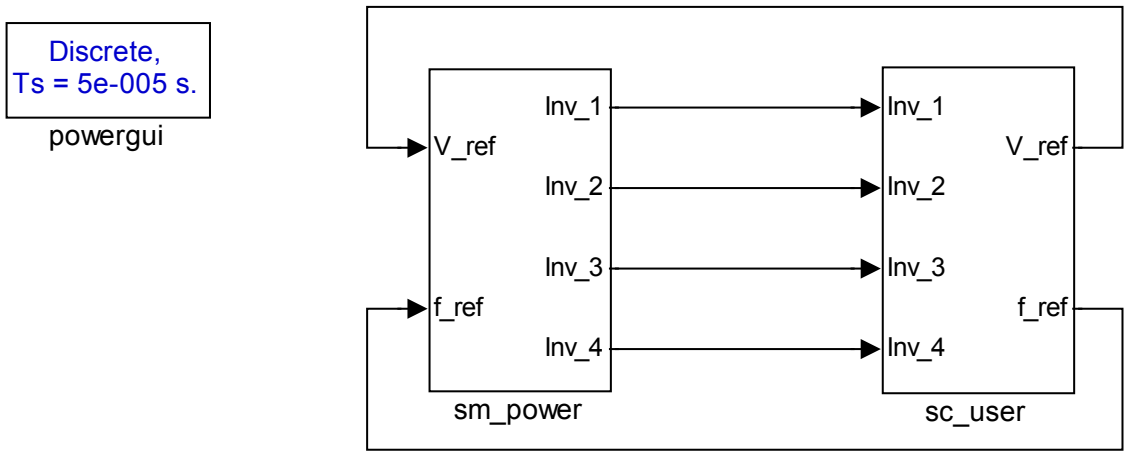



Fig. B.1: First screen of controller block

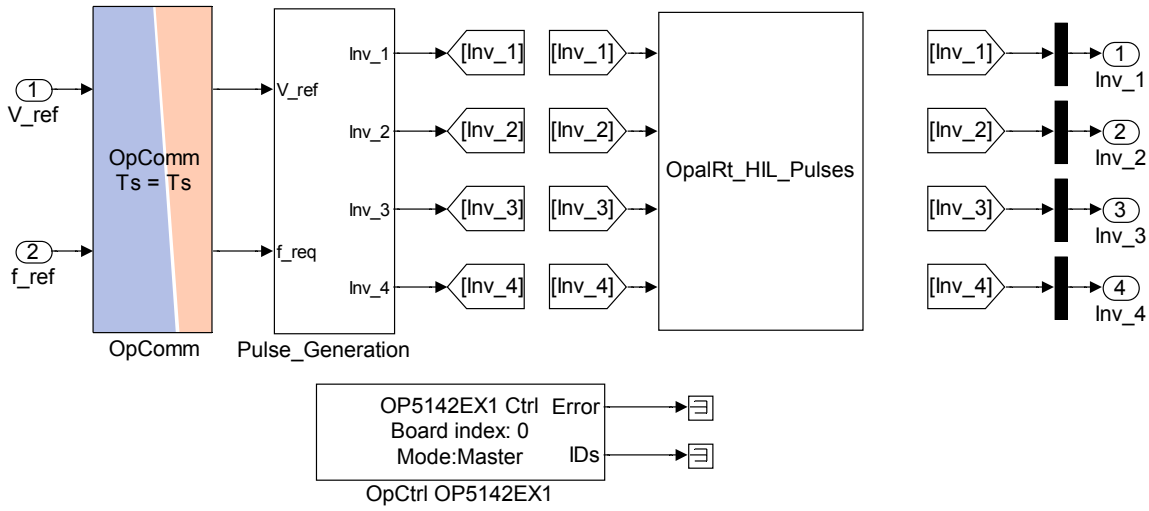



Fig. B.2: PWM pulse generation in MATLAB/Simulink

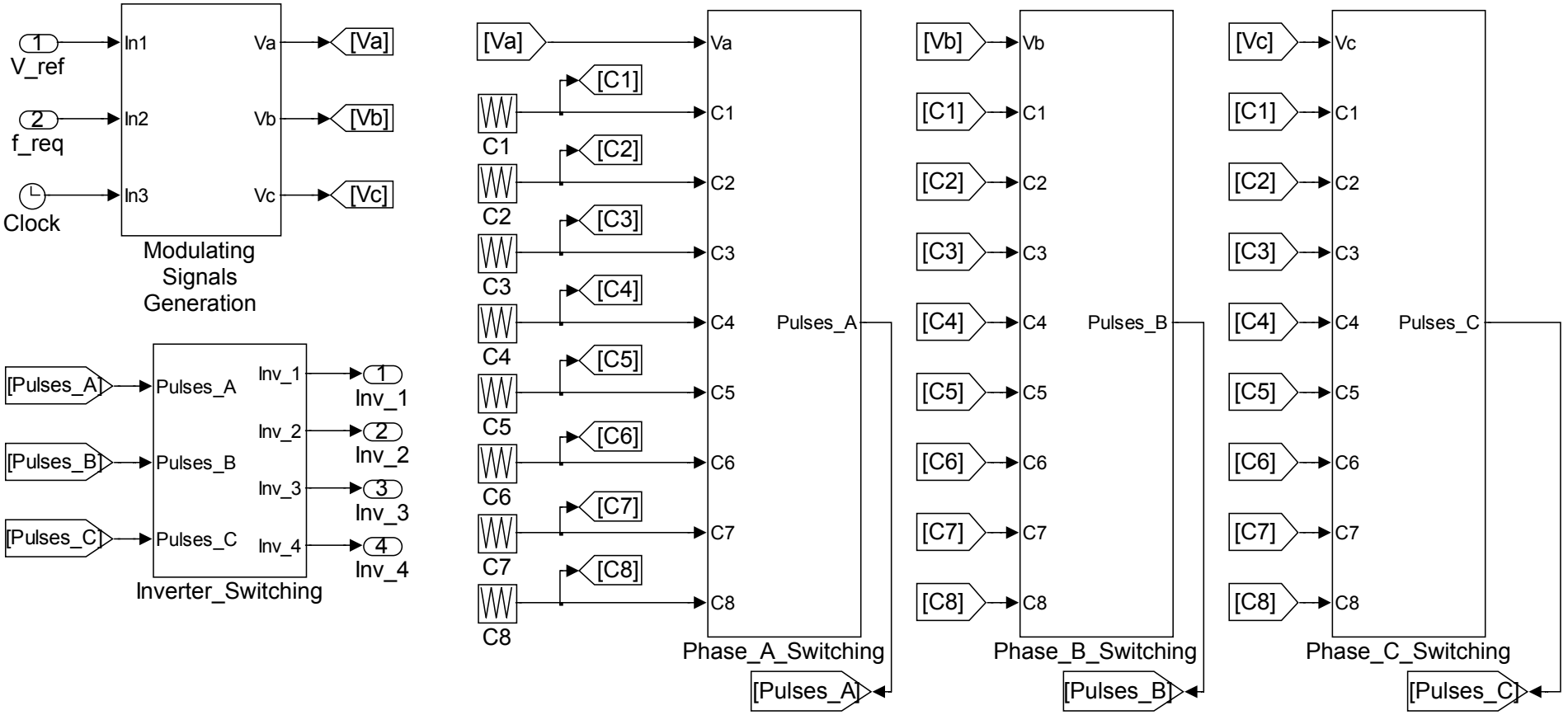



Fig. B.3: SVPWM control logic implementation in MATLAB/Simulink

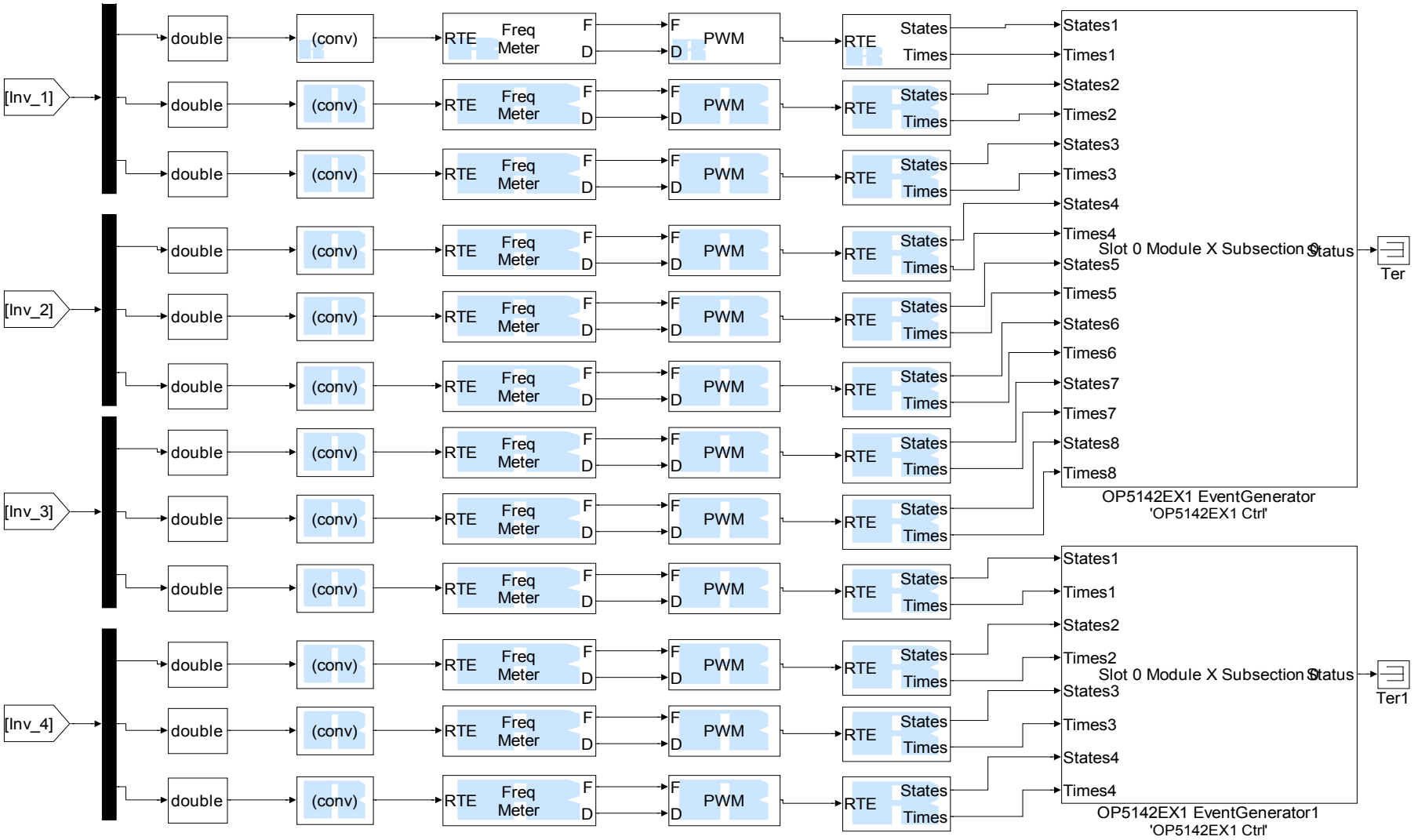



Fig. B.4: Generation of PWM pulses using RT-Events in real-time mode