MLI BASED ACTIVE POWER FILTER FOR POWER QUALITY IMPROVEMENT

A THESIS

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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in this thesis entitled "**MLI BASED ACTIVE POWER FILTER FOR POWER QUALITY IMPROVEMENT"** in partial fulfilment of the requirements for the award of the Degree of Doctor of Philosophy and submitted in the Department of Electrical Engineering of the Indian Institute of Technology Roorkee is an authentic record of my own work carried out during a period from December, 2010 to June, 2015 under the supervision of Prof. S. P. Singh, Professors, Department of Electrical Engineering, Indian Institute of Technology Roorkee, Roorkee.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other Institute.

(**DHANAVATH SURESH**)

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

(S.P. Singh)
Supervisor

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ABSTRACT

Electrical power system is designed to operate at 50 or 60Hz. However, the nonlinear loads connected to the power system generate harmonic currents. The power system harmonics are not new phenomenon. Concern over harmonic distortions has flowed during the history of electrical power systems.

Conventionally, the saturated iron in transformers, induction machines, electric arc furnaces, welding equipment and fluorescent lamps, etc. have been responsible for the generation of harmonics in electric power systems. Most of these equipments also cause the flow of reactive component of current in the system. In recent years, many power electronic converter utilizing switching devices are being widely used in domestic, commercial and industrial applications, ranging from few watts to megawatts. However, these converters suffer from the drawbacks of harmonic generation and reactive power flow from the source and offer highly nonlinear characteristics. The generation of harmonics and reactive power flow in the power systems has given rise to 'Electric Power Quality problems'. These power quality problems are reflected in the system in the form of reduced efficiency of equipment, deteriorated performance of electrical machines, interference with nearby communications networks, neutral burning, mal-operation of relays, blowing of fuses and so on. Thus there is a growing concerned of power quality with proliferation of ac/dc converters in adjustable-speed drives, power supplies, SMPS, DC motor drives, and so on.

Harmonic regulation or standard guide lines such as IEEE-519-1992, IEC 1000-4-7, AS 2279 and IEC 6100, etc. are currently used to keep current and voltage harmonics level within the standard limits. In addition, the equipment designed based on these standards can improve the performance of power system.

To meet these requirements, passive filters, active filters and their combination have been used with two level inverters in order to improve power quality. Conventionally, passive filters have been used for the power quality improvement. Though passive compensations is a simple approach, but they have several drawbacks such as inability to provide dynamic compensation, bulky size, cost, resonance problem, separate filters for each harmonics, etc. and this fact has attracted the attention of power engineers to develop dynamic and adjustable solutions to power quality problems. One modern and very promising group of solutions that deals with load current and/or supply voltage imperfections is active power filter (APF). It is well known that high performance and cost-effective inverter is a prerequisite for the realization of an APF. These inverters can be broadly categorised into two classes, namely, voltage source inverter (VSI) and current source inverter (CSI). A critical comparison of the performance of VSI and CSI when used as a power circuit of APF is beyond the scope of this report. However, in the present work, VSI has been considered as a power circuit for APF as it has higher market penetration and a more noticeable development on VSI has

taken place over the last decade, in comparison to CSI topologies. The high harmonic content of the output voltage makes basic six-pulse (two-level) VSI impractical for direct use in high-power, medium-voltage applications. Instead of using filters and connecting several switching devices in series to achieve the required voltage level, several alternative possible solutions are reported in the literature and can be broadly categorized into two groups: multipulse and multilevel inverters. The first one requires bulky phase-shifting transformers and therefore, its application is limited to high-power, high-voltage systems. The second approach, multilevel inverters, uses the concept of addition of multiple small voltage levels for achieving the required voltage level with the help of additional switching devices and few components like diodes or capacitors. This approach does not require bulky phase shifting transformers and hence these topologies are best suited for medium-power applications. The common multilevel inverters (MLI) topologies are the diode-clamped (DCMLI), flying capacitor (FCMLI), and cascaded H-bridge multilevel inverters (CHBMLI).

The performance of APF depends on the control strategy used for its implementation. The control algorithm proposed in this work aims to eliminate harmonics, compensate reactive power as well as control and balance the dc capacitor voltages of the APFs in steady-state and in transient conditions. The load harmonic currents have been derived by using the measured voltages at point of common coupling (PCC), load currents, and the dc bus voltages of the capacitors of the APF using proposed control strategies based on adaptive neural network such as least mean square (LMS), anti-Hebbian and anti-Hebbian based on TLS (Total least square). The controlling performance of the APF depends on the controller design. However it is difficult to develop the mathematical model of APF with multilevel inverters under parametric varying conditions. Therefore, there is great tendency to use unconventional controllers (intelligent controller) namely type-2 fuzzy logic controller. The type-2 fuzzy logic controller (T2FLC) is one of the intelligent controllers which handles the uncertainty in a better way and has been used in many of the application. The T2FLC, which is a highly nonlinear dynamic controller and does not require the mathematical model of system, not only has a strong adaptive and learning ability but also has a good processing and nonlinear mapping capabilities with large time delay and uncertain conditions. These characteristics result in meeting the control requirement of three level active power filter for three phase three wire system.

A computer simulation study under different load condition has been carried out to verify the performance of the three level DCMLI APF for harmonic elimination and reactive power compensation. The simulation study of the entire system has been carried out in MATLAB/Simulink environment. Various performance indices such as THD, power factor, active and reactive powers have been investigated. From these studies it has been observed that the adaptive control schemes with proposed controllers can compensates the reactive

power of the load and makes the harmonic currents to be less and within the limits imposed by IEEE–519–1992.

The selection of individual inverter topologies for APF applications depends on their performance, cost, size, and implementation issues. DCMLI topology appears to be the most suited for APF applications. But, the large number of power components and voltage unbalance problem at higher levels limits the DCMLI for low power rating applications. On the other hand, Cascaded H-bridge multilevel inverter (CHBMLI) is one of the next generation multilevel inverters intended for high or medium-voltage power conversion without the requirement of line-frequency transformers. The CHBMLI is based on cascade connection of multiple single-phase H-bridge converter cells or chopper cells per leg. The least, low cost, modular structure, easy expansion to any number of levels, high fault tolerance component requirement and absence of bulky complex input transformer and without requirement of pre-charging circuit for the capacitor voltages make CHBMLI best suited for APF applications.

The fuzzy logic controller is promising solution for five levels CHBMLI based APF. Because, they provide a high degree of robustness and immunity to external disturbances. Furthermore, they can be configured to be self-learning and adaptive. However, they require substantial computational power, due to the complex decision-making processes. For example, conventional FLC involves fuzzification, rule-base storage, inference mechanism, and defuzzification operations. For better accuracy in control, a larger set of rules is required, which results in longer computational time. However, this may not be practical because there are many implementation aspects that must be addressed, namely, sampling time and dc voltage excursion. Apart from these constraints, it is known fact that FLC requires simpler mathematics and offers a higher degree of freedom in tuning its control parameters compared to other nonlinear controllers. Most conventional FLCs use the error and the change of error as fuzzy input variables regardless of the complexity of controlled plants. These conventional FLCs came from the concepts of linear PD and PI control schemes. Such FLCs are suitable for simple lower order plants. However, in case of complex large order plants, such as multilevel inverter, all of the states are required to implement state feedback-based FLCs. Then, the design of an FLC is very difficult due to an increased number of fuzzy control rules as well as tuning parameters. Therefore, it is necessary to design an FLC that has a simple control structure and is computationally efficient compared to the conventional FLC. In the presents work, the simplified approach to design a fuzzy logic controller, known as a single-input fuzzy logic controller (SIFLC). The simplification converts two input fuzzy logic controllers to a single input known as signed distance. In this method, the SIFLC control surface can be approximated by a simple piecewise linear (PWL) function, which results in a significant simplification of the design and parameter tuning. The individual

dc voltage regulation of CHBMLI based APF with anti-Hebbian based on total least square using SIFLC and PI controller has been carried out for balancing the voltages of the floating dc capacitors to their corresponding reference values.

Computer simulation studies under different load conditions have been carried out to verify the performance of an APF for harmonic elimination and reactive power compensation. The simulation study of the entire system has been carried out in MATLAB/Simulink environment. The PI and SIFLC have been used to regulate the dc voltage of APF. Extensive simulation studies have been carried out to investigate the performance of the three phase three wire APF in normal voltage condition. The simulation studies have been performed for both steady-state and transient conditions with different non-linear loads. The capacitor voltage balance behaviour has been observed among the individual dc capacitors of the APF. Various performance indices such as THD, power factor, active and reactive power have been investigated. From these studies it has been observed that the PI and SIFLC with the anti-Hebbian based on total least square algorithm completely compensates the reactive power of the load and makes the harmonic currents to be less and within the limits imposed by IEEE–519–1992.

The three-phase, four-wire distribution systems have been widely applied to deliver electric power to three-phase four wire loads. The asymmetrical distribution of larger number of single-phase loads, ranging from few watts to MWs results in voltage and current unbalance in the three phase four wire (3P4W) electrical distribution system. They are responsible for excessive neutral current. The problems associated with the excessive neutral current are: overloading of distribution feeders and transformers, ground voltage fluctuation, flat-topping of voltage waveform and wiring failure etc. Therefore, these excess neutral currents must be compensated for the reliable operation of the 3P4W electrical distribution system.

In recent years, a number of APF schemes have been reported for simultaneous compensation of reactive power, source current harmonics and neutral current in 3P4W electrical distribution systems. They are: (1) split capacitor (2) three H-bridge topology and (3) four-leg topology. However, these schemes were complicated in control and require large volt-ampere rating inverter. Different transformer topologies such as zigzag, star-delta, Scott-connected and star/hexagon-connected have also been used in recent years to attenuate the neutral current on the utility sides due to the advantages of low cost, high reliability and simplified circuit connection. Among these, zigzag transformer based approach requires least kVA inverter rating. However, these configurations also have a low impedance path for zero-sequence voltage of the unbalanced utility, which will further cause a significant neutral current. Further, their attenuation characteristics are dependent on their locations, impedances of the transformers and utility voltage conditions. A reduced rating hybrid

topology comprising of a zigzag-delta transformer, a 3P3W active power filter (APF) and a single-phase APF had been demonstrated for the compensation of source neutral current and phase current harmonics, but, in this topology power factor and displacement factor are not improved. Also, the fundamental-frequency phase currents were also not made balanced. Single-phase powers APF can be combined with the zig-zag/ zero sequence transformers to advance the performance of the neutral current attenuation have been proposed in the literature. However, these schemes suffer from source phase current harmonics and unbalance. To address the above limitations, in the present work, two reduced rating hybrid 3P4W APF have been proposed. The proposed topologies of hybrid 3P4W active power filter comprises of three phase three wire APF, zero sequence transformer, ac power capacitor and single phase APF.

1. A 3P4W active power filter comprises of 3P3W APF, zero sequence transformer and single-phase APF.
2. A 3P4W hybrid active power filter comprises of ac power capacitors, 3P3W APF zero sequence transformer and single-phase APF.

To show the effectiveness of the proposed topologies, extensive simulation studies have been carried out in MATLAB/Simulink® environment. The performances of the proposed schemes have been studied for reactive power compensation, harmonic elimination and neutral current attenuation under various loading and utility voltage conditions. From these studies it is observed that the proposed control schemes completely compensates the reactive power of the load and makes the harmonic currents to be reduced below the limits imposed by IEEE–519–1992. Further, it also attenuates the source neutral current to a very large extent.

In order to further verify the simulation studies, a three-phase downscaled three level DCMLI and five level CHBMLI based APF has been designed, constructed, and tested to verify the viability and effectiveness of the control scheme with intelligent controller techniques. For this purpose, the following prototypes have been developed.

1. Three-level DCMLI based APF for three phase three wire system (LMS, anti-Hebbian and anti-Hebbian based on TLS with PI/type-2 fuzzy logic controller)
2. Five level CHBMLI based APF for three phase three wire system(PI and SIFLC with anti-Hebbian based on TLS algorithm)
3. A 3P4W APF comprising of a zero sequence transformer, CHBMLI based 3P3W APF and series connected single-phase APF (anti-Hebbian based on TLS algorithm with SIFLC).
4. Another 3P4W hybrid APF comprising of a zero sequence transformer, 3P3W APF, AC capacitors and series connected single-phase APF (anti-Hebbian based on TLS algorithm with SIFLC).

For hardware implementation, the IGBTs (IRG4PH40KD) have been used as the switching devices. Different hardware components as required for the operation of the experimental set-up such as pulse amplification, isolation circuit, dead-band circuit, voltage and current sensor circuits, and non-linear loads have been designed and developed. By using the Real-Time Workshop (RTW) of MATLAB and Real-Time Interface (RTI) feature of dSPACE-DS1104, the Simulink models of the various controllers of the prototypes have been implemented. The generated firing pulses have been given to the corresponding semiconductor devices of APF through isolation, delay, and pulse amplification circuits in real-time. An uncontrolled six pulse rectifiers with *RL* elements on their DC sides have been used as nonlinear loads. After compensation with APF, the source currents have been observed to be sinusoidal and their corresponding THDs have also been observed to be well within the limits of IEEE–519–1992 recommended value of 5%. The switching in response and the dynamic performance of APF for a step change in the load has been studied. A smooth control of dc voltages ensures the effectiveness of the DC voltage controllers.

Initially, the simulation and experimentation of three level DCMLI based APF with PI and T2FLC with different adaptive neural network algorithm such as LMS, anti-Hebbian and Anti-Hebbian based on TLS has been carried out to study the performance of three level DCMLI APF for three phase three wire system. From the performance characteristics, it is found that the T2FLC with anti-Hebbian based on TLS adaptive algorithm is better for three level DCMLI APF. However, the T2FLC is very complex to implement with higher level inverter due to the association of length process such as fuzzification, rule base, inference and defuzzification. For this purpose, single input fuzzy logic controller is derived using Conventional FLC. The performance of five level CHBMLI based APF with SIFLC as well as PI controller is also studied with anti-Hebbian based on TLS algorithm. It found that the performance characteristics of CHBMLI based APF with the SIFLC is superior than PI controller. Therefore, for three phase three wire APF, the single input fuzzy logic controller is recommended if number of level in three phase APF is more than three.

Finally, simulation of two 3P4W APF comprising three phase APF, zero sequence transformer, ac capacitors and single phase APF is carried out to study performance characteristics. The single input fuzzy logic controller integrated with anti-Hebbian based TLS algorithm is used for controlling three phase APF. The single phase APF control is implemented using PI controller. The simulated performance characteristics of 3P4W are also experimentally validated.

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(DHANAVATH SURESH)

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LIST OF ACRONYMS

3P3W	Three-phase, Three-wire
3P4W	Three-phase, Four-wire
ac, AC	Alternating Current
APF	Active Power Filter
ASD	Adjustable Speed Drive
CHB	Cascaded H-bridge
CSD	Custom Power Device
CSI	Current Source Inverter
CHBMLI	Cascaded H-bridge multilevel inverter
dc, DC	Direct Current
DCMLI	Diode Clamped Multilevel Inverter
DPF	Displacement Power Factor
DSO	Digital Storage Oscilloscope
DSP	Digital Signal Processor
EMI	Electro Magnetic Interference
FCMLI	Flying Capacitor Multilevel Inverter
GTO	Gate Turn-off Thyristor
HVDC	High Voltage Direct Current
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical & Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
LMS	Least mean square
LSPWM	Level-shifted Pulse width Modulation
MLI	Multilevel Inverter
MOSFET	Metal Oxide Semiconductor Field-effect Transistor
PCC	Point of Common Coupling
PF	Power Factor
PI	Proportional and Integral
PWM	Pulse width Modulation
rms, RMS	Root Mean Square
SMPS	Switch Mode Power Supply
SIFLC	Single input fuzzy logic controller
THD	Total Harmonic Distortion
TLS	Total least square
T2LC	Type-2 fuzzy logic controller

LIST OF SYMBOLS

v_{Sa}, v_{Sb} and v_{Sc}	Three-phase source voltages
i_{Sa}, i_{Sb} and i_{Sc}	Three-phase source currents
i_{La}, i_{Lb} and i_{Lc}	Three-phase load currents
i_{Ca}, i_{Cb} and i_{Cc}	Three-phase APF currents
m	Number of levels in inverter
N	Cascade number
f_{cr}	Carrier signal frequency
f_m	Modulating signal frequency
m_a	Amplitude modulation index
m_f	Frequency modulation index
L_s	Source inductance
L_C	Interfacing inductor of APF
L_f	Coupling inductor of single-phase APF
L_{ac}	Commutation inductance
p, q	Instantaneous real and reactive powers
V_{c1}&V_{c2}	reference voltage of each capacitor of DCMLI
$V_{a1\&}V_{a2}$	Reference dc voltage for each H-bridge cell for phase-a
k_p, k_i	Proportional and integral gains
i_{Sn}	Source neutral current
i_{Ln}	Load neutral current
r	Learning factor

CHAPTER 1: INTRODUCTION

This chapter describes introduction to the research work. It will start with some background on foremost power quality problems in distribution systems. Then, the solutions to the problems will be discussed through which APF will be selected. Next, harmonics detection, scope of work, author's contribution and thesis outlines are explained.

1.1 Overview

From very inception of the interconnected power networks, use of alternating current (AC) circuits has been a commonplace. In these power networks, the basic function of generators is to produce a clean sinusoidal voltage waveform, of constant frequency, at their terminals. However, a pure sinusoidal waveform with zero distortion is a hypothetical entity and not a practical one. The voltage waveform, even at the point of generation, contains a small amount of distortion, due to non-uniformity in the excitation magnetic field and discrete spatial distribution of coils around the generator stator slots. The distortion at the point of generation is usually very low, typically less than 1.0%. In past, majority of the loads in power distribution systems were of constant in nature, as regards to power, impedance, current or any of their combination. Such loads include incandescent lighting, heating, AC motors, etc., and are termed as linear loads. However, in recent years, the requirement for more efficient operation of electrical equipment and energy conditioning has led to the advancement in semiconductor technologies and introduction of new power electronic devices. This has significantly changed the nature of load composition because these power electronics based loads are nonlinear in nature. This nonlinearity results in non-sinusoidal load currents, which are periodic in nature and usually reflect Fourier series expansions. Non-sinusoidal periodic waves contain fundamental and higher order frequency components. These higher order frequency components are called harmonics. Harmonics can be defined as the undesirable components of a distorted periodic waveform whose frequencies are the integer multiples of the fundamental frequency [1-10]

The injected harmonics are responsible for the distortion of voltage and current wave shapes. A substantial amount of these harmonics are produced by high rating power converters. Other devices responsible for generation of harmonics are static var compensators, adjustable speed drives, power supplies, transformers, arc furnaces, personal computers, cyclo-converters, etc. In future, there may be many more new harmonic sources, such as fuel cells, battery storage devices, photovoltaic cells, etc. Non-sinusoidal currents generated by the nonlinear loads are propagated throughout the network, causing voltage drops across the impedance of transmission lines and transformers. Thus, the voltage at the point of common coupling (PCC) is no longer sinusoidal, but periodic and also possesses Fourier series expansions. The quantum of voltage distortion depends on the line impedance and the magnitude of current. When several power users share a common power line, the

voltage distortion produced due to harmonic current injection by one user can impact the quality of power supplied to others. Due to this, standards have been issued to limit the amount of harmonic currents fed into the source by an individual customer [6].

Harmonics are responsible for increased system losses, equipment heating and reduction in useful life, mal-operation of protective devices, failure of reactive power compensating capacitors, interference with protection, control and communication circuits as well as customer loads and amplification of harmonics by means of parallel resonance between the supply system reactance and power factor improvement capacitors [7-50].

1.2 Electrical disturbances

The quality of electric power is closely related to the quality of the voltage wave which is characterized by the following parameters [7]

- Perfectly sinusoidal waveform; no distortion , spikes , dips
- Balance and perfect symmetry of the amplitude and phase phases
- RMS within allowable limits
- Frequency stability.
- Power factor within tolerable limits

Disturbances are all internal and external phenomena to the network with a power to amend a transitional or permanent in amplitude and / or shape of the electrical parameters of the network (current, voltage, frequency). These disturbances can be classified according to two criteria: the length of time or the method of allocation is to say, their effects on electrical parameters

According to the first classification, there are two basic categories:

- Periodic disturbances (which last for a given duration), as the case of harmonic distortion, voltage drops due to reactive power flows in the network , and imbalances :
- Aperiodic disturbances: or mainly in all fugitives' phenomena often very difficult to predict as transient voltage dips or surges.

According to their assignment modes, there are three main families:

- Disturbances on the amplitude or the RMS values ,
- Unbalanced three-phase systems,
- harmonic distortion

1.2.1 Current harmonics (and / or) voltage

1.2.1.1 Sources of harmonics and their effects

The proliferation of electrical equipment using static converters has led in recent years a significant increase in the level of harmonic pollution of power systems. These electrical equipment are considered as non- linear loads emitting harmonic currents whose

frequencies are integer multiples of the fundamental frequency, or sometimes to any of the frequencies (the most significant harmonics being harmonics 5, 7, 11 and 13). The passage of these harmonic currents through the impedances of the electrical network may cause harmonic voltages at the connection points and then pollute users powered by the same electric network.

The presence of harmonics of current or voltage leads to adverse effects on the distribution network, such as

- The heating of the conductors, cables , capacitors and machinery due to additional copper and iron losses,
- The interference with telecommunication networks , caused by the electromagnetic coupling between the electrical network and the telecommunication networks which can induce in these significant noises,
- Dysfunction of some electrical equipment, such as control and regulating devices,
- In the presence of harmonics, voltage and current can change sign several times during a half - period. Therefore, sensitive equipment at the zero crossing these electrical quantities are disrupted,
- The resonance frequencies of the circuits formed by the inductances of the transformer and cable capacities are usually quite high, but they may coincide with the frequency of a harmonic; in this case, there will be a significant amplification of voltage/current, which can destroy the equipment connected to the network,
- The degradation of the accuracy of measuring devices,
- Induced disturbances on the communication lines, electromagnetic radiation in particular.

1.2.1.2 Harmonic distortion rate

Different criteria are defined to characterize this type of disturbance. THD (the rate Harmonic distortion) and power factor are most used to quantify respectively harmonic disturbances and reactive power consumption. THD represents the ratio of the RMS value of the harmonics to the RMS value of the fundamental. THD is defined by the relation

$$THD = \sqrt{\frac{\sum_{n=1}^{\infty} X_h^2}{X_1^2}} \text{X100} \qquad (1.1)$$

Along With X_1 the effective value of the current (voltage) fundamental and X_h effective values different harmonics of the current (voltage). In general, harmonics included in a power grid is lower than 2500 Hz, which corresponds to the range of low interference frequencies

within the meaning of standardization. Higher frequency harmonics are strongly attenuated by the skin effect and the presence of the rows of inductors. In addition, the apparatus generating harmonics have, mostly, lower emission spectrum at 2500 Hz, why the field of study of harmonics is usually from 100 to 2500 Hz, that is to say rows 2-50

TDD is the ratio of the RMS value of the harmonics to the maximum value of current drawn by the load. It is defined by the relation

$$TDD = \sqrt{\frac{\sum_{h=2}^{\infty} I_h^2}{I_L^2}} \times 100\% \qquad (1.2)$$

1.2.1.3 The power factor

For a sine wave power factor is given by the ratio between the power active P and the apparent power S. the generators, transformers, transmission lines and control and measurement devices are designed for the maximum rated voltage and current. A low value of power factor results in misuse of these equipment. In the case where there are harmonics, power factor is degraded additional power called the deforming power (S) given by relation (1.3) is added:

$$S = 3V_1\sqrt{\sum_{h=2}^{50} I_h^2} \qquad (1.3)$$

The power factor (*pf*) becomes

$$PF = \frac{P}{\sqrt{P^2 + Q^2 + S^2}} \qquad (1.4)$$

To limit the influence of a pollution load on the various loads connected to network standards on power quality have been developed. The main standard is IEEE 519: 1992 [Recommended Practices and Requirements for Harmonic Control in Power Systems] it determines the procedure to control the harmonics present on the grid and it also imposes the recommended limits of harmonic pollution generated by customers and total harmonic distortion on the network. This standard limits harmonic distortion (THD) of current networks < 69kV to 5% It is customary to say that in the industrial plants, whose harmonic voltage THD is less than 5% does not produce a significant effect . Between 5% and 7% are beginning to see effects, and to more than 10% the effects are almost certain

Table 1.1 IEEE limits of harmonic current emissions (IEEE 519 :1992)[8]

V_n < 69kV						
I_{sc}/I_{cn}	H<11	11<=h<17	17<=h<23	23<=h<35	35<=h	TDD4.0
<20	4.0	2.0	1.5	0.6	0.3	5.0
20-50	7.0	3.5	2.5	1.0	0.5	8.0
50-100	10.0	4.5	4.0	1.5	0.7	12.0
100-1000	12.0	0	5.0	2.0	1.0	15.0
69kV <= Vn <161kV						
< 20	2.0	1.0	0.75	0.3	0.15	2.5
20-50	3.5	1.75	1.25	0.5	0.25	4.0
50-100	5.0	2.25	2.0	1.25	0.35	6.0
100-1000	6.0	2.75	2.5	1.0	0.5	7.5
> 1000	7.5	3.5	3.0	1.25	0.7	10

Where I_{sc} is the short - circuit current I_{ch} is the nominal load current, the rated voltage V_n and TDD is the total demand distortion (current distortion from the maximum demand).

Table 1.2 IEEE limits for harmonic voltage distortion (IEEE 519: 1992)

Connection point to the voltage (V_n)	Individual Harmonic Distortion	THD V_n(%)
V_n < =69kV	3.0	5.0
69kV < V_n <=161kV	1.5	2.5

1.2.2 Imbalance in the three-phase voltage system

It is said that there is imbalance in a network, when recording steady, asymmetries of amplitudes and phase shifts of the phase voltages. This type of disturbance is caused mainly by impedance mismatches lines of the network, and also by short circuits single-phase or two-phase. This imbalance is manifested by disturbances in rotating machines, overheating, etc.

1.2.2.1 Consequences of unbalanced three-phase system

The imbalance of a three-phase system can cause malfunction of the low voltage devices connected

- Malfunction of a single-phase device powered by a low voltage (incandescent lamp that provides poor lighting)
- Destruction of a single-phase device powered by a voltage too high, it can be destroyed (break-down of a filament lamp overvoltage).

Regarding power electronics devices, mainly the rectifier bridges, and the operation in the presence of imbalance leads to the appearance of components non-characteristic harmonics, including multiple harmonics of third. The appearance of these harmonic currents can cause problems such as generating an anti-resonant when filtering order of the harmonic 5. In addition to the classic effects of harmonics, the frequency characteristics cannot lead, in some cases, the blocking of the order. The consequence of the negative sequence on rotating machinery is the creation of a field rotating in opposite direction to the direction of rotation, from which a braking torque and parasitic losses which cause additional heating of the machine. Regarding the effect of unbalance zero sequence, it must be reported overheating risk neutral conductor in a distribution network, when the size is too small diameter, may cause rupture of the wire or fire.

1.3 Neutral currents effects

In case of a three-phase four-wire (3P4W) system with balanced nonlinear loads, fundamental and harmonics (including triplen harmonics) are present in the phase currents. Summing these currents at the neutral point, the fundamental and non-triplen harmonic components are found to be zero [12-15]. However, the triplen harmonic components in neutral are three times the triplen harmonic phase currents, because they coincide in phase and time. Triplen become an important issue for grounded wye system, as they are added in the neutral and produce a substantial neutral current. The current may exceed the rating of the neutral conductors, resulting in the overheating of power system equipments. The excessive neutral current may cause other adverse effects, such as overloading of power feeders, overloading of distribution transformers, voltage distortion and common mode noise

1.4 Compensation solutions

Two types of solutions are possible, the first is to use less static converters, while the second is the implementation of a harmonic filtering components. The first class of solutions focuses on the design and the second is to offset current or voltage harmonics. Two groups remediation solutions to compensate for any disturbances can be distinguished

- Traditional passive filter most commonly used
- modern solutions (active power filters) that are designed to overcome the limitations of passive filters

1.4.1 Passive filters

These are the first devices used for eliminating harmonic. They are made up of passive elements such as inductors, capacitors and resistors. In general, the harmonic filters are connected in parallel with the harmonic generating load (rectifier diodes or thyristors, an electric arc furnace, etc.). We distinguish four types of passive filter filters set at specific frequencies, the high-pass filters, low pass filters and band pass filters. The most common choice for the rectifier to high power thyristor is to use a combination of multiple filters set to a single frequency (of harmonics 5, 7, 11 and 13) and a high pass filter of the second order set of around the harmonic frequency of the Passive harmonic filters have the advantage of correcting the power factor capacitors correctly sizing to exchange a certain amount of reactive power to the network [27-29, 36-38]. The single-phase circuits of single-tuned, double-tuned and second order high-pass damped shunt passive filters are displayed in Fig. 1.1. However, these filters have some disadvantages:

- The impedance of the network in the presence of the filters may reveal resonances
- The passive filter can absorb harmonic currents from other non-linear loads and in this case , the passive filter can be overloaded,
- The passive filtering is inflexible and in case of changes in the network, it can be difficult to adapt to new needs filtering.

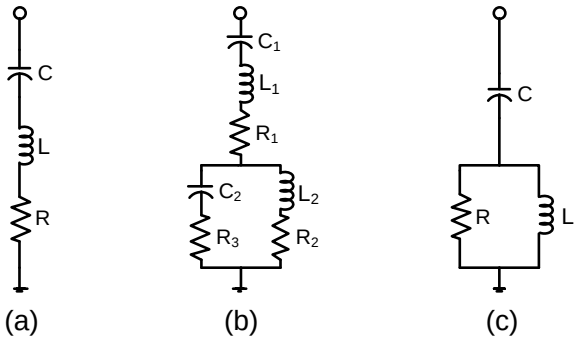


Fig. 1.1: Shunt passive filters: (a) Single-tuned; (b) Double-tuned; (c) Second-order high-pass damped.

1.4.2 Active power filters

These solutions are proposed as effective solutions for Abatement of electrical networks to process the disadvantages of traditional solutions posed by passive filters (not adaptability to load variations and network appearance of resonances) [21, 22, 39]. The purpose of these active filters is to generate either the currents or harmonic voltages so that

the current or the voltage again becomes sinusoidal. The active filter is connected to the network or in parallel or in series as it is designed to compensate respectively currents or harmonic voltages or combined with passive filters to form what we call the hybrid filters

The most important advantages of active filters compared to passive filters are

- The physical volume of the filter is reduced,
- The filtering capacity is higher
- Flexibility and adaptability are much higher.

Yet they also have some disadvantages:

- Their high cost (which limited their implementation)
- The losses are higher (power provided for compensation).

1.4.2.1 Shunt active power filter

APF is connected in parallel with the network in real time and injects harmonic components drawn by non-linear loads connected to the network. Thus the distorted current supplied by the power source is sinusoidal [32]. The aim of the parallel active filter (APF) is to prevent interference currents (harmonics, reactive and unbalanced), produced by pollution loads to flow through the network impedance, located upstream of the active filter connection point. The principle of a shunt active power filter diagram is given by Fig. 1.2.

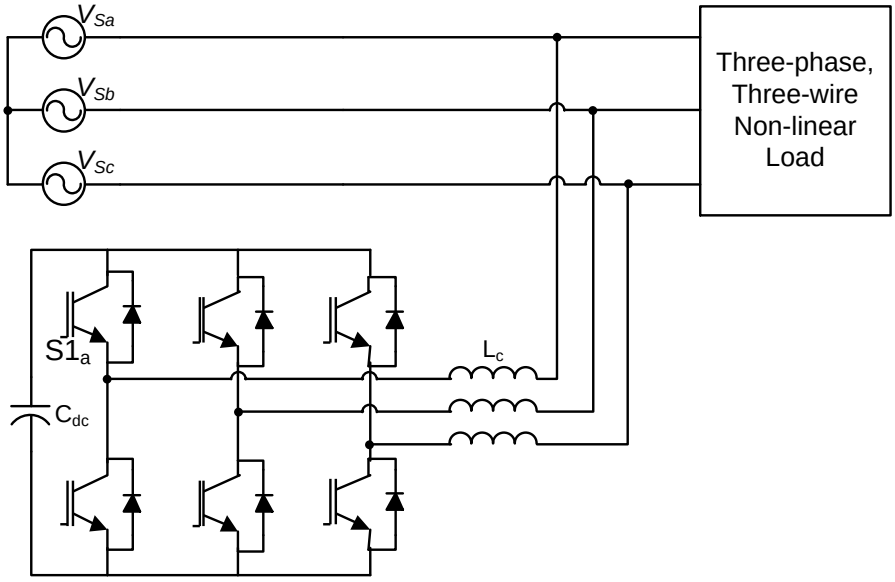


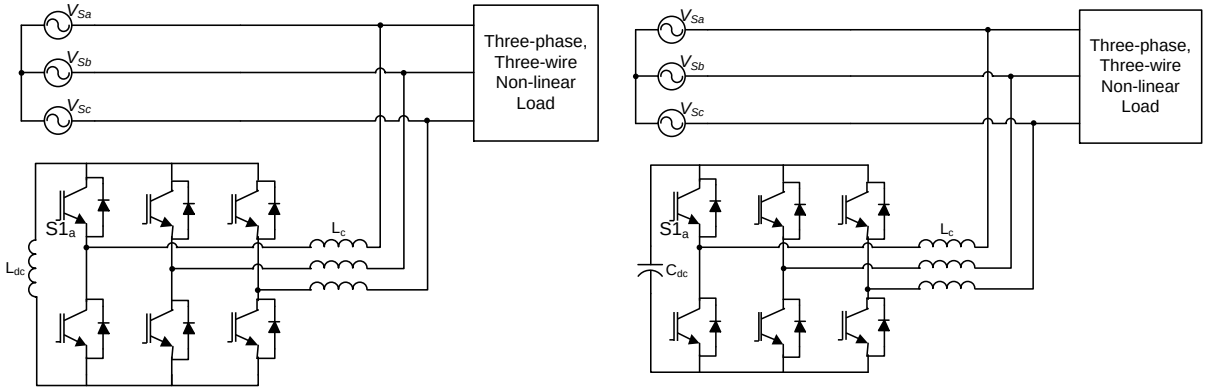
Fig. 1.2: Shunt active power filter.

1.5 Configurations of active power filter

APF‘s can be broadly classified based on its power circuit topology and the type of the supply and they are discussed below:

1.5.1 Power Circuit Based Classification

The power circuit of active power filter can also be classified as current source-fed-type inverters (CSI) and voltage source-fed-type inverters (VSI). The CSI approach is shown in Fig. 1.3 (a) uses a reactor, while the VSI, displayed in Fig. 1.3 (b) uses a dc capacitor.



(a) (b)

Fig. 1.3: (a) Current source inverter based APF; (b) Voltage source inverter based APF.

When CSI approach acting as active power filter, it behaves as non-sinusoidal current source to meet the requirement of the nonlinear load. However, in CSI approach diode is used along with IGBT for reverse blocking. The CSI approach considered to be highly reliable, but have higher losses and require higher values of parallel ac power capacitors. Other converter used as active power filter is VSI; it has a self-supporting dc voltage bus with a large dc capacitor. It has become more dominant, since it is lighter and cheaper [23].

However, these simple topologies are not suitable for high-power, medium-voltage applications because of their high harmonic content and increased cost [30, 32, 33]. For high-power, medium-voltage applications, the CSI based APFs can be realized using pulse-width modulated current source inverters (PWM-CSIs) or load commutated inverters (LCIs) [24]. On the other hand, VSI for high-power, medium-voltage applications can be broadly categorized into two groups: multipulse and multilevel type inverters. These inverters present great advantages compared with conventional and very well-known two-level VSI [69]. These advantages are fundamentally focused on improvements in the output signal quality and a nominal power increase in the inverter.

In multipulse inverters, several six-pulse inverter units can be arranged using transformers as magnetic interfaces, which is a useful technique to achieve high power rating and perform harmonic neutralization. The higher the number of six-pulse units, the lower the distortion of the resultant output voltage.

Multilevel inverters have become increasingly popular in recent years. It uses the concept of utilizing multiple small voltage levels to perform power conversion. Advantages of this approach include good power quality, good electromagnetic compatibility (EMC), low switching losses, and high voltage capability. They synthesize an output voltage waveform

from several levels of capacitor voltage sources. As the number of levels increases, the synthesized output waveform approaches the sinusoidal wave with the reduced harmonic distortion. The most commonly used multilevel inverter topologies are reported in literature. They are:

1. Diode Clamped Multilevel Inverter (DCMLI)
2. Flying Capacitor Multilevel Inverter (FCMLI)
3. Cascaded H-bridge multilevel Inverters (CHBMLI)

These three multilevel inverter topologies could be considered now as the classic or traditional multilevel topologies that first made it into real industrial products during the last two decades.

1.5.1.1 Diode-Clamped Multilevel inverter

The diode-clamped multilevel converter (DCMLI) makes use of capacitors in series to divide the DC bus voltage into a distinct set of voltage levels. For example, in order to produce a m-level phase voltage, a diode-clamped inverter needs m-1 capacitors on the DC bus. A three-phase, five-level diode-clamped inverter is shown in Fig. 1.4. The DC bus consists of four capacitors: C_1, C_2, C_3 and C_4. For a DC bus voltage V_{dc}, the voltage across each capacitor is divided by the number of DC bus capacitors. The device voltage stress will be limited to one capacitor voltage level or Vdc/4, through clamping diodes [63, 68,69 89].In order to explain how the staircase-shaped converter output voltage synthesized, the neutral point N is used as the reference point for the converter output phase voltage. Using the five level converter shown in Fig. 1.4, there are five possible switch combinations that can be used to generate a five level voltage from point A to point N. Table 1.1 is used to illustrate the five possible switching states of the converter as well as their corresponding output phase voltage

From Table 1.1, a 1 is used to represent a condition when the converter switch is on, and a 0 represents a condition when the converter switch is off. For each phase leg, a set of four adjacent switches is on at any given time. There are four complementary switch pairs in each phase

Table 1.1: Diode-Clamped five-level converter voltage levels and their switch states [118].

Output	Switch State							
	Sa1	Sa2	Sa3	Sa4	Sa′1	Sa′2	Sa′3	Sa′4
$V_5=V_{dc}$	1	1	1	1	0	0	0	0
$V_4=3V_{dc}/4$	0	1	1	1	1	0	0	0
$V_3=V_{dc}/2$	0	0	1	1	1	1	0	0
$V_2=V_{dc}/4$	0	0	0	1	1	1	1	0
$V_1=0$	0	0	0	0	1	1	1	1

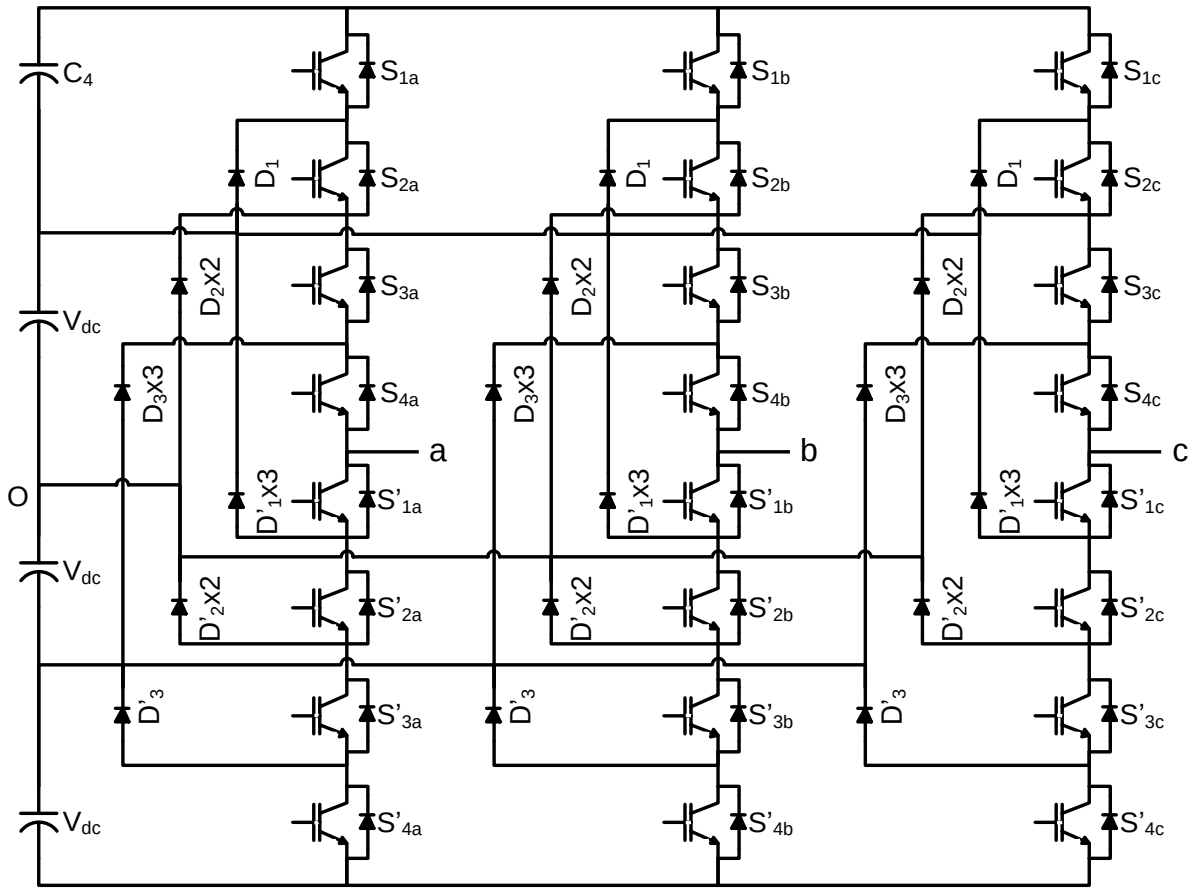


Fig. 1.4: Diode clamped multilevel inverter.

1.5.1.2 Flying-Capacitor Multilevel Inverter

A flying-capacitor multilevel inverter (FCMLI), as shown inFig. 1.5, makes use of a ladder type structure of DC capacitors. The voltage across each capacitor differs from the voltage on the next capacitor. In order to generate an m-level staircase output voltage, m-1 capacitors in the DC bus are needed. The structure of each phase leg is the same. The size of the voltage increments between two capacitors is used to determine the number of levels of the converter's output voltage [119, 124, 125] .

Fig. 1.5 shows three inner capacitors (C_{a1}, C_{a2} and C_{a3}) in phase A that are used for voltage balancing purposes. It must be noted that the capacitors used for voltage balancing purposes are different from phase to phase whereas all three phases of the flying-capacitor topology share the same DC link capacitors. Table 1.2 shows one possible combination for the switching states of the flying-capacitor topology. It must be noted that there is more than one possible set of switch combinations that can generate the desired converter output voltage. Due to this fact, the FCMC has more flexibility than the DCMLI.

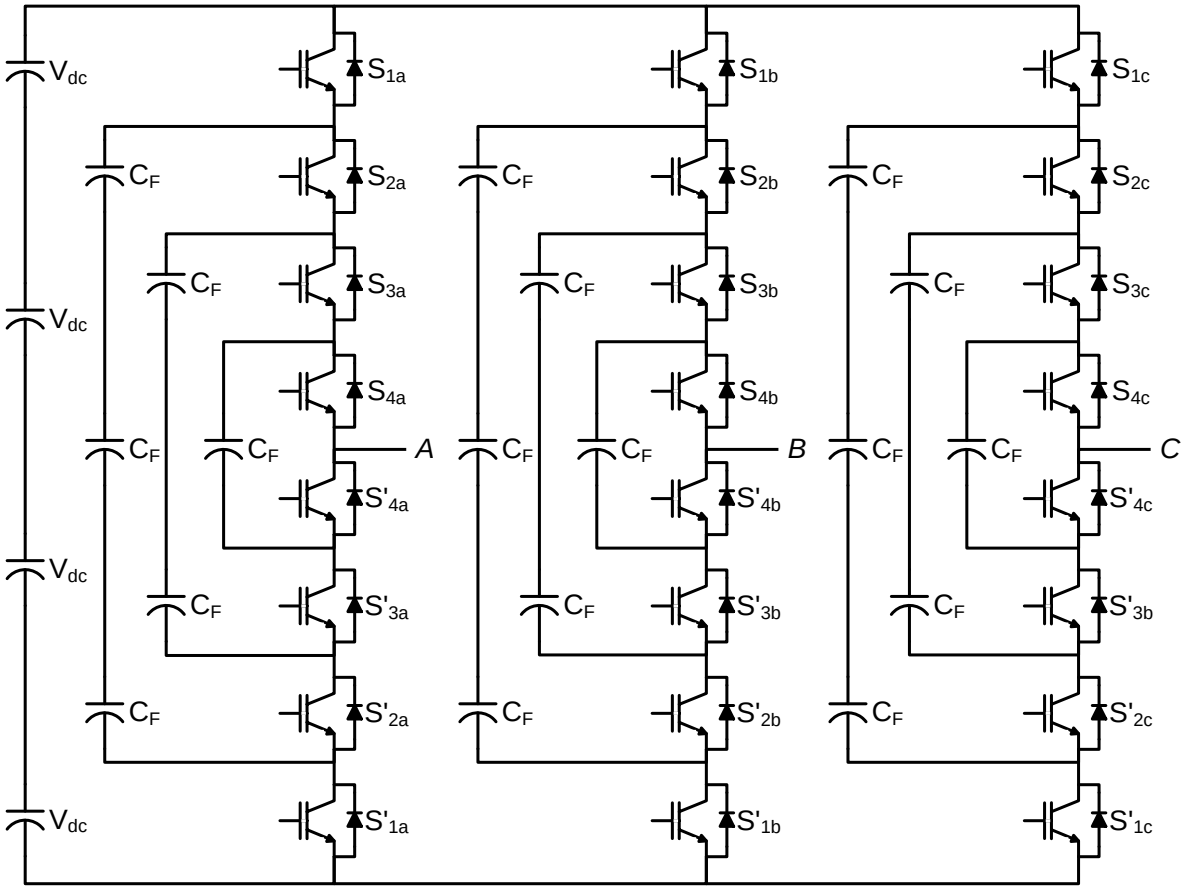


Fig. 1.5: Flying capacitor multilevel inverter.

Table 1.2: Flying-Capacitor five-level converter voltage levels and their switch states.

Output	Switch State							
	Sa1	Sa2	Sa3	Sa4	Sa′1	Sa′2	Sa′3	Sa′4
$V_5=V_{dc}$	1	1	1	1	0	0	0	0
$V_4=3V_{dc}/4$	0	1	1	1	1	0	0	0
$V_3=V_{dc}/2$	0	0	1	1	1	1	0	0
$V_2=V_{dc}/4$	0	0	0	1	1	1	1	0
$V_1=0$	0	0	0	0	1	1	1	1

1.5.1.3 Cascaded-Multilevel Inverter

Finally, the last major type of capacitor-voltage synthesized-based converter discussed in this thesis is the multilevel converter. The multilevel converter consists of several cascaded converters using separate DC sources [63, 66-68, 101, 106, 107, 113. 114]. This converter is known as the CMC. The primary function of the CMC is to synthesize a desired output voltage from the separate DC voltage sources. There are several different types of DC sources that can be used in the CMC. For example, some DC sources include but are not limited by batteries, fuel cells, and solar cells. One of the most popular applications of the

CMC is the high-power AC power supplies and adjustable-speed motor drives. One of the benefits of this converter topology is that the multilevel topology eliminates the use for any additional clamping diodes or voltage balancing capacitors. Fig. 1.6 shows a diagram of five level cascaded H-bridge multilevel inverter (CHBMLI) or CMC. Each single-phase CMC is associated with its own H-Bridge converter. The converter output voltages of each H-Bridge converter are connected in series with one another per phase. If the switch combinations of switches S1-S4 are varied, it is possible to generate three different converter output voltage levels ($+V_{dc}$, $-V_{dc}$ and 0). For the CMC topology, the number of output phase-voltage levels is defined as m = 2N+1, where N is the number of separate DC sources. The Table 1.3 voltage levels and their corresponding switch states for a five-level CMC.

Table 1.3: Voltage levels and their corresponding switch states for a five-level CMC (CHBMLI)

Output Voltage	Switch State (1 means switch is ON and 0 means OFF)							
	S_{11}	S_{31}	S_{12}	S_{32}	S_{41}	S_{21}	S_{42}	S_{22}
$V_{AO} = +2V_{DC}$	1	1	1	1	0	0	0	0
$V_{AO} = +V_{DC}$	1	1	1	0	0	0	0	1
	0	1	1	1	1	0	0	0
	1	0	1	1	0	1	0	0
	1	1	0	1	0	0	1	0
$V_{AO} = 0$	1	1	0	0	0	0	1	1
	0	0	1	1	1	1	0	0
	1	0	0	1	0	1	1	0
	0	1	1	0	1	0	0	1
	1	0	1	0	0	1	0	1
	0	1	0	1	1	0	1	0
$V_{AO} = -V_{DC}$	1	0	0	0	0	1	1	1
	0	1	0	0	1	0	1	1
	0	0	1	0	1	1	0	1
	0	0	0	1	1	1	1	0
$V_{AO} = -2V_{DC}$	0	0	0	0	1	1	1	1

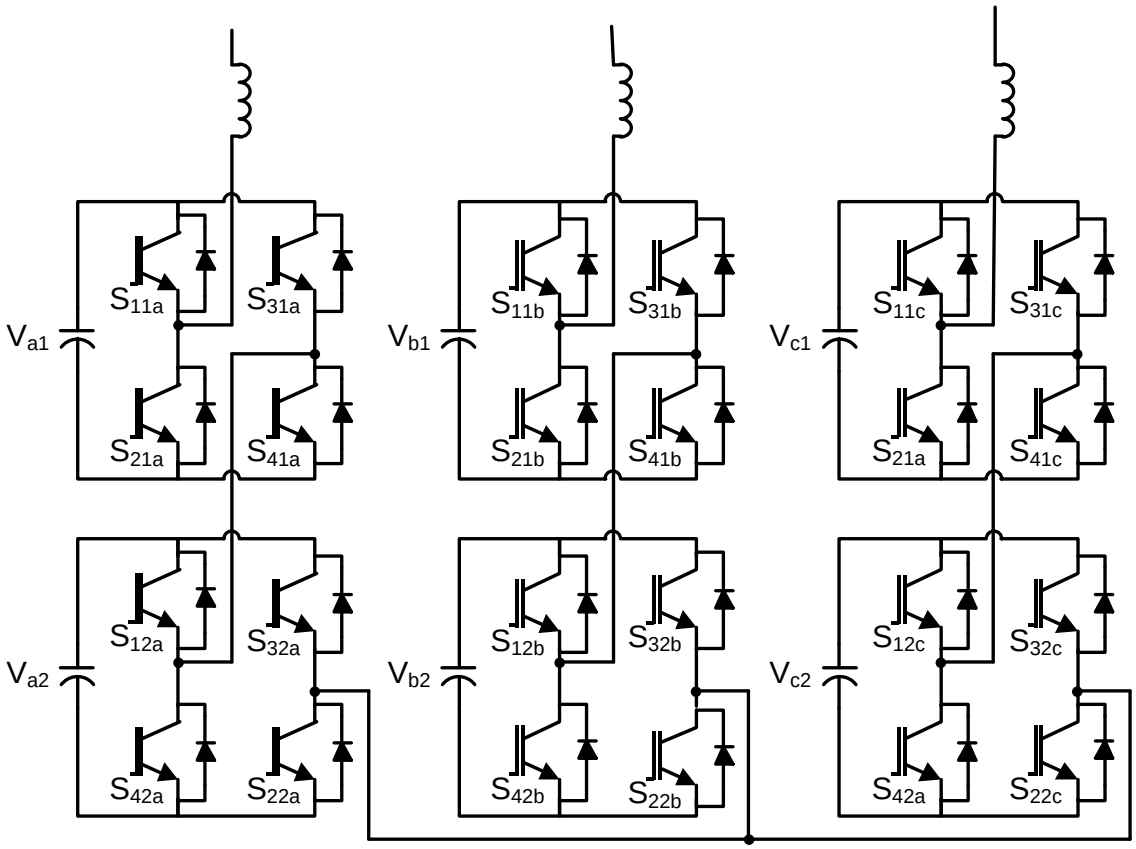


Fig. 1.6: Cascaded five level converter

1.6 Comparison of Multilevel converters for active power filter

The selection of individual inverter topologies for applications depends on their performance, cost, size, and implementation factors. Table 1.4 gives the comparison of power component required per phase-leg for the above discussed multilevel converter topologies[118]. As of Table 1.4, it can be observed that the CHBMLI inverter requires least number of power components

Table 1.4: Comparison of power component requirements per phase-leg among multilevel inverter topologies.

Power component	Inverter topology		
	DCMLC	FCMLC	CHBMLI
Main switching devices	$2(m-1)$	$2(m-1)$	$2(m-1)$
Anti-parallel diodes	$2(m-1)$	$2(m-1)$	$2(m-1)$
Clamping diodes	$(m-1)(m-2)$	0	0
DC bus capacitors	$(m-1)$	$(m-1)$	$\frac{(m-1)}{2}$
Flying capacitors	0	$\frac{(m-1)(m-2)}{2}$	0

1.7 Supply System Based Classification of active power filters

The classification of APF can also be based on the supply and/or the load system having single-phase, three-phase three-wire (3P3W) or three-phase four-wire (3P4W) systems

1.7.1.1 Single-phase active power filter

The single-phase (two-wire) APFs are used for compensation of harmonics and reactive power generated by the operation of nonlinear loads, such as residential, office and commercial complexes, connected to single-phase supply systems. Fig.1.7 shows the power circuit of APFs for harmonics and reactive compensation in single-phase applications.

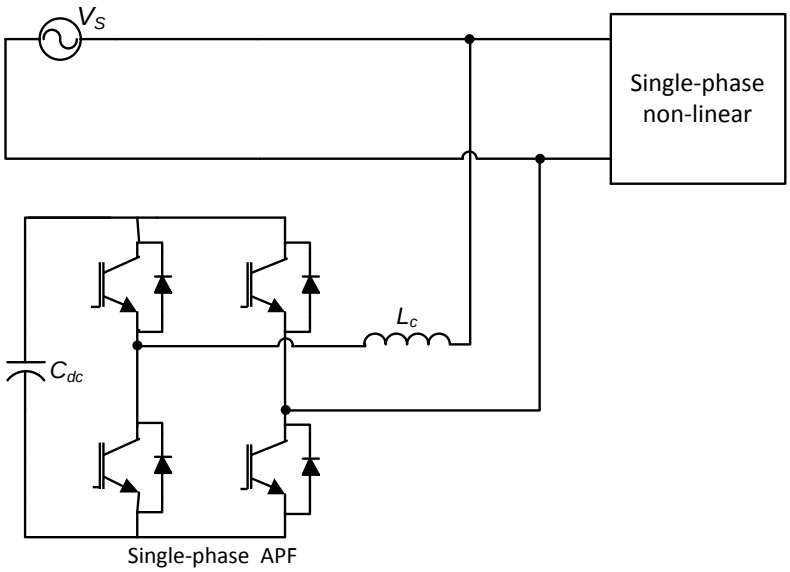


Fig.1.7: APF for two-wire systems.

1.7.1.2 Three-phase, Three-wire active power filter

In three-phase, three-wire (3P3W) distribution systems without neutral wire are used to provide supply for high-power loads such as adjustable speed drives, transactions, arc furnaces, and other industrial applications. For compensation of harmonics and reactive power in these systems, a 3P3W APF is used. Fig. 1.2 shows the connection of APF for reactive and harmonic current compensation in 3P3W distribution system

1.7.1.3 Three-phase, Four-wire active power filter

APFs are specially designed to 3P4W systems for compensating neutral current along with the necessary compensation features of the 3P3W APFs. Three different topologies are available for 3P4W systems and are given below:

1. 3P4W split-capacitor APFs topology
2. 3P4W four-leg APF topology
3. 3P4W APF transformer based topology

1. Three-phase, Four-wire split capacitor APF Topology

The three leg split capacitor APF topology utilizes the standard three-phase conventional inverter where the dc side capacitor is split and the neutral wire is directly connected to the electrical midpoint of the capacitors through an inductance. Fig. 1.8 shows the split capacitor APF topology used in 3P4W system and also known as midpoint clamped topology. The split capacitors allow load neutral current to flow through one of the dc capacitors $C_{dc1,}$ C_{dc2} and return to the ac neural wire. The split capacitor topology suffers from voltage balancing, control complexity and two large dc capacitors.

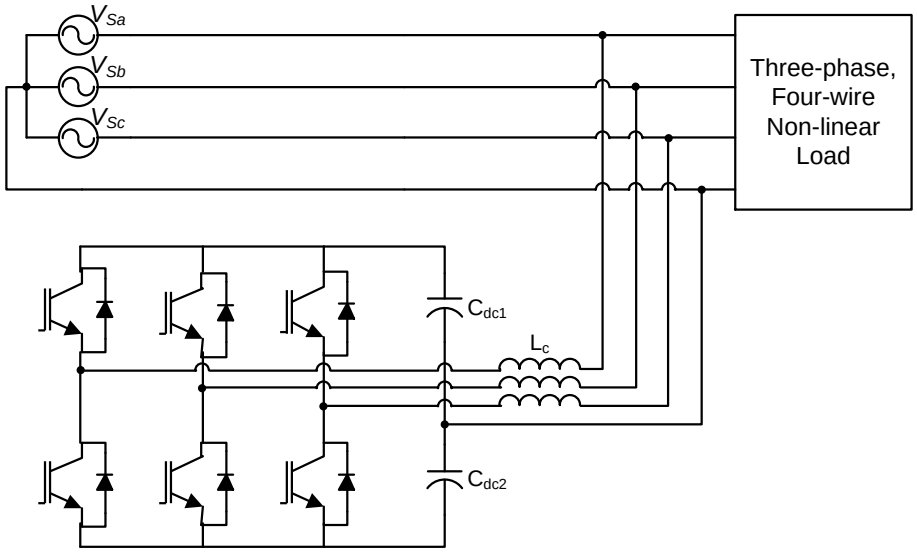


Fig. 1.8: The 3P4W split capacitor.

2. Three-phase, Four-wire Four-leg APF Topology

Fig. 1.9 shows the four-leg or four pole APF topology used in 3P4W system. In this topology, three of the switch legs are connected to the three phase conductors through a series inductance while the fourth leg is exclusively connected to the neutral conductor with an inductor. This topology is most suitable for compensation of high neutral currents. Despite having higher number of switching devices this topology, outweighed the split capacitor topology by number of factors:

Better controllability: In this topology only one dc-bus voltage needs to be regulated, as opposed to two in the capacitor midpoint topology. This significantly simplifies the control circuitry with better controllability.

Lower dc voltage and current requirement: This topology requires a lower dc-bus voltage and capacitor current.

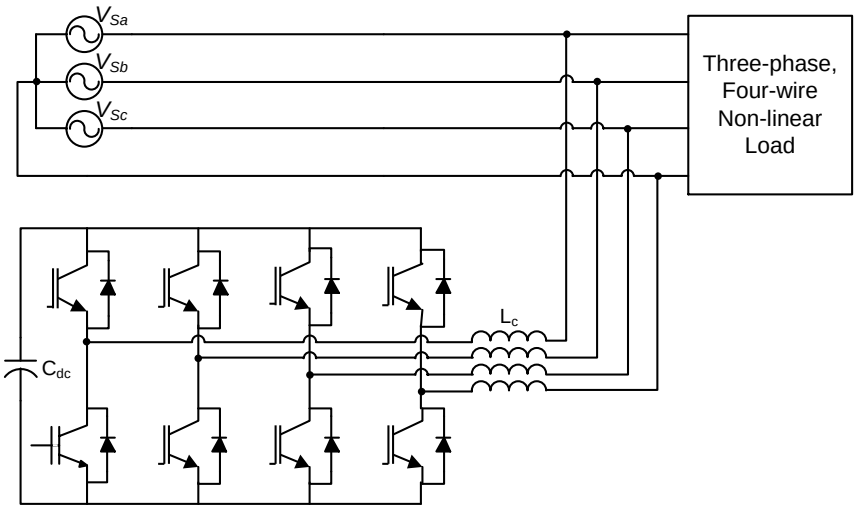


Fig. 1.9: The 3P4W four-leg topology.

1.8 Three phase four active power filter comprising zigzag transformer.

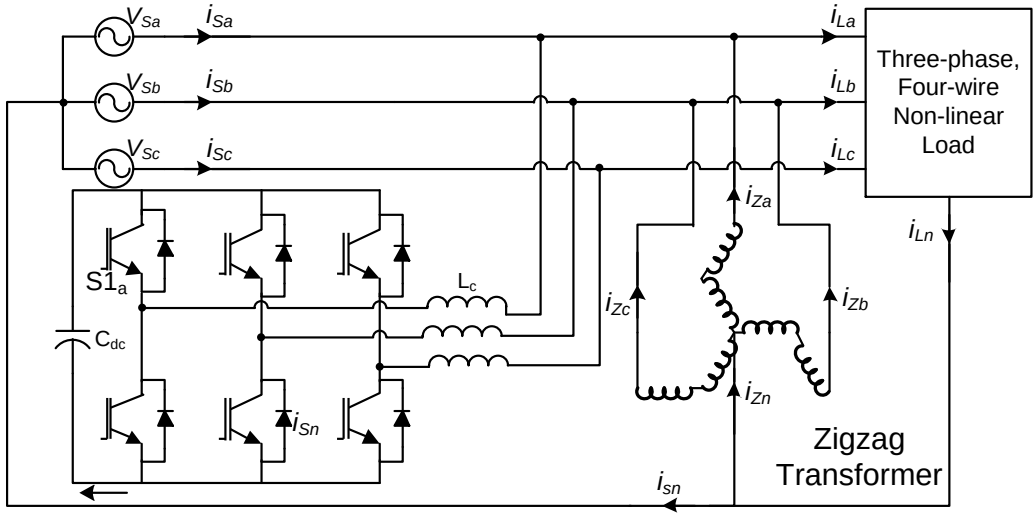


Fig. 1.10 : three phase four active power filter comprising zigzag transformer.

Fig. 1.10 shows the arrangement of the 3P4W APF. A 3P3W APF is connected to point of common coupling for compensating positive and negative sequence component of harmonics requirement of nonlinear load. The 3P3W APF draw or supply real power to keep dc side capacitor voltage constant. A zigzag transformer connected parallel to nonlinear load for attenuating zero sequence current and APF does not required to compensate the load neutral current. Thus effectively reducing the volt-ampere rating of the active power filter. The power rating of active power filter saving in this configuration depend on the zero-sequence components of load currents. However, the compensating performance of this active power filter depends on installation location, impedance and utility voltage conditions [51].

1.9 APF Controller

The compensation performance of the APF depends basically on the design characteristics of the controller.

Control strategy of the APF is implemented in three stages and they are:

1. In the first stage, the essential voltage and current signals are sensed using voltage Hall-effect sensors to gather accurate system information for reference generation.
2. In the second stage, compensating reference signals in terms of current or voltage are derived based on control schemes and APF configurations. This part of the control scheme estimates the current reference waveforms for each phase of the inverter by maintaining a constant dc bus voltage.
3. In the final stage of control scheme, the controller forces the active power filter inverter to track the desired compensating currents from the source. This part of the control scheme is responsible for generation of the gating signals for the solid-state devices of the inverter of APF using different current control techniques such as PWM, hysteresis, sliding-mode.

The combined controller of the APFs is realized using analog and digital devices or advanced microelectronic devices, such as single-chip microcomputers, DSP's, and FPGA.

1.9.1 Harmonics detection

The performance of active power filter is depends upon accurate estimation of reference signals. The several estimation methods were developed in the literature and modification continued. Earlier there were two kinds of control strategies for extracting current or voltage harmonics from the corresponding distorted current or voltage signals. These are time domain and frequency domain technique. In recent research new methods based on wavelet transform and artificial intelligence (AI) are reported for extraction of reference signal. In order to generate the reference signal required by the active power filter. There are three kinds of approaches as follows.

a) Load current detection,

b) Supply current detection and

c) Voltage detection.

Load current detection and supply current detection are commonly used for shunt active power filters.

1.9.2 Frequency domain technique

Compensation in the frequency-domain is based on the principle of Fourier analysis and periodicity of the distorted voltage or current waveform to be corrected. With this strategy the inverter switching frequency must be more than the twice the highest compensating harmonics frequency. Fourier Transform (either conventional or FET) is applied to the captured voltage/current signal. Compensating harmonic components are separated by eliminating the fundamental component and inverse Fourier Transform is applied to derive compensating reference signal in time domain. In order to reduce response time delay by

making computation much faster, some modifications in the Fourier technique were proposed and practiced as Modified Fourier —series technique. The principle behind it is that only the fundamental component of current /voltage Is calculated and this is used to separate the total harmonic signal from the sampled load-current) supply voltage waveform. The practical implementation of this technique relies on modifying the main Fourier series equations to generate a recursive formula with a sliding window. This technique is adapted to use two different circular arrays to store the components of the sine and cosine coefficients computed every sampling sub-cycle. The newly computed values of the desire coefficient are stored in place of the old ones and the overall sum of the sine and Cosine coefficient is updated continuously. The computation time is much less than that of other techniques used for single-phase applications. This technique is equally suitable for single or three-phase systems. Another modified Fourier-series technique was developed relies on the decomposition of the three phase signals into synchronously rotating direct and quadrature axes. The technique is used to compensate for all non-active components of load current signal. The non-active current definition in the d-q reference frame is used to generate desired supply currents. Sliding-window computation techniques are used (similar to that above) to calculate the reference value of the filter current/voltage. This technique is suitable only for three-phase systems.

1.9.3 Time domain technique

It is one among the well-established technique for extraction of compensating signals. It is based on instantaneous derivation of compensating commands in the form of either voltage or current signal from the distorted and harmonic polluted voltage or current signal. The different techniques which are in use are [155]: Instantaneous Reactive Power Theory [156-158]. Synchronous ‘d-q’ reference-frame based algorithm[160], Synchronous detection algorithm [163,164], Instantaneous power balance method [149], Energy balanced (EB) method[161], Direct-detection method [165], Notch-filter based method[166],Sine-multiplication technique [167], Fictitious Power Compensation Technique [168] etc. some of them briefly summarized here.

a) Instantaneous reactive power theory

It is based on the *α-β-0* transformation which transforms three-phase voltages and currents into the *α-β-0* stationary reference frame. From this transformed quantities instantaneous real and reactive power of the load is calculated, which consists of a DC component and an oscillating component. The oscillating component is extracted using high-pass filter and taking inverse *α-β-0* transformation compensating command (or reference) signals in terms of either currents or voltages are derived. These signals are distributed equally to each phase of the three-phase. This method needs several high accuracy multipliers for implementation, so its features are complicated in structure, difficult to adjust,

poor in performance, and only suitable for a three-phase balanced system [156]. The original 'p-q' theory proposed by Akagi et al and then revised by Marshal et al [157] and Nabae et al [158] is modified /extended to make It applicable to eliminate neutral current of three-phase, four wire systems where source voltages are unbalanced and loads are non-Linear and unbalanced. The control scheme based on instantaneous reactive theory is shown in Fig.1.11.

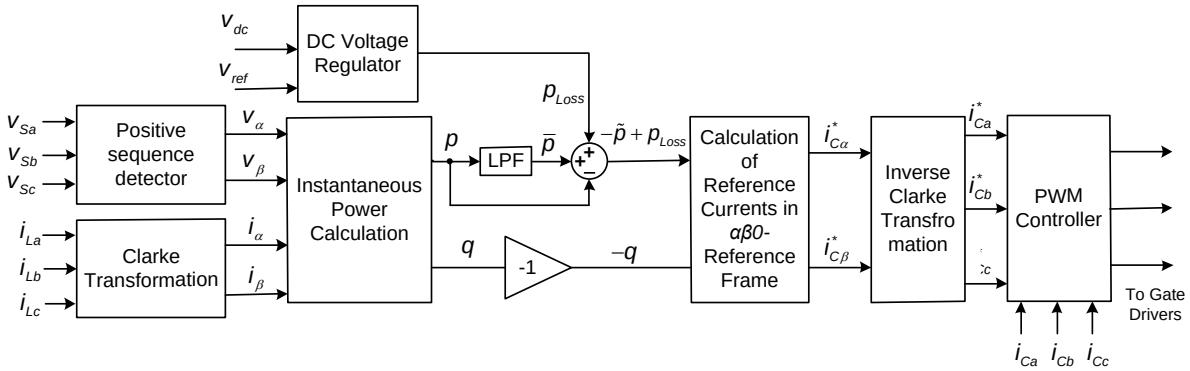


Fig.1.11: Instantaneous reactive power theory.

b) Synchronous d-q' reference-frame based algorithm

It's based on parks transformation. The active and reactive components of the system are represented by the direct and quadrature component respectively. In this approach, fundamental quantities become d-c quantities, and all harmonic components are transformed into dc quantities with a fundamental frequency shift, which can be separated easily through filtering. To implement the synchronous reference frame some kind of synchronizing system such as PLL should be used [167]. The control scheme based on d-q reference frame is shown in Fig. 1.12.

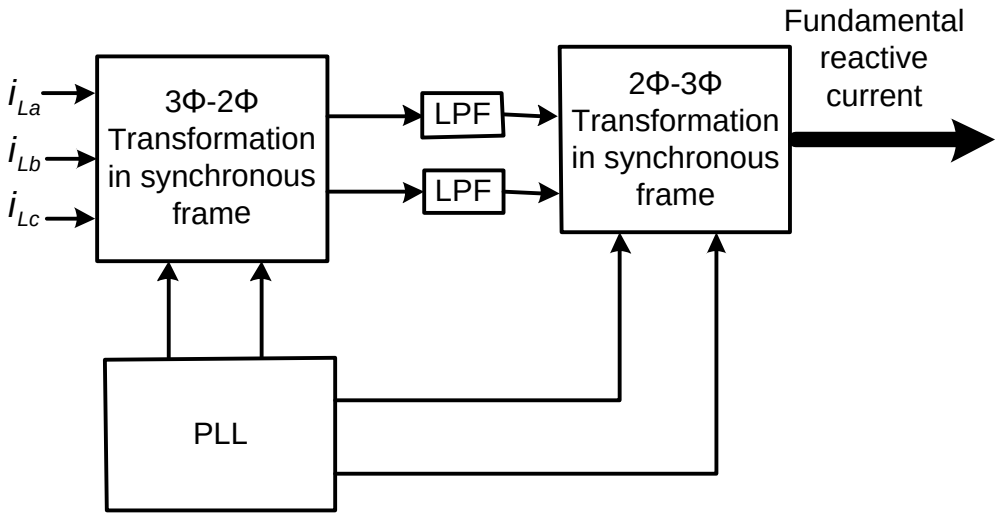


Fig. 1.12: synchronous reference frame based algorithm.

1.9.4 Wavelet transform based algorithm

In recent research wavelet analysis have been proposed extensively as a new tool for fault detection, localization and classification of different power system transients[137]. It is implemented through the Multi Resolution Analysis (MRA) method for extraction of reference signal. In this, a Matlab computer program is written to buffer a Window of data, which come on-line from simulation program. The sampling rate and time step of simulation Program is adjusted based on the maximum harmonic frequency in the System. The reference Signal is extracted by defining the resolution level of the fundamental Signal and makes all the coefficients of that level to be zero and reconstruct the signal to get the Whole disturbance in the signal, the resulting signal is used to generate the reference signal. The block diagram of interfacing process is shown in Fig. 1.13.

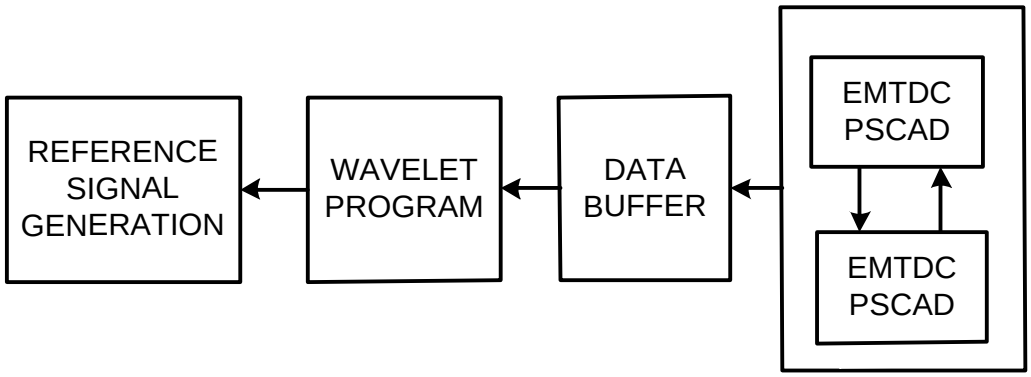


Fig. 1.13: Block diagram of interface process of wavelet.

1.9.5 Artificial Neural Network (ANN) algorithm

Recently, Neural Network has generated a good deal of interest in certain applications [139, 140, 154]. Some of the literatures have proposed Adaptive Linear Neuron based approached to estimate reactive power and harmonics content in the current. For on line estimation of harmonics in a power system (ADALINE) structure is used. ADALINE is highly adaptive and capable of estimating the variations in the amplitude and phase angle of the harmonic components, which will enhance the performance of the active power filter. It is based on original decomposition of the measured signal to specify the neural network inputs. This new decomposition is based on Fourier series analysis of the measured signal where in modified LMS training algorithm carries out the weights. This new estimation strategy appreciably improves the performance over traditional compensating methods and is valid both for single phase and three phase system. The other advantages include high speed, accurate and self- adapting to new environment. The Adaline based harmonics estimator is shown in Fig. 1.14.

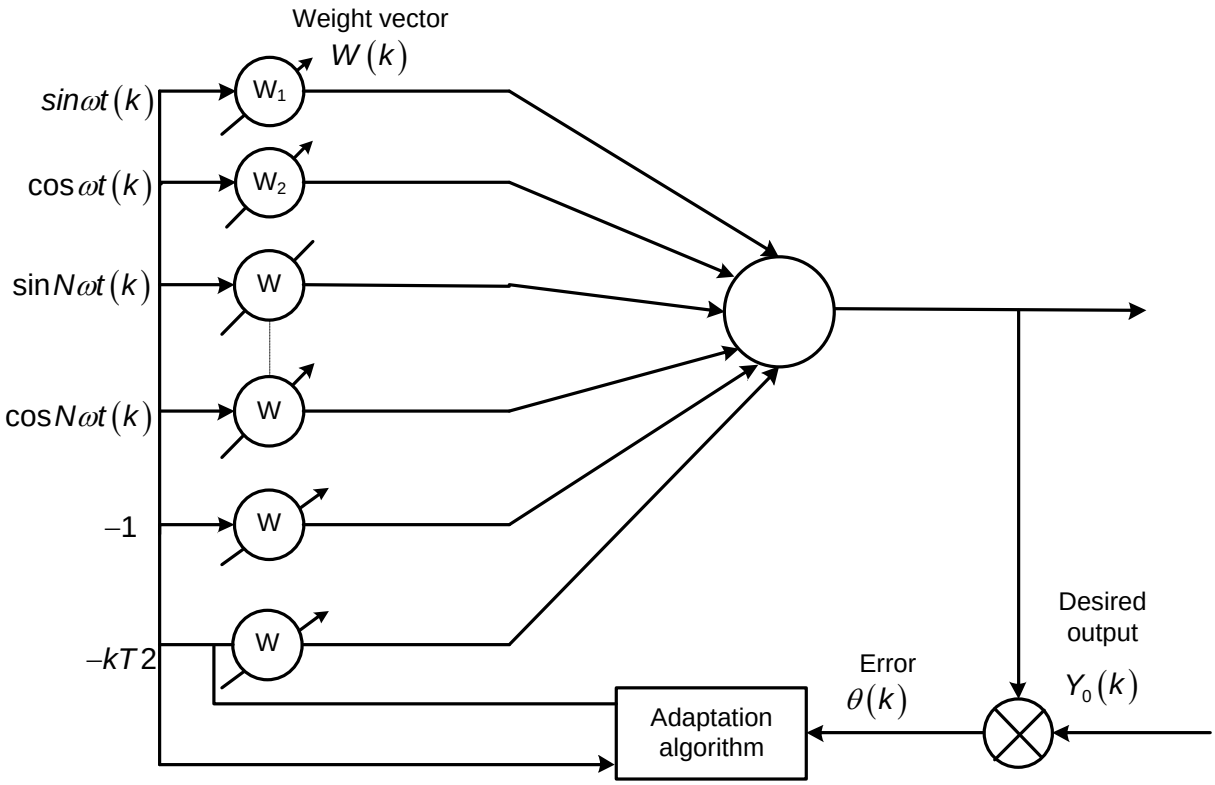


Fig. 1.14: ADALINE based harmonics estimator.

From the brief review of control techniques, it is apparent that a lot of work has been carried out in the area of harmonic power flow studies. Different algorithms for carrying out harmonics analysis have been proposed in the literature. As regards the design, development, analysis and implementation of shunt APFs based on above control strategies is concerned, different researchers around the world have contributed massively, and their efforts and work done is summarized here briefly.

Shireen and Tao [169] have presented DSP based shunt APF for low voltage distribution systems. Authors concluded that the proposed technique requires only the load current information to estimate the fundamental current information which is then used to calculate the required compensation current using the DSP algorithm. Unique feature of DSP have been reported over analog control methods.

Li et al. [171] have developed a novel current detection algorithm of shunt APFs, based on current decomposition for harmonic elimination, power factor correction and balancing of non-linear loads. Several improved/ modified p-q theory have been reported in literature [171] to overcome the limitation of conventional p-q theory.

Performance of the active filter is often degraded due to distorted and/or unbalanced main voltage. Huang and Wu [172] have presented a control algorithm for the performance improvement of three-phase, three-wire active filter under non-ideal mains.

A systematic evaluation is presented on the results of using the instantaneous reactive power algorithm under non-ideal mains and reported that its performance is degraded. Once the main voltage become non-ideal. They also reported that the main current can be effectively controlled by using a simple controller on the average voltage of the DC capacitor voltage. The approach needs only one multipliers, and less number of sensors as compared to the d-q methods. By this algorithm, the main current after compensation is expected to be balanced and undistorted in spite of the variation in the supply voltage.

Kale and Ozdemir [173] presented a new control algorithm for a shunt APF to compensate harmonic and reactive power of a three-phase thyristor bridge rectifier under non-ideal mains voltage scenarios. Sensing load current, dc bus voltage and source voltages compute reference currents of the APF.

Chandra et al. [174] presented DSP based simple control algorithm of shunt APF for AC voltage regulation at the PCC, harmonic elimination power factor correction and load balancing of non-linear loads, using indirect current control technique. Two closed loop PI controllers are used to estimate the amplitude of in-phase and quadrature component of reference supply current. The proposed control algorithm has an inherent property to provide a self-supporting dc bus and require less number of current sensors resulting in an overall cost reduction. Cavallini et al. [175] have made a comparison of various compensation strategies for a shunt active power filter and concluded that the strategy based on unity power factor control is appropriate when the supply voltage waveform is distorted. Marques [147] and Soares et al. [230] have reported simulation and analytical studies of shunt active filters under nonsinusoidal conditions.

Chatterjee et al. [151] has presented an instantaneous reactive volt-ampere compensator and harmonic suppressor system, which operated without sensing the reactive volt-ampere demand and non-linearities present in the load. It is operated cycle-by-cycle reference current control made by regulating the dc-link voltage to achieve the compensating feature. A hardware based PI controller with PLL based sine wave generator was use to implement the control algorithm.

Smedley et al. [176] have presented a unified constant frequency integration (UCI) APF control method based on one cycle control. This method employs an integrator with reset as its core component to control the pulse width on an ac-dc converter so that its current draw is precisely opposite to the reactive and harmonic current draw of the nonlinear load.

Hirve et al. [93] have explored the theory of UCI or one-cycle control for shunt APF control. The scheme compensates unbalanced loads in a three-phase, four-wire system. Author presented a PLL-less control scheme and reported that the APF provides compensation currents in such a way that the utility supplies only the balanced fundamental current at unity power factor, even if the load draws reactive and harmonic currents. The

scheme neither requires the service of a PLL nor requires sense the unity voltages. This makes the scheme insensitive to the distortions that are generally present in the utility voltages. The problem associated with PLL is described.

Mishra et al. [177] have discusses a new general algorithm for shunt APFs using instantaneous reactive power theory. The general vector expression for desired source current has been formulated in terms of instantaneous active and reactive powers. Proper choices of source power terms give different levels and types of compensation.

Chen et al. [178] presented the application of the synchronous detection method for reactive and harmonic current compensation in an unbalanced three phase power system. Ghosh and Joshi [179] have presented a new approach for generating reference currents for an active filter and/or a static compensator by using the theory instantaneous symmetrical components to obtain an algorithm to compute three-phase reference currents which, when injected to the power system, produce desired results. Mishra et al. [180] have proposed an experimental study of the application of instantaneous symmetrical component theory on two-quadrant chopper to equalize the voltage of the capacitor.

Chen [181] has proposed an algorithm for the generation of compensating current in such a way that the source supplies only the balanced fundamental current at unity power factor. It does not use any transformation, but uses the sequence components for power calculation.

George and Agarwal [95, 96, 152] realized a novel scheme for balancing the currents and obtaining the best compromise between the power factor and current distortion under non-sinusoidal voltage conditions. The technique neither uses p-q theory nor sequence transformation. For power calculations, even though the current is unbalanced. The source supplies only the balanced fundamental current at unity power factor.

Jain et al. [182] suggested a control algorithm for shunt APF that maintains similar distortion in the compensated current in present in the source/utility voltage. This attributes the responsibilities of the customer and utility at PCC.

Chandra et al. [183] presented a scheme of presenting an approach to quantify the distortion caused by a single customer when there are many customers in the network. And then mitigate only that portion of harmonics for which the customer is responsible.

In many residential, commercial and industrial application power is distributed through a three-phase, four-wire system, neutral current is another major problem under such cases. Excessive neutral current can cause overloaded power feeders, overloaded transformers, voltage distortion and common mode noise. Load unbalance may have under/over utilization of the feeders. Conventional three-phase three-wire APF does not perform satisfactory in three-phase, four wires to improve power quality. A number of APF schemes have been proposed for three-phase, four wire system. A time sharing method has been used to

eliminate a predetermine number of harmonic components in [78]. A different approach was proposed in [78,] with two converter topologies. In the first termed “split capacitor” topology, the system neutral is connected to the electrical midpoint of the dc-bus through an optional inductance. In the other, called the “four switch leg” topology, the neutral is returned to a fourth switch leg [79] this filter neutralizes the harmonics associated with the load on a three-phase four wire system and prevent the flow of harmonic currents from flowing in the utility’s neutral conductor. These topologies have been shown to have distinct advantages over traditional approaches to the problem, particularly over the three single-phase inverter approaches. The controllability of the four-switching-leg inverter topology is reported better than the split-capacitor topology; however, the conventional three-lag converter is preferred because of its low number of power semiconductor devices.

Quinn et al. [78] have been implemented a shunt APF control scheme which neutralizes current harmonic effects, caused by any configuration of nonlinear loads in three-phase, four-wire systems. The four switching-leg topology is preferred over capacitor midpoint topology, to reduce both voltage and current rating of the DC side capacitor [79].

The theory of instantaneous reactive power, well developed for three-phase, three-wire systems [7,8] have been extended for application in three-phase, four-wire system in [11]. Aredes et al. [11] have proposed a three-phase, four-wire shunt APF using a conventional three-leg converter, without the need of power supply at DC bus. Two approaches have been developed to control the active filter. Both control strategies consider harmonics and zero sequence components in the voltage and current simultaneously.

Thomas et al. [32] have presented the performance of a three-phase, four-wire APF using three-leg inverter with split capacitor topology, for only harmonic compensation case. Authors have reported that the neutral current is considerably reduced without the need of an additional leg in active filter. The harmonic component of the load current have been extracted using a band-pass filter and serve as the current reference. Error signal is process by a PI controller. Detailed design guidelines for the power circuit have been derived and applied to a 5kVA IGBT laboratory prototype.

Lin and Lee [184] have introduced a three-phase voltage-source inverter for a power quality compensator under the unbalanced mains and nonlinear loads is proposed to provide balanced three-phase source current and improve input power factor. The proposed converter is based on the conventional tree phase VSI with three additional ac power switches to achieve three-level pulse-width modulation. The voltage stress of three ac power switches to achieve three-level pulse width modulation. The voltage stress of three ac power switches is clamped to half the dc-link voltage.

Singh et al. [187-190] have developed new/improved approach to eliminate harmonics, to compensate for reactive power and neutral current and to balance supply

current. Detailed analysis and mathematical modelling of the APFs have been presented and supported by in-depth simulation and experimental studies. In [187, 188] a control scheme have been proposed which is based on average power calculation as estimation of different components of reference supply current. The scheme was proposed for three-phase, three-wire and three-phase four-wire] shunt APFs, two type of current control techniques with a view to the problem of switching ripples in the supply current caused by switching of an active filter have been presented. It discussed closed loop control scheme implementation using DSP for direct and indirect current control technique. Significance of indirect current control technique is presented. The design, development and experimental investigations of an active filter are intensely presented in [188]. A current-controlled VSI is used as an APF system.

The APF system employs power balance theory, which in this investigation is implemented using a DSP. The design details, including necessary equations of a prototype model of the AF system, are presented. The p-q theory has been modified to obtain an improved control algorithm of the shunt APF in [174]. Filter design and load variation in the system. It has been found that the proposed control algorithm offers notches and distortion-free supply currents during steady and transient operating conditions of the nonlinear load.

Singh et al. [190] presented a novel three-phase, four-wire distribution static compensator DSTATCOM based on three-leg VSI and a star/delta transformer is proposed. Authors have reported that star/delta transformer connection mitigates the neutral current and the 3-leg VSI compensates harmonic current, reactive power and balances the load. A detailed investigation is made in [52], based on reduced rating voltage source converter with a zig-zag transformer as a DSTATCOM is proposed for power-quality improvement in the three-phase, four-wire distribution system. Authors concluded that proposed DSTATCOM is employed for the compensation of reactive power, harmonics currents, neutral current, load balancing and the voltage regulation at the point of common coupling. Despite the above mentioned methods, few new control schemes have been also reported in the literature [32, 53, 55, 56, 57].

Soft computing has experienced an explosive growth in the last decades, partially due to uncertainties and vagueness in the process signal and occurrence of random events, and partially due to nonlinearity and complexity of the different processes [142, 143,144]. Many intelligent algorithms for designing the control of APF are also proposed [27, 54, 99,112, 138, 139, 194, 195]

Singh and Solanki [196] have proposed shunt APF for compensation of reactive power, unbalanced loading, and harmonic currents. APF is controlled using ADALINE based current estimator to maintain sinusoidal and unity-power-factor source currents. The practical

implementation of the SAF is realized using dSPACE DS1104 R&D controller having TMS320F240 as a slave DSP.

Jain et al. [194] have proposed a fuzzy logic based three-phase shunt APF to improve power quality by compensating harmonics and reactive power required by a nonlinear load. The advantage of fuzzy control is explained. The fuzzy control scheme is realized on dedicated micro-controller (INTEL 8031) based system. Similar approach is presented for three-phase four-wire in [195]. An exhausted survey on fuzzy set theory applications in electrical power systems is presented in [191]. Dixon et al. [192] presented a fuzzy controlled active front-end rectifier with current harmonic filtering characteristics. The amplitude of the current is controlled by a fuzzy system, which adjusts the dc-link voltage of the PWM rectifier. Authors concluded that the measurement and/or calculation of harmonics and reactive power are not required, making the proposed control scheme very simple and hence minimizing sensing variables. A comparison between FLC and conventional PI controller is presented.

Kirawanich and O'Connell [197] have presented a switch-mode active power line conditioner (APLC) that uses fuzzy logic to control the semiconductor switches is described. Frequency domain analysis is used to determine the desired compensation current, and a rule-based piecewise-linear fuzzy proportional-integral controller (FPIC) provides the appropriate switching pattern of the APLC to generate the actual compensation current. An experimental measurement on a low-power (700 VA), DSP based hardware prototype has been carried out to validate the control scheme and simulation results.

Elmitwaliya et al. [198] have presented a three-phase, four-wire shunt APF for harmonic mitigation and reactive power compensation in power system supplying nonlinear load based on neural network. Two neural networks are utilized in the scheme. Adaptive linear neuron is based to extract the active components of three-phase currents from the non-sinusoidal load currents. Another feed forward neural controller is used to govern the generation of the gating pattern of the inverter. Pecharanin N. et al. [199] have reported a methodology of harmonic detection scheme in active power filter from the power line by using neural network.

Rukonuzzaman and Nakaoka [200] have proposed a magnitude and phase determination of harmonic currents by adaptive learning back-propagation neural network. This approach introduce adaptive learning multi-layer back propagation neural network, which converge faster than simple back-propagation neural network. This method is faster than conventional method and this makes possible the no-line determination of instantaneous harmonic current components. Marks and Green [201] have presented a predictive harmonic identifier for generation of a contemporary estimate of the fundamental component of the distorted input current or voltage waveform.

Adaptive neural network techniques like ADALINE have been used in active power filtering in various ways by different researchers [196].

Singh et al. [83, 196] developed an ADALINE based current decomposer for estimating reference currents. Authors have reported a neural network based control scheme to decompose the load current into four parts; positive sequence active power current, positive sequence reactive power current, harmonic current and negative sequence current.

1.9.6 Generation of Gating Signal to Control Switches

After estimation of reference current signals, the next stage of APF control is the generation of switching signals for the power electronic devices of the converter circuit. These switching signals are obtained by comparing the reference compensating signals with the actual current in a controller. Various control techniques for generation of gating signals are reported such as linear PWM, predictive, hysteresis, SVM, etc. [7, 31,85, 86,116, 151, 154, 189, 197]. The performance of an APF is affected significantly by the selection of control techniques [189].

Therefore, the choice and implementation of the control technique is very important in order to achieve satisfactory performance of APF. The control techniques for harmonic current tracking are either analog or digital based, and are generally categorized into two control schemes, linear and nonlinear controls

In linear current control techniques, voltage or current PWM, ramp comparison control, sinusoidal internal model control, etc. are used for obtaining the PWM signals [86]. Nonlinear current control techniques include hysteresis control and space vector modulation (SVM). The hysteresis control is robust, but leads to a widely varying switching frequency, and is difficult to implement.

1.10 Scope of Work and Author's Contribution

The term "power quality" has been used to illustrate the variation of voltage current and frequency in an electrical power system, it has been found that harmonic currents, reactive power requirement of nonlinear load and unbalanced operation are the most dominant types of power quality problems in modern distribution systems. This thesis explores this fact and evaluating the solutions based active power filter for improving the power quality of the distribution systems. In this thesis, an attempt has been made for improving power quality in 3P3W and 3P4W systems with APF.

The main contributions of the author can be summarized as follows:

To begin with, a literature survey on available inverter topologies for the realisation of APF is studied. Based on this study, diode clamped three level inverter and cascaded H-bridge five levels have been selected as a power circuit for the APF. Major attempts have been made to determine the compensating signals using adaptive control schemes such as least mean

square, anti-Hebbian and anti-Hebbian based total least square algorithms. The PI controller with proper gain parameter is used to regulate the dc side capacitor voltages. However, PI controller requires a precise mathematical modeling of the system which is difficult to obtain some time due to parameter variations and/or nonlinear nature of the system. Therefore, it is proposed to design and developed a type-2 fuzzy logic controller (T2FLC) based three level diode clamped shunt active power filter, which is based on linguistic description of system, and offer better transient response without much accurate information of the mathematical model of the system. The fuzzy logic controller provides improved performance in terms of overshoot limitation and sensitivity to parameter variation. However, the T2FLC is very complex to implement with higher level inverter due to the association of length process such as fuzzification, rule base, inference and defuzzification. For better accuracy in control, a larger set of rules is required, which results in longer computational time. The DCMLI topology seems to be the best suited for active power filter applications. But, the large number of power components and voltage unbalance problem at higher levels limits the DCMLI for three level and low-power rating applications. A simplified control approach to design fuzzy logic controller for five level cascaded H-bridge multilevel inverter (CHBMLI) based active power filter. The proposed control scheme used is a single input fuzzy logic controller (SIFLC). The SIFLC reduces the conventional two input fuzzy logic controller (CFLC) to SIFLC controller. The SIFLC also offer significant reduction in the rule inference and simplifies the tuning of control parameters. The SIFLC controller is integrated with anti-Hebbian based on total least square scheme is presented to eliminate current harmonics and reactive power requirement of the nonlinear load. The SIFLC controller is integrated with anti-Hebbian based on total least square scheme is also extend to three phase four wire active power filter for compensation of phase current harmonics, reactive power and neutral current under different voltage conditions.

1. Adaptive reference current generation for active power filter is presented and weights of the reference current are updated using least mean square, anti-Hebbian and anti-Hebbian based on total least square algorithm. The systematic integration of PI and type-2 fuzzy logic controller (T2FLC) is discussed in detailed with three level DCMLI based active power filter.
    - The simulation model of the three level diode clamped active power filter and proposed reference current generation schemes are developed in MatLab/Simulink environment. The exhaustive simulations are carried out to investigate performance of the active power filter under steady state and dynamic conditions of nonlinear load. The comparative study of the adaptive neural network based control schemes integrated with PI and type-2 fuzzy logic

controller has been carried out. The various performance indices such as total harmonics distortion of source current, power factor and magnitude of different currents etc. are observed before and after compensation with active power filter.

- The laboratory prototype of diode clamped three level active power filter has been developed to validate the adaptive control schemes such least mean square, anti-Hebbian and anti-Hebbian based on total least square algorithm integrated with PI/type-2 fuzzy logic controller. An experimental study has been carried out by developing the complete hardware circuitry of the adaptive neural schemes integrated with PI/T2FLC using dSPACE 1104 controller.

2. The dc side capacitors voltage regulation of five level cascaded H-bridge active power filter using single input fuzzy logic controller to improve transient performance of the active power filter is discussed. The simplification convert conventional two input fuzzy logic controller to single input using signed distance. This simplification is accomplished by applying signed distance method. The input to the single input fuzzy logic controller is only one variable known as signed distance whereas conventional fuzzy logic controller requires two variables known as error and change of error of its input. The reduction in number of input from two to one, the rule table also reduced to one dimensional. Therefore, single input fuzzy logic controller reduces the computational burden of the processor due to the reduction of fuzzy rules from p^2 to p, where p represents the level fuzzification. In this method, the control surface of the single input fuzzy logic controller can be approximated to piece wise linear (PWL) function which results in significant reduction of tuning process. The SIFLC controller is integrated with anti-Hebbian based on total least square for reference current generation.
    - In order to observe these advantages, a MATLAB/Simulink model of the five level cascaded H-bridge active power filter is developed using Simpower system block sets. The performance of the three phase three wire active power filter is investigated. The simulation results of single input fuzzy logic controller are compared with conventional fuzzy logic controller. The prototype model of the five level active power filter is developed to validate the single input fuzzy logic controller. The various results are obtained during transients as well as in steady state conditions and compared with results of PI controller.
3. The application of SIFLC controller integrated with anti-Hebbian based total least square algorithm is extended to 3P4W active power filter. The reduced rating hybrid three phase four wire (3P4W) active power filter is proposed for simultaneous

compensation of harmonics and source neutral current. The complete configuration of the three phase four wire active power filter comprise of a 3P3WAPF, a zeros sequence transformer and a single-phase APF (neutral current compensator). This hybrid approaches reduces the rating of the active power filter and improves the performance under non-ideal utility voltage conditions.

- The MatLab/Simulink model of the 3P4W active power filter has been developed to test the efficacy of the 3P4W active power filter for simultaneous compensation of source phase current and neutral current. To validate the simulated response of the 3P4W active power filter, a prototype model is developed and tested for compensation of source phase current.

4. Another reduced rating 3P4W active power filter is proposed for simultaneous compensation of the source current harmonics and neutral current. The proposed filter consists of interfacing ac capacitor, 3P3W active power filter and neutral compensator. The proposed filter significantly reduces the dc side capacitors voltages of the 3P3W active power and rating of the neutral compensator.
    - The MatLab/Simulink model of the 3P4W active power filter has been developed to test the efficacy of the 3P4W active power filter for simultaneous compensation of source phase current and neutral current. To validate the simulated response of the 3P4W active power filter, a prototype model is developed and tested for compensation of source phase current.

1.11 Organization of the Thesis

Apart from this chapter, the thesis contains six more chapters and the work included in each chapter is briefly outlined as follows:

CHAPTER 1 starts with an overview of different topologies of inverters used in high-power, medium-voltage systems. Among the available topologies, the DCMLI and CHBMLI based multilevel inverter for the power circuit of active power filter have been selected.

The testing of three level diode clamped inverter and five-level CHBMLI inverter is given in CHAPTER 2, and also the detailed discussion of the experimental set-ups and their implementation procedure is given in CHAPTER 2,

The investigation of the performance of three levels DCMLI new control schemes based on adaptive neural network is derived. The weights of the neural networks are updated using least mean square, anti-Hebbian and anti-Hebbian based on total least square. The adaptive control schemes are integrated with PI and type-2 fuzzy logic controllers are given in CHAPTER 3. In this chapter, a systematic design procedure, selection of passive components and generation of reference currents for active power filter are also given in detail. Further, simulation results are provided to verify the steady-state and

dynamic performance of the compensator with different control schemes integrated with PI and type-2 fuzzy logic controller.

CHAPTER 4 this presents single input fuzzy logic controlled five level CHBMLI based active power filter to improve the transient response. A simulation model of single input fuzzy logic controlled active power filter is developed in MATLAB/Simulink environment. Various simulation results are obtained for steady state and dynamic condition of load. The validation of single input fuzzy logic controller on CHBMLI based is carried out using dspace controller.

CHAPTER 5 is dedicated to the power quality improvement in 3P4W systems. In this chapter reduced rating hybrid APF is proposed. Simulation results are provided to verify the steady-state and dynamic performance of the compensators with different utility voltage conditions. The detailed discussion for the experimental set-ups is also given in CHAPTER 4.

CHAPTER 6 discuss the power quality improvement in 3P4W electrical distribution systems. In this chapter reduced rating hybrid APF is proposed. Simulation results are provided to verify the steady-state and dynamic performance of the compensators with different utility voltage conditions. The detailed discussion for the experimental set-ups is also given in CHAPTER 6. The chapter concludes with experimental results and the corresponding discussion.

The main conclusions of the presented work and possible future research have been summarised in this CHAPTER 7.

In the end of thesis, the list of references and regarding appendices software and hardware implementations are provided.

CHAPTER 2: EXPERIMENTAL SYSTEM DEVELOPMENT

The system hardware, dSPACE–DS interfacing and experimentation for the laboratory prototype models of the three level diode clamped inverter and five-level CHBMLI inverter for three phase systems are described in detail to validate the simulation results presented. Further, these experimental studies are validated with simulation results using the experimental parameters.

2.1 Introduction

The following prototypes are developed in the laboratory.

1. Three-phase five-level diode clamped based inverter.
2. Three-phase five-level cascaded H-bridge based inverter.

A three-phase downscaled multilevel inverter rated at 100 V, 5 kVA is designed and developed to realise the above mentioned inverter topologies based active power filters.

The inverter topologies mentioned above the power circuits consists of 12 and 24 switching devices having same voltage and current ratings. Three level diode clamped multilevel inverter produce three line to neutral (5-level line to line voltage). Whereas, the cascaded H-bridge inverter produces a five-level line-to-neutral (9-level line-to-line) voltage waveform. In experimental setup, IGBTs (IRG4PH40KD) are used as the switching devices for realising these inverters. The other hardware components as required for the operation of the experimental set-up such as pulse amplification circuit, dead-band circuit, isolation circuit, voltage and current sensor circuits are designed and developed in the laboratory. The complete schematic diagram for the realisation of active power filter is shown in Fig. 2.1.

A Digital Signal Processor (DSP) DS1104 of dSPACE is used for the real-time simulation and implementation of control algorithm. By using the Real-Time Workshop (RTW) of MATLAB and Real-Time Interface (RTI) feature of dSPACE DS1104, the Simulink models of the various controllers of the prototypes are implemented. The control algorithm is first designed in the MATLAB/Simulink software. The RTW of MATLAB generates the optimized C-code for real-time implementation. The interface between MATLAB/Simulink and Digital Signal Processor (DSP, DS1104 of dSPACE) allows the control algorithm to be run on the hardware. The master bit I/O is used to generate the required gate pulses and Analog to Digital Converters (ADCs) are used to interface the sensed line currents, supply voltages and dc-bus capacitor voltages. An opto-isolated interface board is also used to isolate the entire DSP master bit I/O.

The development of different hardware components as required for the operation of the hardware prototypes are discussed in the upcoming sections.

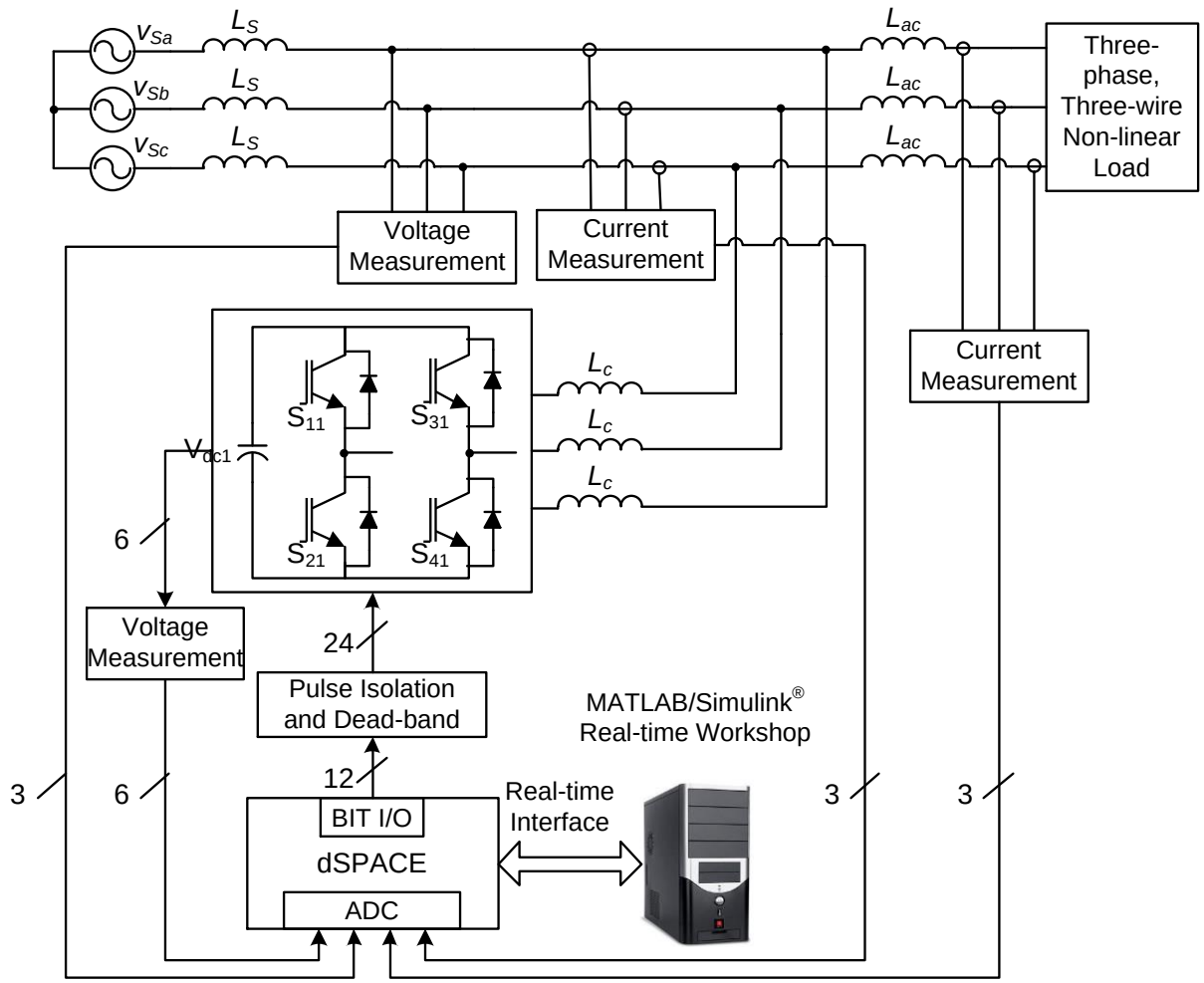


Fig. 2.1: Schematic diagram for hardware implementation of active power filter.

2.2 System Hardware

The developed experimental prototype is comprised of the following basic parts:

1. Power circuit of inverters extended to use as active power filters
2. Measurement circuits
   - Source currents
   - Load current
   - Source and dc capacitor voltages
3. System software
4. Control hardware
   - IGBT driver circuit
   - Dead-band circuit and isolation

2.2.1 Power circuit of inverters extended to use as active power filter

The below mentioned inverter prototypes which are to be extended to use as active power filter has been developed in the laboratory.

i. Three-phase three-level diode clamped inverter.

ii. Three-phase five-level cascaded H-bridge inverter.

These topologies are tested as the inverters and the power circuits were validated to use as active power filter. The power circuits of three-phase three-level inverters with suitably designed loads and sources on its ac and dc side are developed respectively as shown in Fig. 2.2,

Three level diode clamped inverter and five level cascaded inverter topologies consist of 12 and 24 self-commutated power semiconductor switches with anti-parallel diodes. The switches are realized by the IGBTs (IRG4PH40KD). Performance of three-phase three-level diode clamped based inverter.

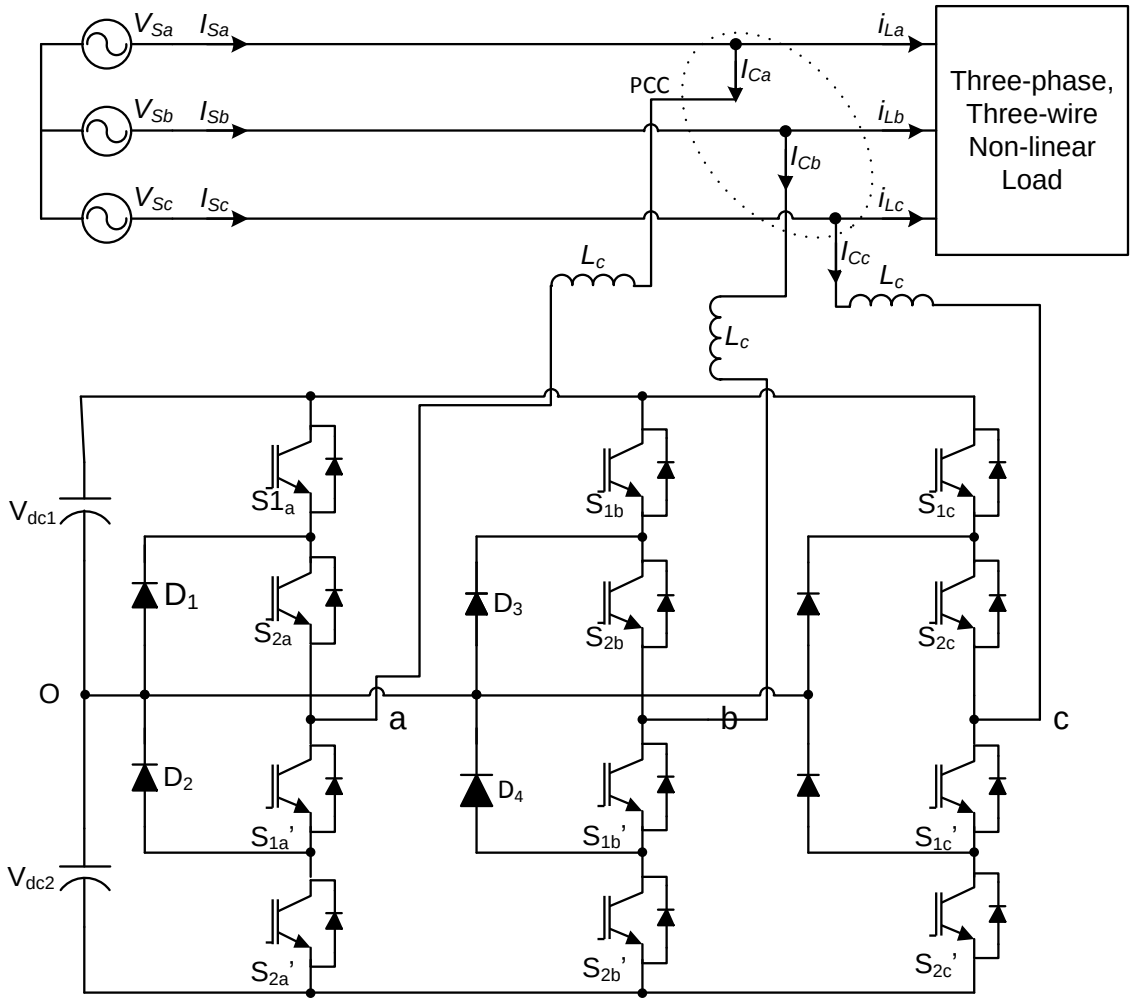


Fig. 2.2: Power circuit of three-level diode clamped active power filter.

To protect each switching device, a suitably designed snubber circuit is connected across it as shown in Fig. 2.3. The snubber comprises of a parallel combination of a resistor and a capacitor connected across a Metal-Oxide Varistor (MOV). All the devices are mounted on heat sinks to ensure proper heat dissipation. Further, these inverter topologies with the designed parameters and the rating of passive components of active power filters are consolidated and tested to validate the simulation results of respective inverter based active power filter. The results of these validated inverter topologies based active power

filters are discussed in the up-coming chapters followed with their respective simulation results.

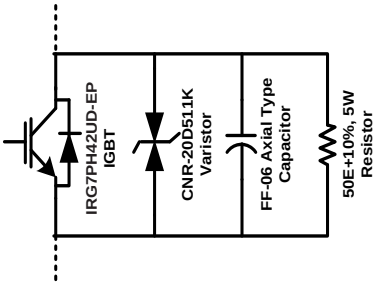


Fig. 2.3: Snubber circuit connected across every switching device of inverter circuits.

The isolated four dc supplies for the converter are provided by two single-phase, three-winding transformers with single-phase diode bridge rectifiers and filter capacitors. A three-phase lamp load is used as a load for the inverter. The parameters used in the experimental study are given in Table 2.1. The Simulink models of the PWM controller schemes of the inverter are implemented using dSPACE-DS1104 controller. The generated firing pulses are given to the corresponding semiconductor devices of the diode clamped inverter through isolation, delay and pulse amplification circuits in real-time.

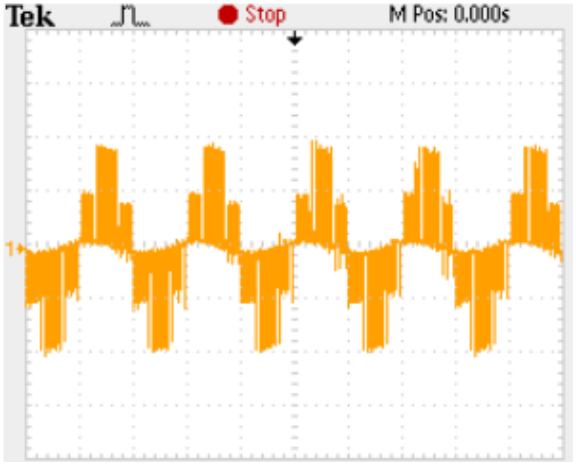
Table 2.1: Parameters used for the experimental validation of diode clamped and H-bridge inverter topologies.

Parameter	**Value**
Amplitude modulation index	m_a = 0.95
Carrier signal frequency	f_{cr} = 2kHz
Isolated dc source voltage	50 V each, provided by three single-phase three-winding transformers (230/115/115 V, 3 kVA) with single-phase bridge rectifiers (KBPC3510)
DC smoothening capacitors	450 V, 1800 µF each
Load	Three-phase lamp load (500 W)

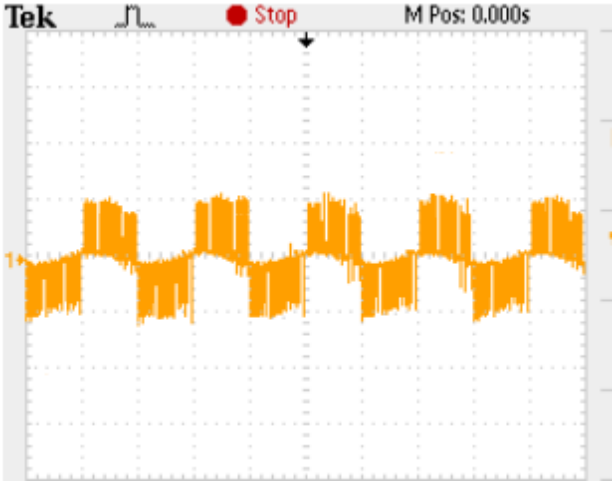
The firing signals generated using dSPACE for phase-*a* of the inverter with level shifted pulse width modulation (LSPWM) technique are shown in Fig. 2.4 (X-axis: 10 ms/div. and Y-axis: 5 V/div.). As seen in Fig. 2.4 digital oscilloscope different channels (from top to bottom) are the firing signals for the switching devices S_{a1} and S_{a2}, respectively (other complementary signals are generated with dead band circuit). Fig. 2.5 (a)-(b) shows the experimentally obtained line-to-line voltages and line-to-neutral voltages of the three level diode clamped

inverter with LSPWM respectively. In these experimental studies the amplitude and frequency modulation indices are kept at 0.95 and 30 respectively. The THD values of line-to-line voltages are 49.5%.

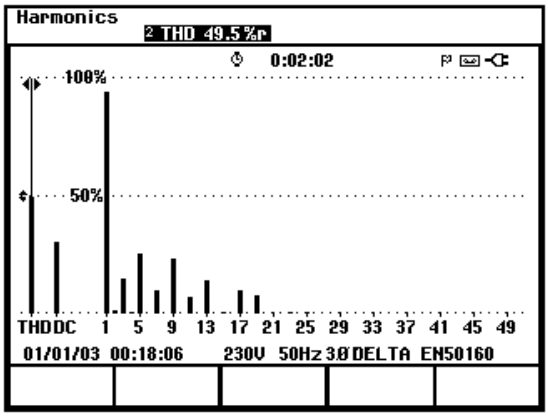
Fig. 2.4: Firing signals of inverter's phase leg–*a* with different modulation techniques (m_a = 0.95, f_m= 50 Hz and m_f = 30) with basic LSPWM



(a) Line-to-line voltage



(b) Line-to-neutral voltage



(c) Harmonic spectrum of line-to-line voltage

Fig. 2.5: Experimental waveforms of a three-level diode clamped inverter

2.2.1.1 Performance of three-phase five-level cascaded H-bridge inverter.

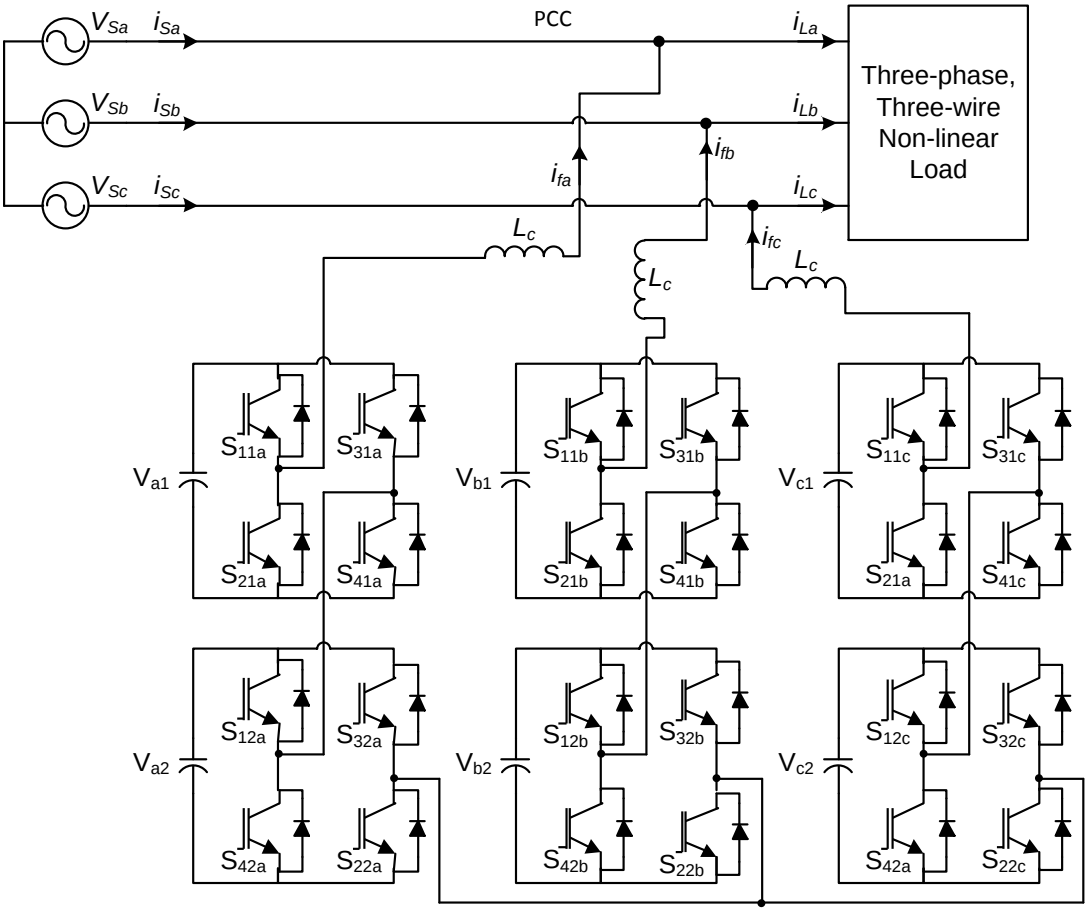


Fig. 2.6: Power circuit of five-level cascaded H-bridge active power filter.

The isolated dc supplies for the six H-bridge cells are provided by three single-phase, three-winding transformers with single-phase diode bridge rectifiers and filter capacitors. A three-phase lamp load is used as a load for the inverter. The parameters used in the experimental study are given in Table 2.1. The Simulink models of the phase shifted PWM controller scheme of the inverter are implemented using dSPACE-DS1104 controller. The generated firing pulses are given to the corresponding semiconductor devices of each H-bridge of the inverter through isolation, delay and pulse amplification circuits in real-time.

The firing signals generated using dspace1104 for phase-*a* of the inverter with phase shifted pulse width modulation technique are shown in Fig. 2.7 (X-axis: 5 ms/div. and Y-axis: 5 V/div.). In Fig. 2.7 different channels (from top to bottom) in each waveform are the firing signals for the switching devices S_{a1}, S_{a2}, S_{a3} and S_{a4} respectively. Fig. 2.8 shows the experimentally obtained line-to-line voltages, line-to-neutral voltages of the five-level cascaded H-bridge inverter with phase shifted pulse width modulation technique. In these experimental studies the amplitude and frequency modulation indices are kept at 0.95 and 30 respectively. The THD values of line-to-line voltages are 18.7% .

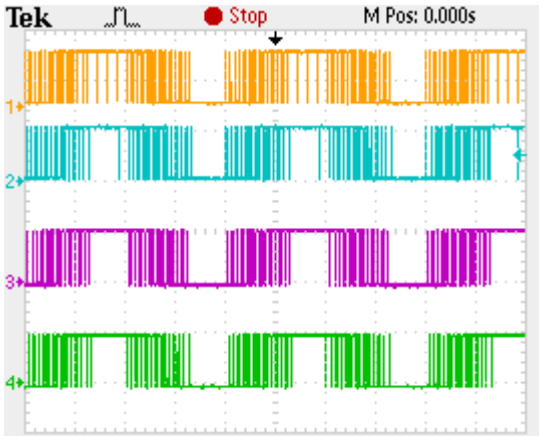
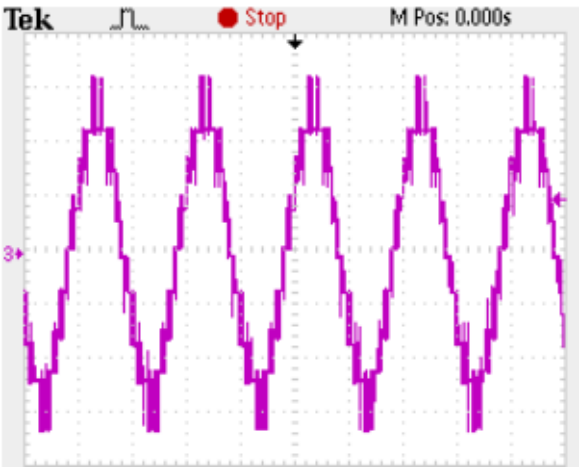
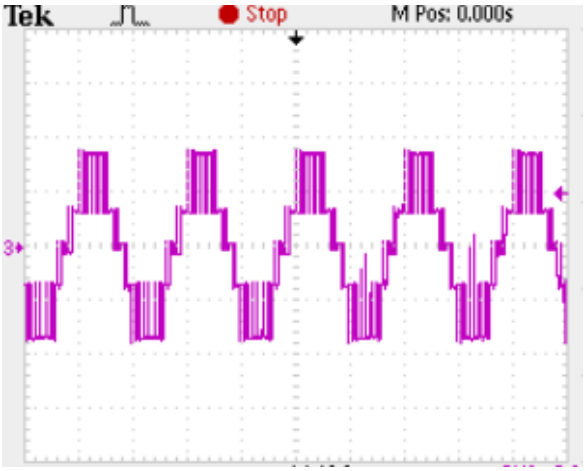


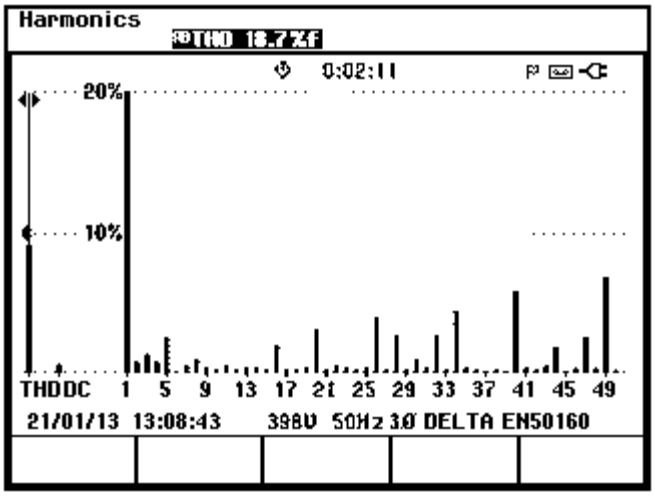
Fig. 2.7: Firing signals of inverter's phase leg–*a* with different modulation techniques (m_a = 0.95, f_m= 50 Hz and m_f = 30) with phase Shifted PWM.



(a) Line-to-line voltage



(b) Line-to-neutral voltage



(c) Harmonic spectrum of line-to-line voltage

Fig. 2.8: Experimental waveforms of a five-level cascaded H-bridge inverter

2.2.2 Measurement Circuits

For reliable and accurate operation of a system in closed loop, measurement of various system parameters and their conditioning is required. The measurement system must fulfil the following requirements:

- High accuracy
- Linearity and fast response
- Galvanic isolation with power circuit
- Ease of installation and operation

With the availability of isolation amplifiers and Hall-effect current sensors, these requirements are fulfilled to a large extent. In order to implement the control algorithms of active power filter in closed loop, following signals are sensed.

1. AC source voltages, source and load currents for reference current generation.
2. DC voltages of the capacitors in all the inverter topologies based active power filters (required for the operation of dc voltage regulator).

2.2.2.1 Sensing of AC Current

The PCB-mounted Hall-effect current sensors (TELCON HTP25) are used to sense the ac source currents. The HTP25 is a closed loop Hall effect current transformer suitable for calibrating the currents up to 25 A. This device provides an output current into an external load resistance. These current sensors provide the galvanic isolation between the high-voltage power circuit and the low-voltage control circuit and require a nominal supply voltage of the range ±12V to ±15V. It has a transformation ratio of 1000:1 and thus, its output is scaled properly to obtain the desired value of measurement. The circuit diagram of the current sensing scheme is shown in Fig. 2.9.

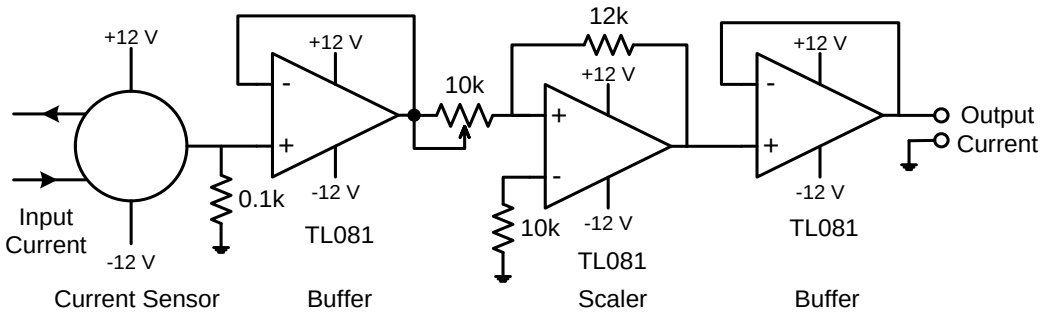


Fig. 2.9: AC current sensing circuit.

2.2.2.2 Sensing of Voltage

The voltages are normally sensed using isolation amplifiers and among them, AD202 is a general purpose, two-port, transformer-coupled isolation amplifier that can be used for measuring both ac and dc voltages. The other main features of the AD202 isolation amplifier are:

1. Small physical size
2. High accuracy
3. Low power consumption
4. Wide bandwidth

5. Excellent common-mode performance

This voltage sensor can sense voltages in the range of ±1 kV (peak) and it requires a nominal supply voltage range of ±12V to ±15V. Fig. 2.10 shows the circuit diagram for the voltage sensing scheme, which uses AD202 isolation amplifier. The voltage (ac or dc) to be sensed is applied between the terminals 1 and 2 (across a voltage divider comprising of 100 kΩ and 1 kΩ) and the voltage input to the sensor is available at the pins 1 and 2 of AD202 via a resistance of 2.2 kΩ. The isolated sensed voltage is available at the output terminal 19 of AD202. The output of voltage sensor is scaled properly to meet the requirement of the control circuit and is fed to the dSPACE via its ADC channel for further processing.

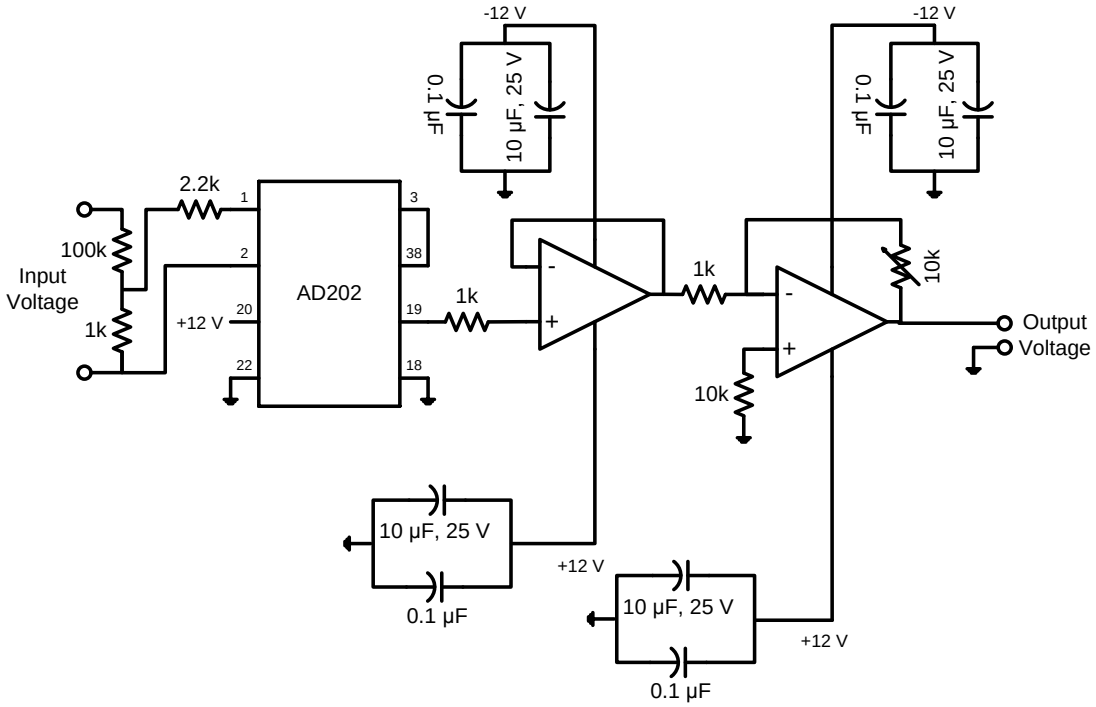


Fig. 2.10: AC/DC voltage sensing circuit.

2.2.3 System Software

Historically, control software was developed using assembly language. In recent years, industry began to adopt MATLAB/Simulink and Real-Time Workshop (RTW) platform based method, which provides a more systematic way to develop control software. Fig. 2.11 shows the Total Development Environment (TDE) of dSPACE and its major component blocks are explained as below:

- MATLAB is widely used as an interactive tool for modelling, analysis and visualization of systems, which itself contains more than 600 mathematical functions and supports additional toolboxes to make it more comprehensive.
- Simulink is a MATLAB add-on software that enables block diagram based modelling and analysis of linear, non-linear, discrete, and continuous and hybrid systems.

- RTW is Simulink add-on software that enables automatic C or ADA code generation from the Simulink model. The generated optimised code can be executed on PC, microcontrollers and signal processors.
- Real Time Interface (RTI) by add-on software of dSPACE provides block libraries for I/O hardware integration of DS1104 R&D controller and generates optimized code for master and slave processors of the board.
- The dSPACE's control desk is a software tool interfacing with real-time experimental setup and provides easy and flexible analysis, visualization, data acquisition and automation of the experimental setup. The major feature of real-time simulation is that the simulation has to be carried out as quickly as the real system would actually run, thus allowing to combine the simulation and the inverter (real plant).

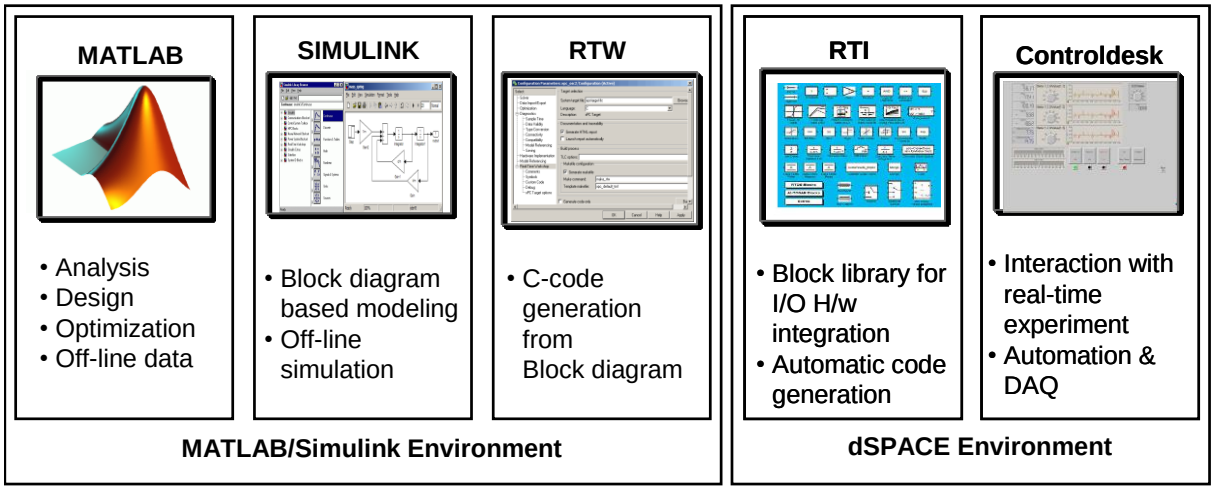


Fig. 2.11: Total development environment of dSPACE with MATLAB/Simulink.

The DSP DS1104 R&D controller board of dSPACE is a standard board that can be plugged into Peripheral Component Interconnect (PCI) slot of a desktop computer. The DS1104 is specially designed for the development of high-speed multivariable digital controllers and real-time simulations for various applications. It is a complete real-time control system based on an AMD Opteron™ processor running at 2.6 GHz. It has 256 MB DDR-400 SDRAM local memory for handling application and dynamic application data and 128 MB SDR SDRAM global memory for host data exchange. DS1104 R&D controller is a very good platform for the development of dSPACE prototype system for cost-sensitive RCP applications. It is used for the real-time simulation and implementation of the control algorithm in real-time.

The sensed ac and dc voltages are fed to the dSPACE Multi-I/O Board (DS2201) of DS1006 via the available ADC channels on its connector panel. In order to add an I/O block (such as ADCs and master bit I/Os in this case) to the Simulink model, the required block is dragged from the dSPACE I/O library and dropped into the Simulink model of these inverter.

In fact, adding a dSPACE I/O block to a Simulink model is almost like adding any Simulink block to the model. In this case, twelve master bit I/Os, configured in the output mode, are connected to the model for issuing twelve gating signals (and twelve complementary signals) to the IGBTs of cascaded H-bridge inverter. In addition, 20 ADCs are connected to the model for giving the source voltages, source currents, load current and dc capacitor voltages of active power filters as input to the DSP hardware.

For balanced three-phase systems, hardware requirement can be minimized by adding electrical quantities of two separate phases and from the resulting quantity, the corresponding value for the third phase is obtained. For example, the source phase voltages v_{an} and v_{bn} are measured and the third phase voltage v_{cn} is obtained by $v_{cn} = -(v_{an} + v_{bn})$. Similarly to sense three phase supply voltages and three load currents, two sensors are used in each case. For dc voltage regulator, only phase-*a* dc voltage of the H-bridge cells of cascaded H-bridge are sensed and the total loss component is obtained by multiplying the phase-*a* loss component by three. The sensed signals are used for processing in the designed control algorithm. The vital aspect for real-time implementation is the generation of real-time code of the controller to link the host computer with the hardware. In dSPACE systems, Real-Time Interface (RTI) carries out this linking function. Together with RTW from the Mathworks®, it automatically generates the real-time code from Simulink models and implements this code on dSPACE real-time hardware. This saves the time and effort considerably as there is no need to manually convert the Simulink model into another language such as 'C'. RTI carries out necessary steps by the addition of the required dSPACE blocks (I/O interfaces) to the Simulink model. In other words, RTI is the interface between Simulink and various dSPACE platforms. It is basically the implementation software for single-board hardware and connects the Simulink control models to the I/O of the board. In the present case, the optimized C-code of the Simulink model of the control algorithm is automatically generated by the RTW of MATLAB in conjunction with RTI of dSPACE.

The generated code is then automatically downloaded into the dSPACE hardware where it is implemented in real-time and the gating signals are generated. The gating pulses for the power switches of converter are issued via the Master-bit I/Os available on the dSPACE board. The DS2201 Connector/LED combo panel provides easy-to-use connections between DS1104 board and the devices to be connected to it. The panel also provides an array of LEDs indicating the states of digital signals (gating pulses). The gating pulses are fed to various power devices driver circuits via isolation and dead-band circuits. Fig. 2.11 shows the schematic diagram of dSPACE-DS1104 board interfaced with the host computer and the real-world plant (power circuit of active power filters). Sensed signals are fed to the ADCs and generated gating pulses are given at Master bit I/Os.

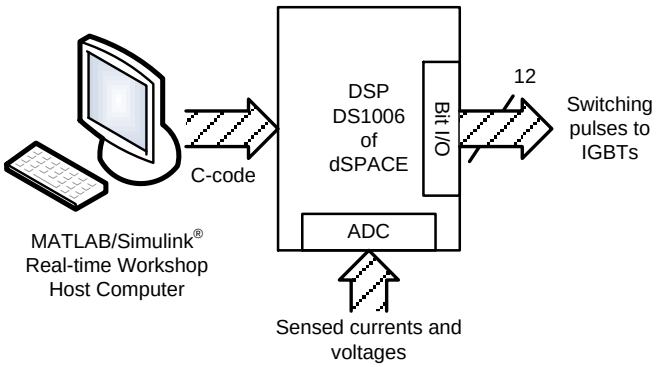


Fig. 2.12: DSP (dSPACE-DS1104) circuit board interfacing.

2.2.4 Control Hardware

The control algorithm is designed and built in MATLAB/Simulink software and the control pulses for 24 IGBTs (Here only 12 firing pulses are generated and remaining 12 are complementary of generated pulses) are generated by real-time simulation using the DSP of dSPACE. The optimized C-code of the Simulink model of control algorithm is generated with the help of (RTW of MATLAB. The RTW of MATLAB and the RTI of dSPACE result in the real-time simulation of the model. The control pulses are generated at various Master-bit I/Os of the dSPACE which are interfaced with the IGBT driver circuits through isolation and dead-band circuits. This ensures the necessary isolation of the dSPACE hardware from the power circuit that is required for its protection. Fig. 2.13 shows the basic schematic diagram of interfacing firing pulses from dSPACE board to switching devices of CHBMLI inverter. In this figure the details of only the phase-*a* of CHBMLI inverter are shown. From Fig. 2.13, it can be observed that the following hardware circuits are required for interfacing the CHBMLI inverter with dSPACE board.

1. Dead-band circuit
2. IGBT driver circuits and isolation

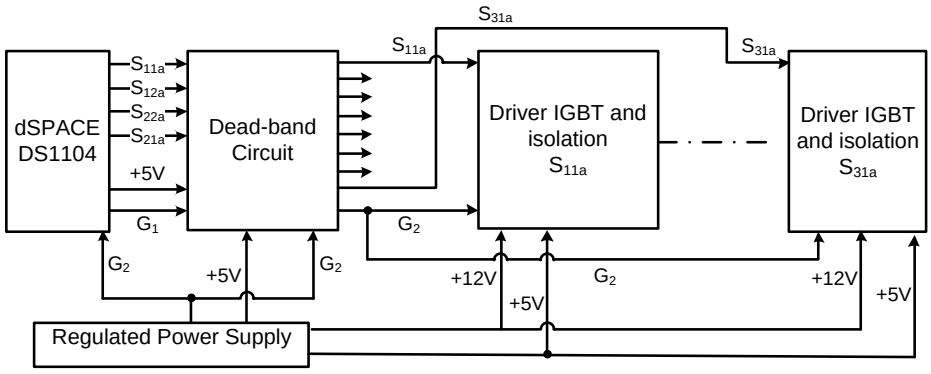


Fig. 2.13: Schematic diagram of interfacing firing pulses from dSPACE controller board to switching devices.

2.2.4.1 Dead-band Circuit

A dead-band (dead-time or delay) circuit is employed to provide a delay time (of about 1 μs) between the switching pulses to two complementary devices connected in same leg of an H-bridge cell. This is required to avoid the short circuit of devices in the same leg due to simultaneous conduction. The delay time between switches of the same leg of H-bridge cell is introduced by a *RC* integrator circuit as shown in Fig. 2.14.

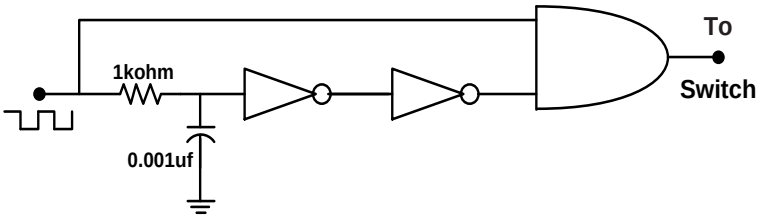


Fig. 2.14: Dead-band circuit for each switching device.

An identical dead-band circuit are used for each leg of all H-bridge cells. The different switching signals obtained experimentally for semiconductor devices in the same leg of an H-bridge cell are shown in Fig. 2.15 with 1 μs delay. In Fig. 2.15 the top and bottom signals are for the switches S_{11a} and S_{41a} respectively.

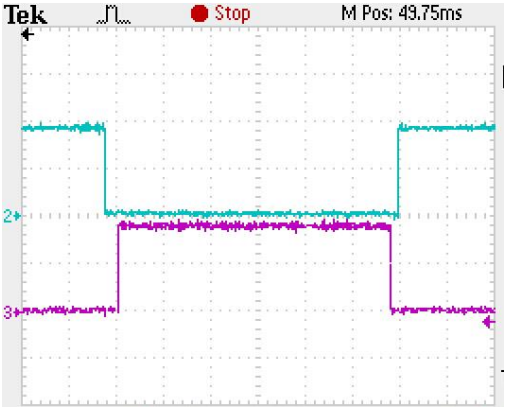


Fig. 2.15: Firing signals for the switches S_1 and S'_1 with dead-band circuit.

2.2.4.2 IGBT Driver and isolation circuit with MCT2E

The IGBT driver circuits are used for pulse amplification and isolation purposes. The control pulses generated from dSPACE unit are not sufficient drive the switching devices. Thus, these signals are further amplified by using proper amplifier circuits. Fig. shows the circuit diagram of pulse isolation and amplifier circuit for IGBT driver circuit. The isolation between power circuit and control circuit provided using MCT2E.

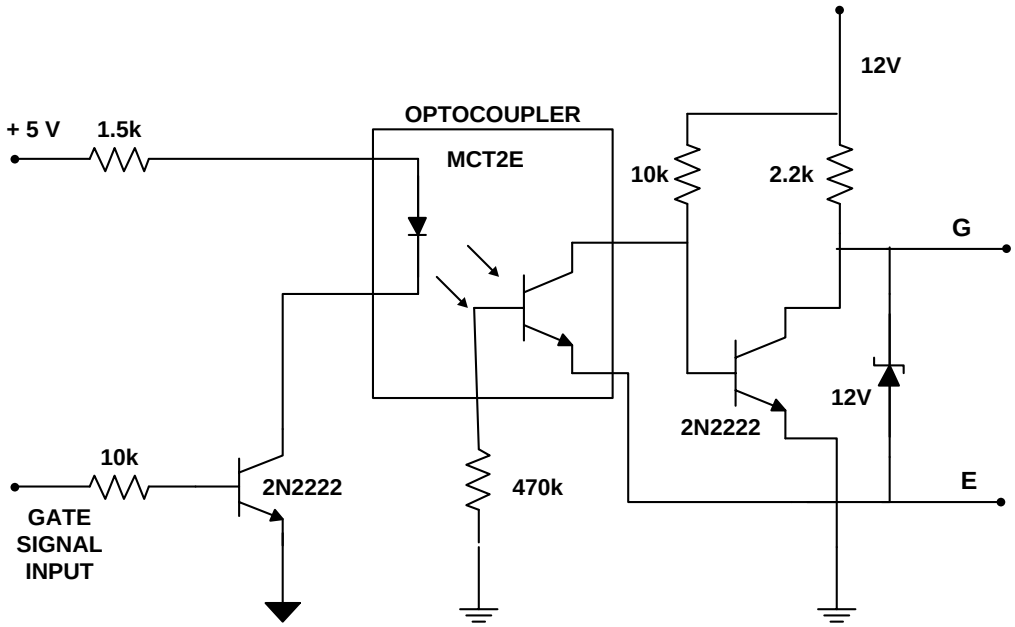
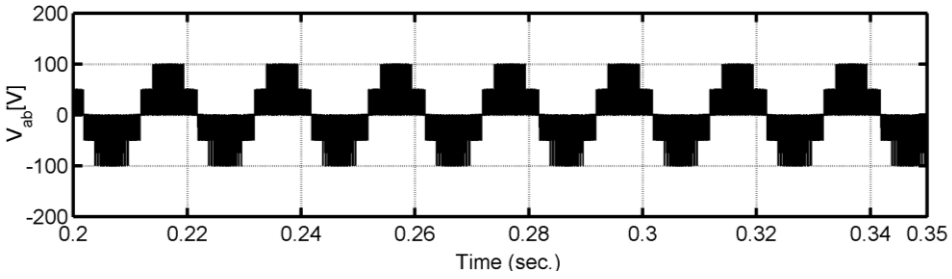
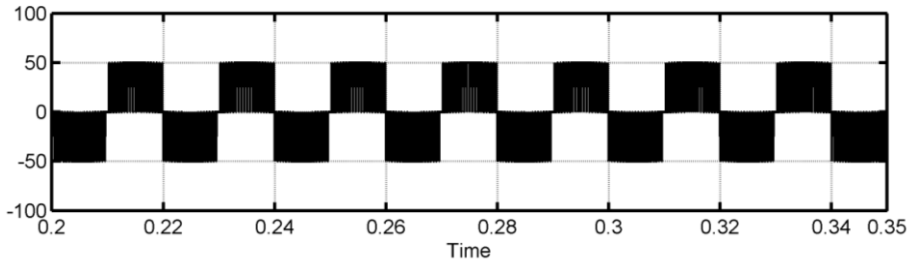


Fig. 2.16: IGBT driver circuit and isolation circuit

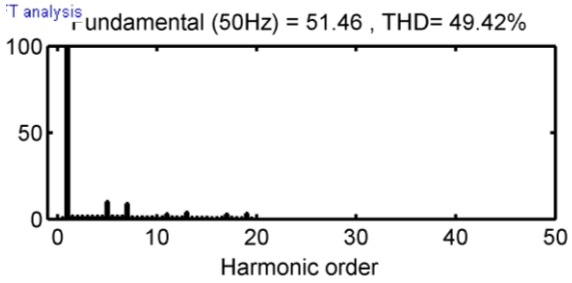
2.2.5 Comparison with Simulation Results



(a) Line to line voltage

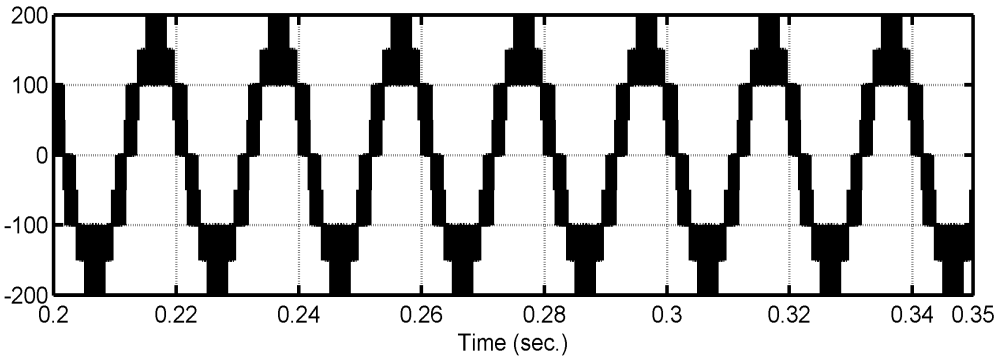


(b) Line to neutral voltage

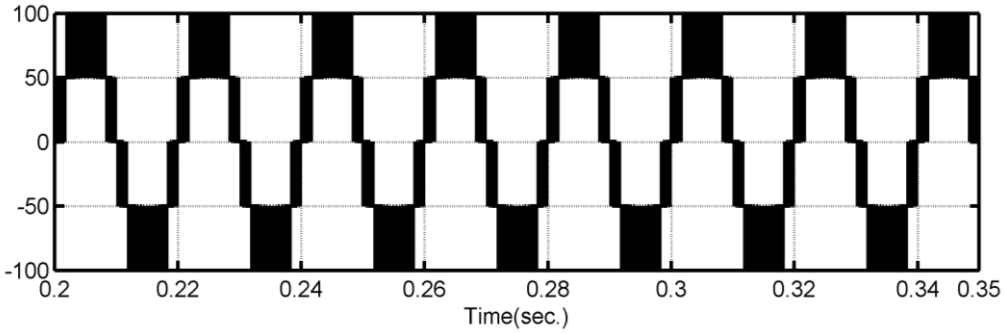


(c) Harmonic spectrum of line-to-line voltage

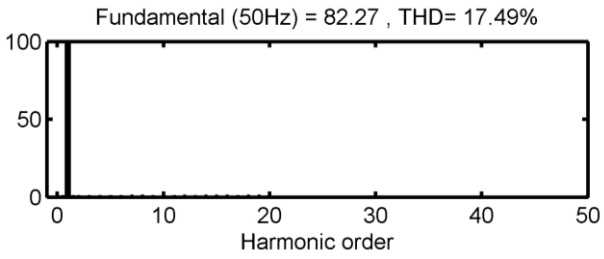
Fig. 2.17: simulated waveforms of a three-level diode clamped inverter.



(a) Line to line voltage



(b) Line to neutral voltage



(c) Harmonic spectrum of line-to-line voltage

Fig. 2.18: simulated waveforms of a five-level cascaded H-bridge inverter

The experimental studies have been conducted at reduced system parameters, for validating the experimental results, the simulation is also carried out with same system parameters. The parameters used in the actual simulation studies are given in Table 2.1.

The simulation is carried out with R-load on ac side and the simulated response are shown in Fig. 2.17 and Fig. 2.18 for three level diode clamped inverter and five-level cascaded H-bridge inverter respectively . Fig. 2.17 (a)-(c) shows the simulated waveforms of line-to-line voltages, line-to-neutral voltages and harmonics spectra of the three-level diode clamped inverter with LSPWM technique, while Fig. 2.18 (a)-(c) shows these results for five-level cascaded H-bridge inverter with phase shifted PWM technique. As can be seen from both these figures, the simulation results are almost with identical experimental results for both inverters.

2.3 Conclusion

In this chapter, the detailed descriptions for the design and development of laboratory prototype active power filters are given. For the developed multilevel inverters, IGBTs are used as switching devices. A DSP DS1104 of dSPACE is used for the real-time implementation of various control algorithms of active power filter topologies in the MATLAB/Simulink environment. The different hardware components as required for the proper operation of experimental set-ups such as isolation and dead-band circuits, voltage and current sensor circuits, non-linear/reactive loads are designed, developed and interfaced with dSPACE.

The developed power circuits are tested initially as a dc-ac inverter to experimentally test the proper working of inverter topologies which are to be further extended to operate as 3P3W active power filters and 3P4W active power filter. A three-phase lamp load is used as load for the inverter. The line-to-line voltage, phase voltage and harmonic spectrum of line-to-line voltage of the inverter are recorded with respective to implemented PWM techniques. From these studies, it is observed that the designed and fabricated inverter topologies are good enough to operate as active power filters.

The developed prototypes are further tested as active power filters with proposed control schemes for harmonic elimination and reactive power compensation and neutral current suppression. These results of experimentation as active power filters are given in the respective discussions in the upcoming chapters with proposed adaptive control schemes integrated with different controller.

CHAPTER 3: ADAPTIVE CONTROL OF THREE LEVEL DIODE CLAMPED ACTIVE POWER FILTER

In this chapter a diode clamped PWM three level inverter used as active power filter, by using the multilevel inverter capabilities such as of low harmonics distortion and reduced switching losses. It is used to compensate the reactive power and eliminates harmonics drawn from nonlinear load. The active power filter control scheme is based on neural network such as least mean square (LMS), anti-Hebbian and anti-Hebbian based on total least square (TLS). The dc side voltage of the shunt active power filter is regulated using PI/type-2 fuzzy logic controller. The level shifted pulse width modulation is implemented to generate the switching pulses for inverter of the active power filter. The performance of the proposed controller is simulated using MATLAB/Simulink environment. The simulated response of the control schemes are validated by developing laboratory prototype. The obtained result shows that proposed active power filter has desired performance.

3.1 Introduction

The power electronics devices and converters such as single phase and three phase rectifier, thyristor converters, adjustable speed drives and arc furnaces introduce considerable harmonic and reactive current in electric power system. It is well fact that harmonics and reactive current do not have any contribution to real power flow and need to be compensated to enhance power quality. In general, current harmonics are responsible for low efficiency, poor power factor, torque pulsation and interference with nearby communication line. To eliminate harmonics and compensate reactive power requirement of the nonlinear load two level active power filter has been widely studied. However, due to the limited power handling capability of power semiconductors, these converters are limited to low and medium power application only [1-7, 27, 40].

Recently, there has been an increasing interest in using multilevel inverters for high power drives, reactive power and harmonics compensation. Multilevel inverters are the next generation inverter and can be used as active power filter for medium or high power applications solving the problem of power semiconductor limitation. The use of neutral-point-clamped (NPC) inverters allows equal voltage shearing of the series connected semiconductors in each phase. It also provides less voltage stress for semiconductor switches increases the power handling capability, reduces current/voltage harmonics and interference [88, 91, 103, 130, 150].

3.2 Power circuit of DCMLI based active power filter

The schematic diagram of an active power filter based on a three-level voltage converter (NPC) is given inFig. 3.1.This converter can compensate the harmonic currents and reactive

power generated by non-linear loads. This converter operates in the power factor controller in the absence of non-linear load. The L_c three reactors are used to raise the voltage and the current filter, two capacitors C_1 and C_2 are necessary to smooth the DC side voltage. It has twelve switches, each switch is associated with a freewheeling diode with six power diodes for the phases of the output of the connection to the medium voltage. Each switch of the blocking voltage is 1/4 of the DC voltage. Each arm of the converter can be clamped to continuous terminals P, O and Q and produce three switching states. When the upper two switches S_{1a}, S_{2a} are turned ON, the output of this phase is connected to the P terminal of the DC voltage. When both switches medium S_{2a}, S_{1a}' are in the ON position, the phase of the output voltage is connected to the middle point N. Similarly when the two lower switches S_{1a}', S_{2a}' are turned ON, the output of this is connected to the terminal Q. This configuration is capable of delivering three different values of the output voltage of each phase of the converter. The two switches of each phase of the NPC inverter are closed, while the other two are open at each instant of time.

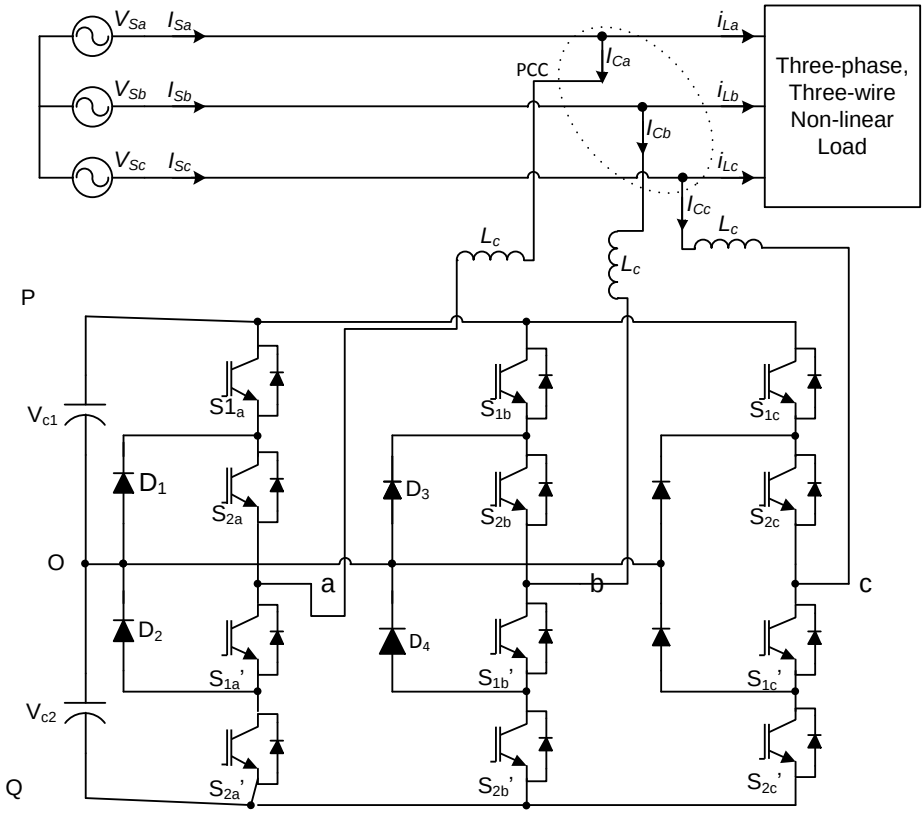


Fig. 3.1. Power circuit of three level active power filter.

3.2.1 Design of passive parameter for the active power filter

Proper design of passive component of active power filter in current tracking mode plays an important role in compensating nonlinear load. The important parameter active power filter is inductance of interfacing reactor and dc side capacitor. Selection of these components depends on the application, operating condition and control strategies.

The following assumptions are made for designing these components

1. Utility voltages area sinusoidal and balanced.
2. The total harmonics distortion of source current is assumed to be less than 5% after compensation with APF
3. The equivalent series resistance R_c associated with interfacing inductor is neglected.
4. Pulse width modulated inverter is assumed to operate in the linear modulation mode (i.e. $0 \le m_a \le 1$, m_a = amplitude modulation index).

3.2.1.1 Selection of DC side Capacitors

The capacitance of the capacitor *C* (in farads) gives its available energy *W* (in joules) written down as follows [53]

$$W = \frac{1}{2}C\left(V_{\text{dcref}}^2 - V_{\text{dc}}^2\right) \tag{3.1}$$

Where V_{dcref} and V_{dc} are (in volts) are the reference and actual capacitor voltages, respectively. From the principles of energy balance equation can be written down as follow:

$$\frac{1}{2}C\left(V_{dcref}^2 - V_{dc}^2\right) = 3V\left(gI\right)t \tag{3.2}$$

$$C_{dc} = 2\frac{3V(gI)t}{\left(V_{dcref}^2 - V_{dc}^2\right)} \tag{3.3}$$

In equation

C_{dc} = Capacitance of the capacitor (in farads),

V_{dc} = Minimum voltage dc bus voltage

V = AC phase voltage of the system

t = Response time of the APF

I = Rated phase current of the converter,

g = Over loading factor.

Considering V_{dc} = 500 V (considering 5% ripple in dc capacitor voltages), $V = \frac{400}{\sqrt{3}}$ V = 230 V,

$I = \frac{20 \times 10^3}{\sqrt{3} \times 400}$ A = 28.869 A, *t* = 300 µs, and *a* = 1.2, the calculated value of C_{dc} is 588.2 µF.

3.2.1.2 Selection of interfacing Inductor

The selection of the interfacing inductor is important task in the design of active power filter. The pulse width modulated active power filter generates undesirable current harmonics around the switching frequency and its multiples. If the switching frequency of the active power filter is sufficiently high, these undesirable current harmonics can be easily filtered out by the interfacing inductor. A proper value of the interface inductor plays a crucial role in

tracking the given reference currents. The connection of the interfacing inductor to the AC system is shown inFig. 3.1 .

The proper design of the interfacing inductance depends on the current ripple $i_{cr,(p-p)}$ and switching frequency of the active power filter (f_c). The value of the interfacing inductance is written down as follows [53]:

$$L_C = \frac{\sqrt{3} m_a V_c}{12 g f_c i_{cr,(p-p)}} \tag{3.4}$$

Where, switching frequency of the converter (f_c) depends on the PWM method used for generating switching pulses. For level-shifted PWM technique with carrier signal frequency f_{cr}, f_c can be calculated as:

$$f_c = 2 f_{cr} \tag{3.5}$$

Considering 5% peak-to-peak current ripple $\left(i_{cr,(p-p)}\right)$ to be 1.2A rms, the switching frequency of the inverter ($2f_{cr}$) = 2×2 kHz = 4 kHz, amplitude modulation index (m_a) = 1, phase-to-neutral of the inverter (V_c) = 230V and overload factor (g) = 1.2, the value is calculated to be 5.7mH.

3.3 Reference current generation

The performance of the active power filter depends on its reference current generation. The instantaneous source voltage is

$$v_s(t) = V_m \sin(\omega t) \tag{3.6}$$

When the nonlinear load connected to the source, then it injects the current harmonics in the source. The load current consist of both fundamental and harmonics components, which can be expressed as follows:

$$\begin{aligned} i_L(t) &= \sum_{n=1}^{\infty} I_n \sin(n\omega t + \phi_n) \\ &= I_1 \sin(\omega t + \phi_1) + \sum_{n=2}^{\infty} I_n \sin(n\omega t + \phi_n) \end{aligned} \tag{3.7}$$

Thus, the instantaneous load power can be expressed as follows:

$$\begin{aligned} i_L(t) &= I_1 \sin(\omega t) * \cos(\phi_1) + \\ & I_1 \sin(\phi) * \cos(\omega t) + \sum_{n=2}^{\infty} I_n \sin(n\omega t + \phi_n) \end{aligned} \tag{3.8}$$

The load current is modelled as:

$$i_L(t) = i_f(t) + i_r(t) + i_h(t) \tag{3.9}$$

$$i_L(t) = i_f(t) + i_c(t) \tag{3.10}$$

The compensating current is the sum of the reactive and harmonics current. The compensating current injected by active power filter is

$$i_c(t) = i_L(t) - i_f(t) = i_L(t) - I_1 \cos(\phi) \sin(\omega t)$$

From (6), after compensation, the current supplied by the source is

Where $I_m = I_1 \cos\phi_1$

$$i_c(t) = i_L(t) - I_m \sin(\omega t) \tag{3.11}$$

The voltage across the dc side capacitors varies with the load demand. In order to maintain dc capacitors voltage constant, the PI/type-2 fuzzy logic controller is used [76]. Under this conditions, assuming that the current drawn from the source is sinusoidal and in phase with respective voltages. The instantaneous value of source current is

$$i_s(t) = I_m \sin(\omega t) \tag{3.12}$$

The power delivered by the source

$$p_s(t) = \frac{1}{2} V_m I_m - \frac{1}{2} V_m I_m \cos(2\omega t) = p_{dc} + p_{ac} \tag{3.13}$$

Where p_{dc} and p_{ac} are ac and dc component of the power delivered by the source. The load real power can be expressed as

$$p_l(t) = V_m \sin(\omega t) \times I_1 \sin(\omega t + \phi_1) + V_m \sin(\omega t) \sum_{n=2}^{\infty} I_n \sin(n\omega t + \phi_n) \tag{3.14}$$

$$p_l(t) = \frac{1}{2} I_1 \cos(\omega t) + p_{lac} = p_{lac} + p_{ldc} \tag{3.15}$$

Where p_{lac} and p_{ldc} are ac and dc components of the load power. The compensating power injected by the active power filter is

$$p_c(t) = p_s(t) - p_l(t) \tag{3.16}$$

$$p_c(t) = (p_{dc} - p_{ldc}) + (p_{ac} - p_{lac}) \tag{3.17}$$

Assume that the reference voltage is V_{dc} and the change in reference voltage is δV_{dc} due load disturbance. The change in energy handled by the capacitor is

$$\delta E = \frac{1}{2} C (V_{dc} + \delta V_{dc})^2 - \frac{1}{2} C V_{dc}^2 \tag{3.18}$$

The ΔV_{dc}^2 is small as compared to ΔV_{dc}

$$\delta E = \frac{1}{2} C \times V_{dc} \times \delta V_{dc}$$

$$\delta E = p_{cdc} T \tag{3.19}$$

$$\delta V_{dc} = \frac{V_m}{2 C V_{dc}} \left(I_m - I_1 \cos(\phi_1) \right)$$

$$\delta V_{dc} = k\left(I_m - I_1\cos\left(\phi_1\right)\right) \tag{3.20}$$

Where

$$k = \frac{V_m}{2CV_{dc}}$$

$$\delta V_{dc} = k\left(I_m - W_p\right)$$

$$I_m = \left(W_p + \frac{1}{k}\delta V_{dc}\right) \tag{3.21}$$

$$I_m = \left(W_p + W_{dc}\right)$$

Where weight W_p is the active component of the load current. The weight W_{dc} is associated with the dc voltage regulation.

$$I_m = W_A \tag{3.22}$$

Then the compensating current (5) can be modified as

$$i_c\left(t\right) = i_L\left(t\right) - W_A\sin\left(\omega t\right) \tag{3.23}$$

According to the least square algorithm, the weight for next iteration can be expressed as

$$W_{A(i+1)} = W_A + ri_c\left(t\right)\sin\left(\omega t\right) \tag{3.24}$$

$$W_{B(i+1)} = W_B + ri_c\left(t\right)\sin\left(\omega t - \frac{2\pi}{3}\right) \tag{3.25}$$

$$W_{C(i+1)} = W_C + ri_c\left(t\right)\sin\left(\omega t - \frac{4\pi}{3}\right) \tag{3.26}$$

The control strategy for derived equation is given in Fig. 3.2.

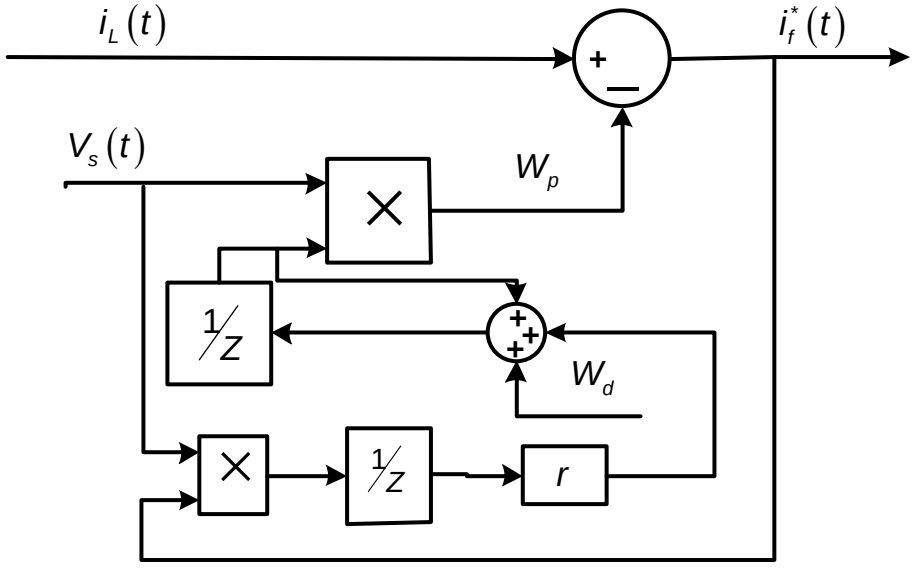


Fig. 3.2: Reference current generation using LMS algorithm for phase-a.

The reference current for active power filter according to Anti-Hebbian algorithm [74] from (3.22) as shown in Fig. 3.3.

$$W_{A(i+1)} = W_A + ri_c(t)\left(\sin(\omega t) + i_{la}(t)W_A\right) \tag{3.27}$$

$$W_{B(i+1)} = W_B + ri_c(t)\left(\sin\left(\omega t - \frac{2\pi}{3}\right) + i_{lb}(t)W_B\right)$$

$$W_{C(i+1)} = W_C + ri_c(t)\left(\sin\left(\omega t - \frac{4\pi}{3}\right) + i_{lc}(t)W_C\right) \tag{3.29}$$

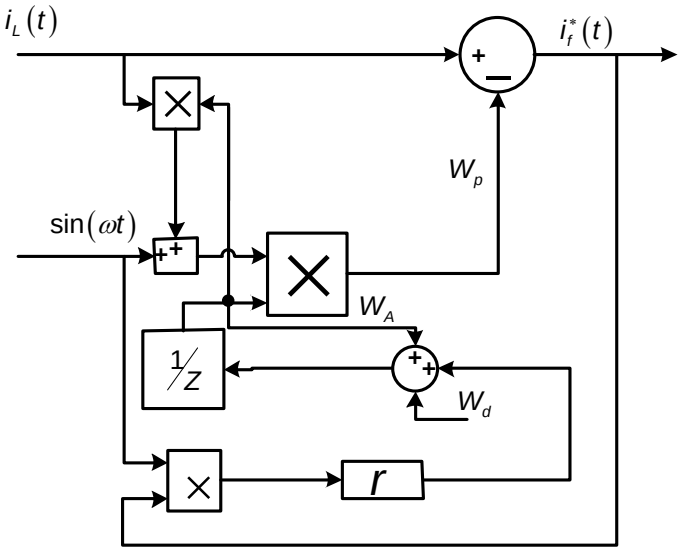


Fig. 3.3: Reference current generation using Anti-Hebbian algorithm for phase-a.

The reference current generations for active power filter according to Anti-Hebbian algorithm based on TLS [141] from (3.22) as shown in Fig. 3.4.

$$W_{A(i+1)} = W_A + ri_c(t)\left(\sin(\omega t) + ki_{la}(t)W_A\right) \tag{3.30}$$

$$W_{B(i+1)} = W_B + ri_c(t)\left(\sin\left(\omega t - \frac{2\pi}{3}\right) + ki_{lb}(t)W_B\right) \tag{3.31}$$

$$W_{C(i+1)} = W_C + ri_c(t)\left(\sin\left(\omega t - \frac{4\pi}{3}\right) + ki_{lc}(t)W_C\right) \tag{3.32}$$

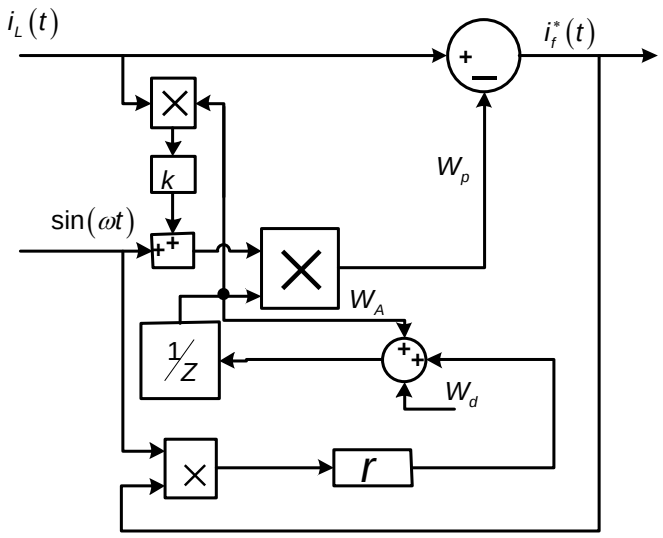


Fig. 3.4: Reference current generation using anti-Hebbian based on TLS algorithm for phase-a.

3.3.1 Type-2 fuzzy logic controller (T2FLC)

Fuzzy sets were designed mathematically to represent vagueness and uncertainty of linguistic problems. Fuzzy logic is form of logic, which deals with approximate rather than precise mode of reasoning. The most of the controller that have been used to date were based on the type-1 fuzzy logic controller. However, the type-1 fuzzy controllers have difficult in modeling and minimizing the effect of uncertainty. One the limiting the ability of type-1 fuzzy logic is its membership function (MF) which handles uncertainty and takes crisp value as input. Recently, type-2 fuzzy set introduced, which deal with a fuzzy-fuzzy sets where the grade of membership is type-1 fuzzy sets rather than the crisp value as input.

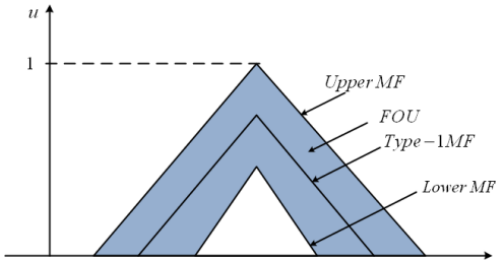


Fig. 3.5: Type-2 fuzzy sets.

Fig. 3.5: illustrates the type-2 fuzzy MF can be obtained by starting with type-1 fuzzy membership function and then blurring it [76, 77]. The blurred area represent the foot point of uncertainty (FOU), which is nothing but the area bounded between the lower and upper MFs and represents the capacity to handle the degree of uncertainty. Type-2 fuzzy logic is very useful in certain application where it is difficult determine the exact membership function for fuzzy set. Therefore, it is effective in handling the uncertainties associated with process. The block diagram of the type-2 fuzzy logic controller is shown in Fig. 3.6. The process involve type-2 fuzzy logic controller is fuzzification, inference, type reduction and defuzzification.

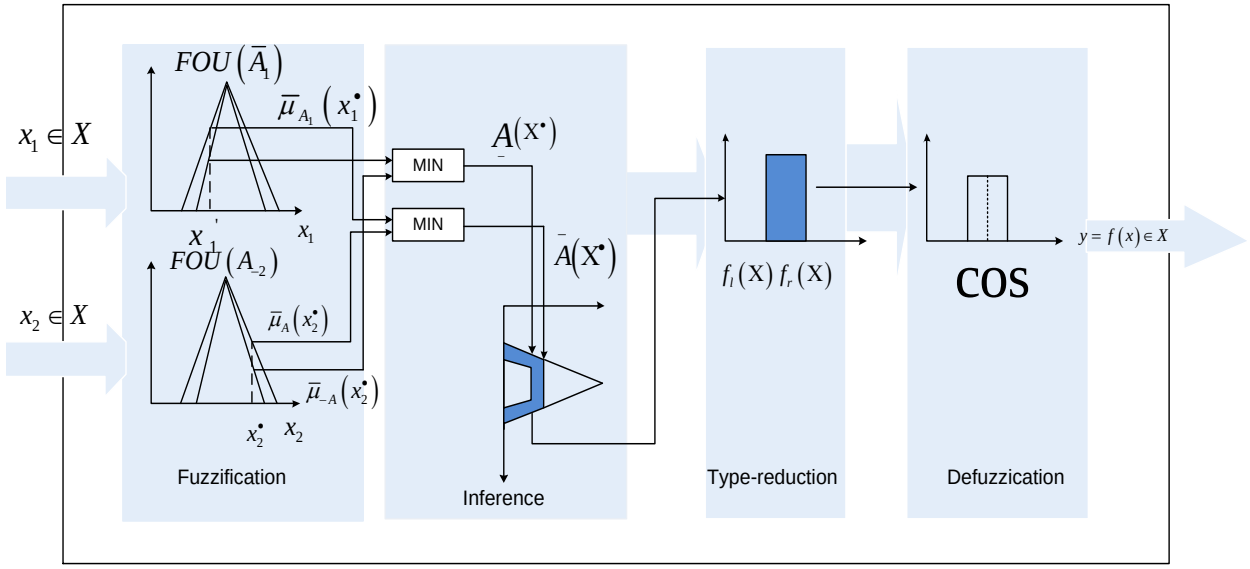


Fig. 3.6: Block diagram of type-2 fuzzy logic controller.

3.3.1.1 Fuzzifier

The Fuzzifier converts the numeric vector $x = (x_1 x_2 ... x_p) \in X_1 \times X_2 \times ,.... \times X_p = X$ into a type-2 fuzzy set $\tilde{A}_x$ in x an interval type-2 fuzzy set in this case. We use type-2 singleton fuzzifier, in a singleton fuzzification, the input fuzzy set has only a single point on nonzero membership. $\tilde{A}_x$ is type-2 fuzzy sets singleton if $\mu_{\tilde{A}_x}(x) = 1/1 \,|$ for $x = x^{'}$ and $\mu_{\tilde{A}_x}(x) = 1/0 \,|$ for $x \neq x^{'}$

3.3.1.2 Rule base

The rule base of type-2 fuzzy logics controller is same as that of type-1 fuzzy logic controller, where antecedent and consequent represented by type-2 fuzzy sets. The type-2 fuzzy set with n input $x_1 \in X_1 , ... x_p \in X_p$ and one output $y \in Y$, known as multiple input and single output. If we assume there are *M* rules, the i^{th} rule in the type-2 Fuzzy logic set can be written down as follows:

$$R^l : \tilde{F}_1^i \times ..... \tilde{F}_n^i \rightarrow \tilde{G}^i = \tilde{A}^i \rightarrow \tilde{G}^i \quad i = 1, ... M \tag{3.32}$$

3.3.1.3 Rule inference

The inference engine combines rules and gives a mapping from input type-2 fuzzy sets to output type-2 fuzzy sets. It is perform the union, intersection as well as extended sup-star compositions (sup star compositions) of type-2 relations.

3.3.1.4 Type reducer

The type-reducer of type-2 fuzzy logic controller generates a type-1 fuzzy set output, which is then converted in a crisp output with the defuzzifier. This type-1 fuzzy set is also an interval set, for the case of type-2 fuzzy logic set we used center of sets (cos) type reduction, Y_{cos}, which can be expressed as

$$Y_{\cos} = [y_l, y_r] = \int_{y^1 \in [y_l^1, y_r^1]} \cdots \int_{y^M \in [y_l^M, y_r^M]} \int_{f^1 \in [\underline{f}^1, \bar{f}^1]} \cdots \int_{f^M \in [\underline{f}^M, \bar{f}^M]} 1 \Big/ \frac{\sum_{i=1}^{M} f^i y^1}{\sum_{i=1}^{M} f^i} \tag{3.33}$$

This interval set is determined by its two end points, y_l and y_r, which corresponds to the centroid of the type-2 interval consequent set $\tilde{G}^i$,

$$C_{\tilde{G}_i} = \int_{\theta_1 \in J_{y1}} \cdots \int_{\theta_N \in J_{yN}} 1 / \frac{\sum_{i=1}^{N} y_i \theta_i}{\sum_{i=1}^{N} \theta_i} = [y_l^i, y_l^r] \tag{3.34}$$

Before the computation of Ycos (x), we must evaluate Eq. (3.33), and its two end points, y_l and y_r. If the values of f_i and y_i that are associated with y_l are denoted f_l^i and y_l^i, respectively, and the values of fi and y_i that are associated with yr are denoted f_r^i and y_r^i, respectively, from Eq. (13), we have

$$y_l = \frac{\sum_{i=1}^{M} f_l^i y_l^i}{\sum_{i=1}^{M} f_l^i} \tag{3.35}$$

$$y_r = \frac{\sum_{i=1}^{M} f_r^i y_r^i}{\sum_{i=1}^{M} f_r^i} \tag{3.36}$$

The values of y_l and y_r define the output interval of the type-2 fuzzy system, which can be used to verify if training or testing data are contained in the output of the fuzzy system.

3.3.1.5 Defuzzifier

From the type-reducer, we obtain an interval set Y_{cos}, to defuzzify it we use the average of y_l and y_r, so the defuzzified output of an interval singleton type-2 fuzzy logic set is

$$y(x) = \frac{y_l + y_r}{2} \tag{3.37}$$

3.3.1.6 DC voltage regulation

The type-2 fuzzy logic controller used in this application is shown in Fig. 3.7. The inputs to the type-2 fuzzy logic controller are error *e* and rate of change of error ce

$$e_n = \Delta v_{dc(n)} = v_{dc(n)}^{*} - v_{dc(n)} \tag{3.38}$$

$$ce_n = \Delta v_{dc(n)} = v^*_{dc(n)} - v_{dc(n-1)} \tag{3.39}$$

The type-2 fuzzy logic controllers compute the change in desired current. The peak reference current $W_d(n)$, at the n[th] sampling time, is determined by adding the previous reference current $W_d(n-1)$ to the calculated change in reference current

$$W_d = W_d(n-1) + \delta W_d(n) \tag{3.40}$$

Where is the sampling time, W_d is the peak value of desired reference current at n[th] sampling time and is gain factor of the type-2 fuzzy logic controller. The rule base of the type-2 fuzzy logic controller is shown in Table 3.1.

Table 3.1: Rule matrix for voltage regulation.

E/CE	NL	NM	NS	ZE	PS	PM	PL
NL	NL	NL	NL	NL	NM	NS	ZE
NM	NL	NL	NL	NM	NS	ZE	PS
NS	NL	NL	NM	NS	ZE	PS	PM
ZE	NL	NM	NS	ZE	PS	PM	PL
PS	NM	NS	ZE	PS	PM	PL	PL
PM	NS	ZE	PS	PM	PL	PL	PL
PL	NL	NM	NS	ZE	PS	PM	PL

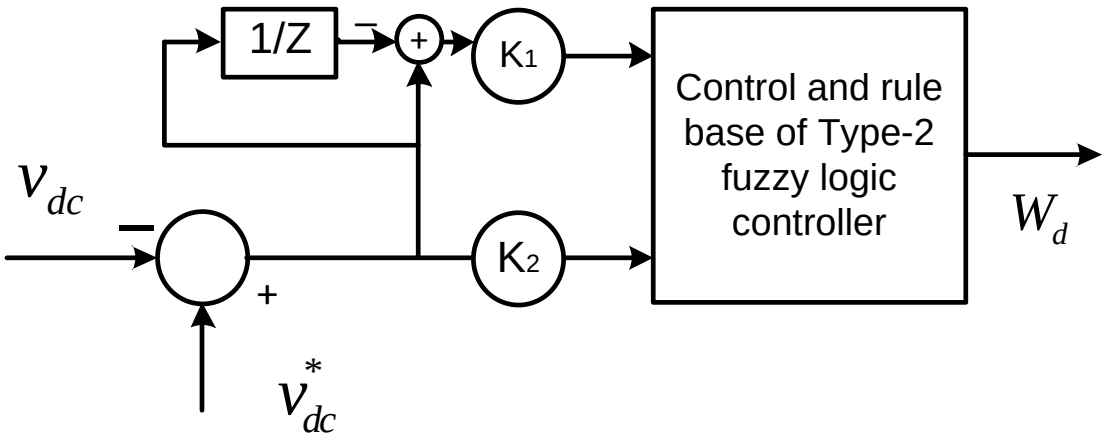


Fig. 3.7: type-2 fuzzy logic controller for dc voltage regulation.

The dc side capacitor voltage regulation loop is shown inFig. 3.8.

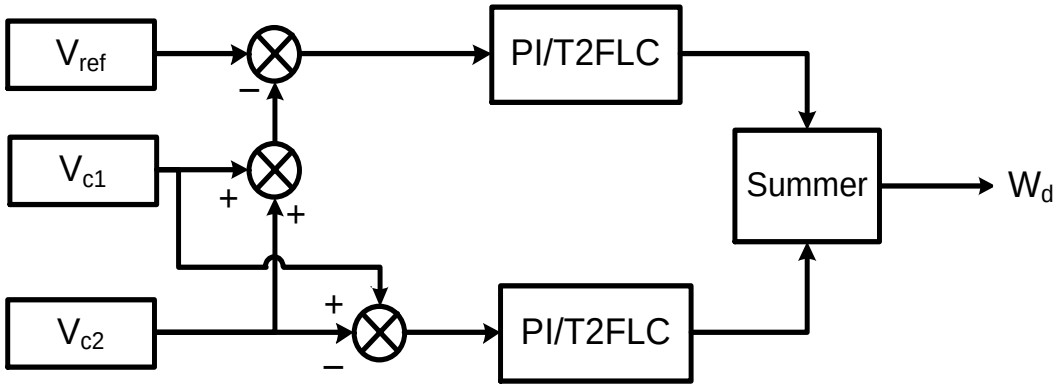


Fig. 3.8 dc voltage regulation loop.

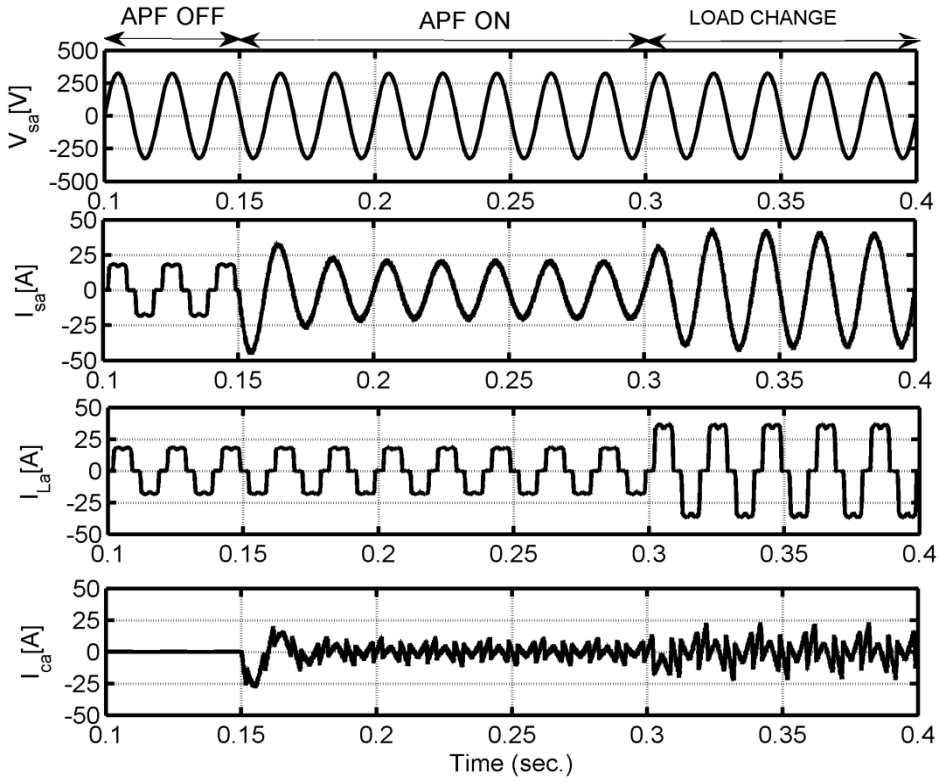
3.3.2 Control scheme based on LMS algorithm integrated with PI/T2FLC

3.3.2.1 Simulations results

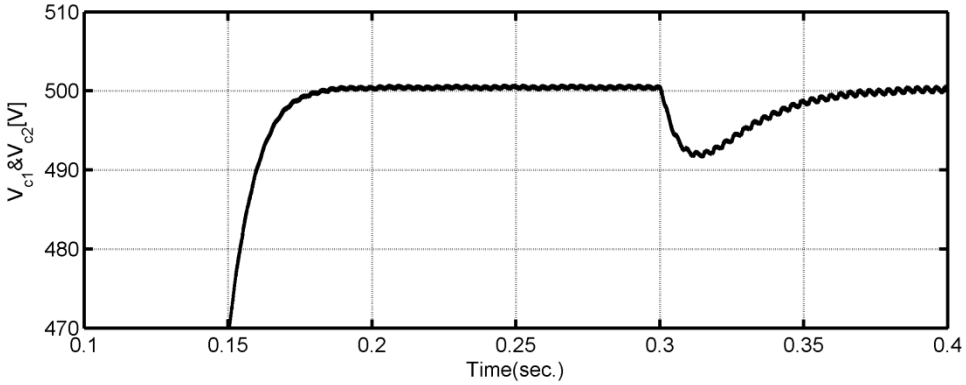
Simulation results of the active power filter with uncontrolled rectifier on its dc presented in this section. The control scheme for the active power filter has also been modelled in MATLAB/Simulink environment using Simpower system block sets. The reference source currents have been derived from the LMS algorithm discussed in Section 3.3 by using the measured ac voltages, load currents and dc side capacitors voltage of the active power filter.

An uncontrolled rectifier with RL load on dc side is used as nonlinear load. Fig. 3.9 (a)-(d) shows the simulated response of currents, dc side capacitor voltages and harmonics spectrum respectively of active power filter using LMS algorithm integrated with PI controller. Fig. 3.10: shows the simulated response of currents, dc side capacitor voltages and harmonics spectrum respectively of active power filter using LMS algorithm integrated with type-2 fuzzy logic controller. After compensation with active power filter, in both the cases the source current is changed from stepped waveform to sinusoidal waveform as seen in Fig. 3.9 (a) and Fig. 3.10 (a). Source current is in phase with source voltage to conform the power factor becomes almost unity. After compensation with active power filter, the load current THD is 26.7% but the source current THD is reduced to 3.41% and 3.40% using LMS algorithm integrated with PI controller and LMS integrated with T2FLC respectively as shown in Fig. 3.9 (d) and with Fig. 3.10 (d). In both the cases dc side capacitor voltage is regulated at reference level but the settling time required for dc side capacitor to attain reference value is 0.06s and 0.05s for LMS integrated with PI and T2FLC respectively as observed from Fig. 3.9 (b) and Fig. 3.10 (b). At instant t=0.3s, load current is increased from 20.2A to 40A. The corresponding change in the source current, compensating current dc side capacitors

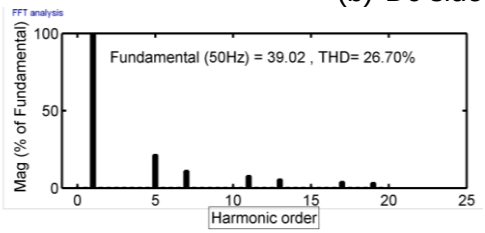
voltages has been observed to be compensating the increased load current. However, the increase of compensating current observed to be smooth in case of LMS integrated with



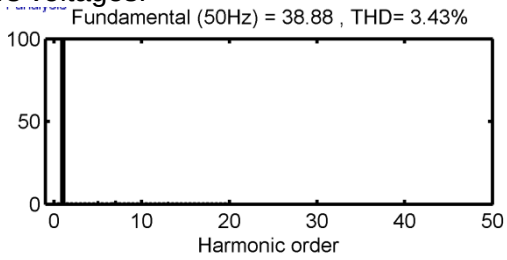
(a) Compensation characteristics of APF using anti-Hebbian with PI controller.



(b) Dc side capacitors voltages.



(c) Source current without compensation

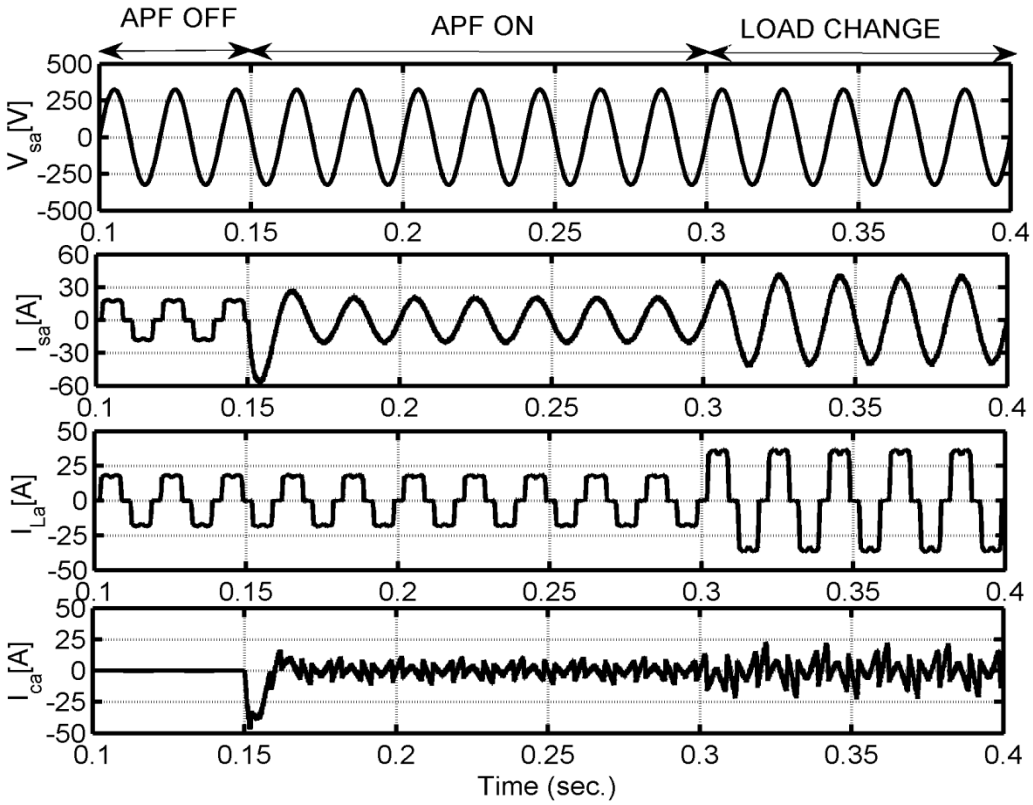


(d) Source current THD Spectrum with compensation.

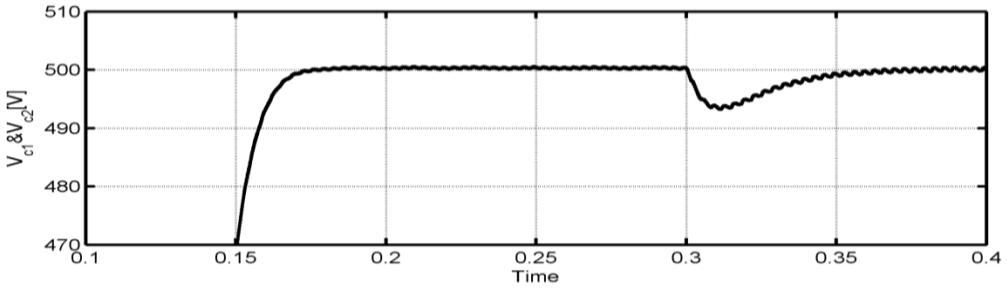
Fig. 3.9: Performance of APF for an RL load on the dc side of an uncontrolled rectifier using anti-Hebbian algorithm integrated with PI controller.

T2FLC than the PI-controller. The increased load current also causes the decrease in the dc side capacitors voltage from it reference value to compensate increase in load current.

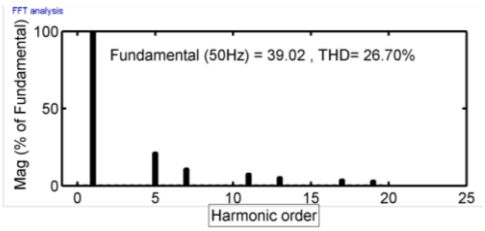
The settling time of the dc side capacitors voltage is 20ms and 10ms for LMS algorithm based control scheme integrated with T2FLC and PI-controller respectively. The dc voltage regulation is smooth in both the cases but restoration time is more in case of LMS integrated with PI than with the T2FLC controller. This shows effectiveness of LMS algorithm integrated with T2FLC controller for dc voltage regulation in transient also.

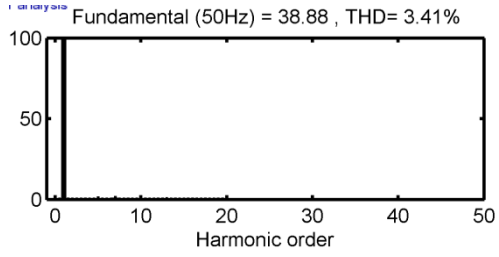


(a) Compensation characteristics of APF using anti-Hebbian with T2FLC controller



(b) DC side capacitors voltages.





(c) Source current without compensation (d) Source current THD Spectrum with compensation.

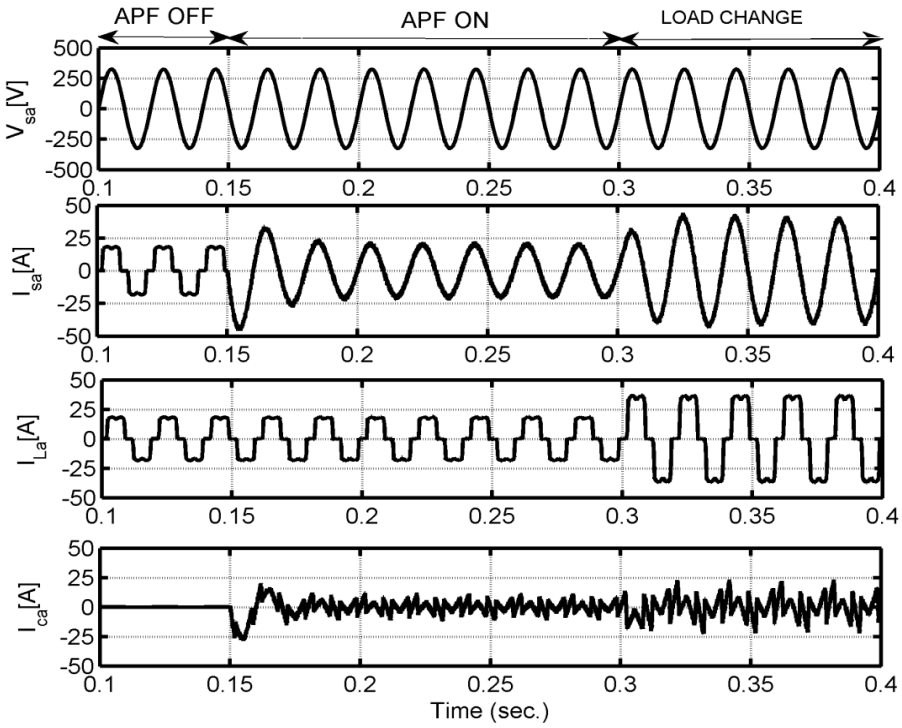
Fig. 3.10: Performance of APF for RL load on the dc side of an uncontrolled rectifier using anti-Hebbian algorithm integrated with T2FLC-controller.

3.3.3 Control scheme based on anti-Hebbian Algorithm integrated with PI/T2FLC

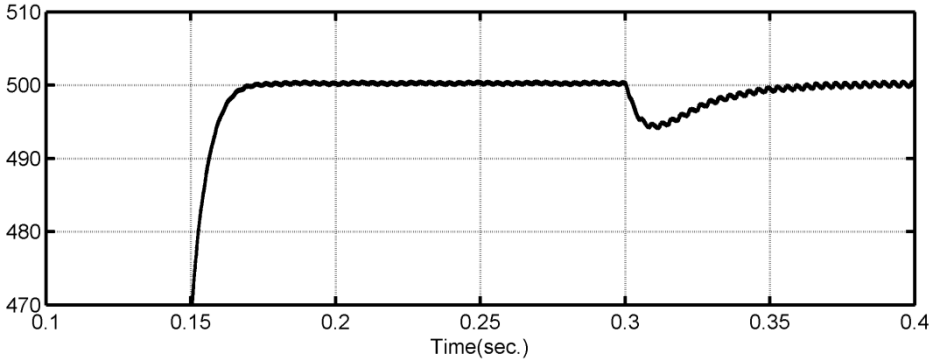
3.3.3.1 Simulations results

Simulation results of the active power filter with uncontrolled rectifier on its dc presented in this section. The control scheme for the active power filter has also been modelled in MATLAB/Simulink environment. The reference source currents have been derived from the anti-Hebbian algorithm discussed in Section 52 by using the measured ac voltages, load currents and dc side capacitors voltage of the active power filter.

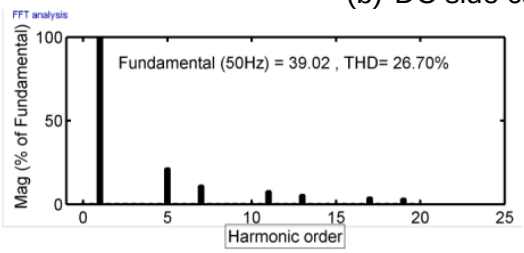
An uncontrolled rectifier with RL load on dc side is used as a nonlinear load. Fig. 3.11 (a)-(d) shows the simulated response of source currents, dc side capacitor voltages and harmonics spectrum respectively of active power filter using anti-Hebbian algorithm integrated with PI controller. Fig. 3.12 (a)-(d) shows the simulated response of currents, dc side capacitor voltages and harmonics spectrum respectively of active power filter using anti-Hebbian algorithm integrated with type-2 fuzzy logic controller. After compensation with active power filter, in both the cases the source current is changed from stepped waveform to sinusoidal waveform as seen in Fig. 3.11 (a) and Fig. 3.12 (a). Source current is in phase with source voltage to conform the displacement factor and power factor becomes almost unity. After compensation with active power filter, the load current THD is 26.7% but the source current THD is reduced to 3.41% and 3.40% using anti-Hebbian algorithm integrated with PI controller and LMS integrated with T2FLC respectively as shown in Fig. 3.11 (d) and Fig. 3.12 (d). In both the cases dc side capacitor voltage is regulated at reference level but the settling time required for dc side capacitor to attain reference value is 20ms and 10ms for anti-Hebbian integrated with PI and T2FLC respectively as evident from Fig. 3.11 (b) and Fig. 3.12 (b). At instant t=0.3s, load current is increased from 20.2A to 40A. The corresponding change in the source current, compensating current dc side capacitors voltages has been observed to be compensating the increased load current. However, the increase of compensating current observed to be smooth in case of anti-Hebbian integrated with T2FLC than the PI-controller. The increased load current also causes the decrease in the dc side capacitors voltage from it set reference value to compensate increase in load current. The settling time of the dc side capacitors voltage is 0.03s and 0.04s for anti-Hebbian algorithm based control scheme integrated with T2FLC and PI-controller respectively. The dc voltage regulation is smooth in both the cases but restoration time is more in case of anti-Hebbian integrated with PI than with the T2FLC. This ensure effectiveness of anti-Hebbian algorithm integrated with T2FLC controller for dc voltage regulation in transient also



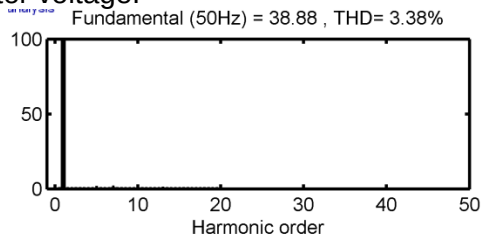
(a) Compensation characteristics of APF using anti-Hebbian with PI controller



(b) DC side capacitor voltage.

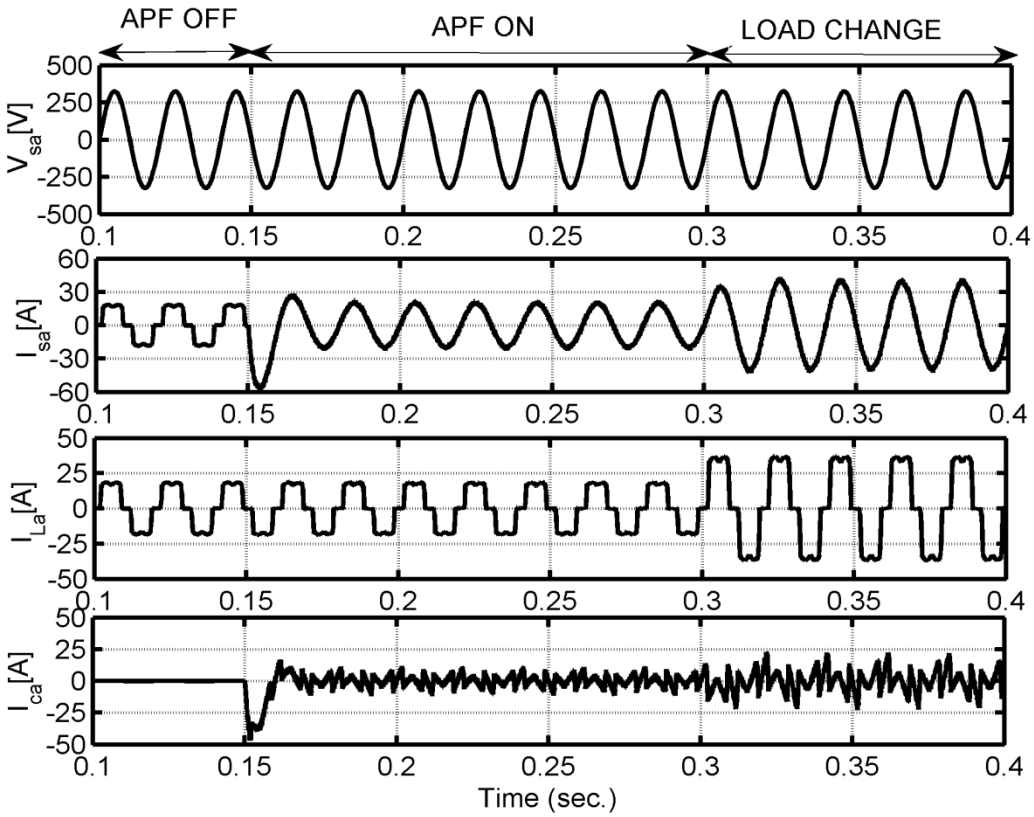


(c)Source current without compensation

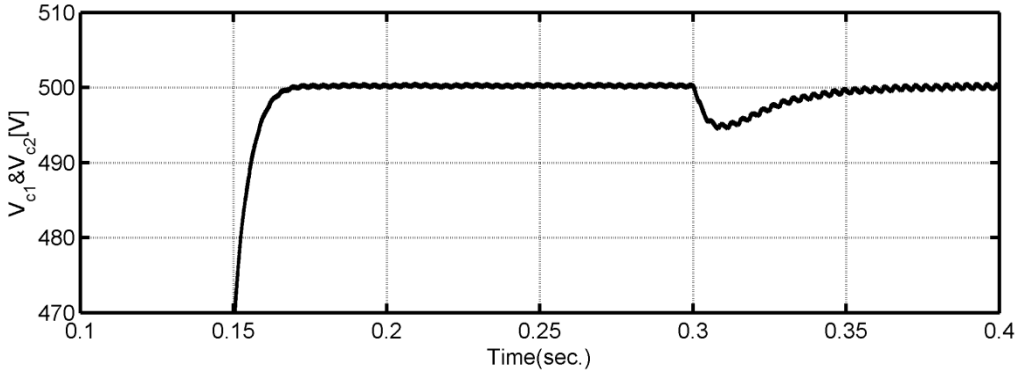


(d) Source current THD Spectrum with compensation.

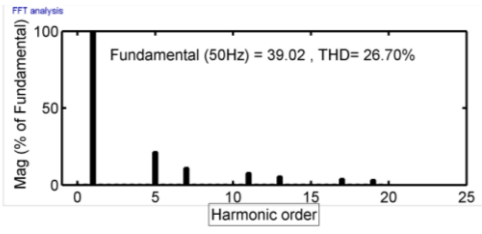
Fig. 3.11: Performance of APF for an RL load on the dc side of an uncontrolled rectifier using anti-Hebbian algorithm integrated with PI controller.



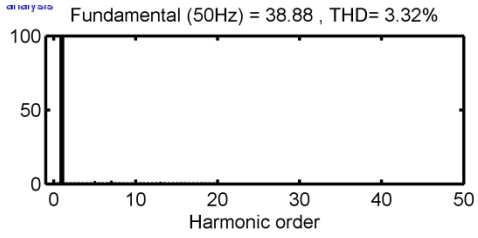
(a) Compensation characteristics of APF using anti-Hebbian with T2FLC controller



(b) DC side capacitors voltages.



(c) Source current without compensation



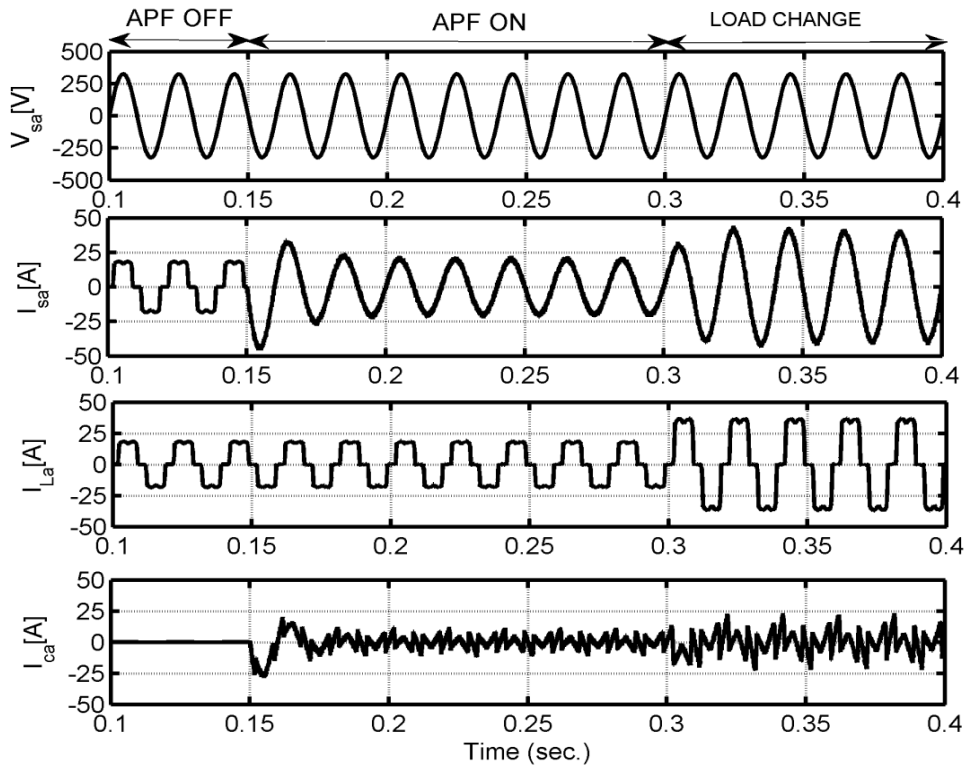
(d) Source current THD Spectrum with compensation.

Fig. 3.12: Performance of APF for an RL load on the dc side of an uncontrolled rectifier using anti-Hebbian algorithm integrated with T2FLC-controller.

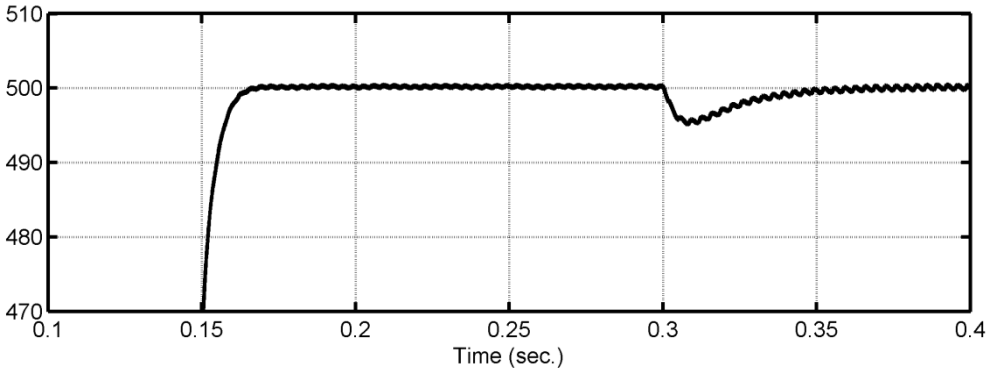
3.3.4 Anti-Hebbian based on total least square algorithm.

3.3.4.1 Simulation results

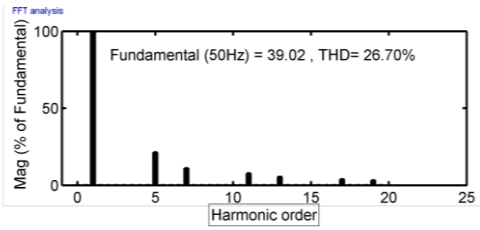
The six pulse uncontrolled rectifier with RL load on the dc side has been considered as a nonlinear load in this case. Fig. 3.13 (a)-(d) shows the simulated response of source current, compensating current, dc side capacitor voltages (V_{c1} to V_{c2}), harmonic spectra of load and source currents respectively with anti-Hebbian based on TLS integrated PI, while Fig. 3.14 (a)-(d) shows the simulated response of source currents, compensating current, dc side capacitor voltages (V_{c1} to V_{c2}), harmonic spectra of load and source currents respectively with anti-Hebbian based on TLS integrated T2FLC. At instant t=0.15s, when APF is switched-on the source current tend to sinusoidal from stepped waveform in both the cases as shown in Fig. 3.13 (a) and Fig. 3.14 (a). After compensation with active power filter, the load current THD is 26.7% but the source current THD is reduced to 2.41% and 2.1% using anti-Hebbian based on TLS integrated with PI controller and anti-Hebbian based on TLS integrated with T2FLC controller respectively as shown in Fig. 3.13 (d) and Fig. 3.14 (d). After compensation with active power filter source power factor has been improved from 0.78 to almost in unity in both the cases. At 0.3 sec., load current is increased from 20.0 A to 40.16 A. The corresponding change in the source current and compensating current have been observed to be very smooth in both cases. However, the number of cycle required for source current to attain steady state is 3-4 cycles and 2-3 cycles for anti-Hebbian algorithm based on TLS integrated with PI and T2FLC respectively. At instant APF is switched-on at t=0.15s, dc side capacitors voltages increases gradually in both cases. However, the settling time required for dc voltage to attain reference level is 0.05s in case of the anti-Hebbian algorithm integrated with PI and in case of T2FLC settling time required is 0.005s as seen in Fig. 3.13 (b) and Fig. 3.14 (b). When load current is changes at t=0.3s, the dc side capacitors voltage changes from its set reference level to compensate the increase in load current. This which causes drop in capacitor voltage is restored in 0.035s and 0.02s for anti-Hebbian integrated based on TLS integrated with PI and T2FLC respectively. This shows that the transient performance of the active power filter with T2FLC better than that of the PI controller.



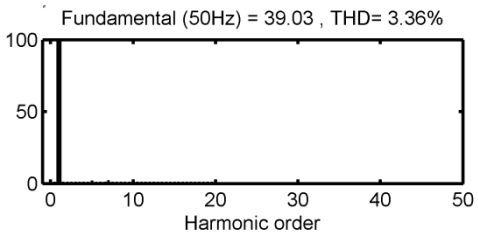
(a)Compensation characteristics of APF using anti-Hebbian with PI controller



(b) DC side capacitors voltages

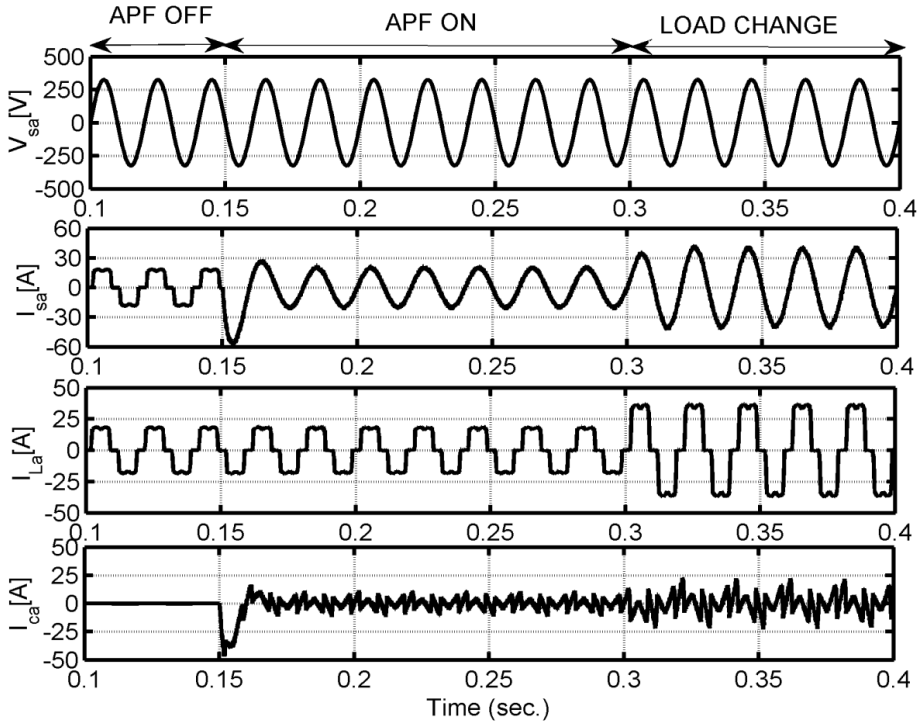


(c) Source current without compensation

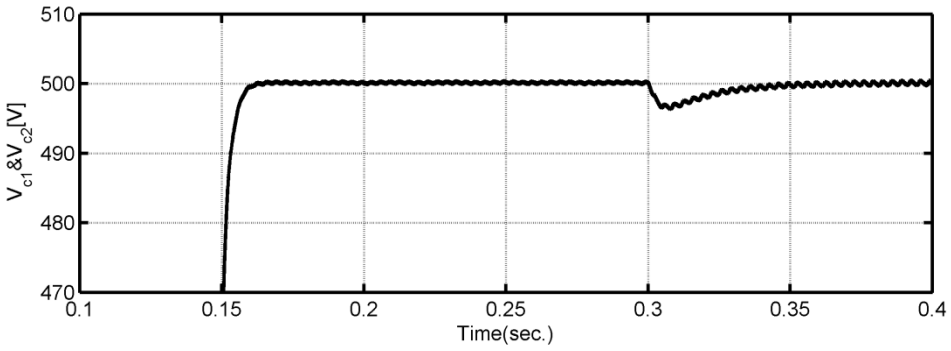


(d) Source current THD Spectrum with compensation.

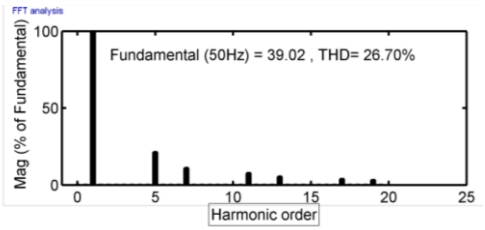
Fig. 3.13: Performance of APF for an RL load on the dc side of an uncontrolled rectifier using anti-Hebbian algorithm based on TLS integrated with PI controller.



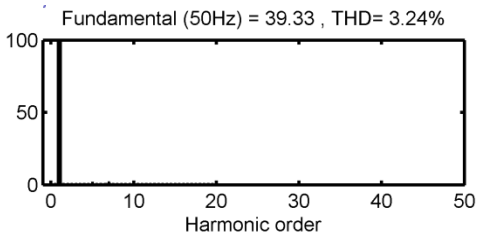
(a) Compensation characteristics of APF using anti-Hebbian with T2FLC controller



(b) Dc side capacitors voltages.



(c) Source current without compensation



(d) Source current THD Spectrum with compensation.

Fig. 3.14: Performance of APF for an RL load on the dc side of an uncontrolled rectifier using anti-Hebbian algorithm based on TLS integrated with T2FLC controller.

3.4 Experimental validation

In this chapter simulation studies are carried out at 400V. However, due to the constraints involved in the development of prototype model, the experimental studies have been conducted at a reduced line voltage of 100V. The downscaled prototype model of the three level active power filter has been developed for investigation of different control schemes integrated with PI/ type-2 fuzzy logic controller. The line to line voltage waveforms of the three level diode clamped active power filter are shown in Fig. 3.15 (a)-(c) (scales for these figures: X-axis-10ms/div., Y-axis-50V/div). The six pulse uncontrolled rectifier with RL-load on dc side used as nonlinear load. The distorted source phase currents and its harmonics spectrum without compensation are shown in Fig. 3.16.

(a) (b) (c)

Fig. 3.15: line to line voltage of three level active power filter.

3.4.1 Control scheme based on LMS algorithm integrated with T2FLC

The down scaled prototype of the active power filter has been developed and tested for harmonic elimination and reactive power compensation with LMS algorithm integrated with PI controller and T2FLC controllers and the experimental waveforms under steady state condition are shown in Fig. 3.17. The source voltage, source current, load current and compensating current for phase-*a* with PI and T2FLC is shown in Fig. 3.17 (a) and in Fig. 3.17 (b) respectively. These figures and all the subsequent figures showing similar experimental results, the different waveforms are recognized as:

Channel–1: source voltage (X-axis: 10 ms/div., Y-axis: 100 V/div.),

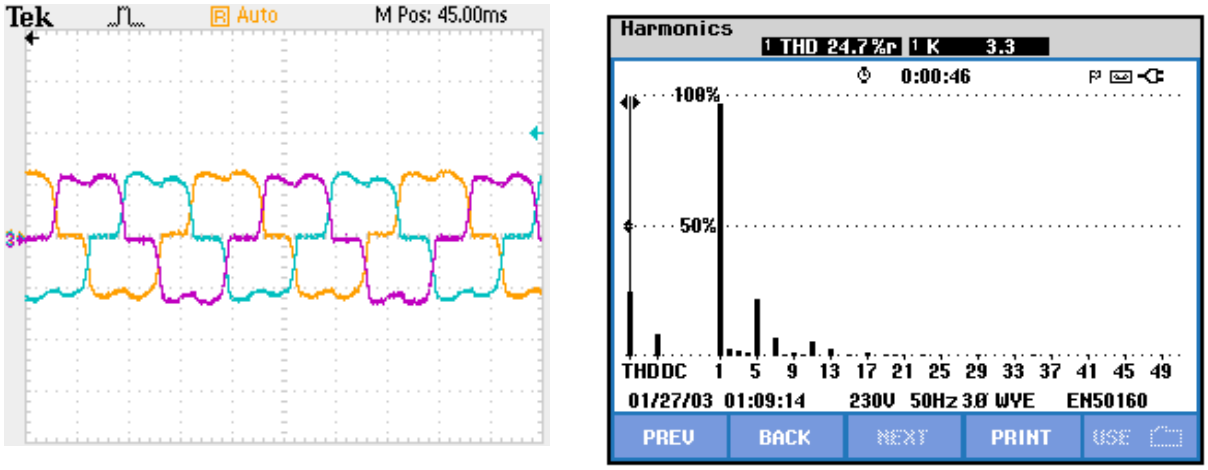
Channel–2: source current after compensation (X-axis: 10ms/div., Y-axis:5 A/div.),

Channel–3: load current (X-axis: 10 ms/div., Y-axis: 5A/div.),

Channel–4: compensating current injected by the Active power filter (X-axis: 10 ms/div., Y axis: 5 A/div.).

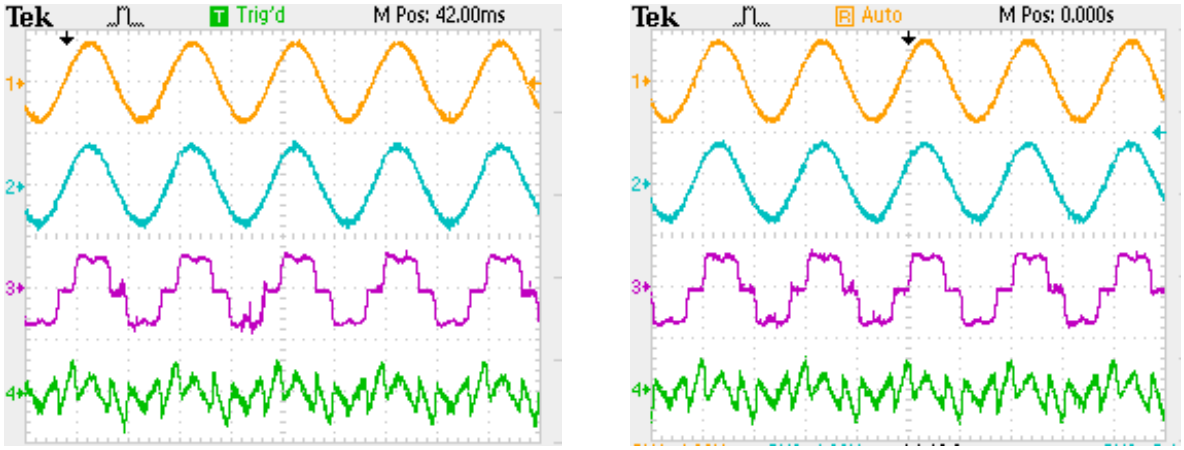
The THD spectrum of load current after compensation with PI controller and T2FLC controller are shown in Fig. 3.17 (c) and (d) respectively. From these figures it is observed that after compensation with active power filter, the load current %THD 24.7%, but source current %THD is reduced to 3.2% and 3.1% with PI controller and T2FLC controller respectively. The power factor becomes unity in both the cases. However, the steady state

performance of active power filter with PI controller and T2FLC are identical. The source currents THDs after compensation with active power filter are well within the limits imposed by IEEE–519–1992 standard in both the cases.

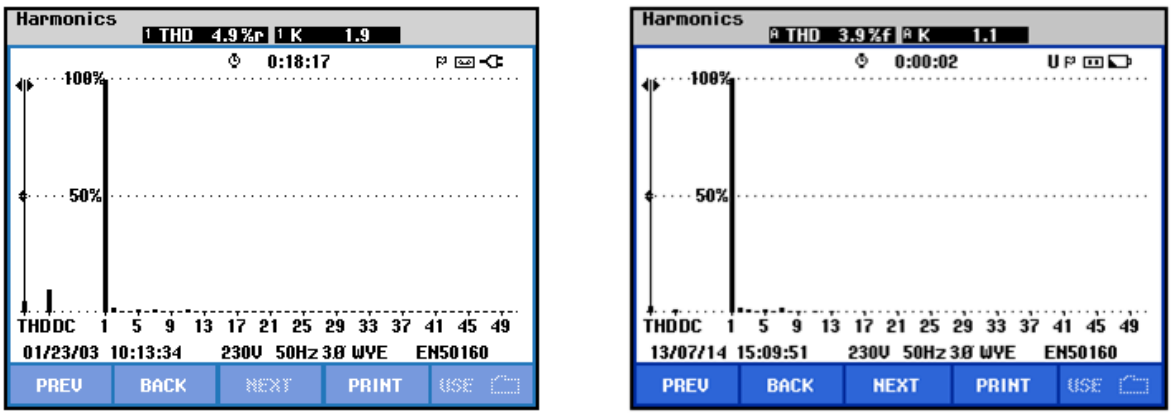


(a) (b)

Fig. 3.16: (a) Three phase load current (b) load current THD spectrum for phase-a.



(a) (b)

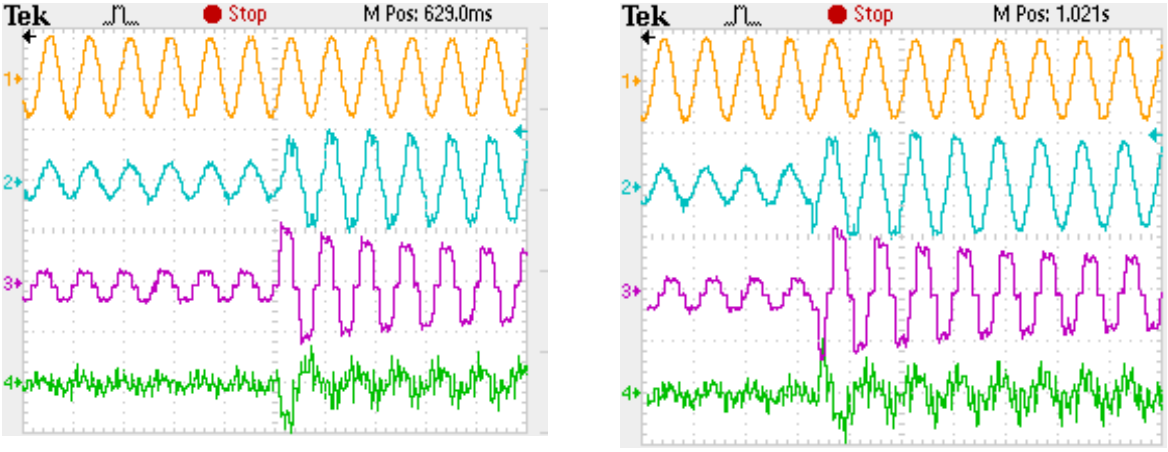


(c) (d)

Fig. 3.17: Experimental results of 3P3W APF for an RL-load on the dc side of a phase-uncontrolled rectifier with PI controller and T2FLC.

3.4.1.1 Transient performance of the active power filter

In Fig. 3.18, the load current rms value has been increased from1.7A to 3.3 A and the corresponding change in the source current are from 1.5A to 2.9A with PI controller and 1.4 to 2.8 A in T2FLC controller respectively. It is also observed that the source current is distorted and takes 3-4 cycles to reach steady state in case of LMS algorithm integrated with PI whereas in case of LMS algorithm integrated with T2FLC, source current takes only 2-3 cycles to reach steady state which ensure the fast transient response of the LMS algorithm integrated with T2FLC controller.



(a) (b)

Fig. 3.18: Experimental results of 3P3W APF for RL-load: (a) LMS integrated with PI controller (b) LMS integrated with T2FLC.

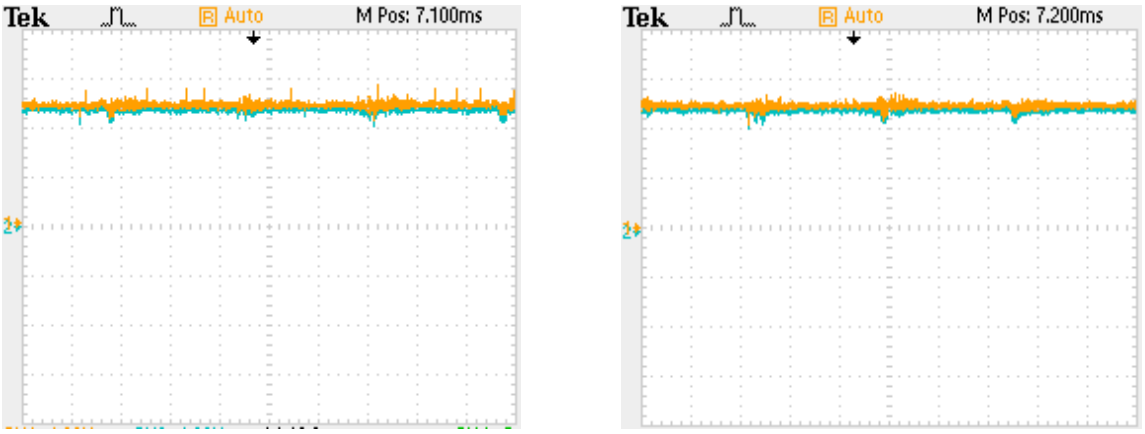
3.4.1.2 DC capacitor voltage regulation

The steady-state performance of active power filter dc side capacitors voltages with PI controller and T2FLC integrated with LMS algorithm are shown in Fig. 3.19. In Fig. 3.19 waveforms show the voltage across each capacitor (v_{c1}, $v_{c2.}$) The scales of these waveforms are: Y-axis: 26 V/div, X-axis: 10 ms/div., the reference level dc side capacitor is set at 90 V.

In Fig. 3.19 (a) that the LMS integrated with PI controller, large ripple content in the dc side capacitor voltages is present. The maximum peak-to-peak ripple in the dc voltages of the capacitors is around 0.6V which affects the performance of the active power filter. But, from Fig. 3.19 (b) it is observed that the maximum peak-to-peak ripple in the dc voltages of the capacitors is 0.5 V in case of LMS algorithm integrated with T2FLC. This ensures the effectiveness of the LMS algorithm integrated with T2FLC. However, in both the cases the capacitors voltage is almost balanced.

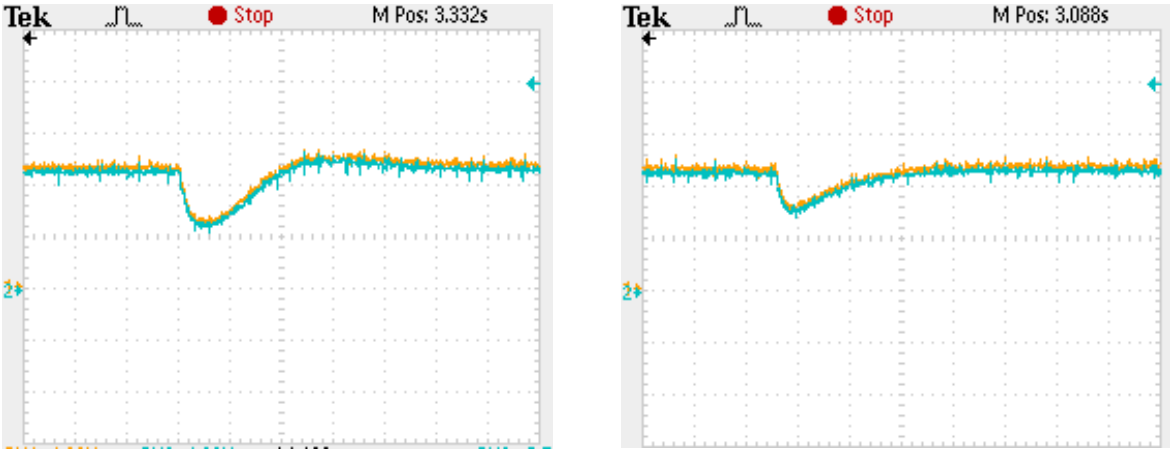
Fig. 3.20 shows the dc capacitor voltages for a LMS algorithm integrated with PI and T2FLC in case of increase in the load current. Fig. 3.20 (a) shows the capacitor voltages vc1 and vc2 (X-axis: 25 ms/div. and Y-axis: 26 V/div.) with PI, whereas Fig. 3.20 (b) shows dc capacitors voltages of active power filter with T2FLC.

At instant, when load current increases, the dc capacitor voltage decreases from its set reference value to compensate the increase in the load current. This decrease in capacitor voltages are achieved steady state in 3-4 cycles with PI controller. However, these capacitor voltages are restored within 2-3 cycles in case of the LMS algorithm integrated with T2FLC, which again demonstrates its superior transient response.



(a) (b)

Fig. 3.19: (a) dc capacitors voltages PI controller (b) dc capacitors voltages with T2FLC.



(a) (b)

Fig. 3.20: (a) DC capacitors voltages PI controller (b) dc capacitors voltages with T2FLC.

3.4.2 Control scheme based on anti-Hebbian algorithm integrated with PI/T2FLC

The six pulse diode rectifier with RL-load on dc side used as nonlinear load in this case. Fig. 3.21 shows the experimental results of active power filter using anti-Hebbian algorithm integrated with PI and T2FLC controller. The source voltage, source current after compensation, load current and compensating currents for phase-a with PI and T2FLC are shown in Fig. 3.21 (a) and Fig. 3.21 (b) respectively. The THD spectra of source currents after compensation with PI and T2FLC are shown in Fig. 3.21 (c) and Fig. 3.21 (d) respectively. As seen in Fig. 3.21, after compensation with active power filter, the source

current %THD has been reduced from 24.7% to 3.9% with PI and 3.5% with T2FLC respectively. The anti-Hebbian algorithm based control scheme with the both controllers, after compensation, the source current waveform is observed to be in phase with the source voltage waveform. This ensures the effectiveness of the anti-Hebbian algorithm based control scheme for compensating harmonics and reactive power requirement of the nonlinear load.

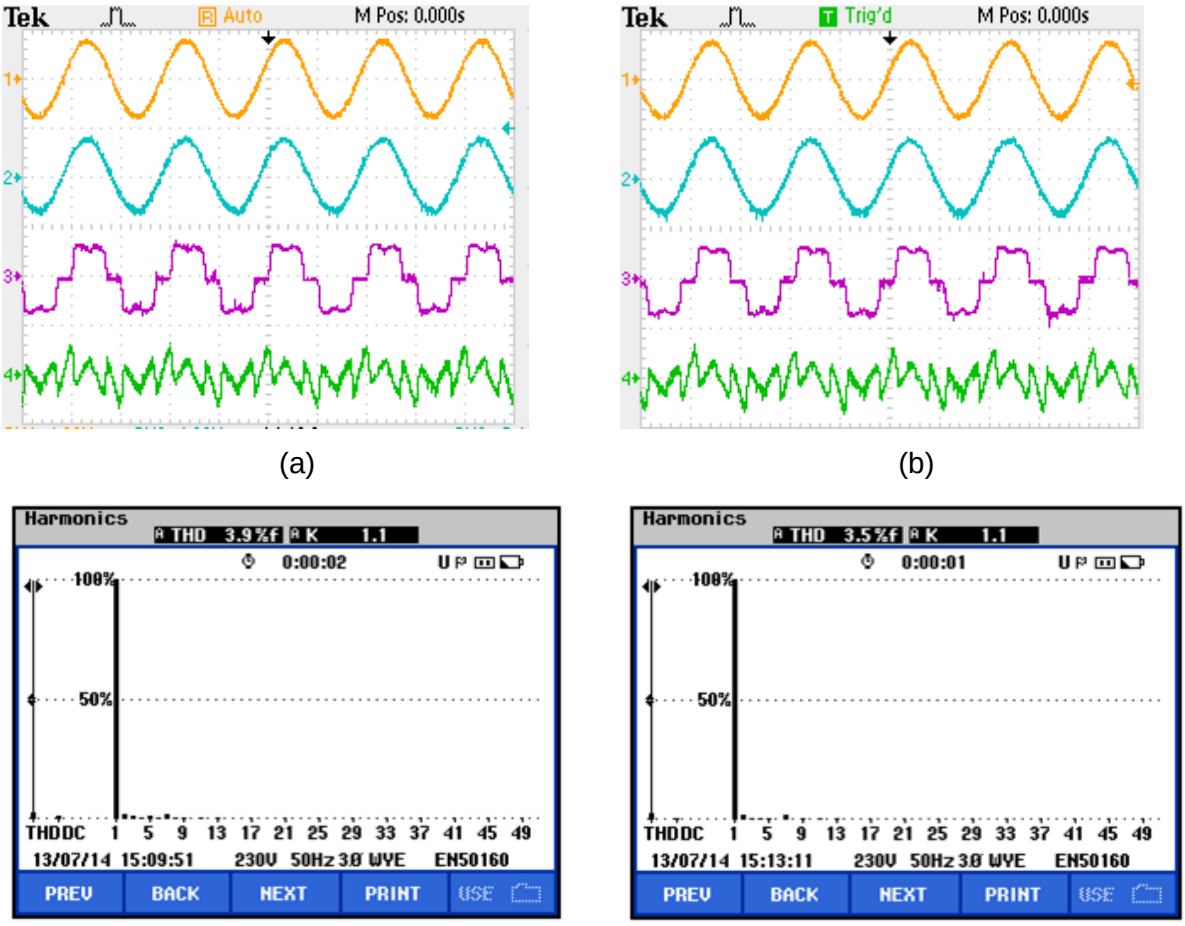
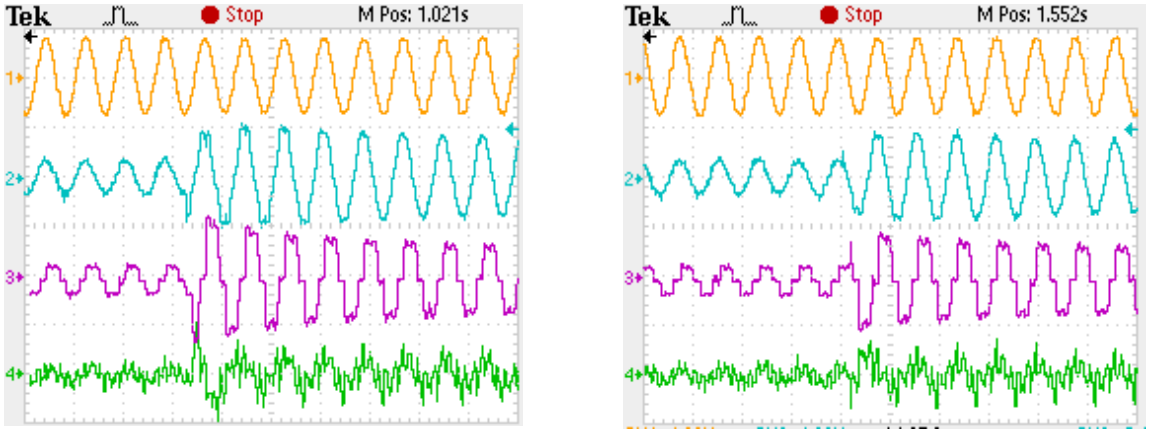


Fig. 3.21: Experimental results of 3P3W APF for an RL-load on the dc side of a phase-uncontrolled rectifier with PI controller and T2FLC.

3.4.2.1 Transient performance of the active power filter

As seen in Fig. 3.22, the load current rms value has been increased from1.7A to 3.3 A and the corresponding change in the source current are from 1.5A to 2.9A with PI controller and 1.4 to 2.8 A in T2FLC controller respectively. It is also observed that the source current is distorted and takes 3-4 cycles to reach steady state in case of anti-Hebbian algorithm based control scheme integrated with PI whereas in case of anti-Hebbian algorithm integrated with T2FLC, source current is distortion free and takes only 2-3 cycles to reach steady state which ensure the fast transient response of the anti-Hebbian algorithm based control scheme integrated with T2FLC controller.



(a) (b)

Fig. 3.22: Experimental results of 3P3W APF for RL-load: (a) anti-Hebbian integrated with PI controller (b) anti-Hebbian integrated with T2FLC.

3.4.2.2 DC voltage regulation

The steady-state performance of active power filter dc side capacitors voltages with PI controller and T2FLC integrated with anti-Hebbian algorithm are shown in Fig. 3.23. In Fig. 3.23 waveforms show the voltage across each capacitor (v_{c1}, $v_{c2.}$) The scales of these waveforms are: Y-axis: 26 V/div, X-axis: 10ms/div., the reference value of dc side capacitors voltage is set at 90 V.

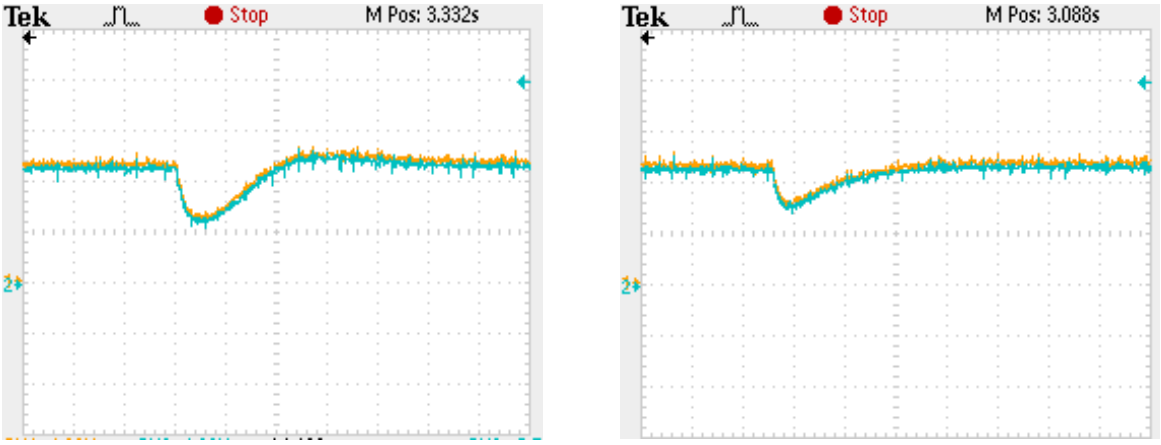
As seen in Fig. 3.23 (a) that the anti-Hebbian algorithm integrated with PI controller, large ripple content in the dc side capacitor voltages is present. The maximum peak-to-peak ripple in the dc voltages of the capacitors is around 0.53 V which affects the performance of the active power filter. But, from Fig. 3.23 (b) it is observed that the maximum peak-to-peak ripple in the dc voltages of the capacitors is 0.43V in case of anti-Hebbian algorithm integrated with T2FLC. This shows the effectiveness of the anti-Hebbian algorithm integrated with T2FLC. But, with both the controllers capacitors voltage is almost balanced.

Fig. 3.24 shows the dc capacitor voltages for anti-Hebbian algorithm integrated with PI and T2FLC in case of increase in the load current. Fig. 3.24 (a) shows the capacitor voltages vc1 and va2 (X-axis: 25 ms/div. and Y-axis: 26 V/div.) with PI, whereas Fig. 3.24 (b) shows dc capacitors voltages of active power filter with T2FLC.

At instant, when load current increases, the dc capacitor voltage decreases from its set reference value to compensate the increase in the load current. This decrease in capacitor voltages are achieved steady state in 2-3 cycles with PI. However, these capacitor voltages are restored within 1-2 cycles in case of the anti-Hebbian algorithm integrated with T2FLC, which again demonstrates its superior transient response.

(a) (b)

Fig. 3.23: (a) dc capacitors voltages PI controller (b) dc capacitors voltages with T2FLC.



(a) (b)

Fig. 3.24: (a) dc capacitors voltages PI controller (b) dc capacitors voltages with T2FLC.

3.4.2.3 Anti-Hebbian algorithm based on total least square (TLS) integrated with PI/T2FLC

Initially, an uncontrolled rectifier with *RL*-load on its dc side has been considered as a nonlinear load and connected to source. The source current waveform and THD spectrum before compensation is presented section 3.3.2 .Fig. 3.25 shows the experimental results of active power filter using anti-Hebbian algorithm based on TLS based control scheme integrated with PI and T2FLC. The steady state source voltage, source current after compensation, load current and compensating currents for phase-*a* with PI and T2FLC are shown in Fig. 3.25 (a) and Fig. 3.25 (b) respectively. The THD spectra of source currents after compensation with PI and T2FLC are shown in Fig. 3.25 (c) and Fig. 3.25 (d) respectively.

The experimental results are in good agreement with simulation results and fromFig. 3.25, it can be observed that after compensation with active power filter, the source current %THD has been improved from 24.7% to 3.3% with PI and 3.3% with T2FLC. The THDs of source current close to the recommended standard of IEEE-519. The steady state response

of the anti-Hebbian algorithm based control scheme integrated with T2FLC is comparable with PI controller. In both cases, the source power factor is almost unity.

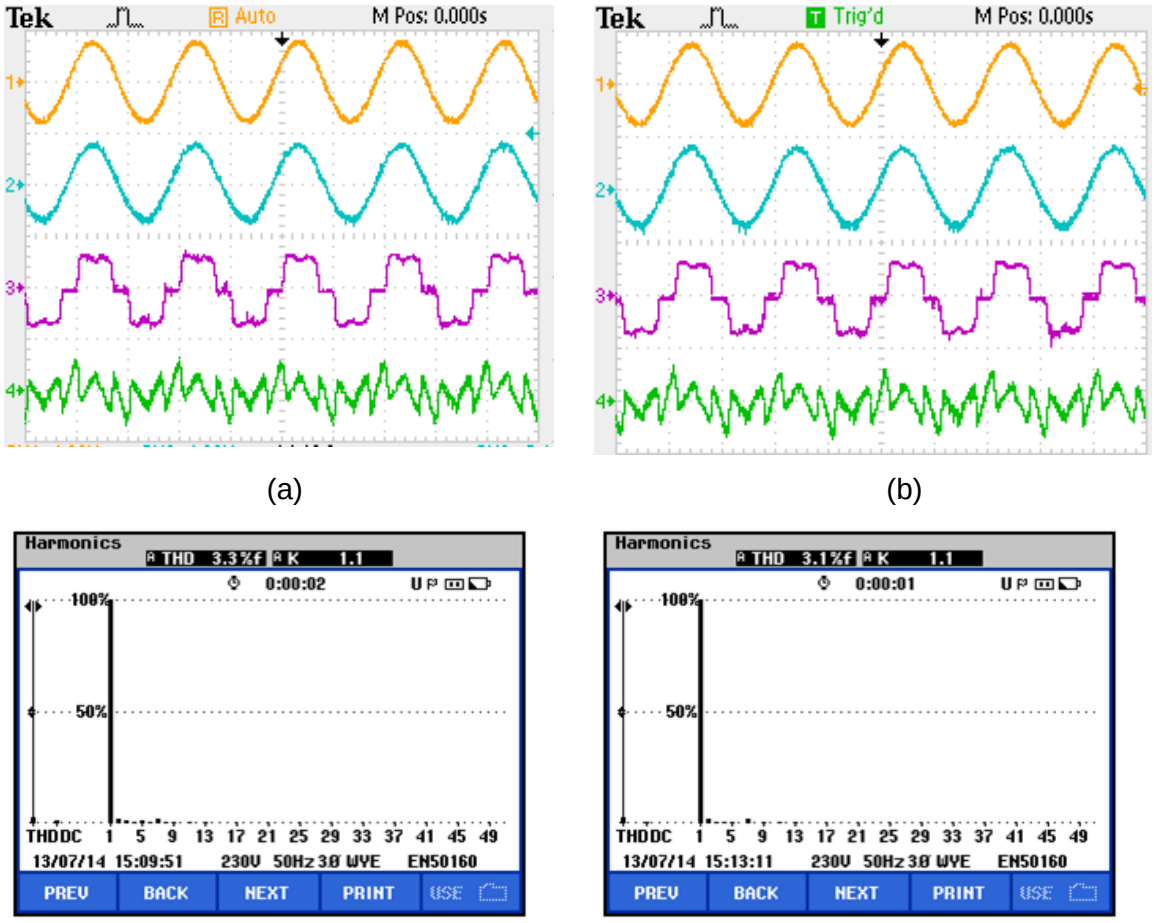
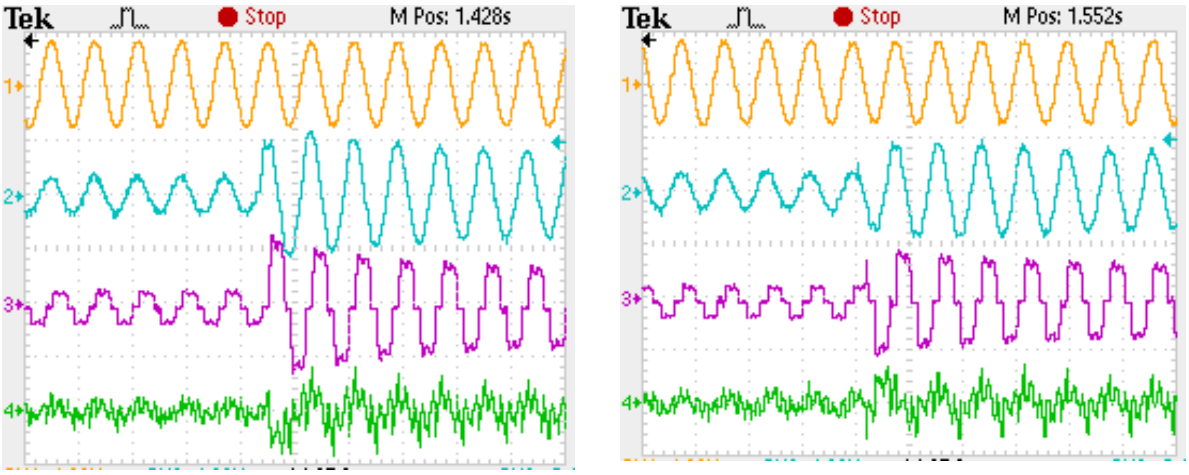


Fig. 3.25: Experimental results of 3P3W APF for an RL-load on the dc side of a phase-uncontrolled rectifier with PI controller and T2FLC.

3.4.2.4 Transient performance of the active power filter

The load perturbation response of active power filter is investigated by sudden increase in load and as shown in Fig. 3.26. Fig. 3.26 (a) shows the load current perturbation response during sudden change in load current with anti-Hebbian based on TLS algorithm based control scheme integrated with PI controller. The load current is increased from 1.6 A to 2.5 A. The corresponding change in the source current and compensating current is observed. The anti-Hebbian based on TLS integrated with PI controller is shown in Fig. 3.26 (b). It is found that the transient response of source current is smooth and fast in case of T2FLC than the PI controller. Also steady state is reached almost taking 2-3 cycles in case of PI controller whereas in case T2FLC source current achieved steady state within 1-2 cycles.



(a) (b)

Fig. 3.26: Experimental results of 3P3W APF for RL-load: (a) anti-Hebbian based on TLS algorithm integrated with PI controller (b) anti-Hebbian integrated based on TLS with T2FLC

3.4.2.5 DC voltage regulation

The steady-state performance of active power filter dc side capacitors voltages with PI controller and T2FLC integrated with anti-Hebbian based on TLS algorithm are shown in Fig. 3.27. In Fig. 3.27 show the voltage across each capacitor (v_{c1}, v_{c2}.) The scales of these waveforms are: Y-axis: 26 V/div, X-axis: 10ms/div., It is to be noted that the dc voltage reference level of capacitor is set at 90 V.

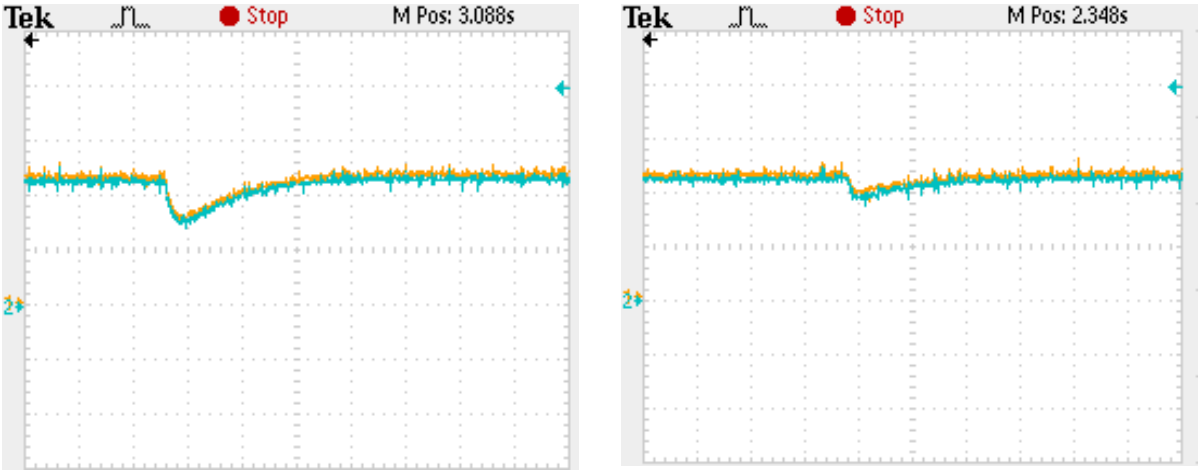
In Fig. 3.27 (a) that the anti-Hebbian based on TLS integrated with PI controller, large ripple content in the dc side capacitor voltages is present. The maximum peak-to-peak ripple in the dc voltages of the capacitors is around 0.5V which affects the performance of the active power filter. But, from Fig. 3.27 (b) it is observed that the maximum peak-to-peak ripple in the dc voltages of the capacitors is 0.3 V in case of anti-Hebbian based on TLS algorithm integrated with T2FLC. This ensures the effectiveness of the anti-Hebbian based on TLS algorithm integrated with T2FLC. But, with both controller capacitors voltage is almost balanced.

Fig. 3.28 shows the dc capacitor voltages for anti-Hebbian based on TLS algorithm integrated with PI and T2FLC in case of increase in the load current Fig. 3.28 (a) shows the capacitor voltages v_{c1} and v_{c2} (X-axis: 25 ms/div. and Y-axis: 26 V/div.) with PI, while Fig. 3.28 (b) shows dc capacitors voltages of active power filter with T2FLC.

At instant, when load current increases, the dc capacitors voltages decrease from its set reference value to release the energy for compensating the increase in the load current. This decrease in capacitor voltages are achieved steady state in 2-3 cycles with PI. However, these capacitor voltages are restored within 1-2 cycles in case of the anti-Hebbian based on TLS algorithm integrated with T2FLC, which again demonstrates its superior transient response.

(a) (b)

Fig. 3.27: a) dc capacitors voltages PI controller (b) dc capacitors voltages with T2FLC



(c) (d)

Fig. 3.28: c) dc capacitors voltages PI controller (d) dc capacitors voltages with T2FLC.

3.5 Comparison of control strategies integrated with PI/T2FLC

As the simulation studies presented in section 3.3.4, the 3P3W DCMLI based three level active power simulation is carried out at 400 V. But, due to the constraints involved in the development of prototype, the experimentations have been carried out at a reduced line voltage of 100V. As the experimentations have been conducted at downscaled system parameters, for validating the experimental results, the simulation is also carried out with downscaled system parameters. The parameters used in the actual simulation and downscaled simulations are given in Table 3.2. The downscaled simulation parameters are maintained as that of the experimental parameters given in Table 3.2.

The simulation results with an uncontrolled rectifier with a *RL* load on dc side has been considered as a nonlinear load and the simulated response are shown in Fig. 3.29 and Fig. 3.30 with anti-Hebbian based on TLS algorithm integrated with PI and T2FLC respectively.

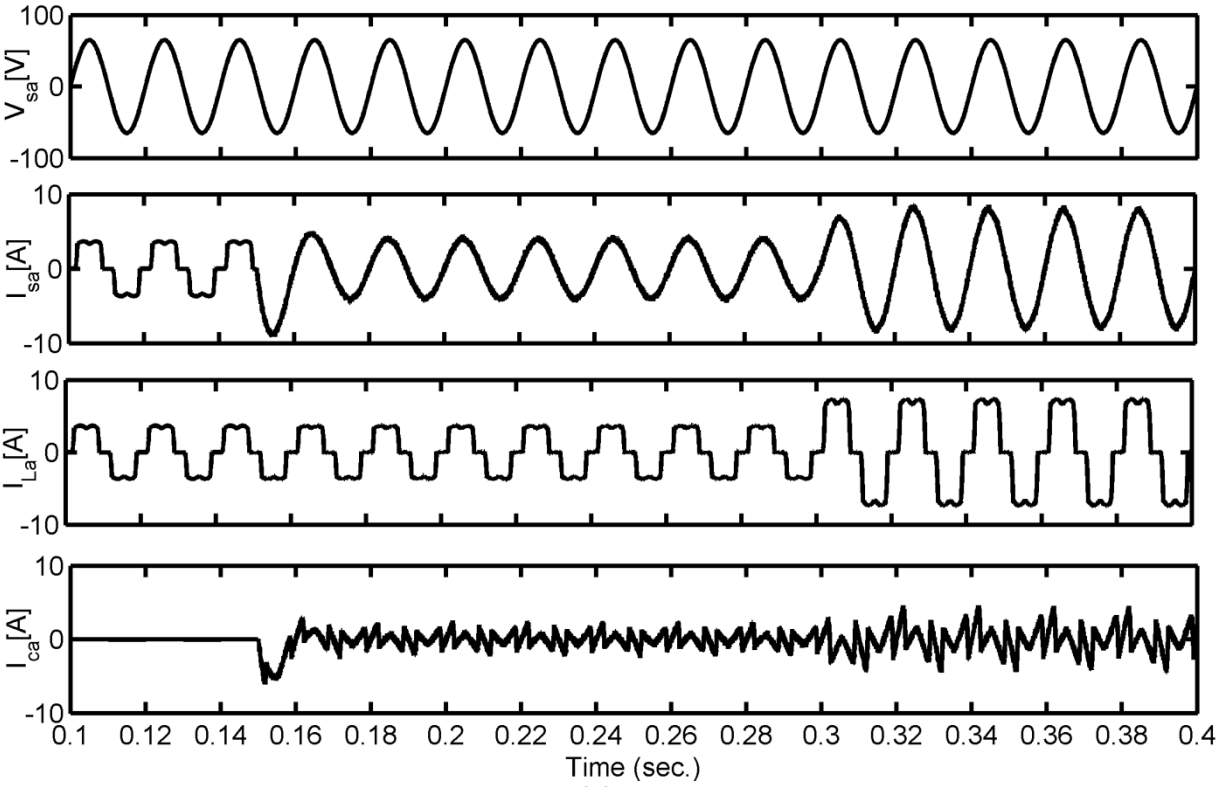
Fig. 3.29 (a)-(d) shows the simulated waveforms, dc side capacitors voltages (v_{c1} and v_{c2}), harmonic spectra of load and source currents respectively using anti-Hebbian based on TLS integrated with PI, whereas Fig. 3.30 (a)-(d) shows these results for T2FLC with anti-Hebbian algorithm based on TLS. In Fig. 3.29 (a) and Fig. 3.30 (a), the quantities shown are as follows (from top to bottom): trace 1: phase–*a* source voltage (v_{Sa}), trace 2: phase–*a* source current (i_{Sa}), trace 3: phase–*a* load current (i_{La}) and trace 4: phase–*a* current injected by APF (i_{Ca}). As can be seen from both these figures, the simulation results are almost with identical experimental results for both controllers.

Table 3.2: The parameters used in the simulation studies.

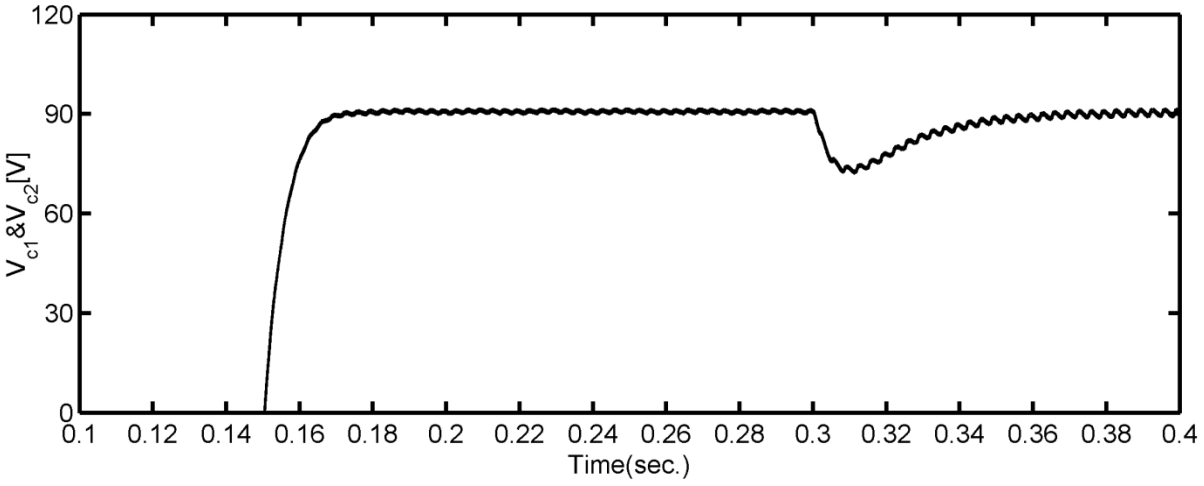
Parameters	**For the actual APF**	**For the downscaled APF**
AC line parameters	Three-phase, three-wire, 400V, 50 Hz	Three-phase, three-wire, 100 V, 50 Hz
DC bus voltage of APF	500 V (for each capacitor)	90 V (for each capacitor)
DC bus capacitance of APF	588μF (for each capacitor)	1800 μF (for each capacitor)
APF interfacing inductor	L_c = 5.7 mH	L_c = 2.4 mH
Commutation inductance	L_f = 2 mH	L_f = 1 mH
PWM switching frequency	1 kHz	1 kHz
PI controller parameters	K_p = 1.4, K_i = 0.9	K_p = 0.8, K_i = 1.9
Load	Three-phase uncontrolled rectifier with *RL* load;	Three-phase uncontrolled rectifier with *RL* load;
Sampling time	T_s = 10 μs.	T_s = 50 μs.

The source current THDs are less than 5% with both controllers, and these values are almost same as that of their equivalent experimental values. Even though sampling time of the experimental study is larger than the sampling time of simulation study. This is due to the fact that, for implementation of control algorithm in dSPACE platform requires a minimum sampling time for execution of program.

The comparison of experimental and simulation results with anti-Hebbian based on TLS algorithm given in Table 3.3 and Table 3.4 for PI and T2FLC controllers respectively.



(a)



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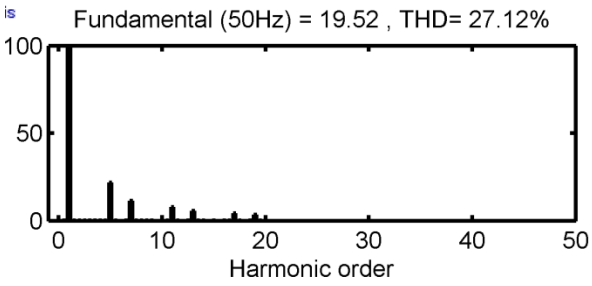

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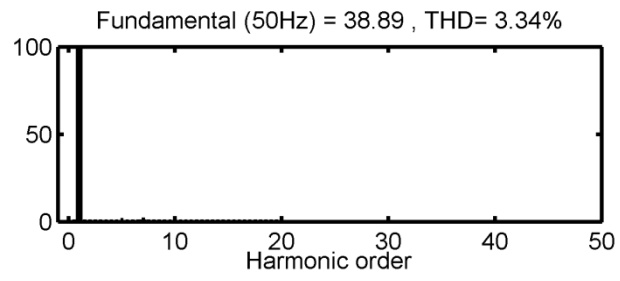
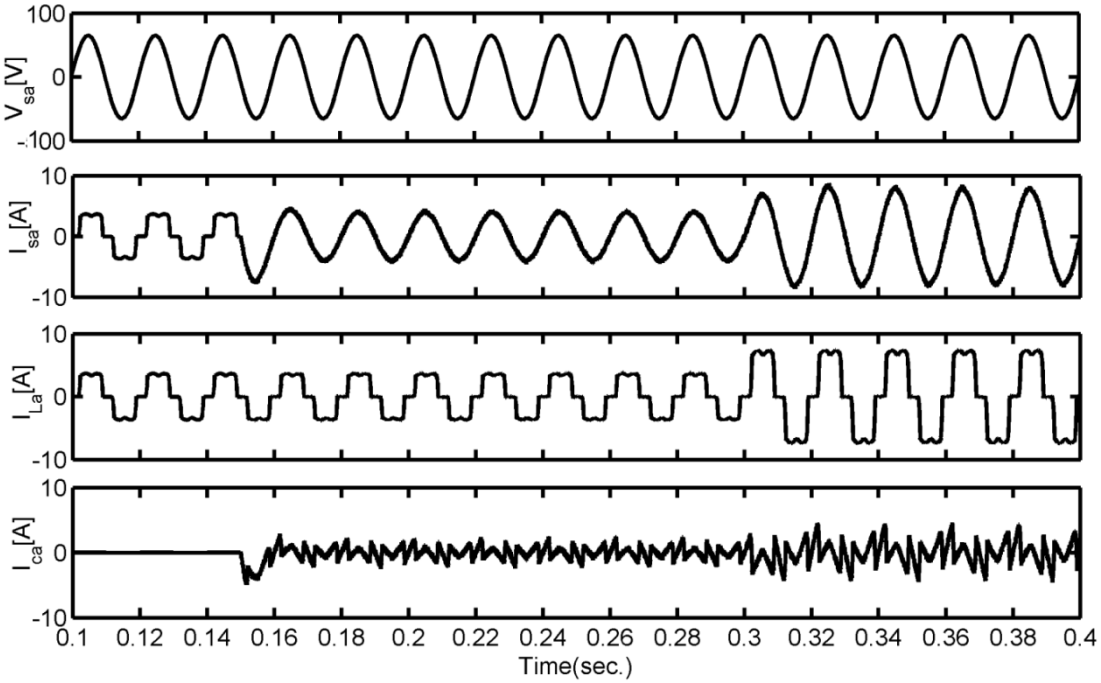
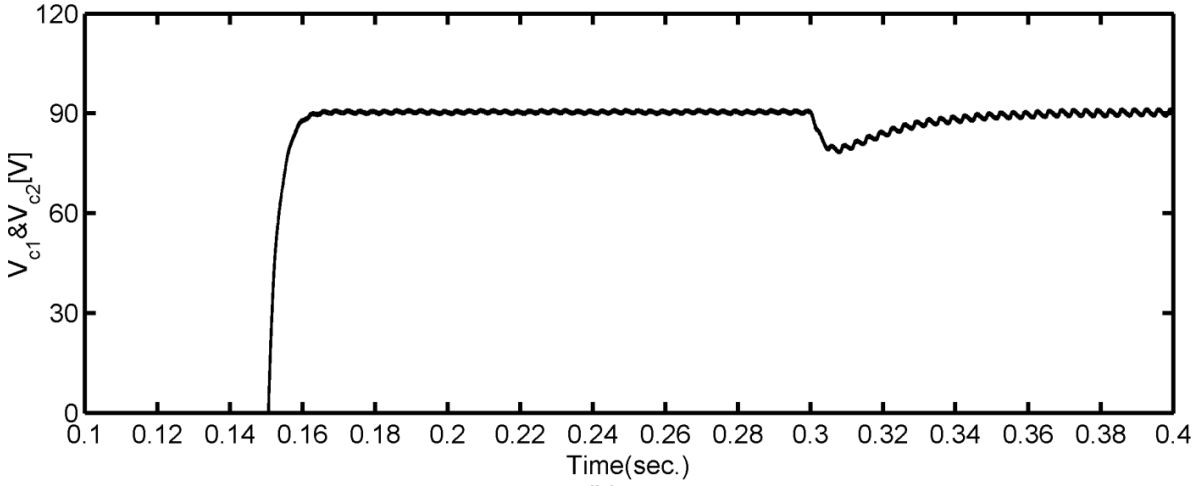


(d)

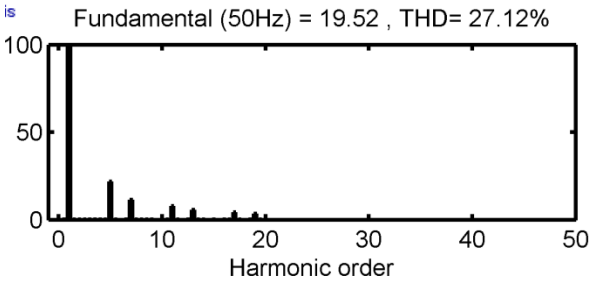
Fig. 3.29: Performance of APF with scaled down simulation studies for *RL* load on dc side of uncontrolled rectifier with anti-Hebbian based on TLS integrated with T2FLC.



(a)



(b)



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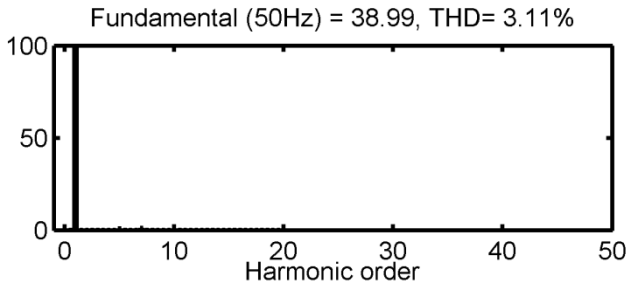


(d)

Fig. 3.30: Performance of APF with scaled down simulation for *RL* load on dc side of uncontrolled rectifier with T2FLC.

The comparison of experimental and simulation results with LMS and anti-Hebbian algorithm integrated with different controllers such as PI and T2FLC using uncontrolled rectifier as non-linear load is given in Table 3.4 and

Table 3.5 respectively.

Table 3.3: Comparison of experimental and simulation results with anti-Hebbian based on TLS algorithm with different controllers.

Parameter	**PI controller**		**T2FLC controller**	
	Exp.	**Simulation**	**Exp.**	**Simulation**
Load current (A, rms)	3.3	3.43	3.1	3.09
% THD of load current	24.7	27.12	24.7	27.12
Source current (A, rms)	3.5	3.61	3.4	3.51
% THD of source current	3.3	3.31	3.1	3.11
Maximum peak-to-peak ripple in dc voltages (V)	0.4	0.4	0.3	0.3
% fall in dc voltage during load changes (% V_{dcref})	8.8	8.72	5.5	5.42

Table 3.4: Comparison of experimental and simulation results with LMS algorithm with different controllers.

Parameter	**PI controller**		**T2FLC controller**	
	Exp.	**Simulation**	**Exp.**	**Simulation**
Load current (A, rms)	3.3	3.43	3.1	3.09
%THD of load current	24.7	27.12	24.9	27.12
Source current (A, rms)	3.6	3.58	3.3	3.55
%THD of source current	4.9	4.53	3.9	4.12
Maximum peak-to-peak ripple in dc voltages	0.6	0.59	0.5	0.52
% fall in dc voltage during load changes (% V_{dcref})	9.92	9.93	6.52	6.61

Table 3.5: Comparison of experimental and simulation results with anti-Hebbian algorithm with different controllers.

Parameter	PI controller		T2FLC controller	
	Exp.	Simulation	Exp.	Simulation
Load current (A, rms)	3.3	3.31	3.2	3.16
% THD of load current	24.7	24.39	24.7	24.78
Source current (A, rms)	3.3	3.58	3.5	3.42
% THD of source current	3.9	4.94	3.5	5.09
Maximum peak-to-peak ripple in dc voltages	0.53	0.49	0.42	0.39
% fall in dc voltage during load changes (% V_{dcref})	8.94	8.95	5.95	5.95

As can be seen from these tables downscaled simulation results are almost identical with the experimental results. However, overall results prove that the control schemes integrated with PI and T2FLC works effectively for compensating harmonics and reactive power induced due the nonlinear load. But, the anti-Hebbian based on TLS algorithm integrated with T2FLC gives improved performance characteristics of active power filter.

3.6 Conclusion

In this chapter, the simulation and experimental study of the DCMLI three level active power filter has been carried out with different adaptive neural network based control schemes. The adaptive neural network based approaches calculate the weights and these calculations perform online. These adaptive control schemes can extract the reference current under varying load condition and it is not possible with other control schemes. The control schemes based on LMS, anti-Hebbian algorithm and TLS with PI/T2FLC have demonstrated satisfactory behaviour of the active power filter. An adaptive control scheme using anti-Hebbian based on the TLS integrated with PI/T2FLC has resulted considerable improvement of compensation characteristics of the active power filter. The simulation and experimental response shows the effectiveness of the control schemes.

CHAPTER 4: ADAPTIVE CONTROL OF FIVE LEVEL CHBMLI BASED ACTIVE POWER FILTER

The performance of the fuzzy logic control depends on its rule inference. In most of the cases to increase the accuracy of the fuzzy logic controller, more number of rules is employed. The large set of fuzzy rule requires more computational time. As a result, it may not be useful for real time implementation with small sampling time. However, such problem can be dealt with artificial intelligent techniques. This chapter proposes a simplified control approach to design fuzzy logic controller for cascaded H-bridge multilevel inverter (CHBMLI) based active power filter. The proposed control scheme used is a single input fuzzy logic controller (SIFLC). The SIFLC reduces the conventional two input fuzzy logic controller (CFLC) to single input fuzzy logic controller. The SIFLC also offer significant reduction in the rule inference and simplifies the tuning of control parameters. The anti-Hebbian based on TLS algorithm integrated with SIFLC controller is used for reference current generation. The simulated performance characteristics of active power filter with PI and single input fuzzy logic controller are compared using MATLAB/ Simulink. The performance characteristics indicate that the SIFLC require less tuning efforts and execution time as compared to conventional FLC. In order to validate the simulated response of SIFLC a prototype of model of the cascaded H-bridge based active power filter has been developed and the dSPACE 1104 is used to generate the firing pulse for prototype. The performance characteristics of the CHBMLI based active power filter are recorded for nonlinear load under different load conditions. The experimental waveforms are found to be in agreement with simulated response.

4.1 Introduction

In previous chapter, the DCMLI based three level active power filter has been discussed with different adaptive control schemes integrated with PI/T2FLC controller. The adaptive control schemes used are LMS algorithm, anti-Hebbian algorithm and anti-Hebbian based on TLS. These adaptive control schemes perform calculation online. Among these adaptive control schemes anti-Hebbian based on TLS algorithm integrated with T2FLC controller gives improved compensation of harmonics and reactive power requirement of the nonlinear load. However, the T2FLC is very complex to implement with higher level inverter due to the association of length process such as fuzzification, rule base, inference and defuzzification. For better accuracy in control, a larger set of rules is required, which results in longer computational time. The DCMLI topology seems to be the best suited for active power filter applications. But, the large number of power components and voltage unbalance problem at higher levels limits the DCMLI for three level and low-power rating applications.

Recently, the multilevel converters are most commonly used in harmonics elimination and reactive power compensation in medium and high power application [72, 88, 101, 103, 106, 107,113]. The multilevel converter, use the concept of addition of multiple small-voltage levels for achieving the required voltage level with the help of additional switching devices and few components like diodes or capacitors. This approach does not require phase shifting transformers and hence these topologies are best suited for medium and high power applications. The bench mark topologies of multilevel inverters are (I) Diode clamped multilevel inverter (DCMLI), (II) Flying capacitor multilevel inverter (FCMLI) and (II) cascaded H-bridge multilevel inverter (CHBMLI). The selection of individual inverter topologies for active power filter applications depends on their performance, cost, size and implementation issues. The DCMLI topology appears to be the best suited for active power filter applications. But, the large number of power components and voltage unbalance problem at higher levels limits the DCMLI for low-power rating applications [89]. On the other hand, FCMLI has a natural voltage balancing operation and modular structure, but its application as an active power filter is limited due to the requirement of a large number of capacitors and their pre-charging circuit. In contrast, CHBMLI is one of the next generation multilevel inverters intended for high or medium-voltage power conversion without the requirement of line-frequency transformers. The CHBMLI is based on cascade connection of multiple single-phase H-bridge converter cells or chopper cells per leg. The least component requirement, low cost, modular structure, easy expansion to any number of levels, high fault tolerance and absence of input transformer and non-initialization of the capacitor voltages make CHBMLI best suited for active power filter applications [63, 65-68]. The CHBMLI based active power filter is shown in Fig. 4.1.

The performance of the active power filter depends on its controller and therefore, controller is the main part of the active power filter for it operation. Various controllers are available in the literature such as PI, sliding mode, predictive, unified constant frequency controller and are in use [112]. However, the conventional controllers require precise mathematical modelling and fail to perform under parameter variation, nonlinearity and load disturbance etc.

In recent years, use of fuzzy logic controller have generated considerable interest in various application and have been introduced in the field of power electronics [112, 114, 191, 192, 194,195, 197]. The principle advantages of a fuzzy logic controller are that it does not require precise mathematical modeling and is able to handle imprecise input, nonlinearity and robustness. The fuzzy logic controller involves fuzzification, rule base storage, inference mechanism and defuzzification operation etc. In most of the cases, for better accuracy and control, large set of rules are required. However, large set of fuzzy rule requires more computational time. As a result, it may not be useful for real time implementation with small

sampling time. Despite of these issues, it is known that fuzzy logic controller requires simpler mathematics and offers a higher degree of freedom in tuning its control parameters compared to other nonlinear controllers. To take full advantage of the fuzzy logic controller, the computational time associated with it must be reduced. In this chapter a simple fuzzy logic controller is developed from the conventional fuzzy logic controller to regulate the dc side capacitor of the CHBMLI based active power filter. The method is known as single input fuzzy logic controller. The simplification convert conventional two input fuzzy logic controller to single input using signed distance. This simplification is accomplished by applying signed distance method, which was demonstrated in [109, 110]. The input to the single input fuzzy logic controller is only one variable known as signed distance whereas conventional fuzzy logic controller requires two variables known as error and change of error of its input. The reduction in number of input from two to one, the rule table also reduced to one dimensional. Therefore, single input fuzzy logic controller reduces the computational burden of the processor due to the reduction of fuzzy rules from p^2 to p, where p represents the level fuzzification. In this method, the control surface of the single input fuzzy logic controller can be approximated to piece wise linear (PWL) function which results in significant reduction of tuning process.

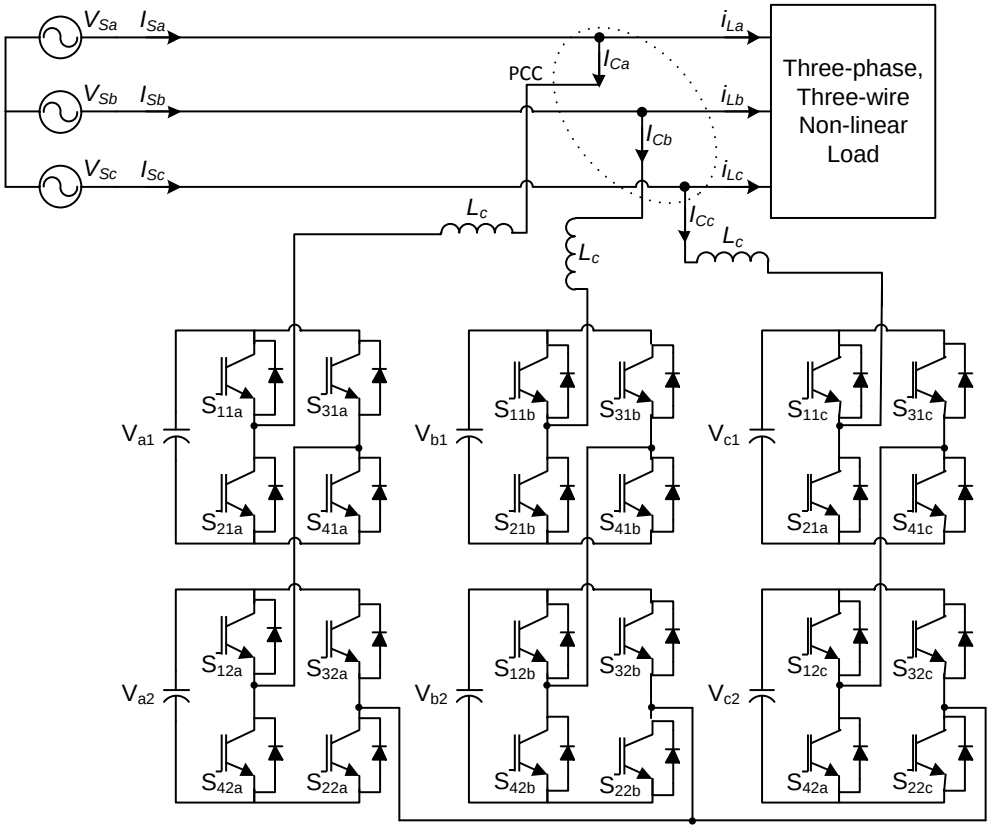


Fig. 4.1: Five level CHBMLI based active power filter.

To verify the effectiveness of the proposed controller, Matlab computer simulation of CHB MLI based active power filter has been carried for individually balancing the dc side

capacitor of the active power filter. The simulated response show that proposed active power filter provides sinusoidal current with low harmonics distortion.

4.2 Design of passive component of active power filter

4.2.1 Design of capacitor

The main objective of an APF is to compensate total reactive and harmonic components of load that causes the dc-bus capacitor voltage fluctuation. To get a proper compensation performance, this voltage fluctuation must be avoided. It is also desirable that the APF should have at least twice the boost in the dc-bus voltage with respect to the amplitude of the ac phase voltage at the PCC. This is an important condition to avoid the violation of current distortion and current control limits [28, 29]

Therefore, the energy storage capability of the dc-bus of APF should be sufficient to sustain disturbances arising during load perturbation. On load perturbation, a desired increase or decrease in amplitude of the reference supply current may not be instantaneously available to the current controller, thereby, necessitating an energy exchange between the APF and the load. In practice, the APF system should have energy storage and exchange capabilities as it ensures local energy management without disturbing the supply system during transient conditions of the load. This can be achieved by proper sizing of the dc-bus capacitor. The energy W required to charge the dc-bus capacitor from actual voltage V_{dc} to the reference voltage V_{dcref} can be expressed as [55]:

$$W = \frac{1}{2} C \left(V_{dcref}^2 - V_{dc}^2 \right) \tag{4.1}$$

From the principles of energy transformation equation can be written as [52]:

$$\frac{1}{2} C_{dc} \left(V_{dcref}^2 - V_{dc}^2 \right) = 3V(aI)t \tag{4.2}$$

$$C_{dc} = 2 \frac{3V(aI)t}{\left(V_{dcref}^2 - V_{dc}^2 \right)} \tag{4.3}$$

In equation,

C_{dc} = Capacitance of the capacitor of each H-bridge cell (in farads),

V_{dc} = Minimum voltage level of the dc bus voltage of H-bridge cell,

V = AC voltage of the each H-bridge cell (in rms) $= V_S \Big/ \left(N\sqrt{3} \right)$,

I = Rated phase current of the APF,

t = Response time of the APF,

a = Over loading factor.

N= Number of H-bridge cells

Considering V_{dc} = 8000 V (considering 5% ripple in dc capacitor voltages), $V = \frac{11\times10^3}{2\times\sqrt{3}}$ V = 3175 V, $I = \frac{1\times10^6}{\sqrt{3}\times11\times10^3}$ A = 52.49 A, t = 300 μs, and a = 1.2, the calculated value of C_{dc} is 58μF.

4.2.2 Interfacing inductor

The performance of the active power filter also depends on the interfacing inductor. The pulse width modulated APF introduces undesirable current harmonics around the switching frequency and its multiples. If the switching frequency of the PWM active power filter is sufficiently high, these undesirable current harmonics can be easily filtered out by the interfacing inductor (L_c). The connection of the interfacing inductor to the point of common coupling is shown in Fig. 4.1.

The selection of the ac inductance depends on the current ripple $i_{cr,(p-p)}$ and switching frequency of the converter (f_c). The approximate value of the ac inductance is given as [55]:

$$L_C = \frac{\sqrt{3}m_a V_c}{12af_c i_{cr,(p-p)}} \tag{4.4}$$

Here, switching frequency of the converter (f_c) depends on the PWM method used for controlling the converter. The level-shifted PWM technique with carrier signal frequency f_{cr}, f_c can be calculated as:

$$f_c = 2Nf_{cr} \tag{4.5}$$

Table 4.1: Parameters used in the simulation study

Parameter	**Value**
AC line voltage	Three-phase, three-wire, 11 kV, 50 Hz
Source impedance	R_s = 0.5 Ω, L_s = 0.5 mH
DC bus reference voltage	8000 V (for each capacitor in the H-bridge cell)
DC side capacitance	58 μF (for each capacitor in the H-bridge cell)
Interfacing inductance	L_{ac} =95mH
PWM switching frequency	2 kHz
PI controller parameters	K_p = .385, K_i = 1.4
Load	Three-phase uncontrolled rectifier, R_{dc} = 40 Ω, L_{dc} = 16 mH,

Considering 5% peak-to-peak current ripple $\left(i_{cr,(p-p)}\right)$ to be 2.52 A rms, the switching frequency of the converter ($2Nf_{cr}$) = $2\times2\times2$ kHz = 8kHz, amplitude modulation index (m_a) =

1, phase-to-neutral of the inverter (V_c) =3175V and overload factor (a) = 1.2, the value is calculated to be 95.45 mH.

On one hand, for a better harmonic elimination and reactive power compensation a higher value of inductance is generally used. But, a very high value of inductance will result in slow transient response of the active power filter and it would result spikes in source current. Therefore, a compromise solution has to be made. To further optimize the value of the interfacing inductor, system performance has been investigated around the calculated value of the interfacing inductor for the system parameters given in Table. The optimized value of the interfacing inductor is given in Table 4.1.

Table 4.2 shows the compensation performance of APF for the selected values of interfacing inductor. It is observed that the APF performance can be significantly improved by reducing the filter inductor to an optimum value. In this work, the value of the interfacing inductor is selected as 19 mH. At this value of interfacing inductor, APF output current THD is minimum and the system transient performance is satisfactory.

Table 4.2: Interfacing inductor

Interfacing inductance L_f (mH)	Settling time (Cycles)	%THD of source current after compensation	Source power factor after compensation
13	1	4.14%	0.992
15	< 2	3.25%	0.994
17	< 2	1.69%	0.999
19	< 3	1.62%	0.999
21	3	1.01%	0.993
23	< 4	2.43%	0.990
25	4	3.92%	0.976

4.3 Single input fuzzy logic controller

In most of the cases, input to the fuzzy logic controller is error (e) and rate of change of error ($e^{\bullet}$). The rules table of fuzzy logic controller can be created on a 2-D space of phase plane as shown Table 4.3 using error and change of error. This is known as the Teoplitz structure. This structure has the same output membership in a diagonal direction, which is the main property of the Teoplitz structure. In addition to that, each point on the particular diagonal line has a magnitude that is proportional to the distance from its main diagonal line [16]. The fuzzy logic controller which uses error and rate of change of error as the input variable follows the Teoplitz structure.

The rule table of the conventional fuzzy logic controller is shown in Table 4.3. It can be seen from the Table 4.3, the output membership follows consistent pattern and therefore, it is

possible to simplify the rule table. It is possible to obtain the corresponding output, using only a single variable input known as signed distance. The significance of the reduction was first demonstrated in [16] and is known as the signed distance method. The signed distance method reduces the number input into single input variable known as distance. Let us consider the n[th] order nonlinear/linear system, represented by the state equation as follows

$$\dot{x} = g(w, t) + b(w, t)u(t) + d(t) \tag{4.6}$$

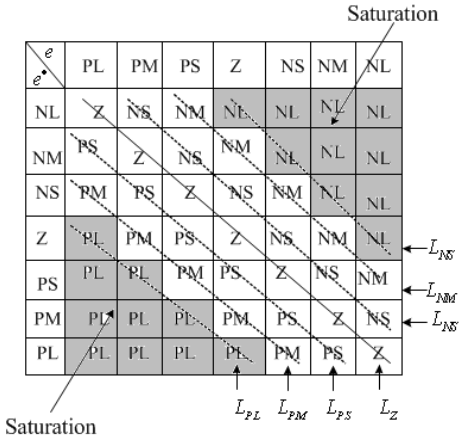
$$y = w \tag{4.7}$$

With $w = [w_1, w_2, ..., w_n]^T = [w, w, ..., w^{(n-1)}]^T$) where $g(w,t)$ and $b(w,t)$, where $w(t) \in \Re^n$ representing the state vectors of the process $u(t) \in \Re$ and $y(t) \in \Re$ are respectively, represent the input and output of the control system; $g(w)$ and $b(w)$ are the nonlinear functions representing the dynamics of the system; $d(t)$ is the unknown external disturbance. The control problem is to force $y(t)$ to track a given bounded reference input signal $w_d(t)$. So the tracking error vector is as follow

$$e(t) = w(t) - w_d(t) = \left[e(t), e^{\bullet}(t), ..., e^{(n-1)}(t) \right]^T \tag{4.8}$$

For sake of simplicity hereafter we omit the parameter t .

Table 4.3: FLC rule table with Teoplitz structure



4.3.1 Design of Signed distance SIFLC

The rule table of conventional FLC has skew symmetry property. For the same control input the boundaries of $(e, e^{\bullet})$ have a stair case shapes. If the quantization of level of independent variable becomes infinitesimal, then the boundaries becomes straight line as shown in Fig. 4.2. Also note that absolute magnitude of the control input proportional to signed distanced from the straight line called switching line [109, 110]. To find the

distance d , let $B(e_0, e_0^{\bullet})$ be an intersection point of the main diagonal line and the line perpendicular to it from a known operating point $A(e_1, e_1^{\bullet})$ as shown in Fig. 4.3.

It can be noted that the main diagonal line can be represented as a straight-line known as the switching line i.e.

$$e + me^{\bullet} = 0 \tag{4.9}$$

Where m is the slope of the main diagonal line L_z as shown in Fig. 4.3. The distance between $A(e_1, e_1^{\bullet})$ and $B(e_0, e_0^{\bullet})$ can be calculated as follows:

$$d = \sqrt{(e_0 - e_1)^2 + (e_0^{\bullet} - e_1^{\bullet})^2} = \frac{\left|e_1^{\bullet} + me_1\right|}{\sqrt{1+\lambda^2}} \tag{4.10}$$

Generalization of (5) can rewrite as follows:

$$d = \frac{\left|e^{\bullet} + me\right|}{\sqrt{1+m^2}} \tag{4.11}$$

For any general point $A(e, e^{\bullet})$ the signed distance defined as follows:

$$d_s = sign(s)\frac{\left|e^{\bullet} + me\right|}{\sqrt{1+m^2}} \tag{4.12}$$

Where

$$sign(s) = \begin{cases} 1 & for\ s > 0 \\ -1 & for\ s < 0 \end{cases} \tag{4.13}$$

Since the sign of the control input is negative for $s > 0$ and positive for $s < 0$, and its magnitude is proportional to the distance from the line, we can conclude that

$$u \propto -d_s \tag{4.14}$$

Hence, the control action can be determined using d_s only. Therefore, we call new FLC as single input fuzzy logic controller. With the derived distance d_s, two dimensional rule table of conventional FLC can be converted into one-dimensional rule table. The reduced rule table is depicted in Table 4.4, where L_{NL}, L_{NM}, L_{NS}, L_Z, L_{PS}, L_{PM} and L_{PL} are the diagonal line of conventional FLC rule Table 4.3. These diagonal lines correspond to the new input, while NL, NM, NS, Z, PS, PM, and PL represents the output of the corresponding diagonal lines as shown in Table 4.4.

Table 4.4: Reduced rule Table

d_S	L_{NL}	L_{NM}	L_{NS}	L_Z	L_{PS}	L_{PM}	L_{PL}
u	NL	NM	NS	ZE	PS	PM	PL

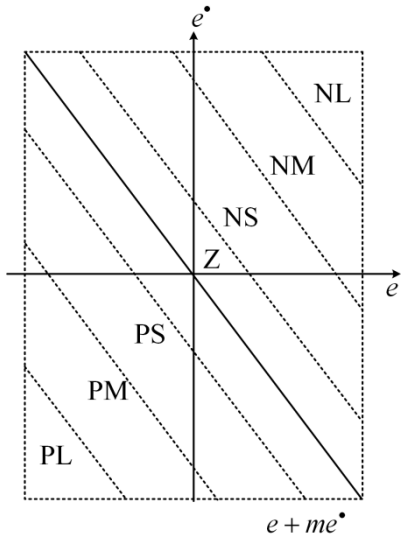


Fig. 4.2: Rule table with infinitesimal quantization levels.

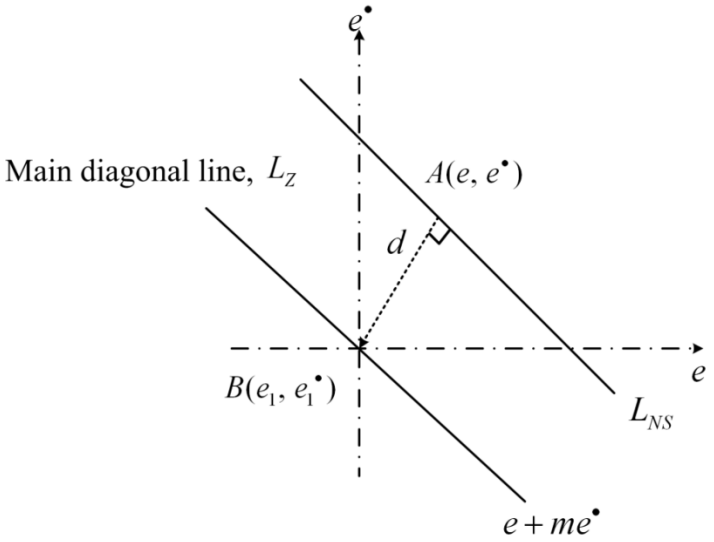


Fig. 4.3: Derivation of signed distance.

4.3.2 Comparison of CFLC and SIFLC

The structure of the single input fuzzy logic controller is shown in Fig. 4.4 this structure is obtained by using signed distance method. The input to the fuzzy controller is d and output is change in the control output u. To generate the final output, the u is multiplied with scaling factor say G_u. The structure of conventional fuzzy logic controller block is shown in Fig. 4.5. By observing Fig. 4.4 the difference in CFLC and SIFLC can be noticed. The inputs scaling factors for conventional FLC are k_e and $k_{e^{\bullet}}$ respectively, and output scaling factor is k_u. The input, output membership function for conventional FLC is shown in Fig. 4.6.

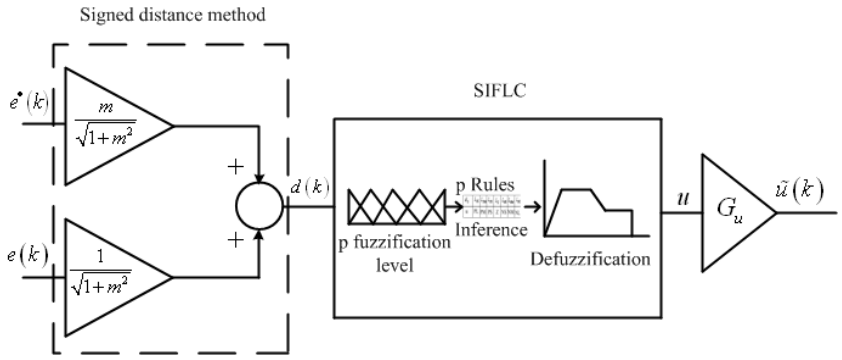


Fig. 4.4: SIFLC control structure.

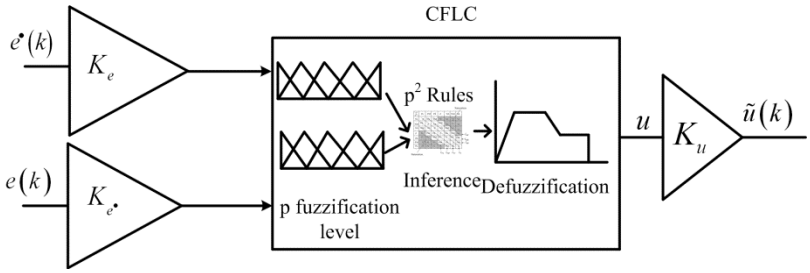


Fig. 4.5: Conventional FLC.

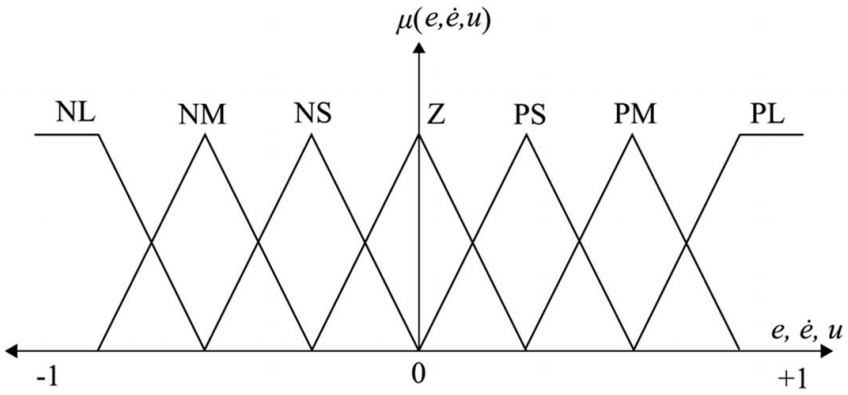


Fig. 4.6: CFLC input (e and $e^{\bullet}$) and output (u) membership functions.

The advantage associated with SIFLC is that the reduction of number of rules. For a conventional fuzzy logic controller with p level of fuzzification requires p^2 rules whereas, in case of SIFLC with p level of fuzzification requires only p rules.

4.3.3 Stability analysis of single input fuzzy logic controller

For a n-dimensional SIFLC the switching hyper plane can be represented [110] as follows:

$$S = e^{(n-1)} + m_{n-1}e^{(n-2)} + \ldots\ldots + m_2 e^{\bullet} + m_1 e = 0. \tag{4.15}$$

Similar to (10), d_s is changed to a general signed distance D_s as

$$D_s = \frac{e^{(n-1)} + m_{n-1}e^{(n-2)} + \ldots\ldots + m_2 e^{\bullet} + m_1 e}{\sqrt{1 + m_{n-1}^2 + \ldots\ldots + m_2^2 + m_1^2}} \tag{4.16}$$

Where D_s represents the signed distance from the operating point to the switching hyper plane as given in (11). With this D_s, the control law (9) is changed to

$$u = -K_f D_s \tag{4.17}$$

Now K_f is the control constant obtained from linear functions. The SIFLC satisfies the pseudo Sliding mode controller represented in [110]. This fact represent that SIFLC based close-loop system is stable. Here, we assume some known upper bounds, say Q and D for the unknown dynamic functions q and d, respectively. Also, the control gain function f has a known bound and is a positive. The stability analysis of the proposed SIFLC is carried out as explained in [17].

Lemma 1: If the following conditions are satisfied:

$$|q| \le Q, |d| \le D, 0 < f_{\min} \le f \le f_{\max} \tag{4.18}$$

And K_f satisfies following in equalities

$$K_f |D_s| \ge f_{\min}^{-1} \left(Q + D + w_d^{(n)} + \sum_{i=1}^{n-1} m_i e^i + \chi \right) \tag{4.19}$$

$$\chi \ge 0$$

Then is stable in the sense of the Lyapunov

Proof: we consider Lyapunov function as follow

$$V = \frac{1}{2} D_s^2 \tag{4.20}$$

Then

$$\begin{aligned} V &= D \dot{D}_s \\ &= \frac{D_s}{\sqrt{1 + m_{n-1}^2 + ... + m_2^2 + m_1^2}} \left(e^n + \sum_{i=1}^{n-1} m_i e^i \right) \end{aligned} \tag{4.21}$$

By using (3) and (16)

$$\dot{V} = \frac{D_s}{\sqrt{m}} \left(q - fu + d - w_d^n + \sum_{i=1}^{n-1} m_i e^i \right) \tag{4.22}$$

Now, substituting the value of u from (4.17) into (4.22)

$$= \frac{D_s}{\sqrt{m}} \left(q - fK_f D_s + d - w_d^{(n)} + \sum_{i=1}^{n-1} m_i e^i \right) \tag{4.23}$$

$$= \frac{D_s}{\sqrt{m}} \left(q - fK_f |D_s| \operatorname{sgn}(D_s) + d - w_d^{(n)} + \sum_{i=1}^{n-1} m_i e^i \right) \tag{4.24}$$

Substituting (4.22) into (4.24), we get

$$\dot{V} \le -\frac{\chi}{\sqrt{m}}|D_S| \tag{4.25}$$

Where $\Lambda = \sqrt{1+m_{n-1}^2+...+m_2^2+m_1^2}$. Therefore, the proposed SIFLC is stable in the sense of Lyapunov.

4.3.4 Control surface of SIFLC

The control surface of SIFLC can be reduced to a two-dimensional plot using 1-dimensional array of the rule table. This can be achieved, by satisfying the procedure outlined in [111]: 1) The input membership function is triangular shape; 2) the output MF has singleton shape; 3) fuzzification using centre of gravity (COG); and 4) defuzzification using COG. The control surface of the SIFLC is shown in Fig. 4.7. This control surface is denoted by ψ_c, which has a constant slope throughout the universe of discourse. This control surface can be achieved when the triangular peaks of the input membership functions and the spacing in between the Singletons are equal. Under these operating conditions, the control output generated by Table II is linear [17], which is given as follows:

$$u = -K_d d_s \tag{4.26}$$

Where K_d is a constant obtained by linear FLC. Here, d_s is bounded with $d_{s1} \le d_s \le d_{sN}$, where d_{s1} and d_{sN} are, respectively, the minimal and maximum values of a signed distance, and N is the number of fuzzy sets for a signed distance.

The piece wise linear (PWL) function easily constructed using look up table. The PWL surface based implementation is simple, because it eliminates the complex process of fuzzification, rule inference and defuzzification. The control surface of the PWL can be constructed with peak location of input and output membership functions.

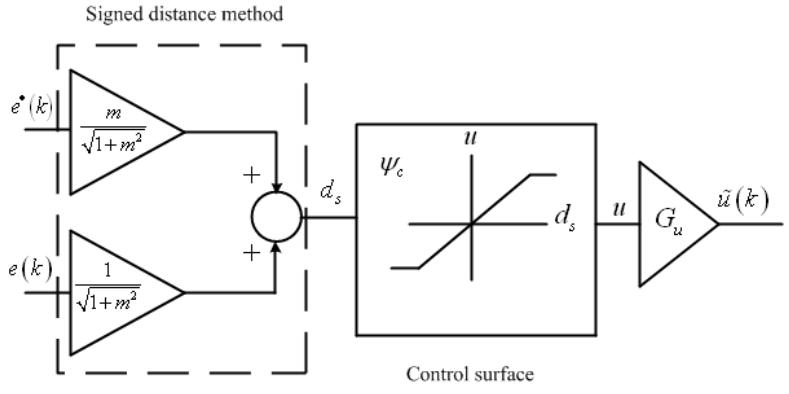


Fig. 4.7: SIFLC with the PWL control surface.

The procedure for obtaining PWL control surface as follow

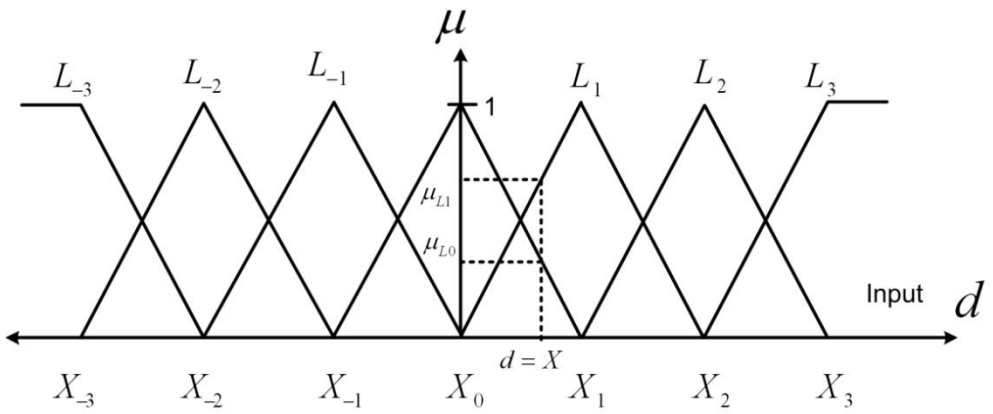


Fig. 4.8: Input membership functions.

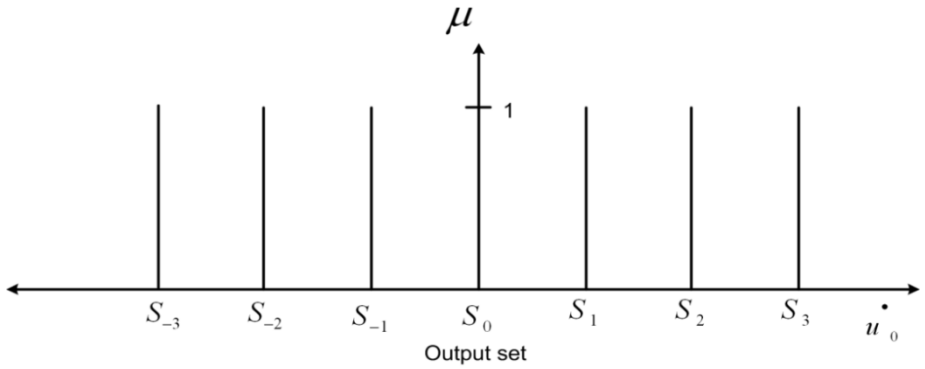


Fig. 4.9: output singleton membership functions

The output $\dot{u}_0$ can be calculated using the Centre of Gravity (COG) operator as

$$\dot{u}_0 = \frac{\sum_{i=-2}^{2} \mu_i S_i}{\sum_{i=1}^{n} \mu_i} \tag{4.27}$$

From Fig. 4.8 and Fig. 4.9 the output is calculated as

$$\dot{u}_0 = \frac{\mu_0 S_0 + \mu_1 S_1}{\mu_0 + \mu_1} \tag{4.28}$$

From Fig. 4.8 intersection point of input membership functions are $(X_{0,}\, 1)$ and $(X_{1,}\, 0)$

$$\mu = \frac{-1}{X_1 - X_0}\left(x - X_1\right) \tag{4.29}$$

At $x = X^{\bullet}$ and $\mu = \mu_0$

$$\mu_0 = \frac{-1}{X_1 - X_0}\left(X^{\bullet} - X_1\right) \tag{4.30}$$

From Fig. 4.8 other intersection points of input membership function such as $(X_{1,}\, 1)$ and $(X_{0,}\, 0)$

The line equations is written down as follow

$$\mu = \frac{1}{X_1 - X_0}\left(x - X_0\right) \tag{4.31}$$

From Fig. 4.8, at $x = X^{\bullet}$ and $\mu = \mu_1$

$$\mu_1 = \frac{1}{X_1 - X_0}\left(X^{\bullet} - X_0\right) \tag{4.32}$$

From (3.30) and (3.31), equation (3.28) can be written as follows

$$\dot{u}_0 = \left(\frac{S_1 - S_0}{X_1 - X_0}\right)X + \frac{X_1 S_0 + X_0 S_1}{X_1 + X_0} \tag{4.33}$$

We can conclude that output of SIFLC the is linear function

$$\dot{u}_0 = md + K \tag{4.34}$$

Where *d* is the input distance variable and *m* is the slope of the line. The variable *K* is the output value when input d is zero, i.e. $K = \dot{u}_0\Big|_{d=0}$

4.4 Reference current generation using anti-Hebbian based on TLS algorithm

The performance of the active power filter depends on its reference current generation. The instantaneous source voltage is

$$v_s(t) = V_m \sin(\omega t) \tag{4.35}$$

When the nonlinear load connected to the source, then it injects the current harmonics in the source. The load current consist of both fundamental and harmonics components, which can be expressed as follows:

$$i_L(t) = \sum_{n=1}^{\infty} I_n \sin(n\omega t + \phi_n) = I_1 \sin(\omega t + \phi_1) + \sum_{n=2}^{\infty} I_n \sin(n\omega t + \phi_n) \tag{4.36}$$

Thus, the instantaneous load power can be expressed as follows:

$$i_L(t) = I_1 \sin(\omega t) * \cos(\phi_1) + I_1 \sin(\phi) * \cos(\omega t) + \sum_{n=2}^{\infty} I_n \sin(n\omega t + \phi_n) \tag{4.37}$$

The load current is consists of active power, reactive power and harmonics component and can be expressed as:

$$i_L(t) = i_f(t) + i_r(t) + i_h(t) \tag{4.38}$$

The compensating current injected by active power filter is

$$i_c(t) = i_L(t) - i_f(t) = i_L(t) - I_1 \cos(\phi)\sin(\omega t) \tag{4.39}$$

After compensation, the current supplied by the source is

Where $I_m = I_1 \cos\phi_1$

$$i_c(t) = i_L(t) - I_m \sin(\omega t) \tag{4.40}$$

The voltage across the dc side capacitors varies with the load demand. In order to maintain dc capacitors voltage constant, the PI/SIFLC controller is used. Under this conditions, assuming that the current drawn from the source is sinusoidal and in phase with respective voltages. The instantaneous value of source current is

$$i_s(t) = I_m \sin(\omega t) \tag{4.41}$$

The power delivered by the source

$$p_s(t) = \frac{1}{2} V_m I_m - \frac{1}{2} V_m I_m \cos(2\omega t) = p_{dc} + p_{ac} \tag{4.42}$$

Where p_{dc} and p_{ac} are ac and dc component of the power delivered by the source. The load real power can be expressed as

$$p_l(t) = V_m \sin(\omega t) \times I_1 \sin(\omega t + \phi_1) + V_m \sin(\omega t) \sum_{n=2}^{\infty} I_n \sin(n\omega t + \phi_n) \tag{4.43}$$

$$p_l(t) = \frac{1}{2} I_1 \cos(\omega t) + p_{lac} = p_{lac} + p_{ldc} \tag{4.44}$$

Where p_{lac} and p_{ldc} are ac and dc components of the load power. The compensating power injected by the active power filter is

$$p_c(t) = p_s(t) - p_l(t) \tag{4.45}$$

$$p_{cdc}(t) = (p_{dc} - p_{ldc}) + (p_{ac} - p_{lac}) \tag{4.46}$$

Assume that the reference voltage is V_{dc} and the change in reference voltage is δV_{dc} due load disturbance. The change in energy handled by the capacitor is

$$\delta E = \frac{1}{2} C (V_{dc} + \delta V_{dc})^2 - \frac{1}{2} C V_{dc}^2 \tag{4.47}$$

The ΔV_{dc}^2 is small as compared to ΔV_{dc}

$$\delta E = \frac{1}{2} C \times V_{dc} \times \delta V_{dc}$$

$$\delta E = p_{cdc} T \tag{4.48}$$

$$\delta V_{dc} = \frac{V_m}{2 C V_{dc}} (I_m - I_{s1} \cos(\phi_1))$$

$$\Delta V_{dc} = k (I_m - I_1 \cos(\phi_1)) \tag{4.49}$$

Where

$$k = \frac{V_m}{2 C V_{dc}}$$

$$\Delta V_{dc} = k (I_m - W_p)$$

$$I_m = \left(W_p + \frac{1}{k} \Delta V_{dc} \right) \tag{4.50}$$

$$I_m = \left(W_p + W_{dc} \right)$$

Where weight W_p is the active component of the load current. The weight W_{dc} is associated with the dc voltage regulation.

$$I_m = W_A \tag{4.51}$$

Then the compensating current (4.39) can be modified as

$$i_c(t) = i_L(t) - W_A \sin(\omega t) \tag{4.52}$$

According to the total least square algorithm [166], the weight for next iteration can be expressed as

$$W_{A(i+1)} = W_A + r i_c(t) \left(\sin(\omega t) + k i_{la}(t) W_A \right) \tag{4.53}$$

$$W_{B(i+1)} = W_B + r i_c(t) \left(\sin\left(\omega t - \frac{2\pi}{3} \right) + k i_{lb}(t) W_B \right) \tag{4.54}$$

$$W_{C(i+1)} = W_C + r i_c(t) \left(\sin\left(\omega t - \frac{4\pi}{3} \right) + k i_{lc}(t) W_C \right) \tag{4.55}$$

The control strategy for equation is given in Fig. 4.10

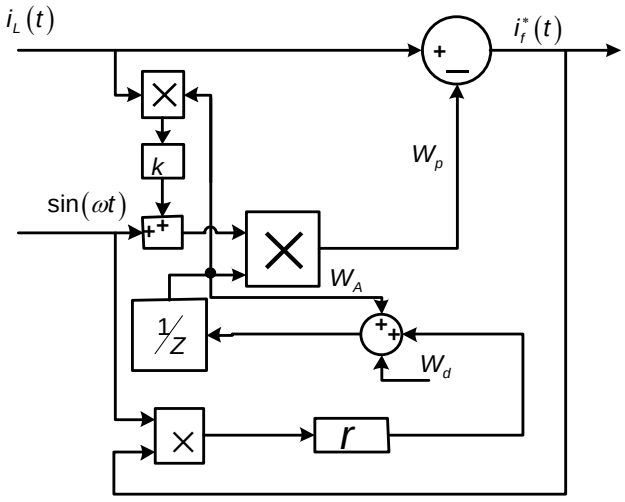


Fig. 4.10: Reference current generation using anti-Hebbian based on TLS algorithm for phase-a.

4.4.1 Voltage regulation of dc side capacitors

Fig. 4.11 shows the block diagram of the voltage regulation loop for phase-a, which balances the voltage of each dc side capacitor of the active power filter. In this voltage balancing scheme, each dc side capacitor voltage is summed up and subtracted and compared with the dc reference voltage (V_{ref}). The error is processed in a PI/SIFLC controller and the output of the PI/SIFLC controller decides the amount of real power required to keep

that particular capacitor voltage at its set reference level. When dc voltage reference is greater than the capacitor voltage, an amount of active power flows into that particular capacitor, thus leading to increase of capacitor voltage. On the other hand, when dc voltage reference is lower than the capacitor voltage, an amount of active power is drawn from that particular capacitor, thereby bringing down the capacitor voltage to its reference value. The sum of the outputs of the SIFLC controllers (W_d) is the total amount of weight required to keep the capacitor voltages of individual cells at their corresponding set reference values.

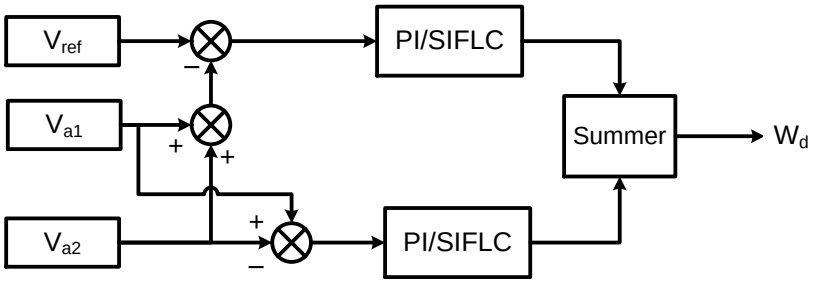


Fig. 4.11: voltage regulation loop for phase-a.

4.5 Simulation results

The MATLAB simulation is carried out to show the compensation characteristics of the active power filter with PI and SIFLC. The purpose of this simulation study is to show the response of the SIFLC is better than PI controller. The Conventional FLC is of the Mamdani's inference and its input membership functions conversion is shown in Fig. 4.12 (a). Fig. 4.12 (b) shows the output membership function with equal spaced singleton. These membership functions universes of discourse are designed with trial error approach using the MATLAB/Simulink Fuzzy logic Toolbox. The rules base of conventional FLC is given in Table 4.5. The control surface of conventional FLC is shown in Fig. 4.13 (a). The reduced rule base of SIFLC is given in Table 4.6. Fig. 4.13 (b) shows the resulting piece wise linear control surface. Note that the Piece wise linear function is designed to have 0.6969 slope throughout the universe of discourse.

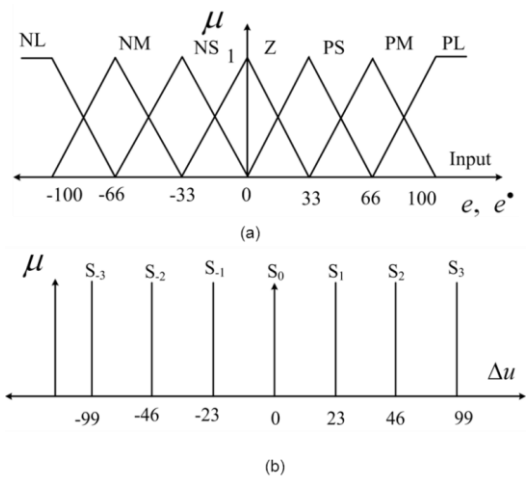


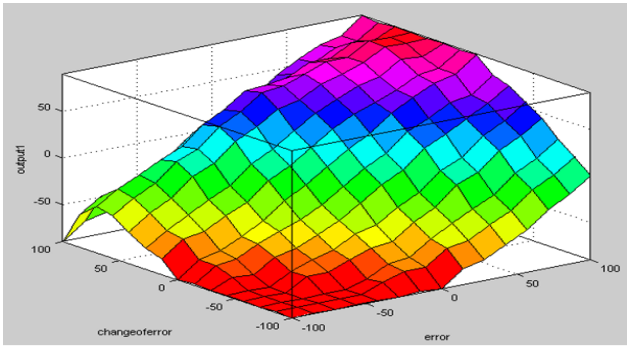
Fig. 4.12: Membership functions (a) error and change of error for inputs and (b) output.

Table 4.5: Rule Table with Teoplitz structure for dc voltage regulation (conventional FLC rule base)

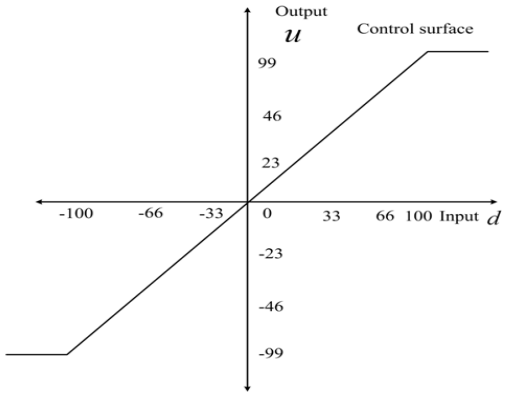
e/ė	PL	PM	PS	ZE	NS	NM	NL
NS	0	-33	-66	-100	-100	-100	-100
NM	33	0	-33	-66	-100	-100	-100
NL	66	33	0	-33	-66	-100	-100
ZE	100	66	33	0	-33	-66	-100
PS	100	100	66	33	0	-33	66
PM	100	100	100	66	33	0	-33
PL	100	100	100	100	66	33	0

Table 4.6: Reduced SIFLC rule table

d_{s1}	-70	-46.6	-23.3	0	23.3	46.6	70
u_{SIFLC}	-99	-66	-33	0	33	66	99



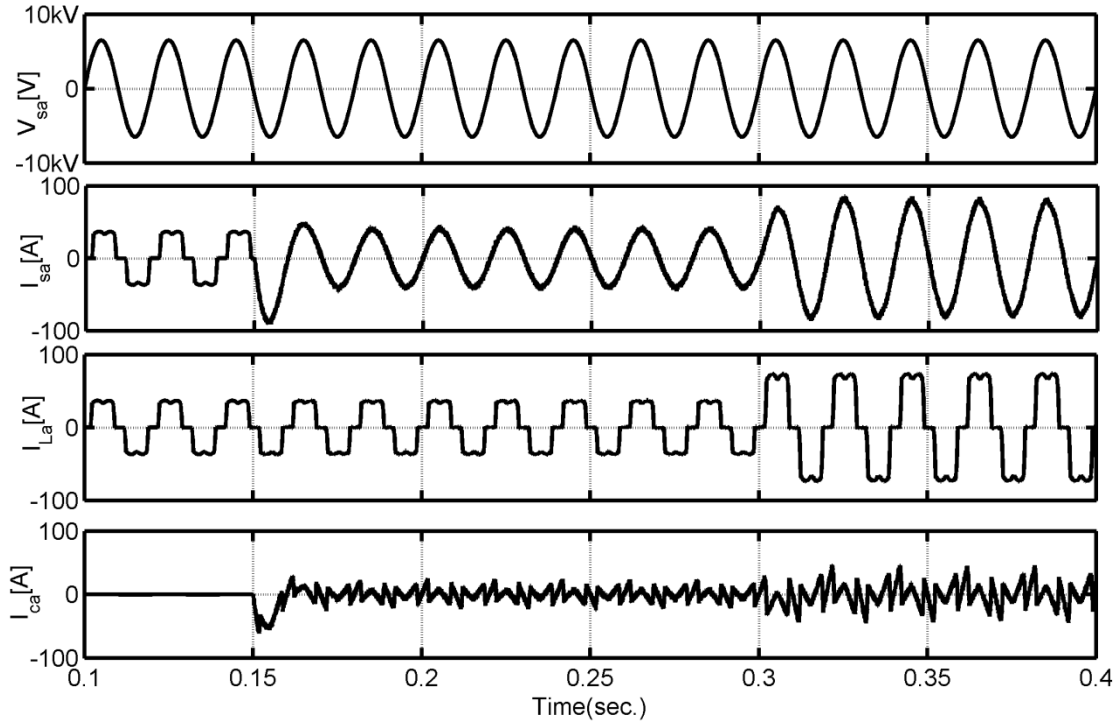
(a)



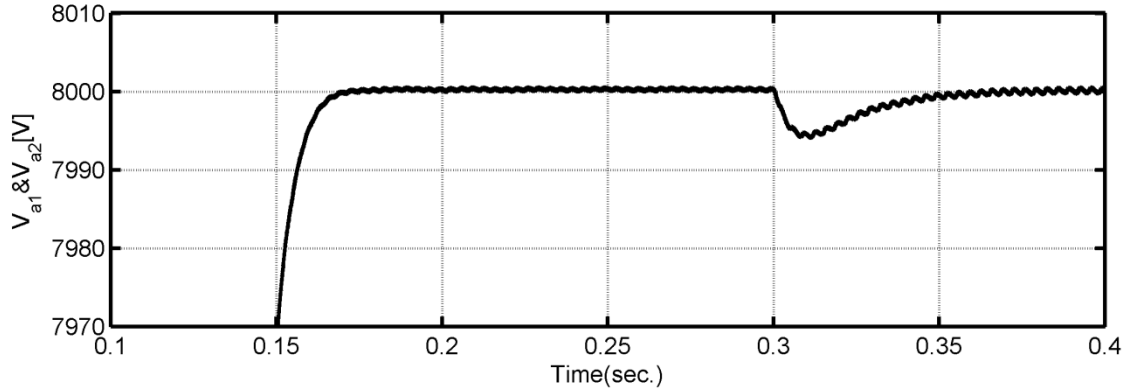
(b)

Fig. 4.13: (a) Conventional FLC Control surface. (b) Equivalent PWL (SIFLC) control surface corresponding to MFs in Fig. 4.12

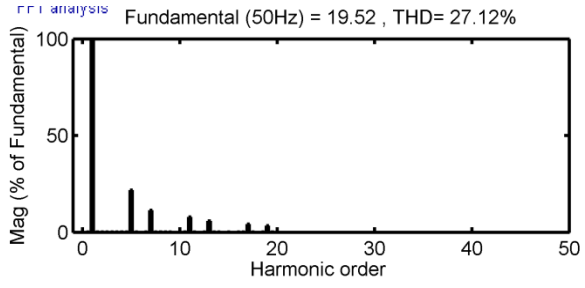
Initially, the nonlinear load consist of the diode rectifier with RL load on dc side is connected to the source. This nonlinear load induce high amount of harmonics in the source.



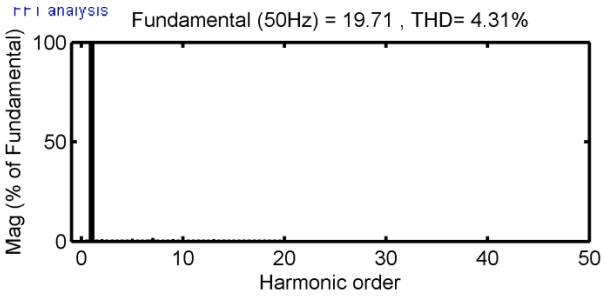
(a) Simulated current waveforms



(b) DC side capacitors voltages.

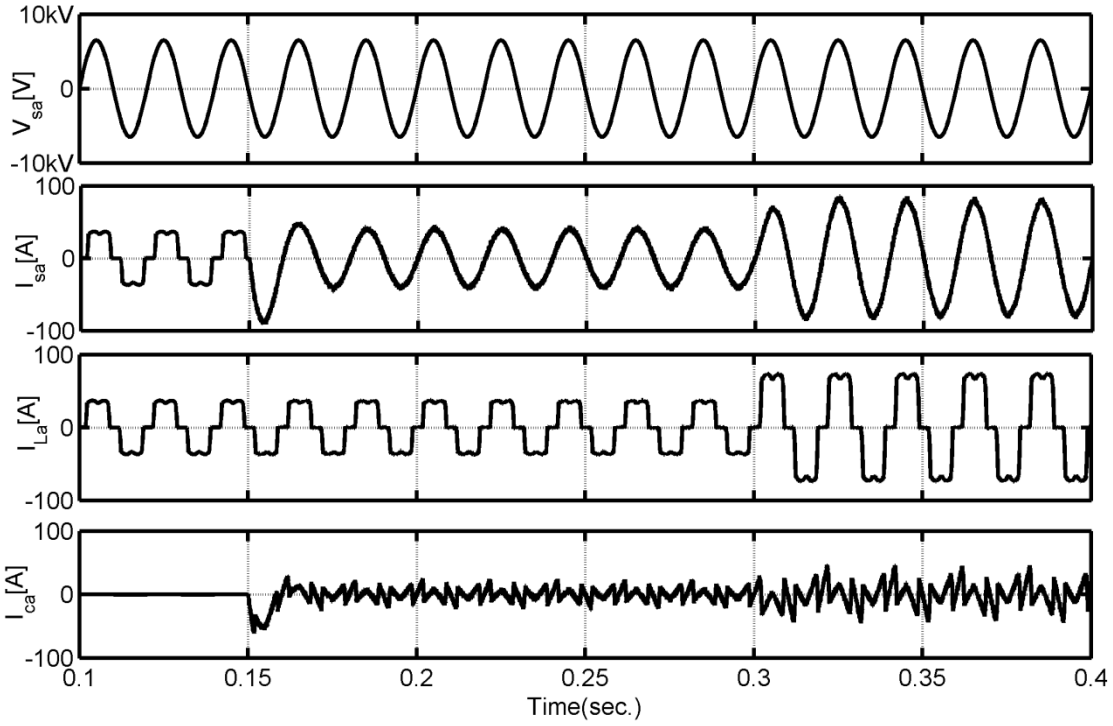


(c) Source current before compensation

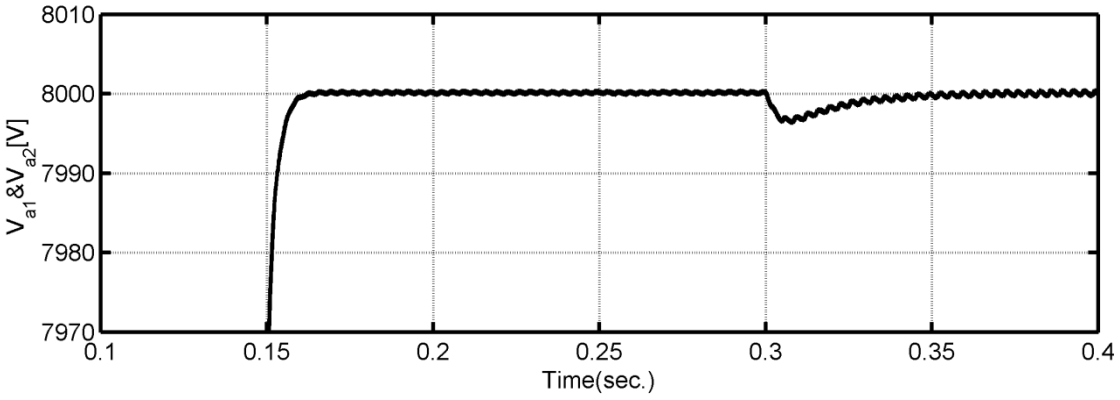


(d) Source current after compensation.

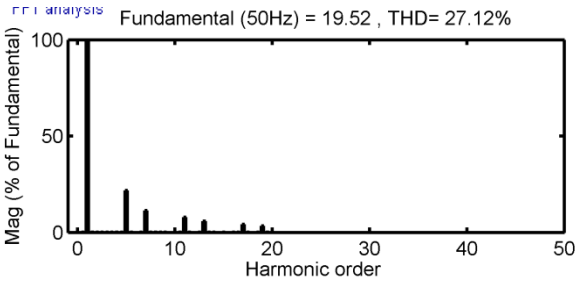
Fig. 4.14: Performance of APF for an RL load on the dc side of an uncontrolled rectifier using anti-Hebbian algorithm based on TLS integrated with PI controller.



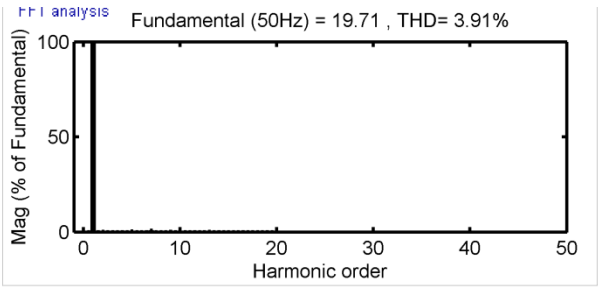
(a) simulated current waveform



(b) DC side capacitor voltages.



(c) Source current before compensation.



(d) Source current after compensation.

Fig. 4.15: Performance of APF for an RL load on the dc side of an uncontrolled rectifier using anti-Hebbian algorithm based on TLS integrated with SIFLC controller.

The active power filter is connected at point of common coupling to compensate the harmonics and reactive power requirement of six pulse uncontrolled rectifier. Fig. 4.14 (a)-(d) shows the simulated response of source current, compensating current, dc side capacitor voltages (V_{a1} to V_{a2}), harmonic spectra of load and respectively with source currents PI controller, while Fig. 4.15 (a)-(d) shows the simulated response of source currents, compensating current, dc side capacitor voltages (V_{a1} to V_{a2}), harmonic spectra of load and source currents respectively with SIFLC for phase-a. At instant t=0.15s, when APF is switched-on the source current tend to sinusoidal from non-sinusoidal waveform in both the cases as shown Fig. 4.14 (a) and Fig. 4.15 (a). The THD of the load current is 27.12%, but the source current THD is reduced to 2.15% and 2.00% with PI and SIFLC controllers respectively. The initial rise of peak value of the source current is 90.92A in case of PI controller and 85.26A in case of SIFLC controller respectively. At instant APF is switched-on at t=0.15s, dc side capacitors voltages increases gradually in both cases.

However, the settling time required for dc voltage to attain reference level is 0.05s in case of PI and in case of SIFLC settling time required is 0.005s as seen in Fig. 4.14 (b) and Fig. 4.15 (b). However, the source current stabilizes almost taking two cycles in case of PI controller whereas in case of SIFLC source current stabilize within one cycle. When load current is changes at t=0.3s, the dc side capacitors voltage changes from its reference level to compensate the increase in load current. This causes drop in capacitor voltage which is restored in 0.05s and 0.005s with PI and SIFLC respectively. This shows that the transient performance of the active power filter with SIFLC better than that of the PI controller.

4.6 Experimental validation

To validate the simulated response of the active power filter with PI controller and SIFLC, a scaled down prototype of active power filter is developed. The voltage and current signals are measured using LEM voltage and current sensors. The measured voltage and current signal conditioned before being fed to DSPACE 1104 digital controller. The dc power supply for the drivers of IGBTs are obtained using dc-dc converter. The nonlinear load is realized using power diode and RL load on dc side. The uncontrolled diode rectifier with RL-load on dc side and active power filter is connected at PCC. Fig. 4.16 shows the load currents waveform and corresponding THD spectrum. Initially, uncontrolled rectifier injects harmonics and reactive power in the source and the total harmonic distortion is found to be 24.4%. The down scaled prototype of the active power filter has been is tested for harmonic elimination and reactive power compensation with PI controller and SIFLC controllers and the experimental waveforms under steady state condition are shown in Fig. 4.17. The source voltage source current, load current and compensating current for phase-*a* with PI and SIFLC is shown in Fig. 4.17 (a) and Fig. 4.17 (b) respectively. These figures and all the

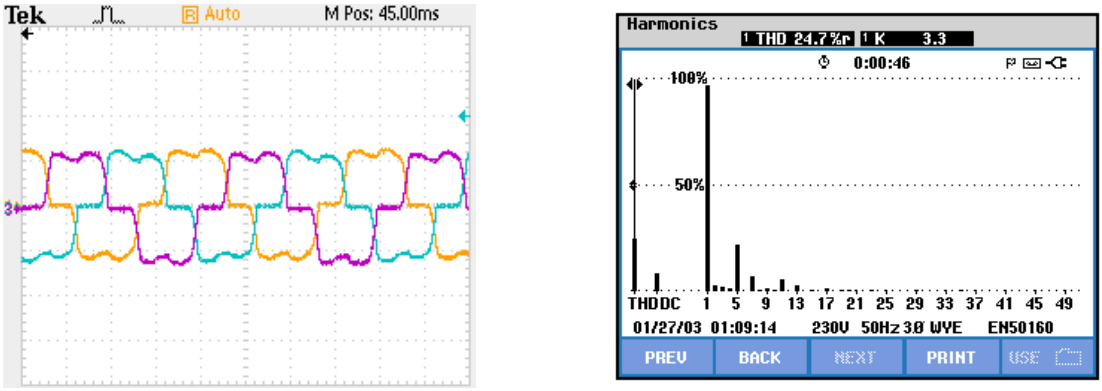
subsequent figures showing similar experimental results, the different waveforms are recognised as:

Channel–1: source voltage (X-axis: 10 ms/div., Y-axis: 100 V/div.),

Channel–2: source current after compensation (X-axis: 10 ms/div., Y-axis: 5 A/div.),

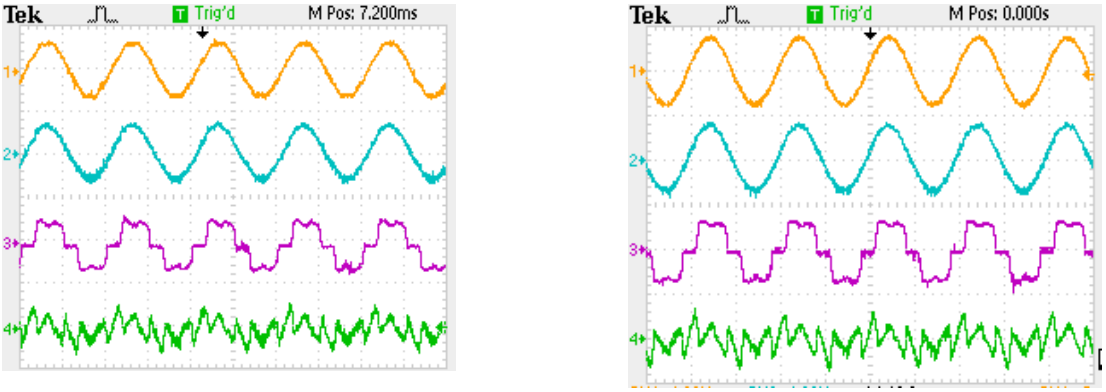
Channel–3: load current (X-axis: 10 ms/div., Y-axis: 5 A/div.),

Channel–4: compensating current injected by the active power filter (X-axis: 10ms/div., Y axis: 5 A/div.).

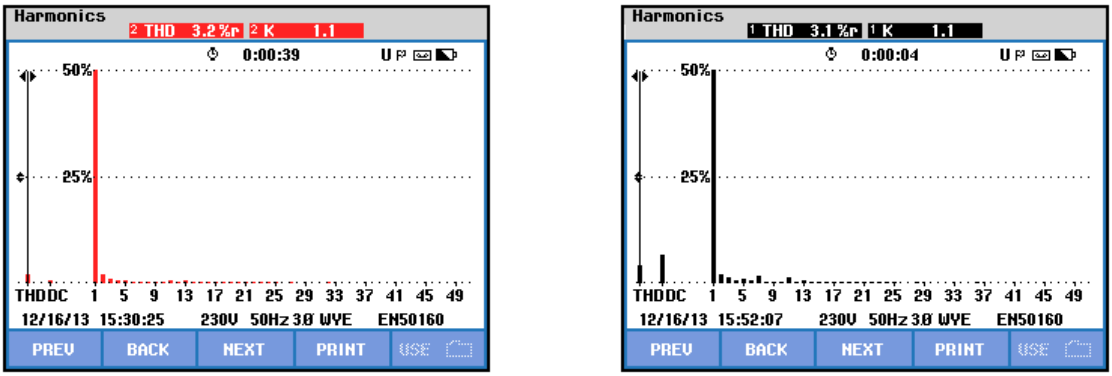


(a) (b)

Fig. 4.16: (a) Three phase load current (b) load current THD spectrum for phase-a.



(a) (b)



(c) (d)

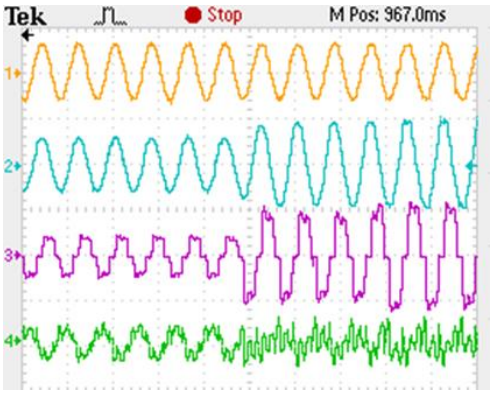
Fig. 4.17: Experimental results of 3P3W APF for an RL-load on the dc side of a phase-uncontrolled rectifier with PI controller and SIFLC.

The THD spectrum of load current after compensation with PI controller and SIFLC controller are shown in Fig. 4.17 (c) and (d) respectively. From these figures it is observed that after compensation with active power filter, the load current %THD 24.4%, while source current %THD is reduced to 3.2% and 3.1% with PI controller and SIFLC controller respectively. The power factor becomes unity in both the cases. However, the steady state performance of active power filter with PI controller and SIFLC are identical. The source currents THDs after compensation with active power filter are well within the limits imposed by IEEE–519–1992 standard.

4.6.1.1 Transient Performance of active power filter

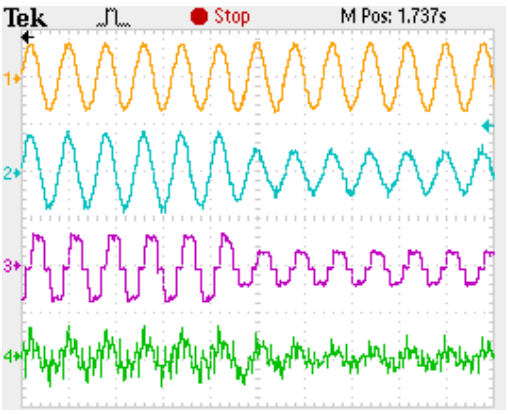
The transient performances of the active power filter with uncontrolled rectifier with RL-load on dc side are shown in Fig. 4.18. Fig. 4.18 (a) shows the experimental results of source voltage, source current after compensation, load current and compensating currents for phase-*a* with PI controller and SIFLC with increase in the load current, while Fig. 4.18 (b) show these experimental results with rejection in load current.

(a.1) PI controller

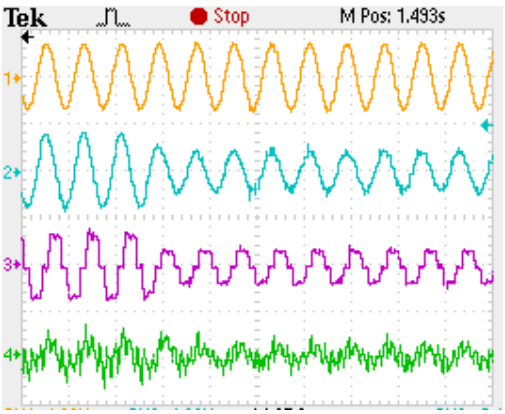


(a.2) SIFLC controller

(a) with increase in load current



(b.1) PI controller



(b.2) SIFLC controller

(b) with rejection in load current

Fig. 4.18: Load perturbation response of active power filter for six pulse diode rectifier RL-load on the dc side with PI controller and SIFLC controller.

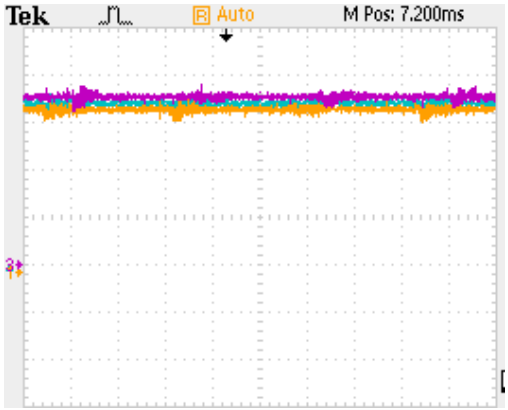
In Fig. 4.18 (a), the load current rms value has been increased from 1.5A to 3.2A and the corresponding change in the source current are from 1.5A to 5.2 A with PI controller and 1.5 to 5 A with SIFLC controller respectively. It is also observed that the change in source current is very high in case of PI controller than SIFLC controller. The source current is achieved steady state almost taking 4-5 cycles in case of PI controller, whereas in case of SIFLC, source current reach steady within 1-2 cycles. Thus, the dynamic response of the SIFLC is better than the PI controller for an increased load condition.

As seen in Fig. 4.18 (b), the load current rms value has been decreased from 3.2A to 1.5A and the corresponding change in the source current are from 3.2 to 1.7 A with PI controller and 3.2 to 1.5 A with SIFLC respectively for two cycles of waveform. In this case also the observed change in source current is very high in case of PI controller than SIFLC controller. The dynamics response is fast in case of SIFLC than PI controller for a decreased load condition.

4.7 DC capacitors voltage regulation

The steady-state performance of active power filter dc side capacitor voltages of H-bridge cells for PI controller and SIFLC controller are shown in Fig. 4.19. The scales of these waveforms are: X-axis: 10 ms/div., Y-axis: 13 V/div.

As seen from Fig. 4.19 (a) with PI controller, large ripple content in the dc side capacitors voltages is observed. The maximum peak-to-peak ripple in the individual voltages of the dc side capacitors is around 0.8 V which affects the performance of the APF. However, the dc side capacitor voltages of H-bridge cell is regulated at their set reference value of 60 V and almost balanced, But, from Fig. 4.19 (b) it is observed that the in case of SIFLC controller, The maximum peak-to-peak ripple in the individual voltages of the dc side capacitors is around 0.3V which is better than the PI controller. The dc side capacitor voltages of H-bridge cell are well regulated at their set reference value of 100 V and dc side capacitor voltages are almost balanced.



(a) dc side capacitor voltages (v_{a1}, v_{a2} and v_{b1})

(b) dc side capacitor voltages (v_{a1}, v_{a2} and v_{b1})

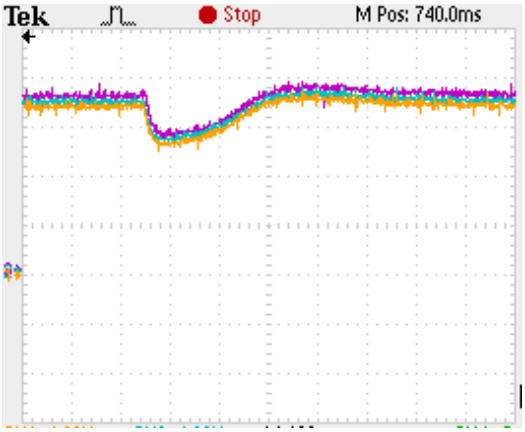
Fig. 4.19: Experimental results of capacitor voltages of the H-bridge cells for a five-level CHB MLI based active power filter.

4.7.1.1 DC voltage regulation during Transient Conditions

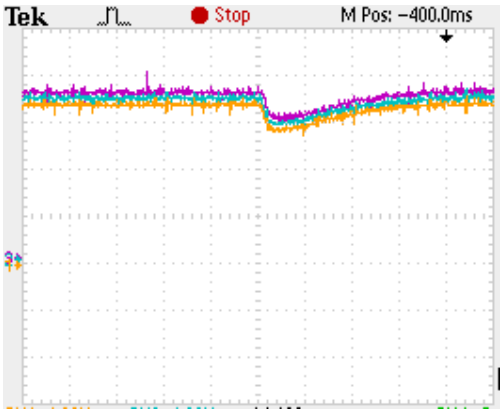
The transient performance of dc side capacitor voltages of active power filter with PI and SIFLC are also studied for increase and reduction of load current.

(a) *with increase in load current*

Fig. 4.20 shows the experimental results of dc capacitor voltages with PI and SIFLC controller for increase in the load current. Fig. 4.20 (a) shows the dc side capacitor voltages v_{a1}, v_{a2} and v_{b2} (X-axis: 25 ms/div. and Y-axis: 13 V/div.) with PI controller whereas Fig. 4.20 (b) shows these dc side capacitor voltages waveform with SIFLC controller.



(a) Capacitor voltages (v_{a1}, $v_{a2\ and}$ v_{b1}) with PI controller.



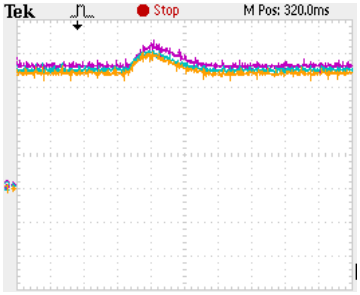
(b) Capacitor voltages (v_{a1} $v_{a2}$and v_{b1}) with SIFLC controller.

Fig. 4.20: Experimental results of capacitor voltages with increase in load current.

In both cases, at the instant when load current increases, the dc capacitor voltage drops from its set reference value to compensate increased the load current. This drop is due to release of the stored energy of the capacitors to compensate the increase load demand and restored in 2-3 cycles in case of PI controller. But with SIFLC, the drops in capacitor voltages are restored in 1-2 cycles. Thus, the dynamics response of the SIFLC is better than PI controller.

(b) *with step reduction in load current*

The experimental results of dc capacitor voltages with PI and SIFLC for reduction in the load current are shown in Fig. 4.21.



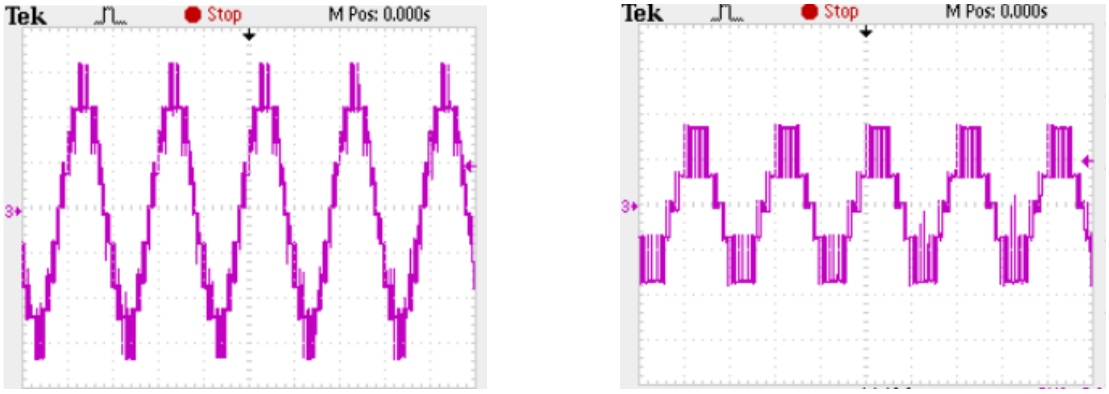
(a) Capacitor voltages (v_{a1}, $v_{a2\ and}$ v_{b1}) with PI controller.

(b) Capacitor voltages (v_{a1}, $v_{a2\ and}$ v_{b1}) with SIFLC controller.

Fig. 4.21: Experimental results of capacitor voltages ($v_{a1,}$ v_{a2} and v_{b1}) of the H-bridge cell of phase–*a* with decrease in load current.

Fig. 4.21 (a) shows the dc side capacitor voltages v_{a1} v_{a2} and v_{b2} (X-axis: 25 ms/div. and Y-axis: 13 V/div.) with PI controller technique while Fig. 4.21 (b) shows these capacitor voltages with SIFLC controller.

In both these cases, at the instant when load current decreases, the dc capacitor voltage increases from its set reference level to balance reduction in the load current demand. This increase in capacitor voltages are restored in 4–5 cycles with PI controller. On the other hand, with SIFLC, this is achieved in 3-4 cycles. Hence, dynamic performance of the SIFLC controller is better than PI controller in load rejection condition also. The experimentally obtained line to line voltage and line to neutral voltages are shown in Fig. 4.22.



(a) (b)

Fig. 4.22: voltage waveforms: (a) line to line voltage (b) line neutral voltage.

4.7.2 Comparison with Simulation Results

In the simulation studies presented in section 4.5, a 3P3W CHBMLI based APF is carried out at 11 kV. However, due to the constraints involved in the development of prototype, the experimentation is conducted at a reduced line voltage of 100 V. As the experimentation is carried out at reduced system parameters, for validating the experimental results, the simulation studies is also carried out with reduced system parameters. The parameters used in the actual simulation and downscaled simulation studies are given in Table 3.2. The downscaled simulation parameters are kept as same as possible to the experimental parameters given in Table 3.2

The simulation results with a uncontrolled rectifier with a *RL* load on the dc side has been considered as a nonlinear load and the simulation studies are shown in Fig. 4.23 and Fig. 4.24 for PI and SIFLC controller respectively integrated with anti-Hebbian based on TLS algorithm. Fig. 4.23 (a)-(d) shows the simulated waveforms, dc side capacitors voltages of the APF (v_{a1} and v_{a2}), THD spectra of load and source currents respectively with PI, while Fig. 4.24 (a)-(d) shows these results for SIFLC integrated with anti-Hebbian based on TLS

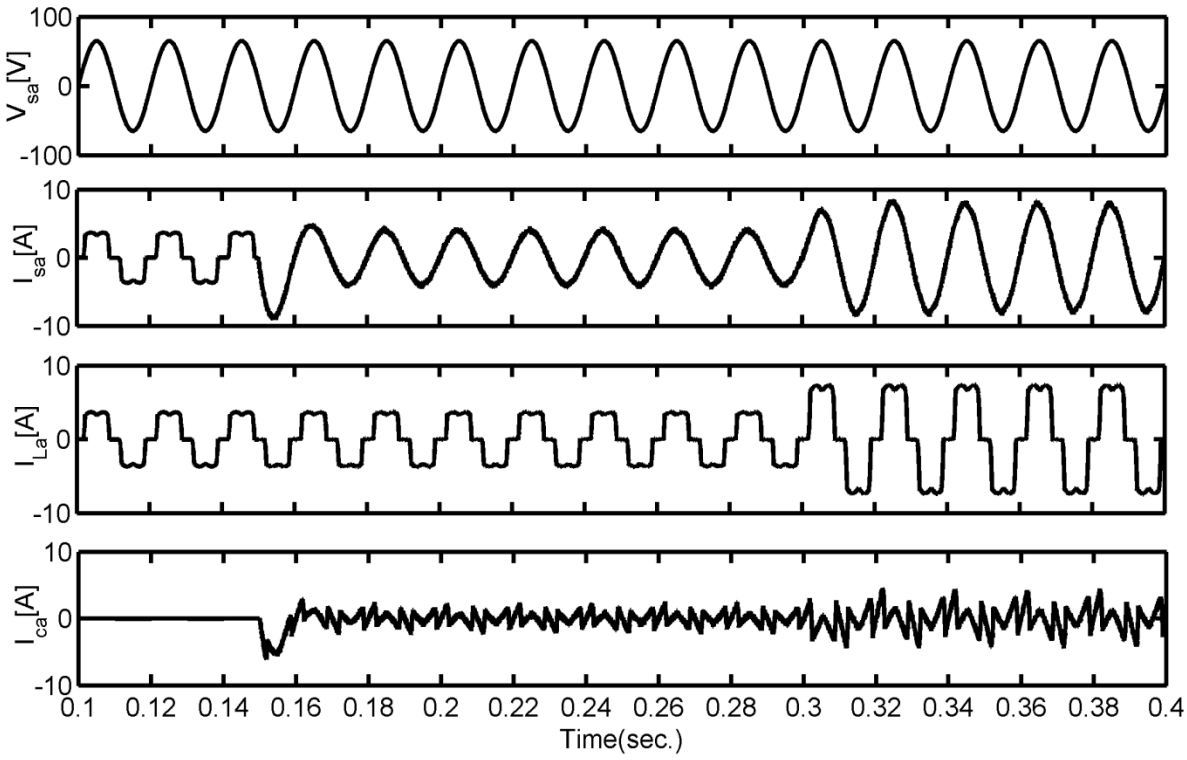
algorithm. In Fig. 4.23 (a) and Fig. 4.24 (a), the channels shown are as follows (from top to bottom): channel-1: phase-*a* source voltage (v_{Sa}), channel-2: phase-*a* source current (i_{Sa}), channel-3: phase-*a* load current (i_{La}) and channel-4: phase-*a* current injected by APF (i_{Ca}). As can be seen from both these figures, the simulation results are almost identical with experimental results for both controller integrated with anti-Hebbian algorithm based on TLS algorithm.

Table 4.7: The parameters used in the simulation studies.

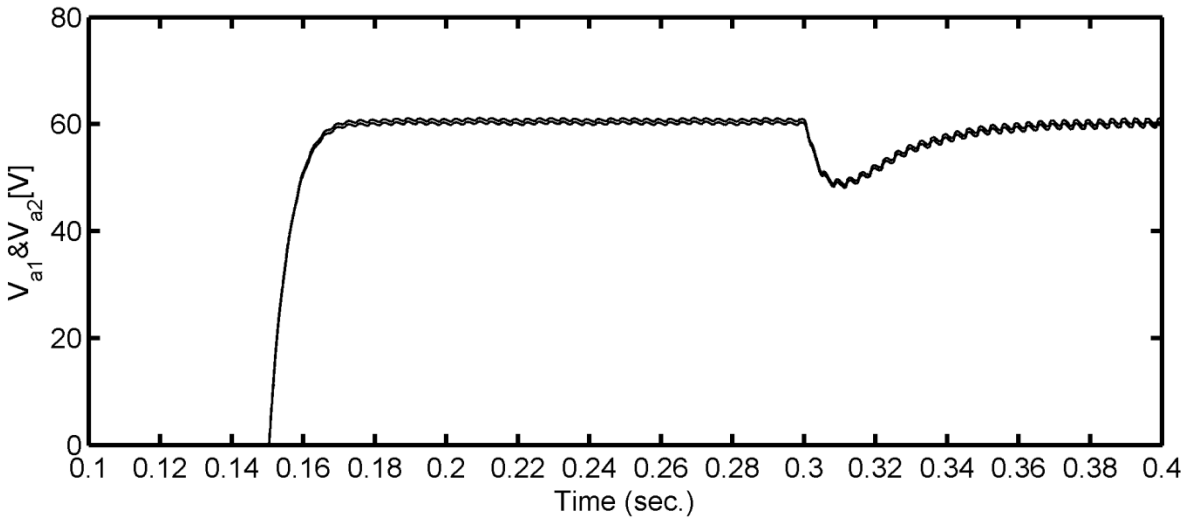
Parameters	**For the actual APF**	**For the downscaled APF**
AC line parameters	Three-phase, three-wire, 11 kV, 50 Hz	Three-phase, three-wire, 100 V, 50 Hz
DC bus voltage of APF	8000 V (for each capacitor in the H-bridge cell)	60 V (for each capacitor in the H-bridge cell)
DC bus capacitance of APF	58μF (for each capacitor in the H-bridge cell)	1800 μF (for each capacitor in the H-bridge cell)
APF interfacing	L_c = 19 mH	L_c = 2.4 mH
Commutation inductance	L_f = 2 mH	L_f = 1 mH
PWM switching frequency	1 kHz	1 kHz
PI controller parameters	K_p = 1.3, K_i = 0.8	K_p = 0.8, K_i = 1.9
Load	Three-phase uncontrolled rectifier with *RL load*	Three-phase uncontrolled rectifier with *RL* load
Sampling time	T_s = 10 μs.	T_s = 50 μs.

However, in simulations results, the source current THDs are nearly 5% with both controller, and these values are almost identical with experimental values. The sampling time of the experimental study is larger than the sampling time of actual simulation study. This is due to the fact that, for implementation of control algorithm in dSPACE requires a minimum sampling time. This ensures the effectiveness of control scheme integrated with P/SIFLC controller with larger sampling time gives same results as that of the simulation study.

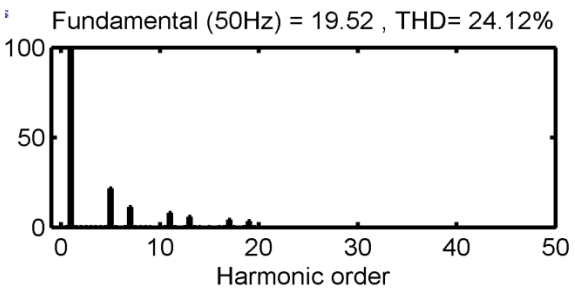
The comparison of experimental and simulation results with non-linear load is given in Table 4.8 for anti-Hebbian algorithm based on TLS integrated with PI and SIFLC controllers.



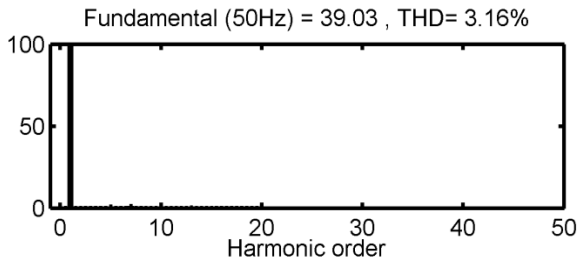
(a)



(b)

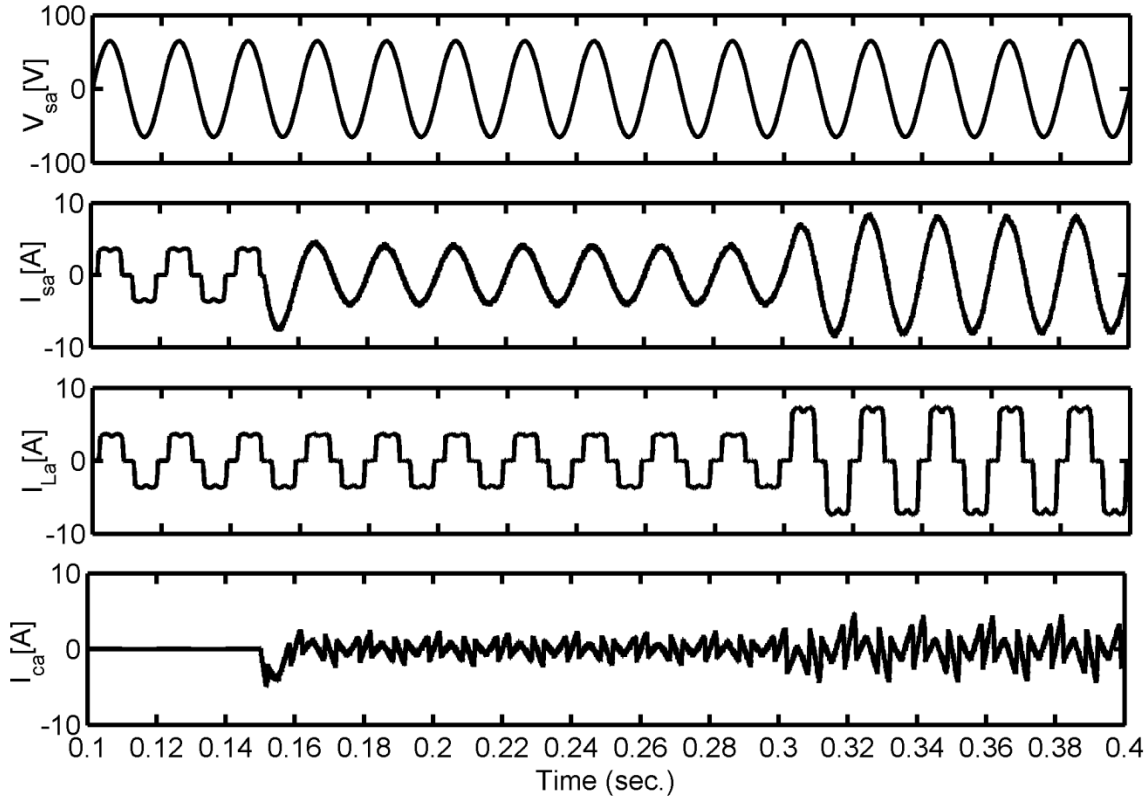


(c)

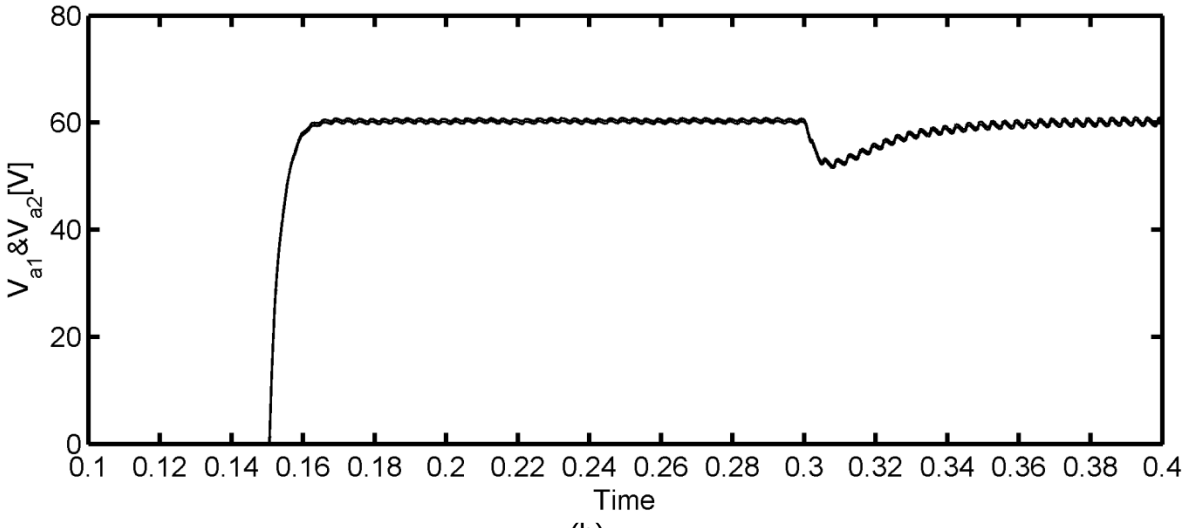


(d)

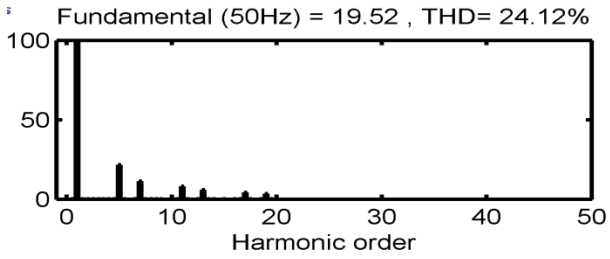
Fig. 4.23: Performance of APF with scaled down simulation studies for a *RL* element at its dc side of an uncontrolled rectifier with PI controller



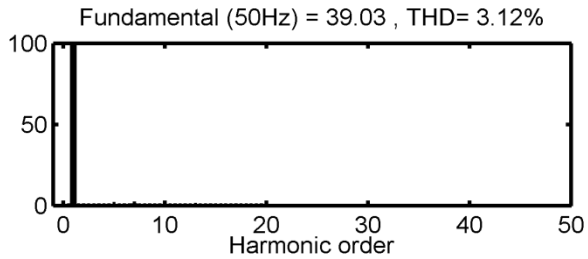
(a)



(b)



(c)



(d)

Fig. 4.24: Performance of APF with scaled down simulation studies for a *RL* load on dc side of an uncontrolled rectifier with SIFLC controller.

Table 4.8: Comparison of experimental and simulation results with different controller with anti-Hebbian based on TLS control algorithm.

Parameter	PI controller		SIFLC controller	
	Exp.	Simulation	Exp.	Simulation
Load current (A, rms)	3.3	3.43	3.1	3.09
% THD of load current	24.7	24.12	24.7	24.12
Source current (A, rms)	3.2	3.16	3.1	3.12
% THD of source current	3.9	4.78	3.9	4.91
Maximum peak-to-peak ripple in dc voltages of H-bridge cells (V)	0.8	0.9	0.3	0.5
% fall of voltage during load change (%Vd_{cref})	2.49	2.89	2.22	2.21

As can be seen from this table the downscaled simulation results are in good agreement with the experimental results. However, simulation and experimental results shows that the anti-Hebbian algorithm based on TLS works effectively with SIFLC controller.

4.8 Conclusion

The dspace implementation of the single fuzzy logic controller for voltage regulation of the CHBMLI based active power filter is described in the present chapter. The single input fuzzy logic controller is derived from the conventional FLC using concept of the signed distance. The single input fuzzy logic controller reduces the 3-D control surface to piece wise linear control surface. The single input fuzzy logic controller with PWL simplifies the implementation procedure and reduces the complexity such as fuzzification, rule inference and defuzzification.

The compensation performance of the CHBMLI based active power filter is observed with PI controller and SIFLC in steady state and transient conditions. Based on simulated responses, it can be concluded that the SIFLC based active power filter performs satisfactorily for compensation of harmonics current and reactive power requirement of the nonlinear load. After providing the compensation by active power filter, input supply current tend to sinusoidal and in phase with respective phase voltages. Also, compensation process reduces the supply current THD well below 5%. However, steady state performance of the PI controller integrated with anti-Hebbian based on TLS algorithm are comparable with results obtained with SIFLC integrated with anti-Hebbian based on TLS.

Dynamic response of the SIFLC controller integrated with anti-Hebbian based on TLS is also explained in detailed simulation studies and found better as compared PI controller control scheme, in terms of settling time and % fall/rise in dc side capacitors voltages. The simulated response shows that the large deviation of the dc side capacitors voltage with longer settling time using PI controller, whereas good compensation, less voltage deviation of dc side capacitors voltages with faster settling time from SIFLC controller. Based on simulation study, it can observe that the SIFLC has a better transient response over PI controller. The SIFLC gives fast response and virtually no overshoot. The SIFLC controller integrated with anti-Hebbian based on TLS algorithm provides improved performance in terms of overshoot limitation and sensitivity to parameter variation.

The proposed controller with anti-Hebbian algorithm based on TLS validated experimentally for CHBMLI based 3P3W active power filter using dspace controller. Based on simulation and experimental results it is found that the compensation process is fast, easy to realize and found effective to meet IEEE-519 standard recommendations on harmonics levels in nonlinear load conditions using anti-Hebbian based on TLS integrated with SIFLC. The simulated and experimental result indicates the efficacy and accuracy of the anti-Hebbian algorithm integrated with SIFLC controller.

CHAPTER 5: THREE PHASE FOUR WIRE REDUCED RATINGACTIVE POWER FILTER

In previous chapter 4, the performance of the five levels CHBMLI based active power filter is discussed. However, most of the distribution systems are 3P4W and active power filter proposed in chapter 4 may not viable such system, due to large size of active power filter. However, the active power filter size can be reduced by adding neutral compensator A 3P4W active power filter consists of three phase three wire five level CHBMLI active power filter (3P3W APF), zero sequence transformer and single phase active power filter is proposed to reduce rating of 3P4W APF. The reference current for tracking desired source current is using anti-Hebbian rule algorithm based on TLS integrated with single input fuzzy logic controller. The 3P3W APF compensates the current harmonics and reactive power requirement of the nonlinear load. The zero sequence transformer and the single phase APF (1P APF) are used to mitigate the neutral current. This proposed hybrid scheme significantly (3P4W-APF) reduces the volt-ampere rating of the APF and improves the performance under different utility voltage conditions. The simulation of the proposed 3P4W APF is carried out for different voltage conditions. Further, the MATLAB simulated response of 3P4W APF has been validated on prototype of the 3P4W-APF. The experimental result obtained from the prototype verifies effectiveness and viability of the 3P4W APF with proposed control scheme.

5.1 Introduction

In previous chapter, effort has been made to compensate customer generated current harmonics and reactive power requirement of the nonlinear load using anti-Hebbian algorithm integrated with single input fuzzy logic controller (SIFLC) for three phase three wire system. However, three phase four wire electrical distribution system are extensively used by small and medium scale power consumers such as domestic, commercial establishment, government organization and small scale industries etc. for supplying low voltage. In these locations, most of the loads have nonlinear input characteristics, which create the power quality problems such as current harmonics, reactive power and excessive neutral current. This adversely affects the other equipment performance connected to distribution system. The effect of power quality includes increase of distribution power system losses, malfunction of protection equipment, series/parallel resonance and overheating of transformer [12] etc.

Recently, many numbers of topologies have been reported in the literature to solve the power quality problem in three phase four wire distribution system. Three single phase active power filter bridges can reduce utility current harmonics and neutral current [14]. However, this topology requires more number of switches and complex to control the dc side capacitors voltages. The split capacitor and four pole active power filter topologies can

mitigate neutral current and the problem of current harmonics. However, these schemes were complicated in control and require large volt-ampere rating inverter [90].

In recent year, different transformer based topologies such as zigzag, star-delta; T-connected, Scott-connected and star/hexagon-connected have also been used to attenuate the neutral current on the utility sides due to the advantages of low cost, high reliability and simplified circuit connection. Among these topologies, zigzag transformer based approach is most commonly used and it requires least Volt-Ampere rating inverter. However, these configurations can attenuate the source neural current to a maximum extent but it will not be able to completely attenuate the same [207]. Further, their effectiveness of neutral current attenuation is dependent on unknown system impedance, installation location and utility voltage conditions [45, 50-57]. To overcome this problem, a reduced rating hybrid active power filter comprises of a zigzag-delta transformer, a 3P3W active power filter (APF) and a single-phase neutral compensator has been presented for the compensation of source neutral current and phase current harmonics, however, in this topology power factor and displacement factor deviates from unity [47, 48]. Also, the source phase fundamental currents were not made balanced. Other hybrid topologies consisting of a transformers and a single-phase neutral current compensator for neutral current attenuation have been proposed in the literature [49, 50, 54 203]. However, these schemes suffer from source phase current harmonics and unbalance. To alleviate the above limitations, in this paper a reduced rating 3P4W APF has been proposed. The proposed topology comprises of three phase three wire APF, zero sequence transformer and single phase APF.

In order to study the performance of the 3P4W APF computer simulation has been made under ideal, unbalanced, distorted and single phase load using MATLAB/Simulink® software. From the simulated response it is observed that the proposed topology with proposed control schemes can compensates the current harmonics and neutral current. In order to validate the simulation result, a downscaled prototype of 3P4W APF has been designed, fabricated and tested to verify the viability and effectiveness of the proposed control strategy.

5.2 Reduced rating 3P4W active power filter

Fig. 5.1 shows the arrangement of the 3P4W APF. A 3P3W APF is connected to point of common coupling for compensating positive and negative sequence component of harmonics requirement of nonlinear load is Fig. 5.2. The 3P3W APF draw or supply real power to keep dc side capacitor voltage constant. A zero transformer connected parallel to nonlinear load and single phase APF (here after it is referred as single phase neutral line compensator) is connected in series with the utility neutral conductor as shown in Fig. 5.3 . The advantage of connecting neutral line compensator in series is that, it considerably reduces the volt-ampere rating of the inverter due to the fact that only the non-zero sequence

current component of the neutral current will flow through neutral line compensator inverter, while zero sequence component of the current flows through zero sequence transformers.

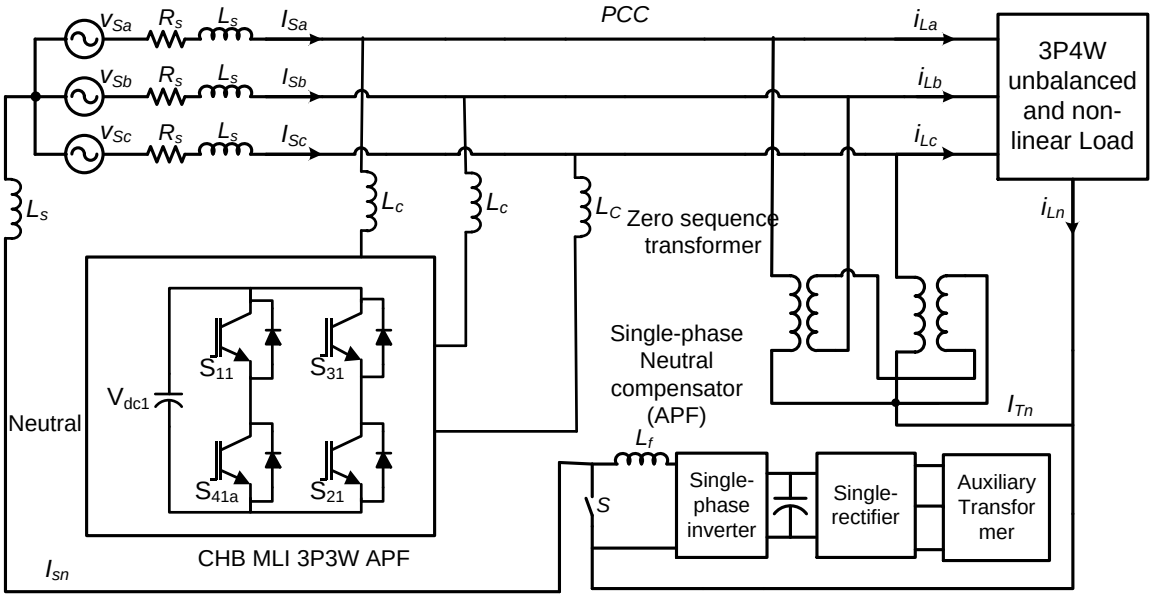


Fig. 5.1: Configuration of the three phase four wire active power filter (3P4W APF).

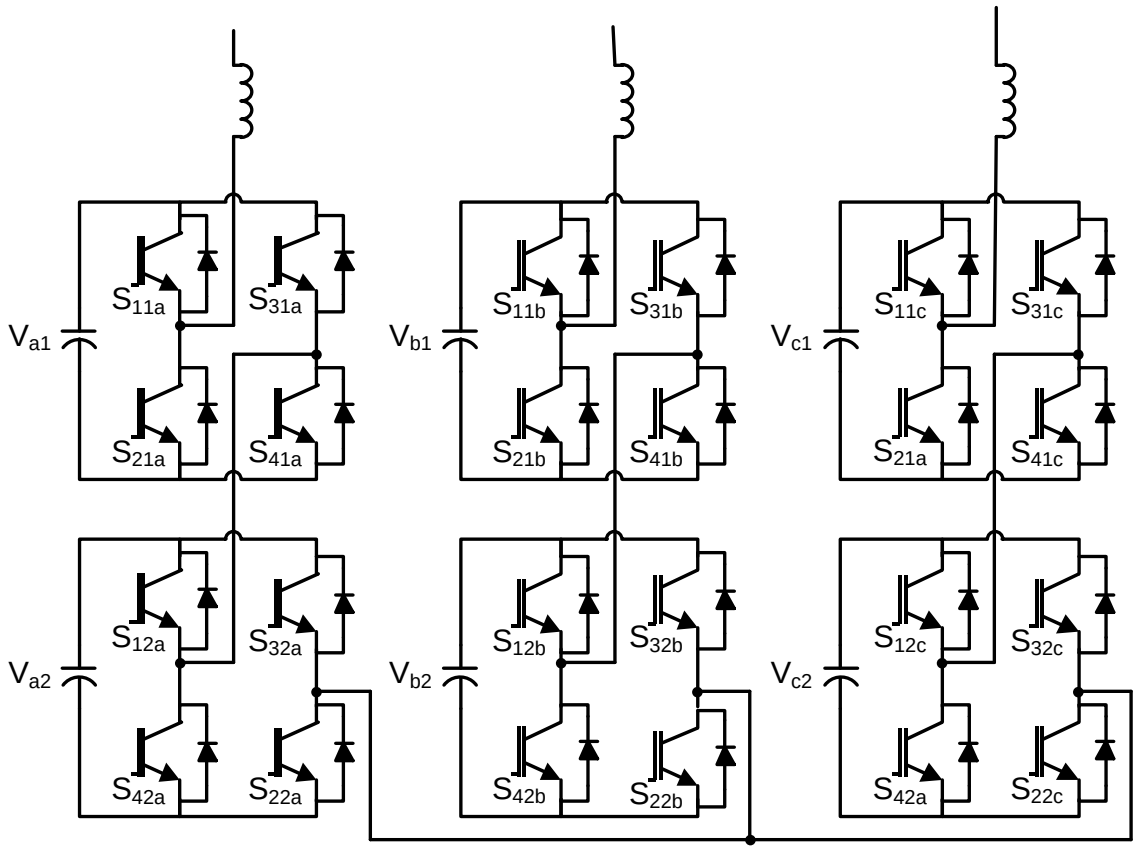


Fig. 5.2: Five level CHBMLI based APF.

The bypass switch (S) is placed in parallel with neutral line compensator and operates in case of faulty condition. The neutral line compensator injects the desired compensating current to attenuate the utility neutral line current and increase the effectiveness of neutral current circulation via zero sequence transformers to the load. The dc side capacitor voltage of the neutral line compensator is maintained using auxiliary low voltage regulated power supply.

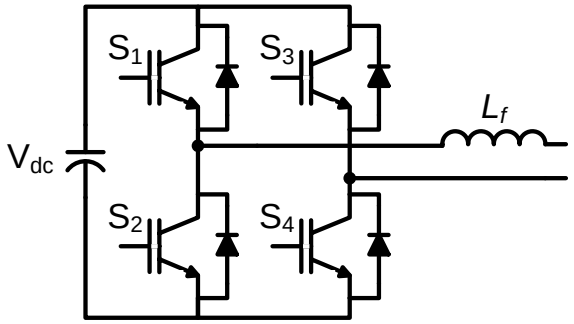


Fig. 5.3 . Single phase active power filter

5.3 Reference current generation for 3P3W APF

The reference control scheme is discussed in chapter 3 section 3.3 used in this chapter for controlling 3P3W active power filter. The block diagram of the reference current generation is shown in Fig. 5.4 using anti-Hebbian based on TLS control scheme integrated with single input fuzzy logic controller. The detail discussion of the single input fuzzy logic controller is presented in chapter 4 and as shown Fig. 5.5.

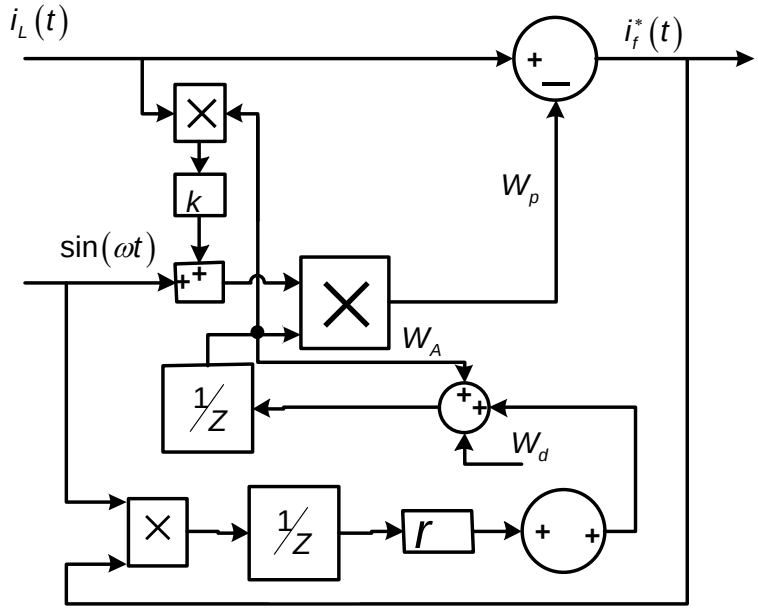


Fig. 5.4: Reference current generation for phase-a using anti-Hebbian learning rule.

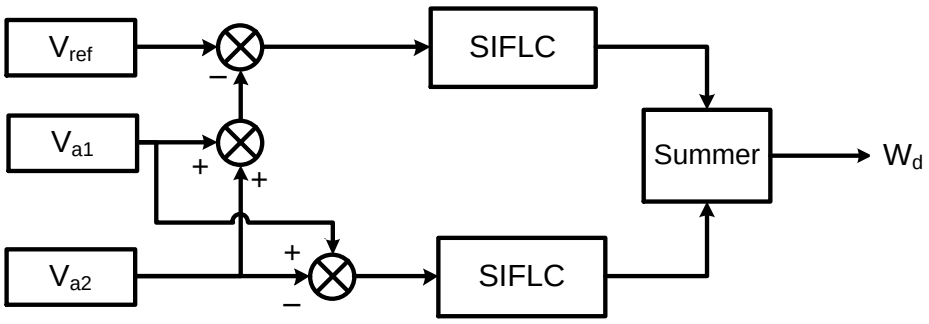


Fig. 5.5: dc voltage regulation using SIFLC controller for phase-a.

5.3.1 Neutral current attenuation under unbalanced/distorted voltage condition

The single phase neutral line current compensator is connected in series with three phase four wire distribution system neutral. It can be seen from Fig. 5.1, the utility neutral conductor and load neutral conductor is connected through single phase neutral line compensator. The zero sequence equivalent circuit of three phase four wire distribution system is shown in Fig. 5.6. The single phase neutral line compensator is supplied with regulated power supply to overcome the switching losses.

The single phase active power filter is controlled with pulse width modulation and its output voltage is represented as

$$v_c = g_{pwm} v_m(t) \tag{5.1}$$

Where g_{pwm} the gain of the single phase active power is filter, and $v_m(t)$ is the modulation signal. The gain of the single phase APF can be denoted as

$$g_{pwm} = V_{dc} \big/ V_{tri} \tag{5.2}$$

Where V_{dc} is the dc side capacitor voltage and V_{tri} is the amplitude of the triangular carrier signal. From the (19) it can be concluding that single phase APF is dependent voltage source. Hence, the single phase neutral compensator has to compensate the zero sequence components, it cannot respond to the positive and negative sequence components. The zero sequence equivalent circuit of the three phase four wire utility is shown in Fig.2. The quantities are shown in figure as follows: Z_{sn} −source neutral impedance; Z_{sp} − phase impedance; Z_{st} −impedance of the zero sequence transformer; v_c is the dependent voltage source of the single phase active power filter. The zero sequence equivalent circuit is power by two zero sequence sources V_{s0} and I_{L0} . Where V_{s0} is zero sequence source voltage generated due to the unbalanced utility voltages. Let V_{san} , V_{sbn} and V_{scn} be the three-phase unbalanced and/or distorted source voltages and I_{La} , I_{Lb} and I_{Lc} be the three-phase load

phase currents. The zero-sequence source voltage (V_{s0}) and zero-sequence load current (i_{L0}) are given as:

$$V_{s0} = \frac{1}{3}\left(V_{san} + V_{sbn} + V_{scn}\right) \tag{5.3}$$

$$I_{s0} = \frac{1}{3}\left(i_{La} + i_{Lb} + i_{Lc}\right) \tag{5.4}$$

The utility zero sequence current can be computed by applying superposition theorem

$$I_{s0} = \frac{Z_{st}}{\left(Z_{sp} + Z_{sn}\right) + Z_{st}} I_{L0} + \frac{1}{\left(Z_{sp} + Z_{sn}\right) + Z_{st}} V_{s0} \tag{5.5}$$

The utility neutral current can represented as

$$I_{sn} = 3I_{so} \tag{5.6}$$

The first term of (4.5) indicates that the magnitude of the utility side neutral current caused by I_{L0} will be reduced after applying the zero sequence transformers. If Z_{sn} is decreased or increased, utility neutral current further attenuated. The second term of (4.6) shows that due to the presence of zero-sequence supply voltage, the zero sequence transformer provides a path for the zero-sequence current flowing between the utility and the zero sequence transformer. However, the impedance of the utility system, the zero sequence transformer and the neutral conductor are very small in most of the distribution systems. This implies that a significant neutral current will be generated after applying the zero sequence transformers under the abnormal utility voltages.

From the above analysis it can be observed that, the zero sequence transformer can attenuate the utility neutral current to a maximum extent but their attenuation characteristics are dependent on their installation locations, the impedances of the transformers and utility voltage conditions as it is evident from (4.6). To alleviate this problem, in the proposed work single phase neutral line current compensator is incorporated to improve the attenuation characteristics of zero sequence transformer. The single phase neutral line current compensator is controlled by simply sensing the utility neutral current and comparing with zero value as shown in Fig. 5.7 The output of the single phase neutral line current compensator can be derived as $v_c = 3g_{pwm}g_F$ Where gain factor due control scheme. Therefore, the zero sequence current of the utility considering the effect of the single phase neutral line current compensator can be re-written as follows

$$I_{s0} = \frac{Z_{st}}{\left(Z_{sp} + Z_{sn}\right) + Z_{st} + 3g_{pwm}g_F} I_{L0} + \frac{1}{\left(Z_{sp} + Z_{sn}\right) + Z_{st} + 3g_{pwm}g_F} V_{s0} \tag{5.7}$$

From (5.7) it can conclude that the single phase active power filter act as a dynamic resister inserted in series with utility neutral.

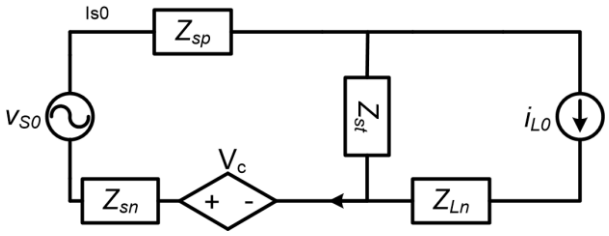


Fig. 5.6: Zero-sequence equivalent circuit of the 3P4W distribution system.

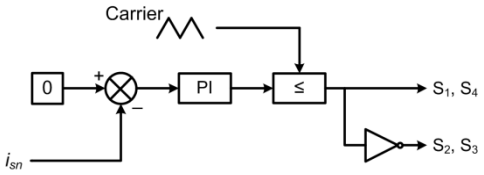


Fig. 5.7: Control block diagram for single phase active power filter.

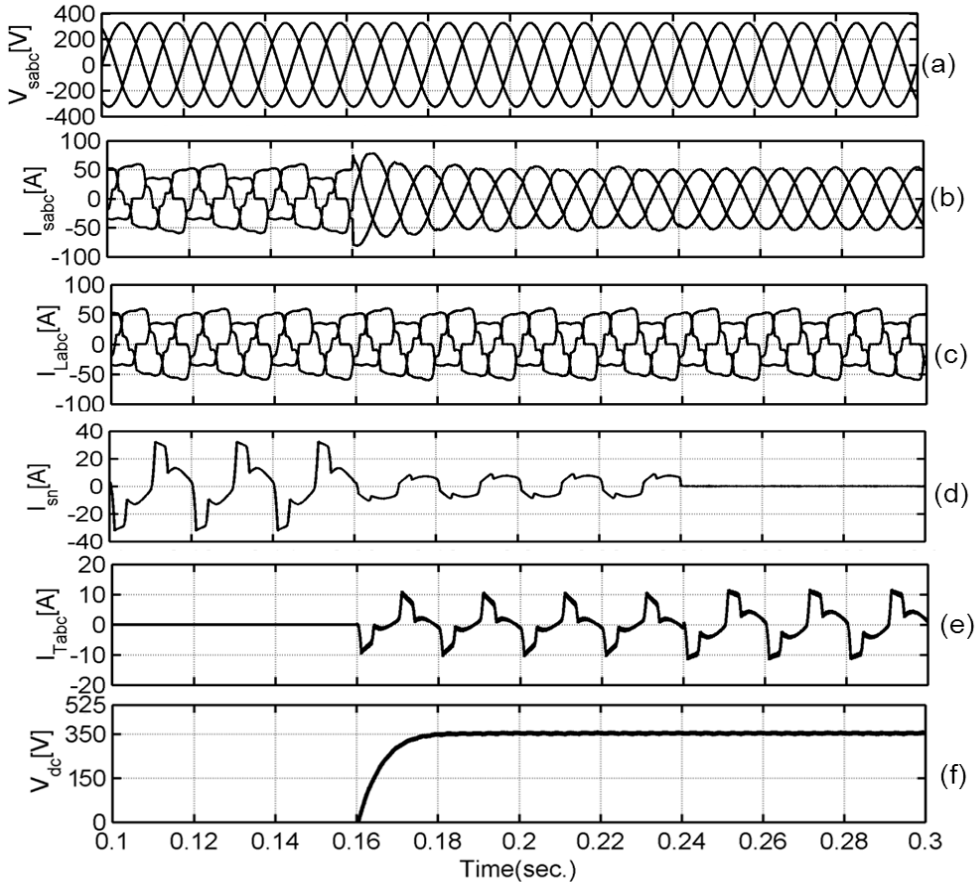
5.4 Simulation result

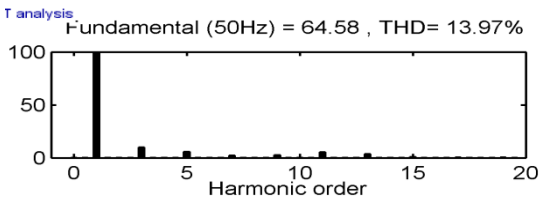
The simulated response of 3P4W APF is obtained using MATLAB/Simulink power system tool box. The proposed topology and control method has been simulated under different utility voltage conditions. The simulated responses of 3P4W APF with different utility voltages is presented below. The parameter used for simulation study is given in Table 5.1.

Table 5.1: The parameter used for simulation study

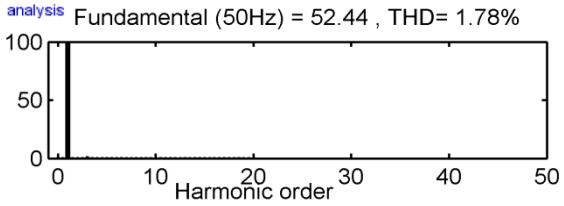
Parameter	**Value**
AC line voltage	Three-phase, three-wire, 440V, 50 Hz
Source impedance	R_s = 0.1 Ω, L_s = 0.1 mH
DC bus reference voltage	350 V for each capacitor
DC side capacitance	58 μF
Interfacing inductor of APF	L_c = 19 mH
Commutation inductance	L_{ac} = 2 mH
PWM switching frequency	2 kHz
Zero sequence transformer	Two single phase transformer of rating 10kVA, 230/230V,
Load	Three-phase uncontrolled rectifier, R_{dc} = 20 Ω, L_{dc} =16 mH; Two single phase uncontrolled rectifier, R_{dc} = 20 Ω, L_{dc} =16 mH;

5.4.1 Ideal utility voltage

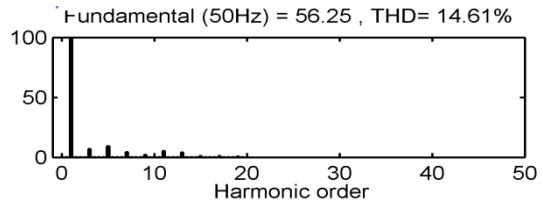




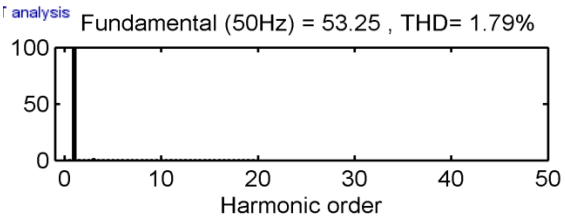
(g.1) phase-a load current THD spectra



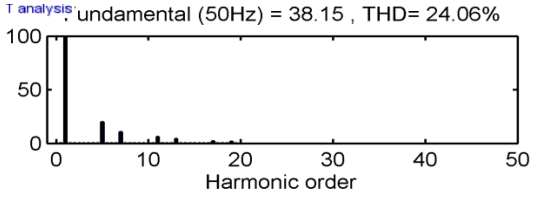
(h.1) phase-a source current THD spectra



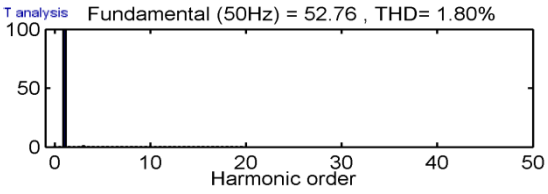
(g.2) phase-b load current THD spectra



(h.2) phase-b source current THD spectra



(g.3) phase-c load current THD spectra



(h.3) phase-b source current THD spectra

Fig. 5.8: Performances of 3P4W active power filter under balance utility voltage.

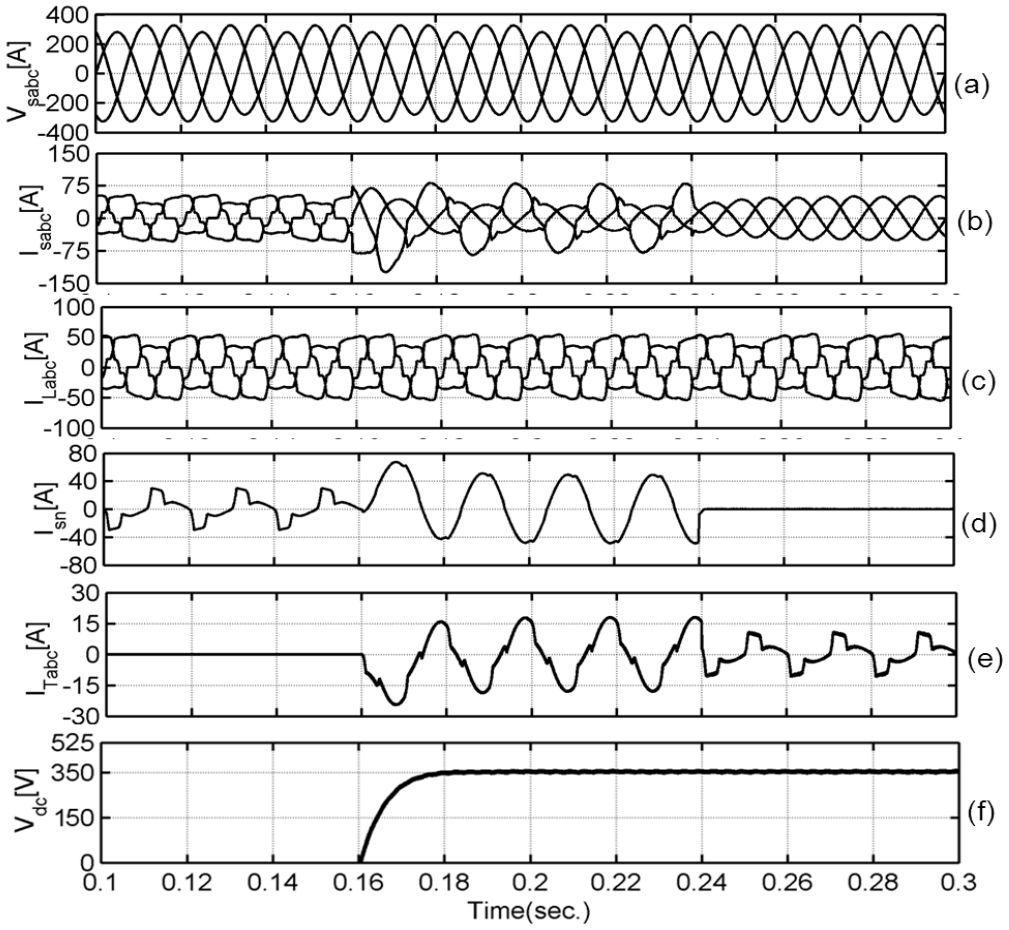
The simulated respose of 3P4W distribution system with 3P4W APF under ideal utility condition is shown in Fig. 5.8. The three phase four wire load consist of a three phase uncontrolled rectifeir and two single phase uncontrolled rectfier connected between the phase and neutral. The symbol used in various figures to represent the waveforms are as follow: source voltage–(V_{sabc}), source current–(I_{sabc}), load current–(I_{Labc}), source neutral current–(I_{sn}), current circulation in zero sequence transformer–(I_{Tabc}) and capacitor dc voltage–(V_{dc}). In order to study the performance of the 3P4W active power filter, the zero sequence transformer and 3P3W APF is connected at t=0.16 sec whereas the single phase APF is connected at t=0.24 sec. Before the operation of the active power filter the utility current is distorted, unbalanced and THDs for phase-a, phase-b and phase-c are found to be 13.91%, 14.61% and 24.06% respectively as shown in Fig. 5.8 (g) . It can be seen from Fig. 5.8 (b), when zero sequence transformer alone acting as neutral current compensator (switch closed (s)), it reduces the neutral current (I_{sn}) from 50A to 20A. Therefore, zero sequence transformer reduce the source neutral current to maximum extent but not completely as evident from Fig 5(d). At this instant utility current is nearly sinusoidal as seen in Fig. 5.8 (b). The source current THDs are 5.4% 6.7% and 5.1% for phase-a, phase-b and phase-c respectively. This indicates that presence of zero sequnece current in utitlity neutral current detoriates the compensation performance of the 3P3W APF.

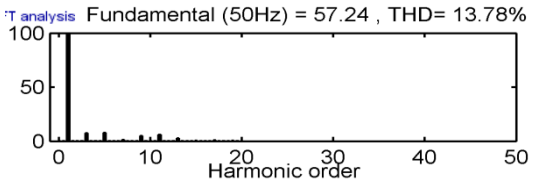
However, When neutral compensator switched-on at t=0.24 sec, the source neutral line current almost disapear due to the compensating current injected neutral line current compensator. The source currents tend to sinusoidal and balanced as shown in Fig. 5.8 (b). The compensated source current THDs are 1.78%, 1.79% and 1.80% for phase-a, phase-b and phase-c respectively as shown in Fig. 5.8 (h).

5.4.2 Unbalance utility voltage condition

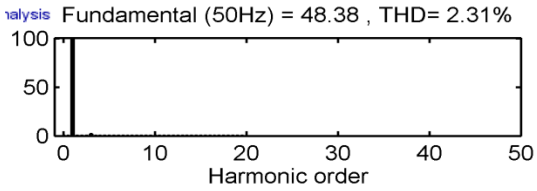
For ideal utility condition the amplitude of the voltage of each phase is same. However, the voltage unbalance may occur frequently in three phase four wire distribution system. Due to the supply voltage unbalance the zero sequence voltage is produced, which results in circulation zero sequence current between the source neutral conductor and zero sequence transformer. Fig. 5.9 shows the simulated response of 3P4W APF with 10% voltage amplitude unbalance condition for the proposed system.

To study the performance of the 3P4W active power filter, the zero sequence transformer and 3P3W APF is connected at t=0.16 sec whereas the single phase APF is connected at t=0.24 sec. As seen in Fig. 5.9(d), when zero sequence transformer alone act as source neutral compensator, the neutral current (I_{sn}) on utility side increase from 30A to 50A.

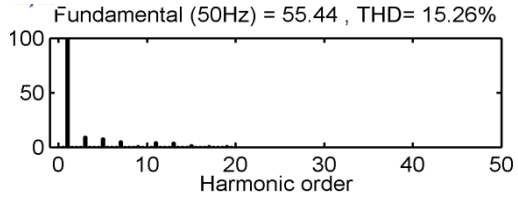




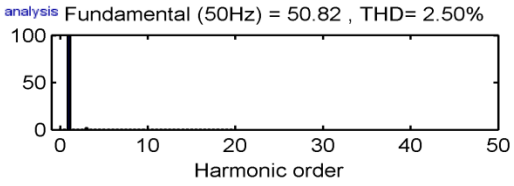
(g.1) phase-a load current THD spectrum.



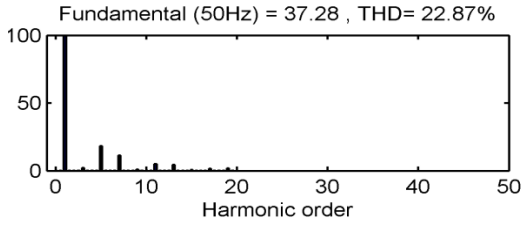
(h.1) phase-a source current THD spectrum.



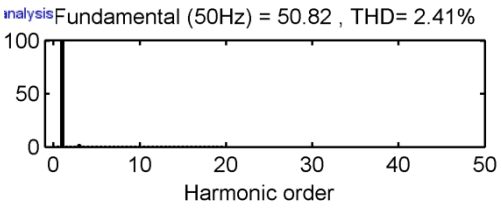
(g.2) phase-b load current THD spectrum.



(h.2) phase-b source current THD spectrum.



(g.3) phase-c load current THD spectra.



(h.3) phase-c source current THD spectrum.

Fig. 5.9. Performance of 3P4W APF under unbalance utility condition.

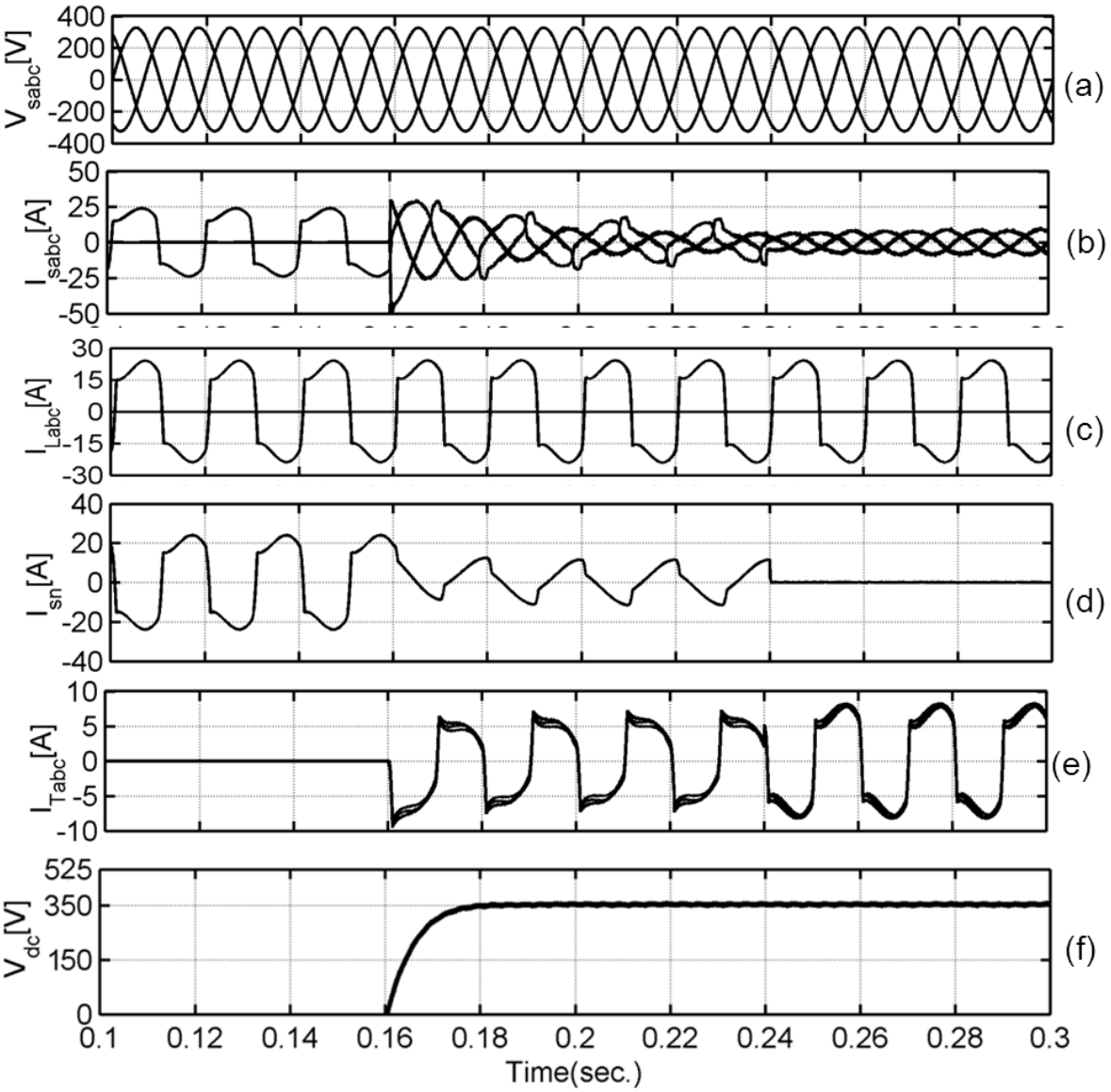
This large circulation of the zero sequence current is due to the presence of zero sequence voltage. The source currents are also increased and unbalanced. The THDs of the source currents are 42.5%, 38.5% and 41.5% for phase-a, phase-b and phase-c respectively. This source current is not compensated by the 3P3W APF due to the saturation of the controller.

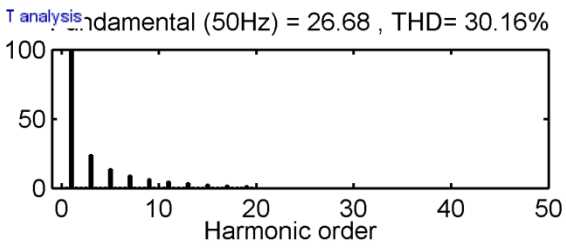
When single phase neutral line current compensator switched-on at t=0.24 sec., the source neutral line current completely disappear as seen in Fig. 5.9(d). And the source current tends to a sinusoidal and it is evident from Fig. 5.9(b). The THDs of the source phase current after compensation are 2.31%, 2.50% and 2.41% for phase-a, phase-b and phase-c respectively as evident from Fig. 5.9 (h).

5.4.3 Single phase load condition with ideal utility voltage

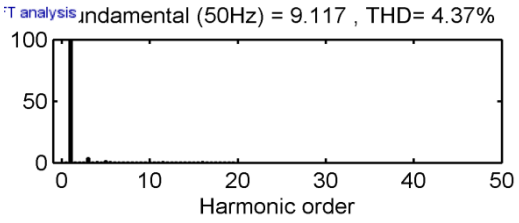
The simulated response of the three phase four wire distribution system with 3P4W APF under single phase condition is shown in Fig. 5.10. Before active power filters compensation RMS value of the source currents are 25A, 0A and 0A as it is evident from Fig. 5.10 (b). Then the source currents THD value are 26.6%, 0% and 0% for phase-a, phase-b and phase-c respectively as shown in Fig. 5.10 (g). When only zero sequence transformer and 3P3W APF are acting as compensators, the source neutral current is reduced from 25.0A to 10.5A and it is observed from Fig. 5.10 (d). The source current after compensation found to be unbalanced and THD values of source current for phase-a, phase-b and phase-c are 31.12%, 17.51% and 13.60% respectively.

When single phase neutral compensator is switched-on at t=0.24 sec., the source neutral line current completely disappear and it is evident from Fig. 5.10 (d). The source phase currents tends to sinusoidal and balanced (10.1A, 10.8A and 10.8A for phase-a, phase-b and phase-c respectively). The THD values of source currents are reduced to 4.57%, 4.37% and 4.56% for phase-a, phase-b and phase-c respectively as it can be observed from Fig. 5.10. The dc side capacitors voltage of the 3P3W APF is maintained at reference level as seen from Fig. 5.10 (f).

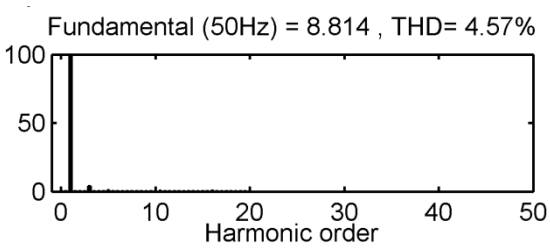




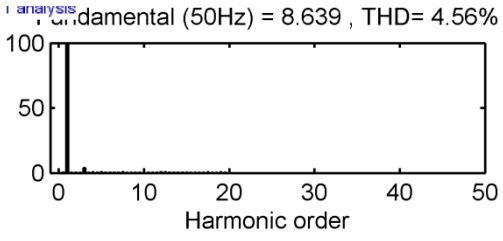
(g) phase-a load current THD spectrum.



(h.2) phase-b load current THD spectrum.



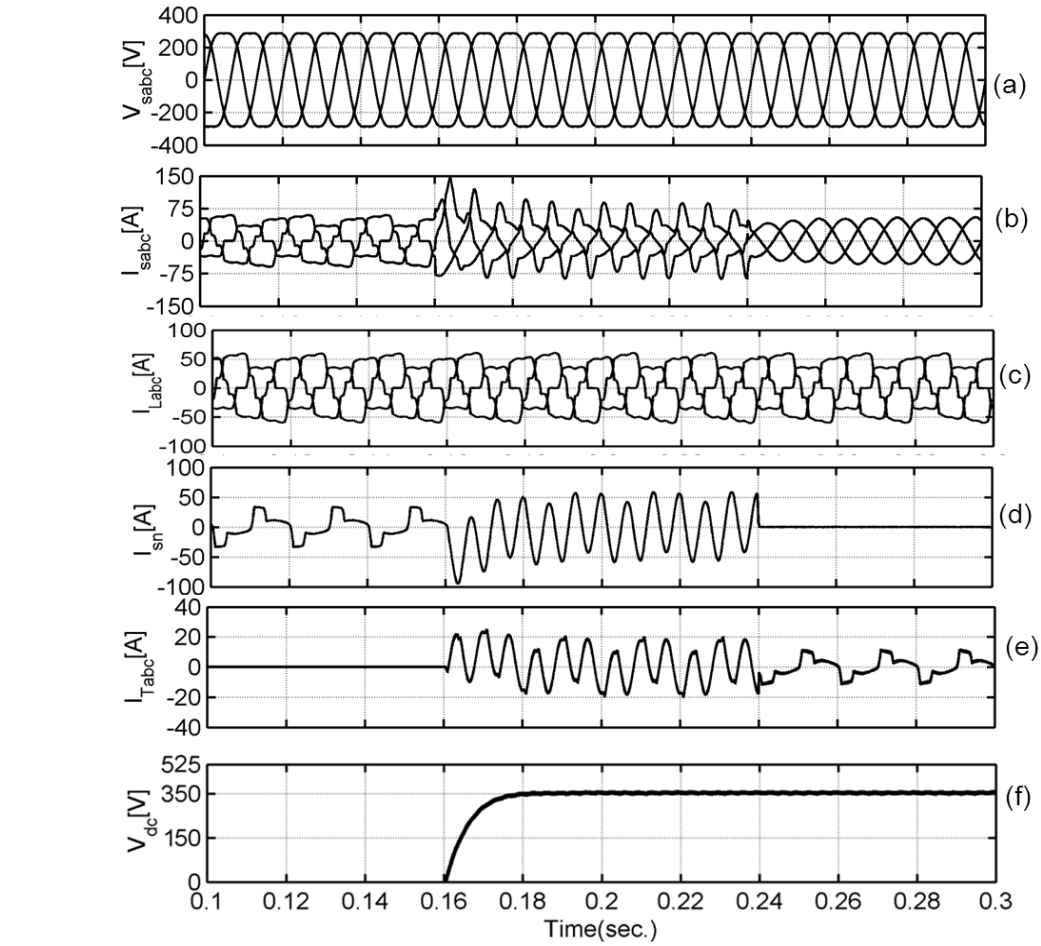
(h.1) phase-a load current THD spectrum.

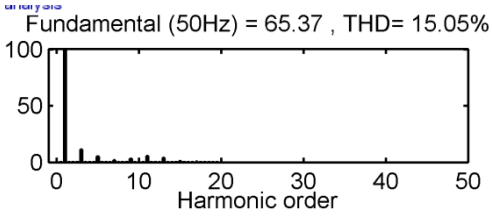


(h.3) phase-c load current THD spectrum.

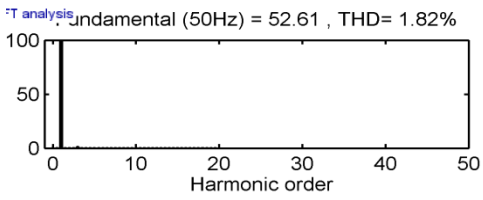
Fig. 5.10. Performance of 3P4WAPF under single phase load.

5.4.4 Distorted voltage conditions

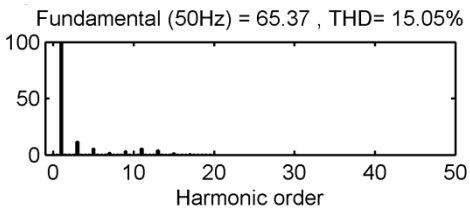




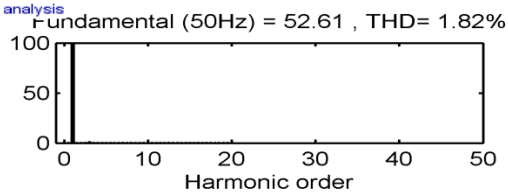
(g.1) phase-a load current THD spectrum.



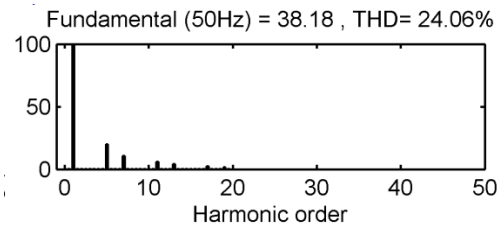
(h.1) phase-a source current THD spectrum.



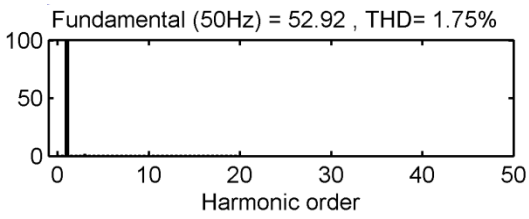
(g.2) phase-b load current THD spectrum.



(h.2) phase-b source current THD spectrum.



(g.3) phase-c load current THD spectrum.



(h.3) phase-c source current THD spectrum.

Fig. 5.11. Performance of 3P4W APF under distorted utility condition.

To verify the performance characteristics of the 3P4W APF under distorted utility voltage conditions, a 3% third order harmonic component is introduced in the utility voltages. Fig. 5.11 (a) shows the distorted voltage waveform under this condition.

It can be seen from Fig. 5.11 (b) that, before operation of 3P4W APF the RMS values of three-phase source current are 60.65 A, 60.2 A and 40.12 A and their corresponding THD values are 15.04%, 15.02% and 24.06% respectively for the three phases. At t = 0.15 sec when only zero sequence transformer and 3P3W APF are acting as compensators, the source neutral current is increased from 30.0 A to 50.6 A, due to the presence of zero-sequence voltage in the utility as shown in Fig. 5.11 (d). The source currents after compensation are observed to be unbalanced and the THD values are 41.12%, 67.51% and 63.60% for phase-a, phase-b and phase-c respectively. The increase of source current THDs is due to the circulation of large zero-sequence current between source neutral line and zero sequence transformer which is initiated by the zero-sequence voltage in the utility. This current is not compensated by the 3P3W APF due the saturation of controller.

When neutral compensator is switched-on at t=0.24 sec., the source neutral current completely disappear as seen in Fig. 5.11 (d) and the source currents tend to sinusoidal and balanced (60.24A, 60.4A and 60.8A for phase-a, phase-b and phase-c respectively) and are in synchronous with their respective voltage waveform. The THD values of source currents are reduced to 1.86%, 1.82% and 1.75% for phase-a, phase-b and phase-c respectively. After attenuation of neutral current with single phase neutral compensator, the current circulation in zero sequence transformer is also reduced as seen in Fig. 5.11 (e).

5.4.5 Comparison of 3P4W APF configurations

The Table 5.2 shows the advantages of the proposed 3P4W APF topology over the conventional schemes. The compensation characteristics of the schemes demonstrated in [13-15, 18] are dependents on the voltage conditions, installation location and impedance. But, with incorporation of the single-phase APF in series with utility neutral conductor, the compensation characteristics of the 3P4W APF is improved under various operating utility conditions (unbalance/distorted) and independent of utility voltage and impedance of the zero sequence transformer.

Table 5.2: Comparison of three-phase four-wire active power filters compensation characteristics.

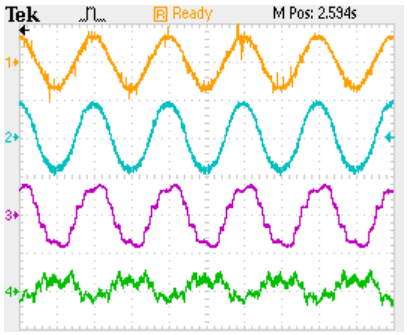
Characteristic	Type of configuration		
	Proposed3P4W-APF	3P3W APF and zigzag transformer based solution [51]	Three-phase, four-wire APF [80]
Operation under various voltage conditions	Improved	Abnormal rise of line current and neutral current	Degrades
Installation location	Not dependent	Dependent	Not dependent
Impedance of transformer	Not dependent	Dependent	Not dependent
Inserted series reactor in utility neutral (L_S)	Not required	Required	Not required

5.5 Experimental validation

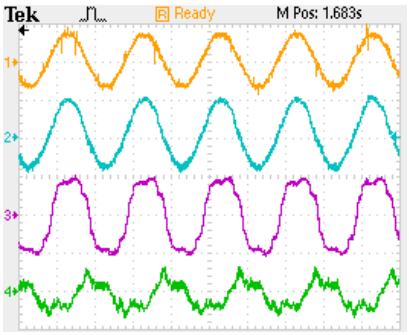
In order to verify the simulated response of the three phase four wire active filter a down- scaled laboratory prototype has been developed. The laboratory prototype of 3P4W APF consisting of zero sequence transformers, 3P3W APF and a single phase active power filter is shown in Fig. 5.1. The power circuits of three phase three wire (3P3W) APF and single phase APF are realized using IGBTs. The zero sequence transformer is realized by using two single phase transformer of rating 2kVA, 230/230V. The DC link voltage of the single phase neutral current compensator is maintained at 50V using regulated power supply.

5.5.1 Balance utility voltage

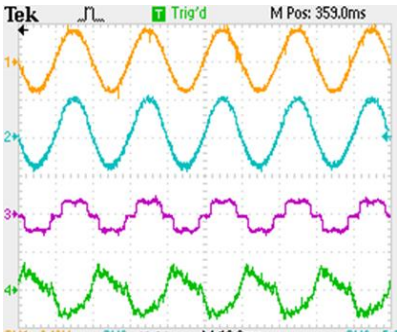
The compensation performance under balance voltage condition with 3P4W APF kept-on is shown Fig. 5.12. The source voltage, source current after compensation, load current and compensating currents for phase a, b and c in steady-state conditions are shown in Fig. 5.12 (a)-(c), respectively.



(a) phase-a waveforms

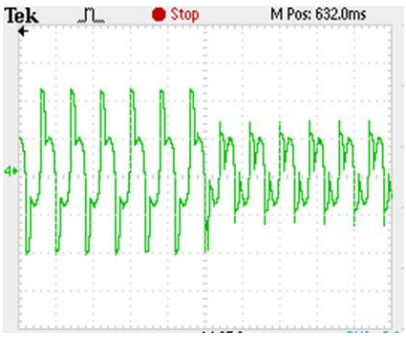


(b) phase-b waveforms



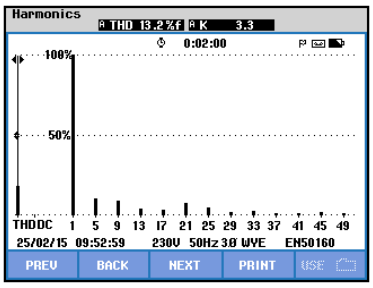
(c) phase-c waveforms

(d) Source neutral current before compensation

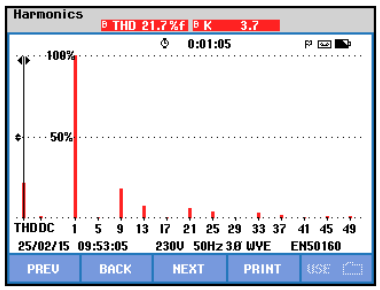


(e) Source neutral current after compensation with transformer

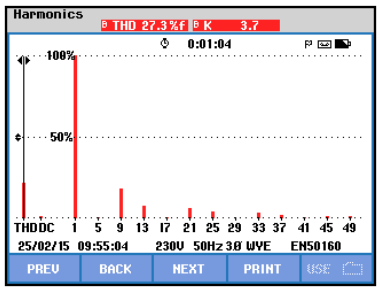
(f) Source neutral current after compensation with single phase neutral compensator



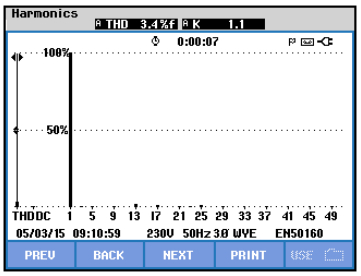
(g) Phase-a load current harmonics spectra.



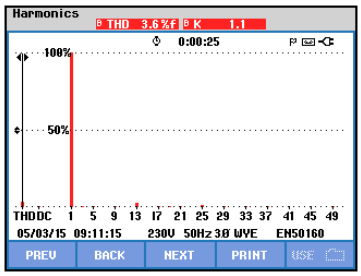
(h) Phase-b load current harmonics spectra.



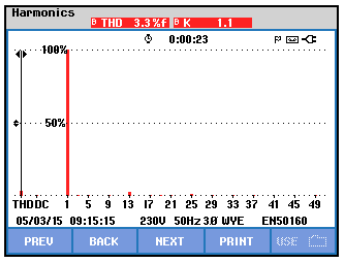
(i) Phase-c load current harmonics spectra.



(j) Phase-a source current harmonics spectra.



(k) Phase-b source current harmonics spectra.



(l) Phase-c source current harmonics spectra.

Fig. 5.12. Experimental waveform of 3P4W APF for balance utility voltage.

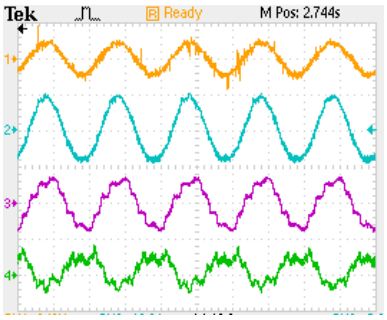
In these Fig. 5.12 (a)-(c), The different channels of waveforms are recognised as; Channel-1: source voltage (X-Axis: 5 ms/div. and Y-Axis: 100 V/div.); Channel- 2: source current after compensation (X-Axis: 10 ms/div. and Y-Axis: 5 A/div.); Channel-3: load current (X-Axis: 10 ms/div. and Y-Axis: 5 A/div.) and channel-4: compensating current injected by the active power filter. The three-phase four wire load which is comprises of three phase uncontrolled rectifier and two single phase uncontrolled rectifier, the load currents in channle-3 of Fig. 5.12 (a)-(c) are different shape. As seen from Fig. 5.12 (d) shows the source neutral line current before being compensated by neutral line current compensating circuit (X-Axis: 25 ms/div. and Y-Axis: 5 A/div.).

The source neutral line current after compensation with zero sequence transformer alone is shown in Fig. 5.12 (e) (X-Axis: 25 ms/div. and Y-Axis: 1 A/div.) As seen in Fig. 5.12 (e), after applying zero sequence transformer, the source neutral line current is reduced to great extent but not completely eliminated. As can be seen, after applying single-phase neutral compensator the source neutral line current almost disappear. The source neutral line current when neutral compensator is connected as shown in Fig. 5.12 (f) (X-Axis: 25 ms/div. and Y-Axis: 5 A/div.) it can be observed from Fig. 5.12, with the 3P4W APF the harmonics elimination reactive power compensation, load balancing, and neutral current compensation is realized. When neutral current compensator is switched-on, the source neutral line current almost disappear, the three phase source currents tends to sinusoidal and source supply balanced current. The experimental responses of 3P4W APF are almost identical to the simulated response.

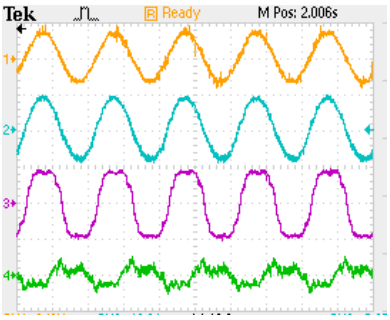
The THD spectra of load current for phases a, b and c are shown in Fig. 5.12 (g)–(i) respectively. Before compensation with 3P4W APF, the THDs of the load currents are 13.2%, 21.7% and 27.3% respectively. The THD spectra of source current after compensation for phases a, b and c are shown in Fig. 5.12, (j)–(l) respectively. The THDs of the compensated source currents are 3.4%, 3.6% and 3.3% respectively, which are well within the limits imposed by IEEE–519–1992 standards.

5.5.2 Unbalance utility voltage

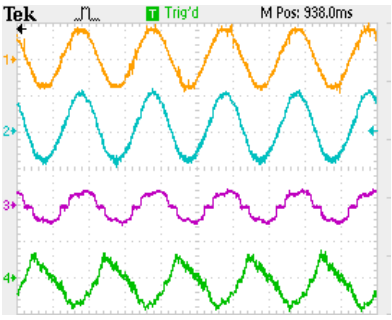
The proposed 3P4W APF has been tested for current harmonics elimination and source neutral current attenuation under unbalance utility voltage conditions is shown in Fig. 5.13. The source voltage, source current after compensation, load current and compensating currents for phase a, b and c in steady-state condition are shown in Fig. 5.13 (a)-(c), respectively.



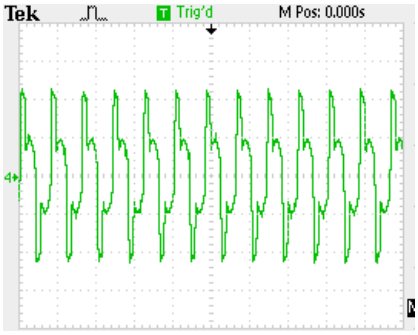
(a) phase-a waveforms



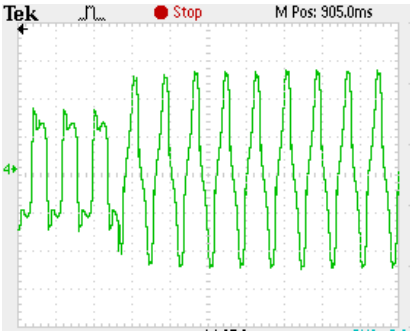
(b) phase-b waveforms



(c) phase-c waveforms

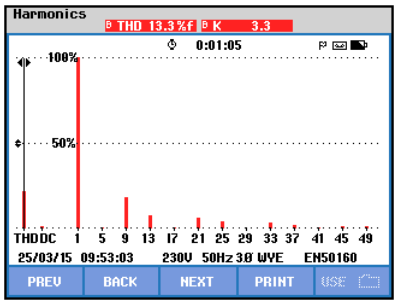


(d) source neutral current before compensation

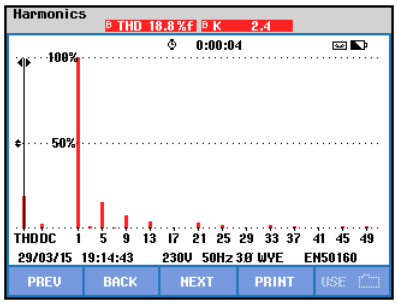


(e) Source neutral current after compensation with transformer

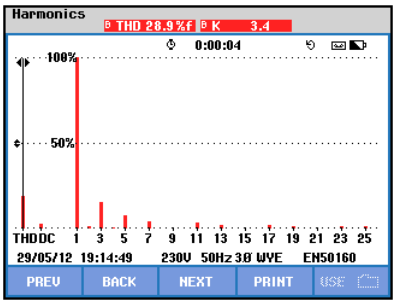
(f) Source neutral current after compensation with single phase neutral compensator



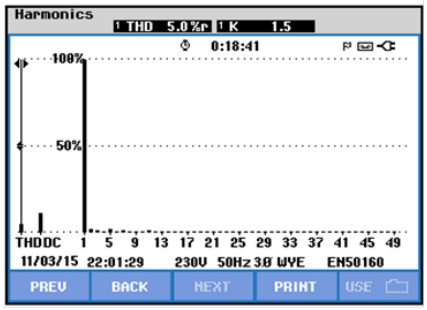
(g) Phase-a load current harmonics spectrum.



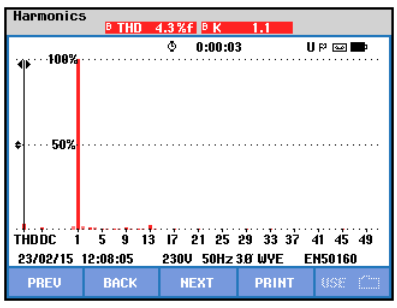
(h) Phase-b load current harmonics spectra.



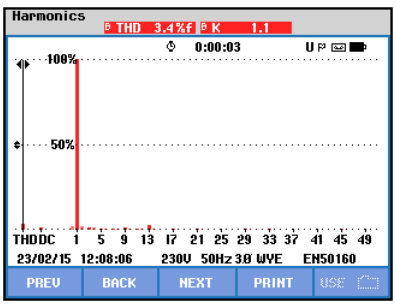
(i) Phase-b load current harmonics spectra.



(j) Phase-a source current harmonics spectra.



(k) Phase-b source current harmonics spectra.



(l) Phase-c source current harmonics spectra.

Fig. 5.13. Experimental waveform of 3P4W APF for unbalance utility voltage.

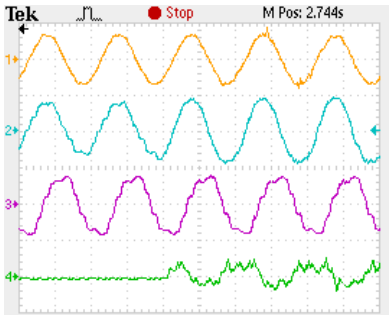
In these Fig. 5.13(a)-(c), the different digital oscilloscope channels of waveforms are recognised as; channel-1: source voltage (X-Axis: 5 ms/div. and Y-Axis: 100 V/div.); channel-2: source current after compensation (X-Axis: 10 ms/div. and Y-Axis: 5 A/div.); channel-3: load current (X-Axis: 10 ms/div. and Y-Axis: 5 A/div.) and channel-4: compensating current injected by the active power filter. Three-phase four wire load which is composed of three phase rectifier and two single phase rectifier, the load currents in channel-3 of Fig. 5.13 (a)-(c) are different shape. Fig. 5.13 (d) shows the source neutral current before compensation (X-Axis: 25 ms/div. and Y-Axis: 1 A/div.). The source neutral line current after applying zero sequence transformer with bypass switch (S) closed is shown in Fig. 5.13 (e) (X-Axis: 25 ms/div. and Y-Axis: 5 A/div.). As seen Fig. 5.13 (e), after applying zero sequence transformer, the neutral line current has increased on the source side.

The increase in the source neutral line current is due to the existence of 3^{rd} harmonics in utility voltage. However, after applying neutral current compensator (single phase APF), the source neutral line current almost disappears. The source neutral line current after being compensated by single phase neutral current compensator as shown in Fig. 5.13 (f) (X-Axis: 25 ms/div. and Y-Axis: 5 A/div.).

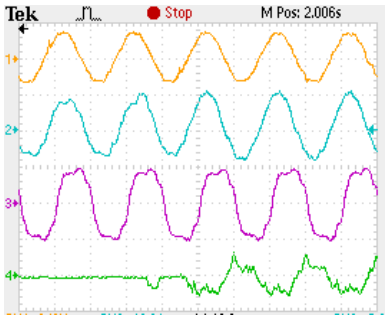
The THD spectra of source current before compensation with 3P4W APF for phases a, b and c are shown in Fig. 5.13 (g)–(i) respectively. Before compensation, the THD in the source currents in phases a, b and c is found to be 13.9%, 18.8% and 28.9% respectively. The THD spectra of source current after compensation with 3P4W APF for phases a, b and c are shown in Fig. 5.13 (j)–(l) respectively. The THDs of the compensated source currents are reduced to 5.0%, 4.3% and 3.4% respectively. Thus, the proposed active power filter with anti-Hebbian algorithm based on total least square integrated with single input fuzzy logic controller gives satisfactory under unbalanced condition.

5.5.3 Transients performance of the 3P4W APF

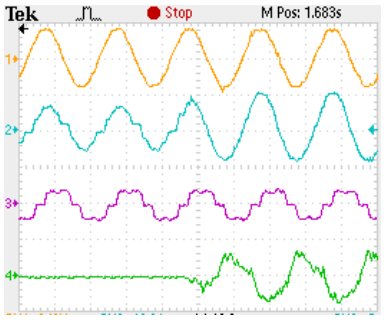
The transient performance of the 3P4W APF is shown in Fig. 5.14. Initially, zero sequence transformer alone operating as compensator, the 3P3W APF and single phase APF are from turning off to turning on. As evident from Fig. 5.14 (a)-(b), before compensation with 3P3W and single phase neutral compensator the source current is distorted. After compensation with 3P3W APF and single phase neutral compensator, source current tend to sinusoidal. It can be observed that the proposed 3P4W APF has good transient response for this condition Fig. 5.14 (e) shows experimental result for the conditions of 3P3W APF alone acting as current harmonic compensator and zero sequence transformer is from switched off to switched-on (the scale of channel-4: X-Axis: 25 ms/div. and Y-Axis: 5 A/div.).



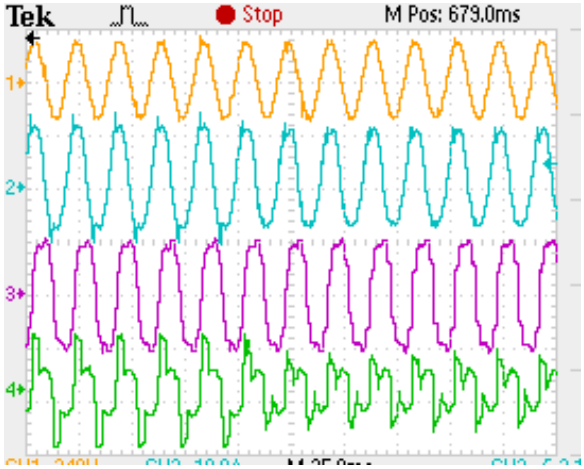
(a) phase-a waveforms



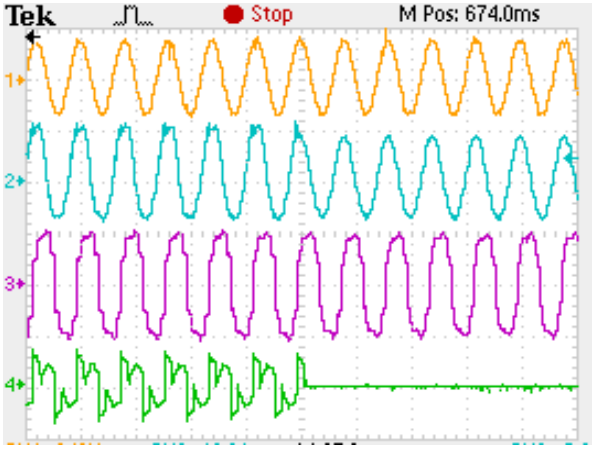
(b) phase-b waveforms



(c) phase-c waveforms



(e) Transient performance of 3P4W APF with Transformer acting as neutral compensator.



(f) Transient performance of 3P4W APF with Transformer and single phase neutral compensator acting as compensator

Fig. 5.14: Experimental waveform under transient condition.

The source current is distorted and contains zero sequence current. Further, as can be seen that the zero sequence current still exists in the source neutral line. Fig. 5.14 (f) shows experimental results for the condition of 3P3W APF and zero sequence transformers acting as compensator, while single phase APF is from switched-off to switched-on. As seen in Fig. 5.14 (f), the single phase neutral current completely attenuate neutral current and source current tend to sinusoidal. These experimental results show that the proposed filter has good transient response.

5.6 Comparison with Simulation Results

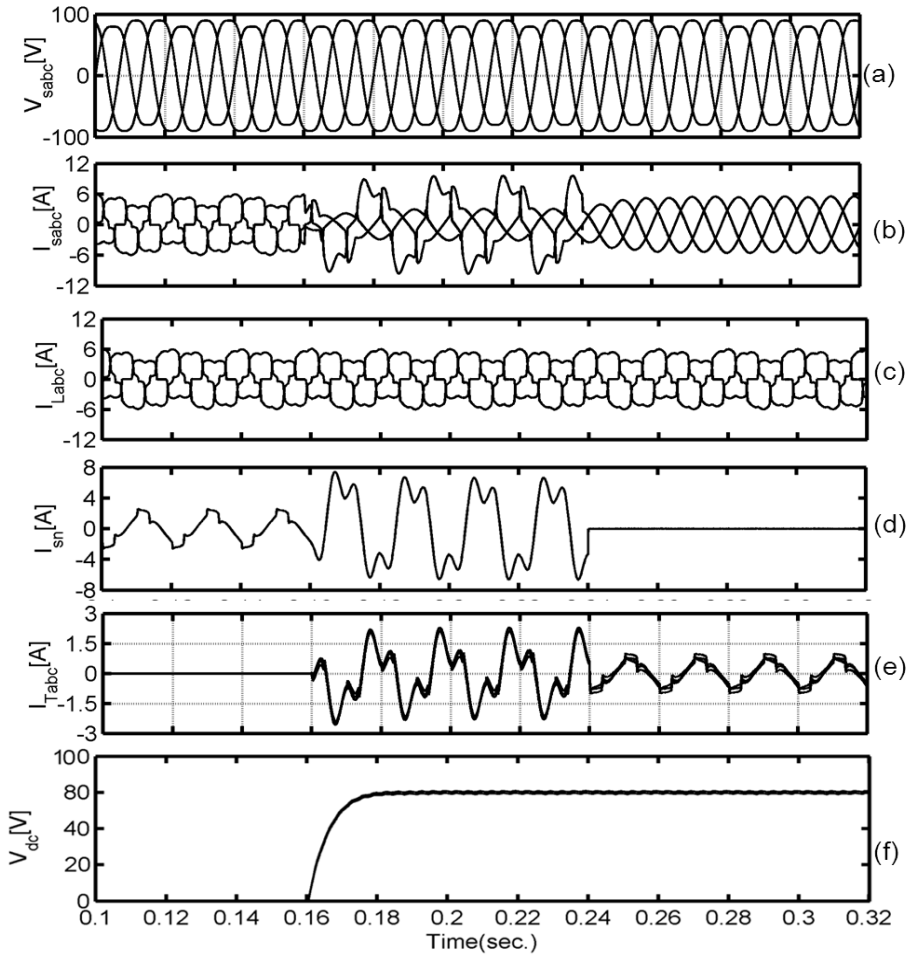
In the simulated response presented in section 5.4 , the 3P4W active power filter is tested at 400 V. However, due to the limitation involved in the development of prototype, the experimental studies are conducted at a reduced line voltage of 100 V. As the experimental studies are conducted at reduced system parameters, in order to validate the experimental results, the simulation is also carried out with reduced system parameters. The parameters used in the actual simulation and downscaled simulation studies are also given in Table 5.3.

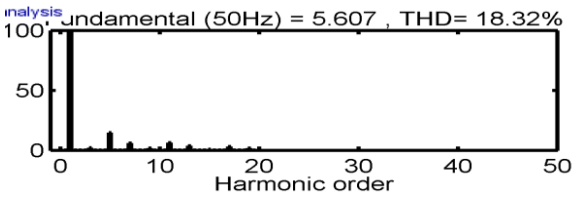
The downscaled simulation parameters are kept as same as possible to the experimental parameters as given in Table 5.3.

The simulated waveforms, load and source current harmonic spectra with nonlinear load composed of single-phase and three-phase uncontrolled rectifier with RL load under unbalanced/distorted utility voltage conditions are shown in Fig. 5.15 (a)-(h). As can be seen from Fig. 5.15, the simulated responses are almost identical with experimental results. Furthermore, in simulations results, the THDs in source current are reduced below 5%, but their values are slightly higher than their corresponding experimental values. These increases in %THD of source currents is due to the large value of sampling time for the simulation.

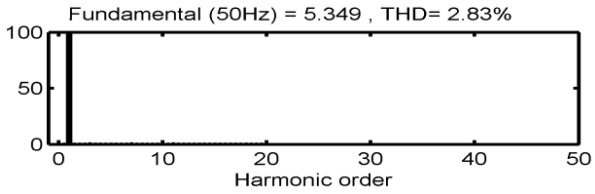
Table 5.3: The parameters used in the downscaled simulation studies.

Parameters	**Actual 3P4W APF**	**Downscaled 3P4W APF**
AC line parameters	Three-phase, four-wire, 400 V, 50 Hz	Three-phase, three-wire, 100 V, 50 Hz
DC bus voltage of APF	350 V (for each capacitor in the H-bridge cell)	80 V (for each capacitor in the H-bridge cell)
DC bus voltage of single-phase APF	50 V	50 V
DC bus capacitance of APF	58 μF (for each capacitor in the H-bridge cell)	1800 μF, 80 V (for each capacitor in the H-bridge cell)
APF interfacing inductor	Lc = 19 mH	L_c = 2.4 mH
Commutation inductance	L_{ac} = 1 mH	L_{ac} = 1 mH
Single-phase APF output inductor	L_f = 1.2 mH	L_f = 0.8mH
PWM switching frequency	2 kHz	2 kHz
PWM switching frequency for single-phase APF	1 kHz	1 kHz
Two single phase Transformers	10KVA, 230/230V;	2KVA, 230/230V;
Load	Three-phase uncontrolled rectifier with *RL* load; Two single uncontrolled rectifier with RL load	Three-phase uncontrolled rectifier with *RL* load Two single phase uncontrolled rectifier with *RL* load
Sampling time	T_s = 10e–6 sec.	T_s = 40e–6 sec.

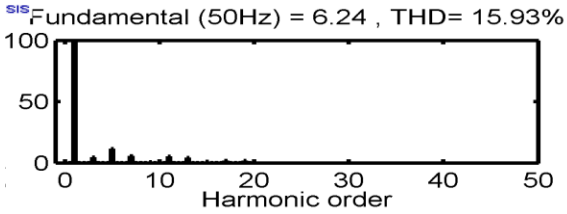




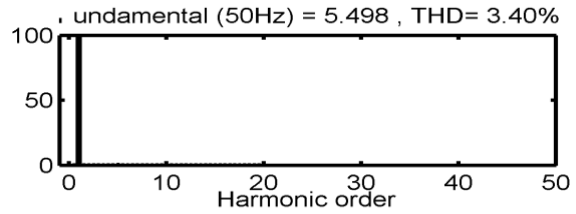
(g.1) phase-a load current THD spectrum.



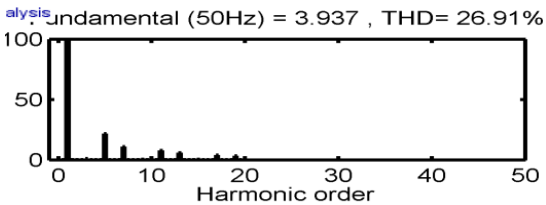
(h.1) phase-a source current THD spectrum.



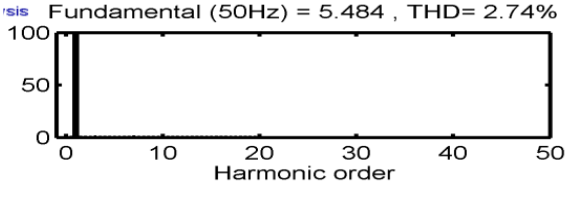
(g.2) phase-b load current THD spectrum.



(h.2) phase-b source current THD spectrum.



(g.3) phase-c load current THD spectrum.



(h.3) phase-c source current THD spectrum.

Fig. 5.15: The performance of 3P4W APF with downscaled simulation parameter under unbalanced/distorted utility voltage conditions.

Table 5.4: Comparison of experimental and downscaled simulation results under normal utility voltage conditions with 3P4W APF

Parameters	**Experimentation**			**Simulation**		
	phase *-a*	phase-*b*	phase-*c*	phase-*a*	phase-*b*	phase-*c*
Load current (A, rms)	2.6	3.8	1.5	2.711	4.128	1.433
Source current (A, rms)	3	3	3	2.601	2.642	2.595
%THD of load current	13.2%	21.7%	27.3%	17.08%	22.27%	29.61%
%THD of source current after compensation	3.4%	3.6%	3.3%	2.84%	3.74%	3.79%
Load neutral current (A, rms)	3.5 A			3.6 A		
Peak value of source neutral current when switch *S* is closed (A)	1.6 A			1.5 A		
Source neutral current when switch *S* is open (rms, A)	0.2 A			0.214 A		

Table 5.5: Comparison of experimental and downloaded simulation results under unbalanced/distorted utility voltage conditions 3P4W APF.

Parameters	**Experimentation**			**Simulation**		
	phase-*a*	phase-*b*	phase-*c*	phase-*a*	phase-*b*	phase-*c*
Load current (A, rms)	3.2	4.6	1.8	3.145	4.723	1.831
Source current (A, rms)	3.5	3.4	3.5	3.621	3.414	3.569
%THD of load current	13.9%	18.8%	28.9%	18.93%	15.93%	26.91%
%THD of source current after compensation	5.7%	4.3%	3.4%	2.83%	3.40%	2.74%
Load neutral current (A, peak)	3.6 A			3.65 A		
Peak value of source neutral current when switch *S* is closed (A)	5A			6 A		
Source neutral current when switch *S* is open (rms, A)	0.12 A			0.24 A		

The comparison of experimental and simulation results under normal and unbalanced/distorted utility voltage condition are given in Table 5.4 and Table 5.5 respectively. As can be seen from Table 5.4 and Table 5.5 the simulation results are almost identical with the experimental results. The increase in %THD of source currents is due to the large value of sampling time of the simulation. However, the anti-Hebbian algorithm integrated with SIFLC controller work effectively under unbalance/distorted voltage conditions.

5.7 Conclusion

This chapter presents a reduced rating three phase four wire hybrid active power filter for simultaneous compensation of load current harmonics, reactive power, and source neutral current. The main reason for reduction in the active power filter rating is that the separation of the zero-sequence currents from the positive and negative-sequence currents to be compensated. The performance of the proposed 3P4W APF is examined through MATLAB simulation and experimental studies. This 3P4W APF is independent of the impedance, installation location and utility voltage conditions. To control the 3P3W APF anti-Hebbian learning rule based on TLS integrated with SIFLC is proposed and implemented with dSPACE1104 R&D controller. From the simulation and experimental studies it is observed that proposed 3P4W APF can compensate current harmonics and source neutral current effectively under different utility voltage conditions.

CHAPTER 6: HYBRID 3P4W APF FOR SUPPRESSING HARMONICS AND NEUTRAL CURRENT IN 3P4W DISTRIBUTION SYSTEM

In this chapter, a new hybrid three phase four wire active power filter (3P4WAPF) is proposed for compensating current harmonics, reactive power and neutral current in three-phase four-wire distribution power systems (3P4W). The proposed hybrid 3P4W APF is consist of a neutral current compensator and a hybrid 3P3W APF. The hybrid APF, realized by a five level CHBMLI 3P3W APF and ac power capacitor, is used for compensating the nonzero-sequence currents harmonic in the 3P4W distribution system. The 3P3W APF is connected to the power capacitors and its volt-ampere rating can thus be reduced effectively. The neutral current compensator is connected between the power capacitors with interfacing inductors of the 3P3W APF and compensates the source neutral current in the 3P4W distribution system. With the major fundamental voltage of the utility dropping across the power capacitors of the 3P4W APF, the power rating of the source current compensator can thus be reduced. Hence, the proposed hybrid 3P4W APF can effectively reduce the volt-ampere rating of passive and active components of the system. A hardware prototype is developed to verify the performance characteristics of the proposed 3P4W APF. Experimental results show that the proposed hybrid 3P4W APF can compensate current harmonics, reactive power and neutral current.

6.1 Introduction

In previous chapter, a three phase four wire active power filter have been discussed for harmonics elimination, reactive power compensation, load balancing and neutral current compensation. The reference current estimated using anti-Hebbian algorithm based on TLS integrated with SIFLC. The neural network based control schemes extract the distortion free voltage signal and estimates the reference current. However, dc side capacitors voltages' rating largely influences the compensation performance of an active power filter. In general, the dc side voltage for the active power filter has much higher value than the peak value of the line-to-neutral voltage. This is done in order to ensure a proper compensation at the peak of the source voltage. The primary condition for harmonics elimination and reactive power compensation is that the magnitude of reference dc side capacitor voltage should be higher than the peak voltage at the point of common coupling [52-57].

Recently, many numbers of topologies of the three phase four wires APF has been proposed in literature [80, 188] for compensation of current harmonics, reactive power and neutral current at higher dc side capacitors voltages. The use of three single phase bridge converter can compensates the current harmonics, reactive power and neutral. But, this topology requires more number of switches and dc side capacitor voltage is 1.414 times the phase to neutral voltage for distortion free compensation of source current harmonics and neutral

current. Other, three phase four wire topologies based on split capacitor and four pole can compensates the current harmonics and neutral current to large extent. However, split capacitor topology suffers from voltage unbalancing and the four pole topology requires more number of switches. The dc side capacitor voltages for both the topologies is 2.815 and 2.45 times line to neutral voltage of system respectively, for effective compensation current harmonics, reactive power and neutral current. With the high value of dc side capacitor, the voltage-ampere rating of voltage source inverter increases, which is in turn, make system bulky and costly. The switching losses and switching stresses are also increased.

In literature few attempts have been made to reduce the dc side capacitor voltage of the active power filter. A reduced rating hybrid active power filter has been demonstrated in [205] and [206] for motor drive application. In [204] reduced rating hybrid APF has been proposed for reactive power compensation and neutral current elimination. But, topology suffers from dc side capacitor unbalancing problem.

To alleviate the above limitation, in this paper, a new 3P4W APF topology with reduced rating is proposed. The proposed topology composed of 3P3W APF, neutral compensator and power capacitor with interfacing inductor. The power capacitor enables reduction in dc side capacitor voltage and simultaneously compensating the reactive power requirement of the nonlinear load. In order to study the performance of the 3P4W APF computer simulation has been made under ideal, unbalanced, distorted and single phase load using MATLAB/Simulink® software. From the simulated response it is observed that the proposed topology with proposed control schemes can compensates the current harmonics and neutral current. In order to validate the simulation result, a downscaled prototype of 3P4W APF has been designed, fabricated and tested to verify the viability and effectiveness of the proposed scheme.

6.2 Configuration of the 3P4W APF

Fig. 6.1 shows, the topology of the proposed three phase four wire active power filter. The proposed topology consists of the hybrid three phase three wire active power filter (3P3P APF) and neutral current compensator. The neutral current compensator comprises of zero sequence transformer and single phase active power filter (APF). The 3P3W APF and neutral current compensator integrated to hybrid 3P3W APF. The integration of neutral current compensator, the hybrid 3P3W APF is need compensate only non-zero sequence current in three phase four wire distribution system. The ac series enable reduction of rating of three phase three wire active power filter and neutral current compensator due to voltage drop across series capacitor. The ac capacitor has the capability compensate the harmonics, reactive power requirement of load and also enable reduction in dc voltage of active power filter. The voltage rating of the zero sequence transformer is almost equal to the voltage of

interfacing inductors. The size of the zero sequence transformer also reduced in the proposed neutral current compensator. As seen from Fig. 6.1, the single phase active power filter is connected in series with source neutral conductor and zero sequence transformer directly connected to load neutral. The advantage of connecting single phase APF in series is that, it considerably reduces the volt-ampere rating of the inverter due to the fact that only the non-zero sequence current component of the neutral current will flow through single phase APF inverter, while zero sequence component of the current flows through zero sequence transformers. The dc side of the single phase active power filter supplied with diode bridge rectifier and single phase transformer. The bypass switch is placed in parallel to the single phase active power filter to protect in case of faulty conditions.

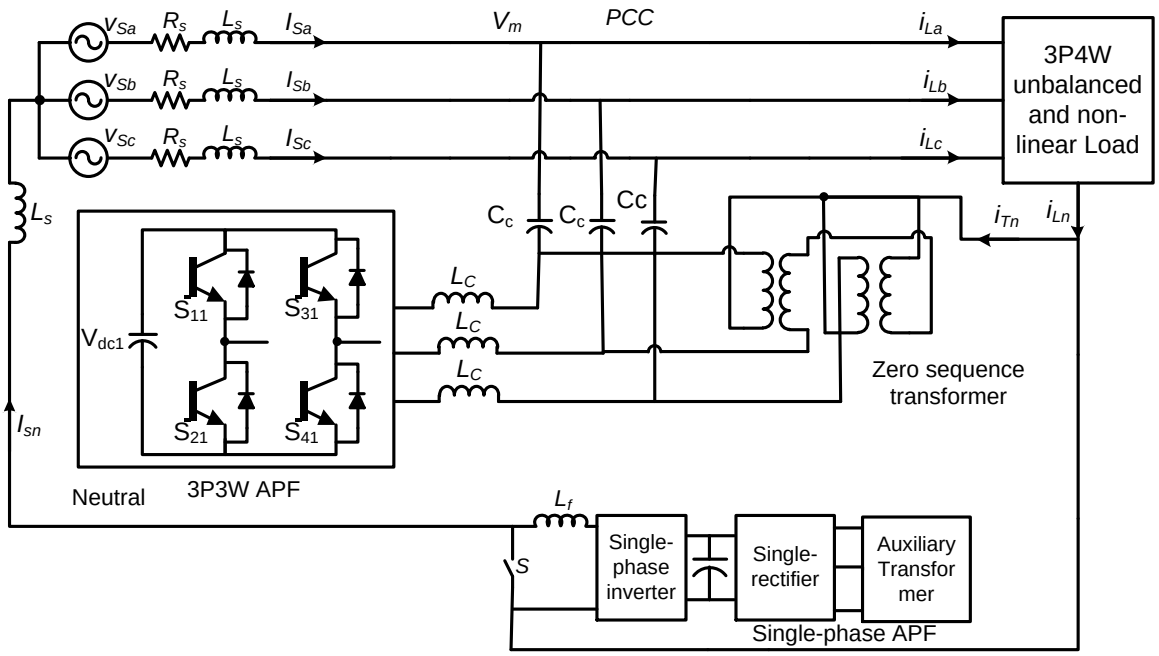


Fig. 6.1 A reduced rating hybrid APF for 3P4W distribution systems using transformer, 3P3W APF and single-phase APF.

6.3 Neutral current attenuation under unbalanced/distorted voltage condition

The zero sequence equivalent circuit of the proposed active power filter is shown in Fig. 6.2. Since the three-phase three wire active power filter, it will not appear in the zero-sequence equivalent circuit. Furthermore, the interfacing inductors of three phase three wire active power filters are not connected to the neutral path, and they will not appear in the zero-sequence equivalent circuit. The single phase active power filter is connected in series with three phase four wire distribution system neutral. It can be seen from Fig. 6.1, the utility neutral conductor and load neutral conductor is connected through single phase active power filter. The single phase active power filter is controlled with pulse width modulation and its output voltage is represented as

$$v_c = g_{pwm} v_m(t) \tag{6.1}$$

Where g_{pwm} the gain of the single phase active power is filter, and $v_m(t)$ is the modulation signal. The gain of the single phase APF can be denoted as

$$g_{pwm} = V_{dc} \big/ V_{tri} \tag{6.2}$$

Where V_{dc} is the dc side capacitor voltage and V_{tri} is the amplitude of the triangular carrier signal. From the (5.2) it can be concluding that single phase APF is dependent voltage source. The quantities are shown in figure as follows: Z_{sn} −source neutral impedance; Z_{sp} − phase impedance; Z_{zt} −impedance of the zero sequence transformer; Z_c - impedance due to capacitance; v_c is the dependent voltage source of the single phase active power filter. The zero sequence equivalent circuit is power by two zero sequence sources V_{s0} and I_{L0} . Where V_{s0} is zero sequence source voltage generated due to the unbalanced utility voltages. Let V_{san} , V_{sbn} and V_{scn} be the three-phase unbalanced and/or distorted source voltages and I_{La} , I_{Lb} and I_{Lc} be the three-phase load phase currents. The zero-sequence source voltage (V_{s0}) and zero-sequence load current (i_{L0}) are given as:

$$V_{s0} = \frac{1}{3}\left(V_{san} + V_{sbn} + V_{scn}\right) \tag{6.3}$$

$$I_{s0} = \frac{1}{3}\left(i_{La} + i_{Lb} + i_{Lc}\right) \tag{6.4}$$

The utility zero sequence current can be computed by applying superposition theorem

$$I_{s0} = \frac{Z_{zt} + Z_c}{\left(Z_{sp} + 3Z_{sn}\right) + Z_{zt} + 3g_{pwm}g_F} I_{L0} + \frac{1}{\left(Z_{sp} + 3Z_{sn}\right) + Z_{zt} + Z_c + 3g_{pwm}g_F} V_{s0} \tag{6.5}$$

The utility neutral current can represented as

$$I_{sn} = 3I_{so} \tag{6.6}$$

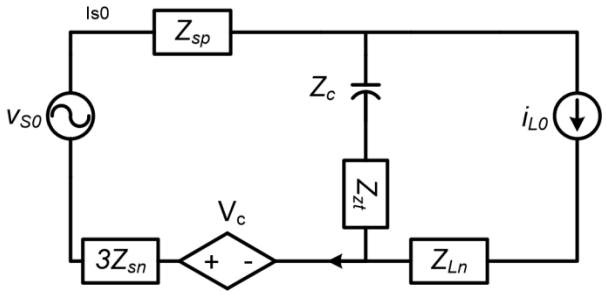


Fig. 6.2: Zero-sequence equivalent circuit.

6.3.1 Control of 3P3W APF

The detailed discussion of the reference current generation using anti-Hebbian based on total least square algorithm given in chapter 3 sections 3.3. The 3P3W active power filter is given in chapter 5 section 5.2.

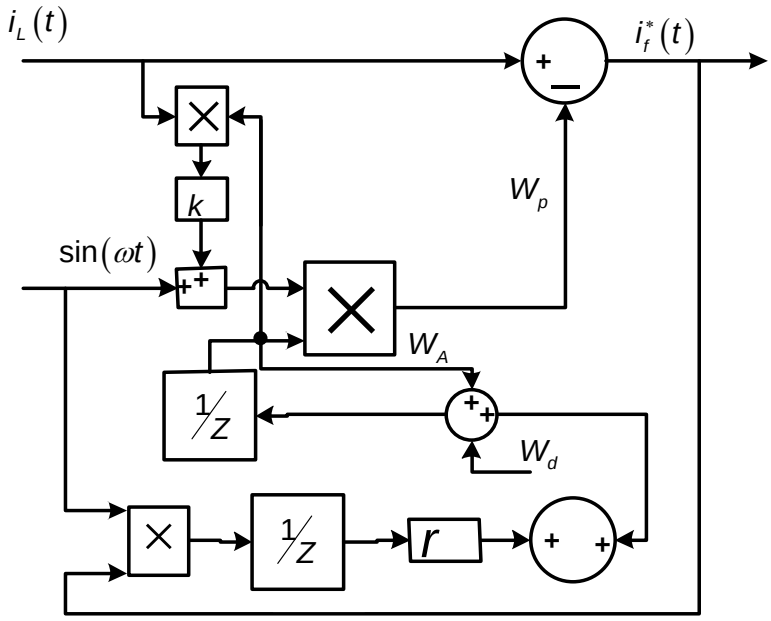


Fig. 6.3: reference current generation using anti-Hebbian based on total least square algorithm for phase-a.

6.3.2 DC voltage regulation

The dc side capacitor voltage regulation using single input fuzzy logic controller is shown Fig. 6.4. The detailed discussion is given in section

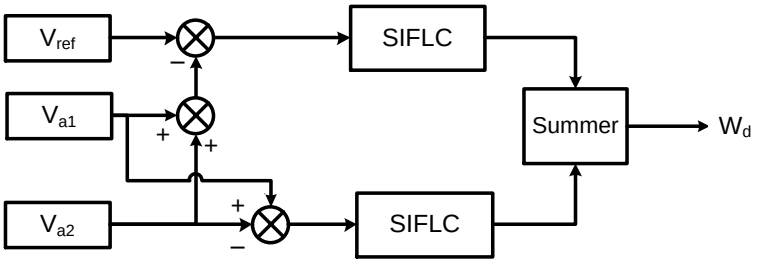


Fig. 6.4: dc voltage regulation using SIFLC controller for phase-a.

6.3.3 Control of single phase neutral compensator

The control of single phase neutral current compensator is given in chapter 5 section 5.3.1.

6.4 Modelling and simulation results

The complete power system model of the 3P4W active power filter has been developed in MATLAB/Simulink platform to study the performance of the system. The control

algorithms of hybrid APF is also modelled with MATLAB/Simulink® power system block sets.. The simulation model of the whole power system is shown in Fig. 6.5.

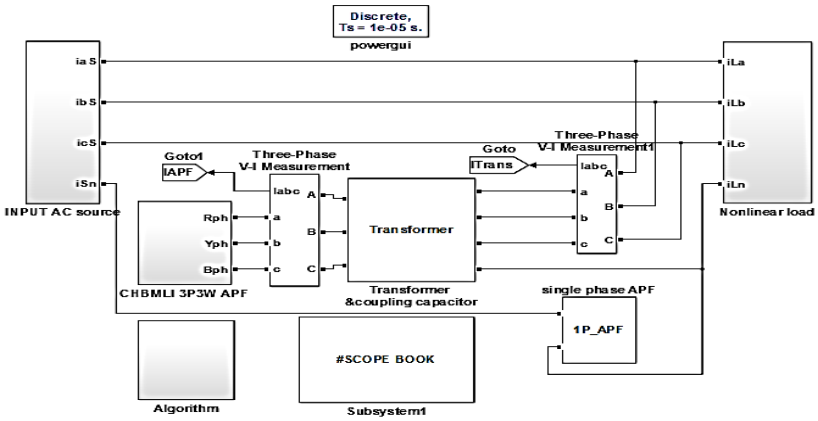


Fig. 6.5: MATLAB/Simulink model of the proposed system.

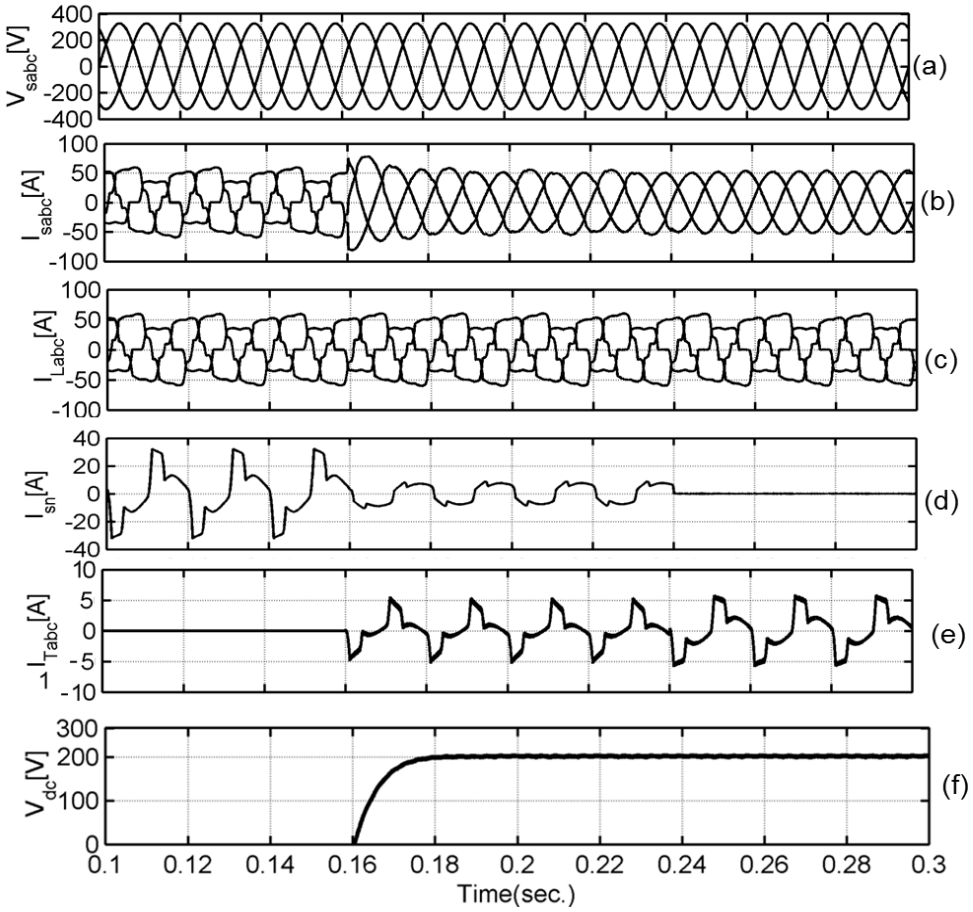
6.4.1 Simulation results

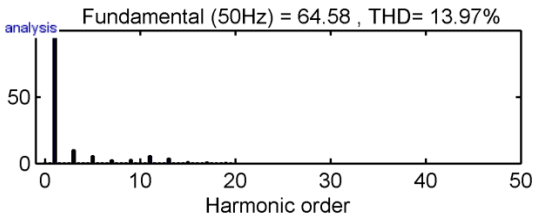
The performances of the proposed scheme has been studied for reactive power compensation, harmonics elimination and neutral current compensation under various operating conditions and are discussed below. The three-phase four wire load composed of three phase rectifier and two single phase uncontrolled rectifier and used as three phase four wire nonlinear load.

6.4.1.1 Under ideal utility condition

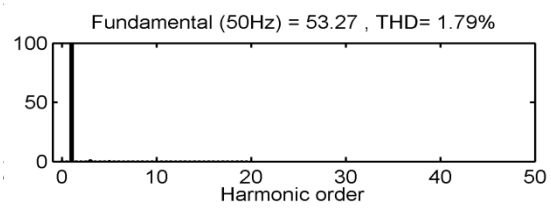
The simulation results of the three phases four wire distribution system with 3P4W active power filter under balance utility condition is shown in Fig. 6.6 The loads are three phase rectifier and two single rectifier loads, the load currents are 48.34, 48.25A and 20.22A for phase-a, phase-b and phase-c respectively. As seen in Fig. 6.6 (d), the utility neutral conductor contains a significant zero-sequence current (30.89 A RMS).

As seen from Fig. 6.6 (b), before active power filter operation, the source currents are 48.34, 48.24 and 20.22A for phase-a, phase-b and phase-c respectively and their corresponding THD values are 13.97%, 14.61 and 24.06% respectively for phase-a, phase-b and phase-c as shown in Fig. 6.6 (g). When the 3P3W and zero sequence transformer switched-on at t=0.16 sec. and acting as compensator, the source phase current are 42.5A, 50.34A and 40.13A for phase-a, phase-b and phase-c respectively. The source phase currents are unbalanced and their THDs values are 12.25%, 8.21% and 5.45% for phase-a, phase-b and phase-c respectively, as it can be observed from Fig. 6.6 (h). It can be seen From Fig. 6.6 (d), the utility neutral conductor still contains zero sequence current (10.52A). This indicates that the zero sequence transformer can attenuates neutral current to some extent and not completely to zero. When neutral current compensator is connected in series with utility neutral conductor, it inject the compensating current to completely attenuates neutral current to zero as shown in Fig. 6.6 (d).

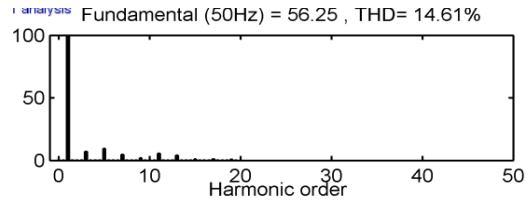




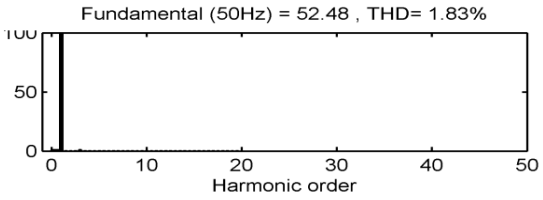
(g.1) phase-a load current THD spectra



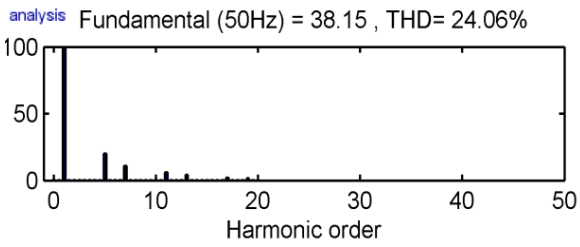
(h.1) phase-a source current THD spectra



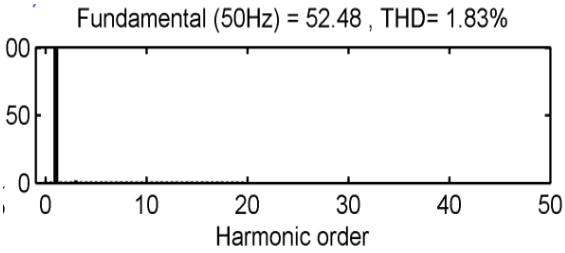
(g.2) phase-b load current THD spectra



(h.2) phase-b source current THD spectra



(g.3) phase-c load current THD spectra



(h.3) phase-c source current THD spectra

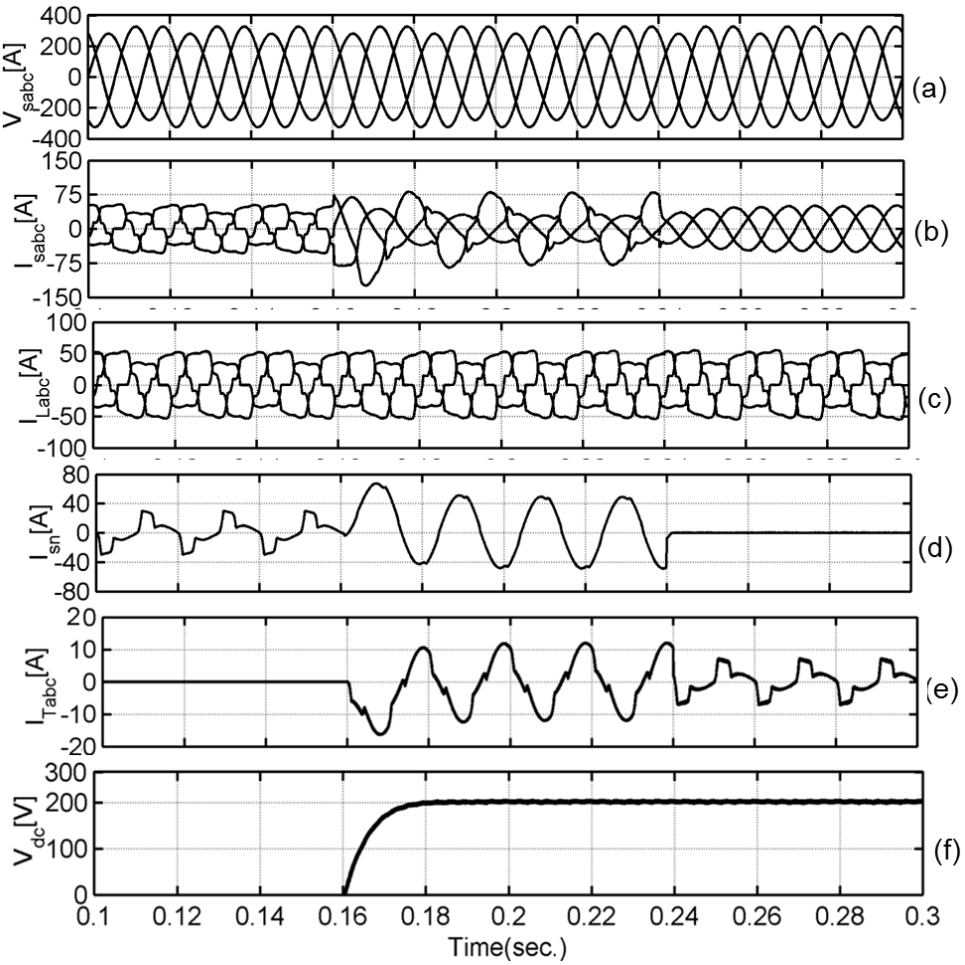
Fig. 6.6. Performance characteristics of 3P4W APF under balance voltage condition.

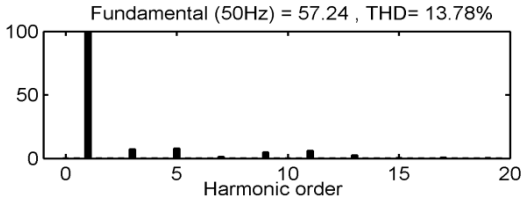
The source phase currents are tends to sinusoidal and balanced. The THDs values of source currents are 1.49%, 1.83% and 1.83% for phase-a, phase-b and phase-c respectively. This indicates that the 3P3W APF along with neutral suppressor circuit can balance the source currents. The dc capacitor voltage is regulated at set reference value as shown in Fig. 6.6 (f).

6.4.1.2 Unbalance utility voltage

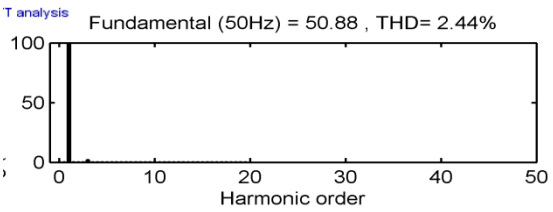
The performance of the three phase four active power filter under unbalanced utility voltages is shown in Fig. 6.7. Before, active power filter operation source current values are 48.24A, 48.08A and 20A for phase-a, phase-b and phase-c respectively as seen in Fig. 6.7 (b). Then the corresponding THDs values of source current are 13.78%, 22.25% and 15.26 as shown in Fig. 6.7 (g). When the 3P3W APF and zero sequence transformer switched-on at t=0.16sec and alone operating as compensator then there is significant increase in source current and it is observed from Fig. 6.7 (b). The increase of the source phase current is due to the presence of the zero sequence voltage. Because amplitude unbalance generates the significant amount of the zero sequence voltage, which result in circulation of zero sequence current between the zero sequence transformer and utility as it is evident from Fig. 6.7 (d). The source phase current after compensation found to be unbalanced and THDs values are 50.56%, 45.26% and 66. 24% for phase-a, phase-b and phase-c respectively.

When neutral current compensator switched-on at t=0.26sec the source neutral current becomes almost zero due to the compensation current injected by the neutral current compensator as shown in Fig. 6.7 (d). The source phase current waveforms tend to sinusoidal and in phase with respective utility voltage waveforms. Further, the values of source current THDs are 2.44%, 2.40% and 2.49% for phase-a phase-b and phase-c respectively as shown in Fig. 6.7 (h). As seen from Fig. 6.7 (e), the compensation with single phase neutral compensator also reduces the circulation in the zero sequence transformer. The dc side capacitors voltages are regulated at the set reference value with single input fuzzy logic controller.

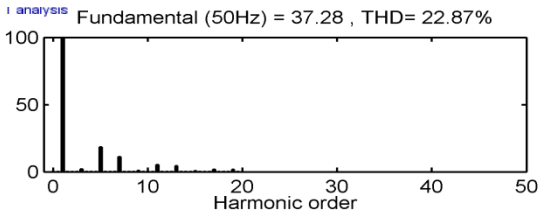




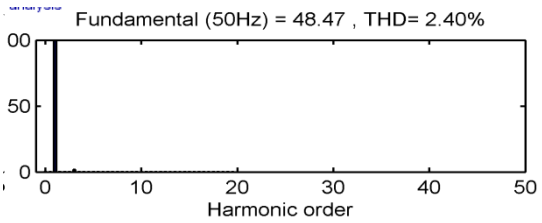
(g.1) phase-a load current THD spectra



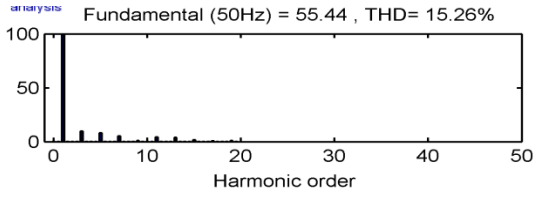
(h.1) phase-a source current THD spectra



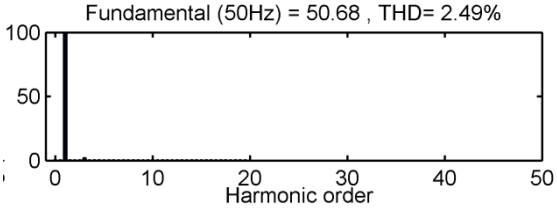
(g.2) Phase-b load current THD spectra



(h.2) phase-b source current THD spectra



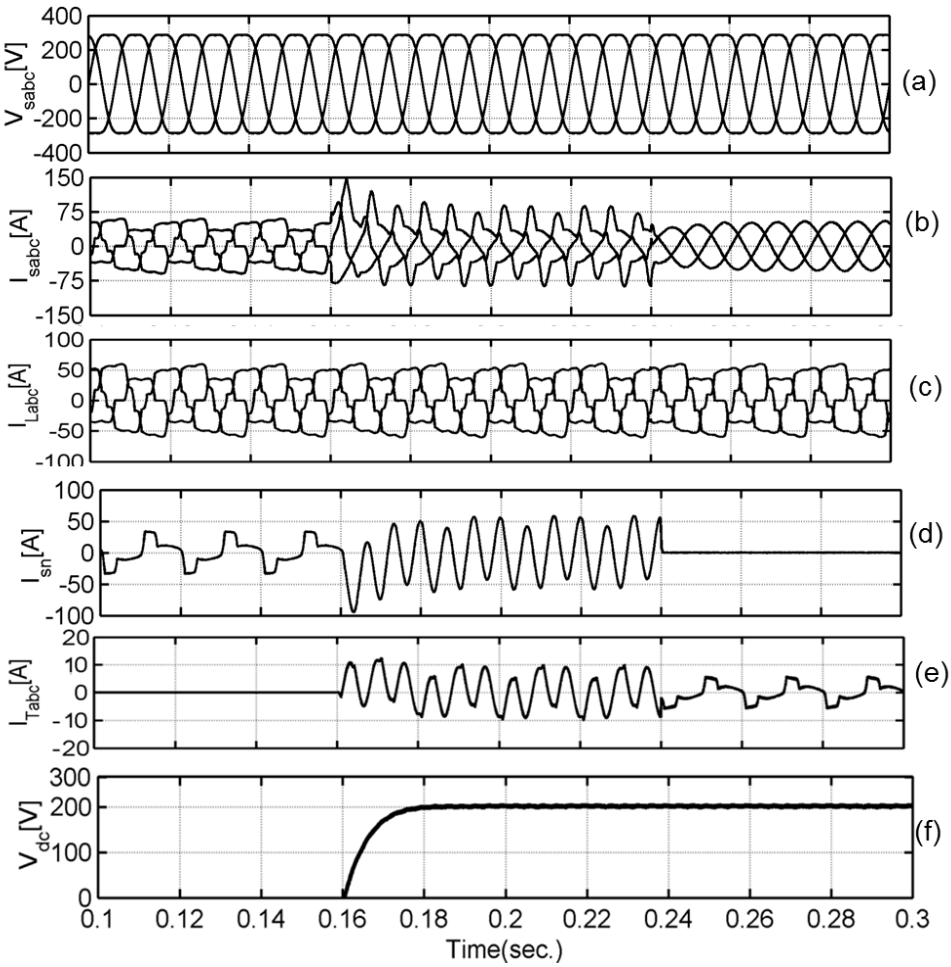
(g.3) phase-c load current THD spectra

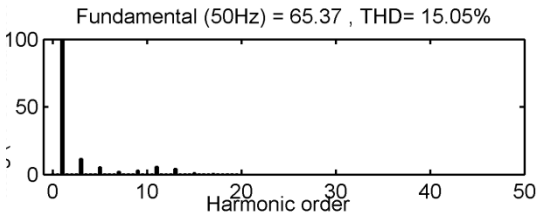


(h.3) phase-c source current THD spectra

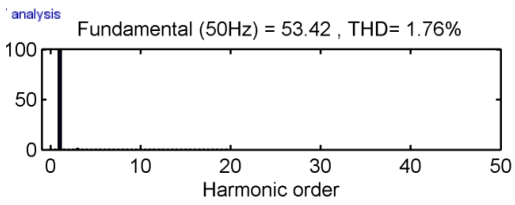
Fig. 6.7. Performance of 3P4W APF under unbalanced utility voltage condition.

6.4.1.3 Distorted voltage condition

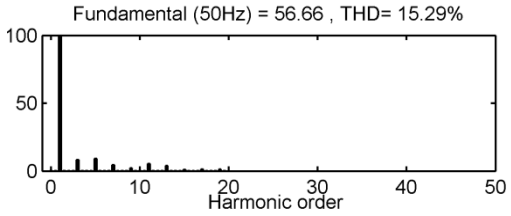




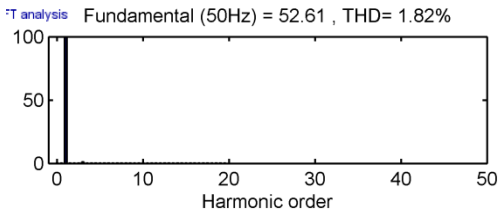
(g.1) phase-a load current THD spectra



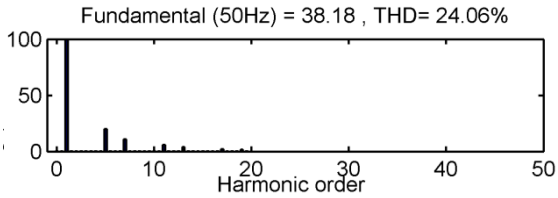
(h.1) phase-a load current THD spectra



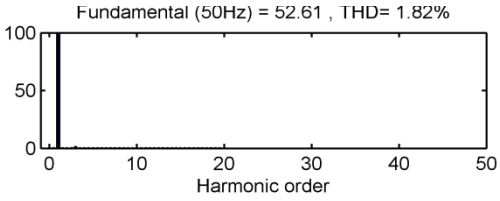
(g.2) phase-a load current THD spectra



(h.2) phase-b source current THD spectra



(g.3) phase-c load current THD spectra



(h.3) phase-c source current THD spectra

Fig. 6.8. Performance of 3P4W APF under distorted voltage condition.

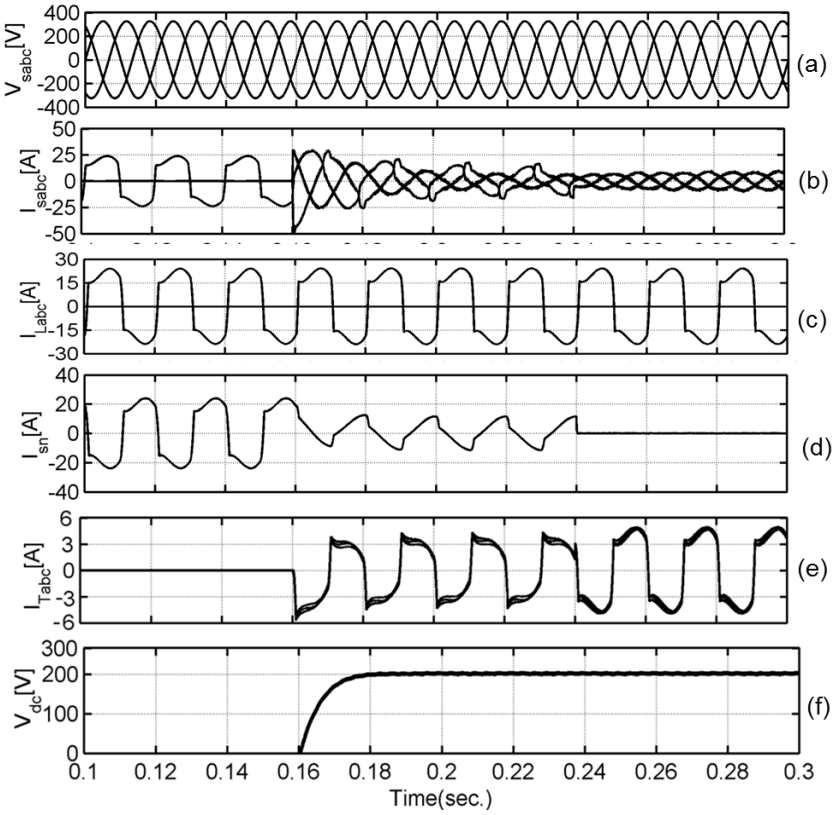
Fig. 6.8 shows performance of the hybrid power filter under distorted voltage condition. Due to the presence of the zero-sequence harmonics in the utility voltage can cause a substantial amount of zero sequence voltage. In order to realize the effect of distorted utility voltage on the 3P4W APF 10% of 3rd order harmonic and 5% of 5^{th} order harmonics component is introduced in the utility voltages. Because, 3^{rd} harmonics is zero sequence voltage which results in circulation of zero sequence current as per analysis seen in (6.5). The simulation results under this condition are shown in Fig. 6.8. Before, active power filter operation source phase current are 40.8, 40.28 and 20.15 for phase-a, phase-b and phase-c respectively as seen in Fig. 6.8 (b). The corresponding THDs values of source current are 15.05%, 15.25% and 24.06 as shown in Fig. 6.8 (g) .The 3P3W, zero sequence transformer and single phase APF are switched-on at t=0.16sec and t=0.26sec respectively. When the 3P3W APF and zero sequence transformer switched-on, source neutral current increases, due to presence of the zero sequence voltage. The source current after compensation found to be unbalanced and THDs are 48%, 69% and 50% for phase-a, phase-b and phase-c respectively. The increase of source current THDs are due to the circulation of large zero sequence current between source and zero sequence transformer. At this instant compensation provided by the 3P3W APF is not effective due to the saturation of the controller.

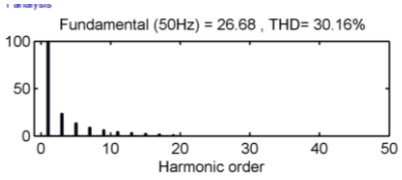
When neutral current compensator is switched-on at t=0.26 sec., the source neutral current almost disappear and it is evident from Fig. 6.8 (d). The source phase current becomes almost balance and synchronous with respective voltages. The THDs of the source currents reduces to 1.76%, 1.82% and 1.82% for phase-a, phase-b and phase-c respectively as evident from Fig. 6.8 (h).

6.4.1.4 Single phase load condition

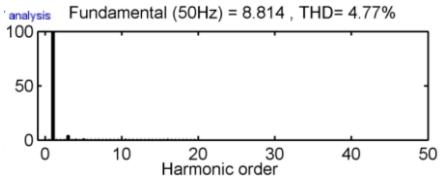
The single phase load conditions commonly occur in three phase four wire distribution system. Due to the single phase load condition large current circulate between the load and source and this can be regarded as most series problem. The simulation result under this condition is shown in Fig. 6.9. Before active power filter operation, the values of the source phase current are 20A, 0A and 0A for phase-a, phase-b and phase-c respectively and it is evident from Fig. 6.9 (b). The corresponding THDs values of source current before compensation are 36.1%, 0%, and 0% for phase-a, phase-b and phase-c respectively as shown in Fig. 6.9 (g). When the 3P3W APF and zero sequence transformer are switched-on at t=0.16sec and act as compensator, the source phase current are 22.02A, 23.21A and 15A for phase-a, phase-b and phase-c respectively. The source phase current is unbalanced and THDs are 57.21%, 45.24% and 34% for phase-a, phase-b and phase-c respectively.

As seen in Fig. 6.9 (d), when neutral current compensator is switched-on at t=0.24sec., the source neutral current almost disappear. Then the source phase currents tend to sinusoidal and in phase with respective voltages. The values of the source current THDs are 4.37%, 4.77% and 4.99% for phase-a, phase-b and phase-c respectively as shown in Fig. 6.9 (h).

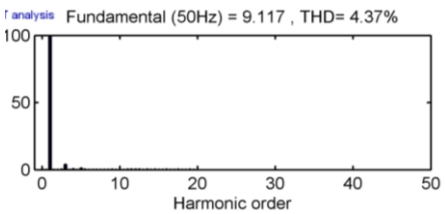




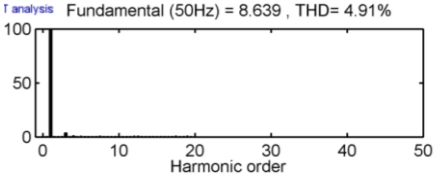
(g.1) phase-a load current THD spectra.



(h.2) phase-a source current THD spectra.



(h.1) phase-a source current THD spectra.



(h.3) Phase-c source current THD spectra.

Fig. 6.9. Performance of 3P4W under single phase load condition.

6.4.2 Volt-ampere rating of 3P4W APF

The Volt-ampere rating of the complete filter is the sum of the rating of the 3P3W APF and single phase active power filter [207]. The procedure for calculating volt-ampere rating of 3P3W APF and single phase active power filter is discussed in this section.

6.4.2.1 Volt-ampere rating of the Single-phase active power filter

The volt-ampere rating of the single phase active power filter is calculated as product of the peak compensating current and peak voltage. The peak current of the single phase active power filter can be calculated by considering fundamental zero-sequence component of the load current [207]. The peak voltage rating of the single phase active power filter switches is equal to the dc side capacitor voltage.

6.4.2.2 Volt-ampere rating of the three phase three wire APF

The Volt-Ampere rating of the 3P3WAPF is calculated as the product of the peak value of current injected by 3P3W APF and the peak value of dc side capacitor voltage. The Table 6.1 gives the comparison of Volt-Ampere ratings of 3P4W APF against the rating of the 3P4W APF as given in [80] .As seen in Table 6.1, the overall volt-ampere rating of the proposed 3P4W APF is reduced compared to other topologies.

Table 6.1: Comparison of active power filters ratings

Parameter	Split capacitor topology[80]	Four-wire pole[80]	Proposed 3P4W APF
Peak compensating current of APF (A)	100	100	40
DC side capacitor voltage of APF (V)	750	610	400
Rating of APF (VA)	7500	61000	24000
Peak compensating current of single-phase APF (A)	0	0	20
DC side voltage of single-phase APF (V)	0	0	25
Rating of single-phase APF (VA)	0	0	500
Total rating (VA)	75000	61000	16500

6.4.3 Experimental validation

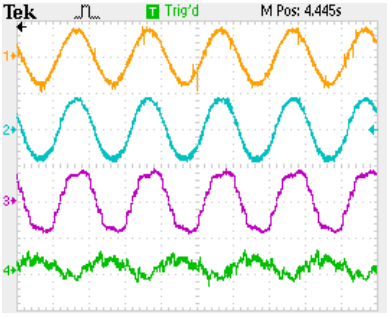
In order to verify the simulated response of the three phase four wire active filter a scaled down laboratory prototype has been developed. The laboratory prototype of 3P4W APF consisting of zero sequence transformers, 3P3W APF, ac power capacitors and a single phase active power filter is shown in Fig. 6.1. The power circuits of three phase three wire (3P3W) APF and single phase APF are realized using IGBTs. Two transformers of turn ratio

1:1 are used. The DC side voltage of the single phase APF is maintained at 25V using regulated power supply.

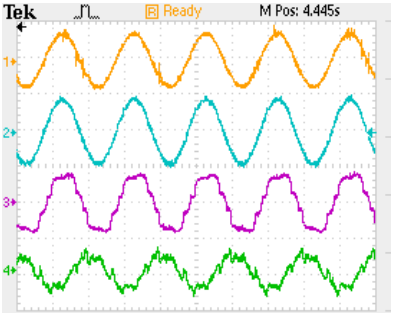
6.4.4 Balance utility voltage/distorted

The compensation performance of the 3P4W active power filter with single input fuzzy logic controller integrated with anti-Hebbian based on TLS is shown in Fig. 6.10. The source voltage, source current after compensation, load current and compensating currents for phase a, b and c in steady-state conditions are shown in Fig. 6.10 (a)-(c), respectively. In these figures, the channels of the different (DSO) waveforms are identified as; channel-1: source voltage (X-Axis: 10 ms/div. and Y-Axis: 100 V/div.); channel- 2: source current after compensation (X-Axis: 10 ms/div. and Y-Axis: 5 A/div.); channel-3: load current (X-Axis: 10 ms/div. and Y-Axis: 5 A/div.) and channel-4: compensating current injected by the 3P3W APF (X-Axis: 10 ms/div. and Y-Axis: 5 A/div.). Meanwhile the load is unbalanced, the load currents in channel-3 of Fig. Fig. 6.10(a)-(c) are not the same shape.

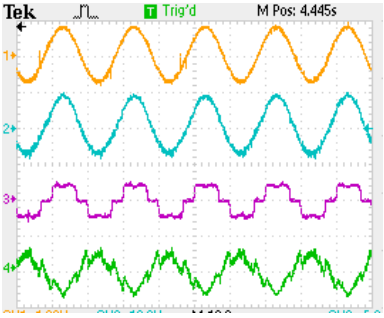
Fig. 6.10 (d) shows the source neutral current before compensation (X-Axis: 25 ms/div. and Y-Axis: 1 A/div.). The source neutral current when zero sequence transformer is alone acting as neutral current compensator (i.e. switch S is closed) is shown in Fig. 6.10 (e) (X-Axis: 25 ms/div. and Y-Axis:1 A/div.). As seen in Fig. 6.10(e), when zero sequence transformer alone operating as neutral current compensator, the source neutral current is reduced maximum extent then it is not completely eliminated. When the single-phase neutral compensator is switched-on, the source neutral current almost disappear. The source neutral current when zero sequence transformer and single-phase neutral compensator are acting as compensator as shown in Fig. 6.10 (f) (X-Axis: 25 ms/div. and Y-Axis: 1 A/div.) As seen from Fig. 6.10, the harmonic elimination, load balancing, and neutral current compensation is achieved with 3P4W hybrid APF. When single-phase neutral compensator is switched-on, the source almost disappear, the utility is supplying balanced three-phase currents only. The total harmonics distortion THD spectra of load current for phases a, b and c are shown in Fig. Fig. 6.10 (g)-(i) respectively. Before compensation with 3P4W APF, the THDs of the load currents are 18.2%, 21.7% and 20.3% respectively. The harmonic spectra of source current after compensation for phases a, b and c are shown in Fig. 6.10(j)–(l) respectively. The THDs of the compensated source currents are 3.1%, 3.6% and 3.1% respectively, which are well within the recommended standard of IEEE–519–1992.



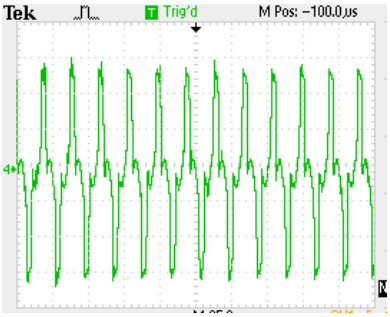
(a) phase-a waveforms



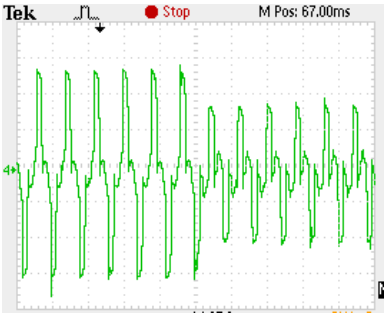
(b) phase-b waveforms



(c) phase-c waveforms

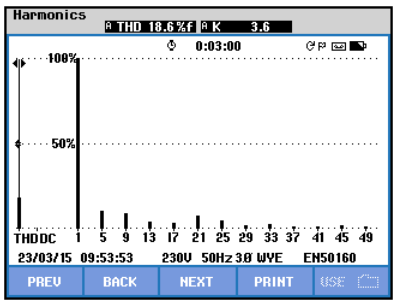


(d) Source neutral current before compensation.

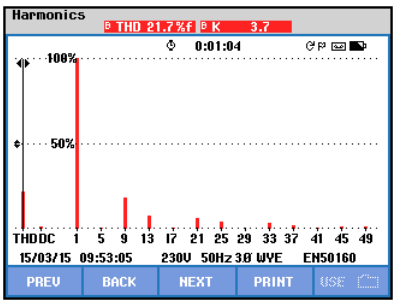


(e) Source neutral compensation with zero sequence transformer

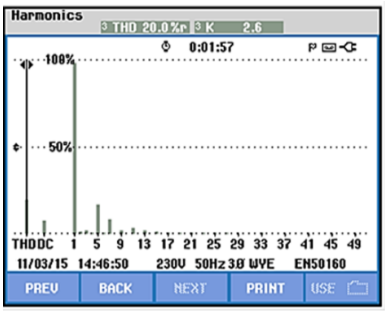
(f) Source neutral compensation with single phase neutral compensator.



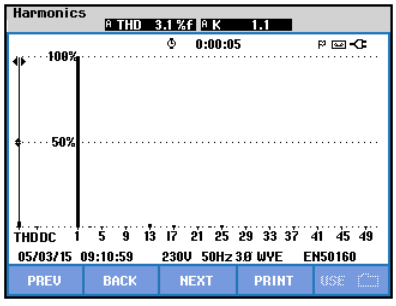
(g) Phase-a load current harmonics spectra.



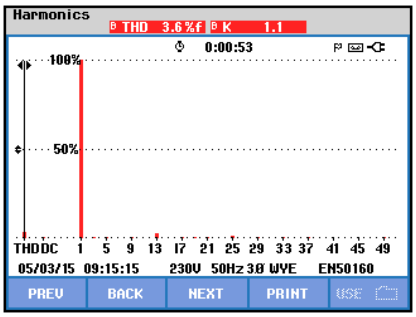
(h) Phase-b load current harmonics spectra.



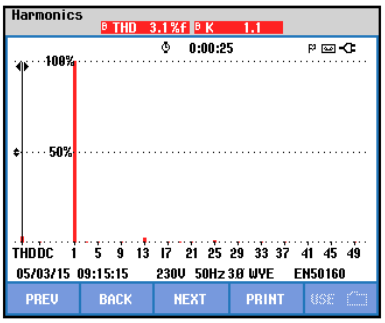
(i) Phase-c load current harmonics spectra.



(j) Phase-a source current harmonics spectra.



(k) Phase-b source current harmonics spectra.



(l) Phase-c source current harmonics spectra.

Fig. 6.10: Experimental waveform of 3P4W APF for balance utility voltage.

6.4.5 Unbalance utility voltage/distorted.

The proposed 3P4W APF has also been tested for harmonic elimination, load balancing and neutral current compensation in the existence of unbalanced/distorted voltage conditions. Fig. 6.11 shows the three-phase unbalanced/distorted source voltages, whereas the THD spectra of source voltage are shown in Fig. 6.12 (a)-(c). The THDs of the source voltages are 7.2%, 8.1% and 6.1% respectively.

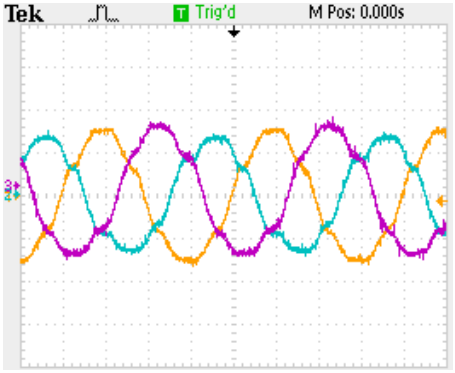
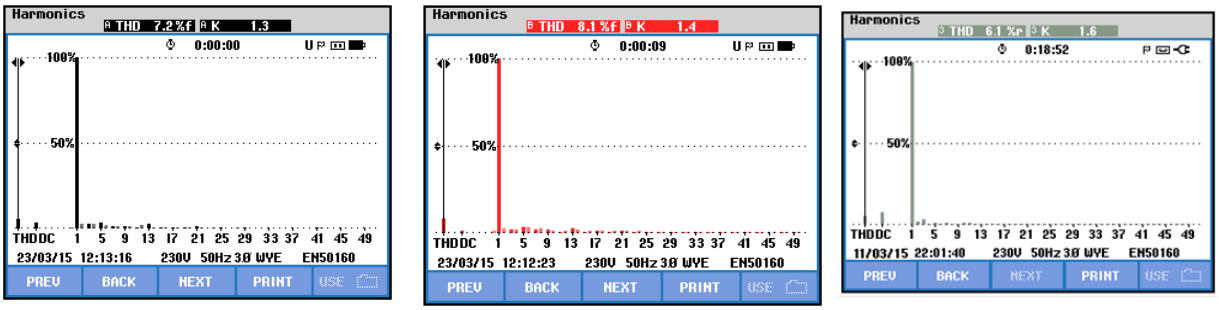


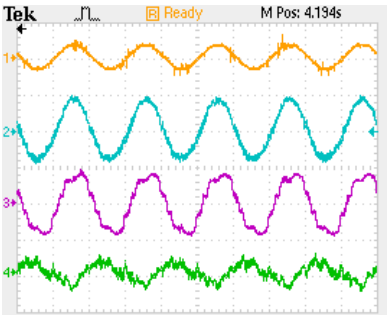
Fig. 6.11: Unbalanced/distorted three-phase source voltages



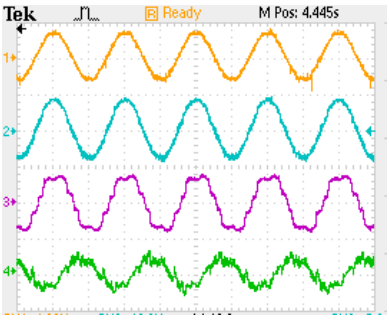
(a) (b) (c)

Fig. 6.12: THD spectra of source voltages: (a) phase–*a*; (b) phase–*b*; (c) phase–*c*.

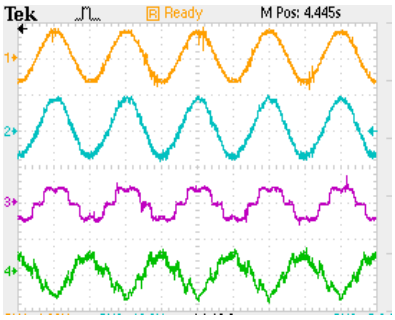
The source voltage, source current after compensation, load current and compensating currents for phase *a*, *b* and *c* in steady-state condition is shown in Fig. 6.13 (a)-(c), respectively. In these figures, the channels of (DSO) different waveforms are recognised as; channel-1: source voltage (X-Axis: 10 ms/div. and Y-Axis: 100 V/div.); channel- 2: source current after compensation (X-Axis: 10 ms/div. and Y-Axis: 5 A/div.); channel-3: load current (X-Axis: 10 ms/div. and Y-Axis: 5 A/div.) and channel-4: compensating current injected by 3P3W APF (X-Axis: 25 ms/div. and Y-Axis: 5 A/div.). Fig. 6.13 (d) shows the source neutral current before compensation (X-Axis: 25 ms/div. and Y-Axis: 1.3 A/div.). The source neutral current when only zero sequence transformer is connected (i.e. switch *S* is closed) is shown in Fig. 6.13 (e) (X-Axis: 25 ms/div. and Y-Axis: 1.3 A/div.). From Fig. 6.13 (e) It can be observed that when zero sequence transformer alone acting as a neutral current compensator, the source neutral current is increased.



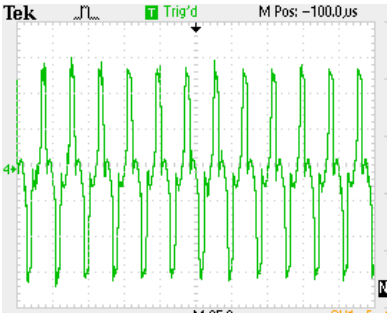
(a) phase-a waveforms



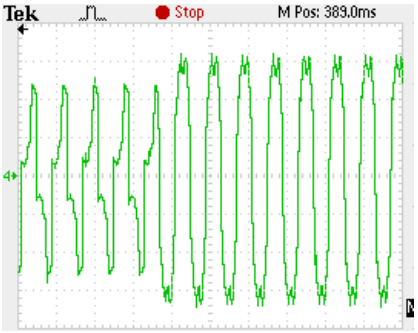
(b) phase-b waveforms



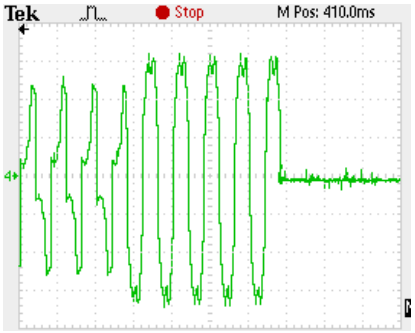
(c) phase-c waveforms



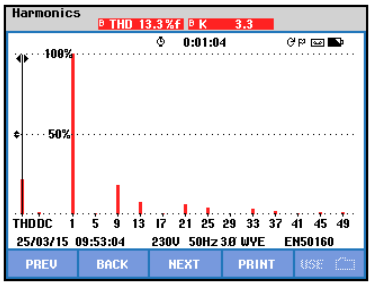
(d) Source neutral current before compensation



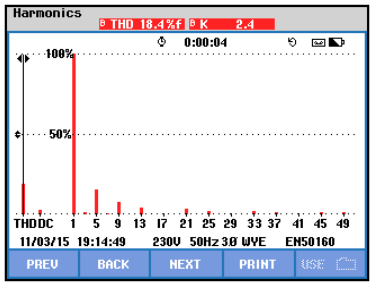
(e) Source neutral current compensation with zero sequence transformer



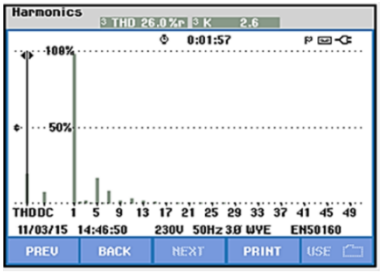
(f) Source neutral current compensation with single phase neutral compensator.



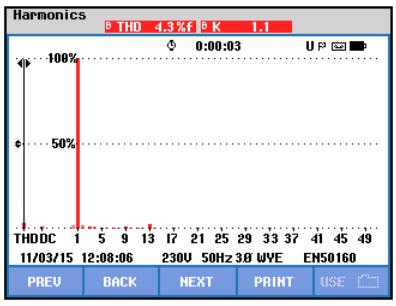
(g) Phase-a load current harmonic spectra.



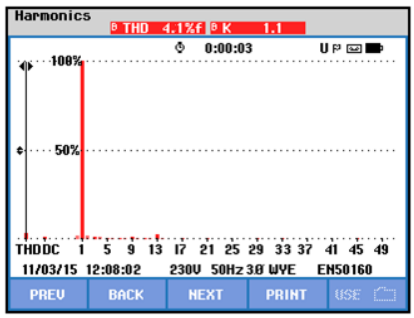
(h) Phase-b load current harmonic spectra.



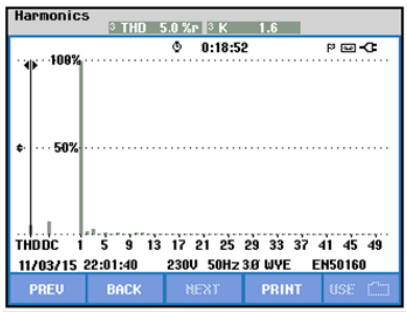
(i) Phase-c load current harmonic spectra.



(j) Phase-a source current harmonic spectra.



(k) Phase-b source current harmonic spectra.



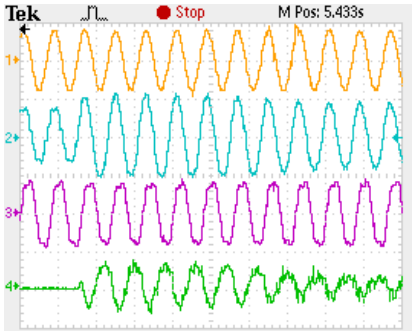
(l) Phase-c source current harmonic spectra.

Fig. 6.13: Experimental waveform of 3P4W APF for unbalance utility voltage.

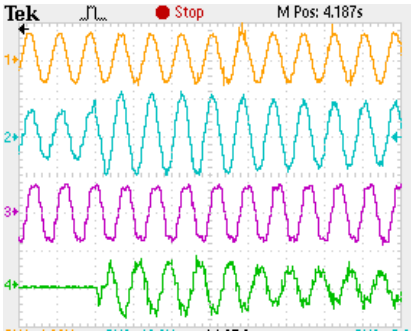
The increase in neutral current is due to circulation of large zero sequence current which is resulted from the existence of zero-sequence harmonics in source voltage. However, when switch *S* is open, the single-phase neutral compensator is switched-on and the source neutral current almost disappear. The source neutral current when single-phase APF is connected is shown in Fig. 6.13 (f) (X-Axis: 25 ms/div. and Y-Axis: 1.3 A/div.). As seen from Fig. 6.13, the proposed hybrid active power filter effectively compensates under unbalanced/distorted voltage conditions also with anti-Hebbian algorithm.

The harmonic spectra of load current for phases *a*, *b* and *c* are shown in Fig. 6.13 (g)-(i) respectively. Before compensation, the THDs of the load currents are 13.4%, 21.7% and 26.0% respectively. The harmonic spectra of source current after compensation for phases *a*, *b* and *c* are shown in Fig. 6.13 (j) − (l) respectively. The THDs of the source currents after compensation with 3P4W APF are reduced to 4.3%, 4.1% and 4.5% respectively, which shows the effectiveness of the 3P4W APF under unbalanced/distorted source voltage conditions. The power factors after compensation with 3P4W APF almost become unity.

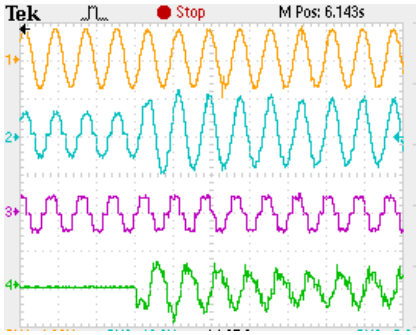
6.4.6 Transients performance of the 3P4W APF



(a) phase-a waveforms

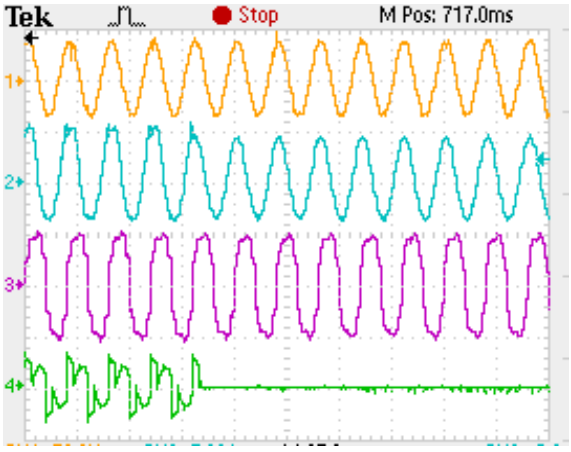


(b) phase-b waveforms



(c) phase-c waveforms

(e) Transient performance of 3P4W APF with Transformer acting as neutral compensator.



(f) Transient performance of 3P4W APF with Transformer and single phase neutral compensator acting as compensator.

Fig. 6.14: Experimental waveform under transient condition.

Fig. 6.14 shows the transient performance of the hybrid 3P4W APF. Initially, zero sequence transformer connected, the 3P3W APF and single phase APF are enabled are shown in Fig. 6.14 (a)-(c). As evident from these figures, before compensation with 3P3W and single phase APF the source current is distorted. After compensation with 3P3W APF and single phase neutral compensator, source phase current tend to sinusoidal. It can be observed that the proposed 3P4W APF has good transient response for this condition. Fig. 6.14 (e) shows experimental result for the conditions of 3P3W APF alone acting as current harmonic compensator and zero sequence transformer is enabled, the source current is distorted and contains zero sequence current. Further, it can be observed that the zero sequence current still exists in the source neutral. Fig. 6.14 (f) shows experimental results for the condition of 3P3W APF and zero sequence transformer acting as compensator, while single phase neutral compensator is enabled. As seen in Fig. 6.14 (f), the single phase neutral compensator completely attenuate source neutral current and source current tend to sinusoidal. These experimental results show that the proposed filter has good transient response.

6.5 Comparison with Simulation Results

In the simulated response presented in section 6.4.1, the 3P4W hybrid active power filter is tested at 400 V. However, due to the limitation involved in the development of prototype, the experimental studies are conducted at a reduced line voltage of 100 V. As the experimental studies are conducted at reduced system parameters, in order to validate the experimental results, the simulation is also carried out with reduced system parameters. The parameters used in the actual simulation and downscaled simulation studies are also given in Table 6.1. The downscaled simulation parameters are maintained same as that of experimental parameters as given in Table 6.1.

The simulated waveforms, load and source current harmonic spectra with nonlinear load composed of single-phase and three-phase uncontrolled rectifier with RL load under unbalanced/distorted utility voltage conditions are shown in Fig. 6.15 (a)-(h). As can be seen from Fig. 6.15, the simulated responses are almost identical with experimental results. Furthermore, in simulations results, the THDs in source current are reduced below 5%, but their values are somewhat higher than their equivalent experimental values. These increases in %THD of source currents is due to the large value of sampling time for the simulation study. The comparison of experimental and simulation results under normal and unbalanced/distorted utility voltage condition are given in Table 6.2 and Table 6.3 respectively.

Table 6.1: The parameters used in the downscaled simulation studies.

Parameters	**Actual 3P4W APF**	**Downscaled 3P4W APF**
AC line parameters	Three-phase, four-wire, 400 V, 50 Hz	Three-phase, three-wire, 100 V, 50 Hz
DC bus voltage of APF	200 V (for each capacitor in the H-bridge cell)	45 V (for each capacitor in the H-bridge cell)
DC bus voltage of single-phase APF	25 V	25 V
DC bus capacitance of APF	58μF (for each capacitor in the H-bridge cell)	1800 μF, 450 V (for each capacitor in the H-bridge cell)
APF interfacing inductor	*Lc* = 19 mH	L_c = 2.4 mH
Commutation inductance	L_{ac} = 1 mH	L_{ac} = 1 mH
Single-phase APF output inductor	L_f = 1.2 mH	L_f = 0.8mH
PWM switching frequency	2 kHz	2kHz
PWM switching frequency for single-phase APF	2kHz	2 kHz
Two single phase Transformers	10KVA, 230/230V;	2KVA, 230/230V;
Ac capacitor	180 μF 10kVAR	180 μF 10kVAR
Load	Three-phase uncontrolled rectifier with *RL* load; Two single uncontrolled rectifier with RL load.	Three-phase uncontrolled rectifier with *RL* load; Two single phase uncontrolled rectifier with *RL* load
Sampling time	T_s = 10e–6 sec.	T_s = 40e–6 sec.

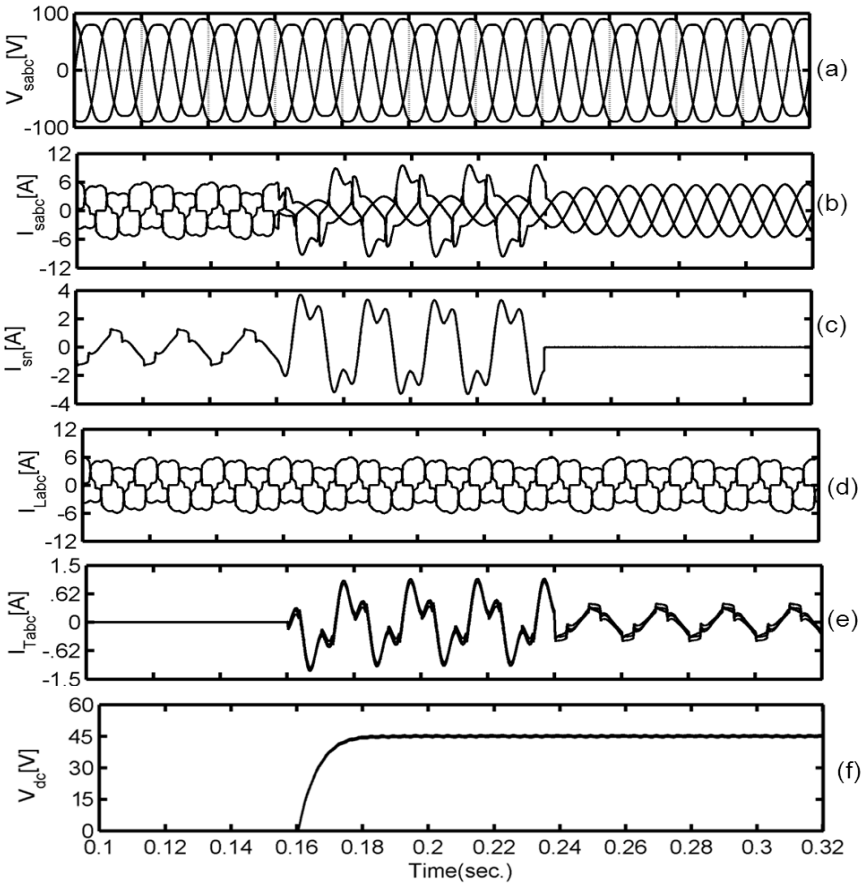
Table 6.2: Comparison of experimental and downscaled simulation results under normal utility voltage conditions with 3P4W APF

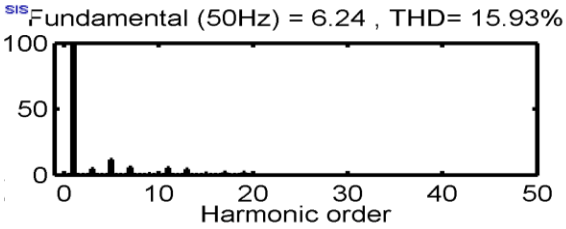
Parameters	**Experimentation**			**Simulation**		
	phase-*a*	phase-*b*	phase-*c*	phase-*a*	phase-*b*	phase-*c*
Load current (A, rms)	2.6	3.8	1.5	2.711	4.128	1.433
Source current (A, rms)	3	3	3	2.601	2.642	2.595
%THD of load current	18.6%	21.7%	20.3%	17.08%	22.27%	26.61%
%THD of source current after compensation	3.1%	3.6%	3.1%	2.84%	2.74%	3.79%
Load neutral current (A, rms)	3.5 A			3.6 A		
Peak value of source neutral current when switch *S* is closed (A)	1.6 A			1.5 A		
Source neutral current when switch *S* is open (rms, A)	0.12 A			0.214 A		

Table 6.3: Comparison of experimental and downloaded simulation results under unbalanced/distorted utility voltage conditions 3P4W APF.

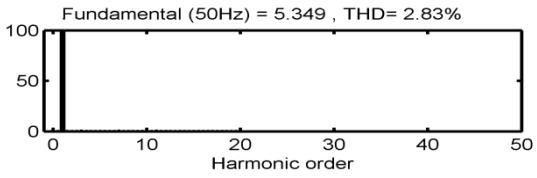
Parameters	**Experimentation**			**Simulation**		
	phase-*a*	phase-*b*	phase-*c*	phase-*a*	phase-*b*	phase-*c*
Load current (A, rms)	3.2	4.6	1.8	3.145	4.723	1.831
Source current (A, rms)	3.28	3.3	3.3	3.621	3.414	3.569
%THD of load current	13.3%	18.4%	26.0%	15.93%	18.32%	26.91%
%THD of source current after compensation	4.3%	4.1%	5.0%	2.83%	3.40%	2.74%
Load neutral current (A, rms)	3.6 A			3.65 A		
Peak value of source neutral current when switch *S* is closed (A)	3.9 A			4 A		
Source neutral current when switch *S* is open (rms, A)	0.2 A			0.23 A		

As can be seen from Table 6.2 and Table 6.3 the simulation results are almost identical with the experimental results. The increase in %THD of source currents is due to the large value of sampling time for experimental study. However, the anti-Hebbian algorithm integrated with SIFLC controller work effectively under unbalance/distorted voltage conditions in case of 3P4W hybrid active power filter also.

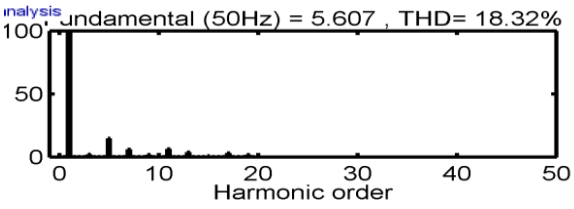




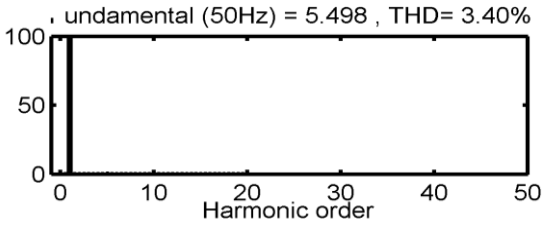
(g.1) phase-a load current THD spectrum.



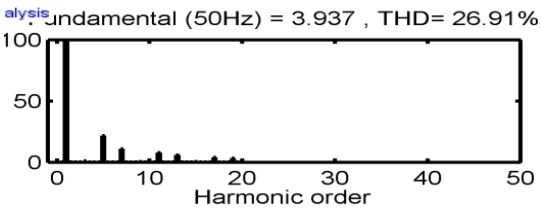
(h.1) phase-a source current THD spectrum.



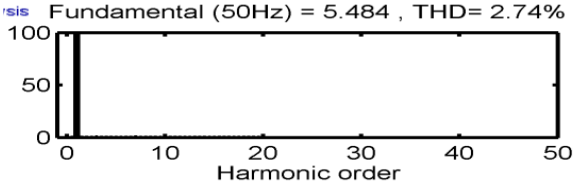
(g.2) phase-b load current THD spectrum.



(h.2) phase-b source current THD spectrum.



(g.3) phase-c load current THD spectrum.



(h.3) phase-c source current THD spectrum.

Fig. 6.15: The performance of 3P4W APF with downscaled simulation parameter under unbalanced/distorted utility voltage conditions.

6.6 Conclusion

Three-phase four-wire distribution power systems have been widely applied to low-voltage applications; however, they suffer from the problems of source phase harmonic current and large neutral current. In this chapter, a new hybrid 3P4W APF, comprised of a hybrid 3P3W active power filter, ac power capacitor and a neutral current compensator is proposed. The use of ac coupling capacitor enables in reduction in voltage at the point connection of 3P3P active power filter and neutral current compensator. In the proposed hybrid 3P4W active power filter, the overall power rating of power converters in the hybrid power filter and neutral current compensator can be effectively reduced, thus increasing its use in high-power applications and increases the operating efficiency. A prototype is developed and tested. Experimental results verify that the proposed hybrid 3P4W APF can compensates the source phase harmonic currents and neutral current under the balanced load or unbalanced load conditions. Hence, the proposed hybrid 3P4W active power filter is an effective solution to the problems of source phase current harmonic and neutral current in 3P4W electrical distribution power systems.

CHAPTER 7: CONCLUSION

The thesis dealt with the detailed review on application of shunt active power filter low and medium power applications. The digital controlled 3P3W and 3P4W APF have been proposed to compensate harmonics and reactive power requirement of nonlinear/ unbalanced to improve the power quality of the source current waveform in 3P3W and 3P4W distribution systems. The major conclusions derived from this work are summarised as follows.

- The aim of this thesis is to perform the comprehensive study of the issues related to power quality, specially, harmonics distortion, reactive power, unbalancing, neutral current and their remedies using active power filters.
- Among different topologies of VSI for high-power, medium-voltage active power filter proposed in the literature, diode clamped multilevel inverter and cascaded H-bridge has been found to be the best suitable topology for active power filter.
- In active power filter control, the calculation of the reference current is complex task in nonlinear load condition. The reference current is generated using adaptive neural network techniques such as least mean square, anti-Hebbian and anti-Hebbian based on total least square algorithms. These adaptive control schemes are integrated with PI and type-2 fuzzy logic controller. The adaptive neural network based approaches calculate the weights and these calculations perform online. These adaptive control schemes can extract the reference current under varying load condition and it is not possible with other control schemes. These adaptive control schemes are further validated by developing a three level DCMLI based active power filter. The different hardware components required for the proper operation of experimental set-ups such as pulse amplifier, isolation and dead-band circuits, voltage and current sensor circuits, non-linear loads have been designed and developed. A DSP of dSPACE has been used for the real-time implementation of the control schemes of the active power filter. The experimentally obtained source current and dc side capacitor voltage balancing and their corresponding harmonic spectra of the active power filter is observed to be in good agreement with simulation results. It is concluded that the control scheme based on anti-Hebbian with total least square along with T2FLC controller (for regulating capacitor voltage) are found to be most effective for three level DCMLI 3P3W active power filter. This proposed integrated with T2FLC remain most effective for lower level up to three levels. However, for MLI beyond three levels T2FLC controller become more complex to tune the controller parameters with larger rule base.
- The fuzzy logic controller involves fuzzification, rule base storage, inference mechanism and defuzzification operation etc. In most of the cases, for better accuracy and control, large set of rules are required. However, large set of fuzzy rule requires more

computational time. As a result, it may not be useful for real time implementation with small sampling time for multilevel inverter. The dspace implementation of the single fuzzy logic controller for voltage regulation of the CHBMLI based active power filter is described in detail. The single input fuzzy logic controller is derived from the conventional FLC using concept of the signed distance. The single input fuzzy logic controller reduces the 3-D control surface to piece wise linear control surface. The single input fuzzy logic controller with piece wise linear simplifies the implementation procedure. From the simulation and experimental results, it can be conclude that the SIFLC with PWL control surface has similar performance as that of the conventional FLC. Hence, the conventional can be FLC replaced by SIFLC with PWL control surface without significant degradation in the compensation performance of active power filter. The comparative study of the PI and SIFLC shows that the SIFLC has superior dynamic performance.

- As most of the distribution system are 3P4W. Therefore, detailed analysis of CHBMLI based 3P4W APF is carried out. The application of single input fuzzy logic controller integrated with anti-Hebbian based on TLS algorithm has been extend to 3P4W systems for simultaneous compensation of source phase current harmonics, neutral current and load balancing. To accomplish this, a reduced rating hybrid 3P4W APF have been proposed. The hybrid approach comprises of a 3P3W CHBMLI based APF, zero sequence transformer and single phase neutral current compensator. The simulation study has been presented to verify the efficacy of topology under ideal and non-ideal utility voltage conditions with anti-Hebbian algorithm integrated with single input fuzzy logic controller. The comparison of performance between transformer based topologies and 3P4W APF is presented. The simulated response of the proposed hybrid 3P4W APF is validated by developed laboratory prototype. The developed prototype of 3P4W APF is studied for compensation of source current harmonic and neutral current compensation with different utility voltage conditions. From these studies it has been observed that the proposed control schemes improve the power quality of the source currents even under distorted/unbalanced utility voltage conditions. Therefore, overall results prove that the control algorithm works efficiently and independent of the voltage.
- In order to further reduce the rating of 3P4W active power filter, a new hybrid three 3P4W APF is proposed for compensating current harmonics, reactive power and neutral current in 3P4W. The proposed hybrid 3P4W APF is consist of a neutral current compensator, CHBMLI based 3P3W APF and AC capacitor. The hybrid APF, realized by a 3P3W APF and ac power capacitor, is used for compensating the nonzero-sequence currents harmonic in the 3P4W distribution system. The 3P3W APF is connected to the power capacitors and its volt-ampere rating can thus be reduced effectively. The neutral current compensator is connected between the power capacitors with interfacing inductors of the

3P3W APF and compensates the source neutral current in the 3P4W distribution system. With the major fundamental voltage of the utility dropping across the power capacitors of the 3P4W APF, the power rating of the source current compensator can thus be reduced. Hence, the proposed hybrid 3P4W APF can effectively reduce the volt-ampere rating of passive and active components of the system. The simulated response of the proposed hybrid 3P4W APF is validated by developed prototype. The developed prototype of 3P4W APF is studied for compensation of current harmonic and neutral current compensation with different utility voltage conditions. From these studies it has been observed that the control scheme based on total least square with SIFLC improves the power quality of the source currents even under distorted/unbalanced utility voltage conditions.

7.1 Future scope

Research is an endless process. The end of a research project may begin opportunities for a lot of other avenues for future work. There are several important issues, which are experienced during this research work and these can be further investigated. Some of the important aspects as identified for future research works in this area are as:

1) The addition of active filter functions in the existing inverter of the grid interactive distributed generation systems like photovoltaic, fuel cell and wind with proper boosting, maximum power point tracking and conversion is a potential area for further research.
2) An integrated protection scheme and its performance for the proposed topologies of the filters under power system faults may be investigated.
3) Design of the controller of the active power using model predictive control is an active area of research.
4) Development of new modulation techniques for high power inverters with reduced power losses and natural balance of capacitor voltages is a potential area of research.
5) The experimental study was conducted based on a model of about 5kVA, while real industrial application with much larger powers of the order of several MVA. So it will be interesting to extend this study to high power systems to better understand the physical limitations imposed on the rise.
6) Extending our study to other topology such as double star bridge cell multilevel converters (seven and eleven levels) without changing control strategies which will allow us to reduce the switching frequency at the IGBT switches.

PUBLICATIONS FROM THE WORK

Journal published/ communicated

1. Dhanavath Suresh, S. P. Singh “Design of single input fuzzy logic controller for shunt active power filter,” pp. 1-10, DOI: 10.1080/03772063.2015.1024176, IETE Journal of research Taylor and Francis.
2. Dhanavath Suresh, S.P. Singh “Type-2 fuzzy logic controlled three level active power filter for power quality improvement,” Electr. Power component and system Taylor and Francis (Accepted).
3. Dhanavath Suresh, S.P. Singh “hybrid reduced rating active power filter for three phase four wire distribution system,” Journal of electrical engineering and technology (Accepted).
4. Dhanavath Suresh, S.P. Singh “A zero sequence transformer based hybrid active power filter for three phase four wire distribution system,” Electric Power component and system Taylor and Francis (Accepted).
5. Dhanavath Suresh, S.P. Singh, “T-T connected transformer based hybrid active power filter for three phase four wire distribution system,” Int. J Electr. Power and energy sys. Elsevier (Under review).
6. Dhanavath Suresh, S. P. Singh “Single-star bridge cell based active power filter with renewable energy interface,” Arabian journal of science and Engineering Springer (under review).
7. Dhanavath Suresh, S. P. Singh “Single-star bridge cell based active power filter for power quality improvement,” IETE journal of research Taylor and Francis (submitted after major revision).
8. Dhanavath Suresh, S. P. Singh, “adaptive control active power filter with type-2 fuzzy logic controller” Int. J Electr. Power and energy sys. Elsevier (Under review).
9. Dhanavath Suresh, S.P. Singh, “Design of SIFLC for five level active power filter,” IET power electronics (communicated).
10. Dhanavath Suresh, S.P. Singh, “Hybrid 3P4W DSTATCOM for suppressing harmonics and neutral current in 3P4W distribution system,” Int. J Electr. Power and energy sys. Elsevier (communicated)
11. Dhanavath Suresh, S.P. Singh, “ Total least square algorithm based reference current generation for DCMLI based active power filter,” Int. J Electr. Power and energy sys. Elsevier (communicated).
12. Dhanavath Suresh, S.P. Singh, “Performance investigation of LMS algorithm with PI/T2FLC controller,” Journal of power electronics (communicated).

Conference

1. Dhanavath Suresh, S. P. Singh “Reduced rating hybrid active power filter in a three phase Four-Wire Distribution System,” ICCCI Coimbatore 2014, pp.1-5, January 2014.
2. Dhanavath Suresh, S. P. Singh “Performance investigation of the shunt active power filter using neural network,” SCEECS MANIT Bhopal 2014, pp.1-5, January 2014.
3. Dhanavath Suresh, S. P. Singh “Inter leaved buck converter based active power filter control using artificial neural network,” PEDES 2014, IIT Bombay, December 2014.
4. Dhanavath Suresh, S.P. Singh “Improved performance of active power filter using type-2 fuzzy logic controller,” IICPE 2014 NIT Kurukshtra, December 2014

PHOTOGRAPHS OF THE EXPERIMENTAL SETUP

Fig.1 Host computer generating firing pulses

Fig.2. Experimental setup

Fig. 3 Host computer running dSPACE

Fig. 4 Ac power capacitor

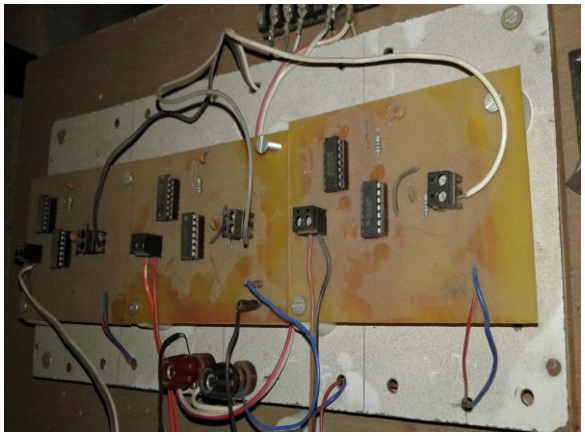


Fig.5. Dead Band circuit

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In this appendix, the snapshots of the MATLAB/Simulink models of the 3P3W three level DCMLI active power filter is shown

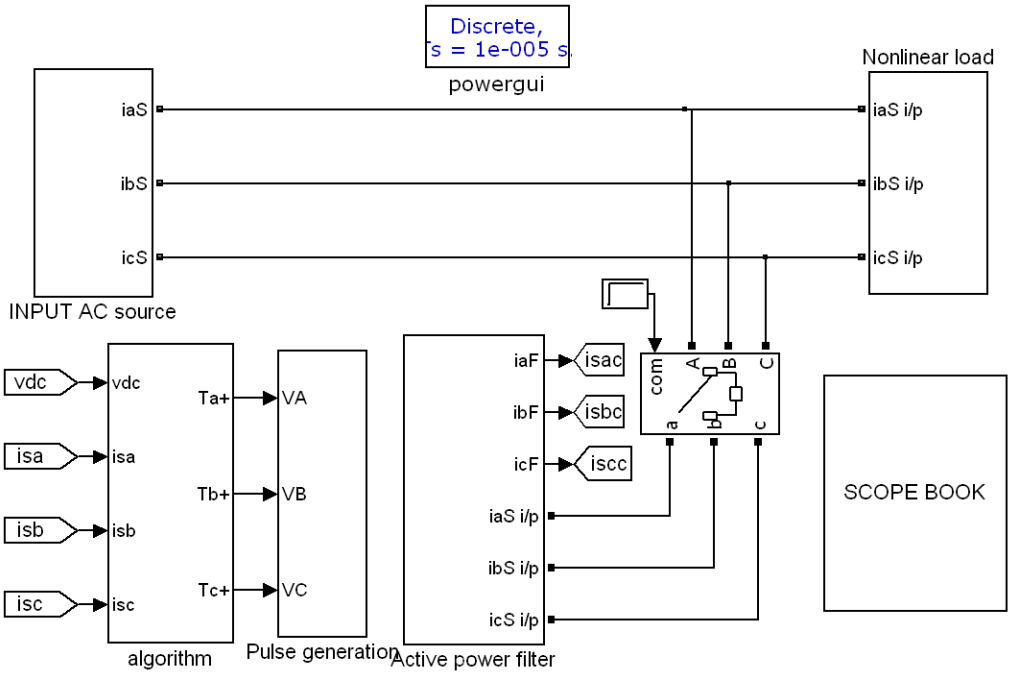

Fig. A. 1: Simulation model of three level active power filter.

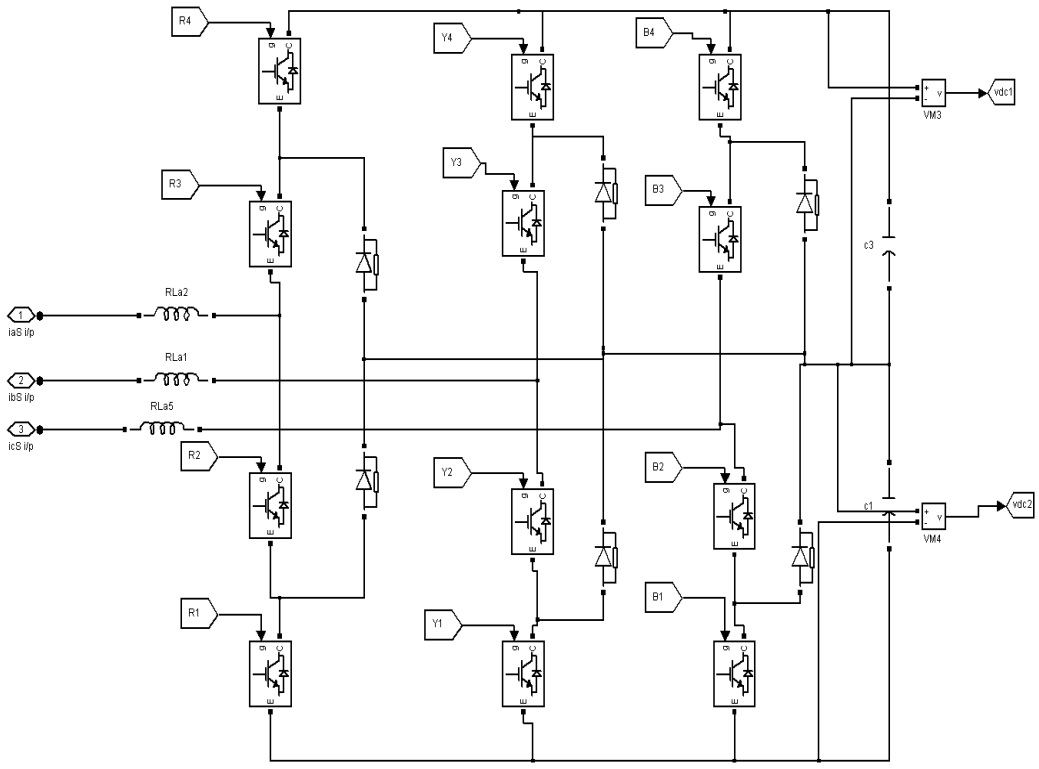

Fig. A. 2: Power circuit of three level DCMLI.

In this appendix, Matlab/simulink model of the 3P3W CHBMLI based five level active power filter is shown.

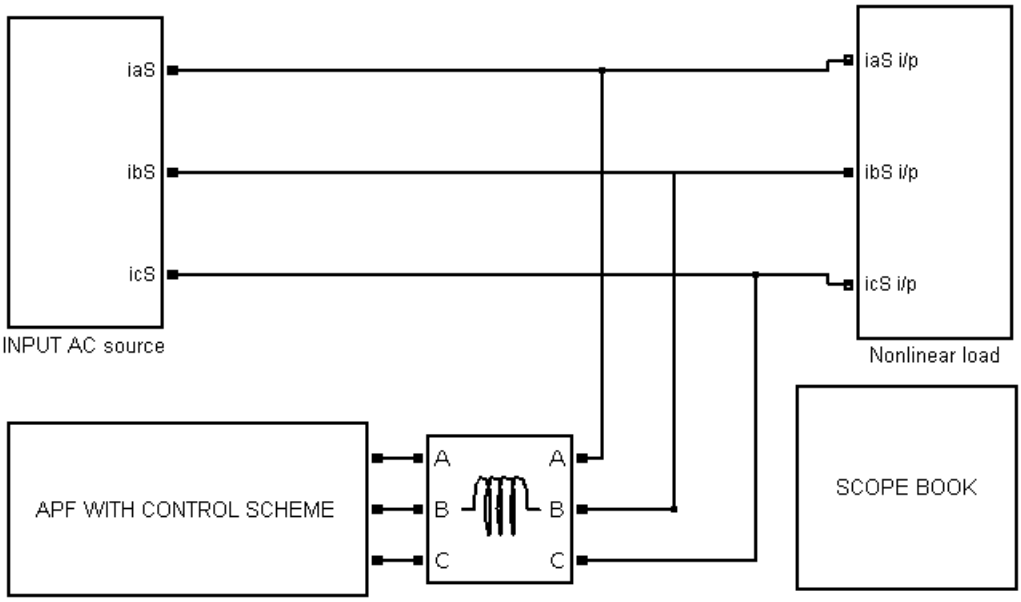

Fig.B.1: Snapshot of five level active power filter.

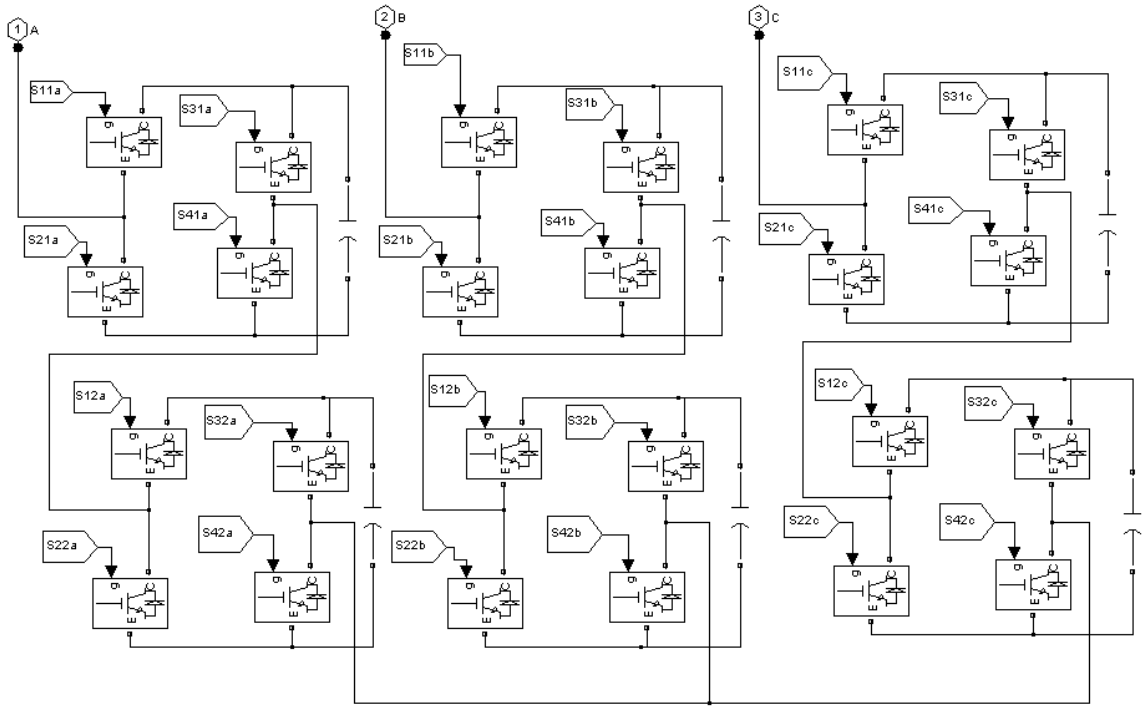

Fig.B.2. Simulink model of five level filter.