DESIGN AND IMPLEMENTATION OF DC-DC BI-DIRECTIONAL BUCK AND BOOST CONVERTER

A DISSERTATION

Submitted in partial fulfillment of the
requirements for the award of the degree
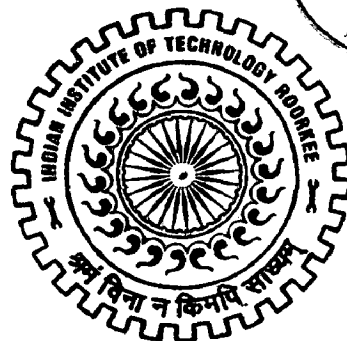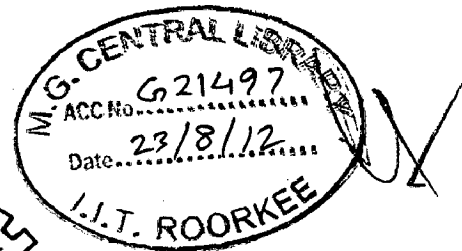*of*

INTEGRATED DUAL DEGREE

in

ELECTRICAL ENGINEERING
(With Specialization in Power Electronics)

By

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CANDIDATE'S DECLARATION

I hereby declare that the work that is being presented in this dissertation entitled "**Design and Implementation of DC-DC Bi-directional Buck and Boost Converter**" in partial fulfillment of the requirement for the award of the degree of **Integrated Dual Degree in Electrical Engineering** with specialization in "**Power Electronics**" submitted to the **Department of Electrical Engineering, Indian Institute of Technology, Roorkee, INDIA** is an authentic record of my own work carried under the guidance of **Dr. S.P. SINGH, Professor**, Department of Electrical Engineering, Indian Institute of Technology, Roorkee.

The matter embodied in this dissertation has not been submitted for the award of any other degree or diploma.

Date: 15/06/2012

SUMANTH PALA

Place: Roorkee

CERTIFICATE

This is to certify that the above statement made by the candidate is true to the best of my knowledge.

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ACKNOWLEDGEMENT

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ABSTRACT

Switch Mode Power Supplies (SMPS) are very important components in present day electronics and have continued to thrive and grow over the past 25 years. Electronic switch-mode DC to DC converters convert one DC voltage level to another, by storing the input energy temporarily and then releasing that energy to the output at a different voltage. The storage may be in either magnetic field storage components (inductors, transformers) or electric field storage components (capacitors). This conversion method is more power efficient (often 75% to 98%) than linear voltage regulation (which dissipates unwanted power as heat).

Most DC to DC converters are designed to transfer power in only one direction, from the input to the output. However, all switching regulator topologies can be made bi-directional by replacing all diodes with independently controlled active rectification. A bi-directional converter can transfer power in either direction, which is useful in applications requiring regenerative braking etc.

This project deals with the bi-directional buck and boost converter, their basic functioning and their stability under closed loop. It discusses clearly about how to design, implement the analog controller and digital controller for bi-directional buck and boost converter. It also discuss about non-linear controller design i.e. fuzzy controller for the boost converter. Designing of the controller is verified with the help of MATLAB simulation.

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LIST OF SYMBOLS

V_{in}, V_i, V_d	Input voltage
R	Resistance
R_L	Load resistance
i_L	Inductor current
I_o	Output current
I_{in}	Input current
V_o	Output voltage
r_L	ESR value of the inductor
r_C	ESR value of the capacitor
C	Capacitor
L	Inductor
D, d	Duty cycle or duty ratio
F_{sw}, f_{sw}	Switching frequency
f_{co}	Cross over frequency
V_{sw}	Voltage across a switch

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CHAPTER-I

INTRODUCTION

[This chapter gives basic insight about SMPS, bi-directional dc-dc converters. It also presents literature review on bi-directional dc-dc converters, their recent advancements and applications.]

1.1 Introduction to SMPS

In day to day life many applications need well-regulated dc supply for their proper operation. In majority of the cases the required voltages are of magnitudes varying between -24 to +24 volts. Some equipment may need multiple output power supplies. For example, in a Personal Computer one may need 3.3 volt, ±5 volt and ±12 volt power supplies. The digital ICs may need 3.3volt supply and the hard disk driver or the floppy driver may need ±5 and ±12 volts supplies. The individual output voltages from the multiple output power supply may have different current ratings and different voltage regulation requirements. The input connection to these power supplies is often taken from the standard utility power plug point (ac voltage of 115V / 60Hz or 230V / 50Hz). It may not be unusual, though, to have a power supply working from any other voltage level which could be of either ac or dc type.

There are two broad categories of power supplies: Linear regulated power supply and switched mode power supply (SMPS). In some cases one may use a combination of switched mode and linear power supplies to gain some desired advantages of both the types.

1.2 Linear regulated power supply

Fig. 1.1 shows the basic block for a linear power supply operating from an unregulated dc input. This kind of unregulated dc voltage is most often derived from the utility ac source. The utility ac voltage is first stepped down using a utility frequency transformer, and then it is rectified using diode rectifier and filtered by placing a capacitor across the rectifier output. The voltage across the capacitor is still fairly unregulated and is load dependent. The ripple in the capacitor voltage is not only dependent on the capacitance magnitude but also depends on load and supply

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voltage variations. The unregulated capacitor voltage becomes the input to the linear type power supply circuit. The filter capacitor size is chosen to optimize the overall cost and volume. However, unless the capacitor is sufficiently large the capacitor voltage may have unacceptably large ripple. The magnitude of voltage-ripple across the input capacitor increases with increase in load connected at the output.

The end user of the power supply will like to have a regulated output voltage (with voltage ripple within some specified range) while the load and supply voltage fluctuations remain within the allowable limit. To achieve the unregulated dc voltage is fed to a voltage regulator circuit. The circuit in Fig.1.1 shows, schematically, a linear regulator circuit where a transistor is placed in between the unregulated dc voltage and the desired regulated dc output. Efficiency of linear voltage regulator circuits will be quite low when supply voltage is on the higher side of the nominal voltage.
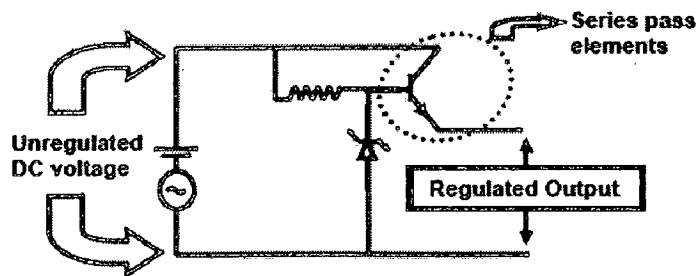
Fig 1.1: Schematic linear voltage regulator

1.3 Switched Mode Power Supply (SMPS)

Like a linear power supply, the switched mode power supply too converts the available unregulated ac or dc input voltage to a regulated dc output voltage. However in case of SMPS with input supply drawn from the ac mains, the input voltage is first rectified and filtered using a capacitor at the rectifier output. The unregulated dc voltage across the capacitor is then fed to a high frequency dc-to-dc converter. Most of the dc-to-dc converters used in SMPS circuits have an intermediate high frequency ac conversion stage to facilitate the use of a high frequency transformer for voltage scaling and isolation. In contrast, in linear power supplies with input

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voltage drawn from ac mains, the mains voltage is first stepped down (and isolated) to the desired magnitude using a mains frequency transformer, followed by rectification and filtering. The high frequency transformer used in a SMPS circuit is much smaller in size and weight compared to the low frequency transformer of the linear power supply circuit.

The 'Switched Mode Power Supply' owes its name to the dc-to-dc switching converter for conversion from unregulated dc input voltage to regulated dc output voltage. The switch employed is turned 'ON' and 'OFF' (referred as switching) at a high frequency. During 'ON' mode the switch is in saturation mode with negligible voltage drop across the collector and emitter terminals of the switch whereas in 'OFF' mode the switch is in cut-off mode with negligible current through the collector and emitter terminals. On the contrary the voltage-regulating switch, in a linear regulator circuit, always remains in the active region.

A high switching frequency (of the order of 100 KHz) and a fast control over the duty ratio results in application of the desired mean voltage along with ripple voltage of a very high frequency to the output side, consisting of a low pass filter circuit followed by the load. The high frequency ripple in voltage is effectively filtered using small values of filter capacitors and inductors.
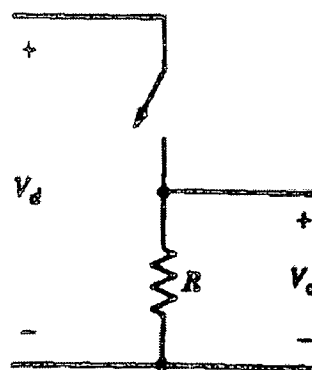
Fig 1.2: Schematic SMPS

1.4 SMPS versus linear power supply

As discussed above, in a linear regulator circuit the excess voltage from the unregulated dc input supply drops across a series element (and hence there is power loss in proportion to this voltage

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drop) whereas in switched mode circuit the unregulated portion of the voltage is removed by modulating the switch duty ratio. The switching losses in modern switches (like: MOSFETs) are much less compared to the loss in the linear element.

In most of the switched mode power supplies it is possible to insert a high frequency transformer to isolate the output and to scale the output voltage magnitude. In linear power supply the isolation and voltage-scaling transformer can be put only across the low frequency utility supply. The low frequency transformer is very heavy and bulky in comparison to the high frequency transformer of similar VA rating. Similarly the output voltage filtering circuit, in case of low frequency ripples is much bulkier than if the ripple is of high frequency. The switched mode circuit produces ripple of high frequency that can be filtered easily using smaller volume of filtering elements.

Linear power supply though more bulky and less efficient has some advantages too when compared with the switched mode power supply. Generally the control of the linear power supply circuit is much simpler than that of SMPS circuit. Since there is no high frequency switching, the switching related electro-magnetic interference (EMI) is practically absent in linear power supplies but is of some concern in SMPS circuits. Also, as far as output voltage regulation is concerned the linear power supplies are superior to SMPS. One can more easily meet tighter specifications on output voltage ripples by using linear power supplies.

1.5 Literature Review

Switch mode power supplies were already developed in the beginning of the 1920s. the first switching power supplies used mercury-arc rectifiers and grid controlled mercury arc tubes. However, these mercury arc supplies had limited commercialization due to some problems found in the switching devices used. They were namely poor efficiency, high cost, questionable reliability and high maintenance [16].

During the late 1960s, these problems were overcome when the semiconductor industry developed a variety of high performance switching devices. The discovery of these switching devices became significant to power supplies and had a great impact on its industry. Their superior performance characteristics had allowed them to break markets that had been

unattainable for mercury arc. Nonetheless, it was only until the 1970s that SMPS had been widely used [5].

The first switched-mode power supply was patented in 1976. In the following year, Apple Computer became the first computer manufacturer to use a SMPS in a production unit. The use of this type of power supply allowed the Apple II to be lighter and more compact than other competing computers.

Prior to the development of the switched-mode power supply, most personal computers used linear regulators. These earlier power units produced a set, unvaried amount of voltage. In order to keep this output constant, linear supplies typically used simple resistors. This generated a significant amount of heat, and wasted voltage during the regulation process.

In 1986, Lab.gruppen achieved an industry breakthrough with development of the Regulated Switch Mode Power Supply, or R.SMPS. The concept of a switch mode power supply was well known at the time, but difficult engineering challenges had prevented successful implementation in high-power audio amplifiers. Lab.gruppen's Kenneth Andersson had devised an innovative solution, though the components required to make it work were not yet available. As soon as Siemens introduced its first high voltage MOSFET devices, Andersson's design was quickly implemented in the revolutionary SS 1300.

D. R. Northcott, S. Filizadeh, A. R. Chevrefils [17] presented a process for the design and development of a bidirectional buck-boost dc/dc converter for use as a generator controller in a series hybrid electric vehicle is presented. The converter allows a single permanent magnet dc (PMDC) electric machine to be used for both engine starting and generating modes. The power electronics and the control system methodology are studied. A control system is developed for which the parameters are selected and optimized using nonlinear simplex simulation based optimization. The converter and optimized control system are tested under a simulated scenario to verify acceptable functionality and performance.

Wei Li, Géza Joós, and Chad Abbey [18] have proposed a parallel structure of bidirectional buck/boost converters and its power-tracking control scheme for wind ESS applications. The converter performance is studied and compared to the single-unit topologies. The proposed

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converter has smooth currents and fast dynamics which allow reduction of converter switching frequency and dc filtering capacitor. Other advantages of this topology include reduction of switching losses, improved reliability and flexibility.

Chin Chang, Zytec Corporation, [19] describes the dynamic behavior of the Buck converter for voltage mode control. For the current mode control case, an unstructured multiplicative uncertainty model is used to capture the family of perturbed small signal dynamics of the Buck converter. The powerful Kharitonov's theorem and the LQG/LTR technique are suitable for the design of robust controllers for DC-DC converters even it is more challenge for Boost and Fly back converters.

RD.Middlebrook And Slobodan Cuk [20] developed a method for modeling switching-converter power stages, whose starting point is the unified state-space representation of the switched networks and whose end result is either a complete state-space description or its equivalent small-signal low-frequency linear circuit model. The new canonical circuit model predicts that, in general, switching action introduces both zero and poles into the duty ratio to output transfer function in addition to those from the effective filter network.

Jian-ming HU, Yuan-rui CHEN, Zi-juan [21] discuss about high power bidirectional flow capability, with wide input voltage range, and output voltage of energy storage devices such as super capacitors or batteries vary with the change in load. Then the selection and design of aforementioned converter is proposed.

H. Li, Fang Z. Peng [22] presented a new zero-voltage-switching (ZVS) bidirectional dc–dc converter. Compared to the traditional bidirectional dc–dc converters for the similar applications, the new topology has the advantages of simple circuit topology with no total device rating (TDR) penalty, soft-switching implementation without additional devices, high efficiency and simple control. These advantages make the new converter promising for medium and high power applications especially for auxiliary power supply in fuel cell vehicles and power generation where the high power density, low cost, lightweight and high reliability power converters are required.

Mikkel C. W. Høyerby, Michael A. E. Andersen [26] describes the derivation of a practical solution to designing a medium-power non-isolated DC/DC power converter with very low

output ripple voltage and very high output voltage slew-rate capability. A simple and effective analog control scheme for the converter is developed, along with an accurate linear model.

Duan and Jin from University of British Columbia [27] made a thorough evaluation of different digital control design approaches and the performance of the approaches is compared in terms of both the bandwidth and the phase margin of the control loop, as well as the output transient response subject to line and load step change. Best digital design approach for power converter applications is identified based on the comparison results.

Giuseppe Capponi, Patrizia Livreri, Giuseppe Di Blasi, Filippo Marino [30] presents a new linear model for the Sigma-Delta modulator, based on modeling the nonlinear quantizer with a linear factor. The use of a 1-bit Sigma-Delta modulator in dc/dc power converter systems permits to implement a complete digital control.

J. Carwardine, F. Lenkszus [32] review current trends in the use of advanced technology such as embedded DSP controllers, and the application of real-time algorithms to the regulation and control of power supplies for accelerators and other large scale physics applications.

P R Holme and C D Manning [33] presented a method for the digital control of high frequency pwm converters. Digital current mode control and its advantages are discussed. Slope compensation is not required to stabilise the converter at duty ratios above 0.5. A modular architecture is put forward for practical circuit implementation.

R. M. Button, P. E. Kascak, R. Lebron-Velilla [38] discuss the digital control technologies that have been developed to greatly reduce the input filter requirements for paralleled, modular DC-DC converters. The use of phase shift technique reduced the filter size required for commercial DC-DC converters.

Dragon Maksimovic, and Regan Zane [42] presented an exact small-signal discrete-time model for digitally controlled pulse width modulated (PWM) dc–dc converters operating in constant frequency continuous conduction mode (CCM) with a single effective A/D sampling instant per switching period. The model, which is based on well-known approaches to discrete-time modeling and the standard -transform, takes into account sampling, modulator effects and delays in the control loop, and is well suited for direct digital design of digital compensators.

N. Rajarajeswari and K. Thanushkodi [43] introduces a novel Bi-directional DC-DC converter with artificial neural network controller (ANN).Bidirectional power flow is obtained by the same power components and provides a simple, efficient, and galvanically isolated converter. In the presence of DC mains the converter operates as buck converter and charges the battery. When the DC main fails, the converter operates as boost converter and the battery feeds the load.

N. Rajarajeswari and K. Thanushkodi [44] introduces a Bi-directional DC-DC converter with adaptive fuzzy logic controller. The power switches are controlled by Pulse Width Modulation technique and the pulses are generated by the application of fuzzy logic with an adoption algorithm.

1.5.1 Bi-directional dc-dc converters (BDC)

Bidirectional dc-dc converters (BDC) have recently received a lot of attention due to the increasing need to systems with the capability of bidirectional energy transfer between two dc buses. Apart from traditional application in dc motor drives, new applications of BDC include energy storage in renewable energy systems, fuel cell energy systems, hybrid electric vehicles (HEV) and uninterruptible power supplies (UPS). The fluctuation nature of most renewable energy resources, like wind and solar, makes them unsuitable for standalone operation as the sole source of power. A common solution to overcome this problem is to use an energy storage device besides the renewable energy resource to compensate for these fluctuations and maintain a smooth and continuous power flow to the load. As the most common and economical energy storage devices in medium-power range are batteries and super-capacitors, a dc-dc converter is always required to allow energy exchange between storage device and the rest of system. Such a converter must have bidirectional power flow capability with flexible control in all operating modes.

In HEV applications, BDCs are required to link different dc voltage buses and transfer energy between them. For example, a BDC is used to exchange energy between main batteries (200-300V) and the drive motor with 500V dc link. High efficiency, lightweight, compact size and high reliability are some important requirements for the BDC used in such an application.

BDCs also have applications in line-interactive UPS which do not use double conversion technology and thus can achieve higher efficiency. In a line-interactive UPS, the UPS output

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terminals are connected to the grid and therefore energy can be fed back to the inverter dc bus and charge the batteries via a BDC during normal mode. In backup mode, the battery feeds the inverter dc bus again via BDC but in reverse power flow direction.

BDCs can be classified into non-isolated and isolated types. Non-isolated BDCs (NBDC) are simpler than isolated BDCs (IBDC) and can achieve better efficiency. However, galvanic isolation is required in many applications and mandated by different standards. The complexity of IBDCs stems from the fact that an AC link must be present in their structure in order to enable power transfer via a magnetically isolating media, i.e. a transformer. In this chapter, first some NBDC structures are briefly discussed. As isolation and/or voltage matching is required in many applications, more attention in this chapter is paid on the description of different IBDC configurations. It should be stated that in order to improve the efficiency, almost all recently proposed medium-power IBDC configurations have exploited the benefits of soft-switching or resonant techniques to increase the switching frequency and achieve lower size and weight.

1.5.2 Non-isolated BDC

Basic dc-dc converters such as buck and boost converters (and their derivatives) do not have bidirectional power flow capability. This limitation is due to the presence of diodes in their structure which prevents reverse current flow. In general, a unidirectional dc-dc converter can be turned into a bidirectional converter by replacing the diodes with a controllable switch in its structure. As compared to high-frequency transformer-isolated bidirectional dc-dc converters, non-isolated bi-directional dc-dc converters generally have advantages of simple structure, high efficiency, low cost, high reliability, etc. These BDC are used in high power applications i.e is around 30kW if isolation is already taken care [46].

1.5.3 Isolated BDC (IBDC)

Galvanic isolation between multi-source systems is a requirement mandated by many standards. Personnel safety, noise reduction and correct operation of protection systems are the main reasons behind galvanic isolation.

Most of the Medium-power IBDCs have a structure similar to Fig.1.3 generally rated at rated at 1-5 kW. This structure consists of two high-frequency switching dc-ac converters and a high-

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frequency transformer which is primarily used to maintain galvanic isolation between two sources. This transformer is also essential for voltage matching in case of large voltage ratio between two sources. The transformer calls for ac quantities at its terminals and thus a dc-ac converter is employed on each side. As energy transfer in either direction is required for the system, each dc-ac converter must also have bidirectional energy transfer capability. With the same token, the dc buses in this structure must also be able to either generate or absorb energy. Galvanic isolation by a transformer provides a measure of safety, and the design of this transformer introduces many choices. These BDC are preferred for high power applications i.e is around 35kW.
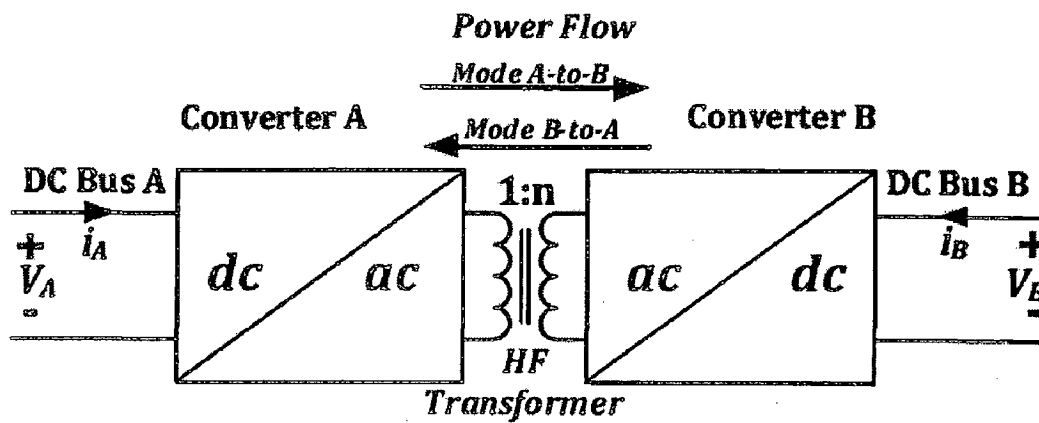
Fig 1.3: Basic structure of an IBDC

1.5.4 Applications

Minimizing greenhouse gas effects by reducing CO_2 and other emissions is one of the most challenging issues that human is presently facing. As electricity generation is one of the major causes of the pollution, finding alternative clean electricity generation methods is thus becoming attractive. In this regard, renewable energy resources such as wind and solar energy are among the most important substitutes for traditional fuel-based energy production. However, the intermittent nature of most renewable sources does not allow having a reliable and continuous source of energy when these resources are used alone. The fluctuating energy produced by these sources may also cause adverse effects on the power quality of the grid that these resources are connected to. By using energy storage devices, these fluctuations can be absorbed to deliver smooth power to consumers and at the same time maximize the energy output of renewable

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resources. This reduces the output required from conventional power stations which directly reduces CO2 emissions. The dc-dc converter shown in this system is of non-isolated type, e.g. the converter shown in Fig.1.4.
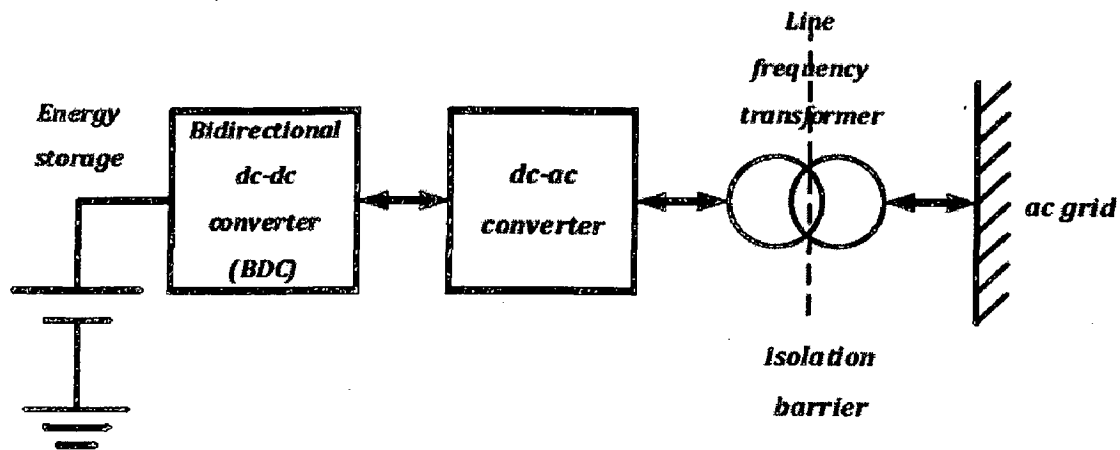
Fig 1.4: Basic structure of an energy storage device connected to an ac grid through a line frequency transformer.

Besides smoothing the energy output of renewable resources, energy storage systems have other technical applications in the utility grid including grid stabilization, frequency and voltage support, power quality and reliability enhancement and load shifting.

1.6 Recent advancements

- Bi-directional DC-DC converter with artificial neural network controller (ANN). In the presence of DC mains the converter operates as buck converter and charges the battery. When the DC main fails, the converter operates as boost converter and the battery feeds the load. In both the modes the PWM pulses are generated by application of ANN controller.

- Bi-directional DC-DC converter with adaptive fuzzy logic controller. The power switches are controlled by Pulse Width Modulation technique and the pulses are generated by the application of fuzzy logic with an adoption algorithm.

- DSP or FPGA controlled Bi-directional buck and boost converter. In both the modes the power switches are controlled by PWM technique and the PWM pulses are

generated by DSP or FPGA. By using this digital processor we can implement neural network controller (ANN), Adaptive fuzzy logic controller.

1.7 Objectives of Thesis Work

My current area of working is to design implementation of Bi-directional buck and boost converter using both analog controller and digital controller. Analog controller is designed using the available analog ICs; the digital controller is designed with the use of DSP or FPGA

The methodology to achieve the objectives is as follows

1. Design the power circuit for the both buck and boost converters based on the requirements.
2. Design the compensation or controller using type 3 for analog controller and digital controllers are designed using PID, fuzzy, direct & In-direct digital design approach.
3. Modelling of the converter with complete closed loop control using Simulink in MATLAB.
4. Hardware is implemented of the bi-directional converter using analog controller with IC's and for digital implementation DSP or FPGA is used.

DC-DC CONVERTERS

[Presented in this chapter are the basic operations of different non-isolated dc-dc converters like buck converter, boost converter, bi-directional buck and boost converter.]

2.1 Introduction

Switch-mode DC-DC converters are used to convert the unregulated DC input to a controlled DC output at a desired voltage level. Switch-mode DC-DC converters include buck converters, boost converters, buck-boost converters, Cuk converters and full-bridge converters, etc. Among these converters, the buck converter and the boost converter are the basic topologies. Both the buck-boost and Cuk converters are combinations of the two basic topologies. The full-bridge converter is derived from the buck converter. There are usually two modes of operation for DC-DC converters: continuous and discontinuous. The current flowing through the inductor never falls to zero in the continuous mode. In the discontinuous mode, the inductor current falls to zero during the time the switch is turned off. Only operation in the continuous mode is considered in this dissertation.

2.2 Buck Converter

A buck converter is a step-down DC to DC converter. This converter takes an input voltage source and step it down to a lower voltage. Switch-based regulators move energy from input to
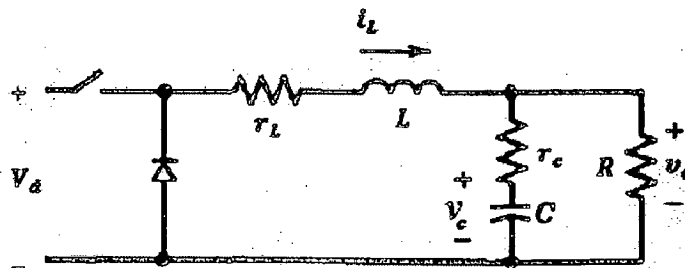
Fig 2.1: Buck Converter Circuit

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output in discrete packets via two or more switches. An inductor is used as the energy storage element that transfers energy from the input to the output of the power supply circuit.

2.2.1 Theory of Operation

During the interval when the switch is on, the diode in Fig.2.1 becomes reverse biased and the input provides energy to the load as well as to the inductor. During the interval when switch is off, the inductor current flows through the diode, transferring some of its stored energy to the load. . The output voltage is controlled by varying the duty cycle. During steady state, the ratio of output voltage over input voltage is (D), which is given by

$$\frac{V_{out}}{V_{in}} = D \qquad (2.1)$$

2.2.2 Continuous Mode

A buck converter operates in continuous mode if the current through the inductor (I_L) never falls to zero during the commutation cycle.

$$L > \frac{V_{out}}{2I_{out}f} \qquad (2.2)$$

2.2.3 Discontinuous Mode

A buck converter operates in discontinuous mode if the current through the inductor (I_L) falls to zero during the commutation cycle.

2.3 Boost Converter

A boost converter (step-up converter) is a power converter with an output DC voltage greater than its input DC voltage. It is a class of switching-mode power supply (SMPS) containing at least two semiconductor switches (a diode and a transistor) and at least one energy storage element. Filters made of capacitors (sometimes in combination with inductors) are normally added to the output of the converter to reduce output voltage ripple.

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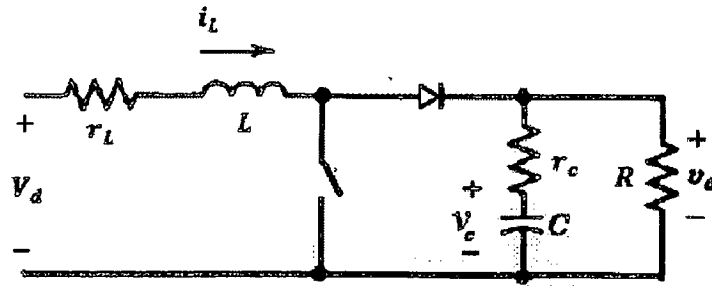
Fig 2.2: Boost Converter Circuit

2.3.1 Theory of Operation

When the switch is on, the diode is reversed biased, thus isolating the output stage. The input supplies energy to the inductor. When the switch is off, the output stage receives energy from the inductor as well as from the input. The output voltage is controlled by varying the duty cycle. During steady state, the ratio of output voltage over input voltage is (1-D), which is given by

$$\frac{V_{in}}{V_{out}} = 1 - D \qquad (2.3)$$

2.3.2 Continuous Conduction Mode (CCM):

In continuous conduction mode inductor current is continuous. The continuous conduction mode depends up on value of inductor. If the value of inductor is greater than that of critical inductance value then we say that converter under continuous conduction mode.

$$L > \frac{DT(1-D)^2R}{2} \qquad (2.4)$$

2.3.3 Discontinuous Conduction Mode (DCM):

In this mode of operation inductor current is discontinuous. If the inductance value is less than critical inductance then it is in discontinuous conduction mode.

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2.4 Bi-directional DC-DC buck & boost converter

A converter which can transfer power in two directions i.e. take or give power is called bi-directional converter. Now we will discuss about the basic structure and function of the bi-directional buck & boost converter.
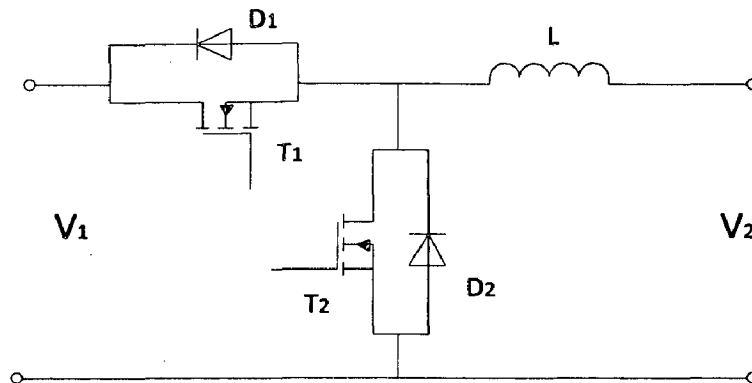
Fig 2.3: Bi-directional buck and boost converter (V_1>V_2).

A bidirectional buck and boost converter is shown in Figure 2. In this circuit, both switches are composed of a transistor and an antiparallel diode. They can conduct current in both directions, but can support the voltage in only one direction. In other words, the switches are bidirectional for the current and unidirectional for the voltage. These are two-quadrant switches, which permit energy flow in both directions, from left to right, and vice versa.

2.4.1 Theory of Operation

This converter behaves as a two types of dc-dc converter. It depends on the direction of operation. In one direction, it behaves as buck converter and in other direction it behaves as boost converter.

2.4.2 Buck operation:

If a dc voltage source V_1 is connected in parallel with the capacitor C_1 and a load is connected in parallel with the capacitor C_2, the buck converter is obtained. In this case, the energy flows from left to right. The MOSFET (T_1) channel is used as a controllable switch and its antiparallel diode

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D_1 is permanently OFF, whereas the diode D_2 is used as a passive (naturally commutated) switch. The channel of the MOSFET (T_2) can be held permanently OFF or can be turned on by a driver, when the diode D_2 is ON. This buck operation is shown in the below Fig.2.4.
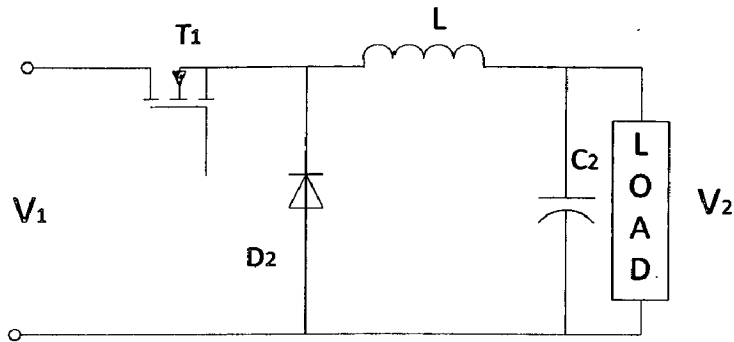
Fig 2.4: Buck operation of bi-directional converter

2.4.3 Boost operation

If a dc voltage source V_2 is connected in parallel with the capacitor C_2 and a load is connected in parallel with the capacitor C_1, the boost converter is obtained. In this case, the energy flows from right to left. The MOSFET (T_2) channel is used as a controllable switch and its antiparallel diode D_2 is permanently OFF, whereas the diode D_1 is used as a passive (naturally commutated) switch. The channel of the MOSFET (T_1) can be held permanently OFF or can be turned on by a driver, when the diode D_1 is ON. This boost operation is shown in the below Fig.2.5
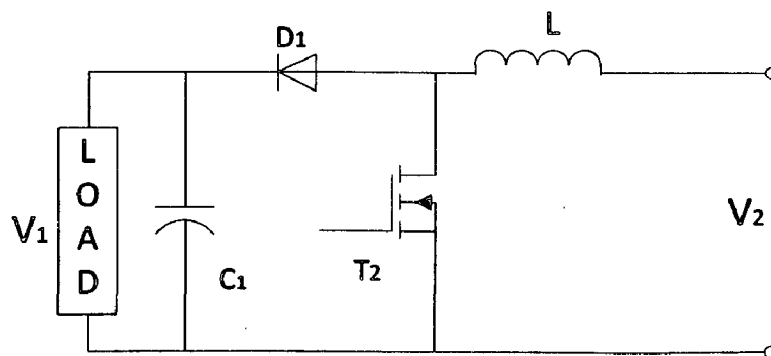
Fig 2.5: Boost operation of bi-directional converter.

CHAPTER-III

CONTROL TECHNIQUES

[Presented in this chapter are the control techniques, stability criteria, types of compensation for DC-DC converters for closed loop control.]

3.1 Introduction to closed loop control

The buck & boost converters can be controlled in two ways, known as:

1. Constant-frequency operation or pulse-width modulation control
2. Variable-frequency operation or control by frequency modulation

With pulse-width modulation control, the regulation of output voltage is achieved by varying the duty cycle of the switch, keeping the frequency of operation constant. Duty cycle refers to the ratio of the period for which the power semiconductor is kept ON to the cycle period. Usually control by pulse width modulation is the preferred method since constant frequency operation leads to optimization of LC filter and the ripple content in output voltage can be controlled within the set limits. On the other hand, if the load on the converter is below a certain level, voltage regulation of output becomes a problem and in such a case, control by frequency modulation is to be preferred. When control by frequency modulation is to be achieved, the ON period of the power semiconductor switch is kept constant and the frequency of operation is varied to effect voltage regulation. Design of LC filter is not easy in such a case.

3.2 Control requirements and techniques

A power supply should be designed to [4]:

1. Have good line regulation, such that output remains constant, if the input voltage varies.
2. Have good load regulation, such that the output remains constant, if the load changes.
3. Have good transient response to system disturbances, such a sudden changes to the input voltage, or to the load.
4. Remain stable under all operating conditions.

The above requirements are met by designing a feedback control system, which will control the duty ratio, of the transistor to keep the output all the times.

The output voltage of a switch mode power supply is kept constant with the help of closed loop control. The value of the output voltage (actual value) is compared with a reference voltage (nominal voltage). The difference between actual and nominal value controls the duty cycle of the transistor drive. The function of the control loop is to regulate the variation of the mains and of the change of the output current. This is called line regulation and load regulation.

There are two different methods of regulation:

* Voltage-mode
* Current-mode control.

The voltage-mode control is the "traditional" method of regulation.
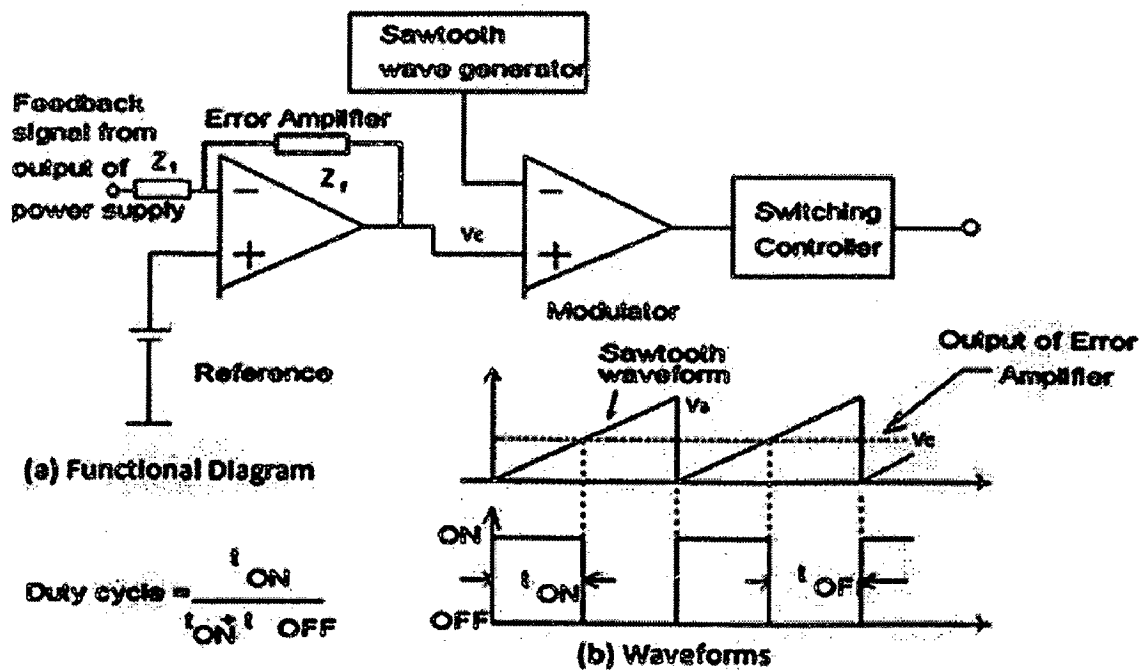
Fig 3.1: Voltage-mode control

The simplified functional diagram of a typical pulse-width modulator is shown in Fig, whereas the waveforms in Fig explain the operation. The pulse-width modulator circuit consists of a saw-tooth generator, an error amplifier, and a comparator. The error amplifier compares the reference

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voltage and the feedback signal. The feedback signal is obtained using a voltage divider network across the output of the SMPS circuit.

The output of the error amplifier is compared with the saw-tooth waveform and when this voltage is greater than the output of saw tooth generator, the output of the comparator would be at logic '1'. When the output of comparator is at logic '1', the switch in the SMPS circuit can be kept in the ON state. When the comparator is at logic '0', the switch in the SMPS circuit can be kept in the OFF state. If the output voltage tends to be greater than the ref voltage, the output voltage of the error amplifier would fall and the duration for which the output of comparator remains at logic '1' would decrease.

$$D= (t_{on}/T) = V_o/V_s$$

Thus the duty cycle of the switch reduces and the output of the SMPS would fall. Thus it can be seen that the negative feedback control maintains the output at the desired value.

3.3 Stability Criteria

It is the desire of all designers of power supplies, whether they are switching or not, for accurate and tight regulation of the output voltage. To accomplish regulation we need to add a feedback loop. The feedback loop can cause an otherwise stable system to become unstable. Even though the transfer function of the original converter might not contain any right hand poles but after feedback it is possible that right hand poles may be introduced.

There are three important points to be followed for the system to be stable. They are:

- The first criterion was that the total phase shift at the crossover frequency (frequency where total open-loop gain is unity or 0 dB) should be short of 360° by the "phase margin," which is usually taken as at least 45°.

- The second criterion for a stable circuit is that to prevent rapid changes of phase shift with frequency characteristic of a circuit with a - 2 gain slope, the slope of the open-loop gain-frequency curve of the entire circuit (arithmetic sum in decibels of all the gain elements involved) as it passes through crossover frequency should be − 1 gain slope.

- The third criterion for a stable loop is to provide the desired phase margin, which will be set at 45° herein. To satisfy all three criteria, it is necessary to know how to calculate gains and phase shifts of all the elements.

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We have to design the error amplifier (compensator) satisfying the above stability criteria for the analog controller.

3.4 Compensator (error amplifier)

There are three types of compensation or error amplifier for the stabilizing the analog circuit based on the requirement. They are Type I, Type II &Type III. In most cases, a Type II or Type III compensated network will properly compensate the system [6].

3.4.1 Type I Compensation

Dominant pole compensations, or single pole compensation, are referred to as a Type I Compensation. This type of compensation is used for converter topologies that exhibit a minimal phase shift prior to the anticipated gain crossover point. This compensation yields, though, a relatively poor transient response time because the gain crossover frequency occurs at a low frequency. Its load regulation is very good, though, since its DC gain is very high.
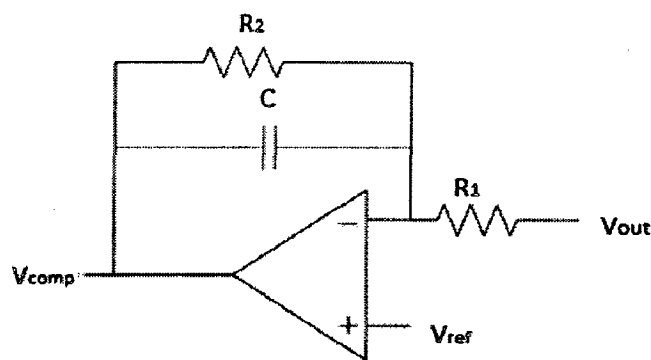
Fig.3.2: Type I Compensation

3.4.2 Type II Compensation:

The Type II network helps to shape the profile of the gain with respect to frequency and also gives a 90° boost to the phase. This boost is necessary to counteract the effects of the resonant output filter at the double pole.
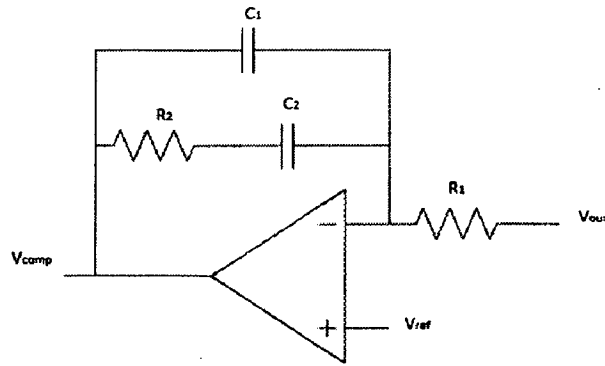
Fig 3.3: Type II Compensation

3.4.3 Type III Compensation:

Type III network shapes the profile of the gain with respect to frequency in a similar fashion to the Type II network, but utilizes two zeroes to give a phase boost of 180°. This boost is necessary to counteract the effects of an under damped resonance of the output filter at the double pole. The Type III compensation circuit has two poles, with two zeros and a pole at its origin providing an integration function for better DC accuracy. Optimal selection of the compensation circuit depends on the power-stage frequency response [11].
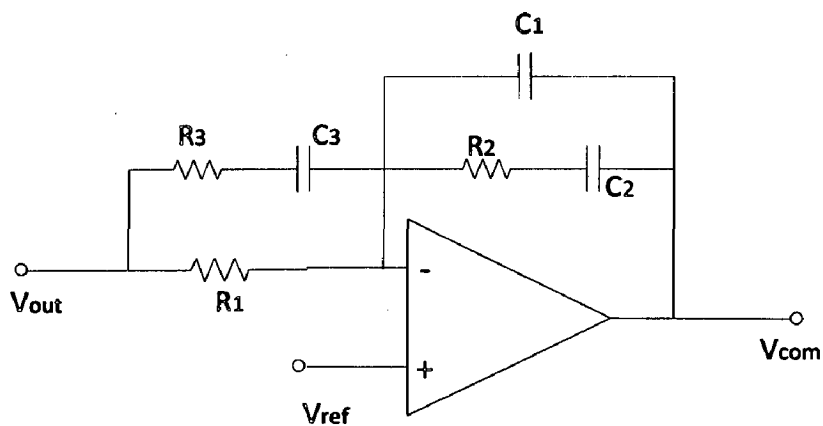
Fig 3.4: Type III Compensation

CHAPTER-IV

Design and Implementation of Bi-directional Buck and Boost Converter Using Analog Controller

[Presented in this chapter is the control design for DC-DC converters using linear control methods. An accurate model is essential to design linear controllers. Small signal models for buck and boost converters were obtained using the standard state-space averaging techniques. Modeling and implementation of buck, boost and bi-directional buck/boost converter are also discussed.]

4.1 State-Variable Description for Each Circuit State

In a converter operating in a continuous-conduction mode, there are two circuit states: one state corresponds to when the switch is on and the other to when the switch is off. A third circuit state exists during the discontinuous interval, which is not considered in the following analysis because of the assumption of a continuous conduction mode of operation.

During each circuit state, the linear circuit is described by means of the state variable vector x consisting of the inductor current and the capacitor voltage. In the circuit description, the parasitic elements such as the resistance of the filter inductor and the equivalent series resistance (ESR) of the filter capacitor should also be included. Here V_d is the input voltage. A lowercase letter is used to represent a variable, which includes its steady-state dc value plus a small ac perturbation, for example,

$$v_o = V_o + \hat{v}_o \qquad (4.1)$$

Therefore, during each circuit state, we can write the following state equations:

$$\dot{x} = A_1 x + B_1 v_d \qquad \text{during } d.T_S$$

and

$$\dot{x} = A_2 x + B_2 v_d \qquad \text{during } (1 - d).T_S \qquad (4.2)$$

where A1 and A2 are state matrices and B1 and B2 are vectors.

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The output v_o in all converters can be described in terms of their state variables alone as

$$v_0 = C_1 x \qquad \text{during } d.T_S$$

and

$$v_0 = C_2 x \qquad \text{during } (1-d).T_S \qquad (4.3)$$

where C1 and C2 are transposed vector s

4.1.1 Averaging the State-Variable Description Using the Duty Ratio d

To produce an average description of the circuit over a switching period, the equations corresponding to the two foregoing states are time weighted and averaged, resulting in the following equations:

$$\dot{x} = (dA_1 + d'A_2)x + (dB_1 + d'B_2)v_d$$

$$v_o = (dC_1 + d'C_2)x \qquad (4.4)$$

4.1.2 Introducing Small ac Perturbations and Separation into ac and dc Components

Small ac perturbations, represented by "~", are introduced in the dc steady-state quantities (which are represented by the upper case letters).
Therefore,

$$x = X + \hat{x}(t)$$
$$v_o = V_o + \widehat{v_o}(t)$$
$$d = D + \hat{d}(t) \qquad (4.5)$$

In general, $v_d = V_d + \widehat{v_d}(t)$. However, in view of our goal to obtain the transfer function between voltage $\widehat{v_o}$ and the duty ratio $\hat{d}$, the perturbation $\widehat{v_d}$ is assumed to be zero in the input voltage to simplify our analysis. Therefore

$$v_d = V_d$$

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Using Eq. 4.5 in Eq 4.4 and recognizing that in steady state,

$$\dot{\hat{x}} = AX + BV_d + A\hat{x} + \{(A_1 - A_2)X + (B_1 - B_2)V_d\}\hat{d}$$
$$+\text{terms containing products of }\hat{x}\text{ and } \hat{d} \quad \text{(to be neglected)} \qquad (4.6)$$

Where

$$A = A_1 D + A_2(1 - D)$$

And

$$B = B_1 D + B_2(1 - D) \qquad (4.7)$$

The steady-state equation can be obtained from Eq.8.6 by setting all the perturbation terms and their derivatives to zero. Therefore, the steady-state equation is

$$AX + BV_d = 0 \qquad (4.8)$$

and therefore in Eq. 4.6

$$\dot{\hat{x}} = A\hat{x} + \{(A_1 - A_2)X + (B_1 - B_2)V_d\}\hat{d} \qquad (4.9)$$

Similarly, using Eqs.4.5 in Eq.4.4 results in

$$V_o + \hat{v_o} = C\hat{x} + CX + \{(C_1 - C_2)X\}\hat{d}$$

Where

$$C = C_1 D + C_2(1 - D) \qquad (4.10)$$

In Eq. 4.10, the steady-state output voltage is given as

$$V_o = CX \qquad (4.11)$$

and therefore,

$$\hat{v_o} = C\hat{x} + \{(C_1 - C_2)X\}\hat{d} \qquad (4.12)$$

Using Eqs.4.8 and 4.11, the steady-state dc voltage transfer function is

$$\frac{v_o}{v_d} = -CA^{-1}B \qquad (4.13)$$

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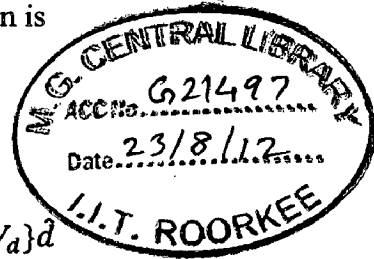
4.1.3 Transformation of the ac Equations in to s-Domain to Solve for the Transfer Function.

Equations 4.9 and 4.12 consist of the ac perturbations. Using Laplace transformation in Eq4.9,

$$s\hat{x}(s) = A\hat{x}(s) + \{(A_1 - A_2)X + (B_1 - B_2)V_d\}\hat{d}(s)$$

$$\hat{x}(s) = [sI - A]^{-1}\{(A_1 - A_2)X + (B_1 - B_2)V_d\}\hat{d}(s) \tag{4.14}$$

Where I is a unity matrix. Using a Laplace transformation in Eq.4.12 and expressing in terms $\hat{x}(s)$ in terms of $d(s)$ from Eq.4.14 results in the desired transfer function Tp(s) of the power stages:

$$T_p(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = C[sI - A]^{-1}\{(A_1 - A_2)X + (B_1 - B_2)V_d\} + (C_1 - C_2)X \tag{4.15}$$

4.2 Buck Converter Operation

Linearizing the power stage and the output filter of the Buck Converter given in Figure 4.1. The two switches are represented by diodes.

Fig 4.1: Buck Converter Circuit[1]

r_L is inductor resistance, r_c is the equivalent series resistance of the capacitor, and R is the load resistance.

Fig 4.2: Buck Converter (a) switch on; (b) switch off [1]

From Figure 4.2 the following equations can be derived

When switch is closed or ON

$$V_d = r_L i_L + L\frac{di_L}{dt} + R(i_L - C\frac{dv_c}{dt})$$ (4.16)

$$R\left(i_L - C\frac{dv_c}{dt}\right) = r_c C\frac{dv_c}{dt} + v_c$$ (4.17)

Using 4.16&4.17

$$\frac{dv_c}{dt} = \frac{Ri_L}{C(R+r_c)} - \frac{v_c}{C(R+r_c)}$$ (4.18)

When switch is open or OFF

$$V_d = 0$$

$$0 = r_L i_L + L\frac{di_L}{dt} + R(i_L - C\frac{dv_c}{dt})$$ (4.19)

$$R\left(i_L - C\frac{dv_c}{dt}\right) = r_c C\frac{dv_c}{dt} + v_c$$ (4.20)

When we consider ON condition

Sub Eq.4.21 in Eq.4.16 we get

$$\frac{di_L}{dt} = \frac{V_d}{L} - \left(\frac{r_L r_c + R r_L + r_c R}{L(R+r_c)}\right)i_L - \left(\frac{R}{R+r_c}\right)\frac{v_c}{L}$$ (4.21)

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Using eq.4.21 & eq.4.18 we can get matrices A_1, B_1, C_1, D_1 when switch is ON.

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} -\left(\frac{r_L r_c + R r_L + r_c R}{L(R+r_c)}\right) & -\left(\frac{R}{R+r_c}\right)\frac{1}{L} \\ \frac{R}{C(R+r_c)} & -\frac{1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_d \tag{4.22}$$

$$V_o = \begin{bmatrix} \frac{Rr_c}{(R+r_c)} & \frac{R}{(R+r_c)} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} \tag{4.23}$$

When switch is open or OFF $V_d = 0$,So $A_1 = A_2$, $B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$, $C_1 = C_2$. In all practical circuits $R \gg (r_c + r_L)$,now we get the final simplified matrices as.

$$A_1 = A_2 = \begin{bmatrix} -\left(\frac{r_L + r_c}{L}\right) & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR} \end{bmatrix} \tag{4.24}$$

$$B_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}, B_2 = 0 \tag{4.25}$$

$$C_1 = C_2 = \begin{bmatrix} r_c & 1 \end{bmatrix} \tag{4.26}$$

According to the state-space average methods the averaged matrices are

$$A = DA_1 + D'A_2$$
$$B = DB_1 + D'B_2$$
$$C = DC_1 + D'C_2$$
$$E = DE_1 + D'E_2 \tag{4.27}$$

Whereas D'=1-D. Here A=A_1, C=C_1, $B = B_1 D = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} D$.

the steady-state dc voltage transfer function is

$$\frac{V_o}{V_d} = -CA^{-1}B = D \tag{4.28}$$

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$$T_p(s) = \frac{\widehat{v_o}(s)}{\hat{d}(s)} = C[sI - A]^{-1}\{(A_1 - A_2)X + (B_1 - B_2)V_d\} + (C_1 - C_2)X$$

$$\Rightarrow C[sI - A]^{-1}B_1V_d$$

$$T_p(s) = \frac{\widehat{v_o}(s)}{\hat{d}(s)} = V_d \frac{1 + sr_cC}{LC\{s^2 + s\left[\frac{1}{CR} + \frac{(r_c + r_L)}{L}\right] + \frac{1}{LC}\}} \tag{4.26}$$

4.3 Boost Converter Operation

Linearizing the power stage and the output filter of the Boost Converter given in Figure 4.3. The complete diagram of the boost converter is given.
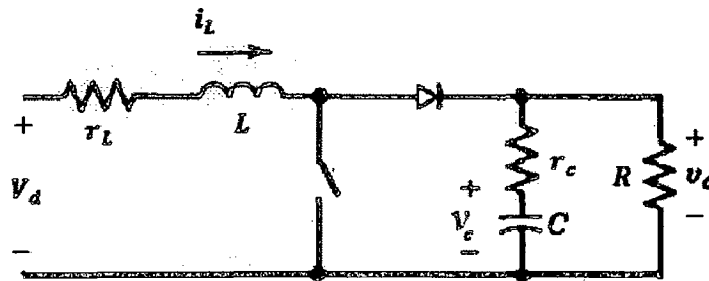
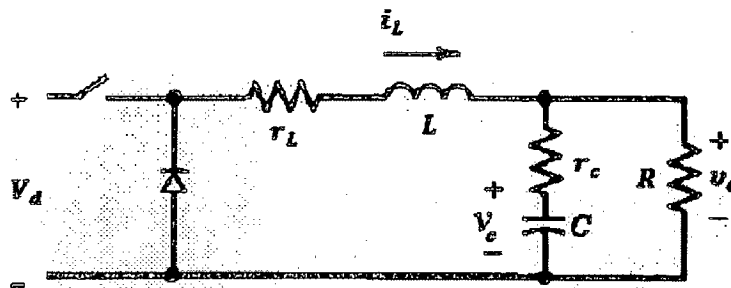Fig 4.3: Boost Converter Circuit

r_L is inductor resistance, r_c is the equivalent series resistance of the capacitor, and R is the load resistance.
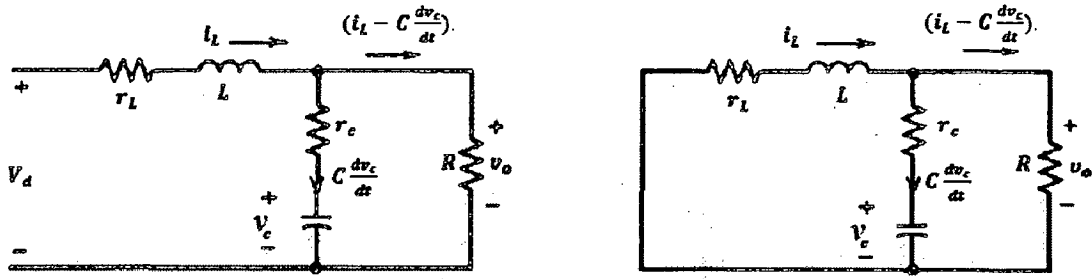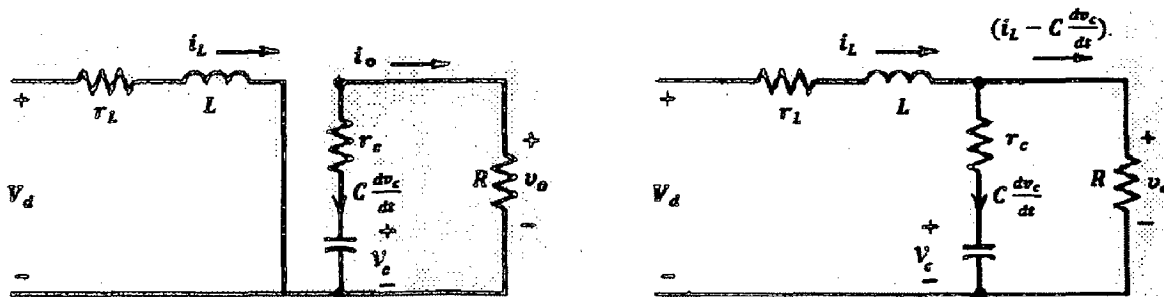

Fig 4.4: Boost Converter (a) switch on; (b) switch off [1]

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From Figure 4.4 the following equations can be derived

When switch is closed or ON

$$V_d = r_L i_L + L \frac{di_L}{dt}$$
(4.30)

$$V_o = r_c C \frac{dv_c}{dt} + v_c$$
(4.31)

$$V_o = -RC \frac{dv_c}{dt}$$
(4.32)

Sub Eq.4.32 in Eq.4.31 we get

$$\frac{dv_c}{dt} = -\frac{v_c}{(RC + r_c C)}$$
(4.33)

$$\frac{di_L}{dt} = \frac{V_d}{L} - \frac{r_L}{L} i_L$$
(4.34)

Using eq.4.33 & eq.4.34 we can get matrices A_1, B_1, C_1, D_1 when switch is ON.

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{r_L}{L} & 0 \\ 0 & -\frac{1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_d$$
(4.35)

$$V_o = \begin{bmatrix} 0 & \frac{R}{(R+r_c)} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix}$$
(4.36)

When switch is open or OFF

$$V_d = r_L i_L + L \frac{di_L}{dt} + R(i_L - C \frac{dv_c}{dt})$$
(4.37)

$$R \left(i_L - C \frac{dv_c}{dt} \right) = r_c C \frac{dv_c}{dt} + v_c$$
(4.38)

$$\frac{dv_c}{dt} = \frac{R i_L}{C(R+r_c)} - \frac{v_c}{C(R+r_c)}$$
(4.39)

Sub Eq.4.39 in Eq.4.37 we get

$$\frac{di_L}{dt} = \frac{V_d}{L} - \left(\frac{r_L r_c + R r_L + r_c R}{L(R+r_c)} \right) i_L - \left(\frac{R}{R+r_c} \right) \frac{v_c}{L}$$
(4.40)

Using eq.4.39 & eq.4.40 we can get matrices A_2, B_2, C_2, D_2 when switch is OFF.

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$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} -\left(\frac{r_L r_c + R r_L + r_c R}{L(R+r_c)}\right) & -\left(\frac{R}{R+r_c}\right)\frac{1}{L} \\ \frac{R}{C(R+r_c)} & -\frac{1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_d \qquad (4.41)$$

$$V_o = \begin{bmatrix} \frac{R r_c}{(R+r_c)} & \frac{R}{(R+r_c)} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} \qquad (4.42)$$

In all practical circuits $R \gg (r_c + r_L)$,now we get the final simplified matrices as.

$$A_1 = \begin{bmatrix} -\frac{r_L}{L} & 0 \\ 0 & -\frac{1}{CR} \end{bmatrix}$$

$$B_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}$$

$$C_1 = \begin{bmatrix} 0 & 1 \end{bmatrix}$$

$$A_2 = \begin{bmatrix} -\left(\frac{r_L + r_c}{L}\right) & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR} \end{bmatrix}$$

$$B_2 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}$$

$$C_2 = \begin{bmatrix} r_c & 1 \end{bmatrix} \qquad (4.43)$$

According to the state-space average methods the averaged matrices are

$$A = DA_1 + D'A_2$$
$$B = DB_1 + D'B_2$$
$$C = DC_1 + D'C_2$$
$$E = DE_1 + D'E_2 \qquad (4.44)$$

Whereas D '=1-D.

the steady-state dc voltage transfer function is

$$\frac{V_o}{V_d} = -CA^{-1}B = \frac{1}{(1-D)} \qquad (4.45)$$

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$$T_p(s) = \frac{\widehat{v_o}(s)}{\widehat{d}(s)} = C[sI - A]^{-1}\{(A_1 - A_2)X + (B_1 - B_2)V_d\} + (C_1 - C_2)X$$

On solving we get[6]

$$T_p(s) = \frac{\widehat{v_o}(s)}{\widehat{d}(s)} = V_d \frac{(R+r_c)(sCr_c+1)\{-(sL+r_L)(R+r_c)+D'^2R^2\}}{P(s)\{D'R(D'R+r_c)+r_L(R+r_c)\}} RV_d \qquad (4.46)$$

Where,

$$P(s) = s^2 LC(R + r_c)^2 + s\{L(R + r_c) + r_L C(R + r_c)^2 + D'Rr_c C(R + r_c)\} + r_L(R + r_c) + D'R(D'R + r_c)$$

4.4 Pulse Width Modulator

In the direct duty ratio pulse-width modulator, the control voltage v_{ctr}(t), which is the output of the error amplifier, is compared with a repetitive waveform v_r (t) , which establishes the switching frequency f_s , as shown in the Figure 4.5. The control voltage v_{ctr}(t) consists of a dc component and a small ac perturbation component [13].

$$v_{ctr}(t) = V_{ctr} + \widehat{v_{ctr}}(t) \qquad (4.47)$$

Where $v_{ctr}(t)$ is in a range between zero and $_r V_r$, as shown in Figure . Here $v_{ctr}(t)$ is a sinusoidal ac perturbation in the control voltage at a frequency ω, where ω is much smaller than the switching frequency ω_s $(=2\pi f)$.
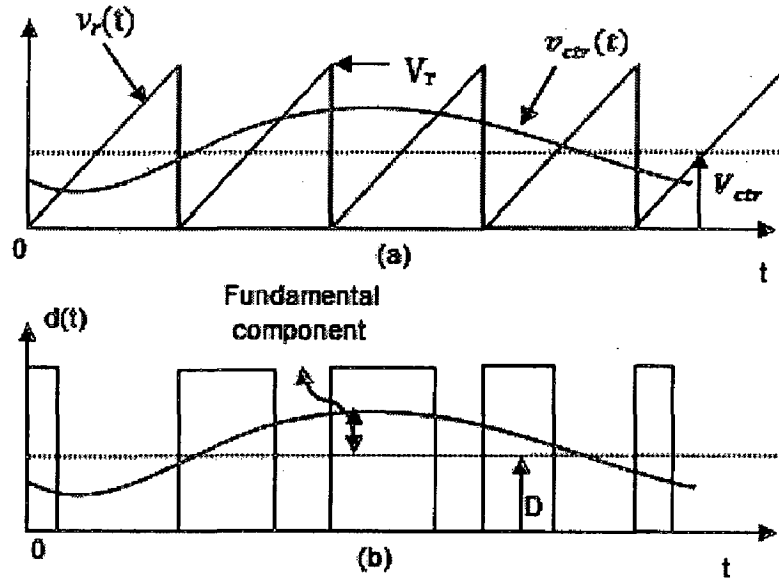
Fig 4.5: Pulse-width modulator

The ac perturbation in the control voltage can be expressed as

$$\widehat{v_{ctr}}(t) = a \sin(wt - \phi) \tag{4.48}$$

by means of an amplitude a and an arbitrary phase angle φ.

In Figure 4.5, the instantaneous switch duty ratio $d(t)$ is as follows:

$$d(t) = \begin{cases} 1 \\ 0 \end{cases} \tag{4.49}$$

The sinusoidal PWM can be expressed in terms of the Fourier series as

$$d(t) = \frac{V_{ctr}}{V_r} + \frac{a}{V_r} \sin(wt - \phi) + other\ high\ frequency\ components \tag{4.50}$$

The higher frequency components in the output voltage v_o due to the high frequency components in $d(t)$ are eliminated because of the low-pass filter at the output of the converter. Therefore, the high-frequency components in Eq.4.50 can be ignored. In terms of its dc value and its ac perturbation

$$d(t) = D + \hat{d}(t) \tag{4.51}$$

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Comparing Eq.4.50 and 4.51 yields,

$$D = \frac{V_{ctr}}{V_r}$$

and

$$\hat{d}(t) = \frac{a}{V_r} si\, n(wt - \phi) \tag{4.52}$$

From Eqs.4.48 and 4.52, the transfer function T_m (s) of the modulator is given by

$$T_m(s) = \frac{\hat{d}(s)}{\widehat{v_{ctr}}(s)} = \frac{1}{V_r} \tag{4.53}$$

4.5 Compensator

After the values for external filter components are chosen (according to our requirements) than only the power stage is complete. The original filter of the buck converter by itself has a very low phase margin which needs to be increased. A better phase margin can be included by adding a suitable controller in a closed loop configuration. Proper compensation of the system will allow for a predictable bandwidth with unconditional stability. In most cases, a Type II or Type III compensated network will properly compensate the system. The ideal Bode plot for the compensated system would be a gain that rolls off at a slope of -20dB/decade, crossing 0db at the desired bandwidth and a phase margin greater than 45° for all frequencies below the 0dB crossing[9] .

4.5.1 Type III Compensation

Figure 4.6, 4.7 shows a generic Type III compensation, its transfer function and asymptotic Bode plot. The Type III network, however, utilizes two zeroes to give a phase boost of 180 degrees. This boost is necessary to counteract the effects of an under damped resonance of the output filter at the double pole. The Type III compensation circuit has two poles, with two zeros and a pole at its origin providing an integration function for better DC accuracy. Optimal selection of the compensation circuit depends on the power-stage frequency response [15].

The guidelines for positioning the poles and zeroes and for calculating the component values are discussed below after the fig 4.6, 4.7.
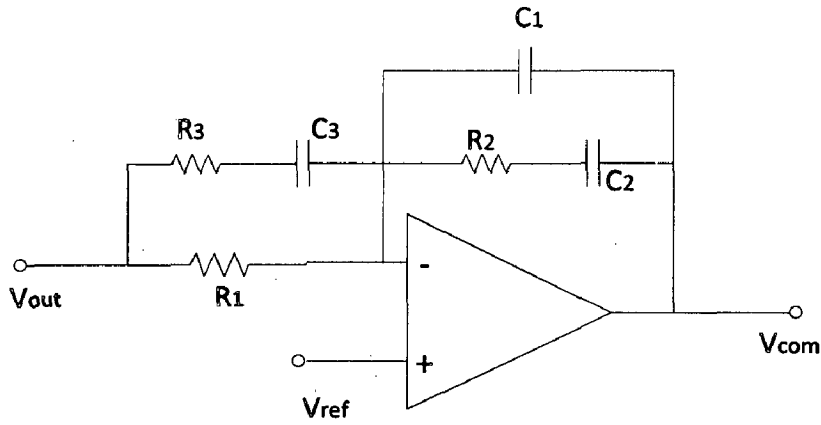
Fig 4.6: Type 3 compensation
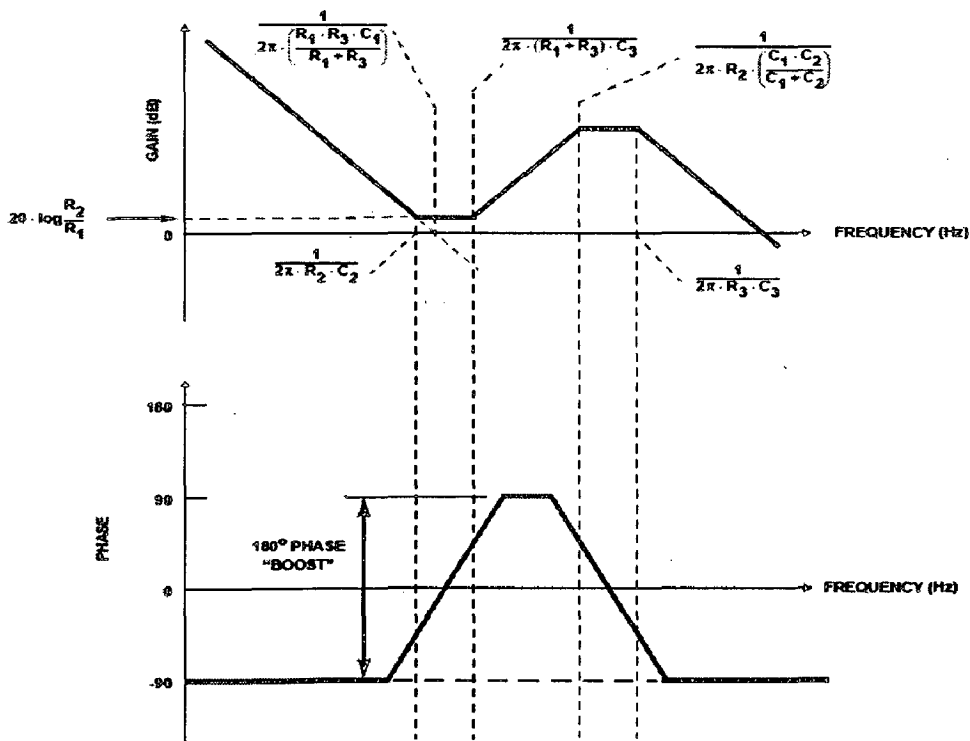
Fig 4.7: Behavior of Type 3 compensation

$$GAIN_{TYPE3} = \frac{R_1+R_3}{R_1R_3C_1} \frac{\left(s+\frac{1}{R_2C_2}\right)\left(s+\frac{1}{(R_1+R_3)C_3}\right)}{s\left(s+\frac{C_1+C_2}{R_2C_1C_2}\right)\left(s+\frac{1}{R_3C_3}\right)} \qquad (4.54)$$

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Choose a value for R_1, usually between 2k and 5kΩ.

Pick a gain (R_2/R_1) that will shift the Open Loop Gain up to give the desired bandwidth. This will allow the 0dB crossover to occur in the frequency range where the Type III network has its second flat gain. The following equation will calculate an R_2 that will accomplish this given the system parameters and a chosen R_1.

$$R_2 = \frac{DBW}{f_{LC}} * \frac{\Delta V_{osc}}{V_{in}} R_1$$

$$DBW = 0.3 * f_{LC}$$

$$f_{LC} = \frac{1}{2\pi\sqrt{(LC)}} \qquad (4.55)$$

1. Calculate C_2 by placing the zero at 50% of the output filter double pole frequency:

$$C_2 = \frac{1}{\pi R_2 f_{LC}} \qquad (4.56)$$

2. Calculate C_1 by placing the first pole at the ESR zero frequency:

$$C_1 = \frac{C_2}{2\pi R_2 C_2 f_{ESR} - 1}$$

$$f_{ESR} = \frac{1}{2\pi\sqrt{(r_C C)}} \qquad (4.57)$$

3. Set the second pole at half the switching frequency and also set the second zero at the output filter double pole. This combination will yield the following component calculations:

$$R_3 = \frac{R_1}{\frac{f_{sw}}{2f_{LC}} - 1}$$

$$C_3 = \frac{1}{\pi R_3 f_{sw}} \qquad (4.58)$$

It is recommended that the actual Gain and phase plots are generated through the use of a commercially available analytical software package that has the capability to plot.

The compensation gain must be compared to the open loop gain of the error amplifier. The compensation gain should not exceed the error amplifier open loop gain because this is the limiting factor of the compensation. In the analog design process, Type III compensator is used to compensate a second-order LC filter, usually from a voltage-mode converter.

4.6 Feedback Control System

The output voltages of dc power supplies are regulated to be within a specified tolerance band (e.g., ±1% around its nominal value) in response to changes in the output load and the input voltage lines [15]. This process is accomplished by employing a negative feedback system which can be seen in Figure 4.8.
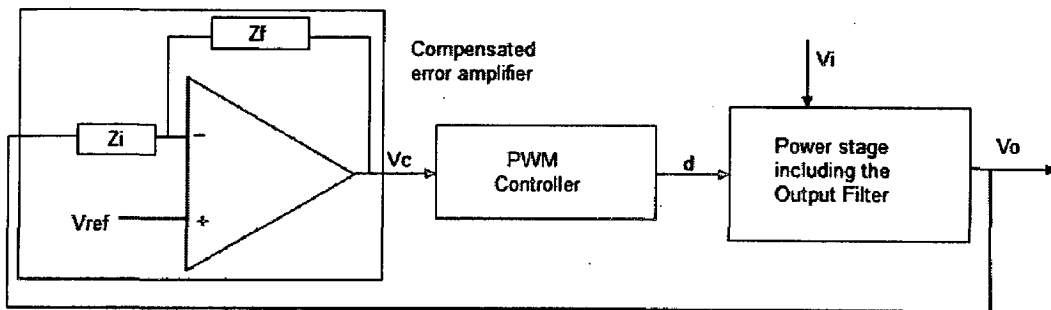
Figure 4.8: Feedback Control System

The Power stage of the switch converter is not linearized. Since nonlinear systems are not equal to the sum of their parts, they are often difficult (or impossible) to model, and their behaviour with respect to a given variable (for example, time) is extremely difficult to predict. When modelling non-linear systems, therefore, it is common to approximate them as linear, where possible.

With the Linear model, it will make possible certain mathematical assumptions and approximations, allowing for simple computation of results. In nonlinear systems these assumptions cannot be made.

If the power stage of the switch-mode converter in Figure 4.8 can be linearized, then the Bode plots can be used to determine the appropriate compensation in the feedback loop for the desired steady-state and transient response. Each block in Figure 4.8 can be linearized around a steady-state operating point as using the state-space averaging technique [20] which allowed the theoretical prediction of a converters frequency response, and therefore a better understanding of a switched-mode regulator's feedback loop and stability criteria.
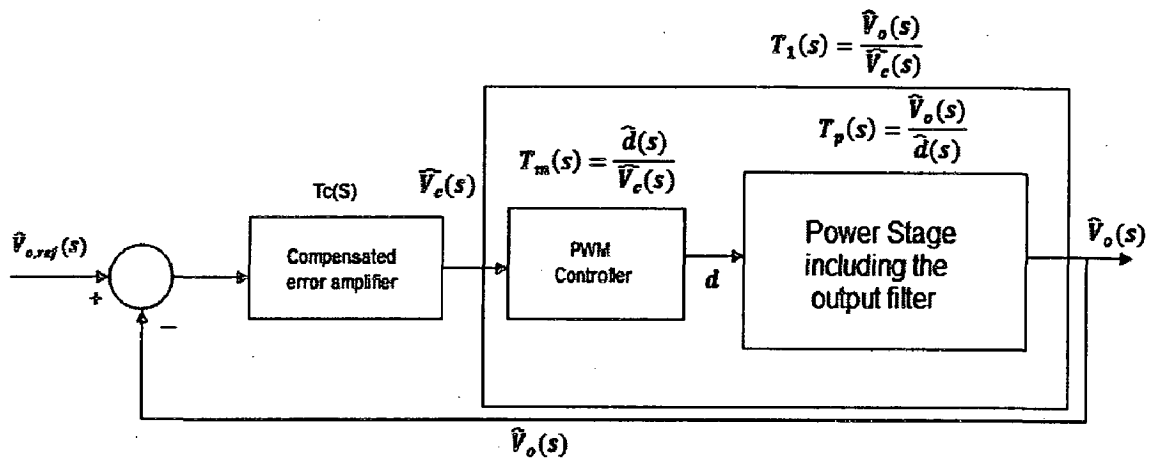
Fig 4.9: Linearized Feedback Control System

4.7 Simulation Results

4.7.1 Stability analysis of Buck Converter

The bode plot of the buck converter is drawn using the state-space average method with help of MATLAB. The bode plot helps to realize the stable operation under closed loop. The phase margin and gain margin decides the stability under closed loop [6].
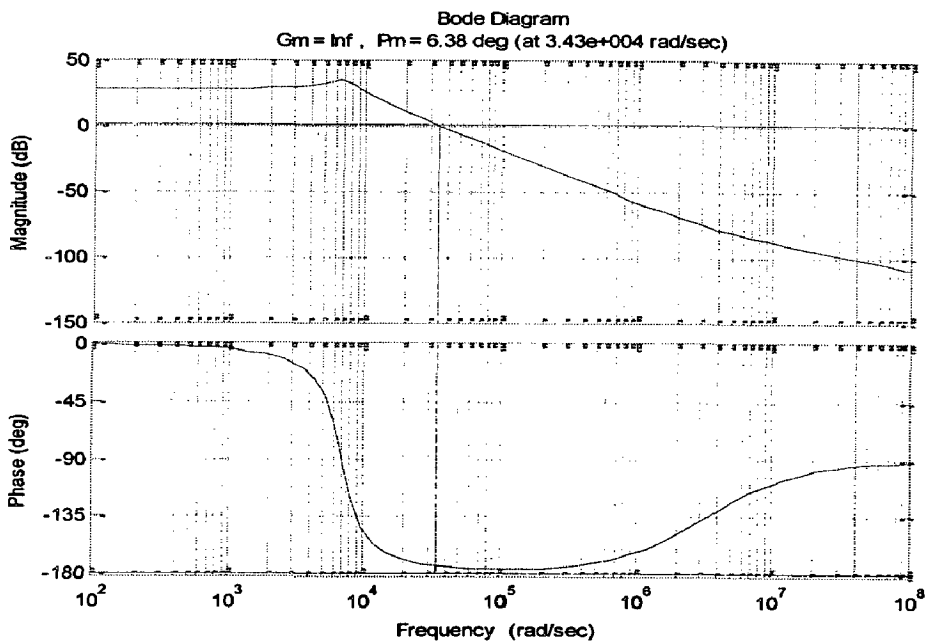
Fig 4.10: Bode plot of buck converter

The bode plot in fig 4.10 shows that the open loop phase margin of the buck converter is less than 45 deg, It doesn't provide satisfying conditions to add a feedback to this buck converter. So compensation circuit using error amplifier should be designed such that it will have the required phase margin i.e. between 45-65 deg. In order to provide necessary compensation type III error amplifier is designed. The parameter used for the design are given in appendix table A.1, A.2.
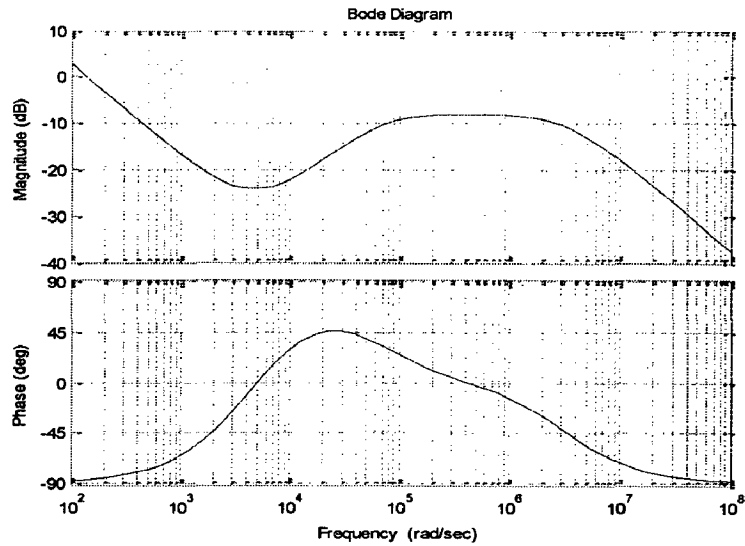
Fig 4.11: Bode plot of type3 compensation

Bode Diagram
Gm = Inf dB (at Inf rad/sec) , Pm = 63.2 deg (at 9.83e+003 rad/sec)
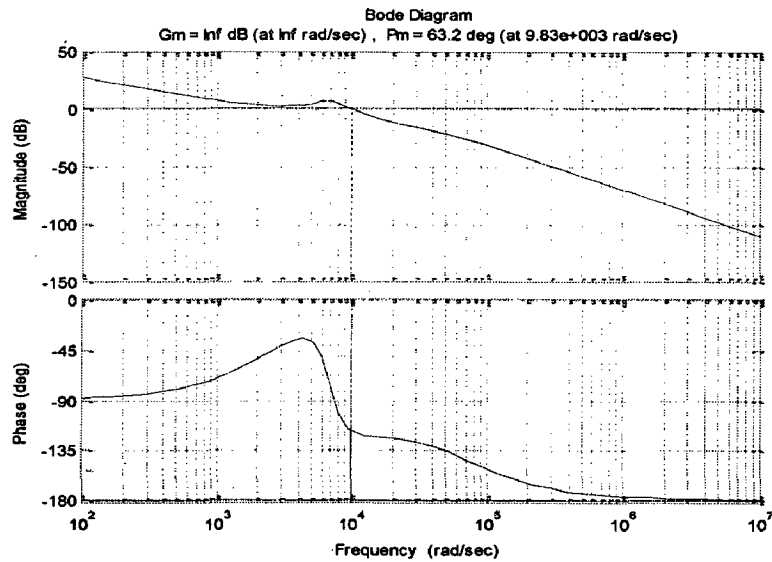
Fig 4.12: Bode plot of compensated open loop buck converter.

The bode plot of the type III error amplifier is shown in fig 4.11 whose gain is given in appendix (A.1). The steps to design the error amplifier are already discussed [15]. Now the designed compensator gain (4.54) should be multiplied with the buck converter gain (4.29) along with the PWM gain (4.53) in order to get the total open loop gain of the compensated buck converter. The bode plot of the compensated buck converter is shown in fig 4.12 and it clearly shows that the type three compensation has improved the phase margin of the open loop buck converter. It has

increased the phase margin from 7 deg to 57 deg. This gives the satisfying condition for the stable operation of closed loop control of the buck converter.

4.7.2 Simulation of a closed loop Buck Converter
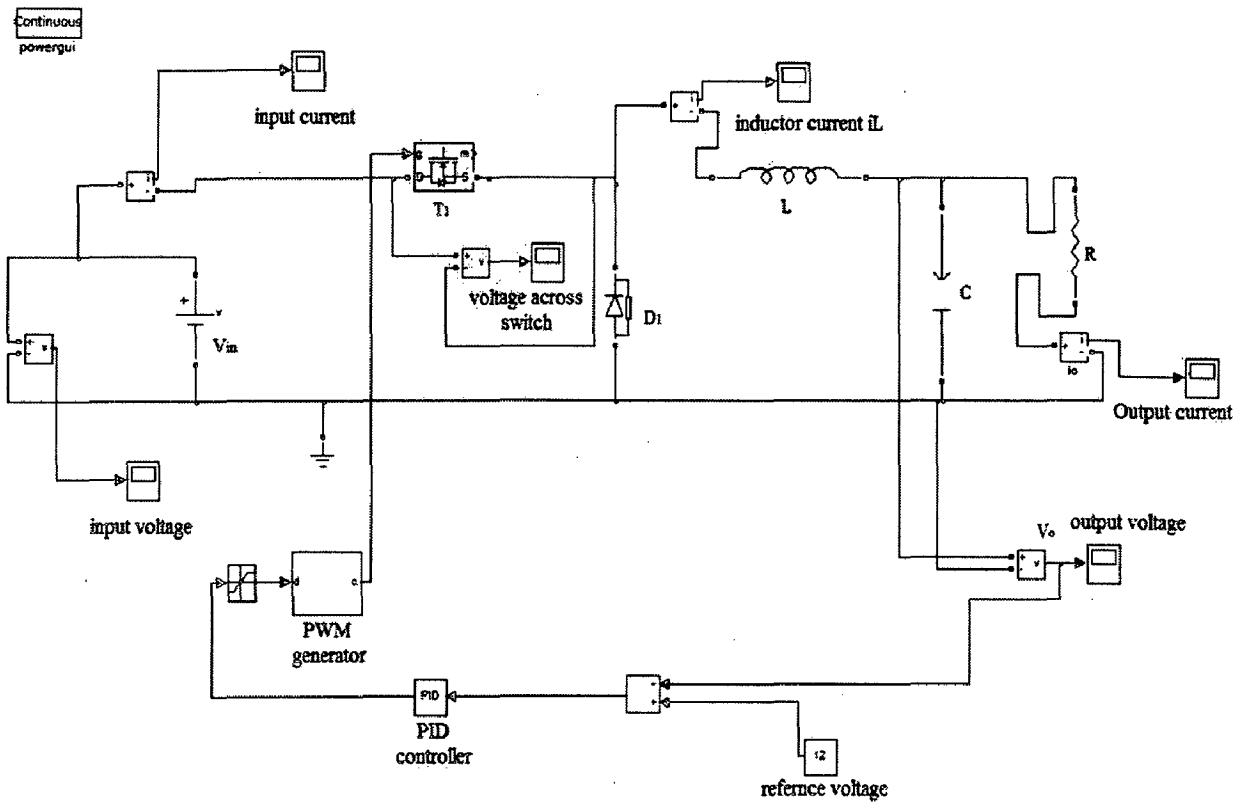
Fig 4.13: MATLAB simulation of buck converter.

Simulation model of the buck converter using the MATLAB SimPowerSystems is shown in fig 4.13. The PID controller is used and values of the PID are obtained by tuning. The results are shown in fig.4.14 and 4.15. It shows various parameters like I_{in}, V_{in}, V_{out}, V_{sw} etc. The input parameters used are shown in appendix table A.1. In fig 4.14 we can see how the controller is working. When supply voltage 24V is ON, the output voltage should be 12V. But the initial output voltage is 0V, so the controller takes the error voltage and increase the duty cycle such that the output voltage reaches 12V. Duty cycle remains constant as output voltage reaches 12V and as seen in fig 4.14 at 0.5. The fig 4.14 is the enlarged in fig 4.15 to see various wave forms of the buck

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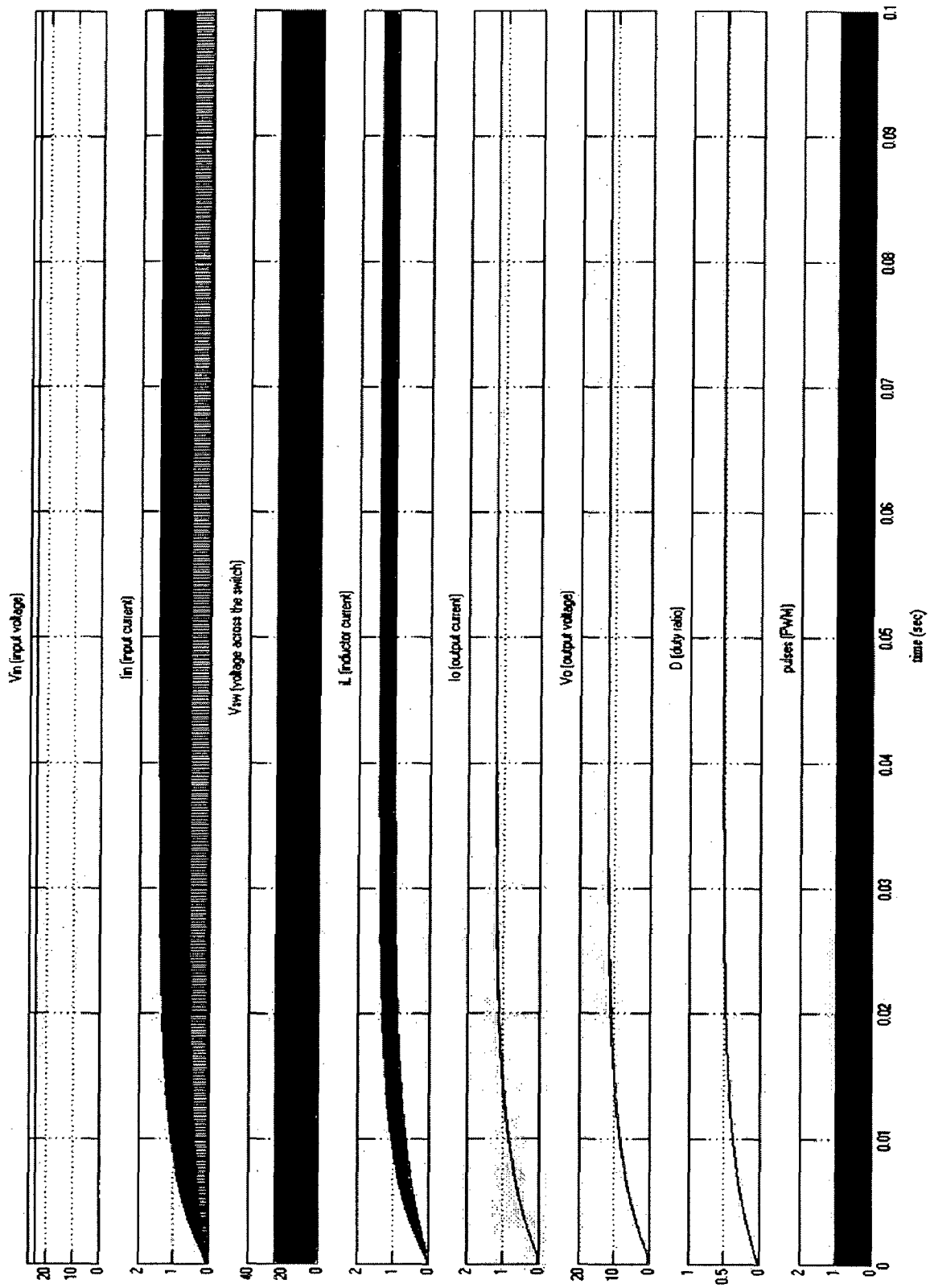
Fig 4.14: Simulation response of buck converter

Fig 4.14: Simulation response of buck converter

42
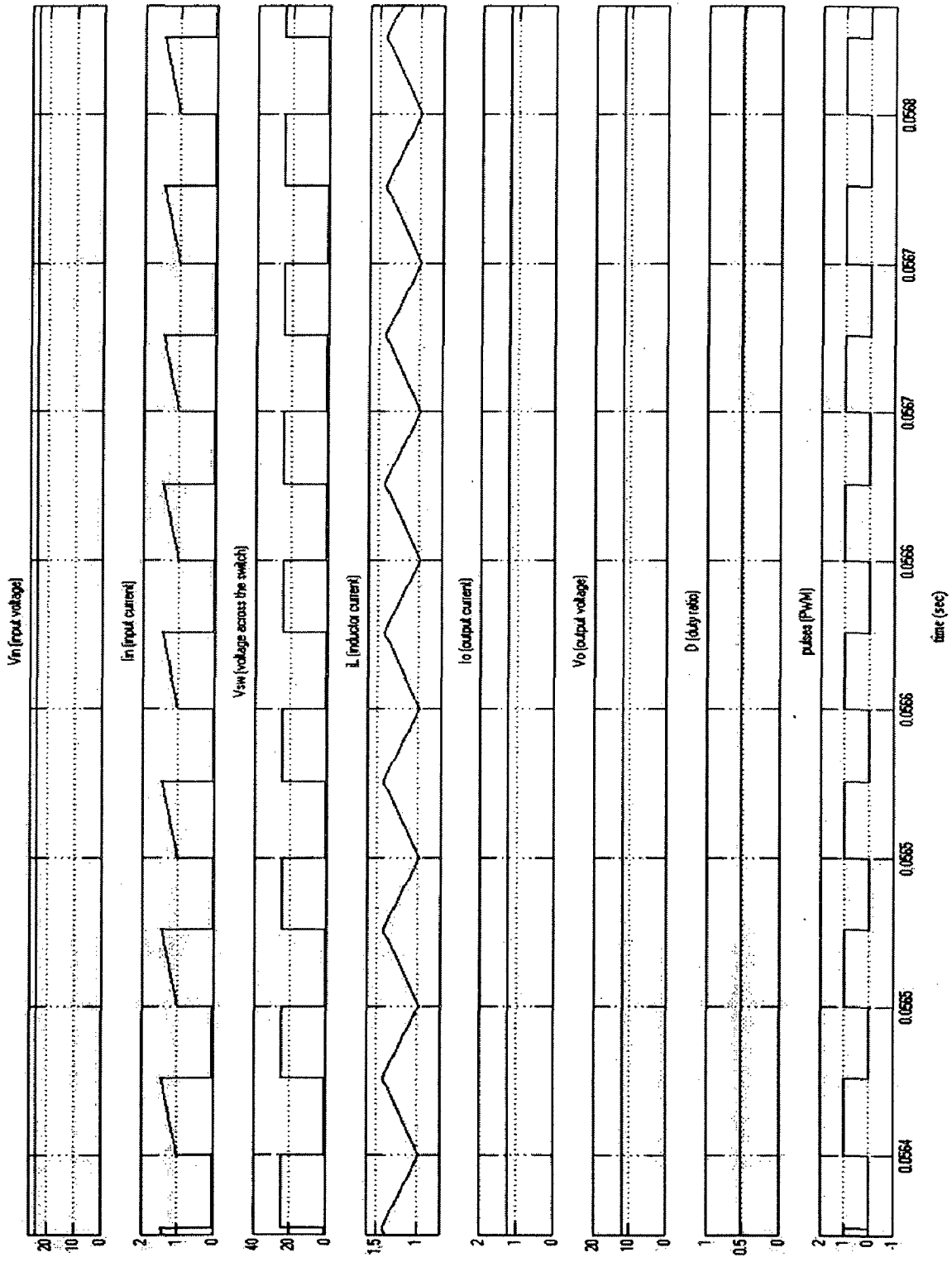
Fig 4.15: Simulation response of buck converter under steady state (enlarged view)

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converter under normal or steady state conditions. The pulses of 0.5 duty cycle are produced by the controller and given to the switch to get 12V output at 24V input. It also shows the continuous inductor current, voltage across the switch, input and output current wave forms. This gives complete details of the buck converter.

4.7.3 Closed loop Simulink model of Buck Converter with type III controller

Modeling of the buck converter is done in MATLAB Simulink using the state space average method. Various blocks for the closed loop control are shown in fig 4.16. Every block is designed using MATLAB Simulink. The designed type III compensator is used as a controller.

Fig 4.16: Closed loop Simulink model for buck converter

In place of the dc-dc converters buck converter model is placed which is shown in the fig.5.3. The type III compensator (A.1) which is designed previously is used in the TypeIII block and it acts as a controller. Variable input voltage and variable load is provided to the system to check the proper functioning of the controller. In fig 4.17 we can clearly see that the input voltage and load resistance is varied to see the effect on the output voltage and current. In buck converter the output current(I_o) is equal to the inductor current(i_L), so when the load resistance varies the I_o, i_L

44
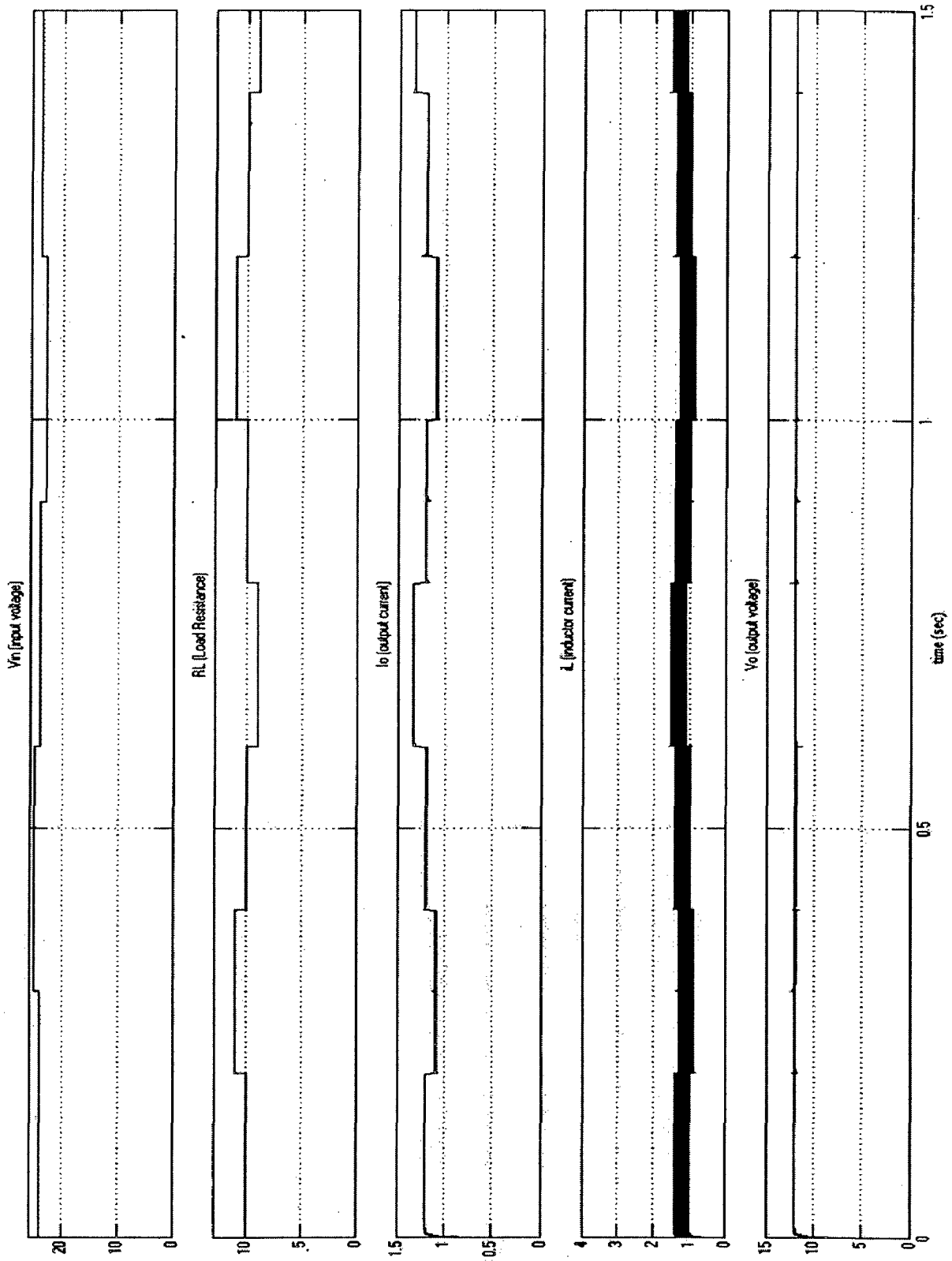
Fig.4.17: Closed loop response of Buck converter (V_{in} and R_L variation)

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varies accordingly i.e when R_L, increases I_o and i_L decreases, similarly when R_L decreases, I_o and i_L increases. But due the variation in the input voltage the I_o, i_L does not change except small disturbance during the transition of the input voltage because of small varioation in V_o. With variation in R_L and V_{in} the output voltage remains constant, this is done by the type III controller. Whenever the input voltage varies, the controller will adjust the duty cycle such that V_o remains constant. If the V_o has changed due to change in load then the controller adjusts the duty cycle such that V_o remains constant. So fig.4.17 shows that the designed type III controller is providing satisfactory results.

4.7.4 Stability analysis of Boost converter

The bode plot of the boost converter is drawn using the state-space average method with help of MATLAB. The bode plot helps to realize the stable operation under closed loop. The phase margin and gain margin decides the stability under closed loop [6].

Bode Diagram
Gm = -33.6 dB (at 2.93e+003 rad/sec) , Pm = -85 deg (at 5.77e+004 rad/sec)
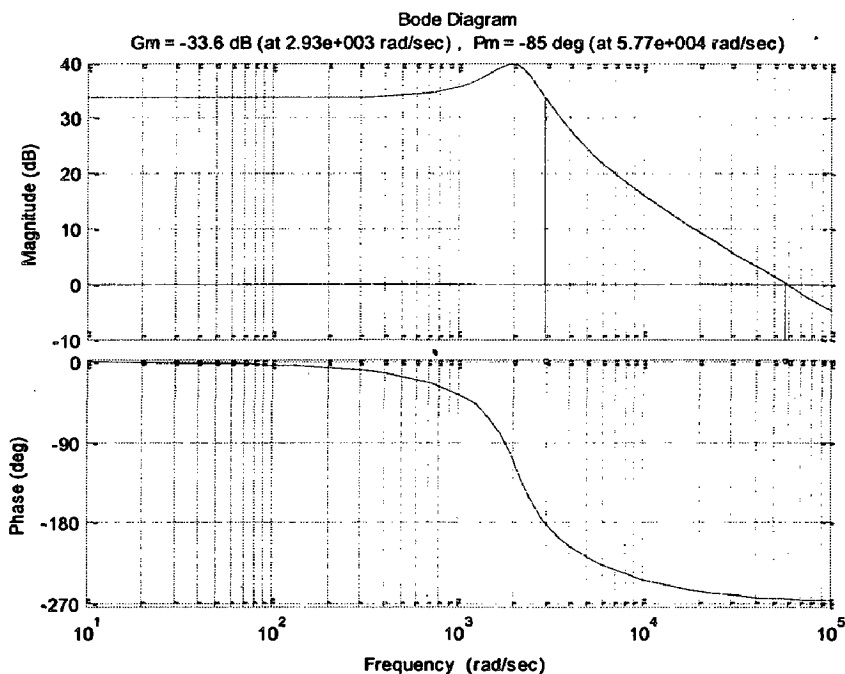
Fig 4.18: Bode plot of boost converter

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The bode plot in fig 4.18 shows that the open loop phase margin of the boost converter is -85 deg, which is less than 45 deg. It doesn't provide satisfying conditions to add a feedback to this boost converter. So compensation circuit using error amplifier should be designed such that we will have the required phase margin i.e. between 45-65 deg. In order to provide necessary compensation type III error amplifier is designed.
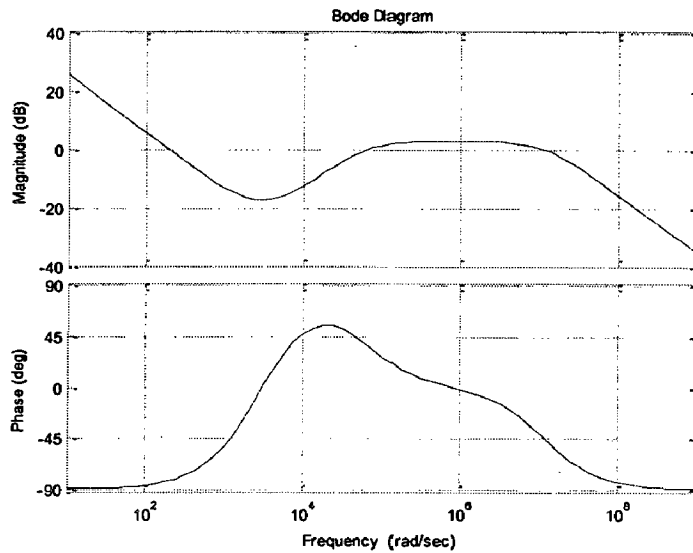
Fig 4.19: Bode plot of type3 compensation
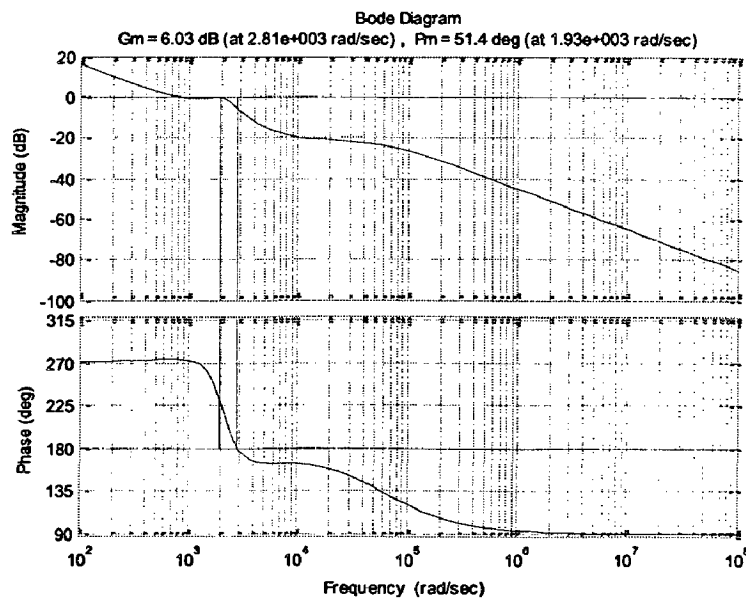
Fig 4.20: Bode plot of compensated open loop boost converter

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The parameter used for the design are given in appendix table A.1, A.2.The bode plot of the type III error amplifier is shown in fig 4.19 whose gain is (A.2). The steps to design the error amplifier are already discussed [11]. Now the designed compensator gain (4.54) should be multiplied with the boost converter gain (4.46) along with the PWM gain (4.53) in order to get the total open loop gain of the compensated boost converter. The bode plot of the compensated boost converter is shown in fig 4.20 and it clearly shows that the type three compensation has improved the phase margin of the open loop boost converter. It has increased the phase margin to 51.4 deg. This gives the satisfying condition for the stable operation of closed loop control of the boost converter.

4.7.5 Simulation of a closed loop boost converter
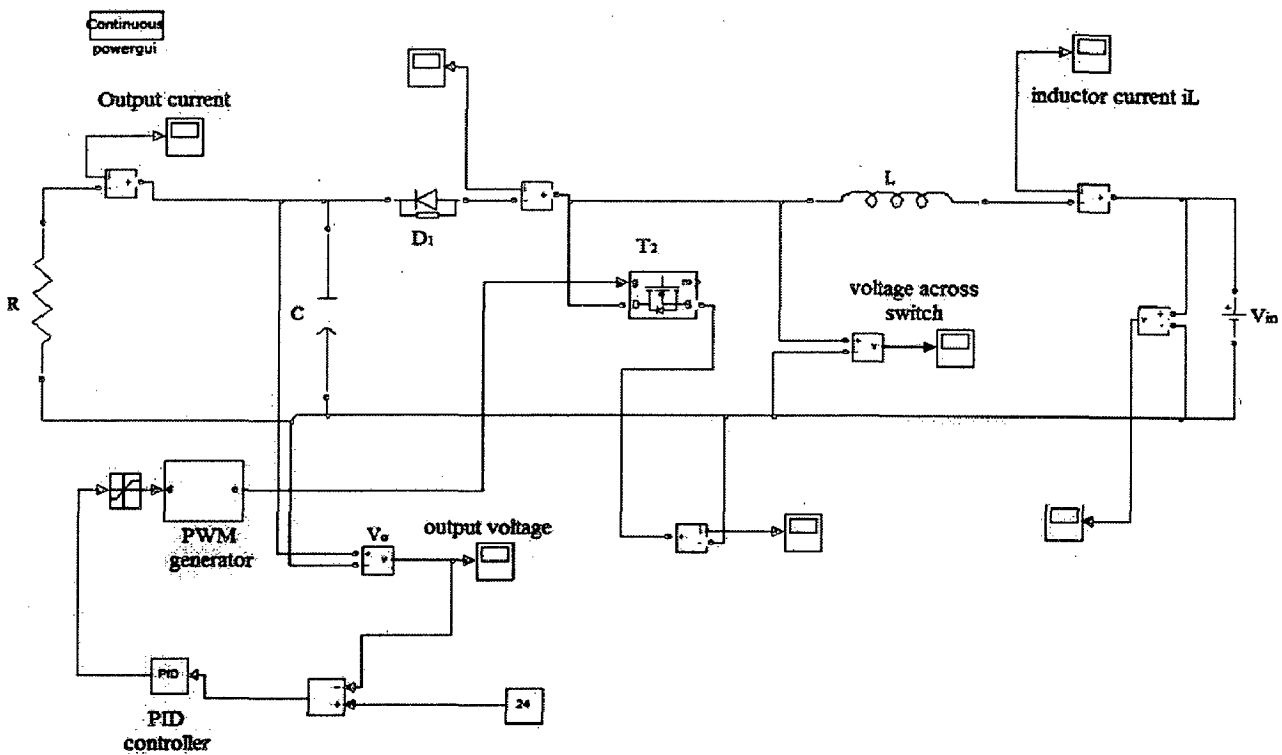
Fig 4.21: MATLAB simulation of boost converter.

Simulation model of the boost converter using the MATLAB SimPowerSystems is shown in fig 4.13. The PID controller is used and values of the PID are obtained by tuning. The results are

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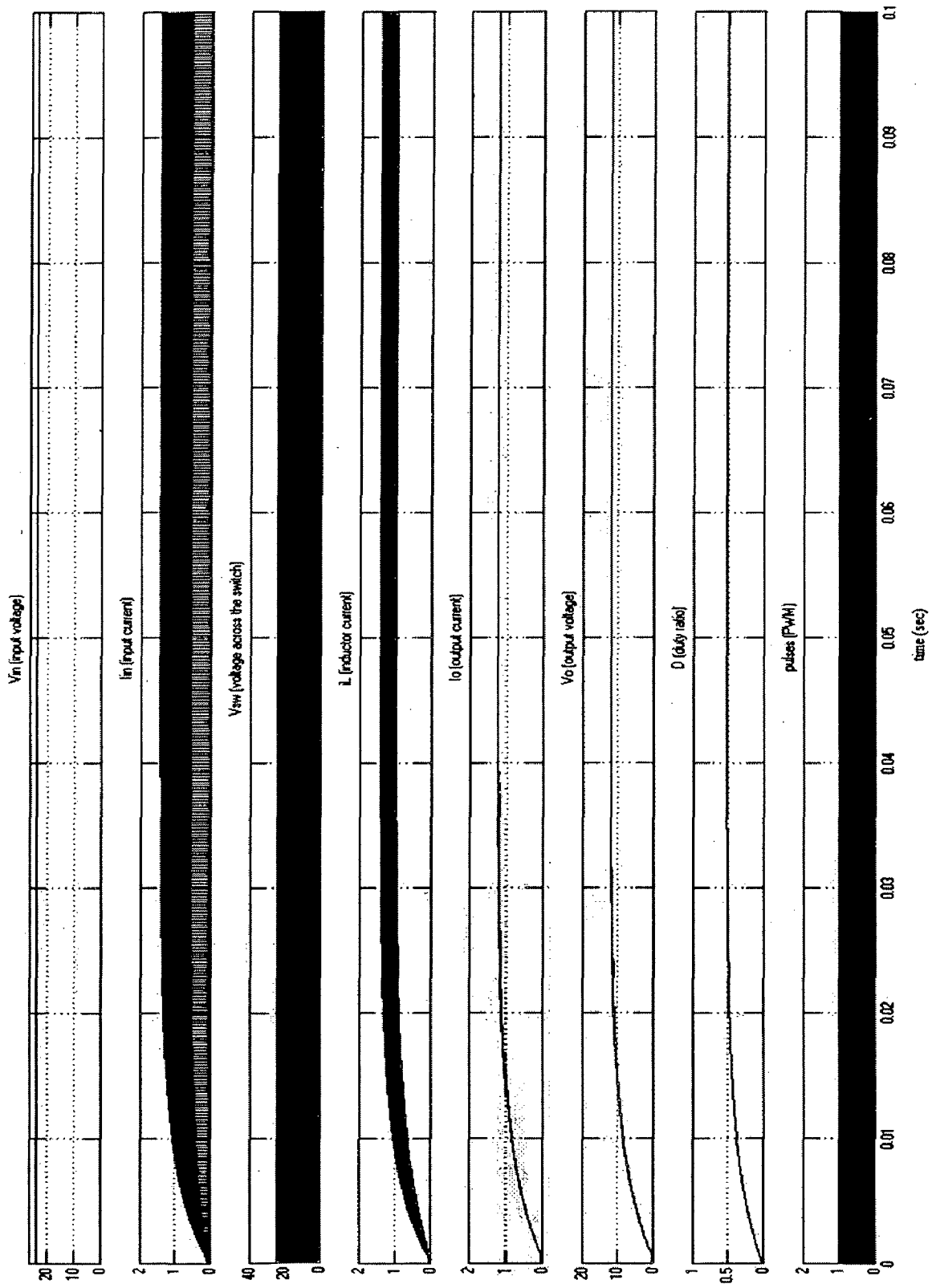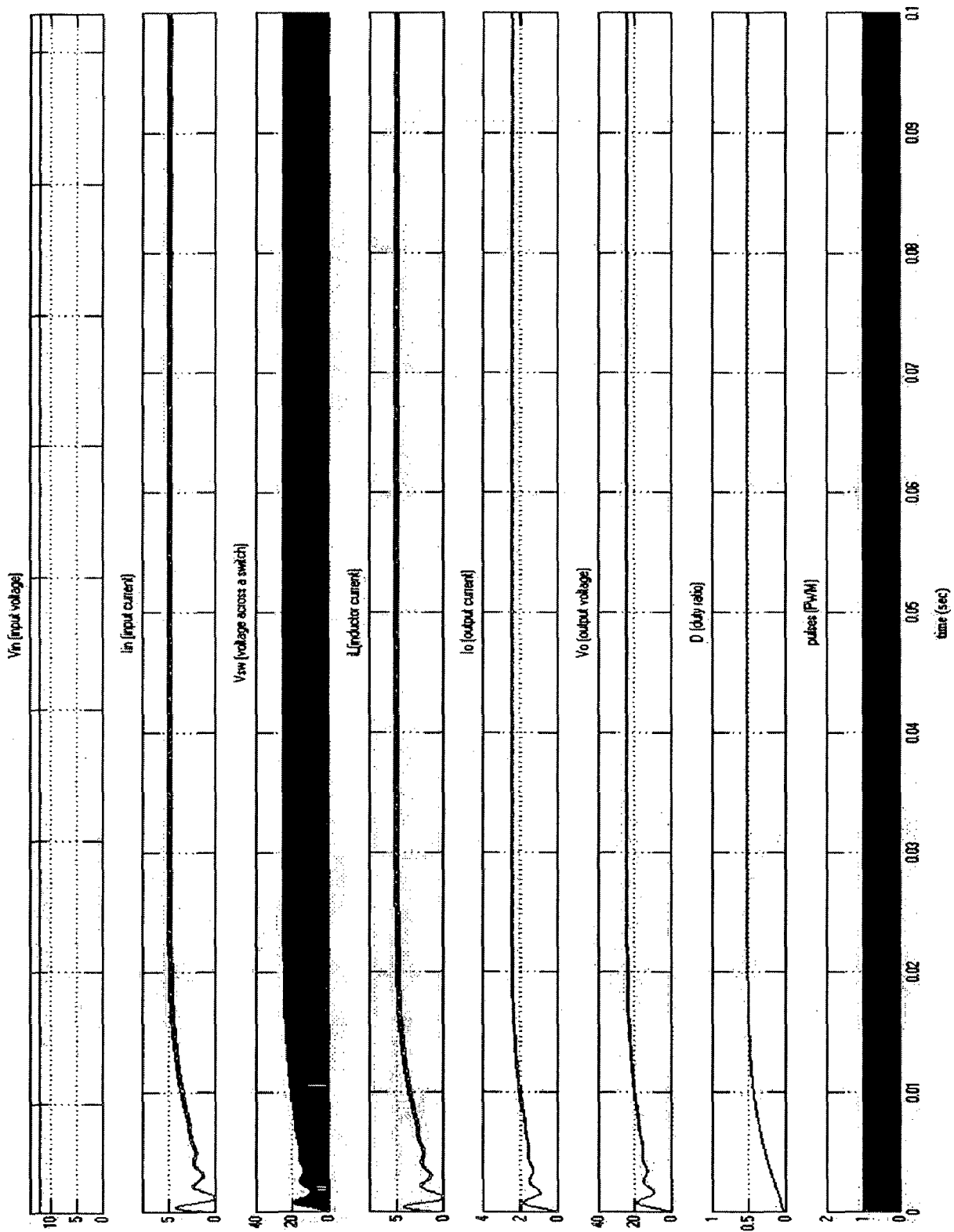
Fig 4.22: Simulation response of boost converter.
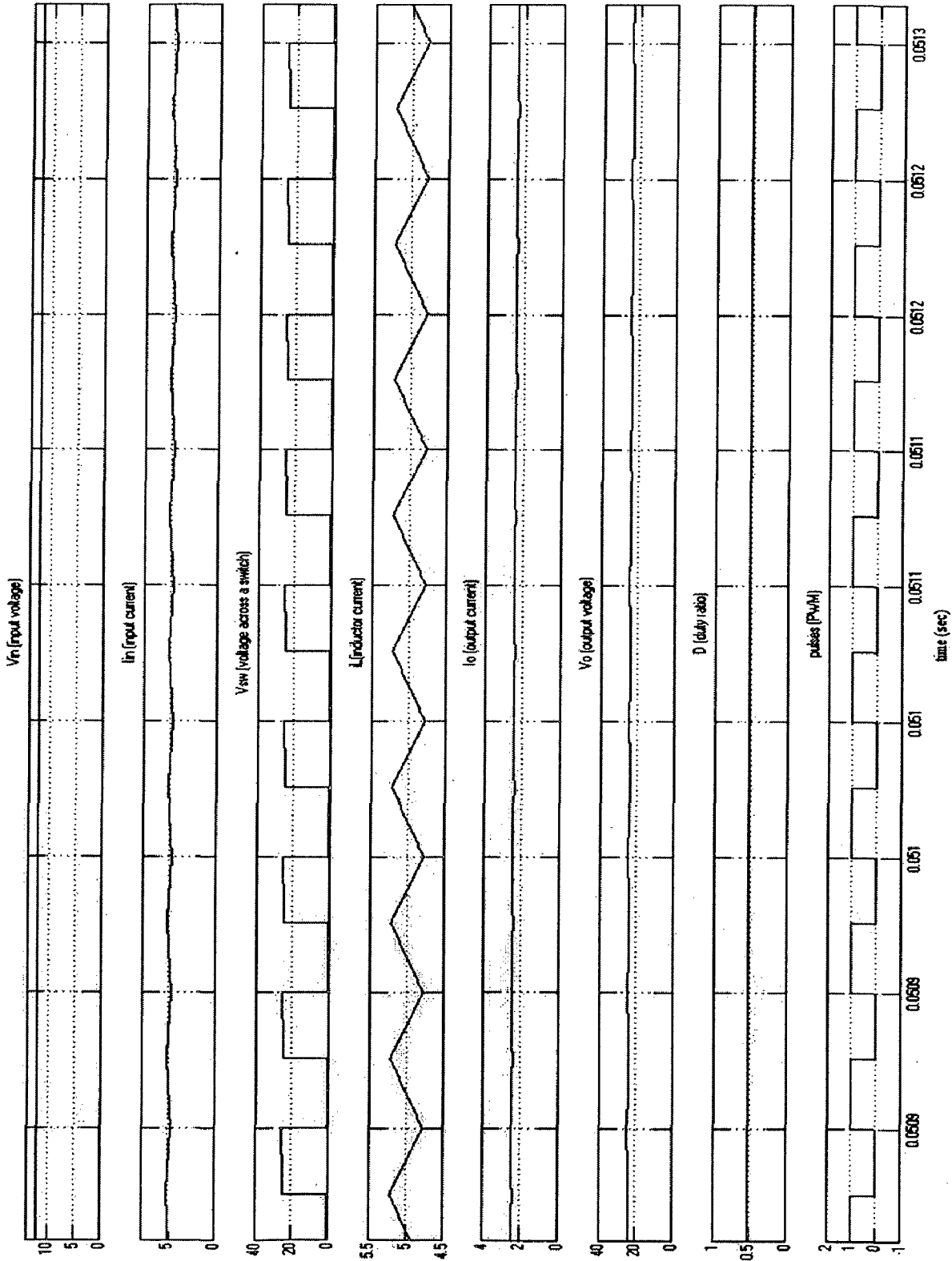
Fig 4.23: Simulation response of boost converter under steady state (enlarged view).

shown in fig.4.14 and 4.15. It shows various parameters like I_{in}, V_{in}, V_{out}, V_{sw} etc. The parameters used are shown in appendix table A.1. In fig 4.14 we can see how the controller is working. When supply voltage 12V is ON, the output voltage should be 24V. But the initial output voltage is 0V, so the controller takes the error voltage and increase the duty cycle such that the output voltage reaches 24V. Duty cycle remains constant as output voltage reaches 24V and as seen in fig.4.22 at 0.5. The fig 4.23 is the enlarged in fig 4.22 to see various wave forms of the boost converter under normal or steady state conditions. The pulses of 0.5 duty cycle are produced by the controller and given to the switch to get 24V output at 12V input. It also shows the continuous inductor current, voltage across the switch, input and output current wave forms. This gives complete details of the boost converter.

4.7.6 Closed loop Simulink model of Boost Converter with Type III controller

Modeling of the boost converter is done in MATLAB Simulink using the state space average method. Various blocks for the closed loop control are shown in fig 4.24. Every block is designed using MATLAB Simulink. The designed type III compensator is used as a controller.
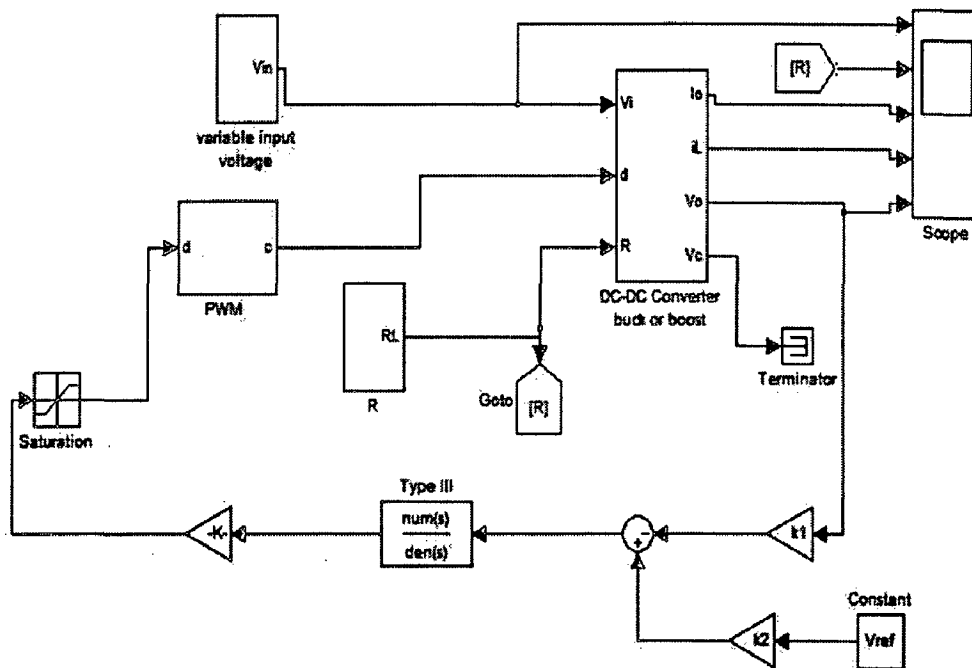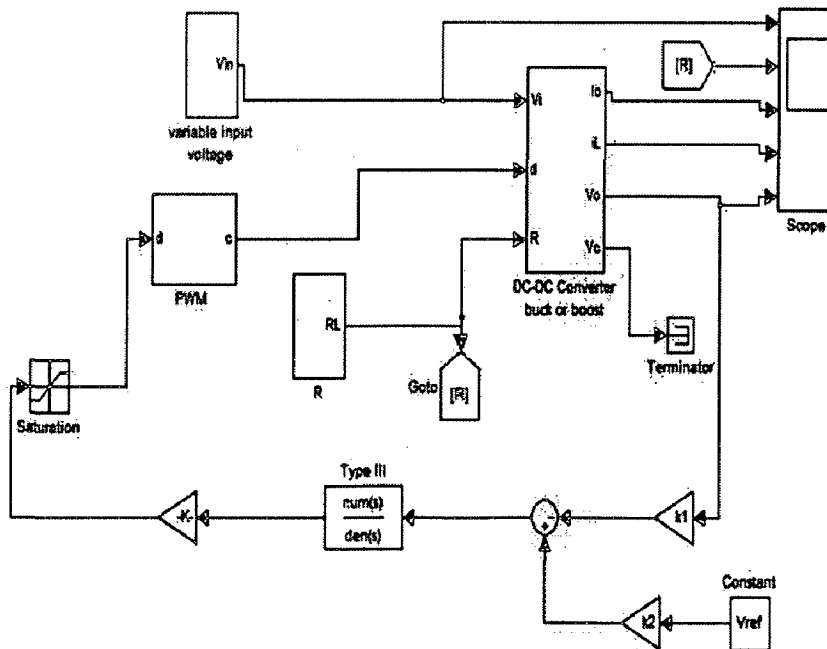

Fig 4.24: Closed loop Simulink model for boost converters
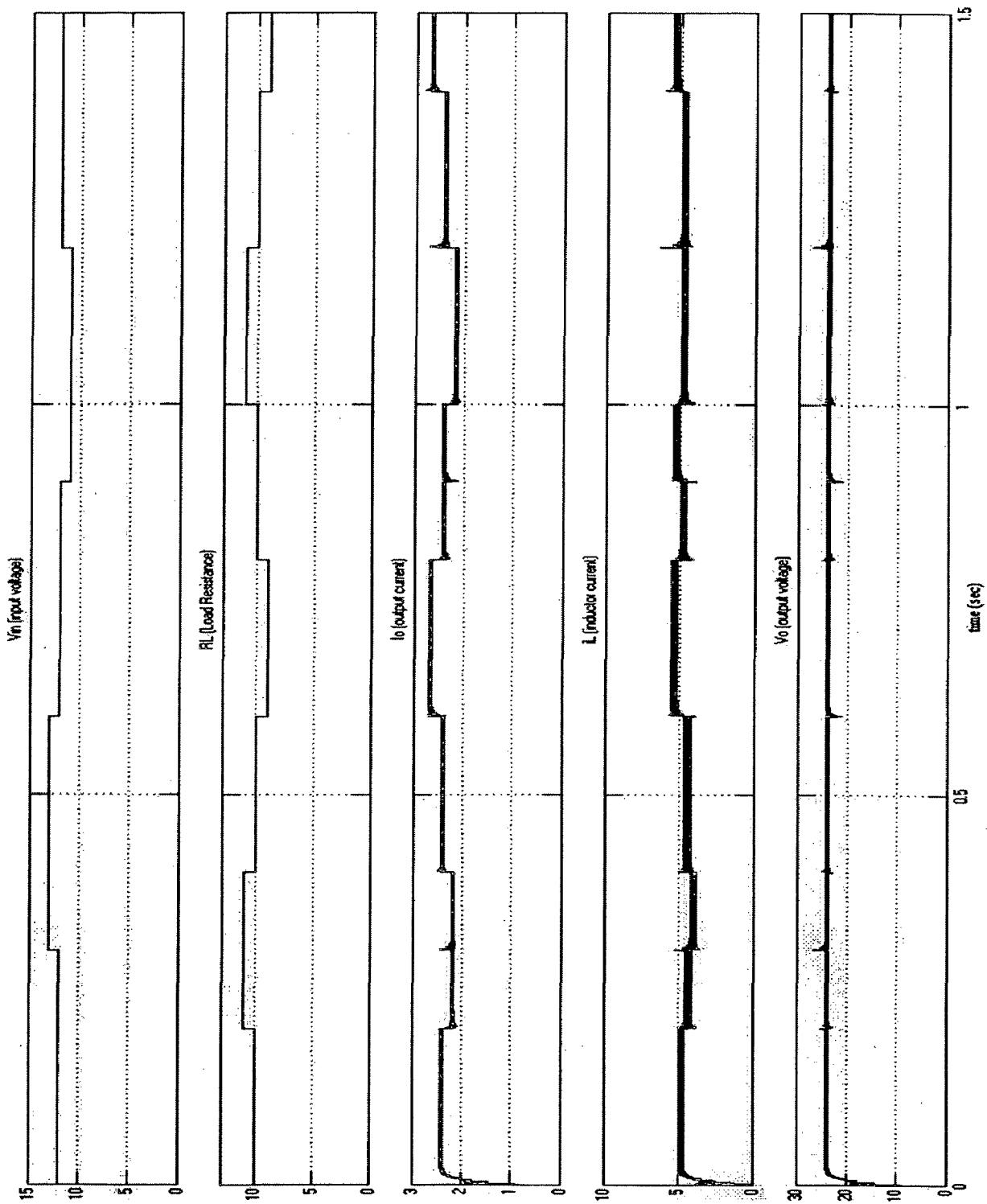
Fig.4.25: Closed loop response of Boost converter (V_{in} and R_L variation)

In place of the dc-dc converters boost converter model is placed which is shown in the fig.5.9. The type III compensator (A.2) which is designed previously is used in the TypeIII block and it acts as a controller. Variable input voltage and variable load is provided to the system to check the proper functioning of the controller. In fig 4.25 we can clearly see that the input voltage and load resistance is varied to see the effect on the output voltage and current. In boost converter the inductor current(i_L) is equal to the input current (I_{in}) which varies with both R_L and V_{in}, so when the load resistance varies, I_o and i_L varies accordingly i.e when R_L increases, I_o and i_L decreases, similarly when R_L decreases, I_o and i_L increases. Due the variation in the input voltage the I_o does not change except small disturbance during the transition of the input voltage because of small variation in V_o. Increase in the input voltage causes the i_L to decrease and decrease in V_{in} increase the i_L. With variation in R_L and V_{in} the output voltage remains constant, this is done by the type III controller. Whenever the input voltage varies, the controller will adjust the duty cycle such that V_o remains constant. If the V_o has changed due to change in load then the controller adjusts the duty cycle such that V_o remains constant. So fig.4.25 shows that the designed type III controller is providing satisfactory results for the boost converter.

4.7.7 Bi-directional buck and boost converter

Modeling of the converter can be done using the sim power system blocks in MATLAB. A complete bi-directional converter is modeled as shown in fig.4.26 using sim power system to give better understanding. Control logic is used such that it acts as buck converter for some time and as boost converter for some time by controlling e MOSFET T_1 or T_2 respectively to show the bi-directional property of the converter. It clearly shows in simulation results Fig.4.27 that the buck inductor current is positive for some time and is negative for remaining time. Similarly the boost inductor current is negative in the initial stage and become positive. This explains the bi-directional nature of the converter. Both the buck and boost inductor currents are same. When the buck inductor current is in negative it means it is in the boost mode, in the same way when the boost inductor current is negative then it means it is operating under buck mode. If the buck or boost currents are positive it means they are operating as respective converters.

The controls signals (CS) are provided to the bi-directional converter to get required mode of the operations. Based on different operating conditions the control signal should be chosen. Here the CS is given to shows the basic functioning of the bi-directional converter. The mode of operation

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is decided by the control signal (CS). When CS=1 buck operation and CS=0 boost operation takes place.

When CS is equal to 1 then the MOSFET (T₁) gets the pulses from the buck controller and voltage (V₁) acts as source voltage and R₂ acts as a load and V₂, R₁ are made off the circuit. Similarly When CS is equal to 0 then the MOSFET (T₂) gets the pulses from the boost controller and voltage (V₂) acts as source voltage and R₁ acts as a load and V₁, R₂ are made off the circuit.
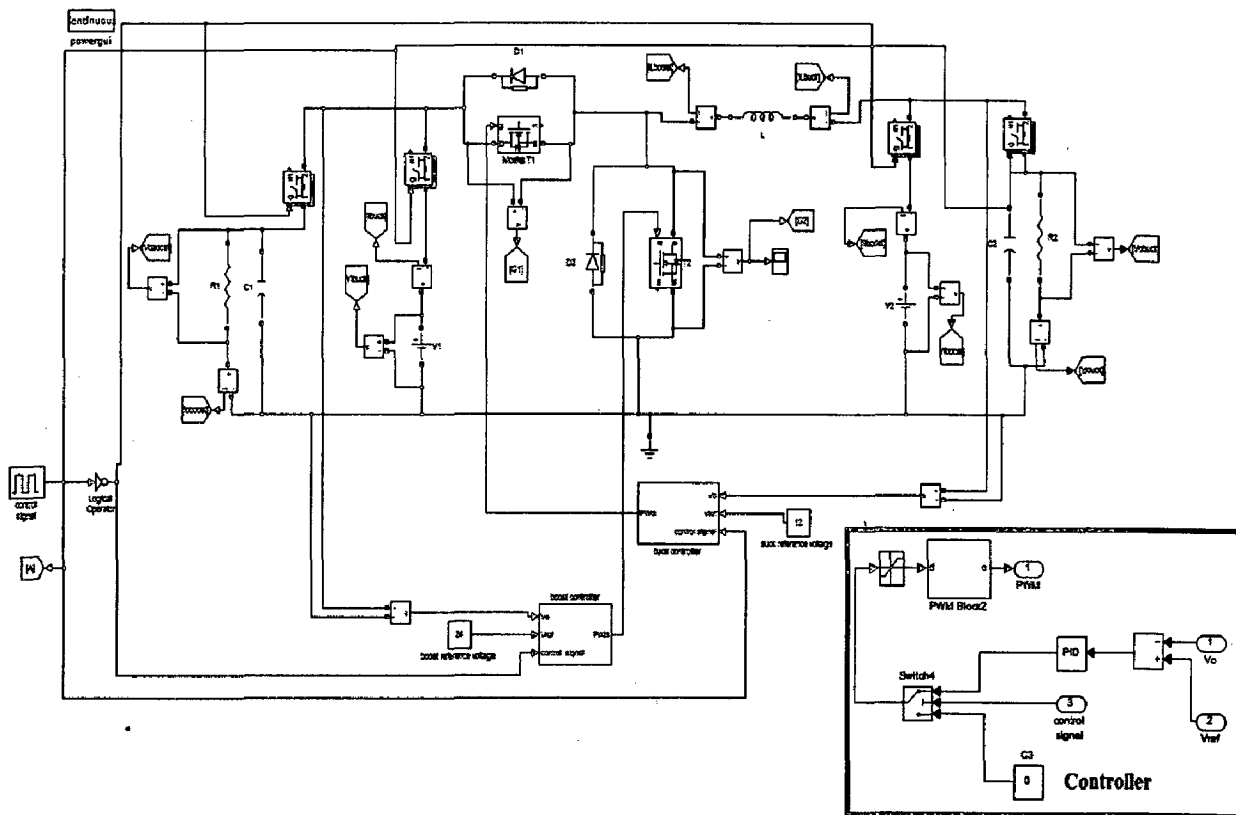
Fig 4.26: Simulink model of bi-directional buck and boost converter with control logic.

The results shown in the fig 4.27 clearly shows the buck and boost mode operation according to the control signals. V₁ and V₂ are seen as zeros in the results, they only represents that they are not acting as sources voltages. V₁ is zero means the load R₁ is active on that side and voltage source V₁ is out of the circuit. Similarly V₂ is zero means the load R₂ is active on that side and voltage source V₂ is out of the circuit.

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control signal(CS)

buck input voltage(Vin)

buck inductor current

buck output voltage (Vo)

boost input voltage(Vin)

boost inductor current

boost output voltage Vo

Time (sec)
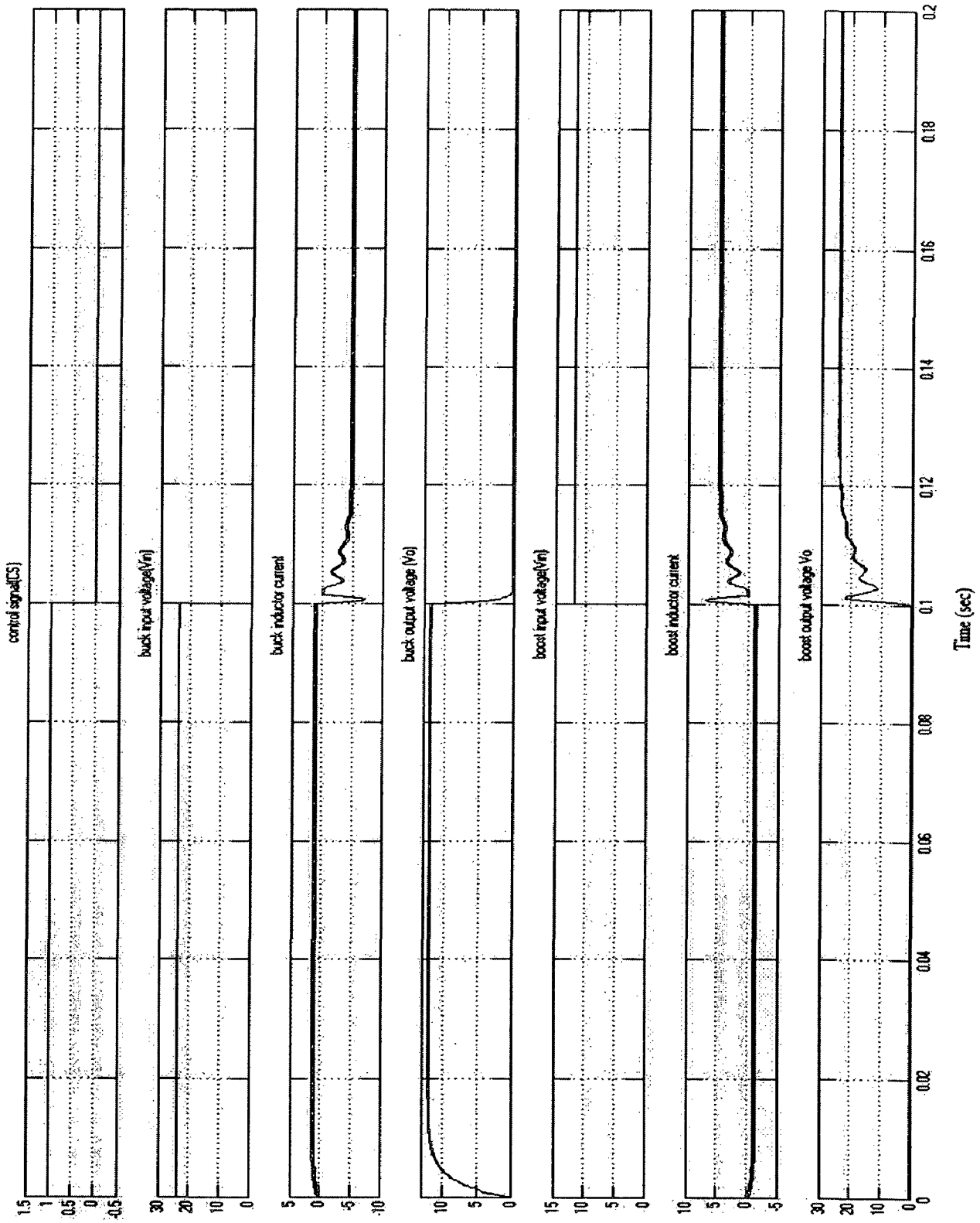
Fig 4.27: Operation of bi-directional buck and boost converter

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4.8 Hardware & results

The analog controller is done using TL494 Chip which has in built error amplifier. The frequency of the pulses is tuned using Rt and Ct values. They fix the frequency of the saw tooth wave form, which eventually gives the fixed frequency.

4.8.1 PWM Controller

The heart of a switching power supply is its switch control circuit (controller).One of the key objectives in designing a controller for the power converter is to obtain tight output voltage regulation under different line and load conditions [19]. Often, the control circuit is a negative-feedback control loop connected to the switch through a comparator and a Pulse Width Modulator (PWM). The switch control signal (PWM), controls the state (on or off) of the switch. This control circuit regulates the output voltage against changes in the load and the input voltage.

4.8.2 PWM Generation

Switching power supplies rely on negative feedback to maintain the output voltages at their specified value. To accomplish this, a differential amplifier is used to sense the difference between an ideal voltage (the reference voltage) and the actual output voltage to establish a small error signal ($v_{control}$).
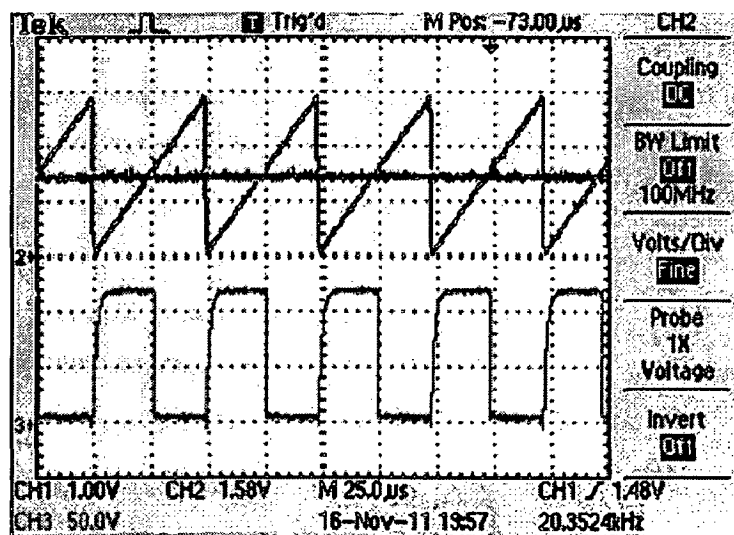
Figure 4.28: PWM Comparator Signals

$$D = \frac{t_{on}}{T_s} = \frac{V_{control}}{V_{st}} \qquad\qquad (4.59)$$

Duty cycle refers to the ratio of the period for which the power semiconductor is kept ON to the cycle period. A clearer understanding can be acquired by the Figure 4.29 .
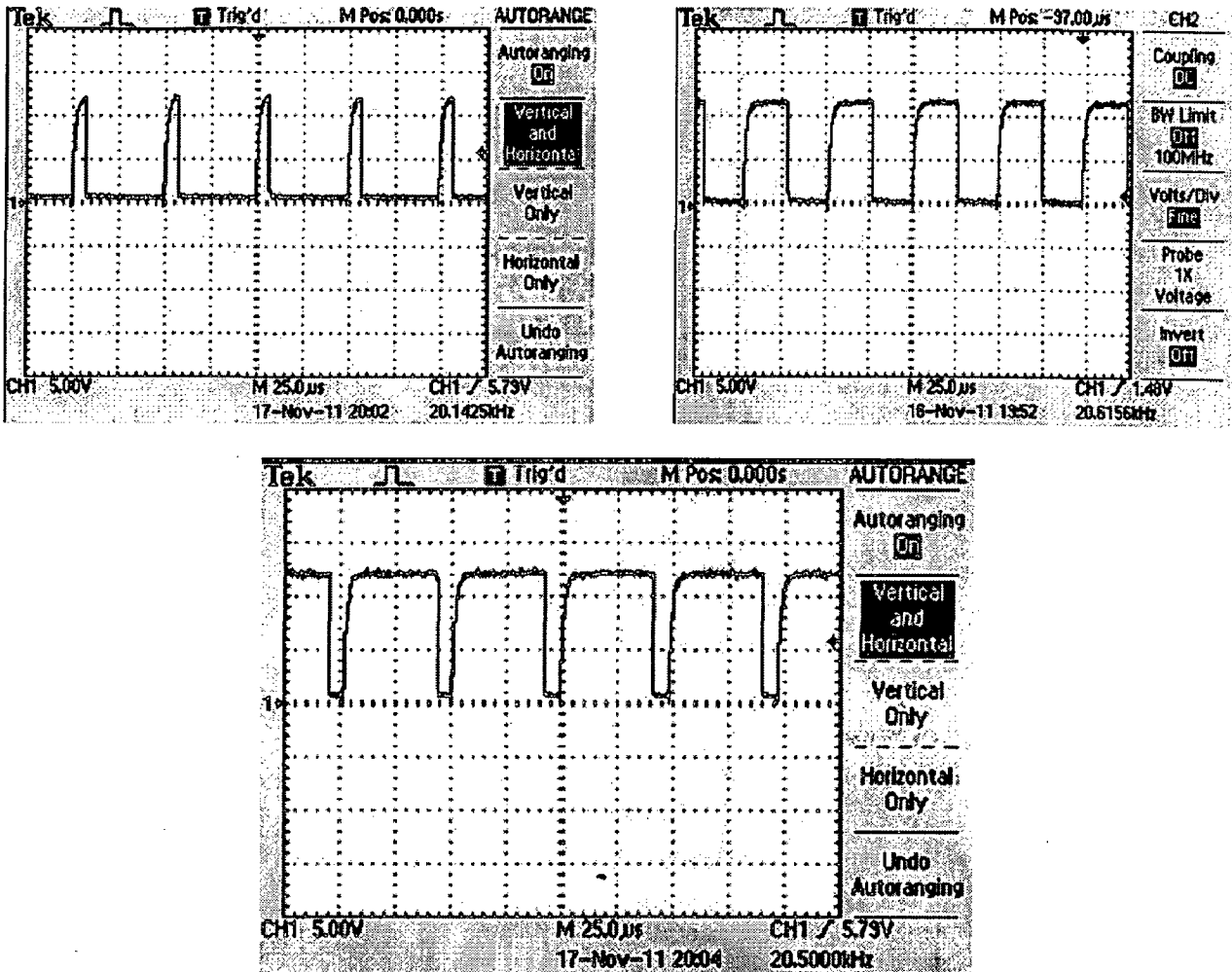
Fig 4.29: PWM (10%,50%,90%)

The Figure 4.29 shows PWM signals for 10% (a), 50% (b), and 90% (c) duty cycles. Usually control by PWM is the preferred method since constant frequency operation leads to optimization of LC filter and the ripple content in output voltage can be controlled within the set limits.

4.8.3 Buck Converter (using TL494)

The controller IC TL494 is used for the control circuit of the PWM switching regulator. The TL494 consists of 5V reference voltage circuit, two error amplifiers, flip flop, an output control circuit, a PWM comparator, a dead time comparator and an oscillator. This device can be operated in the switching frequency of 1 KHz to 300 KHz.
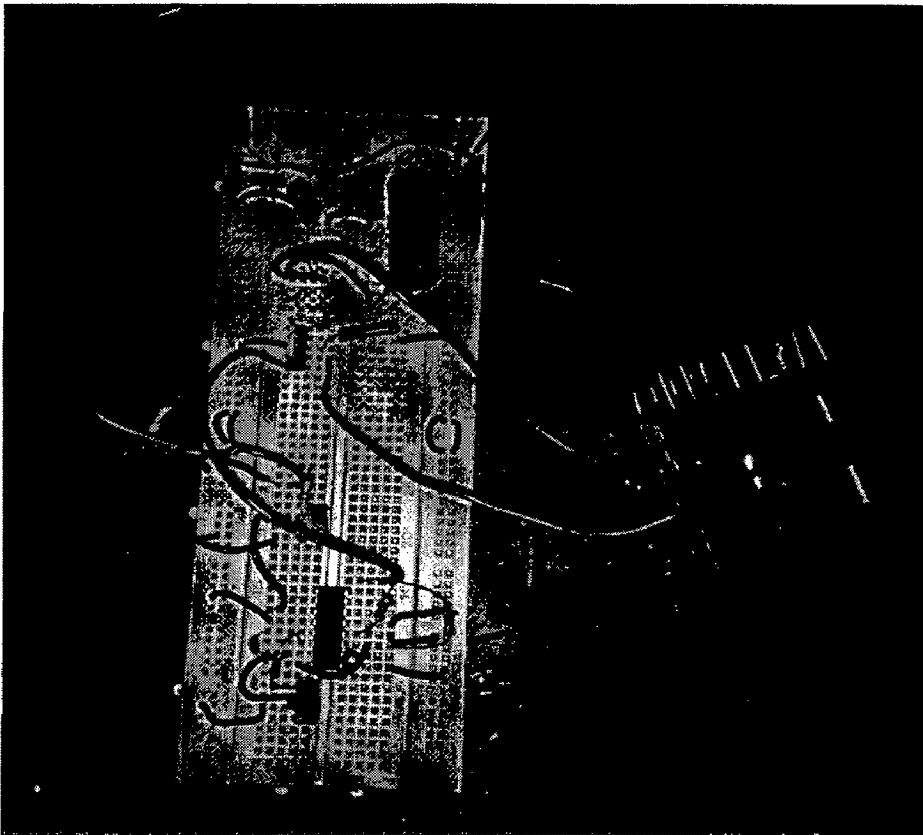
Fig 4.30: Buck converter (24V-12V).

The fig 4.30 shows the practical circuit of the buck converter using IC tl494. In this buck converter Tip 127 PNP transistor is used as a switching device. So the pulse will act as reverse i.e. the ON time becomes OFF time & OFF time becomes ON time.

The fig 4.31 shows the buck converter operation stepping down the voltage from 24V to 12V. the duty ratio of the PWM is 0.3 that is duty to reverse switching as explained in the above paragraph. The parameter used for this operation is mentioned in the appendix. The controller is designed for the buck converter and the same controller is used for the BDC, so the controller

testing is explained in the next section under buck mode operation since both are same. Output voltage measured from axis-1 at scale of 5volts/div in the results. The parameter used for this operation is mentioned in the appendix table A.3.
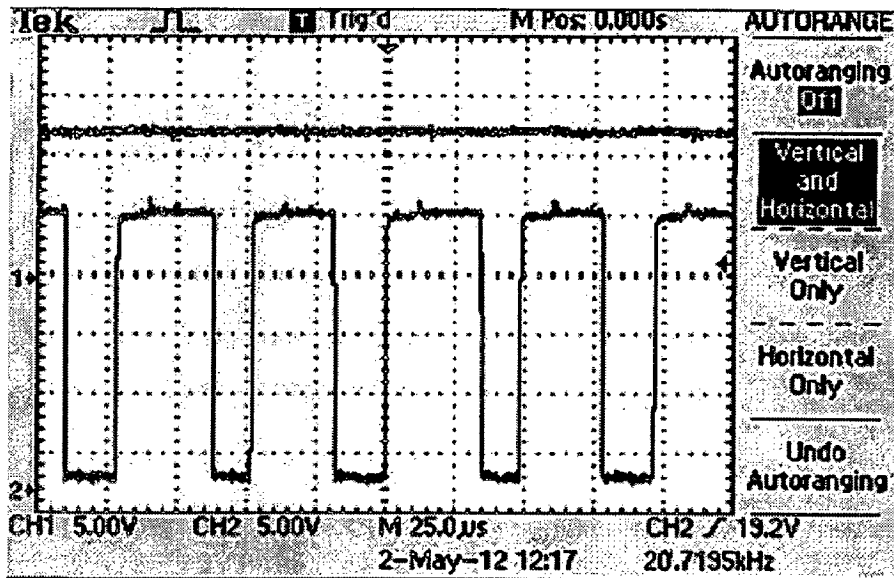
Fig 4.31: Buck converter gate pulses and output voltage (24V to 12V).

4.8.4 Boost Converter (using TL494)

The controller IC TL494 is used for the control circuit of the PWM switching regulator. The TL494 consists of 5V reference voltage circuit, two error amplifiers, flip flop, an output control circuit, a PWM comparator, a dead time comparator and an oscillator. This device can be operated in the switching frequency of 1 KHz to 300 KHz. Along with TL494, 7404 NOT gate is also used for the implementation of the boost converter.

The fig 4.32 shows the practical circuit of the boost converter using IC tl494. Unlike the buck converter N-channel MOSFET irf 560 is used as a switching device since boost converter has low side switching. The fig 4.33 shows the boost converter operation stepping up the DC voltage from 24V to 12V. the duty ratio of the PWM is around 0.3. The controller is designed for the boost converter and the same controller is used for the BDC, so the controller testing is explained

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in the next section under boost mode operation since both are same. Output voltage measured from axis-1 at scale of 5volts/div in the results. The parameter used for this operation is mentioned in the appendix table A.3.

Fig 4.32: Boost converter (12V-24V)
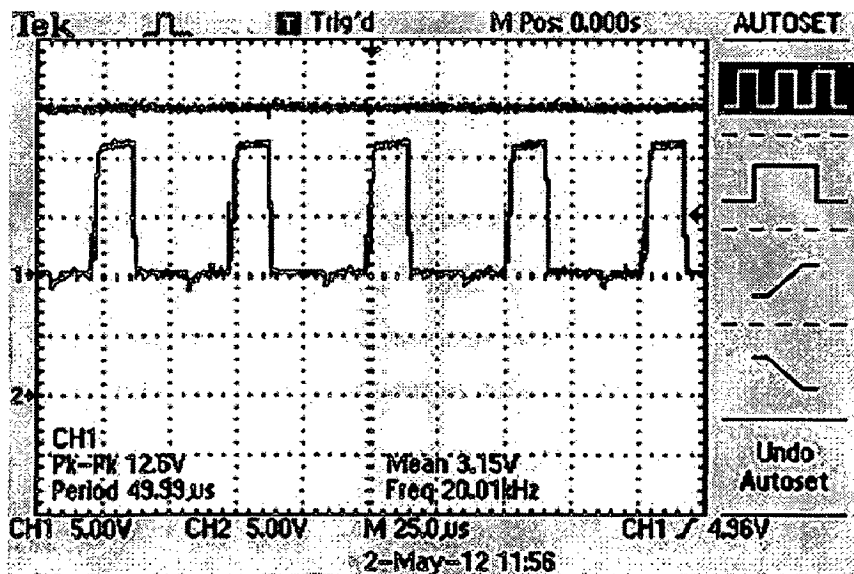
Fig 4.33: Boost converter gate pulses and output voltage (12V to 24V).

4.8.5 Bi-directional Buck and Boost Converter

The topology of the converter is explained in the previous chapter. Let's recall it from the fig 4.34 given below. The above circuits are properly merged to get the proper results. The practical circuit is shown in the next page.
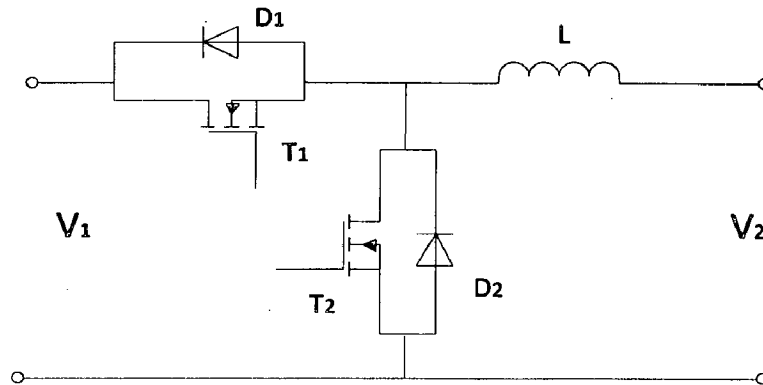
Fig. 4.34: Bi-directional buck and boost converter ($V_1 > V_2$).

By now we designed two properly working controllers, one for the buck operation and one for the boost operation. These exact controllers are used in the bi-directional converter. The bi-directional converter will act as independent buck converter in buck mode and it also act as an independent boost converter in the boost converter. Because of this, first independent controllers are designed for the buck converter and the boost converter. To test the bi-directional property of the converter, power supplies as well as loads are provided on both sides. Now the switches are provided to test the buck mode and boost mode operation as shown in fig 4.35. When power supply is switched ON at V_1, then load is switched ON or provided at V_2. Then controller will control the switch T_1 and operates as a buck converter i.e buck mode. During buck mode the load at V_1 and power supply at V_2 should be OFF. When power supply is switched ON at V_2, then load is switched ON or provided at V_1. Then controller will control the switch T_2 and operates as a boost converter i.e boost mode. During boost mode the load at V_2 and power supply at V_1 should be OFF. The buck controller and boost controller will be ON or gets power based on which side we applied the power supply. The bi-directional converter is shown in the fig 4.35 with power supplies and switches. The switches are provided to switch ON the power supply and also to switch ON the load. The system is arranged in such a way that we have to switch ON the

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power supply one side and load on the other side manually. Then the respective controller will be ON and operates in respective mode. During this time the other controller will be idle. This whole process should be done automatically which is very difficult with the analog controller. so the digital controller are preferred to analog controllers in complex controller circuit because it is easy to assess the operating conditions in the digital controller.
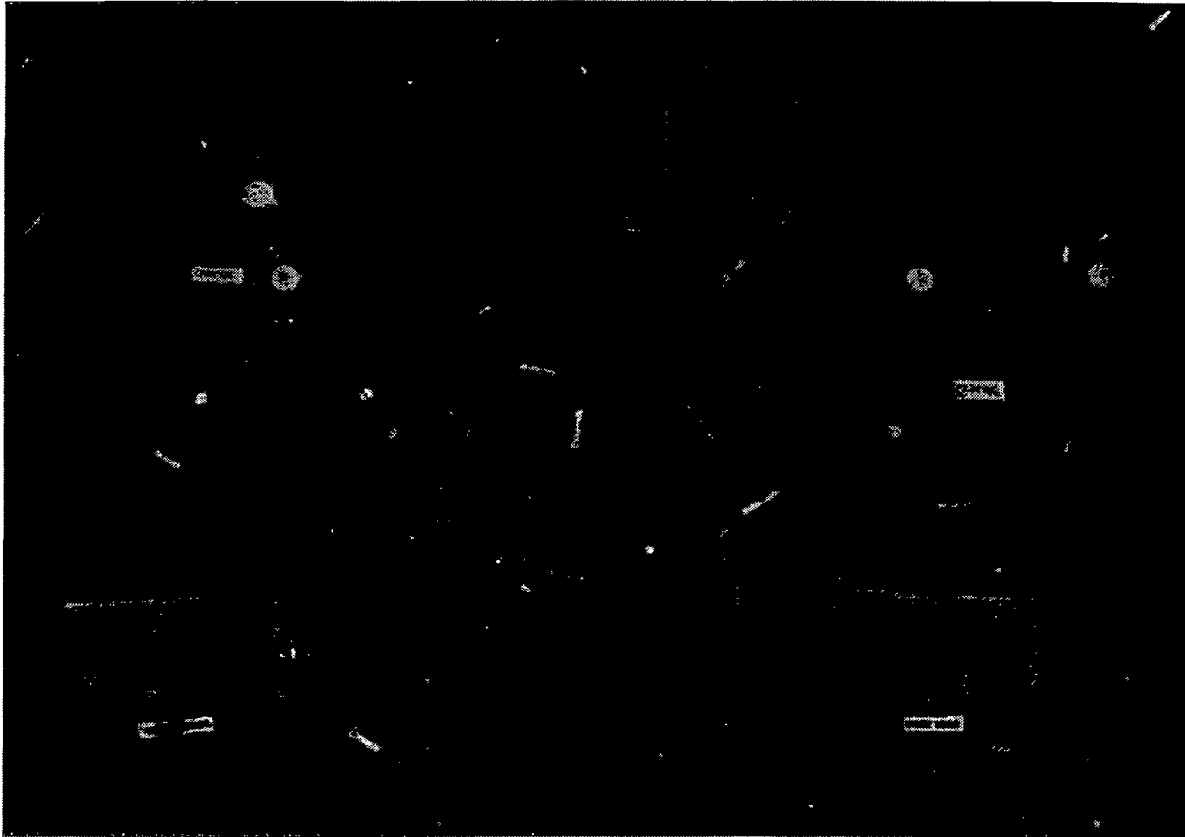
Fig.4.35: Bi-directional buck and boost converter (V₁>V₂)

(A) BDC in Buck Mode operation

A dc voltage source at V_1 side and a load is at V_2, to test the buck mode of operation as shown in fig 2.4. In this case, the energy flows from left to right. The MOSFET (T_1) channel is controlled by the controller and its antiparallel diode D_1 is permanently OFF, whereas the diode D_2 is used as a passive (naturally commutated) switch. The channel of the MOSFET (T_2) can be held permanently OFF. During this mode the controller designed for the buck converter will be active.

In the buck mode Tip 127 PNP transistor is used as a switching device. So the pulse will act as reverse i.e the ON time becomes OFF time & OFF time becomes ON time. So for voltage regulation, as V_{in} increases the duty cycle of PWM should also increase, so that the OFF time of the transistor increases, hence the V_{out} remains constant. Thus the voltage is regulated.

(i) Input Voltage (V_{in}) Variation

In order to check the function of the converter controller, the input voltage is varied to check whether output voltage is remaining constant or not. When the input voltage is varied, the output voltage should be maintained constant by the controller by changing the duty cycle of the PWM. The hardware results for variation of input voltage are presented below. The parameter used for the results from the fig.4.36 to fig.4.39 is given in the appendix table A.4.
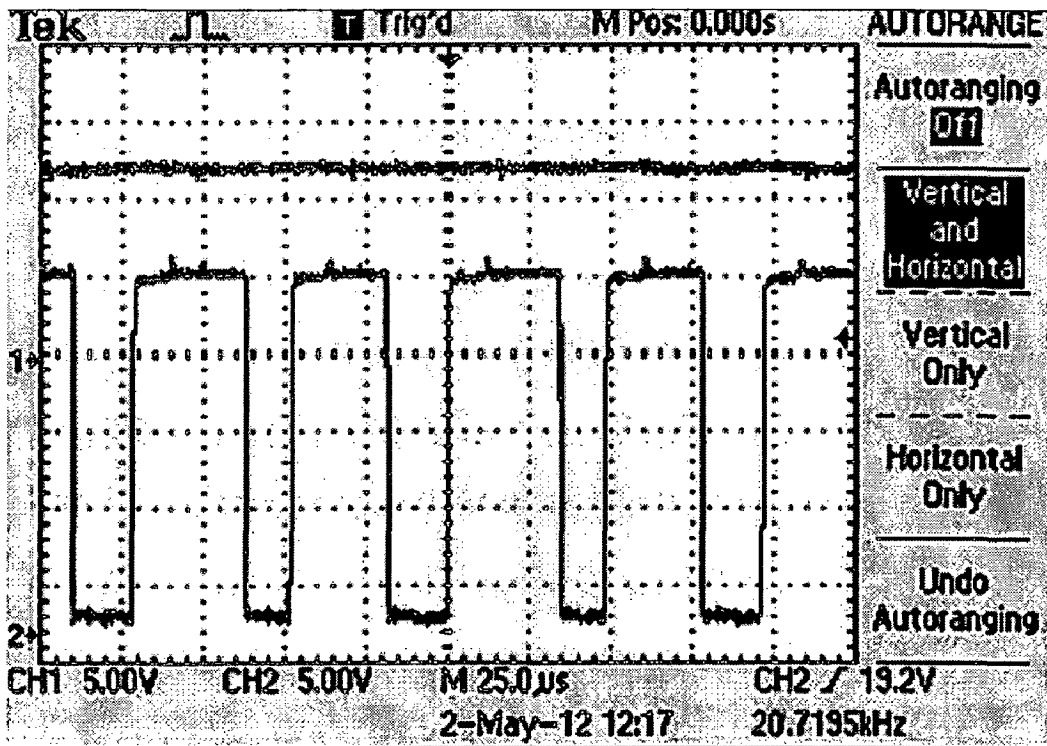
Fig 4.36: BDC in buck mode, gate pulses and output(24V to 12V).

Fig 4.37: BDC in buck mode, gate pulses and output voltage at V_{in}=19V

Fig 4.38: BDC in buck mode, gate pulses and output voltage at V_{in}=15V

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Fig 4.39: BDC in buck mode, gate pulses and output voltage at V_{in}=13V

From the fig 4.36 to fig 4.39 the input voltage is varied from 24V to 13V. In fig 4.36 one can see that the duty ratio (d) is around 0.7, in fig 4.37 d is 0.55, in fig 4.38 d is 0.3 and in fig 4.39 d is 0.2. Here it clearly shows that with decrease in the input voltage, d is decreasing but d has to increase (2.1) to make the output voltage constant. This is because we used PNP transistor as a switching device, so during PWM ON time switch will be OFF and during PWM OFF time switch will be ON. So effectively from fig 4.36 to fig 4.39 the d values will be 0.3, 0.45, 0.7, and 0.8. Now we can clearly see that with variation in the input voltage the controller is changing the duty cycle of the PWM such that the output remains constant. From the figures we can see the output voltage is reaming constant and measured from axis-1 at scale of 5volts/div in the results.

(ii) Load (R_L) Variation

In order to complete the buck mode controller testing, the load resistance is also varied to find out whether the controller is able to maintain the output voltage constant with load variation. When the load is increased (RL decreased), the output voltage tends to decrease, if load is decreased then the output voltage tend to increase. So the controller should be able to keep the output voltage constant with load variation by changing the duty cycle of the PWM. The circuit

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is tested with variable DC voltage source of rating 25V , 1A, which can give the maximum current of 0.8A. Based on the input source the load is varied and able to get the good results. The parameter used for the results from the fig.4.40 to fig.4.44 is given in the appendix table A.5.

Fig 4.40: BDC in buck mode, gate pulses and output voltage at R_L=14 ohms

Fig 4.41: BDC in buck mode, gate pulses and output voltage at R_L=65 ohms

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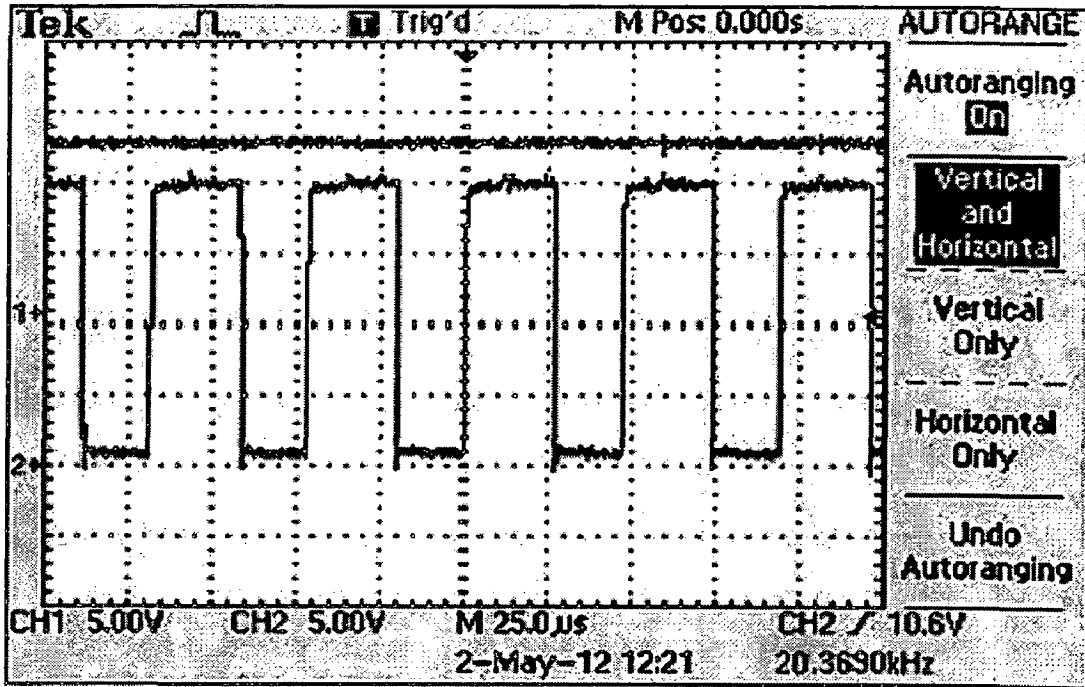
Fig 4.42: BDC in buck mode, gate pulses and output voltage at R_L=95 ohms

Fig 4.43: BDC in buck mode, gate pulses and output voltage at R_L=150 ohms

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Fig 4.44: BDC in buck mode, gate pulses and output voltage at R_L=250 ohms

From the fig 4.40 to fig 4.44 the load resistance is varied from 14ohms to 250ohms. As load resistance increases the output voltage will increase, so the controller has to decrease the duty ration in order to make the output voltage constant. In fig 4.40 one can see that the duty ratio (d) is around 0.1, in fig 4.41 d is 0.4, in fig 4.42 d is 0.5, in fig 4.43 d is 0.65, in fig 4.44 d is 0.9. Here it clearly shows that with increase in the load resistance, d is increasing but we discussed earlier that d have to decrease with increase in load resistance or decrease in load, to make the output constant. This is because we used PNP transistor as a switching device so during PWM ON time switch will be OFF and during PWM OFF time switch will be ON. So effectively from fig 4.40 to fig 4.44 the d values will be 0.9, 0.6, 0.5, 0.35, 0.1 which are decreasing. Now we can clearly see that with variation in load, the controller is changing the duty cycle of the PWM such that the output voltage remains constant. From the figures we can see the output voltage is reaming constant and measured from axis-1 at scale of 5volts/div in the results.

(B) BDC in Boost Mode operation

A dc voltage source is applied at V_2 side and a load is connected at V_1 side, to test boost mode of operation as shown in the fig 2.5. In this case, the energy flows from right to left. The

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MOSFET (T_2) channel is controlled by the controller designed for the boost converter previously and its antiparallel diode D_2 is permanently OFF, whereas the diode D_1 is used as a passive (naturally commutated) switch. The channel of the MOSFET (T_1) can be held permanently OFF. During this mode the boost mode controller will be active.

Unlike the buck converter, here MOSFET is used. So when the V_{in} is increased the D value should decrease (2.3) and if V_{in} is decreased the D value should increase in order to maintain the out voltage constant. As input voltage increases the OFF time should increase, if input voltage decreases the ON time should increase or OFF time should decrease.

(i) Input Voltage(V_{in}) Variation

In order to test the function of the boost mode controller, the input voltage is varied to check whether output voltage is remaining constant or not. When the input voltage is varied, the output voltage should be maintained constant by the controller by changing the duty cycle of the PWM. The hardware results for variation of input voltage are presented below. The parameter used for the results from the fig.4.45 to fig.4.49 is given in the appendix table A.4.
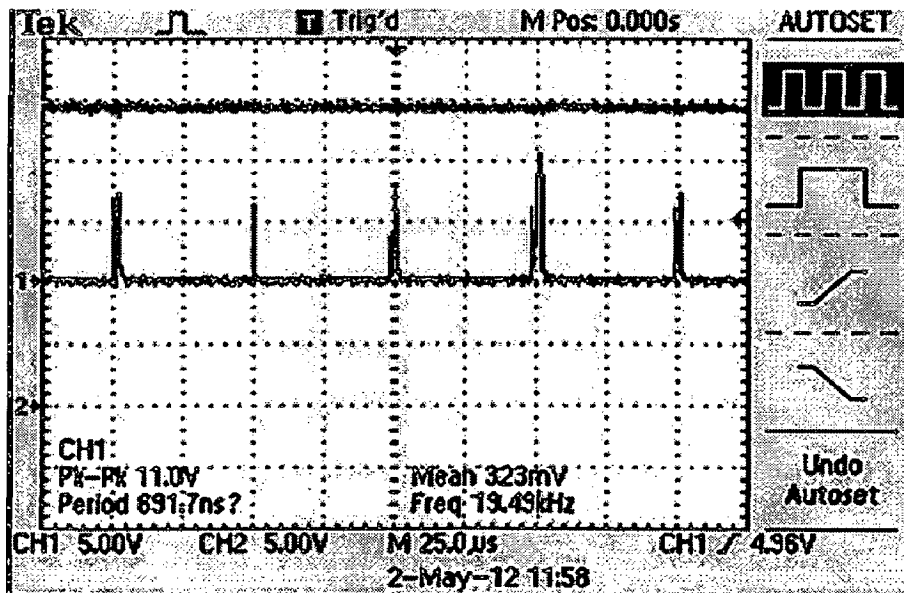
Fig 4.45: BDC in boost mode, gate pulses and output voltage at V_{in}=22V
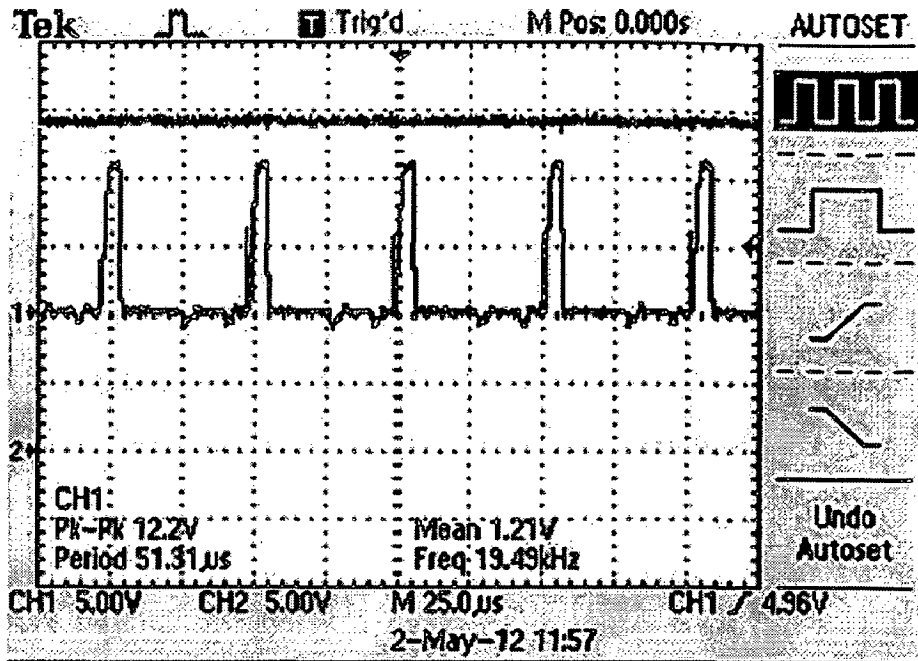
Fig 4.46: BDC in boost mode, gate pulses and output voltage at $V_{in}=17V$
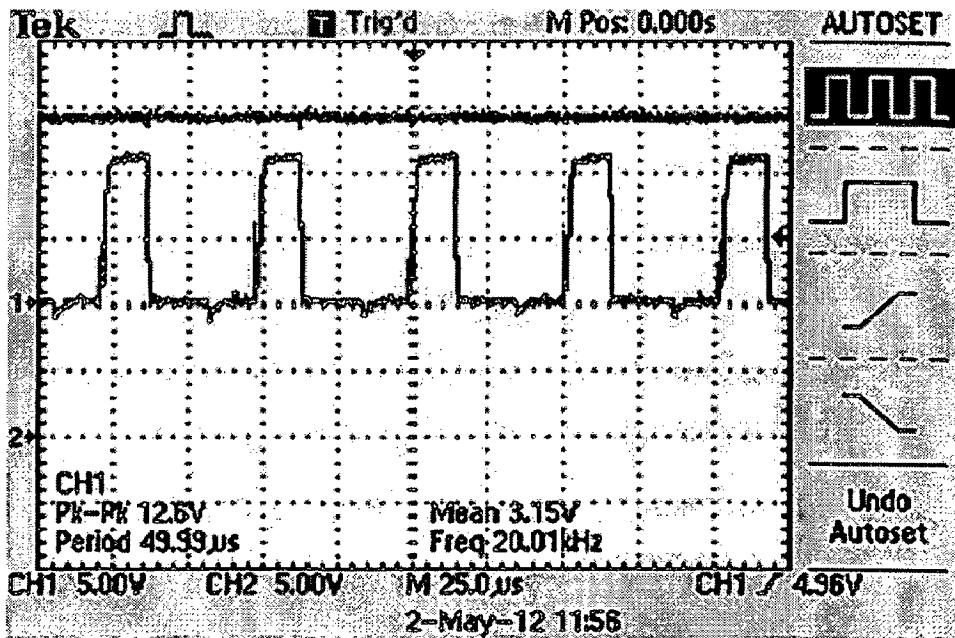
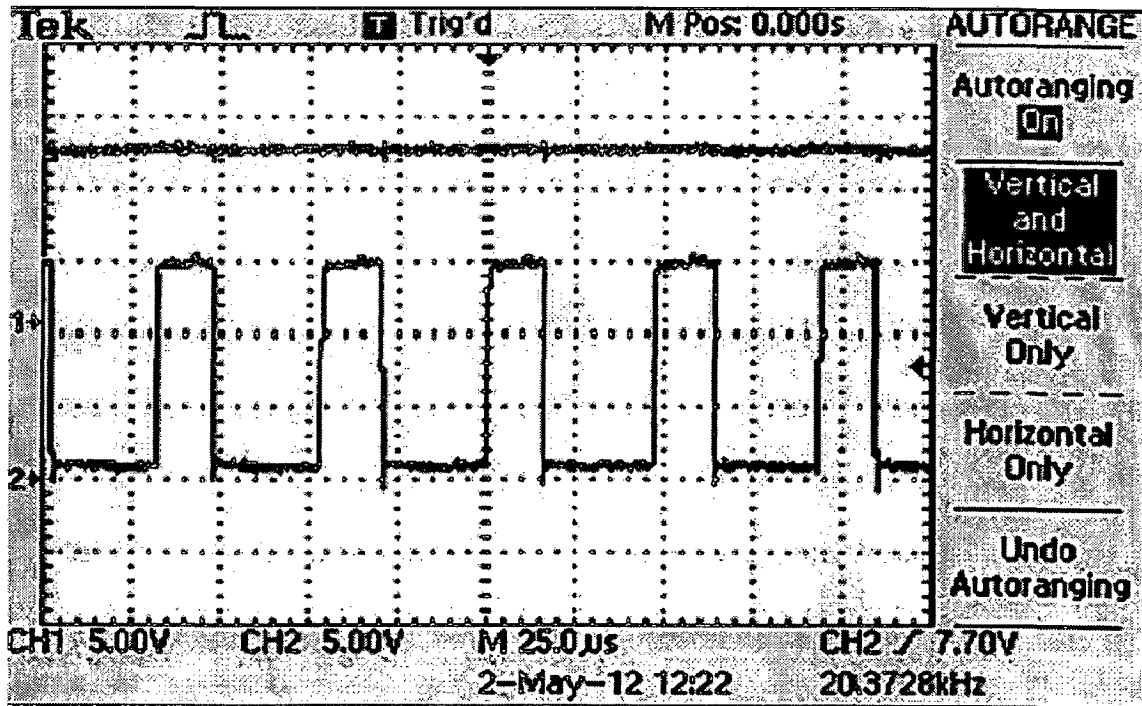Fig 4.47: BDC in boost mode, gate pulses and output (12V to 24V).

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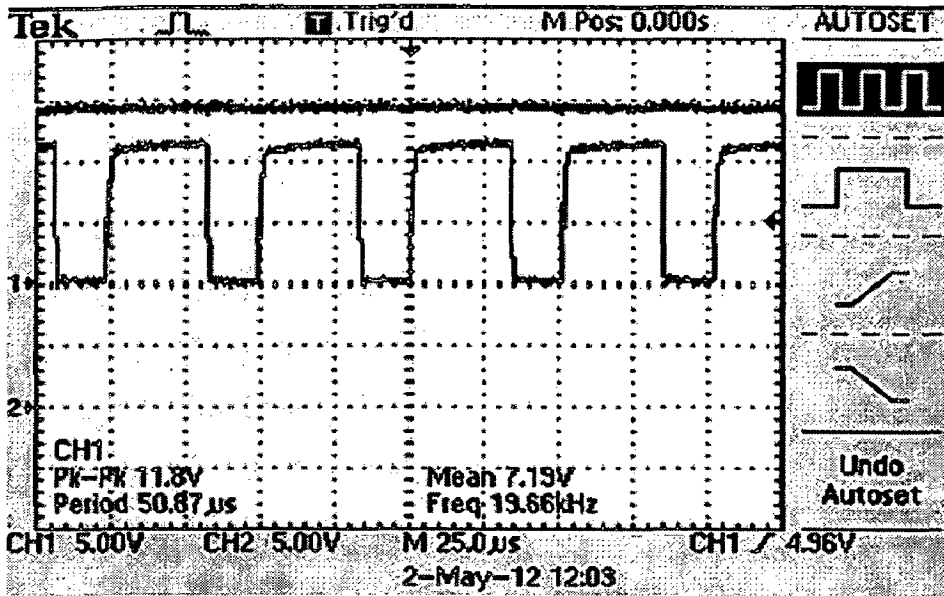
Fig 4.48: BDC in boost mode, gate pulses and output voltage at V_{in}=8.5V
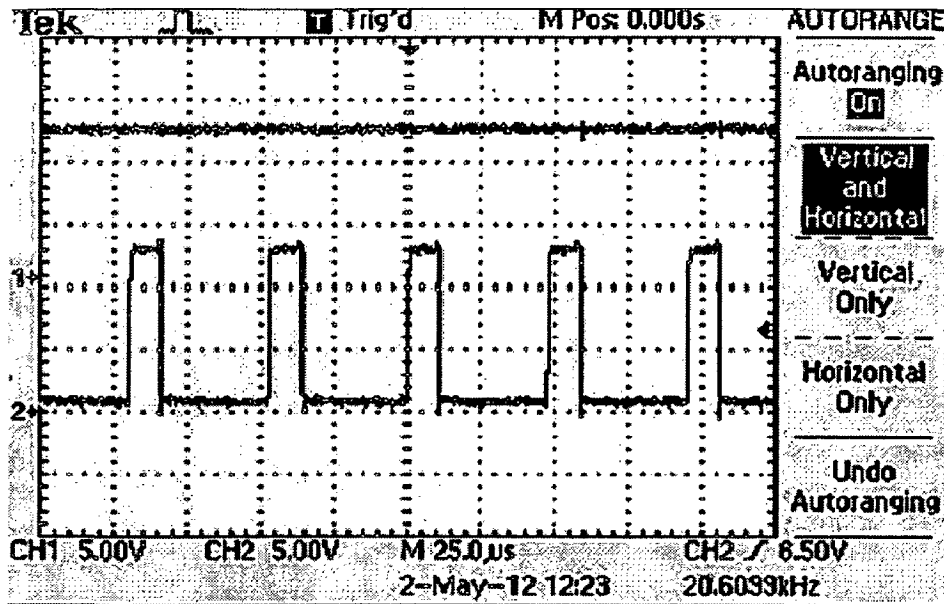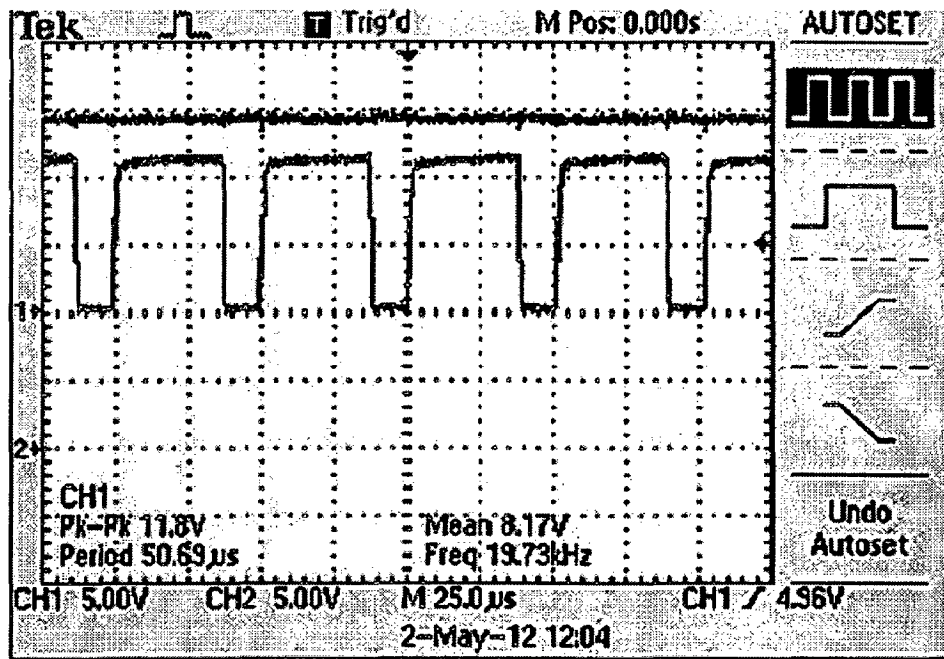

Fig 4.49: BDC in boost mode, gate pulses and output voltage at V_{in}=6.5V

From the fig 4.45 to fig 4.49 the input voltage is varied from 22V to 6.5V. In fig 4.45 one can see that the duty ratio (d) is around 0.05, in fig 4.46 d is 0.1, in fig 4.47 d is 0.3 and in fig 4.48 d is 0.7 and in fig 4.49 d is 0.8. Here it clearly shows that with decrease in the input voltage, d is

increased by the controller to make the output voltage constant. From fig 4.45 to fig 4.49 the ON time of the PWM is keep on increasing hence the duty cycle. Hence the controller is giving satisfactory results. From the figures 4.41 to 4.45, we can see the output voltage is reaming constant and measured from axis-2 up at scale of 5volts/div in the results.

(ii) Load (R_L) Variation

In order to complete the boost mode controller testing, the load resistance is also varied to find out whether the controller is able to maintain the output voltage constant with load variation. When the load is increased (RL decreased), the output voltage tends to decrease, if load is decreased then the output voltage tend to increase. So the controller should be able to keep the output voltage constant with load variation by changing the duty cycle of the PWM. The circuit is tested with variable DC voltage source of rating 25V, 1A, which can give the maximum current of 0.8A. Based on the input source the load is varied and able to get the good results. The parameter used for the results from the fig.4.50 to fig.4.54 is given in the appendix table A.5.
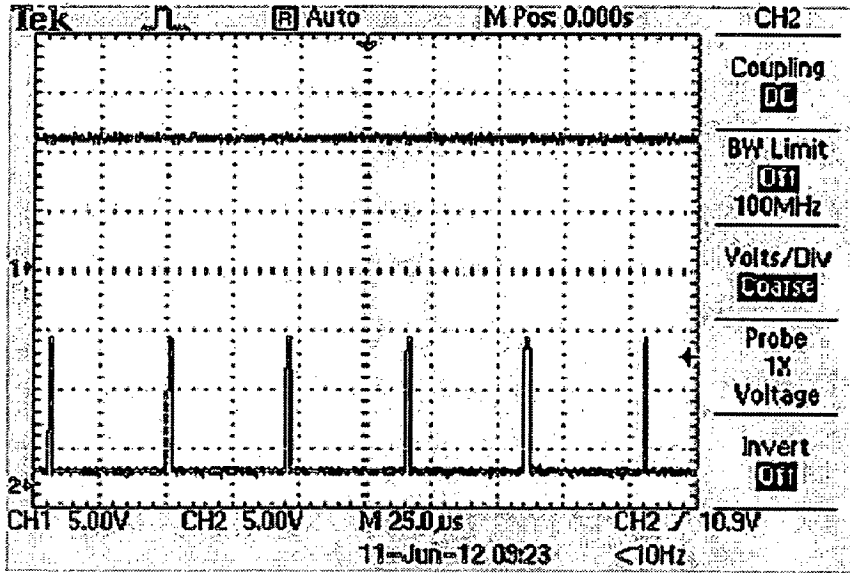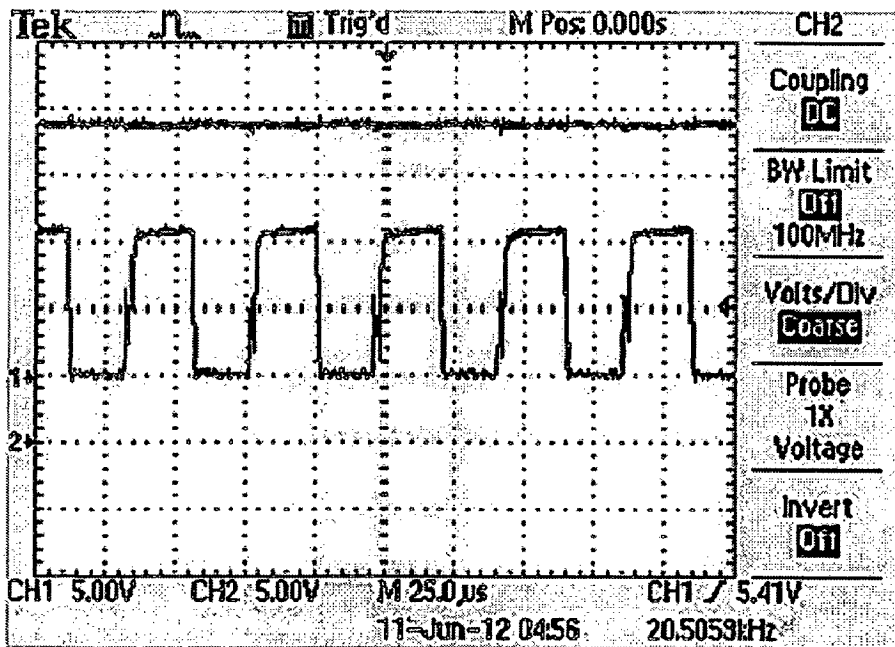

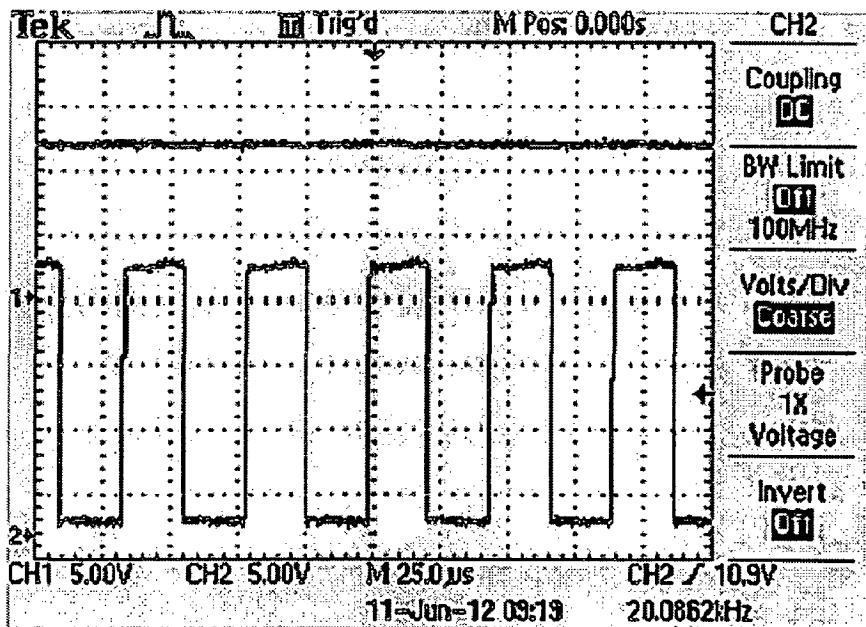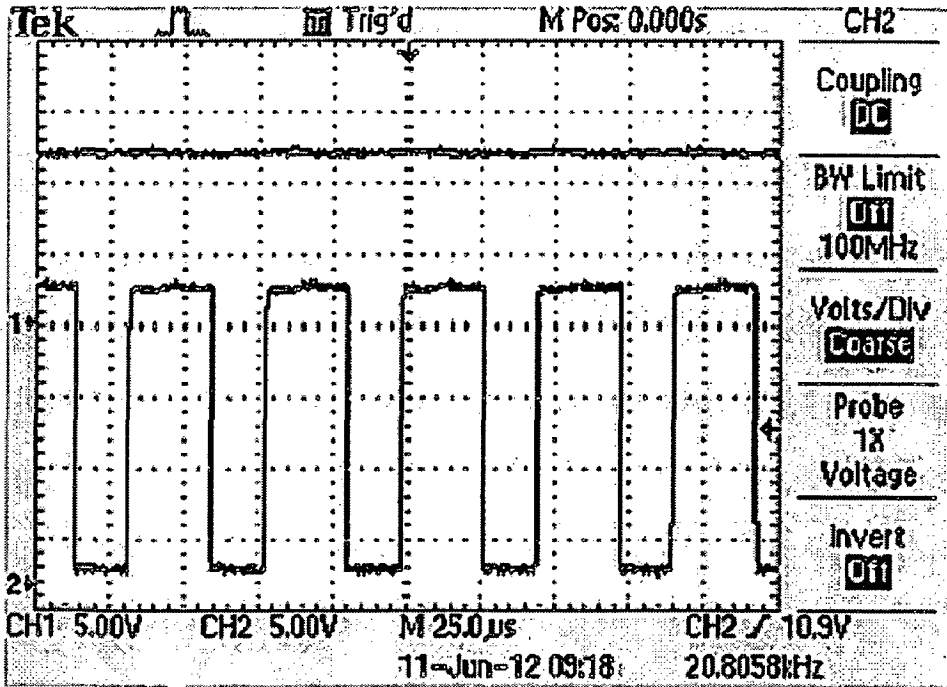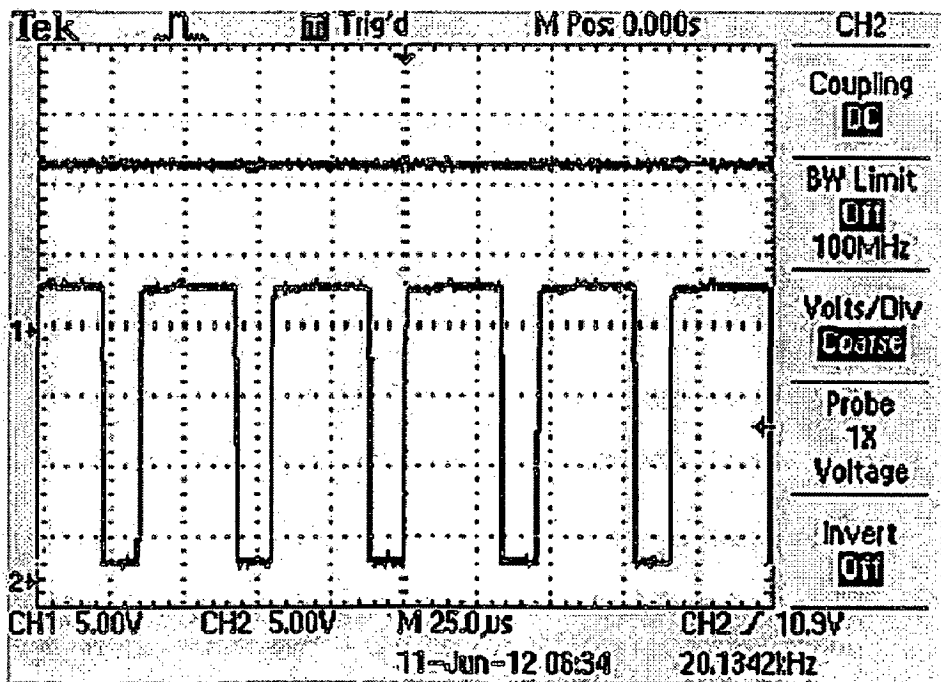Fig 4.50: BDC in boost mode, gate pulses and output voltage at R_L=110 ohms
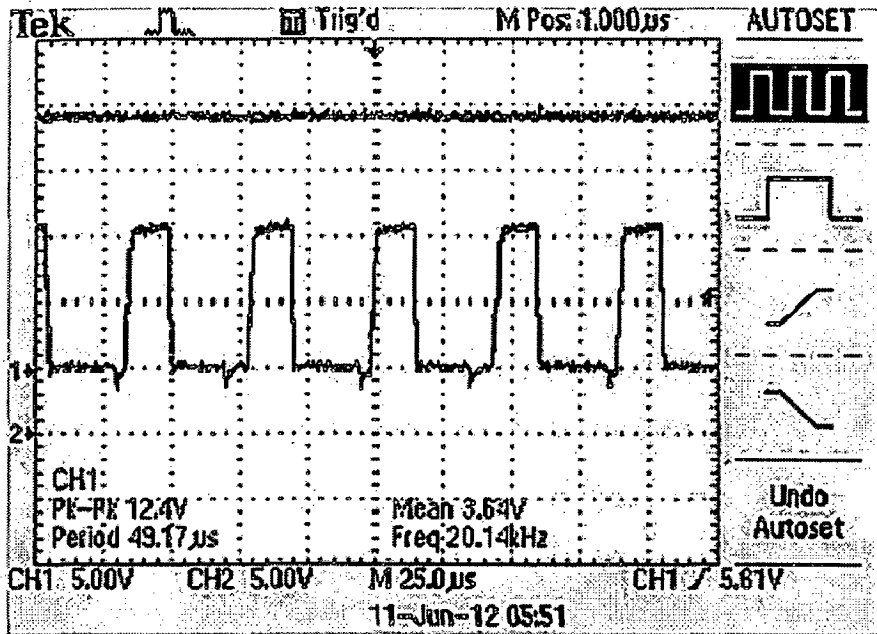
Fig 4.51: BDC in boost mode, gate pulses and output voltage at R_L=200 ohms
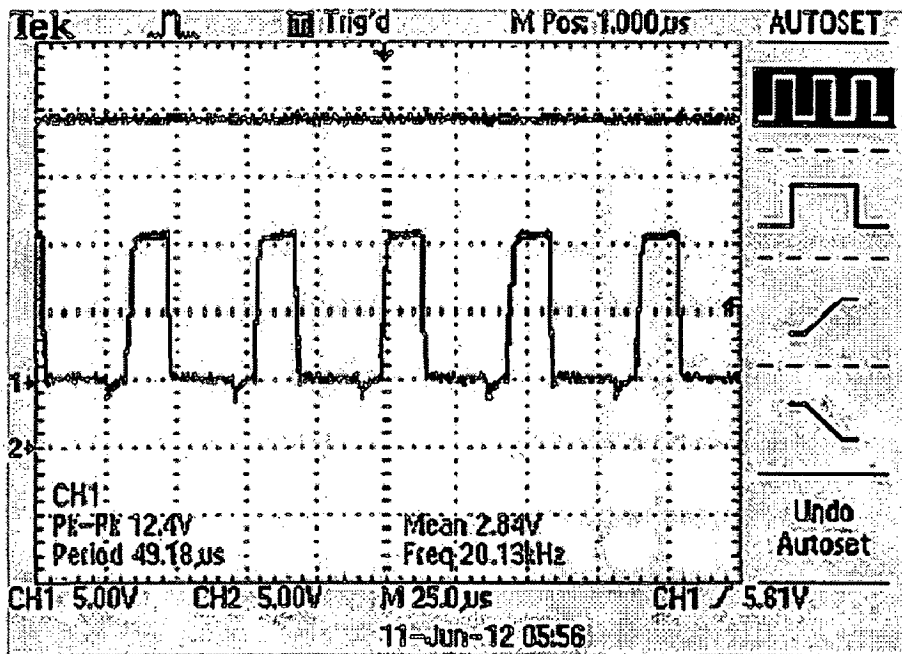
Fig 4.52: BDC in boost mode, gate pulses and output voltage at R_L=450 ohms

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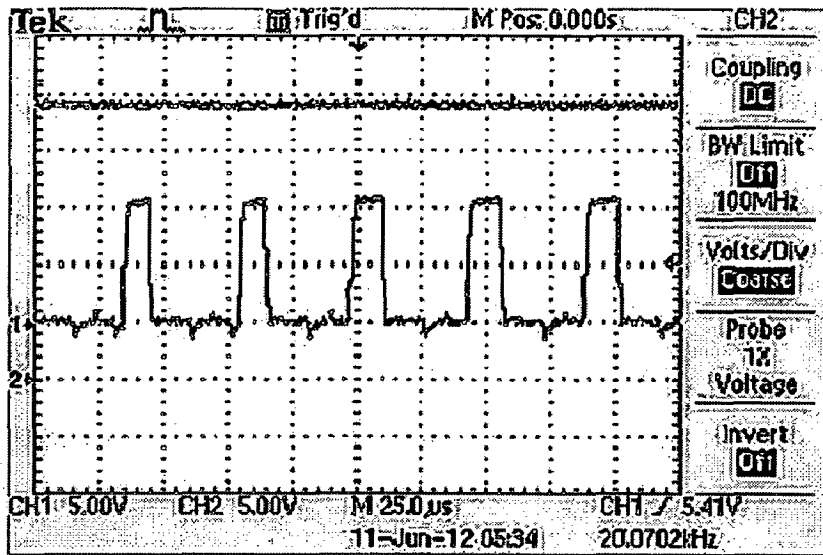
Fig 4.53: BDC in boost mode, gate pulses and output voltage at R_L=550 ohms
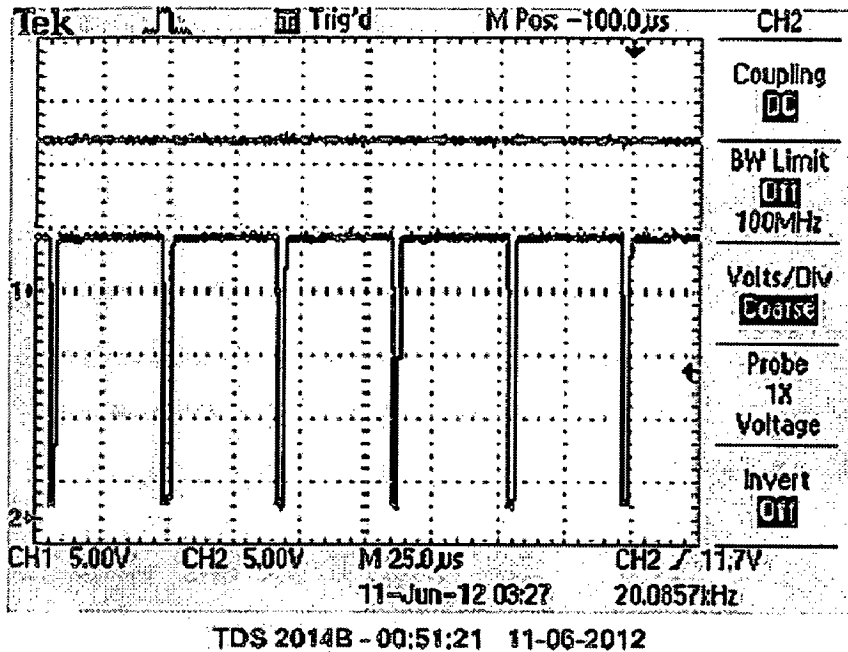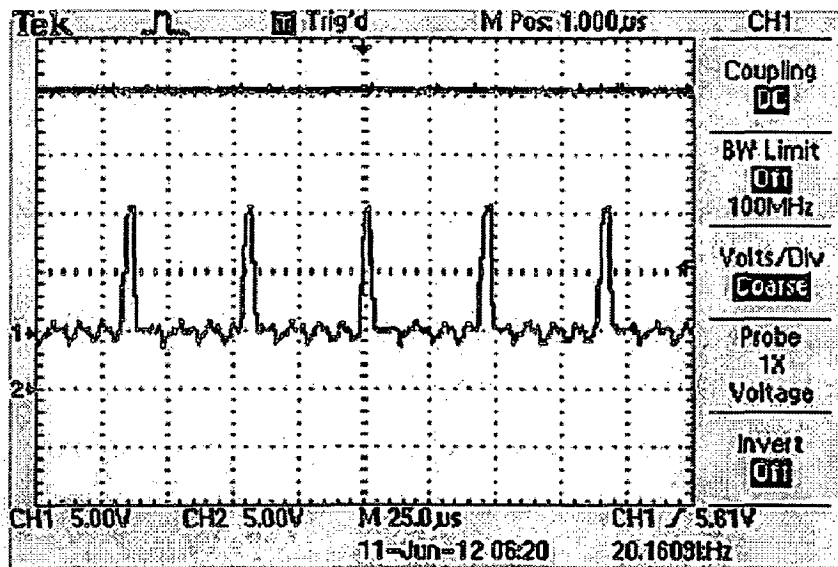

Fig 4.54: BDC in boost mode, gate pulses and output voltage at R_L=1.5k ohms

From the fig 4.50 to fig 4.54 the load resistance is varied from 110ohms to 1.5k ohms. As load resistance increases the output voltage will increase, so the controller has to decrease the duty ration in order to make the output voltage constant. In fig 4.50 one can see that the duty ratio (d) is around 0.4, in fig 4.51 d is 0.3, in fig 4.52 d is 0.25, in fig 4.53 d is 0.2, in fig 4.54 d is 0.1. Here it clearly shows that with increase in the load resistance, d is decreasing to make the output

constant. Now we can clearly see that with variation in load, the controller is changing the duty cycle of the PWM such that the output voltage remains constant. From the figures we can see the output voltage is reaming constant and measured from axis-2 up at scale of 5volts/div in the results.

4.9 Conclusion

Analog controller for buck mode and boost mode are properly designed and implemented using TL494. The results are also satisfactory. Even though the values of the resistance and capacitance of error amplifier are found using the method described in the previous section, in practical circuit, the stability is achieved by the tuning the values of the resistance. The parameters give the nearest values only. In buck converter we cannot use the MOSFET directly because the source of the MOSFET is not ground (high side switching) but has some potential. So the driver circuit should be properly designed to use the MOSFET or can use PNP transistor or P-channel MOSFET directly. Just by joining the both circuits as explained we can get the bidirectional buck and boost converter. The controller part remains same. This converter either acts as buck or boost, one at a time depending upon the side at which the input voltage is applied. The operating conditions of the BDC depend on the input power supply voltage rating and current rating. The variable DC power supply of 25V, 1A is used. BDC in boost mode is able to operate approx. between (9V-22V, 240mA). BDC in buck mode is able to operate approx. between (13V-24V, 1A). The limitations are solely based on the availability of the power supply ratings can work smoothly up to 50W in boost mode and 15W in buck mode.

CHAPTER-V

Design and Implementation of Bi-directional Buck and Boost Converter Using Digital Controller

[Presented in this chapter is the digital control design, modeling for DC-DC converters using linear and nonlinear control methods. The design of the controllers is done using direct, indirect approach and fuzzy technique also used. Modeling and implementation of buck, boost and bi-directional buck and boost converter are also discussed.]

5.1 Introduction

Digital control of switching power supplies is becoming more and more common in industry today because of the availability of low cost, high performance DSP controller with enhanced and integrated power electronic peripherals such as analog-to-digital (A/D) converters and pulse width modulator (PWM). DSP based digital control allows for the implementation of more functional control schemes, standard control hardware design for multiple platforms and flexibility of quick design modifications to meet specific customer needs. Digital controllers are less susceptible to aging and environmental variations and have better noise immunity. Modern 32-bit DSP controllers with processor speed up to 150MHz and enhanced peripherals such as, 12-bit A/D converter with conversion speed up to 80nSec, 32x32-bit multiplier, 32-bit timers and real-time code debugging capability gives the power supply designers all the benefits of digital control and allows implementation of high bandwidth, high frequency power supplies without sacrificing performance. The extra computing power of such processors also allows implementation of sophisticated nonlinear control algorithms, integrate multiple converter control into the same processor and optimize the total system cost. However, the power supply engineers, mostly familiar with analog control design, are faced with new challenges as they start to adopt these new digital control techniques in their designs.

5.1.1 Design by Emulation

This is also known as Digital Redesign Approach. In this method, an analog controller is first designed in the continuous domain as if one were building continuous time control system, by

ignoring the effects of sampling and hold associated with the AD converter and the digital PWM circuits. The analog controller is then converted to a discrete-time compensator by some approximate techniques. Figure 3 represents a simplified block diagram of a system. It shows all the different components of this closed loop control system in s-domain.
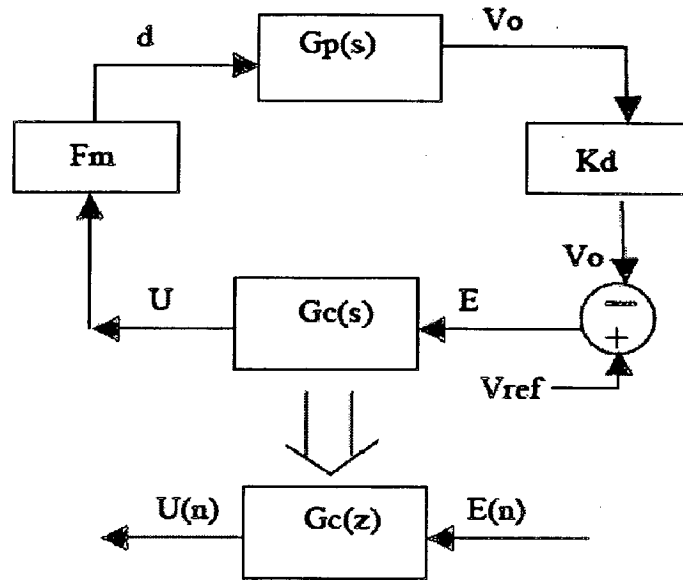
Figure 5.1: DC-DC Converter Control Loop Block Diagram in s-domain

5.1.2 Direct Digital Design

In this type of design sampling process by the on-chip ADC is represented by an ideal sampler with time period T_s. ADC can be represented this way as compared to the model given in [20], since the ADC gain is taken into account in the block labeled K_d and ADC conversion time is included in the computation delay block labeled H_c. The on-chip PWM module acts as a hold device. Representing this as a zero-order-hold (ZOH), the ADC and the PWM module together form a sampling and hold device. The s-domain transfer function of such a device can be expressed as $[1- \exp(-s*Ts)]/s$. The computation delay block H_c, models the time delay between the ADC sampling instant and the subsequent duty ratio update. If this time delay is denoted by T_d then the transfer function for H_c is, $H_c = \exp(-s*T_d)$. Now, the continuous time power stage model is first discretized with ZOH and the sampler
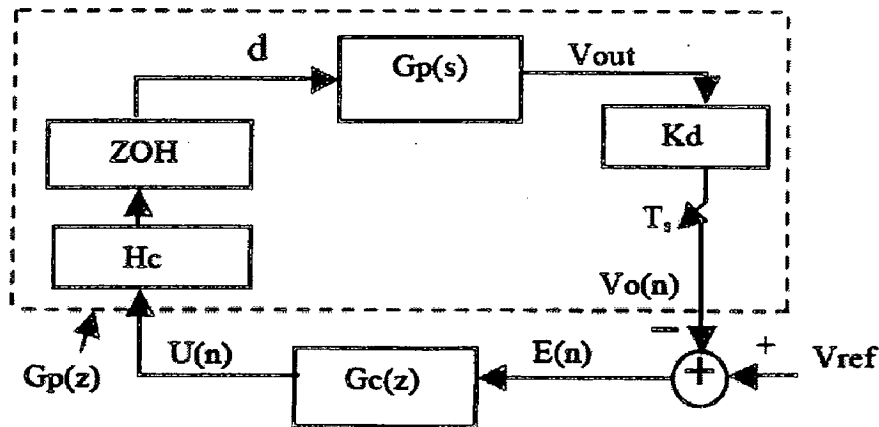
Figure 5.2: DC-DC Converter Digital Control Loop Block Diagram

Once this is available, the discrete-time compensator. i.e., a digital controller Gc(z) is designed directly in the z-domain using methods similar to the continuous-time frequency response methods. This has the advantage that the poles and zeros of the digital controllers are located directly, resulting in a better load transient response, as well as better phase margin and bandwidth for the closed loop operation of the power converter.

5.2 Design And MATLAB Simulation

5.2.1 Buck Converter

Modeling of the buck converter is done using state space average method equations (4.22),(4.23) obtained in previous chapters. Using those equations Simulink model of buck converter shown in fig 5.3 is done in the MATLAB. After mathematical manipulation of the state-space equations, the final dynamic and output equations are made, to develop Simulink model of power stage. Due importance is given in the model to the effect of non-linear parameters in voltage converters, such as equivalent series resistance ESL of the inductor, ESR of capacitor and RDS(on) of MOSFET switches.
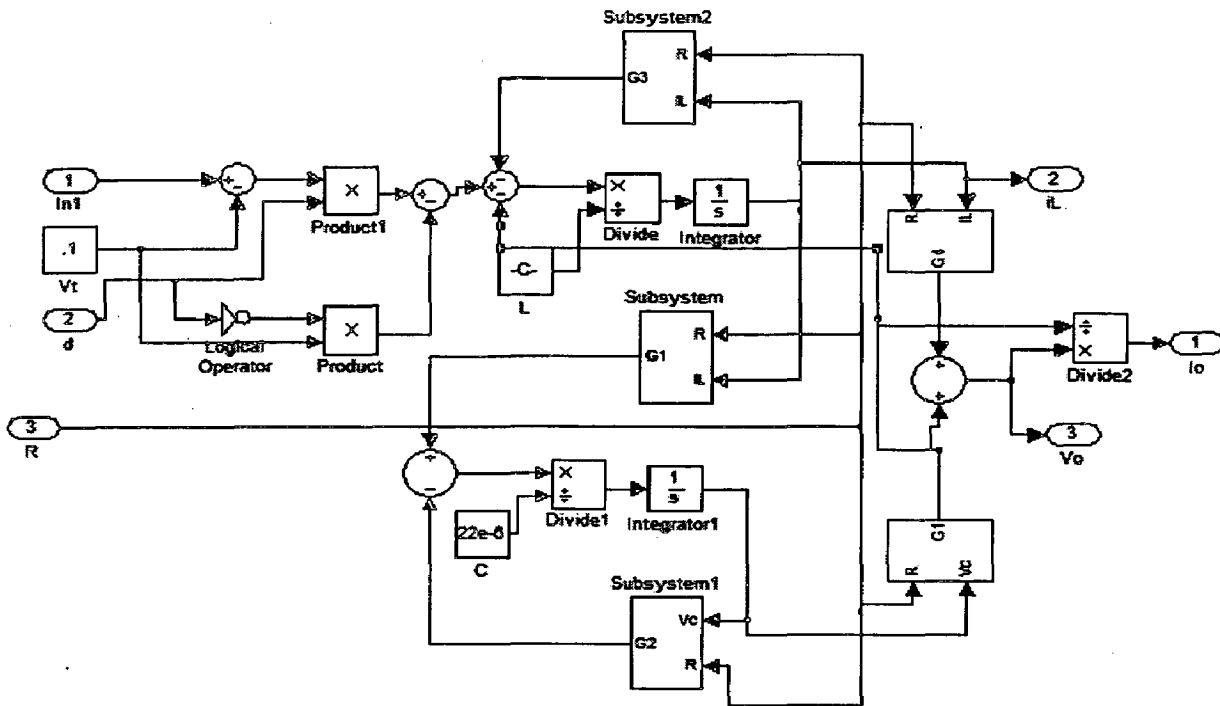
Fig 5.3: Simulink Model of Buck converter (Power stage using state-space)

5.2.2 Design of PID Controller

The performance of a closed loop converter is highly influenced by controller parameters. In order to avoid approximation errors associated with indirect digital design methods, we apply a direct digital design procedure for controller design.

5.2.3 Discrete PID Controller

A typical closed loop system using a PID controller is shown in Fig.5.The PID block provides the compensation in the feedback control of the switching converters. The ideal continuous time

PID controller can be expressed as:

$$u(t) = K_p[e(t) + \frac{1}{T_i}\int_0^t e(t)\, d(t) + T_d \frac{d}{dt} e(t)] \qquad (5.1)$$

Where $u(t)$ is the control output, K_p is constant coefficient of the proportional gain, T_i is integral

time or reset time, T_d is the derivative time or rate time and e is the error between the reference V_{Ref} and output V_o, the transfer function of corresponding PID controller is given as

$$u(s) = [K_p + \frac{K_i}{s} + K_d]e(s)$$ (5.2)

Where K_P, $K_i=K_P/T_i$, and $K_d=K_P.T_d$ are the proportional, integral and the derivative gains of the controller, respectively. The continuous-time domain controller of (5.2) is transformed into the discrete-time domain using the backward difference method (5.3). Using this method, the discrete transfer function of a numerical integrator and numerical differentiator are obtained (5.4). Then, the discrete PID controller in z-domain is given by (5.5).

$$s = \frac{z-1}{z*T_s}$$ (5.3)

$$u(z) = [K_p + \frac{K_i T_i z}{z-1} + \frac{K_d}{T_s}\frac{z-1}{z}]e(z)$$ (5.4)

Rearranging gives

$$u(z) = [\frac{(K_p+K_d+K_i)+(-2K_d-K_i)z^{-1}+K_d z^{-2}}{1-z^{-1}}]e(z)$$ (5.5)

It assumes the open loop process curve to be of S- shape as given below. Then it assumes that the optimum response of the curve occurs when the ratio of successive peaks in closed loop response of the system is 4:1. Thus the PID controller parameters are thus evaluated as given below. For tuning of a PID controller, we use Zeigler Nicholas Process Reaction Curve Method shown in fig 5.4 [45].
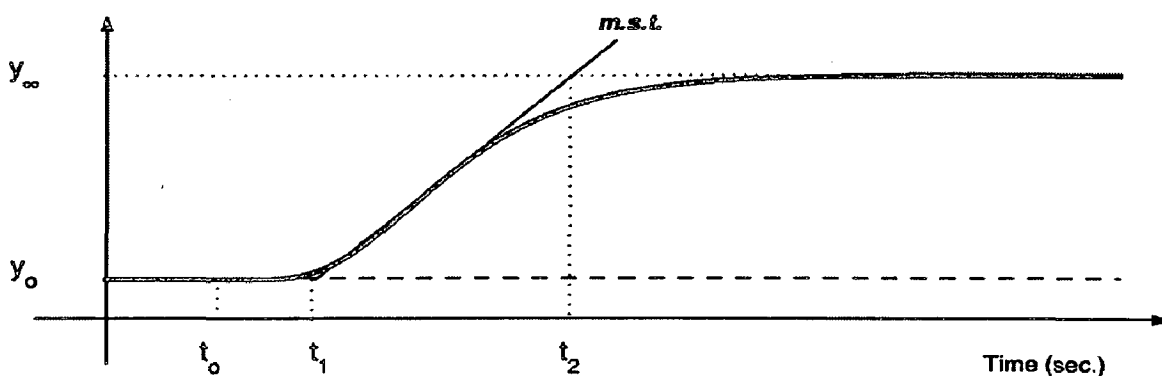
Fig 5.4: Process Reaction Curve Method

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Where

$$K_o = \frac{y_\infty - y_o}{u_\infty - u_0}; \quad \tau_o = t_1 - t_o; \quad \nu_o = t_2 - t_1;$$

And the desired K_p, T_r and T_d are then evaluated by the table below:

Table 5.1 Calculation of PID parameters

	K_p	T_r	T_d
P	$\dfrac{\nu_o}{K_o \tau_o}$		
PI	$\dfrac{0.9\nu_o}{K_o \tau_o}$	$3\tau_o$	
PID	$\dfrac{1.2\nu_o}{K_o \tau_o}$	$2\tau_o$	$0.5\tau_o$

Proportional Controller: A proportional controller is an amplifier with an adjustable gain. For a first order system, it always produces a steady state error. Increasing the gain reduces the steady state error but may result in instability for higher order plants.

PI Controller: The inclusion of an integrator reduces the steady state error. A first order system will give a second order response with PI controller.

PID Controller: The further inclusion of derivative controller generally gives improved damping and stability.

PID controller performance with disturbance: When some external disturbance is added, the process response is delayed further to achieve a response. But it is observed that system achieves a minimal steady state error as an effect of PID controller.

By using above method K_p, K_d, K_i values are found for the buck converter from the step response shown in the fig 5.5 and used in the simulation sown in fig 5.6 to get required results. Using those values discrete controller is designed.
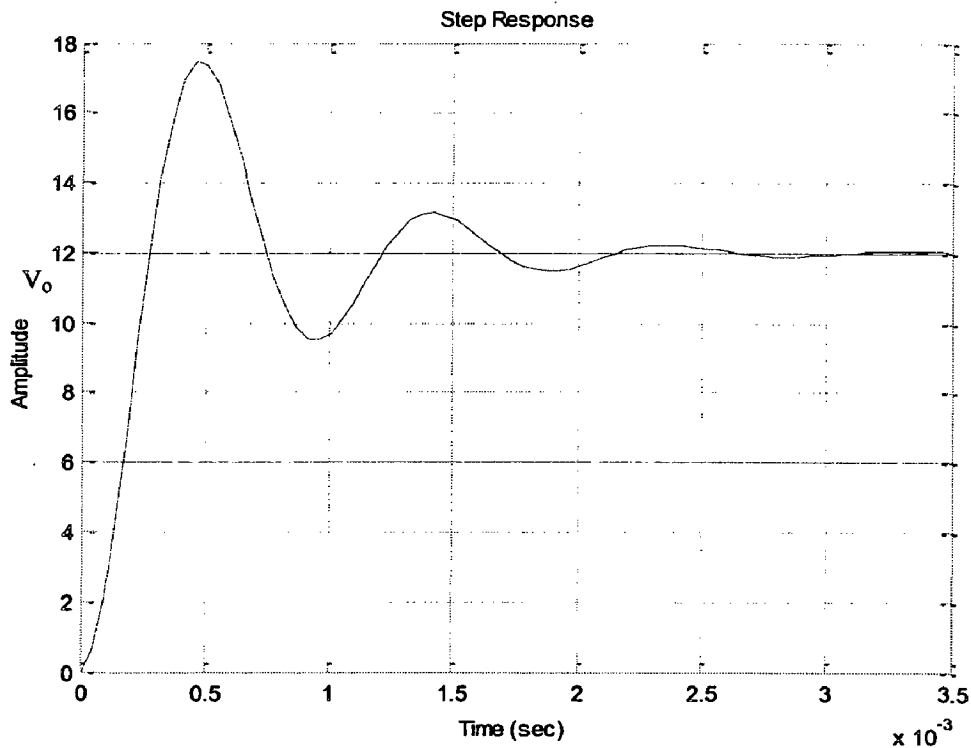
Fig 5.5: Step response of open loop buck converter

The ADC model consists of an element that performs subtraction of the output voltage value from the reference to generate the error voltage, S/H, quantization effects, delay, and saturation blocks. In the considered model, the DPWM generates the pulse signal corresponding to duty command presented by the controller and it has 8-bit resolution. The quantizer, gain block and a duty ratio limiter are included. The variable load and source voltage models are included in the converter to study the dynamic performances of the converter.

5.2.4 Closed loop Simulink model of buck converter

Modeling of the buck converter is done in MATLAB Simulink using the state space average method. Various blocks for the closed loop control are shown in fig 5.6. Every block is designed using MATLAB Simulink. The calculated PID values from Zeigler Nicholas are used for the
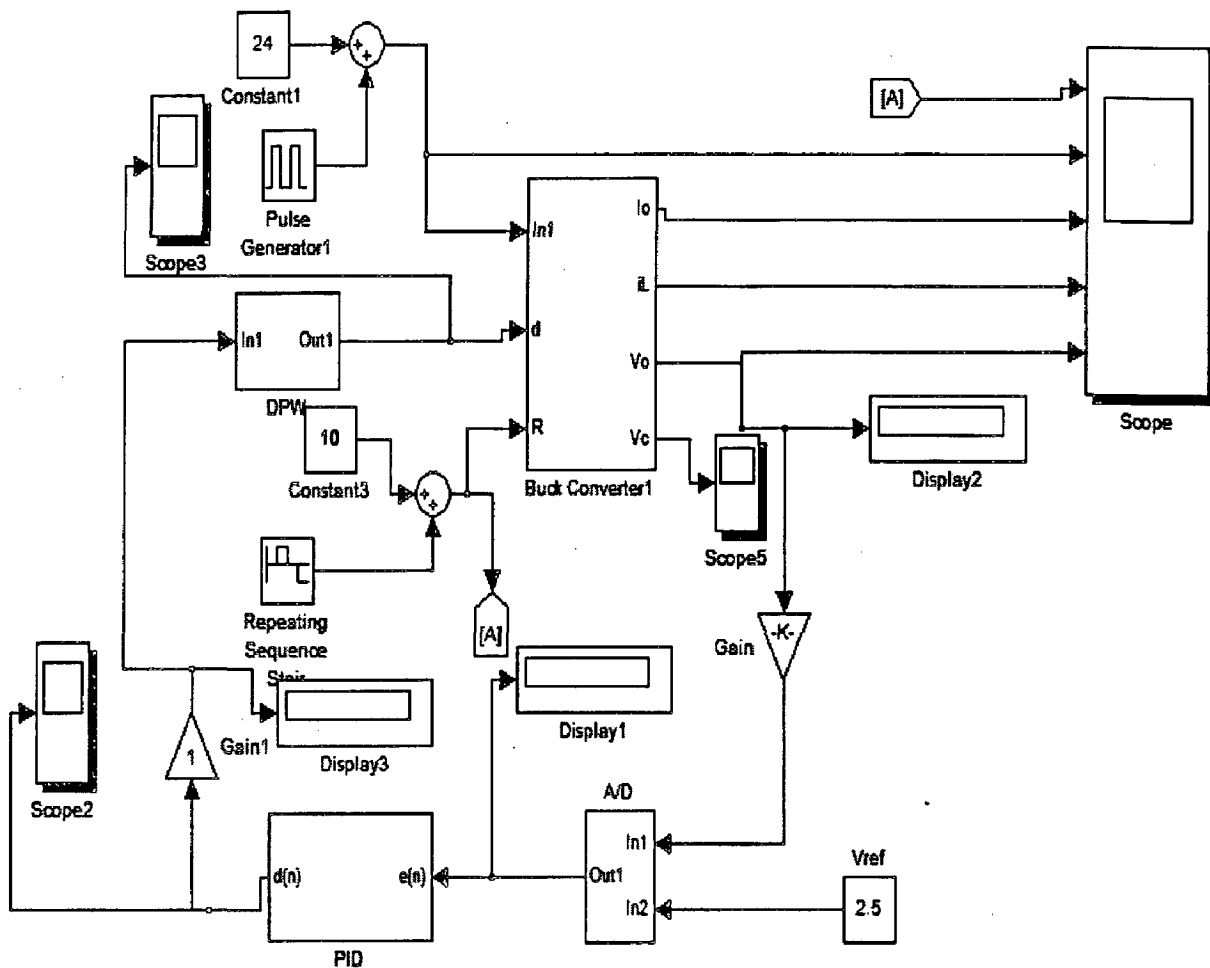
Fig 5.6: MATLAB simulation of buck converter using PID(digitally)

PID digital controller. Variable input voltage and variable load is provided to the system to check the proper functioning of the controller. In fig 5.7 we can clearly see load resistance is varied to see the effect on the output voltage and current. In buck converter the output current (I_o) is equal to the inductor current (i_L), so when the load resistance varies, the I_o and i_L varies accordingly i.e when R_L increases, I_o and i_L decreases, similarly when R_L decreases, I_o and i_L increases. In fig 5.8 input voltage is varied.

But due the variation in the input voltage the I_o, i_L does not change except small disturbance during the transition of the input voltage because of small variation in V_o. With variation in R_L and V_{in} the output voltage remains constant, this is done by the PID controller.
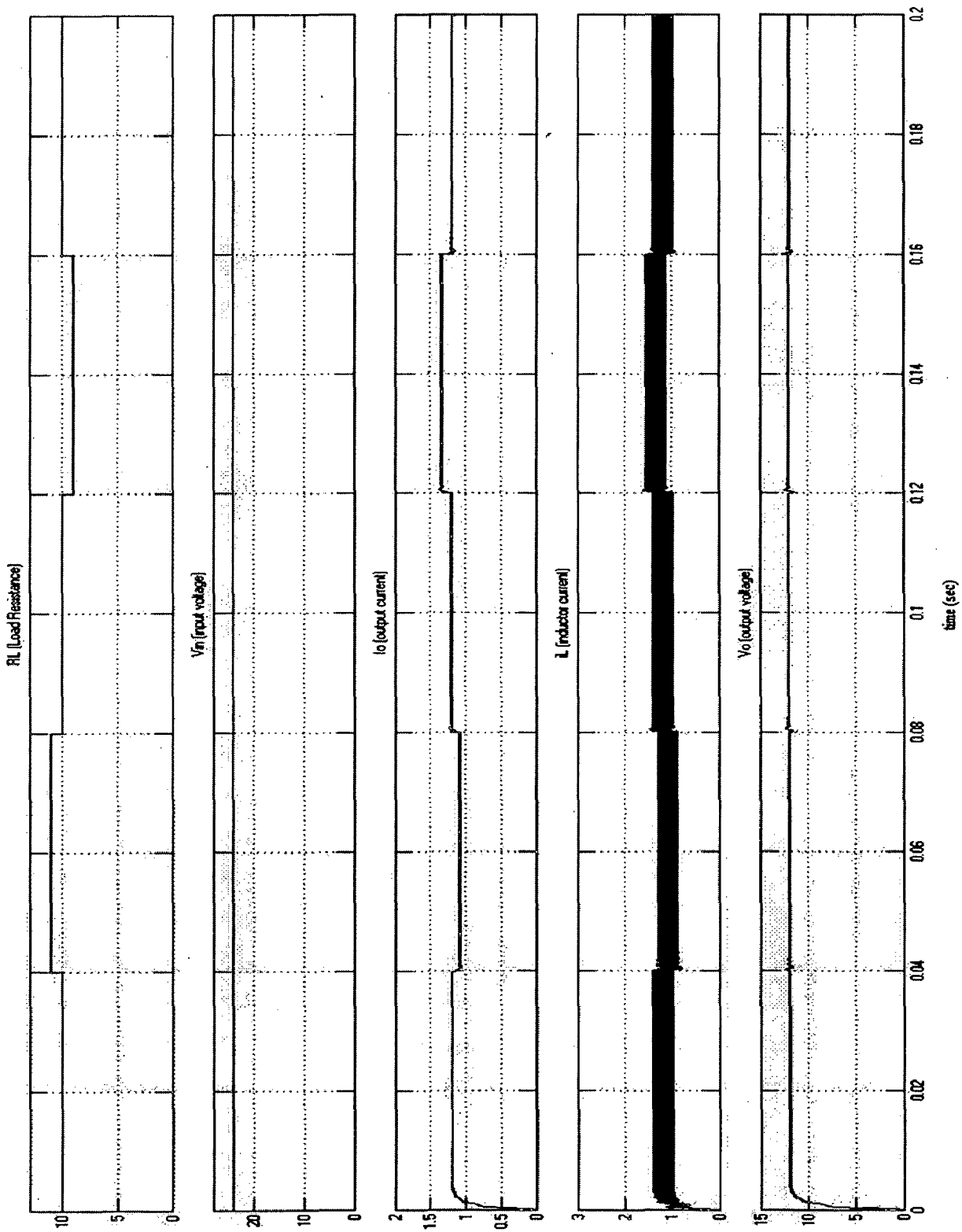
Fig 5.7: Simulation response of buck converter using PID(digital) with variation in load

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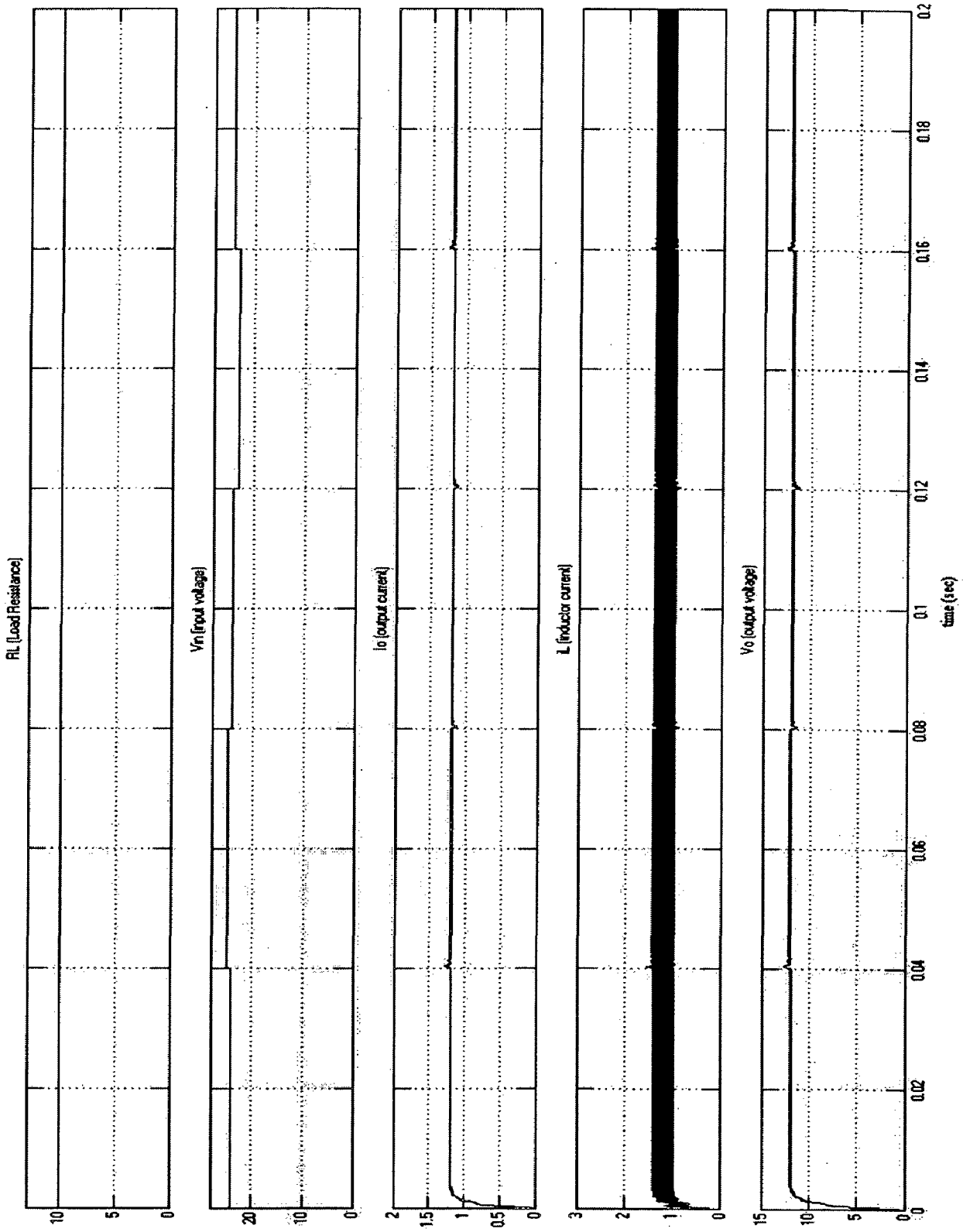
Fig 5.8: Simulation response of buck converter using PID (digital) with variation in V_{in}

Whenever the input voltage varies, the controller will adjust the duty cycle such that V_o remains constant. If the V_o has changed due to change in load then the controller adjusts the duty cycle such that V_o remains constant. The PID values should be tuned to get the satisfactory results. In fig.5.7 and fig 5.8 simulation results show high steady state and dynamic performances. The parameters used for the simulation are given in the appendix table A.1.

5.3 Boost Converter

Modeling of the boost converter is done using state space average method equations (4.41),(4.42) obtained in previous chapters. Using that equation Simulink model of boost converter shown in fig 5.9 is done in the MATLAB. After mathematical manipulation of the state-space equations, the final dynamic and output equations are made, to develop Simulink model of power stage.
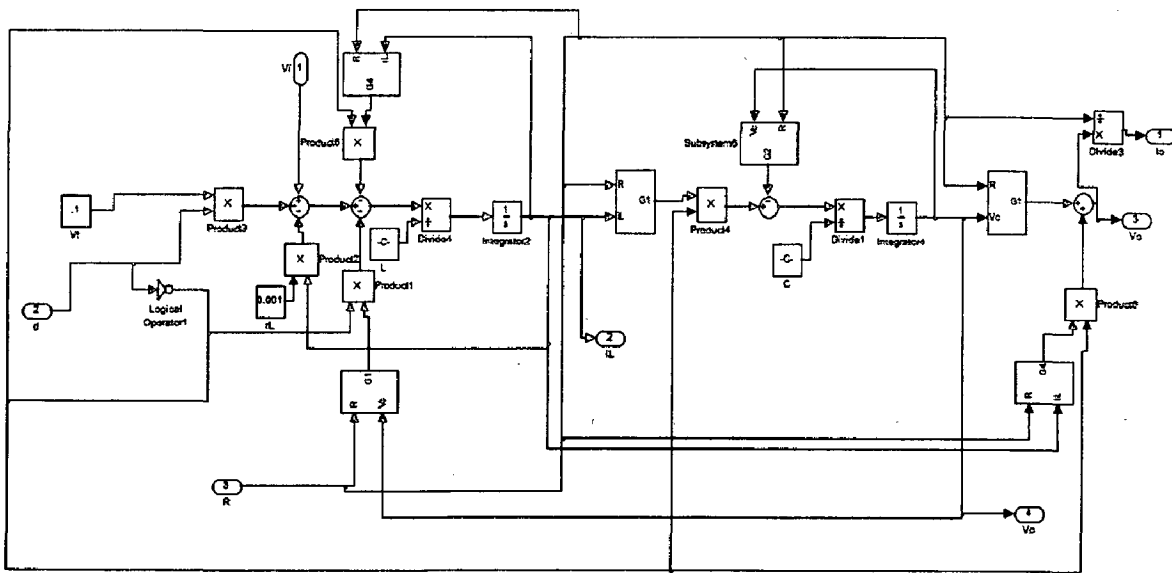
Fig 5.9: Simulink Model of Boost converter (Power stage using state-space)

5.3.1 DESIGN OF PID CONTROLLER

When we observe carefully, the transfer function of the boost converter has right hand zero (RHZ). The presence of RHZ makes the system unstable, when one observe the step response of

the boost converter using state space transfer function of boost converter, it clearly shows the undershoot, for these kind of responses we cannot use Zeigler Nicholas tuning method.
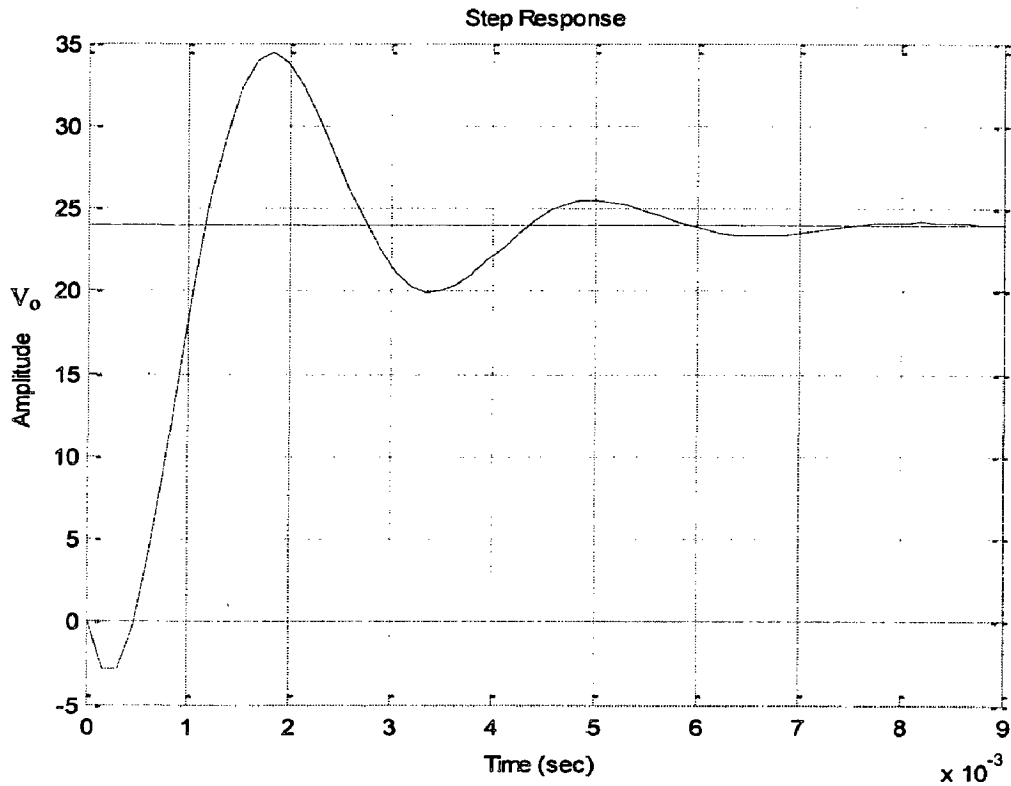
Fig 5.10: Step response of open loop boost converter

The above fig 5.10 shows the undershoot, so an analog controller is first designed in the continuous domain as if one were building continuous time control system, by ignoring the effects of sampling and hold associated with the A/D converter and the digital PWM circuits. The analog controller is then converted to a discrete-time compensator by some approximate techniques like bilinear transformation. Using this technique the type 3 compensation of analog design is converted into digital domain (discrete) by using bilinear transformation and it acts as a PID controller for the boost converter.

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The other method is using fuzzy controller. It gives more satisfying results as we can design the non-linear controller with the fuzzy. Brief details of the fuzzy technology are given below.

5.3.2 Fuzzy Controller

Linear controllers for DC-DC converters are usually designed based on mathematical models. To obtain a certain performance objective, an accurate model is essential. For the boost converter's small signal model, the poles and a right half plane zero, as well as the magnitude of the frequency response, are all dependent on the duty cycle D. This makes the transfer function of the boost converter's small signal model a nonlinear function of the duty cycle. The right-half plane zero and the nonlinear nature of the boost converter's small signal model makes the control design for this converter more challenging from the point of view of stability and bandwidth

To achieve a stable and fast response, two solutions are possible. One is to develop a more accurate model for the converter. However, the model may become too complex to use in controller development. A second solution is to use a nonlinear controller . Since fuzzy controllers don't require a precise mathematical model, they are well suited to nonlinear, time-variant systems. Different from conventional control, fuzzy control is based on the expert knowledge of the system. Fuzzy control provides a formal methodology to represent and implement a human's heuristic knowledge about how to control the system. A block diagram of a fuzzy control system is shown in Figure 5.11.

A fuzzy controller contains four main components: (1) the fuzzification interface that converts its inputs into information that the inference mechanism can use to activate and apply rules, (2) the rule base which contains the expert's linguistic description of how to achieve good control,(3) the inference mechanism that evaluates which control rules are relevant in the current situation, and (4) the defuzzification interface which converts the conclusion from the inference mechanism into the control input to the plant .
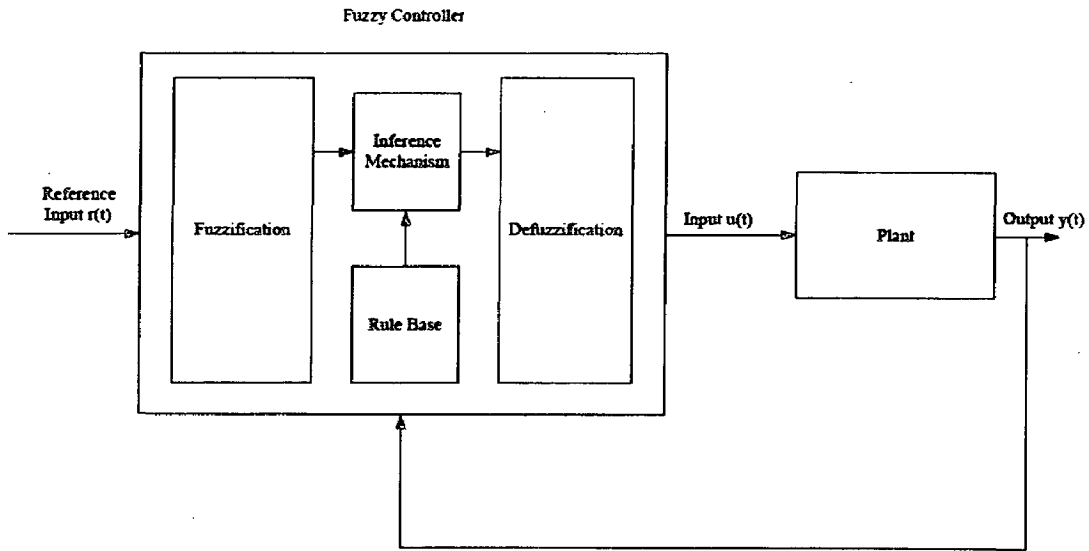
Fig 5.11: Block diagram of fuzzy control system

The performance objectives and design constraints are the same as those for conventional control. Design of fuzzy controllers involves the following procedures: (1) choose the fuzzy controller's inputs and outputs, (2) choose the preprocessing for the controller inputs and post processing for the controller outputs, and (3) design each of the four components of the fuzzy controller shown in Figure 5.11.

Table 5.2 Rule base

		Change in error (CE)						
		NB	NM	NS	Z	PS	PM	PB
Error (E)	PB	Z	NS	NM	NM	NB	NB	NB
	PM	PS	Z	NS	NM	NM	NM	NB
	PS	PM	PS	Z	NS	NS	NM	NB
	Z	PM	PM	PS	Z	NS	NM	NM
	NS	PB	PM	PS	PS	Z	NS	NM
	NM	PB	PM	PM	PM	PS	Z	NS
	NB	PB	PB	PB	PM	PM	PS	Z

The rule base for the fuzzy controller is made using above table and the satisfied results are observed in the MATLAB simulation.

5.3.3 Closed loop Simulink model of boost converter

Modeling of the boost converter is done in MATLAB Simulink using the state space average method. Various blocks for the closed loop control are shown in fig 5.12. Every block is designed using MATLAB Simulink. The controller block is replaced by discretized type III controller and fuzzy controller. The ADC model consists of an element that performs subtraction of the output voltage value from the reference to generate the error voltage, S/H, quantization effects, delay, and saturation blocks. In the considered model, the DPWM generates the pulse signal corresponding to duty command presented by the controller and it has 8-bit resolution.
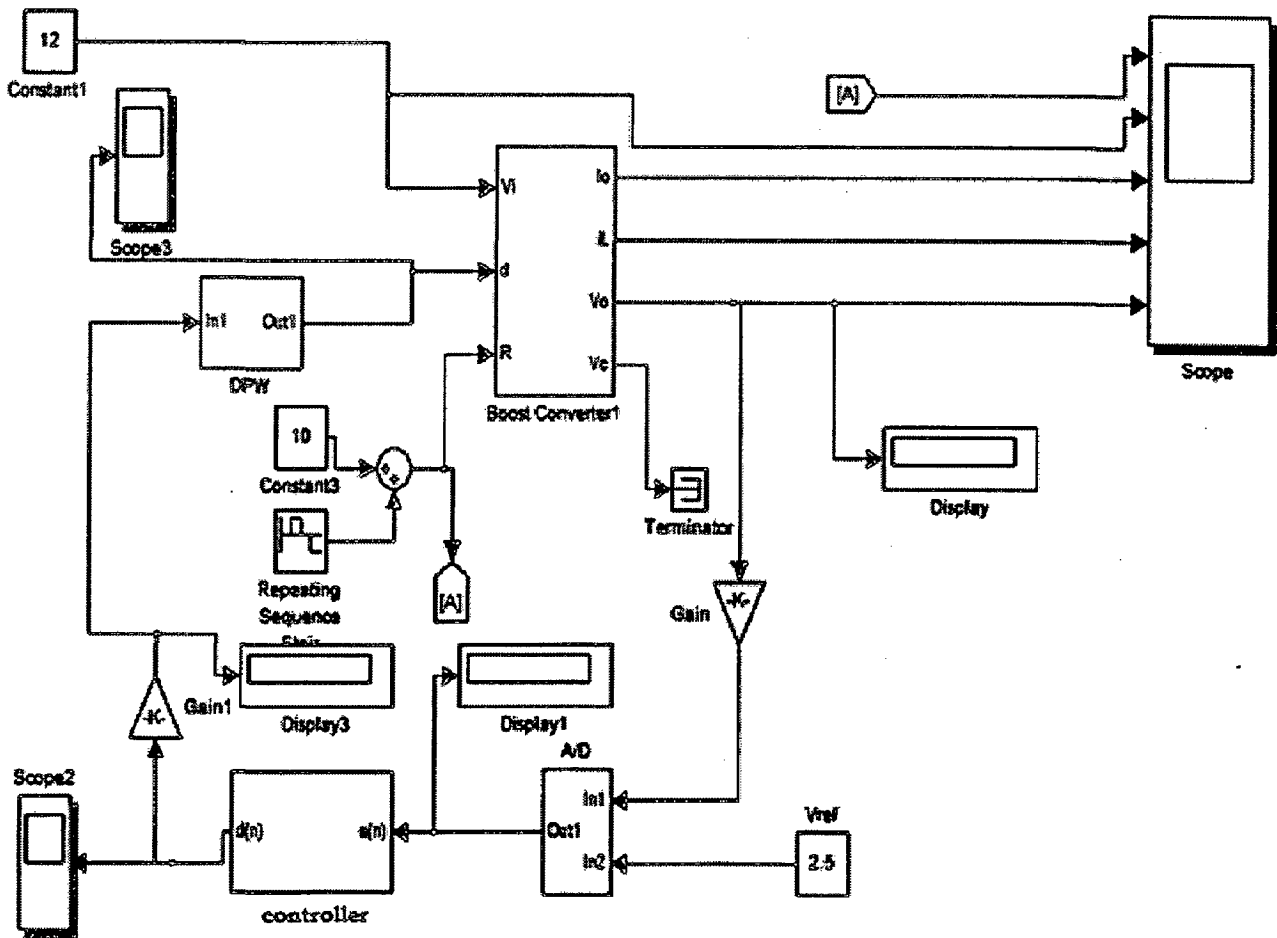
Fig 5.12: MATLAB simulation of boost converter using type III (discretized) or fuzzy controller

Fig 5.13: Simulation response of boost converter using Type III (digital) with variation in Vin
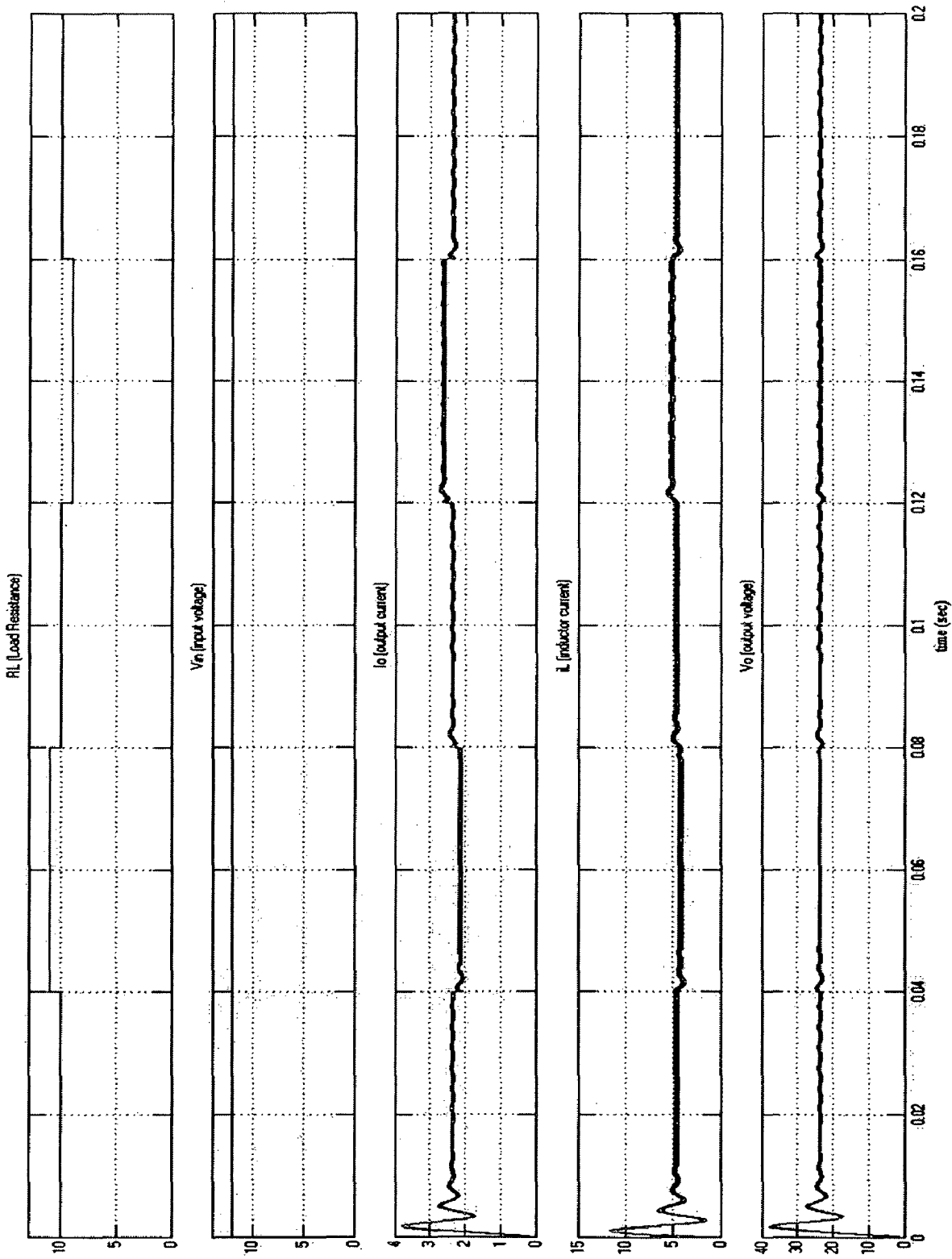
Fig 5.14: Simulation response of boost converter using Type III (digital) with variation in R

The quantizer, gain block and a duty ratio limiter are included. The variable load and source voltage models are included in the converter to study the dynamic performances of the converter.

Variable input voltage and variable load is provided to the system to check the proper functioning of the controller. In fig 5.14, fig 5.15 the load resistance is varied to see the effect on the output voltage and current. In boost converter the inductor current(i_L) is equal to the input current (I_{in}) which varies with both R_L and V_{in}, so when the load resistance varies, I_o and i_L varies accordingly i.e. when R_L increases, I_o and i_L decreases, similarly when R_L decreases, I_o and i_L increases. In fig 5.15, fig 5.13 the input voltage is varied then the output current I_o does not change, except small disturbance during the transition of the input voltage because of small variation in V_o. Increase in the input voltage causes the i_L to decrease and decrease in V_{in} increase the i_L. With variation in R_L and V_{in} the output voltage remains constant, this is done by the type III controller or fuzzy controller. Whenever the input voltage varies, the controller will adjust the duty cycle such that V_o remains constant. If the V_o has changed due to change in load then the controller adjusts the duty cycle such that V_o remains constant. So fig 5.13, fig 5.14,fig 5,15, fig 5.16 shows that the designed type III controller and fuzzy controller is providing satisfactory results for the boost converter.

In fig 5.13, fig 5.14 the maximum overshoot is very high. If we decrease the gain then the response time is slow, the gain has to be adjusted in such a way that the maximum overshoot should not be more than the system limitations. But the speed of response is good. The dynamic performance is also good. The initial high currents are the inrush currents due to the capacitor which can be limited by using soft switching. In fig 5.15, fig 5.16 maximum overshoot is less but the initial oscillations are high. These can be removed by writing more number of rules but they are not necessary because the dynamic performance and steady state performance are good. The more the number of the rules in the rule base the finer the controlling power of the controller. Generally the in-direct designed type controller is preferred that the fuzzy controller because of the its difficulty to implement in DSP or FPGA. The parameters used fror the simulations are given in the appendix table A.1 and A/D, DPWM, FUZZY, discrete Type III models are shown in fig A.1 to A.5
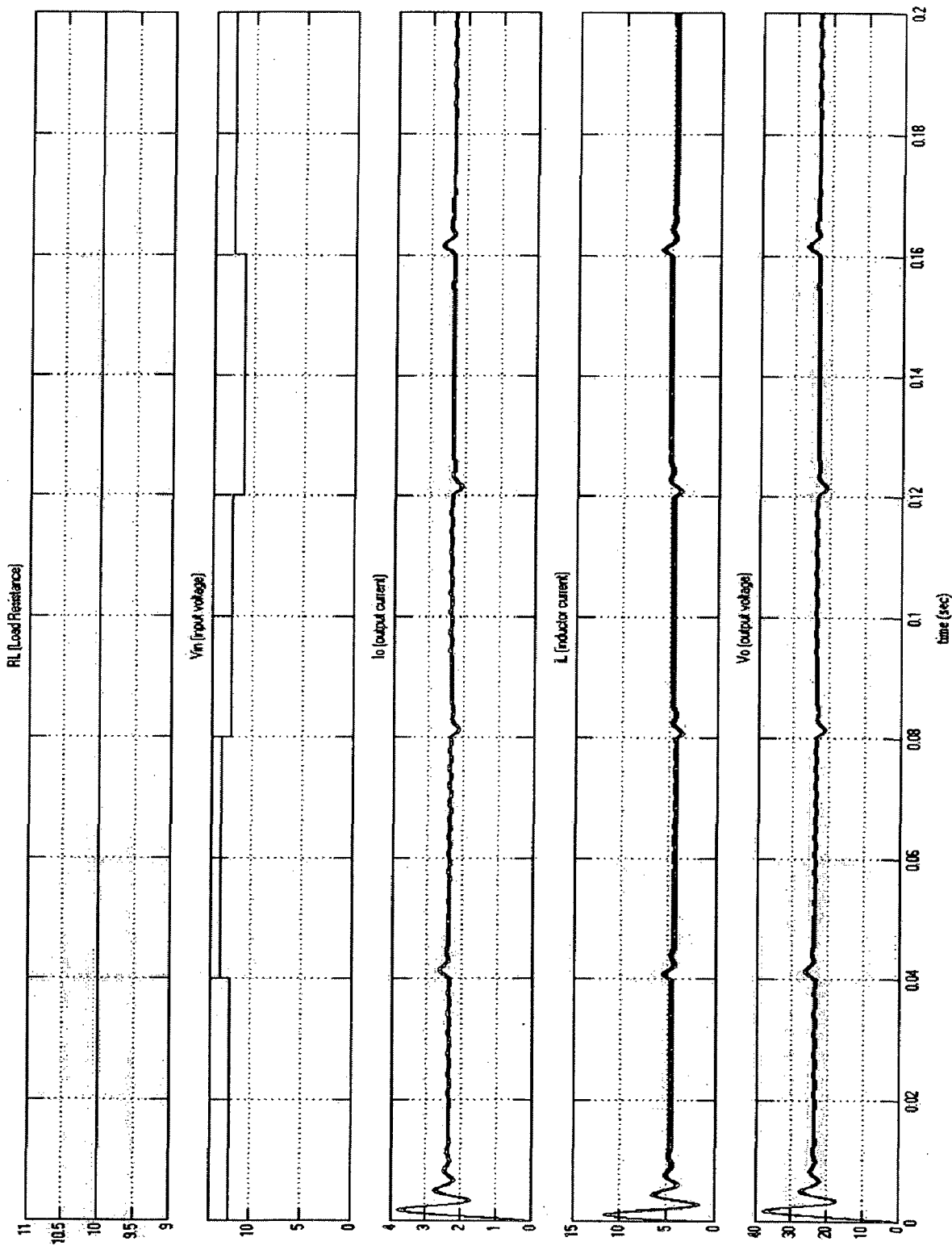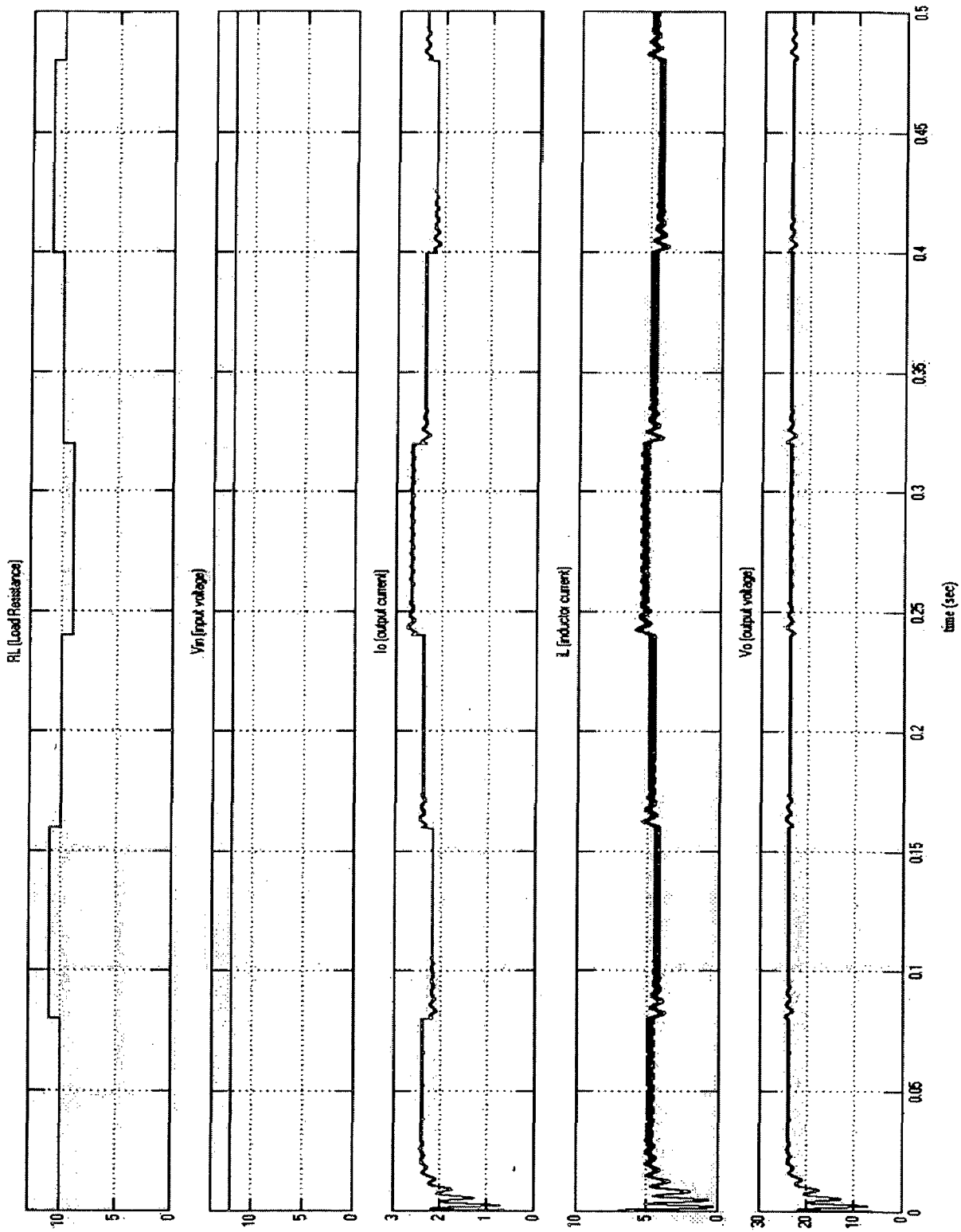
Fig 5.15: Simulation response of boost converter using FUZZY controller with variation in R

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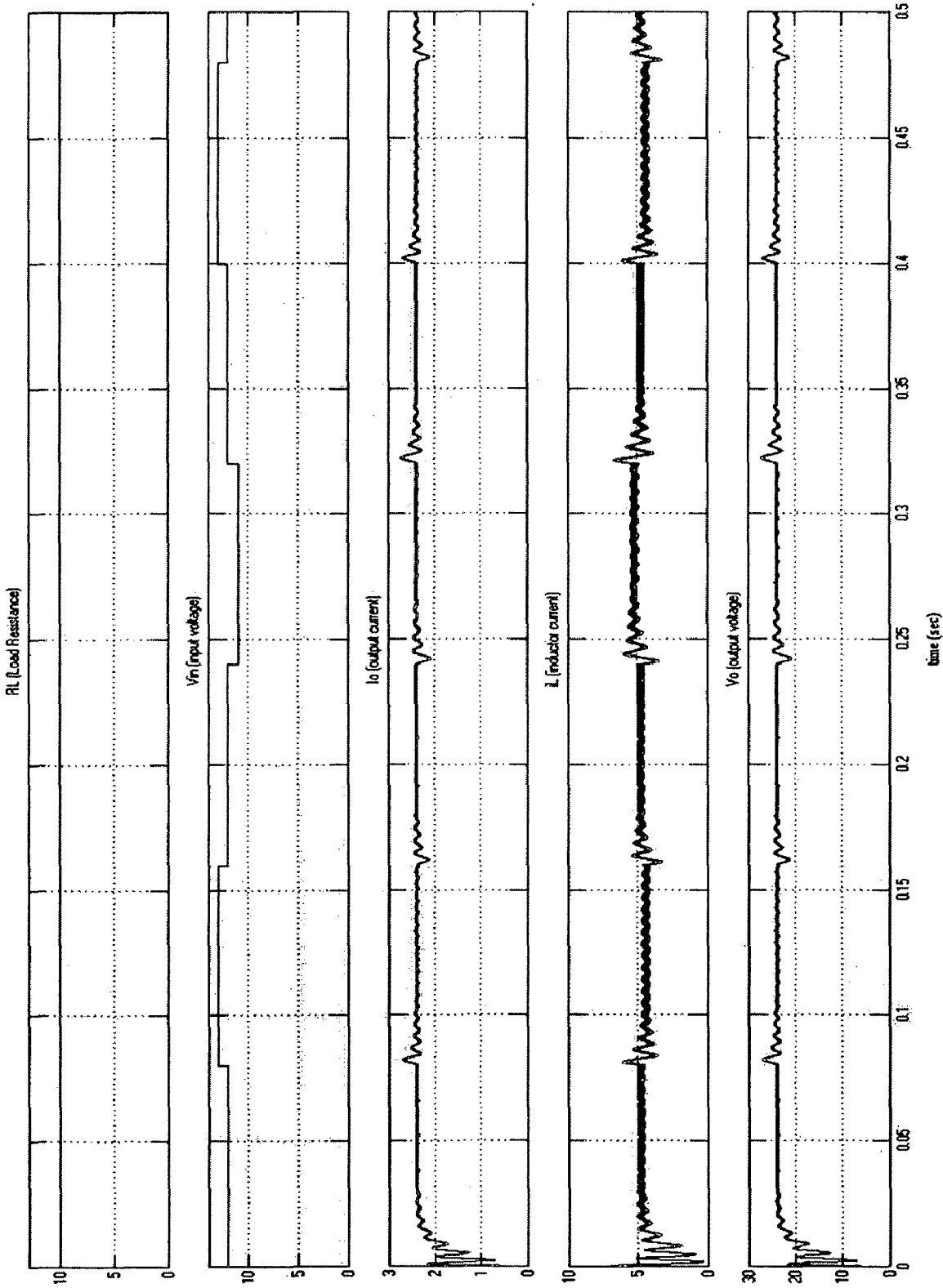
Fig 5.16: Simulation response of boost converter using FUZZY controller with variation in V_{in}

5.4 Hardware Implementation

It is similar to the Analog bi-directional converter, the only difference here is that the PWMs are generated using DSP kit. The simulink model is done in MATLAB and dumped into DSP.

5.4.1 Digital Signal Processor

A. Overview of Digital Signal controllers

A digital signal controller (DSC) can be thought of as a hybrid of microcontrollers and digital signal processors (DSPs). Like microcontrollers, DSCs have fast interrupt responses, offer control-oriented peripherals like PWMs and watchdog timers, and are usually programmed using the C programming language, although they can be programmed using the device's native assembly language. On the DSP side, they incorporate features found on most DSPs such as single-cycle multiply–accumulate (MAC) units, barrel shifters, and large accumulators. Not all vendors have adopted the term DSC. The term was first introduced by Microchip Technology in 2002 with the launch of their 6000 series DSCs and subsequently adopted by most, but not all DSC vendors. For example, Infineon and Renesas refer to their DSCs as microcontrollers.)

DSCs are used in a wide range of applications, but the majority of applications are in motor control, power conversion, and sensor processing applications. Currently DSCs are being marketed as green technologies for their potential to reduce power consumption in electric motors and power supplies.

DSCs, like microcontrollers and DSPs, require software support. There are a growing number of software packages that offer the features required by both DSP applications and microcontroller applications. Code Composer Studio (CCS) is one such software package used for developing applications for Texas Instruments embedded processors. More details of CCS are included in the topics of this chapter.

B. Specifications of 28335eZdsp

The Texas Instruments (TI) TMS320F28335 is a 32-bit Digital Signal Controller (DSC) that is used in high performance control applications such as motor control, power conversation, optical networking. The eZdsp F28335 is a stand-alone card--allowing developers to evaluate the TMS320F28335 digital signal controller (DSC) to determine if it meets their application requirements. Furthermore, the module is an excellent platform to develop and run software for the TMS320F28335 processor .Different Tables in Appendix-A summarizes the basic features of TMS320F28335 DSC with detailed pin diagram.

C. Key Features of the F28335 eZdsp

- TMS320F28335 Digital Signal Controller

- 150 Mhz. operating speed

- On chip 32-bit floating point unit

- 68K bytes on-chip RAM

- 512K bytes on-chip Flash memory

- 256K bytes off-chip SRAM memory

- On chip 12 bit Analog to Digital (A/D) converter with 16 input channels

- 30 MHz. input clock

- On board RS-232 connector with line driver

- On board CAN 2.0 interface with line driver and connector

- Multiple Expansion Connectors (analog, I/O)

- On board embedded USB JTAG Controller

- 5-volt only operation with supplied AC adapter

- On board IEEE 1149.1 JTAG emulation connector

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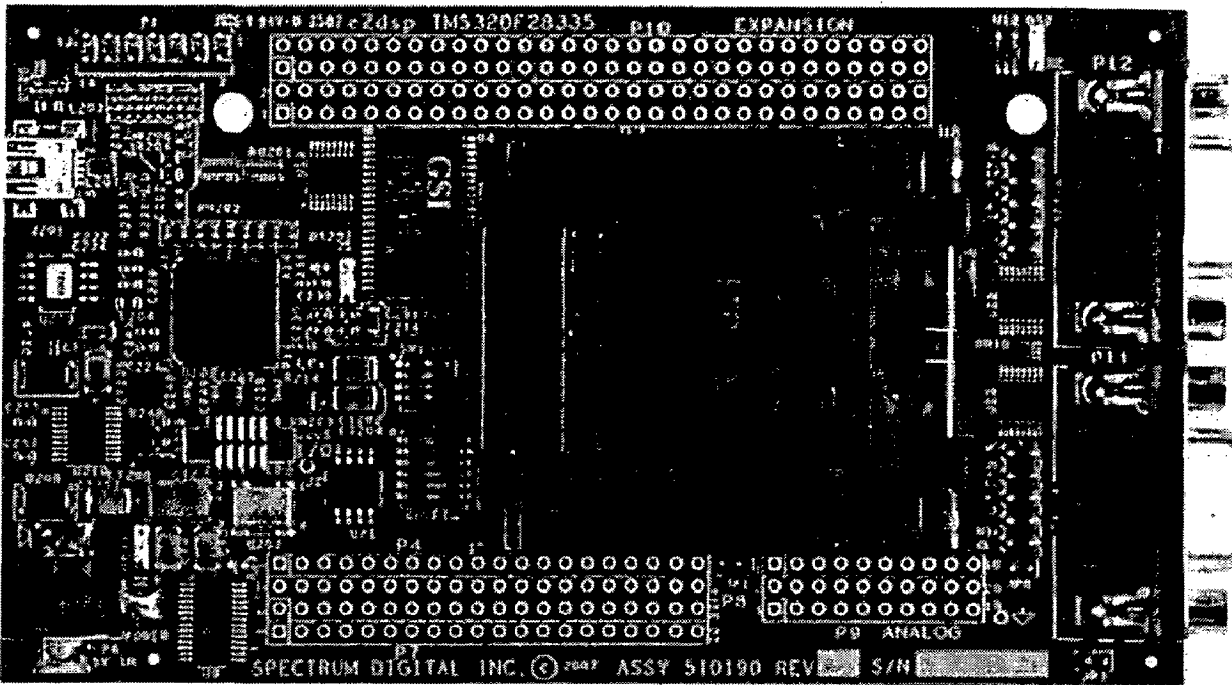
Fig 5.17: The pictorial view of eZdsp F28335 kit

The all above features make this DSC more practical. The major advantage of DSC is that it has enhanced PWM(ePWM) signals. Essentially a ePWM is counter which can be programmed in three different ways i.e. down counting mode, up counting mode and up-down counting mode. This DSC has six ePWM modules each capable of giving two signals.the module includes sub modules of time base module, event trigger module .dead band module (enables a dead band area of no signal overlap) etc.

Another important peripheral of this DSC is ADC. The purpose of ADC is to convert sensed analog current and voltage signals into digital. The ADC module provided is unipolar one and has 16 channels, configurable as two independent 8-channel modules; each module has choice of selecting any one of the respective channels available through MUX. The resolution of ADC is 3/4096.

5.4.2 Implementation

The PWM are created using Texas Instrument's **Code Composer Studio (CCS)** is a user-friendly, Windows-based debugger for developing and debugging software for the TMS320F28335. It allows users to write and debug code in C or in TI assembly language. **Simulink Code Generator**

- Automatically generates C code from your Simulink model.
- Generates optimized customizable code.
- There are several styles of generated code, which can be classified as either embedded (production phase) or rapid prototyping.
- Supports all Simulink features, including 8-, 16-, and 32-bit integers and floating-point double and single data types.
- Provides fixed-point capabilities for scaling of integer words ranging from 1 (unsigned) or 2 (signed) to 32 bits. Code generation is limited by the implementation of char, short, int, and long in embedded C compiler environments (usually 8, 16, and 32 bits, respectively).
- Generates processor-independent code.
- A separate run-time interface is used to execute this code.

By using this software the PWM are produced with the help of Simulink model in the MATLAB. It generates code of dsp for the Simulink model.

For open loop at 0.5 duty cycle pulses are created to check open-loop function of both buck and boost converter. The Simulink model of the set is shown below.

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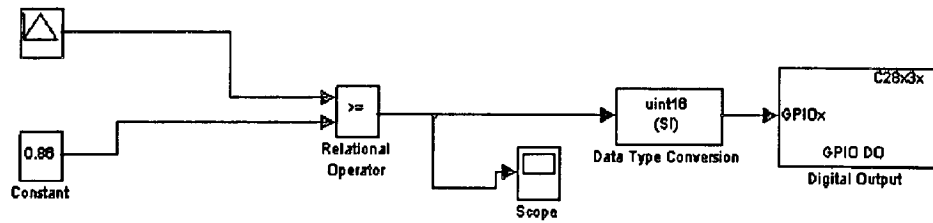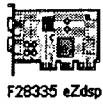
Fig 5.18: Simulink model for PWMs in DSP.

For closed loop control, the generation of source code for the feedback circuit is tested using the environment controller. The schematic or the Simulink model is given below shown in fig 5.19.
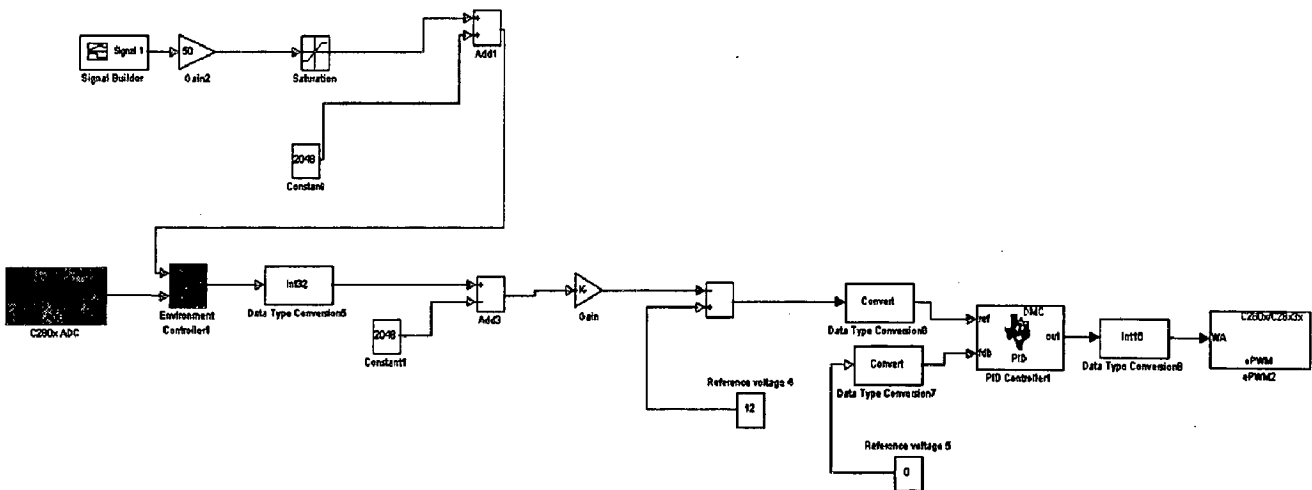
Fig 5.19: Simulink model of closed loop for DSP.

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5.4.3 Hardware Results
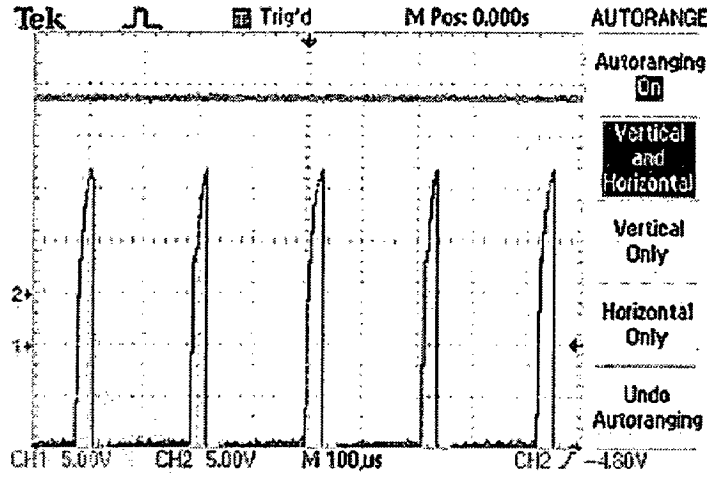
Fig 5.20: BDC in boost mode using DSP (12V to 24V).
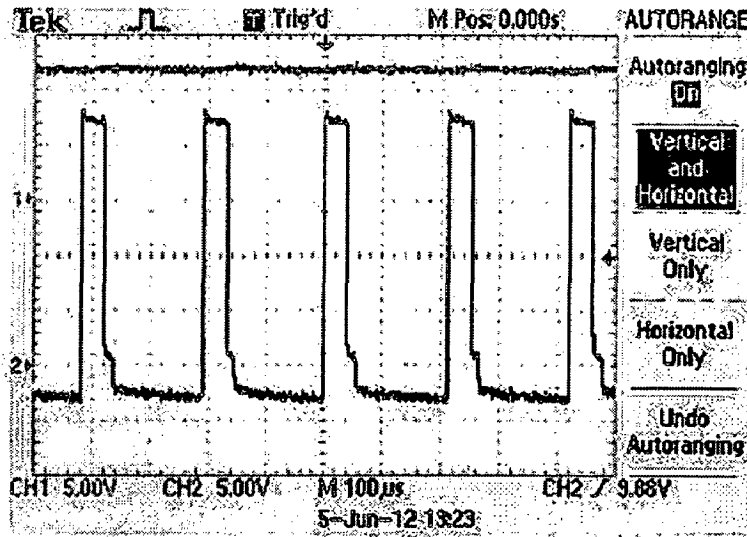
Fig 5.21: BDC in buck mode using DSP (24V to 12V).

The boost operation and buck operation of BDC are shown in the fig 5.20 and fig 5.21. In fig 5.20 V_{in}=12V is converted to 24V and in fig 5.21 V_{in}=24V is converted to 12V. The PWMS for the BDC are generated from the DSP using Code Composer Studio (CCS) from the model shown in the fig 5.18. for boost mode operation the PWM of the duty ratio 0.2 are given to switch T_2 in fig 4.34 and no gate pulse is given to switch T_1. Similarly for the buck mode

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operation PWM of the duty ratio 0.2 are given to switch T_1 in fig 4.34 and no gate pulse is given to switch T_2. The parameters used for the hardware setup is given in the appendix table A.3.

5.5 Conclusion

Digital control design, modeling for DC-DC converters using linear and nonlinear control methods is done. The design of the controllers is done using direct, in-direct approach and fuzzy technique also used. For buck mode operation of BDC normal PID controller is designed using the Zeigler Nicholas method and simulated. For the boost mode operation of BDC type III discretized controller and fuzzy controller has been designed and simulated. Satisfying simulation results are achieved. Then the open loop BDC is implemented using DSP kit. The parameters used for the hardware setup is given in the appendix table A.3. The variable DC power supply of 25V, 1A is used. BDC in boost mode is able to operate at appr (12, 240mA). BDC in buck mode is able to operate approx. between (24V, 120mA). The limitations of ratings used for testing are solely based on the availability of the power supply ratings and will work up to 50W for boost mode and 15W for buck mode.

CHAPTER-VI

CONCLUSION AND FUTURE SCOPE

[Presented in this chapter is work done, advantages of the digital control over analog control, the future scope.]

6.1 Conclusion

Bi-directional buck and boost converter is implemented using both the analog controller and digital controller. Satisfying results are obtained under closed loop for the bi-directional buck and boost converter using the analog controller. The same BDC is implemented in open loop using the DSP. The type III compensations or controllers are designed for the buck mode and boost mode for analog implementation. The buck and boost converters are modeled using Simulink MATLAB since Bi-directional buck and boost converter act as an independent buck converter and boost converter, then the modeled converters are simulated with the controller and satisfying results are achieved. Then independent buck converter and boost converters are implemented with IC tl494 using the type III compensation. Once the closed loop control is achieved then BDC buck and boost converter is implemented using those controllers. Satisfying hardware results are achieved in closed loop for both load and input voltage variation (using analog controller). For the digital closed loop implementation PID controller is designed and modeled for the buck converter and for the boost converter using in-direct approach, type III analog controller is converted to the digital controller is designed and also a fuzzy controller is designed, modeled. Using these controllers buck and boost converters are simulated and satisfying results are achieved. The variable DC power supply of 25V, 1A is used. BDC in boost mode is able to operate approx. between (9V-22V, 240mA). BDC in buck mode is able to operate approx. between (13V-24V, 1A). The limitations of ratings used for testing are solely based on the availability of the power supply ratings and will work up to 50W for boost mode and 15W for buck mode.

6.2 Pros and Cons of the Digital Control

For many years, analog controllers have dominated the control of power electronics systems. Digital controls have continued to improve in cost and usability in the past several years. This has made digital controls more appealing to replace analog control in some devices. The benefits of adding digital control in power electronics are not based solely on adding performance to the individually controlled components, but in system monitoring capabilities. In a distributed power system it would be very helpful to have the controllers alert the operator of a potential problem. This is not achievable using traditional analog control. Also digital control allows for a more complex control scheme than what can be achieved with traditional control. An example would be using nonlinear control. Also digital control allows more flexibility for change. Unlike analog control, using a digital signal processor to control a system allows for reprogramming should the need arise without having to switch out hardware. With all this in mind there are still some issues associated with digital control. One major issue is the delay introduced with a digital controller.

6.2.1 Pros of Digital Control

There are several reasons why digital control is desired over analog control. The following are citations directly from papers that address the digital pros over analog.

"Potential advantages of digital controller implementation include much improved flexibility, reduced design time, programmability, elimination of discrete tuning components, improved system reliability, easier system integration, and possibility to include various performance enhancements." [33].

"...the opportunity to realize non-linear, predictive and adaptive control strategies provides a strong reason why digital control could yield worthwhile advantages compared with traditional analog control concepts." [22]

"Some advantages of digital control are as follows:

(1) Digital components are less susceptible to aging and environmental variations.

(2) They are less sensitive to noise.

(3) Changing a controller does not require an alteration in the hardware.

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(4) They provide improved sensitivity to parameter variations." [23]

"...analog control circuits of power electronics products are becoming digitalized because of improvements of the following undesirable characteristics;

-Difficulty in adjusting,

-Lack of flexibility to higher functions and system alteration,

-Low reliability, and so on" [24]

"Technological advances in digital signal processors (DSPs), networking, microprocessors, and programmable logic devices (PLDs) have empowered designers with entirely new techniques and methodologies that were economically unthinkable two decades ago. These advances, along with increased performance demands, have fueled the push of digital technology deeper into the controlled devices. The justification often quoted for this push to digital includes reproducibility, increased stability, increased resolution, and decreased infrastructure costs (networks replace control wiring)." [25]

"Adaptive control remains inherently difficult using analogue systems. With digital current mode control, however, a variety of adaptive schemes are possible. ... Access can be gained to most control parameters in software. ... This gives potential for the investigation of other novel forms of adaptive control." After some cons were listed about digital control the paper goes on to say "... However, by taking proper care good system performance can be achieved." [26]

"The use of a Digital Signal Processor (DSP) and of Erasable Programmable Logic Devices (EPLD) make the board remarkably flexible and adaptive to different operation modes, requiring only software re-programming." [27]

As can be seen there are a few main points that all people see as advantages over analog control. First being that the controls are able to realize more complex control processes. Another advantage being that digital controllers can be reprogrammed to meet changing control needs when conventional analog controllers must be replaced. Another major advantage is that digital controllers are less sensitive to noise, which is good for power converters that switch at high

frequencies. Also digital controls provide monitor capability to the system that is unheard of with analog controllers.

6.2.2 Cons of Digital Control

With all the pros in mind of digital control over analog there must be some trade off. The following are citations directly from papers that address the digital pros over analog.

"Some of the disadvantages of digital control are as follows:

(1) Signal resolution due to finite word length of the digital processor.

(2) Limit cycles due to the finite word length of the digital processor or analog-to-digital (A/D) and digital-to-analog (D/A) converters.

(3) Time delays in control loop due to the computation of control algorithm by the processor." [23]

"Consequently, operating properties of the digital control system are inferior to an analog control system." [24]

"Using digital control introduces several features affecting the operation of the converter. Computation time, if 0 to 100% duty ratio operation is required, causes a two-cycle delay to be present in the current loop. To maintain an adequate phase margin, this delay must be accounted for in designing the current loop compensation. Resolution is an issue in sampled data systems. For example, the duty cycle can only be set to a finite resolution, depending on the system clock frequency. Also, the accuracy of the inductor current and output voltage sampling directly affects the regulation and dynamic characteristics of the converter. Finite word lengths for variables within the digital processor result in round off errors. Also, storing filter coefficients to finite precision affects the emulation accuracy of the digital compensators. Floating point processors may help to ease these constraints."[26]

6.3 Future Scope

- Implementation of Bi-directional DC-DC converter with artificial neural network controller (ANN). In the presence of DC mains the converter operates as buck converter and charges the battery. When the DC main fails, the converter operates as boost converter and the battery feeds the load. In both the modes the power switches are controlled by PWM technique and the PWM pulses are generated by application of ANN controller.

- Implementation of Bi-directional DC-DC converter with adaptive fuzzy logic controller. The power switches are controlled by Pulse Width Modulation technique and the pulses are generated by the application of fuzzy logic with an adoption algorithm.

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[1] Sumanth Pala and Dr.S.P. Singh: — "Design, Modeling and Implementation of Bi-directional Buck and Boost Converter", International Conference on Advances in Electronics, Electrical and Computer Science Engineering, EEC 2012, Dehradun, India. (Accepted for presentation).

APPENDIX

Table A.1 Power circuit specifications

PARAMETERS	BUCK CONVERTER	BOOST CONVERTER
V_{in}	24V	12V
V_O	12V	24V
D	0.5	0.5
C (μF)	22	83
R(LOAD)(Ω)	10	10
L (μH)	700	700
F_{sw}(kHz)	20	20
PWM CHIP	TL 494	TL 494

Table A.2 Parameters of type III compensation

Parameter of type III	Buck Converter	Boost converter
R1	5K Ω	5K Ω
R2	183 Ω	1K Ω
R3	546 Ω	400 Ω
C1	1.6 nF	91 pF
C2	1.5 μF	0.5 μF
C3	29 nF	45 nF

Table A.3 Power circuit specifications for hardware implementation

PARAMETERS	BUCK CONVERTER	BOOST CONVERTER
V_{in}	24V	12V
V_O	12V	24V
D	0.3	0.3
C (μF)	50	100
R(LOAD)(Ω)	100	0.3k
L (μH)	700	700
F_{sw}(kHz)	20	20
PWM CHIP	TL 494	TL 494

Table A.4 Parameters of the converter for the input voltage variation

PARAMETERS	BUCK MODE	BOOST MODE
V_O	12V	24V
C (μF)	50	100
R(LOAD)(Ω)	100	0.3 K
L (μH)	700	700
F_{sw}(kHz)	20	20
PWM CHIP	TL 494	TL 494

Table A.5 Parameters of the converter for the load variation

PARAMETERS	BUCK MODE	BOOST MODE
V_{in}	24V	12V
V_O	12V	24V
C (μF)	50	100
L (μH)	700	700
F_{sw}(kHz)	20	20
PWM CHIP	TL 494	TL 494

The transfer functions obtained for the buck and boost converter are respectively given in the equation (A.1), (A.2)

$$G_{type\ III} = \frac{1.226e006S^2+1.18e010S+2.606e013}{S^3+3.367e006S^2+2.076e011S} \tag{A.1}$$

$$G_{type\ III} = \frac{3.316e007S^2+2.059e011S+2.842e014}{S^3+1.206e007S^2+7.54e011S} \tag{A.2}$$

MATLAB FILE FOR TYPE 3 COMPENSATION:

```
Vd= input('Enter input voltage ');
Vo = input('Enter output voltage ');
Vr = input('enter the peak of sawtooth');
R = input('enter the load resistance');
fsw = input('Enter Switching Frequency in KHz ');
fsw = fsw*1E3
C = input('Enter value of C in uF ');
C = C*1E-6;
L = input('Enter value of L in uH ');
L = L*1E-6;
D=input('Enter the duty ratio')
R1 = input ('Enter value of R1 (K) between 2 & 5 ');
R1 = R1*1E3;
rC = input ('Enter value of ESR ');
rL = input ('Enter value of DCR ');
DBW = 0.3*fsw
FESR = 1/(2*3.1415926535*rC*C)
FLC= 1/(2*3.1415926535*sqrt(L*C))
Rz2 = (DBW/FLC)*(Vr/Vd)*R1
Cz2 = 1/(3.14159*Rz2*FLC)
Cp1 = Cz2/((2*3.14159*Rz2*Cz2*FESR)-1)
Rz3 = R1/((fsw/(2*FLC))-1)
Cz3 = 1/(3.14159*Rz3*fsw)
 s = tf('s');
G1 = (R1+Rz3)/(R1*Rz3*Cp1);
N1 = s + (1/(Rz2*Cz2));
N2 = s + (1/((R1+Rz3)*Cz3));
D0 = s;
D1 = s + ((Cp1+Cz2)/(Rz2*Cp1*Cz2));
D2 = s + (1/(Rz3*Cz3));
Type3 = G1*((N1*N2)/(D0*D1*D2));
figure(2)
grid
bode(Type3)
```

Design of the fuzzy controller in MATLAB

Fig A.1: Simulink model of the fuzzy controller with a linear integrator for the DC-DC converters Method 2:(d[k] = K$_I$*I[k]+h*δd[k])

Design of the PID controller in MATLAB

Fig A.2: Simulink model of the PID controller

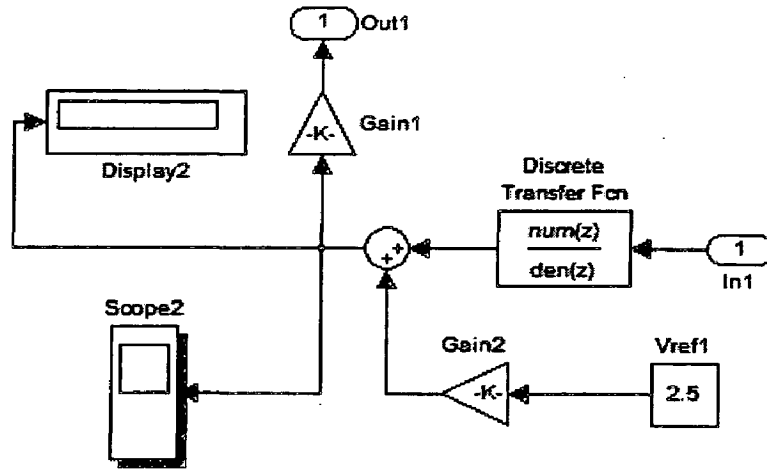# Design of the controller in MATLAB (Design by Emulation)
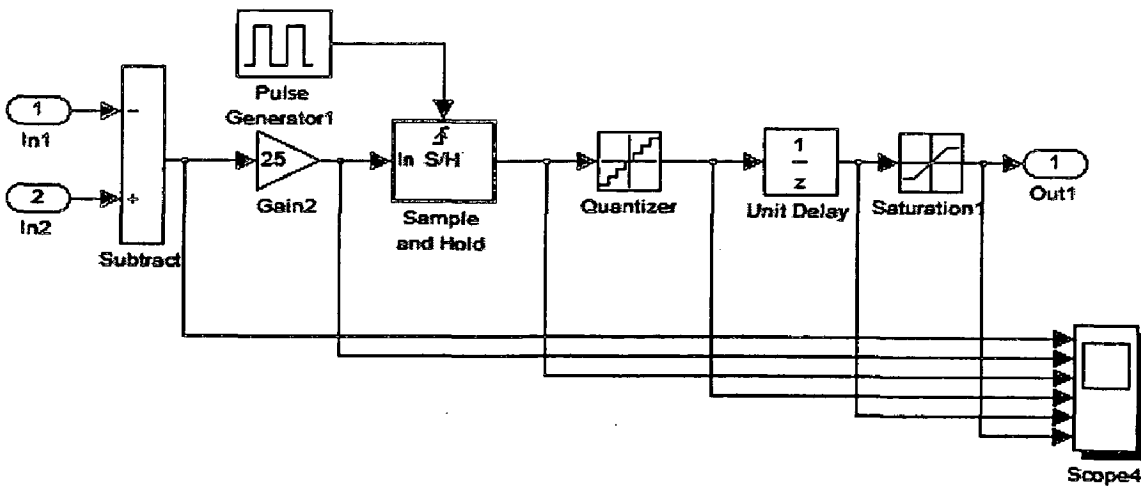

Fig A.3: Simulink model of the controller

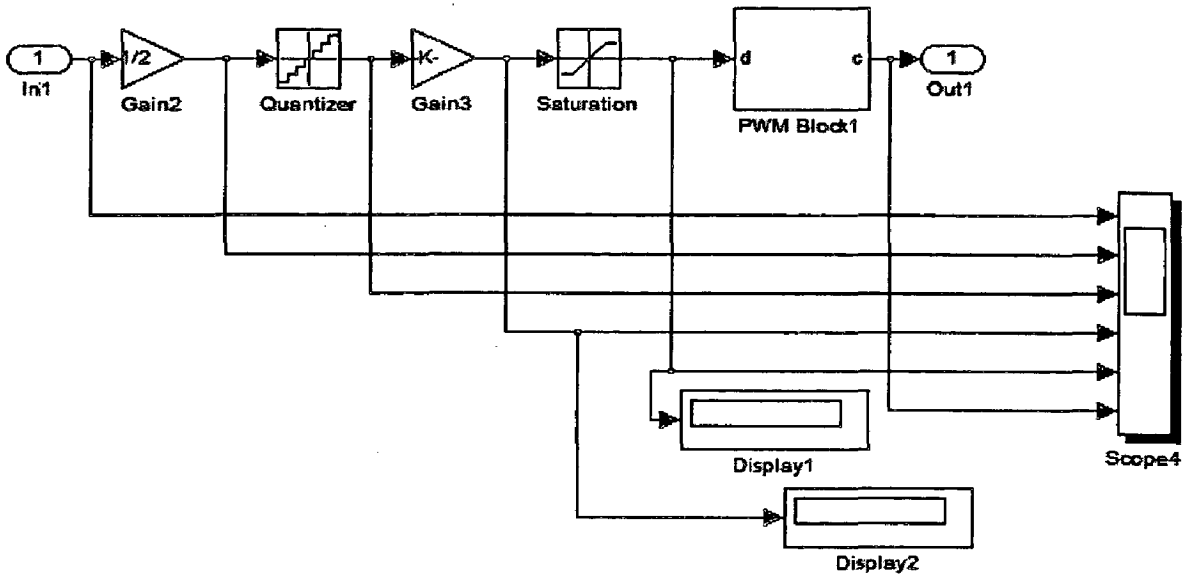# A/D converter

Fig A.4: Simulink model of the A/D converter

DPWM

Fig A.5: Simulink model of the DPWM.

(M) MOTOROLA

SWITCHMODE™ Pulse Width Modulation Control Circuit

The TL494 is a fixed frequency, pulse width modulation control circuit designed primarily for SWITCHMODE power supply control.

o Complete Pulse Width Modulation Control Circuitry
o On–Chip Oscillator with Master or Slave Operation
o On–Chip Error Amplifiers
o On–Chip 5.0 V Reference
o Adjustable Deadtime Control
o Uncommitted Output Transistors Rated to 500 mA Source or Sink
o Output Control for Push–Pull or Single–Ended Operation
o Undervoltage Lockout

TL494

SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUIT

SEMICONDUCTOR
TECHNICAL DATA

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

N SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS

(Top View)

MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted.)

Rating	Symbol	TL494C	TL494I	Unit
Power Supply Voltage	VCC	42		V
Collector Output Voltage	VC1, VC2	42		V
Collector Output Current (Each transistor) (Note 1)	IC1, IC2	500		mA
Amplifier Input Voltage Range	VIR	–0.3 to +42		V
Power Dissipation @ TA ≤ 45°C	PD	1000		mW
Thermal Resistance, Junction–to–Ambient	RθJA	80		°C/W
Operating Junction Temperature	TJ	125		°C
Storage Temperature Range	Tstg	–55 to +125		°C
Operating Ambient Temperature Range TL494C TL494I	TA	0 to +70 –25 to +85		°C
Derating Ambient Temperature	TA	45		°C

NOTE: 1. Maximum thermal limits must be observed.
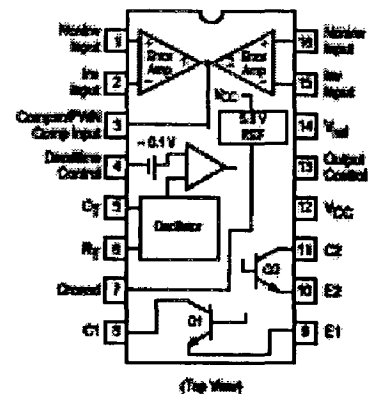
ORDERING INFORMATION

Device	Operating Temperature Range	Package
TL494CD	TA = 0° to +70°C	SO–16
TL494CN		Plastic
TL494IN	TA = –25° to +85°C	Plastic

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Submitted by Shri / Mrs ...Sumanth Pala...

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(Batch ...2007-15...) for further necessary action at your end please.

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For ASSTT. REGISTRAR (ACD.)
15/6/12

Encl. : As Above