DSP BASED REAL TIME SIMULATION OF A SMALL HYDRO POWER PLANT

A DISSERTATION

Submitted in partial fulfillment of the
requirements for the award of the degree
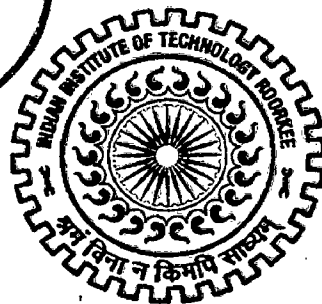*of*
MASTER OF TECHNOLOGY
in
ELECTRICAL ENGINEERING
(With Specialization in Power System Engineering)

By

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JUNE, 2008

Candidate's Declaration

I here by declare that the work presented in this dissertation entitled "DSP BASED REAL TIME SIMULATION OF SMALL HYDRO POWER PLANT" in the partial fulfillment of the requirement for the award of the degree of Master of Technology in Civil Engineering with the specialization in **Power System Engineering**, submitted in the department of Civil engineering, Indian Institute of Technology Roorkee, Roorkee, is an authentic record of my own work carried out from September 2007 to June 2008 under the supervision of **Dr. J.D. Sharma**, Professor, Department of Electrical Engineering, Indian Institute of Technology Roorkee and **Sri. Bharat Gupta**, Assistant Professor, Department of Electrical Engineering, Indian Institute of Technology Roorkee, Roorkee.

The matter embodied in this dissertation has not been submitted by me for the award of any other degree or diploma.
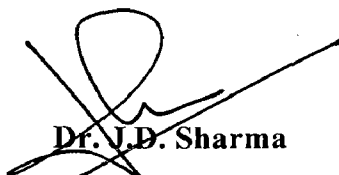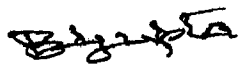
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Date: 30 June 2008

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(SHIVANI KANSAL)

CERTIFICATE

This is to certify that the above statement made by the candidate is correct to the best of our knowledge and belief.

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Acknowledgements

First of all, let me thank my thesis supervisors Dr. J.D. Sharma and Sri. Bharat Gupta for their patient and knowledgeable guidance. Their critical comments at the various stages of thesis helped me in understanding the concepts & techniques and solving the problems in an effective manner.

I am also thankful to the computing facilities provided by Electrical Engineering Department without which my thesis could not have been possible. I would also like to thank Phd. and project students of Geomatics Engineering for accompanying me in the lab work, especially Mr. R.D. Patidhar and Mr. P. Banerjee.

I am deeply grateful to my family and friends for their blessings. Finally, thanks to almighty God for giving me such a beautiful life.

(Shivani Kansal)

Abstract

Fast depleting natural reservoir and near saturation of larger hydro plants has prompted engineers to focus on other alternatives. Small hydro power is reemerging as one of the alternatives, which can be easily developed, are cost competitive and are minimally disruptive to the environment.

This thesis covers the features and evaluation of a digital signal processor/computer-based simulator of a small hydro power plant to carry out real time simulation. Real-time simulation is synchronization with the actual behavior via a real-time clock and an interface system that allows the external systems to operate just as if they were connected to the real system.

The basic mathematical models of each component of the hydraulic SHP are analyzed. With the DSP Processor, the transients of the different operating conditions of the generating unit could be calculated and simulated in real-time.

The SHP Model represents the modeling of various components of high and medium head and small hydro plant. The main components of a hydroelectric system may be classified into two groups: the hydraulic system components that include the turbine, the associated conduits- like penstock, tunnel and its control system; and secondly the electric system components formed by the synchronous generator and its control system.

Digital signal processing is concerned with the digital representation of signals and the use of digital systems to analyze, modify, store, or extract information from these signals.

DSP starter kit TMS320F2812 member of the TMS320C28x^{TM} DSP generation, is highly integrated, high-performance solutions for demanding control applications. Texas Instruments (TI) offers an extensive line of development tools for the C28x generation of DSPs, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

Contents

List of Figures

List of Acronyms

DSP	Digital Signal Processing
CCS	Code Composer Studio
RTDX	Real Time Data Exchange
ALU	Arithmetic Logic Unit
TI	Texas Instruments
MAC	Multiply Accumulate
SHP	Small Hydro Power
ADC	Analog to Digital Convertor
DAC	Digital to Analog Convertor
DMA	Direct Memory Access
CPU	Central Processing Unit
CSM	Code Security Module
McBSP	Multichannel Buffered Serial Port
SPI	Serial Peripheral Interface
SCI	Serial Communication Interface
RTW	Real Time Workshop

Chapter 1

Introduction

There are many literatures available highlighting benefits of the real time simulation using Digital Signal Processors, evolution of DSP Processors and its application in various fields. Huge literature is available regarding modeling of various components of Hydro Power Plant.

The literatures relevant to our field are summarized below:-

1.1 Literature Review

Working group on prime mover and energy supply models for system dynamic performance study [1] recommends the hydraulic model suitable for a relatively wide range of studies. The two main sections of the report provide models for (a) Prime movers including water supply conduits and (b) Prime movers speed control.

The section on prime mover model includes both linear and nonlinear controls. Nonlinear models are required where speed and power changes are large such as in islanding, load rejection and system restoration studies.

Modeling of hydro plants in which multiple units share a common conduit was examined and a model is derived by L.N. Hannet, [2] et al. the turbine/governor parameter settings and their relation to hydraulic coupling effects is also discussed. A testing procedure to obtain governor models for hydro units is presented [5] by L.N. Hannet, et al. along with steps to identify values for model parameters.

T. Bin Ng, et al. presented [3] the model of the Francis turbine for single-machine hydroelectric power plant. It describes the problems with the exciting IEEE model and proposed additional nonlinear features have been adopted to improve the accuracy of the turbine model.

A non linear model for dynamic studies of hydro-turbine is proposed by E.De.Jager, et al. [6], the model of single turbine including the water supply conduit is presented. It also describes the friction pressure loss into account and proportional to flow square, and also given the parameter estimation from field tests.

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C. K. Sanathanan [10] has demonstrated that at least a second order transfer function is necessary to model a turbine penstock. Furthermore a properly synthesized second order transfer function is usually sufficient to guarantee accuracy required for control system designing and evaluation. A procedure for synthesizing reduced order transfer function is presented. The effect of hydraulic friction can be captured accurately in the reduced order transfer function.

The influence of water column elasticity on the stability limits of a hydro-turbine generating unit with long penstock operating on an isolated load is investigated by M.S.R. Murty and M.V. Hariharan [11] in paper. D-decomposition method is used for deriving the stability regions including the elastic water column. It also has been shown that a modified water column compensator enhances the stability regions and dynamic performance considerably.

P. Kundur [7] describes the development of detailed mathematical model of synchronous machine and briefly reviews its steady state and transient performance characteristics. It defines the derived parameters of synchronous machine that are directly related to observed behavior under suitable test conditions and develops their relationships to the fundamental parameters. The simplifications required for the representation of the synchronous machine in stability studies are also discussed. It describes the characteristics and modeling of different types of synchronous generator excitation system as recommended by IEEE. In addition, it discusses dynamic performance criteria and provides definition of related terms useful in the identification and specification of excitation system requirements. It examines the characteristics of prime movers and energy supply systems and develops appropriates model suitable for their representation in power system dynamic studies. It also illustrates the nature of transient stability problems, identifies the factors influencing them and describes modeling considerations and analytical techniques applicable to transient stability analysis.

The generator model is derived starting from the basic circuit equations and the use of Park's transformation by K. R. Padiyar [8]. The models of excitation system and turbine governor system, the analysis of single machine connected to infinite bus and the study of transient stability by simulation are also presented in this book.

In the book [9] by P. M. Anderson and A. A. Fouad, a mathematical model for a synchronous machine is developed for stability studies. Two models are developed, one using the current as state variables and another using the flux linkages. Simplified model,

which are often used for stability studies are also discussed. It also covers some practical consideration in the use of the mathematical model of synchronous machines in stability studies. Among these considerations are the determination of initial conditions, determination of the parameters of the machine from available data and construction of simulation models for the machine.

A model for depicting the dynamic behaviour of reservoirs is introduced in the paper [14] by P. A. Frick. As regulation of the head is very desirable under run of river mode operation of small hydro plants, so, a simple and inexpensive modification to presently used governors is also proposed to perform the head control..

Fritz [12] provides enough background about small hydro-plant. It deals with essential components of small hydro-plants, i.e. turbines and hydraulic structures, in enough depth to promote an understanding of their functions as well as to serve as a planning and designing tool.

In the book by V.K. Madisetti and D.B. Williams [22], captures the entire range of DSP: from theory to applications - from algorithms to hardware. This book provide information on both theoretical and practical issues suitable for a broad audience—ranging from professionals in electrical engineering, computer science, and related engineering fields. It provides large number of excellent introductory texts covering areas where digital signal processing has made a significant impact include telecommunications, man-machine communications, computer engineering, multimedia applications, medical technology, radar and sonar, seismic data analysis, and remote sensing, etc.

Prototype laboratory environment, which directly links Simulink to a Texas Instrument DSP device is described and evaluated by [28] C. Gustavsson. The prototype system converts graphical models and makes available various real-time signal processing algorithms, such as adders, delays, FFTs, IIR filters and multipliers.

The paper by S.M. Kuo and W.S. Gan [32] presents modem digital signal processor architectures including multiply-accumulate unit, shifter, pipelining and parallelism, buses, data address generators, and special addressing modes and instructions.

J. Eyre and J. Bier [33] trace the evolution of DSP processors, from early architectures to current state-of-the-art devices. Some of the key differences among architectures like their strengths and weaknesses have been highlighted. It also covers the growing class of general purpose processors that have been enhanced to address the needs of DSP applications.

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The Real-Time Workshop, for use with MATLAB and Simulink, produces code directly from Simulink models and automatically builds programs that can be run in a variety of environments, including real-time systems and stand-alone simulations. The various features of RTW like:-

- A rapid and direct path from system design to implementation.
- Seamless integration with MATLAB and Simulink.
- A simple, easy to use interface.
- An open and extensible architecture.
- A fully configurable code generator— virtually every aspect of the generated code can be configured by using the Target Language Compiler™.
- Fast design iterations by editing block diagrams and automatically building a new executable.

and its usage in various applications are explained in User's Guide Version 3, RTW for use Simulink [23].

Code composer Studio User's Guide [37] contains an introduction to the basic concepts and features of Code Composer Studio. It also describes how to set breakpoints to control the execution of program and how to set Probe Points for signal analysis. This chapter describes how you can stream files into your actual or simulated target as signals. It also tells you how to load and store PC files with target memory values. Code Composer Studio incorporates an advanced signal analysis interface that enables developers to monitor signal data critically and thoroughly. User's guide also describes how you can use the graphing capabilities of Code Composer Studio to view signals on your actual/simulated target system.

1.2 Problem Statement

This thesis covers the features and evaluation of a digital signal processor/computer-based simulator of a small hydro power plant to carry out real time simulation. Real-time simulation is synchronization with the actual behavior via a real time clock and an interface system that allows the external systems to operate just as if they were connected to the real system. Modeling of various components of SHP is carried out in MATLAB/Simulink. The model of SHP is integrated with Embedded Target for TI TMS320C2000™ Plateform. Real-Time simulation of SHP is carried out in

steady state and various fault conditions like, load rejection to analyze the performance of various components of the system.

The objective of this thesis is to use digital signal processing to carry out real time simulation of small hydro power plant.

Purpose of the carrying out real-time analysis of SHP stations can be stated broadly:

a) To confirm that all parts, systems and auxiliaries in the power station are performing their assigned functions correctly.

b) To confirm that the generating units are operating efficiently.

The objective at (a) is to check the qualitative working of the power station, while that of (b) is to find out whether the power station is meeting the efficiency requirements in quantitative terms.

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Chapter 2

Modeling of Various Components of Small Hydro Power Plants

In this chapter, the modeling of various components of small hydro-plants and necessary equations representing their dynamic behavior is presented.

2.1 Penstock and Turbine Modeling [1][8]

2.1.1 Non-Linear Model (Assuming Non-Elastic Water Column)

The linear model of the hydraulic turbine is inadequate for studies involving large variations in power output and frequency. The block diagram in figure 2.1 represents the dynamic characteristics of the turbine with a penstock, which is suitable for large-signal time domain simulation [1]. The penstock is modeled assuming an incompressible fluid and a rigid conduit.
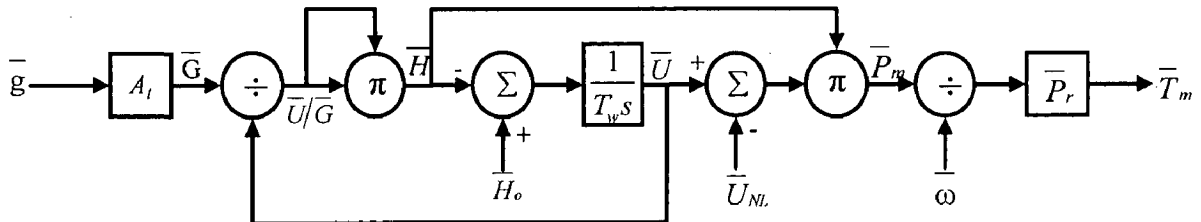

Figure 2.1: Non-Linear Model of Turbine (Non-Elastic Water Column)

Basic Hydrodynamic equations are:

$$U = K_u G \sqrt{H} \tag{2.1}$$

$$P = K_P H U \tag{2.2}$$

$$\frac{dU}{dt} = -\frac{a_g}{L}(H - H_o) \tag{2.3}$$

$$Q = AU \tag{2.4}$$

where,

U=water velocity

G=ideal gate opening

H=hydraulic head at gate

H_O=initial steady-state value of H

P=turbine Power

Q=water-flow rate

A=pipe area

L=length of conduit

a_g=acceleration due to gravity

t=time in seconds

U_{NL}=No-load water velocity

Normalizing above equations based on rated values.

$$\bar{U} = \bar{G}(\bar{H})^{1/2} \tag{2.5}$$

$$\bar{P} = \bar{U}\bar{H} \tag{2.6}$$

$$\frac{d\bar{U}}{dt} = -\frac{1}{T_W}(\bar{H} - \bar{H_O}) \tag{2.7}$$

where T_W is the water starting time at rated load. It has a fixed value for a given turbine-penstock unit and is given by:-

$$T_W = \frac{LU_r}{a_g H_r} = \frac{LQ_r}{a_g A H_r} \tag{2.8}$$

Mechanical power output P_m is given by: -

$$P_m = P - P_L \tag{2.9}$$

where, P_L represents the fixed power loss of the turbine.

Turbine mechanical torque on a base equal to generator MVA rating given by:-

$$\bar{T}_m = \left(\frac{\omega_o}{\omega}\right)\bar{P}_m\left(\frac{\bar{P}_r}{\text{MVA}_{base}}\right) = \frac{1}{\bar{\omega}}(\bar{U} - \bar{U}_{NL})\bar{H}\bar{P}_r \tag{2.10}$$

where,

$\bar{\omega}$ = per unit speed

MVA$_{base}$ = base MVA on which turbine torque is to be made per unit

$\bar{P}_r$ = per unit turbine rating

2.1.2 Non-linear Model of Penstocks and Turbines supplied from Common tunnel. (Assuming elastic water column in Penstock and tunnel). [1]

The effects of water compressibility can be introduced into a multiple penstock model in a similar manner to the single penstock representation. The model now incorporates the

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nonlinear single penstock model shown in figure 2.2. The coupling of the tunnel is included by using the same form of transfer function between the head and the flow, which, for the tunnel is the sum of the flows in the individual penstocks. The nonlinear model of hydraulic-turbine including the hydraulic interaction model is shown below. The head loss in the upper tunnel is proportional to the coefficient f_t times flow rate times absolute value of flow rate to maintain direction of head loss where the flow can reverse.

The flow at the turbine tunnel can be calculated using the continuity equation:

$$Q = \sum_{i=1}^{j} Q_i \tag{2.11}$$

The total flow in the common tunnel must be equal to the sum of the flows in the individual penstocks. The momentum equation for the water at the common tunnel is:

$$h_o - h = \frac{L}{gA}\left(\frac{dq_1}{dt} + \frac{dq_2}{dt} + \frac{dq_3}{dt}\right) \tag{2.12}$$

The momentum of water in the individual penstock is:

$$h - h_1 = \frac{L_1}{A_i g}\left(q_{io}\frac{dq_i}{dt}\right) \tag{2.13}$$
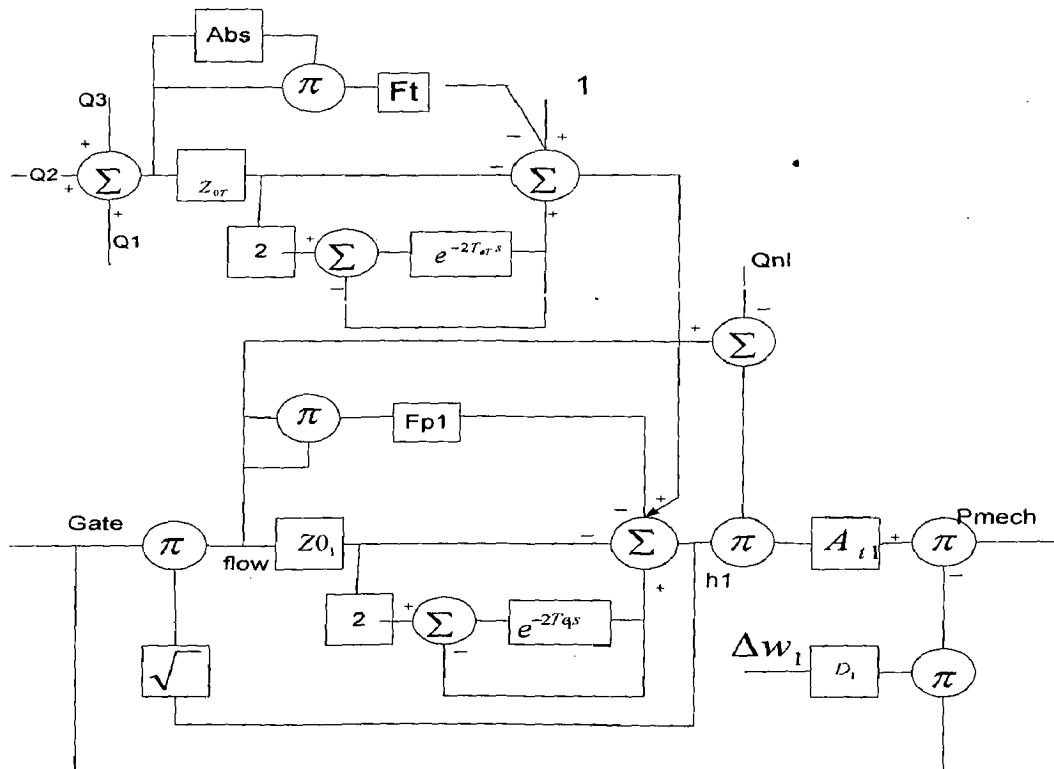
Figure 2.2: Non-linear model of multiple penstocks supplied from a common tunnel.

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Using above 2 equations to eliminate h and expressing the head in per unit form by dividing by the rated static head $h_\Box$, can be written as:

$$\begin{bmatrix} 1 - h_1 \\ 1 - h_2 \\ 1 - h_3 \end{bmatrix} = \begin{bmatrix} T_{wt} + T_{w1} & T_{wt} & T_{wt} \\ T_{wt} & T_{wt} + T_{w2} & T_{wt} \\ T_{wt} & T_{wt} & T_{wt} + T_{w3} \end{bmatrix} \begin{bmatrix} \dfrac{dQ_1}{dt} \\ \dfrac{dQ_2}{dt} \\ \dfrac{dQ_3}{dt} \end{bmatrix} \tag{2.14}$$

2.2 Governor Modeling

The basic function of a governor is to control speed and/or load. The primary speed/load control function involves feeding back speed error to the gate position.

2.2.1 Electro-Hydraulic Governor Modeling [1][7]

Modern speed governors for hydraulic turbines use electro-hydraulic systems. Functionally, their operation is very similar to that of mechanical-hydraulic governors. Speed sensing, permanent droop, temporary droop and their measuring and computing functions are performed electrically. Block diagram representing governing system for system stability studies is shown in figure 2.3.

Transfer function of the relay valve and gate servomotor is:-

$$\frac{g}{a} = \frac{K_1}{s} \tag{2.15}$$

The transfer function of the pilot valve and pilot servo is:-

$$\frac{a}{b} = \frac{K_2}{1 + sT_p} \tag{2.16}$$

Combining Equations (2.15) and (2.16):-

$$\frac{g}{b} = \frac{K_s}{s(1 + sT_P)} \tag{2.17}$$

where, K_s is servo gain and T_p is pilot valve/servomotor time constant.
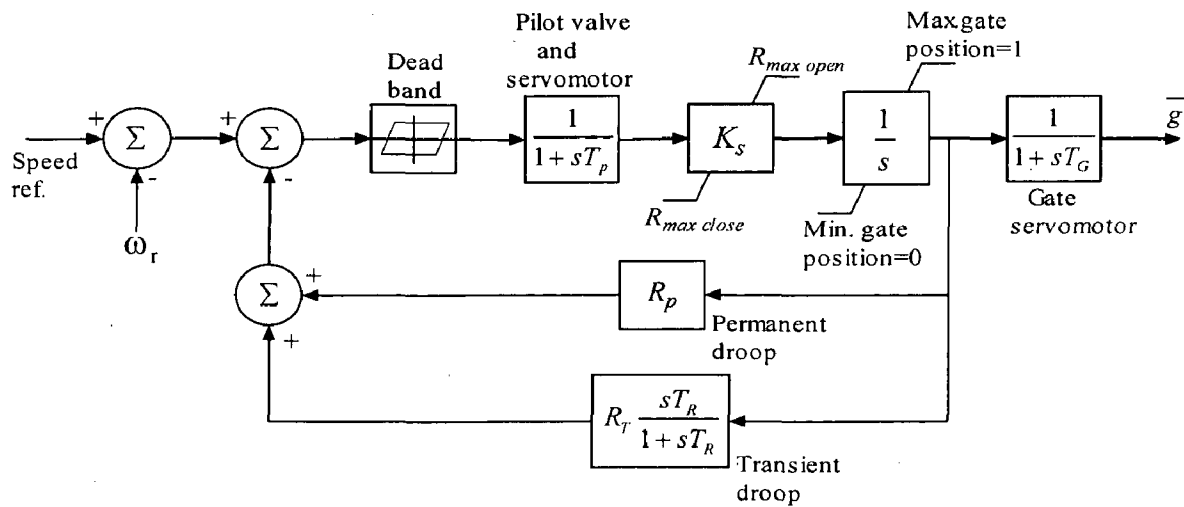
Figure 2.3: Electro-Hydraulic Governor Model

2.2.2 PID Governor Modeling [1] [7]

Some electro hydraulic governors are provided with three-term controllers with proportional-integral-derivative (PID) action. These allow the possibility of higher response speeds by providing both transient gain reduction and transient gain increase. Without derivative action, it is equivalent to hydraulic governor. The proportional and integral gains can be adjusted to obtain desired temporary droop and reset time. The derivative action is beneficial for isolated operation. Figure 2.3.2 shows the block diagram of the PID governor [1] with head controller [21].

The necessary equations representing dynamic behavior of the PID governing system are as below: -

$$V_1 = \omega_{ref} - \omega_r - R_p X_{13} + X_{16} \qquad (2.18)$$

$$\frac{dX_{11}}{dt} = V_1 K_i \qquad (2.19)$$

$$\frac{dX_{13}}{dt} = \frac{X_{12} - X_{13}}{T_a} \qquad (2.20)$$

$$V_2 = V_1 K_p + K_d \left[-\frac{d\omega_r}{dt} - R_p \frac{dX_{13}}{dt} + \frac{dX_{16}}{dt} \right] + X_{11} \qquad (2.21)$$

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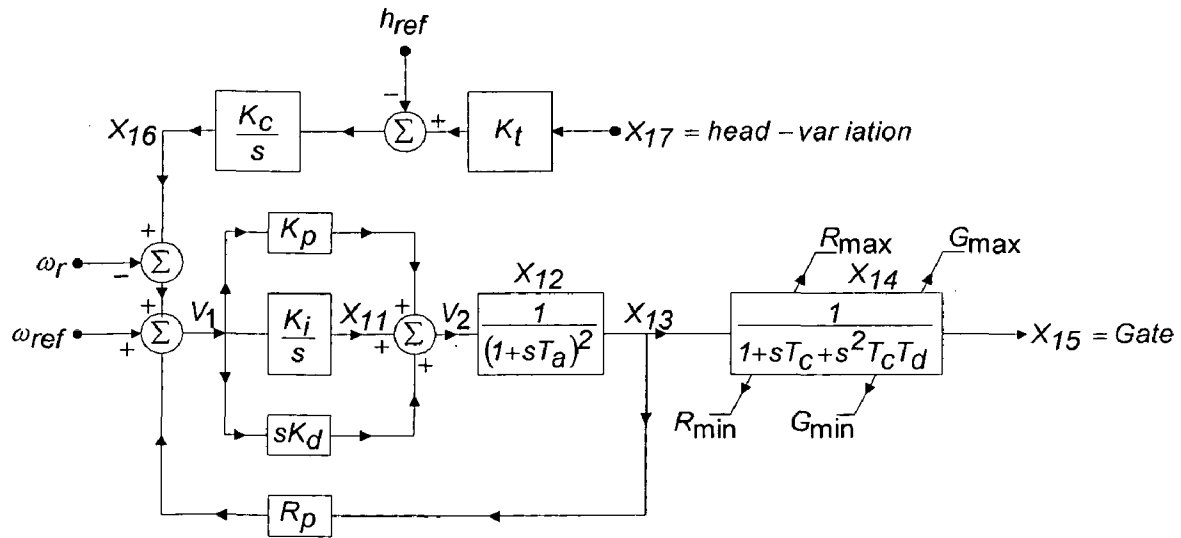
Figure 2.4: PID Governor Model

$$\frac{dX_{12}}{dt} = \frac{V_2 - X_{12}}{T_a} \tag{2.22}$$

$$\frac{dX_{16}}{dt} = K_c[K_t X_{17} - h_{ref}] \tag{2.23}$$

$$\frac{dX_{14}}{dt} = \frac{X_{13} - X_{15} - T_c X_{14}}{T_c T_d} \tag{2.24}$$

2.3 Excitation System [15] [16]

The general functional block diagram shown in Figure 2.5 indicates various synchronous machine excitation subsystems. These subsystems may include a terminal voltage transducer and load compensator, excitation control elements, an exciter, and in many instances, a power system stabilizer (PSS).

Three distinctive types of excitation systems are identified on the basis of excitation power source, as follows:

a) *Type DC excitation systems,* which utilize a direct current generator with a commutator as the source of excitation system power.

b) *Type AC excitation systems,* which use an alternator and either stationary or rotating rectifiers to produce the direct current needed for the synchronous machine field.

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c) *Type ST excitation systems*, in which excitation power is supplied through transformers or auxiliary generator windings and rectifiers.
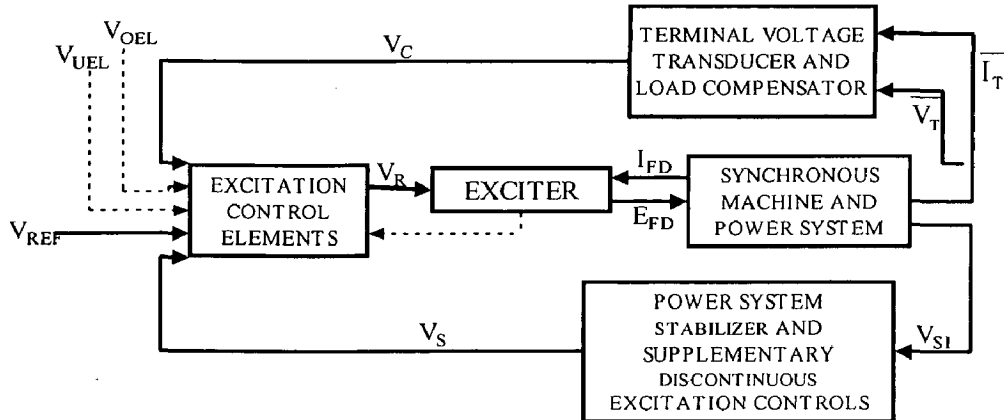
Figure 2.5: Functional Block Diagram of Synchronous Machine Excitation System

2.3.1 DC Excitation System [16]

The model, described by the block diagram of Figure 2.6, is used to represent field-controlled dc commutator exciters with continuously acting voltage regulators. The principal input to this model is the output, V_C, from the terminal voltage transducer and load compensator model previously described. At the summing junction, terminal voltage transducer output, V_C, is subtracted from the set point reference, V_{REF}. The stabilizing feedback, V_F, is subtracted and the power system stabilizing signal, V_S, is added to produce an error voltage. The major time constant, T_A, and gain, K_A, associated with the voltage regulator are shown incorporating nonwindup limits typical of saturation or amplifier power supply limitations. The voltage regulator output, V_R, is used to control the exciter, which may be either separately excited or self-excited. A signal derived from field voltage is normally used to provide excitation system stabilization, V_F, via the rate feedback with gain, K_F, and time constant, T_F.
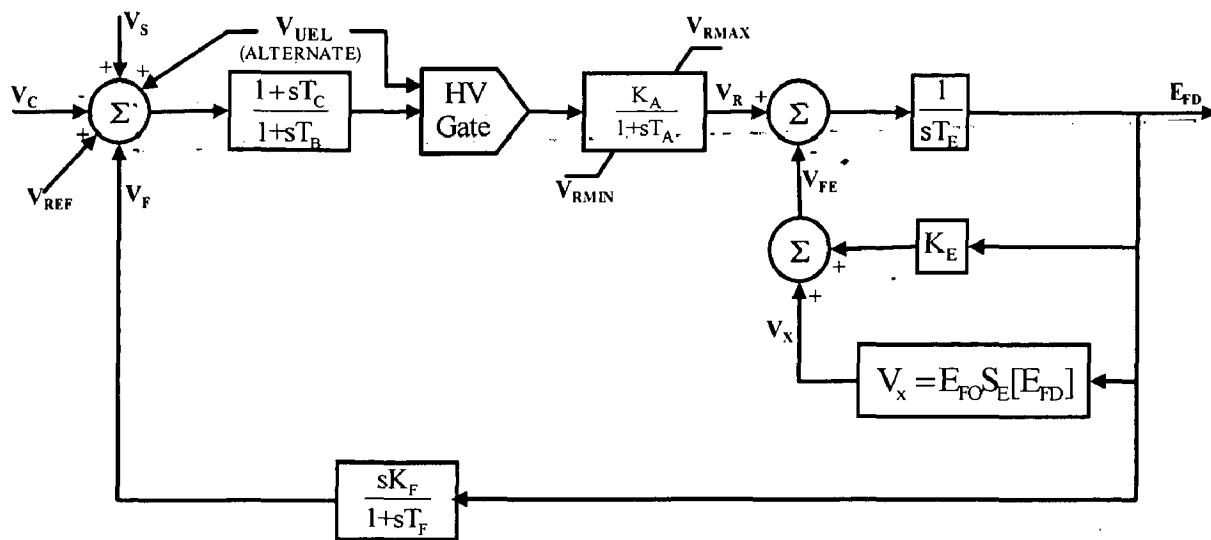
Figure 2.6: DC Excitation System

2.4 Synchronous Machine Modeling [8] [7]

Synchronous generators form the principal source of electrical energy in power systems. Power system stability problem is largely one of keeping interconnected synchronous machines in synchronism.

The magnetic circuits and all rotor windings are symmetrical with respect to both polar and inter-polar axis. Therefore, for the purpose of identifying synchronous machine characteristics, two axes are defined: -

1. The direct (d) axis, centered magnetically in the centre of the North Pole,

2. The quadrature (q) axis, 90° (electrical) ahead of the d-axis.

The position of the rotor relative to the stator is measured by the angle θ between the d-axis and the magnetic axis of the phase a winding.

The model takes into account the dynamics of the stator, field, and damper windings. In developing the equations of a synchronous machine, the following assumptions are made: -

➤ The stator windings are sinusoidally distributed along the air-gap as far as the mutual effects with the rotor are concerned,

➤ The stator slots cause no appreciable variation in the rotor inductances with rotor position,

➤ Magnetic hysteresis is negligible,

➤ Magnetic saturation effects are negligible.

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The equivalent circuit of the model is represented in the rotor reference frame that is dq-frame. All rotor parameters and electrical quantities are viewed from the stator. All rotor parameters and electrical quantities are viewed from the stator. The electrical model of the machine is shown below in figure 2.7.
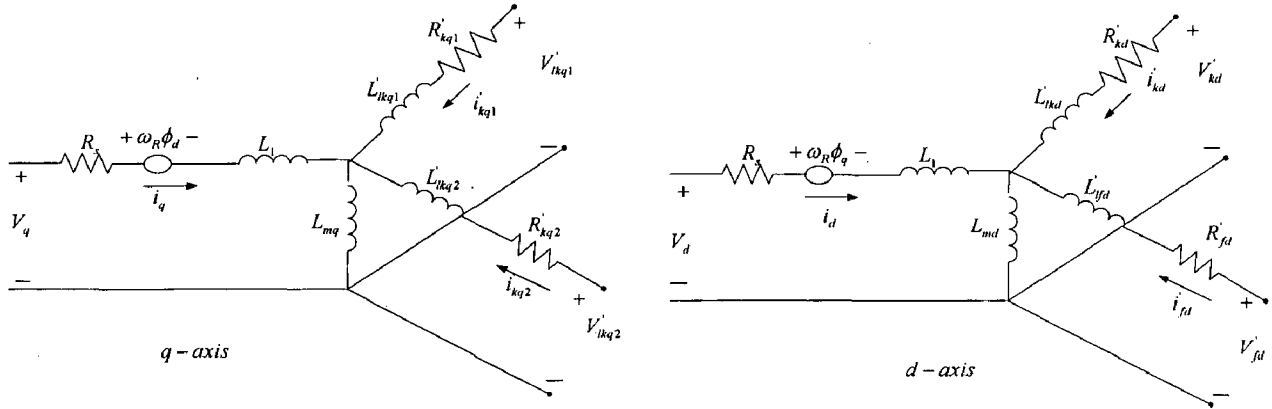
Figure 2.7: The d-q axis, Electrical Model of the Synchronous Machine

The necessary voltage and flux equation of synchronous machine are as below: -

$$V_d = R_s i_d + \frac{d}{dt}\varphi_d - \omega_R \varphi_q \qquad\qquad \varphi_d = L_d i_d + L_{md}(i'_{fd} + i'_{kd}) \qquad (2.25)$$

$$V_q = R_s i_q + \frac{d}{dt}\varphi_q + \omega_R \varphi_d \qquad\qquad \varphi_q = L_q i_q + L_{mq} i'_{kq} \qquad (2.26)$$

$$V'_{fd} = R'_{fd} i'_{fd} + \frac{d}{dt}\varphi'_{fd} \qquad\qquad \varphi'_{fd} = L'_{fd} i'_{fd} + L_{md}(i_d + i'_{kd}) \qquad (2.27)$$

$$V'_{kd} = R'_{kd} i'_{kd} + \frac{d}{dt}\varphi'_{kd} \qquad\qquad \varphi'_{kd} = L'_{kd} i'_{kd} + L_{md}(i_d + i'_{fd}) \qquad (2.28)$$

$$V'_{kq1} = R'_{kq1} i'_{kq1} + \frac{d}{dt}\varphi'_{kq1} \qquad\qquad \varphi'_{kq1} = L'_{kq1} i'_{kq1} + L_{mq} i_q \qquad (2.29)$$

$$V'_{kq2} = R'_{kq2} i'_{kq2} + \frac{d}{dt}\varphi'_{kq2} \qquad\qquad \varphi'_{kq2} = L'_{kq2} i'_{kq2} + L_{mq} i_q \qquad (2.30)$$

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Chapter 3
Digital Signal Processing

3.1 Introduction [22]

Digital signal processing (DSP) is concerned with the digital representation of signals and the use of digital systems to analyze, modify, store, or extract information from these signals. Much research has been conducted to develop DSP algorithms and systems for real-world applications. In recent years, the rapid advancement in digital technologies has supported the implementation of sophisticated DSP algorithms for real-time applications. DSP is now used not only in areas where analog methods were used previously, but also in areas where applying analog techniques is very difficult or impossible.

DSP is the mathematics, the algorithms, and the techniques used to manipulate signals after they have been converted into a digital form. This includes a wide variety of goals, such as: enhancement of visual images, recognition and generation of speech, compression of data for storage and transmission.

DSP systems are required to perform intensive arithmetic operations such as multiplication and addition. These tasks may be implemented on microprocessors, microcontrollers, digital signal processors, or custom integrated circuits. The selection of appropriate hardware is determined by the applications, cost, or a combination of both.

There are two types of DSP applications: non-real-time and real-time. Non-real-time signal processing involves manipulating signals that have already been collected in digital forms. This may or may not represent a current action, and the requirement for the processing result is not a function of real time. Real-time signal processing places stringent demands on DSP hardware and software designs to complete predefined tasks within a certain time frame.

3.2 DSP Processors

Programmable DSP Processors are a class of microprocessors optimized for DSP and are popular solution for several reasons: They can potentially be programmed in the

field, allowing product upgrades or fixes. In comparison to other type of microprocessors, DSP processors have an advantage in terms of speed, cost, and energy efficiency.

In 1979, [33] Intel introduced the 2920, a 25-bit integer processor with a 400 ns instruction cycle and a 25-bit arithmetic-logic unit (ALU) for DSP applications. In 1982, Texas Instruments introduced the TMS32010, a 16-bit fixed-point processor with a 16 × 16 hardware multiplier and a 32-bit ALU and accumulator. This first commercially successful DSP processor was followed by the development of faster products and floating-point processors. The performance and price range among DSP processors vary widely. Today, dozens of DSP processor families are commercially available. In the low-end and low-cost group are Texas Instruments' TMS320C2000 (C24x and C28x) family, Analog Devices' ADSP-218x family, and Freescale's DSP568xx family. These conventional DSP processors include hardware multiplier and shifters, execute one instruction per clock cycle, and use the complex instructions that perform multiple operations such as multiply, accumulate, and update address pointers. They provide good performance with modest power consumption and memory usage, thus are widely used in automotives, appliances, hard disk drives, modems, and consumer electronics. For example, the TMS320C2000 and DSP568xx families are optimized for control applications, such as motor and automobile control, by integrating many microcontroller features and peripherals on the chip.

The midrange processor group includes Texas Instruments' TMS320C5000 (C54x and C55x), Analog Devices' ADSP219x and ADSP-BF5xx, and Freescale's DSP563xx. These enhanced processors achieve higher performance through a combination of increased clock rates and more advanced architectures. These families often include deeper pipelines, instruction cache, complex instruction words, multiple data buses (to access several data words per clock cycle), additional hardware accelerators, and parallel execution units to allow more operations to be executed in parallel. For example, the TMS320C55x has two multiply–accumulate (MAC) units. These midrange processors provide better performance with lower power consumption, thus are typically used in portable applications such as cellular phones and wireless devices, digital cameras, audio and video players, and digital hearing aids. These conventional and enhanced DSP processors have the following features for common DSP algorithms such as filtering:

❖ *Fast MAC units [26]* – The multiply–add or multiply–accumulate operation is required in most DSP functions including filtering, fast Fourier transform, and

correlation. To perform the MAC operation efficiently, DSP processors integrate the multiplier and accumulator into the same data path to complete the MAC operation in single instruction cycle.

❖ *Multiple memory accesses* – Most DSP processors adopted modified Harvard architectures that keep the program memory and data memory separate to allow simultaneous fetching of instruction and data. In order to support simultaneous access of multiple data words, the DSP processors provide multiple on-chip buses, independent memory banks, and on-chip dual-access data memory.
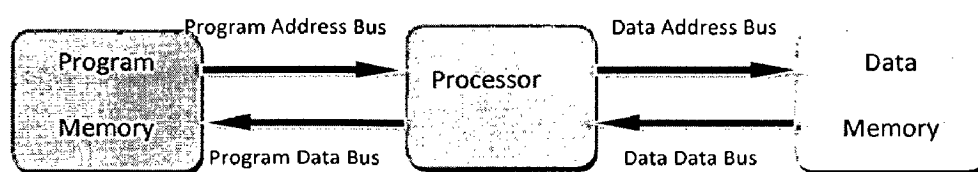
a) Harvard Architecture
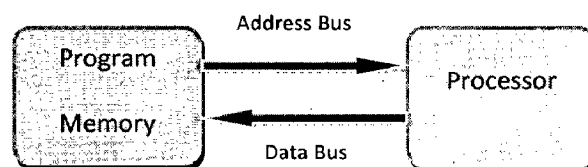
b) von Newmann Architecture

Fig 3.1: Different Memory Architectures: a) Harvard Architecture; b) von Newmann Architecture

❖ *Special addressing modes* – DSP processors often incorporate dedicated data address generation units for generating data addresses in parallel with the execution of instruction. These units usually support circular addressing and bit-reversed addressing for some specific algorithms.

❖ *Special program control* – Most DSP processors provide zero-overhead looping, which allows the programmer to implement a loop without extra clock cycles for updating and testing loop counters, or branching back to the top of loop.

❖ *Optimize instruction set* – DSP processors provide special instructions that support the computational intensive DSP algorithms. For example, the TMS320C5000 processors support compare-select instructions for fast Viterbi decoding.

❖ *Effective peripheral interface* – DSP processors usually incorporate high-performance serial and parallel input/output (I/O) interfaces to other devices such as ADC and DAC. They provide streamlined I/O handling mechanisms such as buffered serial ports, direct memory access (DMA) controllers, and low-overhead interrupt to transfer data with little or no intervention from the processor's computational units.

3.3 TMS320C28x DSP Platform [31]

The TMS320F2810, TMS320F2811, TMS320F2812, TMS320C2810, TMS320C2811, and TMS320C2812 devices, members of the TMS320C28x DSP generation, are highly integrated, high-performance solutions for demanding control applications.

3.3.1 C28x CPU Description

The C28x DSP generation is the newest member of the TMS320C200□DSP platform. The C28x is as efficient in DSP math tasks as it is in system control tasks that typically are handled by microcontroller devices. This efficiency removes the need for a second processor in many systems. The 32 x 32-bit MAC capabilities of the C28x and its 64-bit processing capabilities, enable the C28x to efficiently handle higher numerical resolution problems. The C28x has an 8-level-deep protected pipeline with pipelined memory accesses. This pipelining enables the C28x to execute at high speeds without resorting to expensive high-speed memories.

3.3.2 Memory Bus (Harvard Bus Architecture)

The C28x memory bus architecture contains a program read bus, data read bus and data write bus. The program read bus consists of 22 address lines and 32 data lines. The data read and write busses consist of 32 address lines and 32 data lines each. The 32-bit-wide data busses enable single cycle 32-bit operations. The multiple bus architecture, commonly termed "Harvard Bus", enables the C28x to fetch an instruction, read a data value and write a data value in a single cycle.

The priority of Memory Bus accesses can be summarized as follows:

Highest: Data Writes

                     Program Writes

                     Data Reads

                     Program Reads

Lowest: Fetches

3.3.3   Real-Time JTAG and Analysis

The F281x and C281x implement the standard IEEE 1149.1 JTAG interface. Additionally, the F281x and C281x support real-time mode of operation whereby the contents of memory, peripheral and register locations can be modified while the processor is running and executing code and servicing interrupts. The F281x and C281x implement the real-time mode in hardware within the CPU.

3.3.4   Flash (F281x Only)

The F2812 and F2811 contain 128K x 16 of embedded Flash memory and 1K x 16 of OTP memory. The Flash memory is segregated into four 8K x 16 sized sectors, and six 16K x 16 sized sectors. The user can individually erase, program and validate a sector while leaving other sectors untouched. However, it is not possible to use one sector of the Flash (or the OTP) to execute flash algorithms that erase/program other sectors. Special memory pipelining is provided to enable the Flash module to achieve higher performance. The Flash/OTP is mapped to both program and data space hence can be used to execute code or store data information.

3.3.5   Boot ROM

The Boot ROM is factory-programmed with boot-loading software. Boot-mode signals are provided to tell the bootloader software what boot mode to use on power up. The user can select to boot normally or to download new software from an external connection or to select boot software that is programmed in the internal Flash.

3.3.6 Security

Code security module (CSM) is used to protect the Flash/ROM/OTP and the L0/L1 SARAM blocks. The security feature prevents unauthorized users from examining the memory contents via the JTAG port.

3.3.7 Oscillator and PLL

The F281x and C281x can be clocked by an external oscillator or by a crystal attached to the on-chip oscillator circuit. A PLL is provided supporting up to 10-input clock-scaling ratios. The PLL ratios can be changed on-the-fly in software, enabling the user to scale back on operating frequency if lower power operation is desired.

3.3.8 Control Peripherals

The F281x and C281x support the following peripherals which are used for embedded control and communication:

EV: The event manager module includes general-purpose timers, full-compare/PWM units, capture inputs (CAP) and quadrature-encoder pulse (QEP) circuits. Two such event managers are provided which enable two three-phase motors to be driven or four two-phase motors.

ADC: The ADC block is a 12-bit converter, single ended, 16-channels. It contains two sample-and-hold units for simultaneous sampling.

3.3.9 Serial Port Peripherals

The F281x and C281x support the following serial communication peripherals:-

McBSP: This is the multichannel buffered serial port that is used to connect to phone-quality codecs for modem applications or high-quality stereo-quality Audio DAC devices. The McBSP receive and transmit registers are supported by a 16-level FIFO. This significantly reduces the overhead for servicing this peripheral.

SPI: The SPI is a high-speed, synchronous serial I/O port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmable bit-transfer rate. Normally, the SPI is used for communications between

the DSP controller and external peripherals or another processor. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. On the F281x and C281x, the port supports a 16-level, receive and transmit FIFO for reducing servicing overhead.

SCI: The serial communications interface is a two-wire asynchronous serial port, commonly known as UART. On the F281x and C281x, the port supports a 16-level, receive and transmit FIFO for reducing servicing overhead.

3.4 The eZdsp™ F2812 Board [30]

The eZdsp™ F2812 is a 5.25 x 3.0 inch, multi-layered printed circuit board, powered by an external 5-Volt only power supply. Figure 3.2 shows the layout of both the socketed and unsocketed version of the F2812 eZdsp.
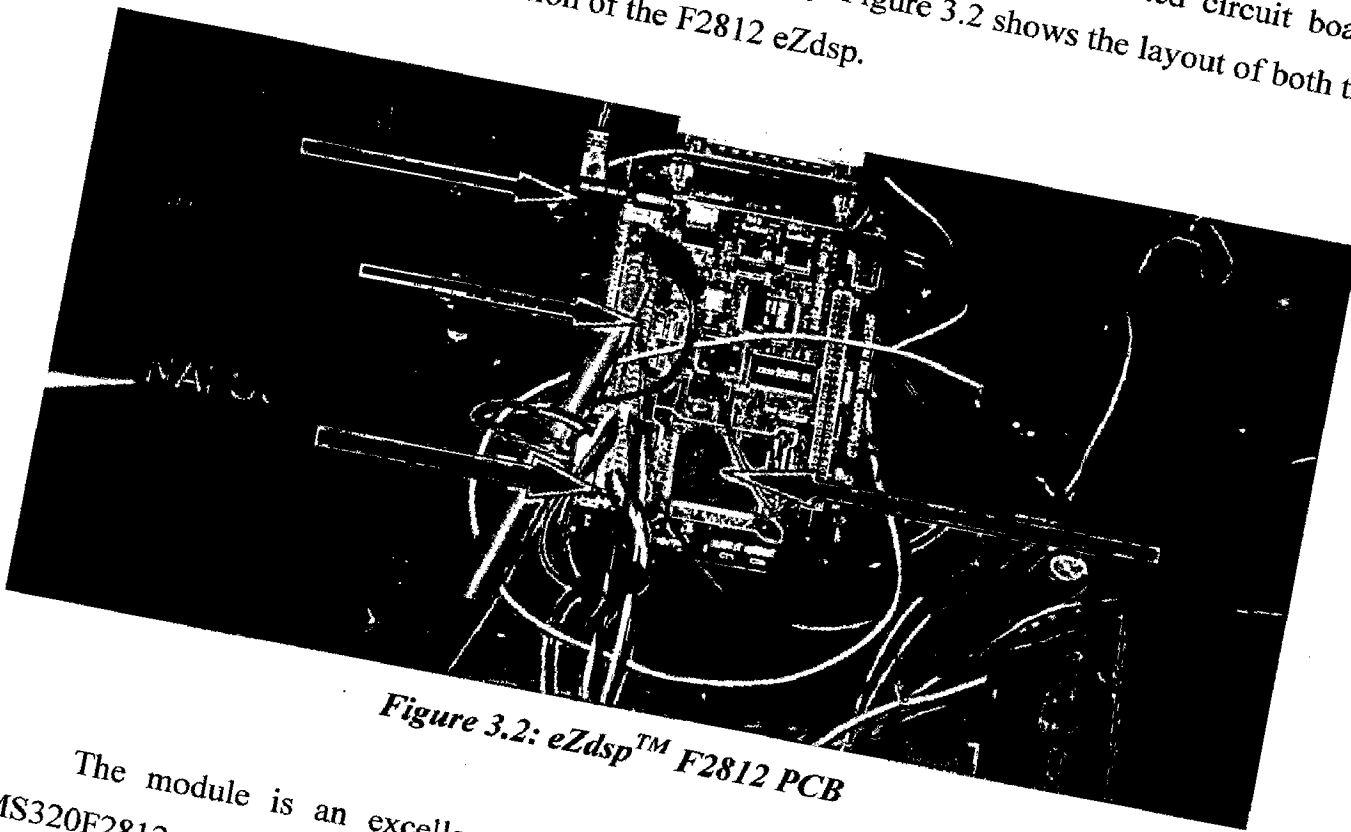

Figure 3.2: eZdsp™ F2812 PCB

The module is an excellent platform to develop and run software for the TMS320F2812 processor. The eZdsp™ F2812 allows full speed verification of F2812 code. To simplify code development and shorten debugging time, a C2000 Tools Code Composer driver is provided. In addition, an onboard JTAG connector provides interface to emulators, operating with other debuggers to provide assembly language and 'C' high level language debug.

The eZdsp™ F2812 consists of four major blocks of logic:

> Analog Interface Connector
> I/O Interface Connector
> JTAG Interface
> Parallel Port JTAG Controller Interface

3.4.1 Key Features of the eZdsp™ F2812

The eZdsp™ F2812 has the following features:

> TMS320F2812 Digital Signal Processor
> 150 MIPS operating speed
> 18K words on-chip RAM
> 128K words on-chip Flash memory
> 64K words off-chip SRAM memory
> 30 MHz. clock
> 2 Expansion Connectors (analog, I/O)
> Onboard IEEE 1149.1 JTAG Controller
> 5-volt only operation with supplied AC adapter
> TI F28xx Code Composer Studio tools driver
> On board IEEE 1149.1 JTAG emulation connector

3.4.2 Power Connector

The eZdsp™ F2812 is powered by a 5-Volt only power supply, included with the unit. The unit requires 500mA. The power is supplied via connector P6.

3.4.3 eZdsp™ F2812 Memory

The eZdsp includes the following on-chip memory:

> 128K x 16 Flash
> 2 blocks of 4K x 16 single access RAM (SARAM)
> 1 block of 8K x 16 SARAM
> 2 blocks of 1K x 16 SARAM

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In addition 64K x 16 off-chip SRAM is provided. The processor on the eZdsp can be configured for boot-loader mode or non-boot-loader mode.

3.4.4   eZdsp™ F2812 Connectors

The eZdsp™ F2812 has five connectors. Pin 1 of each connector is identified by a square solder pad. Figure 3.2 show position of various connectors of eZdsp™ F2812. The function of each connector is shown in the table below:

Table 1: eZdsp™ F2812 Connectors

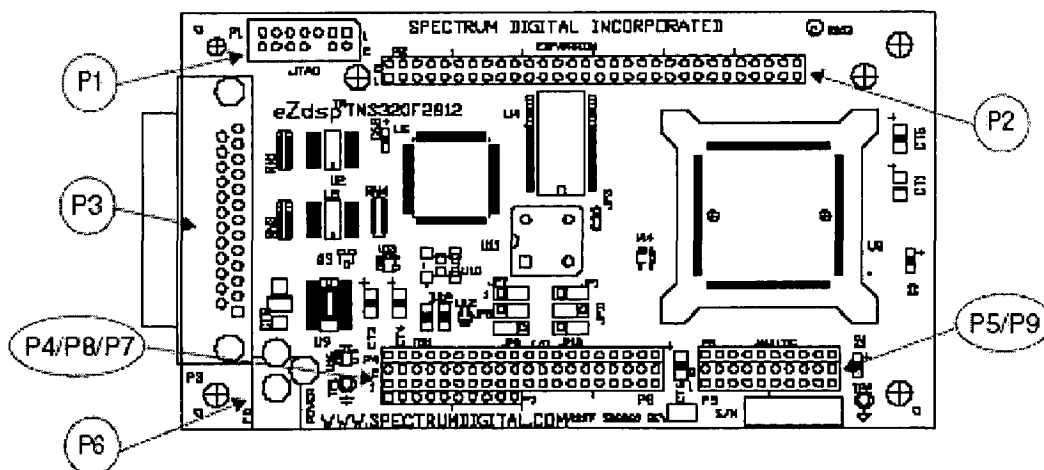| Connector	Function
P1	JTAG Interface
P2	Expansion
P3	Parallel Port/JTAG Controller Interface
P4/P8/P7	I/O Interface
P5/P9	Analog Interface
P6	Power Connector

Figure 3.3: eZdsp™ F2812 Connector Positions

Chapter 4

Matlab Interface for DSP Applications

4.1 Matlab/Simulink [17]

MATLAB is a high-level language and interactive environment that enables to perform computationally intensive tasks faster than with traditional programming languages such as C, C++, and Fortran. MATLAB provides a number of features for documenting and sharing work by integrating MATLAB code with other languages and applications, and by distributing MATLAB algorithms and applications.

Simulink is an environment for multidomain simulation and Model-Based Design for dynamic and embedded systems. It provides an interactive graphical environment and a customizable set of block libraries that let you design, simulate, implement, and test a variety of time-varying systems, including communications, controls, signal processing, video processing, and image processing, power systems.

Simulink is integrated with MATLAB, providing immediate access to an extensive range of tools that help to develop algorithms, analyze and visualize simulations, customize the modeling environment, and define signal, parameter, and test data.

4.2 SimPowerSystems [17][18]

SimPowerSystems is a modern design tool that allows scientists and engineers to rapidly and easily build models that simulate power systems. SimPowerSystems uses the Simulink environment, allowing building a model using simple click and drag procedures. Not only one can draw the circuit topology rapidly, but analysis of the circuit can include its interactions with mechanical, thermal, control, and other disciplines. This is possible because all the electrical parts of the simulation interact with the extensive Simulink modeling library. Since Simulink uses MATLAB as its computational engine, designers can also use MATLAB toolboxes and Simulink blocksets.

One can rapidly put SimPowerSystems to work. The libraries contain models of typical power equipment such as transformers, lines, machines, and power electronics.
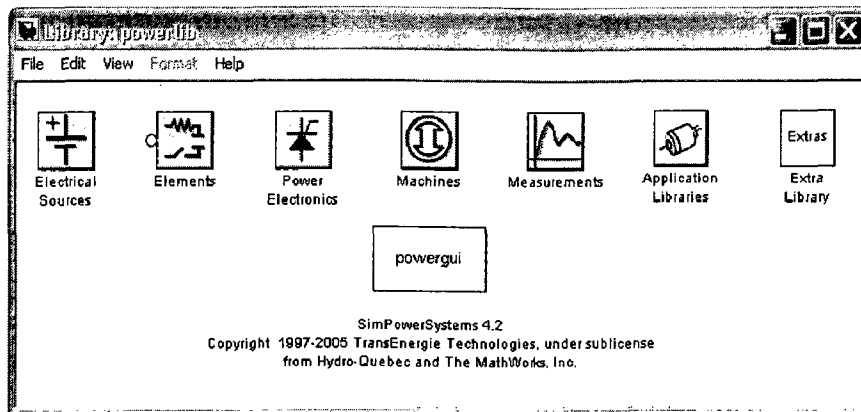
Figure 4.1: Powerlib Library Containing Models of Various Power Equipments

4.3 Embedded Target for the TI TMS320C2000 DSP Platform [24]

The Embedded Target for the TI TMS320C2000™ DSP Platform integrates Simulink and MATLAB with Texas Instruments expressDSP™ tools. Product can be used to develop and validate digital signal processing and control designs from concept through code.

The Embedded Target for the TI TMS320C2000 DSP Platform uses C code generated by Real-Time Workshop and TI development tools to generate a C language real-time implementation of Simulink model. Real-Time Workshop builds a Code Composer Studio project from the C code.

Generated code can be compiled, linked, downloaded on an LF2407, F2808, or F2812 eZdsp™ DSP board. Figure 4.2 below shows C2000lib library Integrating Matlab/Simulink with TI DSP™ Tools.
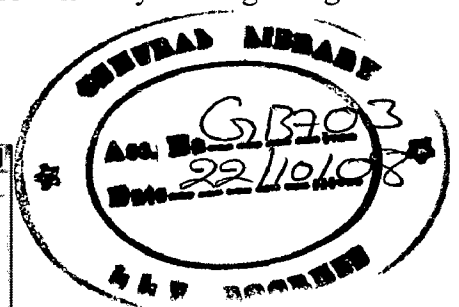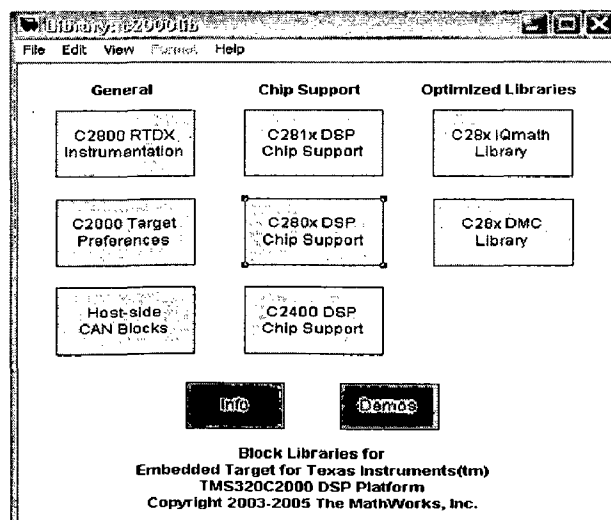

Figure 4.2: C2000lib Integrating Matlab/Simulink with TI DSP™ Tools.

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4.4 Real-Time Workshop [23]

Real-Time Workshop is an extension of capabilities of Simulink and MATLAB that automatically generates, packages, and compiles source code from Simulink models to create real-time software applications on a variety of systems. By providing a code generation environment for rapid prototyping and deployment, Real-Time Workshop is the foundation for production code generation capabilities. Along with other tools and components from the MathWorks, Real-Time Workshop provides:-

❖ Automatic code generation tailored for a variety of target platforms.

❖ A rapid and direct path from system design to implementation.

❖ Seamless integration with MATLAB and Simulink.

❖ A simple graphical user interface.

❖ An open architecture and extensible make process.

The process of generating source code from Simulink models using Real-Time Workshop is shown in the following diagram.
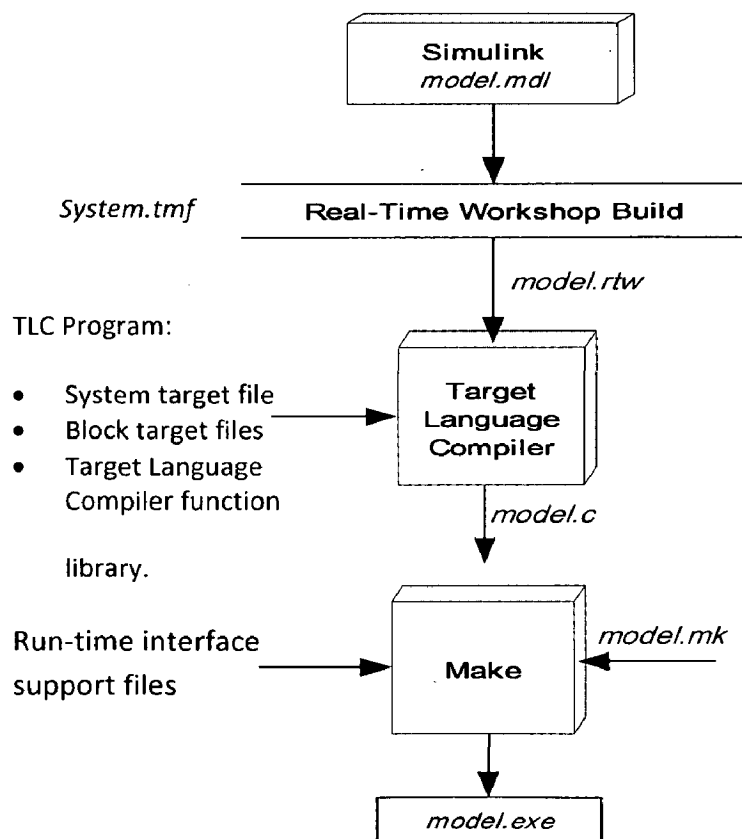

Figure 4.3: Real-Time Workshop's Open Architecture

4.5 RTDX

In all cases, developers create algorithms that they need to accomplish the desired result. Once they have the algorithms, developers use models and DSP processor development tools to test their algorithms, to determine whether the processing achieves the goal, and whether the processing works on the proposed platform. The Link for Code Composer Studio and the links for RTDX and CCS IDE ease the job of taking algorithms from the model realm to the real world of the target digital signal processor on which the algorithm will run.

RTDX and links for CCS IDE provide a communications pathway to manipulate data and processing programs on your target digital signal processor. RTDX offers real-time data exchange in two directions between MATLAB and your target process. Data you send to the target has little effect on the running process and plotting the data you retrieve from the target lets you see how your algorithms are performing in real time.

4.6 Link for Code Composer Studio [17]

Link for Code Composer Studio Development Tools lets you use MATLAB functions to communicate with Code Composer Studio™ and with information stored in memory and registers on a target. With the links you can transfer information to and from Code Composer Studio and with the embedded objects you get information about data and functions stored in your signal processor memory and registers, as well as information about functions in your project.

4.7 Code Composer Studio (CCStudio) [37]

Code Composer Studio (CCStudio) software is a fully integrated development environment (IDE) supporting Texas Instruments industry-leading DSP platforms. Code Composer Studio is one of the key components of eXpressDSP Software and Development Tools that slashes development and integration time for DSP software. Code Composer Studio IDE is the first intelligent development environment to offer TMS320C2000, TMS320C5000 and TMS320C6000 application development for multi-processor, multi-user and multi-site projects. Code Composer Studio integrates all host and target tools in a unified environment to simplify DSP system configuration and

application design. This is easy to use development environment that allows DSP designers of all experience levels full access to all phases of the code development process. Tools and interfaces allow users to get started faster than ever before and add functionality to their application.

CCStudio must be configured correctly to pick up correct simulator configuration. In CCStudio setup import configuration from the available drivers or select custom configuration according to target configuration. Figure 4.4 shows screen shot of CCStudio setup after importing the configuration.
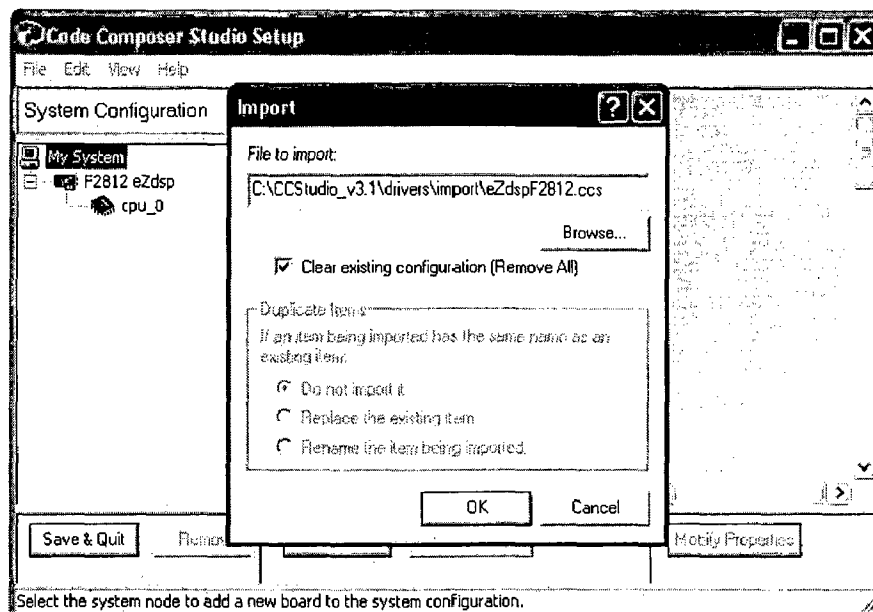

Figure 4.4: CCStudio setup Import Configuration

The CCStudio integration provides basic supports for debugging, namely,

❖ Read and Write to IO registers and DSP memory including program load.

❖ Execution Control : Run, Step, Halt, Reset

❖ Set and Clear Breakpoints: CCStudio shows only those breakpoints which are set from CCStudio. Breakpoints can also be set, cleared and seen from Virtio command window.

❖ CCStudio can be connected and disconnected multiple times. Connect and disconnect happen automatically when CCStudio is brought up and exited respectively.

Chapter 5

Simulation and Implementation Results

This chapter describes the experimental setup, simulation and results of simulation of small hydro power plant under different operating conditions. The system is modeled and simulated using MATLAB SIMULINK and Embedded Target for the TI TMS320C2000 DSP Platform. The simulated system is then targeted to the eZdsp^{TM} F2812 board for hardware implementation. The designed system is used for analyzing the working of SHP on real time using RTDX.

5.1 System Model for Simulation

Modeling of various components of small hydro power plant is described in chapter 2 according IEEE standards. Simulation of SHP is carried out in two cases mentioned below:
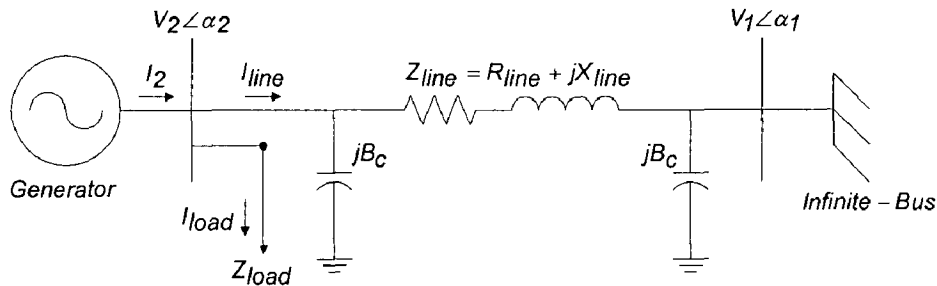
Case 1:-

Figure 5.1: Generator connected to Infinite Bus.

In the above diagram, Generator is having local load at its terminal, is connected to infinite bus through a transmission line is shown in figure 5.1. The load power is 50 MW, 25 MVAR is connected to generator terminal. In this case the load is decreased and simulated at generator terminal at 8 seconds. Simulation results of various parameters like real power generated, rotor speed, rotor angle, etc. are shown below.
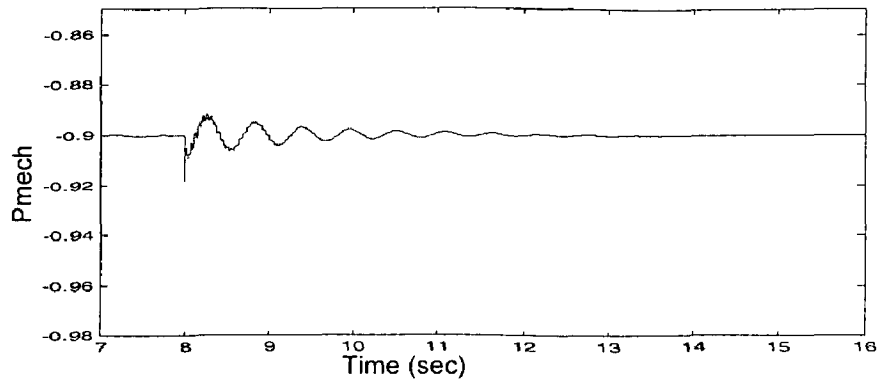
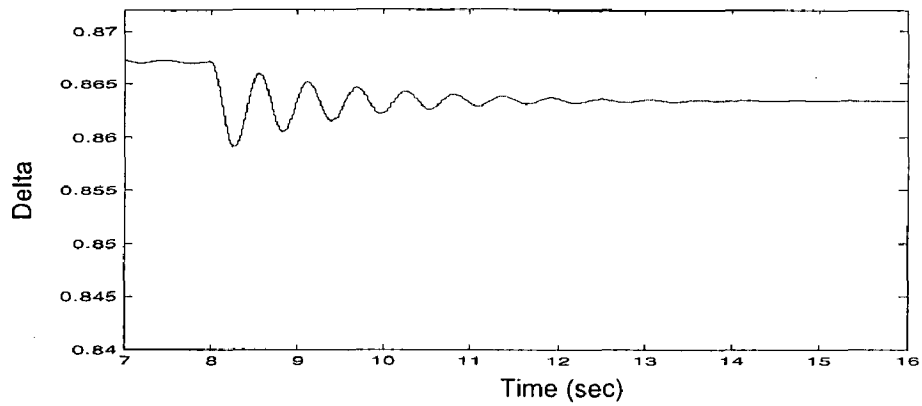**Figure 5.2: Mechanical Power Vs Time Characteristics**

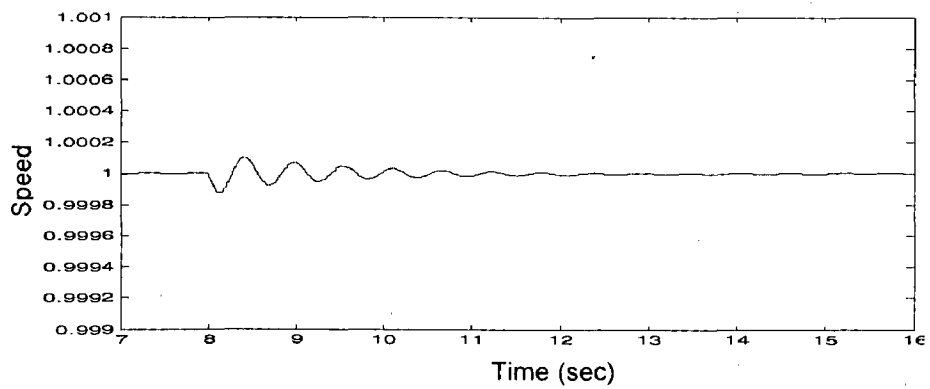**Figure 5.3: Rotor angle deviation Vs Time Characteristics**

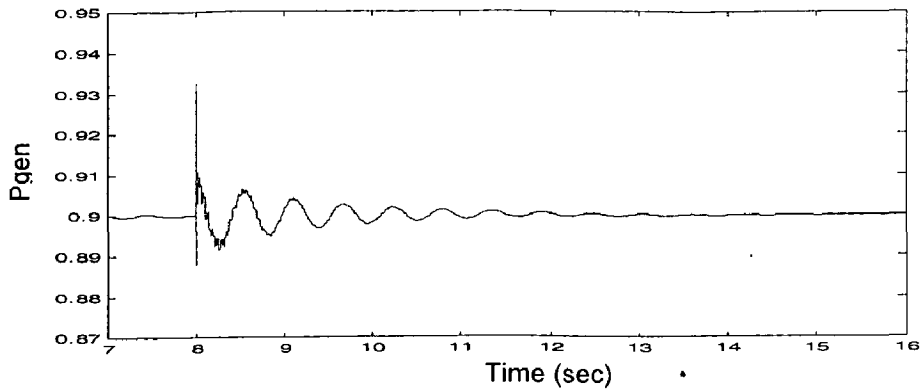**Figure 5.4: Speed Vs Time Characteristics**

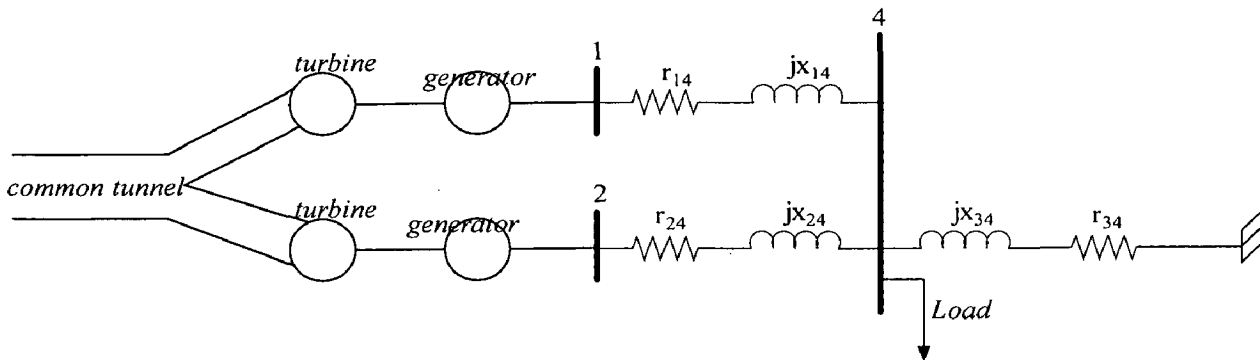*Figure 5.5: Real Power Generated Vs Time Characteristics*

Case 2:-

Figure 5.6: Common Tunnel for three Turbines and Generators connected to Infinite Bus.

In this case, a common penstock is used for two turbines, and each generator is having load at its terminal, and they are connected to infinite bus through a transmission line is as shown in figure 5.6. Infinite bus is treated as a swing bus and a load of 50MW, 25 MVAR is connected at each generator. In this case, 3-phase symmetrical fault is simulated at first generator terminal at 3 seconds and is cleared after 0.2 seconds. The simulation results are shown below.
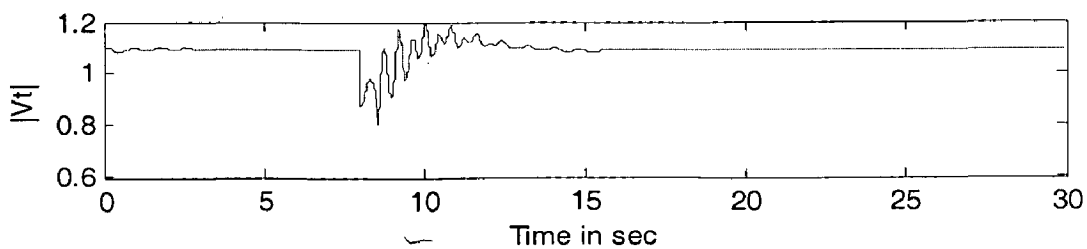
Figure 5.7: Terminal Voltage Vs Time Characteristic of Generator 1

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Figure 5.8: Real Power generated Vs Time Characteristic of Generator 1

Figure 5.9: reactive Power generated Vs Time Characteristic of Generator 1

Figure 5.10: Rotor angle Vs Time Characteristic of Generator 1

Figure 5.11: Mechanical Torque Vs Time Characteristic of Generator 1

Figure 5.12: Terminal Voltage Vs Time Characteristic of Generator 2

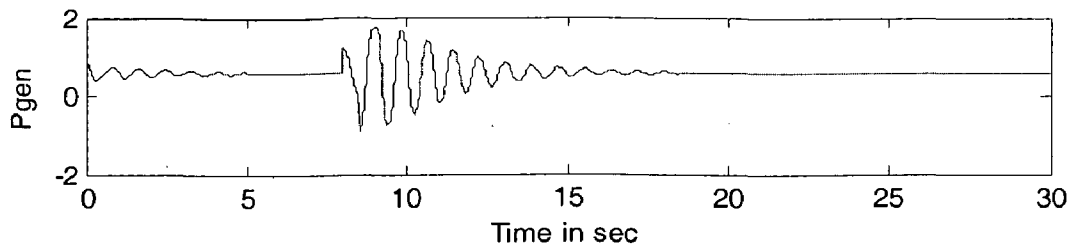Indian Institute of Technology Roorkee

Figure 5.13: Real Power Generated Vs Time Characteristic of Generator 2

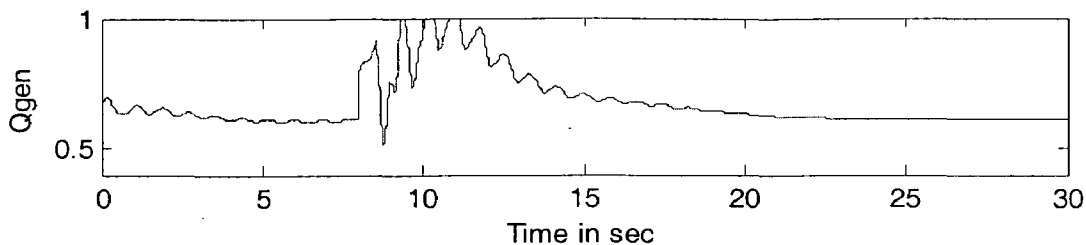**Figure 5.14: Reactive Power generated Vs Time Characteristic of Generator 2**
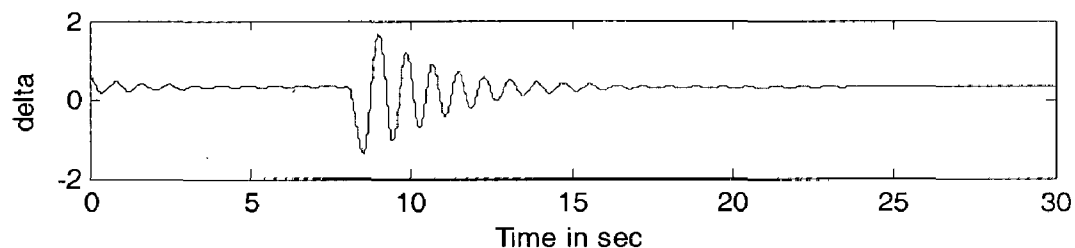

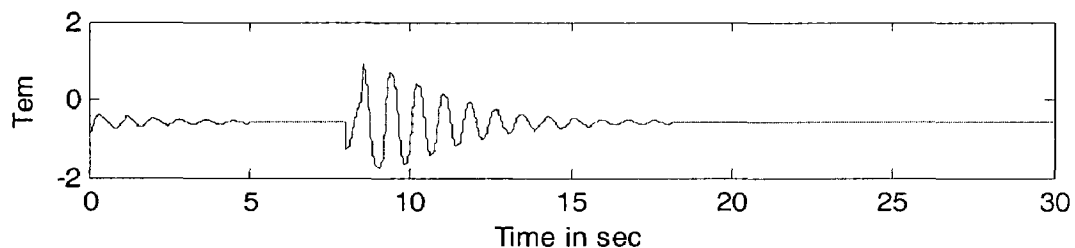**Figure 5.15: Rotor Angle Vs Time Characteristic of Generator 2**

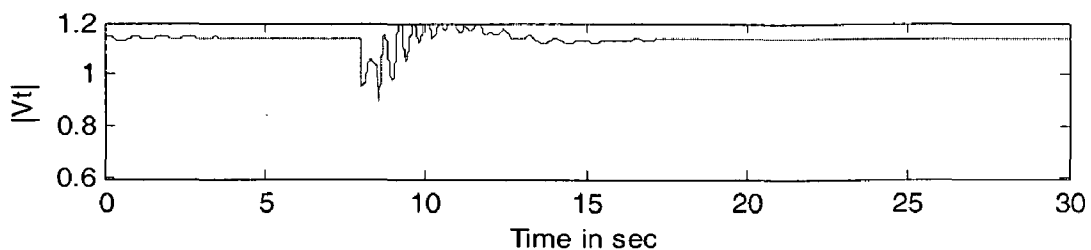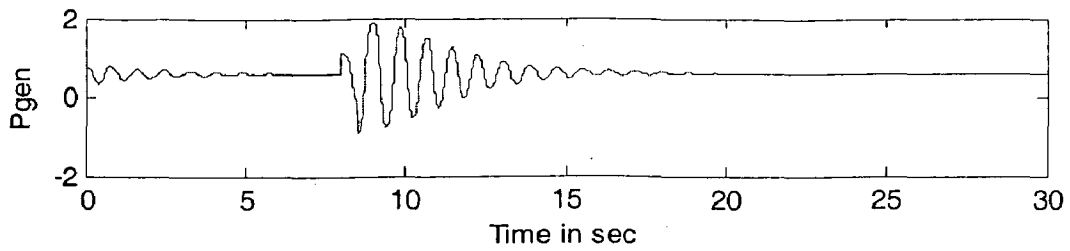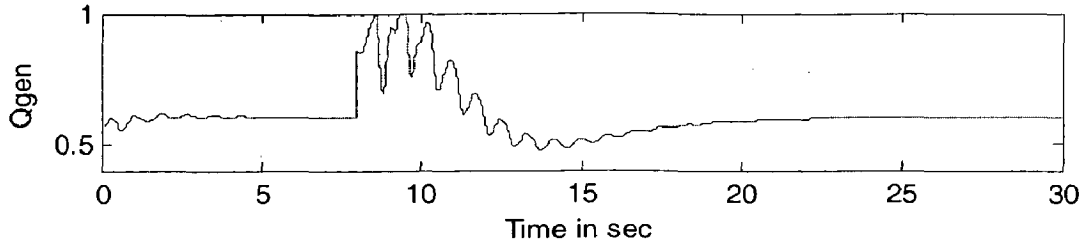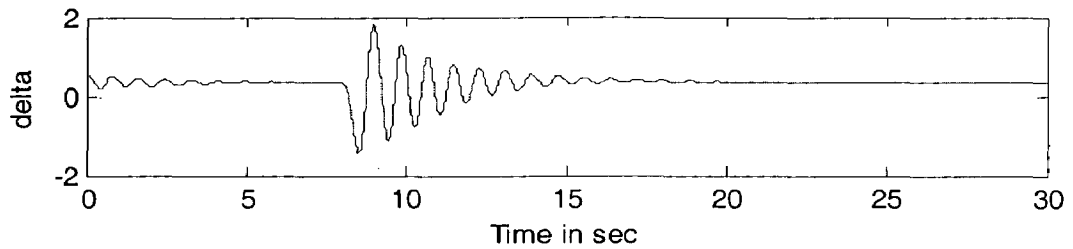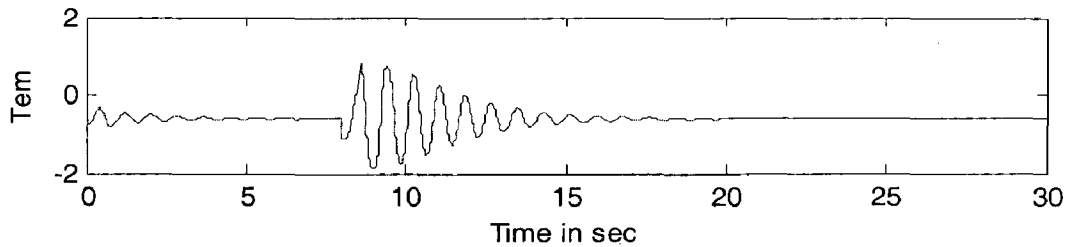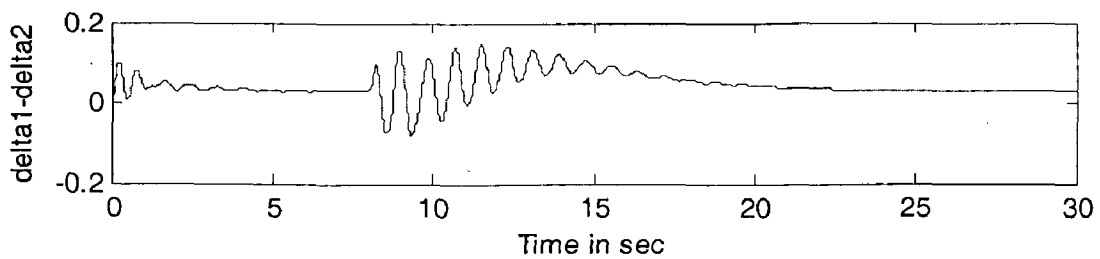**Figure 5.16: Mechanical Torque Vs Time Characteristic of Generator 2**

Figure 5.17: Rotor Angle Difference between two generators Vs Time Characteristic

5.2 DSP Implementation

After simulation and analysis of the results, the system is implemented on a TI eZdsp™ F2812 board. The eZdsp hardware board, which has a TMS320F2812 DSP chip on it, is used to implement the system in hardware. The eZdsp™ F2812 is programmed using a custom parallel port-JTAG interface device. This device incorporates a standard parallel port interface that support bidirectional communication with host computer.

The eZdsp includes the following on-chip memory: 128K x 16 Flash, 2 blocks of 4K x 16 single access RAM (SARAM), 1 block of 8K x 16 SARAM, 2 blocks of 1K x 16 SARAM, in addition 64K x 16 off-chip SRAM is provided. The eZdsp RAM can be loaded for debuging or FLASH ROM can be loaded and run. With careful attention to the I/O mapping in the software, the application code can be easily ported to the F2812.

Real Time Workshop creates c-code of SIMULINK simulation. Code Composer Studio and Embedded Target for the TI TMS320C2000 DSP Platform are used for the initial design of the DSP program. The Embedded Target for the TI TMS320C2000™ DSP Platform integrates Simulink and MATLAB with Texas Instruments eXpressDSP™ tools..

Once the compilation target is selected, the Code composer studio is invoked using fixed standard instruction to compile the model for hardware simulation. With eZdsp F2812 drivers and target content already installed, it is selected in the code composer studio setup. The CCStudio produces a binary object file format (COFF) that promotes modular programming by supporting the concept of sections. All COFF sections are independently relocatable in memory space. CCStudio not only generates code but also integrates basic supports for debuging, namely: read and write to IO registers and DSP memory, run, step, halt, reset, set and clear breakpoints.

RTDX and links for CCS IDE provide a communications pathway to manipulate data and processing programs on your target digital signal processor. RTDX offers real-time data exchange in two directions between MATLAB and your target process.

Computer Simulation Result

DSP Simulation Results

Time (sec)
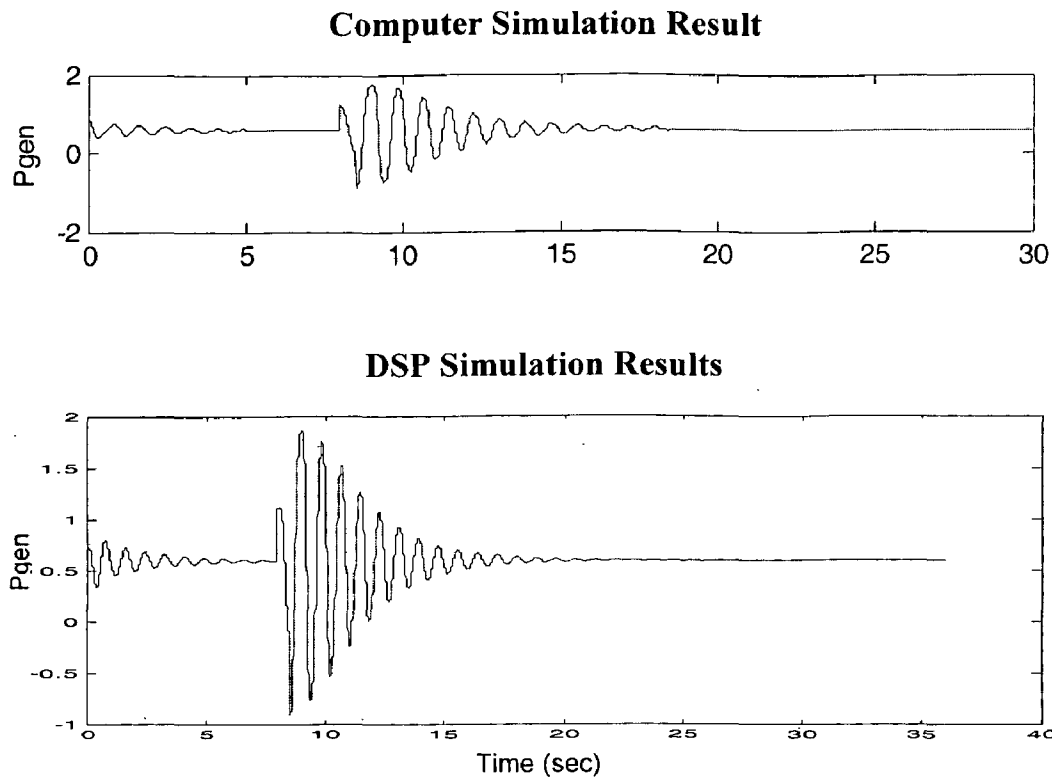
Figure 5.18 : Comparison of Computer and DSP Simulation Results: Reactive Power Generated Vs Time Characteristic of Generator 2

Computer Simultion Result

DSP Simulation Results

Time (sec)
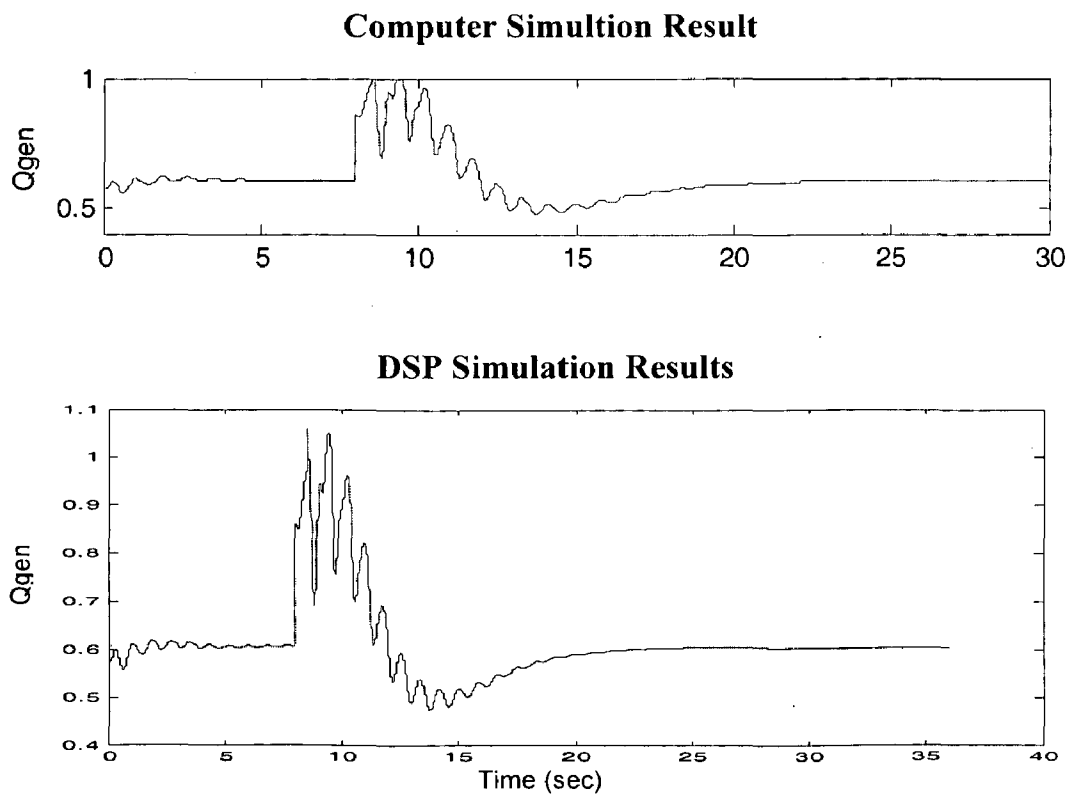
Figure 5.19 : Comparison of Computer and DSP Simulation Results: Reactive Power Generated Vs Time Characteristic of Generator 2

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5.3 Summary

In this Chapter, the experimental setup, simulation, DSP implementation and corresponding results for the simulation of SHP are presented Also hardware implementation of the system is presented. The simulation results were compared with the results from FPGA implementation.

Conclusion and Future Scope

Power systems are constantly evolving and there is need to include new technologies for controlling the flow of power and for improving the reliability of networks using advanced protection strategies. Real time simulation provides a solid frame work to test the new control/protection concepts so as to detect, analyze, and correct any potential problems.

Simulations of SHP under different operating conditions have been conducted, and the results indicate that the DSP based real-time simulator has a good performance.

The system combines the benefits of Simulink's intuitiveness and user-friendliness, with the real-time capabilities of DSP-implementation. DSP boards provide a quantum leap in performance over many powerful single- CPU computers. DSP technology is the choice of scientists and engineers who want a cost-effective solution to their processing needs. With the wide selection of hardware and software systems available, researchers can harness the power of DSP for use in real-time analysis applications. The power of DSP is limited only by the developer's ability to combine these components into real-time processing environments. As for the DSP implementation, there is a trade-off between flexibility and speed.

By developing DSP based real time simulator for analysing transient conditions in of SHP, several possibilities have been observed and could be carried out if the project is carried out on bigger scale:

- ✓ on existing hydroelectric power plants it is possible to investigate contingent restriction of operation conditions which are the consequence of bad design or if different requirements have been imposed upon the power system,
- ✓ in the process of new hydroelectric power plants design the simulator may be an efficient tool for choosing the optimal parameters of the main hydro mechanical equipment and electric devices for the plant, and
- ✓ it is possible to use the simulator in the training hydroelectric of the staff running the plant in order to improve reliability and availability.

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Data Used in Simulation:-

Penstock and Turbine data ([1])-

L_t	=	3850 m		A_t	=	38.5 m^2
L_p	=	250.0 m		A_p	=	5.0 m^2
f_p	=	0.0 m/ (m^3/sec)^2		g	=	9.8 m/sec^2
P_t	=	125 kW		H_o	=	15.0 m
H_r	=	10.0 m		Q_r	=	4.43 m^3/sec
Q_{nl}	=	0.00 m^3/sec		G_r	=	0.70 p.u.
D_t	=	0.01		a	=	1400 m/sec

PID Governor ([7])-

K_p	=	3.00		K_i	=	0.70
K_d	=	0.2		T_a	=	0.05 sec
T_c	=	0.02 sec		T_d	=	0.02 sec
R_{max}	=	0.2 p.u. /sec		R_{min}	=	-0.2 p.u. /sec
G_{max}	=	1.00		G_{min}	=	0.00
K_t	=	0.15		K_c	=	0.15

DC1A Exciter ([7])-

T_t	=	0.001		T_c	=	0.173
T_b	=	0.06		K_a	=	187

T_a	=	0.01	V_{max}	=	1.70
V_{min}	=	-1.70	T_e	=	0.01
A_{ex}	=	0.014	B_{ex}	=	1.55
K_f	=	0.1	T_f	=	0.001

4. Synchronous Generator ([7])-

H	=	3.7 sec	K_D	=	0.05
f_s	=	60.00 Hz	R_a	=	0.003 p.u.
L_l	=	0.150 p.u.	L_d	=	1.305 p.u.
L_q	=	1.76 p.u.	L_d'	=	0.296 p.u.
L_q'	=	0.65 p.u.	L_d''	=	0.252 p.u.
L_q''	=	0.23 p.u.	T_{do}'	=	4.5 sec
T_{qo}'	=	1.00 sec	T_{do}''	=	0.0681 sec
T_{qo}''	=	0.07 sec			

6. Transmission Line ([7])-

R_{line}	=	0.10	X_{line}	=	0.30
B_c	=	0.05			