MODELLING AND SIMULATION OF DC/DC CONVERTER

A DISSERTATION

Submitted in partial fulfillment of the requirements for the award of the degree

of

MASTER OF TECHNOLOGY

in

ELECTRICAL ENGINEERING

(With Specialization in Power Apparatus and Electric Drive)

By

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JUNE, 2006

CANDIDATE'S DECLARATION

I hereby declare that the work that is being presented in this dissertation report entitled "**MODELLING AND SIMULATION OF DC/DC CONVERTER**" submitted in partial fulfillment of the requirements for the award of the degree of **MASTER OF TECHNOLOGY** in **ELECTRICAL ENGINEERING** with specialization in **POWER APPARATUS AND ELECTRIC DRIVE**, submitted in the Department of Electrical Engineering, Indian Institute of Technology, Roorkee, is an authentic record of my own work carried out under the guidance of Dr. Pramod Agrawal, Professor, Department of Electrical engineering, IIT Roorkee, and Dr. S.P. Gupta, Professor & Head, Department of Electrical engineering.

The matter embodied in this dissertation report has not been submitted by me for the award of any other degree or diploma.

Date: 30.5.01

Place: Roorkee

(SUDHA BANSAL)

This is to certify that the above statement made by the candidate is correct to the best of our knowledge.

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ACKNOWLEDGEMENT

I wish to express my deep sense of gratitude and sincere thanks to my guides **Dr. Pramod Agrawal**, Professor, Department of Electrical engineering, IIT Roorkee, and **Dr. S.P. Gupta**, Professor & Head, Department of Electrical engineering, IIT Roorkee, for being helpful and a great source of inspiration. Their keen interest and constant encouragement gave me the confidence to complete my work. I wish to extend my sincere thanks for excellent guidance and suggestions for the successful completion of my dissertation work.

I am thankful to all of my classmates in PAED group for their constant support for successful completion of my work. I gratefully acknowledge my special thanks to Mr. Abdul Hamid Bhat, Ph.D, Research scholar for his valuable guidance and to my friends and family members for their inspirational impetus and moral support during the course of this work.

I also express sincere thanks to all staff members of Drives Lab and Electrical workshop for their help in completion of this work.

(Sudha Bansal)

ABSTRACT

The SMPS are used for many applications where regulated DC is required e.g. office equipment, spacecraft power systems, laptop computers, cordless phone etc. because of its high efficiency and high energy density. Though linear power supply can serve the purpose. The disadvantage with linear power supply is their bulkiness and poor efficiency. They can not work at high frequency. Earlier AC to DC conversion was achieved using Motor-Generator (MG) sets, Mercury-arc rectifiers, Cascade converter, Rotary Converters, thyratrons. The disadvantages of these are bulkiness and its poor regulation.

To overcome these limitations switch mode power supply are in use. Full bridge dc/dc converter topology is extensively applied in medium to high power conversion. In a power level up to 3 kW, the full bridge converter now employs MOSFET switches. High efficiency, high power density, high reliability and low EMI are some of the most desirable features in these applications, particularly for computer and telecom systems. To achieve these features, soft switching techniques are normally employed. Various types of soft switching topology are reviewed in the literature review. However, the conventional soft switching full bridge converter topologies would either lose the soft switching at some operating conditions, or become rather complex in design and implementation for a few kilo watts applications.

In this dissertation a novel zero voltage switching dc/dc full bridge converter topology is presented and analyzed. The proposed topology employs phase-shift at the rectifier section and does not employ any passive component. However, the advantage of the proposed topology is significant: it achieves soft switching independent of line and load conditions.

Experimental and simulation results of a prototype 200 W 100-110 Vdc to 50 Vdc converter operating at 10 KHz verify the analysis and design.

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CHAPTER- 1

INTRODUCTION

1.1 GENERAL

The DC supply is widely used in automotive, aerospace, communication systems, marine industry, medical and military applications. It is also used in various equipments including power supplies for office equipment, spacecraft power systems, laptop computers, cordless phone, portable personal equipment i.e. MPEG player, personal computers and telecommunications equipment, as well as dc motor drives and also in specialised high-power applications such as battery charging, plating and welding.

Many Industrial applications require variable DC power. Some of these are:

i) Steel mills, paper and textiles mills employing DC motor drives.

ii) AC- fed traction system using DC traction motors.

iii) Electro-chemical and electro-metallurgical processes.

iv) Magnet power supplies.

v) Reactor controls.

vi) Portable hand- tool drives.

For these applications earlier AC to DC conversion was achieved using Motor-Generator (MG) sets, Mercury-arc rectifiers, Cascade converter, Rotary Converters, thyratrons.

A Cascade Converter is a type of motor-generator which consists of an induction motor driving a dynamo through a shaft. In addition, the rotor of the induction motor is electrically connected to the armature of the dynamo. When the machine is running, half the power is transmitted mechanically through the shaft while the other half is transmitted electrically. The advantage of this arrangement is that the machine can be smaller than a conventional motor-generator of the same power. The rotary converter can be thought of as motor- generator where the two machines share a single rotating armature and set of field coils. In this two commutators one at each end of the armature are used. The advantage of rotary converter over the discrete motor-generator set is that the rotary converter avoids converting all of the power flow into the mechanical energy and then back into electrical energy, some of the electrical energy instead flows directly

from input to output, allowing the rotary converter to be much smaller and lighter than amotore- generator set of an equivalent power –handling capability. Mercury arc rectifiers were used until the 1960s for the production of high voltage direct current. applications included power supply for streetcars and electric railways, variable-voltage power supplies for large radio transmitters, and static inverters. Small mercury arc rectifiers were used in the power supplies for vacuum tube (valve) electronic equipment such as power amplifiers and transmitters.

Since 1960 mercury arc rectifiers were increasingly replaced by silicon rectifiers. Conventionally such rectifiers have been being made using a diode bridge rectifier the input to which is given through a three phase autotransformer which in turn is controlled by a stepper motor or a servomotor to get a controlled output. Linear power supplies also used to regulate the output by generating a higher voltage than needed at the output, then reducing it by converting some of the electrical power to heat. This loss is a necessary part of the operation of the circuit, and cannot be eliminated by improving the design.

Such systems are simple in configuration but they are quite bulky. The power factor of the system is poor and the total harmonic distortion is also high, efficiency is poor. The system is slow in response due to the mechanical movement of the motor used to control the applied input voltage. Linear power supplies use a mains-transformer operating at the mains frequency of 50/60 Hz (if they are isolating types), and line-frequency smoothing filters. These components are larger and heavier.

1.2 SWITCH MODE POWER SUPPLY

Today in the quest for the ultimate in user comfort, the tendency to reduce the physical size and weight of the battery of portable personal equipment. The switching-mode power supply offers a better solution in this case. It provides the power supply function through low loss components such as capacitors, inductors, and transformers and the use of switches that are in one of two states, on or off. The advantage is that the switch dissipates very little power in either of these two states and power conversion can be accomplished with minimal power loss, which equates to high efficiency. Switched power supplies are more efficient, lighter in weight , having

excellent closed loop operation , no mechanical wear and tear and they tend to have an efficiency of 80% or more. Block Diagram of an SMPS is shown in figure-1.1.

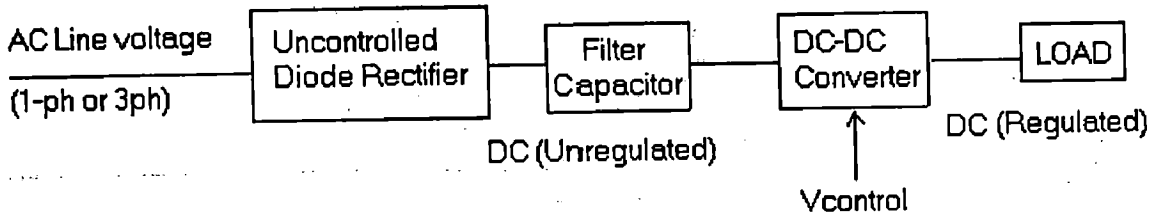


Figure-1.1 : Block Diagram of an SMPS

The main controlling block of the switching-mode power supply is DC-DC converters. Switched-mode power supplies can be classified according to the circuit isolation in the two categories:

- Non –isolating converters (i.e. Buck, Boost, Buckboost, Cuk converters).
- Isolating converters (i.e. Flyback, Forward converters).

Isolating forward converters are mainly two switch forward, and half-bridge converters, full-bridge, type. Among these possibilities for the power level under consideration (1 kW), half-bridge converter and full bridge converter provide the best combination of simple structure, low device stress and soft switching capability. Isolating full-bridge forward converter uses transformer for isolation purpose, which has certain advantages over non-isolating converters. These are:

- to obtain dc isolation between the converter input and output
- when a large step-up or step-down conversion ratio is required, the use of a transformer can allow better converter optimization. By proper choice of the transformer turns ratio, the voltage or current stresses imposed on the transistors and diodes can be minimized, leading to improved efficiency and lower cost.
- The ability to set the turns ratio also removes the V_{in} vs. V_o and polarity restrictions that apply to the basic topologies. Also, multiple outputs at various voltages are easily obtained with multiple secondary windings.

- since transformer size and weight vary inversely with frequency, thus high frequencies lead to dramatic reductions in transformer size.

Disadvantages are:

- additional cost, size and weight,
- losses in the core and windings,
- potential core saturation (especially in push-pull circuits, core reset in single-ended circuits, and voltage spikes and losses due to transformer leakage reactance).

Full-bridge dc/dc converters are extensively used in medium to high power level applications. For most of these applications, particularly those for the computer and telecommunication systems, the most desirable features of the converter are high efficiency, high power density, high reliability and low Electro-Magnetic Interference (EMI). The standard full bridge topology operates in hard switching, and the hard switching converter is unable to achieve high efficiency and high power density for the following reasons:

- in order to achieve high power density, the switching frequency is normally increased, because at increased frequencies, the converter can employ smaller sized power magnetics and capacitors, both of which are the largest devices of a power converter.

However, as the switching frequency increases, the switching losses associated with the turning on and off of switches will become excessive. These losses greatly reduce the converter's overall efficiency, and high power density is not achievable due to the resultant high cooling requirements. Switching loss imposes an upper limit on the switching frequencies of practical converters. Several mechanisms lead to switching loss. During the switching transitions, the transistor voltage and current are simultaneously large. In consequence, the transistor experiences high instantaneous power loss. This can lead to significant average power loss, even though the switching transitions are short in duration. The diode reverse recovery process induces substantial additional energy loss in the transistor during the transistor turn-on transition. The energy stored in the semiconductor output capacitances is dissipated during the transistor turn-on transition. Energy stored in transformer leakage inductances and other stray inductances

is usually dissipated by the transistor during the turn-off transition. The total switching loss is equal to the sum of the energy losses that arise via these mechanisms, multiplied by the switching frequency. Switching loss causes the converter efficiency to decrease as the switching frequency is increased.

1.3 SOFT SWITCHING TECHNIQUES

To solve these problems, soft switching techniques are normally used. Basically there are two types of the soft switching techniques: Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS). Either of the techniques can greatly reduce and even completely eliminate the switching losses in the converter. However, it is well understood that ZVS is more advantageous for a MOSFET switch topology than the ZCS. High power level full bridge converters usually use IGBT switches, due to IGBT's low conduction losses and higher power capability. However, IGBT is not as fast as MOSFET, and its switching frequency can not be increased beyond 50 kHz even if softly switched. Contrary to IGBT, MOSFET is a resistive device when it is turned on, and the conduction losses are higher as compared to IGBT at high power levels. However, MOSFET is a faster device and is able to operate up to a few MHz.

Isolated converter topologies provide advantages in applications requiring large voltage conversion ratios. Hence an isolated topology is favored for converter optimization through the incorporation of a small high-frequency transformer. Transformer isolation can reduce switch and diode device stresses and allows multiple windings or taps to be used to for multiple converter outputs. The full-bridge is a popular design for both buck and boost applications and has become a basis for numerous resonant zero voltage and zero current switching (ZVS, ZCS) schemes. Often in high power applications a phase shift modulation (PSM) switching scheme is used to achieve ZVS and/or ZCS transitions through the interaction of converter parasitic energy storage. The main limitations of phase-shift ZVS/ZCS topologies are:

- High circulating current
- Soft switching is not achieved for wide load range

1.4 ORGANISATION OF THIS THESIS

CHAPTER 2: This chapter is a review of the various publications in this field has been discussed briefly.

CHAPTER 3: This chapter focuses on the various principle of control strategy i.e. voltage mode control, current mode control, peak current mode control, hysteresis current control etc. The comparative advantages and disadvantages of each strategy are discussed.

CHAPTER 4: In this chapter, the topology of ZVS PWM for the full-bridge Phase-shifted secondary dc/dc converter has been selected and the reasons for selecting the topology have been mentioned. The comparison with ZVS PWM for the full-bridge Phase-shifted Primary dc/dc converter topology in which phase shift is given at the inverter section is also discussed. The advantages of using phase-shifted strategy at the secondary side are described.

CHAPTER 5 : This chapter discusses the detailed circuit operation of the ZVS PWM for the Full-bridge Phase-shifted secondary dc/dc converter topology and the circuit equation at the various interval are given. Equivalent circuit in different mode is drawn and the state space equation are derived. Then small signal model is obtained for the system by which overall transfer function of the whole system is found.

CHAPTER 6 : This chapter calculates the various parameters which is required in deciding the component selection for hardware development. The selection of switches, diodes, Transformer parameters on the basis of design specification is done.

CHAPTER 7 : This chapter includes the simulation of Full-Bridge ZVS Phase-shifted DC/DC converters . The converter's performance is tested in the case

- when step up change in the input voltage occurs at 0.1 sec.
- when the load is step up changed at 0.2 sec.

The voltage across the devices is recorded in order to see whether ZVS is achieved.

CHAPTER 8 : This chapter consists of hardware development of control circuit for single-phase inverter and phase-shifted gating control circuit for the synchronous rectifier section. These pulses obtained from the control circuits are amplified through Firing Pulse Amplification & Isolation Circuit. The +5 V, +12 V, -12V power supply for the dc

biasing of different IC's are developed. Current sensor circuit for the measurement of current is fabricated.

CHAPTER 9 : In this chapter the experimental results for the developed prototype recorded are presented. The waveform of firing pulses to MOSFETs, voltage across transformer primary and secondary ,current in the transformer primary, the voltage across the switches and the output voltage have been described.

CHAPTER 10 : Conclusions of the thesis work are drawn in this chapter followed by suggestions for future work

In this chapter, the need for a DC supply has been emphasized. The various industrial approaches for the generation of DC supply and its regulation and their limitations have been discussed. The use of switch mode power supply to overcome those limitations has also been presented. Block diagram of switch mode power supply and various types of it has been discussed. The benefits and limitations of use of high frequency in the switch mode power supply with the stress upon using soft-switching in overcoming the limitations and reducing the size and weight of power supply has been detailed. In the next chapter the limitations occur in the conventional converters will be discussed and the methods to improve soft-switching at various load conditions are being discussed.

CHAPTER- 2

LITERATURE REVIEW

The problems faced in the conventional Full bridge ZVS PWM dc/dc converters are discussed in this chapter and suggestion of remedial measures by researchers to overcome these problems are reviewed. Each of them has suggested one or the other modification in the conventional circuit so as to get improvement in the results. Full bridge ZVS PWM dc/dc converters are some of the simplest power electronic circuits. They are widely used in the power supply equipment for most electronic instruments and also in specialized high-power applications such as battery charging, plating and welding etc. Various topologies are used to make such dc/dc converters. Each topology has got its own advantages and disadvantages and the real choice depends on the application. In this chapter, a brief overview of the various topologies used for Full bridge Phase- shifted ZVS PWM dc/dc converters is presented.

Full Bridge Zero Voltage Switched Phase Shift DC-DC Converter is preferred due to its remarkable features [1] –[4]. It combines the advantages of quasi-resonant converters in what concerns the turn on switching losses, and also the advantages of classical PWM converters related to conduction losses and operating frequency. These benefits can be summarized as follows:

- zero voltage switching for all the bridge transistors;
- reduction of the conduction losses when compared with Quasi Resonant converters;
- reduction of the electromagnetic noise;
- utilization of the devices' output capacitances and transformer leakage inductance; and
- fixed frequency operation.

However, there are some drawbacks:

1. High circulating currents;
2. loss of duty cycle and

3. ZVS is lost for light loads.

These problems are due to the fact that to assure ZVS in a wide range of load and input voltage, it is necessary to have sufficient stored energy in the leakage inductor. Especially at light loads, the energy stored in the leakage inductor of the transformer is not sufficient to achieve ZVS. Therefore, there is a need of adding a commutating inductor in series with the primary winding of the transformer. As it is known the size of this inductor increases with the ranges of variation of the input voltage and of the load, where ZVS is to be maintained. A large commutating inductor enables ZVS in a wide range of load and input voltage but also causes higher circulating energy, which increases the conduction losses. A large commutating inductor is also responsible for a larger loss of duty cycle because the primary current transitions, in order to change its polarity, are slower. So, there must be a design compromise considering the specifications of input voltage and load ranges and the effective duty cycle and efficiency.

To solve these problems some different solutions have been proposed:

- Richard Redl in [5]-[6] uses a primary commutating inductor with one terminal connected to the passive to active leg midpoint, and the other connected to the input voltage source via two clamping diodes shown in Fig-2.1. With this process, zero voltage switching is achieved in a wide range of load current for the bridge transistors. However, the clamping diodes, that provide a continuous current in the P-A leg, suffer from hard switching, with the consequent commutating losses.

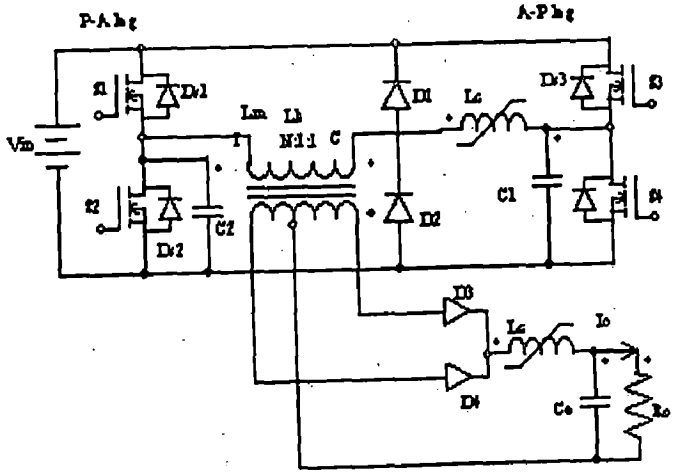


Fig- 2.1: Optimum ZVS Full-Bridge DC/DC Converter with PWM Phase-Shift Control [5]

Advantages

i) Reduce the voltage stress due to ringing and overshoot across the rectifier diodes.

ii) The extension of soft switching toward light load

iii) An optimal winding configuration of the power transformer (There is no need to build in a large leakage inductance in the transformer)

➢ A New Family of Full-Bridge ZVS Converters is proposed in [7]-[8]. The ZVS of primary switches is achieved by employing two magnetic components whose volt-second products change in the opposite directions with a change of phase shift between the two bridge legs. One magnetic component is a transformer while the other magnetic component is either a coupled inductor or a single-winding inductor. In this the energy available for ZVS increases as the input voltage increases, which is the desirable direction of change since more energy is required to achieve ZVS at higher input voltages.

Advantages :

- The stored energy is independent of load.
- Ideally, the auxiliary circuit needs to provide very little energy, if any, at full load because the full-load current stores enough energy in converter's inductive components to achieve a complete ZVS for all switches. As the load current decreases, the auxiliary circuit needs to provide progressively more ZVS energy, with the maximum energy required at no load.
- zero-voltage-switching (ZVS) of all bridge switches over a wide range of input voltage

Disadvantage

- duty cycle loss and circulating current
- voltage unbalance of the transformer at starting up.

➢ A comparative study of a class of full bridge zero-voltage-switched PWM converters is discussed in [7]. Four different topologies are compared-

a) linear resonant inductor is employed to achieve ZVS, in this approach ZVS is achieved for a narrow range and also secondary parasitic ringing is very large.

b) It is observed that by employing saturable inductor and reducing the leakage inductance of the transformer ZVS range can be extended to a wide range, circulating energy is reduced and ringing in the secondary side is small.

c) ZVS range can be extended to no-load if magnetizing inductor is used; also secondary parasitic oscillations are greatly reduced because of the very small leakage inductance.

Disadvantage:

i) deliberately increased magnetizing energy circulates in the primary, resulting in an increased conduction loss.

d) In this approach, Instead of using the energy stored in the magnetizing inductance to achieve ZVS, the saturable reactors can be arranged to utilize the energy of the output filter inductor to obtain ZVS. It causes circulating energy very small, hence efficiency is higher. Secondary parasitic ringing is virtually eliminated because of the use of a very small leakage inductance and because of the damping effect of the saturable reactors.

- The converter topology presented [10] here employs an asymmetrical auxiliary circuit consisting of four drain-to-source snubber capacitors, each connected across one switch, a capacitor voltage divider, and two auxiliary inductors.. With this auxiliary circuit, the full bridge converter can achieve ZVS independent of line and load conditions.

In terms of power transfer from the input to load, the power circuit operates in exactly the same way as does a conventional phase-shift full bridge converter, and the auxiliary circuit hardly interferes with this power transfer. However, the auxiliary circuit does have significant influences on the switching

transients of the switches: it removes the switching losses from all the switches, at both turn-on and turn-off.

- In reference [11-[13] define the limitations of the FB-ZVS-PWM converter and use a saturable reactor in series with the primary winding or with the secondary rectifier diodes. This process enables a wider range of operation under ZVS without a significant increase in conduction losses. However, it is always a problem to eliminate energy excess when saturation occurs.

- Novel soft-commutation DC–DC power converter with high-frequency transformer secondary side phase-shifted PWM active rectifier [14], can achieve ZVS for non-controlled active power switches on the primary side of the transformer and ZCS for PS–PWM active switches on the secondary side of the transformer under wide load variations as well as a wide PS–PWM regulation range. The switching power losses and conduction power losses of the active devices of the proposed DC–DC converter can be considerably reduced, because it blocks circulating current.

- Two distinct resonant dc/dc converter topologies, which exhibit near zero switching losses is presented in [15] shown in Fig-2.2. The difference between two topologies is the connection of auxiliary circuit in series or in parallel. Connection of an inductor and a capacitor in the series branch makes it well suited for low input voltage, low output voltage, and high output current. While parallel-connected topology is favorable for high voltage, high power system with ultra low ripples requirements.

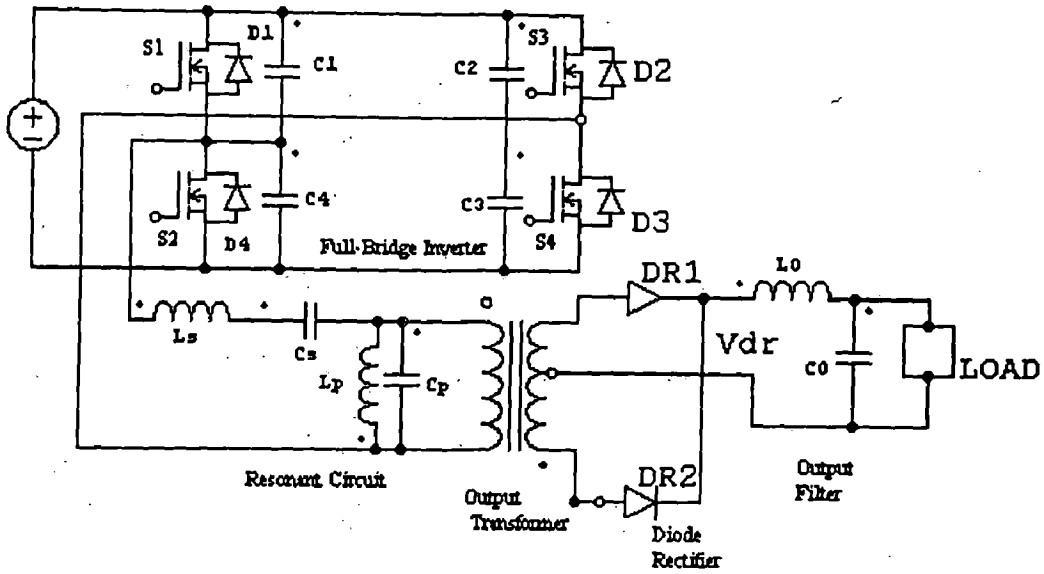


Fig-2.2 : Constant Frequency Resonant DC/DC Converters With Zero Switching Losses [15]

- A single-stage converter with an auxiliary circuit that allows its main power circuit switches to operate with ZVS is given in [16]. The features of this converter include soft switching all switches, fixed frequency operation, and PFC with a continuous input current. The auxiliary circuit shown in Fig-2.3, is simple, requires only one active switch, and operates with a ZCS turn-on and a ZVS turn-off.

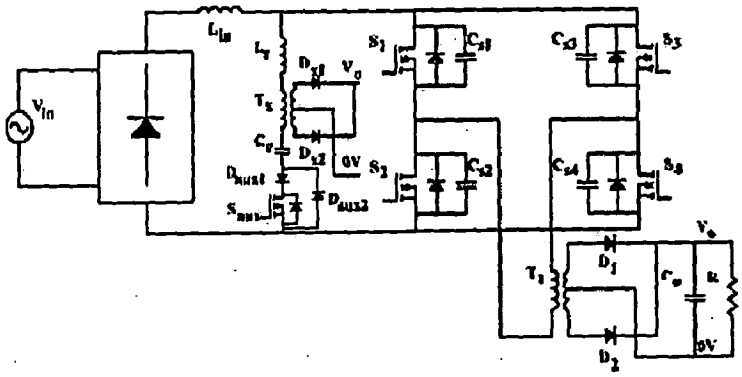


Fig-2.3: Single-Stage ZVS PWM Full-Bridge Converter [16]

- [17] is based on the principle of the self-resonance, that is: an auxiliary voltage source feeds the resonant circuit, charging the capacitor, which provides the condition for the zero voltage switching (ZVS) of the main switches.

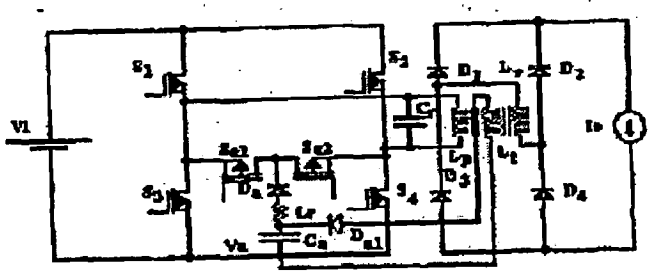


Fig-2.4: A Novel Single-Phase Soft-Switched Rectifier with Unity Power Factor and Minimal Component Count [17]

- A novel, single-phase soft-switched boost ac–dc rectifier [18]-[19] that operates with power-factor correction are discussed. The rectifier is a modified boost voltage-doubler converter well suited for low-line-input applications. It operates with fewer conduction losses and half the switch voltage stresses found in a standard boost converter. Soft switching in the converter is achieved using a zero-current-switching quasi-resonant technique.

- By replacing the linear resonant inductor with a nonlinear inductor. The inductance value of which decreases with the increasing of the load current and hence achieve zero-voltage switching for a wide load range [20].

- A soft-switching converter topology [21], which employs a small saturable reactor, can achieve soft- switching in a wide load range from no load to full load without substantial reduction for the output voltage and no substantial increase in current stresses. Since saturable reactor acts as a magnetic switch, blocks the load current during the switching transition interval.

- '1 kW/250 kHz Full Bridge Zero Voltage Switched Phase Shift DC-DC Converter with Improved Efficiency' is proposed in [22]. In this a two-windings inductor is used. The inductor primary winding is connected in series with the transformer primary and its secondary is connected to the output capacitor by two rectifier diodes is shown in Fig-2.5. This process enables the recovering of the excess of energy directly to the load and in an increase in the effective duty cycle, which

permits to increase the converter performance. Stress analysis of switches is presented in [23].

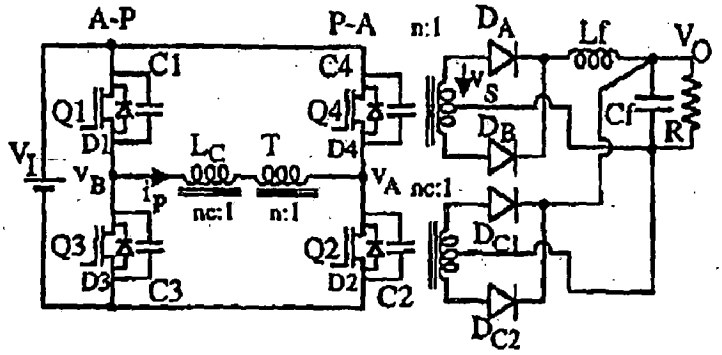


Fig-2.5: Full Bridge Zero Voltage Switched Phase Shift DC-DC Converter with Improved Efficiency [22]

- Liviu Mihalache, proposed a new PWM technique [24] to ensure uniform losses among all four devices. The basic idea is to make one leg behave as the "leading leg" in one period and as a "lagging leg" in the next period, thus the average losses over two periods are equal for all four devices, for this it utilizes a different gating method.

- In [25] leakage inductance is increased to achieve ZVS with wide input voltage range and load range but it causes voltage ringing across rectifier diodes, which is reduced by adding two clamp diodes in the primary side of the transformer.

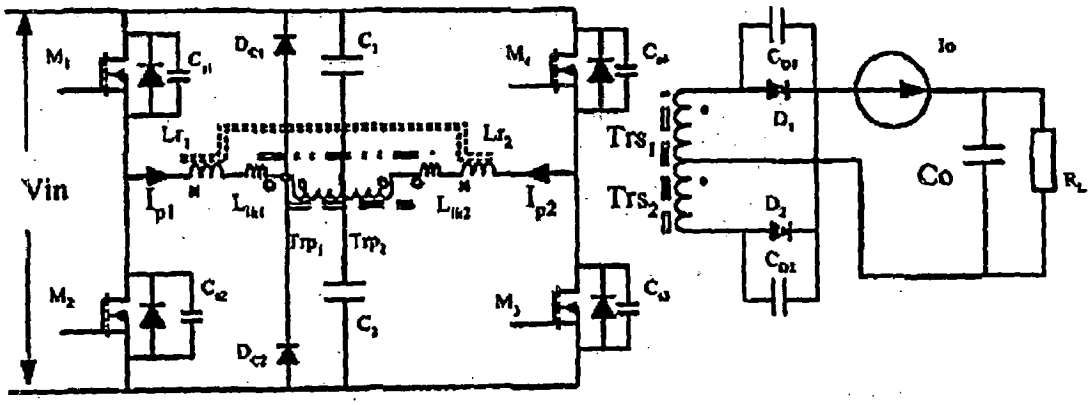


Fig-2.6: An improved high efficiency Full Bridge ZVS DC-DC converter [25]

- With the inclusion of a LCC auxiliary circuit [26], primary current will become reinforced during the passive-to active transition, thus increasing the available energy to achieve ZVS and minimizing the problems of duty cycle.

- It utilizes the magnetizing inductance of the transformer to achieve zero voltage turn-on of the primary switches [27]. By employing saturable inductor(s) on the secondary-side, soft turn-off of the output rectifier(s) is obtained with a minimum circulating energy flowing through the converter.

- In [28] a New Start-up Schemes for Isolated Full-Bridge Boost Converters is proposed The purpose of using a start-up circuit for a boost-type converter is to establish an initial output voltage before the converter operates in the normal boost mode. The initial output voltage should not be lower than the input voltage (reflected).

- ZVS for the leading-leg switches is easily achievable for very wide line and load ranges. However, ZVS of the lagging-leg switches is achieved by the energy stored in the transformer leakage inductance. So, the ZVS range of the lagging-leg switches is quite limited unless the leakage inductance is very large. IGBT's with large external capacitors cannot be used for the lagging-leg switches, since the external capacitor reduces the ZVS range. In [29] by using the dc blocking capacitor and a saturable inductor, the primary current during the freewheeling period is reduced to zero, allowing the lagging-leg switches to be operated with zero- current-switching (ZCS). The new converter overcomes the limitations such as high circulating energy, loss of duty cycle, and limited ZVS load range for the lagging-leg switches. In [30] little modification in the circuit is made by adding a secondary active clamp instead of using lossy components or the saturable reactor, ZVS (for leading-leg switches) and ZCS (for lagging-leg switches) are achieved. It increases efficiency of the converter.

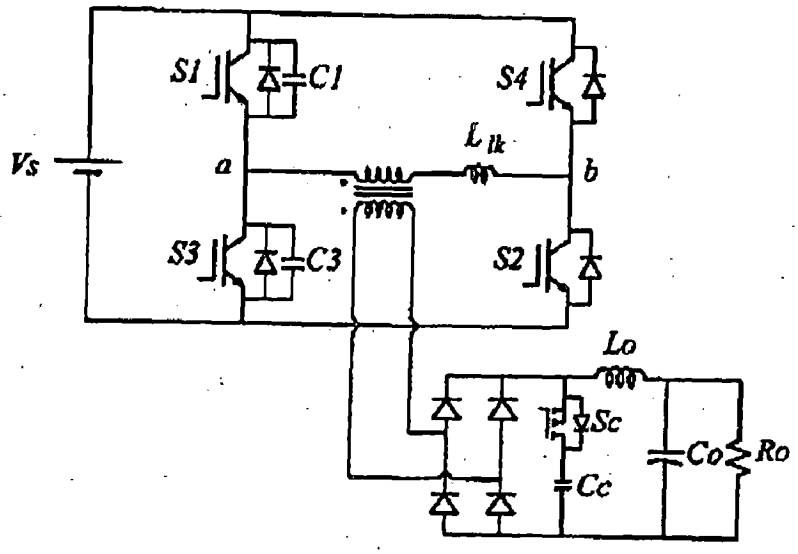


Fig-2.7: Zero-Voltage and Zero-Current-Switching Full Bridge PWM Converter [29]

In this chapter an overview of the various topology of Full-bridge PWM ZVS phase-shifted dc/dc converter has been provided. These topologies are basically related to the various method employed for achieving ZVS at wide load range and supply variation. These topologies employ various auxiliary circuits to achieve this. Most of the topologies have used the phase-shifted in the primary Inverter section. In the chapter 4, the topology selected will use the phase-shift in the secondary rectifier section. Two diodes are being replaced with active switches for the purpose. It will help in achieving the ZVS at wide load range without incorporating any auxiliary circuit and hence will reduce the component count.

CHAPTER- 3
CONTROL TECHNIQUES FOR DC –DC CONVERTERS

In this chapter various control techniques used for dc/dc converters are discussed. Each technique has its own advantages and disadvantages. These techniques depend on the parameter, which is sensed in the converter to regulate the output in the closed loop operation. These are categorized into, voltage mode control, peak current mode control, average current mode control, sensor less current mode control etc. This technique is used in the chapter-8 for designing the control circuit for phase-shift control.

In all switching converters the output voltage v(t) is a function of input line voltage $v_g(t)$, duty cycle d(t), and the load current $i_{load}(t)$ as well as the converter circuit element values. In DC-DC converter applications it is desired to obtain a constant output voltage v(t) = V, in spite of the disturbances in $v_g(t)$ and $i_{load}(t)$, and in spite of variations in the converter circuit element values. The unknown and unmeasurable variations of the process parameters degrade the performance of the control system. Feedback is used in conventional control systems to reject the effect of the disturbances upon the controlled variables and to bring them back to their desired values. To achieve this, first the controlled variables are measured then compared with the desired values and the difference is fed into controller, which will appropriately control these variables to meet the desired specifications.

3.1 Voltage Mode Control [D]

A feedback loop can be constructed for regulation of the output voltage. The output voltage v(t) is compared to a reference voltage V_{ref}, to generate an error signal. This error signal is applied to the input of a compensation network, and the output of the compensator drives the control signal d(t) as shown in Figure 3.1.

In the case of a full bridge converter, the control signal d(t) is given to the control circuit to generates the appropriate turn on signals for all four switches .

Limitation :

1. In voltage mode control any change in the source or load is only detected after it has propagated to the output.
2. This slows the control, especially when the source voltage changes.

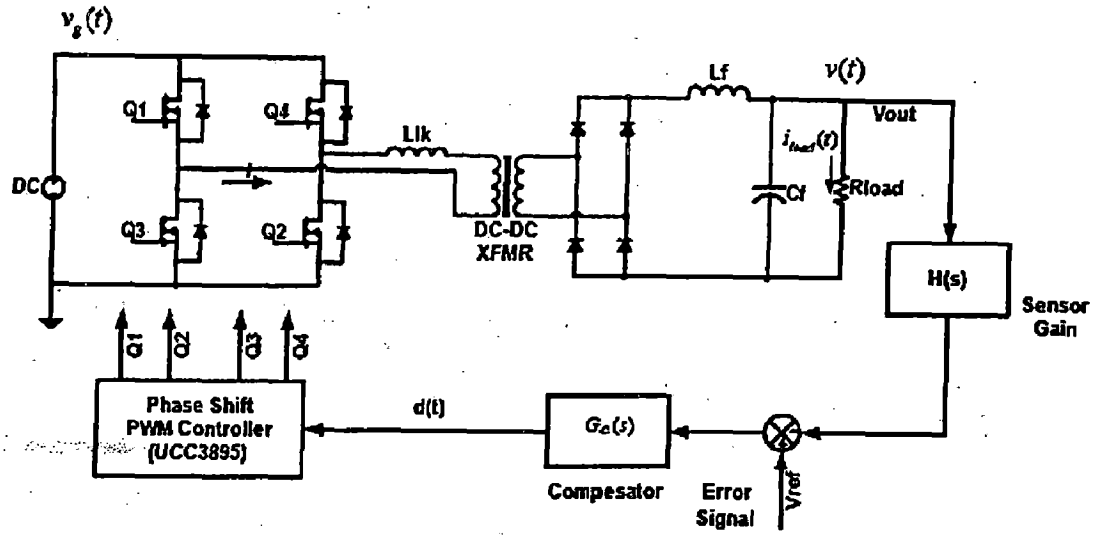


Fig.-3.1: Voltage Mode Control

3.2 Current Mode Control [D]

Another control scheme that finds a wide application is current mode control. In this type of control the inductor current is used as a feedback state. However the current and voltage reference values are not independent and this specifically requires knowledge of the load. To overcome this obstacle the voltage error signal is used to generate a current error signal as shown in Figure-3.2 . Using the current creates the drawback that the knowledge of how the current affects the voltage is needed. For example, in a resistive system, $v = ir$, and increasing v will increase i. However, in a constant power load, increasing v will decrease i to maintain the relationship $iv = p$, where p is typically constant. This means that the current reference should be smaller for larger voltages. This dependency in undesired, and is a drawback of this type of control. Misrepresenting the load can lead to decreased performance, and possibly instability. Current mode control requires knowledge of the inductor current, which is controlled via the inner loop. The outer loop manages the output voltage error by commanding the necessary current. The inner loop makes the converter act as a current source. There are many schemes that deal with current mode control. There are many methods to use to do current mode control, such as peak current mode control, average current mode control, sensor less current mode control. In this chapter a brief overview of the main schemes is described [D].

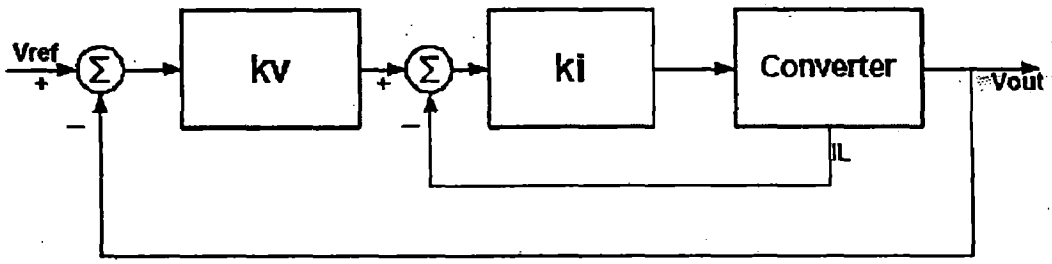


Fig-3.2: Current Mode control

3.3 Peak Current Mode Control [D]

The basic scheme of the peak current controller is shown in Figure-3.3 alongwith the generic inductor current of a switching converter operating in continuous conduction mode (CCM). The inductor current changes with a slope *m1* during the first subinterval, and a slope *–m2* during the second subinterval. At D > 0.5 there is an inherent instability which is not dependent of the converter topology. The controller can be made stable for all duty cycles by the addition of an artificial ramp with a slope M_a to the sensed current waveform. When $M_a \geq 0.5^* m_2$, then the controller is stable for all duty cycles. The controller now switches the transistor off when this summation crosses the reference value i_{ref}, as shown in Figure 3.3. The relationship between the ramp, inductor and reference current is given in equation (3.1) [D].

$$i_a(dT) + i_L(dT) = i_{ref} \qquad (3.1)$$

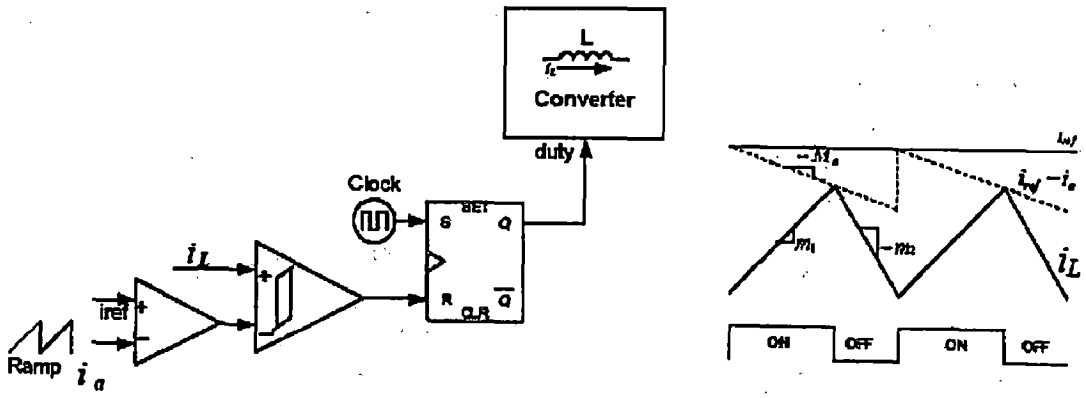


Figure 3.3. Peak current mode control

Some benefits of peak current mode control are:

- Control of the peak inductor current.
- Constant switching frequency.

- No need of current amplifier and its compensating network.
- Inherent current limiting and sharing.
- Good dynamics and performance.

Some of the limitations are:

- Limited accuracy in controlling the average inductor current (especially in the DCM case) (The peak and average inductor current are not related)
- Increased sensitivity to line variations
- Presence of sub-harmonic oscillations at duty cycle greater than 50%, so a compensation ramp is needed.
- Input current distortion which increase at high line voltages and light load and is worsened by the presence of compensation ramp.
- Increased switching noise problems.

3.4 Average Current Mode Control

In the average current mode control (ACM) a compensator is added to make the average inductor current track a reference as shown in Figure-3.4. The triangle carrier waveform in this case remains in place. In this case the variations in the duty cycle are dependent on the value of the averaged current [D].

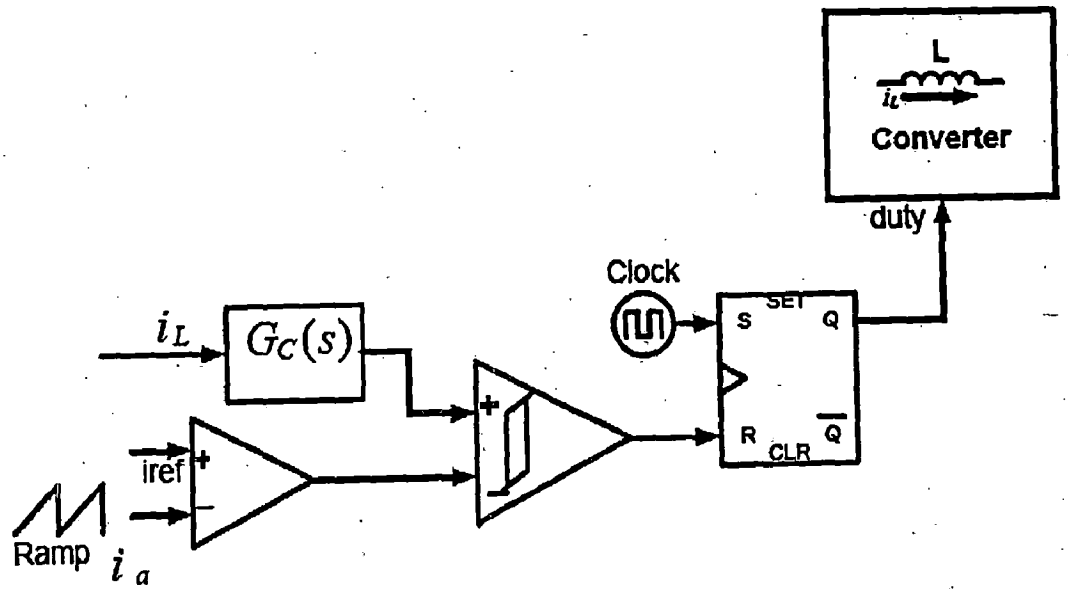


Figure 3.4. Average Current Mode Control (ACM)

Benefits :

- Constant switching frequency.
- No need of compensation ramp.
- Control is less sensitive to communication noises due to the current filtering.
- Better input current waveform than for the peak current control since near the zero crossing of the line voltage the duty cycle is close to unity, so reducing the dead angle in the input current.

Limitations :

- Inductor current must be saved.
- A current amplifier is needed.

3.5 Sensorless Current Mode Control

An alternative method for current mode control is to use an observer method. In an observer, a model of the system to be controlled is used in place of the system to provide estimates of the control state values. In the case of sensor less current mode control an observer state is used in the place of inductor current. Since the output should match the reference, the output is a command rather than a dynamic state. So the desired output reference value replaces the output state [D].

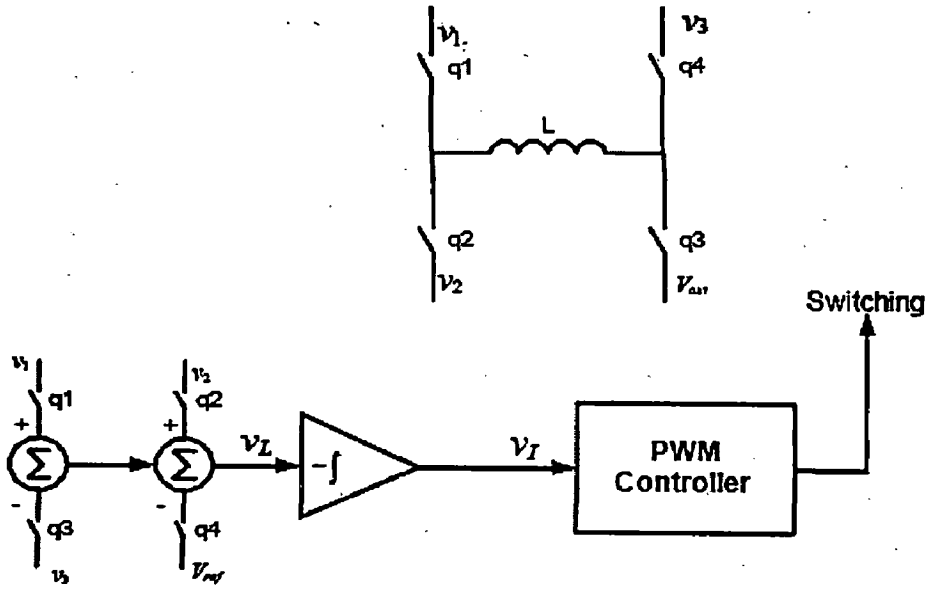


Figure 3.5. General SCM Process

The SCM signal can be used as a direct substitute for peak current mode control. It shares the two key properties of the current mode controls and it provides a direct match to peak current mode control :

- It compensates for changes in the input source
- It requires a stabilizing ramp to reach duty ratios above 50%.

This method, however, has its disadvantages:

- Since an integration step involves an arbitrary constant, the average DC current is not controlled.
- For current limiting or current sharing some extra control is needed
- The general version requires an analog representation of the switches or other means to create the observer, as shown in Figure 3.5.

In summary, the sensorless current mode (SCM) control uses the integrated inductor voltage as shown in Figure 3.6 in place of measured inductor current, and substitutes an intended command reference for the states intended to be fixed. The approach is based on an observer, which emulates the converter's operation. To implement the general form, low power switches are added to the PWM IC in order to support the method.

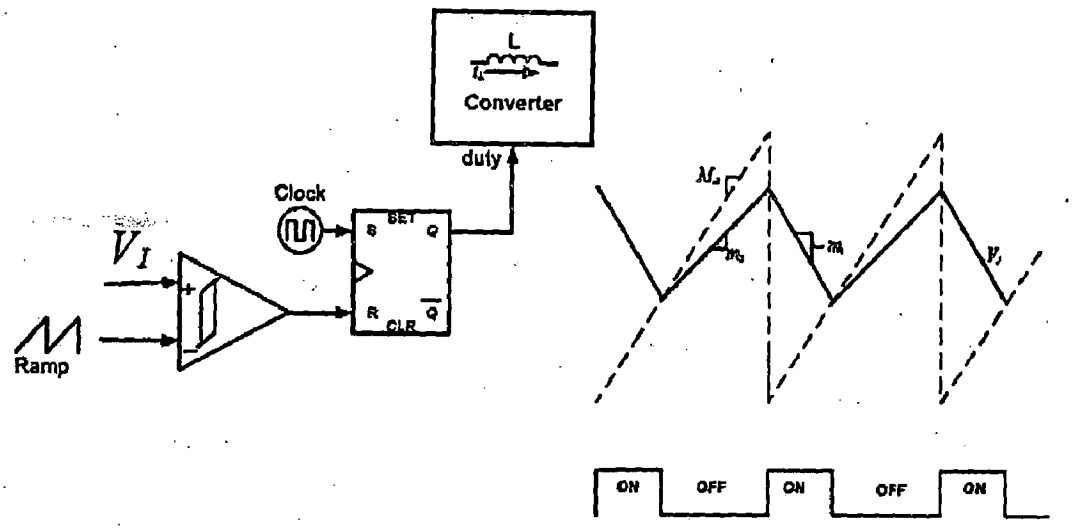


Figure 3.6. Sensorless Current Mode Control

In this chapter various control techniques has been discussed. Although the operation of the phase shifted full bridge converter is well known, its behaviour is dependent on some factors that are not known well. Such parameters have to do with the

nonlinear behavior of the converter itself. The transformers turns ratio, the coupling coefficient, the leakage inductance of the transformer, and the series resistance of the filter inductor are some of the parameters that can not be controlled closely and they vary with the load conditions, input source, and operating frequency.

All these factors could be controlled to a certain degree with relatively easy controllers, but if a tight performance is expected and the output voltage from the converter is required to be stiff, the controller has to be fast and noise immune and should have good disturbance rejection. As discussed in this chapter the current control methods are fast but are highly sensitive to noise. On the other hand, a voltage mode controller is noise immune, but usually its performance is slow and it does not correct until the disturbance has already taken effect. The most of the control technique differs only in the way the input current is controlled either in Continuous conduction mode or discontinuous conduction mode. Some techniques lead to constant switching frequency while others to variable switching frequency.

In the development of system the control technique used is voltage mode control technique. Output voltage is sensed with the voltage sensor IC AD 202. It is compared with the reference voltage and error signal is given to the PI controller. The control technique is described in chapter –5 and chapter-8 in detail.

CHAPTER - 4
ZVS FULL BRIDGE PHASE SHIFTED DC-DC CONVERTERS

4.1 INTRODUCTION

In this chapter two topology for the full-bridge ZVS PWM Phase-shifted dc/dc converters is described and a comparison in both is also presented. The simulation and experimental verification for both topology are given in the chapter 7 and chapter 9 respectively. In one topology the phase shift is given between the two legs of the Full-bridge Inverter connected to the primary of the transformer while in the second topology this phase-shift is given in the rectifier-section connected to the secondary of the transformer. Two active switches are connected in the secondary of the transformer forming Synchronous rectifier.

DC/DC Converter mainly consists of primary inverter topology and secondary rectifier section. Most front-end DC/DC converter designs evolve around full-bridge, two switch forward, and half-bridge converters. Among the possibilities and for the power level under consideration (1 kW), half-bridge converter and full bridge converter provide the best combination of simple structure, low device stress and soft switching capability.

4.2 ZVS Primary Phase Shifted Full Bridge Topology [1]

4.2.1 General Description

In the case of the conventional full bridge converter, the diagonally opposite switches (Q1 and Q2, or Q3 and Q4) are turned on and off simultaneously as shown in Fig- 4.1. In the FB-PWM converter, when all four switches are turned off, the load current freewheels through the rectifier diodes. In this case the energy stored in the leakage inductance of the power transformer causes severe ringing with MOSFET junction capacitances. This creates the need for using snubbers that increase the overall losses bringing down the efficiency. If snubbers are not used, the selection of the devices becomes more difficult as the voltage rating for these switches has to be much higher. As

the voltage rating goes up, so do the conduction losses and as a result the overall losses increase. At the same time the cost increases as well.

In order to minimize the parasitic ringing, the gate signals of Q2 and Q4 are delayed (phase-shifted) with respect to those of Q1 and Q3 , shown in Figure -4.2, so that the primary of the transformer is either connected to the input voltage or shorted. The leakage inductance current is never interrupted, thus solving the problem of parasitic ringing associated with the conventional full-bridge PWM converter. The energy stored in the leakage inductance can be used to discharge the energy stored in the MOSFET junction capacitances to achieve zero voltage switching (ZVS) conditions for all four switches in the primary side. In this case, the converter requires no additional resonant components.

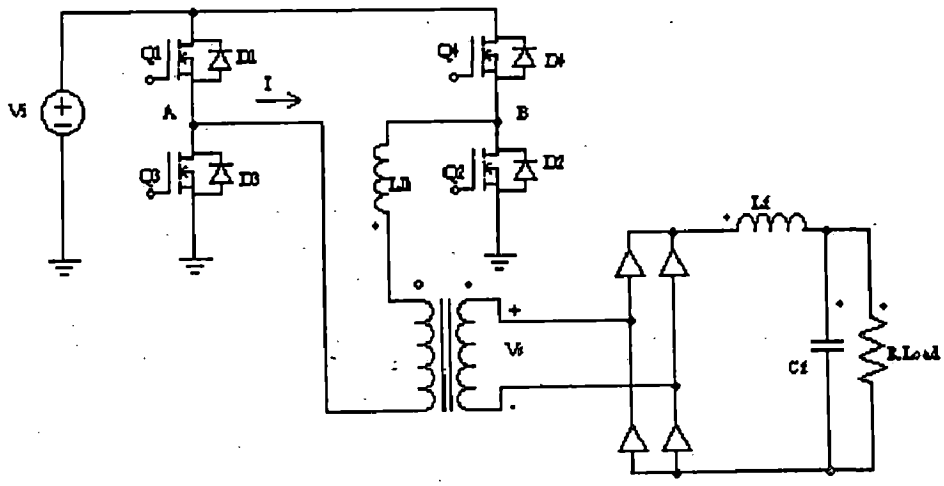


Fig-4.1: Full-bridge primary phase-shifted ZVS dc/dc converter

The gating signals for all four switches and the current waveform are shown in fig-4.2. To achieve ZVS, the two legs of the bridge are operated with a phase shift. This operation allows a resonant discharge of the output capacitances of the MOSFET's, and subsequently, forces the conduction of each MOSFET's antiparallel diode prior to the conduction of the MOSFET.

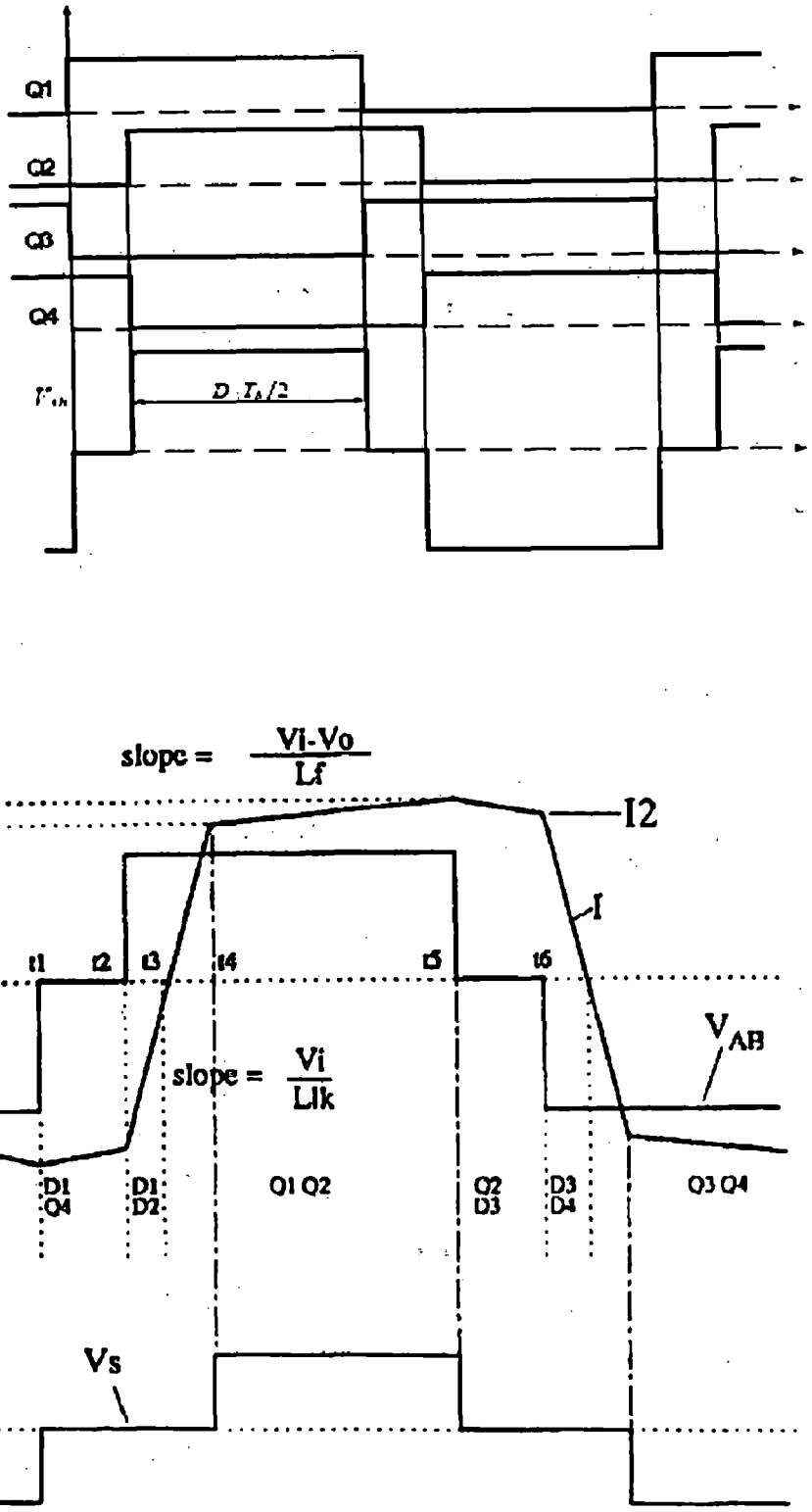


Fig-4.2: Operation and Current waveform [1]

4.2.2 CASPOC SIMULATION

The simulation of this topology are performed in the CASPOC to know about the performance of converter, the results are shown if figure-4.3. In the chapter -7 the simulation of both topologies are being carried out in the MATLAB for the switches performance under zero voltage switching. These results are compared with the actual experimental results.

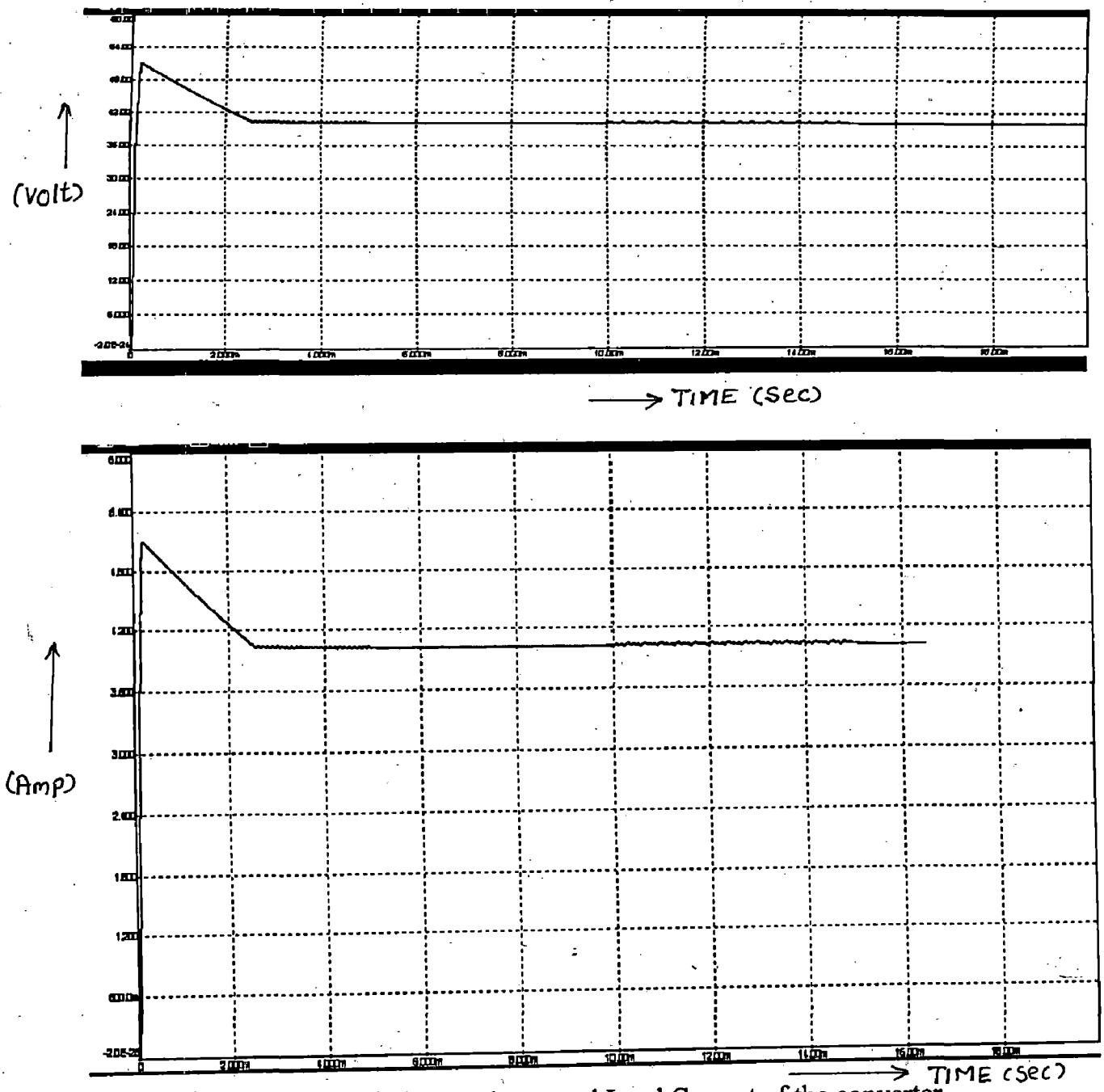


Fig.-4.3(a): Output Voltage and Load Current of the converter

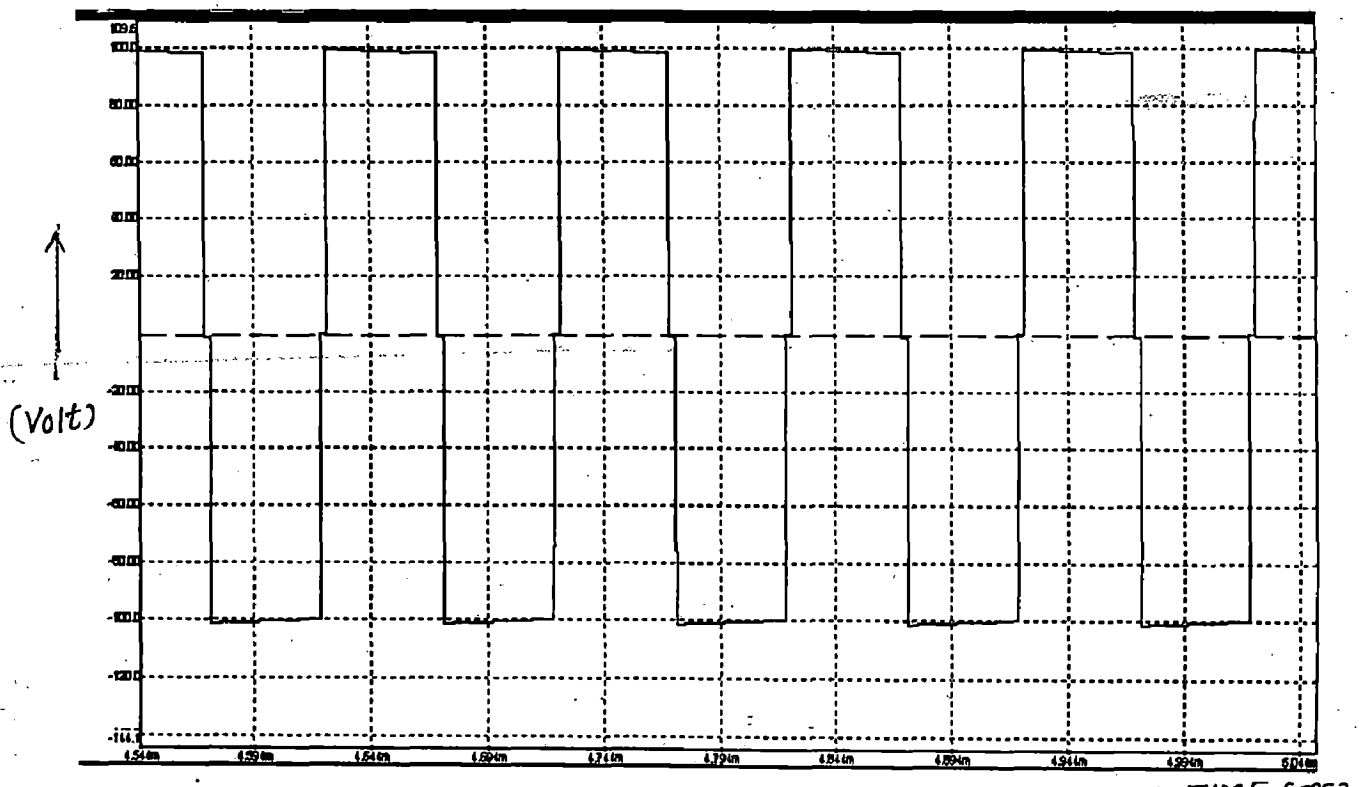


Fig-4.3(b): The Inverter output Voltage

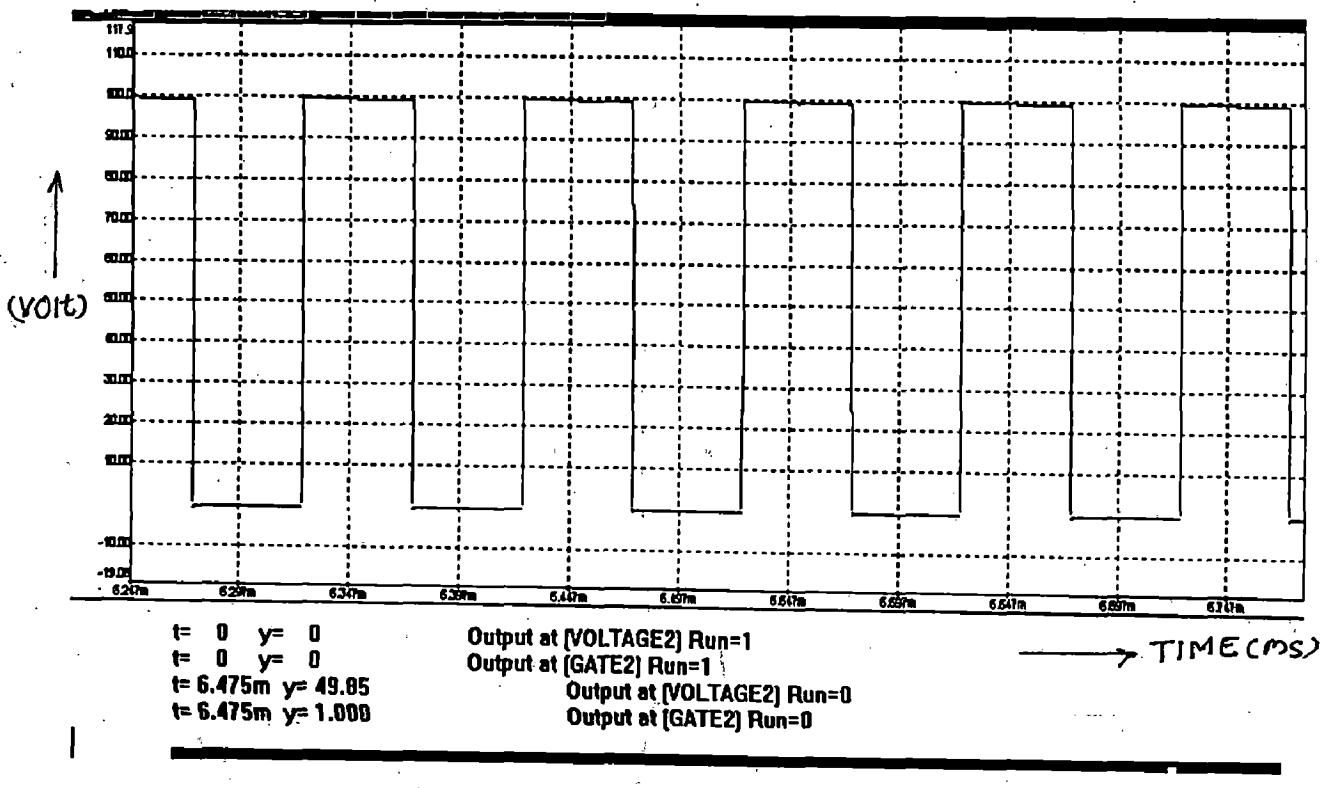


Fig.-4.3(c): Drain to source voltage across device

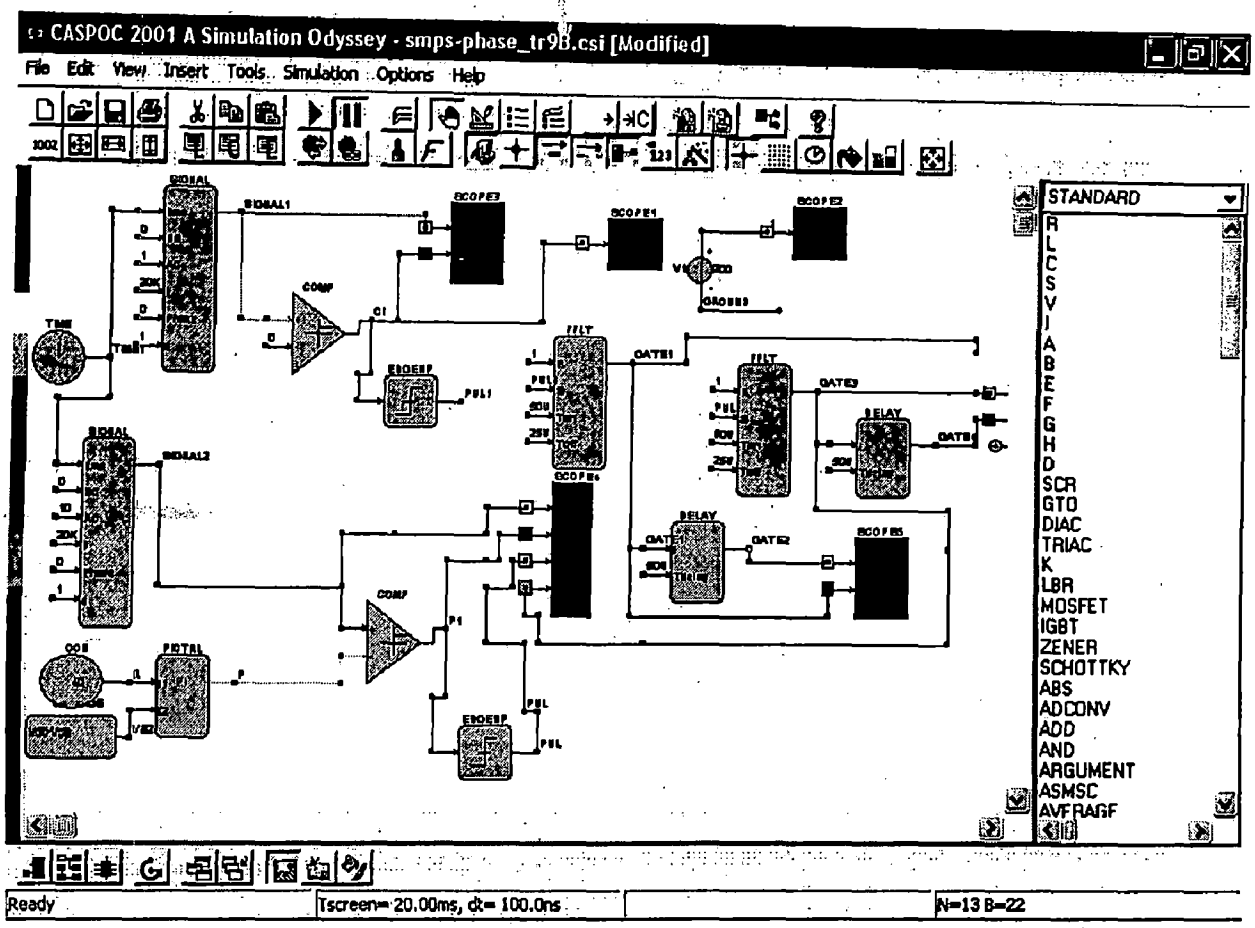


Fig.4.3(d): Control Circuit

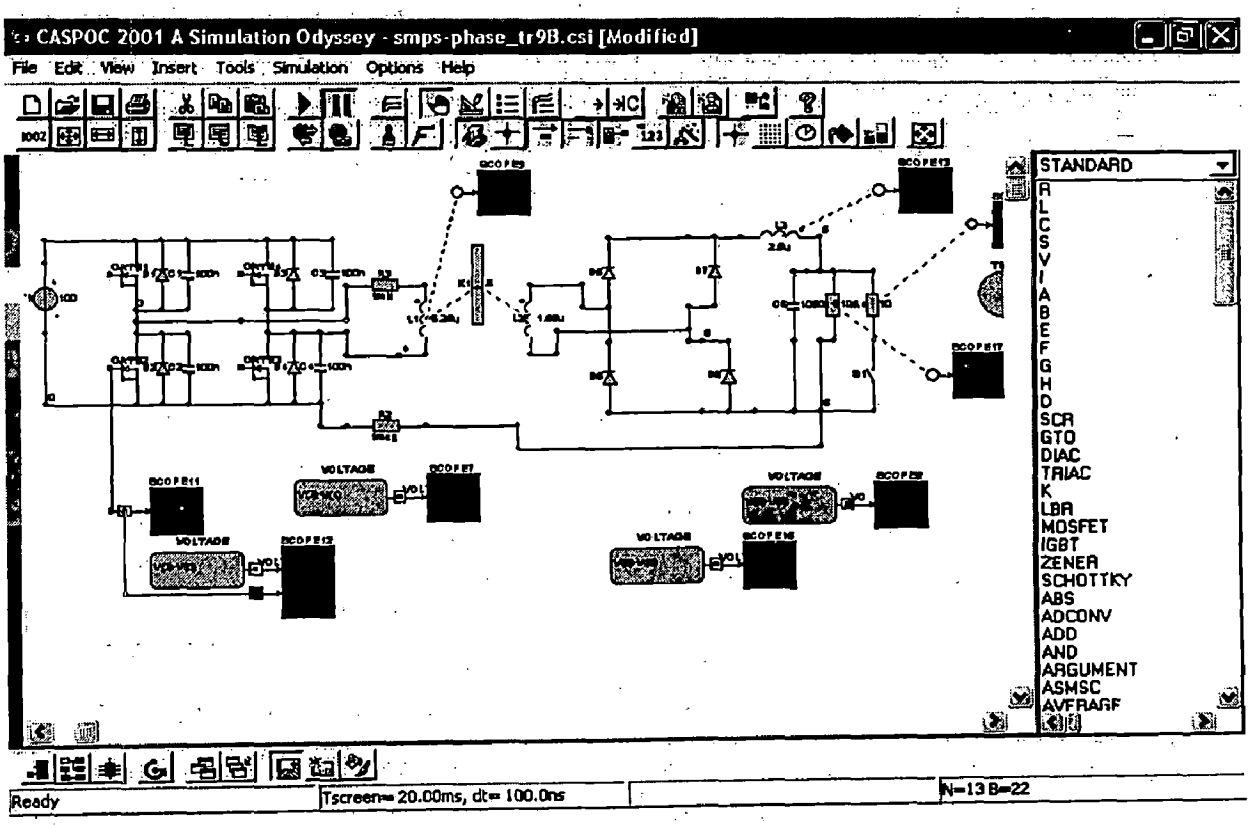


Fig.4.3(e): Power Circuit

4.1.3 Advantages and Disadvantages

Due to its advantageous characteristics, the full-bridge, zero voltage-switched, phase-shifted converter has been one of the preferred topologies for DC-DC conversion, to be used in power applications under a few hundred watts and with high input voltage.

The main advantages of the FB-ZVS-PS converter are:

- high efficiency due to zero-voltage-switching
- constant frequency operation, allowing a simple control, similar to the hard-switched PWM full-bridge converter.

The main disadvantage of the conventional FB-ZVS-PS converter is

- the load dependence of the ZVS condition that is lost for light loads. Therefore, almost every application needs a large commutating inductor in series with the power transformer to obtain ZVS in a wide range of loads. This large inductor, not only produces unacceptably high conduction losses when the load is high, but also prevents slower changes of primary current polarity, which are responsible for a decrease in the effective duty-cycle.
- It has somewhat higher rms current than the conventional full-bridge PWM converter.
- Loss of duty cycle due to the finite slope of the rising and falling edges of the primary current.
- Circulation energy is large.

4.3 ZVS Full Bridge with Secondary Phase Shifted Topology [F]

The main difference between earlier topology and this topology is that the phase shift is provided in the rectifier section instead of the Inverter section, hence two active switches are used in the secondary of the transformer, and the phase shift the input bridge generates square-waves. The leg with two active switches at the output bridge is phase shifted from the input bridge. ZVS for these switches can be achieved in the whole load range. Due to the influence of inductor Lk, the reverse recovery currents of diodes in the rectifier are reduced dramatically.

The inclusion of secondary-side switching achieves:

i) a load independent ZVS range by utilizing the energy stored in the isolation transformer's magnetizing inductance.

ii) This secondary-side switching concept is used to control of the output bus voltage, resulting in a considerable simplification in the methods used to maintain control and isolation of the DC bus.

iii) Furthermore, the maximum reverse recovery voltage will not exceed the output voltage.

4.3.1 CIRCUIT DESCRIPTION

A novel ZVS DC/DC Converter is proposed for high power application with simply two active switches adopted to the secondary side is shown in Fig. 4.4. Phase shift PWM is used as the control technique to regulate the output voltage.

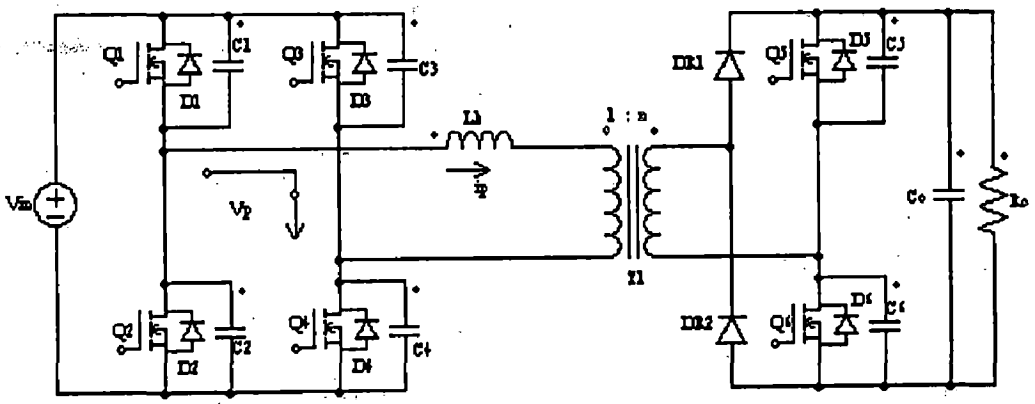


Figure- 4.4 – Novel ZVS Full Bridge DC/DC Converter [F]

Various features of this topology includes-

i) The switch operates with Zero voltage switching.

ii) Phase- shift control strategy is used.

iii) Two active switches are adopted at the secondary side as synchronous rectifiers to improve efficiency. The input bridge generates square-waves and the leg with active switches at the output bridge is phase shifted from the input bridge.

iv) The high frequency transformer provides the step-down function and then the output is rectified to give the DC output.

v) Since the entire control is electronic the response is quite fast and there is no problem of mechanical wear and tear. The transformer operates at high frequency so the size and weight of the transformer gets reduced.

The topology of Novel ZVS Phase-shifted PWM DC/DC converter consists of :

Rectifier module: This is used to obtain a DC voltage from the main power supply.

Single Phase Inverter : It consists of MOSFETs (Q_1 - Q_4) connected in full-bridge configuration for getting high power output. These switches are operated at high frequency and are controlled by the control circuit.

High Frequency Transformer : It is used to provide both isolation and required voltage level conversion.

The resonant loop : It is composed by the parasitical capacitor of the switches , leakage inductor and the magnetizing inductor of the Transformer to realize ZVS under all load conditions.

Secondary Rectifier Section : It consists of two active switches (Q_5& Q_6), control pulses to these swithes are phase shifted and whose are controlled by the control circuit.

4.3.2 CASPOC SIMULATION

The simulation result of this topology are performed in the CASPOC to know about the performance of converter, the results are shown if figure-4.5.

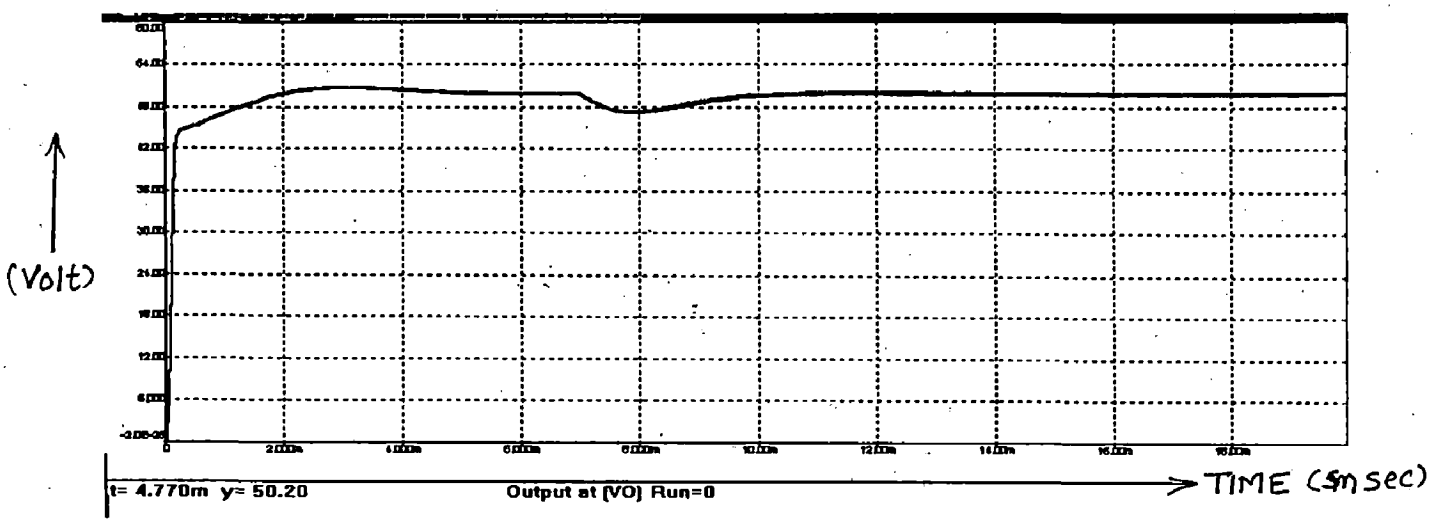


Fig.-4.5(a): Output Voltage of the converter with step change in the load at 5 msec.

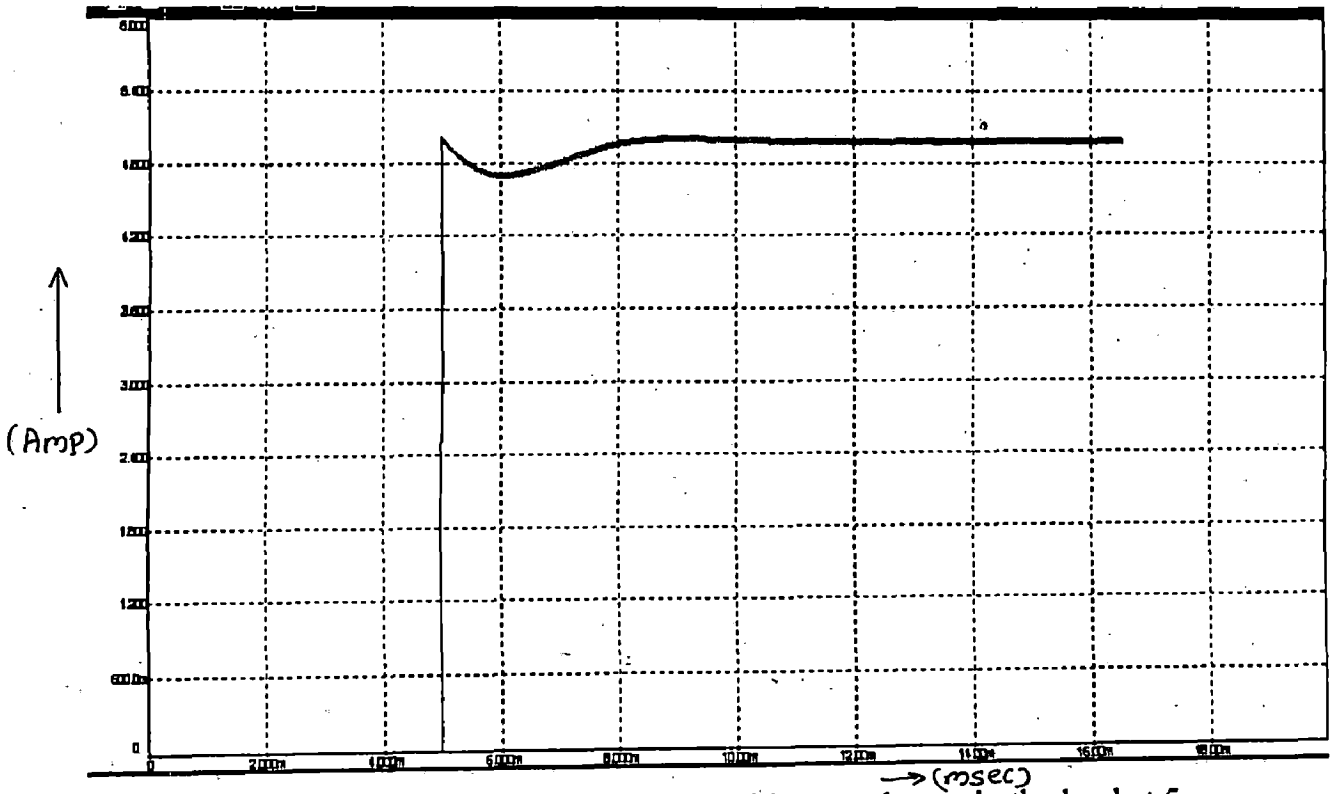


Fig.- 4.5(b)- Load Current with step change in the load at 5 msec

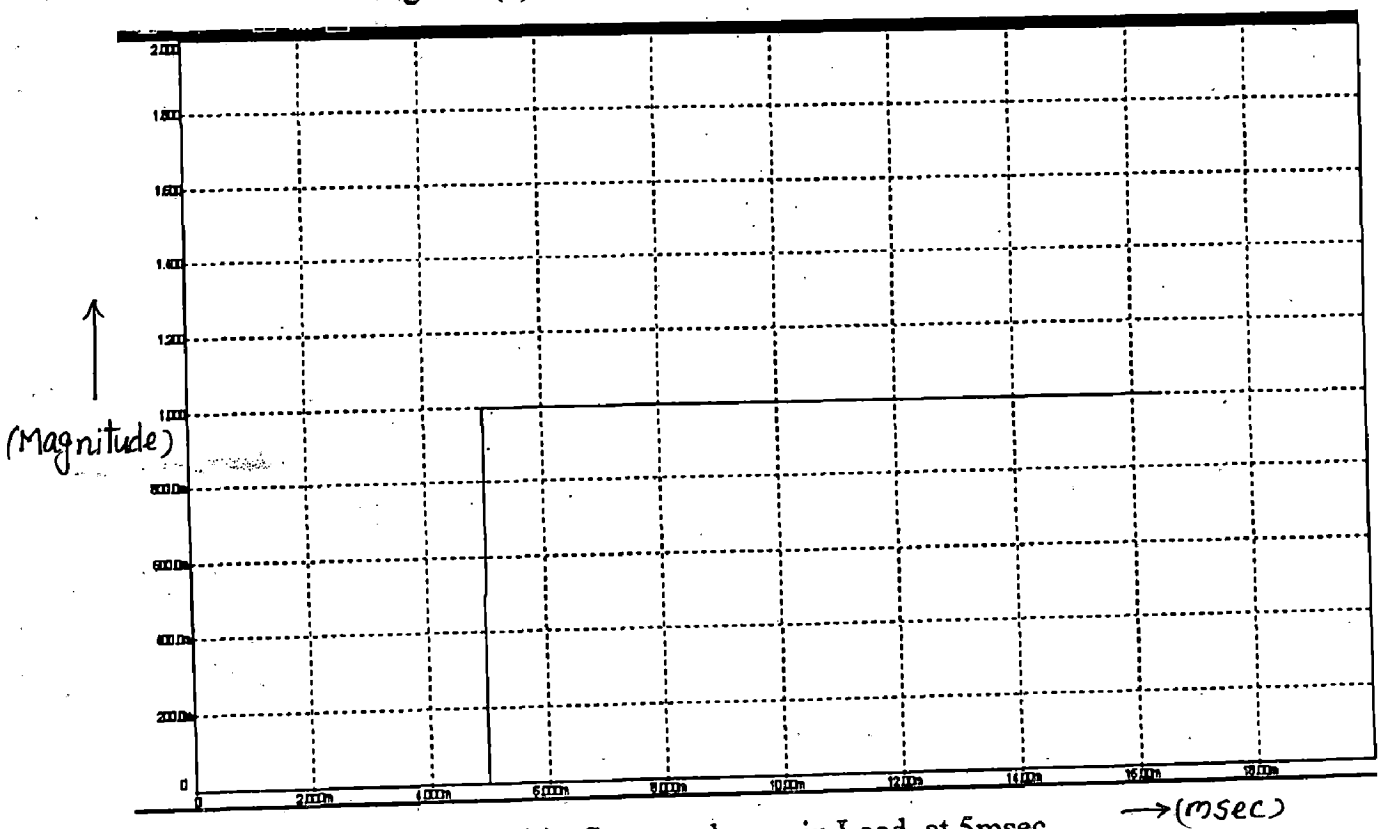


Fig. – 4.5 (c) : Step up change in Load at 5msec

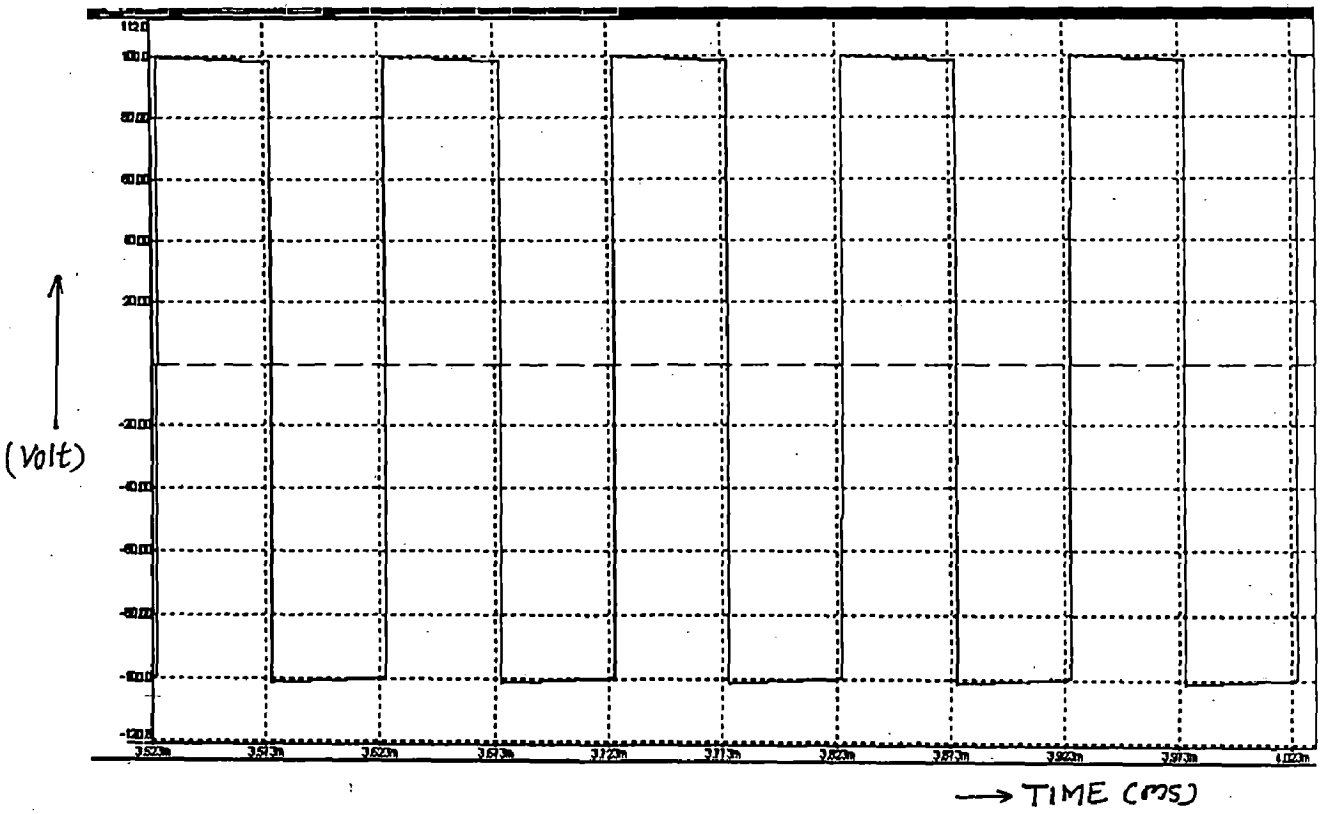


Fig-4.5(d): Inverter output voltage

4.3.3 Advantages and Disadvantages

The advantages and disadvantages of the this topology are as follows:

Advantages:

i) Due to the soft-switching of all switches helps in reducing the switching losses, the improved reliability due to reduced stress, reduced losses in passive components

ii) Reduction of weight and volume of the components resulting from the higher switching frequency

iii) A higher bandwidth resulting from the high internal switching frequency

iv) Integration of parasitic elements in the commutation mechanism (e.g. leakage inductance of the transformer in the resonant circuit)

v) It can reduce circulating currents. Hence, the total conduction power losses and switching power losses of the proposed phase shift PWM soft-switching DC–DC power converter treated here were effectively lowered in comparison

with those of the previously developed transformer primary side controlled phase-shift PWM soft-switching DC–DC converter.

vi) It was noted that the presented voltage source type soft-switching DC–DC converter can completely achieve soft-commutation operation of all the active switches from light load to full load.

In this chapter, the topology for the full-bridge ZVS PWM Phase-shifted secondary dc/dc converter has been selected and the reasons for selecting the topology has been mentioned. Simulation in CASPOC for both the topology is being performed in this chapter and an overview of circuit performance is analyzed in both the conditions. In the next chapters modeling of the system will be done and the performance of the given system will be investigated.

CHAPTER-5

MODELING OF ZVS DC/DC CONVERTER

In this chapter, the modeling of the novel zero voltage switching secondary phase-shifted dc/dc converter will be presented. The modeling has been split into various parts where first the models of the different subsystems (unregulated rectifier, high frequency inverter, phase shifted secondary side active rectifier , PI controller) will be presented and then overall integrated model of the topology will be presented. The state space equation will be determined on the basis of equivalent circuit in each mode, then average state space equation and AC and DC model will be obtained. Small signal analysis will be done considering small perturbation in the system.

5.1 Modeling of Unregulated Rectifier

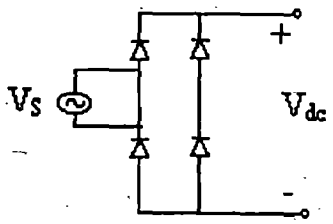


Fig. 5.1 – Full- Bridge Diode Rectifier

Single phase ac supply is given to the rectifier module. This module is a full bridge diode rectifier. Input ac voltage Vs is rectified and the output is V_{dc}. Where voltage Vs is

$$Vs = Vm \sin \omega t$$

The output voltage equation is

$$V_{dc} = \frac{2\,V_m}{\pi}$$

5.2 Operation of the High Frequency Inverter and Phase- shifted secondary active Rectifier :

A voltage fed full bridge is adopted at the primary side and a full bridge type rectifier with two active switches is used in the secondary side. C1-C6 are snubber capacitors including related internal output capacitance of the power switches. D1-D6 are anti-paralleled body diodes of the power MOSFETs. The inductor is serially connected with the transformer T1, whose inductance includes the leakage inductance of the transformer T1. DR1-DR2 are output rectifier diodes.

The input bridge generates square-waves. The leg with two active switches at the output bridge is phase shifted (ϕ) from the input bridge. ZVS for these switches can be achieved in the whole load range.

Following assumptions are taken for the analysis of the circuit are-

i) all the components used in this converter have ideal characteristics:

ii) the snubber capacitors are negligible;

iii) the magnetizing inductance of the transformer is infinite;

iv) the capacity of the output filter capacitors is sufficiently large so that the output voltage can be considered as an ideal dc voltage source.

There are six operating modes during a single steady state switching cycle [13]. The operation waveform and the equivalent circuits of each mode are shown in fig.5.2. These details are already been discussed in [13], for continuity of analysis they are reproduced here.

a) CCM Mode1 [t0-t1]-

Before this mode, Q_2, Q_3, Q_5 and DR_2 are conducting. The input power is delivered to the output. At t_0, Q_2 and Q_3 are turned off and Q_1 and Q_4 are turned on at ZVS condition. The inductor current increases linearly. The inductor current i_P in this mode is given by

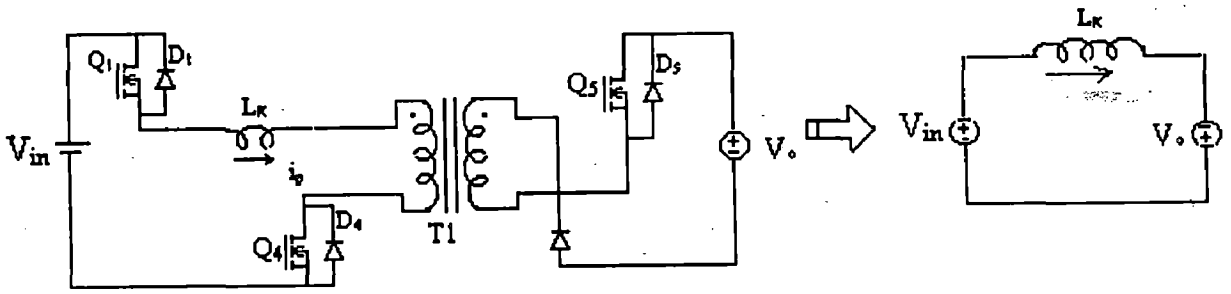


Fig. 5.2 (a) -Mode 1 (When Q_1 & Q_4 conducts)

$$i_p(t) = i_p(t_0) + \text{Vin } (1+\text{d}) . \frac{(t-t_0)}{L_k} \quad (5.1)$$

where d is defined as the conversion ratio,

$$\text{d} = V_o / \text{ n. } V_{in}$$

(b) CCM Mode2 [t1 -t2] and DCM Mode1 [t1 -t2]:

When i_P reaches zero, DR_2 and DR_1 commutate naturally, so that the soft commutation of the diodes is achieved. As Q_5 still turns on, the secondary side of the transformer is shorted through Q_5 and DR_1 , as shown in Fig.- 5.2(b), the input voltage directly applied on inductor L_k, and i_P increases linearly. The energy is stored in the inductor L_k, and the current i_P can be expressed as

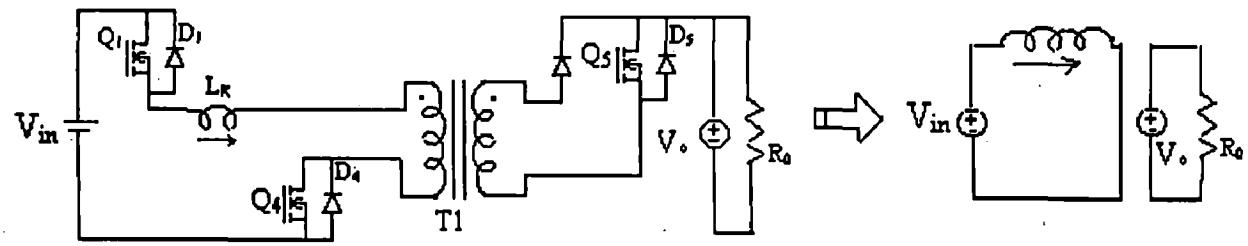


Fig. 5.2 (b) -Mode 2

$$i_p(t) = i_p(t_1) + \text{Vin } . \frac{(t-t_1)}{L_k} \quad (5.2)$$

(c) CCM Mode2 [t2 -t3] and DCM Mode2 [t2 -t3]:

At t_2, Q_5 turns off and Q_6 turns on at ZVS condition. The input power is delivered to the output via inductor L_k. Current i_p is given as

$$i_p(t) = i_p(t_2) + \text{Vin}\ (1-\text{d}).\ \frac{(t-t_2)}{L_k} \qquad (5.3)$$

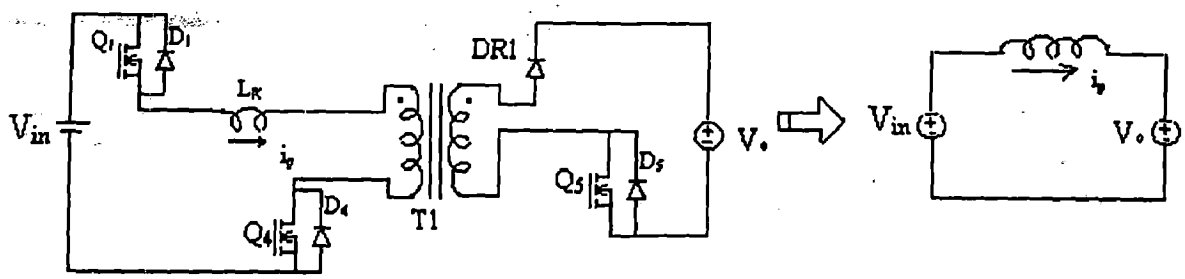


Fig. 5.2 (c) -Mode 3

(d) DCM Mode3 [t3 -t4]:

In this mode, though Q_1, Q_4 and Q_6 still turn on, there is no power delivered from input to the output, the equivalent circuit is shown in Fig.-5.2(d). This is an idle mode. The load is powered by the output capacitors.

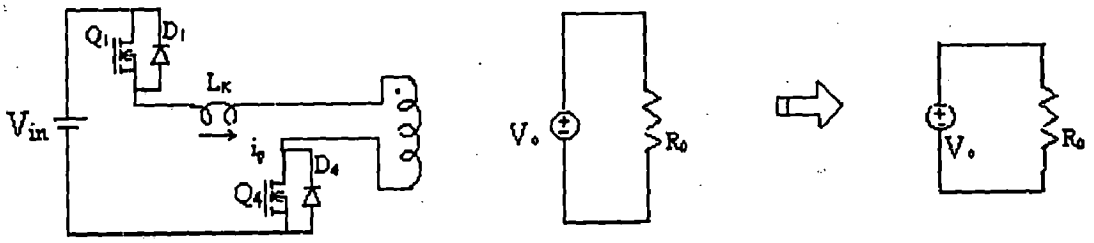


Fig. 5.2 (d) –DCM Mode 3

In this mode no power is delivered from input to output.

The operation modes during the next half switching cycle are the same as those described above.

➢ Output Characteristics

The phase shift between the input bridge and the output bridge is ϕ and the phase lag between the input bridge and the diode leg in secondary side is β which depended on the load condition and output voltage, at the end of half cycle the relationship of inductor current i_P is given by,

$$i_P(0) = -i_P(\pi)$$
$$i_p(\beta) = 0 \qquad (5.4)$$

In order to simplify the expression, all the quantities have been normalized to the following base:

Voltage base: $V_b = V_{in}$

Current base: $I_b = \dfrac{V_{in}}{\omega_s \cdot L_K}$

Power base: $P_b = \dfrac{V_{in}^2}{\omega_s \cdot L_K}$

where ω_S is the switching frequency in radians per second.

We can further discuss this topology under three operation conditions according to the dc conversion ratio d.

(a) d<1: Buck mode

The converter always operates in CCM mode [13]. In heavy load condition, the phase shift angle ϕ is larger than β. The current equation at the various interval can be written as:

We can rewrite (5.1)- (5.3) as

$$i_P(\theta) = i_P(0) + (1+d).I_b.\theta \qquad 0 \le \theta \le \beta$$
$$i_P(\theta) = i_P(\beta) + I_b.(\theta - \beta) \qquad \beta \le \theta \le \phi \qquad (5.5)$$
$$i_P(\theta) = i_P(\phi) + (1-d).I_b.(\theta - \phi) \qquad \phi \le \theta \le \pi$$

From (5.4) and (5.5), we can get the identity for the current

$i_P(\pi) = -i_P(0) = (1+d).I_b.\beta$,

$$i_P(\phi) = I_b.(\phi - \beta) \tag{5.6}$$

and phase shift angle can be represented as

$$\beta = \frac{[(1-d)\cdot\pi + d\cdot\phi]}{(2+d)} \tag{5.7}$$

Based on the previous analysis, the average current drawn from the input voltage source is

$$I_{in}(av) = \frac{i_P(0)\cdot\beta}{2\cdot\pi} + \frac{i_P(\phi)\cdot(\phi-\beta)}{2\cdot\pi} + \frac{[i_P(\pi)+i_P(\phi)]\cdot(\pi-\phi)}{2\cdot\pi} \tag{5.8}$$

Assuming the input power is fully delivered to the output, at an ideal condition, using equations (5.6)-(5.8), we get the expression for the power as,

$$P_O = V_{in}\cdot I_{in(av)} = \frac{d\cdot P_b}{2\cdot(2+d)^2}\cdot f(\phi) \tag{5.9}$$

Where $f(\phi) = \pi.(1+d-2.d^2)+4.\phi.(1+d+d^2)-2.(2+2.d+d^2).\phi^2/\pi$

In light load condition, the phase shift angle ϕ is smaller than β. The current equation at the various interval can be written as:

$$\begin{aligned} i_P(\theta) &= i_P(0) + (1+d).I_b.\theta && 0 \le \theta \le \phi \\ i_P(\theta) &= i_P(\phi) + I_b.(\theta-\phi) && \phi \le \theta \le \beta \\ i_P(\theta) &= i_P(\beta) + (1-d).I_b.(\theta-\beta) && \beta \le \theta \le \pi \end{aligned} \tag{5.10}$$

From (5.4) and (5.10), the current expression is given as,

$i_P(\pi) = -i_P(0) = (1-d).I_b.(\pi-\beta)$,

$$i_P(\phi) = I_b.(\phi - \beta) \tag{5.11}$$

and phase-shift angle is given by

$$\beta = \frac{[(1-d)\cdot\pi - d\cdot\phi]}{(2-d)} \tag{5.12}$$

The average current drawn from the input voltage source will be calculated by multiplying magnitude of the current at each interval with duration of interval and then dividing by the whole period.

$$I_{in}(av) = \frac{i_P(\pi)\cdot(\pi-\beta)}{2\cdot\pi} + \frac{i_P(\phi)\cdot(\beta-\phi)}{2\cdot\pi} + \frac{[i_P(0)+i_P(\phi)]\cdot\phi}{2\cdot\pi} \tag{5.13}$$

Assuming the input power is fully delivered to the output, at an ideal condition, using equations (5.11)-(5.13), we get

$$P_O = V_{in}\cdot I_{in(av)} = \frac{d\cdot P_b}{2\cdot(2-d)^2}\cdot f(\phi) \tag{5.14}$$

Where $f(\phi) = (\pi + 4.\phi).(1-d) + 2.(-2 + 2.d - d^2).\phi^2/\pi$

The critical phase shift angle ϕ can be derived simply using (5.7) - (5.12) and is given in (5.15).

$$\phi_{min1} = (1-d).\frac{\pi}{2} \tag{5.15}$$

The output power versus ϕ is shown in Fig. 5. In conclusion, in $d < 1$ conditions, if, $\phi \geq \phi_{min1}$ the output power can be calculated by (5.9); else, the output power can be calculated by (5.14).

➢ *Soft Switching Operation [13]*

(a) ZVS for input bridge switches

At t_0 shown in Fig. 5.2(a), the voltage across the switch Q_2 is given as

$$u_{c2} = \frac{V_{in}}{2}(1-\cos(\omega_r \cdot t)) - \frac{i_p(0)}{2} \cdot Z_0 \cdot \sin(\omega_r \cdot t) \qquad (5.16)$$

Where $i_P(0)$ is the primary side inductor current at t_0 and

$$\omega_r = \frac{1}{\sqrt{L_m \cdot C}}$$

$$Z_0 = \sqrt{\frac{L_m}{C}}$$

The influence of the leakage inductane L_k is neglected due to the fact that inductance $L_{,m}$ is much larger than L_k. If u_{c2} reaches V_{in}, ZVS can be achieved for Q_1 and Q_4.From (5.16), we can see that ZVS condition for the input bridge switches is always satisfied even at no load condition if the dead time between gate drive signals of Q_1, Q_4, and Q_2, Q_3 is long enough.

By simply assuming the magnetizing current as a triangle waveform $i_m(0)$ is estimated as:

$$i_m(0) = \frac{V_{in}}{(4 \cdot L_m \cdot f_S)}$$

where f_S is the switching frequency.

In order to achieve ZVS during the dead time T_d, which is usually rather small compared to the resonant frequency ω_r, we can get $\cos(\omega_r \cdot T_d) \approx 1$ and $\sin(\omega_r \cdot T_d) \approx \omega_r \cdot T_d$. Then, the maximum L_m is simply estimated as

$$L_m = \frac{T_d}{8 \cdot C \cdot f_S} \tag{5.17}$$

the dead time T_d can be derived as

$$T_d \geq \frac{\phi_{min1}}{\omega_S} + \frac{\cos^{-1}(1-d)}{\omega_{r1}}$$

➢ Steady state operation waveform

The gating sequence of different switches of the converter is shown in Fig-5.3. Operation of the converter and the current flowing through the inductor is shown . The phase shift between the input bridge and the output bridge is ϕ and the phase lag between the input bridge and the diode leg in secondary side is β, which depends on the load condition and output voltage.

In steady state, the effective duty ratio D_R of each output diode is determined by

$$D_R = \frac{kV_o}{2V_d}$$

and it is also equal to

$$D_R = \frac{1}{2} - f_S(\pi - \phi) - t_d f_s$$

where t_d is the switching dead time, f_s *is* the switching frequency and ϕ the phase shifted angle expressed as a fraction of one switching cycle.

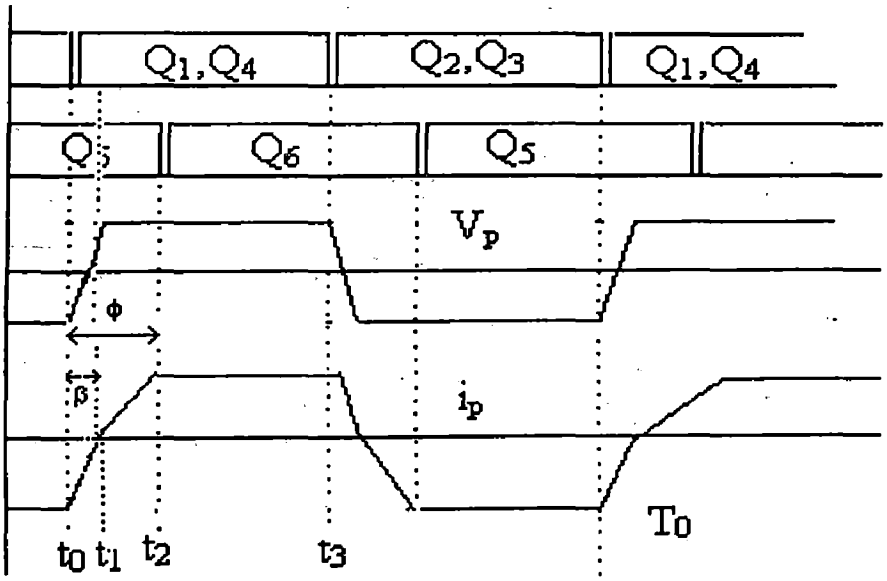


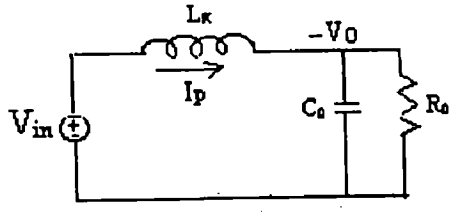
Fig.5.3 – Operation Waveform [13]

Operation waveform for the various mode of the converter is shown in fig. 5.3. It is seen that Q_6 is phase- shifted to that of control pulses of $Q_1 - Q_4$. Some dead time is given so as to get Zero Voltage switching, because in this time the capacitor of the switches going to turn-off starts charging and those switches which are going to turn-on starts discharging.

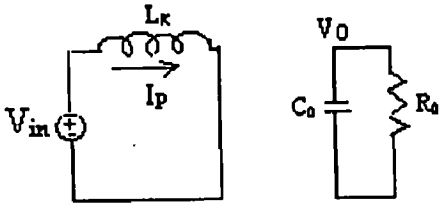
5.3 Modes of operation and the equivalent circuits

As stated previously, the circuit operation seen from the secondary side has three distinct modes when the converter is in CCM. Specifically in these three modes, the output stage sees respectively, (i) a negative input voltage when both Q_1 and Q_4 are ON in the primary side and DR6 and Q_5 are conducting , (ii) Voltage supplied by the filter capacitor when Q_5 still turns on, the secondary side of the transformer is shorted through Q_5 and DR_1, and (iii) a positive input voltage across Ro in the rest of the switching cycle.

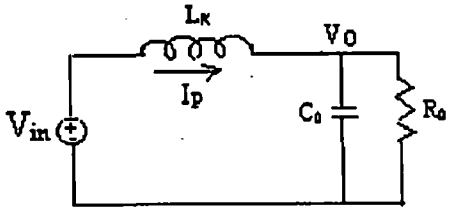
A unity turns ratio k is assumed for convenience in the following discussion initially. The equivalent circuits for different modes are shown in Fig. 5.4



a. CCM Mode 1 [t_0 - t_1]



b) CCM Mode2[$t_1 - t_2$] and DCM Mode1[$t_1 - t_2$]



c) CCM Mode3[$t_2 - t_3$] and DCM Mode2[$t_2 - t_3$]

Fig. 5.4- Equivalent circuits in three different modes each switching cycle.

5.4 State space equations

State space equations are derived on the basis of the equivalent circuit as shown in Fig.-5.4.

A. *Mode I*

In this mode both Q_1 and Q_4 are ON in the primary side and DR6 and Q_5 are conducting in the secondary of the transformer. Hence power is transferred to the load via DR6 and Q_5 .Then network equation for the circuit shown in fig-5.4(a), will be

$$L_k \frac{di_p}{dt} = V_o + V_{in}$$

And

$$C_o \frac{dV_o}{dt} = -i_P + \frac{V_0}{R_0}$$

Thus the state space equations for this mode are obtained as follows:

$$\begin{bmatrix} \frac{di_P}{dt} \\ \frac{dV_O}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{L_K} \\ -\frac{1}{C_O} & \frac{1}{R_O C_O} \end{bmatrix} \cdot \begin{bmatrix} i_P \\ V_O \end{bmatrix} + \begin{bmatrix} \frac{1}{L_K} \\ 0 \end{bmatrix} \cdot V_{in} \tag{5.18}$$

The period of this mode is β.

B- Mode 2

When i_P reaches zero, DR_2 and DR_1 commutate naturally, so that the soft commutation of the diodes is achieved. As Q_5 still turns on, the secondary side of the transformer is shorted through Q_5 and DR_1, as shown in Fig.- 5.4(b), the input voltage directly applied on inductor L_k, and i_P increases linearly. In this period no power is transferred from input to the load.

Thus the state space equations for this mode are defined by

$$\begin{bmatrix} \frac{di_P}{dt} \\ \frac{dV_O}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & \frac{-1}{R_O C_O} \end{bmatrix} \cdot \begin{bmatrix} i_P \\ V_O \end{bmatrix} + \begin{bmatrix} \frac{1}{L_K} \\ 0 \end{bmatrix} \cdot V_{in} \tag{5.19}$$

The period of this mode is $\phi - \beta$.

C. *Mode* **3**

At t_2, Q_5 turns off and Q_6 turns on at ZVS condition. The input power is delivered to the output via inductor L_k.

The state space equations for this mode can be expressed as

$$\begin{bmatrix} \frac{di_P}{dt} \\ \frac{dV_O}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{L_K} \\ \frac{1}{C_O} & \frac{1}{R_O C_O} \end{bmatrix} \cdot \begin{bmatrix} i_P \\ V_O \end{bmatrix} + \begin{bmatrix} \frac{1}{L_K} \\ 0 \end{bmatrix} \cdot V_{in} \tag{5.20}$$

The period of this mode is $\pi - \phi$.

5.4.1 Modeling of PI Controller

The controller transfer function H(s) is chosen to have an integral characteristic at low frequency in order to ensure zero steady-state error is shown in Fig. 5.5. A compensation term is added at higher frequency to provide a satisfactory crossover frequency and stability margin. The crossover frequency of the control frequency since this usually provides an acceptable compromise between speed of response and avoiding switching frequency related instabilities. The V_{EA} is the output of the error detector and then this error is processed in the PI controller and the output is compared with sawtooth waveform to get desired phase-shift ϕ. In the actual design circuit the pulse obtained from the comparator is passed to the D- flip-flop to get the phase-shift.

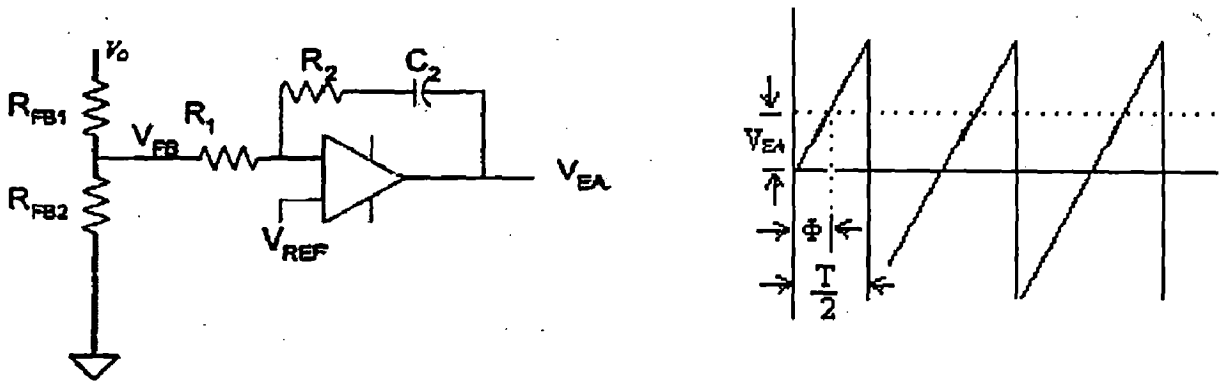


Fig. 5.5- PI Controller and the output of the comparator

The transfer function of the PI controller is given as

$$\frac{V_{EA}}{\phi} = \frac{1}{T/2}$$

$$\phi = \frac{0.5 \cdot V_{EA}}{f} \cdot [\, k_P + k_i \cdot \int dt \,] \qquad (5.21)$$

5.4.2 Averaged state space equations

For each cycle, the averaged state space equations are obtained by weighted summing ofv(5- 18) to (5- 20), i.e. by applying (5- 18).β + (5- 19). $\phi-\beta$+ (5- 20). $\pi-\phi$ (The duration of each interval). This yields:

$$\begin{bmatrix} \frac{di_p}{dt} \\ \frac{dV_o}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \frac{\beta-\pi+\phi}{L_k} \\ \frac{-\beta+\pi-\phi}{C_0} & \frac{-\pi}{R_o \cdot C_0} \end{bmatrix} \begin{bmatrix} i_p \\ V_o \end{bmatrix} + \begin{bmatrix} \frac{\pi}{L_k} \\ 0 \end{bmatrix} . V_{in} \qquad (5\text{-}22)$$

5.4.3 DC and AC models

Under small perturbation steady state condition will be destroyed and the AC components which represents the transient condition will appear in the system. Thus writing each variable into DC and AC components i.e.,

$$\begin{bmatrix} i_p \rightarrow I_p + \tilde{i}_p \\ \phi \rightarrow \phi + \tilde{\phi} \\ V_o \rightarrow V_0 + \tilde{v}_o \\ V_{EA} \rightarrow V_{EA} + \tilde{v}_{EA} \\ V_{in} \rightarrow V_{in} + \tilde{v}_{in} \end{bmatrix} \qquad (5\text{-}23)$$

Substituting the values of (5-23) into equations (5-22) and (5.21), and rearranging the result, it yields:

$$L_k \frac{d\tilde{i}_p}{dt} = (V_o + \tilde{v}_o) \cdot \left(\frac{\beta-\pi+\phi+\tilde{\phi}}{L_k} \right) + \frac{\pi}{L_k} \cdot (V_{in} + \tilde{v}_{in})$$

$$\frac{d\tilde{v}_o}{dt} = (I_p + \tilde{i}_p) \cdot \left(\frac{-\beta+\pi-\phi-\tilde{\phi}}{C_o} \right) - \frac{\pi}{R_o \cdot C_o} \cdot (V_o + \tilde{v}_o) \qquad (5\text{-}24)$$

$$\phi + \tilde{\phi} = \frac{0.5 \cdot V_{EA} + \tilde{v}_{EA}}{f} \cdot [\, k_p + k_i \cdot \int dt \,]$$

$$L_k C_o \frac{d^2\tilde{i}_p}{dt^2} + \tilde{i}_p \cdot (\ -\beta + \pi - \phi\ )^2 = \frac{0.5}{f}[k_P + k_i \cdot \int dt] \cdot \left[C_o V_o \cdot \frac{d\tilde{v}_{EA}}{dt} - I_p \cdot \{\beta - \pi + \phi)\tilde{v}_{EA} \right]$$

$$-\frac{\pi}{R_o} \cdot \{\beta - \pi + \phi)(\tilde{v}_o) + \pi \cdot C_0 \cdot \left(\frac{d\tilde{v}_{in}}{dt} \right)$$

5.4.5 Transfer Function

Taking the Laplace transform of the above equation, and using the following designations,

$$L(\tilde{i}_P) = \hat{i}_p(s), L(\tilde{v}_{EA}) = \hat{v}_{EA}(s), L(\tilde{v}_o) = \hat{v}_o(s)$$

we get :

$$[\ L_k C_o s^2 + (\ -\beta + \pi - \phi\ )^2\ ] \cdot \hat{i}_p(s) = \frac{0.5}{f}[k_P + \frac{k_i}{s}] \cdot [s \cdot C_o V_o - I_p \cdot \{\beta - \pi + \phi)] \cdot \hat{v}_{EA}(s)$$

$$-\frac{\pi}{R_o} \cdot \{\beta - \pi + \phi) \cdot \hat{v}_o(s) + \pi \cdot C_0 \cdot \hat{v}_{in}(s) \qquad (5\text{-}31)$$

Then the transfer function from output of the error voltage amplifier to the output inductor current is given by

$$\frac{\hat{i}_p(s)}{\hat{v}_{EA}(s)} = \frac{[s \cdot C_o V_o - I_p \cdot \{\beta - \pi + \phi)]}{[\ L_k C_o s^2 + (\ -\beta + \pi - \phi\ )^2\ ]} \cdot \frac{0.5}{f}[k_P + \frac{k_i}{s}] \qquad (5\text{-}32)$$

Substituting I_p with $I_p = \frac{V_o}{R_o} \cdot \left(\frac{\pi}{\pi - \beta - \phi} \right)$, and taking turn ratio k into account

Hence $\hat{i}_P(s)$ is replaced with $\hat{i}_L(s)$

$$\frac{\hat{i}_L(s)}{\hat{v}_{EA}(s)} = V_o \cdot \frac{\left[s \cdot C_o + \frac{1}{R_o}\right]}{\left[k^2 L_k C_o s^2 + (-\beta + \pi - \phi)^2\right]} \cdot \frac{0.5}{f}\left[k_P + \frac{k_i}{s}\right] \qquad (5\text{-}33)$$

The output filter has the following transfer function

$$\frac{\hat{v}_o(s)}{\hat{i}_L(s)} = \frac{R_o}{sR_oC_o + 1}$$

Thus the overall Transfer function is given by,

$$\frac{\hat{v}_o(s)}{\hat{v}_{EA}(s)} = V_o \cdot \frac{R_o}{\left[k^2 L_k C_o s^2 + (-\beta + \pi - \phi)^2\right]} \cdot \frac{0.5}{f}\left[k_P + \frac{k_i}{s}\right] \qquad (5\text{-}34)$$

5.5 Control loop

Fig. 5.6 shows the block diagram of a closed loop of the converter.

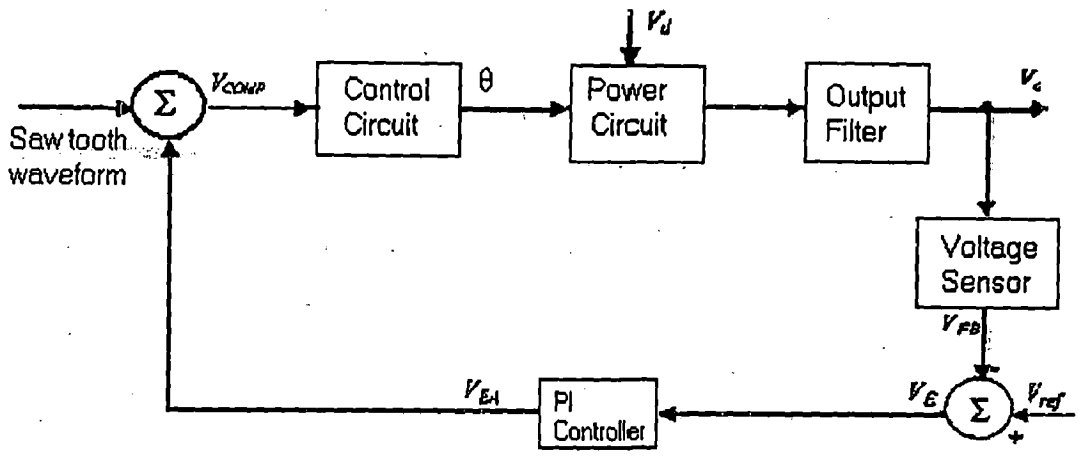


Fig. 5.6- Closed Loop of the Converter

The operating principle of it is as follows:

The voltage sensor senses the output voltage *Vo* and compares the sensed signal with the reference voltage V_{REF} & and this producing the error voltage V_E. Which

processed in the PI controller to produce V_{EA}. It is compared with sawtooth waveform and this signal is used by the control circuit to generate the phase shift in the control pulse. For instance, as soon as the input voltage has a step up changes. Voltage sensor and PI controller command the control circuit to increase the phase shift angle immediately. The increased phase shift angle reduces the effective duty ratio of the switches, cutting off the possible overflow of energy to the output and thus keeping the output voltage at the regulated point. Similarly, as the input voltage steps down, the control circuit directly detects the change and decreases the phase shift angle immediately. This increases the effective duty ratio to regulate the output voltage. In this way, the output regulation against the input voltage variations is fulfilled.

In this chapter modeling of different subsystem i.e. PI controller, output filter, converter has been developed. For this equivalent circuit of the converter in each mode is drawn. On the basis of which, state space equations of the system are derived for each interval. Then subsequently by this DC and AC model of the system has found considering small perturbation by separating out steady state and transient portion. Then small signal analysis of the system is explained and in the last overall Transfer Function of the system has derived with the help of Laplace Transform. The function of closed loop operation is discussed and the dependence of phase angle to the load change is determined. The behaviour of the system is determined by experimental and simulation results of the prototype and presented in Chapter -7 and 9. In the next chapter design calculation of the various parameters will be discussed.

CHAPTER -6

DESIGN OF ZVS DC-DC CONVERTER

In this chapter a design procedure of the various components used for the development of ZVS full bridge phase- shifted dc/dc converter topology for general-purpose applications is presented. As seen from the previous chapters, the selected topology is simply a combination of a conventional full bridge converter, a transformer and a dc blocking capacitor. Because the design for the conventional full bridge converter has already been well addressed in the literature and the design of the transformer will be discussed in the chapter-8. Hence this chapter will only discuss the optimal design calculation of the filter capacitor, dead time, Magnetizing Inductance for the Transformer so as to achieve zero voltage switching for the wide load range. Since resonant loop in this converter is composed by the parasitical capacitance, leakage inductance and the magnetizing inductance of the transformer.

The following specification is used for design calculation:

i) f_s, switching frequency - 10 kHz

ii) Maximum output power - 200 Watt

iii) Input Voltage - 200 Volt

iv) Output Voltage -100 Volt

v) MOSFET switches - IRFP460

vi) Output Capacitance of the MOSFET from Data sheet- 1 nF

On the basis of specification given above of some important design parameters are calculated, which helps in selecting various components e.g. filter capacitor, transformer for hardware development.

6.1. T_d, switching dead time

The Turn-On Delay Time and Rise Time of the IRFP 460 are 35ns and 120 ns respectively. Hence dead time should be greater than the sum of these two i.e. 155ns so that overlapping of the voltage and current rise can be avoided. The dead time taken is 200ns.

6.2 Selection of the Magnetizing Inductance

Magnetizing inductor helps in realizing ZVS using the magnetizing current if the following two conditions are satisfied:

- Dead time is long enough
- The energy stored in the magnetizing inductance is larger than the energy that needs to charge the MOSFET parasitical capacitance.

$$½ * i_m^2 (t_o) (L_{lk} + L_m) \geq 4*1/2\ C*V_{in}^2 \qquad (6.1)$$

Less magnetizing inductance enlarges the magnetizing current, which can help realize ZVS in light load and no load, but leads to larger circulation current and conduction loss, which should be carefully considered in practical design. Thus magnetizing inductance is given by,

$$L_m \leq \frac{T_d}{8 \cdot C \cdot f_S} \qquad (6.2)$$

Where,

T_d ,is the dead-time = 200 ns,

C, is the MOSFET parasitical capacitance = 1nF and

f_S, is the swithing frequency = 10KHz

Hence calculated value of L_m is

$$L_m \leq 0.0025 \text{ Henery}$$

The measured value of the Magnetizing Inductance of the Transformer is 1.9398 mH. It satisfied the design criteria.

6.3 Selection of filter Capacitor

If the ac input frequency is 50 Hz, then the current flowing through the diode rectifier has a 100 Hz component because the shape of the current will be that of a rectified sinusoid. This rectified sinusoidal current can be expressed as a $\sin 2\omega t$

function equivalent to M(1 - cos 2ωt) where M is the average value. The amplitude of the ac component of the current waveform is equal to the dc component

$$I_{chg,pk} = \frac{P_{0,max}}{V_0} \tag{6.3}$$

and it is this current component that must be filtered by the output capacitor. In the case of the proposed converter, this 100 Hz component exists at the output even though the isolation transformer does not pass a 100 Hz component from the primary to the secondary. The 100 Hz component gets reconstructed at the output by the rectifier and is fed to the output capacitor. The amplitude of the peak-to-peak ripple voltage $V_{co,rpp}$ across C_o is

$$V_{co,rpp} = \frac{I_{chg,pk}}{2 \cdot \pi \cdot f_{in} \cdot C_O} \tag{6.4}$$

From equation (6.3) & (6.4), the value of output filter capacitor is given by,

$$C_o \geq \frac{P_{o,max}}{2 \cdot \pi \cdot f_{in} \cdot V_o \cdot V_{co,rpp}} \tag{6.5}$$

Where $P_{o,max}$ is the maximum power output = 200 watt, V_o is the output voltage = 100 volt and let the allowable peak-to-peak voltage ripple $V_{co,rpp}$ = 10%,i.e. 10% of 100 volt is 10volt. and C_o is calculated

$$C_o \geq 636.6\ \mu F$$

The value of the filter capacitor used is 1000 μF.

6.4 Selection of the Diode

For high frequency operation fast recovery diodes are chosen. Based on initial converter simulation results, diode ratings of V_R = 600 V (reverse blocking voltage), and $I_F(AV)$ = 50 A (average forward current) were selected. Other specifications such as forward voltage drop, reverse recovery time and peak reverse recovery current are strongly considered during device selection.

A low diode forward voltage drop (V_F) is important to minimize device power consumption. Also, low reverse recovery time and small peak reverse recovery current were important criteria to reduce reverse conduction and provide the most continuous load current. Here fast recovery diode is having following specifications:

i) Diode forward voltage drop (V_F) = 1.5 V

ii) Reverse recovery time (t_{rr}) = 45 ns

iii) Average forward current = 50A

6.5 Active switch selection

MOSFET is used here as an active switch. The selection of MOSFET is on the basis of the voltage range and current rating. The switch used are IRFP 460. It's a 500 Volt N-Channel MOSFET having in-built anti-parallel diode. Various specifications of its are:

i) Continuous Drain Current = 21 A

ii) Drain-to-Source Breakdown Voltage= 500Volt

iii) Static Drain-to-Source On-State Resistance= 0.27 Ohm

iv) Turn-On Delay Time = 35ns

v) Rise Time= 120 ns

vi) Turn-Off Delay Time= 130ns

vii) Output Capacitance = 1 nF

viii) Diode Forward Voltage =1.8 Volt

In this chapter the design guideline for the various important parameters i.e. calculation of magnetizing inductance, filter capacitances and selection of switches are discussed. Selection of magnetizing Inductance determines the proper soft switching in the converter. On the basis of these selection the Full-bridge dc/dc converter is fabricated. The control circuit design and transformer design will be discussed in detail in the chapter-8.

CHAPTER -7
SIMULATION OF ZVS DC-DC CONVERTERS

The conventional Full-Bridge ZVS Phase-shifted DC/DC converter consists of a single-phase full-bridge high frequency inverter, high frequency transformer and full-bridge diode rectifier. In this phase shift is given in the two leg of the transformer, its operation waveform are already described in chapter –4. The selected Full-Bridge ZVS Phase-shifted DC/DC converter consists of a single-phase full-bridge high frequency inverter, high frequency transformer and full-bridge rectifier with two active switches. In this phase shift is given in the two switches connected in the synchronous rectifier section. In order to theoretically investigate the performance of both Full-Bridge ZVS Phase-shifted DC/DC converters the simulation of both the topology was performed with CASPOC and MATLAB/SIMULINK. The results of CASPOC are already been mentioned in the chapter- 4. The input voltage was taken 100 volt and a resistive output load of 12.5 ohm is used. Transformer is a step down transformer at 100/50 volt. The frequency of operation is taken as 10 KHz. The results for both the topology obtained are compared with experimental results in Chapter-9.

7.1 SIMULATION OF FULL-BRIDGE ZVS PRIMARY PHASE-SHIFTED DC/DC CONVERTER

Simulation results of the Full-Bridge ZVS Primary Phase-shifted DC/DC converter topology are given here under.

- **Simulation Results of Control circuit -**

The control pulses for all the four switches of the Inverter are shown in Figure-7.1. In this pulse given to Q_2 is inverted to the pulse given to Q_1 . But the pulse of switch Q_3 is phase shifted to the pulse of switch Q_2.

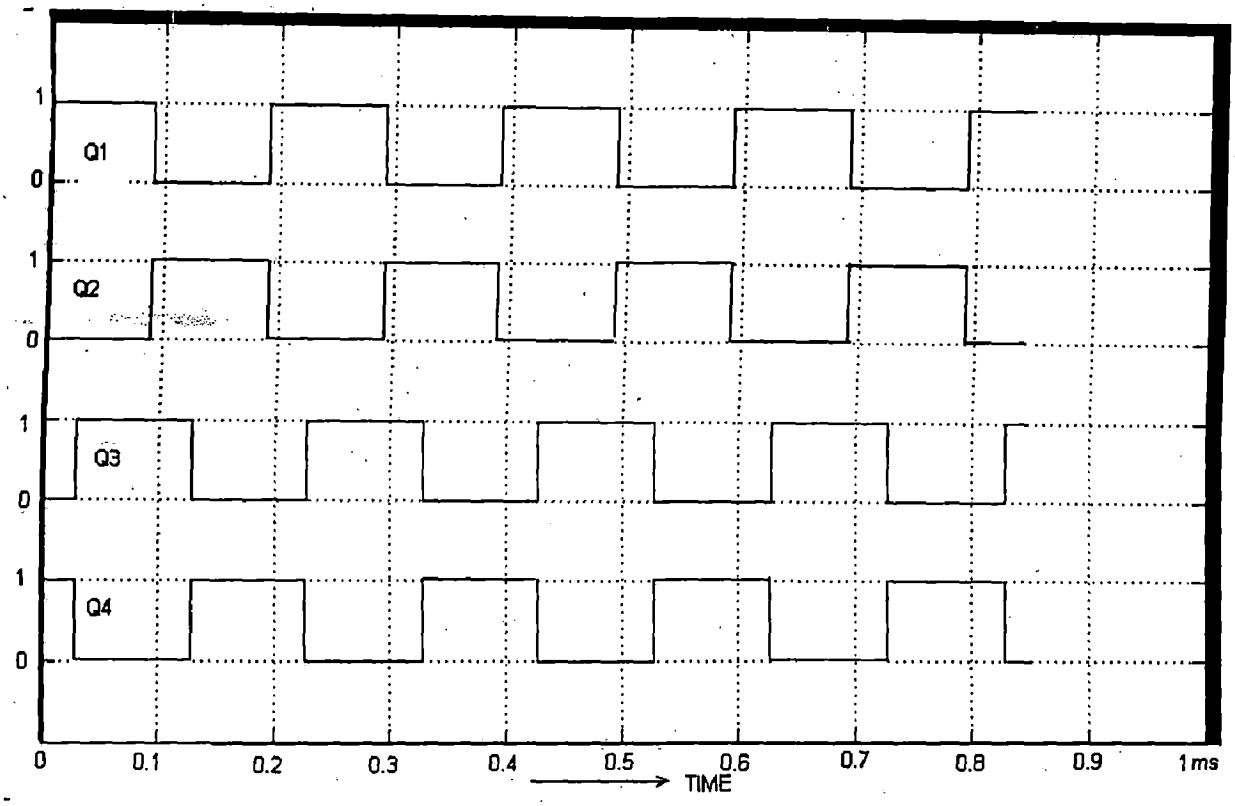
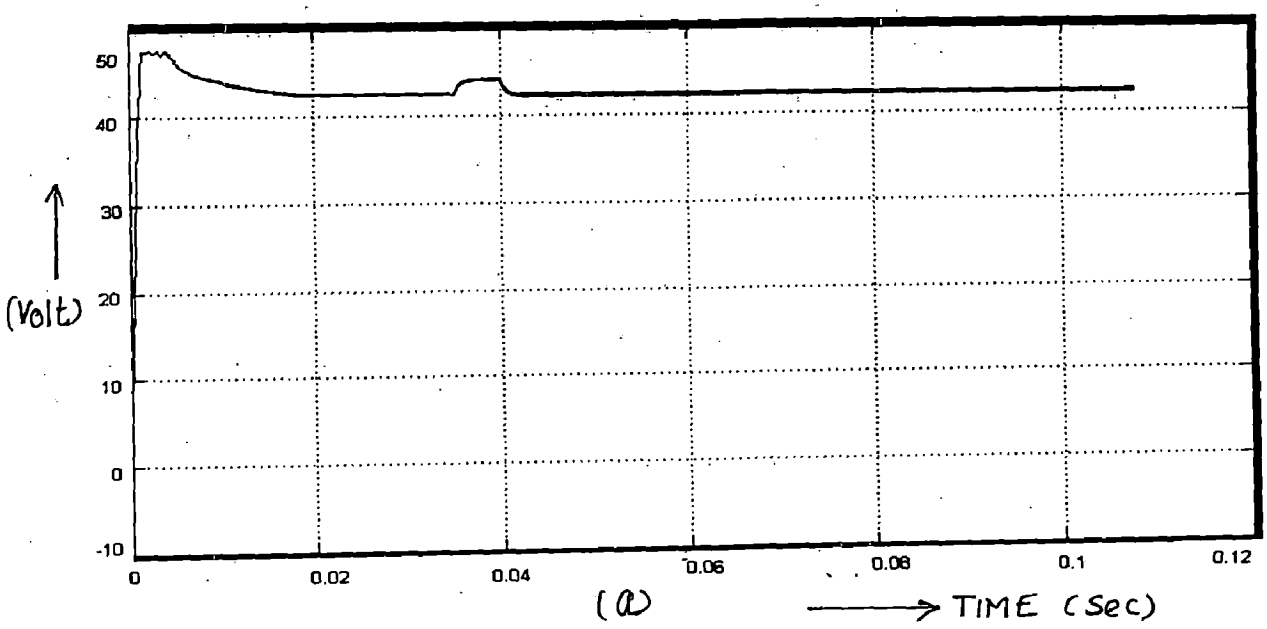


Fig-7.1: Phase –shifted Gate pulses

- **Simulation Results of Power circuit**

  i) Output Voltage and Load Current

The output voltage of the converter is shown in Fig.-7.2. The converter's performance is tested in the case of step up change in the input voltage and step up change in the load. The converter's output voltage and current waveform is studied under both conditions.



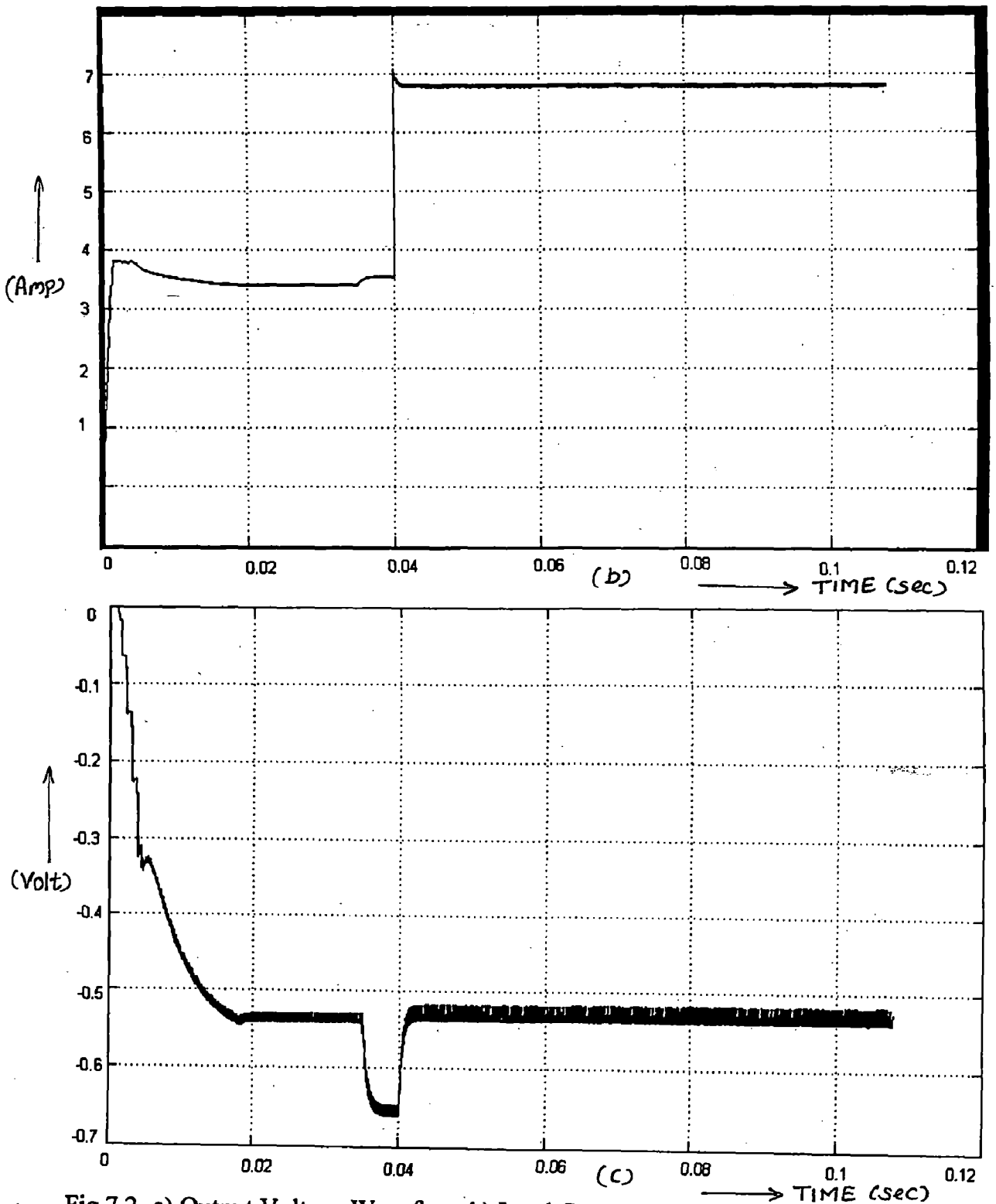


Fig.7.2- a) Output Voltage Waveform b) Load Current c) PI Controller Output with change in Load at 0.04 sec

ii) Voltage and Current At Inverter Output

The DC input given to the Inverter is inverted into high frequency AC square wave. The output current in the Inverter or the current in the primary winding of

the transformer is also shown. These high frequency AC voltage and current at Inverter output is shown in Figure-7.3.

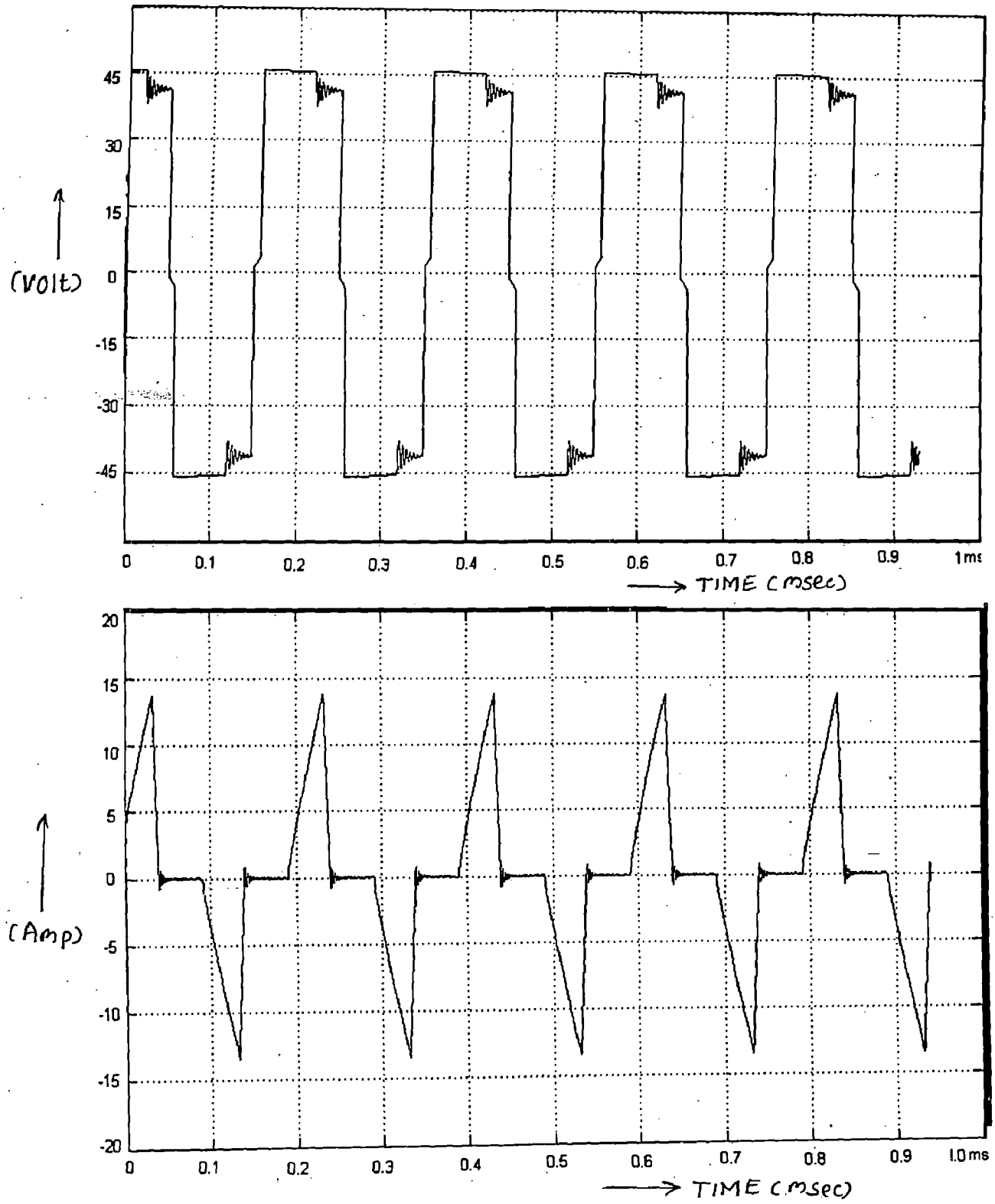


Figure-7.3: Inverter Voltage & Current waveform

7.1 SIMULATION OF FULL-BRIDGE ZVS SECONDARY PHASE-SHIFTED DC/DC CONVERTER TOPOLOGY

Simulation results of the Full-Bridge ZVS Secondary Phase-shifted DC/DC converter topology are given here under.

- **Simulation Results of Control circuit -**

The control pulses for all the four switches of the Inverter and two switches for rectifier are shown in Figure-7.4. In this pulses given to Q_2 -Q_4 is inverted to the pulse given to Q_1 -Q_3 . But the pulse of switch Q_5 is phase shifted to the pulse of switch Q_2.

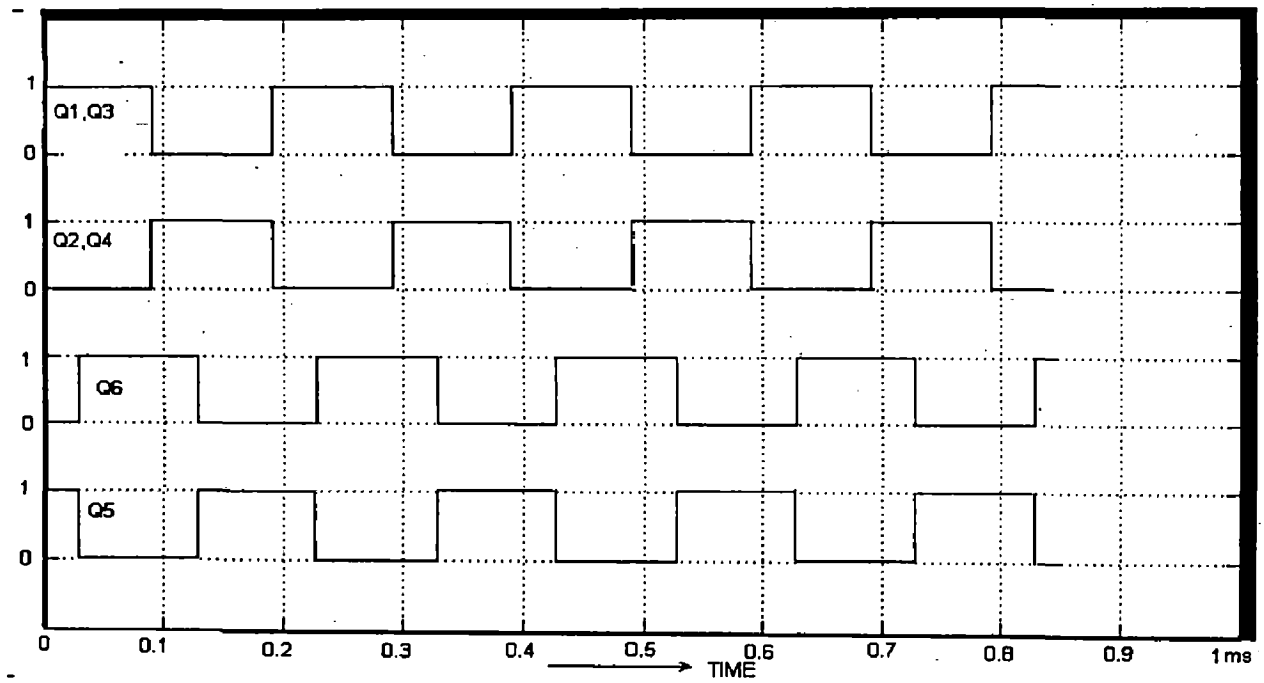


Fig-7.4: Gate pulses for the Switches

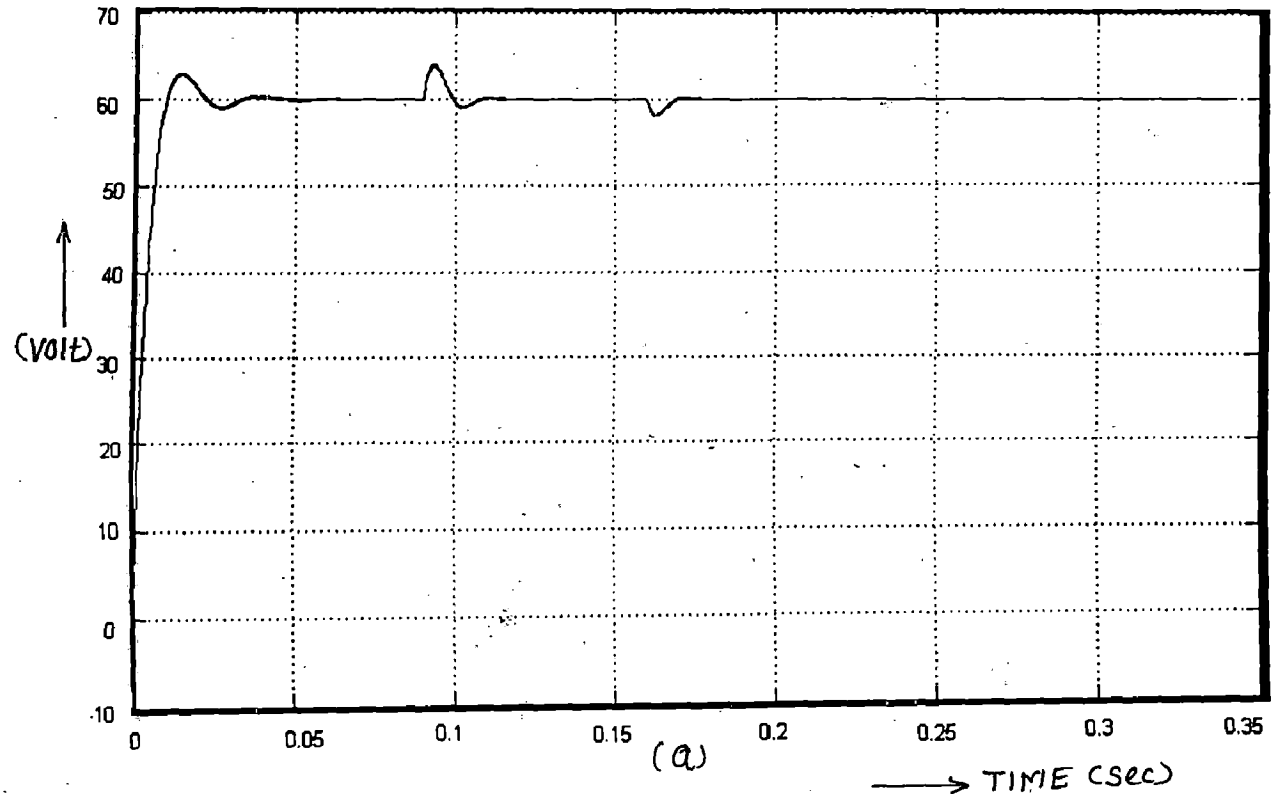
- **Simulation Results of Power circuit**

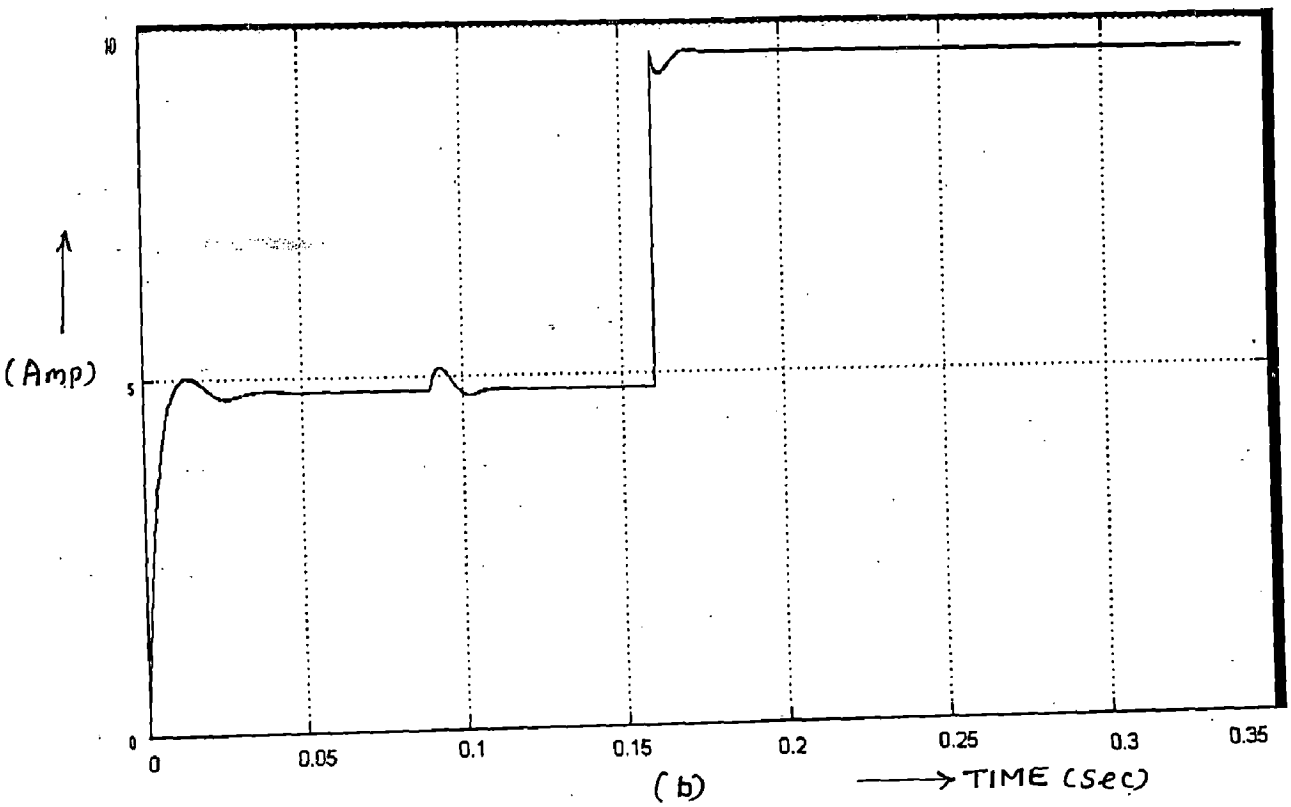
i) Output Voltage and Load Current

The converter's performance is tested in the case :-

- when step up change in the input voltage occurs at 0.1 sec.
- when the load is step up changed at 0.2 sec.

The converter's output voltage and current waveform is studied under both conditions Regulation of output voltage and load current waveform is shown in the figure-7.5.


70
60
50
40
30
20
10
0
-10
(VOLT)
0
0.05
0.1
0.15
0.2
0.25
0.3
0.35
(a)
TIME (sec)


10
5
0
(Amp)
0
0.05
0.1
0.15
0.2
0.25
0.3
0.35
(b)
TIME (sec)

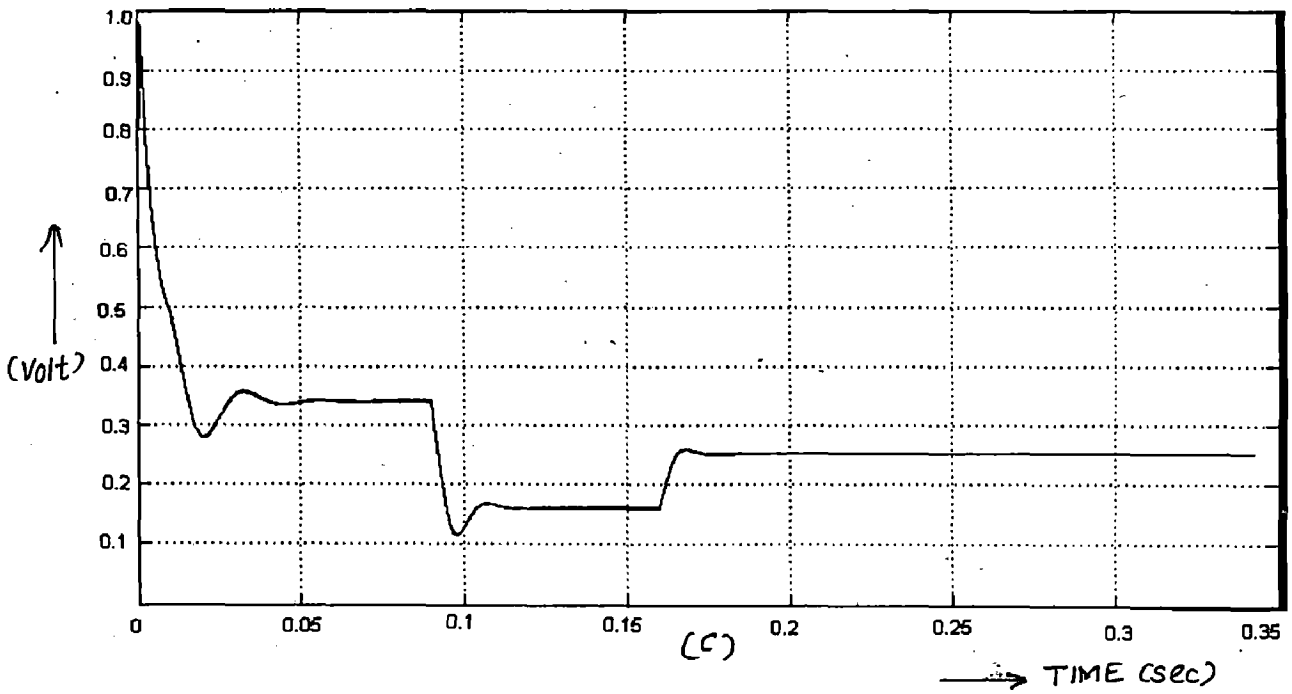
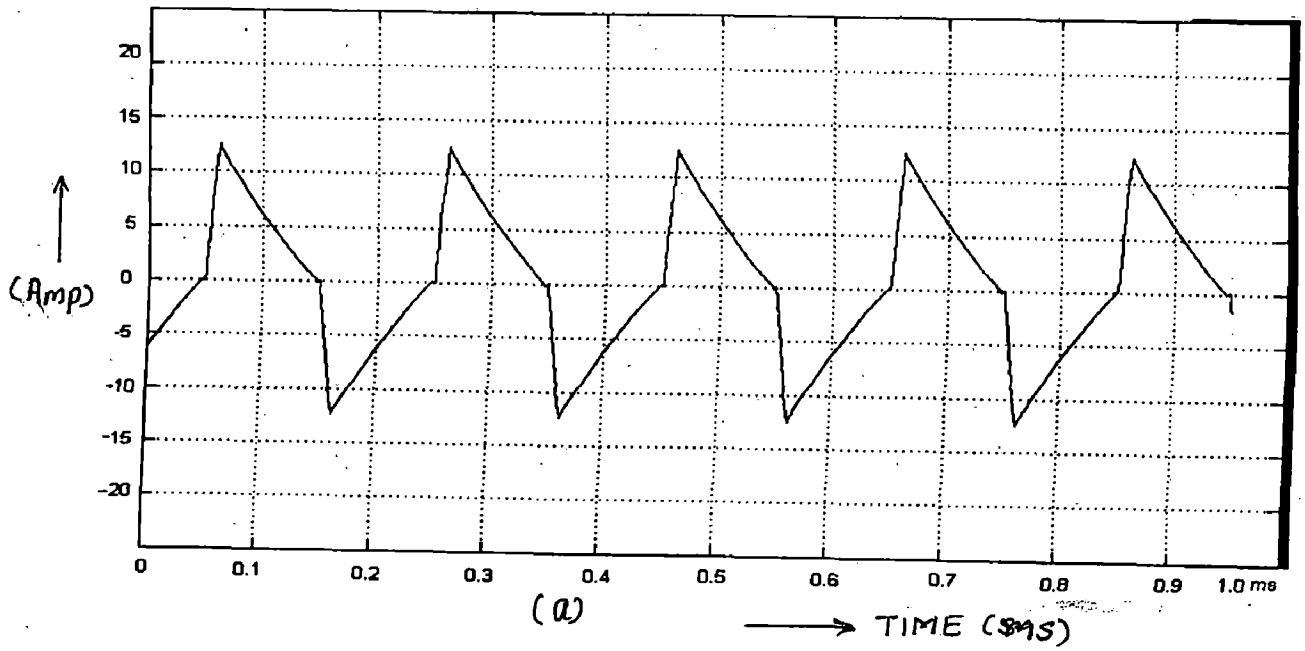


Figure-7.5.: (a) Output voltage (b) Load Current (c) PI Controller output variation. with step up change in input voltage at 0.1sec and with step up change in load at 0.2 sec

ii) Voltage And Current At Inverter Output

The DC input given to the Inverter is inverted into high frequency AC square wave. The output current in the Inverter or the current in the primary winding of the transformer is also shown. Transformer voltage and the current waveform before the change in with the step up change in input voltage and step up change in load and after the change takes place are shown in Fig.7.6 and 7.7 respectively.



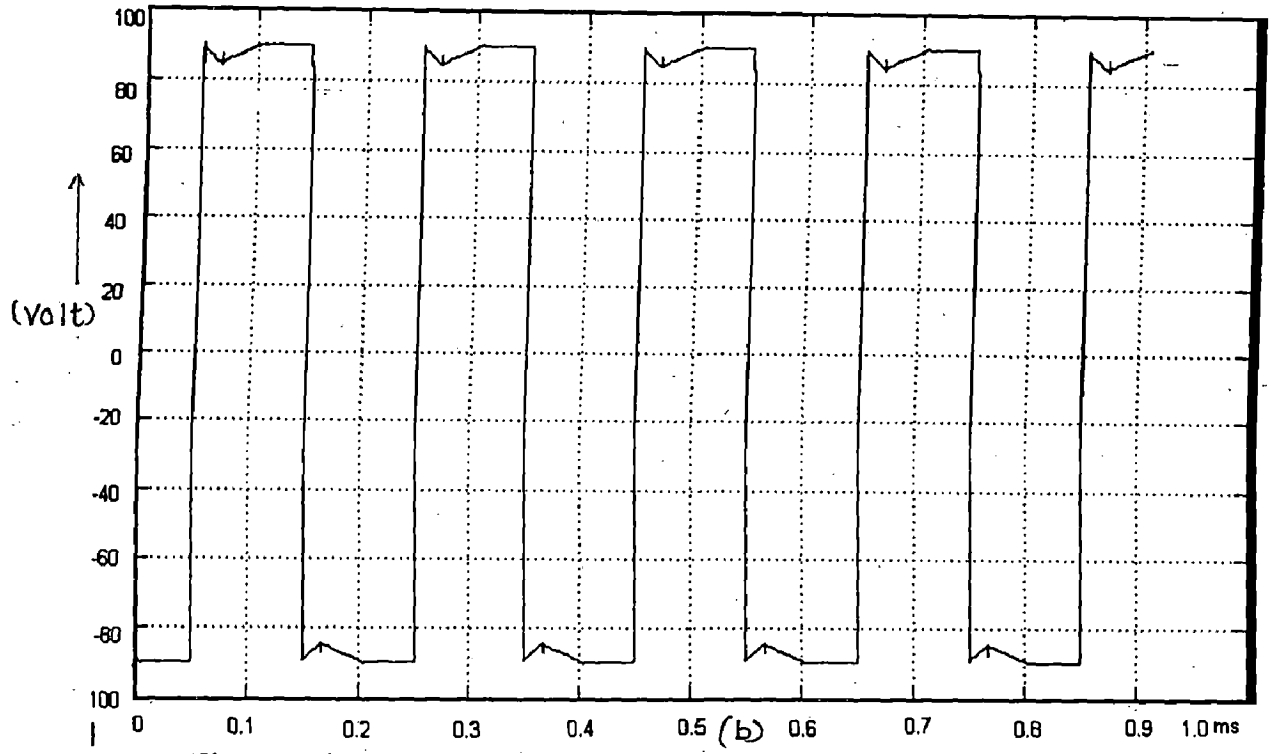
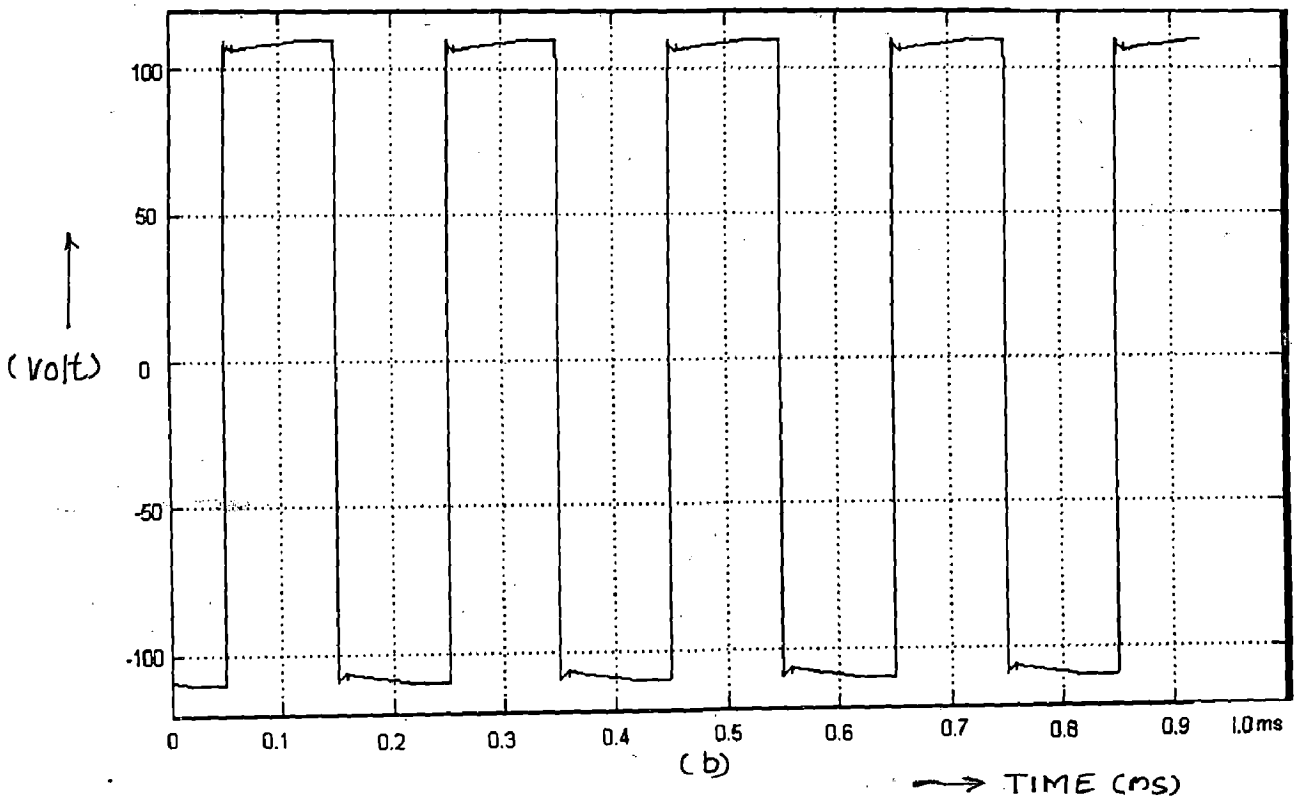


Figure-7.6: (a) Output Current of the Inverter, (b) Output Voltage of the Inverter before the load and voltage change takes place



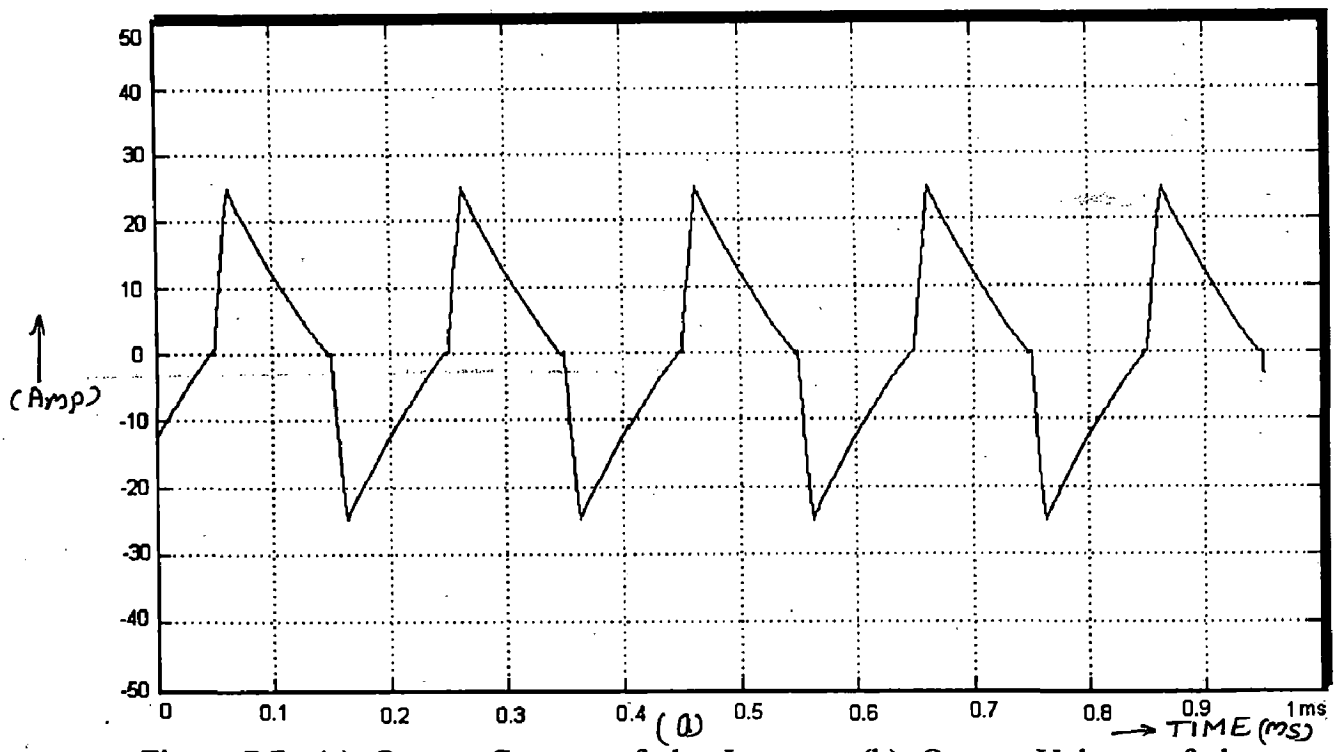


Figure-7.7: (a) Output Current of the Inverter, (b) Output Voltage of the Inverter after the input voltage changes from 100V to 110V and load is step up

It can be seen from the Fig.7.6 and Fig.7.7 that when Input voltage changes from 100V to 110 V Voltage of the Inverter output also varies from $\pm$100 V AC to $\pm$110 V AC. The current in the transformer changes from 12 Amp to around 24 Amp due to change in the load.

iii) Drain To Source Voltage

The drain to source voltage at the switches for each leg is shown in figure-7.8. It is shown from the figure that zero voltage switching is achieved for the switches at both turn-on and turn-off condition.

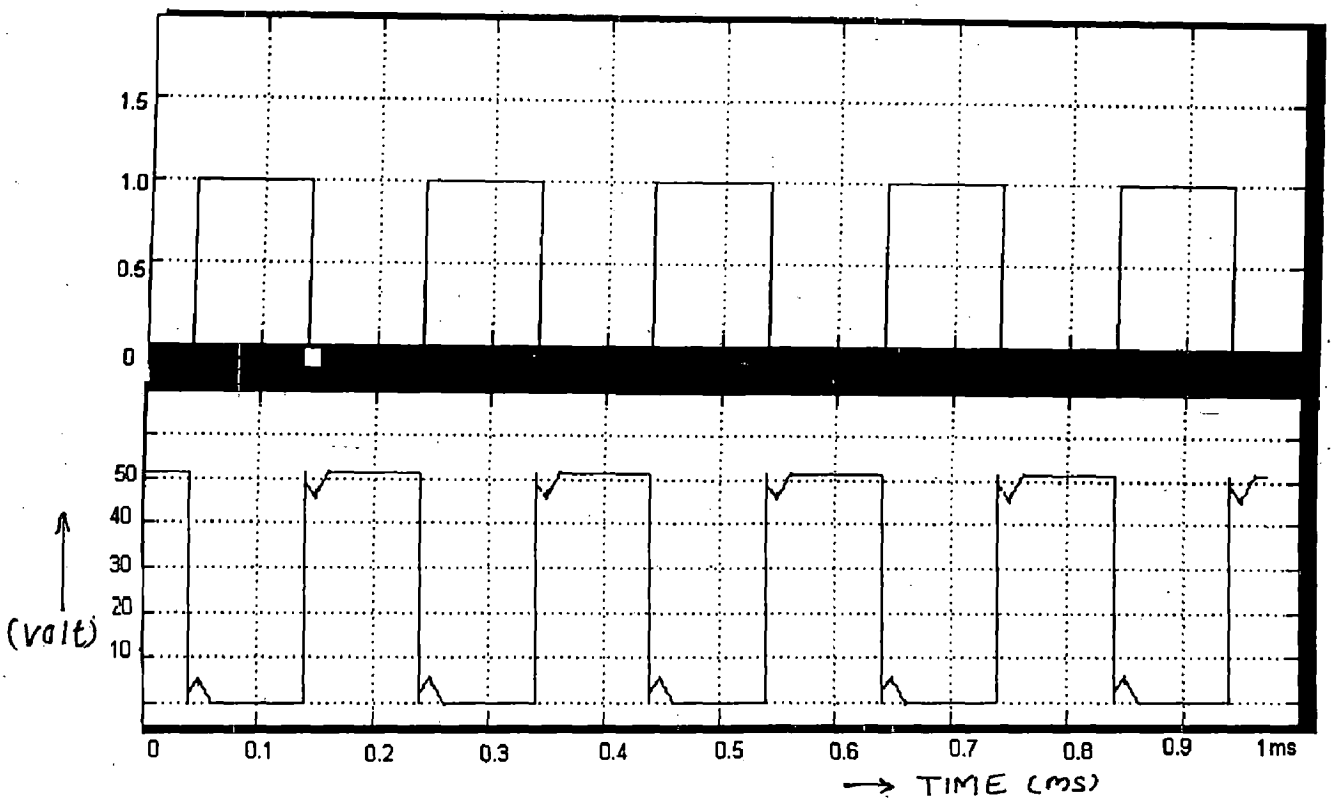


Figure-7.8: Gate pulse and Voltage across Drain to Source of the Switch

In this chapter the simulation results of the Two Full-Bridge ZVS Phase-shifted DC/DC converter topology have been presented in MATLAB. One is Full-Bridge ZVS Primary Phase-shifted DC/DC converter and another is the Full-Bridge ZVS Phase-shifted Secondary DC/DC converter. The simulation result of output voltage with step up change in load and Input voltage is also taken. From the results it is evident that the Zero voltage switching is achieved for all the switches, which will help in reducing switching losses, switching stress on the devices. In the later topology Phase-shifted pulse is given to the synchronous rectifier section this phase- shift depends upon the change in load voltage. Voltage mode control technique is used for the generation of phase-shifted control pulses. These results will be compared with the experimental results in the chapter-9.

CHAPTER- 8

HARDWARE DESIGN

In this chapter, the design of the hardware for the prototype of 200 watt,10 kHz, 100V output DC/DC converter developed is described. The design of control circuit for single-phase inverter and phase-shifted gating control circuit for the synchronous rectifier section is developed. These pulses obtained from the control circuits are amplified through Firing Pulse Amplification & Isolation Circuit. These pulses are then given to the Gates of the switches. The design aspect of the high frequency transformer is also discussed. The design of high frequency transformer has been done using ferrite-core which are quite suitable for high frequency operation and results in low volume and weight of the products. The power supply required for the IC's of the control circuit is fabricated. The current sensor circuit based on the hall-effect current sensor has been used for the current measurement. The design criteria for output filter section and the transformer magnetizing Inductor for achieving zero voltage switching has already been discussed in the chapter-6, is used here for the selection and fabrication of the different circuit.

8.1 Control Circuit:

The control circuit is designed to provide the Gate pulses for the switches used in the Inverter section and the rectifier section of the DC/DC converter. The switching sequence is such as the same gate pulse is given in the diagonally opposite switches in the inverter section. While gate pulses for the active switches used in the synchronous rectifier section i.e. at the secondary of the transformer are phase-shifted. Some dead time is provided to achieve zero voltage switching, i.e. parasitic capacitance finds sufficient time to discharge before the particular device goes into conduction. Since both synchronous rectifier and Inverter operate at the high frequency while designing the control circuits the components compatible with high frequency are selected.

The single-phase inverter is to be operated at high frequency; it is a simple full-bridge inverter. Control pulse and its complementary is required for the operation of the inverter.

The philosophy of the pulse- generation in the control circuit is as follows:

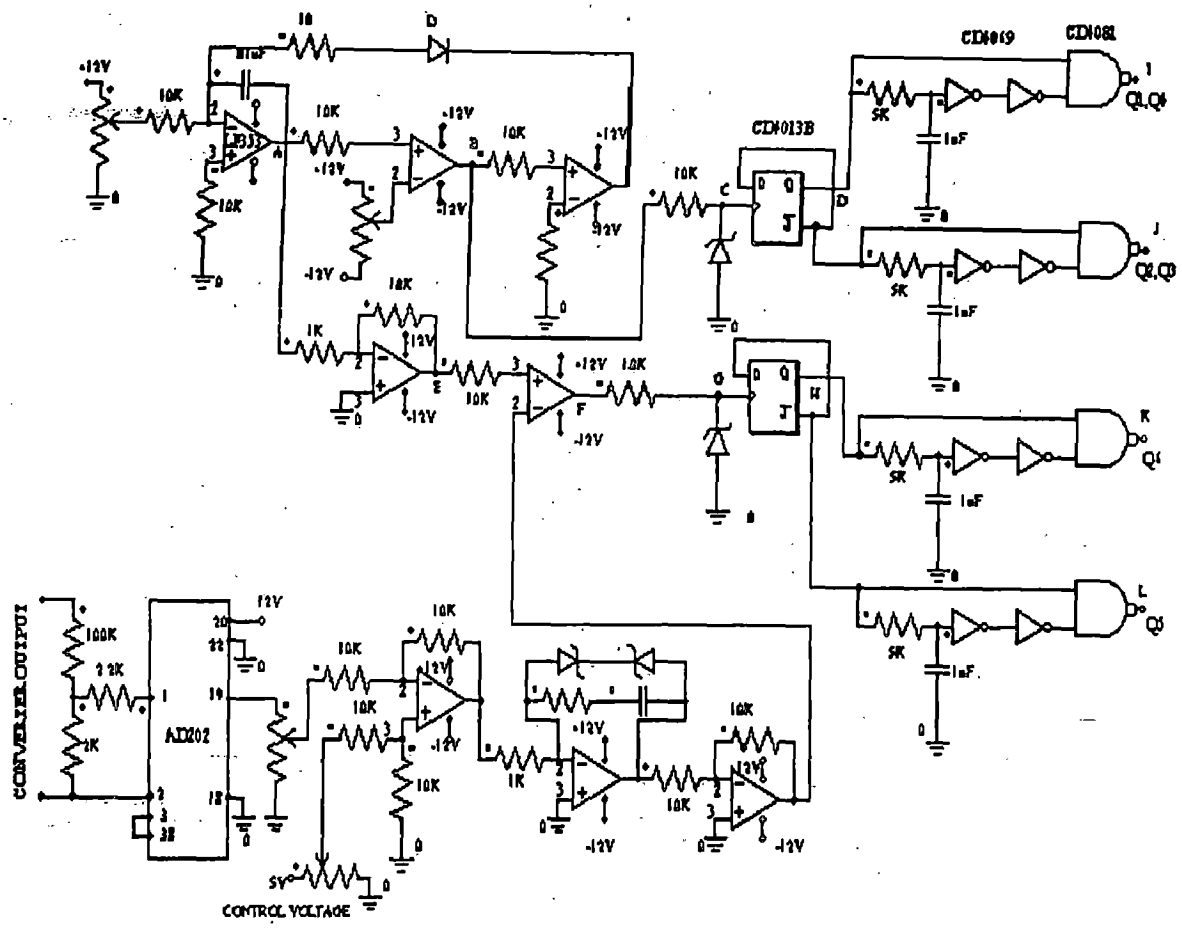


Fig. 8.1 Control Circuit for Single phase inverter & rectifier

At point A a sawtooth waveform of high frequency is generated through charging of capacitor through 1K ohm resistor and discharging through the 10 ohm resistor. The output of the comparator at point B is pulsed waveform going +12V to –12Vdc. This pulse is then clamped by a zener to 5 volts (at point C). This pulse is then fed to a positive edge-triggered D-flip flop (CD4013B) arranged in divide by 2 configuration which converts this pulse waveform into a square waveform of half the frequency of the clock pulse. The waveforms obtained at the pin number 1&2 of the flip-flop are the complementary to each other, since they are the outputs of the Q and Q! respectively. These pulses are then passed through a delay network to introduce the delay between the turning off & on of the devices of the same leg of the inverter. It is composed of the RC circuit , logic Inverter gate (CD 4069) and logic AND gate (CD 4081). The pulses

generated at point J & K are inverted & delayed so as to avoid shoot- through fault. The pulse at point J is used as gate drive signal for the switches S_1 and S_3, while the output at point K is used as gate drive signal for the switches S_2 and S_4.

8.2 Philosophy of Phase Shift Control and closed loop control

The rectifier section is to be operated at high frequency through phase shift control has been shown in Fig-8.1. First, At point A a saw tooth waveform of high frequency is generated through charging of capacitor through 1K ohm resistor and discharging through the 10 ohm resistor, this waveform is having some positive voltage to some negative value. The waveform at point E is amplified sawtooth is obtained by passing the sawtooth waveform in the Operational Amplifier in the non - inverted mode. This inverted sawtooth is compared with the output of PI regulator. The output of PI regulator can be positive or negative. The output of the comparator at the point F is a square wave which is going both positive and negative. This pulse is then clamped by a zener to 5 volts level at point G. This clock pulse is fed to the positive edge-triggered D-flip flop (CD4013B) which is as before arranged in divide by 2 configuration which converts this pulse waveform into a square waveform. This waveform (H) is phase shifted with respect to square wave (at the point D). These pulses are then passed through a delay network to introduce the delay between the turning off & on of the devices of the same leg of the inverter. The pulse at the point L is inverterd to the pulse at the point M.

Thus controllable phases shift as desired for the phase shift control of the synchronous rectifier is obtained. AD202 is used for sensing the output voltage of the converter and this sensed voltage is then compared with the reference voltage signal, which is set to get the desired output voltage. The error between the reference and the actual is then processed in a PI regulator. The output of this PI regulator is then inverted and then compared with inverted sawtooth wave to get clock pulse for getting Phase shifted waveforms. The control is maintained in a manner that pulse- width of each pulse is maintained constant but phase shift angle is varied in accordance with the output voltage and hence the period for which the input power is delivered to the output is varied.

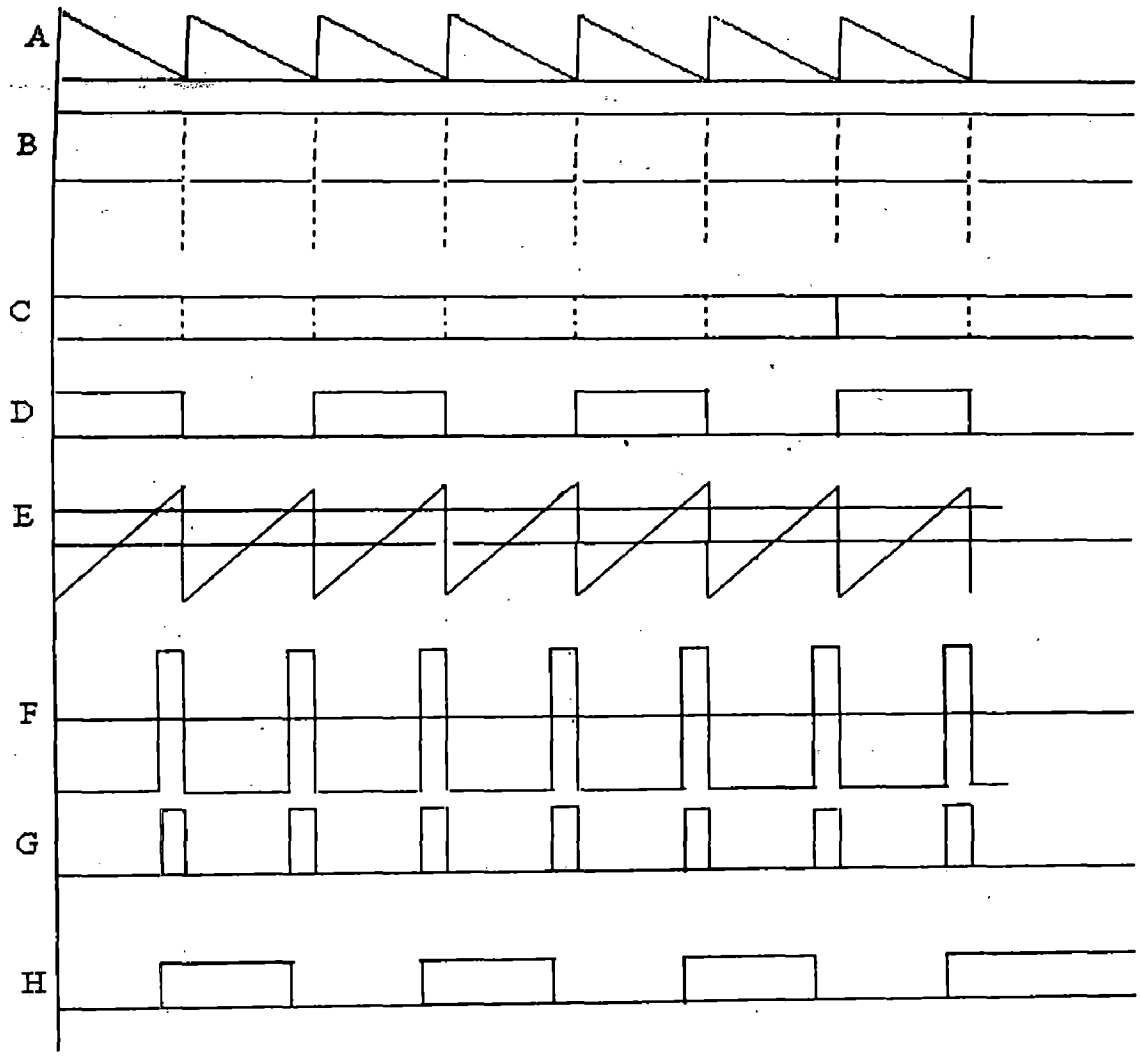


Fig. 8.2 : Generation of Phase shifted Square Waves for DC/DC converter

Various IC's used for the purpose of designing control circuit are;

LF 353- Dual Operational Amplifier

CD4013B- Dual Flip- flop

CD4069 - Hex Inverter

CD4081 - Quad 2-input AND Gate

AD 202- Voltage sensor

8.3 Firing Pulse Amplification and isolation Circuit

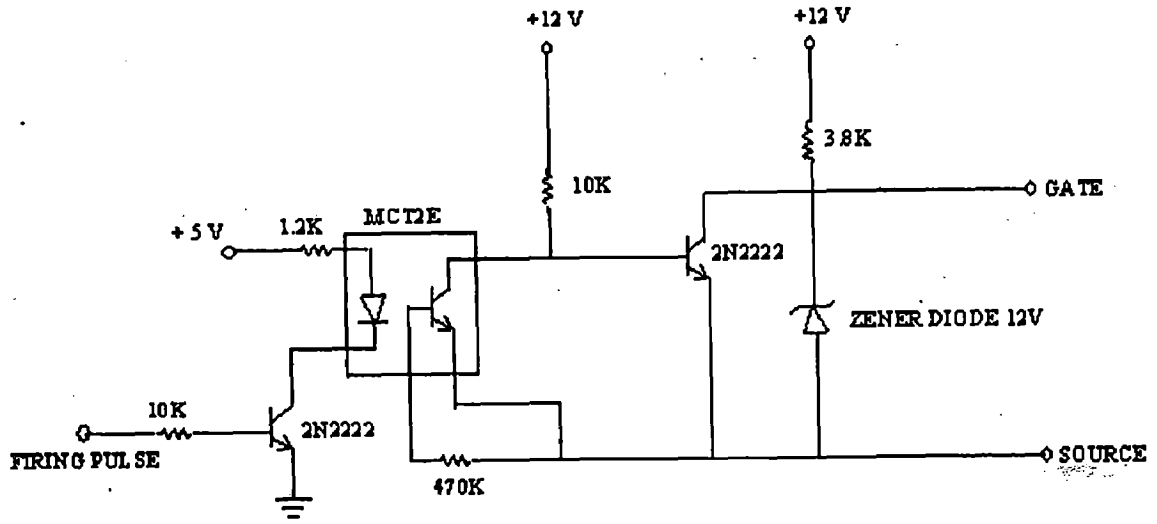


Fig.8.3 : Firing Pulse Amplification and isolation Circuit

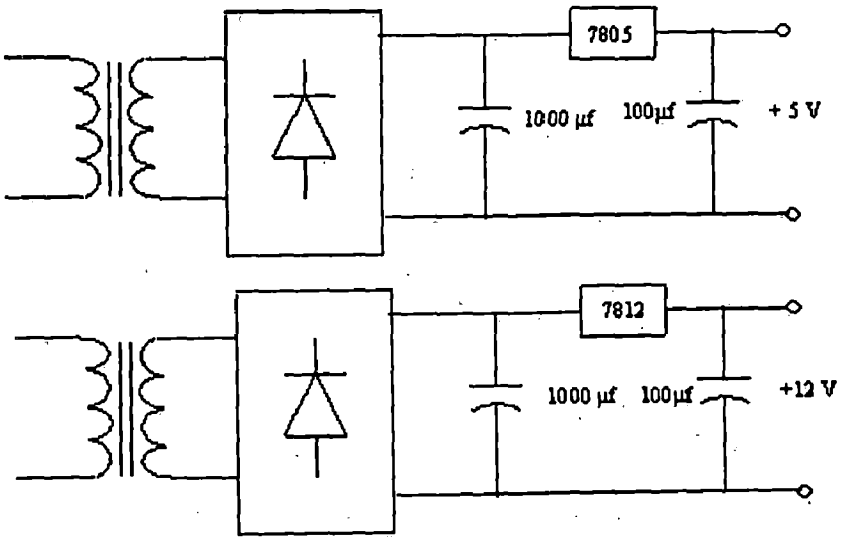
The pulse amplification and isolation circuit for MOSFET is shown in fig.8.3. The opto-coupler (MCT-2E) provides the necessary isolation between the low voltage isolation circuit and high voltage power circuit. The pulse amplification is provided by the output amplifier transistor 2N2222. The 0-5 V gating pulse from control circuit drives the base of 2N2222 switching transistor. When the input gating pulse is at +5V level, the transistor saturates, the LED conducts and the light emitted by it falls on the base of phototransistor, thus forming its base drive. The output transistor thus receive no base drive and, therefore remains in cut-off state and a +12 V pulse (amplified) appeared across its collector terminal (w.r.t. ground). When the input gating pulse reaches the ground level (0 V), the input switching transistor goes into cut-off state and LED remains off , thus eliminating no light and therefore a photo transistor of the opto-coupler receives no base drive and, therefore remains in cut-off state. A sufficient base drive now applies across the base of the output amplifier transistor and it goes into the saturation state and hence the output falls to ground level. Therefore circuit provides proper amplification and isolation.

Further since slightest spike above 20 Volts can damage the MOSFET, a 12V Zener diode is connected across the output of isolation circuit. It clamps the triggering voltage at 12V.

8.4 POWER SUPPLIES

D.C. regulated power supplies (± 12V, +12 V and + 5V) are required for providing the biasing to various IC's, etc. the system development has in-built power supplies for this purpose. The circuit diagram for various regulated DC power supplies are shown in fig.8.4. As shown the single phase AC voltage is stepped down by the transformer and then rectified using diode bridge rectifier. A capacitor of 1000 μf is connected at the output of the bridge rectifier for smoothing out the ripples in the rectified DC voltage of each supply. IC voltage regulated chips 7812, 7912, 7805 are used for obtaining the dc-regulated voltages of +12 Volt, -12 Volt and +5Volt respectively. A capacitor of 100 μf, 50 Volt is connected at the output of the IC voltage regulator of each supply for obtaining the constant, ripple – free dc voltage.

DC VOLTAGE	IC REGULATOR
+5 Volt	7805 (TO-3)
+12Volt	7812 (TO-3)
±12Volt	7812 (220Type), 7912 (220Type)



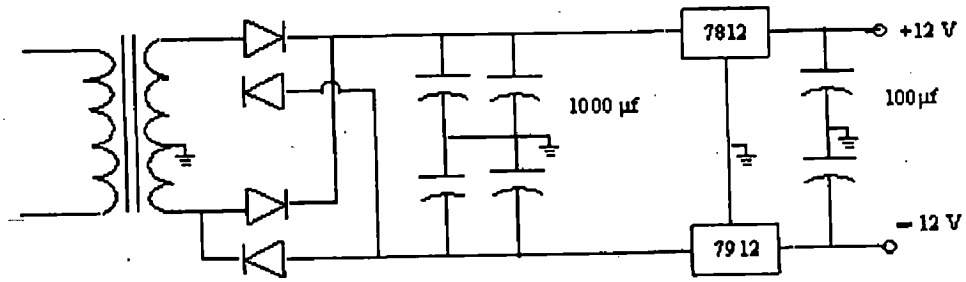


Fig. 8.4 : DC Power supplies (a) +5 V supply (b) +12 V supply (c) ± 12 V supply

8.5 CURRENT SENSOR CIRCUIT:

For sensing the current at primary of the transformer and load current TELCON HTP 25 hall effect current sensor is used. The output of sensor is a current which depends upon number of turns wound on sensor itself and current flowing in the primary circuit: the output current is given by

$$I_o = I_L * (N_p / N_s)$$

Where

N_p = Number of turns in the primary

N_s = Number of turns in the secondary

I_o = output current

I_L = load current

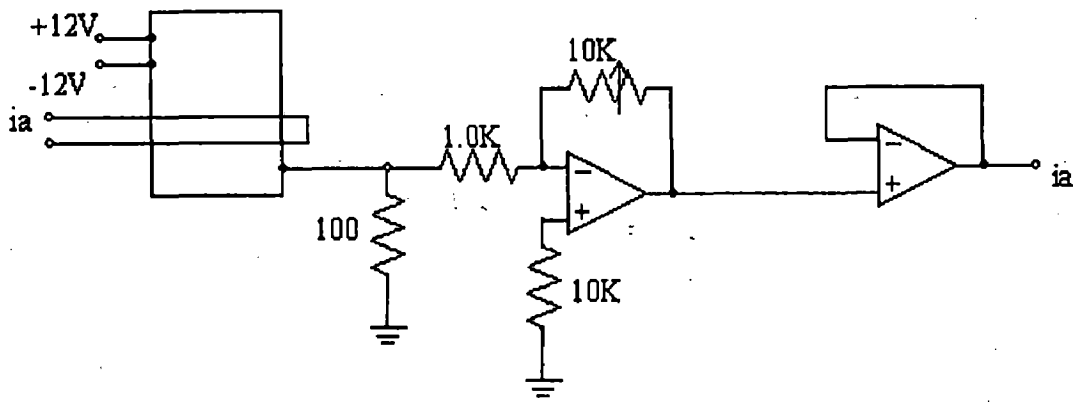


Fig- 8.5: Hall effect current measurement circuit

The transformation ratio of current sensor is 1000:1. Hence when the sensor is wound for two turns then

$$I_o = I_L * 2 * 10^{-3}$$

Scheme to measure current is shown in figure 8.5. The output of current sensor is converted into volt by passing it to the 470 ohm resistor. The output of current sensor is given to unity gain OP-AMP. For the elimination of harmonics low pass filter has been used.

8.6 PROTECTION OF MOSFETS

An RC snubber circuit has been used for the protection of the main switching device. The circuit diagram is given in Fig. 8.6. The design of the circuit is given below.

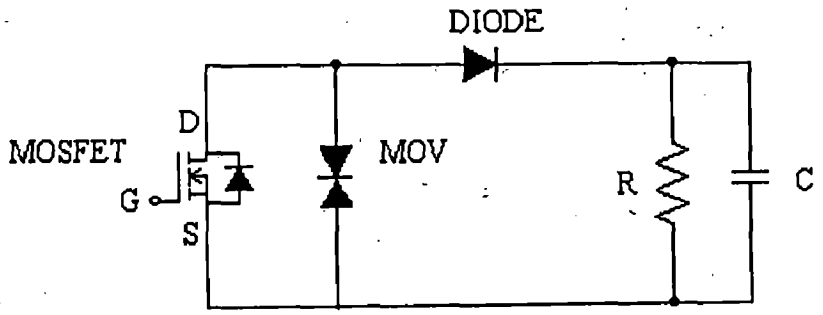


Fig.- 8.6: Snubber circuit

Energy stored in C, $E_c = (1/2) * C * V_{dc}^2$

$$\text{Power} = E_c * f_{max}$$

This is the power to be dissipated P_R in the resistance R.

Where V_{dc} is the maximum DC level and f_{max} is the maximum frequency of the output wave.

This energy needs to be dissipated within Ton for the worst case i.e. $T_{on(min)}$.

Since the outermost MOSFETS are switched for the minimum period, this duration comes out to be four times the minimum step of the output wave.

Therefore $T_{on(min)} = 1 / (6x\ f_{max})$

The time constant of the RC circuit is taken as one-fifth of $T_{on(min)}$

Therefore $T_{RC} = 1 / (5 \times 6x\ f_{max}) = R \times C$

Constant losses in R for the worst case are given by

$$P = V_R^2 / R$$

Taking an average value of V_R as 100 V, P= 2W

Also P_R for V_{dc} = 400V and f_{max} = 100 Hz is 0.8 W

Total power dissipation in R is P_R + P and = 2.8 W

The value of R is found from (3) for C= 0.1 μF and R comes out as 50 Ω.

A 100 Ω, 5W resistor has been used.

8.7 Transformer Design

The function of a transformer in switch-mode power supply is to provide both isolation and required voltage level conversion. The core selection for high frequency transformer design opts for ferrite cores. In the design of ferrite core transformers for use in switchmode power supplies, one must take into consideration switching frequency, operating flux density, the resulting core loss, and temperature of operation . Temperature rise above ambient is a direct result of core losses in the ferrite material and of copper losses in the windings. To limit the temperature rise due to core losses, it is must to limit the operating flux density for the specified switching frequency. The type of ferrite material chosen will influence the core losses at the given operating conditions. Ferrite materials have one paramount advantage, that is very high electrical resistivity, which means that eddy current losses are much lower than metals.

For ferrite transformers at 10 kHz, it is common practice to apply equation (3) using flux density (B) levels of 2 kG maximum and accordingly core dimensions & number of turns are calculated. Reductions in the size of magnetic components have been achieved by operating at higher frequencies, mainly in switching circuits. The advantages and disadvantages of the various types of ferrite core materials and geometries in transformers are reviewed in Tables 1 and 2.

Toroidal cores are made from a continuous strip grain oriented silicon steel, and are bonded to prevent vibration and maximise the "packing density". It is important that there are no gaps between the individual layers, which will lower the performance of the core. The sharp corners are rounded off, and they are usually coated with a suitable insulating

material to prevent the primary (which is always wound on first) from contacting the core itself.

C-cores are made by rolling a continuous strip into the desired shape, and after bonding, it is cut in half. To ensure the best possible magnetic coupling (i.e. no air gap), the cut ends are machined and polished as a pair, it is very important to ensure that the two are properly mated or unacceptable losses will occur. The core halves are commonly held together with steel banding, similar to that used for large transport boxes. The main disadvantage of the single c-core arrangement shown above is that its leakage inductance is rather high. C-cores are not as efficient as toroidal cores, but are easier to wind with conventional coil winding machines. The overall efficiency lies between the E-I core and the toroidal. E cores will dissipate heat more readily than enclosed shapes of pot cores.

Table-1-Ferrite Core Comparative Geometry Consideration

	Core cost	Bobbin cost	Winding cost	Winding Flexibility	Assembly	Mounting Flexibility	Heat dissipation	Sheilding
Pot core	High	Low	Low	Good	Simple	Good	Poor	Excellent
Slab-sided core	High	Low	Low	Good	Simple	Good	Good	Good
E-core	Low	Low	Low	Excellent	Simple	Good	Excellent	Poor
EC core	Medium	Medium	Low	Excellent	Medium	Fair	Good	Poor
Toroid	Very low	None	High	Fair	Nine	Poor	Good	Good
PQ cores	High	High	Low	Good	Simple	Fair	Good	fair

Table-2 :Advantages and disadvantages of various types of ferrite core

(a) Pot Cores	**Advantages** 1. Shielding excellent 2. Bobbin winding (inexpensive) 3. Hardware availability good 4. Mounting and assembly easy 5. Low loss materials available 6. Printed circuit mounting available 7. Can be gapped for specific inductance	**Disadvantages** 1. Size limitation 2. Heat confined 3. More expensive than other ferrites 4. Cannot handle large conductors
(b) E Cores	**Advantages** 1. Simple low cost winding 2. Heat dissipated readily 3. Mounting hardware simple 4. Can mount in different directions 5. Printed circuit board mounting available	1. Shielding is minimal

	6. Assembly is simple 7. Cores are inexpensive 8. Large wires can be accommodated 9. Low profile available 10. Low loss materials available 11. Can be gapped for specific inductance	
(c) EC Cores	1. Round center leg provides shorter path length for windings, saving wire and reducing losses 2. Core can handle more power 3. Round center leg prevents bends in wire 4. Can accommodate large wires 5. Printed circuit mounting available 6. Mounting hardware available 7. Low loss materials available 8. Can be gapped for specific inductance	1. Shielding low 2. More costly than E core 3. Takes up more space
(d) PQ Cores	1. Optimum ratio of volume to winding area 2. Minimum core size for given design 3. Minimum assembled size for a given design 4. Minimum PC board area 5. Easy assembly 6. Printed circuit bobbin available 7. Cores operate cooler 8. Low loss materials available 9. Can be gapped for specific inductance	1. More expensive than E Cores
(e) Toroids	1. No radiating flux 2. No accessories required 3. Low loss materials available 4. Cores can be gapped for specific inductance 5. Cores have a large radius to prevent sharp bends in wires 6. Cores can be painted with protective insulation to prevent shorting core to windings 7. Cores are inexpensive 8. High input impedance	1. Toroidal winding equipment necessary 2. Subjected to external stray fields 3. Cores are prone to saturate if excitation is unbalanced

Traditionally transformer design has been based on power frequency transformers with sinusoidal excitation. Empirical rules have evolved which generally lead to conservative designs.

Transformer core selection is usually done by solving two equations simultaneously:

Equation (1): $E = K*B_m*N*f*A_C \times 10^{-8}$

Where,

E = Primary voltage across N turns (volts)

B_m = Peak flux density in the core (gauss)

N = Number of turns

f = Frequency (Hz)

A_C = Effective cross sectional area of the core (cm^2)

K = waveform coefficient

= 4.44 for sine wave and

= 4 for square wave.

It is convenient to restate this expression as:

$$N \cdot A_C = \frac{E \times 10^8}{4 \cdot B_m \cdot f} \qquad (8.1)$$

By definition The window utilization factor can be represented as ,

Equation (2): $$K_u = \frac{N \cdot A_W}{W_a}$$

where ,

K_u = Winding Factor

W_a = Core winding area

A_w= Cross section of wire to be used

N = Number of turns

And Equation (2) may be restated as:

$$N = \frac{K_u \cdot W_a}{A_W}$$

If both side of the equation is multiplied by A_C , then

$$N^* A_C = \frac{K_u \cdot W_a \cdot A_C}{A_W} \qquad (8.2)$$

Equating equation (8.1) and (8.2) results in,

$$\frac{K_u \cdot W_a \cdot A_C}{A_W} = \frac{E \times 10^8}{4 \cdot B_m \cdot f}$$

Solving for $W_a A_C$,

$$W_a * A_C = \frac{E \cdot A_W \times 10^8}{4 \cdot B_m \cdot f \cdot K_u} \qquad (8.3)$$

$W_a * A_C$ is a factor that indicates power handling capacity in magnetic cores. Equation (8.3) allows one to select a core size regardless of operating conditions.

By definition, current density J= amp/cm^2 which may also be stated as:

$$J = \frac{I}{A_W}$$

On rearranging.

$$A_W = \frac{I}{J}$$

The transformer efficiency is defined as

$$\eta = \frac{P_0}{P_{in}} = E*I$$

Taking value of E from equation –1

$$E* A_W = 4*B_m* K_u *f* W_a *A_C \times 10^{-8} = \frac{E \cdot I}{J}$$

and

$$\frac{E \cdot I}{J} = \frac{P_O}{J \cdot \eta}$$

Since

$$P_t = \frac{P_O}{\eta} + P_O$$

Where P_t = apparent power, primary plus secondary

Then

$$W_a * A_C = \frac{P_t \times 10^8}{4 \cdot B_m \cdot f \cdot K_u \cdot J}$$

And

$$J = K_j \cdot A_p^{-0.14}$$

Where K_j - is the current density coefficient

Then combining the equation A_p can be found as follows:

$$A_p = \left(\frac{P_t \times 10^8}{4 \cdot B_m \cdot f \cdot K_u \cdot K_j} \right)^{1.16}$$

For full- wave bridge topology for Inverter and Rectifier

$$V_p = V_1 - 2 * V_d$$

$$V_s = V_o + 2 * V_d$$

Let us assume that forward voltage drop $V_d = 1$, then

$$V_p = V_1 - 2$$

$$V_s = V_o + 2$$

On substituting the value of V_p in equation (1)

$$N_p = \frac{(V_1 - 2) * 10^8}{4 \cdot f \cdot B_{max} \cdot A_c}$$

$$N_s = \frac{(V_O + 2)}{(V_1 - 2)} * N_P$$

In this chapter hardware design related issues are discussed. The control circuit design to generate gate pulses for the switches of the inverter circuit are developed. Also the phase-shift gate pulse generation for the switches in the rectifier section is developed. Here voltage mode control technique is used for the control of output voltage and accordingly in the generation of phase- shift gate pulse . The pulse amplification and isolation circuit is developed so as to isolate the main control circuit's ICs if any fault occurs in the power circuit. Power supply of $\pm$12V,+5 V are fabricated to supply the control circuit and current sensor. Current measurement circuit is also made. The design of high frequency transformer is described with the comparative advantages and disadvantages of various types of ferrite cores.

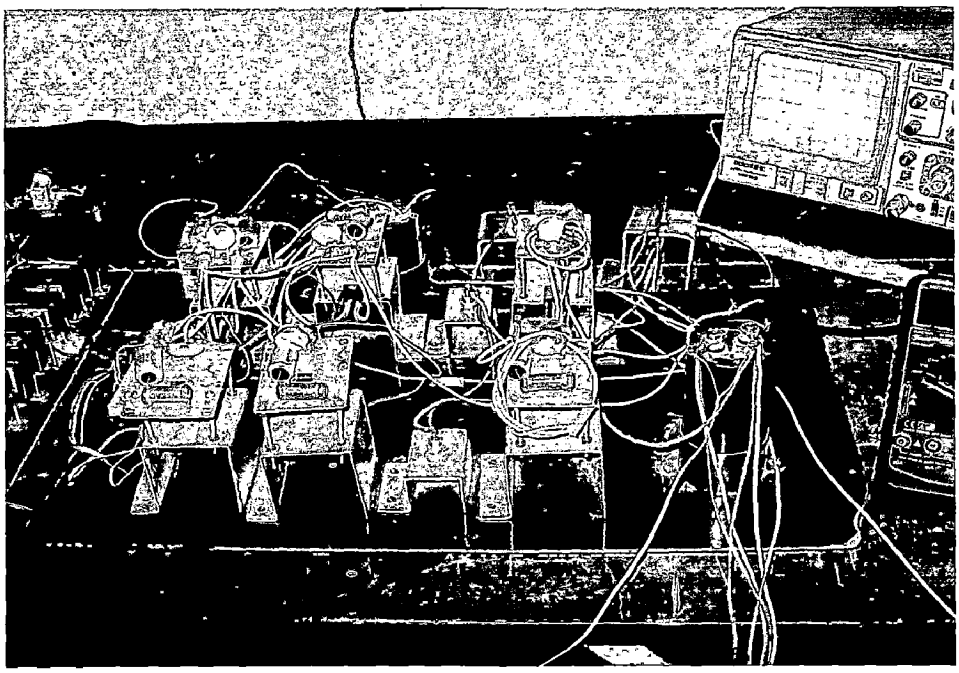


Figure- 9.1: Power Circuit

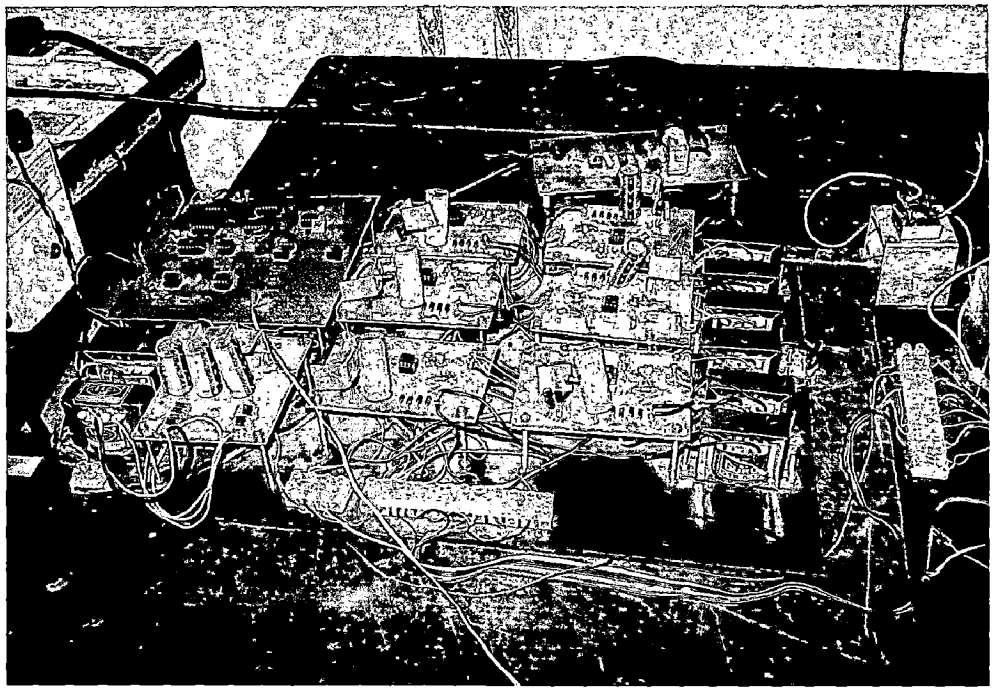


Figure-9.2: Control Circuit

In chapter-7 the simulation results of the Full- bridge ZVS Primary Phase-shifted dc/dc converter and Full- bridge ZVS Secondary Phase-shifted dc/dc converter are already discussed. In order to investigate the performance of both dc/dc converter prototypes delivering 200Watts at 200/100 volt are fabricated as shown in figs-9.1 and 9.2. In this chapter the results of the experimentation carried on these systems are presented. The results of the control circuit and power circuit waveforms for both the topologies have been taken . The control circuit used is same for both the topologies, hence control circuit results are taken once.

CONTROL CIRCUIT WAVEFORMS:

Since same control circuit is used for both topologies, the control circuit is discussed separately. The control circuit is used for the generation of high frequency pulses for all six switches in which the phase-shifted square wave pulses are given to the switches connected in the rectifier section has already been shown in Fig.8.2. Figure 9.3 below shows the waveforms of the control circuits at various points. Figure-9.3(a) shows the sawtooth waveform generated at point A.

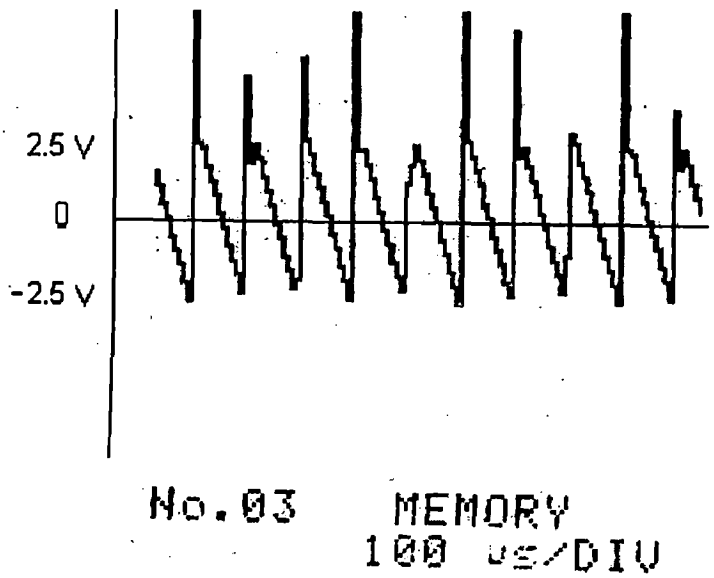


Fig. 9.3(a) Sawtooth Waveform Generation

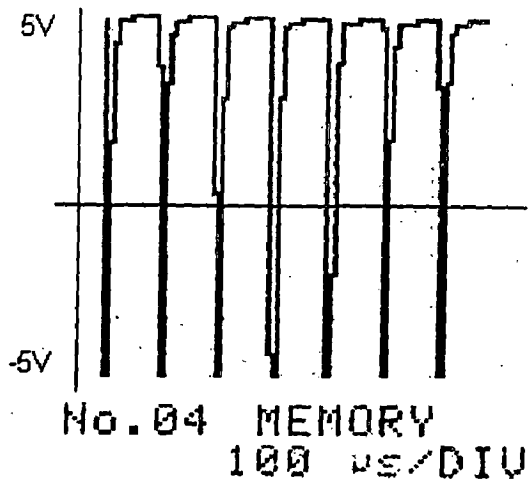
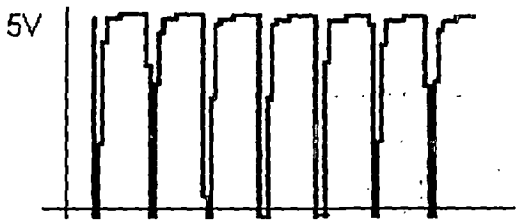


Fig. 9.3 (b) Waveform at point B in (Fig.8.2)



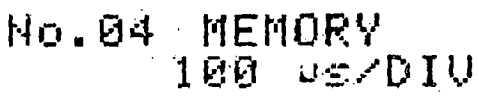


Fig.9.3(c) Clamped waveform at point C

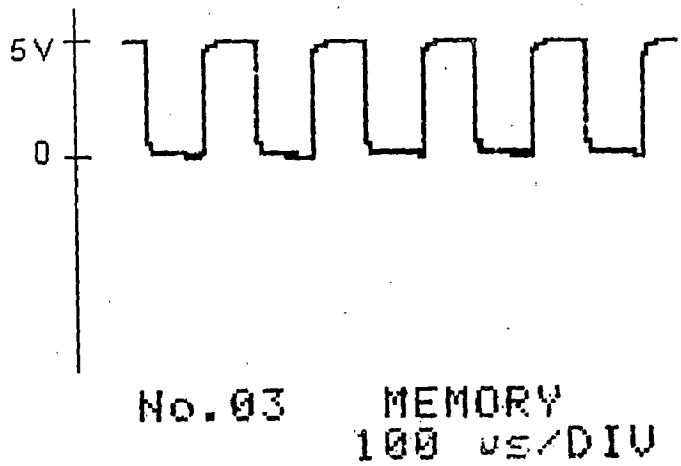


Fig.9.3 (d) Square wave at point D

The waveform shown in Fig.9.3 (b) is clamped so that the negative portion is trimmed off and the magnitude is limited to 5V; the resulting signal can easily be used for logic level signal generation. The resulting waveform is shown in Fig.9.3(c). The small negative voltage in the clamped signal is due to the drop in the zener diode used for clamping. But this is not a problem since the logic level circuits consider such signals as zero voltage level signals. When such a signal is fed to a positive edge triggered D- flip-flop in divide-by-2 configuration a square wave as shown in Fig-9.3(d) is produced.

The pulse waveform for switch 1 and the phase- shifted waveform for switch 6 is shown in figure-9.3(e).

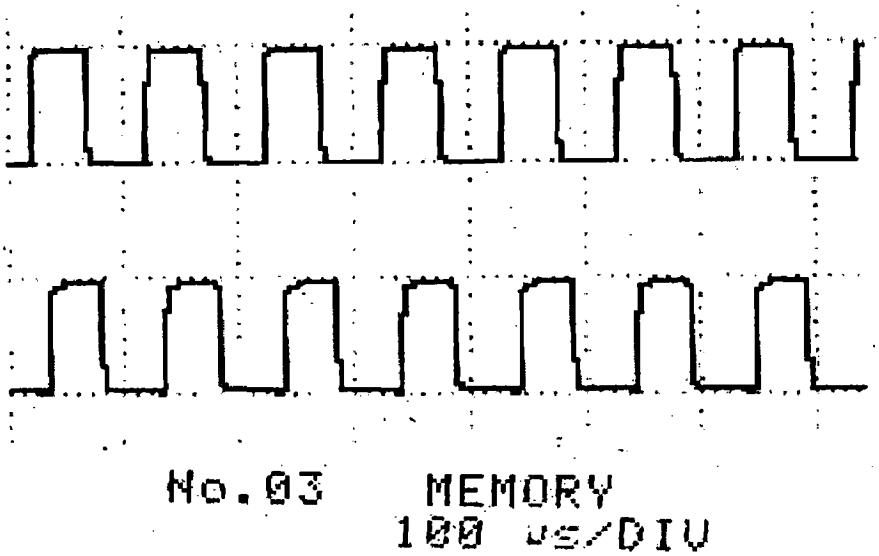


Fig.- 9.3(e) – Phase-shifted pulse waveform

POWER CIRCUIT WAVEFORMS:

- FULL- BRIDGE ZVS PRIMARY PHASE-SHIFTED DC/DC CONVERTER

In this topology Inverter section has all four switches, while rectifier section is a full bridge diode rectifier. The power circuit was tested under different load conditions. The results of waveforms at different point of the power circuit is recorded.

➢ Transformer Primary and Secondary Voltage Waveform :

The transformer Primary and Secondary Voltage waveform are shown in fig-9.4. The transformer is step down with turn-ratio of 2:1. The waveform is a high frequency AC square wave. The results obtained are same as those obtained during simulation.

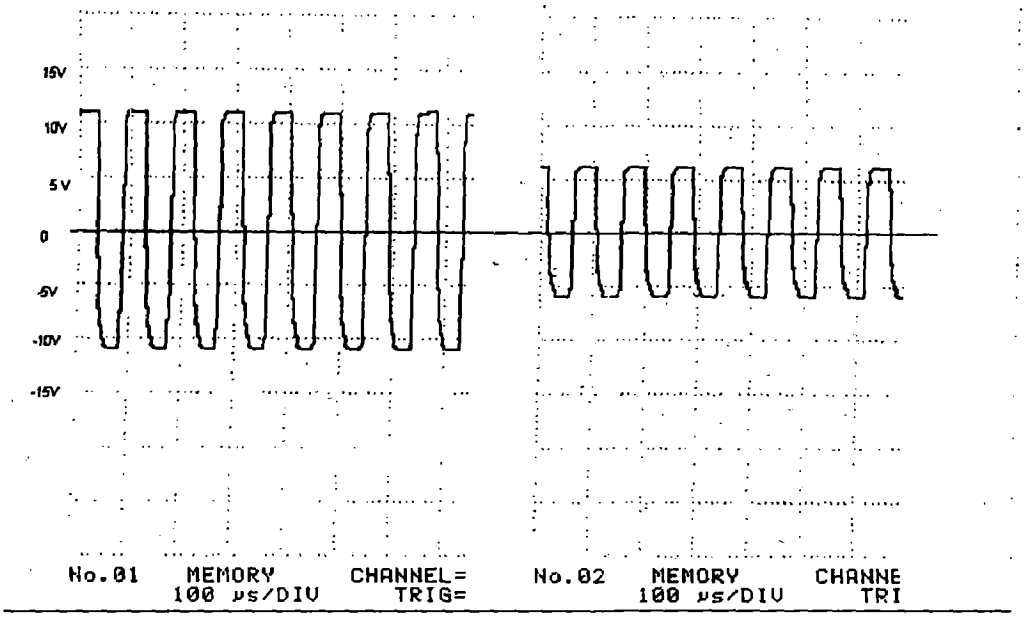


Fig.9.4(a) - Transformer Primary and Secondary Voltage
The volts / div=5 ; and Timing: 100 µS/div,

Frequency of AC square voltage is 10 kHz.

➢ Primary Current of Transformer:

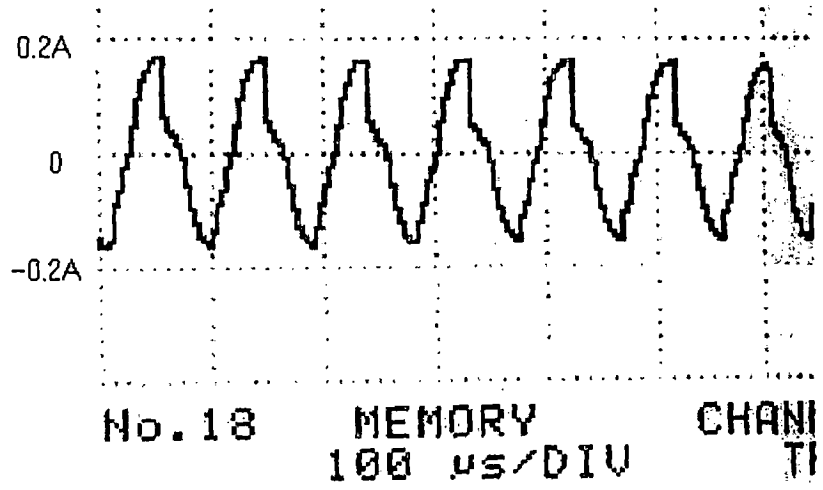


Fig.- 9.4(b): Transformer Primary Current

➢ The Drain to Source voltage at each leg of the Inverter is shown in Fig.-9.5. It is seen that zero voltage switching is achieved for both the switches. But switching transients are there at the time of turn-off the switch.

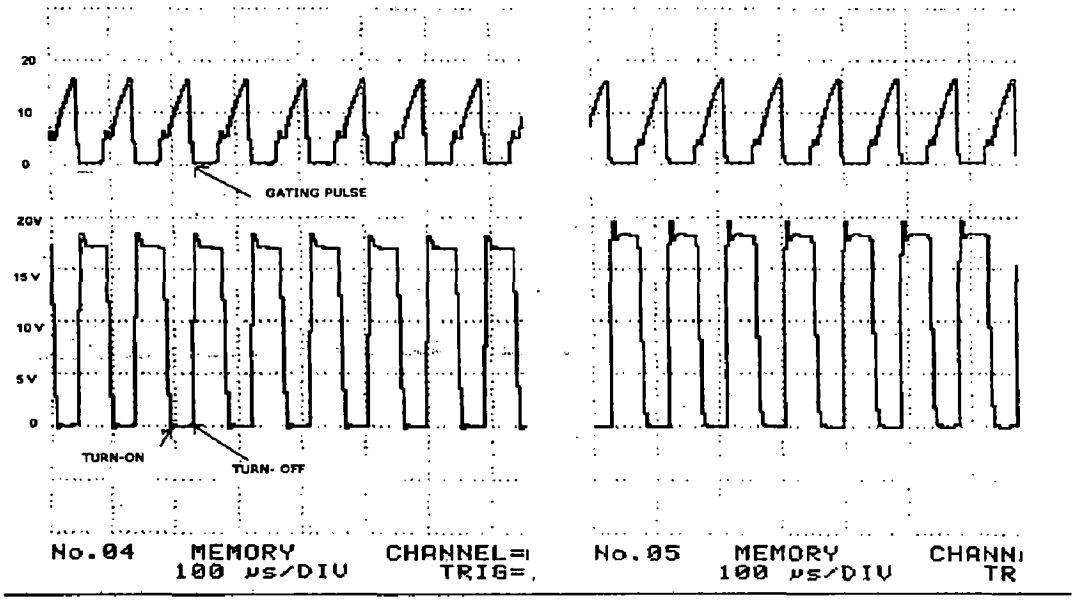


Fig. 9.5 (a)- The gating and drain-to-source voltage waveforms of the switches

f_s=10 kHz, V_o=17.5 V, P_o=100 W

Vertical scales: 5V/div. for the drain voltage and for the gating signal.

Timing: 100 µS/div.

➢ The voltage across the Diode :

The Anode to Cathode voltage at the leg of the Diode Rectifier is shown in Figure- 9.5(b). It is clear that switching transient in the diode is considerably reduced at turn- on but some switching losses are there at the turn- off.

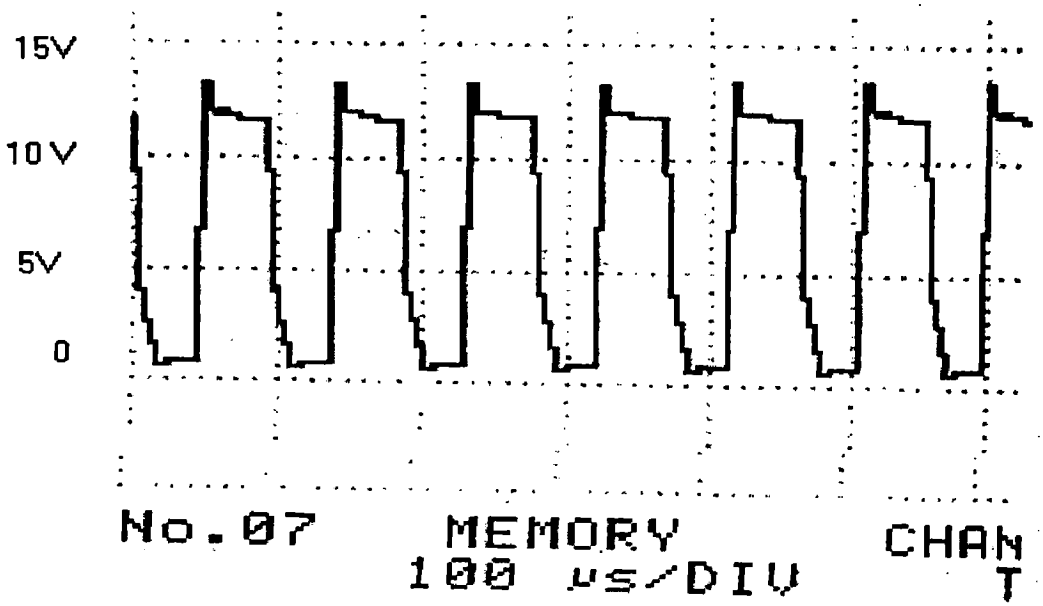


Fig.-9.5(b) Voltage across the Diode

➢ The Output Voltage and the Load Current

The transient response of output voltage and load current with step up increase in the load from 100watt to 200watt are shown in fig.9.6(a). It causes increase in the load current and decrease of voltage for a moment and then it recovers .

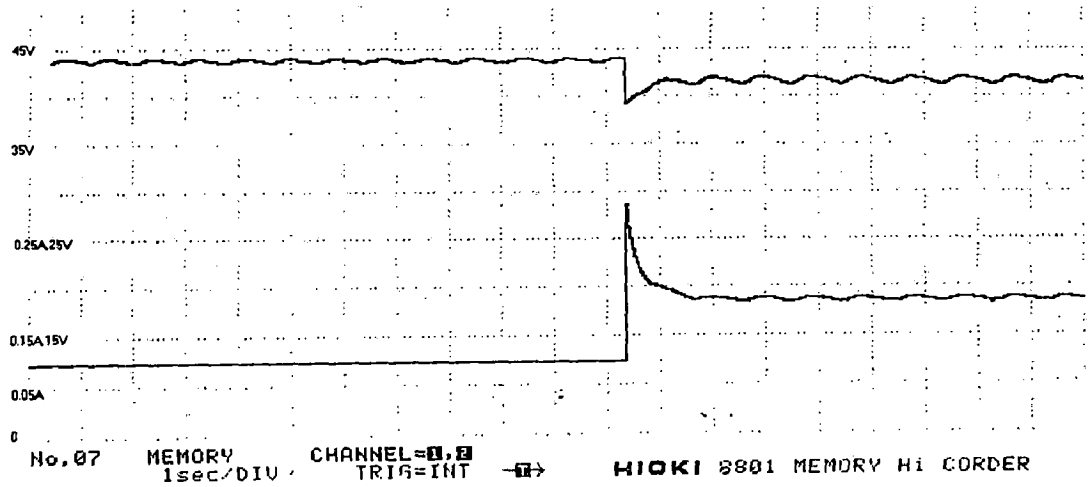


Fig.9.6(a):- Transient response of Output Voltage and Load Current with step increase in the load from 50% to 100%.

Vertical Scale: 100 mV/div. For Current

500 mV/div. For Voltage

Timing: 1sec/div.

The transient response of output voltage and load current with step down decrease in the load from 200watt to 100watt are shown in fig.9.6(b).

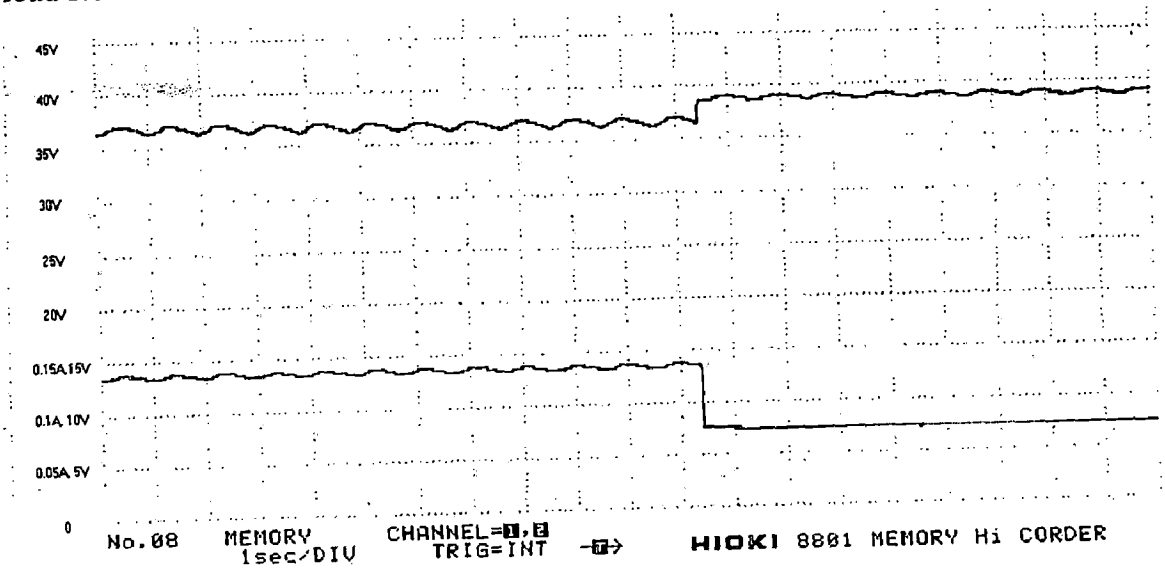


Fig. 9.6(b) : Transient response of Output Voltage and Load Current with step decrease in the load from 100% to 50%.

- FULL- BRIDGE ZVS SECONDARY PHASE-SHIFTED DC/DC CONVERTER TOPOLGY

  ➢ Transformer Secondary and Primary Voltage Waveform :

The transformer Secondary and Primary Voltage waveform are shown in fig-9.7(a). The transformer is step down with turn-ratio of 1:2.

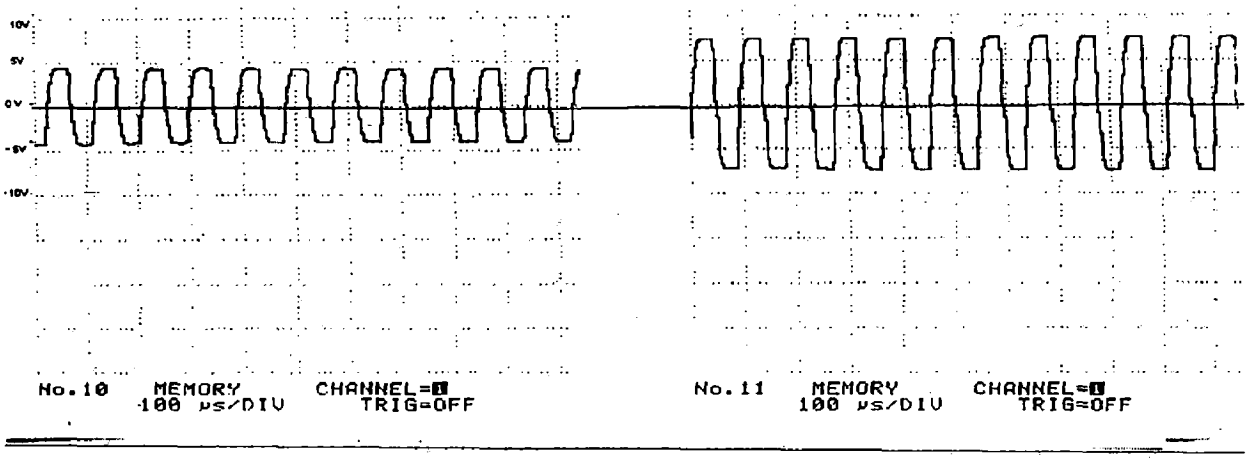


Fig.-9.7(a) - Transformer Secondary and Primary Voltage

The current in the transformer is shown in figure-9.7(b).

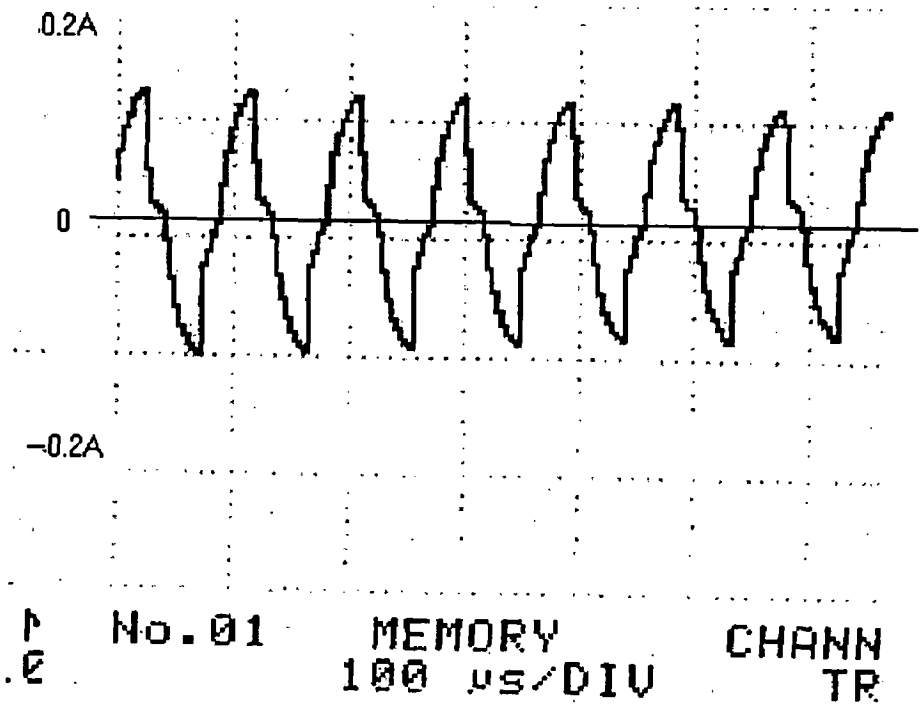


Fig.-9.7(b)- Transformer primary Current

➢ The Drain to Source voltage:

The Drain to Source voltage at each leg of the Inverter is shown in Figure-9.9. The volts/ div = 2. The applied voltage is 8.4 volt. It is seen from the figure that zero voltage switching is achieved for turn – on and for turn-off as well, even at a very low voltage i.e. 8.4V , approx.8 % of the rated voltage.

Also in this zero voltage switching is achieved for turn – on and for turn-off , even at no-load. The result of drain to source voltage with its control pulse is taken.

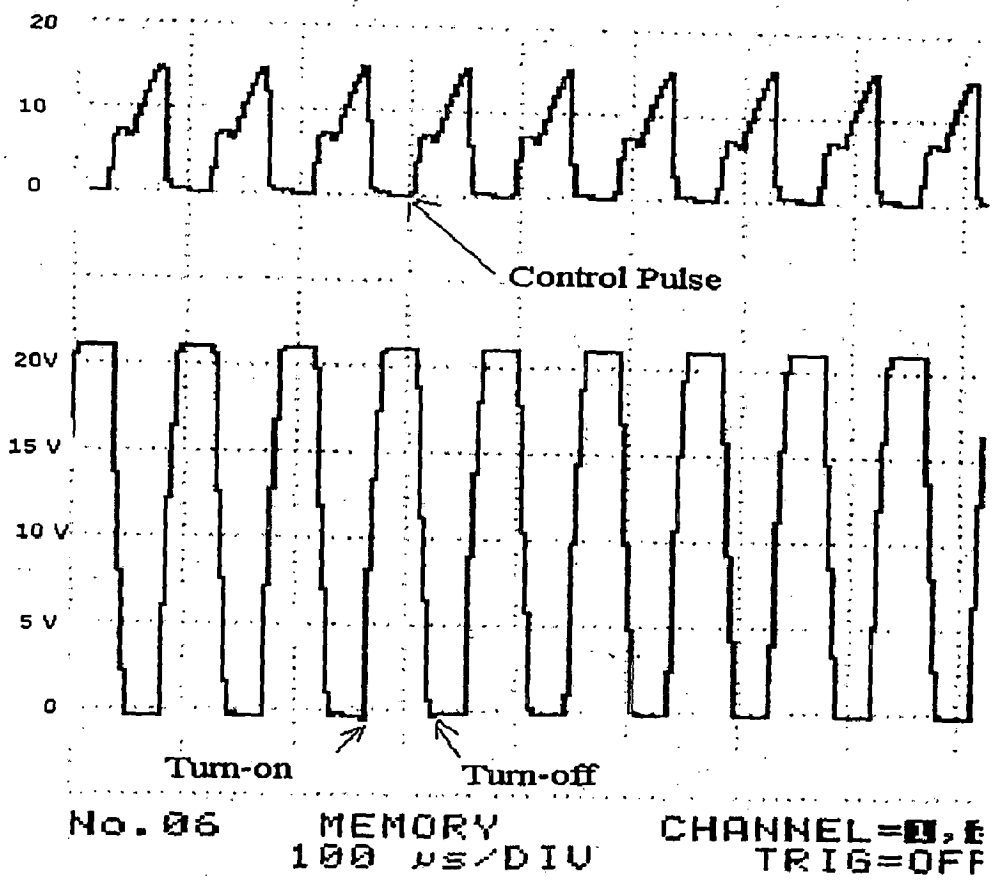


Fig.-9.9: Control pulse and Drain to Source Voltage

➢ The output voltage and load current

Fig. 9.10(a) shows the converter response to the step up increase in the load from half- full load to full-load i.e. 100 watt to 200watt. It is seen that the output voltage transient is a damped response. The output voltage and load current is recorded and is shown in the figure- 9.10(a).

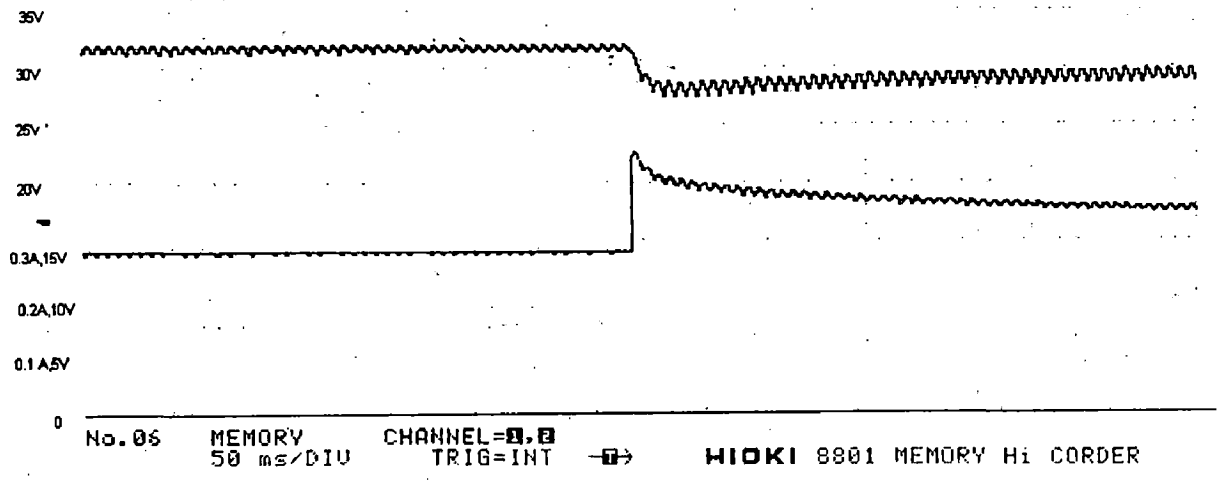


Fig.-9.10(a): The output voltage and load current dynamics with the step up increase in the load

Now the converter response when load steps down from 200 watt to 100 watt. Output voltage and load current transient response is shown in fig- 9.

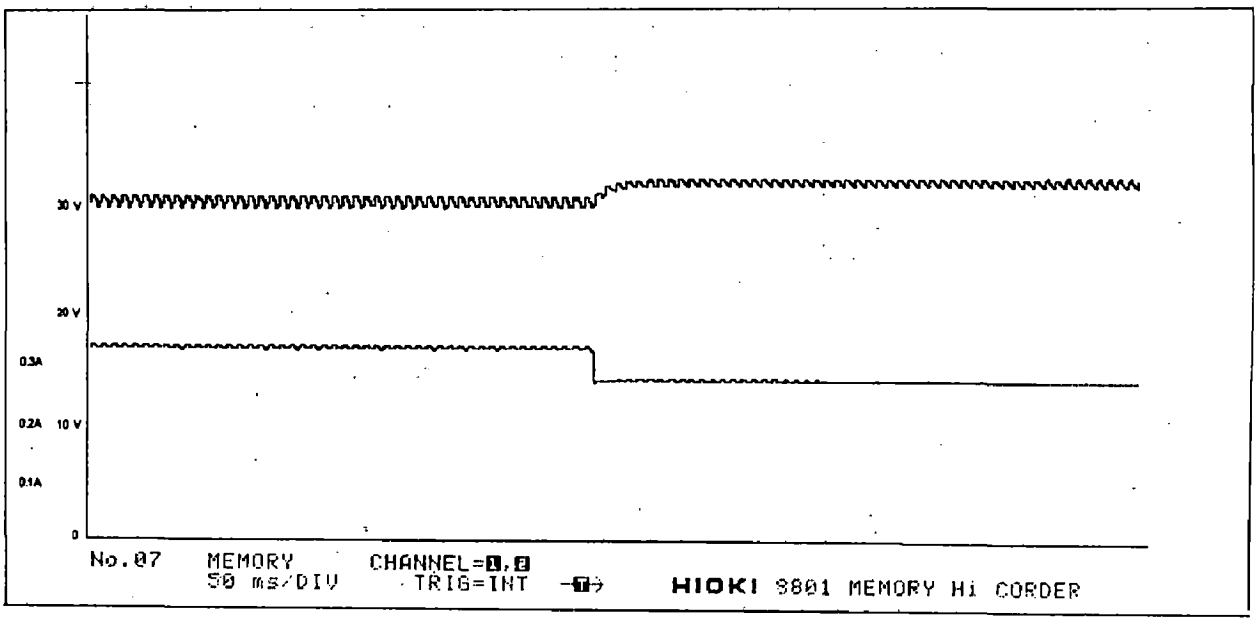


Fig. -9.10(b): Converter responses to load stepping down to 50%

Vertical Scale: 100 mV/div. For Current

5 V/div. For Voltage

Timing: 50msec/div.

In this chapter experimental prototype for both type of the Full bridge ZVS phase – shifted DC/DC converter is developed. One in which phase- shifted is given in the Inverter section and the rectifier is a diode full-bridge rectifier and the other one in which phase- shifted is given in the rectifier section and the rectifier is having two active switches and two diodes. The experimental results of both the developed systems has been taken in the closed loop operation. It is seen from the figures mentioned earlier in the chapter that the later system is able to achieve zero voltage switching even at no-load. Switching transients are comparatively less in the proposed system. Duty cycle loss is reduced, because in the Full bridge ZVS Primary phase – shifted DC/DC converter topology quasi-square waveform of Inverter output voltage is obtained while in the later topology a AC square type of waveform is obtained.

CHAPTER 10

CONCLUSIONS

Zero voltage switching is an adopted methodology in overcoming the switching losses owing to the operation of the converter at high frequency. Since high frequency operation in the converter is desired to reduce the size of magnetic components i.e. transformer, inductors and capacitance etc. At high frequency switching losses will be more, in order to reduce these losses soft switching is adopted. It reduces switching loss but many other problems arises i.e. duty cycle loss, large circulating current. Many remedies are suggested to remove these problems, a review of these was done in literature review in chapter-2. Phase – shifted method is also one of the solutions for this. Earlier phase-shift approach is used with phase- shift given in the one leg of the inverter section. It helps in achieving zero voltage switching but duty cycle loss is not addressed properly. Instead of giving phase-shift in the one leg of the inverter it is given in the secondary rectifier section. Two active switches are used instead of diode and the gate pulse given to these switches are phase-shifted with that of inverter section. It achieves zero voltage switching under wide load range and also eliminates duty cycle loss and reduces circulating current

The control method implemented in this provides not only input disturbance rejections from the input source, but also very good load dynamics. The need for such an advanced controller arises because of the nonlinearity that accompanies the full bridge PS-PWM converter. This control model was relatively simple to implement and required only one simple isolated voltage sensor.

SCOPE FOR FUTURE WORK

As mentioned previously, ZVS in the full bridge PS-PWM converter topology is achieved at the costs of increased conduction losses. If this converter topology is switched at low voltage, i.e. the resonant capacitors are not completely discharged when the switches are turned on, then the resonant circuit does not need to provide such high currents. This will reduce the conduction losses, although there are some switching losses due to the non-ZVS operation. An optimal low voltage switching condition, that results in the highest efficiency, may be found. Thus it is worthwhile to investigate the overall efficiency at low voltage switching instead of ZVS.

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Appendix-I **Core Characteristics**

S.No.	Core Number	A_c,Cm^2	MLT, cm	Volume, Cm^3	Weight	W_a, cm^2
1.	EE-3031	0.0502	1.72	0.651	1.02	0.176
2.	EE-2829	0.0907	2.33	1.35	2.19	0.252
3.	EE- 187	0.204	3.20	4.34	7.09	0.530
4.	EE-2425	0.363	5.08	9.22	15.5	0.807
5.	EE-2627	0.816	5.79	19.1	45.8	1.11
6.	EE-375	0.816	6.30	25.3	49.7	1.51
7.	EE-50	1.45	7.09	36.8	90.6	1.21
8.	EE-21	1.45	7.57	39.2	99.3	1.63
9.	EE-625	2.27	8.84	60.0	179	1.89
10.	EE-75	3.27	10.6	104.0	312	2.72
11.	EE-87	4.45	12.3	164.0	481	3.71
12.	EE-100	5.81	14.5	246.0	712	4.83
13.	EE-112	7.34	16.0	350.0	1029	6.12
14.	EE-125	9.07	17.7	481.0	1414	7.57
15.	EE-138	11.6	19.5	629.0	1880	9.20
16.	EE-150	13.1	21.2	829.0	2457	10.9
17.	EE-175	17.8	24.7	1312.0	3575	14.8
18.	EE-36	15.3	26.5	1654.0	3906	21.2
19.	EE- 19	17.8	31.7	2875.0	4889	33.8