SIMULATION AND EXPERIMENTAL VALIDATION OF MULTI PULSE AC/DC CONVERTER FOR MEDIUM VOLTAGE ASDs

A DISSERTATION

Submitted in partial fulfillment of the requirements for the award of the degree of

MASTER OF TECHNOLOGY

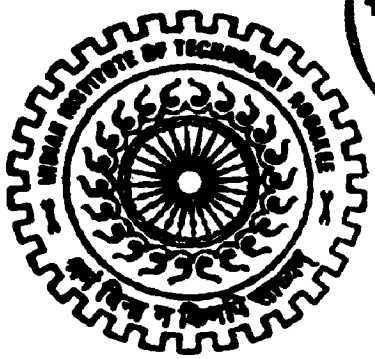
in

ELECTRICAL ENGINEERING

(With Specialization in Power Apparatus and Electric Drives)

By

SANJIV KUMAR



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Candidate's Declaration

I here by declare that the work which has being presented in the Dissertation Thesis entitled **"Simulation And Experimental Validation Of Multi Pulse AC/DC Converter For Medium Voltage ASDs"** in partial fulfillment of the requirements for the award of the degree of **Master of Technology** in **Electrical Engineering** with specialization in **Power Apparatus and Electric Drives**, submitted in the **Department of Electrical Engineering, Indian Institute of Technology, Roorkee, INDIA – 247667**. This is an authentic record of my own work carried out in the period of last two semesters from August 2005 to June 2006, under the supervision of **Shri Y. P. Singh**, Assistant Professor, Department of Electrical Engineering, Indian Institute of Technology, Roorkee, INDIA – 247667.

The matter embodied in this Dissertation Thesis has not been submitted by me for the award of any other degree or diploma.

Date: 27/06/06

Place: Roorkee

(Sanjiv Kumar)

This is to certify that the above statements made by the candidate are correct to the best of my knowledge.

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Abstract

In this dissertation work a 24-Pulse Buck-Boost AC/DC Converter is discussed. The objective of presented dissertation work is to simulate 24-pulse buck-boost AC/DC converter in MATLAB, and to validate experimentally the voltage regulation and power quality of the converter from utility side.

In the proposed scheme, phase shifted transformer is used in which secondary (that supply the power cells i.e. cascade single phase VSI modules in each phase of the A.C. motor) are wound to obtain small phase angle between them. The phase angle differs by multiples of 20° for 2.4 KV drives; multiples of 15° for 3.3 KV drives & by multiples of 12° for 4.6 KV drive. They cancel most of the harmonic currents drawn by individual power cell so that primary current are nearly sinusoidal & confirm to or approaches to IEEE power quality standards 519 -1992.

The proposed scheme also take care of unbalancing in secondaries winding voltage of phase shifted transformer or fluctuation in supply voltage. Developed converter maintains constant DC voltage of all the modules for entire range of supply voltage. Harmonic spectrum of input current, power factor of supply side also tested.

A simulation model is developed in MATLAB for different topologies and also for proposed scheme to compare the results and to obtain the performance comparison. Simulation results are also verified with experimental results and these are found satisfactory.

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Nomenclature

THD	Total Harmonic Distortion
IEEE	Institute of Electrical ad Electronics Engineers
MV	Medium Voltage
IEC	International Electro Technical Commission
PWM	Pulse width Modulation
AC	Alternating Current
DC	Direct Current
MV-ASD	Medium Voltage – Adjustable Speed Drive
MWPST	Multi-Winding Phase Shifting Transformer
IC	Integrated Chip
KHz	Kilo-Hertz
IPQC	Improved Power Quality AC-DC Converter
IGBT	Insulated Gate Bi-polar Transistor
GTO	Gate Turn Off Transistor
VFD	Variable Frequency Drive
ASD	Adjustable Speed Drive
VSI	Voltage Source Inverter
CSI	Current Source Inverter
SCR	Silicon Controlled Rectifier
FFT	Fast Fourier Transform
LH VFD	Low Harmonic Variable Frequency Drive
SC	Single Phase Cascade

Contents

Chapter 1

Introduction, Literature Survey and Overview

1.1 Introduction:

THREE-PHASE ac–dc conversion of electric power is widely employed in adjustable-speeds drive (ASDs), uninterruptible power supplies (UPSs), HVDC systems, and utility interfaces with nonconventional energy sources such as solar photovoltaic systems (PVs), etc., battery energy storage systems (BESSs), in process technology such as electroplating, welding units, etc., battery charging for electric vehicles, and power supplies for telecommunication systems [1] traditionally, ac–dc converters, which are also known as rectifiers, are developed using diodes and thyristors to provide controlled and uncontrolled unidirectional and bi-directional dc power. They have the problems of poor power quality in terms of injected current harmonics, resultant voltage distortion and poor power factor at input ac mains and slowly varying rippled dc output at load end, low efficiency, and large size of ac and dc filters. In view of their increased applications, a new breed of rectifiers has been developed using new solid-state self-commutating devices such as MOSFETs, insulated gate bipolar transistors (IGBTs).

In recent years, the harmonics in the power system are serious due to the widely applications of the electronic equipments in which the AC/DC converter are usually used. Therefore, it is an important topic to reduce harmonic components in the AC/DC converter [2]. The harmonic problems can be solved by using the active filters which are usually operated at high switching frequency and are not suitable for high power applications. The power factor and harmonic components of the utility input line current can be improved by the poly-pulse AC/DC converter.

In high-power applications, ac–dc converters based on the concept of multi-pulse, namely, 12, 18, 24, 30, 36, 48 pulses are used to reduce the harmonics in ac supply currents as well as the power factor of the input supply. These are named as multi-pulse converters [1]. They use either a diode bridge or thyristor bridge and a special arrangement of magnetic coupling through transformers and tapped inductors. One of the important reasons for such an extensive development in ac–dc converters is due to self-commutating devices. At low power rating, MOSFETs are used with unsurpassed performance because of their high switching rate with negligible losses. At medium power rating, an IGBT is considered an ideal device for such converters

with PWM technology. At a higher power rating, a GTO is normally used with self-commutating and reverse voltage-blocking capabilities at only a few kilohertz switching frequency.

1.2 Harmonics: Variable frequency drives all generate line currents at multiples of the AC line frequency-harmonics of 50 Hz. In three-phase drives they are generally a series of currents at harmonics 5, 7, 11, 13, 17, 19 and higher odd multiples of the 50 Hz fundamental frequency. The series is given by $6*n\pm1$ where n takes on all integer values. The magnitude of these harmonics depends on several factors.

1.2.1 Source of Harmonics:

These sources are briefly classified in to two as current-source nonlinear loads and voltage-source nonlinear loads [3].

Thyristor converters are a common and typical source of harmonic currents. Thyristor rectifier with a sufficient dc inductance produces a dc current. This is shown in figure (1.1a) below.

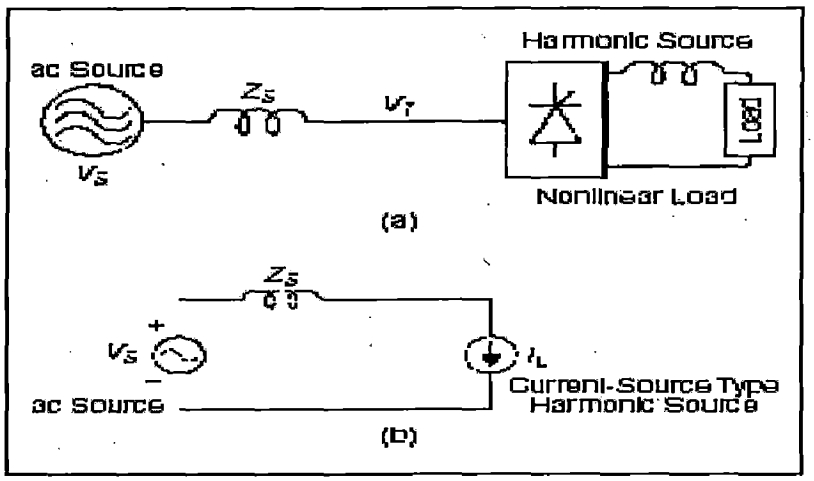

fig. (1.1a&b) Harmonic Source Current Type

The current waveform distortion i.e., the generation of harmonics results from the switching operation. A typical waveform is shown in figure (1.2). Because the harmonic current contents and characteristics are less dependent on the ac-side, this nonlinear load behaves like a current source non-linear load and represented as current source as shown in figure (1.1b). Therefore it is called a current source. Similarly, diode rectifiers with a sufficient dc inductance, a highly inductive load with silicon-controlled rectifier (SCR) ac power control, etc., are current-source nonlinear loads.

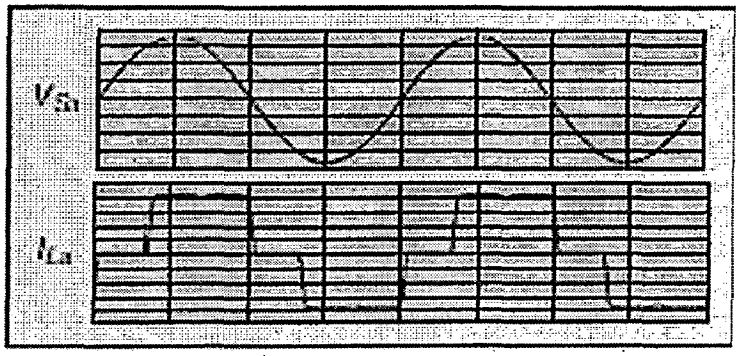

fig. (1.2) Harmonic Voltage and Current Waveform

Another common type of harmonic source is a diode rectifier with smoothing dc capacitors as shown in figure (1.3a).

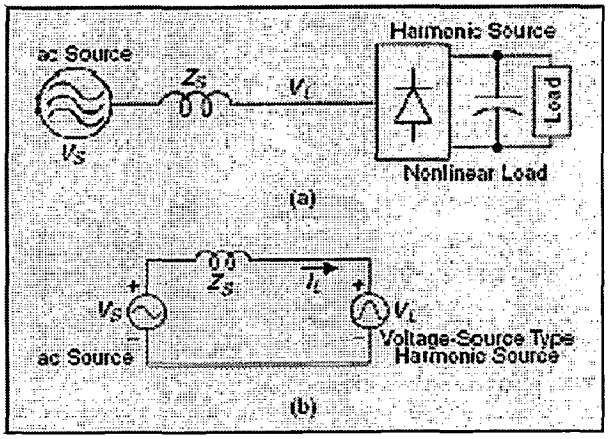

fig. (1.3a&b) Harmonic Source Voltage Type

Current and voltage waveforms are shown in figure (1.4). Although the current is highly distorted, its harmonic amplitude is greatly affected by the ac side impedance and source voltage unbalance, whereas the rectifier voltage, such as the voltage at the rectifier input terminal are less dependent on ac side impedance. Therefore, the diode rectifiers behave like a voltage source, rather than a current source. Figure 3(b) shows the equivalent circuit of the diode rectifier system where the diode rectifier behaves like a voltage source, rather than a current source.

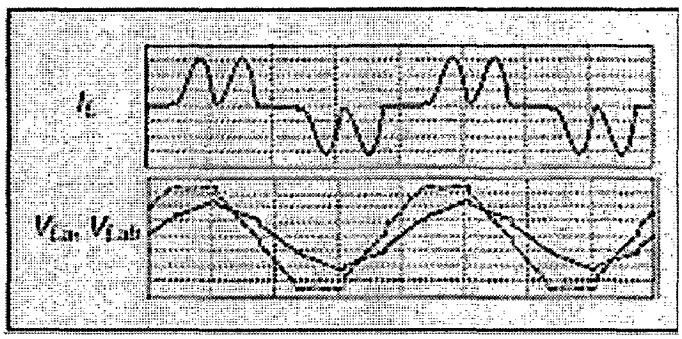

fig. (1.4) Harmonic Voltage and Current Waveform

- The current source SCR drives, generally used in the higher ratings, have harmonic amplitudes which are equal to the reciprocal of the harmonic order. Thus, 20% of 5th, 14% of 7th, 9% of 11th and so on. Total current distortion can reach about 30% , PWM or "diode front end" drives can have very high 5^{th} and 7^{th} harmonic distortion, reaching levels of 60% and 30% respectively, but their higher frequency harmonics are much lower than those for the SCR drives.
- A second factor is the source reactance. In general, increasing the reactance on the load side of a distribution transformer will have a favorable effect on harmonic amplitudes.

1.2.2 Effects of Harmonics: [17]

There are several common problem areas caused by harmonics:-

1) Problems caused by harmonic voltages:
   - Voltage distortion in induction motors
   - Zero-crossing noise
2) Problems caused by harmonic currents
   - Overloading of neutrals
   - Overheating of transformers
   - Nuisance tripping of circuit breakers
   - Over-stressing of power factor correction capacitors
   - Skin effect
   - These harmonic currents flow into the utility supply lines. Since the supply is generally characterized by transformer and distribution circuit reactance, the harmonic currents will cause harmonic voltage drops and consequent distortion of the line voltage. The results may be interference to electric clocks, data communications, telephone circuits, digital controls and a host of other effects in connected customer facilities.
   - They can also overheat transformers and supply apparatus.

Finally, harmonics can flow into power factor capacitors and actually be magnified by resonances with the supply reactance. The result is blown fuses or failure of capacitor.

1.2.3 Power Quality Concepts Related to Harmonics:

The impact of harmonics on power system components such as transformers and relays, and on consumers such as transformers, induction machines, and electronic devices can be described as a function of the below listed parameters. One most know how to calculate the harmonics in the system. The system voltages and currents can be shown in form of equations.

Harmonic Voltage is given by:

$$v(t) = V_o + \sqrt{2} \sum_{k=1,2,3,...}^{k\,max} V_{krms} \cos(kwt + \alpha_k)$$

Harmonic Current is given by:

$$i(t) = i_o + \sqrt{2} \sum_{k=1,2,3,...}^{k\,max} I_{krms} \cos(kwt + \alpha_k)$$

Total harmonic distortion of voltage is given by:

$$THDv = \frac{\sqrt{\sum_{k=2}^{k\,max} V_h^{\,2}}}{V_1}$$

Total harmonic distortion of current is given by:

$$THD_I = \frac{\sqrt{\sum_{k=2}^{k\,max} I_h^{\,2}}}{I_1}$$

1.2.4 Harmonic standards: [17]

1.2.4.1 IEEE 519-1981: A task force of industry engineers formed IEEE 519-1981, IEEE Guide for Harmonic Control and Reactive Compensation of Static Power Converters. This specification defined the allowable levels of voltage distortion on distribution feeders and served as a procurement document for new equipment. Unfortunately, the voltage distortion is very much a function of the short circuit capability of the source, and the filters used to obtain compliance with the specification had to be designed for each application. Still, this specification did much to get voltage distortion under control and it served as a valuable standard for mitigation of harmonic effects.

1.2.4.2 IEEE 519-1992: The problem arose in the implementation of IEEE 519-1981 that a number of customers on a distribution feeder could individually meet the distortion but, in the aggregate, exceed allowable limits. The specification was then revised to become IEEE 519-1992,and places severe restrictions on allowable levels of current harmonics from variable frequency drives. Filtering is not usually practical, and new technologies must be employed. It is suggested that conformance to IEEE 519-1992 should be a part of any new drive procurement document unless the drive is a small part of a large plant load. IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems, a document which now places limits on harmonic currents which a customer is allowed to source into the utility lines. The effects of this new standard are to introduce a whole new ball game for harmonic control. IEEE 519-1992 allows a graduated series of harmonic current levels depending on the source short circuit ratio.

Some other standards are:-

- EN 50 006," The limitation of disturbances in electricity supply networks caused by domestic and similar appliances equipped with electronic devices," European standard prepared by CENELEC.
- IEC Norm 555-3, prepared by the International Electrical commission.
- West German Standards VDE 0838 for household appliances, VDE 0160 for converters, and VDE 0712 for fluorescent lamp ballasts.

1.2.5 <u>Remedial Measures</u>: some basic techniques for removal of harmonics are as follows:-

- Install input/output filters to reduce harmonic distortion and improve power factor. This option was initially considered for existing wells, but the maintenance of each filter, coupled with the additional limitation imposed by the filters to the VFD power output and the substantial investment to install them in all wells, proved this a non-viable solution.
- Install twelve pulse VFDs. This topology was not a viable solution either, since while offering an input harmonic distortion lower than the Six Pulse CSI VFD, it had the same harmonics problem in the output.
- Install standard single level PWM Drives. This again was not implemented because even though PWM drives have a harmonic distortion lower than Six Pulse CSI VFDs, they have shown to cause detrimental effects to the ESP motor and cable insulation. These problems are associated with the rapid switching and dv/dt stresses.
- Utilize existing alternatives of Medium Voltage VFDs with low harmonic distortion (input/output) and without the rapid switching and dv/dt stress problems.

1.2.6 Emerging Solution:

Recent trained is to use higher pulse number drives. Drives are now manufactured with 24-pulse rectification at 2400V and 30-pulse rectification at 4160V. Medium-Voltage Adjustable Speed drives used modularity concept in which the single-phase cascaded voltage-source inverter that uses series connection of insulated gate bipolar transistor (IGBT) modules with isolated dc buses. The concept of using cascaded inverters is further extended to a new modular motor–modular inverter system where the motor winding connections are reconnected into several three-phase groups, either six-lead or 12-lead connection according to the voltage level, each powered by a standard IGBT inverter module [12,20]. These types of drives are known as multi-pulse drives. THD of these types of drives meets the IEEE-519 and power factor of input supply also gets improve. These drives uses phase shifted multi winding transformer which may have unbalancing in secondaries winding voltages, in this dissertation a concept to nullify the winding unbalance effect employing buck-boost converter is used along with rectifier system to maintain constant DC link voltage.

The developed converter is also suitable for that system which is powered by week link where voltage fluctuation is around +/- 20%. The developed converter maintains constant DC link voltage even in case supply voltage varies +/- 30%.

1.3 Literature Survey:

Multi-Pulse AC/DC converters are gaining popularity in many industries such as aerospace, petroleum, marine, air conditioning etc. Many authors have discussed about multi-pulse converters their uses advantages and disadvantages. The significant contributions in this field are discussed in this section.

Bhim Singh, Brij N. Singh, Ambrish Chandra,Kamal Al-Haddad, Ashish Pandey and Dwarka P. Kothari,Y Shakweh, P Aufleger [1],[26] presents an exhaustive review of three-phase improved power quality ac–dc converters (IPQCs) configurations, control strategies, selection of components, comparative factors, recent trends, their suitability, and selection for specific applications. The main aim of this paper is presenting a state of the art on the IPQC technology of three-phase ac–dc converters.

Richard H. Osman [2] compares the performance characteristics of five commonly used types of medium voltage motor drives. All of them have a DC link. Two of the drives are voltage fed types, the neutral point clamped inverter using GTO.s or IGBT.s, and the series-cell inverter using IGBT.s. The other three are current-fed designs, the filter-commutated drive using series thyristors in the inverter, the current-fed inverter with series GTO.s and auxiliary capacitors, and the load commutated inverter. Input characteristics of power factor and harmonics will be compared particularly with regard to IEEE-519 compliance. Output characteristics of waveform quality and common mode voltage also studied.

In this paper Fang Zheng Peng [3] describes the applications of active power filters and different topologies. How these filter helps to improve harmonic spectrum of input line current are studied. Various developed active filter are compared and tabulated in the proper manner. Application issues of these active power filters have been discussed elaborately

J.Ghaisari and A.Bakhshai [4] a PWM switching technique, which can be implemented on a multi-pulse converter system. It is also verified in this paper that proposed PWM switching technique preserves advantage of multi-pulse converter. Voltage control through PWM is linear, fast and straightforward. Thus PWM mode of operation is more useful in transient state.

D. Rendusara , K.J. Slater ,B.S. Lee , P. Enjeti [5] and others describes auto transformer connected 12-pulse and 24-pulse rectifier schemes as cost effective

methods for reducing line current harmonics in PWM drive systems. Design considerations for these rectifiers are also explained and performances of 12/24 pulse rectifier systems are also discussed.

Peter W. Hammond [6] describes a new approach to medium voltage variable frequency static AC drives which offers improvements in power quality and harmonic current injection in the power lines. The power factor of this new type of drive is high, motor voltage, current voltage waveforms are improved and also that torque pulsations are reduced.

Tsomg-Juu Liang, Jim-Fuh Chen, Ching- Lung Chu,Kuen-Jyh Chen [7] and Toshihko Tanaka, Naotsugu Koshio, Hirofumi Akagi [15] given idea about the unbalanced current in the 12-pulse phase control AC/DC converters in this paper. The 12-pulse star-delta type AC/DC converter will keep a balanced voltage with 30^{o} phase shifted at the low coupling coefficient condition. But an unbalanced current will be obtained in the 12-pulse autotransformer phase shift AC/DC converter at the low coupling coefficient condition. The theoretical phasor analysis of the unbalanced current was presented and a feedback controller was designed to overcome this problem.

Sewan Choi, Bang Sup Lee and Prasad N. Enjeti [8] [19] proposes two new passive 24-pulse diode rectifier systems for utility interface of pulse-width modulated (PWM) ac motor drives. The first approach employs an extended delta transformer arrangement, which results in near equal leakage inductance in series with each diode rectifier bridge. This promotes equal current sharing and improved performance. The proposed system exhibits clean power characteristics with fifth, seventh, eleventh, thirteenth, seventeenth, and nineteenth harmonics eliminated from the utility line currents. The second scheme is a reduced volt-ampere approach employing autotransformers to obtain 24-pulse operation. Detailed analysis and simulations verify the proposed concept, and experimental results from a 208-V 10-kVA rectifier system are provided.

In this paper Y.H. Liu, J. Arrillaga and N.R. Watson [9] proposed multilevel voltage-sourced converter is based on the reinjection of DC voltage pulses at six times the fundamental frequency. Substantial reduction in the capacitor size at the cost of extra components required is achived.It is shown that the resulting voltage and current

harmonics are well within the present standards without the assistance of pulse width modulation and theoretical waveforms are verified by computer simulation.

Bang Sup Lee, Prasad N. Enjeti and Ira J. Pitel [10] propose a 24-pulse diode rectifier system suitable for utility interface of PWM ac motor drive systems with low kVA components. Functioning of autotransformer and two zero sequence blocking transformers (ZSBT) in the dc link and a tapped interphase reactor is studied. Results produce near equal leakage inductance in series with each diode rectifier bridge ensuring equal current sharing and performance improvements. How the conventional 12-pulse converter can be converted in to 24-pulse operation from an input current stand point with use of specially tapped interphase reactor and two additional diodes is also discussed.

Ekrem Cengelci, Prasad N. Enjeti and JamesW. Gray [11],[24] discussed the modular motor–modular inverter concept for a medium-voltage adjustable-speed drive (MV-ASD) system. It is shown that standard MV motor winding connections can be reconnected into several three-phase groups, each powered by a separate three-phase pulse width modulation inverter, resulting in a high-performance MV-ASD system.

R. Teodorescu, F. Blaabjerg, J.K. Pedersen, E.Cengelci and P. Enjeti [12] discussed the Single-phase Cascaded (SC) VSI, triphase cascaded (TC) VSI that uses three IGBT triphase inverter modules along with an output transformer to obtain a 3 p.u. multilevel output voltage. The system yields a high-quality multistep voltage with up to 4 levels and low dv/dt, balanced operation of the inverter modules that supply each a third of the motor kVA. A staggered space vector modulation (SSVM) technique applicable to triphase cascaded VSI topologies is also demonstrated.

Mohamed C. Ghanem, Kamal Al-Haddad and Gilles Roy [13] presents a detailed theoretical analysis and experimental results of a novel means of obtaining sinusoidal input current and unity power factor (UPF) via a cascade buck-boost converter. Gating signals are generated by comparison of stored value in EPROM and instantaneous value of output voltage and current. Complete theoretical analysis, simulation results and experimental data on a 500 W converter are presented.

Vanice Scaini, P. Eng. [14] describe the availability of larger power switching devices that brought the development of larger power electronic circuits in recent years. One such circuit which is dc to dc converter, known as a DC chopper is explained and the benefits of DC choppers are also explained.

In this paper Someshwar C. Gupta [16] has given an idea of phase-locked loop (PLL). Apart from discussing the various analyses, design it is also discussed how this PLL circuit helps in synchronization.

Keith H. Sucker and Rafael A. Lastra, Carlos A.Loza and Albert Roc [17][18] discussed the various harmonic issues in case of variable frequency drives. Cause and effect of these harmonics are also studied. Author also suggested the remedial measures for these harmonics. Authors also suggested an alternative to conventional VFD technologies and the test of this drive is the subject of this paper. This Medium Voltage Low Harmonic Variable Frequency Drive (LH VFD) offers improvements in power factor, system efficiency and a reduction in harmonics effects as compared to traditional approaches.

Remus Teodorescu, Frede Blaabjerg, John. K. Pedersen, Ekrem Cengelci and Prasad N. Enjeti [20] describe the modularity concept applied to medium-voltage adjustable speed drives. This concept is applied to three-phase cascaded voltage-source inverter along with an output transformer to obtain a 3-pu multilevel output voltage. The system yields in high-quality multi step voltage up to four levels having low dv/dt. Both computer simulation results and experimental results are also demonstrated.

Sewan Choi, Prasad N. Enjeti and Ira J. Pitel [21] describes the polyphase transformer arrangements with reduced KVA capacities for harmonic current reduction in high power diode rectifier-type utility interface system, based on the concept of an autotransformer. The advantages of these systems are also explained.

A. Sapin, P. Allenbach, J.J. Simond [22] describes the modeling of multi-winding transformers. Two application examples of multi-winding phase shifting transformers (18 and 24 pulse) are also described in this paper.

G. Gonzalez, Microwave Transistor Amplifiers: Analysis and Design [23] describe the design consideration of inductor. Design procedure for air core inductor and toroidal core are also studied.

Leon M. Tolbert and Fang Z. Peng [25] describe two different multilevel topologies which can be used to make a converter for electric drives. Simulation and experimental results are also discussed and verified.

Richard Dickinson & Shaun Milano [27] describes the current sensing techniques using Hall Effect type sensors and also explains the advantages and disadvantages of these type of current sensor circuit.

1.4 Organization of Thesis:

Chapter 1: Introduction, Literature Survey and Overview

This gives brief introduction about the causes of harmonic, how does it affect the system, different disadvantages of harmonics. As it is need to reduce the harmonics due to different disadvantages traditional solutions are discussed to become familiar with the basic principles of compensation. The emerging topologies to improve the performance are discussed. Different harmonic standards that are dealt with in common are listed following with literature study. The objective of the dissertation work presented here is also indicated.

Chapter2: Multi-Pulse AC/DC Converters

Basic introduction of Multi-Pulse AC/DC converter is given in this chapter. Various topologies of Multi-Pulse AC/DC converter are also given along with their circuit diagram. Harmonic spectrum of various topologies is also discussed in this chapter.

Chapter 3: 24-Pulse AC/DC Buck-Boost Converter

The drive system where we use 24-Pulse converter is discussed in this chapter. Winding configuration of 24- pulse transformer, 3-phase diode rectifier along with Buck-Boost chopper circuit is also discussed. How to generate firing pulses in Buck and Boost mode is studied along with the mode selection logic.

Chapter 4: Simulation Study

Simulation models are developed using MATLAB Simulink. A 24-Pulse AC/DC Buck-Boost converter is developed. Error estimation block for close loop operation, pulse generation block, buck-boost chopper circuit, phase shifted transformer are simulated in this chapter and detail design of simulation is given in this chapter.

Chapter 5: Simulation Results

In this chapter simulation result of 6-Pulse, 12-Pulse and 24-Pulse are discussed. Voltage and Current wave form of input current of 6-Pulse, 12-Pulse are shown. Harmonic spectrum using FFT analysis is presented and various harmonic components are tabulated. 24-pulse Buck-Boost converter output voltage waveform for buck and boost mode is presented. Harmonic spectrum of converter input line current using FFT analysis is also presented and various harmonic components are tabulated. Performance of converter with change in load is also studied.

Chapter 6: System Development and Experimentation

The second part of the thesis is the experimental validation of simulated system. The hardware circuits which are developed are presented and recorded results are displayed. The fabrication of control circuit and power circuit is briefly discussed. The organization of control circuit fabrication is briefly presented. Closed loop results which are recorded are presented and FFT analysis is carried out. Tabulation of harmonic contents is done for different topologies to clearly specify the improvement achieved which is proved by using simulation model.

Chapter 7: Conclusion and Future Scope

Conclusion is drawn from the simulation and experimental work done, and presented in this chapter. Future scope for improvements in the same field to improve the performance and to handle the problems associated are briefly studied and presented to carry out in upcoming projects.

2.1 Introduction:

In Multi-pulse converter, quasi-square output voltage of N element six-pulse converter are combine through an electromagnetic interface electro-magnetically to produce a nearly sinusoidal output waveform [4,26]. The basic structure is shown in figure (2.1).

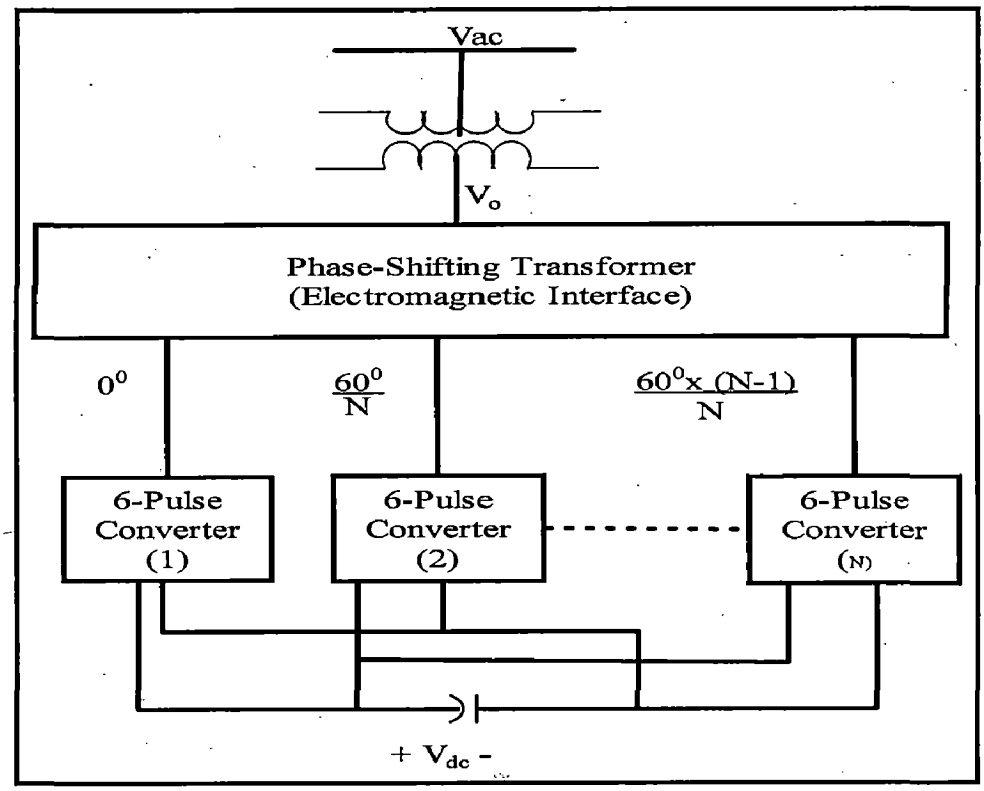

fig. (2.1) Basic Structure

The reduction in output distortion that is achieved by increasing the number of six-pulse unit, N, comes about through harmonics cancellation. Each unit produces a quasi-square-wave time shifted from that required for the final output. The phase-shift transformers align the fundamental component in the output voltage of multi-pulse converter. This provides the best utilization of the DC side voltage among the other power converter. The frequency of harmonics in the output of a 6N-pulse converter are (6N*k±1) f, where f is the fundamental frequency, N is the number of converter modules, and k=1, 2, 3, an integer. The Multi-Pulse configuration consists of several six-pulse converter units in either series or parallel on the DC side and phase shift in each unit is obtained by the special type of phase shifting transformer.

Pulse numbers as high as 48 are used in industrial drives system; however pulse numbers higher than 24 requires complicated and costly transformer and circuitry. But these are gaining popularity in market due to their additional features and the latest techniques in construction of multi-winding phase shifting transformers [5,6] have reduced their constructional complexity and cost is reduced significantly as well. The recent developments in auto-transformers allow us to make multi-winding phase shifting transformers (MW-PST's) of higher voltage and current ratings on same three phase cores. These transformers are used to feed rectifier modules which may be single phase or three phase and other buck boost switch arrangements. The PWM inverter modules are used in the rectified outputs and the whole circuit is used as a motor drive system. The harmonics are reduced as numbers of pulses are increased and the input current is nearly sinusoidal. These multi pulse converters are most popularly used in marine, aerospace and many other industrial applications where the size and power ratings are major considerations.

2.2 Multi-pulse Topologies:

According to number of pulses multi-pulse converter can be characterized in to following :

a) 6-Pulse Converter
b) 12-Pulse Converter
c) 18-Pulse converter
d) 24-Pulse Converter
e) Improve 12-Pulse converter

2.2.1 6-Pulse Converter:

This is the simplest converter as shown in figure 2.2. A diode bridge rectifier unit fed from the delta-star transformer. This is the cheapest converter. It has the poorest harmonic performance. The input current spectrum has 20% fifth and 12% seventh harmonics. The rapid commutation rate results in significant harmonic components out to the 35^{th}.

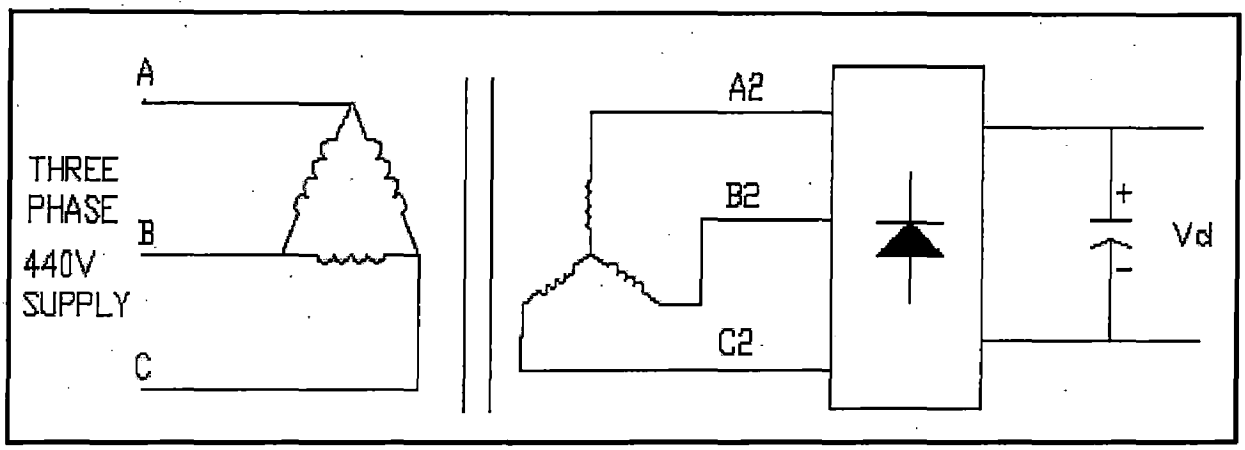

fig (2.2) 6-Pulse Rectifier

2.2.2 12-Pulse Converter :[7]

12-Pulse converter is divided into following two category on the basis of transformer used

a) Δ-Y Isolated Transformer 12-Pulse converter

b) Auto Transformer 12-Pulse converter

2.2.2.1 Δ-Y Isolated Transformer 12-Pulse converter :

The conventional Δ-Y Isolated Transformer 12-Pulse converter is shown in figure (2.3). The 12-pulse converter requires two six-pulse converters connected through isolation transformers (fig. 2.3).

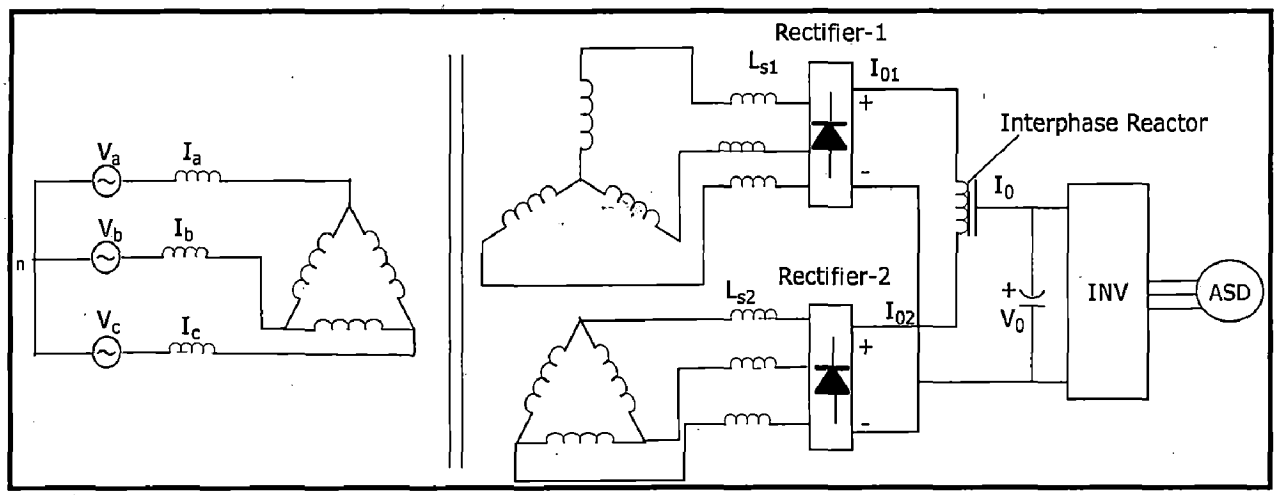

fig. 2.3 Δ-Y Isolated Transformer 12-Pulse converter

An interphase transformer (IPT) is required to ensure independent operation of the two three-phase diode bridge rectifiers. The operation of the conventional 12-pulse converter results in the absence of the fifth and seventh harmonics in the input utility line current. However, the total harmonic distortion (THD) of input line currents are still high and do not qualify as clean power [8] .The power factor and

harmonic components of the utility input line current can be improved by shifting the input voltages 30° in the Δ-Y connected AC/DC converter as well as in the autotransformer phase-shifted AC/DC converter. But the output voltages of these AC/DC converters are not controllable. The output voltage of the 12-pulse AC/DC converter can be controlled by using the thyristors instead of diodes. The 12-pulse phase control AC/DC converters with Δ -Y isolated transformer is shown in figure (2.4) [7]. A very important point is that although only half of the harmonic spectrum is present in the 12-pulse case compared to the 6 pulse, those components of the 12 pulse spectrum are about equal to the 6-pulse values. Due to the rapid commutation rates, the high order harmonics are quite significant. For the current-fed cases, the total current harmonic distortion at the converter input is about 15% for 12-pulse.

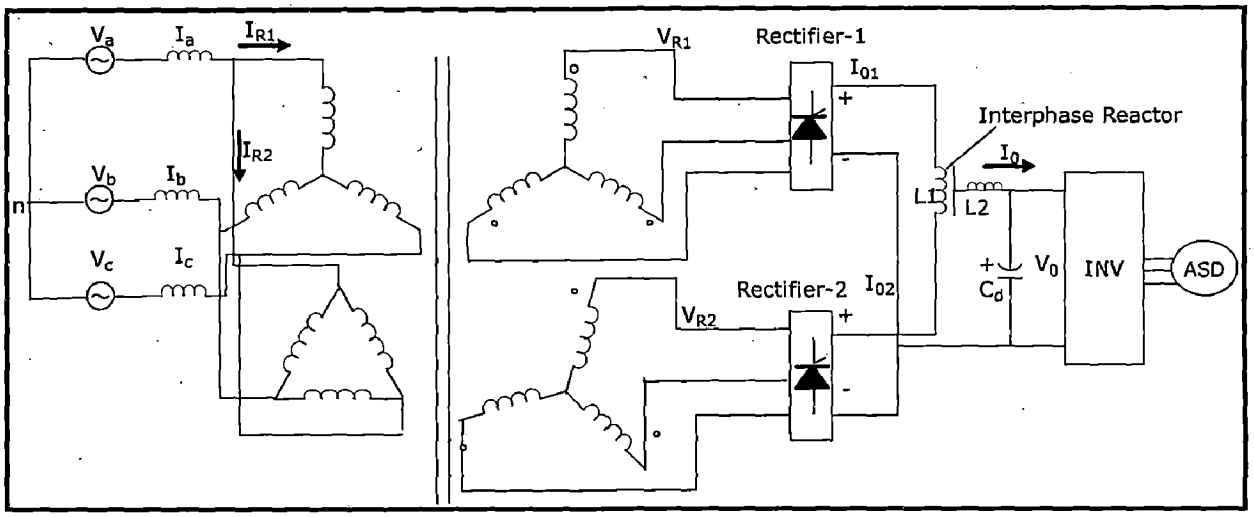

fig.(2.4) 12-Pulse Phase Control AC/DC Converters
With Δ -Y Isolated Transformer

2.2.2.2 Auto Transformer 12-Pulse converter :

The conventional Auto Transformer 12-Pulse converter shown in figure (2.5). The power factor and harmonic components of the utility input line current can be improved by autotransformer phase-shifted AC/DC converter. But the output voltages of this AC/DC converters are not controllable . The output voltage of the 12-pulse AC/DC converter can be controlled by using the thyristors instead of diodes. The 12-pulse phase control AC/DC converters with autotransformer connected is shown in figure (2.5) [7,21].

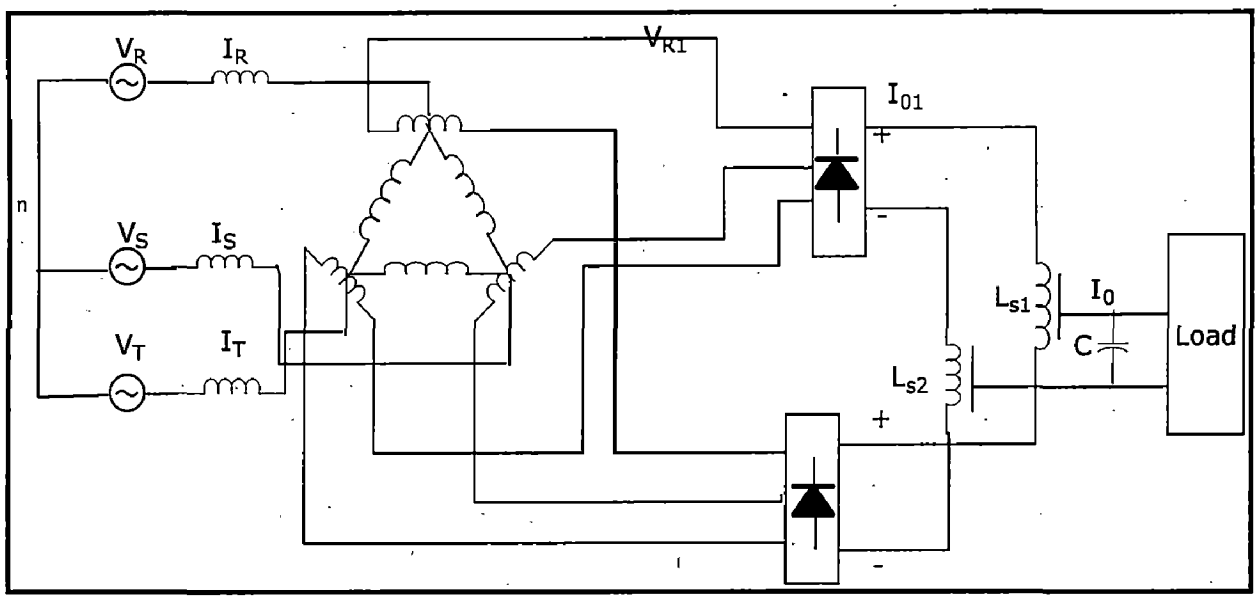

fig.(2.5) 12-Pulse Phase Control AC/DC Converters With Autotransformer

2.2.3 18-Pulse Converter :

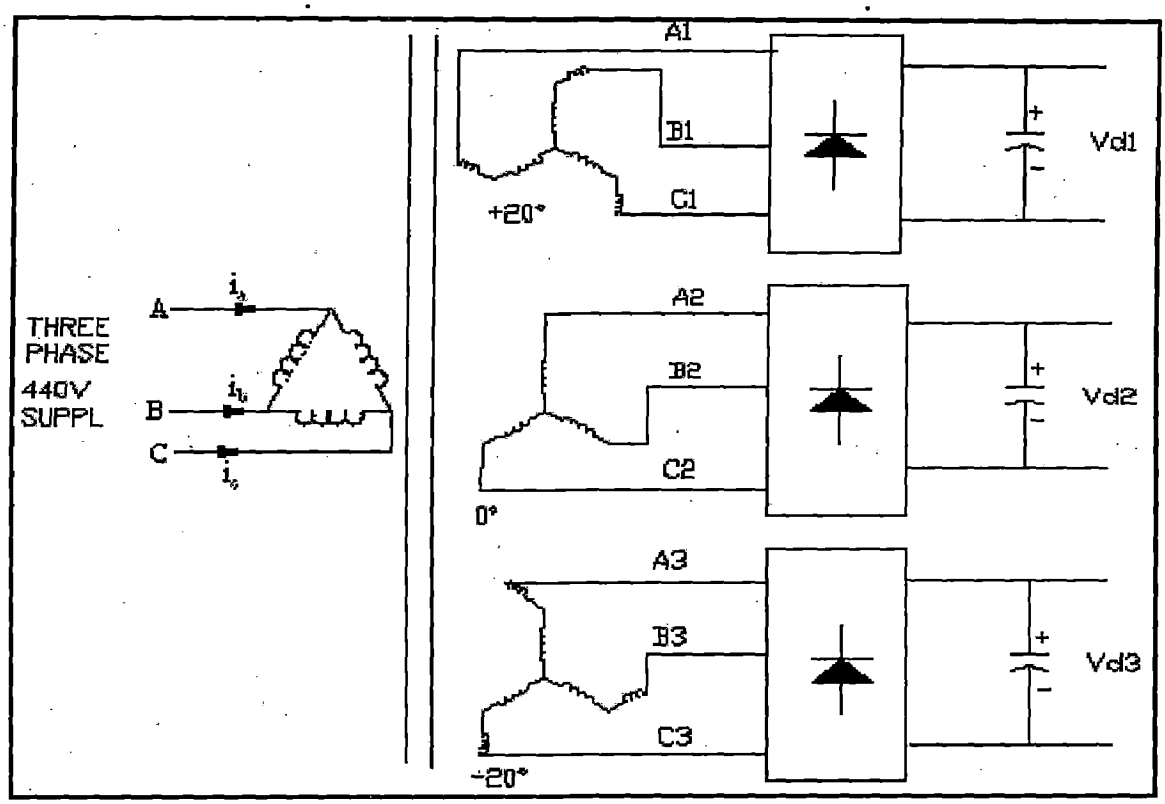

fig.(2.6) 18-Pulse Converter

Figure (2.6) shows the schematic diagram of 18-pulse rectifier with a three phase delta–star multi winding phase shifting transformer. The secondary windings voltages are displaced with respect to each other by 20° and are phase displaced by +20°, 0°,-20° with respect to primary. The current waveform of this rectifier shows that the input current is 18 stepped and is approaching more towards sinusoidal. The harmonics are further reduced in this type of multi-pulse converter. This type of rectifier system is gaining more and more popularity due to the fact that certain order harmonics which it reduces to minimum.

2.2.4 24-Pulse Converter :[8]

24-pulse converter can be divided in to following two categories on the basis of transformer used:

a) Non-Isolated type converter

b) Isolated type converter

2.2.4.1 24-Pulse Auto Transformer Converter:

Figure (2.7) shows the 24-pulse system with auto transformer [10, 19]. This approach employs a polyphase autotransformer to provide 30° phase-shifted voltages to rectifier bridges I and 11.

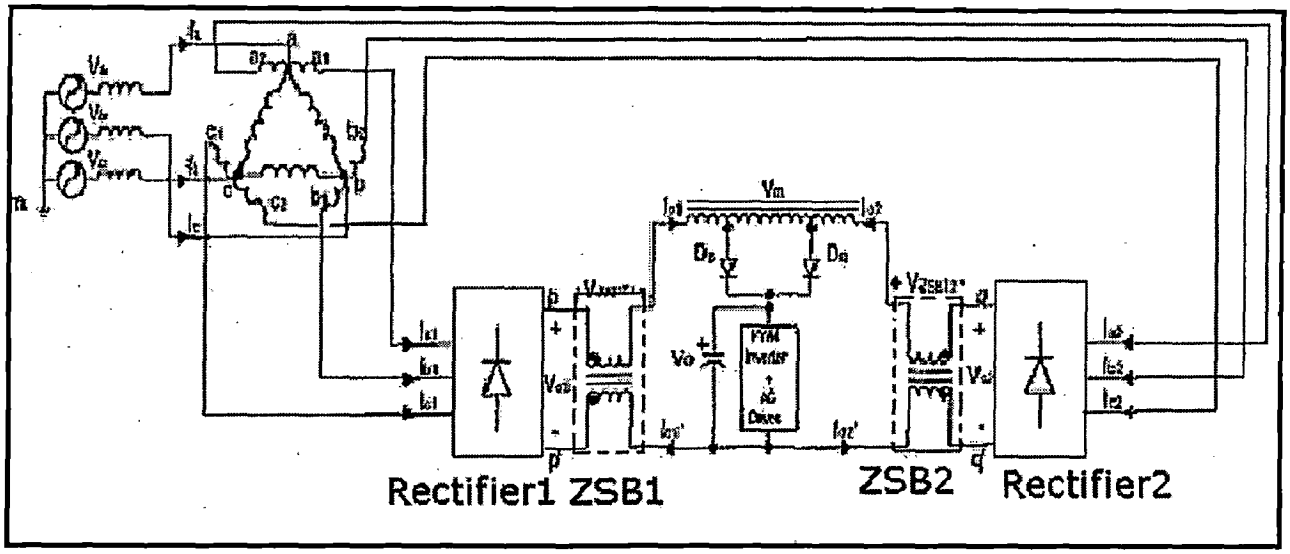

fig. (2.7) Circuit Diagram of 24-Pulse System

The kVA rating of each ZSBT is 3.7% and the interphase reactor is 1.65% of the total output power for the 24-pulse system.

2.2.4.2 24-Pulse Isolated Transformer Converter :

24-pulse system by using isolated transformer can be made by two way first is identical to the conventional 12-pulse isolated system, with some modification in transformer configuration and the two diodes connected to a specially tapped interphase transformer as shown in figure (2.8).

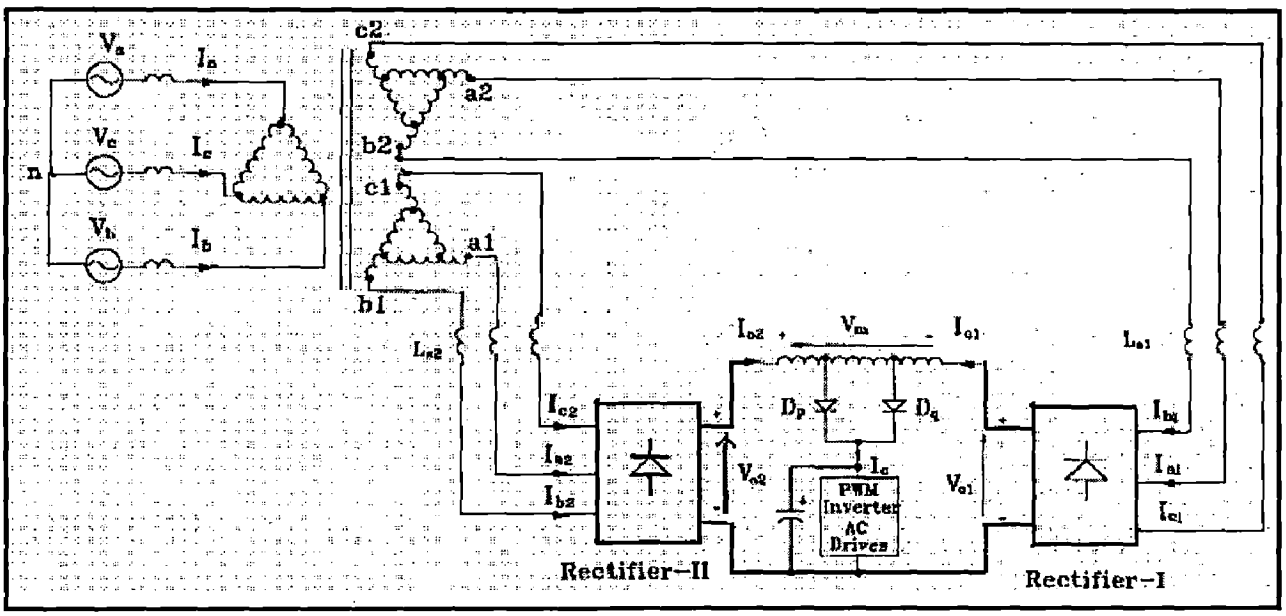

fig. (2.8) Circuit Diagram of 24-Pulse Extended Delta Converter

The secondary windings of the input transformer are configured in extended delta and generate balanced sets of three-phase voltages with 30° phase shift for the diode rectifiers. The extended delta arrangement provides equal leakage reactance in series with rectifiers I and II.

The second way of making 24-pulse converter is by using 24-pulse transformer, where primary is connected in delta and 4-phase shifted secondaries are connected to rectifier module [11]. Each secondary is phase shifted by 15° with each other, and with respect to secondary these are phase shifted by +22.5°, +7.5°, -7.5°,-22.5°. Rectifier module is connected to Buck/Boost chopper which control the D.C out put voltage of converter. This controlled D.C output will be fed to PWM Inverter circuit and output of inverter circuit goes to modular motor. The complete approach is shown below in figure (2.9).

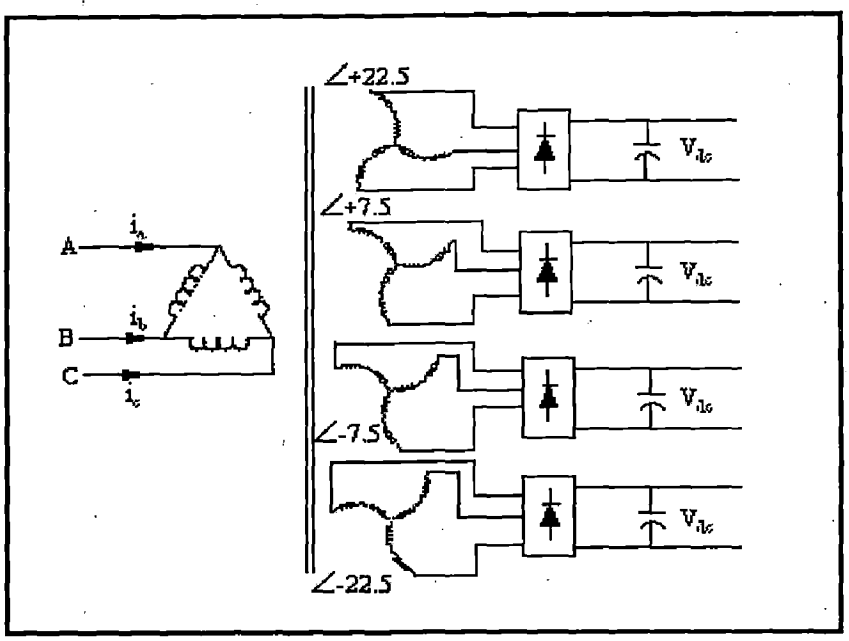

fig. (2.9) 24-Pulse Converter

2.2.5 Improved 12-Pulse Converter :[9]

The multi-pulse and most multilevel arrangements use fundamental frequency modulation because each switch in the converter turns on and off only once per cycle to reduce the switching losses. A ripple reinjection concept has been developed for line-commutated converters which are used to increase the pulse number of the conventional converter units and thus reduce harmonic distortion. Using a similar concept, we can developed a new scheme based on the reinjection of direct voltage pulses at six times the fundamental frequency to reduce the harmonic

content produced by voltage-source converters. An improve 12-pulse converter is shown in figure (2.10).

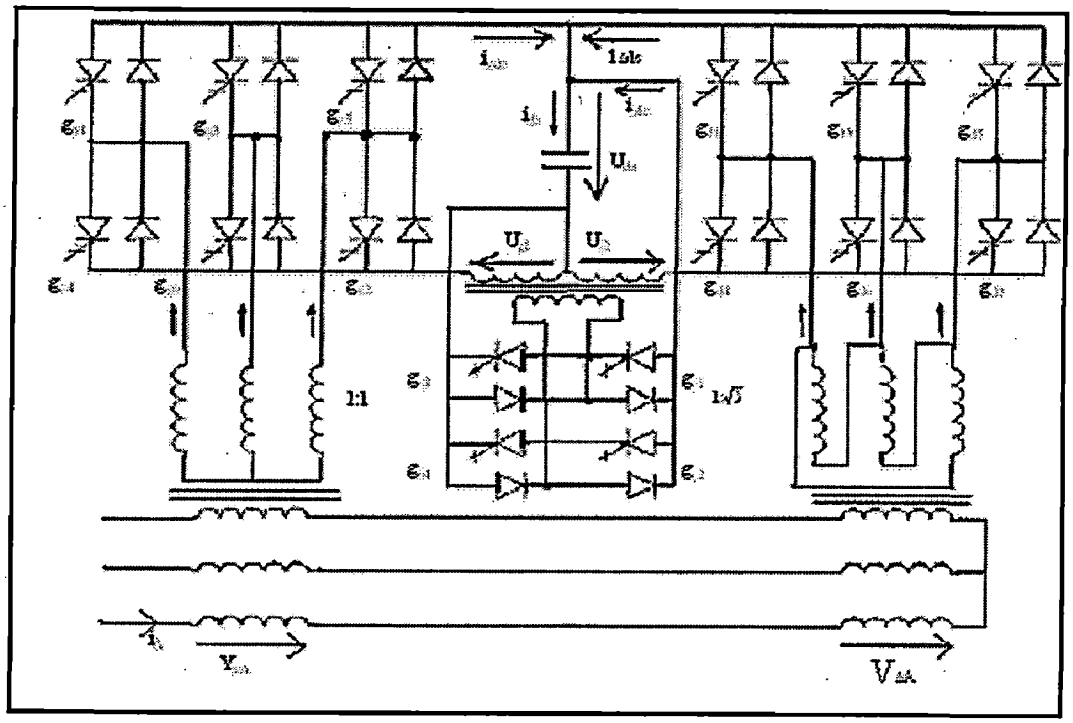

fig (2.10) 36-Pulse Self-Commutated Voltage-Source Converter

The improve harmonic performance is shown in Table-2.1

Table-2.1

Harmonic Order	11	13	23	25	35	37
%THD of Voltage	0.387	0.444	0.251	0.170	2.86	2.70
%THD of Current	0.352	0.341	0.109	0.068	0.816	0.731

Table-(2.1) Harmonic Spectrum of 36-Pulse Converter

24-Pulse AC/DC Buck-Boost Converter

3.1 Introduction:

In modularity concept of Medium-Voltage Adjustable Speed drives, the Single-phase Cascaded (SC) VSI that uses series connection of IGBT based inverter modules with isolated dc-buses for each inverter [12]. The system yields a high-quality multi step voltage with up to 4 levels and low dv/dt, balanced operation of the inverter modules that supply each a fourth of the motor kVA. This modular structure leads to important advantages such as lower cost per kW due to the cheaper IGBT technology, power scalability, built-in redundancy and easy maintenance. Fault tolerance can be achieved by bypassing the fault modules [20,24]. The main drawbacks are high dc-link capacitive energy storage requirement especially in constant torque applications and a special expensive transformer with 24 pulses/l2 windings for ASD, required to provide the isolated dc- buses. The complete drive system is shown in figure (3.1).

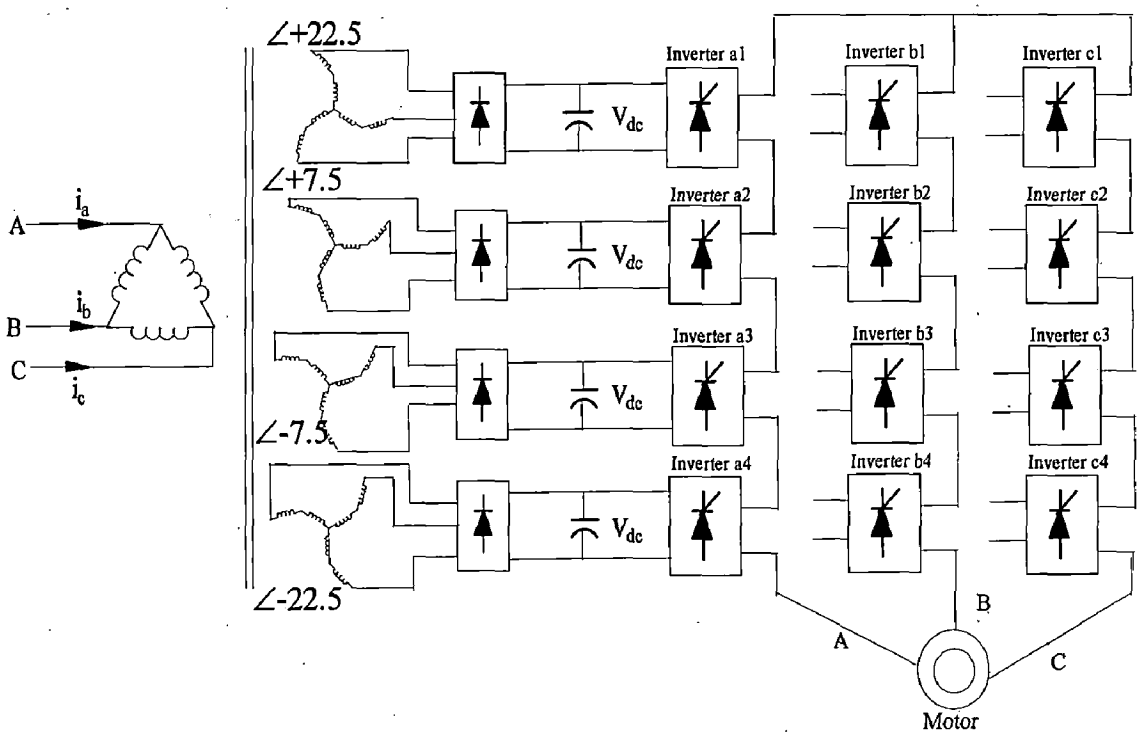

fig. (3.1) Single-Phase Cascaded ASD

So to provide constant DC link voltage for each inverter module this converter is implemented and other objective is to reduce DC link capacitor value, as well as input line current harmonics.

3.2 Design of 24-Pulse Converter :

In this dissertation a 24-Pulse converter is implemented to provide D.C. link voltage to all four inverter module of a single leg. The complete system can be divided in to following three parts

a) Multi-Winding Transformer
b) Rectifier Modules
c) Chopper Circuit
d) Control Circuit

3.2.1 Multi-Winding Transformer :

A multi-winding transformer is used in system to developed four secondary, which are used to feed AC supply to four rectifier module [22]. The transformer has four three phase secondary windings each winding voltage is phase shifted from each other by an angle of 15^0. The criterion for deciding the phase angle is as follows.

360/pulse number = phase shift in degree

Table 3.1 represents the pulse number and the respective phase shift on the basis of this criterion.

Table- (3.1)

Pulse Number	Phase shift	Phase Shifting Angles
12	30	0^0,30^0
18	20	20^0,0^0,-20^0
24	15	$+22.5^0$,$+7.5^0$,$+7.5^0$,$+22.5^0$
30	12	24^0,12^0,0^0,-12^0,24^0

Table (3.1) Number of Pulse and Phase Shift

Transformer is used to convert three-phase AC power to phase shifted four 3-phase AC power module. it helps in providing reduced harmonics on the AC side and minimizing ripple on the DC side of an AC to DC rectifier.

These AC phases are phase-shifted by each other by 15° and with respect to primary these are phase shifted by an angle of +22.5°, +7.5°,-7.5^0 and -22.5° respectively. It is designed in such a way that all line to line three phase output voltage will be equal in magnitude and phase shifted from the input voltage by these angles and these are phase shifted from each other by an angle of 15^0. Figure (3.2)

shows the winding diagram for phase shifting transformer. First winding is phase shifted +22.5°, second +7.5° phase shifted third -7.5° phase shifted and fourth is -22.5° phase shifted. All the windings are phase shifted from each other by an angle of 15°.

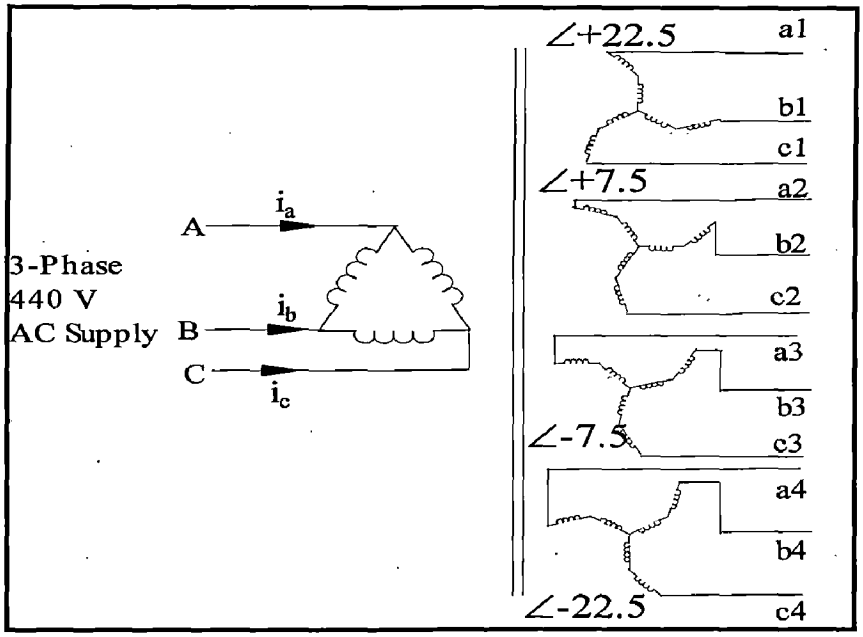

fig (3.2) Winding Diagram of Phase Shifting Transformer

From figure (3.2) it is clear that secondaries of transformer are connected in such a way that they give required phase shift i.e. +22.5°, +7.5°,-7.5° and -22.5°.

3.2.1.1 Connection for +22.5° Phase Shifted Winding :

Figure (3.3) shows the connection diagram for +22.5° phase shift. To get +22.5° phase shift some number of turns of one phase is added with some number of turns of other phase to get the desired phase shift . For +22.5° phase shift for the desired voltage in A phase, 69 turns of phase A are added with 43 turns of phase C . Similarly in phase B 69 turns of phase B are added with 43 turns of phase A and in phase C 69 turns of phase C are added with 43 turns of phase B.

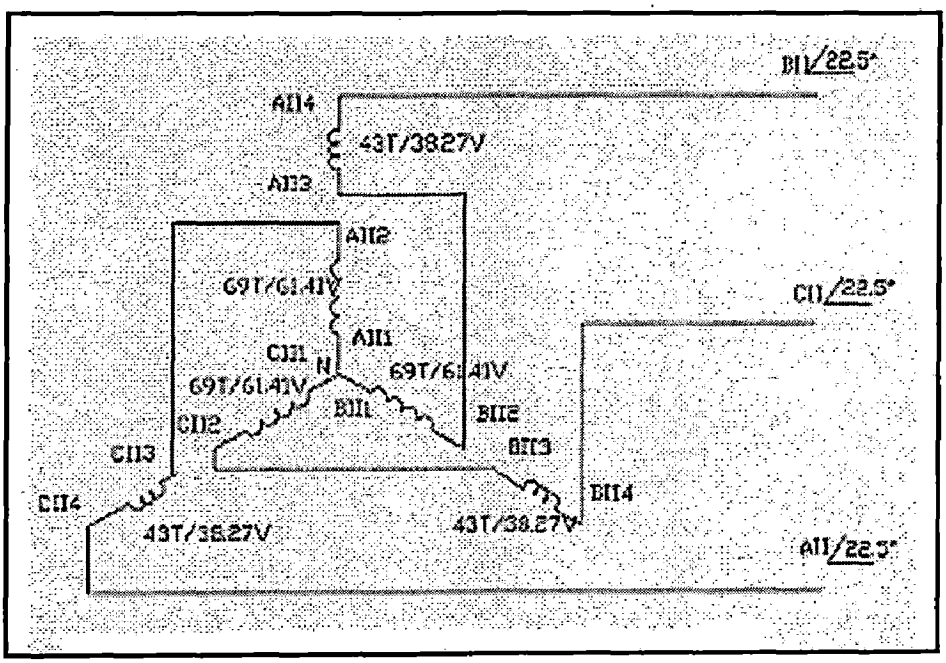

fig (3.3) Connection Diagram for +22.5° Phase Shift

3.2.1.2 Connection for +7.5° Phase Shifted Winding:

Figure (3.4) shows the connection diagram for +7.5° phase shift. To get +7.5° phase shift some number of turns of one phase is added with some number of turns of other phase to get the desired phase shift . For +7.5° phase shift for the desired voltage in A phase, 90 turns of phase A are added with 15 turns of phase C . Similarly in phase B 90 turns of phase B are added with 15 turns of phase A and in phase C 90 turns of phase C are added with 15 turns of phase B.

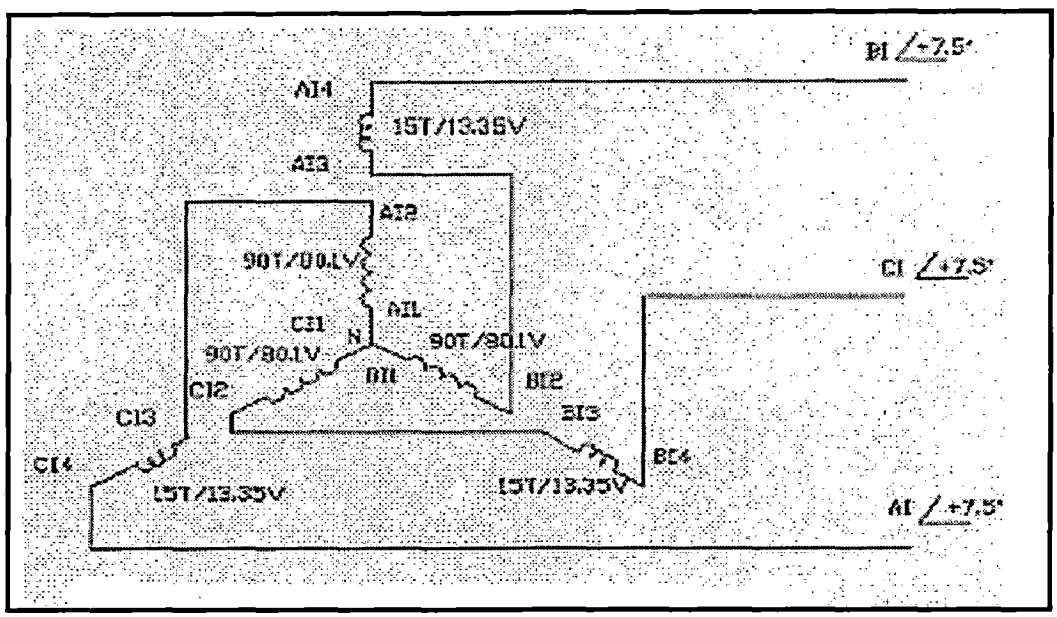

fig (3.4) Connection Diagram of +7.5° Phase Shift

3.2.1.3 Connection for -7.5° Phase Shifted Winding:

Figure (3.5) shows the connection diagram for -7.5 ° phase shift. To get -7.5° phase shift some number of turns of one phase is added with some number of turns of other phase to get the desired phase shift . For -7.5° phase shift for the desired voltage in A phase, 90 turns of phase A are added with 15 turns of phase B. Similarly in phase B 90 turns of phase B are added with 15 turns of phase C and in phase C 90 turns of phase C are added with 15 turns of phase A.

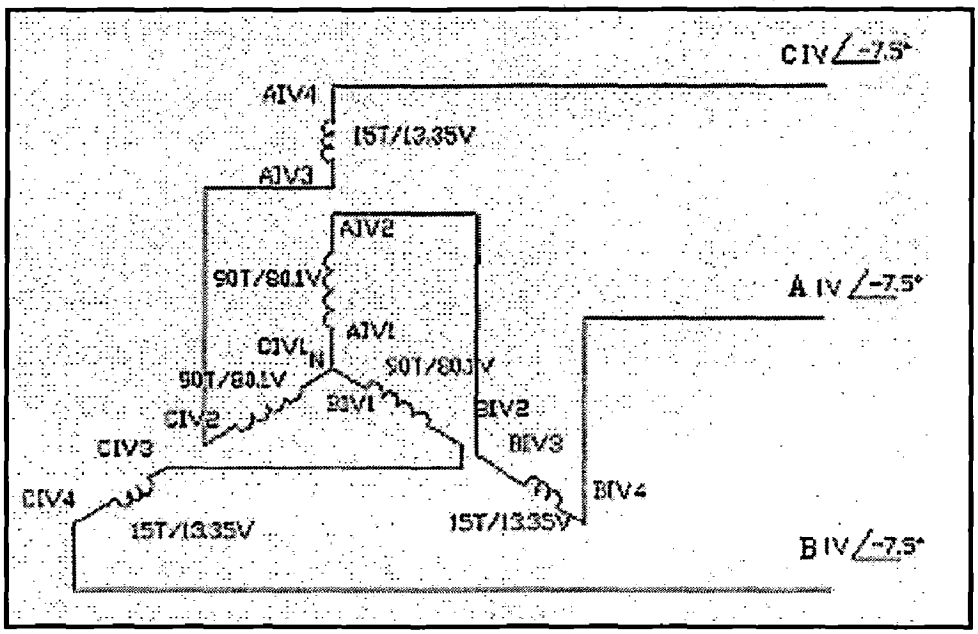

fig (3.5) Connection Diagram for -7.5 ° Phase Shift

3.2.1.4 Connection for Getting -22.5° Phase Shift :

Figure (3.6) shows the connection diagram for -22.5 ° phase shift. To get -22.5° phase shift some number of turns of one phase is added with some number of turns of other phase to get the desired phase shift . For -22.5° phase shift for the desired voltage in A phase, 69 turns of phase A are added with 43 turns of phase B . Similarly in phase B 69 turns of phase B are added with 43 turns of phase C and in phase C 69 turns of phase C are added with 43 turns of phase A.

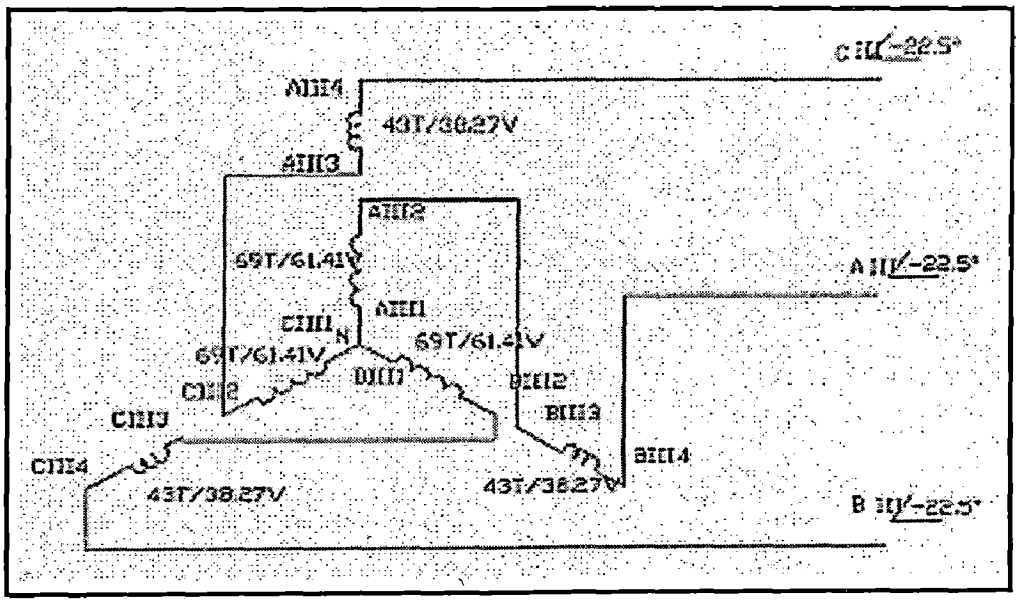

fig (3.6) Connection Diagram for -22.5° Phase Shift

3.2.2 Rectifier Modules:

An ordinary 3-phase diode bridge rectifier is used for developing rectifier modules. 24- pulse converter consists of four such type of rectifier modules which are connected to four secondaries winding of transformer. Single unit of rectifier system is shown in figure (3.7a) and complete rectifier system is shown in figure (3.7b).

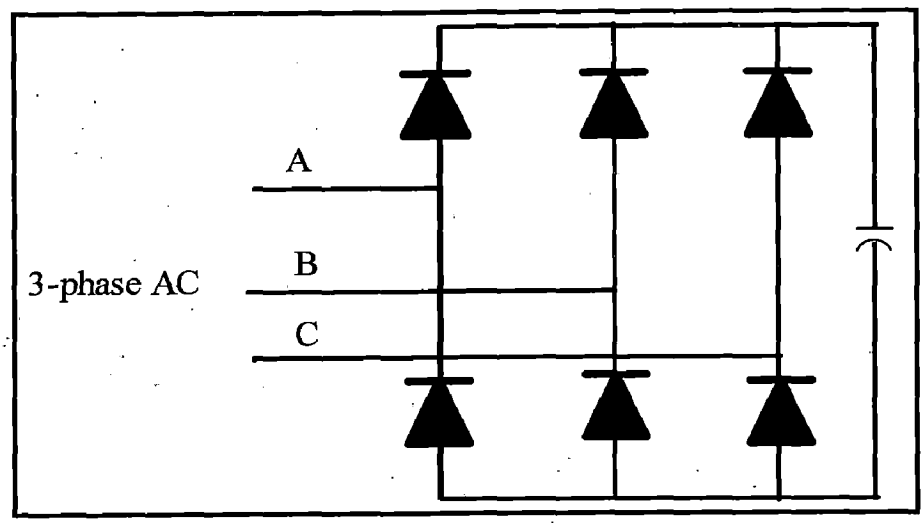

fig. (3.7a) 3-Phase Rectifier

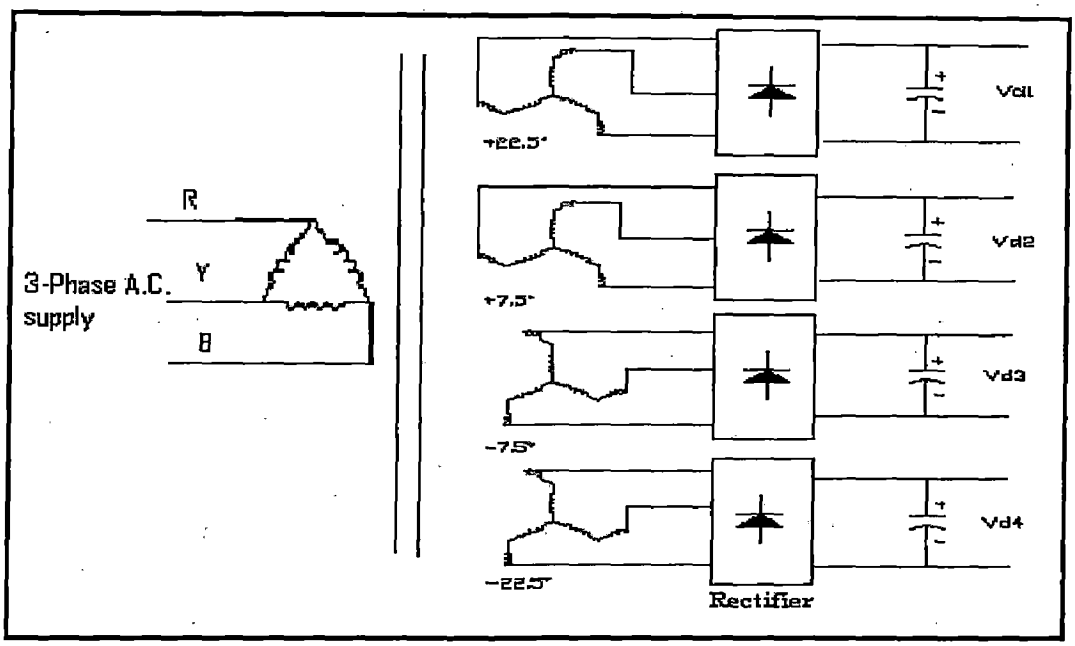

fig. (3.7b) Complete Rectifier System

3.2.3 Chopper Circuit :

The buck-boost chopper is dc to dc converter, it is used to maintain constant dc link voltage. The complete buck-boost is shown in figure (3.8) [13,14]. The chopper operates in three modes buck ,boost and ideal, depending upon the chopper input voltage. If output voltage goes high chopper operates in buck mode, if output voltage of chopper goes below desired level then chopper operates in boost voltage to make output voltage constant, if the output voltage is within certain limit then chopper operates in ideal mode that is what soever the input voltage of the chopper that will appear at the output.

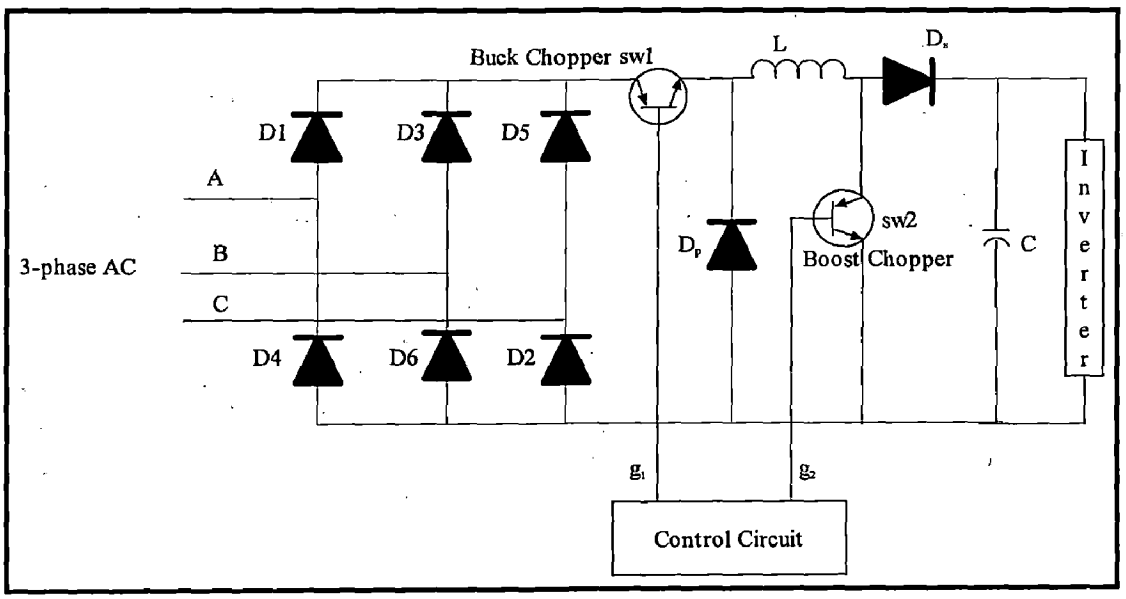

fig (3.8) Buck-Boost Chopper Rectifier

3.2.3.1 Buck Chopper :

The buck chopper, also known as the step-down chopper because it produces an output voltage less than the input voltage. The ideal buck converter has the four basic components, namely a power semiconductor switch, a diode, an inductor, and a controller circuit to provide gating pulse to semiconductor switch. The basic circuit of the buck converter is shown in the figure (3.9). Buck operation of chopper can be easily understand with the help of figure (3.10), as voltage across the capacitor goes high to the desired level sw1 get open for the period of T_{OFF} and get closed for the period of T_{ON}. During T_{ON} inductors gets charged and store the energy and during T_{OFF} it dissipates the store energy through load and freewheeling diode. Since T_{ON} is less then T_{OFF} hence store energy is less as compared to dissipated energy hence voltage goes down and come to desired set level. Figure (3.10) shows the equivalent circuit during switch on and off condition.

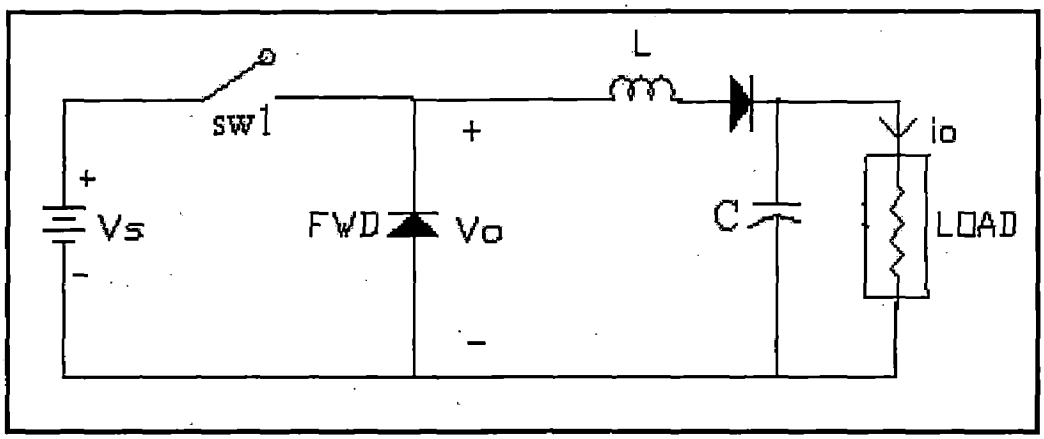

fig. (3.9) General circuit for Buck Chopper

To analyse the voltages of this circuit when the switch is closed let us consider the changes in the inductor current over one cycle. From the relation

$$Vs - Vo = L\frac{di}{dt}$$

the change of current satisfies

$$di = \int_{on} (Vs - Vo)dt + \int_{off} (Vs - Vo)dt$$

For steady state operation the current at the start and end of a period T will not change. To get a simple relation between voltages we assume no voltage drop across transistor or diode while ON and a perfect switch change. Thus during the ON time Vs = Vo and in the OFF Vs = 0. Thus

$$0 = di = \int_{0}^{Ton} (Vs - Vo)dt + \int_{Ton}^{Ton+Toff} (-Vo)dt$$

This simplifies to

$$(Vs - Vo)T_{on} - Vo * T_{off} = 0$$

or

$$\frac{Vo}{Vs} = \frac{Ton}{T}$$

Output Voltage is given by $V_O = \alpha V_S$

Where T_{OFF} = off -time

T_{ON} = on-time

$T = T_{OFF} + T_{ON}$ = Total Time Period

Where $\alpha = T_{on}/T$ = Duty cycle.

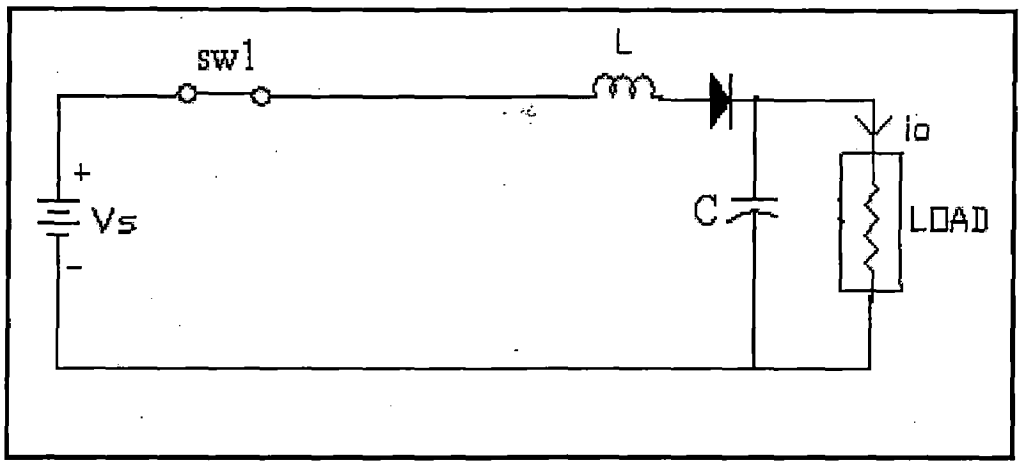

fig. (3.10a) Equivalent Circuit of Buck Chopper During T_{ON} Period

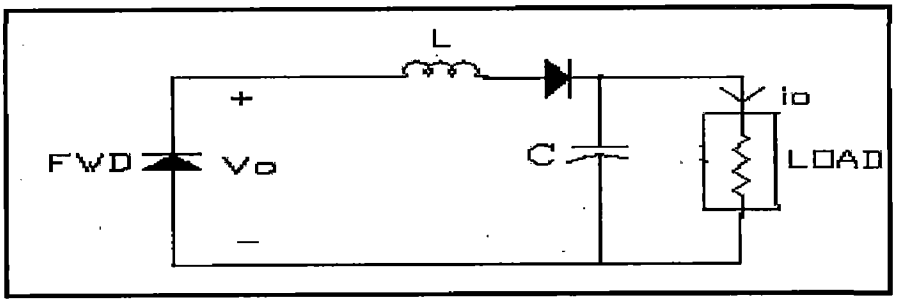

fig. (3.10b) Equivalent Circuit of Buck Chopper During T_{OFF} Period

3.2.3.2 Boost Chopper :

The boost chopper, also known as the step-up chopper because it produces an output voltage greater than the input voltage. The ideal boost converter has the four basic components, namely a power semiconductor switch, a diode, an inductor, controller circuit to provide gating pulse to semiconductor switch. The basic circuit of the boost converter is shown in the figure (3.11).

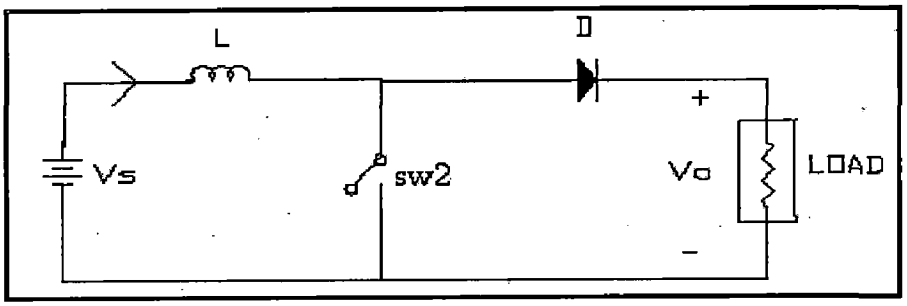

fig. (3.11) General Circuit For Boost Chopper

When the switch is ON as shown in figure (3.12a), the current through the inductor increases and hence the energy stored in the inductor also increased and when the switch is off as shown in figure (3.12b), current through the inductor continues to flow via the diode D and back to source. The inductor is discharging its energy and the polarity of inductor voltage is such that its terminal connected to the diode is positive with respect to its other terminal connected to the source. It can be seen that the inductor acts like a pump, receiving energy when the switch is closed and transferring it to the load when the switch is open.

When chopper is ON source voltage is applied to inductor i.e. $V_L=V_S$.When chopper is OFF, applying KCL to circuit figure (3.12b) gives

$V_L-V_O+V_S=0$ i.e. $V_L=V_O-V_S$

Assuming linear variation of output current the energy input to inductor from during T_{ON} is

W_{ON} = (inductor voltage)*(average current through inductor)*T_{ON}

$W_{ON}=Vs*((I_1+I_2)/2)*T_{ON}$

Where I_1 and I_2 are the current through inductor when switch is on and off respectively

During T_{OFF} energy is released by the inductor

W_{OFF} = (voltage across L) *(average current through inductor)*T_{ON}

W_{OFF} = (Vo-Vs)*((I_1+I_2)/2))*T_{OFF}

Considering lossless system two energies should be equal

i.e. Vs*((I_1+I_2)/2)* T_{ON} = (Vo-Vs)* *((I_1+I_2)/2)* T_{OFF}

V_O = Vs (T/(T-T_{ON})) = Vs (1/1-α)

Where α = T_{ON}/T = duty cycle

Thus final output voltage is Vo = V_S / (1- α)

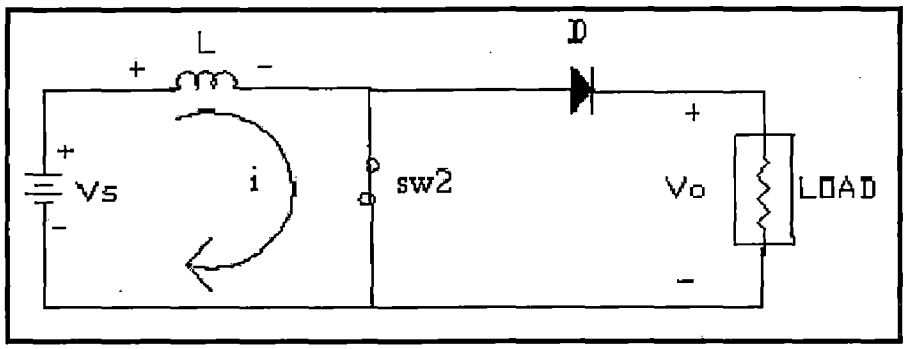

fig. (3.12 a) Equivalent Circuit of Boost Chopper During T_{ON} Period

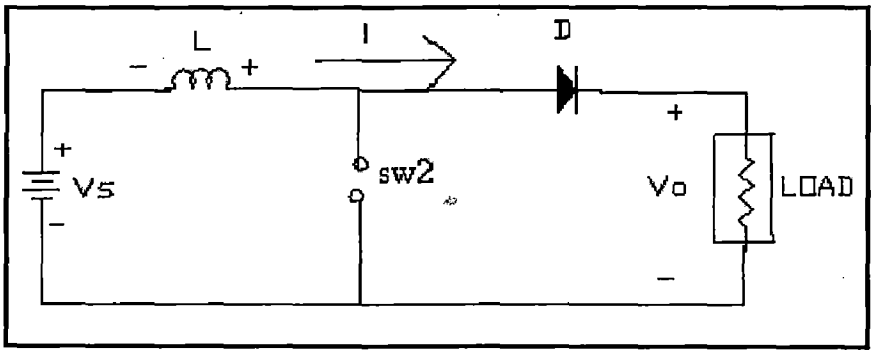

fig. (3.12 b) Equivalent Circuit of Boost Chopper During T_{OFF} Period

3.2.3.3 Filter Circuit:

In buck-boost mode of operation a series inductor is used which not only helps in boosting the output voltage in conjunction with switching device but also serves as filter circuit with parallel capacitors. This filter circuit helps in reducing the output DC ripple content. The dc link inductor smoothens out the output current and makes the current continuous in the circuit. Hence the large value of inductance is connected in the dc link of the system. Capacitor doesn't allow the output voltage to change instantaneously and thus besides minimizing the dc ripple it also serves for the protection of entire electronic circuit.

3.2.3.4 Designing Principle of Inductor:

The calculation of inductance value is done using following calculations. Here air cored inductors are used. The equation calculates inductance using well known '*Wheeler's Formula*' used for design of air cored inductors by most of the industries.

$$L\,(\mu H) = \frac{0.8 * (N*A)\ ^2}{(6A) + (9B) + (10C)}$$

Where N = number of turns, A = average coil radius, B = coil length, and C = coil thickness [23]. All dimensions are in inches and the result is micro henries.

The use of this formula results in large dimensions of inductors and can be used for lower ratings only. However for large rating the inductor can be designed using iron cores specifically for this purpose. These values can be calculated as

Maximum ripple current $\Delta I = \frac{V_S * k}{f * L}$

As per design

Maximum Source Voltage = V_S = 160V

Maximum Output Voltage =V_O=100V

Switching frequency=f=1 kHz

Duty Ratio =k=0.431

Maximum Current Rating I = 5A

Ripple Current =ΔI=+/- 20% of I

= 20% of 5A = 1A

1) For maximum ripple current (+/- 20% of rated), for the nominal values of Vs, Vo and f (frequency), the inductor required is calculated as

$$L = \frac{V_S * k}{f * \Delta I}$$

$$\Rightarrow \quad L = \frac{160 \times 0.431}{1 \times 1000} = 68.96\text{mH}$$

2) For the same maximum ripple current, Vs, Vo & inductor of 4.4 mH (used in system) the switching frequency is calculated as

$$\Delta I = \frac{V_S * k}{f * L}$$

$$f = \frac{160 \times 0.431 \times 1000}{1 \times 4.4} = 15.67\ \text{kHz}$$

3.2.4 Control Circuit :

Control Circuit is required to control the output voltage i.e. to maintain the desired level. Control circuit consists of error estimation circuit, pulse generation circuit and protection circuit. These circuits can be explain as fallows:

3.2.4.1 Error estimation Circuit:

Buck-Boost action of the chopper circuit is depends upon the operation of SW1 and SW2. To producing firing pulses for these switches we first calibrate the error of output voltage and desired or reference voltage [15]. Error estimation circuit is basically a continuously programmable PWM Controller, which take the output voltage as a feed back signal and compare it with reference voltage and generate the two error signal for SW1 and SW2 depending upon the difference of these two signals. Another important point to be noted that generated error signal should be such that modulation index should not go beyond 0.8. The block diagram Error estimation controller is shown in figure (3.13).

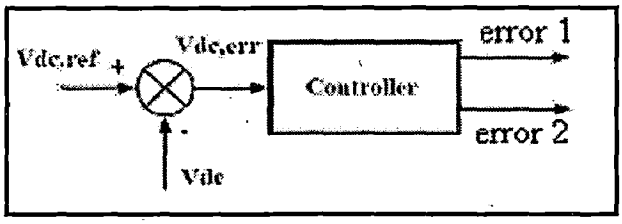

fig. (3.13) Block Diagram of Error Estimator Block

3.2.4.2 Pulse Generation Circuit :

To make turn on the power semiconductor device a gate pulse has to be given to the device. These gate pulse are generated according to the logic as shown in table-(3.2)

Condition	Sw1	Sw2
Output Voltage< Reference	Permanently ON	Operate According to Pulses
Output Voltage> Reference	Operate According to Pulses	Permanently OFF
Output Voltage is within limit	Permanently ON	Permanently OFF

Table (3.2) Logic State of Sw1 and Sw2

Pulses are generated by comparison of error signal with triangular carrier. The complete scheme is shown in figure (3.14).

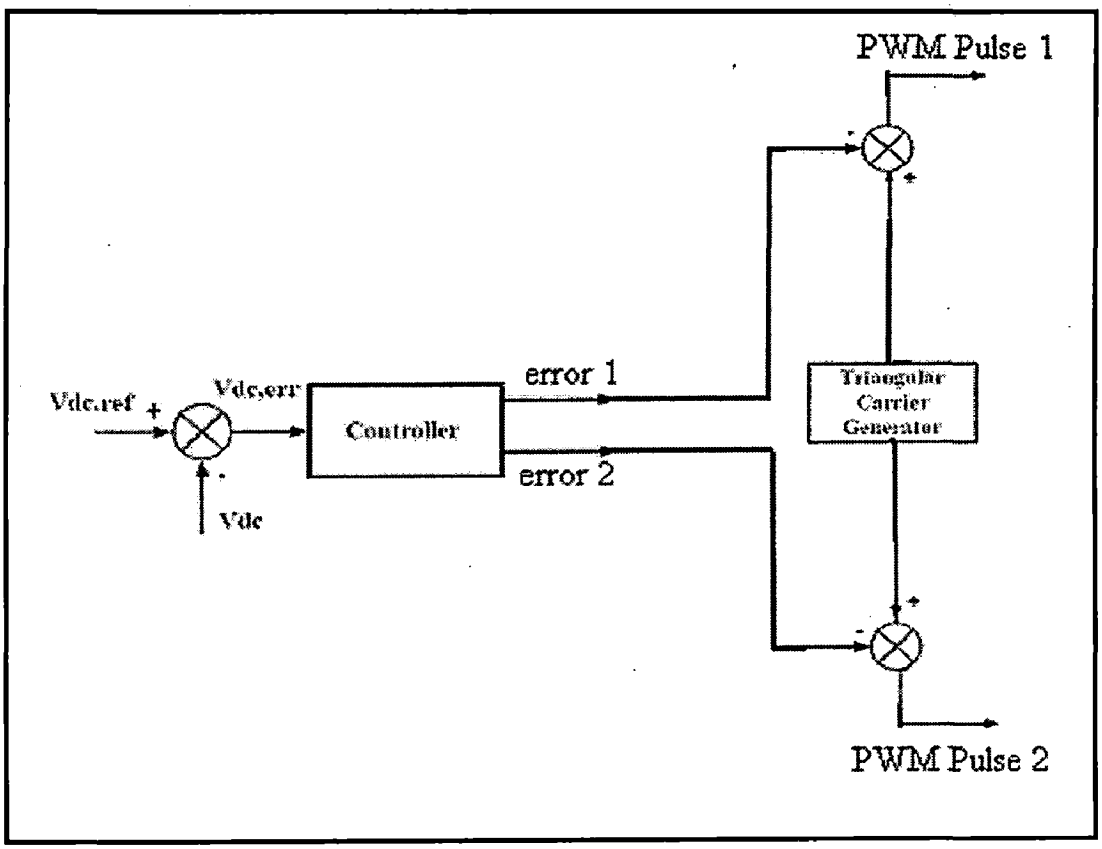

fig. (3.14) Block Diagram of PWM Pulse Generation

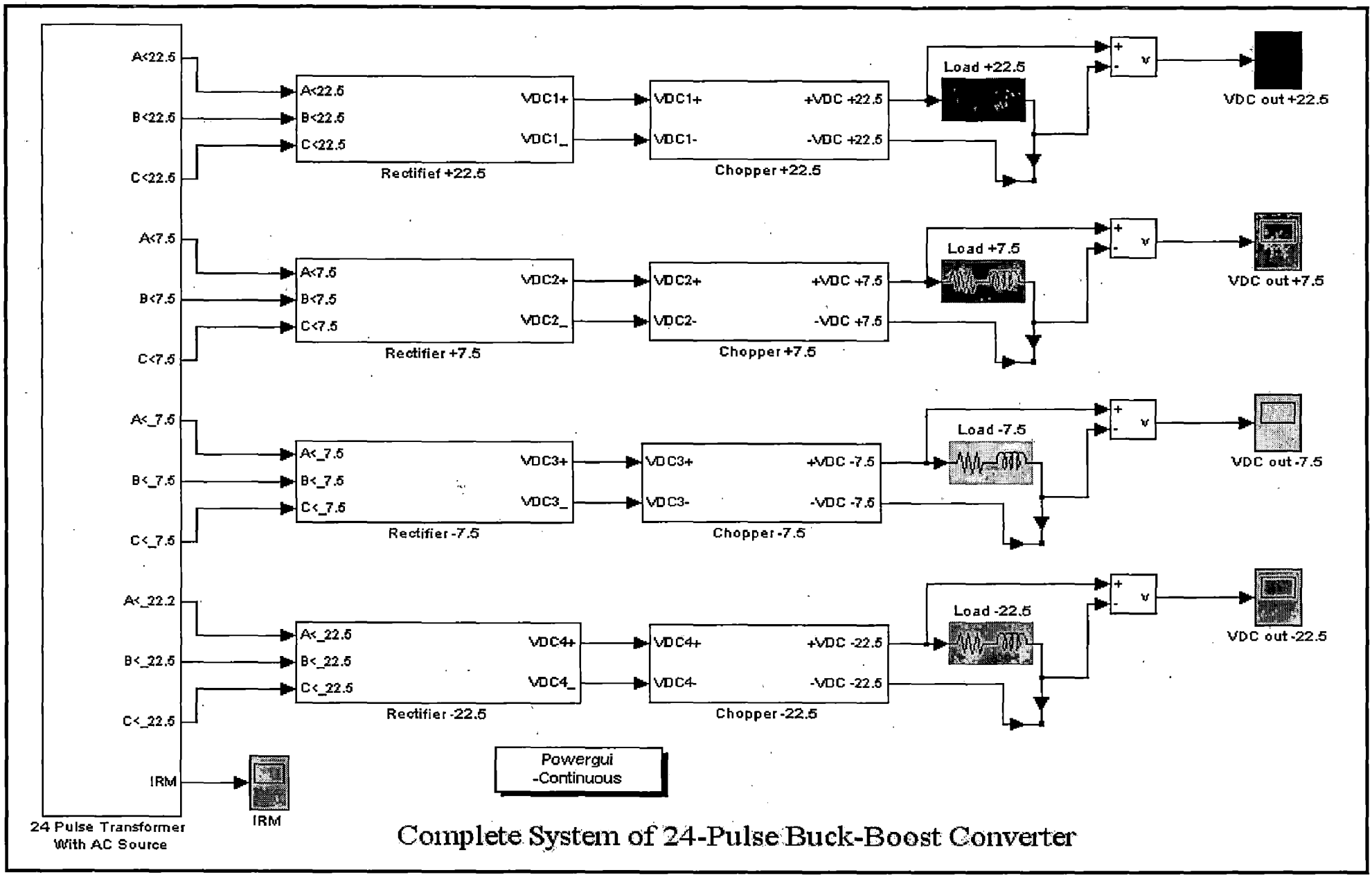

fig. (4.1) Simulated 24-Pulse AC/DC Converter

4.2 24-Pulses Transformer:

Simulated 24-Pulses Transformer is shown in figure (4.2). There are four set of subsystem which represents the primary side connected in delta and four phase shifted star connected secondaries each secondaries is phase shifted with each other by an angle of 15^{o} and from primary it is phase shifted by $+22.5^{0}$, $+7.5^{0}$,-7.5^{0} and -22.5^{0} respectively. All the four subsystem are shown in fig. (4.3). A<22p5 stands for 'A' phase of $+22.5^{0}$ phase shifted secondaries, similarly A<_22p5 stands for 'A' phase of -22.5^{0} phase shifted secondaries. Same for others 'B' and 'C' phases and phase shifting of $+7.5^{0}$ and -7.5^{0}.

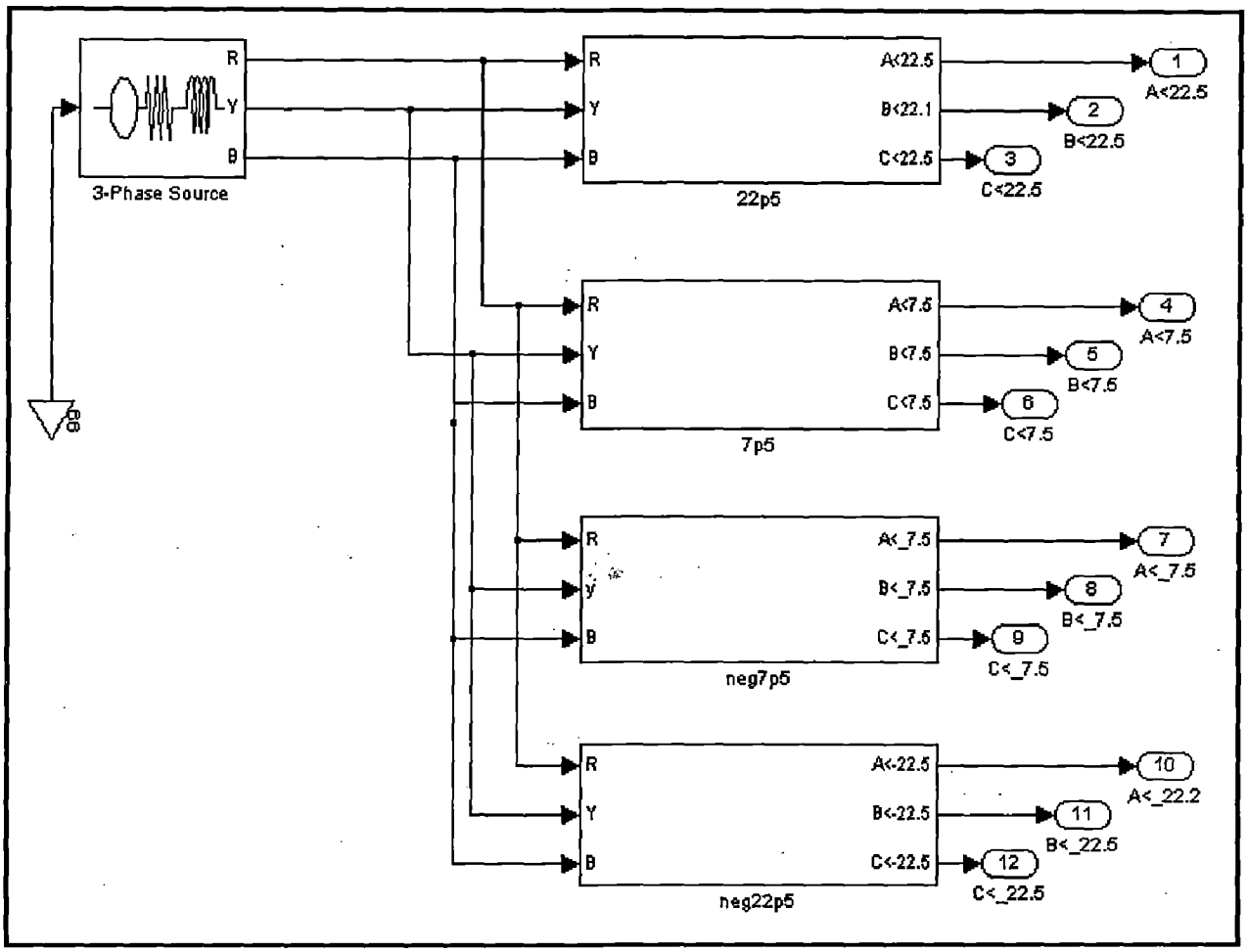

fig. (4.2) Simulated 24-Pulse Transformer

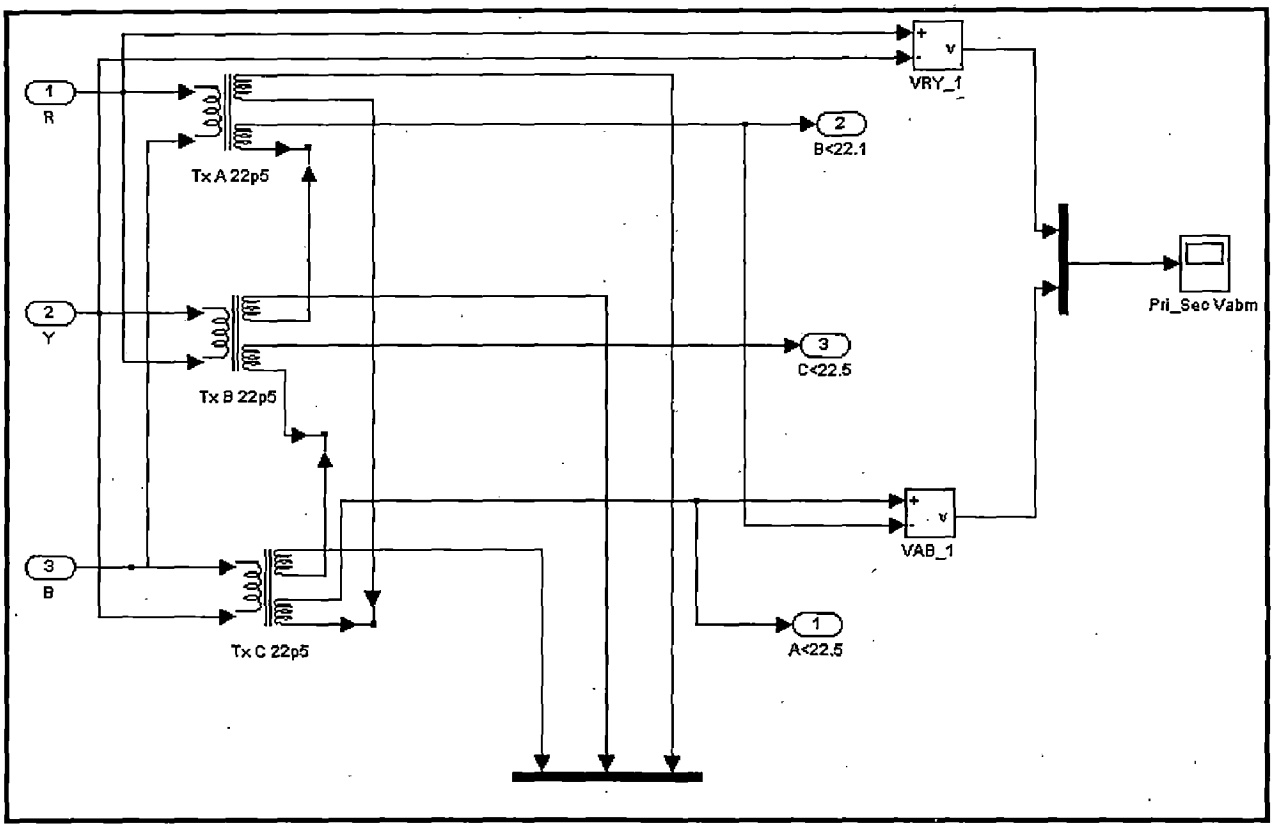

fig. (4.3a) Simulated +22.5^0 Phase Shifted Secondaries

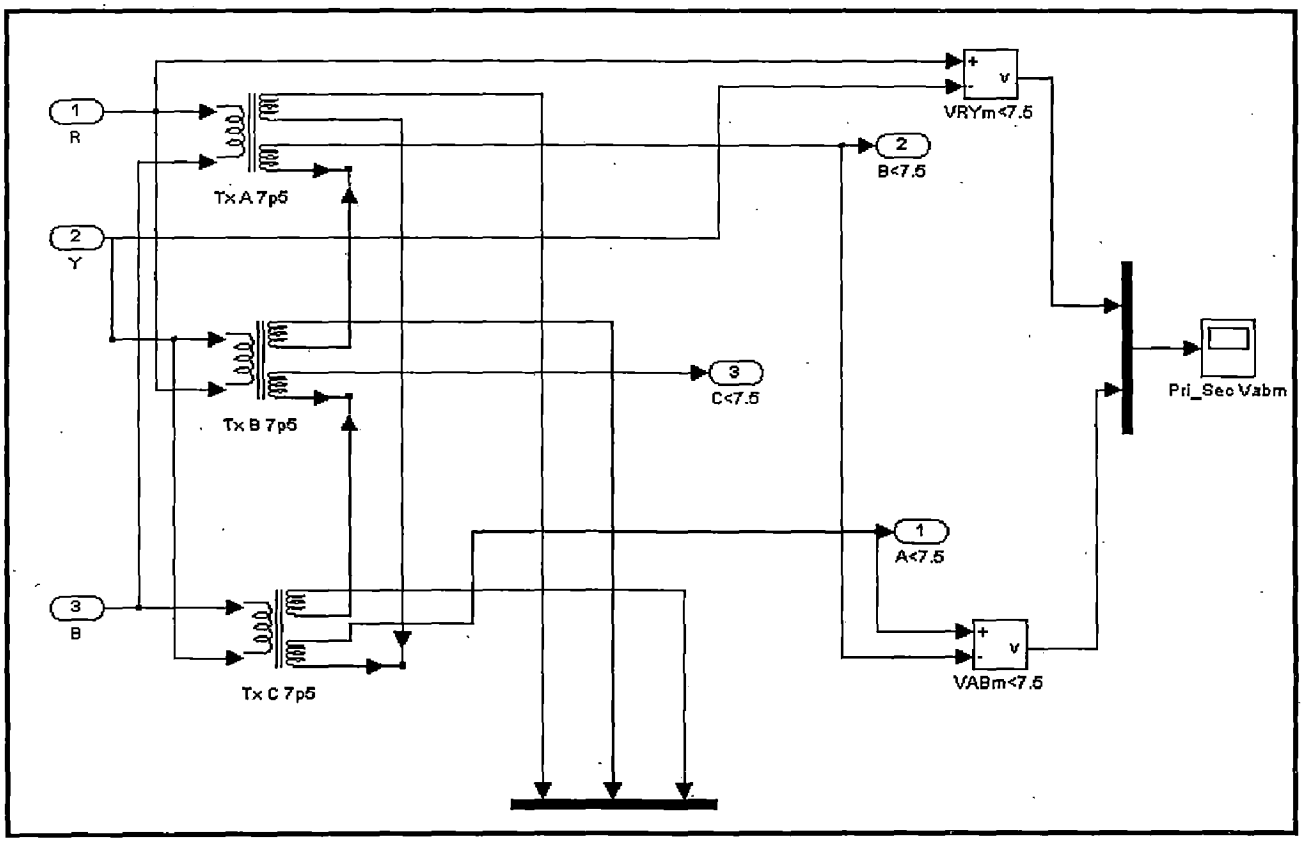

fig. (4.3b) Simulated +7.5^0 Phase Shifted Secondaries

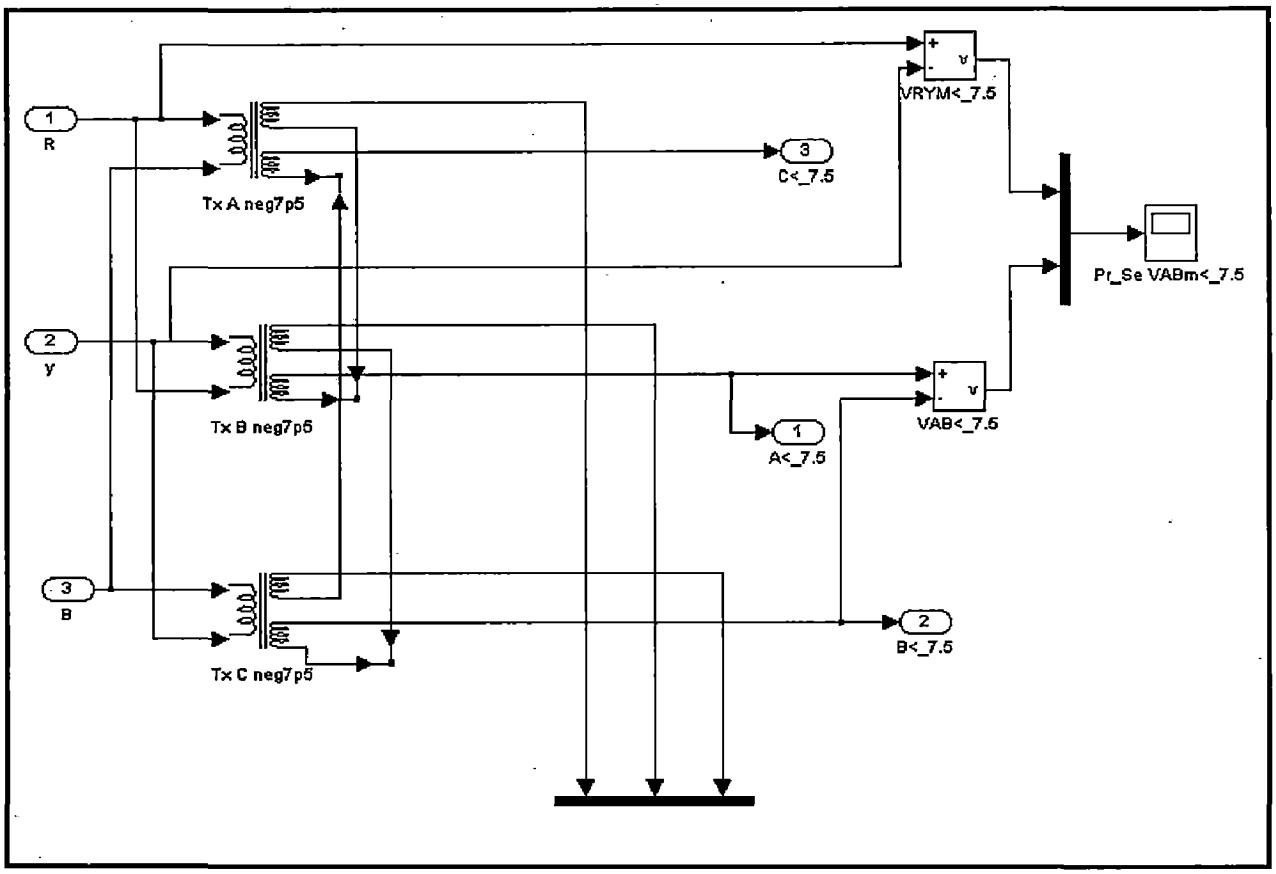

fig. (4.3c) Simulated -7.5^0 Phase Shifted Secondaries

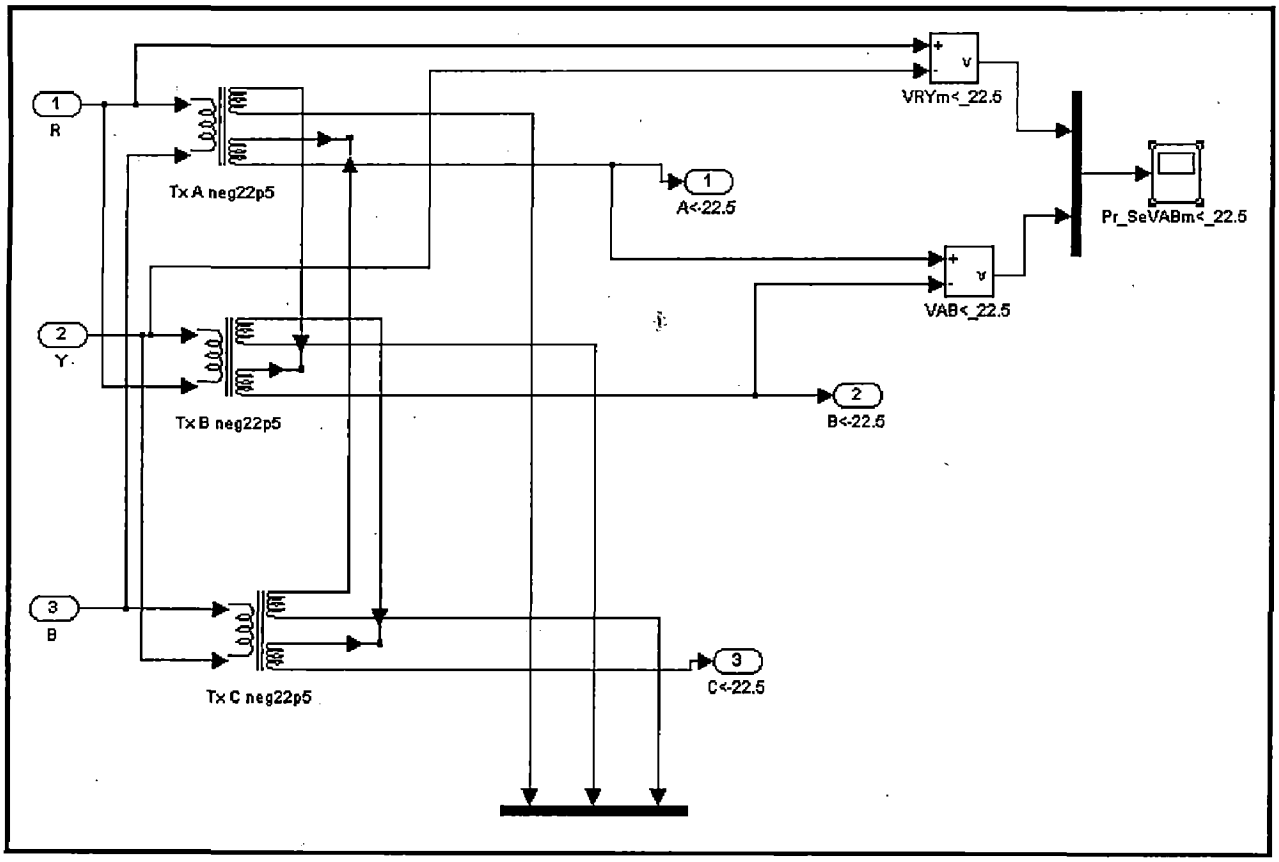

fig. (4.3d) Simulated -22.5^0 Phase Shifted Secondaries

4.3 Rectifier Modules:

After getting four phase shifted secondaries these are connected to rectifier modules. Rectifier modules are made by 3-phase universal bridge available in Sim Power System block set of Simulink. The Simulated rectifier is shown in figure (4.4). At the output of rectifier a capacitor is connected to filter DC ripples. The same type of rectifier module is connected to all the four secondaries.

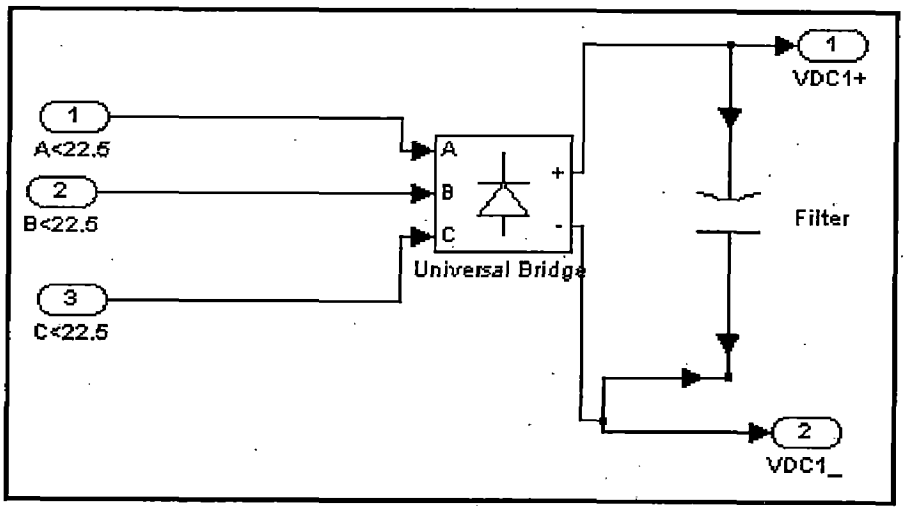

fig. (4.4) Simulated Rectifier Module

4.4 Buck-Boost Converter:

In simulated system figure (4.1) the next block is chopper. A Buck-Boost chopper is simulated in Matlab by using Simulink and Simpower System block set. Output of each DC module is connected to such type of chopper circuit to maintain DC link voltage constant. Buck-Boost chopper contains two devices SW1 and SW2, these devices operated according to buck or boost mode required. The operation of switches is according to Table-(4.1).Block diagram of simulated chopper is shown in figure (4.5).

Table-(4.1).

Condition	SW1	SW2
Output Voltage< Reference	Permanently ON	Operate According to Pulses
Output Voltage> Reference	Operate According to Pulses	Permanently OFF
Output Voltage is within limit	Permanently ON	Permanently OFF

Table-(4.1) Switching State

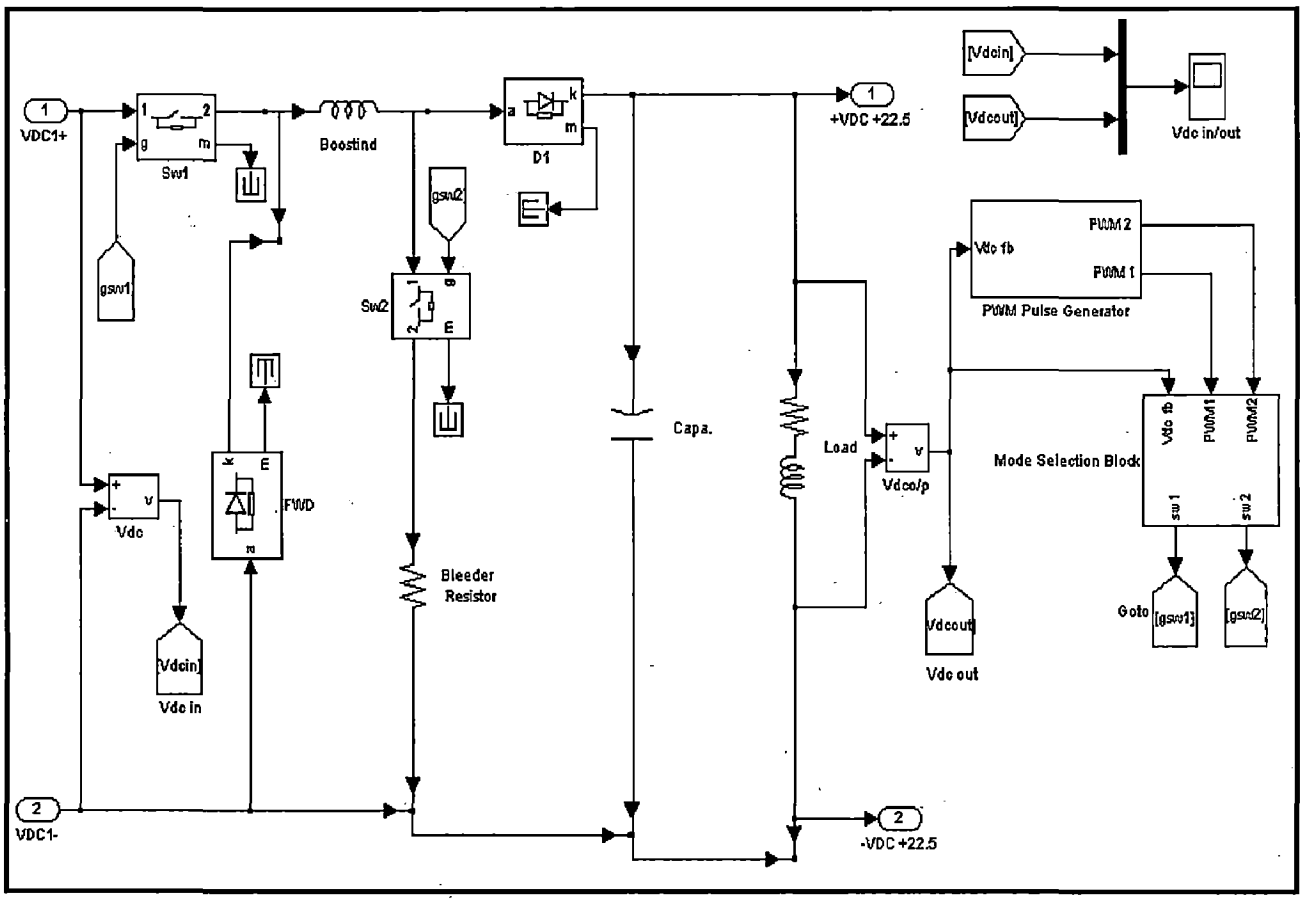

fig. (4.5) Simulated Buck-Boost Chopper

This chopper circuit contain two sub-system blocks which are PWM Pulse Generator and Mode Selection Block. Description of these blocks are as follows :

4.4.1 PWM Pulse Generator:

Firing pulses to operate IGBT is generated by pulse generator system block. The pulse generation block is shown in figure (4.6). This Pulse Generator block contain error estimation block which generates triangular carrier and error signal namely error1 and error2 for SW1 and SW2 respectively. These error signals are compared with triangular carrier and pulses are generated accordingly for SW1 and SW2. When error has magnitude lower than carrier wave, then only comparator output is high, otherwise it is low. The error estimation block takes actual voltage as an input and generates these error signals. The Error Estimation block will be explain in next article (4.4.1.1).

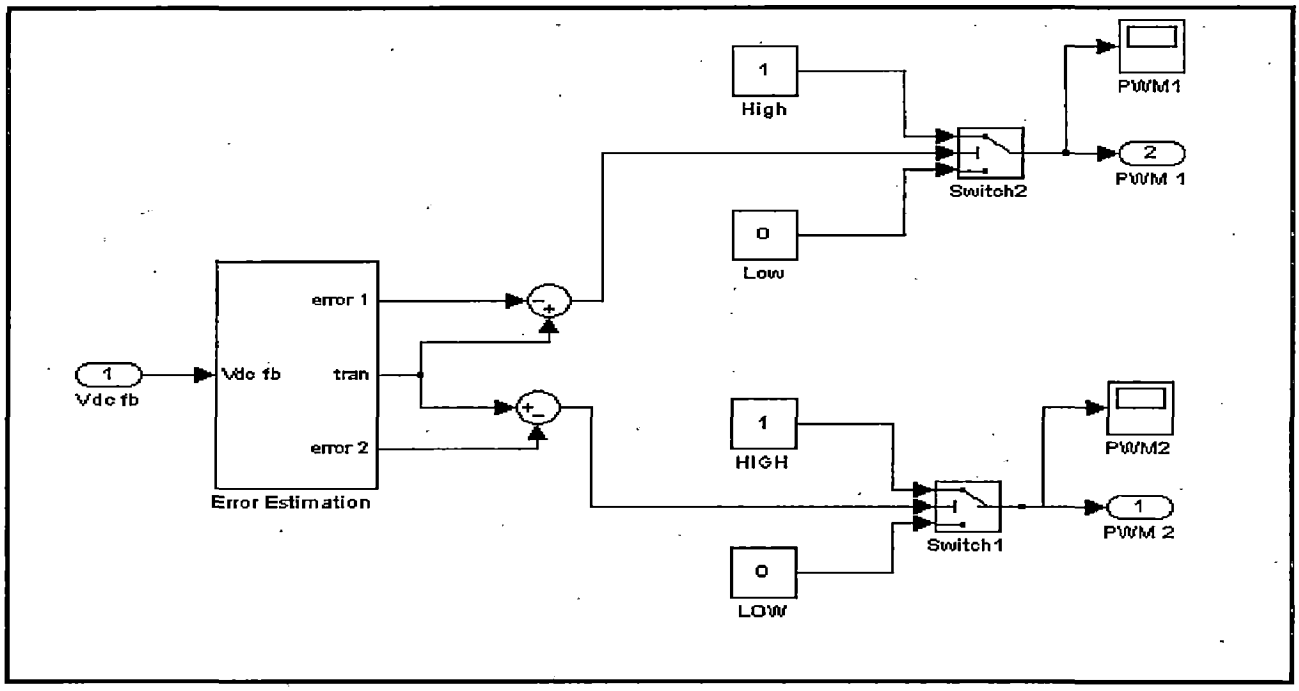

fig. (4.6) Simulated PWM Pulse Generator Block

4.4.1.1 Error Estimation Block:

Error Estimation block takes actual output voltage Vdc fb as a feedback for voltage sensing. After scaling this feed back, error estimation block add some offset and set the gain of this error signal such that it should not disturb the maximum limit of modulation index for SW2 and SW1. Error generation block is shown in figure (4.7a). The triangular carrier is generated by integration of square wave .This synchronized with sin wave and frequency of generated triangular wave is 1kHz. Triangular wave generator is shown in figure (4.7b).

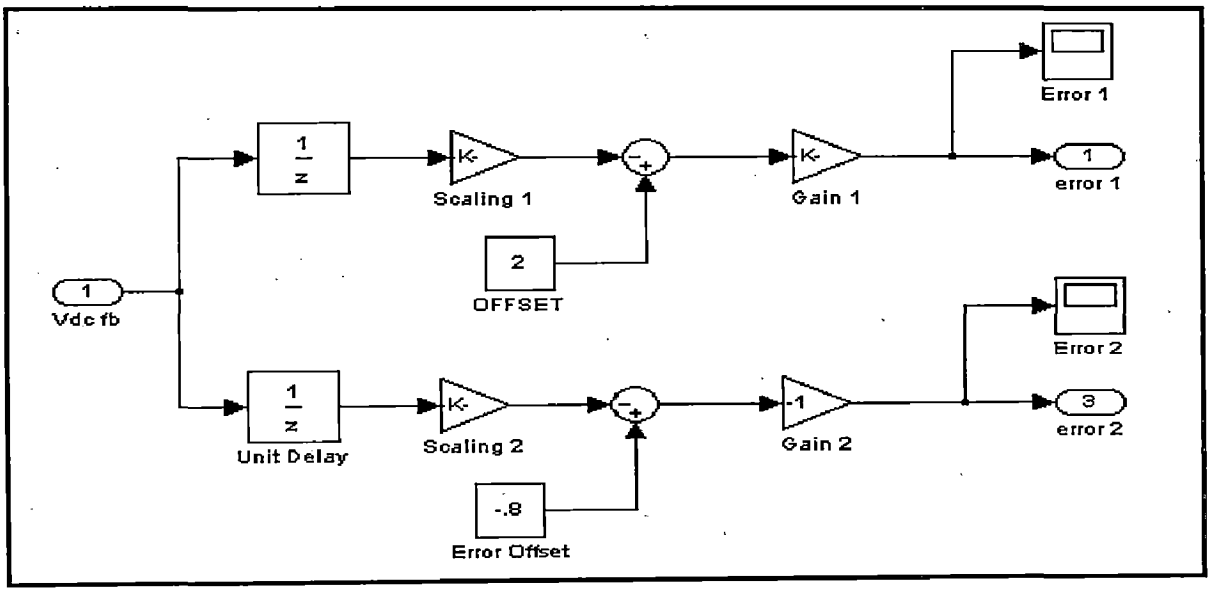

fig. (4.7a) Simulated Error Estimation Block

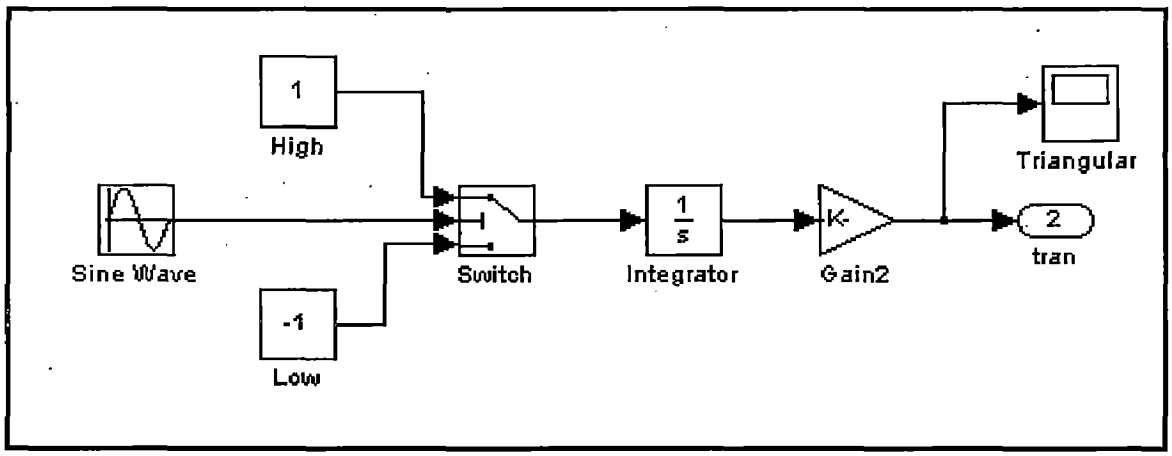

fig. (4.7b) Simulated Triangular Wave Generator Block

4.4.2 Mode Selection Block:

Mood selection logic decides at what instance gate pulse will go to switching device. The actual voltage is compared with a reference voltage, if actual voltage is high then reference then Buck mode will be selected and chopper will operate in buck mode. If actual voltage is low then reference then Boost mode will be selected and chopper will operate in boost mode. The simulated Mode Selection Block is shown in figure (4.8).

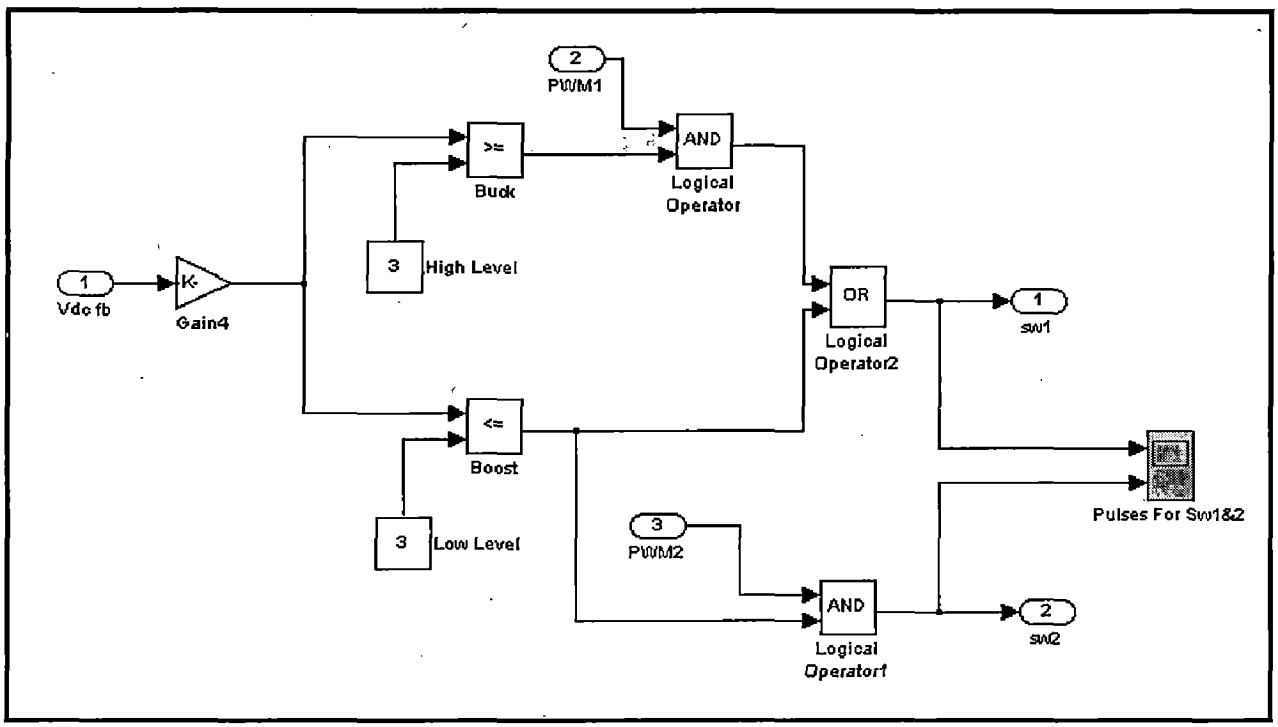

fig. (4.8) Simulated Mode Selection Block

Simulation Results

5.1 Introduction:

In high-power applications, ac–dc converters based on the concept of multi-pulse, namely 12, 18, 24, 30, 36, 48 pulses are used to reduce the harmonics in ac supply currents. These are named as multi-pulse converters [1]. In simulation various type of AC/DC converter are simulated and their voltage and current wave form are studied. THD of input line current of various converter is also studied, tabulated and checked against IEEE-519 standards. Effect of various type of load on converter input current is studied and results are shown in upcoming articles.

5.2 6-Pulse Converter:

A six pulse converter is simulated as shown in figure (5.1). Its harmonic spectrum is calculated by using Power GUI block. Rectifier is loaded with R and R-L load and its input current and input voltage wave forms are recorded by scope, wave forms are shown in figure (5.2 a&b). Simulation parameter are shown in Appendix-A.

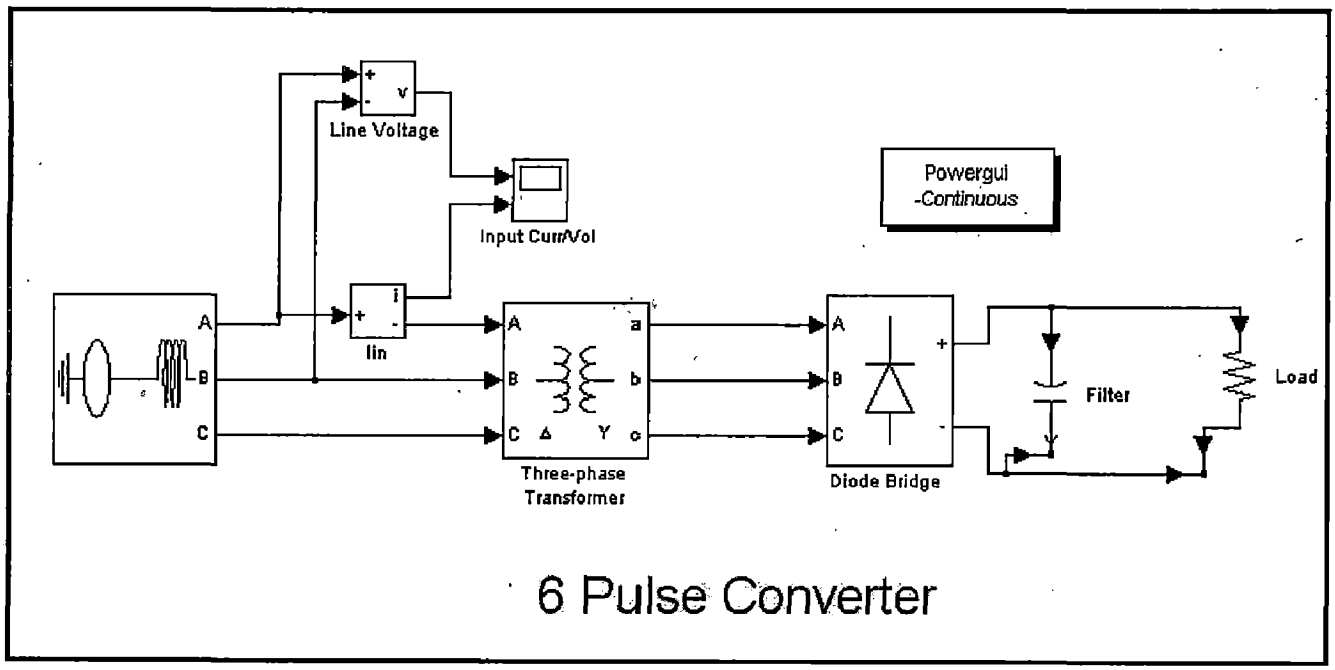

fig. (5.1) Simulated 6-Pulse Converter

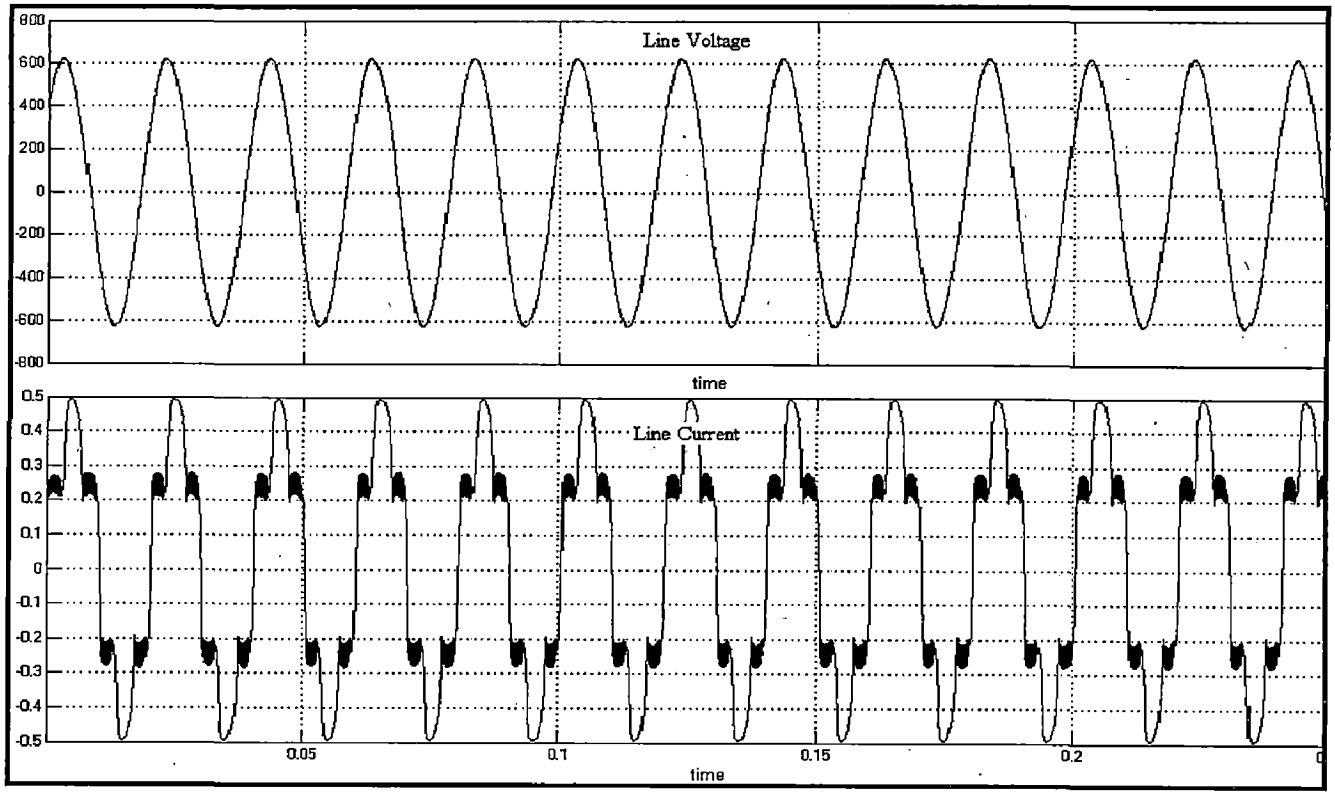

fig. (5.2a) Input Line Voltage and Current Waveform for Resistive Load

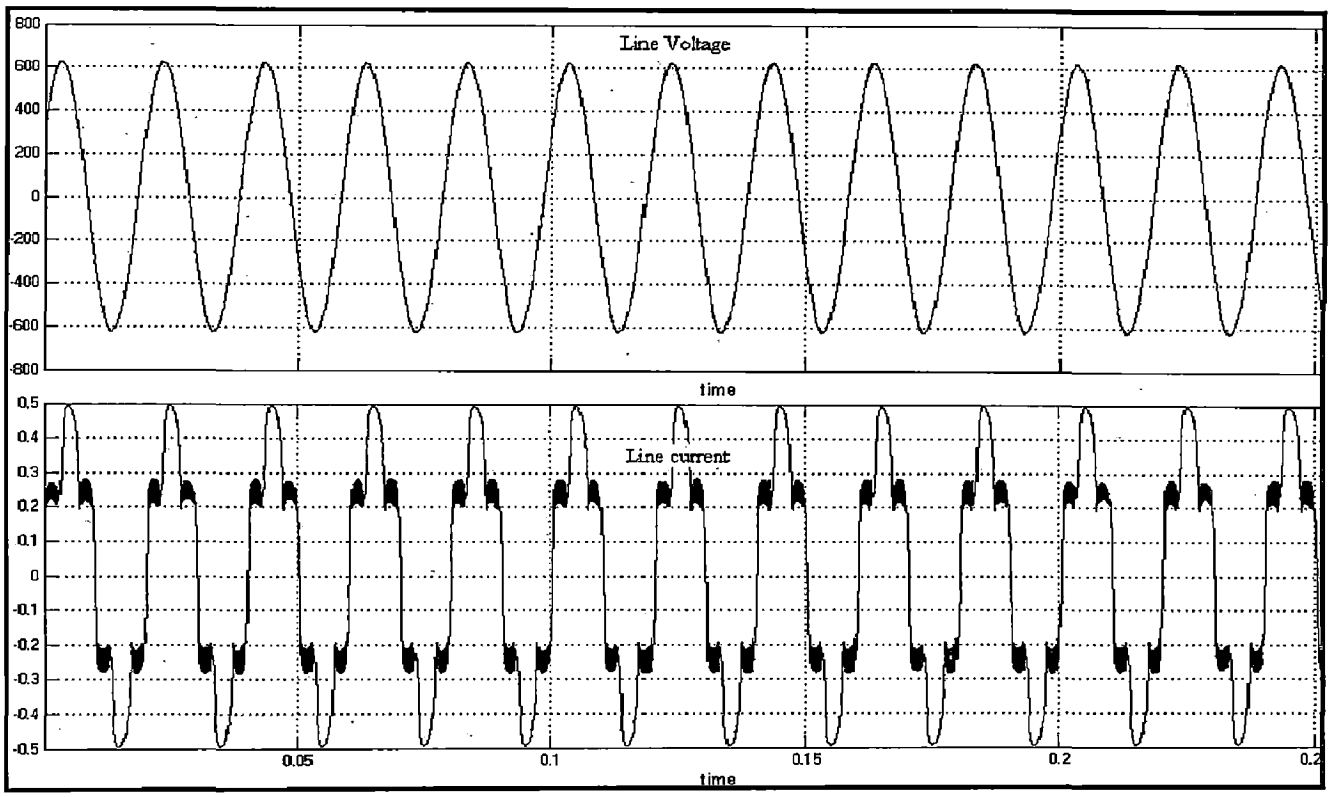

fig. (5.2b) Input Line Voltage and Current Waveform for R-L Load

Harmonic analysis is carried out by using FFT of Power GUI block. FFT spectrum is shown in figure (5.3 a&b) for R and R-L load respectively. THD of input line current is 25.80 % and 25.55 % in case of R and R-L load respectively. Percentage contribution in THD of various order current harmonic is tabulated in Table-(5.1), it can be noted from table that major component is 5^{th} and 7^{th} which are having 22.11 % and 9.30 % in case of resistive load and in case of R-L load it is 22.12 % and 8.94 % of fundamental.

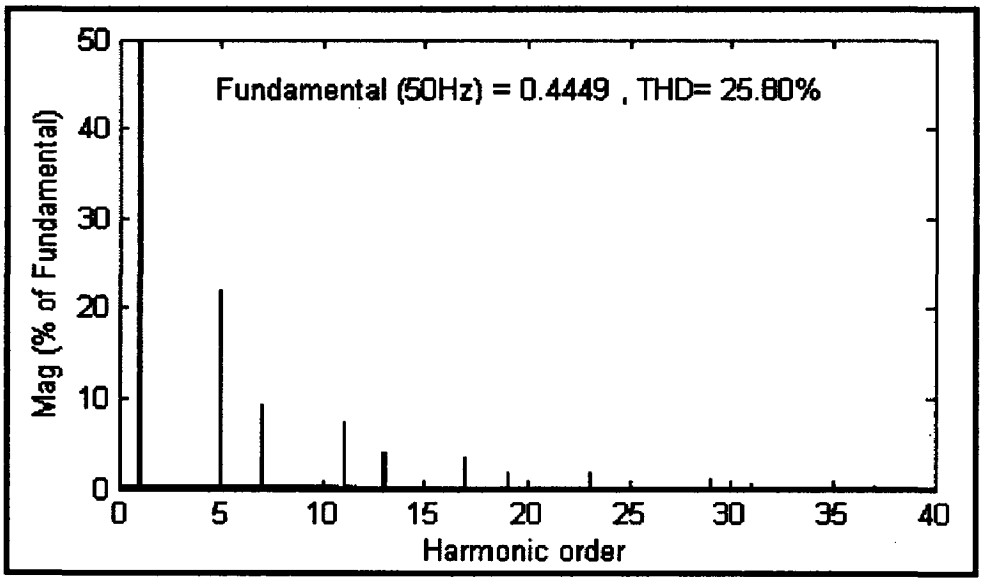

fig .(5.3a) FFT Analysis of Input Current (Resistive Load)

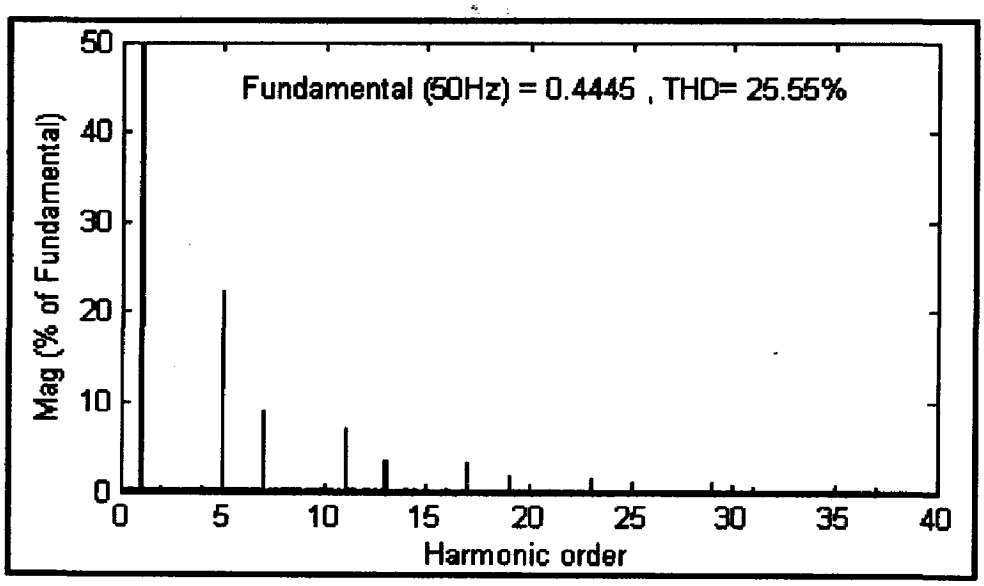

fig .(5.3b) FFT Analysis of Input Current (R-L Load)

Table (5.1)

% of Fundamental Current		
Harmonic Order	Resistive Load	R-L Load
3	.32	.02
5	22.11	22.12
7	9.30	8.94
9	0.26	0.05
11	7.33	7.10
13	3.86	3.58
15	0.18	0.07
17	3.38	3.16
19	1.86	1.76

Table (5.1) Harmonic Currents Represents in % of Fundamental Component by FFT Analysis of Rectifier Input Current

5.3 12-Pulse Converter:

In 12-Pulse converter a three winding transformer is used which is having one primary winding and two secondaries winding. In secondaries one winding is in delta and other is in star so net phase shift between these two is 30^0. A 3-phase bridge rectifier unit is connected to each of the winding. This system generates two DC link which can be connected either in series to increase the voltage level or in parallel to increase current rating. Both type of connection are simulated and harmonic spectrum is calculated by using Power GUI block. Rectifier is loaded with R and R-L load and its input current and input voltage wave forms are recorded by scope, effect of change in load on harmonic spectrum is also studied. Simulation parameter are given in Appendix-A.

5.3.1 12-Pulse Parallel Converter:

Simulated 12-Pulse Series Converter is shown in figure (5.4). Simulation is carried out for R and R-L load and its input voltage and current wave form is shown in figure (5.5 a& b).

An interphase reactor is required for paralleling of two DC bus bar. This configuration is used to increase the current rating at same DC voltage. The important thing for this converter is 5^{th} and 7^{th} harmonic are absent. Simulation parameter are given in Appendix-A.

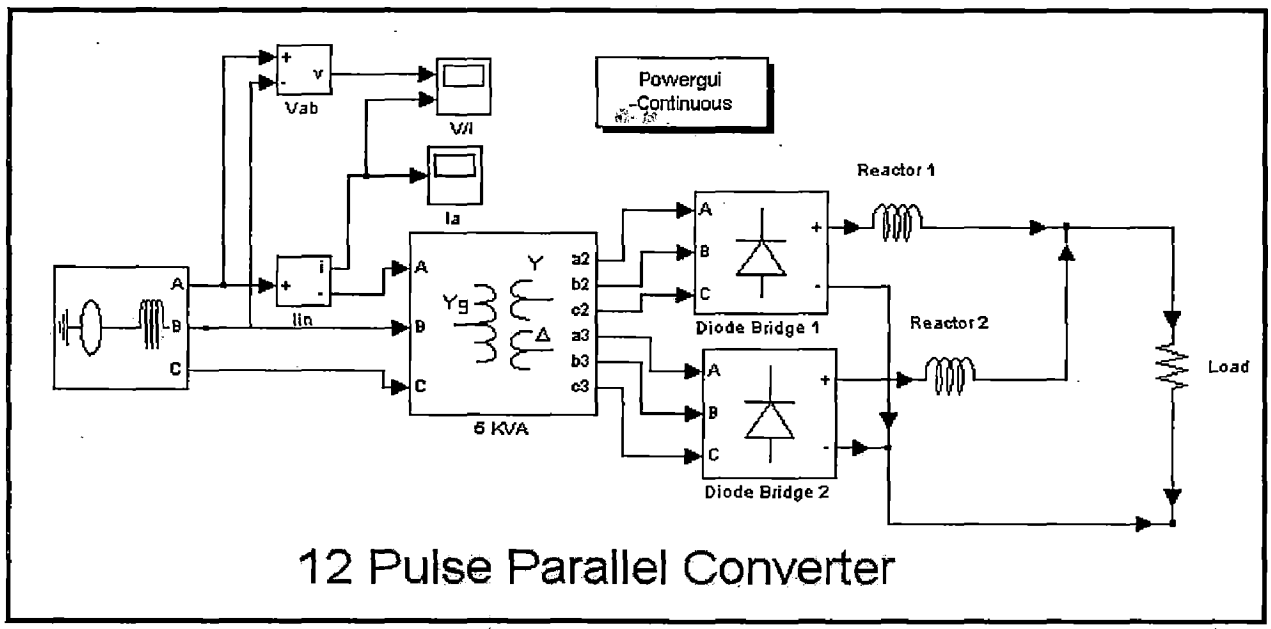

fig. (5.4) Simulated 12-Pulse Parallel Converter

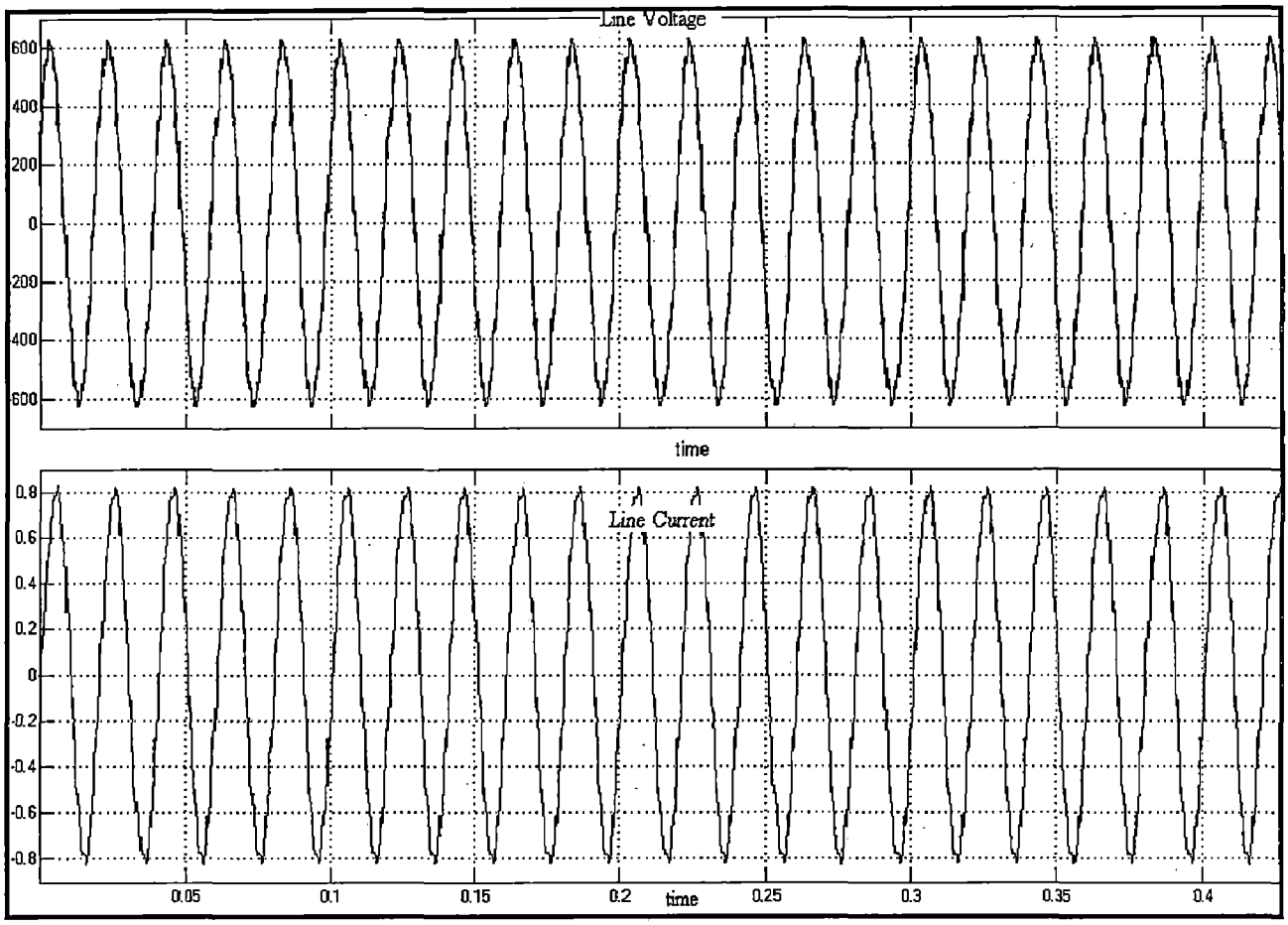

fig. (5.5 a) Input Line Voltage and Current Waveform for Resistive Load

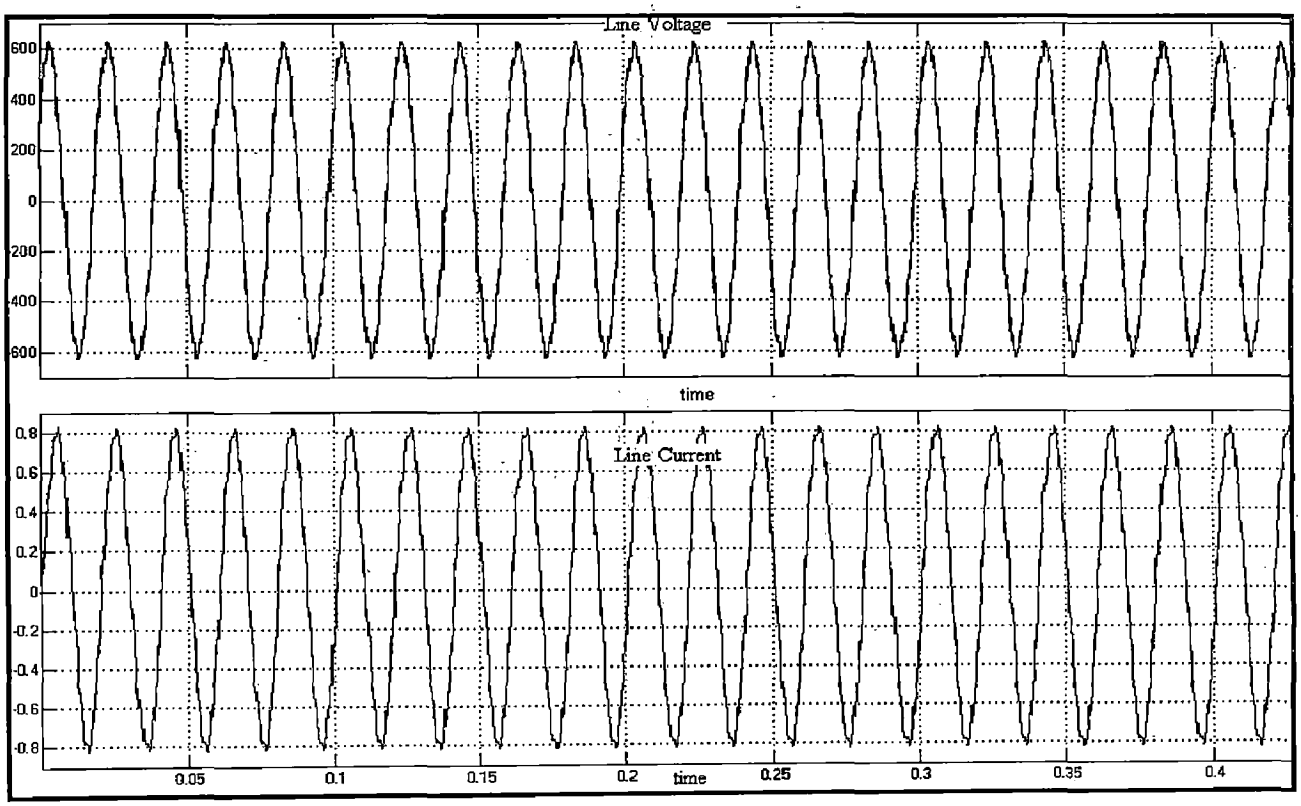

fig. (5.5 b) Input Line Voltage and Current Waveform for R-L Load

Harmonic analysis is carried out by using FFT of Power GUI block. FFT spectrum is shown in figure (5.6 a&b) for R and R-L load respectively. THD of input line current is 6.07 % and 6.00 % in case of R and R-L load respectively. Percentage contribution in THD of various order current harmonic is tabulated in Table-(5.2), it can be noted from table that most troublesome harmonics 3^{rd}, 5^{th} and 7^{th} are absent, dominant harmonics are 11^{th} and 13^{th} which are having 5.03 % and 2.11 % in case of resistive load and in case of R-L load it is 4.88 % and 2.21 % of fundamental.

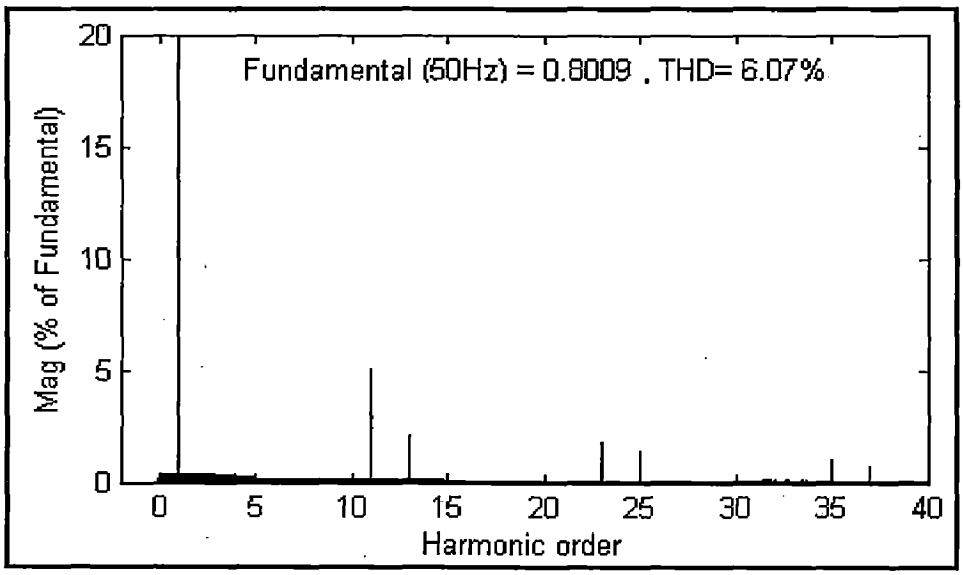

fig .(5.6 a) FFT Analysis of Input Current (Resistive Load)

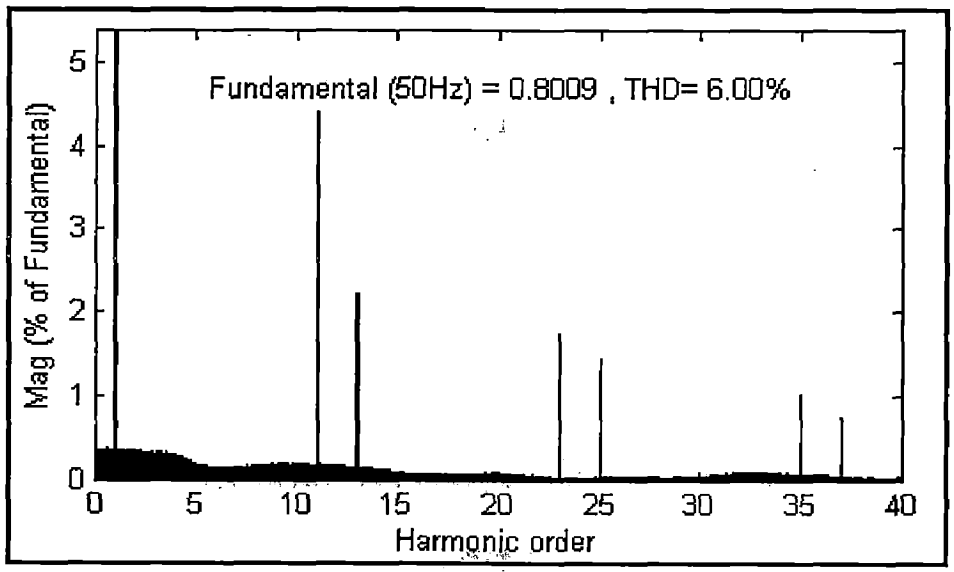

fig .(5.6 b) FFT Analysis of Input Current (R-L Load)

Table (5.2)

% of Fundamental Current		
Harmonic Order	Resistive Load	R-L Load
3	0.33	0.31
5	0.2	0.19
7	0.14	0.14
9	0.18	0.18
11	5.03	4.88
13	2.11	2.21
15	0.09	0.09
17	0.07	0.07
19	0.07	0.07

Table (5.2) Harmonic Currents Represents in % of Fundamental Component by FFT Analysis of 12-Pulse Rectifier Input Current

5.3.2 12-Pulse Series Converter :

To increase the voltage rating two DC link are connected in series as shown in figure (5.7).The converter input voltage and current wave form is studied for R-L load and variation in THD with changing in load is studied. An important point is to be noted that for the same load as applied for parallel converter input current THD is come out to be 50 % of the previous case. Simulation parameter are given in Appendix-A.

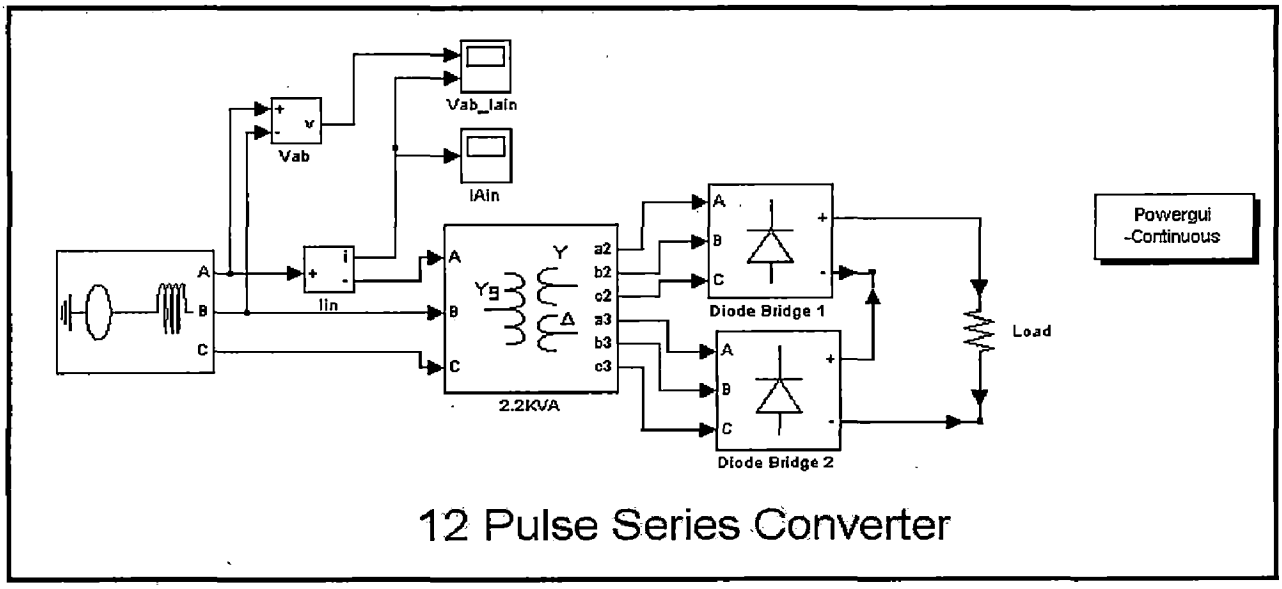

fig. (5.7) Simulated 12-Pulse Series Converter

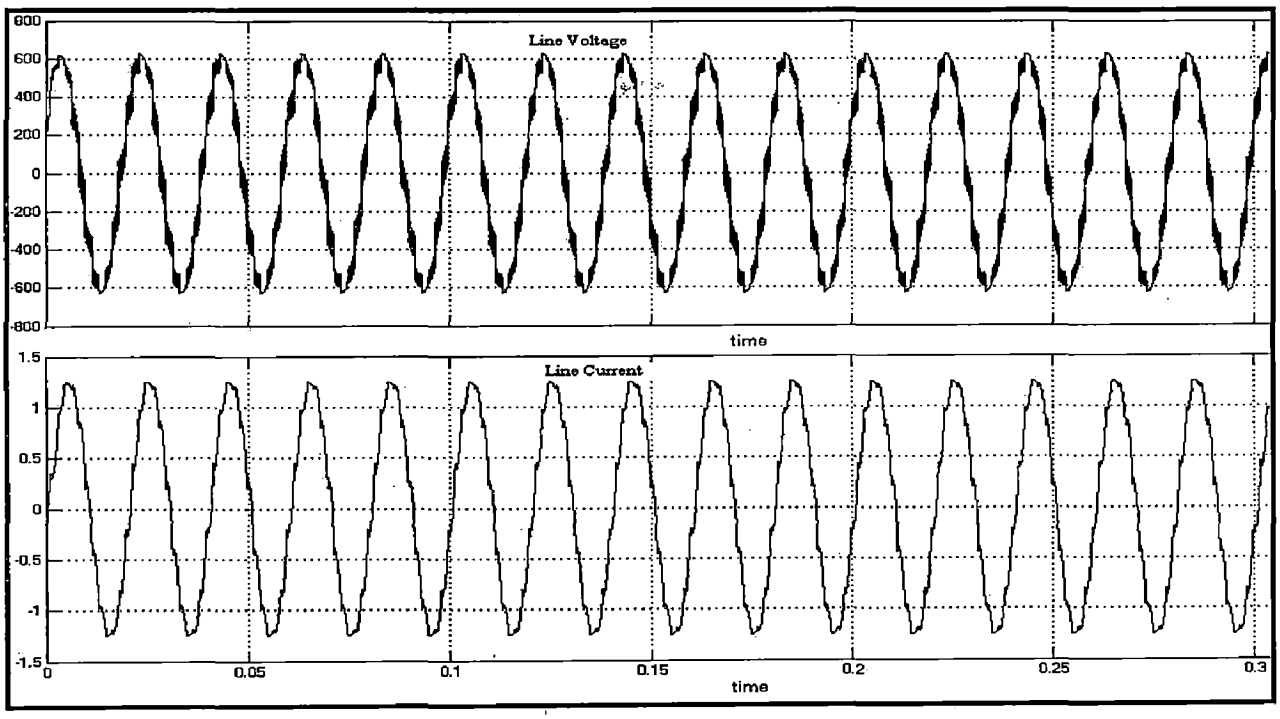

fig. (5.8) Input Line Voltage and Current Waveform for R-L Load

Harmonic analysis is carried out by using FFT of Power GUI block. FFT spectrum is shown in figure (5.9 a&b) for R-L load . THD of input line current is 5.91 % when R =250 ohms L = 4mH and when resistance become half i.e. R = 125 ohms L = 4mH then THD gets reduce and become 3.19 % . Percentage contribution in THD of various order current harmonic is tabulated in Table-(5.3), it can be noted from table that most troublesome harmonics 3^{rd} , 5^{th} and 7^{th} are absent, dominant harmonics are 11^{th} and 13^{th} which are having 4.86 % and 2.86 % in first case and it is 2.58 % and 1.46 % of fundamental in second case. An another point to be notice that higher order such as 23^{rd} is increased and it is 1.20 % in first case and 0.67 % in second case.

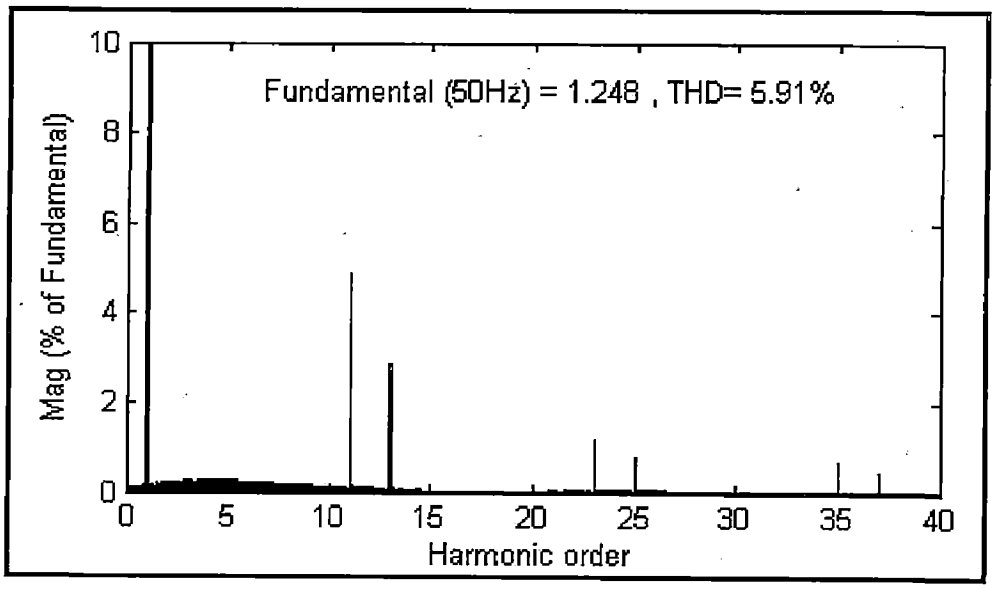

fig .(5.9 a) FFT Analysis of Input Current (R-L Load)

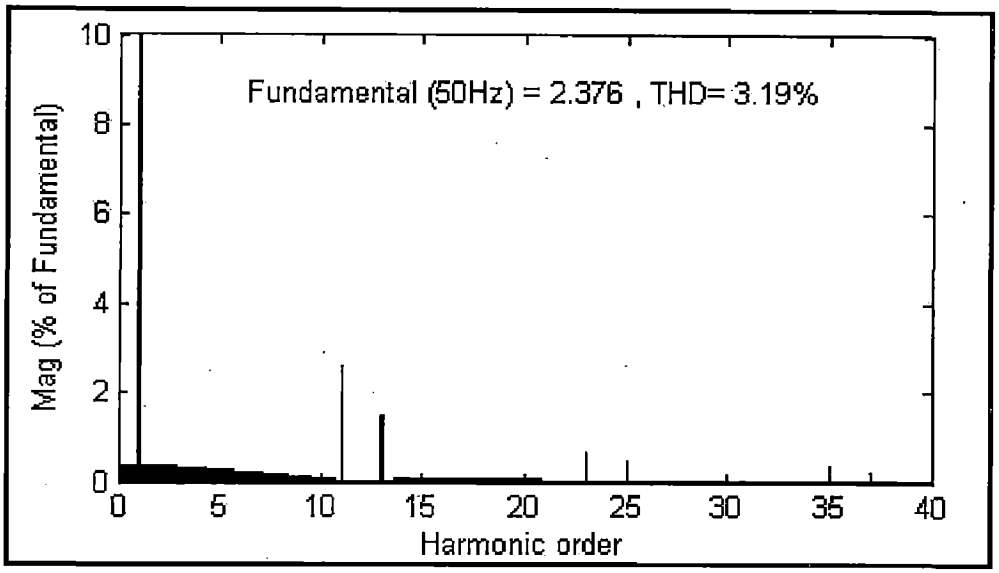

fig .(5.9 b) FFT Analysis of Input Current (50% of previous R-L Load)

Table (5.3)

% of Fundamental Current		
Harmonic Order	R-L Load	50 % of Previous Load
3	0.25	0.34
5	0.26	0.26
7	0.21	0.20
9	0.15	0.12
11	4.86	2.58
13	2.86	1.46
15	0.04	0.06
17	0.02	0.07
19	0.04	0.07
23	1.20	*0.67*

Table (5.3) Harmonic Currents Represents in % of Fundamental Component by FFT Analysis of 12-Pulse Series Connected Rectifier Input Current

5.4 24-Pulses Converter:

For getting four phase shifted secondaries a 24- pulse transformer is simulated as discussed section (4.2) and phase shifted wave forms are recorded by scope as shown in figure (5.10). From figure it can be noted that there is phase shift of 15° between same phases of any two consecutive secondaries.

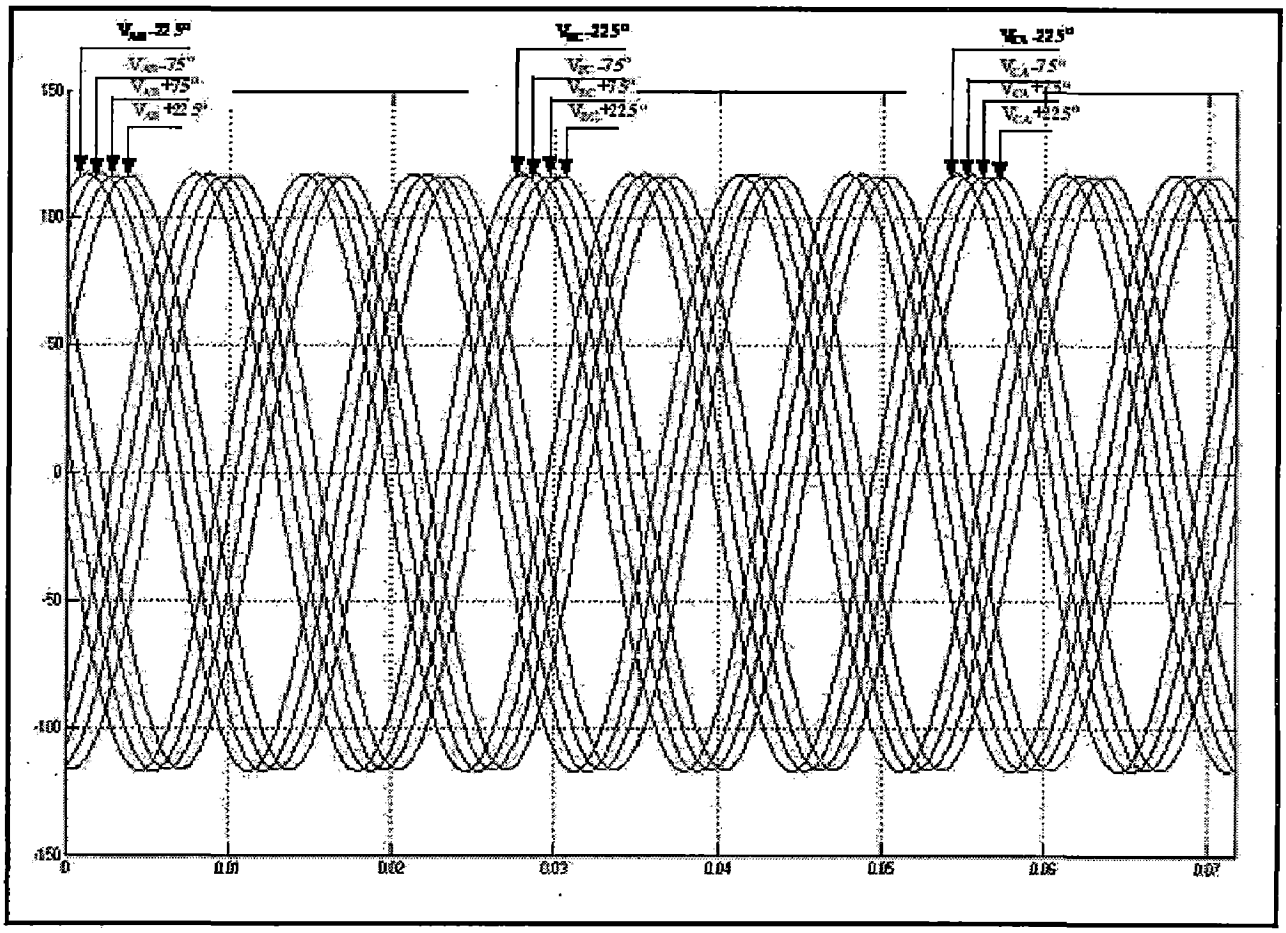

fig. (5.10) Phase Shifted Line to Line voltages of all Secondaries

5.4.1 Simulation Results of Buck-Boost Chopper:

A Buck-Boost chopper is simulated as discussed section (4.4). Simulated system is tested at 200V and 400V AC which is the minimum and maximum range of operating voltage. THD of input line current is also measured by using FFT analyzer. Simulation parameters are given in Appendix-A.

5.4.1.1 Chopper Operating in Boost Mode:

When input supply of converter is 200V AC then DC output of chopper goes below the normalized voltage which is 100V DC in this case chopper operates in Boost mode. Waveforms of DC input and output of all the four choppers are recorded and shown in figure (5.11).

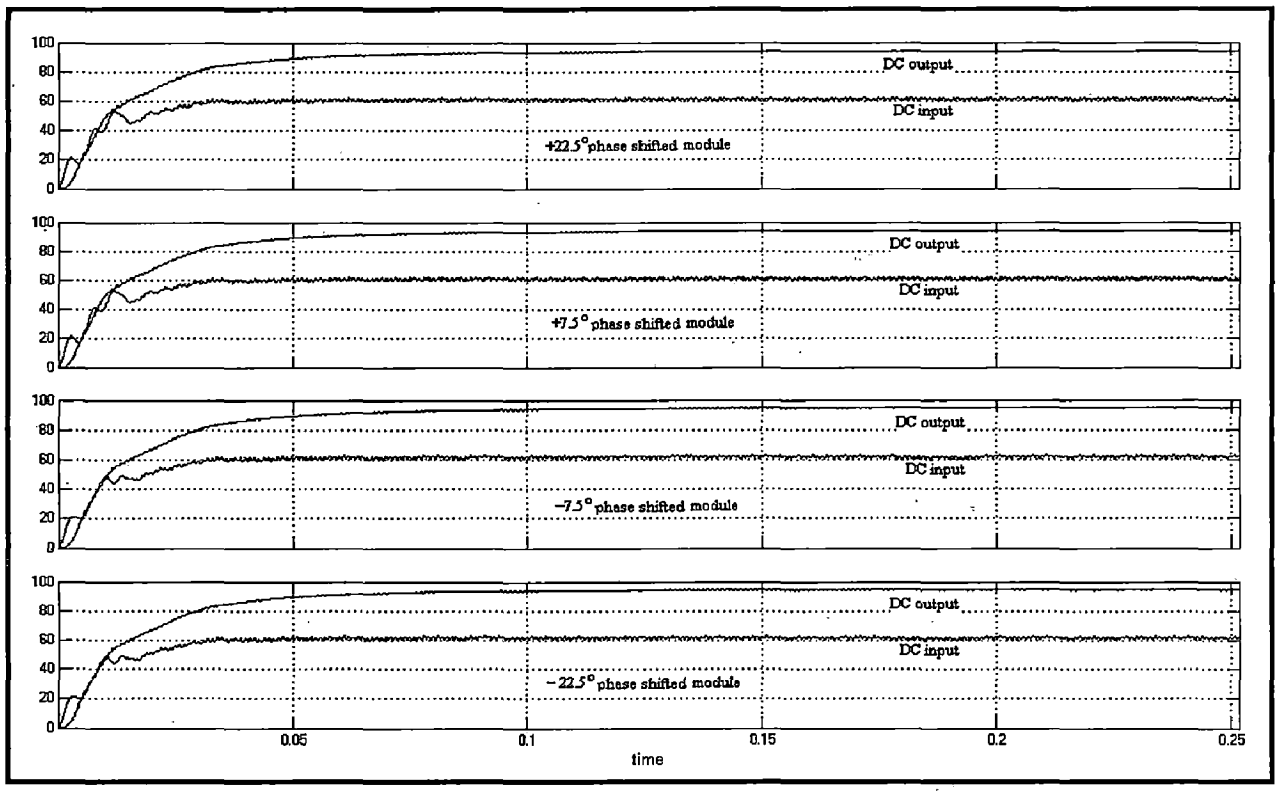

fig. (5.11) Waveforms of DC input and output of all the four choppers

From the above figure following observation has been made:

$$\% \text{ Average Boost} = \frac{96-60}{60} * 100 = 60 \text{ at } 200\text{V AC}$$

Input current waveform when converter is operating in boost mode is recorded, and it is shown in figure (5.12).

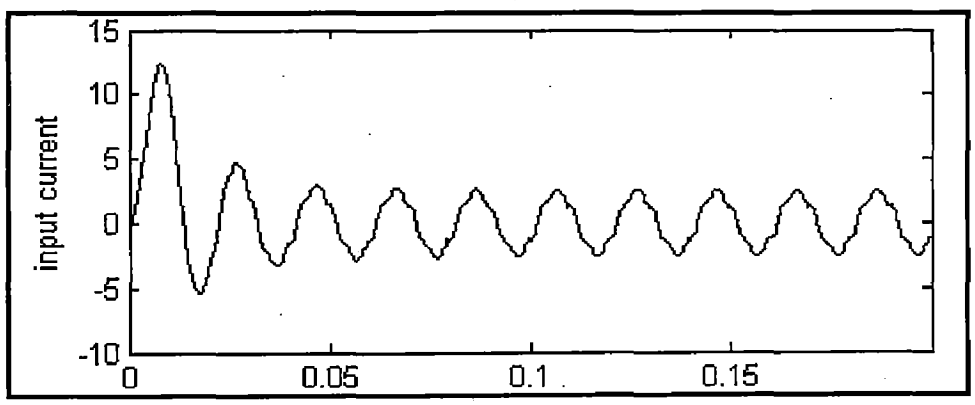

fig. (5.12) Input Current Waveform in Boost Mode

5.4.1.2 THD of Input Line Current:

When converter is operated in Boost mode harmonic spectrum is recorded as shown in figure (5.13). Various harmonics component are tabulated in table-(5.4). THD is come out 5.04% and it can be also noted that reduction in fifth and seventh harmonic as compare to 6-pulse converter where these harmonic were in the ranges of 22% and 10% respectively.

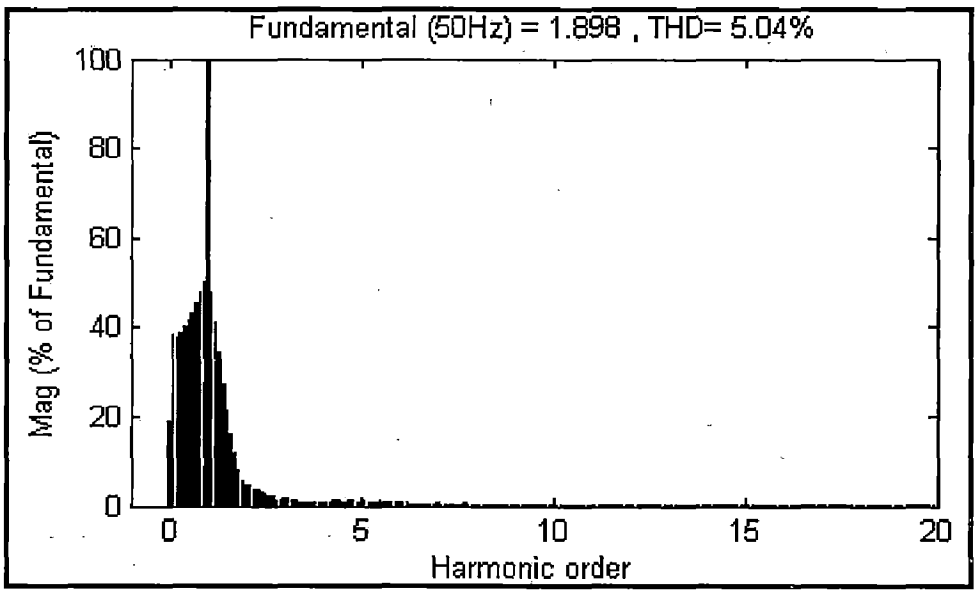

fig .(5.13) FFT Analysis of Input Current

Table (5.4)

Harmonic Order	% of Fundamental Current
3	1.56
5	0.73
7	0.63
9	0.29
11	0.22
13	0.07
15	0.06
17	0.16
19	0.16

Table (5.4) Harmonic Currents Represents in % of Fundamental Component

5.4.1.3 Chopper Operating in Buck Mode:

When input supply of converter is 400V AC then DC output of chopper goes high from the normalized voltage which is 100V DC in this case chopper operates in Buck mode. Waveforms of DC input and output of all the four choppers are recorded and shown in figure (5.14).

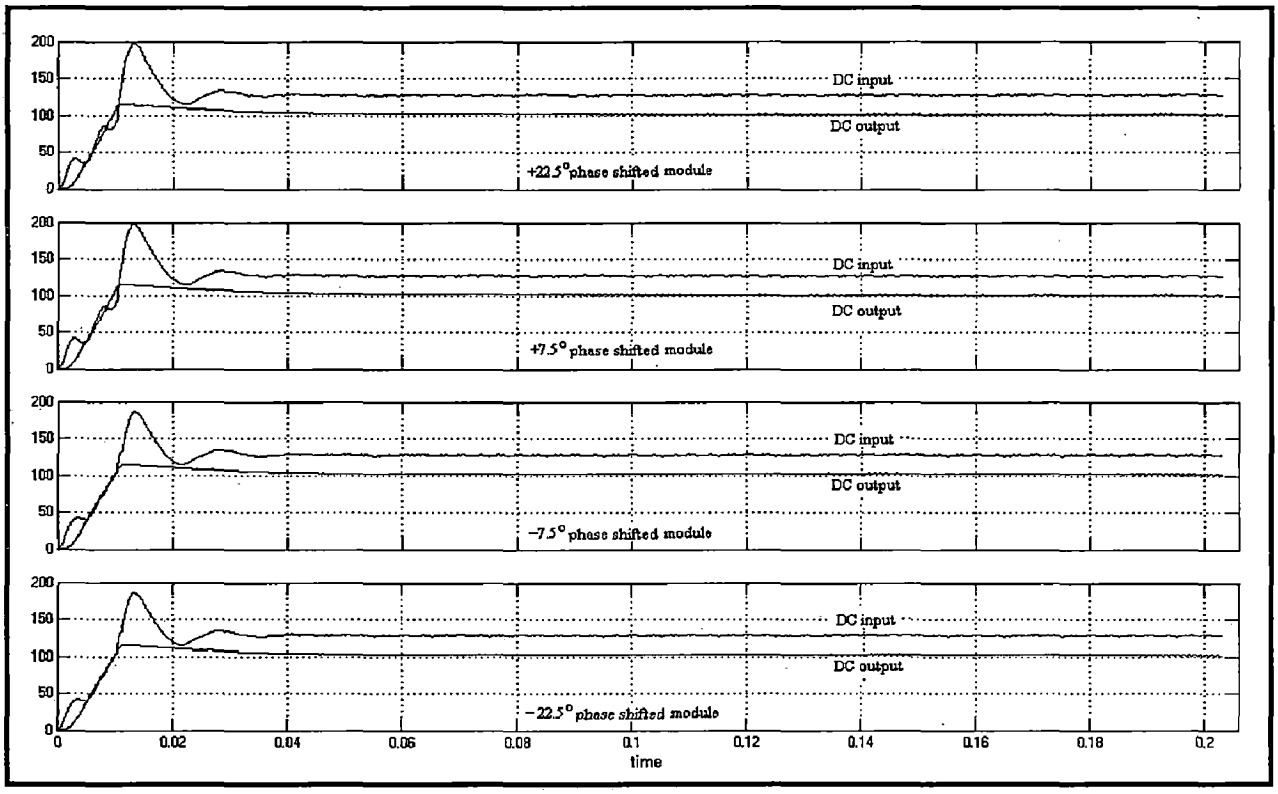

fig. (5.14) Waveforms of DC input and output of all the four choppers

From the above figure following observation has been made:

$$\% \text{ Average Buck} = \frac{130-100}{130} * 100 = 23 \text{ at } 400\text{V AC}$$

Input current waveform when converter is operating in buck mode is recorded, and it is shown in (5.15).

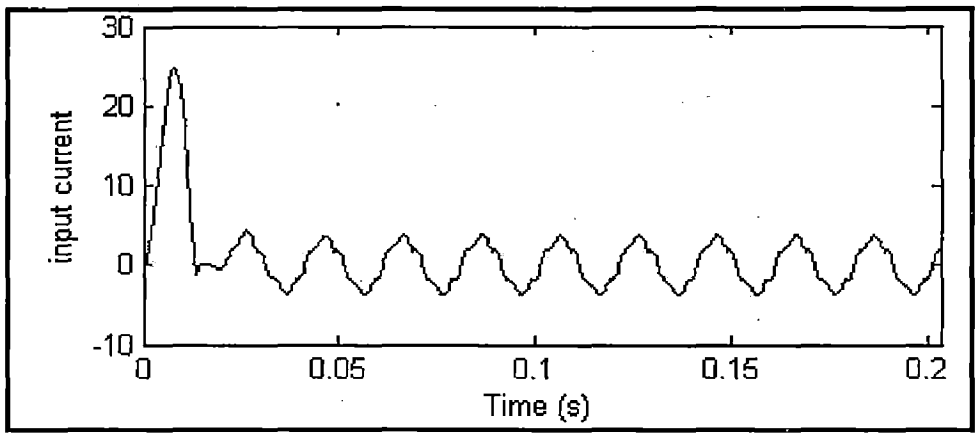

fig. (5.15) Input Current Waveform in Buck Mode

5.4.1.4 THD of Input Line Current:

When converter is operated in Buck mode harmonic spectrum is recorded as shown in figure (5.16). Various harmonics component are tabulated in table-(5.5). THD is come out 12.05% and it can be also noted that reduction in fifth and seventh harmonic as compare to 6-pulse converter where these harmonic were in the ranges of 22% and 10% respectively.

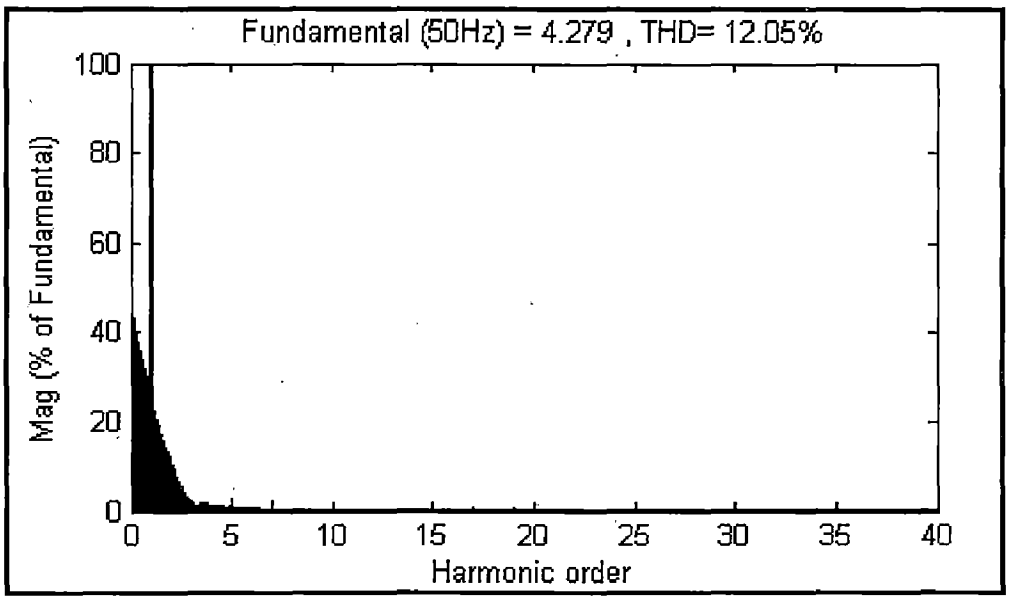

fig .(5.16) FFT Analysis of Input Current

Table (5.5)

Harmonic Order	% of Fundamental Current
3	2.27
5	2.87
7	2.20
9	0.11
11	0.12
13	0.19
15	0.18
17	0.57
19	0.58

Table (5.5) Harmonic Currents Represents in % of Fundamental Component

5.5 24-Pulses Unbalance Converter:

Transformer which is used to developed hardware prototype model is having heavy unbalancing in its secondaries to analyse the effect of this unbalancing, a 24-pulse unbalance transformer is also simulated. Phase shifted wave forms are recorded by scope and shown in figure (5.17). From figure it can be noted that there is unbalanced in transformer secondaries.

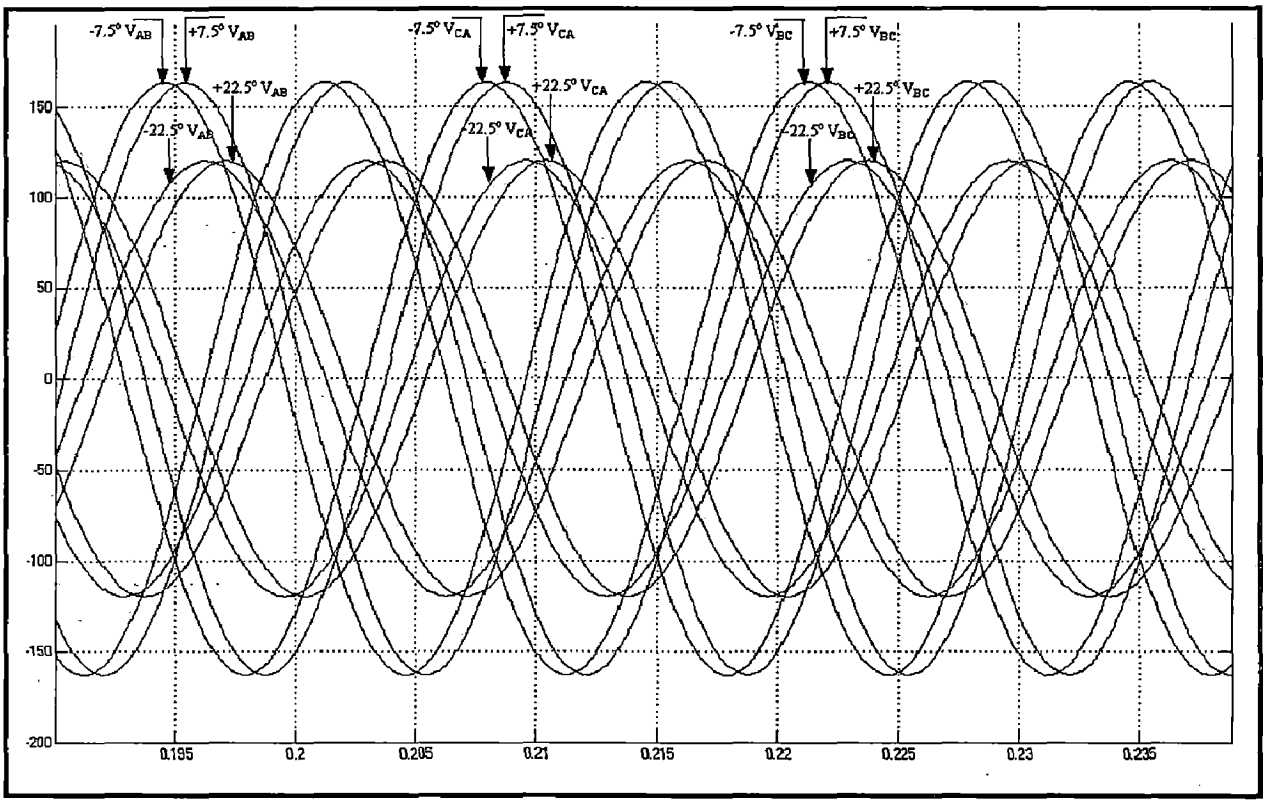

fig. (5.17) Phase Shifted Line to Line voltages of all Secondaries

5.5.1 Unbalance Buck-Boost Chopper:

A Buck-Boost chopper by using unbalanced transformer is simulated. Simulation is done at two frequency first is at 1 kHz and second is at 10 kHz, to check the power quality performance of converter. Simulated system is tested at 200V and 400V AC which is the minimum and maximum range of operating voltage. THD of input line current is also measured by using FFT analyzer. Simulation parameters are given in Appendix-A.

5.5.1.1 Chopper Operating in Boost Mode:

When input supply of converter is 200V AC then DC output of chopper goes below the normalized voltage which is 100V DC in this case chopper operates in Boost mode. Waveforms of DC input and output of all the four choppers are recorded and shown in figure (5.18). It can be noted that even DC input of +22.5° and -22.5° modules are low as compare to +7.5° and -7.5° modules but output voltage is same.

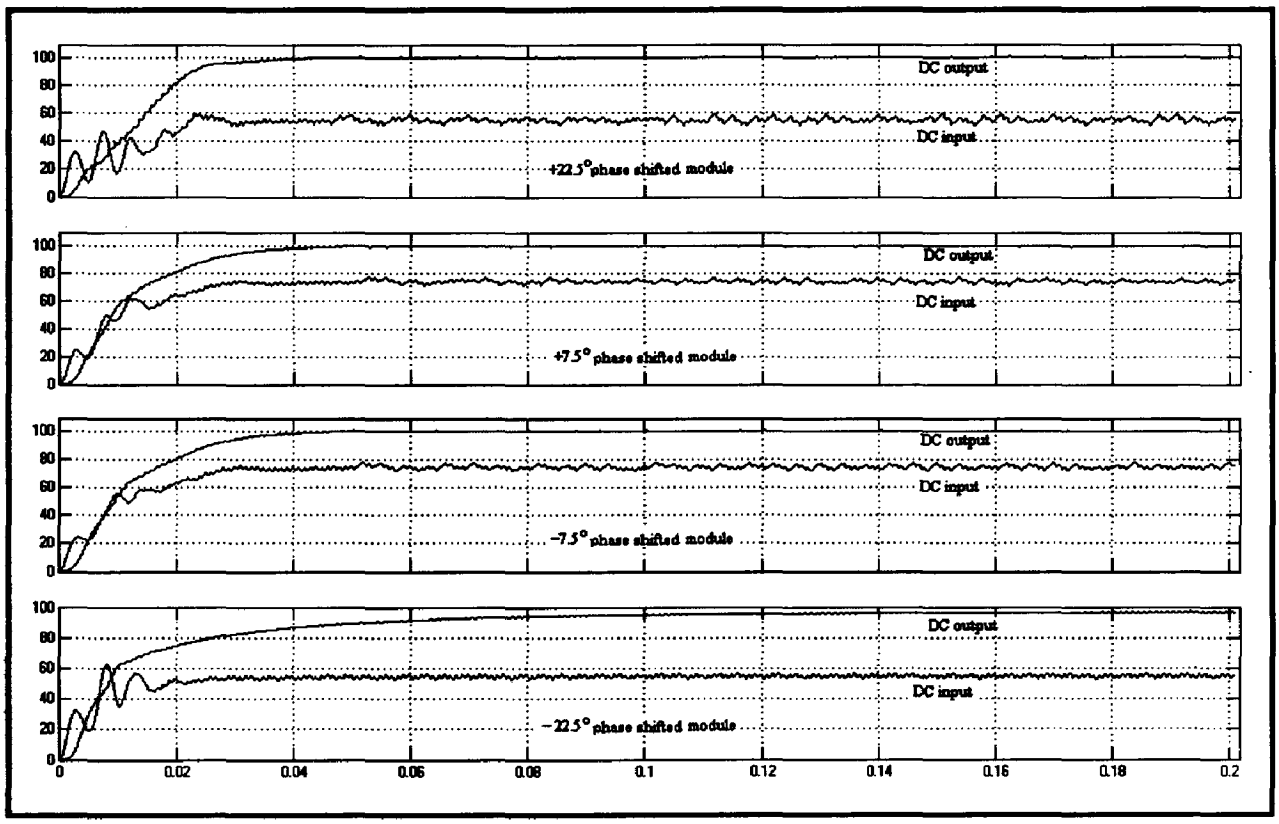

fig. (5.18) Waveforms of DC input and output of all the four choppers

From the above figure following observation has been made:

$$\% \text{ Boost in } +22.5°/-22.5° = \frac{100-57}{57} * 100 = 75 \text{ at } 200\text{V AC}$$

$$\% \text{ Boost in } +7.5°/-7.5° = \frac{100-78}{78} * 100 = 28 \text{ at } 200\text{V AC}$$

Input current waveform when converter is operating in boost mode at 1 kHz and at 10 kHz is recorded and it is shown in figure (5.19 a&b). For 10 kHz measurement current multiplication factor is taken as 100, just to make input voltage and current scale same and input voltage and current is shown in figure (5.19 b) and power factor is calculated.

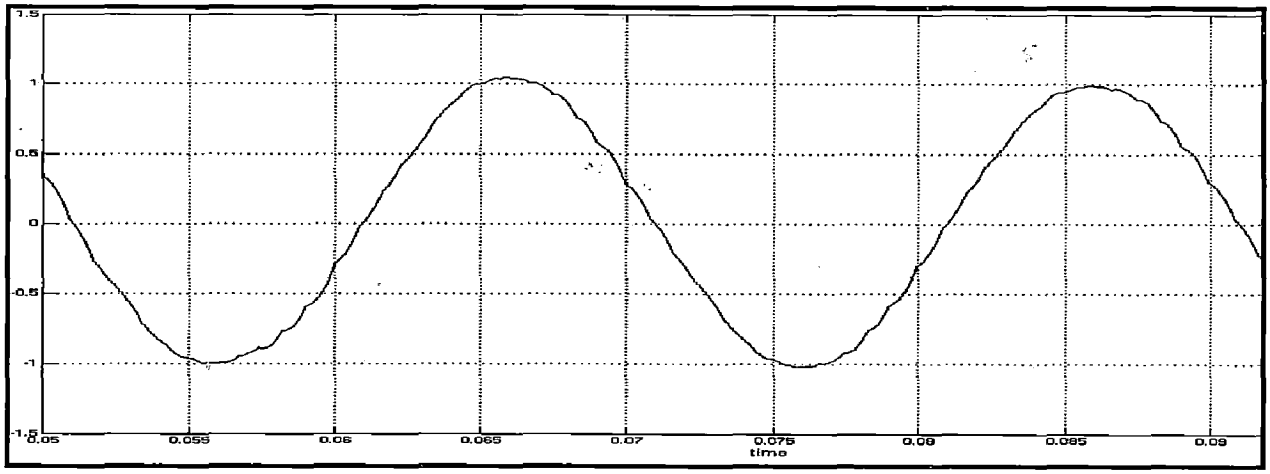

fig. (5.19a) Input Current Waveform in Boost Mode at 1 kHz

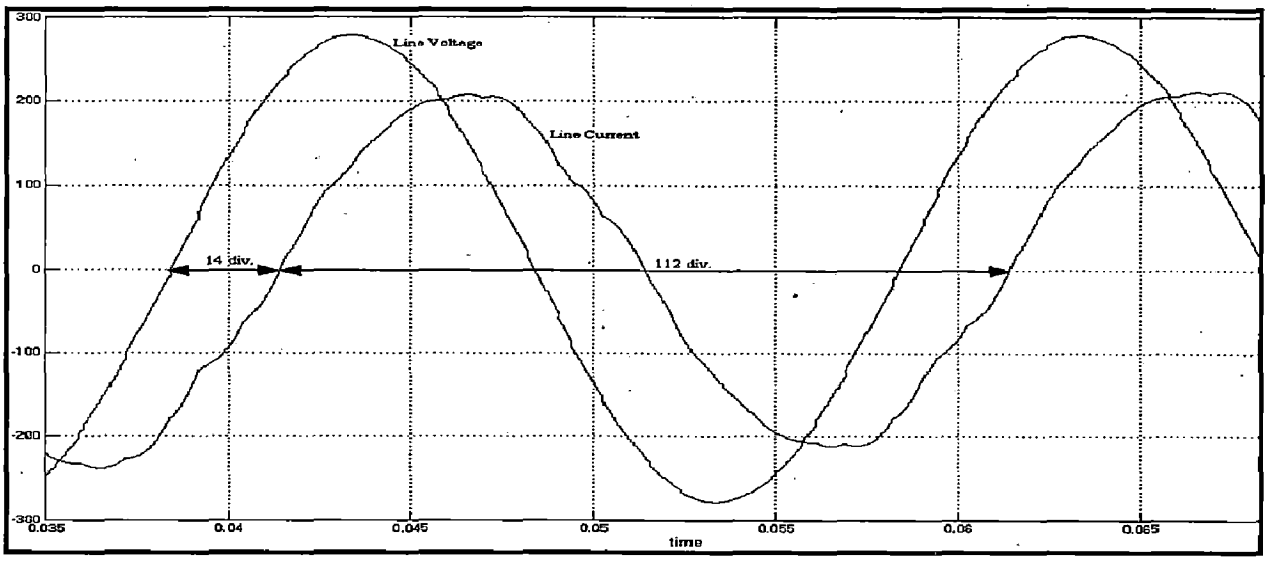

fig. (5.19b) Input Voltage and Current Waveform in Boost Mode at 10 kHz

From figure (5.19b) we can calculate the power factor as follows:

One cycle is in 112 division = 360°

Voltage and Current waveforms are displaced by 14 divisions

14 division = 45°

Hence power factor = (cos 45°) = 0.70

5.5.1.2 THD of Input Line Current:

When converter is operated in Boost mode harmonic spectrum is recorded as shown in figure (5.20a) and (5.20b) for 1 kHz and 10 KHz respectively. For 10 kHz current multiplication factor is taken as 100. Various harmonics component are tabulated in table-(5.6). THD is come out 7.57% for 1 kHz and 5.39% for 10 kHz. It can be also noted that reduction in fifth and seventh harmonic as compare to 6-pulse converter where these harmonic are in the ranges of 22% and 10% respectively and all the lower order harmonics are absent.

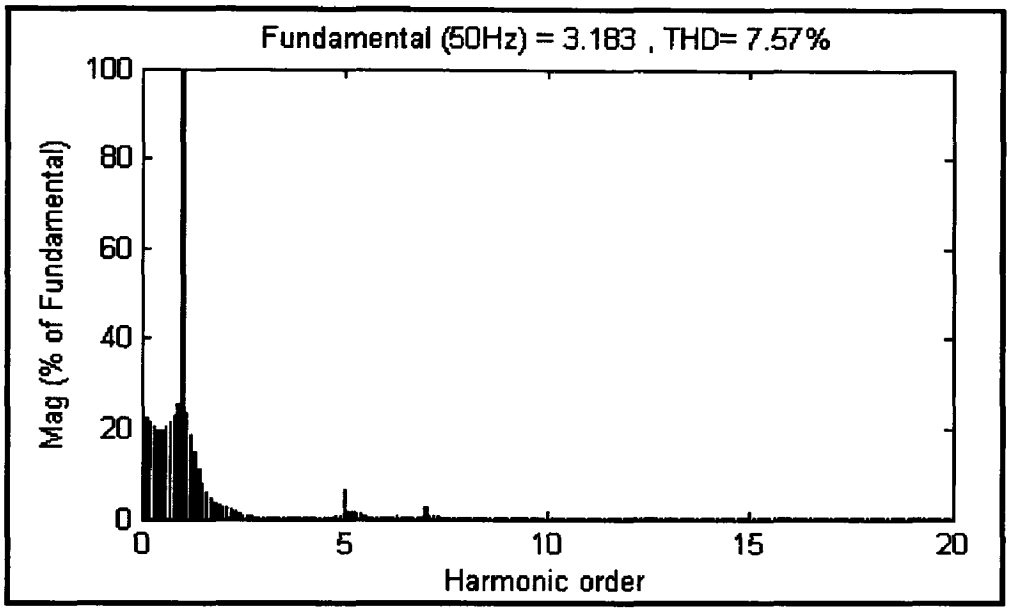

fig .(5.20a) FFT Analysis of Input Current (1 kHz)

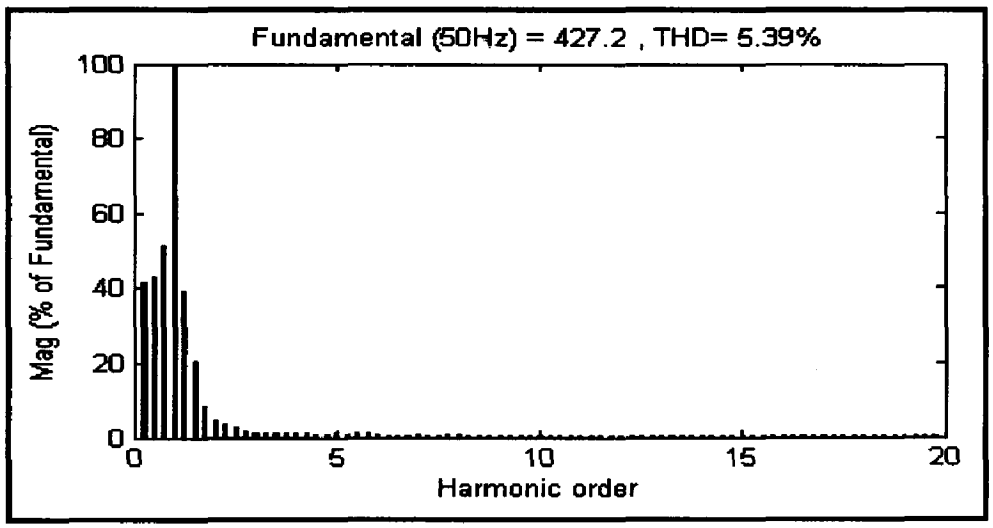

fig .(5.20b) FFT Analysis of Input Current (10 kHz)

Input current waveform when converter is operating in buck mode at 1 kHz and at 10 kHz is recorded and it is shown in figure (5.22 a&b). For 10 kHz measurement current multiplication factor is taken as 100, just to make input voltage and current scale same and input voltage and current is shown in figure (5.22 b) and power factor is calculated.

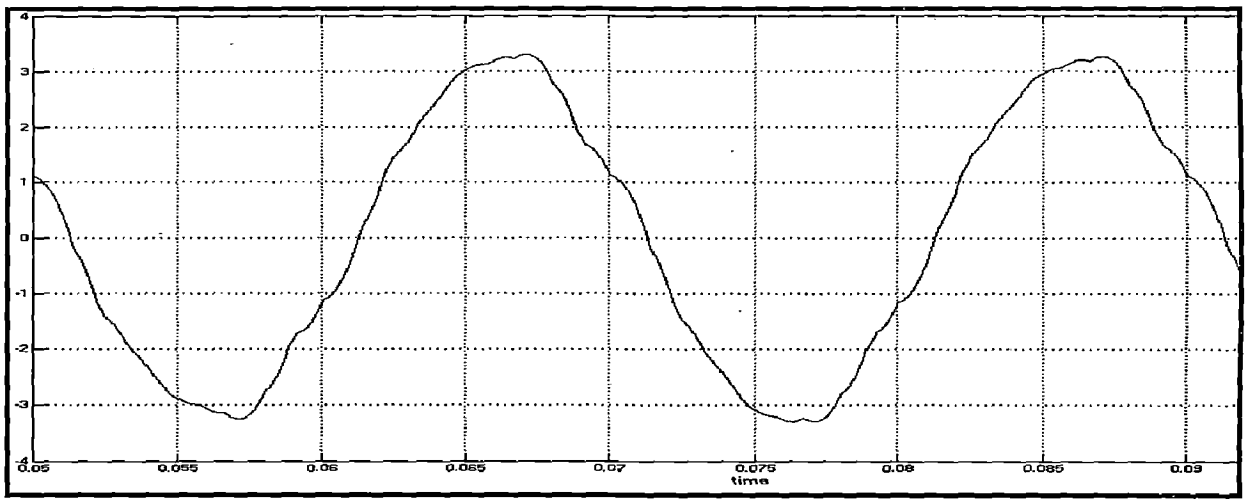

fig. (5.22a) Input Current Waveform in Buck Mode at 1 kHz

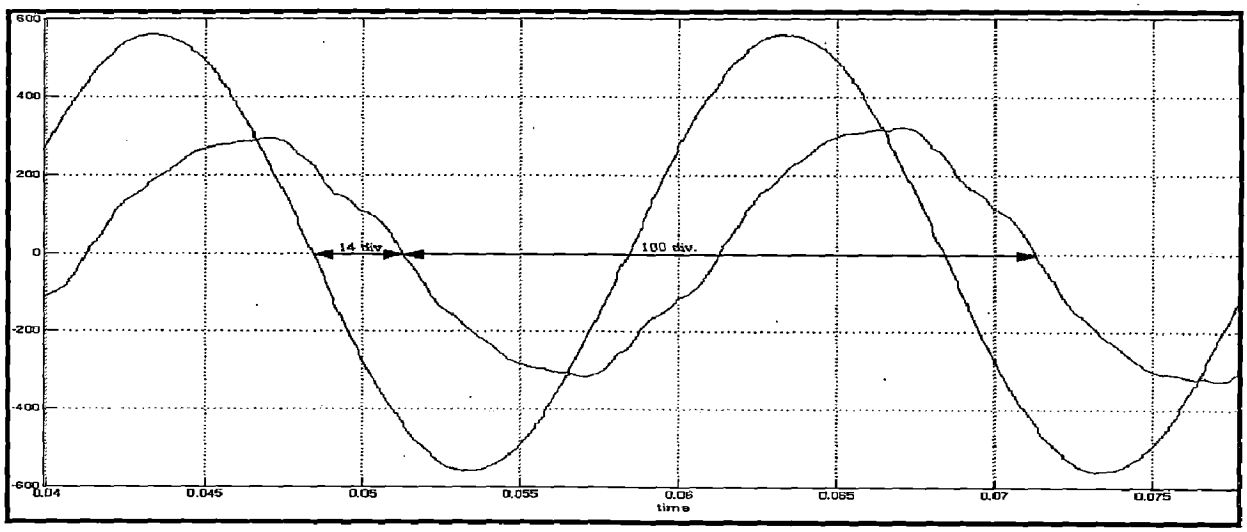

fig. (5.22b) Input Voltage and Current Waveform in Buck Mode at 10 kHz

From figure (5.19b) we can calculate the power factor as follows:

One cycle is in 100 division = 360°

Voltage and Current waveforms are displaced by 14 divisions

14 division = 50.4°

Hence power factor = (cos 50.4°) = 0.63

5.5.1.4 THD of Input Line Current:

When converter is operated in Buck mode harmonic spectrum is recorded as shown in figure (5.23a) and (5.23b) for 1 kHz and 10 KHz respectively. For 10 kHz current multiplication factor is taken as 100. Various harmonics component are tabulated in table-(5.7). THD is come out 13.68% for 1 kHz and 4.72% for 10 kHz. It can be also noted that reduction in fifth and seventh harmonic as compare to 6-pulse converter where these harmonic were in the ranges of 22% and 10% respectively and all the lower order harmonics are absent.

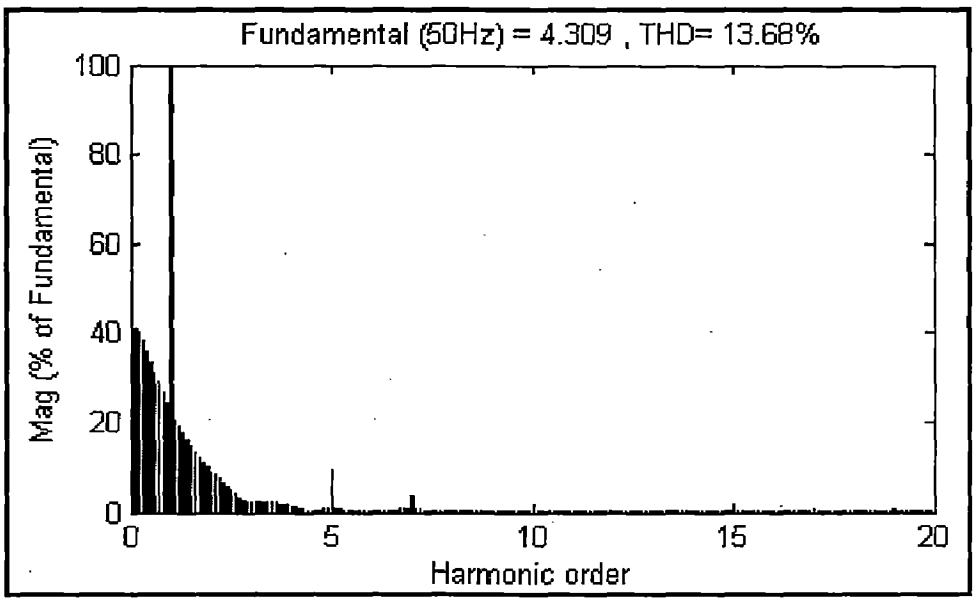

fig .(5.23a) FFT Analysis of Input Current (1 kHz)

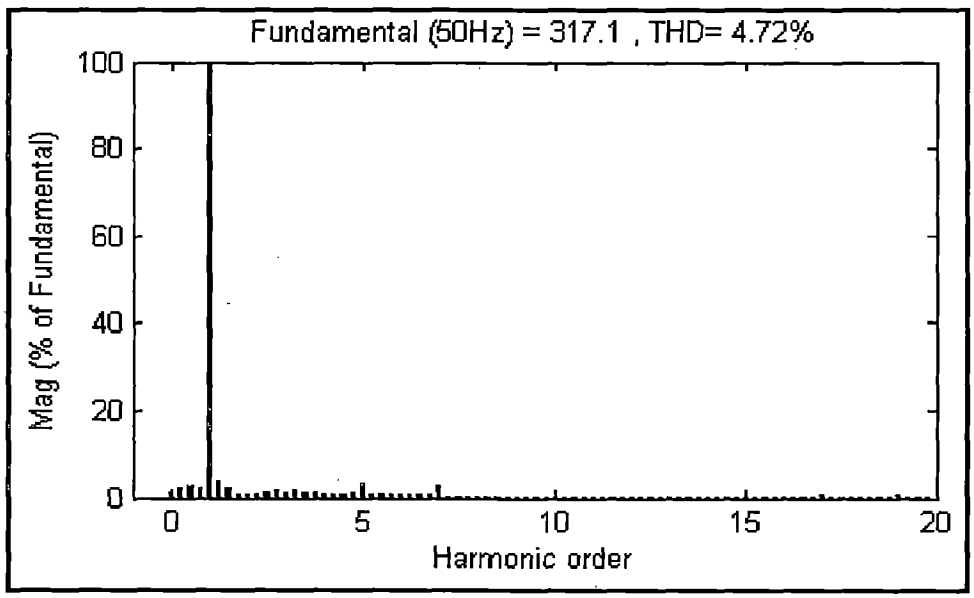

fig .(5.23b) FFT Analysis of Input Current (10 kHz)

Table (5.8)

Harmonic Order	% of Fundamental Current
3	1.80
5	2.16
7	1.35
9	0.13
11	0.13
13	0.05
15	0.03
17	0.31
19	0.24

Table (5.8) Harmonic Currents Represents in % of Fundamental Component

6.1 Introduction:

A prototype model for 24-pulse AC/DC converter as discussed in chapter-3 is developed in the laboratory for experimentation purpose [11, 12]. The developed converter is tested for whole range of supply, assuming variation in AC supply is +/- 25%. The THD and Power factor of developed converter is also checked and recorded using power quality analyzer. The THD is found within IEEE – 519 standards. Complete block diagram of developed 24-pulse converter is shown in figure (6.1).The complete system contain 24-pulse transformer as discussed in chapter-3, is having four phase shifted secondaries each feed the power to buck-boost chopper system.

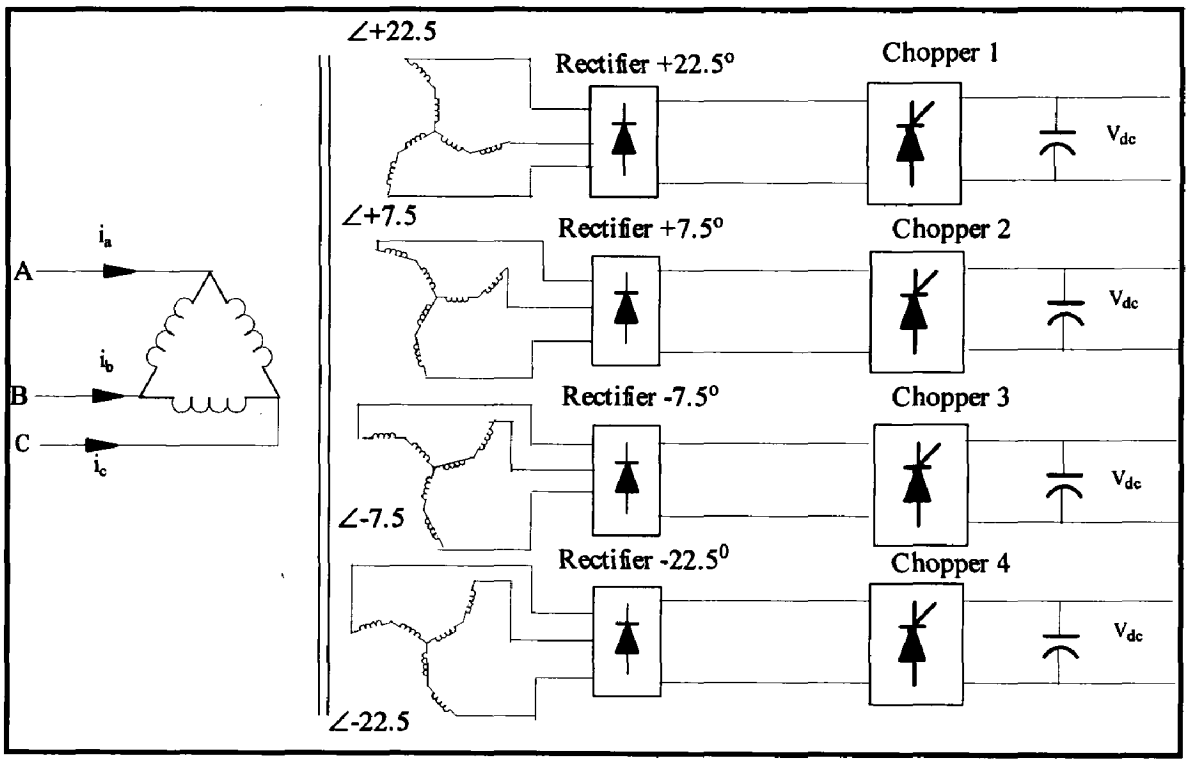

fig. (6.1) Block Diagram of Developed 24-pulse Converter

6.2.1.1 Analysis of Input Line Currents:

The input line currents I_a, I_b and I_c are obtained by summing all currents through windings at same node. All four secondary winding will draw current from primary; since secondaries are phase shifted hence the input line current has to be 24 steps per cycle. Input line current of developed converter is recorded as shown in figure (6.2) and it is found as expected.

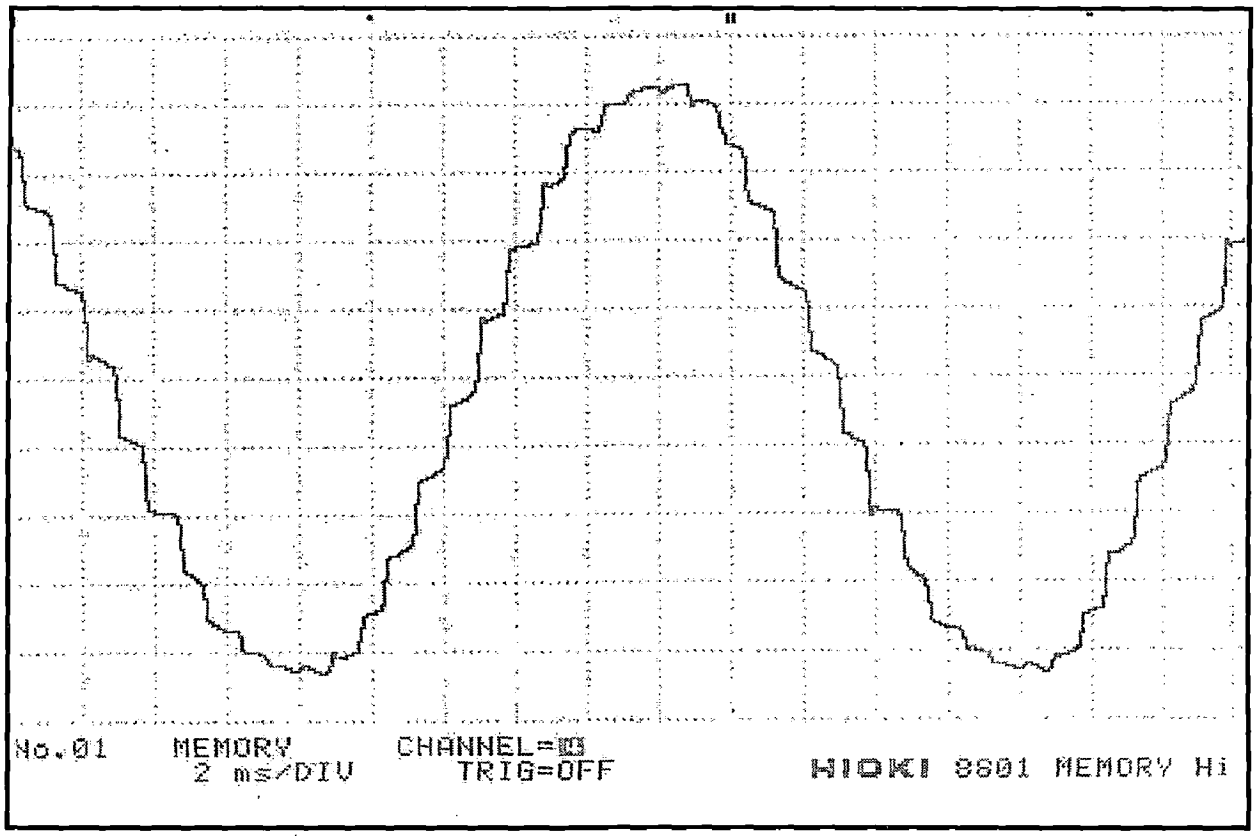

fig (6.2) Recorded Input Line Current Waveform of 24-Pulse Converter

6.2.1.2 Testing of Secondaries Voltages:

The connections for getting phase shift of +22.5°,+7.5°,-7.5° and -22.5° are made as discussed in chapter-3. Individual line to line voltages as well as phase voltages were tested and sample readings are tabulated in table (6.2).

The sample readings on the multiphase secondary side were noted corresponding to various input voltages. All the voltage readings in the secondary sides are taken simultaneously so as to check the balance output voltage.

Table - (6.2)

Sl. No.	V_{in} (V)	+22.5° Phase Shifted Winding Voltage(V)		+7.5° Phase Shifted Winding Voltage(V)		-7.5° Phase Shifted Winding Voltage(V)		-7.5° Phase Shifted Winding Voltage(V)	
		V_{LL}	V_P	V_{LL}	V_P	V_{LL}	V_P	V_{LL}	V_P
1	50	11.11	6.12	14.82	8.54	15.14	8.55	11.21	6.05
2	100	21.43	12.24	29.15	17.21	29.22	16.8	21.78	12.04
3	150	31.70	18.18	43.6	25.58	43.5	24.9	32.2	17.92
4	200	42.6	24.29	58.5	34.27	58.2	33.3	43.4	23.98
5	300	63.3	36.01	87.3	51.5	86.3	50.0	64.7	35.62
6	400	84.7	48.7	116.5	69.3	115.0	67.0	85.7	48.5

Table (6.2) Transformer Primary and Phase Shifted Secondary Winding Voltages

Table – (6.3)

Phase	Primary Voltage(V)	Secondary Voltages(V)							
		+22.5° Phase Shifted Winding Voltage(V)		+7.5° Phase Shifted Winding Voltage(V)		-7.5° Phase Shifted Winding Voltage(V)		-22.5° Phase Shifted Winding Voltage(V)	
		V_{LL}	V_P	V_{LL}	V_P	V_{LL}	V_P	V_{LL}	V_P
AB	200	42.4	24.2	58.3	34.1	57.7	33.07	43.2	23.84
BC	197.3	42.9	24.56	58.4	35.13	58.6	33.43	42.2	23.90
CA	201.0	42.4	24.2	59.9	34.01	58.3	33.56	43.12	24.62

Table (6.3) Transformer Primary and Secondary Winding Voltages for all Phases.

From the table following observation has been made:

$$\%\ \text{Boost} = \frac{97.9 - 53.8}{53.8} * 100 = 81 \text{ at } 200\text{V AC}$$

$$\%\text{Buck} = \frac{116.8 - 102.5}{116.8} * 100 = 12 \text{ at } 400\text{V AC}$$

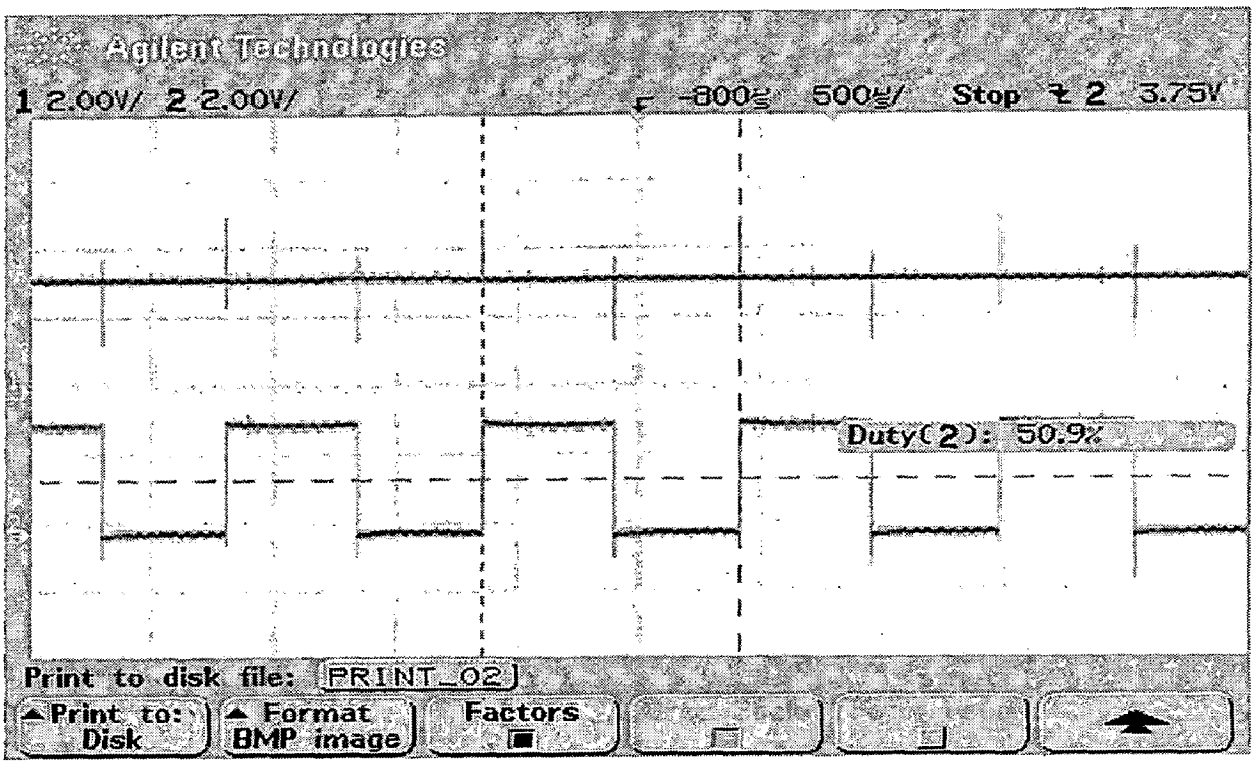

fig (6.6a) Gating Pulses when Converter Operated in Boost Mode

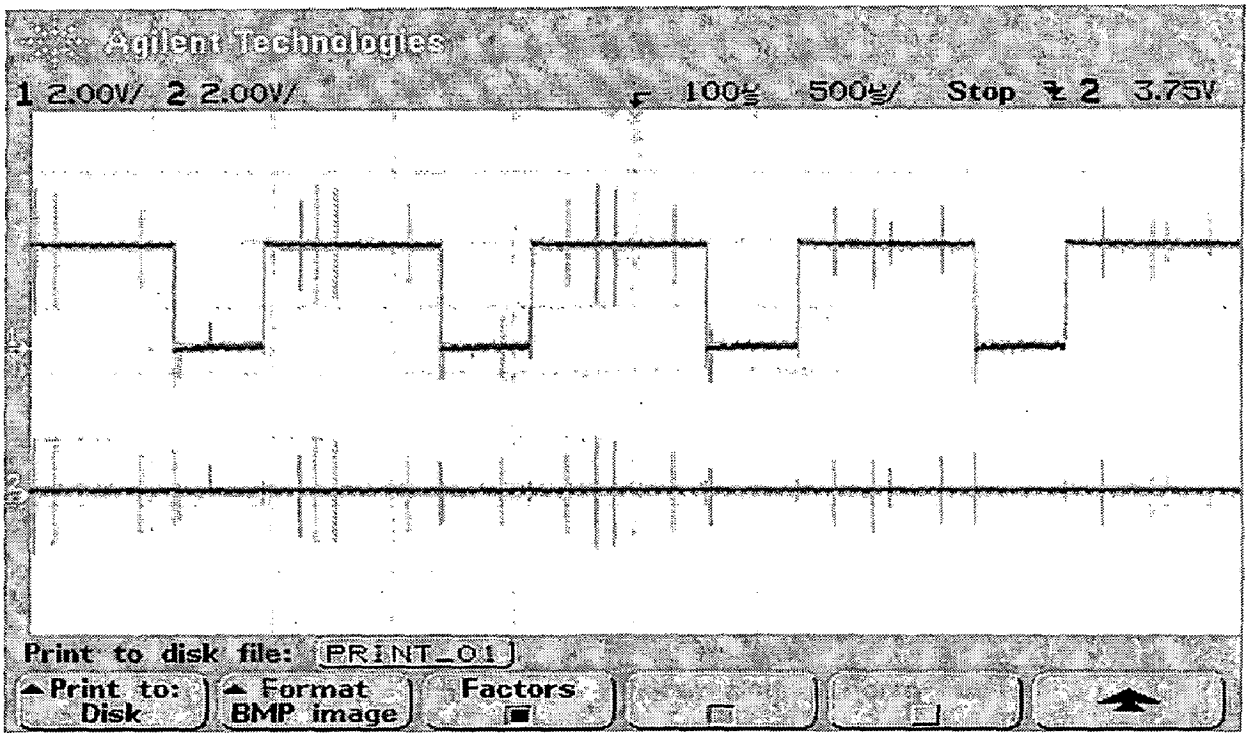

fig (6.6b) Gating Pulses when Converter Operated in Buck Mode

6.2.3.3 Experimental Result of +7.5° Module:

Various readings for this module are tabulated in table-(6.6) and gating signals are recorded when converter is operating in buck mode as well as in boost mode and these signals are shown in figure (6.7).

Table- (6.6)

Sl. No.	Table- (6.5) AC Input Voltage (Volts)	Chopper DC Input Voltage (Volts)	Chopper DC Output Voltage (Volts)	% Duty Cycle	
				SW1	SW2
1	200	78.9	102	100	28.6
2	254	100	100.4	100	0
3	400	168	105	63	0

Table –(6.6) Experimental Reading of +7.5° Module

From the table following observation has been made:

$$\% \text{ Boost} = \frac{102 - 78.9}{78.9} * 100 = 29.27 \text{ at } 200\text{V AC}$$

$$\%\text{Buck} = \frac{168 - 105}{168} * 100 = 37.5 \text{ at } 400\text{V AC}$$

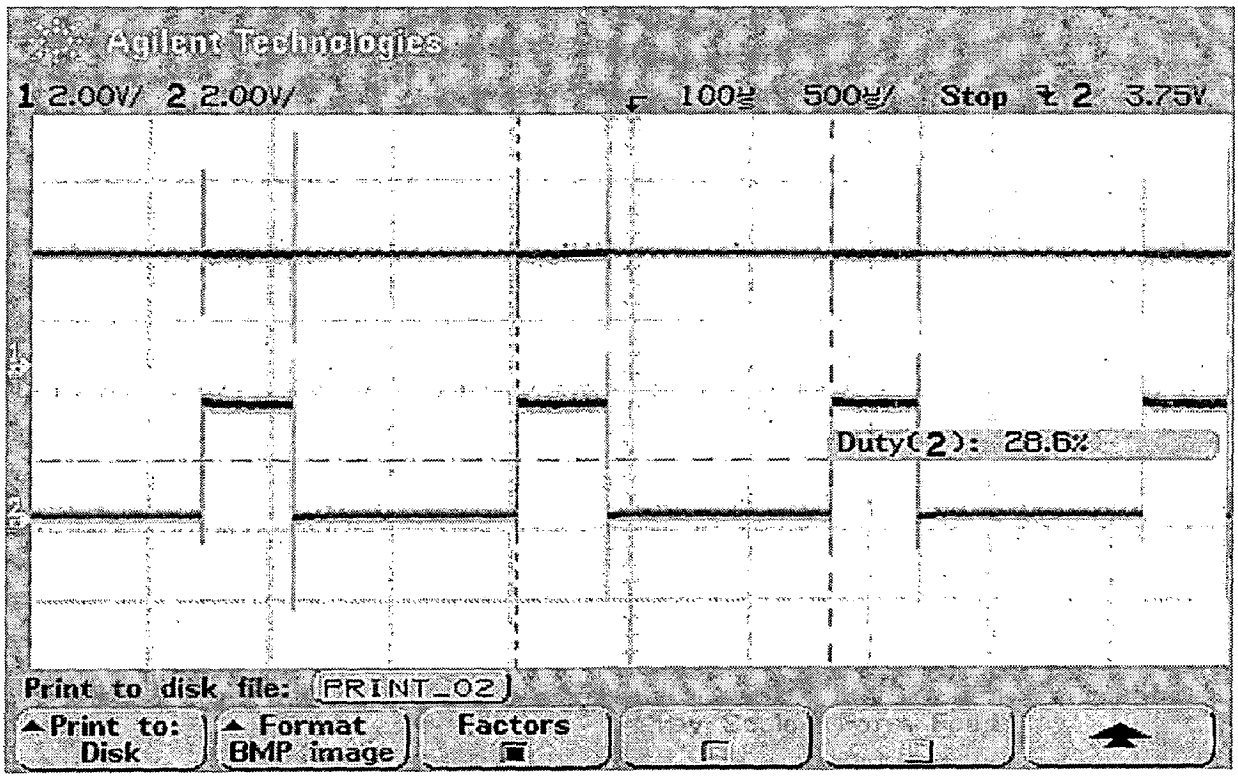

fig (6.7a) Gating Pulses when Converter Operated in Boost Mode

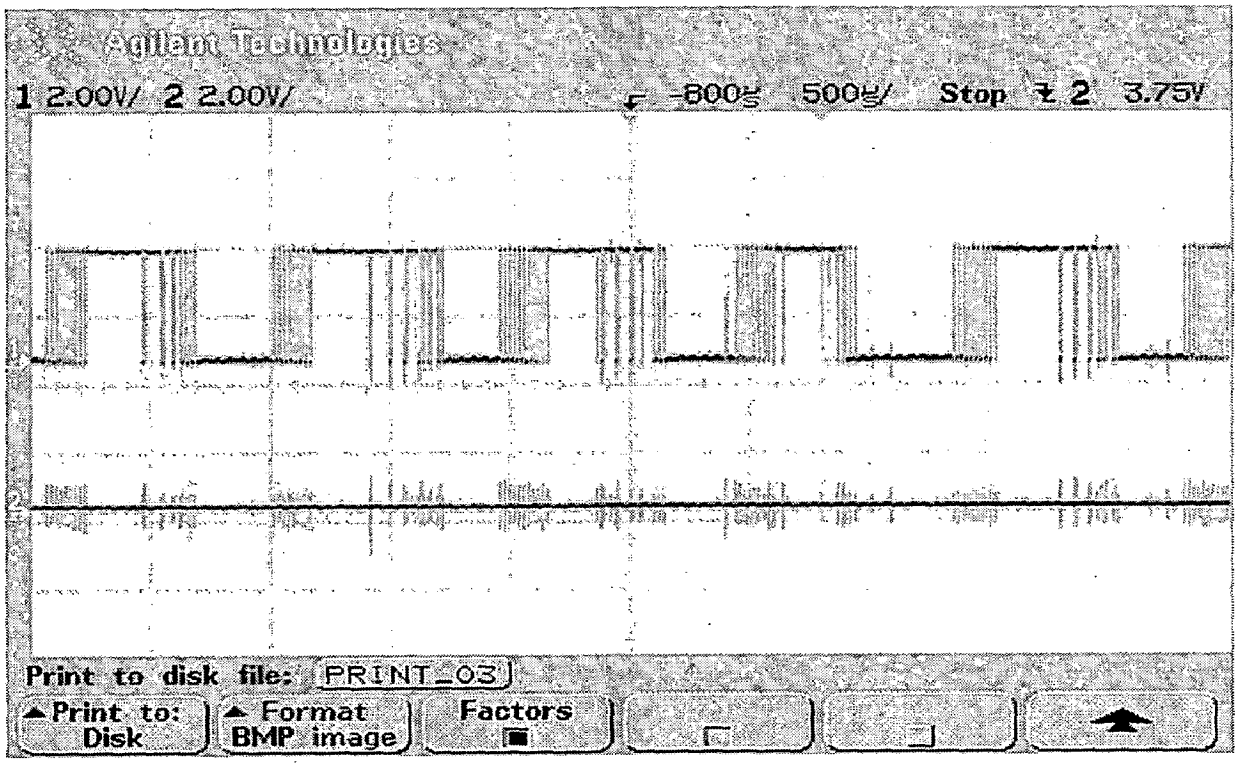

fig (6.7b) Gating Pulses when Converter Operated in Buck Mode

6.2.3.4 Experimental Result of -7.5° Module:

Various readings for this module are tabulated in table-(6.7) and gating signals are recorded when converter is operating in buck mode as well as in boost mode and these signals are shown in figure (6.8).

Table- (6.7)

Sl. No.	Table- (6.5) AC Input Voltage (Volts)	Chopper DC Input Voltage (Volts)	Chopper DC Output Voltage (Volts)	% Duty Cycle	
				SW1	SW2
1	200	76.7	98	100	25
2	256	100	98	100	0
3	400	159	104	65	0

Table –(6.7) Experimental Reading of -7.5° Module

From the table following observation has been made:

$$\% \text{ Boost} = \frac{98 - 76.7}{76.7} * 100 = 27.8 \text{ at } 200\text{V AC}$$

$$\%\text{Buck} = \frac{159 - 104}{159} * 100 = 34.6 \text{ at } 400\text{V AC}$$

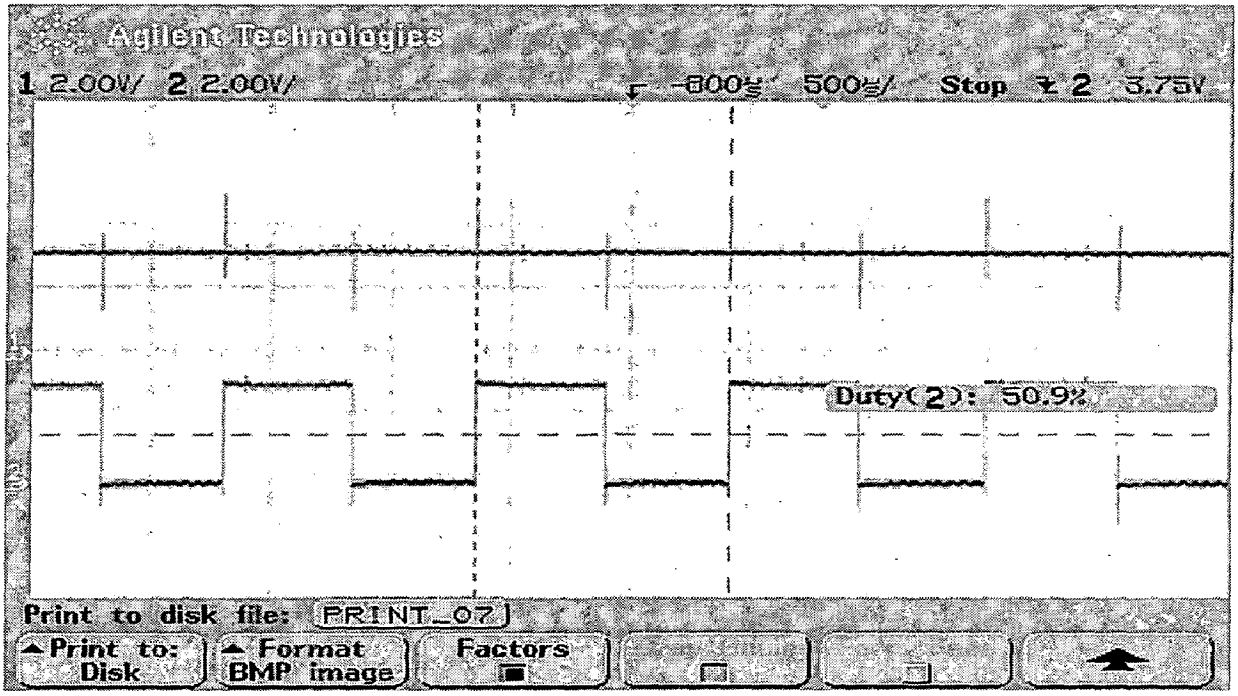

fig (6.9a) Gating Pulses when Converter Operated in Boost Mode

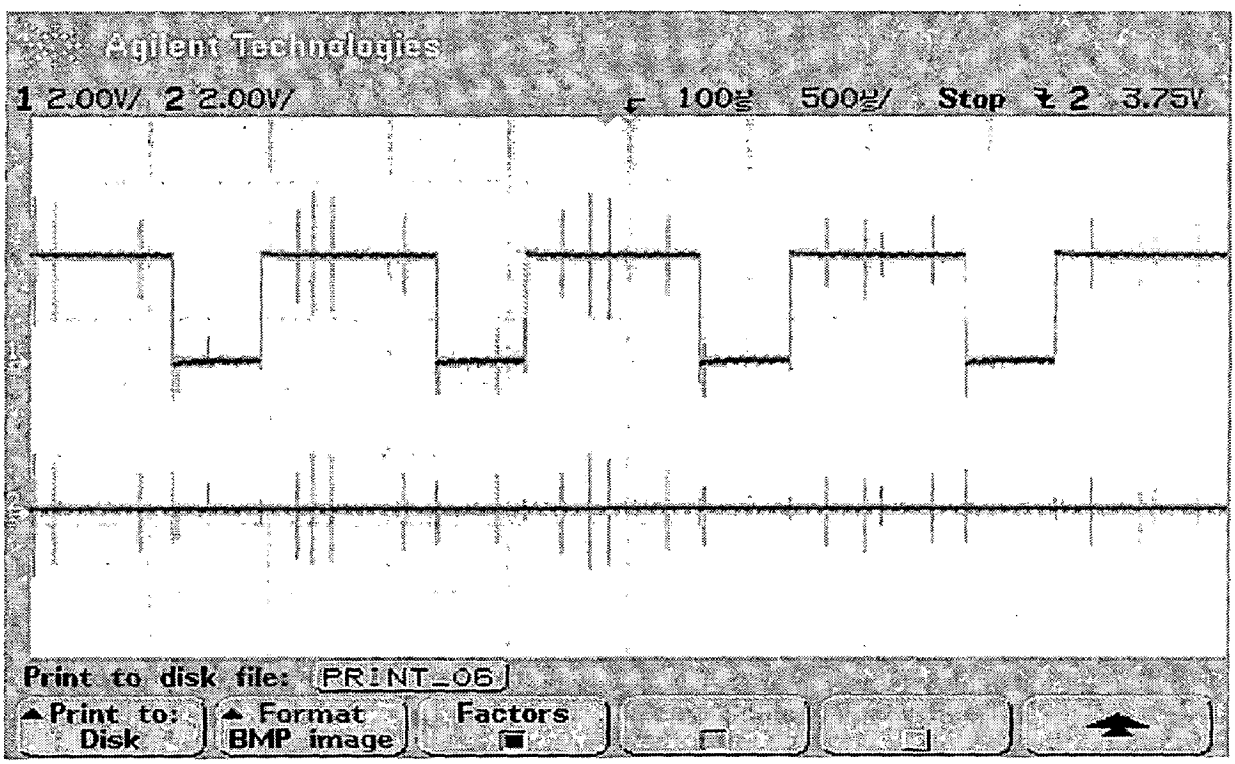

fig (6.9b) Gating Pulses when Converter Operated in Buck Mode

6.2.4 Boost Operation of All Modules :

All the modules are tested simultaneously at minimum operating voltage, input current and voltage waveform, power factor, THD of input current and voltage are measured and recorded by power quality analyzer. DC input voltages of all chopper and corresponding DC boost voltage of all modules at 200 volts AC input are tabulated in table-(6.9).

Table-(6.9)

+22.5° Chopper Voltage		+7.5° Chopper Voltage		-7.5° Chopper Voltage		-22.5° Chopper Voltage	
Input (Volts)	Output (Volts)	Input (Volts)	Output (Volts)	Input (Volts)	Output (Volts)	Input (Volts)	Output (Volts)
54	98.1	77.8	101	77.8	98.2	53.5	100

Table-(6.9) Maximum Boost Voltages of All Modules

6.2.4.1 Input Current in Boost Mode:

When converter is running in boost mode means input voltage is at minimum level of 200 volts AC then input voltage and current waveform is recorded as shown in figure (6.10). The expended view of input current is shown in figure (6.11) and it is clear from figure that input current is sinusoidal.

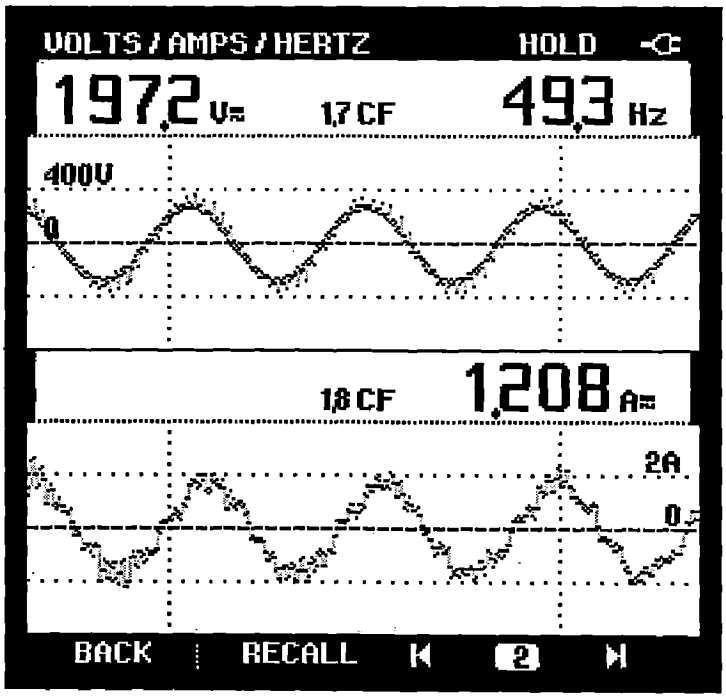

fig.(6.10) Converter Input Voltage & Current

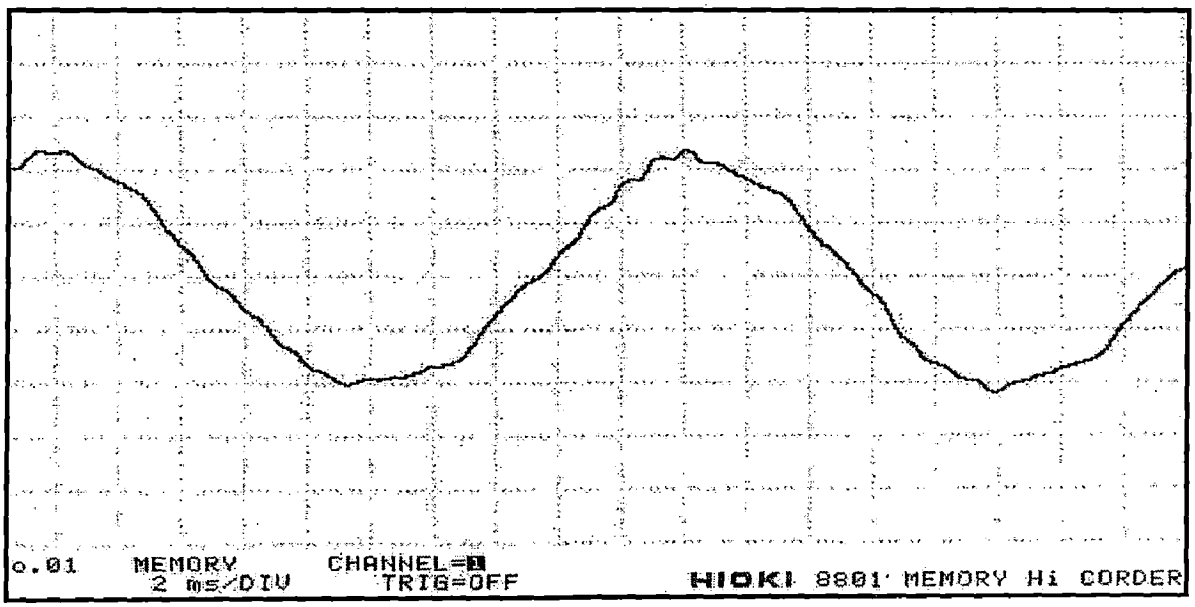

fig.(6.11) Expended View of Converter Input current

6.2.4.2 Input Power Factor:

When converter was operated in boost mode at minimum supply of 200V AC then input side power factor recorded by power quality analyzer as shown in figure (6.12). Input power factor is 0.8 which shows improvement in power factor as compare to ordinary 6-pulse converter.

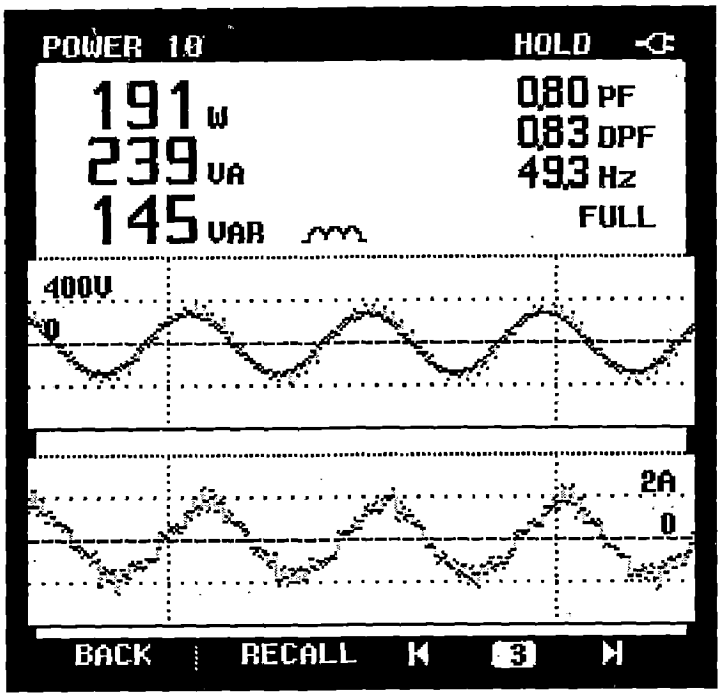

fig. (6.12) Input Side Power Factor

6.2.4.3 THD of Input Current:

Total Harmonic Distortion of input current have been analyzed by power quality analyzer and harmonic spectrum of input current is recorded as shown in figure (6.13). THD is come out to be 16.8%

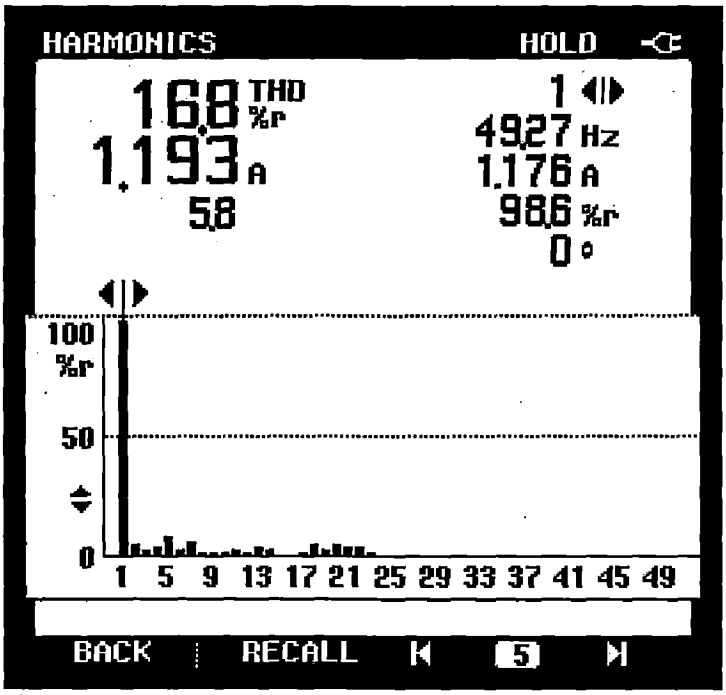

fig. (6.13)Harmonic Spectrum of Input Current

6.2.5 Buck Operation of All Modules :

All the modules are tested simultaneously at maximum operating voltage, input current and voltage waveform, power factor, THD of input current and voltage are measured and recorded by power quality analyzer. DC input voltages of all chopper and corresponding DC buck voltage of all modules at 400 volts AC input are tabulated in table-(6.10).

Table-(6.10)

+22.5° Chopper Voltage		+7.5° Chopper Voltage		-7.5° Chopper Voltage		-22.5° Chopper Voltage	
Input (Volts)	Output (Volts)	Input (Volts)	Output (Volts)	Input (Volts)	Output (Volts)	Input (Volts)	Output (Volts)
115.9	101.5	168	104.2	159.6	103.9	117.5	101.3

Table-(6.10) Maximum Buck Voltages of All Modules

6.2.5.1 Input Current in Buck Mode:

When converter was running in boost (buck) mode means input voltage is at maximum level of 400 volts AC then input voltage and current waveform is recorded as shown in figure (6.14).The expended view of input current is shown in figure (6.15) and it is clear from figure that input current is peaky in nature that is just because of increase of third harmonic component.

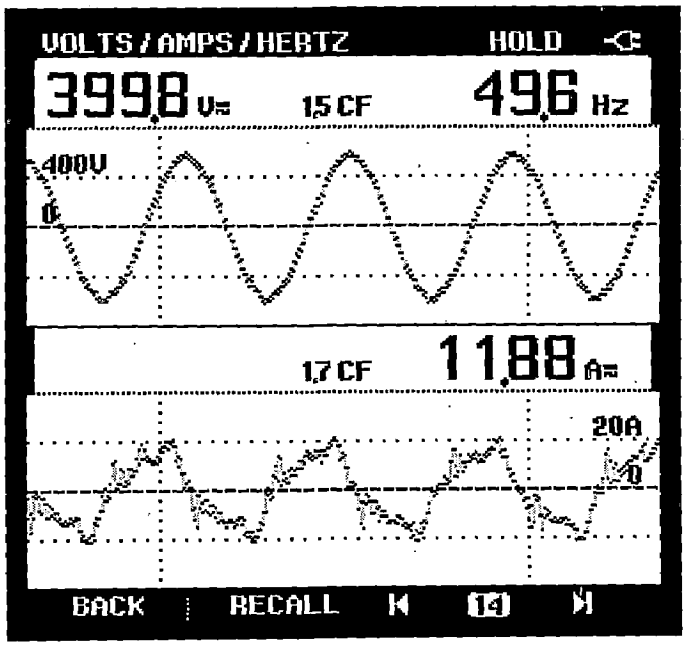

fig.(6.14) Converter Input Voltage & Current

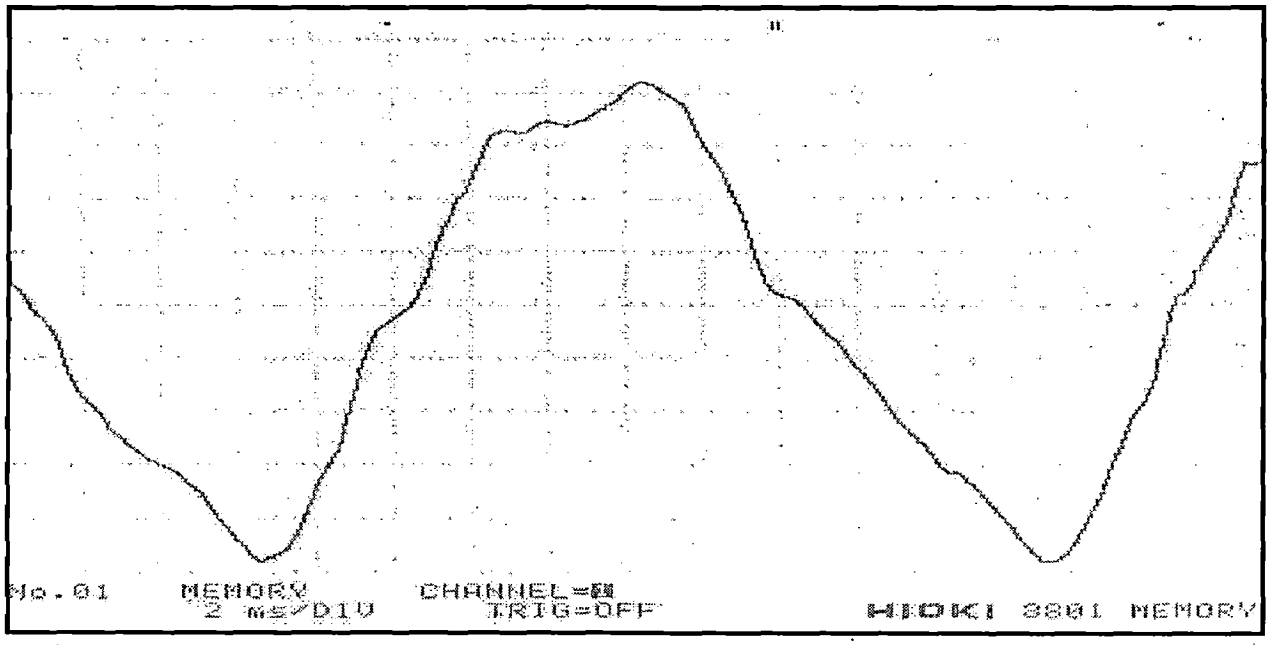

fig.(6.15) Expended View of Converter Input Current

6.2.5.2 Input Power Factor:

When converter was operated in buck mode at maximum supply of 400V AC then input side power factor recorded by power quality analyzer as shown in figure (6.16). Input power factor is 0.32.

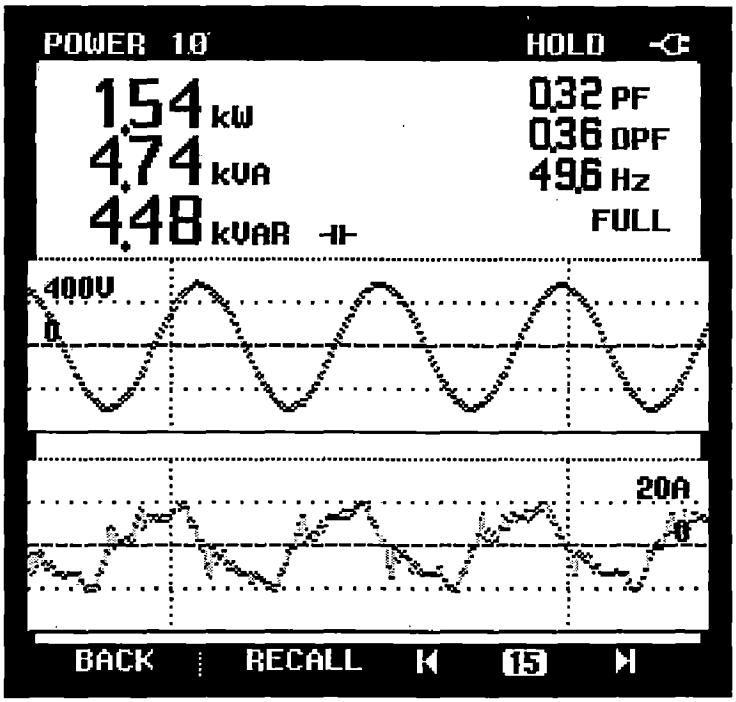

fig. (6.16) Input Side Power Factor

6.2.5.3 THD of Input Current:

Total Harmonic Distortion of input current have been analyzed by power quality analyzer and harmonic spectrum of input current is recorded as shown in figure (6.17). THD is come out to be 30.6% and there is another drawback that is increased in third harmonics.

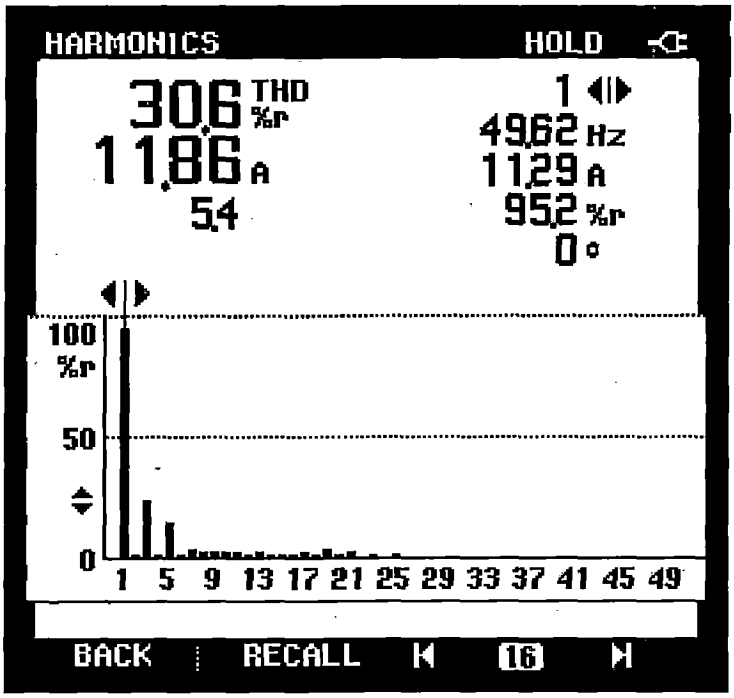

fig. (6.17)Harmonic Spectrum of Input Current

6.2.6 Uncontrolled Operation:

An uncontrolled operation of developed converter is also achieved by connecting uncontrolled DC output of all the rectifier modules in series. This combination produces high voltage DC link. A load of 200 ohms is connected across it. Converter input voltage and current are recorded and shown in figure (6.18). It can be noted that input current is almost sinusoidal.

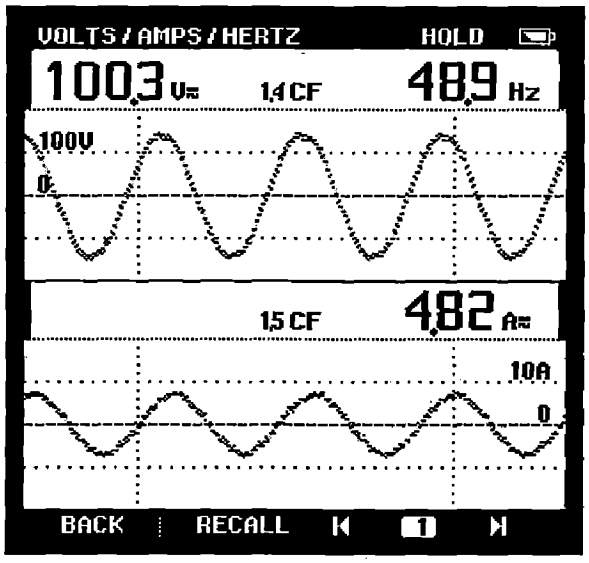

fig. (6.18) Input Current and Voltage

6.2.6.1 Input Power Factor:

When converter was operated in uncontrolled mode at input supply 100V AC then input side power factor recorded by power quality analyzer as shown in figure (6.19). Input power factor is 0.82 that proves one of the advantages of multi-pulse AC/DC converter.

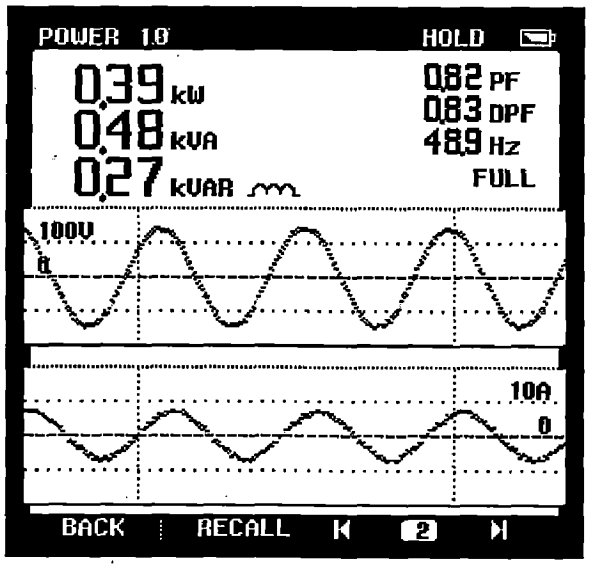

fig. (6.19) Input Side Power Factor

6.2.6.2 THD of Input Current:

Total Harmonic Distortion of input current have been analyzed by power quality analyzer and harmonic spectrum of input current is recorded as shown in figure (6.20). THD is come out to be 5.1% which full fill the IEEE-519 standard.

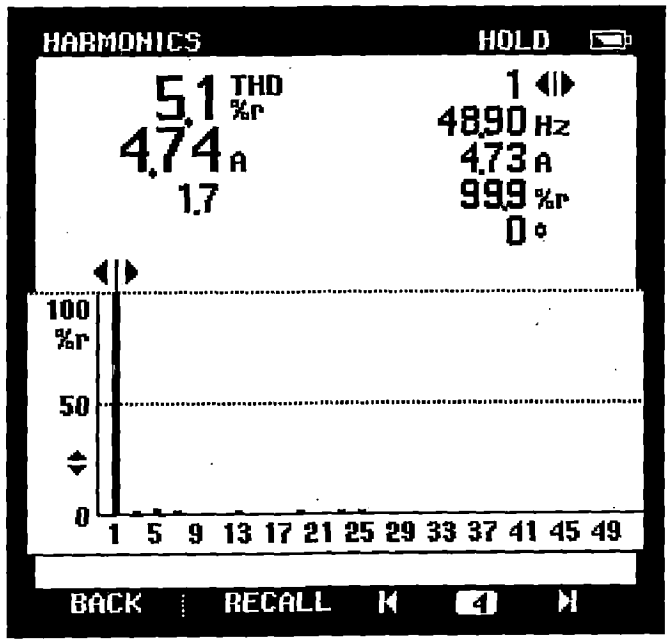

fig. (6.20)Harmonic Spectrum of Input Current

6.3 Control Circuits:

To develop a system we required control circuit to get the desired output some circuitry required for this purpose is common like, DC power supply for the control circuitry, Gate driver circuit and measurements circuit like DC link voltage measurement, Current measurement etc. These are common in all the systems and are developed using standards method which are easily available. Apart from these circuits Triangular Carrier Generator, Programmable Controller Circuit for error calculation and PWM pulse generation and Mode Selection Circuit are made to have full control over system.

6.3.1 Power Supply Circuits

DC regulated power supplies (+12v, -12v, +5v) are required for providing biasing to various transistors, IC's etc. The circuit diagram for various dc regulated power supplies are shown in figure (6.21) in it the single phase AC voltage is stepped down to 12V and then rectified using a diode bridge rectifier. A capacitor of 1000μf, 50volts is connected at the output of the bridge rectifier for smoothening out the ripples in the rectified DC regulated voltages. IC voltage regulators are used for regulating the voltages on load also. Different IC voltage regulator that are used are; 7812 for +12V, 7912 for -12V and 7805 for +5V. A capacitor of 100μf, 25V capacitor is connected at the output of the IC voltage regulator of each supply for obtaining the constant and ripple free DC voltage. The data sheets for Voltage Regulators specified above are given in Appendix – C.

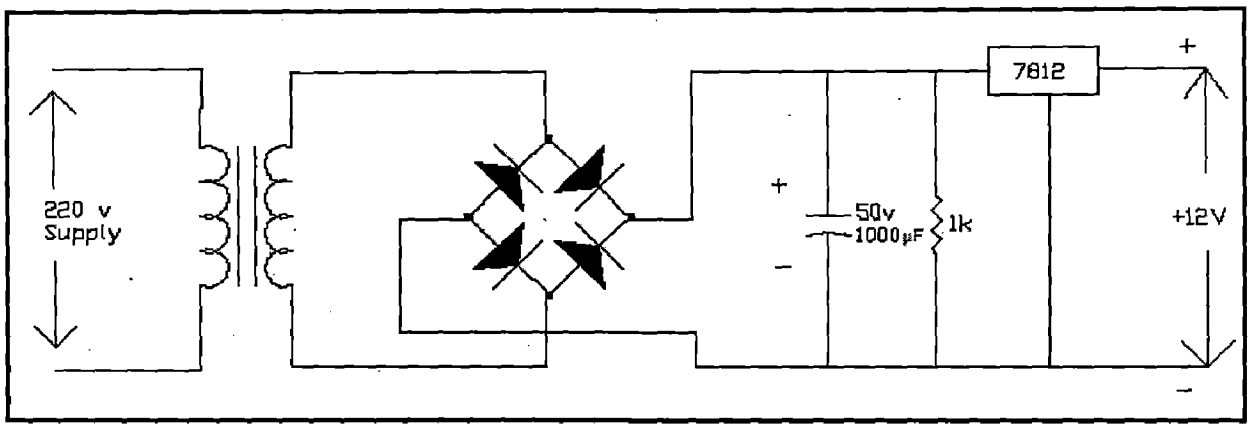

fig. (6.21a) +12V D.C. Supply

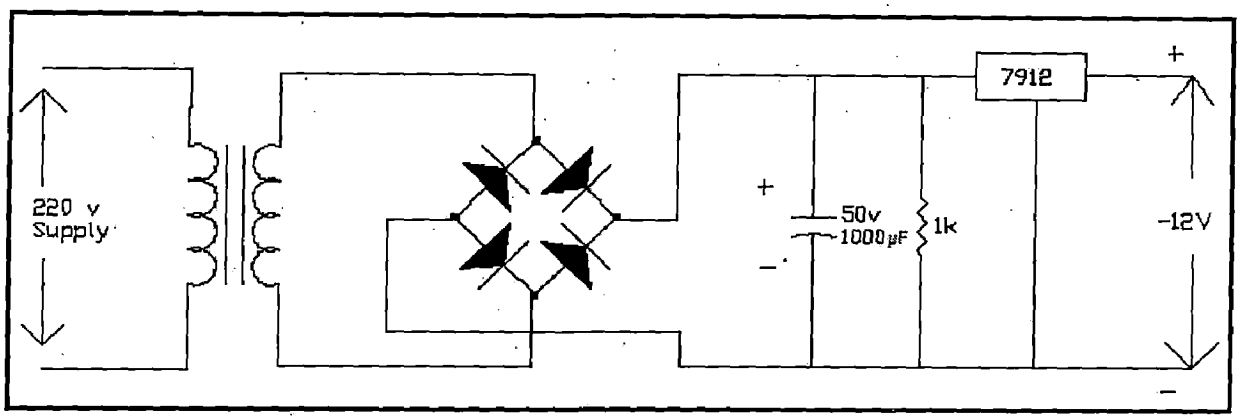

fig. (6.21b) -12V D.C. Supply

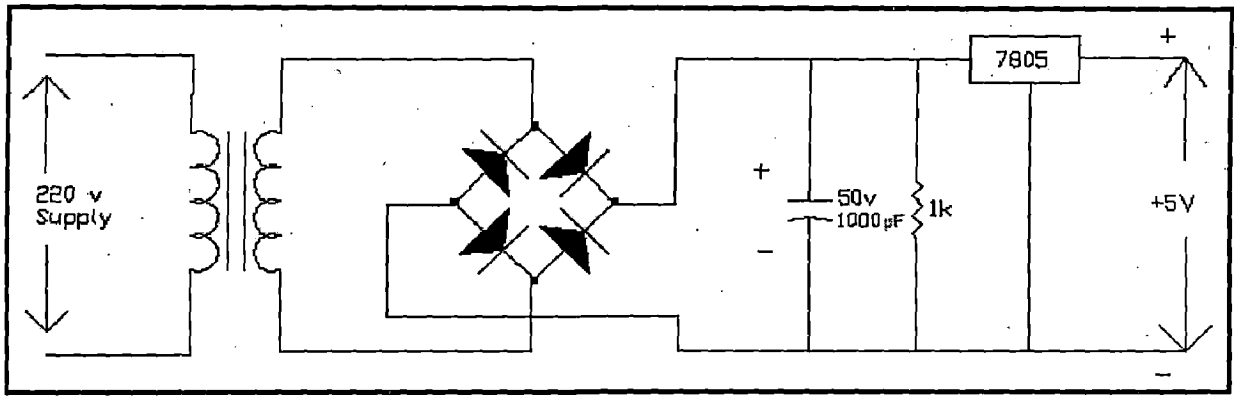

fig. (6.21c) +5V D.C. Supply

6.3.2 Voltage Sensing Circuit :

Voltage sensing circuit is used to measure of voltage across the output capacitor. The DC output voltage is sensed through isolation amplifier AD202 for the voltage control of the converter. AD202 provide the total galvanic isolation between input and output stages of the isolation amplifier through the use of internal transformer coupling. It gives a bi-polar output voltage $\pm$8V, adjustable gain range from 1v/v to 100v/v, +0.025% max non-linearity, 130db of CMR and 75mw of power consumption. Circuit diagram is shown in figure (6.22) and for IC configuration and special features refer to the Appendix - C. In the shown figure output amplifier is made using op-amp which will be helpful in calibration. The transient response will deteriorate by using passive filter at the input side of AD202.

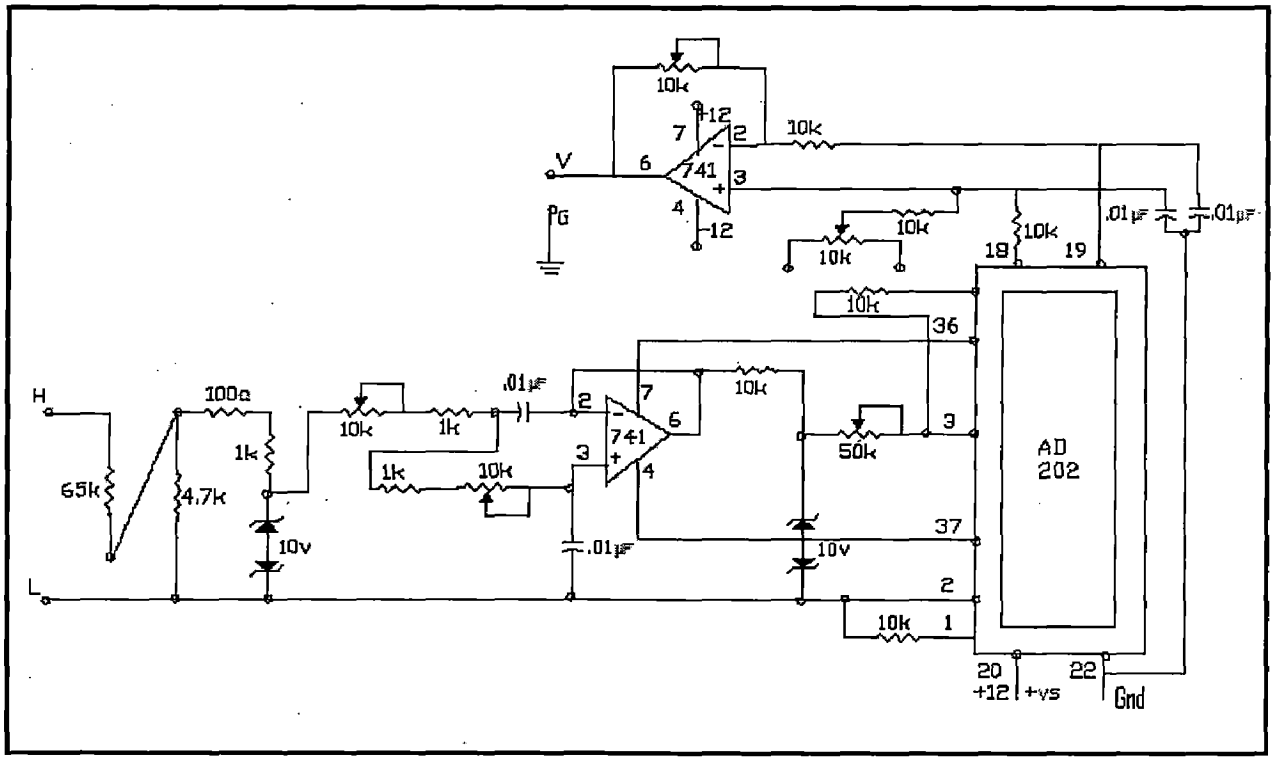

fig. (6.22) AD 202 Based Voltage Sensing Circuit

6.3.2.1 Operating Principal :

DC input is fed to a potential divider by adding a resistance of 65k; 2 Watt so that maximum voltages drop is less. The output of AD 202 goes to scaling amplifier to scale the feedback level. The output voltage scaled at 3V for 150V. The voltage is fixed at zero by varying the offset resistance. Saturation level of IC-741 is to be taken into account while measuring the output voltage. It can be seen that IC 741 saturates at the voltage level of 3.8 Volts. So voltage is scaled unto 3.8 V and then it is fed to the isolation amplifier through this inverting amplifier. Separate grounding was provided to the input as well as the power supply.

6.3.3 Current Sensing Circuit with OLT:

For sensing the load current TELCON HTP 25 current sensor is used. The output of current sensor is given to unity gain OP-AMP [27]. For the elimination of harmonics low pass filters has been used. For instantaneous current monitoring since no phase delay is required the filter must be tuned to a cut-off frequency, which is set for the end of the fundamental frequency so that phase lag is minimum. But if we choose a high value of cut off frequency it will result a relatively reduced attenuation factor to the higher order harmonics. The current sensing circuit is calibrated in ratio 10A to 5V. The calibrated output of current sensor is compared with reference current, and when ever device current goes above reference current the over load trip signal generated which is latch trough IC 7474.This latch signal is ANDED with PWM signal through IC 7408 and its output is overload protected PWM signals. Circuit diagram is shown in figure (6.23).

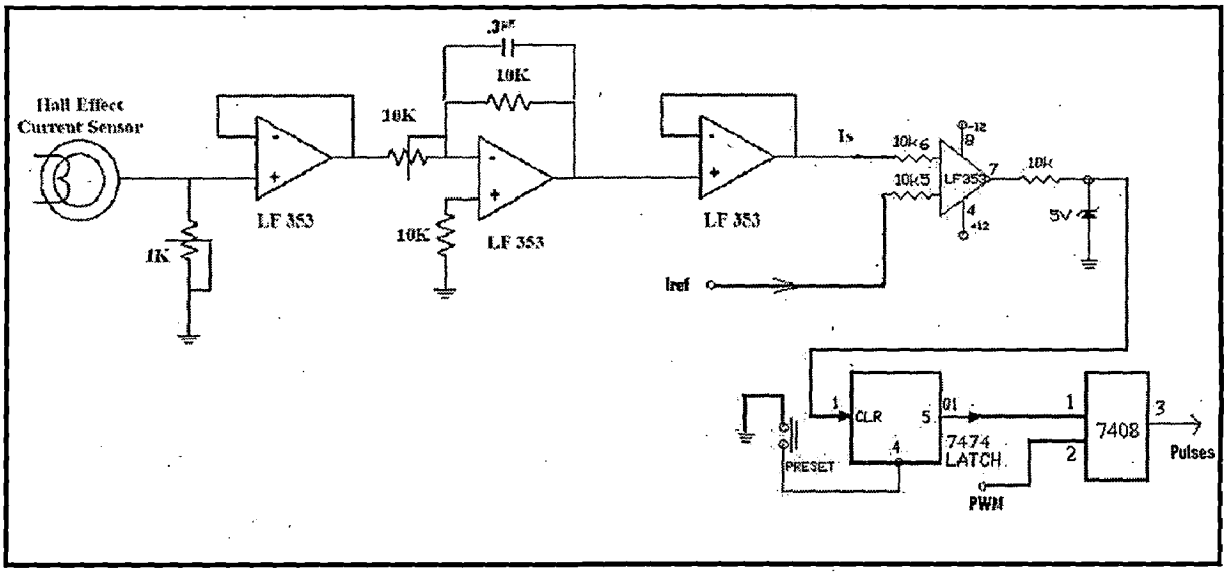

fig. (6.23) Current Sensing Circuit With OLT

The advantages and disadvantage of using current sensor are as fallows :

Advantages:

- Galvanic isolated.
- May be used for both AC and DC measurements.
- Simple to implement.
- High measuring accuracy < 1% uncertainty.
- Wide frequency range.

- Good overall accuracy.
- Fast response time.
- Low temperature drift.
- Excellent linearity.
- No insertion losses

Disadvantages:

- Relative expensive.
- Requires bipolar (+/-) power supply.

6.3.4 Gate Driver Circuit :

The driver circuit is used to provide electrical isolation between control circuit and power circuit. The most common way is the control of the IGBT via gate resistor. To reach the required levels, the gate driver must be able to switch safely and reliably and must provide full protection for every state of operation, for itself as well as for the given application. The circuit diagram is shown in figure (6.24).

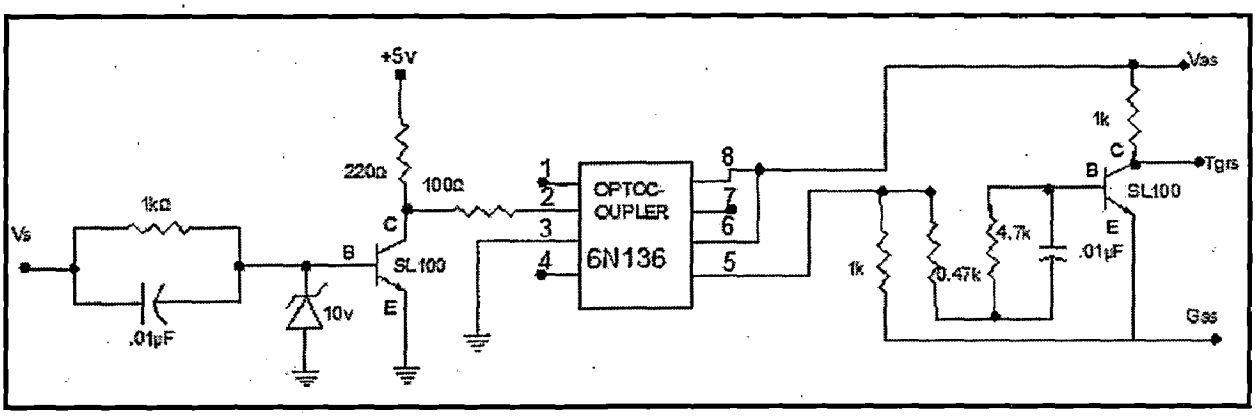

fig. (6.24) Gate Driver Circuit

The circuit can be seen into two parts one part is input side of driver circuit and other is the output side of driver side. On input side a supply of +5 volts is given and on output side isolate +12 volts supply is given to the circuit. The pulses are given at 1 kHz frequency generated by a PWM generator. The circuit gives the same firing pulses as given on input side both input side and output side grounds are isolated from each other. The firing pulses used may not be strong enough to turn ON the IGBT so these pulses are amplified. Similarly the isolation between power circuit and control circuit is essential requirement especially in the micro controlled system in which sophisticated devices are used since they don't have transient and withstand capability. For isolation an OPTOCOUPLER 6N136 is used with additional circuitry as shown in above figure.

6.3.5 Triangular Carrier Generator :

To trigger chopper devices sw1 and sw2 we need firing pulses for this purpose we need to modulate high frequency signal with low frequency signal this technique is known as modulation. When a high frequency signal has amplitude varied in response to a lower frequency signal we have AM (amplitude modulation). When the signal frequency is varied in response to the modulating signal we have FM (frequency modulation). These signals are used for radio modulation because the high frequency carrier signal is needed for efficient radiation of the signal. When communication by pulses was introduced, the amplitude, frequency and pulse width modulation become possible modulation options. In many power electronic converters where the output voltage can be one of two values the only option is modulation of average conduction time.

To generate the high frequency triangular carrier wave a PLL is used . The operating principal of PLL is as fallows:

6.3.5.1 Operating Principal:

A PLL is a device which continuously tries to track the phase of the incoming signal. It is realized by a phase detector, a loop filter, and a voltage controlled oscillator (VCO). The block diagram is shown in figure (6.25). The phase detector compares the phase of the input signal with that of the VCO, and its output voltage is filtered and applied to the VCO whose output frequency moves in the direction so as to reduce the phase difference of the input signal and output of VCO. When the loop is locked, the frequency of the VCO is exactly equal to the average frequency of the input signal. This is the main advantage of using PLL based triangular carrier generator since the frequency of generated triangle carrier is fixed it reduced the unwanted harmonic which are generated because of change in carrier frequency.

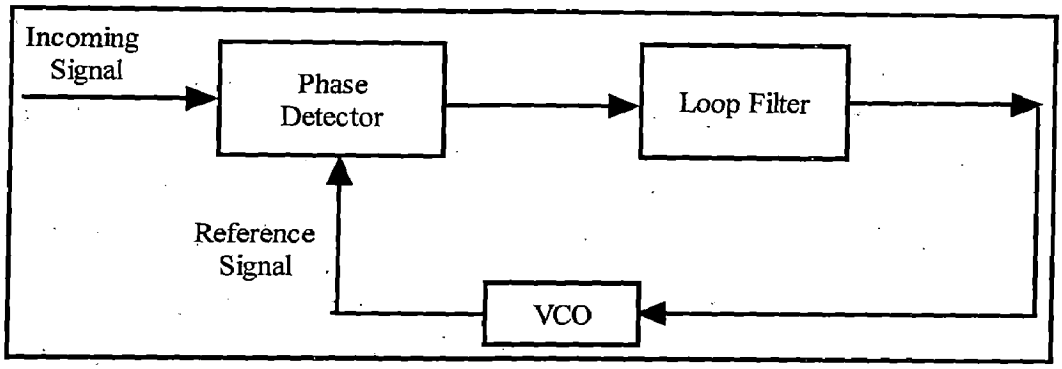

fig. (6.25) Block Diagram of PLL Circuit

6.3.5.2 Circuit Diagram :

For Generation of triangular carrier PLL IC NE565 is used to generate square pulse of 1kHz.After that a two stage frequency divider circuit is used to fed back the VCO input signal to pin 5 of 565. For frequency dividing 7492 and 7493 IC are used. The VCO is locked with supply frequency that is inputted to pin no. 2 of 565. After that Op-amp LF 353 are used to generate triangular carrier. The complete circuit diagram is shown in figure (6.26). The generated triangular carrier for all the four module is shown in figure (6.27) and synchronization with supply frequency is shown in figure (6.28).

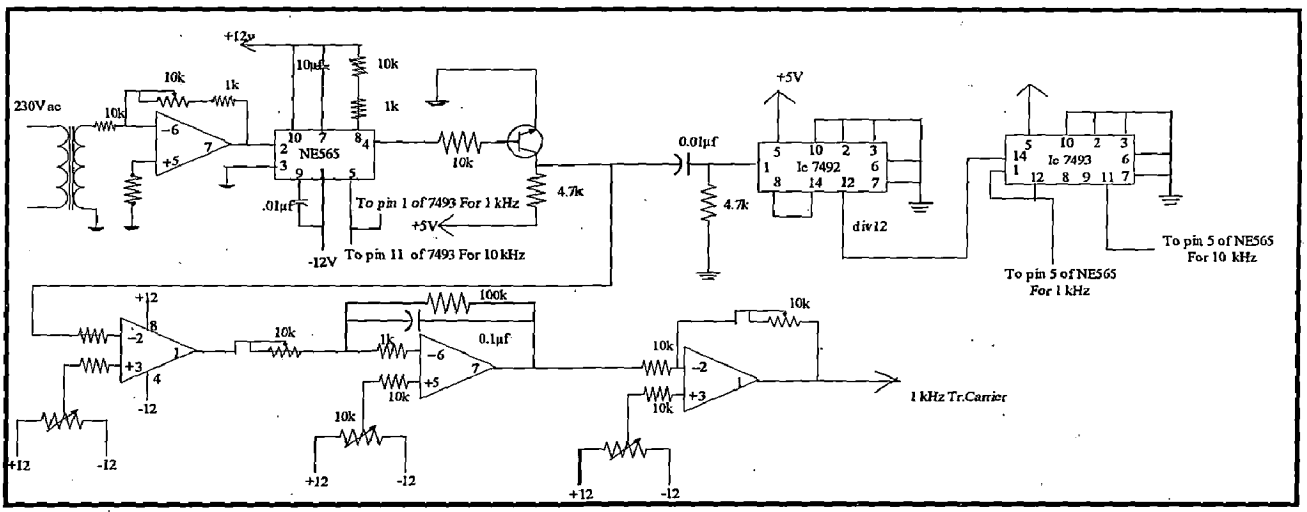

fig. (6.26) PLL Based Triangular Carrier Generator

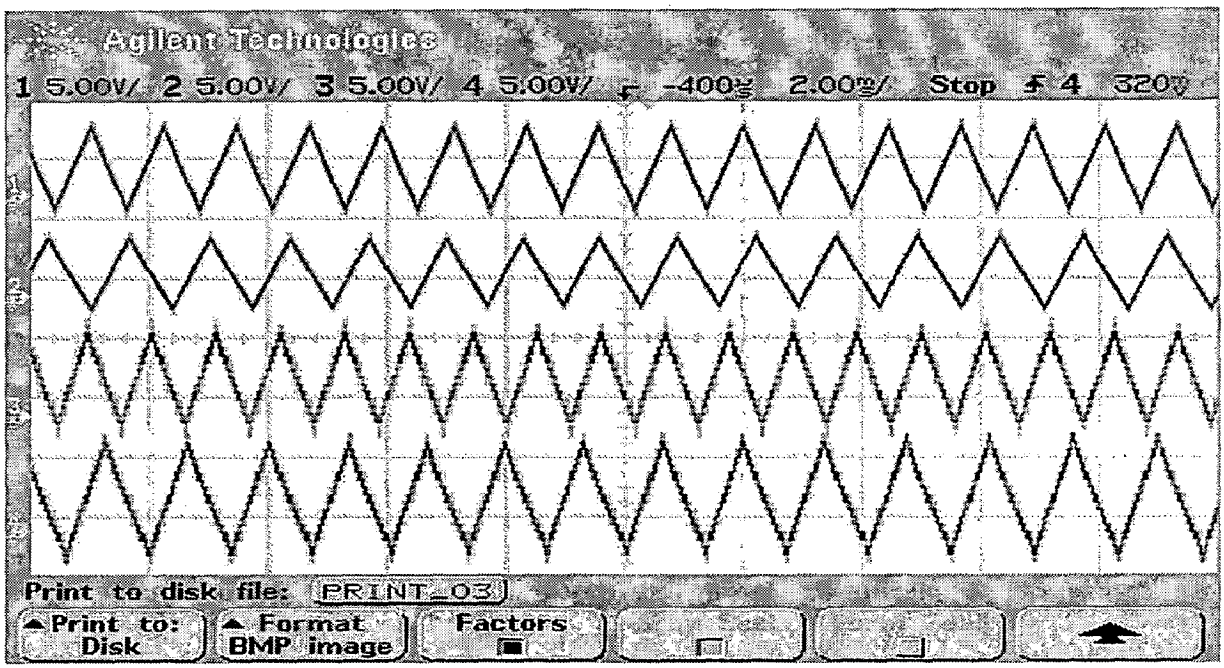

fig. (6.27) Generated Triangular Carrier for all the Four Modules

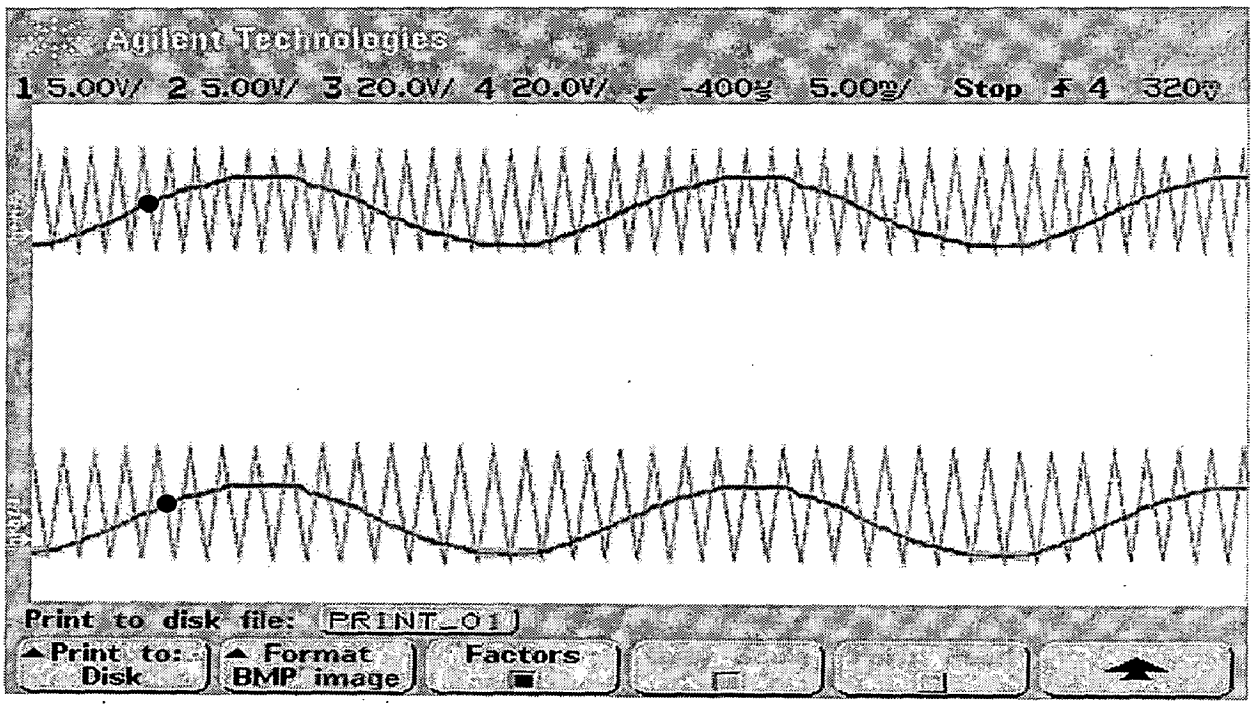

fig. (6.28a) Synchronization With Supply Frequency for Module 1&2

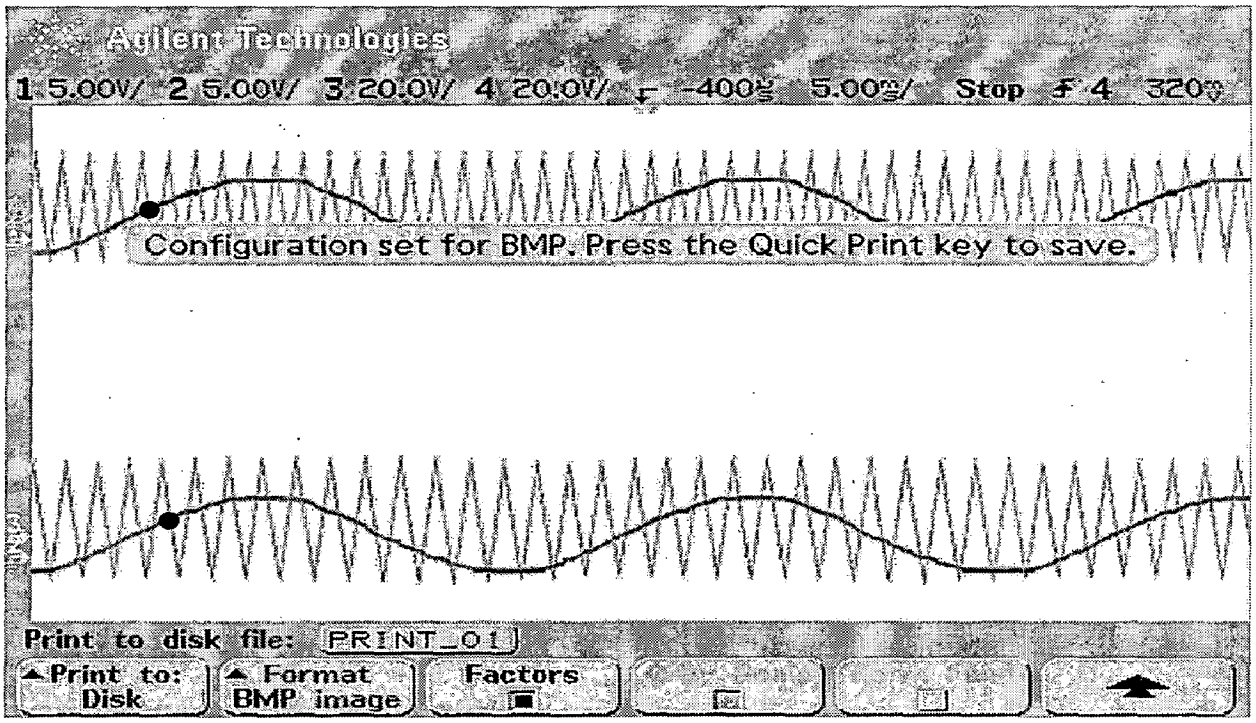

fig. (6.28b) Synchronization With Supply Frequency for Module 3&4

6.3.6 Programmable Controller Circuit :

Programmable controller circuit consists of error estimation block and a comparator circuit. In this dissertation eight such type of circuit are made, four for SW1 of all four module and four for SW2 of all four module. Error estimation block take the actual output DC signal as a feed back and generate the error accordingly this error is compared with triangular carrier in third comparator. When the triangular voltage rises above the error voltage, comparator output goes to high level and in reverse case comparator output is low. This gives a square wave output to the IGBT driver circuit. Since there was heavy unbalancing in uncontrolled DC output so to get same DC level at the output of chopper this type of controller circuit design. This controller circuit is design to get 100 volts DC for the whole range of supply that is 200V-400V AC. The circuit diagram of programmable controller for SW1 and SW2 is shown in figure (6.29a & b) respectively and generated PWM signal are shown in figure (6.30).

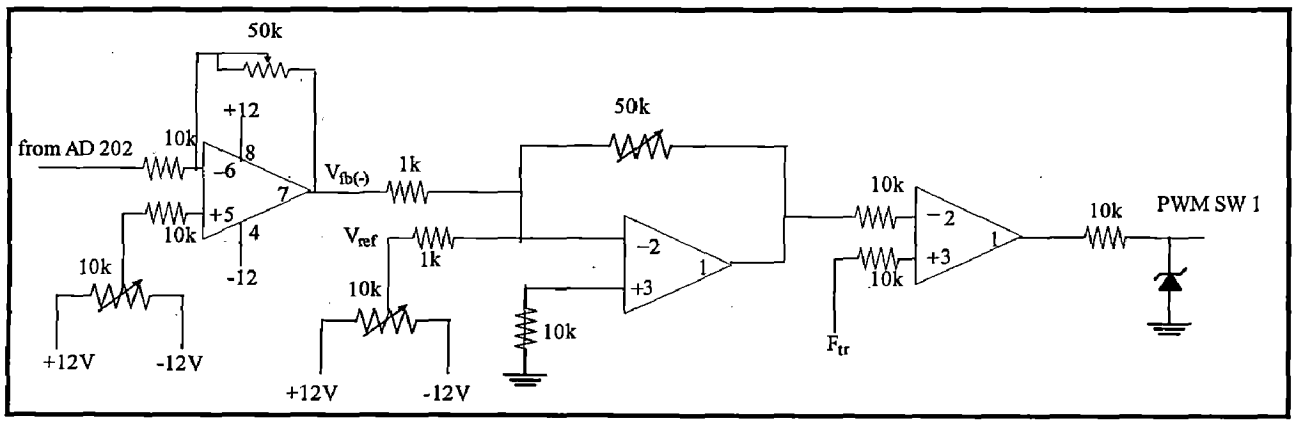

fig. (6.29a) Programmable Controller for SW1

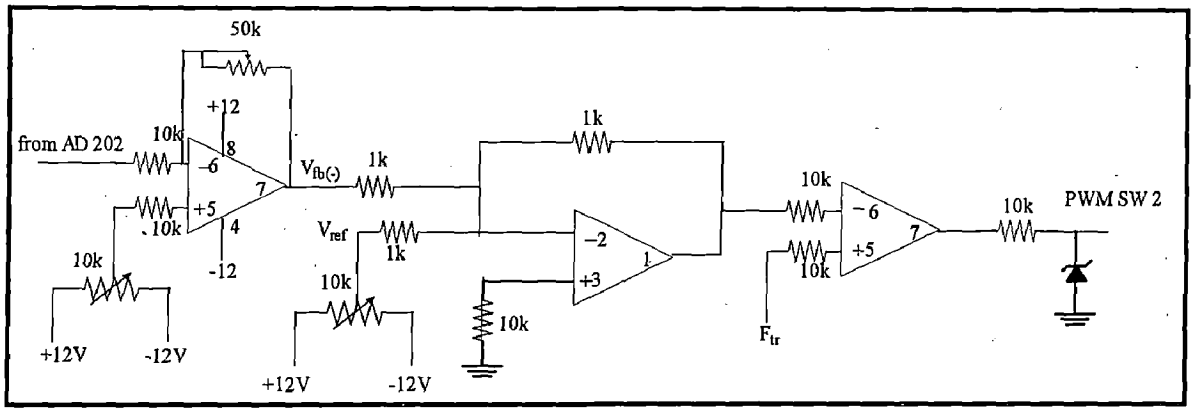

fig. (6.29b) Programmable Controller for SW2

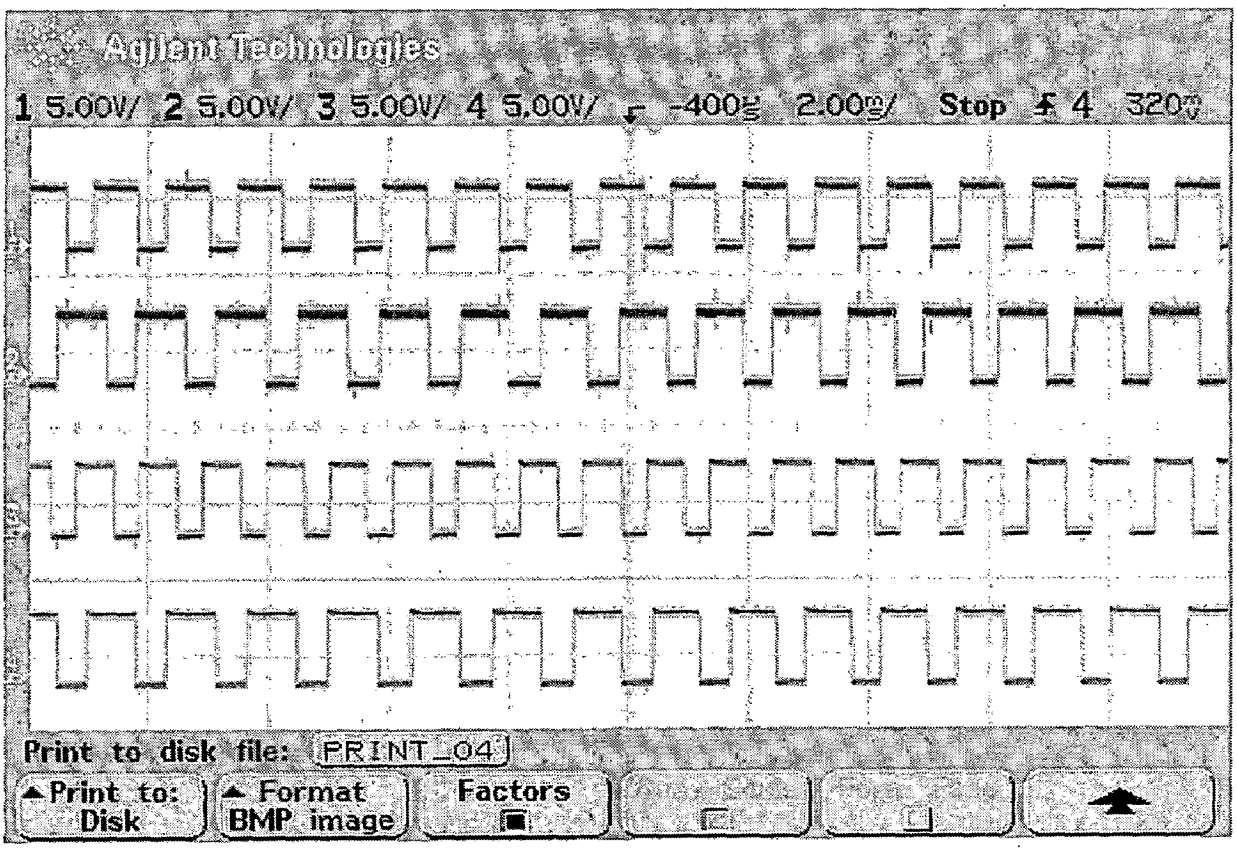

fig (6.30) Generated PWM Signal for All The Four Module

6.3.7 Mode Selection Circuit:

Mode selection circuit is used to set operating mode of chopper. If DC output goes below desired level then Boost mode select bit gets high and chopper operate in Boost mode until desired level of output is not achieved. If DC output goes beyond desired level then Buck mode select bit gets high and chopper operate in Buck mode until desired level of output is not achieved. In the implemented converter desired level is set to 100 volts DC, Mode selection circuit takes the output of AD202 as a feed back and compare it with desired level that is 2 volts (equivalent to 100V DC), according to this comparison result particular bit gets high. The PWM signals generated by controller circuit for SW1 and SW2 are ANDED with generated mode selection bit and finally pulses are generated for SW1 and SW2. Circuit diagram of implemented Mode Selection Circuit is shown in figure (6.31).

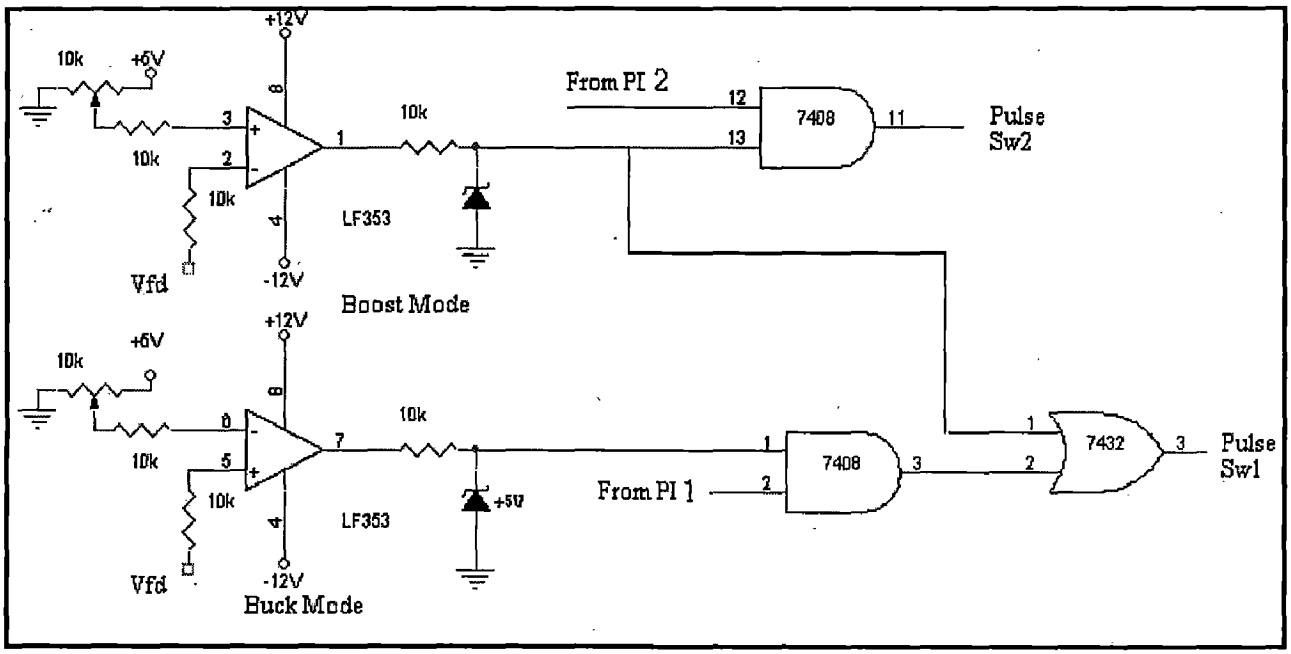

fig. (6.31) Mode Selection Circuit

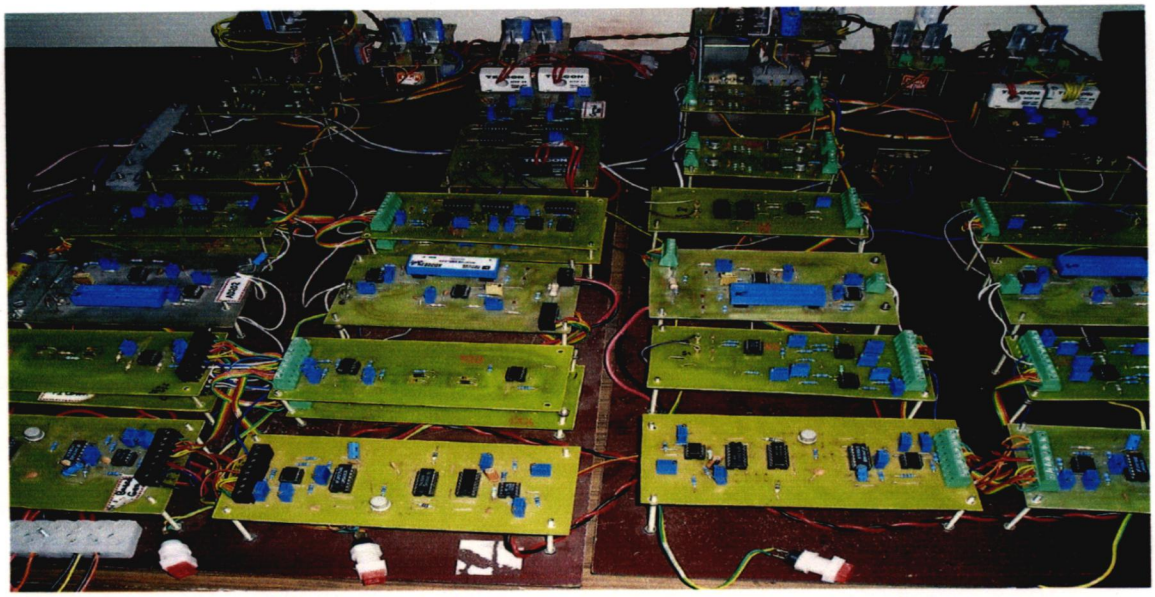

Photo Graph of Developed Control Circuit of Converter

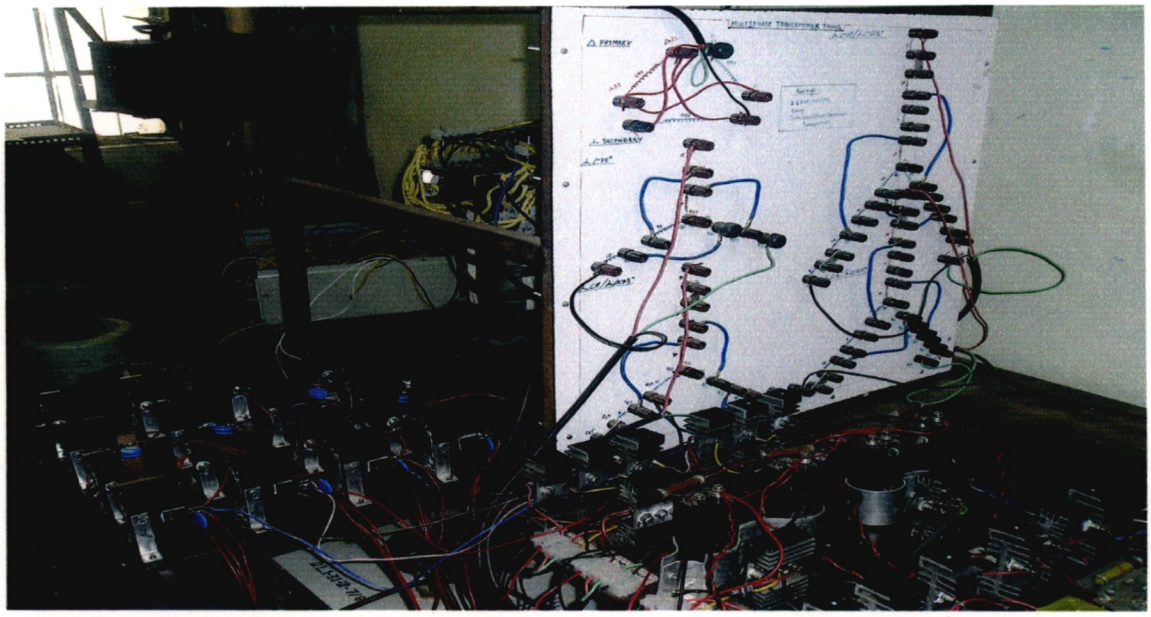

Photo Graph of Developed Power Circuit of Converter

Chapter 7

Conclusion and Future Scope

Conclusion:

There is a need to compensate the harmonic in AC/DC converter, to achieve this multi-pulse AC/DC converter are used. In this dissertation a 24-pulse buck-boost converter is simulated and simulation results are verified by developing a prototype model of converter system.

The proposed topology is implemented in simulation to estimate the performance. It is found to be satisfactory. Simulation study is carried out for 6-pulse, 12-pulse and 24-pulse converter to study the comparative performance of each type of converter system. It is observed from the simulation results that THD of input current of 6-pulse converter is poorest which contain the 5^{th} and 7^{th} harmonic in the ranges of 22% and 10% while in 12-pulse these harmonics component are in the order of 0.2% and 0.14% but 11^{th} and 13^{th} are increased up to 5.03% and 2.11% respectively. In the case of 24-pulse uncontrolled converter THD of input current is found to be 4.74% and all lower order harmonics component are absent, THD satisfy the IEEE-519 standards.

Simulation study is also carried out for 24-pulse buck-boost converter which is having heavy unbalancing in transformer secondaries winding. Simulation is carried out at minimum and maximum supply voltage and it is found that DC output voltage of all the modules are 100V irrespective of supply voltage whether it is 200V AC (minimum level) or 400V AC (maximum level).

THD of input current at 1 kHz switching frequency, in Boost mode is 7.57% and in Buck mode it is 13.68% which is higher because switching frequency of chopper is very low that is 1 kHz. At 10 kHz switching frequency THD is observed 5.39% and 4.72% for Boost and Buck mode respectively. Power factor is also measured at 10 kHz and it is 0.7 and 0.63 for Boost and Buck mode respectively.

The second phase of presented dissertation work was experimental validation of the simulation model developed in MATLAB and for this a prototype model of 24-pulse buck-boost converter is developed in laboratory and experimental results are found almost tally the simulation results. Developed converter is operated at entire range of supply and it is found DC link voltage remains constant and there is also improvement in input supply power factor. Even though THD of input current comes

out some what higher, that is just because of heavy switching transient because of lower switching frequency of chopper that is 1 kHz, if we go beyond 10kHz THD may be improved as it is observed in simulation. Another cause of increase of this THD is we have not use any snubber circuit across the switching device if we use properly design snubber circuit then these harmonics may get reduced.

Future Scope:

Proposed scheme gives the solution of all the problems for which it is implemented but still there is lots of work has to be done. Some areas where further work can be done are as follows:

1) Generated triangular carrier suffers from integrator offset problem, this can be solve by quenching of integrator capacitor which requires extra circuit. Other solution is generate triangular wave digitally which requires costly EPROM. Future work can be done to rectify this offset problem.
2) The triangular carriers are generated by PLL, these triangular carriers are synchronized with individual phase shifted secondaries voltage; in order to reduce some unwanted harmonics in supply side. Due to this provision further scope of research exists in this area.
3) Developed converter can be configured in high voltage, low current (400V, 5A) mode in this configuration all the modules will be connected in series.
4) Developed converter can be configured in high current, low voltage (100V, 20A) mode in this configuration all the modules will be connected in parallel series.
5) Developed converter can be configured in medium voltage, medium current (200V, 10A) mode in this configuration four modules will be connected to make two set of module in which two modules are in parallel and then these two set are connected in series.

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[25] Leon M. Tolbert, Fang Z. Peng, "Multilevel Converters for Large Electric Drives," APEC '98, Anaheim, California, February 15-19, 1998, pp. 530-536.

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[27] Richard Dickinson and Shaun Milano, "Isolated Open Loop Current Sensing Using Hall Effect Technology in an Optimized Magnetic Circuit," Allegro MicroSystems, Inc.USA, 7/11/2002.

Web Resources:

www.robicon.com

www.google.com

http://ieeexplore.ieee.org

Books Referred:

i. IEEE Press Notes; "Power Electronics Converter Harmonics, Multi-pulse Methods For Clean Power" by K.A.Paice

ii. "Power Electronics CIRCUITS, DEVICES AND APPLICATION" by RASHID

iii. "Op-amps And Linear Integrated Circuits" by Gayakwad, R.A.

Simulation Parameter

1) Simulation parameter for 6-Pulse Converter (Article 5.2) is as follows:

   Line to Line Supply Voltage = 440V AC

   Load Resistance R_L = 100 ohms

   Load Inductance L = 1mH

   Output Filter capacitor = 100μF

2) Simulation parameter for 12-Pulse Parallel Converter (Article 5.3.1) is as follows:

   Line to Line Supply Voltage = 440V AC

   Load Resistance R_L = 100 ohms

   Load Inductance L = 4mH

   Inter Phase Reactor = 1mH

3) Simulation parameter for 12-Pulse Series Converter (Article 5.3.2) is as follows:

   Line to Line Supply Voltage = 440V AC

   Load Resistance R_L = 250 ohms

   Load Inductance L = 4mH

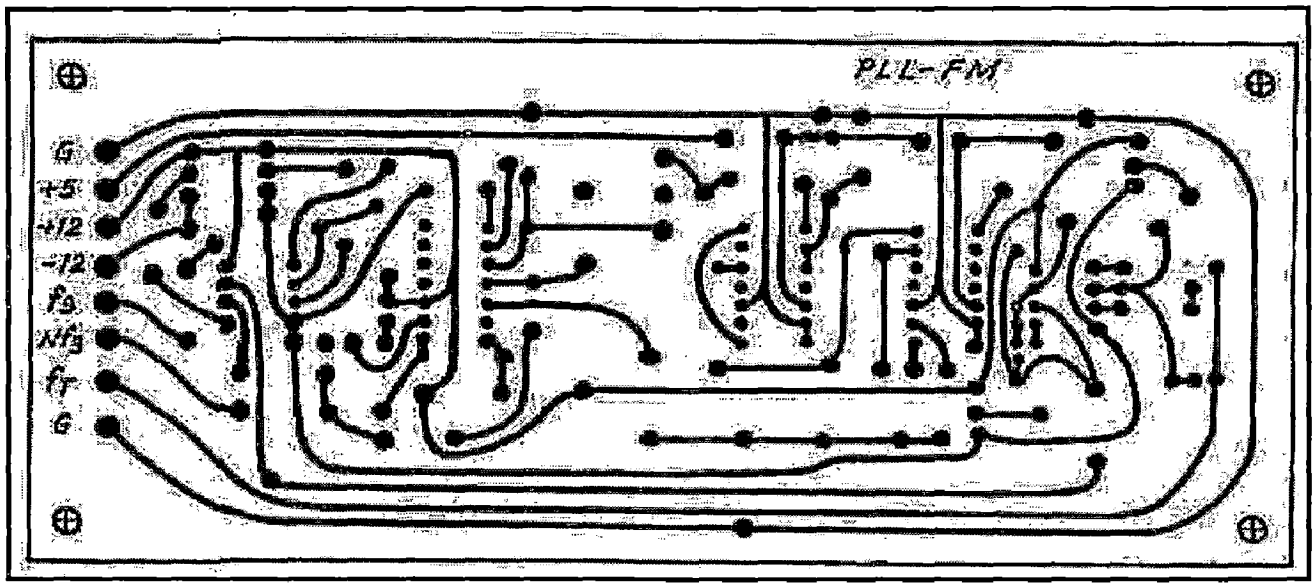
4) Simulation parameter for All 24-Pulse Converter is as follows:

   Line to Line Supply Voltage in Boost Mode = 200V AC

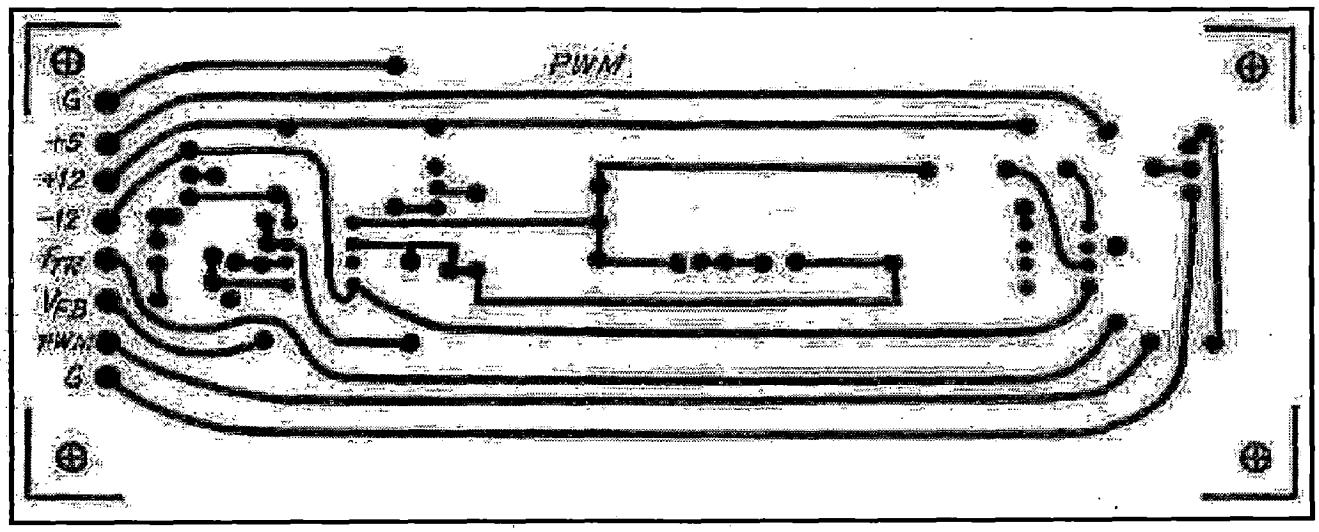
   Line to Line Supply Voltage in Buck Mode = 400V AC

   Load Resistance R_L = 200 ohms

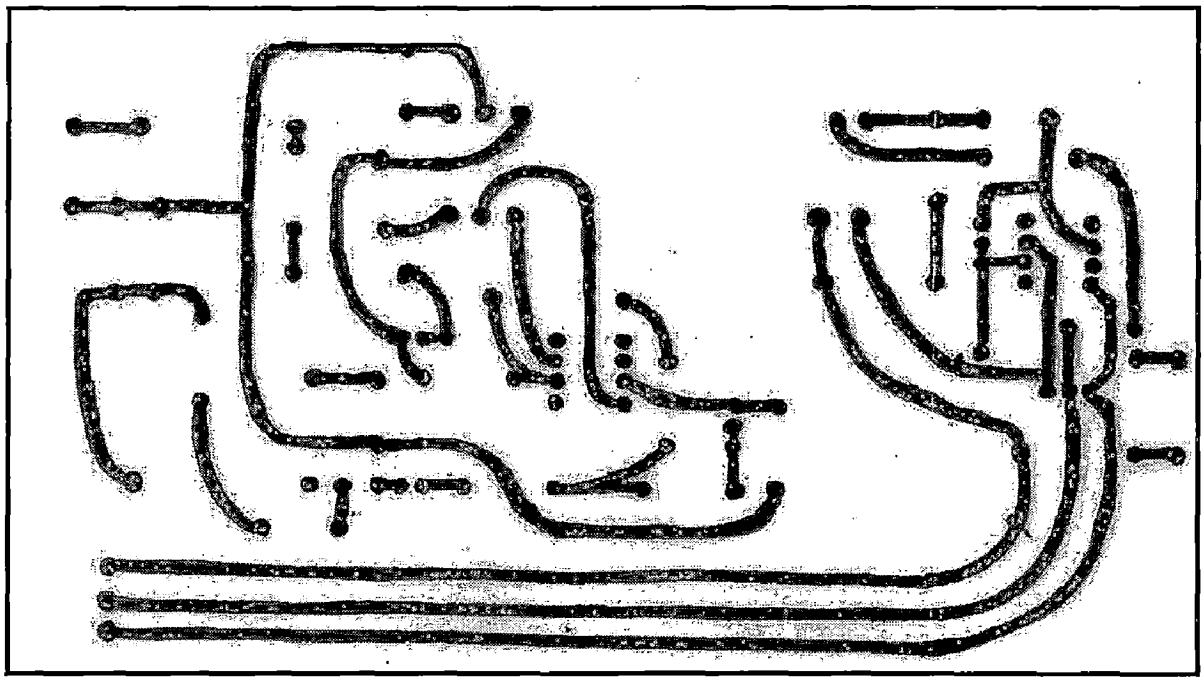
PCB Layouts



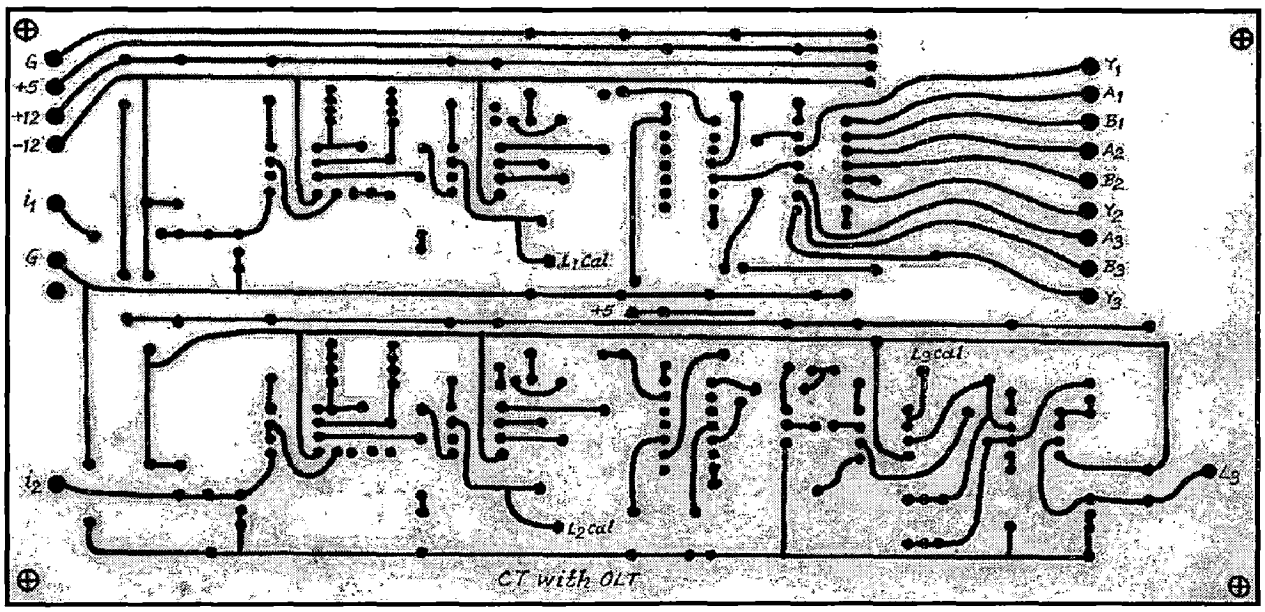
PCB Layout of PLL Based Triangular Carrier Generator



PCB Layout of Error Estimation and PWM Signal Generator



PCB Layout of AD 202 Based Voltage Sensing Circuit



PCB Layout of Current Sensing Circuit with Over Load Trip

Appendix-C

Sample of Data Sheets

NE/SE565
Phase-Locked Loop

Product Specification

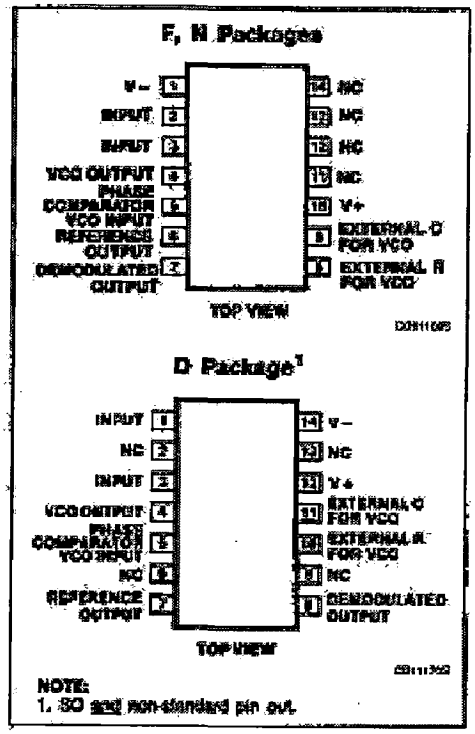
DESCRIPTION

The NE/SE565 Phase-Locked Loop (PLL) is a self-contained, adaptable filter and demodulator for the frequency range from 0.001Hz to 500kHz. The circuit comprises a voltage-controlled oscillator of exceptional stability and linearity, a phase comparator, an amplifier and a low pass filter as shown in the Block Diagram. The center frequency of the PLL is determined by the free-running frequency of the VCO; this frequency can be adjusted externally with a resistor or a capacitor. The low pass filter, which determines the capture characteristics of the loop, is formed by an internal resistor and an external capacitor.

FEATURES

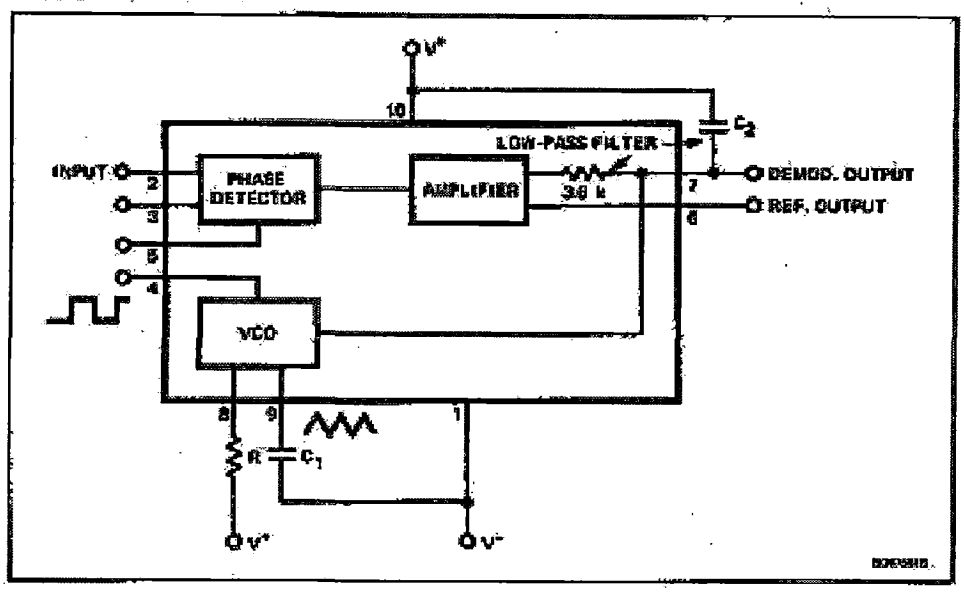
- Highly stable center frequency (200ppm/°C typ.)
- Wide operating voltage range (±6V to ±12V)
- Highly linear demodulated output (0.2% typ.)
- Center frequency programming by means of a resistor or capacitor, voltage or current
- TTL and DTL compatible square wave output; loop can be opened to insert digital frequency divider
- Highly linear triangle wave output
- Reference output for connection of comparator in frequency discriminator
- Bandwidth adjustable from <±1% to >±60%
- Frequency adjustable over 10 to 1 range with same capacitor

PIN CONFIGURATIONS



NOTE:
1. SO and non-standard pin out.

BLOCK DIAGRAM

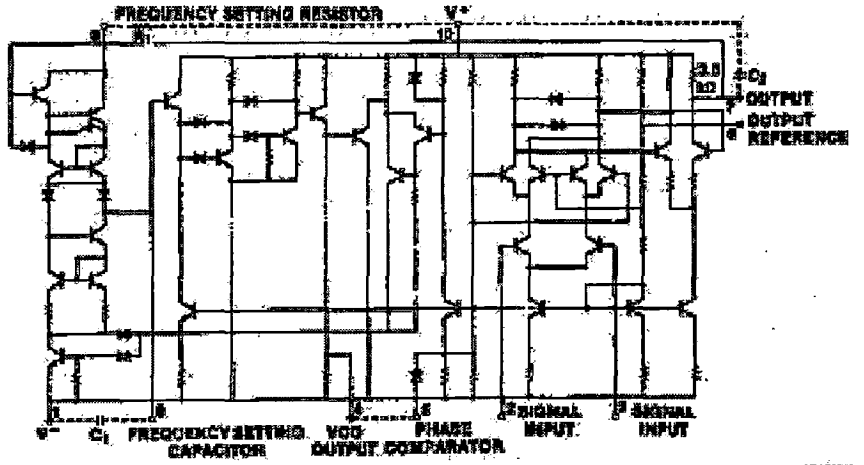


APPLICATIONS

- Frequency shift keying
- Modems
- Telemetry receivers
- Tone decoders
- SCA receivers
- Wide-band FM discriminators
- Data synchronizers
- Tracking filters
- Signal restoration
- Frequency multiplication & division

Phase-Locked Loop NE/SE565

EQUIVALENT SCHEMATIC



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic SO	0 to +70°C	NE565D
14-Pin Cerdip	0 to +70°C	NE565F
14-Pin Plastic DIP	0 to +70°C	NE565N
14-Pin Cerdip	−55°C to +125°C	SE565F
14-Pin Plastic DIP	−55°C to +125°C	SE565N

ABSOLUTE MAXIMUM RATINGS T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V+	Maximum operating voltage	26	V
V_{IN}	Input voltage	3	V_{P-P}
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range NE565 SE565	 0 to +70 −55 to +125	 °C °C
P_D	Power dissipation	300	mW

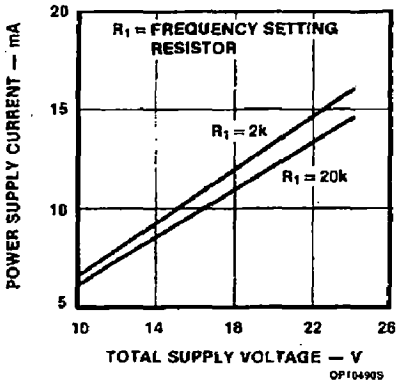
DC AND AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = \pm 6V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE565			NE565			UNIT
			Min	Typ	Max	Min	Typ	Max	
Supply requirements									
V_{CC}	Supply voltage		±6		±12	±6		±12	V
I_{CC}	Supply current			8	12.5		8	12.5	mA
Input characteristics									
	Input impedance[1]		7	10		5	10		kΩ
	Input level required for tracking	f_O = 50kHz, ±10% frequency deviation	10			10			mV_{RMS}
VCO characteristics									
f_C	Center frequency Maximum value distribution[2]	Distribution taken about f_O = 50kHz, R_1 = 5.0kΩ, C_1 = 1200pF	300 −10	500 0	 +10	 −30	500 0	 +30	kHz %
	Drift with temperature Drift with supply voltage	f_O = 50kHz f_O = 50kHz, V_{CC} = ±6 to ±7V		500 0.1	 1.0		600 0.2	 1.5	ppm/°C %/V
	Triangle wave output voltage level linearity		1.9	2.4 0.2	3	1.9	2.4 0.5	3	V_{P-P} %
	Square wave logical "1" output voltage logical "0" output voltage	 f_O = 50kHz f_O = 50kHz	 +4.9	 +5.2 −0.2	 +0.2	 +4.9	 +5.2 −0.2	 +0.2	 V V
	Duty cycle	f_O = 50kHz	45	50	55	40	50	60	%
t_R	Rise time			20	100		20		ns
t_F	Fall time			50	200		50		ns
I_{SINK}	Output current (sink)		0.6	1		0.6	1		mA
I_{SOURCE}	Output current (source)		5	10		5	10		mA
Demodulated output characteristics									
V_{OUT}	Output voltage level	Measured at Pin 7	4.25	4.5	4.75	4.0	4.5	5.0	V
	Maximum voltage swing[3]			2			2		V_{P-P}
	Output voltage swing	±10% frequency deviation	250	300		200	300		mV_{P-P}
THD	Total harmonic distortion			0.2	0.75		0.4	1.5	%
	Output impedance[4]			3.6			3.6		kΩ
V_{OS}	Offset voltage (V6 − V7)			30	100		50	200	mV
	Offset voltage vs temperature (drift)			50			100		µV/°C
	AM rejection		30	40			40		dB

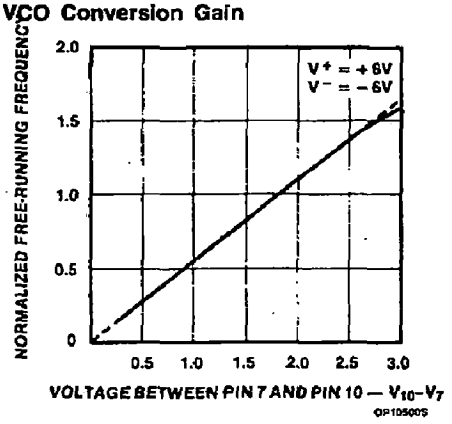
NOTES:
1. Both input terminals (Pins 2 and 3) must receive identical DC bias. This bias may range from 0V to −4V.
2. The external resistance for frequency adjustment (R_1) must have a value between 2kΩ and 20kΩ.
3. Output voltage swings negative as input frequency increases.
4. Output not buffered.

TYPICAL PERFORMANCE CHARACTERISTICS

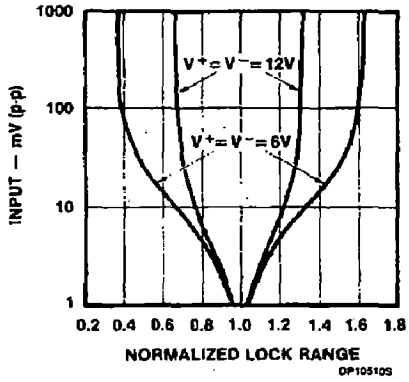
Power Supply Current as a Function of Supply Voltage



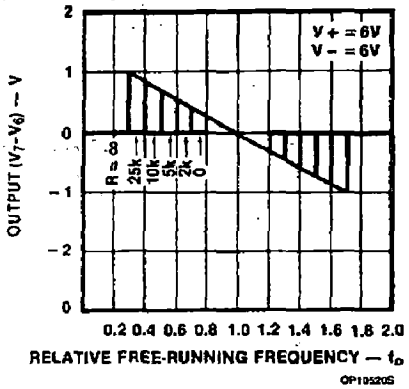
VCO Conversion Gain



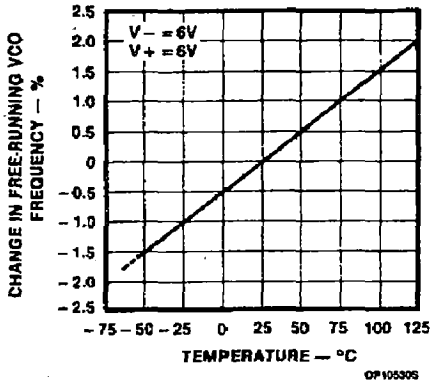
Lock Range as a Function of Input Voltage



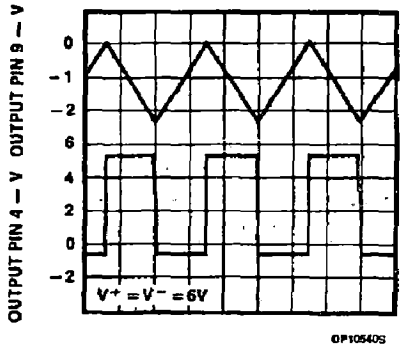
Lock Range as a Function of Gain Setting Resistance (Pins 6 – 7)



Change in Free-Running VCO Frequency as a Function of Temperature



VCO Output Waveform



DESIGN FORMULAS (See Figure 1)

Free-running frequency of VCO:

$$f_O \simeq \frac{1.2}{4R_1C_1} \text{ in Hz}$$

Lock range: $f_L = \pm \frac{8f_O}{V_{CC}}$ in Hz

Capture range: $f_C \simeq \pm \frac{1}{2\pi}\sqrt{\frac{2\pi f_L}{\tau}}$

where $\tau = (3.6 \times 10^3) \times C_2$

TYPICAL APPLICATIONS

FM Demodulation

The 565 Phase-Locked Loop is a general purpose circuit designed for highly linear FM demodulation. During lock, the average DC level of the phase comparator output signal is directly proportional to the frequency of the input signal. As the input frequency shifts, it is this output signal which causes the VCO to shift its frequency to match that of the input. Consequently, the linearity of the phase comparator output with frequency is determined by the voltage-to-frequency transfer function of the VCO.

Because of its unique and highly linear VCO, the 565 PLL can lock to and track an input signal over a very wide bandwidth (typically ±60%) with very high linearity (typically, within 0.5%).

A typical connection diagram is shown in Figure 1. The VCO free-running frequency is given approximately by

$$f_O \simeq \frac{1.2}{4R_1C_1}$$

and should be adjusted to be at the center of the input signal frequency range. C_1 can be any value, but R_1 should be within the range of 2000 to 20,000Ω with an optimum value on the order of 4000Ω. The source can be direct coupled if the DC resistances seen from Pins 2 and 3 are equal and there is no DC voltage difference between the pins. A short between Pins 4 and 5 connects the VCO to the phase comparator. Pin 6 provides a DC reference voltage that is close to the DC potential of the demodulated output (Pin 7). Thus, if a resistance is connected between Pins 6 and 7, the gain of the output stage can be reduced with little change in the DC voltage level at the output. This allows the lock range to be decreased with little change in the free-running frequency. In this manner the lock range can be decreased from ±60% of f_O to approximately ±20% of f_O (at ±6V).

A small capacitor (typically 0.001μF) should be connected between Pins 7 and 8 to eliminate possible oscillation in the control current source.

A single-pole loop filter is formed by the capacitor C2, connected between Pin 7 and the positive supply, and an internal resistance of approximately 3600Ω.

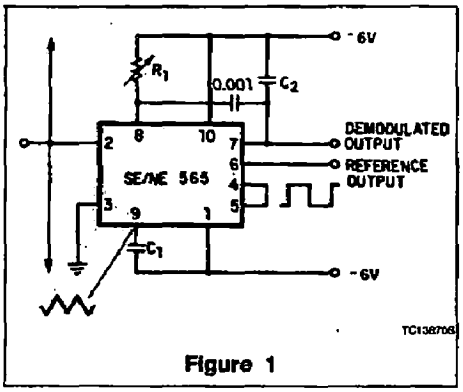


Figure 1

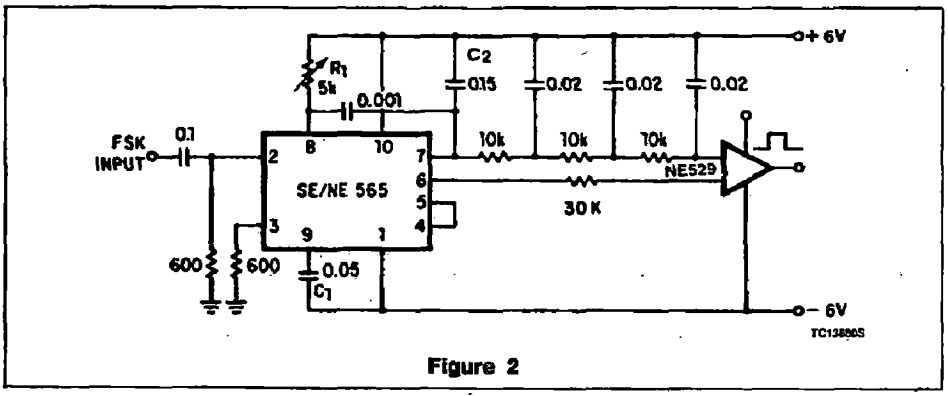


Figure 2

Frequency Shift Keying (FSK)

FSK refers to data transmission by means of a carrier which is shifted between two preset frequencies. This frequency shift is usually accomplished by driving a VCO with the binary data signal so that the two resulting frequencies correspond to the "0" to "1" states (commonly called space and mark) of the binary data signal.

A simple scheme using the 565 to receive FSK signals of 1070Hz and 1270Hz is shown in Figure 2. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding DC shift at the output.

The loop filter capacitor C_2 is chosen smaller than usual to eliminate overshoot on the output pulse, and a three-stage RC ladder filter is used to remove the carrier component from the output. The band edge of the ladder filter is chosen to be approximately half way between the maximum keying rate (in this case 300 baud or 150Hz) and twice the input frequency (approximately 2200Hz). The output signal can now be made logic compatible by connecting a voltage comparator between the output and Pin 6 of the loop. The free-running frequency is adjusted with R_1 so as to result in a slightly-positive voltage at the output with f_{IN} = 1070Hz.

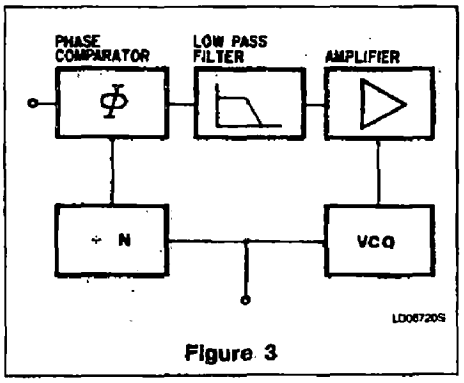


Figure 3

The input connection is typical for cases where a DC voltage is present at the source and therefore a direct connection is not desirable. Both input terminals are returned to ground with identical resistors (in this case, the values are chosen to effect at 600Ω input impedance).

Frequency Multiplication

There are two methods by which frequency multiplication can be achieved using the 565:

1. Locking to a harmonic of the input signal.
2. Inclusion of a digital frequency divider or counter in the loop between the VCO and phase comparator.

The first method is the simplest, and can be achieved by setting the free-running frequency of the VCO to a multiple of the input frequency. A limitation of this scheme is that the lock range decreases as successively higher and weaker harmonics are used for locking. If the input frequency is to be constant with little tracking required, the loop can generally be locked to any one of the first 5 harmonics. For higher orders of multiplication, or for cases where a large lock range is desired, the second scheme is more desirable. An example of this might be a case where the input signal varies over a wide frequency range and a large multiple of the input frequency is required.

A block diagram of the second scheme is shown in Figure 3. Here the loop is broken between the VCO and the phase comparator, and a frequency divider is inserted. The fundamental of the divided VCO frequency is locked to the input frequency in this case, so that the VCO is actually running at a multiple of the input frequency. The amount of multiplication is determined by the frequency divider. A typical connection scheme is shown in Figure 4. To set up the circuit, the frequency limits of the input signal must be determined. The free-running frequency of the VCO is then adjusted by means of R_1 and C_1 (as discussed under FM demodulation) so that the output frequency of the divider is midway between the input frequency limits. The filter capacitor, C_2, should be large enough to eliminate variations in the demodulated output voltage (at Pin 7), in order to stabilize the VCO frequency. The output can now be taken as the VCO squarewave output, and its fundamental will be the desired multiple of the input frequency (f_{IN}) as long as the loop is in lock.

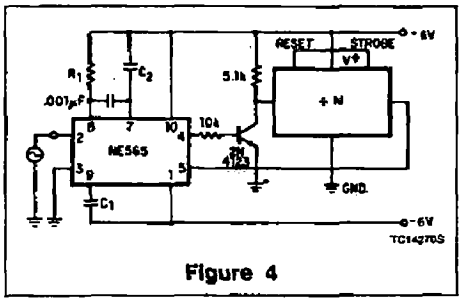


Figure 4

SCA (Background Music) Decoder

Some FM stations are authorized by the FCC to broadcast uninterrupted background music for commercial use. To do this, a frequency modulated subcarrier of 67kHz is used. The frequency is chosen so as not to interfere with the normal stereo or monaural program; in addition, the level of the subcarrier is only 10% of the amplitude of the combined signal.

The SCA signal can be filtered out and demodulated with the NE565 Phase-Locked Loop without the use of any resonant circuits. A connection diagram is shown in Figure 5. This circuit also serves as an example of operation from a single power supply.

A resistive voltage divider is used to establish a bias voltage for the input (Pins 2 and 3). The demodulated (multiplex) FM signal is fed to the input through a two-stage high-pass filter, both to effect capacitive coupling and to attenuate the strong signal of the regular channel. A total signal amplitude, between 80mV and 300mV, is required at the input. Its source should have an impedance of less than 10,000Ω.

Phase-Locked Loop

NE/SE565

The Phase-Locked Loop is tuned to 67kHz with a 5000Ω potentiometer; only approximate tuning is required, since the loop will seek the signal.

The demodulated output (Pin 7) passes through a three-stage low pass filter to provide de-emphasis and attenuate the high-frequency noise which often accompanies SCA transmission. Note that no capacitor is provided directly at Pin 7; thus, the circuit is operating as a first-order loop. The demodulated output signal is in the order of 50mV and the frequency response extends to 7kHz.

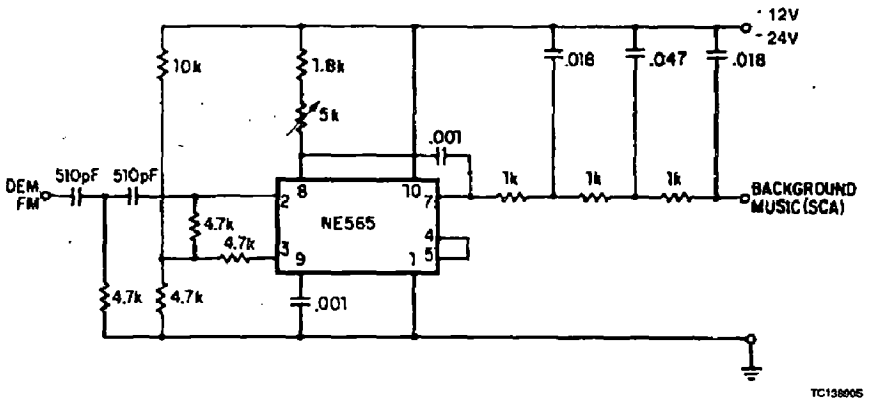
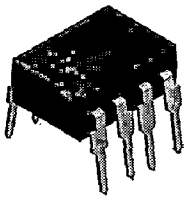


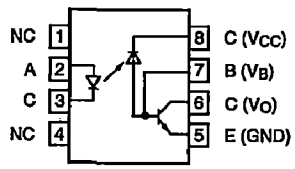
Figure 5

High Speed Optocoupler, 1 MBd, Photodiode with Transistor Output

Features

- Isolation Test Voltage: 5300 V_{RMS}
- TTL Compatible
- High Bit Rates: 1.0 Mbit/s
- High Common-Mode Interference Immunity
- Bandwidth 2.0 MHz
- Open-Collector Output
- External Base Wiring Possible
- Lead-free component
- Component in accordance to RoHS 2002/95/EC and WEEE 2002/96/EC





Agency Approvals

- UL1577, File No. E52744 System Code H or J, Double Protection
- DIN EN 60747-5-2 (VDE0884)
  DIN EN 60747-5-5 pending
  Available with Option 1
- CSA 93751

Description

The 6N135 and 6N136 are optocouplers with a GaAlAs infrared emitting diode, optically coupled with an integrated photo detector which consists of a photo diode and a high-speed transistor in a DIP-8 plastic package.

Signals can be transmitted between two electrically separated circuits up to frequencies of 2.0 MHz. The potential difference between the circuits to be coupled should not exceed the maximum permissible reference voltages

Order Information

Part	Remarks
6N135	CTR ≥ 7 %, DIP-8
6N136	CTR ≥ 19 %, DIP-8
6N135-X007	CTR ≥ 7 %, SMD-8 (option 7)
6N136-X006	CTR ≥ 19 %, DIP-8 400 mil (option 6)
6N136-X007	CTR ≥ 19 %, SMD-8 (option 7)
6N136-X009	CTR ≥ 19 %, SMD-8 (option 9)

For additional information on the available options refer to Option Information.

Absolute Maximum Ratings

T_{amb} = 25 °C, unless otherwise specified

Stresses in excess of the absolute Maximum Ratings can cause permanent damage to the device. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this document. Exposure to absolute Maximum Rating for extended periods of the time can adversely affect reliability.

Input

Parameter	Test condition	Symbol	Value	Unit
Reverse voltages		V_R	5.0	V
Forward current		I_F	25	mA
Peak forward current	t = 1.0 ms, duty cycle 50 %	I_{FSM}	50	mA
Maximum surge forward current	t ≤ 1.0 µs, 300 pulses/s		1.0	A
Thermal resistance		R_{th}	700	K/W
Power dissipation	T_{amb} = 70 °C	P_{diss}	45	mW

Output

Parameter	Test condition	Symbol	Value	Unit
Supply voltage		V_S	- 0.5 to 15	V
Output voltage		V_O	- 0.5 to 15	V
Emitter-base voltage		V_{EBO}	5.0	V
Output current		I_O	8.0	mA
Maximum output current			16	mA
Base current		I_B	5.0	mA
Thermal resistance			300	K/W
Power dissipation	T_{amb} = 70 °C	P_{diss}	100	mW

Coupler

Parameter	Test condition	Symbol	Value	Unit
Isolation test voltage (between emitter and detector climate per DIN 50014 part 2, NOV 74	t = 1.0 s	V_{ISO}	5300	V_{RMS}
Pollution degree (DIN VDE 0109)			2.0	
Creepage			≥ 7.0	mm
Clearance			≥ 7.0	mm
Comparative tracking index per DIN IEC112/VDE 0303 part 1, group IIIa per DIN VDE 6110			175	
Isolation resistance	V_{IO} = 500 V, T_{amb} = 25 °C	R_{IO}	≥ 10^{12}	Ω
	V_{IO} = 500 V, T_{amb} = 100 °C	R_{IO}	≥ 10^{11}	Ω
Storage temperature range		T_{stg}	- 55 to + 125	°C
Ambient temperature range		T_{amb}	- 55 to + 100	°C
Soldering temperature	max. ≤ 10 s, dip soldering ≥ 0.5 mm from case bottom	T_{sld}	260	°C

Electrical Characteristics

T_{amb} = 25 °C, unless otherwise specified
Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluation. Typical values are for information only and are not part of the testing requirements.

Input

Parameter	Test condition	Symbol	Min	Typ.	Max	Unit
Forward voltage	I_F = 16 mA	V_F		1.6	1.9	V
Breakdown voltage	I_R = 10 µA	V_{BR}	5.0			V
Reverse current	V_R = 5.0 V	I_R		0.5	10	µA
Capacitance	V_R = 0 V, f = 1.0 MHz	C_O		125		pF
Temperature coefficient, forward voltage	I_F = 16 mA	$\Delta V_F/\Delta T_A$		-1.7		mV/°C

Output

Parameter	Test condition	Part	Symbol	Min	Typ.	Max	Unit
Logic low supply current	I_F = 16 mA, V_O open, V_{CC} = 15 V		I_{CCL}		150		µA
Supply current, logic high	I_F = 0 mA, V_O open, V_{CC} = 15 V		I_{CCH}		0.01	1	µA
Output voltage, output low	I_F = 16 mA, V_{CC} = 4.5 V, I_O = 1.1 mA	6N135	V_{OL}		0.1	0.4	V
	I_F = 16 mA, V_{CC} = 4.5 V, I_O = 2.4 mA	6N136	V_{OL}		0.1	0.4	V
Output current, output high	I_F = 0 mA, V_O = V_{CC} = 5.5 V		I_{OH}		3.0	500	nA
	I_F = 0 mA, V_O = V_{CC} = 15 V		I_{OH}		0.01	1	µA

Coupler

Parameter	Test condition	Symbol	Min	Typ.	Max	Unit
Capacitance (input-output)	f = 1.0 MHz	C_{IO}		0.6		pF

Current Transfer Ratio

Parameter	Test condition	Part	Symbol	Min	Typ.	Max	Unit
Current Transfer Ratio	I_F = 16 mA, V_O = 0.4 V, V_{CC} = 4.5 V	6N135	CTR	7	16		%
		6N136	CTR	19	35		%
	I_F = 16 mA, V_O = 0.5 V, V_{CC} = 4.5 V	6N135	CTR	5			%
		6N136	CTR	15			%

Switching Characteristics

Parameter	Test condition	Part	Symbol	Min	Typ.	Max	Unit
High-low	I_F = 16 mA, V_{CC} = 5.0 V, R_L = 4.1 kΩ	6N135	t_{PHL}		0.3	1.5	µs
	I_F = 16 mA, V_{CC} = 5.0 V, R_L = 1.9 kΩ	6N136	t_{PHL}		0.2	0.8	µs
Low-high	I_F = 16 mA, V_{CC} = 5.0 V, R_L = 4.1 kΩ	6N135	t_{PLH}		0.3	1.5	µs
	I_F = 16 mA, V_{CC} = 5.0 V, R_L = 1.9 kΩ	6N136	t_{PLH}		0.2	0.8	µs

Common Mode Transient Immunity

Parameter	Test condition	Part	Symbol	Min	Typ.	Max	Unit
High	I_F = 0 mA, V_{CM} = 10 V_{P-P}, V_{CC} = 5.0 V, R_L = 4.1 kΩ	6N135	$\lvert CM_H \rvert$		1000		V/µs
	I_F = 0 mA, V_{CM} = 10 V_{P-P}, V_{CC} = 5.0 V, R_L = 1.9 kΩ	6N136	$\lvert CM_H \rvert$		1000		V/µs
Low	I_F = 16 mA, V_{CM} = 10 V_{P-P}, V_{CC} = 5.0 V, R_L = 4.1 kΩ	6N135	$\lvert CM_L \rvert$		1000		V/µs
	I_F = 16 mA, V_{CM} = 10 V_{P-P}, V_{CC} = 5.0 V, R_L = 1.9 kΩ	6N136	$\lvert CM_L \rvert$		1000		V/µs

Typical Characteristics (Tamb = 25 °C unless otherwise specified)

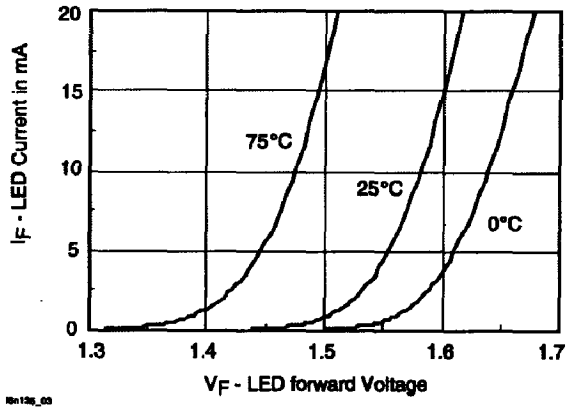


Figure 1. LED Forward Current vs.Forward Voltage

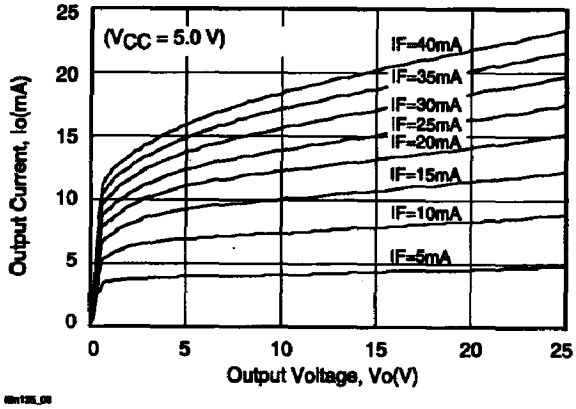


Figure 4. Output Current vs. Output Voltage

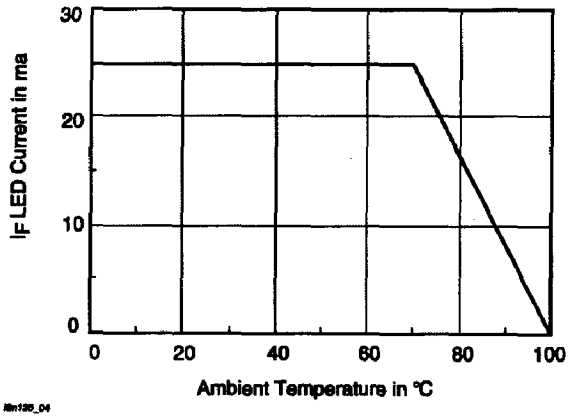


Figure 2. Permissible Forward LED Current vs. Temperature

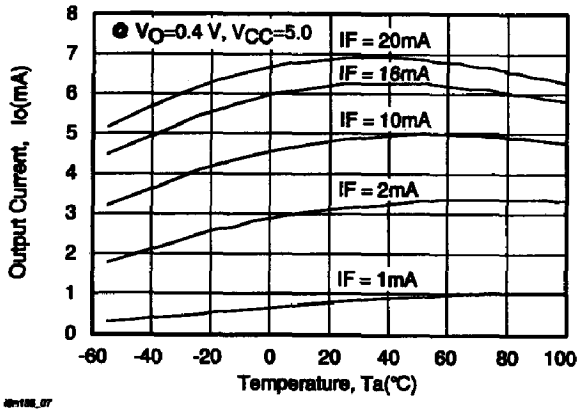


Figure 5. Output Current vs. Temperature

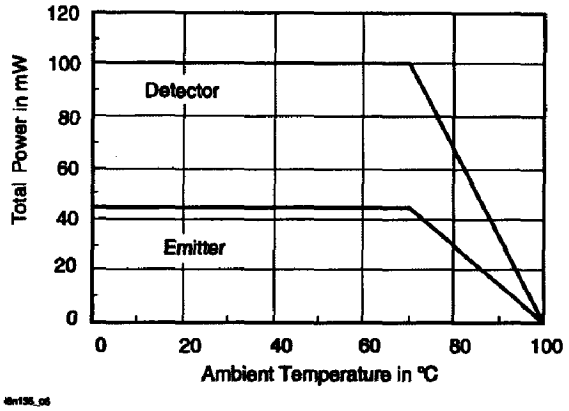


Figure 3. Permissible Power Dissipation vs. Temperature

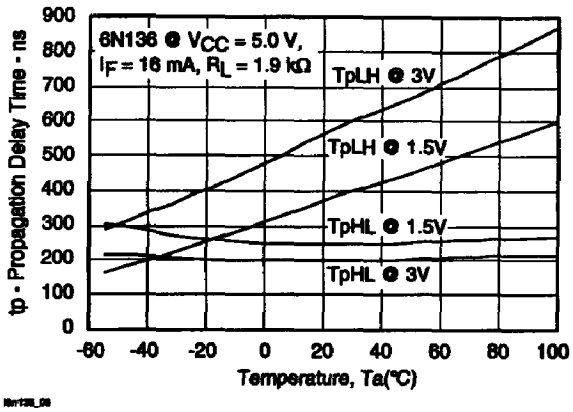


Figure 6. Propagation Delay vs. Ambient Temperature

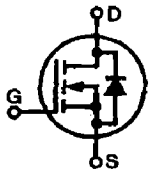
IXYS

MegaMOS™ Power MOSFET

IRFP460

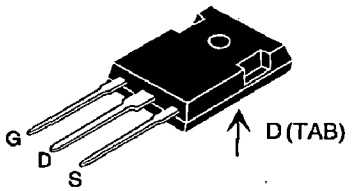
V_{DSS} = 500 V
$I_{D(cont)}$ = 20 A
$R_{DS(on)}$ = 0.27Ω

N-Channel Enhancement Mode, HDMOS™ Family



Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	500	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 MΩ	500	V
V_{GS}	Continuous	±20	V
V_{GSM}	Transient	±30	V
I_{D25}	T_C = 25°C	20	A
I_{DM}	T_C = 25°C, pulse width limited by T_{JM}	80	A
I_{AR}		20	A
E_{AR}	T_C = 25°C	28	mJ
dv/dt	$I_S \le I_{DM}$, di/dt ≤ 100 A/µs, $V_{DD} \le V_{DSS}$, $T_J \le 150°C$, R_G = 2 Ω	3.5	V/ns
P_D	T_C = 25°C	260	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
M_d	Mounting torque	1.15/10	Nm/lb.in.
Weight		6	g
Maximum lead temperature for soldering 1.6 mm (0.062 in.) from case for 10 s		300	°C

TO-247 AD



G = Gate, D = Drain,
S = Source, TAB = Drain

Features

- Repetitive avalanche energy rated
- Fast switching times
- Low $R_{DS(on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- High Commutating dv/dt Rating

Applications

- Switching Power Supplies
- Motor controls

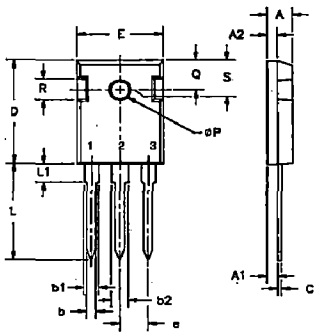
Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
V_{DSS}	V_{GS} = 0 V, I_D = 250 µA	500			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	2		4	V
I_{GSS}	V_{GS} = ±20 V_{DC}, V_{DS} = 0			±100	nA
I_{DSS}	$V_{DS} = 0.8 \cdot V_{DSS}$, V_{GS} = 0 V; T_J = 25°C			25	µA
	T_J = 125°C			250	µA
$R_{DS(on)}$	V_{GS} = 10 V, I_D = 12 A; Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %		0.25	0.27	Ω

Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
g_{fs}	V_{DS} = 10 V; I_D = 12 A, pulse test	13	21		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		4200		pF
C_{oss}			450		pF
C_{rss}			135		pF
$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 250 V, I_D = 20 A R_G = 4.3 Ω, (External)		23	35	ns
t_r			81	120	ns
$t_{d(off)}$			85	130	ns
t_f			65	98	ns
$Q_{g(on)}$	V_{GS} = 10 V, V_{DS} = 200 V, I_D = 20 A		135	210	nC
Q_{gs}			28	40	nC
Q_{gd}			62	110	nC
R_{thJC}				0.45	K/W
R_{thCK}			0.25		K/W

Source-Drain Diode

Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
I_S	V_{GS} = 0 V			20	A
I_{SM}	Repetitive; pulse width limited by T_{JM}			80	A
V_{SD}	I_F = 20 A, V_{GS} = 0 V, Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %			1.8	V
t_{rr}	I_F = 20 A, -di/dt = 100 A/µs, V_R = 100 V		570	860	ns
Q_{rr}			5.7		µC

TO-247 AD Outline



Terminals: 1 - Gate 2 - Drain
3 - Source Tab - Drain

Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.7	5.3	.185	.209
A_1	2.2	2.54	.087	.102
A_2	2.2	2.6	.059	.098
b	1.0	1.4	.040	.055
b_1	1.65	2.13	.065	.084
b_2	2.87	3.12	.113	.123
C	.4	.8	.016	.031
D	20.80	21.46	.819	.845
E	15.75	16.26	.610	.640
e	5.20	5.72	0.205	0.225
L	19.81	20.32	.780	.800
L1		4.50		.177
ØP	3.55	3.65	.140	.144
Q	5.89	6.40	0.232	0.252
R	4.32	5.49	.170	.216
S	6.15 BSC		242 BSC	

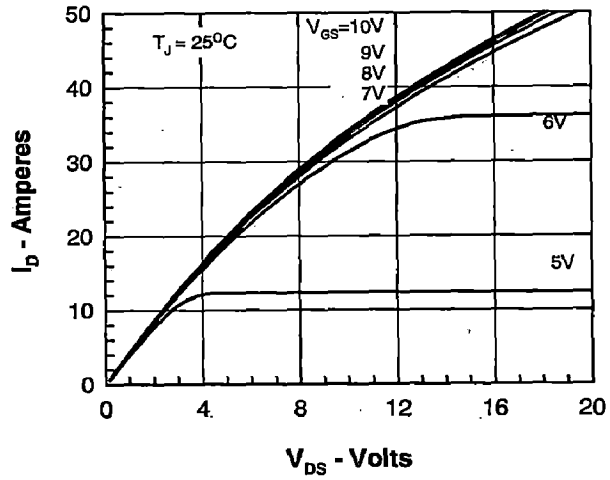


Figure 1. Output Characteristics at 25°C

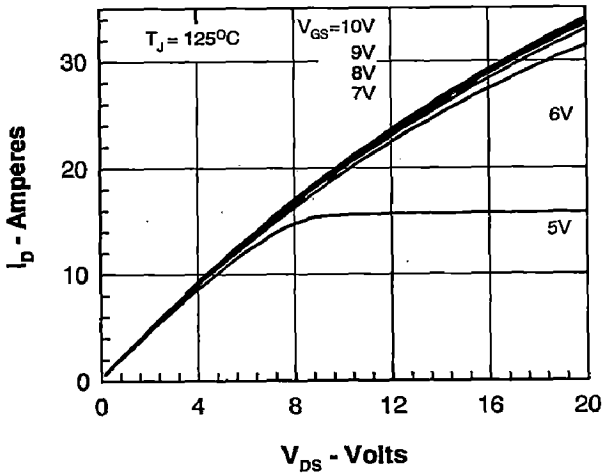


Figure 2. Output Characteristics at 125°C

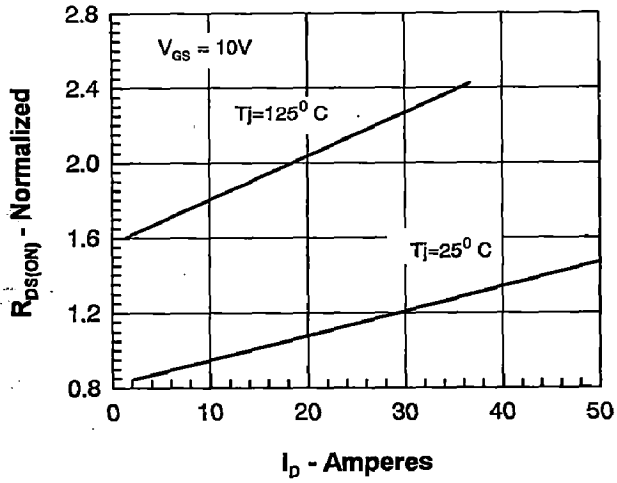


Figure 3. $R_{DS(on)}$ normalized to value at I_D = 12A

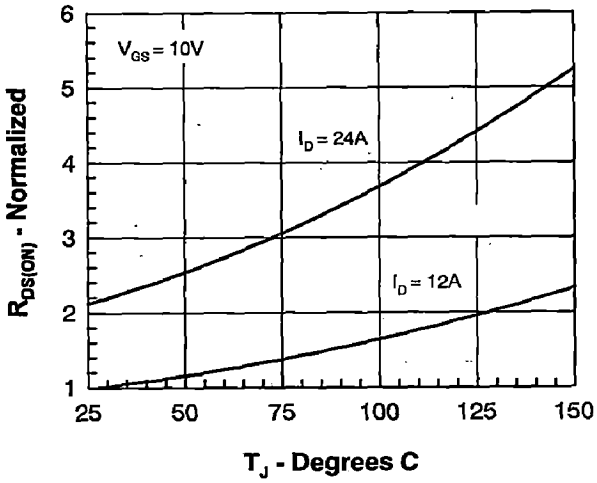


Figure 4. $R_{DS(on)}$ normalized to value at I_D = 12A

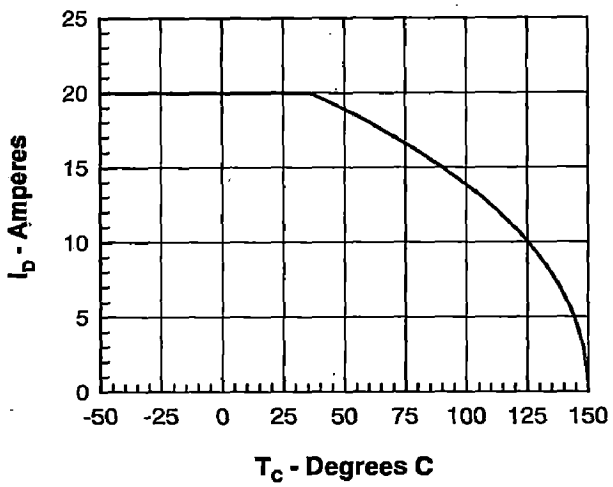


Figure 5. Drain Current vs. Case Temperature

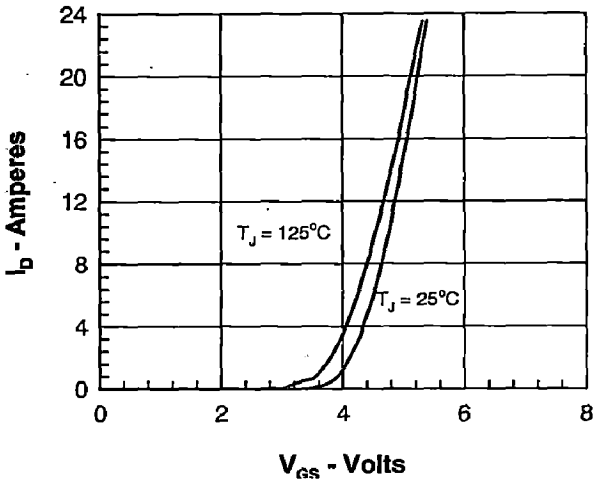
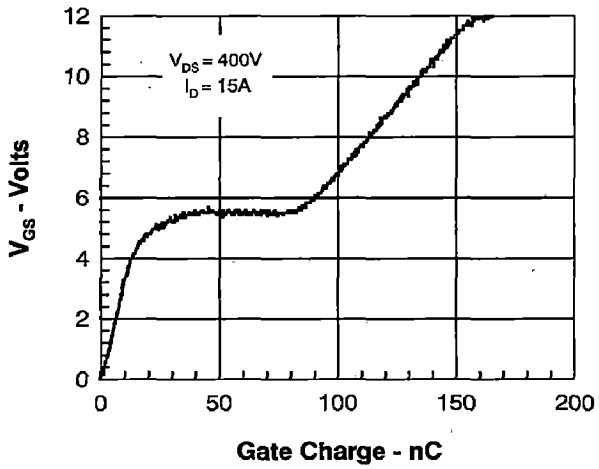
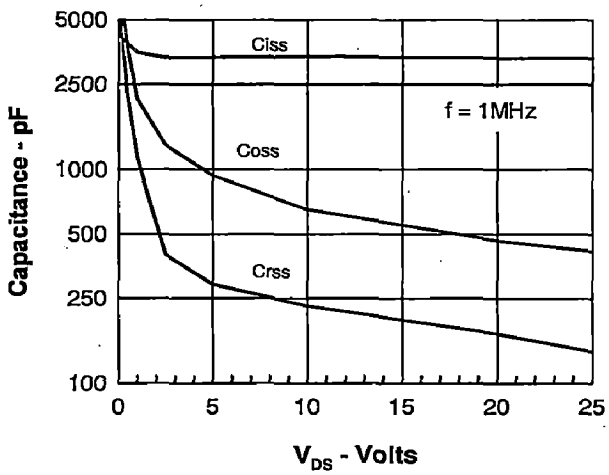
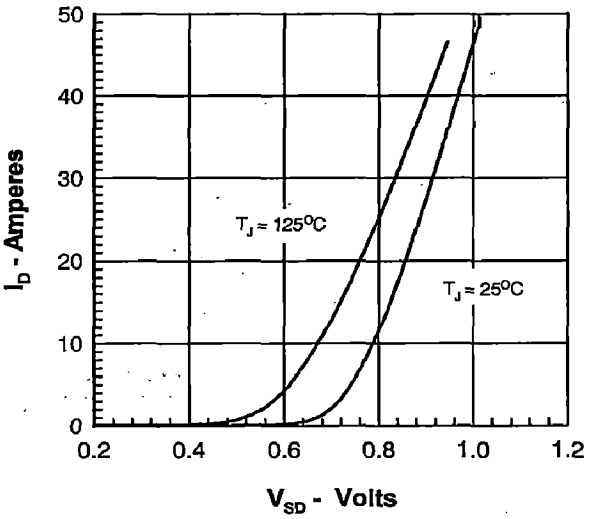
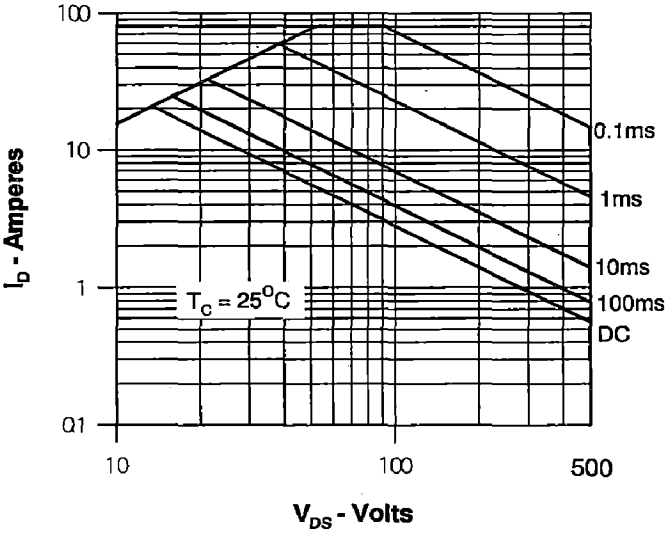


Figure 6. Admittance Curves









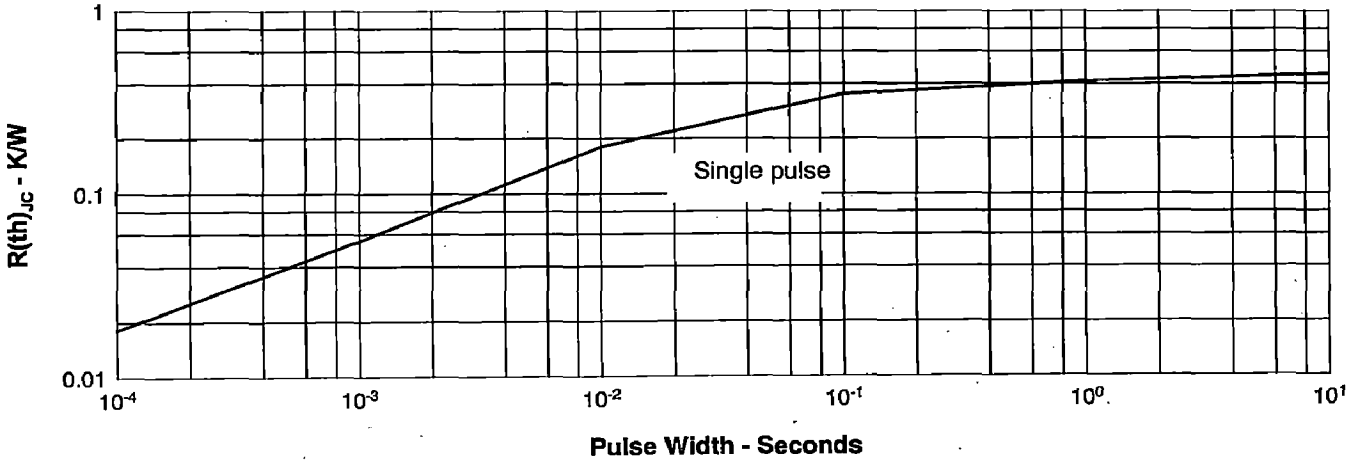


Figure 11. Transient Thermal Resistance

TOSHIBA Insulated Gate Bipolar Transistor
Silicon N Channel IGBT

GT25Q102

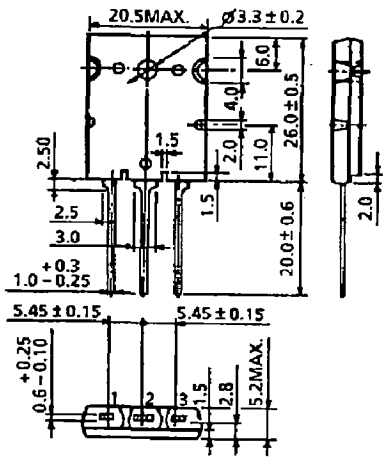
High Power Switching Applications

- The 3rd Generation
- Enhancement-Mode
- High Speed: $t_f = 0.32$ μs (max)
- Low Saturation Voltage: $V_{CE\ (sat)} = 2.7$ V (max)

Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Collector-emitter voltage		V_{CES}	1200	V
Gate-emitter voltage		V_{GES}	±20	V
Collector current	DC	I_C	25	A
	1 ms	I_{CP}	50	
Collector power dissipation (Tc = 25°C)		P_C	200	W
Junction temperature		T_j	150	°C
Storage temperature range		T_{stg}	−55~150	°C

Unit: mm



1. GATE
2. COLLECTOR (HEAT SINK)
3. EMITTER

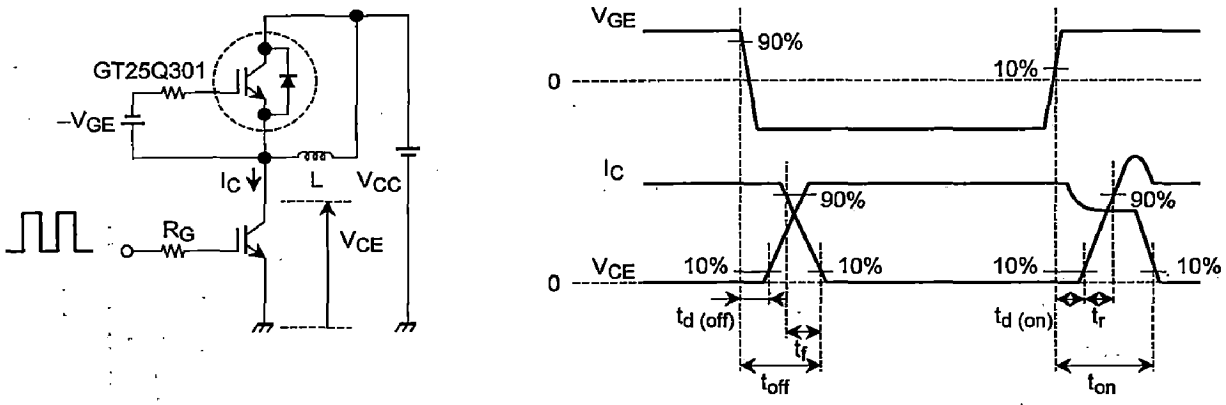
JEDEC	—
JEITA	—
TOSHIBA	2-21F2C

Weight: 9.75 g (typ.)

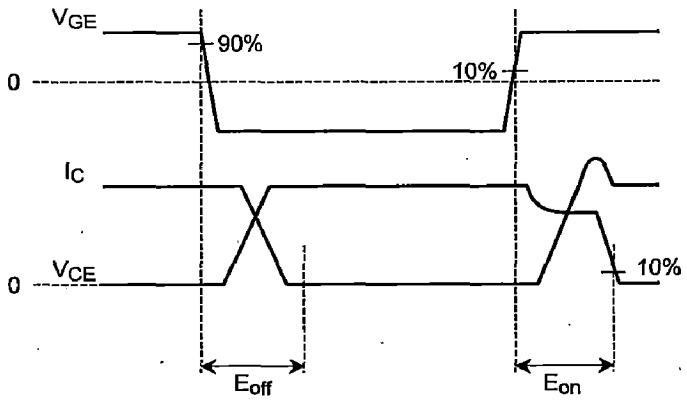
Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GES}	V_{GE} = ±20 V, V_{CE} = 0	—	—	±500	nA
Collector cut-off current		I_{CES}	V_{CE} = 1200 V, V_{GE} = 0	—	—	1.0	mA
Gate-emitter cut-off voltage		$V_{GE\ (OFF)}$	I_C = 2.5 mA, V_{CE} = 5 V	4.0	—	7.0	V
Collector-emitter saturation voltage		$V_{CE\ (sat)}$	I_C = 25 A, V_{GE} = 15 V	—	2.1	2.7	V
Input capacitance		C_{ies}	V_{CE} = 50 V, V_{GE} = 0, f = 1 MHz	—	1360	—	pF
Switching time	Rise time	t_r	Inductive Load	—	0.10	—	µs
	Turn-on time	t_{on}	V_{CC} = 600 V, I_C = 25 A	—	0.30	—	
	Fall time	t_f	V_{GG} = ±15 V, R_G = 43 Ω	—	0.16	0.32	
	Turn-off time	t_{off}	(Note1)	—	0.68	—	
Thermal resistance		$R_{th\ (j\text{-}c)}$	—	—	—	0.625	°C/W

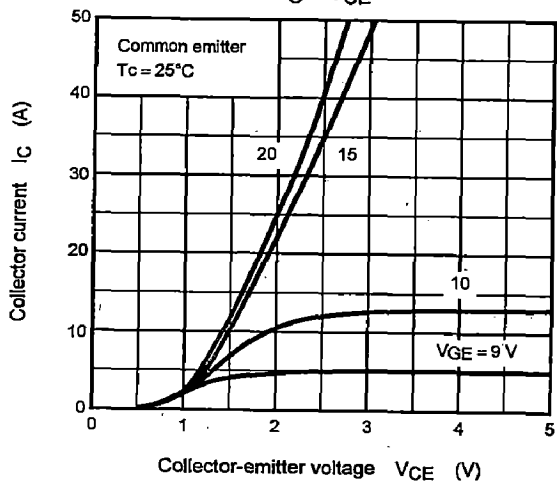
Note1: Switching time measurement circuit and input/output waveforms



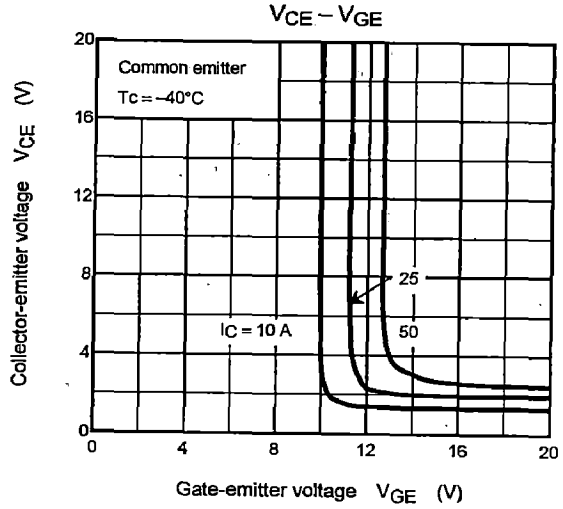
Note2: Switching loss measurement waveforms



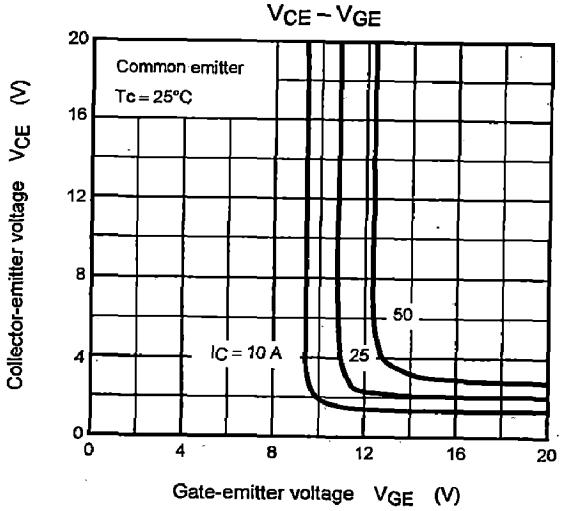
$I_C - V_{CE}$



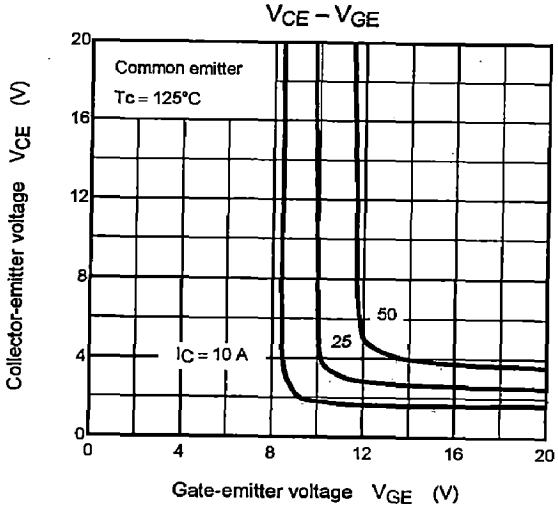
$V_{CE} - V_{GE}$



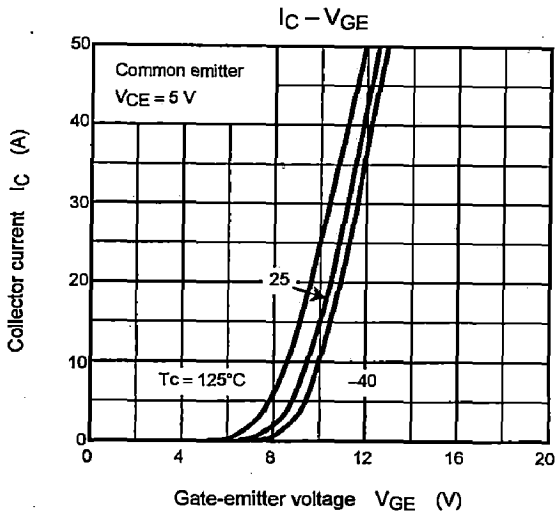
$V_{CE} - V_{GE}$



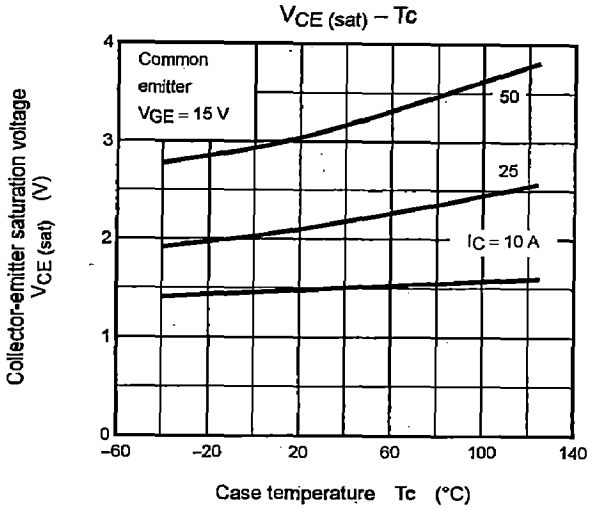
$V_{CE} - V_{GE}$



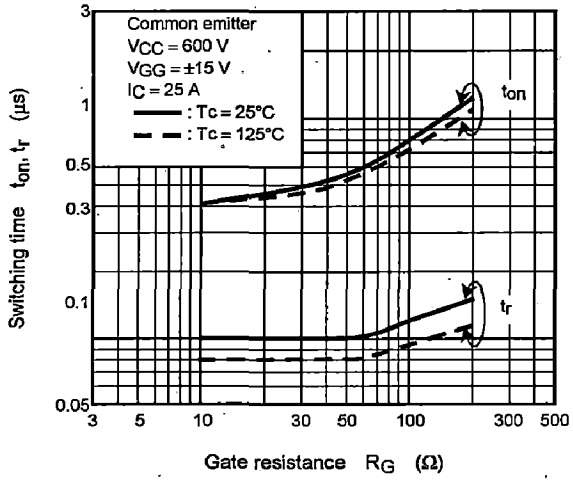
$I_C - V_{GE}$



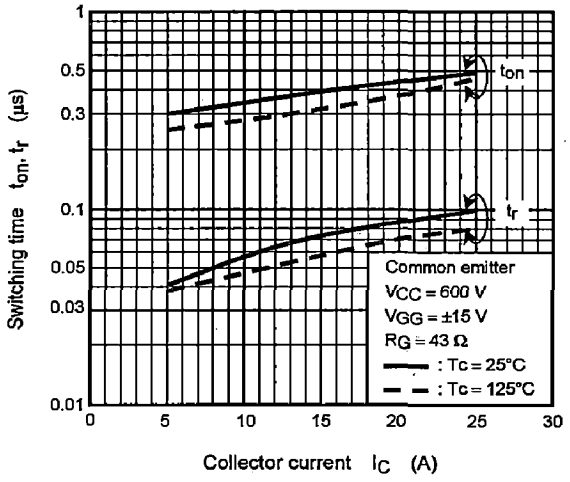
$V_{CE\ (sat)} - Tc$



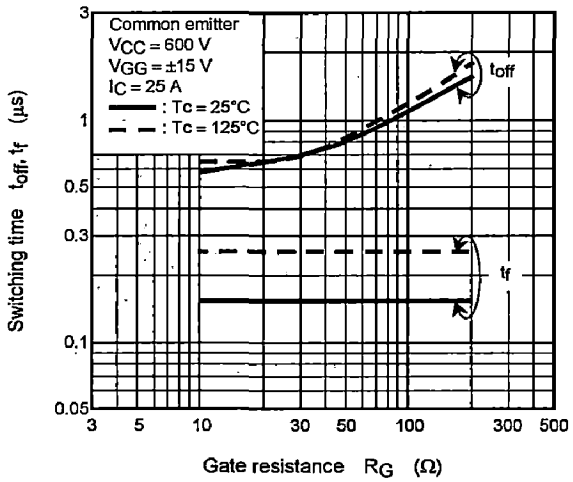
Switching time t_{on}, t_r – R_G



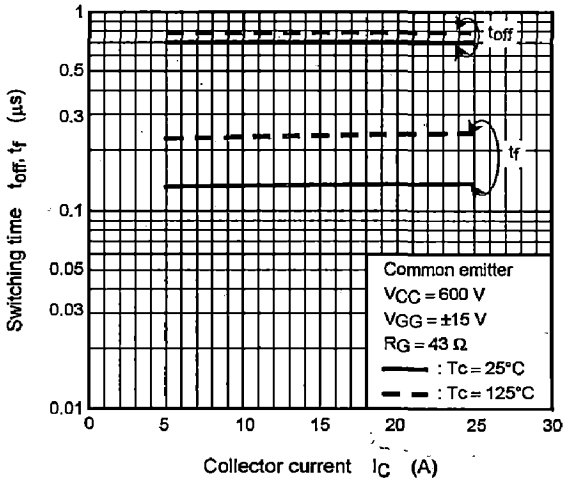
Switching time t_{on}, t_r – I_C



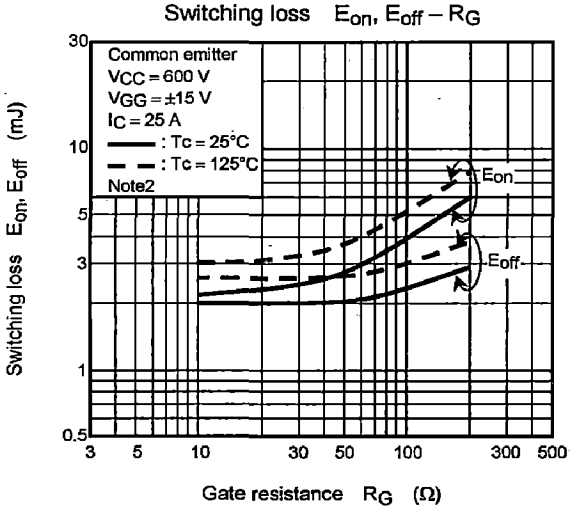
Switching time t_{off}, t_f – R_G



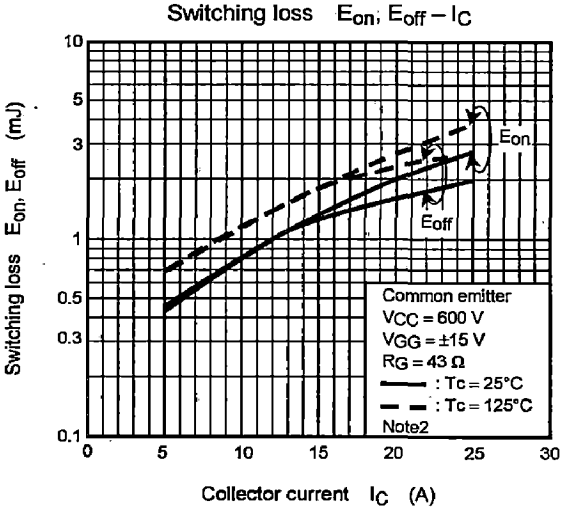
Switching time t_{off}, t_f – I_C



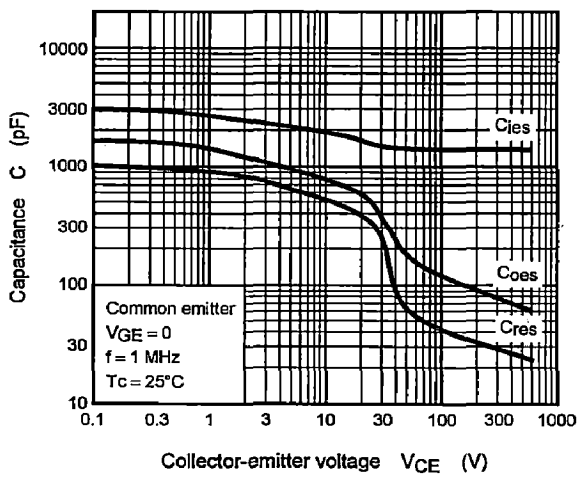
Switching loss E_{on}, E_{off} – R_G



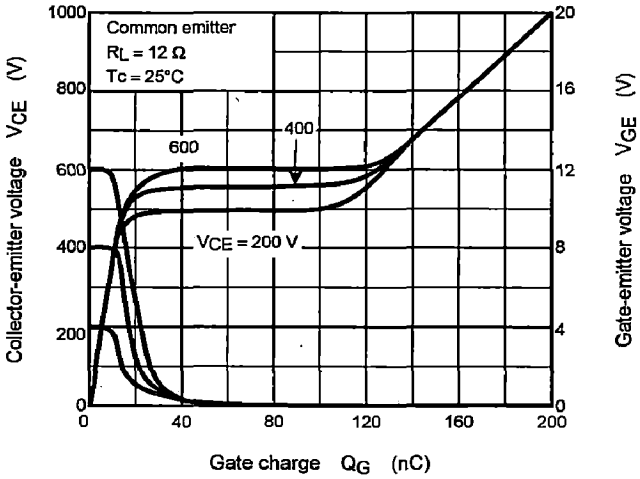
Switching loss E_{on}, E_{off} – I_C



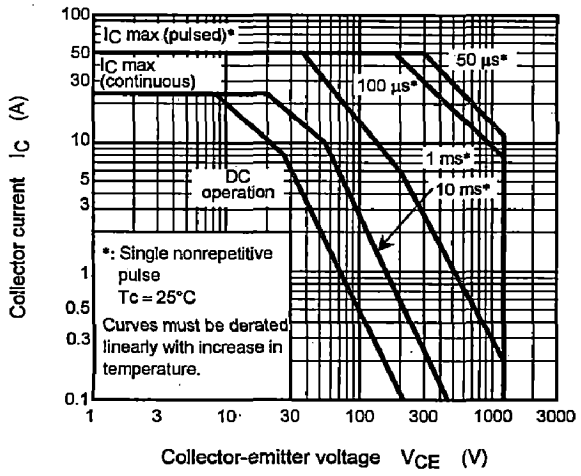
$C - V_{CE}$



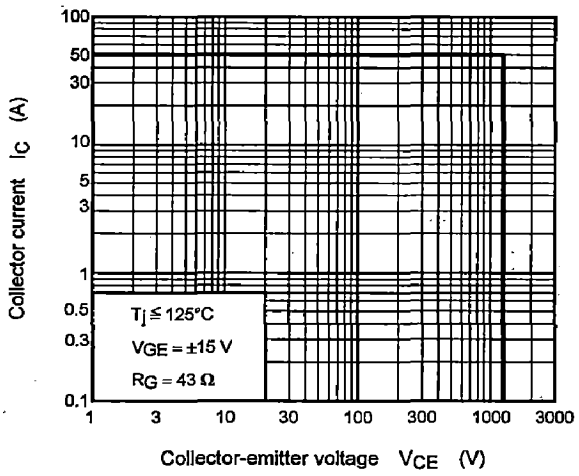
$V_{CE}, V_{GE} - Q_G$



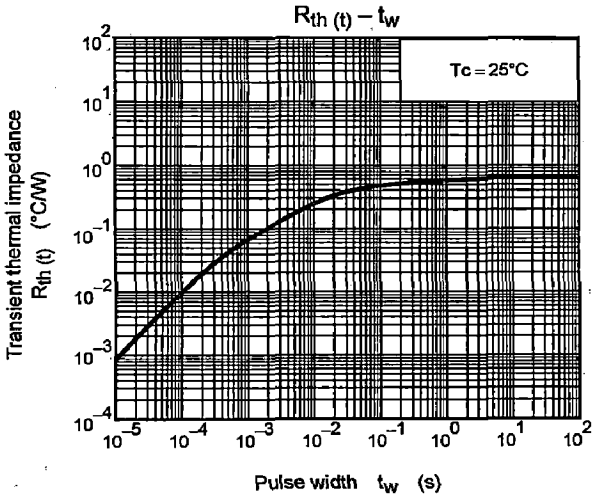
Safe operating area



Reverse bias SOA



$R_{th\,(t)} - t_w$



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ANALOG DEVICES

Low Cost, Miniature Isolation Amplifiers

AD202/AD204

FEATURES

Small Size: 4 Channels/Inch
Low Power: 35 mW (AD204)
High Accuracy: ±0.025% Max Nonlinearity (K Grade)
High CMR: 130 dB (Gain = 100 V/V)
Wide Bandwidth: 5 kHz Full-Power (AD204)
High CMV Isolation: ±2000 V pk Continuous (K Grade) (Signal and Power)
Isolated Power Outputs
Uncommitted Input Amplifier

APPLICATIONS

Multichannel Data Acquisition
Current Shunt Measurements
Motor Controls
Process Signal Isolation
High Voltage Instrumentation Amplifier

GENERAL DESCRIPTION

The AD202 and AD204 are general purpose, two-port, transformer-coupled isolation amplifiers that may be used in a broad range of applications where input signals must be measured, processed, and/or transmitted without a galvanic connection. These industry standard isolation amplifiers offer a complete isolation function, with both signal and power isolation provided for in a single compact plastic SIP or DIP style package. The primary distinction between the AD202 and the AD204 is that the AD202 is powered directly from a 15 V dc supply while the AD204 is powered by an externally supplied clock, such as the recommended AD246 Clock Driver.

The AD202 and AD204 provide total galvanic isolation between the input and output stages of the isolation amplifier through the use of internal transformer-coupling. The functionally complete AD202 and AD204 eliminate the need for an external, user-supplied dc-to-dc converter. This permits the designer to minimize the necessary circuit overhead and consequently reduce the overall design and component costs.

The design of the AD202 and AD204 emphasizes maximum flexibility and ease of use, including the availability of an uncommitted op amp on the input stage. They feature a bipolar ±5 V output range, an adjustable gain range of from 1V/V to 100 V/V, ±0.025% max nonlinearity (K grade), 130 dB of CMR, and the AD204 consumes a low 35 mW of power.

The functional block diagrams can be seen in Figures 1a and 1b.

PRODUCT HIGHLIGHTS

The AD202 and AD204 are full-featured isolators offering numerous benefits to the user:

Small Size: The AD202 and AD204 are available in SIP and DIP form packages. The SIP package is just 0.25" wide, giving the user a channel density of four channels per inch. The isolation barrier is positioned to maximize input to output spacing. For applications requiring a low profile, the DIP package provides a height of just 0.350".

High Accuracy: With a maximum nonlinearity of ±0.025% for the AD202K/AD204K (±0.05% for the AD202J/AD204J) and low drift over temperature, the AD202 and AD204 provide high isolation without loss of signal integrity.

Low Power: Power consumption of 35 mW (AD204) and 75 mW (AD202) over the full signal range makes these isolators ideal for use in applications with large channel counts or tight power budgets.

Wide Bandwidth: The AD204's full-power bandwidth of 5 kHz makes it useful for wideband signals. It is also effective in applications like control loops, where limited bandwidth could result in instability.

Excellent Common-Mode Performance: The AD202K/AD204K provide ±2000 V pk continuous common-mode isolation, while the AD202J/AD204J provide ±1000 V pk continuous common-mode isolation. All models have a total common-mode input capacitance of less than 5 pF inclusive of power isolation. This results in CMR ranging from 130 dB at a gain of 100 dB to 104 dB (minimum at unity gain) and very low leakage current (2 μA maximum).

Flexible Input: An uncommitted op amp is provided at the input of all models. This provides buffering and gain as required, and facilitates many alternative input functions including filtering, summing, high voltage ranges, and current (transimpedance) input.

Isolated Power: The AD204 can supply isolated power of ±7.5 V at 2 mA. This is sufficient to operate a low-drift input preamp, provide excitation to a semiconductor strain gage, or power any of a wide range of user-supplied ancillary circuits. The AD202 can supply ±7.5 V at 0.4 mA, which is sufficient to operate adjustment networks or low power references and op amps, or to provide an open-input alarm.

REV. D

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Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

AD202/AD204—SPECIFICATIONS (Typical @ 25°C and V_S = 15 V unless otherwise noted.)

Model	AD204J	AD204K	AD202J	AD202K
GAIN				
Range	1 V/V–100 V/V	*	*	*
Error	±0.5% typ (±4% max)	*	*	*
vs. Temperature	±20 ppm/°C typ (±45 ppm/°C max)	*	*	*
vs. Time	±50 ppm/1000 Hours	*	*	*
vs. Supply Voltage	±0.01%/V	±0.01%/V	±0.01%/V	±0.01%/V
Nonlinearity (G = 1 V/V)[1]	±0.05% max	±0.025% max	±0.05% max	±0.025% max
Nonlinearity vs. Isolated Supply Load	±0.0015%/mA	*	*	*
INPUT VOLTAGE RATINGS				
Input Voltage Range	±5 V	*	*	*
Max Isolation Voltage (Input to Output)				
AC, 60 Hz, Continuous	750 V rms	1500 V rms	750 V rms	1500 V rms
Continuous (AC and DC)	±1000 V Peak	±2000 V Peak	±1000 V Peak	±2000 V Peak
Isolation-Mode Rejection Ratio (IMRR) @ 60 Hz				
$R_S \leq 100\ \Omega$ (HI and LO Inputs) G = 1 V/V	110 dB	110 dB	105 dB	105 dB
G = 100 V/V	130 dB	*	*	*
$R_S \leq 1\ k\Omega$ (Input HI, LO, or Both) G = 1 V/V	104 dB min	104 dB min	100 dB min	100 dB min
G = 100 V/V	110 dB min	*	*	*
Leakage Current Input to Output @ 240 V rms, 60 Hz	2 μA rms max	*	*	*
INPUT IMPEDANCE				
Differential (G = 1 V/V)	$10^{12}\ \Omega$	*	*	*
Common-Mode	2 GΩ‖4.5 pF	*	*	*
INPUT BIAS CURRENT				
Initial, @ 25°C	±30 pA	*	*	*
vs. Temperature (0°C to 70°C)	±10 nA	*	*	*
INPUT DIFFERENCE CURRENT				
Initial, @ 25°C	±5 pA	*	*	*
vs. Temperature (0°C to 70°C)	±2 nA	*	*	*
INPUT NOISE				
Voltage, 0.1 Hz to 100 Hz	4 μV p-p	*	*	*
f > 200 Hz	50 nV/√Hz	*	*	*
FREQUENCY RESPONSE				
Bandwidth ($V_O \leq 10$ V p-p, G = 1 V–50 V/V)	5 kHz	5 kHz	2 kHz	2 kHz
Settling Time, to ±10 mV (10 V Step)	1 ms	*	*	*
OFFSET VOLTAGE (RTI)				
Initial, @ 25°C Adjustable to Zero	(±15 ±15/G)mV max	(±5 ± 5/G) mV max	(±15 ±15/G) mV max	(±5 ±5/G) mV max
vs. Temperature (0°C to 70°C)	$\left(\pm 10 \pm \frac{10}{G}\right)\mu V/°C$	*	*	*
RATED OUTPUT				
Voltage (Out HI to Out LO)	±5 V	*	*	*
Voltage at Out HI or Out LO (Ref. Pin 32)	±6.5 V	*	*	*
Output Resistance	3 kΩ	3 kΩ	7 kΩ	7 kΩ
Output Ripple, 100 kHz Bandwidth	10 mV p-p	*	*	*
5 kHz Bandwidth	0.5 mV rms	*	*	*
ISOLATED POWER OUTPUT[2]				
Voltage, No Load	±7.5 V	*	*	*
Accuracy	±10%	*	*	*
Current	2 mA (Either Output)[3]	2 mA (Either Output)[3]	400 μA Total	400 μA Total
Regulation, No Load to Full Load	5%	*	*	*
Ripple	100 mV p-p	*	*	*
OSCILLATOR DRIVE INPUT				
Input Voltage	15 V p-p Nominal	15 V p-p Nominal	N/A	N/A
Input Frequency	25 kHz Nominal	25 kHz Nominal	N/A	N/A
POWER SUPPLY (AD202 Only)				
Voltage, Rated Performance	N/A	N/A	15 V ± 5%	15 V ± 5%
Voltage, Operating	N/A	N/A	15 V ± 10%	15 V ± 10%
Current, No Load (V_S = 15 V)	N/A	N/A	5 mA	5 mA
TEMPERATURE RANGE				
Rated Performance	0°C to 70°C	*	*	*
Operating	–40°C to +85°C	*	*	*
Storage	–40°C to +85°C	*	*	*
PACKAGE DIMENSIONS[4]				
SIP Package (Y)	2.08" × 0.250" × 0.625"	*	*	*
DIP Package (N)	2.10" × 0.700" × 0.350"	*	*	*

NOTES
*Specifications same as AD204J.
[1]Nonlinearity is specified as a % deviation from a best straight line.
[2]1.0 μF min decoupling required (see text).
[3]3 mA with one supply loaded.
[4]Width is 0.25" typ, 0.26" max.

Specifications subject to change without notice.

AD246–SPECIFICATIONS

(Typical @ 25°C and V_S = 15 V unless otherwise noted.)

Model	AD246JY	AD246JN
OUTPUT[1]		
Frequency	25 kHz Nominal	*
Voltage	15 V p-p Nominal	*
Fan-Out	32 Max	*
POWER SUPPLY REQUIREMENTS		
Input Voltage	15 V ± 5%	*
Supply Current		
Unloaded	35 mA	*
Each AD204 Adds	2.2 mA	*
Each 1 mA Load on AD204 $+V_{ISO}$ or $-V_{ISO}$ Adds	0.7 mA	*

NOTES
*Specifications the same as the AD246JY.
[1]The high current drive output will not support a short to ground.
Specifications subject to change without notice.

AD246 Pin Designations

Pin (Y)	Pin (N)	Function
1	12	15 V POWER IN
2	1	CLOCK OUTPUT
12	14	COMMON
13	24	COMMON

PIN DESIGNATIONS

AD202/AD204 SIP Package

Pin	Function
1	+INPUT
2	INPUT/V_{ISO} COMMON
3	–INPUT
4	INPUT FEEDBACK
5	$-V_{ISO}$ OUTPUT
6	$+V_{ISO}$ OUTPUT
31	15 V POWER IN (AD202 ONLY)
32	CLOCK/POWER COMMON
33	CLOCK INPUT (AD204 ONLY)
37	OUTPUT LO
38	OUTPUT HI

AD202/AD204 DIP Package

Pin	Function
1	+INPUT
2	INPUT/V_{ISO} COMMON
3	–INPUT
18	OUTPUT LO
19	OUTPUT HI
20	15 V POWER IN (AD202 ONLY)
21	CLOCK INPUT (AD204 ONLY)
22	CLOCK/POWER COMMON
36	$+V_{ISO}$ OUTPUT
37	$-V_{ISO}$ OUTPUT
38	INPUT FEEDBACK

ORDERING GUIDE

Model	Package Option	Max Common-Mode Voltage (Peak)	Max Linearity
AD202JY	SIP	1000 V	±0.05%
AD202KY	SIP	2000 V	±0.025%
AD202JN	DIP	1000 V	±0.05%
AD202KN	DIP	2000 V	±0.025%
AD204JY	SIP	1000 V	±0.05%
AD204KY	SIP	2000 V	±0.025%
AD204JN	DIP	1000 V	±0.05%
AD204KN	DIP	2000 V	±0.025%

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD202/AD204 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

DIFFERENCES BETWEEN THE AD202 AND AD204

The primary distinction between the AD202 and AD204 is in the method by which they are powered: the AD202 operates directly from 15 V dc while the AD204 is powered by a non-isolated externally-supplied clock (AD246) that can drive up to 32 AD204s. The main advantages of using the externally-clocked AD204 over the AD202 are reduced cost in multichannel applications, lower power consumption, and higher bandwidth. In addition, the AD204 can supply substantially more isolated power than the AD202.

Of course, in a great many situations, especially where only one or a few isolators are used, the convenience of standalone operation provided by the AD202 will be more significant than any of the AD204's advantages. There may also be cases where it is desirable to accommodate either device interchangeably, so the pinouts of the two products have been designed to make that easy to do.

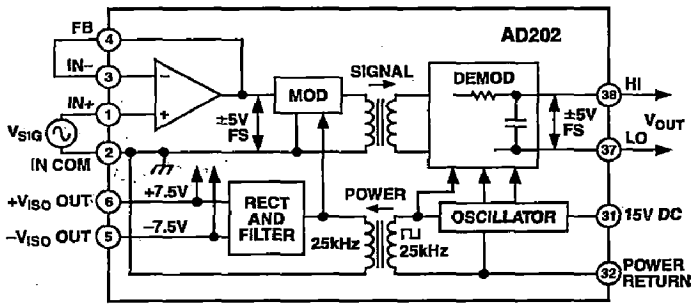


Figure 1a. AD202 Functional Block Diagram

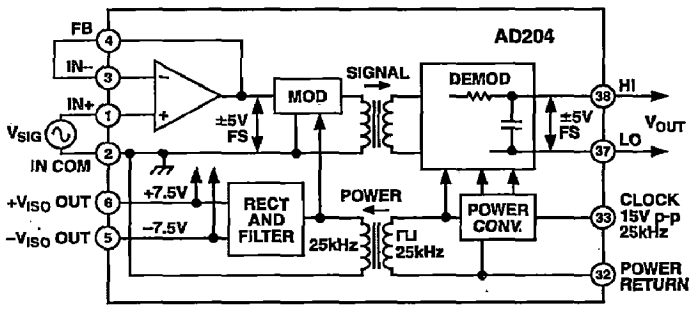


Figure 1b. AD204 Functional Block Diagram (Pin Designations Apply to the DIP-Style Package)

INSIDE THE AD202 AND AD204

The AD202 and AD204 use an amplitude modulation technique to permit transformer coupling of signals down to dc (Figure 1a and 1b). Both models also contain an uncommitted input op amp and a power transformer that provides isolated power to the op amp, the modulator, and any external load. The power transformer primary is driven by a 25 kHz, 15 V p-p square wave generated internally in the case of the AD202, or supplied externally for the AD204.

Within the signal swing limits of approximately ±5 V, the output voltage of the isolator is equal to the output voltage of the op amp; that is, the isolation barrier has unity gain. The output signal is not internally buffered, so the user is free to interchange the output leads to get signal inversion. Additionally, in multichannel applications, the unbuffered outputs can be multiplexed with one buffer following the mux. This technique minimizes offset errors while reducing power consumption and cost. The output resistance of the isolator is typically 3 kΩ for the AD204 (7 kΩ for AD202) and varies with signal level and temperature, so it should not be loaded (see Figure 2 for the effects of load upon nonlinearity and gain drift). In many cases, a high impedance load will be present or a following circuit such as an output filter can serve as a buffer so that a separate buffer function will not often be needed.

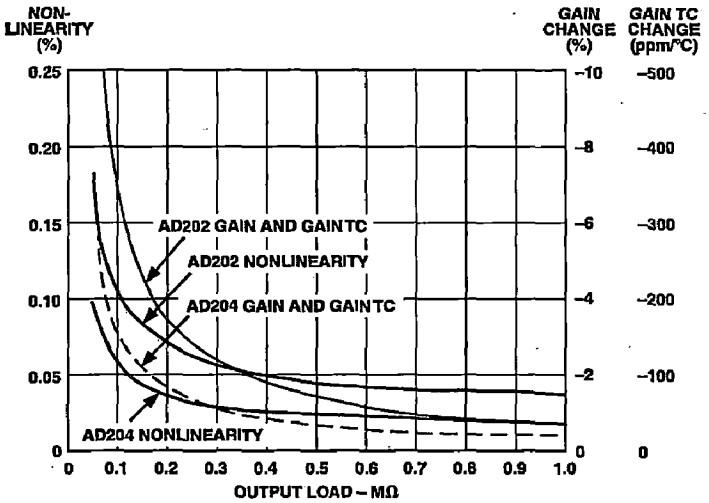


Figure 2. Effects of Output Loading

USING THE AD202 AND AD204

Powering the AD202. The AD202 requires only a single 15 V power supply connected as shown in Figure 3a. A bypass capacitor is provided in the module.

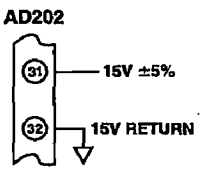


Figure 3a.

Powering the AD204. The AD204 gets its power from an externally supplied clock signal (a 15 V p-p square wave with a nominal frequency of 25 kHz) as shown in Figure 3b.

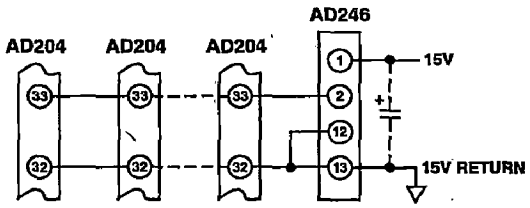


Figure 3b.

(NOTE: Circuit figures shown on this page are for SIP-style packages. Refer to Page 3 for proper DIP package pinout.)

AD246 Clock Driver. The AD246 is a compact, inexpensive clock driver that can be used to obtain the required clock from a single 15 V supply. Alternatively, the circuit shown in Figure 4 (essentially an AD246) can be used. In either case, one clock circuit can operate at least 32 AD204s at the rated minimum supply voltage of 14.25 V and one additional isolator can be operated for each 40 mV increase in supply voltage up to 15 V.

A supply bypass capacitor is included in the AD246, but if many AD204s are operated from a single AD246, an external bypass capacitor should be used with a value of at least 1 µF for every five isolators used. Place the capacitor as close as possible to the clock driver.

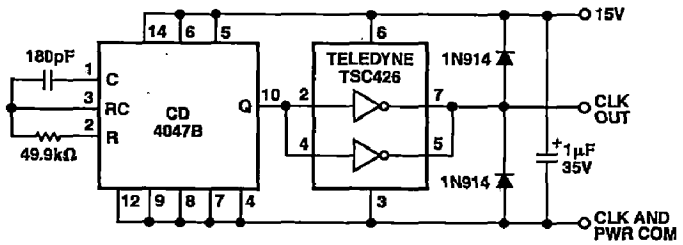


Figure 4. Clock Driver

Input Configurations. The AD202 and AD204 have been designed to be very easy to use in a wide range of applications. The basic connection for standard unity gain applications, useful for signals up to ±5 V, is shown in Figure 5; some of the possible variations are described below. When smaller signals must be handled, Figure 6 shows how to achieve gain while preserving a very high input resistance. The value of feedback resistor R_F should be kept above 20 kΩ for best results. Whenever a gain of more than five is taken, a 100 pF capacitor from FB to IN COM is required. At lower gains this capacitor is unnecessary, but it will not adversely affect performance if used.

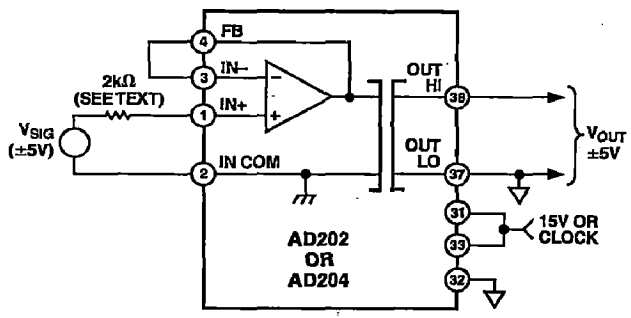


Figure 5. Basic Unity-Gain Application

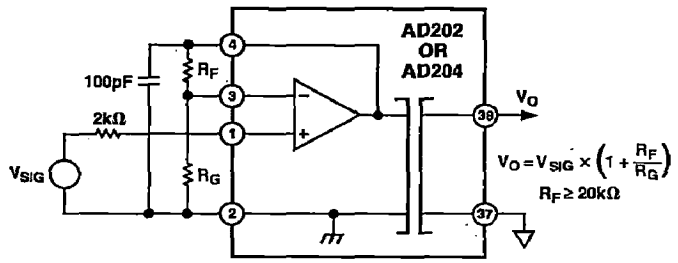


Figure 6. Input Connections for Gain > 1

The noninverting circuit of Figures 5 and 6 can also be used to your advantage when a signal inversion is needed: just interchange either the input leads or the output leads to get inversion. This approach retains the high input resistance of the noninverting circuit, and at unity gain no gain-setting resistors are needed.

When the isolator is not powered, a negative input voltage of more than about 2 V will cause an input current to flow. If the signal source can supply more than a few mA under such conditions, the 2 kΩ resistor shown in series with IN+ should be used to limit current to a safe value. This is particularly important with the AD202, which may not start if a large input current is present.

Figure 7 shows how to accommodate current inputs or sum currents or voltages. This circuit can also be used when the input signal is larger than the ±5 V input range of the isolator; for example, a ±50 V input span can be accommodated with R_F = 20 kΩ and R_S = 200 kΩ. Once again, a capacitor from FB to IN COM is required for gains above five.

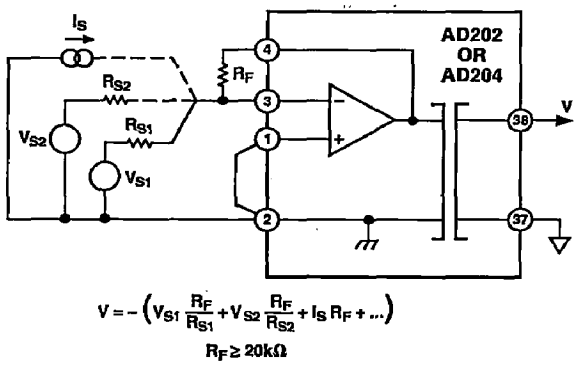


Figure 7. Connections for Summing or Current Inputs

(NOTE: Circuit figures shown on this page are for SIP-style packages. Refer to Page 3 for proper DIP package pinout.)

Adjustments. When gain and zero adjustments are needed, the circuit details will depend on whether adjustments are to be made at the isolator input or output, and (for input adjustments) on the input circuit used. Adjustments are usually best done on the input side, because it is better to null the zero ahead of the gain, and because gain adjustment is most easily done as part of the gain-setting network. Input adjustments are also to be preferred when the pots will be near the input end of the isolator (to minimize common-mode strays). Adjustments on the output side might be used if pots on the input side would represent a hazard due to the presence of large common-mode voltages during adjustment.

Figure 8a shows the input-side adjustment connections for use with the noninverting connection of the input amplifier. The zero adjustment circuit injects a small adjustment voltage in series with the low side of the signal source. (This will not work if the source has another current path to input common or if current flows in the signal source LO lead). Since the adjustment voltage is injected ahead of the gain, the values shown will work for any gain. Keep the resistance in series with input LO below a few hundred ohms to avoid CMR degradation.

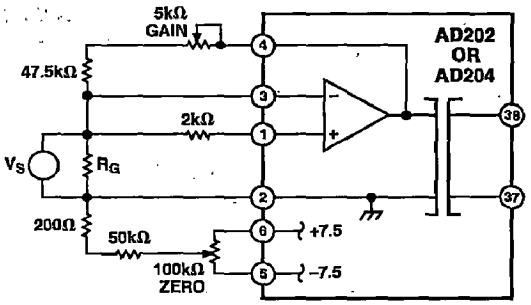


Figure 8a. Adjustments for Noninverting Connection of Op Amp

Also shown in Figure 8a is the preferred means of adjusting the gain-setting network. The circuit shown gives a nominal R_F of 50 kΩ, and will work properly for gains of ten or greater. The adjustment becomes less effective at lower gains (its effect is halved at G = 2) so that the pot will have to be a larger fraction of the total R_F at low gain. At G = 1 (follower) the gain cannot be adjusted downward without compromising input resistance; it is better to adjust gain at the signal source or after the output.

Figure 8b shows adjustments for use with inverting input circuits. The zero adjustment nulls the voltage at the summing node. This method is preferable to current injection because it is less affected by subsequent gain adjustment. Gain adjustment is again done in the feedback; but in this case it will work all the way down to unity gain (and below) without alteration.

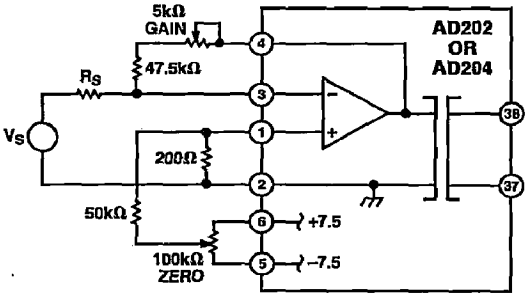


Figure 8b. Adjustments for Summing or Current Input

Figure 9 shows how zero adjustment is done at the output by taking advantage of the semi-floating output port. The range of this adjustment will have to be increased at higher gains; if that is done, be sure to use a suitably stable supply voltage for the pot circuit.

There is no easy way to adjust gain at the output side of the isolator itself. If gain adjustment must be done on the output side, it will have to be in a following circuit such as an output buffer or filter.

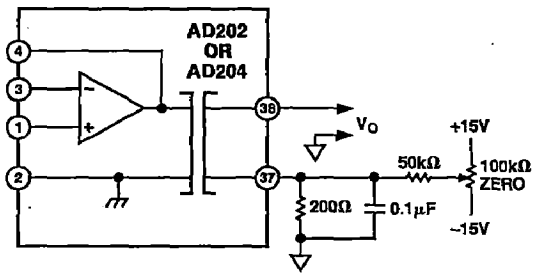


Figure 9. Output-Side Zero Adjustment

Common-Mode Performance. Figures 10a and 10b show how the common-mode rejection of the AD202 and AD204 varies with frequency, gain, and source resistance. For these isolators, the significant resistance will normally be that in the path from the source of the common-mode signal to IN COM. The AD202 and AD204 also perform well in applications requiring rejection of fast common-mode steps, as described in the Applications section.

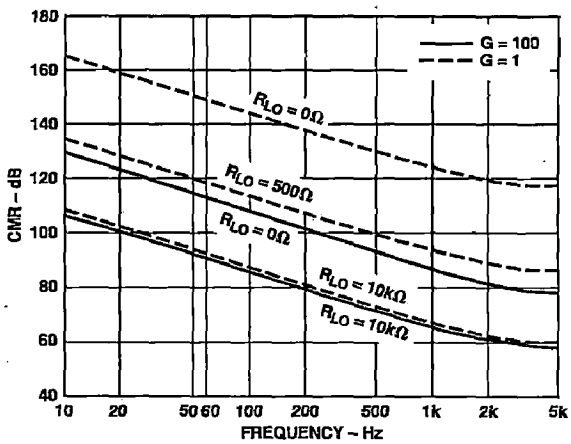


Figure 10a. AD204

(NOTE: Circuit figures shown on this page are for SIP-style packages. Refer to Page 3 for proper DIP package pinout.)

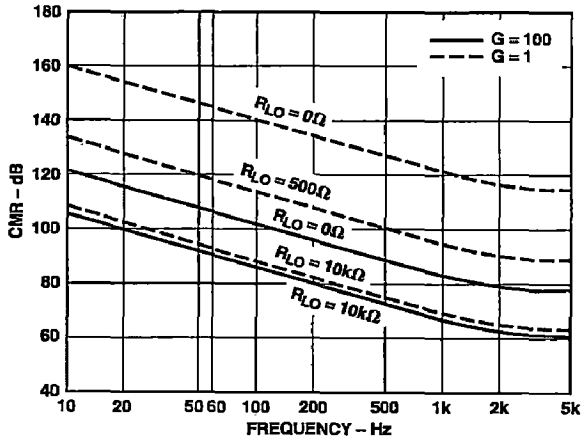


Figure 10b. AD202

Dynamics and Noise. Frequency response plots for the AD202 and AD204 are given in Figure 11. Since neither isolator is slew-rate limited, the plots apply for both large and small signals. Capacitive loads of up to 470 pF will not materially affect frequency response. When large signals beyond a few hundred Hz will be present, it is advisable to bypass $-V_{ISO}$ and $+V_{ISO}$ to IN COM with 1 µF tantalum capacitors even if the isolated supplies are not loaded.

At 50 Hz/60 Hz, phase shift through the AD202/AD204 is typically 0.8° (lagging). Typical unit to unit variation is ±0.2° (lagging).

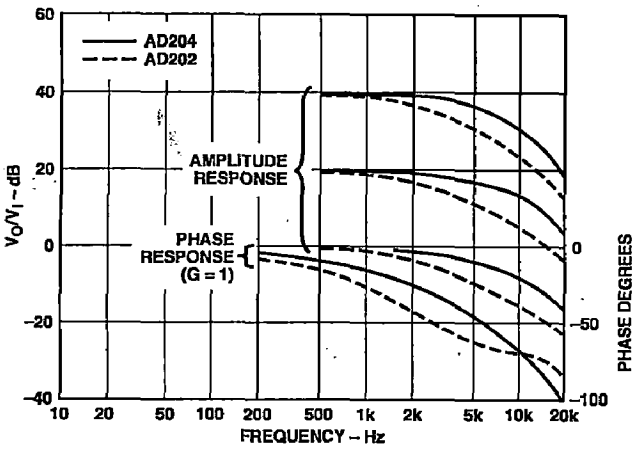


Figure 11. Frequency Response at Several Gains

The step response of the AD204 for very fast input signals can be improved by the use of an input filter, as shown in Figure 12. The filter limits the bandwidth of the input (to about 5.3 kHz) so that the isolator does not see fast, out-of-band input terms that can cause small amounts (±0.3%) of internal ringing. The AD204 will then settle to ±0.1% in about 300 µs for a 10 V step.

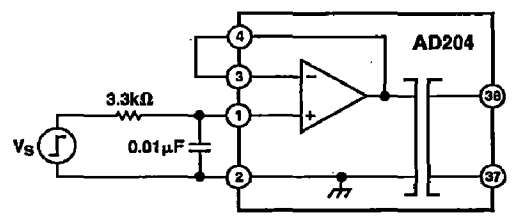


Figure 12. Input Filter for Improved Step Response

Except at the highest useful gains, the noise seen at the output of the AD202 and AD204 will be almost entirely comprised of carrier ripple at multiples of 25 kHz. The ripple is typically 2 mV p-p near zero output and increases to about 7 mV p-p for outputs of ±5 V (1 MHz measurement bandwidth). Adding a capacitor across the output will reduce ripple at the expense of bandwidth: for example, 0.05 µF at the output of the AD204 will result in 1.5 mV ripple at ±5 V, but signal bandwidth will be down to 1 kHz.

When the full isolator bandwidth is needed, the simple two-pole active filter shown in Figure 13 can be used. It will reduce ripple to 0.1 mV p-p with no loss of signal bandwidth, and also serves as an output buffer.

An output buffer or filter may sometimes show output spikes that do not appear at its input. This is usually due to clock noise appearing at the op amp's supply pins (since most op amps have little or no supply rejection at high frequencies). Another common source of carrier-related noise is the sharing of a ground track by both the output circuit and the power input. Figure 13 shows how to avoid these problems: the clock/supply port of the isolator does not share ground or 15 V tracks with any signal circuits, and the op amp's supply pins are bypassed to signal common (note that the grounded filter capacitor goes here as well). Ideally, the output signal LO lead and the supply common meet where the isolator output is actually measured, e.g., at an A/D converter input. If that point is more than a few feet from the isolator, it may be useful to bypass output LO to supply common at the isolator with a 0.1 µF capacitor.

In applications where more than a few AD204s are driven by a single clock driver, substantial current spikes will flow in the power return line and in whichever signal out lead returns to a low impedance point (usually output LO). Both of these tracks should be made large to minimize inductance and resistance; ideally, output LO should be directly connected to a ground plane which serves as measurement common.

Current spikes can be greatly reduced by connecting a small inductance (68 µH–100 µH) in series with the clock pin of each AD204. Molded chokes such as the Dale IM-2 series, with dc resistance of about 5 Ω, are suitable.

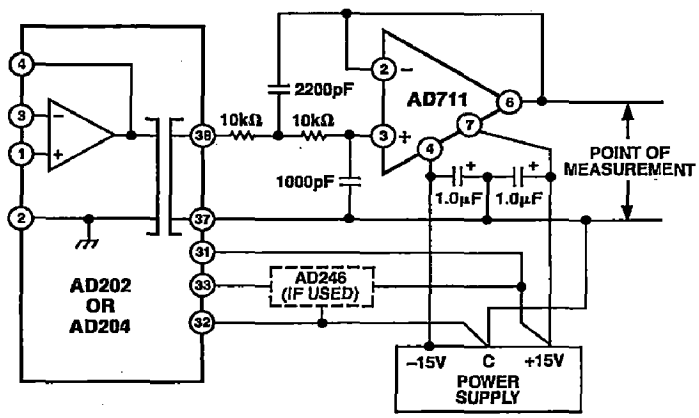


Figure 13. Output Filter Circuit Showing Proper Grounding

(NOTE: Circuit figures shown on this page are for SIP-style packages. Refer to Page 3 for proper DIP package pinout.)

Using Isolated Power. Both the AD202 and the AD204 provide ±7.5 V power outputs referenced to input common. These may be used to power various accessory circuits that must operate at the input common-mode level; the input zero adjustment pots described above are an example, and several other possible uses are shown in the section titled Application Examples.

The isolated power output of the AD202 (400 µA total from either or both outputs) is much more limited in current capacity than that of the AD204, but it is sufficient for operating micropower op amps, low power references (such as the AD589), adjustment circuits, and the like.

The AD204 gets its power from an external clock driver, and can handle loads on its isolated supply outputs of 2 mA for each supply terminal (+7.5 V and –7.5 V) or 3 mA for a single loaded output. Whenever the external load on either supply is more than about 200 µA, a 1 µF tantalum capacitor should be used to bypass each loaded supply pin to input common.

Up to 32 AD204s can be driven from a single AD246 (or equivalent) clock driver when the isolated power outputs of the AD204s are loaded with less than 200 µA each, at a worst-case supply voltage of 14.25 V at the clock driver. The number of AD204s that can be driven by one clock driver is reduced by one AD204 per 3.5 mA of isolated power load current at 7.5 V, distributed in any way over the AD204s being supplied by that clock driver. Thus a load of 1.75 mA from $+V_{ISO}$ to $-V_{ISO}$ would also count as one isolator because it spans 15 V.

It is possible to increase clock fanout by increasing supply voltage above the 14.25 V minimum required for 32 loads. One additional isolator (or 3.5 mA unit load) can be driven for each 40 mV of increase in supply voltage up to 15 V. Therefore if the minimum supply voltage can be held to 15 V – 1%, it is possible to operate 32 AD204s and 52 mA of 7.5 V loads. Figure 14 shows the allowable combinations of load current and channel count for various supply voltages.

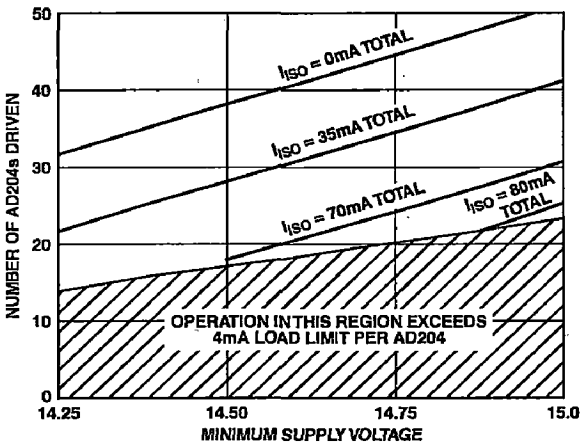


Figure 14. AD246 Fanout Rules

Operation at Reduced Signal Swing. Although the nominal output signal swing for the AD202 and AD204 is ±5 V, there may be cases where a smaller signal range is desirable. When that is done, the fixed errors (principally offset terms and output noise) become a larger fraction of the signal, but nonlinearity is reduced. This is shown in Figure 15.

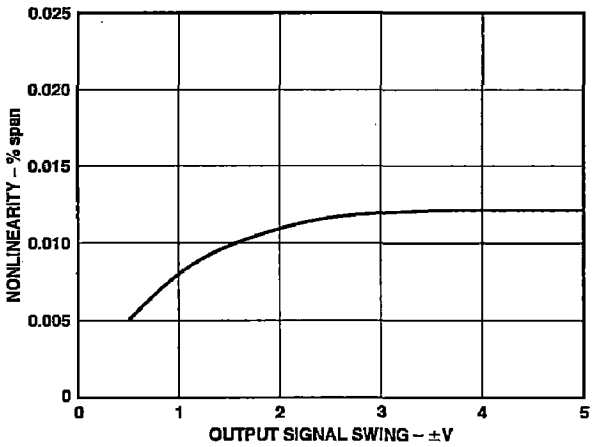


Figure 15. Nonlinearity vs. Signal Swing

PCB Layout for Multichannel Applications. The pinout of the AD204Y has been designed to make very dense packing possible in multichannel applications. Figure 16a shows the recommended printed circuit board (PCB) layout for the simple voltage-follower connection. When gain-setting resistors are present, 0.25" channel centers can still be achieved, as shown in Figure 16b.

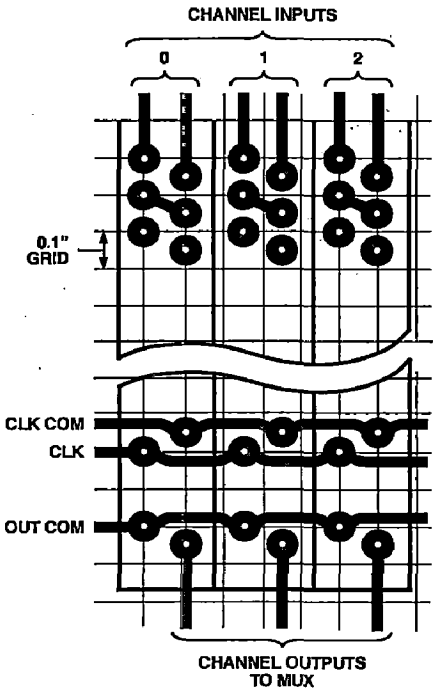


Figure 16a.

(NOTE: Circuit figures shown on this page are for SIP-style packages. Refer to Page 3 for proper DIP package pinout.)

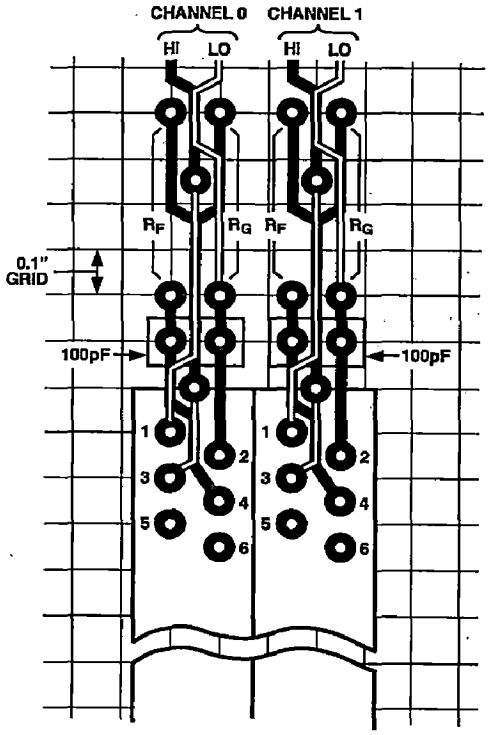


Figure 16b.

Synchronization. Since AD204s operate from a common clock, synchronization is inherent. AD202s will normally not interact to produce beat frequencies even when mounted on 0.25-inch centers. Interaction may occur in rare situations where a large number of long, unshielded input cables are bundled together and channel gains are high. In such cases, shielded cable may be required or AD204s can be used.

APPLICATIONS EXAMPLES

Low Level Sensor Inputs. In applications where the output of low level sensors such as thermocouples must be isolated, a low drift input amplifier can be used with an AD204, as shown in Figure 17. A three-pole active filter is included in the design to get normal-mode rejection of frequencies above a few Hz and to provide enhanced common-mode rejection at 60 Hz. If offset adjustment is needed, it is best done at the trim pins of the OP07 itself; gain adjustment can be done at the feedback resistor.

Note that the isolated supply current is large enough to mandate the use of 1 µF supply bypass capacitors. This circuit can be used with an AD202 if a low power op amp is used instead of the OP07.

Process Current Input with Offset. Figure 18 shows an isolator receiver that translates a 4-20 mA process current signal into a 0 V to 10 V output. A 1 V to 5 V signal appears at the isolator's output, and a –1 V reference applied to output LO provides the necessary level shift (in multichannel applications, the reference can be shared by all channels). This technique is often useful for getting offset with a follower-type output buffer.

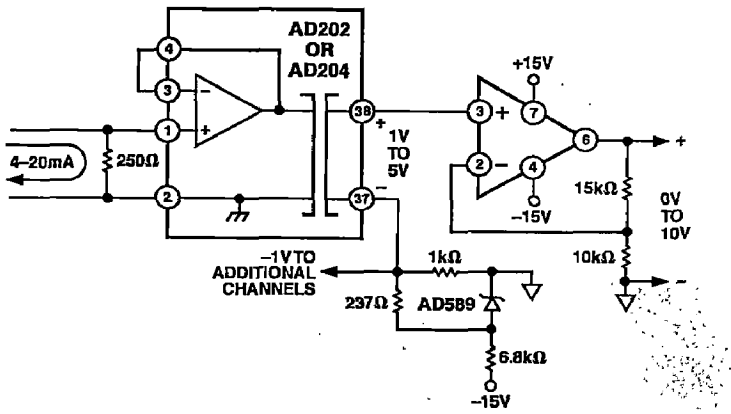


Figure 18. Process Current Input Isolator with Offset

The circuit as shown requires a source compliance of at least 5 V, but if necessary that can be reduced by using a lower value of current-sampling resistor and configuring the input amplifier for a small gain.

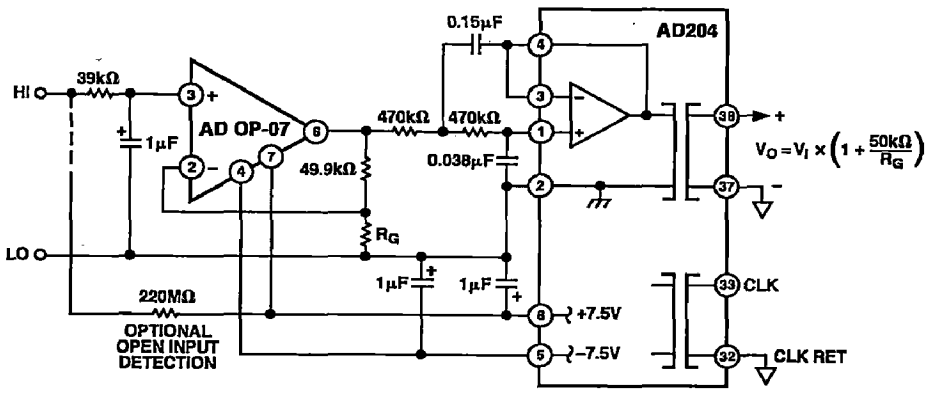


Figure 17. Input Amplifier and Filter for Sensor Signals

(NOTE: Circuit figures shown on this page are for SIP-style packages. Refer to Page 3 for proper DIP package pinout.)

High Compliance Current Source. In Figure 19, an isolator is used to sense the voltage across current-sensing resistor R_S to allow direct feedback control of a high voltage transistor or FET used as a high compliance current source. Since the isolator has virtually no response to dc common-mode voltage, the closed-loop current source has a static output resistance greater than 10^{14} Ω even for output currents of several mA. The output current capability of the circuit is limited only by power dissipation in the source transistor.

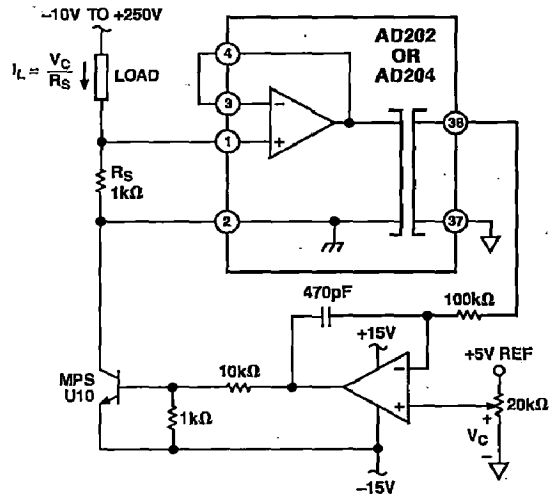


Figure 19. High Compliance Current Source

Motor Control Isolator. The AD202 and AD204 perform very well in applications where rejection of fast common-mode steps is important but bandwidth must not be compromised. Current sensing in a fill-wave bridge motor driver (Figure 20) is one example of this class of application. For 200 V common-mode steps (1 µs rise time) and a gain of 50 as shown, the typical response at the isolator output will be spikes of ±5 mV amplitude, decaying to zero in less than 100 µs. Spike height can be reduced by a factor of four with output filtering just beyond the isolator's bandwidth.

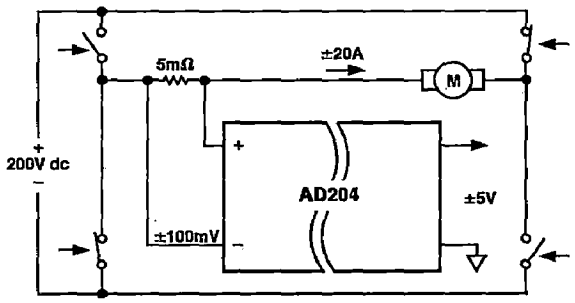


Figure 20. Motor Control Current Sensing

Floating Current Source/Ohmmeter. When a small floating current is needed with a compliance range of up to ±1000 V dc, the AD204 can be used to both create and regulate the current. This can save considerable power, since the controlled current does not have to return to ground. In Figure 21, an AD589 reference is used to force a small fixed voltage across R. That sets the current that the input op amp will have to return through the load to zero its input. Note that the isolator's output isn't needed at all in this application; the whole job is done by the input section. However, the signal at the output could be useful as it's the voltage across the load, referenced to ground. Since the load current is known, the output voltage is proportional to load resistance.

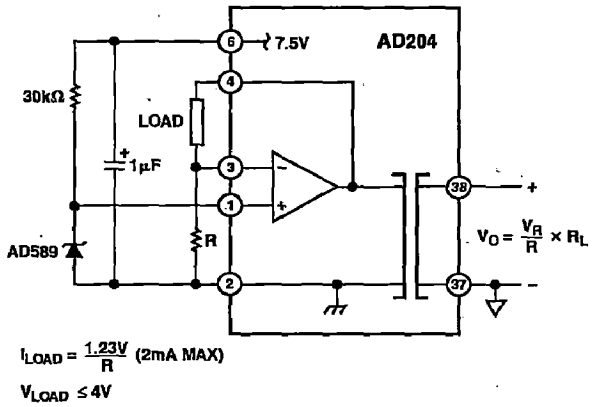


Figure 21. Floating Current Source

Photodiode Amplifier. Figure 22 shows a transresistance connection used to isolate and amplify the output of a photodiode. The photodiode operates at zero bias, and its output current is scaled by R_F to give a 5 V full-scale output.

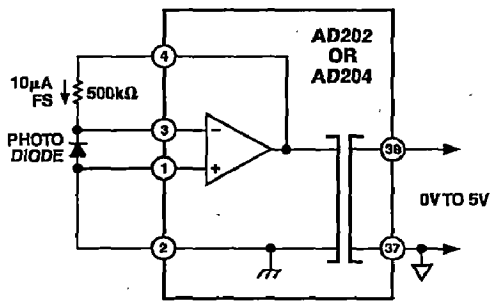


Figure 22. Photodiode Amplifier

(NOTE: Circuit figures shown on this page are for SIP-style packages. Refer to Page 3 for proper DIP package pinout.)

National Semiconductor

December 2003

LF353
Wide Bandwidth Dual JFET Input Operational Amplifier

General Description

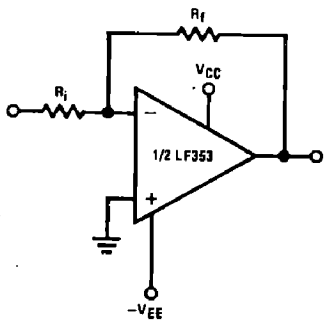
These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF353 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

Features

- Internally trimmed offset voltage: 10 mV
- Low input bias current: 50pA
- Low input noise voltage: 25 nV/√Hz
- Low input noise current: 0.01 pA/√Hz
- Wide gain bandwidth: 4 MHz
- High slew rate: 13 V/µs
- Low supply current: 3.6 mA
- High input impedance: $10^{12}\Omega$
- Low total harmonic distortion : ≤0.02%
- Low 1/f noise corner: 50 Hz
- Fast settling time to 0.01%: 2 µs

Typical Connection



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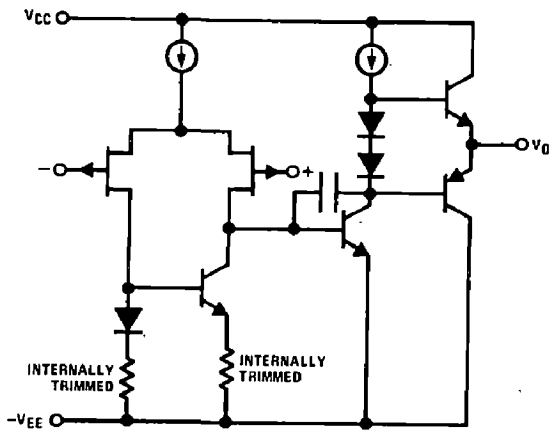
Simplified Schematic

1/2 Dual



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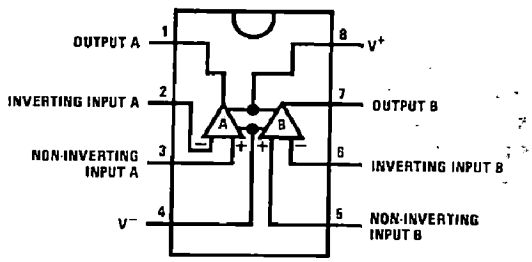
Connection Diagram

Dual-In-Line Package



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Top View
Order Number LF353M, LF353MX or LF353N
See NS Package Number M08A or N08E

BI-FET II™ is a trademark of National Semiconductor Corporation.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation	(Note 2)
Operating Temperature Range	0°C to +70°C
T_j(MAX)	150°C
Differential Input Voltage	±30V
Input Voltage Range (Note 3)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 8)	1000V
θ_{JA} M Package	TBD

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

DC Electrical Characteristics

(Note 5)

Symbol	Parameter	Conditions	LF353			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S=10kΩ, T_A=25°C		5	10	mV
		Over Temperature			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=10 kΩ		10		µV/°C
I_{OS}	Input Offset Current	T_j=25°C, (Notes 5, 6)		25	100	pA
		T_j≤70°C			4	nA
I_B	Input Bias Current	T_j=25°C, (Notes 5, 6)		50	200	pA
		T_j≤70°C			8	nA
R_{IN}	Input Resistance	T_j=25°C		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, T_A=25°C	25	100		V/mV
		V_O=±10V, R_L=2 kΩ				
		Over Temperature	15			V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10kΩ	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage	V_S=±15V	±11	+15		V
	Range			−12		V
CMRR	Common-Mode Rejection Ratio	R_S≤ 10kΩ	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)	70	100		dB
I_S	Supply Current			3.6	6.5	mA

AC Electrical Characteristics

(Note 5)

Symbol	Parameter	Conditions	LF353			Units
			Min	Typ	Max	
	Amplifier to Amplifier Coupling	T_A=25°C, f=1 Hz–20 kHz		−120		dB
		(Input Referred)				
SR	Slew Rate	V_S=±15V, T_A=25°C	8.0	13		V/µs
GBW	Gain Bandwidth Product	V_S=±15V, T_A=25°C	2.7	4		MHz
e_n	Equivalent Input Noise Voltage	T_A=25°C, R_S=100Ω,		16		nV/√Hz
		f=1000 Hz				
i_n	Equivalent Input Noise Current	T_j=25°C, f=1000 Hz		0.01		pA/√Hz

AC Electrical Characteristics (Continued)

(Note 5)

Symbol	Parameter	Conditions	LF353			Units
			Min	Typ	Max	
THD	Total Harmonic Distortion	A_V=+10, RL=10k, V_O=20Vp−p, BW=20 Hz-20 kHz		<0.02		%

Note 2: For operating at elevated temperatures, the device must be derated based on a thermal resistance of 115°C/W typ junction to ambient for the N package, and 158°C/W typ junction to ambient for the H package.

Note 3: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 4: The power dissipation limit, however, cannot be exceeded.

Note 5: These specifications apply for V_S=±15V and 0°C≤T_A≤+70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM}=0.

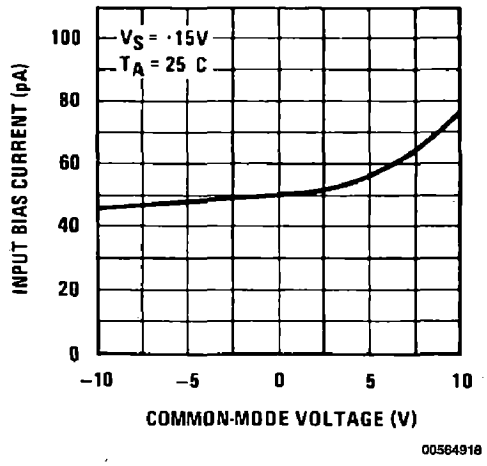
Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. T_j=T_A+θ_{jA} P_D where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. V_S = ±6V to ±15V.

Note 8: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

Input Bias Current



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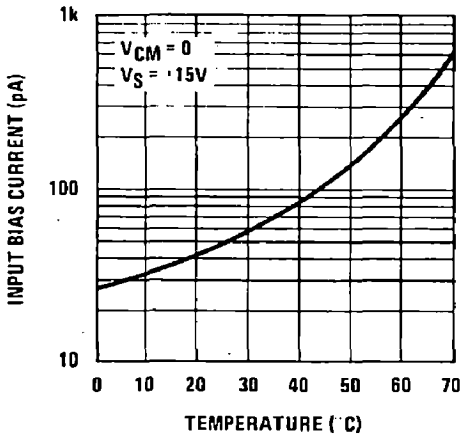
Input Bias Current



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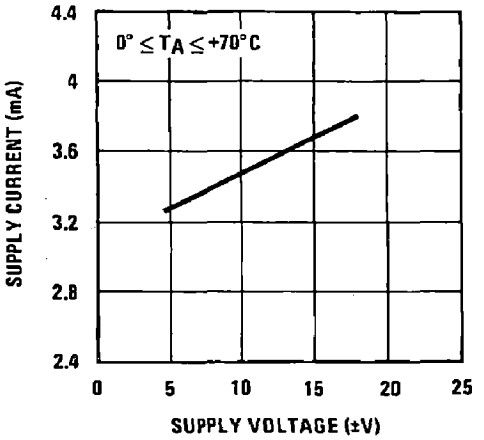
Supply Current



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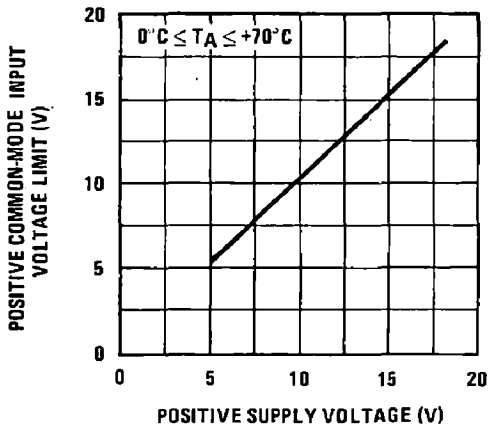
Positive Common-Mode Input Voltage Limit



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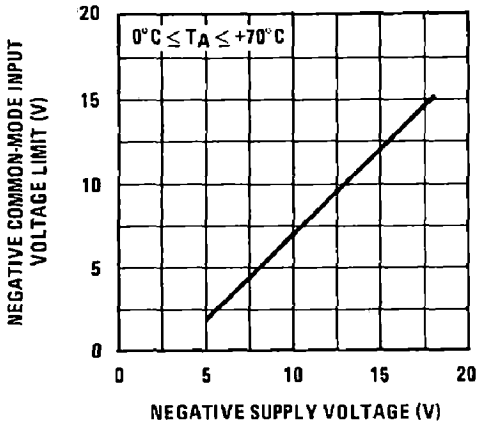
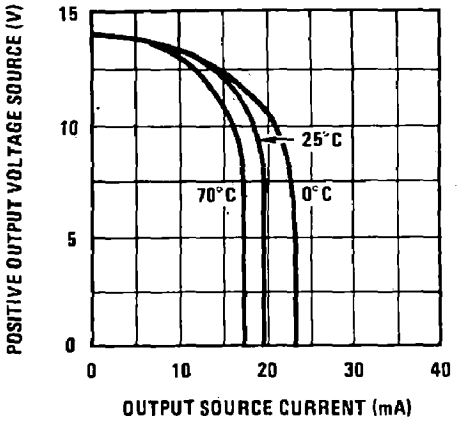
Typical Performance Characteristics (Continued)

Negative Common-Mode Input Voltage Limit



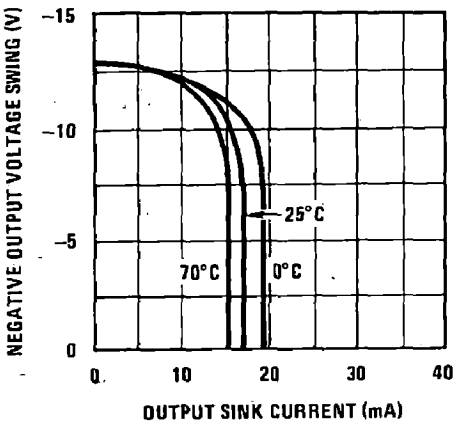
00564922

Positive Current Limit



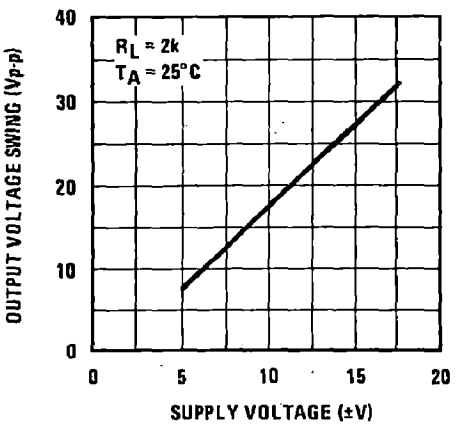
00564923

Negative Current Limit



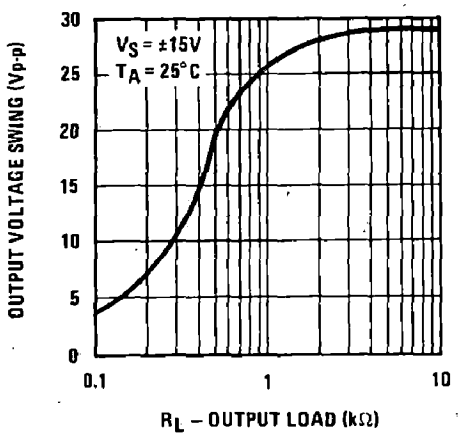
00564924

Voltage Swing



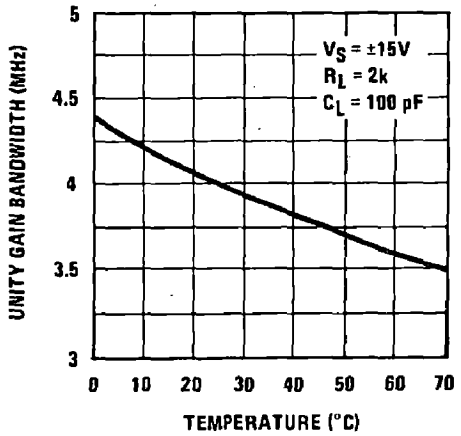
00564925

Output Voltage Swing



00564926

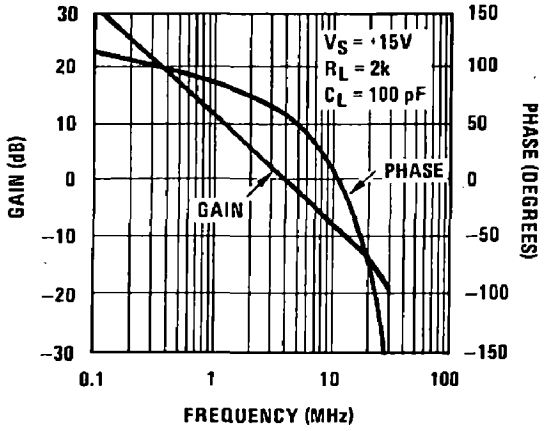
Gain Bandwidth



00564927

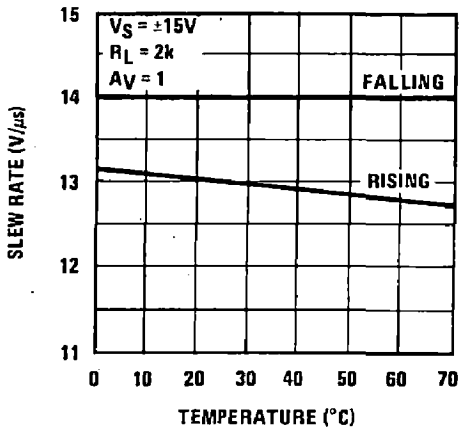
Typical Performance Characteristics (Continued)

Bode Plot



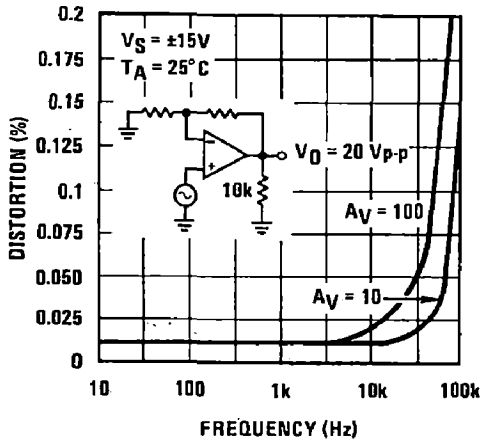
00564928

Slew Rate



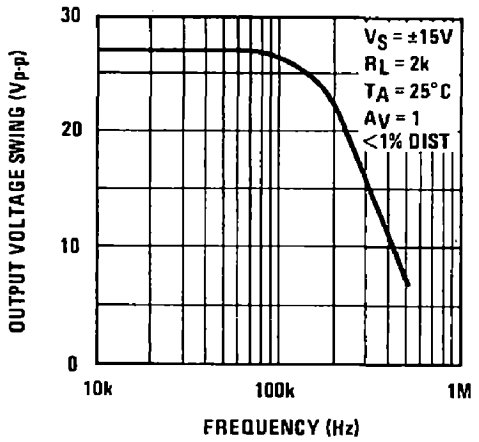
00564929

Distortion vs. Frequency



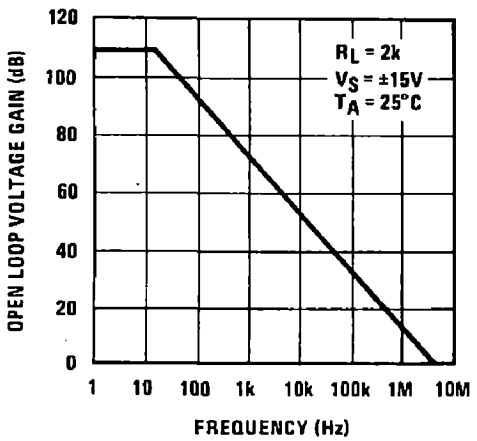
00564930

Undistorted Output Voltage Swing



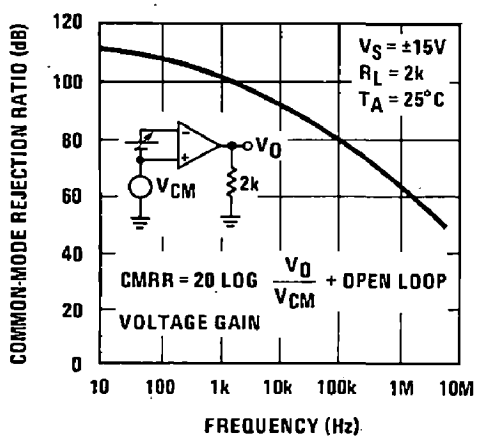
00564931

Open Loop Frequency Response



00564932

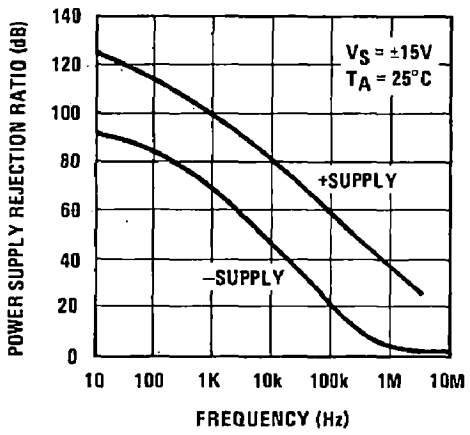
Common-Mode Rejection Ratio



00564933

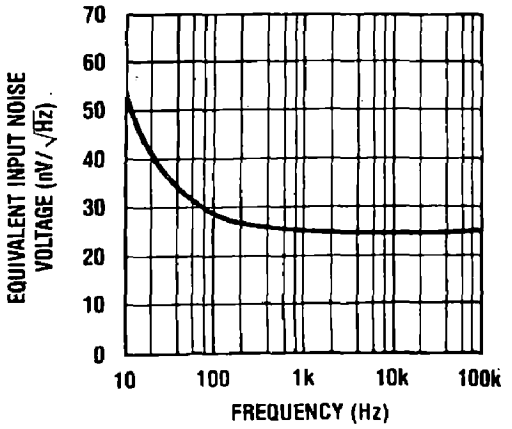
Typical Performance Characteristics (Continued)

Power Supply Rejection Ratio



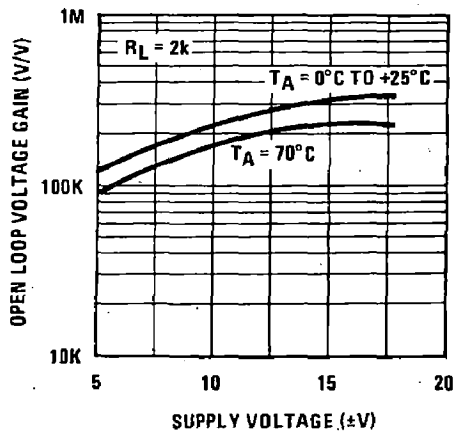
00564934

Equivalent Input Noise Voltage



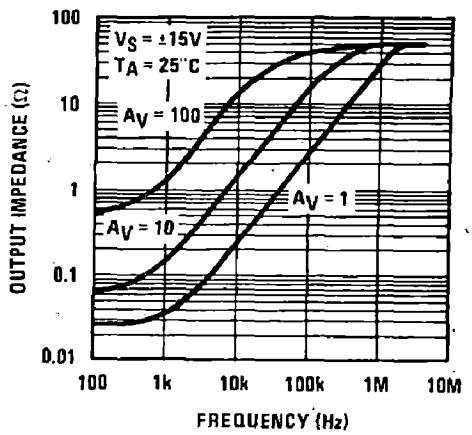
00564935

Open Loop Voltage Gain (V/V)



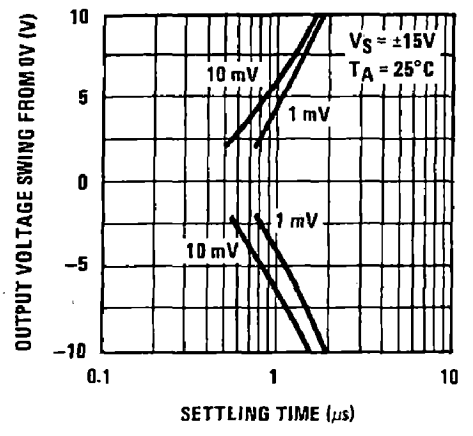
00564936

Output Impedance



00564937

Inverter Settling Time



00564938

List of used IC's, Power Switches, Diode

Semiconductor Switch

I.G.B.T. : GT25Q101, 1200V, 25A

MOSFET : IRFP460, 500V, 20A

Power Diodes

LSR 16 PB, 16A, 1000V

Voltage Sensor

AD 202 Isolation Amplifier

Current Sensor

TELCON HTTP 50, Ratio 1:1000

Voltage Regulator ICs

IC 7805 (+5V), 7812 (+12V), 7912 (-12V)

PLL IC

NE565

Divided by 'N' ICs

7492, 7493

Optocoupler

6N136

Operational Amplifiers

LF353, IC741

Latch IC

IC 7474

Logic Gates

7404 (NOT), 7408 (AND), 7432 (OR)

Boost Inductor

4.4 mH

Output Capacitor

1000μF, 450V (Chopper Output Side)

Load Resistance

300Ω, 2.7A