MODELING AND SIMULATION OF THREE PHASE POWER FACTOR CORRECTED ACTIVE RECTIFIER WITH REDUCED SWITCH COUNT

A DISSERTATION

Submitted in partial fulfillment of the requirements for the award of the degree of

MASTER OF TECHNOLOGY

in

ELECTRICAL ENGINEERING

(With Specialization in Power Apparatus and Electric Drives)

By

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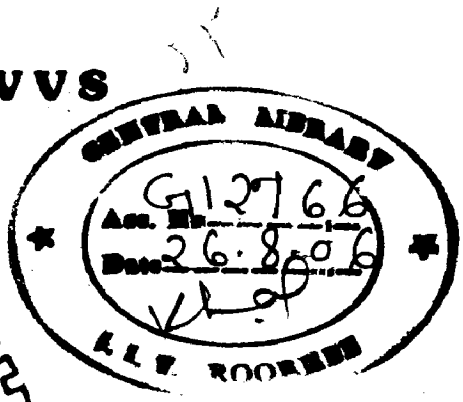

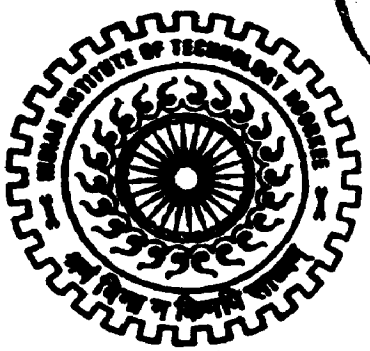

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CANDIDATE'S DECLARATION

I hereby declare that the work that is being presented in this dissertation report entitled **"MODELING AND SIMULATION OF THREE PHASE POWER FACTOR CORRECTED ACTIVE RECTIFIER WITH REDUCED SWITCH COUNT"** submitted in partial fulfillment of the requirements for the award of the degree of **Master Of Technology** with specialization in **Power Apparatus and Electric Drives,** to the **Department Of Electrical Engineering, Indian Institute Of Technology, Roorkee**, is an authentic record of my own work carried out, under the guidance of **Dr. Pramod Agrawal**, Professor, Department of Electrical Engineering.

The matter embodied in this dissertation report has not been submitted by me for the Award of any other degree or diploma.

Date: 29/06/06
Place: Roorkee

(RAVI KUMAR T V V S)

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

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I am also thankful to all my friends for their continuous support and enthusiastic help.

Date: **30-06-2006.**

Place: **ROORKEE.**

(RAVI KUMAR T V V S)

ABSTRACT

The AC–DC converters, also known as rectifiers, are conventionally developed using diodes and thyristors to provide controlled and uncontrolled unidirectional and bidirectional dc power. However, these rectifiers can pollute the AC supply with significant levels of low frequency harmonics, pulsating input current (electromagnetic interference (EMI)), and excessive VAR. With tough regulations and severe economic restraints, the design of a three-phase switching mode rectifier which draws nearly sinusoidal three-phase input currents with unity power factor is very important from the point of view of energy saving and also to satisfy harmonic standards such as IEEE 519 or IEC 1000-3-2.

In response to these problems, a significant amount of research has been devoted to the area of pulse width modulation (PWM) rectifiers (i.e., switching-mode interfaces). Current research has been focusing recently on decreasing the number of power semiconductor switches to simplify the circuit and increase its reliability.

In the present work, a four switch three-phase active rectifier(reduced switch topology) is considered. Detailed power circuit analysis for the undertaken topology is presented. The design considerations are detailed. Four high performance control strategies(reduced hysteresis, space vector modulation, direct power modulation, Fuzzy space vector modulation) are diccussed and verified and compared through simulations. The application of the considered four switch three phase topology to the improvement of power quality is investigated. The considered rectifier can also be used for harmonic current filtering. The feasibility is tested through simulation. A reduced switch count series filter is presented and verified. Finally experimental prototype of the considered four switch three phase rectifier is constructed and tested for reduced hysteresis control scheme.

LIST OF FIGURES

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NOMENCLATURE

PWM	Pulse width Modulation
THD	Total Harmonic Distortion
IEEE	Institute of Electrical ad Electronics Engineers
EMI	Electromagnetic Interference
IEC	International Electro technical Commission
PFC	Power Factor correction
KHz	Kilo-Hertz
IGBT	Insulated Gate Bi-polar Transistor
PI	Proportional Integral
VSI	Voltage source inverter
MOV	Metal Oxide Varistor
SVM	Space Vector Modulation
DPM	Direct Power Modulation
FFT	Fast Fourier Transform
AC	Alternating Current
DC	Direct Current
IC	Integrated Chip

CONTENTS

Class A includes: balanced three-phase equipment; household appliances, excluding equipment identified as Class D, tools, excluding portable tools, dimmers for incandescent lamps; and audio equipment. Equipment not specified in one of the other three classes should be considered as Class A equipment. The limits for Class A are presented in Table 1.1.

Class B equipment includes: portable tools; and nonprofessional arc welding equipment. The limits for this class are those shown in Table 1.2 multiplied by a factor of 1.5.

TABLE 1.2

Harmonic order 'n'	Maximum permissible harmonic current Expressed as a percentage of the input Current at the fundamental frequency %
2	2
3	30.PF *
5	10
7	7
9	5
11. n. 39	3
PF * is the circuit power factor	

Class C includes lighting equipment. For an active input power greater than 25W, the harmonic currents should not exceed the limits resented in Table 1.2 the harmonic limits for Class D are presented in Table 1.3. They are defined in both power related and absolute terms. These includes personal computers, personal computer monitors, and television receivers, equipment having active input power less than or equal to 600W.

TABLE 1.3

Harmonic order 'n'	Maximum permissible Harmonic current per Watt 'Ma/W'	Maximum permissible Harmonic current 'A'
3	3.4	2.30
5	1.9	1.14
7	1.0	0.77
9	0.5	0.44
11	0.35	0.33
13. n. 39	3.85. n	As in Class A

- It causes poor voltage regulation at the load.
- As the load voltage decreases due to poor voltage regulation the power transfer capacity is adversely affected
- The investment in system facilities per KW of load supplied increases with decrease in supply power factor

Improving the power factor brings three benefits:

- Power distribution costs for the electric company are reduced, making the power company much happier. A side benefit is to reduce the tendency of the current peaks to "flatten" the tops of the input voltage sinusoidal waveform.
- More power can be drawn from a line of a given current rating, allowing more powerful equipment to be connected without having to re-wire a building, saving time and money.
- Various governmental and quasi-governmental agencies are passing laws requiring improved power factors on certain types of equipment, especially those which draw a lot of power. These laws make it illegal to sell certain types of equipment without testing and certification of a minimum power factor. To continue to sell medium-to high power supplies in the future, power supply manufacturers will have to deal with power factor correction.

Because of the severity of problems due to low power factor, some options such as passive filters, active filters, and hybrid filters, to be used along with traditional Thyristor/Diode rectifiers have been extensively developed, especially in large rating and already existing installations. However, these filters are quite costly, bulky, and have reasonable losses, which reduce overall efficiency of the complete system. Even in some cases the rating of converter used in active filters is almost close to the rating of the load. Under such circumstances, it is considered better option to use such converters as an inherent part of the system of AC-DC conversion, which provides reduced size, high efficiency, and well controlled and regulated DC to provide comfortable and flexible operation of the system.

transformers and tapped inductors. Therefore, the last category is multipulse converters with unidirectional and bidirectional power flow.

One of the important reasons for such an extensive development in ac–dc converters is due to self-commutating devices. At low power rating, MOSFETs are used with unsurpassed performance because of their high switching rate with negligible losses. At medium power rating, an IGBT is considered an ideal device for such converters with PWM technology. At a higher power rating, a GTO is normally used with self-commutating and reverse voltage-blocking capabilities at only a few kilohertz switching frequency. Another breakthrough in PFCs has been because of fast response Hall-effect voltage and current sensors, and isolation amplifiers normally required for the feedback used in the control of these ac–dc converters result in a high level of dynamic and steady-state performance. Many manufacturers, such as ABB, LEM, HEME, Analog Devices, and others are offering the sensors at competitively low prices. A major boost to the technology of PFCs has also been due to the revolution in microelectronics. Because of the heavy volume requirement, a number of manufacturers have developed dedicated ICs for cost-effective and compact control of these converters. Moreover, high-speed microcontrollers and digital signal processors (DSPs) are available at reasonable cost. Many processors have been developed to give direct PWM outputs with fast software algorithms such as space-vector control (SVC), normally used in some of these converters, which reduce hardware drastically. With these processors it is now possible to implement new and improved control algorithms to provide fast dynamic performance of PFCs. Starting with proportional– integral (PI) controllers, sliding-mode, fuzzy logic, and neural network- based controllers have been employed for the control of these converters. Some of the popular topologies are presented in Fig. 1.1 through Fig. 1.8.

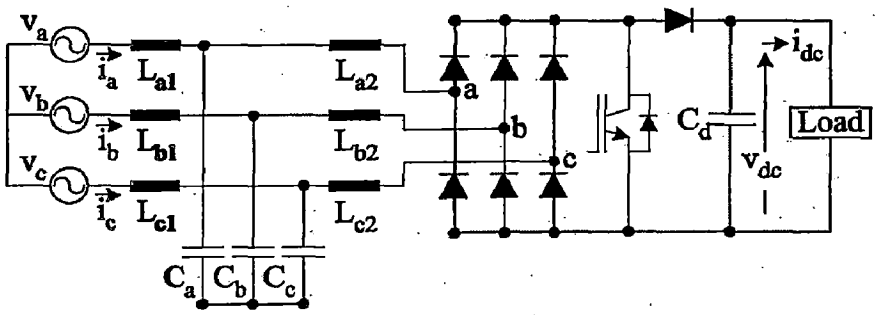


FIG 1.1 SINGLE SWITCH UNIDIRECTIONAL BOOST CONVERTER

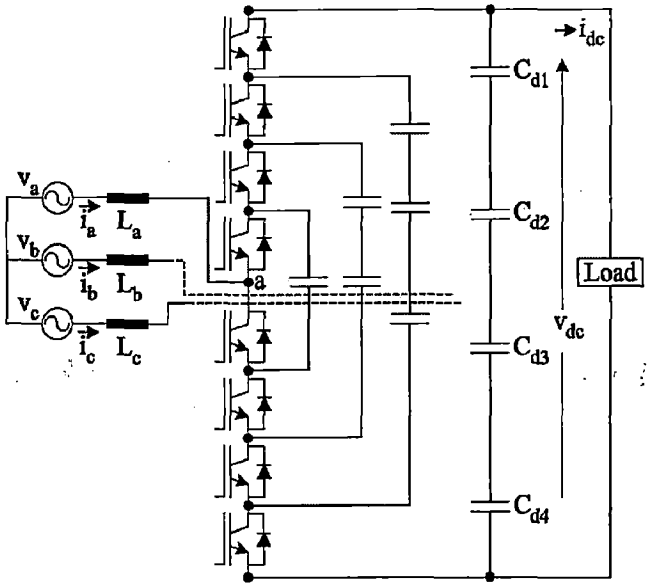


FIG 1.7 FIVE-LEVEL FLYING CAPACITOR BIDIRECTIONAL CONVERTER

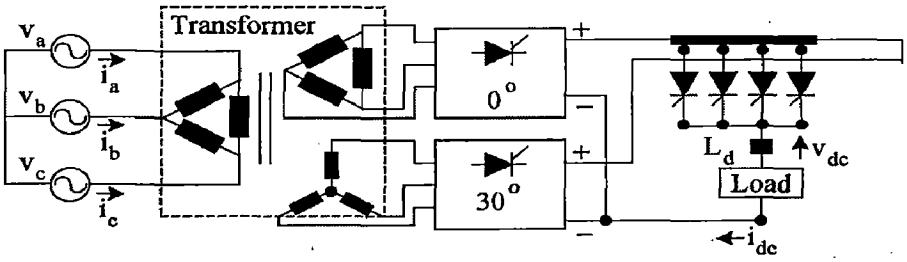


FIG 1.8 48-PULSE BIDIRECTIONAL CONVERTER

1.3 REDUCED SWITCH COUNT PFC RECTIFIERS

The PFC stage performs an additional power processing operation, and therefore it has a negative impact on the overall efficiency of the power supply.

Conduction losses are caused by the current flowing through a non-ideal switching device in the on state, which determines a certain voltage drop on the device. A static model of the switching device is useful for estimating the conduction losses. Static models are presented in Fig. 1.9, for on-state diode and MOSFET.

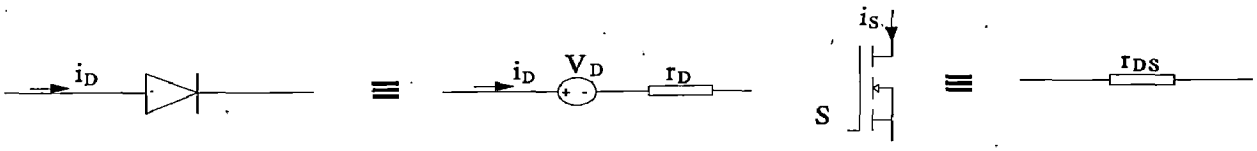


FIG 1.9 STATIC MODELS OF ON STATE SWITCHING DEVICES

- Greater switching frequencies required for same performance.

1.4 LITERATURE SURVEY

Maoh chin Jiang[2] proposed a novel three-phase bidirectional interface(shown in Fig.1.10) using only four power semiconductor switches to simplify the hardware circuit. The circuit is analyzed and design considerations are elaborated. An accurate simulation model is proposed for convenient simulation using common PC software tools. A critical inductance condition is derived for successful current tracking. The capacity to generate maximum active power is also estimated. A systematic design method for the feedback controller is presented to find the parameters of the controller.

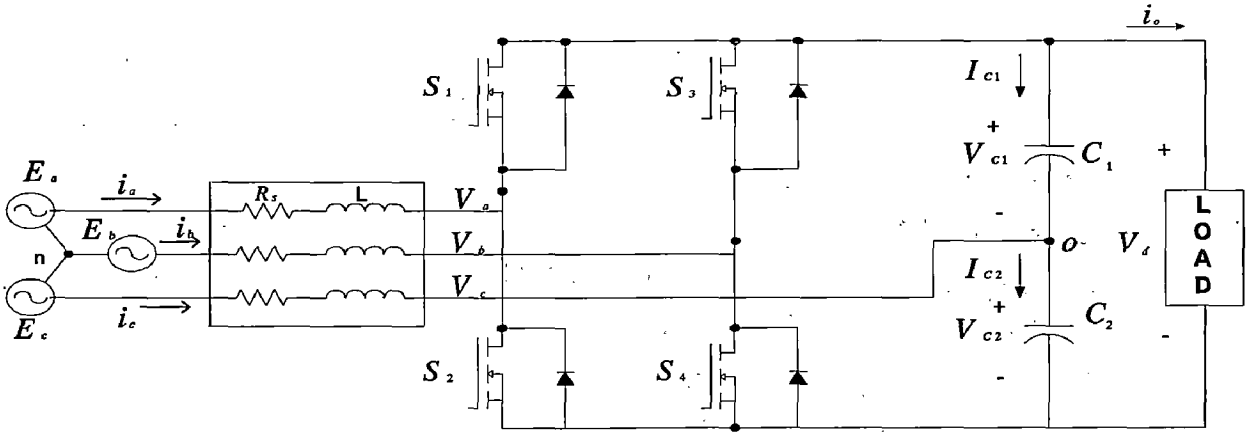


FIG 1.10 NOVEL POWER ELECTRONICS BIDIRECTIONAL INTERFACE

J.J.Shieh, C.-T, Pan Z.-J.Cuey[3], proposed a reversible three-phase switching mode rectifier consisting of a four-active-switch and without current sensor. To achieve controllable power factor, clean sinusoidal input current, adjustable DC output voltage, and bidirectional power flow capability, a closed-form pulse width modulation (PWM) duty cycle function is derived. The popularly used state space averaging technique is extended for modeling the reversible three-phase four-active switch rectifier. The space vector representation technique is then used to simplify the modeling process without sacrificing accuracy and valid frequency range. Both steady-state and small signal analyses are made. Guidelines for determining the *LC* parameters and the PI controller gains are described .

adaptive SVM algorithm with the advantage of improving the response of the dc-link filter and the output quality of the inverter becoming high.

Toshihiko Noguchi, Hiroaki Tomiki, Seiji Kondo, and Isao Takahashi[8] proposed a novel control strategy of a pulse width modulation (PWM) converter with no power-source voltage sensors. The strategy has two main features to improve a total power factor and efficiency, taking harmonic components into account without detecting the voltage waveforms. One feature is a direct instantaneous power control technique for the converter, which has been developed to control the instantaneous active and reactive power directly by selecting the optimum switching state of the converter. The other feature is an estimation technique of the power-source voltages, which can be performed by calculating the active and reactive power for each switching state of the converter from the line currents.

Kevork Haddad and Geza Joos[9] proposed a low cost three-phase active filter based on a PWM voltage structure with a reduced number of switches. Operation, cost, rating, and practical issues are considered and compared with the conventional six switch PWM-VSI. The paper also investigates the unbalance in the voltages of the two capacitors and discusses a new control scheme to eliminate the voltage difference.

Geza Joos Su Chen and Kevork Haddad[10] presented an active filter with reduced numbers of power switches and current sensors. The power circuit is a four-switch voltage source topology with a self controlled dc bus. Two power switches are eliminated, the third phase being connected to the capacitor center tap. Harmonic compensation is achieved by forcing the line current to be sinusoidal and no harmonic current extraction is therefore required. The proposed the algorithm is robust and there are no spikes in the line current. The active filter operates effectively in the presence of unbalanced and distorted ac mains.

S.K Jain, Pramod Agarwal and H.O Gupta[11] proposed a Fuzzy logic controlled shunt active power filter for power quality improvement. The compensation process is based on

only one reverse blocking power semiconductor conducts at any time. A sliding mode control of the 3-phase input currents using a space vector *a.* current modulator, capable of fast and robust current control, is also proposed. Using this control method, the converter presents high power factor and draws near sinusoidal input currents. A Proportional Integral (PI) controller is adopted to regulate the output voltage of the converter. This external voltage controller modulates the amplitudes of the current references, which are sinusoidal.

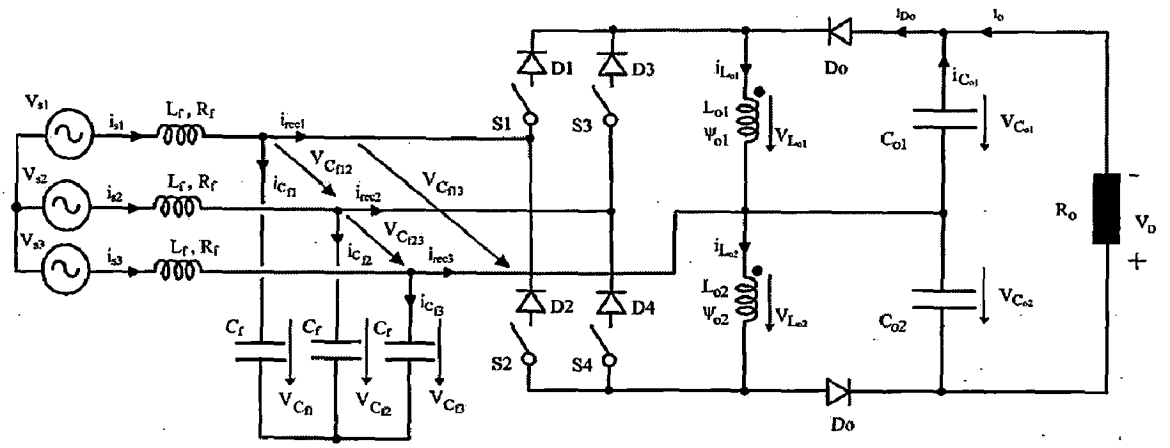


FIG 1.11 THREE PHASE FOUR SWITCH STEP-UP/DOWN RECTIFIER

1.5 STATEMENT OF PROBLEM

A particular reduced switch count topology shown in Fig. 1.10 is considered.

- A three phase power factor corrected Active rectifier which draws unity power factor sinusoidal currents and which develops the desired output DC voltage with only four active switches is to be modeled, simulated and experimentally verified.

In the present work, detailed power circuit analysis was done for the undertaken topology. The design considerations and the applicability range of the rectifier were detailed. Four control strategies(reduced hysteresis, space vector modulation, direct power modulation, Fuzzy space vector modulation) were proposed and verified and compared through simulations. The application of the considered four switch three phase topology to the improvement of power quality was investigated. It is proposed that the considered rectifier can also be used for harmonic current filtering. The feasibility is

are briefly stated followed by the introduction of Shunt and series active power filters as viable power conditioners for mitigating power quality problems. Low cost three-phase active filters based on a PWM voltage structure with a reduced number of switches are proposed.

Chapter 6: Simulation models are developed using MATLAB/SIMULINK. Elaborate simulation study was done to check the validity of the control strategies proposed in chapter 3. The three control strategies were compared and It is found that the performance of Space vector modulated technique and direct power modulated technique are far superior than the reduced hysteresis scheme. SIMULINK models are also developed for the proposed fuzzy controlled active rectifier, reduced switch shunt active filter and reduced switch count series filter and their validity is verified.

Chapter 7: The second part of the thesis is the experimental validation of simulated system or proposed scheme. The hardware circuits which are developed are presented. The fabrication of control circuit and power circuit is briefly discussed.

Chapter 8: The recorded experimental results are displayed in this chapter.

Chapter 9: Conclusion is drawn from the work done and presented. Future scope for improvements in the same field to improve the performance is presented to carry out in upcoming projects.

CHAPTER-2

FOUR SWITCH THREE PHASE ACTIVE RECTIFIER: ANALYSIS, MODELING AND DESIGN

2.1 POWER CIRCUIT DESCRIPTION

The main circuit of the proposed reversible four switch three-phase switching mode rectifier (SMR) with sinusoidal input current and regulated DC output voltage is shown in Fig 2.1. Fig 2.1 shows that the proposed rectifier consists of four switches together with two output Capacitors in series (C1 = C2) and a three-phase boost-type coupling inductor to decrease the volume, weight and size of the SMR. In order to reduce the total harmonic distortion of the input line current, a filter inductor is used on the ac side. The dc load is assumed to have resistance r_0, The power circuit is rather simple which renders the rectifier more reliable and more efficient. Because the three-phase system is balanced, it is only necessary to control two phases: the current in the third phase is controlled automatically.

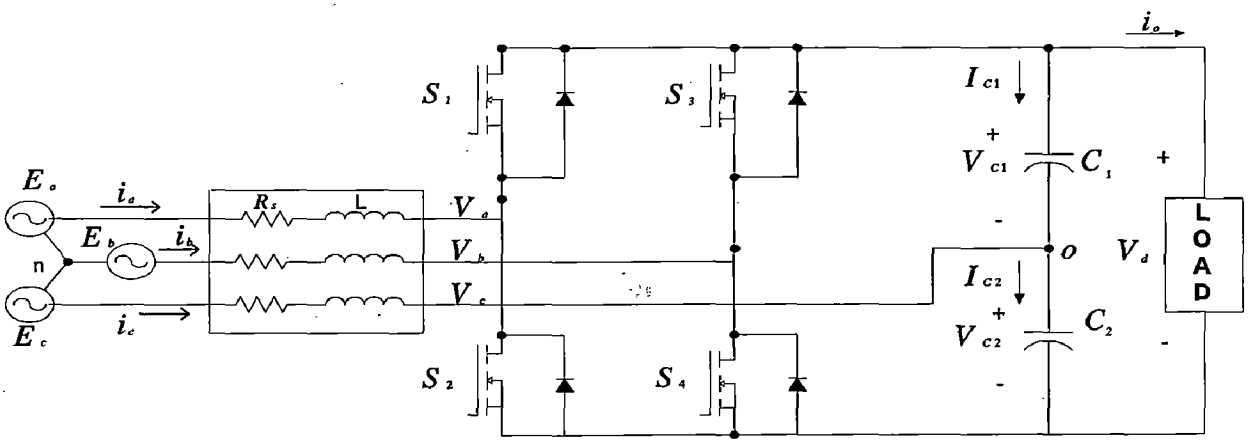


FIG 2.1 REVERSIBLE FOUR SWITCH THREE PHASE ACTIVE RECTIFIER

2.2 POWER CIRCUIT ANALYSIS

Kevork Haddad and Geza Joos[9] presented the power circuit analysis for Four switch Three-phase topology. For analysis, the following assumptions are made:

(i) the dc bus voltage V_{c1} , V_{c2} , are pure dc and balanced

(V_{c1}+ V_{c2}= V_d/2).

(ii) the converter switching elements are ideal.

and k represents the switching modes of the rectifier as given in Table 2.1.

TABLE 2.1

S_a	S_b	mode k	$S_{wa}(k)$	$S_{wb}(k)$	$S_{wc}(k)$
0	0	1	-1/3	-1/3	2/3
1	0	2	1	-1	0
1	1	3	1/3	1/3	-2/3
0	1	4	-1	1	0

Further, from Fig 2.1 one can derive

$$V_{an}=E_a+L\frac{di_a}{dt} \tag{9}$$

$$V_{,bn}=E_b+L\frac{di_b}{dt} \tag{10}$$

$$V_{,cn}=E_c+L\frac{di_c}{dt} \tag{11}$$

To facilitate the analysis, the phase variables are transformed into d-q plane. The transformation is defined as:

$$\mathbf{I}_{ref}=\begin{bmatrix} i_d^* \\ i_q^* \end{bmatrix}=\mathbf{T}\begin{bmatrix} i^*_a \\ i^*_b \\ i^*_c \end{bmatrix} \text{ and } \mathbf{I}=\begin{bmatrix} i_d \\ i_q \end{bmatrix}=\mathbf{T}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{12}$$

where

$$\mathbf{T}=\sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{13}$$

$$\mathbf{V}_a(k)=\mathbf{E}+L\frac{d}{dt}\mathbf{I} \tag{14}$$

where $$\mathbf{E}=\begin{bmatrix} E_d \\ E_q \end{bmatrix}=\mathbf{T}\begin{bmatrix} E_a \\ E_b \\ E_c \end{bmatrix} \text{ and}$$

$$V_d > V_{d,\min} = 2\sqrt{3}\left(\hat{E} + L\left|\frac{di^*}{dt}\right|_{\max}\right) \tag{17}$$

where $\hat{E}$ is the peak phase voltage of the supply.

2.3 DESIGN OF FOUR SWITCH THREE PHASE RECTIFIER

From Fig. 2.1, one can see that the design of the power stage mainly involves determining the values of L and $C = C_1 = C_2$. Hence, in this section the critical condition of the inductance value needed for successful current tracking of the reference current command is derived (Ref[2]) and an analytic design method is presented to find the value of the output capacitor. For simplicity, the series resistance R_s of inductance L is neglected and it is assumed that $V_{c1} = V_{c2} = V_d/2$.

2.3.1. Critical Inductance Condition

From the above geometrical interpretation, one can find that the critical condition occurs only when the circle is tangent to the parallelogram. Hence, one has the following inequality:

$$(wL)^2 < \frac{\left(\frac{V_d^2}{12} - E_m^2\right)}{I_m^2} \tag{18}$$

where V_d is the output dc voltage, E_m and I_m, are the peak source phase voltage and peak source line current, respectively. For design purposes, the inductance value should be based on the worst case. This is obtained by setting the output power equal to the input power so that I_m can be expressed in terms of E_m and P_{om} . This allows us to arrange the above equation in the following form

$$L < \frac{3E_m}{2wP_{om}}\sqrt{\frac{V_d^2}{12} - E_m^2} \tag{19}$$

where P_{om} is the maximum output power.

2.3.2. Capacitor Design

The average storage energy of the capacitor can be stated as

$$I_m = \frac{E_m}{wL}\left(\frac{K}{2} - \sin\theta\right) \tag{29}$$

where $K = V_d/E_m$, is the normalized capacitor dc voltage parameter. The maximum active power is

$$P_m = \frac{3E_m^{\ 2}}{2wL}\left(\frac{K}{2} - \sin\theta\right)\cos\theta \tag{30}$$

The normalized value of the maximum active power is

$$P_{mn} = \frac{P_m}{\frac{3E_m^{\ 2}}{2wL}} = \left(\frac{K}{2} - \sin\theta\right)\cos\theta \tag{31}$$

2.4 COMPARISON WITH SIX SWITCH TOPOLOGY

The reduced switch count inverter and the conventional three phase inverter each impose different type of stress on the active and the passive components.

2.4.1. Dc Bus Voltage

For three phase inverter the condition to track the reference current is given by [15]:

$$V_d > V_{d,\min} = 2\sqrt{3}\left(\hat{E} + L\left|\frac{di^*}{dt}\right|_{\max}\right) \tag{32}$$

Comparing (17) and (32) we obtain

$$\frac{(V_d)_{FourSwitch}}{(V_d)_{SixSwitch}} = 2 \tag{33}$$

Equation (33) shows that the proposed topology requires switches with blocking capability twice as high when compared to the six switch topology.

2.4.2. Three Phase Inductor

The peak to peak ripple, ΔI, generated by the six switch topology is expressed by [16]:

$$\Delta i = \frac{(V_d)_{SixSwitch}}{6L\ f_{sw}} \tag{34}$$

Where f_{sw} is the switching frequency.

It can be shown that the worst case peak to peak ripple for the reduced switch count topology is given by

and S_b^-) in Fig 2.1. For convenient simulation using common software tools available for PC's, one can define the currents i_1 , i_2 and i_3 and voltages V_{an} , V_{bn} , V_{cn} as shown in Fig. 2.1 as well as the following switching functions:

$S_a(t)$= +1 if S_a^+ is off and S_a^- is on.

= -1 if S_a^+ is on and S_a^- is off.

$S_b(t)$= +1 if S_b^+ is off and S_b^- is on.

= -1 if S_b^+ is on and S_b^- is off.

From Fig.2.1 it is quite straight forward to find the following state equations and the output equations

$$\frac{d}{dt}\begin{bmatrix} v_{c1} \\ v_{c2} \\ i_a \\ i_b \end{bmatrix} = \begin{bmatrix} -\frac{1}{R_0 C} & -\frac{1}{R_0 C} & a_{13} & a_{14} \\ -\frac{1}{R_0 C} & -\frac{1}{R_0 C} & a_{23} & a_{24} \\ a_{31} & a_{32} & -\frac{r}{L} & 0 \\ a_{41} & a_{42} & 0 & -\frac{r}{L} \end{bmatrix} \begin{bmatrix} v_{c1} \\ v_{c2} \\ i_a \\ i_b \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \end{bmatrix}$$

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{1}{6}\begin{bmatrix} 1+2S_a(t)-S_b(t) & -1+2S_a(t)-S_b(t) \\ 1-S_a(t)+2S_b(t) & -1-S_a(t)+2S_b(t) \\ -2-S_a(t)-S_b(t) & 2-S_a(t)-S_b(t) \end{bmatrix} \begin{bmatrix} V_{c1} \\ V_{c2} \end{bmatrix}$$

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \frac{1}{2}\begin{bmatrix} 1+S_a(t) & 1+S_b(t) \\ -2 & -2 \\ 1-S_a(t) & 1-S_b(t) \end{bmatrix} \begin{bmatrix} i_a \\ i_b \end{bmatrix}$$

where

$$a_{13}=\frac{1}{2C}[S_a(t)+1]$$

2.6 CONCLUSIONS

- A minimum DC output voltage condition for successful current tracking for a given boost inductor value is derived (eqn.17).
- A critical Inductance condition for successful current tracking is derived (eqn.18) for a given maximum output power.
- A design criteria for capacitance value is derived (eqn.26) in terms of ΔP_{max}, the maximum expected variation of the output power, and T_r is the response time of the voltage control loop.
- Comparisons were made between six switch topology and four switch case in terms of capacitor values, inductor values and switching losses.
- An accurate simulation model for convenient simulation using common PC software tools is given.

CHAPTER-3

CONTROL STRATEGIES

This chapter mainly focuses on the control techniques of Four switch Three-Phase active rectifier. The traditional controls (Hysteresis,Closed form PWM duty cycle control) are briefly discussed. Three High performance control strategies Reduced hysteresis control, Space vector modulated control, Direct Power modulated control of the reduced switch Interface are then presented. The basic theory and implementation of the control strategies are explained.

3.1 INTRODUCTION

Fig 3.1 shows the general control block diagram of the four switch three phase active rectifier. The PI controller controls the sum of capacitor voltage, the overall dc link voltage. For unity power factor operation the controller output I_{mag} is multiplied by the ac main phase voltage templates to generate the input current references. Because the input references are in phase with the input phase voltages, the PI controller output is, in effect, the magnitude of power component of current, the required power by the capacitors to maintain the dc link voltage constant. Reactive current components can be added to the current references to control input power factor.

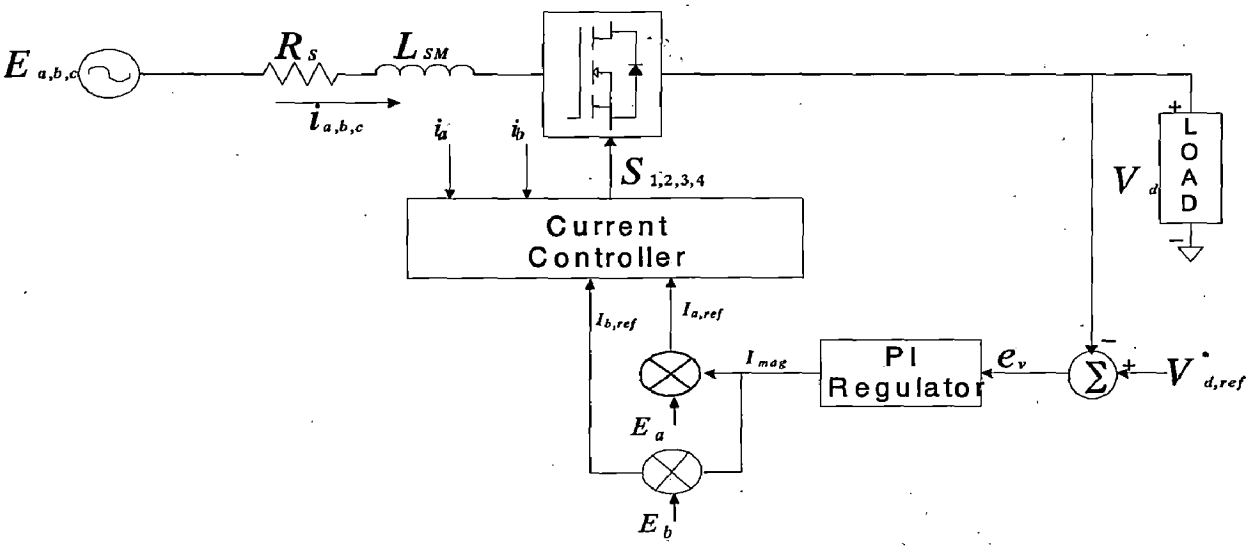


FIG 3.1 GENERAL CONTROL BLOCK DIAGRAM

are then forced to follow the respective reference current signals by two hysteretic current controllers. As far as the rectifier objective is concerned, it is the output dc voltage which has to be controlled. Hence, the second loop is the voltage control loop. By comparing the output voltage signal V_o with the reference signal V_o^*; one can obtain the error signal. A voltage controller, such as the simple proportional-integral (PI) controller G_C in Fig 3.2, is used to shape the system dynamic response characteristics. Naturally, in a practical implementation, a limiter must be imposed to obtain a reasonable output. This output is then used in the current loop to control the magnitude of the current-command signals.

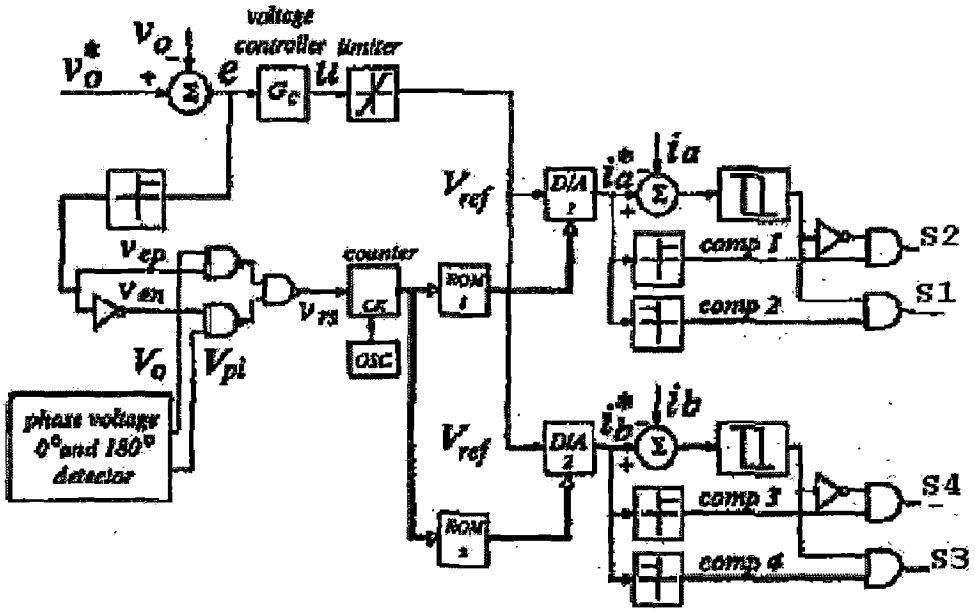


FIG 3.2 BLOCK DIAGRAM OF HYSTERESIS CONTROL

3.2.2 Closed-form PWM duty cycle Control

A closed form PWM duty cycle control law is derived. The input line current is forced to be sinusoidal by following the derived equations. Also, by closed-loop implementation, I_m^* can be controlled automatically and indirectly without using any current sensor. Fig. 3.3 shows the schematic diagram of the control function.

Derivation of closed form PWM duty cycle control law

A typical gating signal and ideal three-phase input current waveforms are shown in Figs 3.4 and 3.5, respectively. Figs 3.6 and 3.7 show the resulting equivalent circuit during time intervals A and B in Fig. 3.5 for one switching cycle t_o -t_4.

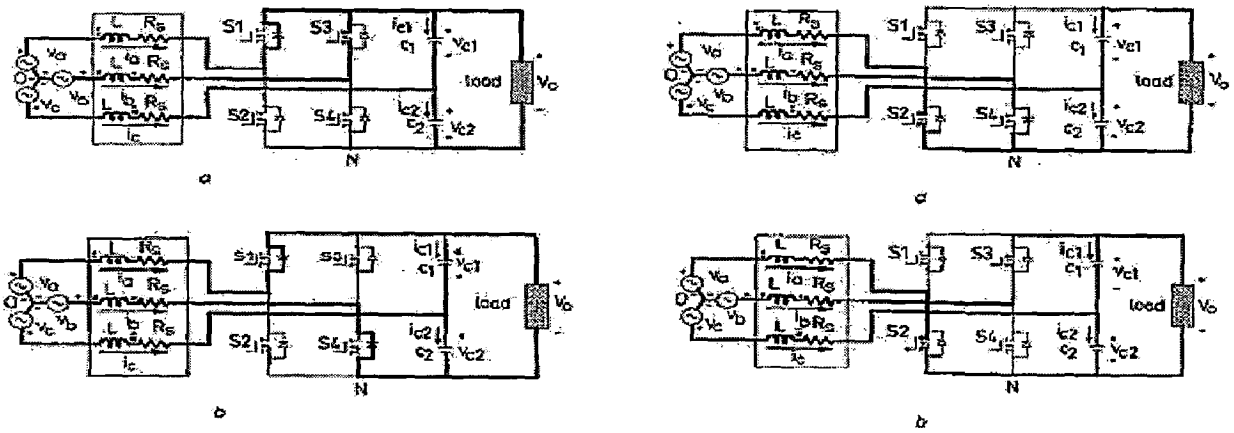


FIG 3.6
FIG 3.7
} EQUIVALENT CIRCUITS FOR SECTION A AND B OF FIG 3.5

$$\begin{bmatrix} L+2L_m & 0 & 0 & 0 & 0 \\ 0 & L+2L_m & 0 & 0 & 0 \\ 0 & 0 & L+2L_m & 0 & 0 \\ 0 & 0 & 0 & C & 0 \\ 0 & 0 & 0 & 0 & C \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \\ v_{c1} \\ v_{c2} \end{bmatrix}$$

$$= \begin{bmatrix} -R_s & 0 & 0 & -d_a & -d_a \\ 0 & -R_s & 0 & -d_b & -d_b \\ 0 & 0 & -R_s & 0 & 1 \\ d_a & d_b & 0 & -\frac{1}{R} & -\frac{1}{R} \\ d_a-1 & d_b-1 & 0 & -\frac{1}{R} & -\frac{1}{R} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \\ v_{c1} \\ v_{c2} \end{bmatrix}$$

$$+ \begin{bmatrix} v_a \\ v_b \\ v_c \\ 0 \\ 0 \end{bmatrix} - \begin{bmatrix} 1 \\ 1 \\ 1 \\ 0 \\ 0 \end{bmatrix} v_{NO}$$

Where d_a, and d_b are duty ratios of switch S1, and S3, respectively.

Assuming that the three-phase source is balanced, i.e.

$v_a + v_b + v_c = 0$ $\qquad$ $i_a + i_b + i_c = 0$

decrease. The maximum ripple of i_c could happen under this condition. In other conducting path (say 2), i_a increases and i_b decreases. Therefore, i_c could increase or decrease. However, $|i_c|$ must be smaller than the maximum of $|i_a|$ and $|i_b|$. Originally, it needs four control inputs (two for determining the section number and two for indicating the polarities of . i_a and . i_b) to choose from 16 combinations of switching states, as shown in Table 3.2, where "1" represents turned-on, "0" represents turned-off, and "x" means "do not care." When the state of a switch is "do not care," the current is actually carried by its paralleled reverse diode. However, the switch can still be turned on without affecting the circuit operations. If we replace "x" in Table 3.2 with "1," the dimension of the lookup table can be greatly reduced. For example, in case i_a and i_b are to be increased, we can always select the switching state as (0 1 0 1). There is no need to detect the section number. Therefore, only two control inputs are required to choose from four switching states. Fig. 3.8 shows the schematic diagram of the proposed system, in which d_a and d_b are the outputs of the hysteresis comparators. For example, if both i_a and i_b are to be decreased, then (d_a d_b) will be (0 0). Thus, *S2* and *S4* should be turned on according to Table 3.2 .The current commands i_{aref} and i_{bref} are sinusoidal and in phase with the respective source voltages. Their magnitudes are determined by the feedback dc output voltage V_d.

TABLE 3.1

Conducting Path	Conducting Switches	V_a	V_b	V_c	Δi_a	Δi_b	Δi_c
1	S2(D2),S4(D4)	$-V_d/3$	$-V_d/3$	$2V_d/3$	+	+	-
2	S2(D2),S3(D3)	$-V_d$	V_d	0	+	-	$\|. i_c\|<\max\{\|. i_a\|,\|. i_b\|\}$
3	S1(D1),S4(D4)	V_d	$-V_d$	0	-	+	$\|. i_c\|<\max\{\|. i_a\|,\|. i_b\|\}$
4	S1(D1),S3(D3)	$V_d/3$	$V_d/3$	$-2V_d/3$	-	-	+

TABLE 3.2

Section/Δi_a,Δi_b	++	+-	-+	--
I(E_a>0,E_b<0)	(0 1 0 x)	(0 1 1 0)	(x 0 0 x)	(x 0 1 0)
II(E_a>0,E_b>0)	(0 1 0 1)	(0 1 x 0)	(x 0 0 1)	(x 0 x 0)
III(E_a<0,E_b>0)	(0 x 0 1)	(0 x x 0)	(1 0 0 1)	(1 0 x 0)
IV(E_a<0, E_b<0)	(0 x 0 x)	(0 x 1 0)	(1 0 0 x)	(1 0 1 0)
2π period	(0 1 0 1)	(0 1 1 0)	(1 0 0 1)	(1 0 1 0)

increase in switching frequency. If surplus modulation time is shared between, (V_3, V_4) then V_c has more ripple and hence i_c ripple increases causing increased voltage imbalance across two capacitors.

TABLE 3.3
SPACE VECTORS FOR DIFFERENT COMBINATIONS

	Active switches	V_a	V_b	V_c	Space Vector (V)
11 (C_1)	S_1S_3	$\frac{V_d}{6}$	$\frac{V_d}{6}$	$\frac{-V_d}{3}$	$\frac{V_d}{6}(1+j\sqrt{3})$ (V_1)
00 (C_2)	S_2S_4	$\frac{-V_d}{6}$	$\frac{-V_d}{6}$	$\frac{V_d}{3}$	$\frac{-V_d}{6}(1+j\sqrt{3})$ (V_2)
10 (C_3)	S_1S_4	$\frac{V_d}{2}$	$\frac{-V_d}{2}$	0	$\frac{V_d}{6}(3-j\sqrt{3})$ (V_3)
01 (C_4)	S_2S_3	$\frac{-V_d}{2}$	$\frac{V_d}{2}$	0	$-\frac{V_d}{6}(3-\sqrt{3})$ (V_4)

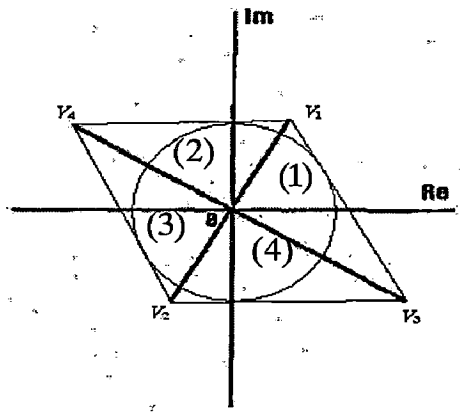


FIG 3.9 SPACE VECTOR DIAGRAM

Hence (V_1,V_2) combination is preferred. If $V_{a,ref}$, $V_{b,ref}$, $V_{c,ref}$ are the desired rectifier input phase voltages to be synthesized, It can be written in space vector notation as

$$V_{ref} = (V_{d,ref}+jV_{q,ref}) = V_{a,ref}+V_{b,ref}e^{j2\pi/3}+V_{c,ref}e^{-j2\pi/3} \qquad (A)$$

The quadrant in which the desired V_{ref} lies can be obtained using Table 3.4.

b. Using eqn. (A) calculate $V_{d,ref}, V_{q,ref}$, From Table 3.4, the quadrant in which V_{ref} is present can be found.

c. The duty ratios d_1, d_2, d_3,d_4 for which the switching states, V_1, V_2, V_3, V_4 are applied is calculated from Table 3.5.

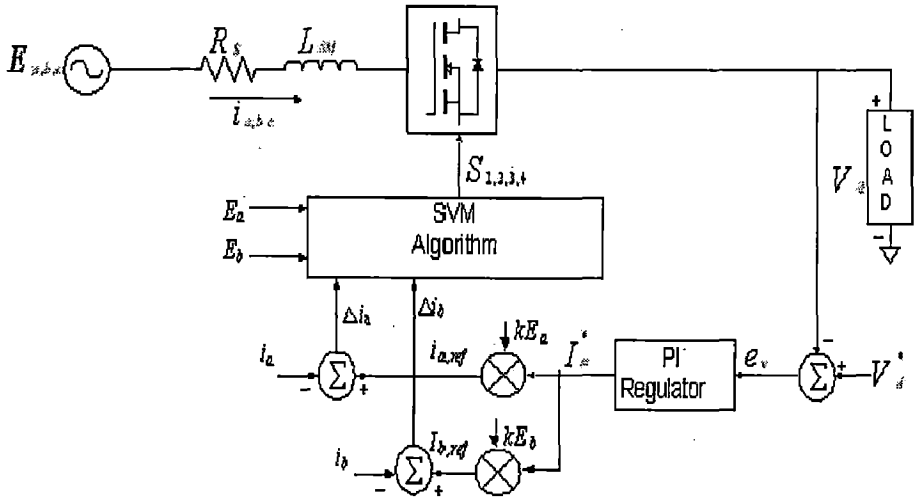


FIG 3.10 COMPLETE BLOCK DIAGRAM OF THE SVM SCHEME

TABLE 3.5

DUTY RATIO CALCULATION

Quadrants	Duty ratios
2,3	$d_1 = \frac{1}{2} + \frac{V_{a,ref} - V_{c,ref}}{V_d}$ $d_2 = \frac{1}{2} + \frac{V_{c,ref} - V_{b,ref}}{V_d}$ $d_4 = \frac{V_{b,ref} - V_{a,ref}}{V_d}$
1,4	$d_1 = \frac{1}{2} + \frac{V_{b,ref} - V_{c,ref}}{V_d}$ $d_2 = \frac{1}{2} + \frac{V_{c,ref} - V_{a,ref}}{V_d}$ $d_3 = \frac{V_{a,ref} - V_{b,ref}}{V_d}$

b. The following equations are to be solved to obtain d_1,d_2,d_3 .

$$p_{ref}=p_1d_1+p_2d_2+p_3d_3$$

$$q_{ref}=q_1d_1+q_2d_2+q_3d_3$$

$$d_1+d_2+d_3=1$$

where p_{ref}, q_{ref} are reference instantaneous active and reactive powers.

c. If $d_1>0$,$d_2>0$ and $d_3>0$,then the duty ratios for which switching states C_1,C_2,C_3 are to be applied are obtained. Else replace p_3,q_3d_3 by p_4,q_4,d_4 respectively, in the above equations and solve them to obtain d_1,d_2,d_4. The obtained duty ratios are the duty ratios for which C_1,C_2,C_4 are to be applied with in a sampling period.

The complete control block diagram for DPM bidirectional interface is shown in Fig 3.11 The active power reference(p_{ref}) is set by dc-link voltage controller while the reactive power reference(q_{ref}) is set to zero for unity power factor.

Suppose instantaneous active and reactive powers that would have developed if C_1 were to be applied for the entire sampling period is to be calculated, the currents at the end of the sampling period are obtained from Table 3.3 as

$$i_{a,n+1}= i_{a,n}+\frac{\Delta T}{L}(E_a-\frac{V_d}{6})$$

$$i_{b,n+1}= i_{b,n}+\frac{\Delta T}{L}(E_b-\frac{V_d}{6})$$

where $(n+1)^{th}$ instant is the instant at the end of sampling period and n^{th} instant is the present instant. The instantaneous active and reactive powers at $(n+1)^{th}$ instant $p_{1,n+1},q_{1,n+1}$ are obtained from

$$p_{1,n+1}=E_{a,n+1}i_{a,n+1}+E_{b,n+1}i_{b,n+1}+E_{c,n+1}i_{c,n+1}$$

$$q_{1,n+1}=\frac{1}{\sqrt{3}}[(E_{b,n+1}-E_{c,n+1})i_{a,n+1}+(E_{c,n+1}-E_{a,n+1})i_{b,n+1}+(E_{a,n+1}-E_{b,n+1})i_{c,n+1}]$$

where $E_{a,n+1}$, $E_{b,n+1}$, $E_{c,n+1}$ are the input phase voltages at $(n+1)^{th}$ instant.

For balanced three phase system

$$E_{c,n+1}= -(E_{a,n+1}+E_{b,n+1})$$

$$i_{c,n+1}= -(i_{a,n+1}+i_{b,n+1})$$

Hence sensing two phase voltages (E_a,E_b) and two line currents (i_a,i_b) is enough. The

CHAPTER-4

FUZZY CONTROL OF FOUR SWITCH THREE PHASE ACTIVE RECTIFIER

This chapter mainly focuses on the application of fuzzy controller to the DC output voltage control loop. The use of fuzzy controller improves the dynamic response of the rectifier. The theoretical aspects and design procedures of fuzzy controllers are briefly discussed followed by the definition of membership functions and Rule base used in the adopted fuzzy controller.

4.1 INTRODUCTION

Since the introduction of the theory of fuzzy sets by L. A. Zadeh in 1965, and the industrial application of the first fuzzy controller by E.H. Mamadani in 1974, fuzzy systems have obtained a major role in engineering systems and consumer's products in 1980s and 1990s. New applications are presented continuously. A reason for this significant role is that fuzzy computing provides a flexible and powerful alternative to contract controllers, supervisory blocks, computing units and compensation systems in different application areas. With fuzzy sets very nonlinear control actions can be formed easily. The transparency of fuzzy rules and the locality of parameters are helpful in the design and maintenances of the systems. Therefore, preliminary results can be obtained within a short development period. However, fuzzy control does have some weaknesses. One is that fuzzy control is still lacking generally accepted theoretical design tools. Although preliminary results are easily obtained, further improvements need a lot of labor especially when the number of inputs increases, the maintenances of the multi-dimensional rule base is time consuming.

Due to continuously developing automation systems and more demanding Control performance requirements, conventional control methods are not always adequate. On the other hand, practical control problems are usually imprecise. The input output relations of the system may be uncertain and they can be changed by unknown external disturbances. New schemes are needed to solve such problems. One such an approach is to utilize fuzzy control.

universe is U= (-5, -4, .. 0, ..., 4, 5). The quantiser rounds to 5 to fit it to the nearest level. Quantisation is a means to reduce data, but if the quantisation is too coarse the controller may oscillate around the reference or even become unstable. When the input to the controller is error, the control strategy is a static mapping between input and control signal. A dynamic controller would have additional inputs, for example derivatives, integrals, or previous values of measurements backwards in time. These are created in the preprocessor thus making the controller multi-dimensional, which requires many rules and makes it more difficult to design. The preprocessor then passes the data on to the controller.

4.2.2 Fuzzification

The first block inside the controller is fuzzification, which converts each piece of input data to degrees of membership by a lookup in one or several membership functions. The fuzzification block thus matches the input data with the conditions of the rules to determine how well the condition of each rule matches that particular input instance. There is a degree of membership for each linguistic term that applies to that input variable

4.2.3 Rule base The rule base is to do with the fuzzy inference rules. The step response of the system can be roughly divided into four areas $A_1 \sim A_4$ and two sets of points: cross-over $\{b_1, b_2\}$ and peak-valley $\{c_1, c_2\}$ as shown in Fig.4.2. The system equilibrium point is the origin of the phase plane

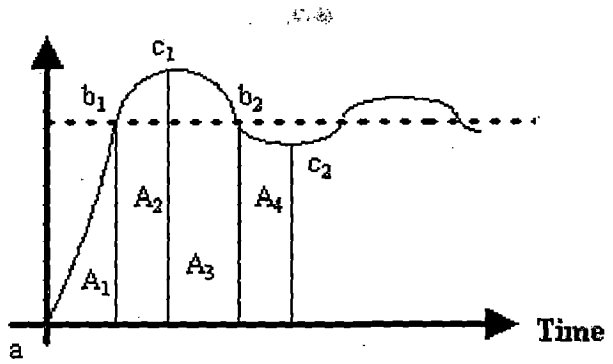


FIG 4.2 GENERAL STEP RESPONSE

a) The sign of rules: The sign of the rule base can be determined by following meta-rules

Activation: The activation of a rule is the deduction of the conclusion, possibly reduced by its firing strength. Thickened lines in the third column indicate the firing strength of each rule. Only the thickened part of the singletons are activated, and **min** or product (*) is used as the activation operator. It makes no difference in this case, since the output membership functions are singletons, but in the general case of s- , . - and z- functions in the third column, the multiplication scales the membership curves, thus preserving the initial shape, rather than clipping them as the **min** operation does. Both methods work well in general, although the multiplication results in a slightly smoother control signal. In Fig. 4.3, only rules four and five are active.

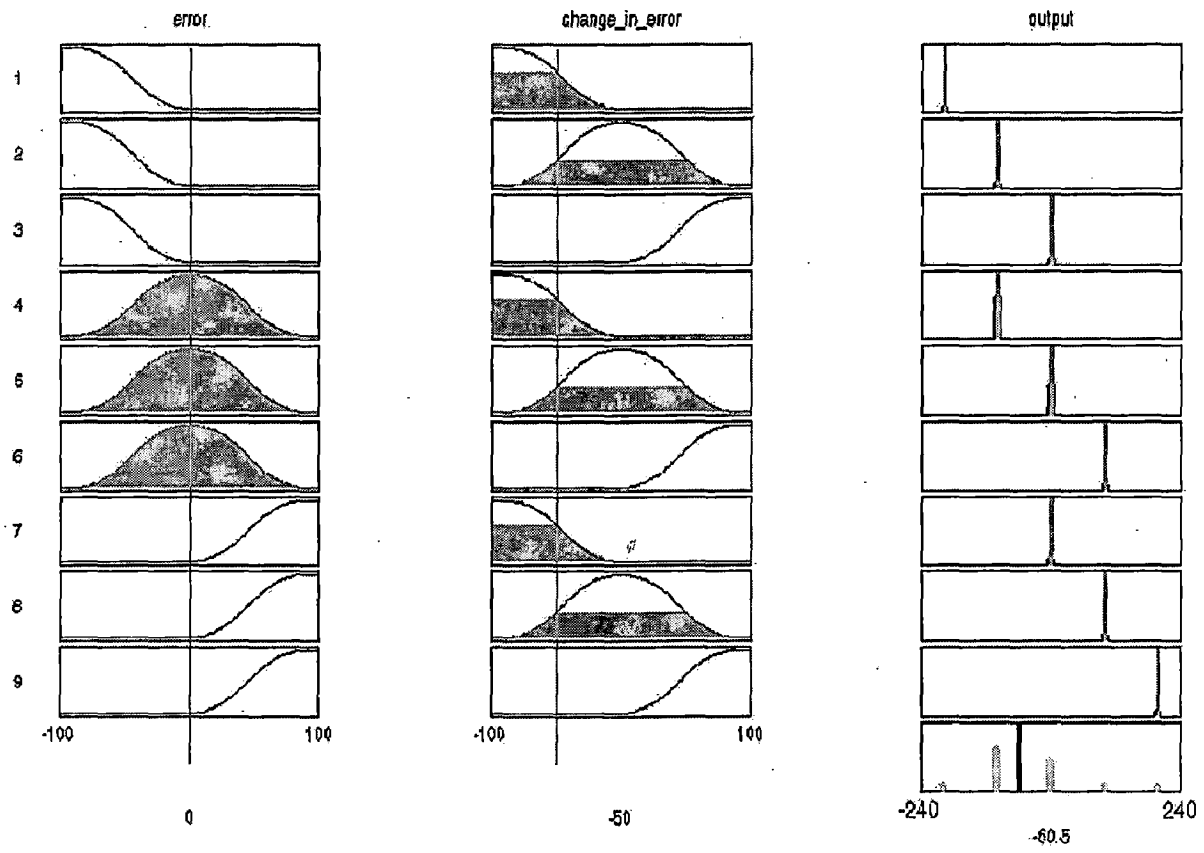


FIG 4.3 GRAPHICAL CONSTRUCTION OF THE CONTROL SIGNAL IN A FUZZY PD CONTROLLER (GENERATED IN THE MATLAB FUZZY LOGIC TOOLBOX).

The alphas are the firing strengths from the k rules and s1 ... sn are the output singletons. Since this can be computed as a vector product, this type of inference is relatively fast in a matrix oriented language. There could actually have been several conclusion sets. An example of a one-input two- outputs rule is "If e_a is **a** then o_1 is **x** and o_2 is **y**'. The inference engine can treat two (or several) columns on the conclusion side in parallel by applying the firing strength to both conclusion sets. In practice, one would often implement this situation as two rules rather than one, that is, "If e_a is **a** then o_1 is **x**", "If ea is **a** then o_2 is **y**".

4.2.5 Defuzzification

The resulting fuzzy set (Fig. 4.3, bottom right; Fig. 4.4, extreme right) must be converted to a number that can be sent to the process as a control signal. This operation is called defuzzification, and in Fig. 4.4 the x-coordinate marked by a white, vertical dividing line becomes the control signal. The resulting fuzzy set is thus defuzzified into a crisp control signal. There are several defuzzification methods.

Centre of gravity (COG): The crisp output value u (white line in Fig. 4.4) is the abscissa under the centre of gravity of the fuzzy set,

$$u = \frac{\sum_i \mu(x_i)\, x_i}{\sum_i \Sigma_i \mu(x_i)}$$

Here x_i is a running point in a discrete universe, and $\mu(x_i)$, is its membership value in the membership function. The expression can be interpreted as the weighted average of the elements in the support set. For the continuous case, replace the summations by integrals. It is a much used method although its computational complexity is relatively high. This method is also called centroid of area.

Centre of gravity method for singleton (COGS): If the membership functions of the conclusions are singletons (Fig.4.3), the output value is

$$u = \frac{\sum_i \mu(s_i)\, s_i}{\sum_i \mu(s_i)}$$

4.3 FUZZY CONTROL OF FOUR SWITCH PFC RECTIFIER

Fig 4.5 shows the schematic control block diagram of Four switch three phase active rectifier with fuzzy output control. In order to implement the control algorithm in closed loop, the DC side capacitor voltage is sensed and then compared with a reference value. The obtained error $e(=V_d^*-V_d)$ and change of error signal $ce(n)=e(n)-e(n-1)$ at the n^{th} sampling instant are used as input to fuzzy processing. The output of fuzzy controller is integrated in discrete time to get the amplitude of current reference I_m^*. This current I_m^* takes care of the active power demand of the load and losses in the system. For unity power factor operation I_m^* is multiplied by input phase voltage templates to get reference instantaneous currents ($i_{a,ref}$, $i_{b,ref}$). Then the reduced hysteresis control or SVM or DPM algorithm discussed in previous chapter can be applied to make the actual current track the references.

The adopted Fuzzy controller has the following characteristics

a. seven sets for each input and output
b. Triangular membership functions for simplicity
c. Fuzzification using continuous universe of discourse
d. Implication using mamdani's min operator
e. Defuzzification using centre of gravity method

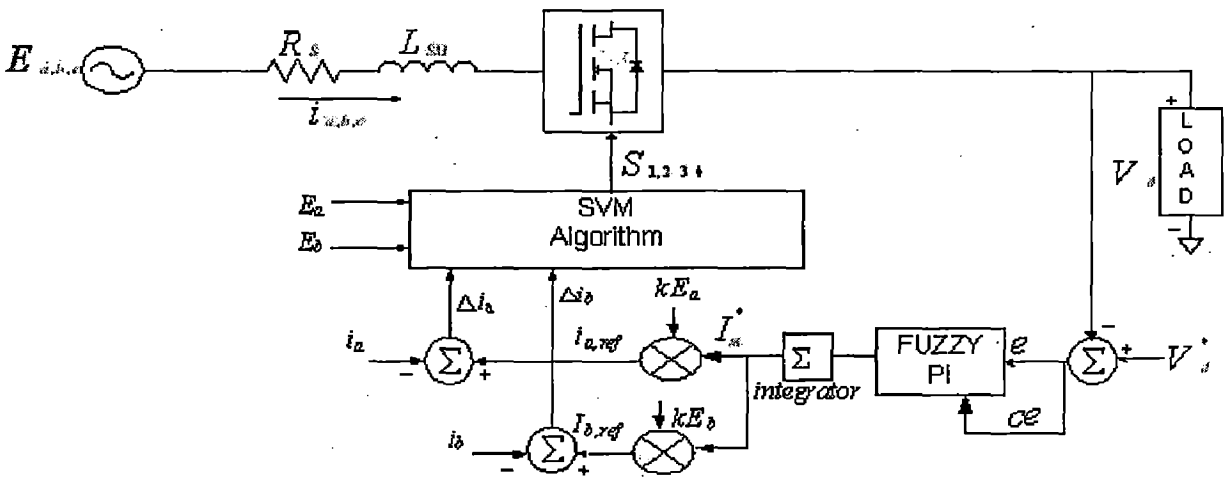


FIG 4.5 BLOCK DIAGRAM OF FUZZY SVM CONTROL

CHAPTER-5

APPLICATION OF FOUR SWITCH THREE-PHASE TOPOLOGY TO POWER QUALITY IMPROVEMENT

The main focus of this chapter is to investigate application of four switch three-phase topology for power quality improvement. The causes of power quality problems are briefly stated followed by the introduction of Shunt and series active power filters as viable power conditioners for mitigating power quality problems. The four-switch three phase topology discussed in the previous chapters can be extended to filter harmonic line currents. The control scheme for such rectifier acting as shunt filter is discussed. A Low cost three-phase series active filter to compensate source voltage unbalances and harmonics is also discussed along with its control strategy.

5.1 POWER QUALITY ISSUES: AN INTRODUCTION

Power quality phenomena include all possible situations in which the waveform of the supply voltage (voltage quality) or load current (current quality) deviate from the sinusoidal waveform at rated frequency with amplitude corresponding to the rated rms value for all three phases of a three-phase system. The wide range of power quality disturbances covers sudden, short duration deviations, e.g. impulsive and oscillatory transients, voltage dips (or sags), short interruptions, as well as steady-state deviations, such as harmonics and flicker. One can also distinguish, based on the cause, between disturbances related to the quality of the supply voltage and those related to the quality of the current taken by the load.

To the first class belong, among others, voltage unbalances, harmonics and interruptions, mostly caused by faults in the power system. The voltage imbalance is usually due to the unbalanced consumption of single-phase loads connected to the distribution network or due to the unbalanced emf of the network itself. The voltage harmonics are mainly caused by nonlinear loads which inject current harmonics through supply impedance or by voltage harmonics present in the mains emf. These disturbances may cause tripping of "sensitive" electronic equipment with disastrous consequences in industrial plants, where tripping of critical equipment can bear the stoppage of the whole

5.2 A FOUR SWITCH THREE-PHASE ACTIVE RECTIFIER WITH THE FUNCTION OF A SHUNT ACTIVE POWER FILTER

A number of topologies have been proposed in the literature for shunt active power filters based on voltage source structures. The most common is the conventional six-switch structure, as in Fig. 5.2. However, these filters become costly at increased power levels. The growing interest in low cost active filters has led researchers to investigate hybrid active filters. By combining passive and active filters, the rating of the active filter is reduced, hence the cost. This section present a cost effective reduced switch count PWM rectifier based active filter Fig. 5.3. Most of the compensation schemes for active filters are based on sensing harmonics and reactive volt-ampere requirements of the nonlinear load, and require complex control. Duke and Round [17] have proposed a scheme in which the required compensating current is determined using a simple synthetic sinusoid generation technique by sensing the load current. This scheme is further modified by sensing line currents only, which is simple and easy to implement. The three phase currents/voltages are detected using only two current/voltage sensors. The DC capacitor voltage is regulated to estimate the reference current template. Fig. 5.3 shows the configuration of a four switch three phase active rectifier with active line current filtering capability. The main advantages of the proposed active filter are:

(i) reduced number of switches and lower cost

(ii) lower overall converter and switch ratings and higher efficiency

(iii) increased reliability

(iv) simple power structure

(v) reduced number of current sensors.

A PWM rectifier is used here for active power filtering purpose. The active power filter and PWM rectifier have basically the same circuit configuration and can operate based on the same control principle. Therefore, a power converter capable of both the active filter operation and PWM rectifier operation at the same time can be designed. Such a converter operates as a PWM rectifier to supply DC power to its own load and, at the same time, operates as an active filter to supply to the AC line a compensating current equal to the harmonic current produced by the nonlinear load connected to the same AC line.

5.2.1 Compensation Principle

The active filter is controlled to draw/supply a compensating current i_{af} from/to the utility, so that it cancels current harmonics on the AC side, and makes the source current in phase with the source voltage. Fig. 5.4 shows the different waveforms. Curve 'A' shows the load current waveform and curve 'B' shows the desired source current. Curve 'C' shows the compensating current injected by the active power filter containing all the harmonics, to make the source current sinusoidal.

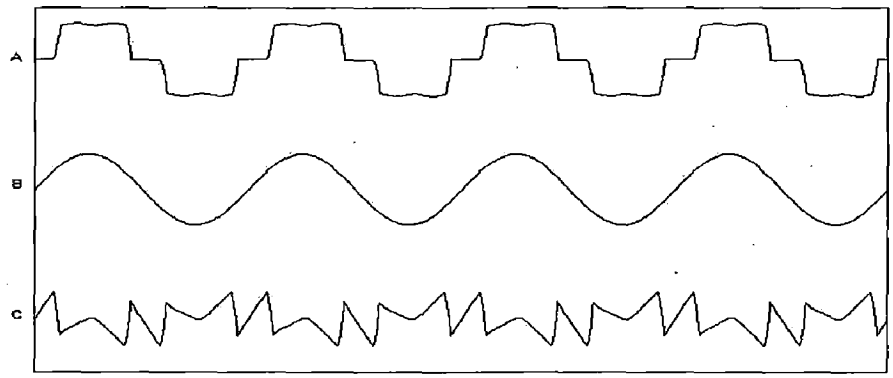


Fig 5.4:A NON LINEAR LOAD CURRENT
B DESIRED SOURCE CURRENT
C HARMONIC CONTENT IN LOAD CURRENT

5.2.2 The Control Scheme

Ref [18, 19] proposed a indirect estimation for harmonic and reactive power compensation. This technique has brought a revolution in the control technique. It can be easily implemented using simple and less analog circuits. The voltage and current sensors can also be reduced making the control circuitry simple.

Role of DC link capacitors serves important role in this technique. They maintain a DC voltage with small ripples in steady state and serves as an energy storage element to supply real power difference between load and source during transients. In steady state the real power supplied by the source should be equal to the real power demand of the load plus some small power to compensate the losses in the active filter. Thus DC link voltage can be maintained at a reference value. However, when the load condition changes the real power balance between the mains and the load will be disturbed. This

From (4) , the real (fundamental) power drawn by the load is

$$p_f(t)= V_m I_1 \sin^2 \omega t * \cos \phi_1 = v_s(t)* i_s(t) \qquad (6)$$

From (6) , the source current supplied by the source , after compensation is

$$i_s(t)= p_f(t)/ v_s(t)= I_1 \cos \phi_1 \text{ sin. } t = I_{sm} \sin \omega t$$

where $I_{sm} = I_1 \cos \phi_1$.

There are also some switching losses in the PWM converter, and hence utility must supply a small overhead for capacitor leakage and converter switching losses in addition to the real power of the load. The total peak current supplied by the source is therefore

$$I_{sp}= I_{sm}+ I_{sl} \qquad (7)$$

If the active filter provides the total reactive and harmonic power, then $i_s(t)$ will be in phase with the utility voltage and purely sinusoidal. At this time, the active filter must provide the following compensation current:

$$I_{af}(t)= i_{load}(t)- i_s(t)$$

hence for accurate and instantaneous compensation of reactive and harmonic power it is necessary to estimate $i_s(t)$,i.e. the fundamental component of the load current as the reference current.

The peak value of reference current I_{sp} can be estimated by controlling the DC capacitor voltage. Ideal compensation requires the main current to be sinusoidal and in phase with the source voltage, irrespective of the load current nature. The desired source currents after compensation can be given as

$$i_{sa}^* = I_{sp} \sin \omega t$$
$$i_{sb}^* = I_{sp} \sin (\omega t - 120^0)$$
$$i_{sc}^* = I_{sp} \sin (\omega t + 120^0)$$

where I_{sp} ($=I_1 \cos \phi_1 + I_{sl}$) is the amplitude of the desired source current, while the phase angle can be obtained from the source voltages. Hence the waveform and phases of the source currents are known, and only the magnitudes of the source currents need to be determined.

This peak value of reference current has been estimated by regulating the DC side capacitor voltage of the PWM converter. This capacitor voltage is compared with a reference value and the error is processed in a PI controller. The output of the PI controller has been considered as the amplitude of the desired source current, and the

5.3 A SERIES ACTIVE POWER FILTER BASED ON A FOUR SWITCH THREE-PHASE TOPOLOGY

Series active filters are introduced in 1980's and are intended to mainly operated as voltage regulators and thus to compensate voltage unbalances, harmonics, voltage sags and swells. The basic configuration of series active filter is shown in Fig. 5.7. Several structures have been considered for the implementation of series active filters and the topology shown in Fig. 5.8 is one of the widely used. Different approaches have been proposed in the power electronic literature to perform the control of such a filters and the PQ theory is the most common. Fig. 5.9 shows the proposed series filter using four switch Three-phase topology. The C-phase is connected to the centre point of DC split capacitor. The proposed filter has all the advantages stated in section 5.2 for shunt filter. However It is to be noted that the proposed topology cannot compensate zero sequence components.

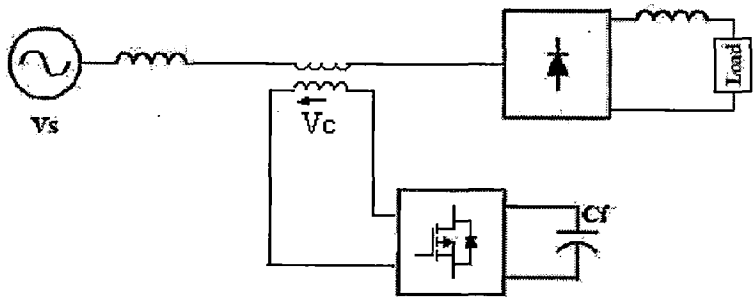


Fig 5.7: CONFIGURATION OF SERIES ACTIVE POWER FILTER

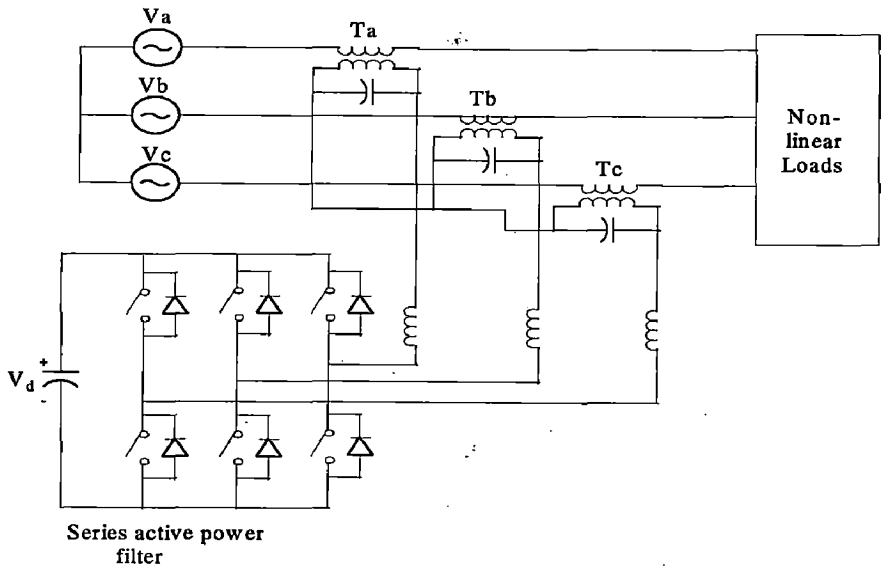


Fig 5.8: SERIES ACTIVE POWER FILTER USING VSI BRIDGE

where V_a, V_b, V_c and $V_{a(+)}$, $V_{b(+)}$, $V_{c(+)}$ are instantaneous source voltages and positive-sequence components, respectively. The j in above equation means the phase shift of 90 which is simply obtained in practical realization by using digital all-pass filters as

$$Y(s) = \frac{s^2 - bs + c}{s^2 + bs + c} X(s)$$

where b=314.16rad/s and c=$\pi/2$. Since the all-pass filter can give a desired phase shift of $\pi/2$ between the input and the output, with the magnitude kept unchanged, it gives better performance than the other methods using low-pass or band pass filters in deriving the positive-sequence voltage component. From the positive-sequence component of $V_{a(+)}$, $V_{b(+)}$ and $V_{c(+)}$ which is a balanced voltage set, the source phase angle is derived, using the d–q transformation, as follows:

$$\theta_e = \tan^{-1} \frac{-V_{ds(+)}}{V_{qs(+)}}$$

Where

$$V_{qs(+)} = \frac{(2V_{a(+)} - V_{b(+)} - V_{c(+)})}{3}$$

$$V_{ds(+)} = \frac{(V_{c(+)} - V_{b(+)})}{\sqrt{3}}$$

The positive sequence voltages $V_{a(+)}$, $V_{b(+)}$ and $V_{c(+)}$ can be transformed into a synchronous reference frame as

$$\begin{bmatrix} V^e_{q(+)} \\ V^e_{d(+)} \end{bmatrix} = \begin{bmatrix} \cos\theta_e & \sin\theta_e \\ -\sin\theta_e & \cos\theta_e \end{bmatrix} \begin{bmatrix} V_{qs(+)} \\ V_{ds(+)} \end{bmatrix}$$

where the superscript "e" means a quantity in a synchronous reference frame. Thus, the required fundamental component set of the balanced source phase voltage can be calculated as

$$\begin{bmatrix} V_{a,bal} \\ V_{b,bal} \\ V_{c,bal} \end{bmatrix} = K_u \begin{bmatrix} V_{a(+)} \\ V_{b(+)} \\ V_{c(+)} \end{bmatrix}$$

where K_u is a gain to recover the required fundamental magnitude of V, which is expressed as

$$K_u = \frac{V}{V^e_{q(+)}}$$

CHAPTER-6

SIMULATION RESULTS

Extensive simulation is carried out to verify the validity of the proposed schemes (Reduced hysteresis, Space Vector modulation, Direct power modulation, Fuzzy Space vector modulation) for the control of Four switch three phase active rectifier. Simulation model of the four switch three phase active rectifier and the control strategies are developed using MATLAB™ and its SIMPOWERSYSTEMS BLOCKSET in SIMULINK. The different components which are used to develop the model are : 3-ph voltage source, Mosfet, Diode, Current Measurement, Voltage Measurement, Capacitor, Inductor, Comparator, Multiplexers/ De-Multiplexers, Scopes. Scopes are used to obtain the nature of the current, voltage of the system at any point. These scopes have the facility of storing data which come from simulation into workspace. Various curves are plotted from scope. These curves can also be plotted from MATLAB command window after storing data variables in workspace from the scope.

The circuit parameters of the adopted Four switch three phase active rectifier(Fig. 2.1) in the simulations are

E_m=50V,$V_{d,ref}$=240V

C_1=C_2=2200μF,R=87.85Ω.

R_s=0.45Ω, L=6.4mH

Input voltage frequency ω=377 rad/sec

Switching frequency for SVM/DPM=3KHz.

6.1 REDUCED HYSTERESIS CONTROL

The control strategy is verified in the following aspects

a. The line current drawn from the AC mains is sinusoidal and is in-phase with the respective phase voltages (High power factor operation).
b. The DC output voltage is maintained at the reference value.
c. The Transient response of the rectifier is satisfactory.
d. The regenerative capability of the interface is maintained.

Fig. 6.4 and Fig. 6.5 illustrates the transient waveforms of the DC link voltage and input current for the step change of the reference voltage of DC link from 220V to 270V. One sees that the magnitude of input current, which is the output of the voltage PI controller, changes according to the step change of the reference voltage and that the DC link voltage follows the voltage command. To show the regenerative capability of the proposed rectifier, the load is assumed to be active and consists of a DC source of 245V and a load of 2 ohms. Due to the higher applied output voltage, the load current is reversed. Fig. 6.6 shows the waveforms of A phase input current and A phase voltage.

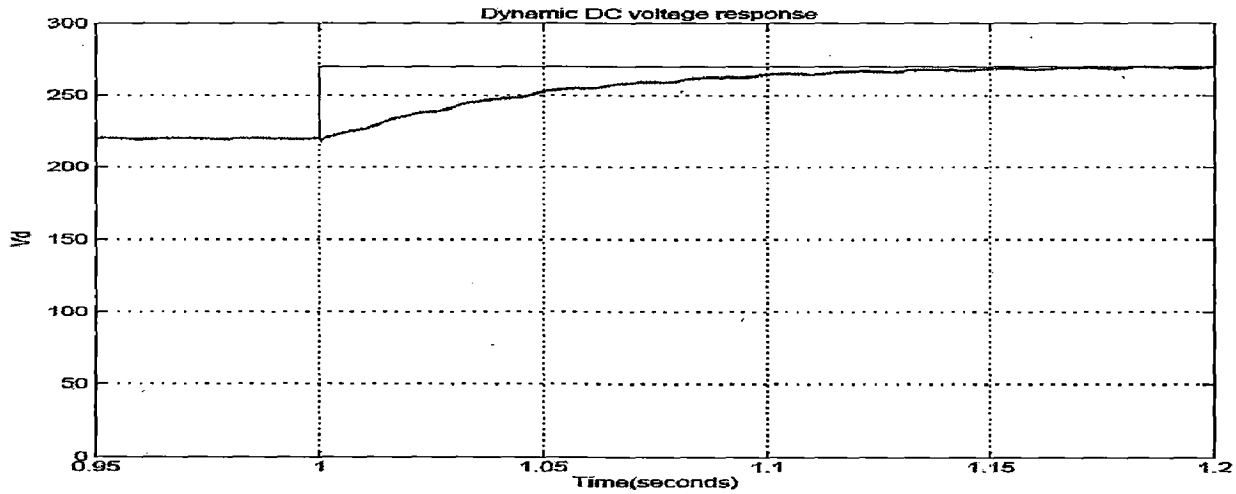


FIG 6.4

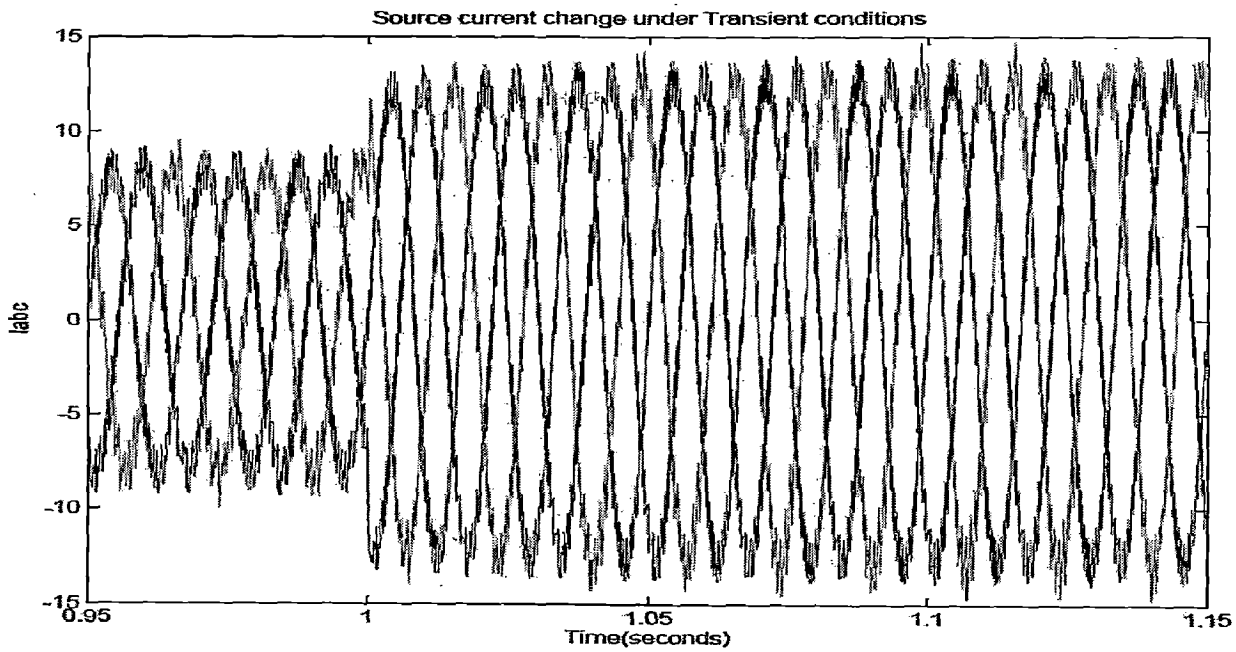


FIG 6.5

6.2 SPACE VECTOR MODULATED CONTROL

The control strategy is verified in the following aspects

a. The line current drawn from the AC mains is sinusoidal and is in-phase with the respective phase voltages (High power factor operation).
b. The DC output voltage is maintained at the reference value.
c. The Transient response of the rectifier is satisfactory.
d. The regenerative capability of the interface is maintained.

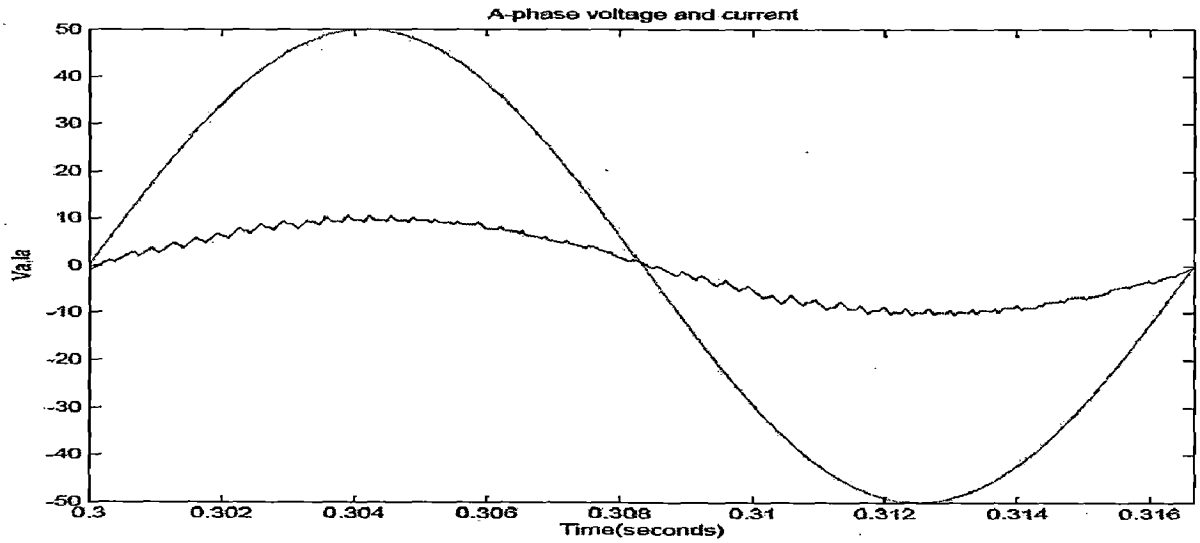


FIG 6.8

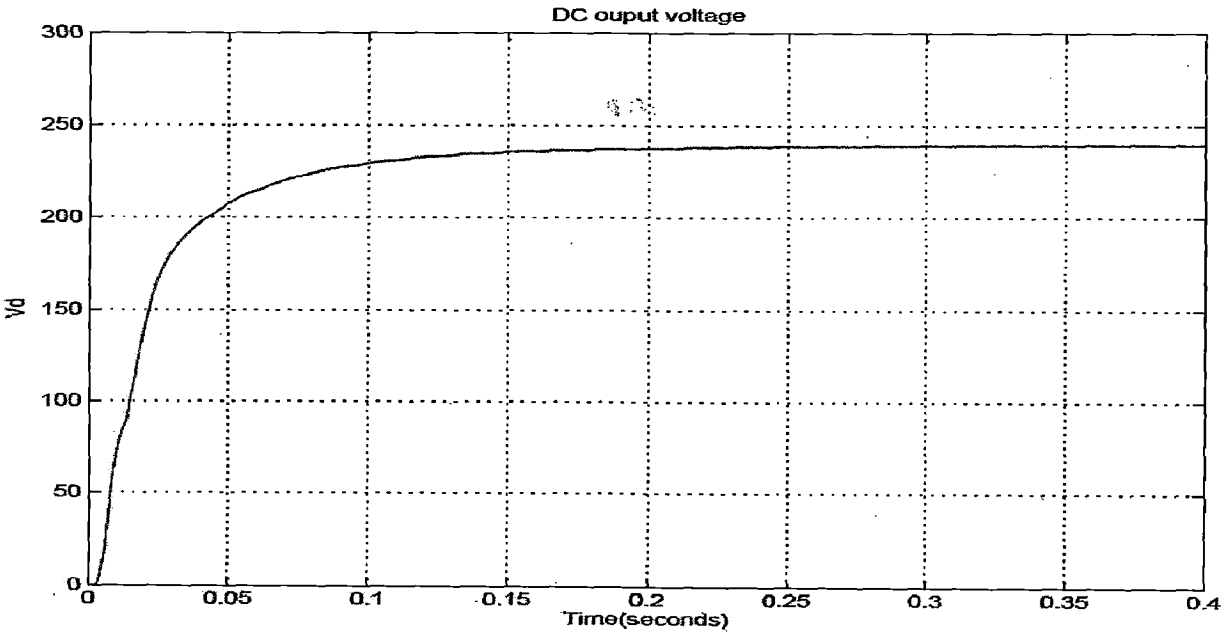


FIG 6.9

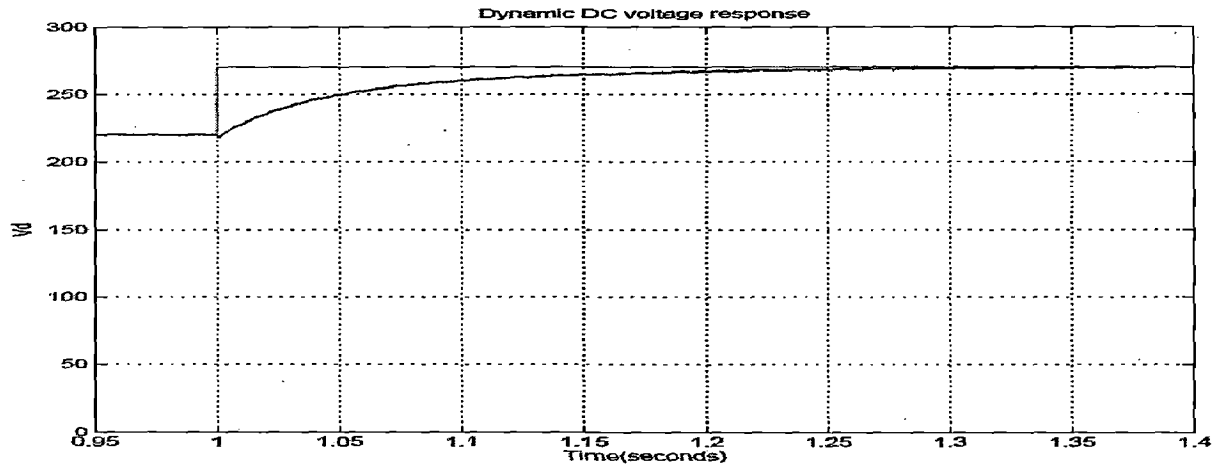


FIG 6.12

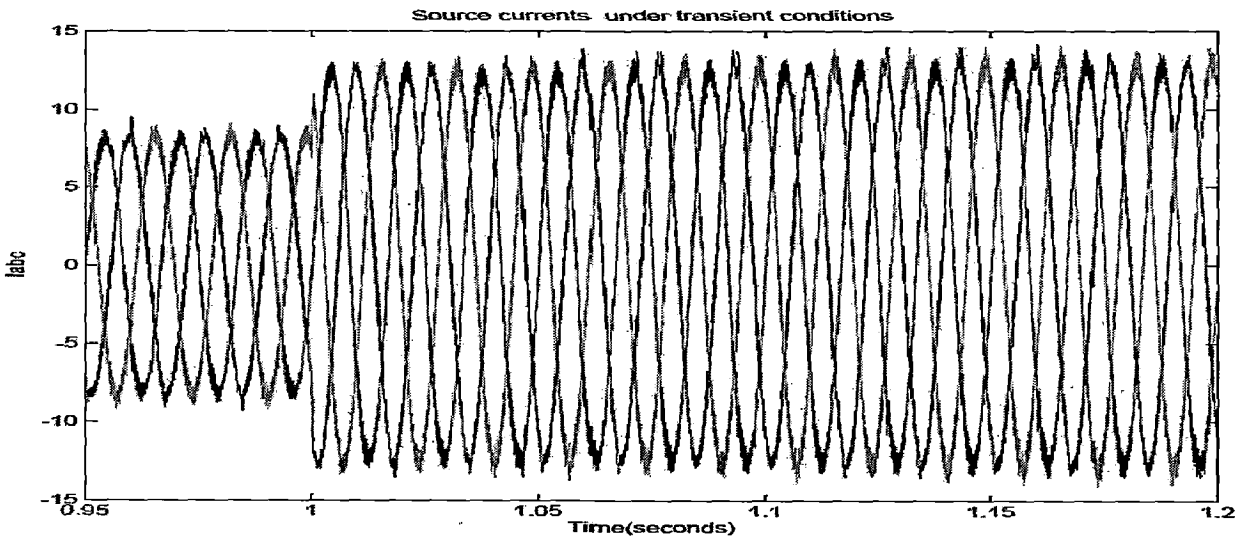


FIG 6.13

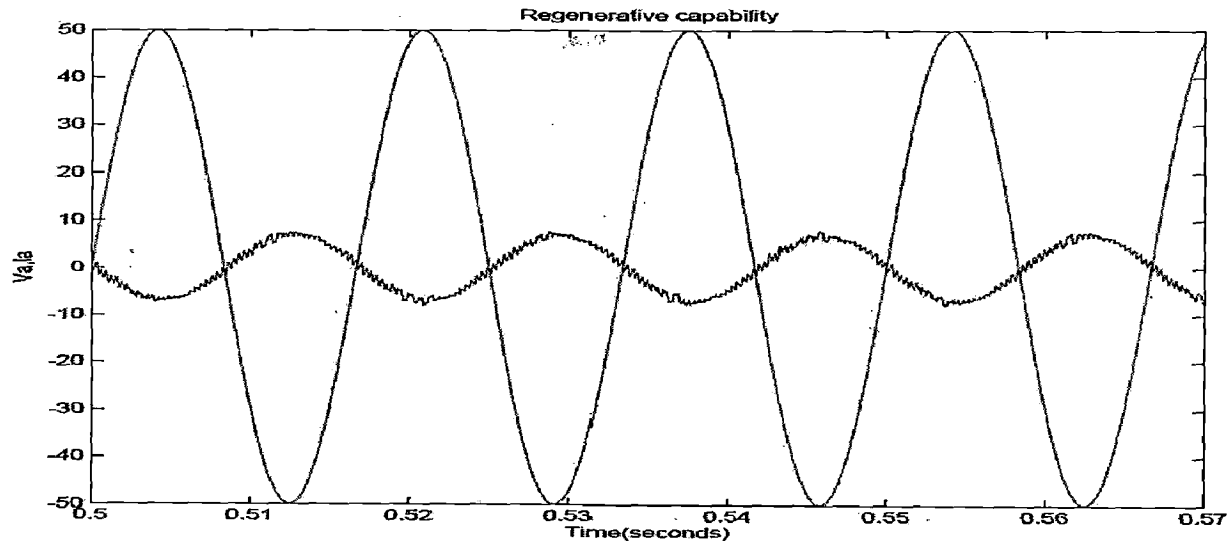


FIG 6.14

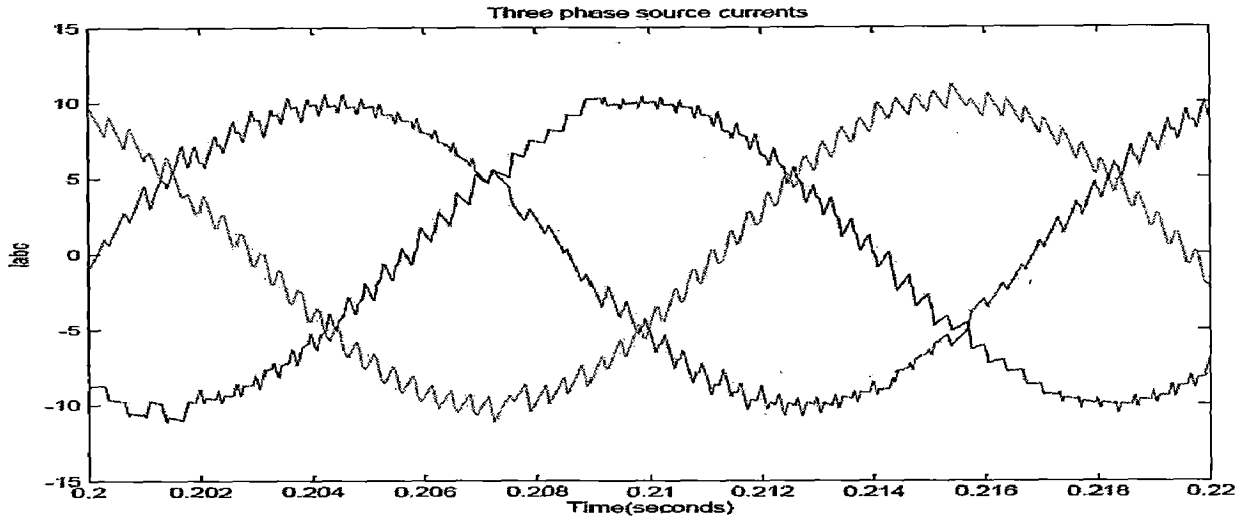


FIG 6.17

Fig. 6.18 and Fig. 6.19 illustrates the transient waveforms of the DC link voltage and input current for the step change of the reference voltage of DC link from 220V to 270V. One sees that the magnitude of input current, which is the output of the voltage PI controller, changes according to the step change of the reference voltage and that the DC link voltage follows the voltage command. To show the regenerative capability of the proposed rectifier, the load is assumed to be active and consists of a DC source of 245V and a load of 2 ohms. Due to the higher applied output voltage, the load current is reversed. Fig. 6.20 shows the waveforms of A phase input current and A phase voltage.

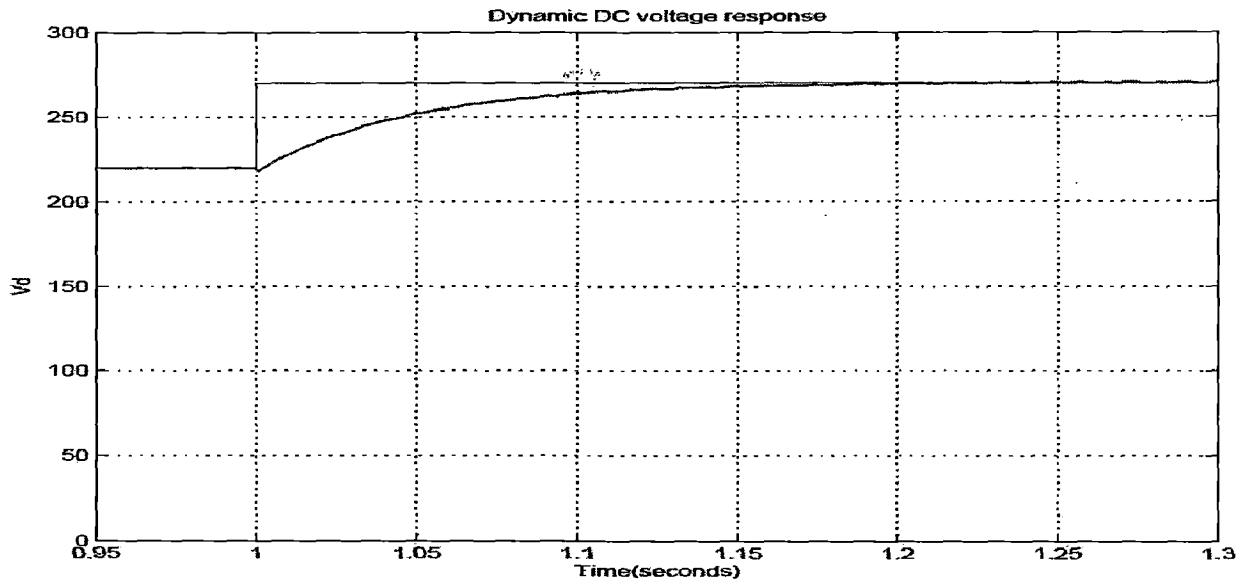


FIG 6.18

6.4 FUZZY SPACE VECTOR MODULATED CONTROL

The control strategy is verified in the following aspects

a. The line current drawn from the AC mains is sinusoidal and is in-phase with the respective phase voltages (High power factor operation).

b. The DC output voltage is maintained at the reference value.

c. The Transient response of the rectifier is satisfactory.

d. The regenerative capability of the interface is maintained.

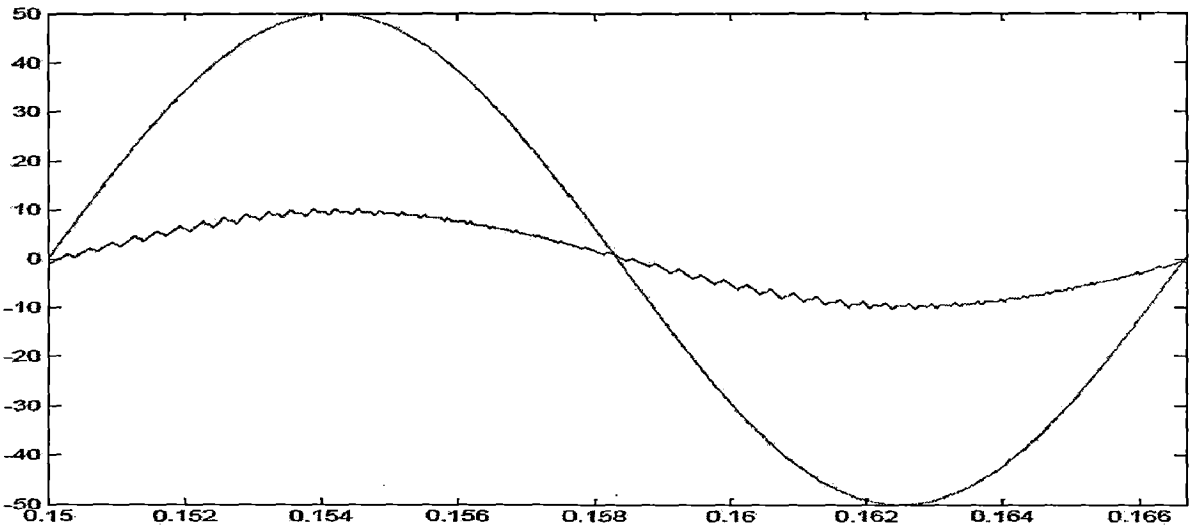


FIG 6.21 A-PHASE VOLTAGE AND CURRENT

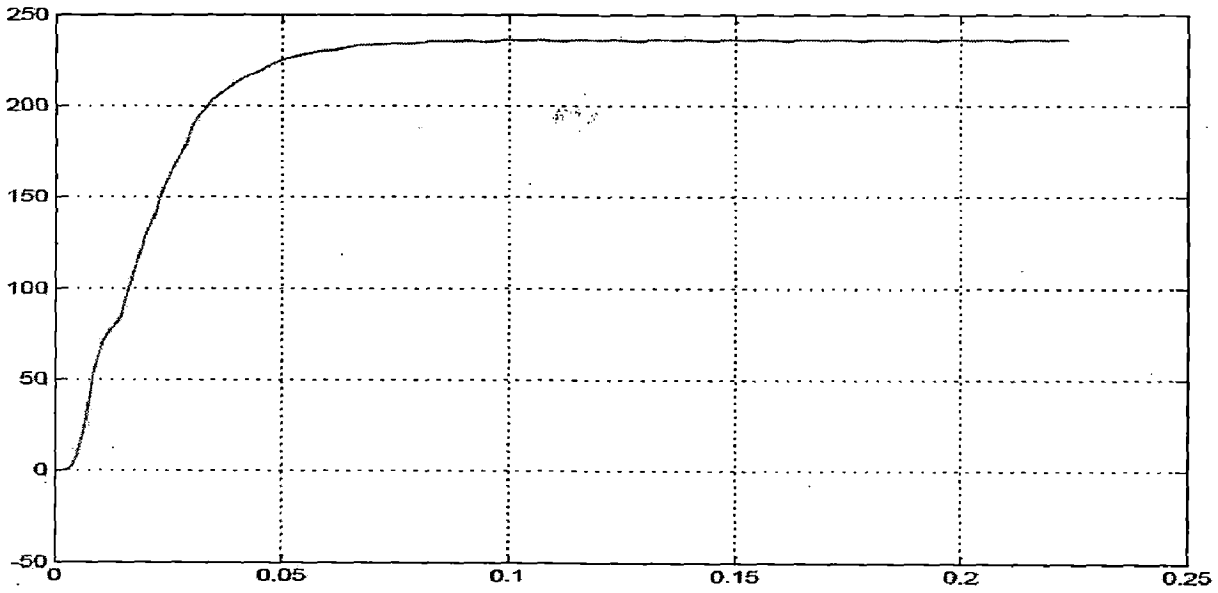


FIG 6.22 DC OUTPUT VOLTAGE

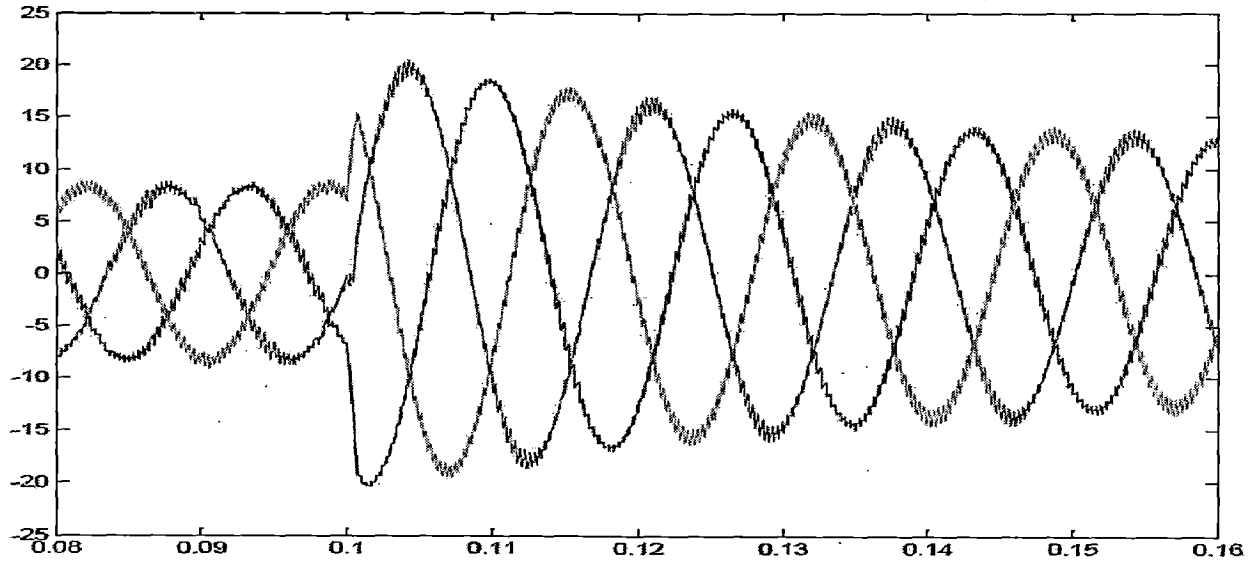


FIG 6.25 SOURCE CURRENTS UNDER TRANSIENT CONDITIONS

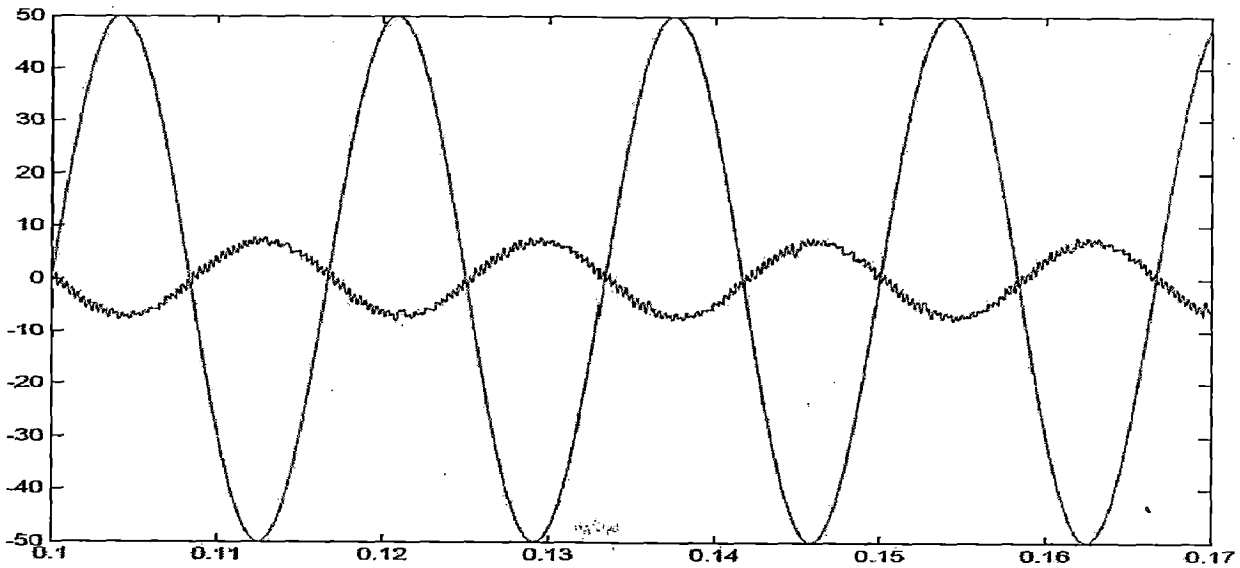
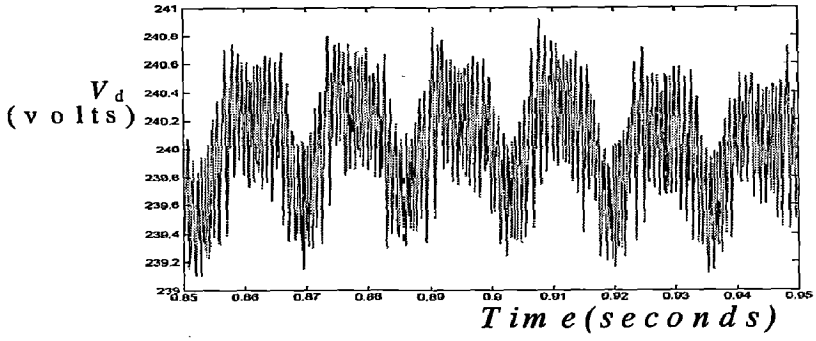


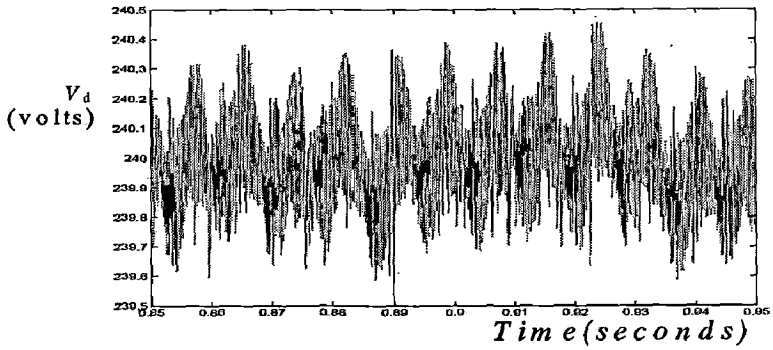
FIG 6.26 REGENERATIVE CAPABILITY

Thd(i_a) is observed to be 0.44%, Thd(i_b) is observed to be 0.6% and Thd(i_c) is observed to be 0.39%.

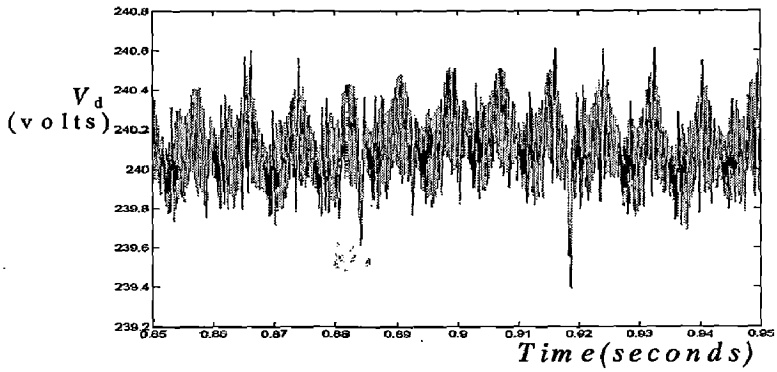
due to reduction of ripple in i_c.



a. reduced hysteresis



b.SVM



c. DPM

FIG 6.28 V_d RIPPLE FOR DIFFERENT CONTROLS

By the use of Fuzzy control in Fuzzy SVM scheme, the dynamic response of Fuzzy SVM is better than that of ordinary SVM. Fig.6.23 shows the dynamic response of two controls under two conditions. In the first case the reference DC voltage is changed from 220V to 270V. In the second case keeping the reference constant the load is changed from 150Ω to 100Ω. The waveforms prove that the fuzzy scheme

6.6 A FOUR SWITCH THREE PHASE ACTIVE RECTIFIER WITH THE FUNCTION OF ACTIVE POWER FILTER

Fig. 6.30 shows the diagram of reduced switch rectifier acting as a Active power filter. The control scheme discussed in chapter 5 was adopted.

The parameters selected for simulation studies are:

Source voltage peak, Vs=100V

Source resistance R_s=0.1Ω, Inductance of line before Active filter L_s=0.15mH

Boost inductor before active rectifier, L_{af}=0.5mH, C_1=C_2=2200μF

$V_{dc,ref}$= 350V, Active rectifier load R_0=100Ω.

Diode bridge with a load of R_L=10Ω, L_L=15mH is considered as a nonlinear load.

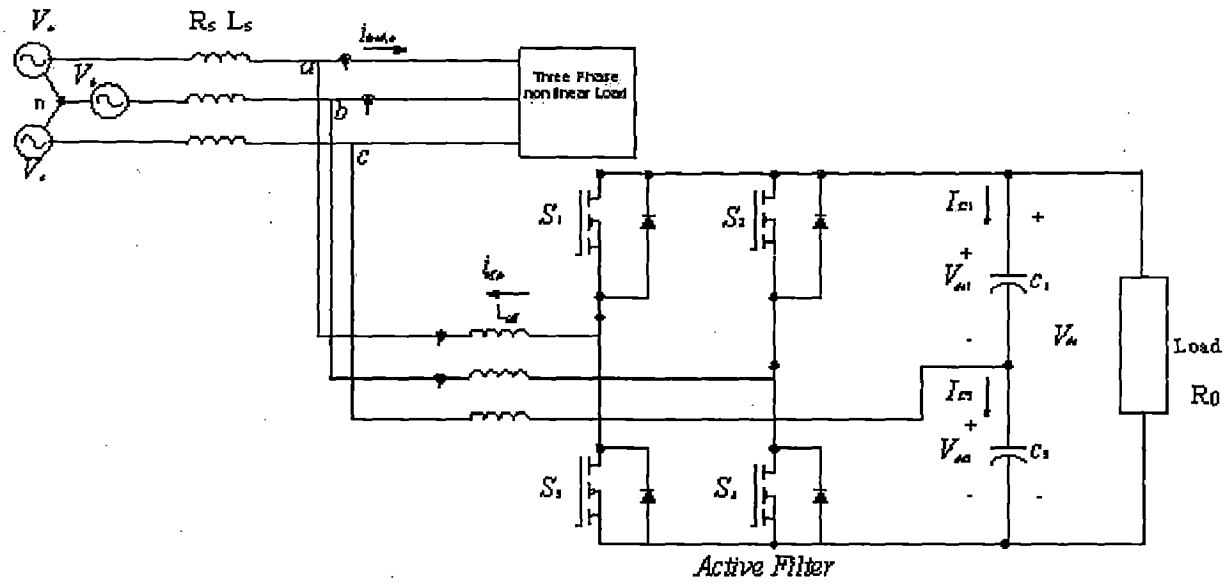


Figure 6.30: FOUR SWITCH THREE PHASE ACTIVE RECTIFIER ACTING AS A ACTIVE POWER FILTER

Fig. 6.31 shows the A-phase source voltage. The nonlinear load current in phase A is shown in Fig. 6.32. Fig. 6.33 shows the source phase-A current with compensation, the current is sinusoidal and in phase with source voltage. Fig. 6.34 shows the current drawn by active rectifier acting as a Active power filter. The current is a in-phase sinusoidal superimposed by the harmonic current required to make the line current sinusoidal. Fig. 6.35 shows the three phase currents with compensation. The output DC voltage and DC load current waveforms are shown in Fig.6.36 and Fig. 6.37 respectively. The FFT analysis for three phase currents with compensation is shown in Fig. 6.38.

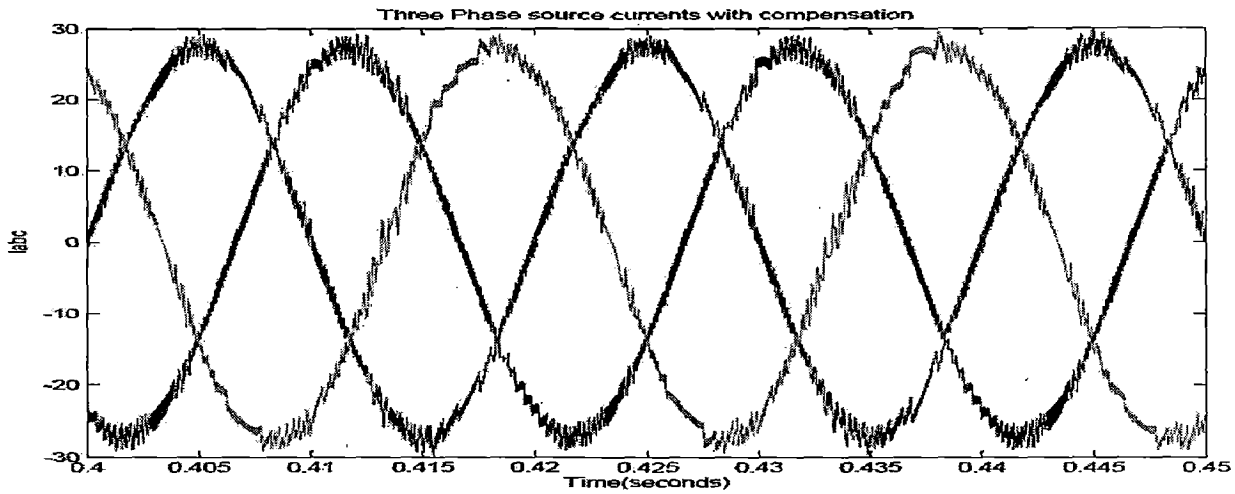


FIG 6.35

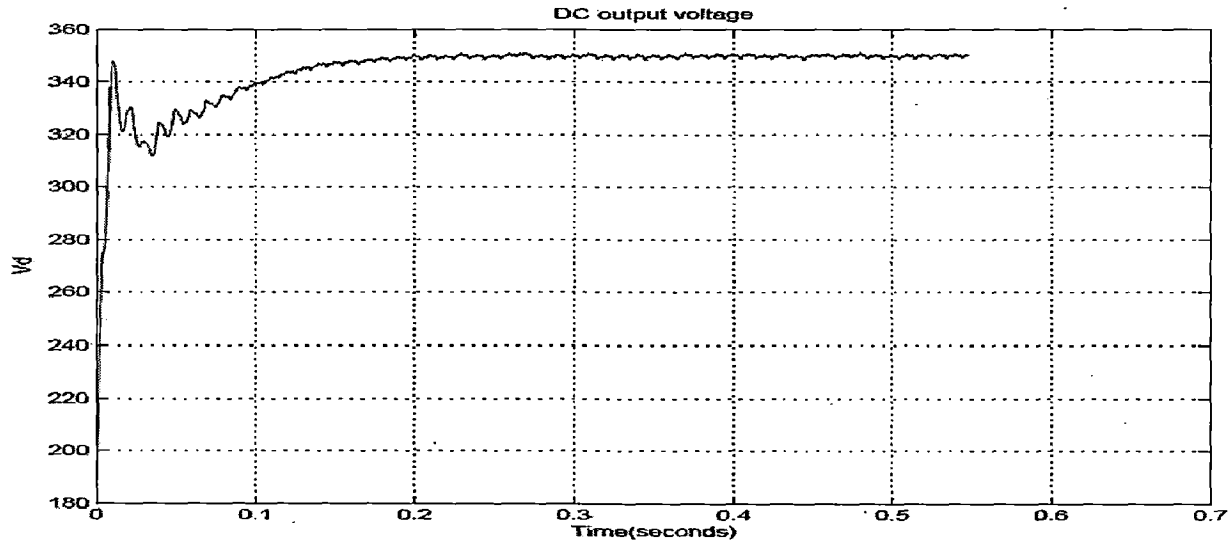


FIG 6.36

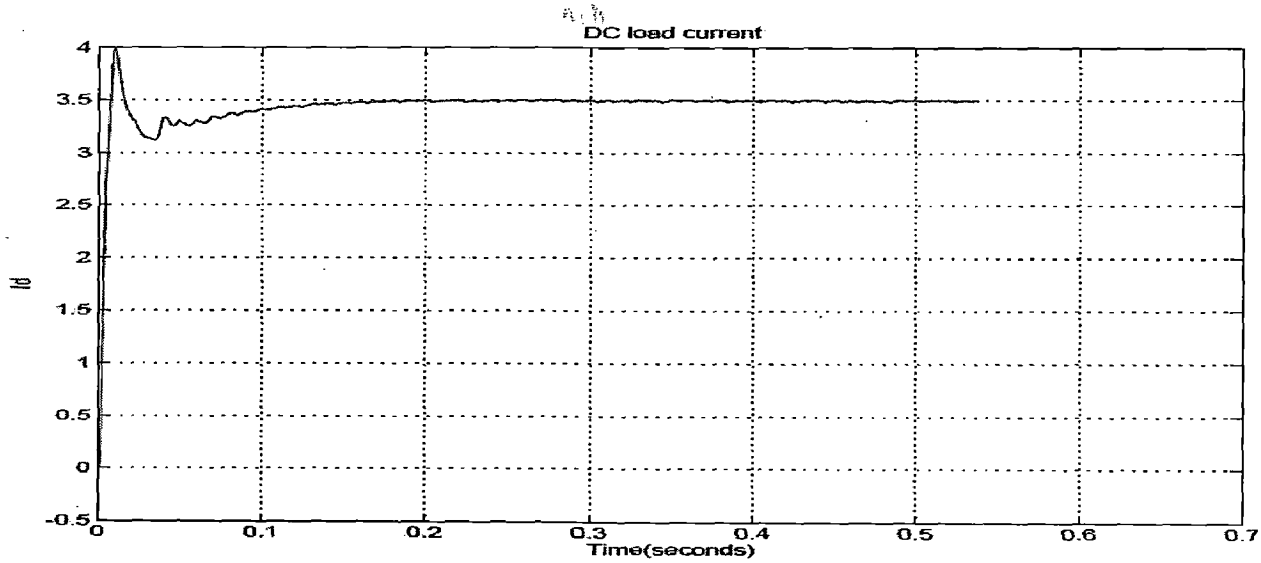
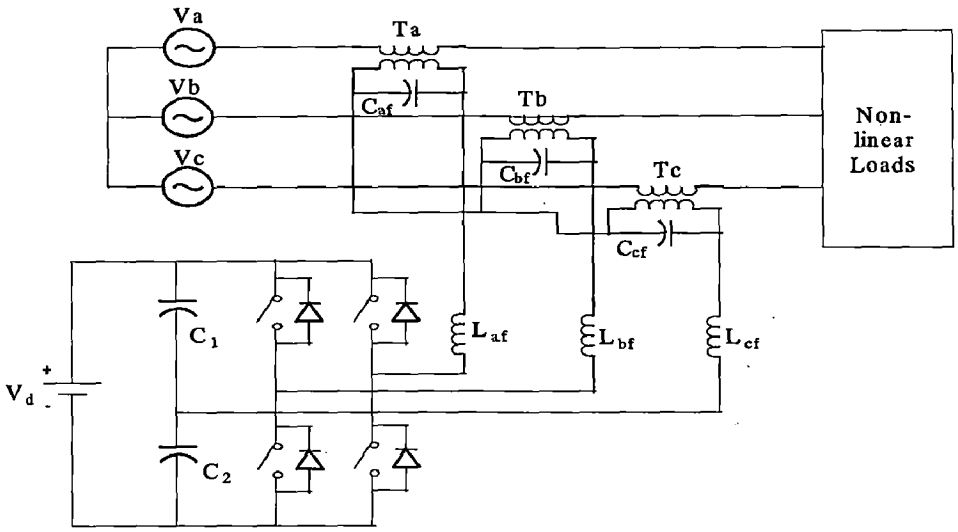


FIG 6.37



Four switch three phase Series active power filter

FIG 6.39

Unbalance Compensation

$V_a=110\sin(\omega t)$
$V_b=90\sin(\omega t-130)$
$V_c=90\sin(\omega t+130)$

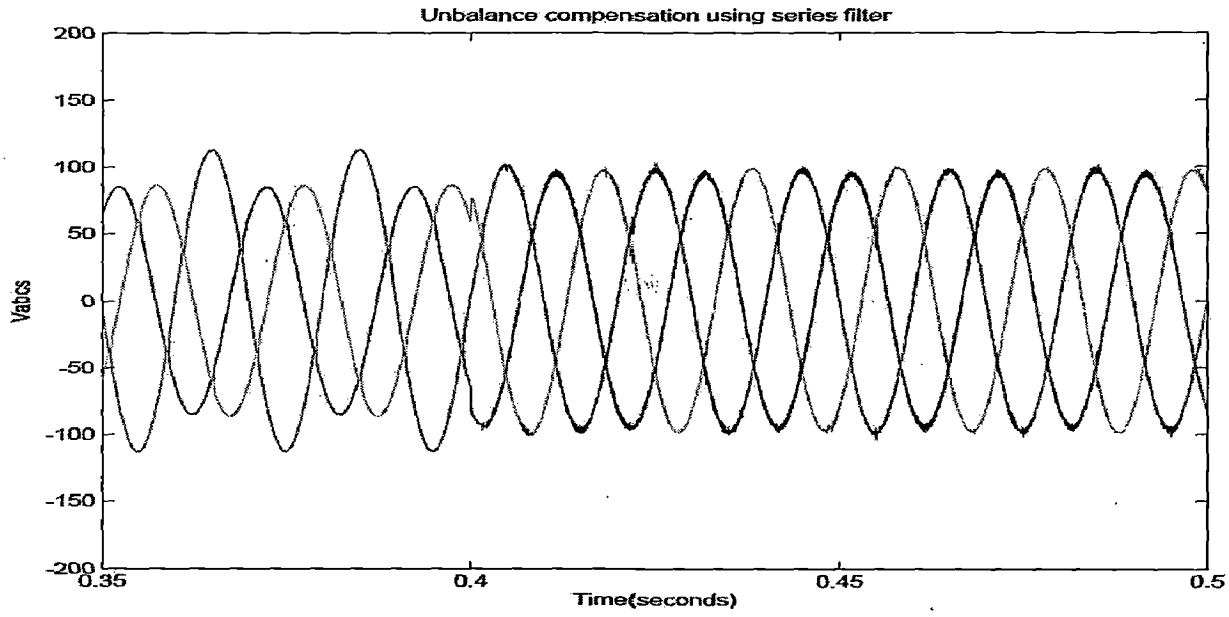


FIG 6.40

Fig. 6.40 validates the unbalance compensation capability of the proposed topology and its control scheme. Note, that here the unbalance is such that no zero sequence component voltages need to be compensated.

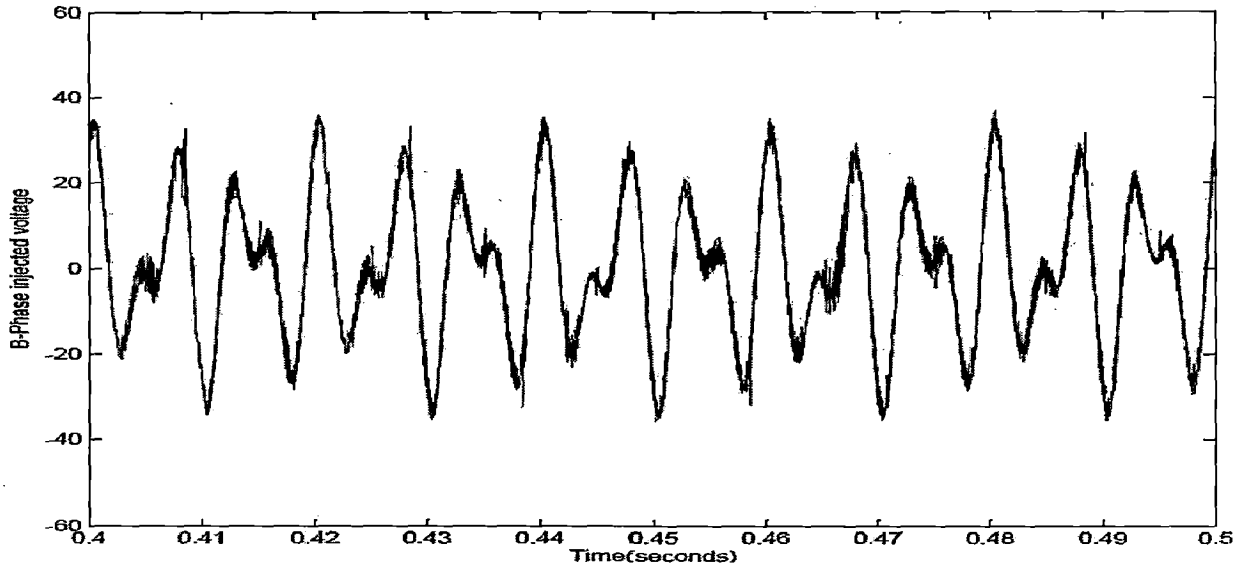


FIG 6.44

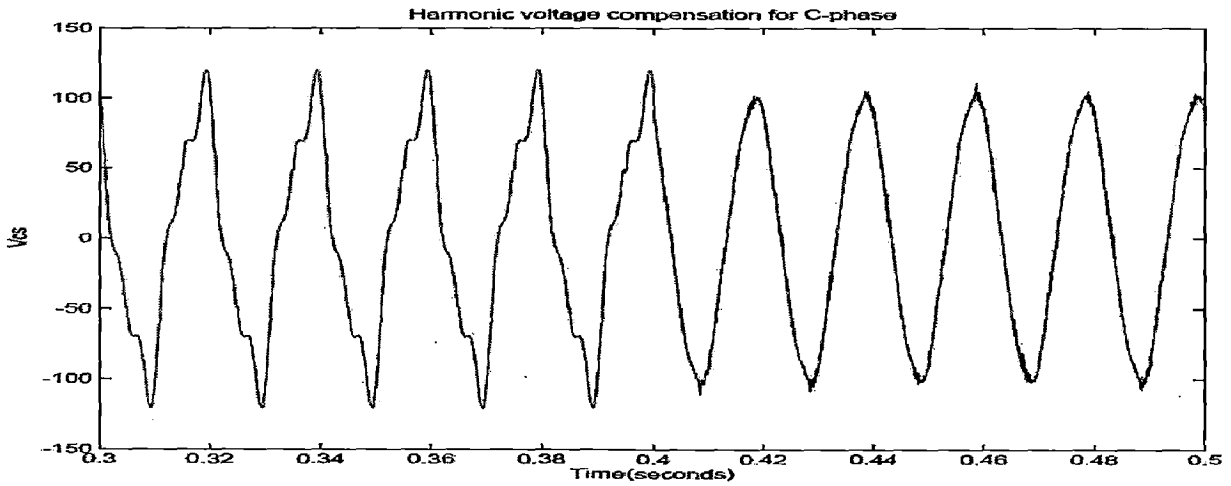


FIG 6.45

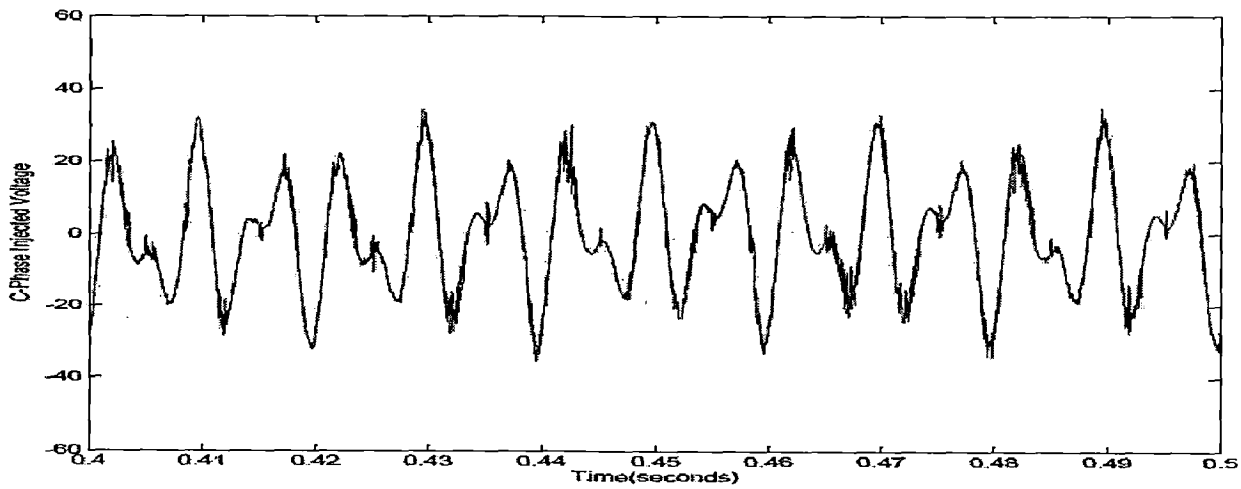


FIG 6.46

CHAPTER-7

SYSTEM DEVELOPMENT

The system hardware can be divided into following blocks:

- Power circuit
- Pulse amplification and isolation circuits
- AC current measurement circuits
- DC and AC Voltage measurement circuits
- Power supplies
- Circuit protection
- Hysteresis current controller

7.1 POWER CIRCUIT

Fig. 7.1 shows the power circuit of four switch three phase active rectifier. Each MOSFET switch used in the circuit consists of an inbuilt anti parallel free wheeling diode. No forced commutation circuits are required for MOSFETs because they are self commutated devices (they turn on when the gate signal is high and turn of when the gate signal is low). The source inductance restricts large di/dt through MOSFETs, hence only turnoff snubber is required for protection. An RCD (resistor, capacitor and diode) turn-off circuit is connected to protect the circuit against high dv/dt and is protected against power voltage by connecting MOV (Metal Oxide Varistor).

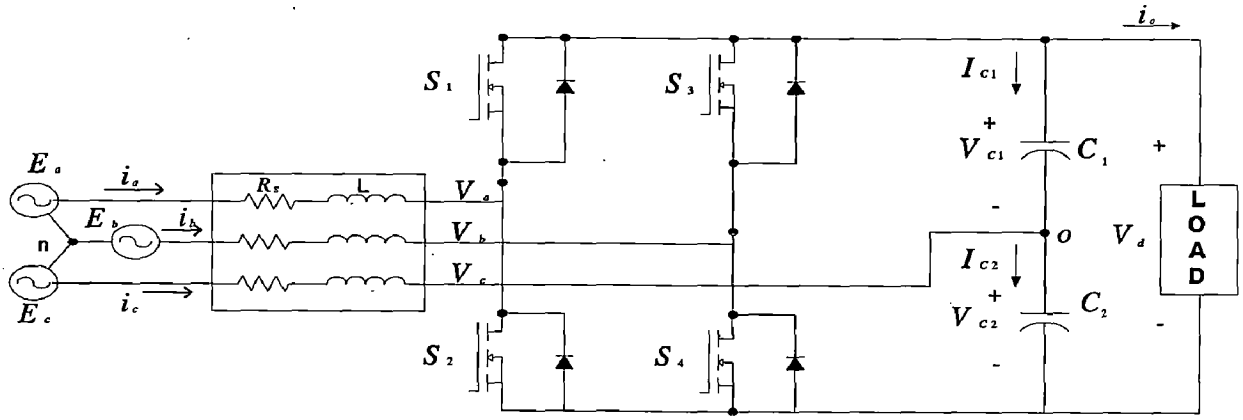
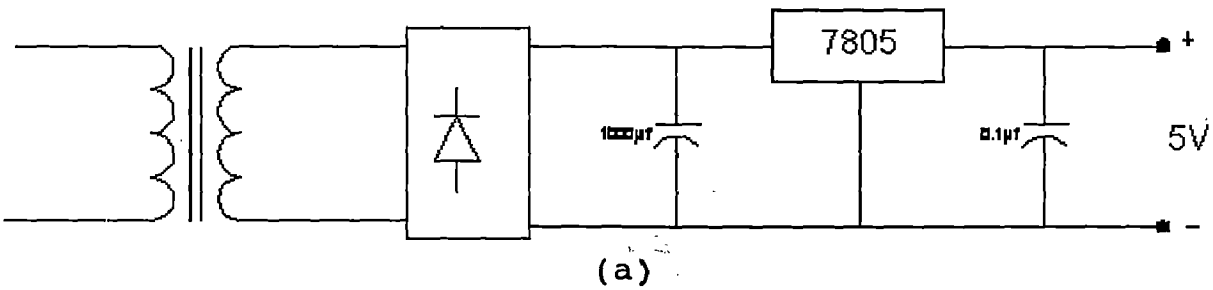


FIG 7.1 FOUR SWITCH THREE PHASE ACTIVE RECTIFIER

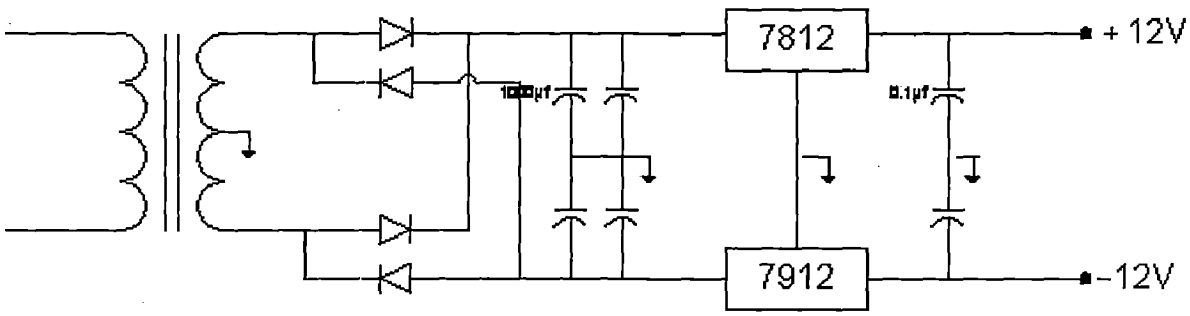
7.3. POWER SUPPLIES

D.C regulated power supplies (±12 V and +5 V) are required for providing the biasing to various ICs, etc. the system development has in-built power supplies for this purpose. The circuit diagram for various dc regulated power supplies are shown in Fig. 7.3. As, shown the single phase AC voltage is stepped down and the rectified using diode bridge rectifier. A capacitor of 1000. F, 50V is connected at the output of the bridge rectifier for smoothing out the ripples in the rectified dc voltage of each supply. IC voltage regulated chips, 7812, 7912, 7805 are used for obtaining the dc-regulated voltages. A capacitor of 0.1. F, 50 V is connected at the output of the IC voltage regulator of each supply for obtaining the constant, ripple-free dc voltage.

DC VOLTAGE	IC REGULATOR
+5V	7805
+12V	7812
-12V	7912



(a)



(b)

FIG. 7.3 POWER SUPPLIES (a) +5V SUPPLY (b) ±12V SUPPLY

output from the hall element away from the steady state condition. This output is amplified to produce a current(I_s),which is passed trough a secondary winding causing a magnetizing force to oppose that of the primary current, thereby reducing the air gap flux. The secondary current is increased until the flux is reduced to zero. At this point the hall element output will return to steady state condition and the ampere turn product of secondary circuit will match that of the primary. The current that passes through the secondary winding is the output current. The transformation ratio is calculated by the standard current transformation equation:

$$N_pI_p=N_sI_s$$

Where, N_p= Primary turns

I_p= Primary current

N_s= Secondary turns

I_s= Secondary current

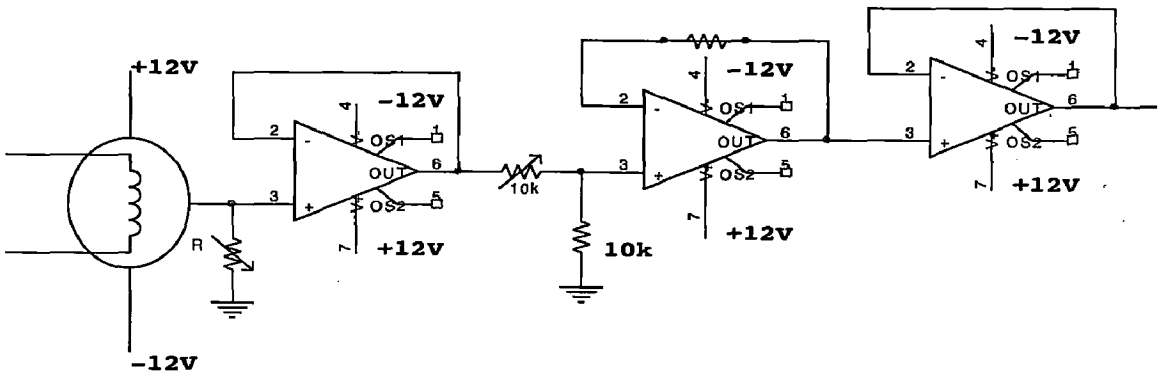


Fig.7.5. HALL-EFFECT CURRENT SENSOR

A 10K. resistor is used in the negative feed back path of the OP-AMP for gain adjustment so as to obtain a voltage of 1 volt corresponding to 1 Amp (DC current). The current carrying conductors are passed in the reverse direction in the current sensor in order to obtain right polarity current at the output of the inverting amplifier. Same circuit is used for measuring other currents (I_b, I_c).

7.6 VOLTAGE SENSING CIRCUIT

The DC or AC voltages are sensed through isolation amplifier AD202 for the voltage control of the converter. We are using AD202 of SIP configuration, although it is available in DIP configuration. AD202 provide the total galvanic isolation between input

$$G_C(s) = \frac{K_C(1+sT_C)}{s}$$

$$where, T_C = C_f R_f and$$

$$K_C = \frac{1}{R_1 C_f}$$

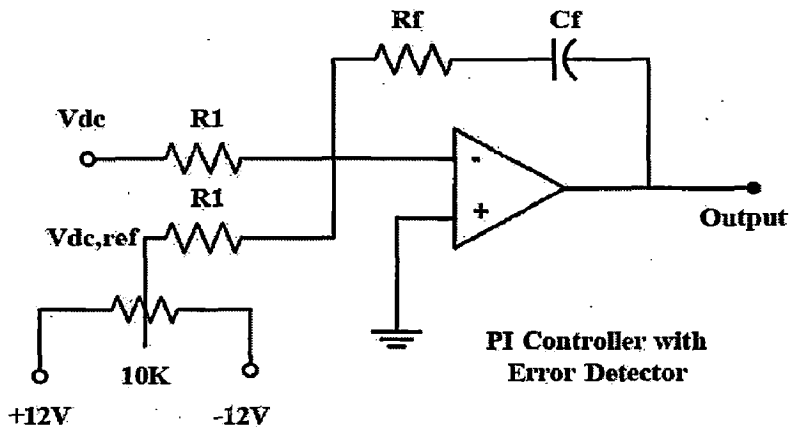


Figure 7.7: ANALYSIS OF PI CONTROLLER WITH ERROR DETECTOR

From the design of PI controller, values of proportional and integral constants are selected as K_P = 0.5 and K_I = 10. From, the design given for the above, it is derived by selecting capacitor value as C_f = 0.1uF, R_1 = 1Mohm, and R_f = 470Kohm. The output of the PI controller will estimate the peak of the fundamental current that has to drawn from the source. Using voltage supply templates, by multiplying them with the peak value, the instantaneous reference currents are estimated. For multiplication operation IC AD 633 is selected to implement the above operation. The above operation is shown in circuit form in Fig 7.8.

7.8 HYSTERESIS CURRENT CONTROLLER

Once the reference currents are known the next aim is to make actual currents track reference values. Hysteresis current controller (HCC) circuit consists of error amplifier, Schmitt trigger. Figure 7.9 shows the circuit diagram of the hysteresis current controller. The actual line current is subtracted from the reference current and error is amplified by ($-R_2/ R_1$) factor. The amplified error is send to the inverting comparator as a Schmitt trigger through the trimpot. The upper threshold voltage of the Schmitt trigger is $+VR_4/(R_4+R_5)$ and the lower threshold voltage is $-VR_4/(R_4+R_5)$. Hence, hysteresis

7.9 DELAY CIRCUIT

Values of R and C are chosen to provide a delay around 5μs i.e larger than turn-off transition time of the MOSFET. The switching signals from the lockout delay circuit are sent to the pulse amplification and isolation circuit.

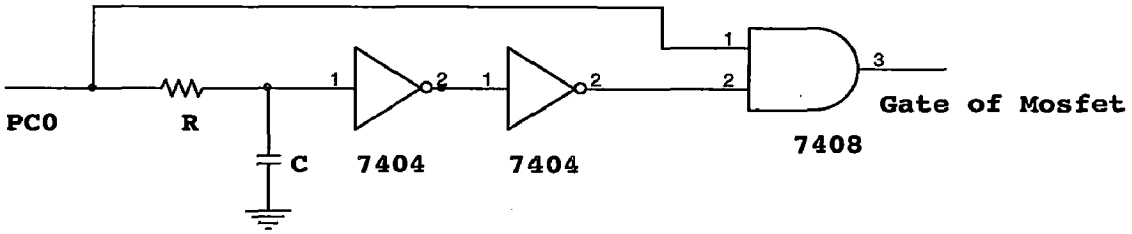


Fig.7.10. DELAY CIRCUIT

This circuit provides 5μS delay and R=5kΩand C=0.001μF

CHAPTER-8

EXPERIMENTAL RESULTS

The complete hardware required to test reduced hysteresis control of four switch three phase power factor corrected active rectifier is developed using the circuits given in chapter 8. The output DC voltage is sensed using the voltage sensing circuit of section 7.6. The reference DC voltage and the output DC voltage are the inputs to the PI controller of section 7.7. The output of PI controller, reference current magnitude is input to the AD633 multiplier circuit. The outputs of the multiplier circuit are the instantaneous reference currents for A-phase and B-phase. The instantaneous reference currents and the actual source currents sensed through the current sensing circuits of section 7.5 are compared using a opamp subtractor circuit followed by the Schmitt trigger circuit discussed in section 7.8. The outputs of two hysteresis controllers are pulses to S1 and S3(Fig 2.1). S1 is inverted to get S2 and S3 is inverted to get S4. The pulses for four switches are then passed through the delay circuits of section 7.9 in order to get protection from shoot through faults. There after the four switch pulses are given to their respective pulse amplification and driver circuits of section 7.2 to get the final gating pulses for four switches.

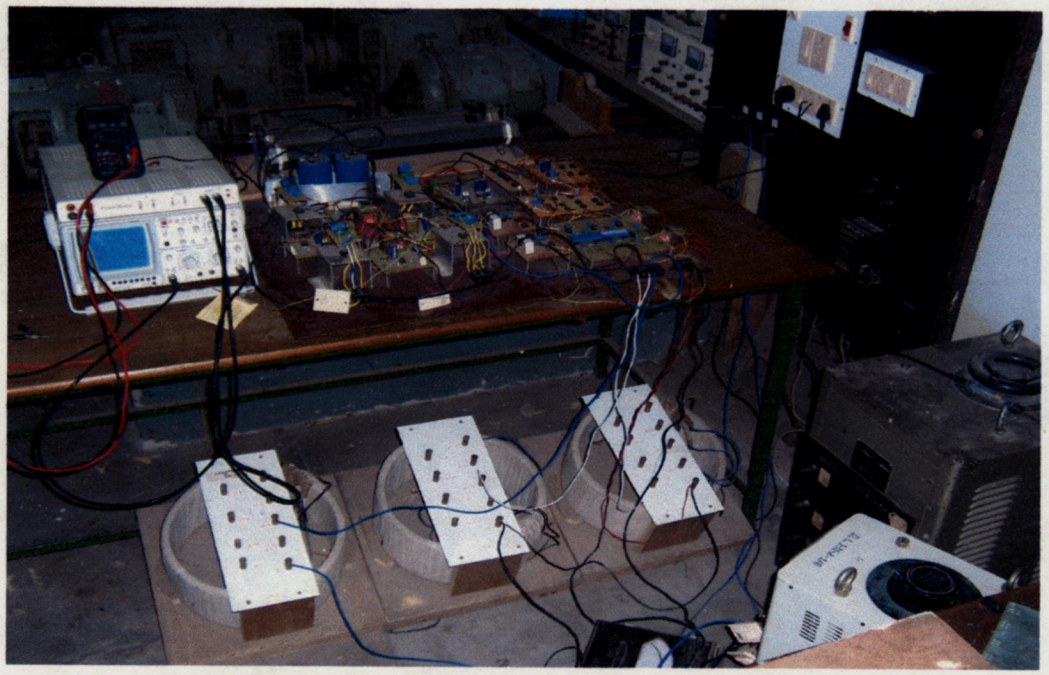


FIG 8.1 LABARATORY EXPERIMENTAL SETUP

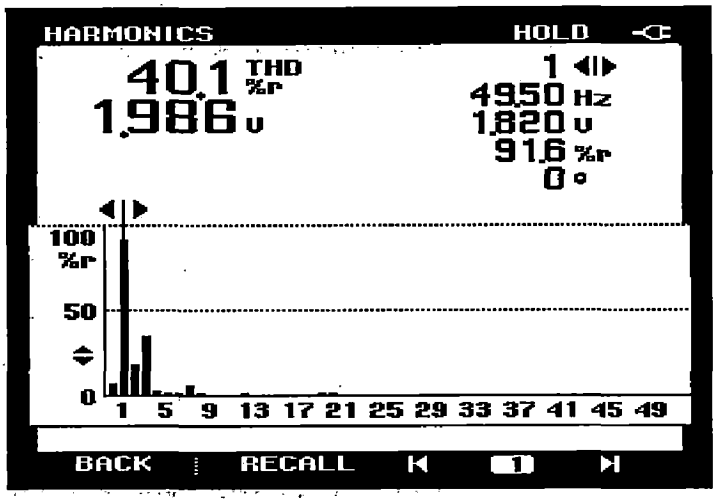


FIG 8.4 THD FOR SOURCE CURRENT

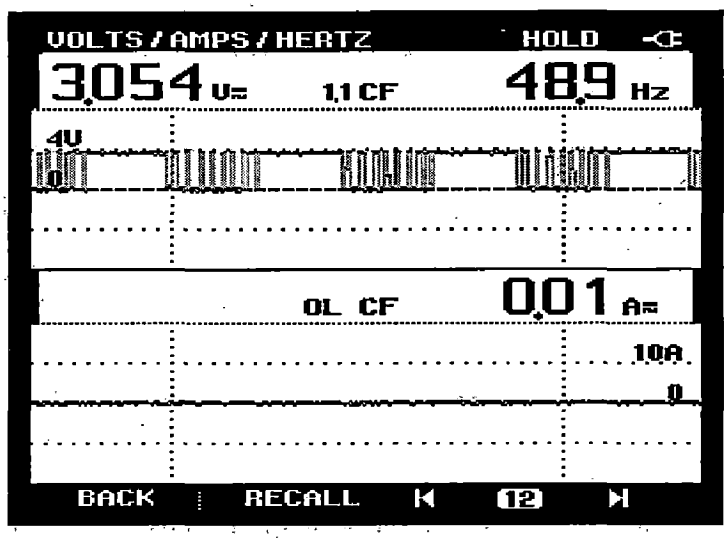


FIG 8.5 SWITCHING PULSES TO S1

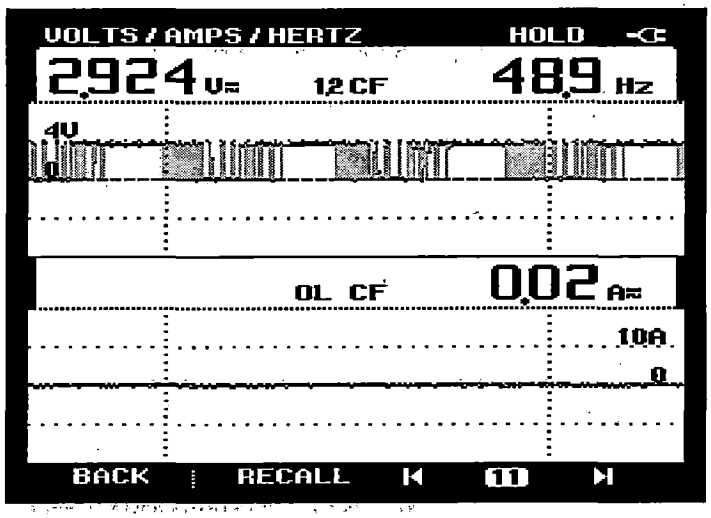


FIG 8.6 SWITCHING PULSES TO S3

CHAPTER-9

CONCLUSIONS AND FUTURE SCOPE

CONCLUSIONS

The following conclusions are drawn from the present work

- The traditional diode/thyristor rectifiers can pollute the AC supply with significant levels of low frequency harmonics, pulsating input current (electromagnetic interference (EMI)), and excessive VAR. With tough regulations and severe economic restraints, the design of a three-phase switching mode rectifier which draws nearly sinusoidal three-phase input currents with unity power factor(power factor corrected rectifiers) is very important.
- Reduced switch count power factor rectifiers posses several desirable features such as low cost, more reliability, high efficiency, less number of sensors.
- All the presented controls(reduced hysteresis, Space vector modulation, Direct power modulation, Fuzzy space vector modulation) for the considered four switch three-phase active rectifier(reduced switch topology) develops the reference DC voltage maintaining unity power factor sinusoidal currents).
- Reduced hysteresis control of the considered rectifier is a variable switching frequency technique and causes more ripple in i_c .
- Space vector modulated control and direct power modulated control are constant switching frequency schemes and the overall input current waveform quality is improved. The ripple in i_c is also less. The dynamic performance of SVM(or DPM) can be improved by using outer loop fuzzy control.
- The considered rectifier can also be used for line harmonic current filtering. A reduced switch series filter based on the considered four switch three-phase topology can also be developed for improving source voltage quality.
- Experimental prototype of the considered rectifier is developed and reduced hysteresis control is tested.

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Hall-Effect Current Transformers/Sensors

Closed-loop HALL-Effect current sensors are widely used in a variety of applications requiring an accurate, fast response signal proportional to the current being measured. Products are available for panel and PCB mounting covering primary current up to 1000A and provide complete galvanic isolation between the primary and the measuring circuit.

Closed-loop Hall effect current-sensors use the ampere-turn compensation method to enable measurement of current from dc to high frequency with the ability to follow rapidly changing level or wave shapes. The application of primary current (I_p) causes a change of the flux in the air-gap, this in turn produces a change in output from the hall element away from the steady-state condition. This output is amplified to produce a current (I_s) which is passed through the secondary winding causing a magnetizing force to oppose that of the primary current, there by, reducing the air-gap flux. The secondary current will increase until the flux is reduced to zero. At this point, the hall element output will have returned to the steady state condition and the ampere-turn product of the secondary circuit will match that of the primary. The current that passes through the secondary winding is the output current.

Main features of the current-sensor used are:

I. High accuracy.
II. Galvanic isolation between primary and secondary.
III. Non-Contact ness.
IV. Covers ac, dc and impulse current measurements.
V. Ease of installation.
VI. Wide dynamic range.

Linearity of the sensor is 0.1% of normal primary current and the operating temperature range is 0-70°C.

Voltage Sensors AD202/AD204

Features

I. Small Size: 4 Channels/Inch
II. Low Power: 35mW (AD204)
III. High Accuracy: ±0.025% Max Nonlinearity (K Grade)
IV. High CMR: 130 dB (Gain = 100 V/V)
V. Wide Bandwidth: 5 kHz Full-Power (AD204)
VI. High CMV Isolation: ±2000 V_{PK} Continuous (K Grade)

(Signal and Power)

I. Isolated Power Outputs
II. Uncommitted Input Amplifier

Applications

I. Multi-channel Data Acquisition
II. Current Shunt Measurements
III. Motor Controls
IV. Process Signal Isolation
V. High Voltage Instrumentation Amplifier

General Description

The AD202 and AD204 are general purpose, two-port, and transformer- coupled isolation amplifiers that may be used in a broad range of applications where input signals must be measured, processed, and/or transmitted without a galvanic connection. These industry standard isolation amplifiers offer a complete isolation function, with both signal and power isolation provided for in a single compact plastic SIP or DIP style package. The primary distinction between the AD202 and the AD204 is that the AD202 is powered directly from a 15 V dc supply while the AD204 is powered by an externally supplied clock, such as the recommended AD246 Clock Driver.

The AD202 and AD204 provide total galvanic isolation between the input and output stages of the isolation amplifier through the use of internal transformer-coupling. The functionally complete AD202 and AD204 eliminate the need for an external, user-

supplied dc-to-dc converter. This permits the designer to minimize the necessary circuit overhead and consequently reduce the overall design and component costs. The design of the AD202 and AD204 emphasizes maximum flexibility and ease of use, including the availability of an uncommitted op-amp on the input stage. They feature a bipolar ±5 V output range, an adjustable gain range of from 1V/V to 100 V/V, ± 0.025% max nonlinearity (K grade), 130 dB of CMR, and the AD204 consumes a low 35mW of power.

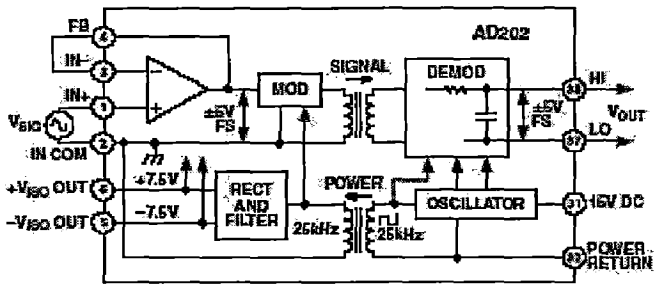

Figure A-1

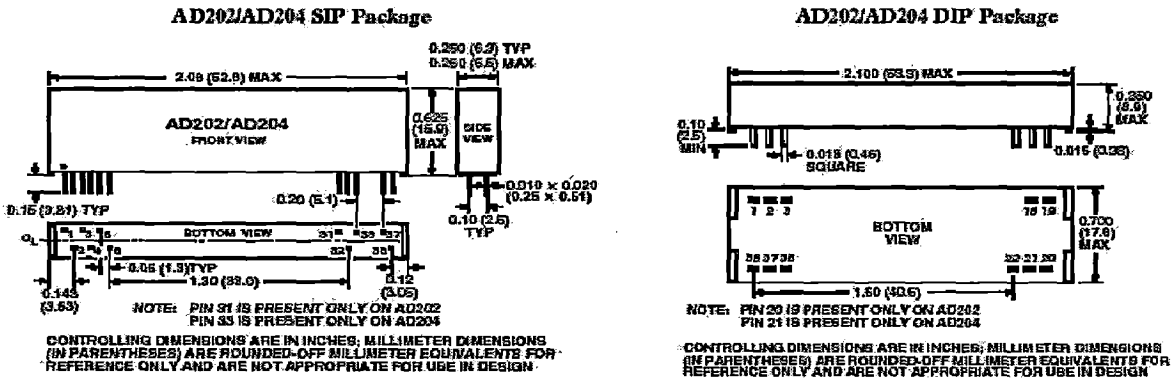

Figure A-2

The functional block diagram of AD202 is shown in *fig A-1* and *fig A-2* shows the pin configuration of AD202 in SIP and DIP package respectively

Power Semiconductor Switches

Traditionally thyristors have been used as switches in converters. But the PWM technique requires forced-commutation of thyristors that necessitates the need for additional commutation circuitry, thus, adding to the cost, bulkiness and complexity of

the converter circuit. Further more, the thyristors can't be switched at higher frequencies and this puts a limit on the switching frequency of the PWM converters. In recent years, more and more power semiconductor devices with high switching frequencies and/or power capability such as bipolar transistors, power MOSFETs, GTOs and IGBTs are becoming quite popular. This makes possible the easy use of the PWM technique to improve the quality of input current waveform and power factor.

Power Transistor

A power-transistor employed as a solid-state switching device and requires only one signal to turn it ON and it turns OFF automatically on the removal of this signal. Thus, in the PWM voltage-source converters, no commutation circuitry is required and the problems associated with the commutation (of thyristors) are automatically overcome. Further, the control circuitry is much simplified. Since the turn-ON and turn-OFF times of the order of 1μsec or less are achieved in power transistors, the devices can be operated at a high switching frequency. The power transistors suffer from a major problem of the second breakdown (SB), which is a destructive phenomenon, resulting from the current-flow to a small portion of the base and producing localized hotspots. If the energy in these hotspots is sufficient, the excessive localized heating may damage the device. Other drawbacks are the sensitivity to transients and low overload capacity. The schematic block diagram is shown in *fig A-3*.

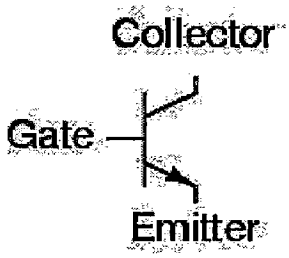

Figure A-3

Gate Turn OFF Thyristors (GTOs)

GTOs seems to hold a lot of promise fo the future. Presently their use is limited because of high cost and non-availability. A GTO can be turned-OFF by a negative gate-

pulse and can be triggered by a positive gate-pulse. When a GTO has been turned-ON, it behaves as a thyristor. It can be manufactured for the highest voltage and current ratings (several kV and kA) and is mainly used for high power and/or high voltage equipment. With the obvious advantage of the non-requirement of a commutation circuit, which lays a restriction on the operating frequency of thyristors, the GTO has also some disadvantages. During turn-ON and turn-OFF, a GTO acts like a transistor, running a risk of second breakdown if the gate-pulse is insufficient. A GTO has a higher ON-state voltage as compared to a thyristor and the latching and holding currents are also high.

Power MOSFET

A Power Mosfet is a voltage-controlled device and requires only a small input current. The switching speed is very high and the switching times are of the order of nano-seconds. Power Mosfet's are finding increasing applications in low-power, high frequency converters. Mosfet's don't have the problems of the second breakdown as do the BJT's. Mosfet's are of two types

1) Deletion Mosfet's and,
2) Enhancement Mosfet's.

The main features of power Mosfet's are summarized as below:

I. Better reliability.
II. Simpler and cheaper driver circuitry.
III. Higher switching frequency (well above 1Mhz) due to fast switching speed and better efficiency, smaller overall circuit size and weight at high frequency.
IV. High overload and peak current handling capability.
V. Absence of second breakdown reduces the snubber circuitry in switching applications and
VI. Better temperature capability.

Like any other semiconductor device, Power Mosfet's do have their own subtleties and these must be recognized for the successful operation of the devices.

STATIC CHARGE: Power Mosfet's can be damaged by static charge when handling, testing or installing into a circuit. However, they have greater self-capacitance and are much more able to absorb the static charge. It is wise to employ the elementary

precautions such as the grounded wrist straps, electrically grounded stations and grounded soldering irons.

GATE-VOLATGE TRANSIENTS: Excessive voltage applied to the gate of a power Mosfet's will punch through the gate oxide, thus causing a permanent damage. A typical gate-source voltage rating is ±20V. The simplest solution where the gate voltage transients are suppressed is to connect a clamping Zener diode between the gate and the source.

All the power Mosfet's have an integral body-drain diode built into their structure. This is shown in the *fig A–4*.

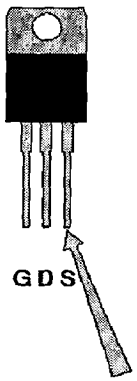

Figure A-4