DISTURBANCE EFFECT ON RELAY

A DISSERTATION

Submitted in partial fulfillment of the requirements for the award of the degree

of

MASTER OF TECHNOLOGY

in

ELECTRICAL ENGINEERING

(With Specialization in Power Systems Engineering)

By

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Candidate's Declaration

I hereby certify that the work which is being presented in this dissertation report entitled, "**Disturbance effect on Relay**", which is submitted in the partial fulfillment of the requirements for the award of the degree of **Master of Technology** in Electrical Engineering with specialization in **Power systems Engineering**, submitted in Electrical Engineering Department, Indian Institute of Technology, Roorkee, is an authentic record of my own work carried out during the period from July 2005 to June 2006 (IV semester) under the supervision of **Sri Bharat Gupta**, *Assistant Professor*, Electrical Engineering Department, Indian Institute of Technology, Roorkee.

The matter embodied in this report has not been submitted by me for award of any other degree or diploma.

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23-06-06

K.G.V. Kumar
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CERTIFICATE

This is to certify that the above statements made by the student are correct to the best of my knowledge.

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Acknowledgement

I take this opportunity to express my sincere gratitude towards my guide **Sri Bharat Gupta,** *Assistant Professor,* Electrical Engineering Department, Indian Institute of Technology Roorkee, for his guidance, advice and encouragement, which were the constant source of inspiration for the completion of dissertation work.

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My heartfelt gratitude and indebtedness are due to my parents for their never fading love and encouragement.

I also thank all those who helped me directly or indirectly in the successful completion of my dissertation.

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Abstract

The design of protective relays has been changed significantly over the past years, due to the advancement in microprocessor and signal processing technology. Use of numerical relays in switchgear necessitates that the user to be familiar with their design and functionality. A Digital Distance Relay (MHO) is designed in this work by using TMS320C10 Processor, for converting both the voltage and current analog signals into Digital Signals, and an 8255 is used to transfer the data to the Personal Computer through Parallel Port.

Filtering requirements, for the digital distance relays are critical because they must estimate precisely and quickly the electrical distance to the fault, even highly distorted input signals. All types of Recursive Fourier filters (1/2 Cycle, 1 Cycle, 2 Cycle, and 3 Cycle), Differential equation based algorithm and the algorithm based on a differential equation combined with Fourier transform are implemented.

The Fourier algorithms possess good high-frequency characteristics. Also, the computation time can be significantly reduced by using recursive calculations. However, the presence of the exponentially decaying DC component adversely affects the calculation accuracy. The differential-equation-based algorithms exhibit poor high-frequency characteristics so that significantly time-delaying filters are required.

Algorithms based on a differential equation combined with a Fourier transform present a better solution for both DC rejection and high-frequency characteristics.

The filters still possess transients for disturbances. All disturbances may not be severe; they may impact on the performance of the relays. Actually the study of disturbance impact on the digital relay will improve the reliability of the power system. The assessment of disturbance impact can be done by quantification of disturbances. This has been done in two ways One is Setting based Quantification and another one is Design based Quantification.

In Setting Based Quantification, the impact factor is calculated for every setting and delay values of the relay. From this data we have to select optimum setting and delay values. This will improve the reliability. In Design based Quantification the impact factor is calculated for all types of filters and compared with the response of each and every type of filter. This gives a better idea for selecting the best filter type.

The digital relay is implemented practically. The testing could have been done practically, but because of equipment failure (Disturbance Generator), the testing has been done in MATLAB simulation. The relay algorithm is implemented in MATLAB and tested by the disturbances generated in PSCAD Power System simulation software. In practical there are so many unexpected disturbances existed. The practical testing will give us better details of disturbance impact.

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Chapter – 1

Introduction

1.1 Introduction

Protective relays are the devices that detect faults or abnormal operating conditions in power systems. In the history of protective relay development, electromechanical relays formed the first generation, followed by static relays and digital relays.

Electromagnetic relays are having problems like, maintenance slow in action, high power consumption for auxiliary mechanisms and worst of all, incapability of implementing complex characteristics. With the advent of integrated circuits and static circuits, a new generation of devices called static relays was developed. Compared with electromechanical relays, static relays are faster, more accurate and can realize more complex functions. They require much less power consumption and little maintenance. In practical applications static relays, also called solid-state relays, are mainly applied in protection for transmission level systems.

But there are some weak points in static relays. Since static relays consist of many electronic components, the overall reliability can be affected by individual components, and these electronic components are sensitive to ambient temperature. Even worse is that static relays are vulnerable to voltage transients, which might cause mal-operation. When relays based on computer could provide performance at least as good as conventional relays. The relays of the 3rd generation are called digital relays, numeric relays, or microprocessor relays alternatively.

The main advantages of digital relays over conventional relays are their reliability, functional flexibility, self-checking and somewhat self adaptability. They are able to implement more complex function, be more accurate and be immune from physical environment effects. Although they are relatively costly, the benefits in enhancing system security and reliability by adopting these relays can make their application worthwhile. At present, their application is mainly in transmission system protection as well as for generation unit protection. The rapid growth in computer and communication industries will alleviate their price disadvantage and explore new horizons for their wider application.

The digital relays are having digital filters like Fourier filters for extracting the fundamental components. But these filters are not ideal in general. Instead of giving accurate result they develop transients. This causes change in the output which is not desirable or causes to mal-trip. The filter effect on different types of disturbances can be calculated by the method described in this dissertation. This is very useful to test the different types of filters.

1.2 Objective of the Dissertation

In this dissertation various types of digital filter algorithms for a digital mho relay are implemented and tested under various disturbances. The digital filter is the heart of digital relay. It should have accuracy, property to eliminate the decaying dc component, less influence at the higher frequencies and fast response. All filters are not ideal. They tend to be ideal by selecting proper signal processing. In general Fourier filter is the best filter among all. Even though it has some disadvantages like cannot eliminate decaying dc component it is best among all

other filters. Generally four types of Fourier filters are used ½ cycles, 1 cycle, 2 cycles, & 3 cycles filter.

The testing on filters is done in two different processes. One is to evaluate severity of impact of disturbance on the relay and another one is to compare responses of the different types of relays. Later one also gives the details of the disturbance signal. These two methods are very useful to improve the reliability of the relay.

In this dissertation the tested relay filters are

1. ½ cycle Fourier
2. Full cycle Fourier
3. 2 cycle Fourier
4. 3 cycle Fourier
5. Differential equation Algorithm
6. Mixed Fourier & Differential equation Filter

All the above mentioned filters are implemented in real time and tested in MATLAB® simulation with the disturbance data generated by the PSCAD™ software. And all the above mentioned filters are recursive type. The advantage of recursive type filters can be studied in later chapters.

1.3 Literature Review

Based on independent research and studies by different institutions, various technical standard systems exist, among which IEC and IEEE [1] standards are the most commonly used ones in the world. The definitions of common disturbances are taken from the guide titled "IEEE Recommended Practice for Power Quality for Monitoring Electric Power Quality" published by IEEE.

A.T. Johns and S.K. Salman [2] explain the different types of relay filters and digital relay architecture clearly. This book is an extraction of journals published in IEEE.

Michael P. Ransick [3], explains the implementation techniques of the digital relay or microprocessor relay. The papers discuss the functional blocks of digital relay. Filtering requirements for distance relays are very critical, because they must estimate precisely and quickly the electrical distance to the fault, even with highly distorted input signals. A number of digital filtering algorithms for distance relays have been proposed and some of them are in use in practical relays; however, power system evolution increases the corruption level of signals and imposes the necessity of continuing the research efforts in this area.

M. G. Adamiak, G. E. Alexander [4], provide recent developments in adaptive algorithms and the use of higher sampling rates combine to provide secure high speed protection are explained. These advancements are in both the area of phasor calculation and the protective algorithm (DSP filter) implementation. The DSP algorithms [5] can make the relay more flexible, faster and capable of removing unwanted signals.

Jose A. Rosendo Macias., Antonio Gomez Exposito[6] discussed the implementation of recursive, approximate non-recursive and exact not recursive algorithms. Recursive Fourier transform algorithm is the most suitable in real time implementation of relay. It provides lesser calculations compared to normal DFT.

Altuve Ferrer. H.J., Diaz Verduzco. et.al [7] explained a comparative evaluation of different digital filtering algorithms for distance protection. An evaluation method is proposed, which gives comprehensive information about filter transient behavior on a wide frequency range of noise. The discussion is focused in well-known algorithms based on Fourier and Walsh transforms, and includes a recently proposed combined sine-cosine filter.

Magnus Akke, James T. Thorp [8] presented some improvements of the differential equation algorithm for transmission line protection.

H. C. Wood and M. S. Sachdev [9] described the application of modern signal processing techniques to power system protection and those aspects of signal processing that are unique to the fast, real time operation necessary in electric power system.

Wang F., Bollen M. H. J, [11], explained a method to quantify the effect of disturbances on a protective relay is presented. Both solid-state and digital relays are modeled- and tested under various measured disturbance conditions. As the effect of disturbances on protection devices is dependent on the structure and principle of a relay, a method is developed to evaluate the severity of disturbances as experienced by the relay. They also explained [10] quantification of the potential impacts of disturbances on power system protection and give the information about disturbance database setup [12] for protective relay testing.

Rafael Collantes-Bellido, Tomas Gomez [15] proposed a model for arc-furnace to generate voltage disturbance like voltage fluctuation and harmonics. The model is based on the stochastic nature of the electric arc current-voltage characteristic. The generated voltage disturbance signals are applied in this dissertation for testing the relay. In [16] and [17] the transformer switching and capacitor switching responses are modeled for generating inrush and current transients. These are also utilized for testing the relay.

Chapter – 2

Power System Disturbance

2.1 Introduction

To precisely describe the power system disturbance phenomenon some well known defined terminology is adopted. IEC and IEEE [1] made some standards to them and these are adopted in Asia and America respectively. In this dissertation IEC standards are taken.

2.2 Definitions and Sources

Transient[1]**:** Pertaining to or designating a phenomenon or a quantity which varies between two consecutive steady states during a time short compared with the time-scale of interest. A transient can be a unidirectional impulse of either polarity or a damped oscillatory wave with the first peak occurring in either polarity.

Dip[2]**:** A sudden reduction of the voltage at a point in an electrical system followed by voltage recovery after a short period of time from a few cycles to a few seconds.

Swell[3]**:** An increase in RMS voltage or current at the power frequency for duration from 0.5 cycles to 1 min. typical values are 1.1 to 1.8 pu.

Undervoltage: A voltage of a value falling below the lowest rated value.

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[1] IEC 161-02-01
[2] IEC 161-08-10
[3] Not available in IEC but exist in IEEE (1159) standards

Overvoltage: A voltage of a value exceeding the highest rated value.

Waveform Distortion: Any unintentional and generally undesired change in the form of a signal. The main waveform distortions are harmonics, inter harmonics and DC components.

Voltage Fluctuation: A series of voltage changes or cyclic variations of the voltage envelop. Voltage fluctuation may cause the luminance or spectral distribution of a light source to fluctuate with time, thus inducing the impression of unsteadiness of visual sensation of human eyes. This direct sequence is defined as voltage flicker.

Voltage Unbalance: In a poly phase system, a condition in which the RMS values of the phase voltages or the phase angles between consecutive phases are not all equal.

2.3 Illustration of Disturbance Phenomena

The following diagrams demonstrate the waveforms of electrical parameters during disturbances. Most of them come from practical measurements.

Transient: The waveform shown in Figure 2.1 (a & b) were obtained in a distribution system. The transient in current waveform in Figure 2.1(a) was due to capacitor switching in a 10 kV system. In Figure 2.1 (b) a current transient due to energizing of a loaded transformer is shown. This is also called as Inrush current. It was taken from a 13.8 kV system and was simulated in PSCAD™.

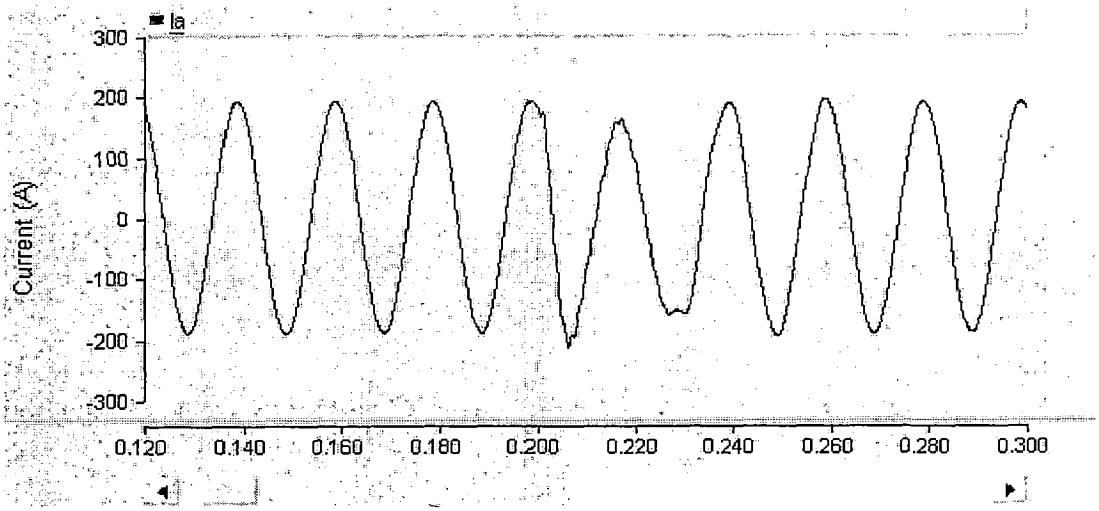


Figure 2.1 (a) Transient due to capacitor switching

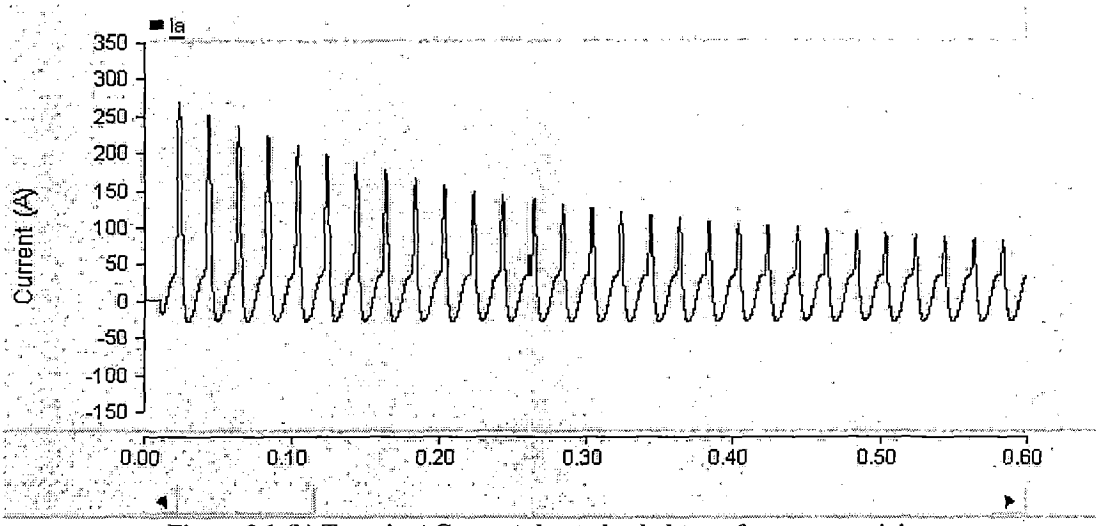


Figure 2.1 (b) Transient Current due to loaded transformer energizing

Dip (Sag): An example of a voltage dip is shown in Figure 2.2. This event was captured from PSCAD™ simulation. This phenomenon was due to a single-phase-to-ground fault in a 230 kV system. The fault was cleared about 4 cycles (80 ms) later.

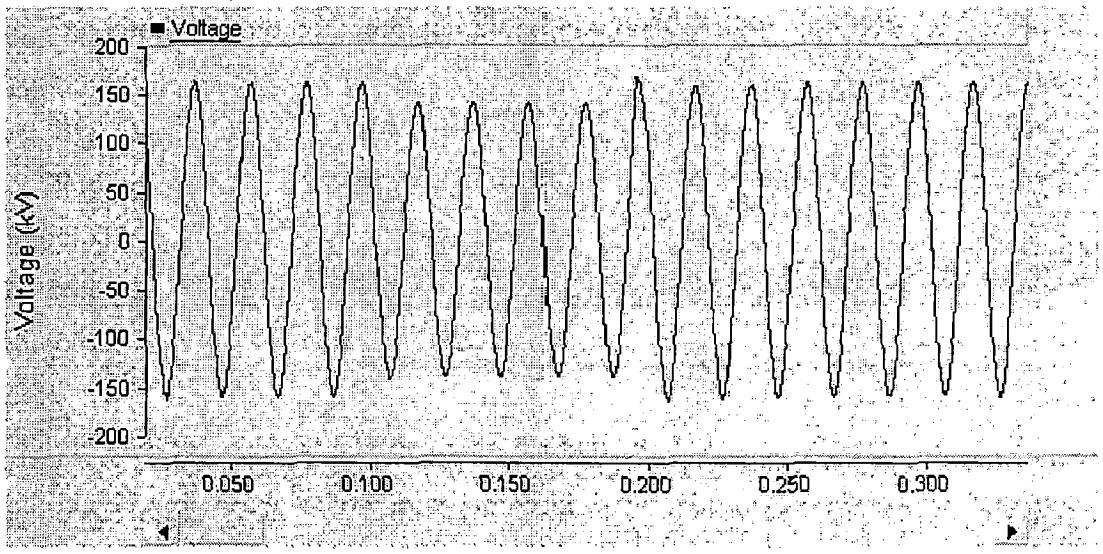


Figure 2.2 Voltage dip due to System Fault

Voltage Fluctuation: Figure 2.3 shows an example of voltage fluctuation. This is measured near an arc-furnace [15]. As the arc-furnace is an intermittent load, its power consumption keeps on changing. The fluctuation in current causes irregular voltage magnitude fluctuations. The situation in the other two phases is similar.

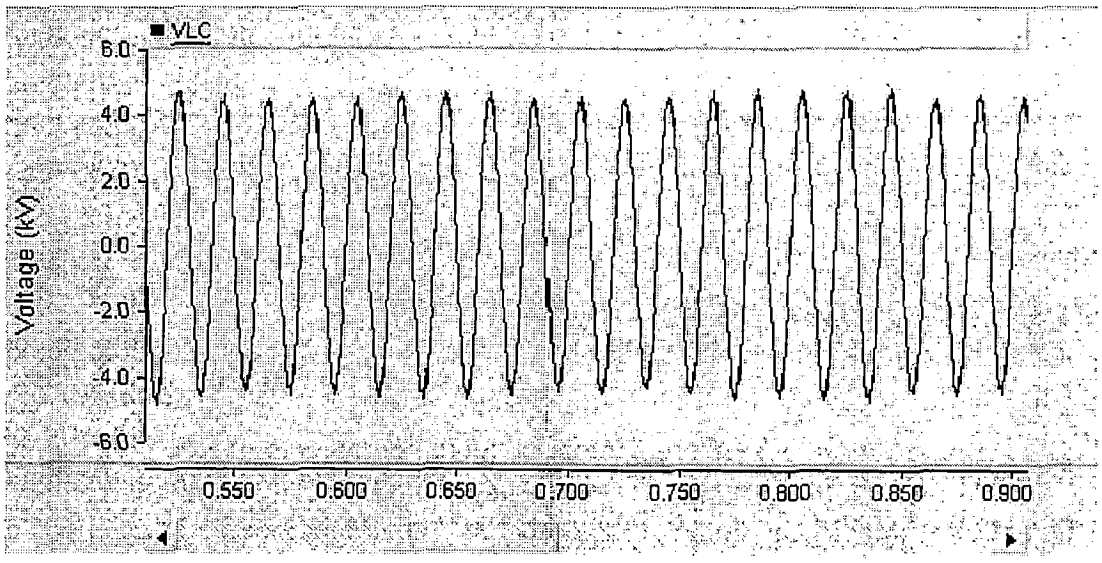


Figure 2.3 Voltage Fluctuation due to arc-furnace

High Frequency Harmonics & Noise: Figure 2.4 shows an example of high frequency harmonics and noise. It is happened due to high frequency switching of load. That causes of introducing high frequency components and/or noise in the current waveform. This is simulated in PSCAD™.

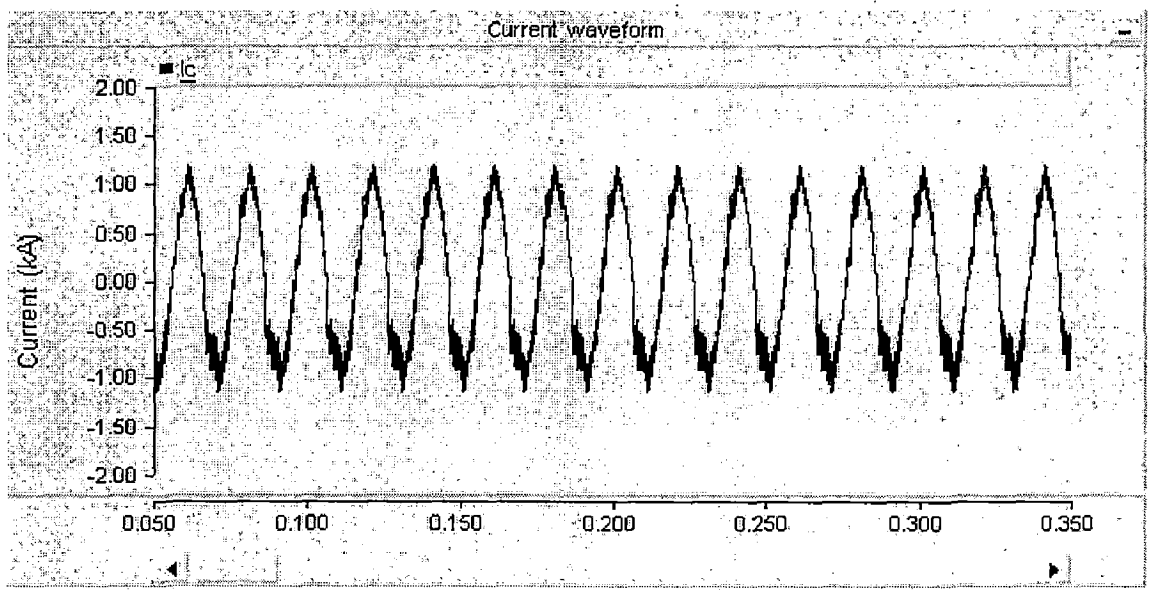


Figure 2.4 High frequency harmonics and noise

Chapter – 3

Digital Protective Relays

3.1 Introduction

Operating voltages and currents flowing through a power system are usually at kilovolt and kilo ampere levels. However, for digital protection it is necessary to reduce the level into digitally manageable levels i.e. less than 5 Volts. So that the analogue signals are converted to digital form, thereby allowing subsequent digital processing to the performed to determine the circuit state.

3.2 Structure of Digital Relay

Any digital relay consists of the following subsystems [2] and is shown in Figure 3.1.

- Signal conditioning subsystem
- Conversion subsystem
- Digital processing relay subsystem

The first two subsystems are generally common to all digital protective schemes, while the third varies according to the application of a particular scheme.

3.3 Signal conditioning subsystem

3.3.1 Transducers

Primary power system currents and voltages are usually relatively high. For digital relays they must be reduced to much lower levels. In normal currents are reduced either to 5A or 1A and voltages are reduced to 100V or 120V. This is

normally achieved by using primary current and voltage transducers (CTs and VTs). Auxiliary transducers are used to further reduction of voltage and current levels to the digital relay level.

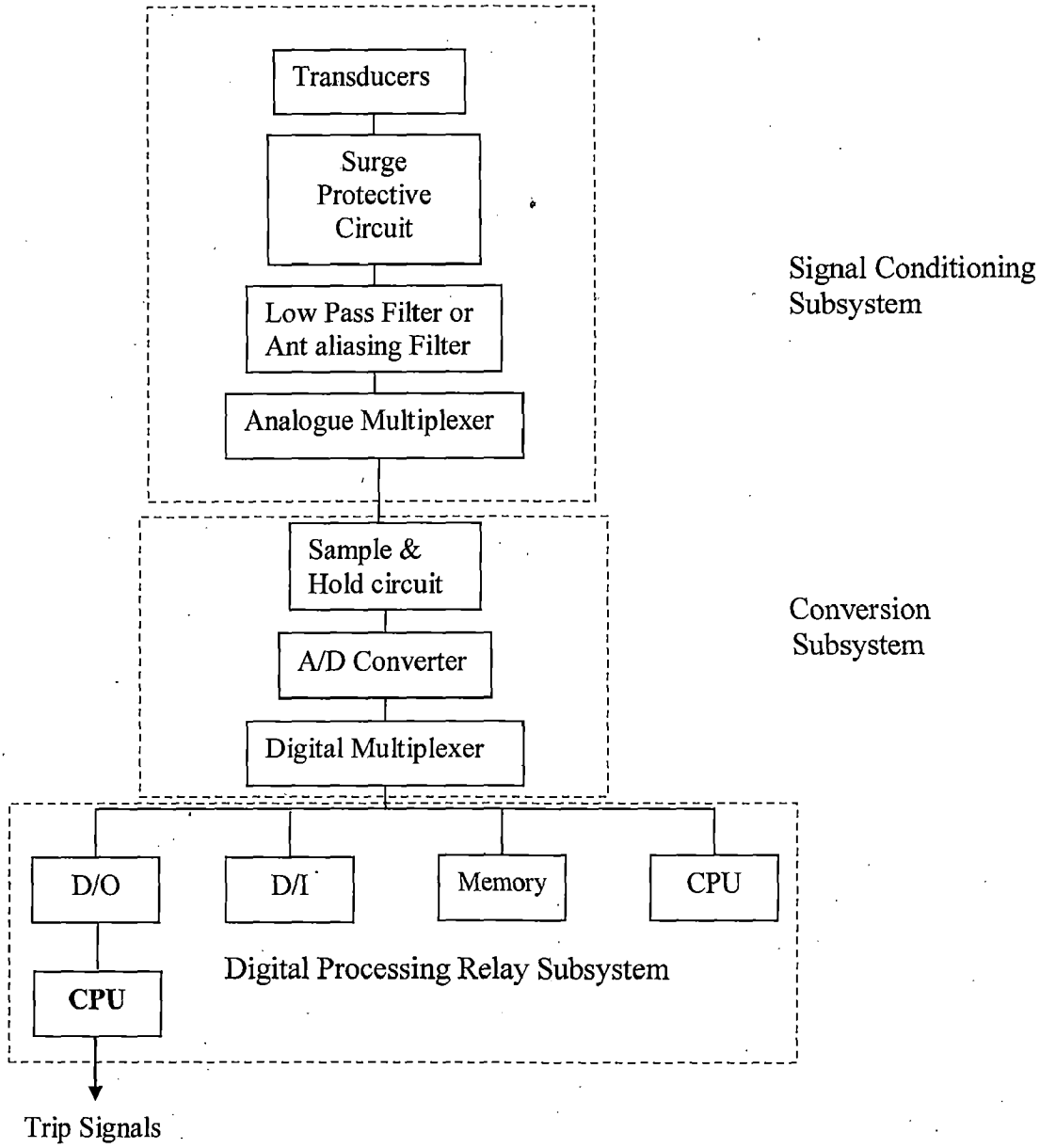


Figure 3.1 Basic Components of Digital Relay

3.3.2 Surge protection circuit

The current and voltage from the secondaries of the CTs and VTs is connected to surge protective circuits, which typically consist of capacitors and isolating transformers. Zener diodes are also commonly used to protect electronic circuits against surges, though their placement depends on the exact physical circuit arrangement used.

3.3.3 Analogue filtering

The analogue filter or anti-aliasing filter [3] is used to avoid possible errors in reconstructing the input signal, which is carried out after the A/D Sample/Hold section. Any signal sampled at a frequency of N*50 Hz can exhibit aliasing when reconstructed, if the signal contains harmonic components of order N±1, 2N±1,...,kN±1. An anti-aliasing filter has to cut off all signal components above the Nyquist rate N/2, i.e. the cut-off frequency for anti-aliasing filter should be set not higher than (N/2)*50 Hz. In practice however, such a filter cannot remove all out of band frequencies so the cut-off frequency for the anti-aliasing filter is typically set at about (N/3)*50 Hz.

3.3.4 Analogue multiplexers

In digital relaying applications, it is usually necessary to use an analogue multiplexer. An analog multiplexer is a device that selects a signal from one of the number of input channels and transfers it to its output channel, thereby permitting the transmission of several signals in a serial manner over a single communication channel.

3. 4 Conversion subsystem

3.4.1 A/D and S/H circuit

To maintain a constant, non-time varying input to be quantized, a sample and hold circuit is often used. An example of S/H is shown in Figure.3.2

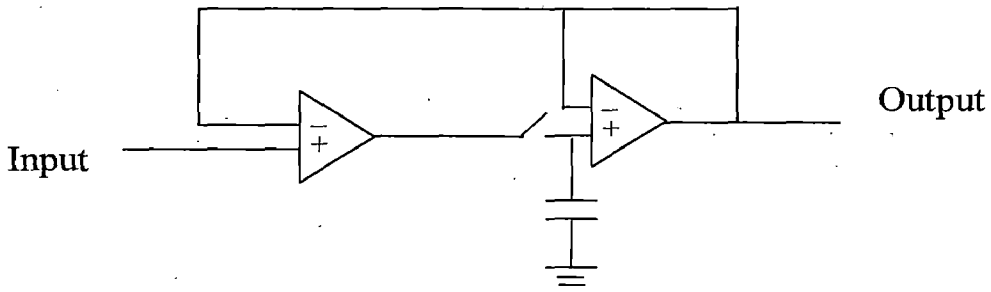


Figure 3.2 Sample and Hold Circuit

The Analog to Digital converter (A/D) is really the heart of the sampling process. The sampled values that represent the continuous time signal are converted to digital binary value by the A/D. The number of bits can be selected according the requirement of accuracy. In real time the current is to be measured from 20% to 4000% [9] of its nominal. So the requirement of accuracy is very high. In this project 12 bits of A/D converter is selected.

The objective of sampling is to measure the instantaneous values of a signal. Both synchronous and asynchronous sampling techniques are used in power system applications, but synchronous sampling is more popular. The consequence of asynchronous sampling is that the accuracy of the estimated values of a signal may be adversely affected if the system frequency deviates from its nominal value.

3.5 Digital Relay subsystem

The digital relay subsystem comprises both hardware and software. The hardware largely consists of a central processor unit (CPU), memory, data input and output (I/O). The software is influenced by two major factors. Figure 3.3 shows an example of a flow-chart for the software of a typical digital protective relay. The algorithms used and the software required vary significantly according to the application.

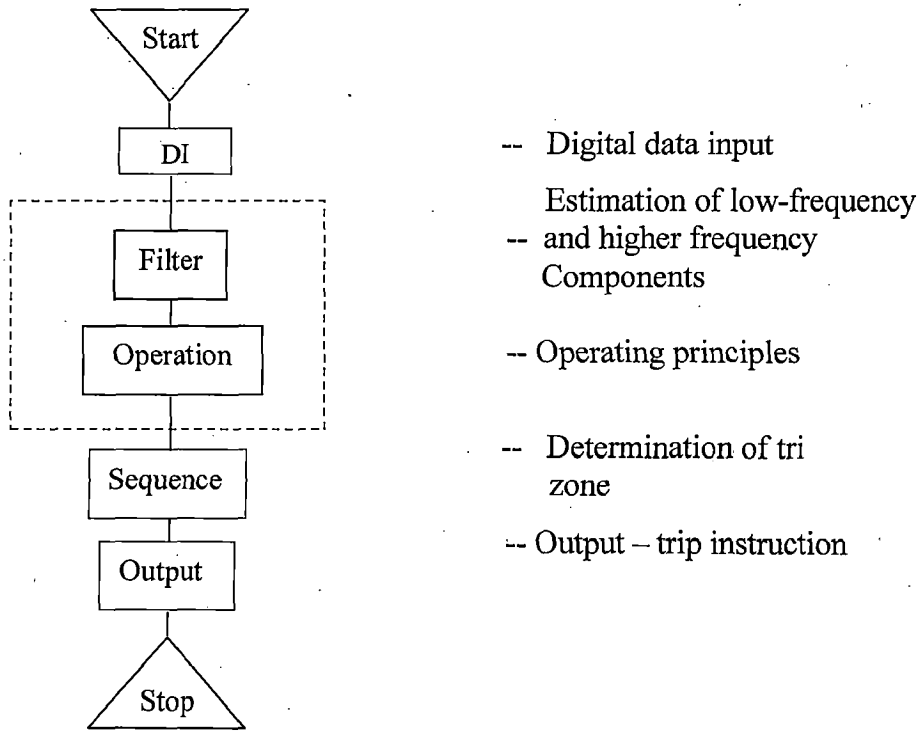


Figure 3.3 Flow-chart for the software of a digital protective relay

3.6 Estimation of Current and Voltage Phasors

3.6.1 Window technique

To scan the whole signal, a data window [3] of limited length is applied to acquire information on part of the signal. Within the section of the signal that is scanned by the data window, a limited number of points of the waveform are sampled. With the window moving forward, more samples are obtained at different snapshots of time. In figure 3.4, it is illustrated that the input signal is frozen by the data window to achieve simultaneous sampling at each moment, when the oldest sample point is discarded and the newest one is embedded. These samples are held until the next sampling moment. The sampling window length, sampling number in the window as well as the shape of the sampling window is dependent on the relay algorithm stored in the processor.

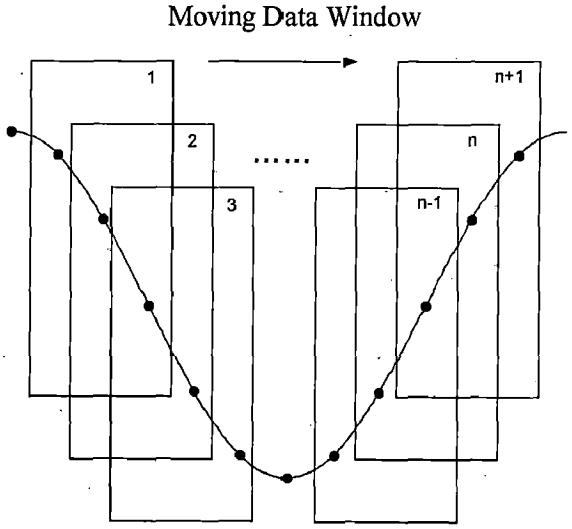


Figure 3.4 Data window for sampling

The relay algorithm stored in the processor is the core of the digital relay. It determines the way to reconstruct the input signal based on the digital samples form the A/D converter. As the input signal may contain unwanted components such as harmonics, interharmonics and DC, the algorithm is designed to remove

them as much as possible. The algorithm functions as a digital filter to extract the fundamental component of the input signal, based on which the relay operation is carried out. With different algorithm principles, the shape of data window varies. The rectangular window, as shown in figure 3.4, is only one option. The length of the data window is dependent of the required decision speed and accuracy of the algorithm. The number of sampling points in the data window is determined by the sampling frequency set in the algorithm.

In digital output system, the reconstructed signal from the digital filter is compared with the pre-set threshold. The decision on whether the relay should operate is made according to this comparison.

The window size can be selected according to requirement. The requirement is the sense of fast and accuracy. There exists a trade of between fast and accuracy. And here most commonly used window sizes will be explained. Those are 1. Half cycle window and 2. Full cycle window [4]

3.6.2 Half cycle window verses Full cycle window

The Discrete Fourier Transform has the capability of working on different sized "windows". The DFT will be described later. The Full Cycle window generates the sums using all the sampled data collected over the last cycle. This means that the "window" includes the last full cycle's worth of data.

The Half Cycle window generates the sums using the sampled data collected in the last half cycle. Therefore, the data "window" is a half cycle. Using a Half Cycle window allows the Discrete Fourier Transform to more quickly track a change in the sampled data than is possible with a Full Cycle window.

However, there are differences in the filtering actions of the Half and Full Cycle filters. For example, the Half Cycle Fourier is subject to errors due to dc offset and even harmonics of the fundamental frequency. Both the Full and Half Cycle Fourier may be implemented as either a Recursive or Non-recursive filter.

3.6.3 Discrete Fourier Transform technique

This technique is used to eliminate the unwanted components in the original signal i.e. it is required to extract the fundamental component from the signal to make the decision for the relay.

The main concept of Fourier filter [5] is that any signal can be regarded as a combination of periodic cosine and sine components, the fundamental components can be expressed as

$$Y = \frac{2}{K}\sum_{k=1}^{K} y(k)e^{-jk\frac{2\pi}{K}} \qquad \ldots (3.1)$$

Y is a complex number that represents the signal in phasor representation. The magnitude equals to the amplitude of the given input signal of y(k) (k^{th} sample). The equation 3.1 can be separated into real and imaginary components as shown in equation 3.2.

$$Y = \frac{2}{K}\left(\sum_{k=1}^{K} y(k)\cos\left(\frac{2\pi k}{K}\right) - j\sum_{k=1}^{K} y(k)\sin\left(\frac{2\pi k}{K}\right)\right) \qquad \ldots (3.2)$$

The DFT can be applied to both current and voltage waves. That gives the phasor of both waves. The DFT can be applied in two different ways [6]

1. Non-recursive method
2. Recursive method

3.6.4 Recursive verses Non-recursive

The Non-recursive method requires that each sampled data point be saved in memory (amount of data is determined by the "window" size) and that the entire coefficient multiplication and summation process be performed every sample. The newest sample becomes the N^{th} sample; the oldest sample is dropped from the calculation. The real and imaginary terms must be recalculated from the beginning.

The Recursive method requires that the product of the sine and cosine coefficients and the sample data values used to generate the sums are saved (the amount is still determined by the "window" size) and an abbreviated summation process is performed. In this method, the oldest product is removed from the sum and the newest product is added into the sum.

With this Recursive implementation, only the product for the newest sample needs to calculate instead of recalculating the values for all the samples in the "window". This reduces the amount of calculations performed. Therefore, the time required to complete this process is also reduced enabling the relay to perform additional tasks or increase its sampling rate. The Non-Recursive method, on the other hand, requires more time and/or computing speed to complete.

3.6.5 Recursive approach

The computational cost can be made independent of N (samples/cycle). The different categories are possible, depending on whether the time origin moves with the window or remains fixed.

3.6.5.1 Shifting time origin, constant coefficients

By evaluating equation 3.1 at two consecutive instants and subtracting, the following algorithm can be obtained.

$$X_n(k)^L = [X_{n-1}(k) + x(n)e^{-2j\pi kL} - x(n-N)]e^{j\frac{2\pi k}{N}} \quad \ldots (3.3)$$

Assuming real data, the above complex expression can be written in terms of real and imaginary parts as follows

$$C_n(k)^L = (C_{n-1}(k)^L + \Delta x_n)\cos\theta_k - (S_{n-1}(k)^L + x(n)\sin(2\pi kL))\sin\theta_k$$
$$S_n(k)^L = (C_{n-1}(k)^L + \Delta x_n)\sin\theta_k + (S_{n-1}(k)^L + x(n)\sin(2\pi kL))\cos\theta_k \quad \ldots (3.4)$$

Where $\Delta x_n = x(n) - x(n-NL)$ & L is the Window Length L=1 means Full cycle.

3.6.5.2 Fixed time origin, varying coefficients

The DFT can be also defined with respect to static time origin, leading to periodically varying coefficients.

$$X_n(k)^L = \sum_{i=0}^{NL-1} x(n - NL + 1 + i)e^{-j\frac{2\pi k(n-NL+1+i)}{N}} \quad \ldots (3.5)$$

A recursive expression for this transform can be obtained as

$$X_n(k)^L = X_{n-1}(k)^L + [x(n)e^{-j\frac{2\pi kn}{N}} - x(n-NL)e^{-j\frac{2\pi k}{N}(n-NL)}]$$

For the real data case, the following expressions are obtained

$$C_n(k)^L = C_{n-1}(k)^L + x(n)\cos\theta_k - x(n-NL)\cos(\theta_k + 2\pi L)$$
$$S_n(k)^L = S_{n-1}(k)^L - x(n)\sin\theta_k + x(n-NL)\sin(\theta_k + 2\pi L) \quad \ldots (3.6)$$

Note that N memory locations are also needed by recursive algorithms to obtain Δx_n. The output magnitude of such Fourier filter can be calculated as

$$|X(k)^L| = \frac{2}{NL}\sqrt{(C_n(k)^L)^2 + (S_n(k)^L)^2} \text{ and } \delta^L = \tan^{-1}(S_n(k)^L/C_n(k)^L)$$

In terms of phasor representation

$$X(k)^L = \frac{2}{NL}(C(k)^L + jS(k)^L) \quad \ldots (3.7)$$

These are the generalized formulae for all types of window lengths.

3.6.6 Frequency response of DFT Filters

The Fourier filter uses moving a sampling window to scan the input signal. The decision making time of the relay is dependent on the length of the sampling window.

The frequency response of all types of DFT filters can be shown in figure 3.5

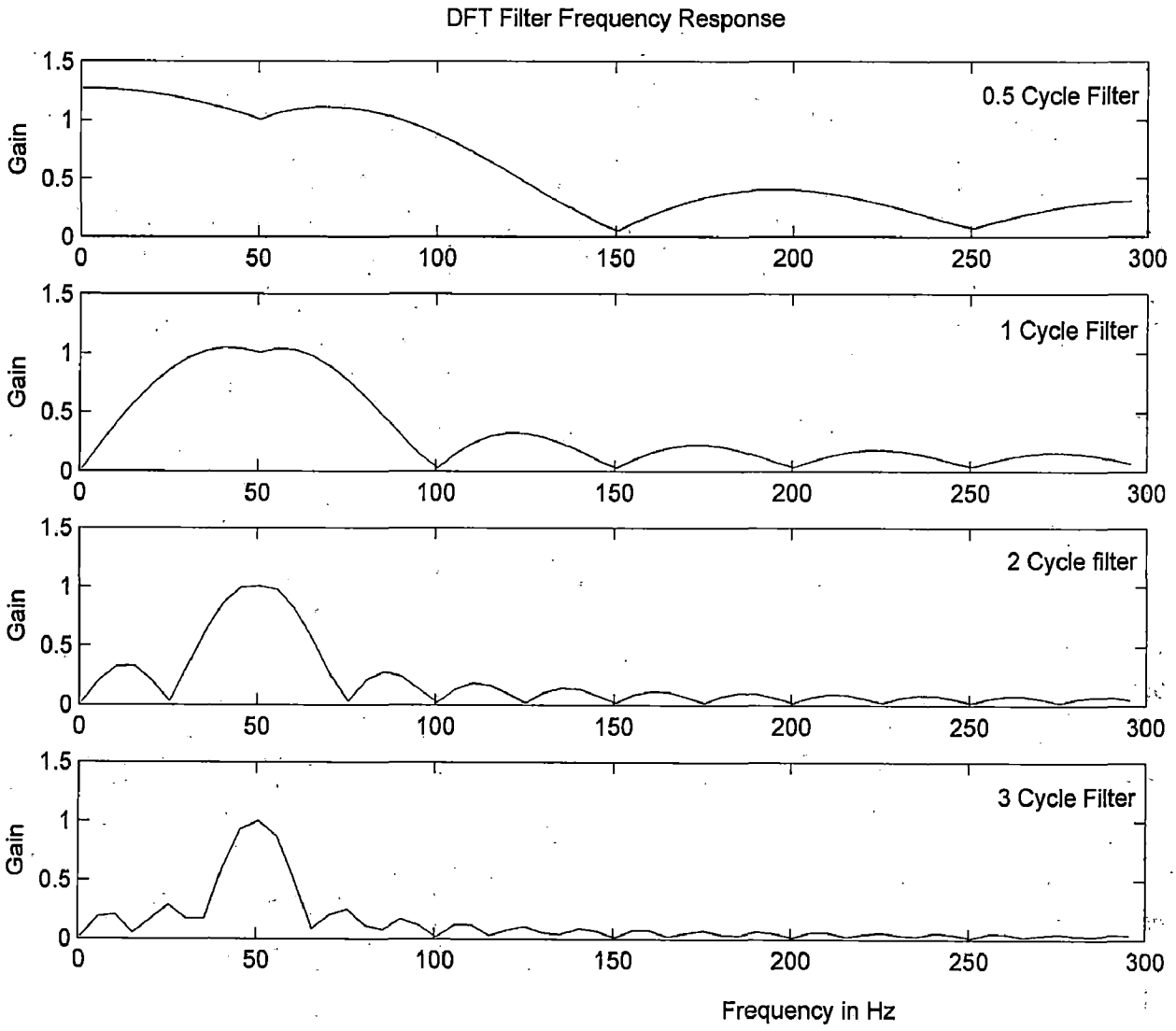


Figure 3.5 Frequency response of all types of DFT Filters

From figure 3.5 we can observe that

Table 3.1 Capability of filter in removing disturbances

	½ Cycle	1 Cycle	2 Cycle	3 Cycle
Odd Harmonics	Yes	Yes	Yes	Yes
Even Harmonics	NO	Yes	Yes	Yes
DC	NO	Yes	Yes	Yes
1/2 interharmonics	NO	NO	Yes	NO
1/3 interharmonics	NO	NO	NO	Yes

From the above table it can be observed that One-Cycle filter is the best suitable one for all types of filters. Because it is faster than 2 and 3 cycle filters. Even though it is having less accurate than 2 and 3 cycle filters it is enough to get better response for a digital relay.

3.6.7 Differential Equation Algorithm

Unlike Fourier algorithm which is based on the description of the waveform, differential equation algorithm [8], [2] is based on a system model. The studied line is modeled as an R-L series connection by the following differential equation

$$Ri + L\frac{di}{dt} = v \qquad \ldots (3.8)$$

To determine the values of R and L using this equation 3.8, it is basically required to have at least two sets of voltage and current samples. Let v_k, i_k be the voltage and current samples at time t_k and let Δt be the sampling time interval. The derivative of the current with respect to time $\frac{di}{dt}$ can be approximately determined as shown in equation 3.9.

$$\frac{di}{dt} = \frac{i_{k+1} - i_{k-1}}{2\Delta t} \quad \ldots (3.9)$$

Therefore using sample notations equation 3.9 becomes

$$v_k \cong Ri_k + L\frac{(i_{k+1} - i_{k-1})}{2\Delta t} \quad \ldots (3.10)$$

Similarly by using the following sets of samples at t_{k+1} equation 3.10 becomes

$$v_{k+1} \cong Ri_{k+1} + L\frac{(i_{k+2} - i_k)}{2\Delta t} \quad \ldots (3.11)$$

In matrix form, equations 3.10 & 3.11 can be combined to give

$$\begin{bmatrix} i_k & \frac{(i_{k+1} - i_{k-1})}{2\Delta t} \\ i_{k+1} & \frac{(i_{k+2} - i_k)}{2\Delta t} \end{bmatrix} \begin{bmatrix} R \\ L \end{bmatrix} = \begin{bmatrix} v_k \\ v_{k+1} \end{bmatrix} \quad \ldots (3.12)$$

By solving equation 3.12

$$R \cong \frac{v_k(i_{k+2} - i_k) - v_{k+1}(i_{k+1} - i_{k-1})}{i_k(i_{k+2} - i_k) - i_{k+1}(i_{k+1} - i_{k-1})}$$

$$L \cong 2\Delta t\left(\frac{i_k v_{k+1} - i_{k+1} v_k}{i_k(i_{k+2} - i_k) - i_{k+1}(i_{k+1} - i_{k-1})}\right) \quad \ldots (3.13)$$

Compared with the Fourier algorithm the differential equation algorithm is faster and more suitable for transient conditions. However, the approximation of the line as an ideal R-L loop somewhat affects the accuracy of this algorithm. Both of them have application in line relaying.

Differential Equation algorithm is not accurate for the higher frequencies. It doesn't give exact R & L values when the voltage and/or current waves having higher frequencies. So it is better to use a filter to avoid such frequency components. Generally Fourier filter is used to reduce those components. So the combined type of filter will give faster and accurate response.

Chapter – 4

Hardware Description

4.1 S/H and A/D Conversion

Analog to Digital conversion is the heart of any digital signal processing. In this dissertation TMS320C10 [18] processor is used to convert the analog to digital signal. A sample and hold circuit is done through analog switch and high speed buffer. As the End of Conversion comes the sample and hold amplifier which is used in the S/H, starts sampling, whereas on Start of Conversion the hold capacitor provides the analog input through the high speed buffer.

Here in this dissertation the A/D is on board, uses the successive approximation technique by using the data in EPROM simulating a 12 bit SAR. On each trail D/A output is neutralized with the D/A reference input and checks the output of the comparator. The End of Conversion is available on $D15^{th}$ bit which can be read by the program. The D0 to D11 contains the data.

The current range in any power system is about 20% to 4000% of its nominal and measurement has to be done with an accuracy of 1%. So 12 bit or more, required for getting the desired requirement. 6400 Hz sampling frequency is selected for both current and voltage waves. The conversion time of A/D per sample is approximately 28μs.

4.2 8253

There are two types in sampling technique. They are Synchronous and another one Asynchronous technique and were discussed in section 3.4.1. Because of

synchronous technique is having advantage over asynchronous, synchronous is used. For that it is required to generate a clock of certain frequency. 8253 is most commonly used timer. It is having three independent 16-bit counters. In that timer1 is used for generating SOC (Start of Conversion). This signal is also used to select the channel (Voltage and Current) by 7493 counter. To get 128 samples per cycle per channel, it is required to take each sample with a gap of 78.125 μs.

4.3 Active Low-pass filter (Anti aliasing Filter)

The sampling rate in a sampled-data system is an important parameter to be considered. Theoretical considerations dictate that the sampling frequency (f_s) must be at least twice the largest frequency (f_m) present in the sampled information to avoid aliasing errors. According to Nyquist criterion in practice the cut off frequency should be one third of the sampling frequency. A low-pass filter is used to avoid aliasing error in a sampled data system. The low-pass filter can be passive, consisting of resistance and capacitance exclusively, or active ones utilizing operational amplifiers. Figure 4.1 shows the circuit of an active low-pass filter. The cut-off frequency f_c of this filter is given by

$$f_c = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} \qquad \ldots (4.1)$$

The sampling frequency is 6400 Hz. For this it is required to select the cut off frequency as 2.1 kHz. To verify the performance of the relay for different sampling frequencies the cut off frequency is selected as 1.6 kHz.

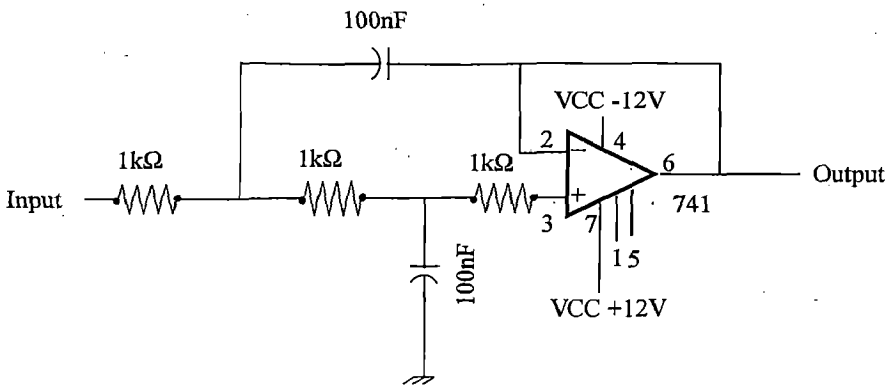


Figure 4.1 Active Low-pass Filter

4.4 Overvoltage Protection

Electronic circuits are needed to protect from overvoltages. The voltage levels should not be more than the specified limit. To protect the same the selection of suitable ratings of the Zener diodes and resistance R is needed. In the circuit shown in Figure 4.2, two Zener diodes are connected back to back, i.e. one is forward biased and another one is reverse biased. If the peak voltage is to be limited to 5 V and the voltage drop in the forward biased Zener is 0.6 volt, the reverse biased Zener will take (5-0.6) = 4.4 V. Selecting a Zener diode of 4.9 V rating the resistance R is calculated. The R value is approximately 4.7 Ω.

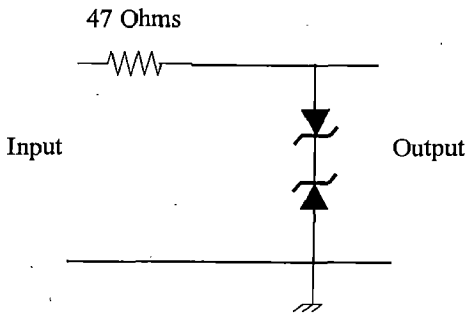


Figure 4.2 Overvoltage protection circuit

4.5 Analog Multiplexer

Voltage and current signals have to be supplied to the distance relays. They must be sampled alternatively by A/D converter for getting continuous signals. So it required for time multiplying single channel supply of voltage and current signals.

AM3705 is an analog multiplexer that can be used to multiplex the two signals by selecting address of the channel and Output Enable pins.

4.6 Programmable Peripheral Interface (8255)

The Intel 8255 is a single chip programmable peripheral interface (PPI) [19] that provides three programmable I/O ports. Using these three ports it is easy to send the digital data of 12 bit to Personal computer. Port - A pins are connected to data pins of parallel port. Being lesser availability of pins i.e. 8 pins, 12 bit data can be sent in two times. B5 of port B is connected to pin 10 of parallel port. It is taken for sending 'Request to send' (RS) signal. C4 of port C is connected to pin 1 of parallel port. It is connected though a 7404 NOT gate. Because pin 1 of parallel port is hardware inverted pin. It is taken for receiving 'Request to receive' (RR) signal.

All these things are considered for handshaking between A/D converter and the Personal computer.

The below algorithms are required to send and receive the data perfectly between the A/D converter and PC.

ALGORITHM FOR DSP KIT:

1. INITIALIZE TIMER FOR 80μs TIME INTERVALS
2. WAIT FOR OUTPUT (DIGITAL)
3. MAKE AVAILABLE THE LOWER BYTE IN 8255-I (PORT A)
4. MAKE RS=0 (PORT B)
5. GOTO 5 TILL RR=1 (PORT C)
6. MAKE AVAILABLE THE UPPER BYTE IN 8255-I (PORT A)
7. MAKE RS=1 (PORT B)
8. GOTO 8 TILL RR=0 (PORT C)
9. GOTO 2.

ALGORITHM FOR PC:

```
CHP=0;
RR=0;
WHILE(1)
{
        DO{
        WHILE(RS!=0) { }
        RECEIVE LOWER BYTE DATUM;
        RECEIVE CH;
        RR=1;
        WHILE(RS!=1)
        RECEIVE HIGHER BYTE DATUM;
        RR=0;
        }WHILE(CH==CHP);
        CH=CHP;
        MANUPLATE DATA;
}
```

The block diagram of the model is shown in figure 4.3.

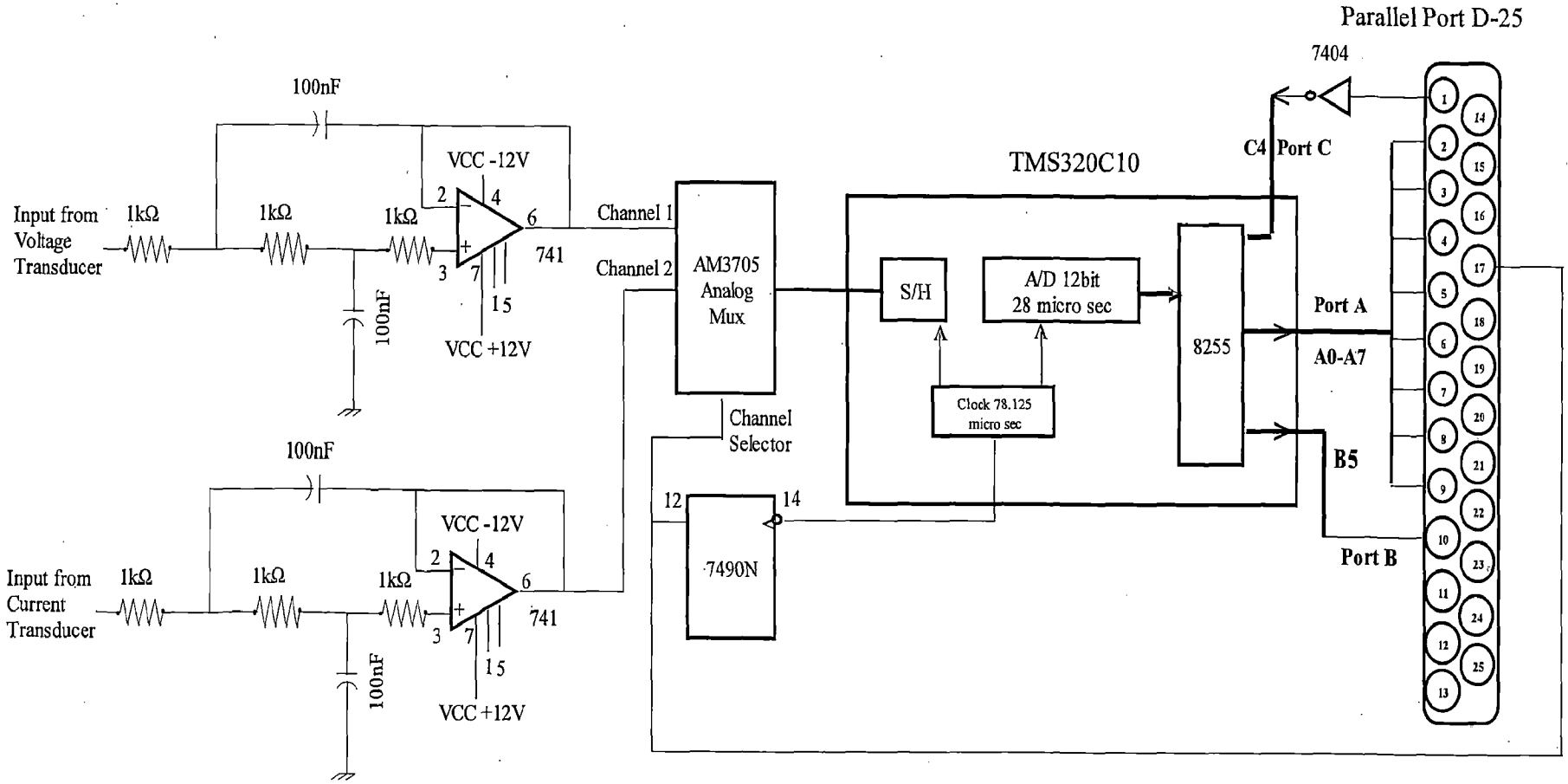


Figure 4.3 Block diagram of duel element digital relay hardware

Chapter – 5

Quantification of Disturbances in Protection

5.1 Introduction

A disturbance may cause relay mal-trip or fail-to-trip, depending on the particular case. If the disturbance that causes relay mal-trip is due to a fault, it will lead to the loss of the faulted as well as the non-faulted component. For other disturbances, several relays may react in the same way. The loss of multiple components in a transmission system may cause a large-scale Blackout. The risk of a mal-trip due to a disturbance is minimized during the design process of a relay (mainly through the use of filters) and by a conservative choice of threshold and time delay settings. All this typically leads to an increase of the fault-clearing time and greater risk of fail-to-trip. Actually, generating a tripping signal too late (e. g. exceeding the critical fault-clearing time in angular stability) is also considered as a fail-to-trip event. To make an accurate trade-off between fail-to-trip, fault-clearing time and mal-trip, a detailed knowledge is needed of voltage and current disturbances at the relay terminals. Assessment of disturbance impact on relays can in no doubt facilitate the choice of proper relay parameters.

5.2 Two Ways of Quantification

To assess the disturbance impact [10] on relays, relay testing under the disturbance condition is necessary. For this it is needed to have disturbance database to test the relays. The output of the relays is generally trip or non-trip. By this we can evaluate the impact factor of disturbance on that particular type of relay. A

disturbance might not lead to relay mal-trip as a final result, but make the relay characteristics shifted near the critical boundary of mal-trip, which is also potentially risky. Also possible is that a disturbance that causes no mal-trip for a certain type of relay may lead to mal-trip for another relay type, due to the trade-off between relay speed and security.

The assessment of disturbance impact can be made in two ways [10], [11] & [13]. A disturbance may cause the measured parameter to falsely enter the relay tripping zone, leading to a mal-trip. The approach based on this effect is referred to as "setting-based quantification". Disturbances will affect the relay operation in another way as well. A digital relay can be seen as a filter that extracts the desired component from the measured voltages and/or currents. The presence of a disturbance will produce an error in extracting the desired component. This approach is referred to as "design based quantification".

5.2.1 Setting-Based Disturbance Quantification

In practical installation, the main concerns are whether the disturbances may trigger the relay protection by falsely entering the protection tripping region. In this study, disturbance means a voltage and/or current signal with a short-term transient, or a long-term distortion, or both. To evaluate the disturbance impact, it is necessary to study the possible impact region for disturbances.

5.2.1.1 Disturbance impact Factor

Figure 5.1 & 5.2 give two examples of disturbances for overcurrent and impedance relays respectively.

Figure 5.1 shows voltage dip results a disturbance in both voltage and current signals. With the dip in voltage causes increase or decrease in the current. The increase or decrease in current depends on the situation. Here in this example raise in current is taken. This is happened due to a single line to ground fault.

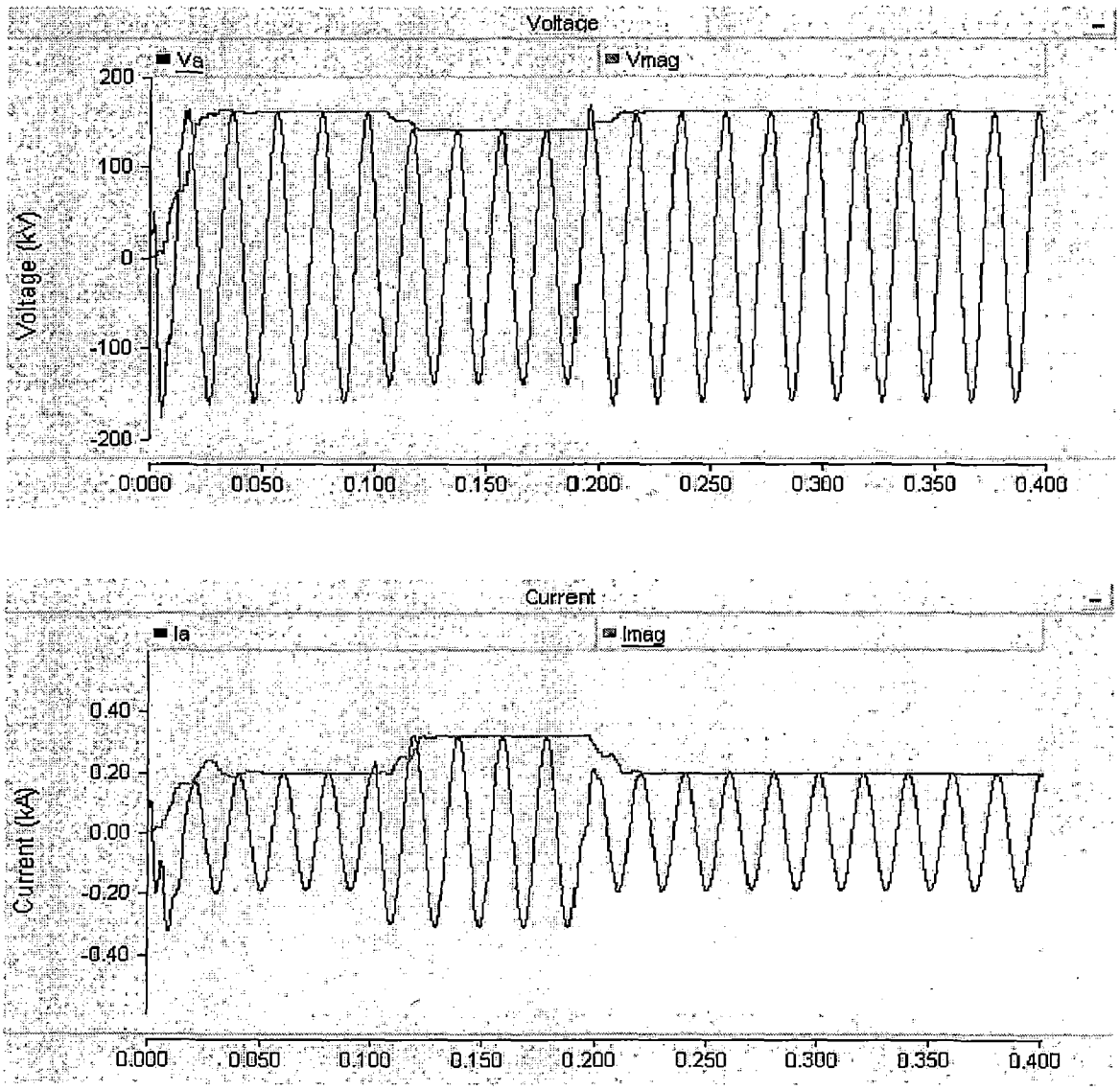


Figure 5. 1 Voltage Sag (Both Current and Voltage waves) & their fundamental component magnitude extraction by Fourier one cycle Filter.

The output curve is obtained by applying the Fourier algorithm filter to the current waveform. A sampling window length of 1 cycle has been used. The diagram demonstrates that such a relay can remove the spikes on the waveform of the input signal. However the output shows transient characteristics at the beginning and end of the dip period. As the sampling window is of 1 cycle length, the output within 1 cycle after any sudden change or transient in the signal is inaccurate.

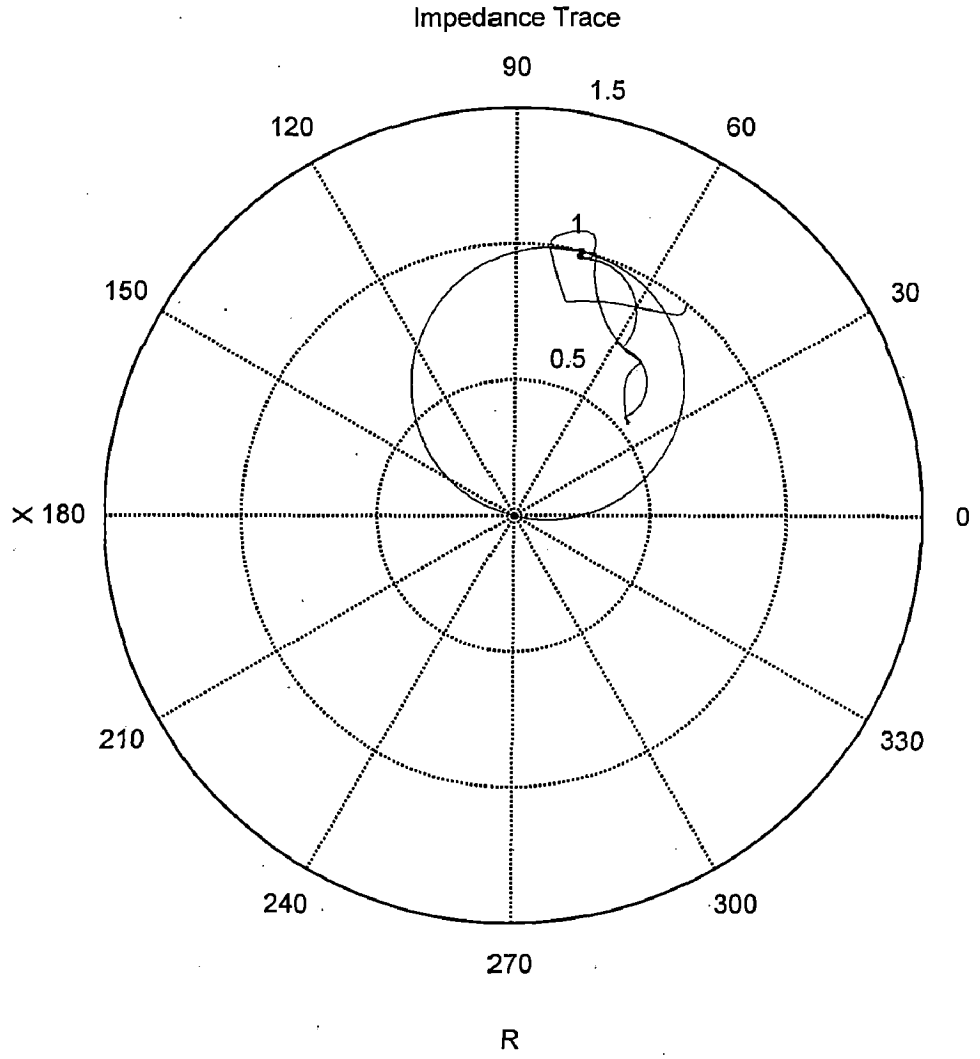


Figure 5. 2 The impedance Trace and the mho circle of angle 75 degrees and line impedance = 1 unit.

The apparent impedance observed by the relay filter moves around the R-X plane during the disturbance before it returns to a place near the original starting point. The impedance trace is obtained by applying the Fourier Filter algorithm.

The status at both the beginning and the end of the measurement window are considered stable for at least one cycle; the variation in the signal in between determines the impact on relay operation. The severity of the disturbance is given relative to a steady state value. Either the pre-disturbance or the post disturbance value is used, whichever one is more severe. Two examples are given in Figure 5.3 and 5.4.

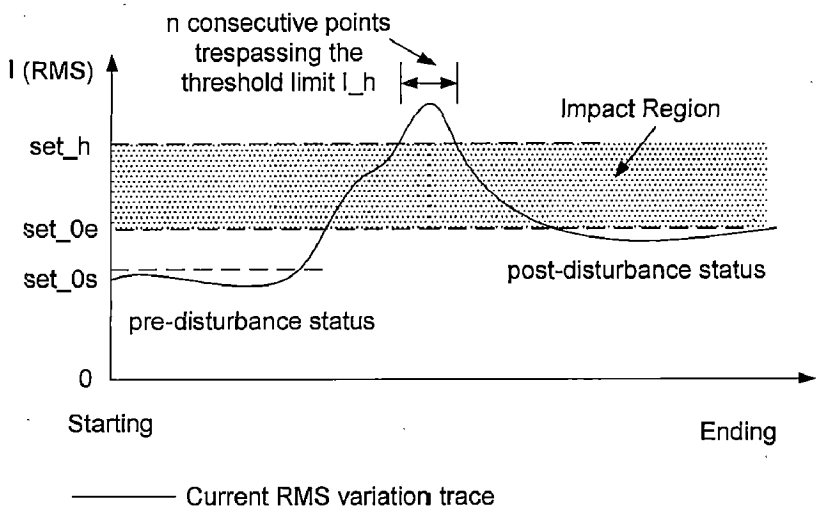


Figure 5. 3 Impact region for overcurrent relay

In Figure 5.3, a relay filter output is shown as a curve. During a certain part of the disturbance, the relay filter output exceeds the pre-disturbance and post-disturbance levels. A time delay is adopted for verifying the decision. In digital relaying, such a time delay means a certain number of consecutive points that are above the pre-set threshold. By moving a line parallel to the time axis up

In Figure 5.4, the relay output is shown as an impedance moving trace. Similarly as in Figure 5.3, a setting region can be located inside which a pre-defined number of consecutive points fall during the disturbance. The diameter of such a region (as MHO setting region is a circle) is defined as set_h. The diameters of the two imaginary circles, on which the pre-disturbance and post-disturbance status points locate, are defined as set_0s and set_0e respectively.

To quantify the severity of an impact, a disturbance factor D is introduced. Let set_0 = max (set_0s, set_0e), or set_0=min (set_0s, set_0e), depending on the type of protection, then the disturbance factor is defined [10] as:

$$D = | (set\_h - set\_0)/set\_h | \qquad (5.1)$$

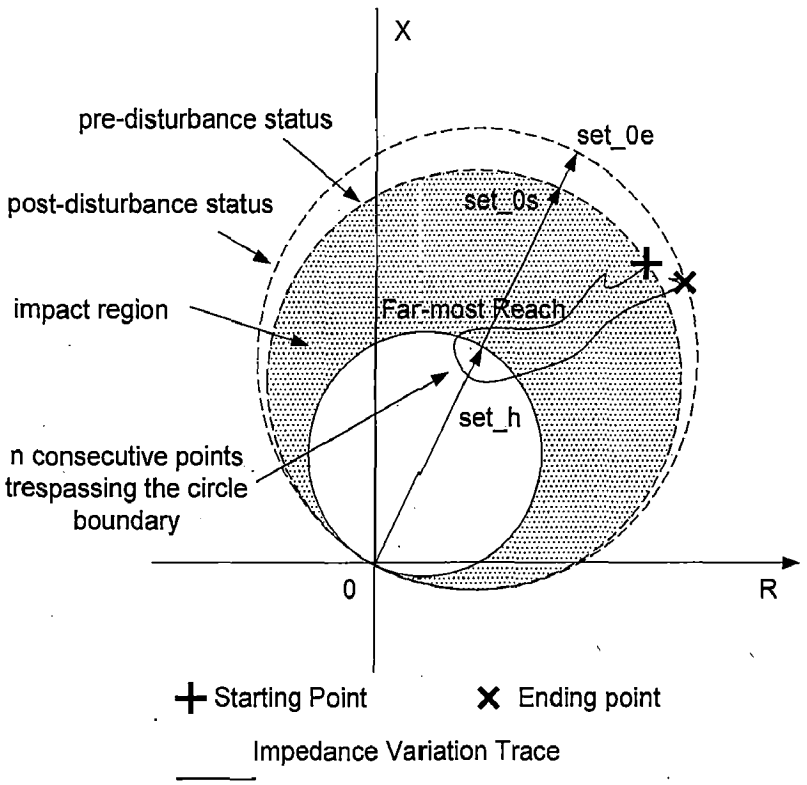


Figure 5. 4 Impact region for impedance relay

Figure 5.3shows an impact region starting from the post-disturbance value. In Figure 5.4, the impact region is counted from the pre-disturbance point because it is closer to the setting region compared with the post-disturbance point.

5.2.2 Design-Based Disturbance Quantification

An important part of the design of digital relays involves the extraction of the fundamental component by a digital filter. Whatever the cause of the disturbance, it is just regarded by a digital filter as a (group of) input signals that contain not only the fundamental component, but also the other unwanted ones. Among the unwanted components, some can easily be removed while others can appear in the filter output. The design-based quantification aims at short listing the signals containing difficult-to-remove components. The following section describes the way to assess the impact of these components on relay output characteristics.

5.2.2.1 Disturbance impact factor

The window size and shape significantly affect the filter output. This is shown in Figure 5.5 where the amplitude of the fundamental component is plotted for cosine/sine windows of different size, together with the (time domain) disturbance factor.

$$\hat{Y}_c = \frac{2}{LK}\sum_{k=1}^{LK} y_k \cos(k\theta) \qquad \ldots(5.2)$$

$$\hat{Y}_s = \frac{2}{LK}\sum_{k=1}^{LK} y_k \sin(k\theta) \qquad \ldots(5.3)$$

Where $\theta = 2\pi/K$, L is the multiple size of the window, K is the number of sampling point per cycle.

Plots (a), (b), (c) and (d) in Figure 4.5 are obtained by applying Fourier filters with window lengths 0.5, 1, 2 and 3 cycles respectively. The plots show a strong oscillation for a half-cycle window, but only minor oscillations for longer window lengths. Extending the window length from one to three cycles doesn't further reduce the oscillations. Note that these conclusions only apply to this specific signal and may not necessarily hold generally.

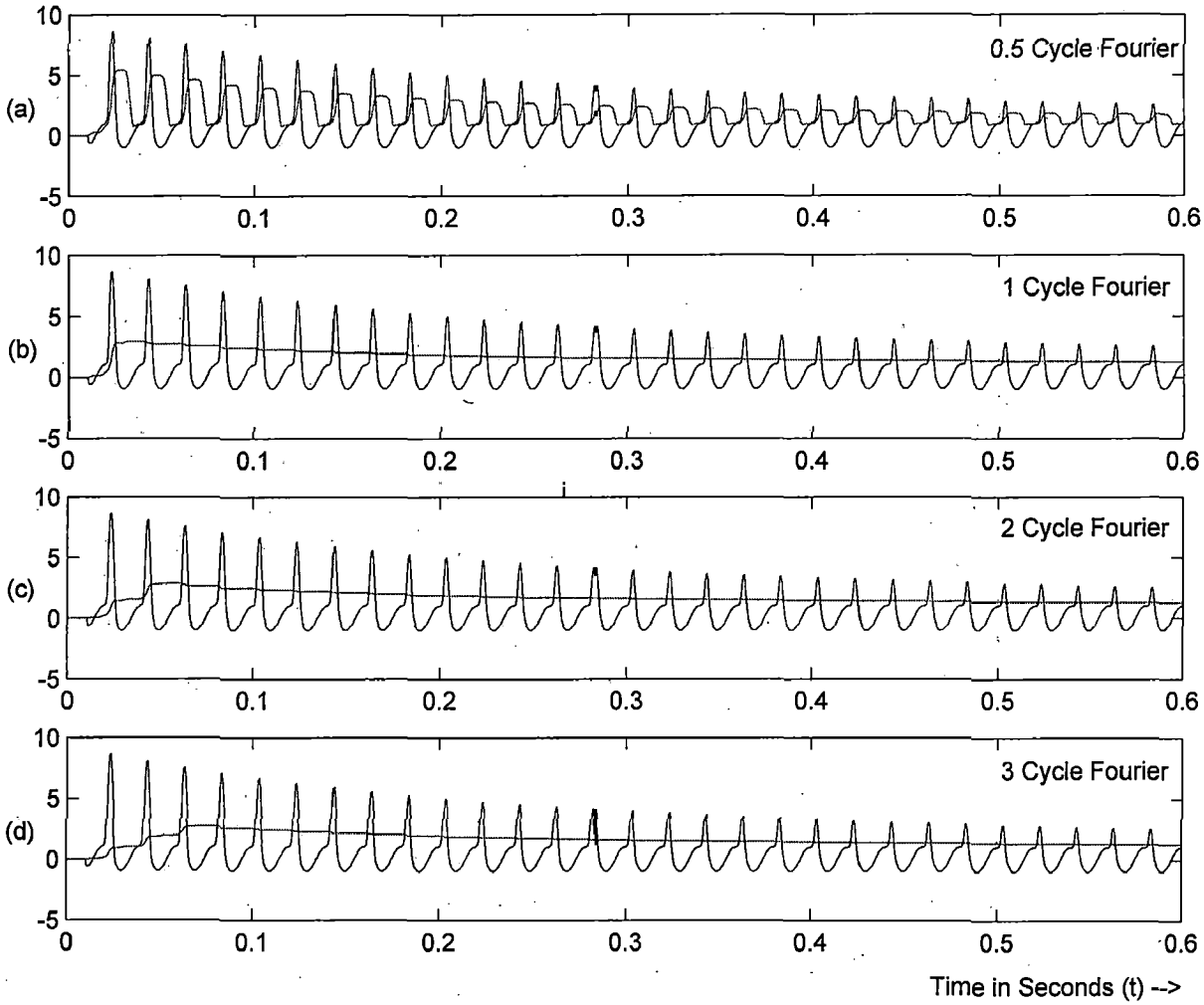


Figure 5. 5 Outputs of the Filtered Signal by different filters

Corresponding to relay output characteristics [11], different filters may yield different results. An example is shown in Figure 5.6 where the output characteristics of both 1-cycle Fourier filter and another filter (0.5-cycle Fourier filter) with different sampling window size are compared.

In the figure, the knee point corresponds to the setting limit. It means a relay which, equipped with a certain type of filter and a certain time delay for decision-making, will not operate if the actual setting is greater than this limit. From the figure it can be observed that the type of relay filter may affect the output performance obviously. Most relays are designed to operate under fundamental frequency.

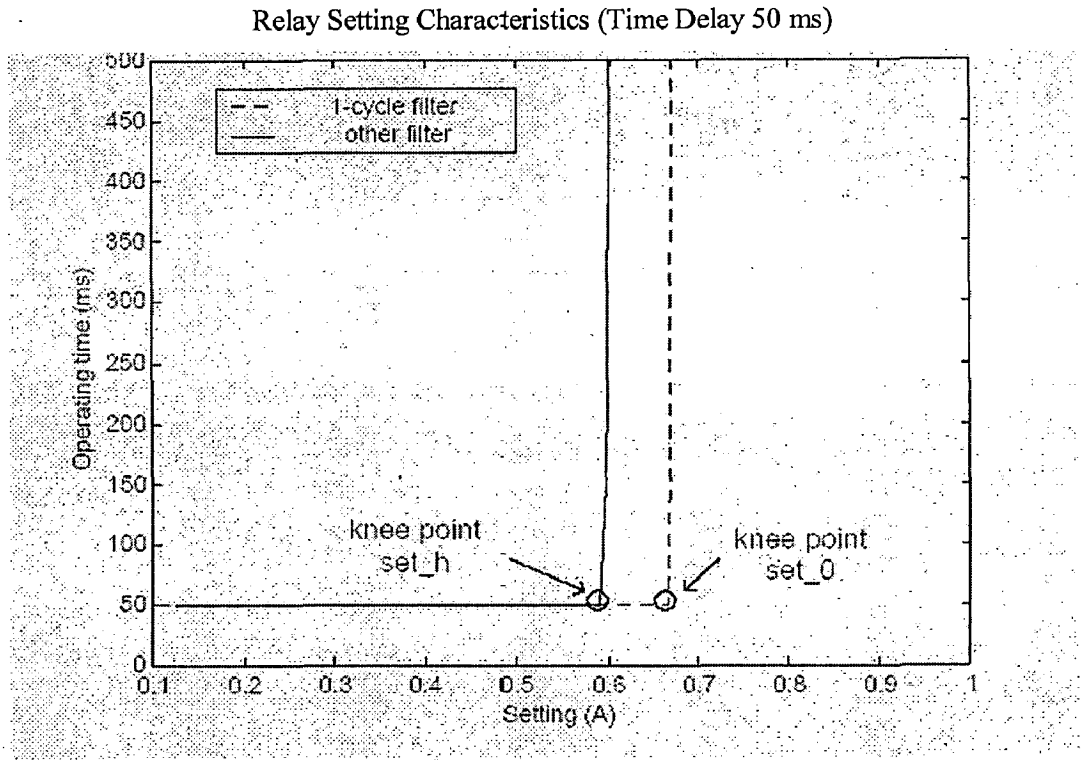


Figure 5. 6 Shift of relay setting characteristics

If the fundamental component is available, the impact of a disturbance on relay performance can then be evaluated by checking the setting limit shift due to the disturbance. However, the large number of possible events and system Configurations give an almost unlimited amount of combinations of signal components. It is not possible to design a filter that in all cases extract the exact value of the fundamental component. There is thus no reference to which the output of a given filter can be compared. There is however an indirect way to evaluate the impact of a given disturbance by comparing the filter outputs by different relay filters. If all the filters yield similar setting limits, then it can be safely assured that the unwanted components in the input signal are not of much concern. They can either be of small magnitude or easily removed by all of the filters. If there is significant shift in setting limits among different filters, it means there is something in the input signal that may seriously affect relay performance. Let the setting of 1-cycle filter be the reference value set_0 and the setting of another filter be set_h, the disturbance factor D, which has a somewhat different meaning from the one introduced in section 5.2.1.1, is defined through the following expression:

$$D = | (set\_h - set\_0)/set\_h | \qquad (5.4)$$

Where set_h and set_0 are defined as above. This expression is the same in form as equation. 5.1.

According to the observations done from above methods, one should select the required delay in relay operation, desired filter and the setting value. One can observe that most of the relays show that if the delay of operation is increased the setting value will be reduced. So we have to make a tradeoff between them

To do all these things, one need database [12] of disturbances to test the desired relay.

Chapter – 6

Case Studies & Simulation Results

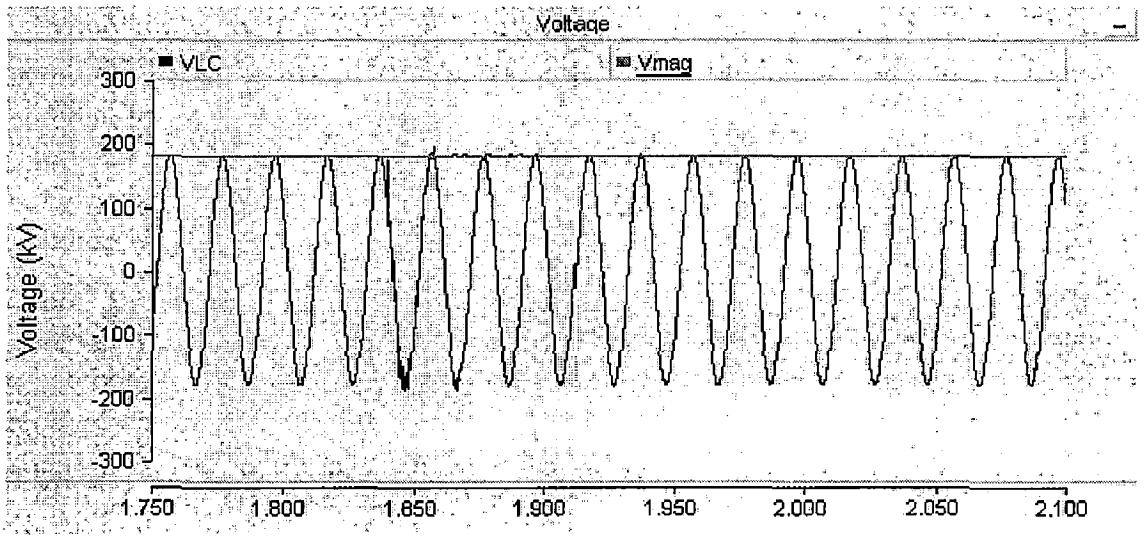
6.1 Introduction

The Case Studies are carried out for both setting-based quantification and design-based quantification. Under each of the two conditions, several typical disturbances are tested. Their disturbance impacts are illustrated in such diagrams. The diagrams are interpreted and discussed.

6.2 Setting-based Evaluation of Disturbance Impact

Case 1: Transient 1

This is a type of disturbance occurred due to switching of capacitors [17] in the line. This may cause some transients in current waveform. Here this was observed in a 230 kV system simulated in PSCAD™. The current and voltage waveforms are illustrated in figure 6.1.



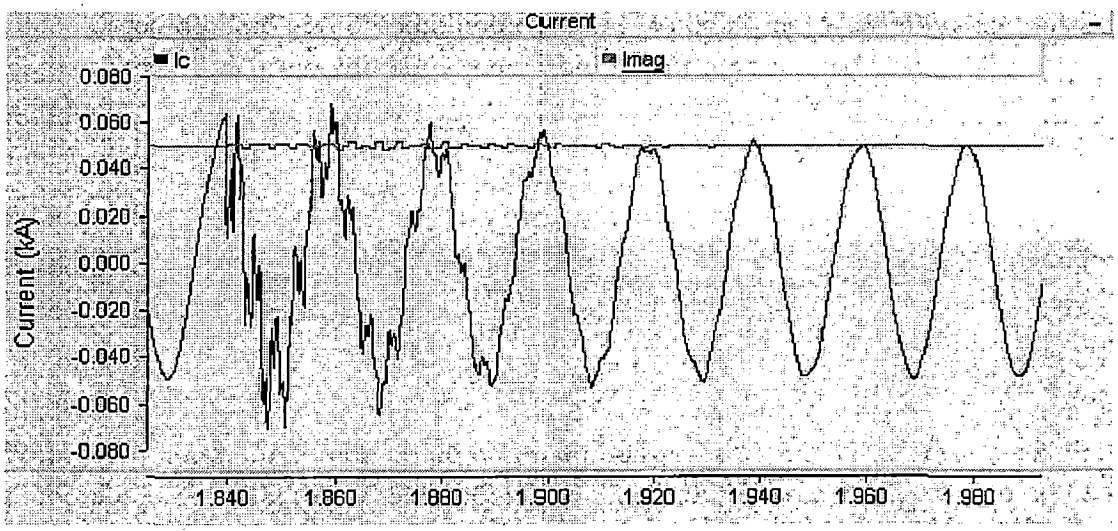


Figure 6. 1 Current & Voltage Transient Disturbance type-1

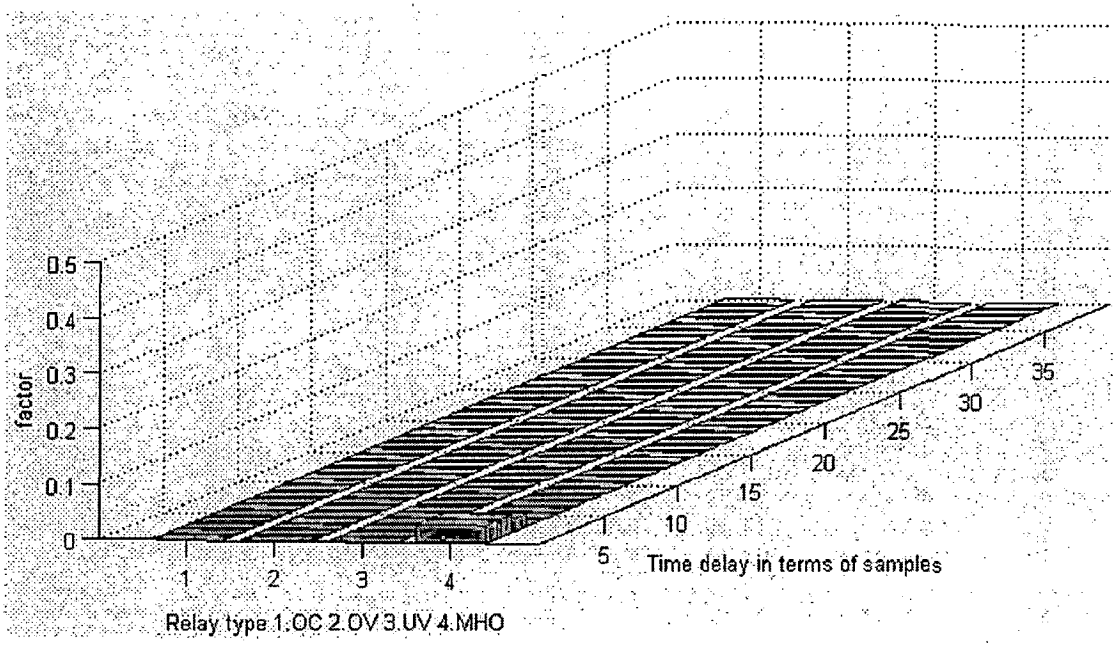


Figure 6. 2 Impact on relay setting zone by current transient

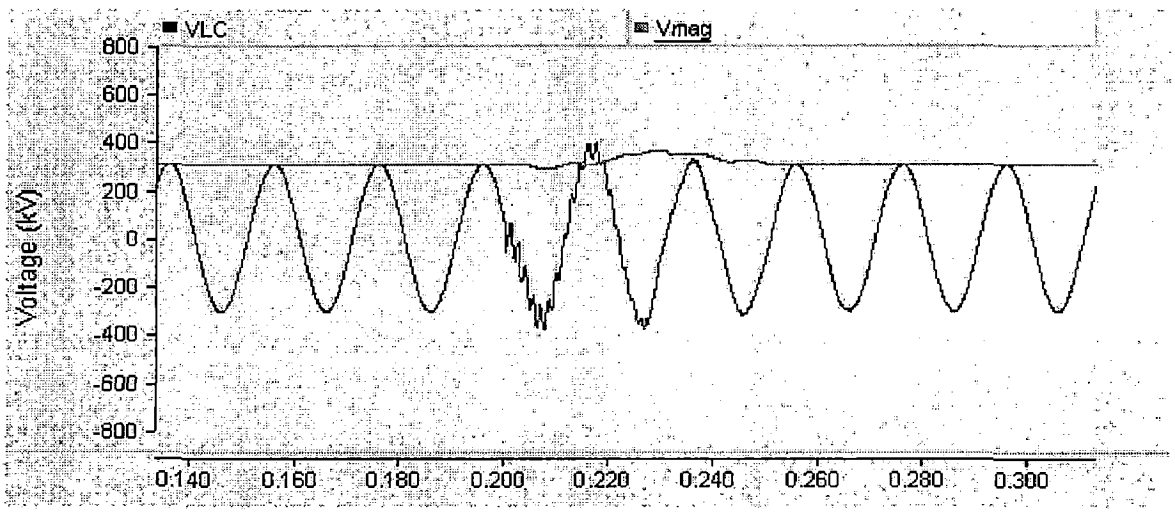
The switching of capacitor causes both current and voltage transients. But according to the situation either of them is significant, not both. In this case of current transient is dominant than voltage transient. In figure 6.1 the extracted

fundamental component by one cycle Fourier filter is also shown. From figure 6.2, it is observed that the transient severity is very less for all types of relays because the impact factor is very much less than 0.5[1].

Case 2: Transient 2

This is a type of disturbance occurred due to switching of capacitors [17] in the line. Here the transients were observed in a 230 kV system simulated in PSCAD®. The current and voltage waveforms are illustrated in figure 6.3.

From figure 6.4 we can observe that the overvoltage relay has an impact and reducing after a cycle period. And other types of relays are having no significant effect, masking the risk of overvoltage relay tripping if the time delay is 20ms or less.



[1] 0.5 means 50% variation in the setting (<50% change is allowed)

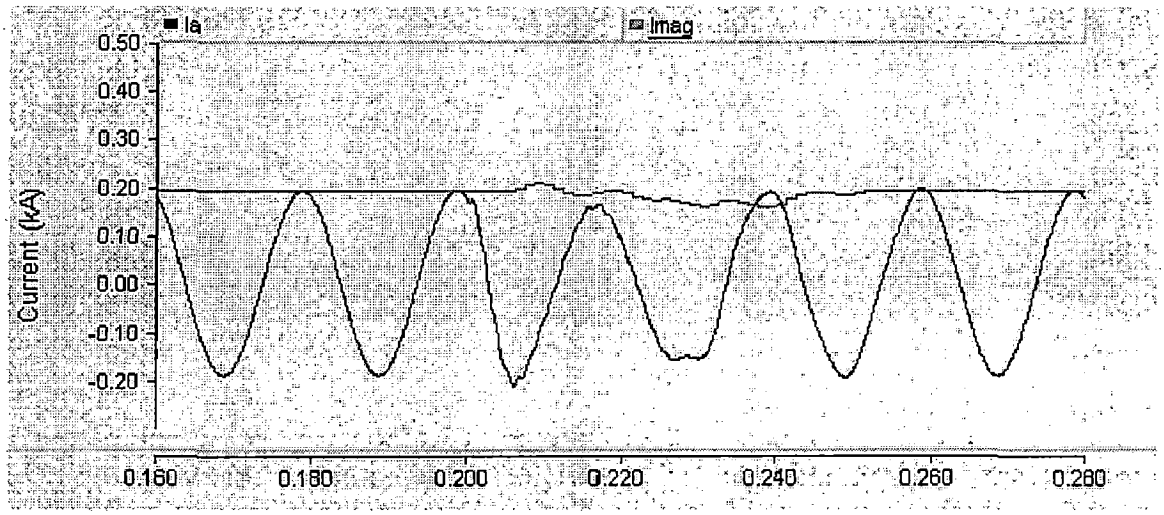


Figure 6. 3 Current and Voltage Transients disturbances waveforms (type-2)

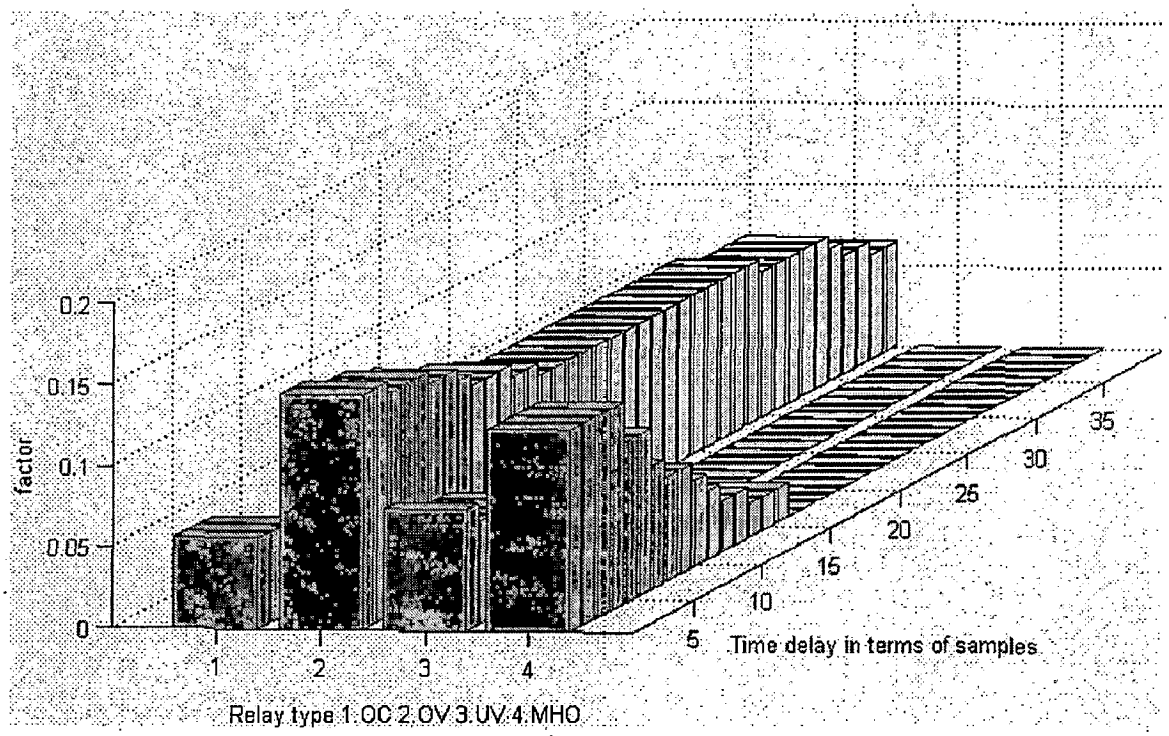


Figure 6. 4 Impact of disturbance transient type-2

Case 3: Current inrush Transient

The transient due to switching of loaded transformer [16]. The transient generated in this situation contains both odd and even harmonics, which attenuate after some time. The attenuation period is so long that the transient does threaten the operation of some relays. From figure 6.6 it is demonstrated that both overcurrent relay and impedance relay are potentially affected. Figure 6.5 shows the current inrush transient waveform.

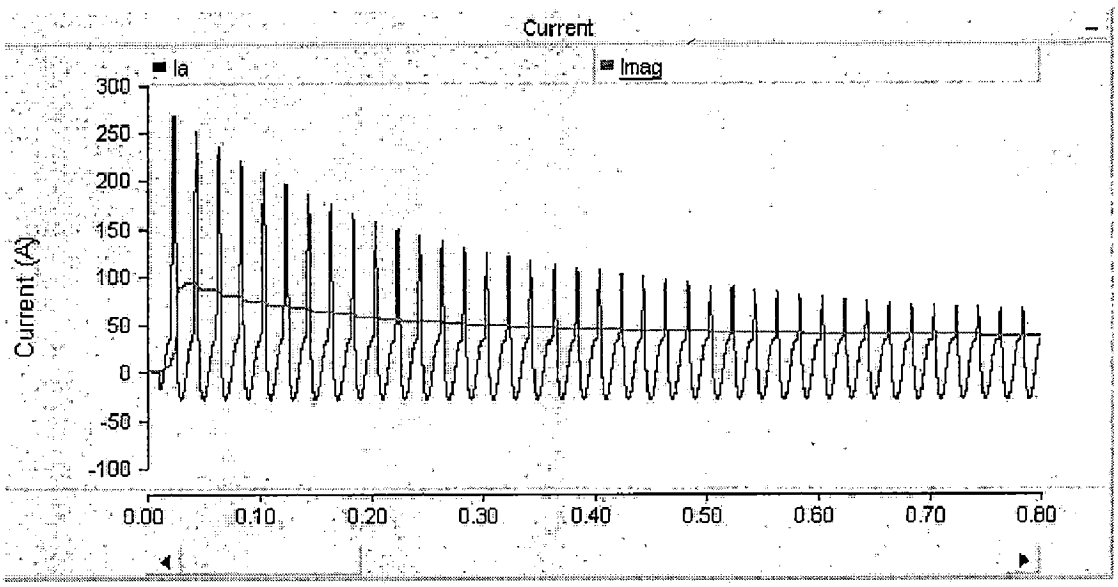


Figure 6. 5 Inrush Current Transient (13.8 kV System)

Due to high overcurrent, the disturbance has considerable impact on overcurrent relays. The impact on impedance relays can be depicted with the help of impedance trace diagram as shown in figure 6.7.

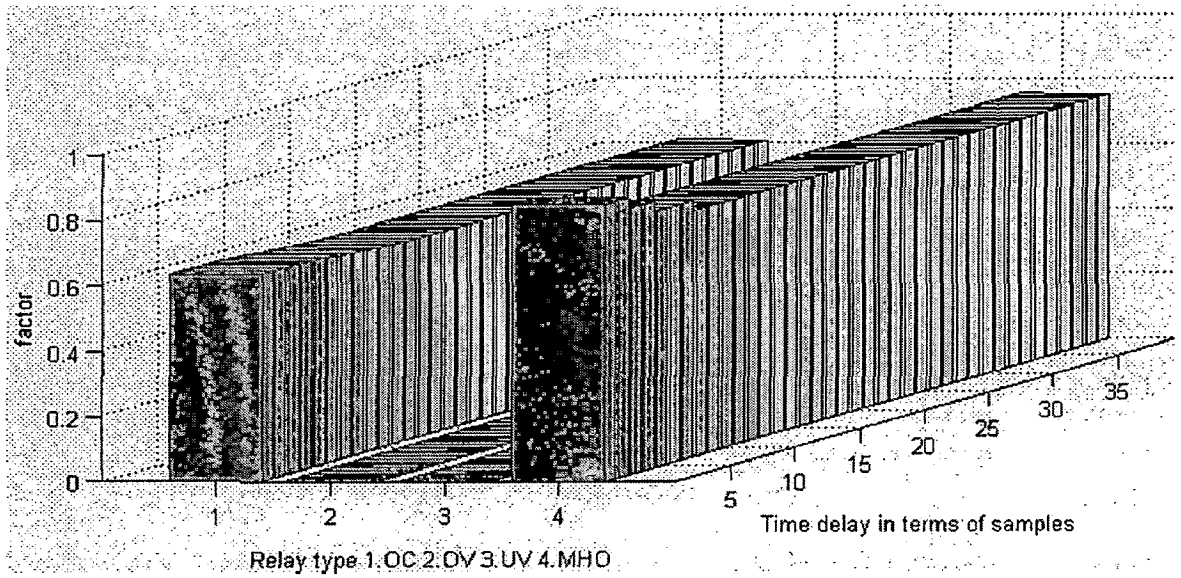


Figure 6. 6 Impact of inrush current on relay setting zone

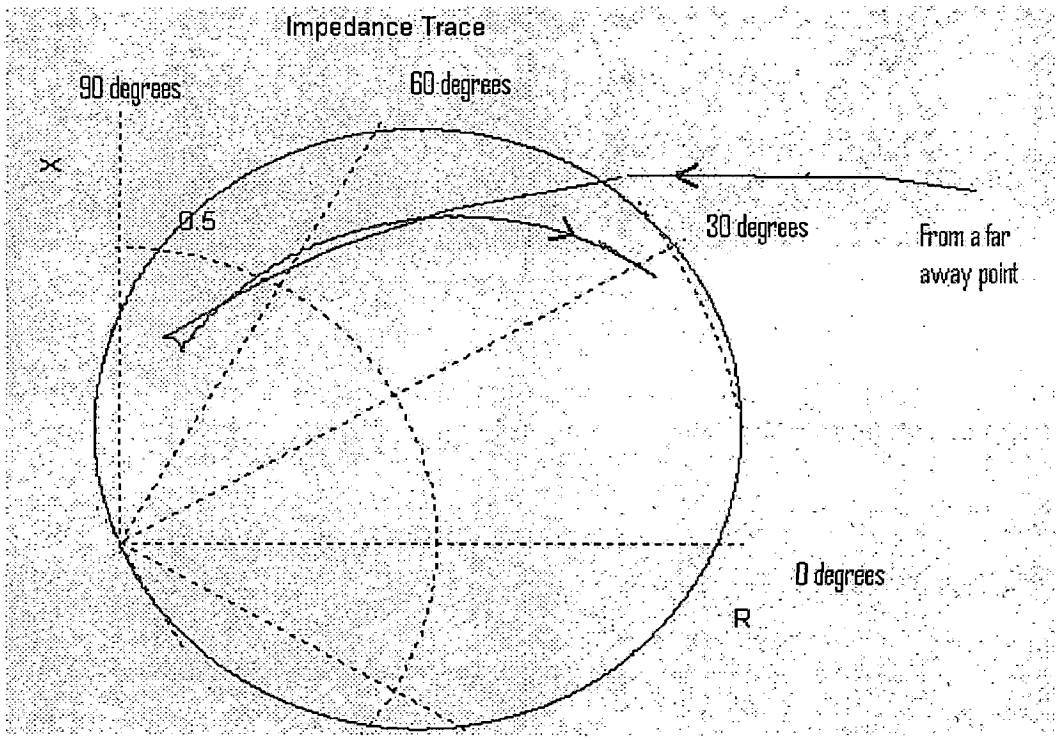


Figure 6. 7 Impedance Trace for inrush current disturbance

Case 4: Voltage Dip

When there is a voltage dip in the system, the load current on a particular feeder can experience either a short time increase or decrease, depending on the type of the attached load and the location of the monitor. Figure 6.8 shows an example of increase in current and dip in voltage.

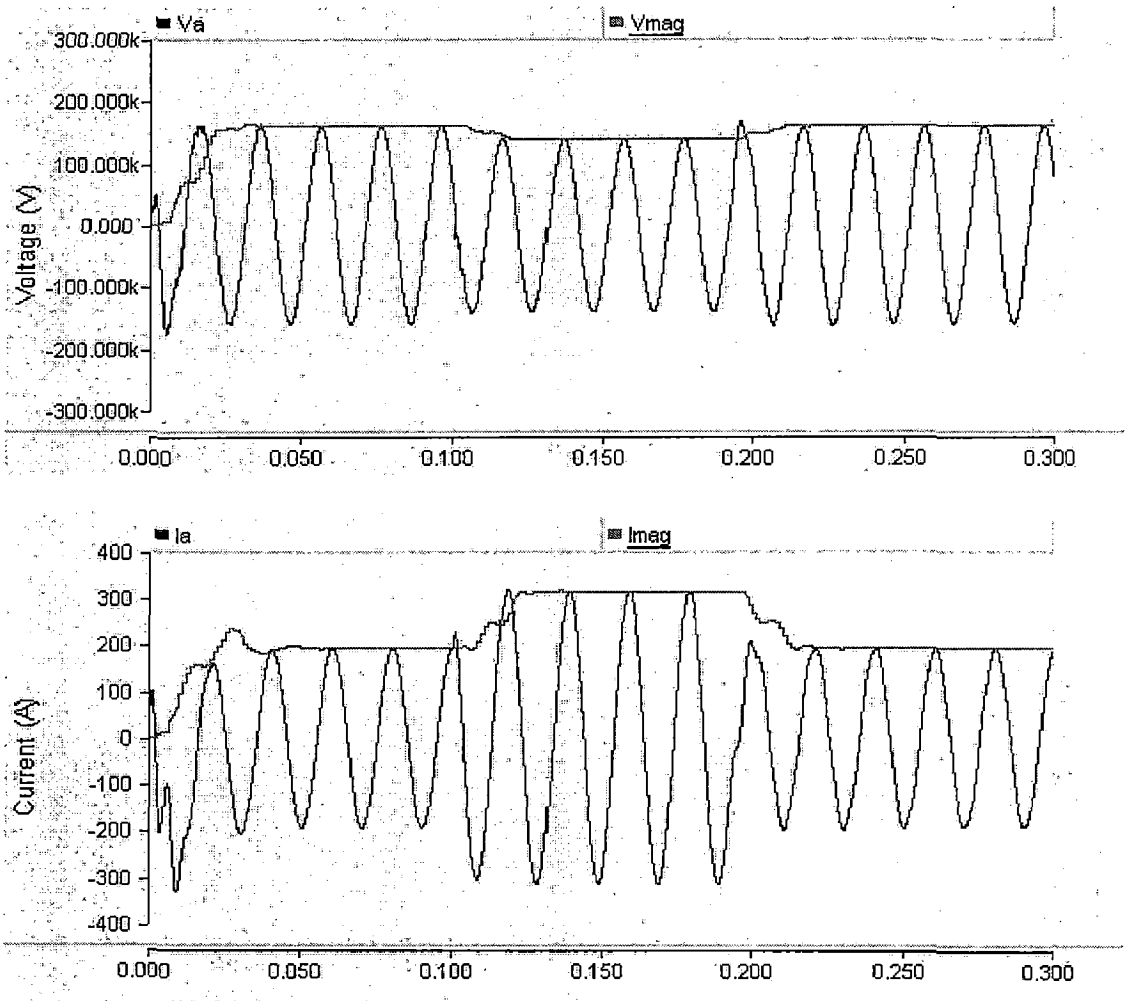


Figure 6. 8 Voltage Dip disturbance

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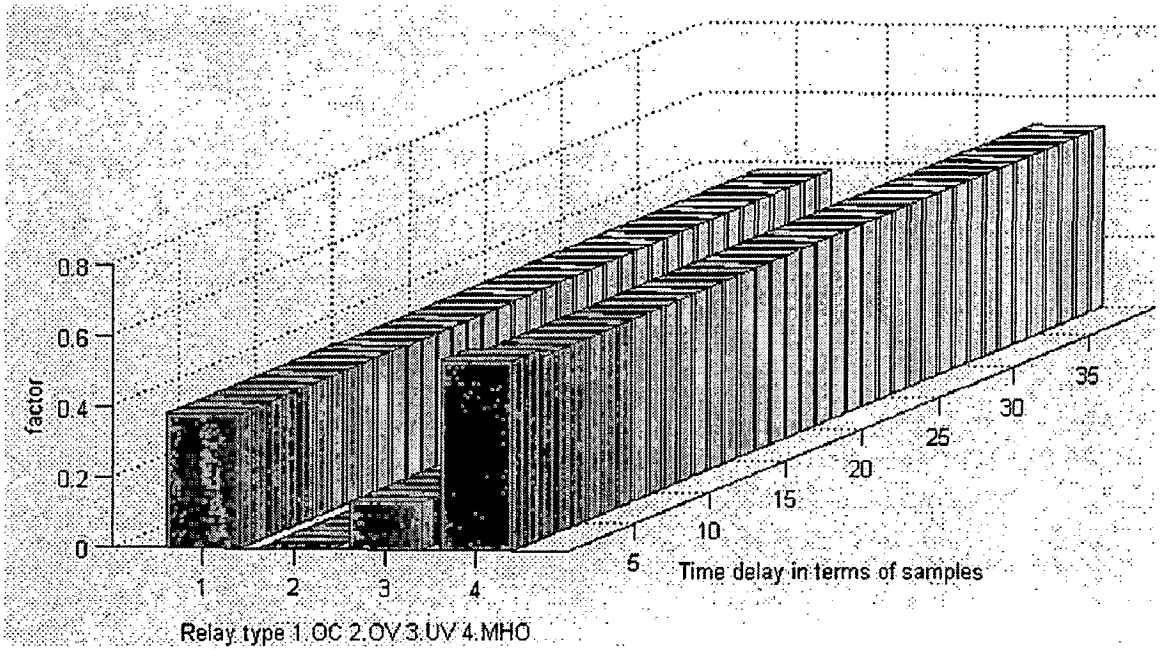

Figure 6. 9 Impact on relay protection zone

In this case, three types of relay are affected, as shown in figure 6.9. There is much impact on overcurrent and impedance relays, less impact on undervoltage relay and almost no impact on overvoltage relay. The impact duration is quite long (more than 20ms). The heights of the bars show the relative disturbance variation towards the relay setting region. The higher the bar, the greater the potential risk of the relay mal-operation.

6.3 Design-based evaluation of Disturbance impact

In this type of evaluation only overcurrent relay is tested for all types of Fourier filter so only current signal is taken for evaluation. This can also be done for all types of relay. But that is not necessary because in this type of evaluation only different types of filters are tested that doesn't depend on the type of relay. For all types of relay it gives same response.

Case 1: Current Transient:

Figure 6.10 shows the current transient taken from 230 kV systems and the disturbance occurred due to capacitor switching.

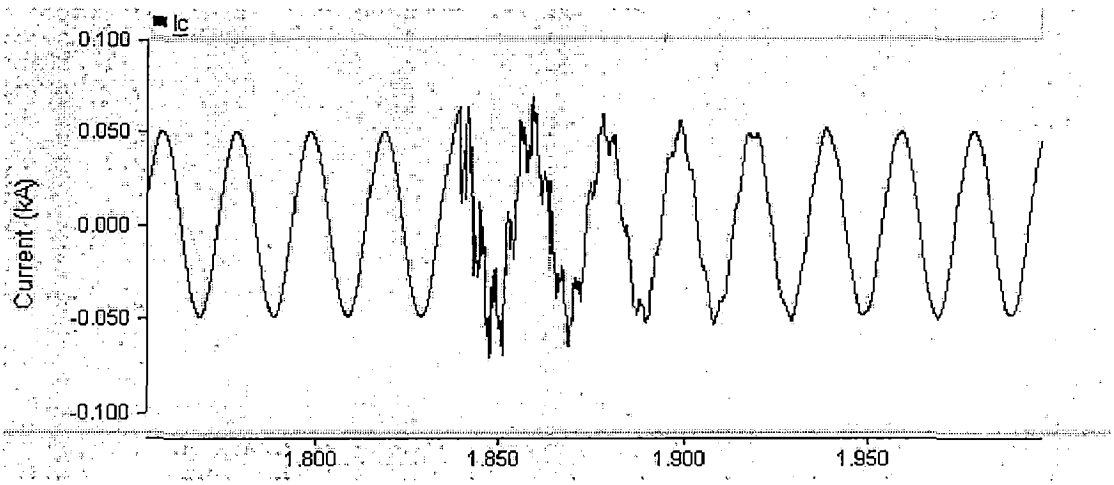

Figure 6. 10 Current Transient

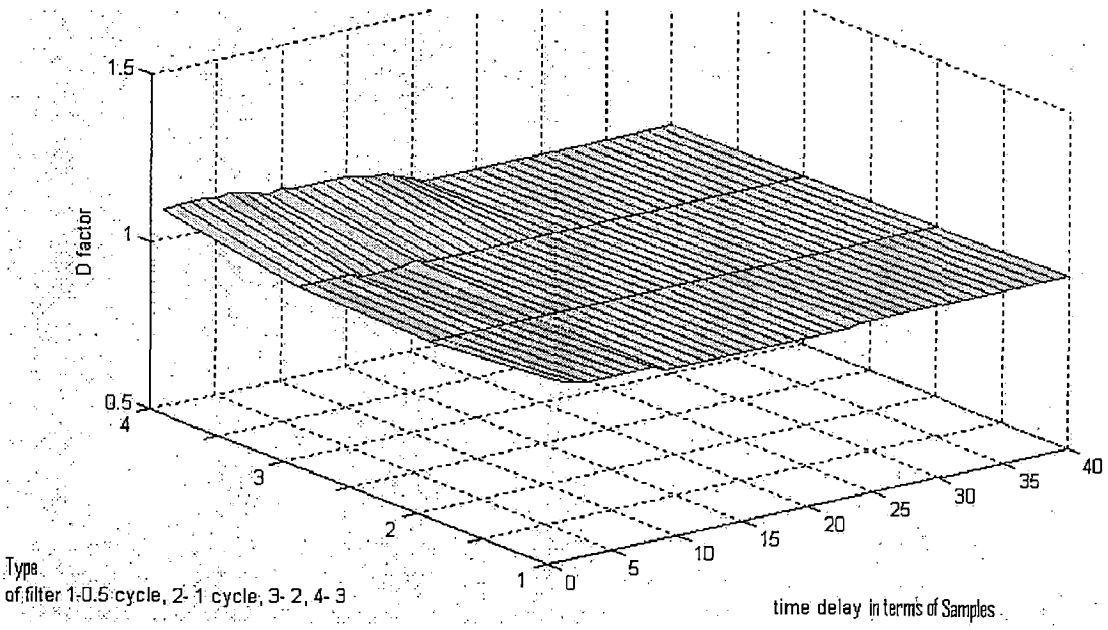

Figure 6. 11 Impact of current transient on relay performance

The response to the current transient by different filters is shown in figure 6.11. The result is a rather float plane, which implies that there is no difference on the observation of the input signal by all the filters. In other words, the spikes on the current waveform are ignored by almost all the algorithms.

Case 2: Inrush Current

The inrush current is observed in a 13.8kV system. This is happened when a loaded transformer is energized. Figure 6.12 shows the inrush current waveform

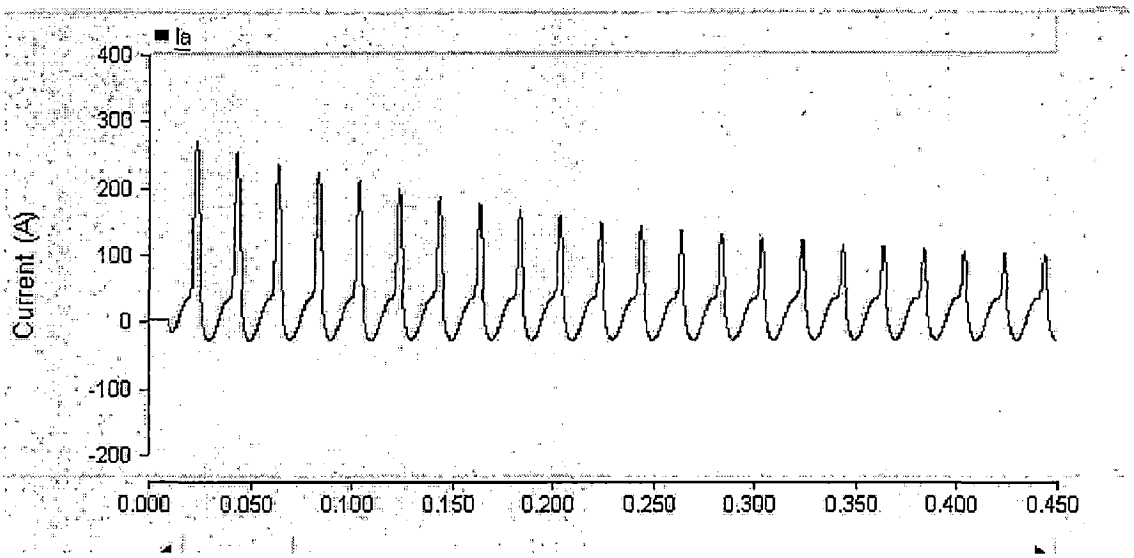

Figure 6. 12 Inrush Current

From the result in figure 6.13, it is observed that the transient has severe impact on relay performance if 0.5 cycle filter algorithm is selected. The reason is that 0.5 cycle filter algorithm can't remove the even harmonics. As the inrush current is rich in 2^{nd} and 4^{th} harmonics, the relay characteristic curve will be shifted considerably. And the differences among the remaining three filters are much smaller as all of them are capable of removing even harmonics.

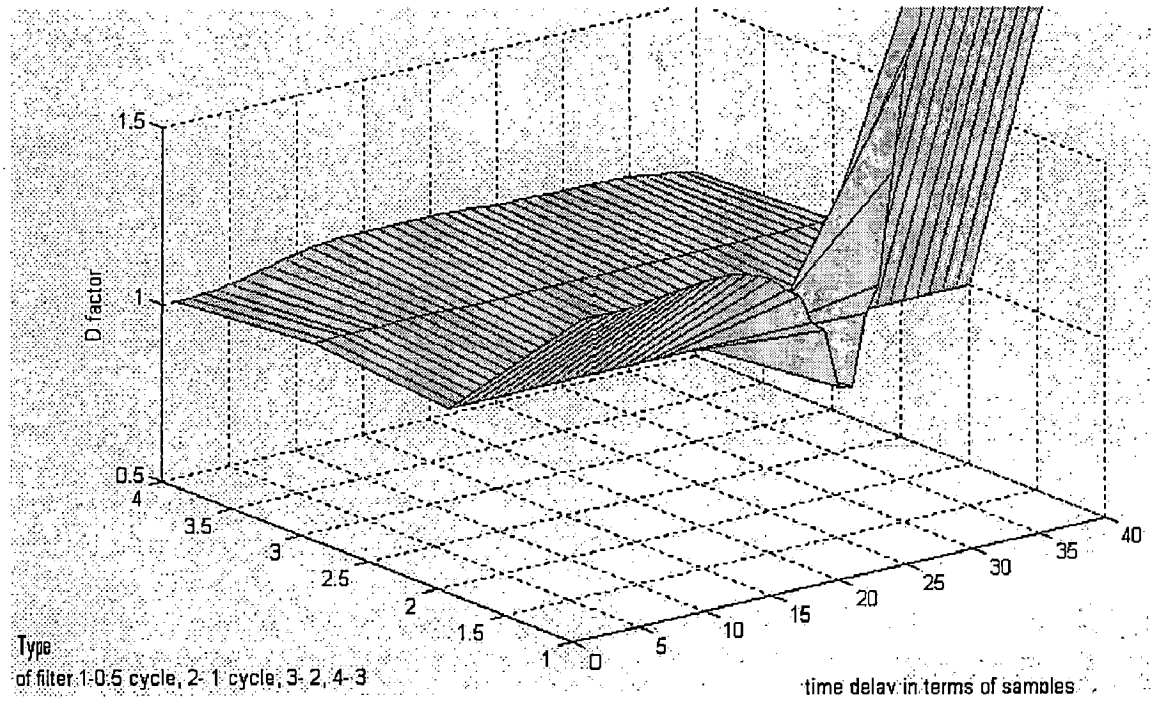

Figure 6. 13 Impact of inrush current on relay performance

Case 3: Current Swell

This case shows the current waveform during a voltage dip, in this case current increases during the dip.

The result in figure 6.15 indicates that the input signal causes no difference among the responses of various relay filters.

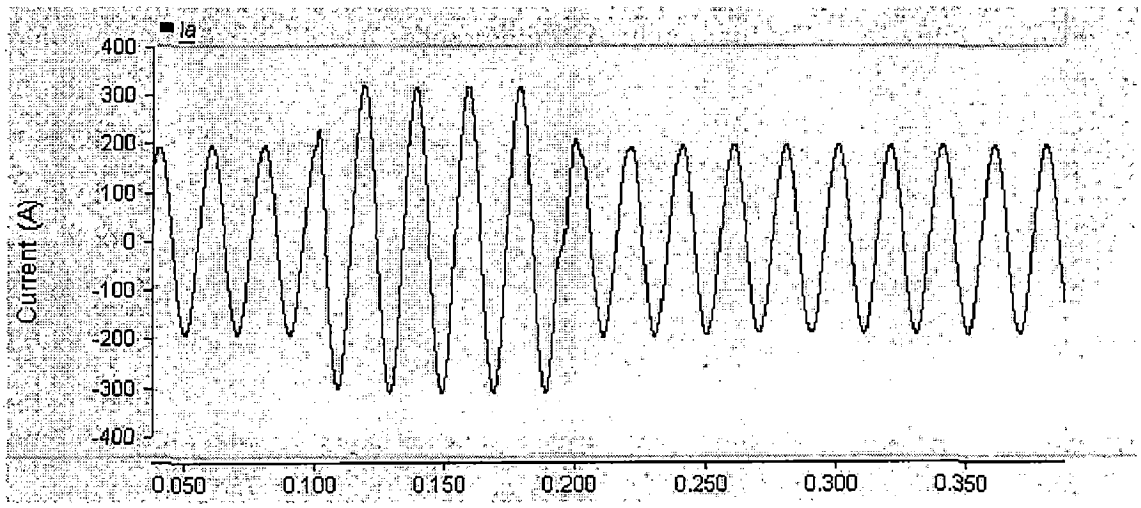

Figure 6. 14 Current Swell

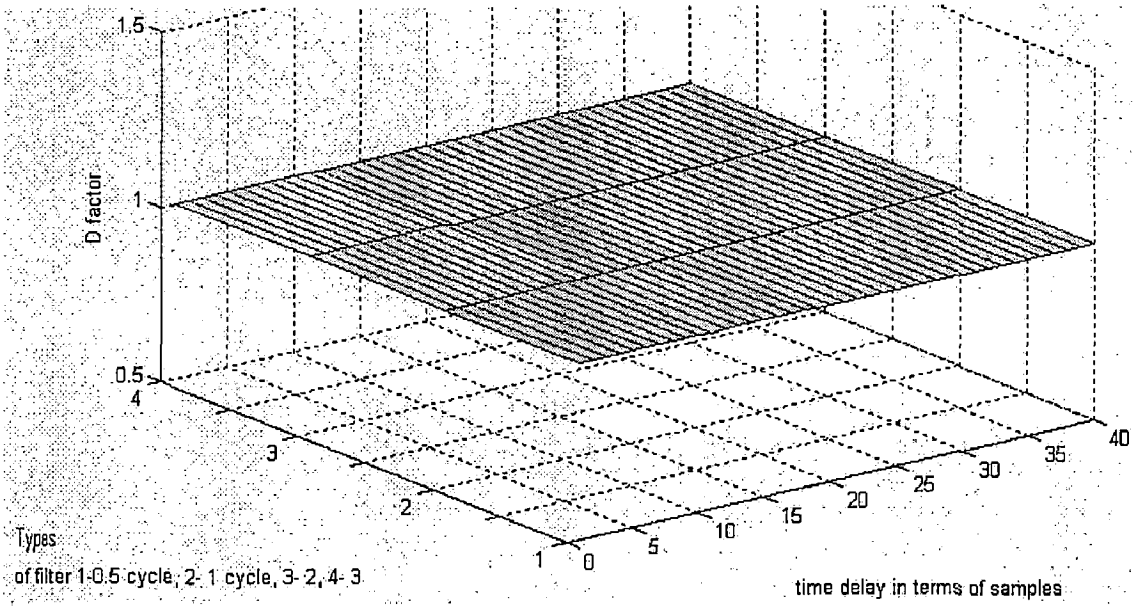

Figure 6. 15 Impact of current swell on relay performance

Case 4: High frequency harmonics and noise

Figure 6.16 shows a current waveform with a large amount of high frequency harmonics and noise.

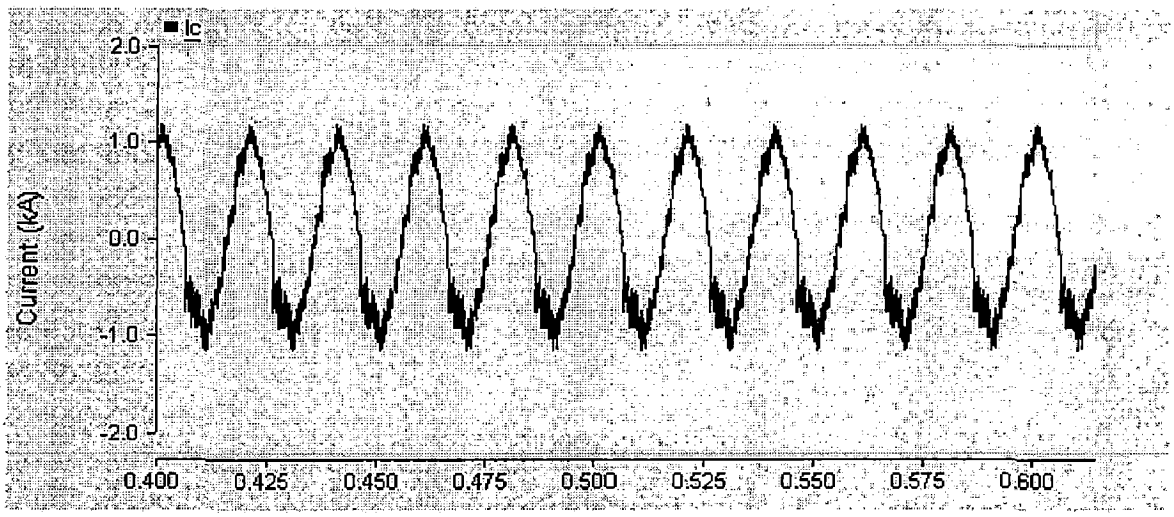

Figure 6. 16 High frequency harmonics and noise

The result in Figure 6.17 indicates that the impact of the input signal on all the filters. The impact can be ignored if the time delay is greater than 10ms.

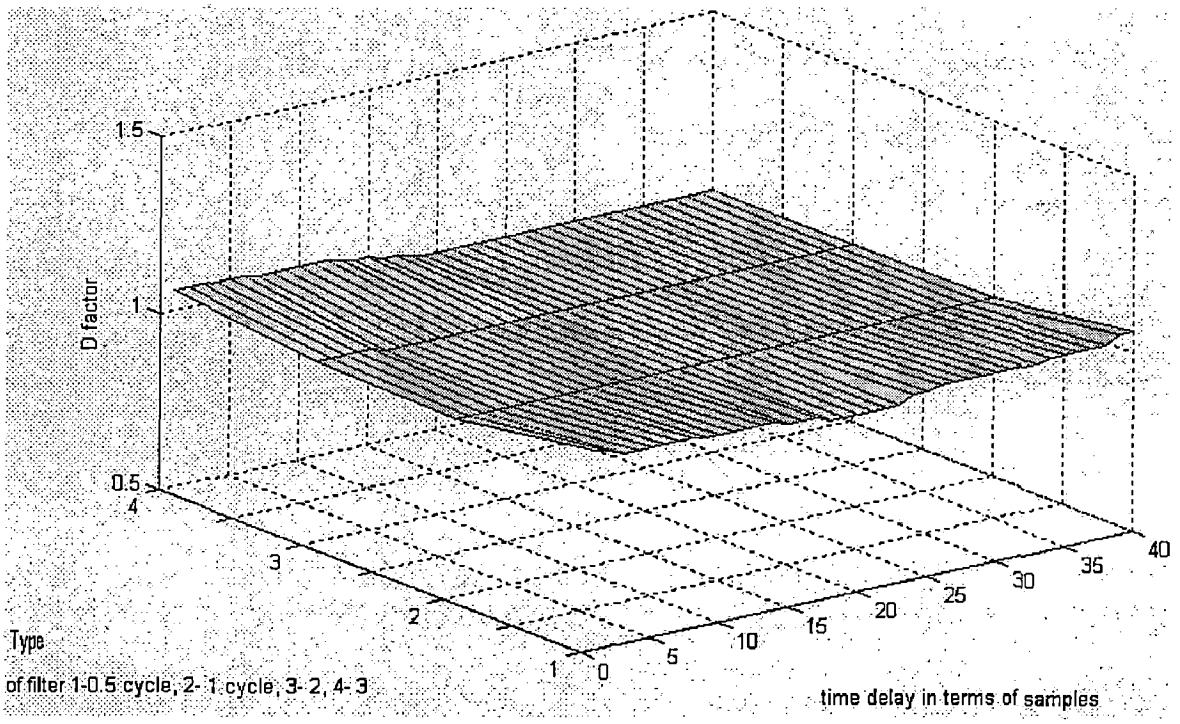

Figure 6. 17 Impact of High Frequency harmonics and noise on relay performance

6.4 Comparing Among Cases

From the result it is observed that a voltage dip disturbance is likely to affect more relays with greater severity, when compared with other disturbances. Also of concern is the switching inrush disturbance.

With the help of impact diagrams as shown in the case studies, the disturbances effect on relay setting can be ranked based on the disturbance factors illustrated in the impact diagrams. As one disturbance might affect more than one type of relay, further ranking of disturbances for a particular relay type can be made. For example, all the voltage dips can be ranked according to their impact on relay setting selection. Such information is very useful to relay users when determining relay settings.

The design based evaluation study focused on whether the disturbances make different relay filters response differently. From the results it is observed that the most severe disturbances are even harmonics, inter harmonics and long transients.

The impact of a disturbance on relay filters can be examined by checking the flatness and smoothness of the surface formed by filter responses. A plain surface means the disturbance signal yields similar outputs by different filters, while a surface with great curvature implies much unwanted components or transient in the signal. The disturbance can be ranked based on the curvature of the surfaces. Those with higher rank can be applied to test the effectiveness of any existing or new filter algorithm.

Conclusions and Future Scope

A Digital Distance relay (MHO) is implemented in this work. It required both voltage and current waveform for estimating distance from the fault to the location of the relay. Fourier, Differential and a Differential equation combined with Fourier transform based algorithms are implemented. In all these cases Differential equation combined with Fourier transform is showing better response in the case of presence of decaying DC component.

Fourier one cycle filter shows good response among all types of Fourier Filters. It is a best algorithm for rejecting both even and odd harmonics and faster than others. Differential equation algorithm shows very much faster response. But it is having lesser accuracy.

By using Quantification techniques all types of relays under several disturbances, are tested. The impact factors for all types of disturbances are calculated. This will give us an idea to grade the disturbance impact on relays. So the disturbances can also be classified according to the impact factor. It can be concluded that Voltage sag is the very severe disturbance for all types of relay. This can be graded to one. Inrush current is also considered as one of the severe disturbance that can affect the relay.

Future Scope of the Work:

The quantification diagrams provide some intuitive information on the details of the disturbance. By developing criteria on the impact diagrams, the disturbances can be classified according to their impact severity and duration; based on which databases can be setup for relay testing. Maintaining the database setup can be

included in the future work. And the criteria, which will be used for classification, will be changed according to application and type of relay.

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Appendix

Recursive DFT Algorithm

The DFT for a current wave can be calculated by

$$I(n)_{DFT}^{L} = \frac{2}{LN}\sum_{k=0}^{LN-1} I_k e^{-jk\frac{2\pi}{N}} \qquad \ldots (1)$$

Assume $I_0, I_1, I_2, \ldots I_{LN-1}, I_{LN}, I_{LN+1}$ are the currents at $LN+1^{th}$ sample. If $LN+1^{th}$ sample is entered I_0 will become vanished in the formula. It can be written as

$$I(n+1)_{DFT}^{L} = \frac{2}{LN}\sum_{k=0}^{LN-1} I_{k+1} e^{-jk\frac{2\pi}{N}}$$

Replacing k with k-1 then

$$I(n+1)_{DFT}^{L} = \frac{2}{LN}\sum_{k=1}^{LN} I_k e^{-j(k-1)\frac{2\pi}{N}}$$

$$I(n+1)_{DFT}^{L} = \frac{2}{LN} e^{\frac{j2\pi}{N}}\left[\sum_{k=0}^{LN-1} I_k e^{-jk\frac{2\pi}{N}} + I_{LN} e^{-j2\pi L} - I_0\right]$$

$$I(n+1)_{DFT}^{L} = \frac{2}{LN} e^{\frac{j2\pi}{N}}\left[I(n)_{DFT}^{L} + I_{LN} e^{-j2\pi L} - I_0\right]$$

This is a complex expression to express the same with complex terms,

Assume $C(n)_{DFT}^{L} = real(I(n)_{DFT}^{L})$

$S(n)_{DFT}^{L} = real(I(n)_{DFT}^{L})$

After simplification equation 1 becomes to

$$C(n+1)_{DFT}^{L} = (C(n)_{DFT}^{L} + I_{LN}\cos 2\pi L - I_0)\cos\frac{2\pi}{N} + (\mathrm{S}(n)_{DFT}^{L} + I_{LN}\sin 2\pi L)\sin\frac{2\pi}{N}$$

$$S(n+1)_{DFT}^{L} = (C(n)_{DFT}^{L} + I_{LN}\cos 2\pi L - I_0)sin\frac{2\pi}{N} - (\mathrm{S}(n)_{DFT}^{L} + I_{LN}\sin 2\pi L)\cos\frac{2\pi}{N}$$

Where

$$I(n+1)_{DFT}^{L} = C(n+1)_{DFT}^{L} + j\,S(n+1)_{DFT}^{L}$$

The advantage of this method is lesser multiplications are required compared to the normal DFT.