COMPARISON OF CONFIGURATIONS OF CONVERTER FOR UPFC

A DISSERTATION

Submitted in partial fulfillment of the requirements for the award of the degree of

MASTER OF TECHNOLOGY

in

ELECTRICAL ENGINEERING

(With Specialization in Power System Engineering)

By

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CANDIDATE'S DECLARATION

I hereby declare that the work presented in this dissertation entitled **"Comparison of configurations of converter for UPFC"** is submitted in partial fulfillment of the requirement for the award of the degree of **Master of Technology** with specialization in **Power Systems Engineering** in the Department of Electrical Engineering, **Indian Institute of Technology Roorkee**, Roorkee is an authentic record of my own work carried out from July 2005 to June 2006 under the esteemed guidance of **Dr. B.Das,** Associate professor & **Dr. Vinay pant**, Assistant professor, Department of Electrical Engineering, Indian Institute of Technology Roorkee, Roorkee.

I have not submitted the matter embodied in this report for the award of any other degree or diploma.

Date: 30th June, 2006

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CERTIFICATE

This is to certify that the above statement made by the candidate is true to the best of my knowledge and belief.

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(Ega Ajith Kumar)

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ABSTRACT

In this thesis, the various configurations of UPFCs have been simulated using the digital simulation tool, PSCAD/EMTDC V4.1. And the comparative analysis is presented, by analyzing the various configurations of UPFCs on the basis of DC Bus voltage magnitude and its variations, physical structure, possible scheme for implementation, switching frequency, harmonic content and rating of UPFC. The simulation studies have been carried out using the four machine, 10 bus, two area standard system. It is concluded that, the compensation provided by the series inverter, and hence the amounts of real and reactive power supplied by the series inverter to the power system are same in both the cases by maintaining the two different DC Bus voltages by two different configurations of the inverters.

CHAPTER: 1

Introduction

The power system is an interconnection of generating units to load centers through high Voltage electric transmission lines and in general is mechanically controlled. It can be divided into three subsystems: generation, transmission and distribution subsystems. Until recently all three subsystems were under supervision of one body within certain geographical area providing power at regulated rates. In order to provide cheaper electricity the deregulation of power system, which will produce separate generation, transmission and distribution companies, is already being performed. At the same time electric power demand continues to grow and also building of the new generating units and transmission circuits is becoming more difficult because of economic and environmental reasons. Therefore, power utilities are forced to relay on utilization of existing generating units and to load existing transmission lines close to their thermal limits. However, stability has to be maintained at all times. Hence, in order to operate power system effectively, without reduction in the system security and quality of supply, even in the case of contingency conditions such as loss of transmission lines and/or generating units, which occur frequently, and will most probably occur at a higher frequency under deregulation, a new control strategies need to be implemented.

In the late 1980s the Electric Power Research Institute (EPRI) has introduced a new technology program known as Flexible AC Transmission System (FATCS) [1-2]. The main idea behind this program is to increase controllability and optimize the utilization of the existing power system capacities by replacing mechanical controllers by reliable and high speed power electronic devices.

1.1 FACTS IN POWER SYSTEMS

FACTS technology refers to devices that enable flexible electrical power system operation, i.e. controlled active & reactive power flow redirection in transmission paths by controlling different parameters in the transmission system.

It opens up new opportunities for controlling and enhancing the useable capacity of present, as well as new upgraded lines. The possibility that current through a line can be controlled at a reasonable cost enables a large potential of increasing the capacity of existing lines thereby enabling them to carry power closer to their thermal ratings.

Because of their fast response FACTS Controllers can also improve the stability of an electrical power system by helping critically disturbed generators to give away the excess energy gained through the acceleration during fault [2]. This can be done by correctly changing the pattern of power flow. A lot of studies show that the reason for the loss of transient stability in a power system is that some overloads occurred in some lines while some other lines were tripped off after faults. After having adopted FACTS devices, the operating point of the power system can be altered to improve the transient stability to a certain extend.

1.1.1 CONTROLLABLE PARAMETERS FOR FACTS DEVICES [2]

Following are the few basic points regarding the possibilities of power flow control:

- Control of the line impedance X (e.g. with thyristor controlled series capacitor) can provide a powerful means of current control.
- When the angle is not large, which is often the case, control of X or the angle substantially provides the control of active power.
- Control of angle (with a phase regulator for example), which in turn controls the driving voltage, provides a powerful means of controlling the current flow and hence active power flow when the angle is not large.
- Injecting a voltage in series with the line, and perpendicular to the current flow, can increase or decrease the magnitude of current flow. Since the current flow

lags the driving voltage by 90 degrees, this means injection of reactive power in series, can provide a powerful means of controlling the line current, and hence the active power when the angle is not large.

- Injecting voltage in series with the line and with any phase angle with respect to the driving voltage can control the magnitude and the phase of the line current. This means that injecting a voltage phasor with variable phase angle can provide powerful means of precisely controlling the active and reactive power flow. This requires injection of both active and reactive power in series
- When the angle is not large, controlling magnitude of one or the other line voltages can be a very cost effective means for the control of reactive power flow through the interconnection
- Combination of the line impedance control with a series controlled and voltage regulation with a shunt controller can also provide a cost effective means to control both the active power flow and reactive power flow between the two systems.

1.1.2 TYPES OF FACTS CONTROLLERS [1, 2]

In general FACTS controllers can be divided into four categories

a) Series controller
b) Shunt controller
c) Combined series-series controllers
d) Combined series-shunt controllers

(a) Series controller [2]:

The series controller could be variable impedance, such as capacitor, reactor, etc or power electronics based variable source of main frequency, sub synchronous and harmonic frequencies to serve the desired need. Fig.1.1 shows the series controller. In principle all the series controllers inject voltage in series with the line. As long as the voltage is in phase quadrature with the line current, the series controller only supply or consumes variable reactive power. Any other phase relationship will involve handling of

real power as well. Series connected controller impacts the driving voltage and hence the current and power flow directly. Therefore, if the purpose of the application is to control the current/ power flow and damp oscillations, the series controller for a given MVA size is several times more powerful than the shunt controller.

Static synchronous series compensator (SSSC), interline power flow controller (IPFC), thyristor controlled switched series capacitor (TCSC) etc are the example of series controllers.

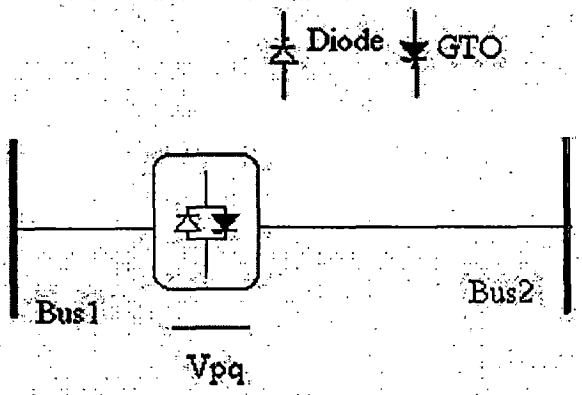


Figure 1.1: Series Controller.

(b) Shunt controller [2]:

As in the case of series controllers, the shunt controllers may be variable impedance, variable source, or a combination of these. In principle, all shunt controllers inject current into the system at the point of connection. Fig. 1.2 shows the shunt controller.

The shunt controller is like a current source, which draws from or injects current into the line. The shunt controller is therefore a good way to control voltage at and around the point of connection through injection of reactive current (leading or lagging), alone or a combination of active and reactive current for a more effective voltage control and damping of oscillations.

One important advantage of the shunt controller is that it serves the bus node independently of the individual lines connected to the bus. Static synchronous compensator (STATCOM), static synchronous generator (SSG), static VAR compensator

(SVC), thyristor controlled reactor (TCR), thyristor switched capacitor etc are the examples of shunt controllers.

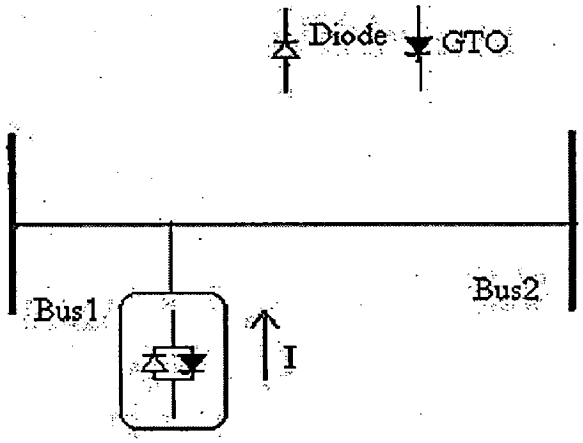


Figure 1.2: Shunt Controller

(c) Combined series-series controllers [2]:

This could be a combination of separate series controllers, which are controlled in a coordinated manner, in a multi line transmission system or it could be a unified controller, in which series controller provide independent series reactive compensation for each line but also transfer real power among the lines via the power link. Series-series controller is shown in Fig. 1.3.

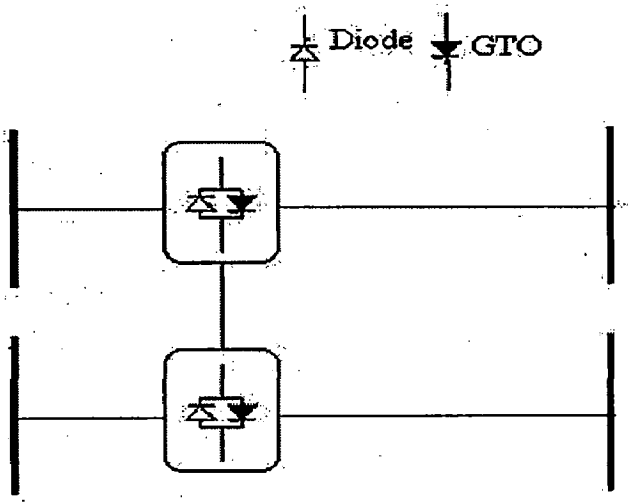


Figure 1.3: Combined series-series controller

The real power transfer capability of the unified series-series controller, referred as interline power flow controller, makes it possible to balance both the real and reactive power flow in the lines and thereby maximize the utilization of the transmission system.

(d) Combined series-shunt controllers [2]:

This could be a combination of separate shunt and series controllers, which are controlled in a coordinated manner, or a unified power, flow controller with series and shunt elements. In principle, combined shunt and series controllers inject current into the system with the shunt part of the controller and voltage in series in the line with the series part of the controller. Series-shunt controller is shown in Fig. 1.4.

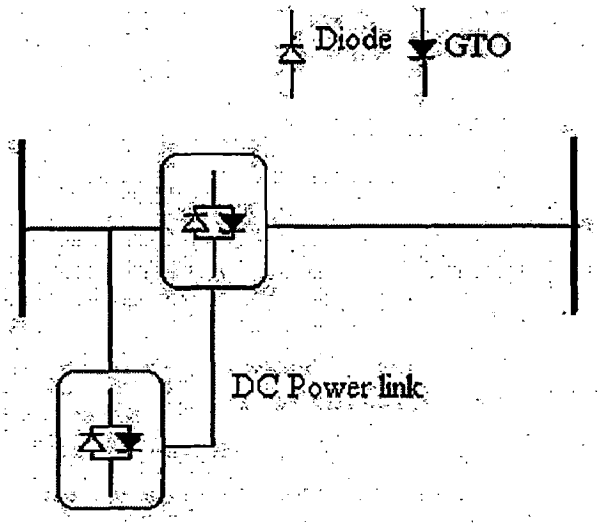


Figure1.4: Combined series-shunt controller

Unified power flow controllers (UPFC), thyristor controlled phase shifting transformer (TCPST) are the example of shunt series controller.

1.1.3 ADVANTAGES OF FACTS TECHNOLOGY [1, 2]

FACTS controllers enable the transmission system to obtain one or more of the following benefits:

- Control of power flow as ordered. The use of control of the power flow may be to follow a contract, meet the utilities' own needs, ensure optimum power flow, ride through emergency conditions, or a combination thereof.

- Increase the loading capability of lines to their thermal capabilities, including short term and seasonal. This can be accomplished by overcoming other limitations, and sharing of power among lines according to their capability
- Increase the system security through raising the transient stability limit, limiting short circuit currents and overloads, managing cascading blackouts and damping electromechanical oscillations of power systems and machines.
- Provide secure tie line connections to neighboring utilities and regions thereby decreasing overall generation reserve requirements on both sides.
- Provide greater flexibility in siting new generation
- Upgrade of lines
- Reduce reactive power flows, thus allowing the lines to carry active power
- Reduce loop flows
- Increase utilization of lowest cost generation.
- Balancing the power flow over a wide range of operating conditions, thereby using the power system network most efficiently.
- Balancing the power flow in parallel networks operating at different voltage levels.

A comparison of different features of various FACTS Controllers is given in Table 1.1. From this table, it is observed that among the various FACTS Controllers, Unified Power Flow Controller (UPFC) is the most versatile one.

Table 1.1: Comparison of controllable parameters of different FACTS Controllers

FACTS Controller	Control Attributes
Static Synchronous Compensator (STATCOM without storage)	Voltage control, VAR compensation, damping oscillations, voltage stability
Static Synchronous Compensator (STATCOM with storage, BESS, SMES, large dc capacitor)	Voltage control, VAR compensation, damping oscillations, transient and dynamic stability, voltage stability, AGC
Static VAR Compensator (SVC, TCR, TCS, TRS	Voltage control, VAR compensation, damping oscillations, transient and dynamic stability, voltage stability
Thyristor-Controlled Braking Resistor (TCBR)	Damping oscillations, transient and dynamic stability
Static Synchronous Series Compensator (SSSC without storage)	Current control, damping oscillations, transient and dynamic stability, voltage stability, fault current limiting
Static Synchronous Series Compensator (SSSC with storage)	Current control, damping oscillations, transient and dynamic stability, voltage stability
Thrystor-Controlled Series Capacitor (TCSC, TSSC)	Current control, damping oscillations, transient and dynamic stability, voltage stability, fault current limiting
Thyristor-Controlled Series Reactor (TCSR, TSSR)	Current control, damping oscillations, transient and dynamic stability, voltage stability, fault current limiting
Thyristor-Controlled Phase-Shifting Transformer (TCPST or TCPR)	Active power control, damping oscillations, transient and dynamic stability, voltage stability
Unified Power Flow Controller (UPFC)	**Active and reactive power control, voltage control, VAR compensation, damping oscillations, transient and dynamic stability, voltage stability, fault current limiting**
Thyristor-Controlled Voltage Limiter (TCVL)	Transient and dynamic voltage limit
Thyristor-Controlled Voltage Regulator (TCVR)	Reactive power control, voltage control, damping oscillations, transient and dynamic stability, voltage stability
Interline Power Flow Controller (IPFC)	Reactive power control, voltage control, damping oscillations, transient and dynamic stability, voltage stability

1.2 Unified Power Flow Controller (UPFC)

The idea of the unified power flow controller (UPFC) was first proposed by Gyugyi in 1992[3]. Since then, as the most sophisticated flexible ac transmission systems (FACTS) device, the UPFC has been researched widely and many papers dealing with UPFC's modeling; analysis, control, and application have been published in the literature.

The UPFC combines the functions of several FACTS devices and is capable of realizing voltage regulation, series compensation, and phase angle regulation at the same time, thus realizing the separate control of the active power and reactive power transmitted simultaneously over the line [2-4]. The general configuration of the UPFC is shown in Fig. 1.5. As it can be seen, the UPFC consists of two voltage source inverters. Inverter 1 is in parallel with the transmission line, while Inverter 2 is in series with the transmission line. The two inverters are connected back-to-back through a common dc-link. This arrangement enables real power flow in either direction between the two inverters.

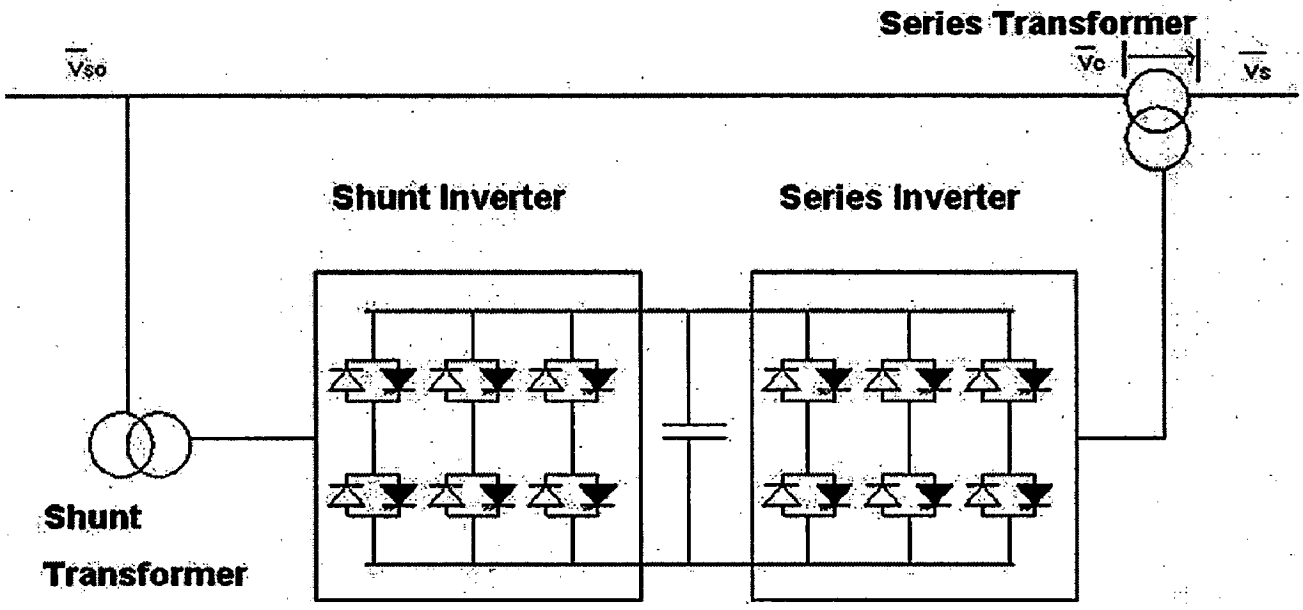


Figure 1.5: Conceptual representation of the UPFC in a power system

1.2.1 BASIC OPERATING PRINCIPLE [2, 5]

From the conceptual point of viewpoint, the UPFC is a generalized synchronous voltage source (SVS), represented at the fundamental frequency by voltage phasor V_{pq} with controllable magnitude V_{pq} ($0 \leq V_{pq} \leq V_{pqmax}$) and angle ρ ($0 \leq \rho \leq 2\pi$), in series with the transmission line.In this functionally unrestricted operation, which clearly includes voltage and angle regulation, the SVS generally exchanges both reactive and real power with the transmission system. But the SVS is able to generate only the reactive power exchanged; the real power must be supplied to it, or absorbed from it, by suitable power supply or sink. In UPFC arrangement the real power exchanged is provided by one of the end buses (e.g. the sending end bus).

In the practical implementation, the UPFC consists of two voltage-sourced converters, as shown in Fig. 1.6. These back-to-back converters, labeled "converter 1" and "converter 2" in the fig, are operated from a common DC link provided by a dc storage capacitor. This arrangement functions as an ideal ac-to-dc power converter in which the real power can freely flow in either direction between the ac terminals of the two converters, and each converter can independently generate or absorb reactive power at its own ac output terminal.

Converter 2 provides the main function of the UPFC by injecting a voltage V_{pq} with controllable magnitude V_{pq} and phase angle ρ in series with the line via an insertion transformer [2, 4]. This injected voltage acts essentially as a synchronous ac voltage source. The transmission line current flows through this voltage source resulting in active and reactive power exchange between it and the ac system. The reactive power is exchanged at the ac terminal (i.e. at the terminal of the series insertion transformer) is generated internally by the converter. The real power exchanged at the ac terminal is converted into dc power, which appears at the dc link as a positive or negative real power demand.

The basic function of converter 1 is to supply or to absorb the real power demanded by converter 2 at the common dc link to support the real power exchange resulting from the series voltage injection. This dc link power demand of converter 2 is

converted back to ac by converter 1 and coupled to the transmission line bus via a shunt-connected transformer. In addition to the real power need of converter 2, converter 1 can also generate or absorb controllable reactive power, if it is desired, and thereby provide independent shunt reactive compensation for the line. There is a closed path for the real power balance by the action of series voltage injection through converter 1 and 2 back to the line, the corresponding reactive power exchanged is supplied or absorbed locally by converter 2 and therefore does not have to be transmitted by the line. Thus, converter 1 can be operated at a unity power factor or to be controlled to have a reactive power exchange with the line independent of the reactive power exchanged by converter 2.

1.2.2 Conventional Transmission Control Capabilities

Viewing the operation of the unified power flow controller from the standpoint of traditional power transmission based on reactive shunt compensation, series compensation, and phase angle regulation, the UPFC can fulfill all these functions and thereby meet multiple control objectives by adding the injected voltage V_{pq}, with appropriate amplitude and phase angle, to the (sending end) terminal voltage V_s. using phasor representation, the basic UPFC power flow control functions are illustrated in Fig. 1.6.

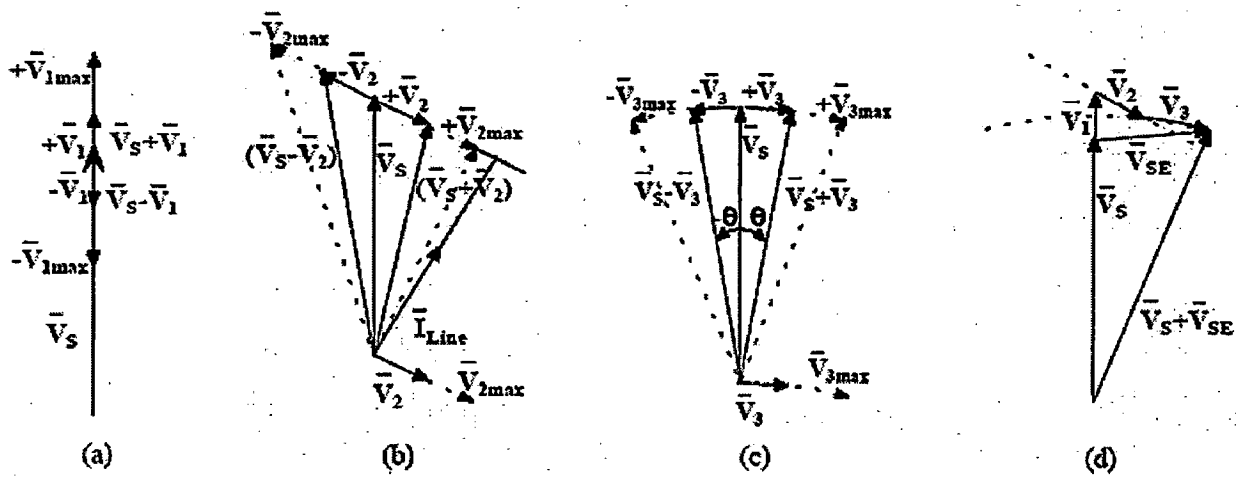


Figure 1.6: Phasor diagram illustrating the conventional transmission capabilities of the UPFC (a) voltage regulation (b) line impedance compensation (c) phase shifting (d) simultaneous control of voltage, impedance, and angle

Voltage regulation with continuously variable in-phase/anti-phase voltage injection, is shown in Fig. 1.6(a) for voltage increments $V_{pq} = \Delta V$ ($\rho = 0$). This is functionally similar to that obtainable with a transformer tap changer having infinitely small steps

Series reactive compensation is shown in Fig. 1.6(b) where $V_{pq} = V_p$ is injected in quadrature with the line current I. Functionally this is similar to series capacitive and inductive line compensation attained by the SSSC. The injected series compensating voltage can be kept constant, if desired, independent of line current variation, or can be varied in proportion with the line current to imitate the compensation obtained with series capacitor or reactor.

Phase angle regulation is shown in Fig. 1.6(c) where $V_{pq} = V_\sigma$ is injected with an angular relationship with respect to V_s that achieves the desired σ phase shift without any change in magnitude. Thus the UPFC can function as a perfect phase angle regulator, which can also supply the reactive power involved with the transmission angle by internal VAR generation.

Multifunction power flow control, executed by simultaneous terminal voltage regulation, series capacitive line compensation, and phase shifting, is shown in Fig 1.7(d) where $V_{pq} = V_q + V_\sigma + \Delta V$. This functional capability is unique to the UPFC. No single conventional equipment has similar multifunctional capability.

1.2.3 Basic Control Structure of UPFC [2, 4, 5]

The superior operating characteristics of the UPFC are due to its unique ability to inject an ac compensating voltage vector with arbitrary magnitude and angle in series with the line upon command, subject only to equipment rating limits. With suitable electronic controls, the UPFC can cause the series injected voltage vector to vary rapidly and continuously in magnitude and angle as desired. Thus, it is not only able to establish an operating point within a wide range of possible P, Q conditions on the line, but also has the inherent capability to transition rapidly from one such achievable operating point to any other.

The UPFC control system can be divided into two parts; internal control and functional operation control. The internal controls operate the two converters so as to produce the commanded series injected voltage and, simultaneously, draw the desired shunt reactive current. The internal controls provide gating signals to the converter valves so that the converter output voltage will properly respond to the internal reference variables, i_{pRef}, i_{qRef} and v_{pqRef}, in accordance with the basic control structure shown in Fig. 1.7. As can be observed, the series converter responds directly and independently to the demand for series voltage vector injection. Changes in series voltage vector, v_{pq} can therefore be affected instantaneously. In contrast, the shunt converter operates under a closed loop current control structure whereby the shunt real and reactive power components are independently controlled. The shunt reactive power responds directly to an input demand.

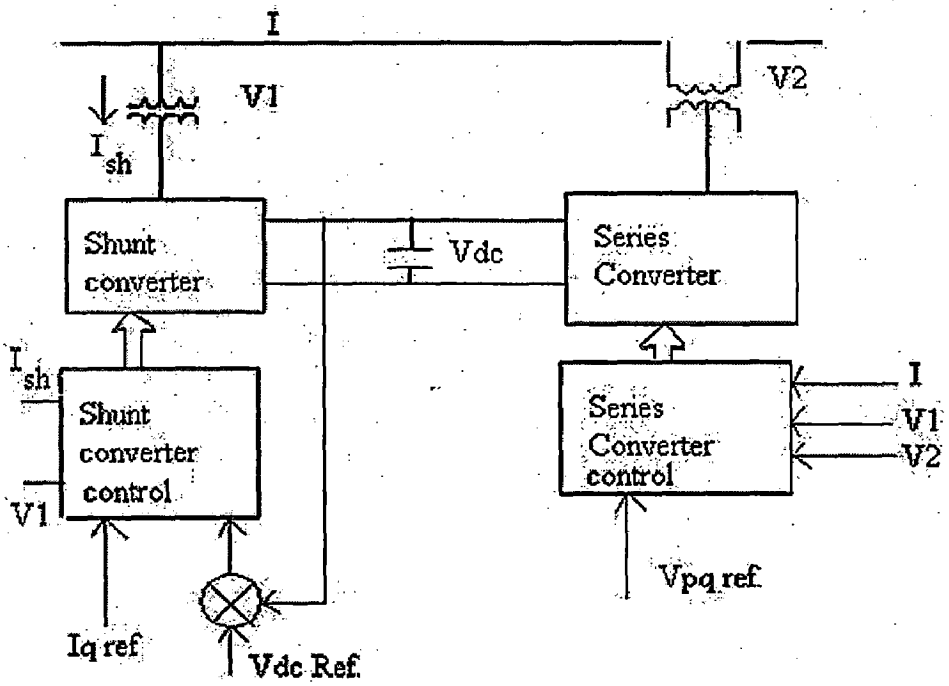


Figure 1.7: Basic UPFC control structure

The external or functional control operation control defines the functional operating mode of the UPFC and is responsible for generating the internal references,

i_{pRef} and $v_{pqRef,}$ for the series and shunt compensation to meet the prevailing demands of the transmission system [2, 6]. The functional operating modes and compensation demands, represented by external reference inputs, can be set manually by the operator or dictated by an automatic system optimization control to meet specific operating contingency requirements [6].

1.2.4 Different configurations of UPFC & literature review

Essentially, the requirements for implementing the UPFC with different types of converter topologies are [14];

1. To reduce the harmonic distortion in the output of the inverter, i.e. approximating the inverter output to the almost possible sinusoidal.

2. To increase the voltage and hence total power rating of the device.

3. To decrease the voltage stress on each power semi conductor device, by connecting the devices in series.

Recently, multi-level converters of various topologies have emerged as an alternative way of implementing low-distortion and high-power voltage source inverters [7]. In general, these converters synthesize the output voltage from a number of available DC voltage supplies held on storage capacitors. The complex phase shifting transformers of the multi-pulse converter are not needed and, in principle, the series connection of devices can be avoided.

Relevant review of literature

In [8],The neutral-point-clamped multilevel converter has been shown as an attractive implementation of the unified power flow controller because it facilitates back to back operation, high voltage operation (without direct series connection of devices) and low distortion (without the use of multi-pulse transformers). A UPFC using three converters is proposed. Two phase-shifted converters are required to provide a full range of voltage control of the series connection while ensuring low distortion and a balanced DC link. A single shunt converter is used. A commutation angle solution that balances the voltages of the multiple DC link capacitors is analyzed in terms of the active power

balance at each node. Control of shunt reactive power requires a variable DC link voltage. Control schemes for both shunt and series converters are developed and verified in terms of voltage balancing and power flow control on a micro-scale experimental system, using 5-level converters.This paper describes a back-to-back multi-level converter implementation of a UPFC which achieves independent control of the shunt and series voltage magnitudes, maintains capacitor voltage balance and maintains transmission quality harmonic distortion. The control system required for this UPFC is then examined.

Reference [10] compares four converter topologies for the implementation of flexible ac transmission system (FACTS) controllers: three multilevel topologies (multipoint clamped (MPC), chain, and nested cell) and the well-established multi pulse topology. In keeping with the need to implement very-high-power inverters, switching frequency is restricted to line frequency. The study addresses device count, dc filter ratings, restrictions on voltage control, active power transfer through the dc link, and balancing of dc-link voltages. Emphasis is placed on capacitor sizing because of its impact on the cost and size of the FACTS controller. A method for the dimensioning the dc capacitor filter is presented. It is found that the chain converter is attractive for the implementation of a static compensator or a static synchronous series compensator. The MPC converter is attractive for the implementation of a unified power flow controller or an interline power flow controller, but a special arrangement is required to overcome the limitations on voltage control.

In [14], proposes a novel UPFC based on 3-level half-bridge modules, isolated through single -phase multi winding transformers. The dynamic performance of proposed system was analyzed by simulations with EMTDC, assuming that the UPFC is connected with the 138-kV transmission line of one-machine-infinite-bus power system. The proposed system can be directly connected with the transmission line without series injection transformers. It has flexibility in expanding the operation voltage by increasing the number of 3-level half bridge Modules.

In [15], Operation of UPFC consisting of two VSCs is demonstrated through digital simulations studies on PSCAD/EMTDC software [17]. In this unified power flow

controller (UPFC) constructed by a back to back connection of a hysteresis current forced (HCF) converter and a pulse width modulated (PWM) inverter. The performance of the proposed switching schemes and associated controllers in providing the desired UPFC internal characteristics such as constant DC bus voltage and bi-directional power transfer capability is illustrated.

In this paper [16], the author has proposed a novel UPFC based on H-bridge modules, isolated through single-phase multi-winding transformers. The dynamic performance of proposed system was analyzed by simulations with EMTDC, assuming that the UPFC is connected with the 138-kV transmission line of one-machine-infinite-bus power system. The proposed system can be directly connected to the transmission line without series injection transformers. It has flexibility in expanding the operation voltage by increasing the number of H-bridge modules. The author has also given the various practical considerations of UPFC and also the realization of a simple power system with UPFC.

In [17], one method of meeting high mega volt ampere specifications by using multiple modules of two-level three-phase converter modules controlled by the phase-shifted triangle carrier technique of the sinusoidal pulse width modulation (SPWM) strategy. Two conceptual designs are presented. The first is the gate-turn-off (GTO)-SPWM-UPFC at the lowest switching rate, fc=fm = 3; to minimize GTO switching loss. The design is based on applying the fundamentals of SPWM theory to overcome unbalances arising from sideband harmonic interferences. The second is the insulated gate bipolar transistor (IGBT)-SPWM-UPFC, at fc=fm = 12 or higher, which SPWM theory assures that direct paralleling of the modules is free of current unbalance. A laboratory UPFC based on six modules of three-phase 5-kVA size IGBT converters operating at the baseline condition of dual unity displacement factor at the sending end and the receiving end has been implemented.

In [19], it is proved here that, as the diode-clamped, multilevel converter has been found to have attractive features for STATCOM application; there is interest in extending it to UPFC application by using multilevel converters as the series and the shunt converters. Unfortunately, as is demonstrated in this paper, the dc voltages at their dc

links are inherently unstable. Faced with this impasse, a solution is sought in a system of local feedback controlled Class B choppers to equalize the dc. Laboratory experimental model establishes the feasibility of the proposal. Digital simulations show that current ratings in the choppers need be only 10% of the current ratings in the converters. The chopper cost is estimated as 1% of the cost of the multilevel converters.

1.3 OUTLINE OF THE THESIS

In this thesis three different configurations of UPFCs have been considered. The considered configurations are

(1) UPFC using 2 levels, 6 pulse voltage source converters.

(2) UPFC based on 3-level Half-Bridge DC MLI Modules

(3) H-Bridge inverter module based UPFC.

The studies have been carried out through detailed digital simulations on PSCAD/EMTDC V4.1 for investigating the behaviors of UPFCs, the two area 4-M/c, 10 bus system [18] has been chosen.

In Chapter 2, the basic 2-level, 6 pulse voltage source converters are used as shunt and series inverters, which are triggered by two different techniques among the many methods that are available which are listed below. Here, Hysteresis current control (HCC) and PWM switching scheme have been used for the shunt and the series inverter respectively. The simulation results of this UPFC are also discussed at the end of this chapter.

In Chapter 3, the in-depth description of multi level inverters and different types are discussed. The idea and the basic operating principles of diode clamped multi level inverter are also given in this chapter. Later, the UPFC composed of 3 level, diode clamped half bridge inverter modules is being described in detail including the gate pulse generation scheme and structure of this configuration of UPFC. The block diagram of the used control system is also given here. The operation of the proposed system was verified through simulations with PSCAD/EMTDC as said earlier. This system can be directly

connected to the transmission line without series injection transformers. Detailed simulation description is also given including the inverter standalone simulations.

The detailed results of this configuration of UPFC based on 3 level, diode clamped half bridge inverter modules as controlling various parameters like controlling the bus voltage, real power and reactive powers is also given. The automatic power flow controller is also developed and its block diagram is also given and the corresponding results are also included at the end of this chapter.

Chapter 4 describe the operation of H-bridge inverter module based UPFC, isolated through single-phase multi-winding transformers. This system can be directly connected to the transmission line without series injection transformers. Detailed simulation description is also given including the inverter standalone simulations.

The results of this novel UPFC based on H-bridge modules as controlling various parameters like controlling the bus voltage, real power and reactive powers is also given. The automatic power flow controller is also developed and its block diagram is also given and the corresponding results are also included at the end of this chapter.

Chapter 5 broadly compares the different configurations of UPFC, which are simulated & described in above chapters. These configurations of UPFCs are compared on various parameters like, DC bus voltage magnitudes and its oscillations, switching frequency, harmonic content and also on the basis of their physical structure including the required no. of different components to implement practically for designing and put into operation. Finally the conclusions and future scope of thesis work have been presented.

1.3.1 Description of Test System

In this work, the four synchronous machines of the system are modeled as fixed voltage sources. All the transmission line parameters have been taken as lumped parameters. And the fixed loads at two different buses have been modeled as lumped impedance. The single line diagram of the above described system is as shown in Fig 1.8.

The system data is given in the Appendix. Simulation studies have been carried out by connecting the UPFC (each of the above three configurations) at bus no. 3.of the

above test system. The single line diagram of the above test system incorporating the UPFC is shown in Fig. 1.8.

The load flow result given in the same standard text book, shown in Appendix I is most accurately achieved in the modeled system using PSCAD/EMTDC V 4.1 and taken as the initial condition for simulating the performance of the UPFC.

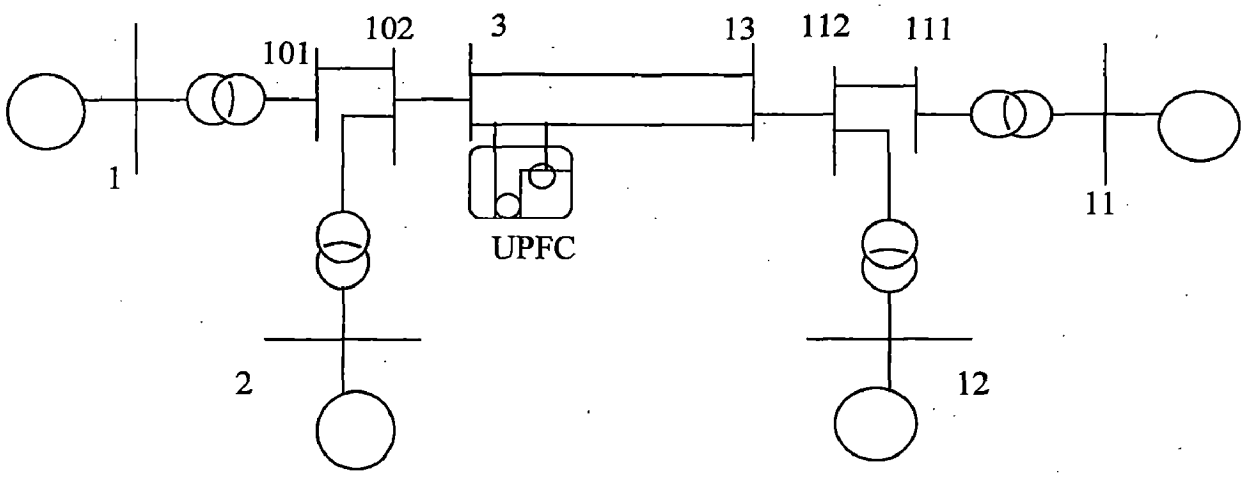


Figure 1.8: Single line diagram of the UPFC connected system

The graphical view of the simulated system in PSCAD/EMTDC is given in Appendix A. The steady state results of the above test system achieved with PSCAD/EMTDC are shown in Table 1.2. For comparison, the load flow results are given in [18] are also reproduced in Table 1.2. From this table it can be observed that these two results are close agreement.

Table 1.2: comparison of the actual and simulated results of the test system

Bus No.	Voltage mag. Load flow result (pu)	Voltage mag. Simulated result (pu)
1	1.03	1.03
2	1.01	1.01
11	1.03	1.03
12	1.01	1.01
101	1.0108	1.0106
102	0.9875	0.9871
111	1.0095	1.0089
112	0.9850	0.9848
3	0.9761	0.9731
13	0.9716	0.9698

1.4 conclusions

In this chapter, beginning with the introduction to FACTS into power systems and then the various types of FCATS Controllers are described briefly. The comparison of different FACTS controllers is also presented with concluding that, the UPFC is the most versatile Controller among all others. Later, the in-depth description of operating principle and control structure of UPFC are presented. I have finished this chapter by giving introduction to the test system considered for the simulation studies of various configurations of UPFCs.

UPFC using basic 2-level VSC

2.1 Introduction:

The basic operating principle and the control structure of UPFC are already discussed in previous Chapter 1. A UPFC consists of a shunt inverter, (exciter), a large DC capacitor and a series inverter (booster) as shown schematically in Fig. 2.1 [19].

In this chapter, the basic 2-level, 6 pulse voltage source converters are used as shunt and series inverters, which are triggered by two different techniques among the many methods that are available which are listed below. Hysteresis current control (HCC) and PWM switching scheme have been used for the shunt and the series inverter respectively. Detailed modeling of the UPFC has been carried out using PSCAD/EMTDC to develop a three-phase representation of a UPFC taking into account many practical constraints. The application of the UPFC in power system operation and control are illustrated in the test system described in chapter 1.

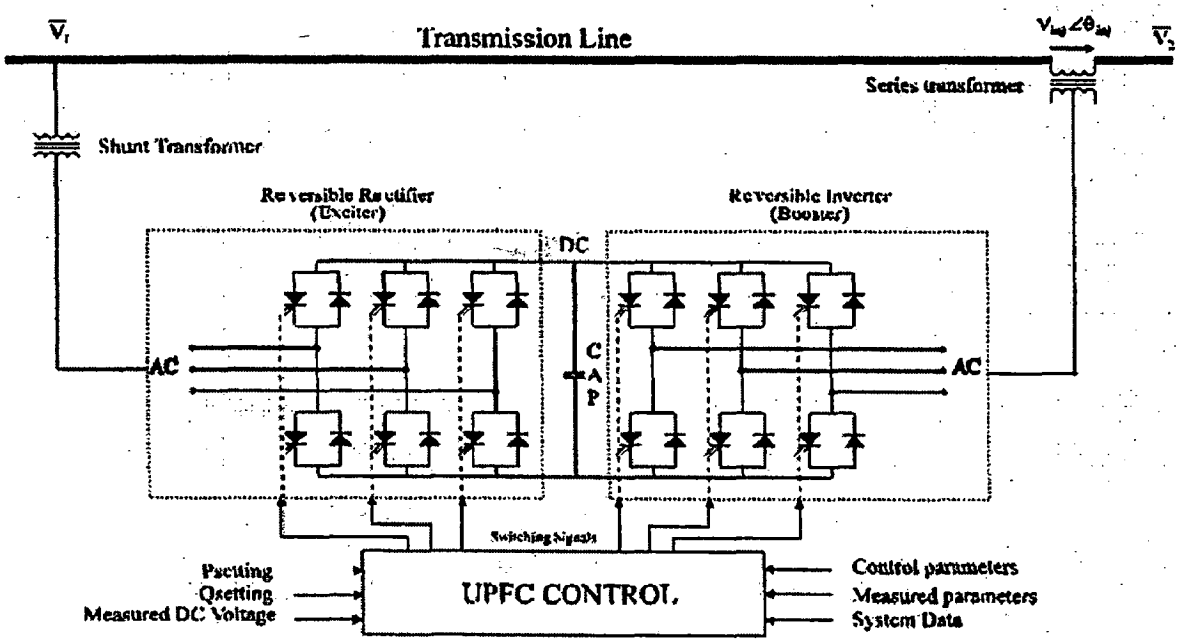


Figure 2.1: Schematic diagram of a UPFC using 2-level VSCs

2.2 Shunt Inverter switching scheme

The function of the exciter is to provide a constant DC bus voltage for the booster whether the power flow within the UPFC is from the exciter toward the booster or in the opposite direction. Hysteresis current forcing (HCF) is used here as the switching scheme for the exciter. The main reasons for selecting this technique are:

- The scheme is very simple to implement and its control technique is very adaptive to non-linear effects such as inductor saturation, switching delays and AC voltage fluctuations [23, 24].
- Several modules can operate in parallel to provide desired VA rating; and
- The response of the converter to change in power demand is very fast and the converter is robust to the fluctuations of the AC supply.

In HCF switching, the AC side current is forced to track a referenced current by high frequency switching of the switch pairs of the converter bridge. To limit the switching rate a hysteresis band is defined about the reference current and the input current is forced to stay within this band, as shown in the figure. To obtain a constant DC bus voltage, a controller is used to control the switching of the converter. The block diagram of this controller is shown in Fig 2.2. This controller regulates the DC bus voltage by modifying the reference current, i_{ref} and the hysteresis band, h. In HCF switching scheme, choosing the width of the hysteresis band is important, since a narrow band increases the switching frequency above the rated switching frequency of GTOs, whereas with a wide band a smooth and constant DC bus voltage is not achievable. Moreover, the harmonic distortion of the exciter current is increased with the band. In this HCF scheme for the UPFC, a variable hysteresis band proportional to the AC current is used. This band is selected as 14% of the peak amplitude of the input AC current as described by the following Equation [19].

$$h = 14\% \times Is = 14\% \times \sqrt{2} * P / (\sqrt{3} * 11kV) \approx 0.01 * P$$

where P is the three phase real power on the AC side; I_s the peak amplitude of the input current of the exciter; and h is the hystersis band.

2.2.1 Hysterisis Current Controls [23]

With the hysterisis control, limit bands are set on either side of a signal representing the desired output waveform. The inverter switches are operated as the generated signals within limits. Hysterisis-band PWM is basically an instantaneous feedback current control method of PWM where the actual current continually tracks the command current within a hysterisis band. Fig 2.3 shows the operating principle of hysterisis-band PWM for a half bridge inverter. The control circuit generates the sine reference current wave of desired magnitude and frequency, and it is compared with the actual phase current wave.

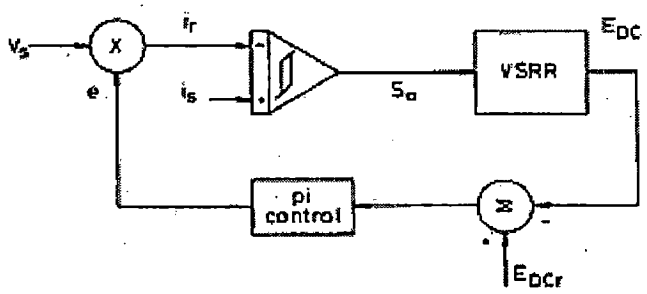


Figure 2.2: Simple hysteresis current control scheme

As the current exceeds a prescribed hysterisis band, the upper switch in the half-bridge is turned OFF and the lower switch is turned ON. As a result the output voltage transitions from $+0.5V_{dc}$ to $-0.5V_{dc}$, and the current starts to decay. As the current crosses the lower limit, the lower switch is turned OFF and the upper switch is turned ON [24]. A lock-out time (t_d) is provided at each transition to prevent a shoot-through fault. The actual current wave is thus forced to track the sine reference wave within the hysterisis band limits.

In a UPFC where E_{dc} is across a capacitor and is required to equal some reference level under different load conditions, it is necessary to produce a current reference that will cause the correct amount of power to flow in the right direction to maintain the bus voltage [23, 24].

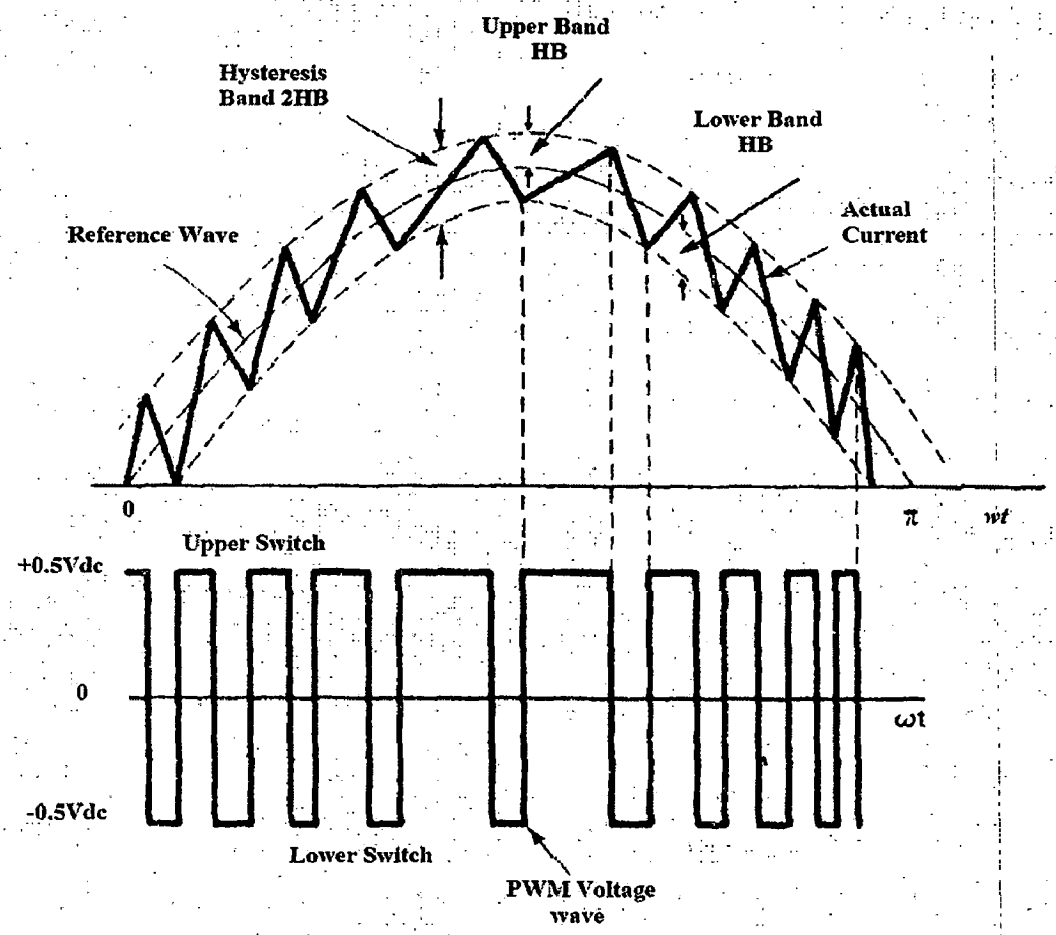


Figure 2.3 Generation of pulses for HCC control

A simple controller that can achieve this again can be explained with the help of Fig 2.2. The signal derived from the supply voltage is multiplied by an error term derived from the DC bus voltage to produce the required current reference, which is then compared with the current to determine which transistors are to be turned on. The process of generation of pulses for HCC scheme is already shown in Figure 2.3 [19].

2.3 Series Inverter switching scheme

Pulse width modulation (PWM) switching technique is used for the booster [20]. Naturally sampled triangulation method (NST) is implemented on the developed PWM inverter of the booster branch in the UPFC. The typical construction of a naturally sampled triangulation modulator is illustrated in Fig 2.4 [19]. In this technique the PWM switching points are defined by point-on-wave comparisons between a control sinusoidal waveform and a high frequency carrier (triangle) waveform. The comparator output is the PWM signal which determines the switching instants. The magnitude, frequency and phase of the fundamental component of the inverter output voltage can be controlled by changing the frequency, magnitude and phase of the control signal.

2.3.1 Sinusoidal Pulse Width Modulation [19, 20]

The sinusoidal PWM technique is very popular for industrial converters. In this, isosceles triangle carrier wave of frequency fc is compared with the fundamental frequency f sinusoidal modulating wave, and the points of intersection determine the switching points of power devices. The notch and pulse widths of Vao wave vary in sinusoidal manner so that average or fundamental component frequency is same as f and its amplitude is proportional to the command modulating voltage. The same carrier wave can be used for all 3 phases.

Fig. 2.4 illustrates the SPWM method. In this method, the switches are turned ON and OFF complimentarily at the instants at which the sinusoidal modulation signal and the triangular carrier signal intersect with each other. This method of encoding the modulating signal through the pulse width is accurate when the frequency of the carrier is sufficiently high. The modulation signal is amplified with a constant gain, without delay. In this regard, three indices are useful to characterize the operation of the SPWM technique.

(a) Modulation Index (M.I) [22] is defined as,

$$M.I(Ma) = \frac{Amplitude\_of\_\mathrm{mod}ulating\_wave\_}{Amplitude\_of\_carrier\_wave}$$

The properties of the Modulation Index are

- M.I. determines the fundamental component output voltage
- If 0<M.I<1 , V_1 = M.I (V_{in}) where V_1,V_{in} are the fundamental of the output voltage and input DC voltage respectively

(b) Modulation Ratio (Freq Ratio), M_R [22]:

$$M_R = \frac{Frequency\_of\_carrier\_wave}{Frequency\_of\_\mathrm{mod}ulating\_wave}$$

- Modulation ration determines the incident of harmonics in the spectra
- f=K.M_R (f_m), where f_m is the frequency of modulating signal and k is integer (1, 2, 3....)

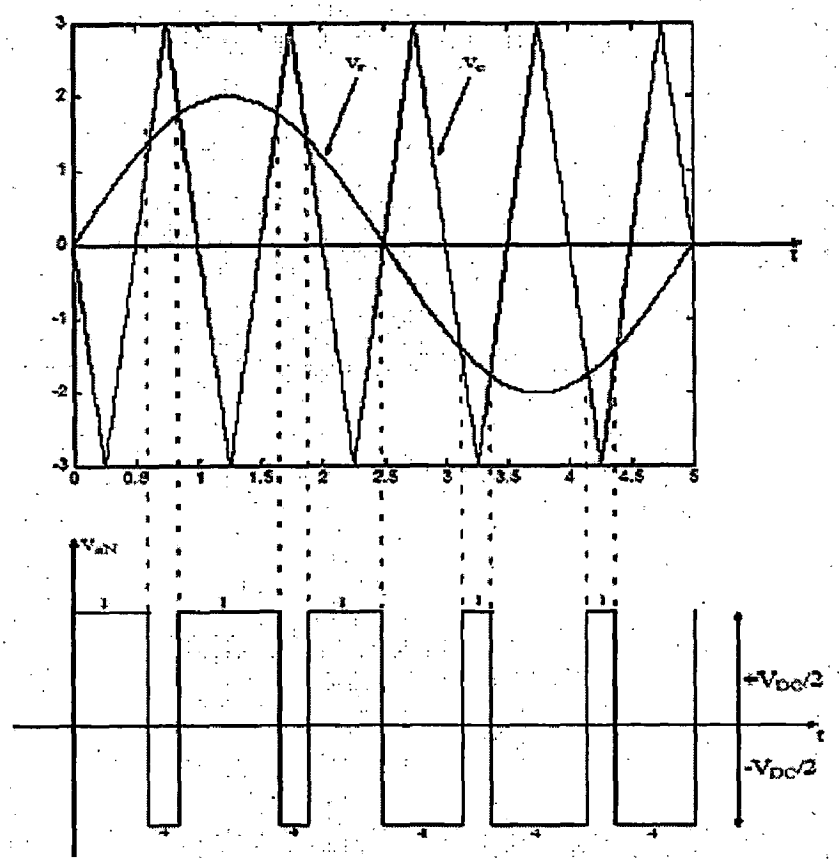


Figure 2.4: Illustrating the SPWM

(c) Total Harmonics Distortion (THD) [22]:

If V_n is voltage of n^{th} harmonic voltage;

$$THDv = \frac{\sqrt{\sum_{n=2}^{\infty}(V_{n,RMS})^2}}{V_{1,RMS}}$$

$$= \frac{\sqrt{V_{2,RMS}{}^2 + V_{3,RMS}{}^2 + ... + V_{2,RMS}{}^2}}{V_{1,RMS}}$$

An oscillator is used to generate a triangular carrier waveform at the switching frequency of the carrier signal. A modulated function, control signal, is generated separately and both applied to a comparator. The comparator as shown in Fig 2.5 generates a high output if control signal is greater than carrier signal and a low output when carrier signal is greater than control signal. Hence the output can be interpreted directly as a switching function. Moreover, since the triangle waveform has a voltage linearly dependent on time, the comparator has an output pulse width linearly dependent on the level of control signal

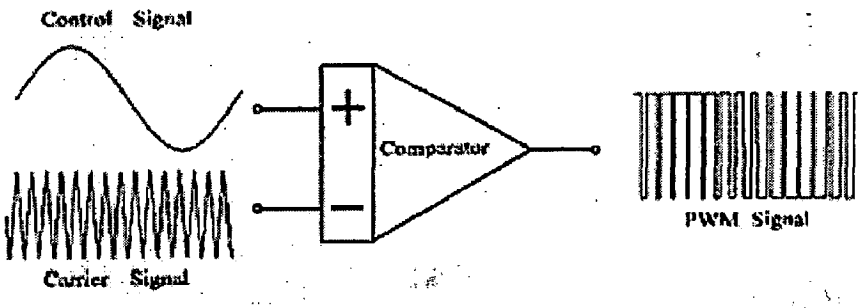


Figure 2.5: Generation of gate pulses for SPWM

2.4 Control Structure

For the purpose of simulating this simple configuration of UPFC, a simple control circuit for controlling the DC bus voltage to a fixed reference value has been chosen. By taking the sys bus voltage waveform and error in the DC bus voltage, passing it to the PI controller, reference current waveform is generated, which is to be tracked by the shunt converter. The block diagram of this controller is as shown in Fig 2.6 below [19].

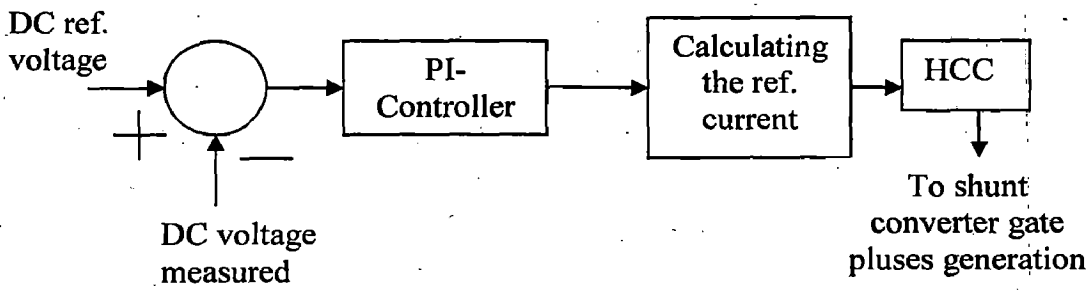


Figure 2.6: Block diagram of control system.

2.5 Simulation results

For simulation of this configuration of UPFC in a grid, the test system as described in chapter 1 has chosen. The PSCAD/EMTDC graphical view is given in Appendix B. The various parameters of the control system and the other apparatus are also given in Appendix B.

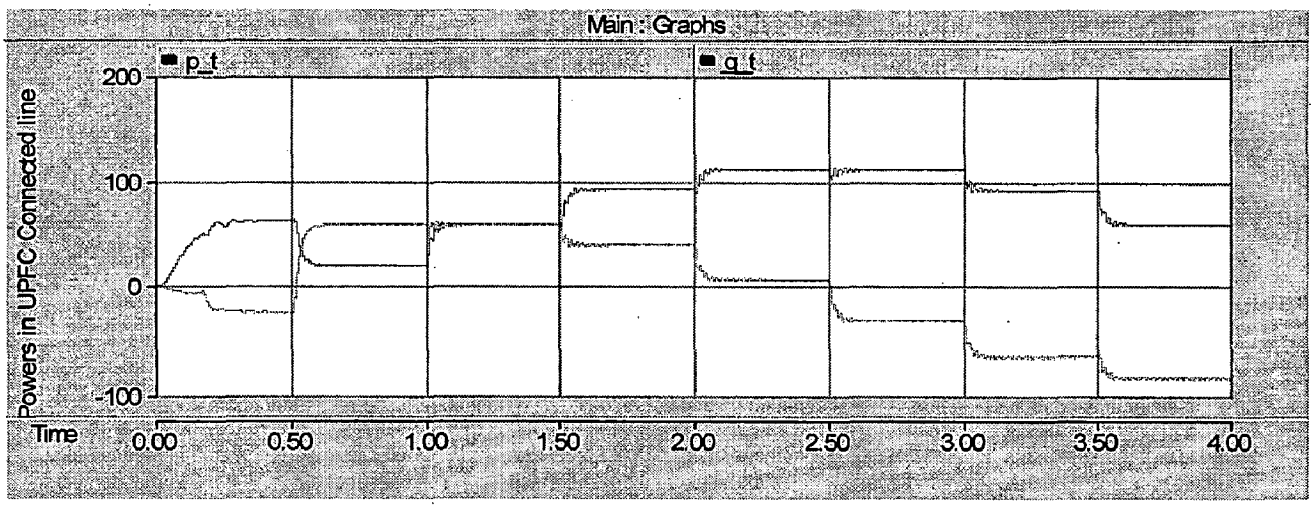
2.5.1 Case (I)

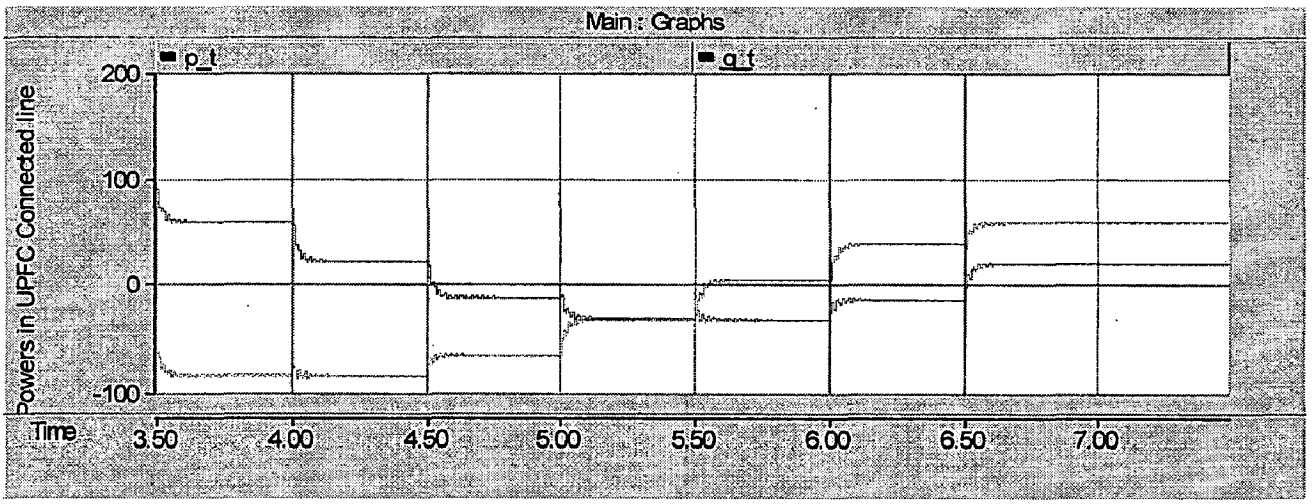
In this case, the parameters of the booster are varied to observe the resultant variations in the real and reactive power flow in the line. Specifically the modulation index of the booster has been kept fixed and phase angle of the injected booster voltage has been changed. The variations of both the real & reactive power flows in the lines, and other parameters are given in Figure 2.7 below. The parameters considered in this work are shown in Table 2.1 below.

Table 2.1: Simulation parameters used for this UPFC for case (i)

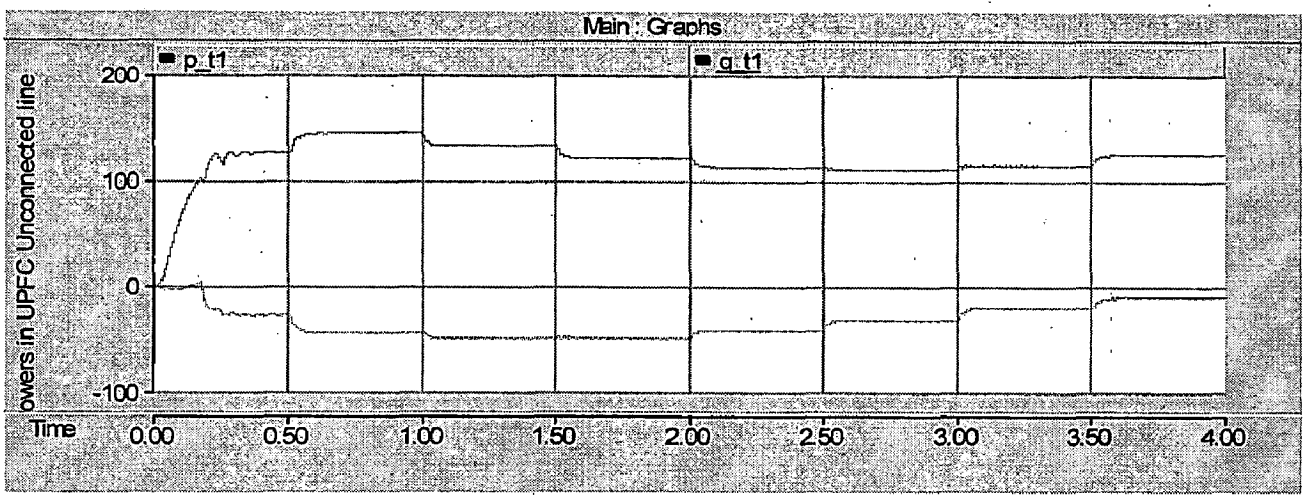
Time Duration Sec. (from-to)	Ma	Phase (degrees)	DC Bus ref. voltage (Kv)
0.5-1.0	0.9	0	25
1.0-1.5	0.9	30	25
1.5-2.0	0.9	60	25

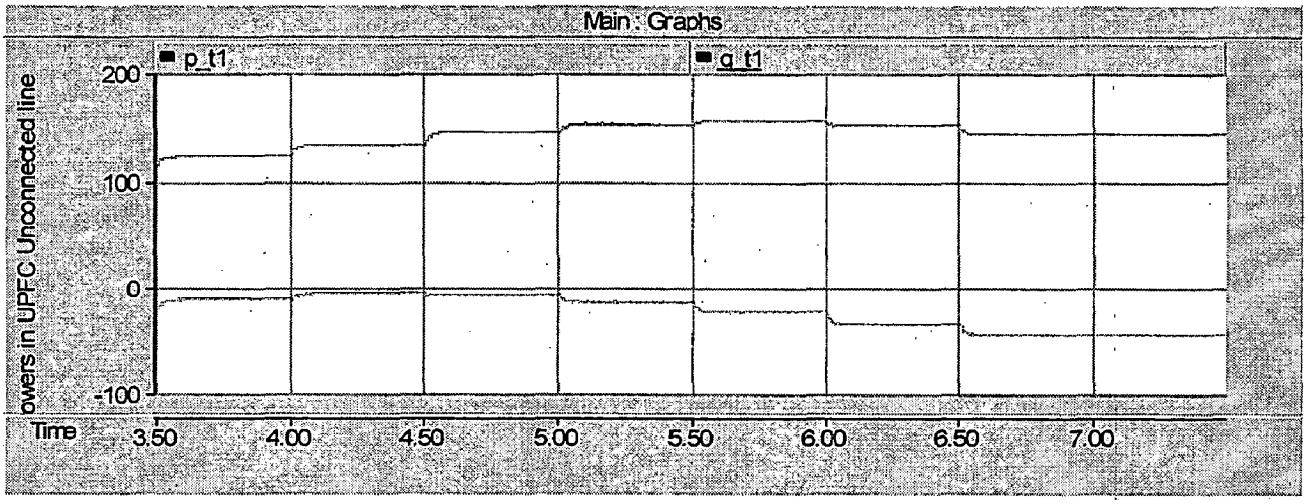
2.0-2.5	0.9	90	25
2.5-3.0	0.9	120	25
3.0-3.5	0.9	150	25
3.5-4.0	0.9	180	25
4.0-4.5	0.9	210	25
4.5-5.0	0.9	240	25
5.0-5.5	0.9	270	25
5.5-6.0	0.9	300	25
6.0-6.5	0.9	330	25
6.5-7.5	0.9	360	25



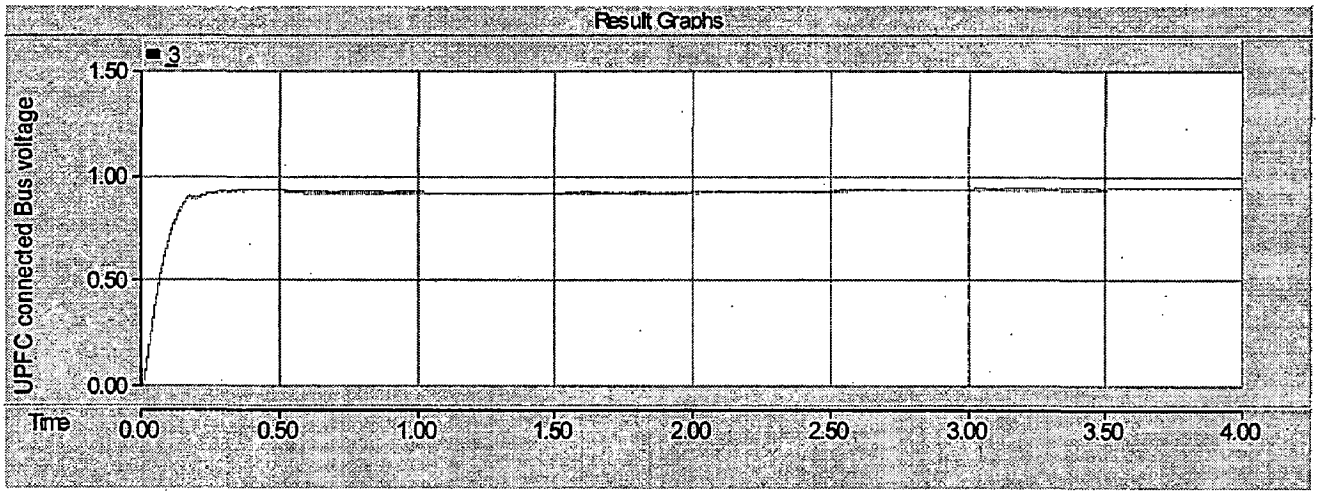


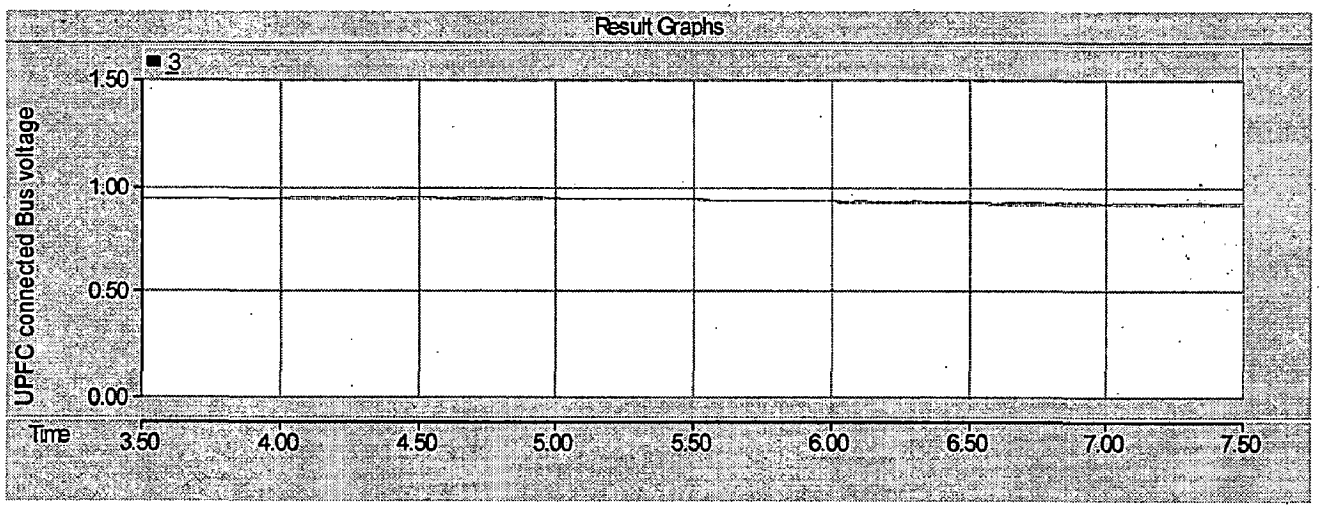
(a)


Main : Graphs
p_t1
q_t1
200
100
0
-100
owers in UPFC Unconnected line
Time
0.00
0.50
1.00
1.50
2.00
2.50
3.00
3.50
4.00

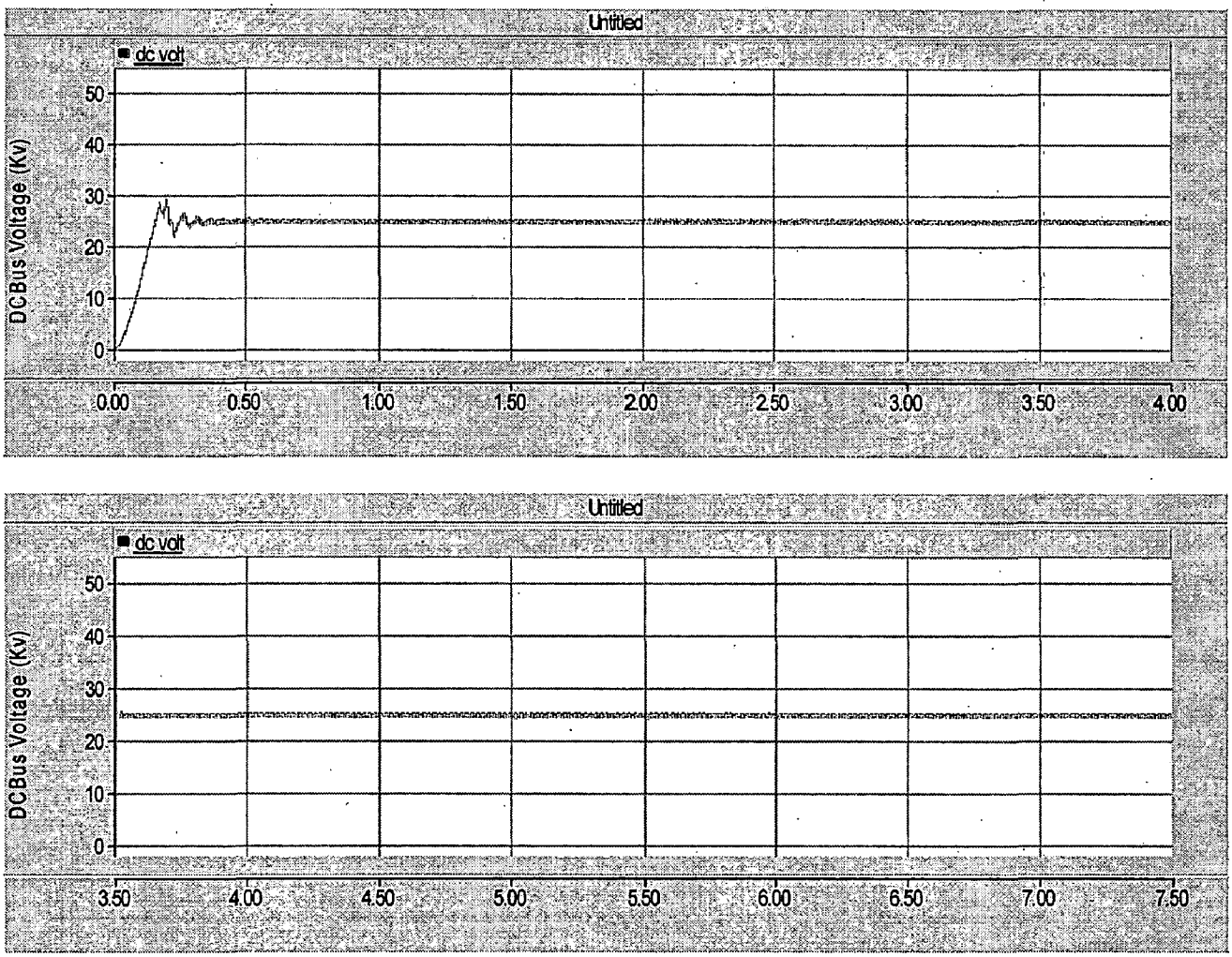

Main : Graphs
p_t1
q_t1
200
100
0
-100
owers in UPFC Unconnected line
Time
3.50
4.00
4.50
5.00
5.50
6.00
6.50
7.00

(b)


Result Graphs
3
1.50
1.00
0.50
0.00
UPFC connected Bus voltage
Time
0.00
0.50
1.00
1.50
2.00
2.50
3.00
3.50
4.00


Result Graphs
3
1.50
1.00
0.50
0.00
UPFC connected Bus voltage
Time
3.50
4.00
4.50
5.00
5.50
6.00
6.50
7.00
7.50

(c)



(d)

Figure 2.7: Simulation results of UPFC in open-loop control. (a) Real & Reactive powers in the UPFC connected line, (b) Real & Reactive powers in the UPFC un-connected line, (c) UPFC Connected Bus voltage, (d) DC Bus voltage.

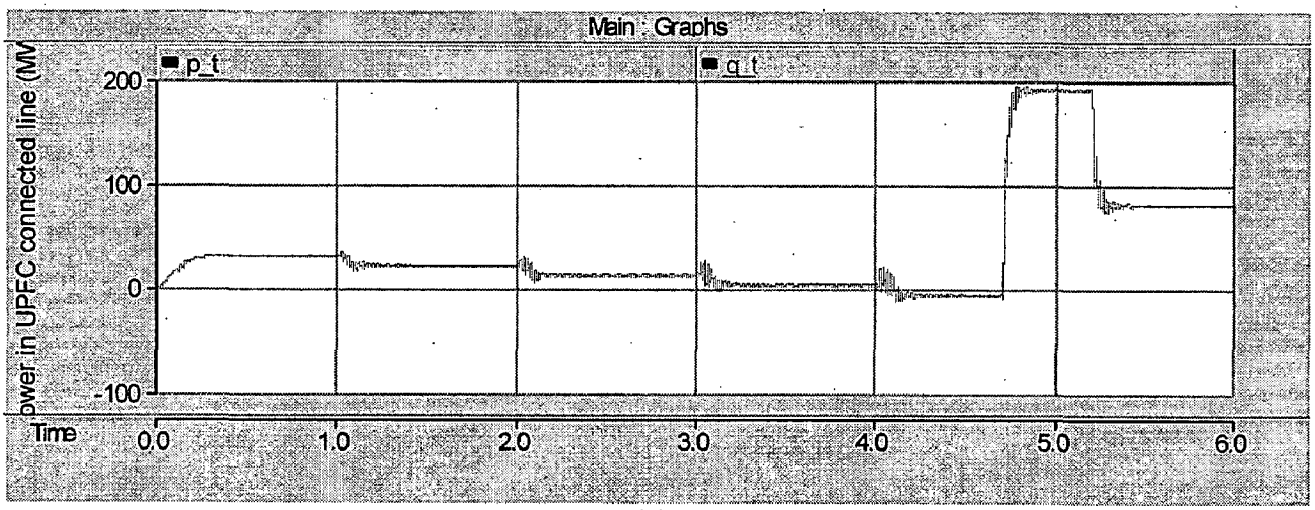
From Fig 2.7, it can be observed that under all variations of the booster parameters, the shunt inverter controller is able to maintain the DC capacitor voltage at the reference value, and correspondingly both the real and reactive powers are changing and coming to steady state.

2.5.2 Case (ii)

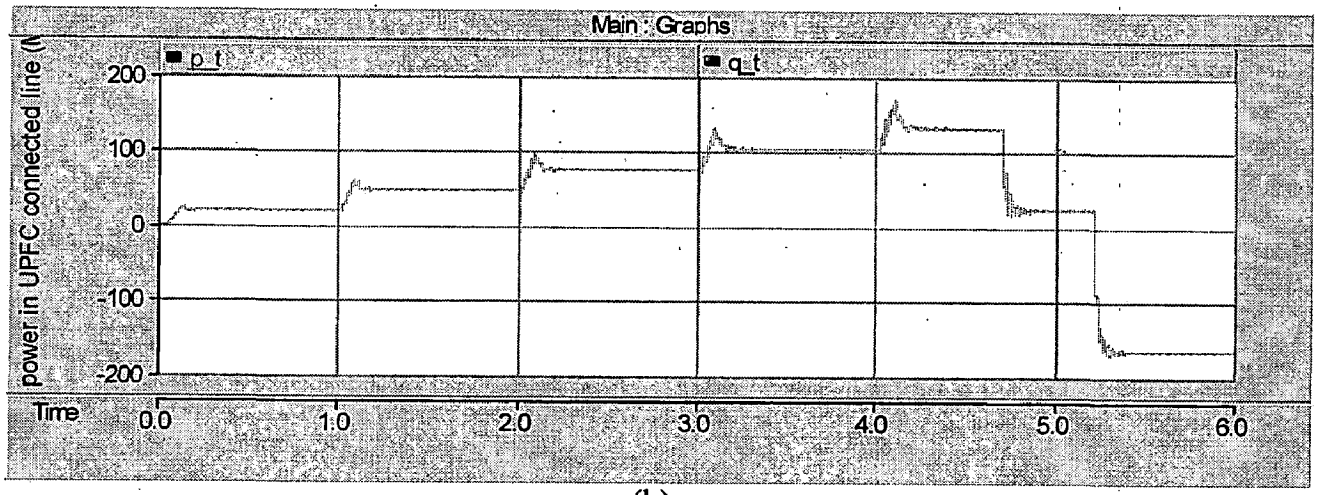
In this case, primarily the DC bus reference voltage has been changed and resultant variations in the line real and reactive powers have been noticed. Moreover, for some small duration, the phase of the injected booster voltage has also been varied. The variations of different parameters in the line are shown in Fig 2.8. The commanded parameters and the corresponding time intervals are listed in the Table 2.2. The Ref. DC Bus voltage is initially kept at 10 Kv, and is increased up to 50 Kv in the steps 10 Kv each time. The corresponding variations in both the real and reactive power are observed.

Table 2.2: Simulation parameters used for this UPFC for case (ii)

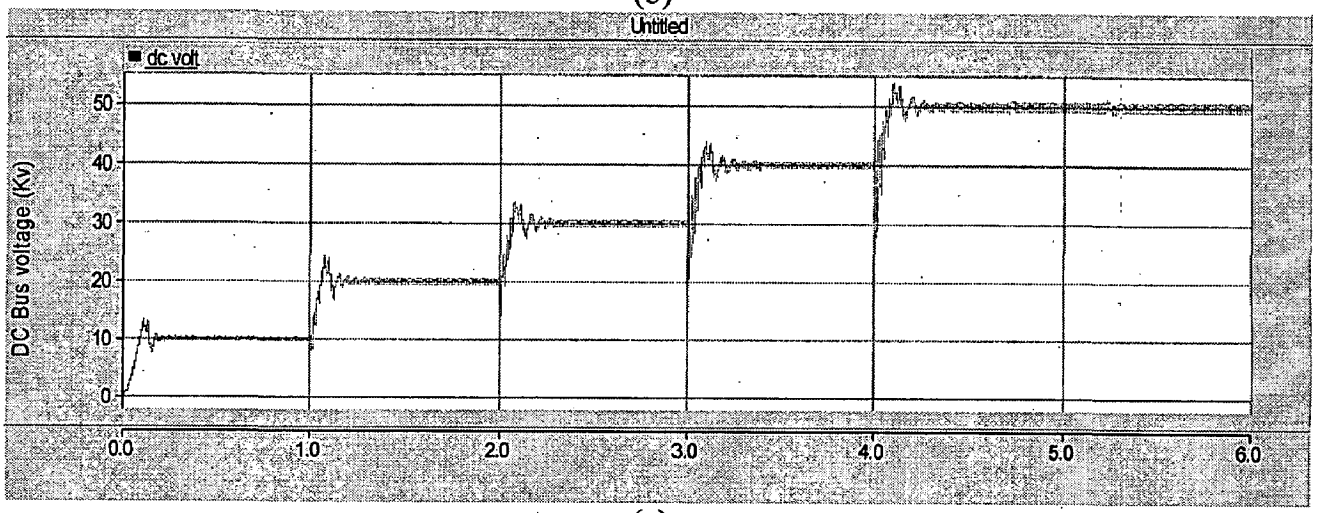
Duration sec. From - to	Ma	Phase (degrees)	DC Bus Ref (Kv)
0 -1.0	0.9	0	10
1.0 -2.0	0.9	0	20
2.0 -3.0	0.9	0	30
3.0 -4.0	0.9	0	40
4.0 - 4.7	0.9	0	50
4.7 – 5.2	0.9	90	50
5.2 – 6.0	0.9	180	50



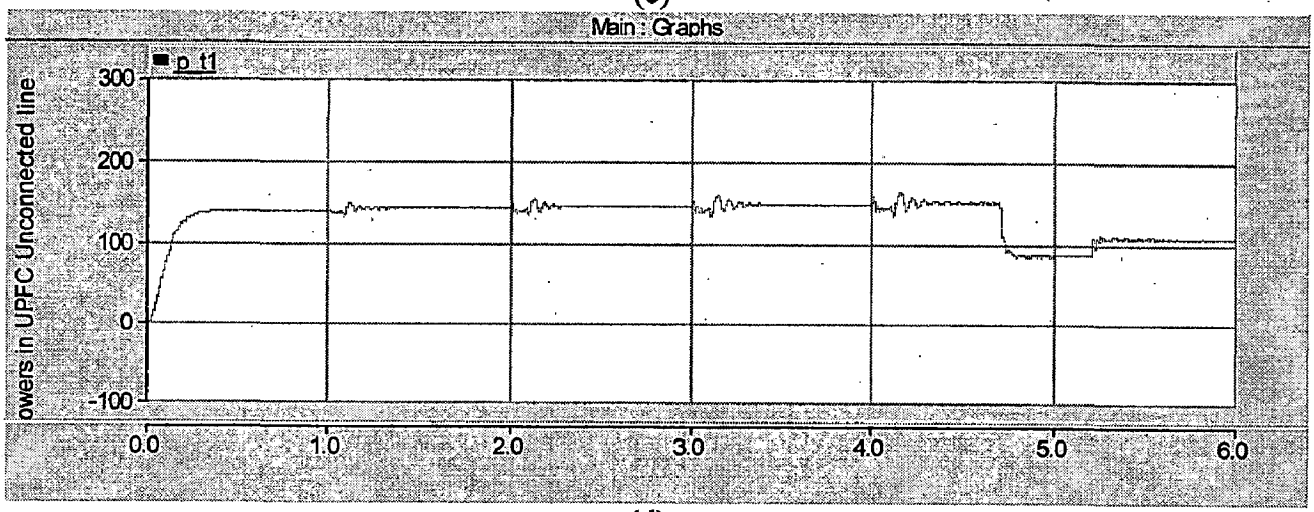
(a)


Main : Graphs
p_t
q_t
power in UPFC connected line (M
200
100
0
-100
-200
Time
0.0
1.0
2.0
3.0
4.0
5.0
6.0

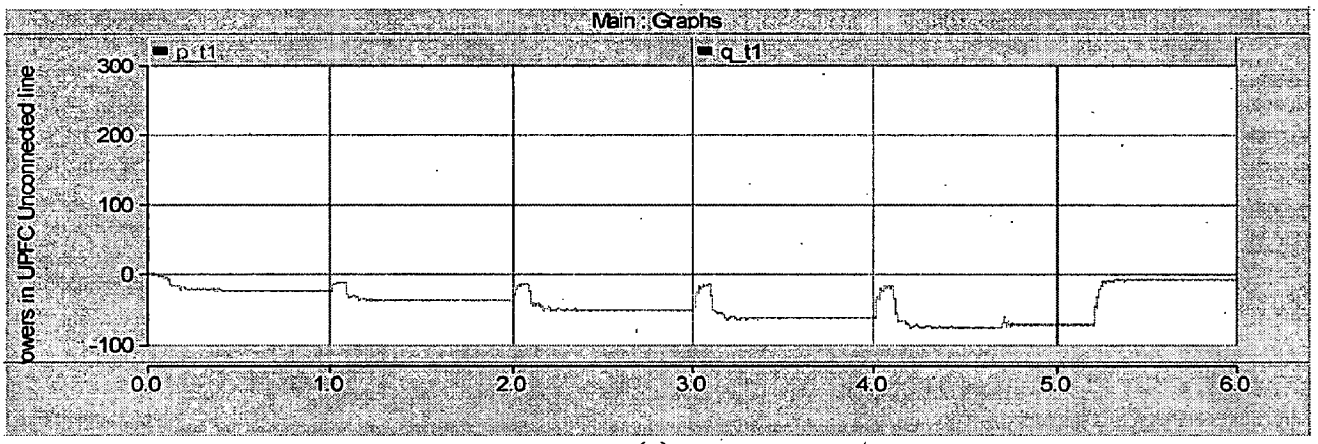
(b)


Untitled
dc volt
DC Bus voltage (Kv)
50
40
30
20
10
0
0.0
1.0
2.0
3.0
4.0
5.0
6.0

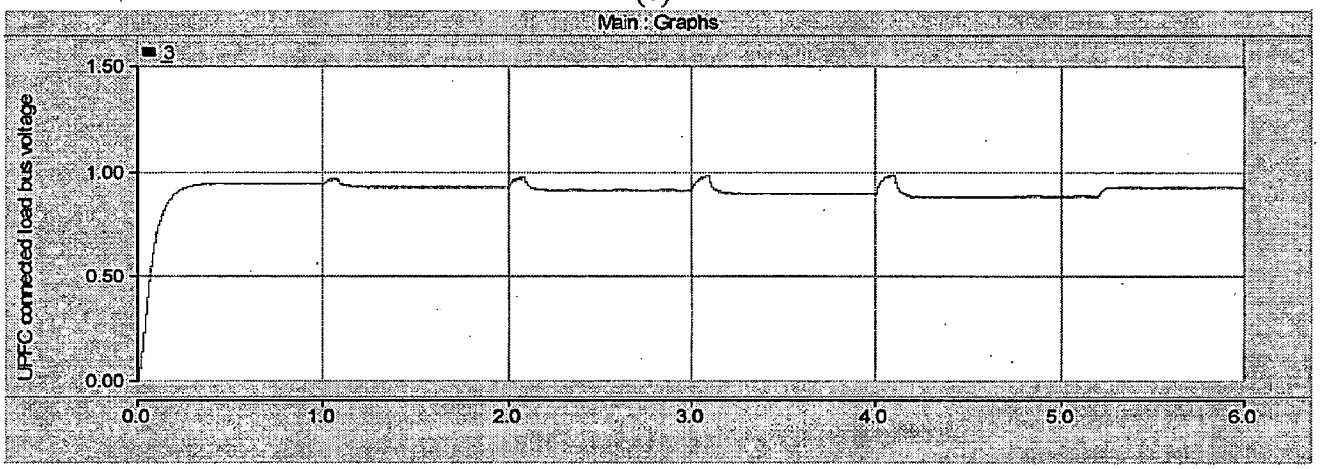
(c)


Main : Graphs
p_t1
owers in UPFC Unconnected line
300
200
100
0
-100
0.0
1.0
2.0
3.0
4.0
5.0
6.0

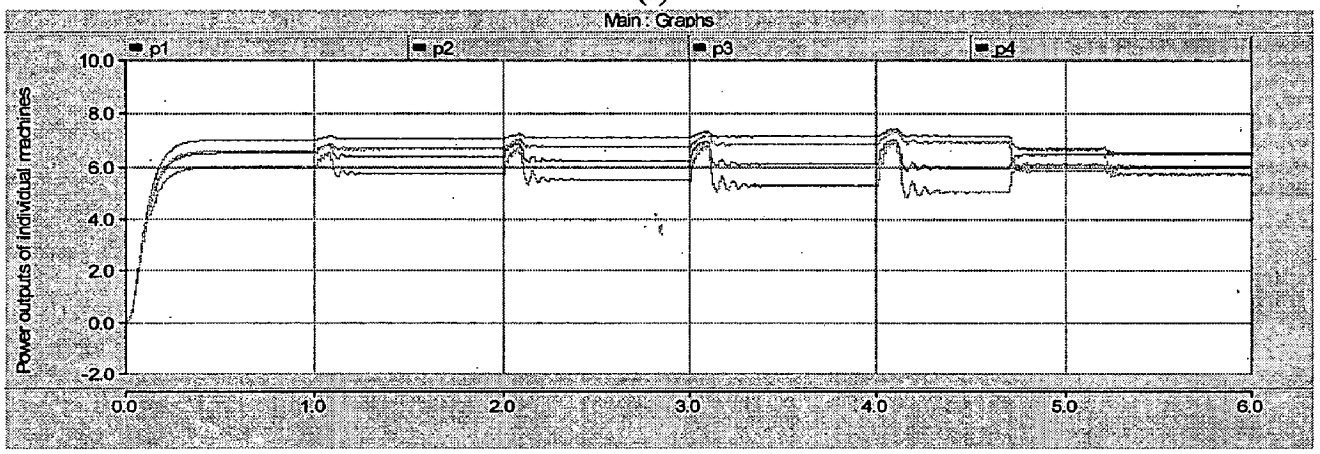
(d)



(e)



(f)



(g)

Figure 2.8: Simulation results of UPFC in open-loop control. (a) Real powers in the UPFC connected line, (b) Reactive powers in the UPFC connected line, (c) DC Bus voltages (d) Real powers in the UPFC un-connected line, (e) Reactive powers in the UPFC un-connected line, (f) UPFC Connected Bus voltage, and (g) Individual machine output powers.

As we are increasing the DC Bus ref. Voltage, immediately, the exciter controller will act, and the corresponding ref. current will be generated. The switching of shunt inverter will change to track the newly set ref. value. So the voltage across the capacitor and hence the DC side voltage of the series inverter will change to new value. Finally, the output voltage of the series inverter, which is a compensation voltage for the power system, will increase. So the compensation provided by the UPFC is going to increase, and reaches to new real and reactive power flows in the UPFC connected line.

The observation made here is that the increment in the DC Bus voltage results in series inverter output voltage, which is the compensation voltage provided by UPFC. This effect is same as if we would have increased the ma of the series inverter. So the effect of increasing ma of the series inverter and the DC Bus voltage is almost the same in the performance UPFC.

2.6 Conclusion

In this chapter, operation of a UPFC based on basic 2 level, 6 pulse VSC has been presented. An appropriate control scheme for the shunt converter has been designed. Simulation results for illustrating the operation of the u\UPFC in the transmission grid have been presented.

CHAPTER: 3

UPFC using 3-level Half-Bridge Diode-Clamped Multi level Inverter (DC MLI) Modules

3.1 Introduction

Conventional power electronic converters can switch each input or output connection between two possible voltage (or three possible current) levels, namely those of the internal DC voltage (or current) link. On the other hand, multilevel converters can switch their outputs between many voltage or current levels, and have multiple voltage or current sources (or simply capacitors or inductors) as part of their structure. A multilevel converter can be implemented in many different ways, each with attendant advantages and disadvantages. The simplest techniques involve the parallel or series connection of conventional converters to form the multilevel waveforms. More complex structures effectively insert converters within converters. Whatever approach is chosen, the subsequent voltage or current rating of the multilevel converter becomes a multiple of the individual switches, and so the power rating of the converter can exceed the limit imposed by the individual switching devices.

This chapter describes a UPFC based on 3-level half bridge diode clamped multi level inverter modules, isolated through single-phase multi-winding transformers. The operation of this system was verified through simulations with PSCAD/EMTDC. This system can be directly connected to the transmission line without series injection transformers.

3.1.1 Multilevel inverters

There are several types of multilevel inverters. The three main types of multilevel converters are: diode-clamped multilevel converters, flying-capacitor (also referred to as capacitor-clamped) multilevel converters, and cascaded H-bridges multilevel converters.

At this point, it seems appropriate to discuss the difference between the terms "multilevel converter" and "multilevel inverter." The term "multilevel converter" refers

to the converter itself. Furthermore, the connotation of the term is that power can flow in one of two directions. Power can flow from the ac side to the dc side of the multilevel converter. This method of operation is called the rectification mode of operation. Power can also flow from the dc side to the ac side of the multilevel converter. This method of operation is called the inverting mode of operation. The term "multilevel inverter" refers to using a multilevel converter in the inverting mode of operation. In this chapter, we will discuss different types of multilevel inverters later in more detail.

The main function of a multilevel inverter is to produce a desired ac voltage waveform from several levels of dc voltages [7]. These dc voltages may or may not be equal to one another. The ac voltage produced from these dc voltages approaches a sinusoid.

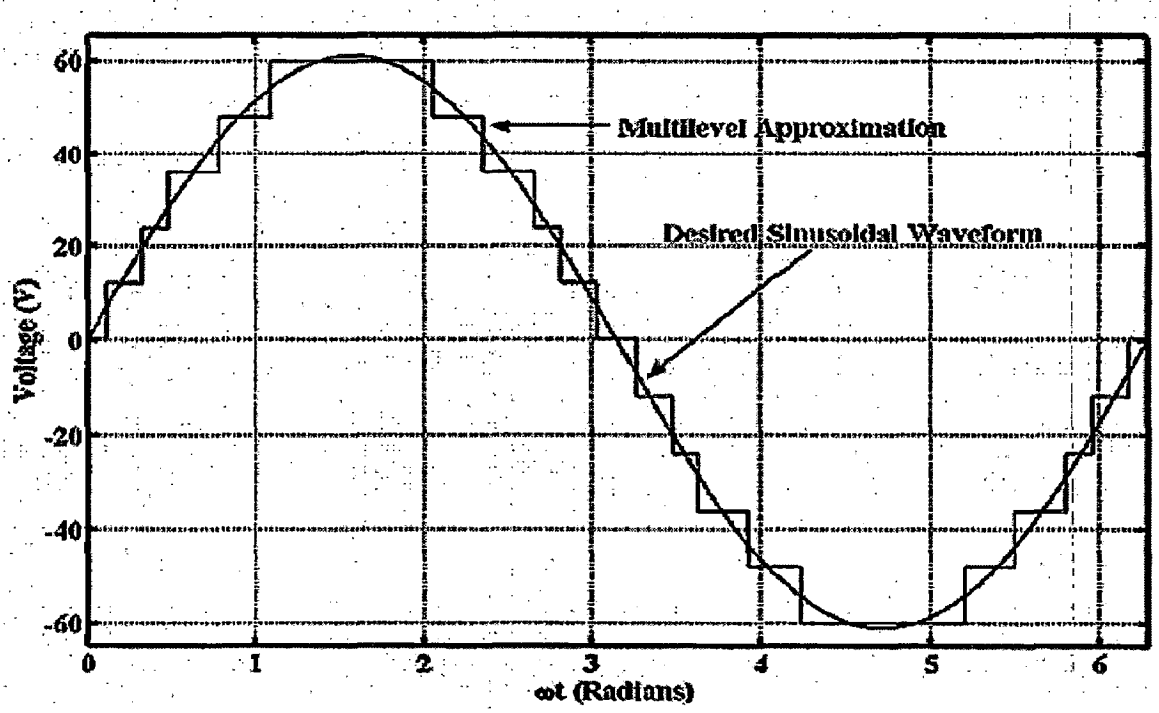


Figure 3.1: Output of a Multi level inverter.

As an example of a multilevel inverter, consider the staircase waveform in Fig. 3.1. In this figure, five 12 V dc sources produce a staircase waveform with a peak-to-Peak voltage of 120 V. In this case, the multilevel inverter produces a fair approximation

to a sinusoidal waveform [8]. As one increases the number of dc sources, this approximation will get better and better. Ideally, as the number of dc sources approaches infinity, the staircase waveform will approach the desired sinusoid.

Fig 3.1 also illustrates the "multilevel fundamental switching scheme." This scheme simply refers to determining the switching angles of the multilevel inverter such that a staircase waveform can be produced that approximates a sinusoid. Furthermore, the fundamental frequency of the produced staircase waveform and the frequency of the desired sinusoid are the same.

There are other switching schemes that can be implemented on a multilevel inverter but do not produce a staircase waveform [12]. Some examples include Bipolar Programmed PWM, Uni polar Programmed PWM, and Virtual Stage PWM.

One pitfall of using multilevel inverters to approximate sinusoidal waveforms concerns harmonics. As one can see in Fig. 3.1 the staircase waveform produced by the multilevel inverter contains sharp transitions. From Fourier series theory, this phenomenon results in harmonics, in addition to the fundamental frequency of the sinusoidal waveform.

However, by altering the times at which these sharp transitions occur, one can reduce and/or eliminate some of the unwanted harmonics. Furthermore, by increasing the number of dc sources, more harmonic content can be eliminated.

In the next session, the basic principle of a diode clamped multi level inverter is presented.

3.2 Basic Operating principle DC MLI

A three-level diode-clamped inverter is shown in Figure 3.2. In this circuit, the DC bus voltage is split into three levels by two series-connected bulk capacitors, C_1 and C_2. The middle point of the two capacitors n can be defined as the neutral point. The output voltage V_{an} has three states: $V_{dc}/2$, 0, and $-V_{dc}/2$. For voltage level $V_{dc}/2$, switches $S_1$and S_2 need to be turned on; for -Vdc/2, switches S_1' and S_2' need to be turned on; and for the 0 level, S_2 and S_1' need to be turned on.

The key components that distinguish this circuit from a conventional two-level inverter are D1 and D2. These two diodes clamp the switch voltage to half the level of the DC bus voltage. When both $S_1$and S_2 turn on, the voltage across 'a' and '0' is V_{dc}, i.e., $V_{a0} = V_{dc}$.

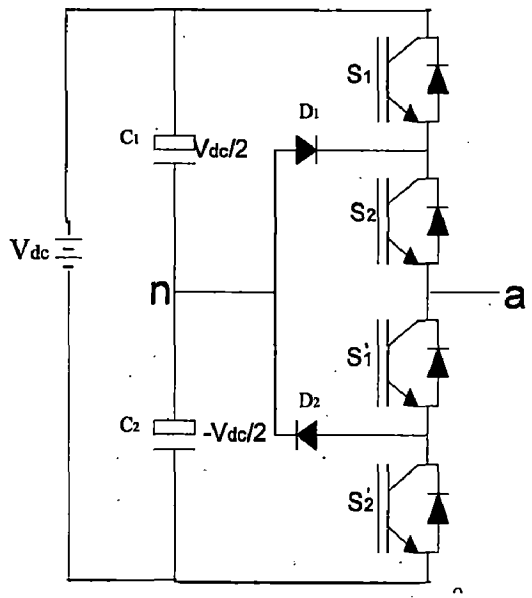


Figure 3.2: Three-level Diode-clamped multilevel inverter circuit topology

In this case, D2 balances out the voltage sharing between S_1' and S_2' with S_1' blocking the voltage across C_1 and S_2' blocking the voltage across C_2.Notice that output voltage v_{an} is ac, and v_{a0} is dc. The difference between v_{an} and v_{a0} is the voltage across C_2, which is Vdc/2. If the output is removed out between 'a' and '0', then the circuit becomes a DC/DC converter, which has three output voltage levels: V_{dc}, $V_{dc}/2$, and 0.

Fig 3.3 shows a five-level diode-clamped converter in which the dc bus consists of four capacitors, C1, C_2, C_3, and C4. For dc-bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/4$, and each device voltage stress will be limited to one capacitor voltage level $Vd_c/4$ through clamping diodes. The switching states are given in Table 3.1.

There are 5 switch combinations to synthesize five level voltages across *a* and *n*.

1) For voltage level $V_{an} = V_{dc}/2$, turn on all upper switches S_1-S_4.

2) For voltage level $V_{an} = V_{dc}/4$, turn on three upper switches S_2-S_4 and one lower

switch S_1'.

3) For voltage level $V_{an} = 0$, turn on two upper switches S_3 and S_4 and two lower switches S_1' and S_2'.
4) For voltage level $V_{an} = -V_{dc}/4$, turn on one upper switch S_4 and three lower switches S_1'-S_3'.
5) For voltage level $V_{an} = -V_{dc}/2$, turn on all lower switches S_1'-S_4'.

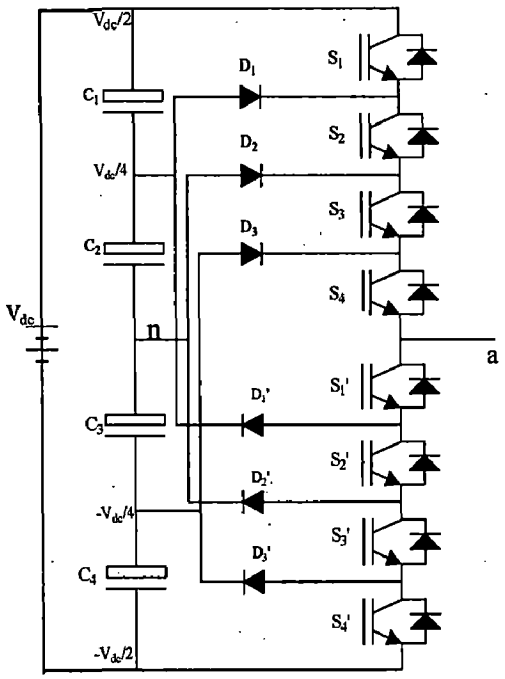


Figure 3.3: Five-level Diode-clamped multilevel inverter circuit topology

Table 3.1: switching states of 5-level DC MLI

	S_1	S_2	S_3	S4	S_1'	S_2'	S_3'	S_4'
Vdc	1	1	1	1	0	0	0	0
Vdc/4	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
-Vdc/4	0	0	0	1	1	1	1	0
-Vdc/2	0	0	0	0	1	1	1	1

Although each active switching device is only required to block a voltage level of V_{dc}/ (m - 1), the clamping diodes must have different voltage ratings for reverse voltage blocking. Using D_1' of Figure 3.3 as an example, when lower devices $S_2' \sim S_4'$ are turned on, DI needs to block three capacitor voltages, or 3Vdc/4. Similarly, D_2 and D_2' need to block $2Vd_c/4$, and D_{a3} needs to block $3Va_c/4$. Assuming that each blocking diode voltage rating is the same as the active device voltage rating, the number of diodes required for each phase will be (m - 1) x (m - 2). This number represents a quadratic increase in m. When m is sufficiently high, the number of diodes required will make the system impractical to implement. If the inverter runs under PWM, the diode reverse recovery of these clamping diodes becomes the major design challenge in high-voltage high-power applications.

Unequal device rating:

The switch S1 conducts only during Va0= Vdc/2, while switch S4 conducts over the entire cycle except Va0=0. Such an unequal conduction duty requires different current for switching devices, the outer switches may be oversized and the inner switches may be undersized.

Capacitor voltage unbalance:

A power needs to transfer real power from ac to dc (rectifier) or dc to ac (inverter). When operating at unity power factor, the charging time for rectifier operation or discharging time for inverter operation for each capacitor is different.

The voltage unbalance problem is solved by several approaches, such as replacing capacitors by a controlled constant dc voltages source such as pulse width modulation (PWM) voltage regulators or batteries. The use of controlled dc voltage results in system complexity and cost penalties. The converter switching frequency should be kept, minimum to avoid switching losses and electromagnetic interference problems.

When operating at zero power factors, the capacitor voltages can be balanced equal charge and discharge in one half cycles.

3.2.1 Advantages:

1. When the no. of levels is high enough, harmonic content will be low enough to avoid the need for filters.
2. Efficiency is high because all devices are switched at the fundamental frequency
3. Reactive power flow can be controlled.

3.2.2 Disadvantages:

1. Excessive clamping diodes are required when the number of levels is high.
2. It is difficult to do real power flow control for the individual inverter.

3.3 Structure of UPFC

Here, a novel UPFC based on several pairs of 3-level half bridge diode clamped multi level inverter modules per phase as shown in Figure. 3.4 is designed. Each pair has two 3-level half bridge diode clamped multi level inverter modules connected in parallel through a common dc link capacitor.

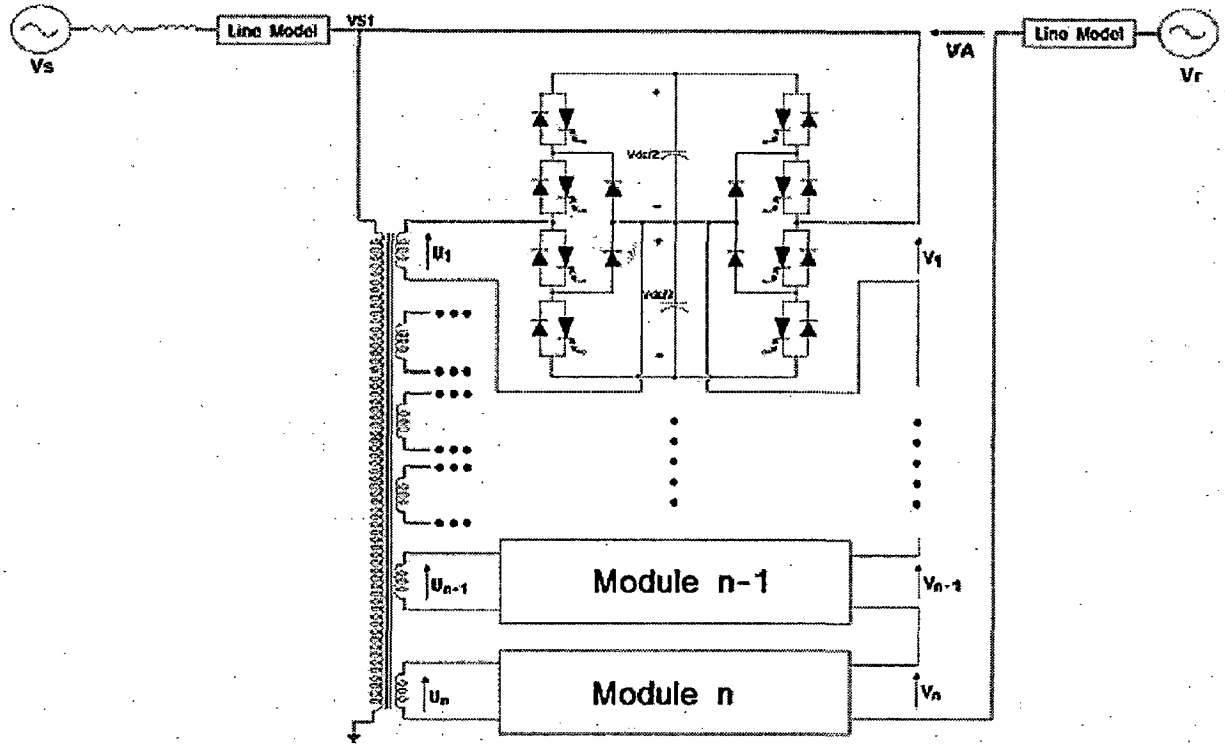
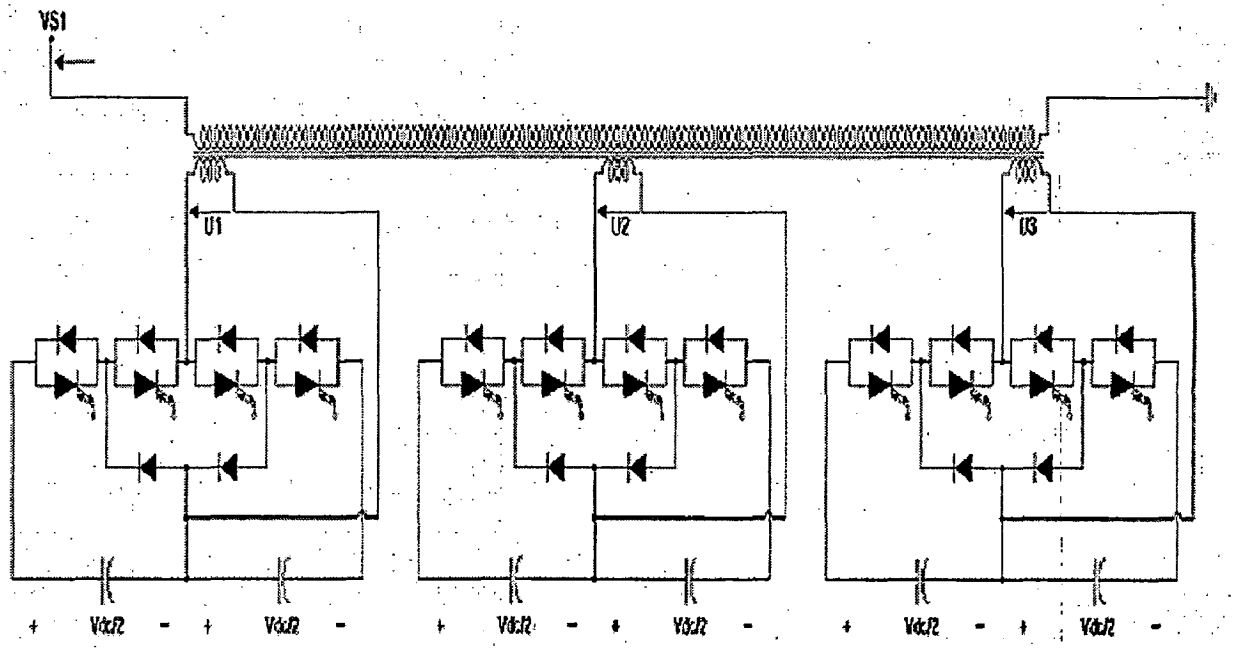
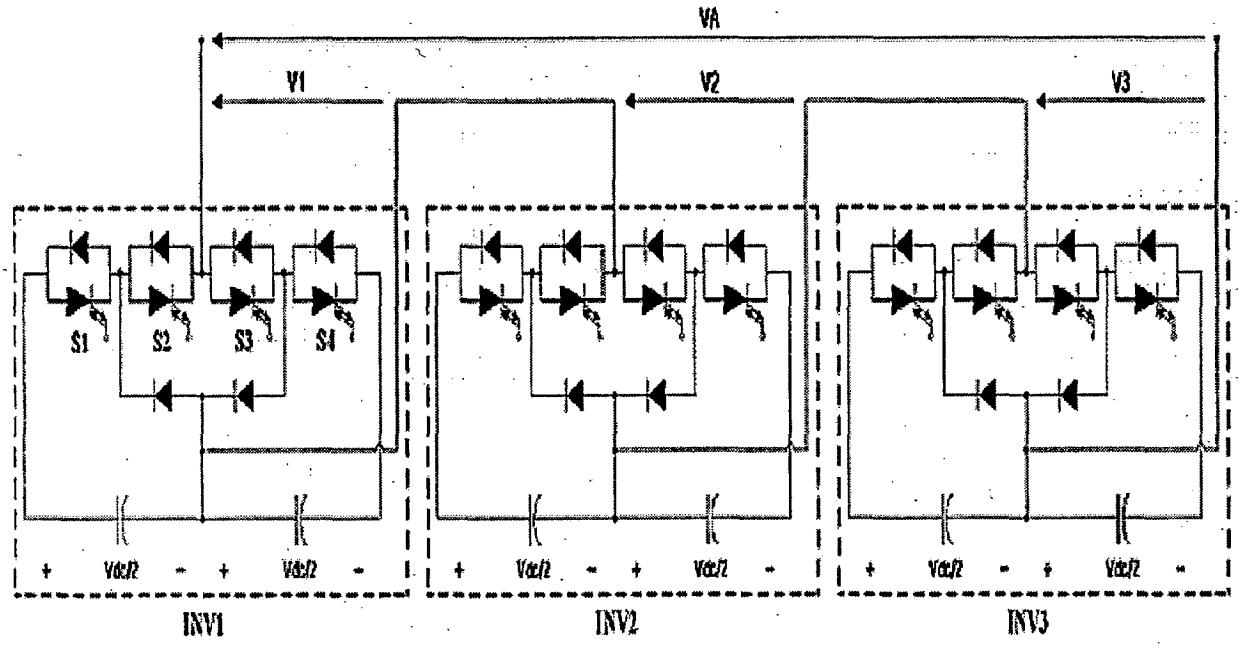


Figure 3.4: Configuration of UPFC using 3-level DC MLI

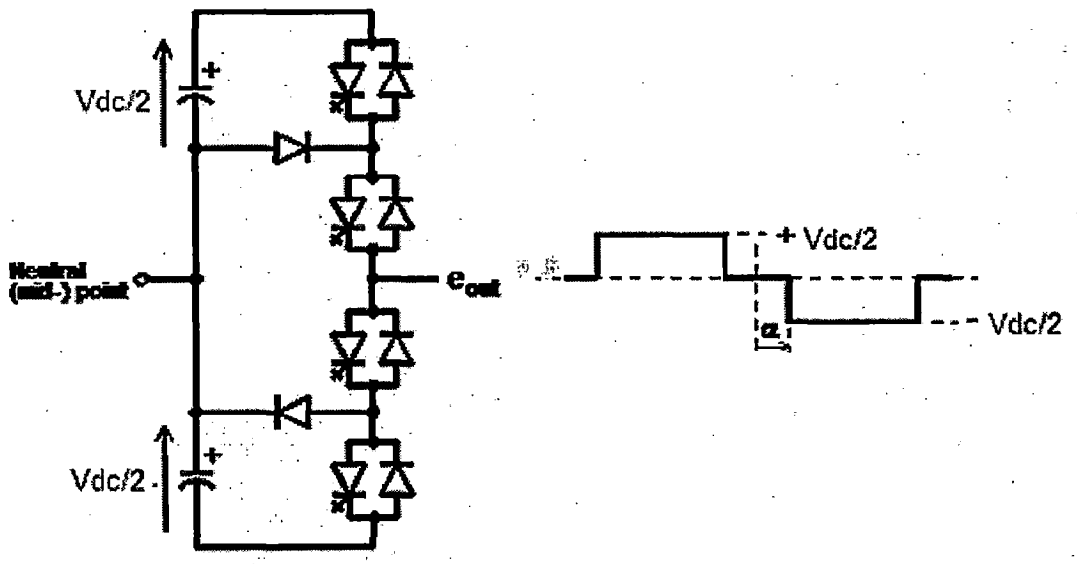
This configuration proposes a novel UPFC based on several pairs of 3-level half-bridge modules per phase as shown in Fig. 3.4 Each pair has two 3-level half-bridge modules connected in parallel through a common dc link capacitor. One 3-level half-bridge module in shunt part is connected in series through single-phase multi-winding transformer for isolation purpose. The other 3-level half-bridge is directly inserted in the transmission line. For the purpose of simulation studies in this thesis, the shunt and series parts are assumed to be composed of three 3-level half-bridge modules per phase as shown in Fig. 3.5(a) and 3.5(b).



(a)



(b)



(c)

Figure 3.5: Inverter structure and switching pattern (a) Shunt part inverter (b) Series part inverter (c) Output voltage formation

Table 3.2: Switching pattern of 3-level DC MLI

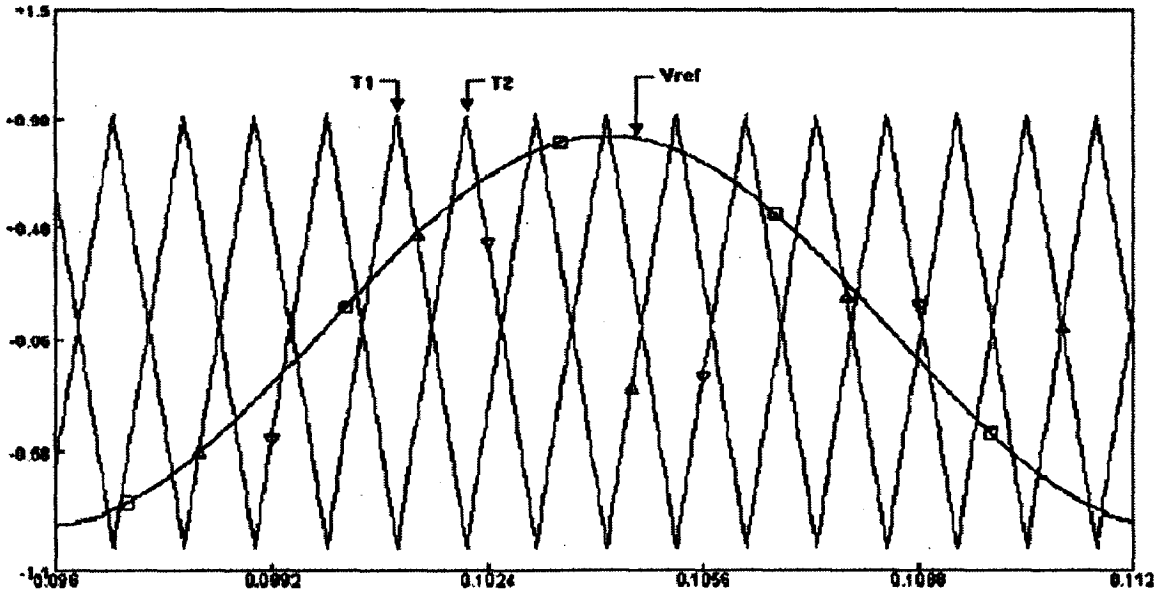
V1A	Switching state
V_{dc}	S_1, S_2: on and S_3, S_4: off
0	S_2, S_3: on and S_1, S_4 off
$-V_{dc}$	S_3, S_4: on and S_1, S_2: off

The output voltage of one module and switching patter can be explained in Fig. 3.5(c). The output of each module has three states $+V_{dc}$, 0, $-V_{dc}$ depending on states of switch S_1-S_4. Table 3.2 shows relationship between output voltage and switching state. By adjusting duration time, the output voltage can be adjusted.

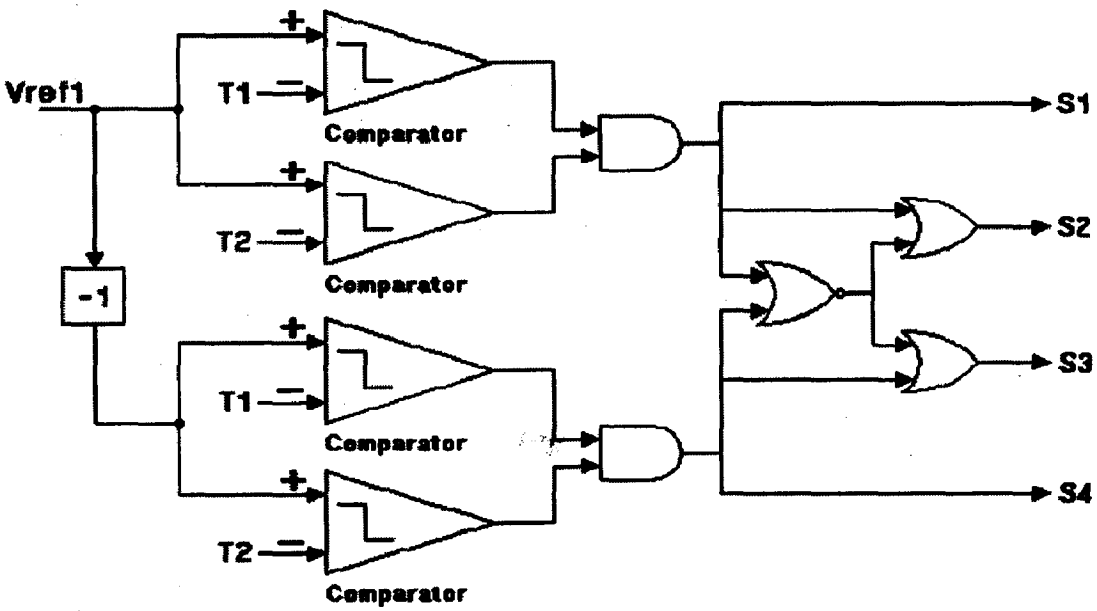
3.3.1 Gate Pulses Generation

Fig. 3.6 shows the principle of PWM gate-pulse generation for the proposed UPFC. The basic principles of sinusoidal pulse width modulation technique are already described in earlier chapter: 2. Figure 2.4 illustrates the SPWM method based on using the intersection points of the modulation signal and the triangle carrier signal as the time instants for turning the switches in a given phase, complementarily ON and OFF.

Fig. 3.6 shows a principle of gate-pulse generation for PWM scheme. Fig. 3.6 (a) shows two carrier signals and the reference signal to generate the gate pulses for inverter module INV1. The frequency of carrier T1, T2 is 450[Hz]. Each of two carriers has 180 °phase shift with each other. Carriers to generate gate pulses for other inverter module have 120°phase shift with each other. The reference signal V_{ref} has maximum value of 1.0 in per unit and has a sinusoidal waveform of 50Hz. Fig. 3.6 (b) shows how to generate the gate pulses using the reference and carrier signals. Carrier T1 and T2 are used as the input to generate gate pulses for inverter module.



(a)



(b)

Figure 3.6: Principle of gate pulse generation (a) Carrier and reference signal (b) Gate pulse generation scheme

As explained before, the carrier shown in Fig. 3.6(a) is used to generate gate pulses for building up output voltage V1. Two sets of 4 carriers with 180° phase shift

from each other are needed to generate gate pulses for building up output voltage V2 and V3. These sets of carriers have 120° phase shift with each other. Since each carrier has a frequency of 450[Hz] and there are six carriers, total output voltage V_A has an equivalent switching effect of 3[kHz]. The complete details of the ref. sine wave and carrier wave of all the modules are given in Table 3.3 below.

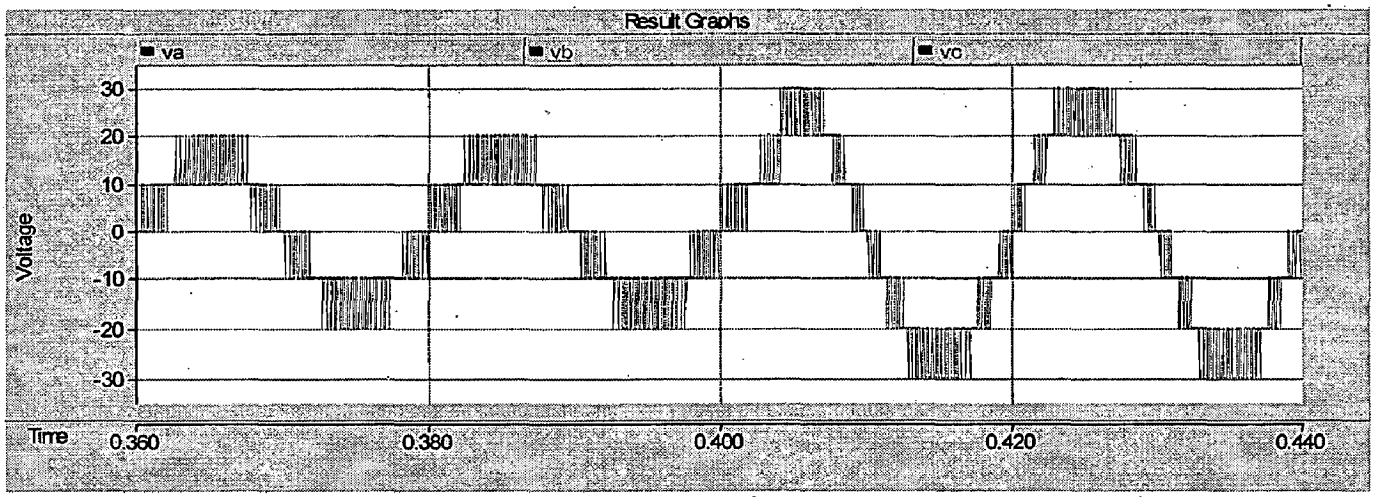
Table 3.3: The complete details of the ref. sine wave and carrier wave of all modules.

Ref. & carriers for V_1	$V_{ref} = m_a \sin(wt)$ $T_1, -T_1$	$V_{ref} = m_a \sin(wt-120)$ $T_1, -T_1$	$V_{ref} = m_a \sin(wt+120)$ $T_1, -T_1$
Ref. & carriers for V_3	$V_{ref} = m_a \sin(wt)$ $T_3 - T_1 \angle 120, -T_3$	$V_{ref} = m_a \sin(wt-120)$ $T_3 - T_1 \angle 120, -T_3$	$V_{ref} = m_a \sin(wt+120)$ $T_3 - T_1 \angle 120, -T_3$

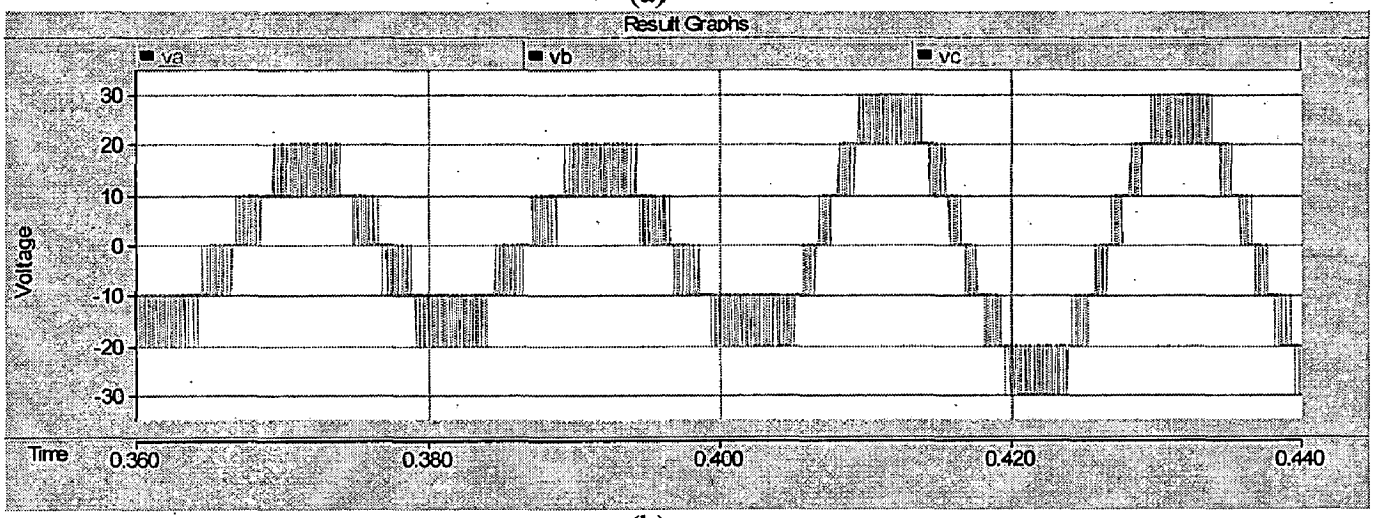
3.4 simulation results of a standalone inverter

To study the diode clamped multi level inverter, the inverter is initially has been simulated in a stand alone mode. It can be observed that large numbers of harmonics are involved in the output of one module, while significantly small numbers of harmonics are involved in the output of cascaded three modules.

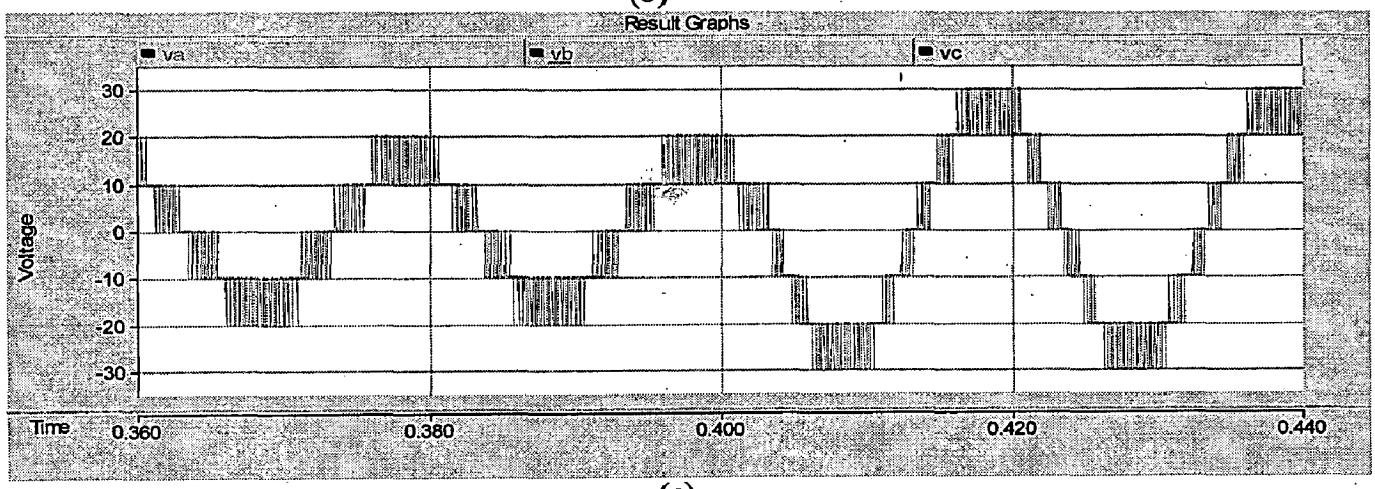
The phase voltages Va, Vb, Vc are as shown in Fig. 3.7. In these results, initially the modulation index (m_a) has been fixed at a value 0.4 and it has been increased to a value of 0.9 at time t=0.4 sec. the DC voltage Vdc has been kept at 1.0 pu. The output voltages of each individual modules of phase a are as shown in Fig. 3.8.



(a)

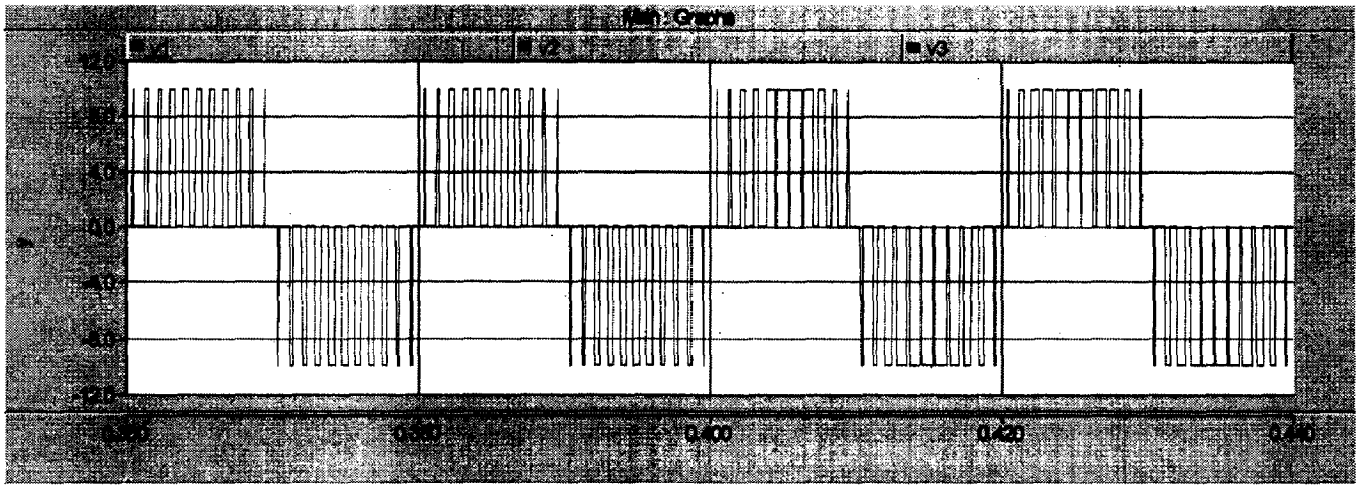


(b)

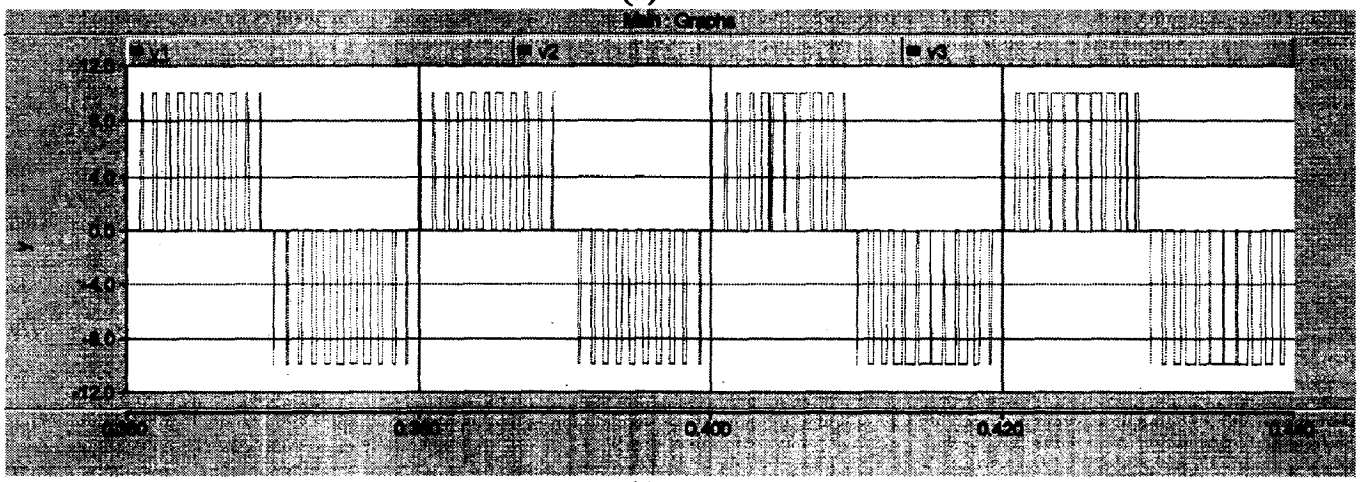


(c)

Figure 3.7 Output voltages of all the phases (a) a, (b) b, (c) c.



(a)



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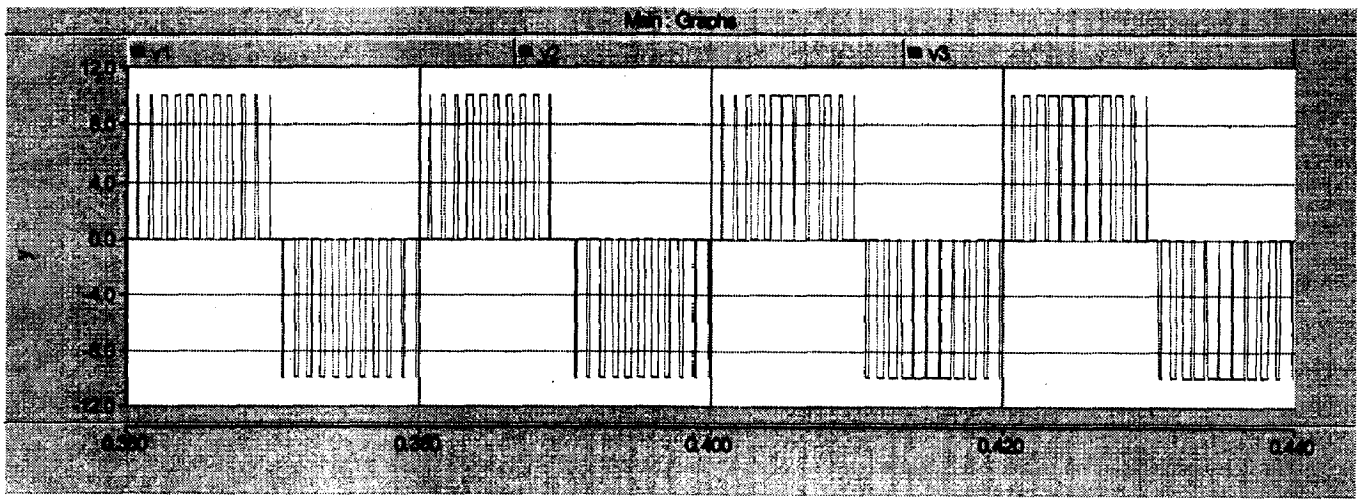


(c)

Figure 3.8: Output voltages of each individual modules of phase a (a) V1 (b) V2 (c) V3.

3.5 Control principles & Structure

The ability of the UPFC to rapidly inject an ac-compensating voltage phasor with variable magnitude and angle in series with the line when needed, bestow it with superior operating characteristics. When the UPFC is to be used in a transmission grid, proper control schemes of the shunt and the series inverters are needed.

3.5.1 Control of the Shunt Converter

The shunt converter draws a controlled current phasor from the line, the real part of which is determined by the real power requirement of the series converter while the reactive part can be set to any desired level within the converter's capability. This operating mode achieves automatic voltage control. Here, the shunt converter reactive current is automatically regulated to maintain the transmission line voltage at the point of connection. The control principle is as shown in Fig. 3.9.

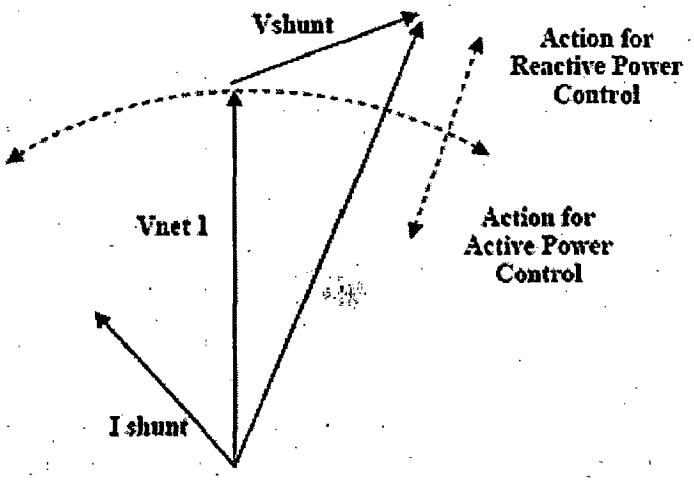


Figure 3.9: Principle of control of the shunt inverter of the UPFC.

In the control scheme for the shunt inverter, the magnitude of the output voltage is directly proportional to the dc voltage and only its angle is controllable. The outer voltage loop regulates the ac bus voltage and also controls the dc capacitor voltage. This outer

loop changes the phase angle of the inverter voltage with respect to the ac bus voltage until the dc capacitor voltage reached the value necessary to achieve the reactive compensation demanded. The block diagram of the control system used is as shown in Figure 3.10.

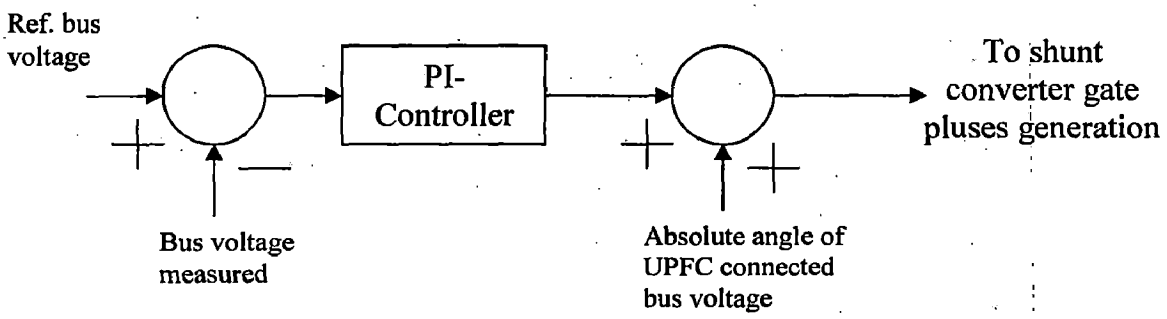


Figure 3.10: Block diagram of shunt inverter control.

3.5.2 Control of the Series Converter

The series converter provides control over the angle of the voltage phasor injected in series with the line. Depending on the operation mode of the UPFC, the voltage injected controls the power flow on the line. This converter has four operating modes, which are the direct voltage injection mode, the line impedance compensation mode, the phase angle shifter mode and the automatic power flow control mode which are already discussed in chapter 1.

When the UPFC is in the automatic power flow control mode, the magnitude and angle of the injected voltage phasor is controlled so as to adjust the line current to achieve the required real or reactive power flow. The control principle is as shown in Fig. 3.11.

Figure 3.12 shows a detail configuration of the UPFC controller used in the simulation, which is a control block diagram for the series inverter in automatic power flow control mode.

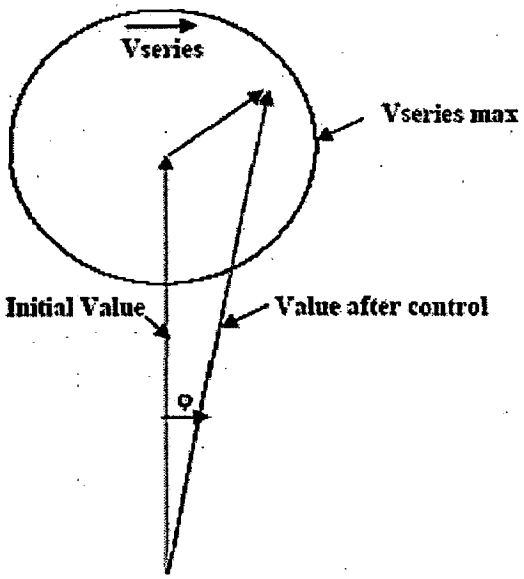


Figure 3.11: Principle of operation of the series part of the UPFC

The automatic power flow control is achieved by means of a vector control scheme that regulates the transmission line current using a synchronous frame, in which the control quantities appear as dc signals in the steady state. The appropriate reactive and real current components, I_q and I_p, are determined for a desired P_{Ref} and Q_{Ref}. These are compared with the measured line currents, I_q and I_p, and used to drive the magnitude and angle of the series inverter voltage, V_{pq} and δ, respectively.

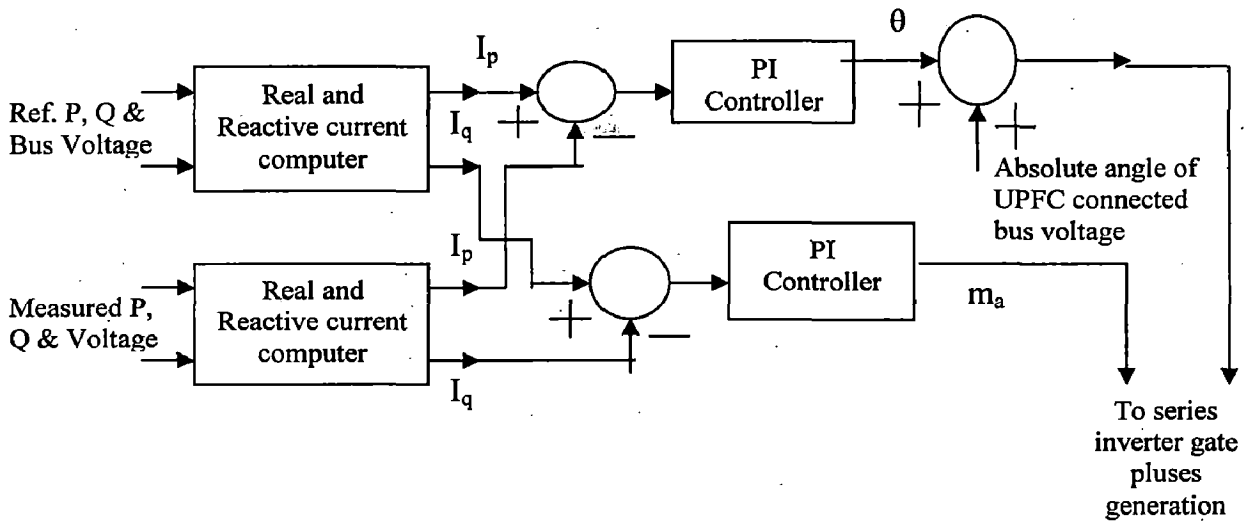


Figure 3.12: Block diagram of UPFC series converter control

3.6 Detailed Simulation studies and Results

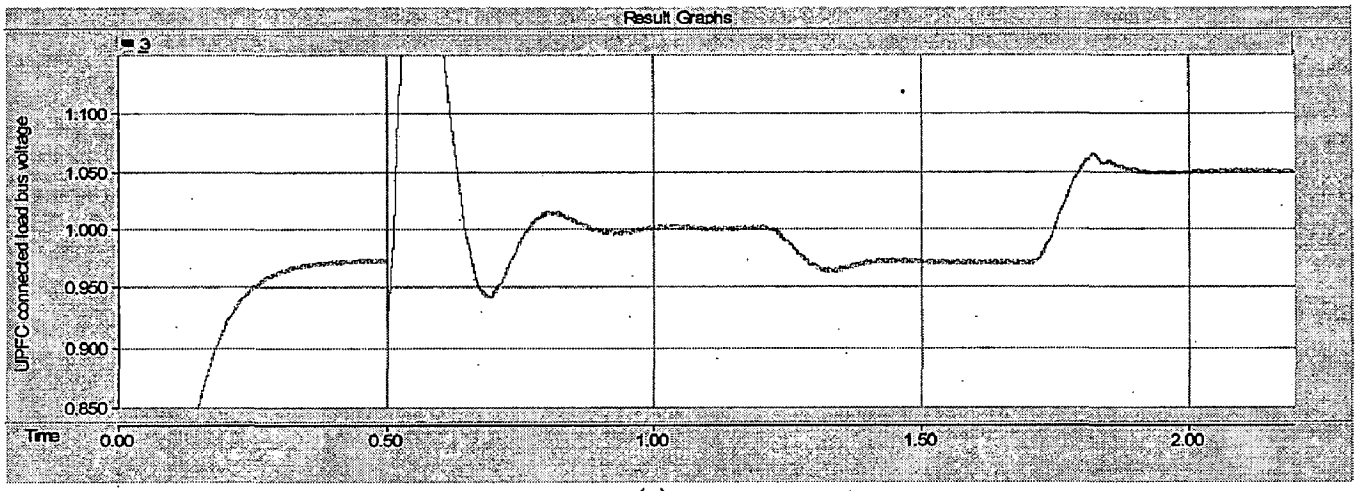
For simulation of this configuration of UPFC in a grid, the test system as described in chapter 1 has been chosen. The PSCAD/EMTDC graphical view is given in Appendix C. The various parameters of the control system and the other apparatus are also given in Appendix C.

3.6.1 Control of Bus voltage

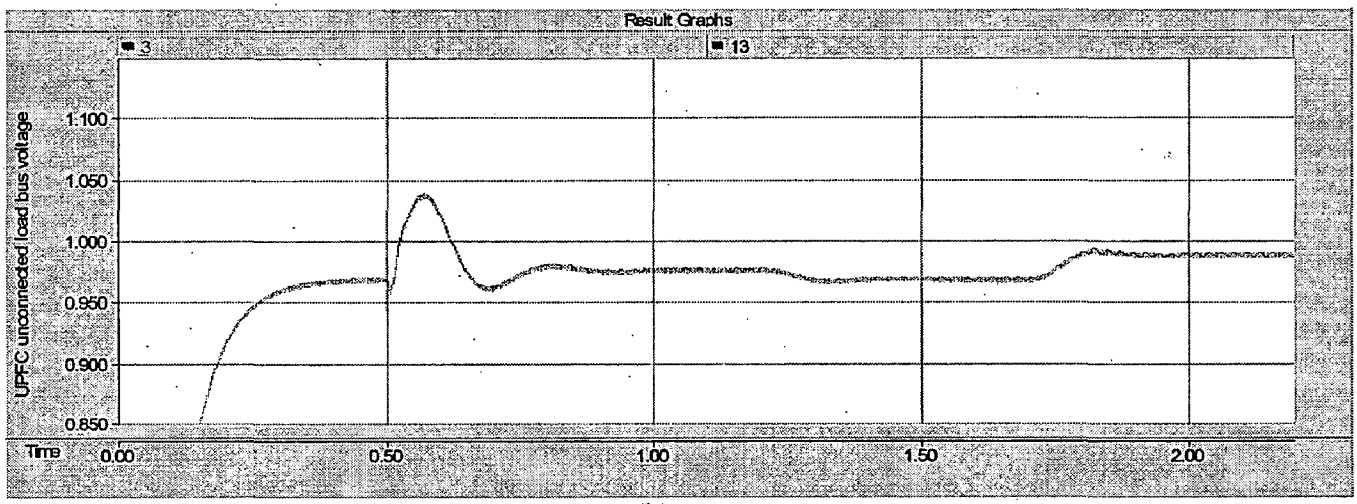
After designing this configuration of UPFC as described above briefly. First the system is run without connecting the UPFC. After reaching to the steady state the UPFC is being connected to the system at time t=0.5sec. Now, only the shunt part of the UPFC is switched on to prove that it can also control the bus voltage, where it is connected at the ref. set value. The various graphs showing the above mentioned result are as shown in Fig. 3.13 below. The corresponding simulation parameters are given in the Table 3.5.

Table 3.5: Simulation parameters for bus voltage control

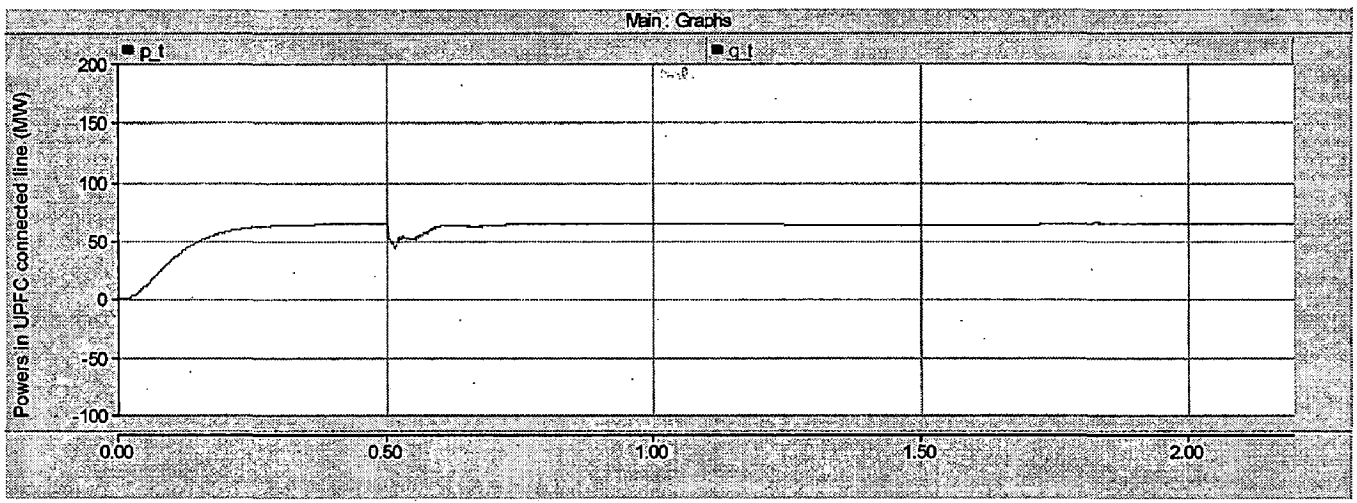
Time in seconds (from-to)	Ref. set voltage (pu)
0.5-1.2	1.0
1.2-1.7	0.97
1.7-2.5	1.05


Result Graphs
3
UPFC connected load bus voltage
1.100
1.050
1.000
0.950
0.900
0.850
Time
0.00
0.50
1.00
1.50
2.00

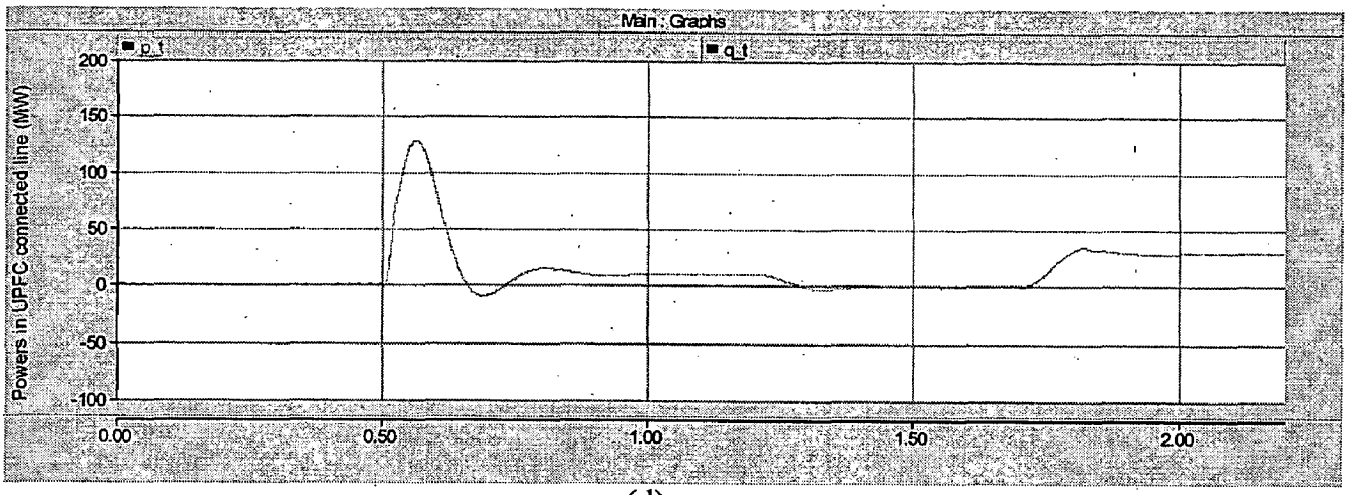
(a)


Result Graphs
3
13
UPFC unconnected load bus voltage
1.100
1.050
1.000
0.950
0.900
0.850
Time
0.00
0.50
1.00
1.50
2.00

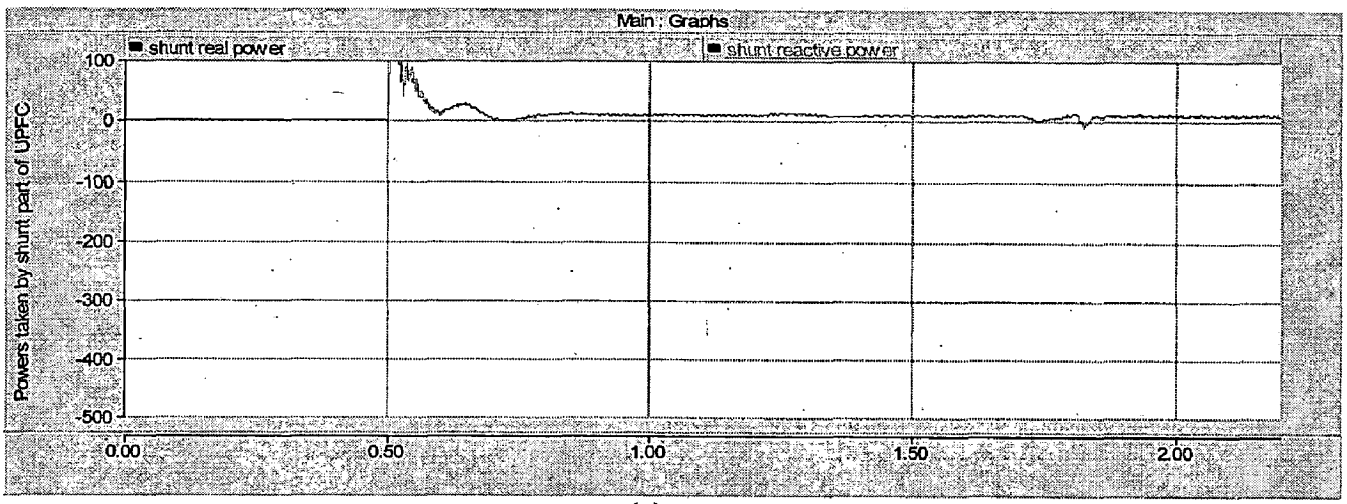
(b)


Main: Graphs
p_t
q_t
Powers in UPFC connected line (MW)
200
150
100
50
0
-50
-100
0.00
0.50
1.00
1.50
2.00

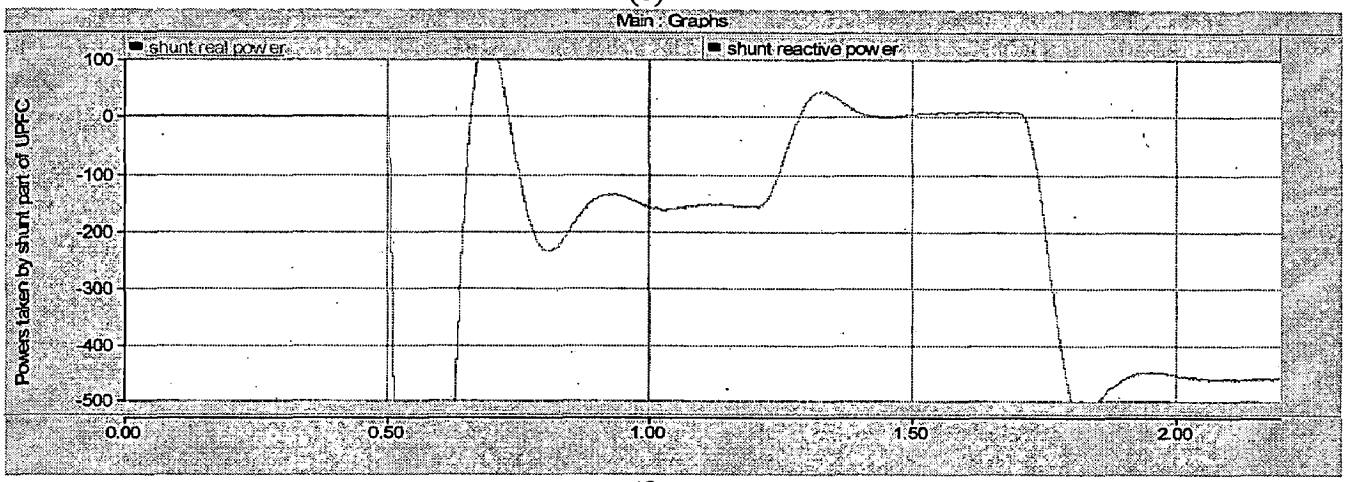
(c)


Main : Graphs
p_t
q_t
Powers in UPFC connected line (MW)
200
150
100
50
0
-50
-100
0.00
0.50
1.00
1.50
2.00

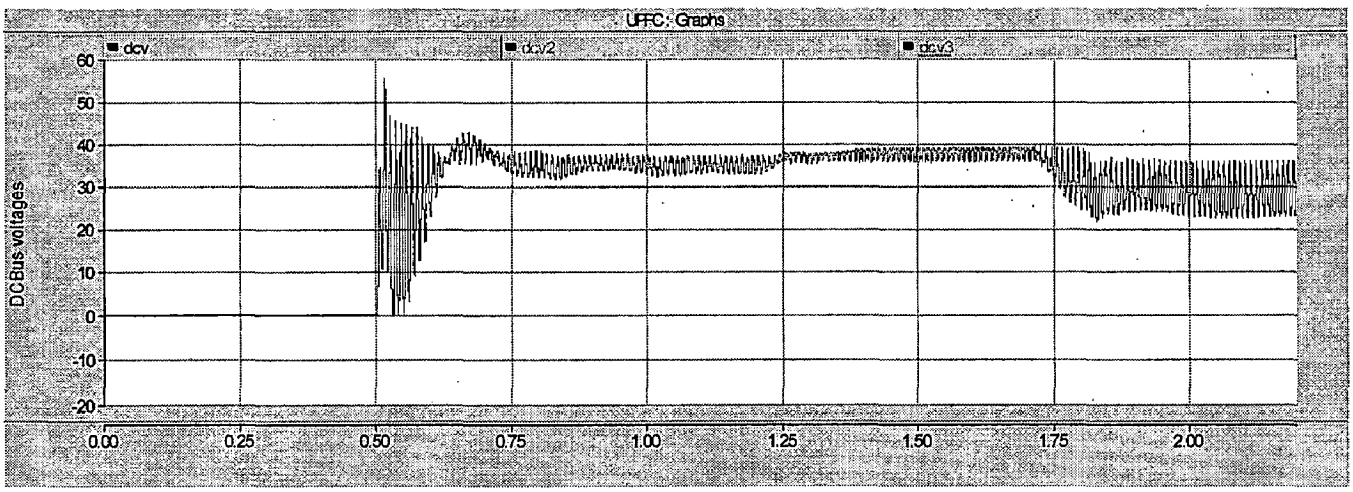
(d)


Main : Graphs
shunt real power
shunt reactive power
Powers taken by shunt part of UPFC
100
0
-100
-200
-300
-400
-500
0.00
0.50
1.00
1.50
2.00

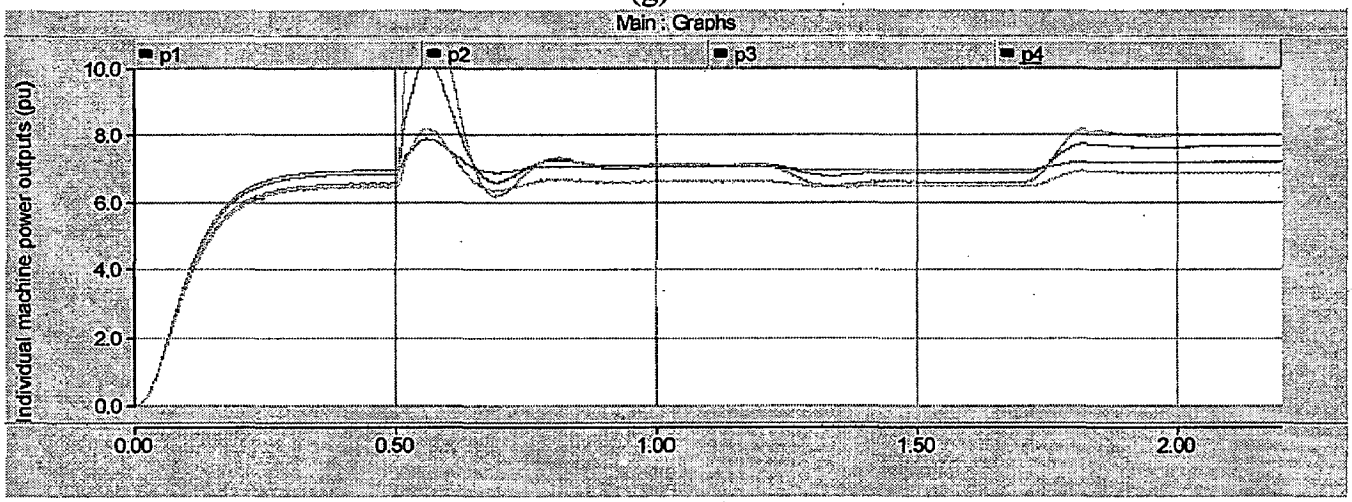
(e)


Main : Graphs
shunt real power
shunt reactive power
Powers taken by shunt part of UPFC
100
0
-100
-200
-300
-400
-500
0.00
0.50
1.00
1.50
2.00

(f)



(g)



(h)

Figure 3.13: Simulation results of UPFC as bus voltage control. (a) UPFC Connected Bus voltage, (b) UPFC Connected Bus voltage, (c) Real power in the UPFC connected line, (d) Reactive power in the UPFC connected line (e) Real power taken by shunt part of the UPFC, (f) Reactive power taken by shunt part of the UPFC (g) DC Bus voltages & (h) Individual m/c output powers.

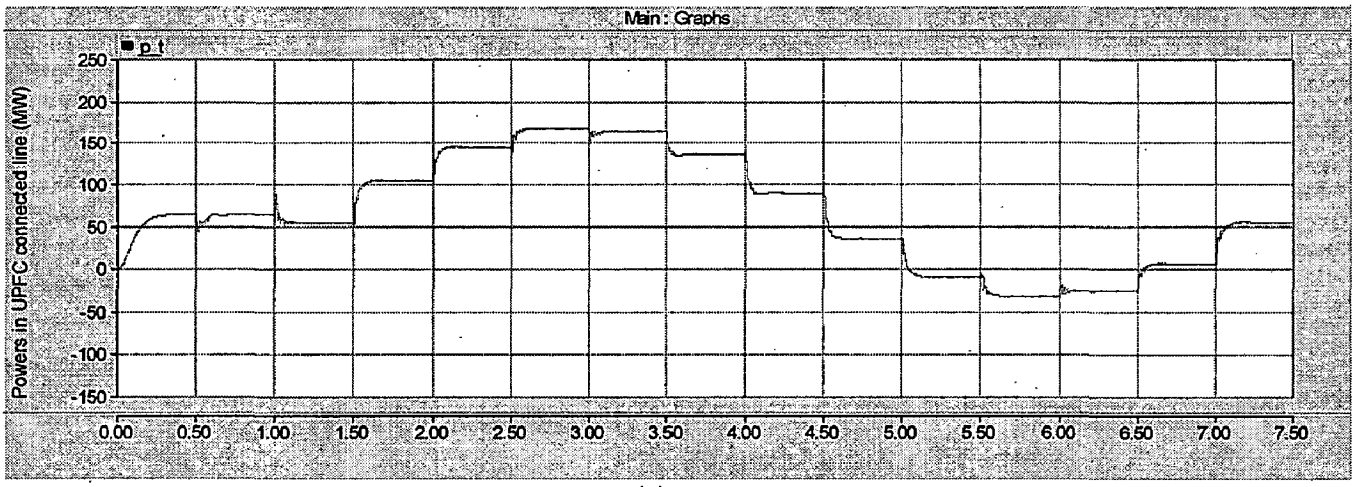
3.6.2 UPFC as controlling the powers in open loop

Now, the system is run without connecting the UPFC. After reaching to the steady state the UPFC is being connected to the system at time t=0.5sec. Now, both the shunt and series inverters of the UPFC are switched on at the same time, and then changed the

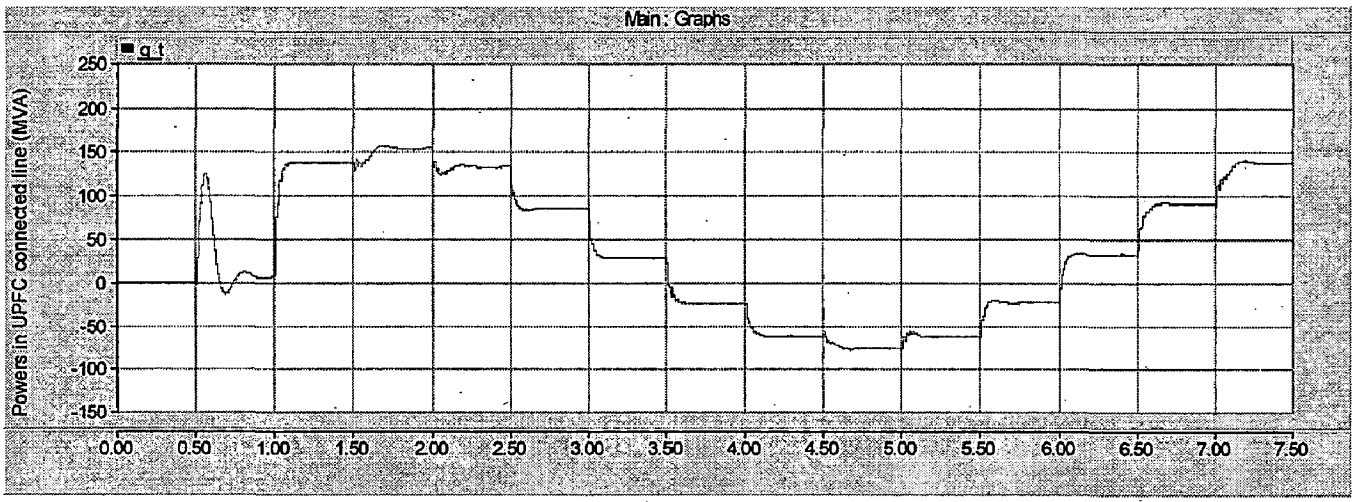
parameters of the series inverter i.e. m_a & phase angle. The various graphs result is as shown in Fig. 3.14 below. The corresponding simulation parameters are given in the Table 3.6.

Table 3.6: Simulation parameters for UPFC in open loop control

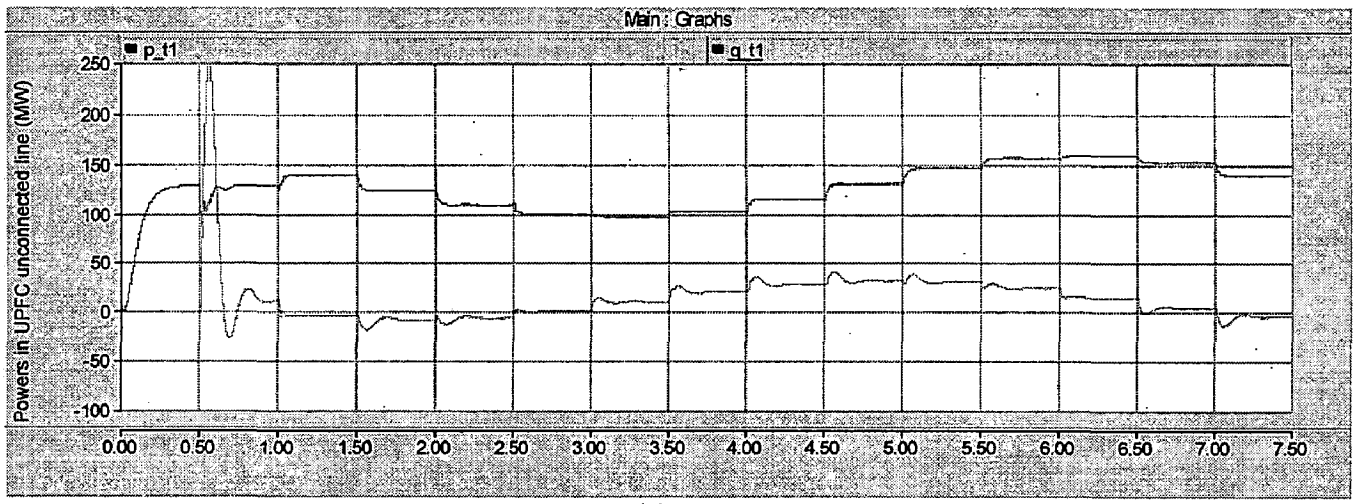
Time (sec.) From-to	Ma	Phase (degrees)	$V_{ref.}$ (pu)
0.5-1.0	0	0	0.99
1.0-1.5	0.9	0	0.99
1.5-2.0	0.9	30	0.99
2.0-2.5	0.9	60	0.99
2.5-3.0	0.9	90	0.99
3.0-3.5	0.9	120	0.99
3.5-4.0	0.9	150	0.99
4.0-4.5	0.9	180	0.99
4.5-5.0	0.9	210	0.99
5.0-5.5	0.9	240	0.99
5.5-6.0	0.9	270	0.99
6.0-6.5	0.9	300	0.99
6.5-7.0	0.9	330	0.99
7.0-7.5	0.9	360	0.99


Main : Graphs
p_t
Powers in UPFC connected line (MW)
250
200
150
100
50
0
-50
-100
-150
0.00
0.50
1.00
1.50
2.00
2.50
3.00
3.50
4.00
4.50
5.00
5.50
6.00
6.50
7.00
7.50

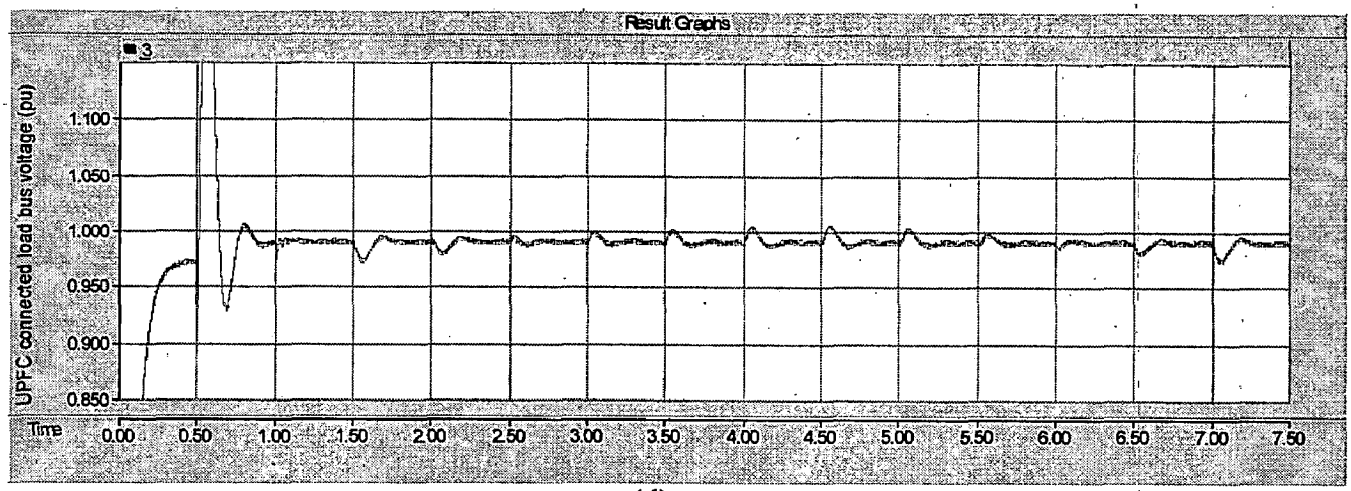
(a)


Main : Graphs
q_t
Powers in UPFC connected line (MVA)
250
200
150
100
50
0
-50
-100
-150
0.00
0.50
1.00
1.50
2.00
2.50
3.00
3.50
4.00
4.50
5.00
5.50
6.00
6.50
7.00
7.50

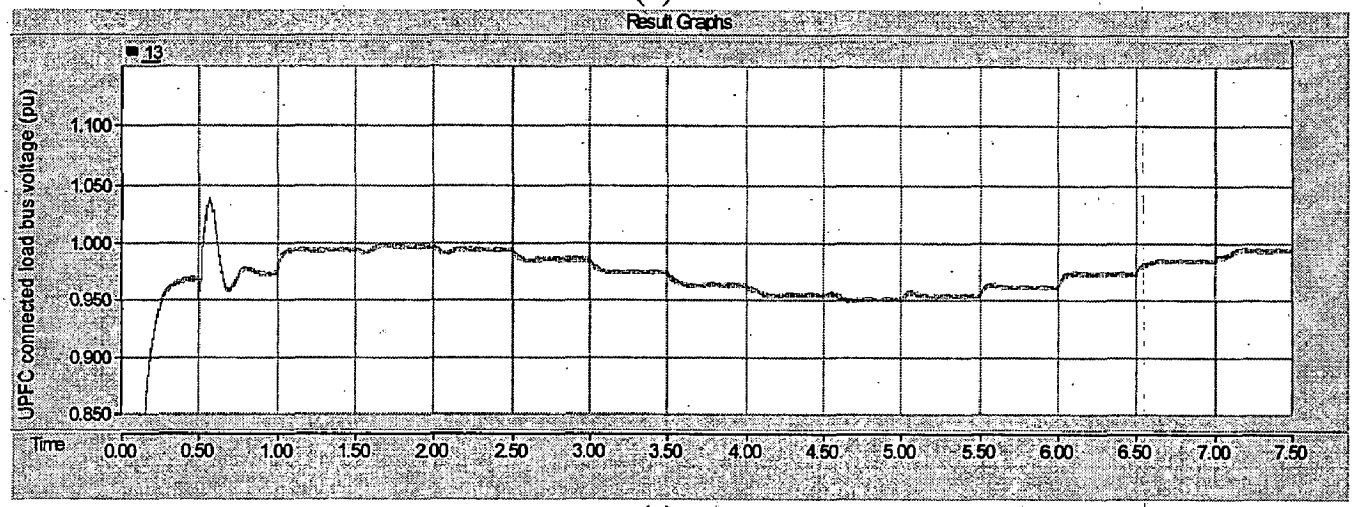
(b)


Main : Graphs
p_t1
q_t1
Powers in UPFC unconnected line (MW)
250
200
150
100
50
0
-50
-100
0.00
0.50
1.00
1.50
2.00
2.50
3.00
3.50
4.00
4.50
5.00
5.50
6.00
6.50
7.00
7.50

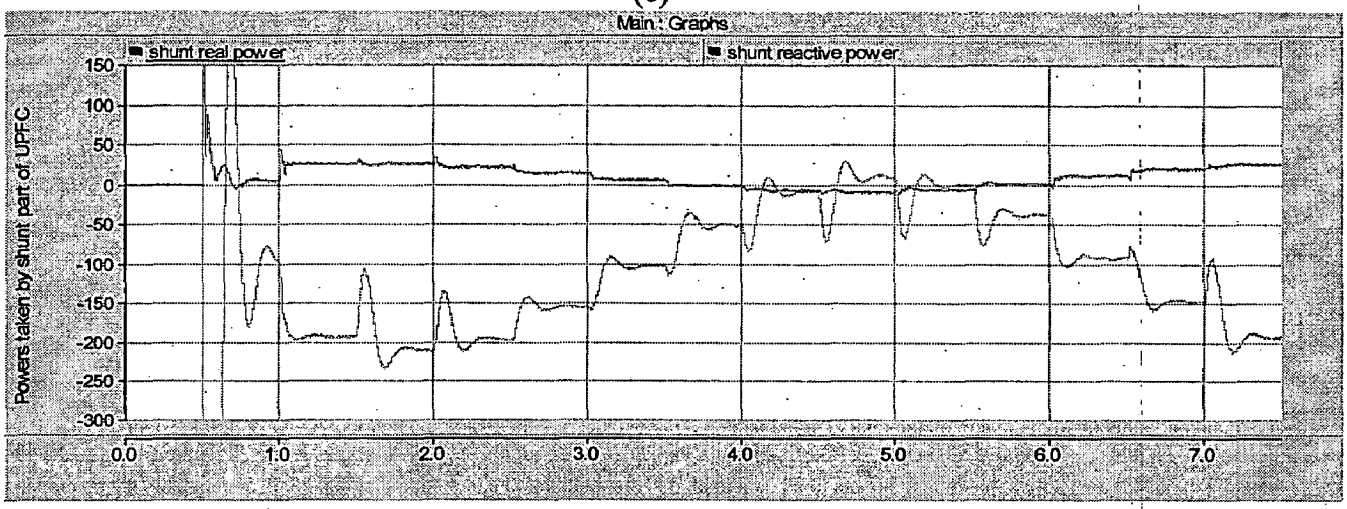
(c)


Result Graphs
3
UPFC connected load bus voltage (pu)
1.100
1.050
1.000
0.950
0.900
0.850
Time
0.00 0.50 1.00 1.50 2.00 2.50 3.00 3.50 4.00 4.50 5.00 5.50 6.00 6.50 7.00 7.50

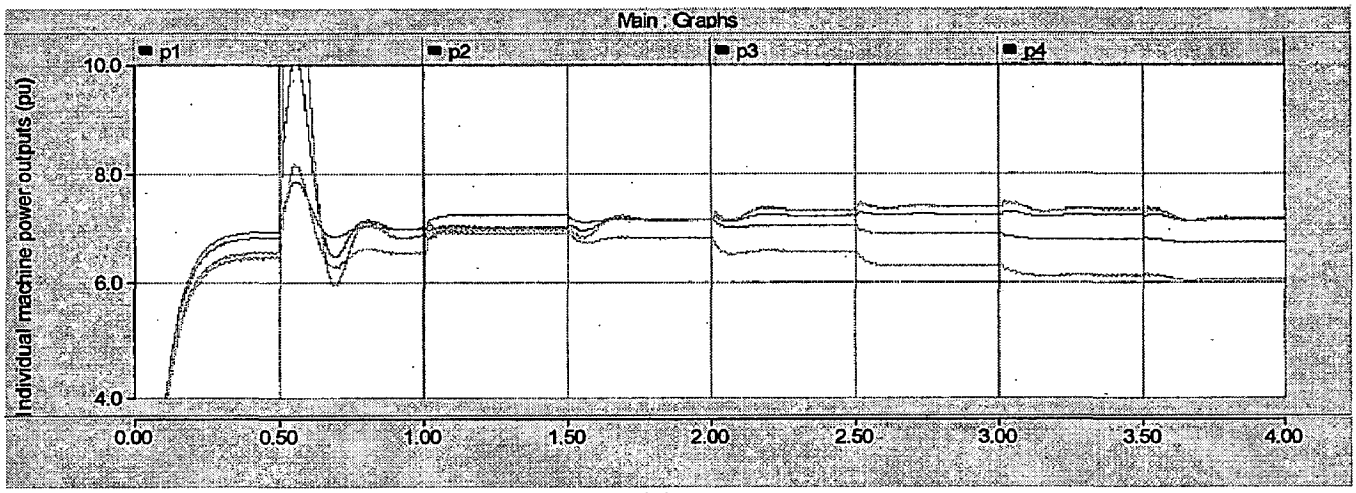
(d)


Result Graphs
13
UPFC connected load bus voltage (pu)
1.100
1.050
1.000
0.950
0.900
0.850
Time
0.00 0.50 1.00 1.50 2.00 2.50 3.00 3.50 4.00 4.50 5.00 5.50 6.00 6.50 7.00 7.50

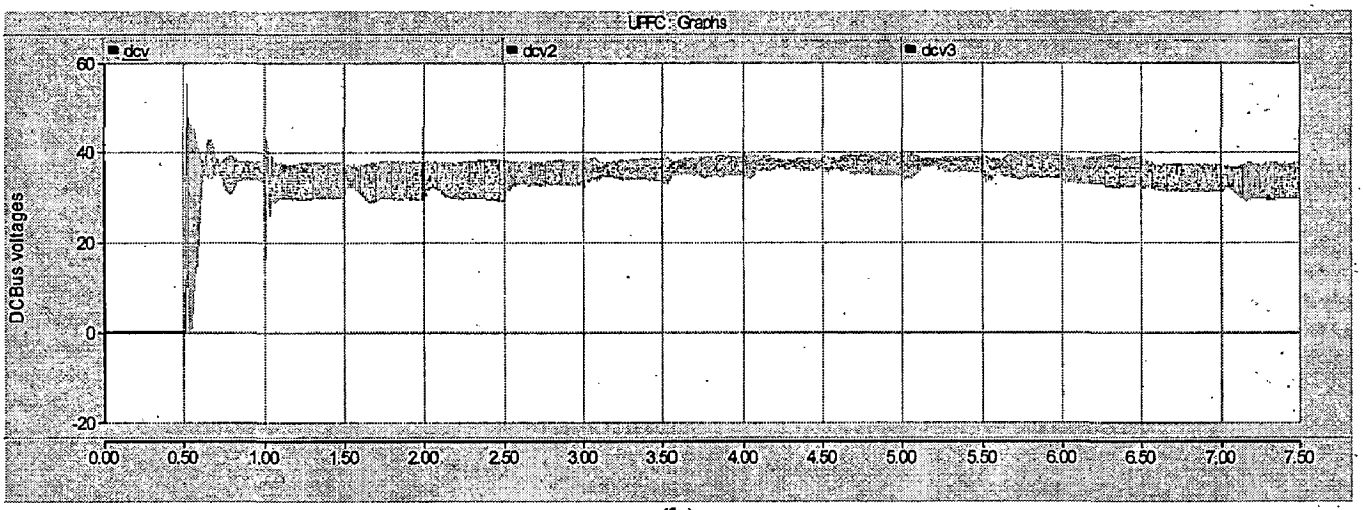
(e)


Main : Graphs
shunt real power
shunt reactive power
Powers taken by shunt part of UPFC
150
100
50
0
-50
-100
-150
-200
-250
-300
0.0 1.0 2.0 3.0 4.0 5.0 6.0 7.0

(f)



(g)



(h)

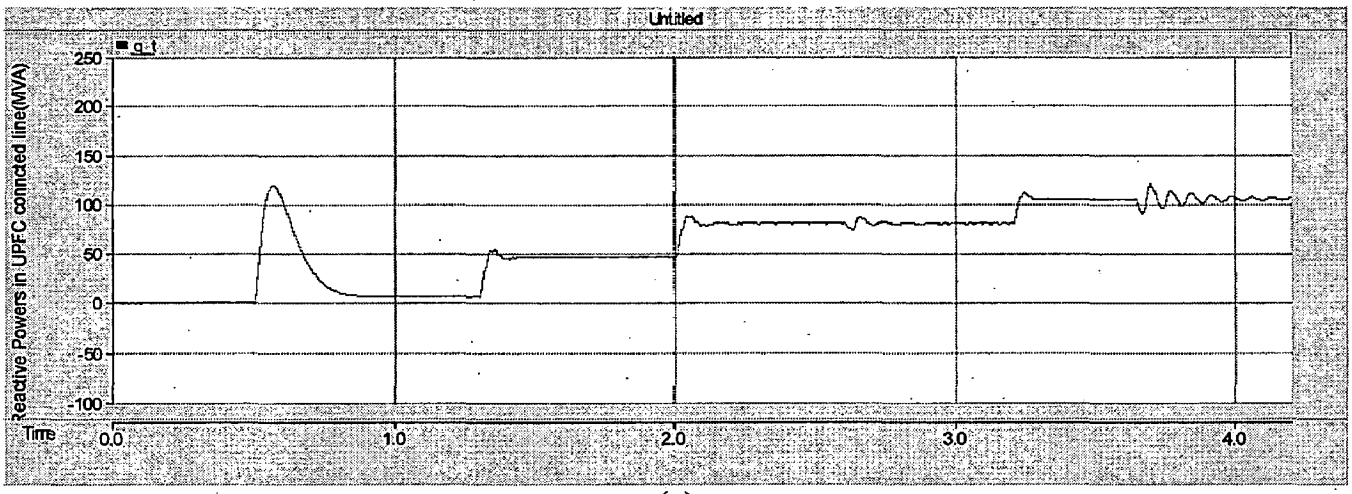
Figure 3.14: Simulation results of UPFC in open-loop control. (a) Real power in the UPFC connected line, (b) Real & Reactive powers in the UPFC connected line, (c) Real & Reactive powers in the UPFC un-connected line, (d) UPFC Connected Bus voltage, (e) UPFC Un-connected Bus voltage (f) Real & Reactive powers taken by shunt part of the UPFC, (f) Individual machine output powers, (g) DC Bus voltages.

3.6.3 UPFC as controlling the powers in closed loop

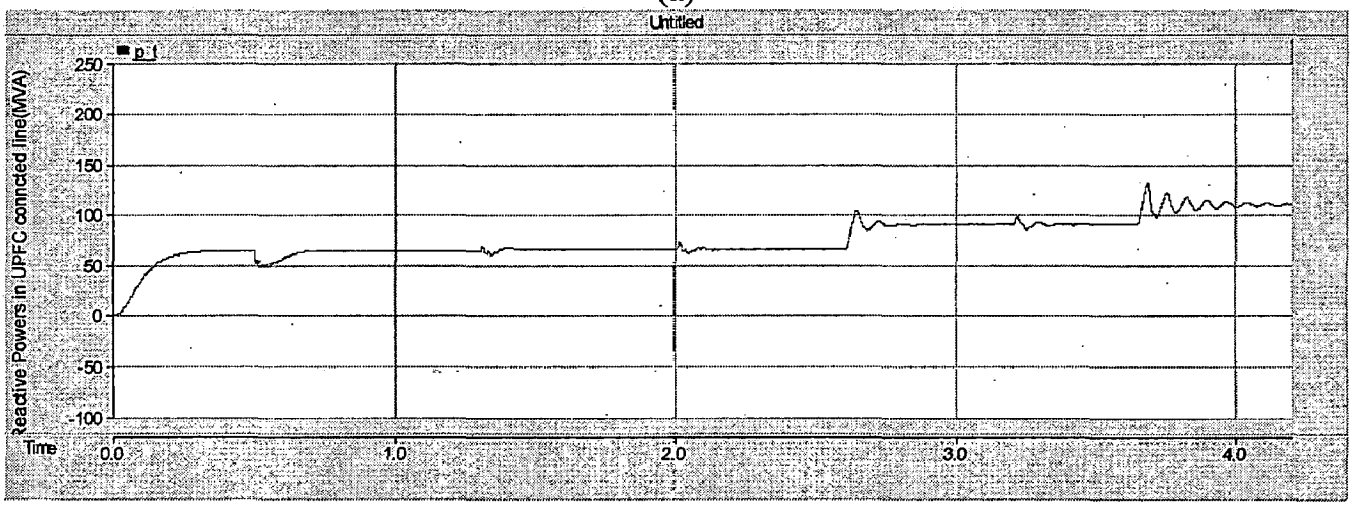
For simulating the performance of UPFC in closed loop control, the block diagram of the control system shown in Fig. 3.15 is used. The automatic power flow control is achieved by means of a vector control scheme that regulates the transmission line current using a synchronous frame, in which the control quantities appear as dc signals in the steady state. Here also, the system is run without connecting the UPFC for reaching the steady state. After reaching to the steady state the UPFC is being connected to the system at time t=0.5sec with P & Q ref. values set at the initial values only to have to zero output voltage from the series inverter, so that reducing the transient effects. Now, both the shunt and series inverters of the UPFC are switched on at the same time. And then changed the P & Q ref. values, and observed that both the real and reactive powers are tracking the corresponding ref. set values with in least min. time. The various graphs result is as shown in Figure 3.15 below. The corresponding simulation parameters are given in the Table 3.7.

Table 3.7: Simulation parameters for UPFC in closed loop control.

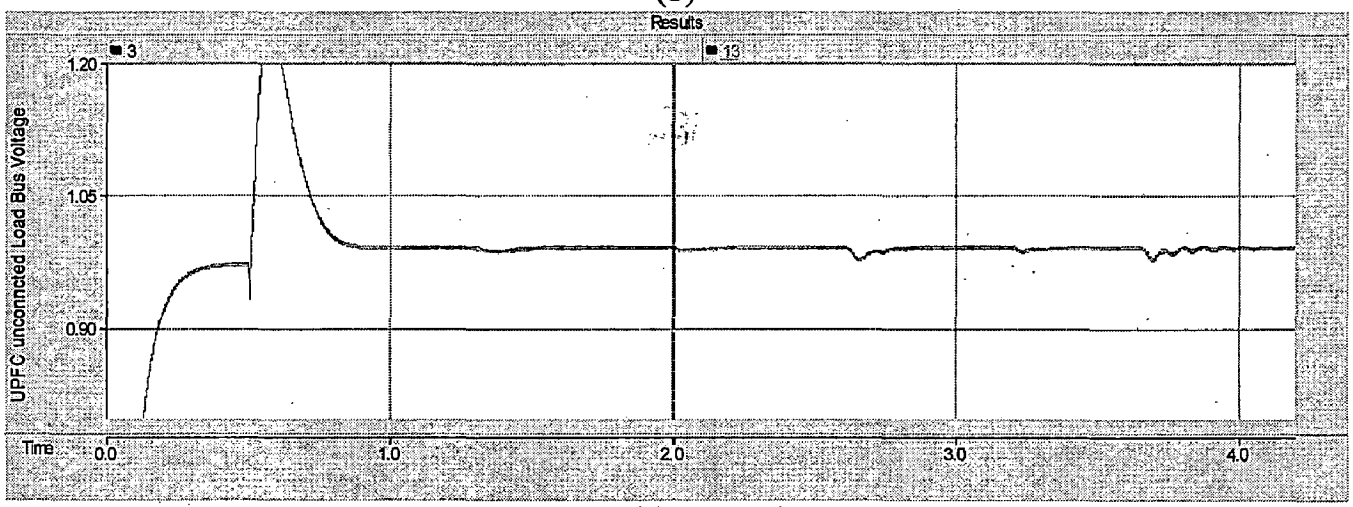
Time (sec.) From-to	$V_{ref.}$ (pu)	$P_{ref.}$ (MW)	$Q_{ref.}$ (MVAR)
1.-1.2	0.99	65	5
1.2-2.0	0.99	65	45
2.0-2.6	0.99	65	80
2.6-3.2	0.99	90	80
3.2-3.65	0.99	90	105
3.65-4.2	0.99	115	100


Untitled
q: 1
Reactive Powers in UPFC conncted line(MVA)
250
200
150
100
50
0
-50
-100
Time
0.0
1.0
2.0
3.0
4.0

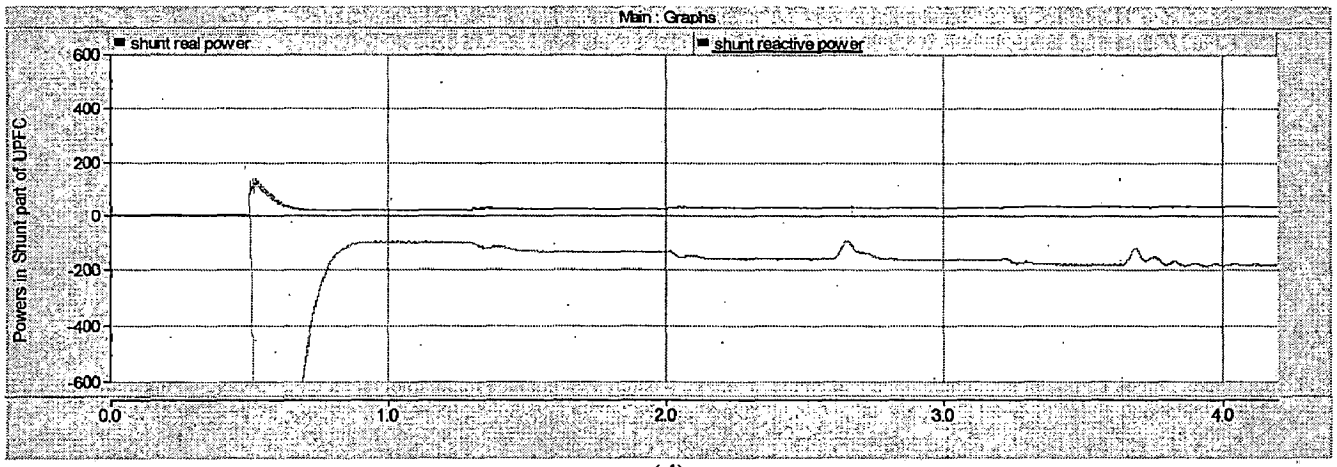
(a)


Untitled
p: 1
Reactive Powers in UPFC conncted line(MVA)
250
200
150
100
50
0
-50
-100
Time
0.0
1.0
2.0
3.0
4.0

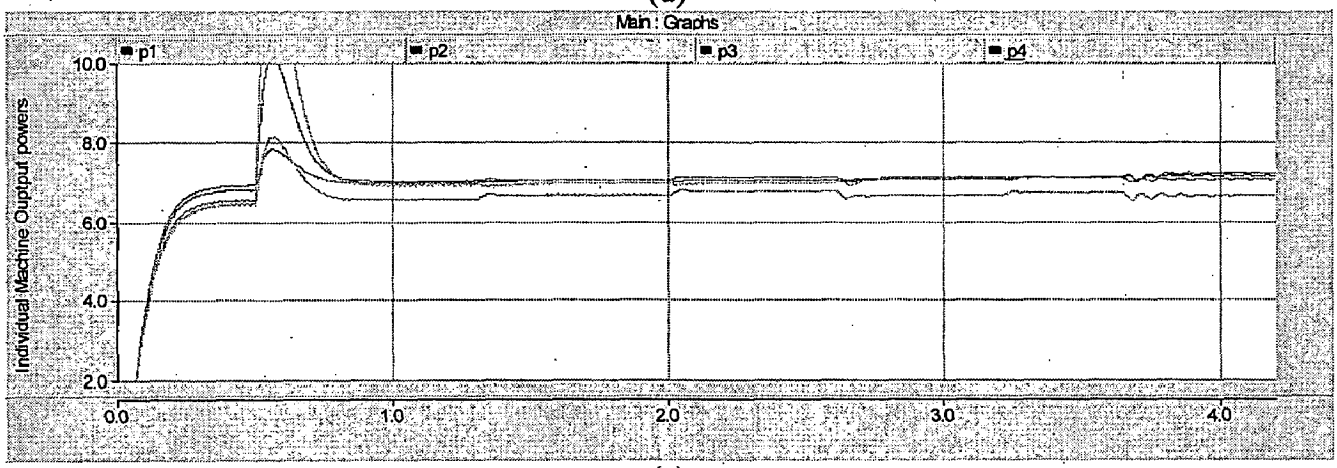
(b)


Results
3
13
UPFC unconncted Load Bus Voltage
1.20
1.05
0.90
Time
0.0
1.0
2.0
3.0
4.0

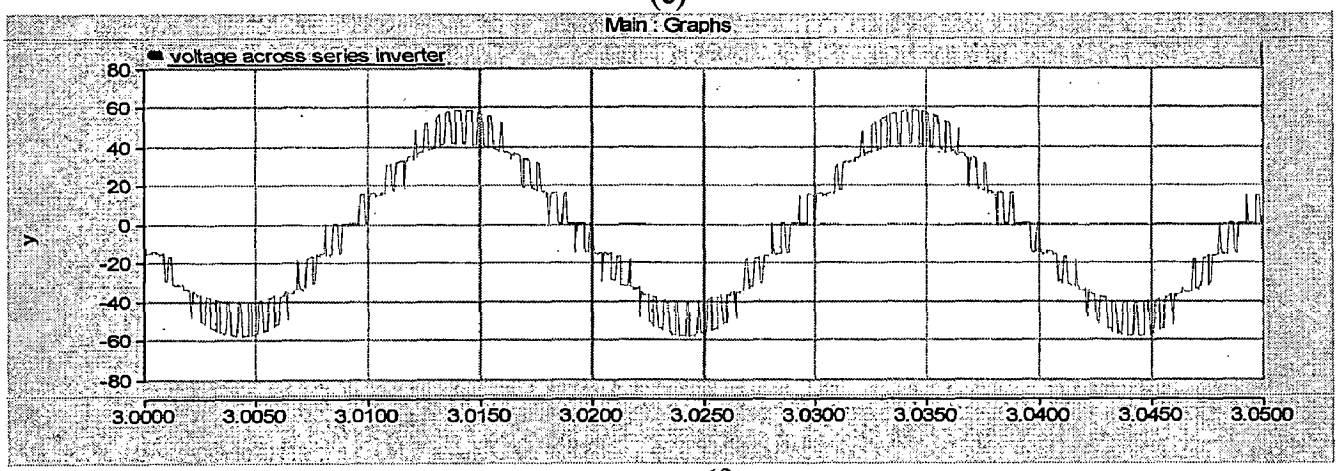
(c)



(d)



(e)



(f)

Figure 3.15: Simulation results of UPFC in closed-loop control. (a) Real power in the UPFC connected line, (b) Reactive power in the UPFC connected line, (c) UPFC Connected Bus voltage, (d) Real & Reactive powers in the UPFC un-connected line, (e) Individual machine output powers (f) series inverter voltage wave form.

3.7 conclusions

In this chapter, the operation of UPFC based on 3 level half bridge Diode clamped multi level inverter is described. The simulation results for the stand alone mode of the inverter have been presented. Also automatic power flow control schemes of the UPFC for controlling the real and reactive power flow over the transmission grid have also been developed. The detailed simulation results are also presented here.

CHAPTER: 4

H-Bridge inverter module based UPFC.

4.1 Introduction

UPFC, based on GTO voltage source converters, was proposed as the most promising FACTS controller to improve the dynamic performance of power transmission system. The presently developed UPFC operates in a dc link voltage much lower than the operation voltage of power transmission system. The reason for low dc link voltage is limitation on the maximum sustain voltage of high-power semiconductor switches. The maximum sustain voltage of commercially available GTO is about 6000V. In order to increase the dc link voltage of UPFC, series connection of GTOs is used. However, still there is limitation in the maximum allowable number of units. Multi-level converter was proposed to increase the system operation voltage avoiding series connection of switching devices. But the multi-level converter has complexity in forming the output voltage and requires many back-connection diodes.

In order to improve this weak point, a multi-bridge converter composed of several H-bridge modules in cascaded connection was proposed in reference. This system can operate without series injection transformers and has flexibility in expanding the operation voltage by means of adding the number of modules. This chapter describes the operation of a UPFC based on H-bridge modules, isolated through single-phase multi-winding transformers. The operation of the proposed system was verified through simulations with PSCAD/EMTDC as said earlier. This system can be directly connected to the transmission line without series injection transformers.

4.2 Basic Operating principle of cascaded H-Bridge MLI

The cascaded H-bridges multilevel inverter is a relatively new inverter structure a cascaded H-bridges multilevel inverter is simply a series connection of multiple H-bridge inverters [7]. Each H-bridge inverter has the same configuration as a typical single-phase

full-bridge inverter.The cascaded H-bridges multilevel inverter consists of (m–1)/2 or h number of single-phase H-bridge inverters. Fig 4.1 provides an illustration of a single phase cascaded H-bridge multilevel inverter. The output of inverter is given by,

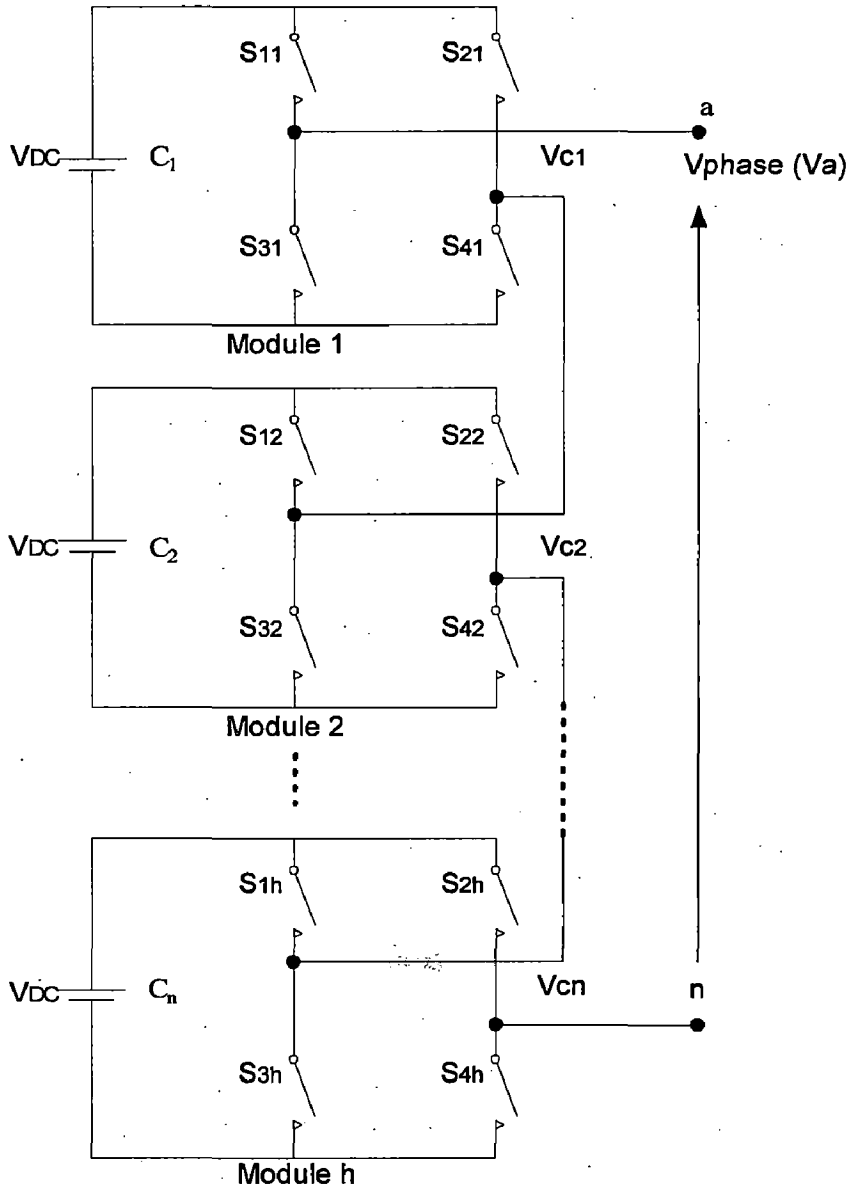


Figure 4.1: Single phase m-level structure of cascaded H-bridge inverter

$V_{an} = V_1 + V_2 + \ldots\ldots V_{(m-1)/2}$,

Where..... V_1: output voltage of module 1

V_2: output voltage of module 2

$V_{(m-1)/2}$: output voltage of module (m-1)/2

The cascaded H-bridges multilevel inverter uses separate dc sources to produce an ac voltage waveform. Each H-bridge inverter is connected to its own dc source V_{dc}. By cascading the ac outputs of each H-bridge inverter, an ac voltage waveform is produced.

Fig 4.2 also illustrates the idea of "levels" in a cascaded H-bridges multilevel inverter. In the figure, one notices that five distinct dc sources can produce a maximum of 11 distinct levels in the output phase voltage of the multilevel inverter.

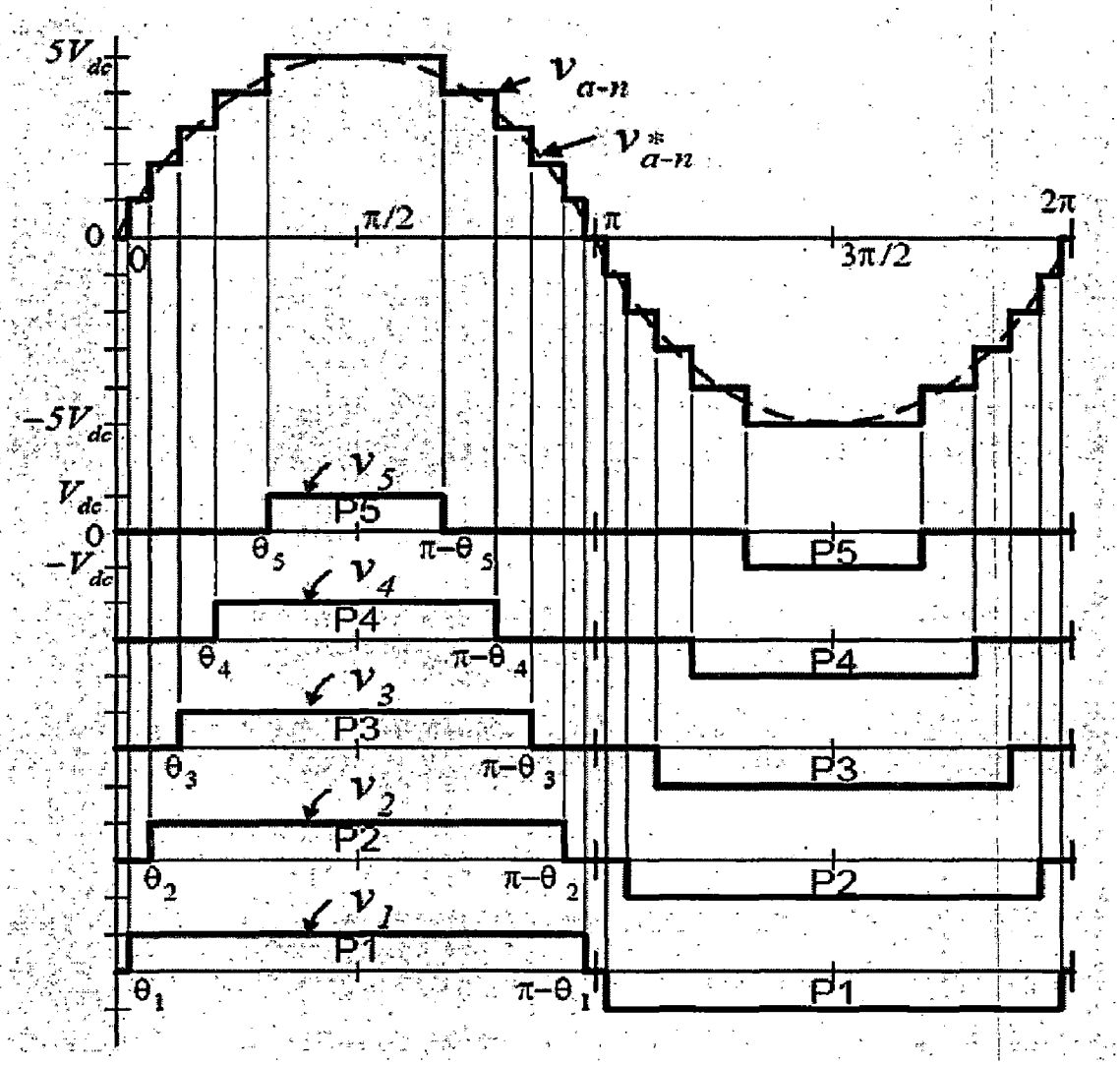


Figure 4.2: Typical 11 level line to neutral voltage wave form.

More generally, a cascaded H-bridges multilevel inverter using s separate dc sources can produce a maximum of $2s + 1$ distinct levels in the output phase voltage.Power devices switching states of a 5-level H-bridge inverter are [7, 9]. Switching states for two series cells is given in the following Table 4.1.

Table 4.1: Switching states for two series cells of 5-level inverter.

Power devices index								Output voltages		
S_{11}	S_{21}	S_{31}	S_{41}	S_{12}	S_{22}	S_{32}	S_{42}	V_{c1}	V_{c2}	V_a
1	0	0	1	1	0	0	1	$+V_{DC}$	$+V_{DC}$	$+2V_{DC}$
1	0	0	1	1	1	0	0	$+V_{DC}$	0	$+V_{DC}$
1	0	0	1	0	0	1	0	$+V_{DC}$	0	$+V_{DC}$
1	0	0	1	0	1	1	0	$+V_{DC}$	$-V_{DC}$	0
1	1	0	0	1	0	0	1	0	$+V_{DC}$	$+V_{DC}$
1	1	0	0	1	1	0	0	0	0	0
1	1	0	0	0	0	1	0	0	0	0
1	1	0	0	0	1	1	0	0	$-V_{DC}$	$-V_{DC}$
0	0	1	1	1	0	0	1	0	$+V_{DC}$	$+V_{DC}$
0	0	1	1	1	1	0	0	0	0	0
0	0	1	1	0	0	1	0	0	0	0
0	0	1	1	0	1	1	0	0	$-V_{DC}$	$-V_{DC}$
0	1	1	0	1	0	0	1	$-V_{DC}$	$+V_{DC}$	0
0	1	1	0	1	1	0	0	$-V_{DC}$	0	$-V_{DC}$
0	1	1	0	0	0	1	0	$-V_{DC}$	0	$-V_{DC}$
0	1	1	0	0	1	1	0	$-V_{DC}$	$-V_{DC}$	$-2V_{DC}$

Some of the advantages and disadvantages of cascaded H-bridges multilevel inverters are the following:

4.2.1 Advantages [11]:

1. To achieve the same number of voltage levels, this type of inverter requires the least number of components

2. Unlike diode-clamped and flying-capacitor multilevel inverters, no extra clamping diodes or voltage balancing capacitors are needed.

3. Since each H-bridge has the same structure, modularized circuit layout and packaging are possible.

4. Since the total output phase voltage is a summation of voltages produced by each H-bridge inverter, switching redundancies exist.

5. Smaller dc sources are usually involved, resulting in fewer safety issues.

4.2.2 Disadvantages [11]:

1. Separate dc sources are required, resulting in limited applicability.

2. For a three-phase system, this type of inverter will require more switches than a more traditional inverter.

Comparison of power component requirements per phase leg among three multilevel inverters is given in above.

4.3 Structure of UPFC

In Fig 4.3, typical configuration of one phase leg of UPFC based on H-bridge modules is shown. As shown in, any phase of the UPFC consists of the several pairs of H-bridge modules. Each pair has two H-bridge modules connected in parallel through a common dc link capacitor.

The H-bridge module in shunt part is connected through single-phase multi-winding transformer for isolation, while the H-bridge module in series part is directly inserted in the transmission line.

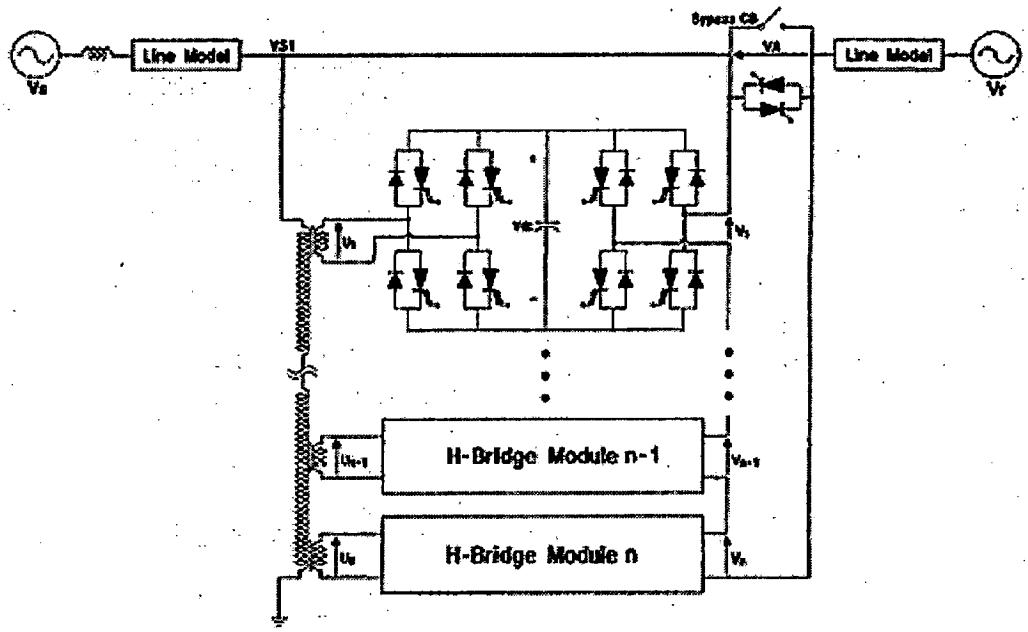


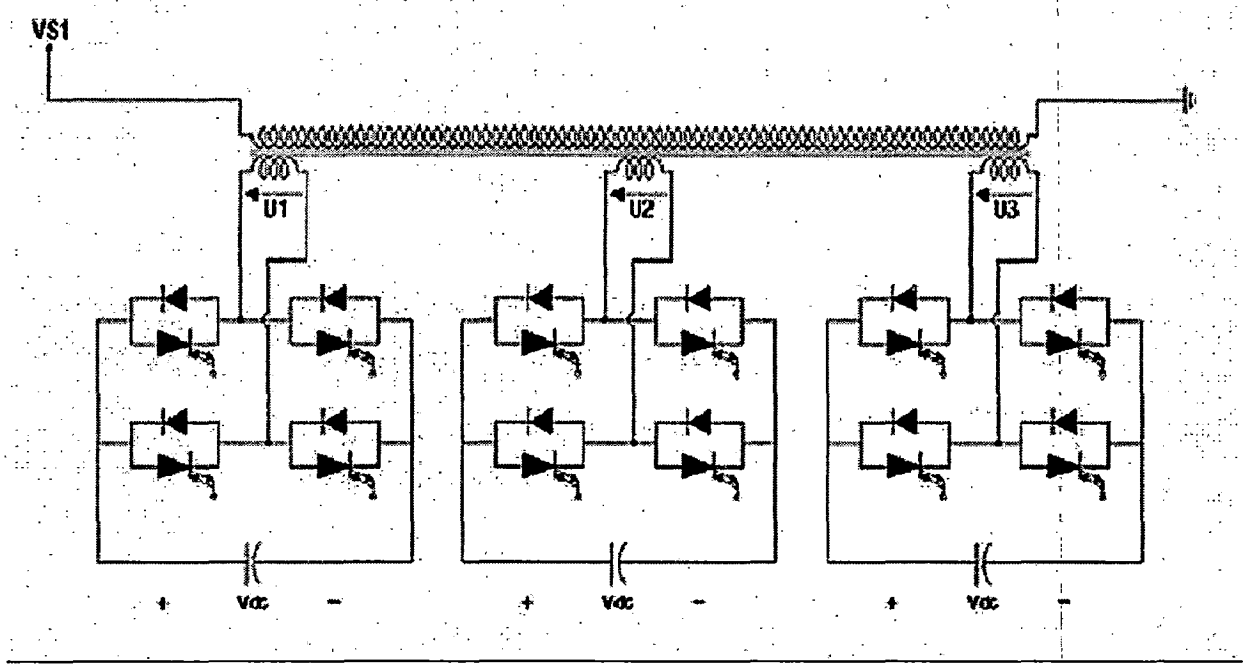
Figure 4.3: Configuration of UPFC based on H-bridge modules

The whole converter, its shunt part as well as its series part, must be insulated to the full insulation level of 230 kV line-to-line voltages. This UPFC has bypass functions to remove the series converter from service during system faults. The bypass function is implemented by the operation of thyristor bypass switch and mechanical circuit breaker as shown in figure. The line over-current can be bypassed first by the thyristor bypass switch and then by the mechanical circuit breaker. However, when the maximum fault current is lower than the maxi-mum current rating of series converter switches, it is possible to attempt a bypass scheme using the converter control, instead of adding separate thyristor bypass switch. This series converter has two possible bypassing ways by making a short circuit at the ac terminal. One is to turn on all the upper two switches in series part simultaneously and another is to turn on all the lower two switches in the series part simultaneously.

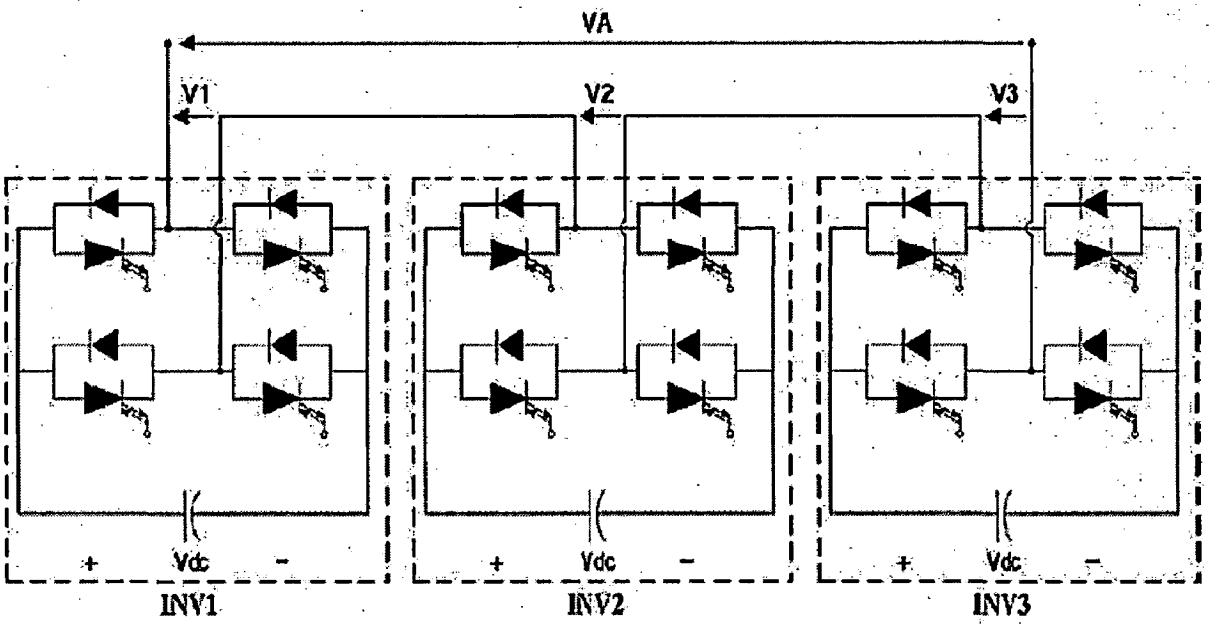
Table 4.2: Switching pattern of one H-bridge module.

V1A	Switching state	Mode
V_{dc}	S_1, S_4: on and S_2, S_3: off	M1
0	S_1, S_3: on and S_2, S_4 off S_2, S_4: on and S_1, S_3: off	M2
$-V_{dc}$	S_2, S_3: on and S_1, S_4: off	M3

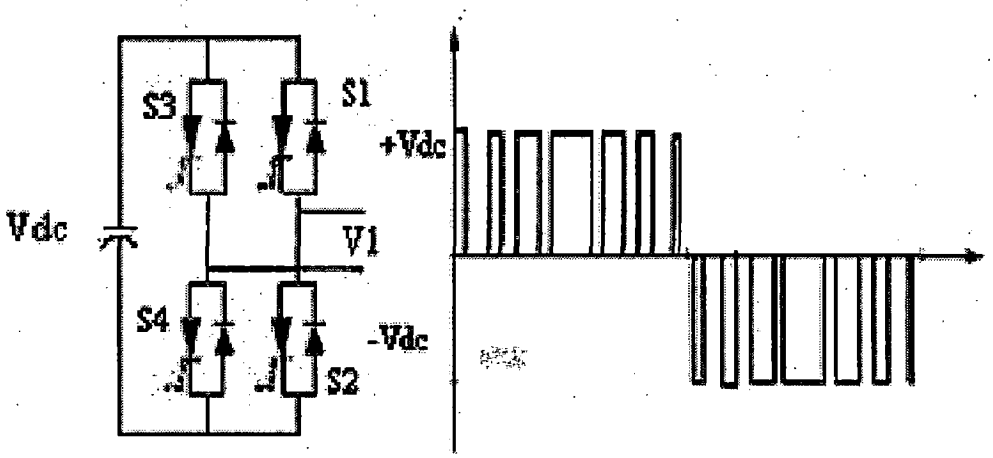
Fig. 4.4 shows the converter structure and the switching pattern for the proposed UPFC. For the purpose of simulation convenience, the shunt and series parts are assumed to be composed of three H-bridge modules for each phase as shown in Fig. 4.4(a) and (b). The output voltage of one module and switching states can be explained using Figure 4.4 (c) and Table 4.2. The output of each module has three states $+V_{dc}$, 0, $-V_{dc}$ depending on states of switch S_1–S_4. By changing the modulation index, the output voltage can be adjusted.



(a)



(b)



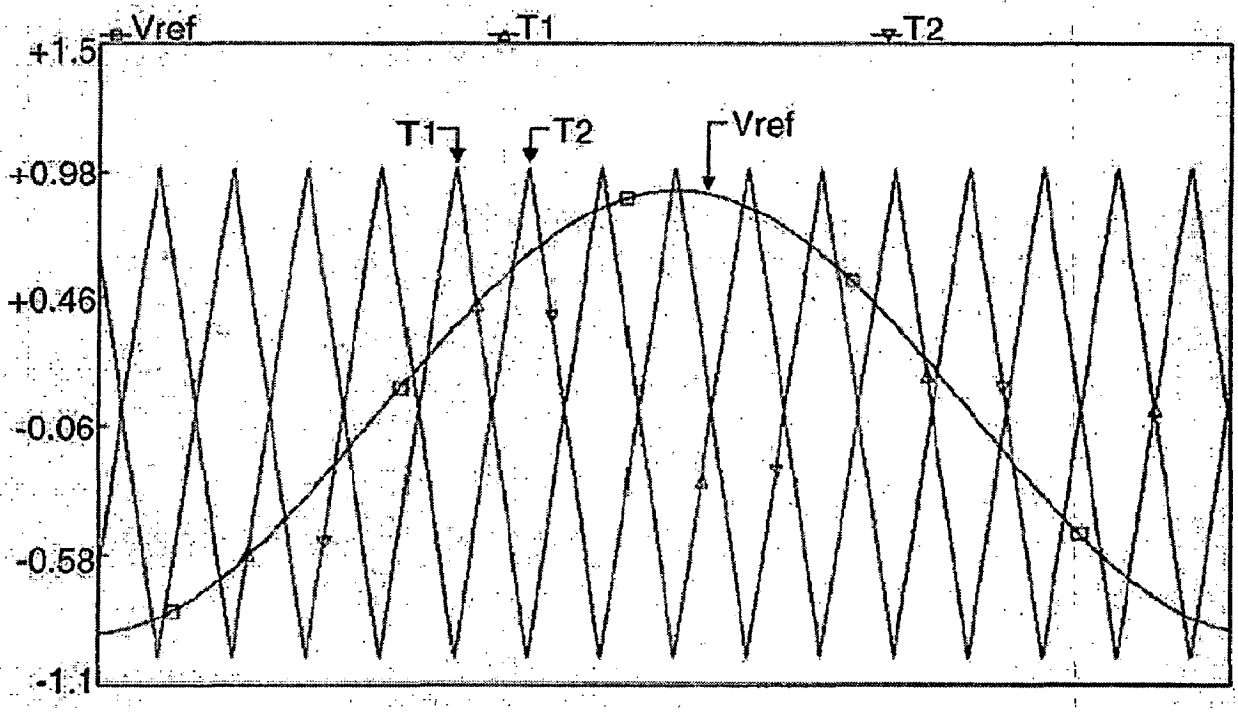
(c)

Figure 4.4: Converter structure and switching pattern, (a) shunt part converter, (b) series part converter, (c) output voltage formation.

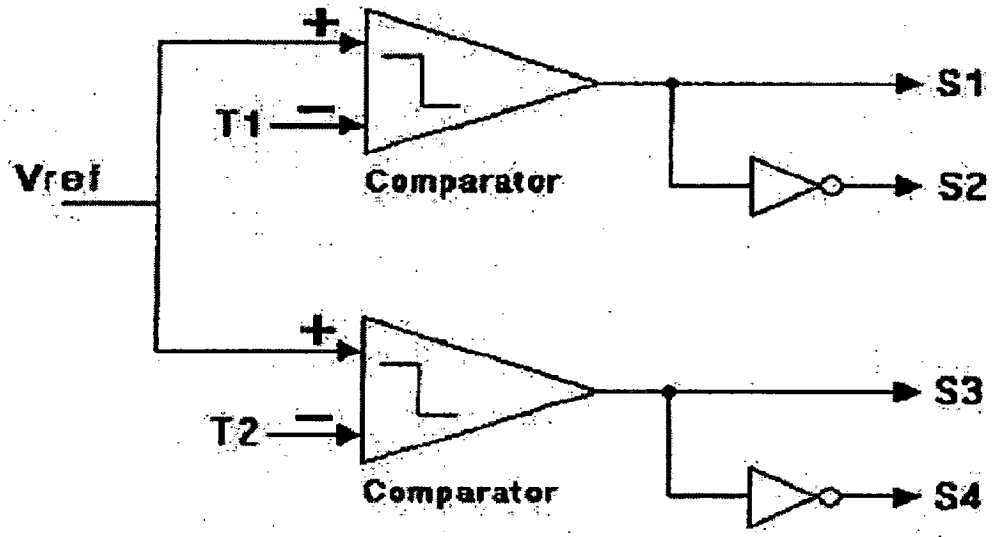
4.3.1 Gate Pulses Generation

The basic principles of sinusoidal pulse width modulation technique are already described in earlier chapter: 2. Fig. 4.5 shows the principle of PWM gate-pulse generation for the proposed UPFC. Fig. 4.5(a) shows two carrier signals and the reference signal to generate the gate pulses for Converter module INV1.

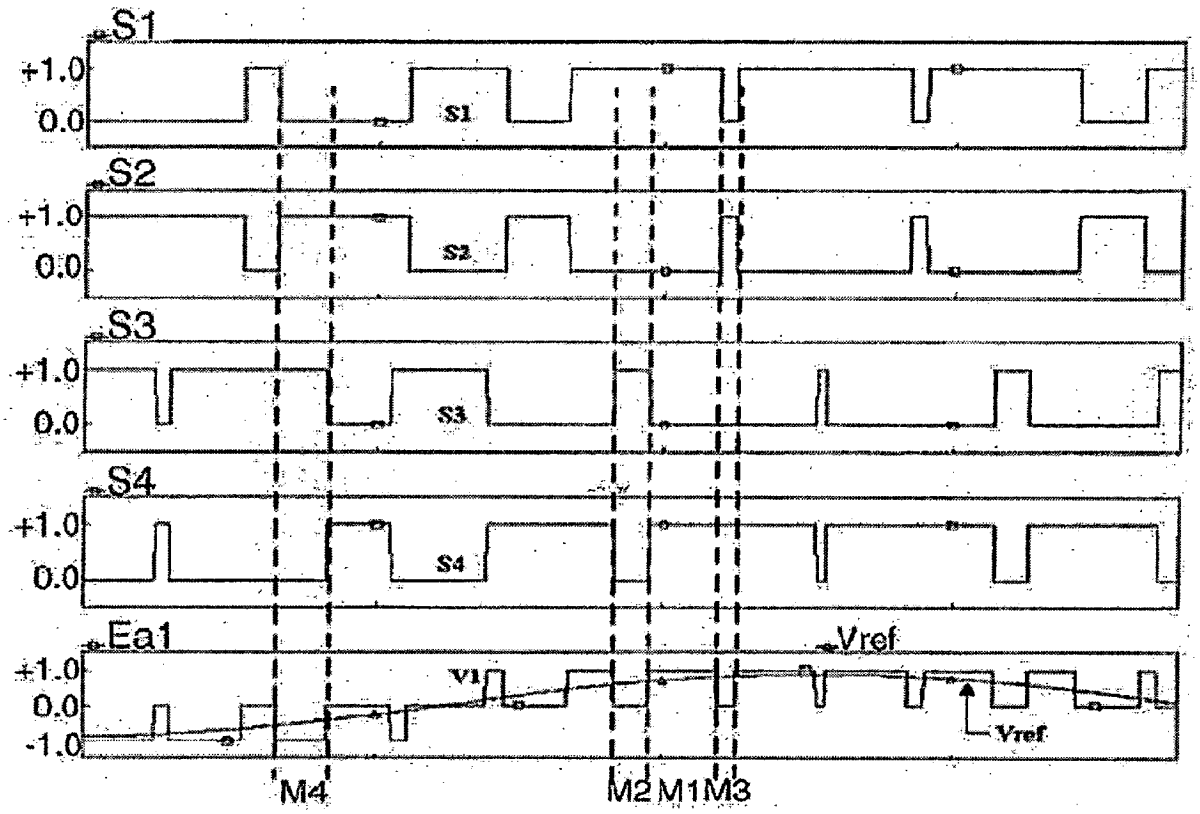
The frequency of carrier T1, T2 is 350 Hz. Each of two carriers has 180° phase shift with each other [16]. The reference signal V_{ref} has maximum value of 1.0 in per unit and has a sinusoidal waveform of 50 Hz Fig. 4.5(b) shows how to generate the gate pulses using the reference and carrier signals. Carrier T1 and T2 are compared with the reference signal. The gate pulses for switches S1 and S3 are inversed to make gate pulses for switches S_2 and S_4. Fig. 4.5(c) shows four gate pulses supplied to switch S_1, S_2, S_3, and S_4, and the output voltage of converter module INV1 with the reference signal Vref. This figure indicates that each switch S_1–S_4 is properly operated according to the switching state in Table 1.



(a)



(b)



(c)

Figure 4.5: Principle of gate pulse generation, (a) carrier and reference signal, (b) gate pulse generation scheme, (c) gate pulse and converter output.

As explained before, two carriers shown in Fig. 4.5(a) are used to generate gate pulses for building up the output voltage $V1$. For generating the voltages V2 and V3, two more sets of carrier waves each set consisting of two carrier waves are used. The carrier waves of each set are 180 degrees phase shifted from each other. Moreover, the carrier waves corresponding to voltages V1, V2, V3 are 120 degrees phase shifted from each other. With this scheme, the output voltage VA has an equivalent switching frequency of 1050 Hz. (3 x 350Hz). Similarly, phase B and C also has the switching frequency of 1050 Hz. The complete details of the ref. sine wave and carrier wave of all the H-Bridges are given in Table 4.2 below.

Table4.2: The complete details of the ref. sine wave and carrier wave of all the H-Bridges

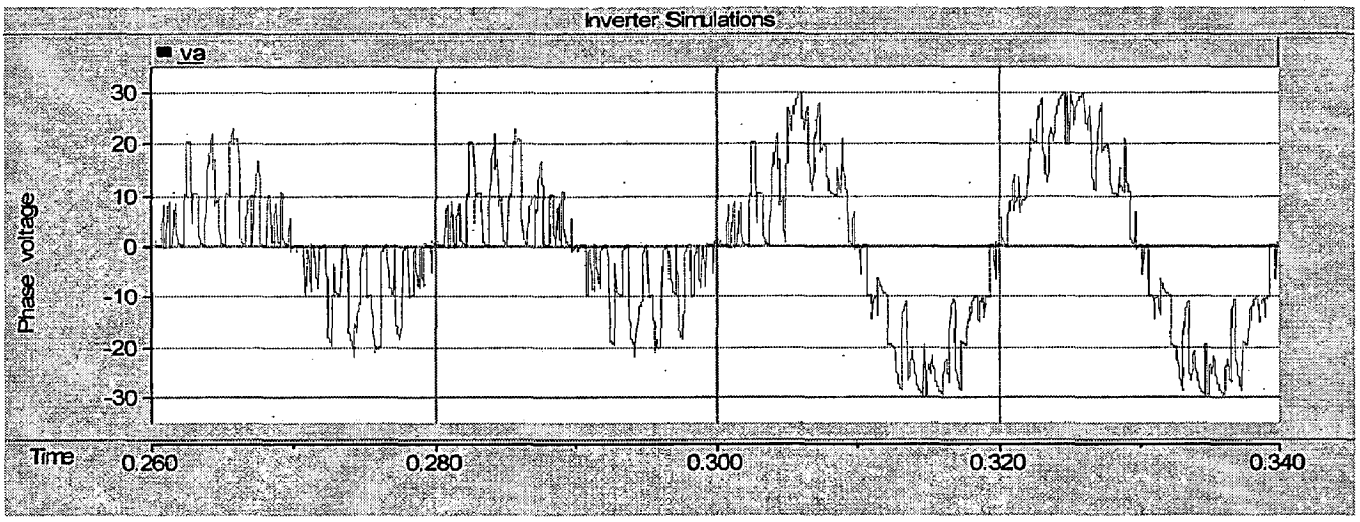
	Phase-a	Phase-b	Phase-c
Ref. & carriers for V_1	$V_{ref} = m_a \sin(wt)$ $T_1, -T_1$	$V_{ref} = m_a \sin(wt-120)$ $T_1, -T_1$	$V_{ref} = m_a \sin(wt+120)$ $T_1, -T_1$
Ref. & carriers for V_2	$V_{ref} = m_a \sin(wt)$ $T_2 = T_1 \angle -120, -T_2$	$V_{ref} = m_a \sin(wt-120)$ $T_2 = T_1 \angle -120, -T_2$	$V_{ref} = m_a \sin(wt+120)$ $T_2 = T_1 \angle -120, -T_2$
Ref. & carriers for V_3	$V_{ref} = m_a \sin(wt)$ $T_3 = T_1 \angle 120, -T_3$	$V_{ref} = m_a \sin(wt-120)$ $T_3 = T_1 \angle 120, -T_3$	$V_{ref} = m_a \sin(wt+120)$ $T_3 = T_1 \angle 120, -T_3$

4.4 Inverter standalone simulations

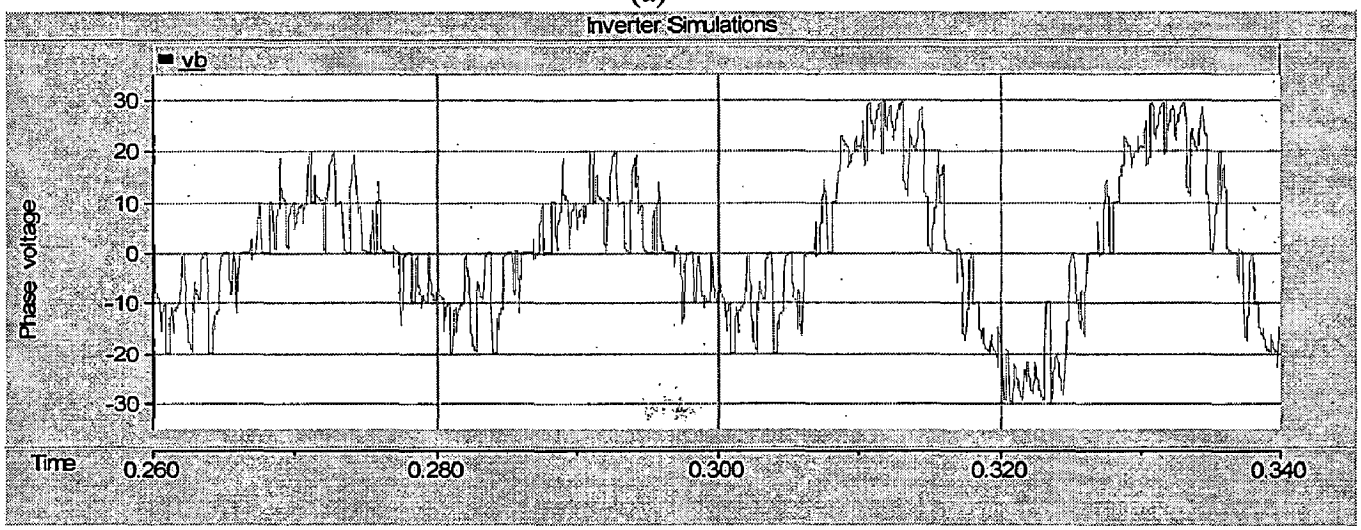
The developed cascaded H-bridge multi level inverter is alone simulated using the PSCAD/EMTDC V4.1. And the corresponding results are given in the Figure 4.6 below.

Fig. 4.6 shows the output voltage build-up of one phase and the harmonic analysis results of the output voltage. Fig. 4.7 shows the output voltage waveforms of each converter modules, V1, V2, V3, and the total output voltage of three converter modules, where the dc voltage V_{dc} is 1.0 per unit Fig. 4.6 shows the spectrum analysis result for the output voltage of one module and the output voltage of cascaded three modules. Large numbers of harmonics are involved in the output of one module, while significantly small numbers of harmonics are involved in the output of cascaded three modules.

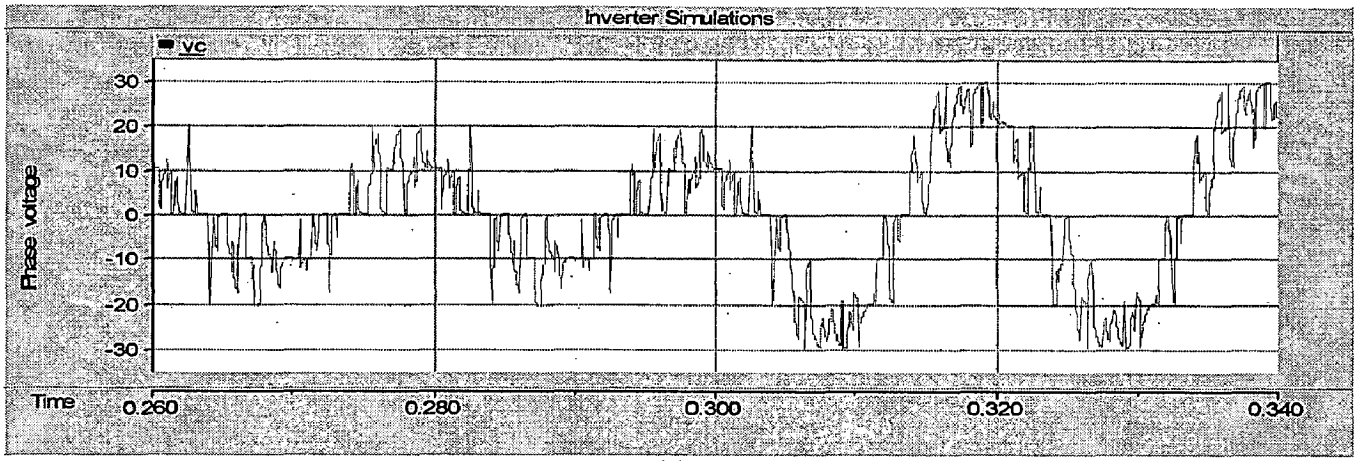
The voltages of all the phases with ma=0.4 initially and then increased to 0.9 at time=0.3sec is as shown in Fig. 4.6 below. Output voltages of each individual H-bridge modules of phase-a are also as shown in Fig. 4.7 below.



(a)

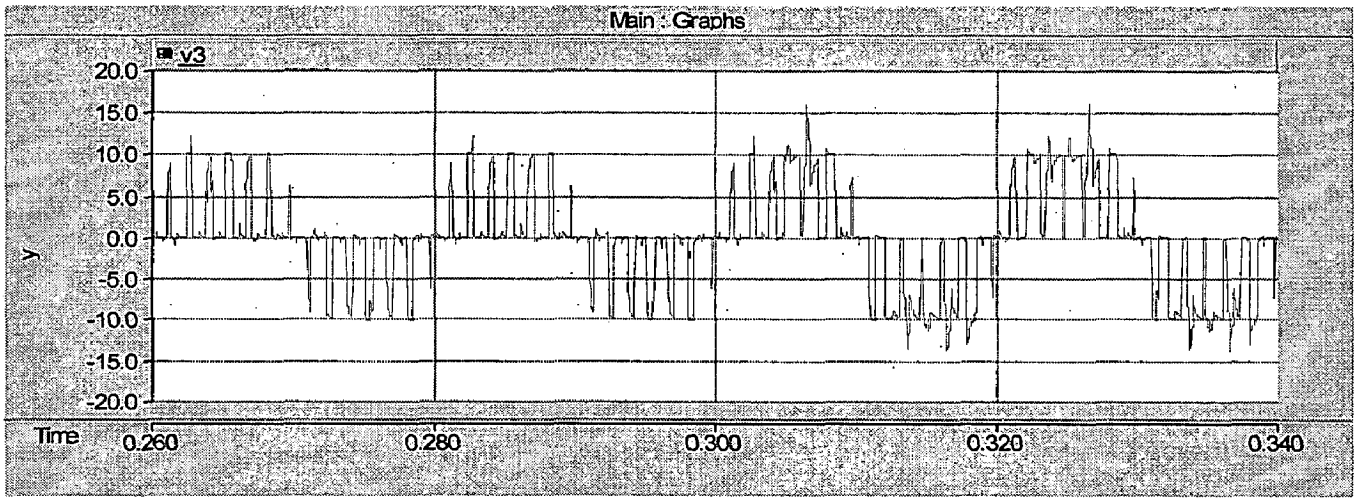


(b)

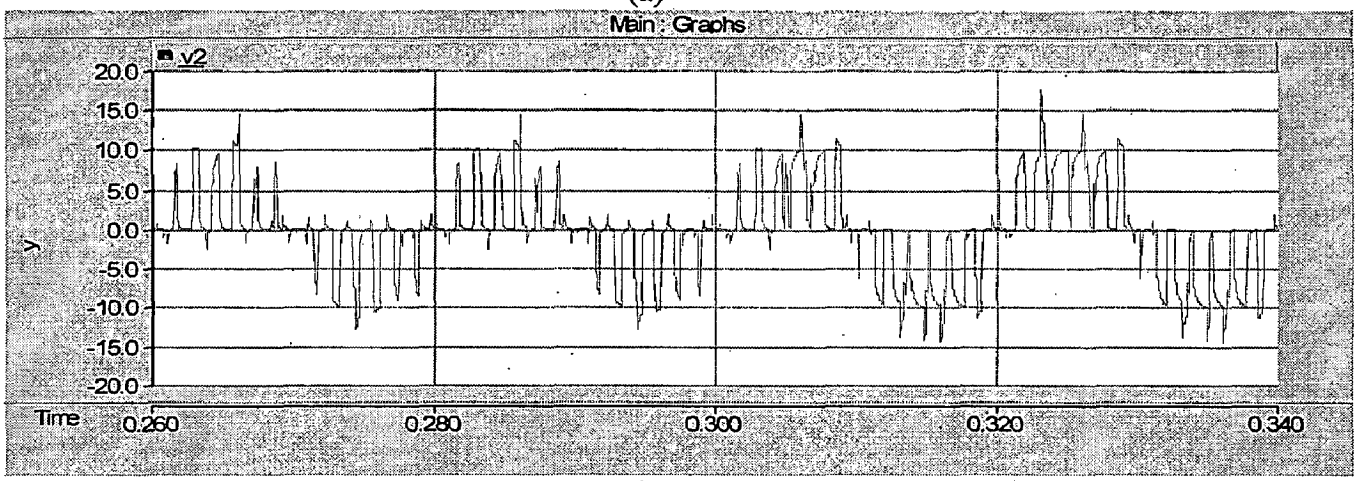


(c)

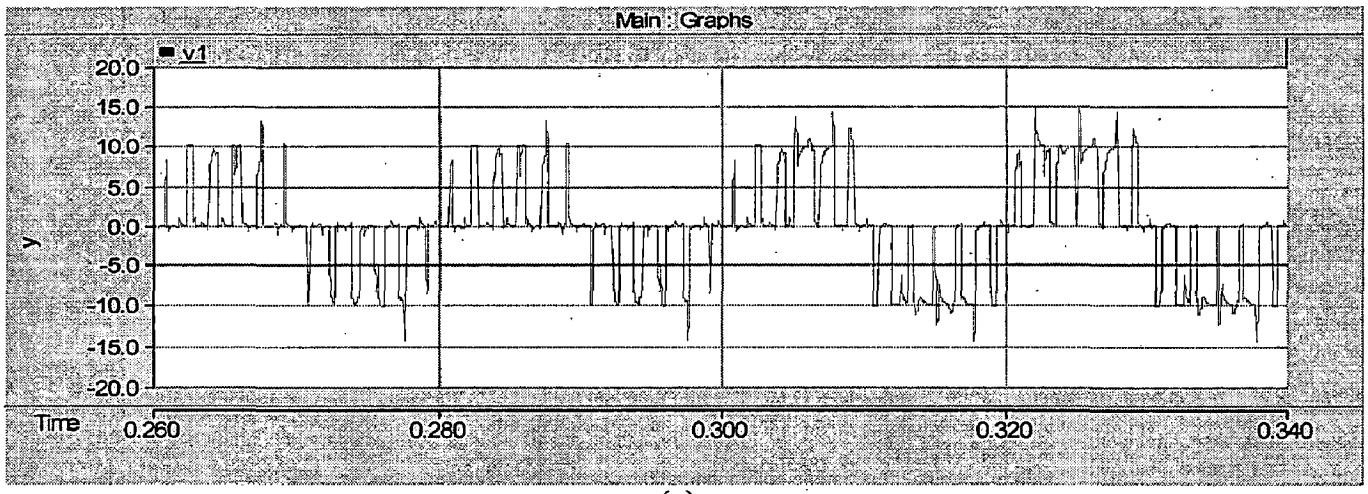
Figure 4.6: Output voltages of all the phases (a) a, (b) b, (c) c.



(a)



(b)



(c)

Figure 4.7: Output voltages of each individual H-bridge modules of phase-a (a) V1 (b) V2 (c) V3.

4.5 Control Schemes for UPFC

As mentioned earlier, both the series and shunt inverters are triggered with SPWM technique. The controllable parameters of this technique are Ma, and phase angle of the reference sine wave. Since the shunt inverter is to control the bus voltage to the ref. set value, it has to supply/absorb the reactive power by maintaining the DC bus voltage at fixed constant value. The used control system block diagram is as shown in fig. below, which is used for controlling the bus voltage at the shunt inverter connected common bus [14].

For achieving power flow control with UPFC in power system, appropriate control schemes of the series and shunt converters of the UPFC are necessary.

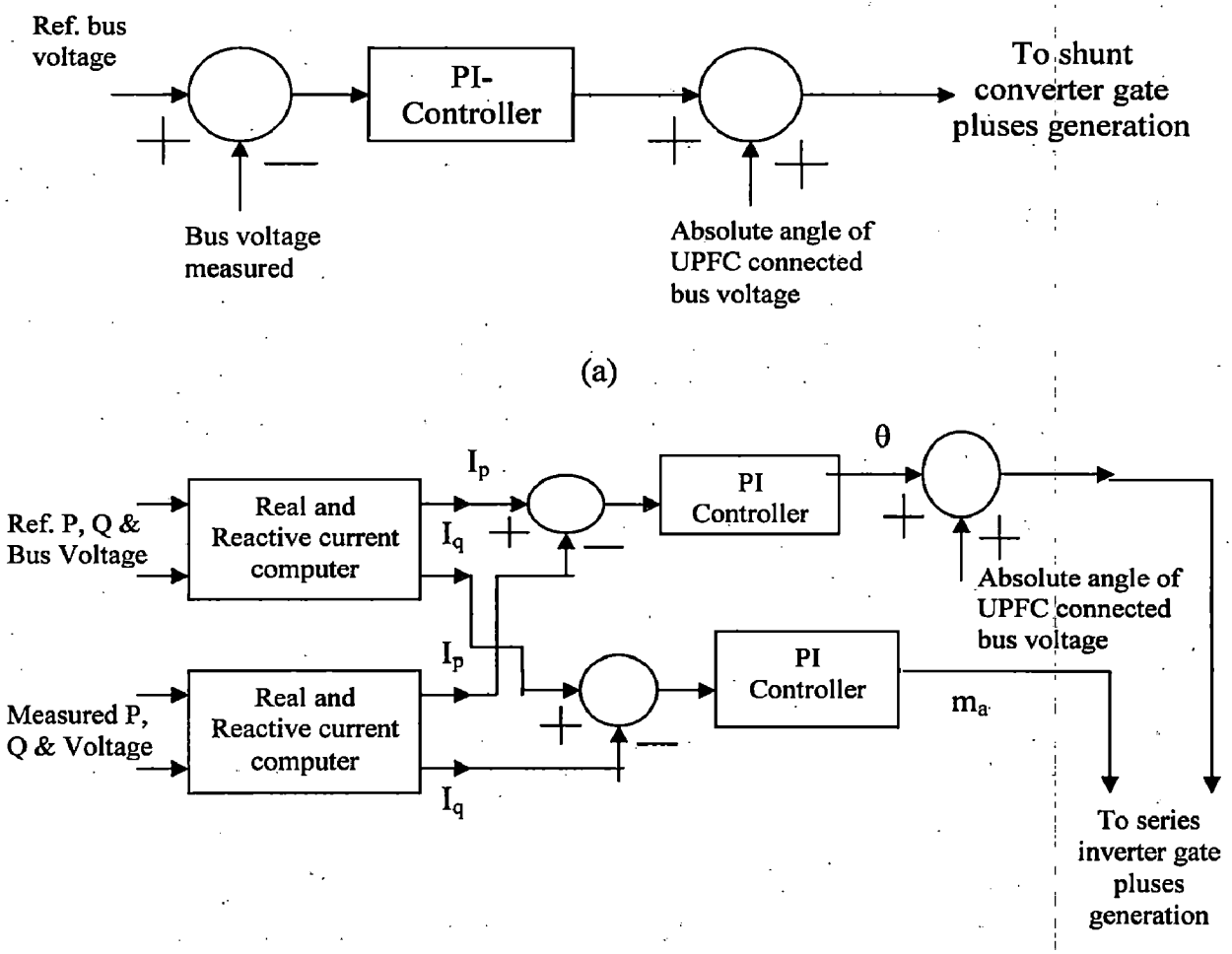


Figure 4.8: Block diagram of UPFC control, (a) shunt converter control, (b) series converter control.

Fig. 4.8 shows a configuration of the UPFC controller used in the simulation. Fig. 4.8(a) shows a control block diagram for the series converter and Fig. 4.8(b) for the shunt converter in automatic power flow control mode. The automatic power flow control is achieved by means of a vector control scheme that regulates the transmission line current using a synchronous frame, in which the control quantities appear as dc signals in the steady state. The appropriate reactive and real current components, i_q and i_p, are determined for a desired P_{ref} and Q_{ref}. These are compared with the measured line

currents, i_q and i_p, and used to drive the magnitude and angle of the series converter voltage, V_{pq} and α_{pq}, respectively [14, 16]. In the control scheme for the shunt converter, the magnitude of the output voltage is directly proportional to the dc voltage and only its angle is controllable. The loop regulates the ac bus voltage and also controls the dc capacitor voltage. It changes the phase angle α of the output voltage with respect to the ac bus voltage until the dc capacitor voltage reached the value necessary to achieve the reactive power compensation demanded.

4.6 Detailed Simulation studies and Results

To study the performance of the UPFC in a sample power system, the test system described in chapter 1 has been used.

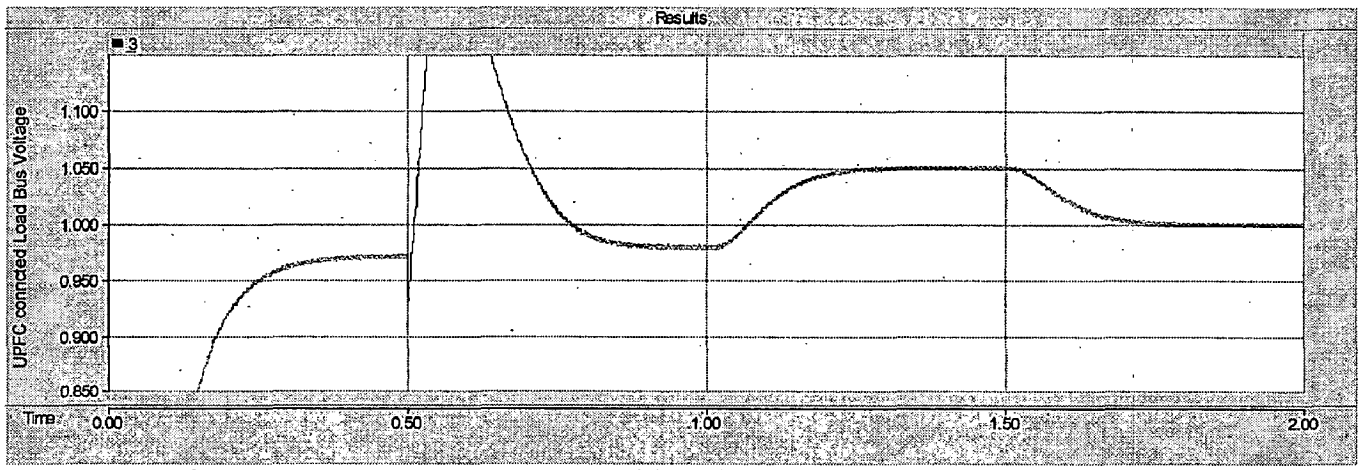
The controlled or uncontrolled m_a and phase angle of the two different converters are taken as the inputs to these corresponding page modules. Using these parameters of the inverters, all the gate pulses are generated (as discussed in the above section) in the same module inside itself. The DC bus terminals of both the inverters are brought out for connecting the capacitors in the main page/module. The PSCAD/EMTDC graphical view is given in Appendix D. The various parameters of the control system and the other apparatus are also given in Appendix D.

4.6.1 Control of Bus Voltage

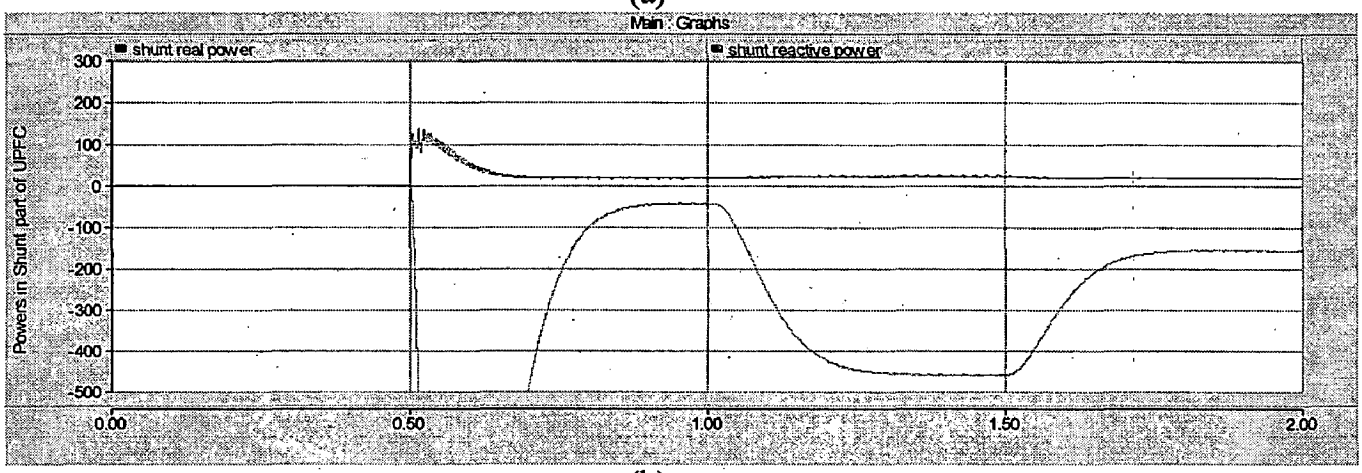
After designing this configuration of UPFC as described above briefly. First the system is run without connecting the UPFC. After reaching the steady state the UPFC is being connected to the system at time t=0.5sec. Now, only the shunt part of the UPFC is switched on to prove that it can also control the bus voltage, where it is connected at the ref. set value. The various graphs showing the above mentioned result are as shown in Figure 4.10 below. The corresponding simulation parameters are given in the Table 4.3.

Table 4.3: Simulation parameters for bus voltage control

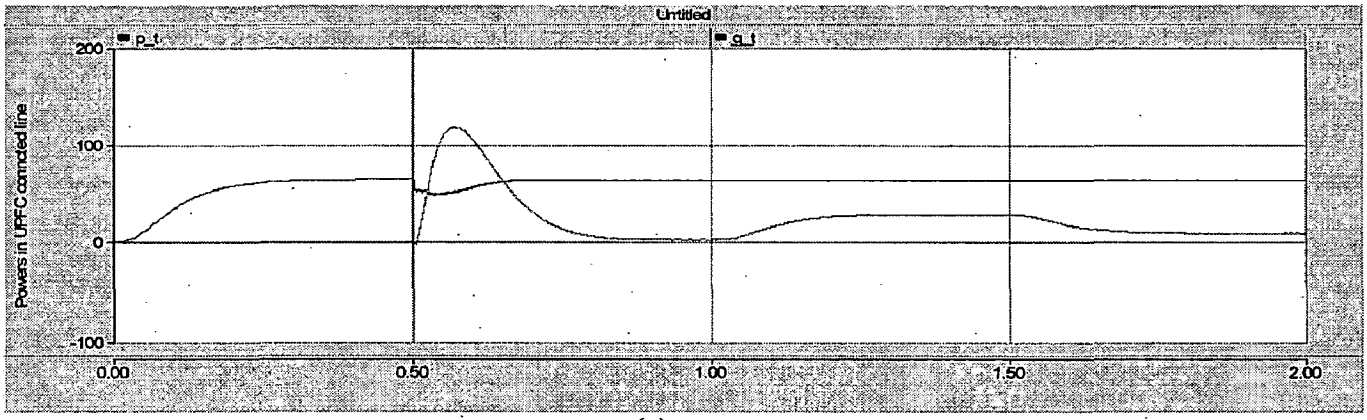
Time in seconds (from-to)	Ref. set Bus voltage $V_{ref.}$ (pu)
0.5-1.0	0.98
1.0-1.5	1.05
1.5-2.0	1.0



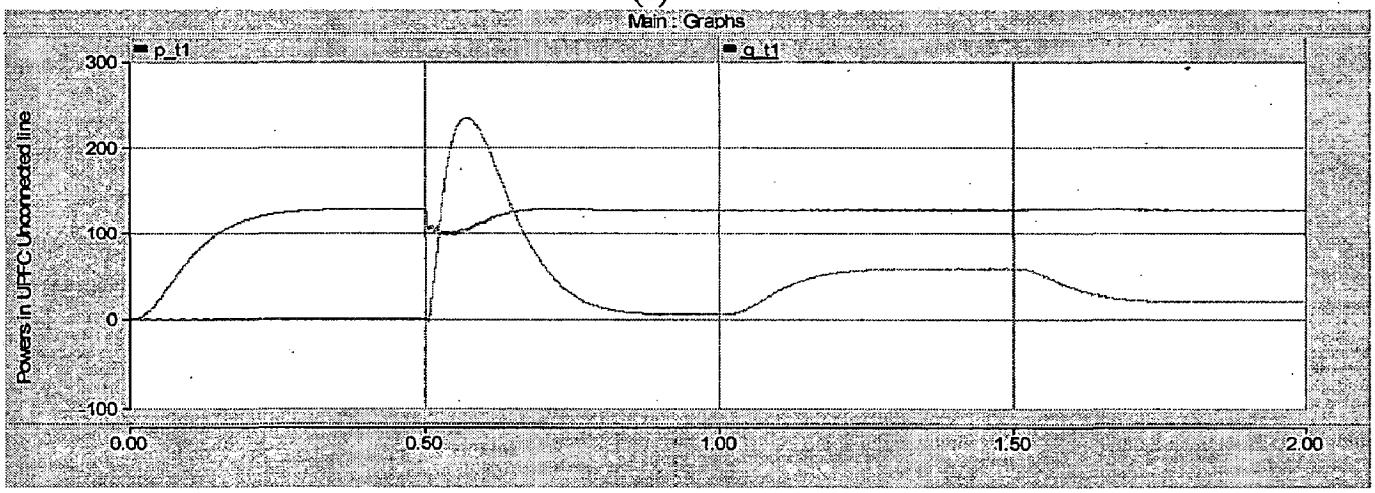
(a)



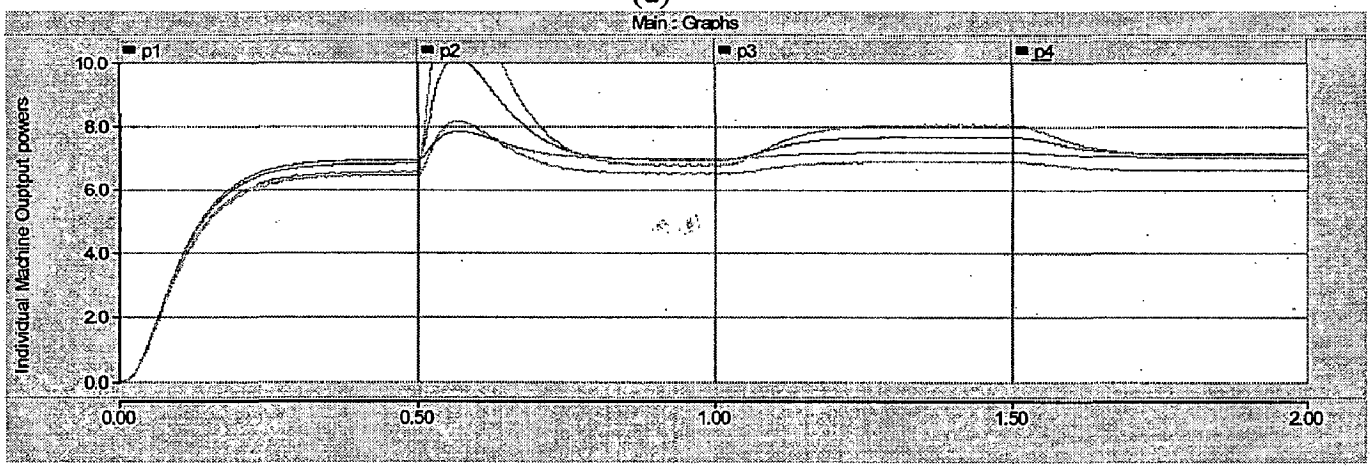
(b)



(c)



(d)



(e)

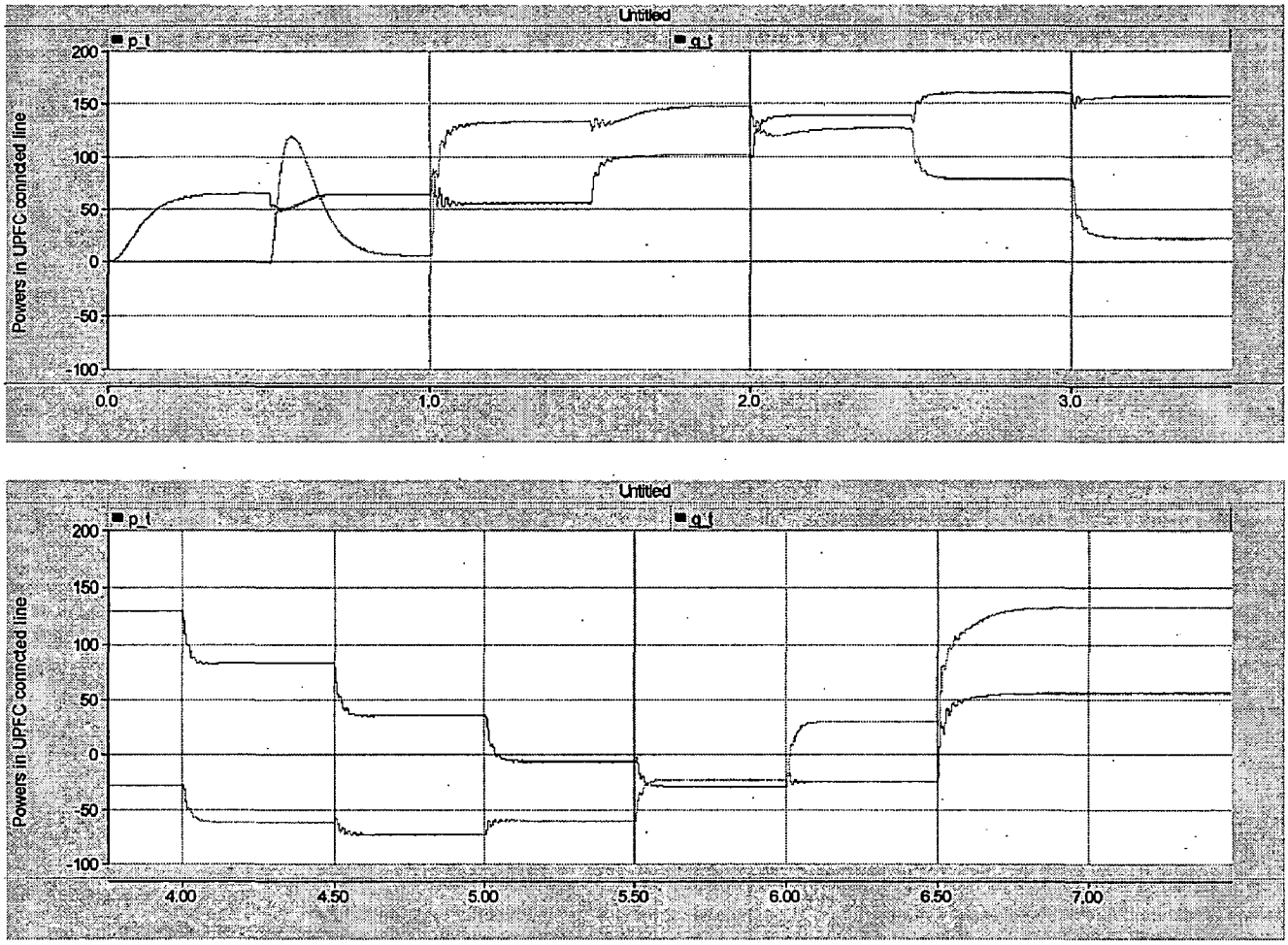
Figure 4.10: Simulation results of UPFC as bus voltage control. (a) Connected Bus voltage, (b) Real & Reactive powers taken by shunt part of the UPFC, (c) Real & Reactive powers in the UPFC connected line, (d) Real & Reactive powers in the UPFC un-connected line, (e) Individual machine output powers, (f) DC Bus voltages.

4.6.2 UPFC as controlling the powers in open loop

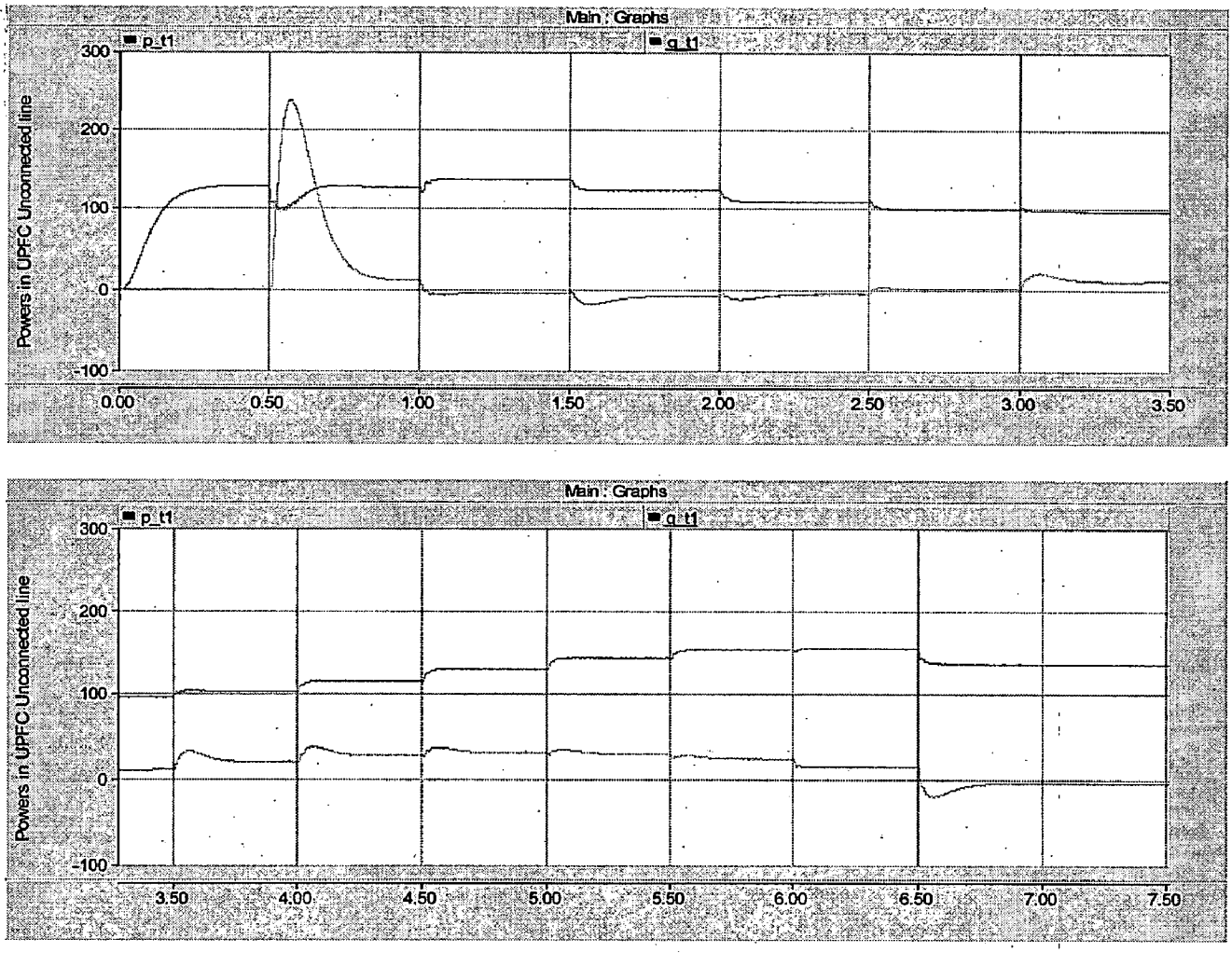
Now, the system is run without connecting the UPFC. After reaching to the steady state the UPFC is being connected to the system at time t=0.5sec. Now, both the shunt and series inverters of the UPFC are switched on at the same time, and then changed the parameters of the series inverter i.e. m_a & phase angle. The various graphs result is as shown in Figure 4.11 below. Keeping the Ma of the shunt inverter fixed at 0.9, the phase angle is changed from 0 to 360 in steps of 30 degrees each time. The corresponding simulation parameters are given in the Table 4.4.

Table 4.4: Simulation parameters for UPFC in open loop control

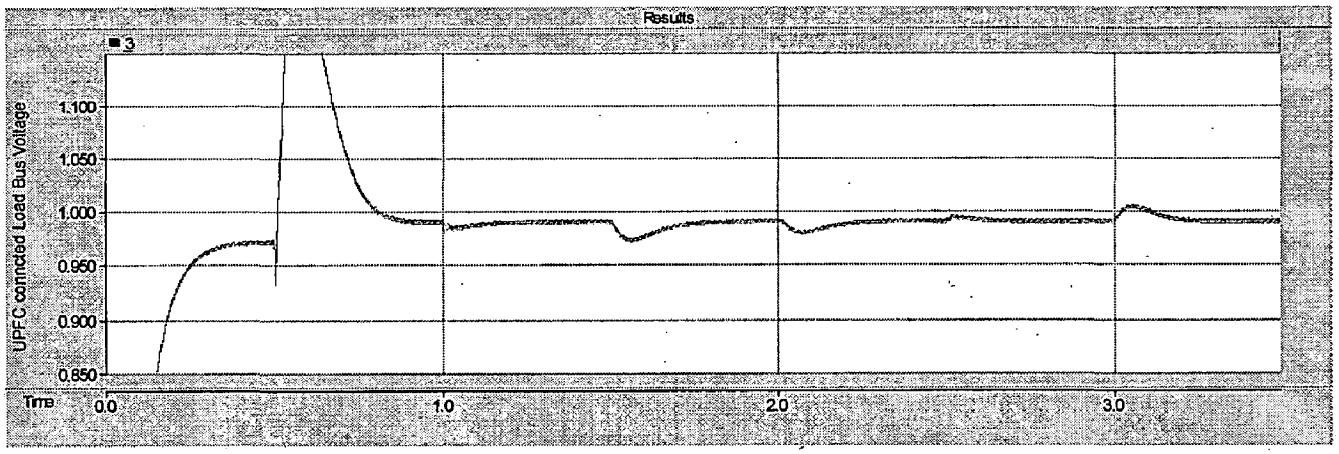
Time (sec.) From-to	Ma	Phase (degrees)	$V_{ref.}$ (pu)
0.5-1.0	0	0	0.99
1.0-1.5	0.9	0	0.99
1.5-2.0	0.9	30	0.99
2.0-2.5	0.9	60	0.99
2.5-3.0	0.9	90	0.99
3.0-3.5	0.9	120	0.99
3.5-4.0	0.9	150	0.99
4.0-4.5	0.9	180	0.99
4.5-5.0	0.9	210	0.99
5.0-5.5	0.9	240	0.99
5.5-6.0	0.9	270	0.99
6.0-6.5	0.9	300	0.99
6.5-7.5	0.9	360	0.99

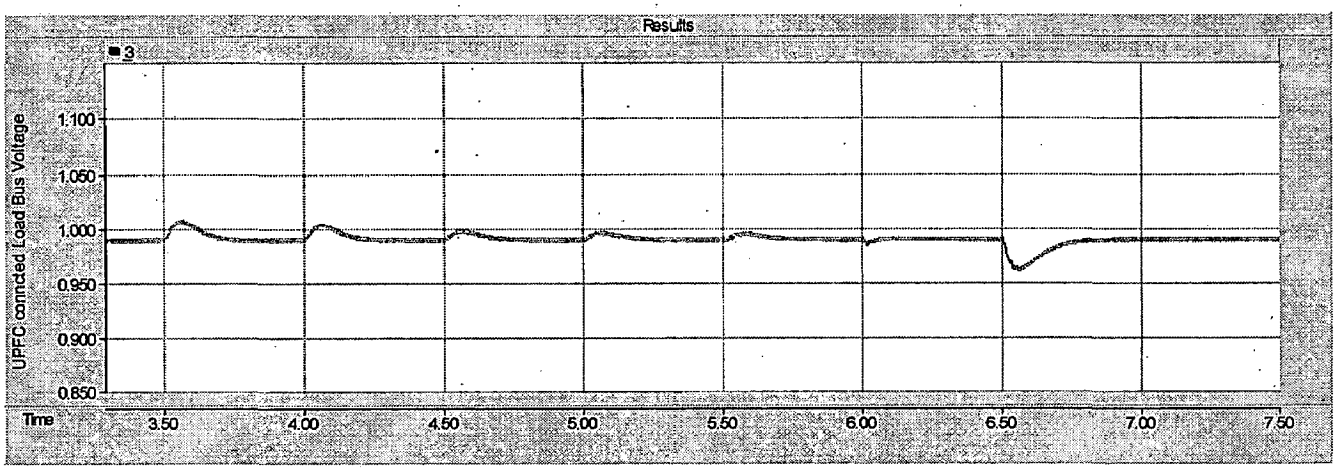

Untitled
p_t
q_t
Powers in UPFC connded line
200
150
100
50
0
-50
-100
0.0
1.0
2.0
3.0
Untitled
p_t
q_t
Powers in UPFC connded line
200
150
100
50
0
-50
-100
4.00
4.50
5.00
5.50
6.00
6.50
7.00

(a)

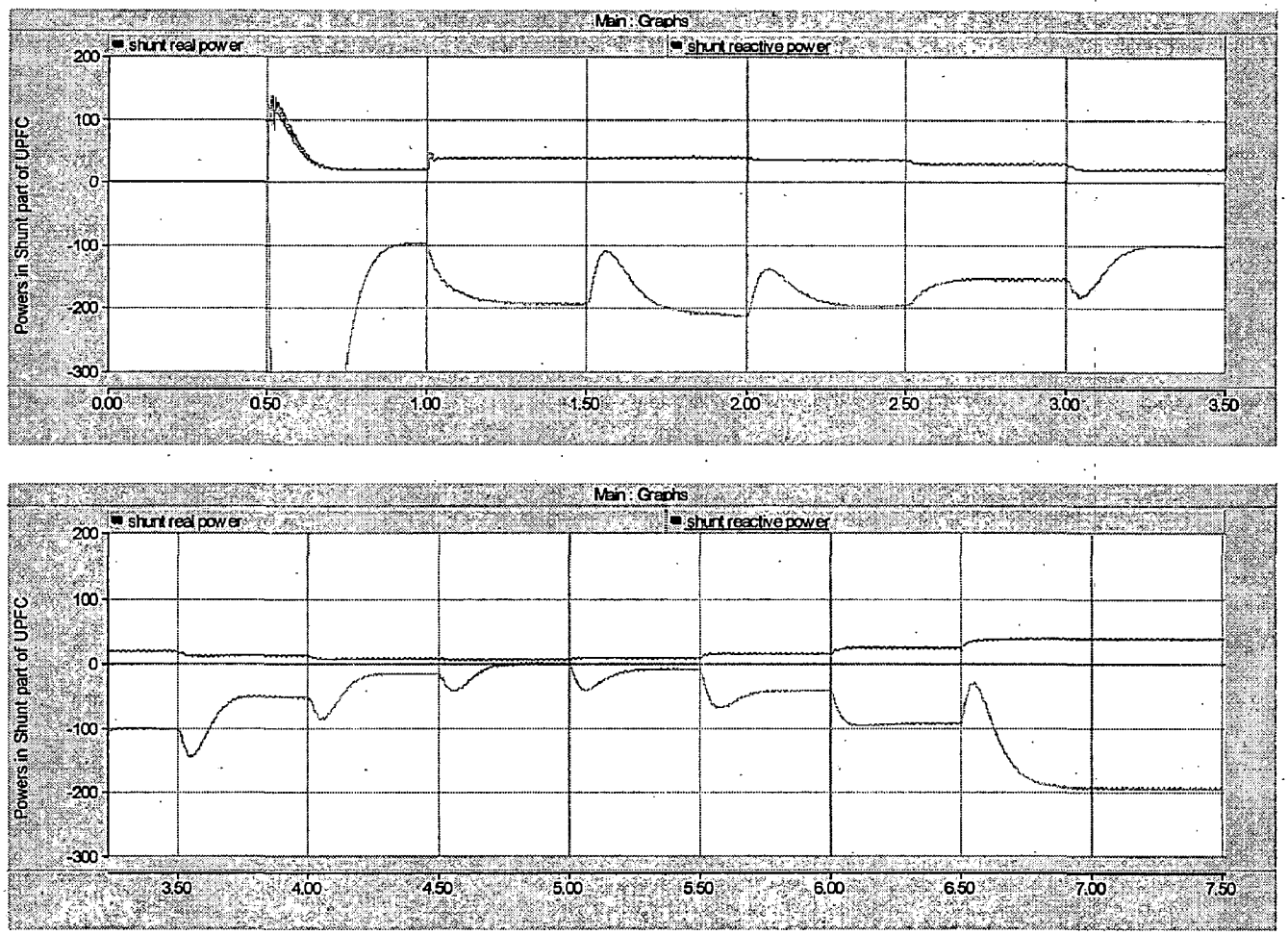

Main : Graphs
p_t1
q_t1
Powers in UPFC Unconnected line
300
200
100
0
-100
0.00
0.50
1.00
1.50
2.00
2.50
3.00
3.50
Main : Graphs
p_t1
q_t1
Powers in UPFC Unconnected line
300
200
100
0
-100
3.50
4.00
4.50
5.00
5.50
6.00
6.50
7.00
7.50

(b)

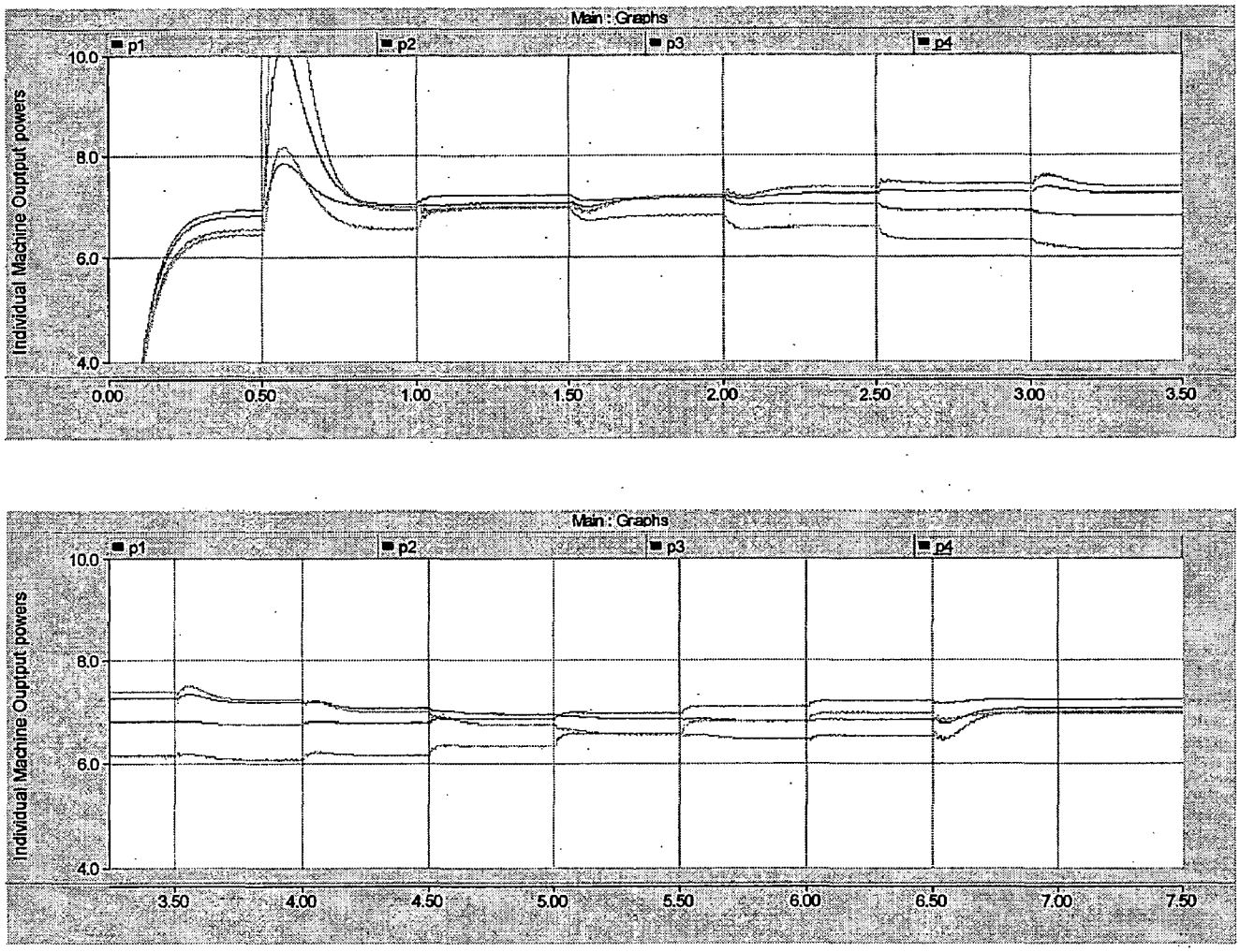

Results
3
UPFC connded Load Bus Voltage
1.100
1.050
1.000
0.950
0.900
0.850
Time
0.0
1.0
2.0
3.0


Results
3
UPFC connded Load Bus Voltage
1.100
1.050
1.000
0.950
0.900
0.850
Time
3.50
4.00
4.50
5.00
5.50
6.00
6.50
7.00
7.50

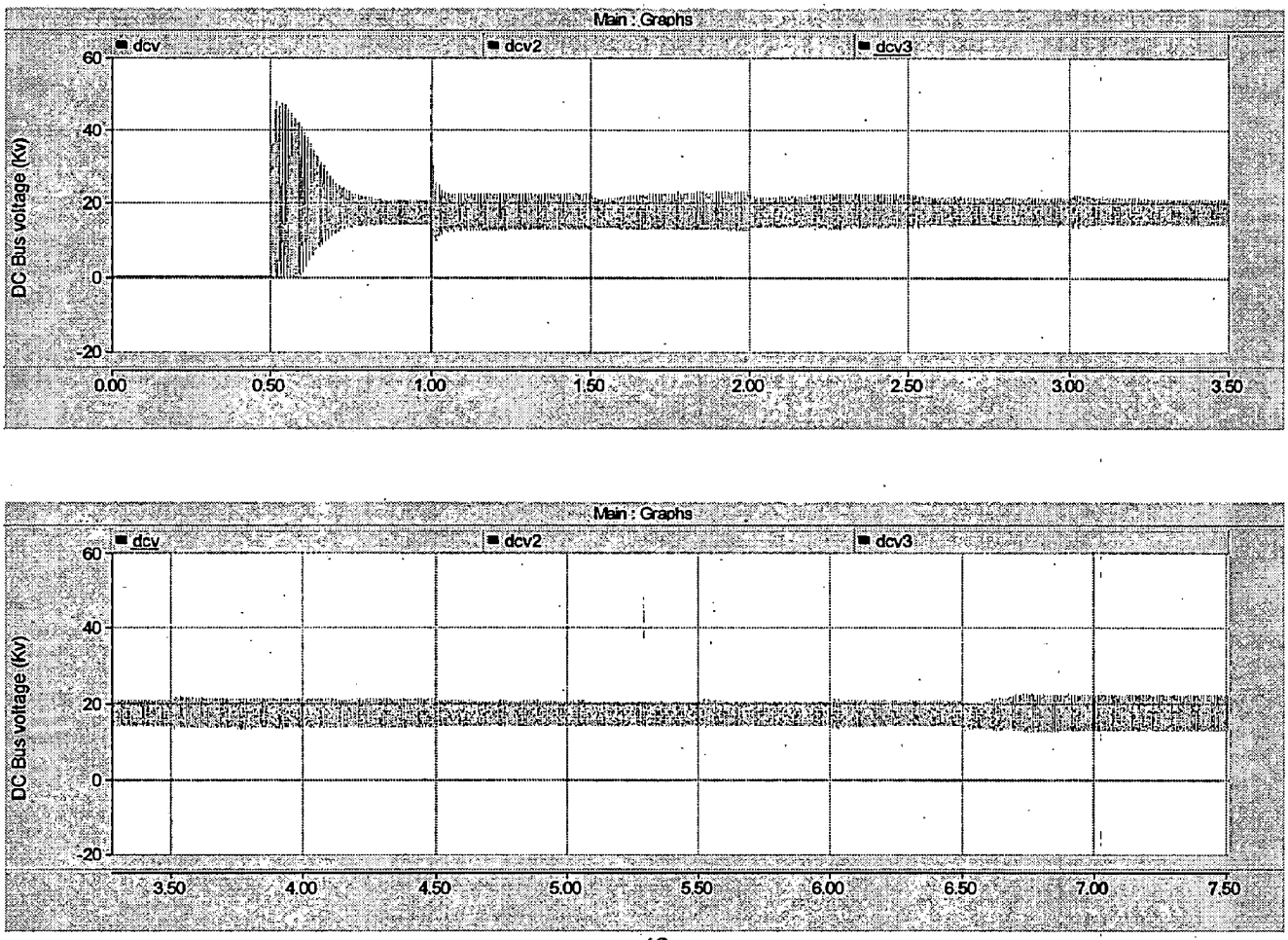
(c)


Main : Graphs
shunt real power
shunt reactive power
Powers in Shunt part of UPFC
200
100
0
-100
-200
-300
0.00
0.50
1.00
1.50
2.00
2.50
3.00
3.50
Main : Graphs
shunt real power
shunt reactive power
Powers in Shunt part of UPFC
200
100
0
-100
-200
-300
3.50
4.00
4.50
5.00
5.50
6.00
6.50
7.00
7.50

(d)


Main : Graphs
p1
p2
p3
p4
Individual Machine Ouptput powers
10.0
8.0
6.0
4.0
0.00
0.50
1.00
1.50
2.00
2.50
3.00
3.50
Main : Graphs
p1
p2
p3
p4
Individual Machine Ouptput powers
10.0
8.0
6.0
4.0
3.50
4.00
4.50
5.00
5.50
6.00
6.50
7.00
7.50

(e)



(f)

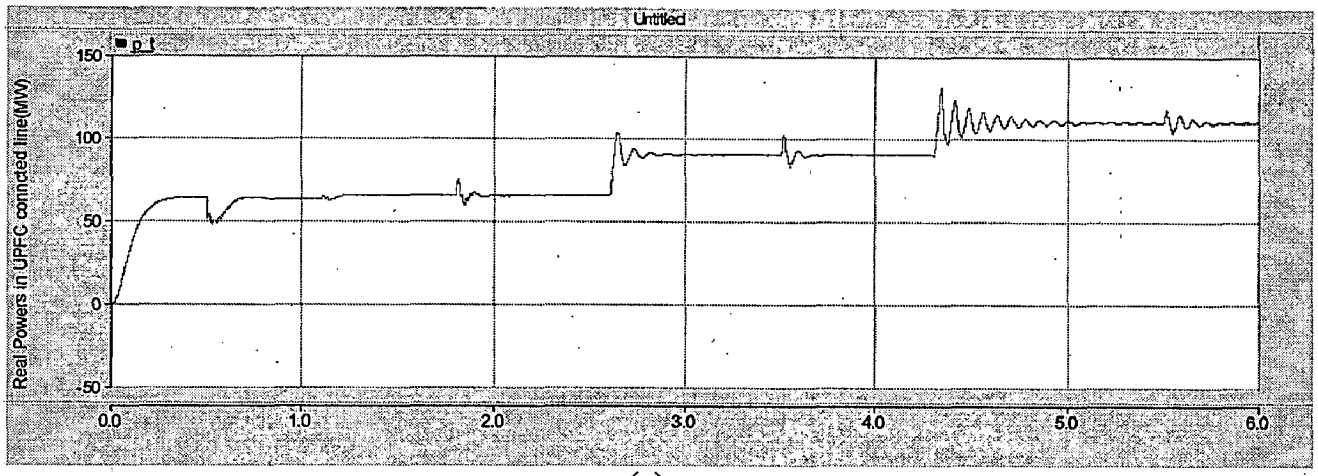
Figure 4.11: Simulation results of UPFC in open-loop control. (a) Real & Reactive powers in the UPFC connected line, (b) Real & Reactive powers in the UPFC un-connected line, (c) Connected Bus voltage, (d) Real & Reactive powers taken by shunt part of the UPFC, (e) Individual machine output powers, (f) DC Bus voltages.

4.6.3 UPFC as controlling the powers in closed loop

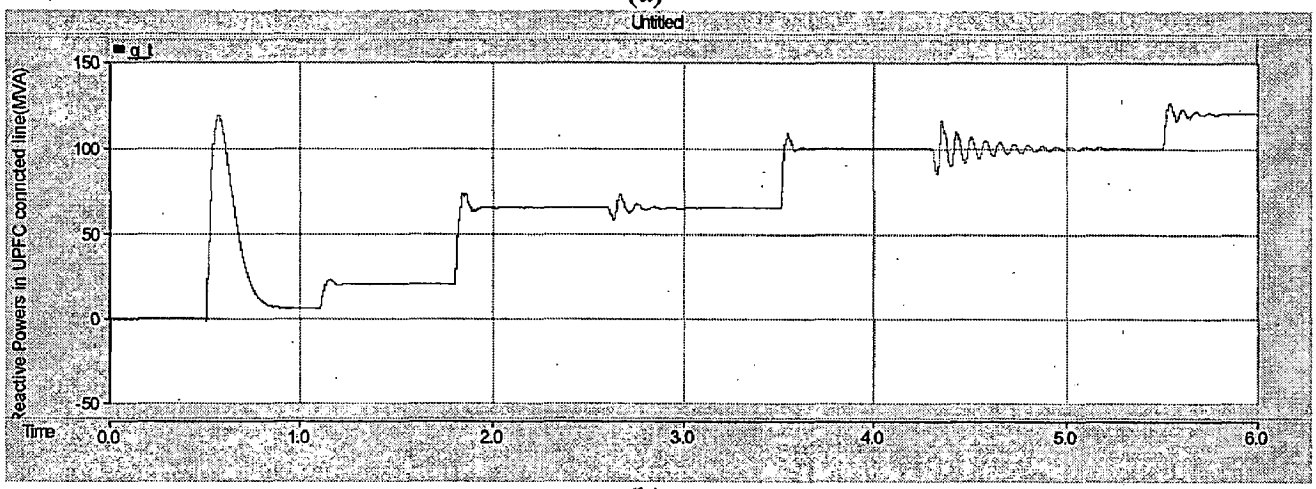
For simulating the performance of UPFC in closed loop control, the block diagram of the control system shown in Figure 4.12 is used. The automatic power flow control is achieved by means of a vector control scheme that regulates the transmission line current using a synchronous frame, in which the control quantities appear as dc signals in the steady state. Here also, the system is run without connecting the UPFC for reaching the steady state. After reaching to the steady state the UPFC is being connected to the system at time t=0.5sec with P & Q ref. values set at the initial values only to have to zero output voltage from the series inverter, so that reducing the transient effects. Now, both the shunt and series inverters of the UPFC are switched on at the same time. And then changed the P & Q ref. values, and observed that both the real and reactive powers are tracking the corresponding ref. set values with in least min. time. The various graphs result is as shown in Figure 4.12 below. The corresponding simulation parameters are given in the Table 4.5.

Table 4.5: Simulation parameters for UPFC in closed loop control.

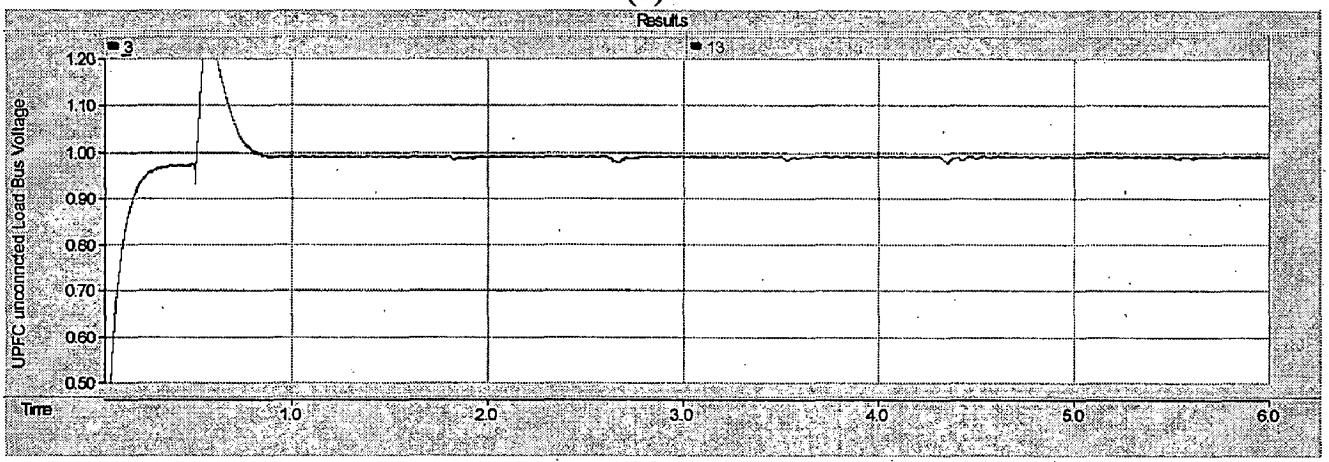
Time (sec.) From-to	$V_{ref.}$ (pu)	$P_{ref.}$ (MW)	$Q_{ref.}$ (MVAR)
1.-1.1	0.99	65	5
1.1-1.8	0.99	65	20
1.8-2.6	0.99	65	65
2.6-3.5	0.99	90	65
3.5-4.4	0.99	90	100
4.4-5.5	0.99	110	100
5.5-6.0	0.99	110	120


Untitled
p_l
Real Powers in UPFC connected line(MW)
150
100
50
0
-50
0.0
1.0
2.0
3.0
4.0
5.0
6.0

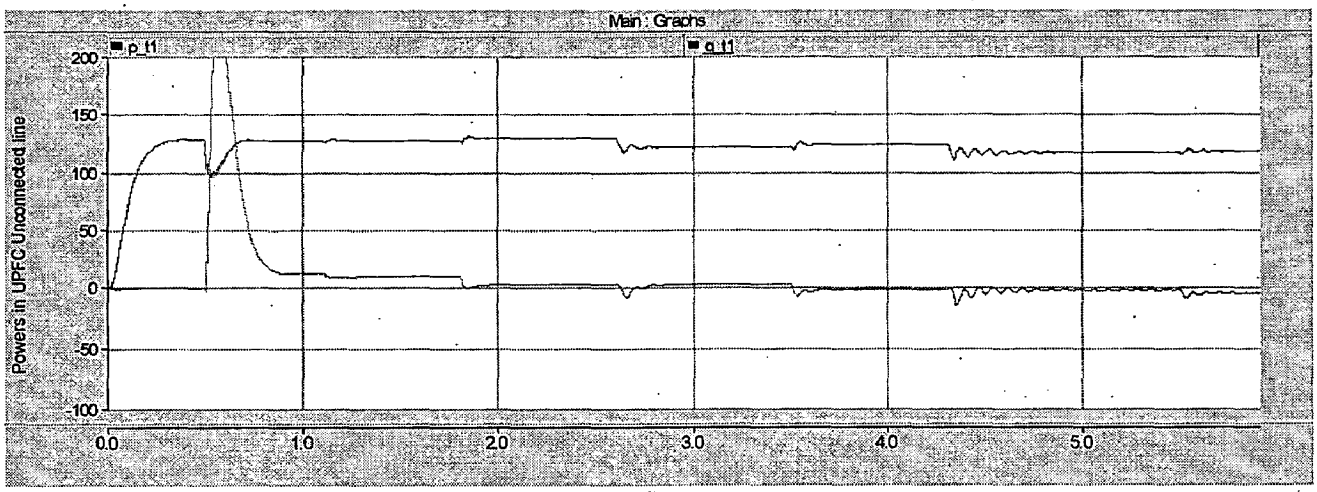
(a)


Untitled
q_l
Reactive Powers in UPFC connected line(MVA)
150
100
50
0
-50
Time
0.0
1.0
2.0
3.0
4.0
5.0
6.0

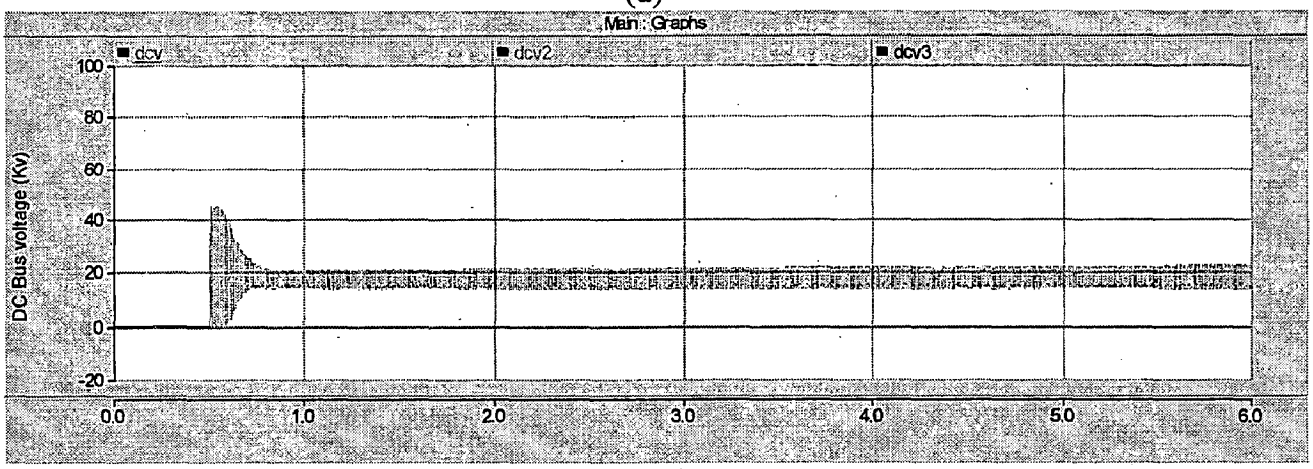
(b)


Results
3
13
UPFC unconnected Load Bus Voltage
1.20
1.10
1.00
0.90
0.80
0.70
0.60
0.50
Time
1.0
2.0
3.0
4.0
5.0
6.0

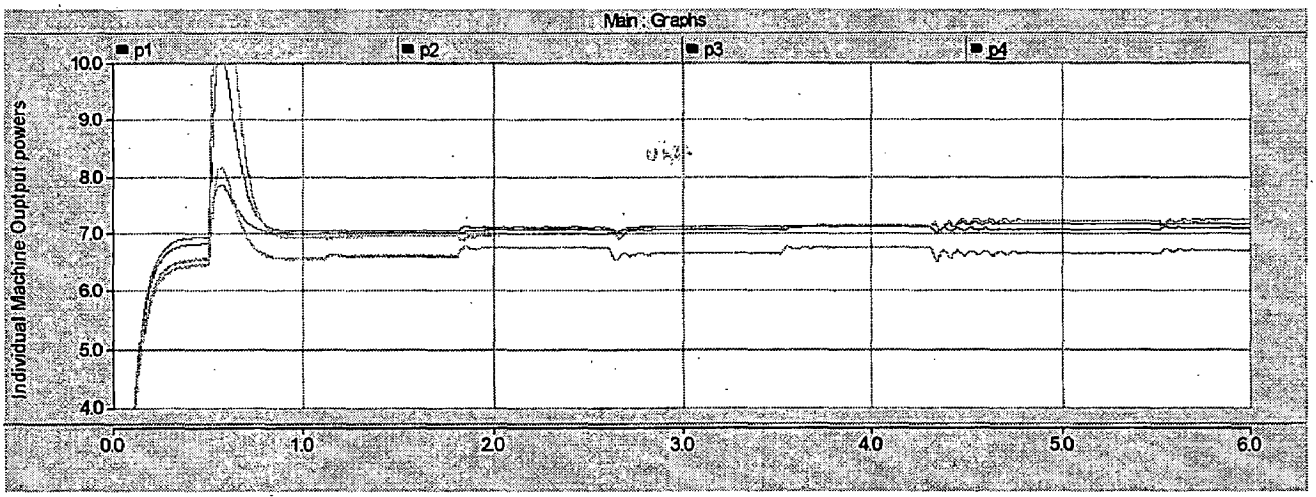
(c)


Main: Graphs
p_t1
q_t1
Powers in UPFC Unconnected line
200
150
100
50
0
-50
-100
0.0
1.0
2.0
3.0
4.0
5.0

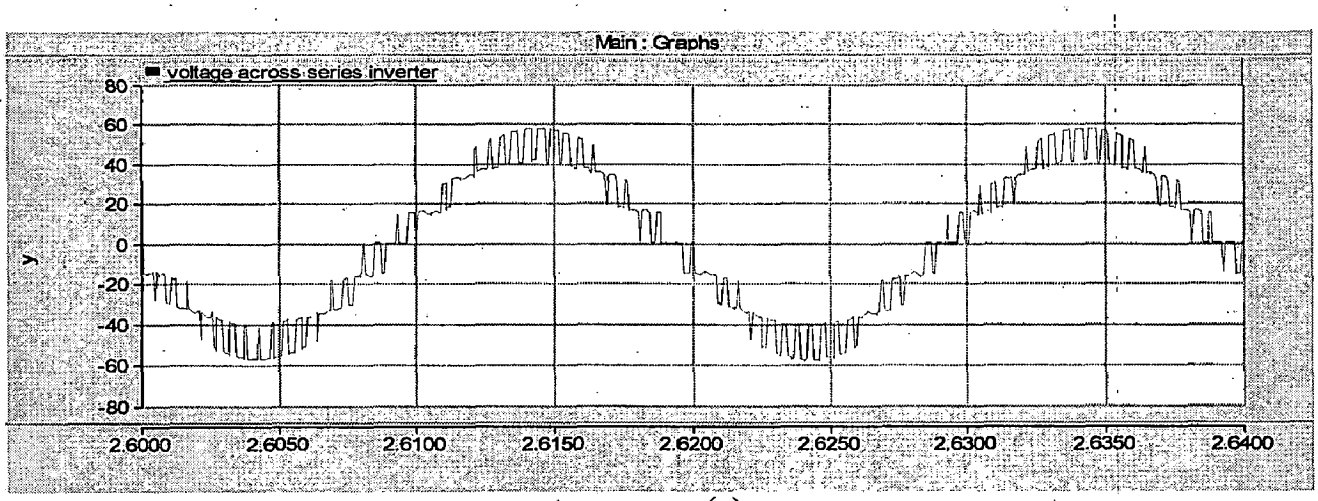
(d)


Main: Graphs
dcv
dcv2
dcv3
DC Bus voltage (Kv)
100
80
60
40
20
0
-20
0.0
1.0
2.0
3.0
4.0
5.0
6.0

(e)


Main: Graphs
p1
p2
p3
p4
Individual Machine Output powers
10.0
9.0
8.0
7.0
6.0
5.0
4.0
0.0
1.0
2.0
3.0
4.0
5.0
6.0

(f)



(g)

Figure 4.12: Simulation results of UPFC in closed-loop control. (a) Real power in the UPFC connected line, (b) Reactive power in the UPFC connected line, (c) UPFC Connected Bus voltage, (d) Real & Reactive powers in the UPFC un-connected line, (e) DC Bus voltages, (f) Individual machine output powers. (g) Series inverter output voltage wave form.

4.7 conclusions

In this chapter, beginning with the basic operating principles of the cascaded H bridge multilevel inverter, the operation of H bridge inverter module based UPFC has been described in detail. The simulation results for the stand alone mode of the inverter have been presented. Also automatic power flow control schemes of the UPFC for controlling the real and reactive power flow over the transmission grid have also been developed. The detailed simulation results in various modes of operation of UPFC are also presented here.

Comparisons & Conclusions

5.1 Comparison of different configurations considered

This chapter outlines the comparative analysis of all the three configurations of UPFC based on steady state analysis carried out in this work. The performances of the UPFCs are compared on the basis of DC Bus voltage magnitude and its variations, physical structure, possible scheme for implementation, switching frequency, harmonic content and rating of UPFC.

5.1.1 Switching frequency and Harmonic content

For the case of UPFC using basic 2-level VSC, the shunt inverter is switched using HCC scheme as discussed in chapter 2. By its own property of HCC, the switching frequency will be very high, thereby increasing the switching losses.

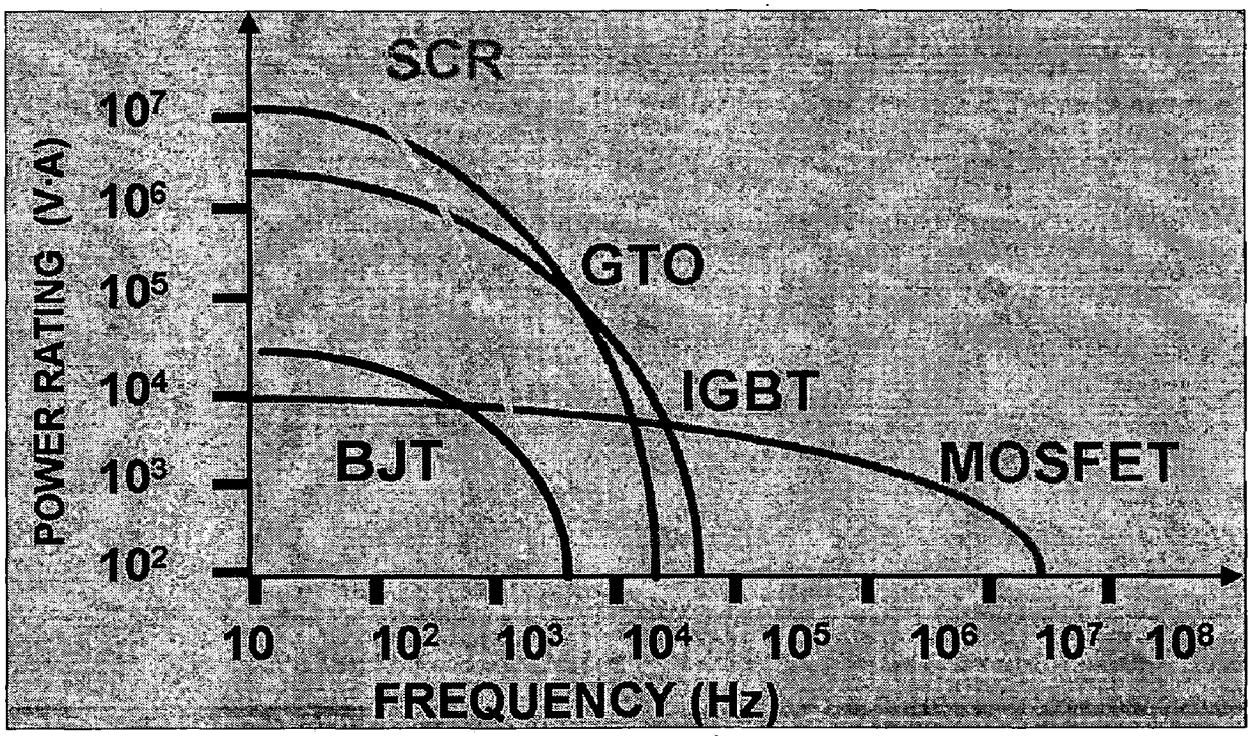


Fig. 5.1 characteristics of different power devices

By nature, since the switching frequency is high, the rating of device will be low. Especially in the case of GTOs, the power rating will be exponentially decreases with increase in switching frequency as shown in Fig. 5.1. So for implementing it practically, GTOs cant be used. So IGBTs / MOSFETs are only the best possible solution for implementing it practically. The harmonic content of the shunt part of UPFC, it is obviously low because the shunt inverter is switched at a high frequency. But whereas the harmonic content on the series side of the UPFC, will be medium or may be even high also since its output is basically 2 level at a frequency of 1150 Hz.

In case of the other two configurations of UPFCs, the switching frequency of each module is 350 Hz and 450 Hz only. Since the series inverters of both these configurations are cascaded modules as discussed in earlier chapters, the effective switching frequencies for UPFC sing 3 level DC MLI and H bridge inverter based UPFCs are 1350 & 1050 Hz respectively. As this is multi level inverter output (7 levels) as ahown in Fig. 5.4, the harmonic content will be quite low when compared with 2 level wave forms. Since the switching frequency is not high, the switching losses are also very less. From the above shown Fig. 5.1, it is clear that, almost all the devices like GTO, IGBT can be used for implementing it practically.

5.1.2 Comparison on the basis of DC voltage

In the case of 2 level VSC, the DC voltage can be controlled quite precisely around its ref. set value. This is due to the fact that, in the case of two level VSC, the shunt converter (by virtue of its HCC scheme) can realize very accurately. The ref. current needed to maintain the DC voltage. As a result the ripple in the DC voltage in the case of two level VSC is quite low as evident from Fig. 5.4.

On the other hand, in the case of H bridge inverter or DC MLI the ref. current cant be tracked very accurately by the SPWM switching technique. As a result, the ripples in the DC voltage in these two types are more as compared to the case of two level VSC. The traces of the DC voltage of these two inverters are shown in Fig. 5.3.

comparision of Fig. 5.2 & 5.3 indeed reveals less ripples in the DC voltage of the two level VSC based UPFC as compared to the other two types.

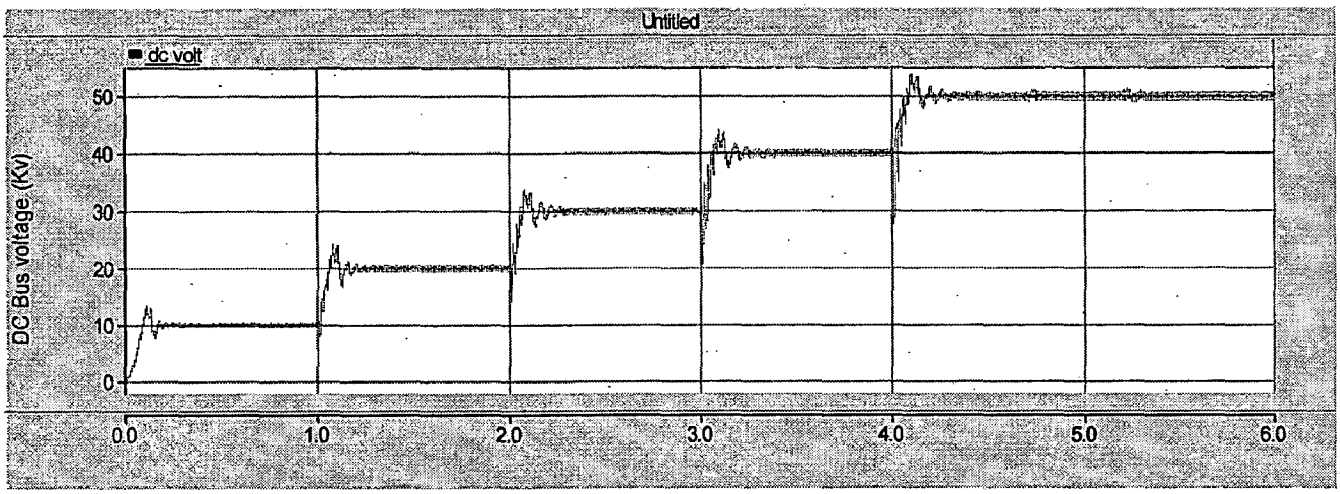
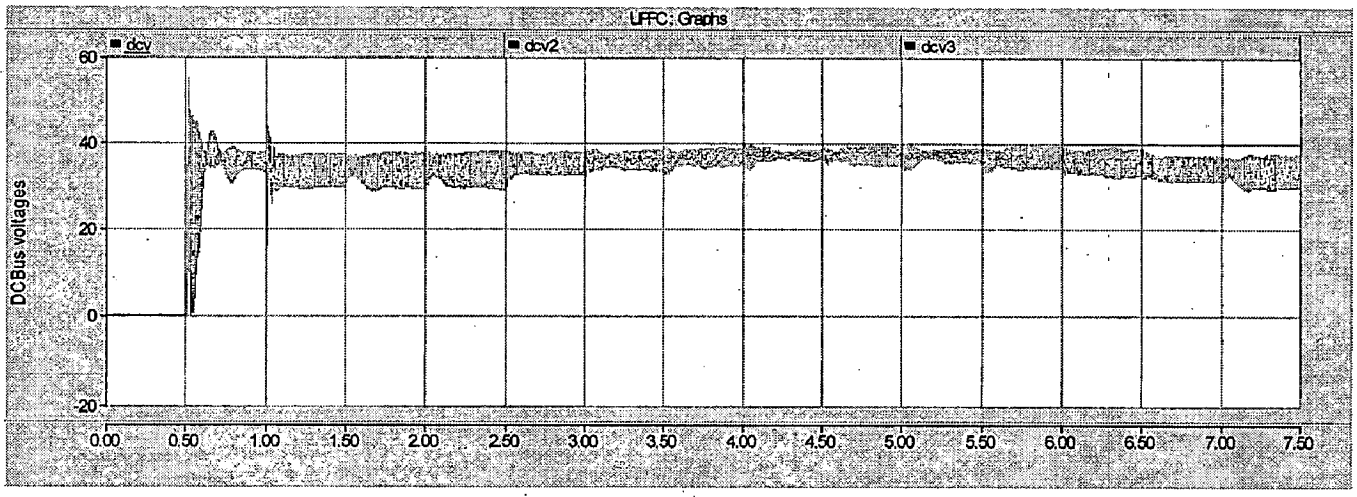


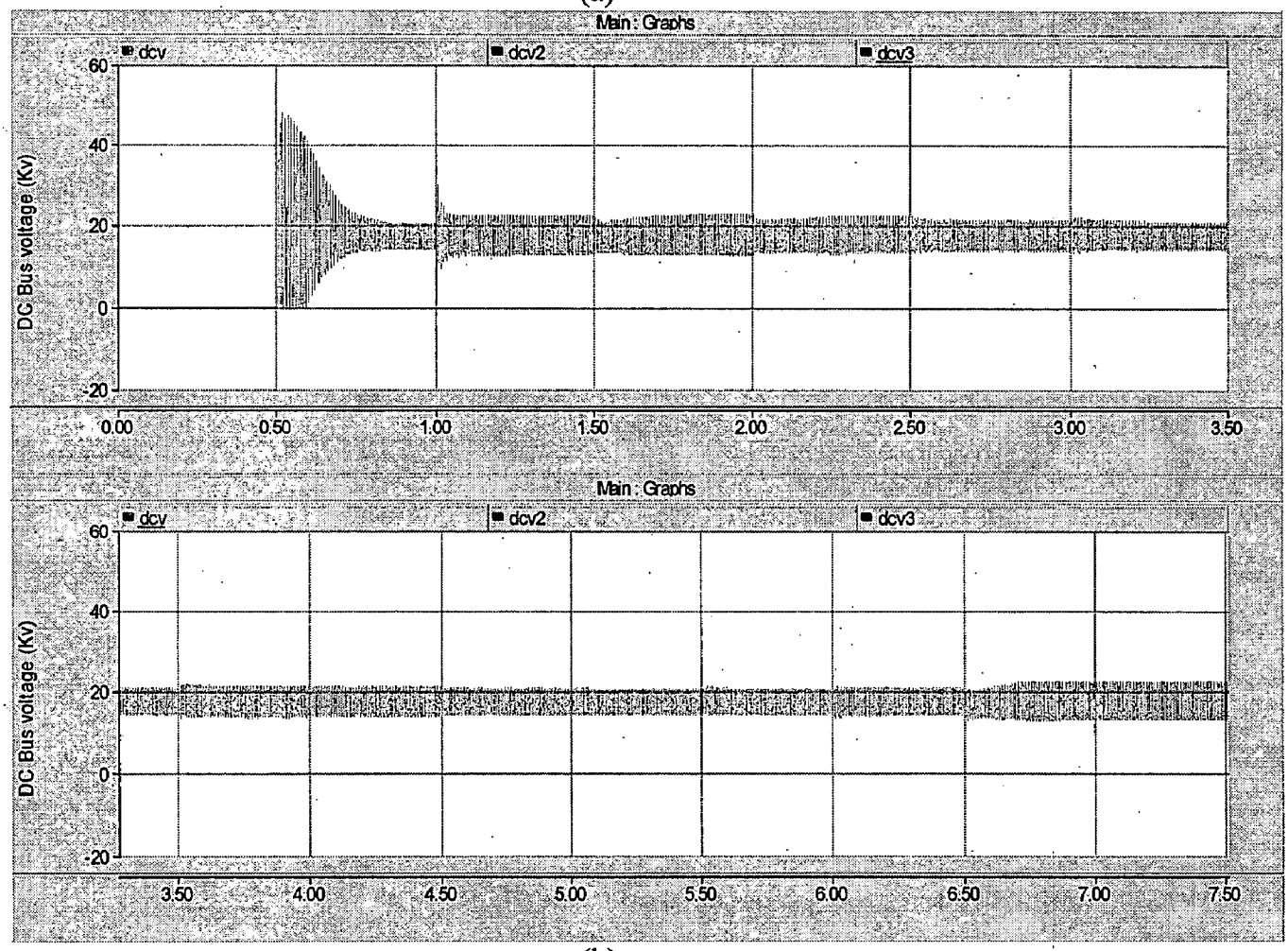
Figure 5.2: Dc Bus Voltage of UPFC using 2-level VSC

Moreover, comparing between the H bridge inverter and the DC MLI, it can be observed that, For a fixed voltage of Vdc across the DC Bus of both the modules, the AC output voltage of 3 level half bridge diode clamped inverter is half that of the AC output voltage of H bridge inverter module. Therefore, for a fixed level of series voltage injection these two UPFCs operate at different level of DC voltages. Also, for both these types of UPFCs, the DC voltage of a individual module are maintained at different levels.Thereby making the rating of the DC capacitors different. On the other hand, for two level VSC based UPFC, only one single capacitor is required, which is advantageous for practical implementation.

However it is to be noted that for properly regulating the DC voltages, detailed control system design of the UPFC based on the accurate mathematical model (of the UPFC) is needed. As the mathematical modeling of UPFC is presently out of the scope of this thesis, no systematic control system design could be attempted and therefore the DC voltage oscillations could not be reduced further.



(a)

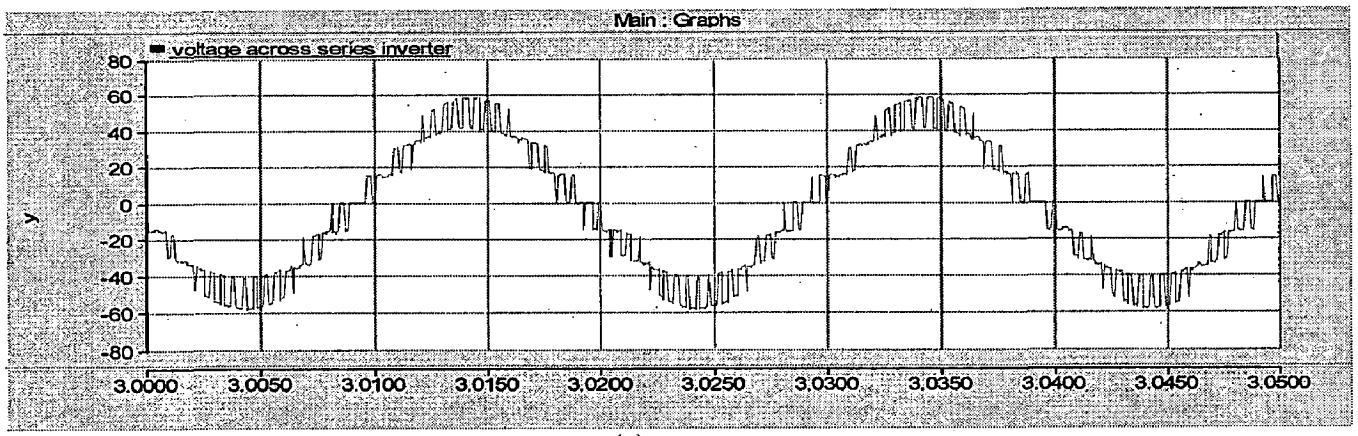


(b)

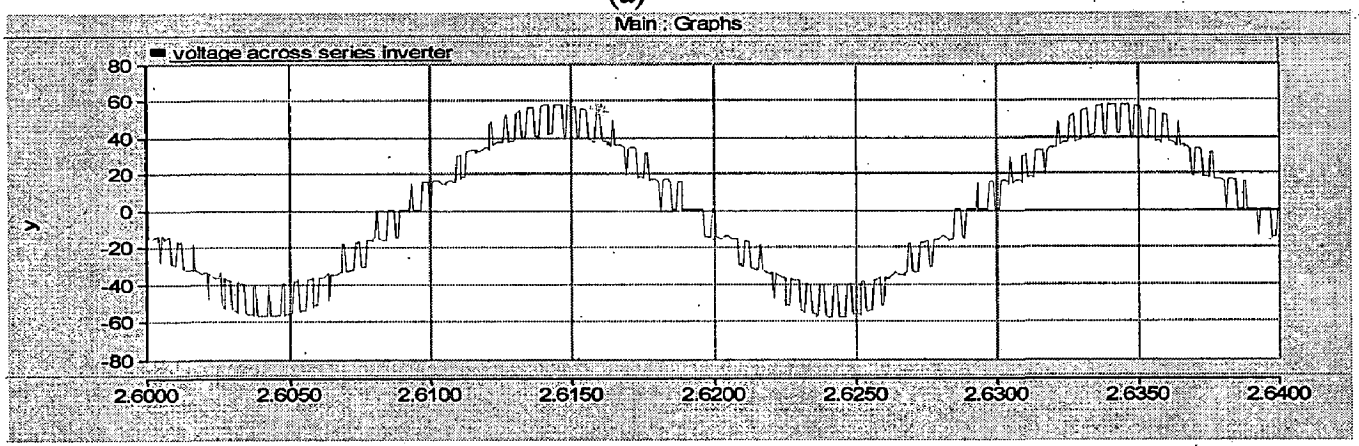
Figure 5.3: DC Bus voltage profiles (a) UPFC using 3-level half bridge DC MLI module (b)H-bridge inverter module based UPFC.

5.1.3 Discussion on Rating of the Valve

The ratings of the capacitors and also the no. of capacitors required is also high for the case of UPFC using 3 level half bridge DC MLI modules when compared with the H bridge inverter module based UPFC. The valves of both the modules have to block the same amount of voltage across them. So the voltage ratings of both the valves are almost the same. But, whereas in diode clamped multi level inverter, since all the period of conduction of all the valves is different by itself. All the valves have the different ratings. In the case of H Bridge inverter, the valves will conduct for the same period, so these valves will have the same current rating also. In case of UPFC using 2 level VSC also, all the valves will have the same ratings, since the period of conduction is also same for all the valves.



(a)



(b)

Figure 5.4: output voltage of series inverter of (a) UPFC using 3 level DC MLI (b) H bridge inverter based UPFC.

5.1.4 Based on physical structure

Comparing both the configurations based UPFCs based on physical structure; it can be concluded to use H bridge inverter module based UPFC, which is advantageous. The following table illustrates the min. no. of main components required for implementing it practically.

Component Required	Min. No Required UPFC Using 2 Level Vsc	Min. No Required For 3 Level Dc Mli Modules Based UPFC	Min. No Required For UPFC H Bridge Inverter Modules
Shunt T/F 1-ph.	3	3	3
Series T/F 1-ph.	3	0	0
Valves	12	36	36
Clamping diodes	0	18	0
DC Bus Capacitors	1	18	9

Table 5.1: comparison based on the physical structure.

As seen from the above table, the extra 18 no. of clamping diodes, and double the no. of capacitors are required for implementing using 3 level half bridge diode clamped multi level inverter modules, when it is compared with the H bridge inverter module based UPFC.

As the level no. increases for enhancing the rating of the UPFC, this no. of extra required components will also increase, which is so disadvantageous economically. And also the complexity in the circuit design will increase.

Here, it is concluded that, H Bridge based UPFC is more advantageous to implement it practically in all the aspects.

Summarizing the above discussions, the comparison has been made in a single Table as shown in Table 5.2.

Table 5.2: illustrating the complete comparison of configurations of UPFC

Parameter compared →	Switching Frequency		Harmonic Content		Possible Devices	No. of Devices		DC Voltage	Power
Configuration of UPFC ↓	**Shunt side**	**Series side**	**Shunt side**	**Series side**		**Shunt side**	**Series side**	**control**	**Rating**
2 level VSC based	High	Medium (1150 Hz.)	Low	Medium	IGBT/ MOSFET	High	Medium	Better	Low
3 level DC MLI module based	Low (350 Hz).	Medium (1350 Hz).	High	Low	GTO / IGBT	Medium	High	Less ripples	High
H bridge inverter module based	Low (450 Hz).	Medium (1050 Hz).	High	low	GTO / IGBT	Medium	high	More ripples	high

5.2 Conclusions

In this thesis, the various configurations of UPFCs have been simulated and the comparative analysis is presented. After analyzing the various configurations of UPFCs, which are discussed and simulated in the above chapters, it is concluded that, the compensation provided by the series inverter, and hence the amounts of real and reactive power supplied by the series inverter to the power system are same in both the cases by maintaining the two different DC Bus voltages by tow different configurations of the inverters.

It can also be concluded that H bridge inverter module based UPFC is advantageous from the physical structure point of view, because, extra no. of clamping diodes, and double the no. of capacitors are required for implementing UPFC using 3

level half bridge diode clamped multi level inverter modules, as compared to the H bridge inverter module based UPFC. The complexity in the design of UPFC using 3 level half bridge DC MLI is more as compared with the other configuration of UPFC. As, different ratings of the valves are required to implement it practically whereas the H bridge inverter module based UPFC requires the equal rating valves.

5.3 Future scope of work

Since only three different configurations of UPFCs have been simulated and compared, which only differs by the structure, there are lot many configurations are implemented today across the globe with different control strategies and for different applications. Some of these other configurations also can be simulated and analyzed keeping the same control strategy.

The other configurations of UPFCs which are not discussed in this thesis are,

1. UPFC using cascaded multi level inverter.
2. UPFC using multi converter operated by phase shifted triangular carrier wave
3. Flying capacitor multi level inverter based UPFC.
4. Chopper stabilized diode clamped multi level inverter based UPFC

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Appendix A

Test System

In this work, the considered test system description has presented in chapter no 1. The single line diagram of the above described system is as shown in Fig 1.8. The graphical view of the simulated system in PSCAD/EMTDC is given in Fig. A-1. The line data of the system is given in Table A-1. The load flow result presented from ref. [18] is as shown in Table A-2.

Table A-1: line data of the test system considered.

Bus No.		Series Resistance (R_s) p.u.	Series Reactance (X_s) p.u.	Shunt Susceptance (B) p.u.
From	To			
1	101	0.001	0.012	0.00
2	102	0.001	0.012	0.00
3	13	0.022	0.22	0.33
3	13	0.022	0.22	0.33
3	13	0.022	0.22	0.33
3	102	0.002	0.02	0.03
3	102	0.002	0.02	0.03
11	111	0.001	0.012	0.00
12	112	0.001	0.012	0.00
13	112	0.002	0.02	0.03
13	112	0.002	0.02	0.03
101	102	0.005	0.05	0.075
101	102	0.005	0.05	0.075
111	112	0.005	0.05	0.075
111	112	0.005	0.05	0.075

31. Pengcheng Zhu, Liming Liu, Xiaoyuan Liu, Yong Kang and Jian Chen,"**Analysis and Comparison of two Control Strategies for UPFC,**" IEEE/PES Transmission and Distribution Conference & Exhibition: Asia and Pacific Dalian, China, 2005.
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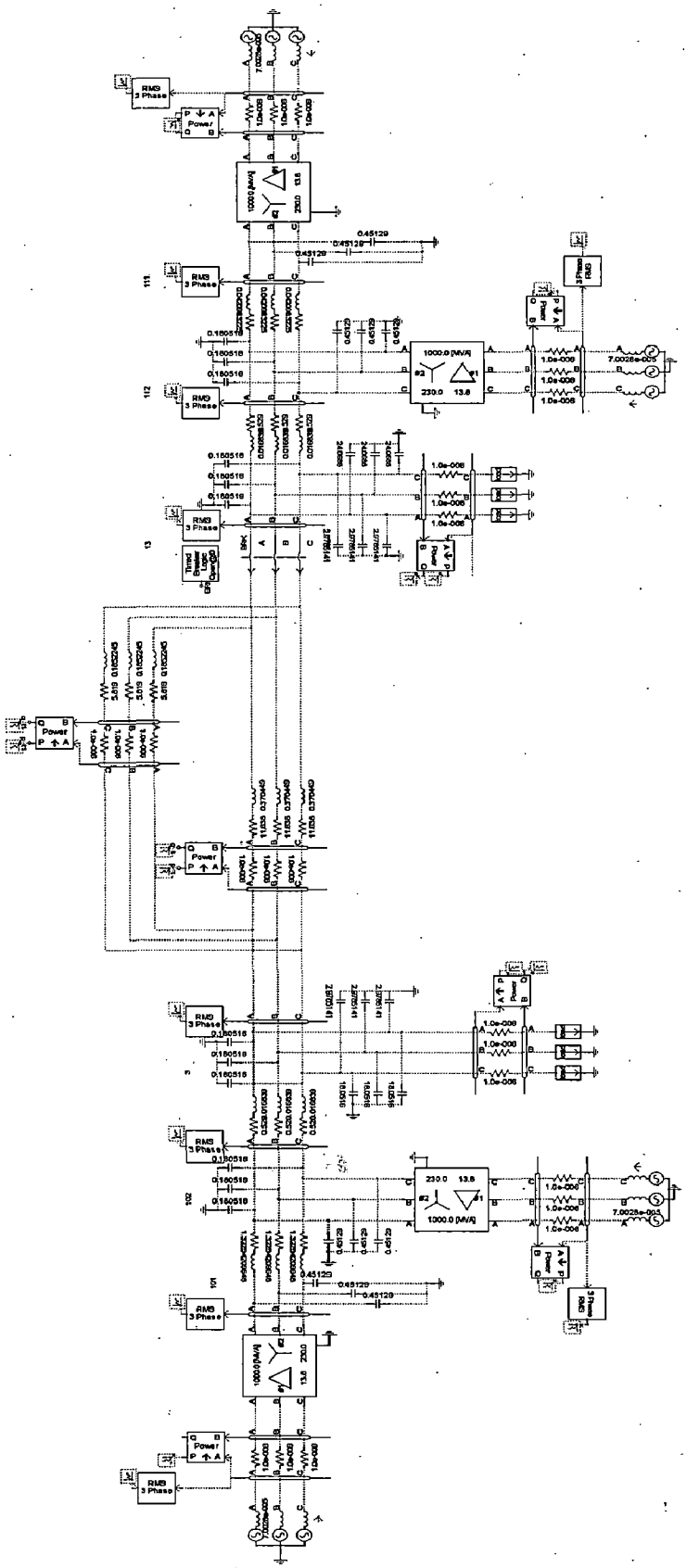


Figure A-1 PSCAD view of the simulated test system standalone

Appendix B

UPFC using basic 2 level VSC

Carrier signal in PWM module:

Frequency: 1150 Hz

Initial phase of signal: 0°

Duty cycle 50%

Max. Output: 1.0

Min. Output: -1.0

PI controller for the HCF converter:

Proportional gain 2

Integral time constant 0.01 s

Max. Limit 10

Min. limit -10

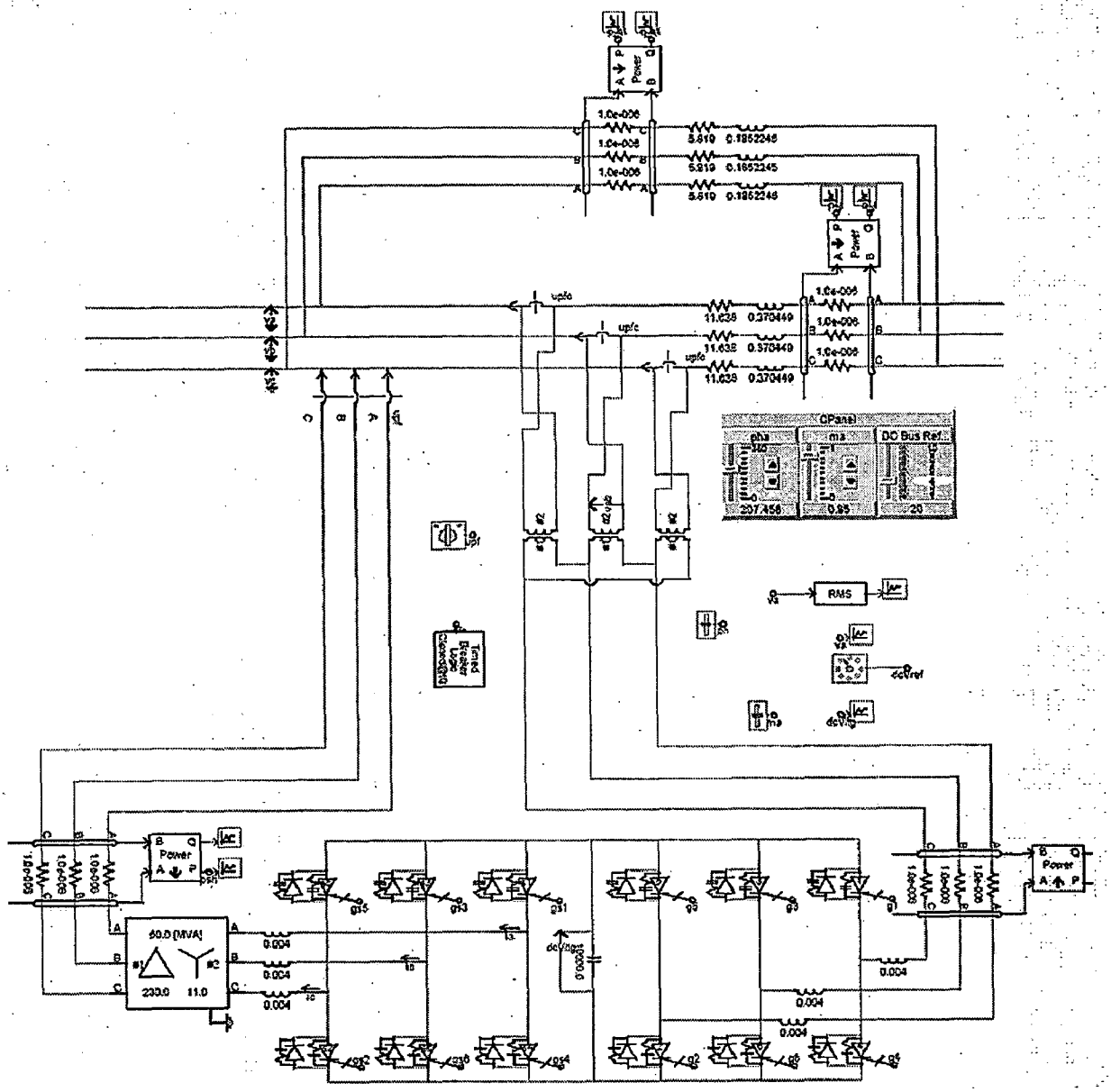


Fig B-1: Graphical view of the UPFC using 2 level VSC in PSCAD

Appendix C

UPFC using 3 level DC MLI modules.

The various parameters used for the simulation of the UPFC using 3 level DC MLI modules are given below.

Shunt inverter:

Gain of PI controller:	0.0000055
Time constant of the PI controller:	0.00000012
Proportional gain:	0.00018

For Automatic power flow control

Series inverter:

For real power control:

Gain of PI controller:	11
Time constant of the PI controller:	0.000025

For reactive power control:

Gain of PI controller:	5.5
Time constant of the PI controller:	0.000325

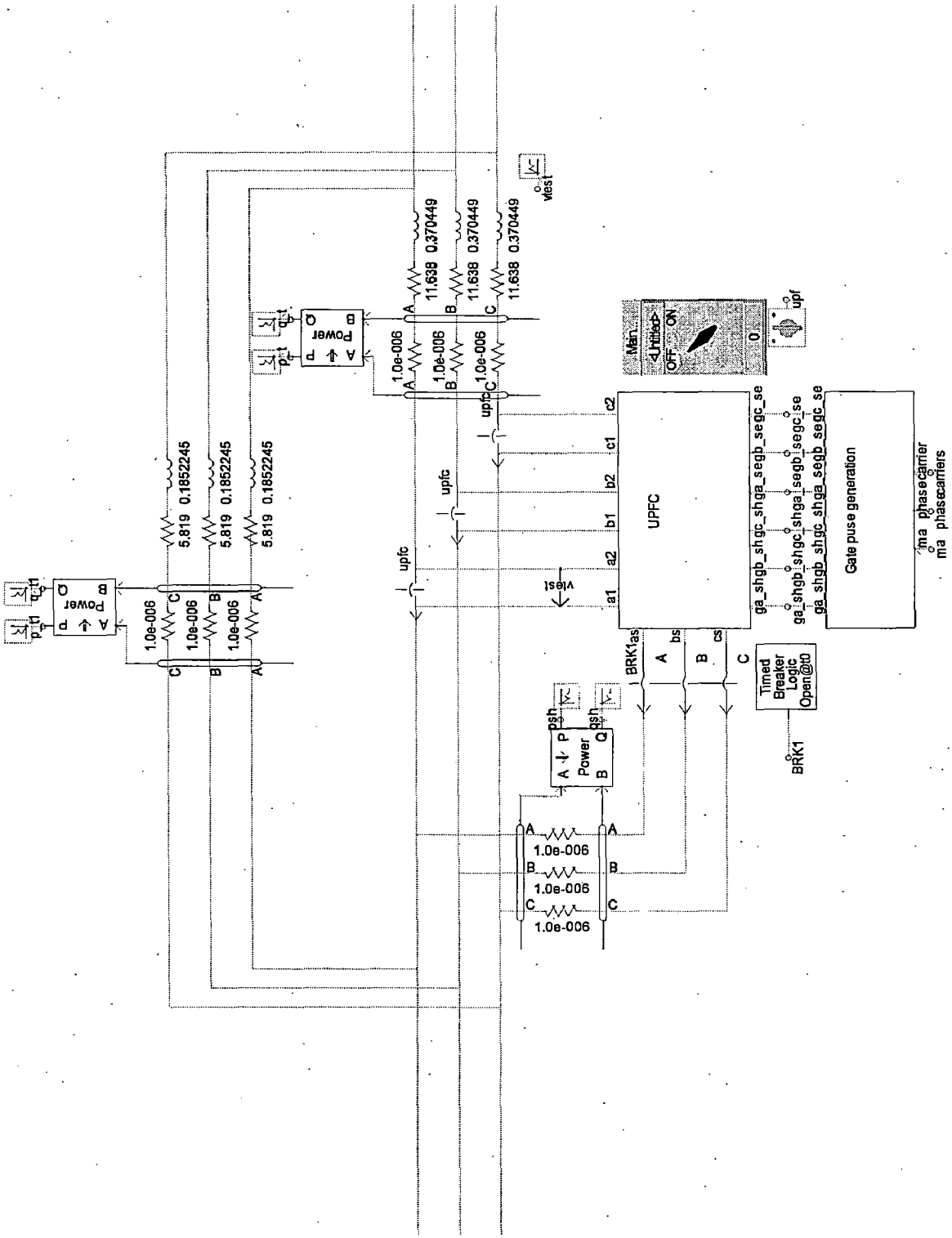


Figure C-1: Graphical view of the UPFC using DC MLI modules in PSCAD

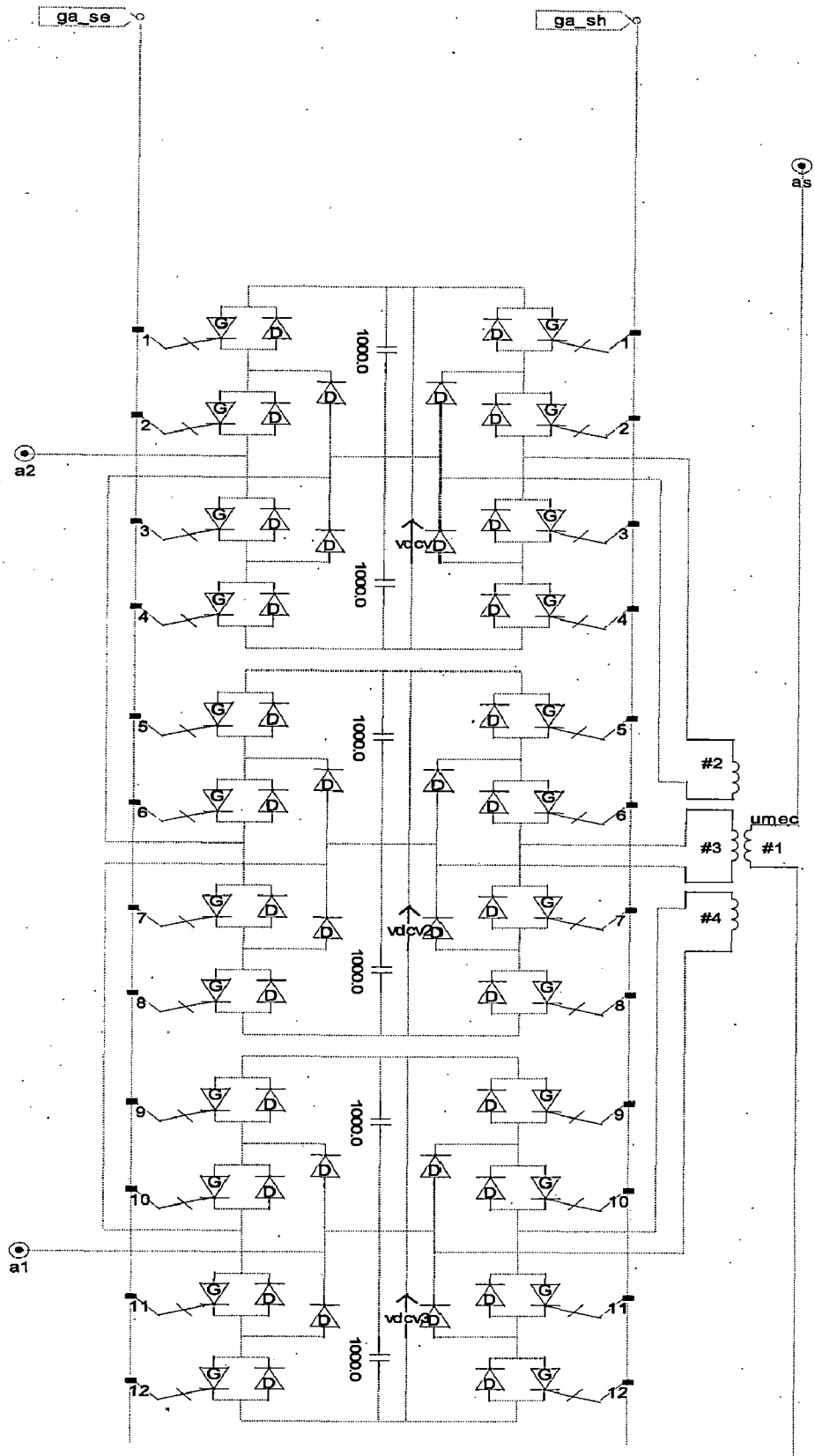


Figure C-2: Graphical view of the DC MLI inverters PSCAD

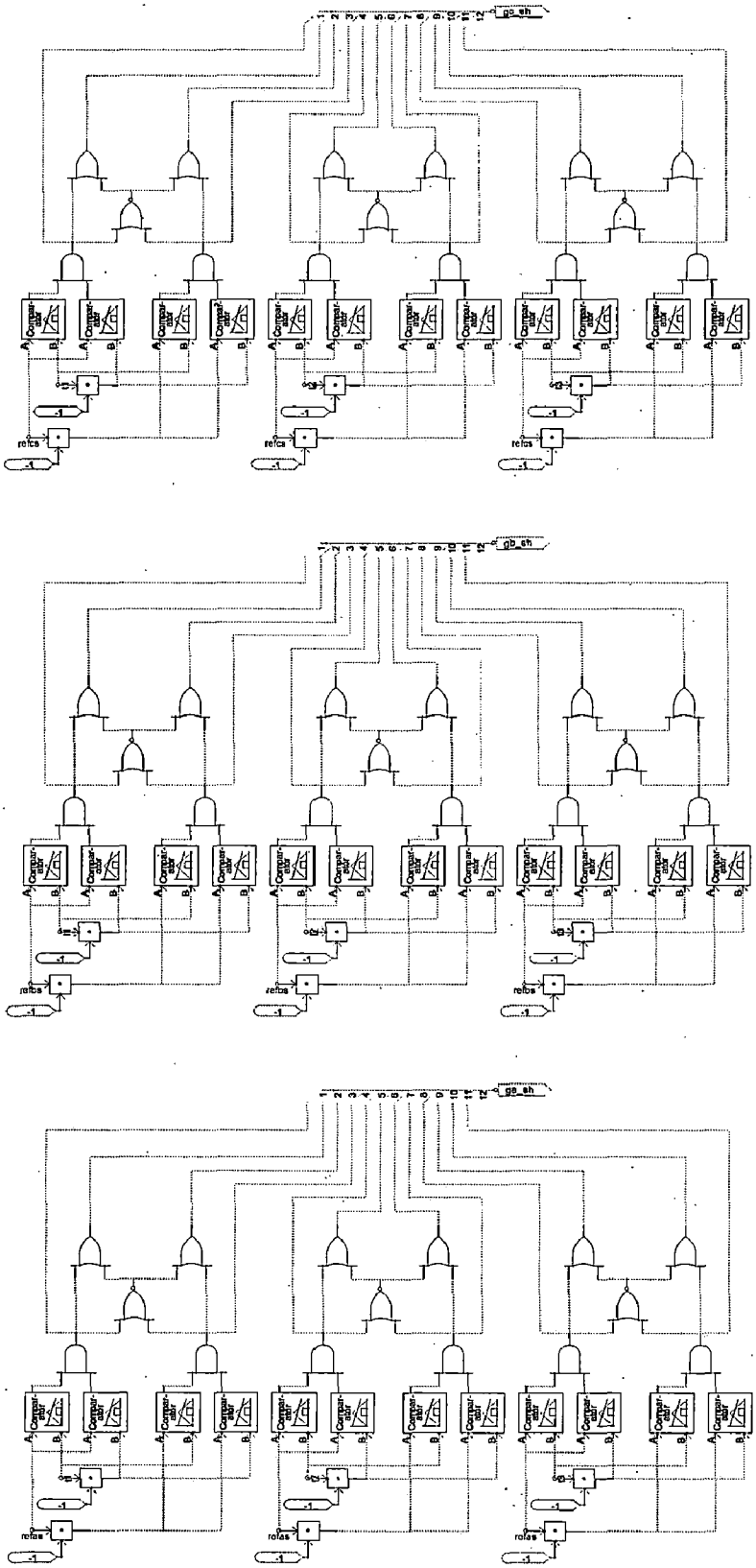


Figure C-3: Graphical view of the Gate pulse generation scheme for DC MLI.

Appendix D

H bridge inverter module based UPFC

The various parameters used for the simulation of the H bridge inverter module based UPFC are given below.

Shunt inverter:

Gain of PI controller:	0.0000025
Time constant of the PI controller:	0.00000075
Proportional gain:	0.00055

For Automatic power flow control

Series inverter:

For real power control:

Gain of PI controller:	10
Time constant of the PI controller:	0.000035

For reactive power control:

Gain of PI controller:	6
Time constant of the PI controller:	0.00045

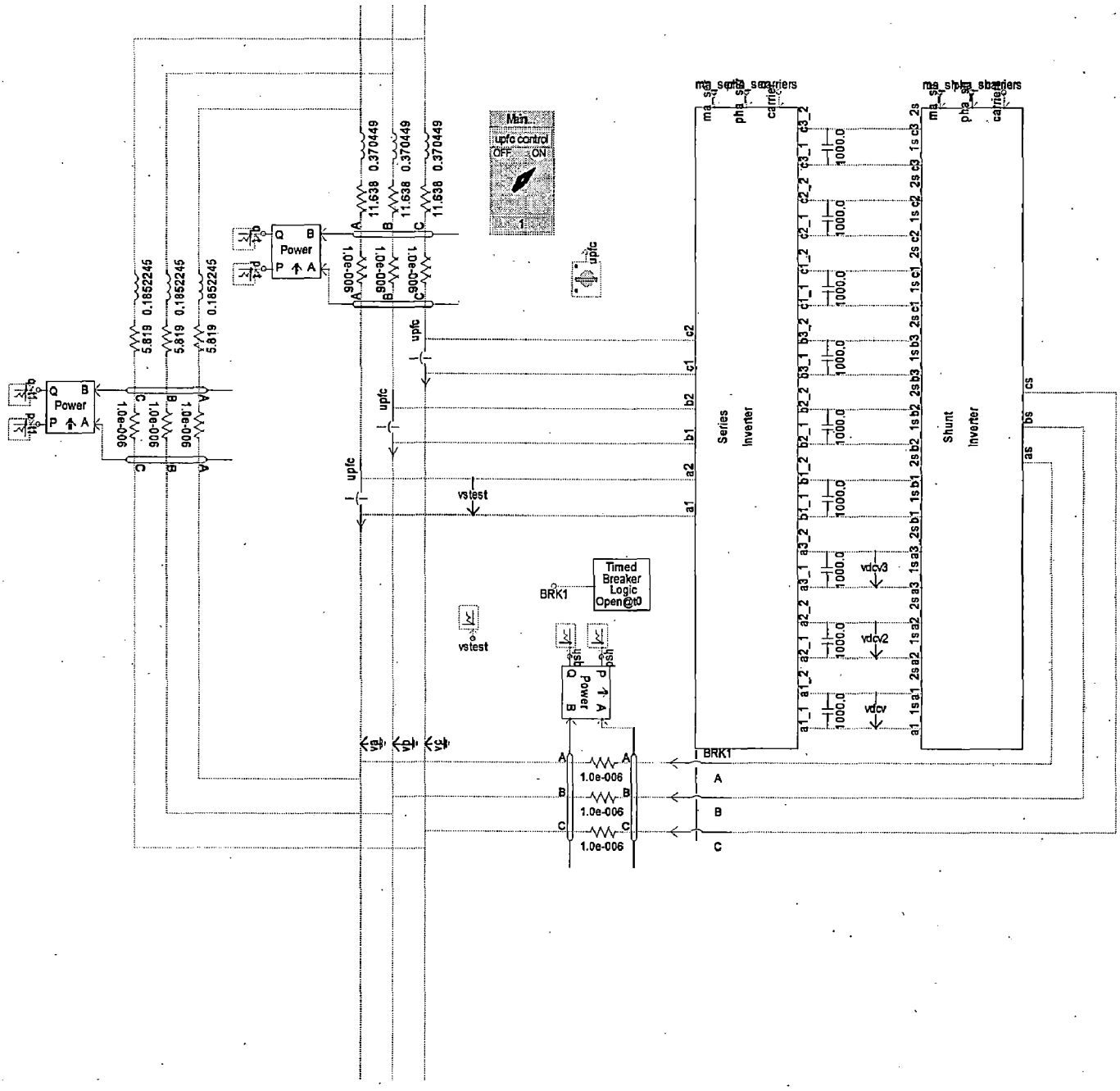
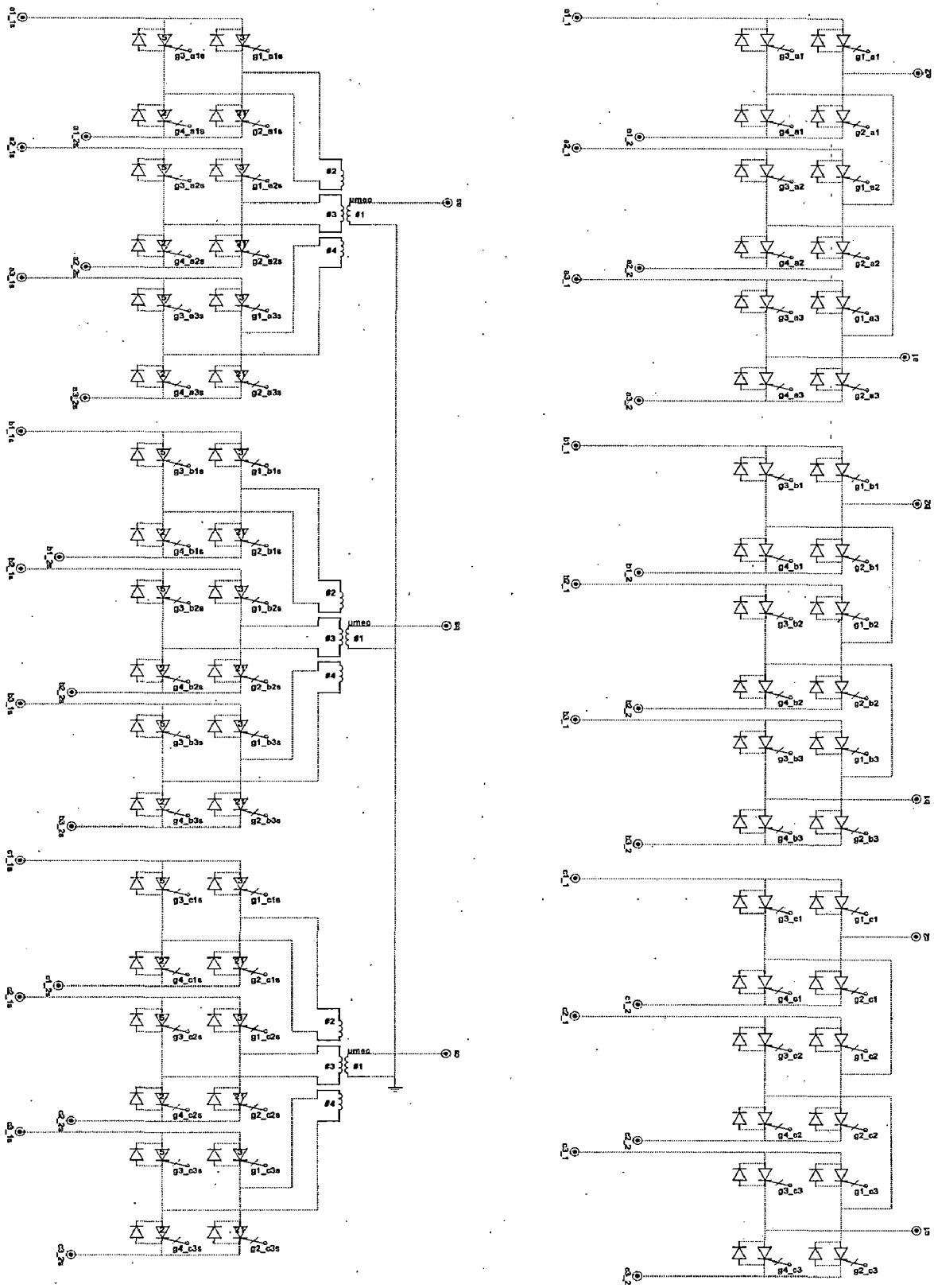


Figure D-1: Graphical view of the H bridge module based UPFC model in PSCAD



(a) (b)

Figure D-2: Graphical view of the H bridge inverters PSCAD (a) Shunt inverter (b) Series inverter

Appendix A

Test System

In this work, the considered test system description has presented in chapter no 1. The single line diagram of the above described system is as shown in Fig 1.8. The graphical view of the simulated system in PSCAD/EMTDC is given in Fig. A-1. The line data of the system is given in Table A-1. The load flow result presented from ref. [18] is as shown in Table A-2.

Table A-1: line data of the test system considered.

Bus No.		Series Resistance (R_s) p.u.	Series Reactance (X_s) p.u.	Shunt Susceptance (B) p.u.
From	To			
1	101	0.001	0.012	0.00
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3	13	0.022	0.22	0.33
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3	102	0.002	0.02	0.03
3	102	0.002	0.02	0.03
11	111	0.001	0.012	0.00
12	112	0.001	0.012	0.00
13	112	0.002	0.02	0.03
13	112	0.002	0.02	0.03
101	102	0.005	0.05	0.075
101	102	0.005	0.05	0.075
111	112	0.005	0.05	0.075
111	112	0.005	0.05	0.075

Table A-2: load flow result of the test system considered.

Bus No.	Voltage mag. (pu)	Angle (deg)	Real power gen. (pu)	Reactive power gen. (pu)	Real power load (pu)	Reactive power load (pu)	Shunt susceptance (pu)
1	1.03	8.2154	7.0	1.3386	0.0	0.0	0.0
2	1.01	-1.5040	7.0	1.5920	0.0	0.0	0.0
11	1.03	0	7.2172	1.4466	0.0	0.0	0.0
12	1.01	-10.2051	7.0	1.8083	0.0	0.0	0.0
101	1.0108	3.6615	0.0	0.0	0.0	0.0	0.0
102	0.9875	-6.2433	0.0	0.0	0.0	0.0	0.0
111	1.0095	-4.6977	0.0	0.0	0.0	0.0	0.0
112	0.9850	-14.9443	0.0	0.0	0.0	0.0	0.0
3	0.9761	-14.4194	0.0	0.0	11.59	2.12	3.0
13	0.9716	-23.2922	0.0	0.0	15.75	2.88	4.0

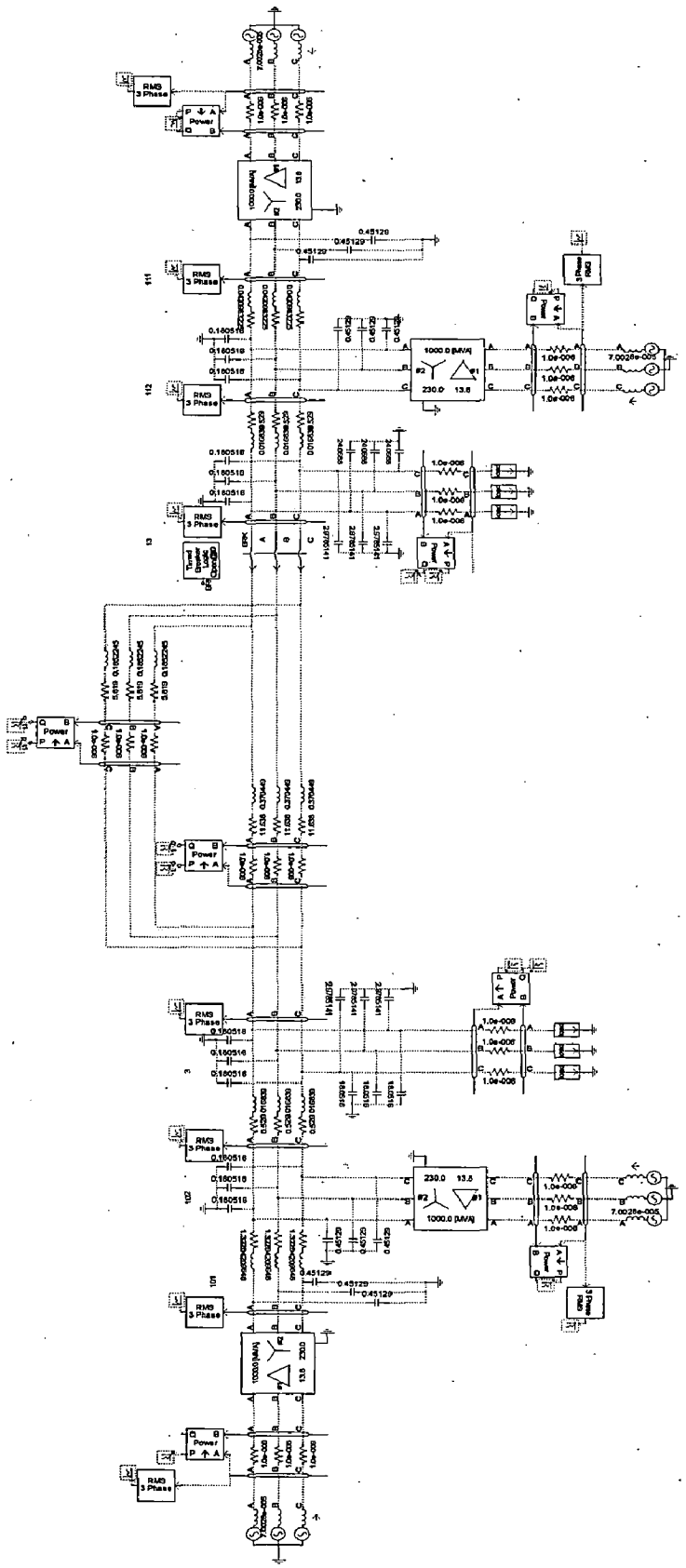


Figure A-1 PSCAD view of the simulated test system standalone

Appendix B

UPFC using basic 2 level VSC

Carrier signal in PWM module:

Frequency: 1150 Hz
Initial phase of signal: 0°
Duty cycle 50%
Max. Output: 1.0
Min. Output: -1.0

PI controller for the HCF converter:

Proportional gain 2
Integral time constant 0.01 s
Max. Limit 10
Min. limit -10

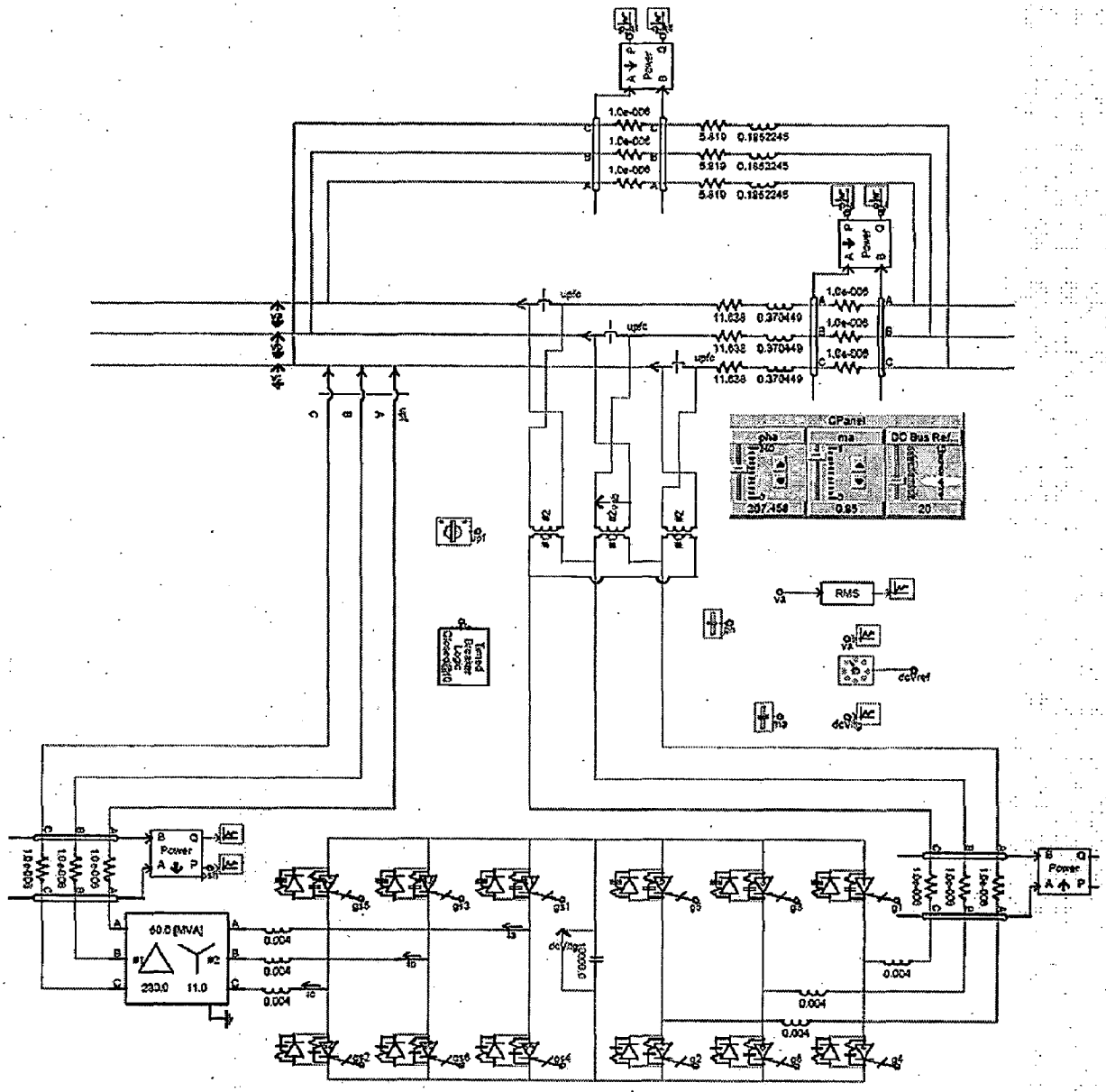


Fig B-1: Graphical view of the UPFC using 2 level VSC in PSCAD

Appendix C

UPFC using 3 level DC MLI modules.

The various parameters used for the simulation of the UPFC using 3 level DC MLI modules are given below.

Shunt inverter:

Gain of PI controller:	0.0000055
Time constant of the PI controller:	0.00000012
Proportional gain:	0.00018

For Automatic power flow control

Series inverter:

For real power control:

Gain of PI controller:	11
Time constant of the PI controller:	0.000025

For reactive power control:

Gain of PI controller:	5.5
Time constant of the PI controller:	0.000325

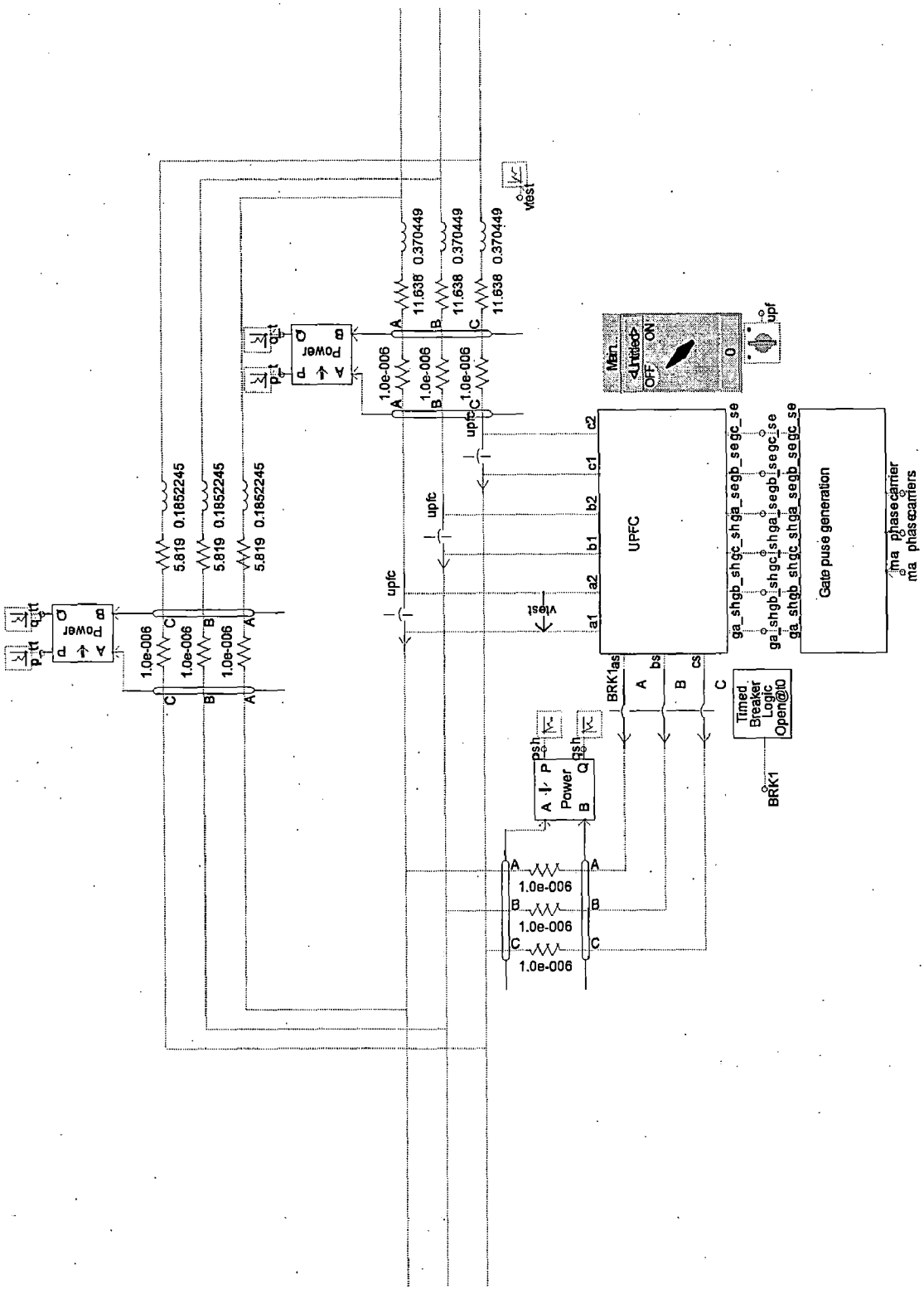


Figure C-1: Graphical view of the UPFC using DC MLI modules in PSCAD

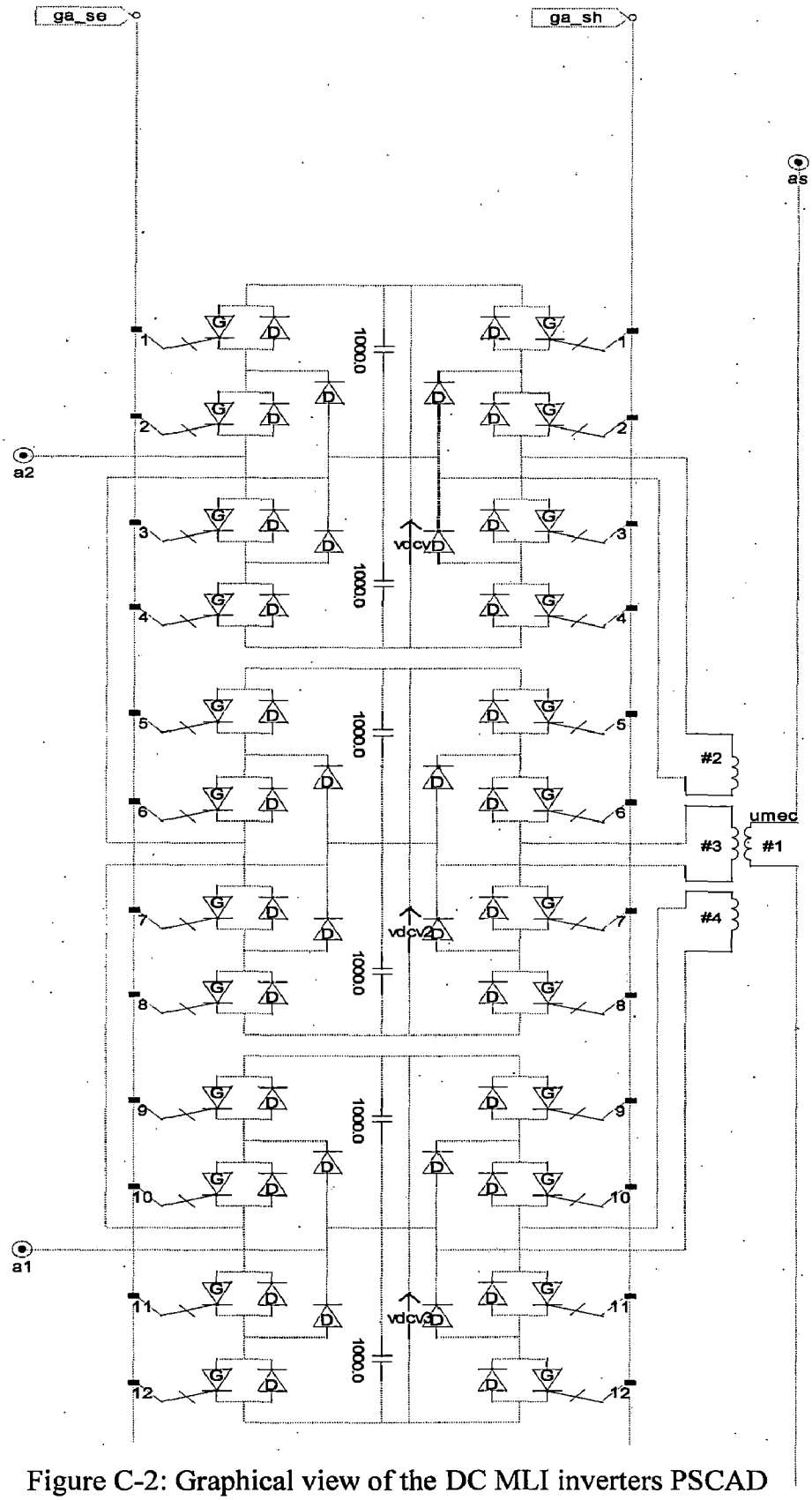


Figure C-2: Graphical view of the DC MLI inverters PSCAD

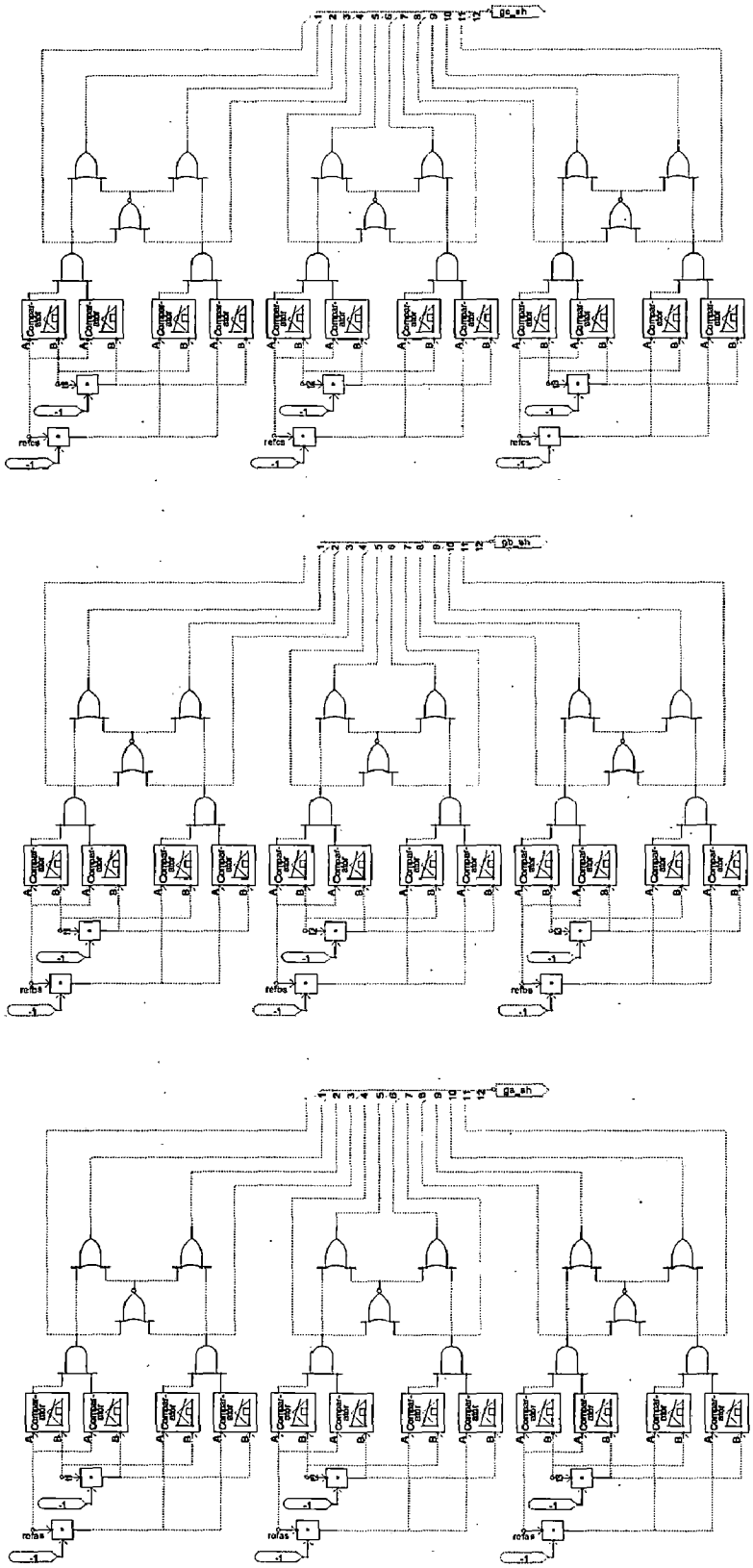


Figure C-3: Graphical view of the Gate pulse generation scheme for DC MLI.

Appendix D

H bridge inverter module based UPFC

The various parameters used for the simulation of the H bridge inverter module based UPFC are given below.

Shunt inverter:

Gain of PI controller:	0.0000025
Time constant of the PI controller:	0.00000075
Proportional gain:	0.00055

For Automatic power flow control

Series inverter:

For real power control:

Gain of PI controller:	10
Time constant of the PI controller:	0.000035

For reactive power control:

Gain of PI controller:	6
Time constant of the PI controller:	0.00045

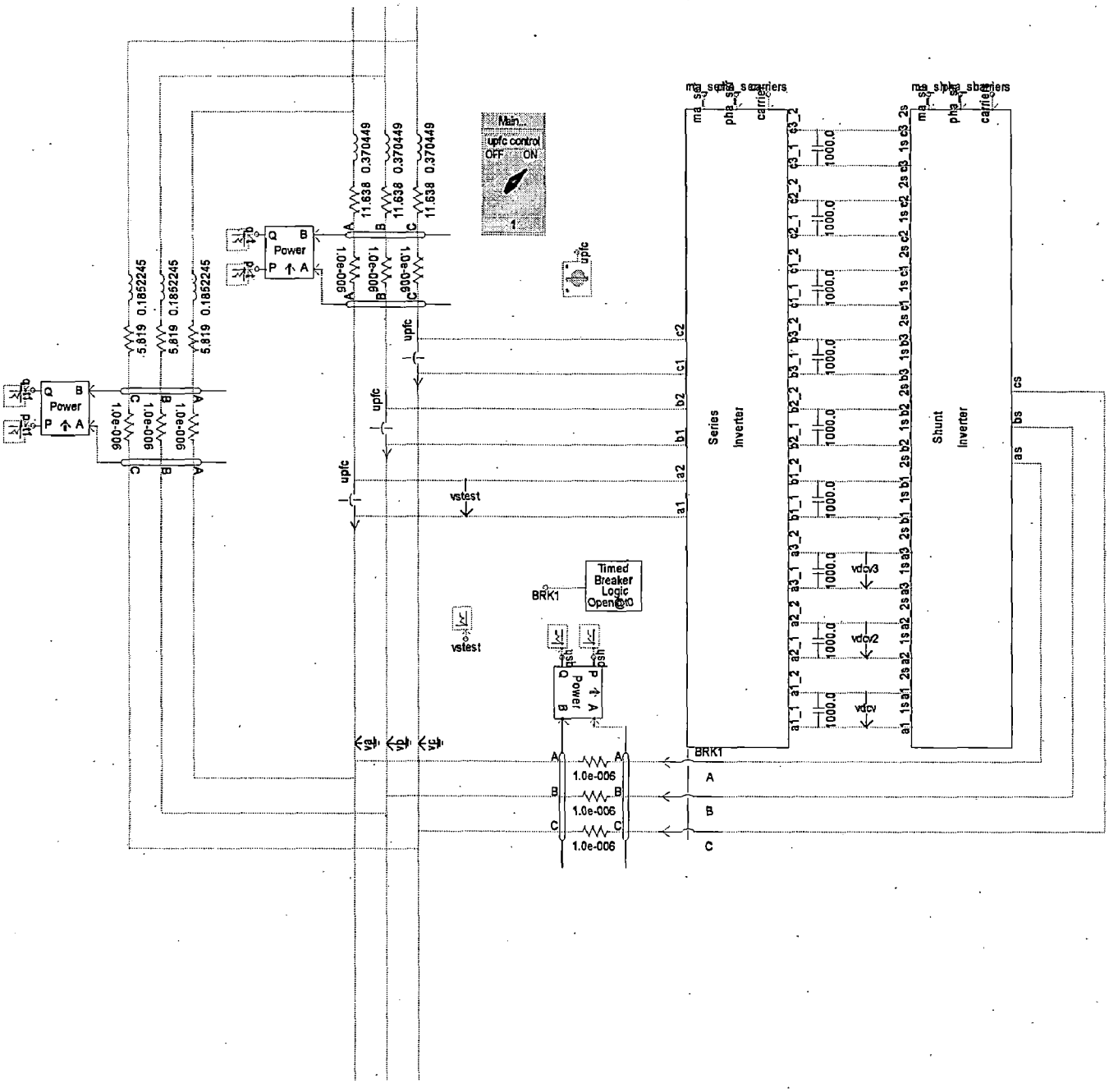
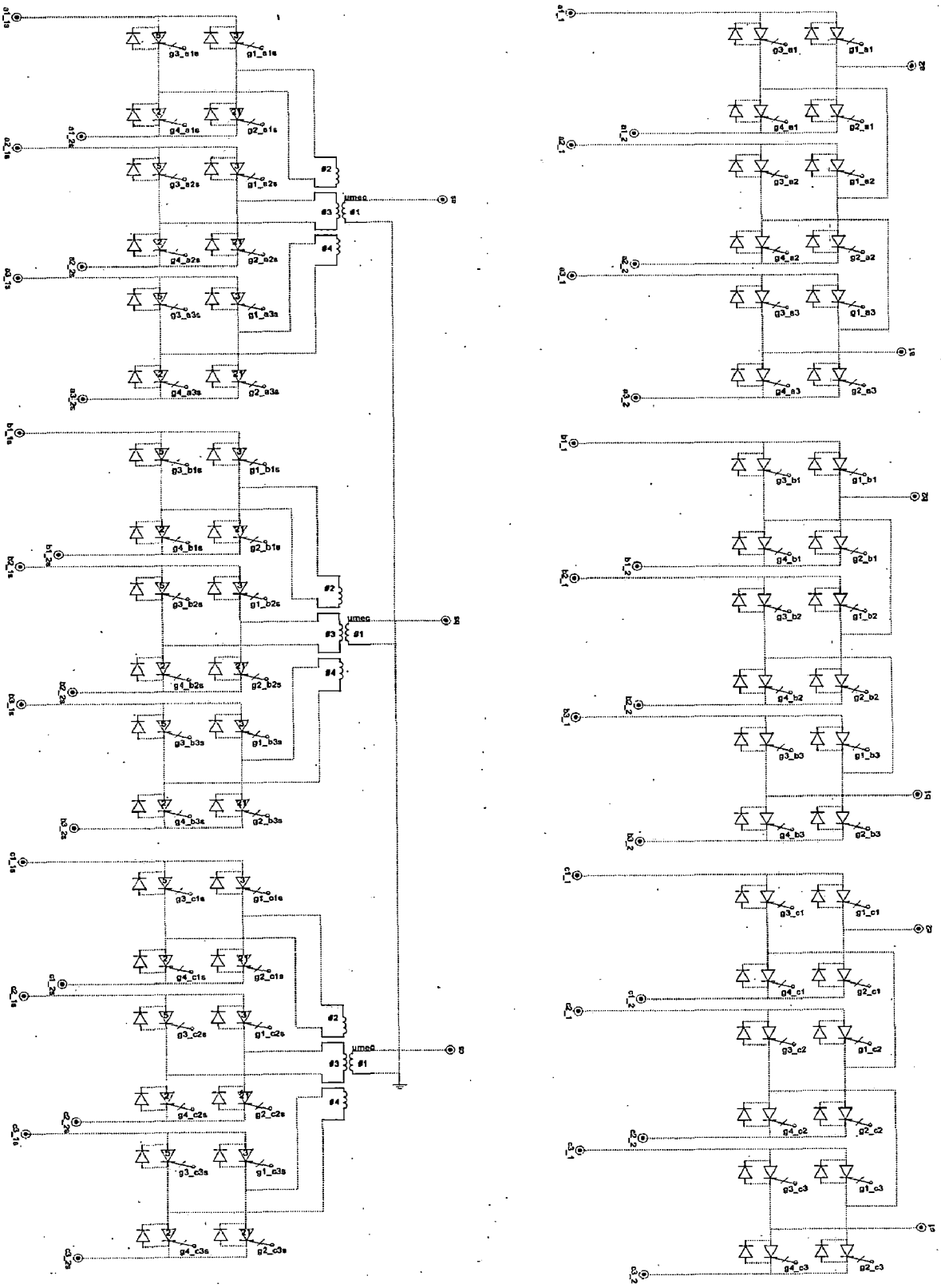


Figure D-1: Graphical view of the H bridge module based UPFC model in PSCAD



(a) (b)

Figure D-2: Graphical view of the H bridge inverters PSCAD (a) Shunt inverter (b) Series inverter