PERFORMANCE INVESTIGATIONS OF STATIC COMPENSATOR USING MULTI LEVEL INVERTER

A DISSERTATION

Submitted in partial fulfillment of the requirements for the award of the degree of

MASTER OF TECHNOLOGY

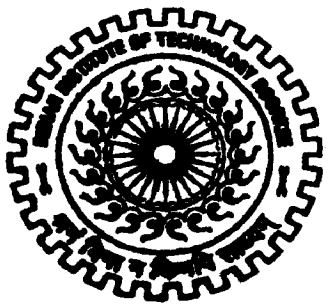
in

ELECTRICAL ENGINEERING

(With Specialization in Power Apparatus and Electric Drives)

By

KORADA THAMMAYYA BABU



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CANDIDATE'S DECLARATION

I hereby declare that the work that is being presented in this dissertation report entitled **"PERFORMANCE INESTIGATIONS OF STATIC COMPENSATOR USING MULTI-LEVEL INVERTER"** submitted in partial fulfillment of the requirements for the award of the degree of **Master Of Technology** with specialization in **Power Apparatus and Electric Drives,** to the **Department Of Electrical Engineering, Indian Institute Of Technology, Roorkee**, is an authentic record of my own work carried out, under the guidance of **Dr. Pramod Agrawal**, Professor, Department of Electrical Engineering.

The matter embodied in this dissertation report has not been submitted by me for the Award of any other degree or diploma.

Date: 29/06/2007
Place: Roorkee

K. Thammayya Babu
(KORADA THAMMAYYA BABU)

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

Date:
Place: Roorkee

(DR. PRAMOD AGRAWAL)
Professor,
Department of Electrical Engineering,
Indian Institute of Technology,
ROORKEE – 247 667,
INDIA.

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(Korada Thammayya babu)

ABSTRACT

Reactive power compensation is necessary in order to increase the power utilization and transmission capability of the power system. This also increases the power quality. Due to the advances in power electronics, the conventional compensators are replaced by static compensators such as STATCOM, TCS, TCR, DVR etc.

The trend to minimize harmonics in conventional 2-level voltage source inverter (VSI) is to use various PWM techniques. However, this has some problems, like generating a common mode voltage, increase of switching frequency and increase of the switching losses which becomes significant at high power levels. Multilevel power converters have gained much attention in recent years due to the significant problems that are shown above. The general structure of the multilevel inverter is such as to synthesize a sinusoidal voltage from several levels of DC voltage. Increasing the number of levels produce a fine staircase waveform approaching close to a sinusoidal wave with minimum harmonic distortion.

In this thesis, simulation of 3-Level inverter is carried and the performance of the inverter is investigated for two different PWM techniques. The performance of STATCOM using 3-level neutral point clamed GTO inverter is done for different loading conditions. The system is analyzed using MATLAB through a set of simulations, to determine the effect of the DC-link capacitors. The control of the system is carried out using the implementation of a PI regulator. And the system performance is compared with different regulators like fuzzy and fuzzy pre compensated PI regulators.

CONTENTS

CHAPTER - I

INTRODUCTION

1.1 GENERAL:

Reactive power is recognized as a significant factor in the design and operation of alternating current electric power systems from long time. The transmission of active power requires a difference in angular phase between voltages at the sending and receive points, where as the transmission of reactive power require a difference in magnitude of these voltages.

The aspects of reactive power have recently acquired increased importance for at least two reasons. First, the increasing pressures to utilize transmission capacity as much as possible. Second, the development of new static type of controllable reactive power compensators. Earlier, Shunt capacitors were installed in distributed circuits to improve voltage profile and to reduce line loading and losses by power factor improvement.

1.2 REACTIVE POWER COMPENSATION:

The problem of reactive power compensation is viewed from two aspects: load compensation and voltage support. In load compensation, the objectives are to increase the value of the system power factor, to balance the real power drawn from the ac supply, compensate voltage regulation and to eliminate current harmonic components produced by large and fluctuating nonlinear industrial loads. Voltage support is required to reduce voltage fluctuation at a given terminal of a transmission line. Reactive power compensation in transmission systems also improves the stability of the ac system by increasing the maximum active power that can be transmitted. It also helps to maintain a substantially flat voltage profile at all levels of power transmission. It improves HVDC (High Voltage Direct Current) conversion terminal performance, increases transmission efficiency, controls steady-state and temporary over voltages, and can avoid disastrous blackouts.

Based on the use of reliable high-speed power electronics, powerful analytical tools, advanced control and microcomputer technologies, Flexible AC Transmission Systems,

(FACTS) have been developed and they represent a new concept for the operation of power transmission systems. In these systems, the use of static VAR compensators with fast response times play an important role, allowing to increase the amount of apparent power transfer through an existing line, close to its thermal capacity, without compromising its stability limits. These opportunities arise through the ability of special static VAR compensators to adjust the inter-related parameters that govern the operation of transmission systems.

1.3 MULTI LEVEL INVERTER FOR REACTIVE POWER COMPENSATION:

Multi level inverters are recently researched and presented for the high power and medium voltage applications, such as static var compensator, active power filter, and motor drives due to their ability to obtain waveforms with better harmonic spectrum and attain higher voltages with a lower maximum device rating.

The advantages of multilevel inverters are:

1. Low voltage stress of power semiconductors;
2. Less current or voltage harmonics; and
3. Less electromagnetic interference.

Neutral point clamped (NPC) topologies were proposed and successfully used in the high power motor drive and utility applications. The disadvantages of the NPC inverters are

1. Many power semiconductors used in the circuits
2. Complex control scheme.
3. The cost of the multilevel converters is also expensive.

Three-level neutral-point-clamped rectifiers are proposed to draw the sinusoidal line currents in phase with mains voltages. The input power factor is unity. However, twelve power switches and six clamped diodes are required in the rectifier. The control scheme is also very complicated. The low cost inverter with less power switches and small size are usually welcome in the industrial applications.

Reactive power compensation is one of the most important actions for control of power systems on transmission and distribution level. It allows better stability of overall

system, decreases losses and permits to maintain better voltage profile. The compensated power system is less prone to failure than a non compensated one. For last 10 years, there have been tendencies to replace the traditional compensators with FACTS devices that are based on power converters. The shunt capacitors and inductances can be replaced with STATCOM and series capacitors with SSSC (Series Static Synchronies Compensator). These devices have advantages of fast response and they need a considerably smaller amount of real estate for their installation. Their main drawbacks are switching and conduction losses. Moreover, voltage rating of switching devices is not high enough. The switches of choice for high voltage applications are GTOs and their voltage rating is about 6000 V till now. To increase the voltage rating of the power converter and so of the overall FACTS controllers, different multilevel topologies have been proposed

Diode clamped VSI is another topology of MLI. The main advantages of diode clamped VSI when applied as STATCOM over its six pulses counter part is in fact that by increasing number of levels the voltage rating of inverter is increased and at the same time the total harmonic distortion (THD) of the inverter output voltage is decreased while fundamental frequency modulation (FFM) switching strategy is used.

Harmonics are one of the major concerns in most FACTS devices currently being developed to enhance existing AC transmission networks. A static synchronous compensator (STATCOM) has ideally converted its DC side voltage into a 3-phase sinusoidal ac voltage in phase with the system voltage to provide an exchange of reactive power. A coupling inductance is required between the system and the STATCOM. Because of the high power rating, the semiconductor switching frequency in the inverter needs to be well below 1kHz and hence low order harmonics will be generated.

1.4 Organization of the Report:

Chapter–II: This chapter focuses on the reactive power compensation basic principles, with shunt and series compensation. Different topologies used for reactive power compensation like thyristorized VAR compensators, self commutated VAR compensators and new VAR compensators are discussed. The advantages and disadvantages of each topology and the salient features of each topology are discussed.

Chapter–III: This chapter focuses on the basic principle of obtaining a multilevel waveform, different topologies and classification of multi-level inverters, which includes some of the recently developed circuit topologies. The salient features of each topology are presented and some modulation techniques are discussed with simulation results.

Chapter–IV: This chapter focuses on the total overview of STATCOM using three level inverter with basic operating principle of STATCOM system. The closed loop operation of STATCOM system with different controllers like PI, FUZZY, Fuzzy Pre Compensated are discussed briefly.

Chapter–V: This chapter consists of simulation results of STATCOM system. The waveform results with MATLAB 7.0.1 are presented. Reactive power plot of source which is compensated by STATCOM is presented for different loading conditions. The change of dc link capacitor voltage, change of phase angle between source voltage and current wave forms in transient state for different loading conditions are presented. Three-Level Inverter output line to line voltage is compared with 3-phase source voltage.

CHAPTER - II

REACTIVE POWER COMPENSATION TECHNIQUES

This chapter focuses on the reactive power compensation principles, different topologies used for reactive power compensation and the advantages and disadvantages of each topology briefly. The salient features of each topology are presented.

2.1 INTRODUCTION:

VAR compensation is defined as the management of reactive power to improve the performance of ac power systems. In wide field of both system and customer problems, especially related with power quality issues the concept of VAR compensation embraces, since most of power quality problems can be eliminated or solved with an appropriate control of reactive power [16].

The problem of reactive power compensation can be viewed from two aspects

- Load compensation
- Voltage support.

In load compensation the main objectives to increase the value of the system power factor, to balance the real power drawn from the ac supply, to compensate voltage regulation and to eliminate current harmonic components produced by large and fluctuating nonlinear industrial loads. Voltage support is generally required to reduce voltage fluctuation at a given terminal of a transmission line [16][17].

Series and shunt VAR compensators are used to modify the natural electrical characteristics of ac power systems. Series compensation modifies the transmission or distribution system parameters, while shunt compensation changes the equivalent impedance of the load. In both cases, the reactive power that flows through the system is effectively controlled and the performance of the overall ac power system can be improved.

Advantages of Reactive power compensation:

- Reactive power compensation in transmission systems improves the stability of the ac system by increasing the maximum active power that can be transmitted.

- It helps to maintain a flat voltage profile at all levels of power transmission,
- It improves HVDC (High Voltage Direct Current) conversion terminal performance, increases transmission efficiency,
- Controls steady-state and temporary overvoltages

2.2 REACTIVE POWER COMPENSATION PRINCIPLES:

In a linear circuit, the reactive power is defined as the ac component of the instantaneous power, with a frequency equal to 100 / 120 Hz in a 50 or 60 Hz system. The reactive power generated by the ac power source is stored in a capacitor or a reactor during a quarter of a cycle, and in the next quarter cycle is sent back to the power source. In other words, the reactive power oscillates between the ac source and the capacitor or reactor, and also between them, at a frequency equals to two times the rated value (50 or 60 Hz). For this reason, it can be compensated using VAR generators, avoiding its circulation between the load (inductive or capacitive) and the source, and therefore improving voltage stability of the power system. Reactive power compensation can be implemented with VAR generators connected in parallel or in series.

2.2.1. Shunt Compensation.

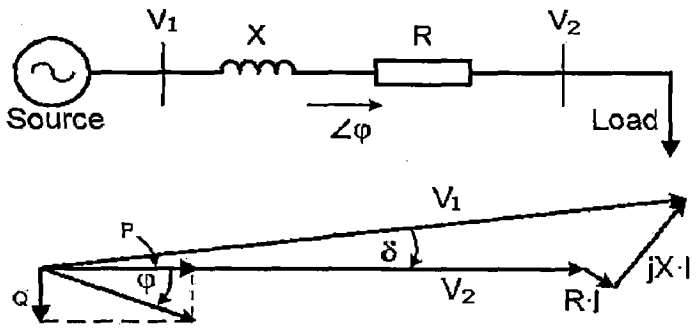
Shunt reactive power compensation in a basic ac system is shown in Figure2.1, which comprises a source V1, a power line and a typical inductive load. Figure (2.1-a) shows the system without compensation, and its related phasor diagram. In the phasor diagram, the phase angle of the current is related to the load side, which means that the active current Ip is in phase with the load voltage V2. Since the load is assumed inductive, it requires reactive power for proper operation and hence, the source must supply it, and increases the current from the generator and through power lines.

If reactive power is supplied near the load, the line current can be reduced, reducing power losses and improving voltage regulation at the load terminals. This can be done in three ways

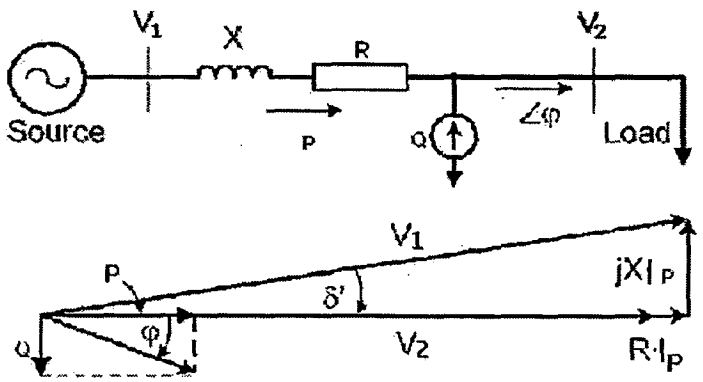
- With a capacitor.
- With a voltage source.

➢ With a current source.

In figure(2.1-b) a current source device is being used to compensate the reactive component of the load current (IQ). As a result, the system voltage regulation is improved and the reactive current component from the source is reduced or almost eliminated.



(a)



(b)

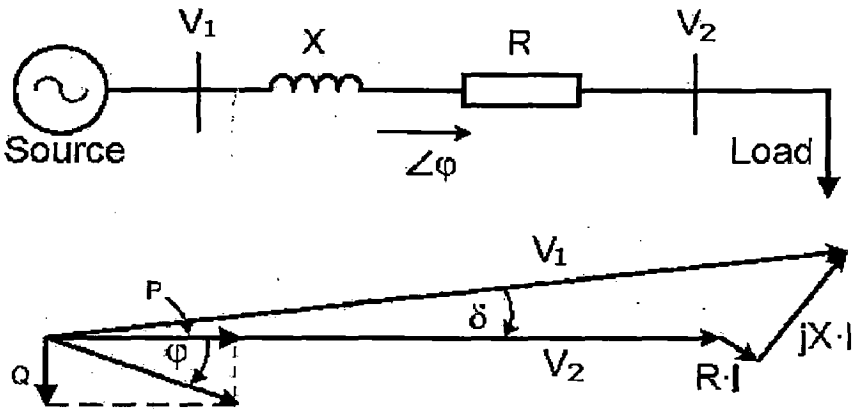
Fig.2.1 Principles of Shunt Compensation in an ac System

a) Without reactive compensation. b) Shunt compensation with a current source.

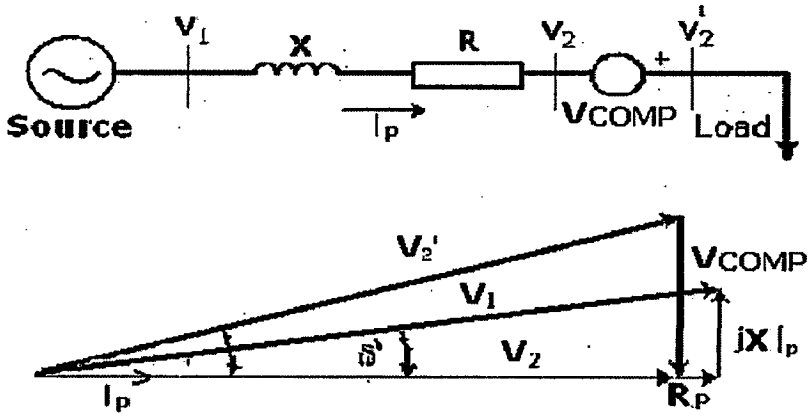
If the load needs leading compensation, then an inductor would be required. Also a current source or a voltage source can be used for inductive shunt compensation. The main advantages of using voltage or current source VAR generators (instead of inductors or capacitors) are that the reactive power generated is independent of the voltage at the point of connection.

2.2.2. Series Compensation.

VAR compensation can also be of the series type. Typical series compensation systems use capacitors to decrease the equivalent reactance of a power line at rated frequency. The connection of a series capacitor generates reactive power in a self-regulated manner, balances a fraction of the line's transfer reactance. Like shunt compensation series compensation may also be implemented with current or voltage source devices as shown in figure2.2 .The power system of figure (2.2-a) shows the same of figure (2.1-a), also with the reference angle in V2, and figure (2.2-b) the results obtained with the series compensation through a voltage source, which is adjusted again to have unity power factor operation at V2. However, the compensation strategy is different when compared with shunt compensation. In this case voltage VCOMP has been added between the line and the load to change the angle of V2, which is now the voltage at the load side. With the appropriate magnitude adjustment of VCOMP, unity power factor can again be reached at V2. It can be seen from the phasor diagram of figure (2.2-b) VCOMP generates a voltage in opposite direction to the voltage drop in the line inductance because it lags the current Ip.



(a)



(b)

Fig.2.2 Principles of series compensation

a) System without compensation. b) Series compensation with voltage source.

2.3 TRADITIONAL VAR GENERATORS:

2.3.1. Introduction:

Rotating and static generators were commonly used to compensate reactive power. In the last decade, a large number of different static VAR generators, using power electronic technologies have been proposed and developed. There are two ways to the realization of power electronics based VAR compensators. First, thyristor switched capacitors and reactors with tap changing transformers, and second, the other group that uses self-commutated static converters [18].

2.3.2. Thyristorised VAR Compensators:

Static VAR compensators (SVC) consist of standard reactive power shunt elements (reactors and capacitors) which are controlled to provide rapid and variable reactive power. They can be grouped into two basic categories.

- Thyristor Switched Capacitor.
- Thyristor Controlled Reactor.

2.3.2.1. Thyristor Switched Capacitors:

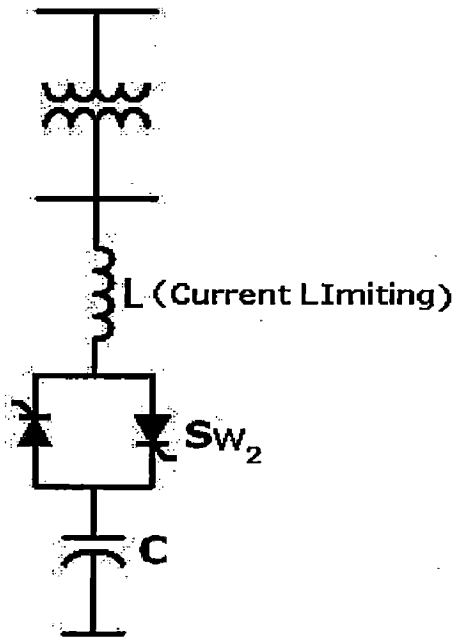


Fig.2.3 Thyristor Switched Capacitor Configuration

Figure 2.3 shows the basic scheme of the thyristor switched capacitor (TSC) type for static var compensation. First introduced by ASEA in 1971 [19].The shunt capacitor bank is split up into appropriate small steps, which are individually switched in and out using bidirectional thyristor switches. Each single-phase branch consists of two major parts, the capacitor C and the thyristor switches Sw1 and Sw2. In addition, there is a minor component, the inductor L, whose purpose is to limit the rate of rise of the current through the thyristors and to prevent resonance with the network (normally 6% with respect to Xc). The capacitor may be switched with a minimum of transients if the thyristor is turned on at the instant when the capacitor voltage and the network voltage have the same value.

Static compensators of the TSC type have the following properties

- Stepwise control,
- Average delay of one half a cycle (maximum one cycle)
- No generation of harmonics since current transient component can be attenuated effectively

2.3.2.2. Thyristor Controlled Reactor:

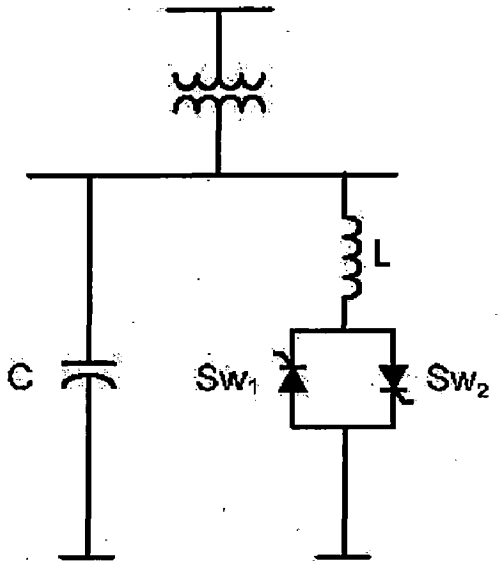


Fig.2.4 The thyristor controlled reactor configuration

Figure 2.4 shows the scheme of a static compensator of the thyristor controlled reactor (TCR) type. Each of the three phase branches includes an inductor L, and the thyristor switches Swl and Sw2. Reactors may be both switched and phase-angle controlled [20].

When phase-angle control is used, a continuous range of reactive power consumption is obtained. It results, however, in the generation of odd harmonic current components during the control process. Full conduction is achieved with a gating angle of 90°. Partial conduction is obtained with gating angles between 90° and 180°, as shown in figure2.5. By increasing the thyristor gating angle, the fundamental component of the current reactor is reduced [20][21]. This is equivalent to increase the inductance, reducing the reactive power absorbed by the reactor. However, it should be pointed out that the change in the reactor current may only take place at discrete points of time, which means that adjustments cannot be made more frequently than once per half-cycle. Static compensators of the TCR type are characterized by the ability to perform continuous control, maximum delay of one half cycle and practically no transients.

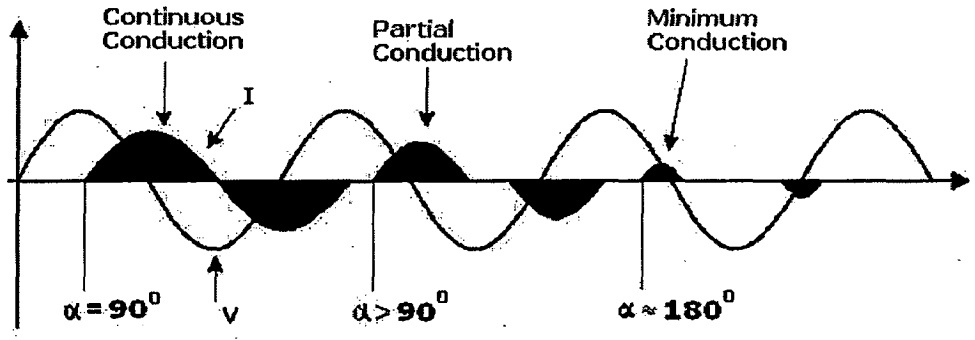


Fig. 2.5 voltage and current waveforms in a TCR for different thyristor phase shift angles.

The principal disadvantages of this configuration are the generation of low frequency harmonic current components, and higher losses when working in the inductive region (i.e. absorbing reactive power)

2.4. SELF-COMMUTATED VAR COMPENSATORS:

The application of self commutated converters as a means of compensating reactive power has demonstrated to be an effective solution. This technology has been used to implement more typical compensator equipment such as static synchronous compensators, unified power flow controllers (UPFCs), and Dynamic Voltage Restorers (DVRs) [22].

2.4.1. Principles of Operation:

With the remarkable progress of gate commutated semiconductor devices, attention has been focused on self-commutated VAR compensators capable of generating or absorbing reactive power without requiring large banks of capacitors or reactors. Several approaches are possible including current-source and voltage-source converters.

The current-source approach shown in figure.2.6 uses a reactor supplied with a regulated dc current, while the voltage-source inverter, displayed in figure.2.7, uses a capacitor with a regulated dc voltage.

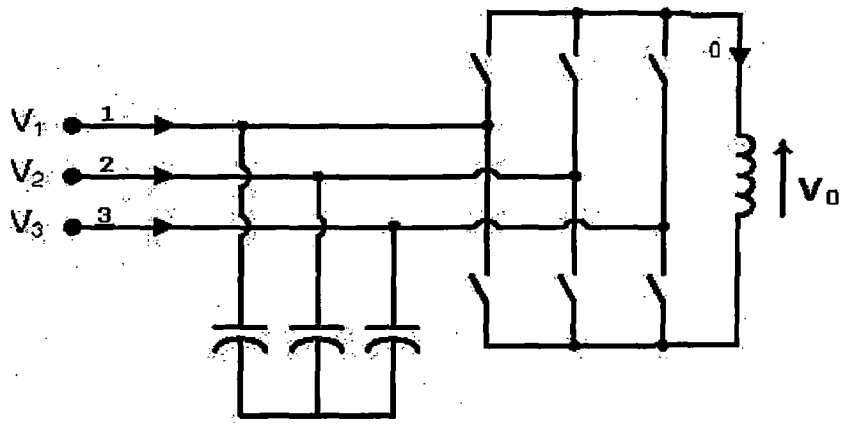


Fig.2.6 AVAR Compensator topology implemented with a current source converter

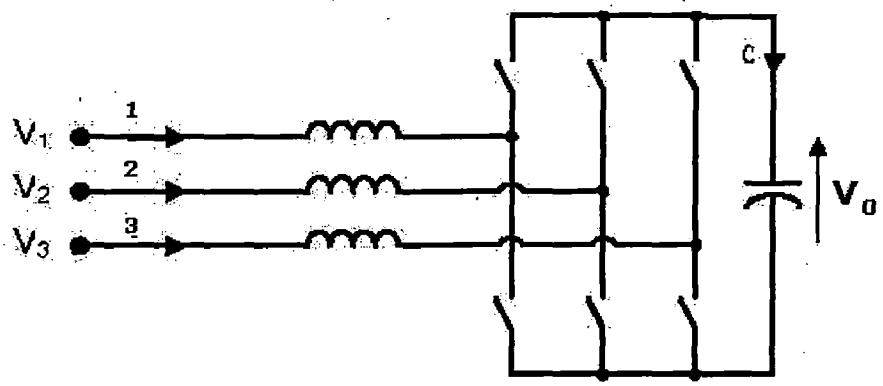


Fig.2.7 A VAR Compensator topology implemented with a voltage source converter

Principal advantages of self-commutated VAR compensators

- Significant reduction of size.
- Potential reduction in cost achieved from the elimination of a large number of passive components.
- Lower relative capacity requirement for the semiconductor switches.
- Because of its smaller size, self-commutated VAR compensators are well suited for applications where space is a premium.

2.4.2. Multi Level Compensators:

Multilevel converters are being investigated and some topologies are used today as static VAR compensators. The main advantages of multilevel converters are less harmonic generation and higher voltage capability because of serial connection of bridges or semiconductors. The most popular arrangement today is the three-level neutral-point clamped topology.

2.4.2.1. Three- Level Compensator:

Figure2.8 shows a shunt VAR compensator implemented with a three-level neutral-point clamped (NPC) converter. Three-level converters are becoming the standard topology for medium voltage converter applications, such as machine drives and active front-end rectifiers. The advantage of three-level converters is that they can reduce the generated harmonic content, since they produce a voltage waveform with more levels than the conventional two-level topology. Another advantage is that they can reduce the semiconductors voltage rating and the associated switching frequency [23].

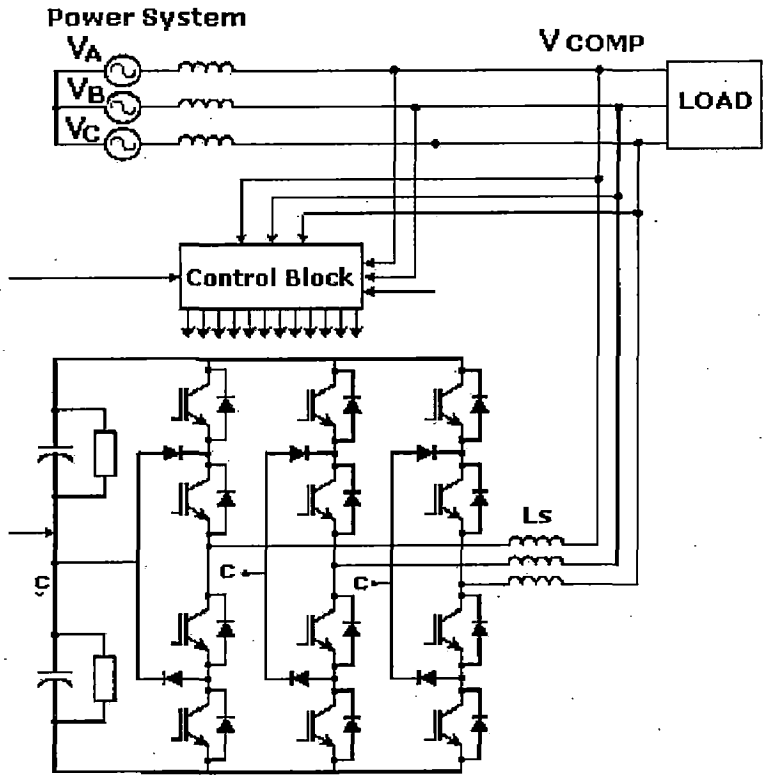


Fig.2.8 Shunt VAR compensator implemented with a three level NPC inverter

Three-level converters consist of 12 self-commutated semiconductors such as IGBTs or IGCTs, each of them shunted by a reverse parallel connected power diode, and six diode branches connected between the midpoint of the dc link bus and the midpoint of each pair of switches as shown in figure2.8. By connecting the dc source sequentially to the output terminals, the converter can produce a set of PWM signals in which the frequency, amplitude and phase of the ac voltage can be modified with adequate control signals.

2.5. NEW VAR COMPENSATOR'S TECHNOLOGY:

Based on power electronics converters and digital control schemes, reactive power compensators implemented with self-commutated converters have been developed to compensate not only reactive power, but also voltage regulation, flicker, harmonics, real and reactive power, transmission line impedance and phase-shift angle. It is important to note, that even though the final effect is to improve power system performance, the control variable in all cases is basically the reactive power. Some of self commutated converters are Static Synchronous Compensator (STATCOM), the Static Synchronous Series Compensator (SSSC), the Dynamic Voltage Restorer (DVR), and Unified Power Flow Controller (UPFC).

2.5.1. Static Synchronous Compensator (STATCOM):

The static synchronous compensator is based on a solid-state voltage source, implemented with an inverter and connected in parallel to the power system through a coupling reactor, in analogy with a synchronous machine, generating balanced set of three sinusoidal voltages at the fundamental frequency, with controllable amplitude and phase-shift angle. This equipment, however, has no inertia and no overload capability. Example of this topology is shown in figure 2.8.

2.5.2. Static Synchronous Series Compensator (SSSC):

A voltage source converter can also be used as a series compensator as shown in figure2.9. The SSSC injects a voltage in series to the line, 90° phase-shifted with the load current, operating as a controllable series capacitor. The basic difference, as compared

with series capacitor, is that the voltage injected by an SSSC is not related to the line current and can be independently controlled.

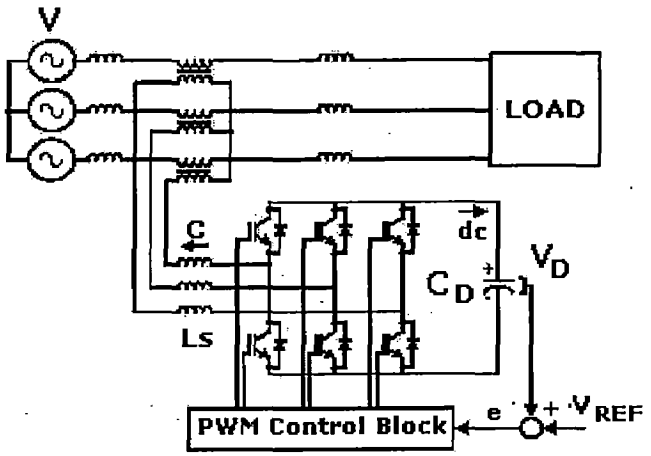


Fig.2.9 Static Synchronous Series Compensator

2.5.3. Dynamic Voltage Restorer (DVR):

A DVR, shown in figure2.10 is a device connected in series with the power system and is used to keep the load voltage constant, independently of the source voltage fluctuations. When voltage sags are present at the load terminals, the DVR responds by injecting three ac voltages in series with the incoming three-phase network voltages, compensating for the difference between faulted and pre fault voltages. Each phase of the injected voltages can be controlled separately (i.e., their magnitude and angle) [25]. Active and reactive power required for generating these voltages are supplied by the voltage source converter, fed from a DC link as shown in figure 2.10.

The key components of the DVR are:

- Switchgear
- Booster transformer
- Harmonic filter
- IGCT voltage source converter
- DC charging unit
- Control and protection system

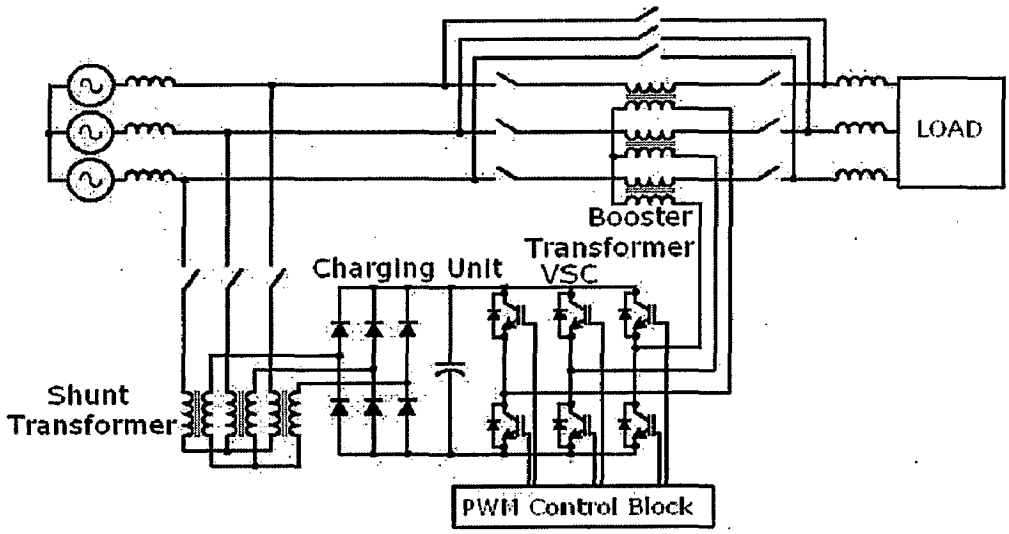


Fig.2.10 Dynamic Voltage Restorer (DVR)

When power supply conditions remain normal the DVR can operate in low-loss standby mode, with the converter side of the booster transformer shorted. Since no voltage source converter (VSC) modulation takes place, the DVR produces only conduction losses. Use of Integrated Gate Commutated Thyristor (IGCT) technology minimizes these losses.

2.5.4. Unified Power Flow Controller (UPFC):

The unified power flow controller (UPFC), shown in figure.2.11 consists of two switching converters operated from a common dc link provided by a dc storage capacitor. One connected in series with the line, and the other in parallel. This arrangement functions as an ideal ac to ac power converter in which the real power can freely flow in either direction between the ac terminals of the two inverters and each inverter can independently generate (or absorb) reactive power at its own ac output terminal. The series converter of the UPFC injects via series transformer, an ac voltage with controllable magnitude and phase angle in series with the transmission line. The shunt converter supplies or absorbs the real power demanded by the series converter through the common dc link. The inverter connected in series provides the main function of the UPFC by injecting an ac voltage with controllable magnitude and phase angle π ($0 \leq \pi \leq 360°$), at the power frequency, in series with the line via a transformer. The real

power exchanged at the ac terminal, that is the terminal of the coupling transformer, is converted by the inverter into dc power which appears at the dc link as positive or negative real power demand. The reactive power exchanged at the ac terminal is generated internally by the inverter [26].

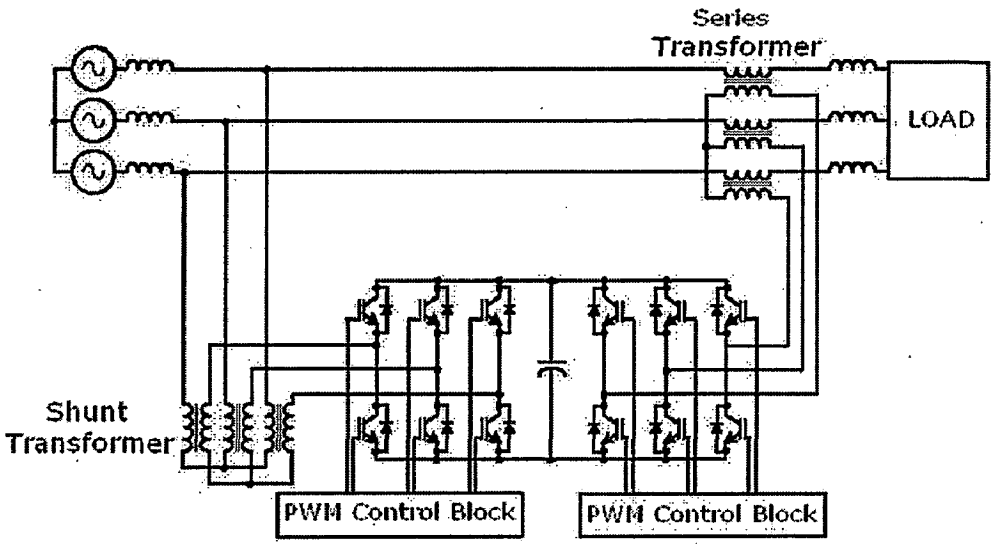


Fig.2.11 UPFC power circuit topology.

The basic function of the inverter connected in parallel (inverter 1) is to supply or absorb the real power demanded by the inverter connected in series to the ac system (inverter 2), at the common dc link. Inverter 1 can also generate or absorb controllable reactive power, if it is desired, and thereby it can provide independent shunt reactive compensation for the line. It is important to note that whereas there is a closed "direct" path for the real power negotiated by the action of series voltage injection through inverter 1 and back to the line, the corresponding reactive power exchanged is supplied or absorbed locally by inverter2 and therefore it does not flow through the line. Thus, inverter 1 can be operated at a unity power factor or be controlled to have a reactive power exchange with the line independently of the reactive power exchanged by inverter 2. This means that there is no continuous reactive power flow through the UPFC.

CHAPTER - III

MULTILEVEL INVERTERS

This chapter focuses on the basic principle of obtaining a multilevel waveform, classification of multi-level inverters and their operation, which includes some of recently developed circuit topologies.

3.1. INTRODUCTION

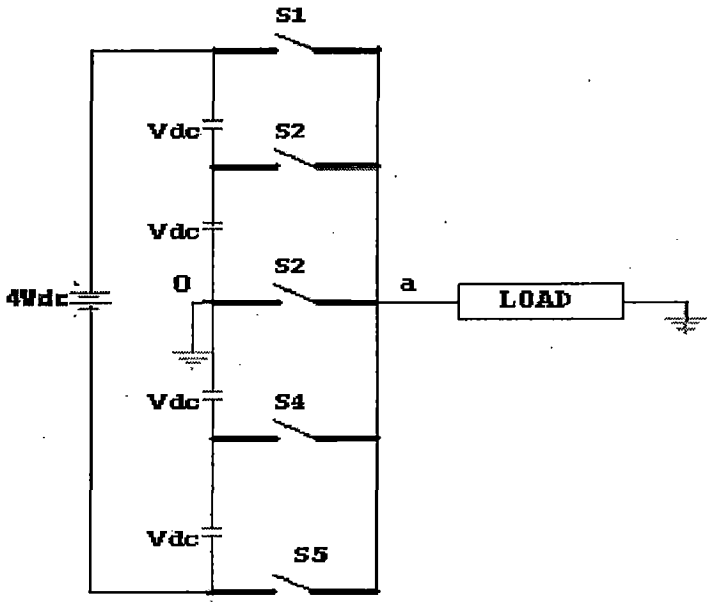
Multi level inverters are based on the fact that sine wave can be approximated to a stepped wave form having large number of steps. The steps being supplied from different DC levels supported by series connected batteries or capacitors. The individual devices in multilevel configuration have a much lower dv/dt per switching at a much lower frequency than PWM- controlled inverter. The unique structure of multi level inverters allows them to reach high voltages and therefore lower voltage rating devices can be used.

Multilevel inverter technology was developed recently as a very important alternative in the area of high-power medium-voltage energy control. The term multilevel starts with the 3-level inverter introduced by "Akari Nabae "in 1981[7]. By increasing the number of levels in inverter the output voltages have more steps generating staircase waveform which has reduced harmonic distortion. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms.

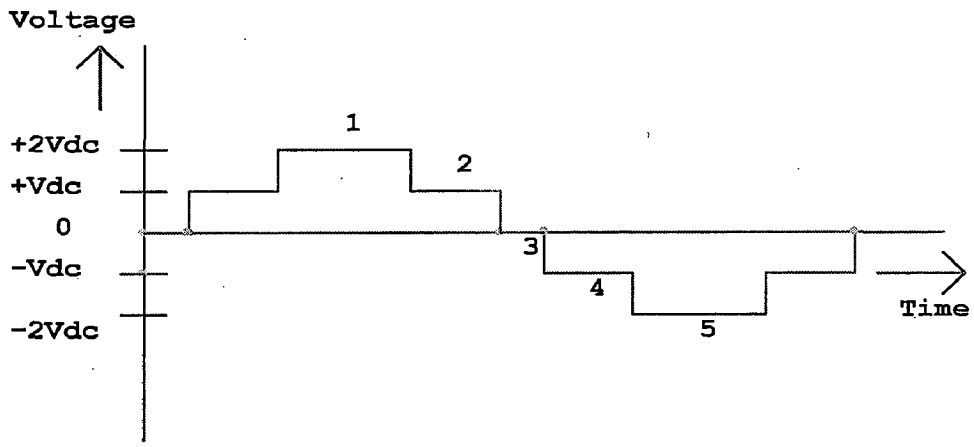
Multi level inverters offer a better choice at a high power end because the high volt-ampere ratings are possible with these inverters without the problems of high dv/dt and the other associated ones [10][11]. As the number of levels increases the obtained output waveform has more steps producing a very fine stair case wave and approaching very closely to the desired sine wave. It can be easily understood that as the more and more steps are included in the waveform the harmonic distortion of the output wave decreases approaching zero as the number of levels approaching infinity.

3.2 BASIC PRINCIPLE:

To understand the concept of multilevel inverters consider the circuit shown in figure3.1. Here capacitors are connected in series and across the main DC source 4 V_{dc}.



(a)



(b)

Fig.3.1 Basic principle of Multi-level inverter (a) Circuit (b) output voltage

Here capacitors are connected in series and across the main DC source V_{dc}. The switches S_1-S_5 are closed one at a time for a fixed duration of time. The load voltage is measured

with respect to the reference point 0, as shown in the waveform in figure.3.1. Table3.1 lists the switching states and output voltage obtained for each state of switches. Switch state '1' means ON and '0' means OFF. It can be seen that a stepped wave is output to the load. The stepped can be approximated to a sine wave by adding more number of capacitors (levels) in series. Also it can be noted that 5-level waveform requires four capacitors and so on. In general an inverter consists of m-1 capacitors on the DC bus and produces m-levels of the phase voltage.

V_{ao}	Switching States				
	S_1	S_2	S_3	S_4	S_5
0	0	0	1	0	0
V_{dc}	0	1	0	0	0
$2V_{dc}$	1	0	0	0	0
V_{dc}	0	1	0	0	0
0	0	0	1	0	1
$-V_{dc}$	0	0	0	1	1
$-2V_{dc}$	0	0	0	0	1
$-V_{dc}$	0	0	0	1	0

Table 3.1 Switching States of Multi-level Inverter

Features of Multilevel Inverters

- This can generate output voltages with extremely low distortion and lower dv/dt.
- They draw input current with very low distortion.
- They can operate with a lower switching frequency.
- Excellent dynamic response
- Increase frequencies up to 200Hz
- Improved AC supply power factor
- Lower audible noise levels

- This topology can be used either to eliminate or minimize lower order harmonics while increasing the overall rating of the static var compensator

Problems associated with Multilevel Inverters

Some of the problems associated with multilevel inverters.

- Difficult and very complex to achieve series redundancy
- Capacitor voltage balancing
- More complex PWM control strategy for higher levels
- Circuit complexity for higher levels
- Large device control

3.3 TOPOLOGIES IN MULTILEVEL INVERTERS:

Different types of topologies are

- 3-level neutral point clamped Inverter(3LNPC)
- Diode Clamped Multi Level Inverter (DCMLI)
- Capacitor Clamped Multi Level Inverter (CCMLI)
- Cascaded Multi Level Inverter (CMLI)

The advantages are

- Reduced harmonic content.
- Snubberless operation for Capacitor Clamped MLI.
- Reduced dv/dt.
- Modular design.
- Snubberless operation for Capacitor Clamped MLI.
- Low switching losses.
- High voltage/power output with reduced rating of individual devices.
- Snubberless operation for Capacitor Clamped MLI.

The disadvantages are

- Large device count for Diode Clamped MLI

- Voltage balancing of DC link capacitors
- Complex PWM control.
- Uneven current stresses on power devices.
- Requirement of split DC link.
- Series redundancy difficult to achieve.
- Separate DC link sources(for ISHB)

3.3.1 Three-Level Neutral Point Clamped Inverter:

In case of the conventional two-level inverter configuration, the harmonic contents reduction of an inverter output current is achieved mainly by raising the switching frequency. However in the field of high voltage, high power applications the switching frequency of the power device has to be restricted below 1 KHz, even with the HVIGBT and GCT, due to the increased switching loss. So the harmonic reduction by raised switching frequency of a two-level inverter becomes more difficult in high power applications. In addition, as the dc link voltage of a two-level inverter is limited by voltage ratings of switching devices, the problematic series connection of switching devices is required to raise the dc link voltage. By series connection, the maximum allowable switching frequency has to be more lowered, thus the harmonic reduction becomes more difficult.

From the aspect of harmonic reduction and high de-link voltage level; three-level approach seems to be the most promising alternative. The harmonic contents of a three-level inverter are less than that of a two-level inverter at the same switching frequency and the blocking voltage of the switching device is half of the de-link voltage. So the three-level inverter topology is generally used in realizing the high performance, high voltage ac drive systems.

For power/high voltage applications, the NPC inverter has advantages such that the blocking voltage of each switch is clamped to the half of DC –link voltage and the output voltage and current waveforms contain low harmonics compared to the conventional two -level inverter operating with the same switching frequency.

Figure 3.2 shows the circuit of a Neutral Point Clamped Three Level, three -phase inverter using MOSFET devices. The dc link capacitor C has been split to create the neutral point 0. A pair of devices with bypass diodes is connected in series with an additional diode connected between the neutral point and the center of the pair. The devices S_{1U} and S_{4U} function as main devices (like two level inverter), and S_{2U} and S_{3U} function as auxiliary devices which help to clamp the output potential to the neutral point with the help of clamping diodes D_1 and D_2.

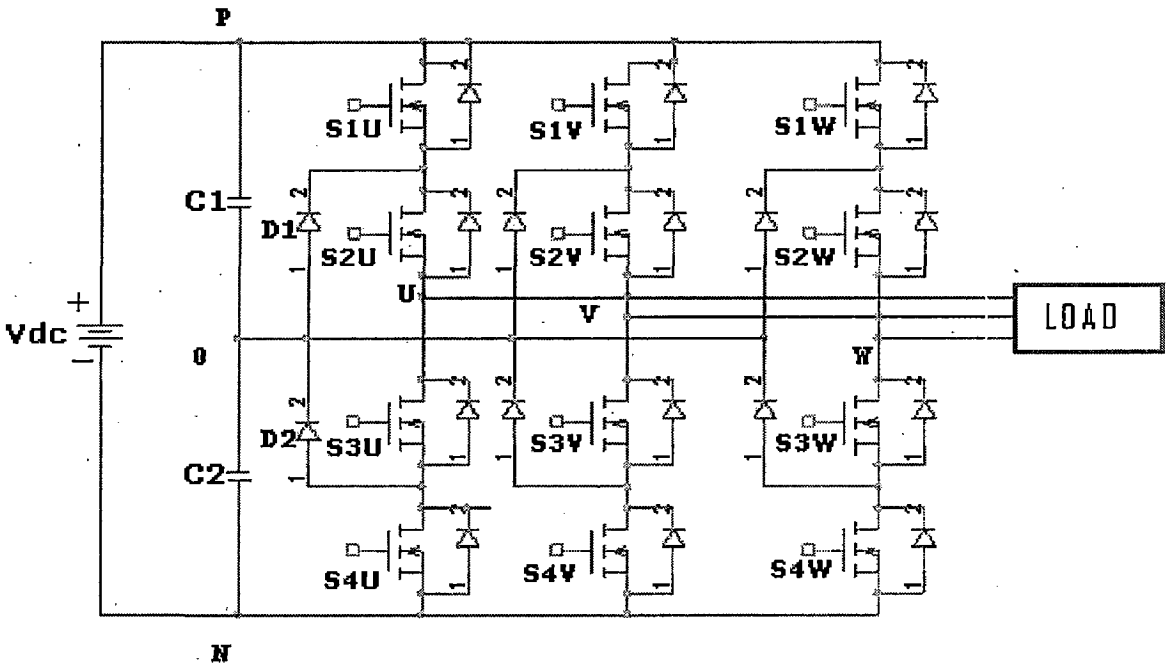


Fig 3.2 Neutral Point Clamped Three-level Inverter

The harmonic contents of a three-level inverter are less than that of a two-level inverter at the same switching frequency and the blocking voltage of the switching device is half of the de-link voltage.

However, the concept of three- level inverter introduces a new zero voltage level (also called neutral point), other than the positive and negative voltage levels in comparison with two- level inverter. This type of DC links inherently associated with neutral point variations and results in a voltage unbalance problems between the lower

and upper capacitor dc-link capacitors, causing undesirable uneven voltage stress at the upper and lower array of switching elements [8][9]. The inherent neutral point potential variation of a three-level inverter has to be effectively suppressed to fully utilize the advantages of three-level inverter. More complex PWM control is needed than 2-level. And requires mid point voltage balance control and neutral point voltage control..

3.3.2. Diode Clamped Multi Level Inverter (DCMLI):

One leg of three-level diode-clamped inverter is shown in figure 3.3.In this circuit, the dc-bus voltage is split into three levels by two series-connected bulk capacitors, C_1 and C_2. The middle point of the two capacitors n can be defined as the neutral point. The output voltage V_{an} has three states: $V_{dc/2}$, 0, and $-V_{dc/2}$. For voltage level $V_{dc}/2$, switches $S_1$and S_2 need to be turned on; for $-V_{dc/2}$, switches S_1' and S_2' need to be turned on; and for the 0 level, S_2 and S_1' need to be turned on.

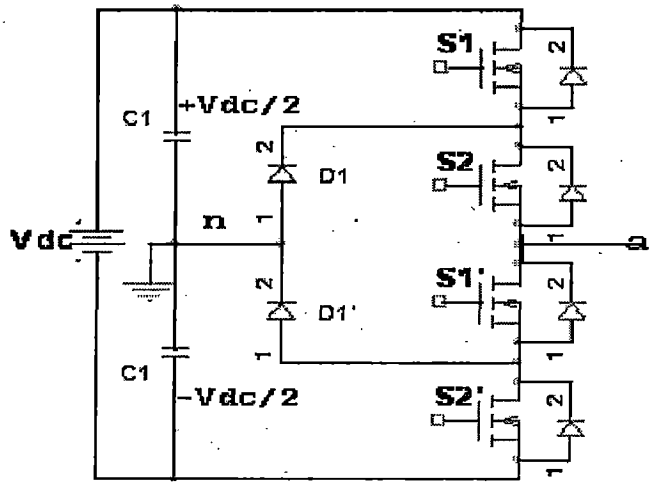


Fig 3.3 3-level Diode-clamped Inverter

The two diodes D_1 and D_1^1 clamp the switch voltage to half the level of the dc-bus voltage. When both switches S_1 and S_2 turn on, the voltage across phase 'a' and neutral is V_{dc}, i.e., $V_{an} = V_{dc}$. In this case, d_1 balances out the voltage sharing between S_1' and S_2' with S_1' blocking the voltage across C_1 and S_2' blocking the voltage across C_2. Notice that output voltage v_{an} is ac, and v_{a0} is dc. The difference between v_{an} and v_{a0} is the voltage

across C_2, which is $V_{dc/2}$. So diodes D_1 and D_1 are the key components that distinguish this circuit from a conventional two- level inverter.

Figure.3.4 shows a five-level diode-clamped converter in which the dc bus consists of four capacitors, C1, C_2, C_3, and C4. For dc-bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/4$, and each device voltage stress will be limited to one capacitor voltage level $V_{dc/4}$ through clamping diodes

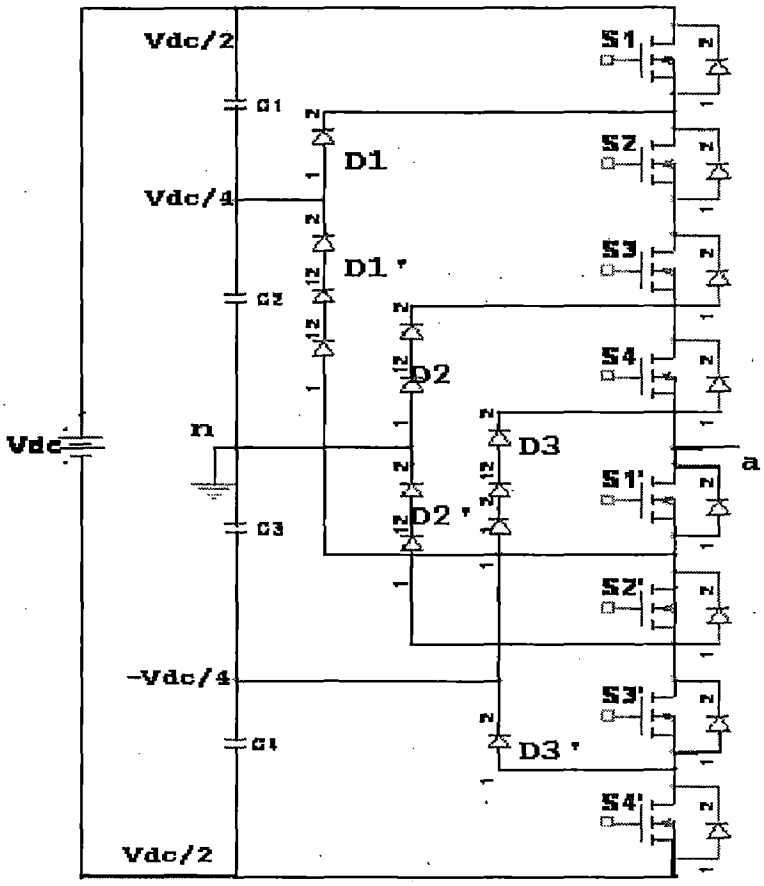


Fig.3.4 5-level Diode Clamped Inverter

The clamping diodes must have different voltage ratings for reverse voltage blocking even though each active switching device is only required to block a voltage level of V_{dc}/ (m - 1) where m is number of levels.

There are 5 switch combinations to synthesize five level voltages across phase *'a'* and *n.*

Output	S_1	S_2	S_3	S_4	S_1^1	S_2^1	S_3^1	S_4^1
V_{dc}	1	1	1	1	0	0	0	0
$V_{dc/4}$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$-V_{dc/4}$	0	0	0	1	1	1	1	0
$-V_{dc/2}$	0	0	0	0	1	1	1	1

Table 3.3 Switching Combinations Vs Output Voltage.

From figure 3.4 when lower devices S_2' to S_4' are turned on, D_1 and needs to block three capacitor voltages, or 3 $V_{dc/4}$. Similarly, D_2 and D_2' need to block $2V_{dc/4}$, and D_3 and D_3' needs to block 3 $V_{dc/4}$. Assuming that each blocking diode voltage rating is the same as the active device voltage rating, the number of diodes required for each phase will be (m — 1) x (m—2). This number represents a quadratic increase in *m*. When *m* is sufficiently high, the number of diodes required will make the system impractical to implement. If the inverter runs under PWM, the diode reverse recovery of these clamping diodes becomes the major design challenge in high-voltage high-power applications.

The diode-clamp Multi Level Inverter has some following advantages and disadvantages.

Advantages

- Reactive power flow can be controlled in power system.
- Large number of levels reduces the harmonic content and avoids the needs for filters.
- Since all devices are switched at fundamental frequency, the efficiency is high because of low switching losses.

Disadvantages

- Real power flow control is difficult for the individual converter.
- For large number of levels, the number of clamping diodes required is very high,(m-1)x(m-2) for each phase for m-level inverter.

3.3.3. Capacitor Clamped Multi Level Inverter (CCMLI):

There are some problems associated regarding high power applications which are dealing with main topologies that are implemented and controlled practically. These are

- Voltages unbalance between split dc capacitors.
- Series connected clamping diodes.
- Indirect clamping of inner switching devices

To overcome these problems, a multilevel structure with flying capacitors was proposed. This approach obviously overcomes the limitation of diode-clamped multilevel inverters. The flying capacitor multilevel inverter has not been widely applied in industry. Nevertheless it seems that it has important advantages over the diode clamp multilevel converter. This is because it uses a clamping capacitor across a two-switch pair. In spite of this, there is a fundamental problem dealing with voltage balancing between flying capacitors and each leg under practical operation. This leads to voltage unbalance and thus, unsafe operation. For its balancing, FCMLI requires the symmetric switching of control signals with a phase shift. Up to now, there has been very little work done to solve a fundamental problem in the FCMLI applications. Figure3.5 illustrates the fundamental block of 'a' phase-leg capacitor-clamped inverter. Clamping capacitor C_1 is charged when S_1 and S_1' are turned on, and is discharged when S_2 and S_2' are turned on.

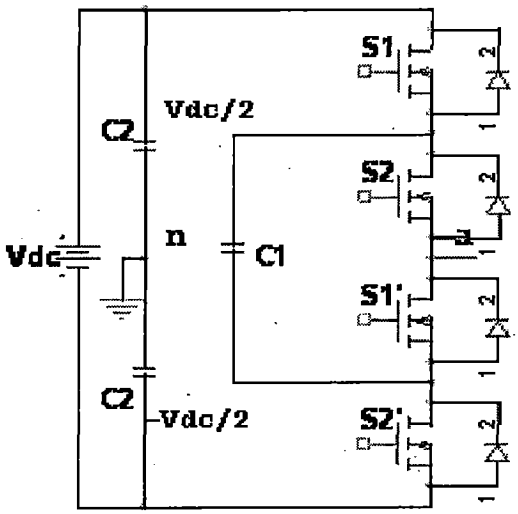


Fig 3.5 Three -level Capacitor Clamped MLI

The voltage synthesis in a five-level capacitor-clamped converter has more flexible and reliable than a diode-clamped inverter. For voltage level $V_{an} = V_{dc/2}$, turn on all upper switches S_1— S_4.

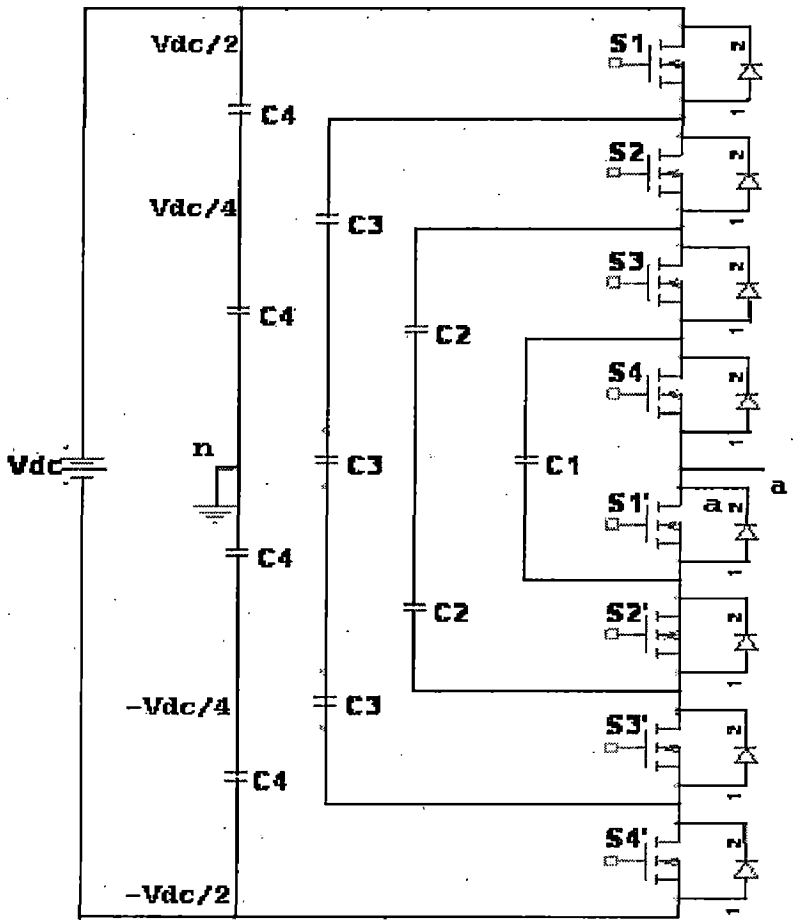


Fig 3.6 Five -level Capacitor Clamped MLI.

From figure.3.6, the voltage of the five-level with one lag of phase-'a' at output with respect to the neutral point *n*, V_{an} can be determined by the following switch combinations.

1. For voltage level $V_{an} = V_{dc/4}$, there are three combinations
   a. S_1, S_2, S_3, S1' (V_{an} = $V_{dc/2}$ of upper C_4's-$V_{dc/4}$ of C_1);
   b. S_2, S_3, S_4, S_4' (V_{on} = $3V_{dc}/4$ of C_3's -Vdc/2 of lower C_4's) ; and
   c. S_1, S_3, S_4, S_3' (V_{an} = Vdc/2 of upper C_4's-$3V_{dc}/4$ of C_3's +$V_{dc}/2$ of C_4's).

2. For voltage level $V_{an} = 0$, there are six combinations:
    a. S_1, S_2, S_1', S_2' (V_{an} = $V_{dc}/2$ of upper C_4's-$V_{dc/2}$ of C_2's);
    b. S_3, S_4, S_3', S_4' (V_{an} = $V_{dc}/2$ of C_2 - $V_{dc/2}$ of lower C_4);
    c. S_1, S_3, S_1', S_3' (V_{an} = $V_{dc}/2$ of upper C_4's -$3V_{dc}/4$ of C_3's + $V_{dc}/2$ of C_2's - $V_{dc}/4$of C_1);
    d. S_1, S_4, S_2', S_3' (V_{on} = $V_{dc}/2$ of upper C_4's -$3V_{dc}/4$ of CVs + $V_{dc}/4$ of C_1);
    e. S_2, S_4, S_2', S_4' (V_{an} = 3Vdc/4 of C_3's - $V_{dc}/2$ of C_2's +$V_{dc}/4$ of C_1- $V_{dc}/2$ of lower C_4's); and
    f. S_2, S_3, S_1', S_4' (V_{an} = $3V_{dc}/4$ of C_3's -$V_{dc}/4$ of C_1 -Vdc/2 of lower C_4's).
3. For voltage level $V_{an} = -V_{dc}/4$, there are three combinations:
    a. S_1, S_1', S_2', S_3' (V_{an} = V_{dc} /2 of upper C_4's -3 V_{dc} /4 of C_3's);
    b. S_4, S_2', S_3', S_4' (V_{an} = V_{dc} /4 of C_1 - V_{dc} /2 of lower C_4's); and
    c. S_3, S_1', S_3', S_4' (V_{an} = $V_{dc}/2$ of C_2's - V_{dc} /4 of C_1 - V_{dc} /2 of lower C_4's).
4. For voltage level $V_{an} = -V_{dc}/2$, turn on all lower switches, S_1'-S_4'.

Similar to diode clamping, the capacitor clamping requires a large number of bulk capacitors to clamp the voltage. Provided that the voltage rating of each capacitor used is the same as that of the main power switch, an m-level converter will require a total of (m - 1) x (m - 2)/2 clamping capacitors per phase leg in addition to (m - 1) main de-bus capacitors.

Advantages

- Both real and reactor power flow can be controlled.
- Large no of storage capacitors provides extra ride through capabilities during power outage.
- Provides switch combination redundancy for balancing different voltage levels.
- When the no. of levels is high enough, harmonic content will be low enough to avoid the need for filters

Disadvantages

- The inverter control will be complicated and switching frequency losses will be high for real power transmission.
- An excessive no of storage capacitors is required when the no. of levels is high.

3.3.4 Cascaded Multi cell Inverters:

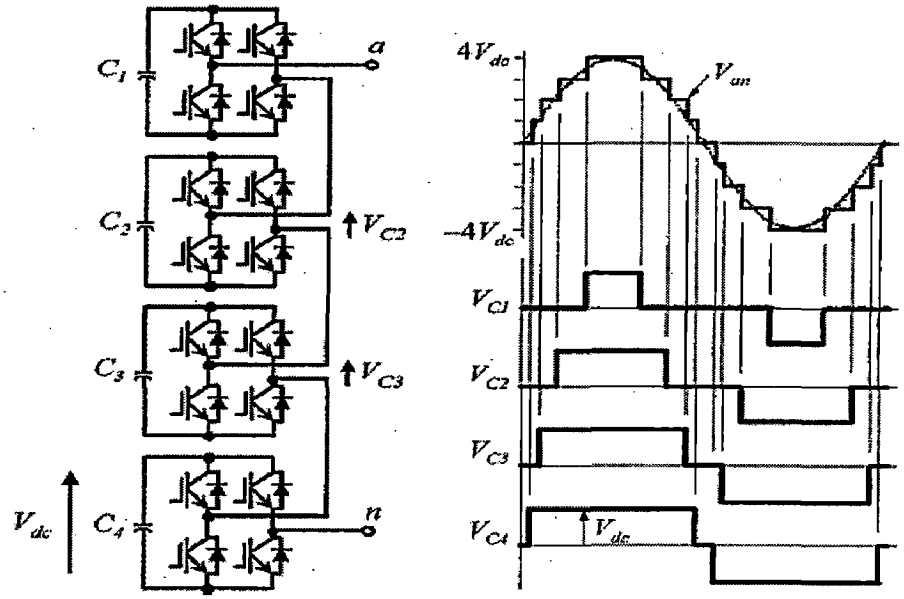


Fig 3.7: Cascaded Inverter circuit Topology and its associated waveform

A different converter topology is introduced here, which is based on the series connection of single-phase inverters with separate dc sources. Figure. 3.7 shows the power circuit for one phase leg of a nine-level inverter with four cells in each phase. The resulting phase voltage is synthesized by the addition of the voltages generated by the different cells. Each single-phase full-bridge inverter generates three voltages at the output: $+V_{dc}$, 0, and $-V_{dc}$. This is made possible by connecting the capacitors sequentially to the ac side via the four power switches. The resulting output ac voltage swings from $-4V_{dc}$ to $+4V_{dc}$ with nine levels and the staircase waveform is nearly sinusoidal, even without filtering.

Advantages

- Requires the least no. of components among all the multilevel inverters to achieve the same number of voltage levels
- Modularized circuit lay out and packaging is possible since each level has the same structure and there are no extra clamping diodes or voltage balancing capacitors.
- Soft switching is possible to avoid bulky and lossy resistor capacitor diode snubbers.

Disadvantage

- Needs separate dc sources for real power conversions and thus its applications are somewhat limited.

3.4 Modulation techniques:

Different type of modulation techniques available for Multi-level inverters out of which SPWM and SVM has implemented in simulation using MATLAB 7.0.1.And the comparison of resulted wave forms with modulation techniques is shown.

3.4.1. Introduction:

Pulse Width Modulation (PWM) techniques has been developed and studied during past decades extensively. This method employs a triangular wave which can be called as carrier wave is modulated by a sine wave and the points of intersection has determined as the switching points of the power devices in the inverter. However, this method is unable to make full use of the inverter's supply voltage and the asymmetrical nature of the PWM switching characteristics produces relatively high harmonic distortion in the supply[12][13].

There are many different PWM methods have developed to fulfill and achieve the following aims

- Wide linear modulation range
- Less switching loss
- Less total harmonic distortion (THD) in the spectrum of switching waveform

- Easy implementation and less computation time.

For a long period, carrier-based PWM methods were widely used in most applications. A more advanced algorithm like Space Vector Modulation has overcome the negative points of Sine PWM technique and increases the overall system efficiency. Space Vector PWM (SVPWM) is a more sophisticated technique for generating a fundamental sine wave that provides a higher voltage to the motor and lower total harmonic distortion.

Advantages of PWM inverters

PWM inverters are mostly operated at low and medium switching frequencies and are the dominant technology used by industry

- Low manufacturing cost
- Simple voltage and control techniques
- Relatively simple and robust power circuit

Disadvantages

As mentioned earlier, most PWM inverters operate at low and medium switching frequency levels, a reason for this is that such converters need to switch rapidly to minimize loss. Any attempt to increase switching frequencies will also follow in an increase of switching loss and an increase in the generation of electromagnetic interference. Thus switching losses become a critical problem in PWM topologies.

3.4.2. Sinusoidal Pulse Width Modulation (SPWM)

In this technique the conduction time of the switching transistor can be varied on and off to regulate the output voltage to a predetermined value. One particularly small process is illustrated in figure 3.8 using simulink here the resulting PWM waveform has obtained in scope. A repeating sequence triangular wave is used as carrier waveform of voltage Vtri and sine wave is used as modulation wave of voltage Vref.

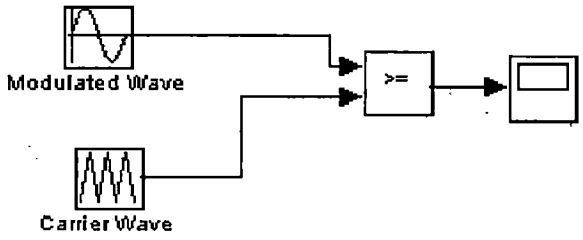


Fig 3.8 Triangle comparison PWM implementation

The comparator generates a high output if V_{ref} is greater than V_{tri} and a low output when V_{tri} is greater than V_{ref}. Hence the output can be interpreted directly as a switching function. Moreover, since the triangle waveform has a voltage linearly dependent on time, the comparator has an output pulse width linearly dependent on the level of V_{ref}.

Simulation of 3-Level Inverter Using SPWM:

Simulation of 3-level inverter has developed using MATLAB7.0.1. Figure 3.9 shows the simulink block diagram of 3-level Inverter.

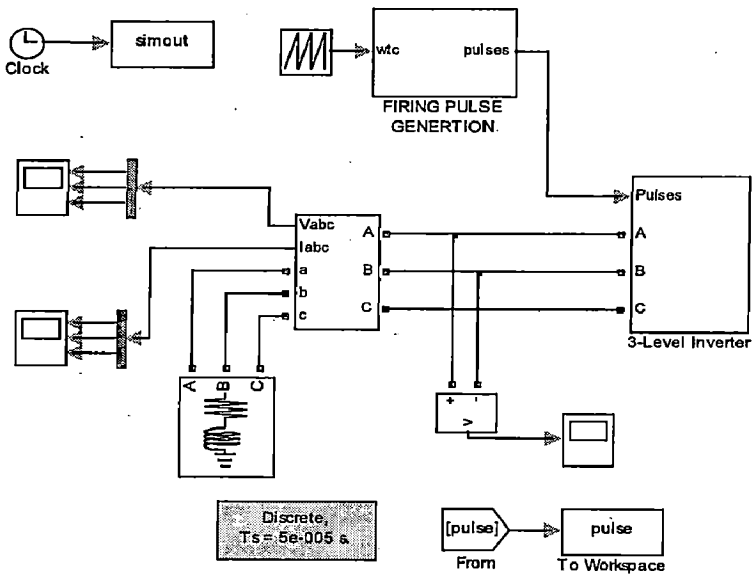


Fig 3.9 Simulink Block Diagram for 3-Level Inverter

Pulse width generation block for Phase A is shown in figure3.10

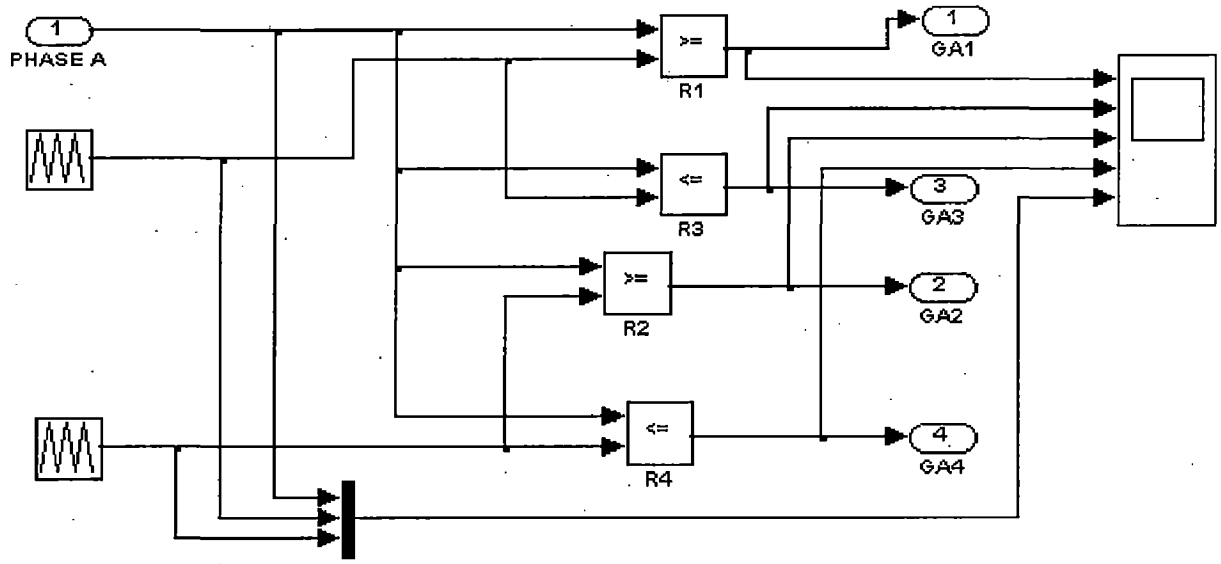


Fig 3.10 Pulse Width generation block of Phase A

Pulse width generation wave form of phase A of 3-level inverter is shown in figure3.11(a) and output line to line voltage and output current wave forms with FFT analysis is shown in figure 3.11(b) and figure 3.11(c).

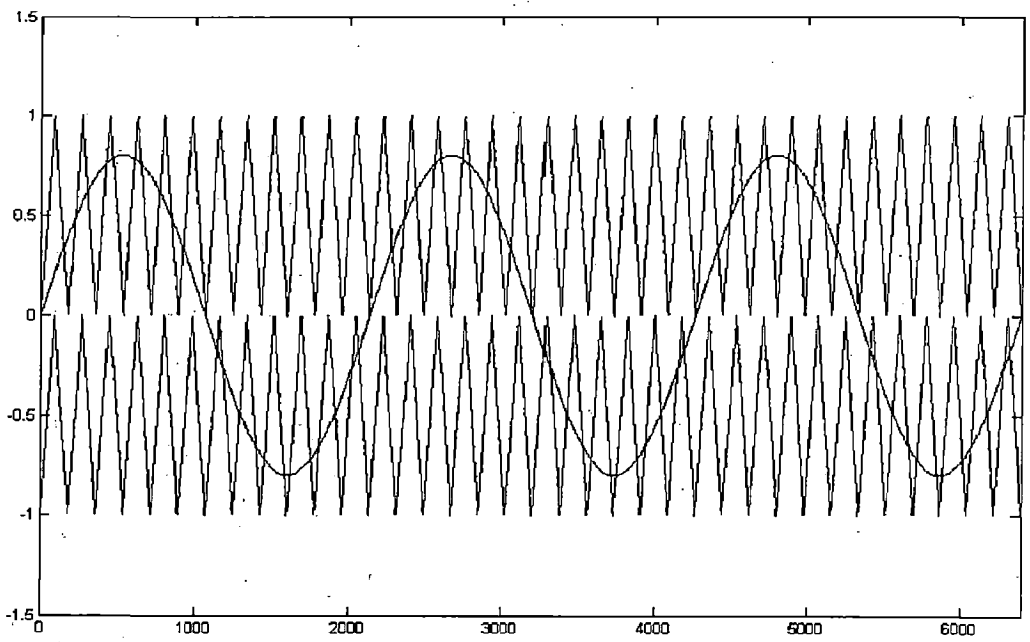


Fig 3.11(a) Modulating wave and Carrier Wave for Pulse width generation

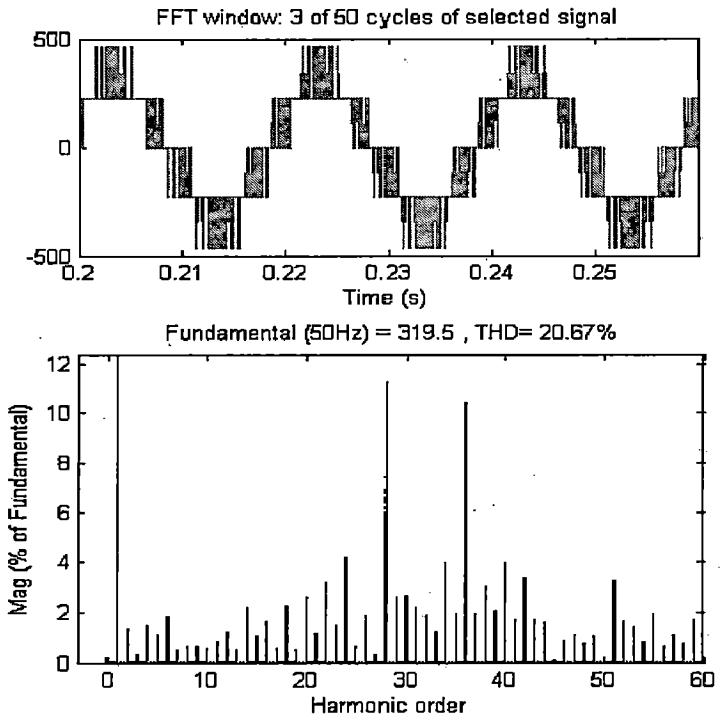


Fig 3.11(b) Line to Line Voltage and Harmonic spectrum at f=50HZ and MI=0.8

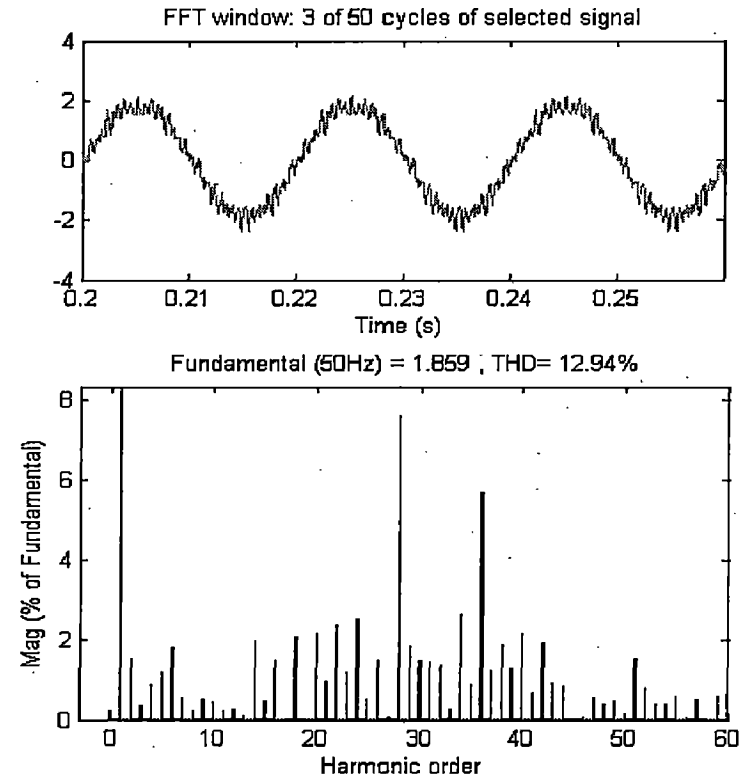


Fig 3.11(b) Line Current and Harmonic spectrum at f=50HZ and MI=0.8

3.4.3 Space Vector Modulation (SVM):

Generally, the PWM schemes generate the switching position patterns by comparing three-phase sinusoidal waveforms with a triangular carrier. In recent years, the space vector theory demonstrated some improvement for both the output crest voltage and the harmonic copper loss. The maximum output voltage based on the space vector theory is $2/\sqrt{3}$ times as large as the conventional sinusoidal modulation. The space-vector PWM (SVM) method is an advanced, computation-intensive PWM method and is possibly the best among all the PWM techniques. Because of its superior performance, it has been finding widespread application in recent years. It enables to feed the motor with a higher voltage than the easier sub-oscillation modulation method. This modulator allows a higher torque at high speeds, and a higher efficiency. It also minimizes THD and switching loss. To understand the SVM theory, the concept of a rotating space vector is very important. For example, if three-phase sinusoidal and balanced voltages given by the equations

$$V_a = V_m \cos(\omega t)$$

$$V_b = V_m \cos\left(\omega t - \frac{2\Pi}{3}\right)$$

$$V_c = V_m \cos\left(\omega t + \frac{2\Pi}{3}\right)$$

Are applied to a three-phase induction motor, it is shown that the space vector V^* with magnitude V_m rotates in circular orbit at angular velocity ω, where the direction of rotation depends on the phase sequence of the voltages.

3.4.3.1 Space Vector Modulation of 3-Level Inverter:

Figure 3.12 shows the circuit of a 3 -level, 3 -phase voltage source inverter using MOSFET devices. The dc link capacitor C has been split to create the neutral point '0'. A pair of devices with bypass diodes is connected in series with an additional diode connected between the neutral point and the center of the pair. The devices S_{1U} and S_{4U} function as main devices (like two level inverter), and S_{2U} and S_{3U} function as auxiliary

devices which help to clamp the output potential to the neutral point with the help of clamping diodes.

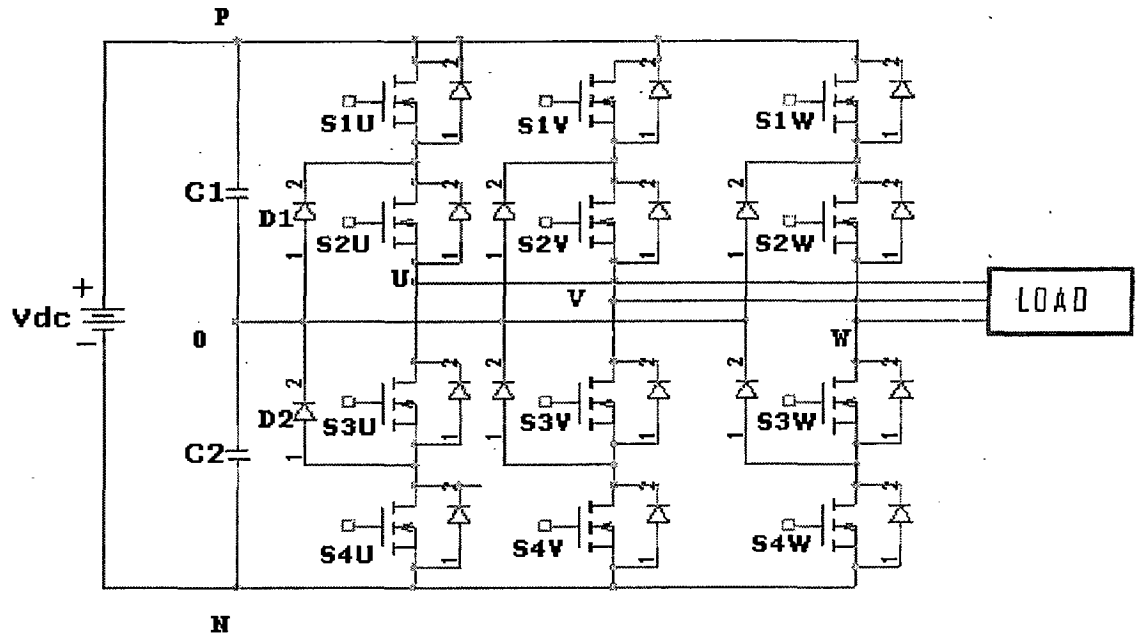


Fig.3.12. Neutral-point Clamped Three-level Inverter

Table.3.4 shows the switching states of a three-level inverter. Since three kinds of switching states exist in each phase, a three-level inverter has 27states [14].

Switching States	S_{1X}	S_{2X}	S_{3X}	S_{4X}	V_{X0}
P	ON	ON	OFF	OFF	+Vdc/2
0	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	-Vdc/2

TABLE 3.4 Switching States of a three-level inverter(X=U, V, W)

Magnitude of the voltage vectors, has divided into four groups:

- The zero group vectors (V_0)
- The small voltages vectors (V_1, V_4, V_7 ,V_{10} ,V_{13} ,V_{16})
- The middle voltage vectors (V_3, V_6 ,V_9 ,V_{12} ,V_{15} ,V_{18})
- The large voltage vectors (V_2, V_5 ,V_8 ,V_{11} ,V_{14} ,V_{17})

The zero voltage vector (ZVV) has three switching states, the small voltage vector (SVV) has two and both the middle voltage vector (MVV) and large voltage vector (LVV) have only one switching state. Figure 3.12 shows same representation of figure3.13. And it shows the space vector diagram of all switching state.

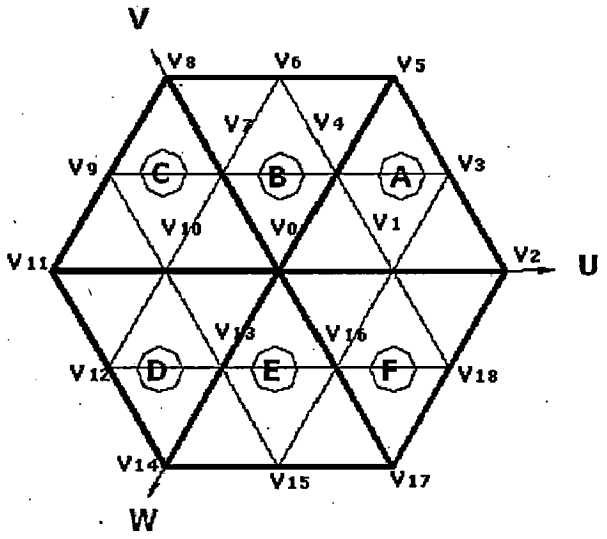


Fig. 3.12 Space voltage vectors representation

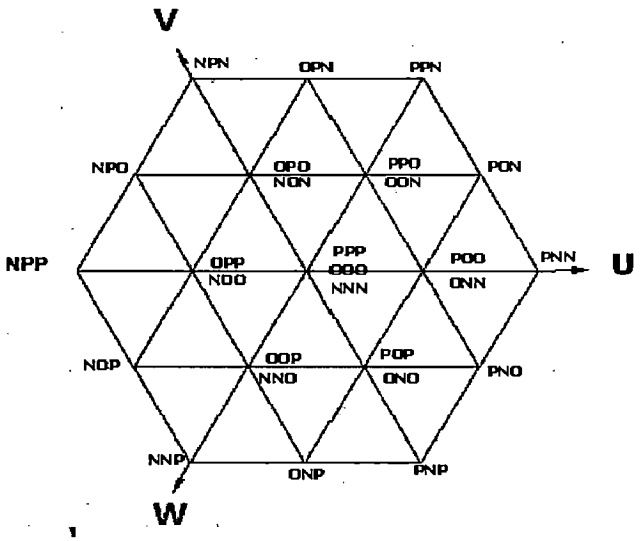


Fig 3.13 Space voltage vectors with their switching states

The triangle formed by the voltage vectors V_0, V_2, and V_5 has shown in figure 3.14 which can be divided into four smaller regions 1, 2, 3 and 4. In the space vector PWM generally the reference voltage vector is obtained by the vector sum of closest three voltage vectors to minimize the harmonic components of the line-to-line voltage at the

output. If the reference voltage vector V^* falls into the region 3 for an instant, the durations of each voltage vector can be calculated by the following sequences.

First, if the voltage vector and the reference voltage vector can be expressed by the exponential form as follows.

$$V_1 = \frac{1}{2} \qquad \textbf{(3.1)} \qquad V_3 = \frac{\sqrt{3}}{2} e^{j\frac{\pi}{6}} \qquad \textbf{(3.2)}$$

$$V_4 = \frac{1}{2} e^{j\frac{\pi}{3}} \qquad \textbf{(3.3)} \qquad V^* = V.e^{j\theta} \qquad \textbf{(3.4)}$$

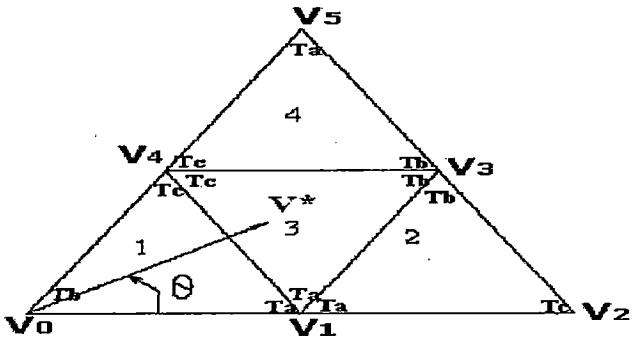


Fig. 3.14 Regions in Sector '0'

The equations 3.5 and 3.6 should be satisfied as space vector PWM for the conventional two-level inverters.

$$V_1.T_a + V_3.T_b + V_4.T_c = V^*.T_s \qquad \textbf{(3.5)}$$

$$T_a + T_b + T_c = T_s \qquad \textbf{(3.6)}$$

Substituting Equations, 4.1, 4.2, 4.3 in 4.5 then

$$\frac{1}{2}T_a + \frac{\sqrt{3}}{2}\left(\cos\frac{\pi}{6} + j\sin\frac{\pi}{6}\right).T_b + \frac{1}{2}\left(\cos\frac{\pi}{3} + j\sin\frac{\pi}{3}\right).T_c = V(\cos\theta + j\sin\theta).T_s \qquad \textbf{(3.7)}$$

Separating real part and imaginary part from above equation

$$\text{Real: } \frac{1}{2}T_a + \frac{\sqrt{3}}{2}\left(\cos\frac{\pi}{6}\right)T_b + \frac{1}{2}\left(\cos\frac{\pi}{3}\right).T_c = V(\cos\theta).T_s \qquad \textbf{(3.8)}$$

$$\text{Imaginary: } \frac{\sqrt{3}}{2}\left(\sin\frac{\pi}{6}\right)T_b + \frac{1}{2}\left(\sin\frac{\pi}{3}\right).T_c = V(\sin\theta).T_s \qquad \textbf{(3.9)}$$

From equations, 3.6, 3.8, 3.9 T_a, T_b and Tc can be calculated. These are shown in below equations which are for region 3.

$$T_a = Ts(1-2k\sin\theta)\ ,\quad T_b = T_s\left[2k\sin\left(\theta+\frac{\pi}{3}\right)-1\right], T_c = T_s\left[2k\sin\left(\theta-\frac{\pi}{3}\right)+1\right]$$

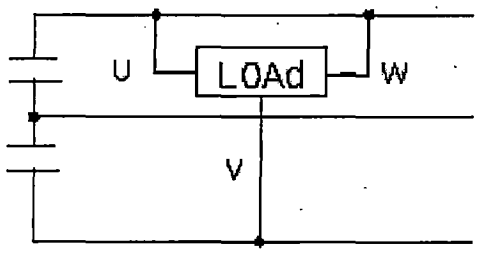
Where $k = \frac{2V}{\sqrt{3}}$ (0<k<1) .

R	1	2	3	4
Ta	$2kT_s\sin\left(\frac{\pi}{3}-\theta\right)$	$2T_s\left[1-k\sin\left(\frac{\pi}{3}+\theta\right)\right]$	$Ts[1-2k\sin\theta]$	$Ts[2k\sin\theta-1]$
Tb	$T_s\left[1-2k\sin\left(\frac{\pi}{3}+\theta\right)\right]$	$2kT_s\sin\theta$	$T_s\left[2k\sin\left(\frac{\pi}{3}+\theta\right)-1\right]$	$2kT_s\sin\left(\frac{\pi}{3}-\theta\right)$
Tc	$2kT_s\sin\theta$	$T_s\left[2k\sin\left(\frac{\pi}{3}-\theta\right)-1\right]$	$T_s\left[2k\sin\left(\theta-\frac{\pi}{3}\right)+1\right]$	$2T_s\left[1-k\sin\left(\frac{\pi}{3}+\theta\right)\right]$

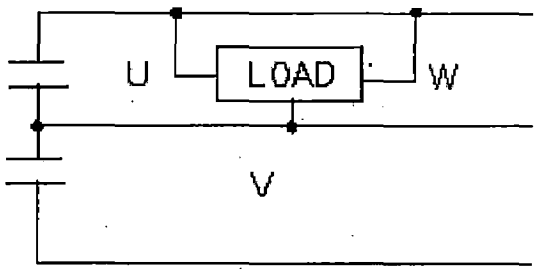
Table.3.5 Durations of voltage vectors in each region

In remaining regions i.e., 1, 2, 4 the durations of each voltage vector can be calculated in same way. Table.3.5. shows durations of the voltage vectors in each region

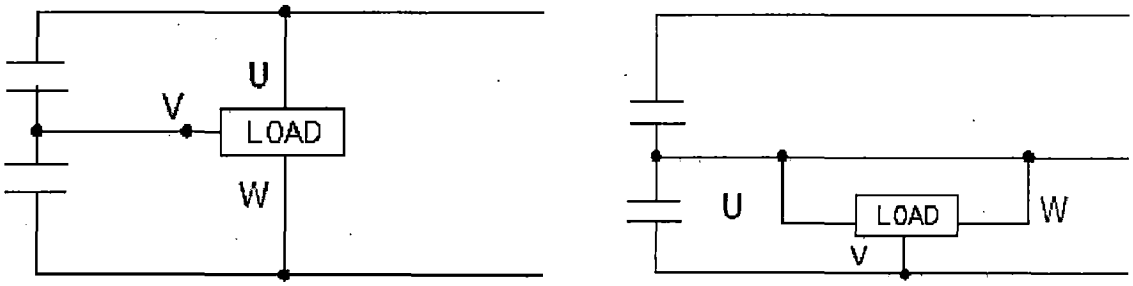
For example in case of voltage vector [PON] S_{U1}, S_{U2}, S_{V2}, S_{V3}, S_{W3}, S_{W4} are in ON state and others in OFF states. Thus the output terminal A, B, C has potential of $+V_{dc}/2$, 0, $-V_{dc}/2$ respectively. And the corresponding load connection is shown in figure3.15.



LVV (PNP)



USVV (POP)

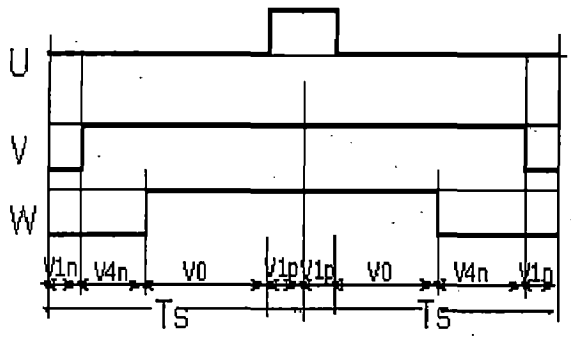


MVV (PON) **LSVV (ONO)**

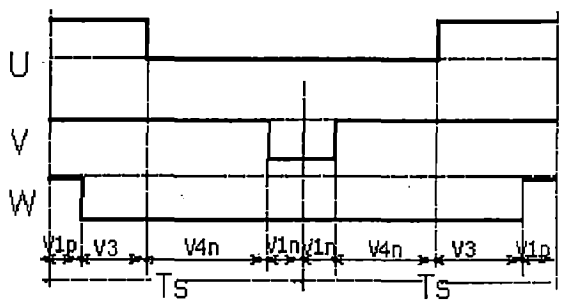
Fig. 3.15 Representative Vectors and Their Load Connections

The ZVV and LVV do not affect the neutral-point voltage because the load is not connected between neutral point and upper/lower capacitor. The MVV may have large effects on the neutral point voltage, because the upper capacitor or the lower capacitor is charged or discharged according to the load condition. The SVV affects the neutral-point voltage and it can be divided into two small groups; one group consists of V_{1n}, V_{4n}, V_{7n}, V_{10n}, V_{13n}, V_{16n} (Lower small voltage vectors: LSVV). It has close relation with charging or discharging of the lower dc-link capacitor. The other group consists of V_{1p}, V_{4p}, V_{7p}, V_{10p}, V_{13p}, V_{16p} (Upper small voltage vectors: USVV). It has close relation with charging or discharging of the upper dc-link capacitor [14][15].

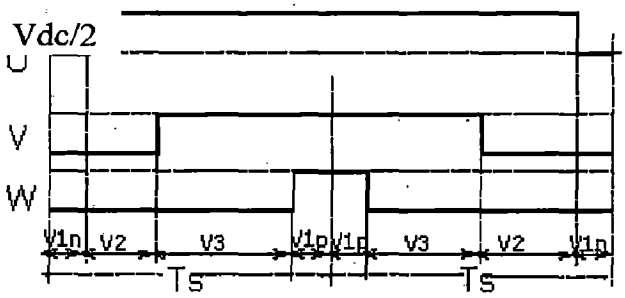
For example if the reference voltage vector is located in 3rd region in sector 1,the sequence of firing commands would be (POO, PON, OON, ONN, ONN, OON, PON, POO) with the durations ($T_a/2$, T_b, T_c, $T_a/2$, $T_a/2$, Tc, T_b, $T_a/2$).



(ONN,OON,OOO, POO, POO,OOO,OON, ONN)
($T_b/2$, T_a, T_c, $T_b/2$, $T_b/2$, T_c, T_a, $T_b/2$)
Sequence in Region 1



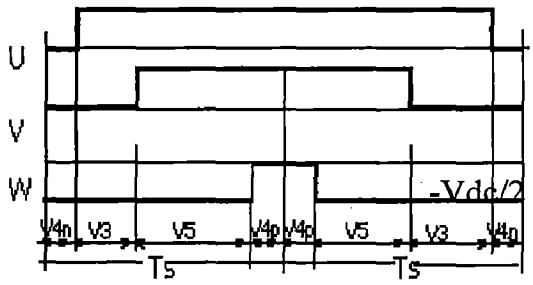
(POO, PON, OON, ONN, ONN, OON, PON, POO)
($T_a/2$, T_b, T_c, $T_a/2$, $T_a/2$, Tc, T_b, $T_a/2$)
Sequence in Region 3



(ONN, PNN, PON, POO, POO, PON, PNN, ONN)

($T_a/2$, T_c, T_b, $T_a/2$, $T_a/2$, T_b, T_c, $T_a/2$)

Sequence in Region 2



(OON, PON, PPN, PPO, PPO, PPN, PON, OON)

($T_c/2$, T_b, T_a, $T_c/2$, $T_c/2$, T_a, T_b, $T_c/2$)

Sequence in Region 4

Fig .3.16 Switching Sequences in four regions

The vector sequences and durations for the other sectors are calculated in the same way. The voltage vector sequences in all regions in each voltage vector are formulated in a table as shown in Table.4.3

SECTOR	REGION	SEQUNCE OF VECTORS
1	1	ONN,OON,OOO,POO,POO,OOO,OON,ONN
	2	ONN,PNN,PON,POO,POO,PON,PNN,ONN
	3	POO,PON,OON,ONN,ONN,OON,PON,POO
	4	OON,PON,POO,PPO,PPO,POO,PON,OON
2	1	PPO,OPO,OOO,OON,OON,OOO,OPO,PPO
	2	PPO,PPN,OPN,OON,OON,OPN,PPN,PPO
	3	OON,OPN,OPO,PPO,PPO,OPO,OPN,OON
	4	OPO,OPN,NPN,NON,NON,NPN,OPN,OPO
3	1	NON,NOO,OOO,OPO,OPO,OOO,NOO,NON
	2	NON,NPN,NPO,OPO,OPO,NPO,NPN,NON
	3	OPO,NPO,NOO,NON,NON,NOO,NPO,OPO
	4	NOO,NPO,NPP,OPP,OPN,NPN,NPO,NOO
4	1	OPP,OOP,OOO,NOO,NOO,OOO,OOP,OPP
	2	OPP,NPP,NOP,NOO,NOO,NOP,NPP,OPP
	3	NOO,NOP,OOP,OPP,OPP,OOP,NOP,NOO
	4	OOP,NOP,NNP,NNO,NNO,NNP,NOP,OOP

5	1	NNO,ONO,OOO,OOP,OOP,OOO,ONO,NNO
	2	NNO,NNP,ONP,OOP,OOP,ONP,NNP,NNO
	3	OOP,ONP,ONO,NNO,NNO,ONO,ONP,OOP
	4	ONO,ONP,PNP,POP,POP,PNP,ONP,ONO
6	1	POP,POO,OOO,ONO,ONO,OOO,POO,POP
	2	POP,PNP,PNO,ONO,ONO,PNO,PNP,POP
	3	ONO,PNO,POO,POP,POP,POO,PNO,ONO
	4	POO,PNO,PNN,ONN,ONN,PNN,PNO,POO

Table.4.3. Switching Patterns in all regions and sectors

Simulation results of 3-Level Inverter Using SVM:

Figure (3.17-a) shows the line to line voltage and figure3.17-b shows line current and its harmonic spectrum of three level inverter using space vector modulation.

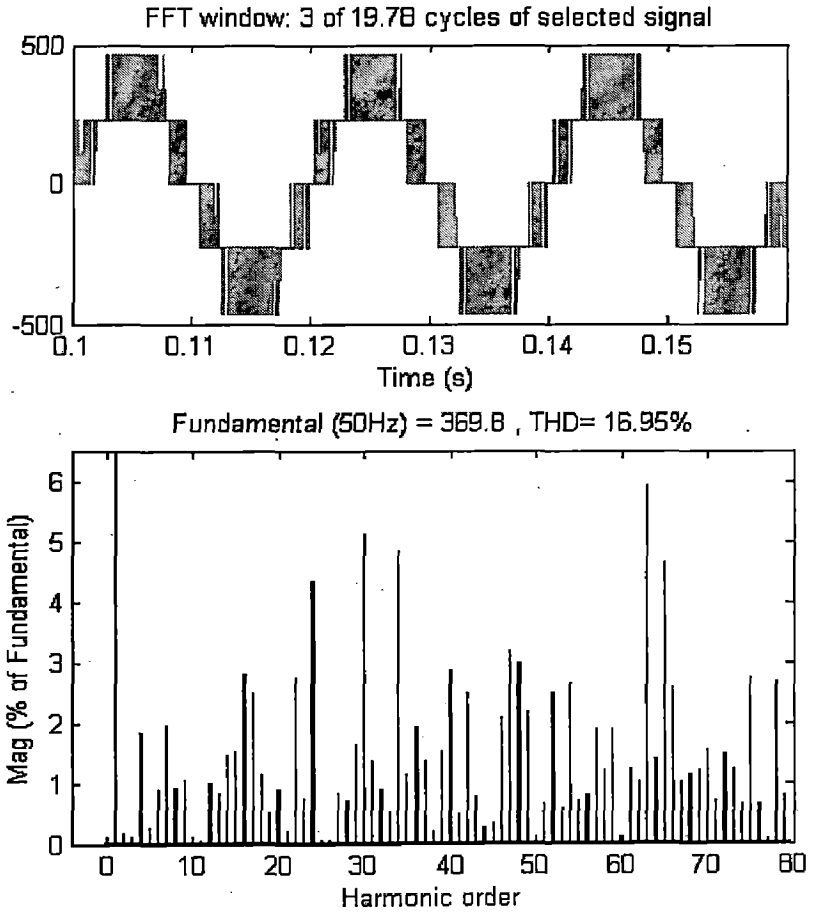


Fig (3.17-a)Line to Line Voltage and Harmonic spectrum at f=50HZ and MI=0.866

STATCOM USING MULTI LEVEL INVERTER

4.1 INTRODUCTION:

Recent advances in the power handling capabilities, of which static switches has made the use of the voltage source inverters (VSI) feasible at both the transmission and distribution levels. As a result, a variety of VSI based equipment such as the static compensators (STATCOM) are used to make flexible AC transmission systems (FACTS) possible [2]. It is well-known that there has been a large demand for high-power, high-voltage static var compensator (SVC) systems to regulate and stabilize transmission lines and to compensate industrial lagging loads

The ability of these FACTS equipments to control reactive power system as well as to improve system stability may need to use VSI with high voltage and high power capabilities. This is not possible for a two-level inverter, as the semiconductor devices must be connected in series to obtain the required high-voltage operation. The second configuration, the multiphase converter configuration, requires more switching devices and very complex transformer arrays to achieve low harmonics distortion at the output voltage. The third approach, a multilevel topology, can be used either to eliminate or minimize lower order harmonics while increasing the overall rating of the SVC.

In the earlier SVC's, multi-inverter systems for large-scale reactive power compensation are developed because of the lack of high-power, self-commutated semiconductor switches and the desire to reduce the harmonics[1]. These inverters are made up of problematic series parallel connections with special transformer arrangements in order to reduce the harmonic contents caused by each inverter. Because of the number of inverter stages or harmonic filter legs, however, such an SVC system becomes expensive, complicated, and large in volume, and suffers from resonances created by peripheral harmonic current sources. So pulse-width modulation (PWM) voltage source inverters with high switching frequency for reactive power compensation is used.

A neutral-point-clamped inverter (NPC inverter, also called three-level inverter) is reported in chapter 3. The three-level inverter has the advantages that the blocking voltage of each switching device is one half of dc-link voltage whereas full dc-link voltage for two-level inverter, and the harmonic contents of 'three-level inverter output voltage are far less than those of two-level one at the same switching frequency. These advantages enable the SVC system using a three-level inverter to be suitable for large scale reactive power compensation.

4.2 BRIEF OVERVIEW OF THE SYSTEM:

The simplified block diagram of the SVC system presented in this paper is shown in figure 4.1. The SVC system consists of a three-level inverter, a set of linked reactors and series- connected dc capacitor tanks, the three-phase loads, and the ac mains [3]. The voltage stress of each switching device is clamped to one half of the dc-link voltage Vdc, whereas full dc-link voltage 2Vdc for two-level conventional inverter and thus power devices could be fully utilized in the high-voltage range. The inverter output voltage waveform Vo is made up of three-state voltages (+Vdc, 0,-Vdc) and thus shows relatively lower harmonic contents in the line currents and requires smaller filter size.

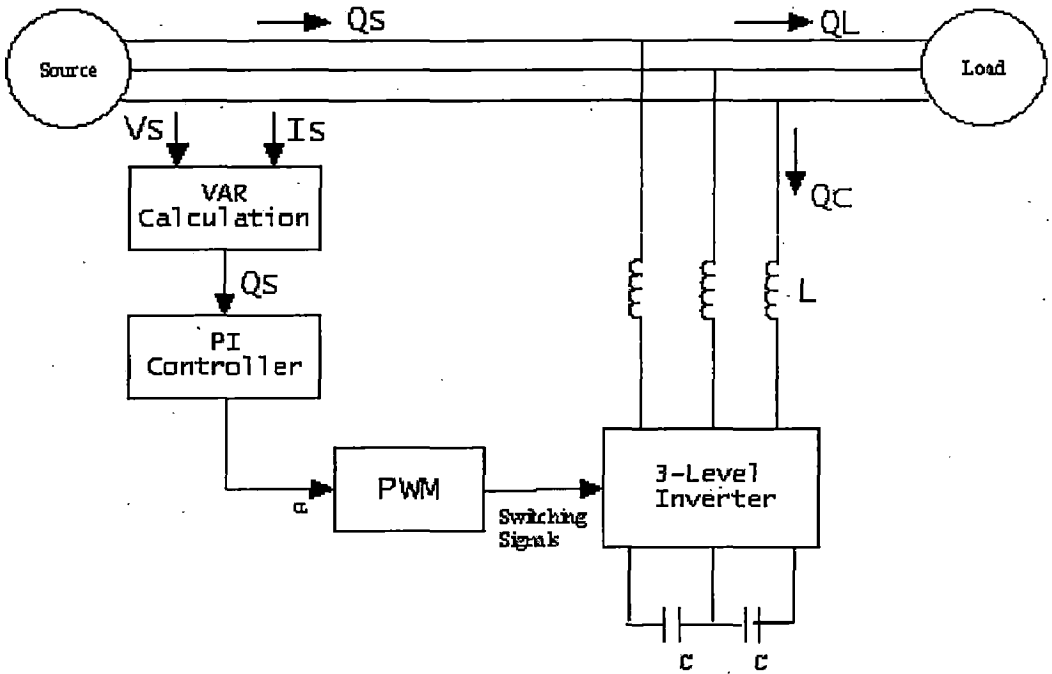
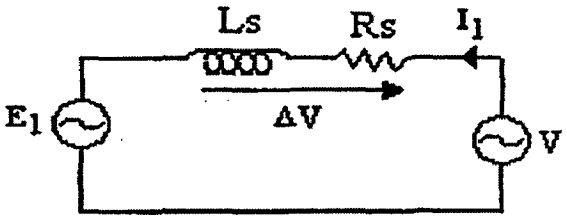


Fig 4.1 Simplified Block Diagram of SVC System with 3-Level Inverter

4.2.1 Operating Principle of STATCOM System

The operating principles of the SVC system can be explained by considering the per phase fundamental equivalent circuit of the SVC systems [4]. An equivalent voltage source Voa1 is connected to the ac mains through a linked reactor *(L)* and a resistor *(Rs)* representing the total losses in the inductor, including the inverter, as shown in figure 4.2. By controlling the phase angle 'α' of the inverter output voltage with respect to the phase of source voltage, the dc capacitor voltage Vdc can be changed. Thus, the amplitude of the fundamental component of the inverter output voltage Vreal can be controlled.



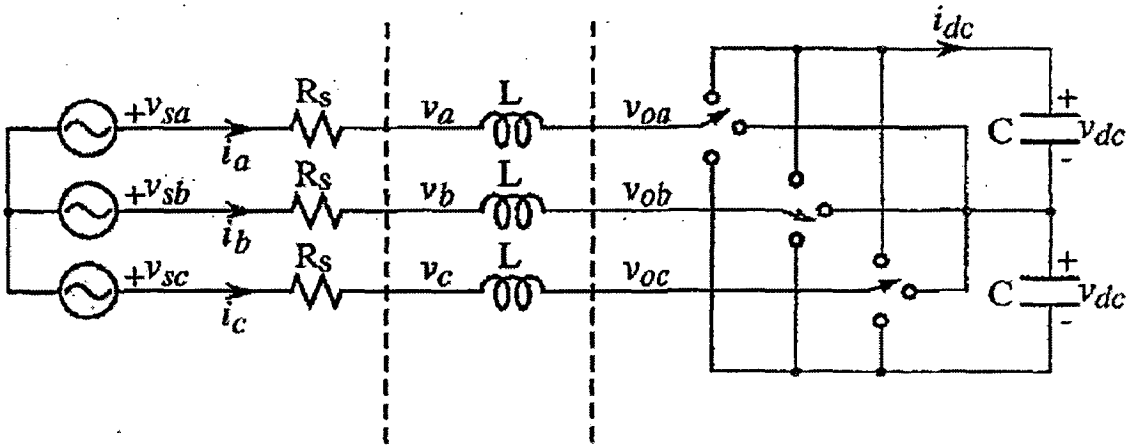


Fig 4.2 Simplified Circuit of STATCOM

As already said by controlling the phase angle 'α' of the inverter output voltage and dc capacitor voltage Vdc can be changed from that view Figure4.3 shows the phasor diagram for leading (capacitive) and lagging (inductive) var generation, respectively.

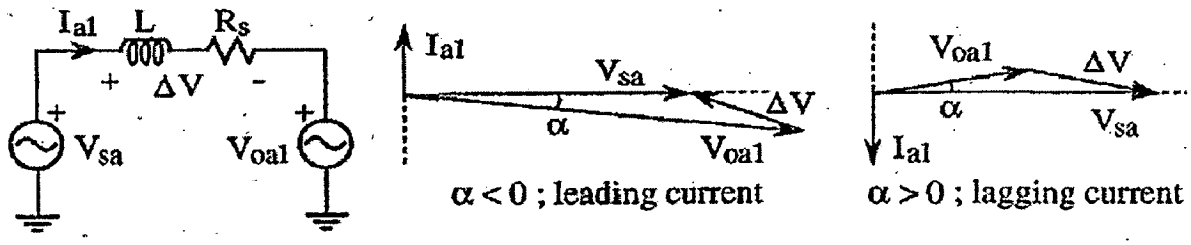


Fig 4.3 Per phase fundamental equivalent circuit, Phasor diagrams for providing leading and lagging VARs

The line current flowing into or out of the VSI is always at 90 degrees to main voltage due to reactive coupling. When the fundamental of the inverter voltage is less than the main voltage, reactive power is absorbed by the STATCOM. On the other hand, when the STATCOM voltage is higher than the main voltage, reactive power flows from the STATCOM to the mains [5]. The magnitude of the reactive power absorbed or supplied by the STATCOM depends on the DC-side capacitor voltage. Adjusting the real power transfer between the STATCOM and the system can control this voltage. If the inverter output voltage Voa1 leads the main voltage Vsa by angle 'α', the capacitor voltage decreases, and it will increase when the inverter output voltage Voa1 lags the main voltage Vsa. By controlling the phase angle 'α' of the inverter, the DC capacitors voltages levels cab be changed. Thus, the amplitude of the fundamental component Voa1 can be controlled, as shown in figure.5.3.

The characteristics of STATCOM system in steady state can be obtained easily by calculating the active power P and reactive power Q in DQ model so the voltages and currents in source side load side and STATCOM has converted from abc to DQ frame. Calculated active and reactive power in DQ frame is shown in below equations [4]

$$Pc = V_{sq}I_q + V_{sd}I_d = \frac{V_s^2}{2R_s}\{1-2\cos(\alpha)\}$$

$$Qc = V_{sq}I_d - V_{sd}I_q = \frac{V_s^2}{2R_s}\{\sin 2\alpha\}$$

4.2.2 Closed Loop Implementation of STATCOM with PI Controller:

The STATCOM control scheme is illustrated in the block diagram of figure 4.4. This circuit consists of a PI controller and switching pattern device to produce the switching signals. The source voltage and the STATCOM's current are transformed in the DQ frame for calculating the reactive power generated by the system. This is compared to the reactive power reference [3]. The PLL detect the phase angle of the supply voltage which is added to the control variable 'α' output of the PI controller. This sum in transient state gives to PWM generated circuit where the inverter states switches are calculated and is given to 3-Level Inverter for controlling the reactive power.

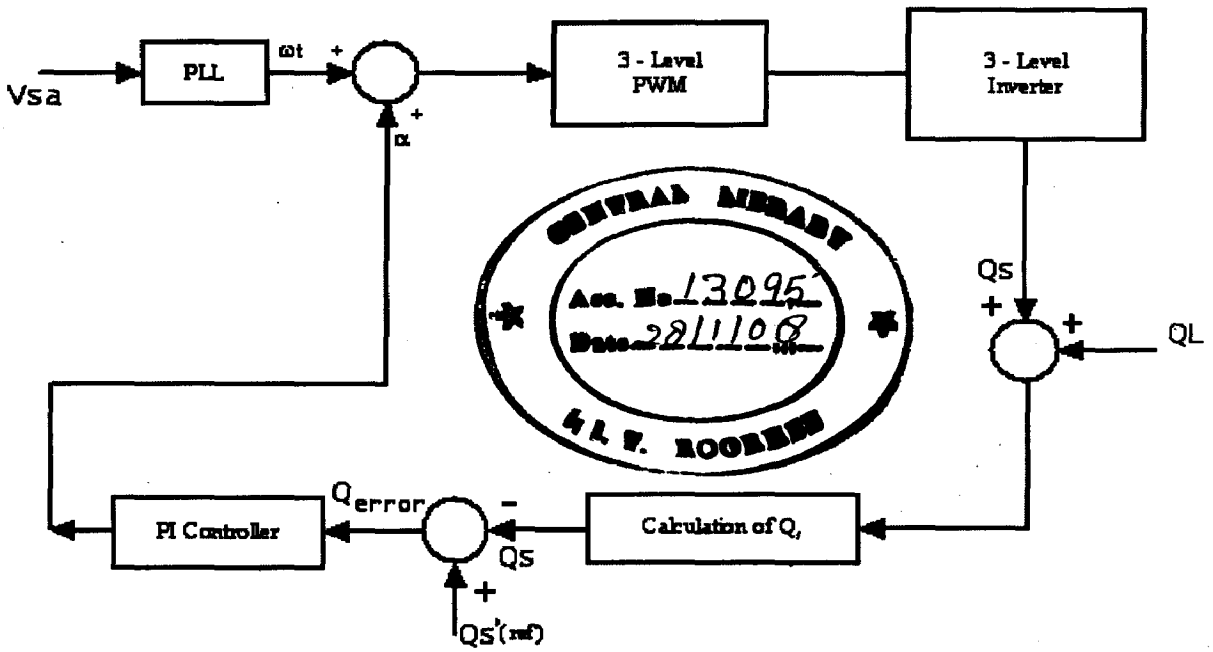


Fig 4.4 Implementation of closed loop STATCOM system with PI controller

4.2.2.1 PI Controller:

The controller can be designed in order that the StaticVar compensator system has fast dynamic characteristics. Figure 4.5 shows the control block diagram of the system constructed by PI controller [3]. From block diagram input to the controller is taken from the reactive power error calculated between source Var and reference Var. Here the

source Var calculated which is equivalent to the sum of reactive powers caluculated by load and the reactive power calculated from 3-Level Inverter. The circuit parameters of STATCOM system is shown in APPENDIX.A

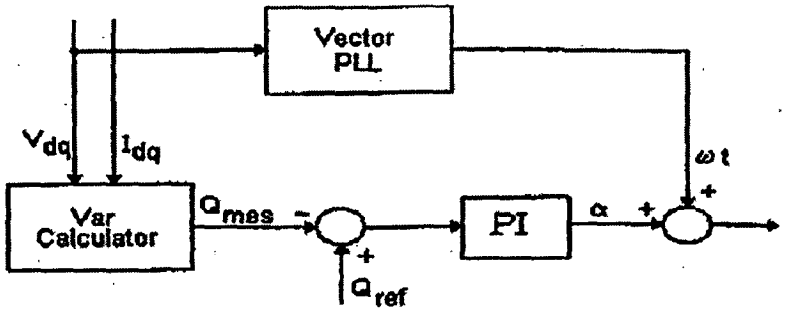


Fig 4.5 Control block diagram with PI controller

The transfer function of PI controller is given below.

$$Gc(s) = Kp + Ki / s$$

To achieve fast dynamic response of the closed-loop system with the circuit parameters given in Table 5.1, the control parameters are determined as follows

$$Kp = 3.2 \text{ e-}5 ;$$

$$Ki = 2.7 \text{ e-}4 ;$$

Simulink block diagram of STATCOM using Multi level Inverter with PI controller:

Simulation of STATCOM using 3-Level Inverter has done on the MATLAB 7.0.1. In this the control technique used is sinusoidal pulse width modulation for generating the pulses from there the system has been controlled as the pulse width can be controlled by closed loop operation of STATCOM. Input coming from the PI controller is angle of small value which has added to source phase angle, and then the sum is converter into 3-phase source of phase shift 120 degrees.

The overall system block diagram is shown in figure 4.6 below

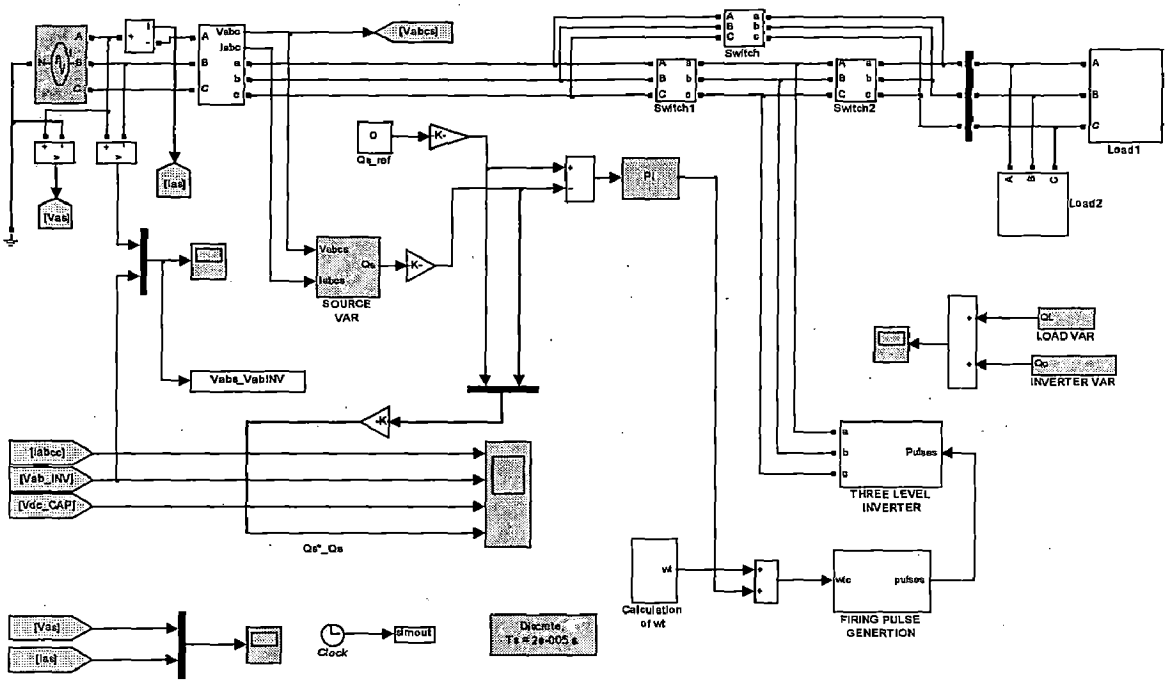


Fig 4.6 Simulink block diagram of STATCOM using 3-Level Inverter using PI controller

Figure4.7 shown is used to find the reactive power

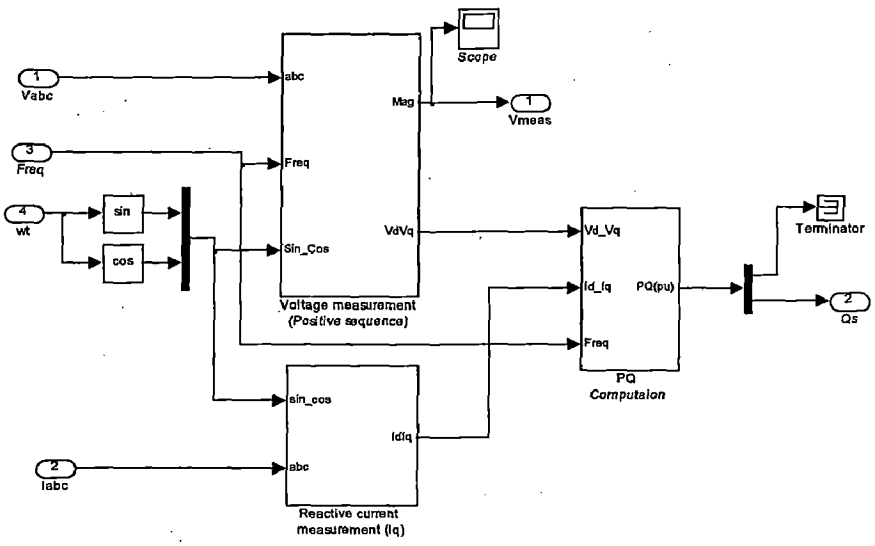


Fig 4.7 Block diagram for reactive power

Figure 4.8 shows the simulation block diagram of firing pulse generation in phase 'a'.

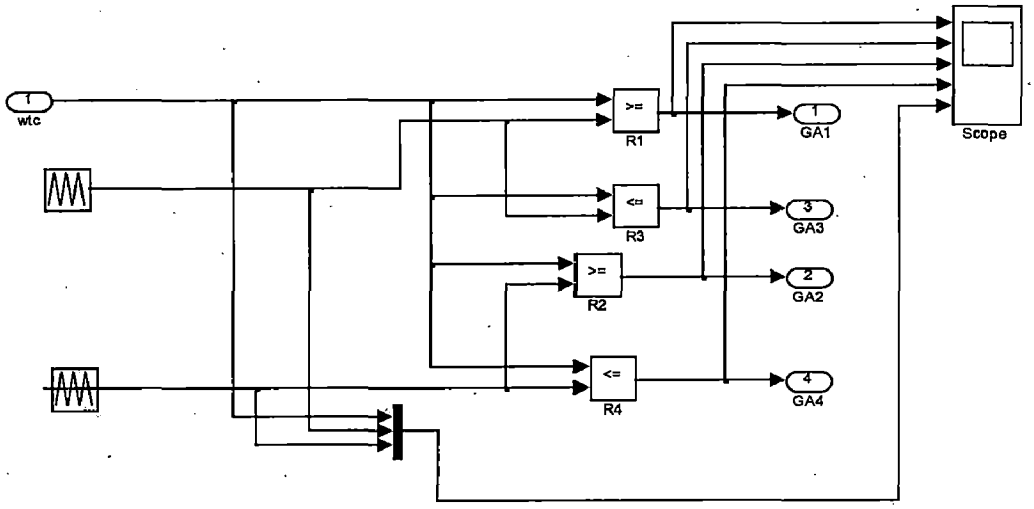


Fig 4.8 Firing Pulse generation in Phase A

4.2.2.2 FUZZY Controller:

During the past several years, fuzzy control has emerged as one of the most active and fruitful areas for research in the applications of fuzzy set theory, especially in the realm of industrial processes, which do not lend themselves to control by conventional methods because of a lack of quantitative data regarding the input-output relations. Fuzzy control is based on fuzzy logic-a logical system which is much closer in spirit to human thinking and natural language than traditional logical systems. The fuzzy logic controller (FLC) based on fuzzy logic provides a means of converting a linguistic control strategy based on expert knowledge into an automatic control strategy [6].

Figure 4.9 shows the basic configuration of an FLC, which comprises four principal components:

Fuzzification Interface: Rule base: Decision making: Defuzzification interface

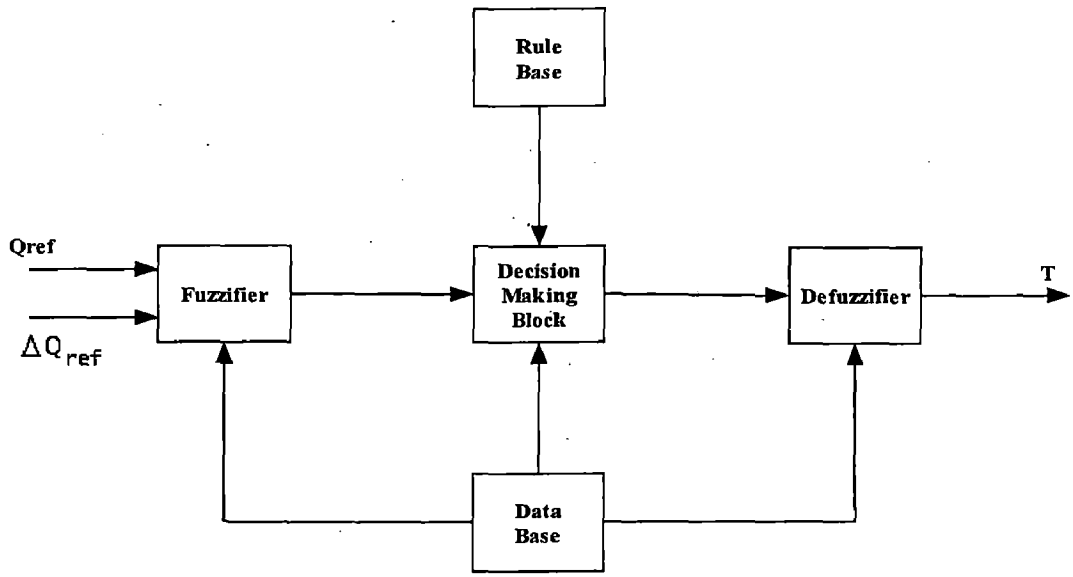


Fig 4.9 Basic configuration of fuzzy logic controller

Design Parameters of the FLC:

The principal design parameters for an FLC are the following

1) Fuzzification strategies and the interpretation of a fuzzification operator (fuzzifier)

2) Data base:

   a) Discretization/normalization of universes of discourse

   b) Fuzzy partition of the input and output spaces

   c) Completeness

   d) Choice of the membership function of a primary fuzzy set

3) Rule base:

   a) Choice of process state (input) variables and control (output) variables of fuzzy control rules

   b) Source and derivation of fuzzy control rules

   c) Types of fuzzy control rules, d) consistency, interactivity, completeness of fuzzy control rules

4) Decision making logic:

   a) Definition of a fuzzy implication,

   b) Interpretation of the sentence connective

c) Interpretation of the sentence connective

d) Definitions of a compositional operator

e) Inference mechanism

5) Defuzzification strategies and the interpretation of a defuzzification operator

Fuzzy Partition of Input and Output Spaces:

A linguistic variable in the antecedent of a fuzzy control rule forms a fuzzy input space with respect to a certain universe of discourse, while that in the consequent of the rule forms a fuzzy output space. In general, a linguistic variable is associated with a term set, with each term in the term set defined on the same universe of discourse. A fuzzy partition, then, determines how many terms should exist in a term set. This is equivalent to finding the number of primary fuzzy sets. The number of primary fuzzy sets determines the granularity of the control obtainable with an FLC.

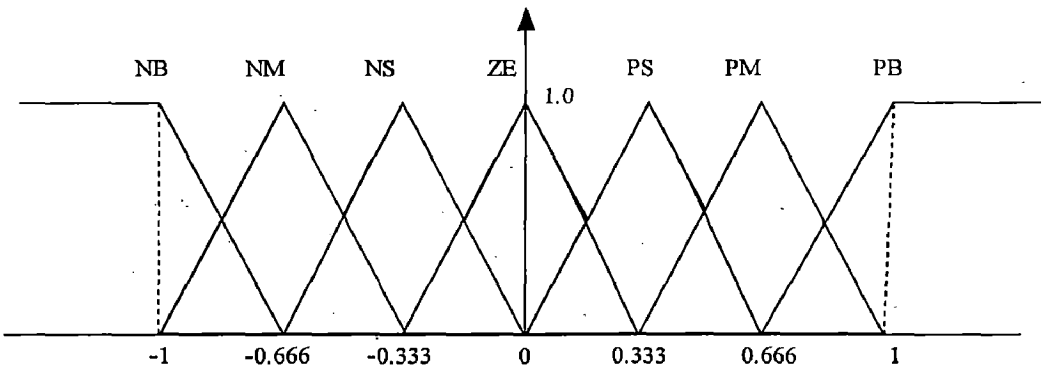


Fig 4.10 Finer fuzzy partition with seven terms: *NB*, negative big; *NM*, negative medium; *NS*, negative small; *ZE*, zero; *PS*, positive small; *PM*, positive medium; and *PB*, positive big.

Figure 4.10 Two fuzzy partitions in the same normalized universe[-1, +1]. Membership functions having the forms of triangle-shaped and trapezoid shaped functions are used here. Since a normalized universe implies the knowledge of the input/output space via appropriate scale mappings, a well formed term set can be achieved.

		E						
		NB	**NM**	**NS**	**ZE**	**PS**	**PM**	**PB**
	NB	NB	NB	NM	NM	NS	NS	ZE
	NM	NB	NB	NM	NS	NS	ZE	PS
ΔE	**NS**	NB	NB	NS	NS	ZE	PS	PM
	ZE	NB	NM	NS	ZE	PS	PM	PB
	PS	NM	NS	ZE	PS	PS	PB	PB
	PM	NS	ZE	PS	PS	PM	PB	PB
	PB	ZE	PS	PS	PM	PM	PB	PB

Table 4.1 Rule base table for error E and change in error ΔE

Table4.1 is used based on the rules that fuzzy controller follow. The error E and change in error ΔE should be in between 1and (-1). Membership functions having the forms of triangle-shaped and trapezoid-shaped functions are used here. Since a normalized universe implies the knowledge of the input/output space via appropriate scale mappings, a well-formed term set can be achieved as shown. If this is not the case, or a non normalized universe is used, the terms could be asymmetrical and unevenly distributed in the universe.

Simuation block diagram STATCOM using fuzzy controller:

Figure 4.11 is a simulink block diagram of STATCOM using fuzzy controller. In fuzzy controller Kp (proportional const) and Ki (Integral const) has been used for tuning the system to produce smooth response of the required output and to reduce the overshoots. Here the saturator in the input side of the fuzzy controller is put to limit input between 1 and -1. Fuzzy controller constants are shown in APPENDIX.A

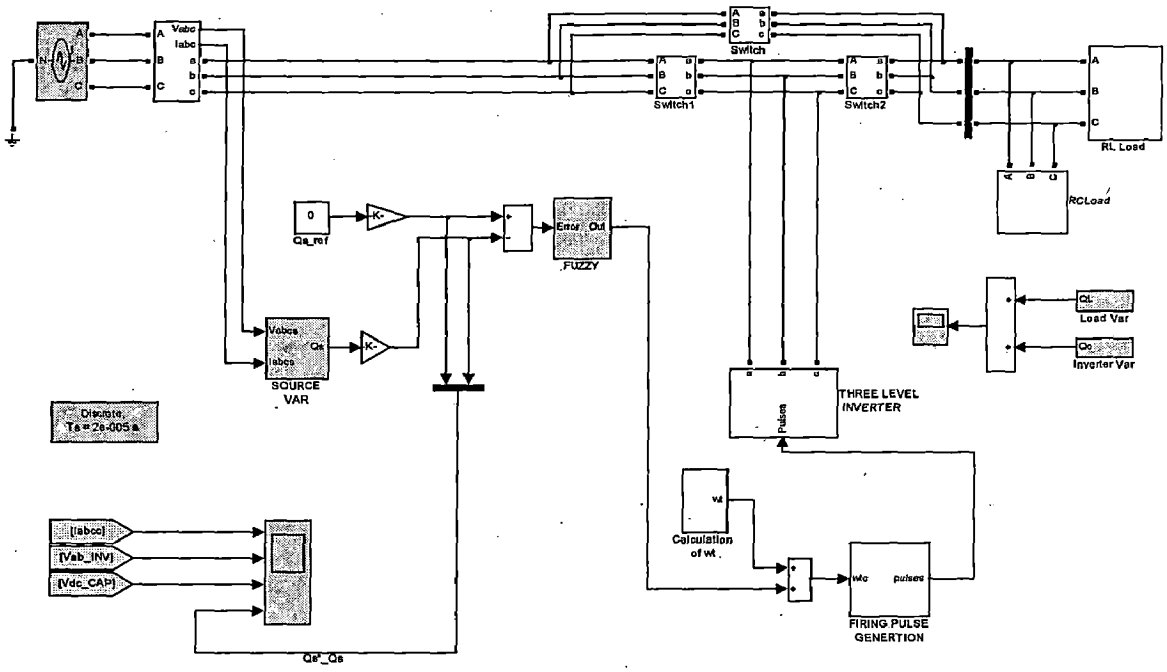


Fig 4.11 Simulink block diagram of STATCOM using fuzzy controller

Block diagram fuzzy controller is shown in figure 4.12

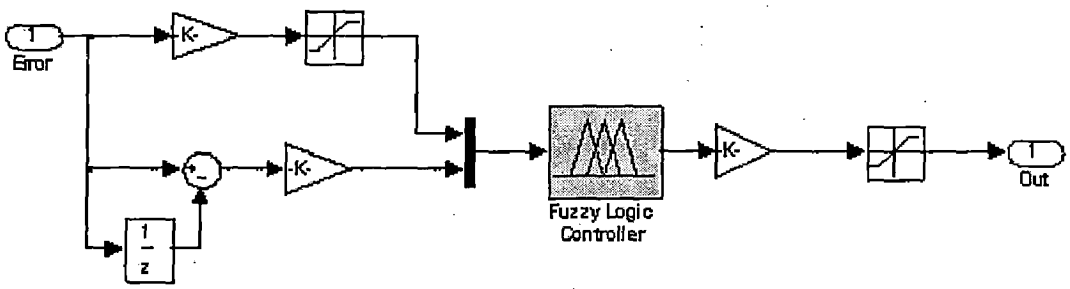


Fig 4.12 Block diagram of fuzzy controller

4.2.2.3 Fuzzy Pre compensated PI controller:

The block diagram fuzzy pre compensated PI controller is shown in figure4.13. Here the error and change in error of a control variable is given to the fuzzy controller and the output of fuzzy controller is added to reference value then that is compared with actual value. The output coming from that comparator i.e. error is given to the PI controller. PI and FUUZY constants are shown in APPENDIX.A

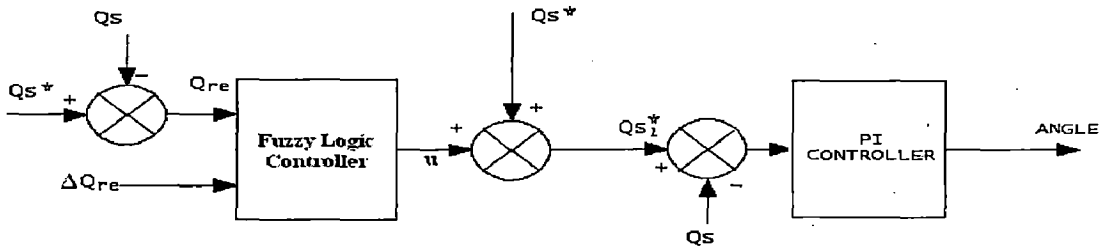


Fig 4.13 Block diagram fuzzy pre compensated pi controller

CHAPTER - V

RESULTS AND DISCUSSIONS

In this chapter, simulation results of STATCOM system using multi level inverter are presented. The performance of static compensator is investigated for inductive and capacitive load conditions both during transient and steady state conditions. Also, their affect on the inverter output voltage is observed. The source reactive power response for different controllers is studied.

5.1 RESULTS OF STATCOM WITH PI CONTROLLER:

The simulation results fort reactive power compensation using three level inverter for the model shown in figure 4.6 are given below. The performance of the STATCOM is investigated for different loading conditions. First, the simulation is made to run without using STATCOM with an inductive load. Static compensator is switched on after some time. This compensates the reactive power. After reaching the steady state conditions the inductive load is switched off and capacitive load is switched on.

Figure 5.1 shows the plot of the source reactive power for changes in the load. The reactive power shown figure is in per unit with base value of 100 KVAR. Initially, STATCOM is switched on for an inductive load. During the transient period, the source also supplies reactive power to the compensator. Hence, there is an increase in the reactive power in the initial period. The static compensator then supplies the required reactive power to the load, thus making the source reactive power follow the zero reference. Similarly, after some time the inductive load is replaced by a capacitive load. For this condition also, static compensator acts in such a way that it takes leading VARs from the load.

Figure 5.2 shows the plot of source voltage and current with out static compensator for an inductive load and figure 5.3 with static compensator. It is clear from these waveforms that there is a phase difference between the source voltage and current without static compensator. The phase difference gradually decreases and reaches zero with the STATCOM in operation.

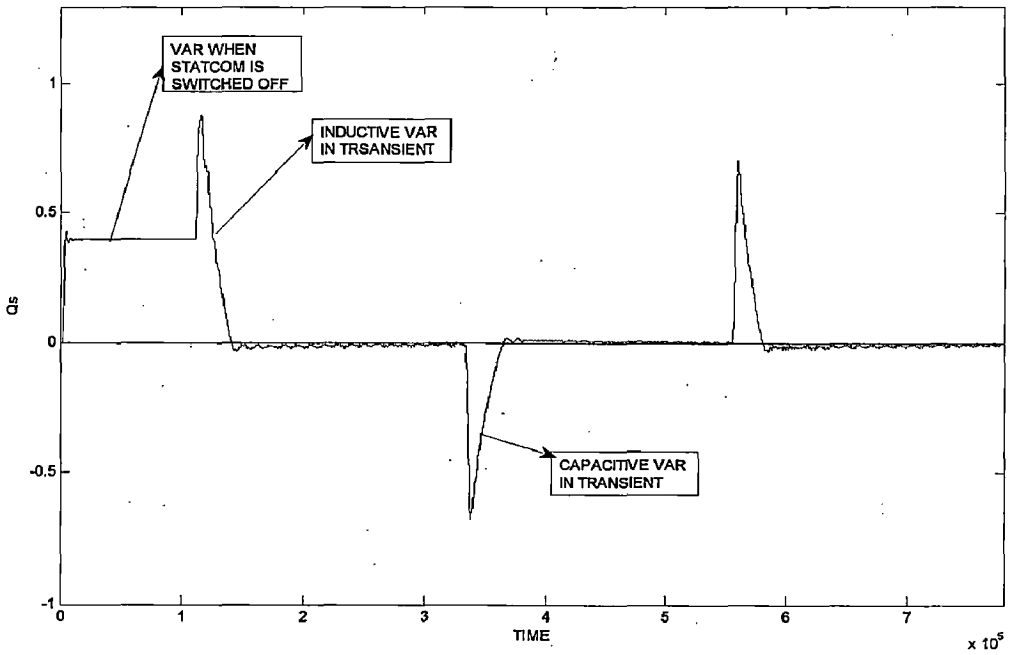


Fig 5.1 Source and reference reactive power plot

At this instant voltage and current wave forms of source is shown in figure5.2. Since load is inductive source current lags the voltage by some angle.

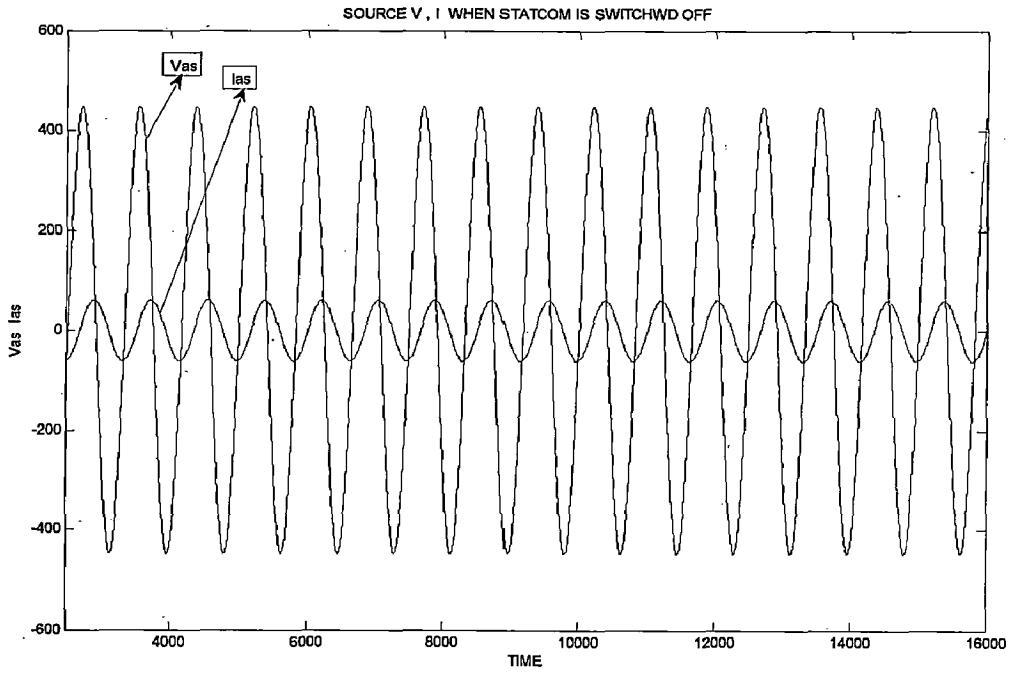


Fig 5.2 Source voltage and current when STATCOM is switched off

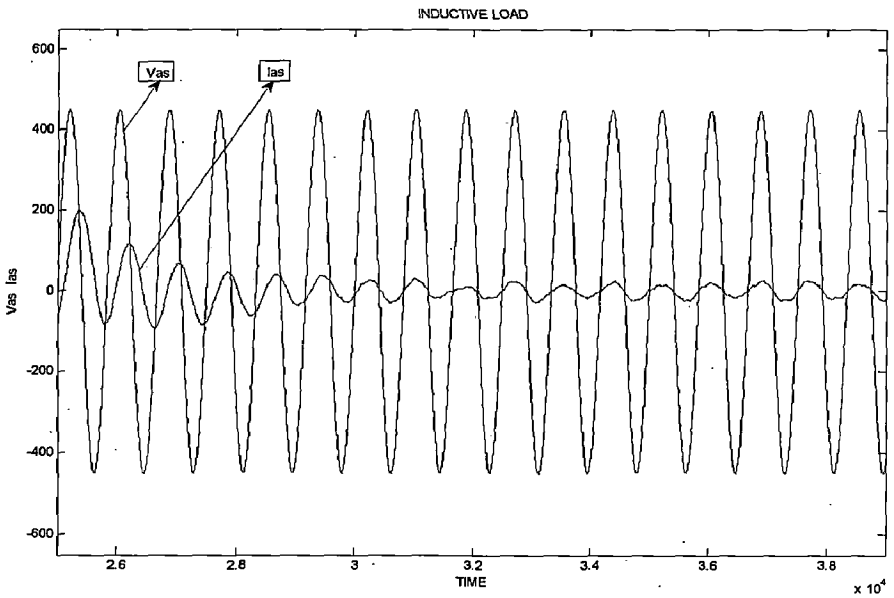


Fig 5.3 Source voltage and current when STATCOM is switched on and during Inductive load

Figure 5.4 shows the waveforms for the three level inverter output voltage and source voltage for an inductive load. The magnitude of the inverter output voltage is more for this load condition because it has to supply the required reactive power to the load.

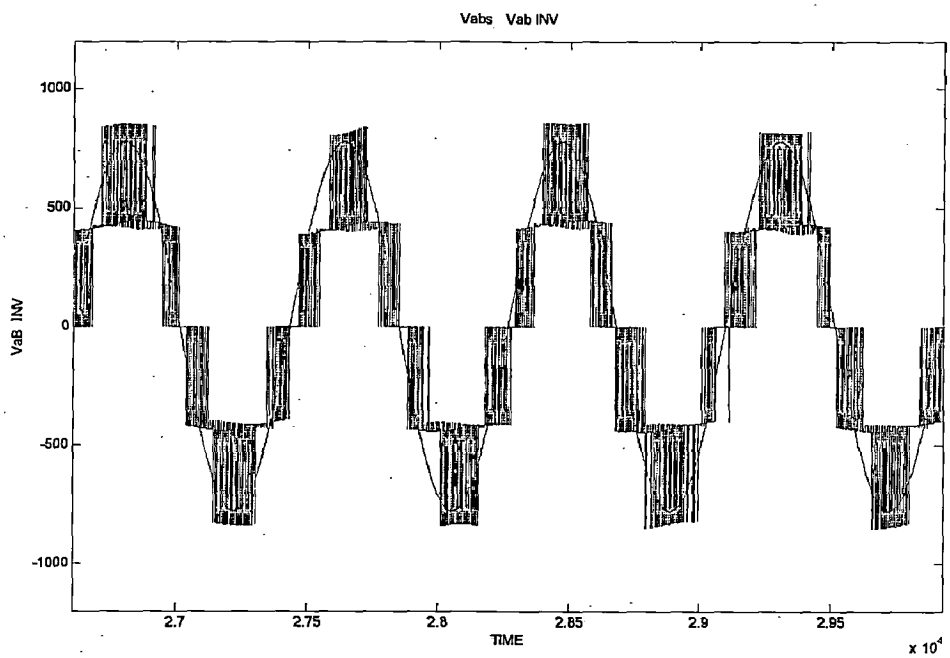


Fig 5.4 Inverter output L-L voltage and source voltage during inductive load

Figure 5.5 shows the source voltage and current waveforms when a capacitive load is switched on replacing an inductive load. The change in phase difference can be observed from transient state to steady state. Figure 5.6 shows the waveforms for the three level inverter output voltage and source voltage for a capacitive load. The magnitude of the inverter output voltage is less for this load condition because it has to absorb the required reactive power from the load.

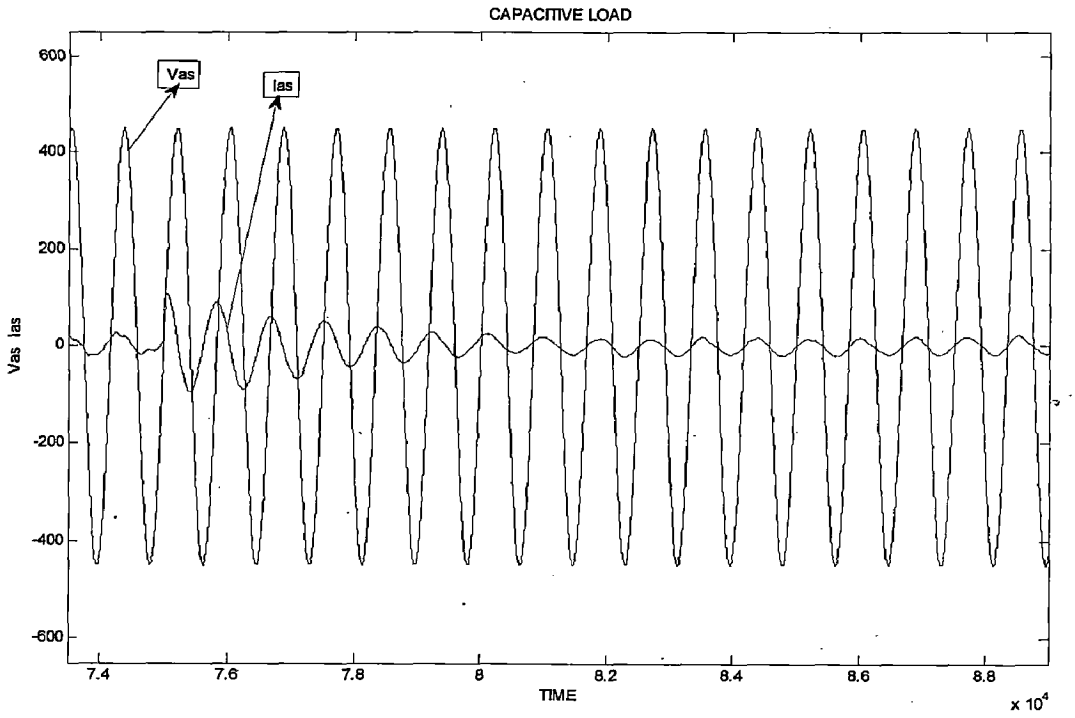


Fig 5.5 Source voltage and current when STATCOM is switched on and during capacitive load.

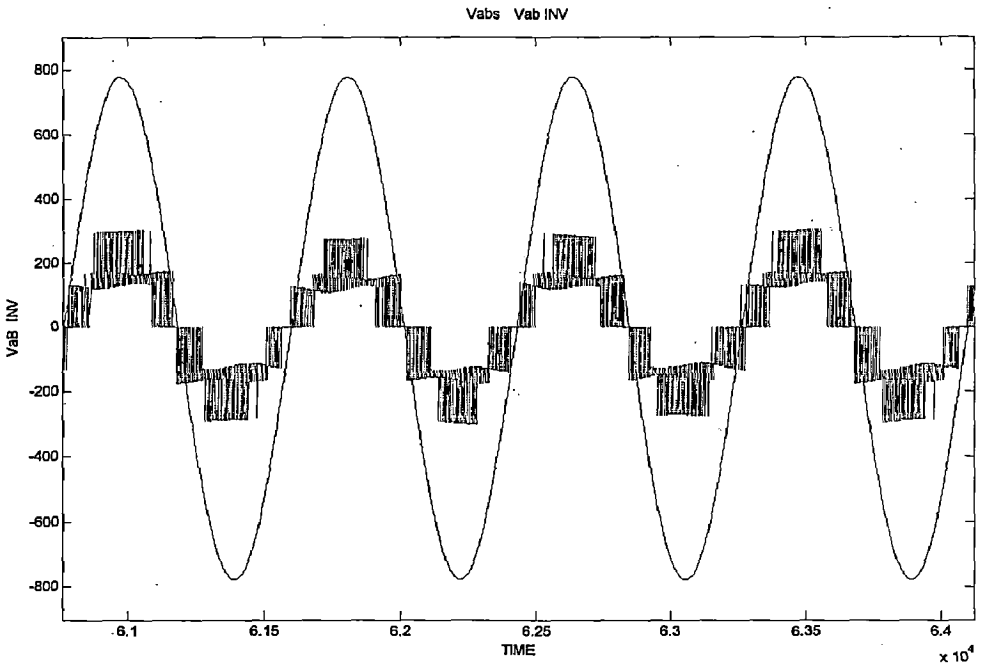


Fig 5.6 Inverter output L-L voltage and source voltage during capacitive load

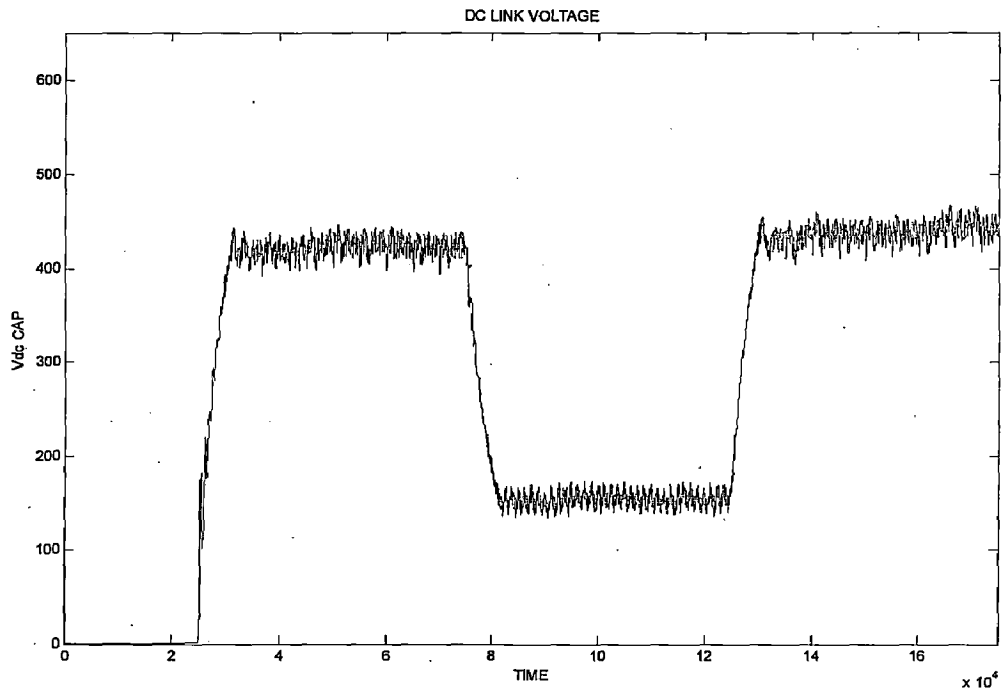


Fig 5.7 DC link capacitor voltage of 3-Level Inverter

Figure 5.7 shows the dc link capacitor voltage for variations in the load. At the initial stage dc link capacitor voltage is zero, since STATCOM is switched off, after that when STATCOM is switched on and load is of inductive type dc link capacitor produces dc voltage. This voltage depends on the phase angle obtained from the PI controller which controls the overall system..

5.2 RESULTS OF STATCOM WITH FUZZY CONTROLLER:

Figure 5.8 shows the control of reactive power with fuzzy controller for different load conditions. The operation of the system is same as that with a PI controller. The loading conditions are repeated in the same fashion. The over shoots in the reactive power response are reduced with fuzzy controller which is clear from the figure. But, the settling time for a fuzzy controller is more. Figure 5.9 shows the dc link capacitor voltage for variations in the load using fuzzy controller. Figure 5.10 shows the source voltage and current waveforms when a capacitive load is switched on replacing an inductive load using fuzzy controller.

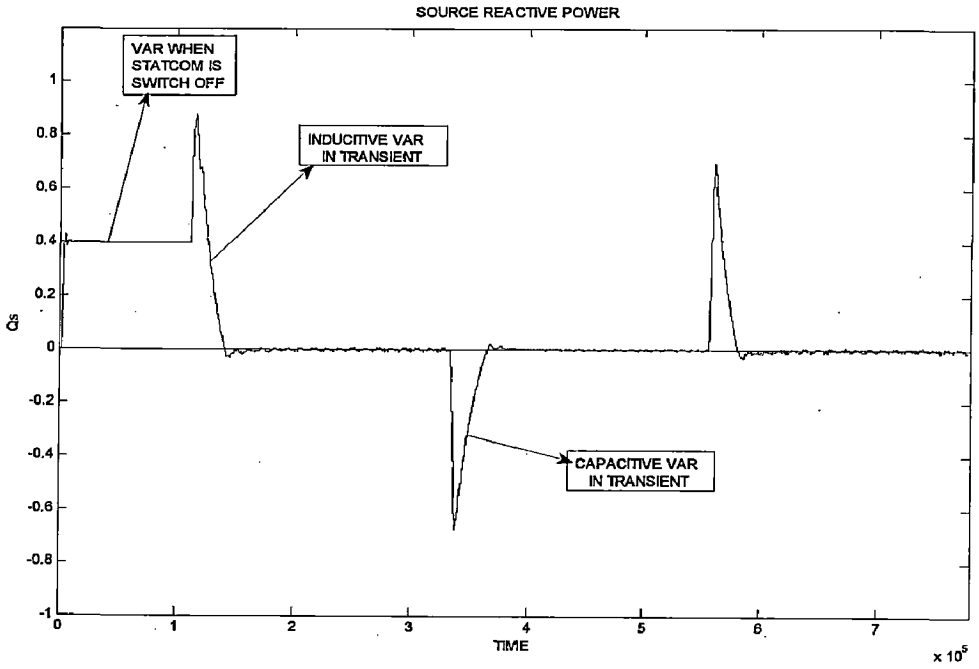


Fig 5.8 Source and reference reactive power plot using fuzzy controller

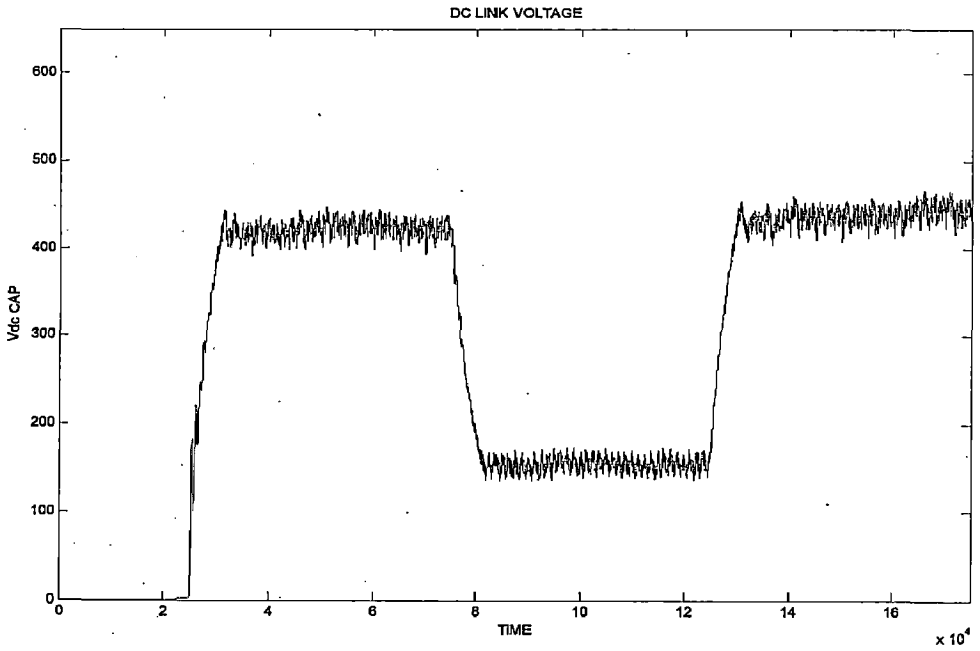


Fig 5.9 DC link capacitor voltage of 3-Level Inverter

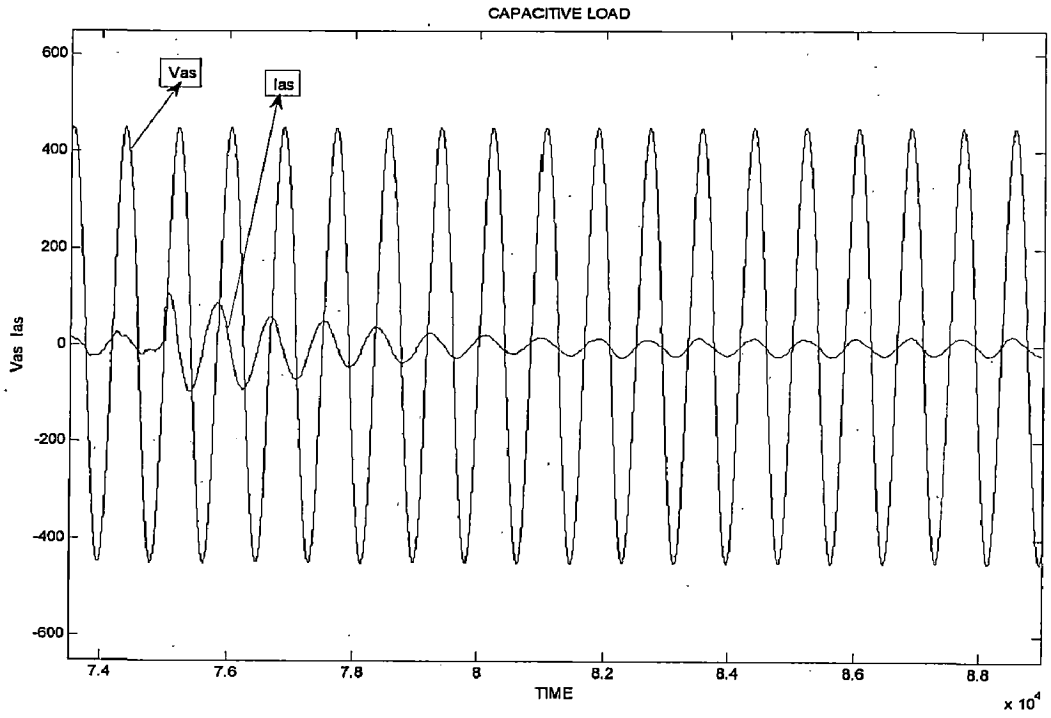


Fig 5.10 Source voltage and current when STATCOM is switched on and during capacitive load.

5.3. FUZZY PRECOMPENSATED PI CONTROLLER RESULTS:

Source reactive power control using fuzzy pre-compensated PI controller is shown in figure 5.11. The response for reactive power control for different loads is shown. Compared with other controllers, this controller gives the best performance .Over shoots are reduced significantly. The rise time and settling time are reduced.

Using this controller, the steady state error compared with other controllers is reduced .In this configuration, the controller output has less peak overshoot. Figure 5.11 shows response for the reactive power for different loading conditions using fuzzy pre compensated PI controller and figure 5.12 shows the dc link capacitor voltage.

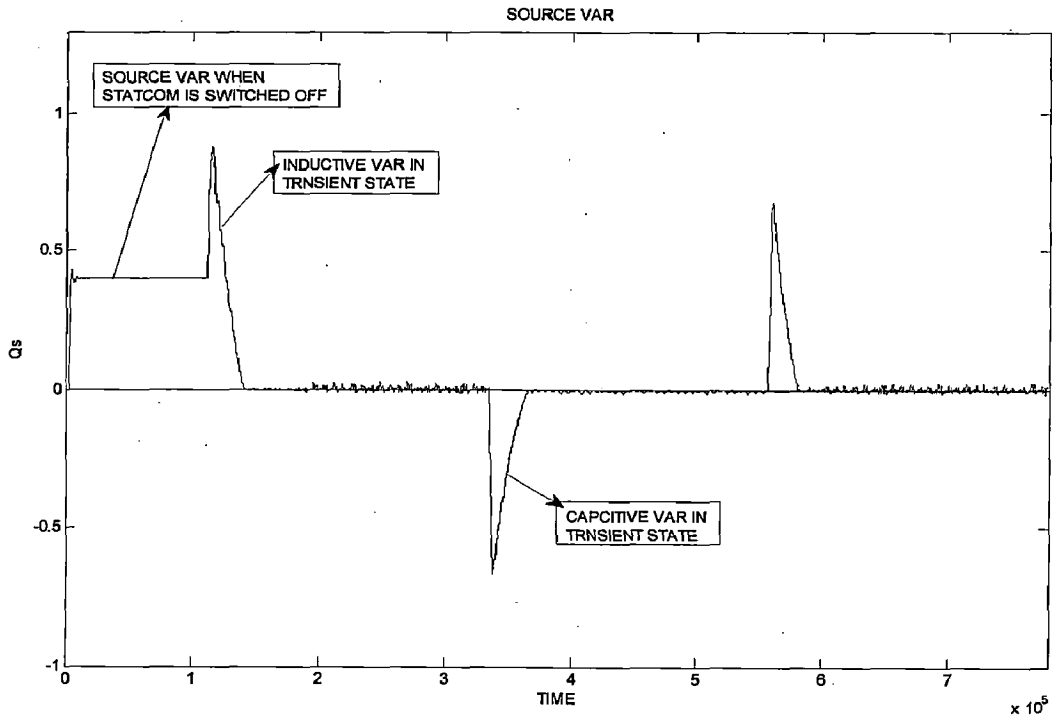


Fig 5.11 Source and reference reactive power plot using fuzzy pre compensated PI Controller

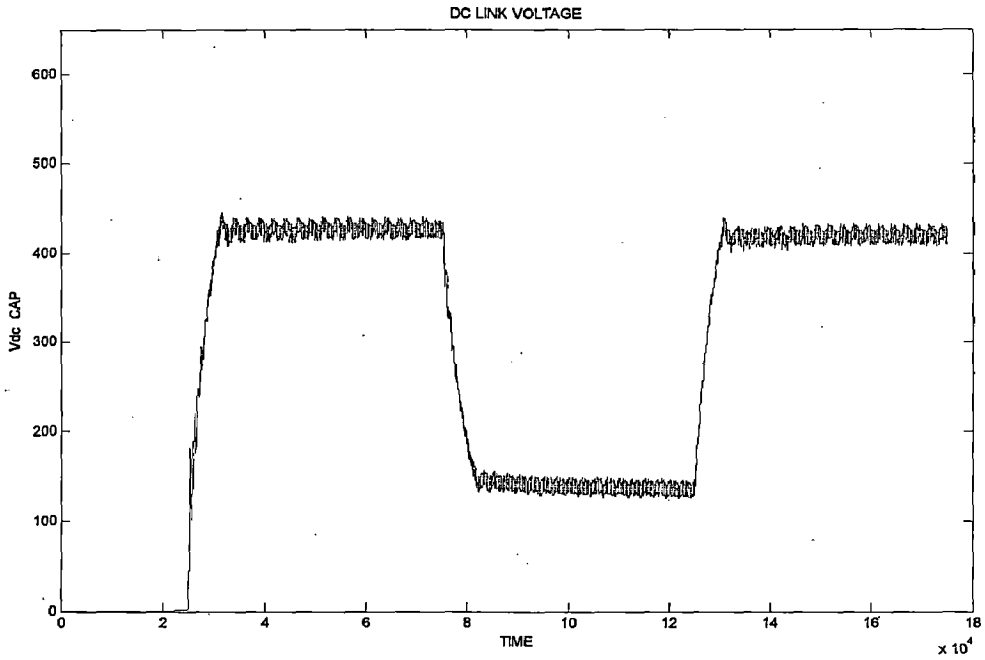


Fig 5.12 DC link capacitor voltage of 3-Level Inverter

CHAPTER 6

CONCLUSION

Reactive power compensation is one of the most important actions for control of power systems on transmission and distribution level. It allows better stability of overall system, decreases losses and permits to maintain better voltage profile. Multilevel power inverters were developed in order to overcome the problems of PWM inverters and this is the reason that they have gained attention in recent years.

Simulation of multilevel inverters was carried using sinusoidal pulse width modulation and space vector modulation. The space-vector PWM (SVPWM) method is an advanced, computation-intensive PWM method and is possibly the best among all the PWM techniques. Because of its superior performance, it is finding widespread application in recent years. THD for SPWM and SVM were compared.

Simulations of STATCOM system with PI controller, Fuzzy controller and Fuzzy pre compensated PI controller were carried. The variation of the phase difference between source voltage and current is observed.

Future Scope :

Performance of Static Compensator using 5- Level inverter can be implemented. The same can be implemented with space vector modulation.

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APPENDIX – A

Circuit Parameters of STSTCOM system:

Meaning	Symbol	Value
Fundamental Frequency	f	50
Fundamental Angular Frequency	ω	2πf [rad/sec]
RMS line to line voltage	Vs	550V
Effective Resistace	Rs	0.4Ω
Linked Reactor	L	10mH
DC side Capacitor	C	1000μf

Controller Constants:

1. **PI Controller:**

   Kp=3.2e-5; Ki=2.7e-4;

2. **Fuzzy Controller:**

   Kfp=3000; Kfi=0.001;

3. **Fuzzy pre compensated PI Controller:**

   Kfp=3000; Kfi=0.001; Kp=3e-5; Ki=0.5e-4;