PERFORMANCE INVESTIGATION ON A MULTILEVEL CONVERTER WITH HIGH INPUT PF

A DISSERTATION

Submitted in partial fulfilment of the requirements for the award of the degree of

MASTER OF TECHNOLOGY

in

ELECTRICAL ENGINEERING

(With Specialization in Power Apparatus and Electric Drives)

By

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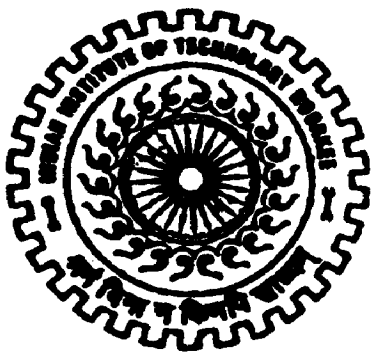

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ROORKEE-247 667 (INDIA)

JUNE, 2005

I.D.No. MT-287/2005-18/NGD-PA-SPS

CANDIDATE'S DECLARATION

I hereby declare that the work, which is being presented in the dissertation entitled "**Performance Investigation on a Multilevel Converter with Unity PF**" in the partial fulfillment of the requirements for the award of degree of M. Tech. in the Power Apparatus and Electric Drives specialization, submitted in the Department of Electrical Engineering, IITR, Roorkee, is an authentic record of my own work carried out under the guidance of **Dr. S. P. Srivastava**, Associate Professor, Elect. Engg. Deptt. and **Dr. Pramod Agarwal**, Professor, Electrical Engg. Deptt, IITR, Roorkee.

The matter embodied in this dissertation has not been submitted by me for the award of any other degree or diploma of this institute or any other university/institute.

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Place: Roorkee

CERTIFICATE

This is to certify that the above statement made by the candidate is correct to the best of my knowledge and belief.

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ACKNOWLEDGEMENTS

I take this opportunity to express my sincere gratitude to **Dr. S. P.Srivastava**, Associate Professor, Electrical Engineering Department and **Dr. Pramod Agarwal**, Professor, Electrical Engineering Department, IITR, for encouraging me to undertake this dissertation work as well as providing me all the necessary guidance and inspirational support throughout this work, without which this work would not have been in its present shape.

I am indebted to my friends specially Mr. P. Siva Krishna and Mr. Deepak Kumar Goyal who took interest in discussing the problem and encouraging me.

Special sincere heartfelt gratitude to my Parents and family members and friends, whose sincere prayer, best wishes, concern, support, unflinching encouragement and thoughtfulness has been a constant source of strength and upliftment to me during the entire work.

I thank all the members of Electrical Engineering Department for their help and encouragement at the hour of need.

Last, but not the least, I thank to Almighty God whose Divine Light provided me guidance, inspiration and strength to complete this work.

(Neeraj Govind Dhopte)

ABSTRACT

The conventional converters have inherent drawbacks like high current harmonics, low power factor and non-sinusoidal line currents. To improve the power factor and reduce the current harmonics, several circuit topologies of the ac to dc converters have been proposed in the past few years. However the conventional converters also have inherent drawbacks like high dv/dt, common mode voltage and high power problems. Multilevel converters are suited for high power, high voltage applications because a greater number of levels are necessitated by advantages of high voltage ratings. Multilevel conversion topologies allows a reduced stress of semiconductor devices and useful in reduction of line harmonics and near unity power factor can be accomplished.

A control topology has been discussed and implemented which operates the multilevel converter (three-level Converter) as an active power filter or rectifier or both at the same time. In rectification mode the converter can supply active power from the DC bus to an output bus, while keeping the input current sinusoidal and with unity power factor. As an active power filter, the converter operates, as a controllable current source injecting the current harmonics required by nonlinear loads. The main problem in multilevel converter is the capacitor voltage balancing. However, the operation of control scheme also maintains the voltages across each capacitor constant and equal.

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the fact that a voltage sine wave (for inverters) or Current sine wave (for rectifiers) can be approximated to a stepped waveform having large number of steps.

Multilevel converters have been developed to overcome the shortcomings in solid state switching device ratings, so that large motors can be controlled by high power adjustable frequency drives. The most popular structure proposed as a transformer less converter is the diode clamped converter based on neutral point converter. The individual devices in multi-level configuration have a much lower dv/dt per switching. The unique structure of multilevel converters allows them to reach high voltages and therefore lower voltage rating devices can be used. As the number of level increases, the synthesized waveform has more steps, producing a very fine staircase and approaching very closely to desired sine wave. It can be understood that as more and more steps are included in the wave form, the harmonic distortion of the output wave decreases, approaching zero as the number of level approaches infinity. Hence multilevel converters are better choice at high power end because the high volt-ampere rating are possible with these converters without the problem of high dv/dt, common mode voltage and other associated ones. The basic three type of multilevel topologies used are

1) Diode-clamped multilevel converter
2) Flying capacitor multilevel converter
3) Series H-bridge multilevel converter

Some of the problems associated with multilevel converters are

1) Difficult and very complex to achieve series redundancy
2) Capacitor voltage balancing
3) More complex PWM control strategy for higher levels
4) Circuit complexity for higher levels
5) Large device count

In spite of these problems, multilevel converters offer a great potential for improving the drive performance in the industry.

1.3 Active Power Filter using Multilevel Converter

Harmonic mitigation in power system is a goal, which has occupied a great deal of research since 1960's. Harmonics are the by-products of modern electronics. They are associated with large numbers of personal computers (single phase load), UPS, variable frequency drives (AC and DC) and any electronic device using a solid state power switching supplies to convert incoming AC to DC. Problems caused by harmonics are as follows,

1) Elevated RMS currents
2) Circuit breaker trips
3) Nuisance fuse operation
4) Reduced equipment life (transformers, conductors, breakers, etc)
5) Equipment malfunctioning
6) High frequency current flow
7) Reduced effective power factor ,and
8) Computer/ telephone may experience interference or failures.

Passive filters are used for harmonics mitigation due to their advantages of simplicity, low cost and easy maintenance. However the disadvantages are

1) The source impedance strongly affects filtering characteristics.
2) As both the harmonic and the fundamental current components flow into filter, the capacity of the filter must be rated by taking into account both currents.
3) When the harmonic current increases the filter can be overloaded
4) Parallel resonance between the power system and the passive filters causes amplification of harmonic currents on the source side at a specific frequency.
5) The passive filter may fall into series resonance with the power system, so that the voltage distortion produces excessive harmonic currents flowing into the passive filter.

Due to these reasons attention of researchers has been drawn to active power filter (APF). Correspondingly pulse width modulated converters with 10kHz of high switching frequency has been used for harmonic compensation and static VAR compensations. However the high initial and running cost are hindering their practical use in power distribution system. In addition it is difficult for the PWM converters to comply with

electromagnetic interference requirements. Due to power handling capabilities of actual power semiconductor devices, these types of active power filter are connected through a coupling transformer to match with the source voltage, thus increasing cost and complexity of the power topology.

However in recent years multilevel converters are rapidly increasing for high power energy conversions for drives and reactive power compensations. Multilevel converters can be connected to high power source without a coupling transformer.

1.4 Objective of Dissertation

In this dissertation a control scheme has been discussed which operates the multilevel converter (three-level converter) as an active power filter or rectifier or both at the same time. At the same time capacitor voltage balancing is also achieved. The objective of this dissertation is as follows:

1) Simulation and hardware implementation of the control scheme, which operates the multilevel converter (three-level converter) as an active power filter and rectifier.
2) Make conclusion from the above analysis.

1.5 Literature Review

Jih-Sheng lai and Fang Zheng in their publication [1] titled," Multilevel converters a new breed of power converters", bring out clearly the working of each of the three basic types of multilevel converters. The potential applications like reactive power compensation, back to back inertie and adjustable speed drives has been presented.

S. J. Finney, A.M. Massoud, and B.W. Williams in their publication [2] titled " A comparison of Three-level converter versus Two-Level Converter for low voltage drives, traction and utility applications", has evaluated three-level topologies as alternative to two–level topologies in medium voltage drives. Topologies, semiconductor losses, filter aspects, part count, initial cost, and life-cycle cost are compared for a grid interface, a Conventional drive application and a high-speed drive application.

M. Basu. S. P. Das. and G. K. Dubey in their presentation [3] titled," Parrallel converter Scheme for high-power active power filters", have proposed a scheme which

connects two converters in parallel with load, ie one is Neutral point clamped multilevel converter and another is VSI converter.

Sun-Kyoung Lim, Jun-Ha Kim and Kwanghee Nam in their publication[4] titled." A DC link Voltage Balancing algorithm for 3-level converter using Zero Sequence current " have given a method of balancing DC link voltage by using the Zero Sequence Current in the flowing in the mid point of DC link For the 3-level Case.

Franco Hernandez C, Luis Moran T, Jose Espinoza C, Juan Dixon R in their publication [5] titled," A Generalized Control Scheme for Active Front End Multilevel Converters", has proposed a generalized control scheme to operate a multilevel converter as an active power filter or rectifier or both at the same time. The main problem in multilevel converters is DC voltage unbalancing . By using this control Scheme the Dc voltage balancing has been achieved.

Sui-Hui , Zou-Ji-Yan, Li Wei-dong in their publication [6] ," A novel Active Power Filter using Multilevel Converter with self voltage balancing", Self balances the voltage across each capacitor. A SPWM control scheme has been used for generation of switching pulses.

Sleven Kincic et. al. in his publication [7] titled ,"Power Factor Correction of single phase and three-phase unbalanced loads using multilevel inverter", proposed the use of multilevel diode clamped VSI for power factor correction.

Bor-Ren Lin, Hsin-Hung Lu, and Shuh-ChuanTsayin their publication [8] titled," Control Technique for high power factor Multilevel Rectifier," proposed three control techniques for a high power factor multilevel pulse-width modulation (PWM) rectifier are proposed. The proposed rectifier is based on series connection of full-bridge cell to achieve a high power factor, low current distortion, low voltage stress of power semiconductors and two balanced output voltages. The look-up table is used in the proposed control schemes to reduce the hardware circuit. A capacitor voltage compensator is used to balance two dc capacitor voltages in order to obtain high quality PWM voltage pattern.

Mario Amrchesoni and Pierluigi Texas in their publication[9] ," Diode Clamped Converters: A Practicable way to balance DC link Voltage", proposes a connection of two multilevel converters ac/dc/ac in back to back connections in which the first

converter act as an rectifier and second as an inverter. This scheme allows the balance of the dc link capacitor voltage and at the same time it offers the Power factor correction capability at the main ac input.

Bor-Ren Lin, Tsuang yu Yang and Yung Chung Lee in their publication [10] titled," Three phase High power Factor Rectifier with unidirectional power flow ," proposes a three phase multilevel rectifier with reduced number of power switches. Six switches are used instead of twelve switches. A control strategy has used to achieve high power factor, low harmonics and high voltage capability.

Luis. A. Moran , Juan. W. Dixon and Rogel. R. wallace in their publication [11] titled ." A Three Phase Active Power Filter with fixed Switching Frequency for Reactive power and Current Harmonic Compensation" analyzes the performance and dynamic characteristics of a three-phase active power filter operating with fixed switching frequency. The proposed scheme has two important characteristics. First, it operates with fixed switching frequency, and second, it can compensate the reactive power and the current harmonic components of nonlinear loads. Reactive power compensation is achieved without sensing and computing the reactive component of the load current, thus simplifying control system.

Chapter 2

MULTILEVEL CONVERTERS

2.1 Introduction

Recently the "multilevel converter" has drawn tremendous interest in the power industry. The general structure of the multilevel converter is to synthesize a sinusoidal voltage from several levels of voltages, typically obtained from capacitor voltage sources. The so-called "multilevel" starts from three levels. A three-level converter, also known as a "neutral-clamped" converter, consists of two capacitor voltages in series and uses the center tap as the neutral. Each phase leg of the three-level converter has two pairs of switching devices in series. The center of each device pair is clamped to the neutral through clamping diodes. The multilevel converter can be operated in two modes i.e

1) ac to dc converter (rectifier)
2) dc to ac converter (inverter).

The waveform obtained from a three-level converter is a quasi-square wave output. The diode-clamp method can be applied to higher level converters. As the number of levels increases, the synthesized output waveform adds more steps, producing a staircase wave which approaches the sinusoidal wave with minimum harmonic distortion. Ultimately, a zero harmonic distortion of the output wave can be obtained by an infinite number of levels. More levels also mean higher voltages can be spanned by series devices without device voltage sharing problems. Unfortunately, the number of the achievable voltage levels is quite limited not only due to voltage unbalance problems but also due to voltage clamping requirement, circuit layout, and packaging constraints.

The magnetic transformer coupled multi-pulse voltage source converter has been a well-known method and has been implemented in 18- and 48pulse converters for battery energy storage and static condenser (STATCON) applications, respectively. Traditional magnetic coupled multi-pulse converters typically synthesize the staircase voltage wave by varying transformer turns ratio with complicated zigzag connections. Problems of the magnetic transformer coupling method are bulky, heavy, and lossy. There are three types multilevel converters:

1) diode-clamp,
2) flying-capacitors, and

3) cascaded-inverters with separated dc sources.

This chapter will describe features, advantages and disadvantages of these capacitor voltage synthesis multilevel converters.

2.2 Classification of Multilevel Converter

Multilevel converters are classified in circuit topology as

1) Diode clamped multilevel converter
2) Flying capacitor multilevel converter
3) Series H-bridge multilevel converter

The multilevel converter used here is a three-level converter.

2.2.1 Diode Clamped Multilevel Converter

Principle: An m- level diode clamped converter physically consists of m-1 capacitors on the DC bus and produces m-levels of phase voltage.

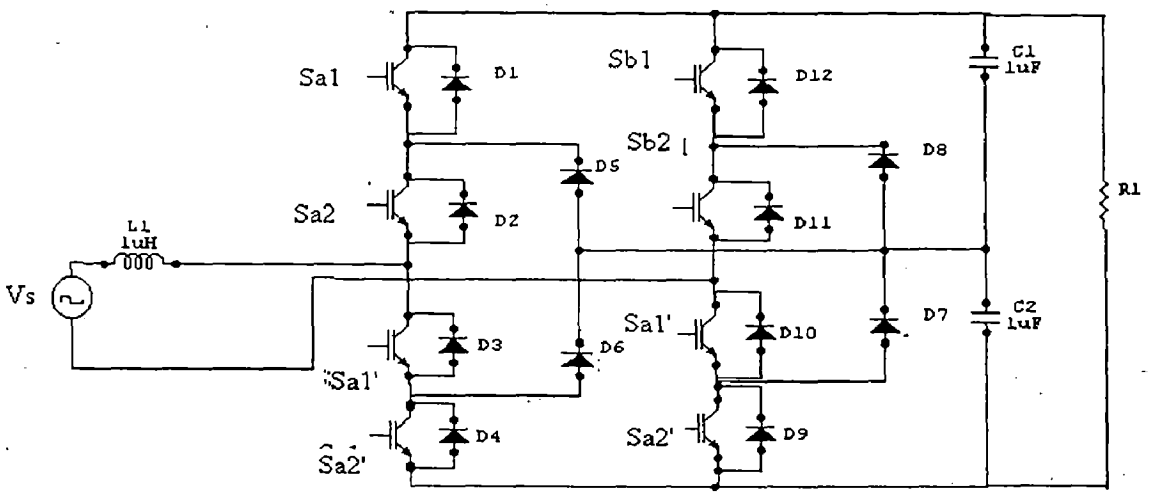


Fig. 2.1

Advantages:

1) When the number of levels is high enough, harmonic content will low enough to avoid need for filters.
2) Efficiency is high because all devices are switched at fundamental frequency.
3) Reactive power flow can be controlled.

Disadvantages:

1) Excessive clamping diodes are required when the number of level is high .

2) It is difficult to do real power flow control for individual converter.

3) There are unequal current stresses on power devices.

4) It requires Snubber circuit.

2.2.2 Multilevel Converter using Flying Capacitors

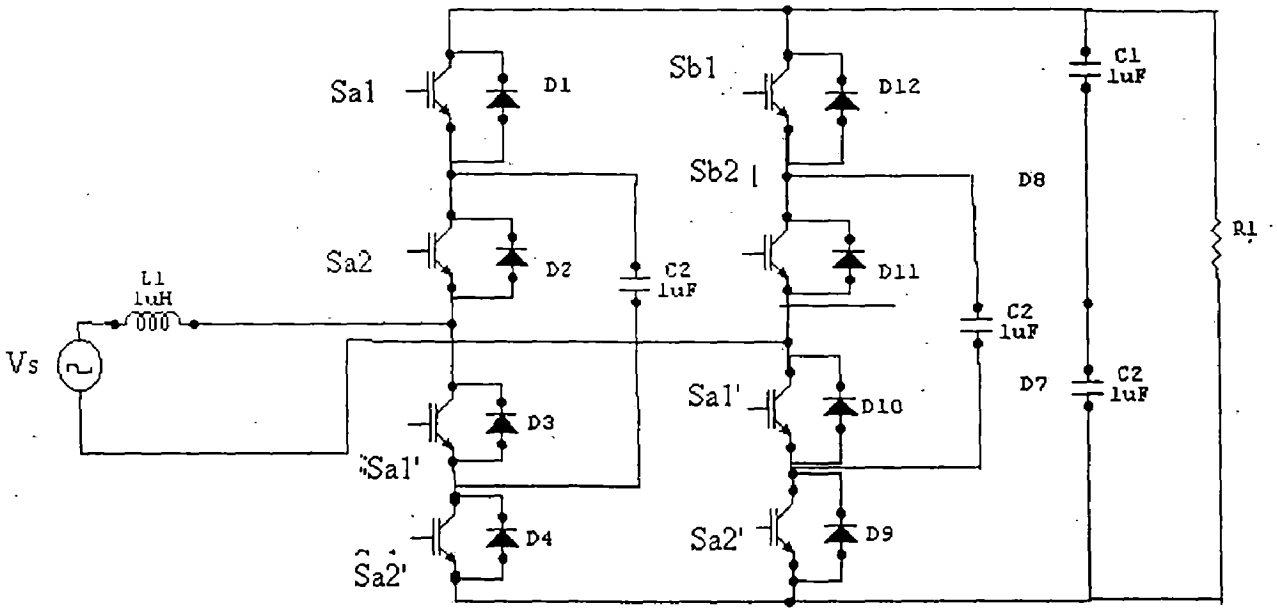


Fig 2.2

Advantages

1) Large number of storage capacitors provide extra ride through capabilities during power outage.

2) Provides switch combination redundancy for balancing different voltages.

3) When the number of levels is high, harmonics current will be low enough to avoid the need of filters.

Disadvantages

1) An excessive number of storage capacitors is required when the number of levels is high.

2) The inverter control will be complicated and switching frequency and switching loss will be very high for real power transmission.

2.2.3 H-bridge Multilevel Converter

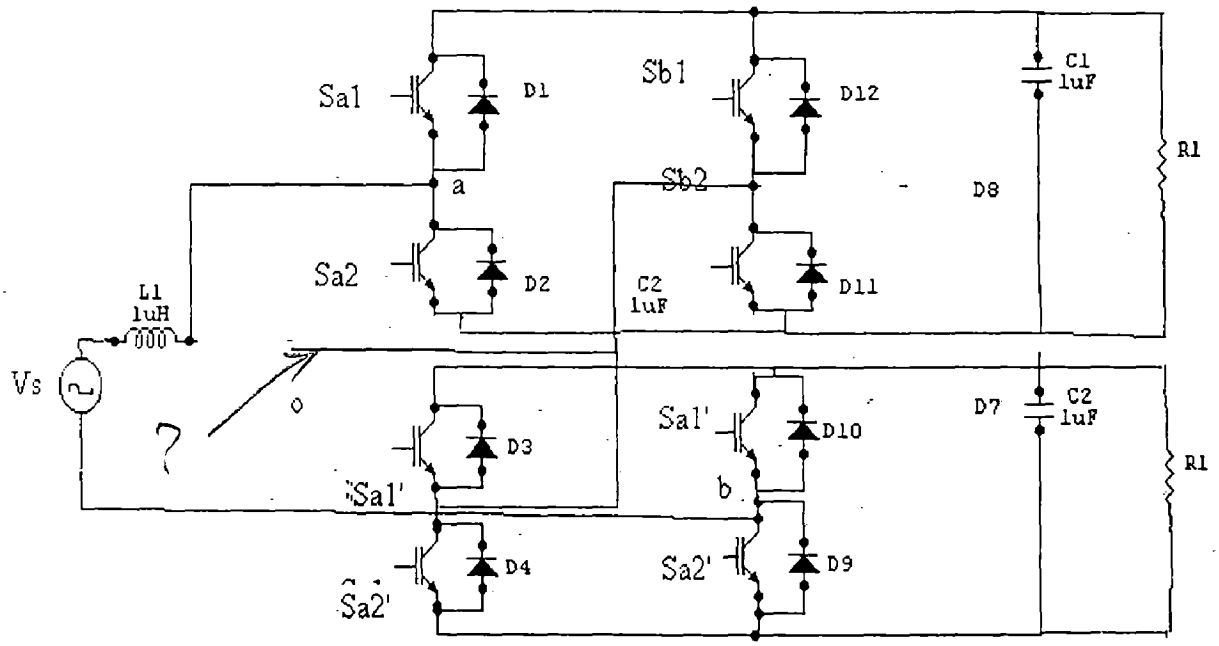


Fig.2.3

Advantages

1) Requires least number of components among all the Multilevel converter to achieve same number of voltage circuits.
2) Modularized circuit layout and packaging is possible since each level has same structures and there are no extra clamping diodes or voltage balancing capacitor.
3) Soft switching is possible to avoid bulky and loss resistor Snubber.
4) Its output has very low harmonics content in spite of low switching frequency.

Disadvantages

1) It requires special type of transformer.
2) Poor utilization of capacitors.
3) Very complex to provide regenerative braking.

Comparison of power components requirements among the Three level converters

Converter configuration	Diode-clamp	Flying Capacitors	H-Bridge
Main-switching devices	2(m-1)	2(m-1)	2(m-1)
Main diodes	2(m-1)	2(m-1)	2(m-1)
Clamping diodes	(m-1)(m-2)	0	0
DC bus capacitors	(m-1)	(m-1)	(m-1)/2
Balancing Capacitors	0	(m-1)(m-2)/2	0

Table 2.1

2.3 Problems in Multilevel Converter

The major problem in multilevel converter is the dc voltage balancing problem. Multilevel converter is used in the case if high power applications. But the major problem associated with it is fluctuation due to irregular and predictable charging and discharging action of dc link capacitors, which lead to unequal voltage across them. Due to these unequal voltages, the voltage stress across the power switches increases beyond their capacity which damages them.

2.4 Causes of Capacitors Voltage Unbalance

1) Unbalanced load due to unbalance between the phases of 3 phase induction motor.

2) Imbalance in parameter of power semiconductor switching devices.

3) Transformer secondary voltage imbalance in case of interlaced scheme.

4) Dissimilarity in the types of capacitor used.

5) Due to dead time implementation.

2.5 Remedies for Capacitor Voltage Unbalance

2.5.1 Back to Back intertie

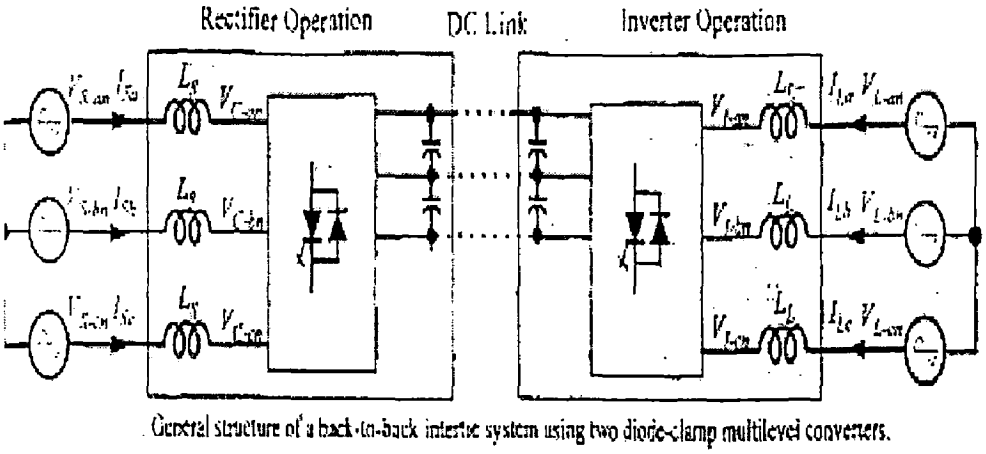


Fig 2.4 Back to back inertie

When interconnecting two diode clamp multilevel converter together with a ' DC capacitor bank', such that the left side converter serve as the AC-to-DC Rectifier and right side converter as the DC-to-AC Inverter to supply the ac load. Each switch is switched on once per fundamental cycle. The result is a well-balanced voltage across each capacitor while maintaining the stair case voltage wave, because the unbalance capacitor voltages on both sides tend to compensate each other. Such a DC link capacitor is characterized as the 'Back to Back Inertie'. In this case we use the redundant switching states in the rectifier and inverter side of the multilevel converter. There is no additional circuit required for balancing the dc Voltage but this advantage is at the cost of more switching losses.

Back to Back Inertie can also be treated as

1) The frequency changer

2) Phase shifter

3) Power flow controller and bi-directional energy conversion

The voltage-balancing problem can be overcome by using separate DC sources or by voltage regulators for each level.

2.5.2 DC Voltage Balancing by Zero Sequence Current

In the case of 3 phase m-level converter, the DC voltage balancing can be achieved by using zero sequence current. The neutral point of transformer is connected to DC link midpoint.

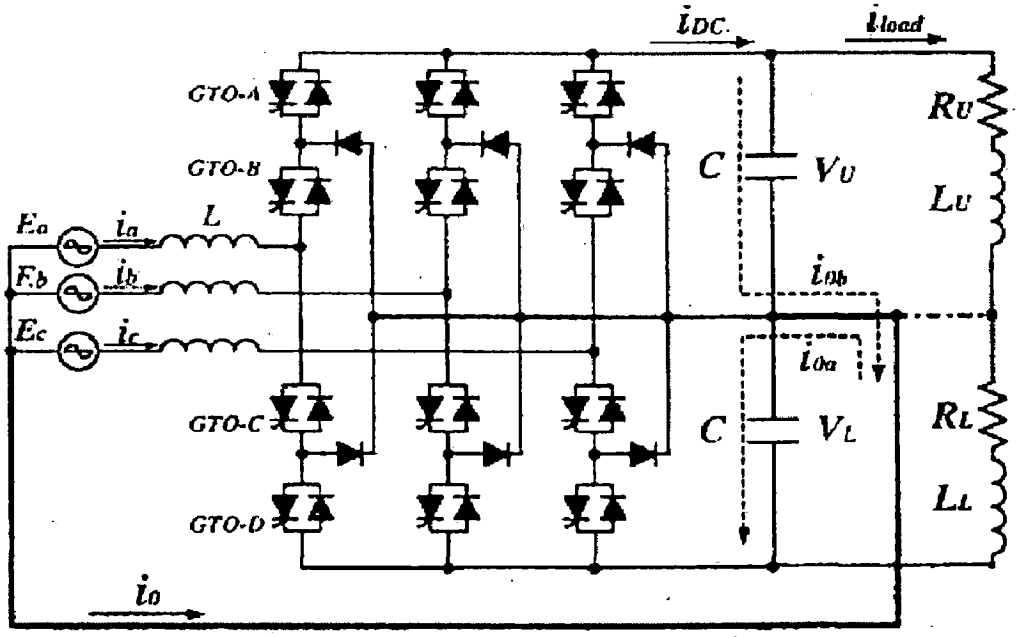


Fig 2.5 DC voltage balancing with zero sequence current.

The important problem in multilevel PWM converter system is the voltage unbalance between the upper and lower capacitors. If such a voltage imbalance occurs, a high voltage may be applied to the semiconductor switching devices exceeding their voltage tolerance. Such an unbalanced high voltage will destroy the semiconductor switches. Therefore to prevent such an unbalance a path of zero sequence current is provided by simply connecting the neutral point of transformer and the DC link midpoint. Then the Zero sequence current can be regulated with a PWM technique that manipulates the zero sequence voltage. Compared with other balancing scheme the proposed scheme is simple and cost effective, since it is the connecting of neutral points.

If i_o is positive, in fig 3 then the zero sequence current flows through the lower capacitor, resulting in the lower part voltage V_L rise. At the same time the upper DC link capacitors discharges, since it is assumed that whole dc link voltage is regulated to constant. Similarly if i_o is negative i.e $i_o=io_b$, then the zero sequence current flows through the

upper capacitors, increasing the upper part voltage Vu. At this time the lower DC link capacitor discharges.

2.5.3 Neutral Point Control for Three-level Converter

The addition of a dc offset equally to the modulation wave used for used for sub harmonics PWM generation (where the wave is compared against a set of carriers) for each of the three phases does not change the effective voltage being seen by the three phases does not change the effective voltage being seen by the machine but changes the effective current path through the capacitor bank. This result is a mean current being drawn from the neutral point. The principal behind the control strategy developed is that if a variation in neutral potential is detected (by measuring a difference between the two capacitors voltages), then the control scheme reacts by introducing a dc offset as described. The offset causes a current in the neutral point to restore the capacitor balance.

The basic procedure is to measure the error between the capacitor voltages and use a controller to calculate an offset to be added to each of the PWM modulation waves. This will change the current factor which in conjunction with the load current will alter the neutral point current and force a redistribution of change on the capacitors.

2.6 Pulse Width Modulation Technique used for Multilevel Converter

2.6.1 Three-level Converter

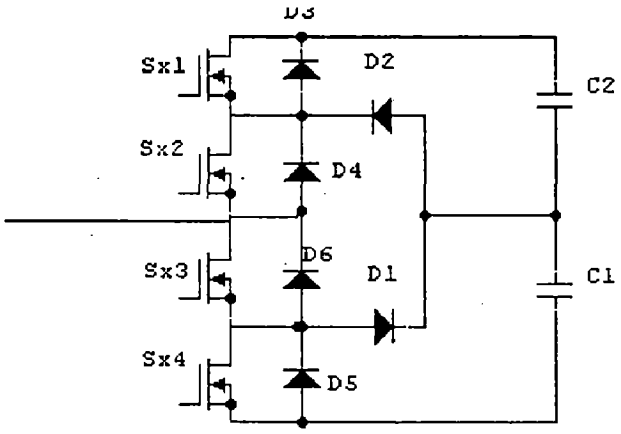


Fig 2.6 One leg of Three-level converter

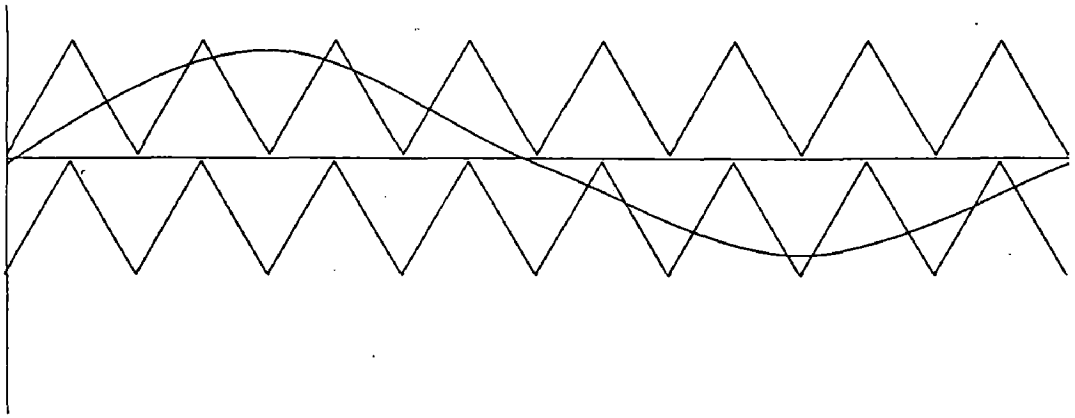


Fig 2.7 Sinusoidal Pulse width modulation for Three-level converter

For the three level converter two triangular carrier waves are compared with the sinusoidal modulating wave to produce the desired switching pulses for one leg of the converter.

2.6.2 Five-level Converter

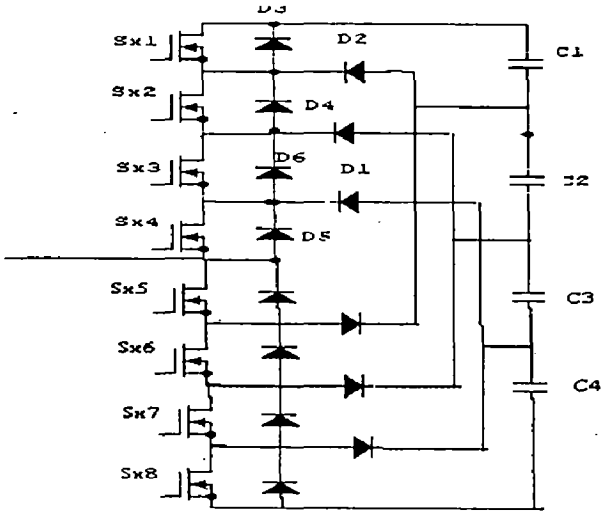


Fig 2.8 One leg of Five level converter

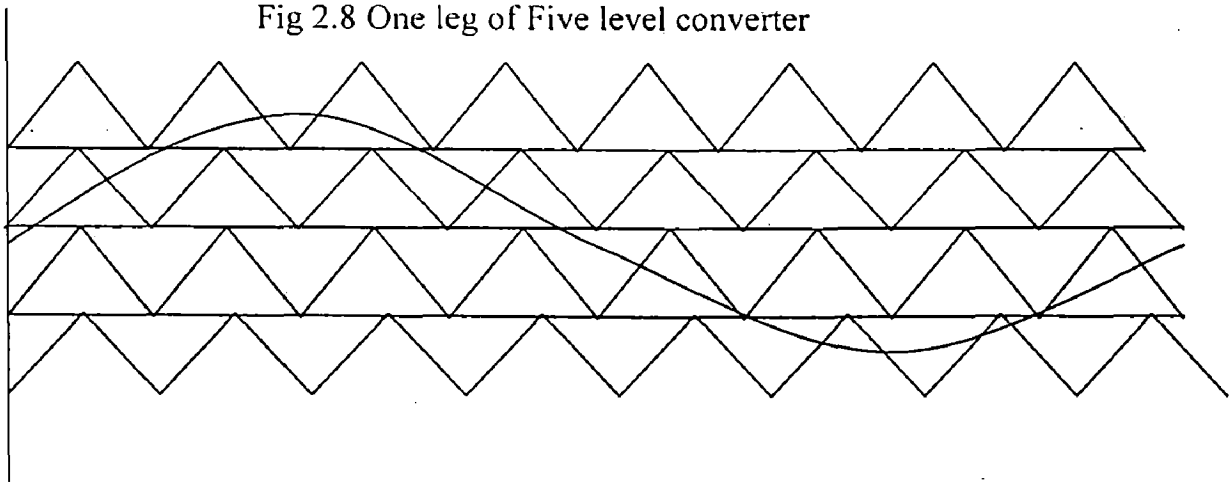


Fig 2.9 Pulse Width Modulation for Five-level converter

For the five-level converter four triangular carrier waves are compared with the sinusoidal modulating wave to produce the desired switching pulses for one leg of the converter.

2.7 Applications of Multilevel Converter

2.7.1 Traction Drive System

Multilevel converters can be used for traction drive systems. The main advantage of this kind of topology is that it can generate almost perfect current or voltage waveforms, because it is modulated by amplitude instead of pulse-width. That means that the pulsating torque generated by harmonics can be eliminated, and power losses into the machine due to harmonic currents can also be eliminated. Another advantage of this kind of drive is that the switching frequency and power rating of the semiconductors is reduced considerably.

The PWM techniques used today to control modern static converters for electric traction, do not give perfect waveforms, which strongly depend on switching frequency of the power semiconductors. Multi-level converters work more like amplitude modulation rather than pulse modulation, and this fact makes the outputs of the converter very much cleaner. This way of operation allows having almost perfect currents, and very good voltage waveforms, eliminating most of the undesirable harmonics. And even better, the bridges of each converter work at a very low switching frequency, which gives the possibility to work with low speed semiconductors, and to generate low switching frequency losses.

2.7.2 Multilevel Converted for DC Motor Speed Control

A PWM Multilevel converter can be used as two quadrant speed control of a DC Motor by connecting the armature of the DC motor across the converter output. The motor armature current can be controlled to control the torque at any speed. In regenerative braking mode, the converter acts as the inverter and energy is pumped back to the source. In this the line current is sinusoidal and pf can be maintained at unity @ all operating condition.

2.7.3 Active power filter

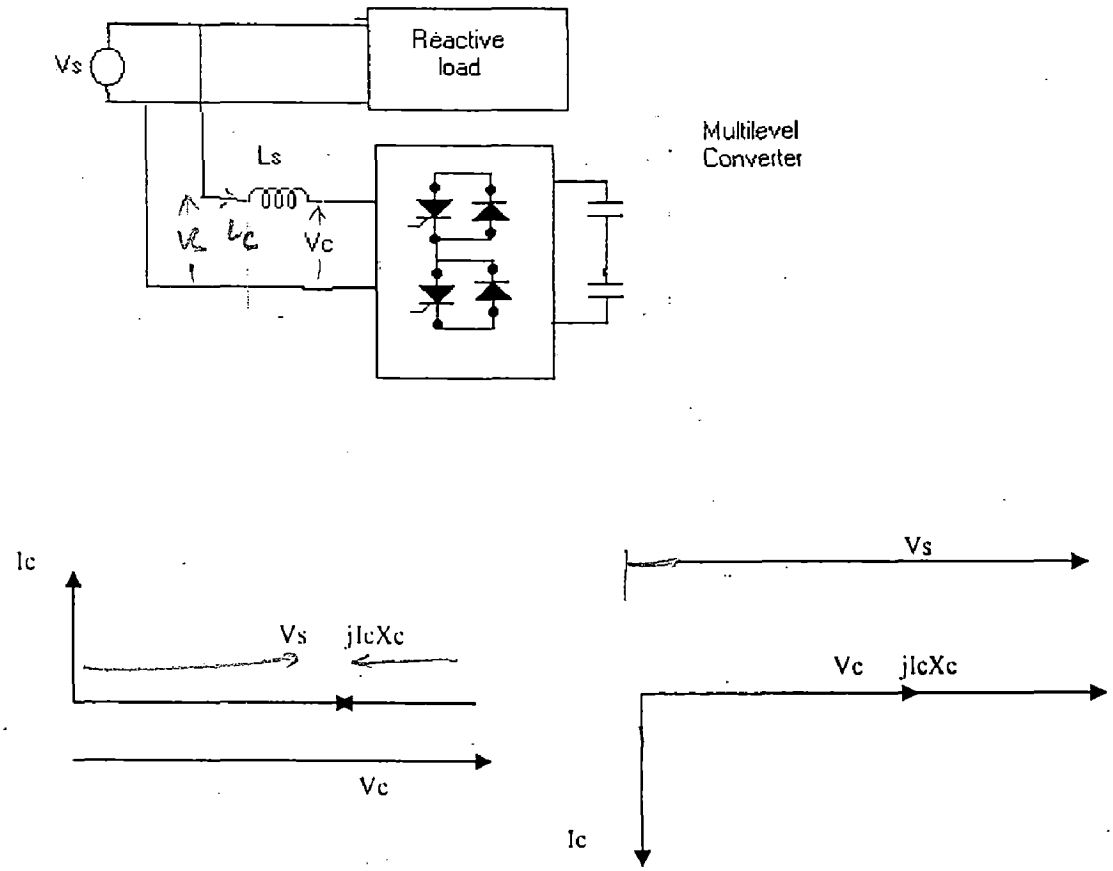


Fig 2.10 Active power filter

When Multilevel converter draws pure reactive power , phase voltage and current are 90 degree apart and the capacitor charge and discharge current can be balanced . Such a converter serving for reactive power compensation is called static VAR generator.

The source voltage vector Vs and converter voltage vector Vc are related by Vs = Vc +jIcXc where Ic is the converter current vector and Xs is impendance of the inductor Ls. The fig shows that converter voltage is in phase with source voltage eith a leading reactive current. The polarity and magnitude of reactive current are controlled by magnitude of converter voltage Vc which is a fuction of DC bus voltage and voltage modulation index.

Conclusions

In this chapter we have studied the feature, advantages and disadvantages of different topologies of multilevel converter. It has been found that every topology of converter has its own advantages and disadvantages. Such as the use of Diode clamping topology reduces the harmonics but requires large number of clamping diodes if the level is high. In Flying capacitors topology a large number of storage capacitors are required. IN this chapter Pulse Width Modulation schemes has been explained for three-level and five-level converters. Multilevel converters are most suited for Medium voltage and high voltage drives and can be used as active power filter.

Handly!

Chapter 3
A CONTROL SCHEME FOR MULTILEVEL CONVERTERS

3.1 Introduction

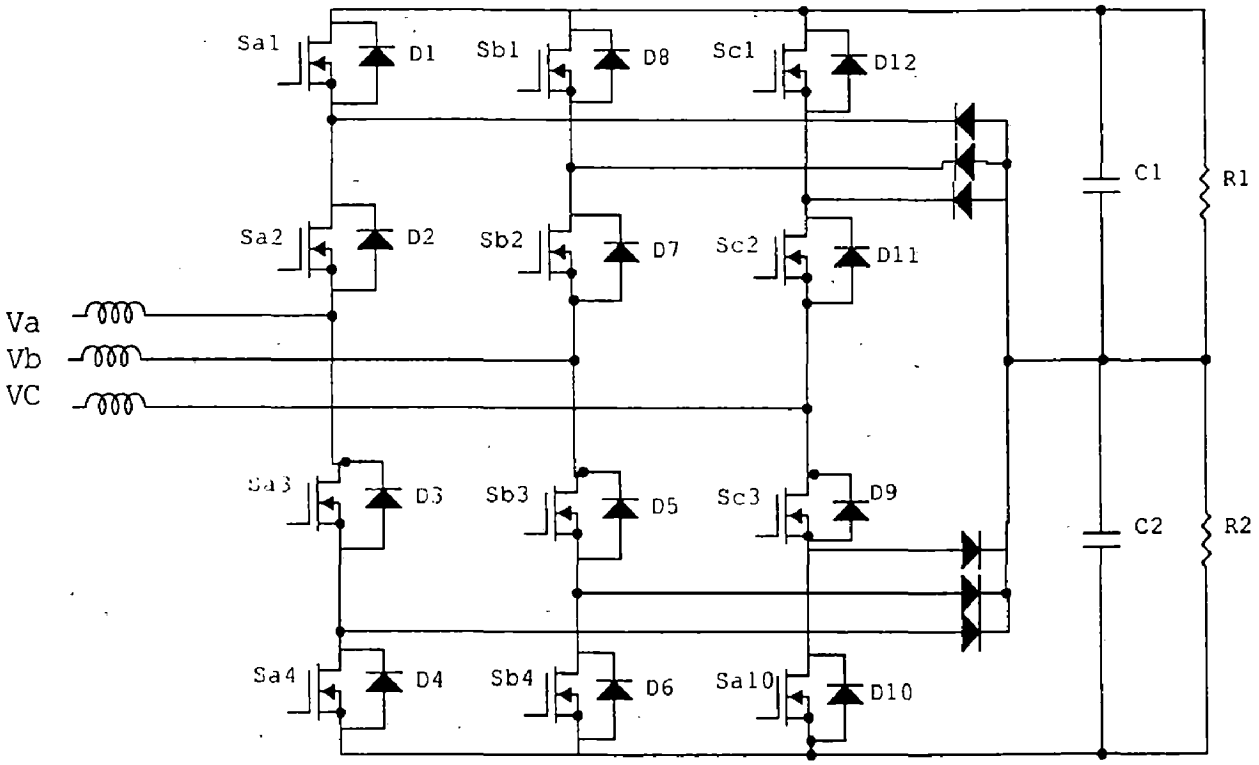
Multilevel converters are suited for medium voltage static power conversion. The series connection of multiples dc voltage sources in the dc bus allows the operation in medium voltage systems, with lower voltage stresses across each semiconductor switch. in both cases as a rectifier or as a multilevel inverter. Moreover the multi-step composition of the output voltage (for the inverter), or the input current (for the rectifier) presents lower THD factors as compared with the two levels converter, due to presence of multiple steps in the respective waveforms. The main application of this converter topology has been found in ac drives and also in reactive power compensators (i.e active power filters).

In this chapter a generalized control scheme has been discussed that allows the operation of the multilevel converter in the four quadrant of the P_Q plane. The principal advantage of this characteristic is that it allows the converter to operate as a rectifier or as an active power filter, or both at the same time. In the rectification mode the converter can operate as a frequency changer supplying active power from the DC bus to an output inverter while keeping the input current sinusoidal and with unity power factor.

As an active power filter, the three-level converter operates, as a controllable current source injecting the current harmonics required by non-linear loads. In this type of application the voltage across each capacitor remains constant and balance even under severe dynamic operating condition. The most important characteristic of the proposed control scheme is that allows the operation of multilevel converter as a frequency changer (or rectifier), while it compensates for the current harmonics and reactive power required by the distribution system. The Converter control scheme only senses the system current and voltage waveforms to generate the required reference signals, thus reducing the number of components and simplicity of the control topology.

In this chapter the control scheme is discussed in terms of principle of operation for steady state and transient operating conditions as a rectifier and active power filter. In this dissertation a Three-level composition of multilevel converter has been used.

Power Circuit



3.1 Power circuit for three-level converter

3.2 Principle of Operation of Control Scheme

In the case of active power filter application. the control scheme must be able to keep the DC voltage constant and equal in each electrolytic capacitor. As a rectifier, the control scheme supply the adequate active power to the DC bus, keeping the DC voltage constant and the input current waveforms sinusoidal and with unity power factor.

The proposed control scheme must perform two important duties. The first one is to keep the DC bus voltage constant, balanced and equal to a defined reference value, and the second one is to force the power distribution system current to be sinusoidal and in phase with the respective phase-to-neutral voltage, independently of the load value

connected to the DC bus. For the above reasons, the multilevel converter can operate as a rectifier (in the case it had load connected to the DC bus), or as an active filter (in case no load connected to the DC bus). When the converter operates as a rectifier, it forces the system line current to be sinusoidal and in phase with the respective phase to neutral voltage, which means that it is also operating as an active power filter. The block diagram of the control scheme is shown in fig.3.2.

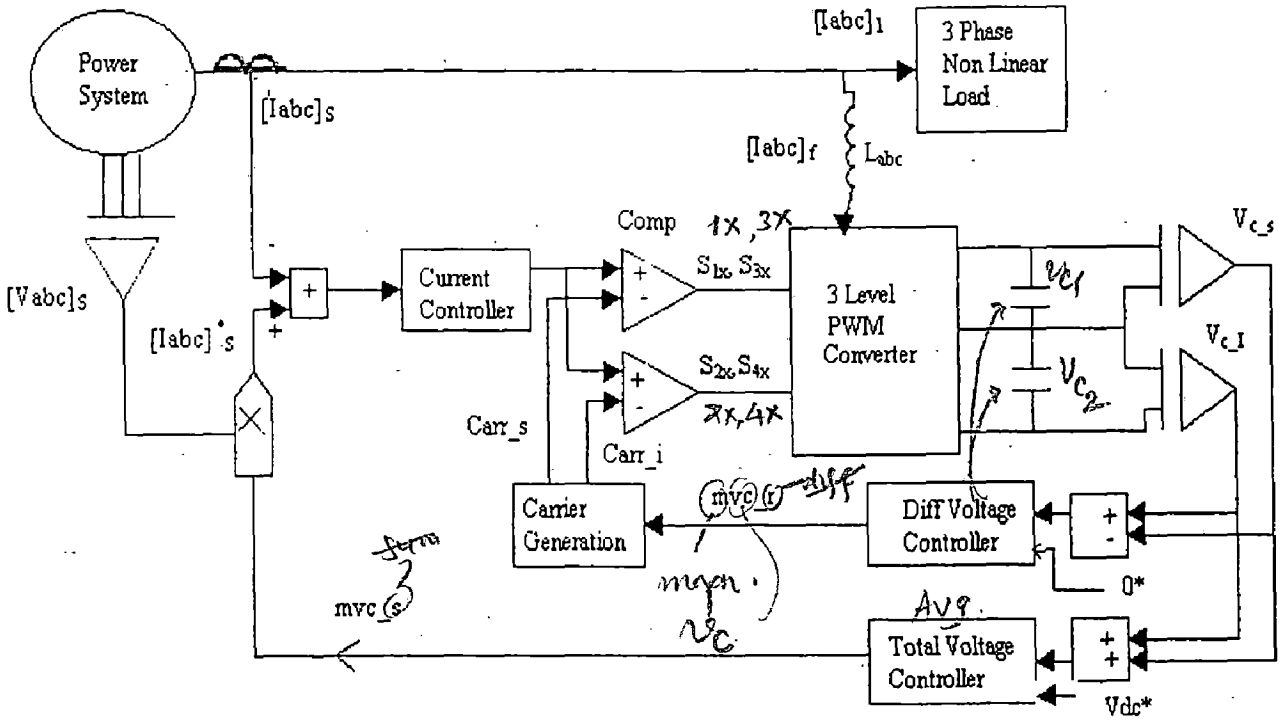


Fig 3.2 Block Diagram of the control Scheme

Fig.3.2 shows that the control scheme has basically two blocks. The first one keeps the DC bus voltage constant and balanced, while the second one is in charged of forcing the power distribution line current to be sinusoidal and with unity power factor.

The DC voltage control system must perform two functions simultaneously: The first one is to keep the DC bus voltage constant and equal to given reference value, and the second one is to maintain the voltage across each electrolytic capacitor constant and balanced. The voltage across each capacitor is equal to the DC bus Voltage divided by the number of capacitors.

The DC bus voltage is controlled by adjusting the amount of active power absorbed by the multilevel converter, while the balance across each capacitor is

achieved by changing the amplitude of each triangular carrier waveforms. The gating signals of the converter are obtained by comparing the error current signal with two Carrier triangular waveforms with fixed frequency and variable amplitude.

3.3 Generation of Gating Signals

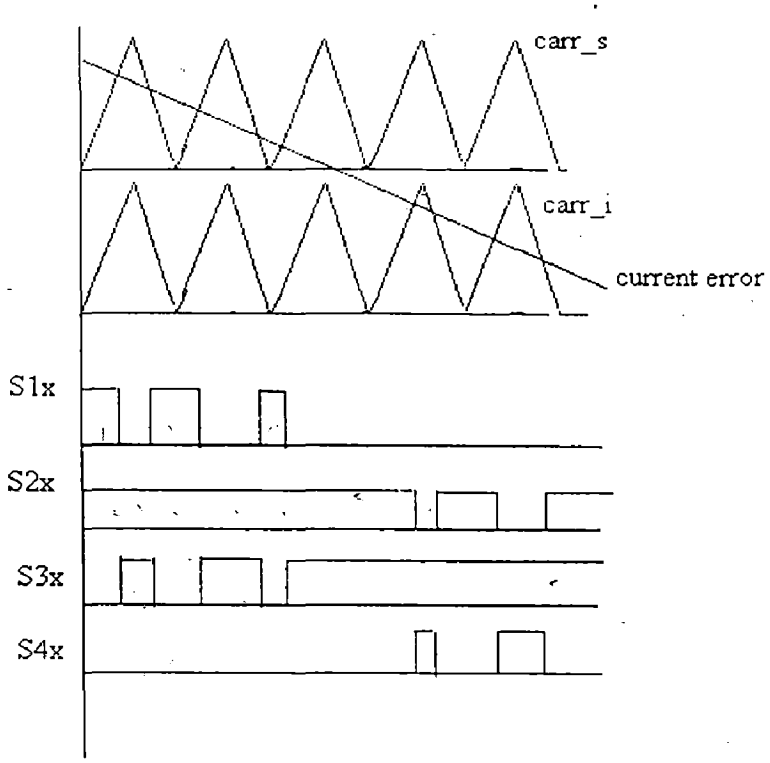


Fig.3.3 Generation of gating signal by comparing the current error

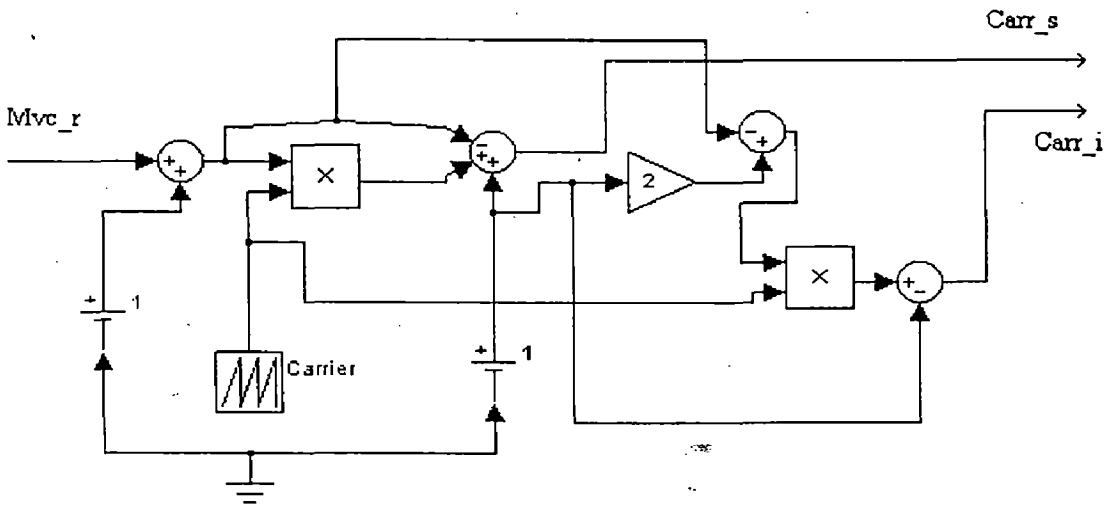


Fig.3.4 Algorithm used to generate the triangular carrier wave signal with two Triangular carrier waveforms

The two triangular carrier waveforms are in phase and their amplitudes are complementary modified following the magnitude of differential DC voltage controller (MVc_R). The modification of the triangular carrier waveform amplitudes allow to control the voltage across each electrolytic capacitor, keeping them constant, balanced and equal to given reference value. MVc_R error signal is generated by comparing the difference between the voltage across each capacitor (Vc1-Vc2) with difference voltage reference (must be equal to zero). The triangular carrier waveforms are modified in such a way that, when a voltage across one capacitor must be increased, the amplitude of respective carrier waveform increases, while the complementary one is reduced in the same proportion. On the other hand if the voltage across one capacitor must be reduced, the respective carrier waveform is decreased, and the complementary one increased in the same proportion.

As shown in fig 3.3 the current error signal is compared with two triangular carriers signals to obtain the firing pulses. The result of comparing current error and carr_s is used to control the switching S_{1x} and S_{3x}. the result of comparing current error and carr_i is used to control the switching S_{2x} and S_{4x}. The principle is that

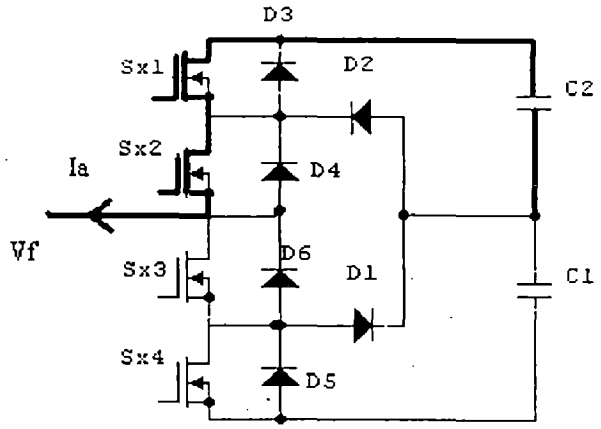
1) if current error > carr_s, then S_{1x} is on and S_{3x} is off.

2) if current error <= carr_s, then S_{1x} is off and S_{3x} is on.

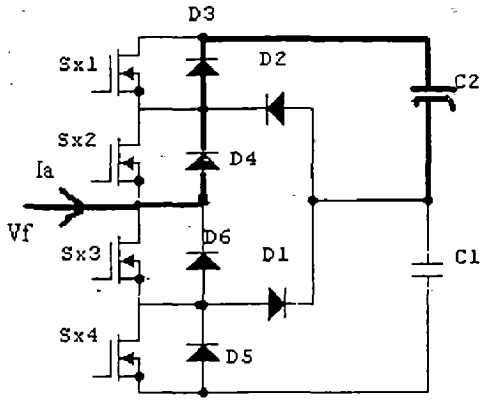
3) if current error > carr_i, then S_{2x} is on and S_{4x} is off.

4) if current error <= carr_i, then S_{2x} is off and S_{4x} is on.

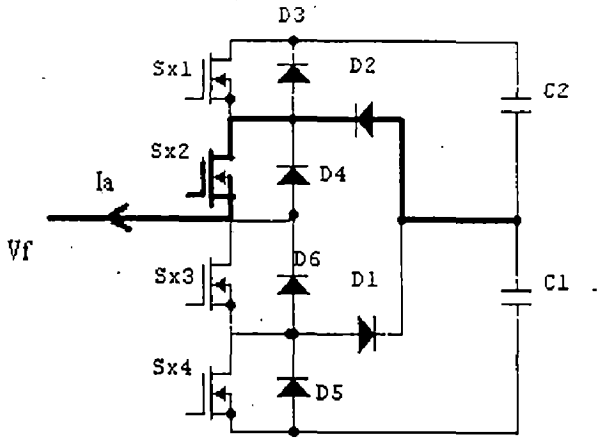
The six different possible gating states for one leg of the converter is shown in fig 8.The gating signals of each converter switch are generated by comparing the current error signals of the corresponding phase with the respective upper or lower triangular carrier waveform. Fig 3.5 shows that each electrolytic capacitor can be connected to the power source (through the coupling reactor), for positive and negative current. In fig .3.5 a1 and a2, the upper capacitor is connected to the power supply for positive and negative current respectively. For the Commutation State shown in fig.3.5 a3 and a4, the DC neutral point is connected to power supply and in fig.3.5 a5 and a6 the lower capacitor is connected to the power supply. Each different connection modifies the voltage value across the capacitor terminals.



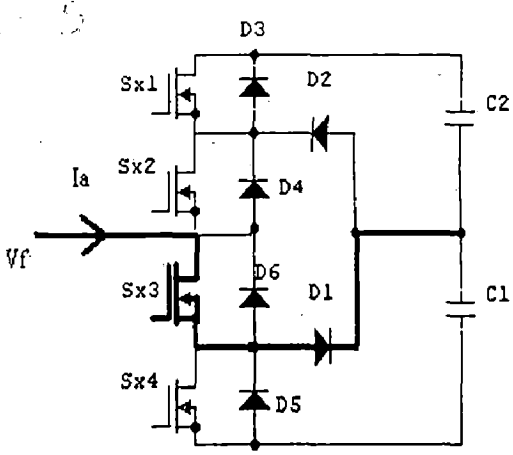
a1)



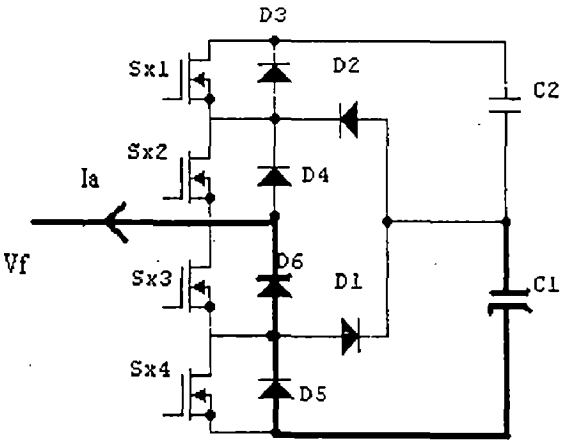
a2)



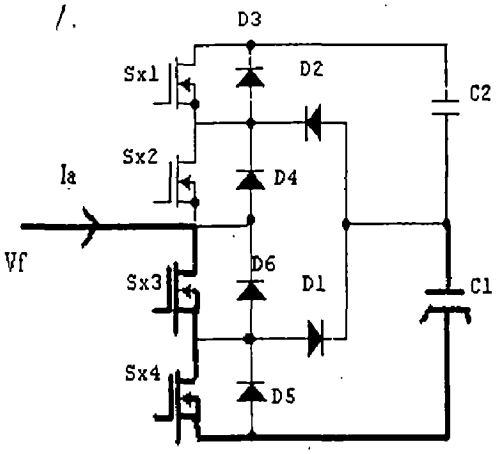
a3)



a4)



a5)



a6)

Fig.3.5 Different gating combination of converter one leg

The effect of changing the amplitude of the triangular carrier waveform is reflected in the number of intersections of these signals with the respective current error waveform. The larger the amplitude of carrier waveforms the more number of intersections will exist and therefore the voltage across this capacitor will increase. The opposite effect occurs if the amplitude of the triangular carrier waveform is decreased.

Conclusion

In this chapter a control scheme has been discussed which operates the multilevel converter in three-level as an rectifier or active power filter or both at the same time. The main problem in multilevel converter is the capacitor voltage balancing problem. By using this control topology the voltage across each capacitor is constant, balanced and equal. Also the total dc bus voltage can be maintained constant. This control topology forces the input current to be sinusoidal and in phase with the respective phase to neutral voltage. Thus acting as an rectifier or active power filter or both at the same time.

Chapter 4
SIMULATION OF CONTROL SCHEME FOR MULTILEVEL CONVERTERS

4.1 Introduction

The simulation of the control scheme of multilevel converters was carried out with the help of MATLAB (version 6.1). Simulink power system block sets were used for the simulation purpose.

Simulation of the control scheme as explained in chapter 3 was carried out which operates the multilevel converter as an active power filter and rectifier at the same time. As explained in chapter 3 control scheme must perform two important duties. The first-one is to keep the DC bus voltage constant, balanced and equal to a defined reference value, and the second one is to force the power distribution system current to be sinusoidal and in phase with the respective phase-to-neutral voltage, independently of the load value connected to the DC bus. Hence two controller has been designed, one is the differential voltage controller which keeps the voltage across each capacitor constant, balanced and equal and the other is the total voltage controller which forces the input current to be sinusoidal and in phase with the respective phase to neutral voltage.

The following waveforms for control scheme operating as an active power filter and rectifier have been observed as follows

1) Input phase voltage
2) Input line current
3) Converter compensating current
4) Load current
5) Voltage across the two capacitors.

The simulation block diagram has been given in figure 4.1 and the blocks used in this simulation have been explained in this chapter.

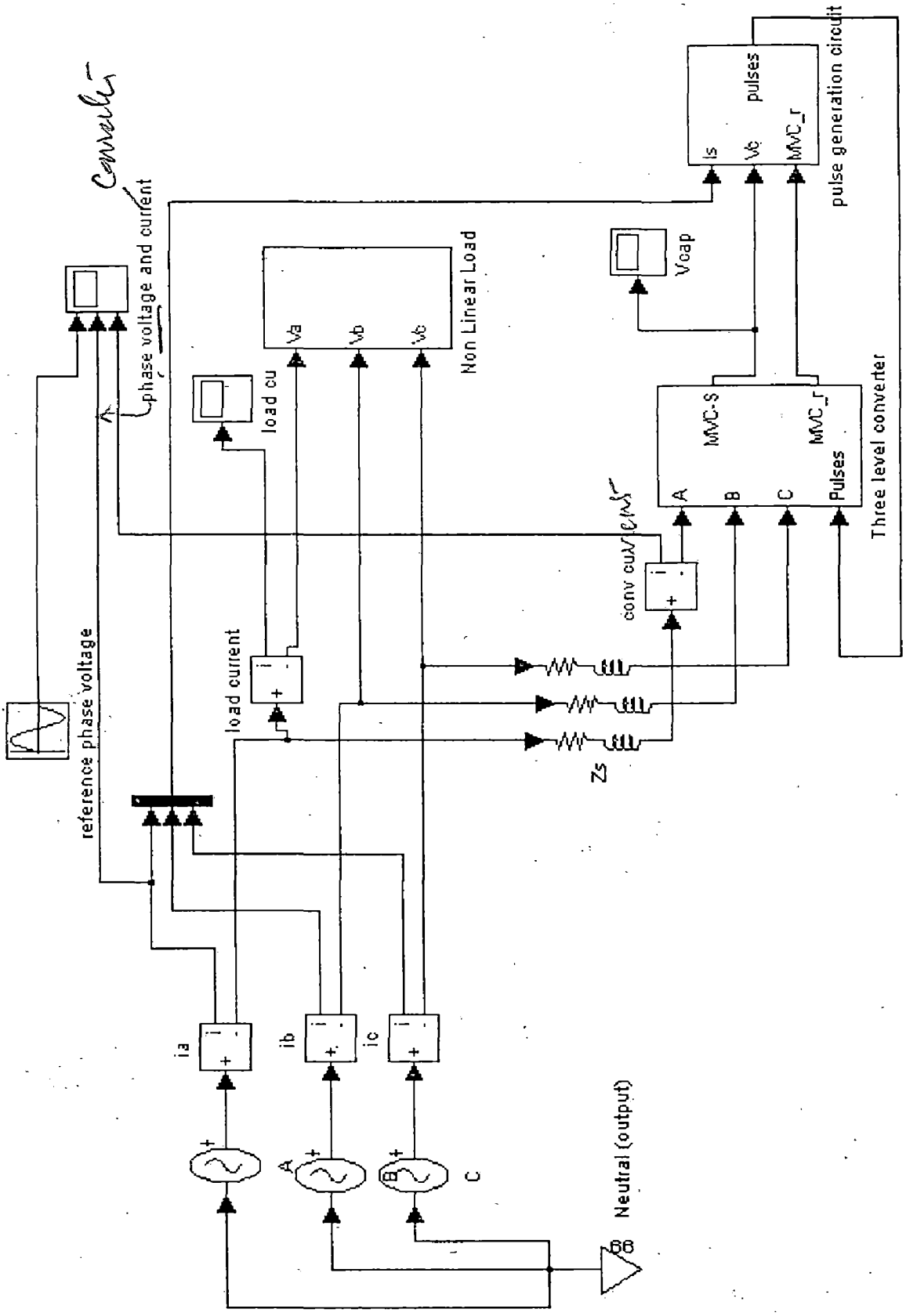


Fig 4.1 Simulation model of the control scheme for multilevel converters

4.2 Simulation Model Explanation

As shown in the simulation module fig 4.1, the module consists of the following blocks

a) Nonlinear load

b) Three-level converter

c) Pulse generation circuit

4.2.1 Nonlinear load

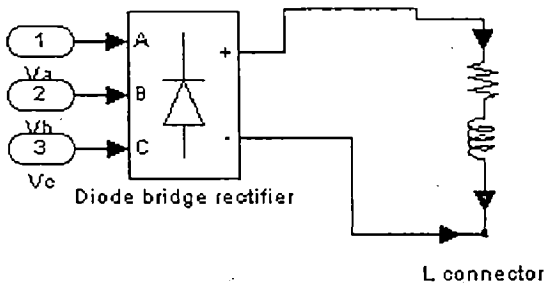


Fig 4.2 Nonlinear load block

The nonlinear load block consists of a diode bridge rectifier followed by an R-L load.

4.2.2 Three-level Converter

The three level converter block consists of a three level converter. One arm of the three level converter is shown in fig 4.1.3. There are three arms connected in parallel.

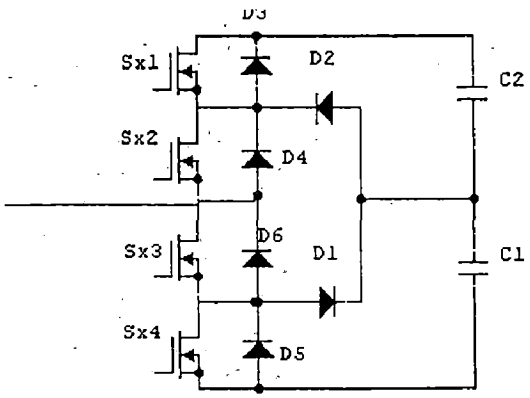


Fig 4.3 One leg of a Three level Converter

4.2.3 Pulse Generation circuit

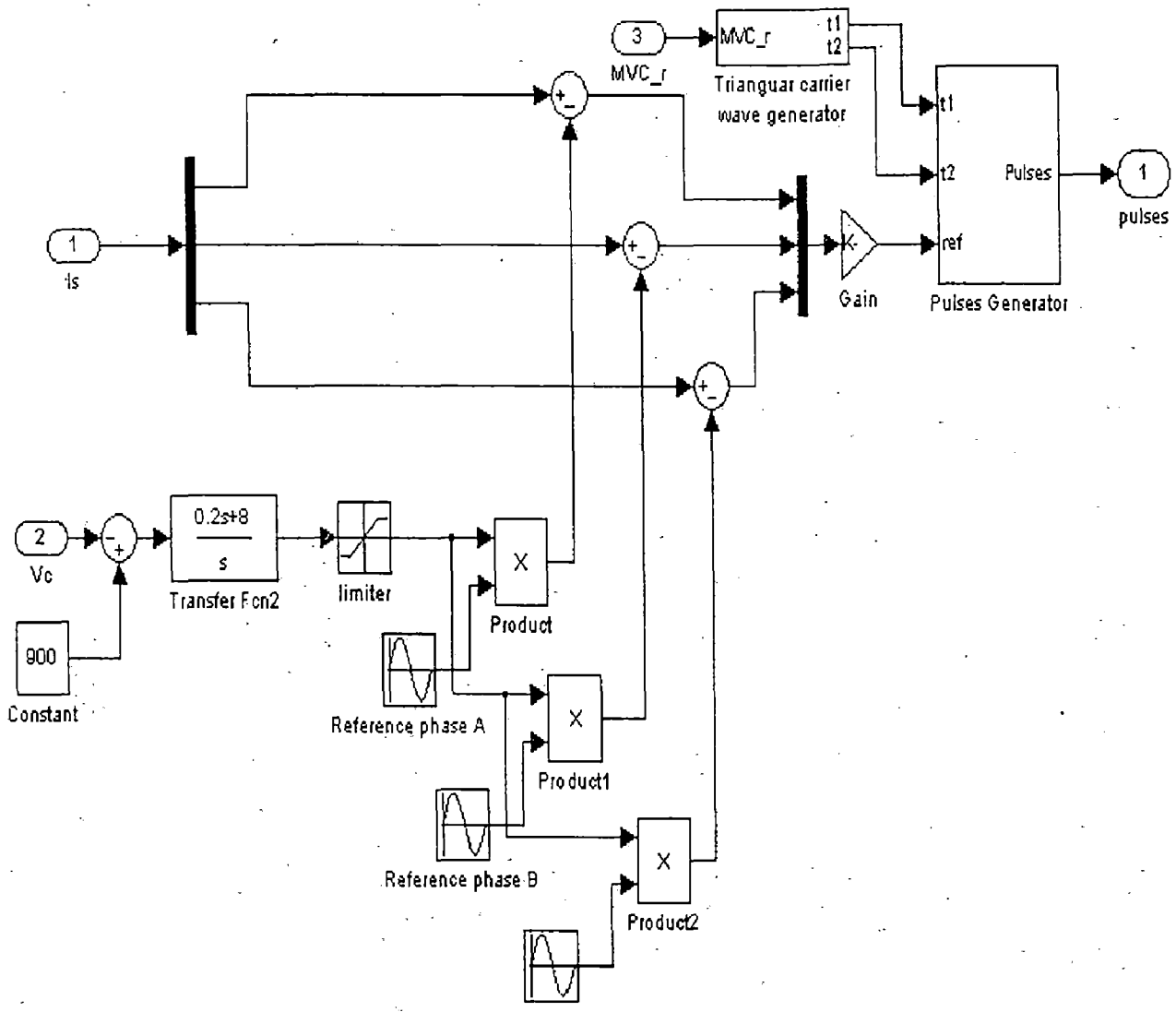


Fig 4.4 Pulse Generation Block for Three-level Converter

The pulse generation block consists of a triangular carrier wave generator which generates two triangular carrier waves, which are of same amplitude, same frequency and are in phase. The amplitude of the triangular carrier waves can be modified on the basis of signal MVc_r, which is the difference between the two capacitors voltages. Three reference signals of current are produced which are in phase with respect to three distribution phase voltages. Their amplitude can be modified by a signal MVc_s which is the difference between a Reference constant voltage and the sum of the two capacitors voltages.

a) Triangular carrier wave generator

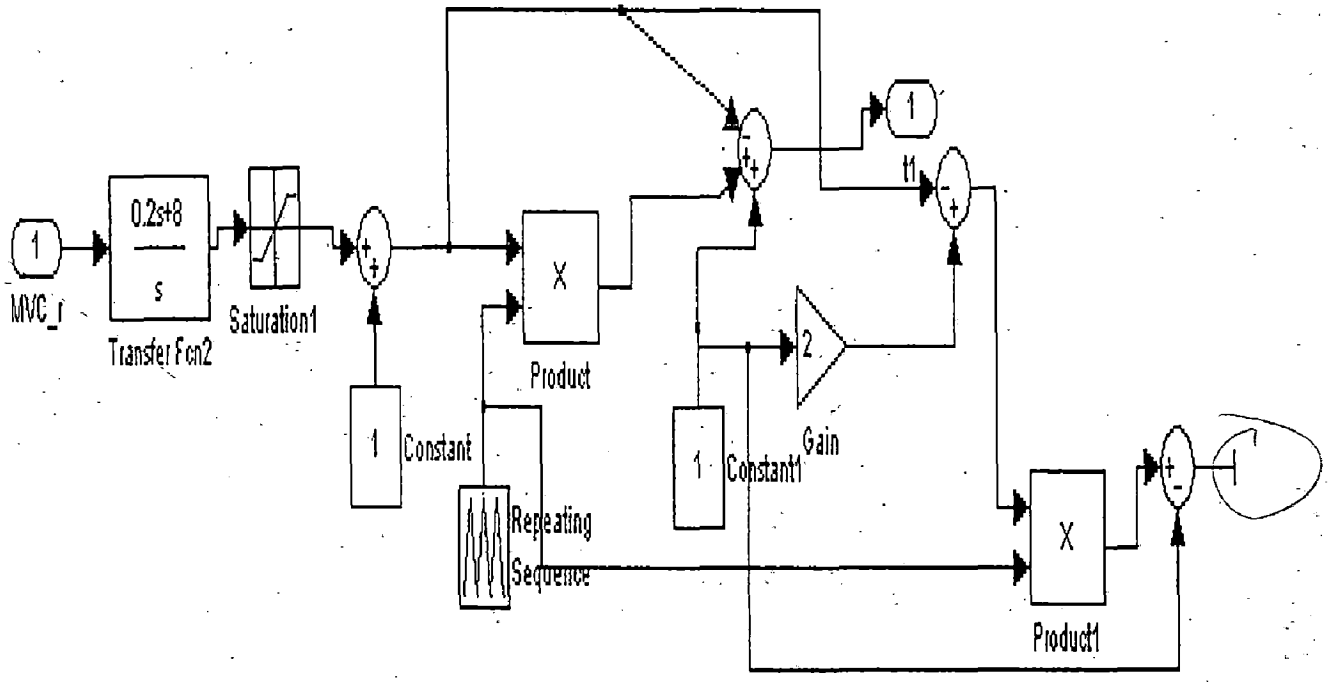


Fig 4.5 Triangular carrier waveform generator

The two triangular carrier waves are of the same magnitude, phase and frequency. The two carrier waves are complimentary modified in such a way that when the voltage across upper capacitor increases, the upper triangular carrier wave increases, whereas the lower triangular carrier wave decreases in the same proportion and vice versa when the voltage across the lower capacitor voltage is greater than the upper capacitor voltage.

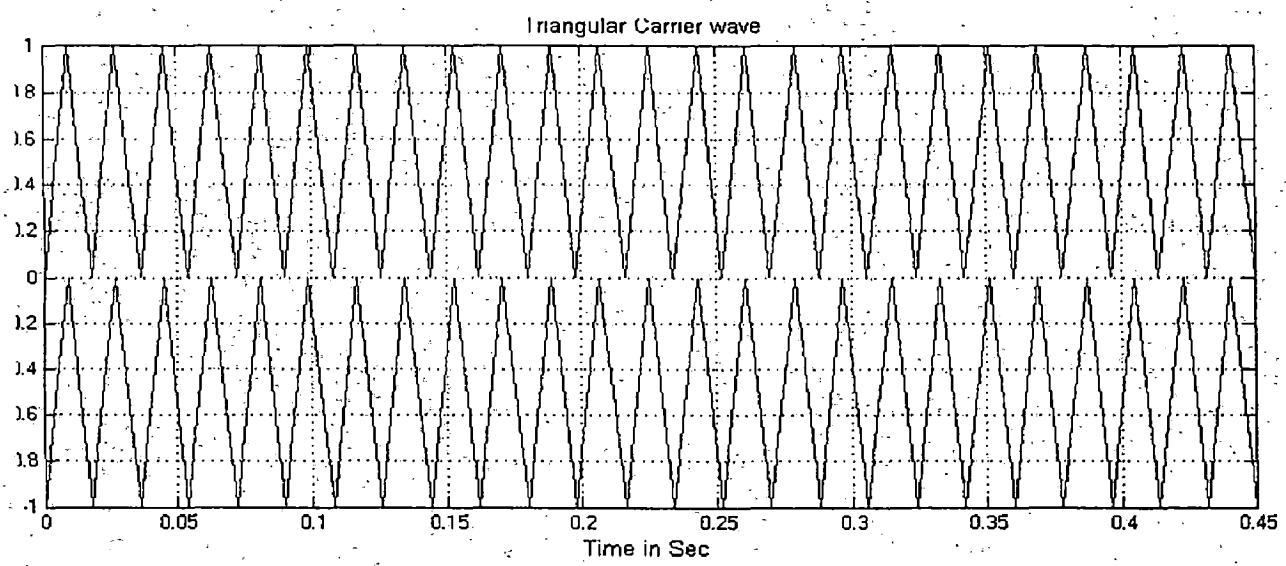


Fig 4.6 Triangular carrier wave when the voltage across each capacitor is equal

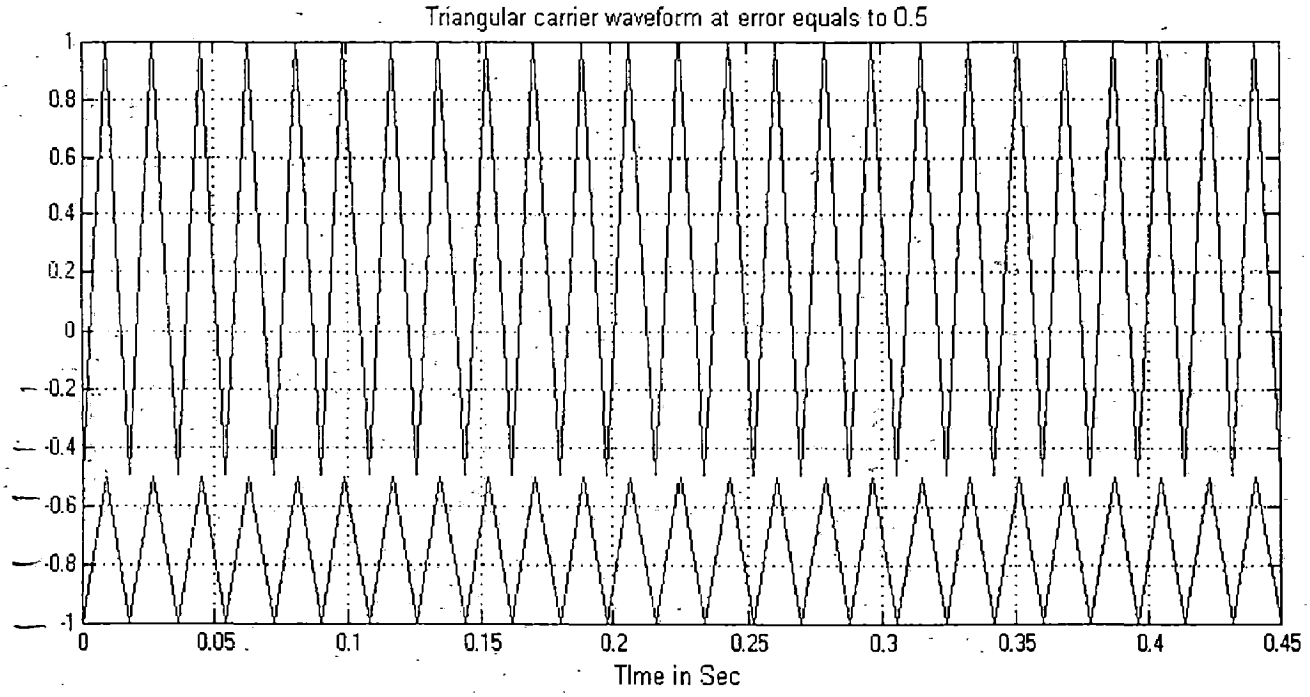


Fig 4.7 Triangular carrier wave when the voltage across Upper capacitor is greater

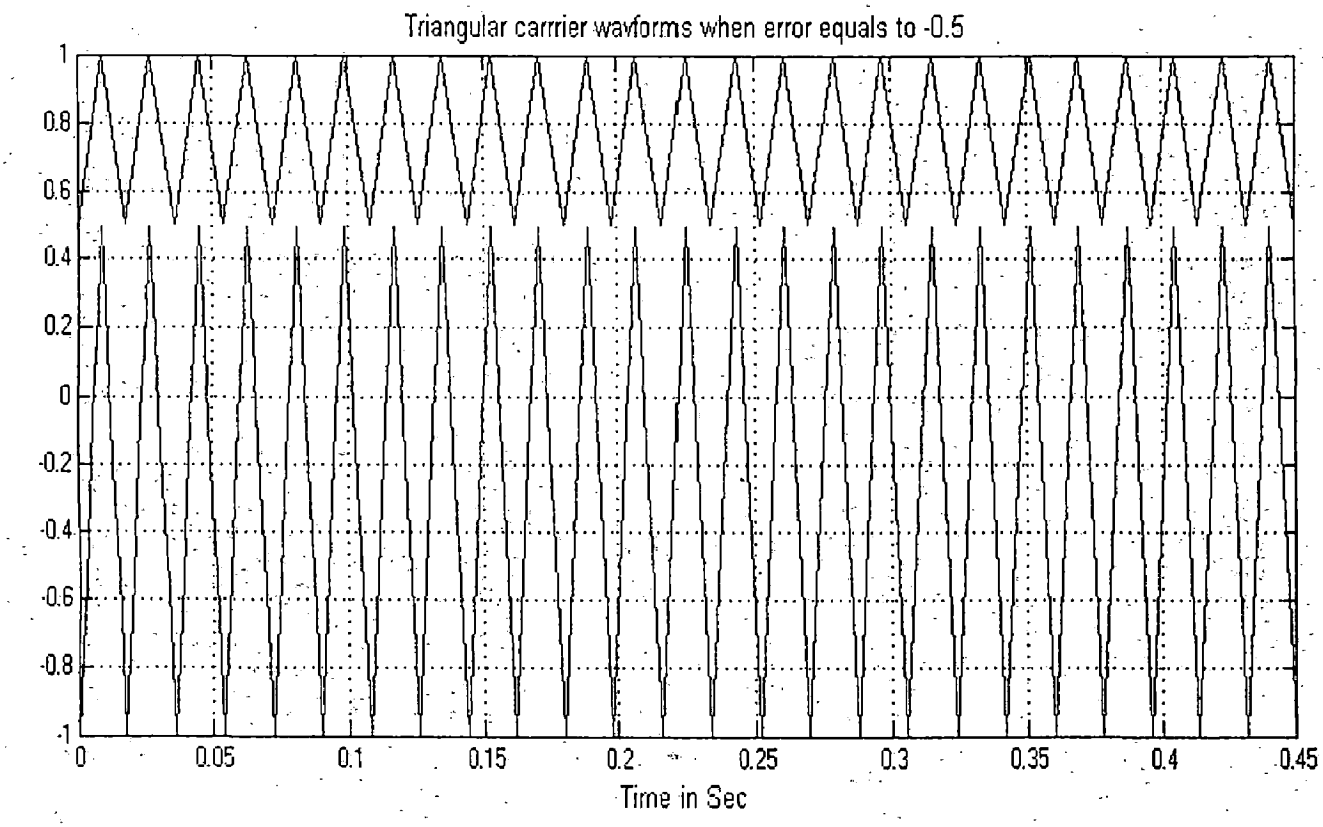


Fig 4.8 Triangular carrier waveforms when the voltage across lower capacitor is greater

4.3 Simulation Results

4.3.1 Control scheme operation as an active power filter and rectifier:

a) When Carrier Frequency = 1 kHz

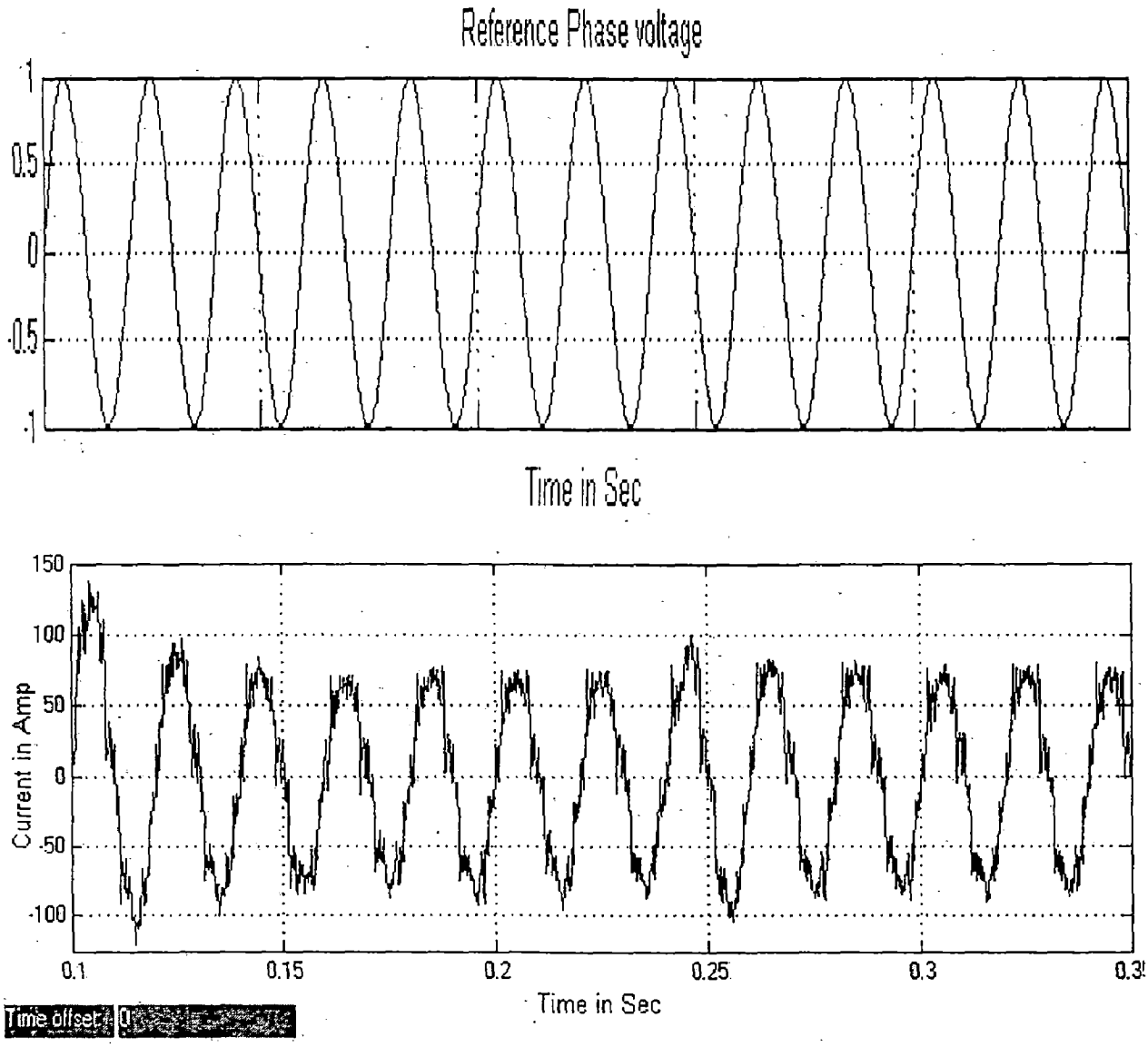
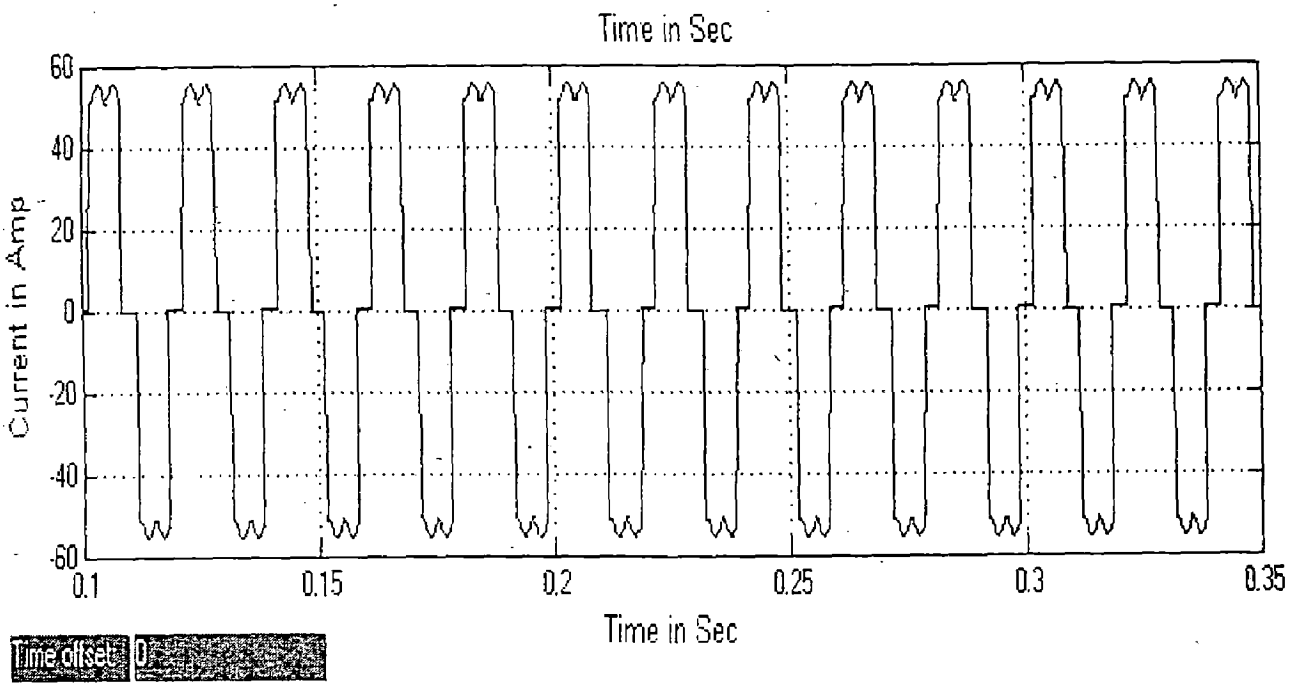


Fig 4.9 Reference phase voltage and respective input line current



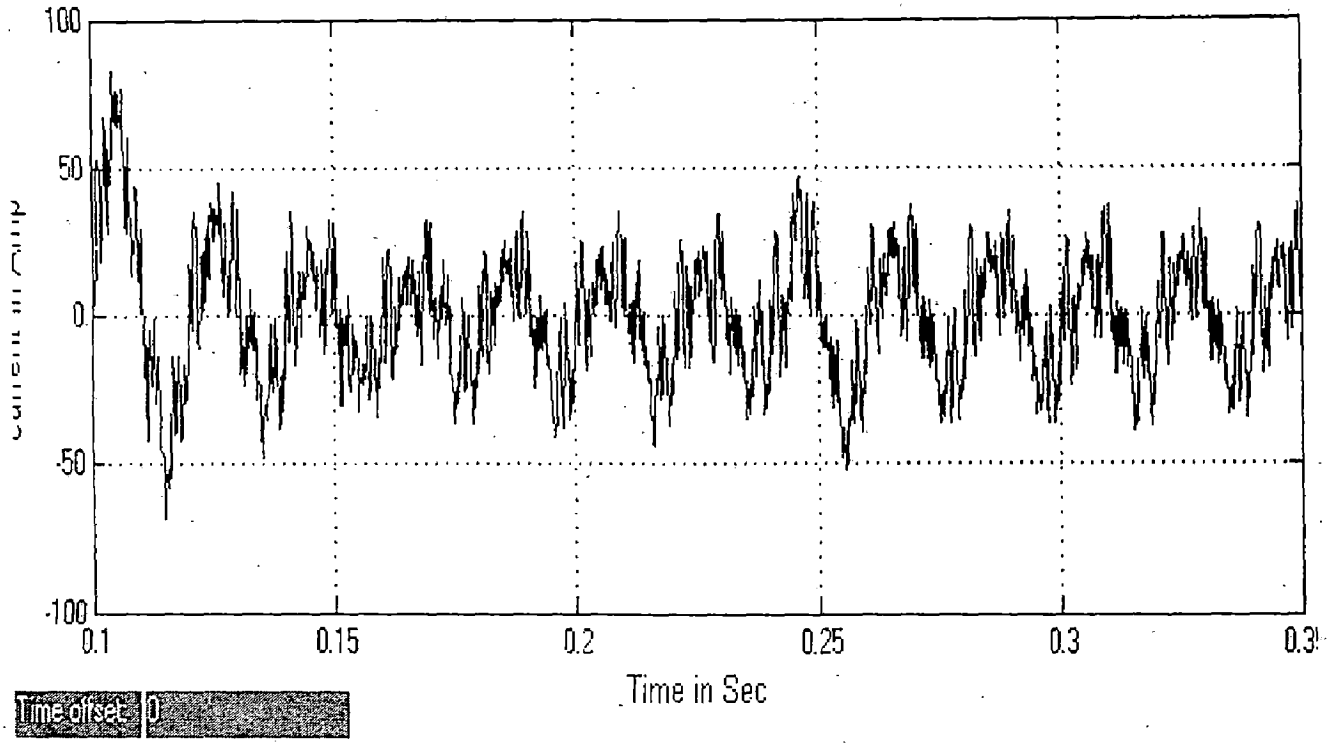
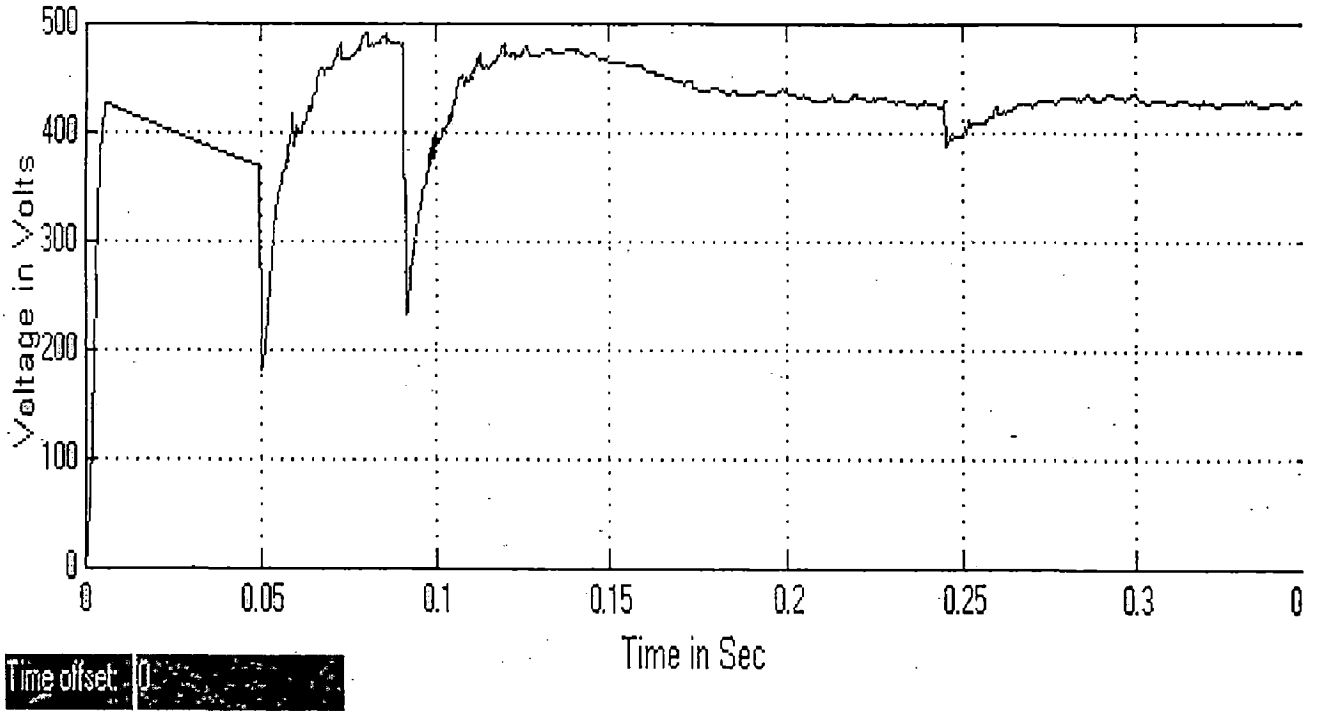


Fig 4.10 Converter compensating Current and Load current



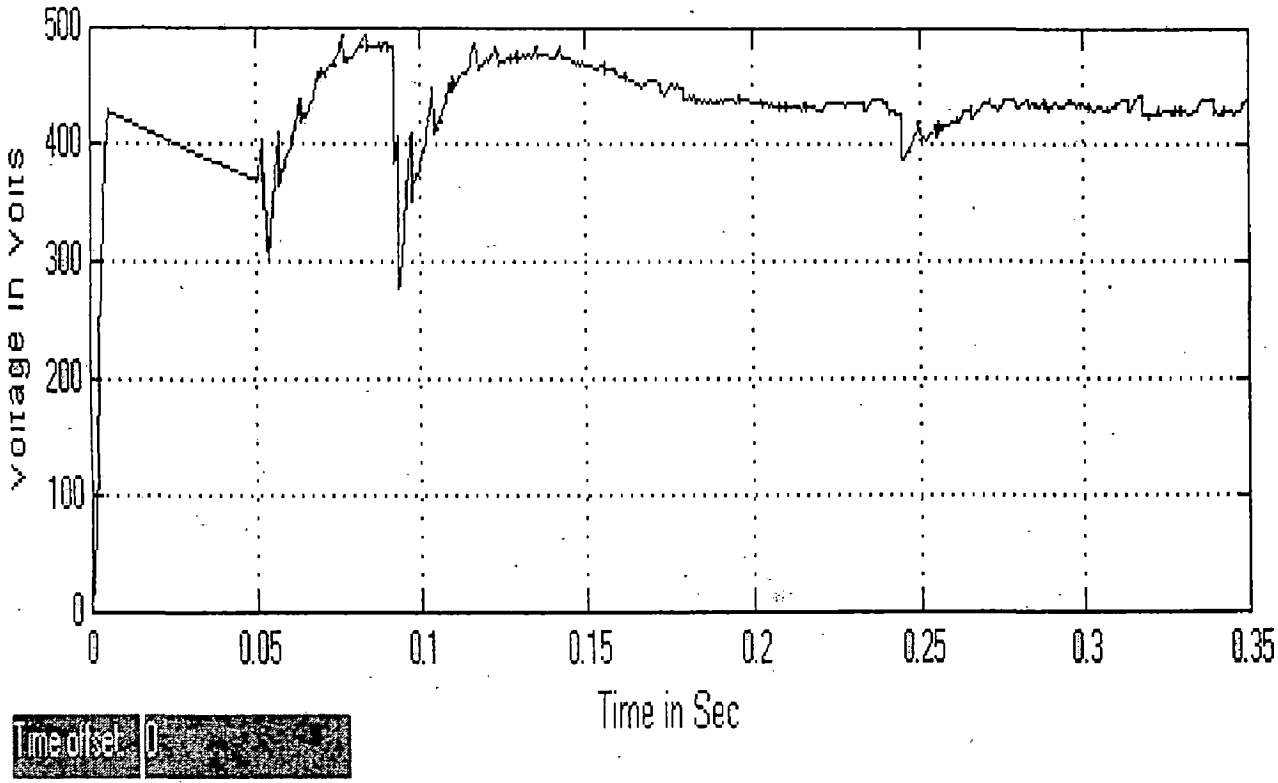


Fig 4.11 Upper and Lower Capacitor Voltages

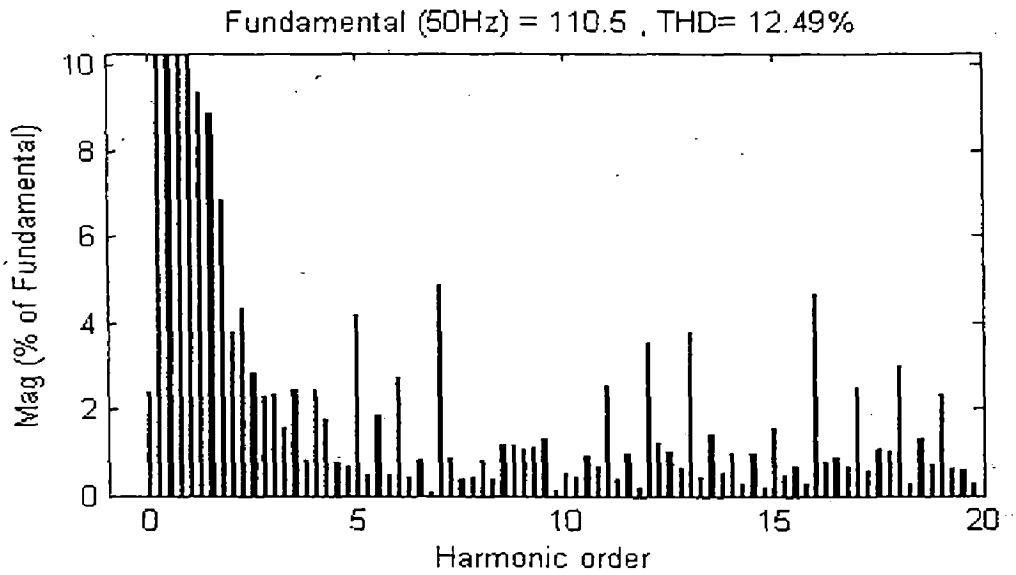


Fig 4.12 THD analysis of Input Source Current

b) At Carrier Frequency = 5 kHz

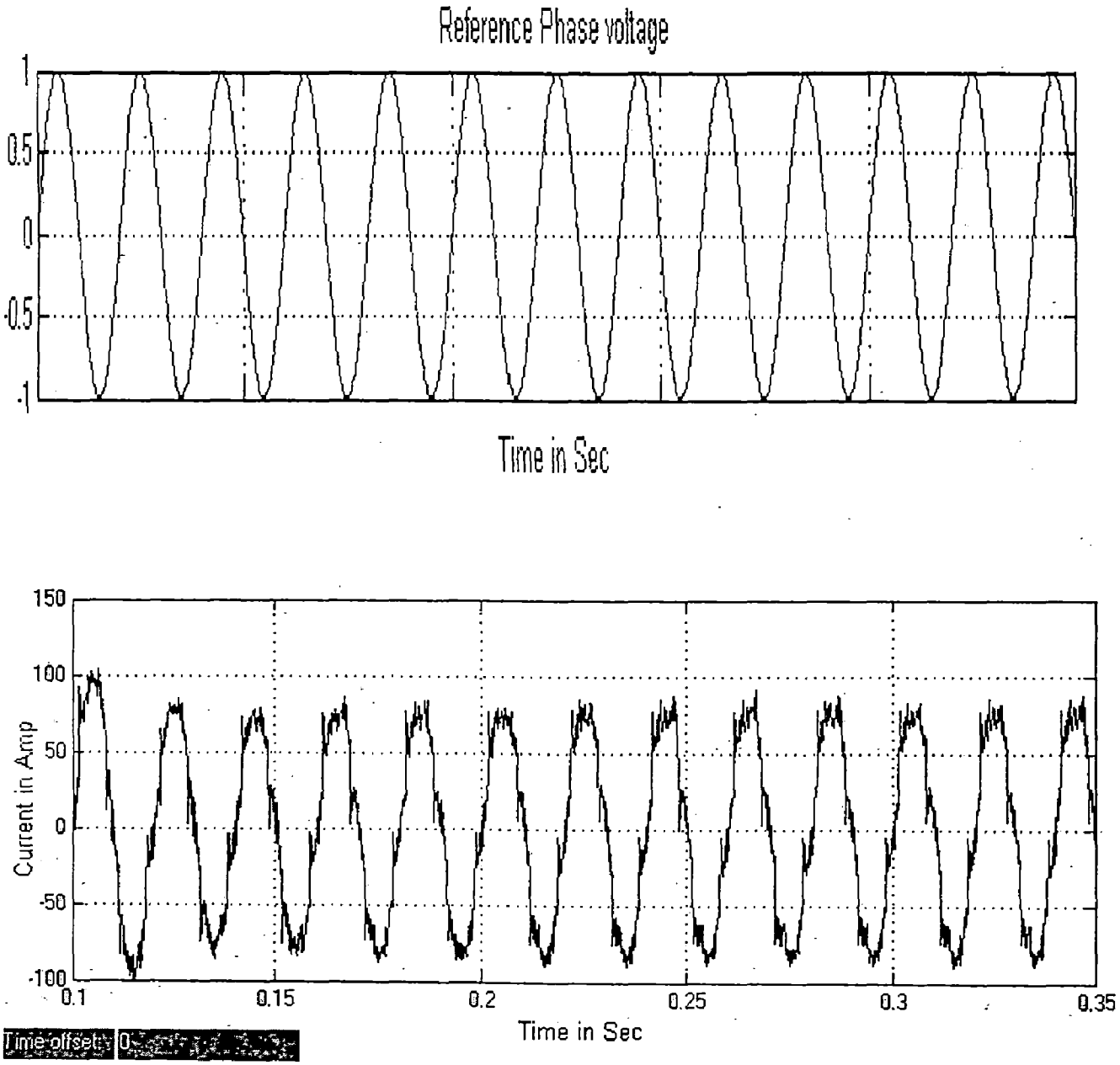
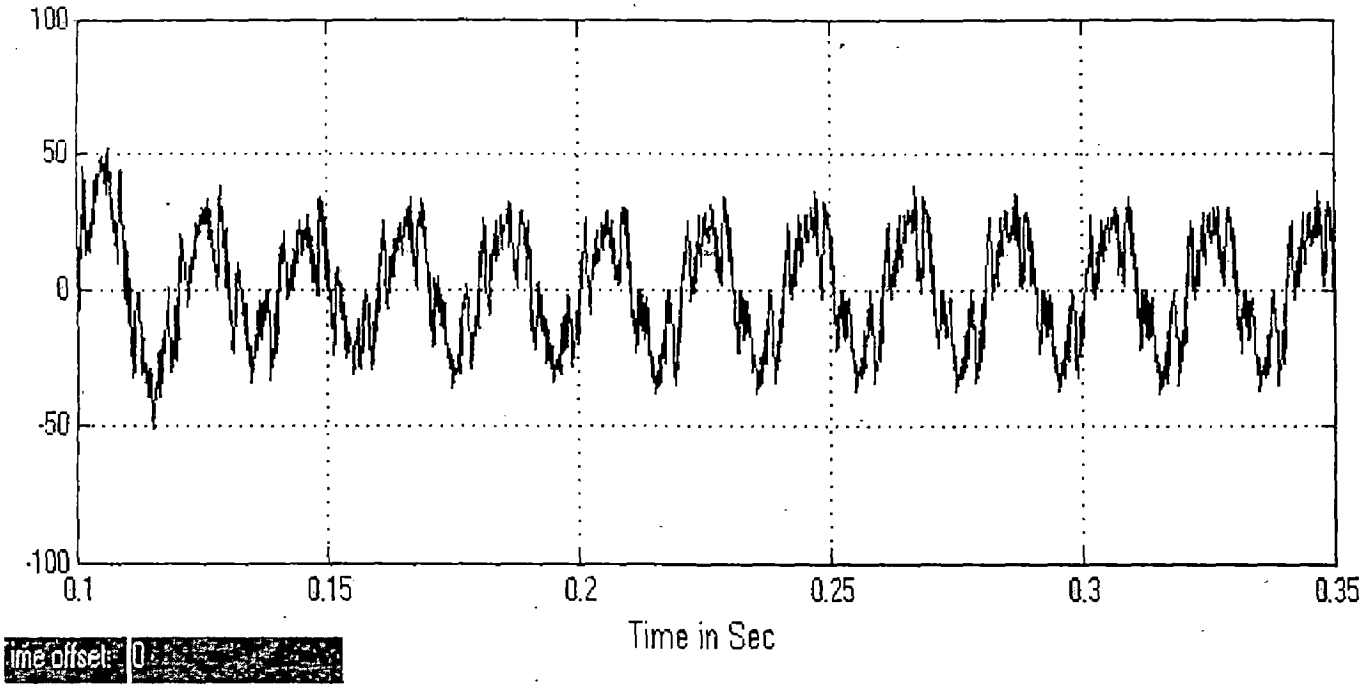


Fig 4.13 Reference phase voltage and respective input line current



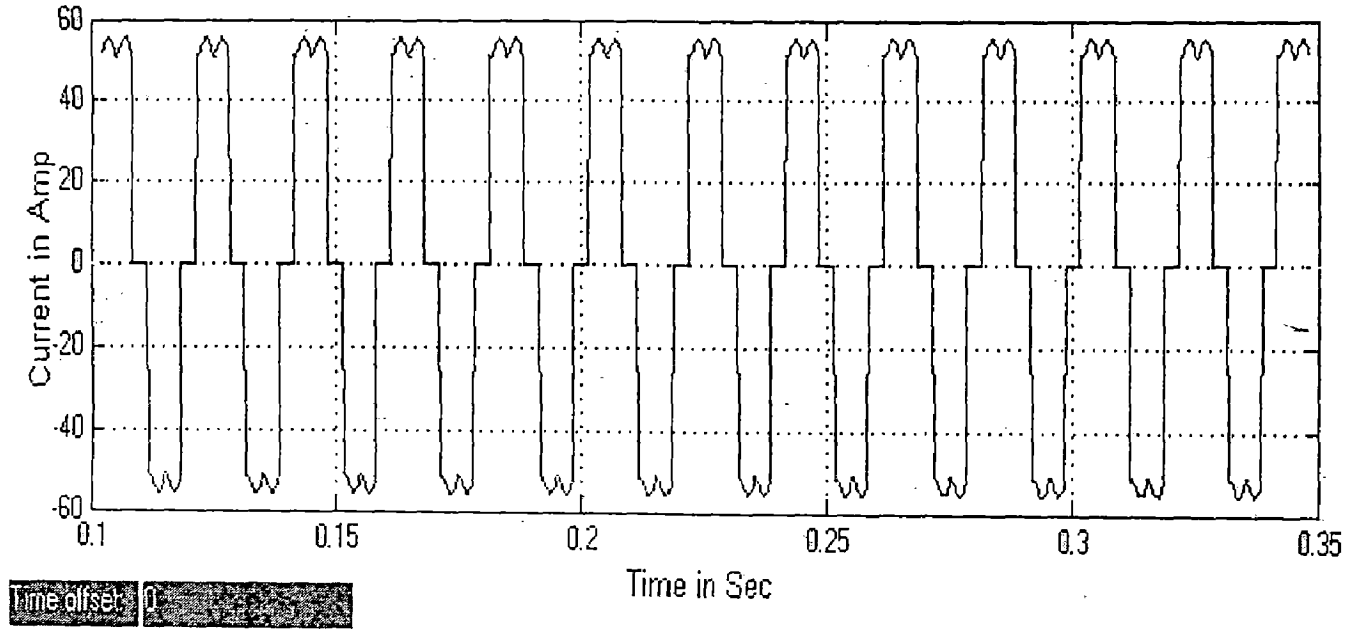
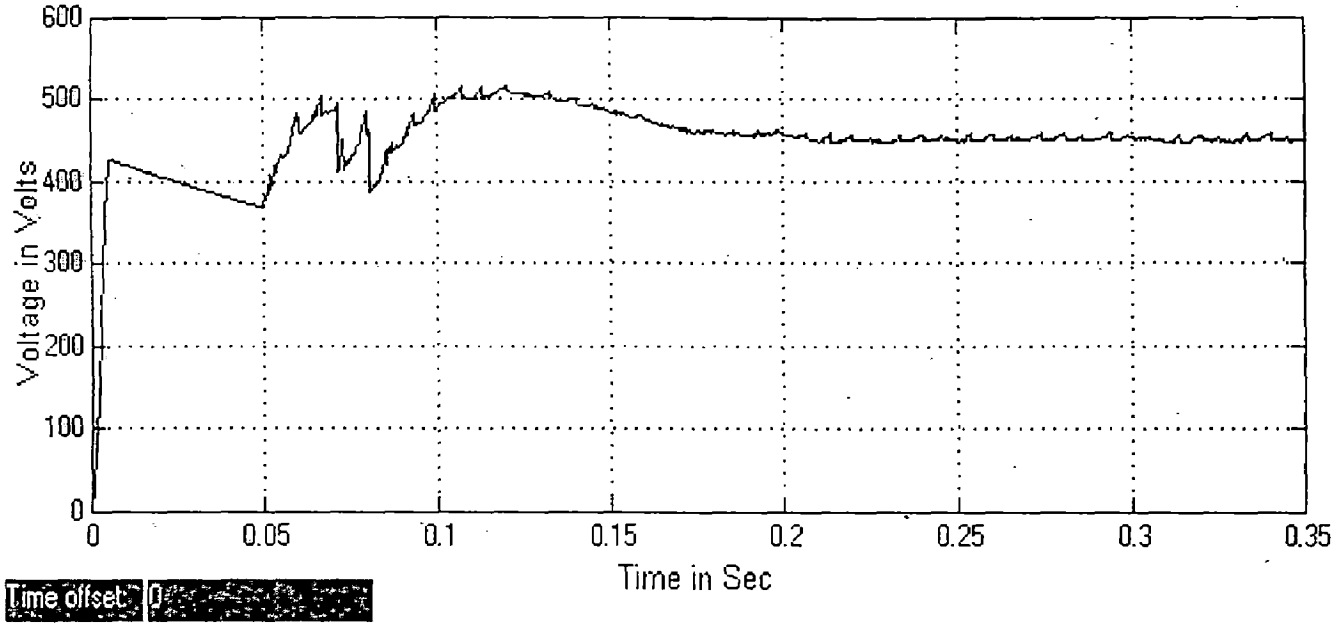


Fig 4.14 Converter compensating Current and Load current



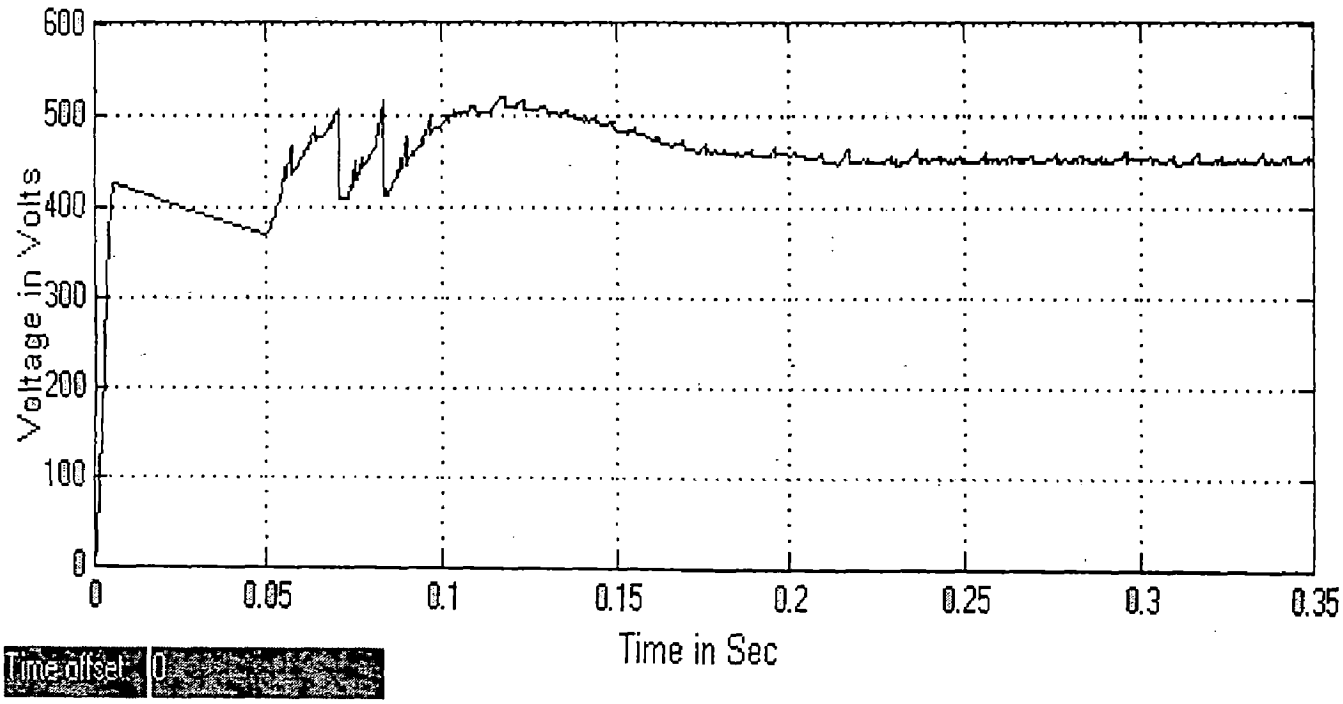


Fig 4.15 Upper and Lower Capacitor Voltages

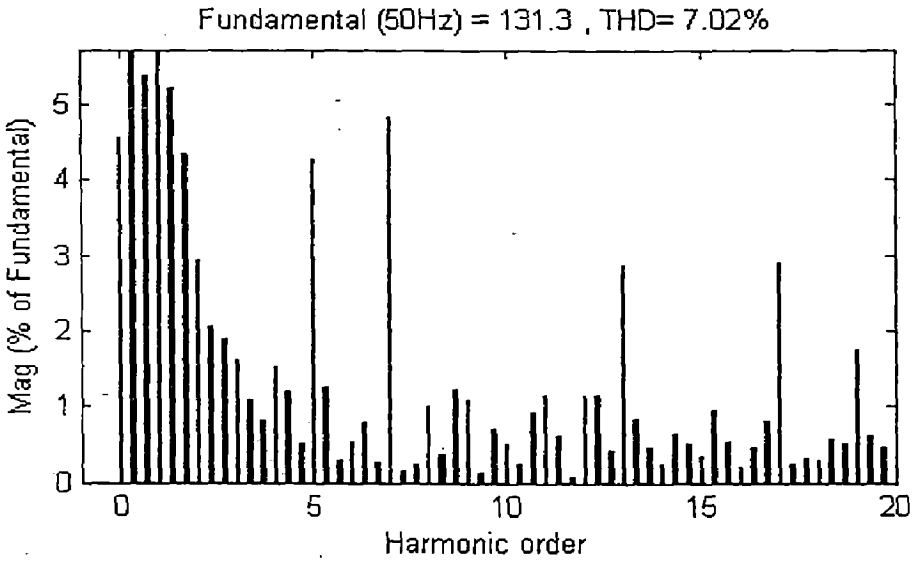


Fig 4.16 THD analysis of Input Source Current

As seen from the above waveforms it has been observed that the input phase voltage and input line current are in phase and with unity power factor. The main problem in multilevel converter is the capacitor voltage unbalancing. Using this control scheme it have been observed that the voltage across each capacitor is equal, constant and balance. Thus operating the multilevel converter as an active power filter and rectifier. It will operate as an active power filter and rectifier at the same time when we connect two resistances across the capacitors.

As seen from the above wave forms it has been observed that, as we are increasing the carrier frequency of triangular waves the input line currents are becoming more sinusoidal and the THD of the input line currents are reducing.

4.3.2 Control scheme operation as an active power filter :

a) At Carrier Frequency = 1kHz

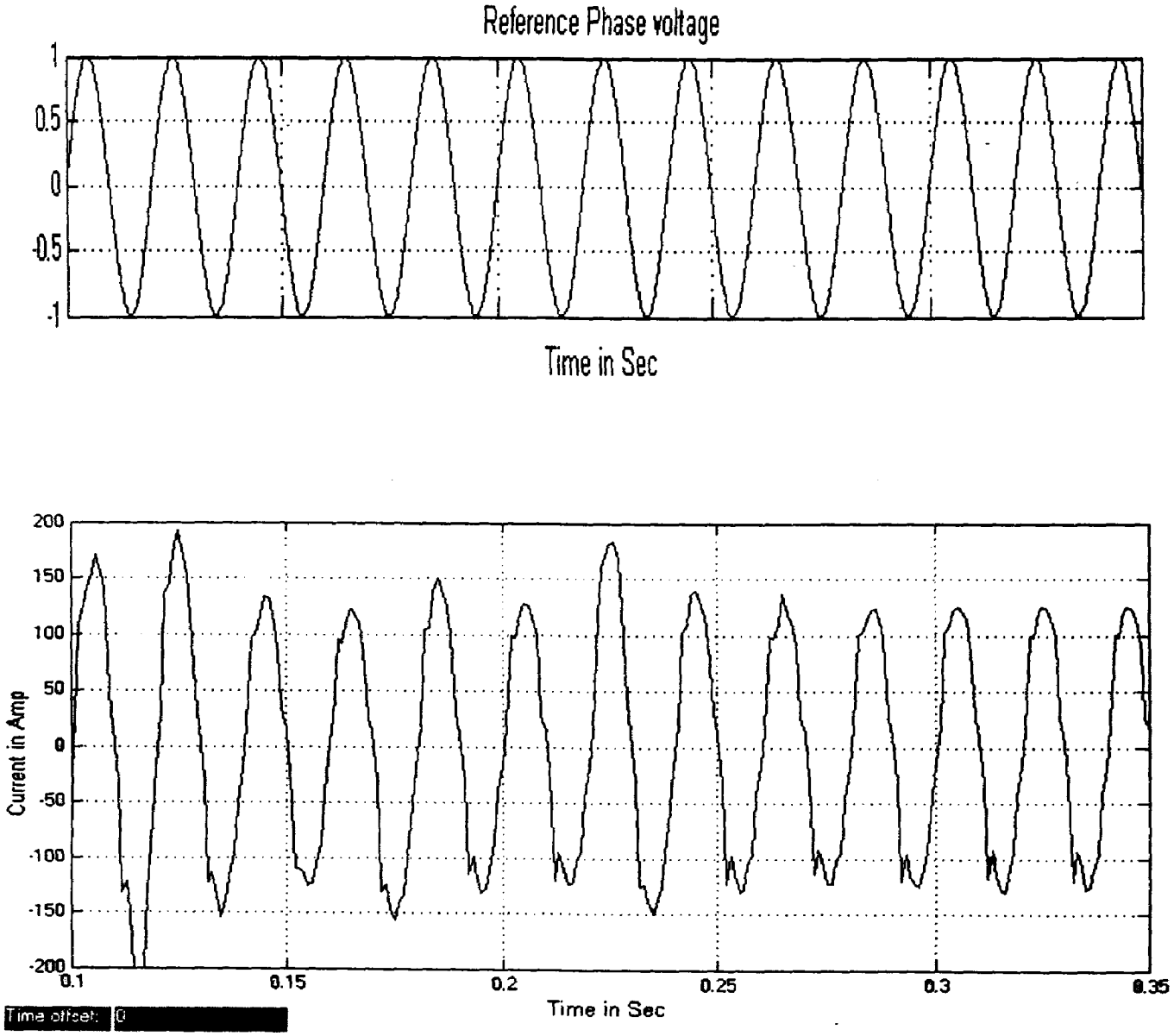
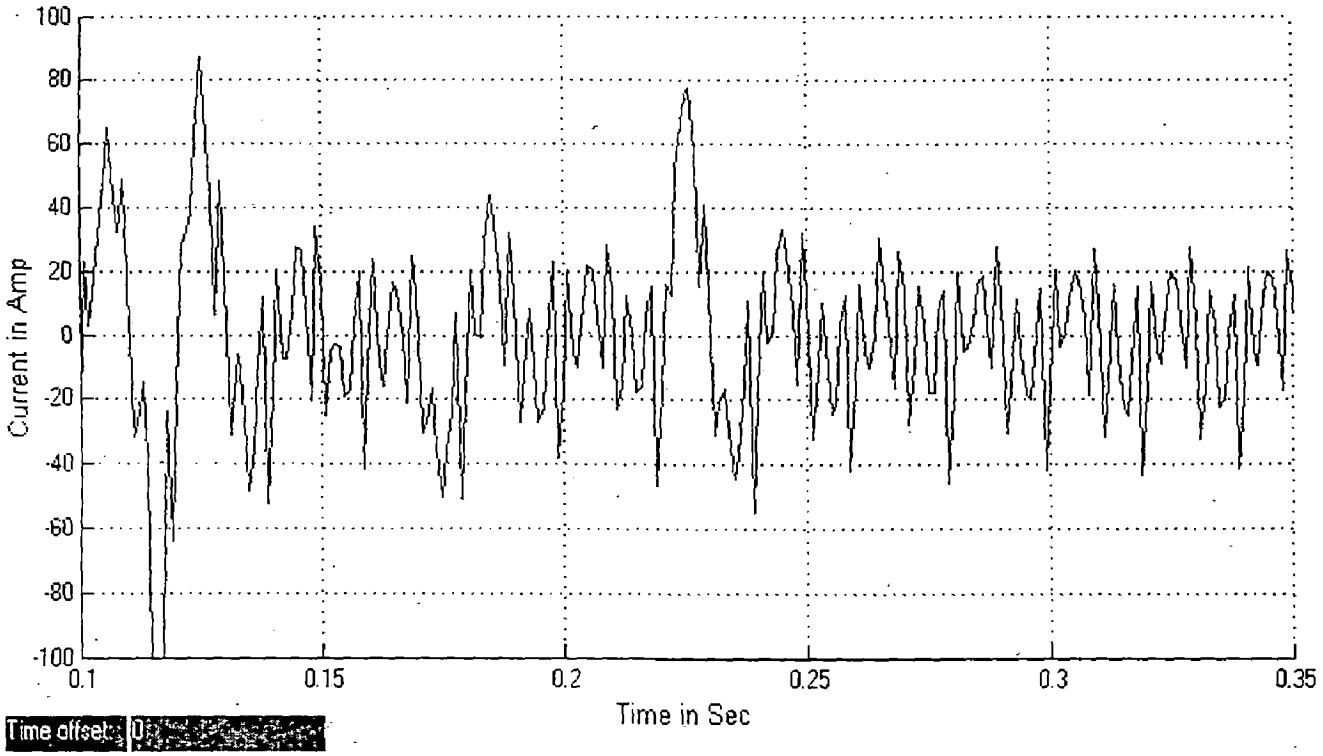


Fig 4.17 Reference input phase voltage and respective input line current



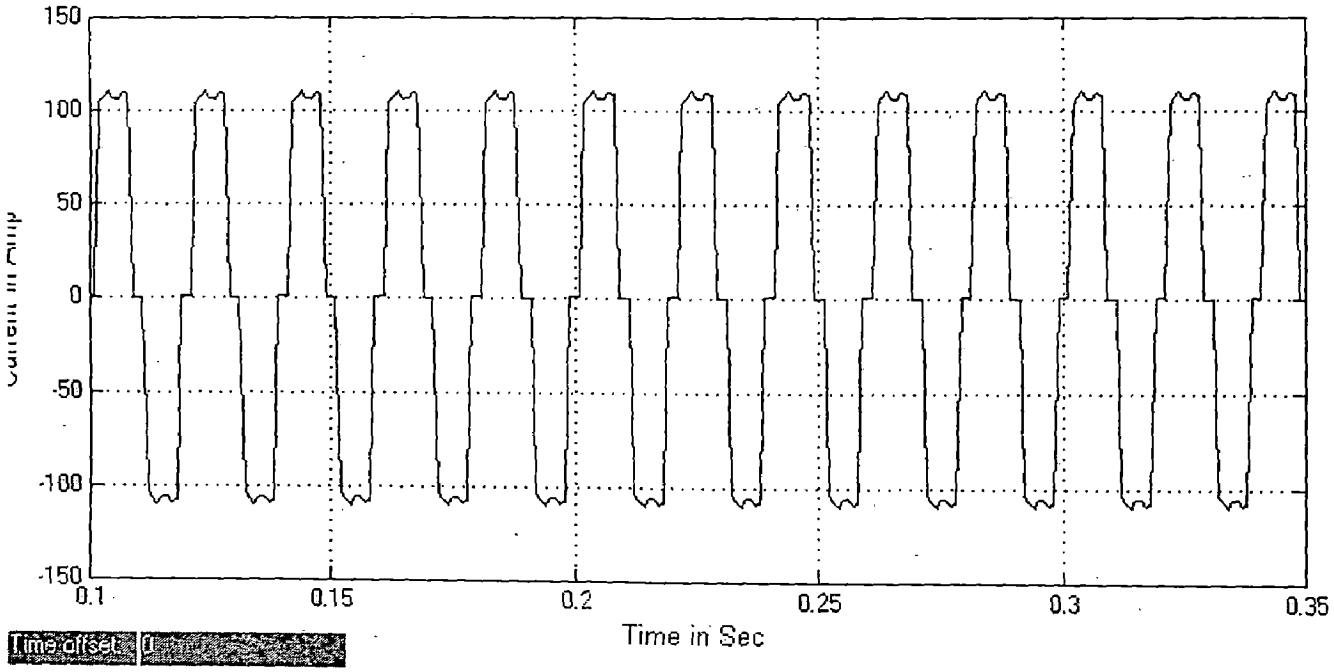
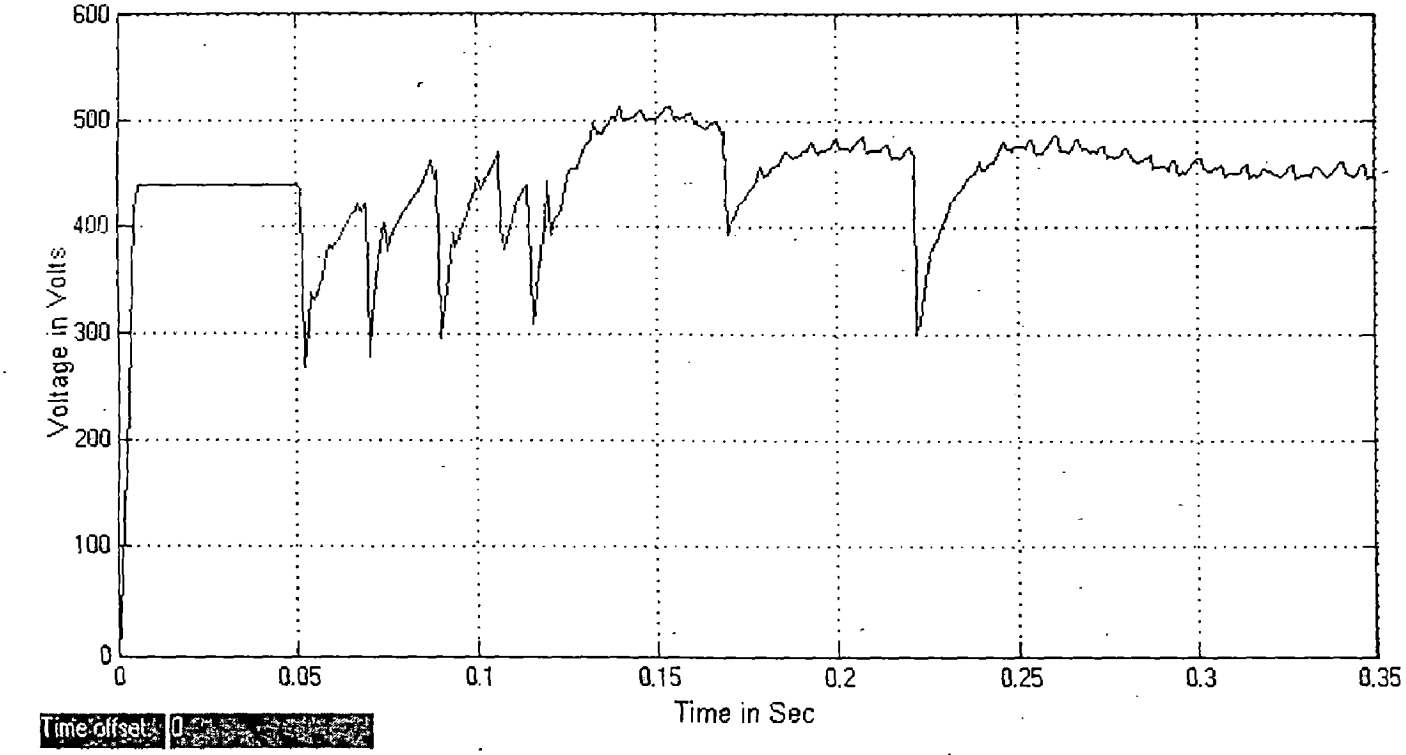
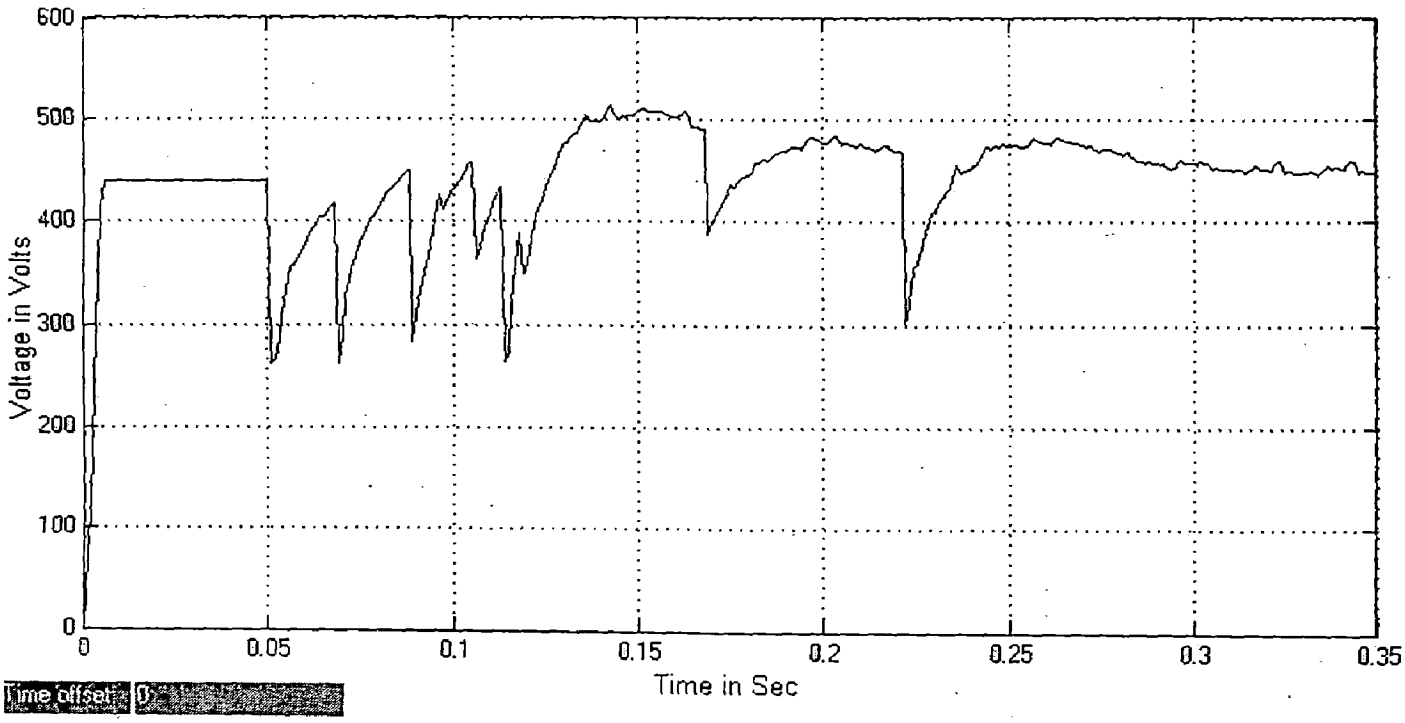
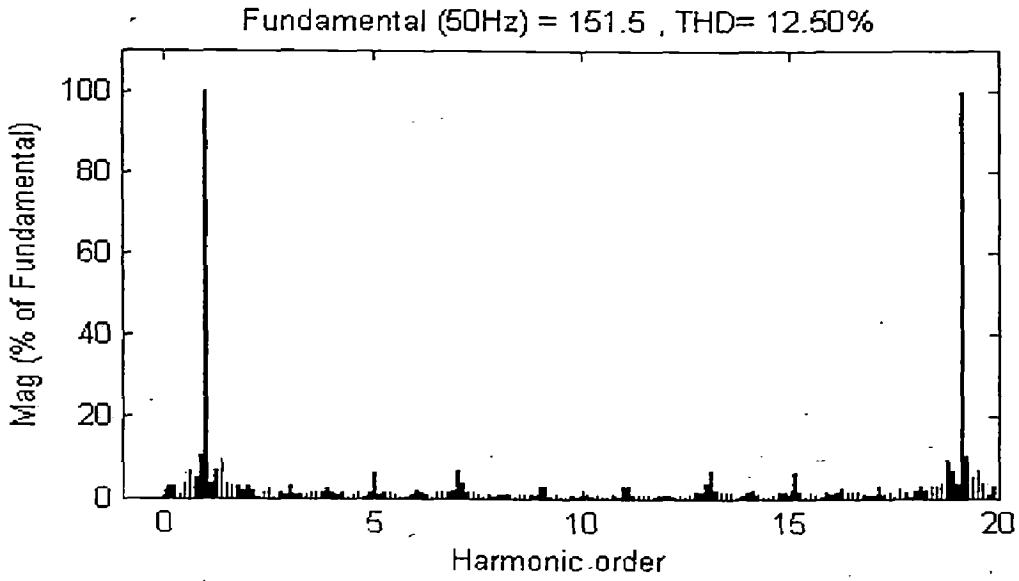


Fig 4.18 Compensating converter current and Load current





4.19 Voltages across the upper and lower capacitors



4.20 THD analysis of Input line Current

4.2.2.2 At Carrier Frequency = 5kHz

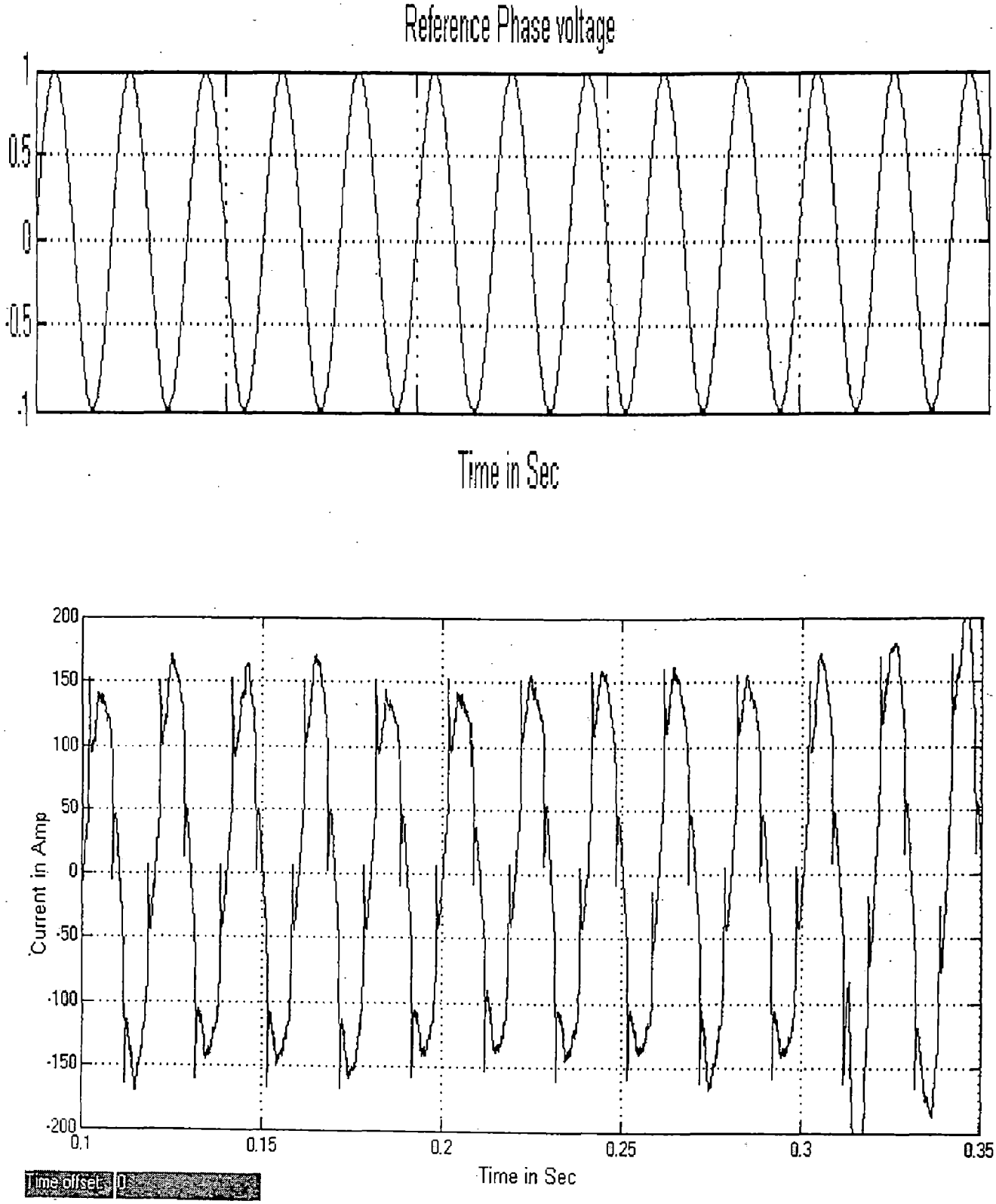


Fig 4.21. Reference Voltage and Input Line Current

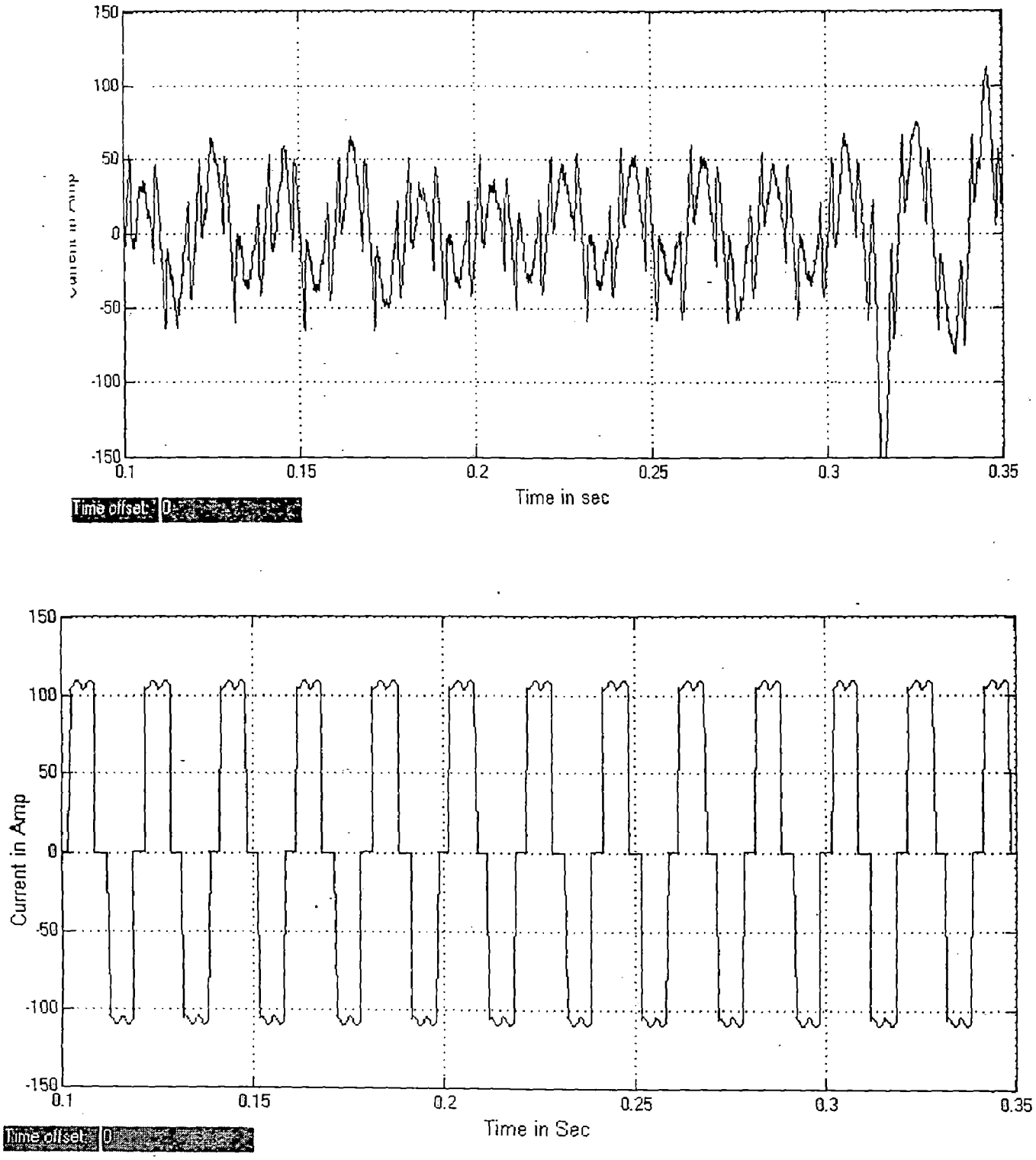


Fig 4.22. Converter Current and Load Current

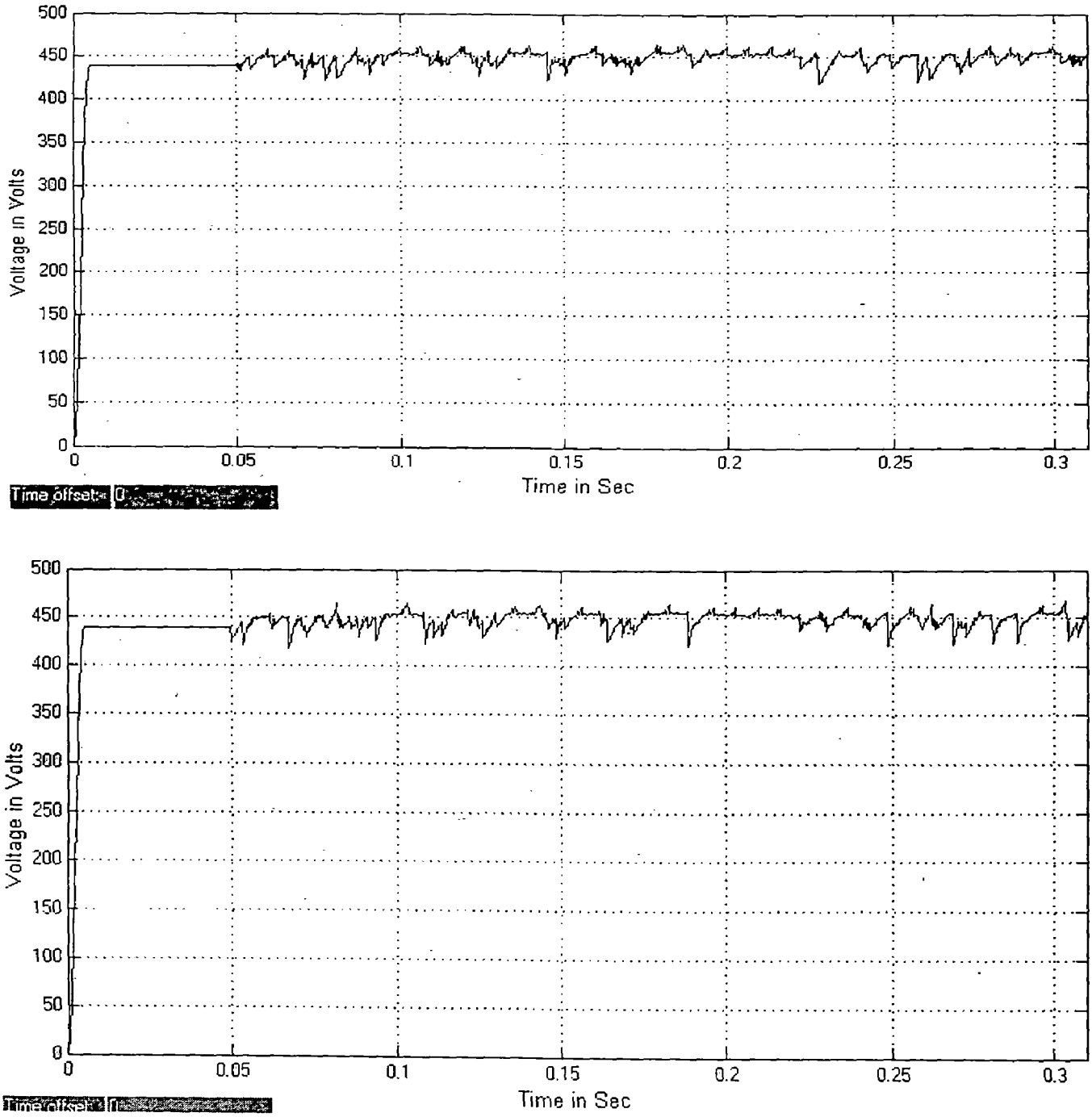


Fig 4.23 Upper and Lower Capacitor Voltage

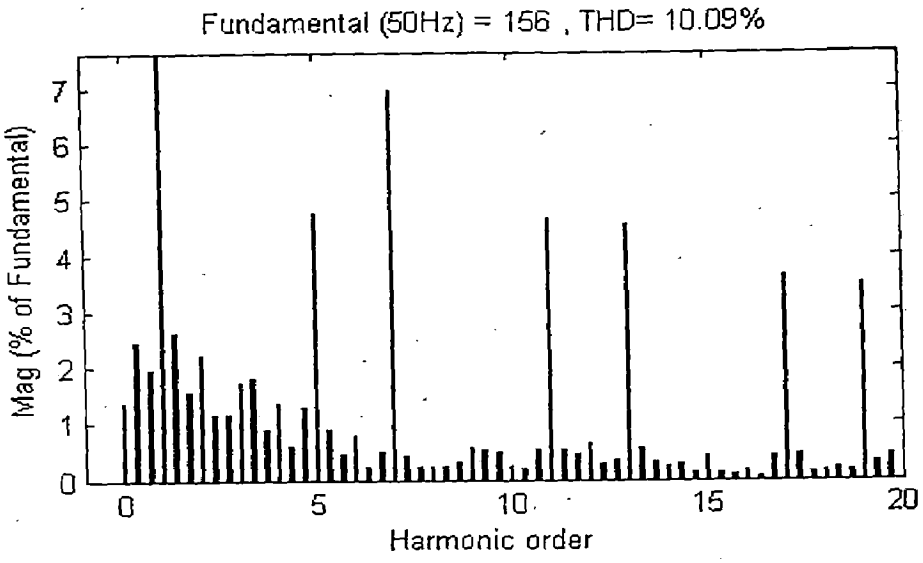


Fig 4.24 THD analysis of Input Line Current and Converter Current

The converter operates as an active power filter only when we remove the resistance across the capacitors. As seen from the above waveforms it have been observed that the input phase voltage and input line current are in phase and with unity power factor. The main problem in multilevel converter is the capacitor voltage unbalancing. Using this control scheme it has been observed that the voltage across each capacitor is equal and balance. Thus operating the multilevel converter as an active power filter.

As seen from the above wave forms it has been observed that, as we are increasing the carrier frequency of triangular waves the input line currents are becoming more sinusoidal and the THD of the input line currents are reducing.

Conclusions

Simulation of control scheme to operate the multilevel converter as a rectifier or as an active power filter or both at the same time was carrier out. It have been observed that in both the multilevel converter operating as a rectifier or as an active power filter the THD of the current waveforms improves as the carrier switching frequency is increased. It have been also observed that the voltage across each capacitor is maintained constant,

balanced and equal. The total dc bus voltage is also forced to be equal, balanced and constant at the specified dc bus voltage.

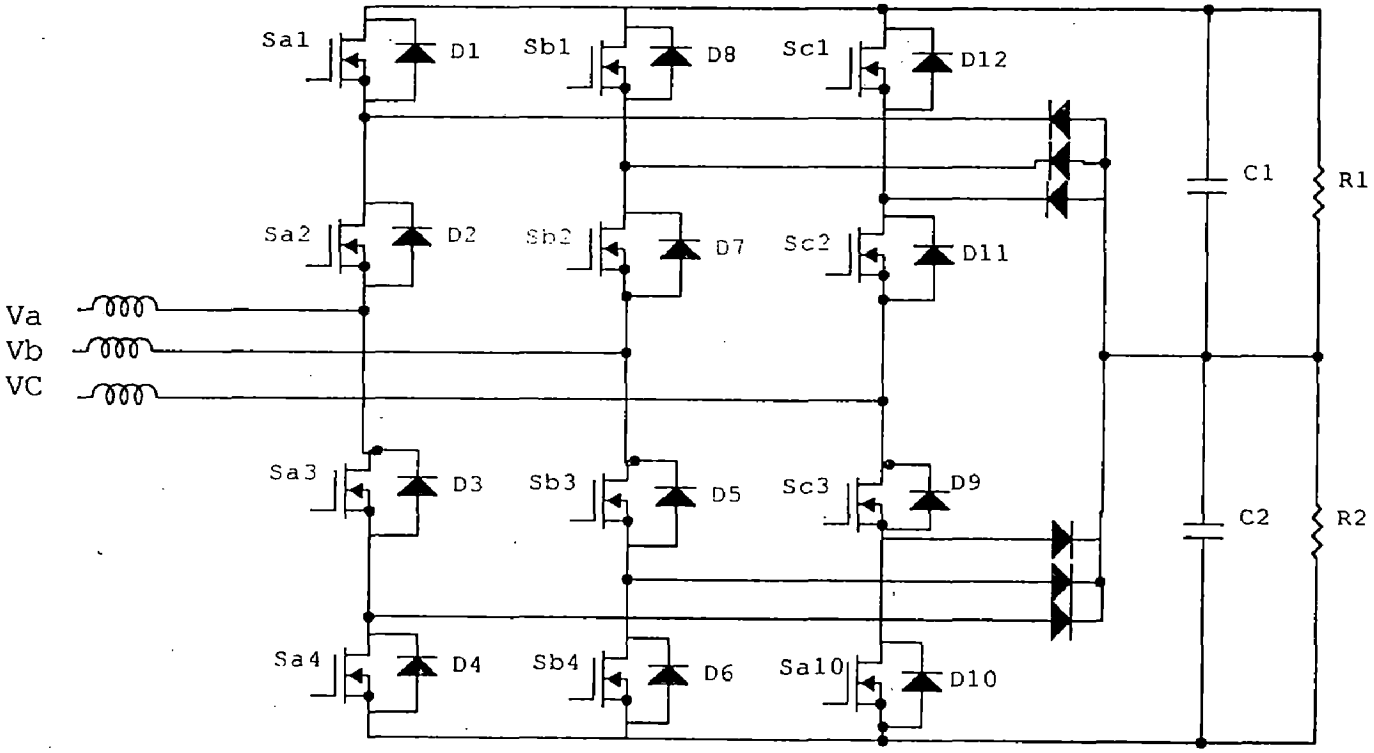
Chapter 5

SYSTEM DEVELOPMENT

5.1 Introduction

In this chapter hardware requirement for the control scheme and the multilevel converter have been explained. In this control scheme, the multilevel converter used is a Three-level converter. Mosfets IRFP460 have been used to construct the power circuit for the three-level converter. Triangular carrier wave generation circuits, reference current generation circuit, Current sensing circuit, total voltage controller and differential voltage controller circuit has been developed using opamps and other analog devices.

5.2 Power Circuit Diagram for Three-level Converter



5.1 Power Circuit

Mosfets IRP460 are used as switching device for multilevel converter. For a m-level converter the number of switches required for per phase leg = 2*(m-1).

Clamping diodes required per phase per leg = (m-1)*(m-2)

DC link capacitors required for m-level converter = (m-1)/2

In this circuit we are using Three-level converter, therefore m=3.

Total number of mosfets required for three level converter=12

Total clamping diodes required = 6

DC link capacitors =2.

Capacitors rating = 2200 μf. 450V

5.3 Snubber circuit:

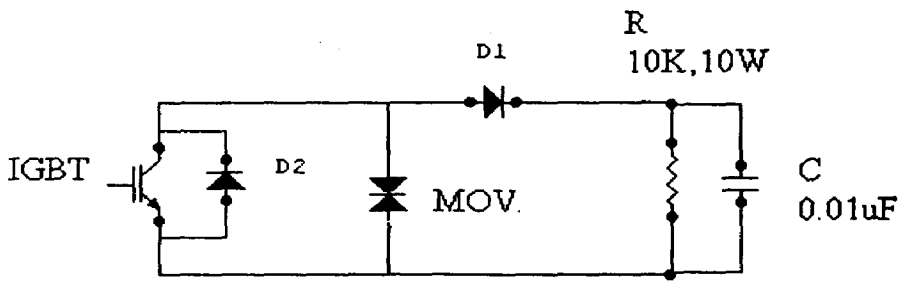


Fig 5.2 Snubber circuit

An RC snubber circuit is used to reduce the dv/dt switching, as IGBT is sensitive to over voltages emitter and collector. The diode prevents the discharging of capacitor via the switching device, which could damage the device owing to large discharge current.

An additional protective device metal–oxide-varistor (MOV) is used across each device to provide the protection against the over voltages. MOV acts as a back to back zener and by passes the transient over voltages across the devices.

Energy Stored in Capacitor C = ½ * $C*V_{dc}^2$

Power = E_c*fmax

This is the power to be dissipated in the resistance R. Where V_{dc} is the maximum DC level an fmax is the maximum frequency of the output wave.

This energy is needed to be dissipated within T_{on}.

Switching frequency fmax = 5kHz.

Time constant for the RC circuit is taken as one-fifth of T_{on}(min), therefore

$T_{RC} = 1/(5*6*fmax) = R*C$.

Constant Power loss for the worst case is given by

$P = V_{dc}^2/R$.

Assuming C = 0.01μf

R = 3kΩ, 5W

5.4 Pulse Amplification and Isolation circuit

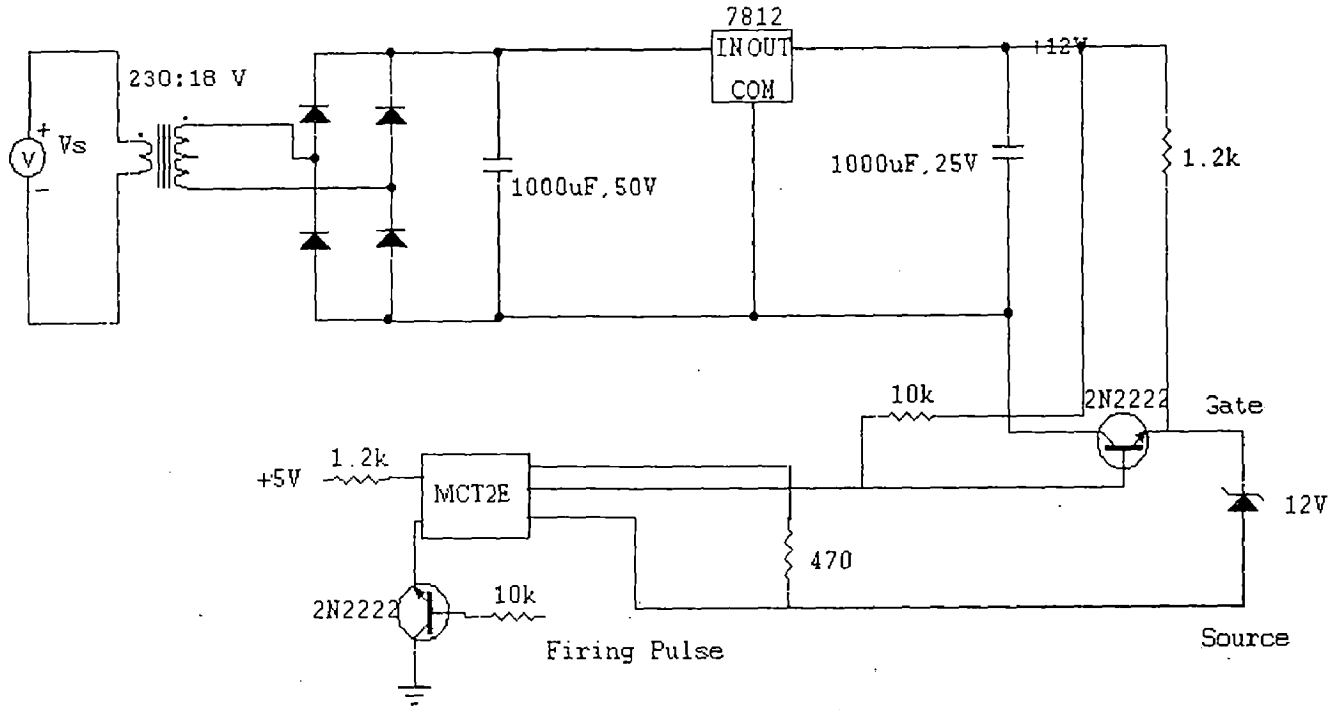


Fig 5.3 Pulse amplification and isolation circuit

MCT2E → opto coupler (provides isolation between power circuit and control circuit

7812 → +12V voltage regulators.

5.5 Power Supplies

DC regulated power supplies (+12V, -12V, +5V) are required for providing the biasing to various transistors, IC's etc. The circuit diagram for various dc regulated power supplies are shown in fig 11 and fig 12.. in it the single phase ac voltage is stepped down and then rectified using diode bridge rectifier. A capacitor of 1000micro farad, 50 V is connected at the output of the bridge rectifier for smoothening out the ripples in the rectified DC voltage of each supply. Voltage regulators chips 7812,7912, and 7805 are used for obtaining the DC regulated voltages, +12V, -12V and +5V respectively. A capacitor of 1000μf, 50V is connected at the output of the IC voltage regulator of each supply for obtaining the constant and ripple free DC voltage.

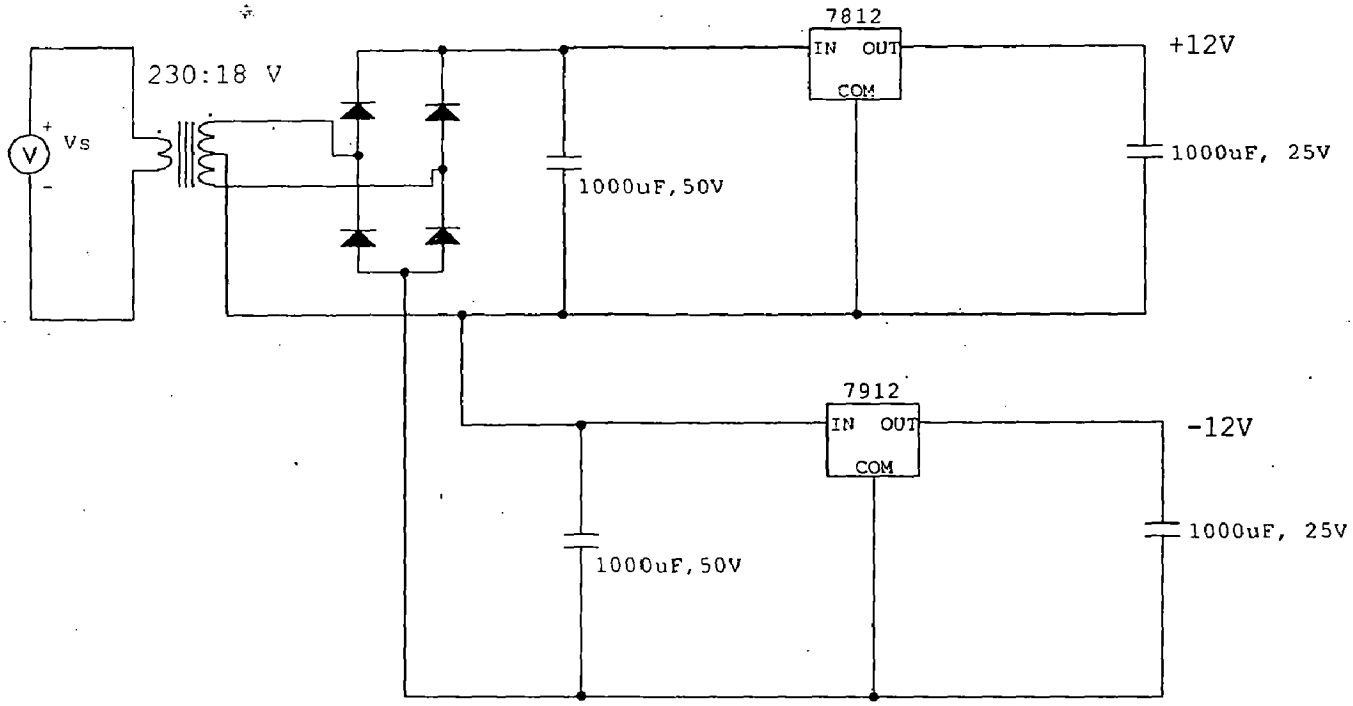


Fig 5.4 a +12, -12 Power Supply

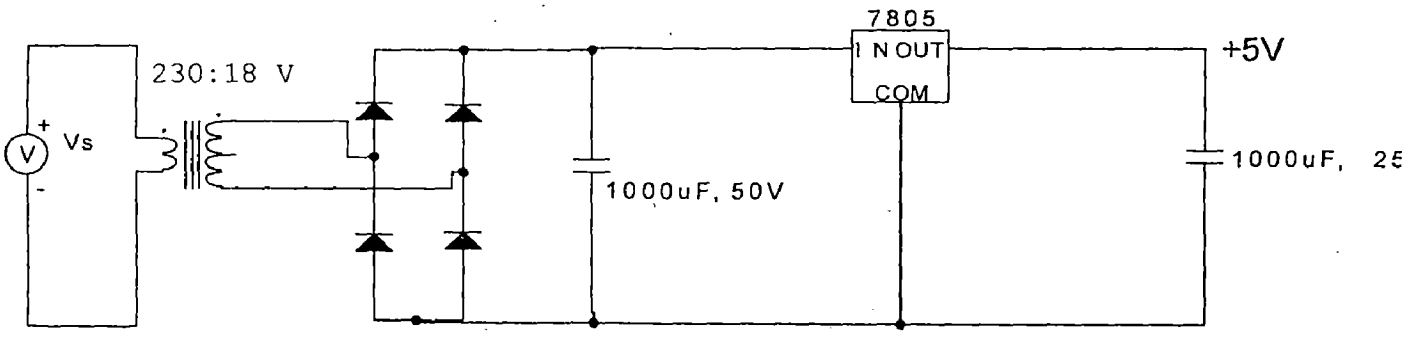


Fig 5.4b +5 Volt Power Supply

5.6 Current Sensing Circuit

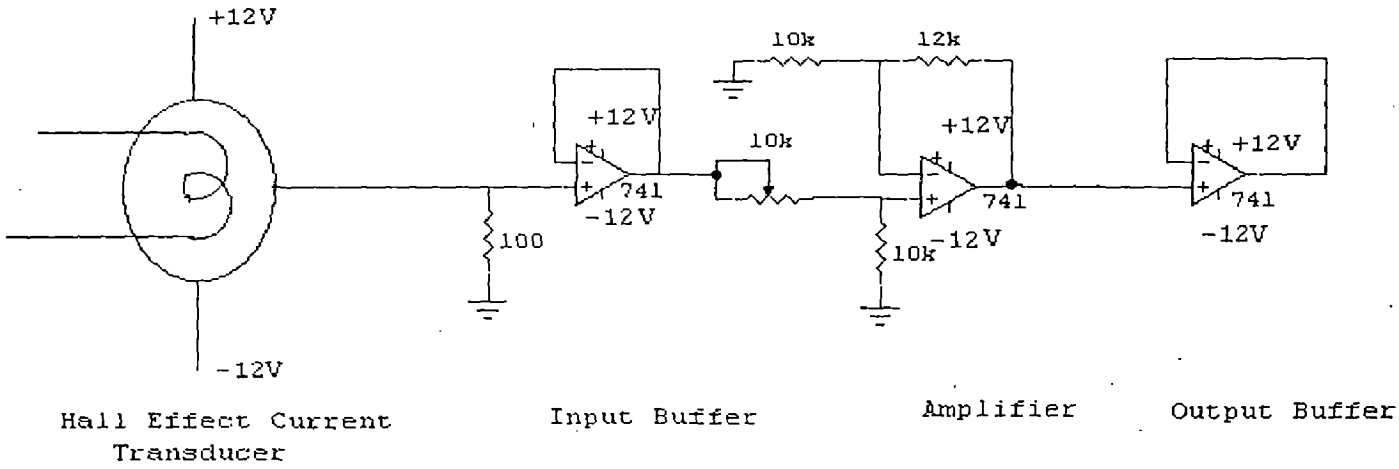


Fig 5.5 Current Sensing Circuit

Closed loop Hall Effect current transducer is used to sense the current. The transducer use the ampere turn compensation method to enable the measurement of current from DC to high frequency with an ability to follow rapidly changing level or wave shapes. The application of primary current (Ip) causes a change in flux in the air gap. This in turn produces a change in output from hall element away from the steady state condition. This output is amplified to produce a current (Is), which is passed through a secondary winding causing a magnetizing force to oppose that of the primary current, thereby reducing the air gap flux. The secondary current is increased until the flux is reduced to zero. At this point the hall element output will return increased until the flux is reduced to zero. At this point the hall element output will return to steady state condition and the ampere-turn product of secondary circuit will match that of primary.

The current that passes through the secondary winding is the output current. The transformation ratio is calculated by the standard current transformation equation

$$NpIp=NsIs$$

Where

Np= primary current

Ns= secondary current

Ip= primary current and Is = Secondary Current

5.7 Triangular Carrier Generator:

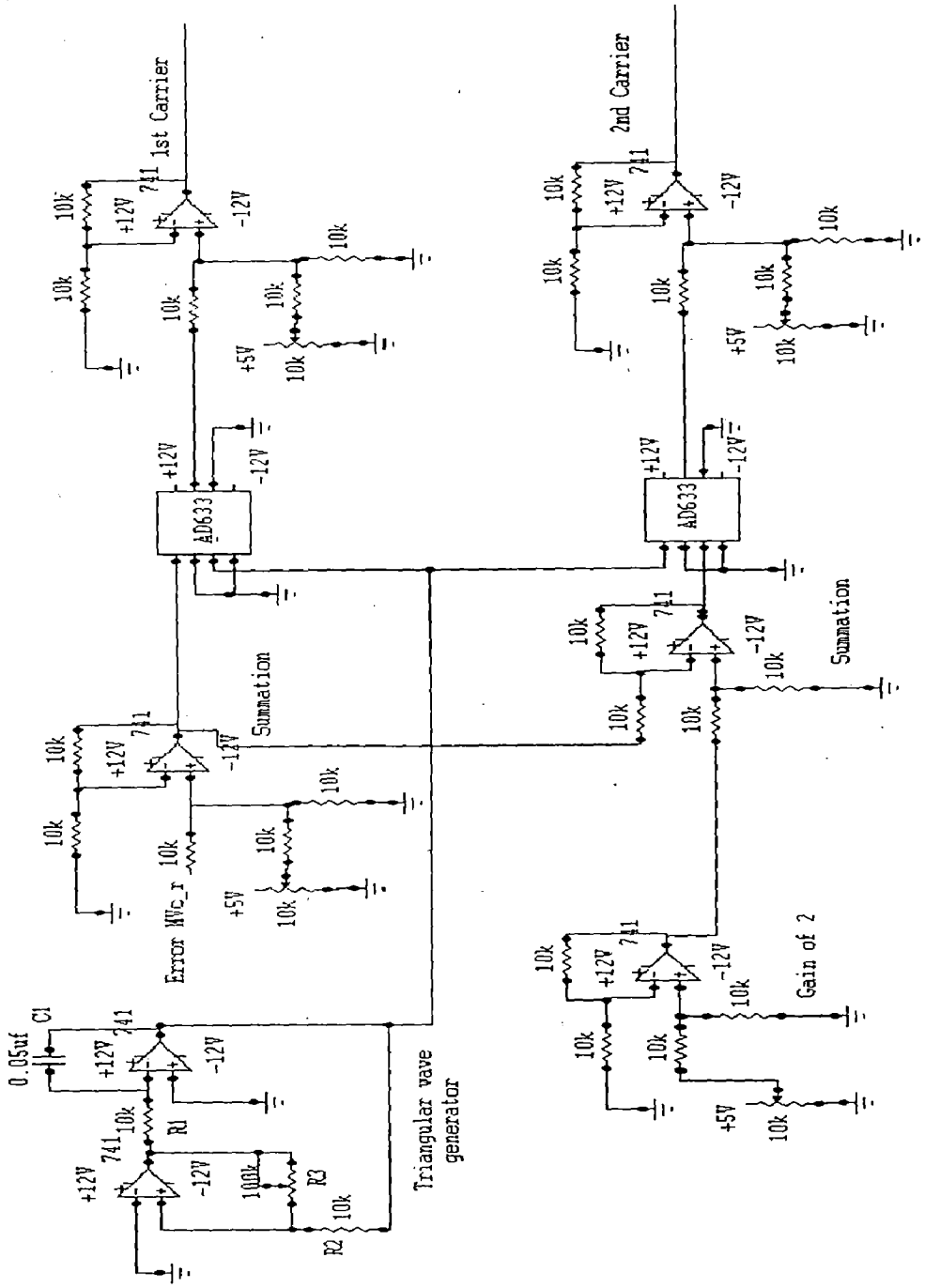


Fig 5.6 Triangular carrier Generators

The circuit diagram given in fig generates two triangular carrier waveforms, which is implemented on the basis of algorithm shown in fig 3.4. The two triangular carriers are complementary modified on the basis of error signal MVc_R (Difference

between the Two capacitors voltages). The two triangular carrier waveforms are then compared with the current error signal to generate the gating signals.

The amplitude and frequency of triangular wave can be determines as follows:

The triangular waveform generator has two opamps 741. When the output of first opamp (comparator) is $+V_{sat}$, the output of second opamp (integrator) steadily decreases until it reaches $-V_{Ramp}$. At this time the output of the first opamp switches from $+V_{sat}$ to $-V_{sat}$. Just before this switching occurs, the output voltage is 0V. This means that the –Vramp must be developed across R_2, and $+V_{sat}$ must be developed across R_3.

$$-Vramp/ R_2 = -V_{sat} / R_3.$$

$$-Vramp = R_2 / R_3 \ (-V_{sat}).$$

The Frequency of Oscillation is given by

$$Fo = R_3/ (4*R_1*R_2*C1).$$

$R1 = R2 = 10k\Omega$

$R3 = 100k\Omega$ pot

$C1 = 0.01\mu f.$

5.8 Generation of Reference Current:

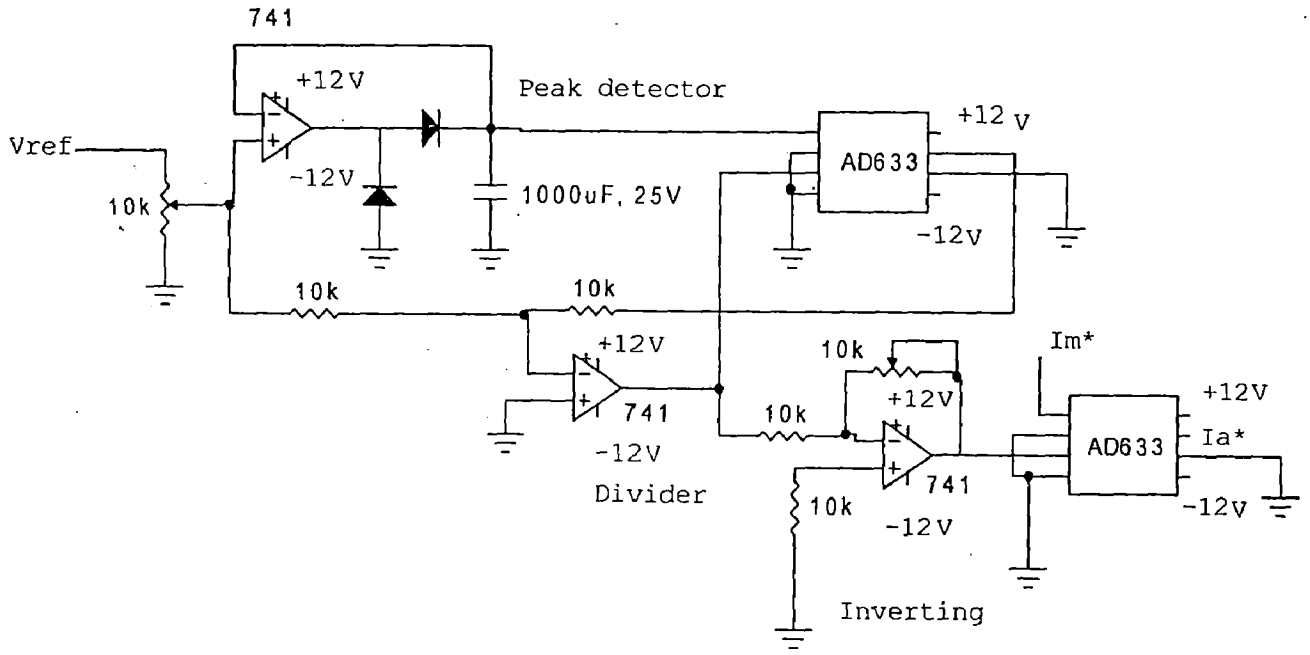


Fig 5.7 Current Reference Generation circuit

Reference voltage is obtained from the circuit shown in fig 5.7, which is in phase with the input voltage. The peak detector circuit generates the peak amplitude voltage of reference voltage . In the peak detecting circuit diode D2 conducts during the negative half cycle of Vref and hence prevents the opamp from going into negative saturation. The divider circuit divides the reference circuit with peak amplitude of the wave. The output of divider circuit is negative in nature and hence it is inverted with the help of inverting circuit. Now the output is a unit voltage signal. This unit voltage signal is now multiplied with the peak reference current Im* value by making use of IC AD633 which gives us reference current Ia*. Im* is obtained by comparing the sum of the two dc bus capacitors voltage (Vc1+Vc2) with the total required reference DC bus voltage V_{dc}.

5.9 Current Error Signal

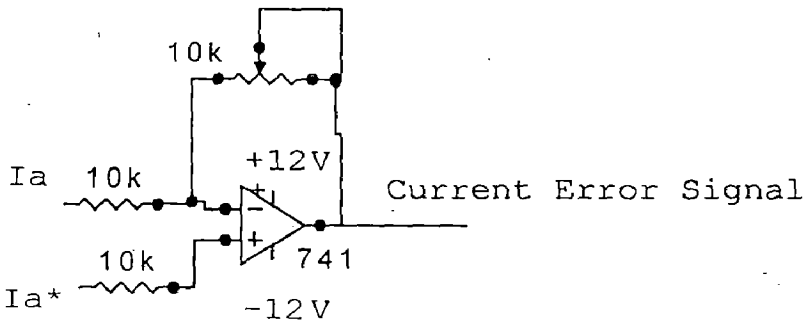


Fig 5.8 Current Error Circuit

The reference current generated is compared with current obtained by current sensor circuit to obtain the current error signal, which will be then compared with the triangular carrier waveforms to obtain the respective firing gating pulses for three level converter.

Since in this control scheme we are using three-phase supply we will have to generate three reference signals and three current sensing circuits will be required. Each phase will produce its current error signal, which will be compared with the carrier waveforms to produce the gating signals to operate the three level converters.

5.10 DC Voltage sensing

To sense the dc voltage across the capacitors AD202 isolation amplifier is used, which provides isolation between the input and output stages through the use of internal transformer coupling.

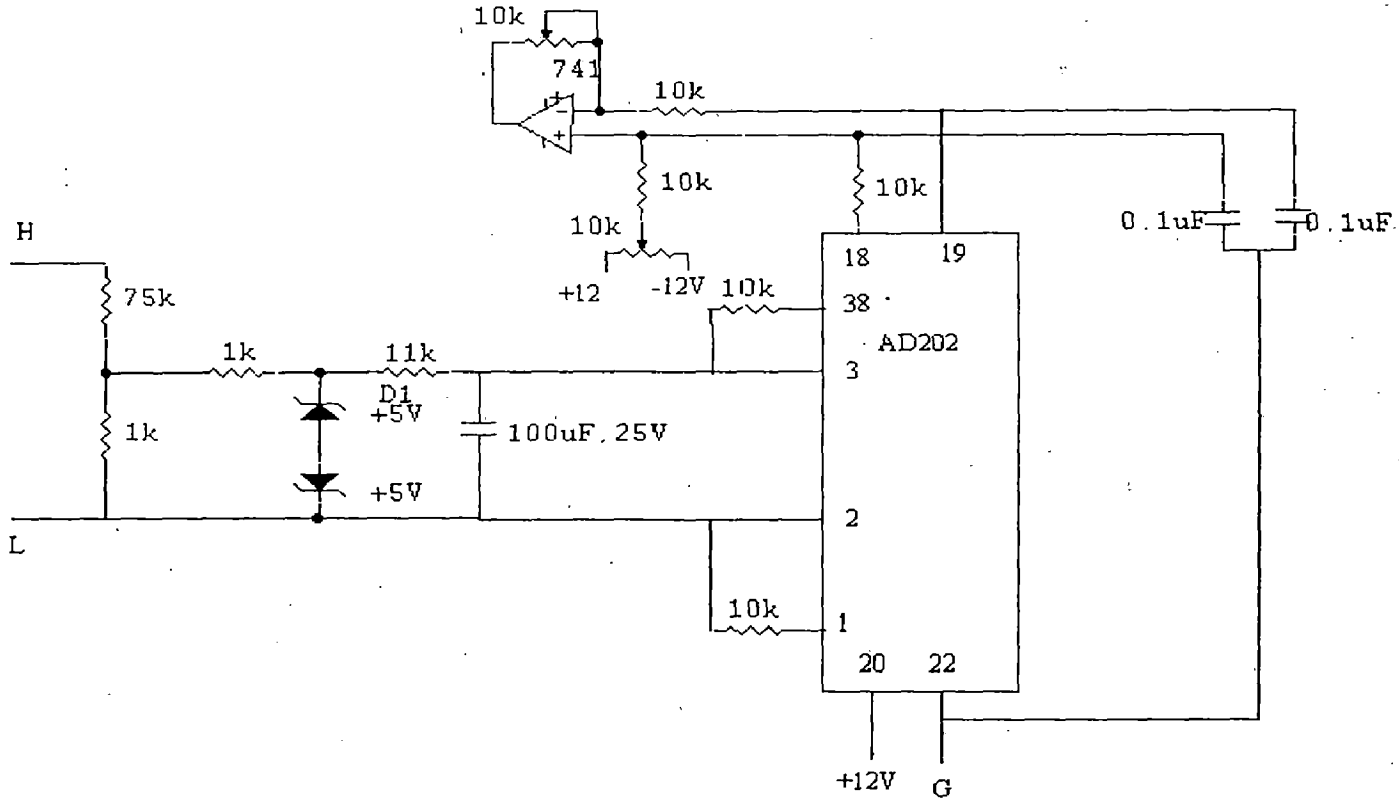


Fig 5.9 DC voltage Sensing Circuit

5.11 Total Voltage Controller

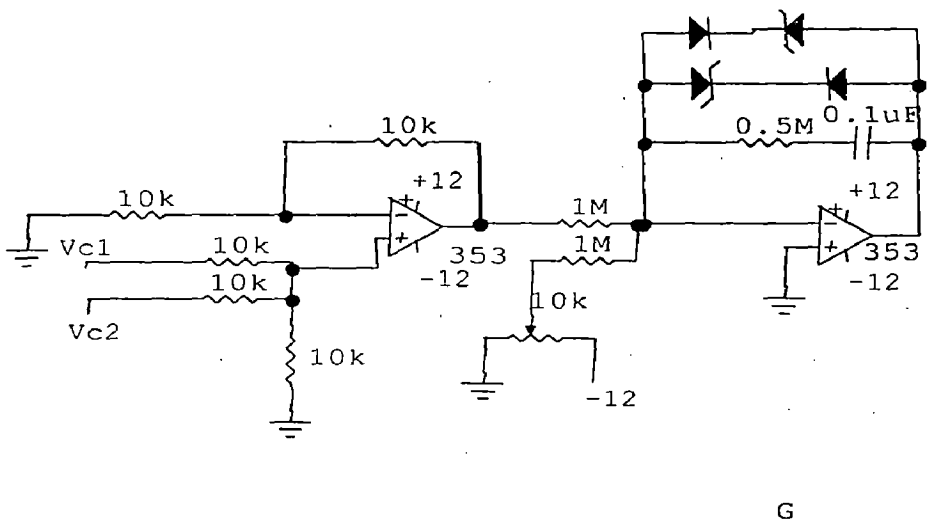


Fig 5.10 Total Voltage Controller

The Dc voltages across each capacitor are sensed by using AD 202 Isolation amplifier. These two voltages are added and are then subtracted by a reference voltage. The Reference voltage is the voltage, which we have to keep constant across the DC bus. A error detector, PI controller and limiter are combined in a single circuit as shown in figure. Diode and zener diode provide limitation on maximum negative and maximum positive voltages. The output of the controller gives us the amplitude of the reference current which is multiplied with unit signal with the multiplier chip and we get a Reference Current.

5.11 Differential Voltage Controller

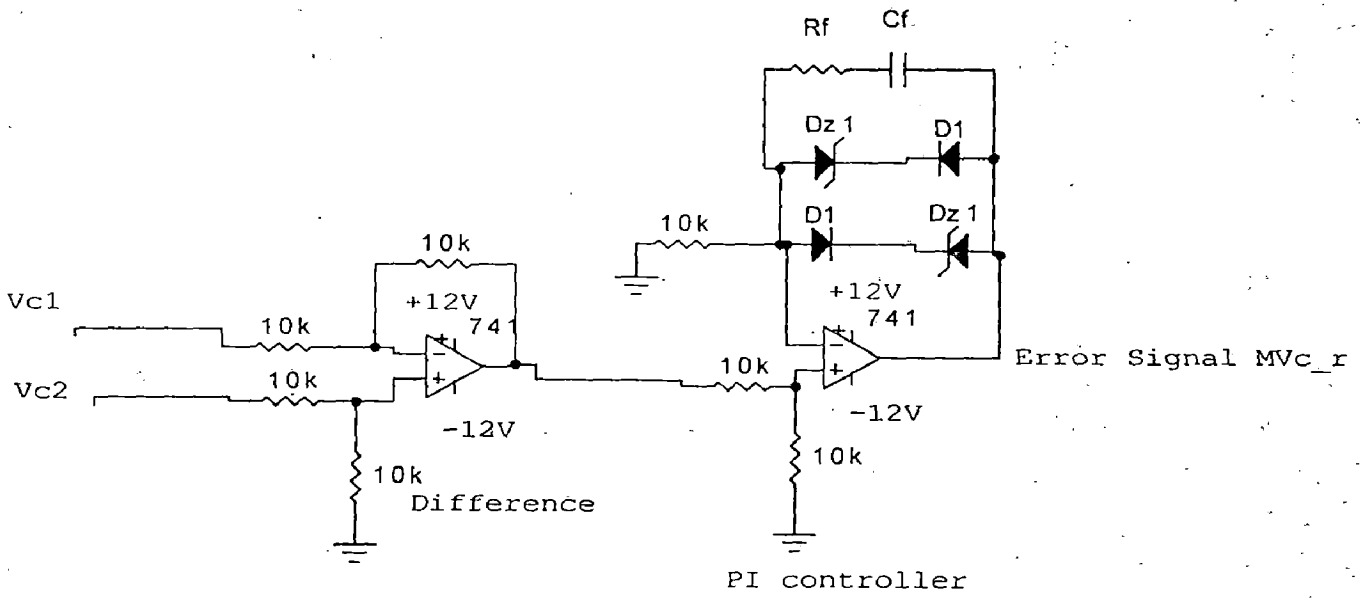


Fig 5.11 Differential Voltage Controller

This controller is used to generate the signal MVc_r (i.e difference between the two capacitors voltages). This signal helps in modification of the amplitude of two triangular carrier waves. The voltage across each capacitor is sensed using an AD 202 Isolation amplifier. The difference between the two capacitor voltages is obtained by using an difference circuit. The output of the difference circuit is then feed to the PI controller circuit. An error detector, PI controller and limiter are combined in a single circuit as shown in figure. Diode and zener diode provide limitation on maximum

negative and maximum positive voltages. The output is then used to modify the amplitude of triangular carrier waves.

5.12 Switching Pulses Generation Circuit:

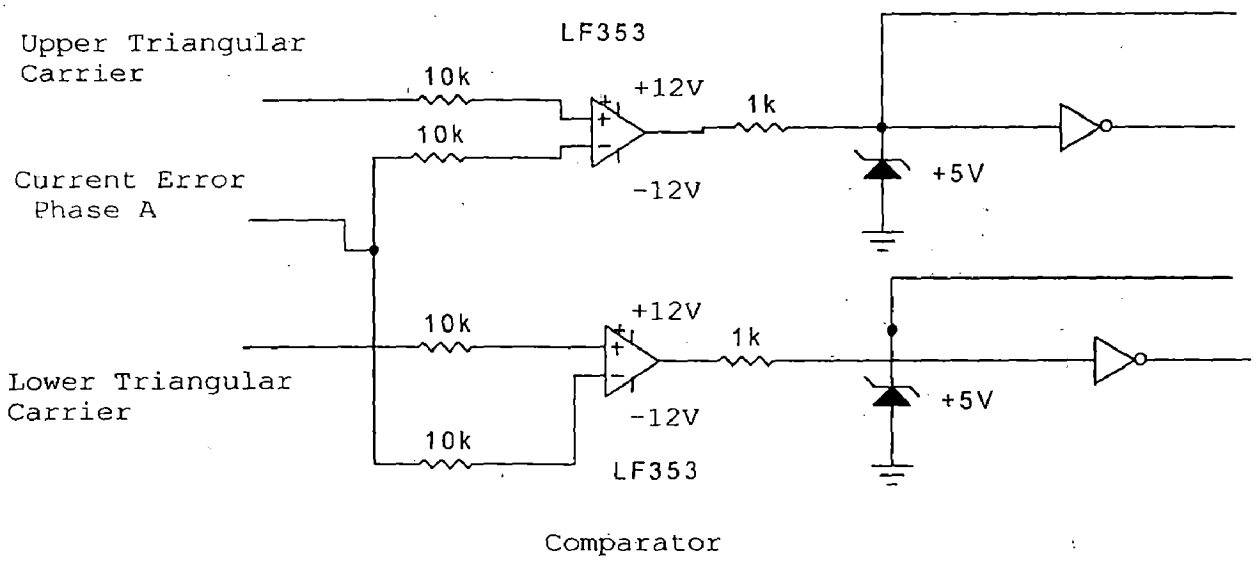


Fig 5.12 Pulse Generation For one leg of Three-level Converter

Circuit Diagram of Pulse generation for one leg of multilevel Converter is shown in fig 5.11. The current error generated is the difference between the reference current signal (which is in phase with the respective phase voltage) and the measured current. This current error is than compared with two triangular carrier waves to generate the required switching gate pulses for the converter. The circuit shown above is for only one leg of the three-level converter (i.e for the one phase). Since there are three phases, there will be two more similar circuits. Opamp LF 353 is used to operate as an comparator. Zener diode is used to limit the output voltage of the comparator equal to +5V. Not gate 7404 is used to invert the comparator output voltage. As explained in Chapter 2, the result of comparing current error and upper triangular carrier is used to control the switching S_{1a} and S_{3a} and the result of comparing current error and lower triangular carrier is used to control the switching S_{2a} and S_{4a}. The principle is

1) if current error > carr_s, then S_{1a} is on and S_{3a} is off.

2) if current error <= carr_s, then S_{1a} is off and S_{3a} is on.

3) if current error > carr_i, then S_{2a} is on and S_{4a} is off.

4) if current error <= carr_i, then S_{2a} is off and S_{4a} is on.

Conclusions

In this chapter the hardware development of multilevel converter and the control scheme which have been implemented is discussed. The working of power circuit, reference circuit , current sensing circuit, differential voltage controller and total voltage controller, pulse generation circuit has been discussed.

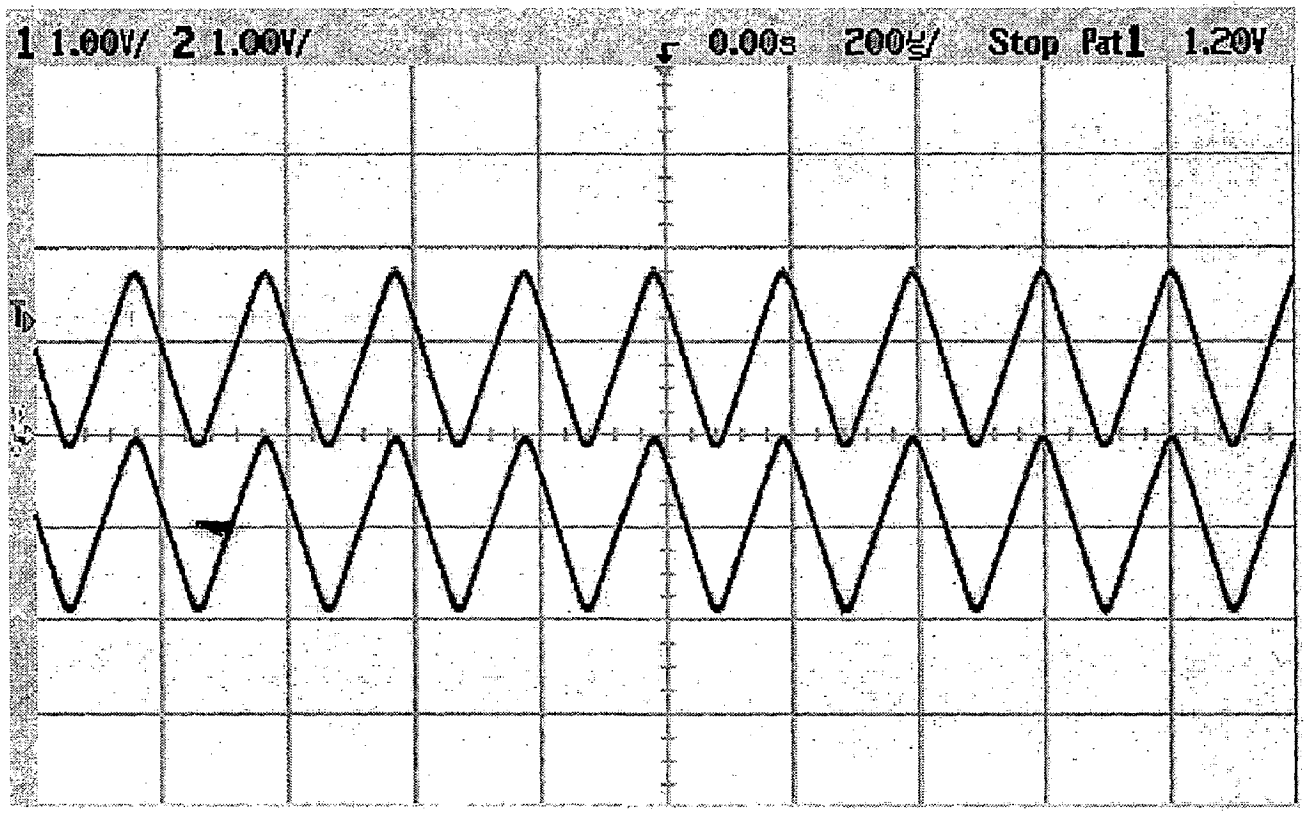
Chapter 6

EXPERIMENTAL RESULTS

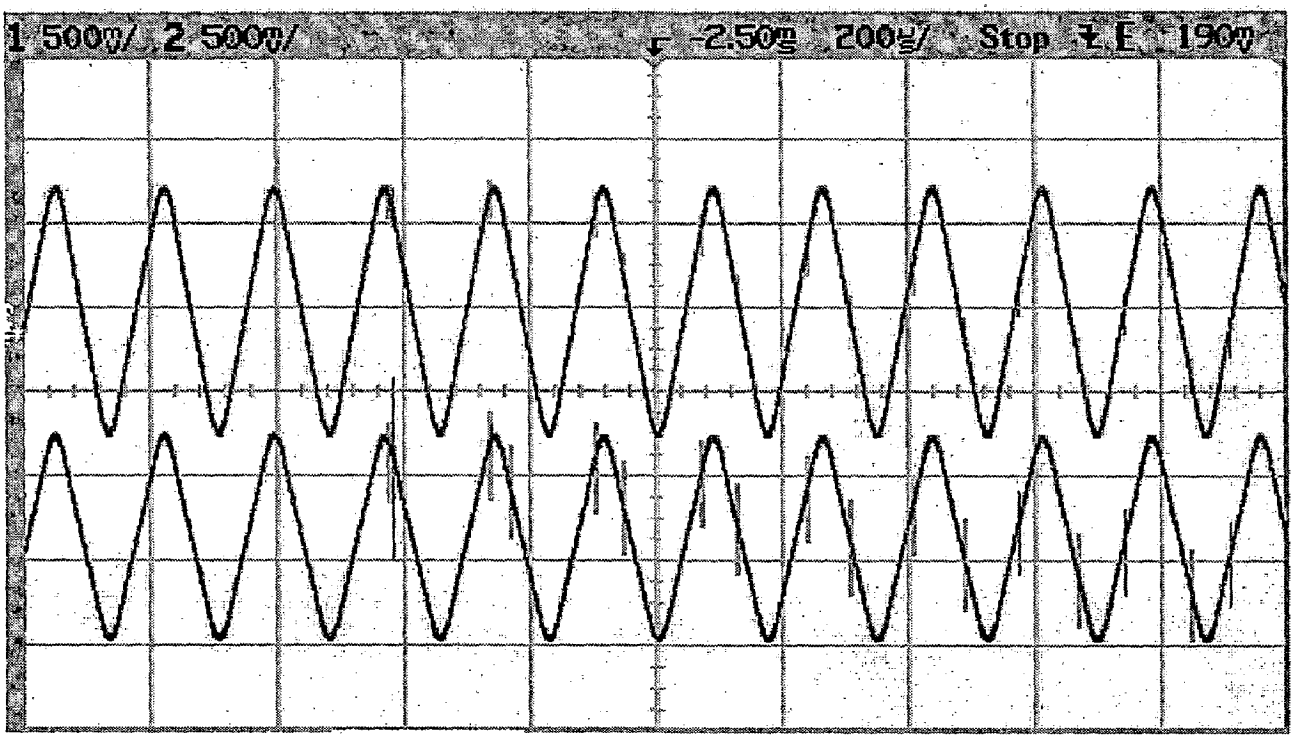
6.1 Introduction

Hardware requirements of the control scheme were developed and results of the control scheme operating the multilevel converter as a rectifier have been recorded. The carrier switching frequency was fixed at 5 kHz and the results of control scheme circuits like triangular carrier waveforms, reference sinusoidal signal were recorded. The input line currents and the output dc bus voltage were also recorded.

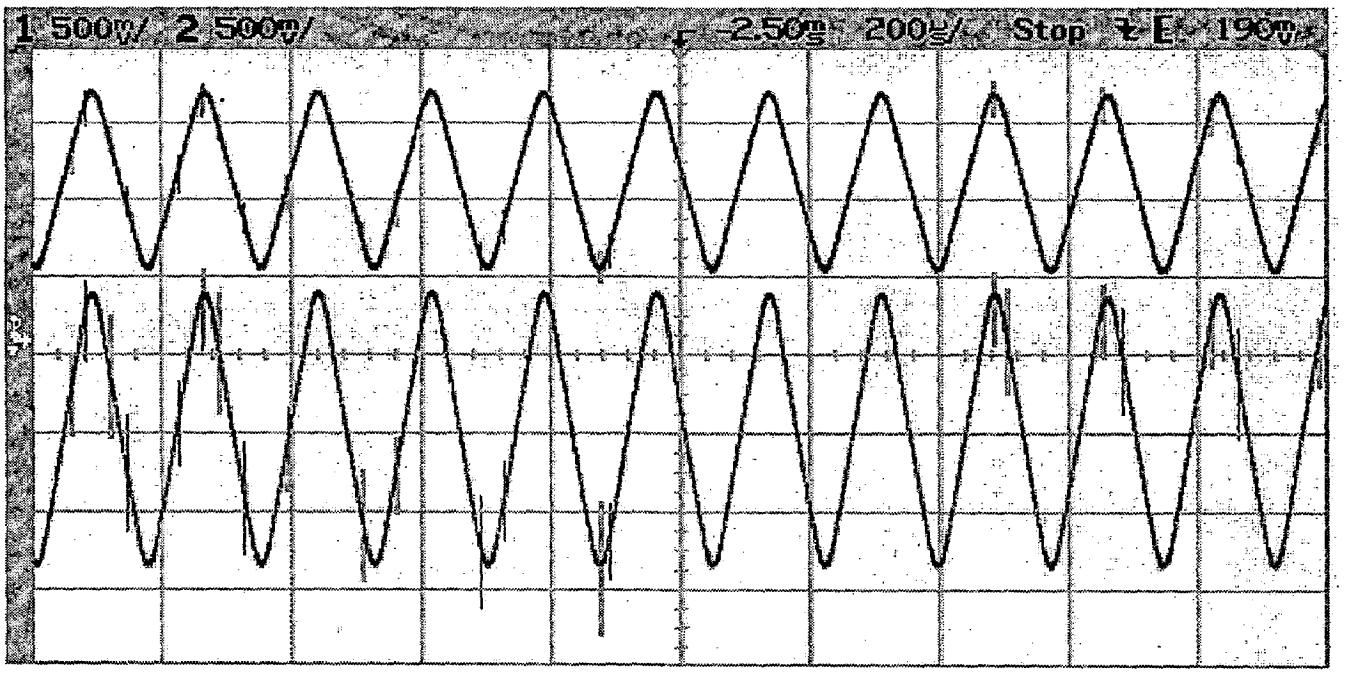
Triangular Carrier Generator



6.1 Triangular carrier waveforms when voltage across each capacitor is equal

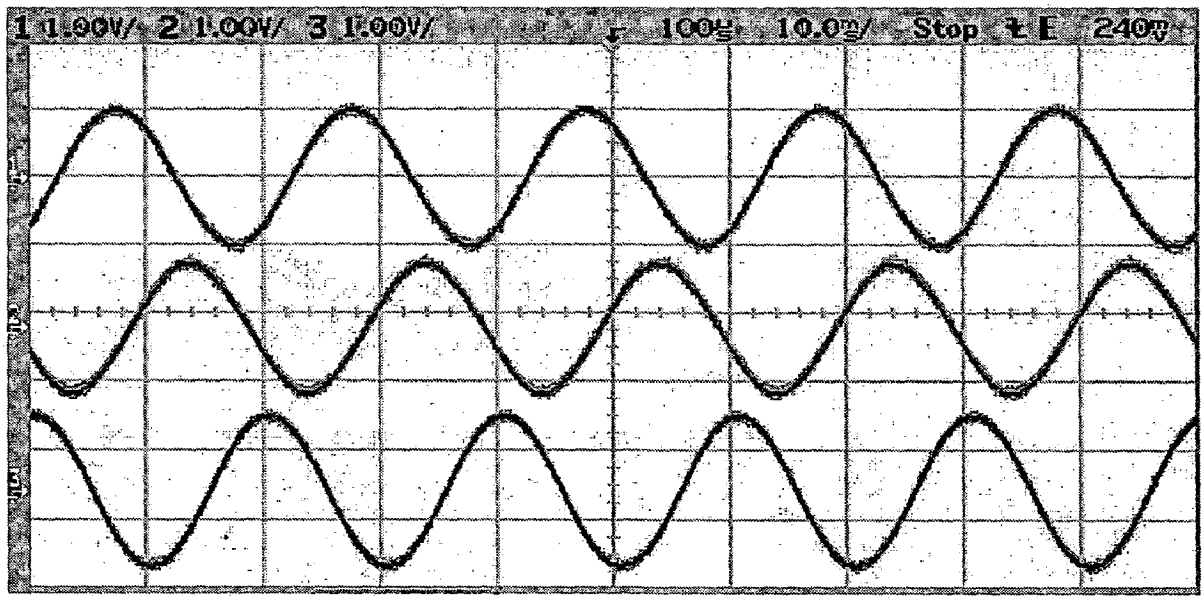


6.2 voltage across the upper capacitor is greater than lower capacitor



6.3 Lower Capacitor voltage is greater than upper capacitor voltage

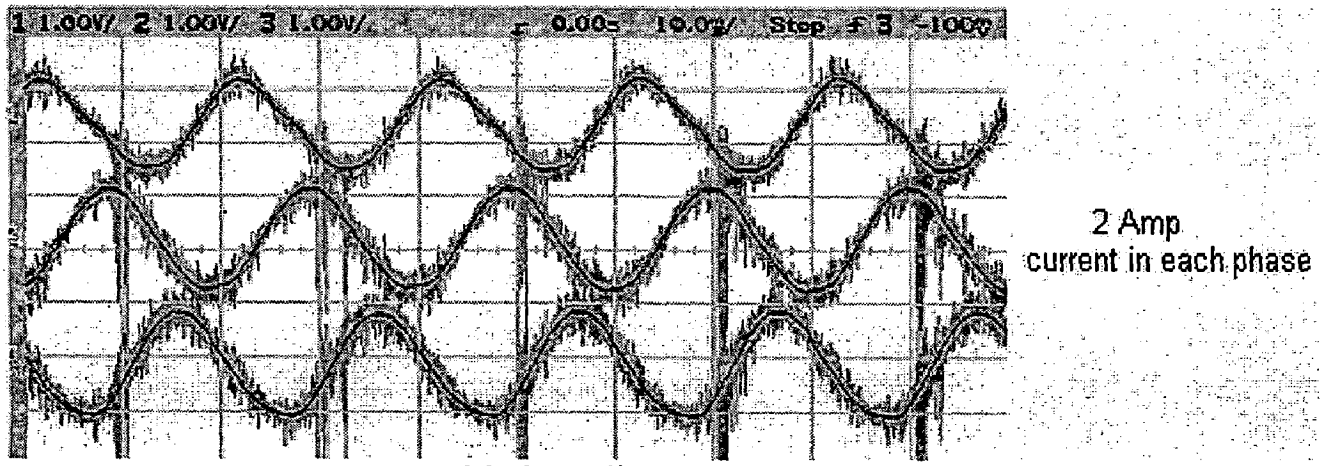
Reference Signals



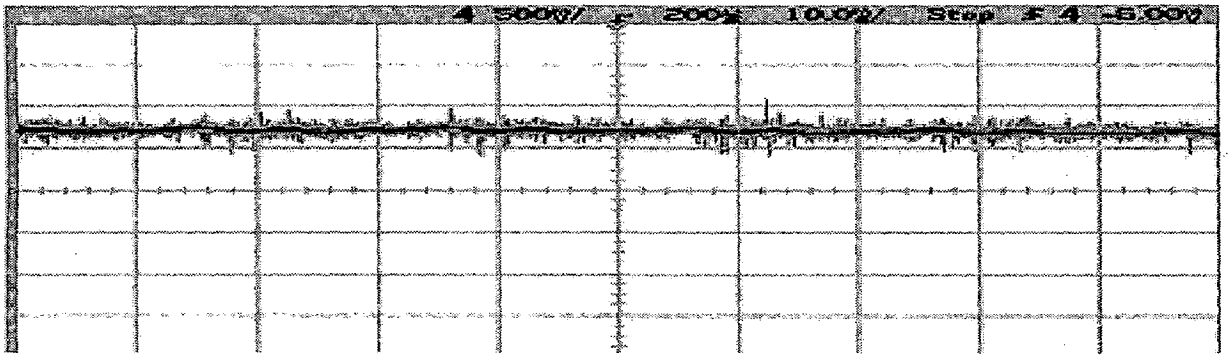
6.4 Reference signals

Three level Rectifier waveforms

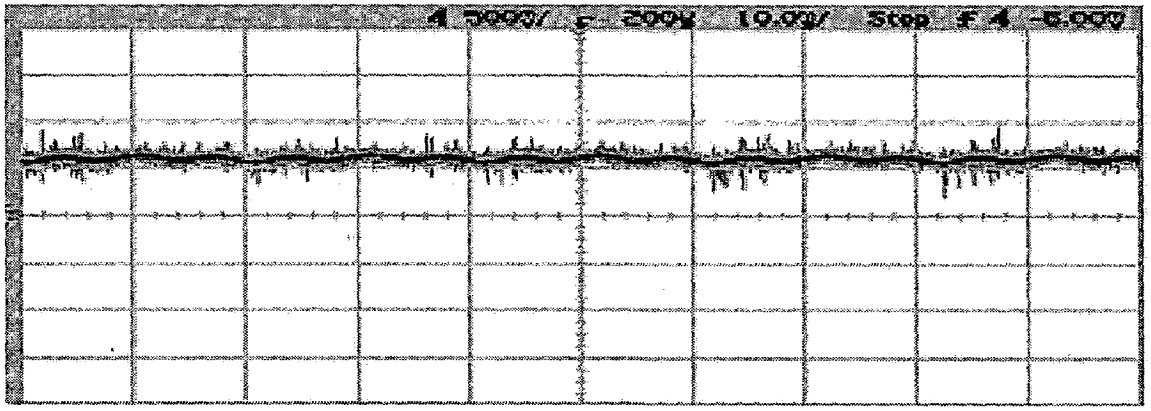
At Input Voltage V = 15V, Frequency of carrier waves =5kHz



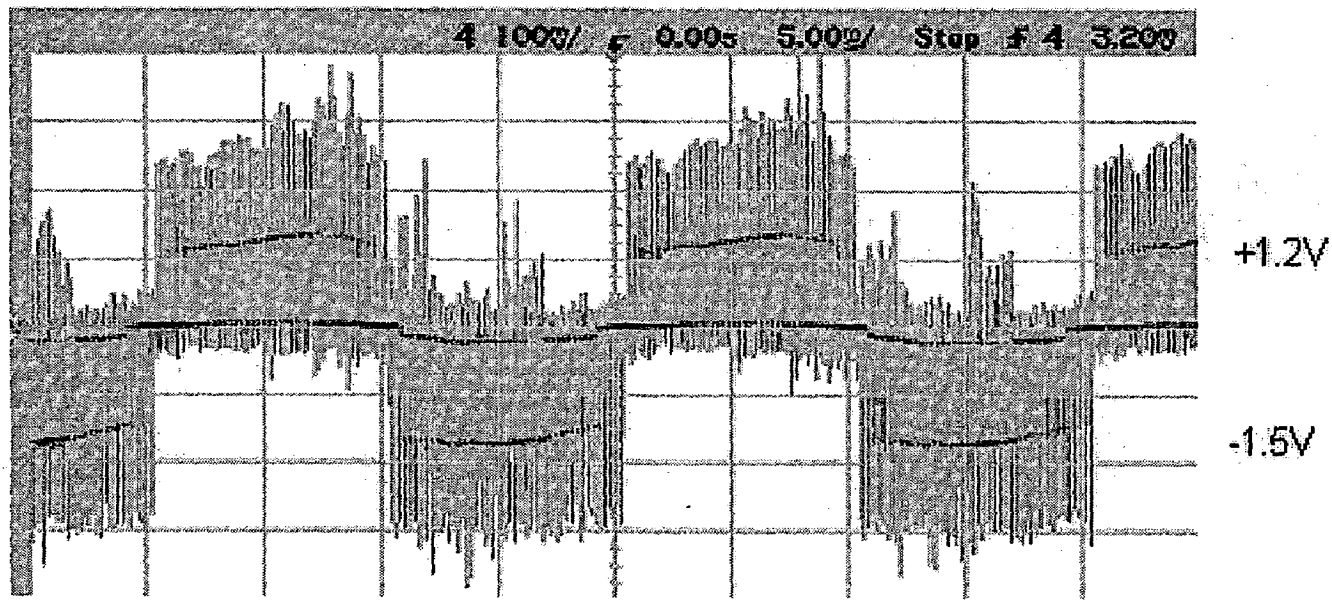
6.3. Input line currents



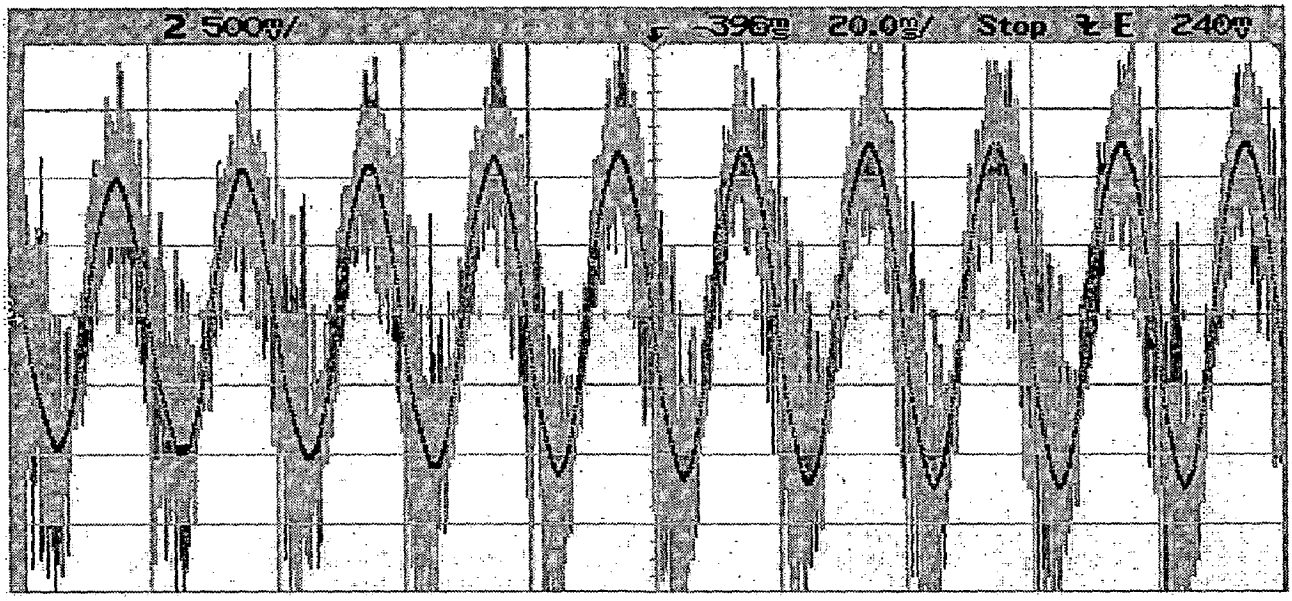
6.4 Upper Capacitor Voltage



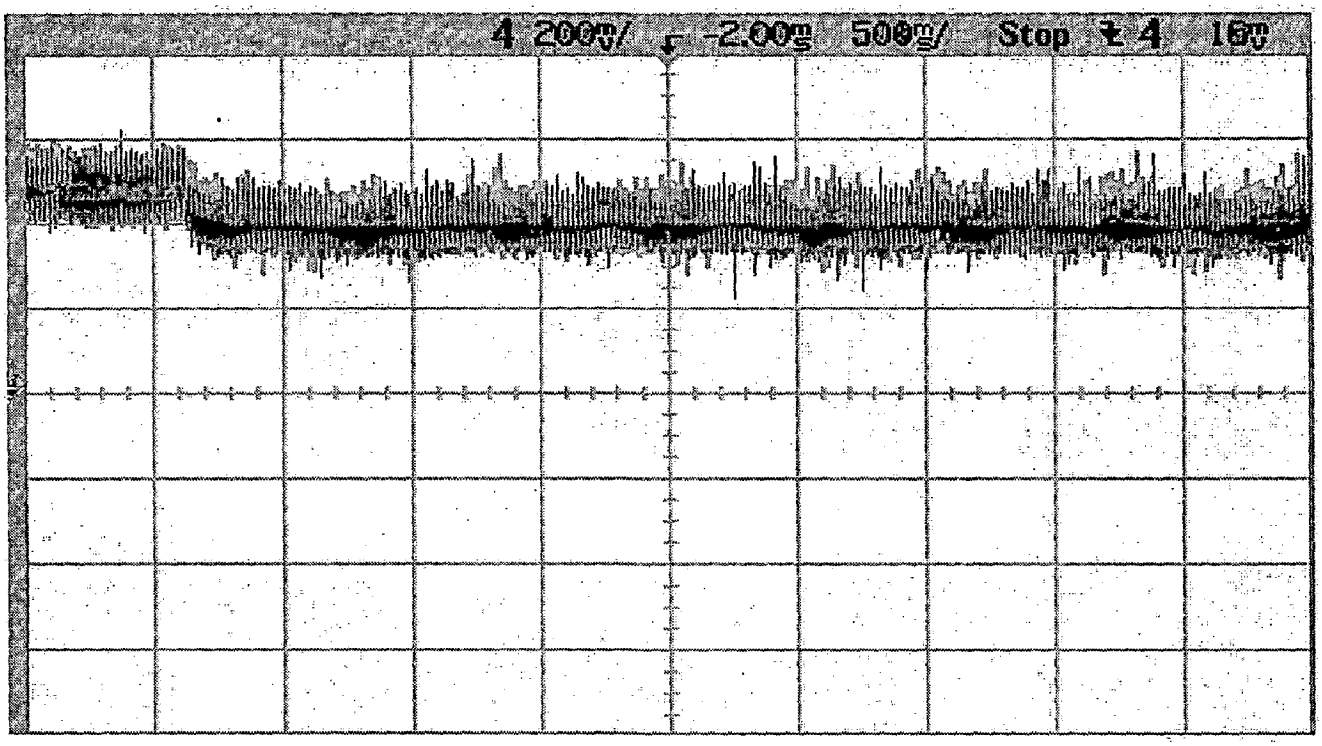
6.5 Lower Capacitor voltage



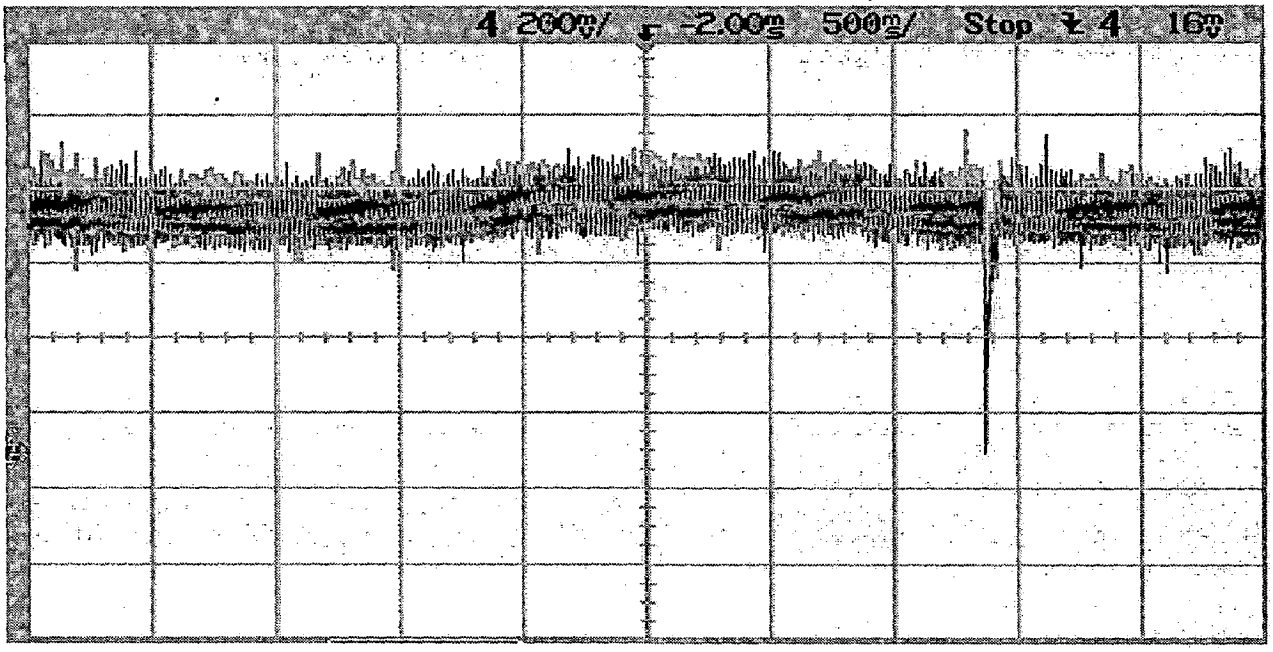
6.6 Voltage between Neutral point of capacitors and the input point of one leg Three-level converter.



6.7 Input current when the Reference Voltage amplitude is decreased



6.8Upper capacitor voltage when the reference voltage amplitude is decreased



6.9 Lower capacitor voltage when the reference voltage amplitude is decreased

Conclusion

The wave forms of control scheme, i.e Triangular carrier waveforms, Reference signals, were recorded. The input current waveforms of the multilevel converter were sinusoidal. Output dc bus voltage was recorded across each capacitor and it has been found that at input line to line voltage of 15 V the output voltage is 28 volts. Since we are operating the control scheme in open loop voltage across the capacitors is unbalance. One of the capacitor is reading 16V and another is reading 12V.

Chapter 7

CONCLUSIONS

7.1 Conclusions

1. Simulation of the control scheme was done by using MATLAB (6.1 Ver). It has been shown in simulation results that the control scheme operates the multilevel converter as a rectifier or as an active power filter or both at the same time. It has been observed that in both the case that, as the switching frequency is increased the input line currents become more sinusoidal that means the THD is improved. The control scheme maintains the voltage across each capacitor constant, balanced and equal, thus act as an remedy for the DC capacitor voltage unbalance. Also the total dc bus voltage is maintained constant and equal to the respective phase value.
2. Hardware implementation of the control scheme was developed and it was operated in open loop as a rectifier. It has been observed that the input current are sinusoidal. The voltage across each capacitor was measured.

Scope for future work

There is lot to done in this direction for future improvement

1. As it has been seen from the simulation results the THD improves as the switching frequency is increased. But as the switching frequency is increased the capacitor voltage fluctuates at a very fast rate. So some better balancing circuit can be implemented in future and better control scheme to reduce the THD of the Input current.
2. In the hardware circuit the work has been completed only till open loop operation of the multilevel converter. Closed loop operation can be done in future on the hardware circuit I have implemented.

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