PERFORMANCE INVESTIGATION OF A HIGH INPUT POWER FACTOR CONVERTER APPLYING SPACE VECTOR MODULATION

A DISSERTATION

Submitted in partial fulfilment of the requirements for the award of the degree of

MASTER OF TECHNOLOGY

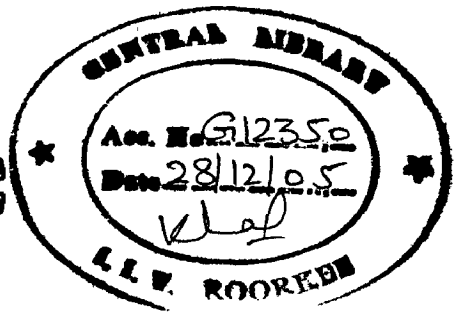
in

ELECTRICAL ENGINEERING

(With Specialization in Power Apparatus and Electric Drives)

By

D. AMARNATH REDDY



DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY ROORKEE
ROORKEE-247 667 (INDIA)

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CANDIDATE'S DECLARATION

I hereby declare that the work that is being presented in this dissertation report entitled **"PERFORMANCE INVESTIGATIONS OF A HIGH INPUT POWER FACTOR CONVERTER APPLYING SPACE VECTOR MODULATION"** submitted in partial fulfillment of the requirements for the award of the degree of **MASTER OF TECHNOLOGY** in **ELECTRICAL ENGINEERING** with specialization in **POWER APPARATUS AND ELECTRIC DRIVE**, submitted in the Department of Electrical Engineering, Indian Institute of Technology, Roorkee, is an authentic record of my own work carried out, under the guidance of Dr. Pramod Agrawal, Professor, Department of Electrical Engineering.

The matter embodied in this dissertation report has not been submitted by me for the award of any other degree or diploma.

Date: 27/6/05

Place: Roorkee

Amarnath

(D.AMARNATH REDDY)

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

Pgpl

(DR. PRAMOD AGRAWAL)

Professor,
Department of Electrical Engineering,
Indian Institute of Technology,
ROORKEE – 247 667,
INDIA.

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Place: Roorkee

(D.AMARNATH REDDY)

ABSTRACT

Due to the increase of non-linear loads in utility systems, the quality of power has attracted much attention in resent years. The low power factor and large harmonics line currents generated by rectifiers are well known problems that can lead to voltage distortion, and increase losses in the transmission and distribution lines. To overcome these problems active current wave shaping techniques have been developed to provide nearly sinusoidal source current. A SVM-based HCC for the three-phase PWM rectifier is proposed. This technique utilizes advantages of the HCC and SVM technique. This configuration reduces significantly the number of switching and at the same time gives the same state space vectors as those obtained from the SVM technique. The proposed current controller confines state space vectors from a region detector and apply a proper space vector selected according to the HCC for better current shape. A set of state space vectors including the zero vectors is determined from the region detector made up of three comparators. Hard ware implementation circuits and software development have been discussed. Simulation and Experimental results have been discussed.

Contents

CHAPTER-1

INTRODUCTION

1.1 General

Traditionally, three phase- Controlled or diode rectifiers perform three-phase AC-to-DC conversions. Since these rectifiers draw non-sinusoidal currents or reactive power from the source, the power quality of the distribution network is greatly deteriorated, resulting in low efficiency of utilities. Recently, more and more stringent limits on the level of harmonics promote the growth of power factor correction techniques in front-end power converters. Among three-phase ac-to-dc pwm rectifiers, boost-type topologies are frequently used because of continuous input currents and high output voltages. Most popular topology is: a six switch full-bridge boost rectifier. This converter uses six switches to achieve sinusoidal input current control and to share the output power. The inductors and capacitor filter the high-frequency switching harmonics, and have little influence on the low frequency ac components of the waveforms. So its features include continuous input current, excellent power factor, and low switch current rating [1].

The dissertation deals with development of high input p.f converter. The SVM based HCC will be used to control the converter. Current control plays most important role in current controlled pwm converter. In a conventional current control scheme, due to easy implementation, fast dynamic response, maximum current limit, and insensitivity to load parameter variations, the 3 independent hysteresis current controls (HCC) are used. But due to lack of coordination among the individual HCC's of these phases, high switching frequency at lower modulation may happen. In addition the current error is not strictly limited. [3]

On the other hand, the space vector modulation (SVM) scheme has two excellent features in that its maximum out put voltage is larger and the no of switching is less at the same carrier frequency as compared to sinusoidal pwm method. In this a set of space vectors including the zero voltage vectors for changing the current direction can be utilized to reduce the no of switching greatly.

The SVM technique confines state space vectors to be applied according to the region where the output voltage vector is located. To minimize the current error between the current command and line current, the SVM technique requires a considerable calculation burden. The space vector approach can provide fast dynamic control, but is quite complicated to implement and requires significant computational resources. High-speed microprocessors or digital signal processors are required. [2]

On the other hand, the HCC can be utilized to make the line current vector track the command vector with almost negligible response time and insensitivity to line voltage and parameter variation. However, the HCC generates other vectors besides the state space vectors required according to the region in the SVM technique and increases the number of switching. If the zero vectors are applied to reduce the magnitude of the line current vector, the line current is decreased with slow slope and the number of switching is decreased. Thus the utilization of non-zero vectors instead of the zero vectors for decreasing the line current increases the number of switching. Therefore, a SVM-based HCC utilizing all features of the HCC and SVM technique needs to be developed.

In the space vector based hysteresis current controller configuration the no of switching reduces, significantly and at the same time gives the same state space vectors as those obtained from the SVM technique. The current controller confine state space vectors from the region detector and applies a proper space vector selected according to the HCC for better current shape. In the dissertation work, SVM based HCC was designed and developed.

1.2 Statement of problem

- Development of three-phase AC-to-DC converter
- Design and development of SVM based HCC control scheme
- Simulation of the High input power factor converter applying space vector modulation using MATLAB

1.3 Organization of this dissertation

- Chapter 2 defines driving concepts behind requirement of power factor correction.
- Chapter 3 presents the basic operation and different topologies of a high power factor rectifier.
- Chapter 4 discusses about the existing and proposed control techniques to achieve unity power factor input current waveform for a converter.
- Chapter 5 presents the simulation results for the proposed high power factor converter.
- Chapter 6 discusses about the development of hardware setup for the proposed high power factor converter.
- Chapter 7 presents the experimental results form the hardware setup.

CHAPTER-2

BACKGROUND OF POWERFACTOR CORRECTION

2.1 Nonlinear loads and their effect on the electricity distribution Network

The equipment connected to an electricity distribution network usually needs some kind of power conditioning, typically rectification, which produces a non-sinusoidal line current due to the nonlinear input characteristic. The most significant examples of nonlinear loads are reviewed next. Line-frequency diode rectifiers convert AC input voltage into DC output voltage in a un controlled manner. Single-phase diode rectifiers are needed in relatively low power equipment that need some kind of power conditioning, such as electronic equipment (e.g. TVs, office equipment, battery chargers, electronic ballasts) and household appliances. For higher power, three phase diode rectifiers are used, e.g. in variable-speed drives and industrial equipment. In both single- and three-phase rectifiers, a large filtering capacitor is connected across the rectifier output to obtain DC output voltage with low ripple. As a consequence, the line current is non sinusoidal. Line-frequency phase-controlled rectifiers are used for controlling the transfer of energy between the AC input and the adjustable DC output. They are applied, for example, in some DC and AC motor drives with regenerative capabilities, or the temperature in resistive heaters. In every case, the line current is non sinusoidal. Gas discharge lamps with line-frequency ballast are nonlinear loads, as well. Hence, their line current is non sinusoidal.

Line current harmonics have a number of undesirable effects on both the distribution network and consumers. These effects include:

- Losses and overheating in transformers shunt capacitors, power cables, AC machines and switchgear, leading to premature aging and failure.
- Reduced power factor, hence less active power available from a wall outlet having a certain apparent power rating.

- Electrical resonances in the power system, leading to excessive peak voltages and RMS currents, and causing premature aging and failure of capacitors and insulation.
- Telephone interference, Errors in metering equipment, increased audio noise.
- Cogging or crawling in induction motors, mechanical oscillation in a turbine-generator combination or in a motor-load system.

2.2 Standards regulating line current harmonics

The previously mentioned negative effects of line current distortion have prompted a need for setting limits for the line current harmonics of equipment connected to the electricity distribution network

Standard IEC 1000-3-2 applies to equipment with a rated current up to and including 16Arms per phase, which is to be connected to 50Hz or 60Hz, 220-240Vrms single-phase, or 380-415Vrms three-phase mains. Items of electrical equipment are categorized into four classes (A, B, C and D), for which specific limits are set for the harmonic content of the line current.[7]

Harmonic order 'n'	Maximum permissible Harmonic current 'A'
Odd harmonics	
3	2.30
5	1.14
7	0.77
9	0.40
11	0.33
13	0.21
15. n. 39	0.15 * 15. n
Even harmonics	
2	1.08
4	0.43
6	0.30
8. n. 40	0.23 * 8. n

Table 2.1

Class A includes: balanced three-phase equipment; household appliances, excluding equipment identified as Class D, tools, excluding portable tools, dimmers for incandescent lamps; and audio equipment. Equipment not specified in one of the other three classes should be considered as Class A equipment. The limits for Class A are presented in Table 2.1.

Class B equipment includes: portable tools; and nonprofessional arc welding equipment. The limits for this class are those shown in Table 2.1 multiplied by a factor of 1.5.

Harmonic order 'n'	Maximum permissible harmonic current Expressed as a percentage of the input Current at the fundamental frequency %
2	2
3	30.PF *
5	10
7	7
9	5
11. n. 39	3
PF * is the circuit power factor	

Table 2.2

Class C includes lighting equipment. For an active input power greater than 25W, the harmonic currents should not exceed the limits resented in Table 2.2 the harmonic limits for Class D are presented in Table 2.3. They are defined in both power related and absolute terms. These include personal computers, personal computer monitors, and television receivers, equipment having active input power less than or equal to 600W.

Harmonic order 'n'	Maximum permissible Harmonic current per Watt 'mA/W'	Maximum permissible Harmonic current 'A'
3	3.4	2.30
5	1.9	1.14
7	1.0	0.77
9	0.5	0.44
11	0.35	0.33
13. n. 39	3.85. n	As in Class A

Table 2.3

The limits for the line current harmonics are given as a percentage of the maximum demand load current I_1 (fundamental frequency component) at the Point of Common Coupling – PCC at the utility. They decrease as the ratio I_{sc}/I_1 decreases, where I_{sc} is the maximum short-circuit current at the PCC.

2.3 Power Factor Correction (PFC) Basics

Reduction of line current harmonics is needed in order to comply with the standard. This is commonly referred to as the Power Factor Correction – PFC, which may be misleading. Therefore, some clarification is needed.

The power factor, *PF*, is defined as the ratio of the active power *P* to the apparent power *S*: $PF = \frac{P}{S}$ $PF = \frac{P}{S}$

For purely sinusoidal voltage and current, the classical definition is obtained:

$$PF = \cos\varphi \qquad 2.1$$

Where cos. is the displacement factor of the voltage and current. In a classical sense, PFC means compensation of the displacement factor.

We assume the line voltage to be sinusoidal, since in most cases the total harmonic voltage distortion is quite low, e.g. the total harmonic distortion of the line voltage shown in Fig. 2..1 is $THD_e=2$ . . However, the line current is non sinusoidal when the load is nonlinear. Therefore, the classical definition of the power factor does not apply. For sinusoidal voltage and non-sinusoidal current, P.F can be expressed as:

$$PF = \frac{V_{rms} I_{1rms} \cos\varphi}{V_{rms} I_{rms}} = \frac{I_{1rms}}{I_{rms}} \cos\varphi = K_p \cos\varphi \qquad 2..2$$

$$K_p = \frac{I_{1rms}}{I_{rms}}, K_p \in [0,1] \qquad 2.3$$

The factor K_P describes the harmonic content of the current with respect to the fundamental. In this case, the power factor depends on both harmonic content and displacement factor. It appears that there is no standard term, which can be used to denote the factor defined by (2.3). Some authors refer to it as the 'purity factor', while others as the 'distortion factor'. We believe that 'purity factor' describes its meaning more

accurately, as the factor is unity f or a pure sinusoidal current, and it decreases as the harmonic content increases. Moreover, defining it as 'distortion factor' is in contradiction with the definition given by the IEEE Standard Dictionary on Electrical and Electronics Terms, which considers it as a synonym for the total harmonic distortion factor, the latter being defined for the line current as:

$$THD_i = \frac{\sqrt{\sum_{n=2}^{\infty} I_{nrms}^2}}{I_{1rms}} \qquad 2.4$$

It is straightforward to show that the relation between K_P and THD_I is:

$$K_p = \frac{1}{\sqrt{1+THD_i^2}} \qquad 2.5$$

Standard IEC 1000-3-2 sets limits on the harmonic content of the current but does not specifically regulate the purity factor K_P or the total harmonic distortion of the line current THD_I. The values of K_P and THD_I for which compliance with IEC 1000-3-2 is achieved depend on the power level. For low power level, even a relatively distorted line current may comply with the standard. In addition to this, it can be seen from (2.5) that the distortion factor K_P of a waveform with a moderate THD_I is close to unity (e.g. K_P = 0.989 for THD_I =15%)[8].

Considering (2.2) as well, the following statements can be made:

• A high power factor can be achieved even with a substantial harmonic content. The power factor *PF* is not significantly degraded by harmonics, unless their amplitude is quite large (low K_P, very large THD_I).

• Low harmonic content does not guarantee high power factor (K_P close to unity, but low cos .).

The supply power factor is critical for an economical design, and efficient and reliable operation of power system. Some of the disadvantages of low power factor are

- Because of large current, the losses in the generators and transmission lines increase causing over heating of the system components.
- It causes poor voltage regulation at the load.

- As the load voltage decreases due to poor voltage regulation the power transfer capacity is adversely affected
- The investment in system facilities per KW of load supplied increases with decrease in supply power factor Improving the power factor brings three benefits:
- Power distribution costs for the electric company are reduced, making the power company much happier. A side benefit is to reduce the tendency of the current peaks to "flatten" the tops of the input voltage sinusoidal waveform.
- More power can be drawn from a line of a given current rating, allowing more powerful equipment to be connected without having to re-wire a building, saving time and money.
- Various governmental and quasi-governmental agencies are passing laws requiring improved power factors on certain types of equipment, especially those which draw a lot of power. These laws make it illegal to sell certain types of equipment without testing and certification of a minimum power factor. To continue to sell medium-to high power supplies in the future, power supply manufacturers will have to deal with power factor correction.[6]

Although the first reason is nice and the second reason saves money, it is the third reason that has given all the impetus to power factor correction development.

Most of the research on PFC for nonlinear loads is actually related to the reduction of the harmonic content of the line current. Methods for limitation and elimination of disturbances and harmonic pollution in the power system have been widely investigated. This problem rapidly intensifies with the increasing amount of electronic equipment (computers, radio set, printers, TV sets etc.). This equipment, a nonlinear load, is a source of current harmonics, which produce increase of reactive power and power losses in transmission lines. The harmonics also cause electromagnetic interference and, sometimes, dangerous resonances. They have negative influence on the control and automatic equipment, protection systems, and other electrical loads, resulting in reduced reliability and availability. Moreover, nonlinear loads and non-sinusoidal currents produce non sinusoidal voltage drops across the network impedances, so that non-

sinusoidal voltages appear at several points of the mains. It brings out overheating of line, transformers and generators due to the iron losses.

Many of harmonic reduction method exist. These techniques based on passive components, mixing single and three-phase diode rectifiers, and power electronics techniques as: multi pulse rectifiers, active filters and PWM rectifiers (Fig. 2.1). They can be generally divided as:

A) Harmonic reduction of already installed non-linear load.

B) Harmonic reduction through linear power electronics load installation.

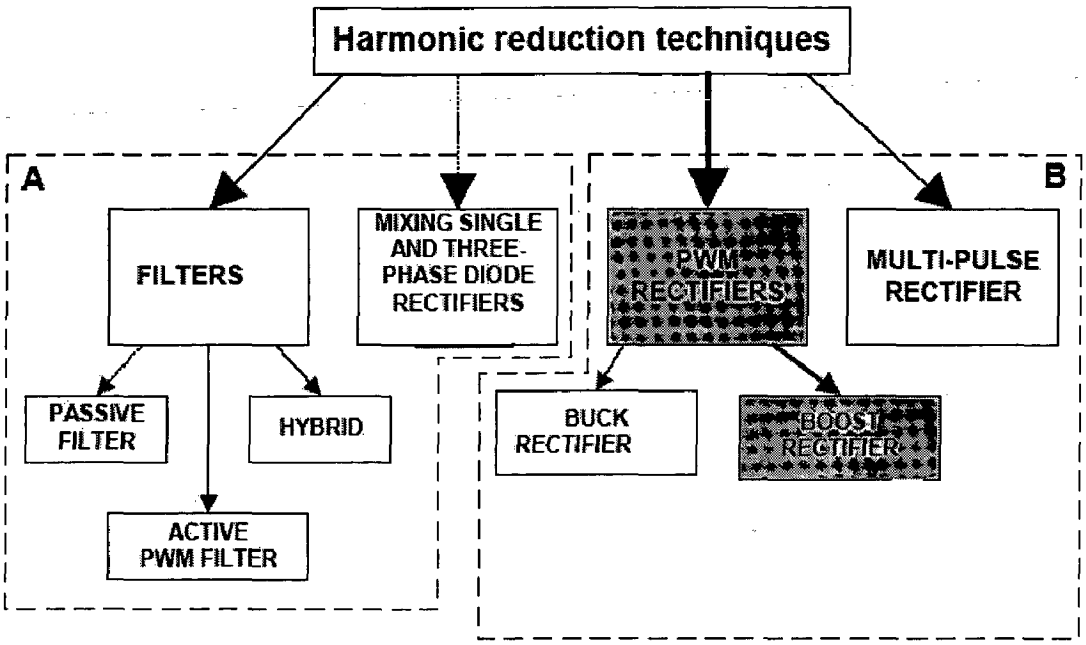


Fig. 2.1 Harmonic reduction techniques

The traditional method of current harmonic reduction involves passive filters LC, parallel-connected to the grid. Filters are usually constructed as series-connected legs of capacitors and chokes. The number of legs depends on number of filtered harmonics (5^{th}, 7^{th}, 11^{th}, and 13th). The advantages of passive filters are simplicity and low cost[9].

The disadvantages are:

- Each installation is designed for a particular application (size and placement of the filters elements, risk of resonance problems),
- High fundamental current resulting in extra power losses,
- Filters are heavy and bulky.

In case of diode rectifier, the simpler way to harmonic reduction of current is additional series coils used in the input or output of rectifier (typical 1-5%). The other technique, based on mixing single and three-phase non-linear loads, gives a reduced THD because the 5th and 7th harmonic current of a single-phase diode rectifier often are in counter-phase with the 5th and 7th harmonic current of a three-phase diode rectifier [10].

The other already power electronics techniques is use of multi pulse rectifiers. Although easy to implement, possess several disadvantages such as: bulky and heavy transformer, increased voltage drop, and increased harmonic currents at non-symmetrical load or line voltages.

An alternative to the passive filter is use of the active PWM filter (*AF*), which displays better dynamics and controls the harmonic and fundamental currents. Active filters are mainly divided into two different types: the active shunt filter (current filtering) and the active series filter (voltage filtering).

The three-phase two-level shunt *AF* consists of six active switches and its topology is identical to the PWM inverter. *AF* represents a controlled current source i_F which added to the load current I_{Load} yields sinusoidal line current I_L (Fig. 2.2).

AF provides:

- Compensation of fundamental reactive components of load current,
- Load symetrization (from grid point of view),
- Harmonic compensation much better than in passive filters.

In spite of the excellent performance, *AF's* possess certain disadvantages as complex control, switching losses and *EMC* problems (switching noise is present in the line current and even in the line voltage). Therefore, for reduction of these effects, inclusion of a small low-pass passive filter between the line and the *AF* is necessary.

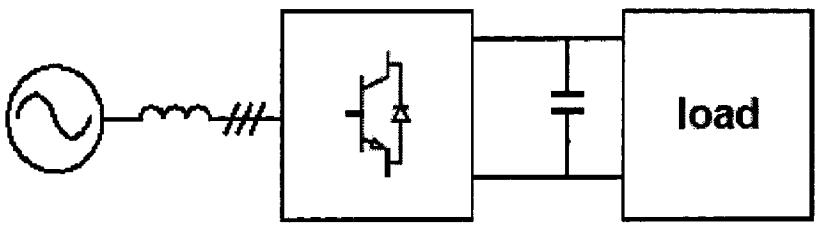


Fig.2.3 PWM rectifier

The other interesting reduction technique of current harmonic is a *PWM* (active) rectifier (Fig. 2.3). Two types of *PWM* converters, with a voltage source output (Fig. 2.4a) and a current source output (Fig. 2.4b) can be used. First of them called a *boost* rectifier (increases the voltage) works with fixed DC voltage polarity, and the second, called a *buck* rectifier (reduces the voltage) operates with fixed DC current flow.

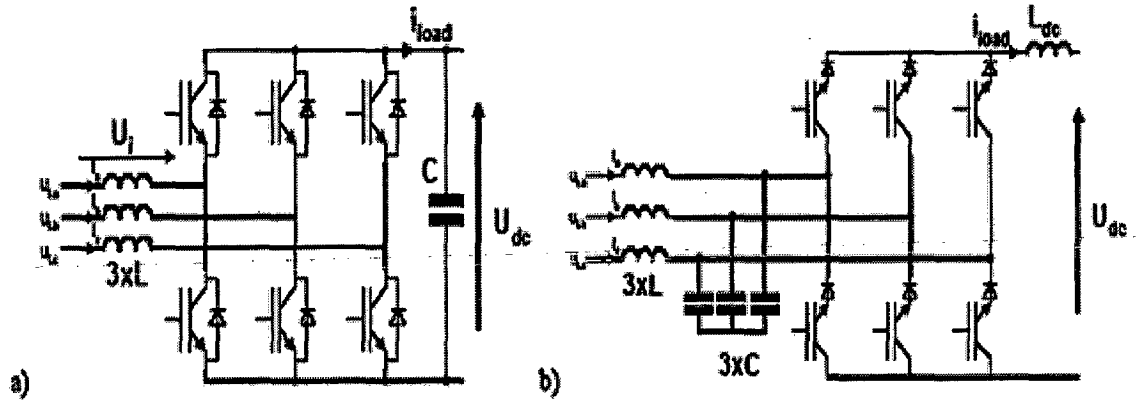


Fig. 2.4 Two basic topologies of PWM rectifier: a) *boost* with voltage output b) *buck* with current output

Among the main features of PWM rectifiers are:

- Bi-directional power flow,
- Nearly sinusoidal input current,
- Regulation of input power factor to unity,
- Low harmonic distortion of line current (*THD* below 5%),
- Adjustment and stabilization of DC-link voltage (or current),
- Reduced capacitor (or inductor) size due to the continues current.

Furthermore, it can be properly operated under line voltage distortion and notching, and line voltage frequency variations. Similar to the *PWM* active filter, the PWM rectifier has a complex control structure; the efficiency is lower than the diode rectifier due to extra switching losses. A properly designed low-pass passive filter is needed in front of the *PWM* rectifier due to *EMI* concerns.

The last technique is most promising thanks to advances in power semiconductor devices (enhanced speed and performance, and high ratings) and digital signal processors, which allow fast operation and cost reduction. It offers possibilities for implementation of sophisticated control algorithm.

CHAPTER-3

HIGH POWER FACTOR RECTIFIERS

3.1 Basic operation of High power factor rectifiers

The high power factor rectifiers can be categorized as single phase and three phases or based on the fact whether the inductor current is continuous or discontinuous.

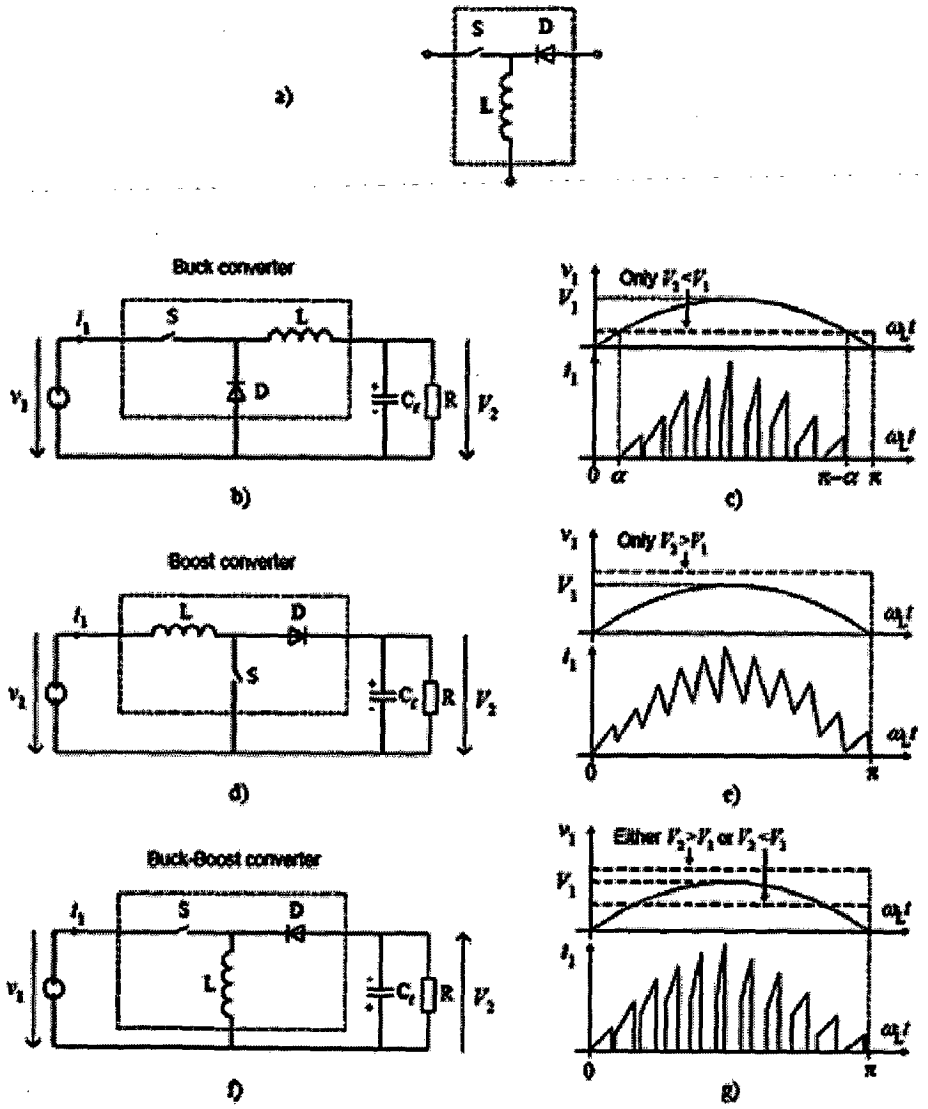


Fig. 3.1 Second-order switching converters and their application for high-frequency active PFC, assuming operation in CICM: a) First-order switching cell, from which second-order switching converter are generated; b) Buck converter, with c) waveforms; d) Boost converter, with e) waveforms; f) Buck-Boost converter, with g) waveforms.

The first-order switching cell is shown in Fig. 3.1 a). The active switch S is controlled by an external control input. In a practical realization, this switch would be implemented, for example, by a MOSFET or an IGBT. The state of the second switch, which is diode D, is indirectly controlled by the state of the active switch and other circuit conditions. The switching cell also contains a storage element, which is the inductor L [7]. In a PFC application, the input voltage is the rectified line voltage

$$V_1(t) = V_1.\sin.\ _L t. \quad . \qquad 3.1$$

The output voltageV_2 is assumed to be constant. The first characteristic, which is determined by the conversion ratio of the converter, is the relation between the obtainable output voltage V_2 and the amplitude V_1 of the sinusoidal input voltage.

The second characteristic refers to the shape of the filtered (line-frequency) input current. If the converter is able to operate throughout the entire line-cycle, a sinusoidal line current can be obtained. Otherwise the line current is distorted, being zero in a region around the zero-crossings of the line voltage where the converter camot operate.

The third characteristic is related to the high-frequency content of the input current. We consider that the input current is continuous if it is not interrupted by a switching action. This means that the inductor is placed in series at the input and only the inductor current ripple determines the high-frequency content of the input current. For CICM operation, the inductor current ripple can be relatively low, a situation in which the input current has a reduced high-frequency content. Conversely, the input current is discontinuous if it is periodically interrupted by the switching action of a switch placed in series at the input. In such a case, the high-frequency content of the input current is large, even in CICM operation. The terms continuous/discontinuous input current should not be confused with CICM/DICM, which refer to the inductor current

We now briefly characterize second-order converters in the light of these topology-specific characteristics. The converters are shown in Fig. 3.1 together with waveforms relevant for a PFC application, assuming operation in CICM. We need to clarify here that the given waveforms are only for supporting the explanation of the topology-specific characteristics. In reality, the switching frequency is much higher than the line-frequency and the input current waveform is dependent also on the type of control that is used

The Buck converter, shown in Fig. 3.1b), has step-down conversion ratio. Therefore, it is possible to obtain an output voltage *V2* lower than the amplitude *V1* of the input voltage. However, the converter can operate only when the instantaneous input voltage V_1 is higher than the output voltageV_2, i.e. only during the interval

$$\omega_1 t \varepsilon (\alpha, \pi - \alpha), \text{ where } \propto = \sin^{-1} \frac{V_2}{V_1} \qquad 3.2$$

Hence, the line current of a power factor corrector based on a Buck converter has crossover distortions, as illustrated in Fig. 3.1c). Moreover, the input current of the converter is discontinuous. Consequently, even in CICM, the input current has a significant high-frequency component that has to be filtered out.

The Boost converter is shown in Fig. 3.1d). It has a step-up conversion ratio; hence the output voltage V_2 is always higher than the amplitudeV_1 of the input voltage. Operation is possible throughout the line-cycle so the input current does not have crossover distortions. As illustrated in Fig. 3.1e), the input current is continuous, because the inductor is placed in series at the input. Hence, an input current with reduced high-frequency content can be obtained when operating in CICM. For these reasons, the Boost converter operating in CICM is widely used for PFC

	Conversion characteristics	Crossover distortions	Input current
Buck	Step-down, $V_2<V_1$	Yes, because operation is Possible only for $\omega_1 t \varepsilon (\alpha, \pi - \alpha), \propto = \sin^{-1} \frac{V_2}{V_1}$	Discontinuous
Boost	Step-up, $V_2>V_1$	NO	Continuous
Buck-Boost	Step-down/up, $V_2 \gtrless V_1$	NO	Discontinuous

Table 3.1

The Buck-Boost converter, shown in Fig. 3.1f), can operate either as a step-down or a step up converter. This means that the output voltageV_2 can be higher or lower than the amplitude V_1 of the input voltage, which gives freedom in specifying the output voltage. Operation is possible throughout the line-cycle and a sinusoidal line current can

be obtained. However, the output voltage is inverted, which translates into higher voltage stress for the switch. Moreover, similar to the Buck converter, the input current is discontinuous with significant high-frequency content, as illustrated in Fig. 3.1g). The topology-specific characteristics are summarized in Table 3.1

One common principle that applies to all three topologies, regardless of operational mode or control method is: In steady state operation, the voltage across the inductor, averaged over each switching cycle, must equal zero. Otherwise, the average inductor current would change, violating the steady state premise. Each of the three basic circuit families has a unique set of relationships between input and output voltages, currents, and duty cycle. For example, the basic buck regulator functions only with output voltage, V_o, less than V_{in} and with the same polarity. The basic boost circuit requires V_o greater than V_{in} with the same polarity. The fly back topology functions with V_o either greater or less than V_{in}, but the polarity must be opposite.

3.1.1 Discontinuous mode operation:

In the discontinuous inductor current mode, or "discontinuous mode", buck, boost and fly back circuits behave in a similar way. The inductor current is zero (hence discontinuous) during the last part of each switching cycle. During the first part of the cycle, the inductor current increases from zero, storing energy taken from the input. During the second part, all of this stored energy is discharged into the load, pumping energy from input to output.

Three States:

There are three distinct operational states during each switching cycle:

1. During the switch 'S', "on" time, ton, inductor current I_L rises from zero to the peak value Ip. This peak current equates to energy stored in the inductor, $LI^2/2$, at the end of ton. During this time the inductor current is drawn from the input, and this energy stored in the inductor each cycle is power taken from the input source.
2. When the switch turns off, the inductor voltage reverses and its stored energy forces the same peak current to flow through the diode. During the diode conduction time, td, the inductor current drives the output and linearly decreases to zero. At the end of td, all the energy that was stored in the inductor has been delivered to the output.

3. When the current reaches zero, the inductor has no more energy. The current in all switching circuit elements is zero for the remainder of the switching period. During this idle time, t_i, the circuit waits for the next clock pulse to turn the transistor back on and begin the next cycle.

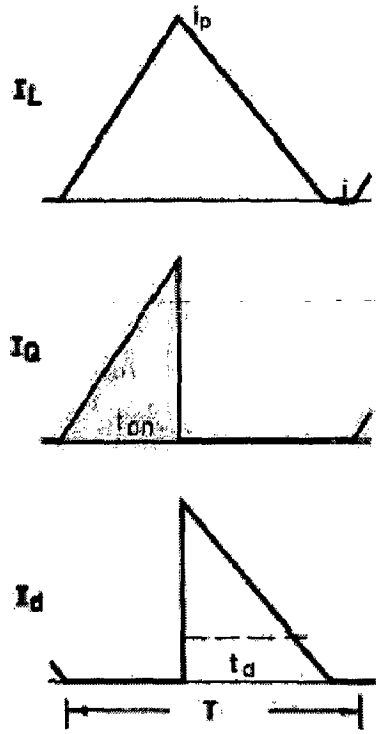


Fig 3.2 Inductor, Switch and Diode current wave forms under discontinuous current mode

	Buck	Boost	Fly back
I_{in}	I_Q	I_L	I_Q
I_o	I_L	I_d	I_d

Discontinuous Mode Boundary:

When load current is increases, the control circuit causes switch 'S', ton (duty cycle) to increase. Peak inductor current then becomes greater and diode conduction time td must also increase. Consequently, an increase in load current causes a steady state reduction in the idle time, ti. When load current increases to a certain level, ti becomes zero, and the discontinuous mode boundary is reached. If the load current is further increased, the inductor current will no longer discharge to zero every cycle, and continuous mode operation results. The circuit will become unstable because the loop gain compensation required for stable discontinuous mode operation is not adequate to prevent oscillation in the continuous mode. It is imperative for the control circuit to sense and limit the inductor current to prevent crossing this mode boundary [11].

Excellent Closed Loop Response:

In the discontinuous mode, it is easy to obtain excellent response in correcting disturbances that result from large step changes in line voltage and load current, because the inductor always starts each switching cycle with zero stored energy. This makes it possible for the control circuit to obtain any energy level (and power output) required, from zero to full output, on a cycle-by-cycle basis. The inductor "vanishes" from the small signal closed loop characteristic, leaving only the output capacitor with its 90-degree phase lag. The resulting single-pole characteristic is inherently stable and easy to deal with in closing the loop. The right half plane zero that severely limits closed loop response in continuous mode boost and flyback circuits is not present in the discontinuous mode topologies.

High Peak Current:

The one main disadvantage of the discontinuous mode is the high peak current through the transistor, diode and output filter capacitor. This requires semiconductors with higher current capability and puts an extreme burden on the output filter capacitor ESR (equivalent series resistance) and RMS current rating requirements. For example, in both boost and fly back circuits, the diode is in the output, and therefore the average diode current, Id, must equal the OC output current, Io. Under full load conditions, if diode time td is 50% of the switching period, the peak current is 4 times the full load Io. In the buck circuit the inductor current with its better form factor drives the output, so the peak current is somewhat less in proportion to the output current. However, the buck topology is seldom used in the discontinuous mode because the continuous mode provides much better performance.

Poor Open Loop Line and Load Regulation:

The basic OC equation for the fly back topology operated in discontinuous mode is given below. The boost regulator has a similar but more complex formula. For the fly back circuit

$$V_o = V_{in} D \sqrt{\frac{R_o}{2 L_f}} \qquad 3.3$$

It can be seen from this equation that if the duty cycle is fixed (open control loop), V_o varies directly with V_{in} and the square root of the output load resistance, Ro. In other words, the open loop line and load regulation is quite poor, and duty cycle D must be changed considerably by the control circuit to maintain the desired out put voltage under the full range of line and load conditions.

Control Method:

In all three constant frequency control methods (direct duty cycle, voltage feed forward, and current mode), the output voltage is compared with a fixed reference voltage. The resulting error voltage is amplified and used as the closed loop control voltage, V_c.

Direct Duty Cycle Control:

Transistor duty cycle $D = \frac{t_{on}}{T}$ is varied in proportion to control voltage V_c. Poor open loop line and load regulation requires fairly high loop gain for correction. The output filter capacitor is part of the closed loop system and introduces a phase lag, which delays correction of V_{in} changes.

Voltage Feed forward Control:

A sample of the input voltage is fed directly into the control circuit and causes the duty cycle to vary inversely with V_{in} as well as directly with V_c

$$D = K \frac{V_c}{V_{in}}$$

If V_{in} increases, D decreases automatically so that the input volt-seconds ($V_{in}D$) remains constant for a fixed V_c. Thus, V_c controls input volt-seconds directly. Open loop line regulation is good, so that less closed loop gain is required to meet DC regulation requirements. Equation 3.3 becomes

$$V_o = KV_c \sqrt{\frac{R_o}{2L_f}} \qquad 3.4$$

Where K is the feed forward ratio = $\frac{V_{in}D}{V_c}$

Current Mode Control:

An inner, second control loop compares the peak inductor current, I_p, to the control voltage, V_c. In the outer loop, V_c now controls I_p directly. The inner loop provides good inherent line regulation, similar to voltage feed forward. Equation 3.3 becomes:

$$V_o = K V_c \sqrt{\frac{R_o L_f}{2}} \qquad 3.5$$

Where K is the inner loop current control factor $K = \frac{\max I_p}{\max V_c}$.

Either voltage feed forward or current mode control is recommended. They both have essentially the same good effect --improved open loop line regulation, providing instantaneous correction to line changes and requiring less closed loop gain.

3.1.2 Continuous mode operation:

In the continuous inductor current mode (continuous mode), the inductor current is never zero during any part of the switching cycle. Compared to the discontinuous mode for the same application parameters, the continuous mode requires much greater inductance. The inductor ripple current is small compared to the full load output current.

Current Waveforms

Continuous mode waveforms are shown in Figure 3.3 Just as with the discontinuous mode, the inductor, transistor and diode current waveforms are exactly the same for the buck, boost or fly back circuits, but the input and output waveforms differ according to which of the three elements are in series with input and output. The boost and fly back circuits have similar behavior. In both cases, the output current is the diode current, Id, which is discontinuous. The peak output current is slightly more than half the value encountered in the discontinuous mode. This reduces the burden on the output capacitor. The buck regulator behaves very differently. Its output current is the inductor current, which is not discontinuous, but has a relatively Figure 3.3 gentle slope and small ripple amplitude. This waveform is easy to filter, substantially reducing the output capacitor ESR and current rating requirements. For this reason, the continuous mode buck regulator is the most popular switching power supply configuration; particularly at higher power

levels where the much higher peak current encountered with all other configurations put an intolerable burden on the output filter capacitor.[11]

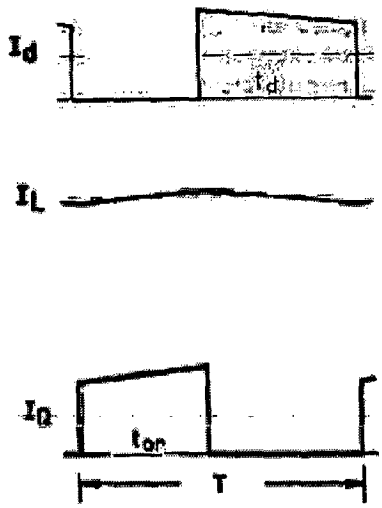


Fig 3.3 Inductor, Switch and Diode current wave forms under continuous current mode

	Buck	Boost	Fly back
I_{in}	I_Q	I_L	I_Q
I_o	I_L	I_d	I_d

Two States:

Because the inductor current is never zero, there is no idle time in the continuous mode and only two operational states during each switching cycle.

1. During transistor "on" time, ton, inductor current I_L increases from an initial value (greater than zero) to a higher value, replacing the inductor energy given up during the "off" time. Current (and power) is drawn from the input.
2. When the transistor is off, the diode conducts for the rest of each cycle. IL declines to the initial value, never reaching zero but giving up energy to the output.

In continuous mode operation, the up slope and down slope of inductor current are dependent only upon the input and output voltage levels and totally independent of the average inductor current or output load current. Without the flexibility provided by the third (idle) state of the discontinuous mode, V_{in}, Vo and duty cycle D are related differently for each topology. In the buck regulator, for example, the average voltage at the input side of the inductor is Vinton/T, or $V_{in}D$, while the voltage at the inductor output is Vo. In the steady state, the average voltage across the inductor must be zero, so $V_o = V_{in}D$. This is the basic DC equation for the buck regulator. There are no terms relating to load current or resistance, which indicates excellent open loop load regulation.

When Io changes, steady-state I_L also changes, but the inductor ripple current and V_o do not change.

Continuous Mode Boundary:

Minimum Load Current, when the load current decreases, the duty cycle and inductor ripple current do not change (except momentarily), but the average inductor current declines proportionately.

For the buck regulator $I_0 = I_L$,

For boost and fly back $I_o = (1\text{-}D)\ I_L$.

At a certain critical load current level, the inductor current reaches zero at the minimum of the ripple waveform. This is the boundary for continuous mode operation. If the load current further decreases, the third state idle time appears, and the circuit operates discontinuously, with completely different operating characteristics. DC regulation degrades radically. In a continuous mode regulator, the load current must not be allowed to drop below the critical level where this boundary is crossed. This minimum load requirement is a disadvantage of continuous mode systems.

Poor Closed Loop Response:

Small signal response of continuous mode regulators is much worse than discontinuous mode circuits because of the two pole second order characteristic of the resonant LC filter. Boost and fly back circuits also have a right half plane zero in their loop gain characteristic. While it is theoretically possible to compensate for the two filter poles, the capacitors used in the compensation network charge to unusual voltage levels during periods of large signal limited operation, when inductor current cannot keep up with changes in load current. This causes output voltage offset errors, which take considerable time for correction. Current mode control overcomes this problem in continuous mode buck regulators by eliminating the inductor pole. Only the single first order filter capacitor pole remains, the same as in the discontinuous mode circuits.

The RHP zero associated with boost and fly back continuous mode circuits is much more difficult to deal with. In buck regulators, output current 10 equals inductor current IL, but in boost and fly back circuits, $I_0 = I_L[1\text{-}D]$. Consider the process in a fly

back regulator. When load current increases, the output capacitor voltage immediately starts to drop. The resulting error voltage temporarily increases the duty cycle, D, causing the inductor current to rise to accommodate the increased load. However, it may take many cycles for the inductor current to complete its rise. During this time, increased D makes [1-D] smaller, so the output current is temporarily decreased, the opposite of what is desired. This additional lag because of the RHP zero inevitably forces the loop gain crossover frequency to be much lower than otherwise desired. There is in addition a large signal problem with continuous mode circuits--the inability to rapidly slew the inductor current as desired with large step changes in load. This is because of the large inductor values used in continuous mode circuits. The problem is most severe when attempting to increase the inductor current when operating near minimum V_{in}, especially if the circuit has been designed with input volt-second capability, V_{in} D, only slightly greater than required for steady state operation.

Good Open Loop Load Regulation & Poor Line Regulation

The basic DC equations for the continuous mode are:

Fly back	Boost	Buck
$V_o = \frac{V_{in} D}{1 - D}$	$V_o = \frac{V_{in}}{1 - D}$	$V_o = V_{in} D$

...3.6

Unlike the discontinuous mode, the above equations reveal that the DC output voltage, V_o, is totally independent of output current or resistance, depending only upon V_{in} and D. The duty cycle does not change with steady-state changes in load current, but D must be changed to make correction for changes in V_{in}.

Direct Duty Cycle Control

Moderately high loop gain is required to correct the inherent poor open loop line regulation. It is difficult to design the closed loop, and many problems cannot be overcome. See earlier comments under "Poor Closed Loop Response."

Voltage Feed forward. Voltage feed forward applied in the same way as the discontinuous mode topologies provides good open loop line regulation in the continuous mode buck regulator. Equation 3.6 (buck) becomes:

$$V_o = KV_c \qquad K = \frac{V_{in}D}{V_c} \qquad 3.7$$

Open loop line and load regulation are both good. Closed loop gain is now required only for good dynamic response to changes in load. Boost and fly back topologies in the continuous mode are only partially compensated by this simple feed forward technique. Methods that are more complex will achieve compensation, but they are beyond the scope of this paper.

Current Mode Control

Applied to continuous mode buck regulators, current mode control provides greatly improved performance. First, the inner current control loop provides inherent good line regulation, even with the outer loop open. Second, the inner loop eliminates the filter inductor pole so that the outer loop no longer has a two-pole second order resonant characteristic, but only the single filter capacitor pole. The gain characteristic becomes very easy to compensate. Third, compensation capacitors at the error amplifier input [which cause output voltage errors after large signal limited operation) are not required because the inductor pole is eliminated. Current mode control has the single disadvantage that it introduces load current dependency, which does need closed loop correction. Buck regulator Equation 4 becomes:

$$V_o = KV_cR_o \qquad K = \frac{\max I_p}{\max V_c} \qquad 3.8$$

Current mode control also facilitates the paralleling of several individual power supply modules. The current control loop insures that each module will always deliver its assigned proportion of the total load current. In the continuous boost and fly back topologies, the performance improvements from current mode control are less dramatic. Only partial voltage feed forward compensation is accomplished. When V_{in} changes, the inner current control loop maintains IL constant, but 10 will change because the (1-D) factor relating I_L to I_0 in boost and fly back circuits changes with V_{in}. Current mode

control does eliminate the inductor pole and thereby simplifies the closed loop design, but it does not eliminate the RHP zero, which is the worst limitation of the continuous mode boost and fly back circuits.

In this operating mode, the inductor current never reaches zero during one switching cycle and there is always energy stored in the inductor. The *volt seconds* applied to the inductor must be balanced throughout the line-cycle by continuously changing the duty-cycle of the converter using an appropriate control method.

3.2 FORCE-COMMUTATED THREE-PHASE CONTROLLED RECTIFIERS

Force-commutated rectifiers are built with semiconductor devices with gate turn-off capability. The gate turn-off capability allows full control of the converter, because valves can be switched ON or OFF whenever required. This allows commutation of the valves hundred of times in one period which is not possible with line commutated rectifiers where thyristors are switched ON or OFF only once a cycle.

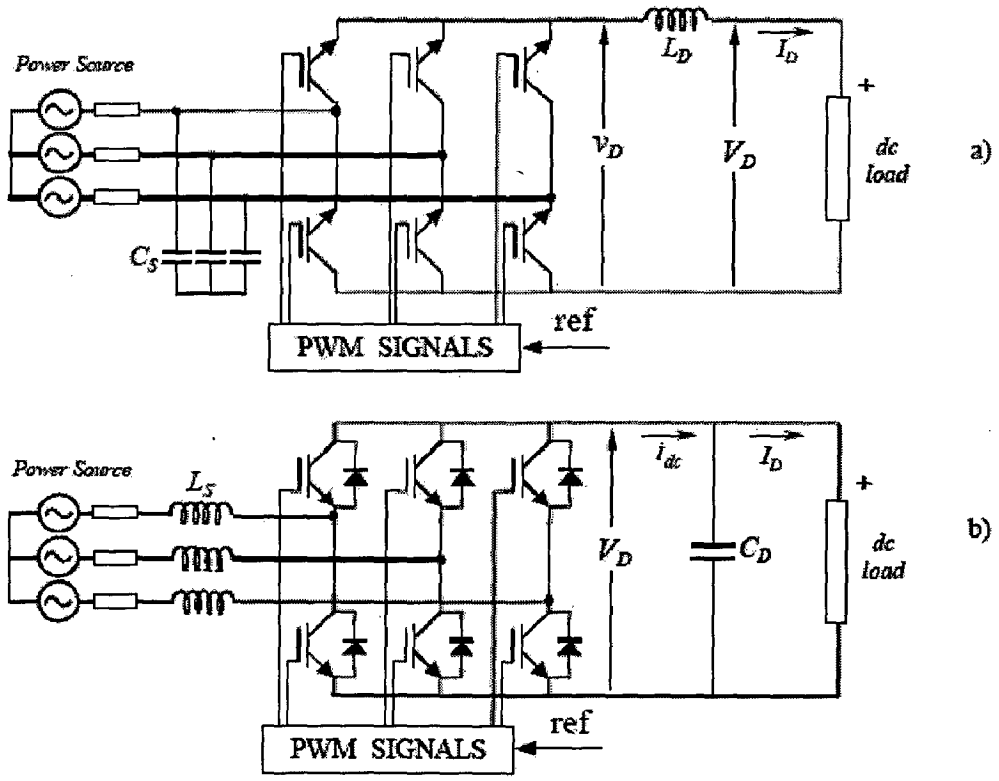


Figure [3.4]: Basic topologies for force-commutated PWM rectifiers
A) Current Source Rectifier, B) Voltage Source Rectifier

Advantages of Force-commutated rectifiers:

a) The current or the voltage can be modulated (Pulse Width Modulation or PWM), generating less harmonic contamination;

b) Power factor can be controlled; it can be made leading also;

c) They can be built as voltage or current source rectifiers;

d) The reversal of power in thyristor rectifiers is by reversal of voltages at the DC link. Instead, the force-commutated rectifiers can be implemented for both reversal of voltage and reversal of current.

Here are two ways to implement force-commutated three-phase rectifiers

- As a current source rectifier, where the power reversal is by dc voltage reversal
- As voltage source rectifier, where the power reversal is by current reversal at the dc link.

Operation of the voltage source rectifier

The voltage source rectifier is the most widely used rectifier and because of its duality with the current source rectifier only its operation will be described in detail.

The basic operation principle of the voltage source rectifier consists on keeping the dc link voltage at a desired reference value, using a feedback control loop. To accomplish this task the voltage V_D is measured and compared with a reference V_{REF}. The error signal generated from this comparison is used to switch ON and OFF the six valves of the rectifier. In this way the power can come or return to the ac source according to the dc link voltage requirements. The voltage V_D is measured at the capacitor C_D.

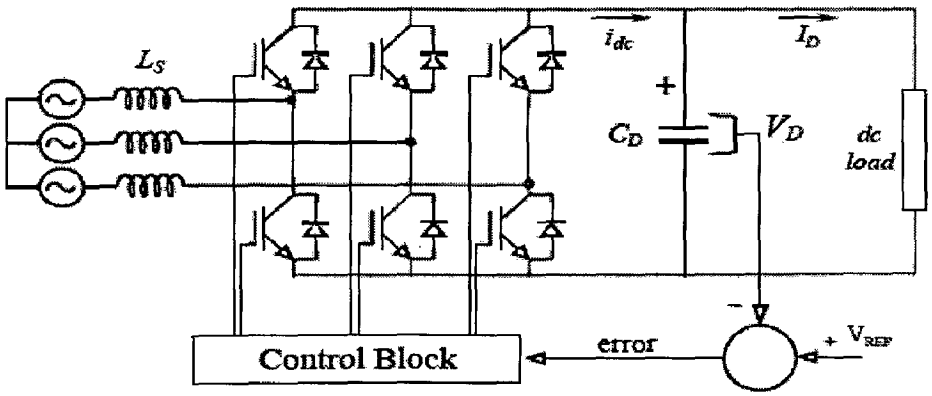


Figure [3.5]: Operation of the Voltage Source Rectifier

When the current I_D is positive (rectifier operation), the capacitor C_D is discharged, and the error signal ask the Control Block for more power from the *ac* supply. The Control Block takes the power from the supply by generating the appropriate PWM signals for the six valves. In this way, more current flows from the *ac* to the *dc* side, and the capacitor voltage is recovered. Inversely, when I_D becomes negative (inverter operation), the capacitor C_D is overcharged, and the error signal ask the control to discharge the capacitor and return power to the *ac* mains [12].

The PWM Control not only can manage the active power, but reactive power also, allowing this type of rectifier to correct power factor. Besides, the ac current waveforms can be maintained almost sinusoidal, reducing hamonic contamination to the mains supply.

The Pulse-Width-Modulation consists on switching the valves ON and OFF, following a pre-established template. Particularly, this template could be a sinusoidal waveform of voltage or current. For example, the modulation of one phase could be as the one shown in figure [3.6]. This PWM pattern is a periodical waveform whose fundamental is a voltage with the same frequency of the template. The amplitude of this fundamental, called V_{MOD} in figure [3.6], is also proportional to the amplitude of the template.

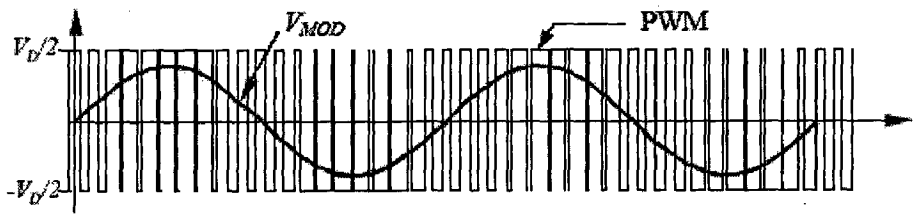


Figure [3. 6]: PWM Patten and its fundamental V_{MOD}

To make the rectifier works properly; the PWM pattern must generate a fundamental V_{MOD} with the same frequency of the power source. Changing the amplitude of this fundamental, and its phase-shift with respect to the mains, the rectifier can be controlled to operate in the four quadrants: leading power factor rectifier, lagging power factor rectifier, leading power factor inverter, and lagging power factor inverter. The interaction between V_{MOD} and V (source voltage) can be seen through a phasor diagram.

This interaction permits to understand the four-quadrant capability of this rectifier. In the figure [3.8], the following operations are displayed: a) rectifier at unity power factor, b) inverter at unity power factor, c) capacitor (zero power factor), and d) inductor (zero power factor)[13] .

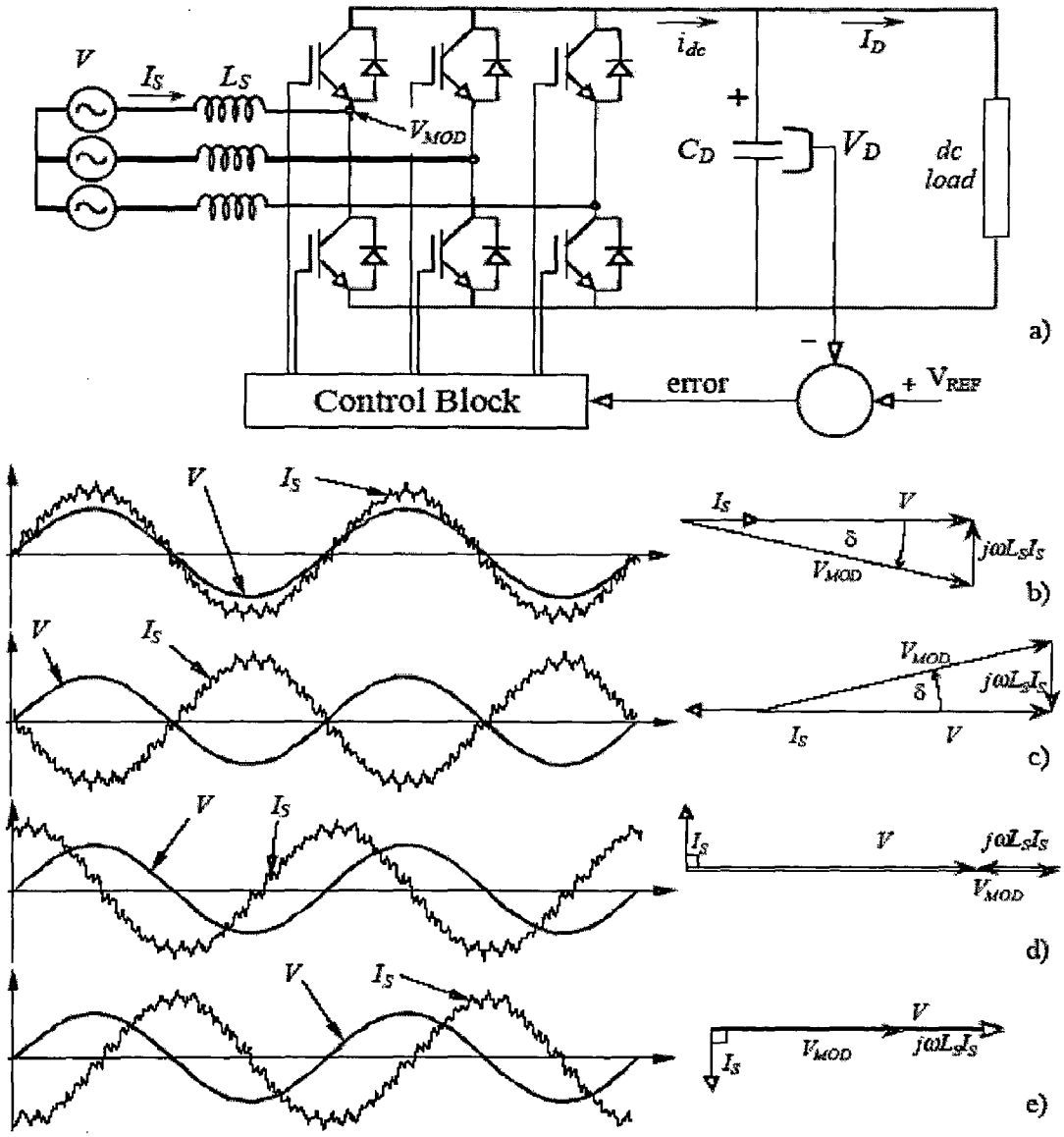


Figure [3.8]: Four-quadrant operation of the force commutated rectifier

a) The PWM force commutated rectifier
b) Rectifier operation at unity power factor
c) Inverter operation at unity power factor
d) Capacitor operation at zero power factor
e) **Inductor operation at zero power factor**

Voltage Source Current Controlled Rectifier:

This type of control as shown in figure [3. 9] is implemented by measuring the instantaneous phase currents and forcing them to follow a sinusoidal current reference template. The amplitude of the current reference template I_{MAX} is evaluated using the following equation.

$$I_{MAX} = G_C.e = G_C.(V_{REF}-v_D) \quad \text{... ... ...3.9}$$

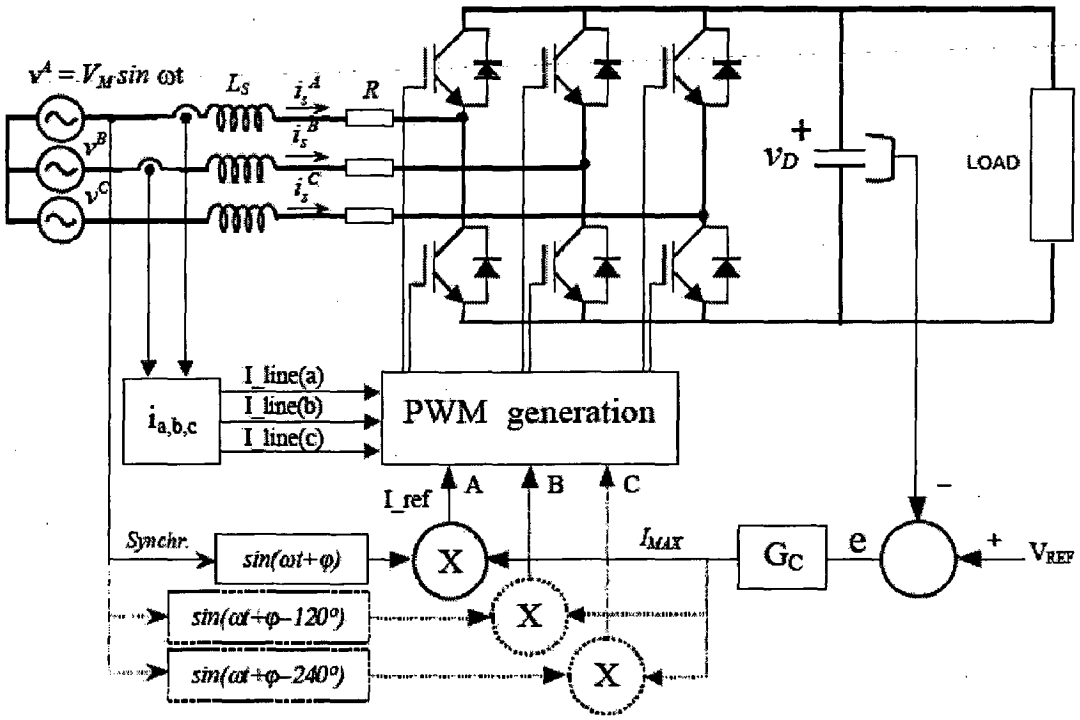


Figure [3. 9]: Voltage Source Current Controlled Rectifer

Where G_C has been shown in figure [3.9], and represents the controller such as fuzzy, PI, P, and other. The sinusoidal waveform of the template is obtained by multiplying I_{MAX} with a sine function, with the same frequency of the mains, and with the desired phase-shift angle ϕ as shown in figure [3.9]. Besides, the template must be synchronized with the power supply. After that, the template has been created, and is ready to produce the PWM pattern.

Voltage source voltage controlled PWM rectifier

The figure [3.10] shows a one-phase diagram from which the control system for a voltage source voltage controlled rectifier is derived. This diagram represents an equivalent circuit of the fundamentals, i.e., pure sinusoidal at the mains side, and pure dc at the *dc* link side. The control is achieved by creating a sinusoidal voltage template V_{MOD}, which is modified in amplitude and angle to interact with the mains voltage V. In this way the input currents are controlled without measuring them. The template V_{MOD} is generated using the differential equations that govern the rectifier.

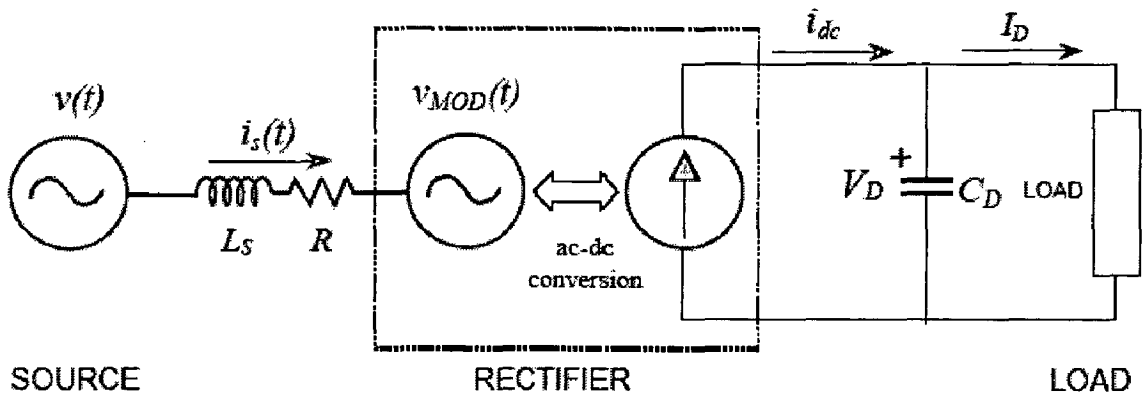


Figure [3. 10]: One-phase Fundamental diagram of the voltage source rectifier

From figure [3.10] the following differential equation can be derived:

$$V(t) = L_s \frac{di_s}{dt} + Ri_s + V_{MOD}(t) \qquad \text{... ... ... .3.10}$$

Assuming that $v(t) = V\sqrt{2}\sin(wt)$, then the solution for $i_s(t)$, to get a template V_{MOD} able to make the rectifier work at constant power factor should be of the form

$$i_s(t) = I_{MAX}(t)\sin(wt + \phi) \qquad \text{... ... ... .3.11}$$

Equations (3.9) (3.11) and v(t) allows to get a function of time able to modify V_{MOD} in amplitude and phase, which will make the rectifier work at fixed power factor. Combining these equations with v(t) it yields:

$$v_{MOD}(t)=\left[V\sqrt{2}+X_S I_{MAX}\sin\phi-\left(RI_{MAX}+L_s\frac{dI_{MAX}}{dt}\right)\cos\phi\right]\sin\omega t-\left[X_S I_{MAX}\cos\phi+\left(RI_{MAX}+L_s\frac{dI_{MAX}}{dt}\right)\sin\phi\right]\cos\omega t \quad \text{3.12}$$

The equation (3.12) allows getting a template for V_{MOD}, which is controlled through variations of the input current amplitude I_{MAX}. The derivatives of I_{MAX} into equation (3.12) make sense, because I_{MAX} changes every time the *dc* load is modified. The term X_S in eq. (3.12) is ωL_S. This equation can also be written for unity power factor operation. In such a case $\cos\phi = 1$, and $\sin\phi = 0$:

$$v_{MOD}(t)=\left(V\sqrt{2}-RI_{MAX}-L_s\frac{dI_{MAX}}{dt}\right)\sin\omega t-X_S I_{MAX}\cos\omega t \quad \text{... ... ...3.13}$$

With the Eq no. (3.13), a unity power factor, voltage source, voltage controlled PWM rectifier can be implemented as shown in figure 3.11]. It can be observed that equations (3.12) and (3.13) have an *in-phase* term with the main supply (sin ωt), and an *in-quadrature* term (cos ωt). These two terms allow the template V_{MOD} to change in magnitude and phase, to have full unity power factor control of the rectifier.

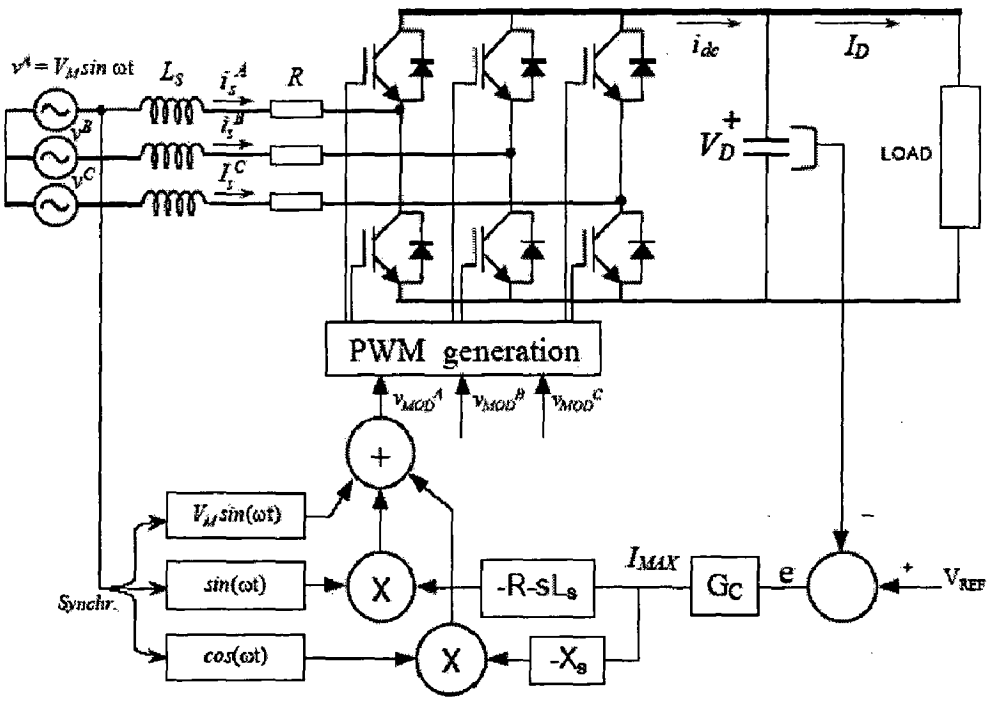


Figure [3.11]: Implementation of the voltage controlled rectifier for unity power factor operation

Compared with the control block of figure [3. 3], in the voltage source voltage controlled rectifier of figure [3.10], there is no need to sense the input currents. However, to ensure stability limits as good as the limits of the current controlled rectifier, the blocks '**–R–sL$_S$**' and '**–X$_S$**' in figure [3.10], have to emulate and reproduce exactly the real values of *R*, *XS* and *LS* of the power circuit. However, these parameters do not remain constant, and this fact affects the stability of this system, making it less stable than the system showed in figure [3. 5].

Voltage source load controlled PWM rectifier

A simple method of control for small PWM rectifiers (up to 10-20 kW) is based on the direct control of the *dc* current. The figure [3.11] shows the schematic of this control system. The fundamental voltage V_{MOD} modulated by the rectifier is produced by a fixed and unique PWM pattern, which can be carefully selected to eliminate most undesirable harmonics. As the PWM does not change, it can be stored in a permanent digital memory (ROM).

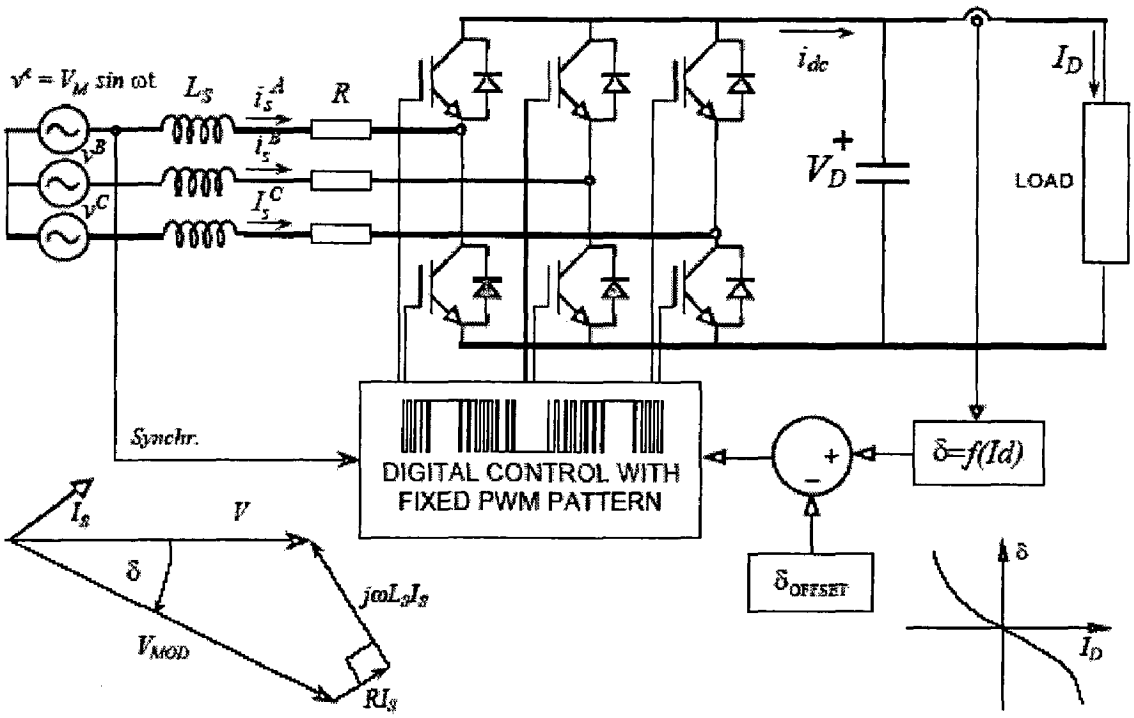


Figure 3.12: Voltage Source Load Controlled PWM Rectifier

The control is based on changing the power angle δ between the mains voltage V and fundamental PWM voltage V_{MOD}. When δ changes, the amount of power flow transferred from the *ac* to the *dc* side changes. When the power angle is negative (V_{MOD} lags V), the power flow goes from the *ac* to the *dc* side. When the power angle is positive, the power flows in the opposite direction. Then, the power angle can be controlled through the current I_D. The voltage V_D does not need to be sensed, because this control establishes a stable *dc* voltage operation for each *dc* current and power angle. With these characteristics, it is possible to find a relation between I_D and δ, to get constant *dc* voltage for all load conditions. This relation is given by:

$$ID = f(\delta) = \frac{V\left(\cos\delta - \frac{\omega L_s}{R}\sin\delta - 1\right)}{R\left[1+\left(\frac{\omega L_s}{R}\right)^2\right]} \quad \ldots\ldots\ldots 3.14$$

From equation (3.14) a plot and a reciprocal function δ = *f(ID)* is obtained to control the rectifier. The relation between I_D and δ allows leading power factor operation and null regulation. The leading power factor operation is shown in the phasor diagram of figure [3.12]. he control scheme of the voltage source load controlled rectifier is characterized by the following: i) there is neither input current sensors nor dc voltage sensor; ii) it works with a fixed and predefined PWM pattern; iii) it presents a very good stability; iv) its stability does not depend on the size of the *dc* capacitor; v) it can work at leading power factor for all load conditions; and vi) it can be adjusted with eq. (3.14) to work at zero regulation. The drawback appears when R in equation (3.14) becomes negligible, because in such a case the control system is unable to find an equilibrium point for the *dc* link voltage. That is the reason why this control method is not applicable to large systems.

The additional advantages of force-commutated rectifiers with respect to line-commutated rectifiers make them better candidates for industrial requirements. They permit new applications such as rectifiers with harmonic elimination capability (active filters), power factor compensators, machine drives with four-quadrant operation, frequency links to connect 50 Hz with 60 Hz systems, and regenerative converters for traction power supplies. The modulation with very fast valves such as IGBTs permits to

get almost sinusoidal currents. The dynamics of these rectifiers is so fast that they can reverse power almost instantaneously. In machine drives, current source PWM rectifiers can be used to drive *dc* machines from the three-phase supply. Four-quadrant applications, using voltage source PWM rectifiers, are extended for induction machines, synchronous machines with starting control, and special machines such as brushless-dc motors. Back-to-Back systems are being used in many countries to link power systems with different frequency.

In this chapter I have discussed about basic types of high power factor converters and basic operations continuous and discontinuous current conduction modes in detail. After that I have discussed about types of forced commutated rectifiers and some of the topologies to get unity power factor and better performance.

CHAPTER-4
PROPOSED CONTROL TECHNIQUE

4.1 Existing control techniques

Due to the increase of non-linear loads in utility systems, the quality of power has attracted much attention in resent years. The low power factor and large harmonics line currents generated by uncontrolled rectifiers are well known problems that can lead to voltage distortion, and increase losses in the transmission and distribution lines. To overcome these problems active current wave-shaping techniques have been developed to provide nearly sinusoidal source current. [14]

Current control technique plays the most important role in current-controlled pulse-width modulated (PWM) rectifiers. Various techniques for the current controller of the PWM rectifier have been proposed. However, among these techniques, considering Easy implementation, fast dynamic response, Maximum current limit and insensitivity to load parameter variation. The HCC is a rather popular one. Nevertheless, due to lack of coordination among individual hysteresis current controllers of three phases, high switching frequency may happen and the current error is not strictly limited. Some hysteresis current control techniques applying the zero vectors to reduce the number of switching were reported recently.

On the other hand, the space vector modulation (SVM) has been very popular in the past few years; the technique has gained ground as an effective means of generating PWM vector controlled drives. Space vector modulation offers many advantages, compared to the conventional pulse width modulation (PWM) method.

Among these, the key benefits are:

- 15% increase in the maximum line-to-line voltage obtainable, without over modulation, when compared to conventional PWM with Only 87% of the dc link voltage.
- Reduced switching losses converter, and
- Reduced harmonic distortion in the current. [15]

The SVM technique confines state space vectors to be applied according to the region where the output voltage vector is located. To minimize the current error between the current command and line current, the SVM technique requires a considerable calculation burden. The space vector approach can provide fast dynamic control, but is quite complicated to implement and requires significant computational resources. High-speed microprocessors or digital signal processors are required. [16]

On the other hand, the HCC can be utilized to make the line current vector track the command vector with almost negligible response time and insensitivity to line voltage and parameter variation. However, the HCC generates other vectors besides the state space vectors required according to the region in the SVM technique and increases the number of switching. If the zero vectors are applied to reduce the magnitude of the line current vector, the line current is decreased with slow slope and the number of switching is decreased. Thus the utilization of non-zero vectors instead of the zero vectors for decreasing the line current increases the number of switching. Therefore, a SVM-based HCC utilizing all features of the HCC and SVM technique needs to be developed.

4.1.1 HYSTERESIS CURRENT CONTROL

Hysteresis band current control method is used for the PWM rectifiers. Figure 4.1 Shows the PWM rectifier with the hysteresis current controller. In this system, three line currents are sensed and compared with their respective reference line currents and resulting errors are amplified and send to their respective hysteresis current controllers. The hysteresis current controllers generate switching gate pulses for the switching devices of the converter as shown in figure 4.1 and 4.2. The hysteresis control is lost if error magnitude is smaller than the magnitude of the hysteresis band. The width of the hysteresis band is chosen sufficient small using trail and error method in order to operate the switching devices well below their maximum switching frequency capability, for a maximum line current operation. For narrow hysteresis band, the switching frequency is higher and current wave shape is more sinusoidal, hence using trail and error a compromise is done between switching frequency and quality of current wave shape. With narrow hysteresis band the possibility of loss of hysteresis control is avoided, hence devices having higher switching frequency range should be selected.

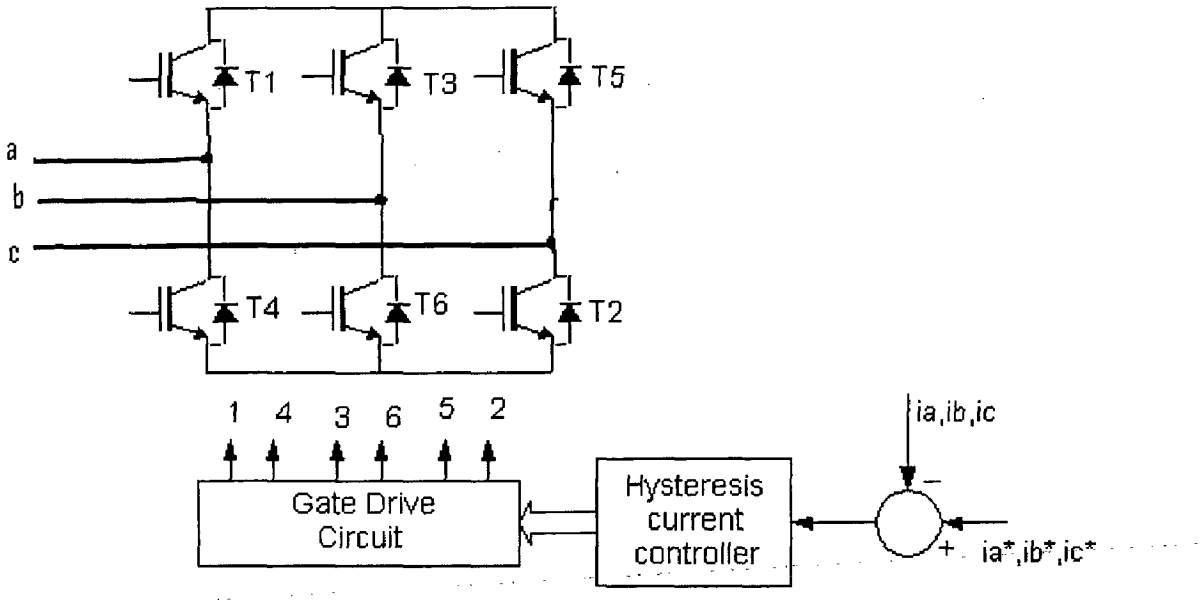


Fig 4.1 Hysterisis current control

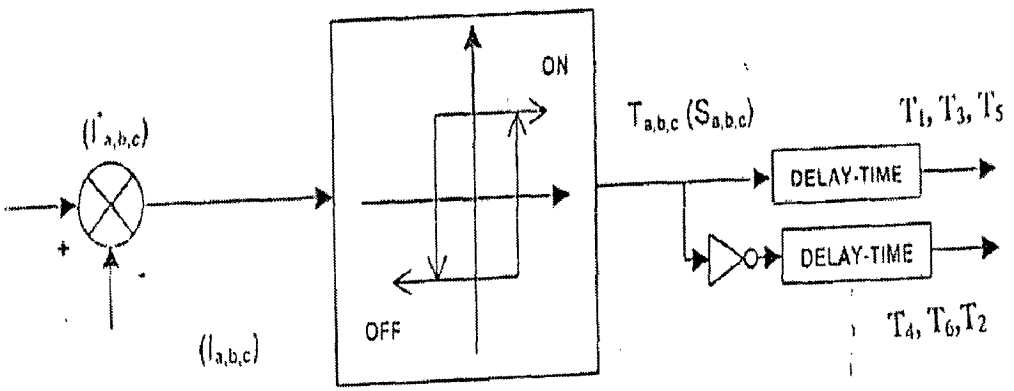


Fig.4.2 Hysterisis current controller

General features of switching table and hysteresis controllers

- The switching frequency depends on the hysteresis wide of active and reactive power comparators.
- Zero vectors decrease switching frequency but it provides short-circuit for the line-to-line voltage.
- Zero vectors $U_0(000)$ and $U_7(111)$ should be appropriate chosen
- Switching table with *PLL* sector detection guarantees a very stable and free of disturbances operation, even under distorted and unbalanced line voltages.

4.1.2 Space Vector Modulation

Space vector modulation (SVM) was originally developed as a vector approach to pulse-width modulation (PWM) for three-phase inverters [14]. As SVM has developed, there appears to be some confusion about its characteristics and advantages.

Typical claims made for SVM include the following.

- It achieves the wide linear modulation range associated with PWM third-harmonic injection automatically, without the need for distorted modulation.
- It has lower base band harmonics than regular PWM or other sine based modulation methods, or otherwise optimizes harmonics.
- Only one switch changes state at a time.
- It is fast and convenient to compute [17]

The general power circuit of the PWM rectifier with voltage link is shown in figure 4.2. The switching function for switch S_k (k= 1, 2 . . . 6) is defined as

S_k^* =1 when switch S_k is on

S_k^* =0 when switch S_k is off

In the PWM rectifier with voltage link, either S_1 or S_4 (S_3 or S_6, S_5 or S_2) is conducting and only one of them is allowed to conduct in any moment, i.e.

$$S_1^* + S_4^* = 1 \qquad (4.1)$$

$$S_3^* + S_6^* = 1 \qquad (4.2)$$

$$S_2^* + S_5^* = 1 \qquad (4.3)$$

In the PWM rectifier, the space vector $\mathbf{V}n$ is represented as

$$V_n = 1/3\ V_d [(S_1^* - S_4^*) + (S3^* - S_6^*)\, e^{j2.\ /3} + (S5^* - S_2^*)\, e^{-j2.\ /3}] \qquad (4.4)$$

Where V_d is the d.c. link voltage. Substituting the switching function, 1 or 0, of each phase into (4.4), the following discrete space vectors are obtained

$$V_n = 2/3\ V_d\, e^{j(n-1).\ /3},\quad n=1,2,\ldots,6 \qquad (4.5)$$

$$V_n = 0,\quad n=0 \qquad (4.6)$$

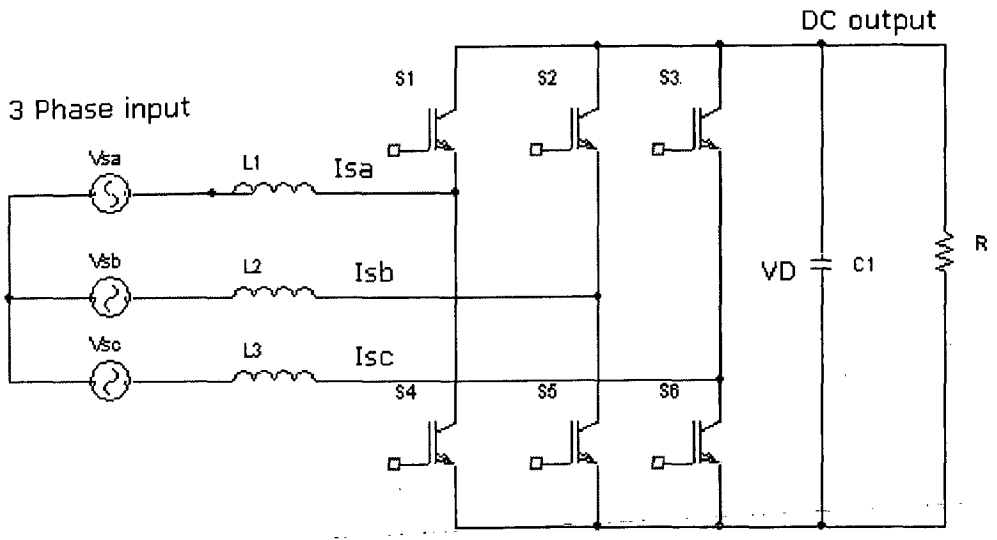


Fig. 4.3 power circuit of PWM rectifier with link

The available space voltage vectors according to eight switch states are shown in figure 4.4(*a*). Among these space voltage vectors, **V0** is the zero voltage vectors and it has two switching patterns $\mathbf{V}_0$ (0 0 0) and $\mathbf{V}_0$ (1 1 1). To obtain the required rectifier input space voltage vector $\mathbf{v}_r(t) = V_{rm} e^{j \cdot st}$, The conduction times of the switches are modulated according to the amplitude and angle of $\mathbf{v}_r$. V_{rm} and . $_s$ are the peak voltage and angular frequency of the space voltage vector $\mathbf{v}_r$, respectively. The angle of $\mathbf{v}_r$ determines a region among six regions in the complex plane. The rectifier input space voltage vector $\mathbf{v}_r$ in figure4.4 (*b*) is modulated as:

$$V_r(t) = d_\alpha V_\alpha + d_\beta V_\beta \qquad (4.7)$$

This is called the space vector modulation. Then the duty cycles d_α and d_β of two state space vectors V_α and V_β adjacent to the required space vector $\mathbf{v}_r$ in a given region, and the duty cycle d_0 of the zero vector are given by

$$d_\alpha = m\sin\left(\frac{\pi}{3} - \theta_r\right)$$

$$d_\beta = m\sin\theta_r$$

$$d_o = 1 - d_\alpha - d_\beta \qquad (4.8)$$

Where the modulation index m (m 0. m . 1) is defined as

$$M = 3V_{rm} / V_d \qquad (4.9)$$

Thus, the SVM technique utilizes three space vectors $\mathbf{V}_.$, $\mathbf{V}_.$, and **V0** to generate the rectifier input voltage vector $\mathbf{v}_r$ in the specified region.

Using Kirchhoff's voltage law from figure 4.1, the following equation is obtained

$$Ldi_s/dt = V_s - V_r \qquad (4.10)$$

Where is i_s the source line current vector, v_s is the source voltage vector, L is the inductance of the input filter, and v_r is the rectifier input space voltage vector. The current error vector i_e is defined as

$$i_e = i_s^* - i_s \qquad (4.11)$$

Where i_s^* is the reference current vector. Substituting (4.11) into (4.10) produces

$$Ldi_e/dt = V_r - V_s + Ldi_s^*/dt \qquad (4.12)$$

Thus, the line current error i_e is influenced by the derivative of the current command, the source voltage and the rectifier input space voltage vector. To obtain the zero current error between the reference current vector i_s^* and the line current vector i_s, the desired input voltage vector vr of the rectifier is as follows from (4.12)

$$V_r^* = V_s - Ldi_s^*/dt \qquad (4.13)$$

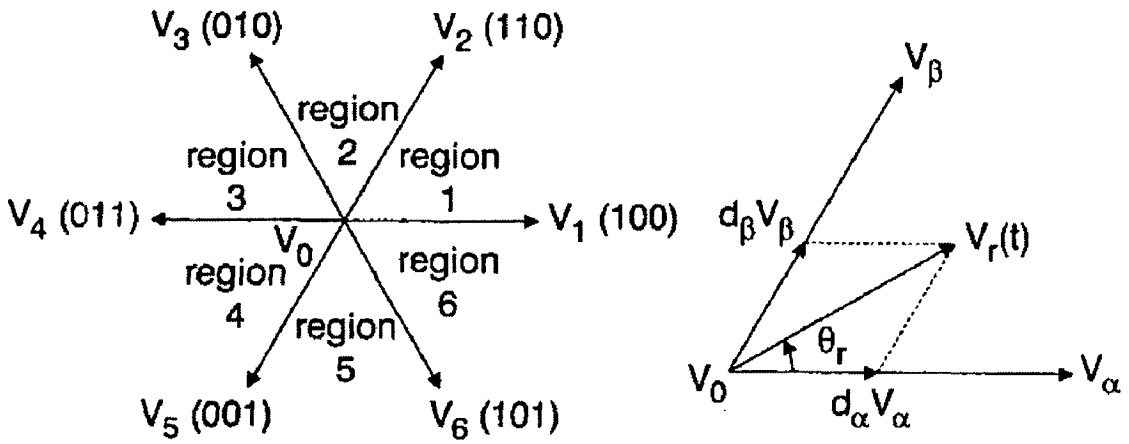


Figure 4.4 State space vectors and voltage components of the PWM rectifier with voltage link: (*a*) state space vectors (*b*) voltage components.

Since the rectifier input voltage v_r is modulated to generate the desired space voltage vector v_r^*, v_r is represented by the quantized space vector V_n. Then equation (4.12) becomes $Ldi_e/dt = V_n - Vr^*$ (4.14)

Where v_r^* is the reference space voltage vector required to generate the current reference vector i_s^* without any current deviation.

4.2 PROPOSED CONTROL TECHNIQUE

SVM-based HCC for the three-phase PWM rectifier

A SVM-based HCC for the three-phase PWM rectifier is proposed. This technique utilizes advantages of the HCC and SVM technique. This configuration reduces significantly the number of switching and at the same time gives the same state space vectors as those obtained from the SVM technique. The proposed current controller confine state space vectors from a region detector and applies a proper space vector selected according to the HCC for better current shape. A set of state space vectors including the zero vectors is determined from the region detector made up of three comparators.

In general, the HCC can be utilized to make the line current vector track the command vector with almost negligible response time and insensitivity to the line voltage and parameter variation. However, due to lack of coordination among three individual hysteresis current controllers, high switching frequency may happen and the current error is not strictly limited. This problem in the HCC can be solved using the space vector concept. When the reference space vector v_r^* is in Region I, the derivative vectors of the current error corresponding to the PWM phase voltage V_n are shown in figure 4.5. The proper state space vectors to generate the reference space voltage vector v_r^* in this region are V_1, V_2, and V_0. However, the general HCC generates other state space vectors including these vectors in fig 4.5(b). To reduce the number of switching, di_e/dt is the most important variable. In order to reduce the number of switching, it is necessary to choose a voltage vector V_n so that . di_e/dt. n is as small as possible[17].

If the zero vectors is applied to reduce the magnitude of the current error vector except V_1 and V_2 in Region I, the line current is decreased with slow slope and the

number of switching is decreased, as shown in fig 4.5(c). The utilization of non-zero vectors instead of the zero vector gives steep slope for the current error due to large voltage difference $\mathbf{v}_r^* - \mathbf{V}_n$ as shown in figure 4. A set of state space vectors to be applied according to the region depends on the position of the reference space voltage vector in (4.1.3)

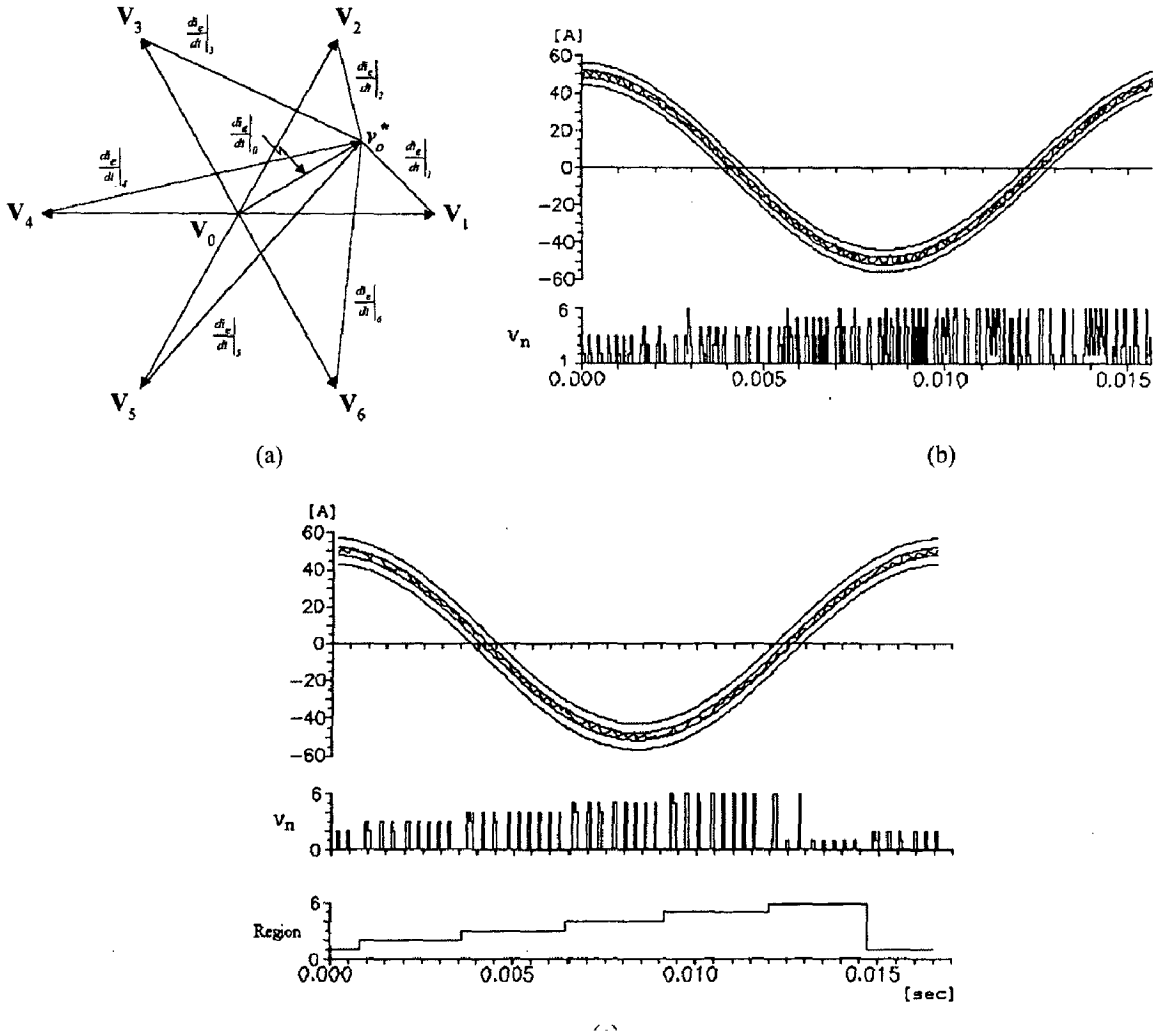


Figure 4.5 Principle of the switching frequency reduction. (a) Derivative vectors of the current error in Sector I. (b) Current waveform and space vectors when the HCC does not use the sector information. (c) Current waveform and space vectors when the HCC uses the sector information.

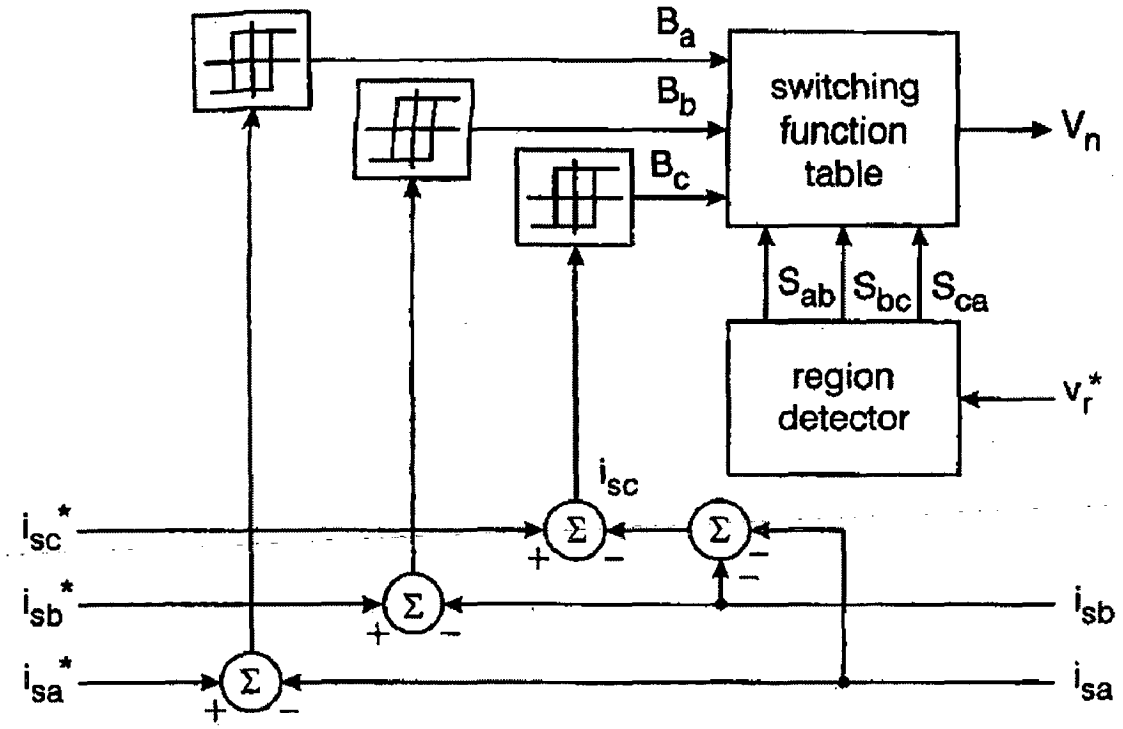


Figure 4.6 SVM-based HCC: (*a*) block diagram of the proposed current controller.

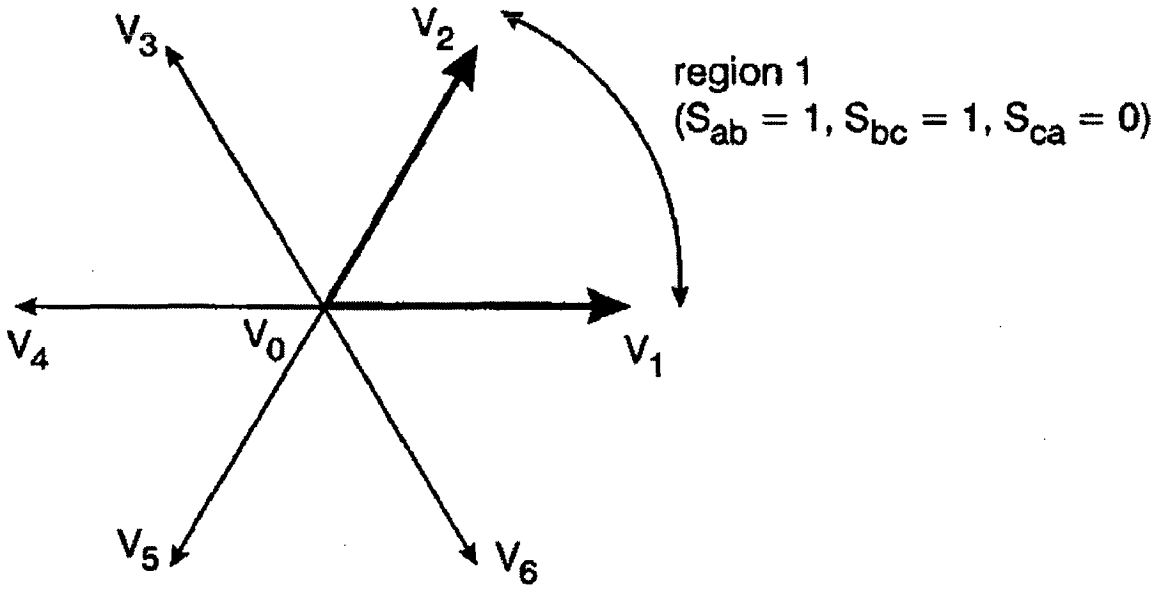


Fig. 4.6 SVM-based HCC: (*b*) Relation of the voltage vectors and the output of the region detector.

The region detector is proposed to detect the position of the reference space voltage vector. A region is detected from output signals of three comparators. The SVM based HCC is shown in figure 4.6(*a*), where a region detector is utilized to detect a region of the reference space voltage vector in (4.13) and it confines state vectors to be applied like the SVM technique. The region detector determines a set of spaœ vectors to be applied according to the digital output signals (S_{ab}, S_{bc}, S_{ca}) of comparators. The input of the comparators is the voltages v_{ra}, v_{rb}, and v_{rc} which are the component of the reference space voltage vector $\mathbf{v}_r^*$. S_{ab}, S_{bc}, and S_{ca} are given as

$$S_{ab}=\text{sign}\,(V_{ra}^* - V_{rb}^*) \qquad (4.15)$$

$$S_{bc}=\text{sign}\,(V_{rb}^* - V_{rc}^*) \qquad (4.16)$$

$$S_{ca}=\text{sign}\,(V_{rc}^* - V_{ra}^*) \qquad (4.17)$$

Where sign (y) =1 if y>0 sign (y) =0 if y. 0 (4.18)

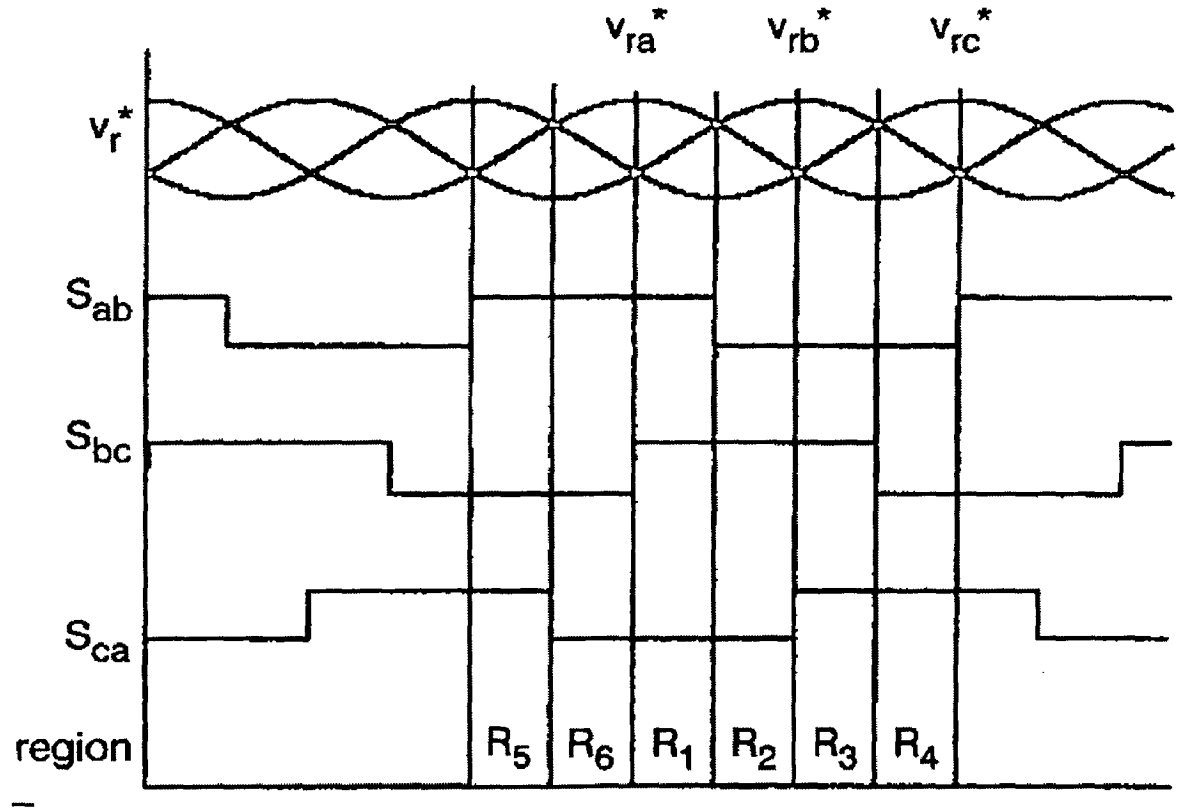


Figure 4.7 Determination of regions from the region detector.

The signals S_{ab}, S_{bc}, and S_{ca} include the information about the region of the reference space voltage vector $\mathbf{v}_r^*$ as shown in figure 4.7. The logic equation to detect the region is given as:

$$R_1 = S_{ab} S_{bc} S_{ca}'$$
$$R_2 = S_{ab}' S_{bc} S_{ca}'$$
$$R_3 = S_{ab}' S_{bc} S_{ca}$$
$$R_4 = S_{ab}' S_{bc}' S_{ca}$$
$$R_5 = S_{ab} S_{bc}' S_{ca}$$
$$R_6 = S_{ab} S_{bc}' S_{ca} \qquad (4.19)$$

Where R means the region and ' is the logical NOT operator. From (19), S_{ab}= 1, S_{bc}= 1, and S_{ca}= 0 indicate Region I.

The relation of the state space vector and the output of the region detector are shown in figure 4.6(*b*). Three hysteresis comparators are used to track the current command vector and limit the current error within the specified bound. B_a denotes a status of the bound of the *a*-axis current error. The state space vectors $\mathbf{V}_0$, $\mathbf{V}_1$, and $\mathbf{V}_2$ in Region I are utilized like the SVM technique as shown in figure 4.6(*b*). When the current error of the *a*-axis hits the upper bound of the hysteresis comparator and the current error of the *b*-axis hits the lower bound, B_a= 1 and B_b= 0. The voltage vector $\mathbf{V}_1$ is applied to increase the *b*-axis current i_b and *c* axis current *ic* simultaneously when B_b= 1 and B_c= 1.

On the other hand, $\mathbf{V}_2$ is applied to decrease i_a and i_b simultaneously when B_a= 0 and B_b= 0. In the other cases, the zero vector $\mathbf{V}_0$ is applied. The switching table for all regions is shown in table 4.1. Figure 6.6 shows the control circuit for the proposed current controller. Therefore, the gate logic of the programmable array logic (PAL) device is given by

$$Y_1 = R_1 (B_a' B_b B_c + B_a' B_b' B_c) + R_2 B_a' B_b' B_c + R_5 B_a' B_b B_c' + R_6 B_a' B_b B_c' + B_a' B_b B_c$$

$$Y_2 = R_3 B_a' B_b' B_c + R_4 (B_a' B_b' B_c + B_a B_b' B_c) + R_5 (B_a B_b' B_c + B_a B_b' B_c') + R_6 B_a B_b' B_c'.$$

$$Y_3 = R_1 B_a B_b' B_c' + R_2 (\mathrm{Ba}\, B_b' B_c' + B_a B_b B_c') + R_3 (B_a B_b B_c' + B_a B_b' B_c' + R_4 B_a' B_b B$$

S_{ab}	S_{bc}	S_{ca}	B_a	B_b	B_c	V_n	Region
1	1	0	0	1	0	V_1	1
			0	0	1	V_2	
			Other Cases			V_0	
0	1	0	0	0	1	V_2	2
			1	0	1	V_3	
			Other Cases			V_0	
0	1	1	1	0	1	V_3	3
			1	0	0	V_4	
			Other Cases			V_0	
0	0	1	1	0	0	V_4	4
			1	1	0	V_5	
			Other Cases			V_0	
1	0	1	1	1	0	V_5	5
			0	1	0	V_6	
			Other Cases			V_0	
1	0	0	0	1	0	V_6	6
			0	1	1	V_1	
			Other Cases			V_0	

Table.4.1. Switching table for the proposed currentcontroller.

. The block diagram of the proposed SVM-based HCC for the PWM rectifier is shown in figure 4.8. To determine practically the region of the desired input voltage vector $\mathbf{v}_r^*$ in (4.13) by the region detector, the derivative of the current command vector $\mathbf{i}_c$ is required. The peak current I of the current command vector is given by the d.c. link voltage controller and the variation of I depends on the dynamic characteristic of the voltage controller.

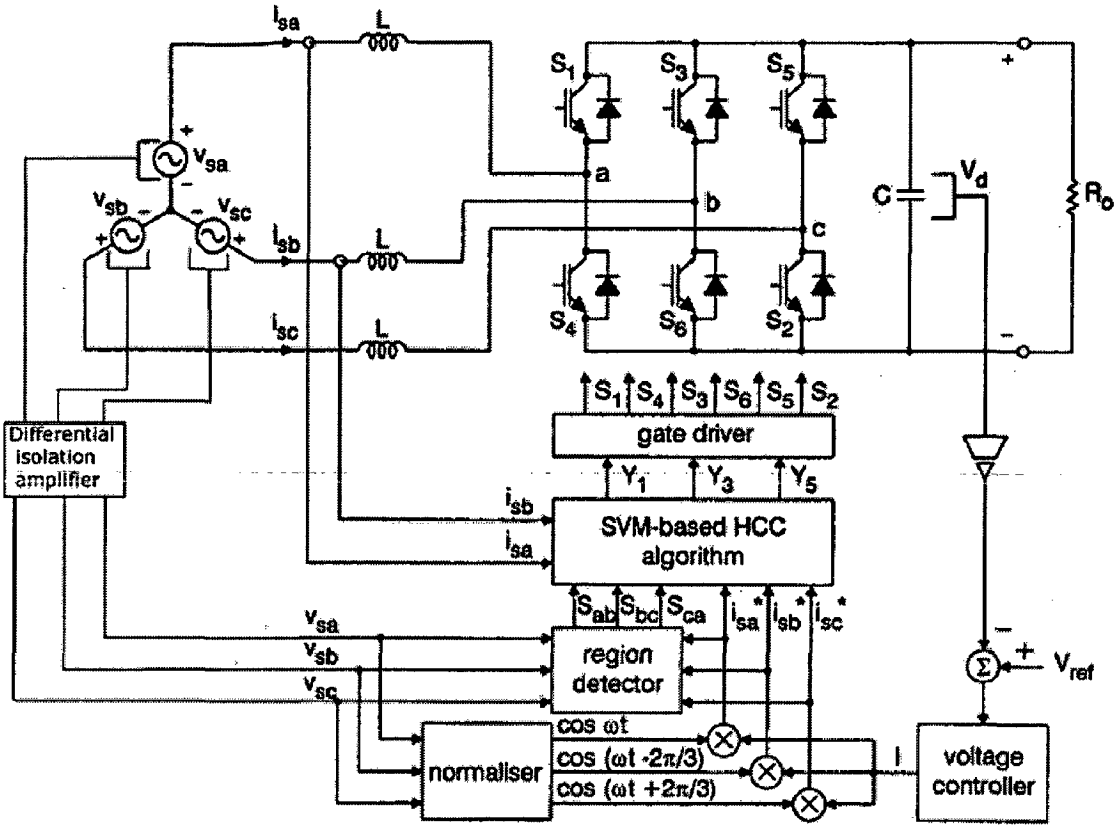


Figure 4.8 Block diagram of the proposed SVM-based HCC.

The current command vector is obtained by the multiplication of the peak current and signals in phase with the source voltage vector via the normalizer as shown in figure 4.7. In general, the differentiator is designed to have the characteristic of the low-pass filter to remove the high frequency noise. Then the bandwidth of the low-pass filter is designed to be greater than that of the voltage controller.

In this chapter I have discussed about existing most popular control techniques to get unity power factor input current waveform. They are hysterisis current control and space vector modulation. These techniques are giving results satisfactorily, but they have some drawbacks. By investigation it can be shown that using other and vise verse can rectify one-control technique drawbacks. So a new technique SVM-Based HCC, which reduces switching frequency as well as gives same state space vectors as svm technique has been proposed this chapter and it has explained in detailed.

CHAPTER 5

SIMULATION RESULTS

The High power factor converter applying space vector modulation consists of 3 phase boost rectifier, voltage sensor, current sensor, normaliser circuit, region detector and svm-based hcc switching table execution circuit. The boost rectifier operates in continuous conduction mode. In order to theoretically investigate the performance of the proposed high power factor rectifier (LVHCR) the simulation of the proposed topology was done in MATLAB/ SIMULINK. The simulation parameters were taken as input source voltage is 50V ac, input boost inductor was 5mH, out put load resistance was 10ohm and the output reference dc voltage is varied between 100 to 130V to show the performance of proposed high power factor converter for different operating condition.

5.1: Simulation Results of Experimental Prototype

Case 1: Figures below show the simulation results for the experimental setup providing 110V output voltage, input ac voltage=50v (rms)

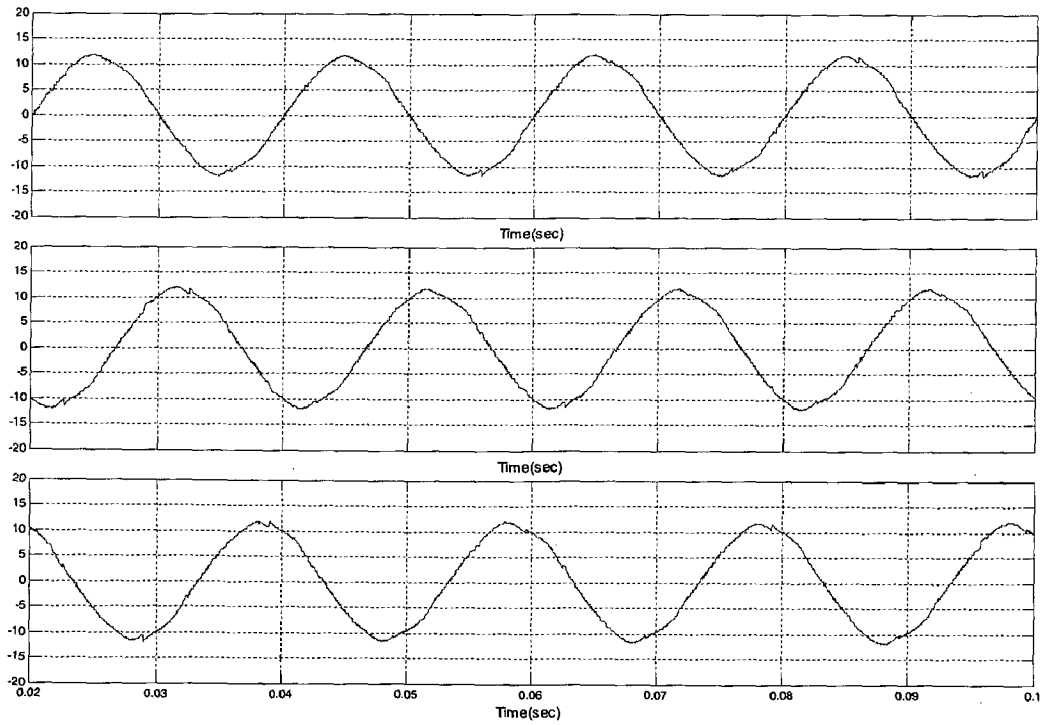


Fig.5.1: 3-phase input current drawn from the supply when V_o = 110V (.02sec/div, 5A/div, 20V/div)

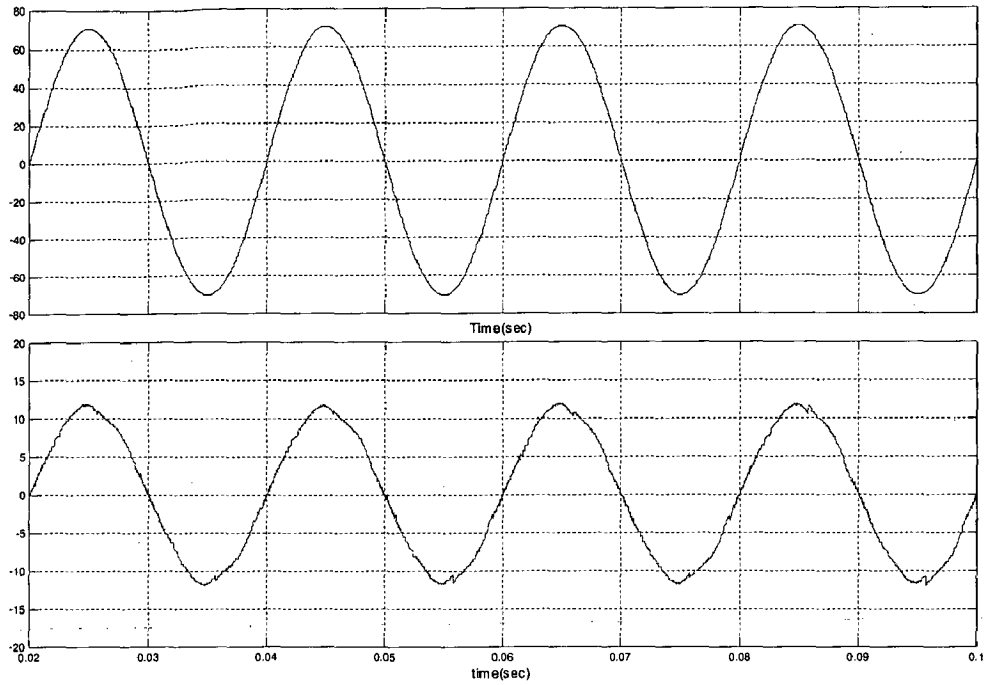


Fig 5.2 Input Voltage and Input Current waveforms

(.02sec/div, 5A/div, 20V/div)

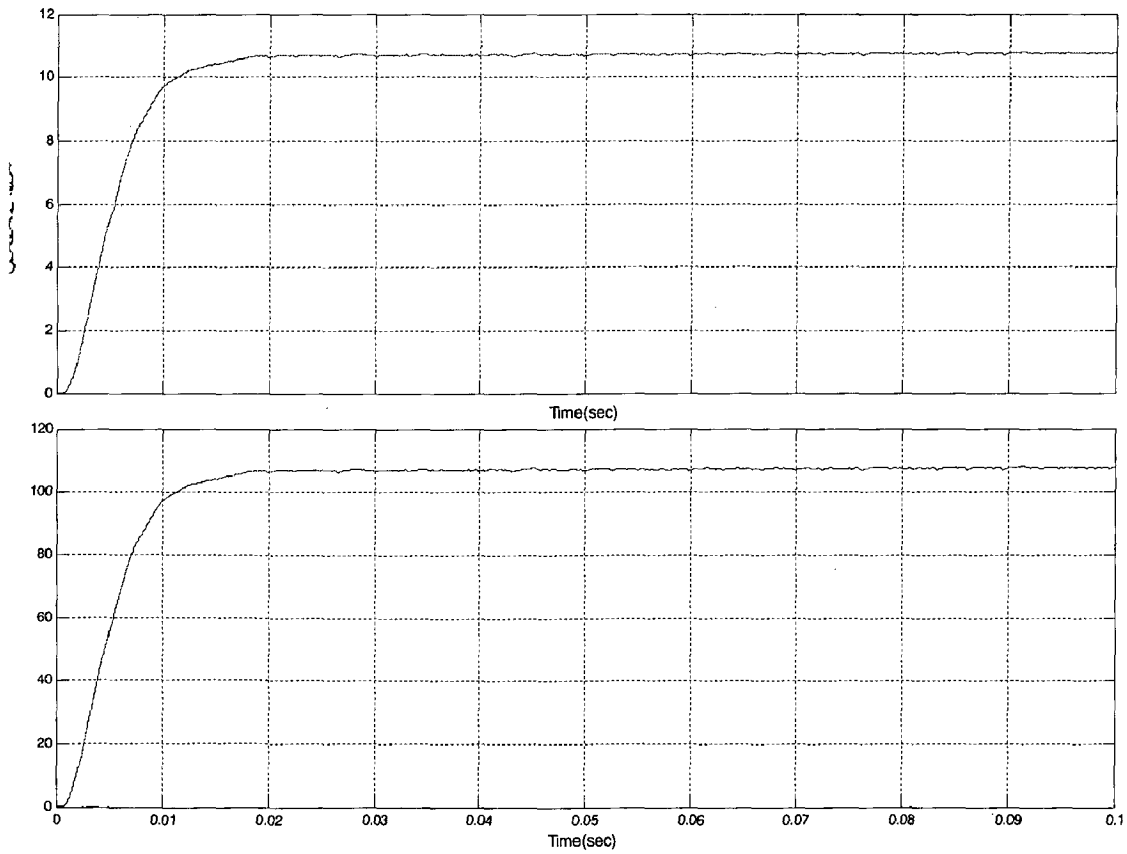


Fig.5.3 Output current, Output voltage wave forms

(.02sec/div, 2A/div, 20V/div)

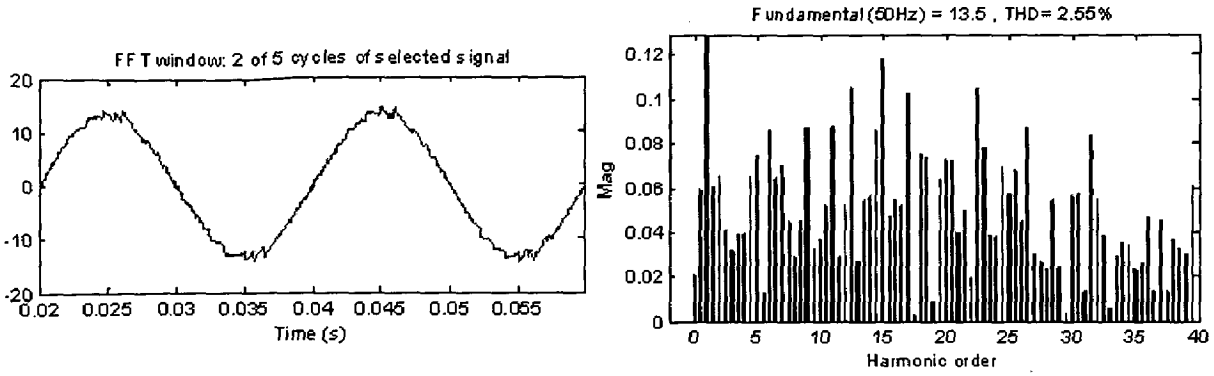


Figure: 5.4: Harmonic Spectrum of Input Current

Figure 5.1) shows the waveforms of 3-phase input currents as drawn from the ac-mains. From the figure 5.1 it is evident that the currents drawn are quite close to sinusoidal thus yielding high power factor. Figure 5.2 shows input voltage and current wave forms of one phase, from this it is clear that the input power factor is unity. Figure 5.3 shows the output voltage and output current waveforms, the dc component of output voltage is 107V which is very close to reference voltage 110V. Figure 5.4 hows harmonic spectrums of input current. The main contributors to the total harmonic distortion (THD) are the 5^{th} and the 7^{th} harmonics. Same explanation can be given for next two cases also.

Case 2 Figures below show the simulation results for the experimental setup providing 120V output voltage, input ac voltage=50v (rms)

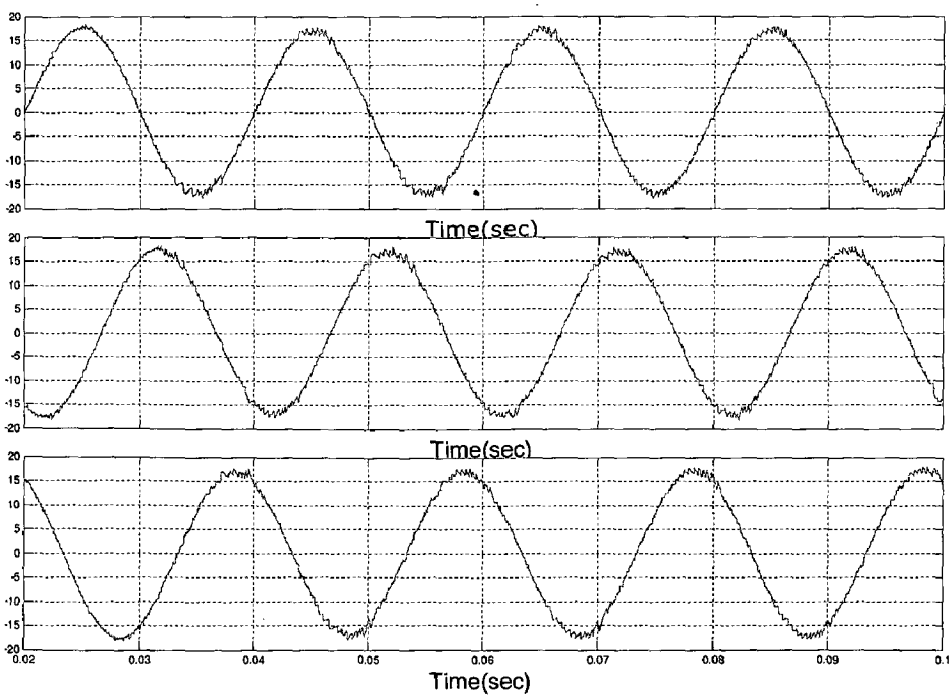


Fig.5.5 3-phase input current drawn from the supply when V_o = 120V (.02sec/div, 5A/div)

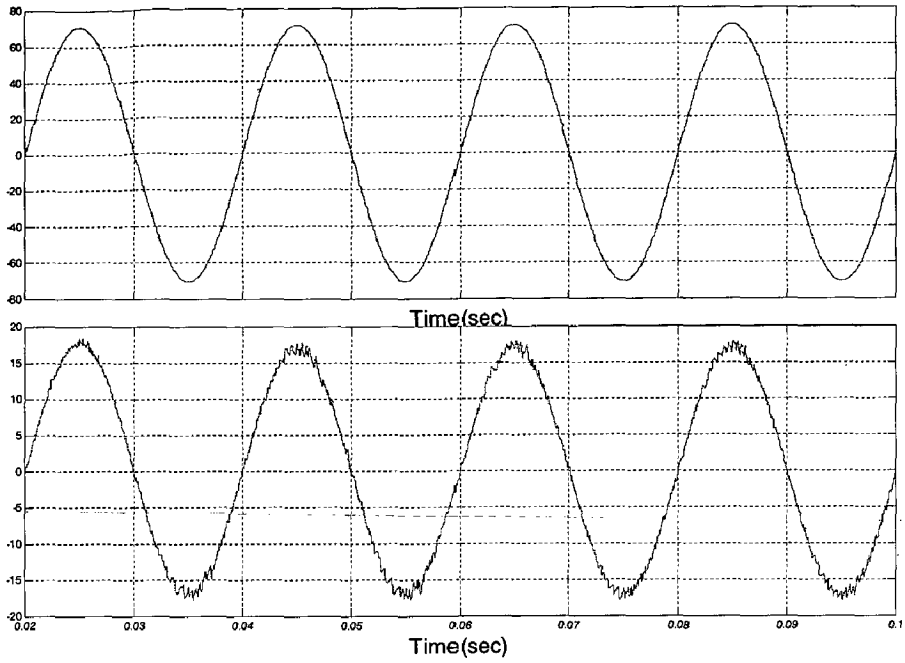


Fig 5.6 Input Voltage and Input Current waveforms

(.02sec/div, 5A/div, 20V/div)

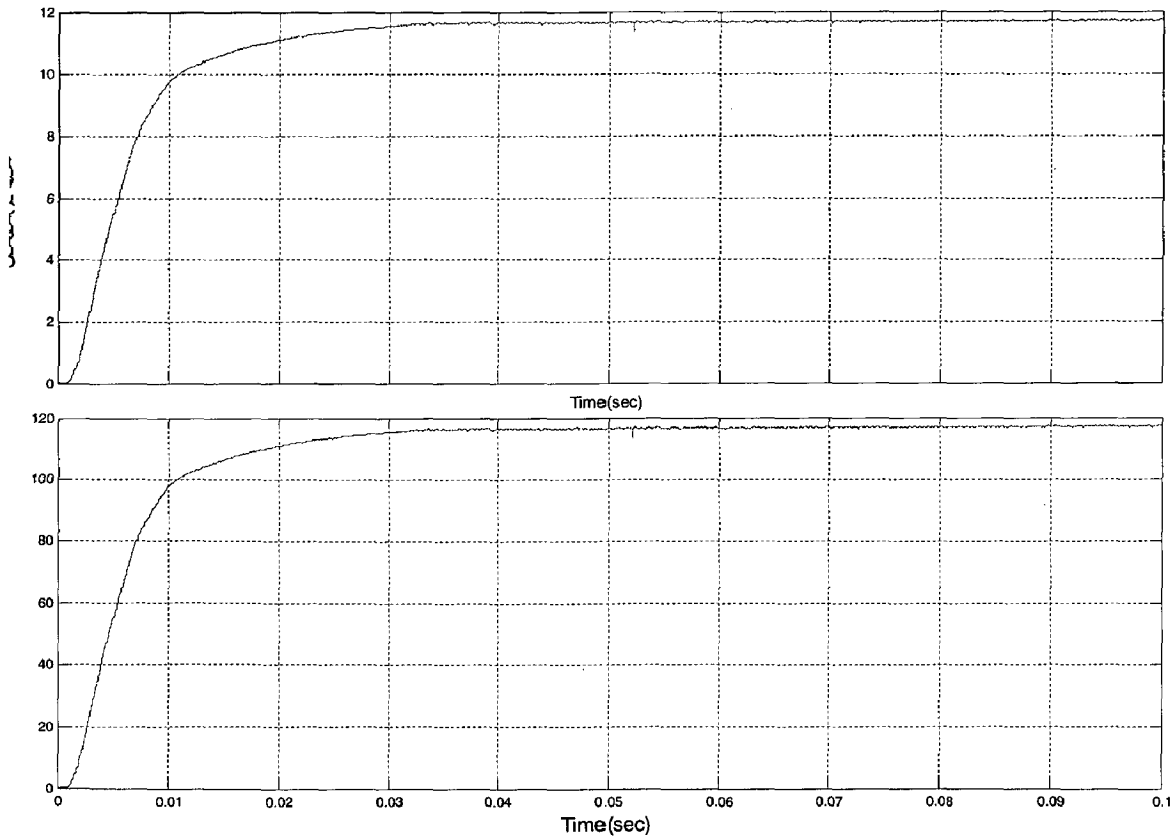


Fig.5.7 Output current, Output voltage wave forms (.02sec/div, 2A/div, 20V/div)

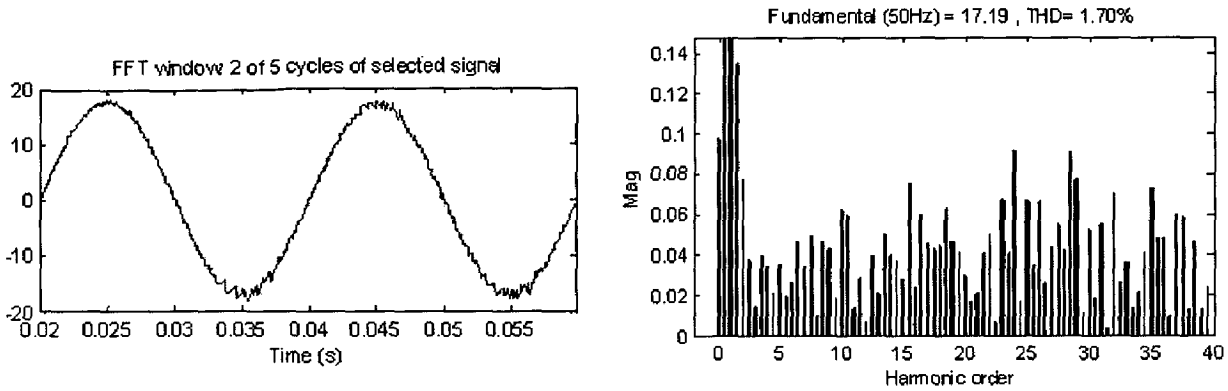


Figure: 5.8: Harmonic Spectrum of Input Current

Case 3 Figures below show the simulation results for the experimental setup providing 130V output voltage, input ac voltage=50v (rms)

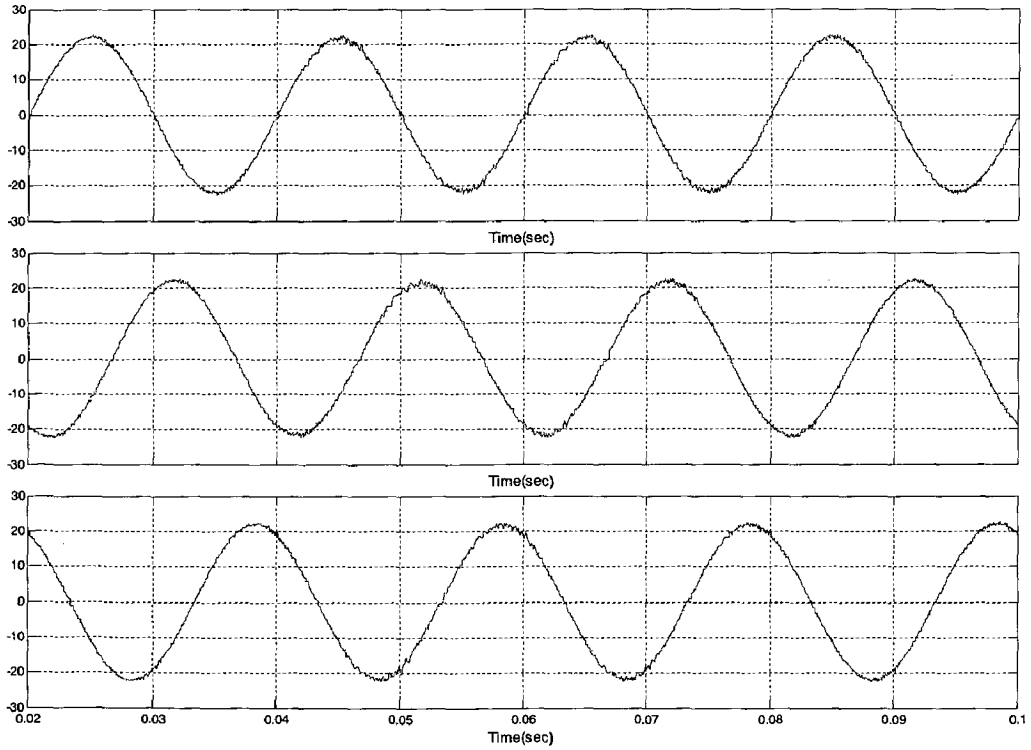


Fig.5.9: 3-phase input current drawn from the supply when V_o = 110V (.02sec/div, 10A/div)

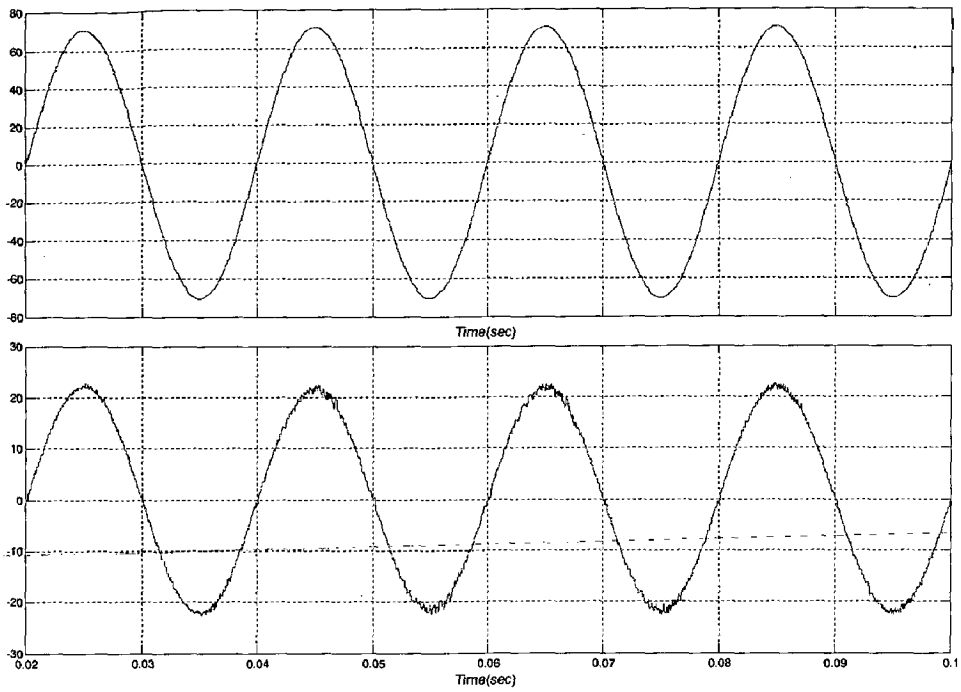


Fig 5.10 Input Voltage and Input Current waveforms

(.02sec/div, 10A/div, 20V/div)

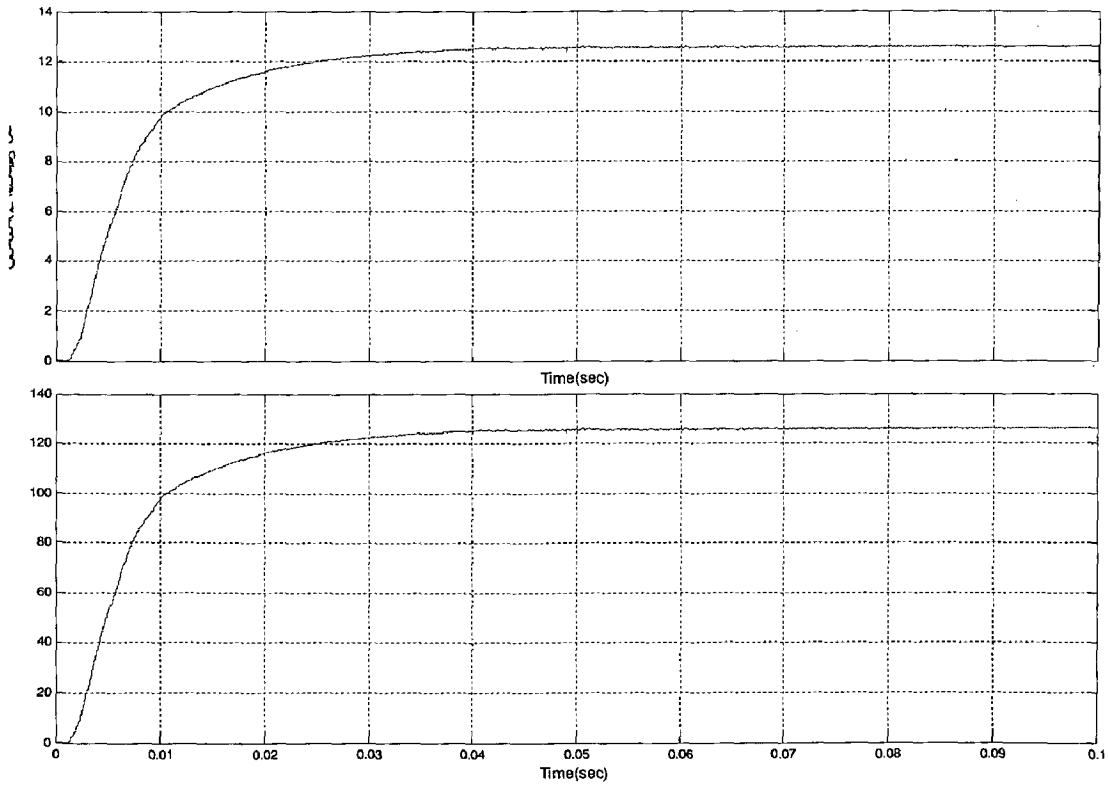


Fig.5.11 Output current, Output voltage wave forms

(.02sec/div, 2A/div, 20V/div)

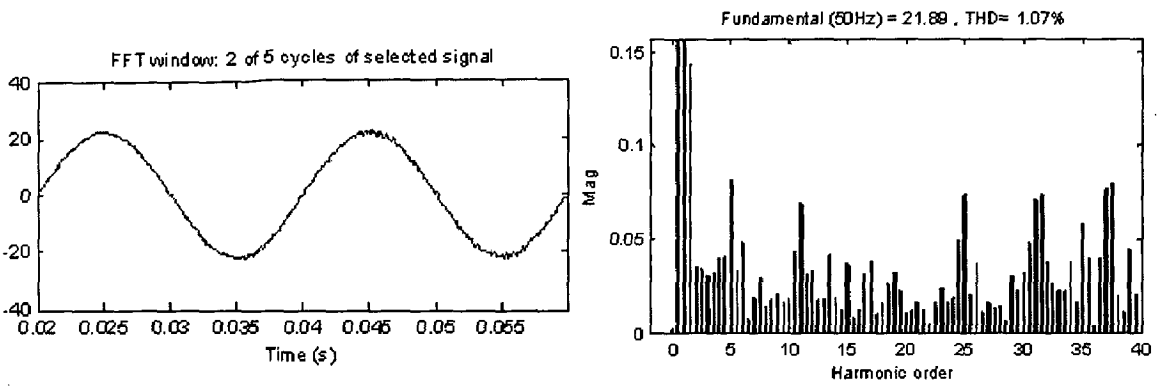


Figure: 5.14: Harmonic Spectrum of Input Current

In simulation the input rms phase voltage applied was of 50v.This voltage applied to boost rectifier, so by considering boost effect output voltage must be 122.45 V. From the simulation results it is clear that whenever output reference voltage approaches this boost voltage, the input current waveform is approximated to sine wave with very low harmonic content(THD is low). From simulation results, it has been shown that whenever output reference voltage equals to 122±. V the harmonic content in input current waveform is increased. However in all the cases the input power factor equals to unity.

Case 4 Step response (100-125V) of the proposed high power factor converter

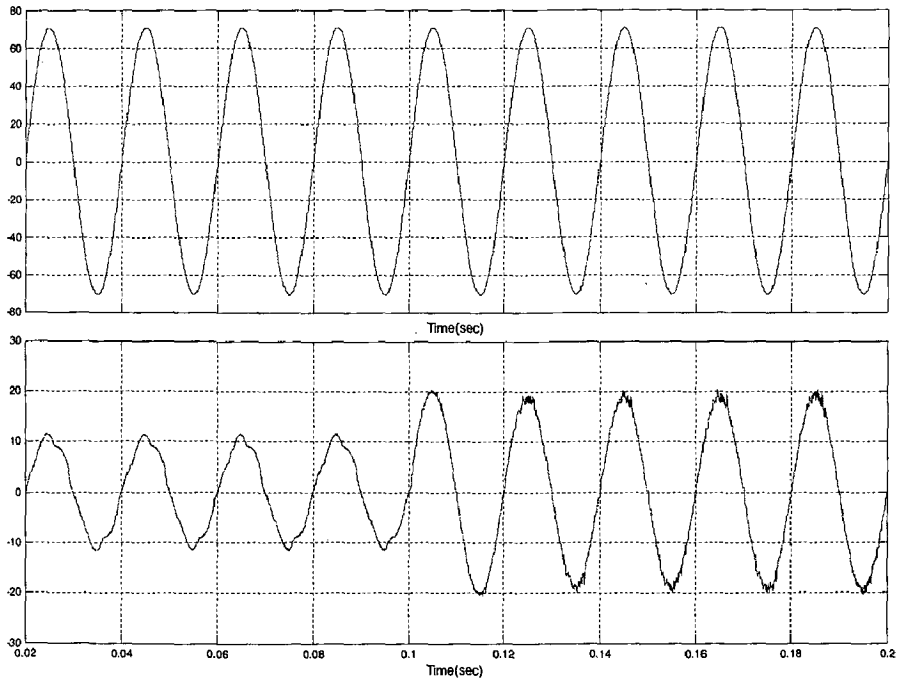


Fig 5.16 Input Voltage and Input Current waveforms (.02sec/div, 10A/div, 20V/div)

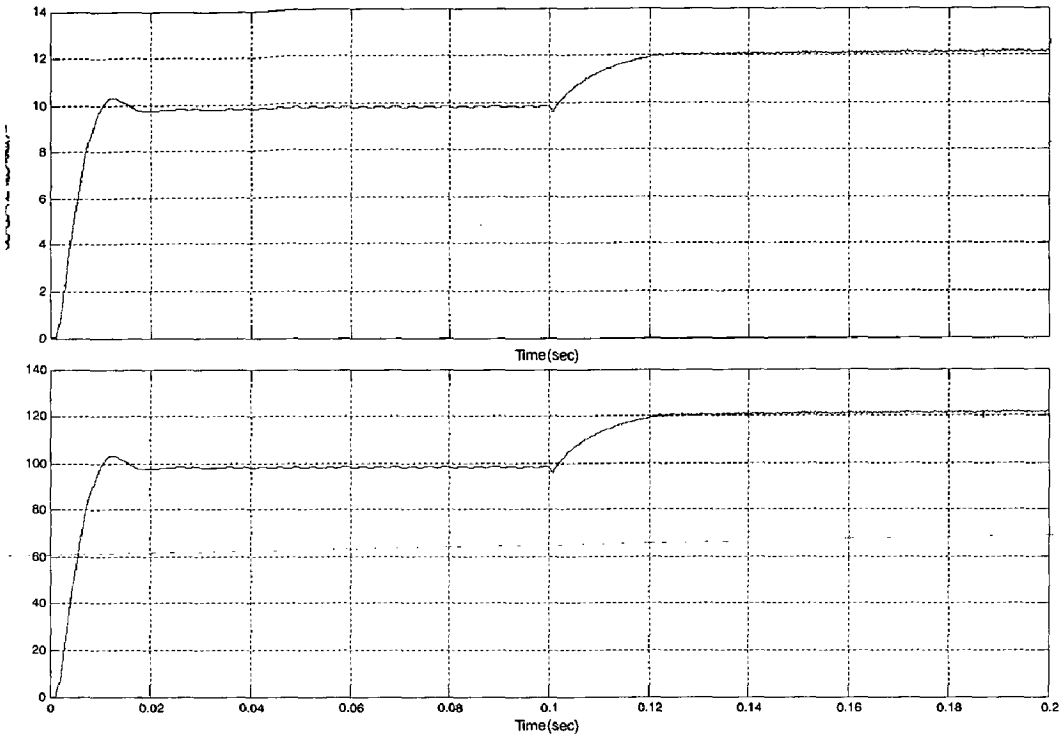


Fig.5.17 Output current, Output voltage wave forms (.02sec/div, 2A/div, 20V/div)

Case 5 Step response (125-100V) of the proposed high power factor converter

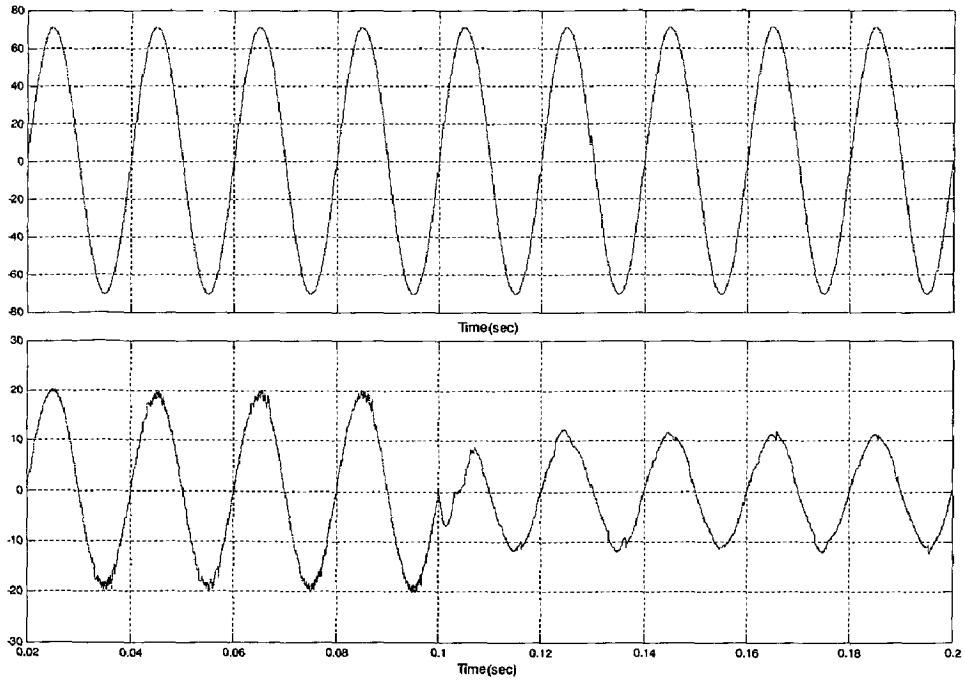


Fig 5.18 Input Voltage and Input Current waveforms (.02sec/div, 10A/div, 20V/div)

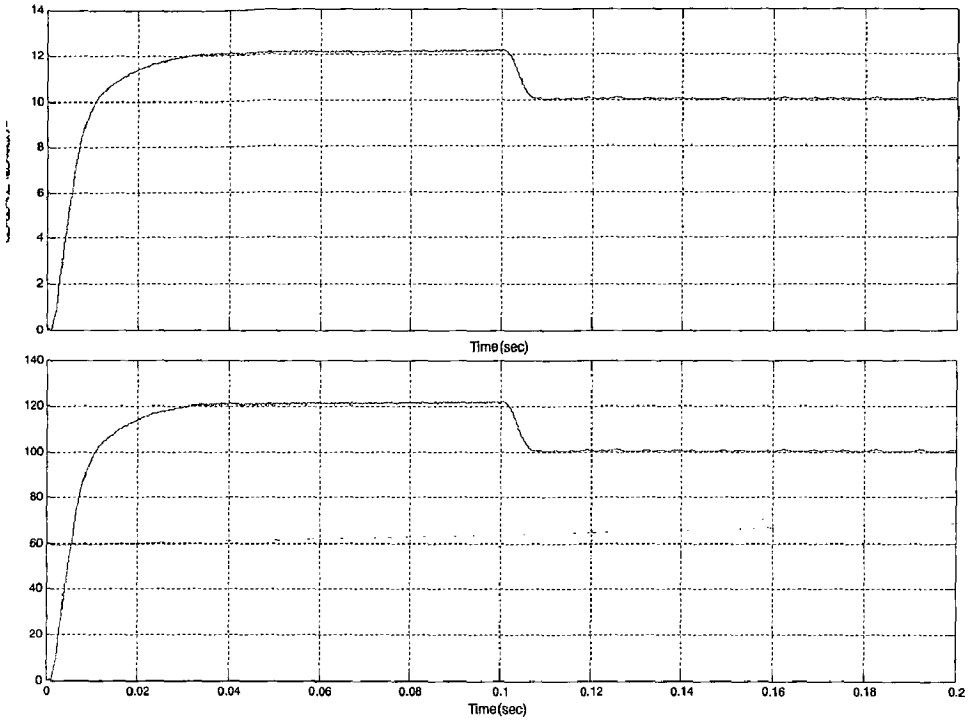


Fig.5.19 Output current, Output voltage wave forms (.02sec/div, 2A/div, 20V/div)

From figures (5.16), (5.17), (5.18), (5.19) it is clear that step response is acceptable for proposed control technique. First two figures shows step response of a converter from 100V out put voltage to step up by 25V. Converter performance under this condition is very much satisfactory. Next two figures shows step response of a converter from 125V out put voltage to step down by 25V. Converter performance under this condition is also very much satisfactory.

In this chapter the simulation results of the proposed high power factor rectifier have been presented. From the results it is evident that the proposed configuration works satisfactorily as high input power factor converter.

CHAPTER 6

SYSTEM DEVELOPMENT

The realization of a high input power factor converter can be divided into two parts

- Hardware development
- Software development

6.1 Hardware development

The system hardware can be divided in the following blocks:

Power circuit

- Pulse amplification and isolation circuit
- AC current measurement circuit
- Power supplies
- Circuit protection
- Reference current waveform generation

6.1.1 POWER CIRCUIT:

Figure6.1 shows the power circuit of the PWM inverter. It consists of six IGBT switches. Each IGBT switch is used in the circuit consists of an inbuilt anti parallel free wheeling diode. No forced commutation circuits are required for IGBTs because these are self commutated devices (they turn on when the gate signal is high and turn of when the gate signal is low). An RCD (resistor, capacitor and diode) turn-off circuit is connected to protect the circuit against high dv/dt and is protected against power voltage by connecting MOV (Metal Oxide Varistor).

Insulated gate bipolar transistors (IGBT's) are widely used in switching power conversion applications because of their distinctive advantages, such as easiness in drive and high frequency switching capability. The performance of IGBT's has been continuously improved, and the latest IGBT's can be operated at 10–20 KHz without including any snubber circuit. Moreover, IGBT's are replacing MOSFET's for the several or several tens of kilowatts power range applications since IGBT's can handle higher voltage and power with higher power density and lower cost compared to

MOSFET's. The maximum operating frequency of IGBT's, however, is limited to 20-30 KHz [1] because of their tail-current characteristic. To operate IGBT's at high switching frequencies, it is required to reduce the turn-off switching loss. Zero-voltage switching (ZVS) with a substantial external snubber capacitor or zero current switching (ZCS) can be a solution. The ZCS, however, is deemed more effective since the minority carrier is swept out before turning off [6].

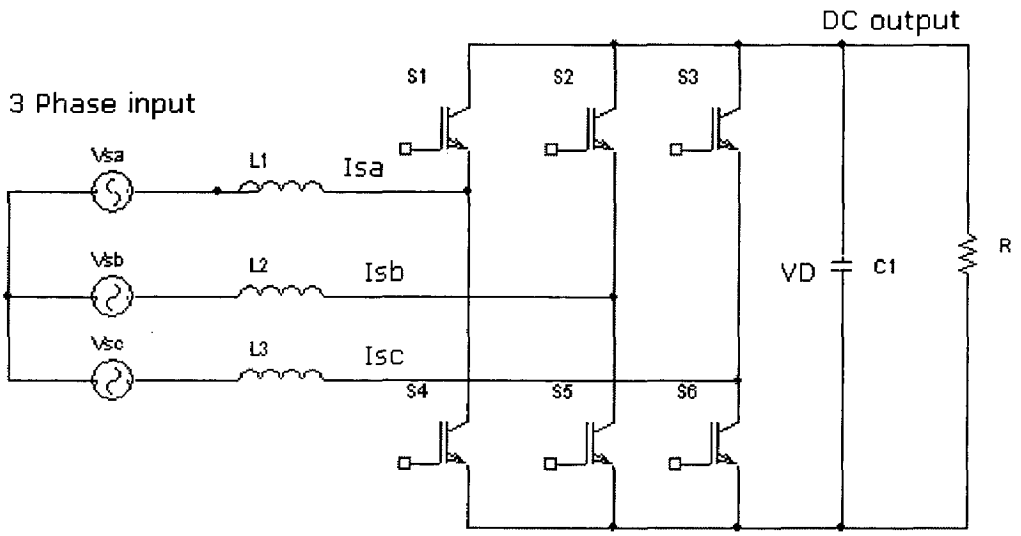


Figure 6.1: PWM rectifier with voltage link.

6.1.2 Pulse Amplification and Isolation Circuit:

The pulse amplification and isolation circuit for IGBT is shown in figure 9 .The opto-coupler (MCT-2E) provides the necessary isolation between the low voltage isolation circuit and high voltage power circuit .The pulse amplification is provided by the output amplifier transistor 2N222.

When the input gating pulse is at +5V level, the transistor saturates, the LED conducts and the light emitted by it falls on the base of phototransistor, thus forming its base drive. The output transistor thus receive no base drive and, therefore remains in cut-off state and a +12 v pulse (amplified) appears across it's collector terminal (w.r.t.ground). When the input gating pulse reaches the ground level (0V), the input

switching transistor goes into the cut-off state and LED remains off, thus emitting no light and therefore a photo transistor of the opto-coupler receives no base drive and, therefore remains in cut-off state .A sufficient base drive now applies across the base of the output amplifier transistor .it goes into the saturation state and hence the output falls to ground level. Therefore circuit provides proper amplification and isolation. Further, since slightest spike above 20v can damage the IGBT, a 12 V zener diode IC connected across the output of isolation circuit .It clamps the triggering voltage at 12 V.

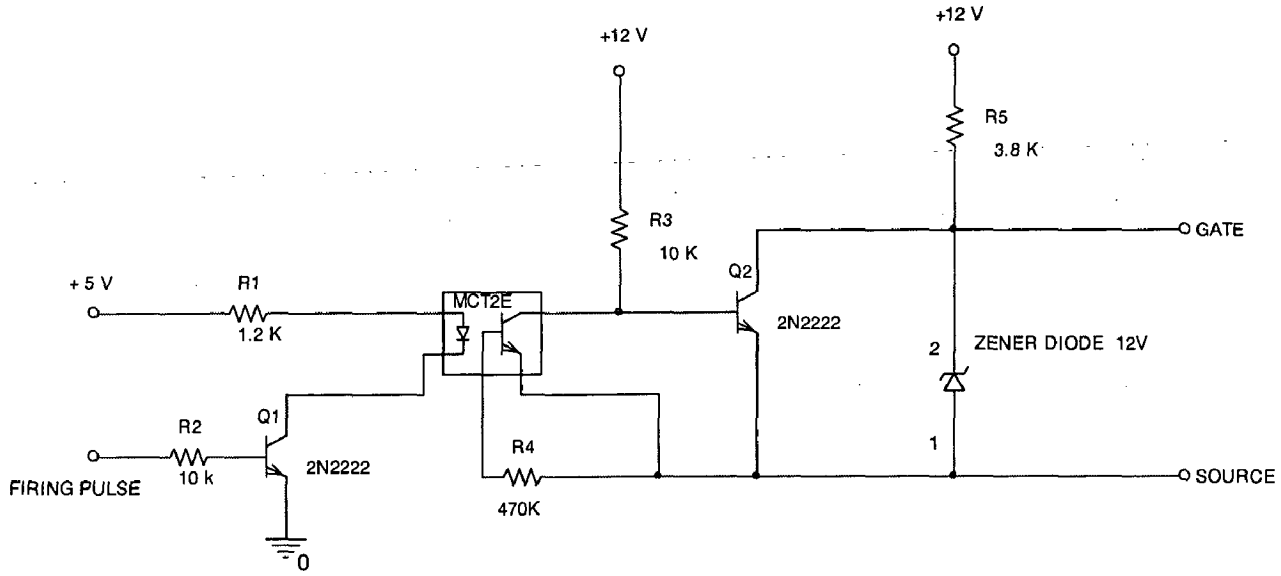


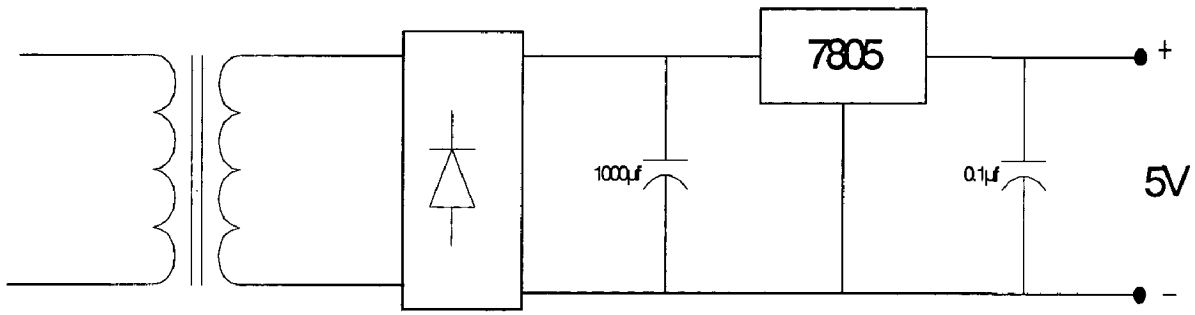
Figure 6.2: PULSE AMPLIFICATION AND ISOLATION CITCUIT

6.1.3 POWER SUPPLIES

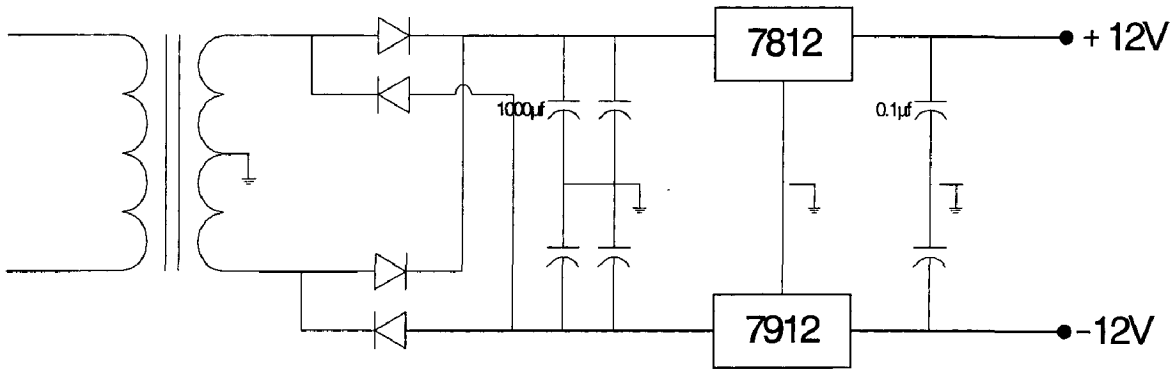
D.C regulated power supplies (±12 V and +5 V) are required for providing the biasing to various ICs, etc. the system development has in-built power supplies for this purpose. The circuit diagram for various dc regulated power supplies are shown in figure 10. As, shown the single phase AC voltage is stepped down and the rectified using diode bridge rectifier. A capacitor of 1000microfarad, 50V is connected at the output of the bridge rectifier for smoothing out the ripples in the rectified dc voltage of each supply. IC voltage regulated chips, 7812, 7912,7805 are used for obtaining the dc-regulated voltages. A capacitor of 0.1microfarad, 50 V is connected at the output of the IC voltage regulator of each supply for obtaining the constant, ripple-free dc voltage.

DC VOLTAGE	IC REGULATOR
+5V	7805 (TO-3)
+12V	7812 (TO-3)
±12V	7812 (220Type), 7912 (220Type)

Table.6.1



(a)



(b)

Figure 6.3: Power supplies (a) +5V supply (b) ±12V supply

6.1.4 Circuit Protection

(A) Snubber Circuit for IGBT protection

IGBTs are increasingly the switch of the choice for pwm rectifiers for used in power electronics application, because of hard switching applications and lower conduction losses. Most of the IGBTs are used in hard switching applications up to 20 kHz, beyond that switching losses in IGBTs becomes very significant.

Switching such high currents in short time gives rise to voltage transients that could exceed the rating of IGBT especially if the bus voltage is close to the IGBT's rating. Snubbers are therefore needed to protect the switch from transients. Snubber circuit for IGBT as shown in Figure

Snubbers are employed to:

- Limit di/dt or dv/dt.
- Transfer power dissipation from the switch to a resistor.
- Reduce total switched losses.

RCD snubbers are typically used in high current application. The operation of RCD snubber is as fallows: The turn-off makes the voltage zero at the instant the IGBT turn-off. At turn-off, the device current is transfer through the diode D_s and the voltage across the device builds up. At the turn-on, the capacitor C_s discharges through the resistor R_s. The capacitor energy is dissipated in the resistor R_s at turn-on.

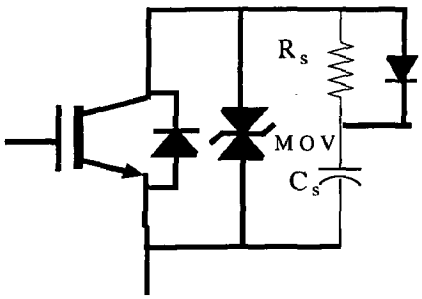


Figure6.4. **Snubber circuit of IGBT**

(B) **Over voltage protection**

An additional protective device Metal-oxide-varistor (MOV) is used across each device to provide protection against the over voltages. MOV acts as a back-to-back zener and bypass the transient over voltage across the device. In general the voltage rating of MOV is kept equal are below the rating of IGBT to protect it from the over voltages.

(C) **Over heating protection**

Due to the ohmic resistance of IGBT and anti - parallel diode, I^2 R loss takes place as a result of the current conduction, which results the heat generation, thus raising the device temperature, this may be large enough to destroy the device. To keep device temperature within the permissible limits, all IGBTs are mounted on aluminum heat sink and is then dissipated to the atmosphere.

(D) Short circuit protection

The thermal capacity of semiconductor device is small. A surge current due to a short circuit may rise device temperature much above its permissible temperature rise limit which may instantaneously damage the device. Hence, the short circuit protection is provided by fast acting fuses in series with each supply line.

6.5 Current Sensor Circuit

Closed loop Hall Effect current transducer is used to sense the current. The transducer use the ampere turn compensation method to enable the measurement of current from DC to high frequency with an ability to follow rapidly changing level or wave shapes. The application of primary current (Ip) causes a change in flux in the air gap. This in turn produces a change in output from hall element away from the steady state condition. This output is amplified to produce a current (Is), which is passed through a secondary winding causing a magnetizing force to oppose that of the primary current, thereby reducing the air gap flux. The secondary current is increased until the flux is reduced to zero. At this point the hall element output will return increased until the flux is reduced to zero. At this point the hall element output will return to steady state condition and the ampere-turn product of secondary circuit will match that of primary. The scaling

of the current measurement is such that for 1 amp current at the input of the circuit their will be 1 volt voltage at the output of the circuit.

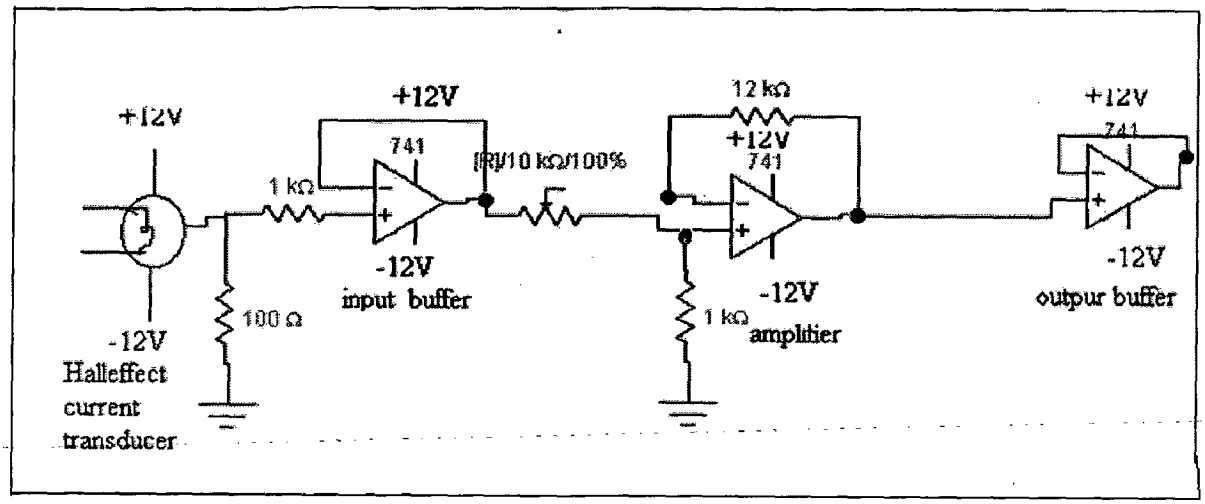


Figure 6.5: Current sensor circuit

The current that passes through the secondary winding is the output current. The transformation ratio is calculated by the standard current transformation equation

$$N_pI_p=N_sI_s$$

Where

N_p= primary current, Ns= secondary current

I_p= primary current, Is = secondary current.

6.1.6 control circuit:

Three hysteresis comparators are used to track the current command vector and limit the current error within the specified bound. B_a denotes a status of the bound of the *a*-axis current error. The state space vectors $\mathbf{V}_0$, $\mathbf{V}_1$, and $\mathbf{V}_2$ in Region I are utilized like the SVM technique as shown in figure 4.5(*b*). When the current error of the *a*-axis hits the upper bound of the hysteresis comparator and the current error of the *b*-axis hits the lower bound, B_a= 1 and B_b= 0. The voltage vector $\mathbf{V}_1$ is applied to increase the *b*-axis current i_b and *c* axis current *ic* simultaneously when B_b= 1 and B_c= 1.

On the other hand, $\mathbf{V}_2$ is applied to decrease i_a and i_b simultaneously when B_a= 0 and B_b= 0. In the other cases, the zero vector $\mathbf{V}_0$ is applied. The switching table for all regions is shown in table 4.1. Figure 6.6 shows the control circuit for the proposed

current controller. The gate logic of the programmable array logic (PAL) device is designed using EPROM

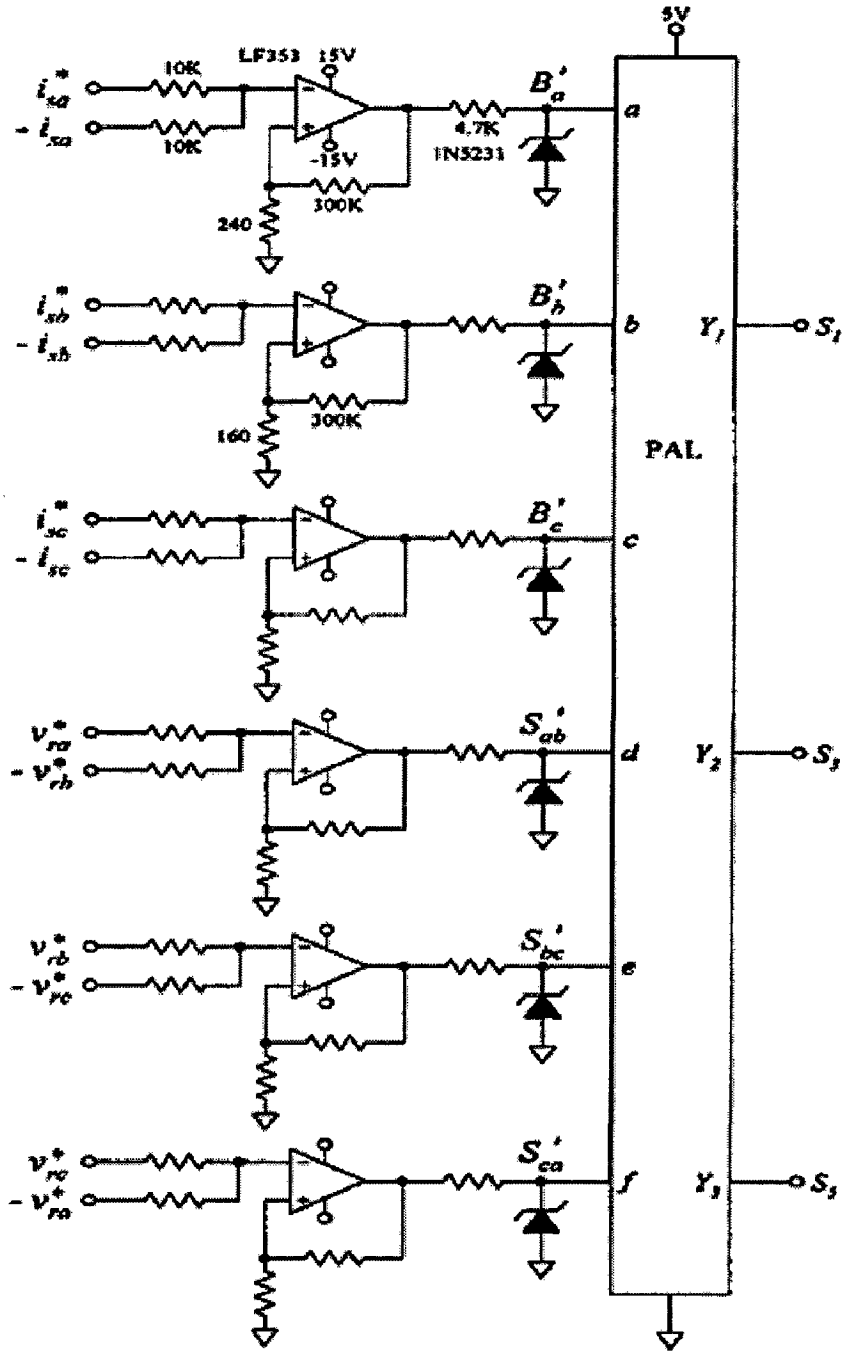


Figure6.6 Control circuit for the proposed current controller.

6.1.7 Generation of Reference Current:

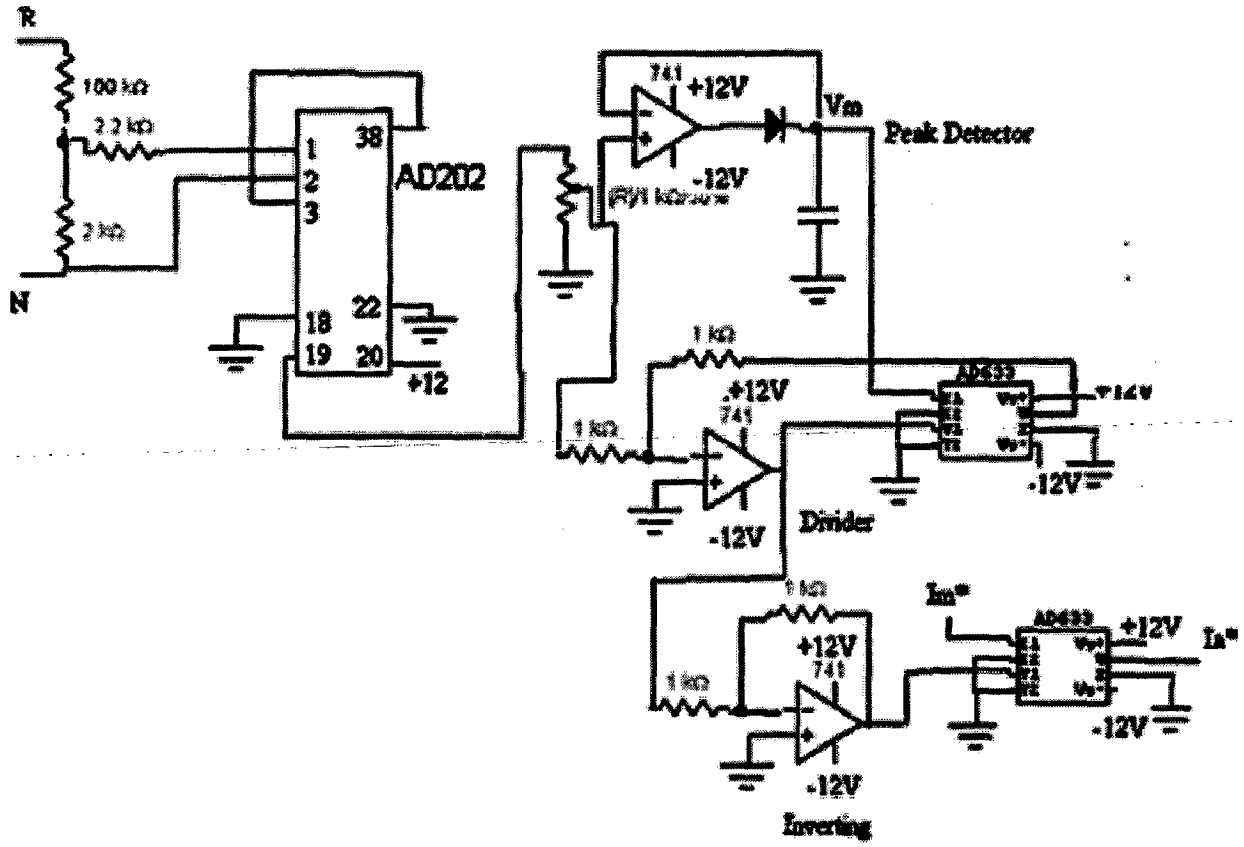


Figure6.7: current reference circuit

The peak amplitude wave and rectified wave is obtained by using isolation amplifier AD202, which provides isolation between the output and input stages through the use of internal transformer coupling. The divider circuit divides the rectified wave with peak amplitude of the wave. The output of divider circuit is negative in nature and hence it is inverted with the help of inverting circuit. Now the output is a unit-rectified signal. This unit rectified signal is now multiplied with the peak reference current value by making use of IC AD633 which gives us reference current I_a^*.The scaling for AD202 isolation amplifier was adjusted as for 10V input, their will be 1V output.

6.2 Software development

Pc Interfacing And Control

Pentium 80486 Processor based PC with clock frequency 2 MHz along with the Timer I/O card and ADC has been used for this application. This card provides two 8255 each having three I/O ports A, B, C.. The card has two timer chips 8253-1 and 8253-2. Each chip has three counters out of which TIMER2_1, TIMER2_2 from 8253-2 have been used to generate time delays. TIMER2_1 from 8253-2 has been used to generate 1ms interrupt. 2MHz clock from this card has been used as clock signal to all counters. Four bits from PORTC are being used as GATES of four counters. The interrupt used is IR3. The source code has been written in 'C' language.

The ACl-8316 data acquisition card was used to read two voltages and two currents from hardware setup and to send two voltages out. The software part was used to generate reference voltages for region detection in space vector modulation. This reference voltage V^* is given as $V^*==V_s - Ldi_s^*/dt$ where V_s is input voltage and i_s^* is reference current.

The formula between A/D data and analog value is

$$Voltage = AD\_data \times \frac{1}{K} \times \frac{10}{gain}$$

Where gain is the value of A/D gain control register. The K is a coefficient and is equal to 32767. Input is 16 bit .

The formula between analog value and A/D data is

$$V_{out} = -V_{ref} \times \frac{DAn}{4096}$$

Where V_{ref} is reference voltage, the V_{out} is output voltage, and the DAn is the digital value in D/A registers. Output is 12 bit.

Implementation of reference voltage generation though pc:

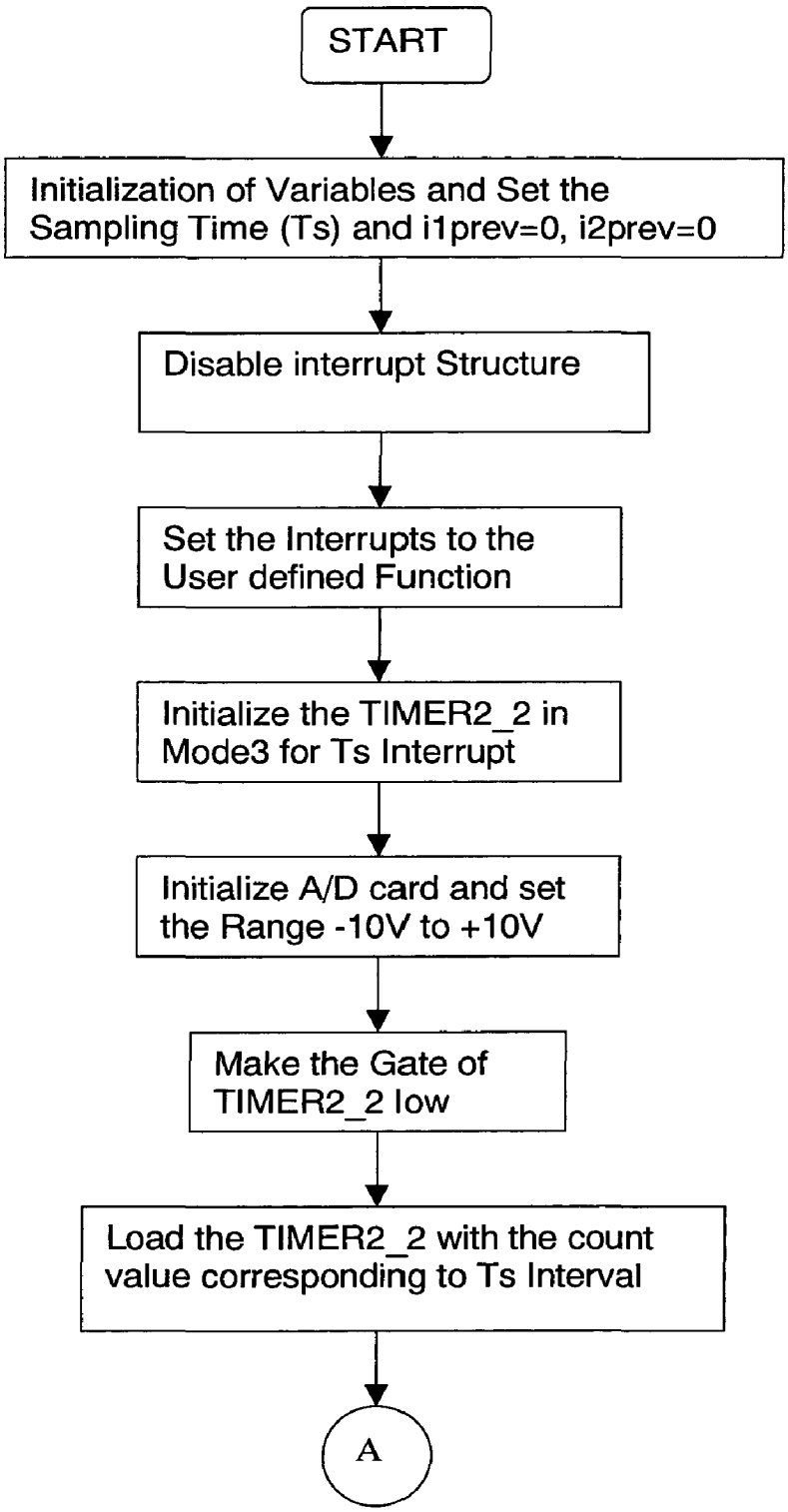
The complete Software for implementation of reference voltage generation is divided into following modules. Each module is explained briefly with the flowcharts given below.

- Main_Programe.

- SAMPLING_ISR Interrupt Service Subroutine.

The flow chart for the Main_Program is given in Fig 6.8. Program starts with the initialization of local variables, global variables, I/0 ports, AD card and 8253. Load the master timer (TIMER2_2) with the count value corresponding to Ts. After that wait for the interrupt to come. Same process is repeated until any key presses to stop the programme.

The Flowcharts for the SAMPLING_ISR module is given in fig 6.9. Program starts with the initialization of channel no to zero, then select a channel to read the data, then give start of conversion signal after conversion read the data and store it, repeat same procedure 4 times to read 4 channels. Calculate the V_{1act} and V_{2act} as per the equation given in 4.13. Send V_{1act} and V_{2act} out though 2 output channels, repeat same when ever interrupt comes.


START
Initialization of Variables and Set the Sampling Time (Ts) and i1prev=0, i2prev=0
Disable interrupt Structure
Set the Interrupts to the User defined Function
Initialize the TIMER2_2 in Mode3 for Ts Interrupt
Initialize A/D card and set the Range -10V to +10V
Make the Gate of TIMER2_2 low
Load the TIMER2_2 with the count value corresponding to Ts Interval
A

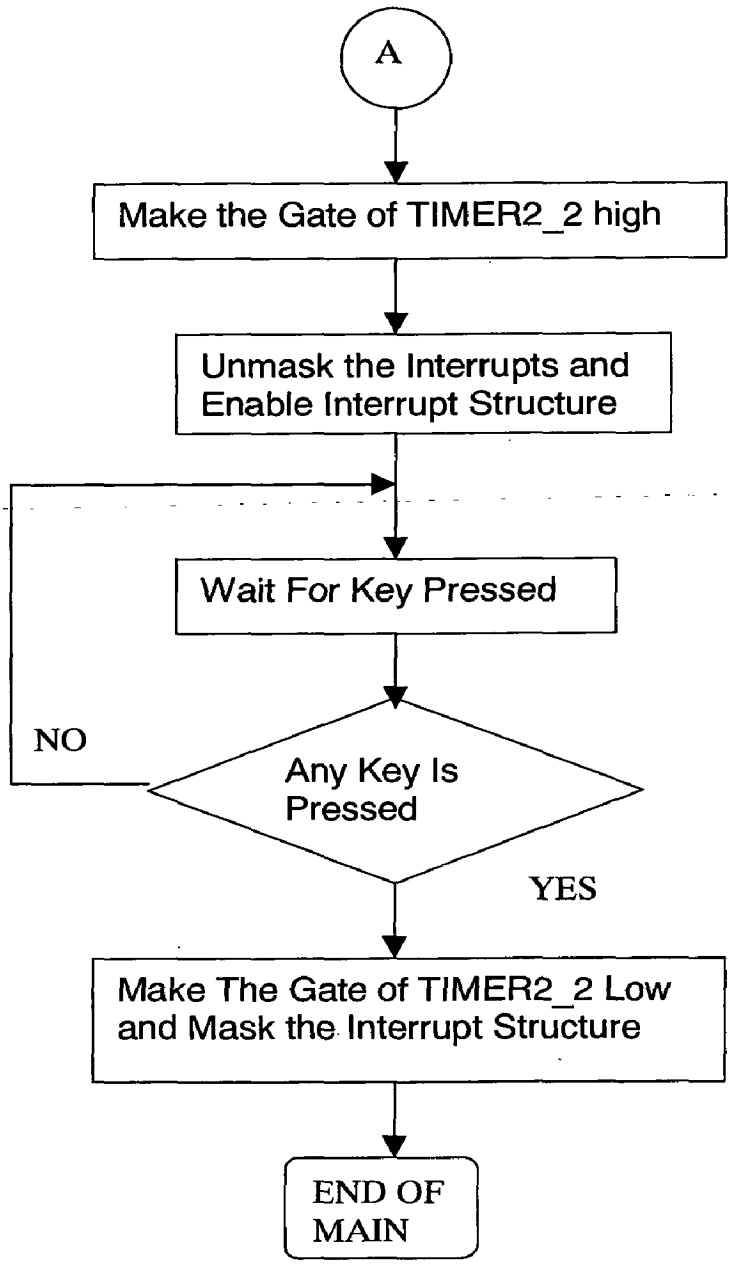
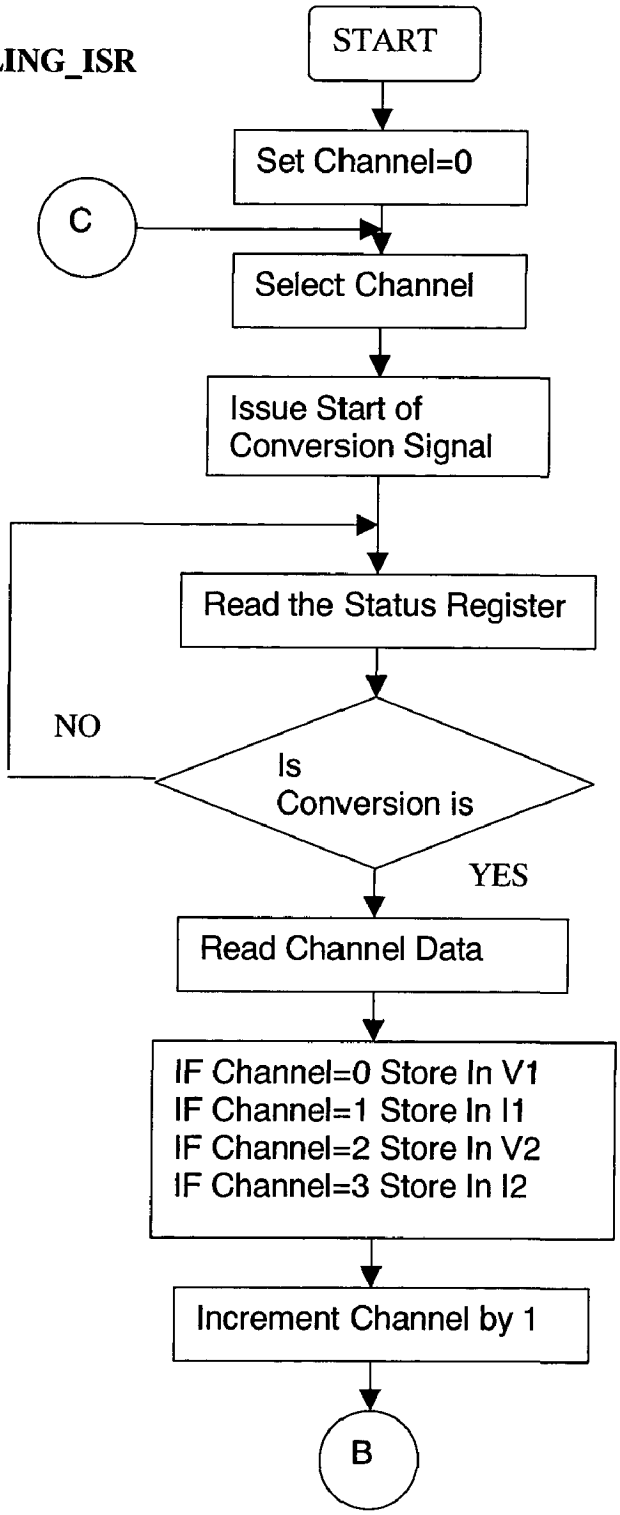


Fig. 6.8 Flow Chart for Main Programme

SAMPLING_ISR



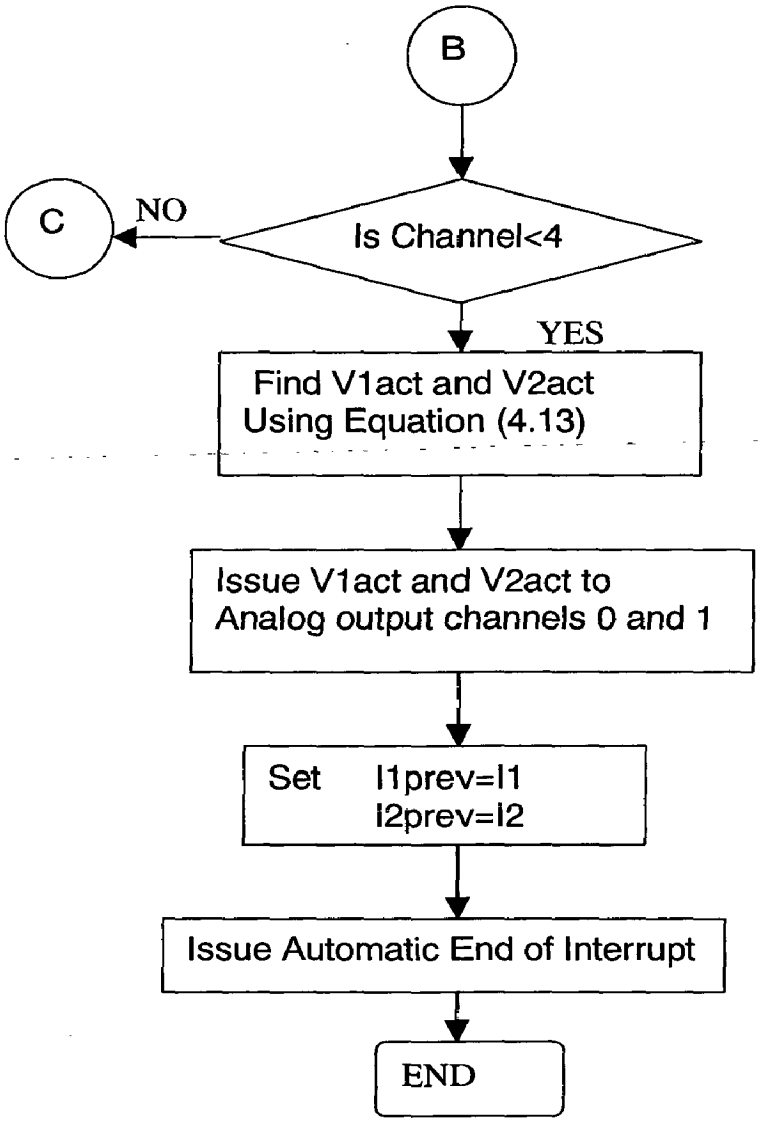


Fig.6.9 Flow Chart For sampling_ISR subroutine

CHAPTER 7

EXPERMENTAL RESULTS

The High input power factor converter applying space vector modulation consists of 3 phase boost rectifier, voltage sensor, current sensor, normaliser circuit, region detector and svm-based hcc switching table execution circuit. 3 phase boost rectifier is one whose output is always greater than input source voltage. A new topology SVM-Based HCC which combines advantages of both space vector modulation and hysterisis current control and rectifies drawbacks of both topologies have been explained in previous chapter. New on this chapter let us discuss about how is it's performance experimentally under open loop. In this chapter the results of the experimentation carried on High input power factor converter are presented.

Specifications

- Filter inductor = 6mH
- Output resistance =50.
- Output capacitor =2200μF, 450V dc

Reference current generation

The reference current for hysterisis current control operation is generated by multiplying dc reference voltages with the unit sine wave vectors which are in phase with the source voltages, and which are generated by using AD 202 isolation amplifier and AD633 multipliers and this circuit has already explained in previous chapter. These references current are shown in fig. 7.1. These reference currents are of sinusoidal waveform and are in phase difference of 120 degrees. These reference currents are in phase with their respective source voltage waveform. This shows this circuit is working satisfactorily.

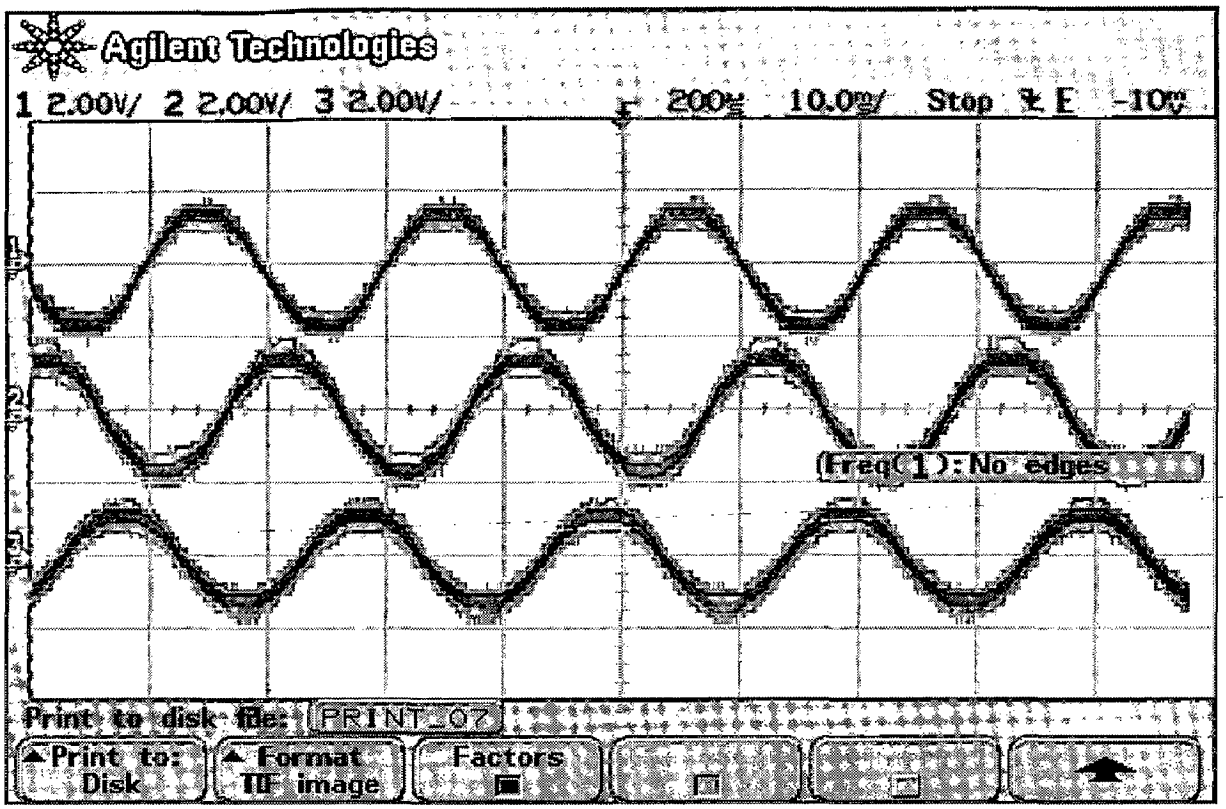


Fig. 7.1 Reference current wave forms (10ms/div, 2V/div)

Reference voltage generation

Reference voltage is generated by interfacing hardware and software circuits. These voltages have been generating by using the data acquisition card. The input voltage vectors V_R , V_Y , i_R^* and i_Y^* are sensed though 4 input channels of the data acquisition card. These voltages and currents are continuously sensed each time whenever an interrupt comes at a sampling period T_S By using these voltages, currents and sampling time reference voltages can be generated according to eq. 4.13. The waveforms of reference voltages are shown in fig.7.2. These reference voltages are of sinusoidal waveform and are in phase difference of 120 degrees. This shows this circuit is working satisfactorily.

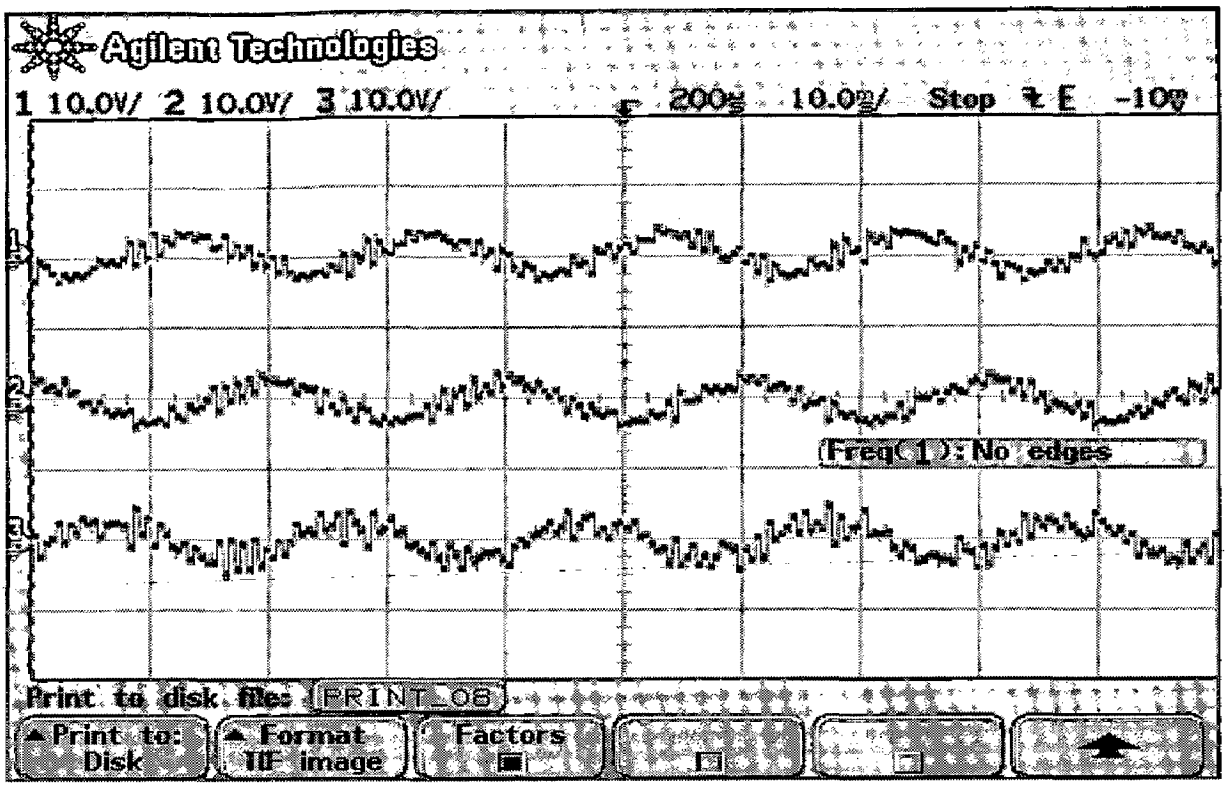


Fig.7.2 Reference voltage wave forms (10ms, 10v)

Now after generating reference currents for hysterisis current control and reference voltages for region detection in space vector modulation. We discuss the performance of high input power factor converter experimentally under various operating conditions explained in the form of different cases. In each case input voltage, input current and output voltage waveforms are recorded. I have shown all these waveforms under various cases, which are recorded under open loop operation of 3-phase boost converter

Waveforms for

Case 1)

Input source voltage = 10V

Output resistance = 50.

Reference current = 3.5V

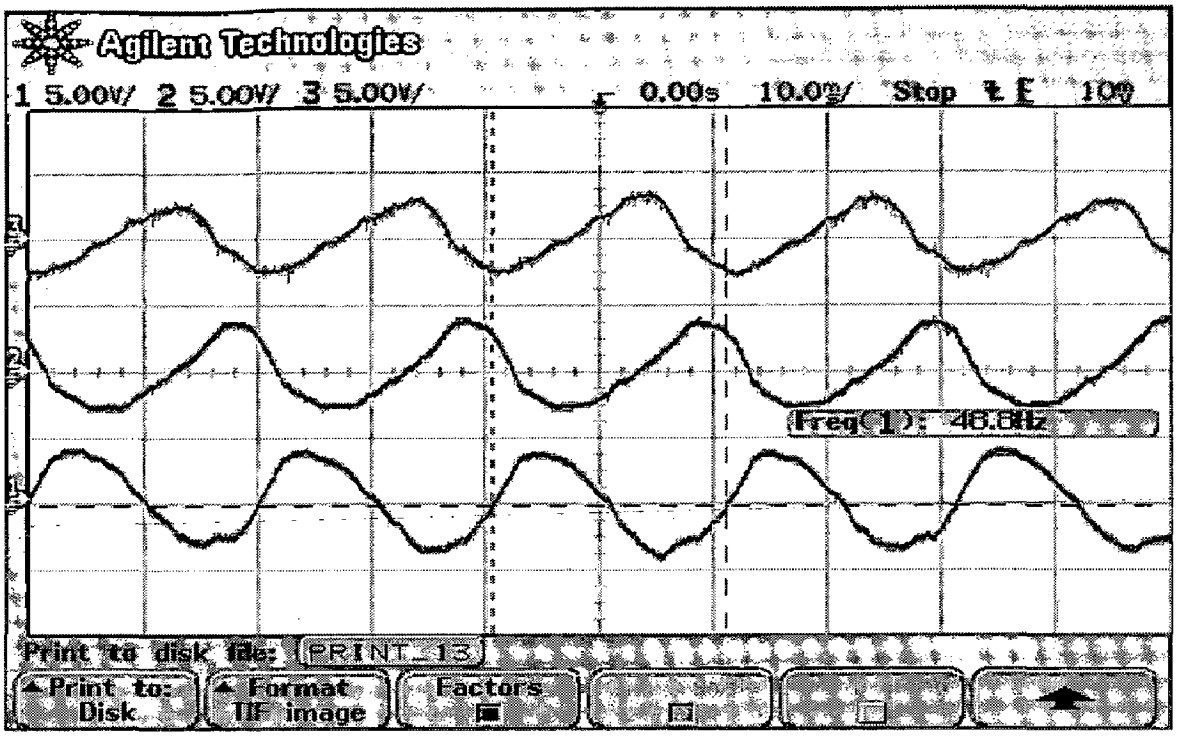


Fig.7.3 Input line currents (10ms/div, 5V/div)

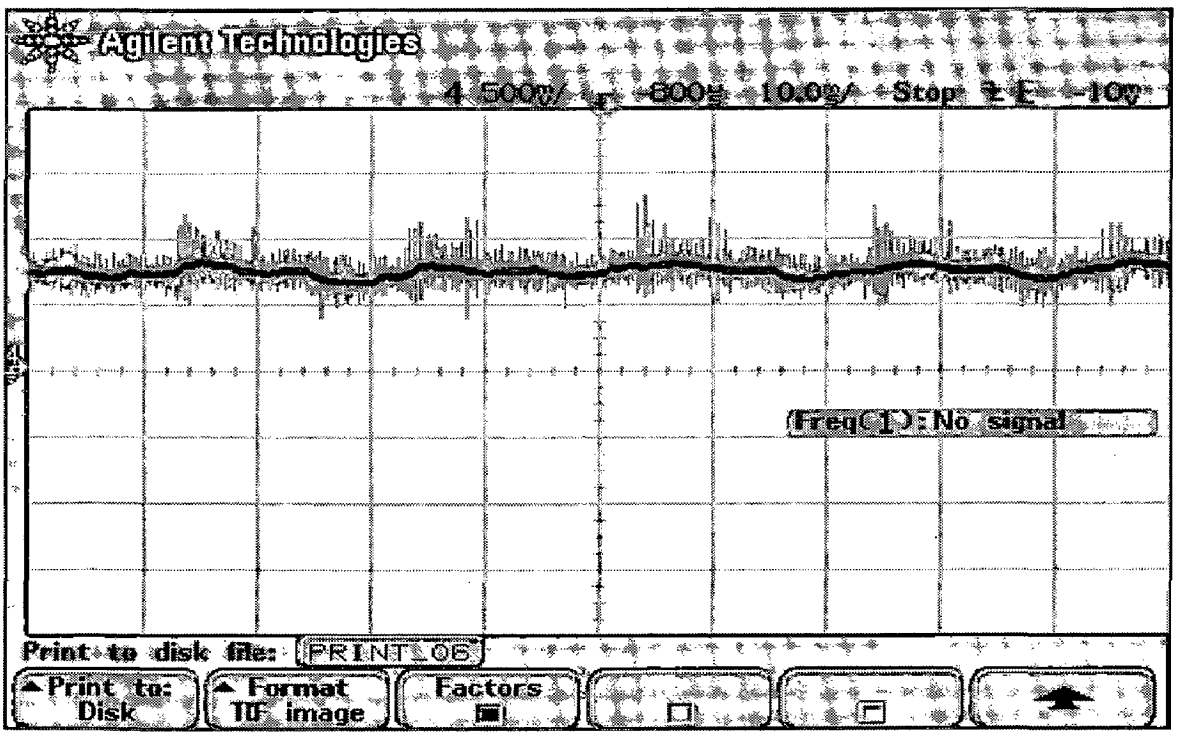


Fig. 7.4 Output Voltage (10ms/div, .5V/div)

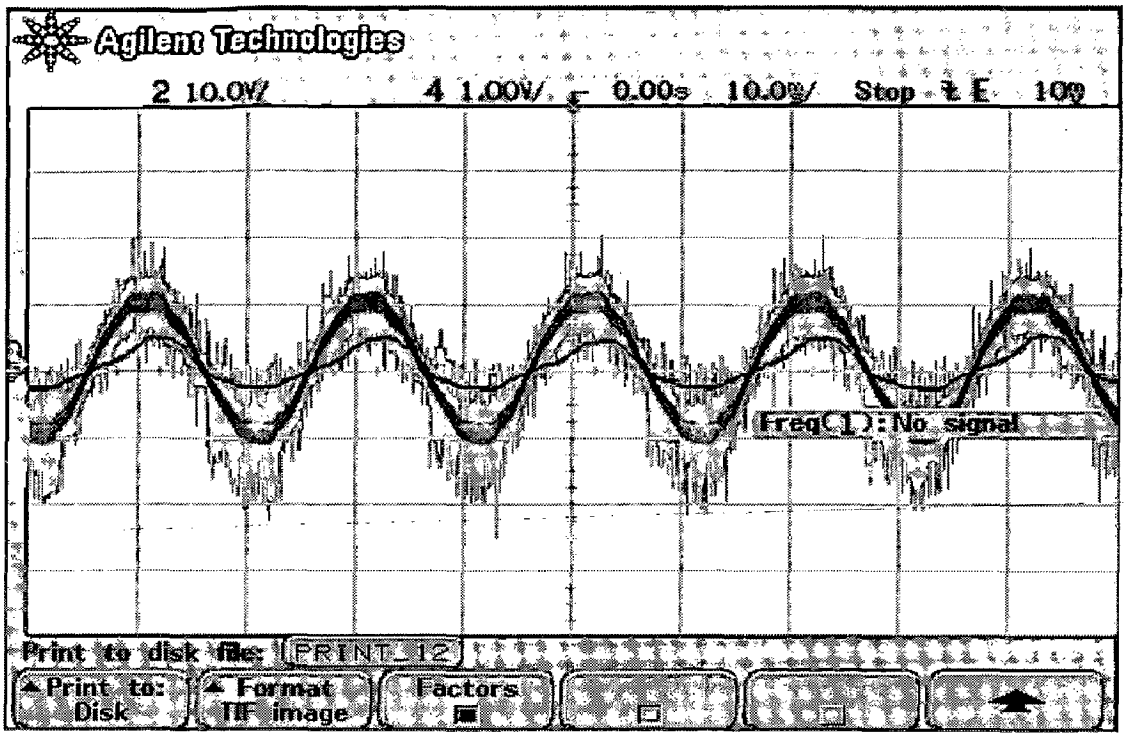


Fig. 7.5 Input voltage and input line current (10ms/div, 10V/div, 1V/div)

From case 1 result it is clear that by using new proposed control technique the input line currents are sinusoidal with phase difference of 120 degrees between each other and they have unity power factor. The switching frequency of the converter is calculated as 8 KHz which is very less compared to conventional hysterisis current control technique in which the switching frequency may go up to 25-30 KHz. The voltages at the input of switches are applied according to space vector modulation with out using any high-speed microprocessor. So by using this new technique we are able to solve draw backs of both SVM as well s HCC. This shows proposed control works very well with unity power factor at the input side.

Case 2

Input source voltage = 13V

Output resistance = 50.

Reference current = 3.5V

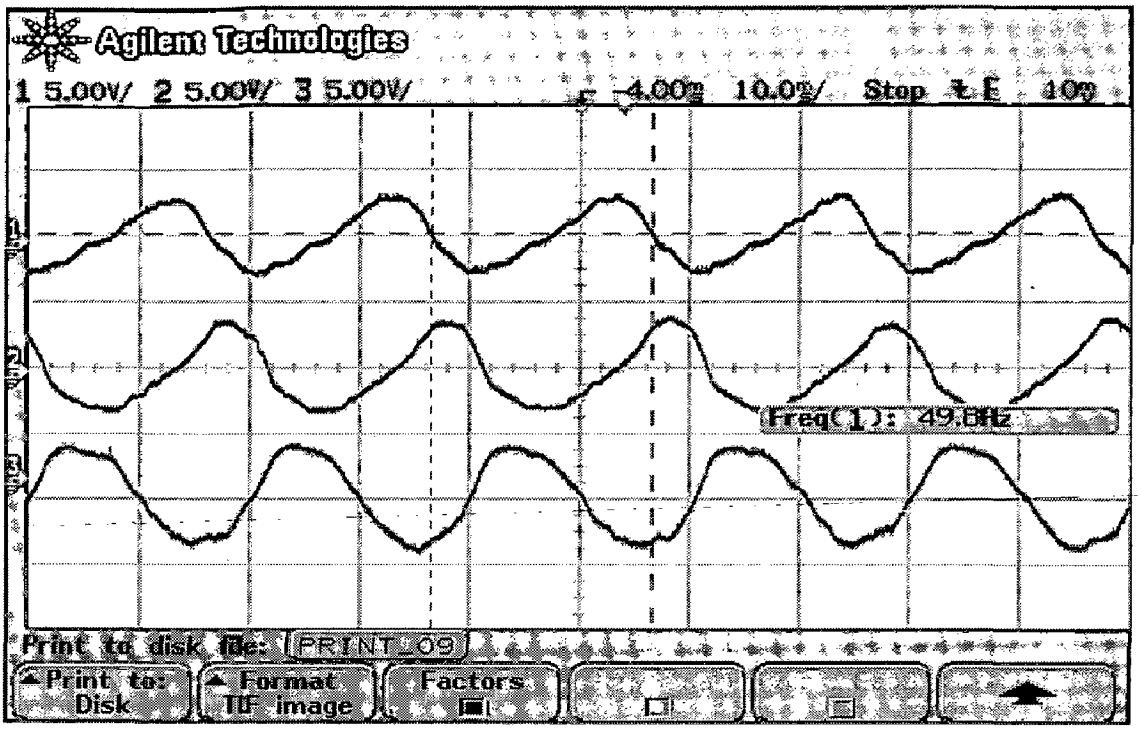


Fig.7.6 Input line currents (10ms/div, 5V/div)

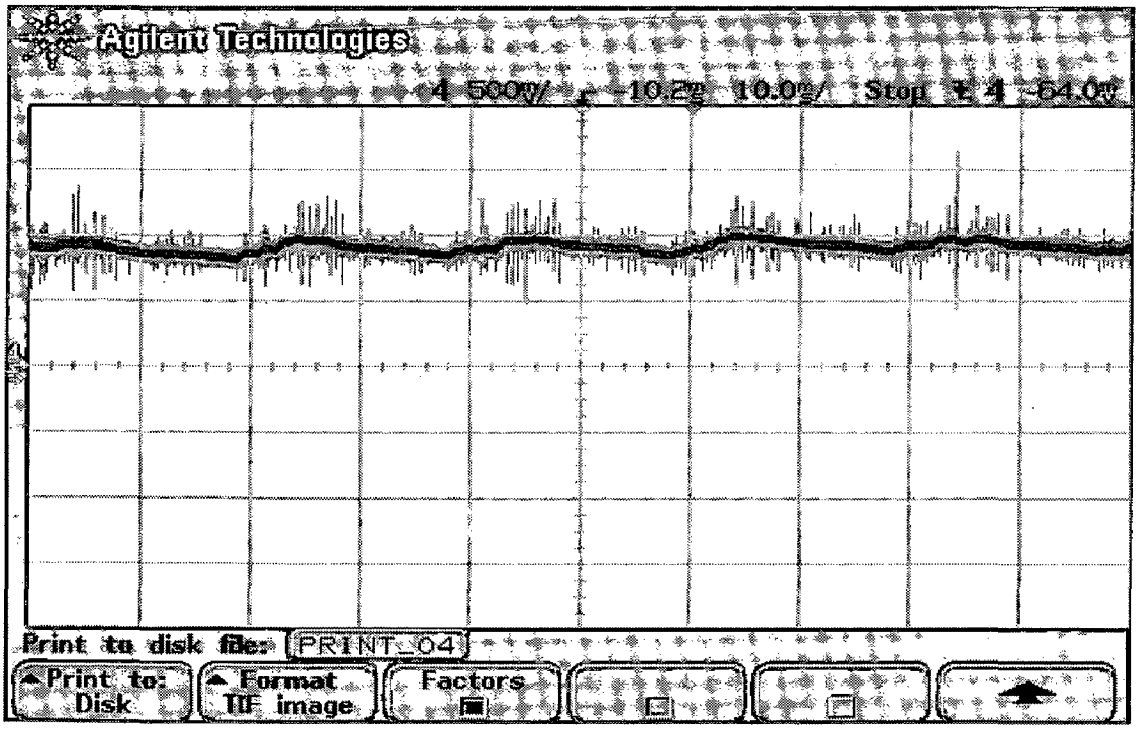


Fig. 7.7 Output Voltage (10ms/div, .5V/div)

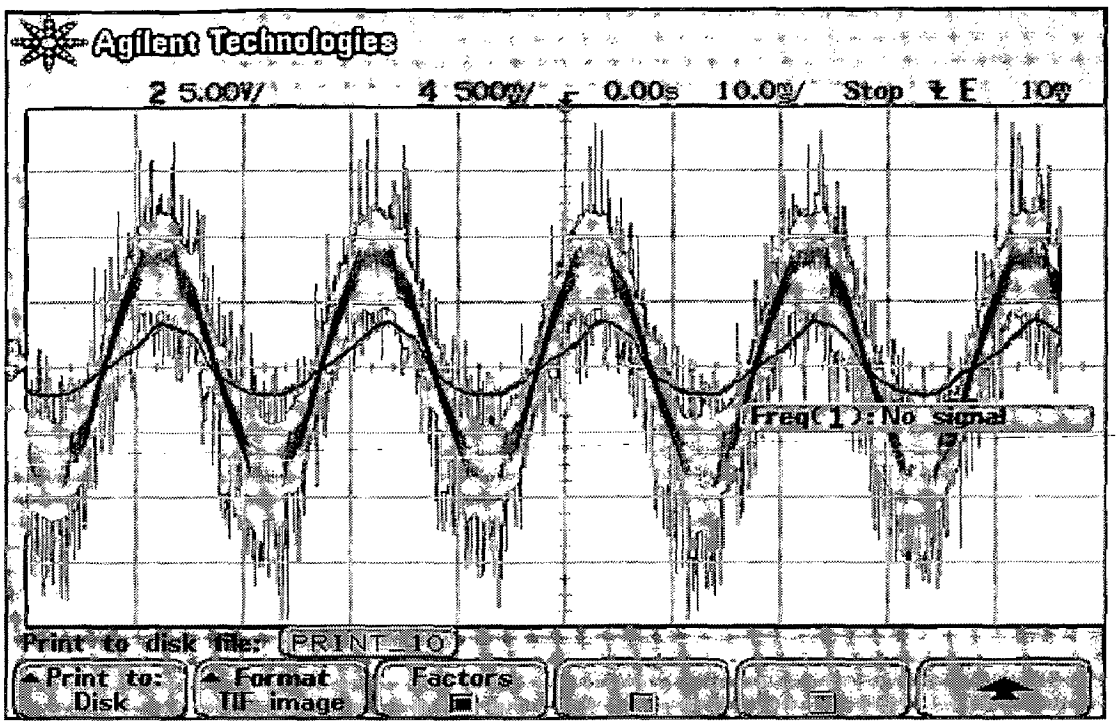


Fig. 7.8 Input voltage and input line current (10ms/div, 5V/div, 1V/div)

From case1 and case 2 it has been observing that the proposed technique is working properly. The input line currents are sinusoidal with unity power factor, and are in phase with input voltages. The output voltage in both cases is dc with very low ripple.

Case 3

Step response of a three-phase boost rectifier in open loop condition for step-down operation.

Input voltage =12V

Output resistance = 50.

First reference current = 3V

Step down reference current = 2 V

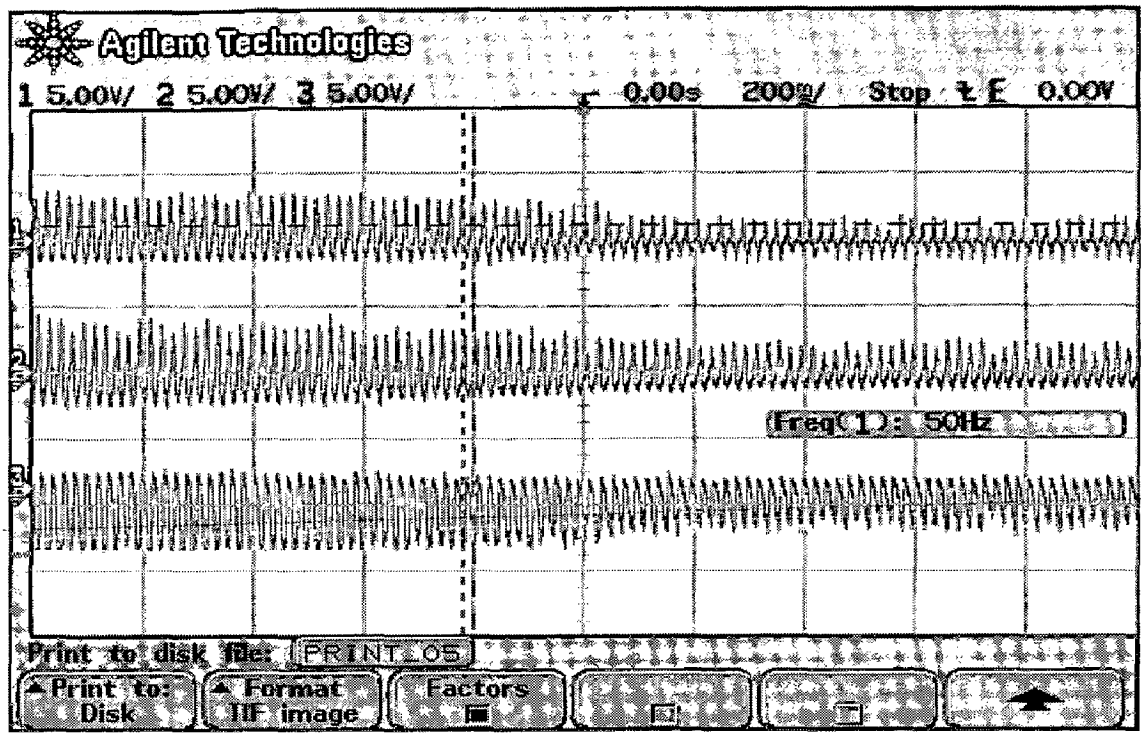


Fig.7.9 Input line currents (200ms/div, 5V/div)

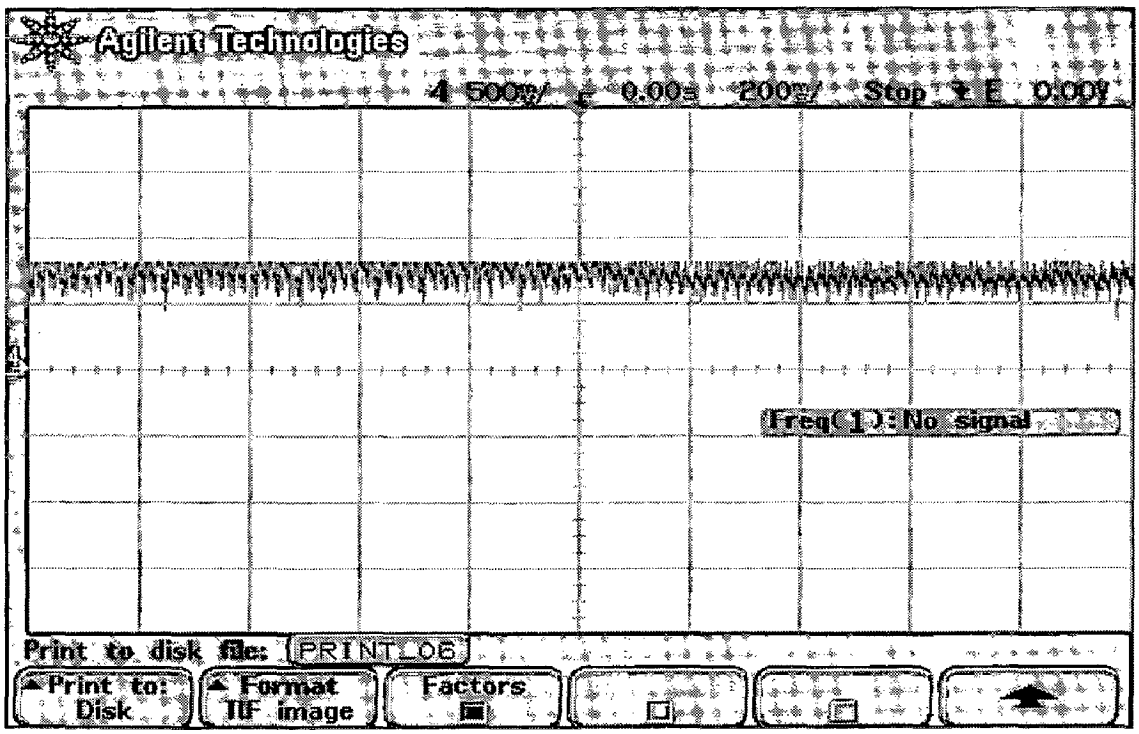


Fig. 7.10 Output Voltage (200ms/div, .5V/div)

Case 4

Step response of a three-phase boost rectifier in open loop condition for step-up operation.

Input voltage =12V

Output resistance = 50.

First reference current = 1.7V

Step down reference current = 3 V

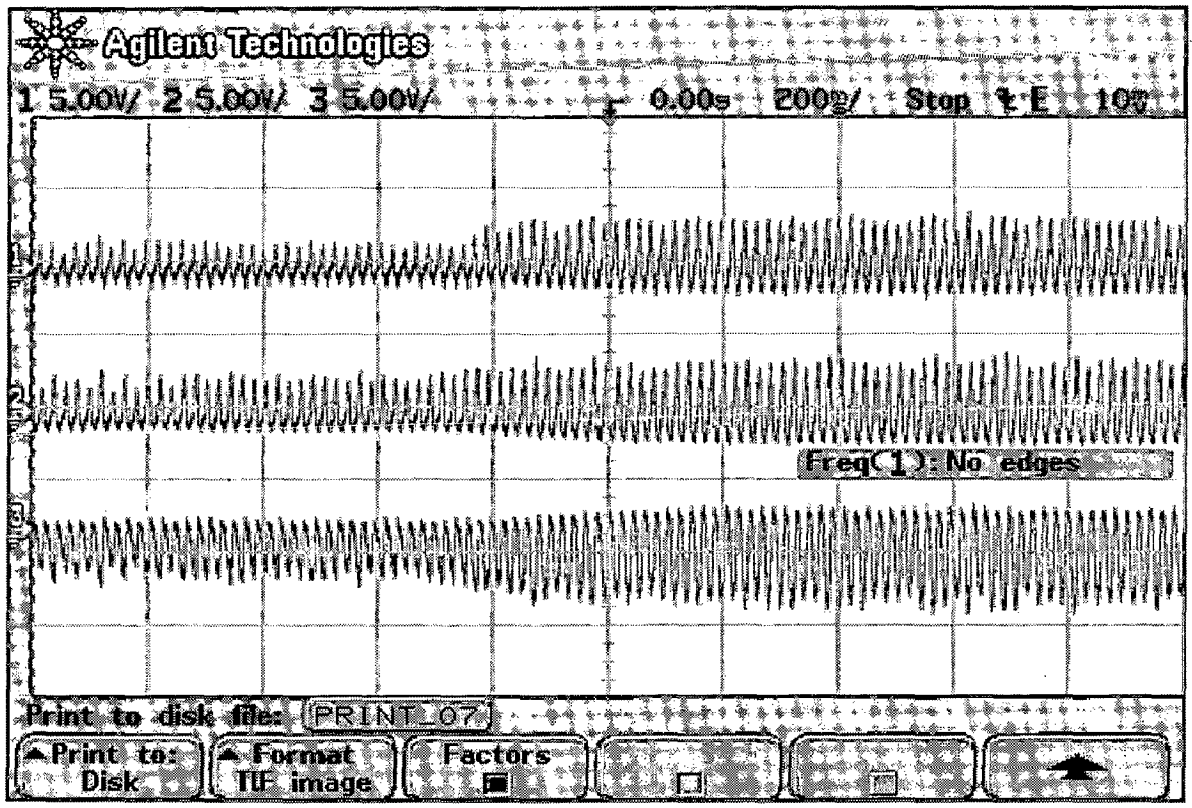


Fig.7.11 Input line currents (200ms/div, 5V/div)

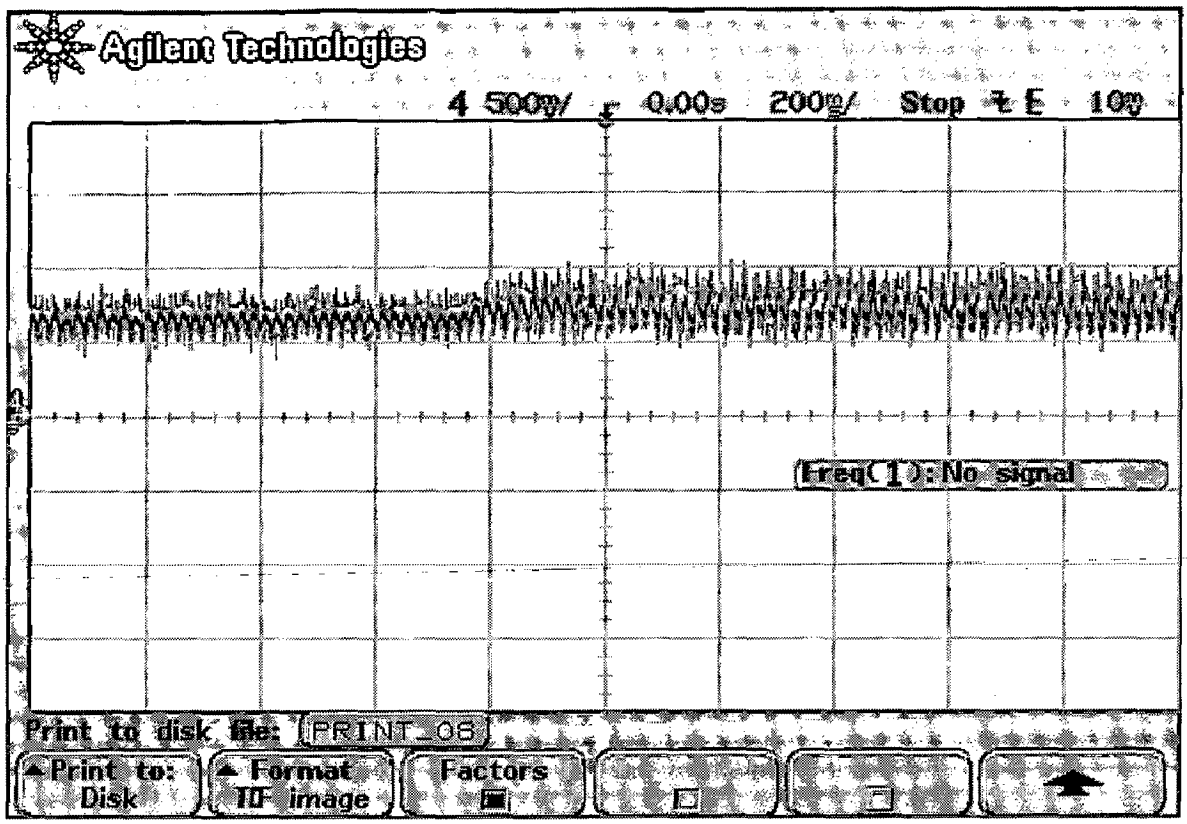
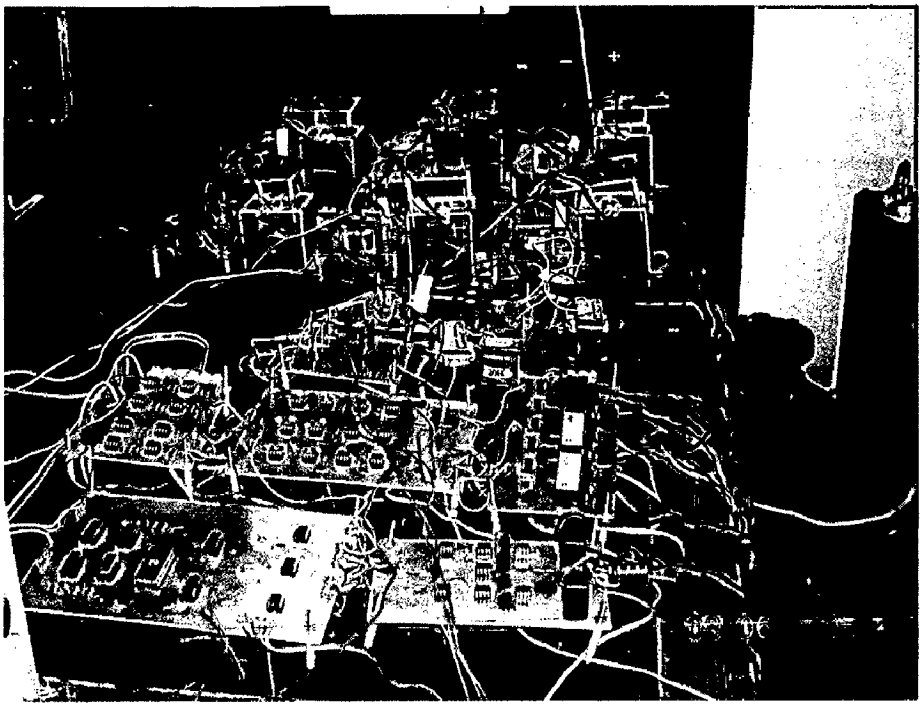


Fig. 7.12 Output Voltage (200ms/div, .5V/div)

From case 3 and case 4 results it has clear that step change in reference is allowed in this setup. When out put reference changes the current waveform is almost similar with change in magnitude.

Thus with all these results which have been recorded under open loop operation of 3 phase boost rectifier, shows that the proposed control technique working correctly with unity power factor input currents coming from source. Thus the converter operates satisfactorily under open loop.

PHOTOGRAPH OF HARDWARE SETUP



COMPLETE ASSEMBLY WITH PC INTERFACING

From above all results it is clear that setup is working well. Still better input line current wave form and output voltage very low ripple can be obtained by operating this setup under closed loop.

CHAPTER 8

CONCLUSIONS

In this thesis a new control technique for three-phase a.c to d.c converter is proposed. By using this control strategy combining space vector modulation and hysterisis current control, the switching numbers can be reduced and input current can be made to follow Source voltage wave form.

A SVM-based HCC for the three-phase PWM rectifier has been presented. This technique utilizes all advantages of the HCC and SVM technique. This configuration reduces significantly the number of switching than the conventional HCC and at the same time gives the same state space vectors as those obtained from the SVM technique. The proposed current controller gives the same maximum voltage as the SVM technique, almost negligible response time of the current error and insensitivity to line voltage and load parameter variation. The current controller confine state space vectors from the region detector and applies a proper space vector selected according to the HCC for better current shape.

The simulation of the High input power factor boost rectifier has been carried out and the response of the system is quite satisfactory. The control circuits for the generation of reference current and reference voltage for the boost rectifier have beendeveloped and tested. The waveforms of the control circuit obtained experimentally have also been shown. The power circuit waveforms have also been shown

All the results shown above have been carried under open loop operation of 3 phase boost rectifier.

As a future scope the converter can be run under closed loop operation for better operation, the control circuit can be still reduced if we can use pc to execute SVM-Based HCC switching table. Instead of pc control we can use DSP kit execute the control circuit and switching table, this may give fast response

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APPENDIX A

INFORMATION OF DATA ACQUISITION CARDS

The following two cards have been used for this application.

(1) **NUDAQ ACL-8316**: The ACL-8316 is a high performance, high speed, multi-function data acquisition card for IBM PC/XT/AT and compatible computers. The key features of this card are given below.

- 16 single-ended and 8 differential analog input channels
- An industrial standard 12-bit successive approximation converter (ADC574 or equivalent) to convert analog input. The maximum A/D sampling rate is 30 KHz in DMA mode.
- Switch selectable versatile analog input ranges.
  Bipolar: $\pm 1V, \pm 2V, \pm 5V, \pm 10V$
- Three A/D trigger modes: Software trigger
  Programmable pacer trigger
  External trigger pulse trigger
- The ability to transfer A/D converted data by program control interrupt handler routine, EOC interrupt, FIFI polling, FIFO or DMA transfer
- An INTEL 8253-5 Programmable Timer/Counter provides pacer output (trigger pulse) at the rate of 0.5 MHz to 35 minutes/pulse to the A/D. The timer time base is 2 MHz. One 16-bit counter channel is reserved for user configurable applications.
- Two 12-bit monolithic multiplying D/A output channels. An output range from 0 to ±10V can be created by using the onboard -10V reference
- 16 TTL/DTL compatible digital input, and 16 digital output channel.
- Auto scanning channel selection
- Up to 100KHz A/D sampling rates
- 3 independent programmable 16-bit down counter.

(2) **VYNITICS TIMER I/0 CARD:** The key features of this card are shown below.

- 48 programmable Input/Output using two 8255.
- Six channel of 16 Bit Timer/Counter.
- 8 optically isolated Input.
- 8 optically isolated Output.
- Jumper selectable I/0 addressing.
- Hardware clock selection for Timer/Counter.

APPENDIX B

IC DATA SHEETS

1. Low Cost, Miniature Isolation Amplifiers AD 202

FEATURES

Small Size: 4 Channels
Low Power: 35 mW (AD204)
High Accuracy: _0.025% Max Nonlinearity (K Grade)
High CMR: 130 dB (Gain = 100 V/V)
Wide Bandwidth: 5 kHz Full-Power (AD204)
High CMV Isolation: _2000 Vpk Continuous (K Grade)
(Signal and Power)
Isolated Power Outputs
Uncommitted Input Amplifier
APPLICATIONS
Multi channel Data Acquisition
Current Shunt Measurements
Motor Controls
Process Signal Isolation
High Voltage Instrumentation Amplifier

GENERAL DESCRIPTION

The AD202 and AD204 are general purpose, two-port, transformer-coupled isolation amplifiers that may be used in a broad range of applications where input signals must be measured, processed, and/or transmitted without a galvanic connection. These industry standard isolation amplifiers offer a complete isolation function, with both signal and power isolation provided for in a single compact plastic SIP or DIP style package. The primary distinction between the AD202 and the AD204 is that the AD202 is powered directly from a 15 V dc supply while the AD204 is powered by an externally supplied clock, such as the recommended AD246 Clock Driver. The AD202 and AD204 provide total galvanic isolation between the input and output stages of the isolation amplifier through the use of internal transformer-coupling. The functionally complete AD202 and AD204 eliminate the need for an external, user-supplied dc-to-dc converter. This permits the designer to minimize the necessary circuit overhead and consequently reduce the overall design and component costs. The design of the AD202 and AD204 emphasizes maximum flexibility and ease of use, including the availability of an uncommitted op amp on the input stage. They feature a bipolar ±5 V output range, an adjustable gain range of from 1V/V to 100 V/V, ± 0.025% max nonlinearity (K grade), 130 dB of CMR, and the AD204 consumes a low 35 mW of power.

AD202/AD204—SPECIFICATIONS (Typical @ 25°C and V_S = 15 V unless otherwise noted.)

Model	AD204J	AD204K	AD202J	AD202K
GAIN				
Range	1 V/V–100 V/V	*	*	*
Error	±0.5% typ (±4% max)	*	*	*
vs. Temperature	±20 ppm/°C typ (±45 ppm/°C max)	*	*	*
vs. Time	±50 ppm/1000 Hours	*	*	*
vs. Supply Voltage	±0.01%/V	±0.01%/V	±0.01%/V	±0.01%/V
Nonlinearity (G = 1 V/V)[1]	±0.05% max	±0.025% max	±0.05% max	±0.025% max
Nonlinearity vs. Isolated Supply Load	±0.0015%/mA	*	*	*
INPUT VOLTAGE RATINGS				
Input Voltage Range	±5 V	*	*	*
Max Isolation Voltage (Input to Output)				
AC, 60 Hz, Continuous	750 V rms	1500 V rms	750 V rms	1500 V rms
Continuous (AC and DC)	±1000 V Peak	±2000 V Peak	±1000 V Peak	±2000 V Peak
Isolation-Mode Rejection Ratio (IMRR) @ 60 Hz				
$R_S \leq 100\ \Omega$ (HI and LO Inputs) G = 1 V/V	110 dB	110 dB	105 dB	105 dB
G = 100 V/V	130 dB	*	*	*
$R_S \leq 1\ k\Omega$ (Input HI, LO, or Both) G = 1 V/V	104 dB min	104 dB min	100 dB min	100 dB min
G = 100 V/V	110 dB min	*	*	*
Leakage Current Input to Output @ 240 V rms, 60 Hz	2 μA rms max	*	*	*
INPUT IMPEDANCE				
Differential (G = 1 V/V)	$10^{12}\ \Omega$	*	*	*
Common-Mode	2 GΩ‖4.5 pF	*	*	*
INPUT BIAS CURRENT				
Initial, @ 25°C	±30 pA	*	*	*
vs. Temperature (0°C to 70°C)	±10 nA	*	*	*
INPUT DIFFERENCE CURRENT				
Initial, @ 25°C	±5 pA	*	*	*
vs. Temperature (0°C to 70°C)	±2 nA	*	*	*
INPUT NOISE				
Voltage, 0.1 Hz to 100 Hz	4 μV p-p	*	*	*
f > 200 Hz	50 nV/√Hz	*	*	*
FREQUENCY RESPONSE				
Bandwidth ($V_O \leq 10$ V p-p, G = 1 V–50 V/V)	5 kHz	5 kHz	2 kHz	2 kHz
Settling Time, to ±10 mV (10 V Step)	1 ms	*	*	*
OFFSET VOLTAGE (RTI)				
Initial, @ 25°C Adjustable to Zero	(±15 ±15/G)mV max	(±5 ± 5/G) mV max	(±15 ±15/G) mV max	(±5 ±5/G) mV max
vs. Temperature (0°C to 70°C)	$\left(\pm 10 \pm \frac{10}{G}\right)\mu V/°C$	*	*	*
RATED OUTPUT				
Voltage (Out HI to Out LO)	±5 V	*	*	*
Voltage at Out HI or Out LO (Ref. Pin 32)	±6.5 V	*	*	*
Output Resistance	3 kΩ	3 kΩ	7 kΩ	7 kΩ
Output Ripple, 100 kHz Bandwidth	10 mV p-p	*	*	*
5 kHz Bandwidth	0.5 mV rms	*	*	*
ISOLATED POWER OUTPUT[2]				
Voltage, No Load	±7.5 V	*	*	*
Accuracy	±10%	*	*	*
Current	2 mA (Either Output)[3]	2 mA (Either Output)[3]	400 μA Total	400 μA Total
Regulation, No Load to Full Load	5%	*	*	*
Ripple	100 mV p-p	*	*	*
OSCILLATOR DRIVE INPUT				
Input Voltage	15 V p-p Nominal	15 V p-p Nominal	N/A	N/A
Input Frequency	25 kHz Nominal	25 kHz Nominal	N/A	N/A
POWER SUPPLY (AD202 Only)				
Voltage, Rated Performance	N/A	N/A	15 V ± 5%	15 V ± 5%
Voltage, Operating	N/A	N/A	15 V ± 10%	15 V ± 10%
Current, No Load (V_S = 15 V)	N/A	N/A	5 mA	5 mA
TEMPERATURE RANGE				
Rated Performance	0°C to 70°C	*	*	*
Operating	–40°C to +85°C	*	*	*
Storage	–40°C to +85°C	*	*	*
PACKAGE DIMENSIONS[4]				
SIP Package (Y)	2.08" × 0.250" × 0.625"	*	*	*
DIP Package (N)	2.10" × 0.700" × 0.350"	*	*	*

NOTES
*Specifications same as AD204J.
[1]Nonlinearity is specified as a % deviation from a best straight line.
[2]1.0 μF min decoupling required (see text).
[3]3 mA with one supply loaded.
[4]Width is 0.25" typ, 0.26" max.
Specifications subject to change without notice.

2. Low Cost Analog Multiplier AD 633

FEATURES

4-Quadrant Multiplication

Low Cost 8-Lead Package

Complete—No External Components Required

Laser-Trimmed Accuracy and Stability

Total Error within 2% of FS

Differential High Impedance X and Y Inputs

High Impedance Unity-Gain Summing Input

Laser-Trimmed 10 V Scaling Reference

APPLICATIONS

Multiplication, Division, Squaring

Modulation/Demodulation, Phase Detection

Voltage Controlled Amplifiers/Attenuators/Filters

PRODUCT DESCRIPTION

The AD633 is a functionally complete, four-quadrant, analog multiplier. It includes high impedance, differential X and Y inputs and a high impedance summing input (Z). The low impedance output voltage is a nominal 10 V full scale provided by a buried Zener. The AD633 is the first product to offer these features in modestly priced 8-lead plastic DIP and SOIC packages. The AD633 is laser calibrated to a guaranteed total accuracy of 2% of full scale. Nonlinearity for the Y input is typically less than 0.1% and noise referred to the output is typically less than 100 μV rms in a 10 Hz to 10 kHz bandwidth. A 1 MHz bandwidth, 20 V/μs slew rate, and the ability to drive capacitive loads make the AD633 useful in a wide variety of applications where simplicity and cost are key concerns. The AD633's versatility is not compromised by its simplicity. The Z-input provides access to the output buffer amplifier, enabling the user to sum the outputs of two or more multipliers, increase the multiplier gain, convert the output voltage to a current, and configure a variety of applications. The AD633 is available in an 8-lead plastic DIP package (N) and 8-lead SOIC (R). It is specified to operate over the 0°C to 70°C commercial temperature range (J Grade) or the –40°C to +85°C industrial temperature range (A Grade).

AD633—SPECIFICATIONS (T_A = 25°C, V_S = ±15 V, $R_L \geq 2$ kΩ)

Model		AD633J, AD633A			
TRANSFER FUNCTION		$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10\ V} + Z$			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
MULTIPLIER PERFORMANCE					
Total Error	−10 V ≤ X, Y ≤ +10 V		±1	±2	% Full Scale
T_{MIN} to T_{MAX}			±3		% Full Scale
Scale Voltage Error	SF = 10.00 V Nominal		±0.25%		% Full Scale
Supply Rejection	V_S = ±14 V to ±16 V		±0.01		% Full Scale
Nonlinearity, X	X = ±10 V, Y = +10 V		±0.4	±1	% Full Scale
Nonlinearity, Y	Y = ±10 V, X = +10 V		±0.1	±0.4	% Full Scale
X Feedthrough	Y Nulled, X = ±10 V		±0.3	±1	% Full Scale
Y Feedthrough	X Nulled, Y = ±10 V		±0.1	±0.4	% Full Scale
Output Offset Voltage			±5	±50	mV
DYNAMICS					
Small Signal BW	V_O = 0.1 V rms		1		MHz
Slew Rate	V_O = 20 V p-p		20		V/μs
Settling Time to 1%	Δ V_O = 20 V		2		μs
OUTPUT NOISE					
Spectral Density			0.8		μV/√Hz
Wideband Noise	f = 10 Hz to 5 MHz		1		mV rms
	f = 10 Hz to 10 kHz		90		μV rms
OUTPUT					
Output Voltage Swing		±11			V
Short Circuit Current	R_L = 0 Ω		30	40	mA
INPUT AMPLIFIERS					
Signal Voltage Range	Differential	±10			V
	Common Mode	±10			V
Offset Voltage X, Y			±5	±30	mV
CMRR X, Y	V_{CM} = ±10 V, f = 50 Hz	60	80		dB
Bias Current X, Y, Z			0.8	2.0	μA
Differential Resistance			10		MΩ
POWER SUPPLY					
Supply Voltage					
Rated Performance			±15		V
Operating Range		±8		±18	V
Supply Current	Quiescent		4	6	mA

Specifications shown in **boldface** are tested on all production units at electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ..... ±18 V
Internal Power Dissipation[2] ..... 500 mW
Input Voltages[3] ..... ±18 V
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range
AD633J ..... 0°C to 70°C
AD633A ..... −40°C to +85°C
Lead Temperature Range (Soldering 60 sec) ..... 300°C
ESD Rating ..... 1000 V

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

[2]8-Lead Plastic DIP Package: θ_{JA} = 90°C/W; 8-Lead Small Outline Package: θ_{JA} = 155°C/W.

[3]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD633AN	−40°C to +85°C	Plastic DIP	N-8
AD633AR	−40°C to +85°C	Plastic SOIC	RN-8
AD633AR-REEL	−40°C to +85°C	13" Tape and Reel	RN-8
AD633AR-REEL7	−40°C to +85°C	7" Tape and Reel	RN-8
AD633JN	0°C to 70°C	Plastic DIP	N-8
AD633JR	0°C to 70°C	Plastic SOIC	RN-8
AD633JR-REEL	0°C to 70°C	13" Tape and Reel	RN-8
AD633JR-REEL7	0°C to 70°C	7" Tape and Reel	RN-8

3 M2764A (NMOS 64 K bit (8Kb x 8) UV EPROM)

FEATURES

- FAST ACCESS TIME: 180ns
- EXTENDED TEMPERATURE RANGE
- SINGLE 5V SUPPLY VOLTAGE
- LOW STANDBY CURRENT: 35mA max
- TTL COMPATIBLE DURING READ and PROGRAM
- FAST PROGRAMMING ALGORITHM
- ELECTRONIC SIGNATURE
- PROGRAMMING VOLTAGE: 12V

DESCRIPTION

The M2764A is a 65,536 bit UV erasable and electrically programmable memory EPROM. It is organized as 8,192 words by 8 bits. The M27C64A is housed in a 28 pin Window Ceramic Frit-Seal Dual-in-Line package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 6	0 to 70 –40 to 85	°C
T_{BIAS}	Temperature Under Bias	grade 1 grade 6	–10 to 80 –50 to 95	°C
T_{STG}	Storage Temperature		–65 to 125	°C
V_{IO}	Input or Output Voltages		–0.6 to 6.5	V
V_{CC}	Supply Voltage		–0.6 to 6.5	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply		–0.6 to 14	V