PERFORMANCE EVALUATION ON MULTI-LEVEL INVERTER FED INDUCTION MOTOR DRIVE

A DISSERTATION

Submitted in partial fulfilment of the requirements for the award of the degree of

MASTER OF TECHNOLOGY

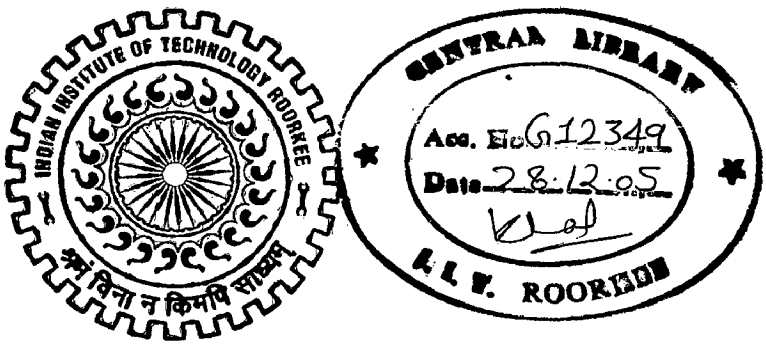
in

ELECTRICAL ENGINEERING

(With Specialization in Power Apparatus and Electric Drives)

By

BONDADA SUBBARAO



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ROORKEE-247 667 (INDIA)

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CANDIDATE'S DECLARATION

I hereby declare that the work that is being presented in this dissertation report entitled **"PERFORMANCE EVALUATION ON MULTI-LEVEL INVERTER FED INDUCTION MOTOR DRIVE"** submitted in partial fulfillment of the requirements for the award of the degree of **Master Of Technology** with specialization in **Power Apparatus and Electric Drives,** to the **Department Of Electrical Engineering, Indian Institute Of Technology, Roorkee**, is an authentic record of my own work carried out, under the guidance of **Dr. Pramod Agrawal**, Professor, Department of Electrical Engineering.

The matter embodied in this dissertation report has not been submitted by me for the Award of any other degree or diploma.

Date: 17/06/05
Place: Roorkee

(BONDADA SUBBARAO)

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

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I wish to express my deep sense of gratitude and sincere thanks to my beloved guide **Dr.** Pramod Agrawal, Prof., Department of Electrical Engineering, IIT Roorkee, for being helpful and a great source of inspiration. His keen interest and constant encouragement gave me the confidence to complete my work. I wish to extend my sincere thanks for his excellent guidance and suggestions for the successful completion of my project work.

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I also express sincere thanks to all staff members of Drives lab and Electric workshop for their help in completion of this work.

(Bondada Subbarao)

ABSTRACT

All the matter in the universe, the general trend to minimize harmonics in conventional 2-level voltage source inverter (VSI) is towards various PWM techniques. However, this trend invited problems, like the increase of switching frequency increased the switching losses, generating a common mode voltage which becomes significant at high power levels. Multilevel power converters have gained much attention in recent years due to the proven mitigation of various problems sited above. The general structure of the multilevel inverter is such as to synthesize a sinusoidal voltage from several levels of DC voltage. Increasing the number of level produces a fine staircase waveform approaching close to a sinusoidal wave with minimum harmonic distortion.

In this thesis simulation of various inverters (from 2-level to 5-level) is carried and the performance of the inverter is investigated under various operating conditions by changing the load and output frequency. The digital implementation of Space Vector Pulse Width Modulation (SVPWM) technique for both Three phase inverter and Neutral Point Clamped Inverter using '80486 Processor Based PC with Data Acquisition Cards' is described in detail. The work mainly focuses on the improvement in THD of both voltage and current waveforms from normal three-phase inverter to Neutral Point Clamped Inverter. The performance of open loop V/f control of three-phase Induction Motor drive fed from both conventional Three-Phase Inverter and Neutral Point Clamped Inverter is investigated in open loop. Finally the vector control scheme with for three-level inverter using SVPWM is implemented to drive an induction motor for variable speed applications.

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CHAPTER -1

INTRODUCTION

1.1 GENERAL

Recent years have seen a sea change in factory automation. The manufacturing lines in an industrial plant typically involve one or more variable speed motor drives that serve to various requirements of the plant like, power conveyor belts, robot arms, overhead cranes, steel process lines, paper mills and other processing lines. Prior to 1950s all such applications required the use of DC motor drive as the AC motor were not so flexible with respect to adjustable and smoothly varying speeds. But the inherent disadvantages of the DC drive promoted development on the side and eventually AC drives emerged as cost-effective and rugged compared to their DC counterparts. The reliability was also high. However the control flexibility with these drives is very limited and these proved to be suitable in applications where the speed need be regulated roughly like fan, pump, compressor etc. But high performance applications like machine tools, spindles; high-speed elevators etc need a much more sophisticated regulation of various variables such as speed, position, acceleration etc. Until recently this area was dominated by the DC drives. But with suitable control the induction motor drives are more than a match for DC drives in these high performance applications. The advances in microelectronics have simplified most of the control complexities of these drives and brought about an improved drive performance. The most common drive for the AC motor is the Voltage Source Inverter (VSI) Drive. Before discussing the multilevel-inverter fed drive a brief overview of the existing VSI fed induction motor drives is presented here.

1.2. VSI FED INDUCTION MOTOR DRIVE

The voltage source inverter (VSI) creates a relatively well-defined switched voltage waveform at the terminals of the motor. This requires stiff DC bus. It is typically sub divided into two types called the six-step inverter and pulse-width modulated inverter. The six-step inverter has six steps in the output line-to-neutral voltage. The harmonics present in the waveform are 6n+1. The Fourier analysis of this waveform reveals a "square-wave" type of geometric progression of the harmonics. That

is, the line-to-line and the line-to-neutral waveforms contain1/5^{th} of the 5^{th} harmonic,1/7^{th} of the 7^{th} harmonic, 1/11^{th} of the 11^{th} harmonic and so on. That 20% 5^{th} harmonic,14.28% 7^{th} harmonic,9.09% 11^{th} harmonic and so on which is quite high.

The harmonics in general have two undesirable effects:

- Harmonic Heating
- Torque Pulsations

The PWM inverter combines both the voltage and frequency control within the inverter itself. Various PWM techniques have been implemented [29]; of these the sinusoidal PWM has been found to be one of the techniques to synthesize the motor currents as near to a sinusoidal as possible. The lower voltage harmonics can be greatly attenuated in this technique. PWM inverter fed motor tends to rotate much more smoothly at low speed. Torque pulsations and harmonic losses are reduced compared to 6-step inverter fed drive. The problems with this drive, as pointed out earlier, is the high dv/dt caused due to high frequency switching between the highest DC levels to zero. This produces common mode voltages across the motor winding that drives currents through the motor bearings resulting in its failure. High dv/dt also causes corona losses in the winding layers. The switching losses in the inverter are also high. Further, the voltage and switching frequency ratings of the devices are required to be high at high-power and high-voltage end applications.

1.3. SPACE VECTOR MODULATION (SVM):

The space-vector PWM (SVPWM) method is an advanced, computation-intensive PWM method and is possibly the best among all the PWM techniques for variable-frequency drive applications. Because of its superior performance, it has been finding widespread application in recent years. It is a carrier less method of generating PWM pattern for entire range of operating frequency. The space vector technique has the advantage that harmonics in motor currents are drastically reduced. This technique can be employed on-line with a processor. The synchronization of carrier to modulating signal is not needed, which reduces the burden of control and firing circuit

The PWM methods given in [29] have only considered implementation of a half-bridge of three-phase bridge inverter. If the load neutral is connected to the center

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tape of dc supply all the three bridges operate independently, giving satisfactory PWM performance. With a machine load, the load neutral is normally isolated, which causes the interaction among the phases. This intersection was not considered before in the PWM discussions. The SVM technique considers this interaction of the phases and optimizes the harmonic content of the three-phase isolated neutral load.

1.4. MULTI-LEVEL INVERTER FED INDUCTION MOTOR DRIVE

The multi level starts with the three-level which is also known as neutral point clamped three-level inverter proposed by Akari Nabae [1]. Recently, with the dramatic improvements in high voltage technologies, high voltage insulated gate bipolar transistor (HVIGBT) and gate commutated thyristor (GCT) are expanding the area of their application. For the high performance ac drive systems at increased power level, high quality inverter output with low harmonic loss and torque pulsation is necessary. In case of the conventional two-level inverter configuration, the harmonic contents reduction of an inverter output current is achieved mainly by raising the switching frequency.

However in the field of high voltage, high power applications and the switching frequency of the power device has to be restricted below 1 KHz, even with the HVIGBT and GCT, due to the increased switching loss. So the harmonic reduction by raised switching frequency of a two-level inverter becomes more difficult in high power applications. In addition, as the dc link voltage of a two-level inverter is limited by voltage ratings of switching devices, the problematic series connection of switching devices is required to raise the dc link voltage. By series connection, the maximum allowable switching frequency has to be more lowered, thus the harmonic reduction becomes more difficult. From the aspect of harmonic reduction and high dc-link voltage level; three-level approach seems to be the most promising alternative. The harmonic contents of a three-level inverter are less than that of a two-level inverter at the same switching frequency and the blocking voltage of the switching device is half of the de-link voltage. So the three-level inverter topology is generally used in realizing the high performance, high voltage ac drive systems [1]. However, the inherent neutral-point potential variation of a three-level inverter has to be effectively suppressed to fully utilize

the above-mentioned advantages of a three-level inverter. So many PWM strategies have been proposed to solve the neutral-point potential unbalance problem [5], [8], [9].

In this thesis, a simple SVPWM method for three-level inverter is proposed. By using the new PWM strategy, dwelling time calculation and switching sequence selection are easily done like conventional two-level inverter. And the neutral-point voltage control algorithm can be easily implemented. In this paper, the proposed three-level SVPWM method is explained in detail.

Multilevel inverters are based on the fact that a sine-wave can be approximated to a stepped waveform having large number of steps. The steps being supplied from different DC levels supported by series connected batteries or capacitors. Multilevel inverters have gained importance recently in power applications because of the problems reported by the industry with regard to two-level PWM based adjustable-speed drives (ASD's). The problems reported were mainly of motor damage, particularly motor bearings failure and motor winding insulation break-down because of circulating currents, dielectric stresses, voltage surges and corona discharge. The problems have attributed to high-rate-of change of voltage (dv/dt), of these inverters, which produces common voltage across motor windings. It has been shown that in general, increasing the switching frequency in voltage-source inverters (VSIs), better voltage/current waveforms are obtained. Advances in the semi-conductor device technology (<1ms required for turn on and turn off) have permitted to advance in his direction. This has allowed faster PWM carrier frequencies to be used, increasing the motor running efficiency. But the associated dv/dt and hence di-electric stresses between winding turns also increased greatly. At the inverter end the high frequency switching increased the switching losses.

Multilevel inverters overcome most of the problems cited above for earlier VSI and PWM techniques. The individual switches in multi-level configuration have a much lower dv/dt per switching, eliminating the problems of voltage stresses and corona discharge. Also multi-level inverters operate at high efficiencies because they can at a much lower frequency than PWM controlled inverter.

The unique structure of multi-level inverters allows them to reach higher voltages and therefore lower voltage-rating devices can be used. As the number of levels increases, the synthesized output waveform has more steps, producing a very fine stair

case wave and approaching very closely to the desired sine wave. It can be easily understood that as more and more steps are included in the waveform, the harmonic distortion of the output wave decreases, approaching zero as the number of levels approaches infinity.

Some of the problems associated with multilevel inverters.

- Difficult and very complex to achieve series redundancy
- Capacitor voltage balancing
- More complex PWM control strategy for higher levels
- Circuit complexity for higher levels
- Large device control

In spite of these problems, multi-level inverters offer a great potential for improving the drive performance in the industry. For a moderate number of levels the number of devices can be limited and combined with modular design, the overall designing of the inverter can be further simplified.

1.5. MICROPROCESSORS IN MOTOR CONTROL

Market analysis shows that most of all industrial motor applications use AC induction motors. The reasons for this include high robustness, reliability, low price and high efficiency (up to 80%). However, the use of induction motors also has its disadvantages, these lie mostly in its difficult controllability, due to its complex mathematical model, its non linear behavior during saturation effect and the electrical parameter oscillation which depends on the physical influence of the temperature. Traditionally motor control was designed with analog components; they are easy to design and can be implemented with relatively inexpensive components. However, there are several drawbacks with analog systems. Aging and temperature can bring about component variation causing the system to need regular adjustment, as the parts count increase the reliability of the system decreases. Analog components raise tolerance issues and upgrades are difficult as the design is hardwired. Digital systems offer improvements over analog designs. Drift is eliminated since most functions are performed digitally, upgrades can easily be made in software and part count is also reduced since digital systems can handle several functions on chips.

Hyo L. Liu, Nam S. Choi and Gyu H. Cho in their publication[5] titled " DSP based Space Vector PWM For Three-Level Inverter With DC-link voltage balancing", presented a new PWM method for three-level inverter considering DC-link capacitor balancing problem using Motorola DSP 56000. In this paper each voltage vector on space vector plane is classified in relation to charging discharging action of DC capacitors.

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Micro Processors go on further to provide high speed, high resolution and sensor less algorithms in order to reduce system costs. Providing a more precise control to achieve better consumption or radiation performances often means performing more calculations speeds-up calculations. Generally fixed point Micro Processors are preferred for motor control for two reasons.

Benefits of the Micro Processor Controllers

The performances of an AC induction motor are strongly dependent on its control. Micro Processors controllers enable enhanced real time algorithms as well as sensorless control. The combination of both allows to reduce the number of components and to optimize the design of silicon, to achieve a system cost reduction. .

- Favours system cost reduction by an efficient control in all speed range implying right dimensioning of power device circuits
- Performs high level algorithms due to reduced torque ripple, resulting in lower vibration and longer life time.
- Enables a reduction of harmonics using enhanced algorithms, to meet easier requirements and to reduce filters cost.
- Removes speed or position sensors by the implementation of sensor less algorithms.
- Decreases the number of look-up tables which reduces the amount of memory required.
- Real-time generation of smooth near-optimal reference profiles and move trajectories, resulting in better-performing.
- Controls power switching inverters and generates high-resolution PWM outputs.
- Provides single chip control system.

Microcontroller has the disadvantage of signal quantization and sampling delay. It is sluggish as compared to dedicated hardware. One of the main difficulties with conventional tracking controllers for electric drives is their inability to capture the unknown load characteristics very a widely ranging operating point. This makes the tuning of the respective controller parameters difficult.

1.6. ORGANIZATION OF THIS THESIS

CHAPTER 2: This chapter a review of the various publications in this field has been discussed briefly.

CHAPTER 3: This chapter focuses on the basic principle of obtaining a multilevel waveform, different topologies and classification of multi-level inverters, which includes some of the recently developed circuit topologies. The salient features of each topology have been presented and relative comparison has also been made.

CHAPTER 4: This chapter includes the simulation of various inverters (2-level, 3-level, 5-level) using 'MATLAB 6.5' software. The performance of these inverters was investigated under various conditions of the load (Both R-L and Induction Motor) by changing output frequency using Sinusoidal Pulse Width Modulation Technique. The main aim of this chapter is to investigate the effect on harmonic spectra and THD as number of levels increased from conventional 2-level to 5-level inverters

CHAPTER 5: This chapter discusses the various PWM techniques for multilevel inverters and briefly explains the theory and digital implementation of Space Vector PWM for both conventional Three-phase Inverter and Neutral-Point Clamped Inverter.

CHAPTER 6: This chapter explains the theory and implementation of open loop V/Hz control and Field Oriented Control for Induction Motor Drive.

CHAPTER 7: This chapter consists of three sections.

- Hardware development
- Software development
- PC interfacing and control

In Hardware development, hardware requirement for the realization of the Thee-level Neutral Point Clamped inverter and Three-phase inverter has been given, and design of various circuits like power supplies, current measurement, delay circuit, snubber circuit for MOSFET are explained in detail. In software development section Open Loop V/f control of induction motor using both conventional Three-phase inverter and Neutral-Point Clamped Inverter has been explained with the flowcharts. PC interfacing with the hardware is discussed briefly. The complete software for the Field Oriented Control of Induction Motor consisting of current measurement, current PI processing, speed measurement, speed PI processing has been discussed briefly with the

help of flowcharts. Only the pictorial representation of software has been given. The complete software has been written using 'C- Language'

CHAPTER 8: This chapter presents the experimental results such as firing pulses to MOSFETs, line voltages and their THDs, phase voltages, line currents and their THDs under various conditions of load at different frequencies using both the inverters. And relative comparison of line currents THDs between 2-level and 3-level inverters has been presented with the help of charts.

CHAPTER 9: This chapter presents the conclusion of this thesis and scope for future work in this area.

CHAPTER-2

LITERATURE REVIEW

Harmonic distortion was one of the most important factors in the evolution of the multilevel inverters. Akira Nabae et. al. [1] in their publication titled, "A New Neutral-Point-Clamped PWM Inverter", has made a clear distinction between the conventional and the multilevel inverters vis-a-vis the harmonic spectra. The multilevel technique was introduced here in combination with the already existing PWM technique.

Jih-Sheng Lai and Fang Zheng Peng in their publication [2] titled, "Multilevel Converters - A New Breed of Power Converters", bring out clearly the working of each of the three basic types of multilevel inverters. The potential applications like reactive power compensation, back-to-back intertie and adjustable speed drives has been presented.

Jose Rodriguez, Jih-Shing Lai and Fang Zheng Peng in their publication [3] titled "Multilevel Inverters: A survey of Topologies, Controls, and Applications", presents the most important topologies like diode-clamped inverter (neutral-point clamped), capacitor-clamped (flying capacitor), and cascaded multicell with separate dc sources. Emerging topologies like asymmetric hybrid cells and soft-switched multilevel inverters are also discussed. This paper also presents the most relevant control and modulation methods developed for this family of converters: multilevel sinusoidal pulse width modulation, multilevel selective harmonic elimination, and space-vector modulation.

Texas Instruments application note no. SPRA284a [4] titled "AC Induction Motor Control Using Constant V/Hz Principle and Space Vector PWM Technique with TMS320C240" presents digital implementation of space vector modulation using d-q model and principles of constant V/Hz control for AC Induction motor. Two different implementations are presented. Implementation issues such as command voltage generation, switching pattern determination, speed measurement and scaling are discussed.

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Fang Zheng Peng in his publication [10] titled, "A Generalized Multilevel Inverter Topology with Self Voltage Balancing", has presented a generalized topology from which any type and any level multilevel inverter can be deduced. The topology proposed has a self-voltage balancing property. But for higher levels, the device count becomes quite high.

Leon M. Tolbert, Fang Z. Peng , Thomas G. Habetler in their publication[11] titled "Multilevel Inverters for Electric Vehicle Applications" presented applications of multilevel inverters for all-electric vehicle(EV) and hybrid-electric(HEV) motor drives. This paper explores the benefits and discussed the control schemes of the cascade inverter for use as an EV motor drive or a parallel HEV drive and the diode clamped inverter as a series HEV motor drive.

Leon M. Tolben, Fang Zheng Peng and Thomas G. Habetler in their publication [12] titled, "Multilevel Converters for Large Electric Drives", have proved the suitability of multilevel converters for high power and/or high voltage electric motor drives. The cascaded inverter has been shown to be a natural fit for large automotive all-electric drives because it uses several levels of DC voltage sources, which would be available from batteries or fuel cells. Also a back-to-back diode clamped converter has been found to be ideal where a source of AC voltage is available, such as in a hybrid electric vehicle.

Texas Instruments application note no. SPRU485A [13] titled "Digital Motor Control, Software Library "describes briefly the digital implementations of PI controllers, Park's transformation, Clark's transformation, Integrator, speed measurement, current measurement through 'C' language.

Texas Instruments Literature Number BPRA076 titled [14] "Implementation of a Speed Field Orientated Control of Three Phase AC Induction Motor using TMS320F240", It consists of two sections The first section deals with the presentation of the field orientated controlled AC induction drive; it explains the AC induction motor, the control hardware, the power electronics hardware as well as the complete FOC structure. The second section deals with the implementation of TMS320F240 drive speed control. Here, the details of how and why the software is

organized, the Per Unit model, the numerical consideration, the current and speed sensing and scaling, the regulators, the system transformations, the current model, the field weakening and the space vector modulation are fully explained step by step.

CHAPTER-3

MULTILEVEL INVERTERS

This chapter focuses on the basic principle of obtaining a multilevel waveform, classification of multi-level inverters and their operation, which includes some of recently developed circuit topologies. The salient features of each topology have been presented and a relative comparison has also been made.

3.1. INTRODUCTION

Multilevel inverter technology has emerged recently as a very important alternative in the area of high-power medium-voltage energy control. The term multilevel starts with the 3-level inverter introduced by "**Akari Nabae** "in 1981[1]. By increasing the number of levels in inverter the output voltages have more steps generating staircase waveform which has reduced harmonic distortion. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of capacitor voltages, which reach high voltage at output, while power semiconductors must withstand only reduced voltages.

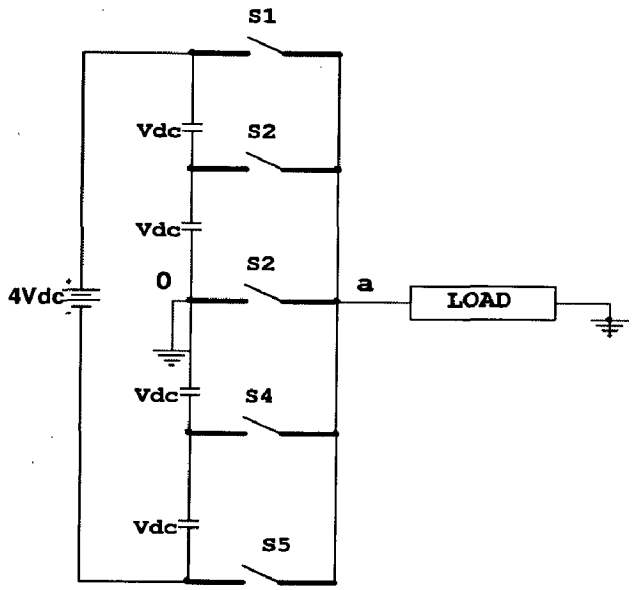
Multi level inverters are based on the fact that sine wave can be approximated to a stepped wave form having large number of steps. The steps being supplied from different DC levels supported by series connected batteries or capacitors. The individual devices in multilevel configuration have a much lower dv/dt per switching at a much lower frequency than PWM- controlled inverter. The unique structure of multi level inverters allows them to reach high voltages and therefore lower voltage rating devices can be used.

As the number of levels increases the synthesized output waveform has more steps producing a very fine stair case wave and approaching very closely to the desired sine wave. It can be easily understood that as the more and more steps are included in the waveform the harmonic distortion of the output wave decreases approaching zero as the number of levels approaching infinity. Hence multi level inverters offer a better choice at a high power end because the high volt-ampere ratings

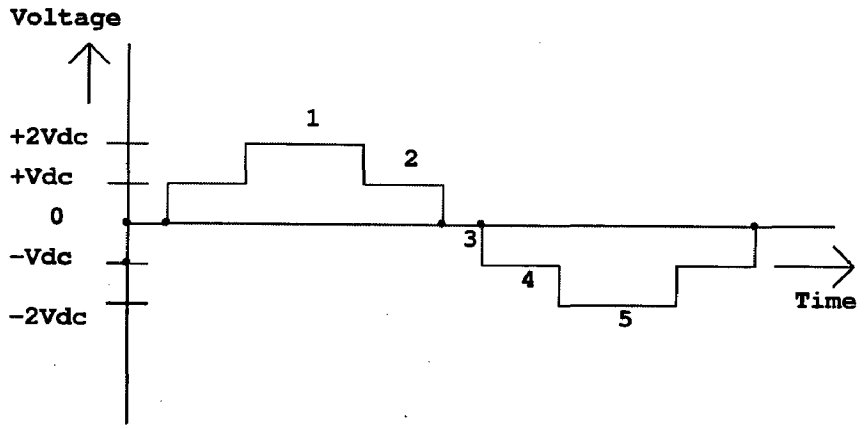
are possible with these inverters without the problems of high dv/dt and the other associated ones.

3.2. BASIC PRINCIPLE

To understand the concept of multilevel inverters consider the circuit shown in Fig 3.1. Here capacitors are connected in series and across the main DC source 4 V_{dc}.



(a)



(b)

Fig.3.1 Basic principle of Multi-level inverter (a) Circuit (b) output voltage

Here capacitors are connected in series and across the main DC source V_{dc}. The switches S_1-S_5 are closed one at a time for a fixed duration of time. The load voltage which is

measured with respect to the reference point 0, in shown in the form of waveform in Fig.3.2. Table3.1 lists the switching states and output voltage obtained for each state of switches. Switch state '1' means ON and '0' means OFF. It can be seen that a stepped wave is output to the load. The stepped can be approximated to a sine wave by adding more number of capacitors (levels) in series. Also it can be noted that 5-level waveform requires four capacitors and so on. In general an inverter consists of m-1 capacitors on the DC bus and produces m-levels of the phase voltage.

V_{ao}	Switching States				
	S_1	S_2	S_3	S_4	S_5
0	0	0	1	0	0
V_{dc}	0	1	0	0	0
$2V_{dc}$	1	0	0	0	0
V_{dc}	0	1	0	0	0
0	0	0	1	0	1
$-V_{dc}$	0	0	0	1	1
$-2V_{dc}$	0	0	0	0	1
$-V_{dc}$	0	0	0	1	0

Table 3.1 Switching States of Multi-level Inverter

Features of Multilevel Inverters

- This can generate output voltages with extremely low distortion and lower dv/dt.
- They draw input current with very low distortion
- They generate smaller common mode voltages thus reducing the stress in the motor bearings. In addition using sophisticated modulation methods, common mode voltages can be eliminated.
- They can operate with a lower switching frequency.
- Excellent dynamic response
- Smooth torque/speed control over full speed range

- Increase frequencies up to 200Hz
- Improved AC supply power factor
- Lesser Torque pulsations
- Lower audible noise levels

Problems associated with Multilevel Inverters

Some of the problems associated with multilevel inverters.

- Difficult and very complex to achieve series redundancy
- Capacitor voltage balancing
- More complex PWM control strategy for higher levels
- Circuit complexity for higher levels
- Large device control

3.3. THE TOPOLOGIES IN MULTILEVEL INVERTERS

The topologies available have been given as:

- Series connected 2-level inverter(SC2L)
- 3-level neutral point clamped MLI(3LNPC)
- Multilevel Inverter.

Series Connected 2-Level Inverter

Switch-mode dc-to-ac inverters used in ac power supplies and ac motor drives where the objective is to produce a sinusoidal ac output whose magnitude and frequency can both be controlled. Practically, we use an inverter in both single-phase and three-phase ac systems. A half-bridge is the simplest topology, which is used to produce a two-level square-wave output waveform. A center-tapped voltage source supply is needed in such a topology. It may be possible to use a simple supply with two well-matched capacitors in series to provide the center tap. The full-bridge topology is used to synthesize a three-level square-wave output waveform. The half-bridge and full-bridge configurations of the single-phase voltage source inverter are shown in Fig. 3.3 and Fig. 3.4 respectively.

In a single-phase half-bridge inverter, only two switches are needed. To avoid shoot-through fault, both switches are never turned on at the same time. S_1 is turned on and S_2 is turned off to give a load voltage, V_{AO} in Fig. 3.2(a), of $V_{dc}/2$. To complete one cycle, S_1 is turned off and S_2 is turned on to give a load voltage, V_{AO} of $-V_{dc}/2$. In full bridge configuration, turning on S_1 and S_4 and turning off S_2 and S_3 give a voltage of V_{dc} between point A and B (V_{AB}) in Fig. 3.2(b), while turning off S_1 and S_4 and turning on S_2 and S_3 give a voltage of $-V_{dc}/2$.

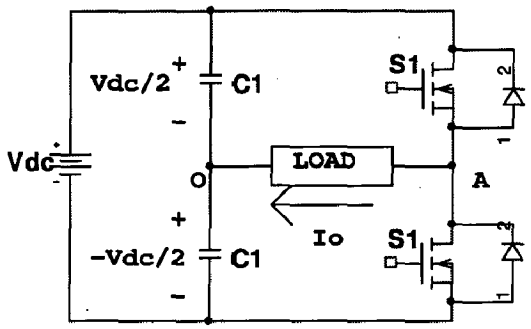


Fig. 3.2(a) Half Bridge Configuration

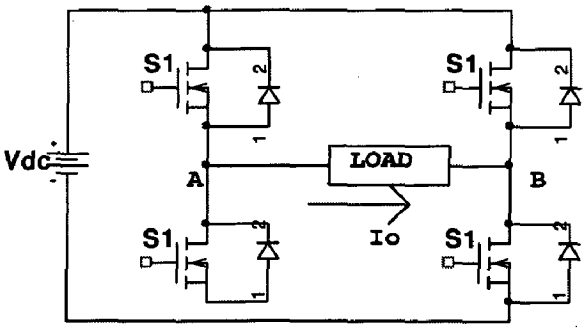


Fig. 3.2(b) Full Bridge Configuration

Note that S_1 and S_3 should not be closed at the same time, nor should S_2 and S_4. Otherwise, a short circuit would exist across the dc source. The output waveform of half-bridge and full-bridge of single-phase voltage source inverter are shown in Fig. 3.3(a) and 3.3(b) respectively.

devices S_{1U} and S_{4U} function as main devices (like two level inverter), and S_{2U} and S_{3U} function as auxiliary devices which help to clamp the output potential to the neutral point with the help of clamping diodes D_1 and D_2.

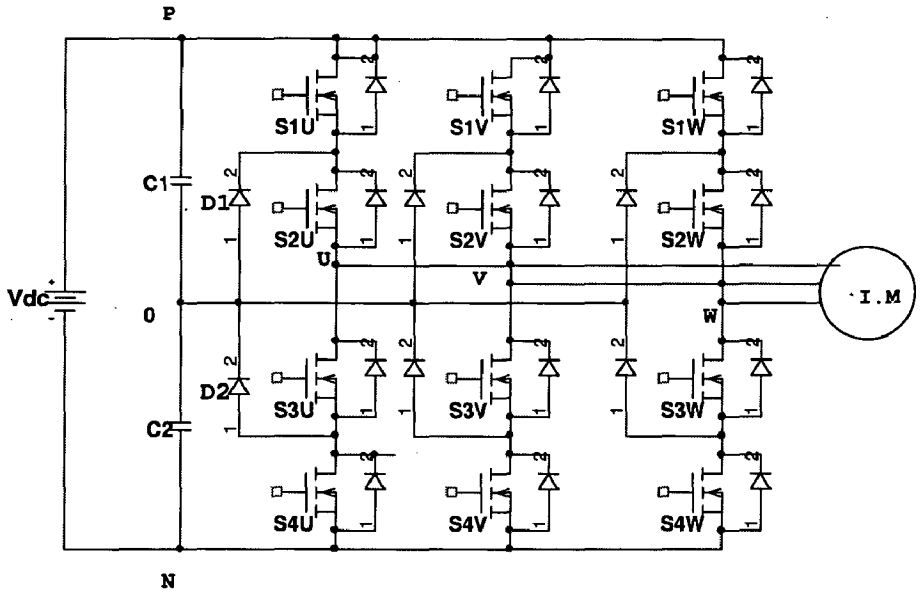


Fig 3.4 Neutral Point Clamped Three-level Inverter

The harmonic contents of a three-level inverter are less than that of a two-level inverter at the same switching frequency and the blocking voltage of the switching device is half of the de-link voltage.

However, the concept of three level inverter introduced a new zero voltage level (also called neutral point), other than the positive and negative voltage levels in comparison to two level inverter. This type of DC links inherently associated with neutral point variations and results in a voltage unbalance problems between the lower and upper capacitor dc-link capacitors, causing undesirable uneven voltage stress at the upper and lower array of switching elements[9][23][26]. The inherent neutral point potential variation of a three-level inverter has to be effectively suppressed to fully utilize the advantages of three-level inverter. More complex PWM control is needed than 2-level. And requires mid point voltage balance control and neutral point voltage control. So many PWM techniques have been proposed in literature [22], [23], [25] and [26] to solve the above mentioned problems.

In a single-phase half-bridge inverter, only two switches are needed. To avoid shoot-through fault, both switches are never turned on at the same time. S_1 is turned on and S_2 is turned off to give a load voltage, V_{AO} in Fig. 3.2(a), of $V_{dc}/2$. To complete one cycle, S_1 is turned off and S_2 is turned on to give a load voltage, V_{AO} of $-V_{dc}/2$. In full bridge configuration, turning on S_1 and S_4 and turning off S_2 and S_3 give a voltage of V_{dc} between point A and B (V_{AB}) in Fig. 3.2(b), while turning off S_1 and S_4 and turning on S_2 and S_3 give a voltage of $-V_{dc}/2$.

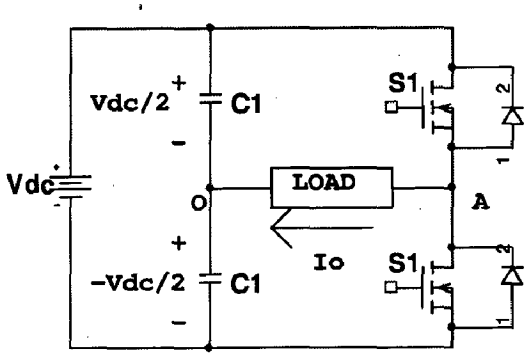


Fig. 3.2(a) Half Bridge Configuration

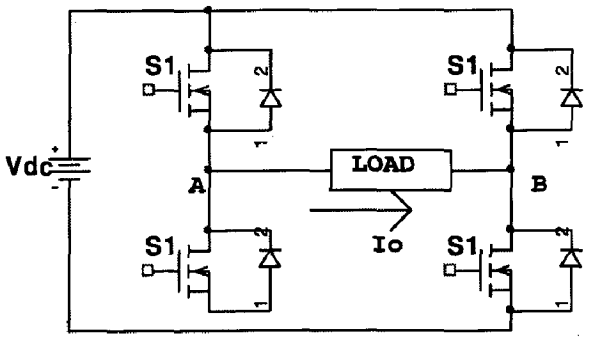


Fig. 3.2(b) Full Bridge Configuration

Note that S_1 and S_3 should not be closed at the same time, nor should S_2 and S_4. Otherwise, a short circuit would exist across the dc source. The output waveform of half-bridge and full-bridge of single-phase voltage source inverter are shown in Fig. 3.3(a) and 3.3(b) respectively.

Conducting Switches	Load Voltage V_{AB}
S1,S4	$+V_{dc}$
S2,S3	$-V_{dc}$
S_1,S_2 or S_3,S_4	0

Table 3.2 Load Voltage With Corresponding Switching States

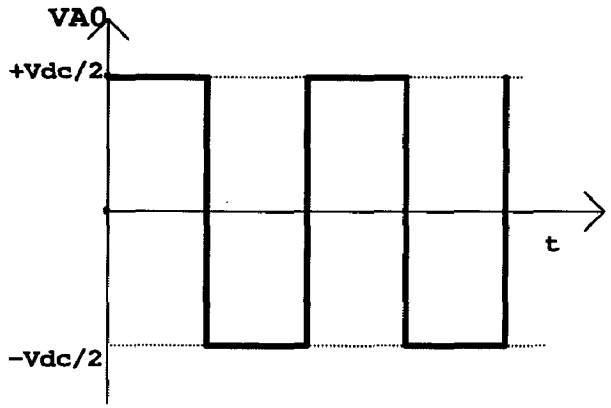


Fig. 3.3(a) Output waveform of half-bridge configuration.

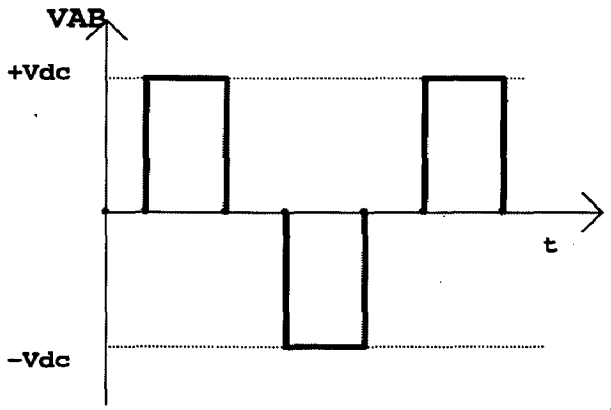


Fig. 3.3 (b) Output waveform of Full-bridge configuration.

Advantages

1. Simple and proven technology
2. Same converter design over supply voltage range
3. Standard fully developed PWM Control

Disadvantages

1. Static and dynamic voltage sharing of series devices
2. High dv/dt due to synchronous commutation of series devices
3. High switching frequency harmonic content in inverter output voltage.

Three-Level Neutral Point Clamped MLI

In case of the conventional two-level inverter configuration, the harmonic contents reduction of an inverter output current is achieved mainly by raising the switching frequency. However in the field of high voltage, high power applications the switching frequency of the power device has to be restricted below 1 KHz, even with the HVIGBT and GCT, due to the increased switching loss. So the harmonic reduction by raised switching frequency of a two-level inverter becomes more difficult in high power applications. In addition, as the dc link voltage of a two-level inverter is limited by voltage ratings of switching devices, the problematic series connection of switching devices is required to raise the dc link voltage. By series connection, the maximum allowable switching frequency has to be more lowered, thus the harmonic reduction becomes more difficult.

From the aspect of harmonic reduction and high de-link voltage level; three-level approach seems to be the most promising alternative. The harmonic contents of a three-level inverter are less than that of a two-level inverter at the same switching frequency and the blocking voltage of the switching device is half of the de-link voltage. So the three-level inverter topology is generally used in realizing the high performance, high voltage ac drive systems.

For power/high voltage applications, the NPC inverter has advantages such that the blocking voltage of each switch is clamped to the half of DC –link voltage and the output voltage and current waveforms contain low harmonics compared to the conventional two -level inverter operating with the same switching frequency.

Fig 3.4 shows the circuit of a Neutral Point Clamped Three Level, three - phase inverter using MOSFET devices. The dc link capacitor C has been split to create the neutral point 0. A pair of devices with bypass diodes is connected in series with an additional diode connected between the neutral point and the center of the pair. The

devices S_{1U} and S_{4U} function as main devices (like two level inverter), and S_{2U} and S_{3U} function as auxiliary devices which help to clamp the output potential to the neutral point with the help of clamping diodes D_1 and D_2.

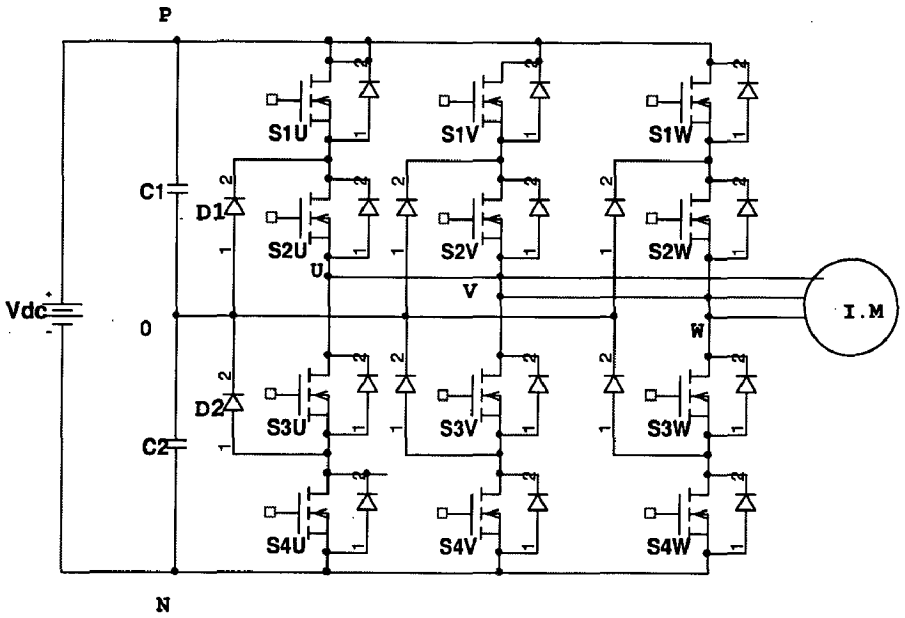


Fig 3.4 Neutral Point Clamped Three-level Inverter

The harmonic contents of a three-level inverter are less than that of a two-level inverter at the same switching frequency and the blocking voltage of the switching device is half of the de-link voltage.

However, the concept of three level inverter introduced a new zero voltage level (also called neutral point), other than the positive and negative voltage levels in comparison to two level inverter. This type of DC links inherently associated with neutral point variations and results in a voltage unbalance problems between the lower and upper capacitor dc-link capacitors, causing undesirable uneven voltage stress at the upper and lower array of switching elements[9][23][26]. The inherent neutral point potential variation of a three-level inverter has to be effectively suppressed to fully utilize the advantages of three-level inverter. More complex PWM control is needed than 2-level. And requires mid point voltage balance control and neutral point voltage control. So many PWM techniques have been proposed in literature [22], [23], [25] and [26] to solve the above mentioned problems.

Multilevel Inverters

Since these are of three types, viz., Diode clamped multilevel inverter (DCMLI), Capacitor clamped (CCMLI) (or flying capacitor) multilevel inverter and Cascaded multi cell inverters, an overall comparison is made here [2],[3] and [12].

The advantages are

- Reduced harmonic content.
- Reduced dv/dt.
- Snubberless operation (for CCMLI).
- Modular design.
- Low switching frequency devices.
- Low switching losses.
- High voltage/power output with reduced rating of individual devices.

The disadvantages are

- Large device count(DCMLI)
- Complex PWM control.
- Requirement of split DC link.
- Voltage balancing of DC link capacitors.
- Series redundancy difficult to achieve.
- Separate DC link sources(for ISHB)
- Uneven current stresses on power devices.

3.4 CLASSIFICATION OF MULTI LEVEL INVERTRS

3.4.1. DIODE-CLAMPED MULTI-LEVEL INVERTER (DCMLI)

A three-level diode-clamped inverter is shown in Fig 3.5(a). In this circuit, the dc-bus voltage is split into three levels by two series-connected bulk capacitors, C_1 and C_2. The middle point of the two capacitors n can be defined as the neutral point. The output voltage V_{an} has three states: $V_{dc/2}$, 0, and $-V_{dc/2}$. For voltage level $V_{dc}/2$, switches $S_1$and S_2 need to be turned on; for $-V_{dc/2}$, switches S_1' and S_2' need to be turned on; and for the 0 level, S_2 and S_1' need to be turned on.

The key components that distinguish this circuit from a conventional two-level inverter are D_1 and D_1'. These two diodes clamp the switch voltage to half the level of the dc-bus voltage. When both S_1 and S_2 turn on, the voltage across a and n is V_{dc}, i.e., $V_{an} = V_{dc}$. In this case, d_1 balances out the voltage sharing between S_1' and S_2' with S_1' blocking the voltage across C_1 and S_2' blocking the voltage across C_2. Notice that output voltage v_{an} is ac, and v_{a0} is dc. The difference between v_{an} and v_{a0} is the voltage across C_2, which is $V_{dc/2}$.

Fig. 3.5(b) shows a five-level diode-clamped converter in which the dc bus consists of four capacitors, C1, C_2, C_3, and C4. For de-bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/4$, and each device voltage stress will be limited to one capacitor voltage level $V_{dc/4}$ through clamping diodes.

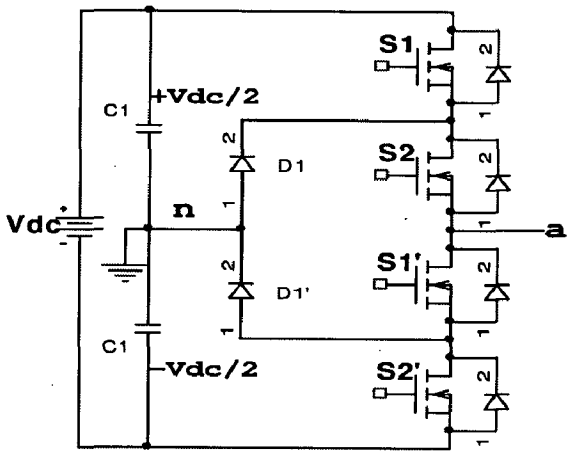


Fig 3.5(a) 3-level Diode-clamped Inverter

Although each active switching device is only required to block a voltage level of $V_{dc}/(m - 1)$ where m is number of levels, the clamping diodes must have different voltage ratings for reverse voltage blocking. Using d_1 of Fig. 3.5(b) as an example, when lower devices S_2' to S_4' are turned on, D_1 and needs to block three capacitor voltages, or 3 $V_{dc/4}$. Similarly, D_2 and D_2' need to block $2V_{dc/4}$, and D_3 and D_3' needs to block 3 $V_{dc/4}$. Assuming that each blocking diode voltage rating is the same as the active device voltage rating, the number of diodes required for each phase will be (m — 1) x (m—2). This number represents a quadratic increase in *m*. When *m* is sufficiently high, the number of diodes required will make the system impractical to implement. If the inverter runs under

PWM, the diode reverse recovery of these clamping diodes becomes the major design challenge in high-voltage high-power applications.

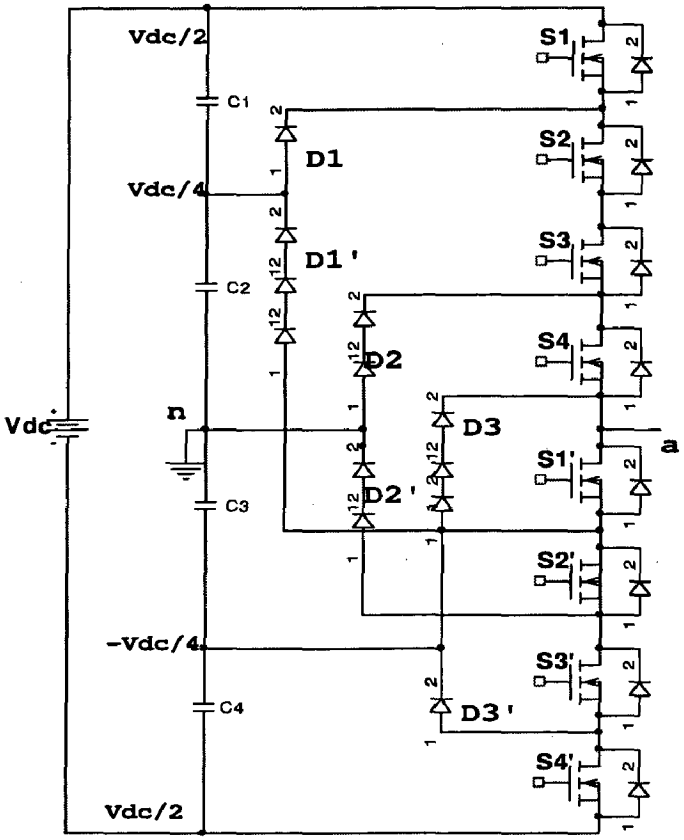


Fig3.5 (b) 5-level Diode Clamped Inverter

There are 5 switch combinations to synthesize five level voltages across *a* and *n*.

Output	S_1	S_2	S_3	S_4	S_1^1	S_2^1	S_3^1	S_4^1
V_{dc}	1	1	1	1	0	0	0	0
$V_{dc/4}$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$-V_{dc/4}$	0	0	0	1	1	1	1	0
$-V_{dc/2}$	0	0	0	0	1	1	1	1

Table. 3.3. Switching Combinations Vs Output Voltage

Unequal device rating and Capacitor Voltage Unbalance

The switch S1 conducts only during $V_{a0}= V_{dc/2}$, while switch S_4 conducts over the entire cycle except $V_{ao}=0$. Such an unequal conduction duty requires different current for switching devices, the outer switches may be oversized and the inner switches may be undersized. A power needs to transfer real power from ac to dc (rectifier) or dc to ac (inverter). When operating at unity power factor, the charging time for rectifier operation or discharging time for inverter operation for each capacitor is different. The voltage unbalance problem is solved by several approaches, such as replacing capacitors by a controlled constant dc voltages source such as pulse width modulation (PWM) voltage regulators or batteries. The use of controlled dc voltage results in system complexity and cost penalties. The converter switching frequency should be kept, minimum to avoid switching losses and electromagnetic interference problems. When operating at zero power factor, the capacitor voltages can be balanced equal charge and discharge in one half cycle.

The voltage unbalance problem in multilevel inverter can be solved by several approaches proposed in the literature [8,9]. A simple solution would be to replace capacitors by constant DC voltage sources, voltage regulators or batteries. But this makes the system complex and costly.

In ref. [8] a simple method of balancing the capacitor voltages has been given. The method is based on buck-boost converter, where half cycle charging of inductors is used for compensating the loss of charge in the capacitors. The method although simple, requires extra components including inductors. Also it exposes the system to over –voltages that can damage the system devices.

In ref. [9], a method using the zero sequence current to control the capacitor voltages for a three-level inverter has been presented. The system is slightly complex and the complexity increases for higher levels.

In ref. [10], the generalized topology has been presented. The topology has a true modular structure with a basic cell and does not require extra components like clamping diodes and voltage balancing capacitors. The generalized topology presents a structure from which any type and any level inverter can be deduced with self voltage-voltage balancing. For higher levels the device count for this topology is excessive.

The diode-clamp Multi Level Inverter can be therefore summarized with the following advantages and disadvantages.

Advantages

- Large number of levels reduces the harmonic content and avoids the needs for filters.
- Since all devices are switched at fundamental frequency, the efficiency is high because of low switching losses.
- Reactive power flow can be controlled

Disadvantages

- For large number of levels, the number of clamping diodes required is very high,(m-1)x(m-2) for each phase for m-level inverter.
- Real power flow control is difficult for the individual converter.

3.4.2 CAPACITOR-CLAMPED MULTI-LEVEL INVERTER(CCMLI)

For high-voltage applications, some problems have been encountered while dealing with the practical control and implementation of main topologies. These include,

- Voltages unbalance between split dc capacitors.
- Indirect clamping of inner switching devices.
- Series connected clamping diodes.

To overcome these problems, a multilevel structure with flying capacitors was proposed. This approach obviously overcomes the limitation of diode-clamped multilevel inverters. The flying capacitor multilevel inverter has not been widely applied in industry. Nevertheless it seems that it has important advantages over the diode clamp multilevel converter. This is because it uses a clamping capacitor across a two-switch pair. In spite of this, there is a fundamental problem dealing with voltage balancing between flying capacitors and each leg under practical operation. This leads to voltage unbalance and thus, unsafe operation. For its balancing, FCMLI requires the symmetric switching of control signals with a phase shift. Up to now, there has been very little work done to solve a fundamental problem in the FCMLI applications. Since most of the

research was focused on uni-directional dc-dc converter applications, this problem was not considered to be a major concern.

Through simulation and experimentation, it was discovered that this topology is not available for bi-directional applications without adding a passive voltage balancing circuit or voltage control loops. For voltage balancing between flying capacitors, various approaches can be considered using voltage stabilizers and switching modulations.

- First, controlling each capacitor voltage within a few cycles makes it possible to maintain a voltage balance.
- The capacitor voltage can be controlled by a modulation scheme, which introduces small changes in the switching instants. In this case, the suggested approach changes slight distortions to the voltage but allow selective charging of each capacitor without requiring an increase in the number of switching events.

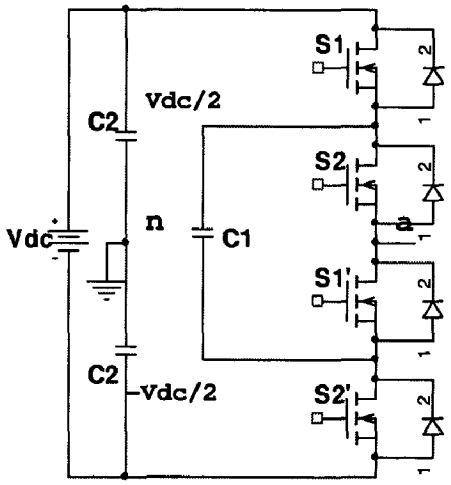


Fig 3.6(a) Three -level Capacitor Clamped MLI

Fig. 3.6(b) illustrates the fundamental building block of a phase-leg capacitor-clamped inverter. Clamping capacitor C_1 is charged when S_1 and S_1' are turned on, and is discharged when S_2 and S_2' are turned on. The voltage synthesis in a five-level capacitor-clamped converter has more flexibility than a diode-clamped converter. Using Fig. 3.2(b) as the example, the voltage of the five-level phase-leg *a* output with respect to the neutral point *n*, V_{an}, can be synthesized by the following switch combinations.

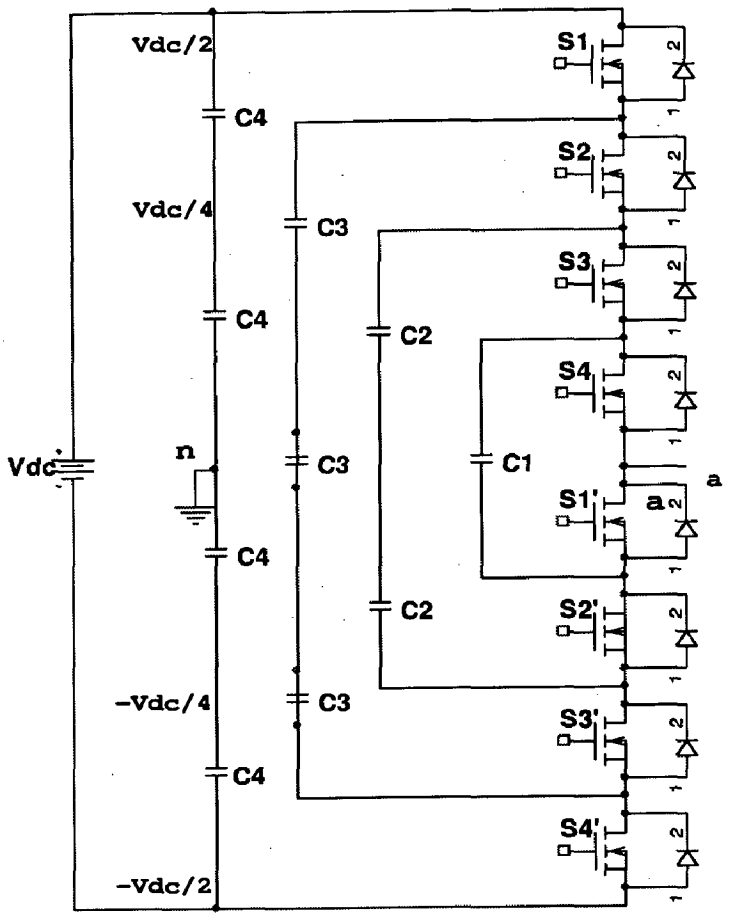


Fig 3.6(b) Five -level Capacitor Clamped MLI

1) For voltage level $V_{an} = V_{dc/2}$, turn on all upper switches S_1— S_4.

2) For voltage level $V_{an} = V_{dc/4}$, there are three combinations

   a) S_1, S_2, S_3, S_i' (V_{an} = $V_{dc/2}$ of upper C_4's-$V_{dc/4}$ of C_1);

   b) S_2, S_3, S_4, S_4' (V_{on} = $3V_{dc}/4$ of C_3's -Vdc/2 of lower C_4's) ; and

   c) S_1, S_3, S_4, S_3' (V_{an} = Vdc/2 of upper C_4's-$3V_{dc}/4$ of C_3's +$V_{dc}/2$ of C_4's).

3) For voltage level $V_{an} = 0$, there are six combinations:

   a) S_1, S_2, S_1', S_2' (V_{an} = $V_{dc}/2$ of upper C_4's-$V_{dc/2}$ of C_2's);

   b) S_3, S_4, S_3', S_4' (V_{an} = $V_{dc}/2$ of C_2 - $V_{dc/2}$ of lower C_4);

   c) S_1, S_3, S_1', S_3' (V_{an} = $V_{dc}/2$ of upper C_4's -$3V_{dc}/4$ of C_3's + $V_{dc}/2$ of C_2's - $V_{dc}/4$of C_1);

   d) S_1, S_4, S_2', S_3' (V_{on} = $V_{dc}/2$ of upper C_4's -$3V_{dc}/4$ of CVs + $V_{dc}/4$ of C_1);

e) S_2, S_4, S_2', S_4' (V_{an} = 3Vdc/4 of C_3's - V_{dc}/2 of C_2's +V_{dc}/4 of C_1- V_{dc}/2 of lower C_4's); and

f) S_2, S_3, S_1', S_4' (V_{an} = 3V_{dc}/4 of C_3's -V_{dc}/4 of C_1 -Vdc/2 of lower C_4's).

4) For voltage level V_{an} = -V_{dc}/4, there are three combinations:

a) S_1, S_1', S_2', S_3' (V_{an} = V_{dc} /2 of upper C_4's -3 V_{dc} /4 of C_3's);

b) S_4, S_2', S_3', S_4' (V_{an} = V_{dc} /4 of C_1 - V_{dc} /2 of lower C_4's); and

c) S_3, S_1', S_3', S_4' (V_{an} = V_{dc}/2 of C_2's - V_{dc} /4 of C_1 - V_{dc} /2 of lower C_4's).

5) For voltage level V_{an} = -V_{dc}/2, turn on all lower switches, S_1'-S_4'.

In the preceding description, the capacitors with positive signs are in discharging mode, while those with negative sign are in charging mode. By proper selection of capacitor combinations, it is possible to balance the capacitor charge. Similar to diode clamping, the capacitor clamping requires a large number of bulk capacitors to clamp the voltage. Provided that the voltage rating of each capacitor used is the same as that of the main power switch, an m-level converter will require a total of (m - 1) x (m - 2)/2 clamping capacitors per phase leg in addition to (m - 1) main de-bus capacitors.

Advantages

- Large no of storage capacitors provides extra ride through capabilities during power outage.
- Provides switch combination redundancy for balancing different voltage levels.
- When the no. of levels is high enough, harmonic content will be low enough to avoid the need for filters
- Both real and reactor power flow can be controlled.

Disadvantages

- An excessive no of storage capacitors is required when the no. of levels is high.
- The inverter control will be complicated and switching frequency losses will be high for real power transmission.

3.4.3. CASCADED MULTICELL INVERTERS:

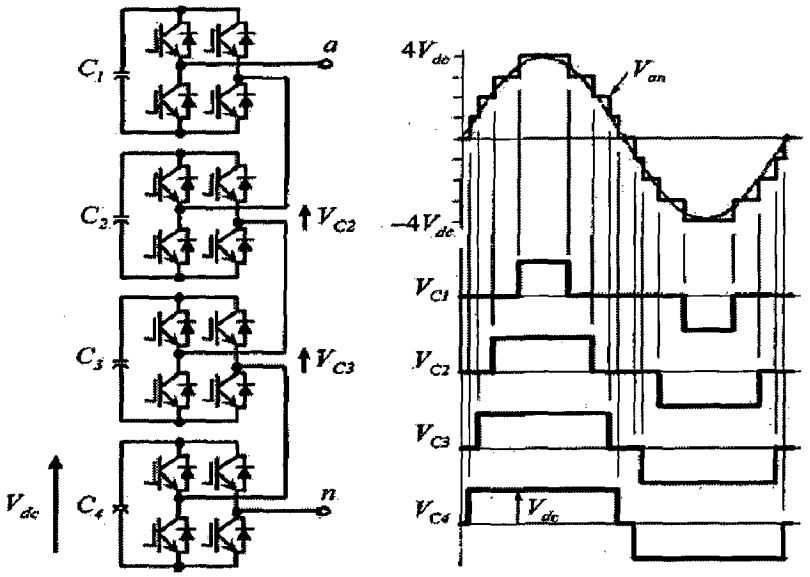


Fig3.7: Cascaded Inverter circuit Topology and its associated waveform

A different converter topology is introduced here, which is based on the series connection of single-phase inverters with separate dc sources [3]. Fig. 3.7 shows the power circuit for one phase leg of a nine-level inverter with four cells in each phase. The resulting phase voltage is synthesized by the addition of the voltages generated by the different cells. Each single-phase full-bridge inverter generates three voltages at the output: $+V_{dc}$, 0, and $-V_{dc}$. This is made possible by connecting the capacitors sequentially to the ac side via the four power switches. The resulting output ac voltage swings from $-4V_{dc}$ to $+4V_{dc}$ with nine levels and the staircase waveform is nearly sinusoidal, even without filtering.

Advantages

- Requires the least no. of components among all the multilevel inverters to achieve the same number of voltage levels
- Modularized circuit lay out and packaging is possible since each level has the same structure and there are no extra clamping diodes or voltage balancing capacitors.
- Soft switching is possible to avoid bulky and lossy resistor capacitor diode snubbers.

Disadvantages

- Needs separate dc sources for real power conversions and thus its applications are somewhat limited.

Inverter Configuration	Diode-clamped	Flying-capacitors	Cascaded-inverters
Main switching devices	2(m-1)	2(m-1)	2(m-1)
Main diodes	2(m-1)	2(m-1)	2(m-1)
Clamping diodes	(m-1)(m-1)	0	0
DC bus capacitors	(m-1)	(m-1)	(m-1)/2
Balancing capacitors	0	(m-1)(m-2)/2	0

Table.3.4 Comparison of power component requirements per phase leg among three multilevel inverters

CHAPTER-4

SIMULATION OF MULTI-LEVEL INVERTERS

In this chapter simulation of various inverters using sinusoidal pulse width modulation was carried out with the help of "MATLAB 6.5". The main objective of this chapter is to observe the improvement in the line voltage THD and Line Current THD for both R-L Load, Motor Load as the inverter level increases from 2-level to 5-level. V/f analysis of the drive has been done using 2-level, 3-level and 5-level inverters. Here it has been assumed that modulation index is proportional to output voltage of inverter.

$MI=K*V_1$ (V_1- Fundamental Component)

where k is constant. So for variable speed drive at different frequencies following quantities have been observed.

- Line Voltage waveform
- Line current waveform for both R-L load and Motor Load
- Variation of Line Voltage THD and frequency

Load Specifications:

(a) R-L load: R=10Ω, L=30mH

(b) Motor Load: 1 HP, RPM: 1440, Current: 2 Amps.

4.1. TWO-LEVEL INVERTER

In 2-level inverter one triangular wave is compared with one sine wave as shown in Fig 4.1. Fig 4.2(a) to Fig 4.2(f) shows the firing pulses to the six MOSFETs, phase voltage line voltage waveform and its harmonic spectrum, line current waveforms and its harmonic spectrum for both R-L load and Induction Motor load respectively.

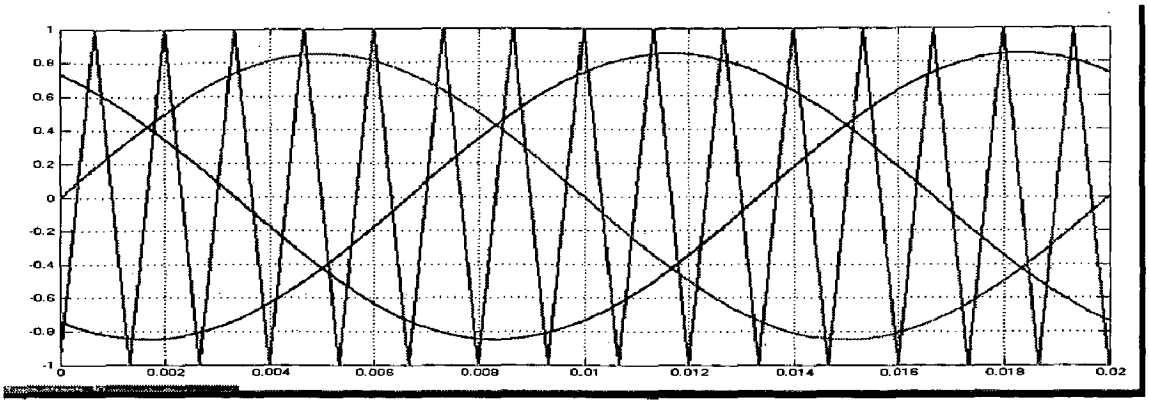


Fig. 4.1 Firing Pulse Generation to 2-level Inverter

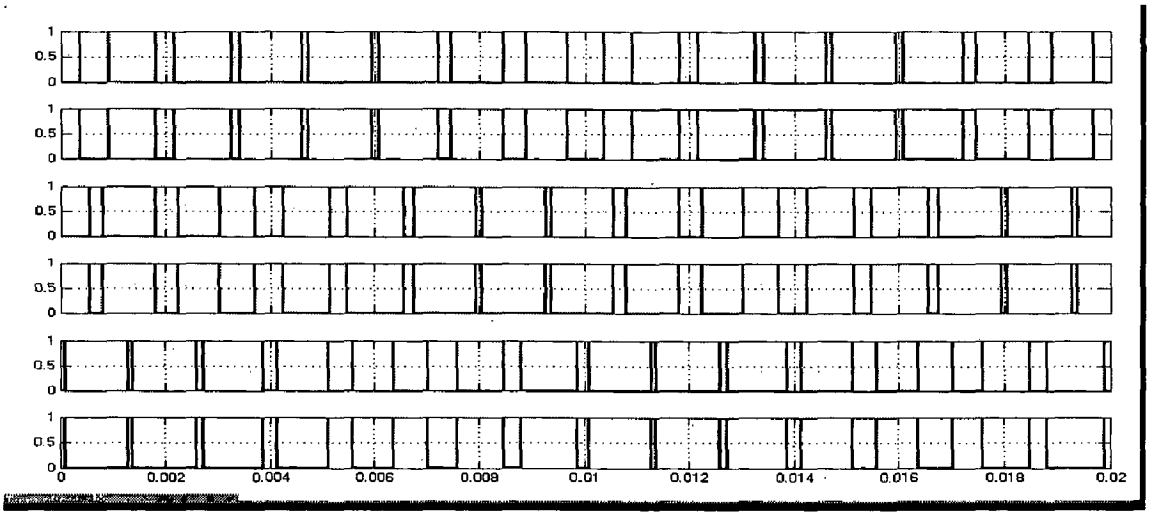


Fig. 4.2(a) Firing Pulses to Six MOSFETs S1, S4, S3, S6, S5, S2 from Top to Bottom

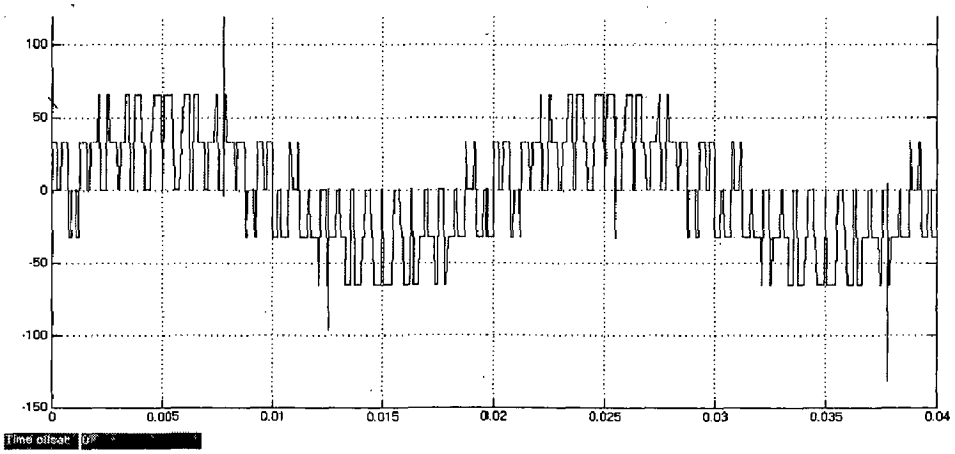


Fig 4.2(b) Phase Voltage at f=50Hz, MI=0.9, fr=15

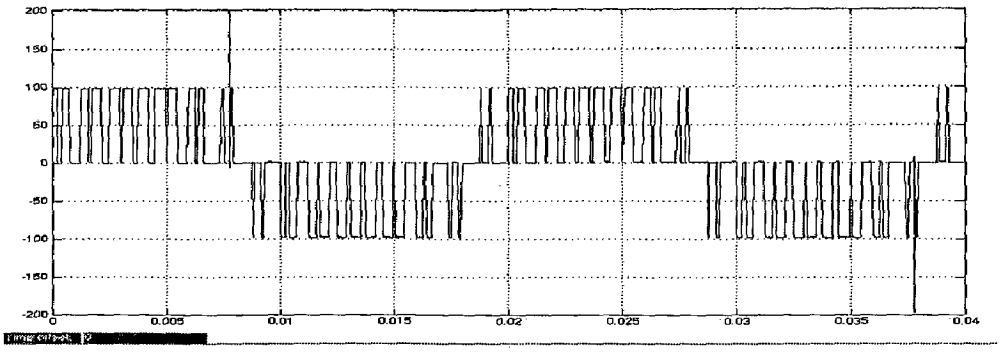


Fig 4.2(c) Line Voltage waveform at f=50Hz, MI=0.9,fr=15

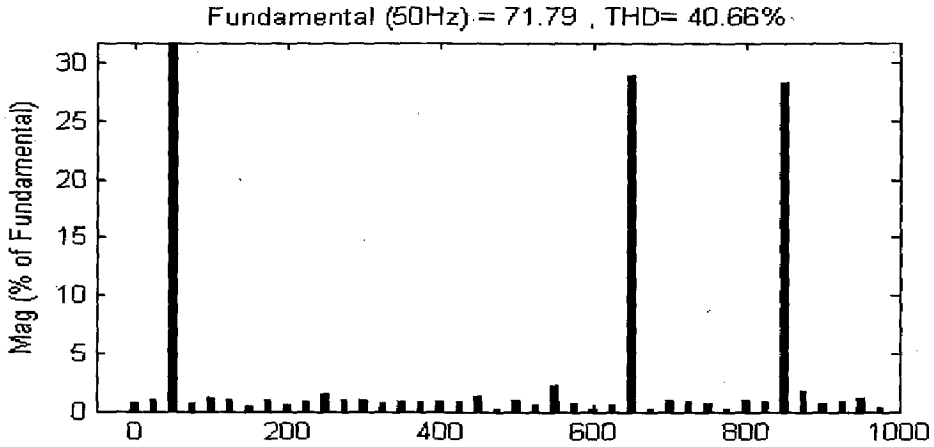


Fig. 4.2(d) Line Voltage Harmonic Spectrum at f=50 Hz

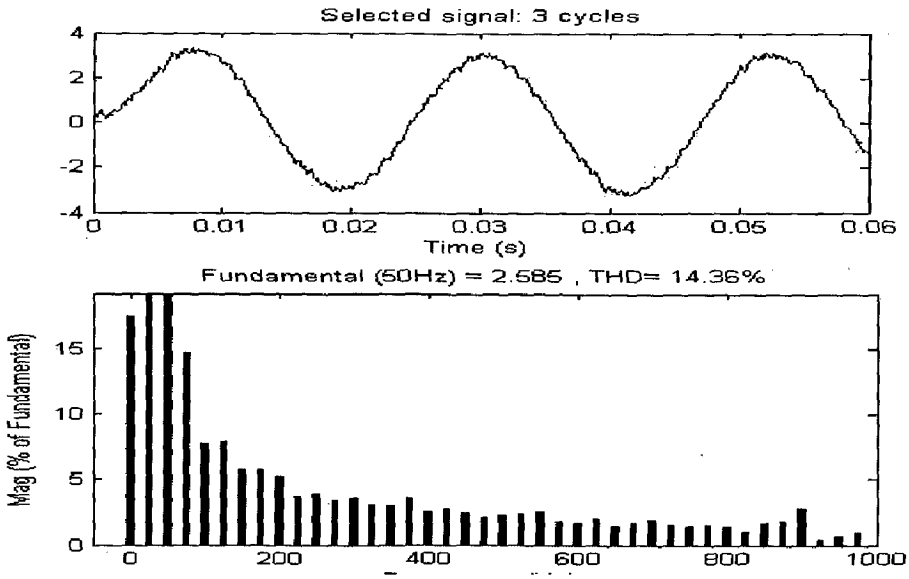


Fig. 4.2(e) Line current waveform and its harmonic spectrum(R-L Load)

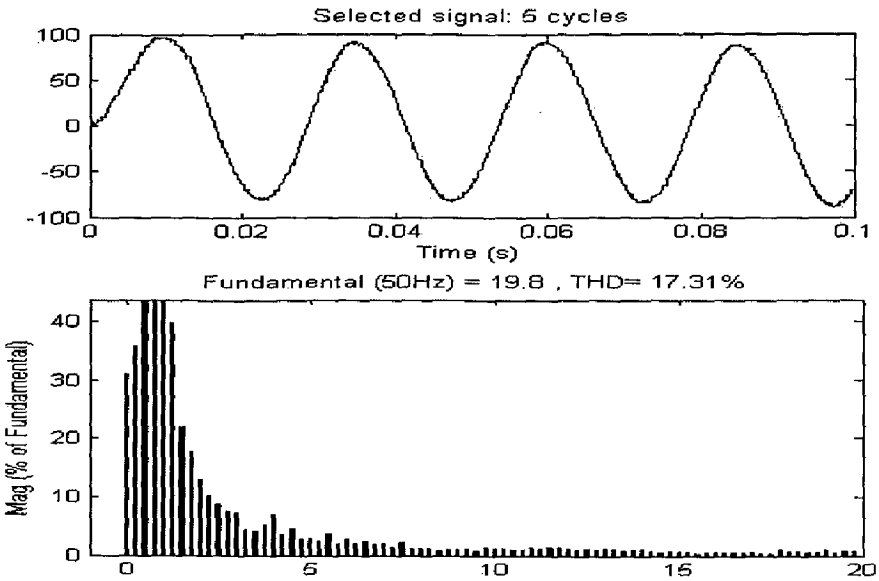


Fig. 4.2(f) Line current waveform and its harmonic spectrum (Motor Load)

Table 4.1 shows V/f analysis of Three-level Inverter along with the THD variation. Fig. 4.3 shows variation of 2-level Line voltage THD with the frequency.

Freq (Hz)	(MI)	Line Current THD%	Line Voltage THD %
50	0.9	14.36	40.66
45	0.81	19.32	45.83
40	0.72	30.00	55.98
35	0.63	35.73	60.23
30	0.54	45.47	82.76
20	0.36	50.04	98.53

Table 4.1 Analysis of Two-level Inverter as V/f drive

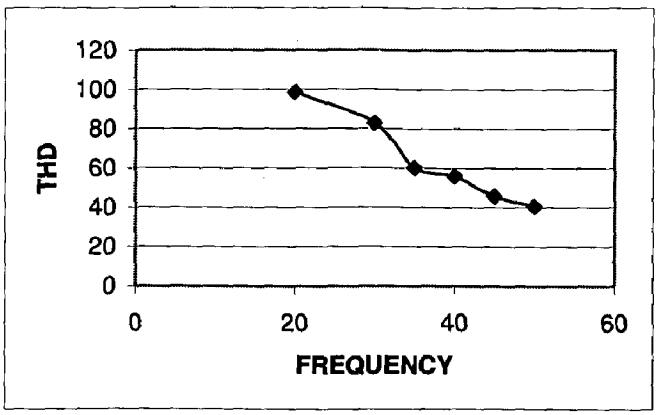


Fig 4.3 Two-Level Line Voltage THD Variation with Frequency

4.2. THREE-LEVEL INVERTER:

In 3-level inverter two triangular waves are compared with one sine wave as shown Fig 4.4. Firing pulses are generated according to logic given in previous chapter. Fig 4.5(a) to Fig 4.5(f) shows the firing pulses four MOSFETs in one phase, phase voltage line voltage waveform and its harmonic spectrum, line current waveforms and its harmonic spectrum for both R-L load and Induction Motor load respectively

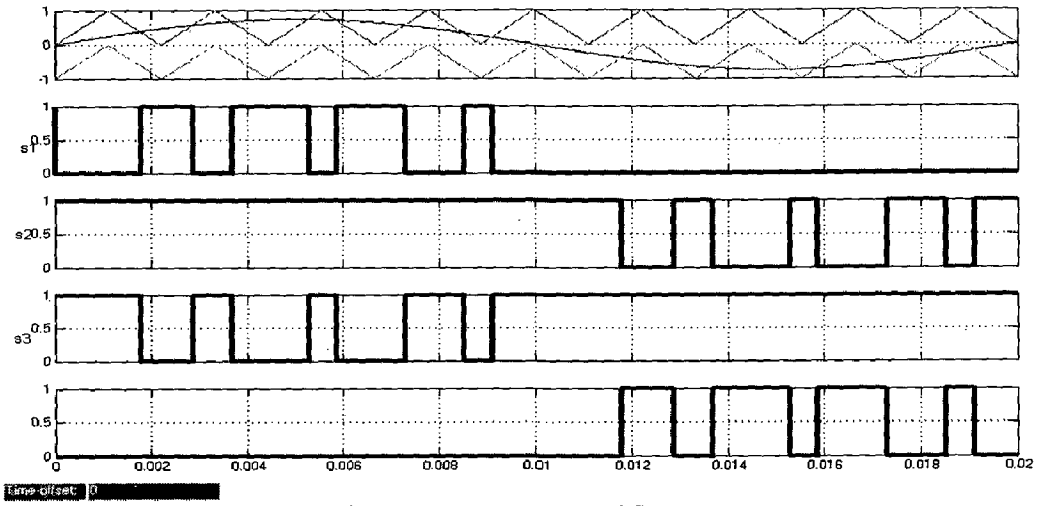


Fig. 4.5(a) Firing Pulses to 3-level Inverter

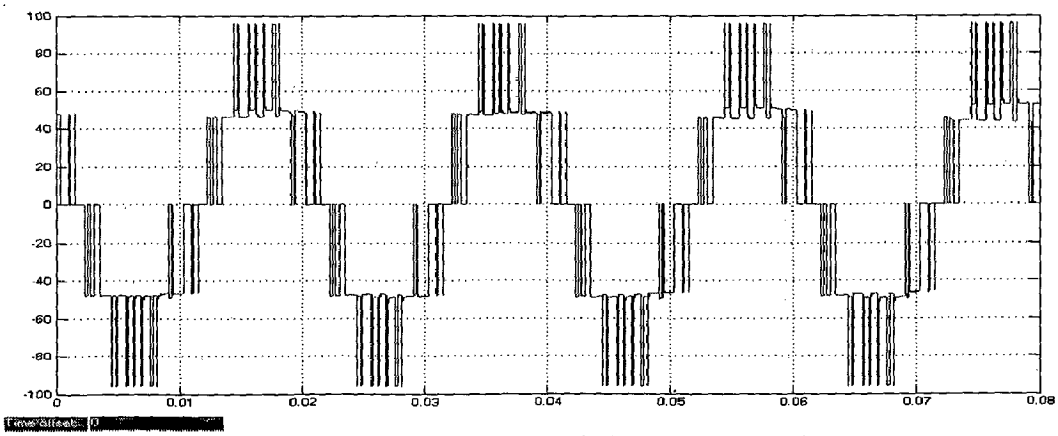


Fig. 4.5(b) Line Voltage for MI =0.75,fr=15, f=50

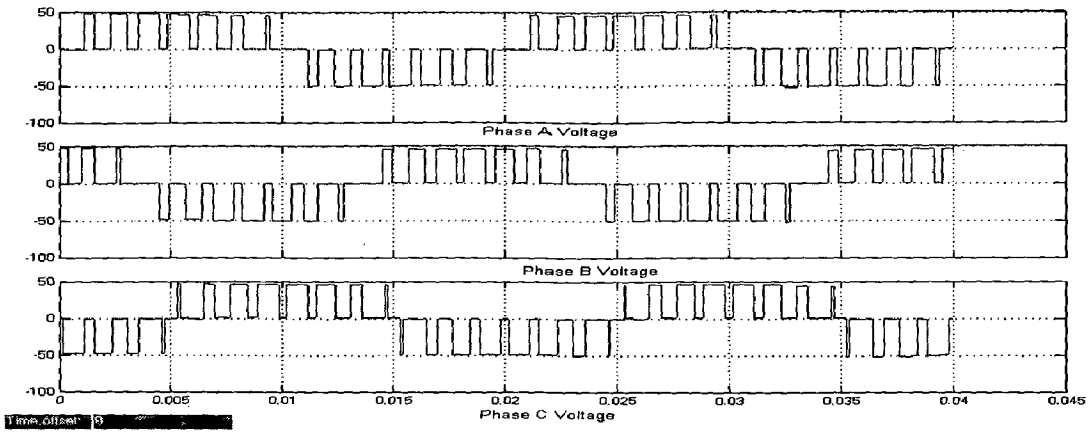


Fig. 4.5(c) Phase Voltage: for MI=0.75,fr=15, f=50

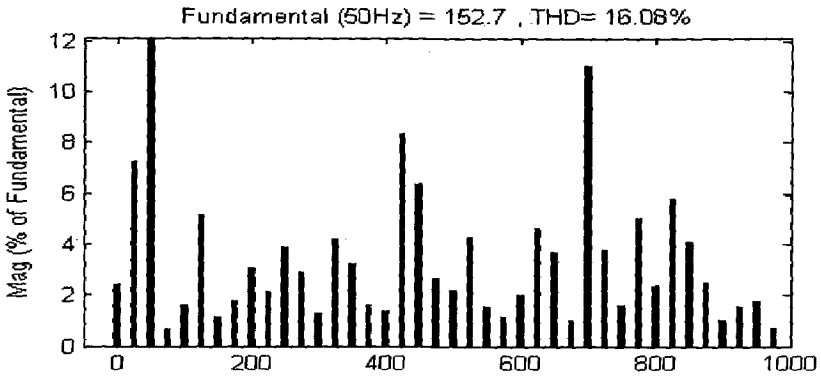


Fig 4.5(d) Harmonic Spectrum 3-Level Inverter f=50, MI=0.9, THD=16.08

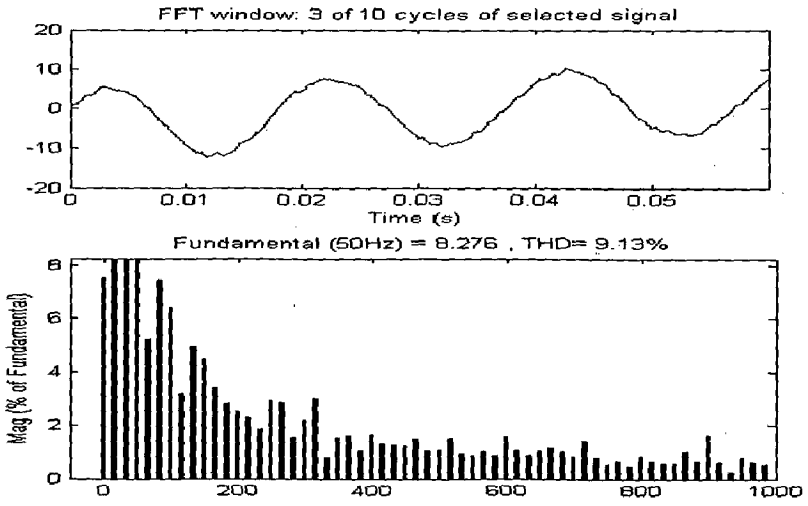


Fig. 4.5(e) Line Current and its harmonic spectrum

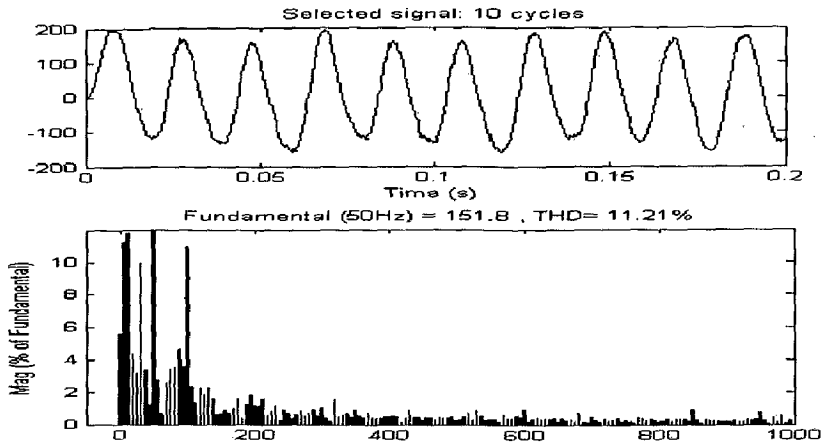


Fig. 4.5(f) Motor Line Current at 50 Hz and its THD

Table 4.2 shows V/f analysis of Three-level Inverter along with the THD variation. Fig. 4.6 shows variation of 3-level Line voltage THD with the frequency.

Freq (Hz)	(MI)	Line Current THD%	Line Voltage THD %
50	0.9	9.13	16.08
45	0.81	15.32	24.06
40	0.72	23.00	33.06
35	0.63	28.73	34.34
30	0.54	32.47	40.54
20	0.36	45.04	90.74

Table 4.2 Analysis of Three-level Inverter as V/f drive

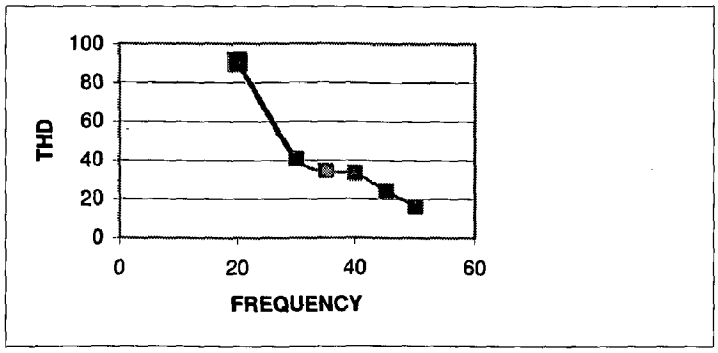


Fig. 4.6 Three-Level Line Voltage THD Variation with Frequency

4.3. FIVE-LEVEL INVERTER

In 5-level inverter shown in Fig. 3.6(b), four triangular waves are compared with one sine wave as shown in Fig 4.7. Firing pulses are generated according to logic given in Table. 3.3. Fig 4.8(a) to Fig 4.8(d) shows the firing pulses four MOSFETs in one phase, phase voltage, line voltage waveform and its harmonic spectrum for R-L load

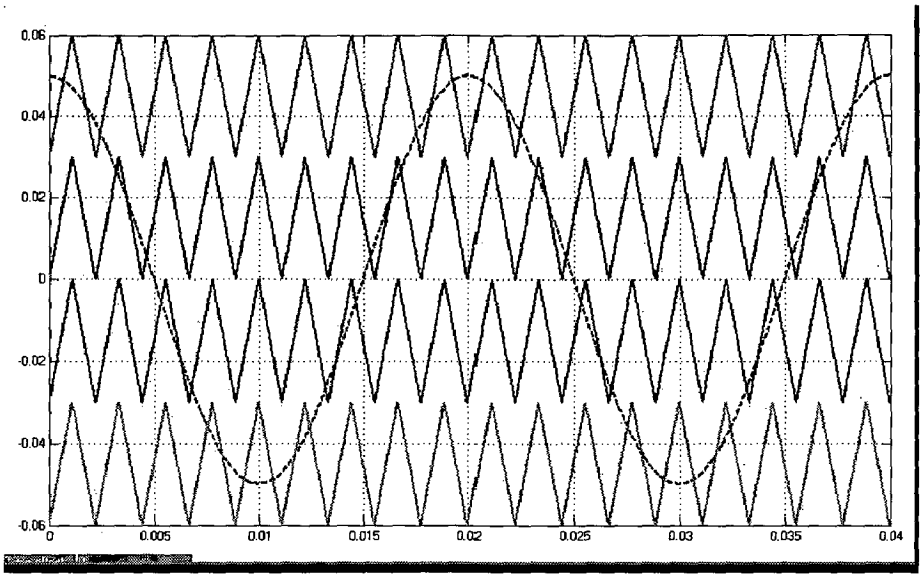


Fig. 4.7 Firing pulse generation to 5-level Inverter

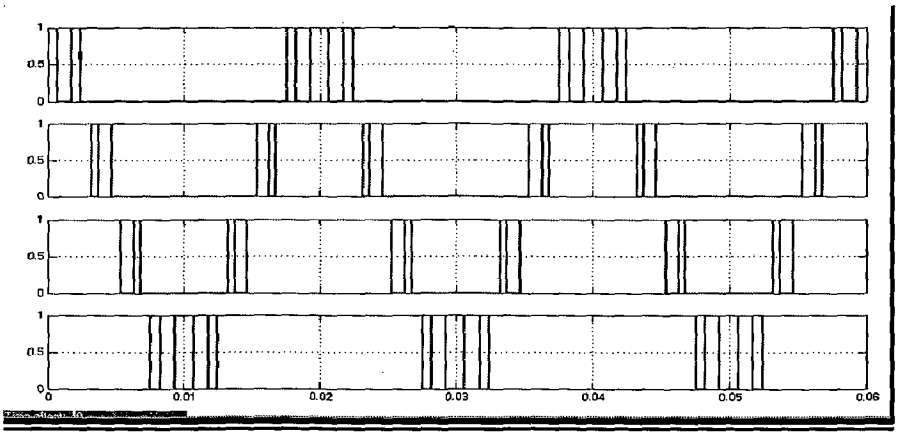


Fig. 4.8(a) Firing pulses for top 4 switches in 5-level inverter

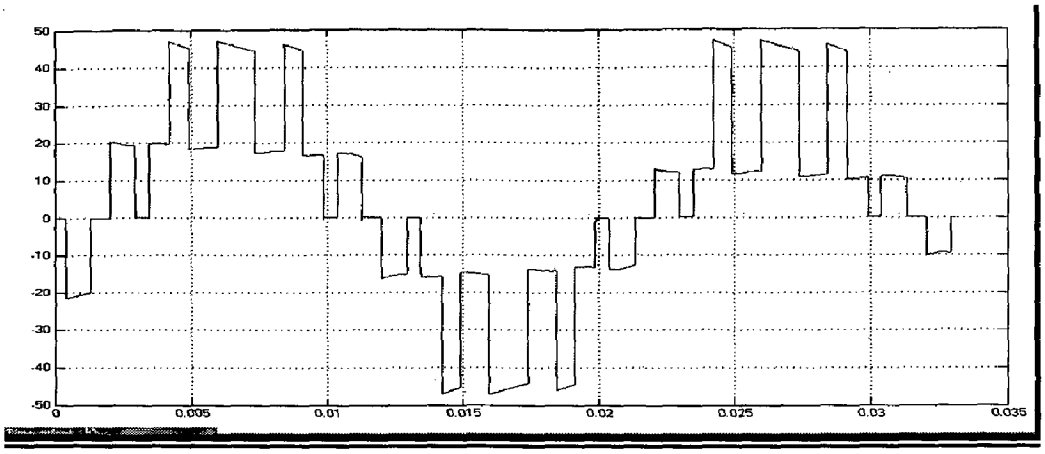


Fig 4.8(b) 5 level Phase Voltage MI=.85, f=50Hz,fr=15

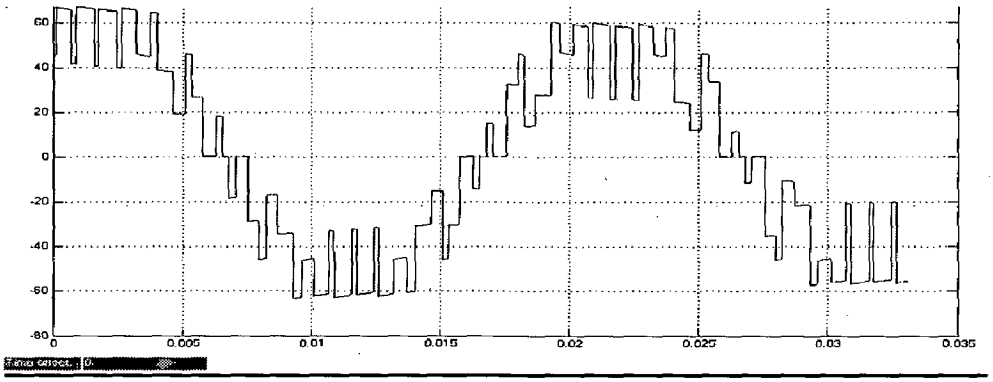


Fig 4.8(c) 5 level Line Voltage MI=.85, f=50Hz, fr=15

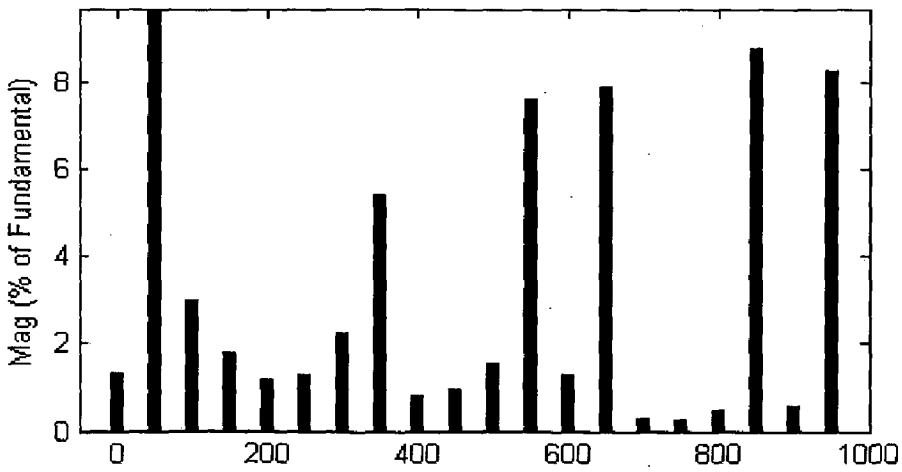


Fig. 4.8(d) Line Voltage Harmonic Spectrum at f=50Hz, MI=0.9, THD=10.22%

Table 4.3 shows V/f analysis of Three-level Inverter along with the THD variation.
Fig. 4.9 shows variation of 5-level Line voltage THD with the frequency

Fq (Hz)	(MI)	Line Voltage THD %
50	0.9	10.22
45	0.81	15.56
40	0.72	25.03
35	0.63	32.34
30	0.54	45.54
20	0.36	60.74

Table 4.3 Analysis of Five-level Inverter as V/f drive

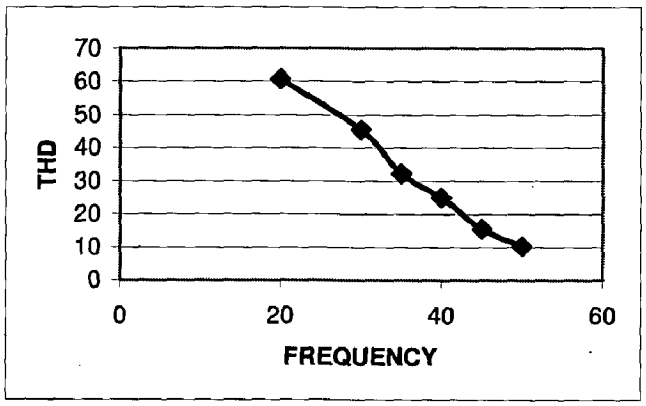


Fig. 4.9 Five-Level Line Voltage THD Variation with Frequency

Comparison of 2-level, 3-level and 5-level inverters

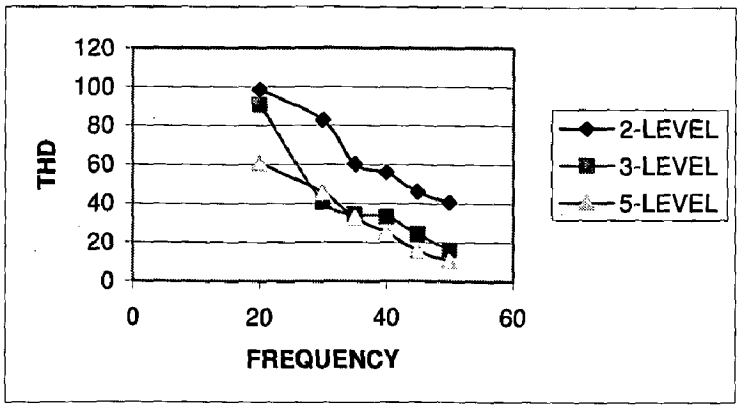


Fig. 4.10 Line Voltage THD Variation with Frequency for All Inverters

CHAPTER 5

PULSE WIDTH MODULATION TECHNIQUES

This chapter discusses the various PWM techniques available for Multi-level inverters and their implementation. The main objective of this chapter is, digital implementation of Space Vector Pulse Width Modulation Technique (SVPWM) for both Three-phase inverter and Neutral-point Clamped Inverter.

5.1. INTRODUCTION

PULSEWIDTH modulation (PWM) has been studied extensively during the past decades. This relatively unsophisticated method employs a triangular carrier wave modulated by a sine wave and the points of intersection determine the switching points of the power devices in the inverter. However, this method is unable to make full use of the inverter's supply voltage and the asymmetrical nature of the PWM switching characteristics produces relatively high harmonic distortion in the supply. Many different PWM methods have been developed to achieve the following aims: wide linear modulation range; less switching loss; less total harmonic distortion (THD) in the spectrum of switching waveform; and easy implementation and less computation time. For a long period, carrier-based PWM methods [15][16] were widely used in most applications. A more advanced algorithm like Space Vector Modulation overcomes the drawbacks of Sine PWM algorithm and increases the overall system efficiency. Space Vector PWM (SVPWM) is a more sophisticated technique for generating a fundamental sine wave that provides a higher voltage to the motor and lower total harmonic distortion, it is also compatible for use in vector control (Field orientation) of AC motors.

5.2. SINUSOIDAL PULSE WIDTH MODULATION (SPWM)

Pulse-Width Modulation has been coded as one of the most economical method of voltage and frequency control [17]. Though this method, the conduction time of the switching transistor can be varied on and off to regulate the output voltage to a predetermined value. One particularly elegant process is illustrated in figure 1-4 with the

resulting PWM waveform shown in Fig 5.1(a). An oscillator is used to generate a triangular carrier waveform at the switching frequency, Vtri. A modulated function, Vref,

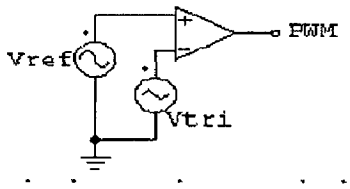


Fig 5.1(a) **Triangle comparison PWM implementation**

is generated separately and both applied to a comparator. The comparator generates a high output if V_{ref} is greater than V_{tri} and a low output when V_{tri} is greater than V_{ref}. Hence the output can be interpreted directly as a switching function. Moreover, since the triangle waveform has a voltage linearly dependent on time, the comparator has an output pulse width linearly dependent on the level of V_{ref}.

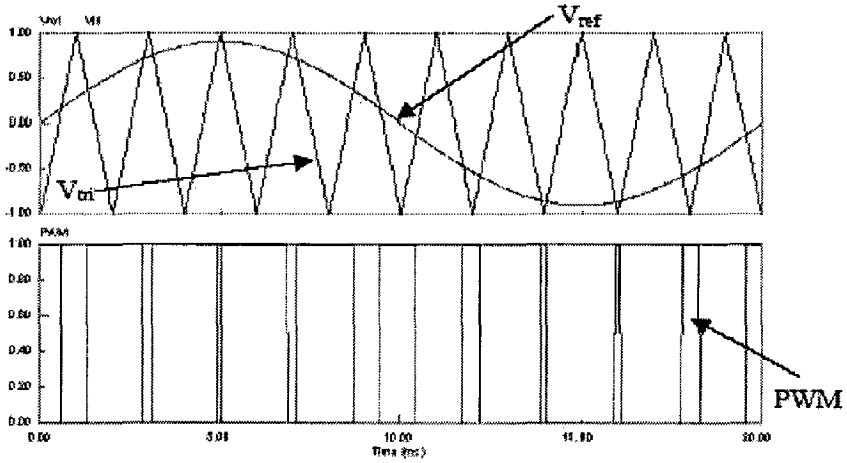


Fig 5.1(b) Resulting waveforms from PWM implementation

Advantages of PWM inverters

PWM inverters are mostly operated at low and medium switching frequencies and are the dominant technology used by industry. Some of its many advantages can be summarized into main points as [18]:

- Relatively simple and robust power circuit
- Low manufacturing cost
- Simple voltage and control techniques

PWM inverter disadvantages

As mentioned earlier, most PWM inverters operate at low and medium switching frequency levels, a reason for this is that such converters need to switch rapidly to minimize loss. Any attempt to increase switching frequencies will also follow in an increase of switching loss and an increase in the generation of electromagnetic interference. Thus switching losses become a critical problem in PWM topologies.

5.3. EXISTING MULTILVEL CARRIER BASED METHODS

Leon M. Tolbert, Thomas G. Habetler in their publication[19] titled "Novel Multilevel Inverter carrier based PWM methods" presented two novel carrier based multi-level PWM schemes are presented along with the existing PWM techniques which are carrier-based method termed Switching Frequency Optimal PWM (SFO-PWM), Sub Harmonic PWM technique (SHPWM) and Carrier Phase Angel Effect on Switching.

SUBHARMONIC PWM METHOD

Many authors have extended 2-level carrier based PWM techniques to multilevel inverters by making the use of several triangular carrier signals and one reference signal per phase[19][20]. For an m-level inverter, m-1 carriers with same switching frequency f_c and same peak-to-peak amplitude A_c are disposed such that the bands they occupy are contiguous. The reference, or modulation, waveform has peak-to-peak amplitude Am and frequency F_m, and it is centered in the middle of carrier set. The reference is continuously compared with each of carrier signals. If the reference is greater than a carrier signal, then the active device corresponding to that carrier is switched on; and if the reference is less than a carrier signal, then the active device corresponding to that carrier is switched off. In multilevel inverters, the amplitude modulation index, m_a, and the frequency ration, m_f are defined as

$$m_a = \frac{A_m}{(m-1).A_c} \tag{5.1}$$

$$m_f = \frac{f_c}{f_m} \tag{5.2}$$

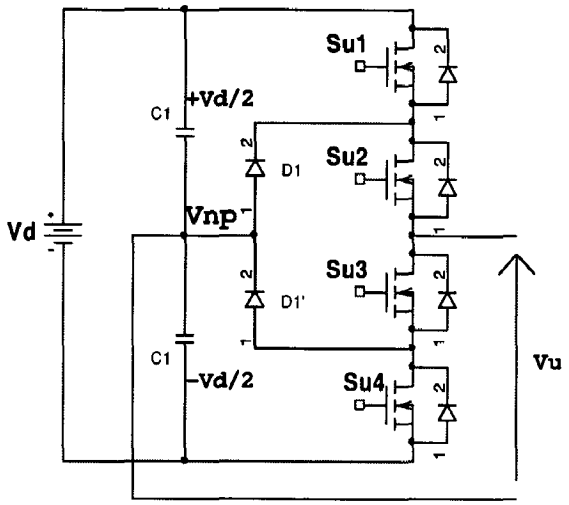


Fig. 5.2(a) One leg of the NPC inverter

Fig. 5.2(a) shows one-phase of NPC Inverter; two carriers are needed to implement the PWM control of NPC inverter [20] as shown in Fig. 5.2(b)

The main switches are S_{u1}, S_{u4} while S_{u2}, S_{u3} are auxiliary switches and along with D_1, D_1^1 are used to clamp the output terminal potential to the neutral point potential. The auxiliary switches S_{u1}, S_{u3} are driven complementary to the main switches Su4, Su1 respectively. As a result, three levels of output potentials are possible:

1. when S_{u1}, S_{u2} are on the output voltage is $+Vd/2$
2. when S_{u2}, S_{u3} are on the output voltage is 0 ·
3. when S_{u4}, S_{u3} are on the output voltage is $-Vd/2$.

Below Fig 5.3 shows a set of carriers in phase (m_f = 21) with all of the carriers in phase for a six-level diode-clamped inverter and a sinusoidal reference voltage with ma = 0.8[19]. The resulting output voltage of the inverter is also shown in Fig.5.3

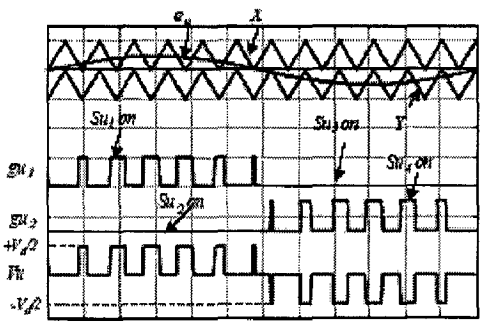


Fig 5.2(b) Control of one of the NPC Inverter

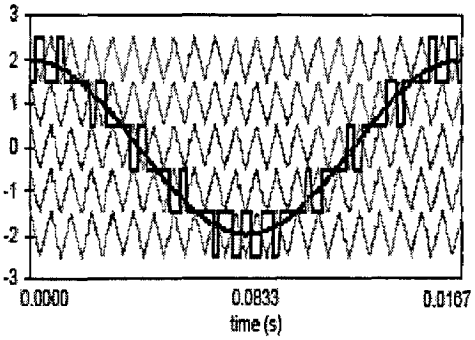


Fig 5.3 Multilevel carrier based SH-PWM for 6-level Inverter

5.4 SPACE VECTOR MODULATION AND ITS DIGITAL IMPLEMENTATION

5.4.1. INTRODUCTION

Pulse Width Modulation technique is used to generate the required voltage or current to feed the motor or phase signals. This method is increasingly used for AC drives with the condition that the harmonic current is as small as possible and the maximum output voltage is as large as possible. Generally, the PWM schemes generate the switching position patterns by comparing three-phase sinusoidal waveforms with a triangular carrier. In recent years, the space vector theory demonstrated some improvement for both the output crest voltage and the harmonic copper loss. The maximum output voltage based on the space vector theory is $2/\sqrt{3}$ times as large as the conventional sinusoidal modulation. The space-vector PWM (SVM) method is an advanced, computation-intensive PWM method and is possibly the best among all the PWM techniques for variable-frequency drive applications. Because of its superior performance, it has been finding widespread application in recent years. It enables to feed the motor with a higher voltage than the easier sub-oscillation modulation method. This modulator allows a higher torque at high speeds, and a higher efficiency. It also minimizes THD and switching loss. SVM is also scalar control. The controlled variables are motor voltage and motor frequency.

To understand the SVM theory, the concept of a rotating space vector discussed in [29] is very important. For example, if three-phase sinusoidal and balanced voltages given by the equations

$$V_a = V_m \cos(\omega t)$$

$$V_b = V_m \cos\left(\omega t - \frac{2\Pi}{3}\right)$$

$$V_c = V_m \cos\left(\omega t + \frac{2\Pi}{3}\right)$$

Are applied to a three-phase induction motor, it is shown that the space vector V^* with magnitude V_m rotates in circular orbit at angular velocity ω, where the direction of rotation depends on the phase sequence of the voltages.

5.4.2 SPACE VECTOR MODULATION OF TWO-LEVEL INVERTER USING d-q MODEL

Switching patters and the basic space vectors

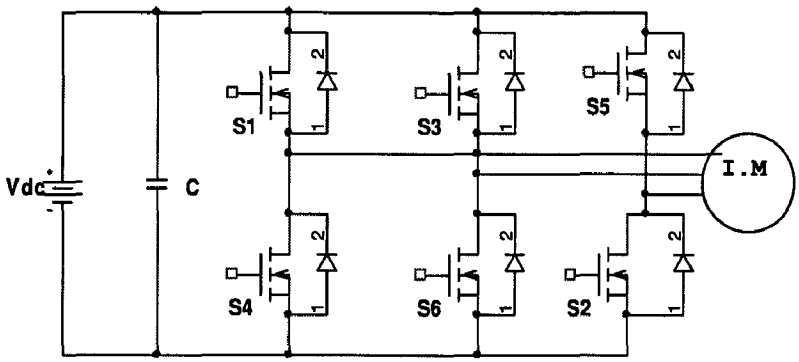


Fig.5.4. Three-phase Inverter

In the space vector PWM theory the motor voltage vector is approximated by a combination of 8 switching states of 3 upper power MOSFETs that feed the three phase power inverter[14][24]. The eight combinations and the derived output line-to-line and phase voltages are shown in Table 5.1.

State	On Devices	V_{an}	V_{bn}	V_{cn}	V_{ab}	V_{bc}	V_{ca}	Space Voltage Vector
0	$S_4S_6S_2$	0	0	0	0	0	0	$V_0(000)$
1	$S_1S_6S_2$	2/3	-1/3	-1/3	1	0	-1	$V_1(100)$
2	$S_1S_3S_2$	1/3	1/3	-2/3	0	1	-1	$V_2(110)$
3	$S_4S_3S_2$	-1/3	2/3	-1/3	-1	1	0	$V_3(010)$
4	$S_4S_3S_5$	-2/3	1/3	1/3	-1	0	1	$V_4(011)$
5	$S_4S_6S_5$	-1/3	-1/3	2/3	0	-1	1	$V_5(001)$
6	$S_1S_6S_5$	1/3	-1/3	1/3	1	-1	0	$V_6(101)$
7	$S_1S_3S_5$	0	0	0	0	0	0	$V_7(111)$

Table 5.1 Summary of Inverter Switching States

The inverter has six states when a voltage is applied to the motor and the states (0 and 7) when the motor is shorted through the upper and lower switches resulting in zero volts being applied to motor. It is useful to express these states as vectors. $V_{0\text{-}7}$ express three voltages V_{an}, V_{bn}, V_{cn} that are spatially separated 120^0 apart as a space vector, V_{out} for each of the switching states 0-7. The six vectors including of zero voltage vectors can be expressed geometrically as shown in Fig 5.5. The eight combinations are the derived

output line-to-line and phase voltages in terms of DC supply voltage V_{dc} according to Eqs., (5.3) and (5.4)

The relationship between the switching variable vector $[a \quad b \quad c]^T$ and the line-to-line voltage vectors $[V_{ab} \quad V_{bc} \quad V_{ca}]^T$ given by following

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = V_{dc} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \tag{5.3}$$

In addition phase (line-to-neutral) output voltage vector $[V_a \quad V_b \quad V_c]^T$ is given by equation

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{V_{dc}}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \tag{5.4}$$

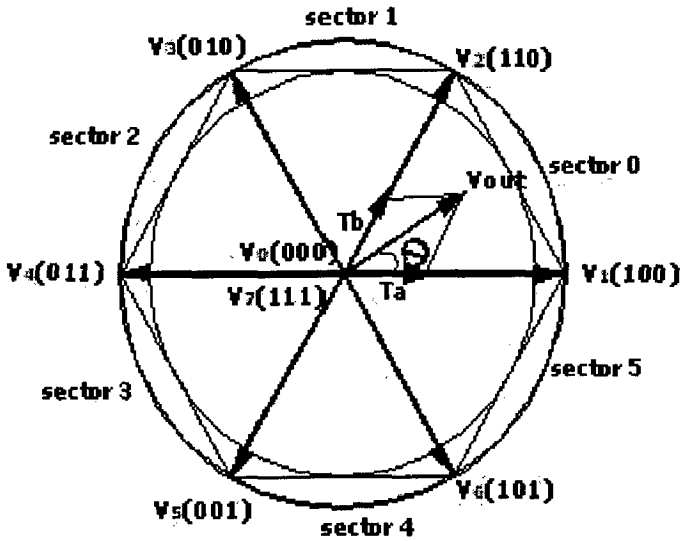


Fig.5.5 Space Vector Diagram

Expressions of the stator voltages in d-q frame

Assuming q and d are the horizontal and vertical axes of the stator coordinate frame the d-q transformation given in **Eq.,(5.5)** can transform a three-phase voltage vector into a vector in the d-q coordinate frame. The advantage using d-q analysis is, quantities in stator reference frame become the dc quantities in the synchronous rotating reference frame. This vector represents the special vector sum of the three-phase voltage. The phase voltages corresponding to the eight combinations of switching

patterns can be mapped into the d-q plane by the same d-q transformation as shown in Table.5.2. This mapping result in 6 nonzero vectors and two zero vectors. The non-zero vectors form the axes of hexagon as shown in Fig 5.5, the angle between any two adjacent non-zero vectors is 60^0.The group of 8 vectors are referred to as the basic state vectors and are denoted by V_0 through V_7. The d-q transformation can be applied to the reference a, b and c voltages to obtain the reference V_{out} in d-q plane as shown in Fig. 5.5

$$\begin{bmatrix} V_q \\ V_d \end{bmatrix} = \frac{2V_{dc}}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{5.5}$$

a	b	c	V_q	V_d	V_{dq}
0	0	0	0	0	$V_1=0$
1	0	0	$\frac{2}{3}V_{dc}$	0	$V_1=\frac{2}{3}V_{dc}$
1	1	0	$\frac{1}{3}V_{dc}$	$-\frac{1}{\sqrt{3}}V_{dc}$	$V_2=\frac{2}{3}V_{dc}$
0	1	0	$-\frac{1}{3}V_{dc}$	$-\frac{1}{\sqrt{3}}V_{dc}$	$V_3=\frac{2}{3}V_{dc}$
0	1	1	$-\frac{2}{3}V_{dc}$	0	$V_4=\frac{2}{3}V_{dc}$
0	0	1	$\frac{1}{3}V_{dc}$	$-\frac{1}{\sqrt{3}}V_{dc}$	$V_5=\frac{2}{3}V_{dc}$
1	0	1	$\frac{1}{3}V_{dc}$	$\frac{1}{\sqrt{3}}V_{dc}$	$V_6=\frac{2}{3}V_{dc}$
1	1	1	0	0	$V_7=0$

Table 5.2 Eight Switching States and Corresponding d-q Voltages.

The objective of the space vector PWM technique is to approximate the reference voltage vector V_{out} by a combination of the eight switching patterns. One simple means of approximation is to require the average output voltage of the inverter (in small period Ts)

to be the same as the average of V_{out} in the same period. For the output voltage in sector 0,where T_1 and T_2 are the respective durations in time for which switching patterns are V_1 and V_2,we can derive the following equation.

$$T_s V_{out} = T_1 V_1 + T_2 V_2 + T_0 (V_0 or V_7) \quad (5.6)$$

Where, $T_1+T_2+T_0=T_s$ (5.7)

The envelope the hexagon formed by space vectors is the locus of maximum V_{out}. Therefore the magnitude of the V_{out} must be limited to the shortest radius of this envelope because V_{out} is rotating vector. This gives a maximum magnitude of $V_{dc}/\sqrt{2}$ for V_{out}. The maximum rms values of the fundamental line-to-line and line-to-neutral output voltages are $V_{dc}/\sqrt{2}$ and $V_{dc}/\sqrt{6}$, these values are $2/\sqrt{3}$ times higher than what a standard sinusoidal PWM technique can generate.

Calculating the time periods of the switching states

The output voltage V_{out} can be in any of Sector 0 to Sector 5. Eqs. (5.6),(5.7) shows that for every Sampling Period T_s, V_{out} is approximated by switching between the two non-zero basic vectors that border the sector of current output voltage V_{out}. For instance if V_{out} is in sector 2, it can be approximated by switching the inverter between states V_3 and V_4 for periods of time T_3 and T_4 respectively. Because the sum of T_1 and T_2 should be less than or equal to Ts the inverter should remain in T_0 or T_7 for rest of period.

$$\begin{bmatrix} T_1 \\ T_2 \end{bmatrix} = T_s \begin{bmatrix} V_{1q} & V_{2q} \\ V_{1d} & V_{2d} \end{bmatrix}^{-1} \begin{bmatrix} V_{outq} \\ V_{outd} \end{bmatrix} \text{ or } \begin{bmatrix} T_1 \\ T_2 \end{bmatrix} = T_s M_0 \begin{bmatrix} V_{outq} \\ V_{outd} \end{bmatrix} \quad (5.8)$$

Where M_0 is the decomposition matrix. By substituting the values of V_{1q}, V_{2q}, V_{1d}, V_{2d} I can be found

$$\begin{bmatrix} T_1 \\ T_2 \end{bmatrix} = T_s \begin{bmatrix} \frac{2}{3} & \frac{1}{3} \\ 0 & \frac{-1}{\sqrt{3}} \end{bmatrix}^{-1} \begin{bmatrix} V_{outq} \\ V_{outd} \end{bmatrix} \quad (5.9)$$

The matrix inverse can be calculated before program execution for each sector and then obtained via a look-up table during execution. Doing so ensures smooth operation

because the calculation load on the Microprocessor is reduced. The following **Table.5.3** shows the sector numbers and the associated normalized decomposition matrix.

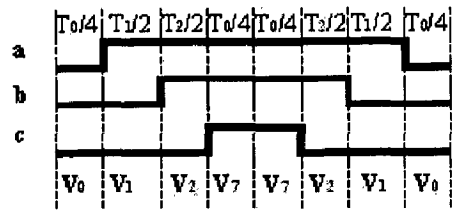
Sector	Durations	Decomposition Matrix
0	T_1 and T_2	$M_0 = \sqrt{3}\begin{bmatrix} \frac{\sqrt{3}}{2} & \frac{1}{2} \\ 0 & -1 \end{bmatrix}$
1	T_2 and T_3	$M_1 = \sqrt{3}\begin{bmatrix} \frac{-\sqrt{3}}{2} & \frac{-1}{2} \\ \frac{\sqrt{3}}{2} & \frac{-1}{2} \end{bmatrix}$
2	T_3 and T_4	$M_2 = \sqrt{3}\begin{bmatrix} 0 & -1 \\ \frac{-\sqrt{3}}{2} & \frac{-1}{2} \end{bmatrix}$
3	T_4 and T_5	$M_3 = \sqrt{3}\begin{bmatrix} 0 & 1 \\ \frac{-\sqrt{3}}{2} & \frac{-1}{2} \end{bmatrix}$
4	T_5 and T_6	$M_4 = \sqrt{3}\begin{bmatrix} \frac{-\sqrt{3}}{2} & \frac{1}{2} \\ \frac{\sqrt{3}}{2} & \frac{1}{2} \end{bmatrix}$
5	T_6 and T_1	$M_5 = \sqrt{3}\begin{bmatrix} \frac{-\sqrt{3}}{2} & \frac{-1}{2} \\ 0 & 1 \end{bmatrix}$

Table 5.3 Decomposition Matrix Vs Sector

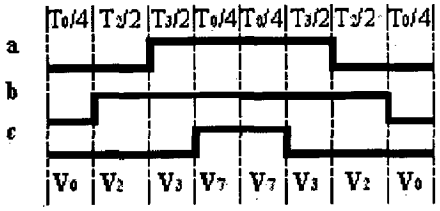
SVPWM switching pattern

The order of the non-zero vectors and zero vectors in each PWM period must be determined. Different switching orders result in different waveform patterns. Fig5.3 shows the waveforms produced for each sector of a symmetric switching scheme and Table5.4 and Table 5.5 shows the sequence of vectors and its firing commands for each sector respectively. Each waveform and sector has the following properties.

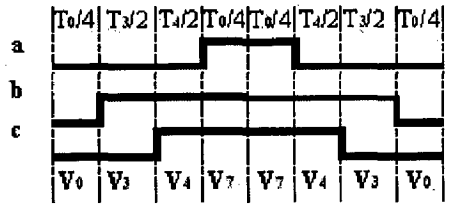
- Each PWM channel switches twice per PWM period except when the duty cycle is 0 or 100%.
- There is a fixed switching order among the three PWM channels for each sector.
- Every PWM period starts and ends with V_0.
- The amount of V_{000} inserted is the same as that of V_{111} in each PWM period.



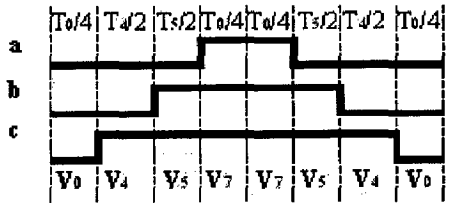
(a) Sector 0



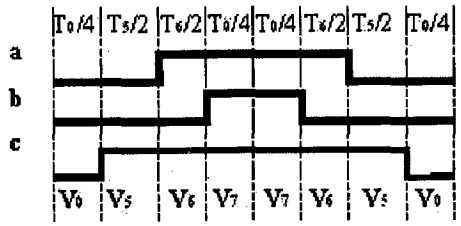
(b) Sector 1



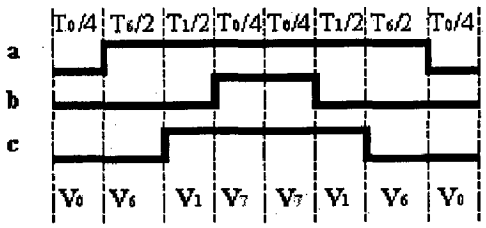
(c) Sector 2



(d) Sector 3



(e) Sector 5



(f) Sector 5

Fig.5.6. Constuction of symmetrical pulse pattern for three phases

Look up table of firing commands depending on the sector

Sector	Sequence of vectors
0	$V_0, V_1, V_2, V_7, V_7, V_2, V_1, V_0$
1	$V_0, V_2, V_3, V_7, V_7, V_3, V_2, V_0$
2	$V_0, V_3, V_4, V_7, V_7, V_4, V_3, V_0$
3	$V_0, V_4, V_5, V_7, V_7, V_5, V_4, V_0$
4	$V_0, V_5, V_6, V_7, V_7, V_6, V_5, V_0$
5	$V_0, V_6, V_1, V_7, V_7, V_1, V_6, V_0$

Table 5.4.Sequence of vectors for each sector

Vector	S_1	S_2	S_3	S_4	S_5	S_6
V_0	0	1	0	1	0	1
V_1	1	1	0	0	0	1
V_2	1	1	1	0	0	0
V_3	0	1	1	1	0	0
V_4	0	0	1	1	1	0
V_5	0	0	0	1	1	1
V_6	1	0	0	0	1	1
V_7	1	0	1	0	1	0

Table5.5. Firing commands for each vector

1: MOSFET ON
0: MOSFET OFF

5.4.3 SPACE VECTOR MODULATION OF THREE-LEVEL INVERTER CONSIDERING DC-LINK VOLTAGE BALANCING AND ITS DIGITAL IMPLEMENTATION

Fig5.5 shows the circuit of a 3 -level, 3 -phase inverter using MOSFET devices. The dc link capacitor C has been split to create the neutral point '0'. A pair of devices with bypass diodes is connected in series with an additional diode connected between the neutral point and the center of the pair. The devices S_{1U} and S_{4U} function as main devices (like two level inverter), and S_{2U} and S_{3U} function as auxiliary devices which help to clamp the output potential to the neutral point with the help of clamping diodes .

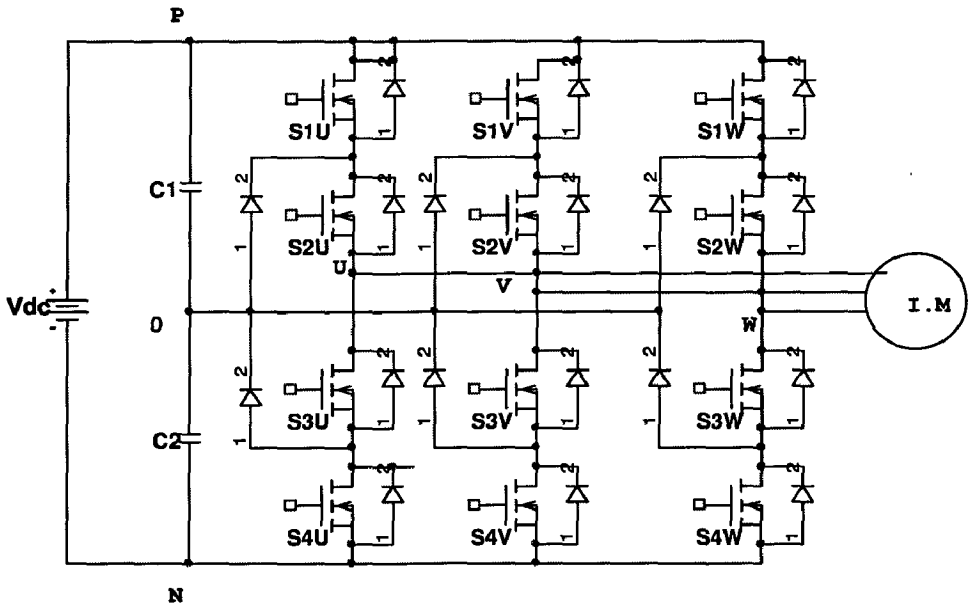


Fig.5.7. Neutral-point Clamped Three-level Inverter

Switching States	S_{1X}	S_{2X}	S_{3X}	S_{4X}	V_{X0}
P	ON	ON	OFF	OFF	+Vdc/2
0	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	-Vdc/2

TABLE 5.6: Switching States of a three-level inverter(X=U,V,W)

Table.5.6 shows the switching states of a three-level inverter. Since three kinds of switching states exist in each phase, a three-level inverter has 27 states. Fig.5.8 (a) shows the representation of the space voltage vectors for three-level inverter. According to the

magnitude of the voltage vectors, we divide tem into four groups: the zero group vectors (V_0), the small voltages vectors (V_1, V_4, V_7 ,V_{10} ,V_{13} ,V_{16}), the middle voltage vectors (V_3, V_6 ,V_9 ,V_{12} ,V_{15} ,V_{18}),the large voltage vectors (V_2, V_5 ,V_8 ,V_{11} ,V_{14} ,V_{17}). The zero voltage vector (ZVV) has three switching states, the small voltage vector (SVV) has two and both the middle voltage vector (MVV) and large voltage vector (LVV) have only one switching state.Fig.5.8 (b) shows same representation for Fig.5.8 (a) It shows the space vector diagram of all switching states[7].

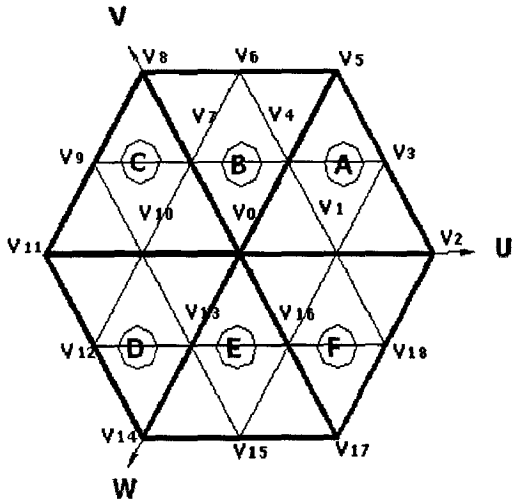


Fig. 5.6(a) Space vector representation

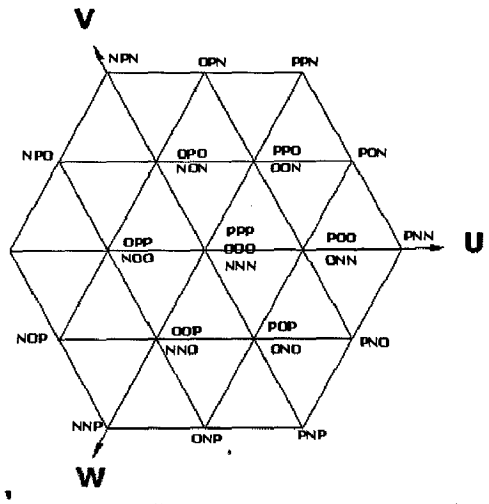


Fig 5.6(b) Space voltage vectors with their switching states

Voltage vectors and their durations

Fig.5.9 shows a triangle formed by the voltage vectors V_0, V_2, and V_5 (Section A). This triangle can be divided into four smaller regions 1,2,3 and 4.In the space voltage vector PWM generally the reference voltage vector is formed by its nearest three voltage vectors in order to minimize the harmonic components of the output line-to-line voltage. For instance if the reference voltage vector V^* falls into the region 3. The durations of each voltage vector can be calculated by the following sequences. First, if the voltage vector and the reference voltage vector can be expressed by the exponential form as follows.

$$V_1 = \frac{1}{2} \qquad \textbf{(5.10)}$$

$$V_3 = \frac{\sqrt{3}}{2} e^{j\frac{\pi}{6}} \qquad \textbf{(5.11)}$$

$$V_4 = \frac{1}{2} e^{j\frac{\pi}{3}} \qquad \textbf{(5.12)}$$

$$V^* = V.e^{j\theta} \qquad \textbf{(5.13)}$$

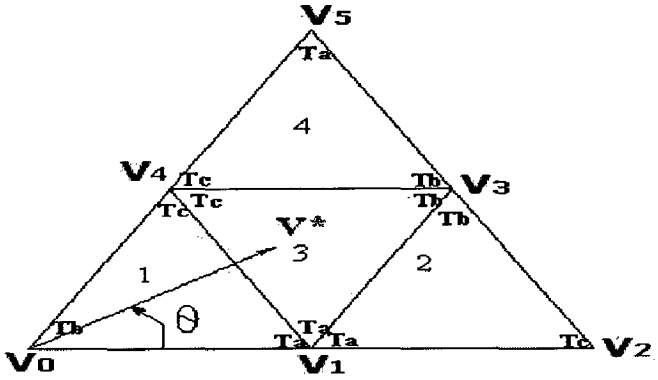


Fig. 5.9 Regions in Sector '0'

Second, the following two equations should be satisfied as space vector PWM for the conventional two-level inverters.

$$V_1.T_a + V_3.T_b + V_4.T_c = V^*.T_s \tag{5.14}$$

$$T_a + T_b + T_c = T_s \tag{5.15}$$

Substituting Eqs., 5.12 to 5.15 in 5.16 and changing trigonometric form

$$\frac{1}{2}T_a + \frac{\sqrt{3}}{2}\left(\cos\frac{\pi}{6} + j\sin\frac{\pi}{6}\right).T_b + \frac{1}{2}\left(\cos\frac{\pi}{3} + j\sin\frac{\pi}{3}\right).T_c = V(\cos\theta + j\sin\theta).T_s \tag{5.16}$$

Separating real part and imaginary part from (A7)

$$\text{Re: } \frac{1}{2}T_a + \frac{\sqrt{3}}{2}\left(\cos\frac{\pi}{6}\right).T_b + \frac{1}{2}\left(\cos\frac{\pi}{3}\right).T_c = V(\cos\theta).T_s \tag{5.17}$$

$$\text{Im: } \frac{\sqrt{3}}{2}\left(\sin\frac{\pi}{6}\right).T_b + \frac{1}{2}\left(\sin\frac{\pi}{3}\right).T_c = V(\sin\theta).T_s \tag{5.18}$$

From Eqs., **5.15, 5.17, 5.18** T_a, T_b and Tc can be calculated and the results are shown as follows.

$$T_a = (1 - 2k\sin\theta)$$

$$T_b = T_s\left[2k\sin\left(\theta + \frac{\pi}{3}\right) - 1\right]$$

$$T_c = T_s\left[2k\sin\left(\theta - \frac{\pi}{3}\right) + 1\right]$$

Where $k = \frac{2V}{\sqrt{3}}$ (0<k<1)

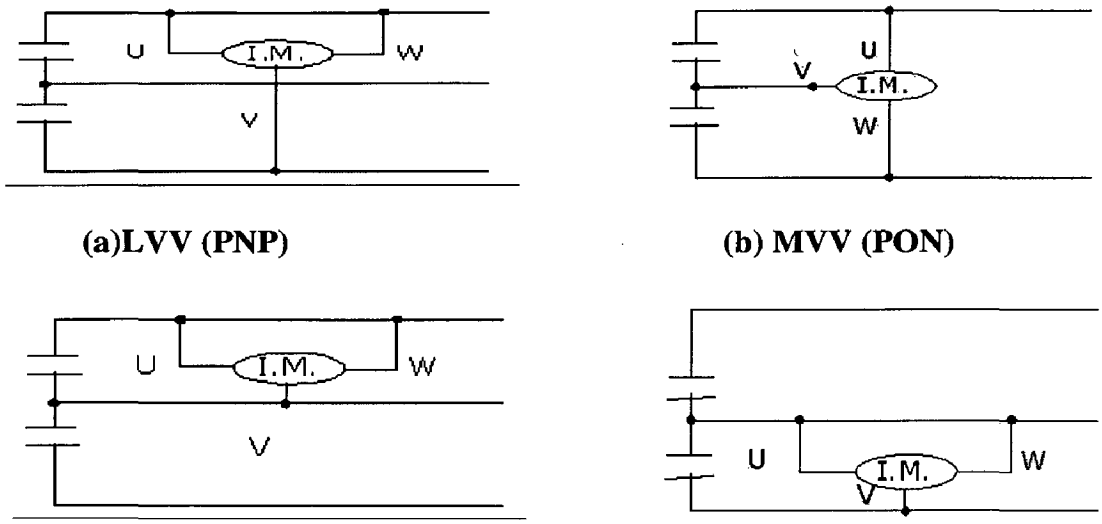
In other regions (1, 2, 4) the durations of each voltage vector can be calculated in same way. Table.5.7. shows durations of the voltage vectors in each region.

R	T_a	T_b	T_c
1	$2kT_s \sin\left(\frac{\pi}{3}-\theta\right)$	$T_s\left[1-2k\sin\left(\frac{\pi}{3}+\theta\right)\right]$	$2kT_s\sin\theta$
2	$2T_s\left[1-k\sin\left(\frac{\pi}{3}+\theta\right)\right]$	$2kT_s \sin\theta$	$T_s\left[2k\sin\left(\frac{\pi}{3}-\theta\right)-1\right]$
3	$Ts[1-2k\sin\theta]$	$T_s\left[2k\sin\left(\frac{\pi}{3}+\theta\right)-1\right]$	$T_s\left[2k\sin\left(\theta-\frac{\pi}{3}\right)+1\right]$
4	$Ts[2k\sin\theta-1]$	$2kT_s \sin\left(\frac{\pi}{3}-\theta\right)$	$2T_s\left[1-k\sin\left(\frac{\pi}{3}+\theta\right)\right]$

Table.5.7 Durations of voltage vectors in each region

Voltage vectors and neutral-point voltage

It is well known how each voltage vector has an effect on the neutral-point voltage. Table5.8 shows the relation between the voltage vectors and the neutral-point voltage. For example, in case of voltage vector [PON] S_{U1}, S_{U2}, S_{V2}, S_{V3}, S_{W3}, S_{W4} are in ON state and others in OFF states. Thus the output terminal A, B, C has potential of $+V_{dc}/2$, 0, $-V_{dc}/2$ respectively and the corresponding load connection is shown in Fig.5.8.(b). The ZVV and LVV do not affect the neutral-point voltage because the load is not connected between neutral point and upper/lower capacitor. The MVV may have large effects on the neutral point voltage, because the upper capacitor or the lower capacitor is charged or discharged according to the load condition. The SVV affects the neutral-point voltage and it can be divided into two small groups; one group consists of V_{1n}, V_{4n}, V_{7n}, V_{10n}, V_{13n}, V_{16n} (Lower small voltage vectors: LSVV). It has close relation with charging or discharging of the lower dc-link capacitor. The other group consists of V_{1p}, V_{4p}, V_{7p}, V_{10p}, V_{13p}, V_{16p} (Upper small voltage vectors: USVV). It has close relation with charging or discharging of the upper dc-link capacitor [6][7].



(a)LVV (PNP)

(b) MVV (PON)

(c) USVV(POP)

(d) LSVV(ONO)

Fig.5.10 Representative Vectors and Their Load Connections

Voltage Vectors	Symbols	Neutral-Point Voltage
ZVV	PPP,OOO,NNN	Not changeable
MVV	PON,OPN,NPO,NOP,ONP,PNO	Increase or decrease
LVV	PNN,PPN,NPN,NPP,NNP,PNP	Not changeable
USVV	POO,PPO,OPO,OPP,OOP,POP	Increase or decrease
LSVV	ONN,OON,NON,NOO,NNO,ONO	Increase or decrease

TABLE.5.8: Relations between Neutral- point Voltage Vector and Load Voltage

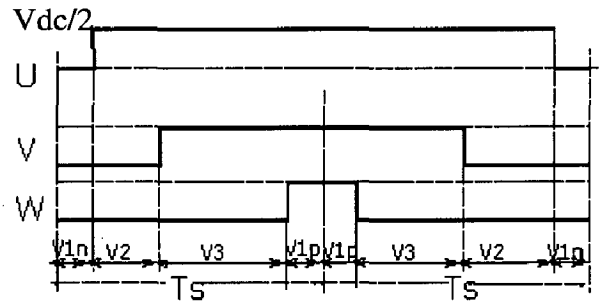
Sequence of voltage vectors

In order to control the neutral point DC voltage, both middle voltage vectors (V_{1n}, V_{1p} or V_{4n}, V_{4p}) which output the same line-to-line voltages have to be selected in time interval T_s [5][6][7]. By considering this condition the sequence of voltage vectors for regions 1,2,3,4 are given in Fig 5.11 along with durations of each voltage vector. The vector sequences and durations for the other sectors are calculated in the same way. The voltage vector sequences in all regions and their Firing Commands for in each voltage vector are formulated in a table as shown in Table.5.9 and Table 5.10 respectively.

This table is stored in 3-dementional matrix as given below

F_cmd[sector-1][region-1] [next_pulse_count].

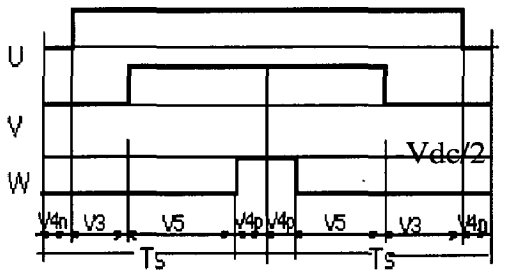
For example if the reference voltage vector is located in 3rd region in sector 1,the sequence of firing commands would be F_cmd[0][2][0] to F_cmd[0][2][7] i.e., **(POO, PON, OON, ONN, ONN, OON, PON, POO)** with the durations **($T_a/2$, T_b, T_c, $T_a/2$, $T_a/2$, Tc, T_b, $T_a/2$).**



(ONN, PNN, PON, POO, POO, PON, PNN, ONN)

($T_a/2$, T_c, T_b, $T_a/2$, $T_a/2$, T_b, T_c, $T_a/2$)

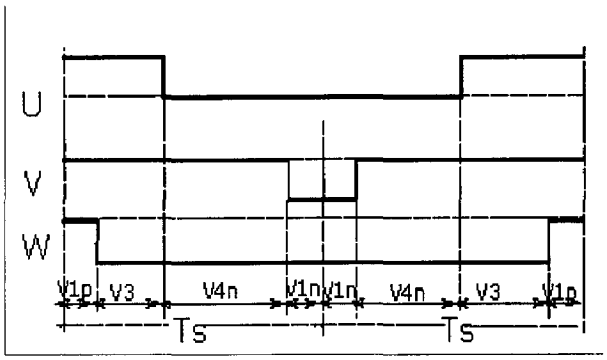
Fig.5.11 (a) Sequence in Region 2



(OON, PON, PPN, PPO, PPO, PPN, PON, OON)

($T_c/2$, T_b, T_a, $T_c/2$, $T_c/2$, T_a, T_b, $T_c/2$)

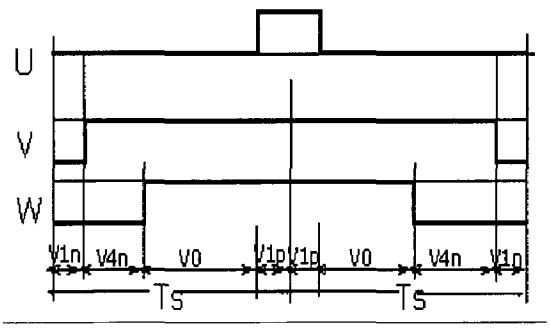
Fig.5.11 (b) Sequence in Region 4



(POO, PON, OON, ONN, ONN, OON, PON, POO)

($T_a/2$, T_b, T_c, $T_a/2$, $T_a/2$, Tc, T_b, $T_a/2$)

Fig.5.11 (c) Sequence in Region 3



(ONN,OON,OOO, POO, POO,OOO,OON, ONN)

($T_b/2$, T_a, T_c, $T_b/2$, $T_b/2$, T_c, T_a, $T_b/2$)

Fig.5.11 (d) Sequence in Region 1

SECTOR	REGION	SEQUNCE OF VECTORS
1	1	ONN,OON,OOO,POO,POO,OOO,OON,ONN
	2	ONN,PNN,PON,POO,POO,PON,PNN,ONN
	3	POO,PON,OON,ONN,ONN,OON,PON,POO
	4	OON,PON,POO,PPO,PPO,POO,PON,OON
2	1	PPO,OPO,OOO,OON,OON,OOO,OPO,PPO
	2	PPO,PPN,OPN,OON,OON,OPN,PPN,PPO
	3	OON,OPN,OPO,PPO,PPO,OPO,OPN,OON
	4	OPO,OPN,NPN,NON,NON,NPN,OPN,OPO
3	1	NON,NOO,OOO,OPO,OPO,OOO,NOO,NON
	2	NON,NPN,NPO,OPO,OPO,NPO,NPN,NON
	3	OPO,NPO,NOO,NON,NON,NOO,NPO,OPO
	4	NOO,NPO,NPP,OPP,OPN,NPN,NPO,NOO
4	1	OPP,OOP,OOO,NOO,NOO,OOO,OOP,OPP
	2	OPP,NPP,NOP,NOO,NOO,NOP,NPP,OPP
	3	NOO,NOP,OOP,OPP,OPP,OOP,NOP,NOO
	4	OOP,NOP,NNP,NNO,NNO,NNP,NOP,OOP
5	1	NNO,ONO,OOO,OOP,OOP,OOO,ONO,NNO
	2	NNO,NNP,ONP,OOP,OOP,ONP,NNP,NNO
	3	OOP,ONP,ONO,NNO,NNO,ONO,ONP,OOP
	4	ONO,ONP,PNP,POP,POP,PNP,ONP,ONO
6	1	POP,POO,OOO,ONO,ONO,OOO,POO,POP
	2	POP,PNP,PNO,ONO,ONO,PNO,PNP,POP
	3	ONO,PNO,POO,POP,POP,POO,PNO,ONO
	4	POO,PNO,PNN,ONN,ONN,PNN,PNO,POO

Table.5.9. Switching Patterns in all regions and sectors

Vector	S_{1u}	S_{2u}	S_{1v}	S_{2v}	S_{1v}	S_{2v}
PNN	1	1	0	0	0	0
PPN	1	1	1	1	0	0
NPN	0	0	1	1	0	0
NPP	0	0	1	1	1	1
NNP	0	0	0	0	1	1
PNP	1	1	0	0	1	1
PON	1	1	1	0	0	0
OPN	1	0	1	1	0	0
NPO	0	0	1	1	1	1
NOP	0	0	1	0	1	1
ONP	1	0	0	0	1	1
PNO	1	1	0	0	1	0
POO	1	1	1	0	1	0
ONN	1	0	0	0	0	0
PPO	1	1	1	1	1	0
OON	1	0	1	0	0	0
OPO	1	0	1	1	1	0
NON	0	0	1	0	0	0

OPP	1	0	1	1	1	1
NOO	0	0	1	0	1	0
OOP	1	0	1	0	1	1
NNO	0	0	0	0	1	0
POP	1	1	1	0	1	1
ONO	1	0	0	0	1	0
PPP	1	1	1	1	1	1
OOO	1	0	1	0	1	0
NNN	0	0	0	0	0	0

Table 5.10 Firing Commands for Each Vector

1: MOSFET ON
0: MOSFET OFF

CHAPTER-6

INDUCTION MOTOR CONTROL

6.1. SCALAR CONTROL OR OPEN LOOP V/Hz CONTROL

Scalar control, as the name indicates, is due to magnitude variation of the control variables only, and disregards the coupling effect in the machine. For example, the voltage of a machine can be controlled to control the flux, and frequency or slip can be controlled to control the torque. However, flux and torque are also functions of frequency and voltage, respectively. Scalar control is contrast to vector or field oriented control (will be discussed in next section), where both the magnitude and phase alignment of vector variables are controlled. Scalar–controlled drives give somewhat inferior performance, but they are easy to implement. Scalar controlled drives have been widely used in industry. However their importance has diminished recently because of the superior performance of vector-controlled drives, which is demanded in many applications.

The Principle of Constant V/Hz for AC Induction Motor

Assume the voltage applied to a three phase AC Induction motor is sinusoidal and neglect the voltage drop across the stator resistor. Then we have, at steady state,

$$\hat{V} \approx j\omega\hat{\Lambda} \text{ i.e, } V \approx \omega\Lambda$$

Where, $\hat{V}$ and $\hat{\Lambda}$ are the phasors of stator voltage and stator flux,

And V and Λ are their magnitude, respectively. Thus, we get

$$\Lambda \approx \frac{V}{\omega} \equiv \frac{1}{2\pi}\frac{V}{f} \qquad (6.1)$$

from which it follows that if the ratio V/f remains constant with the change of f, then Λ remains constant too and the torque is independent of the supply frequency. In actual implementation, the ratio between the magnitude and frequency of the stator voltage is usually based on the rated values of these variables, or motor ratings. However, when the frequency and hence also the voltage are low, the voltage drop across the stator resistance

cannot be neglected and must be compensated. At frequencies higher than the rated value, the constant V/Hz principle also have to be violated because, to avoid insulation break down, the stator voltage must not exceed its rated value. This principle is illustrated in Fig. 6.1. Since the rated voltage which is also the maximum voltage is applied to the motor at rated frequency, only the rated, minimum and maximum frequency information is needed to implement the profile.

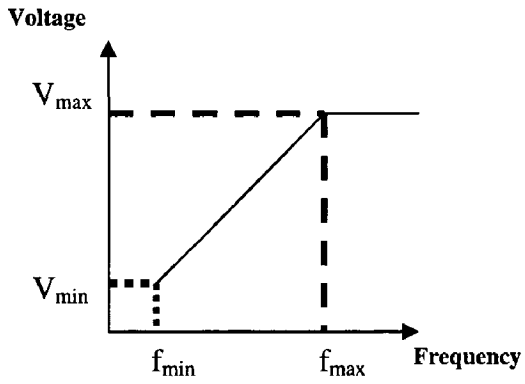


Fig 6.1 V/Hz Profile

6.2. VECTOR CONTROL OR FIELD ORIENTED CONTROL (FOC)

The vector control is referring not only to the magnitude but also to the phase of these variables. Matrix and vectors are used to represent the control quantities. This method takes into consideration not only successive steady-states but real mathematical equations that describe the motor itself, the control results obtained have a better dynamic for torque variations in a wider speed range. The space phasor theory is a method to handle the equations.

Though the induction motor has a very simple structure, its mathematical model is complex due to the coupling factor between a large number of variables and the non-linearities. The Field Oriented Control (FOC) offers a solution to circumvent the need to solve high order equations and achieve an efficient control with high dynamic. This approach needs more calculations than a standard V/f control scheme.

List of Variables Used In FOC

The following lines show the different variables used in this control software and in the equations and schemes presented here.

i_a, i_b, i_c	Phase currents
$i_{s\alpha}, i_{s\beta}$	Stator current (α, β) components
$V_{s\alpha}, V_{s\beta}$	Stator voltage (α, β) components
i_{ds}, i_{qs}	Stator current flux & torque comp.
i_{ds}^*, i_{qs}^*	Reference values of Flux and torque command
θ_e	Rotor flux position
ω_e	Rotor flux speed
ω_{sl}	Slip Speed
ω_{ref}	Reference speed
ω_r	Motor actual speed
V_d, V_q	(d, q) components of the stator voltage
R_r	Rotor Resistance
L_r	Rotor Inductance
V_{DC}	DC bus voltage

Field Oriented Control Theory

During the last few years the field of controlled electrical drives has undergone rapid expansion due mainly to the advantages of semiconductors in both power and signal electronics and culminating in micro-electronic microprocessors and DSPs. These technological improvements have enabled the development of really effective AC drive control with ever lower power dissipation hardware and ever more accurate control structures. The electrical drive controls become more accurate in the sense that not only are the DC current and voltage controlled but also the three phase currents and voltages are managed by so-called vector controls. This document describes the most efficient form of vector control scheme: the Field Orientated Control. It is based

on three major points: the machine current and voltage space vectors, the transformation of a three phase speed and time dependent system into a two co-ordinate time invariant system and effective Pulse Width Modulation pattern generation. Thanks to these factors, the control of AC machine acquires every advantage of DC machine control and frees itself from the mechanical commutation drawbacks. Furthermore, this control structure, by achieving a very accurate steady state and transient control, leads to high dynamic performance in terms of response times and power conversion.

The Field Orientated Control (FOC) consists of controlling the stator currents represented by a vector. This control is based on projections which transform a three phase time and speed dependent system into a two co-ordinate (d and q co-ordinates) time invariant system. These projections lead to a structure similar to that of a DC machine control. Field orientated controlled machines need two constants as input references: the torque component (aligned with the q co-ordinate) and the flux component (aligned with d co-ordinate). As Field Orientated Control is simply based on projections the control structure handles instantaneous electrical quantities. This makes the control accurate in every working operation (steady state and transient) and independent of the limited bandwidth mathematical model.

Space Vector definition and projection

The three-phase voltages, currents and fluxes of AC-motors can be analyzed in terms of complex space vectors. With regard to the currents, the space vector can be defined as follows. Assuming that i_a, i_b, i_c are the instantaneous currents in the stator phases, then the complex stator current vector $\bar{i}_s$ is defined by

$$\bar{i}_s = i_a + \alpha i_b + \alpha^2 i_c \qquad \textbf{(6.2)}$$

Where, $\alpha = e^{j\frac{2}{3}\pi}$, $\alpha^2 = e^{j\frac{4}{3}\pi}$ represent the spatial operators. The above Fig. 6.3 shows the stator current complex space vector: where (a, b, c) are the three phase system axes. This current space vector depicts the three phase sinusoidal system. It still needs to be transformed into a two time invariant co-ordinate system. This transformation can be split into two steps:

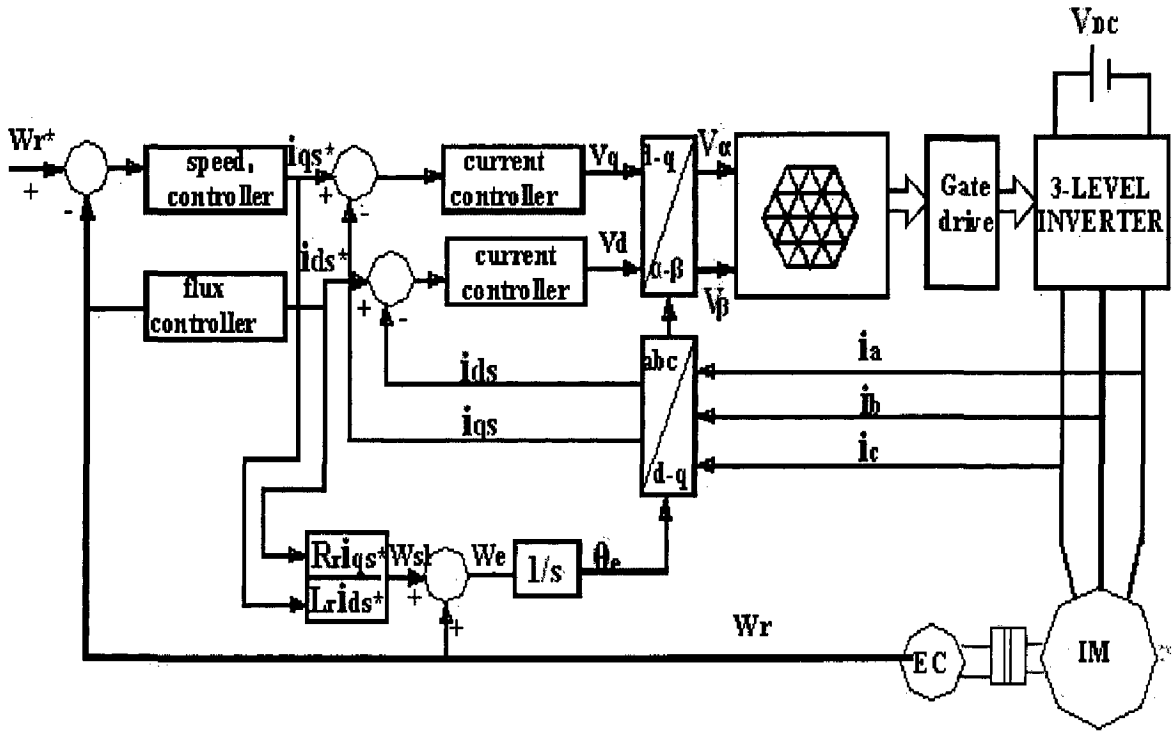


Fig.6.2 Complete AC Induction Drive Dedicated FOC Structure

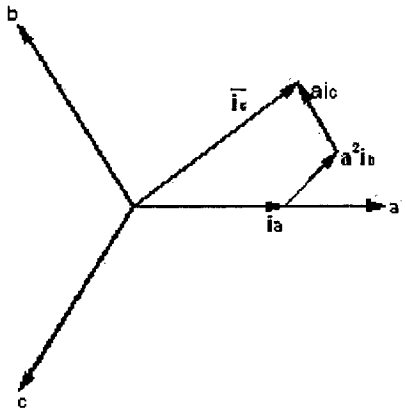


Fig. 6.3 Stator current space vector and its component in (a, b, c)

- (a,b,c) → (α,β) (the Clarke transformation) which outputs a two co-ordinate time variant system.
- (α,β) → (d,q) (the Park transformation) which outputs a two co-ordinate time invariant system.

The (a, b, c) →(α, β) projection (Clarke transformation)

The space vector can be reported in another reference frame with only two orthogonal axis called (α, β). The projection that modifies the three phase system into the (α, β) two dimension orthogonal system is presented below.

$$i_{s\alpha} = \frac{2}{3} i_a - \frac{1}{3} i_b - \frac{1}{3} i_c$$

$$i_{s\beta} = -\frac{1}{\sqrt{3}} i_b + \frac{1}{\sqrt{3}} i_c \qquad \textbf{(6.3)}$$

The (α, β) → (d, q) projection (Park transformation)

This is the most important transformation in the FOC. In fact, this projection modifies a two phase orthogonal system (α, β) into (d, q) rotating reference frame. If we consider the d-axis aligned with the rotor flux, the next diagram shows, for the current vector, the relationship from the two reference frame where θ is the rotor flux position. The flux and torque components of the current vector are determined by the following equations [29].

$$i_{ds} = i_{s\alpha} \cos\theta_e + i_{s\beta} \sin\theta_e$$

$$i_{qs} = -i_{s\alpha} \sin\theta_e + i_{s\beta} \cos\theta_e \qquad \textbf{(6.4)}$$

These components depend on the current vector (α, β) components and on the rotor flux position; if we know the right rotor flux position then, by this projection, the (d, q) component becomes a constant.

The (d, q) → (α, β) projection (inverse Park transformation)

Here, we introduce from this voltage transformation only the equation that modifies the voltages in d,q rotating reference frame in a two phase orthogonal system[29].

$$v_\alpha = v_d \cos\theta_e - v_q \sin\theta_e$$

$$v_\beta = v_d \sin\theta_e - v_q \cos\theta_e \qquad \textbf{(6.5)}$$

Operation

Three phase currents feed the Clarke transformation module. These projection outputs are indicated $i_{s\alpha}$ and $i_{s\beta}$. These two components of the current are the inputs of the Park transformation that gives the current in the d, q rotating reference frame. The i_{sd} and i_{sq} components are compared to the references i_{sdref} (the flux reference) and i_{sqref} (the torque reference). At this point, this control structure shows an interesting advantage: it can be used to control either synchronous or induction machines by simply changing the flux reference and obtaining rotor flux position. As in synchronous permanent magnet motors, the rotor flux is fixed (determined by the magnets) there is no need to create one. Hence, when controlling a PMSM, i_{sdref} should be set to zero. As induction motors need a rotor flux creation in order to operate, the flux reference must not be zero. This conveniently solves one of the major drawbacks of the "classic" control structures: the portability from asynchronous to synchronous drives. The torque command i_{sqref} could be the output of the speed regulator when we use a speed FOC. The outputs of the current regulators are V_{sdref} and V_{sqref}; they are applied to the inverse Park transformation. The outputs of this projection are $V_{s\alpha ref}$ and $V_{s\beta ref}$ which are the components of the stator vector voltage in the (α, β) stationary orthogonal reference frame. These are the inputs of the Space Vector PWM. The outputs of this block are the components of the reference vector $\mathbf{V}^*$ that we call is the voltage space vector to be applied to the motor phases.

Rotor flux position can be calculated as shown below [29].

$$\theta_e = \int(\omega_r + \omega_{sl}) \tag{6.6}$$

Where, ω_r = Actual Speed

$$\text{Slip Speed, } \omega_{sl} = \frac{R_r i^*_{qs}}{L_r i^*_{ds}} \tag{6.7}$$

CHAPTER-7

SYSTEM DEVELOPMENT

In this chapter the hardware requirements for the realization of Neutral point clamped Three-level Inverter along with the various design aspects like modular construction testing and assembling etc. The protection of the MOSFETs has been discussed. Hall effect current sensor has been used for the current measurement. Speed encoder has been used for speed measurement. Delay circuit has been used to provide delay and to protect the devices in the same leg from short circuit for the realization of conventional three-phase inverter. All the hardware requirements have been discussed briefly in the following sections. PC interfacing with the hardware and data acquisition cards has been described briefly. Final section of this chapter consists of the implantation of open loop V/f control of Neutral Point Clamped Inverter Fed Induction Motor Drive and closed loop operation of the drive using Field oriented control. Only pictorial representation of the above control techniques has been given trough flow charts.

7.1. HARDWARE REQUIREMENTS

7.1.1. POWER CIRCUIT:

Fig. 7.1 shows the power circuit of the Neutral point clamped voltage source PWM inverter. We know that for an m-level inverter, the number of switching devices required per phase leg is m-1.

In this case m=3.

Total number of switching devices =12

Capacitors required to get 3-level output=2

Clamping diodes required will be=6.

Each MOSFET switch is used in the circuit consists of an inbuilt anti parallel free wheeling diode. No forced commutation circuits are required for MOSFETs because these are self commutated devices (they turn on when the gate signal is high and turn of when the gate signal is low). The load inductance restricts large di/dt through MOSFETs; hence only turnoff snubber is required for protection. An RCD (resistor, capacitor and diode) turn-off circuit is connected to protect the circuit against high dv/dt

and is protected against power voltage by connecting MOV (Metal Oxide Varistor). Same circuit is utilized for development of three-phase PWM voltage source inverter shown in Fig.7.2 using upper two rows of 3-level Inverter without clamping diodes.

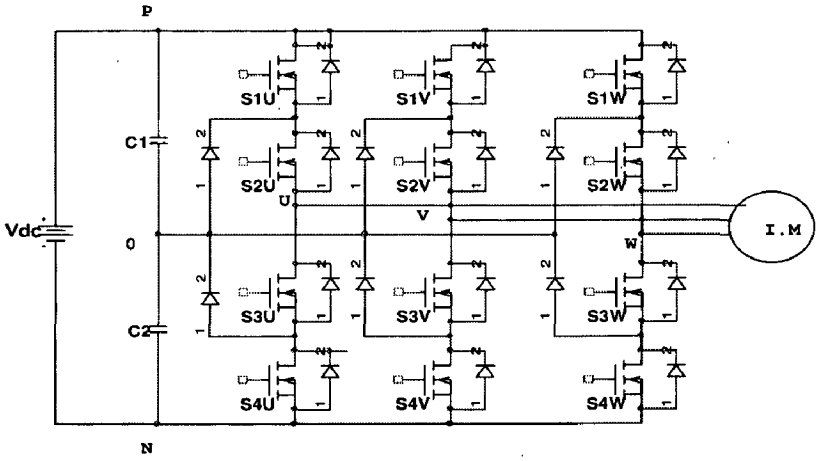


Fig.7.1 Neutral Point Clamped Three level Inverter

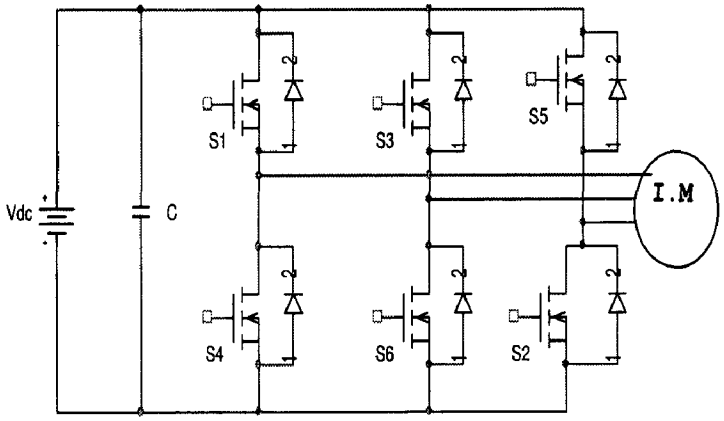


Fig.7.2 Conventional Three –phase Inverter

7.1.2. PULSE AMPLIFICATION AND ISOLATION CIRCUIT:

The pulse amplification and isolation circuit for MOSFET is shown in Fig. 3.3. The opto-coupler (MCT-2E) provides the necessary isolation between the low voltage isolation circuit and high voltage power circuit .The pulse amplification is provided by the output amplifier transistor 2N222.

When the input gating pulse is at +5V level, the transistor saturates, the LED conducts and the light emitted by it falls on the base of phototransistor, thus forming its

base drive. The output transistor thus receive no base drive and, therefore remains in cut-off state and a +12 v pulse (amplified) appears across it's collector terminal (w.r.t.ground). When the input gating pulse reaches the ground level (0V), the input switching transistor goes into the cut-off state and LED remains off, thus emitting no light and therefore a photo transistor of the opto-coupler receives no base drive and, therefore remains in cut-off state .A sufficient base drive now applies across the base of the output amplifier transistor it goes into the saturation state and hence the output falls to ground level. Therefore circuit provides proper amplification and isolation. Further, since slightest spike above 20V can damage the MOSFET, a 12 V Zenor diode is connected across the output of isolation circuit. It clamps the triggering voltage at 12 V.

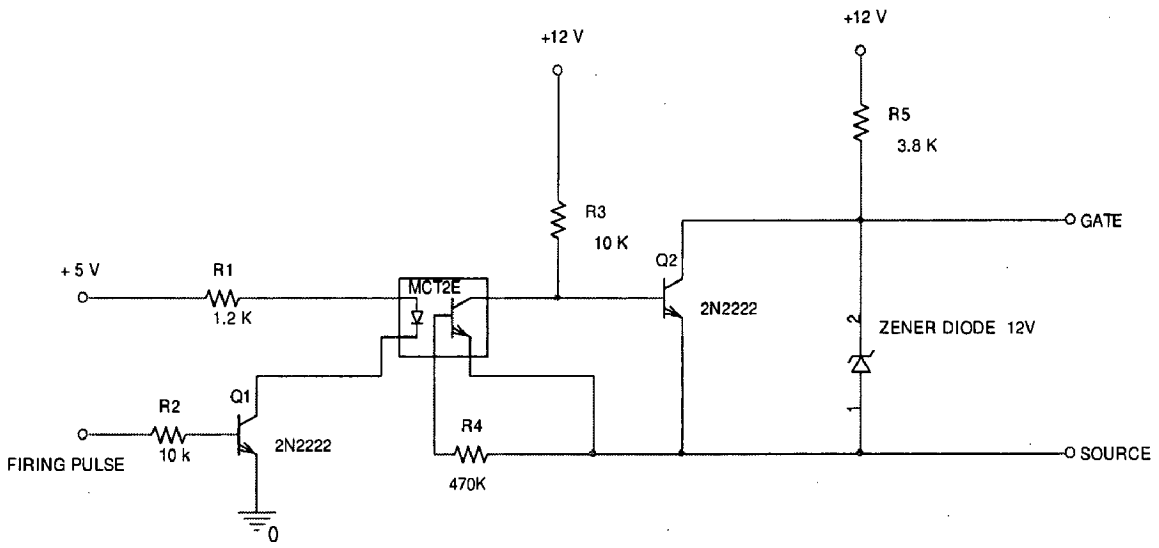


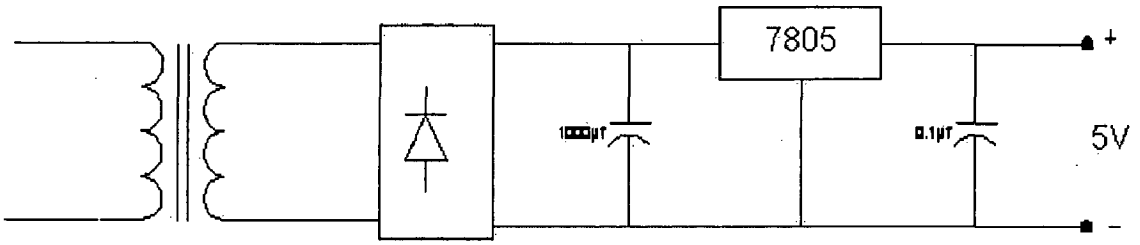
Fig 7.3 Pulse Amplification and Isolation Circuit

7.1.3. POWER SUPPLIES

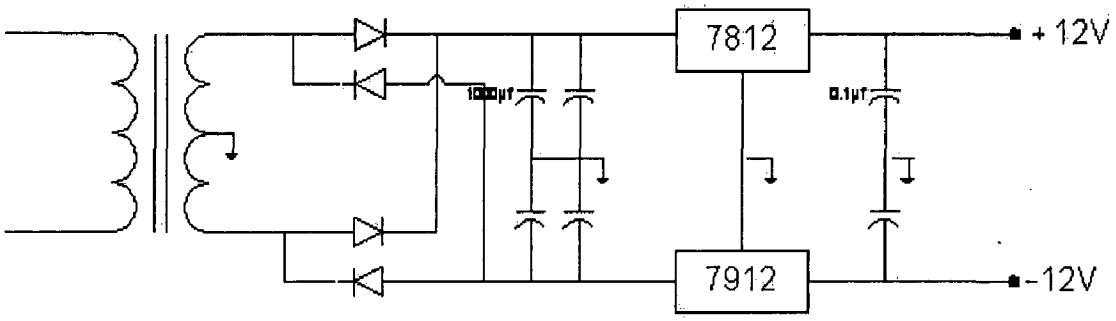
D.C regulated power supplies (±12 V and +5 V) are required for providing the biasing to various ICs, etc. the system development has in-built power supplies for this purpose. The circuit diagram for various dc regulated power supplies are shown in Fig. 7.4. As, shown the single phase AC voltage is stepped down and the rectified using diode bridge rectifier. A capacitor of 1000μF, 50V is connected at the output of the bridge rectifier for smoothing out the ripples in the rectified dc voltage of each supply. IC voltage regulated chips, 7812, 7912, 7805 are used for obtaining the dc-regulated

voltages. A capacitor of 0.1μF, 50 V is connected at the output of the IC voltage regulator of each supply for obtaining the constant, ripple-free dc voltage.

DC VOLTAGE	IC REGULATOR
+5V	7805
+12V	7812
-12V	7912



(a)



(b)

Fig. 7.4 Power supplies (a) +5V supply (b) ±12V supply

7.1.4. CURRENT SENSING CIRCUIT AND SCALING

Closed loop Hall Effect current transformers use the ampere turn compensation method to enable measurement of current from dc to high frequency with the ability to follow rapidly changing level or wave shapes. The application of primary current (Ip) causes a change in flux in the air gap. This in turn produces a change in output from the hall element away from the steady state condition. This output is amplified to produce a current(I_s),which is passed trough a secondary winding causing a magnetizing force to oppose that of the primary current, thereby reducing the air gap

flux. The secondary current is increased until the flux is reduced to zero. At this point the hall element output will return to steady state condition and the ampere turn product of secondary circuit will match that of the primary. The current that passes through the secondary winding is the output current. The transformation ration is calculated by the standard current transformation equation:

$$N_pI_p=N_sI_s$$

Where, N_p= Primary turns

I_p= Primary current

N_s= Secondary turns

I_s= Secondary current

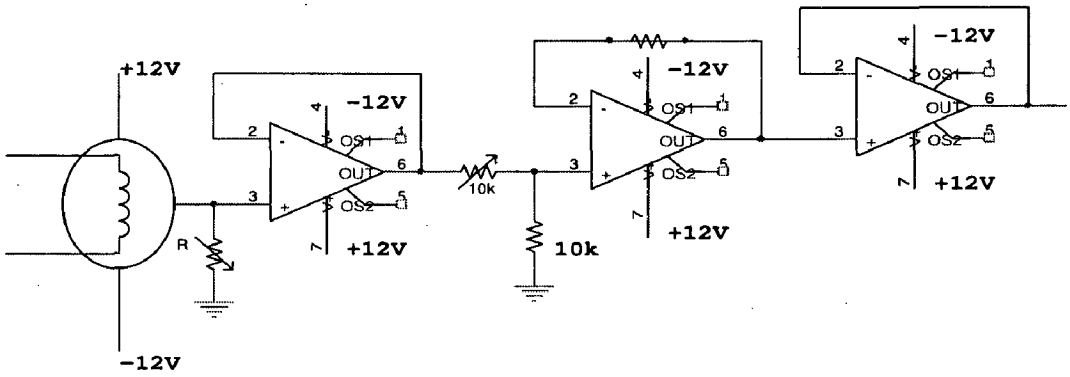


Fig.7.5. Hall-effect Current sensor

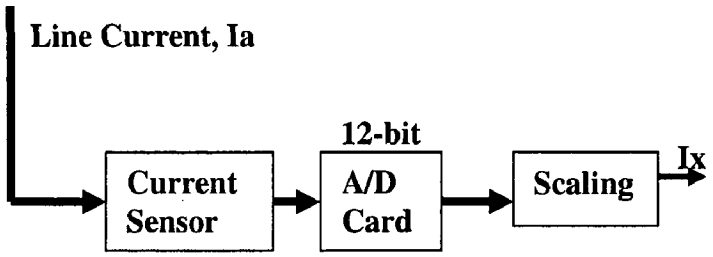


Fig.7.6 Current Sensing and Scaling

A 10KΩ resistor is used in the negative feed back path of the OP-AMP for gain adjustment so as to obtain a voltage of 1 volt corresponding to 1 Amp (DC current). The current carrying conductors are passed in the reverse direction in the current sensor in order to obtain right polarity current at the output of the inverting amplifier. Same circuit is used for measuring other currents (I_b, I_c).

The FOC structure requires three line currents as input. These three current sensor outputs are connected to three channels of ADC Card. These currents therefore needs to be rearranged and scaled so that it can be used by the control software The complete process of acquiring the current is depicted in the Fig. 7.6. ADC range is set to ± 5 V and the gain is 2. The actual current is calculated using the equation:

$$\text{Actual current} = \frac{1}{AD\_DATA} * \frac{4096}{Gain} \qquad (7.1)$$

7.1.5. PROTECTION OF MOSFETS

An RC snubber circuit has been used for the protection of the main switching device. The circuit diagram is given in Fig. 7.7.

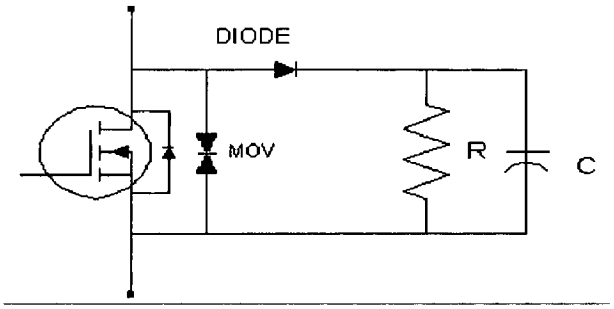


Fig.7.7. Snubber Circuit for MOSFET protection

Energy stored in C, $Ec=(1/2)*C*V_{dc}^2$

Power=E_c*f_{max}

This is the power dissipated P_R in the resistor R.

Where V_{DC} is the maximum DC level and f_{max} is the maximum frequency of the output wave.

This energy needs to be dissipated within Ton for the worst case i.e. $T_{on}(min)$.

The time constant of the RC circuit is taken as one-fifth of $T_{on}(min)$.

Therefore, $T_{RC}= 1/(5*6*f_{max})=R*C$ **(7.2)**

Constant losses in R for worst case are given by

$P=V_R^2/R$ **(7.3)**

Taking an average value of V_R as 200V,P=8W

Also P_R for V_{DC}=400V and f_{max}=100Hz is 0.8W.

The value of R is found from (3) for C=0.1μF and R comes out as 5 KΩ.

A 10 KΩ, 10W resistor has been used.

7.1.6. DELAY CIRCUIT

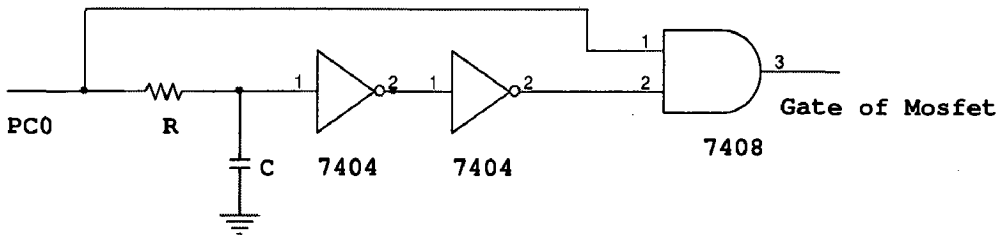


Fig.7.8. Delay Circuit

This circuit provides 5μS delay and R=5kΩ and C=0.001μF

7.2. PC INTERFACING AND CONTROL

Pentium 80486 Processor based PC with clock frequency 2 MHz along with the Timer I/O card and ADC has been used for this application. This card provides two 8255 each having three I/O ports A, B, C. Since there are 12 switches in Neutral Point Clamped Inverter, six bits from PORTB are being used as firing bits of Upper half of 3-level inverter and inverted signals are used as a firing bits of Lower half of 3-level inverter.. The card has two timer chips 8253-1 and 8253-2. Each chip has three counters out of which TIMER2_1, TIMER2_2 from 8253-2 have been used to generate time delays. TIMER1_0 and TIMER1_1 from 8253-1 have been used to generate 1ms interrupt and current measurement respectively for closed loop operation. 2MHz clock from this card has been used as clock signal to all counters. Four bits from PORTC are being used as GATES of four counters. Complete interfacing has been given in **Fig.7.9**

The interrupt used are IR3, IR4, IR7. To avoid any damage to the ports, a buffer circuit has been fabricated (using 74245 buffers) and all firing bits are first buffered and then applied to the switching devices. The source code has been written in 'C' language.

The same configuration has been used to operate conventional Three-phase inverter shown in Fig.7.10. Since there are 6 switches in three phase Inverter, six bits from PORTC are being used as firing bits to these switches through delay circuit which provides 5 micro seconds delay to protect the MOSFETs in same leg from short circuit. Two bits from PORTC are being used as GATES of Two Timers.

Speed Encoder Interfacing Circuit

This module converts the number of pulses sent by the incremental encoder into an absolute mechanical position of the rotor shaft. It is possible to obtain an absolute mechanical position with the incremental encoder by physically locking the rotor in a known position. The number of encoder pulses detected between two PWM periods. Direction of rotor is also to be found using this encoder.

The photo sensors of the encoder shown in Fig.7.11 are activated by the light of an internal LED. When the light is hidden, the sensor sends a logical "0". When the light passes through one of the slots of the encoder, a logical "1" is sent. The count of the edges detected by the Encoder is stored in the counter. The complete interfacing circuit is shown Fig.7.12

Speed Encoder generates train of pulses which is connected to TIMER1_1 as clock. The output of TIMER1_1 is kept open. This timer is loaded is loaded with FFFFH. Speed measurement is done at every 10ms period. So TIMER1_2 is loaded with count value corresponding to 10ms.Both the timers are triggered at the same time. As soon as this time is over it generates an interrupt and control goes to interrupt procedure. Speed is calculated using this formula.

Let m: No of pulses/rev (Fixed for Encoder)

N: Speed in rev/min→N/60 rev/sec;

Frequency of pulse Train = m*N/60 pulses/sec;

T_c: Time over which pulses are counted (10ms).

Count in T_c period, c =m*N*T_c/60;

In this case m=5000 and T_c=10ms.

$$\text{Speed of Motor} = 1.2 * \text{count} \qquad (7.4)$$

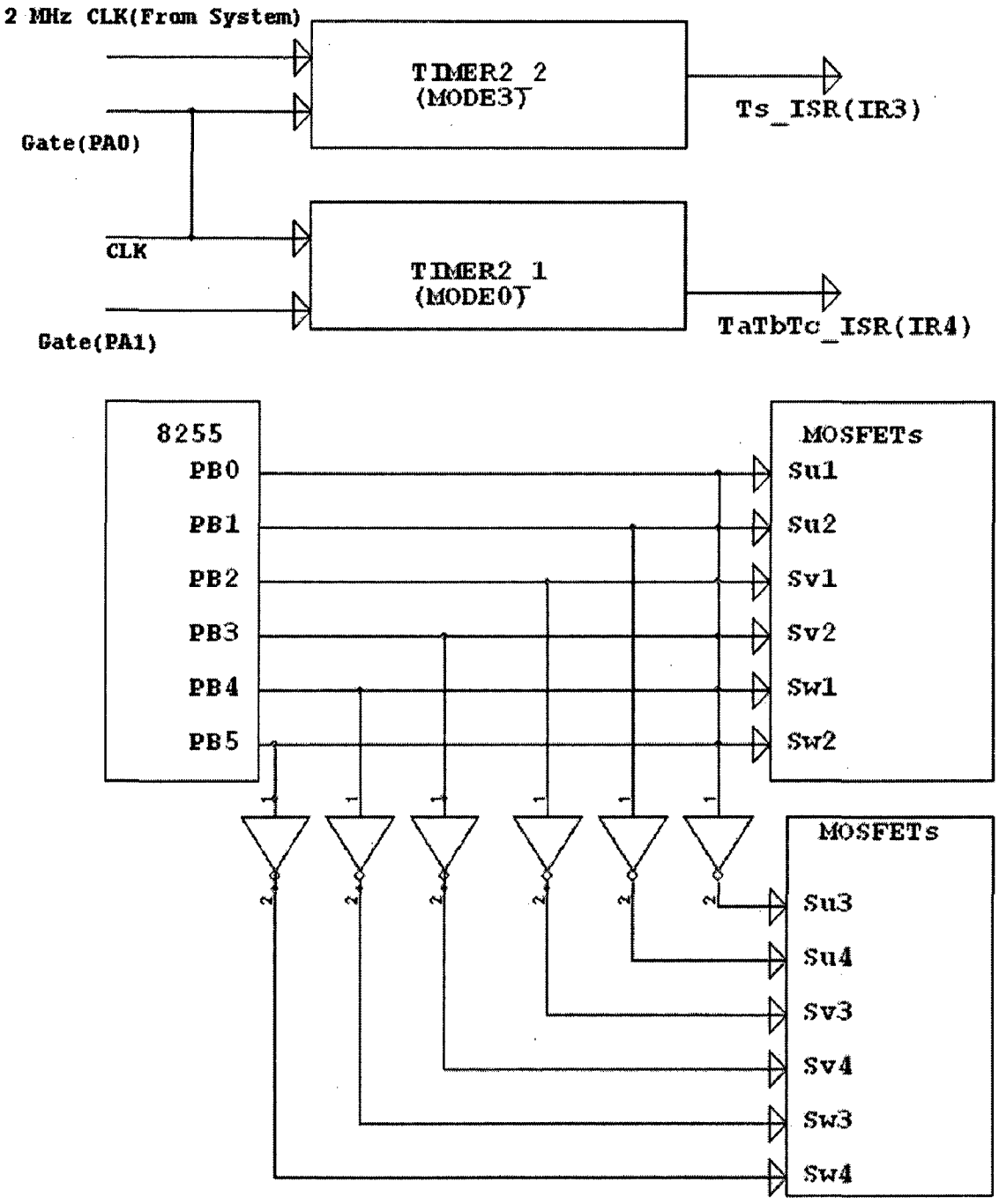


Fig.7.9. PC Interfacing for Neutral Point Clamped Three-level Inverter

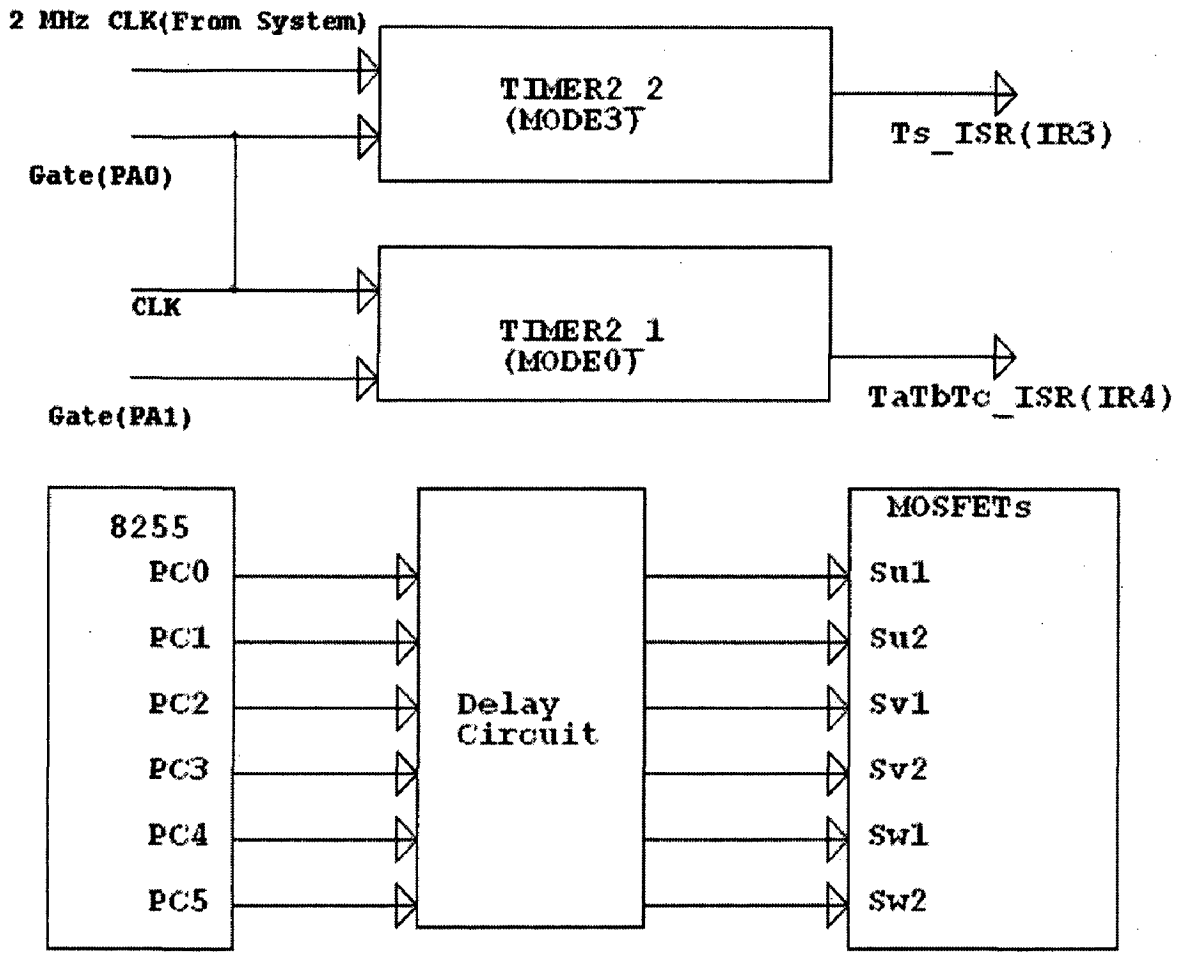


Fig.7.10. PC Interfacing to Conventional Three-phase Inverter

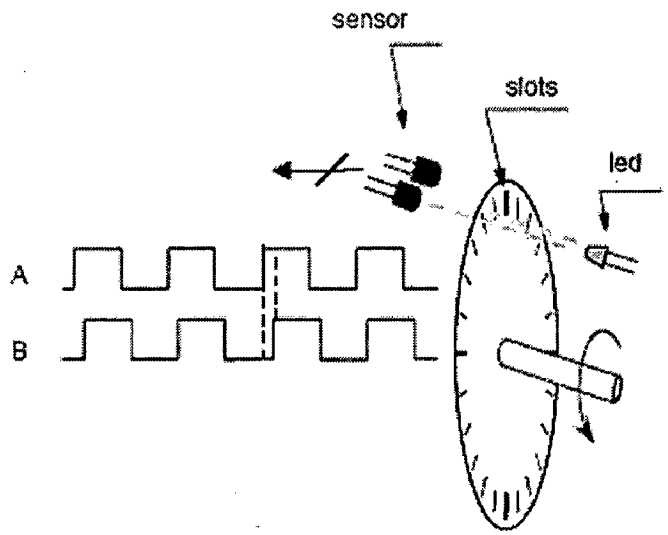


Fig.7.11 Speed Encoder

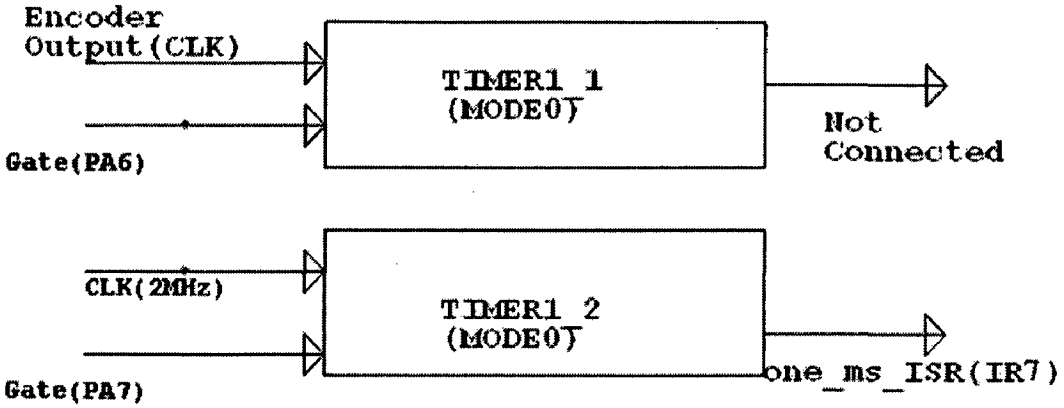


Fig.7.12 PC Interfacing of Speed Encoder for Speed Measurement

7.3. CONTROL TECHNIQUE AND SOFTWARE DEVELOPMENT

The performance of any drive depends on the control technique (discussed in Chapter) and its implementation. In the present drive, the control is implemented through 80486 processor based PC and Data acquisition cards. Microprocessor based control reduces the complexity of the system hardware, increases the reliability and makes the control system fast. Space vector modulation technique is used to control the inverter.

The system hardware of the induction motor drive has been discussed in this chapter. The complete drive is controlled using TIMER I/0 and ADC cards for speed measurement, current measurement and firing pulse generation to Neutral Point Clamped Inverter. For superior performance and fast response of the drive system suitable software is to be developed. The system software development consists of the main program of drive system in open and closed loop, current measurement, interrupt service subroutines, current PI processing, speed measurement and speed PI processing. Only pictorial representation of the various software is given through flow charts. The complete software has been developed using 'C' language.

7.3.1. SOFTWARE ORGANIZATION

This software is based on two modules: the initialization module and the run module. The former is performed only once at the beginning. The second module is based on a waiting loop interrupted by the PWM underflow. When the interrupt flag is set, this

is acknowledged and the corresponding Interrupt Service Routine (ISR) is served. The

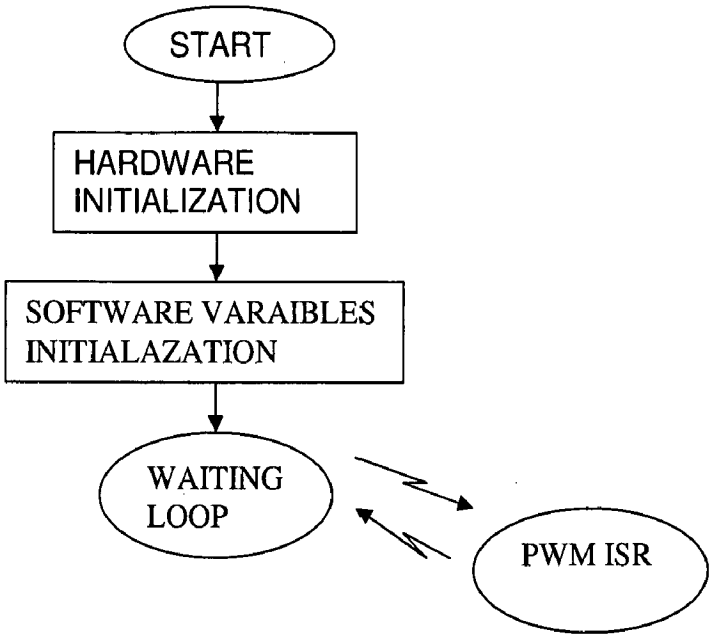


Fig. 7.13. General Software Flow Chart

complete algorithm is computed within the PWM ISR and thus runs at the same frequency as the chopping frequency. The waiting loop can be easily replaced by a user interface. Presentation of the interface is beyond the scope of this report, but is useful to fit the control code and to monitor the control variables. An overview of the software is given in the flow chart below:

7.3.2. OPEN LOOP V/Hz CONTROL OF NEUTRAL POINT CLAMPED INVERTER FED INDUCTION MOTOR DRIVE

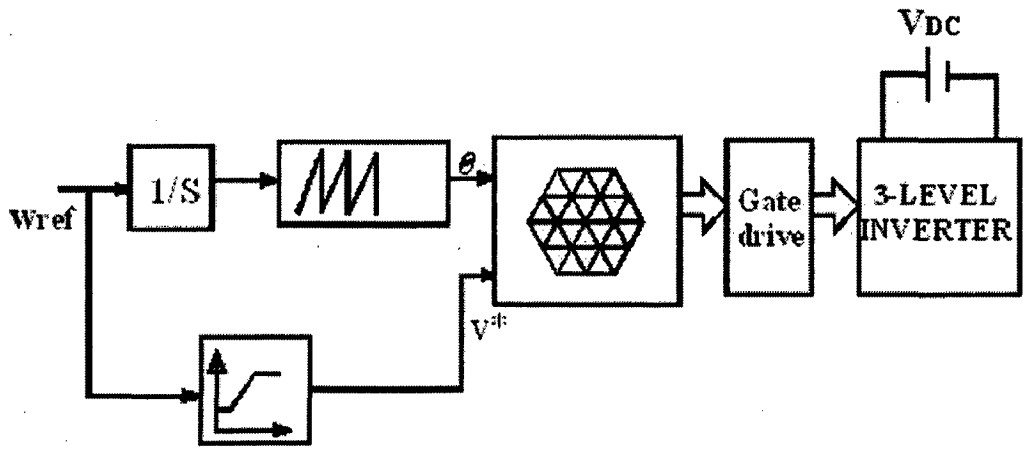


Fig. 7.14.OPEN LOOP V/f CONTROL OF NEUTRAL POINT CLAMPED INVERTER

Software for the Open Loop V/Hz control of Neutral Point Clamped Inverter fed Induction Motor Drive shown in Fig.7.14 consists of main program and Ts_ISR, TaTbTc_ISR interrupt service subroutines. The Flow chart for the main program starts with the initialization of various inputs, output ports, timers and various variables in the program. Set the sampling time with required value, which decides the switching frequency. This gives the minimum voltage (V_{min}) required for the minimum frequency (f_{min}). For the constant V/f control the machine starts with the minimum speed by setting the frequency to a minimum value and then load the master timer with count value corresponding to $2*T_s$. The reference speed is gradually increased until rated speed of the machine is obtained. At this point all the interrupts are enabled to generate the firing pulses. If the character received is 'y' (To change the frequency) frequency is increased by fixed step, if it is 's' (To stop the machine) all the interrupts and gates are disabled and reset firing pulses to all the switches. Otherwise continue the same procedure until key the pressed is 's'. Above procedure is explained through Flow charts given in Fig.7.16, 7.17, 7.18, 7.20.

7.3.3. V/Hz CONTROL OF THREE-PHASE INVERTER FED INDUCTION MOTOR DRIVE

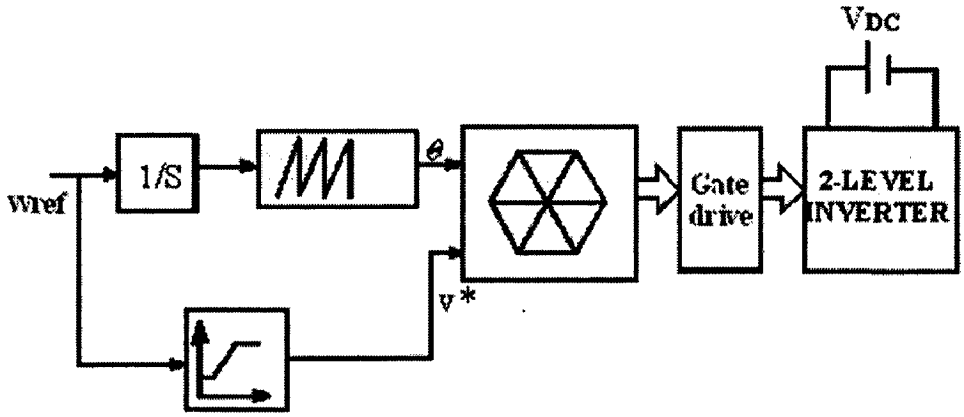
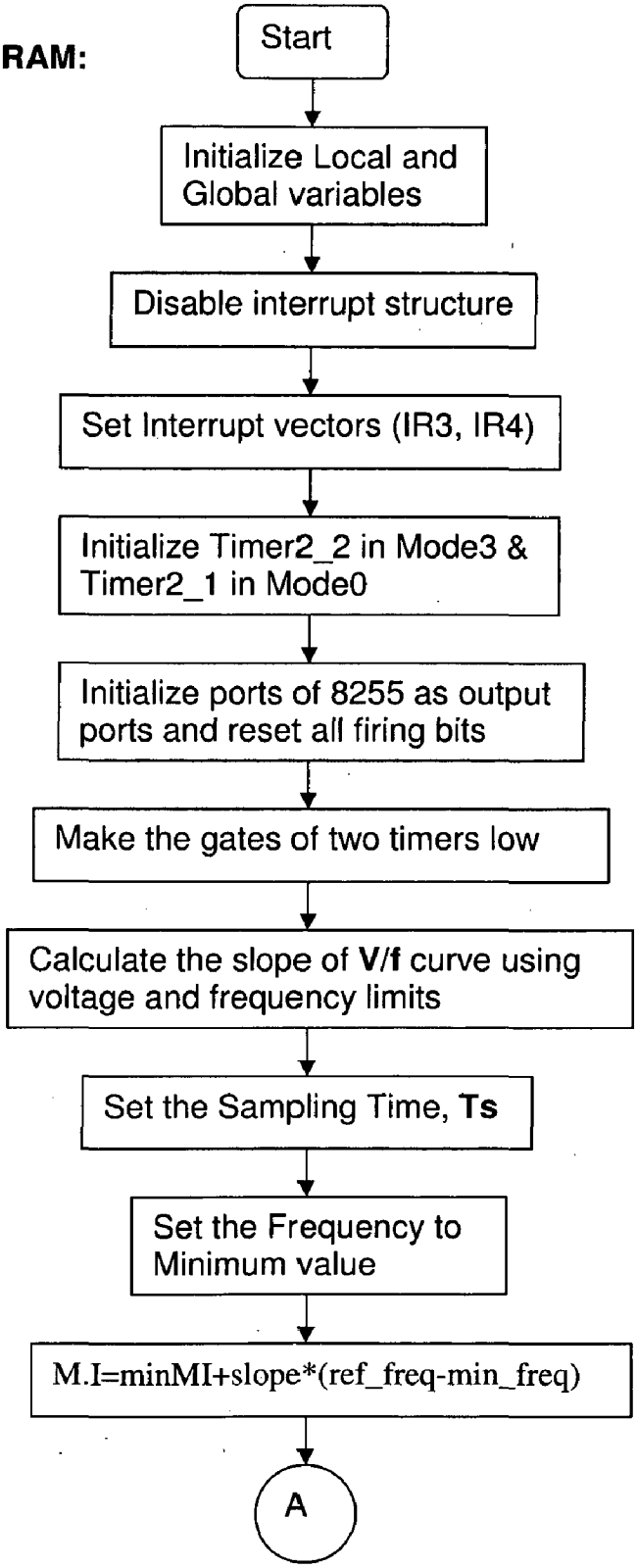


Fig.7.15. V/f CONTROL OF THREE-PHASE INVERTER

Software for the Open Loop V/Hz control of Three-phase Inverter fed Induction Motor Drive shown in Fig. consists of main program and Ts_ISR2L, TaTbTc_ISR2L interrupt service subroutines. The flow chart for main program is same as that of Neutral-Point Clamped Inverter as given Fig.7.16. V/f control is achieved in the same manner as discussed above. Flow charts given in Fig.7.21, 7.22 explains open loop V/f control of Conventional Three-phase Inverter

MAIN PROGRAM:



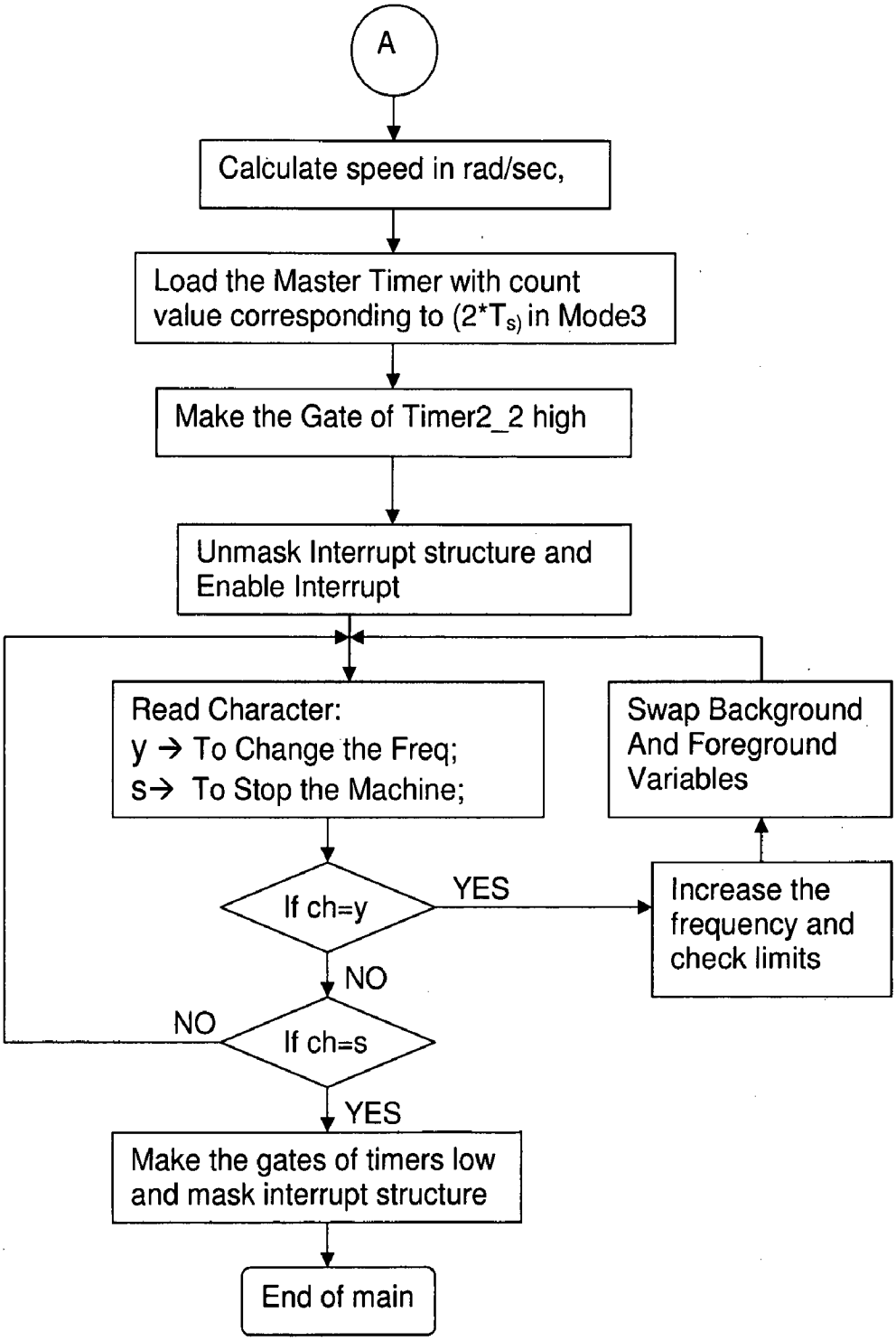
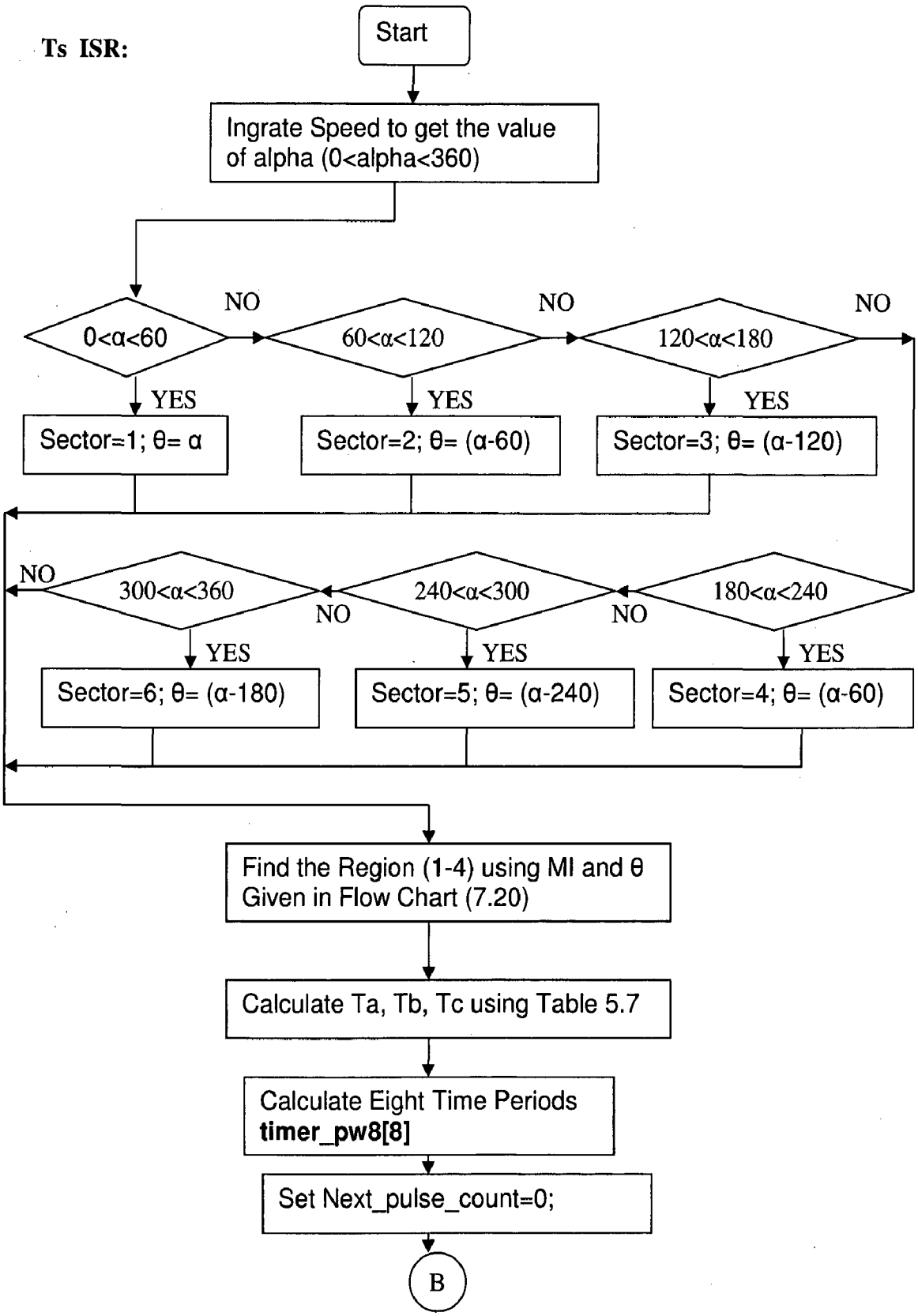


Fig.7.16. Main Program for Open Loop V/f Control of NPC Inverter

Ts ISR:


Start
Ingrate Speed to get the value of alpha (0<alpha<360)
0<α<60
NO
60<α<120
NO
120<α<180
NO
YES
YES
YES
Sector=1; θ= α
Sector=2; θ= (α-60)
Sector=3; θ= (α-120)
NO
300<α<360
NO
240<α<300
NO
180<α<240
YES
YES
YES
Sector=6; θ= (α-180)
Sector=5; θ= (α-240)
Sector=4; θ= (α-60)
Find the Region (1-4) using MI and θ Given in Flow Chart (7.20)
Calculate Ta, Tb, Tc using Table 5.7
Calculate Eight Time Periods timer_pw8[8]
Set Next_pulse_count=0;
B

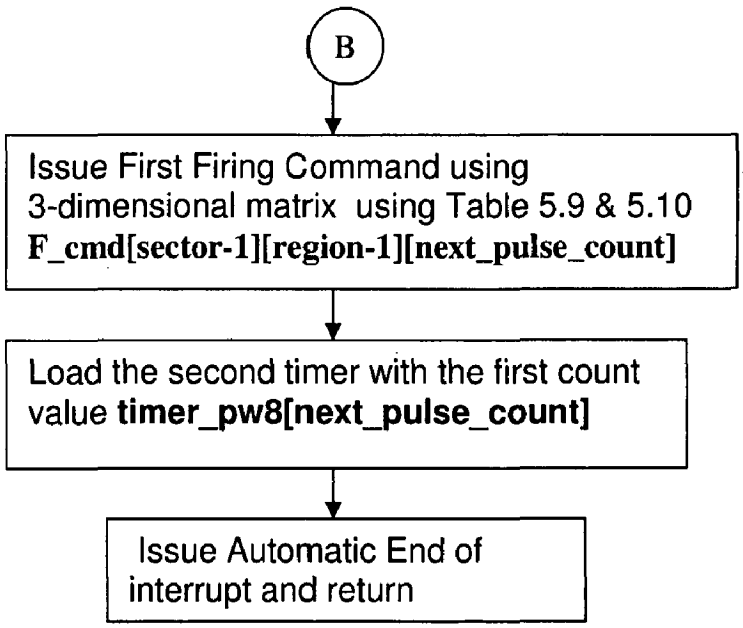


Fig. 7.17 Ts_ISR for Open Loop V/f Control of NPC Inverter

TaTbTc_ISR:

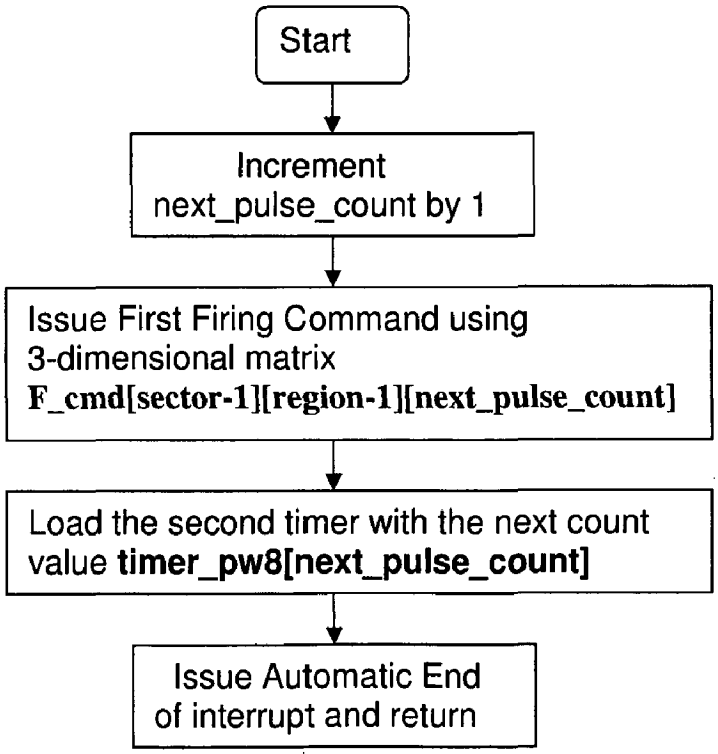


Fig. 7.18 TaTbTc_ISR for Open Loop V/f Control of NPC Inverter

How to find the region using MOD_INDEX and θ values

Fig.7.19 shows Regions in sector 1. By using simple geometry various points can be calculated as shown below.

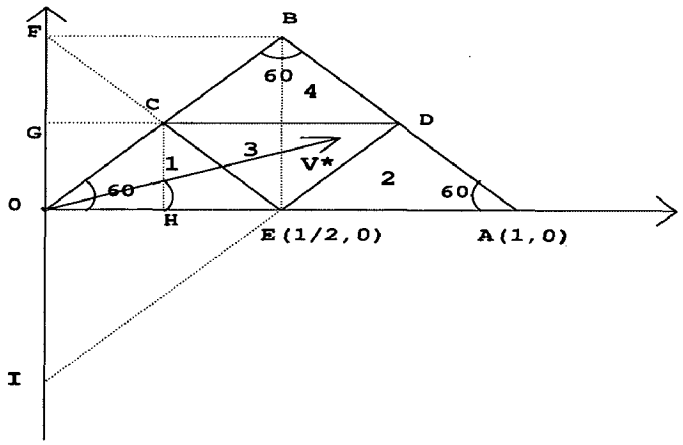


Fig.6.19. Regions In Sector 1

$$E\left(\frac{1}{2},0\right);C\left(\frac{1}{4},\frac{\sqrt{3}}{4}\right);H\left(\frac{1}{4},0\right);I\left(0,-\frac{\sqrt{3}}{2}\right);G\left(0,\frac{\sqrt{3}}{4}\right);F\left(0,\frac{\sqrt{3}}{2}\right)$$

Let length of line OA=1;

Slope of line CE, m1$=-\sqrt{3}$

CE Line Equation $y_1=-\sqrt{3}x_1+c_1$ **(7.5)**

At point $C\left(\frac{1}{4},\frac{\sqrt{3}}{4}\right)$, eq., (1) becomes $\frac{\sqrt{3}}{4}=-\frac{\sqrt{3}}{4}+c_1 \rightarrow c_1=\frac{\sqrt{3}}{2}$

CE line Equation $y_1=-\sqrt{3}x_1+\frac{\sqrt{3}}{2}$ **(7.6)**

Similarly; Slope of line DE or EI, $m_2=\sqrt{3}$

DE Line Equation $y_2=\sqrt{3}x_2+c_2$ **(7.7)**

At point, $E\left(\frac{1}{2},0\right)$, e.q(2) becomes $0=\frac{\sqrt{3}}{2}+c_2 \rightarrow c_2=-\frac{\sqrt{3}}{2}$

DE line Equation, $y_2=\sqrt{3}x_2-\frac{\sqrt{3}}{2}$ **(7.8)**

DC line Equation, $y_3=\frac{\sqrt{3}}{4}$ **(7.9)**

Using Eqs.7.6, 7.8 and 7.9 we can find the region of reference vector at any point;

Below Algorithm explains the above procedure.

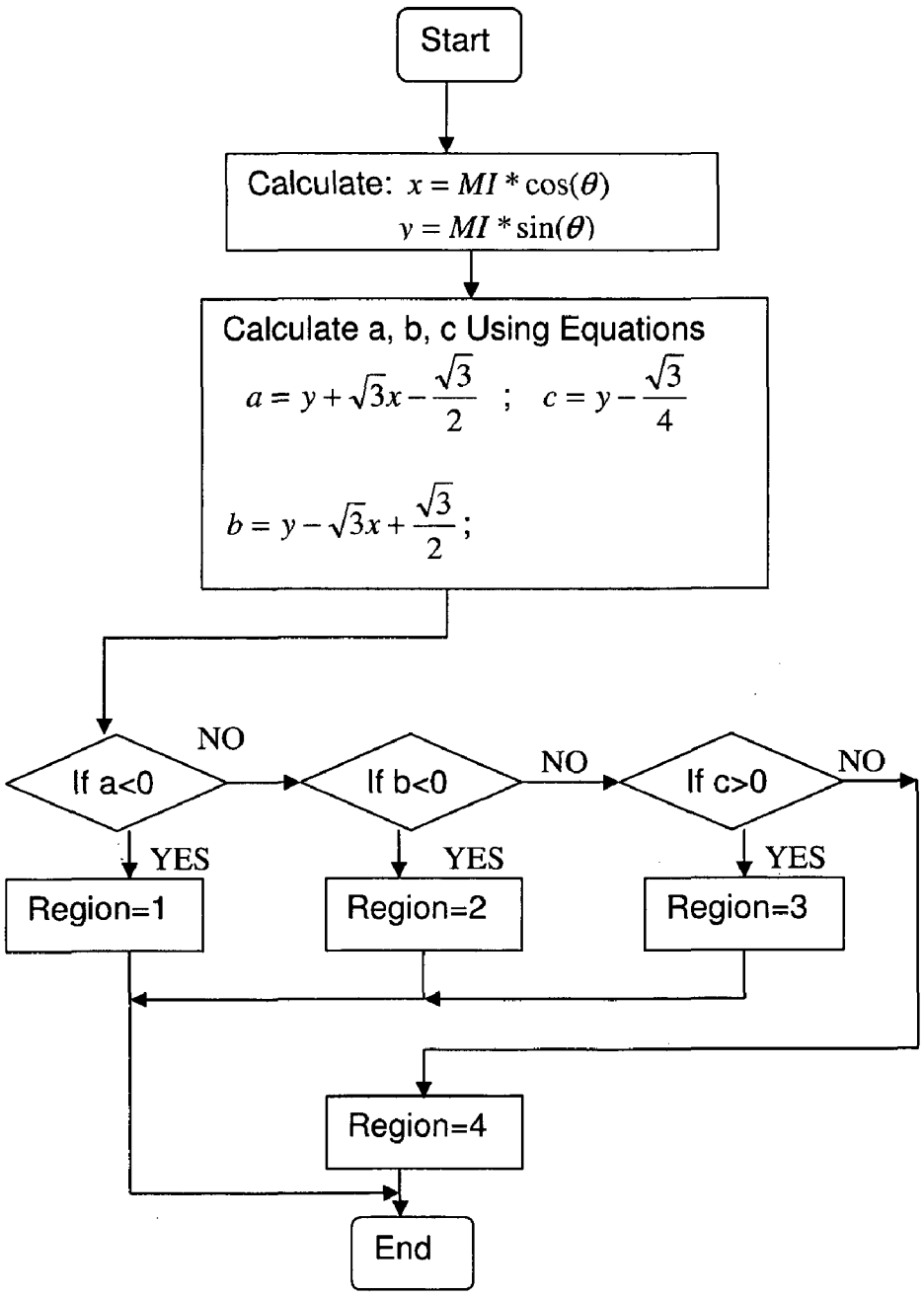
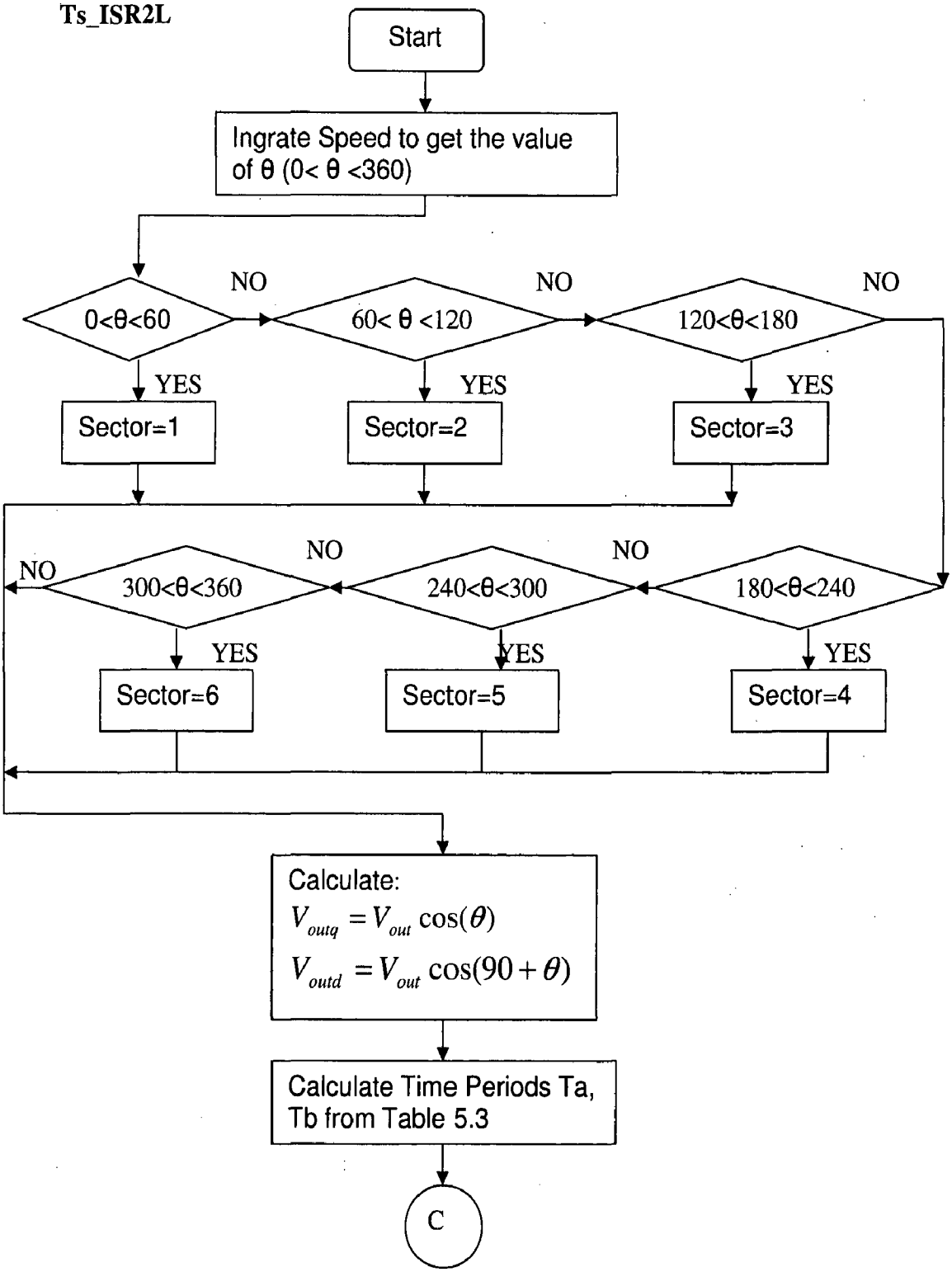


Fig.7.20.Flow chart for the selection of region

Ts_ISR2L


Start
Ingrate Speed to get the value of θ (0< θ <360)
0<θ<60
NO
60< θ <120
NO
120<θ<180
NO
YES
Sector=1
YES
Sector=2
YES
Sector=3
NO
300<θ<360
NO
240<θ<300
NO
180<θ<240
YES
Sector=6
YES
Sector=5
YES
Sector=4
Calculate:
$V_{outq} = V_{out}\cos(\theta)$
$V_{outd} = V_{out}\cos(90+\theta)$
Calculate Time Periods Ta, Tb from Table 5.3
C

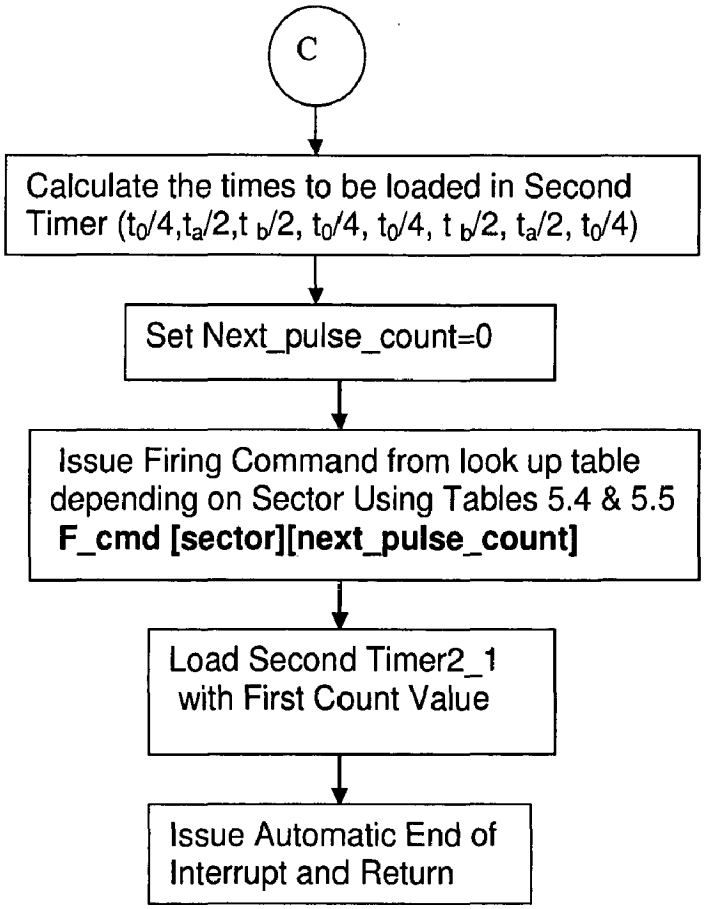


Fig.7.21. Ts_ISR2l for Open Loop V/f Control of Three-phase Inverter

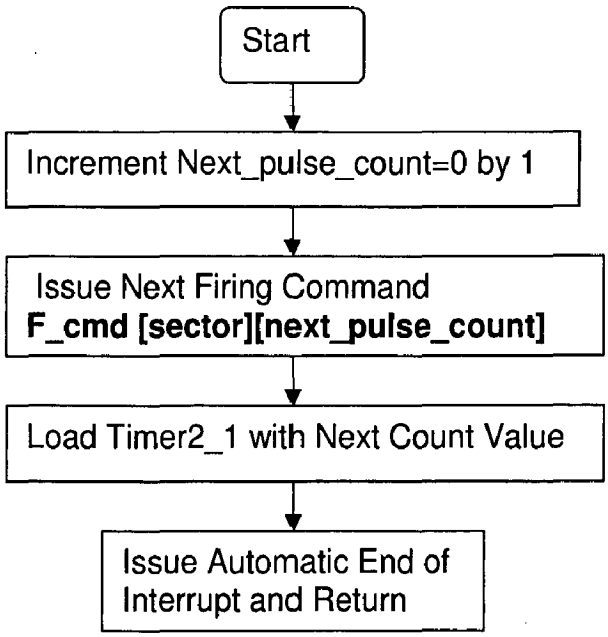


Fig.7.22. TaTbTc_ISR2l for Open Loop V/f Control of Three-phase Inverter

7.4. IMPLEMENTATION OF FOC FOR INDUCTION MOTOR DRIVE

The complete Software for the Field Oriented Control (FOC) of induction motor is divided into following modules. Each module is explained briefly with the flowcharts given below.

- Main_Programe.
- Ts_INT Interrupt Service Subroutine.
- TaTbTc_INT Interrupt Service Subroutine.
- One_ms_INT Interrupt Service Subroutine.

The flow chart for the Main_Program is given in Fig 7.24. Program starts with the initialization of local variables, global variables, I/0 ports and 8253. Load the master timer (TIMER2_2) with the count value corresponding to 2*Ts and load TIMER1_2 with the count value corresponding to 1ms. Set the actual speed to zero Reference speed is inputted through keyboard. After the reference speed is accepted swap the local and global variables and make the gates of the above two timers high and wait for the interrupt to come. Same process is repeated until key presses is 's' to stop the machine.

The Flowcharts for the Ts_INT ISR and TaTbTc_INT ISR modules (Fig. 7.17 and Fig. 7.18) are same as explained above for open loop V/f control of Induction Motor.

Flow chart for one_ms_INT interrupt service subroutine is given in Fig.7.29. It is subdivided into the current measurement, current PI processing, speed measurement, speed PI processing, Clark's Transformation. It gives the magnitude of the reference voltage vector (V*) and θ_e which are inputted to the Ts_INT ISR.

Current Measurement

Current Measurement is done for every 1 ms using PCL812 A/D card. The process of the current measurement is explained below with the help of flowchart given in Fig.7.25.

- Set the input channel by specifying the mux scan range.
- Write the pacer trigger mode to the control register.
- Wait for the EOC by reading the A/D high data byte register
- Read the data from A/D converter by reading the A/D data register.
- Data conversion by converting the binary A/D data to an integer

I_{QS} Current PI Processing Subroutine

The electrical time constant of the drive is less, than mechanical time constant therefore current PI is done at every 1ms. This I_{QS} current PI processing gives the reference value of output voltage along q-direction (Vq) in synchronously rotating reference frame; it can be expressed mathematically as below, and flow chart is given Fig.7.26.

$$V_q(n) = V_q(n-1) + K_{pi}\left[e_i(n) - e_i(n-1)\right] + K_{ii}e_i(n) \qquad \textbf{(7.10)}$$

where,

$e_i(n)$ = Current error between reference i_{qs} and actual i_{qs} at n^{th} sampling instant.

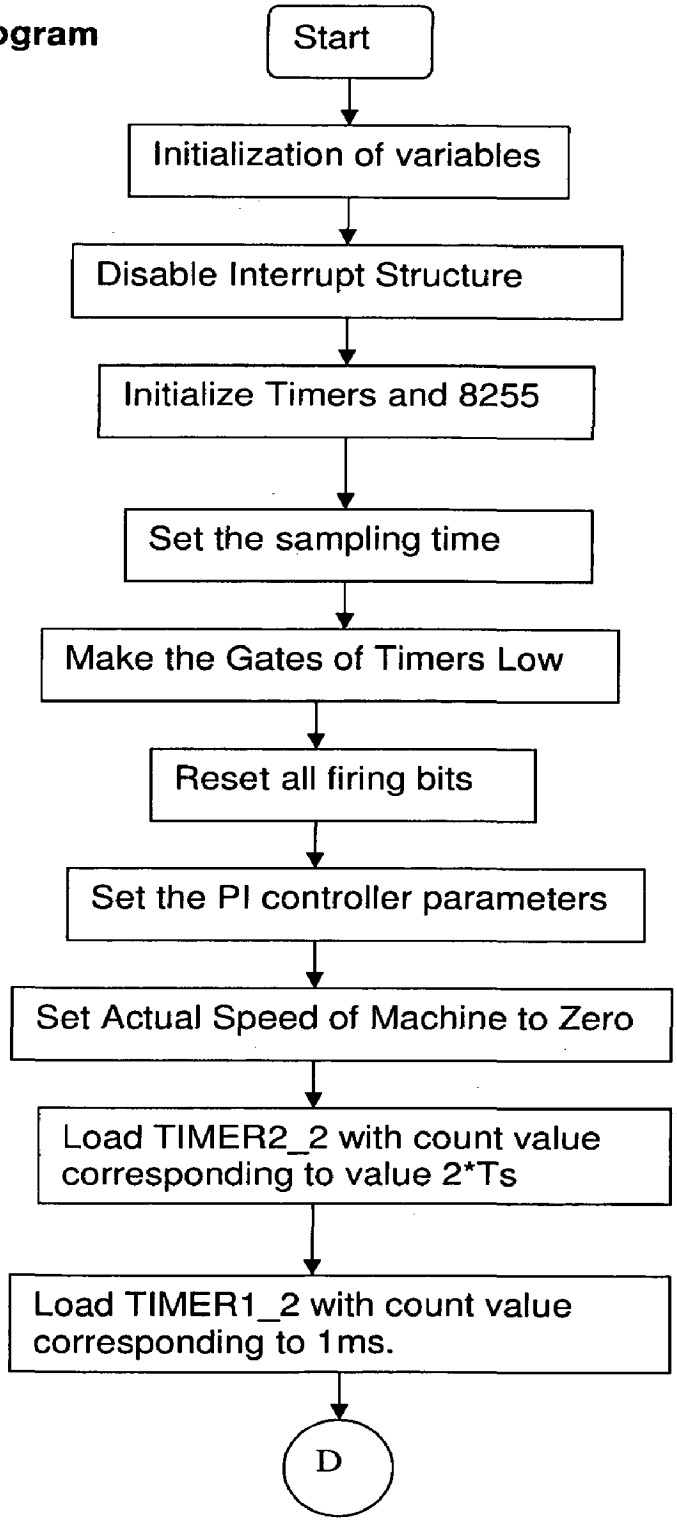
$e_i(n-1)$ = Current error between reference i_{qs} and actual i_{qs} at $(n-1)^{th}$ sampling instant.

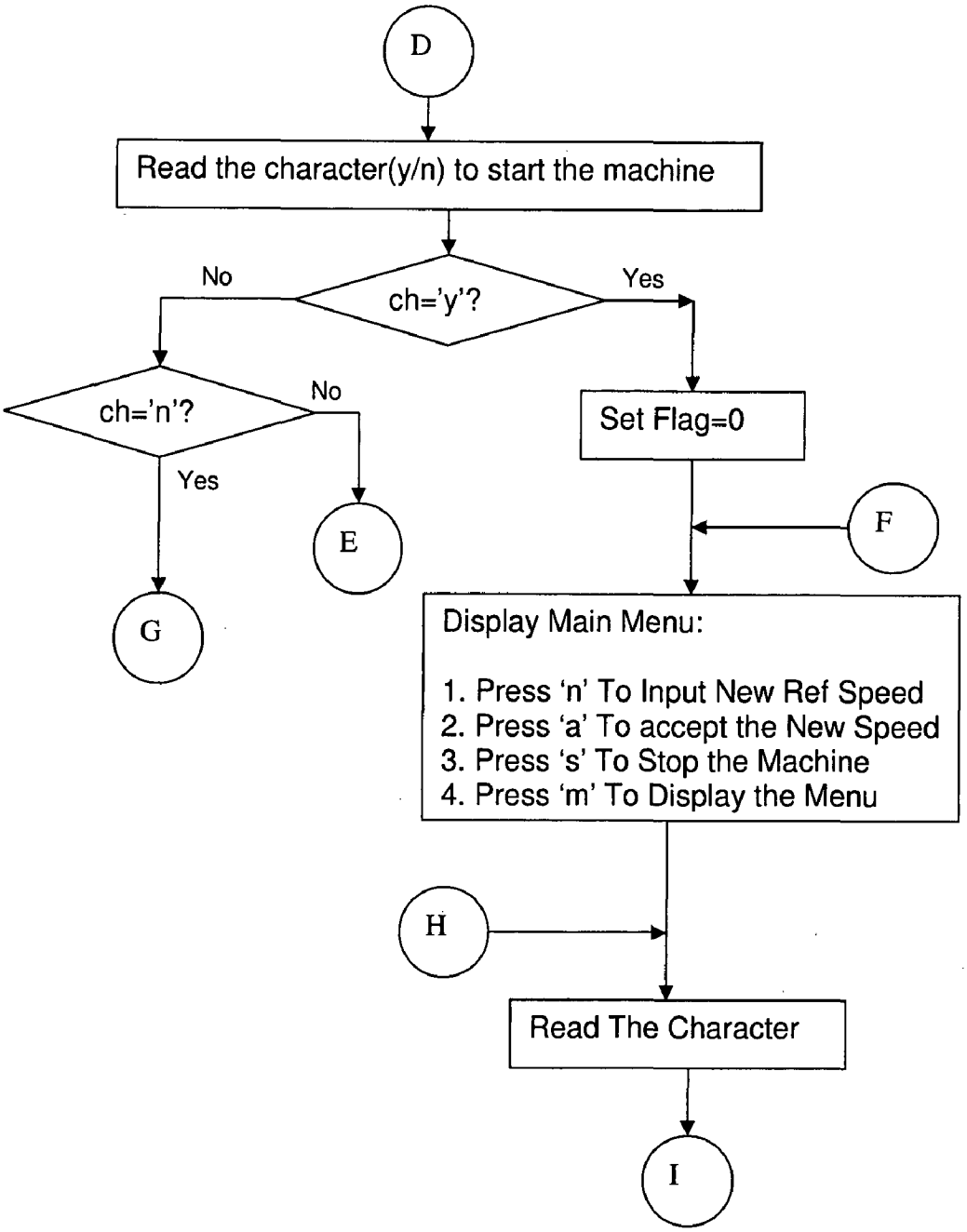
$V_q(n)$ = PI controller output at n^{th} sampling instant.

$V_q(n-1)$ = PI controller output at $(n-1)^{th}$ sampling instant.

Ts = Sampling time of current loop.

FOC Main Program




D
Read the character(y/n) to start the machine
No
ch='y'?
Yes
ch='n'?
No
Yes
Set Flag=0
F
E
G
Display Main Menu:
1. Press 'n' To Input New Ref Speed
2. Press 'a' To accept the New Speed
3. Press 's' To Stop the Machine
4. Press 'm' To Display the Menu
H
Read The Character
I

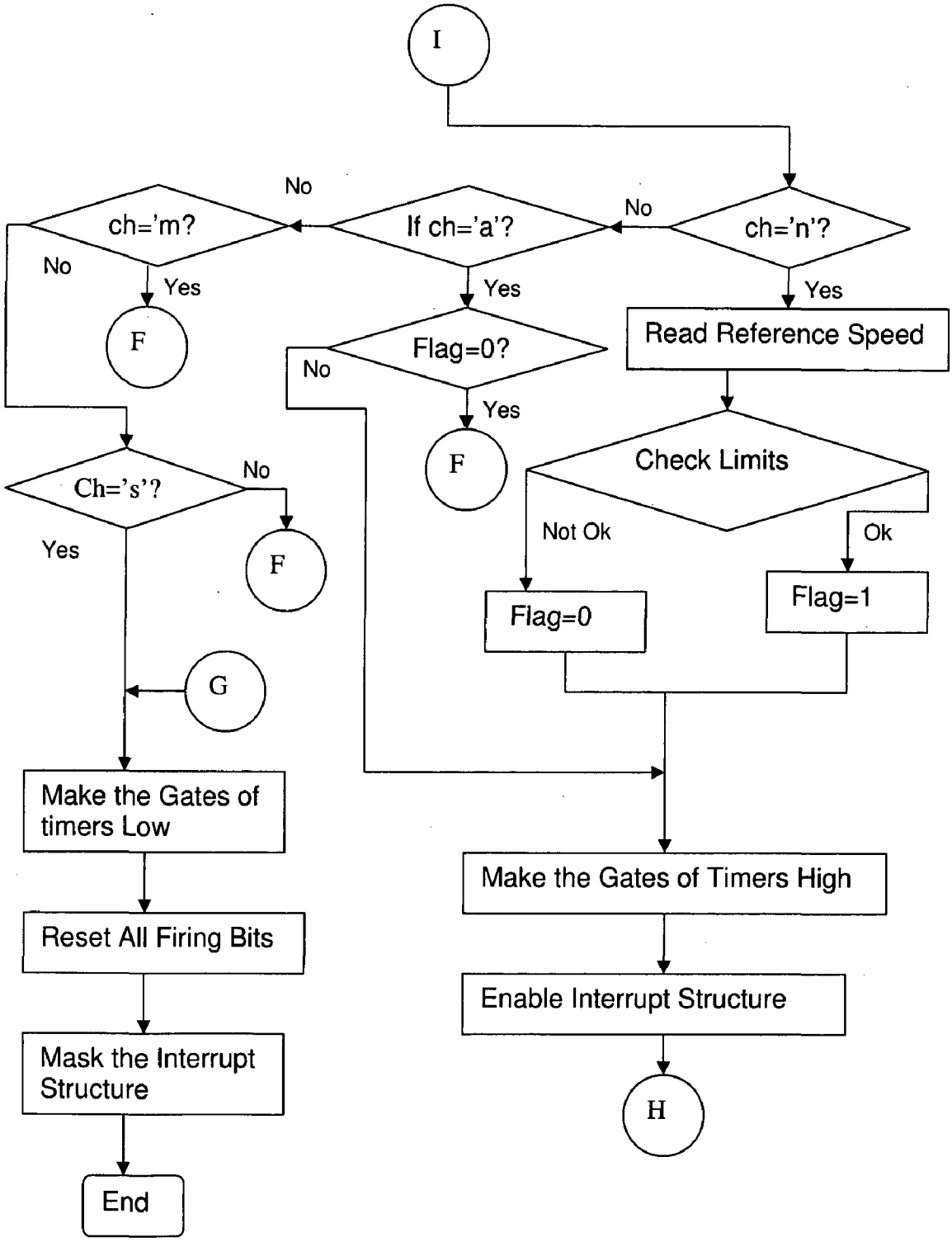
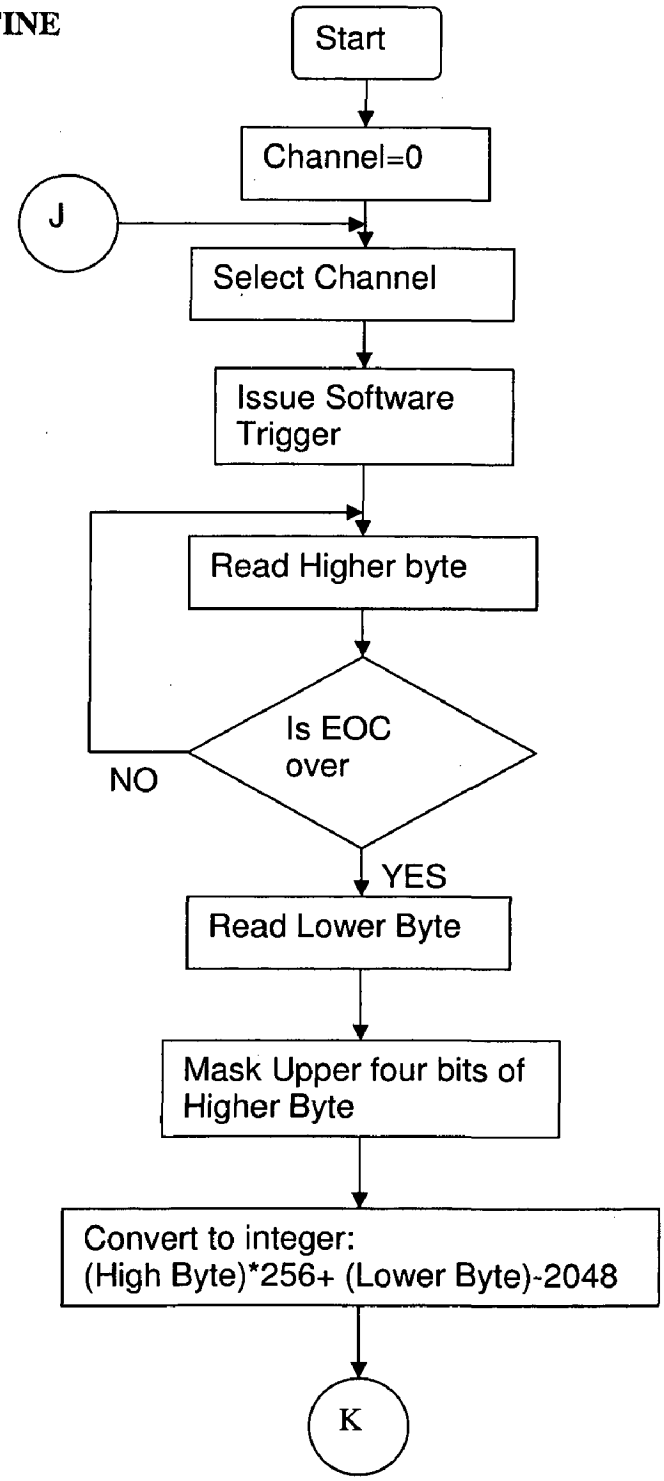


Fig.7.24 FOC Main Program Flow Chart

CURRENT SENSING SUBROUTINE



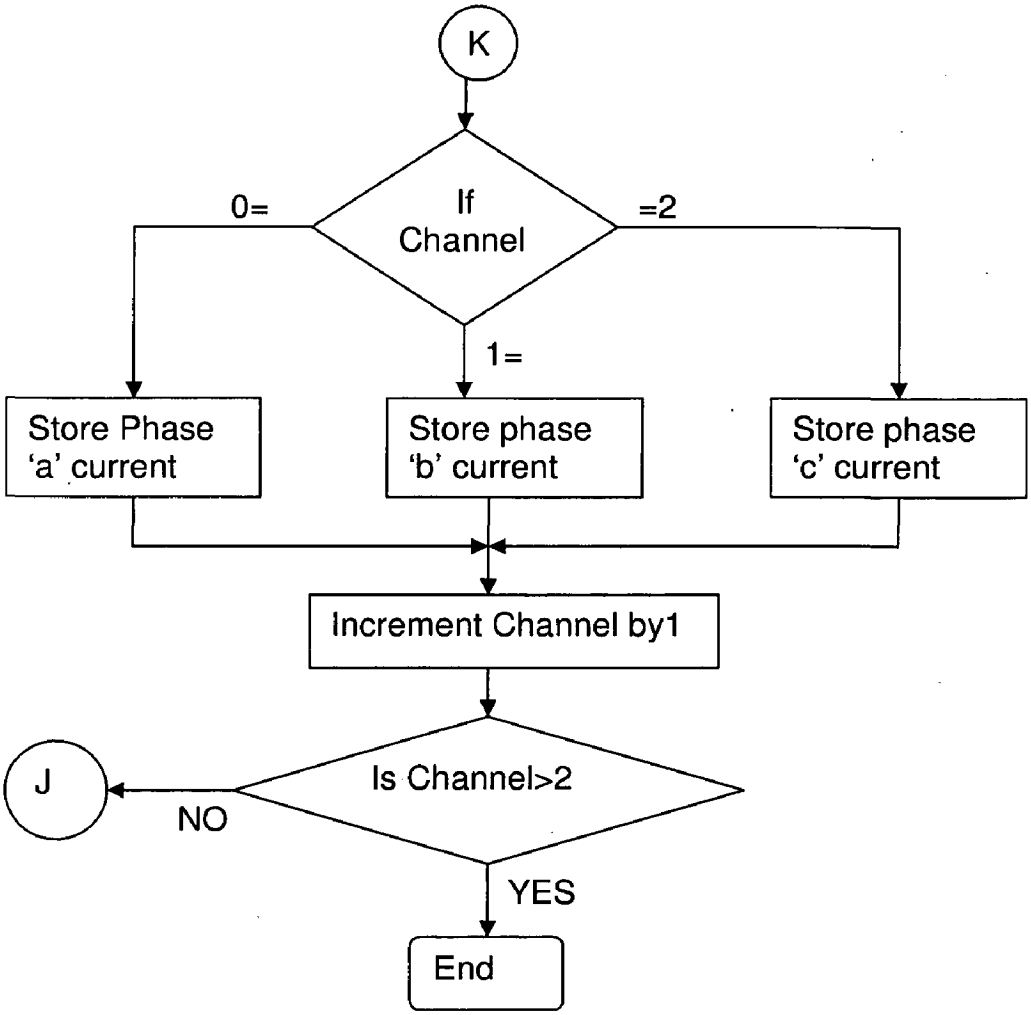


Fig.7.25 Current Measurement Subroutine

I_{DS} Current PI Processing Subroutine

This IDS current PI processing gives the reference value of output voltage along d-direction (V_d) in synchronously rotating reference frame, it can be expressed mathematically as below and its Flow chart is given in Fig.7.27.

$$V_d(n) = V_d(n-1) + K_{pi}\left[e_i(n) - e_i(n-1)\right] + K_{ii}e_i(n) \qquad (7.11)$$

where,

$e_i(n)$ = Current error between reference i_{ds} and actual i_{ds} at n^{th} sampling instant.

$e_i(n\text{-}1)$ = Current error between reference i_{ds} and actual i_{ds} at $(n\text{-}1)^{th}$ sampling instant.

$V_d(n)$ = PI controller output at n^{th} sampling instant.

$V_d(n\text{-}1)$ = PI controller output at $(n\text{-}1)^{th}$ sampling instant.

Ts = Sampling time of current loop.

Speed Measurement and Speed PI Processing

Speed measurement is done for every 10ms and the flow chart for the speed measurement is included in one_ms_INT ISR (Fig.7.29). The speed of the motor is measured at every 10ms; reference speed is inputted to PC through keyboard. The speed PI processing is done to obtain the reference value of torque component current (i^*_{qs}). It can be expressed as below and its flow chart is given in Fig 7.28.

$$i^*_{qs}(n) = i^*_{qs}(n-1) + K_{pspd}\left[\varpi_{err}(n) - \varpi_{err}(n-1)\right] + K_{ispd} * T_s * \varpi_{err}(n) \qquad (7.12)$$

Where,

$i^*_{qs}(n)$ = Reference value of torque producing current at n^{th} sampling instant.

$i^*_{qs}(n-1)$ = Reference value of torque producing current at $(n\text{-}1)^{th}$ sampling instant.

$\varpi_{err}(n)$ = speed error at n^{th} sampling instant.

$\varpi_{err}(n-1)$ = speed error at $(n\text{-}1)^{th}$ sampling instant.

T_s= Sampling rate of speed loop.

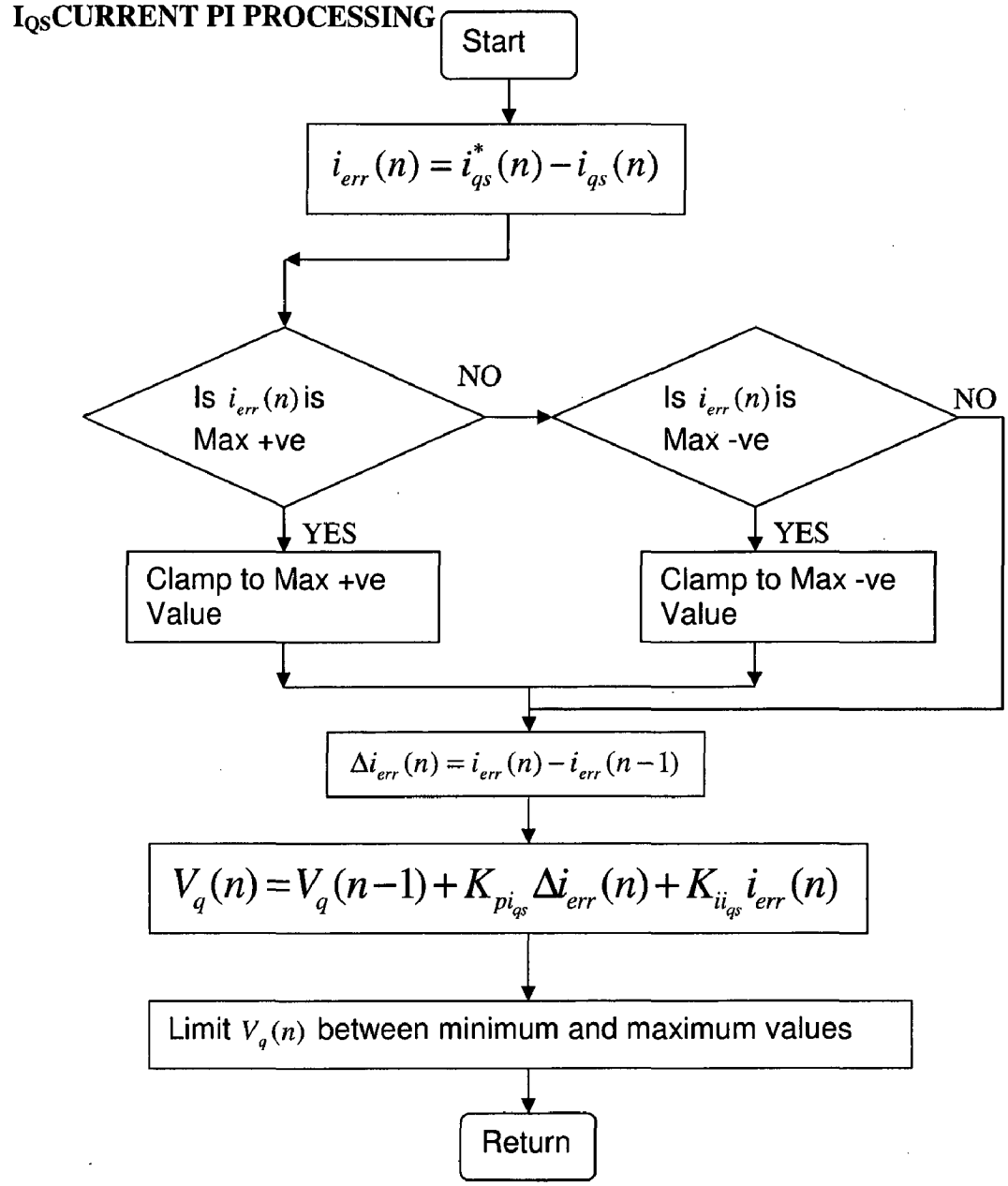


Fig. 7.26 I_{QS} current PI Processing Subroutine

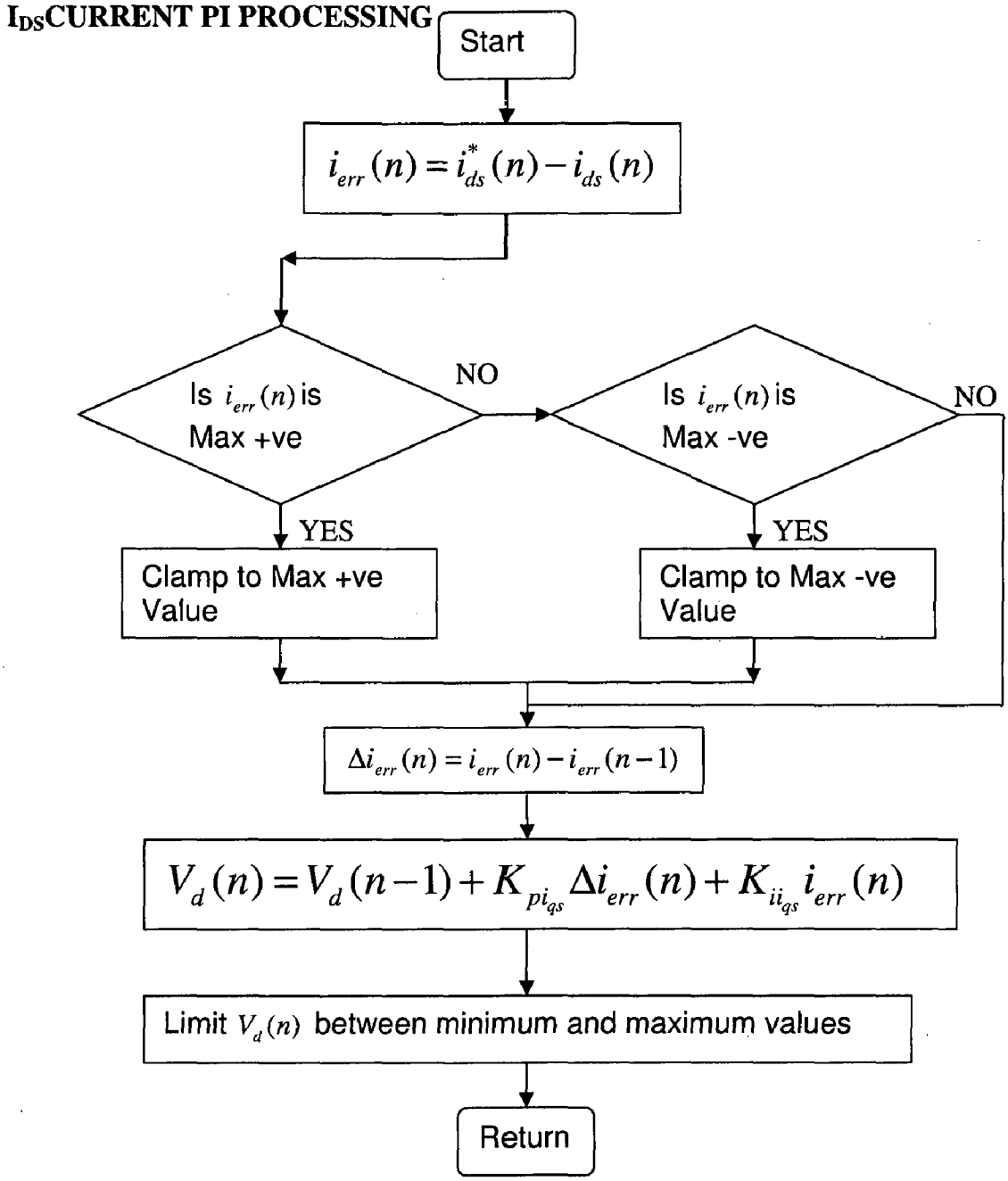


Fig. 7.27 I_{DS} Current PI Processing Subroutine

SPEED PI PROCESSING

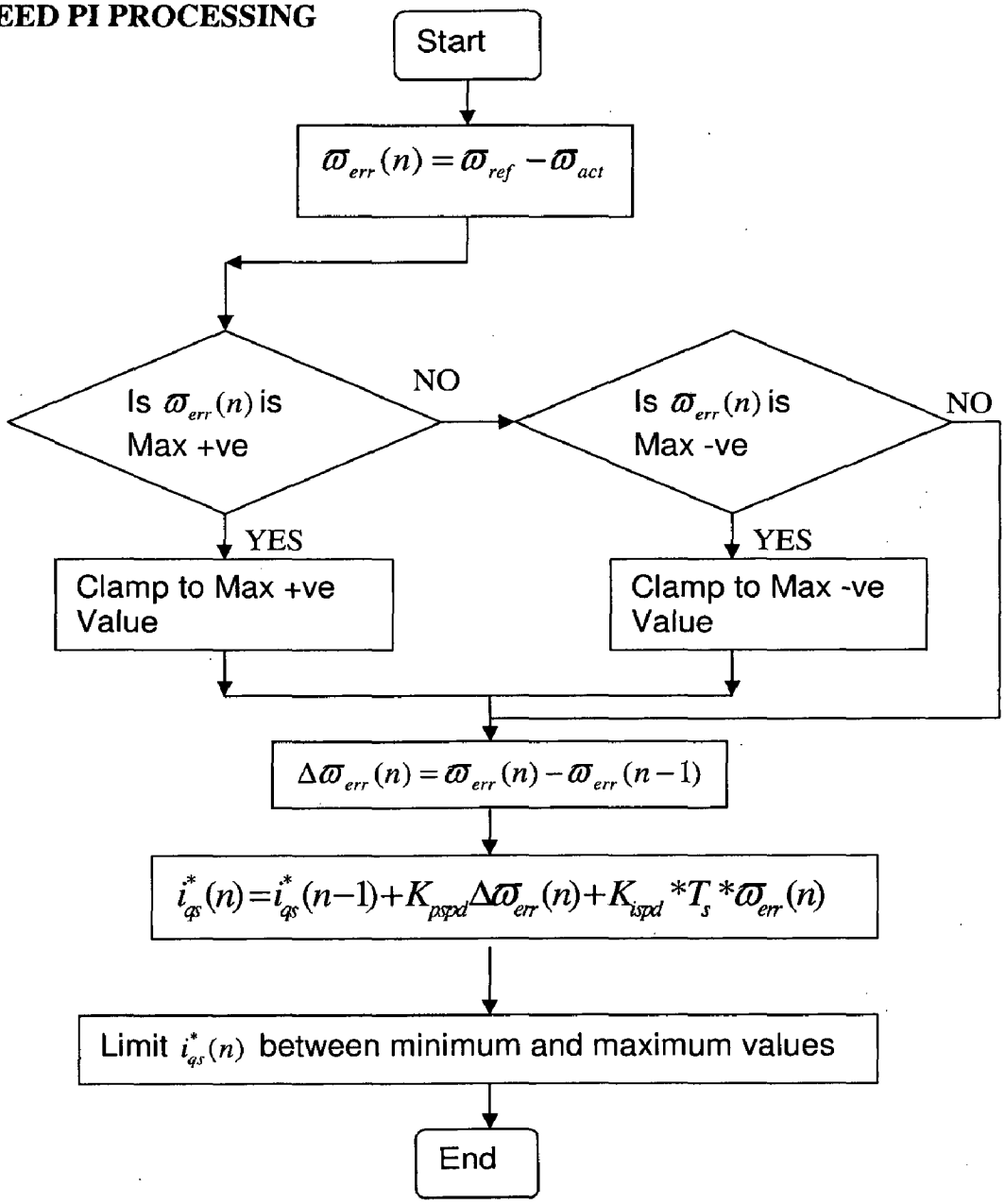
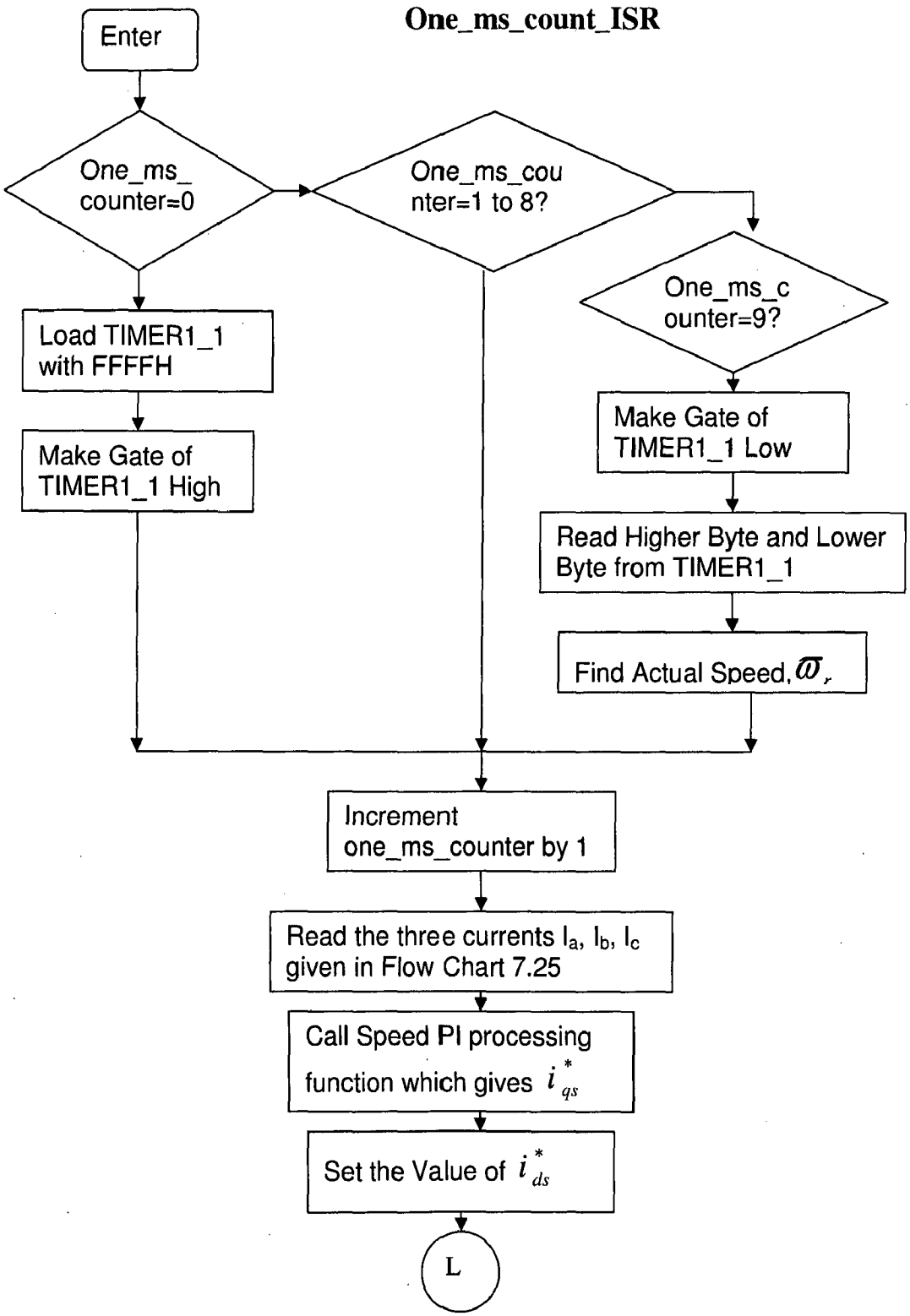


Fig.7.28 Speed PI Processing Subroutine


One_ms_count_ISR
Enter
One_ms_ counter=0
One_ms_cou nter=1 to 8?
One_ms_c ounter=9?
Load TIMER1_1 with FFFFH
Make Gate of TIMER1_1 High
Make Gate of TIMER1_1 Low
Read Higher Byte and Lower Byte from TIMER1_1
Find Actual Speed, ω_r
Increment one_ms_counter by 1
Read the three currents I_a, I_b, I_c given in Flow Chart 7.25
Call Speed PI processing function which gives i_{qs}^*
Set the Value of i_{ds}^*
L

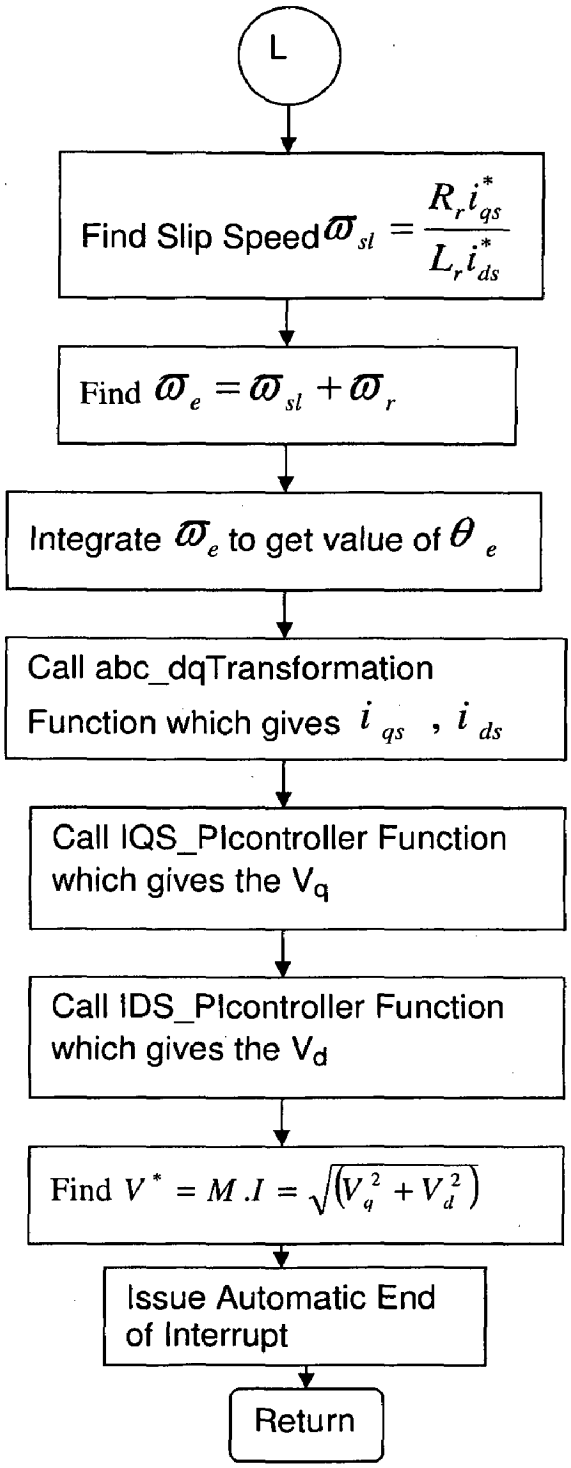


Fig. 7.29 Flow Chart for one_ms_count ISR

CHAPTER 8

EXPERIMENTAL RESULTS

In chapter-7 it has been seen how the system prototype was developed. In this chapter the results of the experimentation carried on this system are presented. Performance of both the three phase inverter and Neutral-point Clamped Inverters was investigated separately using Space Vector Modulation for different kind of loads. It is shown that improvement in THD for both voltage and current from Sinusoidal PWM as shown in simulation to Space Vector Modulation. Finally Open-loop V/f control of Induction Drive has been achieved experimentally using both Three-phase Inverter and Neutral-Point Clamped Inverter and it has been shown that motor currents are much more sinusoidal having less THD using Space Vector Modulation.

Specifications

a) R-L load: R=10Ω and L=80 mH.

b) Induction Motor: 3-phase Squirrel Cage Induction Motor 1 HP, RPM-1440, Amp-1 A.

c) V_{DC}=180 V

8.1. PERFORMANCE INVESTIGATION OF NEUTRAL POINT CLAMPED THREE-LEVEL INVERTER

Fig 8.1 shows master timer output which goes to IR3 interrupt with a time period 0.3msec. Fig. 8.2 shows the firing pulses to the four MOSFETs in the same leg at different frequencies, Fig. 8.3 firing pulses to the three MOSFETs in same row in three-phases showing 120^0 phase shift and Fig. 8.4, Fig. 8.5 shows phase voltage, line voltage waveforms and harmonic spectrum at different frequencies respectively. At low frequencies the 3-level line voltages will resembles as 2-level line voltages as in Three-phase Inverter because of low modulation index. Fig. 8.6 and Fig. 8.7 show the Load current waveforms and Harmonic Spectrums for R-L Load for different frequencies respectively.

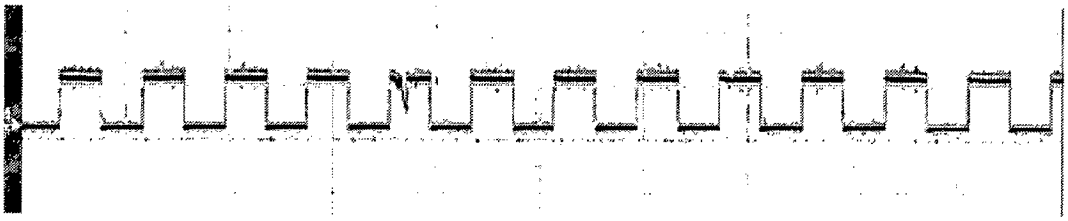


Fig. 8.1.Master Timer Output (0.5 ms/div)

Fig. 8.2(a) Firing Pulses to the MOSFET switches S_{u1},S_{u3},S_{u2},S_{u4} in same phase at 50 Hz(10ms/div)

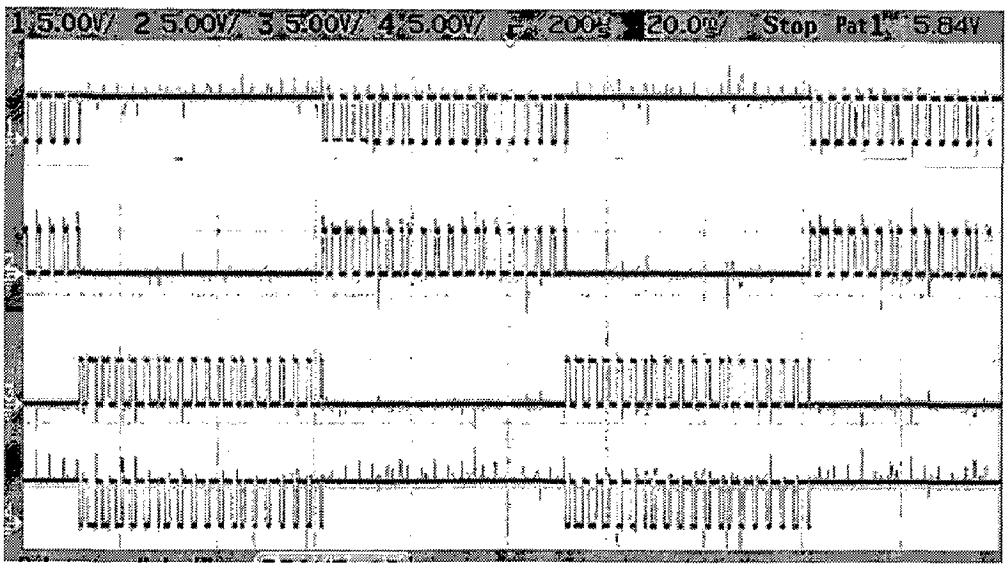


Fig. 8.2(b) Firing Pulses to the MOSFET switches S_{u1},S_{u3},S_{u2},S_{u4} in same phase at 10Hz (20ms/div)

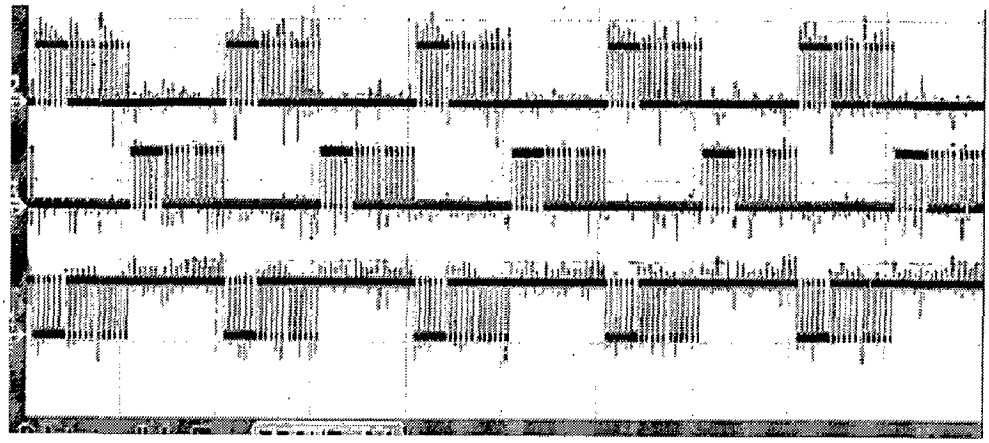


Fig. 8.3 Firing Pulses to the MOSFET switches S_{u1}, S_{v1}, S_{w1} in 3-phase at 50Hz (10ms/div)

Phase Voltages for R-L load at Different Frequencies

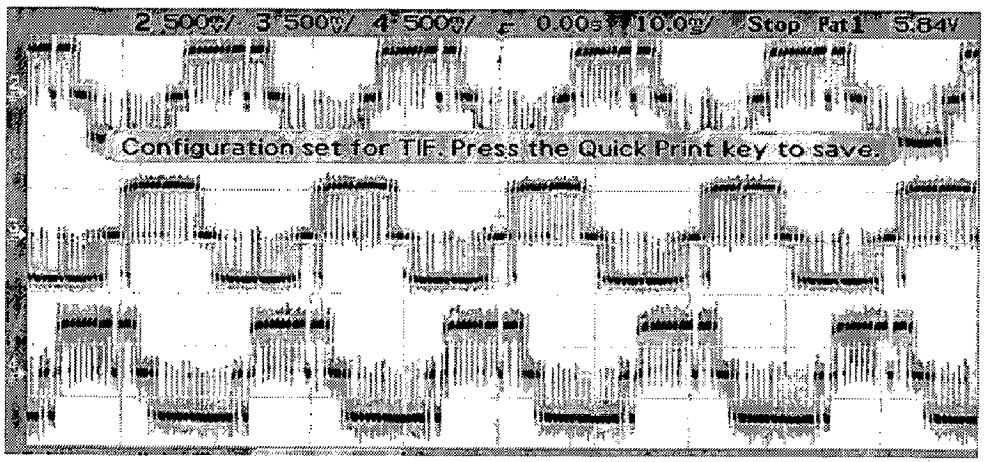


Fig. 8.4(a) Phase Voltages V_{uo}, V_{vo}, V_{wo} at a frequency 50 Hz (90V/div, 10ms/div)

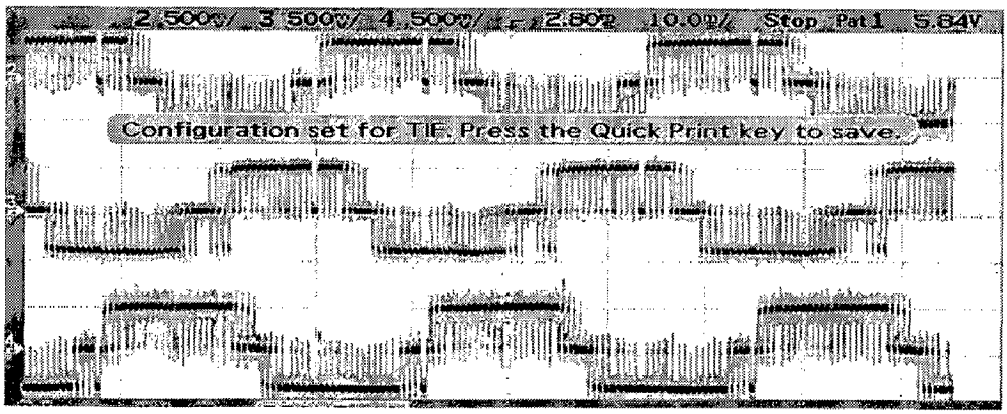


Fig. 8.4(b) Phase Voltages V_{uo}, V_{vo}, V_{wo} at a frequency 30 Hz (90V/div, 10ms/div)

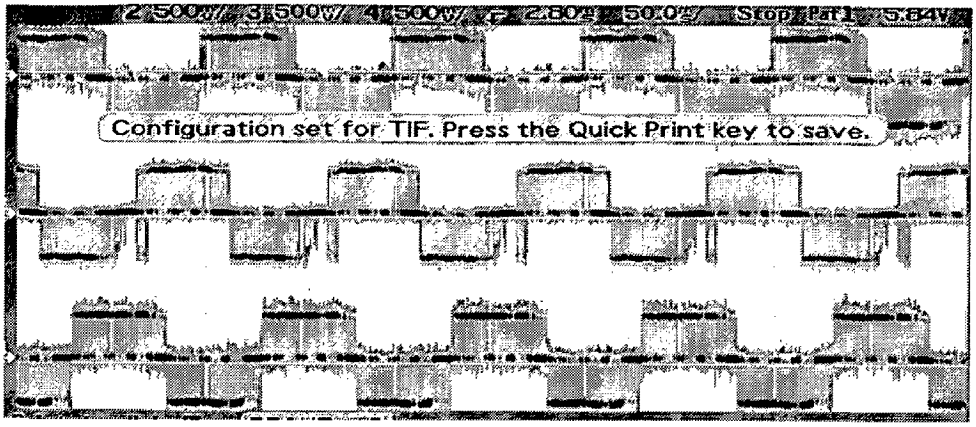


Fig. 8.4(c) Phase Voltages V_{uo}, V_{vo}, V_{wo} at a frequency 10 Hz (90V/div, 50ms/div)

Line-to-Line voltages for R-L load at Different Frequencies

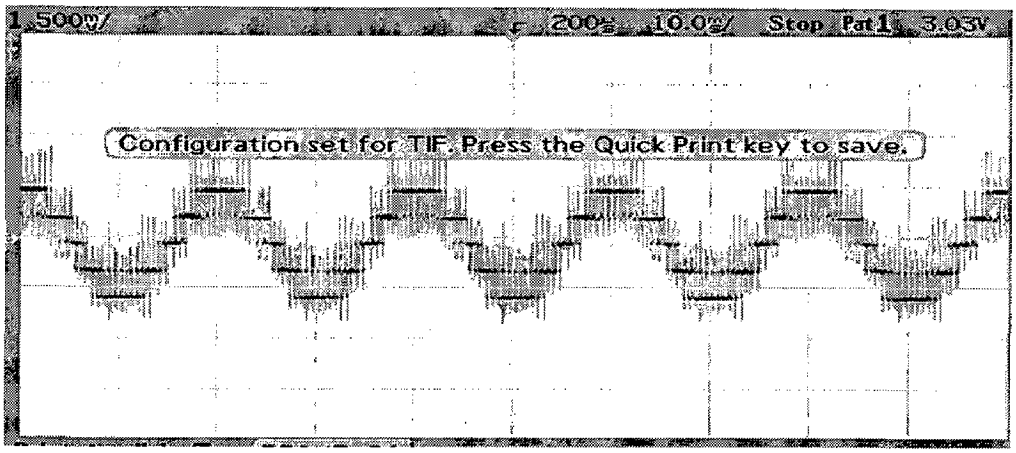


Fig. 8.5(a) Line-to-Line Voltage V_{uv} at a frequency 50Hz (180V/div,10ms/div)

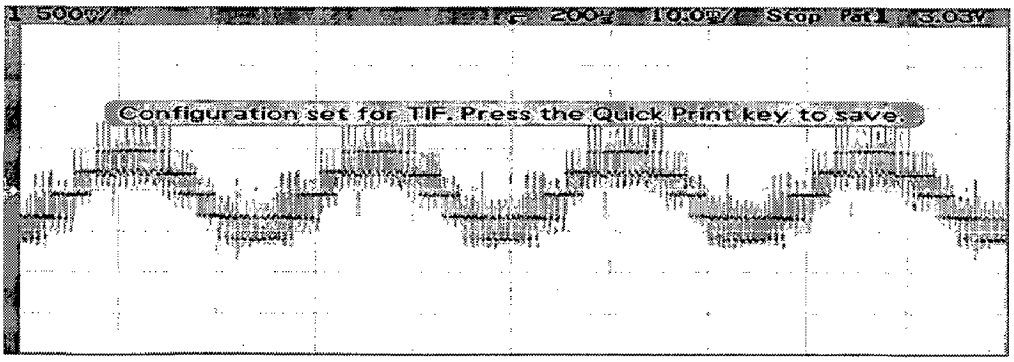


Fig. 8.5(b) Line-to-Line Voltage V_{uv} at a frequency 40 Hz (180V/div,10ms/div)

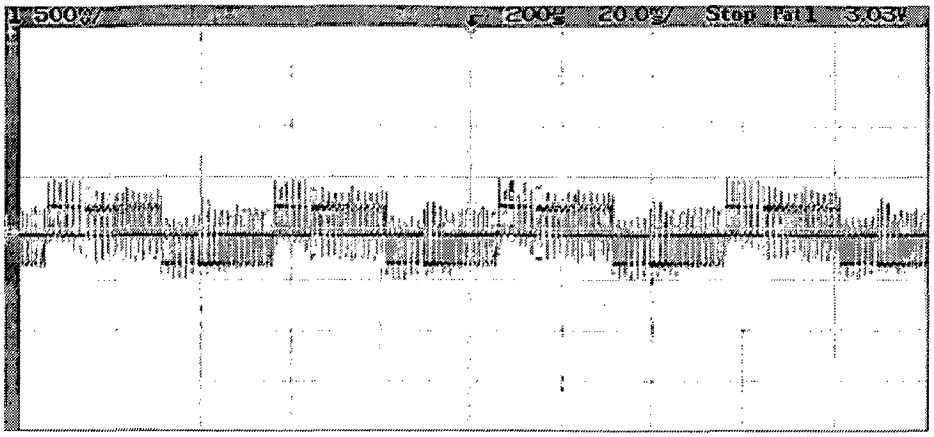


Fig. 8.5(c) Line-to-Line Voltage V_{uv} at a frequency 20 Hz (180V/div, 20ms/div)

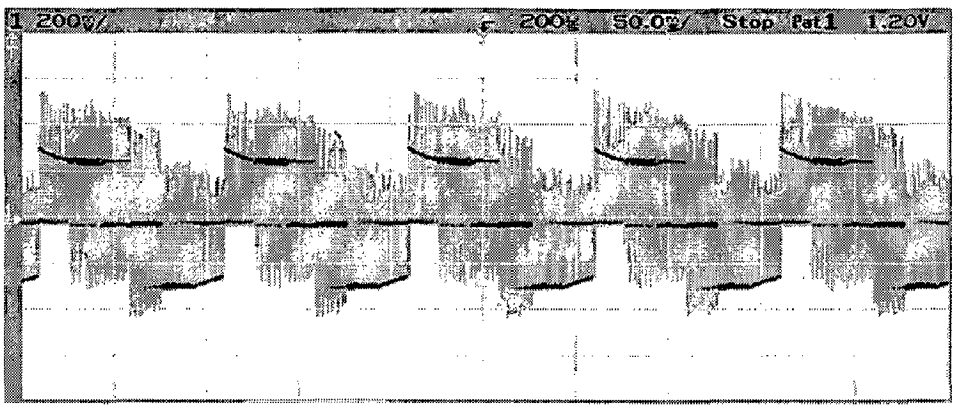


Fig. 8.5(d) Line-to-Line Voltage V_{uv} at a frequency 10Hz (180V/div, 50ms/div)

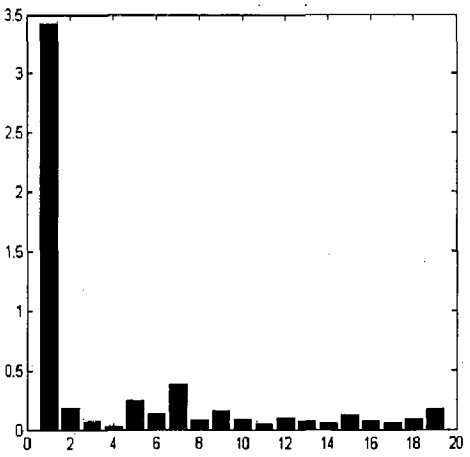


Fig. 8.5(e) At 50 Hz (THD=17.93)

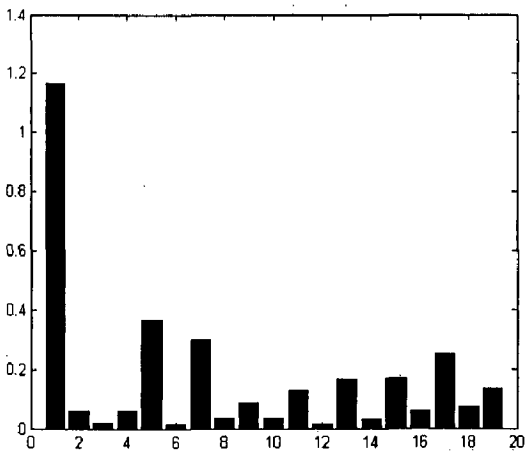


Fig. 8.5(f) At 20 Hz (THD=48.82)

Line currents for R-L load at Different Frequencies

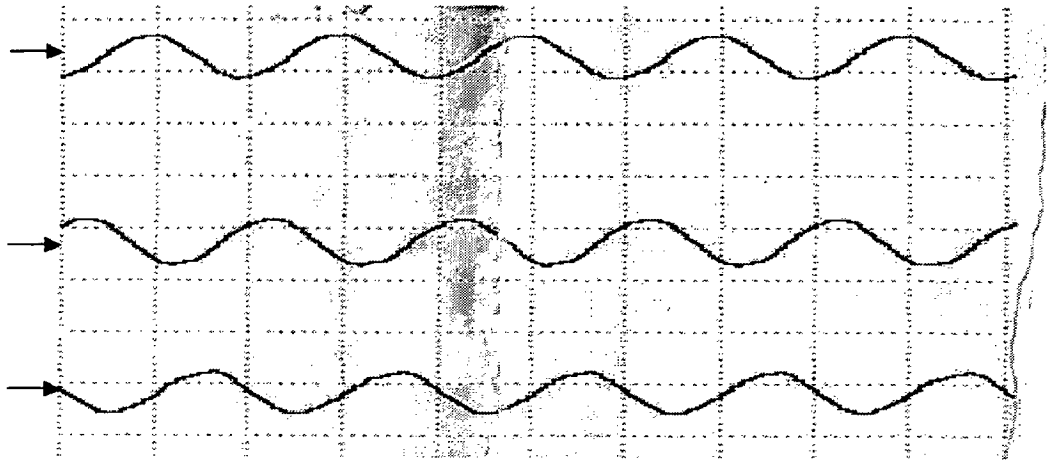


Fig. 8.6(a) Line Currents at 50 Hz (1 A/div, 10ms/div)

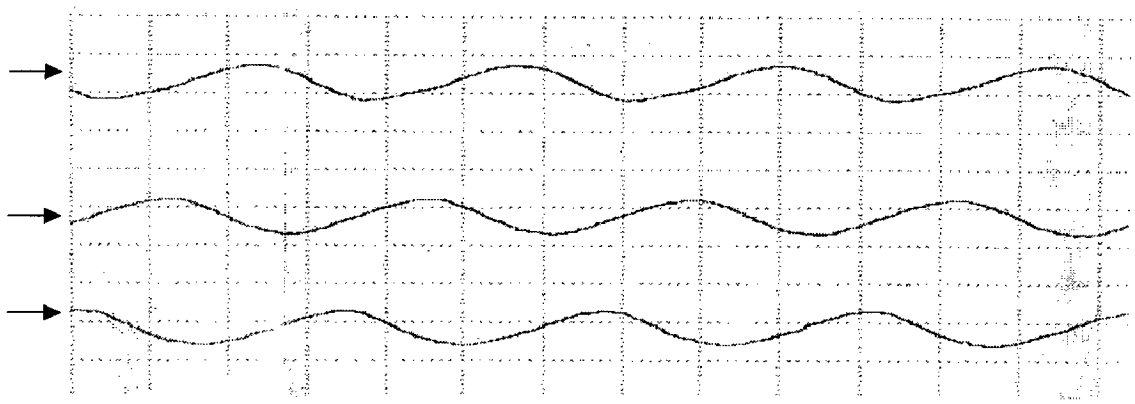


Fig. 8.6(b) Line Currents at 30 Hz (1 A/div, 10ms/div)

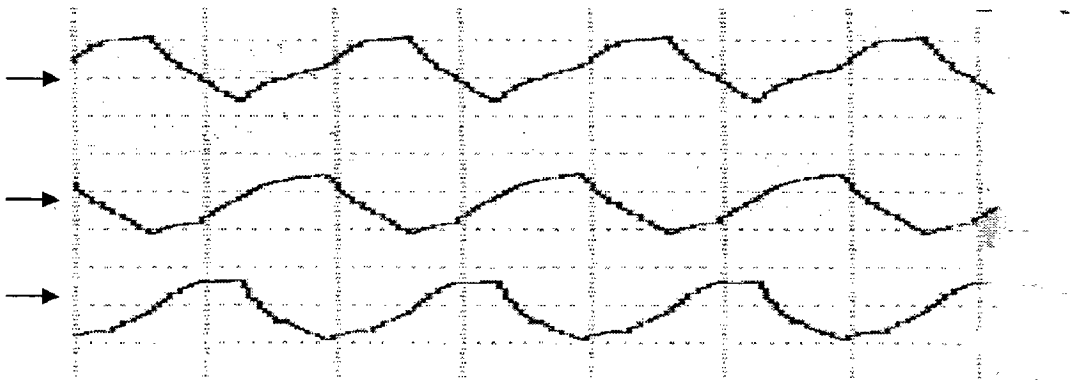
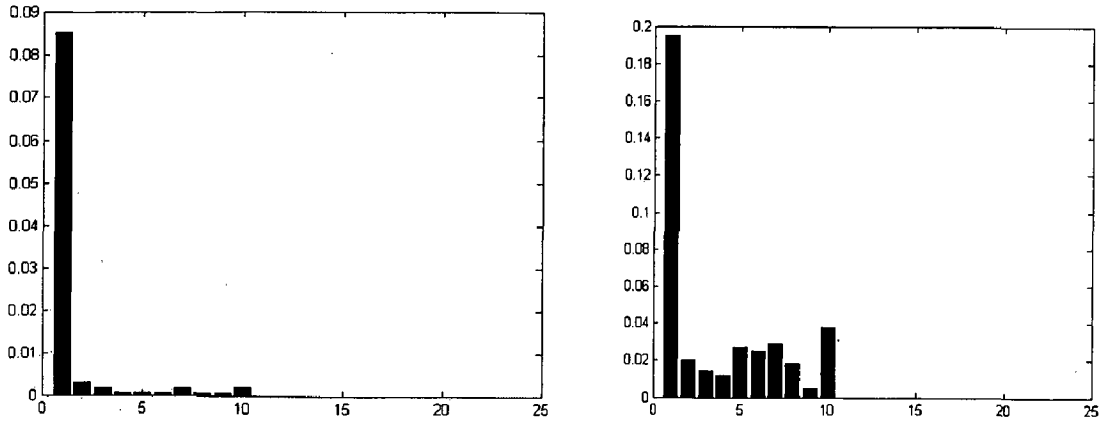


Fig. 8.6(c) Line Currents at 10 Hz (1 A/div, 50ms/div)

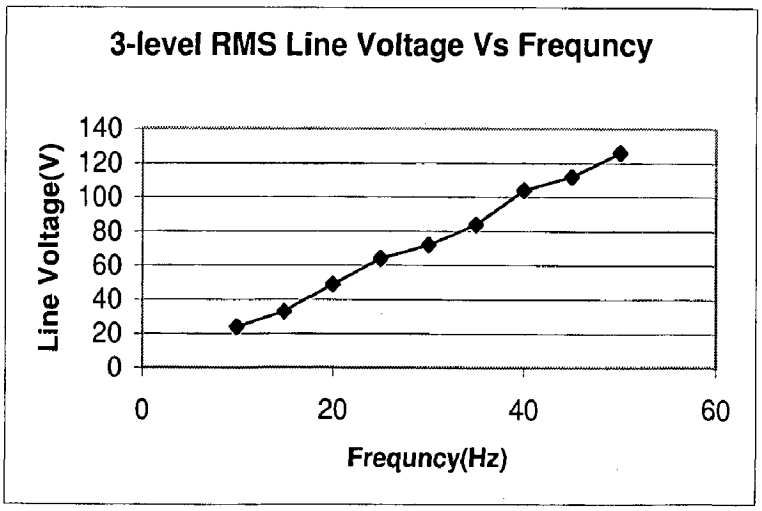


(a)At 50 Hz (THD=5.34) **(b)At 10 Hz(THD=33.45)**

Fig. 8.7 Load Current Harmonic Spectrum

Performance of Induction Motor Drive on V/f basis

Initially Motor is started at minimum frequency, the speed of machine increases gradually by increasing frequency in fixed step. Fig. 8.8 and Fig. 8.9 show the Motor Line current waveforms and Harmonic Spectrums Induction for different frequencies respectively. The following graph shows variation of line-to-line rms voltage applied to the motor as the frequencies increases on constant V/Hz basis.



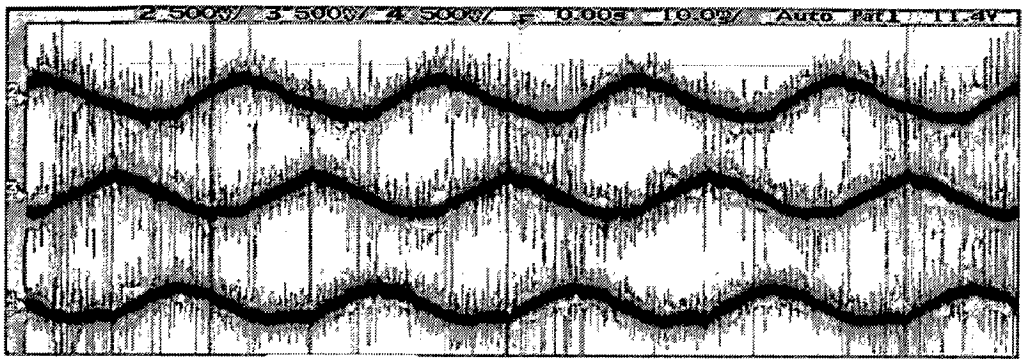


Fig. 8.8(a) Motor Line Currents at frequency 50 Hz (1 A/div, 10ms/div)

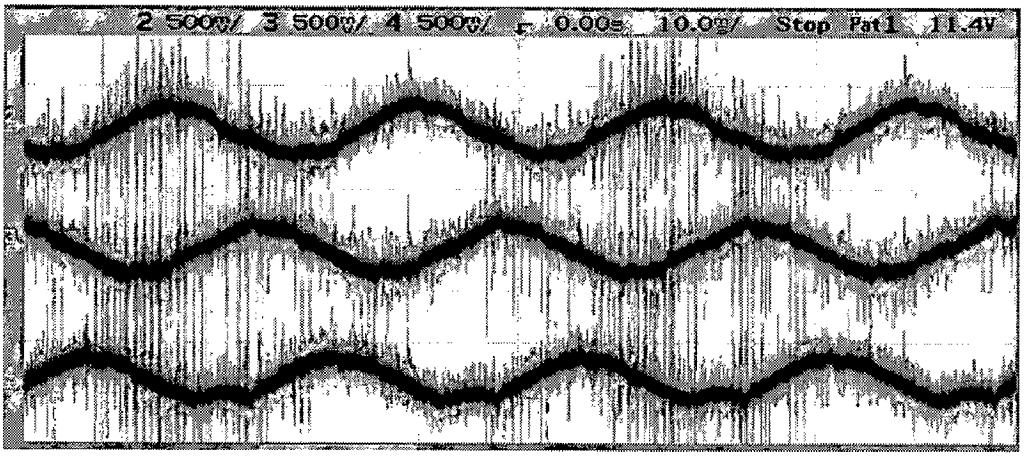
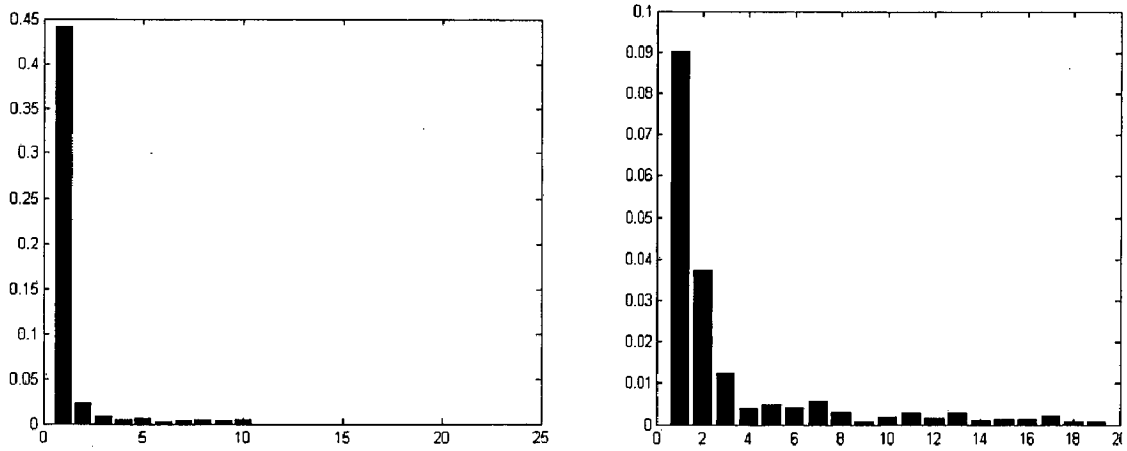
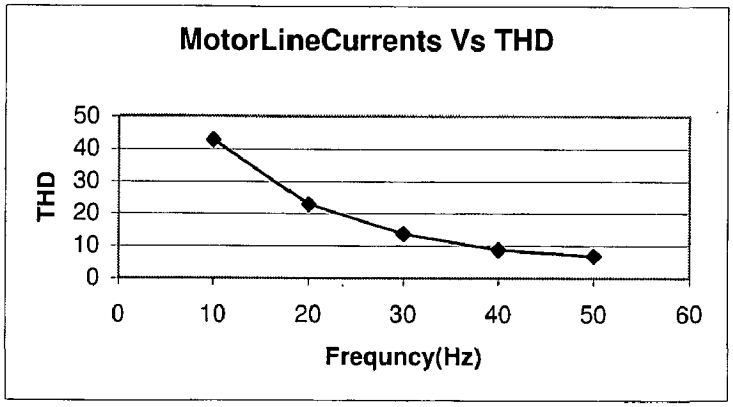


Fig. 8.8(b) Motor Line Currents at frequency 40 Hz (1 A/div, 10ms/div)



(a)At 50 Hz(THD=6.81) (b)At 10Hz (THD=42.73)

Fig. 8.9 Motor Current Harmonic Spectrum



Above figure shows variation of THD as frequency increases. It is shows at higher frequencies THD is less because higher order harmonics are filtered.

8.2. PERFORMANCE INVESTIGATION OF THREE-PHASE TWO-LEVEL INVERTER

Fig. 8.10 shows the firing pulses to the three MOSFETs(S_1,S_3,S5) in same row at different frequencies showing 120^0 phase shift, Fig. 8.11 firing pulses to the two MOSFETs(S_1,S_4) in the same leg which are inverted at different frequencies. Fig. 8.12 and Fig. 8.13 show phase voltage, line voltages respectively different frequencies. Fig. 8.14 and Fig. 8.15 show the Load current waveforms and Harmonic Spectrums for R-L Load for different frequencies respectively.

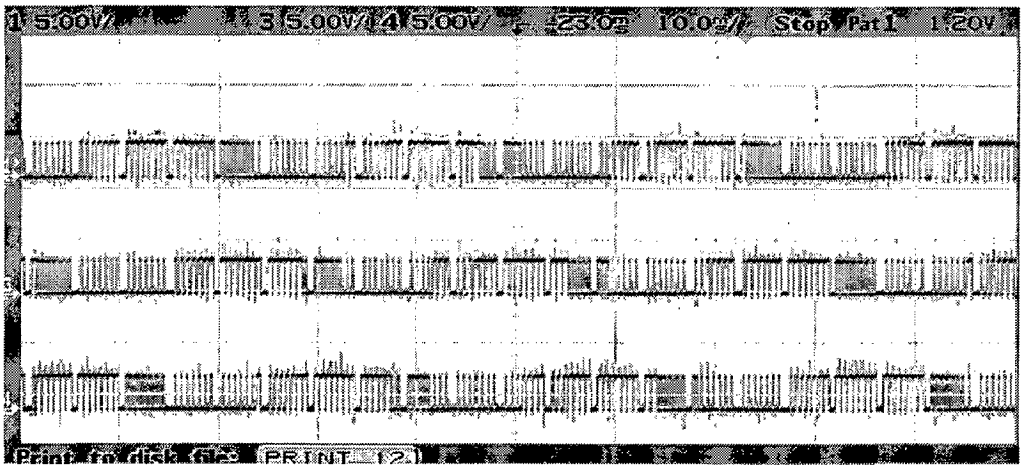


Fig. 8.10(a) Firing pulses to MOSFETs S1, S3, S5 at freq 50 Hz (10ms/div)

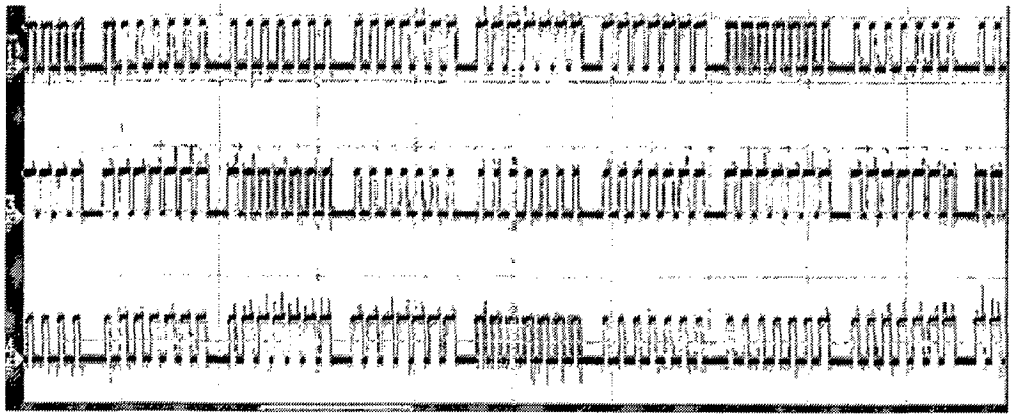


Fig. 8.10(b) Firing pulses to MOSFETs S1, S3, S5 at freq 10 Hz (10ms/div)

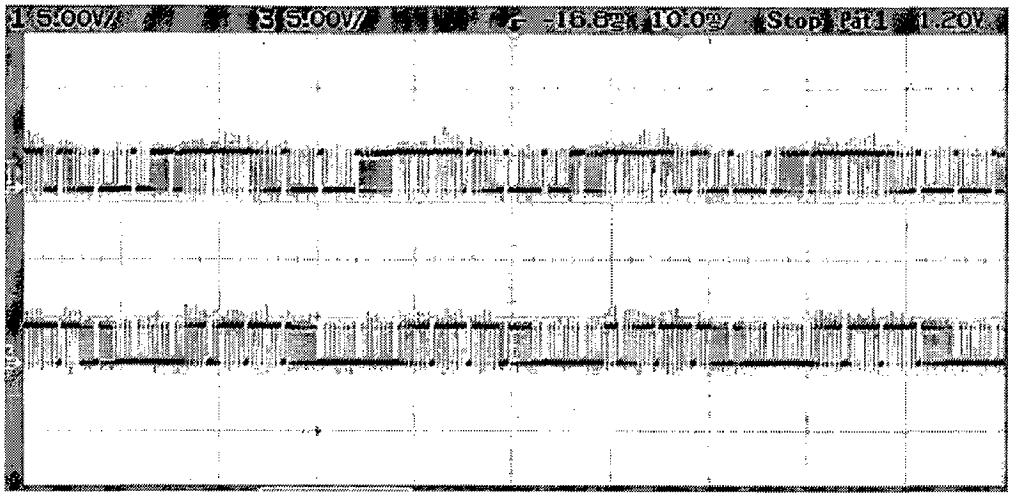


Fig. 8.11(a) Firing pulses to MOSFETs S1, S4 at freq 50 Hz (10ms/div).

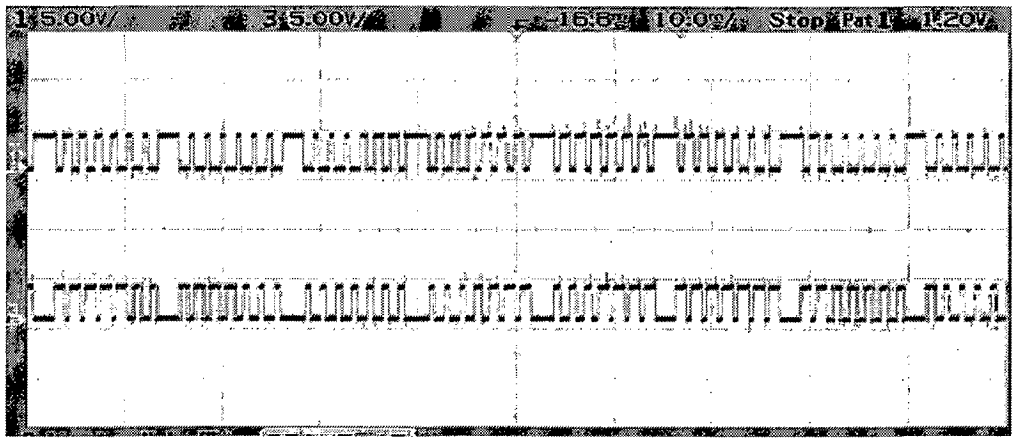


Fig. 8.11(b) Firing pulses to MOSFETs S1, S4 at freq 15 Hz (10ms/div)

Phase Voltages for R-L load at Different Frequencies

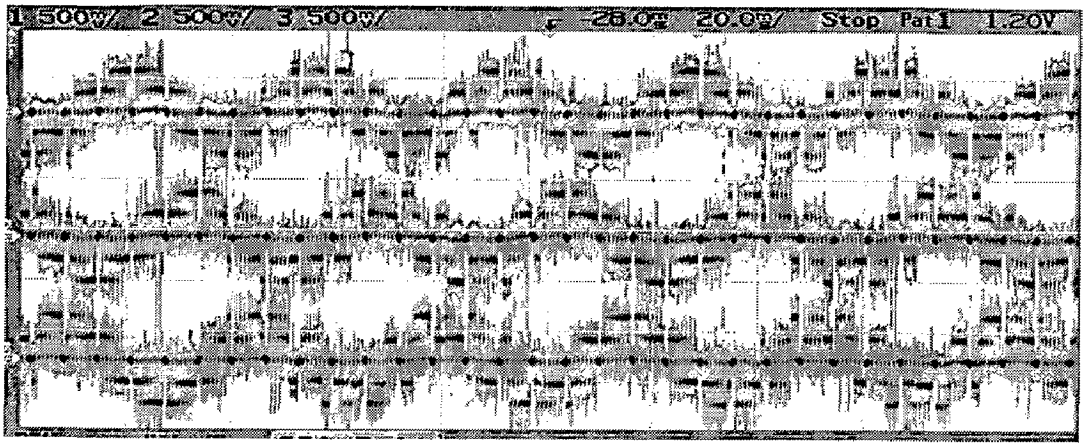


Fig 8.12(a) Phase Voltages at Frequency 30 Hz (90V/div, 20ms/div)

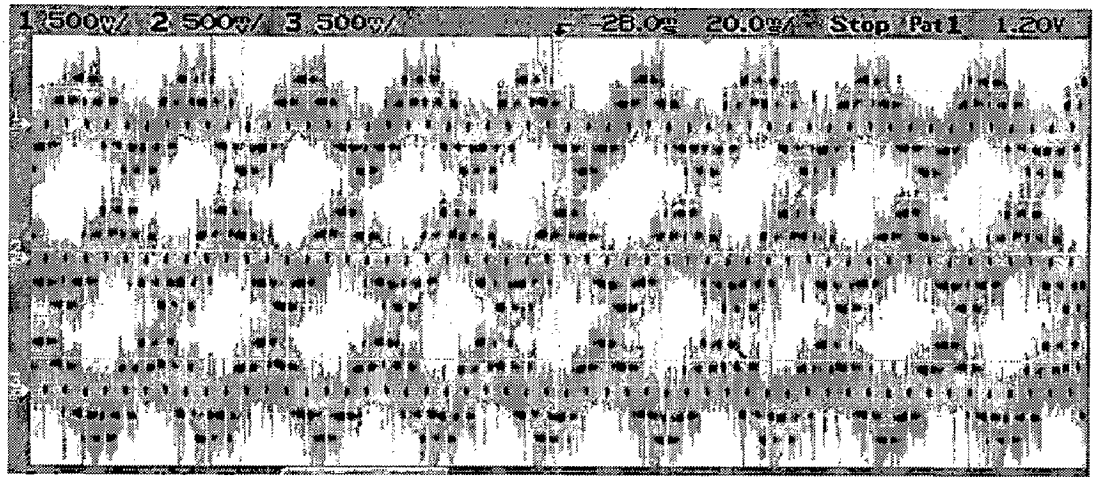


Fig 8.12(b) Phase Voltages at Frequency 50 Hz (90V/div, 20ms/div)

Line Voltages for R-L load at Different Frequencies

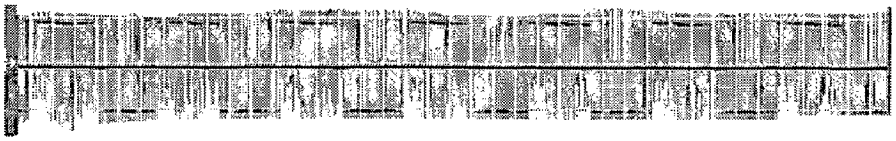


Fig 8.13(a) Line Voltage at Frequency 10 Hz (90V/div, 50ms/div)

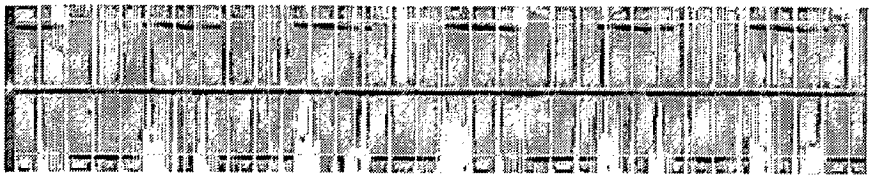


Fig 8.13(b) Line Voltage at Frequency 50 Hz(90V/div, 10ms/div)

Line currents for R-L load at Different Frequencies

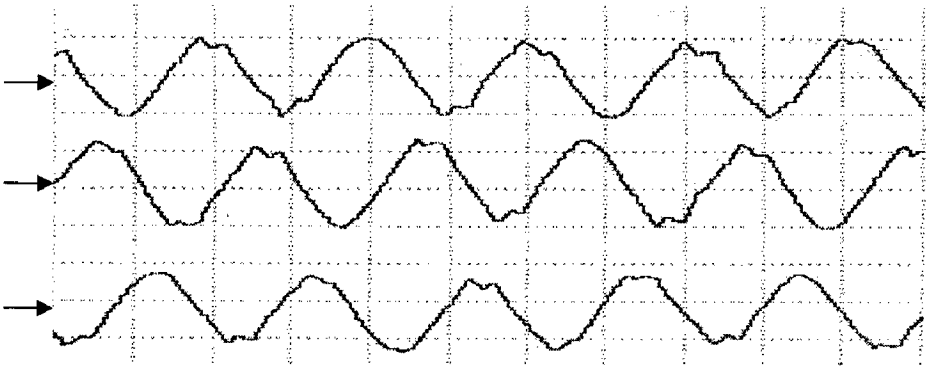


Fig. 8.14(a) Line currents For R-L load at frequency 10 Hz (1 A/div, 50ms/div)

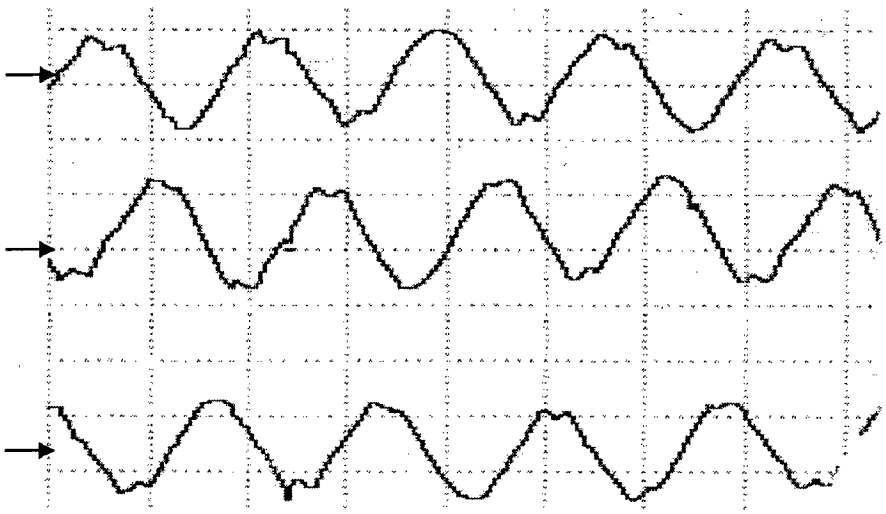


Fig. 8.14(b) Line currents For R-L load at frequency 30 Hz (1 A/div, 50ms/div)

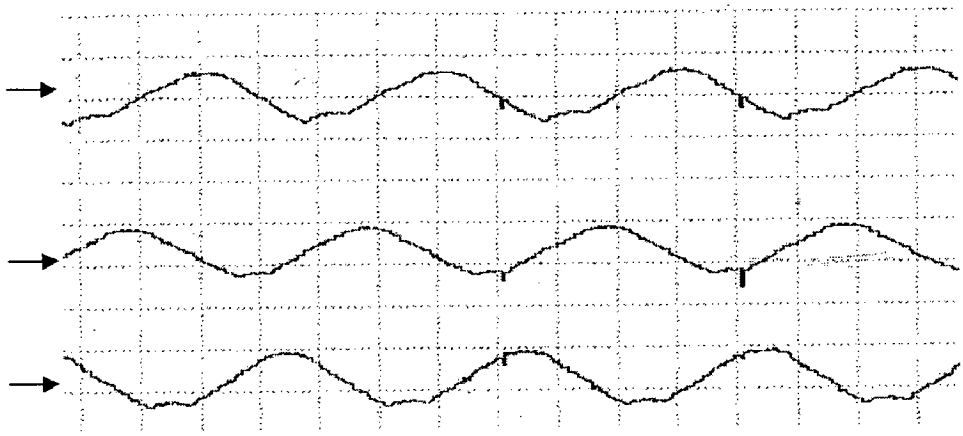
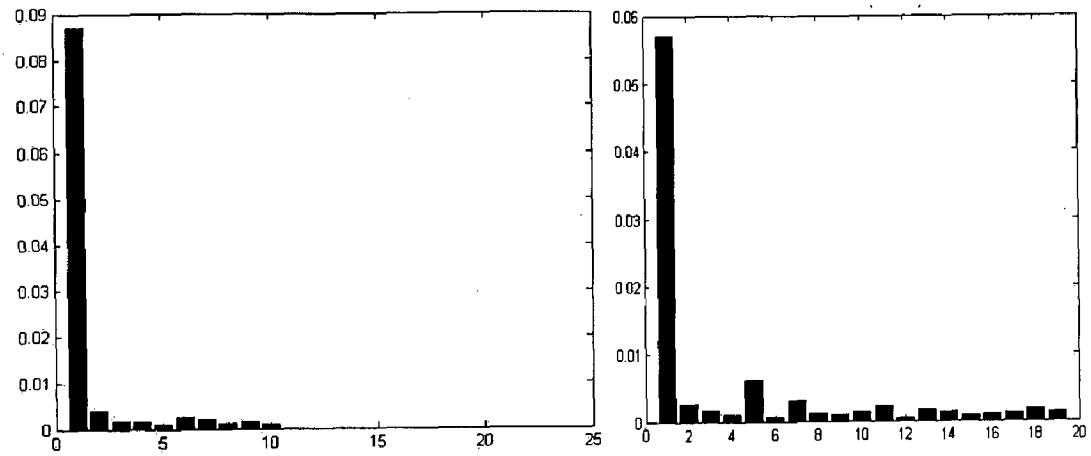


Fig. 8.14(c) Line currents for R-L load at frequency 50 Hz (1 A/div, 50ms/div)

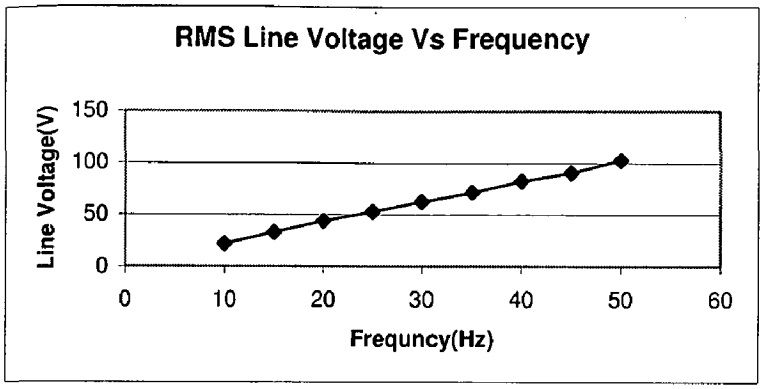


(a)At 50 Hz (6.675) **(b) At 10 Hz (22.019)**

Fig. 8.15 Load Current Harmonic Spectrum

Performance of Induction Motor Drive on V/f basis

Initially Motor is started at minimum frequency, the speed of machine increases gradually by increasing frequency in fixed step. Fig. 8.16 and Fig. 8.17 show the Motor Line current waveforms and Harmonic Spectrums Induction for different frequencies respectively. The following graph shows variation of line-to-line rms voltage applied to the motor as the frequencies increases on constant V/Hz basis.



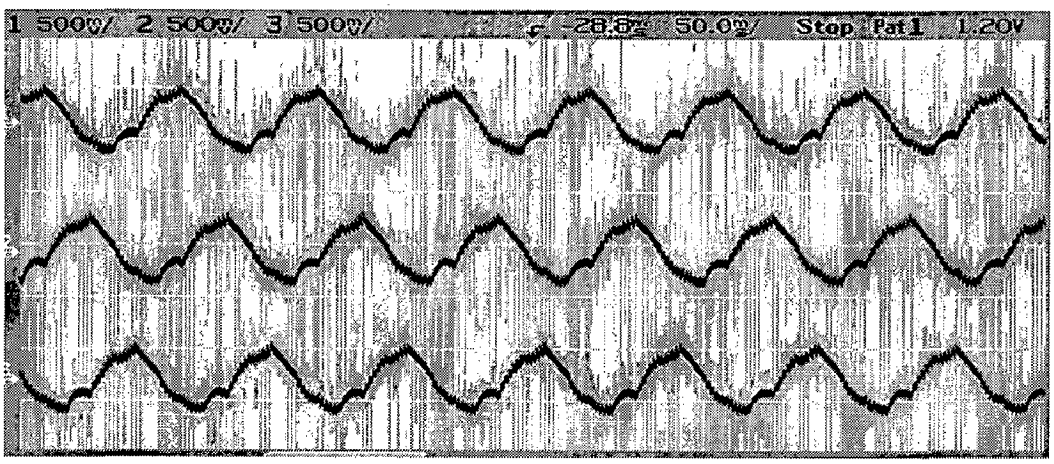


Fig. 8.16(a) Motor Line Currents at 15 Hz(1 A/div, 50ms/div)

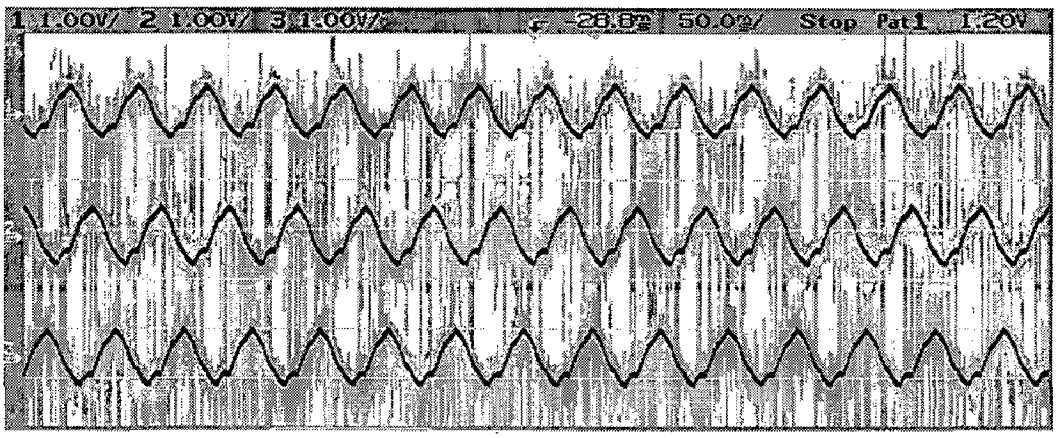


Fig. 8.16(b) Motor Line Currents at 30 Hz (1 A/div, 50ms/div)

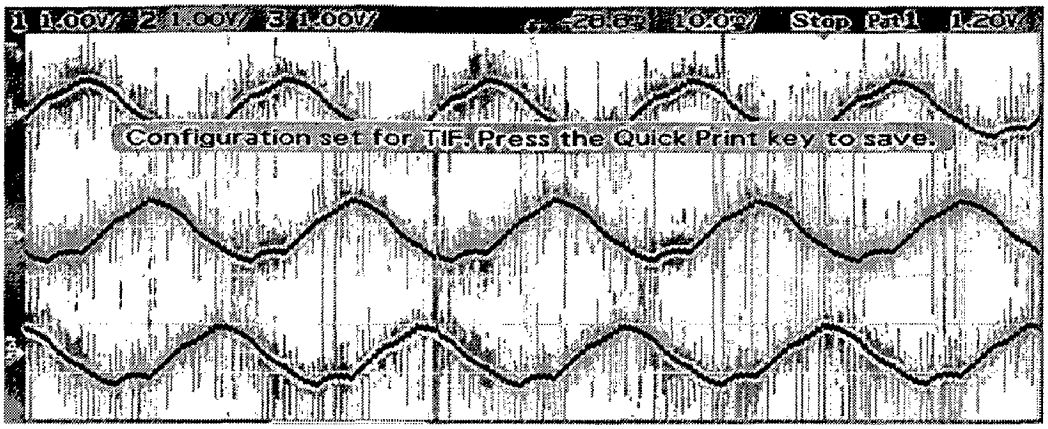
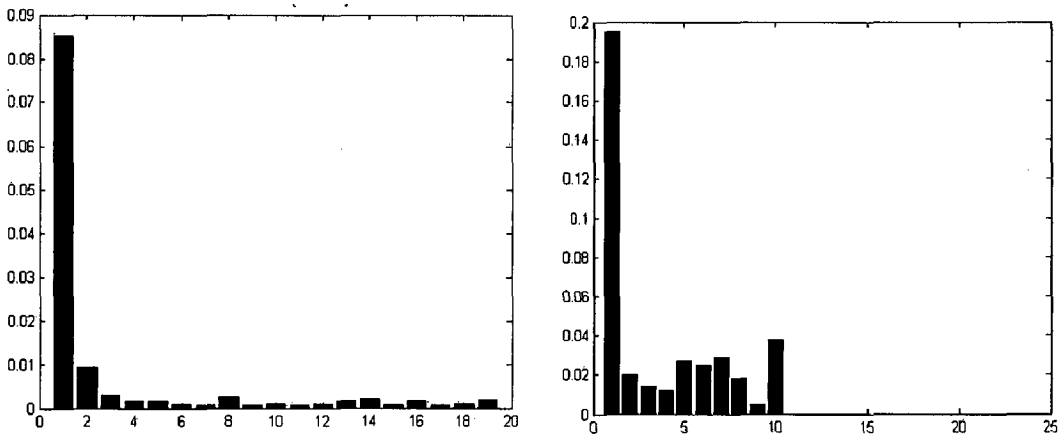
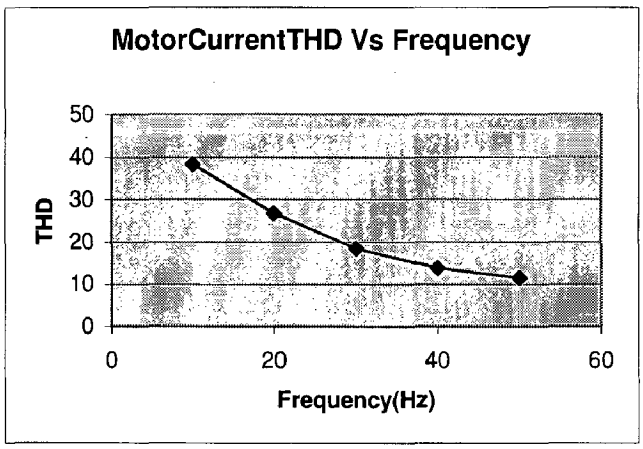


Fig. 8.16(c) Motor Line Currents at 50 Hz (1 A/div, 10ms/div)



(a)At 50 Hz (11.57) **(b) At 15 Hz (35.28)**

Fig. 8.17 Motor Current Harmonic Spectrum



Above figure shows variation of THD as frequency increases for three-phase inverter. It is shows at higher frequencies THD is less because higher order harmonics are filtered.

Fig. 8.18 shows speed encoder output at different frequencies. Fig. 8.19 shows variation of actual speed with reference speed. The small variation between actual and reference speed can be neglected.

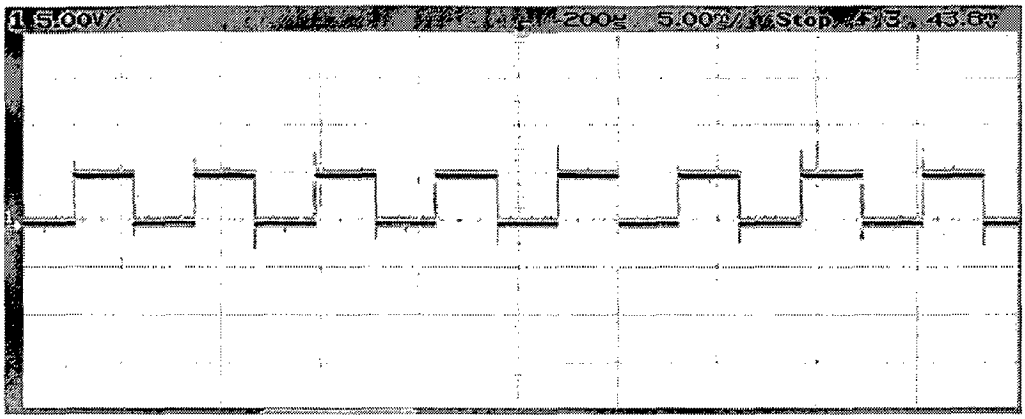


Fig. 8.18(a) Speed Encoder Output at 10 Hz (5 ms/div)

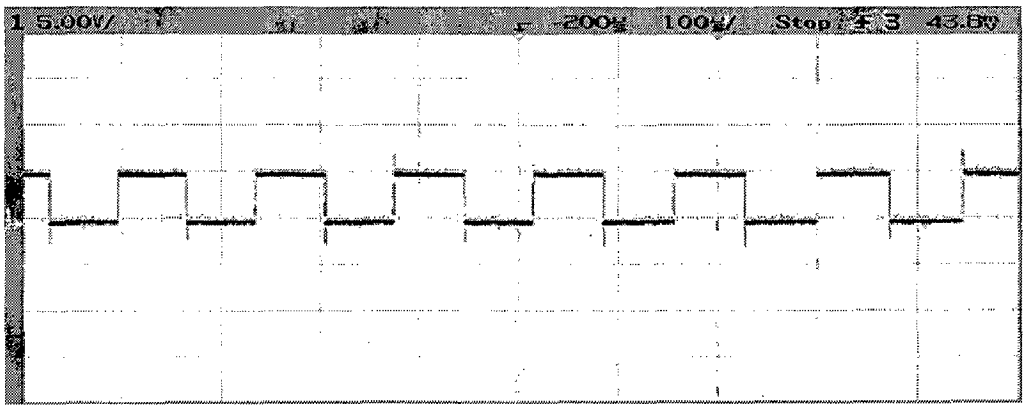


Fig. 8.18(a) Speed Encoder Output at 10 Hz (5 ms/div)

Ref_Spd (rpm)	Act_Spd (rpm)
300	248
600	560
900	860
1200	1164
1500	1454

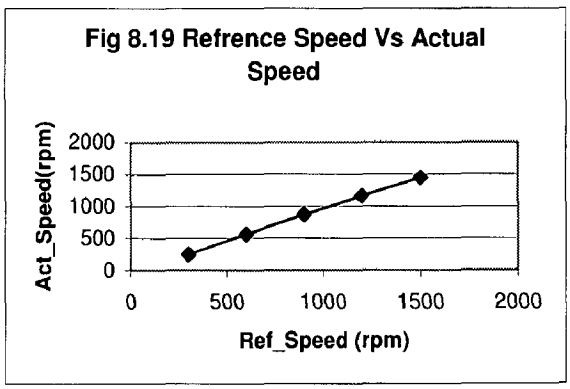


Fig. 8.19 Reference_Speed Vs Actual_Speed

8.3 COMPARISON OF 2-LEVEL AND 3-LEVEL INVERTER

Fig. 8.20 shows the comparison of 2-level and 3-level inverter line-to-line rms voltages as frequency varies on constant. It has been shown in Fig line-to-line voltage for the 3-level inverter is more than 2-level inverter at higher frequencies

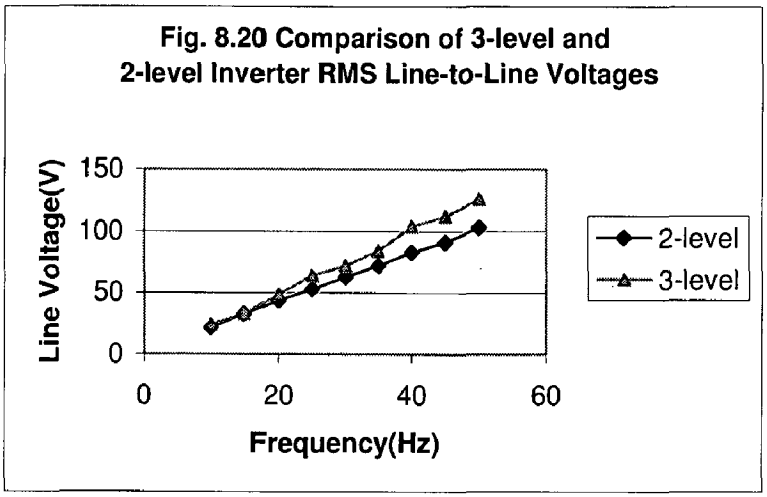
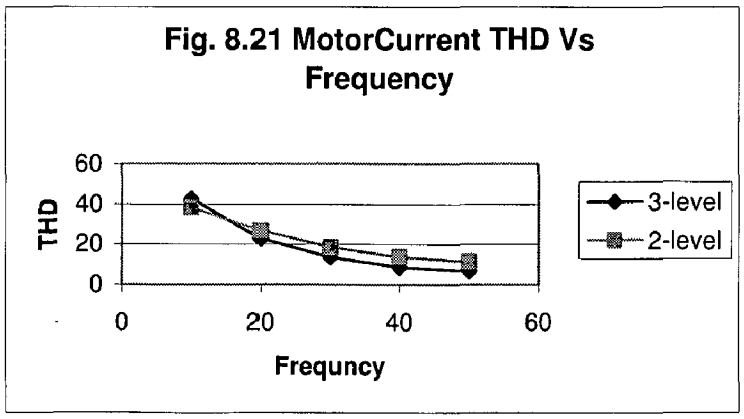


Fig. 8.21 shows the comparison of 2-level and 3-level inverter Motor Line Current THDs as frequency varies on V/f basis. From the figure it is shown that THD curve for Neutral-point Clamped Inverter is below the THD curve for Three-phase Inverter and Motor currents are much more sinusoidal for 3-level inverter for both R-L load and Induction Motor Load.



8.4 PERFORMANCE INVESTIGATION OF FOC OF INCUDCTIOM MOTOR

Fig. 8.22 and Fig. 8.23 shows the motor currents read by ADC after proper scaling, it is observed that offset is completely removed, this is necessary for closed operation of the drive. Fig. 8.24 shows the Clark's transformation (abc $\rightarrow \alpha\beta$) output showing balanced three-phase system when transformed to orthogonal system. Fig. 8.25 shows the motor currents in synchronously rotating reference frame, which are constant in this frame. Fig. 8.26 shows ref_speed Vs act_speed.

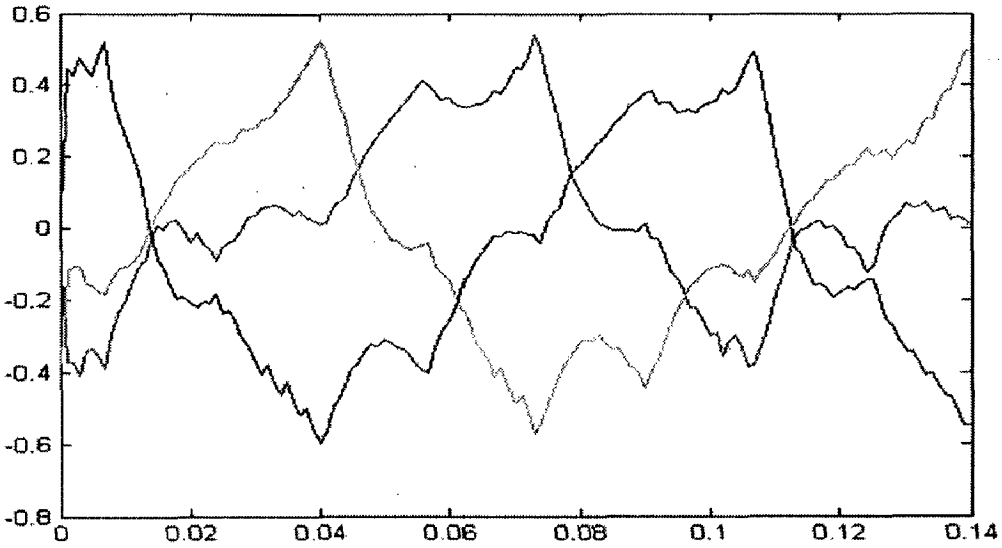


Fig. 8.22 Motor Currents (Ia, Ib, Ic) Read by ADC at 10 Hz

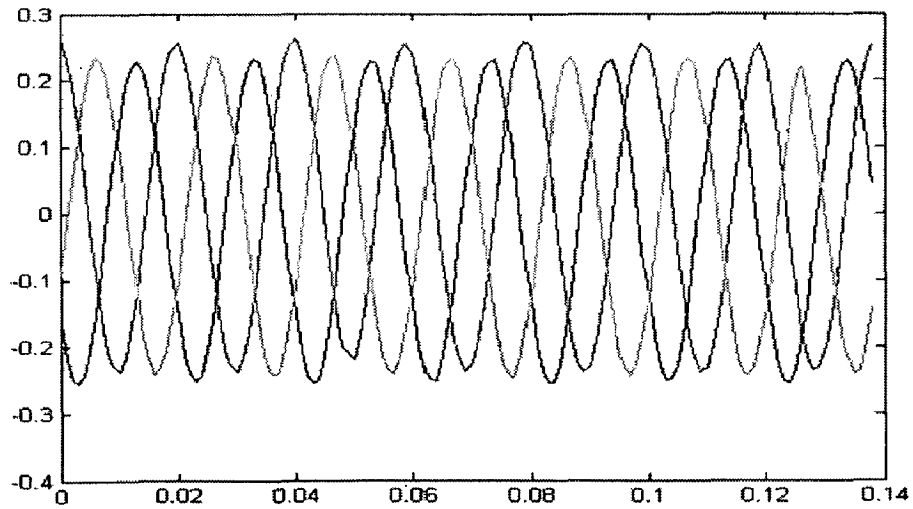


Fig. 8.23 Motor Currents (Ia, Ib, Ic) Read by ADC at 10 Hz

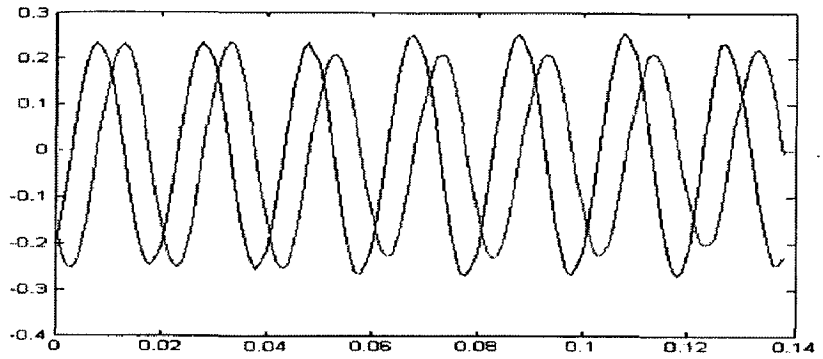


Fig. 8.24 Output of the Clarke Transformation Module ($I_{s\alpha}, I_{s\beta}$)

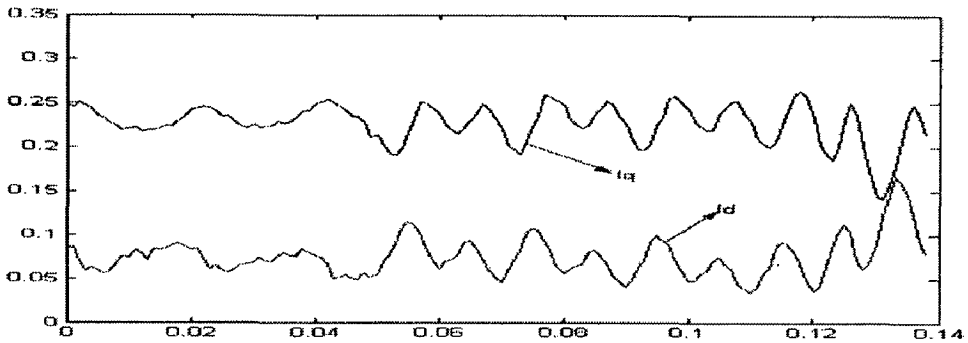


Fig. 8.25 Motor Currents (I_{qs}, I_{ds}) In Synchronously Rotating Reference Frame

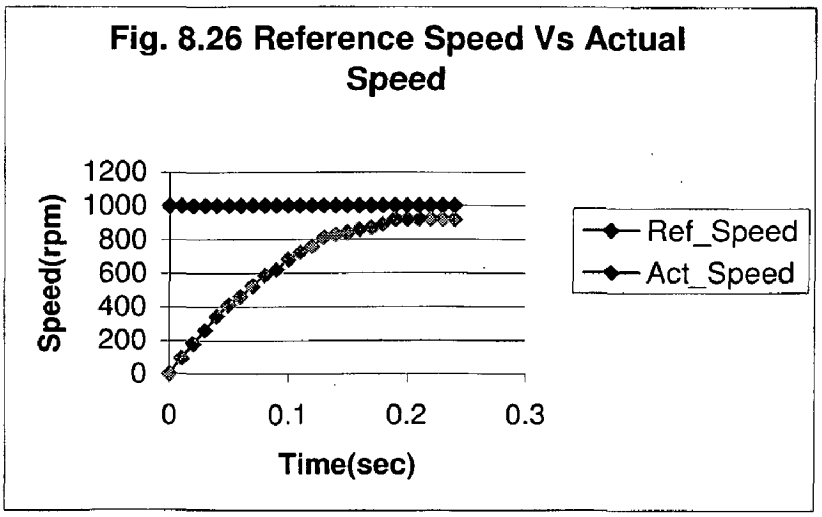
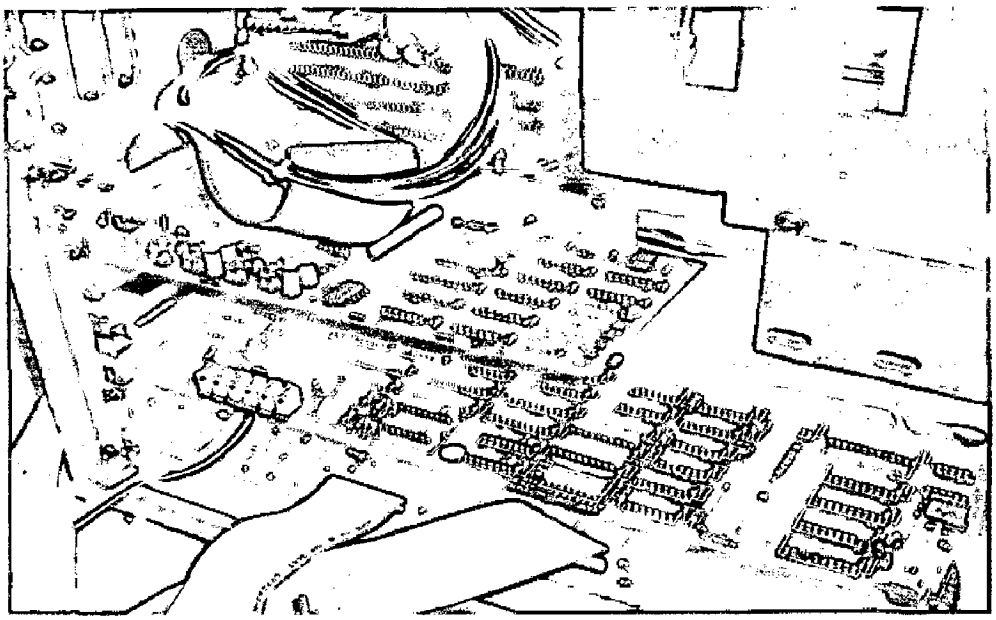
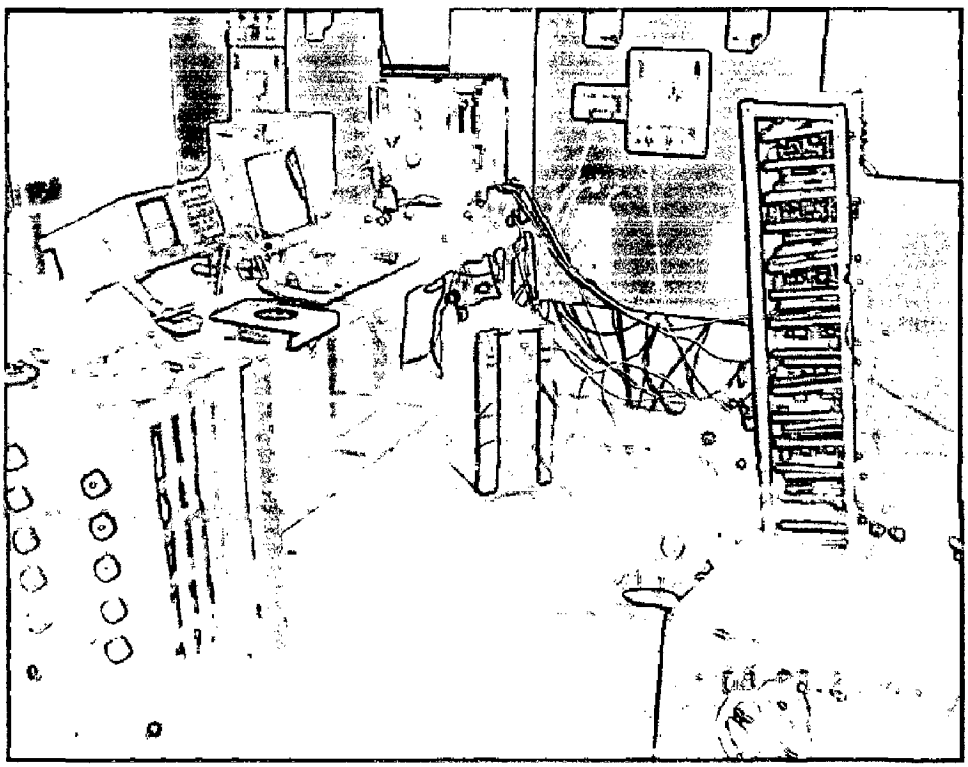


PHOTO GRAPH OF HARDWARE SETUP WITH PC INTERFACING



(A) Processor with A/D card TIMER I/0 card



(B) Complete Assembly With PC Interfacing

CONCLUSION

Multilevel power converters go a long way in overcoming the problems of PWM inverters and this is the reason that they have gained so much attention in recent years. The simulation of the inverters namely conventional three-phase, three-level and five-level was carried using Sinusoidal Pulse Width Modulation (SPWM). It was shown that large decrease in voltage and current THD in moving from three-phase two-level inverter to five-level inverter.

The space-vector PWM (SVPWM) method is an advanced, computation-intensive PWM method and is possibly the best among all the PWM techniques for variable-frequency drive applications. Because of its superior performance, it has been finding widespread application in recent years. This thesis briefly explains theory and digital implementation of Space Vector Pulse Width Modulation (SVPWM) for three-phase two-level and three-level inverter and performance of the both inverters was tested using R-L load. It was shown that load currents for the three-level inverter are much more sinusoidal for all frequencies and improvement in the line current waveform and decrease in the THD from two-level to three-level inverter and relative comparison has been given. Finally performance of the induction motor drive was investigated using open-loop V/Hz control and Field Oriented Control. Motor currents are much more sinusoidal having less THD compared to three-phase two-level inverter and relative comparison has been given.

The complete software has been explained for open-loop control and FOC through flow charts and implemented on 80486 Processor based PC using Timer I/0 and A/D cards. The software is written in '**C-Language**'.

SCOPE FOR FUTURE WORK:

In this thesis, performance of the induction motor using Space Vector PWM was investigated under various operating conditions using 2-level and 3-level inverter. From experimental results it has been shown that as the number of levels increases better performance can be obtained. So same work can be extended to 5-level inverter fed induction motor drive using SVPWM with little modifications.

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APPENDIX

INFORMATION OF DATA ACQUISITION CARDS

The following two cards have been used for this application.

(1) **DYNALOG PCL-812**: The PCL-812 is a high performance, high speed, multi-function data acquisition card for IBM PC/XT/AT and compatible computers. The key features of this card are given below.

- 16 single-ended analog input channels
- An industrial standard 12-bit successive approximation converter (ADC574 or equivalent) to convert analog input. The maximum A/D sampling rate is 30 KHz in DMA mode.
- Switch selectable versatile analog input ranges.
  Bipolar: $\pm 1V, \pm 2V, \pm 5V, \pm 10V$
- Three A/D trigger modes: Software trigger
  Programmable pacer trigger
  External trigger pulse trigger
- The ability to transfer A/D converted data by program control interrupt handler routine or DMA transfer
- An INTEL 8253-5 Programmable Timer/Counter provides pacer output (trigger pulse) at the rate of 0.5 MHz to 35 minutes/pulse to the A/D. The timer time base is 2 MHz. One 16-bit counter channel is reserved for user configurable applications.
- Two 12-bit monolithic multiplying D/A output channels. An output range from 0 to +5v can be created by using the onboard -5V reference
- 16 TTL/DTL compatible digital input, and 16 digital output channel.

(2) **VYNITICS TIMER I/0 CARD:** The key features of this card are shown below.

- 48 programmable Input/Output using two 8255.
- Six channel of 16 Bit Timer/Counter.
- 8 optically isolated Input.
- 8 optically isolated Output.
- Jumper selectable I/0 addressing.
- Hardware clock selection for Timer/Counter.