SIMULATION OF STATIC SYNCHRONOUS SERIES COMPENSATOR USING DIFFERENT INVERTER TOPOLOGIES

A DISSERTATION

Submitted in partial fulfillment of the requirements for the award of the degree of

MASTER OF TECHNOLOGY

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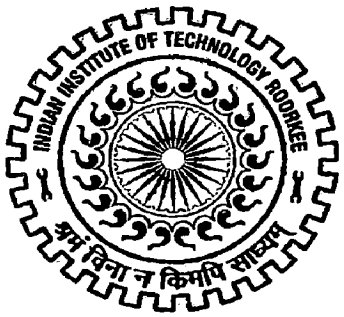
ELECTRICAL ENGINEERING

(With Specialization in System Engineering and Operations Research)

By

SRIKANTH REDDY M



DEPARTMENT OF ELECTRICAL ENGINEERING

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CANDIDATE'S DECLARATION

I hereby declare that the work that is being presented in this dissertation report entitled **"SIMULATION OF STATIC SYNCHRONOUS SERIES COMPENSATOR USING DIFFERENT INVERTER TOPOLOGIES"** submitted in partial fulfillment of the requirements for the award of the degree of **Master Of Technology** with specialization in **System Engineering and Operations Research,** to the **Department Of Electrical Engineering, Indian Institute Of Technology, Roorkee,** is an authentic record of my own work carried out, under the guidance of **Dr. G. N. Pillai,** Assistant Professor, Department of Electrical Engineering.

The matter embodied in this dissertation report has not been submitted by me for the Award of any other degree or diploma.

Date: 28-06-07

Place: Roorkee

M. Srikanth Reddy

(M. Srikanth Reddy)

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

28/6/07

(Dr. G. N. Pillai)
Assistant Professor,
Department of Electrical Engineering,
Indian Institute of Technology,
ROORKEE – 247 667,
INDIA.

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M. Srikanth Reddy

(Srikanth Reddy M)

ABSTRACT

This thesis describes about an active approach to the series line compensation, in which a synchronous voltage source implemented by a gate-turn-off thyristor (GTO) based voltage-sourced inverter, is used to provide controllable series compensation. This compensator called *static synchronous series compensator* (SSSC) can provide controllable compensating voltage. It is immune to classical resonance.

In this thesis, *static synchronous series compensator* (SSSC), for the control of active power flow on a transmission line is proposed and its effective ness is investigated through multi-pulse and multi-level inverters. The SSSC is based on injecting a voltage in given line to counter the voltage drop produced by the inductive reactance of the line. The resulting compensator therefore emulates the control of transmission line reactance and thus it assist in controlling the power transmission capability. The three-phase output voltage of the multi-pulse and multi-level inverter is synchronized to the line frequency and its phase is arranged in quadrature with the line current.

Multi-pulse (12-pulse and 48-pulse) inverters are designed by using different transformer connections. The output voltage of the 48-pulse inverter is sinusoidal and contains fewer harmonics. The SSSC is simulated by using Multi-pulse (12-pulse and 48 –pulse) inverters.

Multi-level voltage source inverters are emerging as a new breed power converter option for high-power applications. The multi-level voltage source converters typically synthesize the staircase voltage waveform with several levels of dc capacitor voltage. In this thesis, the SSSC is simulated by using Diode-clamped multilevel inverter.

The proposed Multi-pulse (12-pulse and 48 pulse) and Multilevel (Diode-clamped) SSSC is simulated by using PSCAD/EMTDC software to validate its working and testing. It is effective to dynamically control active power change in the transmission line.

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CHAPTER 1
INTRODUCTION

With the industrial growth of a nation, there is always an increased consumption of energy, particularly electrical energy. This leads to an increase in the generation and transmission facilities. In developed nations, the demand of electrical energy doubles every ten years. In developing countries, like India, this demand doubles every seven years, which requires considerable investment in the electric power sector [1].

The power supply systems are widely interconnected. This is done for economic reasons, to reduce the cost of electricity and to improve reliability of power supply and to minimize the total power generation capacity and fuel cost. It can be divided into three subsystems: generation, transmission and distribution subsystems. Until recently, all three subsystems were under supervision of one body within certain geographical area providing power at regulated rates. In order to provide cheaper electricity the deregulation of power system, which will produce separate generation, transmission and distribution companies, is already being performed [2]. At the same time, electric power demand continues to grow and building of the new generating units and transmission circuits is becoming more difficult because of economic and environmental reasons. Therefore, power utilities are forced to relay on utilization of existing generating units and to load existing transmission lines close to their thermal limits. However, stability has to be maintained at all times. Hence, in order to operate power system effectively, without reduction in the system security and quality of supply, even in the case of contingency conditions such as loss of transmission lines and/or generating units, which occur frequently, and will most probably occur at a higher frequency under deregulation, a new control strategies need to be implemented.

The power system of today, largely, is mechanically controlled. There is a widespread use of microelectronics, computers and high-speed communications for control and protection of present transmission systems. The problem with the mechanical devices is that control cannot be initiated frequently, from the point of view of both dynamic and steady state operation, the system is uncontrolled.

In the late 1980's the Electric Power Research Institute (EPRI) has introduced a new technology program known as Flexible AC Transmission System (FATCS) [1-2]. The main idea behind this program is to increase controllability and optimize the utilization of the existing power system capacities by replacing mechanical controllers by reliable and high-speed power electronic devices.

1.1 Facts in Power System:

As noted in the introduction, transmission systems is being pushed closer to their stability and thermal limits while the focus on the quality of power delivered is greater than ever. The limitations of the transmission system can take many forms, may involve power transfer between areas within a single area or region, and may include one or more of the following characteristics:

1. Steady-State Power Transfer Limit
2. Voltage Stability Limit
3. Dynamic Voltage Limit
4. Transient Stability Limit
5. Power System Oscillation Damping Limit
6. Inadvertent loop flow Limit.
7. Thermal limit
8. Short-Circuit Current Limit.

FACTS technology refers to devices that enable flexible electrical power system operation, i.e. controlled active & reactive power flow redirection in transmission paths by controlling different parameters in the transmission system.

It opens up new opportunities for controlling and enhancing the useable capacity of present, as well as new upgraded lines. The possibility that current through a line can be controlled at a reasonable cost enables a large potential of increasing the capacity of existing lines thereby enabling them to carry power closer to their thermal ratings.

Because of their fast response, FACTS Controllers can also improve the stability of an electrical power system by helping critically disturbed generators to give

away the excess energy gained through the acceleration during fault [2]. This can be done by correctly changing the pattern of power flow.

1.2 Power Flow over a Transmission Line:

In Fig.1.1 a simple two-machine power system is shown in which two buses are connected by a reactance. The power flow over the transmission line is given by the following approximate formula

$$P = \frac{|V_1||V_2|}{X}\sin(\delta_1 - \delta_2) \tag{1.1}$$

Where

P is line power flow,

$V_1 = |V_1|\angle\delta_1$ And $V_2 = |V_2|\angle\delta_2$ are the voltages at the two ends,

X is the transmission line reactance.

The power angle diagram is shown in Fig. 1.1 where $P_{max} = |V_1||V_2|/X$ .From equation (1.1) it is evident that the power level can be enhanced by either increasing the angle difference $(\delta_1 - \delta_2)$ between the two buses or by increasing the voltage magnitudes at the two ends. The angle difference is usually restricted to below $30°/35°$ from transient stability considerations, i.e., from the consideration of the ability of the system to recover following a severe fault. On the other hand, the voltage magnitudes cannot be increased arbitrarily as they are stipulated to be within $\pm 5\%$ of the nominal voltage.

An alternative approach to enhance the power flow is to decrease the transmission line reactance by constructing a parallel transmission line. This however is an expensive proposition and may not be economically feasible always. Hence, it is crucial to design and develop alternative means of increasing the power transfer capability over a given corridor.

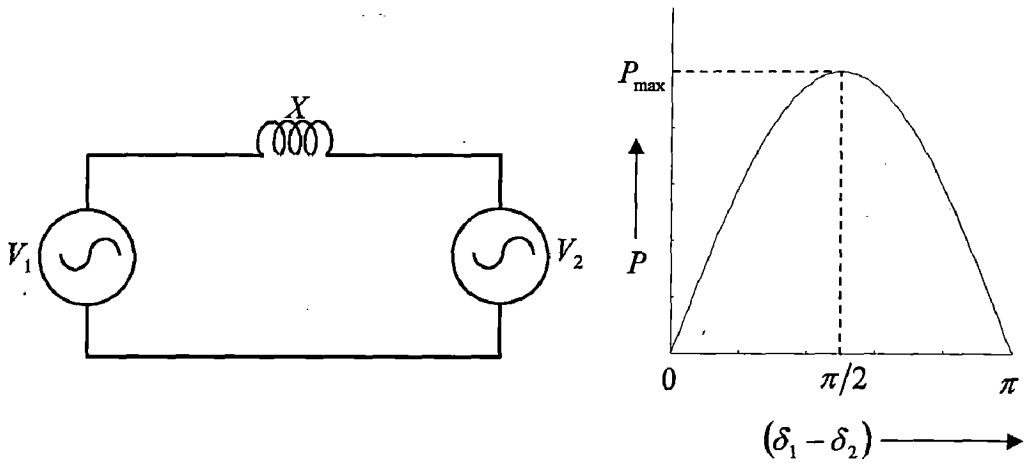

Fig. 1.1 Schematic diagram of a simple two-machine system and the power versus load angle characteristics

1.3 Solution to power transmission problem:

The major issues that are involved in the power transmission are to enhance the power transfer capability and flexible control over power flow. Even though some of these problems have been addressed in the past through electro-mechanical equipments, the current trend is to use solid state devices for faster control, reliable operation and to reduce size. One of the major drawbacks which the utility planners and management face is the cost of the power electronic devices. However, where the problem with bulk power transmission is very severe, installations of these devices are increasingly becoming more appealing. Preliminary studies show that in many occasions the initial installation cost of such a device is paid back by the savings and benefits incurred within a few months.

The powerelectronic devices, which are applied to power systems, are categorized under the generic name of flexible ac transmission systems (FACTS) [3]. Two of the main objectives of FACTS are:

1. To increase the power transfer capability of transmission network and
2. To provide direct control of power flow over designated transmission routes.

There are three major facets of FACTS devices.

3. Shunt compensation.
4. Phase angle regulation.
5. Series compensation.

These are briefly discussed in the below section.

1.3.1 Shunt Compensation:

Shunt compensators are used to provide reactive power compensation to control voltage at desired buses. Consider Fig. 1.2 in which the system of Fig. 1.1 is compensated by a shunt voltage source at the middle of the transmission line.

Let the mid-point voltage be $V_m = V\angle(\delta)$ where $\delta = (\delta_1 - \delta_2)/2$. Also, without any loss of generality, let us assume that $V = |V_1| = |V_2|$. The power transfer over the line is then given by

$$P = \frac{2V^2}{X}\sin\left(\frac{\delta}{2}\right) \tag{1.2}$$

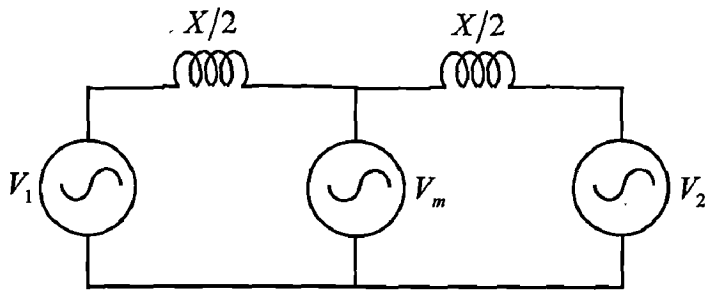

Fig. 1.2 Principle of shunt compensation

It is obvious from the above equation (1.2) that the power capability P_{max} has doubled the Steady state stability limit has been increased to 180-degrees.Shunt compensator devices have long been used in power system. Most such installations around the world use static var compensators (SVC) which require large inductors and capacitors. However, from the point of view of the size and cost associated with these passive devices, the current thinking tends towards all power electronic devices as the cost of power electronic switches are rapidly reducing. The offshoot of this thinking is

the static compensator (STATCOM) which consists of a voltage source inverter (VSI) that is supplied by a dc storage capacitor. Usually this VSI is tied in shunt to the mid-point of a transmission line via an interface transformer. The three-phase output waveforms of the VSI are in phase with that of the respective phases of the mid-point potential of the transmission line. Since these two voltage sources are tied to each other by the leakage inductance of the interface transformer, reactive power between the STATCOM and the mid-point bus can be exchanged depending upon the magnitude of the STATCOM voltage that of the mid-point voltage.

1.3.2 Phase Angle Regulation:

It is evident from equation (1.1) that if the angle difference $(\delta_1 - \delta_2)$ between the two buses in Fig. 1.1 can be increased, the system stability margin can be increased. Hence more amount of power can be transferred with lesser risk of angle instability. The improved power angle characteristics using a shunt compensator or a phase angle regulator is graphically depicted in Fig. 1.3.

Not much work has been reported in the area of thyristor controlled phase angle regulator (TCPAR).

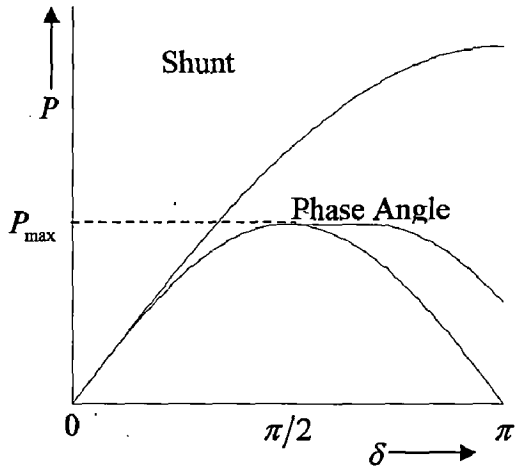

Fig. 1.3 Improvement in power transfer using shunt compensation and phase angle regulation

1.3.3 Series Compensation:

Series compensators, which are connected in series with the transmission line, are used for active power flow control over a transmission line. This can be achieved either by varying (mainly reducing) the reactance of the line or by injecting a series voltage in the line. These two aspects are TCSC and SSSC and are discussed in detail in the next section.

1.4 Series Compensation of Transmission line:

Most of the series compensators that are currently installed either employed a fixed capacitor or use a device called thyristor controlled series capacitor (TCSC).This device includes a fixed capacitor which is connected in parallel with a thyristor switched reactor (TCR). In a TCR a reactor is connected in series with a pair of oppositely poled thyristors.It can be shown that by varying the firing angle of the oppositely poled thyristors, the fundamental frequency reactance of the TCR can be varied. Thus, the TCSC behaves almost like a capacitor that is connected in parallel with a variable reactor. The fundamental frequency impedance of a TCSC is such that it can be varied from inductive to capacitive mode.

The TCSC has certain drawbacks. Deriving a closed-loop model of this is complicated, even though a lot of research has been done in this area. Also, the per MVA cost of such a device is high [4]. Moreover, this device is susceptible to parallel resonance due to the presence of inductors and capacitors, which may lead to a building up of excessive high voltage across the capacitor.

A solid-state alternative of the TCSC is currently been investigated which does not suffer from any of the problems mentioned above. This device is called a solid-state series compensator or static synchronous series compensator (SSSC or S^3C). It employs a VSI that is supplied by a dc storage capacitor. The output of the VSI is connected in series with the transmission line through an interfacing transformer.

The equivalent schematic diagram of a SSSC compensated power system is shown in Fig. 1.4 in which the voltage V_q is injected by the VSI through the interfacing transformer. If the magnitude of the injected voltage is made proportional to that of the

line current, a series compensation equivalent to that provided by a TCSC can be obtained. To explain this, let us define this voltage as

$$V_{a'} = kI_L e^{-j90^\circ} \tag{1.3}$$

Where I_L the line current and k is proportionality constant. The above equation signifies that the voltage that needs to be injected by the S^3C must be in quadrature (lagging) with the line current. The power transfer relation is then given by

$$P = \frac{V^2}{X-k}\sin\delta \tag{1.4}$$

Thus varying the magnitude of the injected voltage the power flow over the transmission line can be controlled in the same manner as a TCSC.

We can also make the injected voltage independent of the line current. In this case however, the characteristic of the S^3C will differ from that of a TCSC. Let the injected voltage, which is still in quadrature with the line current, be redefined as

$$V_{a'} = k\angle\left(I_L \mp 90^\circ\right) \tag{1.5}$$

Where the phase shift of $\mp 90^\circ$ from the line current indicates that this device can be operated either in capacitive or in inductive modes. The power transfer relation for this condition is then given by

$$P = \frac{V^2}{X}\sin\delta + \frac{V}{X}k\cos\left(\frac{\delta}{2}\right) \tag{1.6}$$

The power-angle characteristics for the two above-mentioned cases are given in Fig. 1.5

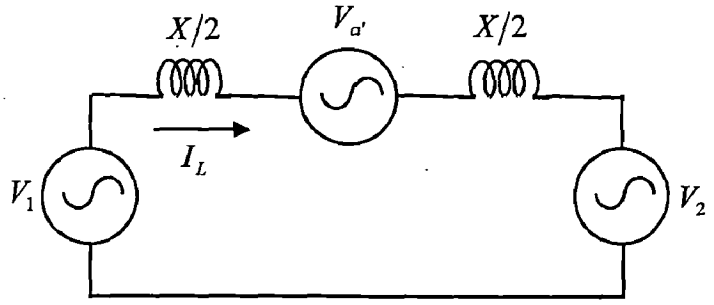

Fig. 1.4 Equivalent circuit of a SSSC compensated power system

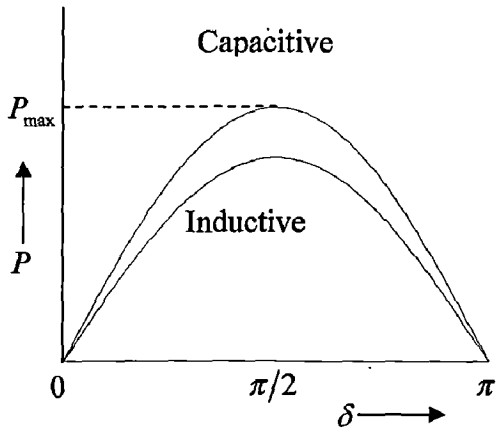

Fig. 1.5 Power angle diagram of a SSSC

1.4.1 Sub synchronous Resonance:

This phenomenon can only be seen in a series compensated power system. Subsynchronous resonance refers to the condition where the subsynchronous complement of the natural frequency of a series capacitor compensated armature circuit is close to the natural frequency of shaft torsional modes. In a system that exhibits this phenomenon severe damage can occur to the generator shaft. Moreover, these torsional modes can interact with the control systems of a series compensated power system which employs a TCSC or an S^3C. Therefore, a systematic study of this phenomenon is necessary [5].

1.5 The Synchronous Voltage Source:

The synchronous voltage source can produce a set of (three) alternating voltage at the desired fundamental frequency with controllable amplitude and phase angle. Generate, or absorb, reactive power when tied to an electrical power system to function like a synchronous condenser (compensator); and convert the active power it exchanges with the ac system into the form(e.g., dc) that is compatible with an electric energy source or storage. Various, static switching power converters can implement the SVS for power transmission applications, using semiconductor-switching devices of suitable rating and characteristics.

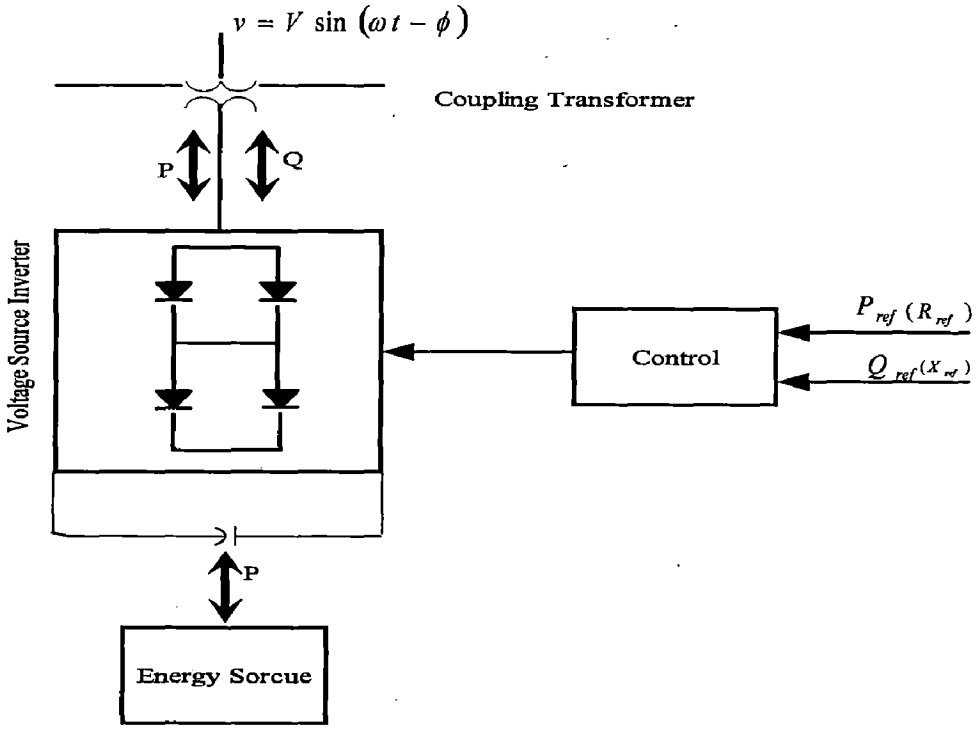

Fig. 1.6 Synchronous voltage source employing a solid-state Voltage-sourced inverter.

The SVS is simply an array of static, solid-state switches operated from a dc voltage source by an electronic control so as to produce a three-phase set of synchronous, nearly-sinusoidal output voltages with independently controllable amplitude V and phase angle ϕ.The amplitude and angle control implies the capability of the SVS to exchange active and reactive power at its ac output terminals. The SVS can be considered functionally as an ideal generator that can be operated with a relatively small dc storage capacitor in self-sufficient manner to exchange reactive power with the ac system or, with external dc power supply or energy storage, to also exchange independently controllable active power. A functional representation of SVS is shown in Fig.1.6 References P_{ref}, Q_{ref}(or other related parameters, such as the desired compensating reactive impedance $X_{ref,}$ and resistance R_{ref}) definer the amplitude V and phase angle ϕ of the generated output voltage necessary to exchange the desired reactive and active power at the ac output[6]. If the SVS is operated strictly for reactive power exchange, P_{ref}(or R_{ref}) is set to zero.

1.6 Thesis Objective:

The scope of the thesis is to examine the use of static synchronous series compensator (sssc) in an electrical power transmission line for real power control. The sssc is simulated by using different inverter topologies.

- The application of multipulse inverters (twelve pulse and forty eight-pulse) to realize Static synchronous series compensator is investigated.
- A real power flow controller is developed for multipulse inverter and a controller is adapted for the sssc.
- The application of multilevel inverter (diode-clamped multilevel invereter) to realize sssc is investigated.
- A controller for the injection of line voltage in quadrature with the line current is developed.
- The power flow control in the transmission line, maintenance of d.c voltage constant across the capacitors of the inverters and injected voltage is in quadrature with the line current are investigated in the simulation.

1.7 Outline of the thesis:

The rest of the thesis is organized as follows. The design of a synchronous voltage source is done with different conFigurations in Chapter 2, the synchronous voltage source is designed as a multipulse inverter. In this chapter the design of 12-pulse and 48-pulse inverter are explained and the corresponding output voltages and harmonic spectrums are presented.

In chapter 3, the test system and the control technique for the injecting the quadrature voltage are explained. The simulation of the test system by connecting 12-pulse and 48-pulse inverter is done by using the PSCAD 4.2.1 software and the results are presented.

In Chapter 4, the synchronous voltage source is designed by using the multilevel inverter technique (diode-clamped Multi level inverter).The simulation studies by using the diodeclaped inverter are presented in chapter 4. Chapter 5 concludes the thesis by comparison of these different inverter topologies, conclusions and future scope of the work.

CHAPTER 2
MULTI-PULSE INVERTER

2.1 Basic Theory of Multi-pulse inverter:

The advances in the switching power converter technology has made the generation of controllable reactive power possible to provide shunt and series reactive compensation for transmission and distribution lines. Usually dc to ac inverters is used for reactive compensation. These inverters are supplied from dc storage capacitors. Unfortunately these power converters generate harmonic voltages and currents on both ac and dc sides. These harmonics lead to problems like the heating of capacitors, telephone interference, controller instability etc. It is to be noted that the above problems are not only restricted to local (i.e., at the source of harmonics) but are global as the harmonics propagate over long distances.

The harmonic output of the converters can be decreased by either increasing the pulse number of the inverter or installing the filters. The installation of filters has found to be more economical as they serve a dual purpose filtering as well as reactive power generation. However, filters have certain disadvantages when we consider an all-electronic device. Some of these disadvantages are:

1. Dynamic over Voltages (DOV) problem.
2. Bulkiness of the filters.
3. Complex design of filters.
4. Introduction of delay in control loop.

Thus in certain systems where controllable series or shunt compensation is required, increased pulse numbers are preferred.

2.2 Configuration of six-pulse inverter:

A typical 6-step inverter is shown in Fig. 2.1. The inverter produces a set of three quasi-square voltage waveforms of a given frequency by connecting the dc voltage sequentially to the three output terminals via appropriate inverter switches (GTO's). The GTO's are denoted by S_1 to S_6 and are fired in the same sequence. An anti-parallel diode is connected across each GTO to maintain the continuity of current.

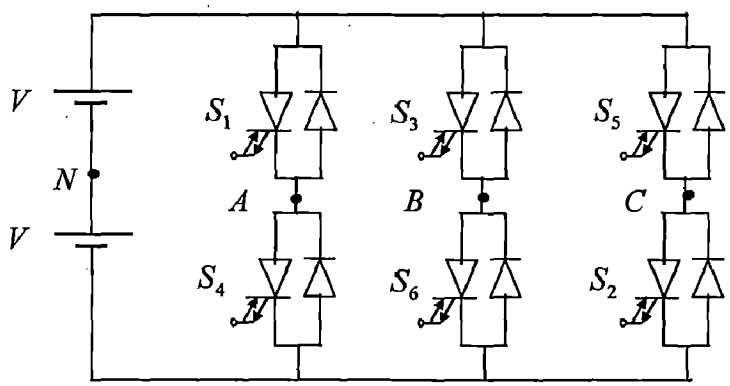

Fig. 2.1 Basic Configuration of a 6-step inverter

The output voltage waveforms, when each switch is conducting for a period of 180° are shown in Fig. 2.2. The Fourier series of the voltage waveforms are given by

$$f_A(t) = \sum_{n=1,3,5,\ldots} \frac{4V}{n\pi} \sin(n\omega t) \tag{2.1}$$

$$f_B(t) = \sum_{n=1,3,5,\ldots} \frac{4V}{n\pi} \sin(n\omega t - 2n\pi/3) \tag{2.2}$$

$$f_C(t) = \sum_{n=1,3,5,\ldots} \frac{4V}{n\pi} \sin(n\omega t + 2n\pi/3) \tag{2.3}$$

Where $\omega (= 2\pi f)$ is the fundamental frequency. From the above three equations it is clear that there are no even harmonics on the ac side. It can also be seen that for a particular value of n the three functions either are in phase, or appear in the sequence *A-B-C* or in the sequence *A-C-B*. Let us denote them as zero-sequence, positive-sequence and negative-sequence respectively. It is to be noted that these sequences are not the symmetrical component sequences used for the representation of unbalanced circuits. The sequences for the various values of n are given in Table 2.1. From this table it is evident that the triplen harmonics (3, 9, 15,...) are zero sequence and thus can circulate in the Δ-connected primary windings of the transformer connected to the inverter and therefore do not appear in the transformer secondary waveform. Alternatively, if the transformer primary is connected in ungrounded *y*, these zero sequence components are forced to zero

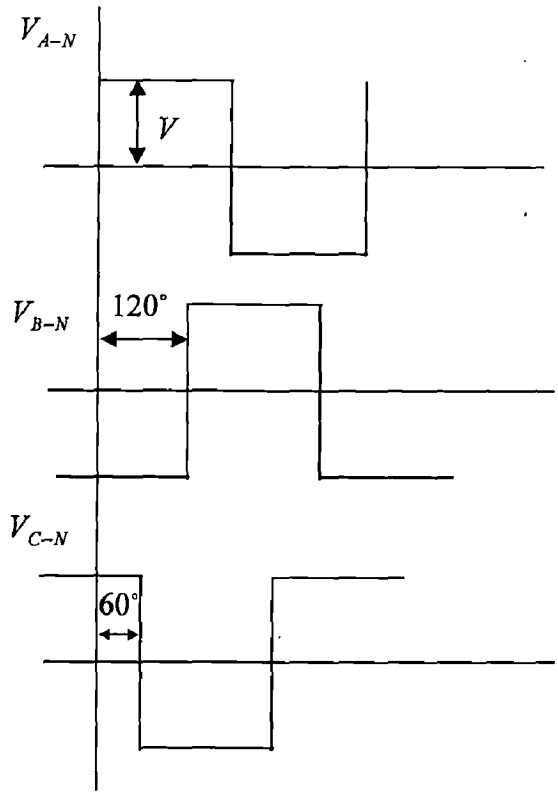

Fig 2.2 Inverter output voltage waveforms

Table 2.1 Harmonic sequences

Sequences	Harmonic Number *n*				
Zero-sequence	3	9	15	21	...
Positive-sequence	1	7	13	19	...
Negative-sequence	5	11	17	23	...

Thus the output (ac) side voltage harmonics that appear in the transformer secondary are $6q \pm 1$ where q = 1, 2, 3,... including both positive and negative sequences. The dc side current harmonics generated are given by $6q$ where q = 1, 2, 3,.... Hence, we can state that the ac side harmonics are complementary of the dc side harmonics.

2.3 Twelve step inverter:

Let us consider two 6-step inverters that are connected as shown in Fig. 2.3. In this diagram, only the dc side is shown. It can be seen that both these inverters are being supplied from the same dc source, which has a potential of $V_{dc} = 2V$.

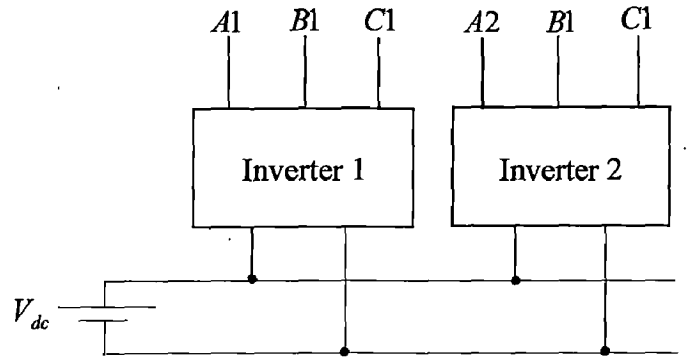

Fig. 2.3 Dc side connection diagram of two 6-step inverters

2.3.1 Elimination of Dc Side Harmonics:

Let us consider the 6^{th} harmonic component on the dc side of the 1^{st} inverter. It can be eliminated if another 6^{th} harmonic component that is shifted by 180° on its frequency is added to it. Their sum will then add up to zero. To effect a phase shift of 180° from the 2^{nd} inverter, firing instants of all the switches of the 2^{nd} inverter must lag the corresponding switches of the 1^{st} inverter by 30° on fundamental frequency such that the 6^{th} harmonic component of the 2^{nd} inverter lags that of the 1^{st} inverter by 180°. Moreover, it force the odd multiples of the 6^{th} harmonic component to cancel out. For example, the 18^{th} harmonic component of the 2^{nd} inverter will lag that of the 1^{st} inverter by 540° making them in phase opposition. Thus, only the even multiples of the 6^{th} harmonic will remain in the dc side.

2.3.2 Elimination of Ac Side Harmonics:

Let us assume that the firing angles of the 2^{nd} inverter are delayed by 30° on fundamental frequency with respect to that of the 1^{st} inverter as mentioned above. The respective phase-*A* output voltage waveform of the two inverters are shown in Fig. 2.4 where the fundamental voltage of one of the inverters (2^{nd} inverter) lags that of the other

(1^{st} inverter) by θ. The Fourier expressions of the phase-A voltage waveforms of these two inverters are then given by

$$f_{A1}(t) = \frac{4V}{\pi}\sin(\omega t) + \sum_{n=5,7,\ldots} \frac{4V}{n\pi}\sin(n\omega t) \tag{2.4}$$

$$f_{A2}(t) = \frac{4V}{\pi}\sin(\omega t - \theta) + \sum_{n=5,7,\ldots} \frac{4V}{n\pi}\sin(n\omega t - n\theta) \tag{2.5}$$

Where θ is equal to 30° for this case.

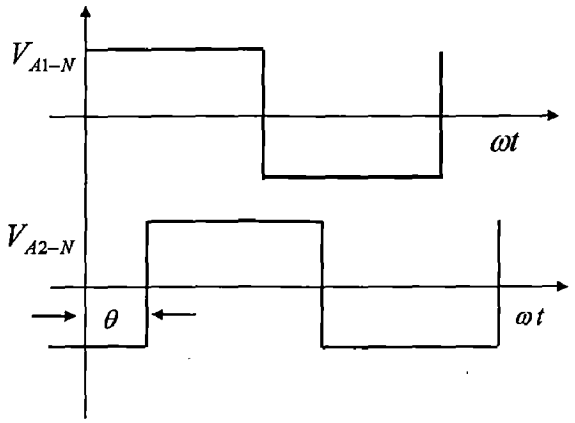

Fig. 2.4 Output waveforms of the phase-shifted inverters

From eqs. (2.4 And 2.5) it's obvious that the 5^{th} and 7^{th} harmonic components of the 2^{nd} inverter are phase shifted by -150° and -210° respectively with respect to that of the 1^{st} inverter. In order to eliminate these two harmonic components, the 5^{th} harmonic component needs to be further phase shifted by -30° and the 7^{th} harmonic component needs a phase shift of $+30^\circ$. this means that the negative sequence be phase shifted by -30° while the positive sequence by $+30^\circ$.

We can connect any three single-phase transformers in $y-\Delta$ to provide $\pm 30^\circ$ phase shift between their primary and secondary windings. In that case, if the positive sequence is phase shifted by $+30^\circ$, the negative sequence gets phase shifted by -30° and vice versa. To explain this, consider the $y-\Delta$ connected transformer that is shown in Fig. 2.5. The uppercase letters denotes the primary side while the secondary side is denoted by lowercase letters. Also adding a suffix 1 to the winding names differentiates the terminal names and the windings. The voltage vector diagram for the positive sequence components has shown in Fig. 2.6 while that of the negative sequence is given

in Fig. 2.7. It is evident from Fig. 2.6 that the voltage vector V_{A-N} leads $-V_{C-A}$ and hence $V_{a-N} = -V_{c-a}$ by 30°. Similarly from Fig. 2.7 we can observe that V_{A-N} lags V_{a-N} by 30°. As the phasor diagrams are valid for all frequencies, it can be deduced that the phase shift provided is same on all frequencies. This means that if the fundamental gets phase shifted by $+30°$, all positive sequence harmonic components (e.g., 7th, 13th etc.) also get phase shifted by +30° on their own frequencies, while the negative sequence components (e.g., 5th, 11th etc.) are shifted by –30° on their respective frequencies.

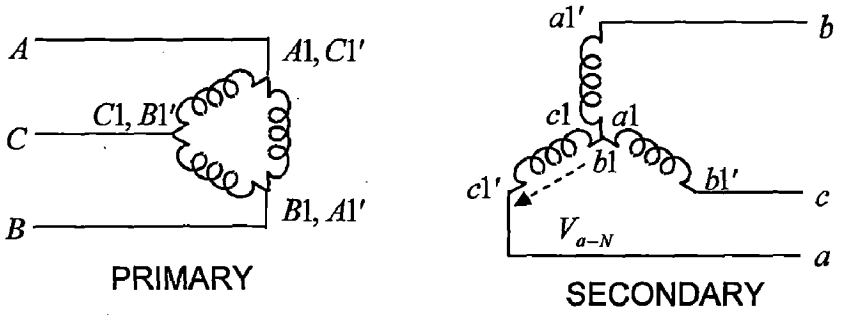

Fig. 2.5 Schematic diagram of three single-phase transformers to provide A phase shift of $+30°$ to the positive sequence

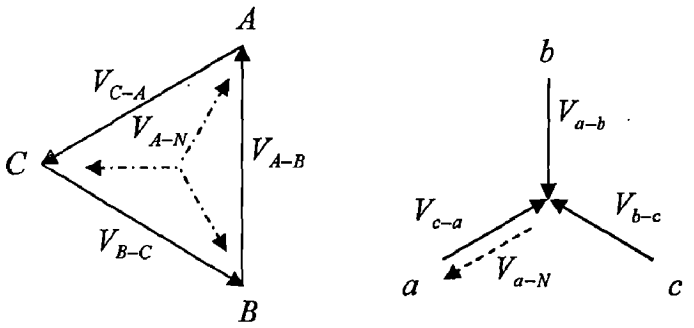

Fig. 2.6 Positive sequence phasor diagram

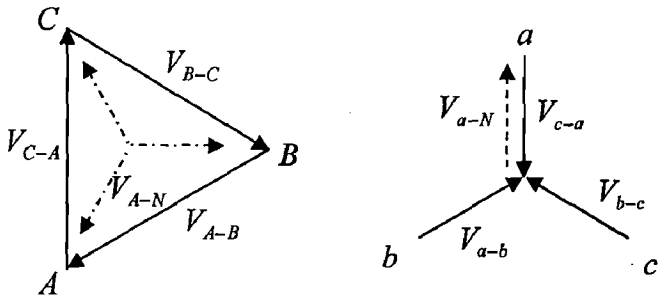

Fig. 2.7 Negative sequence phasor diagram

The transformer connection for the addition of the output waveforms of two inverters is shown in Fig. 2.8. The primary side $A1, C1' - B1, A1' - C1, B1'$ of transformer 1 and $A2, C2' - B2, A2' - C2, B2'$ of transformer 2 are connected to the output of inverter 1 and 2 respectively. As shown in the Figure that the primaries are connected in Δ. The secondary of transformer 2 is connected in Δ. The secondary of transformer 1 is connected to the secondary terminals of transformer 2 as shown in the Figure, which is obviously a y-connection. The connection diagram of the transformer 1 is similar to the one shown in Fig. 2.5. Let Z be the output of a particular phase of the primary side of inverter 1 and X be that of inverter 2 and z and x be the corresponding vectors in the secondary side. The vector z lags the vector Z by 30° for positive sequence components. Similarly, the vector z leads the vector Z by 30° for negative sequence components. It is also to be noted that the vector x is in phase with the vector X*[10]*.

For all the components in the Fourier expansion, X lags Z by $(6q \pm 1) \times 30^\circ$ for $q = 1, 2, \ldots$. This means that x lags Z by the same amount. Therefore, the phase shift between x and z is given by $-(6q+1) \times 30^\circ + 30^\circ$ for positive sequence and $-(6q-1) \times 30^\circ - 30^\circ$ for negative sequence. The phase shift between the vectors x and z for some of the harmonic components is shown in Table 2.2. It is evident from Table 2.2 that the 5^{th} and 7^{th} harmonic components of x are in phase opposition to that of z and will thus cancel out provided that their magnitudes are equal. To accomplish this, the turns ratio of transformer 1 is kept as $1:\sqrt{3}$ while it is chosen 1:1 for transformer 2.

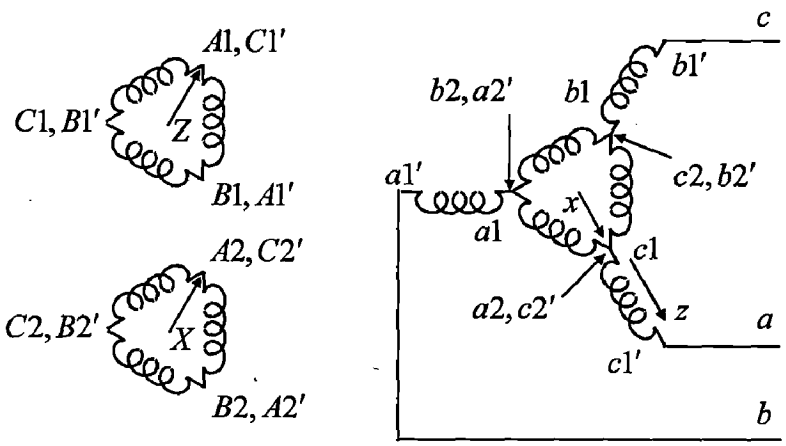

Fig. 2.8 The transformer configuration to add the output of two inverters

Table 2.2 Phase shift of x with respect to z

Harmonic number	Phase shift
1	0°
5, 7	–180°
11, 13	–360°

The circuit discussed above is that of a 12-step inverter. The output line-to-line voltage waveform for this inverter is shown in Fig. 2.9

It is seen that by providing a phase shift of 30° between two inverter-transformer combinations, we are able to generate a 12-step waveform with a certain harmonic spectrum. If we now add two such inverters, we shall be able to get a 24-step inverter. In this case however the successive inverter-transformers must have a phase difference of 15°. In a similar way, we can construct a $6q$-step inverter by providing a phase shift of $360^{\circ}/6q$ between the successive inverter-transformers.

The 12-pulse inverter is simulated using pscadv4.2.1 software. The system configuration is given in Appendix. The graphs shown in the Fig 2.9 and Fig 2.10 are the 12 pulse inverter output voltages for various cycles and one cycle. Its harmonic spectrum is shown in Fig 2.11

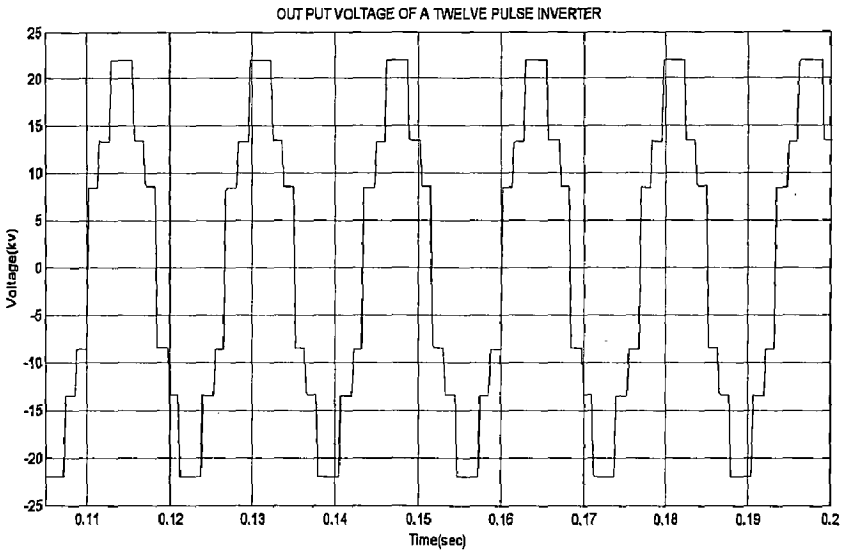

Fig. 2.9 Out put voltage of twelve-pulse inverter

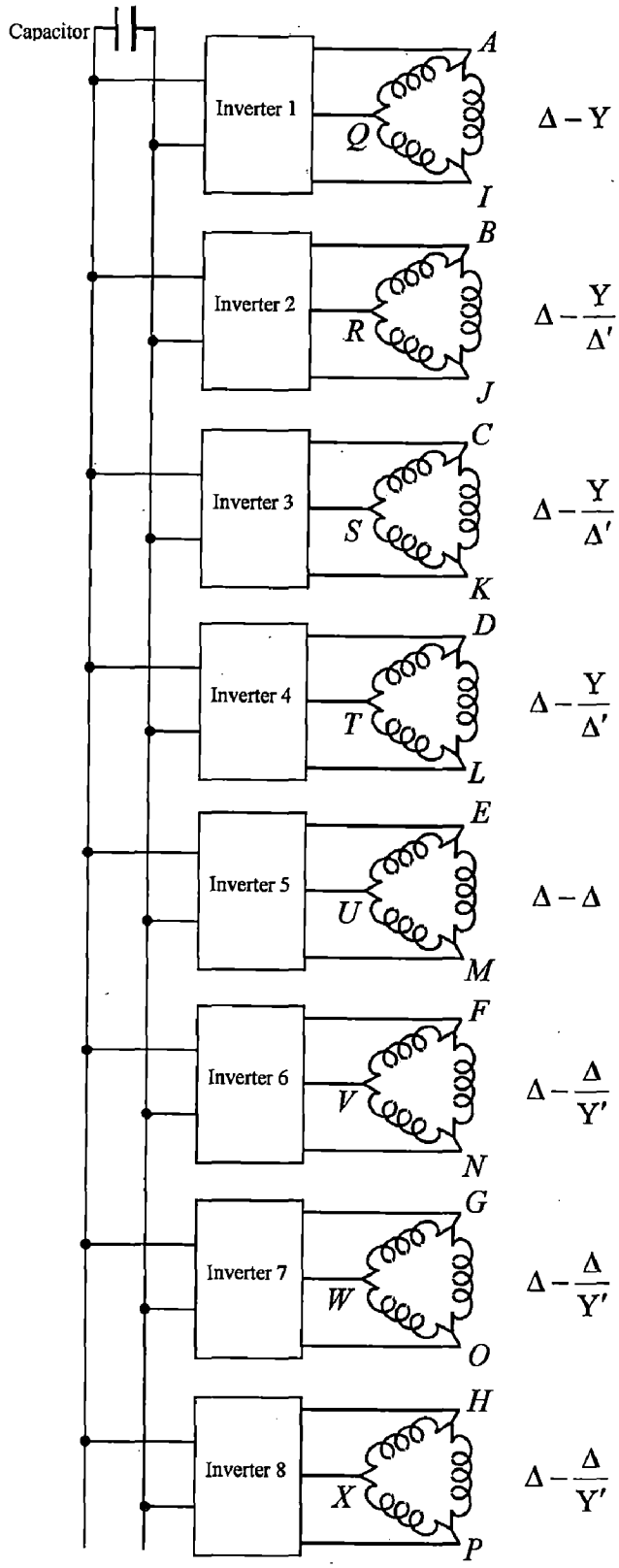

Fig. 2.13 Schematic diagram of 48 pulse inverter

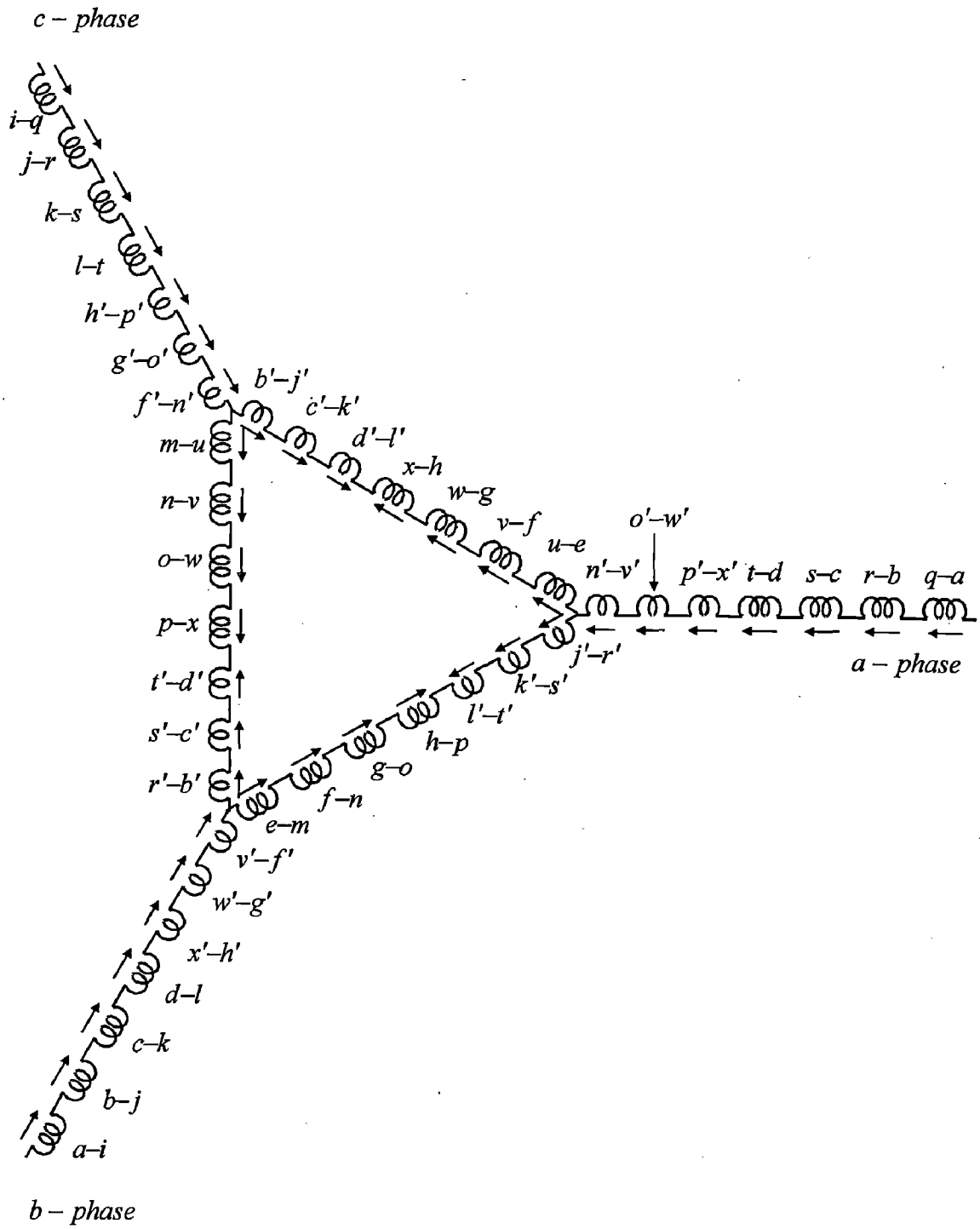

Fig. 2.14 transformer configuration for a 48-step inverter

The output voltage of the 48 pulse inverter is shown in the Fig2.15and Fig2.16and the corresponding harmonic spectrum is given in Fig2.17

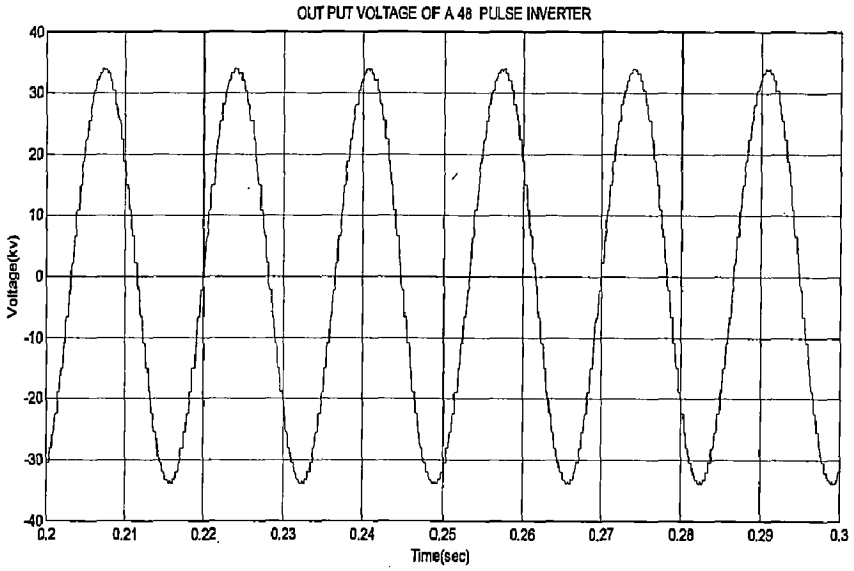

Fig. 2.15 Output Voltage of 48-pulse inverter

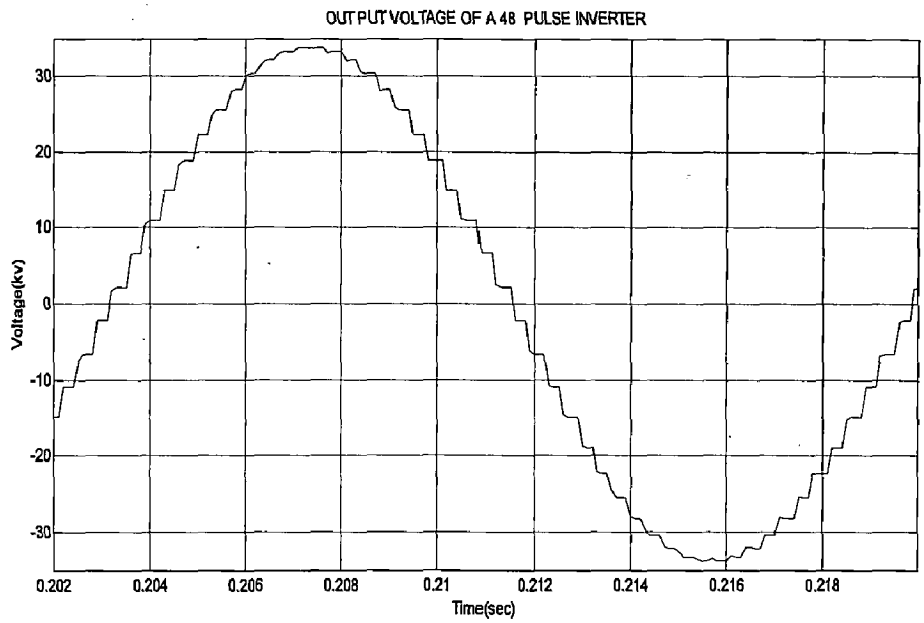

Fig. 2.16 Output voltage of 48-pulse inverter with one cycle

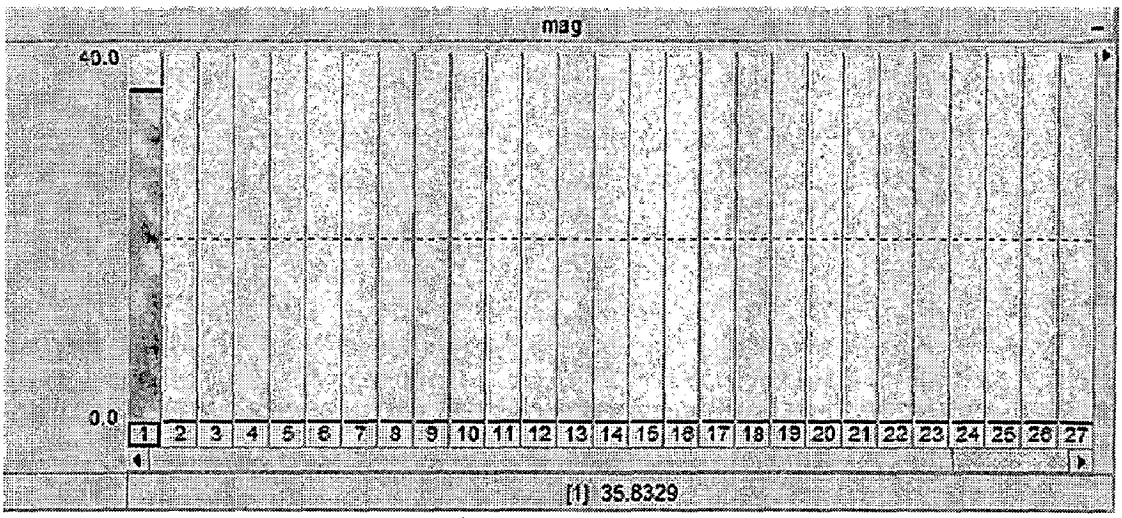

Fig. 2.17 Harmonic spectrum of 48-pulse inverter

2.5 Conclusions:

In this chapter, the configuration of 12-pulse, 24-pulse and 48 pulse inverters by using different transformer connections are explained and the simulation of the inverters is performed in PSCAD software. The output voltage of the 48-pulse inverter is almost sinusoidal. The inverter output voltages (12 pulse and 48 pulse) are included along with their harmonic spectrum.

CHAPTER 3

SSSC USING MULTI-PULSE INVERTER

3.1 Introduction:

The chapter describes a novel series compensator based on multipulse inverters for a transmission line .The series compensated voltage source inverter is called static synchronous series compensator. The theory of its operation has described in chapter1. Synchronous voltage source implemented by voltage source inverters is able to produce a synchronous voltage similar to the one generated by synchronous machine at fundamental frequency. For series compensation, the synchronous voltage source has connected in series with the line through insertion transformers. The real and reactive power of the compensated line has governed by the phase angle and magnitude of the injected voltage with respect to the line current. When the injected voltage is in quadrature with the line current, only the real power has influenced.

3.2 Description of Test System:

In this work, the IEEE First bench Mark model is considered [11]. All the transmission line parameters have taken as lumped parameters. The infinite bus is considered as a constant source. The system data is shown in Appendix A. Simulation studies have been carried out by connecting the twelve pulses and forty-eight-pulse inverter to the above test system. The single line diagram of the above test system incorporating the inverter structure has shown in Fig. 3.1.

The graphical view of the simulated system in PSCAD/EMTDC is shown in Appendix A. The steady state results of the above test system achieved with PSCAD/EMTDC had presented in this chapter.

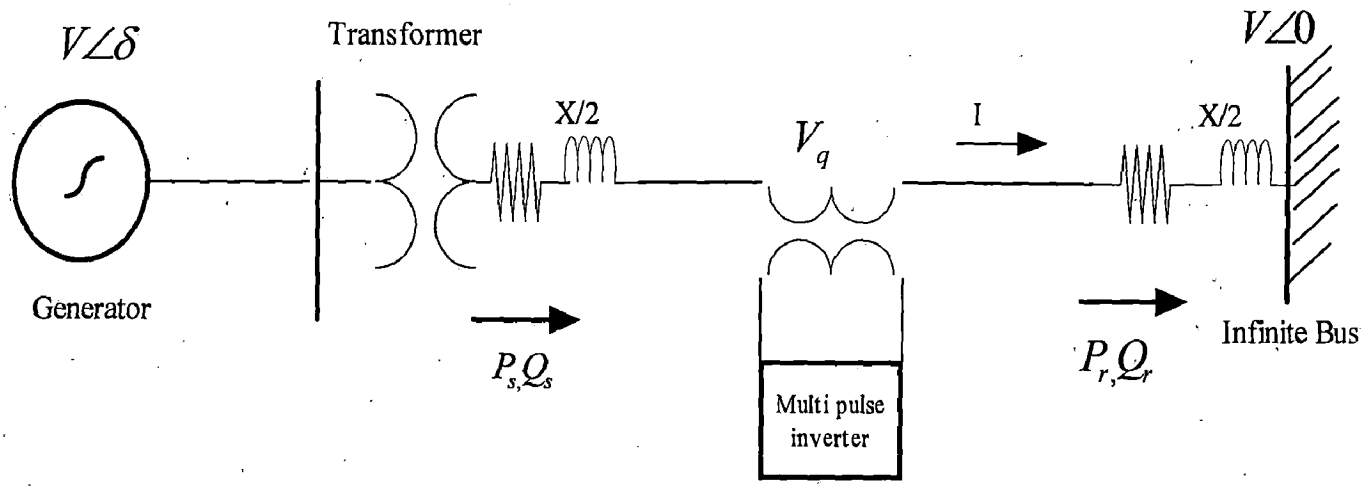

Figure 3.1: Single line diagram of the SSSC connected system

3.3 Basic control scheme of sssc:

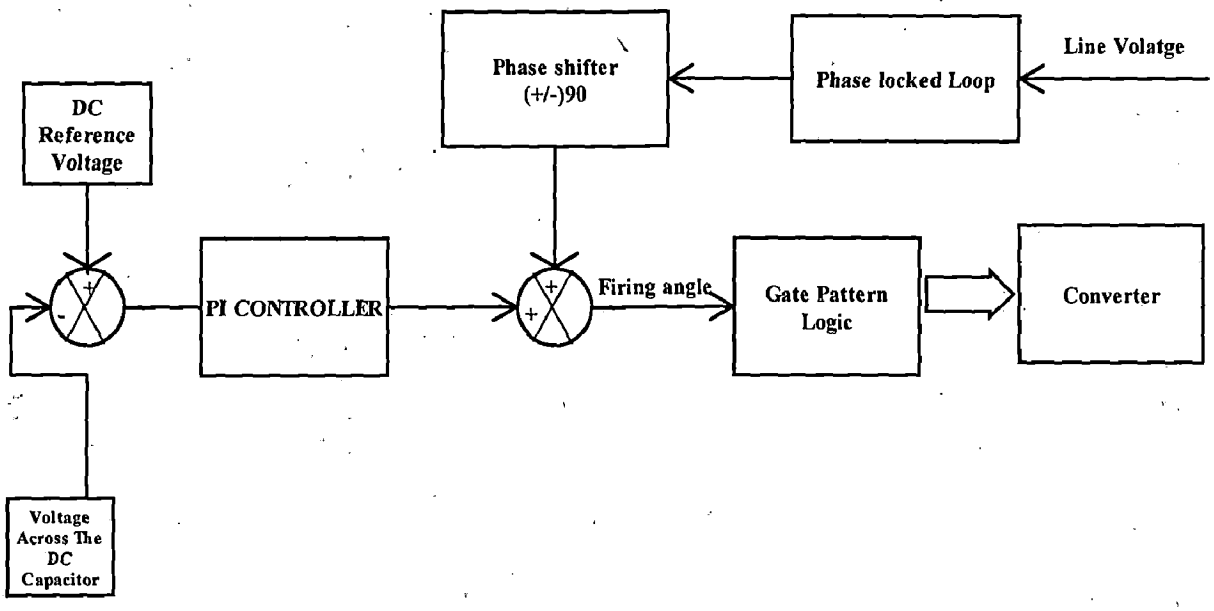

Fig 3.2 Basic control structure of SSSC

A possible control scheme for the controlled SSSC converter is shown in Fig 3.2. The inputs to the controller are line voltage and the dc voltage across the capacitor and the reference capacitor voltage. An instantaneous 3-phase set of line voltages are used to calculate the angle θ that is phase locked to the one of the phase of the line voltage and it is given to the phase shifter shown in Fig3.2. The dc voltage across the capacitor is

compared with the fixed DC voltage (ref voltage) and the error signal is given to the PI Controller. The output angles of the phase shifter, PI controller is added, and the firing angle is given to the gate pattern logic of the inverter.

The purpose of the PI controller is to retain the charge on the dc capacitor and to inject a voltage in quadrature with the line current. The magnitude of the injected voltage is directly proportional to the dc capacitor voltage. If the injected voltage is not in quadrature with the line current, real power exists at the ac terminals of the inverter, which then either charges or discharges the dc capacitor, resulting in a deviation in the voltage from its set point. The PI controller then advances or retards the phase of the injected voltage relative to line current in order to adjust the power at ac terminals and keep the dc voltage constant. At steady state, when the dc voltage remains constant, no real power is exchanged at the ac terminals[10].

The inverter will generate the required injected voltage and the voltage is connected to the system through the inter phasing transformers. The series injected voltage into the system can be varied by changing the dc ref voltage in the above shown control diagram in Fig 3.2

3.4 Simulation Results with 12-pulse inverter:

The test system has simulated by using PSCAD/EMTDC software. The real power variation has observed by varying the d.c reference voltage. The corresponding variation of the real power and the d.c voltage across capacitor has shown in the graphs 3.3 and 3.4. The injected voltage is exactly 90° lagging the line current and it has shown in Fig 3.5.

The simulation time for test system has taken as 10 sec. For 0 to 2 sec, the sssc not connected to the system. At 2sec, the SSSC connected to the system. We can observe the change in the real power in the graph. The real power has changed from 0.75 p.u, to 0.9 p.u. The d.c ref voltage changed at 6.5 sec of the simulation time with the help of slider (a tool that is available in PSCAD) then we can observe the variation of the real power.

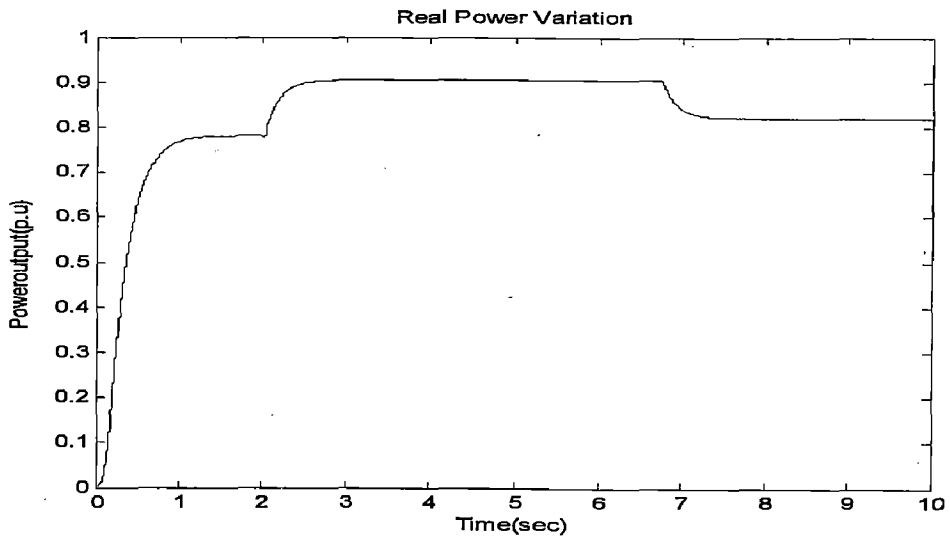

Fig 3.3Real power variation in transmission line

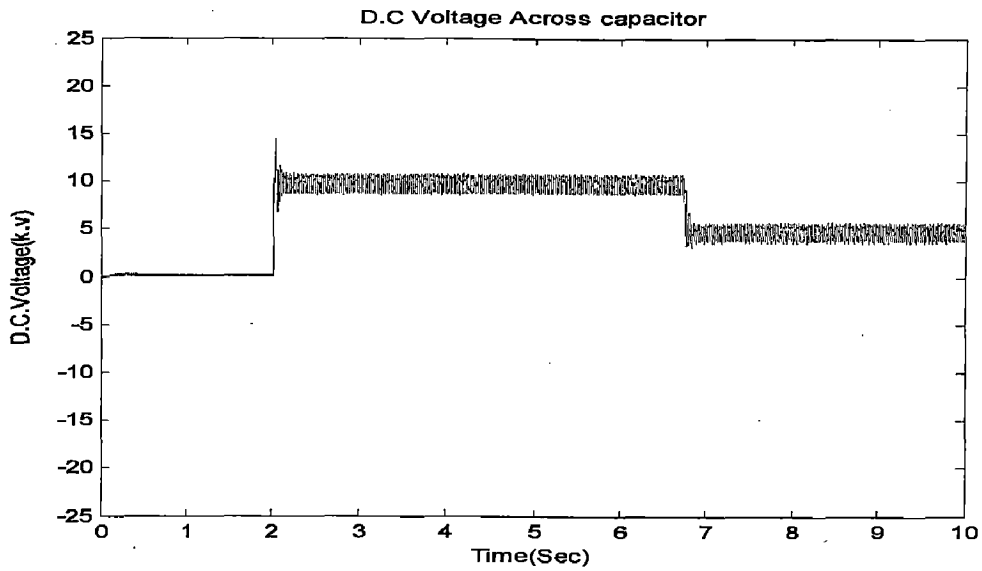

Fig 3.4 D.C voltage across capacitor

The injected voltage is exactly 90° to the line current, it has shown in the simulation result of Fig 3.5. The synchronous voltage source is acting like a static synchronous series compensator.

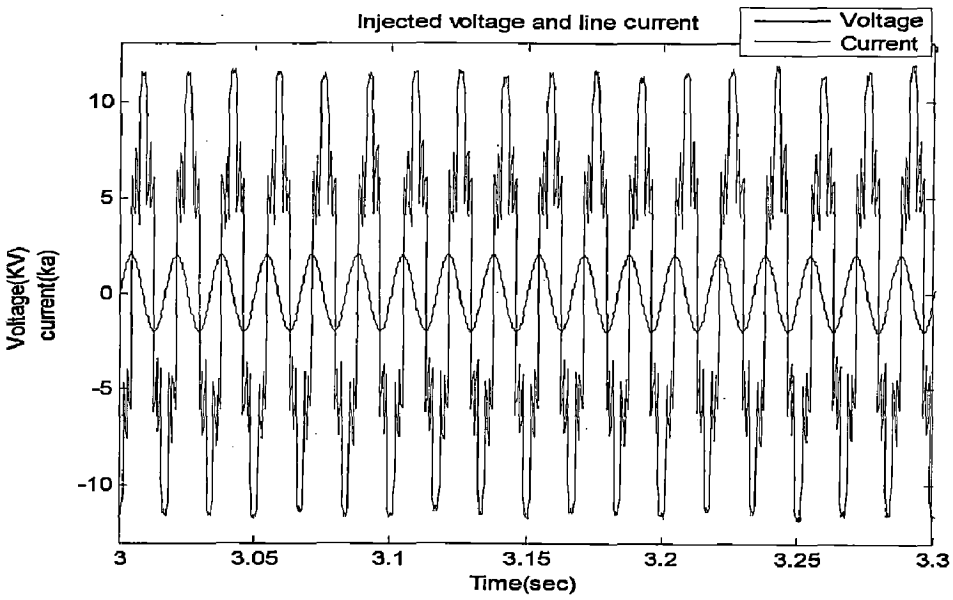

Fig 3.5 injected voltage and line current

3.5 Simulation Results with 48-pulse inverter:

The simulation results of the test system with 48-pulse inverter is shown in the below Figures. The variation of d.c ref voltage with respect to the time has given in table 3.1

Table 3.1 simulation time and D.C ref voltage

Simulation Time(sec)	Ref voltage(Kv)
0-2	5
2-4	5
4-6	10
6-8	8
8-10	5

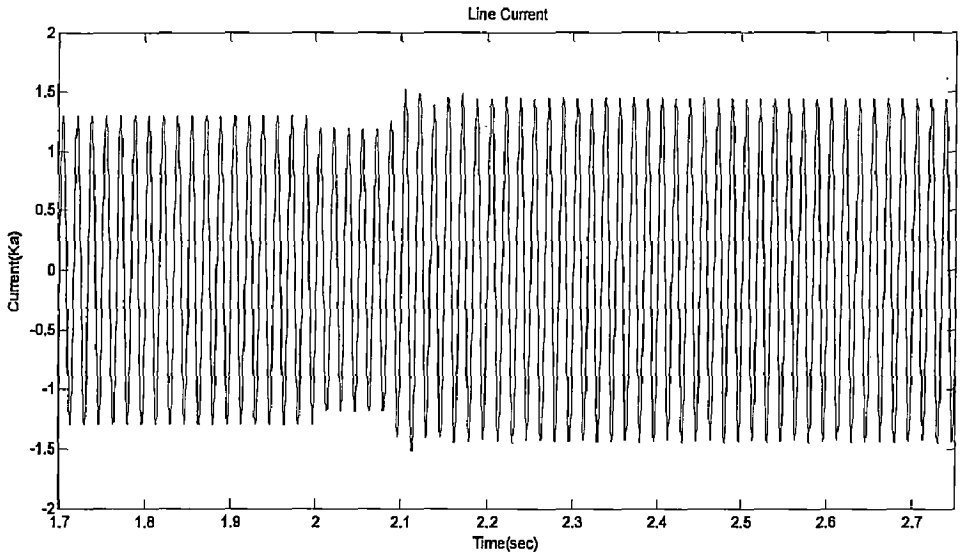

Fig 3.6 variation of line current in the transmission line (1.7sec to 2.7sec)

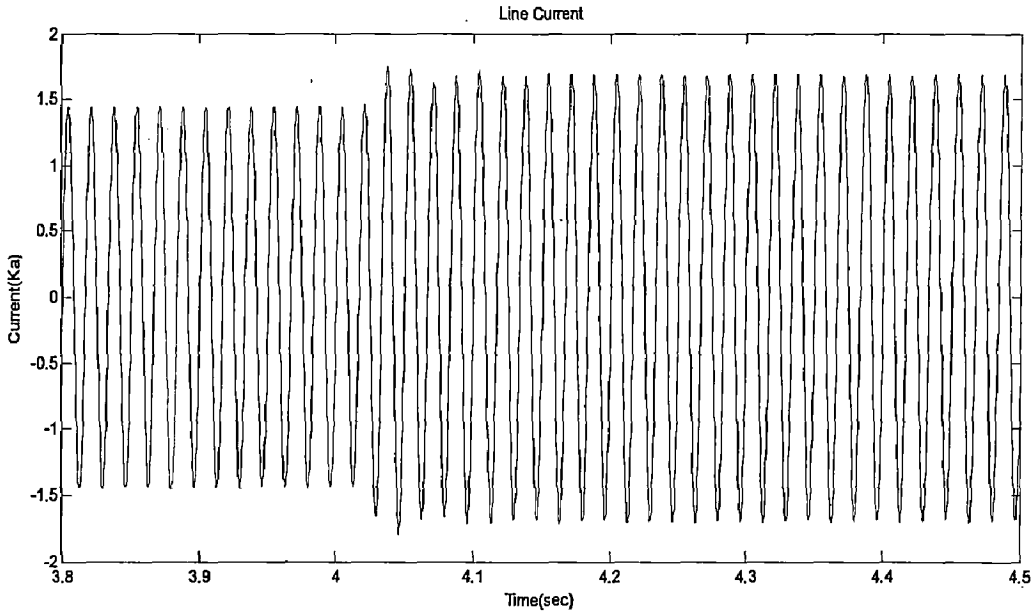

Fig 3.7 variation of line current in the transmission line (3.8sec to 4.5 sec)

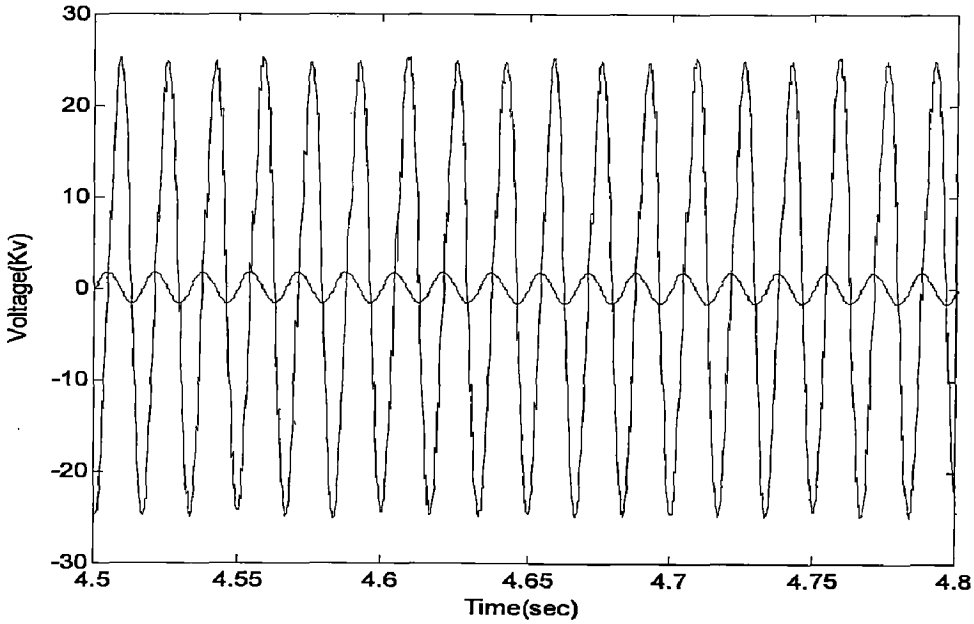

Fig 3.8 relation between injected voltage and line current

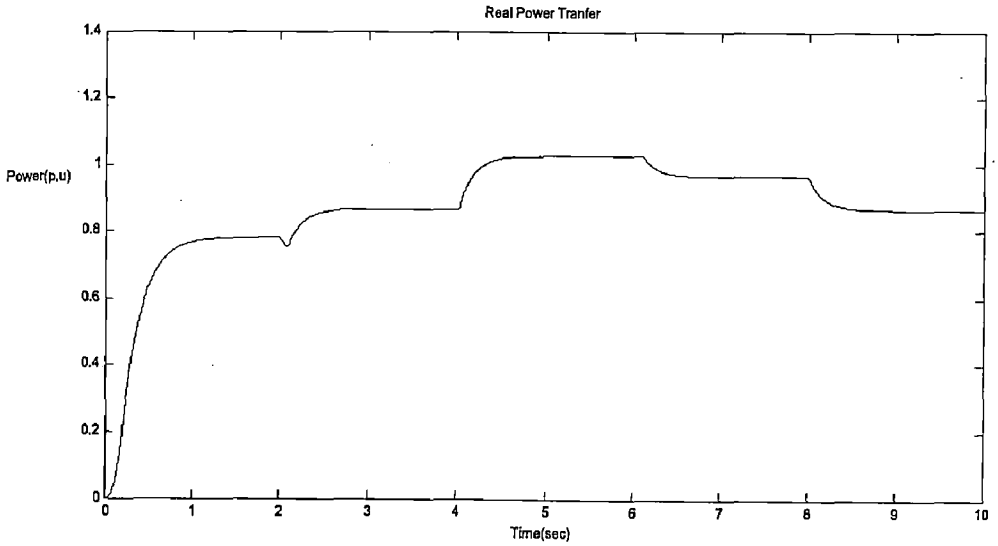

Fig 3.9 variation of real power in the transmission line

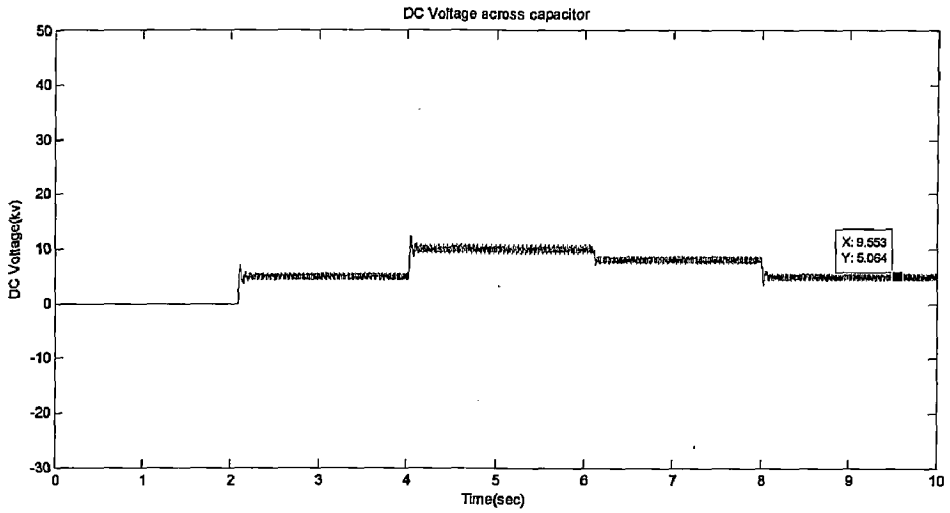

Fig 3.10 variation of D.C voltage across capacitor

Simulation results of the test system with forty-eight pulse inverter is shown in the graphs from 3.6 to 3.10.In Fig 3.6 and Fig 3.7 the variation of the line current is shown. From these Figures, we can observe the change in the line current. The line current in the system has changed due to the injection of quadrature voltage in the system. Fig 3.8 shows the injected line voltage is 90° to the line current. Variation of the D.C ref voltage has shown in the table 3.1 the corresponding power changes and the D.C voltage changes have shown in the Fig 3.9 and Fig 3.10 respectively.

3.6 Conclusions:

In this chapter, operation of a SSSC based on 12 pulse and 48 pulse VSC has been presented. An appropriate control scheme for the series converter has been discussed Simulation results for illustrating the operation of the SSSC in the transmission grid has presented. We can observe the variation of the real power in the transmission line, the phase relation ship between the injected voltage, line current and the d.c voltage across the capacitor of the inverter.

CHAPTER 4

SSSC USING 3-LEVEL HALF-BRIDGE DIODE-CLAMPED MULTI LEVEL INVERTER (DC MLI) MODULES

4.1 Introduction:

Conventional power electronic converters can switch each input or output connection between two possible voltage (or possible current) levels, namely those of the internal DC voltage (or current) link. On the other hand, multilevel converters can switch their outputs between many voltage or current levels, and have multiple voltage or current sources (or simply capacitors or inductors) as part of their structure. A multilevel converter can be implemented in many different ways, each with attendant advantages and disadvantages. The simplest techniques involve the parallel or series connection of conventional converters to form the multilevel waveforms[11]. More structures that are complex effectively insert converters within converters. Whatever approach is chosen, the subsequent voltage or current rating of the multilevel converter becomes a multiple of the individual switches, and so the power rating of the converter can exceed the limit imposed by the individual switching devices.

4.2 Multilevel Inverters:

There are several types of multilevel inverters. The three main types of multilevel converters are diode-clamped multilevel converters, flying-capacitor (also referred to as capacitor-clamped) multilevel converters, and cascaded H-bridges multilevel converters.

At this point, it seems appropriate to discuss the difference between the terms "multilevel converter" and "multilevel inverter." The term "multilevel converter" refers to the converter itself. Furthermore, the connotation of the term is that power can flow in one of two directions. Power can flow from the ac side to the dc side of the multilevel converter. This method of operation is called the rectification mode of operation. Power can also flow from the dc side to the ac side of the multilevel converter. This method of

operation is called the inverting mode of operation. The term "multilevel inverter" refers to using a multilevel converter in the inverting mode of operation. In this chapter, we will discuss different types of multilevel inverters later in more detail.

The main function of a multilevel inverter is to produce a desired ac voltage waveform from several levels of dc voltages these dc voltages may or may not be equal to one another. The ac voltage produced from these dc voltages approaches a sinusoid.

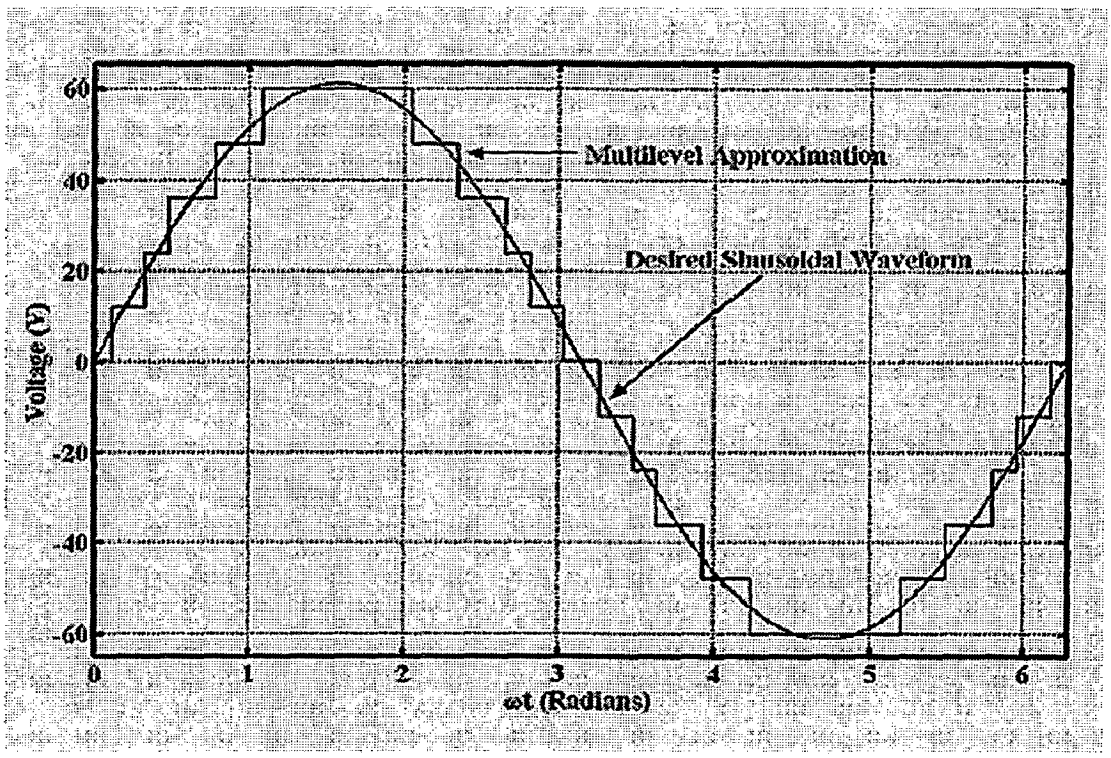

Fig. 4.1: Output of a Multi level inverter [16].

As an example of a multilevel inverter, consider the staircase waveform in Fig. 4.1. In this Figure, five 12 V dc sources produce a staircase waveform with a peak-to-Peak voltage of 120 V. In this case, the multilevel inverter produces a fair approximation to a sinusoidal waveform [16]. As one increases the number of dc sources, this approximation will get better and better. Ideally, as the number of dc sources approaches infinity, the staircase waveform will approach the desired sinusoid.

Fig 4.1 also illustrates the "multilevel fundamental switching scheme." This scheme simply refers to determining the switching angles of the multilevel inverter such

that a staircase waveform can be produced that approximates a sinusoid. Furthermore, the fundamental frequency of the produced staircase waveform and the frequency of the desired sinusoid are the same.

Other switching schemes can be implemented on a multilevel inverter but do not produce a staircase waveform [16]. Some examples include Bipolar Programmed PWM, Uni polar Programmed PWM, and Virtual Stage PWM.

One pitfall of using multilevel inverters to approximate sinusoidal waveforms concerns harmonics. As one can see in Fig. 4.1 the staircase, waveform produced by the multilevel inverter contains sharp transitions. From Fourier series theory, this phenomenon results in harmonics, in addition to the fundamental frequency of the sinusoidal waveform.

However, by altering the times at which these sharp transitions occur, one can reduce and/or eliminate some of the unwanted harmonics. Furthermore, by increasing the number of dc sources, more harmonic content can be eliminated.

In the next session, the basic principle of a diode clamped multi level inverter is presented.

4.3 Basic Operation of Diode-clamped Multilevel Inverter:

A three-level diode-clamped inverter is shown in Figure 4.2. In this circuit, the DC bus voltage is split into three levels by two series-connected bulk capacitors, C_1 and C_2. The middle point of the two capacitors n can be defined as the neutral point[15]. The output voltage V_{an} has three states: $V_{dc}/2$, 0, and $-V_{dc}/2$. For voltage level $V_{dc}/2$, switches $S_1$and S_2 need to be turned on; for -Vdc/2, switches S_1' and S_2' need to be turned on; and for the 0 level, S_2 and S_1' need to be turned on.

The key components that distinguish this circuit from a conventional two-level inverter are D1 and D2. These two diodes clamp the switch voltage to half the level of the DC bus voltage. When both $S_1$and S_2 turn on, the voltage across 'a' and '0' is V_{dc}, i.e., $V_{a0} = V_{dc}$.

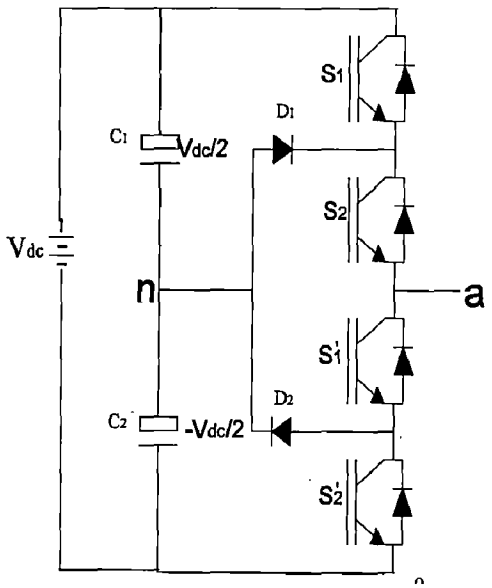

Fig 4.2: Three-level Diode-clamped multilevel inverter circuit topology

In this case, D2 balances out the voltage sharing between S_1' and S_2' with S_1' blocking the voltage across C_1 and S_2' blocking the voltage across C_2.Notice that output voltage v_{an} is ac, and v_{a0} is dc. The difference between v_{an} and v_{a0} is the voltage across C_2, which is Vdc/2. If the output is removed out between 'a' and '0', then the circuit becomes a DC/DC converter, which has three output voltage levels: V_{dc}, $V_{dc}/2$, and 0.

Fig 4.3 shows a five-level diode-clamped converter in which the dc bus consists of four capacitors, C1, C_2, C_3, and C4. For dc-bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/4$, and each device voltage stress will be limited to one capacitor voltage level $Vd_c/4$ through clamping diodes. The switching states are given in Table 4.1.

There are 5 switch combinations to synthesize five level voltages across *a* and *n*.

- For voltage level $V_{an} = V_{dc}/2$, turn on all upper switches S_1-S_4.
- For voltage level $V_{an} = V_{dc}/4$, turn on three upper switches S_2-S_4 and one lower switch S_1'.
- For voltage level $V_{an} = 0$, turn on two upper switches S_3 and S_4 and two lower switches S_1' and S_2'.
- For voltage level $V_{an} = -V_{dc}/4$, turn on one upper switch S_4 and three lower switches S_1'-S_3'.

- For voltage level V_{an} = $-V_{dc}/2$, turn on all lower switches S_1'-S_4'.

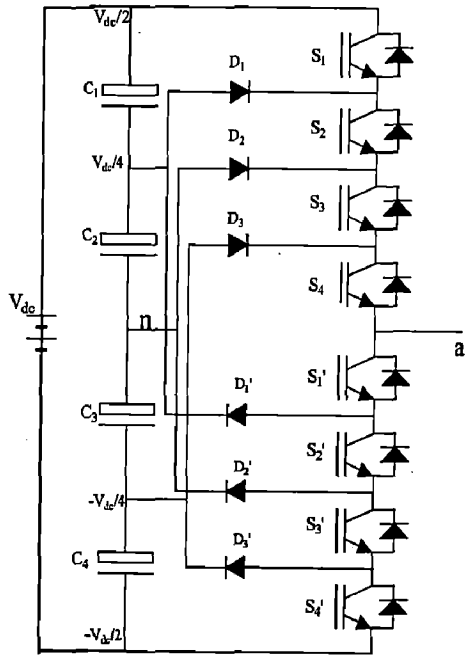

Fig 4.3Five-level Diode-clamped multilevel inverter circuit topology

Table 4.1: switching states of 5-level DC MLI

	S_1	S_2	S_3	S4	S_1'	S_2'	S_3'	S_4'
Vdc/2	1	1	1	1	0	0	0	0
Vdc/4	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
-Vdc/4	0	0	0	1	1	1	1	0
-Vdc/2	0	0	0	0	1	1	1	1

Although each active switching device is only required to block a voltage level of V_{dc}/ (m - 1), the clamping diodes must have different voltage ratings for reverse voltage blocking. Using D_1' of Figure 4.3 as an example, when lower devices S_2' ~ S_4' are turned on, DI needs to block three capacitor voltages, or 3Vdc/4. Similarly, D_2 and D_2' need to block $2Vd_c/4$, and D_3 needs to block $3Va_c/4$. Assuming that each blocking diode voltage rating is the same as the active device voltage rating, the number of diodes required for each phase will be (m - 1) x (m - 2). This number represents a quadratic increase in m.

When m is sufficiently high, the number of diodes required will make the system impractical to implement. If the inverter runs under PWM, the diode reverse recovery of these clamping diodes becomes the major design challenge in high-voltage high-power applications.

Unequal device rating:

The switch S1 conducts only during Vao= Vdc/2, while switch S4 conducts over the entire cycle except Vao=0. Such an unequal conduction duty requires different current for switching devices, the outer switches may be oversized and the inner switches may be undersized.

Capacitor voltage unbalance:

A power needs to transfer real power from ac to dc (rectifier) or dc to ac (inverter). When operating at unity power factor, the charging time for rectifier operation or discharging time for inverter operation for each capacitor is different.

The voltage unbalance problem is solved by several approaches, such as replacing capacitors by a controlled constant dc voltages source such as pulse width modulation (PWM) voltage regulators or batteries. The use of controlled dc voltage results in system complexity and cost penalties. The converter switching frequency should be kept, minimum to avoid switching losses and electromagnetic interference problems.

When operating at zero power factors, the capacitor voltages can be balanced equal charge and discharge in one-half cycles.

4.3.1 Advantages:

1. When the no. of levels is high enough, harmonic content will be low enough to avoid the need for filters.
2. Efficiency is high because all devices are switched at the fundamental frequency
3. Reactive power flow can be controlled.

4.3.2 Disadvantages:

1. Excessive clamping diodes are required when the number of levels is high.
2. It is difficult to do real power flow control for the individual inverter.

4.4 Gate Pulses Generation:

Fig. 4.4 shows the principle of PWM gate-pulse generation for the proposed SSSC. Fig.4.4 and 4.5 shows a principle of gate-pulse generation for PWM scheme. Fig. 4.4 shows two carrier signals and the reference signal to generate the gate pulses for inverter module INV1. The frequency of carrier T1, T2 is 540[Hz]. Each of two carriers has 180 °phase shift with each other. Carriers to generate gate pulses for other inverter module have 120°phase shift with each other. The reference signal V_{ref} has maximum value of 1.0 in per unit and has a sinusoidal waveform of 60Hz[18]. Fig. 4.5 shows how to generate the gate pulses using the reference and carrier signals. Carrier T1 and T2 are used as the input to generate gate pulses for inverter module.

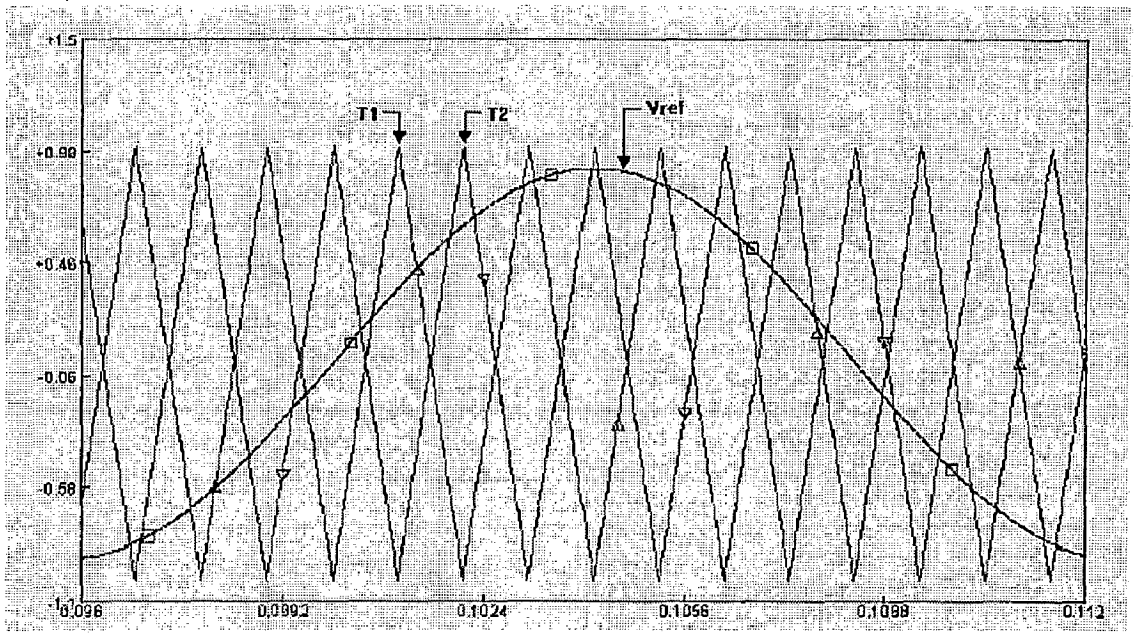

Fig 4.4 Principle of gate pulse generation Carrier and reference signal [17]

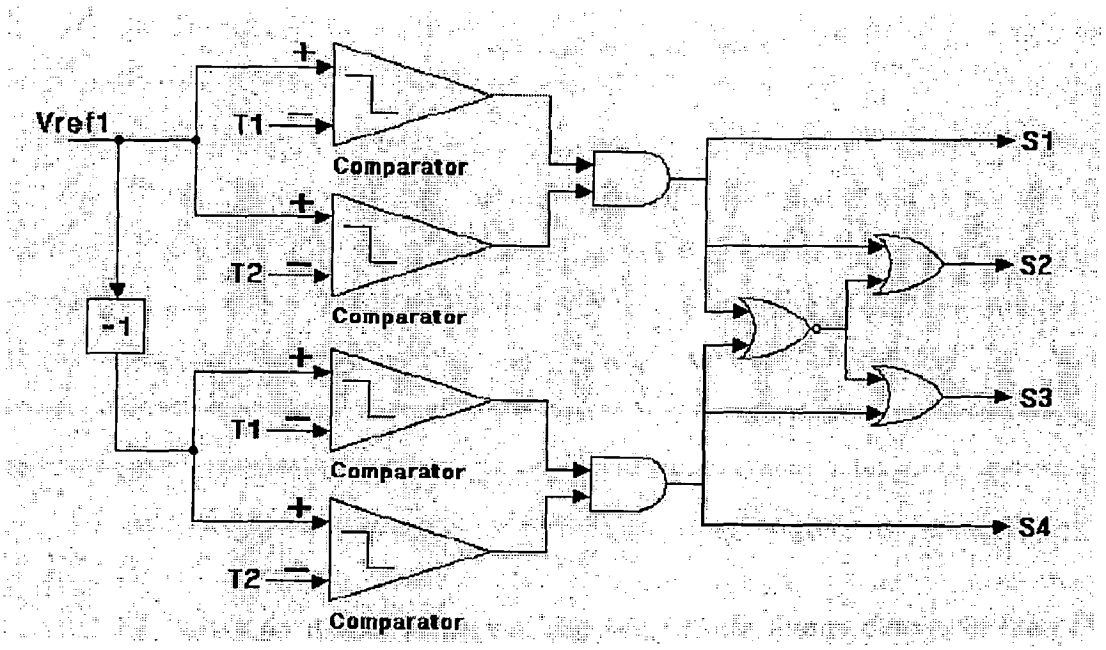

Figure 4.5: Gate pulse generation scheme [17]

As explained before, the carrier shown in Fig. 4.4 is used to generate gate pulses for building up output voltage V1. Two sets of 4 carriers with 180••phase shift from each other are needed to generate gate pulses for building up output voltage V2 and V3. These sets of carriers have 120••phase shift with each other. Since each carrier has a frequency of 540[Hz] and there are six carriers, total output voltage V_A has an equivalent switching effect of 3 [kHz]. The complete details of the ref. sine wave and carrier wave of all the modules are given in Table 4.3 below.

Table 4.2: The complete details of the ref. sine wave and carrier wave of all modules.

	Phase-a	Phase-b	Phase-c
Ref. & carriers for V_1	$V_{ref} = m_a \sin(wt)$ $T_1, -T_1$	$V_{ref} = m_a \sin(wt-120)$ $T_1, -T_1$	$V_{ref} = m_a \sin(wt+120)$ $T_1, -T_1$
Ref. & carriers for V_2	$V_{ref} = m_a \sin(wt)$ $T_2 = T_1 \angle -120, -T_2$	$V_{ref} = m_a \sin(wt-120)$ $T_2 = T_1 \angle -120, -T_2$	$V_{ref} = m_a \sin(wt+120)$ $T_2 = T_1 \angle -120, -T_2$
Ref. & carriers for V_3	$V_{ref} = m_a \sin(wt)$ $T_3 = T_1 \angle 120, -T_3$	$V_{ref} = m_a \sin(wt-120)$ $T_3 = T_1 \angle 120, -T_3$	$V_{ref} = m_a \sin(wt+120)$ $T_3 = T_1 \angle 120, -T_3$

Inverter out put voltage and phase angle are controlled by using below described technique. The voltages across two capacitors of the inverter are considered as Vc1, Vc2, Vc is the total voltage across the capacitors .the θ_d phase angle has generated through the control system blocks

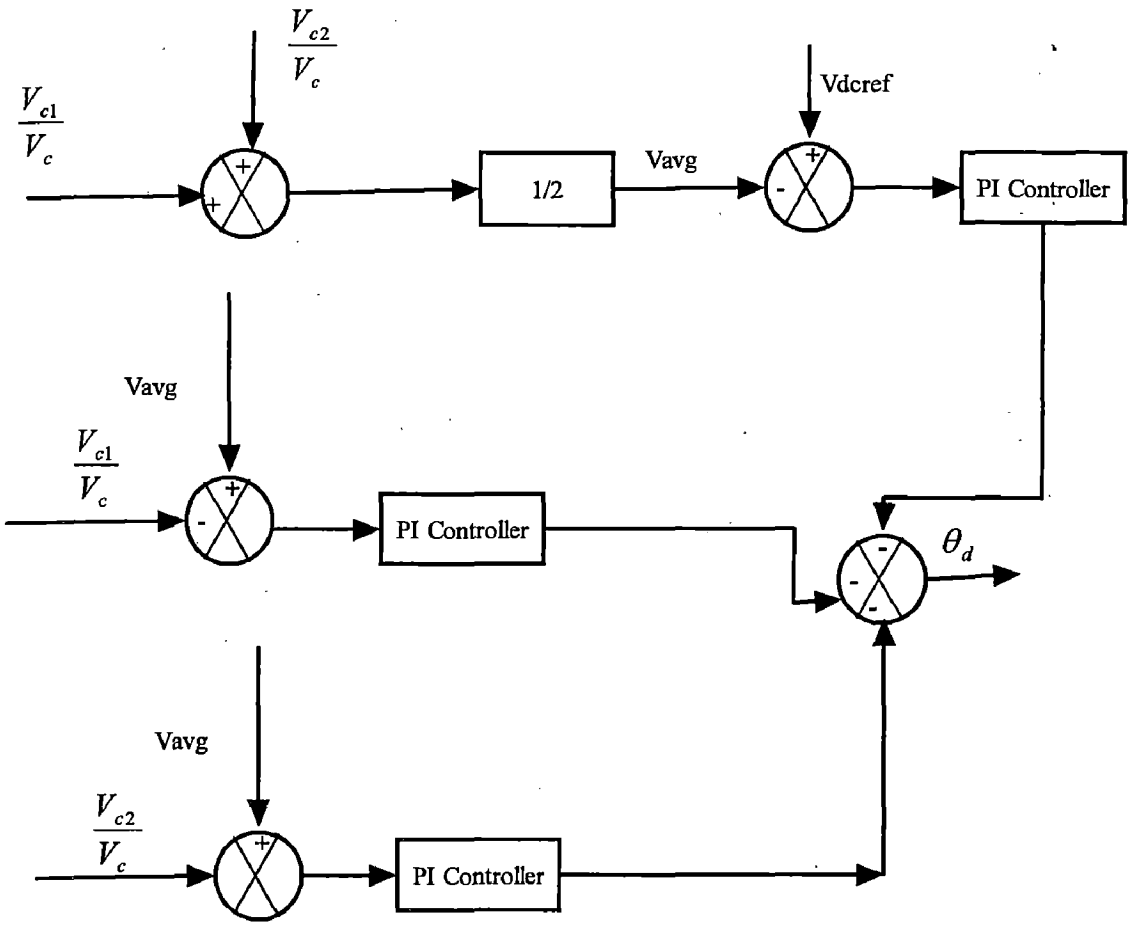

Figure 4.8: Phase angle generation for the control of output voltage of the inverter [19]

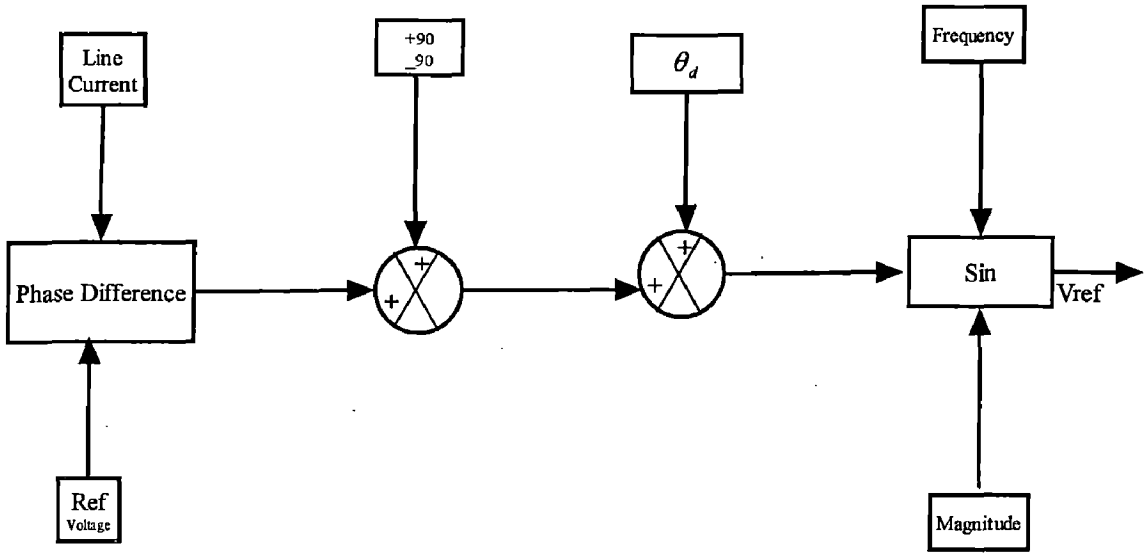

Figure 4.9: Generation of the reference voltage[19]

The angle θ_d is generated by using the control technique given in Fig 4.8.and the ref voltage is generated by using the mechanism given in Fig 4.9.The ref voltage is compared with the carrier frequency(540Hz), the gate pulse are generated by using the technique explained in section 4.4 .the gate pulses will be given to the inverter circuit.

4.6 Simulation Results:

The simulation of results static synchronous series compensator using diode-clamped multi level inverter shows below.

Table 4.3 simulation time and D.C ref voltage

Simulation Time(sec)	Ref voltage(Kv)
0-2	5
2-4	5
4-6	10
6-8	8
8-10	5

The simulation time has taken as 10 sec. the variation of ref voltage with respect to the time is shown in the table 4.3

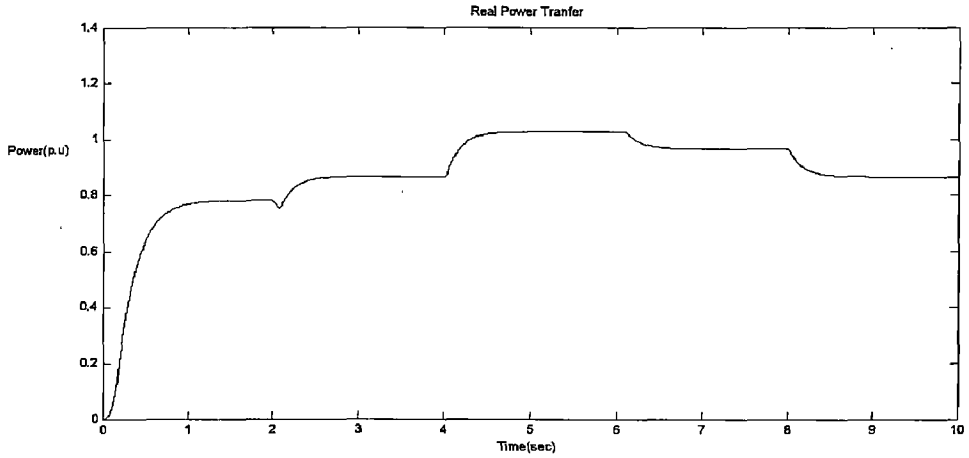

Figure 4.10: Variation of real power in transmission line

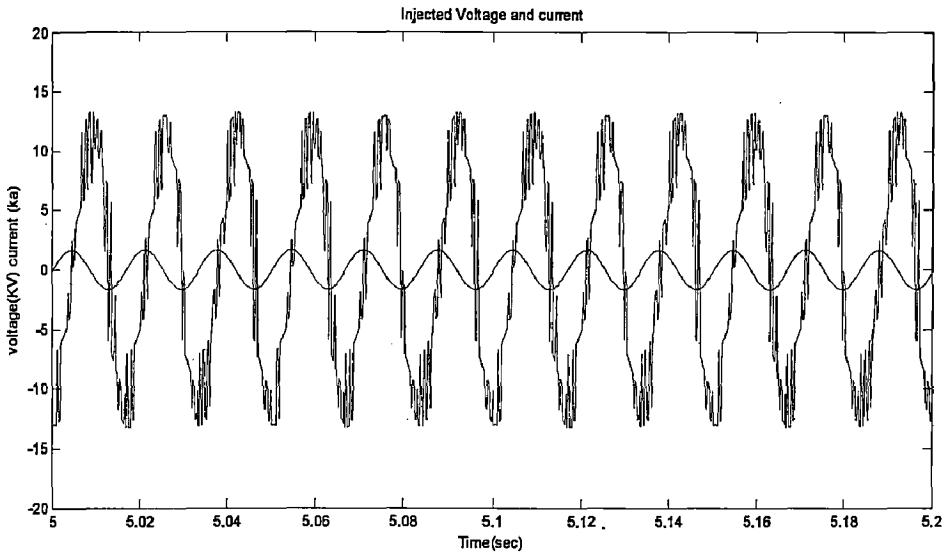

Figure 4.11 injected voltage and line current

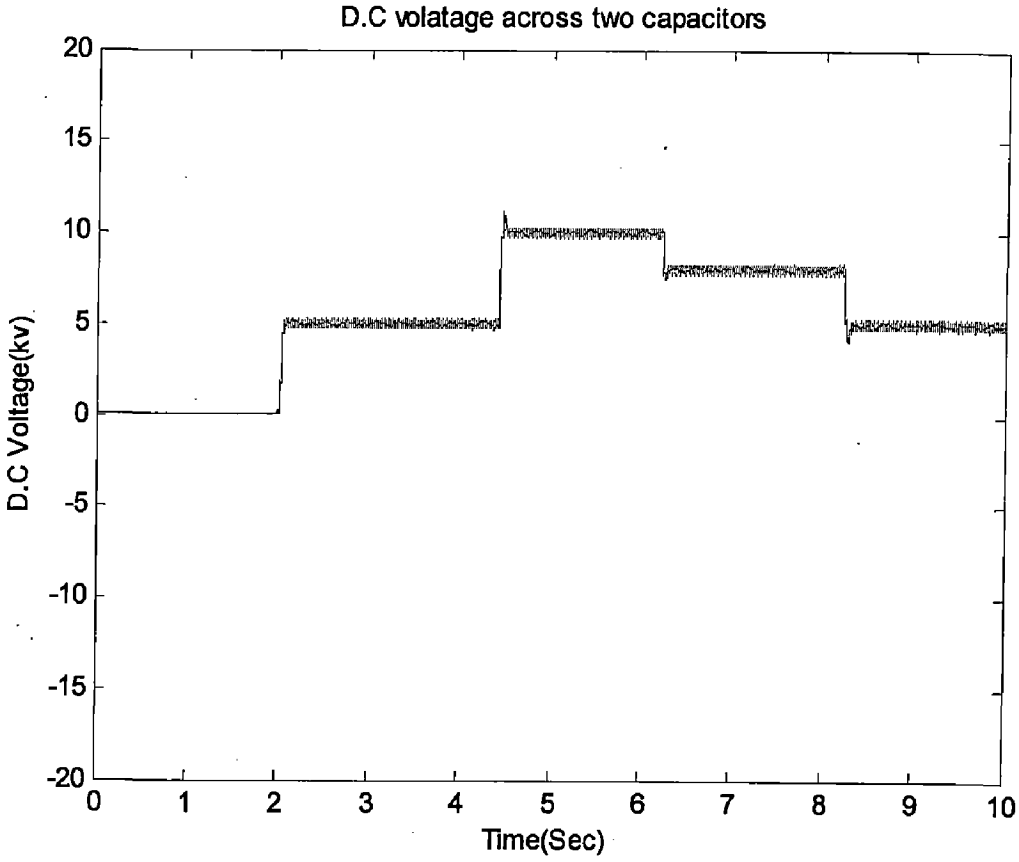

Figure 4.12: D.C voltage across two capacitors

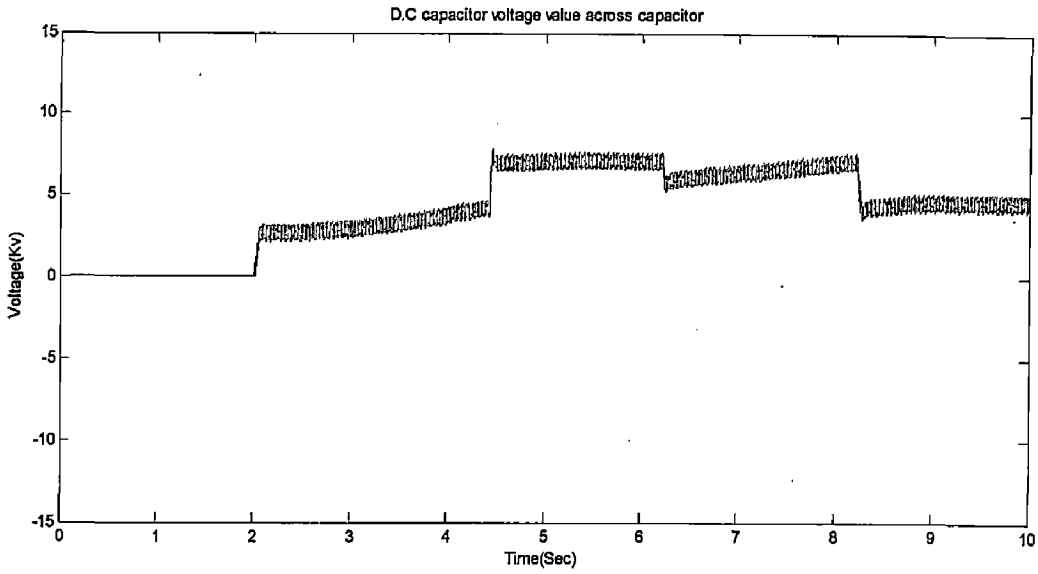

Figure 4.13: D.C voltage across one of the two capacitors of diode-clamped inverter

The simulation results have shown from Fig 4.10 to 4.13. Fig 4.10 shows the variation of power flow in the transmission line and Fig 4.11 shows the injected voltage in quadrature with the line current. Fig 4.12 and Fig 4.13 shows the variation of d.c voltage across the total capacitance and one of the capacitor of the diode-clamped inverter.

4.7 Conclusions:

In this chapter, the simulation of SSSC using diode-clamped inverter had presented. First, the basic operation of the diode clamped inverter (3-level and 5-level) had explained. 3-level diode clamped inverter stand-alone is simulated and the simulation result has shown. By observing the wave forms and control techniques we can observe that the control structure is difficult and the ripples in the d.c voltage across the capacitor. The variation of the real power has observed through the graphs and the injected voltage is in quadrature with the line current. Therefore, we can conclude that the simulation of SSSC using DCMLI is effective.

CHAPTER 5
COMPARISONS & CONCLUSIONS

5.1 Comparison of different configurations considered:

This chapter outlines the comparative analysis of all the configurations of SSSC based on steady state analysis carried out in this work. The performances of the SSSC has compared based on DC Bus voltage magnitude and its variations, physical structure, possible scheme for implementation, switching frequency, harmonic content.

5.1.1 Switching frequency and Harmonic content:

For the case of SSSC using 12-Pulse VSC, the harmonics of 11^{th} and 13^{th} harmonics are predominant and it had shown in frequency spectrum of output waveform in chapter 2.

For the case of SSSC using 48-pulse inverter the dominant harmonics are eliminated and the output voltage is pure sinusoidal as shown in the chapter 2 and the harmonic spectrum is also presented in the same chapter.

The switching frequency of Diode-clamped multilevel inverter is high. The switching frequency of the module is 540Hz. In multi-pulse inverter, the output voltage had obtained by using by the different connections of the transformers so there is no switching frequency in that module.

5.1.2 Comparison based on DC voltage:

In the case of 12 pulse and, 48 pulse VSC, the DC voltage can be controlled quite precisely around its reference set value. This is because, in the case of Multi-pulse VSC, the control technique is so simple, and capacitors are less.

On the other hand, in the case of DC MLI (Diode-clamped multi-level inverter), the control technique was complicated as explained in chapter 4 Fig4.8 and 4.9 ,and as the level of the inverter increases the capacitors are also more .

5.2 Conclusions:

The various configurations of SSSC's have simulated and the comparative analysis had presented. After analyzing the various configurations of SSSC's, which are discussed and simulated in the above chapters, it is concluded that, the compensation provided by the series inverter, and hence the amounts of real power variation in the line by the series inverter to the power system are same in both the cases by maintaining the DC Bus voltage constant.

It can be also concludes that the variation of power flow over the transmission line can be possible by using SSSC and it is verified through the simulation results. The output waveform of the 48-step inverter shows a nearly sinusoidal waveform. Both multi-level and multi-pulse inverters are simulated and the results are satisfactory in both cases. The control technique of the multi-pulse inverter is easy compared to the multi-level inverters and for higher ratings of the voltage levels, multi-level inverters are preferable as the generation of output voltage is easy compared to the multi-pulse inverters.

5.3 Scope for further work:

Some of the improvements of the present work and future direction for further studies are listed below.

- The system behavior for unbalanced fault on line or bus needs to be investigated the charge on the dc capacitor.
- The controller strategy can be suitably modified to facilitate power flow control. This controller must act in sympathy with increase in mechanical input.
- The S^3C and its control can be implemented in a multi-machine system. For that purpose, the stable zone of control operation must be determined first.
- The 48-step inverter and its model can be directly applied to construct an UPFC and its control system.
- SSSC using cascaded multi level inverter.
- Flying capacitor multi level inverter based SSSC.

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APPENDIX A

Test System

A.1 GENERATOR-SHAFT SYSTEM DATA:

The generator-shaft system data used for the studies presented in this thesis are taken from [IEEE'77]. These data are presented below.

A.1.1 Generator Data

The synchronous machine is rated 892.4 MVA at 26 kV with a system frequency of 60 Hz. The per unit values, given on the generator base, are:

$R_a = 0.0$ per unit, $X_a = 0.13$ per unit,

$x_d = 1.79$ per unit, $x'_d = 0.169$ per unit, $x''_d = 0.135$ per unit,

$x_q = 1.710$ per unit, $x'_q = 0.228$ per unit, $x''_q = 0.2$ per unit,

$T'_{do} = 4.3\,\text{sec}$, $T''_{do} = 0.032\,\text{sec}$, $T'_{qo} = 0.85\,\text{sec}$, $T''_{qo} = 0.05\,\text{sec}$

A.1.2 Mechanical System Data

The six-mass shaft system data are presented below. As indicated in Fig. 4.5 the shaft system contains a high-pressure (HP), an intermediate-pressure (IP) and two low-pressure (LPA and LPB) turbines as well as generator and exciter. The inertia and spring constants are listed in Table A.1.

Table A.1 Rotor inertia and spring constants

Mass	Inertia Constant (H)	Shaft section	Spring Constant pu Torque/Rad
HP	0.092897	HP-IP	19.303
IP	0.155589	IP-LPA	34.929
LPA	0.858670	LPA-LPB	52.038
LPB	0.884215	LPB-GEN	70.858
GEN	0.868495	GEN-EXC	2.822
EXC	0.0342165		

Resistance = 0.02 per unit on the generator base

Inductive reactance = 0.5 per unit on the generator base.

A.2 Transformer data:

The system contains two separate transformers. One of these transformers is connecting the generator with the transmission line, while the other one is the interfacing transformer between transmission system and SSSC

A.3 Sending-End Transformer:

Rated 892.4 MVA at 26/539 kV, Δ-y connected with leakage reactance of 0.14 per unit on the generator base.

A.4 Infinite bus data:

Infinite bus voltage is 477.8 kV and it is connected to the transmission line with a small series reactance of 0.06 per unit on the generator base.

APPENDIX B

SSSC using 12-pulse and 48-pulse inverter

The synchronous machine, transmission, receiving end data are given in the Appendix A

B.1 Interfacing Transformer

This is constructed from three single-phase transformer each of which is rated 200 MVA, 60/104 kV with leakage reactance of 0.1 per unit on its own base. The primary (SSSC) side is connected inΔ, while the secondary side is left open to be connected in series with the transmission line.

B.2 SSSC DATA

The SSSC contains two distinct, but interconnected sides – the dc and ac. The dc side contains a storage capacitor and the ac side contains transformers. These data are given below.

B.3 Dc Side Data

Capacitance of storage capacitor $C_{dc} = 2000\,\mu F$.

Turn-off resistance $R_{off} = 1\times10^{6}\ \Omega$, and turn-on resistance $R_{on} = 0.01\ \Omega$

B.3 PI controller for the dc capacitor controller:

Proportional gain 1

Integral time constant 0.002 s

B.4 Ac Side Data

The ac side transformers are single-phase three or two winding transformers. The three transformers that to one individual inverter are identical. Thus we list the data of only one transformer connected to each inverter.

Transformer connected to inverter 1

It is a two winding 100 MVA, 50/28.8675kV transformer with a leakage reactance of 0.1 per unit on its own base.

Transformer connected to inverter 2

It is a three winding transformer rated 100 MVA at 50/28.6205/6.526 kV with leakage reactance ($x_{l12} = x_{l13} = x_{l23}$) = 0.1 per unit on its own base.

Transformer connected to inverter 3

It is a three winding transformer rated 100 MVA at 50/27.8838/12.9409 kV with leakage reactance ($x_{l12} = x_{l13} = x_{l23}$) = 0.1 per unit on its own base.

Transformer connected to inverter 4
It is a three winding transformer rated 100 MVA at 50/26.6701/19.1348 kV with leakage reactance ($x_{l12} = x_{l13} = x_{l23}$) = 0.1 per unit on its own base.

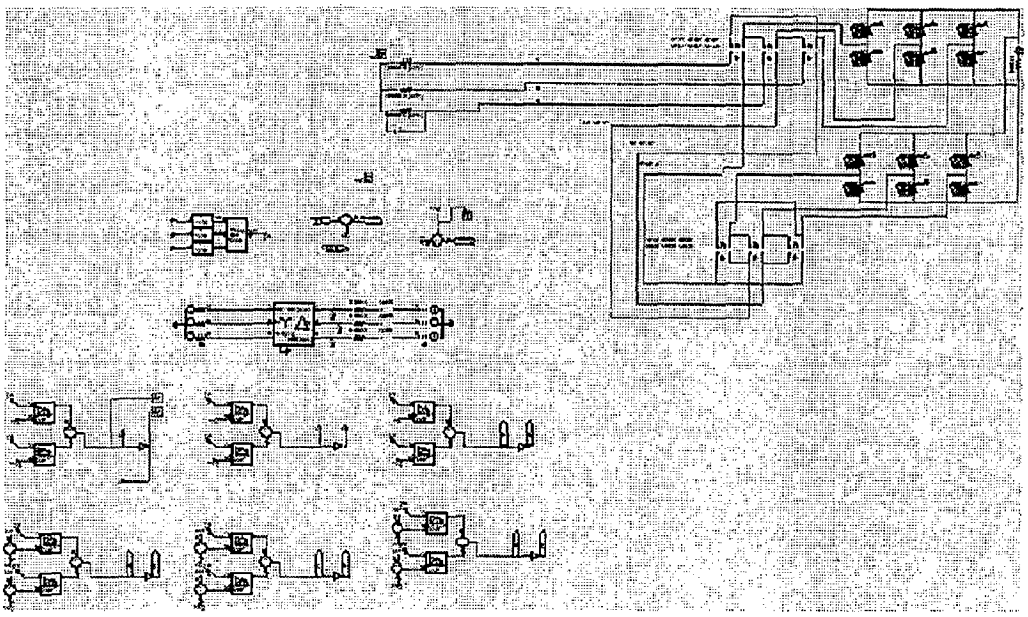
Transformer connected to inverter 5
It is a two winding 100 MVA, 50/50 kV transformer with a leakage reactance of 0.1 per unit on its own base.

Transformer connected to inverter 6
It is a three winding transformer rated 100 MVA at 50/49.5722/3.768 kV with leakage reactance ($x_{l12} = x_{l13} = x_{l23}$) = 0.1 per unit on its own base.

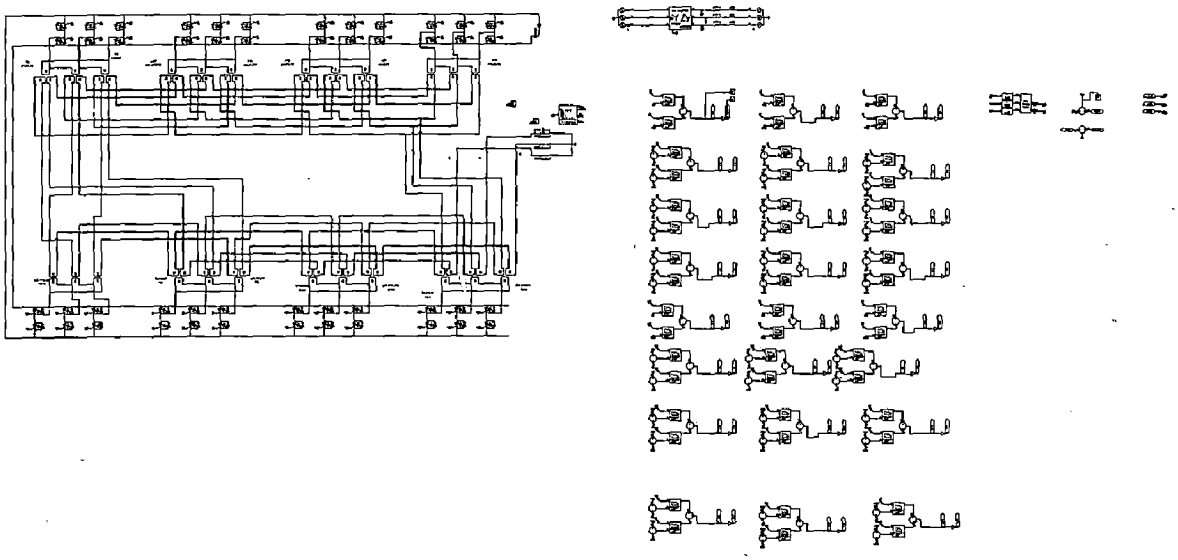
Transformer connected to inverter 7
It is a three winding transformer rated 100 MVA at 50/48.2963/7.4715 kV with leakage reactance ($x_{l12} = x_{l13} = x_{l23}$) = 0.1 per unit on its own base.

Transformer connected to inverter 8
It is a three winding transformer rated 100 MVA at 50/46.1939/11.047 kV with leakage reactance ($x_{l12} = x_{l13} = x_{l23}$) = 0.1 per unit on its own base.

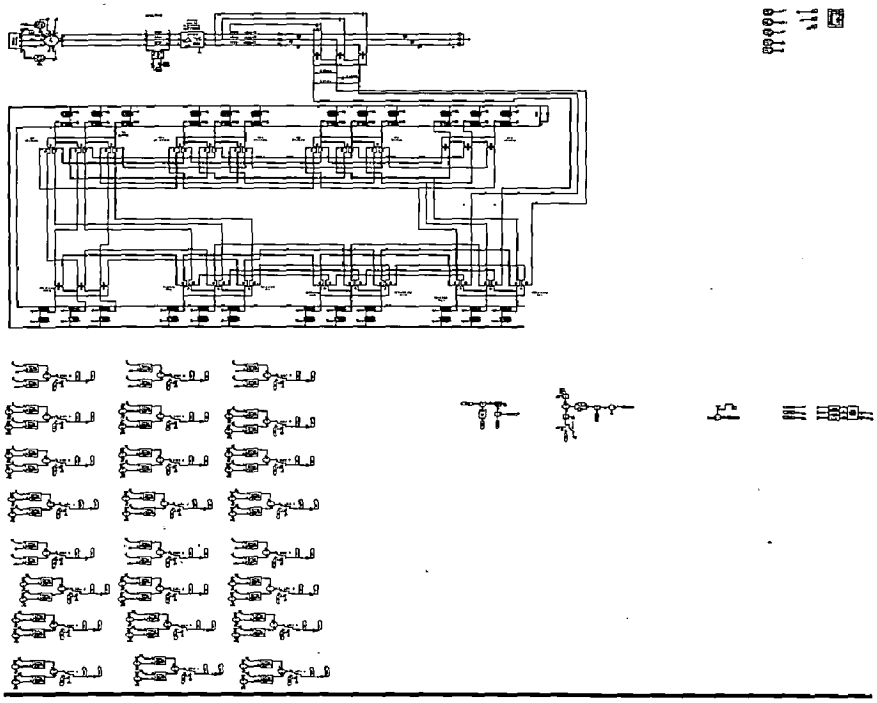
PSCAD VIEW OF 12 PULSE INVERTER:



PSCAD VIEW OF 48-PULSE INVERETR:



PSCAD View Of 48-pulse SSSC:



APPENDIX-C

SSSC using 3 level DC MLI modules.

The various parameters used for the simulation of the SSSC using 3 level DC MLI modules are given below. The test system values are given in appendix-1

Series inverter:
Time constant of the PI controller: 0.002
Proportional gain: 20

C.1 Pscad View of Diode-clamped inveter SSSC: