DESIGN OF 1.1mW 2.4GHZ CMOS LOW NOISE AMPLIFIER BASED ON 90nm TECHNOLOGY

A DISSERTATION

Submitted in partial fulfillment of the requirements for the award of the degree

of

MASTER OF TECHNOLOGY

in

ELECTRONICS AND COMMUNICATION ENGINEERING

(With Specialization in Semiconductor Devices and VLSI Technology)

By

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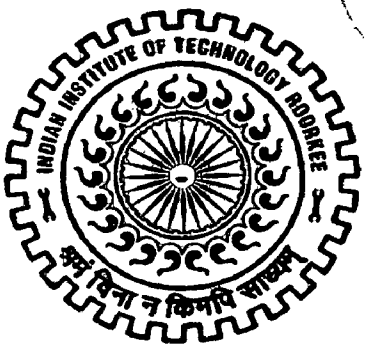

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CANDIDATE'S DECLARATION

I hereby declare that the work, which is presented in this dissertation report, entitled **"DESIGN OF 1.1mW 2.4HZ CMOS LOW NOISE AMPLIFIER BASED ON 90nm TECHNOLOGY"**, being submitted in partial fulfillment of the requirements for the award of the degree of **Master of Technology** in **Electronics and Communication Engineering** with specialization in **Semiconductor Devices & VLSI Technology**, in the Department of Electronics and Computer Engineering, Indian Institute of Technology, Roorkee is an authentic record of my own work carried out from July 2006 to June 2007, under guidance and supervision of **Dr. S. Dasgupta,** Assistant Professor, Department of Electronics and Computer Engineering, Indian Institute of Technology, Roorkee.

The results embodied in this dissertation have not submitted for the award of any other Degree or Diploma.

Date: 28-06-07

Place: Roorkee

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K. SHIVASHANKER REDDY

CERTIFICATE

This is to certify that the statement made by the candidate is correct to the best of my knowledge and belief.

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Abstract

Wireless and mobile are two of the fastest growing microelectronics applications, and have an enormous impact on our daily lives. The design of low cost, low power transceivers has gained substantial significance due to these applications. This work presents a design methodology for CMOS LNA applicable for low power applications.

To demonstrate design methodology a narrow-band source degenerated cascode LNA is designed and simulated in a standard 90nm CMOS process to operate in the 2.4 GHZ band. The LNA achieves a voltage gain of 20.6dB, Noise figure of 2.87dB and consuming 1.1mW power from 1V supply voltage. Simulation study has been done using Micro Wave Office.

The main contributions of this work include: 1) the introduction of a design methodology for power-efficient source degenerated LNA; 2) the collection of design graphs to facilitate the exploration of tradeoffs between LNA performance and power consumption.

CONTENTS

Chapter1

Introduction

1.1 Introduction

Wireless and mobile are two of the fastest growing microelectronics applications, and have an enormous impact on our daily lives. The design of low cost, low voltage, low power transceivers has gained substantial significance due to these applications [1]. The major component in any receiver is the low noise amplifier (LNA). The LNA needs to provide an input match as well as amplify the signal with out adding too much noise while consuming minimal power.

Traditionally, radio frequency integrated circuits (RFIC'S) were implemented in GaAs or in SiGe bipolar technologies, because of their relatively high unity gain cutoff frequency (f_T) and their low noise. However, as the minimum feature sizes of the CMOS devices decreases, the unity gain cutoff frequency (f_T) of the transistors continue to improve, to the point where they can be comparable to those of the GaAs and SiGe processes.

Since the CMOS technology is employed for the digital transceiver back-end, it is attractive to implement the RF front-end also in CMOS, with the goal to integrate all parts of the receiver on a single chip to reduce cost and time to market. In the recent past, numerous CMOS LNA circuits have been presented and have demonstrated good performance [2]-[5].

1.2 Thesis Organization

In this report, the design methodology and design of low power CMOS LNA is documented.

Chapter2 Presents the background information about two-port networks that is useful in the design of low noise amplifiers.Chapter3 Presents about the different noise sources

present in the MOSFET.Chapter4 discusses different LNA topologies.Chaper5 presents a design methodology for LNA for low power applications.Chapter6 presents design and Simulation results of 2.4 GHZ LNA. In chapter7 conclusions are drawn and scope for future work is presented.

Chapter 2

Issues in LNA Design

This chapter discusses about performance measures of the two-port network such as input matching, noise and linearity that are important in the design of LNA.

2.1 Impedance Matching

A network with signal source driving a load is depicted in fig2.1.Where Z_S and Z_L are the source and load impedances, respectively.

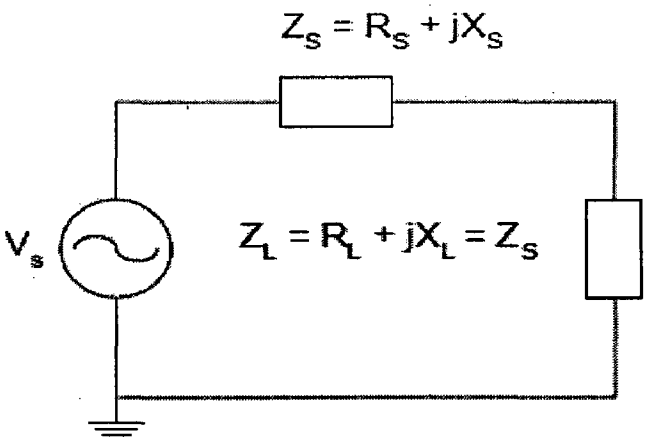


Figure 2.1 A network with a source driving a load.

Impedance matching is important in LNA design because often times the system Performance can be strongly affected by the quality of the termination. For instance, the frequency response of the antenna filter that precedes the LNA will deviate from its normal operation if there are reflections from the LNA back to the filter. Furthermore, undesirable reflections from the LNA back to the antenna must also be avoided. An impedance is matched when $Z_S = Z_L$.

There is a subtle difference between impedance matching and power matching. As stated, earlier the condition for impedance matching occurs when the load impedance is equal to the characteristic impedance. However, the condition for power matching occurs when the load impedance is the complex conjugate of the Characteristic impedance. When the impedances are real, the conditions for power matching and impedance matching are the same.

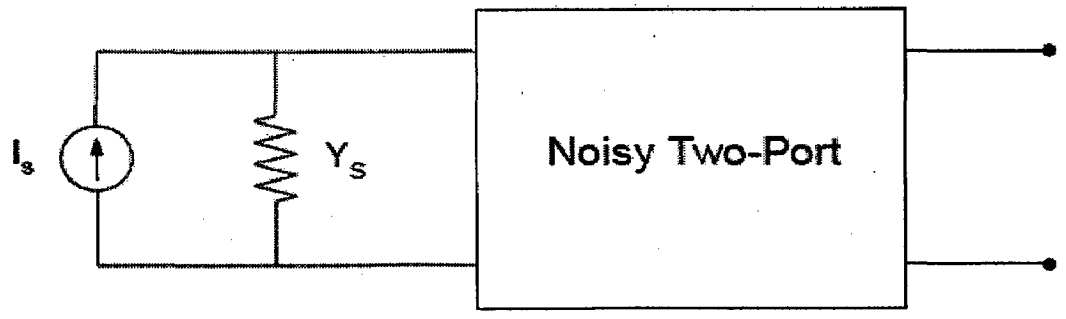
2.2 Two-Port Noise Theory

In order to design a circuit for low noise, it is useful to determine the condition under which noise can be minimized. This condition is then used to relate noise performance to CMOS design parameters. For the analysis of noise in two-port systems, consider a noisy two-port network driven by a noisy source that as an admittance Y_s and an equivalent shunt noise current $\overline{i_s}$ as shown in Fig. 2.2(a).

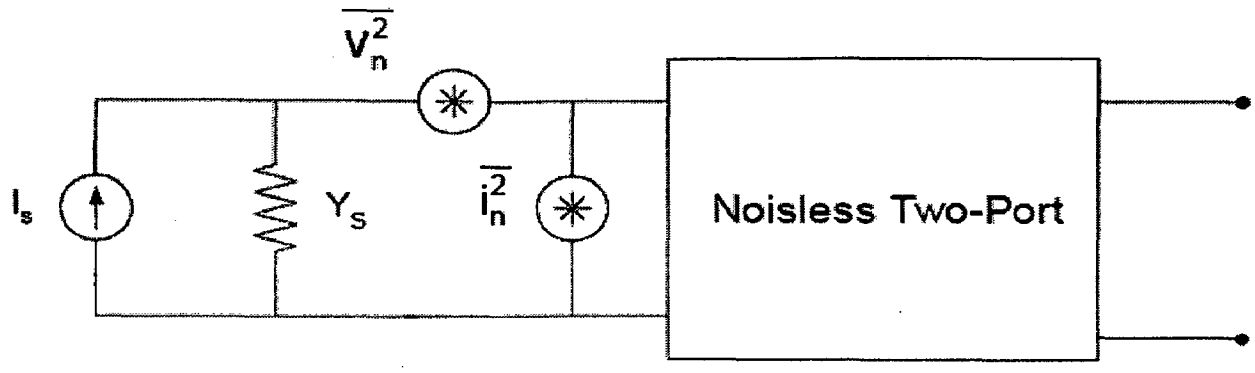
The noise factor (F) is defined as:

$$F = \frac{\text{total output noise power}}{\text{output noise due to input source}} \tag{2.1}$$

To simplify analysis, the noise of a two-port network can be modeled as a noise voltage ($\overline{v_n}$) and a noise current ($\overline{i_n}$) at the input as shown in Fig2.2 (b).



(a)



(b)

Figure 2.2 (a) Noisy two-ports driven by noise source, (b) equivalent noise model

All the noise sources are now input referred as in figure 2.2b and the output power contributions from each term is proportional to it's short-circuit current at the input. As a result, we can now calculate the noise factor by calculating the total short-circuit mean square input noise current, and divide that total by the short-circuit mean-square noise current generated from the input source. The expression then becomes [6]:

$$F = \frac{\overline{i_s^2} + \left|\overline{i_n^2} + Y_s \overline{v_n^2}\right|^2}{\overline{i_s^2}} \tag{2.2}$$

There is a correlation between the current noise generator and the voltage noise generator. We can write i_n as:

$$i_n = i_c + i_u \tag{2.3}$$

Where i_c is the part of i_n that is correlated with v_n, while i_u is the part of i_n that is uncorrelated with v_n. Since i_c is correlated with v_n, it can be written as:

$$i_c = Y_c v_n \tag{2.4}$$

The constant Y_c is known as the correlation admittance Putting the equation (2.3) and equation (2.4) into the equation (2.2), we get a modified expression for the noise factor

$$F = 1 + \frac{\overline{i_u^2} + |Y_c + Y_s|^2 \overline{v_n^2}}{\overline{i_s^2}} \tag{2.5}$$

The expression above contains three independent noise sources. We can then define

$$R_n = \frac{v_n^2}{4KT\Delta f} \tag{2.6}$$

$$G_u = \frac{i_u^2}{4KT\Delta f} \tag{2.7}$$

$$G_s = \frac{i_s^2}{4KT\Delta f} \tag{2.8}$$

Where Δf is noise bandwidth is in hertz, K is Boltzman's constant T is the absolute temperature in Kelvins.Using the equation (2.6)-(2.8), we can then write the noise factor in terms of noise admittances and impedances as followed:

$$F = 1 + \frac{G_u + |Y_c + Y_s|^2 R_n}{G_s} \tag{2.9}$$

$$F = 1 + \frac{G_u + \left[(G_c + G_s)^2 + (B_c + B_s)^2\right] R_n}{G_s} \tag{2.10}$$

At this point, the optimal admittance can be found by taking the first derivatives of the equation above with respect to the source conductance and source susceptance and turning it into zero. This yield:

$$B_c = -B_s = B_{opt} \tag{2.11}$$

$$G_s = \sqrt{\frac{G_u}{R_n} + G_c^2} = G_{opt} \tag{2.12}$$

Substituting equations (2.11) and (2.12) into (2.10) gives the following result for the minimum noise factor:

$$F_{\min} = 1 + 2R_n(G_{opt} + G_c) \tag{2.13}$$

We can express noise factor in terms of $F_{\min}$ as:

$$F = F_{\min} + \frac{R_n}{G_s}\left[(G_s - G_{opt})^2 + (B_s + B_{opt})^2\right] \tag{2.14}$$

The above analysis shows that a minimum noise figure exists for optimal source impedance, but that the source impedance that optimizes for noise is often not the same as the impedance that achieves maximum power transfer.

2.3 Linearity [7, 8]

Ideally, two-port networks are linear, and in many analyses this assumption is made because the input signal is small enough such that the non-linear effects of the two-port network can be ignored. However, in LNA design, linearity is a key issue because the LNA must be able to maintain linear operation even in the presence of large input signals.

2.3.1 Harmonic Distortion

The input V_i and output V_o of a two-port network can be related by a power series:

$$V_o = a_1 V_i + a_2 V_i^2 + a_3 V_i^3 + \ldots\ldots \tag{2.15}$$

Where a_1, a_2, a_3 are constants. Now, if a sine wave drive is applied to the input, given as

$$V_i(t) = V\cos(\omega_1 t) \tag{2.16}$$

Where V_1 and ω_1 are the amplitude and frequency, respectively, then the output is equal to

$$V_o(t) = a_1 V\cos(\omega_1 t) + a_2\frac{V^2}{2}[\cos(2\omega_1 t) + 1] + a_3\frac{V^3}{4}[\cos(3\omega_1 t) + 3\cos(\omega_1 t)] + \ldots.. \tag{2.17}$$

The first term in (2.17) is the linear term, and is the ideal output if the two-port network is completely linear. Other terms in (2.17) are due to non-linear ties, and they cause a DC shift as well as distortion at frequencies $2\omega_1$, $3\omega_1$, and higher harmonics, which result in either gain compression or gain expansion.

2.3.2 1 dB Compression Point

Third order term in the equation can either cause gain compression or gain expansion depending on its sign. If we assume that the sign between a_1 and a_3 are different, then gain compression will occur, and the 1 dB compression point can be measured. It can be expressed as

$$20\log\left[1+\frac{3a_3V^2}{4a_1}\right]=-1dB \tag{2.18}$$

Solving for V gives

$$p_{-1dB}=\sqrt{\frac{4}{3}\left|\frac{a_1}{a_3}\right|}\sqrt{0.11} \tag{2.19}$$

The 1 dB compression point (P-1dB) is a measure of the power of the input signal such that it causes the 3rd order non-linearity to decrease the linear gain by 1 dB.

Chapter 3

MOSFET Noise Sources

The MOS transistors are the main source of noise in RFICs. The main sources of noise in a MOS transistor are

1. Thermal noise
2. Induced gate noise

3.1 Thermal Noise

Thermal noise is due to the random thermal motion of the carriers in the channel. Thermal noise is also known as white noise because of its power spectral density (PSD) holds a constant value up to very high frequency [9]-[10]. Thermal noise is commonly modeled as current source across the drain and the source in shunt with the Trans conductor of the transistor.

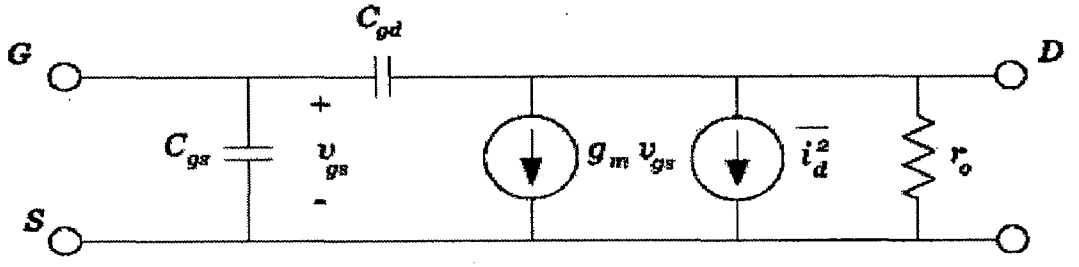


Figure3.1 Thermal noise small signal circuit model

Thermal noise power spectral density (PSD) is given by

$$\overline{i_{nd}}^2 = 4KT\gamma g_{d0} \tag{3.1}$$

Where γ is the bias dependent parameter and g_{d0} is the zero-V_{DS} drain-source conductance for long channel transistors, $\gamma = 2/3$ in the saturation region, and $\gamma = 1$ in the linear region. For short channel transistors, hot carrier effects may cause γ to be as high as 2 or 3[11].

3.2 Induced Gate Noise

In addition to the channel thermal noise, the thermal agitation of channel charge has another important consequence: induced gate noise. Although this noise is negligible at low frequencies, it can dominate at radio frequencies. Vander Ziel[9] has shown that the induced gate noise can be expressed as

$$\overline{i_{ng}^{\ 2}} = 4KT\delta g_g \Delta f \tag{3.2}$$

Where the parameter g_g is

$$g_g = \omega^2 \frac{C_{gs}^{\ 2}}{5g_{d0}} \tag{3.3}$$

Where the parameter δ is equal to 4/3[9] in long channel devices. Since the thermal channel noise and induced gate noise stem from the same physical phenomenon, assumes that the relation $\delta = 2\gamma$ continues to hold for short channel devices.

It was mentioned earlier that the gate noise is related to the drain noise. In fact, it is partially correlated to the drain noise, with a correlation coefficient c, stated as

$$c = \frac{\overline{i_g i_d^{\ *}}}{\sqrt{i_g^{\ 2} i_d^{\ 2}}} \tag{3.4}$$

The value for c is given as 0.395j for long channel devices [9]. The purely capacitive nature of the correlation coefficient is due to the fact that the coupling between the gate noise and drain noise is through the gate capacitance.

3.3 MOSFET Two-Port Noise Parameters

Viewing the MOSFET as a two-port network, with the gate and source forming a port and the drain and source forming another, it is useful to express $F_{\min}$, B_{opt}, G_{opt} and R_n in terms of MOSFET device parameters [6].

$$F_{\min} = 1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_T} \sqrt{\gamma\delta(1-|c|^2)} \tag{3.5}$$

$$R_n = \frac{\gamma g_{d0}}{g_m^2} \tag{3.6}$$

$$G_{opt} = \alpha\omega C_{gs}\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)} \tag{3.7}$$

$$B_{opt} = -\omega C_{gs}\left[1-\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right] \tag{3.8}$$

Where α is given as

$$\alpha = \frac{g_m}{g_{d0}} \tag{3.9}$$

α is unity for long channel devices and decreases as channel length shrink. We can make various observations from the derivations just completed

1. The noise figure degrades at higher frequency of operation.
2. The noise figure improves with technology scaling due to increase in cutoff Frequency.
3. The minimum noise figure is a function of normalized frequency of operation.
4. The minimum noise figure is independent of width of the device.
5. R_n is inversely proportional to the width of the device.
6. B_{opt}, G_{opt} are proportional to the width of the device.

The above presented method is known as classical noise matching (CNM). Limitation of the classical noise matching (CNM) is power is not considered at all in this optimization technique.

Chapter 4

Different Topologies of Low Noise Amplifier

As mentioned in the chapter 2 impedance matching is very important in LNA designs. In most cases, the source impedance of the LNA is 50Ω is wireless system. Since the input impedance of the MOS transistor is almost purely capacitive, providing a good match to the source without degrading noise performance is a challenge. In this section, we will investigate a number of circuit topologies that can be used of the task and discuss their properties.

4.1 Resistive Termination

This is the most straightforward approach to achieve the broadband 50Ω matching at the input as shown in figure. The 50Ω-resistor (R_1) is placed across the input terminal of the LNA and hence providing a broadband input matching [6].

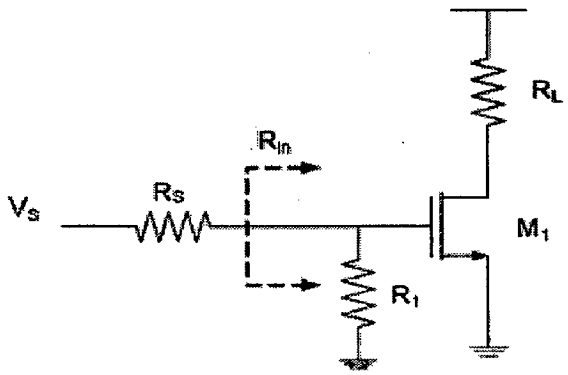


Figure 4.1 Resistive termination matching

The bandwidth of this matching topology is determined by the input capacitance of the transistor M_1 and can be very high. However, the resistor R_1 adds its own thermal noise to the circuit as well as attenuates the incoming signal by a factor of two before it hits the gate of the transistor. These two effects results in an unacceptably high noise factor of the circuit and hence is not practical in most applications.

4.2 Shunt-Series Feedback

The other method used for getting a good input matching is the shunt-series feedback amplifier as shown in figure 4.2. Unlike in the resistive termination case, it does not attenuate the signal by a noisy attenuator before reaching the gate of the amplifying device and hence the noise figure is expected to be much higher. However, the feedback resistor continues to generate thermal noise of its own. These results in the relatively high noise figure[6].

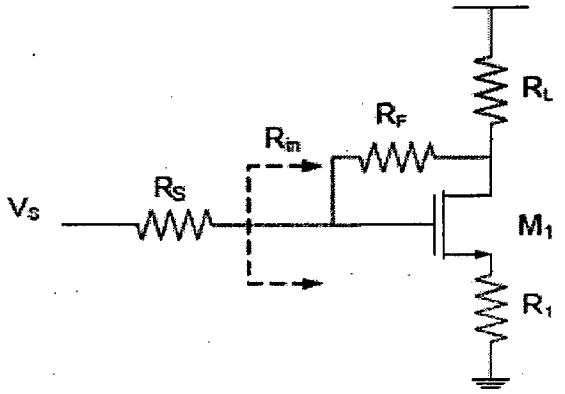


Figure 4.2 Shunt-series feedback matching

4.3 Common-Gate LNA

Another method for realizing a resistive input matching is to use a common-gate configuration. As can be seen in the figure 4.3, the source terminal is used as an input terminal. Since the impedance looking into source of is $1/g_m$, it can be set by proper device sizing and adjusting the bias current of the circuit.

Neglecting gate and flicker noises and assuming a perfect match, we can express the lower bound of the noise figure for the amplifier that uses this matching technique as follow:

$$F \geq 1 + \frac{\gamma}{\alpha} \tag{4.1}$$

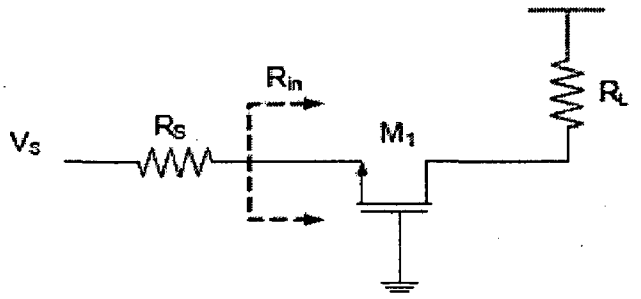


Figure 4.3 Common-gate input matching

Numerical value for the lower bound expressed above is about 2.2dB for long-channel devices and 4.8dB for short channel devices[6],[12].

All the preceding topologies suffer noise figure degradation from the presence of noisy resistance in the signal path (including channel resistance, as in the case of common – gate amplifier).

4.4 Inductive Source Degeneration

4.4.1 Introduction

Unlike the other previously mentioned techniques, this matching topology provides a perfect match without adding any noise to the system or giving any restrictions on the device g_m. It uses an inductor as a source degeneration device and has another inductor connecting to the gate as shown in figure 4.4.

Using the small signal analysis and neglecting C_{gd} of M1, the impedance looking through the gate inductor can be expressed as:

$$Z_{in} = \frac{1}{j\omega C_{gs}} + j\omega(L_s + L_g) + \frac{L_s g_m}{C_{gs}} \qquad (4.2)$$

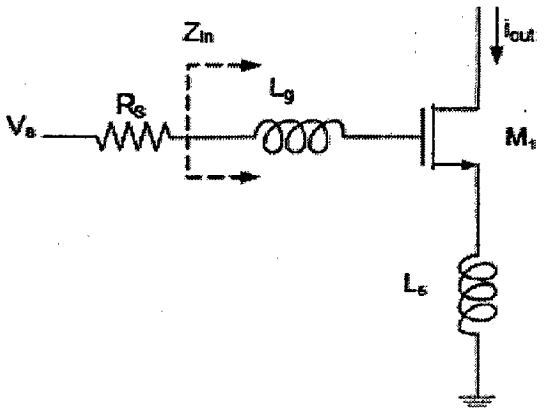


Figure 4.4 Inductive source degeneration matching

At the resonance frequency where the inductor impedance and the capacitor impedance are canceled out, the input impedance is then just the last term in the equation

$$Z_{in}(\omega_o) = \frac{L_s g_m}{C_{gs}} = \omega_T L_s \tag{4.3}$$

Where $\omega_T = \frac{g_m}{C_{gs}}$ and (4.4)

$$\omega_o = \frac{1}{\sqrt{(L_s + L_g)C_{gs}}} \tag{4.5}$$

Since all the inductors are reactive, they do not add any noise into the circuit. In fact, the LC resonating mechanism improves noise and gain performance of the amplifier. Starting from the equivalent model of the input matching (figure 4.5), the quality factor of the circuit given by

$$Q = \frac{1}{\omega_o C_{gs}(\mathrm{R}_{eq} + R_s)} \tag{4.6}$$

Where $\mathrm{R}_{eq} = \omega_T L_s$

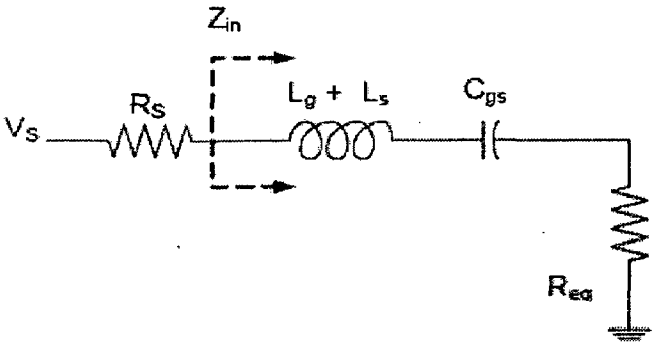


Figure 4.5 Equivalent Circuit at input for Inductive source degeneration matching

At the resonance, the voltage amplitude across C_{gs} is Q times the voltage across the input terminal from the source given matched condition. This effectively increases the transconductance of the input transistor by a factor of Q.

$$G_m = g_m Q \tag{4.7}$$

Substituting equation 4.6 in to equation 4.7 we get

$$G_m = g_m \frac{1}{(R_{eq} + R_s)\omega_o C_{gs}} \tag{4.8}$$

$$G_m = \left(\frac{\omega_T}{\omega_o}\right)\frac{1}{(R_{eq} + R_s)} \tag{4.9}$$

From above equation we can see that effective transconductance G_m is independent of g_m of the device.

Device dimension

In the third chapter we have derived the two port noise parameters of the MOSFET. The two port noise parameter may form a basis for selection of device dimension. But problem with classical noise matching (CNM) is that it won't take power consumption in to account. Hence, even though the noise figure would correspond very closely to F_{min}, the power consumed would be unacceptably high for virtually any application. Since power consumption is an important practical constraint, the most generally useful noise optimization technique must consider power a priori.

4.4.2 Power –Constrained Noise Optimization (PCNO)

To develop desired noise optimization technique, we must express noise figure in a way that takes power consumption explicitly in to account. We start with the general expression for noise figure as given by classical noise theory [6], [13].

$$F = F_{\min} + \frac{R_n}{G_s}\left[(G_s - G_{opt})^2 + (B_s + B_{opt})^2\right] \tag{4.10}$$

Our goal here is to reformulate the given expression in terms of power consumption. After deriving such an equation, we will minimize it subject to the constraints of fixed power and then solve for the width of the transistor that corresponds to this optimum condition.

Let us assume that the source susceptance B_s is sufficiently close to the B_{opt}, so that we may neglect the difference between the two. The expression now becomes

$$F = F_{\min} + \frac{R_n}{G_s}\left[(G_s - G_{opt})^2\right] \tag{4.11}$$

The expression for G_{opt} is given by

$$G_{opt} = \alpha\omega C_{gs}\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)} \tag{4.12}$$

$$\frac{G_{opt}}{\omega C_{gs}} = \alpha\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)} = Q_{opt} \tag{4.13}$$

Defining a quality factor Q_S in which G_{opt} is replaced by G_s, the actual source conductance

$$Q_S = \frac{1}{\omega C_{gs} R_s} \tag{4.14}$$

Re-expressing the noise figure expression

$$F = F_{\min} + \left[\frac{\gamma}{\alpha g_m R_s}\right]\left[1 - \frac{Q_{opt}}{Q_S}\right]^2 \tag{4.15}$$

The parameters α, g_m, Q_{opt} and Q_S are linked to power dissipation . We need to rewrite these terms in terms of power. To do so, first we shall recall that a simple expression of drain current is

$$I_D = WLc_{ox}v_{sat}E_{sat}\frac{\rho^2}{1+\rho^2} \tag{4.16}$$

Where $v_{sat} = \frac{\mu_n}{2}E_{sat}$, $\rho = \frac{V_{GS}-V_{TH}}{LE_{sat}}$

The power dissipation can in turn be written as:

$$P_D = V_{DD}I_D = V_{DD}WLc_{ox}v_{sat}E_{sat}\frac{\rho^2}{1+\rho^2} \tag{4.17}$$

The trans conductance can be written as:

$$g_m = \left[\frac{1+\rho/2}{(1+\rho)^2}\right]\left[\frac{\mu_n c_{ox}W(V_{GS}-V_{TH})}{L}\right] = \alpha\left[\frac{\mu_n c_{ox}W(V_{GS}-V_{TH})}{L}\right] = \alpha g_{do} \tag{4.18}$$

Further Q_S is a function of C_{gs}, which in turn is a function of device width. Equation 4.16 can be solved for width of the device. Resulting expression substituted in to the equation for Q_S (4.14) we will get:

$$Q_S = \frac{P_o}{P_D}\frac{\rho^2}{1+\rho} \tag{4.19}$$

Where $$P_o = \frac{3}{2}\frac{V_{DD}v_{sat}E_{sat}}{\omega R_s} \tag{4.20}$$

The noise figure can now be expressed in terms of ρ and P_D. Minimizing the resulting equation is complex enough that it is best solved graphically in the general case if an exact answer is desired. The minimum noise figure occurs when

$$\rho^2 = \frac{P_D}{P_o}\sqrt{\frac{\delta}{5\gamma}(1-|c|)^2}\left[1+\sqrt{\frac{7}{4}}\right] \tag{4.21}$$

Substituting equation in to equation yields the value of Q_S, that leads to the power constrained noise figure:

$$Q_{Sp} = |c|\sqrt{\frac{5\gamma}{\delta}}\left[1+\sqrt{1+\frac{3}{|c|^2}\left(1+\frac{\delta}{5\gamma}\right)}\right] \tag{4.22}$$

In the above equation $|c|$ value is equal to 0.39(9). Value of Q_{Sp} is sensitive to the ratio of δ to γ. Although the individual values may change the ratio may vary less. More optimum value of Q_{Sp} has been found to be 4.

Once Q_{Sp} has been determined, it is a simple matter to provide, at last, an expression for the width of the optimum device:

$$\frac{3}{2}\frac{1}{\omega L C_{ox} R_s Q_{Sp}} \tag{4.23}$$

The minimum noise figure in this case is given as:

$$F_{\min p} \approx 1+2.4\frac{\gamma}{\alpha}\left[\frac{\omega}{\omega_T}\right] \tag{4.24}$$

Comparing the above equation with the absolute minimum possible, given by

$$F_{\min} = 1+\frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{\gamma\delta(1-|c|^2)} \tag{4.25}$$

For typical values of γ, δ (2,4) above equation reduces to

$$F_{\min} = 1+2.3\frac{\omega}{\omega_T} \tag{4.26}$$

Comparison of equations 4.24 and 4.26 are shown in table 4.1 for typical values of γ, δ, α (2,4,0.85) [6].

Table 4.1 Estimated $F_{\min}$ and $F_{\min p}$

$\frac{\omega_T}{\omega}$	$F_{\min}$ (dB)	$F_{\min p}$ (dB)
20	0.5	1.1
15	0.6	1.4
10	0.9	1.9
5	1.6	3.3

From the table 4.1we can see that the difference between $F_{\min}$ and $F_{\min p}$ is in between o.5dB and 1.5dB but still excellent noise figures are still possible.

4.4.3 Design Steps for Common Source LNA using PCNO Technique

1. Selection of inductor L_s is fairly arbitrary but is ultimately limited on the maximum size of inductance allowed by the technology, which is typically about 10nH.
2. Selection of L_g :

   we know that $Q_{Sp} = \frac{(L_s + L_g)\omega}{R_s}$. Optimal value of Q_{Sp} is given as 4.

   Where ω is operating frequency and R_s=50ohms.
3. Sizing of the device:

   From the equation $W_{opt} = \frac{3}{2}\frac{1}{\omega L c_{ox} R_s Q_{Sp}}$ we can find the width of the device.
4. Calculate value of g_m from

   $$g_m = \omega_T C_{gs}$$
5. Bias current:

   Find the value of $V_{GS} - V_{TH}$ from

   $$V_{GS} - V_{TH} = \frac{g_m L}{\mu_n c_{ox} W}$$

   $$I_D = \frac{1}{2} g_m (V_{GS} - V_{TH})$$

From above values we can design the common source LNA.

4.4.4 Advantages of Cascode Stage

The cascode amplifier consists of an input transistor $M1$ and a cascode transistor $M2$ with a gate bias voltage V_B. Compared to the cascode amplifier, the common-source amplifier suffers from the following shortcomings.

1) Poor isolation between input and output, due to the gate-to-drain parasitic capacitance C_{gd} increases the chance of instability significantly.

2) As CMOS technology scales, the MOSFET output resistance r_o decreases, causing noticeable performance degradation. For a common-source amplifier, r_o appears in parallel with the load impedance in small-signal operation, which reduces the output impedance, and lowers the gain of the LNA. A possible solution is to increase the gate length L, which results in a degradation of NF.

To alleviate the shortcomings of the common-source topology, the cascode topology is often used. The addition of the cascode device reduces the effect of the C_{gd} of M_1 by presenting a low impedance node at the drain of M_1, improving stability. The cascode device also performs impedance transformation so that the output impedance of the amplifier is improved by a factor approximately equal to the intrinsic gain of the cascode device.

One shortcoming of the cascode topology is that the extra transistor consumes voltage headroom. As a result, the load should not consume large voltage headroom. An inductive load L_d , as opposed to a resistive load, is preferred. An inductive load has the added benefit of increasing the gain by resonating with the capacitances associated with the output node and also improving frequency selectivity.

4.4.5 Design Example

To examine the superior performance of inductive source degenerative LNA over common gate LNA a narrowband LNA design is designed to operate at a frequency of 2.4GHZ using both common gate and cascode topologies.

Both circuits have been simulated using BSIM4 [14] 0.6 micron technology for which threshold voltage is 0.67V.

Table 4.2 Comparison between CGLNA and Cascode LNA

parameter	CG LNA	Cascode LNA
Noise figure	3.45dB	1.876dB
Gain	15.6dB(voltage gain)	13.242dB(power gain)
Bias current	10mA	10mA
Supply voltage	1.5v	2.5v
Operating frequency	2.4GHZ	2.4GHZ

From the table 4.2 and fig 4.6 we can see that cascode LNA is giving far better performance than common gate LNA in terms of noise figure. Component values for cascode LNA are given in the table 4.3

Table 4.3 Component values for Cascode LNA

W_1/L_1, W_2/L_2 (in microns)	330/0.6
Bias voltage(V)	1V
Supply voltage (V)	2.5
L_s(nH)	1
L_g(nH)	12
L_d (nH)	5
C_{tune} (fF)	700

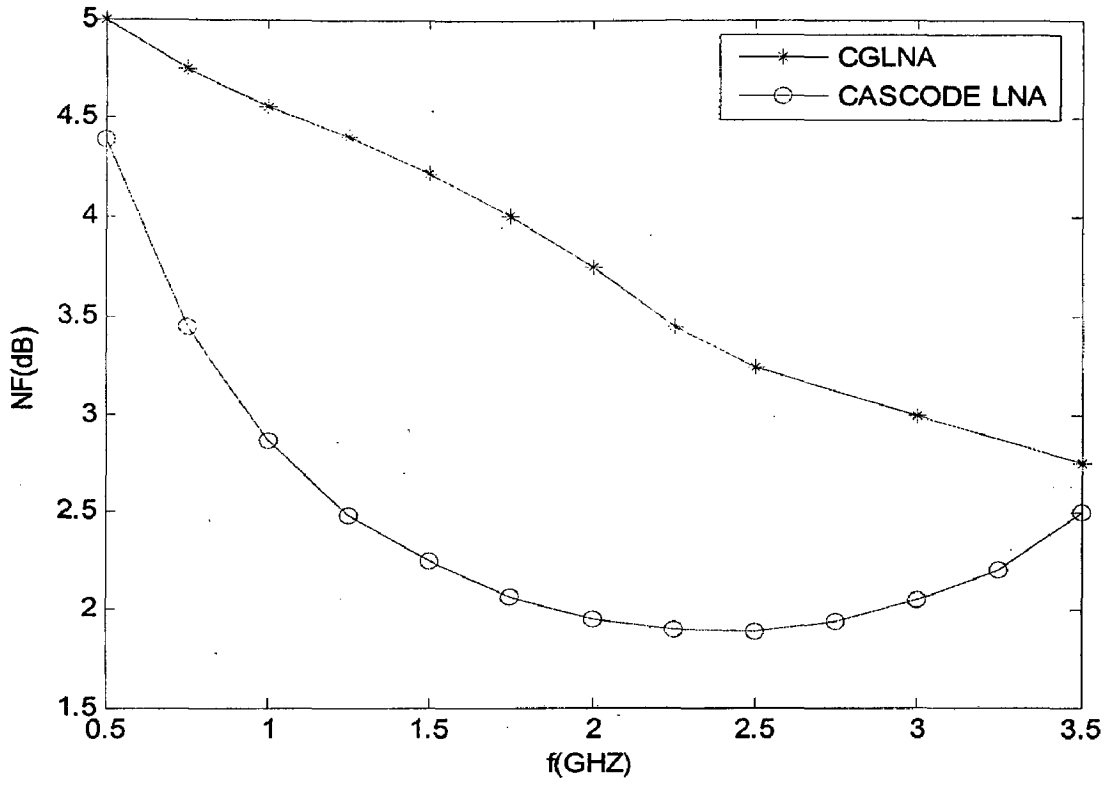


Figure 4.6 Frequency vs noise figure of Cascode LNA and CGLNA

4.4.6 Limitations of PCNO Technique

The techniques is based on first finding an optimal gate width, then biasing the device with the amount of drain current allowed by the power constraint. In sub-mW designs, the large optimal gate width combined with a small drain current often force the device to be biased in the sub threshold region. In sub threshold region the value of ω_T is very less and device may not work in the desired frequency of operation. So we need to use other method such that it can be used for low power applications.

Chapter 5

Design Methodology for Low Power Applications

In this chapter a design methodology has been developed for LNA for low power applications. This chapter describes biasing and the sizing of the device, the two fundamental steps in the LNA design for low voltage applications. All the characteristics have been plotted for BSIM4 90nm n type MOSFET in AWR design environment using MICROWAVE OFFICE.

5.1 Device Parameters

5.1.1Biasing

Performance of any circuit strongly depends up on the biasing of the device and that proper biasing involves knowledge of device characteristics.

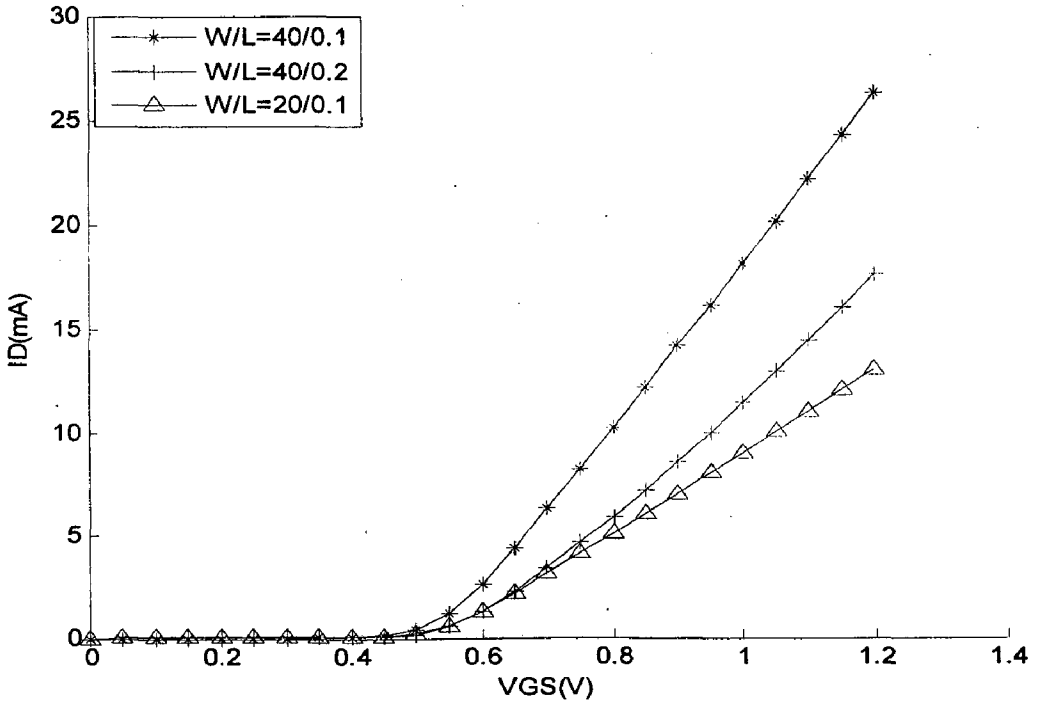


Figure 5.1 I_D vs. V_{GS} at V_{DS} =1V.

Fig5.1 shows the drain current of n channel MOSFET at different gate voltages at constant drain voltage (1V).Threshold voltage of the device is 0.397V. From the graphs we can observe that linearity can be improved by strong biasing of the device. According to the square law devices with sizes 20/0.1 and 40/0.2 should have the same current value, which is not the case here. With the aid of this graph .we can evaluate the extent of the deviation of the I-V characteristics from the classical model.

5.1.2 Transconductance

Transconductance of the device can be obtained by differentiating the DC drain current with respect to gate to source voltage (V_{GS}). Transconductance is important for the design of an amplifier as the internal gain of an amplifier is the product of device transconductance and the output resistance.

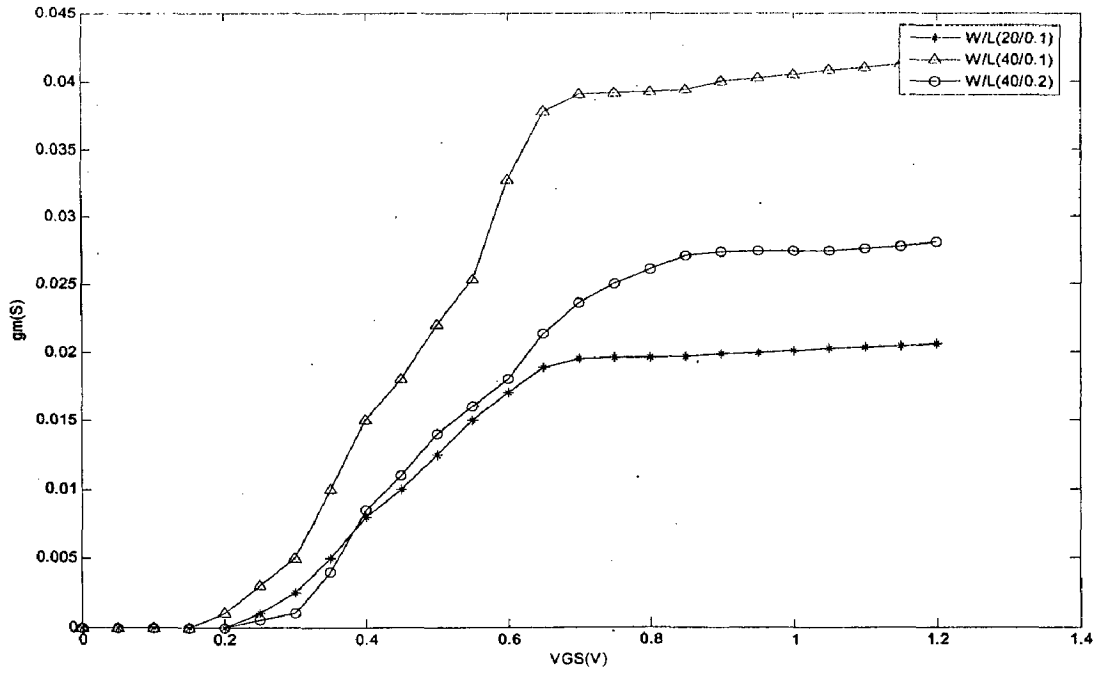


Figure 5.2 g_m vs. V_{GS} at V_{DS}=1V.

From the fig5.2 we can see that g_m increases rapidly with V_{GS} until it reaches a saturated value at V_{GS} a well above threshold voltage (V_{TH}).

5.1.3Transconductance Efficiency

Transconductance efficiency is defined as the ratio of transconductance to drain current (g_m / I_D)[15].fig shows the transconductance efficiency as a function of V_{GS} .

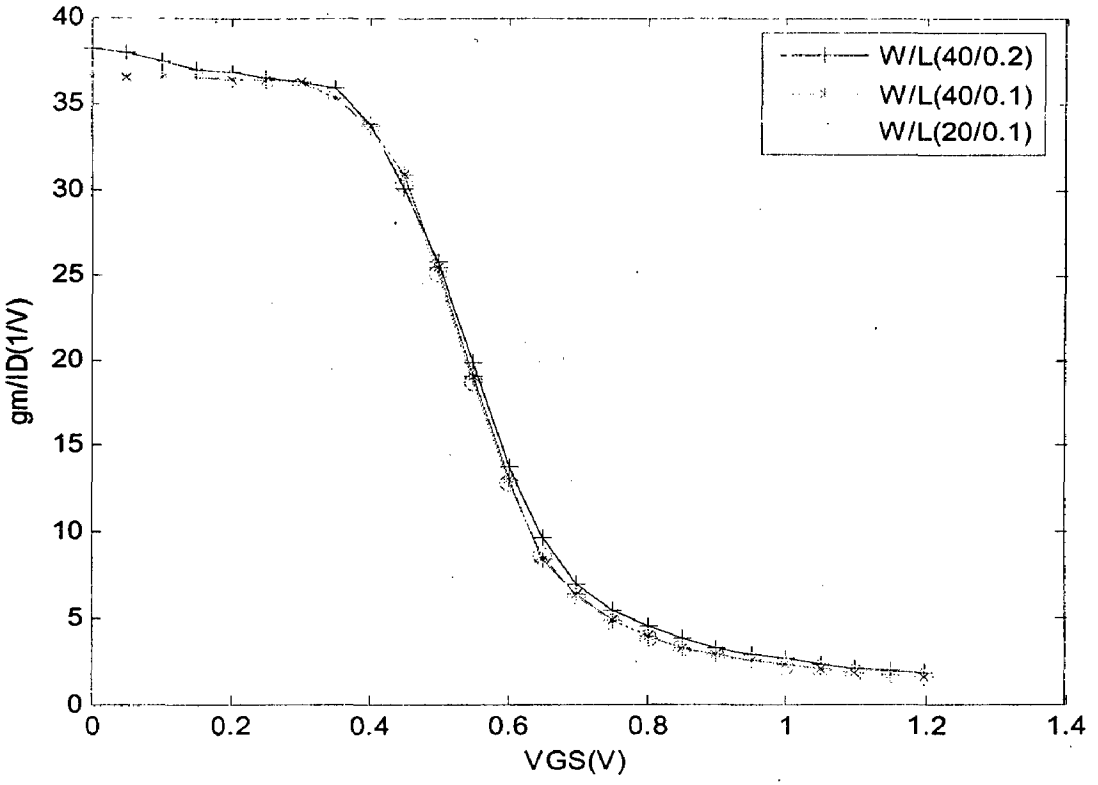


Figure5.3 g_m / I_D vs. V_{GS} at V_{DS}=1V.

From fig5.3 it can be said that transconductance efficiency is independent of width of the device, leaving device biasing as the primary variable for obtaining maximum possible transconductance efficiency. This means that circuit design that optimizes transconductance efficiency can be broken down in to two steps : first determining bias condition for maximum transconductance efficiency, then sizing the device based on the absolute power requirement.

From the fig 5.3 we can see that for maximum transconductance efficiency device should be biased in sub threshold region. However f_T in the sub threshold region may be insufficient. A good compromise is to operate the device just above the threshold voltage.

5.1.4 Cutoff Frequency

Cutoff frequency also known as transition frequency (f_T) is defined as the frequency at which current gain of the device is equal to unity [16].

$$f_T = \frac{g_m}{2\Pi(C_{gs} + C_{gd})} \tag{5.1}$$

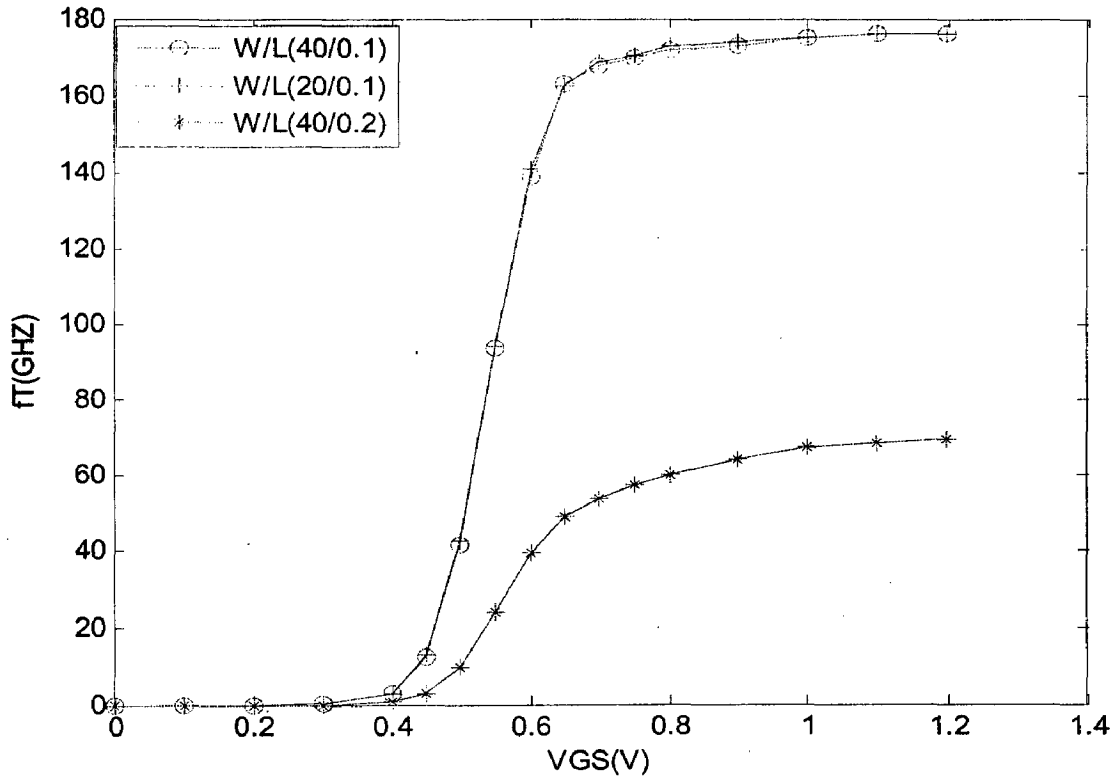


Figure 5.4 f_T vs. V_{GS} at V_{DS}=1V.

Fig5.4 shows f_T as a function of. From the graph we can observe that for device sizes 20/0.1 and 40/0.1 the curves are over lapping, indicating that for a fixed value of L of the device f_T is independent of the width of the device. From above equation we can see that increase in g_m due to increase in W is offset by increase in the parasitic capacitances. Also we can observe from the fig is that f_T is relatively low at low values of Vgs, which is necessary for low voltage applications, and since a high f_T is necessary for a low

noise figure, a tradeoff is needed between noise figure and power. And f_T is degraded when device is operated in sub threshold region and when non minimum L is used.

5.1.5 Output Resistance

Internal gain of an amplifier depends up on the output resistance of the device (or r_o).

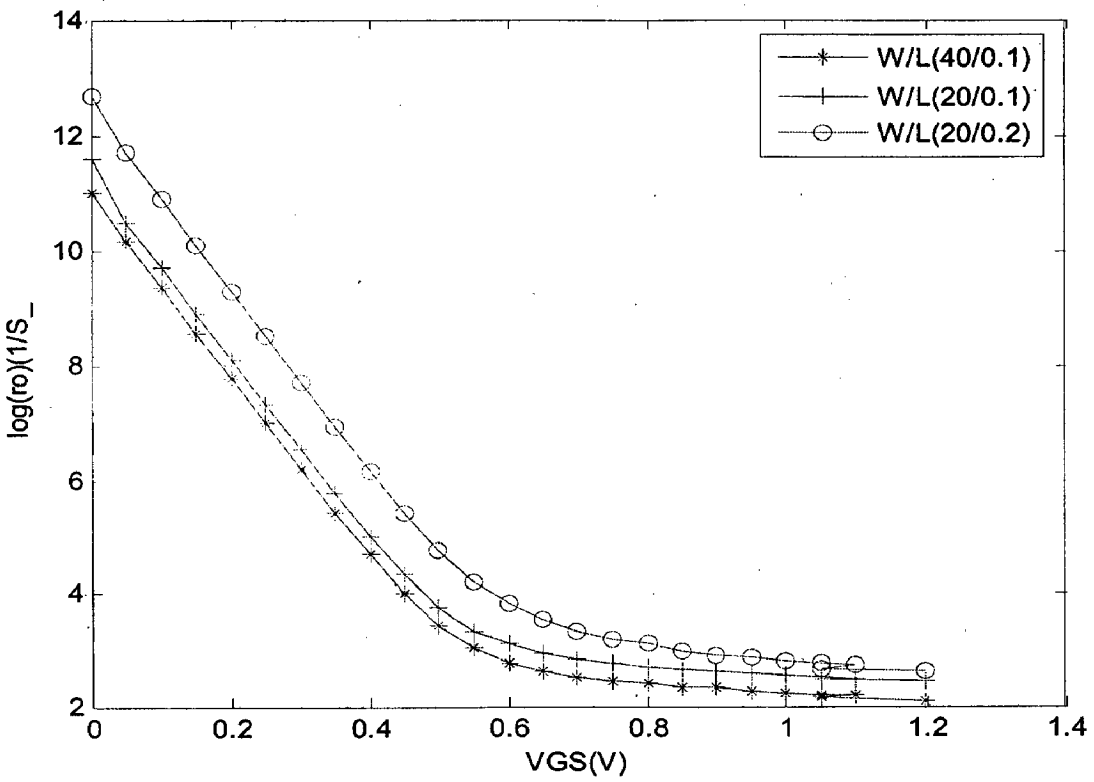


Figure 5.5 $\log r_o$ vs. V_{GS} at V_{DS}=1V.

Whose value can be expressed as $1/g_{ds}$ where g_{ds} is the drain to the source conductance. If r_o is small, as it appears in parallel with the amplifier's load can significantly reduce the output resistance of the amplifier, hence degrading the gain of the amplifier. For micron technologies r_o value is very high so that it can be neglected. As moves in to sub micron region r_o value decreases due to the channel length modulation, as shown in the fig r_o value may be in the order of several hundred ohms for practical biasing voltages. From the fig we can also see that r_o is a strong function of bias voltage, W, L.

5.1.6 Intrinsic Gain

Intrinsic gain is defined as the product of r_o and g_m. Intrinsic gain represents the maximum gain achievable by a single transistor.

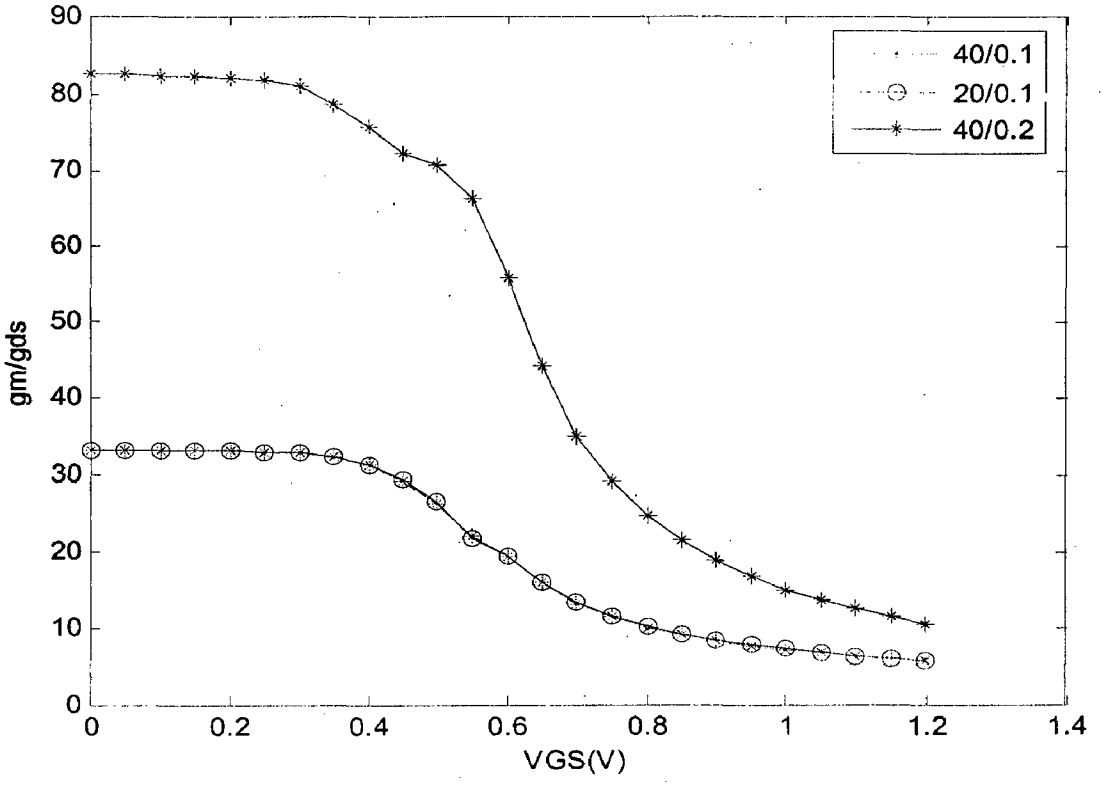


Figure 5.6 intrinsic gain vs. V_{GS} at V_{DS} =1V.

Fig5.6 shows intrinsic gain as a function of bias voltage. From the fig we can see that intrinsic gain improves as the length of the channel is increased. However using non minimum channel length is often not a good practice in designing LNA as it degrades the noise performance. If gain is compromised to achieve low noise, then multiple gain stages may be required.

5.2 Width Dependency of Noise Figure

Fig 5.7 shows the noise figure of common source cascode LNA for different widths of transistor.

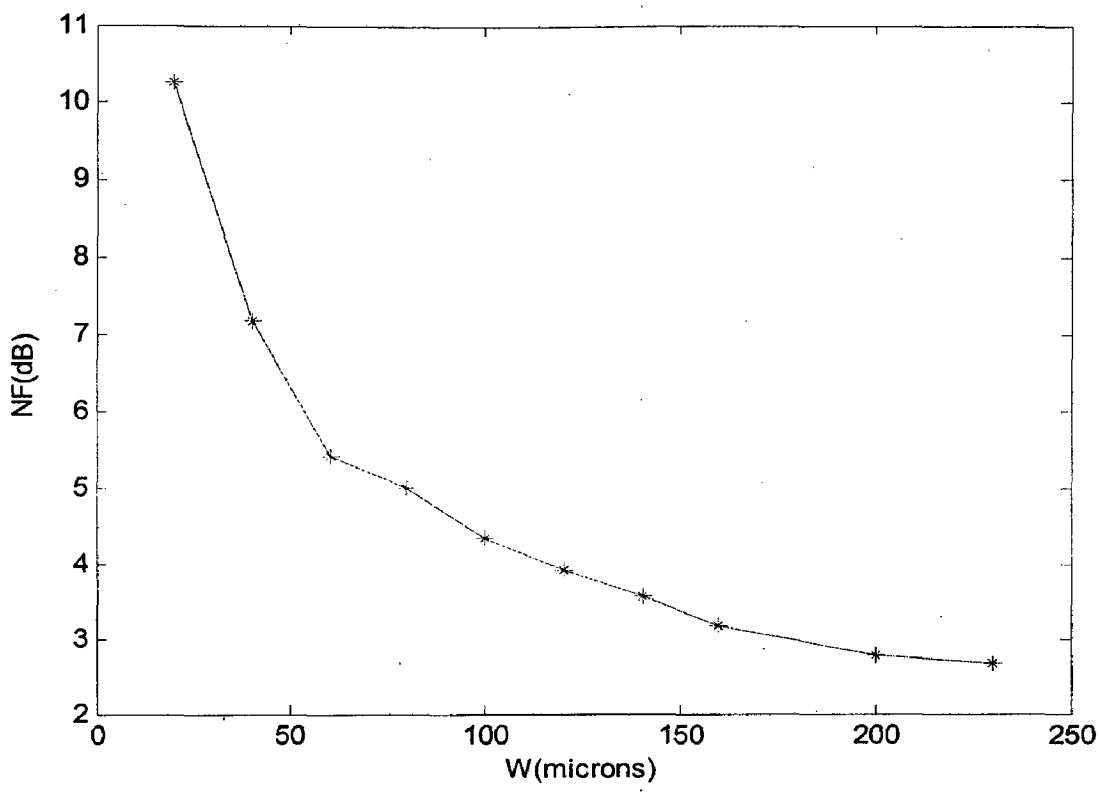


Figure 5.7 NF vs. Width of the device

From the above figure we can see that NF decreases as W increases, which suggests a tradeoff between NF and power consumption, indicating that low noise is fundamentally difficult to achieve for low voltage applications.

5.3 LNA Design for Low Power Applications

Conventional power constrained noise optimization technique when applied for low voltage applications with large gate widths combined with small drain currents often force the device to operate the device in sub threshold region which may lead to the insufficient frequency response.

Instead if we begin the design procedure with device biasing has the advantage that all of gain, noise, and power are taken at the start of the design. In this section a step by step design methodology of cascode LNA shown in the fig5.8 is described.

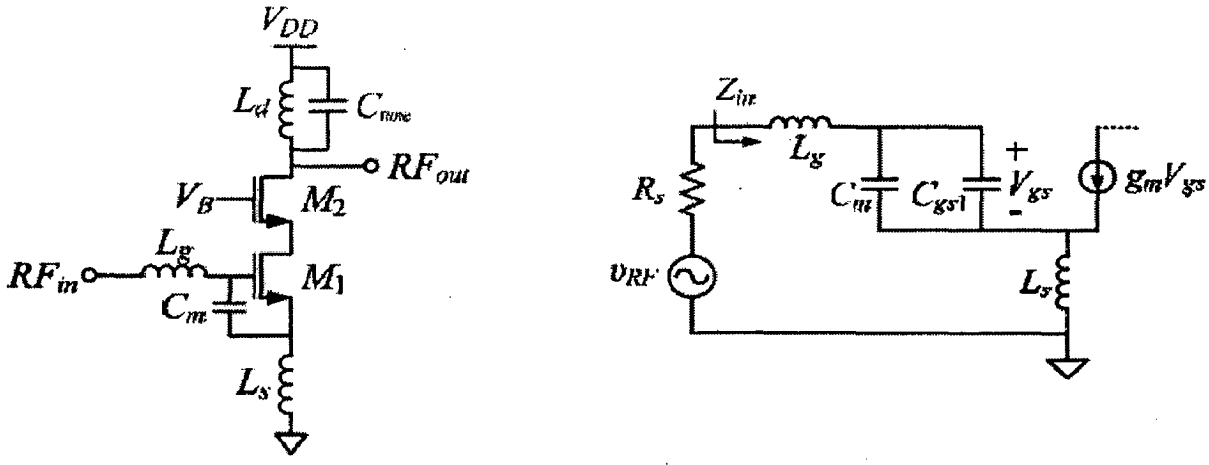


Figure 5.8 (a) Schematic of cascode LNA, (b) small signal equivalent circuit

Choosing bias voltage (V_{GS})

We are deigning the LNA for low power applications we have to choose the value of V_{GS} which maximizes transconductance efficiency (g_m / I_D). From the device characteristics graphs we know that as V_{GS} increases g_m / I_D value decreases but g_m, f_T improves. This suggests that there exist an optimal value of V_{GS} for a given applications. Ideally, V_{GS} should be chosen to be a low value to maximize g_m / I_D, which leads to a power-efficient circuit. But the lower bound of V_{GS} is governed by designing for sufficient g_m, which translates proportionally to amplifier gain, and sufficient f_T, which provides enough bandwidth for the amplifier operating frequency.

V_{GS} can also determine linearity performance. The fact that the device exhibits superb linearity performance when biased in moderate inversion gives the designer more incentive to choose V_{GS} from a narrow range that corresponds to moderate inversion.

Since f_T and g_m fall dramatically as V_{GS} enters the sub threshold values, having V_{GS} slightly above V_{TH} is often a good choice for RF operations (frequency roughly below

10GHz). For operation at a higher frequency, a higher V_{GS} is often needed to achieve a f_T close to the maximum achievable by the technology.

As can be seen from the above discussion, all of gain, noise, and linearity are simultaneously affected by biasing, reflecting the interdependent nature of analog circuit design.

Drain current

Calculate the drain current I_D from the target power consumption (excluding biasing circuits) P_{DC} and target supply voltage V_{DD}, namely $I_D = P_{DC} / V_{DD}$.

Width of the transistor

Drain current of short channel devices is given as [17]

$$I_D = W v_{sat} C_{ox} \frac{(V_{GS} - V_{TH})^2}{(V_{GS} - V_{TH}) + E_c L}(1 + \lambda V_{DS}) \qquad (5.2)$$

Where v_{sat} is the saturation velocity.

E_c is the critical electric field.

λ is the channel length modulation coefficient.

From the above equation width of the device can be determined.

Gate Capacitance

Decide whether or not additional gate-to-source capacitance C_m is beneficial. If the circuit is designed to operate at high frequency, C_{gs} should be minimized to improve f_T. If the circuit is designed for operation at relatively low frequency, the lower resonance frequency of the circuit requires larger combined inductance and capacitance. Since large on-chip inductors cost significant area and cannot be made with high Q in current standard technologies, it is easier to add capacitance.

Input matching inductors (L_s, L_g)

From the small signal equivalent circuit the input impedance of the LNA Z_{in} is given as

$$Z_{in} = \frac{1}{j\omega C_{gs}} + j\omega(L_s + L_g) + \frac{L_s g_m}{C_{gs}} \tag{5.3}$$

Where $C_{gs} = C_{gs1} // C_m$.

Since Z_{in} is to be matched to the source impedance, which is typically 50Ω in an RF system, the real and imagery parts of Z_{in} can be expressed as follows:

$$\mathrm{Re}(Z_{in}) = \frac{L_s g_m}{C_{gs}} = 50 \tag{5.4}$$

$$\mathrm{Im}(Z_{in}) = \frac{1}{j\omega C_{gs}} + j\omega(L_s + L_g) = 0 \tag{5.5}$$

From the bias condition we can determine the value of g_m. From this value we can determine the values of L_s and C_{gs}. It's better to choose the value of L_s first as the inductors that are suitable for on-chip implementation have a smaller range of values. L_g can be found from equation .

Finally we have to choose the load inductor (L_d) and tuning capacitor (C_{tune}) such that they will resonate at the operating frequency.

Chapter 6

LNA Design and Simulation Results

To demonstrate the application of the design methodology proposed in Chapter 4, an LNA is designed and simulated in a commercial 90nm CMOS technology to operate at the 2.4GHz band.

6.1 Power Efficient LNA Design

To alleviate the shortcomings of the common-source topology as discussed in Chapter 3, the cascode topology as discussed previously is used, hereby reproduced as Fig. 5.1 for convenience.

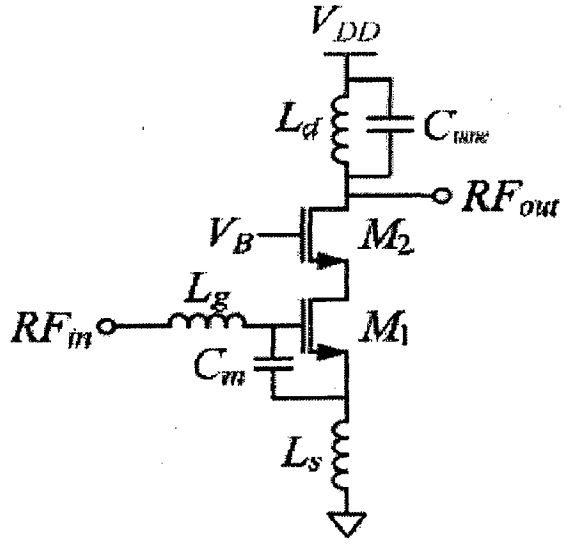


Figure 6.1 cascode LNA

6.1.1 Bias Current

The biasing of the transistors has strong implications on LNA performance such as gain, noise. When a short-channel MOSFET is biased in saturation, I_D can be expressed as:

$$I_D = W v_{sat} C_{ox} \frac{(V_{GS} - V_{TH})^2}{(V_{GS} - V_{TH}) + E_c L} (1 + \lambda V_{DS}) \qquad (6.1)$$

Where v_{sat} is the saturation velocity.

E_c is the critical electric field.

λ is the channel length modulation coefficient.

When L is kept to its minimum, V_{GS} and W are key design parameters that directly link to power consumption. The drain current of a 90nm cascode LNA is plotted in Figures 6.2 and6.3 to quantify the sensitivity of power consumption to V_{GS} and W (supply voltage = 1V). The threshold voltage of the technology used is 0.394V. In the typical analog design space for this technology (i.e., V_{GS} in the range of 0.4V to 0.8V), power consumption increases 8 times whereas, a change of W from 10μm to 80μm (V_{GS} held constant at 0.42V) leads to a power increase of 7 times.

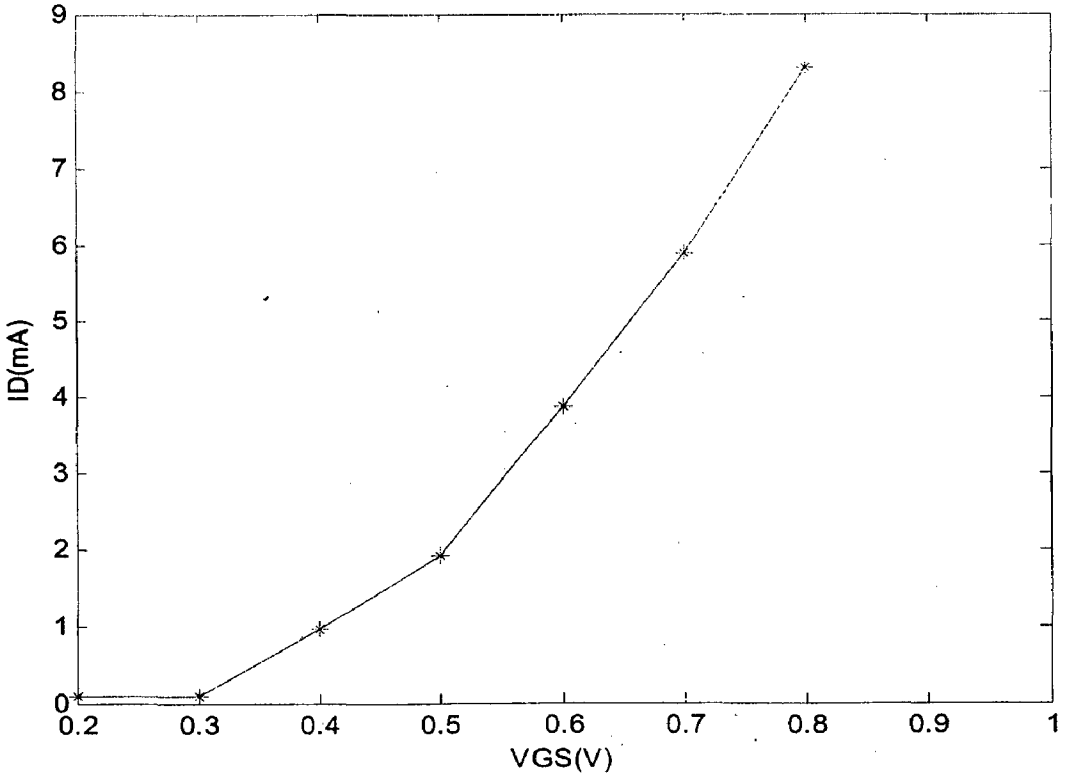


Figure 6.2 drain current of cascode LNA vs. bias voltage for (W=25microns)

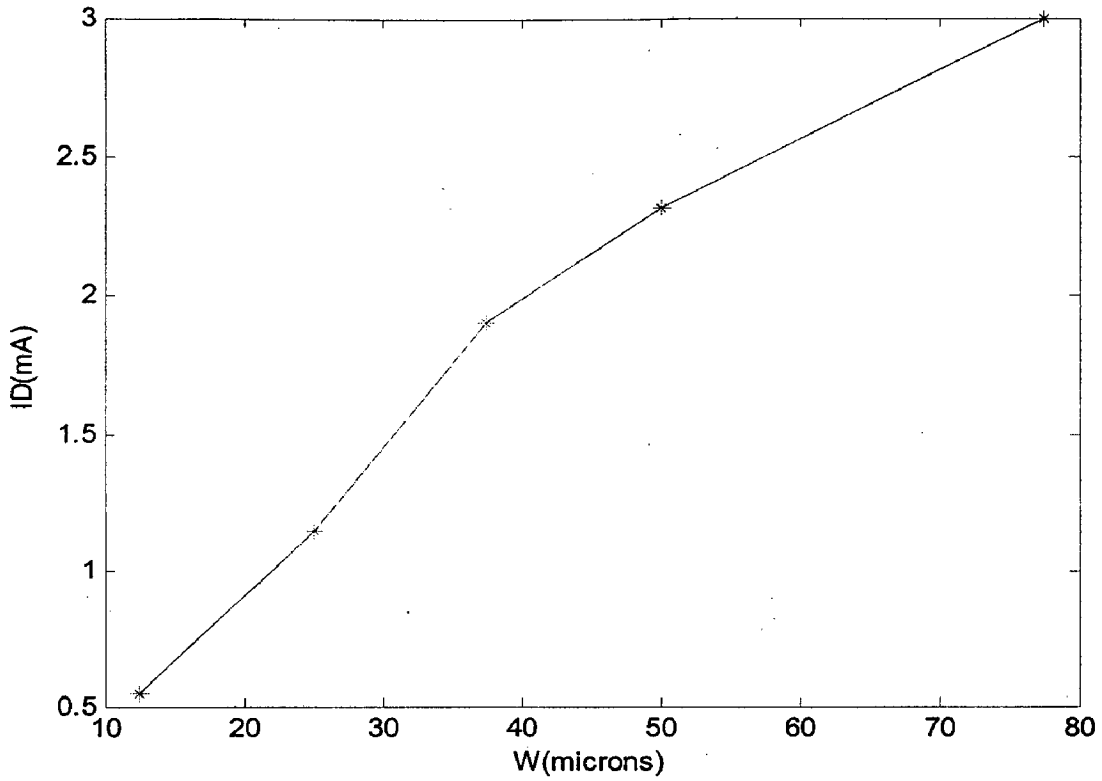


Figure 6.3 drain current of cascode LNA vs. width (at bias voltage=0.42V)

6.1.2 Gain

Figures 6.4 shows the simulated voltage gain Av of the cascode amplifier at 2.4GHz . While sweeping V_{GS} , V_B is also modified such that the ratio V_{GS1}/V_{GS2} , hence g_{m1}/g_{m2}, is relatively constant. It may seem counterintuitive that Av only increases lightly as V_{GS} changes from 0.4V to 0.8V. As V_{GS} increases, I_D also increases, which reduces the overall output impedance of the cascode structure. Since gain is the product of output impedance and transconductance, the reduction of output impedance partially counteracts the effects of increasing g_{m1} on the overall gain.

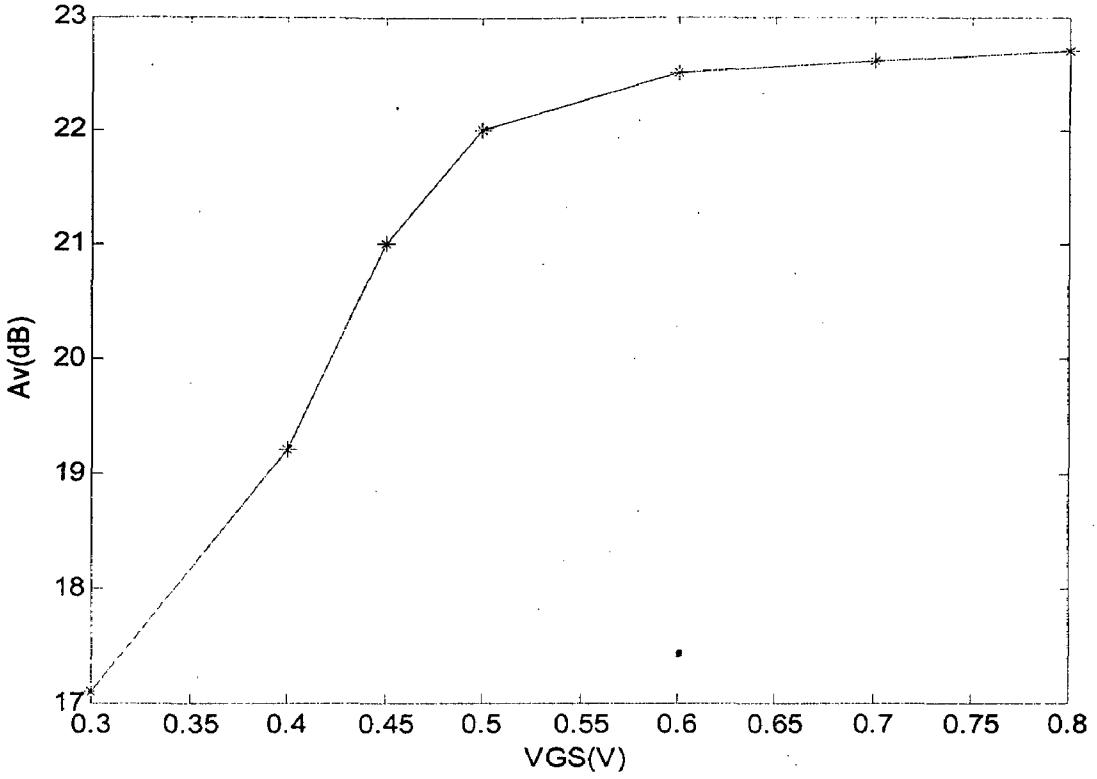


Figure 6.4 voltage gain of cascode LNA vs. bias voltage

6.1.3 Noise

The tables below shows that variations of noise figure with width of the device(W) and biasing(V_{GS}).

Table 6.1 shows NF as V_{GS} of M_1 is swept from 0.3V to 0.8V (W = 25μm). V_B is adjusted accordingly as mentioned earlier. As can be seen from table 1, NF is inadequate when operating in the subthreshold region (V_{GS} = 0.3V). For a change of V_{GS} from 0.4V to 0.8V, NF is reduced by 0.5dB at the expense of a 8 times increase in the power consumption. Table 6.2hows NF as the width of both transistors are changed simultaneously from 10μm to 50μm (V_{GS} = 0.42V), which results in a 3.4dB NF improvement at the expense of7 times the power consumption. This suggests that increasing W is a more effective method for reducing NF.

Table 6.1. Noise figure as a function of V_{GS} W=25 microns.

NF(dB)	V_{GS} (V)
5.8	0.3
2.9	0.4
2.68	0.5
2.54	0.6
2.48	0.7
2.4	0.8

Table 6.2. Noise figure as a function of width V_{GS} =0.42V

NF(dB)	W(microns)
4.6	10
3.1	20
2.68	30
2.42	40
2.3	50

6.2 Simulation Results

The cascode LNA has been simulated using the BSIM4 model provided for 90nm CMOS process using micro wave office. The widths of both transistors are sized equally. V_{GS} is chosen to be 0.42V, slightly above the threshold voltage to exploit the high g_m/I_D in moderate inversion. Table 6.3 is a summary of component values.

Table 6.4 shows the performance summary of LNA. The voltage gain Av is 20.6 dB and NF of the LNA is 2.87dB which is acceptable for short-range applications. $S11$ of −14.7dB provides a good input impedance matching to 50Ω. Circuit consumes a 1.1mW power from 1 volt supply voltage.

Table 6.3 LNA component values

W_1/L_1, W_2/L_2. (in microns)	25/0.1
Bias voltage(V)	0.42
Supply voltage (V)	1
L_s(nH)	1
L_g(nH)	19
L_d (nH)	5
C_m (fF)	192
C_{tun}(fF)	700
V_B (volt)	1

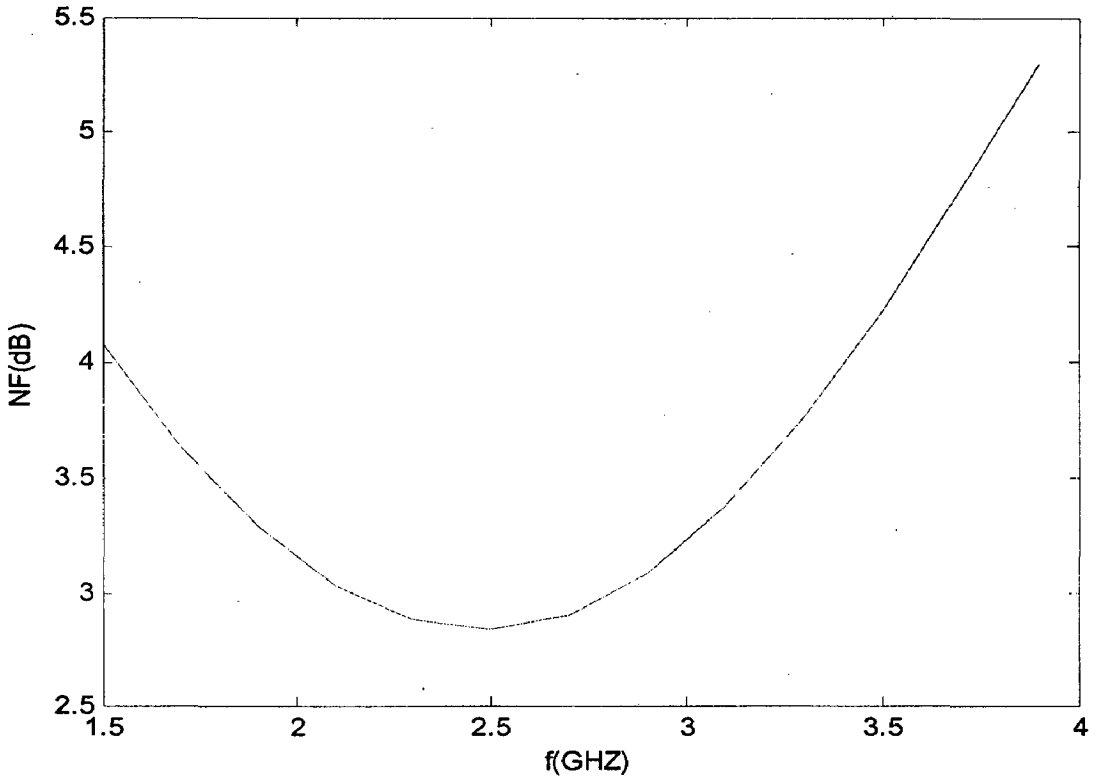


Figure 6.5 Noise figure of cascode LNA vs.frequency

Table 6.4 Performance Summary

Voltage Gain(dB)	20.6
Noise Figure(dB)	2.87
P_{DC}(mW)	1.1
Bias current(mA)	1.1
S_{11}(dB)	-14.7dB
Operating frequency(GHZ)	2.4

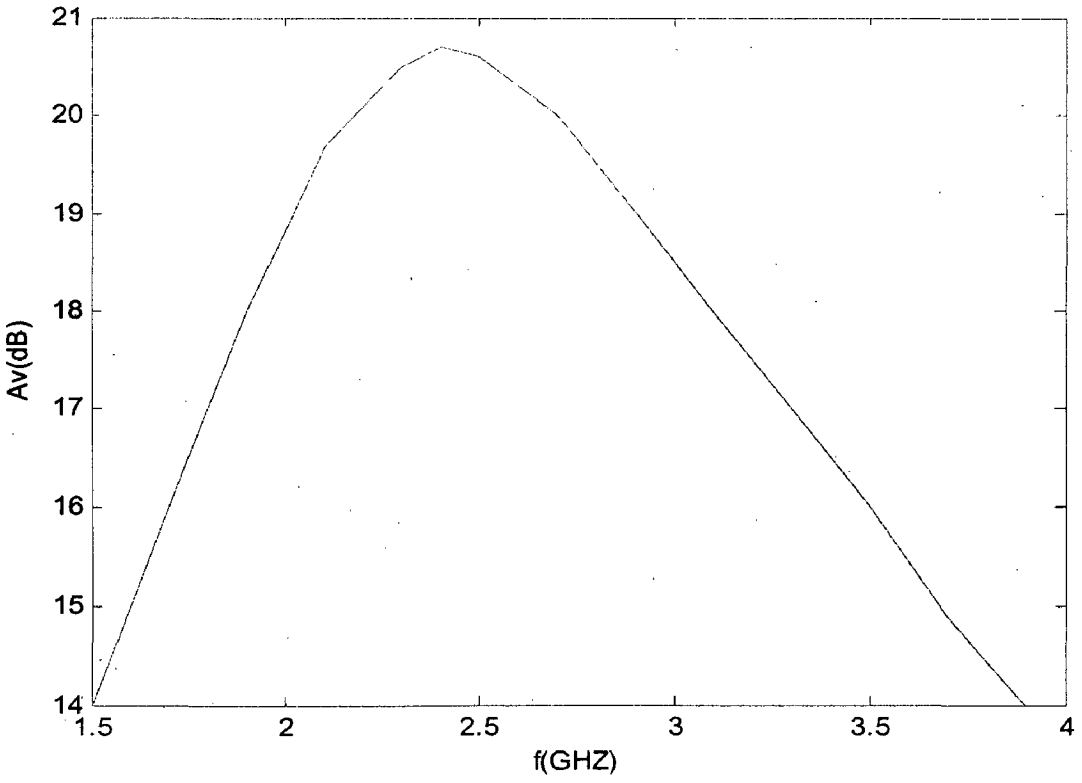


Figure 6.6 Voltage gain of cascode LNA vs. frequency.

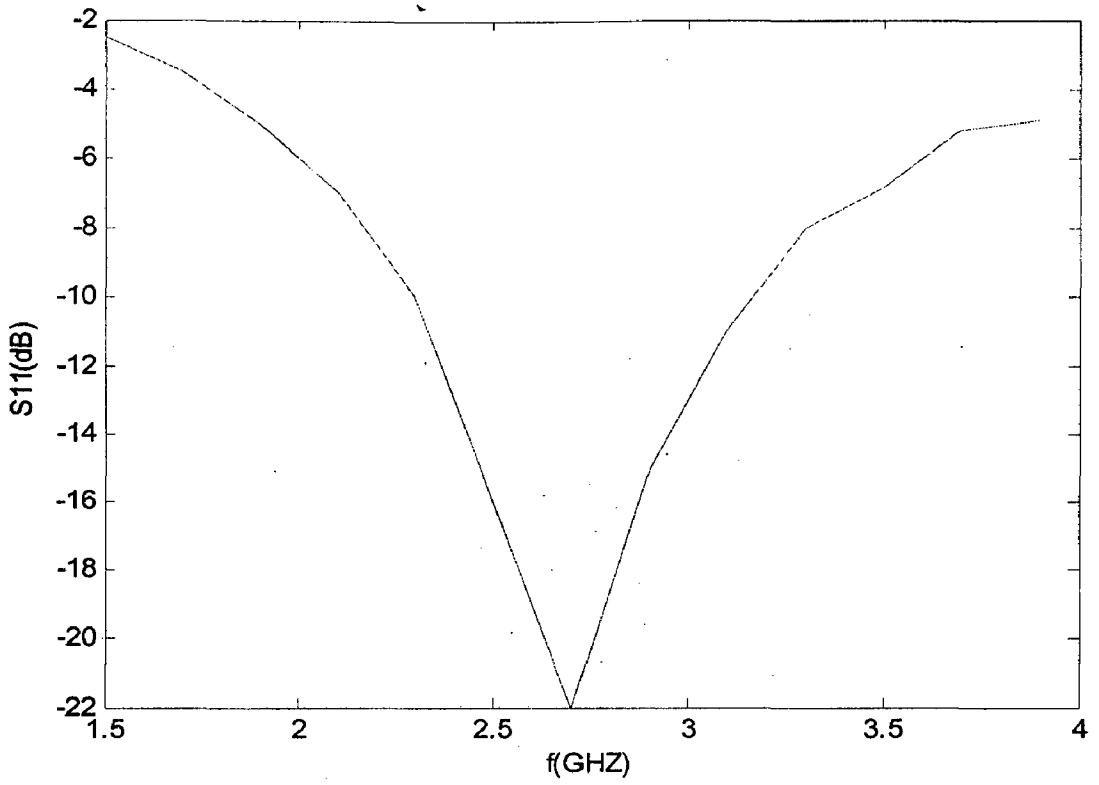


Figure 6.6 Reverse isolation of cascode LNA vs frequency

Chapter 7

Conclusion and Future work

Conclusion

In this work, the design, simulation of a 1.1mW 90nm CMOS low noise amplifier with a gain of 20.6dB and a noise figure of 2.87 dB was shown. The design methodology used in this work differs from the power constrained noise optimization (PCNO) technique in that it begins with determining how device biasing affects gain, noise, and power consumption of the amplifier to ensure a well-rounded design. Design plots have been used to help the circuit designer in understanding the fundamental characteristics of the MOSFET in preparation to applying the design methodology.

Future work

1. The effectiveness of the proposed design methodology has thus far been verified with Microwave office simulation results. Lay out of LNA is the next step for getting more accurate results.
2. Silicon on insulator (SOI) can be used to replace bulk CMOS with increasing difficulties with device scaling of bulk MOSFET.

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APPENDIX

BSIM4 MODEL PARAMETERS FOR 90nm TECHNOLOGY

```
* Beta Version released on 2/22/06

* PTM 90nm NMOS

.model  nmos  nmos  level = 54

+version = 4.0           binunit = 1           paramchk= 1
mobmod  = 0
+capmod  = 2             igcmod  = 1           igbmod  = 1
geomod  = 1
+diomod  = 1             rdsmod  = 0           rbodymod= 1
rgatemod= 1
+permod  = 1             acnqsmod= 0           trnqsmod= 0

+tnom    = 27            toxe    = 2.05e-9     toxp    = 1.4e-9
toxm    = 2.05e-9
+dtox    = 0.65e-9       epsrox  = 3.9         wint    = 5e-009
lint    = 7.5e-009
+ll      = 0             wl      = 0           lln     = 1
wln     = 1
+lw      = 0             ww      = 0           lwn     = 1
wwn     = 1
+lwl     = 0             wwl     = 0           xpart   = 0
toxref  = 2.05e-9
+xl      = -40e-9
+vth0    = 0.397         k1      = 0.4         k2      = 0.01
k3      = 0
+k3b     = 0             w0      = 2.5e-006    dvt0    = 1
dvt1    = 2
+dvt2    = -0.032        dvt0w   = 0           dvt1w   = 0
dvt2w   = 0
+dsub    = 0.1           minv    = 0.05        voffl   = 0
dvtp0   = 1.2e-009
+dvtp1   = 0.1           lpe0    = 0           lpeb    = 0
xj      = 2.8e-008
+ngate   = 2e+020        ndep    = 1.94e+018   nsd     = 2e+020
phin    = 0
+cdsc    = 0.0002        cdscb   = 0           cdscd   = 0
cit     = 0
+voff    = -0.13         nfactor = 1.7         eta0    = 0.0074
etab    = 0
+vfb     = -0.55         u0      = 0.0547      ua      = 6e-010
ub      = 1.2e-018
+uc      = -3e-011       vsat    = 113760      a0      = 1.0
ags     = 1e-020
+a1      = 0             a2      = 1           b0      = -1e-020
b1      = 0
+keta    = 0.04          dwg     = 0           dwb     = 0
pclm    = 0.06
```

```
+pdiblc1 = 0.001        pdiblc2 = 0.001        pdiblcb = -0.005
drout    = 0.5
+pvag    = 1e-020       delta   = 0.01         pscbe1  = 8.14e+008
pscbe2   = 1e-007
+fprout  = 0.2          pdits   = 0.08         pditsd  = 0.23
pditsl   = 2.3e+006
+rsh     = 5            rdsw    = 180          rsw     = 90
rdw      = 90
+rdswmin = 0            rdwmin  = 0            rswmin  = 0
prwg     = 0
+prwb    = 6.8e-011     wr      = 1            alpha0  = 0.074
alpha1   = 0.005
+beta0   = 30           agidl   = 0.0002       bgidl   = 2.1e+009
cgidl    = 0.0002
+egidl   = 0.8

+aigbacc = 0.012        bigbacc = 0.0028       cigbacc = 0.002
+nigbacc = 1            aigbinv = 0.014        bigbinv = 0.004
cigbinv  = 0.004
+eigbinv = 1.1          nigbinv = 3            aigc    = 0.012
bigc     = 0.0028
+cigc    = 0.002        aigsd   = 0.012        bigsd   = 0.0028
cigsd    = 0.002
+nigc    = 1            poxedge = 1            pigcd   = 1
ntox     = 1

+xrcrg1  = 12           xrcrg2  = 5
+cgso    = 1.9e-010     cgdo    = 1.9e-010     cgbo    = 2.56e-011
cgdl     = 2.653e-10
+cgsl    = 2.653e-10    ckappas = 0.03         ckappad = 0.03
acde     = 1
+moin    = 15           noff    = 0.9          voffcv  = 0.02

+kt1     = -0.11        kt11    = 0            kt2     = 0.022
ute      = -1.5
+ua1     = 4.31e-009    ub1     = 7.61e-018    uc1     = -5.6e-011
prt      = 0
+at      = 33000

+fnoimod = 1            tnoimod = 0

+jss     = 0.0001       jsws    = 1e-011       jswgs   = 1e-010
njs      = 1
+ijthsfwd= 0.01         ijthsrev= 0.001        bvs     = 10
xjbvs    = 1
+jsd     = 0.0001       jswd    = 1e-011       jswgd   = 1e-010
njd      = 1
+ijthdfwd= 0.01         ijthdrev= 0.001        bvd     = 10
xjbvd    = 1
+pbs     = 1            cjs     = 0.0005       mjs     = 0.5
pbsws    = 1
+cjsws   = 5e-010       mjsws   = 0.33         pbswgs  = 1
cjswgs   = 3e-010
+mjswgs  = 0.33         pbd     = 1            cjd     = 0.0005
mjd      = 0.5
+pbswd   = 1            cjswd   = 5e-010       mjswd   = 0.33
pbswgd   = 1
```

```
+cjswgd  = 5e-010        mjswgd  = 0.33          tpb     = 0.005
tcj      = 0.001
+tpbsw   = 0.005         tcjsw   = 0.001         tpbswg  = 0.005
tcjswg   = 0.001
+xtis    = 3             xtid    = 3

+dmcg    = 0e-006        dmci    = 0e-006        dmdg    = 0e-006
dmcgt    = 0e-007
+dwj     = 0.0e-008      xgw     = 0e-007        xgl     = 0e-008

+rshg    = 0.4           gbmin   = 1e-010        rbpb    = 5
rbpd     = 15
+rbps    = 15            rbdb    = 15            rbsb    = 15
ngcon    = 1
```