Design and Performance of Phase Comparison Carrier Current Relaying

A Dissertation
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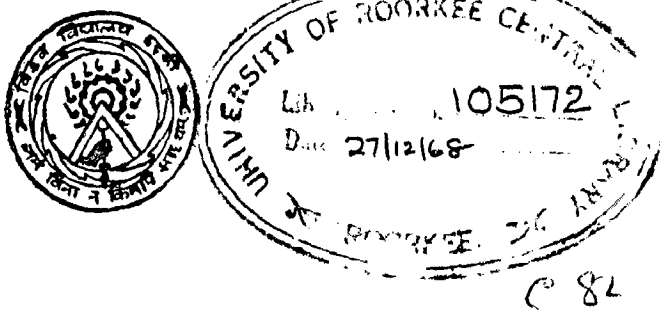
of the requirements for the Degree
of
MASTER OF ENGINEERING
in
POWER SYSTEM ENGINEERING

By
B.L. KAUL



DEPARTMENT OF ELECTRICAL ENGINEERING
UNIVERSITY OF ROORKEE
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CERTIFICATE

Certified that the dissertation entitled "Design and Performance of Phase Comparison Carrier Current Relaying" which is being submitted by Sri B.L. Kaul in partial fulfilment for the award of the Degree of Master of Engineering in "Power System Engineering", of the University of Roorkee, Roorkee, is a record of candidate's own work carried out by him under my supervision and guidance. The matter embodied in this dissertation has not been submitted for the award of any other degree or diploma.

This is further to certify that he has worked for nine months from January 1968 to September, 1968 for preparing dissertation for the Master of Engineering Degree at this University.

ROORKEE,
Dated: 19th Sept. 1968

(T.S.M. RAO)
Professor and Head,
Department of Elect.Engg.,
University of Roorkee,
ROORKEE

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B.L. Kaul

(B.L. KAUL)

Roorkee,
September 19, 1968.

SYNOPSIS

For the past few years, Junction transistors have been widely used for power system protection. Because of their reliability, long life and high speed of operation, they have replaced thermionic valves to a great extent. Only recently, Junction transistors have been used for phase comparison carrier protection. It is seen, that high frequency, high power transistors, which are not now? available, make it possible to obtain the required level of carrier output power.

One of the most important aspects of phase comparison system lies in the choice of relaying quantities. Selection of such a suitable network has been made, which produces all the relaying quantities simultaneously, while using only three main current transformers. Within this network means have been provided for an easy variation of the proportions of positive and negative sequence components in the combined sequence output. A filter network has been used to eliminate the d.c. transient and harmonic components. Two successive equipments have been built and thoroughly tested.

CONTENTS

C H A P T E R - 1

INTRODUCTION

1.1. INTRODUCTION TO CARRIER CURRENT RELAYING:

The use of power line carrier originated long back in 1918 but it was not applied to protection purposes till 1928. Power line carrier has become an accepted medium for the transmission of intelligence for High-Speed Relaying and several other functions between stations on a power system. Because of its versatility, it has been applied extensively to transmission networks of all voltage classes and all degrees of complexity. Viewed broadly, the situation is that with long lines, the transference of information from one end to the other end is uneconomical for a unit type of protection if conventional pilot wires are used and it is possible to justify the cost and complexity of transforming information by means of carrier channels on the power conductors. Recent increase in the use of power line carrier equipment is directly connected with the increased load due to the power industry development and the development of long distance interconnectors on power grids. High speed protection, obtainable on long lines only through the use of carrier pilot relaying, increases the stability limit of transmission circuits so as to permit increased loading of existing lines. This factor alone, provides large savings in copper and other transmission line materials which, otherwise would be required by new construction or by the use of double circuit lines with slower relaying.

The major part of carrier equipment used for the protection forms part of the composite carrier communication equipment. Lately, transistorised audio frequency shift equipment has been employed for protection along with the single side band carrier communication equipment. Frequency shift technique is used to get over the problem of interference and to provide continuous supervision of carrier equipment. Interference problem can be solved by using

high power amplifiers and reducing the sensitivity of the receiver. Reliability and convenience of carrier telephone circuits for despatching permit existing generating and substation equipment to be operated nearer to maximum load and efficiency conditions.

Pilot wire relaying is particularly suited to large metropolitan areas where line sections are short and leased or private cable circuits are available. For longer power circuits and interconnectors, carrier current protection has an economic advantage in addition to the additional functions that it can provide. No other equipment generally provides instantaneous and simultaneous tripping of widely separated circuit breakers for all types of faults and all fault locations within the zone of protection. Such high-speed isolation of the fault contributes greatly to increased continuity of service of minimising fault damage, reducing outage time and generally improving system stability.

Carrier current equipment has greatly increased in reliability since its first development. Thermionic valves, although greatly improved, have been the chief cause of outages. Unless a careful check is maintained on the tube performance, so that proper replacement can be made, failures are certain to occur. However, with the development of transistor technology, this difficulty has been overcome. By their very nature, transistors give promise of long life and therefore a means of eliminating the major cause of carrier failure from tubes. The overall operating time to trip the circuit breakers at both ends has been reduced to 2 cycles or lesser, by the application of transistorised equipment. One such system has been described in detail in the following chapters.

1.2. GENERAL REQUIREMENTS OF A CARRIER RELAYING SYSTEM:

In carrier current relaying, the principle of operation is

somewhat similar to the type of differential relaying employed in pilot wire relaying. But, contrary to the common practice in pilot wire relaying, a quantitative comparison of the currents at the two ends of the line is not made in carrier relaying. Instead the simplest signal is transmitted, that is, the carrier is either on or off. Hence operation is not adversely affected by considerable variation in the strength of the received carrier signal. Fig.1.1 shows schematically the equipment required for a carrier current relaying system. At each end of the protected transmission line, there are protective relays, a transmitter-receiver unit, a coupling capacitor, line trap and line tuner.

The fundamental requirement imposed by the power system is that the means used to adapt the circuits for carrier channels shall not in any way interfere with the primary function of the power transmission. At the same time, to attain the desired degree of reliability, the carrier channels established should be free from interference or interruptions caused by the switching or normal operation of the power system and transient disturbances attributable to lightning or other causes. It is also essential that the carrier circuits should be safe, that is, they should be adequately insulated and protected against normal and abnormal voltages and currents so as to impose no hazard to connected apparatus or to personnel using and maintaining the equipment.

One of the most important factors is the wide difference between the power frequency and carrier current frequency. Circuit elements and power apparatus which offer very low impedance paths to power frequencies may appear as very high impedances at carrier frequencies and vice-versa. This phenomenon is largely responsible for the "trap jumping" myth that has attached itself with the power line

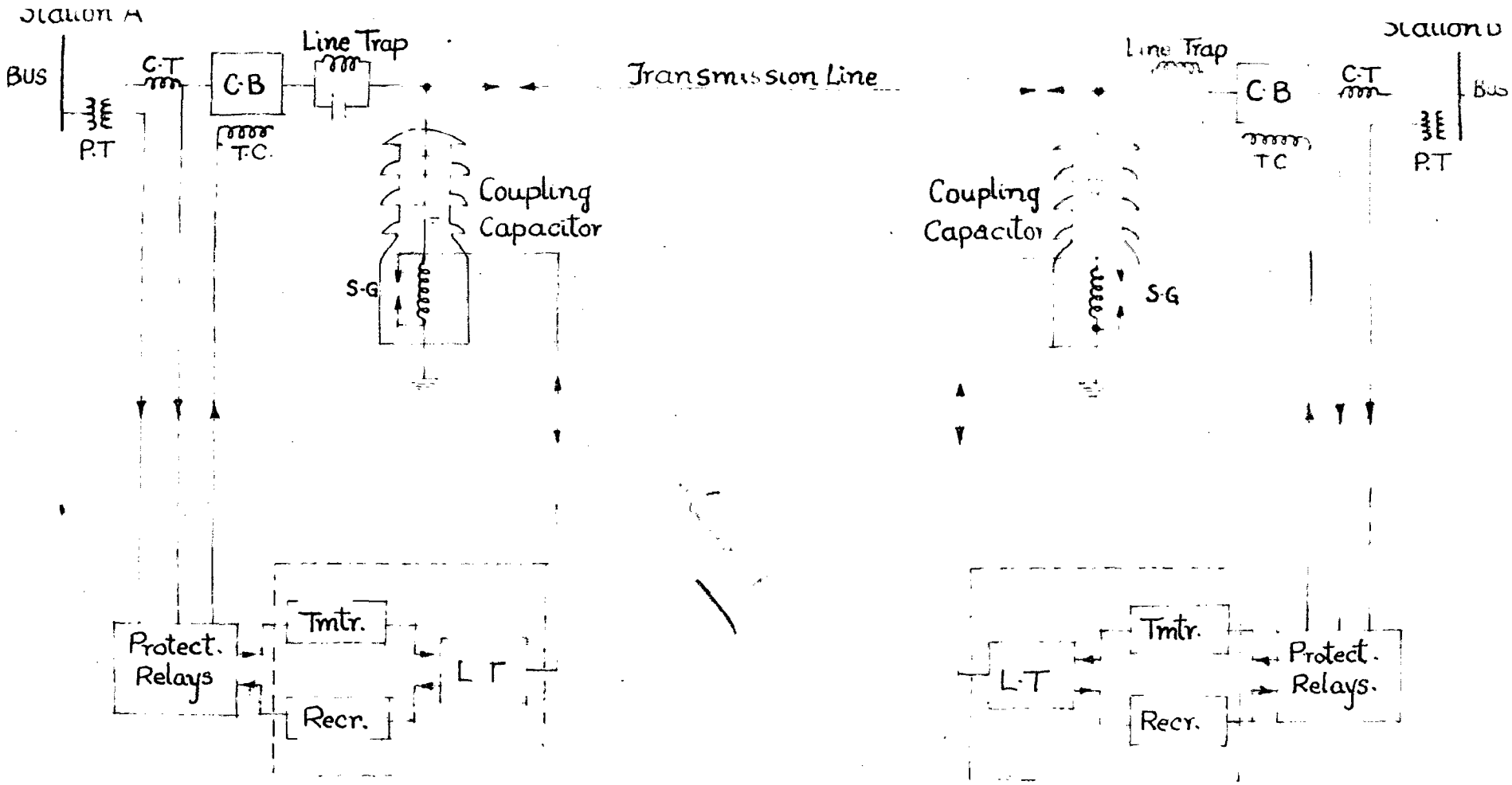


Fig 1.1 Block [illegible] Typical Carrier-Current Relaying System.

carrier.

The physical and economic restrictions imposed by a high voltage power system limit the devices that can be inserted directly in the power line to essentially only two, the coupling capacitor and the line trap. A little may be now said about the line coupling.

1.2.1. Line Coupling:

There are several ways to couple the carrier terminal equipment with the line. Some of these, which are most commonly employed are described below.

1.2.1.1. Single Interphase coupling:

Single interphase coupling as shown in Fig.(1.2) uses two of the three power phases of the transmission line as a path for the carrier energy, consequently, it is not affected by high ground resistances or variations in the ground resistance as in any other type of coupling which requires a ground return path for the carrier energy.

In an interphase coupled carrier circuit, conditions on the phase wires to which coupling is not made have negligible effect on the operation of the carrier channel. In addition, this type of coupling provides a circuit having the most stable operating characteristics, the lowest attenuation and the lowest noise level. Its principal disadvantage lies in the cost and the construction complexity involved in providing coupling and line traps for two phases throughout the circuit, as well as the complexity of the line-tuning equipment at terminals and by passes. It has been used most extensively for long haul circuits where its efficiency justifies its higher cost.

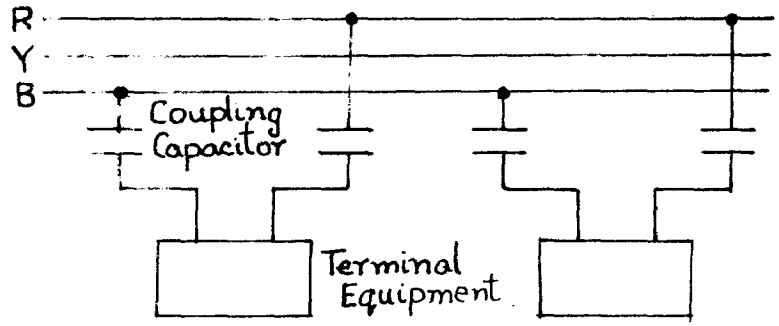


Fig 1-2 Interphase Coupling

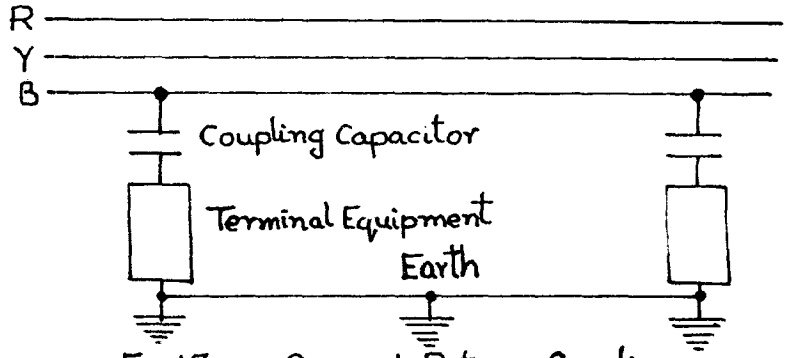


Fig 1-3 Ground Return Coupling

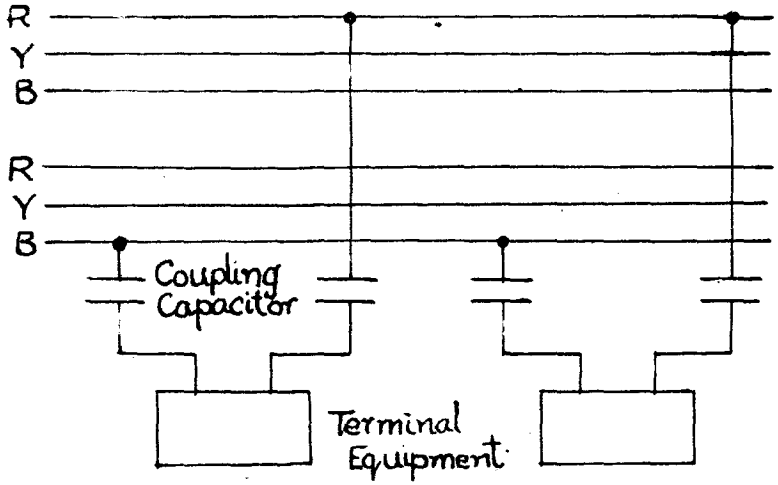


Fig 1-4 Intercircuit Coupling

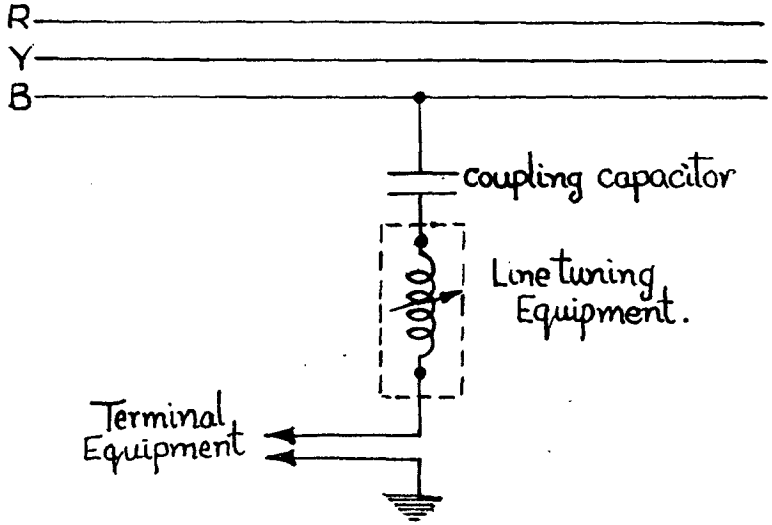


Fig 1-5 Single Frequency Tuning

1.2.1.2. Ground Return Coupling:

Ground return coupling utilizes only one phase wire of the transmission line and ground or any other suitable path for the return side of the circuit, as illustrated in Fig.(1.3) If good grounds are present at the carrier terminals, or if a ground wire is carried between the terminals, this type of coupling compares very favourably, in respect to line attenuation losses, with interphase coupling.

The principal advantage of ground return coupling is that it generally requires only half the number of coupling capacitors and line traps as required for full metallic coupling as interphase. In addition, the line tuning equipment required at terminals and by-passes is usually less complicated. Its main disadvantage is its somewhat higher attenuation and higher noise level as compared with the interphase circuit.

For many types of carrier channels, the disadvantages of the ground return circuit are greatly outweighed by its simplicity and lower cost. It is almost universally used for all pilot relay channels and extensively used on medium and short haul circuits for all other types of carrier channels.

1.2.1.3. Interphase-Coupling:

Where a double circuit transmission line is available between carrier terminal stations, it is sometimes desirable to use both lines for the carrier circuit to ensure its continuity when either line is taken out of service. The intercircuit coupling arrangement shown in Fig.(1.4) is used sometimes to provide this feature.

This is a form of interphase coupling in which coupling is made to one phase wire of one line and to a different phase wire of the other line of a double circuit power line. It is only applicable on double circuit lines which are incapable of being sectionalized between

the carrier terminals. Where a suitable frequency is available to permit the operation of the carrier channel with the increased number of switching configurations possible on the double line channel, as compared with a single line channel, this double circuit type of coupling will provide uninterrupted carrier service with all phases of either line solidly grounded at any point. In this respect, it will provide most of the advantages of double circuit interphase coupling but with half the coupling capacitors and line tuning assemblies required by double interphase coupling.

1.2.2. Coupling Capacitors:

Covering a considerable range in dielectric material and physical shape, the coupling capacitor has attained the status of a standardized and highly dependable piece of equipment, universally accepted as the standard means for connecting carrier circuits to high voltage lines. In its modern form, it consists of an assembly of one or more porcelain shell, oil filled paper dielectric capacitor units together with a base unit containing a grounding switch and protective equipment. The individual capacitor units are co-ordinated as to capacitance and voltage rating, so that they may be connected in series to form assemblies for any standard circuit voltage.

The inclusion of the protective equipment in the capacitor base is now a standard practice. This protective equipment usually consists of a gap and a power frequency drainage coil as shown in Fig.(1.1). The drainage coil ordinarily consists of an inductor connecting the low voltage side of the capacitor to ground. This coil which has an impedance of over 50,000 ohms at carrier frequencies and less than 100 ohms at power frequencies, serves to provide a path for the power frequency current of 50mA or so through the capacitor to ground and thus maintains the lead to the carrier

equipment at a normal power frequency of less than 5 volts. The gap, which is connected across the drainage coil, limits the voltage which can be built up on the carrier lead during transient voltage disturbances.

From the standpoint of power transmission system, it is essential that the insulation level of the capacitor assembly, in terms of impulse, wet and dry flash over withstand voltages, be coordinated with that of associated power line apparatus. From the standpoint of the carrier circuit, it is desirable that the capacitance be as large as possible, consistant with an economic design, preferably at least .001 μF.

Also, from the carrier circuit standpoint, it is essential that the carrier lead brought out from the base of the capacitor assembly be well insulated so as to maintain low capacitance and high leakage resistance to ground between the capacitor and the line tuning equipment.

1.2.3. Line-Trap:

In its simplest form this device consists of an air core reactor with a fixed or tapped capacitor connected in parallel to form a parallel resonant circuit. It is used in series with a conductor of the transmission circuit to provide a high impedance or trap for the currents of the carrier frequency to which the resonant circuit is tuned.

In this position, the reactor of the trap must carry not only the normal line current but all abnormal or short circuit currents that the line itself is expected to carry. Its position in the line also exposes it to transient high voltage disturbances attributable to lightning and switching, and adequate lightning arrestors must be provided across both capacitor and reactor.

Practical considerations of size, weight and cost have limited largely the maximum inductance available in the line trap reactor to approximately 250 micro-henries. Where it is necessary to trap more than two widely separated channels in single line conductor, additional traps are generally used.

More specifically, the principal applications of line traps may be listed as follows:

1. To reduce transmission losses in irrelevant branch-lines.
2. To minimize the effect of low impedance shunts.
3. To prevent interruption attributable to external faults or intentionally applied grounds.
4. To isolate the carrier channel effectively.

1.2.4. Line-Tuner:

This equipment, located in the circuit between the coupling capacitor and the carrier terminal equipment, performs the primary function of tuning or resonating with the capacitive reactance of the coupling capacitor to provide a low loss path for carrier frequency between the terminal equipment and the power line. The combination of the line tuning equipment and coupling capacitor may be thought of as forming a filter of the band pass type, passing or offering a low loss path for the desired carrier frequencies or channels and rejecting or offering a high loss path for the power frequency and undesired frequencies in the carrier band.

The most commonly used line tuning equipment is available in standard units, having various arrangements of variable inductors and capacitors that can be combined to form resonant circuits for one or more channels in the normal range of 50 to 150KC.

In its simplest form, for a single frequency or channel, the line tuning equipment may consist of a single variable inductor

connected in series with the coupling capacitor to form a series resonant circuit for the carrier frequency used. Such a circuit is shown in Fig.(1.5) where for simplicity a ground return circuit is assumed. Since the portion of the circuit between the capacitor and the line tuning inductor operates at high carrier frequency impedance (to ground) it is highly desirable that shunt capacitance or leakage to ground in this lead be kept to a minimum for maximum efficiency. For this reason it is usually desirable to locate the line tuning equipment as close to the coupling capacitor as possible, in order to keep the length of this lead-in conductor to a minimum.

More recent practice is to install all terminal equipment indoors and to carry the circuit in from line tuning equipment through a special low loss concentric cable.

1.2.5. Transmitter-Receiver Unit:

The transmitter-receiver unit resembles a simple radio-telegraph transmitter and receiver. The transmitter consists of a master oscillator and a power amplifier. Its output is from 5 to 40 watts at a frequency which may be adjusted to any value between 50 and 150 kilo cycles per second. The output of receiver goes to the protective relays. Each receiver on a two terminal line is tuned to the same frequency as the transmitter at the other terminal. Either the same frequency may be used for transmission in both directions or a different frequency may be used in each direction if this is desired for the non relaying functions of the carrier channel. On a multiterminal line, however, all transmitters and receivers should be tuned to the same frequency so that each receiver will respond to the transmitter at any other terminal, and incidently to the transmitter at the same terminal.

1.2.6. Carrier-Frequency:

The frequency range from 50 to 150 kilocycles per second has been recognised as standard for power line carrier equipment for a number of years; for this reason, the bulk of application effort is devoted to carrier channels in this range only. There are several factors that should be considered in selecting a frequency for a new channel. If there are already carrier channels in use on the system or on adjoining interconnected systems, the question of possible interference with these other channels is usually of primary importance. The spacing of channels is largely dependent on the type of channels involved, the selectivity characteristics of the carrier receivers and the carrier power levels.

For some types of channels such as are used for single frequency party line telephone systems, reflections attributable to untrapped branch lines or short tap lines may limit the choice of frequencies that will give satisfactory transmission between all stations under a variety of line configuration conditions. Often, in these cases, it is necessary to make, circuit frequency characteristic measurements before the best frequency can be selected. For most medium and short transmission lines, however, reasonable judgement in the use of line traps will usually permit a wide choice of frequencies. In order to reduce the interference on the adjacent carrier systems to a minimum, a carrier frequency map should be maintained from which all new frequency allocations are coordinated.

1.2.7. Attenuation:

The attenuation or dissipation of the carrier frequency energy in the course of its transmission from a carrier transmitter at one terminal to a carrier receiver at another terminal

may be considered as analogus to voltage drop in 50 cycle power transmission. An attenuation of 40 db, is not uncommon in transmitting carrier energy over long lines. With this amount of attenuation, a transmitted power of 10W would appear at the receiver as only 0.001 watt. The principal attenuation components have been described in the following lines.

1.2.7.1. Attenuation in Lead-in Cable at Transmitter Terminal:

This component is the loss in the concentric cable between the transmitter terminals and the terminals of the line-tuning equipment or coupling equipment. When the line tuning equipment is located with the coupling capacitor and the cable is properly matched through an impedance matching transformer at the tuning unit, this loss is determined by multiplying the cable length by the attenuation per 1000feet indicated for the carrier frequency selected[8].

When both the terminal and the line tuning equipment are mounted together and are located near the coupling capacitor, no loss is included for this component.

1.2.7.2. Line Tuning and Coupling losses at Transmitter-Terminal:

The losses in the line tuning and coupling equipment will vary somewhat with the complexity of the tuning circuit and the frequency used. However, since this loss is small and usually less than one decibel, the usual practice is to take this loss as 1 db. The same holds good for such losses at the receiver terminal.

1.2.7.3. Transmission Line Attenuation:

The attentuation of the carrier energy, in transmission over the power line itself, is influenced by a number of factors, principal among these are size, spacing, insulation, and disposition of line conductors, the carrier frequency used, the type of coupling used, that is, whether it is ground return or interphase and so on.

For practical purposes, some of these variables can be neglected and others combined to form a set of curves[8], which give attenuation in dbs per mile of transmission line corresponding to the carrier frequency chosen.

1.2.7.4. Attenuation Attributable to Connected Power Apparatus:

Most high voltage power transformers appear to the carrier circuit as a relatively high capacitive reactance, and a line terminating in a transformer behaves at carrier frequencies essentially as though it were terminated in an open circuit. Such a small amount of carrier energy is transmitted through a transformer that it is seldom necessary to trap it. It is most convenien to include this small amount of loss in the line loss itself.

1.2.7.5. Attenuation in lead-in Cable at Receiver Terminal:

This loss is also considered in the same way, as the loss at the transmitter terminal as indicated previously.

1.2.7.6. Multiplying factors:

The increase in attenuation of a power line carrier circuit as a result of formation of ice, snow or frost on the line conductors and insulators has not as yet been determined accurately. However the most satisfactory method of accomodating these variations is through the use of multiplying factors[8] ranging nearly from 1.2 to 1.7.

1.3. TYPES OF CARRIER CURRENT RELAYING SCHEMES:

There are two main schemes to employ the carrier current relaying for the purpose of protection. These are, the Directional comparison and the phase comparison relaying. Each of these has been discussed in the following lines.

1.3.1. Directional Comparison Scheme:

Carrier pilot relay schemes of the directional comparison type

operate according to the following principle.

Upon the occurrence of fault, either in the protected section of line or in a nearby section, non directional fault detector relays are actuated at each line terminal through which power is fed to the fault. Each fault detector relay turns on the carrier current transmitter at its own terminal. If however, the directional relay at any terminal shows that the fault is flowing into the protected section, that relay turns off the carrier current transmitter. The presence of carrier on the line serves to block tripping at all terminals. During an external fault, power will flow out of the line at one terminal, and a carrier signal transmitted from that terminal will prevent tripping at other terminals, where power is flowing in. During an internal fault, on the other hand, power will usually flow into the line from all terminals, with the result that all carrier transmitters will be turned off and the relays at all terminals will be free to trip instantaneously. If, at the time of an internal fault, a breaker is already open at one terminal or if there is no power source there, then the fault detector will not turn on the carrier transmitter there, thus tripping will not be prevented by the fact that no power flows in at that terminal to make the directional relay turn off the carrier transmitter there. The pilot here is a blocking pilot, since the reception of a pilot signal is not required to permit tripping.

The directional comparison carrier pilot relay schemes in current use are built around standard 3-zone step type distance relays. These relays act in the usual manner to clear the first zone faults instantaneously, and for back up protection, to clear third zone fa-ults with time delay; but time delay is avoided for end zone phase faults through bypassing the second zone timer

contacts by carrier controlled contacts. Separate carrier and back up relays are used for ground faults.

1.3.2. Phase Comparison Scheme:

Phase comparison relaying equipment uses its pilot to compare the phase relation between current entering one terminal of a transmission line section and the current leaving the other. Like some pilot wire relays, this scheme utilizes a single phase relaying quantity, which is obtained by linear combination of the line currents through a filter circuit. The phase difference between the relaying quantities at the opposite ends of the protected transmission line determines whether the circuit breaker should be tripped. During normal conditions or during external faults, the currents entering the line at one end are substantially equal to those leaving the line at the other end, or in other words, the currents entering the line at one end differ in phase by approximately 180° from those entering the line at the other end. During an internal fault, however, the relaying quantities at the two ends of the line have some other phase difference (usually near zero). The existence, at either end of the line of a relaying quantity large enough to indicate the presence of a fault will trip the circuit breaker.

The existence of a fault of any type on the protected line or on a neighbouring circuit produces a large enough output from the filter to actuate a fault detector relay. This relay turns on the Carrier current transmitter, which, however transmits only during alternate half cycles. If the fault is external, the transmitter at the other end transmits during the half cycles when the local transmitter is inactive, and a blocking signal is received all the time, alternately from the near end and from the far end. If the fault is internal, the carrier signal received from the far end more nearly coincides

with the local signal, and there are substantial portions of each cycle during which no blocking signal is present. Under this condition, the local circuit breaker is tripped. The same action occurs at each end of the line unless the fault is fed from only one end. With feed from one end only, no carrier is transmitted from the other end, and the breaker there is not tripped, while at the feeding end, no blocking signal is received and the breaker is tripped.

Information regarding the phase angle of the derived current at each end of the system, is transmitted by a carrier signal modulated by square waves of equal mark/space ratio, the carrier is thus injected into the power lines at each end simultaneously in blocks corresponding to alternate half cycles at the power frequency. During the half cycles at each end when carrier is not being transmitted, tripping is locally effected unless it is blocked by carrier received from the remote end. An arrangement is commonly adopted in which the blocks of modulated carrier injected at each end are in phase opposition for the case of through fault; blocking carrier is thus received at each end during its tripping half cycle, and tripping does not take place in this condition. In the ideal case, the blocks of the modulated carrier appearing on the line from each end are coincident for the case of an internal fault; the circuit breakers will operate since no blocking signal is received during a tripping half-cycle at either end. These arrangements have been indicated in Fig.(1.6).

1.4. RELATIVE PROPERTIES OF DIRECTIONAL AND PHASE COMPARISON SCHEMES:

On the surface the directional comparison scheme appears more complicated, but this is because the back up elements are combined with the carrier elements. Disregarding back up elements, the directional comparison scheme has more mechanical parts and contacts

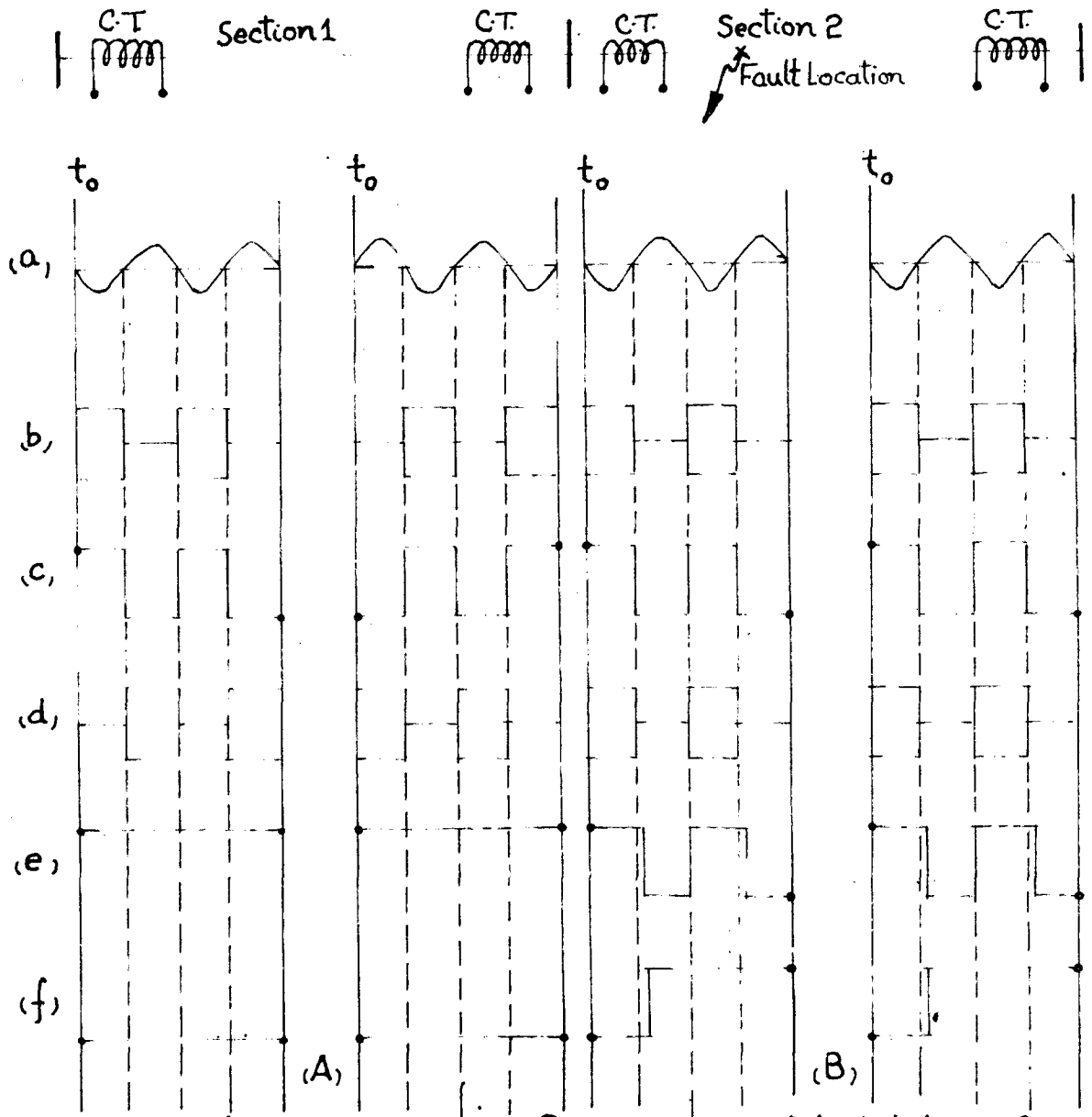


Fig 1.6 Arrangement of Carrier and Modulating Signals for a Phase Comparison Carrier Protection

(A) External Fault Condition.
(B) Internal Fault Condition.

(a) Fault Current.
(b) Local Transmitted Carrier
(c) Tripping Half Cycles.
(d) Received Carrier.
(e) Phase Comparator Output.
(f) Final Tripping Signal.

and fewer electronic circuits, while the phase comparison scheme has fewer mechanical elements and contacts and more electronic circuits. The choice of systems on this score alone is largely a matter of whether one prefers electronic or mechanical parts. On the basis of equivalent back up protection, the two systems occupy approximately the same amount of switchboard space.

The absence of inherent back up protection in the phase comparison scheme is an advantage in applications where the carrier system is used to supplement existing slower speed relays. There is merit in having two independent relay systems, with the phase comparison carrier system as the first line of protection and another system for backup.

A major advantage of the phase comparison system is that no potential transformers or potential devices are required for its operation. This advantage is nullified to a large extent if potential sources are already available or if the back up system requires potential sources. Distance type relays, whether used in the directional comparison carrier scheme or for back up protection require a source of 3-phase potential on the protected line or the associated bus.

Because the phase comparison system operates from the line currents alone, it is immune to out of step conditions. The current entering an unfaulted line section at one end is always equal to that leaving at the other, regardless of system swings. On the other hand, the distance elements used in the directional comparison scheme may operate on out of step conditions or system swings. This occurs whenever the impedance, that is, the ratio of voltage to swing current falls within the tripping area of the relay.

Other advantages of the phase comparison scheme are its immunity to false operation as a result of the following:

1. Zero sequence induction from parallel lines.
2. Unequal closure of C.B. Poles
3. Loss of potential due to blown potential transformer fuses or other causes.

However, directional comparison system is the best suited one for the protection of multiterminal lines, whereas, the phase comparison system has restricted application to multiterminal or tapped lines.

From the two basic systems, the relay protection engineer must select the system best suited to his particular application, taking into account such factors as economics, system operating requirements, previous experience, and the available indications of faults or troubles. It is these factors that make each relaying problem different from the previous ones and make protective relaying as much an art as it is a science.

C H A P T E R - 2

PHASE COMPARISON SYSTEMS

2.0. PHASE COMPARISON SCHEMES:

Phase comparison carrier current relaying itself can be divided into two types of systems, oneutilizing the thermionic valves and the other employing junction transistors. During the early years when the phase comparison carrier current was brought into practice for the first time, only thermionic valves were used, but, with the advancement in transistor technology, the transistorised scheme of phase comparison carrier current protection is coming up rapidly because of the inherent advantages of reliability, long life, quick operation etc. Both of these schemes have been described in the following lines.

2.1. PHASE COMPARISON SYSTEM EMPLOYING THERMIONIC VALVES:

Fundamentally, the operating principle of this system is exactly similar to what has been discussed in article 1.32 in Chapter 1. The relationship of various elements are shown in block diagram in Fig.(2.1) and Fig.(2.2) gives a simplified circuit diagram.

In order to obtain the best method of combination of individual phase currents into a single quantity for comparison, various sequence currents present during different types of faults are considered. Since the use of negative phase sequence current appears desirable for all types of faults, the equipment uses negative phase sequence network with provision for developing a network output on three phase faults as has been shown in Fig.(2.2). This provision consists of three phase-over current relays, operation of all three shifting the network so as to introduce a positive phase sequence component into the network output. Thus the equipment functions on three phase faults at a current magnitude above full load, but for unbalanced faults, phase currents of less than full load magnitude will cause operation.

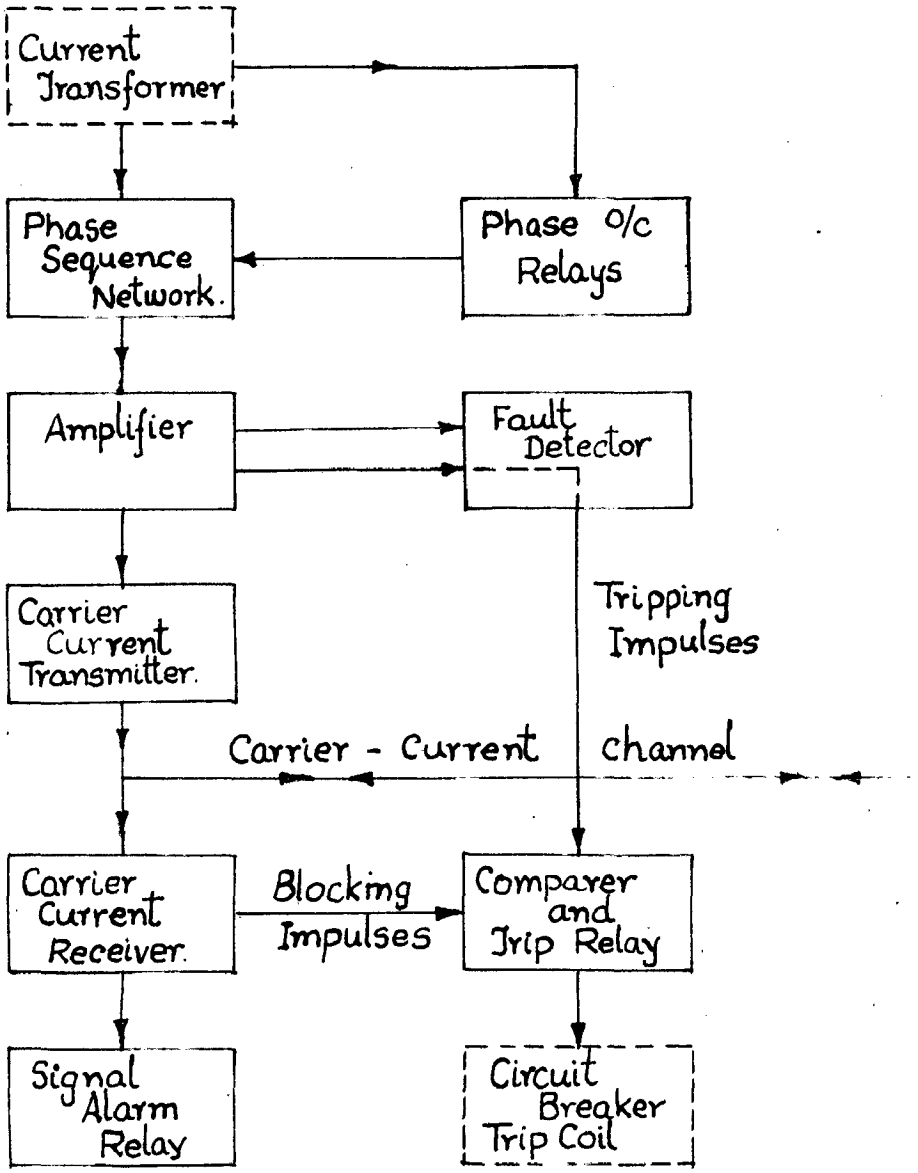


Fig 2.1

Block Diagram showing relations between elements of the Protective System.

Any relaying system for the general application must provide high sensitivity during ground fault conditions. If, because of possible unbalanced loading, the desired high sensitivity is not attained by means of negative phase sequence current alone, then, zero phase sequence current may also be used to obtain the desired network output. This will make the network output of the form $I_2 + KI_o$.

2.1.1. Description of the Relaying Equipment:

All of the tubes are of the type 25B6G like those used in the associated carrier current transmitter receiver. All the auxiliary relays except the seal in relay are of the telephone type operating at their normal contact pressures, thus ensuring reliability proved by long experience.

With reference to Fig.(2.2) the network is housed in a case and consists of transformers T_1 and T_2, resistors R_1, R_2 and R_3 and Capacitor C_1. T_1 and T_2 are fed from phases a and c respectively and R_3 and C_1 provide a 60^o phase shift of the output of T_1 so that, with balanced load, the voltage across C_1 is in phase with the output of T_2, which is then adjusted to equal magnitude by R_2, so that, the vector difference is zero. Zero phase sequence current is neutralized by ground-current windings, one of which has taps for adjustment of K. The output of such a network is proportional to negative sequence current and zero sequence currents only, and independent of positive sequence current. On a phase to phase fault, such a network gives the same magnitude of output voltage regardless of which pair of phases is involved. In order to provide for a three phase fault, overcurrent relays in the three phases, marked as O in Fig.(2.2) are so connected that if all three pick up, they change the setting of R_1 so as to unbalance the network and thus introduce

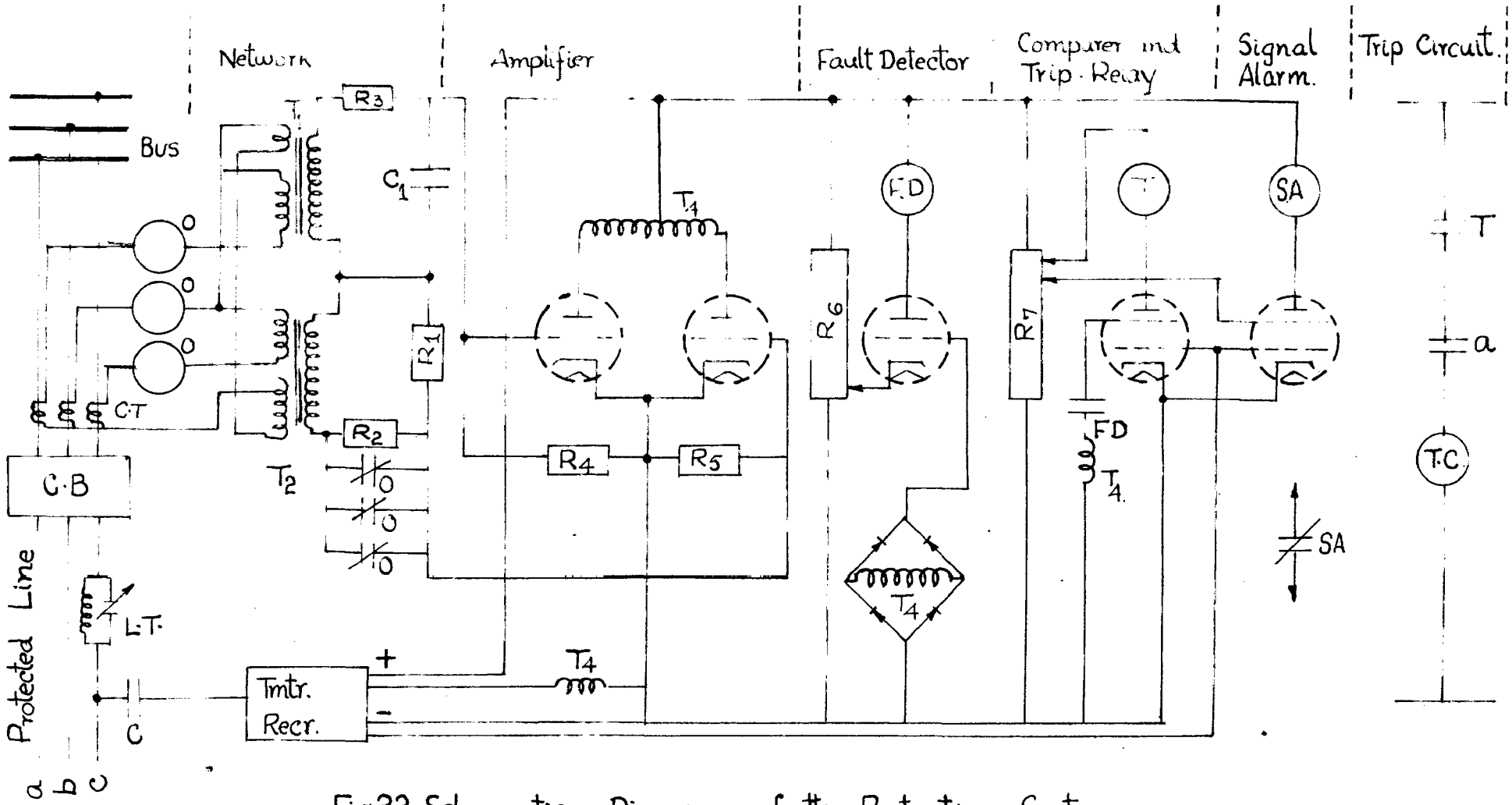


Fig 2.2, Schematic - Diagram of the Protective System

C - Capacitor
FD - Fault Detector
O - Phase Overcurrent Relay
R - Resistor.

SA - Signal Alarm Relay
T - Trip Relay
TC - CB. Trip Coil
T_1, T_2, T_4 - Transformers.

Tmtr. - Carrier Current Transmitter
Recr. - Carrier Current Receiver.

a positive sequence component in the output.

2.1.2. Amplifier:

The amplifier allows the use of low burden network by permitting it to operate into a high impedance, and provides energy to drive the carrier current transmitter. Also the amplifier output controls the fault detector and provides the comparer with a local voltage for comparison with the incoming carrier current signal. It consists of two tubes operating in push-pull through an output transformer which provides a match with the load resistance consiting principally of the transmitter screen grids.

2.1.3. Fault-Detector:

This element is necessary to ensure (on an external fault) that the network output is sufficient to drive the transmitter and produce an adequate blocking signal at the remote terminal, before permitting any attempt to trip. If the same carrier channel is used for communication, the fault detector also serves to transfer control of the channel temporarily from communication to relaying for the duration of a fault.

The fault detector, as shown in Fig.(2.2) consists of a voltage divider resistor, a full wave rectifier, a tube, and an auxiliary relay for its plate circuit. The rectifier is supplied from a separate winding on the amplifier output transformer. The use of fault detector tube permits compensation, by proper biasing, for the reduction of the amplifier output voltage with d.c. supply voltage, thus providing a fault detector pick-up which is substantially constant over an adequate range of d.c. supply voltage.

2.1.4. Comparer and Trip-Relay:

The comparer makes the decision whether to trip the circuit

breaker or not, depending upon the signals that it receives.

The comparer consists of a tube, a voltage divider resistor to adjust its plate voltage and the trip relay in its plate circuit. The tube is mounted on the relay auxiliary unit in the carrier cabinet to minimize the pick up in the lead from the carrier receiver to the comparer control grid. The other elements are mounted in the tripping relay case. A winding of the amplifier output transformer T_4, energises the screen grid of the comparer tube, positive relative to the cathode, during one half cycle, and negative during the other half cycle, During the positive-half cycle, the comparer tube will conduct and cause the trip relay to operate if no incoming carrier current signal during that half cycle causes a negative voltage (rectified carrier signal) to be applied to the control grid, thereby blocking tube conduction, and consequently, the trip relay operates.

2.1.5. Signal Alarm:

This element consists of a tube, a voltage divider resistor to adjust its screen grid voltage, and an auxiliary relay in the plate circuit. The screen grid voltage is adjusted so that the signal alarm tube normally carries enough current to pick up the signal alarm relay. When carrier current is received, the same negative voltage that served as blocking voltage in the comparer is applied to the control grid, reducing the signal-alarm plate current, thereby causing the auxiliary relay to drop out and close the external alarm circuit.

2.1.6. Carrier Current Transmitter-Receiver:

The transmitter is controlled by the voltage on the screen grids of the tubes, During standby conditions, this voltage is

zero and no carrier is transmitted. When 50 cycles excitation voltage from the network amplifier is applied to the screen grid circuit, the transmitter sends a signal on the positive half cycle and is definitely blocked during the negative half cycle of the excitation wave.

The carrier current receiver rectifies and filters the incoming carrier wave and thus provides a pulsuating D.C. blocking voltage which is applied to the control grid of the comparer tube. A twin diode tube is used in the receiver; one of the diodes is used for the relaying function while the other is used to drive an audio-amplifier for telephone or other service employing audio modulation. These diodes operate on opposite half waves of the carrier frequency cycle to obtain a balanced load on the receiver circuit and to reduce interaction between the two circuits.

2.2. PHASE COMPARISON SYSTEM EMPLOYING JUNCTION TRANSISTORS:

The problem of applying transistors to phase comparison carrier protection has been investigated extensively during the past few years. Although, in its operation, this scheme resembles the one using thermionic valves, yet there is a lot of difference involved in the circuitary. There is no question of taking normal electronic carrier equipment and replacing it with transistor equivalents. Substantial economy can be gained by this method, in addition to the advantages associated with power drain, h.t. and heater supplies and the final equipment has got the following features of major interest.

(a) It is wholly electronic from the starting circuit onwards, with the exception of the final slave relay, and consists of a number of separate functional units each arranged as a plug-in sub-assembly. In particular electromagnetic relay arrangements for control of

carrier starting and also for tripping, which are a normal feature of valve operated carrier systems, have been eliminated.

(b) Valves have been eliminated in all circuits including the transmitter- receiver circuit. The valve circuits of conventional carrier arrangements bear no affinity to the transistor circuits which have been used, and in many instances they have an entirely different functional role; transistors are used throughout as individual switches, as phase inverters and/or isolating stages, or as component parts of trigger circuits and only rarely as amplifiers and then in such a way that changes in gain are immaterial.

(c) Means have been adopted for ensuring uniform speed of operation for any fault within the protected section, irrespective of d.c. symmetry in the wave of the fault current.

(d) A method can be adopted for utilizing intertripping facilities in the event of marginal conditions, which comes in for certain phase angles and fault currents, and in the event of fault current being fed from one end of the protected section only.

(e) The system is designed for automatic resetting subsequent to fault clearance.

2.2.1. Operating Principle:

Fig.(2.3) shows a block diagram of the equipment at one end of the protected section. The outputs from the delta connected secondary windings of the main C.Ts. are fed to a sequence network which produces independent positive and negative sequence outputs. These components are fed in parallel to a starting circuit through isolating diodes. Whilst a combination of them is fed to the squaring circuit through a filter which eliminates any harmonic and d.c. transient which may be present. The starting circuit will pick

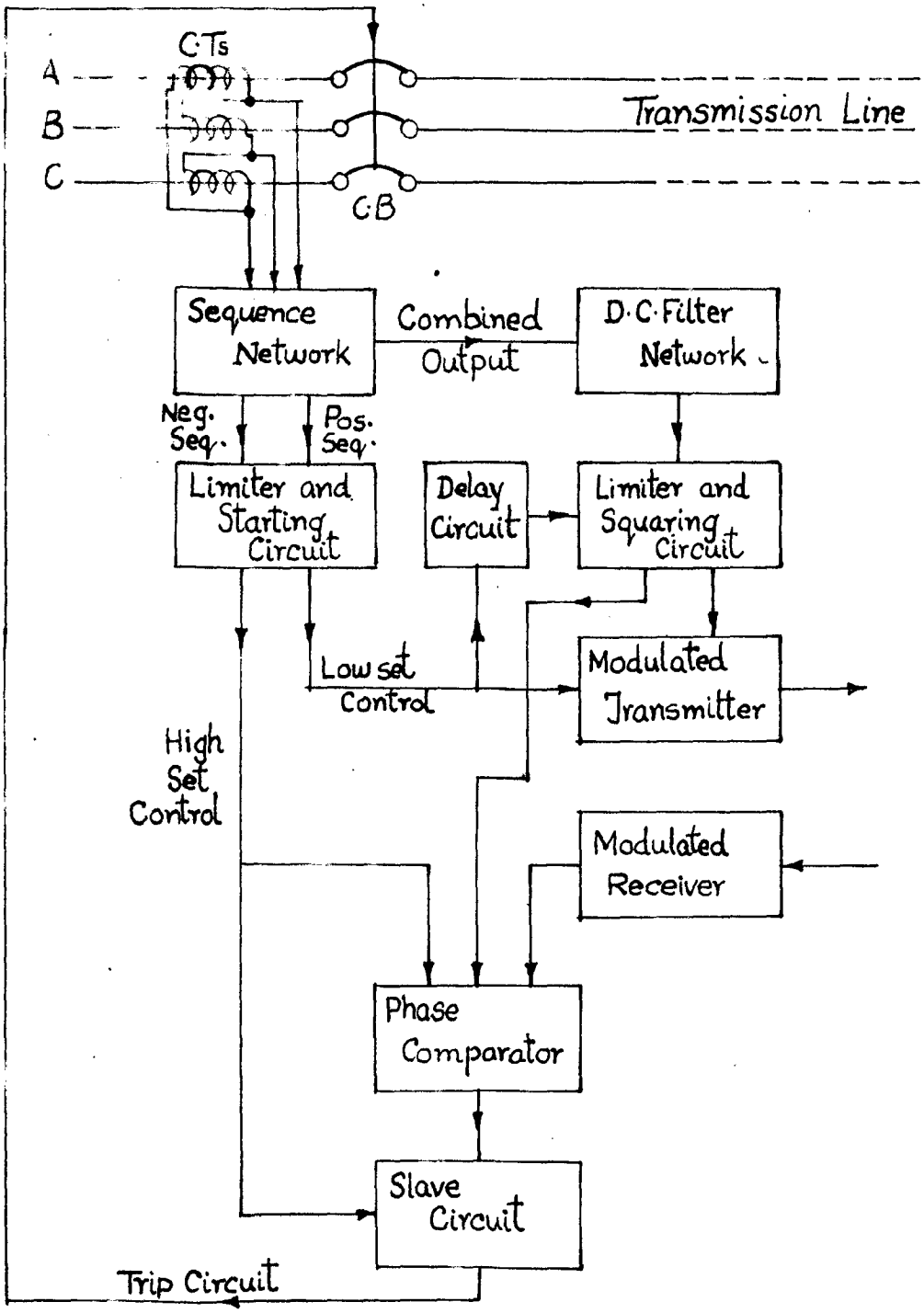


Fig 2.3

Block Diagram of the equipment for one Carrier Terminal

up when the amplitude of the negative sequence component exceeds a predetermined level, or alternatively, when both the amplitude and rate of increase of the positive sequence component exceeds a predetermined level. The only difference between these two starting arrangements is that, with negative sequence starting reset only occurs with fault clearance, whilst the other method has automatic reset after a predetermined time unless reset has occured earlier as a consequence of fault clearance. When the starting circuit picks up it produces four stepfunction outputs which are fed to delay circuit, modulated carrier circuit, phase comparator and slave relay circuit.

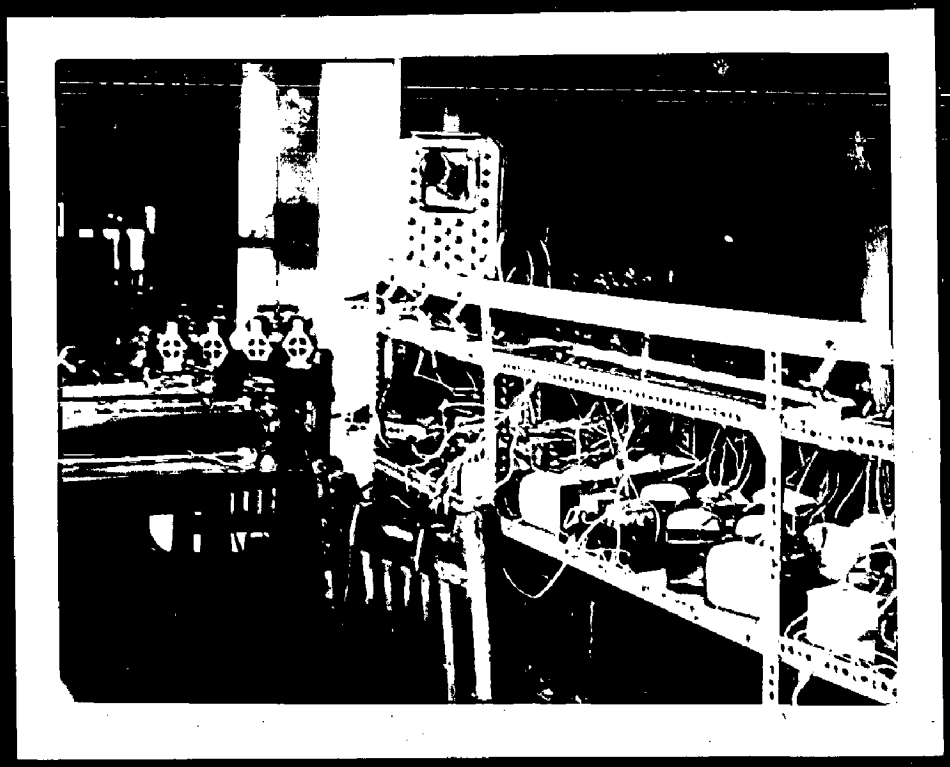
The starting input is preponderant throughout the apparatus; each individual unit which is controlled by a starting signal does not respond to any other input(s) unless starting has occured. The squaring circuit produces two square waves, one of these is fed to the modulated carrier control circuit and the other to phase comparato for comparison with the derived square wave from the remote end. The phase comparator decides whether the fault is internal and if so it produces output which when fed to slave circuit which must have received the starting signal, trips the circuit breakers. The starting circuit signal to the delay circuit causes, in its turn, to produce a time lagged output sufficient to allow clearance in the normal way. The delay circuit output is fed to the last stage of the squaring circuit, where it stops only the square wave fed to the modulated carrier control circuit. This together with the previous existence of the starting signal, causes continuous carrier to be transmitted which blocks tripping at the remote end, thus safeguarding against false tripping when an external fault is being cleared. The same sequence of events then occurs at the remote end and

continuous carrier is transmitted to the nearer and with the same effect.

2.3. PROBLEM UNDER CONSIDERATION:

A three phase, 120 mile long transmission line has been represented by a lumped inductance of about 15 ohms in each phase, which has been subdivided into three sections of 5 ohms each and further mid point of each has been tapped to vary the line reactance according to need. Similar impedance has also been chosen for the neutral wire. A three phase, 440V, 50 c/s power supply has been fed from both ends of the line throughthree phase contactors which close simultaneously through a closing switch. At the middle of the line, provision has been made to create any type of fault by a fault switch which operates a fault producing contactor. Indicating lamps to indicate the presence of the a.c. and d.c. power supply and the presence of a fault have also been provided. Line terminals have been taken out at the panel face so that the line connections can be modified and checked up, as and when desired. Similarly transmitter, receiver connections have been brought out, to check the presence of carrier signal whenever the need arises. A photograph of the so connected panel has been shown in Fig.(2.4).

The problem then is to design a transistorized phase comparison, Carrier output protection system for the above mentioned artificial line. Refering to Fig.(2.3) we see that the first step on our way, would be to design a sequential circuit which nicely represents the phase of the current combination at each end and also gives a suitable pick up signal to the starting circuit whenever a fault comes-in Three various combinations of sequence currents have been considered to select the best phase representing quantity, a detailed analysis of which has been given in Appendix A.1,and a graphic plot of the



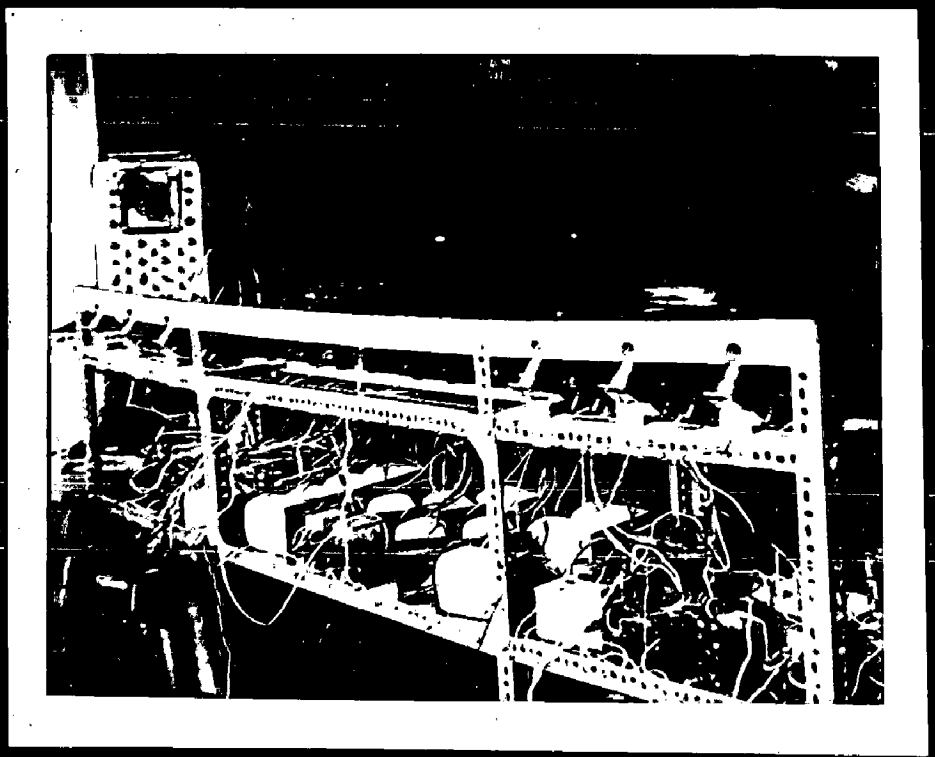


Fig.(B.4) Set up of the Corridor current relaying FEED PANEL.

same is shown in Figs.(A.11 to A.16). From these plots we may sum up as follows:

(i) Considering sequential combination $MI_2 + NI_1$ we see that the percentage output K (= $|I_s| / |I_F|$) increases as M is increased. However, the condition for K = 0 can be averted if proper values of M and N are chosen.

(ii) Considering the sequence combination $AI_2+BI_o+CI_1$, it is seen that K increases as either A or B is increased, but the increase in A gives more effective increase in the output than the increase in B. Here also K attains zero value for the two cases shown in Figs.(A.13a and A.14a) but this also can be avoided by properly selecting the values of A and C.

(iii) Looking into the sequence combination $BI_o + NI_1$ it is seen that K increases with increase in B, but it does not reach the levels obtained in the previous two cases. Moreover for double line to ground fault there is a sharp decrease in K, in an effective range of X_o/X_1.

Finally comparing the above three cases we find that the combination $BI_o + NI_1$ does not give satisfactory output for double line to ground faults and is hence rejected. In the second combination $AI_2+ BI_o + CI_1$, we find that value of K even decreases for some mid values of A and B for double line to ground fault. Moreover, the output leve does not increase beyond the one obtained with the combination $MI_2 + NI_1$ even for A = 10. Since one does not find much of advantage in including the component BI_o in $AI_2 + BI_o+CI_1$, it is economic to select the combination $MI_2 + NI_1$ which does not need any elements to derive the zero sequence current. However, we can easily avoid the condition of K reducing to zero by fixing values of M greater than 2.

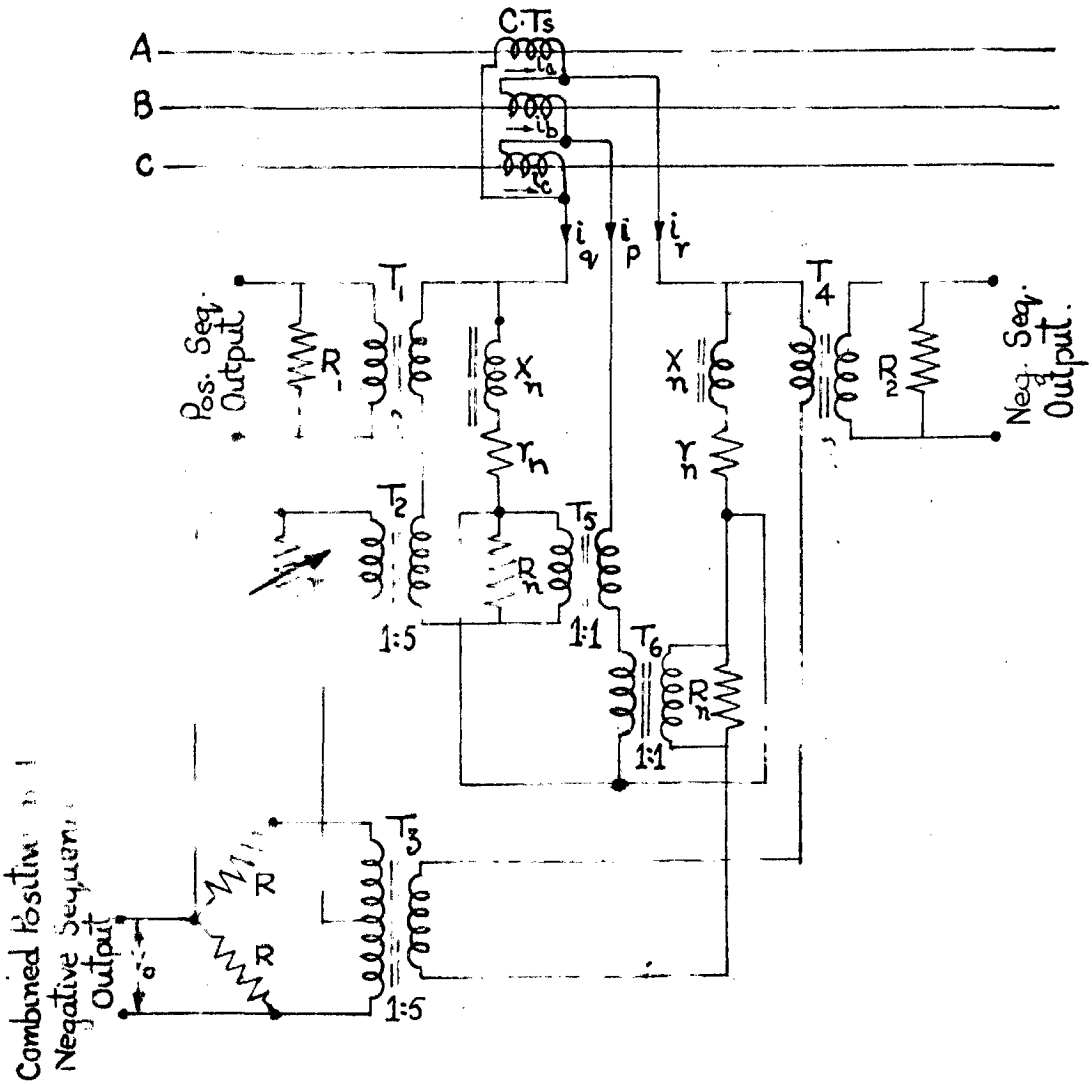


Fig 2.5 Sequence Network Arrangement.

Also, regarding the selection of N, we find that for N =+1 and X_o/X_1 =1(a case which can arise in practice) in Fig.(A.12a), K becomes zero. Hence N = -1 will be selected.

Summing up, $MI_2 + NI_1$ is the best possible sequence combination, and based on this output and the individual positive and negative sequence output that is needed for the starting circuit, a sequential circuit shown in Fig.(2.5) has been designed, the design details being given in Chapter 3.

Next, as is required in the problem, a transistorised scheme has been used to build up the starting circuit, squaring circuit, transmitter, receiver, phase comparator and slave circuit. A detailed report of this scheme has been given in Chapter 4. A carrier frequency of 100 Kilocycles has been used for both way transmission of carrier.

C H A P T E R - 3

DESIGNS

3.0. DESIGNS:

Based on the requirements of the terminal equipment for the carrier current phase comparison scheme under consideration, as has been described in the previous chapters, the design of each component has been considered in this Chapter. Although the results obtained in practice do not coincide with the calculated results exactly, yet provision has been made to obtain the outputs of various components according to the requirements. For example tappings have been provided in the Transactor secondaries, Line tuner etc. to obtain the desired results. All the C.Ts. have been designed for maximum possible burden. The design procedure has been described in detail in the following paras.

3.1. COUPLING CAPACITOR:

Keeping in view the factors necessary for the design of coupling capacitors, as has been discussed in Chapter I, the design of the coupling capacitor for the experimental problem under consideration may be carried out as under:

Line Voltage = 440 Volts.

Let C be the capacitance of the coupling capacitor, and let it be arbitrarily chosen as .001 μF.

∴ Impedance offered by the capacitor to power frequency 50 c/s.

$$= \frac{10^6}{2\pi \times 50 \times .001}$$

$$= \underline{3.18 \text{ Megaohms}}.$$

Impedance offered by the capacitor to carrier frequency 100 Kc/s.

$$= \frac{10^6}{2\pi \times 10^5 \times .001}$$

$$= \underline{1590 \text{ ohms}}$$

Now, if we put C = .002 μ F. the above two impedances change

to 1.6 mega-ohm and 800 ohm values respectively. If we increase the capacitance C to a value of 0.1 μF, we see that the impedance offered to power frequency is .032 megaohms and 16 ohms respectively. Keeping in view the advantage of higher Capacitance C, and the low phase voltage of 230V available for the experimentation, a current of 8mA can flow to ground at power frequency, which is quite negligible. Hence C has been chosen as 0.1 μF for the experiment.

3.2. DRAINAGE COIL:

To keep down the losses in the inductor, air cored type has been wound. Since, the current through the reactor will be of the order of a few milliamperes only, a 30SWG enamelled wire has been used to wind it.

A suitable value of the inductance to keep the carrier signal isolated from the ground and yet connected to the line, will be 100 mH.

We have,

$$L = \frac{0.03948\ a^2 n^2 K}{b}\ \mu H$$

where, a is the radius of the solenoid in Cms.

n the no.of turns.

K a factor depending upon diameter/length.

and b the solenoid wound length in cms.

Using the available former,

coil dia. = 7/4" $\therefore$ a = 2.22.cms.

Length b = 39/8" = 12.88 cms.

Dia./length = 0.359.

which gives value of K as 0.867 from tables.[14]

$$\therefore\ 100 \times 10^3 = \frac{.03948 \times (2.22)^2 n^2 \times 0.867}{12.38}$$

or $n^2 = 735 \times 10^4$

$\therefore$ n = 2720 turns.

The tested value of inductance given by the inductor =104mH. Two such coils have been wound, and each used at one end of the line.

3.3. LINE TRAP:

As mentioned already line trap will be a parallel combination of an inductor and capacitor, the design of which follows:

3.3.1. Reactor:

The value of inductance has been arbitrarily chosen as 2 milli-henries, and the value of capacitance needed will be considered on its bases.

A, Area of cross-section of the core = 3" x 3"

l, length of the winding = 6"

conductor size ... = 16 SWG

Now, $L = 1.26 \frac{\mu A}{l} \times N^2 \times 10^{-5} mH$

where A and l are in centimeter scale, and N is the number of turns to be wound for the reactor.

Since, the reactor will be an air cored one, we can take $\mu=1$.

$$\therefore 2 = \frac{1.26 \times 9 \times (2.54)^2 \times N^2 \times 10^{-5}}{6 \times 2.54}$$

$$\therefore N^2 = 41000$$

$$\therefore N = \underline{202}$$

3.3.2. Capacitor:

For parallel resonance, the capacitance C_{lt} of the parallel capacitor is given by-

$$C_{lt} = \frac{1}{4\pi^2 f^2 . L.}$$

f being the carrier frequency of 10^5 c/s.

$$\therefore C_{lt} = \frac{1}{4\pi^2 \times 10^{10} \times 2 \times 10^{-3}} \text{Farads.} = .00125 \mu F.$$

This value of Capacitance has been fulfilled by two available standard capacitors C_1 and C_2 in parallel, such that,

$C_1 = .001\ \mu F$ and $C_2 = 250$ pF.

3.4. LINE TUNER:

Since the line tuner must neutralize the impedance of the coupling capacitor at carrier frequency, we have-

$$\omega C = \frac{1}{\omega L_T}$$

where L_T is the inductance of the line-tuner.

$\therefore C = 0.1\ \mu F = 10^{-7}$ Farads.

$$\therefore L_T = \frac{1}{(2\pi \times 10^5)^2 \times 10^{-7}}$$

$$= 0.254 \text{ mH.}$$

To calculate the number of turns needed for this purpose, we have,

$$L_T = 1.26 \frac{\mu A}{l} \times N^2 \times 10^{-5} \text{ mH}$$

$$\text{or } N^2 = \frac{l L_T \times 10^5}{1.26\ \mu A}$$

$$= \frac{(.025)10^5}{1.26 \times 2.54} \quad \text{(taking A = 4 sq.inch \& l=4 inches)}$$

$$= 780.$$

$\therefore N = 27$ turns.

However, to make this inductor variable four tappings at intermediate values have been taken out, so that it matches the coupling capacitor perfectly. A 26 SWG wire has been used to wind the inductor.

3.5. COMPONENTS OF THE SEQUENTIAL CIRCUIT:

3.5.1. Delta Connected Current Transformer:

Based on actual creation of fault and the calculated values of fault currents, the following current magnitudes were obtained for different faults.

Phase to ground fault	...	15 Amps.
Phase to phase fault	...	25 Amps.
Double line to ground fault	...	27 Amps.
Three-phase fault	...	30 Amps.

Based on these values, now, a current transformation ratio of 1:5 has been chosen. Let the secondary burden for each of these C.Ts. be taken as 4 ohms maximum.

Voltage across the secondary for maximum current-

$$= 6 \times 4 = 24 \text{ volts.}$$

For further safety, let this voltage be taken as 30volts. Then from the e.m.f. equation-

$$V = 4.44\ B.A.N.f.10^{-8} \text{ Volts}$$

where,

N is the number of secondary turns.

B the flux density in lines/sq.inch.

A the area of cross-section of core in sq.inches.

f the frequency in cycles per second.

Taking B = 45,000 lines/sq.inch

A = 1 sq.inch

f = 50 c/s.

$$N = \frac{30 \times 10^8}{4.44 \times 45000 \times 1 \times 50} = 300.$$

$\therefore$ Number of primary turns, $N_p = \frac{300}{5}$

$$= 60.$$

Since the fault current is expected to flow only for a

short time, a 14SWG copper wire has been used to wind the primary winding of the C.T. and 19 SWG wire has been used to wind the secondary. The selection of 1:5C.T. ratio here, satisfies the design limits of transactors so that these need not be designed for transfer impedance of more than 4 ohms or so, which would otherwise increase the size of the transactor.

Maximum current flowing in each
phase of Delta connected C.T.secondary = 6 amps.

∴ Maximum, value of the currents

i_p, i_q or i_r ... $= 6\sqrt{3}$

$= \underline{10.4 \text{ amps}}$.

In the sequential circuit, resistance R_n has been chosen as 4 ohms (maximum) as this will directly from the burden for 1:1C.T. as shown in Fig.(3.5).

∴ $R_n = 4$ ohms

$R_n\underline{/60^\circ} = 4\ (\frac{1}{2} + j\ \frac{\sqrt{3}}{2})$ ohms.

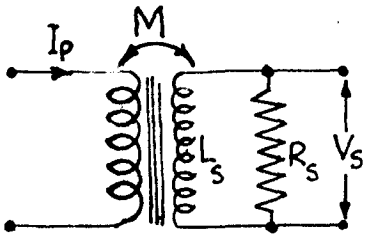
$= \underline{2 + j3.46}$ ohms

Now, to obtain a reactance of 3.46 ohms, an iron core reactor with adjustable air-gap and 300 turns of 20SWG super-enammelled copper wire has been constructed.

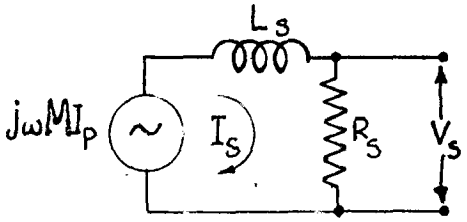
3.5.2. Transactors T_1 - T_4:

Transactor gives an output voltage (V_s) proportional to input current (I_p) or vice-versa. The ratio of voltage V_s to the current I_p is termed as transfer or Replica-Impedance Z_R say.

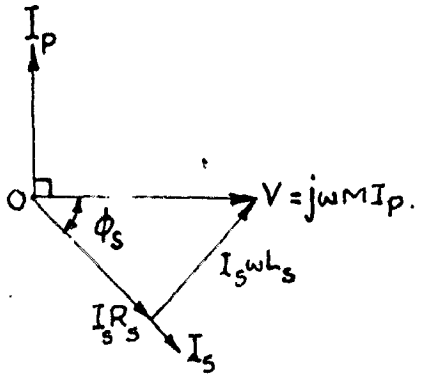
Referring to Fig.(3.1), the transactor secondary has been shown resistance loaded. From the diagram we can write the following equations.



(a) Circuit Diagram.



(b) Equivalent Circuit



(c) Vector Diagram

Fig 3.1 TRANSACTOR

$$Z_R = \frac{V_s}{I_p} \qquad \ldots \quad (1)$$

$$V_s = I_s \cdot R_s \qquad \ldots\ldots \quad (2)$$

$$I_s = \frac{j\omega M I_p \cdot M}{R_s + j\omega L_s} \qquad \ldots \quad (3)$$

where M is the mutual inductance between primary and secondary windings.

$$\frac{V_s}{I_p} = Z_R = \frac{j\omega M \cdot R_s}{\sqrt{R_s^2 + (\omega L_s)^2} \cdot \angle \phi_s}$$

$$= \frac{\omega M R_s \cdot \angle \pi/2 - \phi_s}{\sqrt{R_s^2 + (\omega L_s)^2}} \qquad \ldots (4)$$

Now, in equation (4) if $\omega L_s \lll R_s$, we can neglect L_s and rewrite equation (4) as-

$$\frac{V_s}{I_p} = Z_R = \omega M \angle \pi/2 - \phi_s \qquad \ldots (5)$$

Assuming unity coupling ratio between the two windings, we can write for mutual inductance M as:-

$$M = 1.26\ N_1 N_2 \cdot \frac{\mu A}{l} \cdot 10^{-8} \text{ Henries} \qquad \ldots (6)$$

where,

N_1 = no.of turns of the primary

N_2 = no.of turns on the secondary

A = the area of crossesection of the core in cm^2.

and l = length of core in Cms.

Neglecting the phase-angle in equation (5) we have:-

$$M = \frac{Z_R}{\omega} = \frac{Z_R}{314} \qquad \ldots \qquad \ldots (7)$$

Now, voltage V_s, as applicable to the starting circuit described in Chapter 4 must be of about 20 volt magnitude. Next, the selection of Z_R will depend on the magnitude of positive sequence

current and so we may write:-

$$Z_R = \frac{V_s}{I_1'}$$, where I_1' is the positive sequence current.

Now, Reactance of 1:1 C.T. = j 0.3 ohms.
(referred to secondary)

Parallel equivalent of R_n and this reactance -

$$= \frac{4 \times j0.3}{4 + j0.3}$$

$$= \frac{.02 + j0.3 \text{ ohms}}{}$$

Now, $I_1' = I_p \cdot \frac{4}{6 + j3.47} + I_r \cdot \frac{2 + j3.47}{2 + j3.77}$

Taking I_p as reference, $I_r = I_p \angle 120^\circ$ and considering the maximum value of the current:-

$$I_1' = 10.4 \ (0.05 + j0.5)$$

or $[I_1'] = 5.2$ amps. ... ... (8)

If current I_p is absent, as say in A-C. fault, then the fault current in the line will drop to 15 amps.:-

and $I_1' = 3\left(\frac{2 + j3.47}{2 + j3.77}\right)$

or $[I_1'] = 2.8$ amps. ... ... (9)

Based on the above values of I_1' we obtain Z_R equal to 3.8 and 7.0 ohms respectively. However, since the starting circuit picks up even at a voltage of less than 10 volts, let Z_R be chosen as 5.0 ohms which will be well within the margin for even the least fault-current.

From equation (7) therefore,

$$H = \frac{5.0}{314}$$

and from equation (6),

$$N_2 = \frac{4\pi \times 1 \times 10^8}{1.26 \times N_1 \times \mu \times A.}$$

Taking a gap length of 3 mms. and area of Cross-section of the core as I sq.inch.

$$N_2 = \frac{5 \times 10^8 \times 0.3}{314 \times 1.26 \times N_1 \times 1 \times 6.45}$$

$$= \frac{60 \times 10^3}{N_1} \quad \ldots \quad \ldots (10)$$

From equation (10),

for N_1 = 40 turns, N_2 = 1500 turns

for N_1 = 50 turns, N_2 = 1200 turns

and for N_1 = 60 turns, N_2 = 1000 turns

Super-enamelled copper wire of 18 SWG has been used to wind the primary and since a negligible current flows in the secondary, it has been wound with 30 SWG wire. Depending on the wire-size and window space available N_1 has been taken as 50 and hence N_2 as 1200. However, provision has been made to increase the air-gap upto 1.5 cms, the value of Z_R decreasing for increase in the air-gap. Moreover six intermediate tappings have been taken out on the secondary, so that appropriate value of Z_R is obtained.

The above data has been described for the design of transactor T_1 and the same holds good for T_4.

3.5.3. CTs. T_5 and T_6:

As shown in Fig.(2.5) we need 1:1 CTs. in the sequence network to transfer current i_p to positive and negative sequence networks. Since a maximum burden R_n of 4 ohms is connected across the secondary, it has been designed on the same basis.

Maximum value of i_p = 10.4 amps.

∴ Voltage across secondary ≃ 40 volts.

Again, taking Area A = 1" x 5/4" and B = 45,000 lines/sq.inch

$$40 = 4.44 \times 45{,}000 \times \frac{5}{4} \times 50 \times 10^{-8} \times N$$

$$\therefore N = \frac{160 \times 10^{8}}{4.44 \times 45{,}000 \times 250}$$

$$= \underline{320}.$$

Hence, both primary and secondary has been wound with 320 number of turns and a 18 SWG super enamelled copper wire has been used for winding.

3.5.4. CTs, T_2 and T_3:

Refering to Fig.(2.5) again, we find that the output voltage V_o depends on the way I_1 and I_2 are combined and also on the values of resistances r and R. This is also observed from equations (iii) and (iv) derived in Appendix.

Now, since the voltage V_o is to be fed to the squaring circuit, which also limits this voltage, its magnitude may be any where between say 10 volts and 30 volts. After looking into the various magnitudes and phase shifts in the currents I_1 and I_2 (for different types of faults), a CT ratio of 5:1 and a value 8 to 12 ohms for resistance R has been chosen, whereas resistance r has been made variable so that proper output is obtained with the variation in M.

(a) Considering first the transformer T_2, it is evident that its burden will depend upon the parallel combination of r and R/2, since at the mid point of the secondary of transformer T_3, the two equi-impedance paths of R ohms each are met by the portion of I_1 flowing to transformer T_3. If r is made infinite, burden on T_2 will simply be R/2 ohms and as r is decreased, this burden will go on decreasing. Keeping this in view a maximum burden of 6 ohms may be

considered for the design.

Maximum voltage across secondary = 6 volts.

Again from equation for e.m.f. already used, taking A = 1 sq.inch we can write,

$$6 = 4.44 \times 45{,}000 \times 1 \times 50 \times 10^{-8} \times N,$$

$$N = \frac{6 \times 10^{8}}{4.44 \times 45{,}000 \times 50}$$

$$= \underline{70 \text{ turns}}$$

Hence, no.of turns needed on the primary $= \frac{70}{5}$

$$= \underline{14 \text{ turns}}$$

Super enamelled copper wire of 18 and 26 SWG has been used to wind the primary and secondary respectively.

(b) Next, let us consider the design of $C.T._3$. It is clear from Fig.(2.5) that the burden for the secondary of this C.T. will be 23 ohms i.e. say 24 ohms.

∴ Maximum voltage across secondary = 24 Volts.

Again taking A = 1 sq.inch, we can write-

$$N = \frac{24 \times 10^{8}}{4.44 \times 45{,}000 \times 50}$$

$$= \underline{280 \text{ turns}}$$

Hence number of turns on the primary = 280/5

$$= \underline{56 \text{ turns}}$$

Super enamelled copper wire of 18 and 26 SWG has been used to wind the primary and the centre tapped secondary respectively.

It may be pointed out that such a type of centre-tapped current transformer and bridge connection has been chosen specially, in order that the feedback between positive and negative sequence outputs be avoided.

3.5.5. Filter Circuit:

The importance of filtering the combined positive and negative sequence output has been described in Appendix A.3. Let an inductance of 1 hendry be connected as shown in Fig.A.31.

The value of capacitance C_F that will be needed to match this inductance at power frequency is given by:-

$$C_F = \frac{1}{(2\pi f)^2 \times L} \text{ Farads.}$$

$$= \frac{1}{(2\pi \times 50)^2 \times 1} \text{ Farads.}$$

$$= \underline{10 \ \mu F}$$

Considering the available former section of 1 sq.in. cross-section, assuming an air-gap of 0.1 cm. and neglecting the ampere turns for iron path, the no. of turns N needed to wind the above inductor is given by-

$$N^2 = \frac{L. 1. 10^8}{1.26 \ \mu A}$$

$$= \frac{1 \times 0.1 \times 10^8}{1.26 \times (2.54)^2}$$

$$= 1000000.$$

$$\therefore N = \underline{1000 \text{ turns}}.$$

Since the current drawn by the inductor will be very small, a 30 SWG wire has been used to wind it. A 400 ohms shunting resistor has been used, so that the time constant of the parasatic oscillation is 8 milli-seconds, i.e. less than a half cycle. 3 more tappings have been taken to suit the capacitance perfectly.

C H A P T E R - 4

TRANSISTORISED CIRCUITS

4. TRANSISTORISED CIRCUITS:

Since the principle of transistors was discovered more than 15 years ago, there has been growing interest in this device. Experience has shown that when an application is made which keeps the transistors working inside their design limits, the reliability will be exceptionally good. It has been inevitable to consider transistors for use in power system protection as a means for increasing sensitivity, reducing operating time, and eliminating mechanical movement.

A review of the various kinds of relaying led to the conclusion that the phase comparison transmission-line protective relay offered an excellent opportunity to gain experience without introducing radically new concepts in operating principles and circuitry. The primary reasons for this are:

1. Transmission line faults occur more frequently than any other kind of fault.

2. The phase comparison relaying that was formerly used was based upon vacuum tubes, and these have met with disfavour because of their lack of reliability and tendency to change characteristics after a period of time.

An application of p-n-p type junction transistors has been made in all the terminal equipments described in the following lines. Transistors of the type OC71, OC76, 2SB75, 2SB77, 2N632, 2N363, 2N482, 2SA15 and 2SA12 have been used, the last two types being better suited for high frequency operation.

4.1. THE STARTING CIRCUIT:

As mentioned earlier, the starting circuit picks up in response either to the amplitude of negative sequence component of

the fault current for an unbalanced fault, or both the amplitude and rate of rise of the positive sequence component for a balanced fault. The complete starting circuit arrangement has been shown in Fig.(4.1.), where each of the negative and positive sequence components, as produced by the sequence network of Fig.(2.5) is rectified by a full-wave rectifier bridge. The rectified d.c. outputs corresponding to the negative sequence component are taken, at high and low levels of voltage, from the potentiometers marked H and L, which controls settings, and fed directly to the low and high set starting circuits, respectively, through isolating diodes. The rectified d.c. output corresponding to the positive sequence component are fed to pulse circuits, each consisting of a capacitor C and a discharging diode shunting this capacitor to $+V_B$ supply. Any sudden change in the positive sequence input signal is instantaneously produced at the output and subsequent decay of this output takes place as the capacitor charges. The diodes shunting the capacitors to the $+V_B$ supply cause them to discharge rapidly after fault clearance, thereby making pulse circuits ready to perform their functions immediately in any subsequent operation. The outputs of the impulse circuits are fed to the low and high set starting circuits through isolating diodes in the same manner as those corresponding to the negative sequence components.

The low and high set starting circuit arrangements are identical, apart from being fed from the low and high voltage tappings, respectively on the potentiometer settings. Each circuit consists of a level detector which has been shown as a common emitter trigger circuit, incorporating transistors VT_1 and VT_2 Fig.(4.1) followed by an output stage incorporating transistors VT_3 and VT_4. Each level

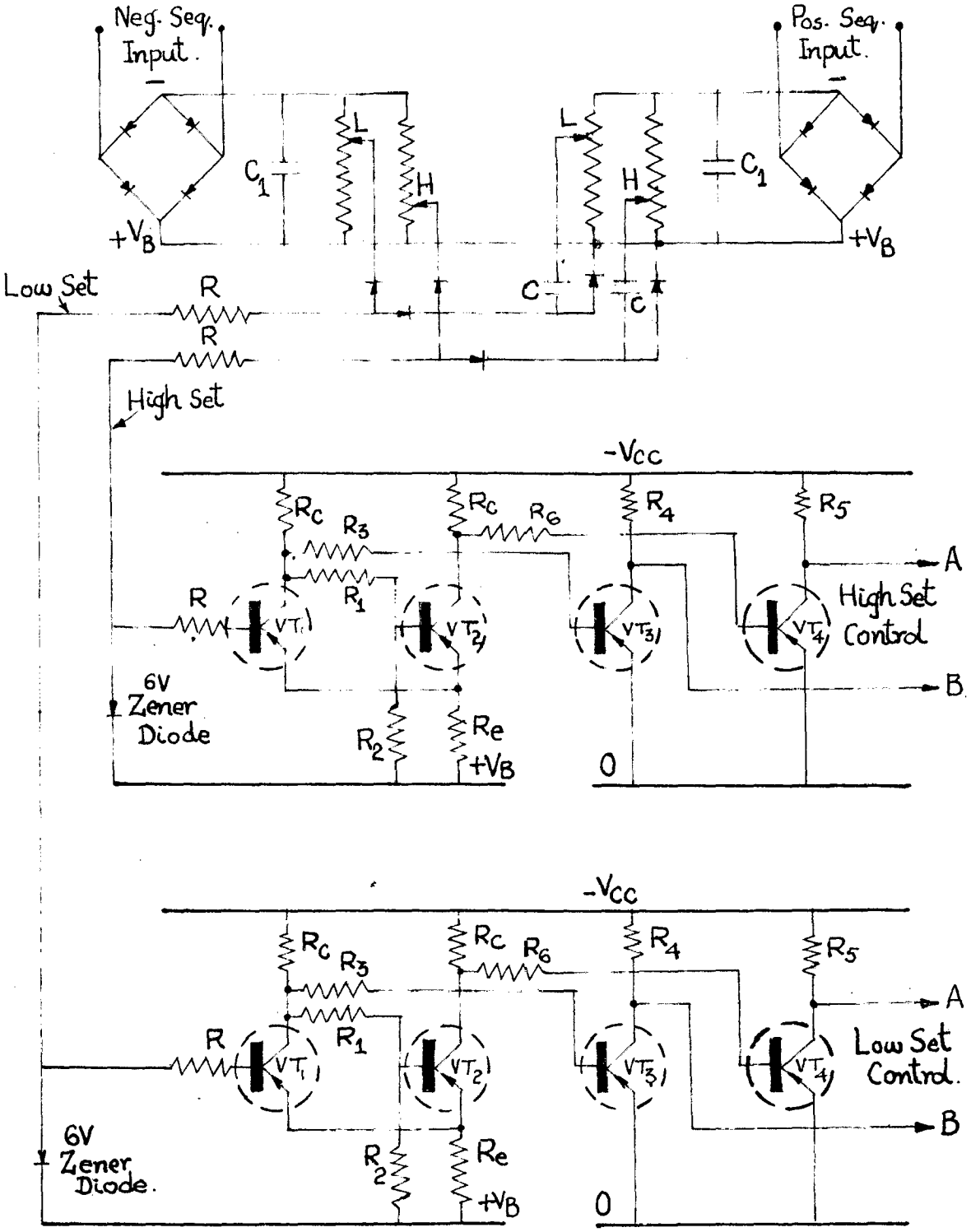


Fig 4.1

Starting - Circuit Arrangement

$R_C = 6.8K\Omega$, $R_1 = 15K\Omega$, $R_3 = 15K\Omega$, $R = 1K\Omega$, $C_1 = 80mfd.$, $V_{CC} = 15$ Volts, $R_6 = 22K\Omega$.
$R_e = 2.2K\Omega$, $R_2 = 39K\Omega$, $R_4 = 10K\Omega$, $R_5 = 10K\Omega$, $C = 20mfd.$, $V_B = 4$ Volts.

detector and output stage uses two transistors, i.e. a total of eight transistors, together with four isolating diodes, two discharge diodes and eight diodes which form the two rectifier bridges. It may be mentioned here that with the available IN38 diodes, the rectification was not perfect and these were finally replaced by a 24 volt, selenium rectifier. The pick up and drop out voltages of the level detector have been adjusted at almost same value by inserting proper values of resistances in the emitters of transistors VT_1 and VT_2.

When no starting signal comes at the base of transistor VT_1, during healthy condition, it does not conduct and voltage at its collector attains nearly -15 volts value, and this in turn triggers transistor VT_2 which conducts and hence the voltage at its collector attains nearly $+V_3$ voltage. This again, in turn, triggers transistor VT_3 which gives a zero volt output at B and since VT_4 remains non-conducting, a voltage of -15 volts appears at its collector and therefore at output A. Now, during faulty condition, a negative voltage signal comes at the base of VT_1 which makes VT_1 to conduct and hence VT_2 stops conduction. This makes the output at A to change from -15 to 0 volts and output B from 0 to -15 volts. Similar operation takes place in High set as well as low set control. A voltage of 6 volts appears across the zener diode during the receipt of pick-up signal. The use of this sudden change over of the voltage at control A and B and the separation of high set and low set control will be made clear at the following stages.

4.2. SQUARING CIRCUIT:

It is quite evident, that two isolated square wave pulses of unity mark/space ratio must be derived; one for modulation and the other as an input to phase comparator. To block the presence of

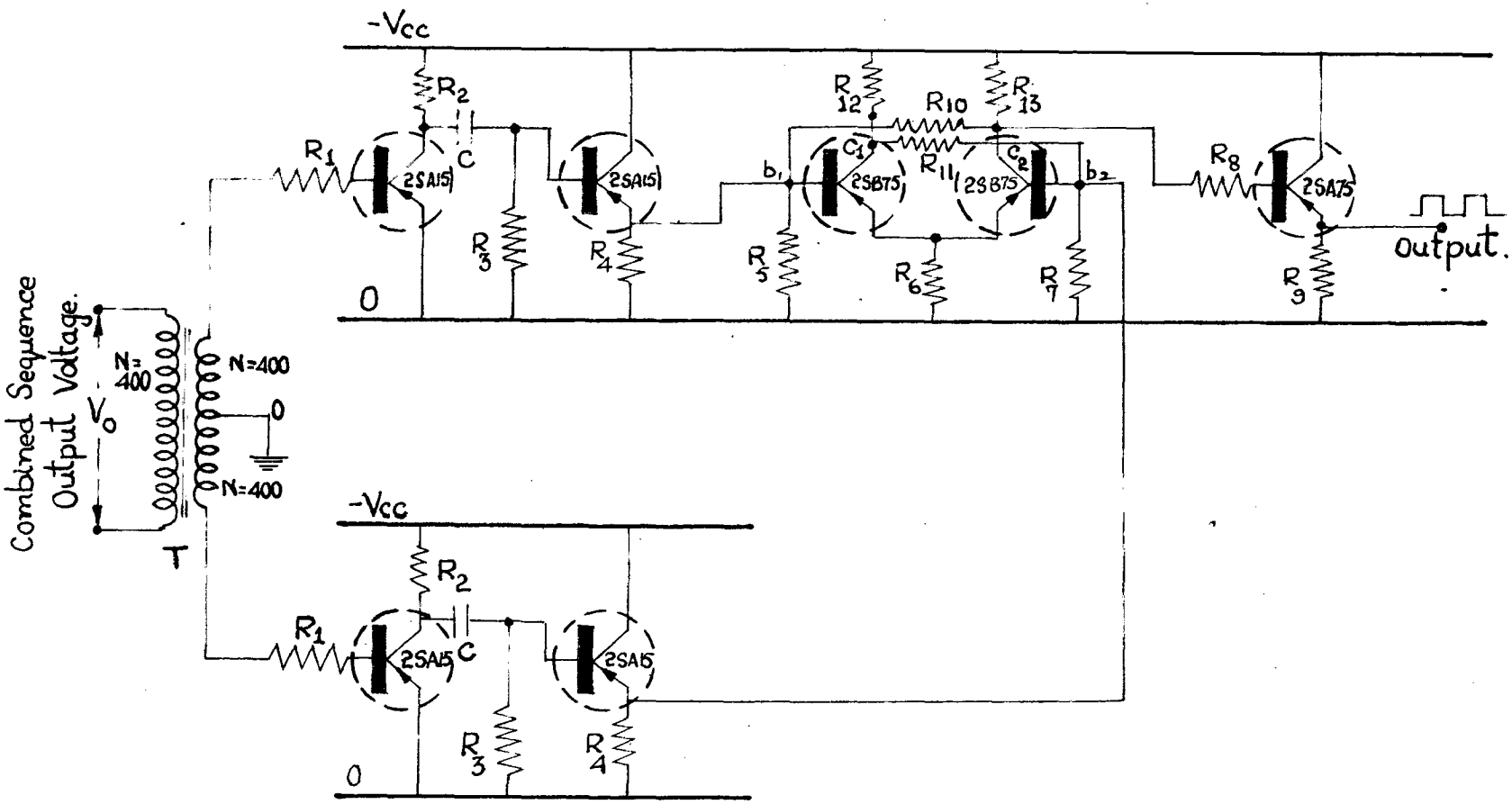


Fig 4.2 Squaring Circuit

$R_1 = 1k\Omega$, $R_3 = R_4 = 33k\Omega$, $R_6 = 1k\Omega$, $R_{10} = R_{11} = 22k\Omega$, $C = 460 P.F$,
$R_2 = 20k\Omega$, $R_5 = R_7 = 22k\Omega$, $R_8 = 1k\Omega$, $R_{12} = R_{13} = 8.2k\Omega$, $V_{cc} = 15$ Volt, $R_9 = 10k\Omega$.

any d.c. in the output ($KI_2 + I_1$) of the sequence network, it has been shown in Appendix A.3, that the elimination of transient time delay can reduce the overall operating time. This has been achieved by means of a filter circuit described in Appendix A.3 which has been connected between the sequence network and the squaring circuit.

A single transistor stage was initially used to obtain the square wave output, but it was observed that the width of the output wave changes with the change in the input sine wave magnitude. Hence a more stable type of squaring circuit which uses a bistable output stage, which has been shown in Fig.(4.2), has been used.

The squaring circuit used has been described in the next few lines. The combined sequence output voltage is transformed to obtain two sine waves of opposite polarity by centre- grounding of the secondary of transformer T. These two sine waves are fed to the bases of the pulse circuits, the pulse circuits being composed of two transistor stages coupled through a capacitor. The output of the pulse circuits is fed to the Bistable-circuit at bases b_1 and b_2 which gives a perfect square wave of 1:1 ratio at collectors C_1 and C_2. It may be mentioned that the square waves at C_1 and C_2 are 180^o out of phase with each other. One of the waves can be used as local square wave and the other used for carrier modulation. By feeding the local square wave from collector C_1 or C_2, to the phase comparator, it was observed that because of loading effect, the square wave changes its form. Hence, it was decided to use an emitter follower circuit for obtaining the local square wave signal as shown in Fig.(4.2) at the output stage, and the modulating signal has been derived from the collector C_1. By the provision of transformer T and the two pulse circuits, the width of the square wave has been reduced to ensure

quick operation.

4.3. CARRIER TRANSMITTER CIRCUIT:

The carrier control and modulation consists of the oscillator and the control arrangements for both modulated and continuous carrier. Control is obtained through the use of transistors with a common emitter circuit as shown in Fig.(4.3). A crystal oscillator of 100 Kc/s, caliberated at 35°C, has been used between the collector of VT_2 and base of VT_3 as shown in the figure. When transistor VT_1 does not conduct, transistors VT_2 and VT_3 behave as the oscillator, oscillating at a frequency of 100 Kc/s. The starting signal is normally negative, but when the starting circuit picks up, a zero voltage comes at the base of VT_1 thus operating the oscillator circuit. The modulated carrier output is finally amplified and tuned by sliding the core of output transformer I.F.T. Final adjustment of tuning is made after transmitting the carrier signals on the transmission line by sliding the core and by the variation of capacitances C_1 and C_2.

It may be pointed out that the I.F.T. that has been used at the output, is of the type used in Radio circuits, which has a separate core for primary and secondary. In the oscillator circuit in question, if a single cored I.F.T. could be available, the output would have been further increased. The transistor VT_1 is of 2SB75 type and VT_2 and VT_3 are the high frequency 2SA12 type. The collector voltage V_{cc} of -15 volts has been used from the common D.C. supply source.

4.4. RECEIVER CIRCUIT:

A full wave rectification has been used to demodulate the received carrier signal as shown in Fig.(4.1). It utilizes four 1N33 diodes which have been connected in a bridge circuit as shown.

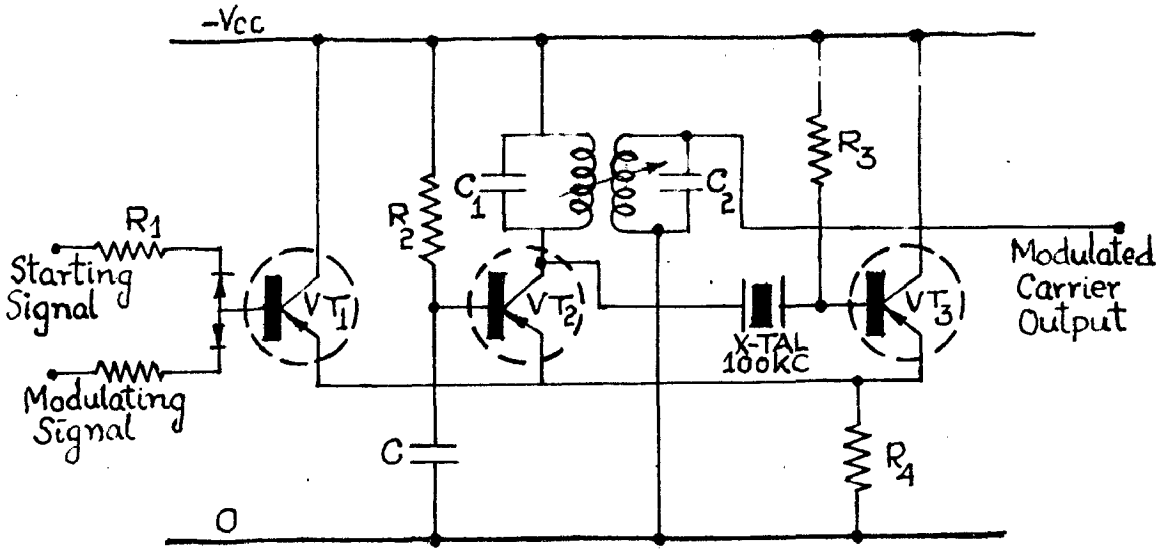


Fig 4.3 Transistor Arrangement for Carrier Control - and Modulation

R_1=3.3KΩ, R_2=220kΩ, R_3=100kΩ, R_4=2.2kΩ, C_1=330PF, C_2=680PF, C=0.5μF, V_{cc}=15 Volts. VT_1 is of 2SB75 Type. VT_2 and VT_3 are of 2SA15 Type.

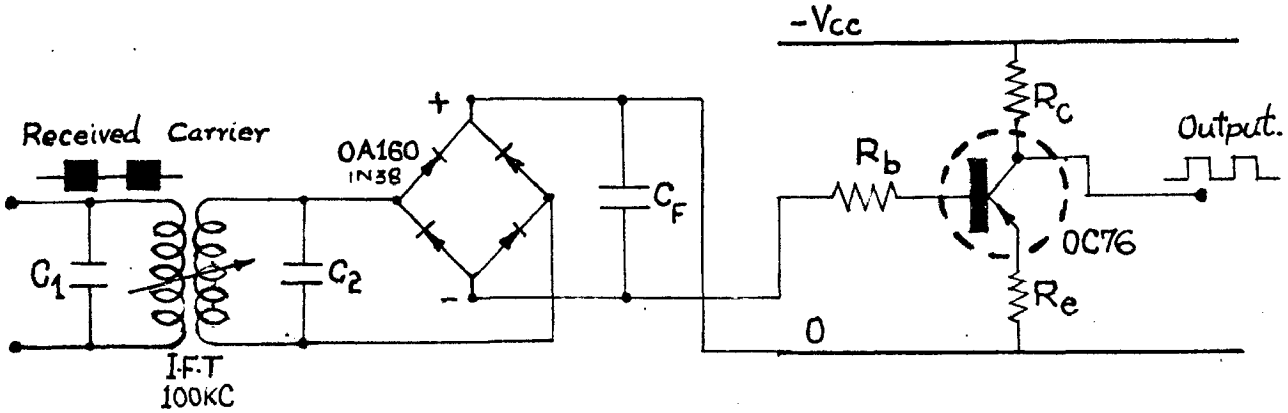


Fig 4.4 Receiver Circuit Arrangement

C_1=470PF. C_2=720PF. C_F=.05μF. R_b=1KΩ. R_c=15KΩ. R_e=2KΩ.

Because of the effect of line attenuation, it is observed, that the amplitude of the modulated carrier at receiver is quite less than the amplitude of the modulated carrier at the transmitter end, and hence the rectified square wave is also quite less in magnitude than the local square wave with which it is to be compared in the phase comparator. The magnitude of the demodulated square wave is hence magnified by the amplifier circuit shown in Fig.(4.4), but it may be mentioned here that it gives a phase reversal of the original square wave. Hence the modulated carrier of correct polarity is to be chosen at the transmitter end. The gain of the amplifier is increased by increasing the collector resistance or by shunting the emitter resistance by a suitable capacitor.

Finally the demodulated and amplified (if found necessary) square wave is fed as one of the inputs 2 and 3 to the phase comparator as shown in Fig.(4.5), to be compared in phase with the local square wave as described in the next section.

4.5. PHASE COMPARATOR CIRCUIT:

As has been already said, the phase comparator compares the locally obtained square wave with the one received from the other end of the line after demodulation and decides whether tripping of the circuit breakers should take place or not depending on whether the fault is internal or external. Of course, the starting signal is also received at the time of comparison. If the fault is external, the two above mentioned square waves are 130^{o} out of phase and hence the phase comparator gives no output. In case of an internal fault, these waves are almost in phase with each other and depending upon their angle of coincidence, pulses are obtained at the output.

Fig.(4.5) shows the circuit connections of the phase comparator

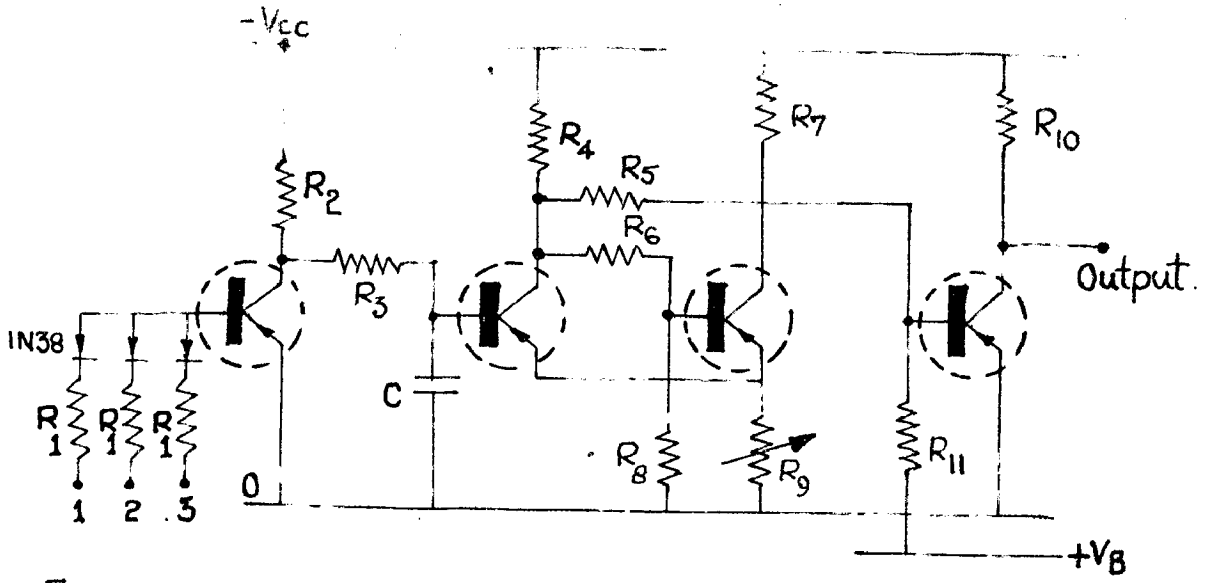


Fig 4.5 Phase Comparator Circuit

R_1=3·3kΩ, C=0·5 mfd. R_6=15 kΩ, R_9=2·2kΩ,
R_2=20kΩ, R_4=10kΩ, R_7=10kΩ, R_{10}=10kΩ,
R_3=2 kΩ, R_5=15kΩ, R_8=39kΩ, R_{11}= 39 kΩ.

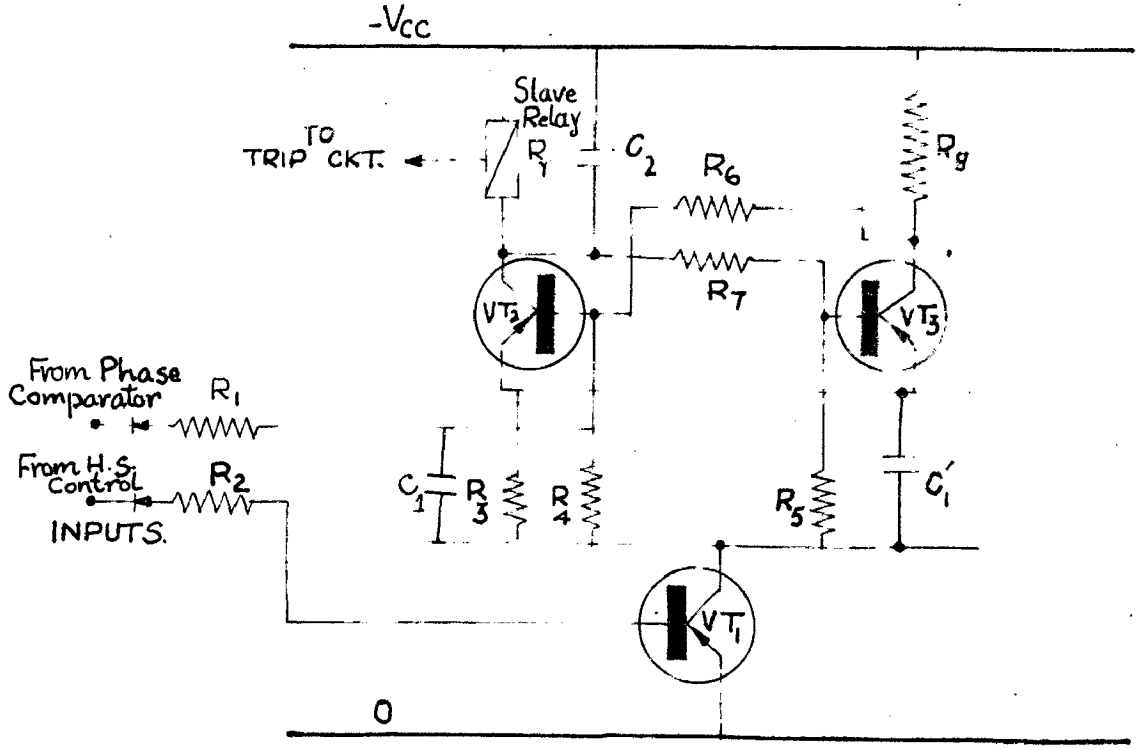


Fig 4.6 SLAVE CIRCUIT

R_1=15kΩ, R_4=R_5=10kΩ, C'_1=0·5μF
R_2=22kΩ, R_6=R_7=5·6kΩ, C_2= 1 μF.
R_3=100Ω, R_8=R_9=3·6kΩ, V_{CC}= 15 Volt

VT_1, VT_2 & VT_3 are of 2SB75 type
C = 1 μF

circuit. It consists of a coincidence stage controlled by the starting input, followed by an integrating circuit and a level detector/ output stage. Three inputs are fed to the base of the input transistor. Input 1 is from the high set control of the starting circuit and is normally negative, thus maintaining the transistor 'on' irrespective of the inputs 2 and 3. When the starting circuit picks up, input 1 assumes zero potential, thereby allowing comparison in phase of the signals 2 and 3. When either of these waves is of negative potential, the transistor at the input will still conduct. And, when both are positive or zero, with the starting input zero, the transistor will be cut off. This gives negative pulses at the output and the duration of the pulse depends upon the angle of coincidence of 2 and 3. A straightforward RC integrating circuit has been used between the coincidence and the level detector stage.

In the experimental circuit under description, the phase shift introduced into the carrier signal, due to long line lengths or shunt capacitance, has been neglected. In an actual circuit the phase angle setting for the phase comparator is made approximately 30°. However, the operation of the phase comparator with artificial line capacitance was also found to be satisfactory.

4.6. SLAVE CIRCUIT:

The basic arrangement of the slave circuit has been shown in Fig.(4.6). A switching transistor VT_1 maintains the slave circuit in a normally unenergized condition, since the starting signal received at its base is normally zero. Because of the supply of a fault, when the high set control of the starting circuit picks up, it brings a negative signal at the base of transistor VT_1 and hence it conducts, thus the circuit remains in a 'ready' condition. It also follows that the resetting will take place automatically after the fault clearance,

since the normal signal (zero voltage) from the starting circuit, i.e. when the system is healthy switches off the transistor VT_1.

The asymmetrical bistable circuit operating the final slave relay consists of transistors VT_2 and VT_3. These are arranged so that, with the circuit first energised, transistor VT_3 conducts and VT_2 is cut off. But, when a negative tripping pulse is obtained from the phase comparator circuit and applied to VT_2, it conducts and VT_3 cuts off. This makes the slave relay to operate. Since the operation of slave relay opens the normally closed contacts of the circuit breaker magnet coil, the breaker trips.

The 3.6K ohms resistance in the collector of VT_3 has been matched with the relay coil resistance which is also 3.6K ohms. The input capacitor C_1 ensures circuit stability against parasitic pulses during fault conditions. Transistors VT_2 and VT_3 are of 2N363 type and VT_1 is of OC71 type. The collector voltage V_{cc} has been increased to 21 volts, since the slave relay at one end of the line could not pick up for V_{cc} = 15 volts.

Starting signal for the slave circuit has been derived from high set control, such that, no operation due to normal load current is ensured. The same reasoning applies to the phase comparator circuit.

C H A P T E R - 5

TESTING AND PERFORMANCE

5.0. TESTING AND PERFORMANCE:

The procedure adopted while testing the whole equipment along with the explanation of its performance with the help of oscillographs has been described in this Chapter.

5.1. TESTING:

After assembling each component of the terminal equipment, in accordance with what has been described in the previous Chapters, each individual component has been initially tested from a low-voltage single phase power supply obtained from a variac. All the transistorised components right from the starting circuit to the slave relay circuit gave satisfactory performance without any transistor getting heated up or damaged. Outputs of all the components have been brought out to banana sockets which made plugging-in with the other components easy. After such an individual check up, all the components have been interconnected in accordance with the block diagram shown in Fig.(2.3) and two views of the complete test panel set has been shown in Fig.(2.4).

After plugging in all the components of the sequential circuit at each end of the line, the line was energised by pressing the line- energising press-button. Fault switch was closed at the next instant, and output voltages from positive, negative and combined positive and negative sequence networks were checked. A slight adjustment has been made in the original settings of rheostats to obtain the suitable values of these voltages at both ends of the transmission line, for all types of faults. Next, the outputs of the sequential circuit were fed to the respective feeding points in the starting circuit and the squaring circuit. Fig.(5.1.1.) shows a section at the one end of the test panel, wherein, C.Ts. of the sequential circuit are shown at the left

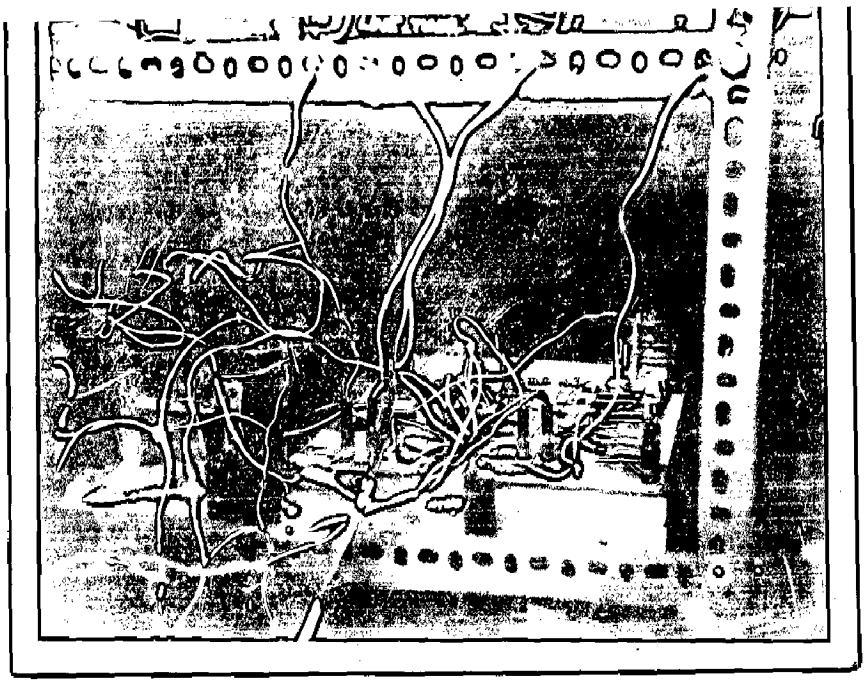


Fig.(5.1.1.) Components of the sequential circuit and the starting circuit, at one end of the line.

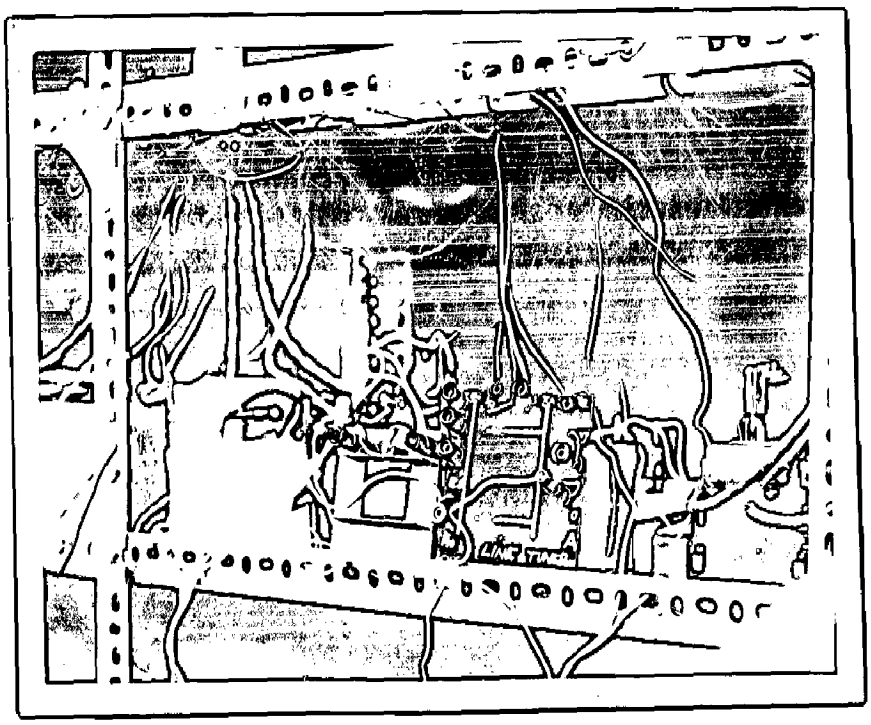


Fig.(5.1.2.) Components of terminal equipment including the slave relay and circuit breaker at one end of the line.

hand, and the starting circuit at the right hand. Fig.(5.1.2) shows some components of the carrier terminal equipment at one end of the line, including the slave relay at the right.

All types of faults were simulated at the mid point of the transmission line by means of a fault switch operating a fault simulating contactor and the presence of a fault was indicated by a fault indicating red neon lamp. Soon after the inception of the fault on the protected line simultaneous tripping of the breakers at the two ends of the line was observed. No tripping was observed for simulating external faults.

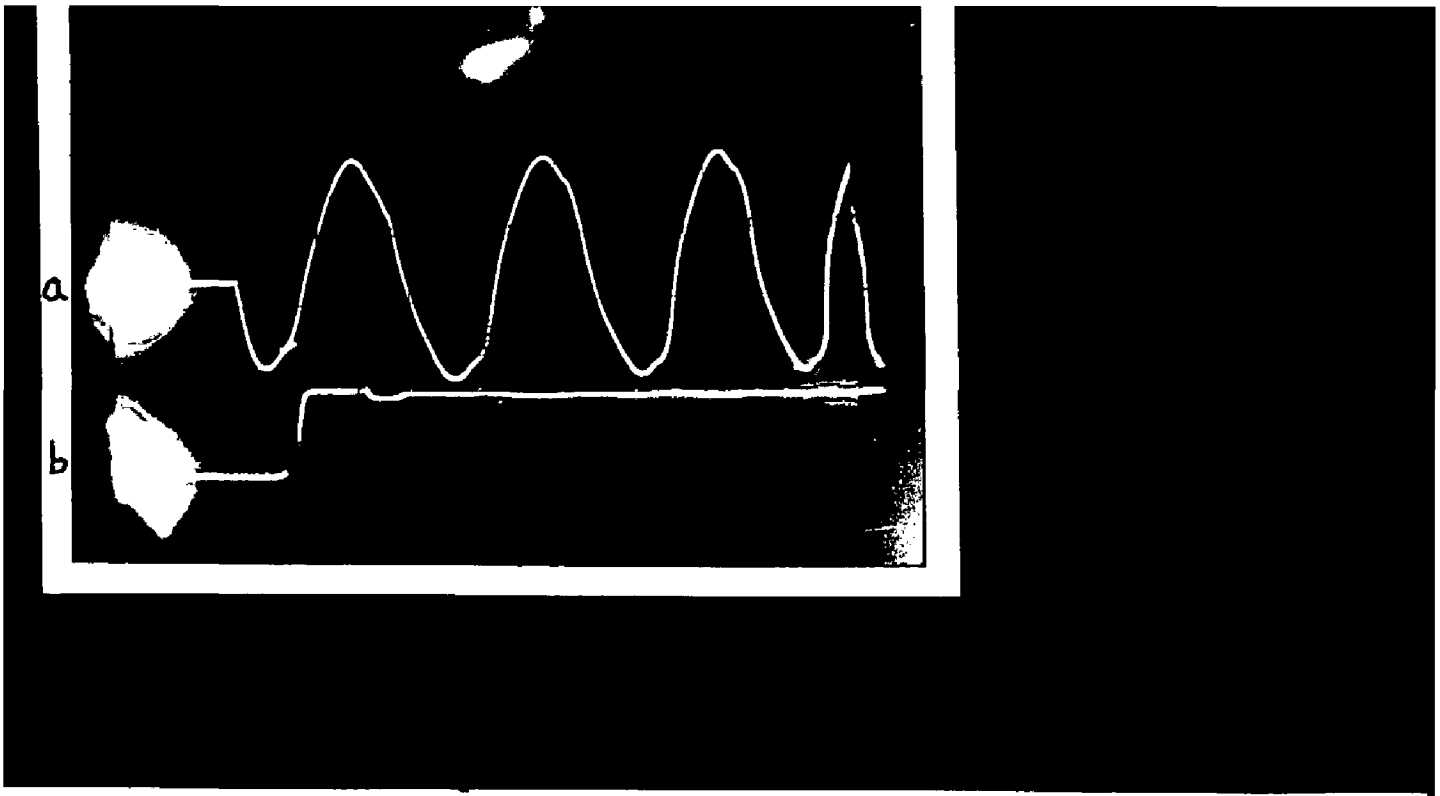
5.2. PERFORMANCE ON INTERNAL FAULTS:

Figures (5.2.1.) to (5.2.7.) illustrate the performance of the above described equipment, as observed under exhaustive laboratory testing.

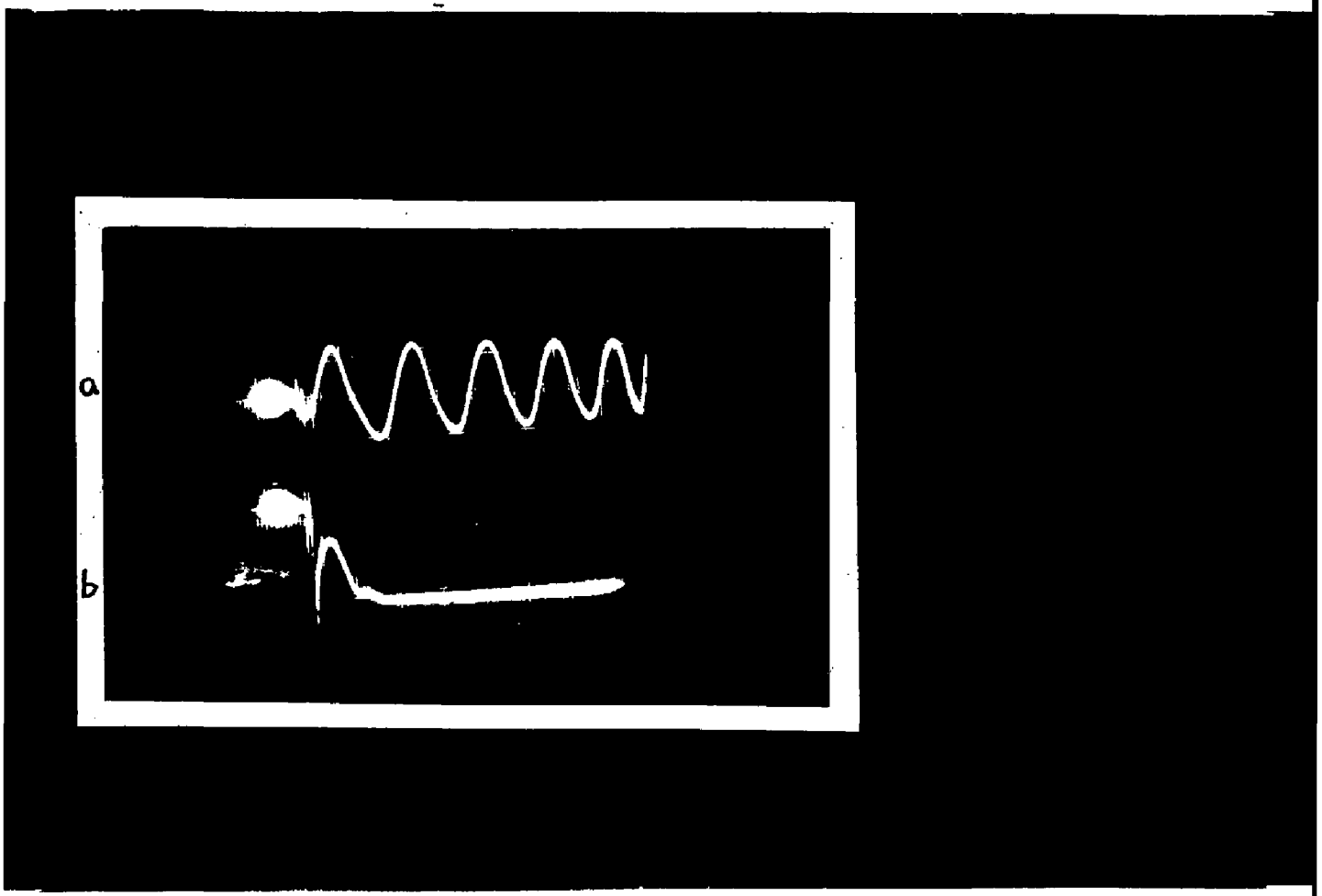
The starting circuit pick up is virtually instantaneous as may be seen from Fig.(5.2.1.) where comparison of the high set starting circuit pick up has been made with the fault current signal. During balanced faults, the starting circuit operates on receipt of the pulse inputs from positive sequence output, which has been shown in Fig.(5.2.2.).

Two out of phase, perfect square waves of 1:1 ratio are obtained from the squarring circuit outputs at C_1 and C_2 as shown in Fig.(4.2). One of these square waves has been shown in Fig.(5.2.3b), which is used as a modulating signal input to the carrier transmitter circuit and the resulting modulated carrier signal has been shown in Fig.(5.2.3.a).

Fig.(5.2.4) shows the transmitted and received modulated carrier signals at one end of the line. A slight phase shift



5.2.1.) (a) Fault current wave,
(b) Pick-up of the starting circuit.



5.2.2.) Starting circuit pick-up for a balanced fault.
(a) Fault current wave,
(b) Pick-up of the starting circuit.

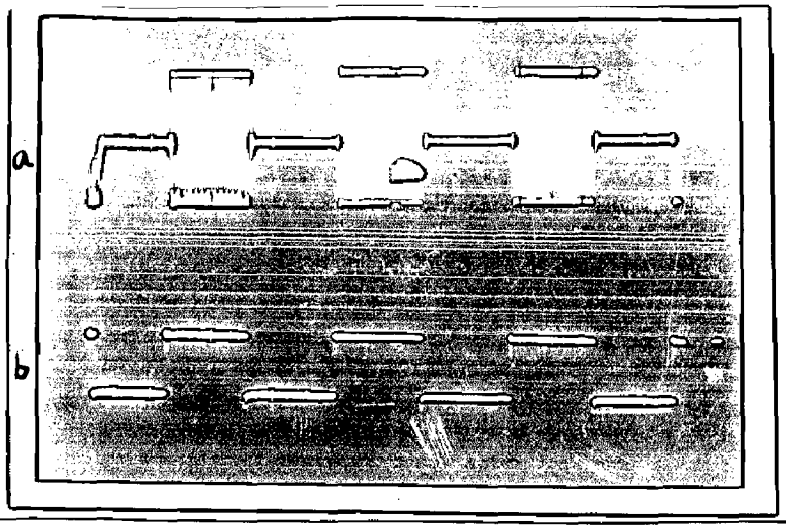


Fig.(5.2.3.) (a) Modulated carrier signal,
(b) Modulating square wave.

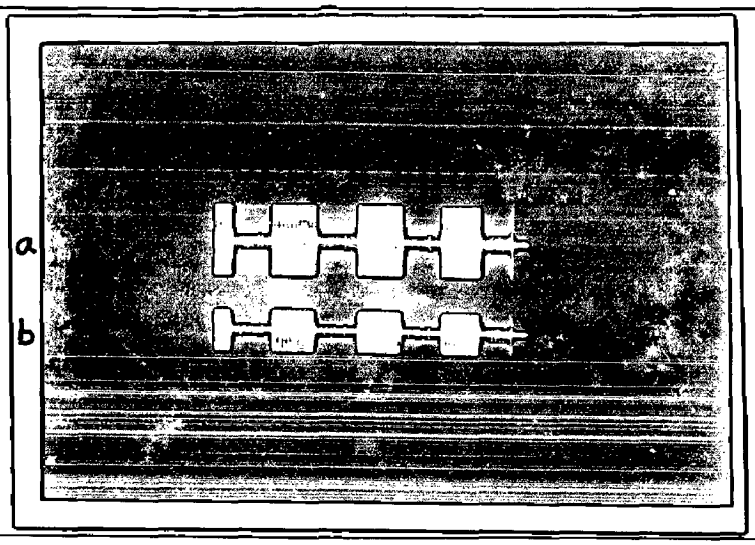


Fig.(5.2.4.) Inphase modulated carrier signals at one end of the line for internal faults.
(a) Transmitted carrier
(b) Received carrier.

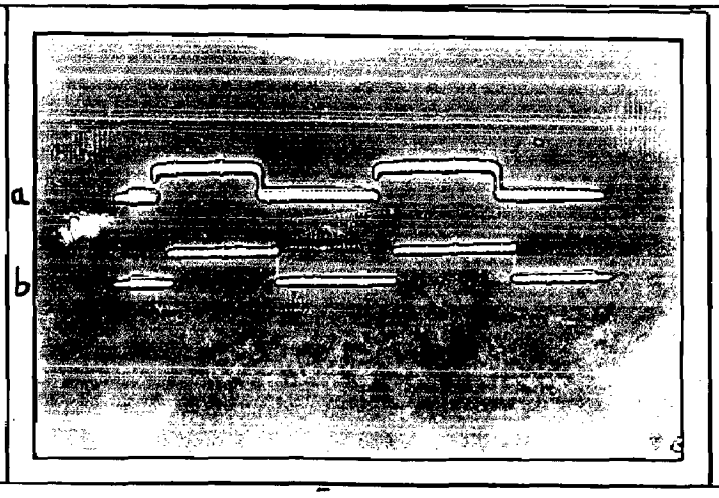


Fig.(5.2.5.) Inputs to the Phase comparator for internal faults.
(a) Local square wave.
(b) Received square wave.

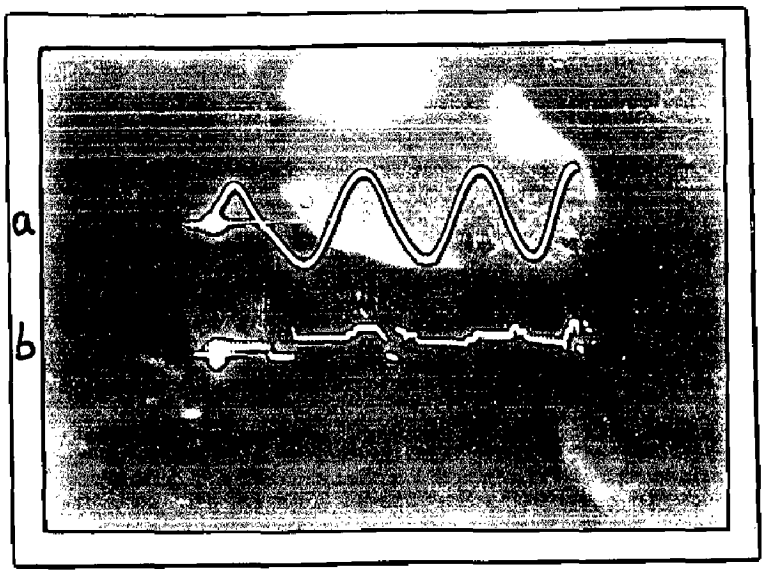


Fig.(5.2.6.) Output of the phase comparator for internal fault.
(a) Fault current wave
(b) Comparator output.

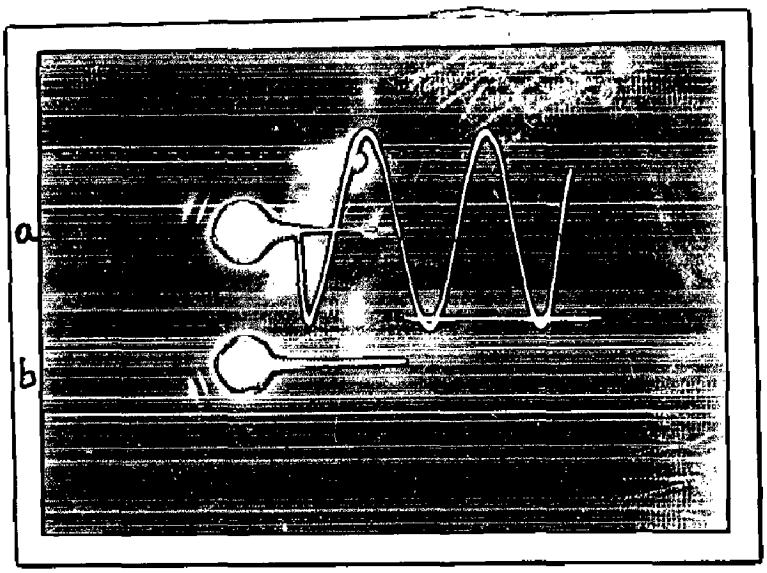


Fig.(5.2.7.) Tripping time,
(a) Fault current wave,
(b) Pick-up of the slave relay.

between these two signals has been noted, without considering the capacitance of the line. Fig.(5.2.5) shows the local square wave and the received square wave obtained after demodulation and amplification of the received carrier signal. However, a slight phase shift observed between these two square waves does not interfere with tripping.

Fig.(5.2.6.) shows the output of the phase comparator, as compared to the fault current signal, after comparing the local and received square wave signals.

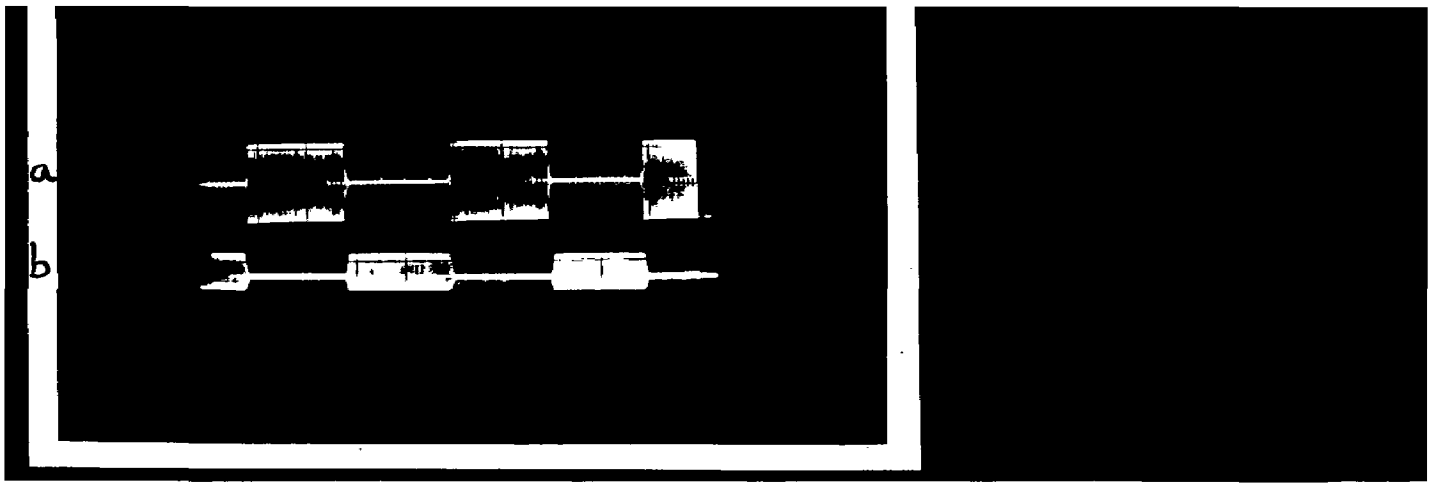
Overall operating time, from the time of closing of the fault switch to the time of opening of the circuit breakers (replaced by contactors here) was measured with the help of a timer, for repeated fault simulation, and the time noted was 67 milliseconds, which is slightly more than 3 cycles.

However, the time of operation upto the triggering of the bistable circuit of the slave relay as shown in Fig.(5.2.7.) is slightly more than 1 cycle, which is well within the desired time limit.

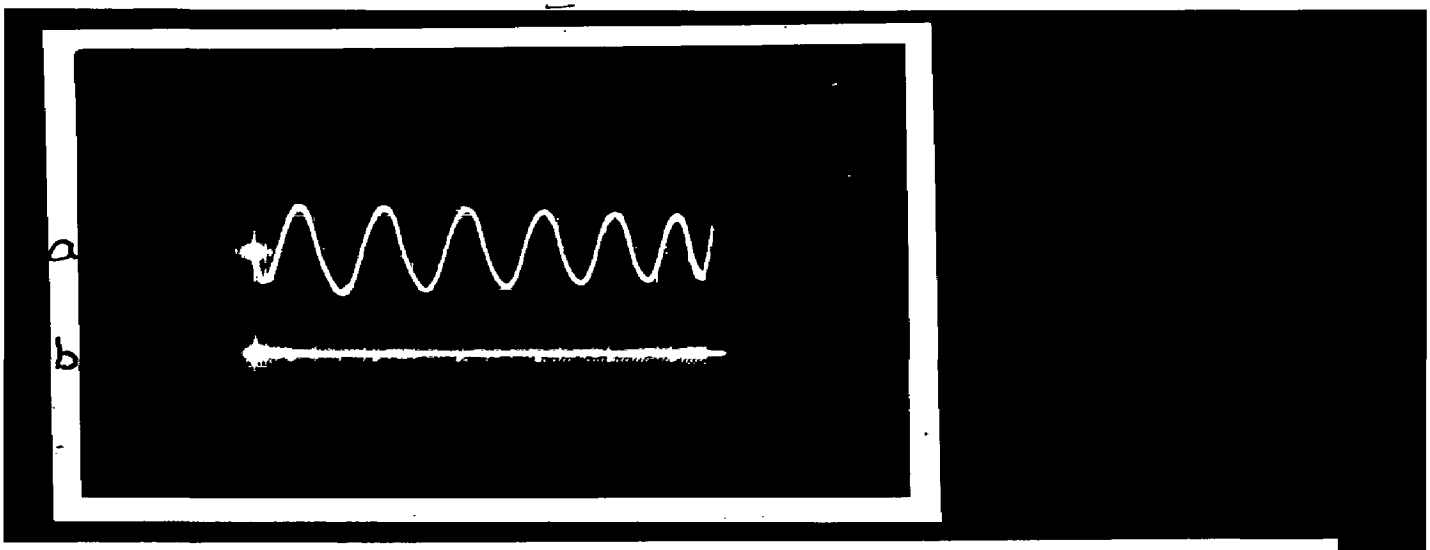
5.3. PERFORMANCE ON EXTERNAL FAULTS:

External faults were simulated by sudden switching of the single, double and three phase loads outside the protected line section, when fed from the opposite end of the line. The performance so obtained is given below.

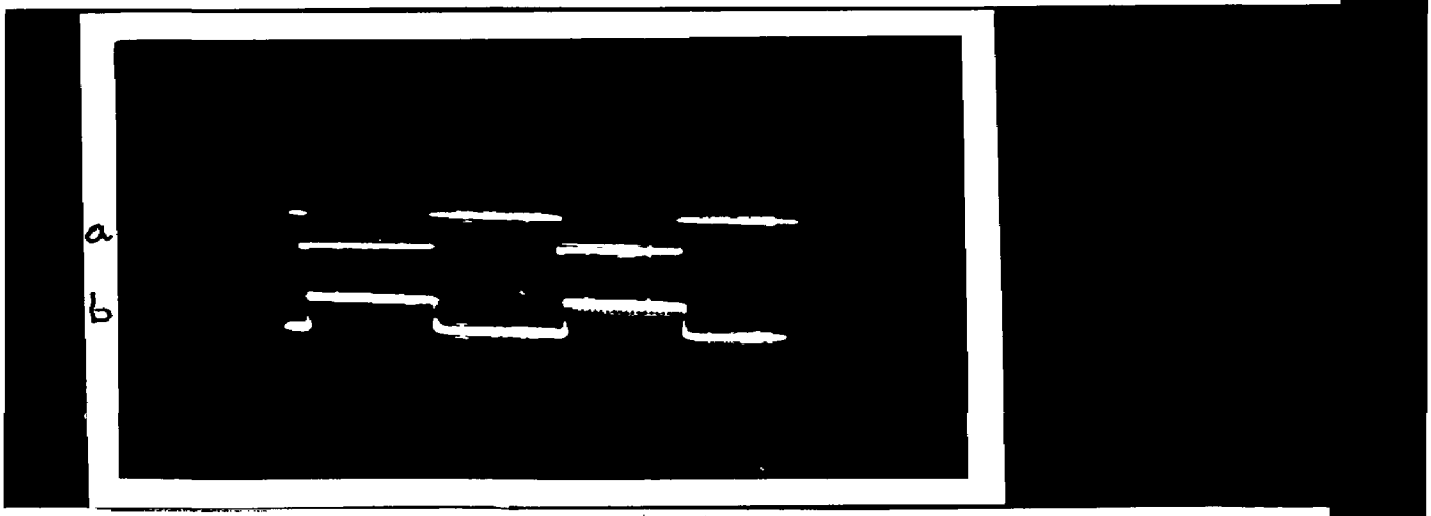
Fig.(5.3.1.) shows the transmitted and received modulated carrier signals at one end of the line, for any type of external fault. Clearly, now these two signals are 180° out of phase with each other.



(5.3.1.) Out of phase modulated carrier signals at one end of the line for external faults.
(a) Transmitted carrier,
(b) Received carrier.



ig.(5.3.3.) Output of the phase comparator for external fault.
(a) Fault current wave,
(b) Output of the phase comparator.



ig.(5.3.2.) Inputs to the phase comparator for external fault.
(a) Local square wave,
(b) Received square wave.

Fig.(5.3.2.) shows the local and received square waves which are also 180^{o} out of phase with each other. These, when fed to the phase comparator circuit, do not give any comparator output as is clearly shown in Fig.(5.3.3.) and hence no tripping takes place.

Distributed line capacitance was introduced at four points inside the protected line section. This, however, did not affect the results.

CHAPTER - 6

CONCLUSIONS

6.0. CONCLUSIONS:

The results described in the previous chapter demonstrate the feasibility of using transistors as important circuit elements in a carrier current phase comparison scheme of protection. The system of protection that has been described is well suited to all the abnormal power system conditions arising from system swings or any type of fault on the system. The conclusions on the working of the various equipments have been described in this Chapter.

The transmitter described in Chapter 4, could not be tuned for the given line impedance of 15 ohms per phase, because in that case it was observed that the received carrier signal appeared only as a noise signal. Finally, only one third of the line impedance has been considered as the carrier channel and the received signal has been amplified after demodulation. To avoid interference between the transmitted carrier signal at the two ends, these signals have been channelised on two different phases of the line. However, on internal faults involving both of these phases, a slight superimposition of one modulated carrier signal upon the other has been observed. But, since these signals for internal faults are almost in phase with each other, its effect has been only to increase slightly the width of one of the square waves, which does not affect the final tripping as the two square waves still remain almost in phase with each other. Further, to keep off the mutual inductance effects between the lumped line reactors, phases A and C which are a little away from each other, have been chosen for transmission of carrier signal from each end. With the use of I.F.Ts. in the transmitter circuits at the two ends, a slight

difference in the amplitudes of the two transmitted carrier signals has been observed.

Balancing of the sequence networks (shown in Fig.2.5) at the two ends of the line is of great importance to obtain the exactly in-phase combined sequence output voltages at the two ends for all types of internal faults, and exactly out-of-phase combined sequence output voltages for all types of external faults. The actual values of resistance R_n and r_n (Fig.2.5) set for obtaining the correct outputs from the sequential circuit are 3.5 ohms and 1.0 ohm respectively, in place of 4 ohms and 2 ohms which are the calculated values. This may be due to the slight difference between the actual and calculated values of the reactance X_n and also due to the resistance of the reactor winding. Initially, use of iron cored reactors was made in the sequential circuit, but, this produced distortion in the output sequence voltage waves, and therefore these had to be replaced by air cored reactors which gave the desired sinusoidal output. The measured values of the negative sequence voltage for the simulation of a balanced fault was about 1 volt at each end instead of zero volt. This may be due to the difference in the line currents because of the inclusion of the line traps.

The squaring circuit shown in Fig.(4.2) gave satisfactory performance for all the a.c. voltage inputs above 1 volt. However, the input transformer of the squaring circuit has been designed for voltages upto about 40 volts. Initially one of the squaring circuit sometimes did not operate satisfactorily for a voltage input from 1 to 3 volts, because of the insufficient output signals obtained from the pulse circuits which trigger the bistable output stage of the squaring circuit. This was finally remedied by shorting the emitter resistance of the bistable

circuit.

Superposition of the power frequency signals upon the carrier signal was observed at the receiving end of the line, when the line was energised. This effect was slightly reduced by decreasing the drainage coil reactance, but was wholly nullified by putting a power frequency filter tuned at 100Kc/s, at the receiving end as shown in Fig.(4.4). Demodulation of the received carrier was found to be well accomplished by using OA 160 diodes, instead of IN38 diodes. Even the half wave rectification gave a perfect square wave output, with the help of OA160 diodes. Only a slight noise signal was observed at the top of the square wave obtained after demodulation, which was finally filtered by a higher output capacitance. Amplification of the demodulated square wave was suitably performed by switching transistor OC76.

The provision of rated d.c. supply voltage and proper biasing of the base and emitter terminals, are the main factors to obtain the desired outputs from the transistor circuits. This has been observed in the case of the phase comparator circuit which needed a proper adjustment of the emitter potential to differentiate between internal and external faults. After exhaustive testing, two out of the three input diodes (IN38) were found to be damaged and had to be replaced.

During the testing carried out at the initial stages, the slave circuit at one end of the line was found to be susceptible to tripping on account of transients and this in turn made the other end also to trip. This defect was however removed by including the input capacitance C_1 in the slave circuit, across the incoming signal from the phase comparator

as shown in Fig.(4.6).

No transistor failure was experienced after exhaustive testing of the equipment. The tests carried out during the hottest season did not show any appreciable effects on the performance of the transistors. The reliability in the operation of transistors, quick operating time and their long life makes them more suitable to this scheme of protection. It may thus be concluded that such a transistorised phase comparison carrier current scheme can be very effectively used for the protection of important high voltage long transmission lines.

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A_P_P_E_N_D_I_C_E_S

A-1. SELECTION OF PHASE REPRESENTING QUANTITY:

A1.1. Theoretical Aspect:

The effective working of a phase comparison carrier system greatly depends upon the choice of relaying quantities and the method of their derivation. Arrangements at each end should provide for the detection of all kinds of faults, which can occur on the system and the derived single phase quantity which is used to modulate the carrier must faithfully represent, for any combination of load and fault currents, the phase angle of the line current at each end with respect to some convenient datum.

To determine the best method of combining the three individual phase currents into a single quantity of comparison, the sequence currents for different faults that are available are as under:

Single phase to ground	...	I_1, I_2, I_o
Two phase to ground	...	I_1, I_2, I_o
Phase to phase	...	I_1, I_2.
Three phase fault	...	I_1
Three phase to ground	...	I_1, I_2, I_o.

Now, since positive sequence current I_1 is present during all types of faults, it is essential to derive it as one of the outputs for phase comparison. But since positive sequence current is also present during normal load conditions, it is advisible to detect it during faults by visualizing its rate of rise. A pulse circuit has been designed for this purpose in the starting circuit. However, through current component may adversely effect the positive sequence current and hence reduce the sensitivity.

Undoubtedly, negative phase sequence current I_2, is present during all types of faults except the three phase fault. Hence it is quite logical to consider it as the phase representing quantity. It's two main advantages are:-

(1) Under Balanced load conditions on the line (which is normally the case when there is no fault on the line) negative sequence current is absent.

(2) Negative sequence current is substantially uneffected by load conditions.

Zero phase sequence current I_p is involved only during ground faults. So, it's provision can increase the sensitivity during ground faults.

Since I_2 can provide a desired sensitivity during all types of faults except the three phase fault, in which case we can rely upon the output of the positive sequence current I_1, a combination of I_2 and I_1 seems to be the best selection for the phase representing quantity. Since I_2 is present whenever I_o is present, I_o may be replaced by I_2 without effecting the sensitivity. However, the final selection of the combination of sequence currents may be based on the following analysis.

A.1.2. Mathematical Analysis:

The output quantity for representing the fault current in phase can effectively be a combination of the following sequence currents.

(1) Output $\propto MI_2 + NI_1$

(2) Output $\propto AI_2 + BI_o + CI_1$

(3) Output $\propto BI_o + NI_1$.

Let the output current be represented by I_s and Fault current per phase by I_F.

(1) Output $MI_2 + NI_1$:-

Let the three line conductors represent phases A, B and C.

(i) Phase A to ground Fault:

Taking phase a of the three phase current I_a, I_b and I_c as reference:

$$I_a = I_1 + I_2 + I_o$$

$$= I_F$$

$$= \frac{3E}{X_1 + X_2 + X_o}$$

where,

resistance being neglected, X_1 = positive sequence reactance of the system network, X_2 = Negative sequence reactance of the system network and X_o = Zero sequence reactance of the system network.

$$I_s = MI_2 + NI_1 = (M+N)\, I_2 = \frac{(M+N)E}{X_1 + X_2 + X_o}$$

$$\frac{|I_s|}{|I_F|} = \frac{M+N}{3} \quad \ldots \quad \ldots \quad (1)$$

(ii) Phase B to Ground Fault:

$$I_1 = \frac{1}{3}.a.I_b, \quad I_2 = \frac{1}{3}.a^2.I_b \text{ and } I_o = \frac{1}{3}.I_b.$$

$$I_1 = \frac{E}{X_o + X_1 + X_2}$$

$$I_F = I_b = I_o + a^2 I_1 + aI_2.$$

$$= \frac{3E\,(-\sqrt{3}/2 + j\frac{1}{2})}{X_1 + X_2 + X_o}$$

E being the positive sequence voltage of the equivalent circuit.

$$I_s = \frac{E}{X_1 + X_2 + X_o}(-j)\,(M_a + N)$$

$$|I_s| = \sqrt{M^2 + N^2 - MN} \cdot \frac{E}{X_o + X_1 + X_2}$$

$$\therefore \frac{|I_s|}{|I_F|} = \frac{\sqrt{M^2+N^2-MN}}{3} \quad \ldots \quad \ldots \quad (2)$$

(iii), Phases BC to ground fault:

$$\text{Here } I_a = 0, \quad I_1 = \frac{E(X_2+X_o)}{X_1X_2+X_2X_o+X_oX_1}$$

$$I_2 = -I_1 \frac{X_o}{X_o+X_2} \text{ and } I_o = -I_1 \frac{X_2}{X_o+X_2}$$

Now, $I_s = MI_2 + NI_1$.

$$= \frac{E}{X_1X_2+X_2X_o+X_oX_1} \cdot \{-MX_o+N(X_2+X_o)\}.$$

$$\therefore |I_s| = \frac{E\{(M-N)X_o-NX_2\}}{X_1X_2+X_2X_o+X_oX_1}$$

$$I_F = \frac{E}{X_1X_2+X_2X_o+X_oX_1}\left\{-1.5X_2 - j\,(\sqrt{3}\,X_o + \sqrt{3}/2\,X_2)\right\}$$

Taking $X_1 = X_2$,

$$\frac{|I_s|}{|I_F|} = \frac{(M-N)X_o-NX_1}{\sqrt{3}\,(X_1^2+X_o^2+X_oX_1)^{\frac{1}{2}}}$$

$$= \frac{(M-N)\,X_o/X_1-N}{\sqrt{3}\,[1+X_o/X_1+(X_o/X_1)^2]^{\frac{1}{2}}} \quad \ldots \quad (3)$$

(iv) Phases AB to ground Fault:

$$\text{Here } I_c = 0$$

$$I_1 = -(I_2 + I_o)$$

$$= \frac{E(X_2 + X_o)}{X_1X_2+X_2X_o+X_1X_o}$$

$$I_2 = -\frac{a^2\,EX_o}{X_1X_2+X_2X_o+X_1X_o}$$

and $I_o = - \frac{a.E.X_2}{X_1X_2+X_1X_o+X_2X_o}$

Now, $I_s = MI_2 + NI_1$

$$= \frac{E}{X_1X_2+X_1X_o+X_2X_o} \left\{ X_o(N+\frac{M}{2})+NX_2+j.\frac{\sqrt{3}}{2}.MX_o \right\}$$

$$\therefore |I_s| = \frac{E}{X_1X_2+X_1X_o+X_2X_o} \left\{ N^2(X_2^2+X_o^2)+M^2X_o^2+MN(X_o^2+X_oZ_2)+2N^2X_2X_o \right\}^{\frac{1}{2}}$$

The magnitude of I_F will remain same as in the above case.

$$\therefore \frac{|I_s|}{|I_F|} = \frac{\left\{ N^2(X_2^2+X_o^2)+M^2X_o^2+MN(X_o^2+X_oX_2)+2N^2X_2X_o \right\}^{\frac{1}{2}}}{\sqrt{3}\ (X_2^2+X_o^2+X_oX_2)^{\frac{1}{2}}}$$

Taking $X_2 = X_1$ and simplifying.

$$\frac{|I_s|}{|I_F|} = \frac{\left\{ N^2\left[1+(X_o/X_1)^2\right]+M^2(X_o/X_1)^2+MN\left[(X_o/X_1)^2+X_o/X_1\right]+2N^2(\frac{X_o}{X_1}) \right\}^{\frac{1}{2}}}{\sqrt{3}\ \left\{1+X_o/X_1+(X_o/X_1)^2\right\}^{\frac{1}{2}}} \quad \ldots \quad (4)$$

Similarly, we can derive for 2 phase and 3 phase faults as well.

(2) Output $AI_2 + BI_o + CI_1$:

(i) Phase A to ground Fault:

$I_1 = I_2 = I_3$

$I_F = I_a = \frac{3E}{X_1+X_2+X_o}$

$I_s = AI_2 + BI_o + CI_1$

$= I_1(A+B+C).$

$$\frac{I_s}{I_F} = \frac{(A+B+C)}{3} \quad \ldots \quad \ldots \quad (5)$$

(ii) Phase B or C to ground Fault:

$I_1 = 1/3\ aI_b$, $I_2 = aI_1$, $I_o = I_1/a$

$I_F = \frac{3E}{X_1+X_2+X_o}$ as above.

$$I_s = \frac{A.aE}{X_o+X_1+X_2} + \frac{BE}{a(X_o+X_1+X_2)} + \frac{CE}{X_o+X_1+X_2}$$

$$= \frac{E}{X_o+X_1+X_2}\left\{(-A/2 -B/2 +C)+j(A\sqrt{3}/2 -B\sqrt{3}/2)\right\}$$

$$\therefore |I_s| = \frac{E}{X_o+X_1+X_2}(A^2+B^2+C^2-AB-BC-AC)^{\frac{1}{2}}$$

Hence,

$$\frac{I_s}{I_F} = \frac{\sqrt{(A^2+B^2+C^2-AB-BC-AC)}}{3} \quad \ldots \quad (6)$$

(iii) Phases B-C to Ground Fault:

$$I_1 = \frac{E(X_2+X_o)}{X_1X_2+X_2X_o+X_1X_o}$$

$$I_2 = -\frac{EX_o}{X_2X_1+X_oX_1+X_oX_2}$$

$$I_o = -\frac{EX_2}{X_1X_2+X_oX_1+X_oX_2}$$

Now, $I_s = AI_2 + BI_o + CI_1$

$$= \frac{E}{X_1X_2+X_oX_1+X_oX_2}\left[X_o(C-A)+X_2(C-B)\right]$$

$$I_F = \frac{\sqrt{3}\,E.\sqrt{X_2^2+X_o^2+X_oX_2}}{X_1X_2+X_oX_1+X_oX_2}$$ as in Eqn. No.(3).

Taking $X_1 = X_2$ and simplifying.

$$\frac{|I_s|}{|I_F|} = \frac{(X_o/X_1)(A-C)+(B-C)}{\sqrt{3}.\sqrt{1+(X_o/X_1)+(X_o/X_1)^2}} \quad \ldots \quad (7)$$

(iv) Phases AB to Ground Fault:

$$I_1 = \frac{E(X_2+X_o)}{X_oX_1+X_1X_2+X_oX_2}$$

$$I_2 = - \frac{a^2 E(X_o)}{X_0X_1+X_1X_2+X_0X_2}$$

$$I_o = - \frac{a.EX_2}{X_0X_1+ X_0X_2+ X_1X_2}$$

$$|I_F| = \frac{\sqrt{3}.E\ (X_2^2 +X_o^2+X_oX_2)^{\frac{1}{2}}}{(X_0X_1+X_1X_2+ X_0X_2)}$$ as before

$$I_s = AI_2 + BI_o + CI_1$$

$$= \frac{E}{X_0X_1+X_1X_2+X_0X_2} \left\{ - a^2AX_o - aBX_2 + C(X_2+X_o) \right\}$$

$$= \frac{E}{X_0X_1+X_1X_2+X_0X_2} \left\{ X_o(A/2+C)+X_2(C+B/2)+j.\sqrt{3}/2(AX_o-BX_2) \right\}$$

or $$|I_s| = \frac{E}{X_0X_1+X_1X_2+ X_0X_2} \left\{ X_o^2(A^2+C^2+AC)+X_2^2(C^2+B^2+BC)+X_oX_2(AC+BC-AB+ 2C^2) \right\}^{\frac{1}{2}}$$

Taking $X_1 = X_2$ and simplifying:-

$$\frac{|I_s|}{|I_F|} = \frac{\left\{ (\frac{X_o}{X_1})^2(A^2+C^2+AC)+(\frac{X_o}{X_1})(2C^2-AB+AC+BC)+(B^2+C^2+BC) \right\}^{\frac{1}{2}}}{\sqrt{3}.\sqrt{1+(X_o/X_2) + (X_o/X_2)^2}}$$

... ... (8)

(3) Output $BI_o + NI_1$

(i) Phase A to ground Fault:

$$I_1 = I_2 = I_o = \frac{E}{X_1 + X_2 +X_o}$$

$$I_F = I_a = I_1 +I_2 +I_o$$

$$\therefore |I_F| = \frac{3E}{X_1 +X_2 +X_o}$$

$$I_s = BI_o + NI_1$$

$$|I_s| = (B+N)\frac{E}{X_1+ X_2+ X_0}$$

$$\frac{|I_s|}{|I_F|} = \frac{B+N}{3} \quad \ldots \quad \ldots \quad (9)$$

(ii) Phase B to Ground Fault:

$$|I_F| = \frac{3E}{X_1+X_2+X_o}, \quad I_2 = aI_1, \quad I_o = a^2 I_1$$

$$I_s = BI_o + NI_1$$

$$= \frac{E}{X_1+X_2+X_0} \left(-B/2+N - j.\sqrt{3}/2B\right)$$

$$|I_s| = \frac{E}{X_1+X_2+X_0} (B^2+N^2-BN)^{\frac{1}{2}}$$

$$\therefore \frac{|I_s|}{|I_F|} = \frac{\sqrt{B^2+N^2-BN}}{3} \quad \ldots \quad \ldots \quad (10)$$

(iii) Phases B,C to ground Fault:

$$I_1 = \frac{E(X_2+X_o)}{X_1X_2+X_0X_1+X_0X_2}$$

$$I_2 = -\frac{I_1X_o}{X_0+X_2}$$

$$I_0 = -\frac{I_1X_2}{X_o+X_2} \text{ as before.}$$

$$I_F = \frac{\sqrt{3}\,E.\sqrt{X_2^2+X_0^2+X_oX_2}}{X_1X_2+X_2X_0+X_1X_2}$$

$$I_s = BI_o + NI_1$$

$$= \frac{E}{X_1X_2+X_0X_1+X_0X_2}.\left\{X_2(B-N)+N.X_o\right\}$$

$$\frac{|I_s|}{|I_F|} = \frac{X_2(B-N)-NX_o}{\sqrt{3}\sqrt{X_2^2+X_0^2+X_oX_2}}$$

Taking $X_2 = X_1$ and simplifying.

$$\frac{|I_s|}{|I_F|} = \frac{(B-N) - N(X_o/X_1)}{\sqrt{3}.\sqrt{1+(X_o/X_1)+(X_o/X_1)^2}} \quad \ldots \quad (11)$$

(iv) Phases AB to Ground Fault:

$$|I_F| = |I_a| = \frac{\sqrt{3}\sqrt{X_o^2 + X_1^2 + X_oX_1}.E}{X_1X_2 + X_oX_1 + X_oX_2}$$

$$I_2 = \frac{-a^2X_o}{X_o+X_2} I_1, \quad I_o = \frac{-aX_2}{X_o+X_2}. I_1$$

$$I_s = BI_o + NI_1$$

$$= \frac{-BX_2(-\frac{1}{2}+j.\sqrt{3}/2)E}{X_1X_2 + X_2X_o + X_oX_1} + \frac{NE(X_2+X_o)}{X_1X_2 + X_2X_o + X_oX_1}$$

$$= \frac{E}{X_1X_2+X_2X_o + X_oX_1}\left\{X_2(N+B/2)+NX_o - j.BX_2.\sqrt{3}/2\right\}$$

$$\therefore |I_s| = \frac{E}{X_1X_2+X_oX_1+X_oX_2}\left\{X_2^2(B^2N^2+BN)+X_o^2N^2+X_oX_2(BN+2N^2)\right\}^{\frac{1}{2}}$$

Hence, $$\frac{|I_s|}{|I_F|} = \frac{\left\{X_2^2(B^2+N^2+BN)+X_o^2N^2+X_oX_2(BN+2N^2)\right\}^{\frac{1}{2}}}{\sqrt{3}\ \sqrt{X_2^2 + X_o^2 + X_oX_2}}$$

Taking $X_2 = X_1$ and simplifying.

$$\frac{|I_s|}{|I_F|} = \frac{\left\{(B^2+N^2+BN)+X_o/X_1(BN+2N^2)+(X_o/X_1)^2.N^2\right\}^{\frac{1}{2}}}{\sqrt{3}\cdot\sqrt{1+(X_o/X_1) + (X_o/X_1)^2}}$$

Now, ... (12)

Representing $[I_s/I_F]$ by the symbol K for simplicity, we can derive its numerical value for all the cases considered above by assigning proper values to the constants M,N,A,B and C in all the above mentioned three combinations one by one.

(1) For example, taking N = +1, in equation No.(1),

If $M = 2$, $K = 1/3(M+N)$

$= 1/3(2+1)$

$= 1.0$

Similarly for different values of M and N the values of K have been tabulated as under:

	N = +1			N = -1		
M	2	4	6	2	4	6
K	1.0	1.6	3.6	0.33	1.0	3.0

Now, considering equation No.(2) and recalculating as above, for $K = 1/3\ (M^2 + N^2 - MN)^{\frac{1}{2}}$

	N =+1			N = -1		
M	2	4	10	2	4	10
K	0.58	1.20	3.18	0.88	1.58	3.51

A plot of the above results is shown in Fig.(A.1.1a) (a) & (b) which indicates that K attains greater values for N=+1 in case of phase A to ground faults whereas for phase B or phase C to ground faults K attains higher values for N = -1.

Next, considering equation No.(3), we can obtain various values of K corresponding to different values of M,N and X_o/X_1. The results have been tabulated as under-

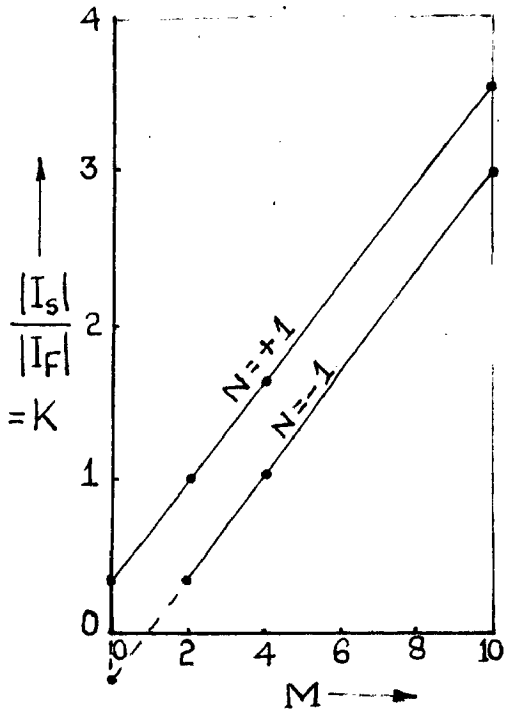


Fig A·1·1(a)

Phase A to Ground Fault

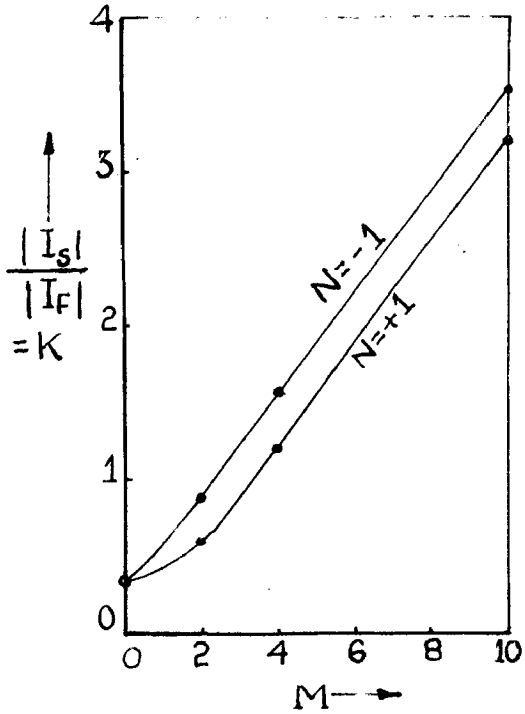


Fig A·1·1(b)

Phase B to Ground Fault.

(1) $I_s = MI_2 + NI_1$

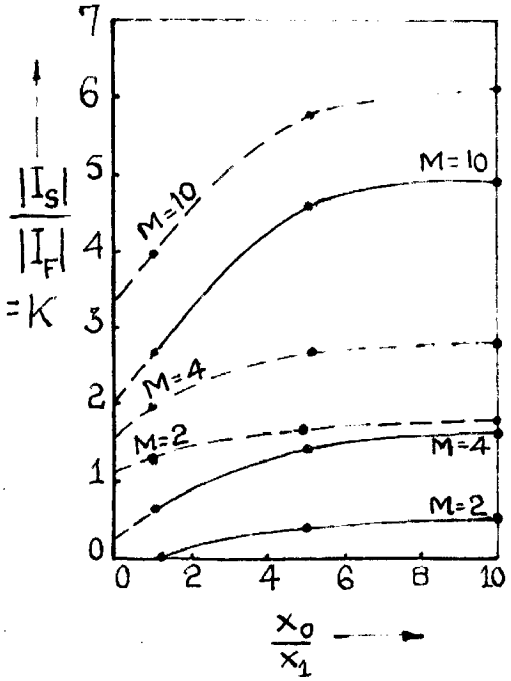
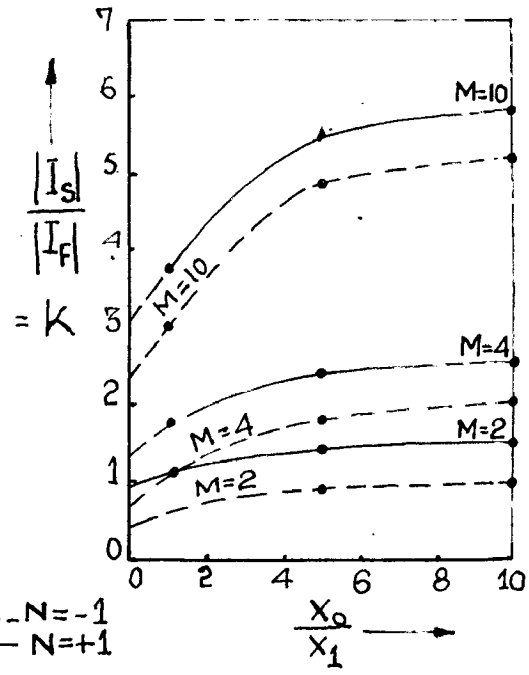


Fig A·1·2(a)

Phases BC-G Fault



N=-1
N=+1

Fig A·1·2(b)

Phases AB-G Fault.

X_o/X_1	N = +1 K (M=2)	N = +1 K (M=4)	N = +1 K (M=10)	N = -1 K (M=2)	N = -1 K (M=4)	N = -1 K (M=10)
1	0	0.66	2.66	1.33	2.0	4.0
5	0.415	1.45	4.45	1.66	2.7	5.8
10	0.492	1.59	4.86	1.70	2.8	6.08

A plot of these results is shown in Fig.(A.1.2a) wherein it is seen that values of K are smaller for N =+1 than for N=-1.

Exactly as has been done above, equation No.(4), which can be written as -

$$\frac{|I_s|}{|I_f|} = \frac{\left\{N^2+X_o/X_1(MN+2N^2)+(X_o^2/X_1)^2(M^2+N^2+MN)\right\}^{\frac{1}{2}}}{\sqrt{3}\left\{1+M_o/X_1+(X_o/X_1)^2\right\}^{\frac{1}{2}}} \quad \ldots \quad (4)$$

has also been calculated for different values of M, N and X_o/X_1 and the results are tabulated as under.

X_o/X_1	N = +1 K (M=2)	N = +1 K (M=4)	N = +1 K (M=10)	N = -1 K (M=2)	N = -1 K (M=4)	N = -1 K M=10)
1	1.15	1.76	3.7	0.66	1.15	3.06
5	1.45	2.44	5.5	0.90	1.84	4.90
10	1.48	2.53	5.8	0.94	1.95	5.2

A plot of the above results has been shown in Fig.(A.1.2.b) wherefrom it is clear that values of K for N = +1 are more than N = -1.

(2) In equation No.(5) constant A has been varied from 2 to 10, B from 0 to 4 and C from -1 to +1. The calculated results have been tabulated below.

(a) Taking C = -1, we obtain,

	B=0			B=1			B=2			B=4		
A	2	4	10	2	4	10	2	4	10	2	4	10
K	1.0	1.6	3.6	1.3	2.0	4.0	1.6	2.3	4.3	2.3	3.0	5.0

(b) Taking C+1, we obtain,

	B=0			B=1			B=2			B=4		
A	2	4	10	2	4	10	2	4	10	2	4	10
K	0.33	1.0	3.0	0.66	1.3	3.33	1.0	1.6	3.66	1.66	2.33	4.33

These results have been plotted in Fig. No.(A.1.3a)

Considering equation (6) in the same way, the results obtained are as under:

(a) Taking C = -1, we obtain:

	B=0			B=1			B=2			B=4		
A	2	4	10	2	4	10	2	4	10	2	4	10
K	0.88	1.53	3.5	0.88	1.45	3.38	1.0	1.45	3.28	1.45	1.66	3.18

(b) Taking C = +1, we obtain,

	B=0			B=1			B=2			B=4		
A	2	4	10	2	4	10	2	4	10	2	4	10
K	0.57	1.2	3.18	3.33	1.0	3.0	0.33	0.88	2.85	0.88	1.0	2.64

The above results have been plotted in Fig.(A.1.3b).

Again, Equation (7), is considered for various values of constants A, B, C and X_o/X_1 and the results obtained for K are tabulated as under-

(a) Taking C=+1

	B=0			B=2			B=4		
A	2	4	10	2	4	10	2	4	10
X_o/X_1	1 5 10	1 5 10	1 5 10	1 5 10	1 5 10	1 5 10	1 5 10	1 5 10	1 5 10
K	0 .4 .5	1.6 1.4 1.6	2.6 4.6 4.8	0.6 0.6 0.6	1.3 1.6 1.7	3.3 4.5 4.9	1.3 0.8 .7	2.0 1.8 1.8	4.0 4.9 5.0

(b) Taking C=-1

	B=0			B=2			B=4		
A	2	4	10	2	4	10	2	4	10
X_o/X_1	1 5 10	1 5 10	1 5 10	1 5 10	1 5 10	1 5 10	1 5 10	1 5 10	1 5 10
K.	1.3 1.6 1.7	2.0 2.7 2.7	4.0 5.8 6.0	2.0 1.8 1.8	2.6 2.9 2.8	4.6 6.0 6.1	2.6 2.0 1.9	3.3 3.1 3.0	5.3 6.2 6.25

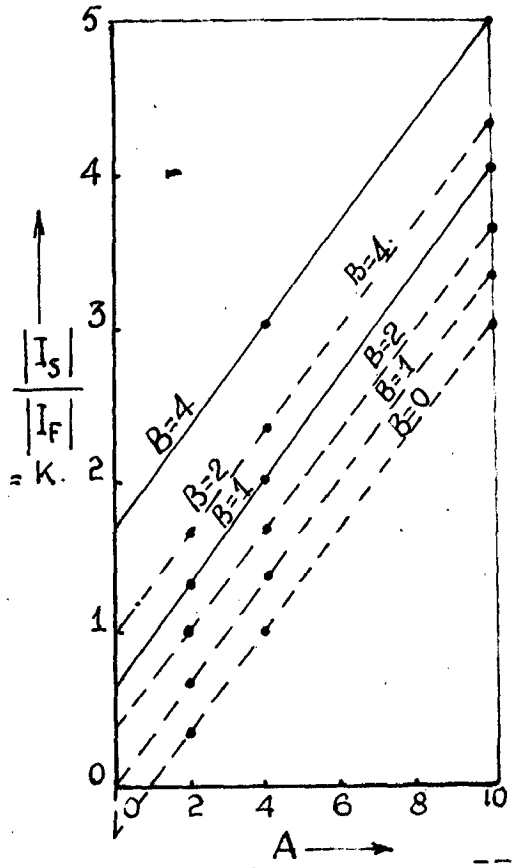


Fig A·1·3(a).

Phase A to Ground Fault.

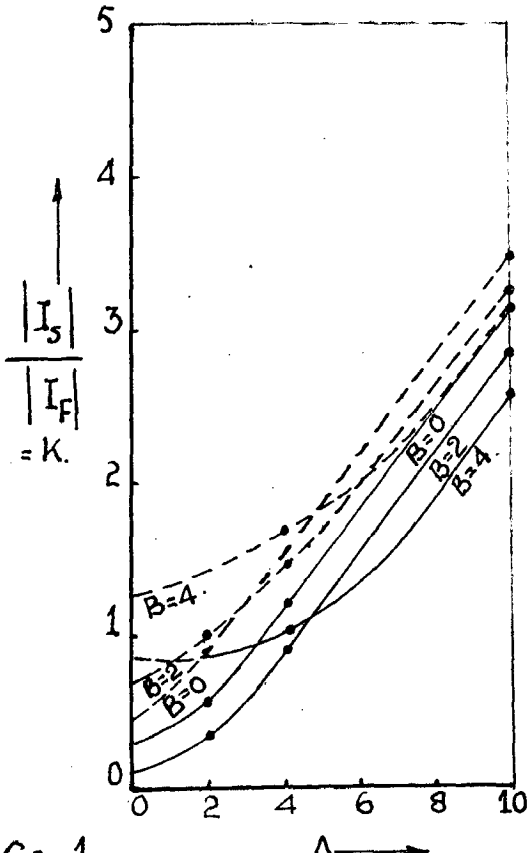


Fig A·1·3(b).

Phase B to Ground Fault.

---- C = -1
—— C = +1

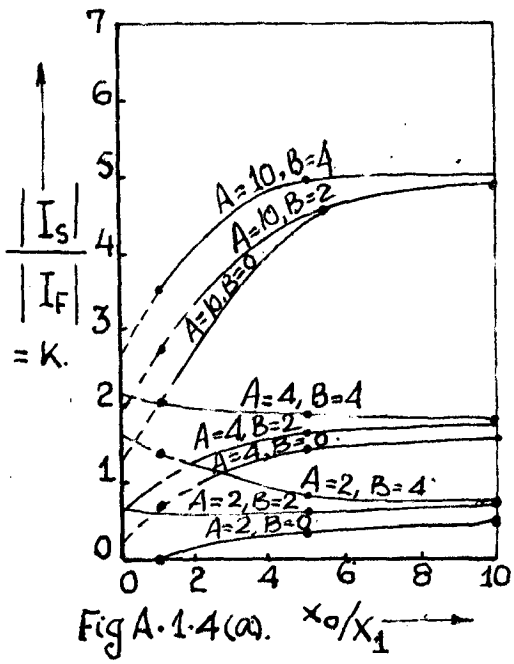


Fig A·1·4(a).

Phases BC to Ground Fault.

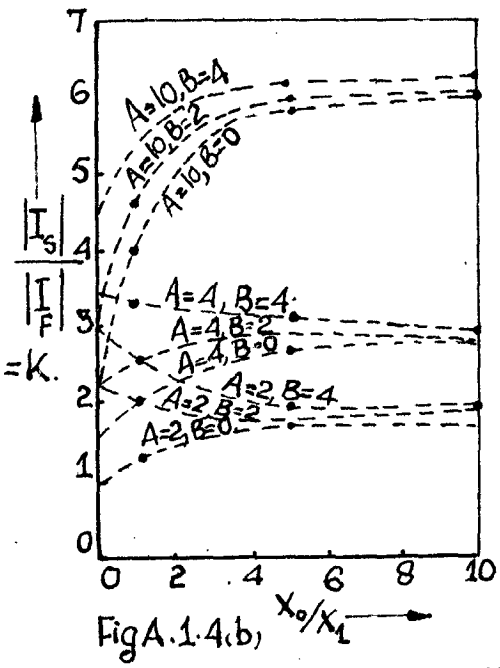


Fig A·1·4(b).

Phases C B to Ground Fault.

(2) $I_s = AI_2 + BI_0 + CI_1$

A plot of the above results is shown in Fig.No.(A.1.4a) and (A.1.4b).

(3) Next, Equation (9) can also be considered for various values of B and N. The results are tabulated below:

(a) N = +1

B	0	1	2	4	5	8	10
K	0.33	0.66	1.0	1.66	2.0	3.0	3.66

(b) N = -1

B	0	1	2	4	5	8	10
K	-0.33	0	0.33	1.0	1.33	2.33	3.0

Similarly considering equation (10) following results are obtained.

(a) N = +1

B	0	1	2	4	6	8	10
K	0.33	0.33	0.58	1.20	1.86	2.5	3.18

(b) N = -1

B	0	1	2	4	6	8	10
K	0.33	0.58	0.88	1.58	2.18	2.85	3.51

The graphic plot of these results is shown in Figs. (A.1.5a) and (A.1.5b).

Again, by putting in values for B, N and X_o/X_1 in Equation No.11, following values of K were obtained.

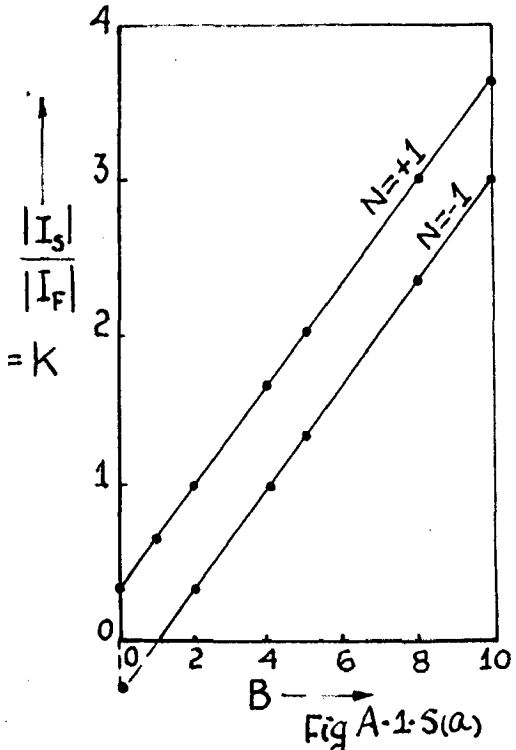


Fig A-1-5(a)

Phase A to Ground Fault

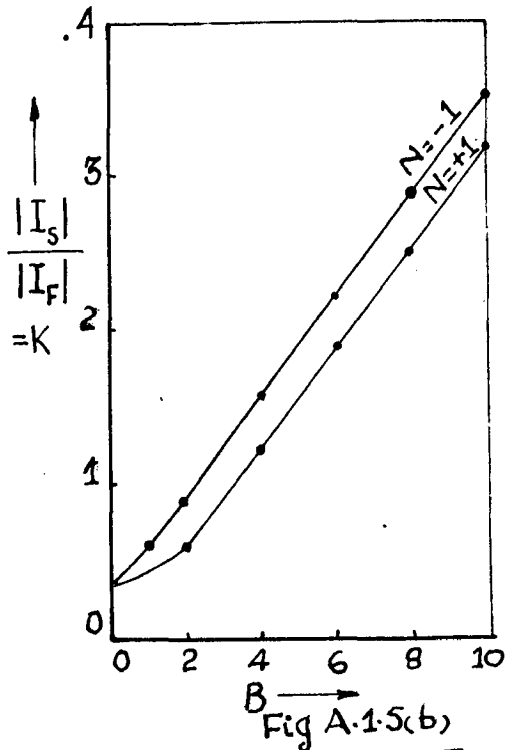


Fig A-1-5(b)

Phase B to Ground Fault.

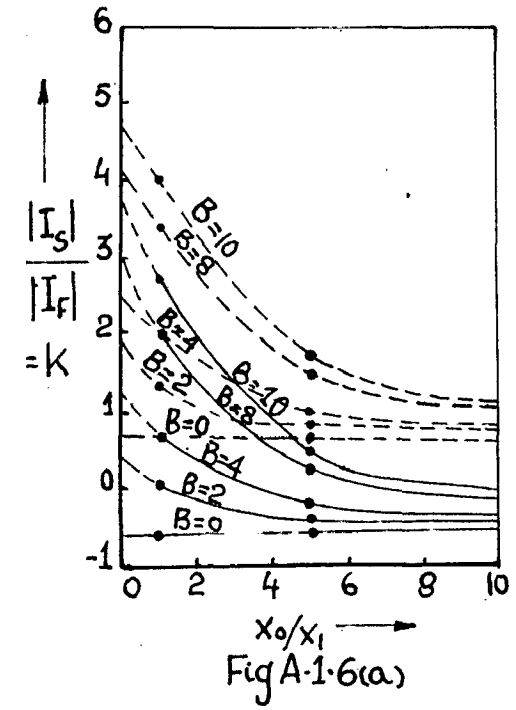


Fig A-1-6(a)

Phases B-C to Ground Fault

N = +1 ——
N = -1 ----

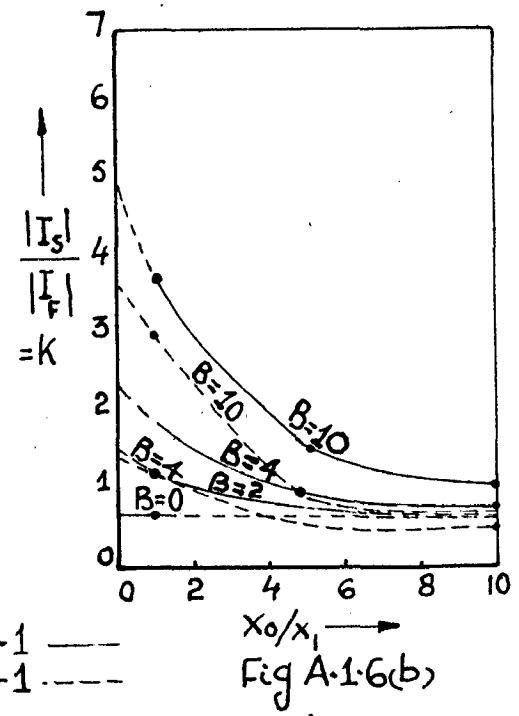


Fig A-1-6(b)

Phases AB to Ground Fault

(3) $I_s = BI_0 + NI_1$

(a) N = +1

X_o/X_1	K (B=0)	K (B=2)	K (B=4)	K (B=8)	K (B=10)
1.0	-0.66	0	0.66	2.00	2.66
5.0	-0.62	-0.415	-0.208	0.208	0.415
10.0	-0.60	-0.49	-0.38	-0.163	-0.05

(b) N = -1

X_o/X_1	K (B=0)	K (B=2)	K (B=4)	K (B=8)	K (B=10)
1.0	0.66	1.33	2.00	3.33	4.00
5.0	0.62	0.83	1.03	1.45	1.66
10.0	1.598	0.708	0.815	1.03	1.14

Similarly for Equation (12) various values of K obtained are tabulated as under-

(a) N = +1

X_o/X_1	K (B=0)	K (B=2)	K (B=4)	K (B=8)	K (B=10)
1.0	0.66	1.15	1.82	3.06	3.72
5.0	0.62	0.75	0.94	1.26	1.45
10.0	0.59	0.66	0.77	0.9	0.99

(b) N = -1

X_o/X_1	K (B=0)	K (B=2)	K (B=4)	K (B=8)	K (B=10)
1.0	0.66	0.66	1.15	2.4	3.06
5.0	0.62	0.54	0.54	0.74	0.90
10.0	0.59	0.55	0.52	0.53	0.57

A graphic plot of these results has been shown in Figs. (A.1.6.a) and (A.1.6.b).

From the above mentioned graphic plots it is quite evident that the combination $MI_2 + NI_1$ will be the best form of combined sequence output. This has been further discussed in article 2.3.

A.2. SELECTION AND CONTROL OF POSITIVE AND NEGATIVE SEQUENCE CURRENTS:

The sequence network used to derive the relaying quantities is shown in Fig.(2.5). The three operating quantities, the positive, the negative and the combined positive and negative sequence components are derived simultaneously by the same network which is supplied from three C.Ts. which are connected in delta.

The delta currents i_p, i_q and i_r, as shown in Fig.(2.5) are fed to the sequence networks and are related to the secondary currents i_a, i_b and i_c as shown in Fig.(A.2.1). The currents I_1' and I_2' passing through the positive and negative sequence network, respectively are given by-

$$I_1' = K\,(i_p + i_q \underline{/60^\circ}) \quad \ldots \qquad \ldots \qquad (i)$$

$$I_2' = K\,(i_p + i_r \underline{/60^\circ}) \quad \ldots \qquad \ldots \qquad (ii)$$

Where, K is a constant, depending upon the loading impedance whose values are maintained equal on both sides of the network.

The combined positive and negative sequence output is obtained by adding the outputs of transformers T_2 and T_3 as shown in Fig.(A.2.2) in one arm of a bridge composed of the two resistors R and the centre tapped transformer T_3, as shown in Fig.(A.2.2). This bridge connection has been specially

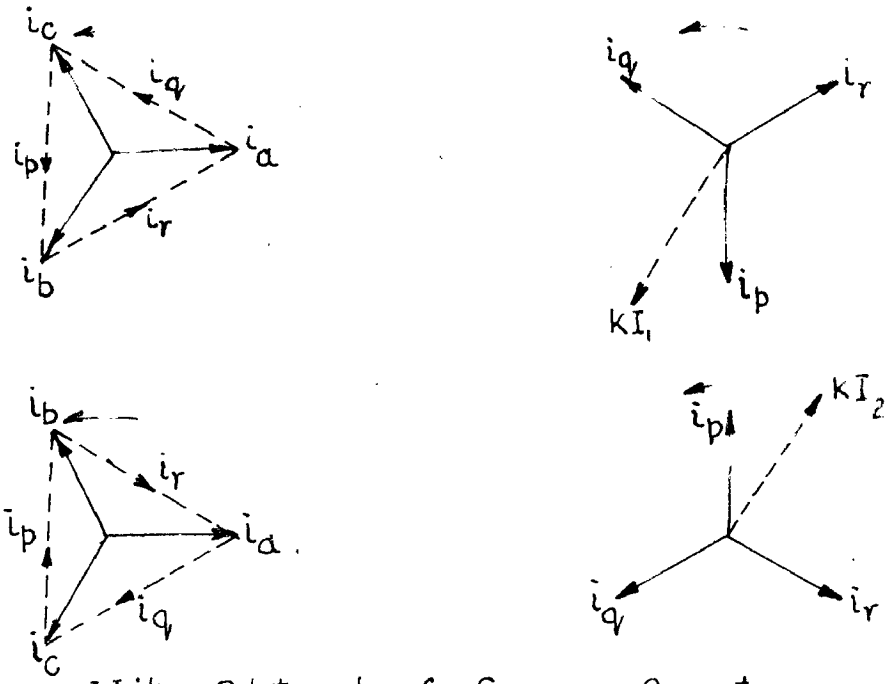


Fig A·21 Vector Relationship for Sequence Currents

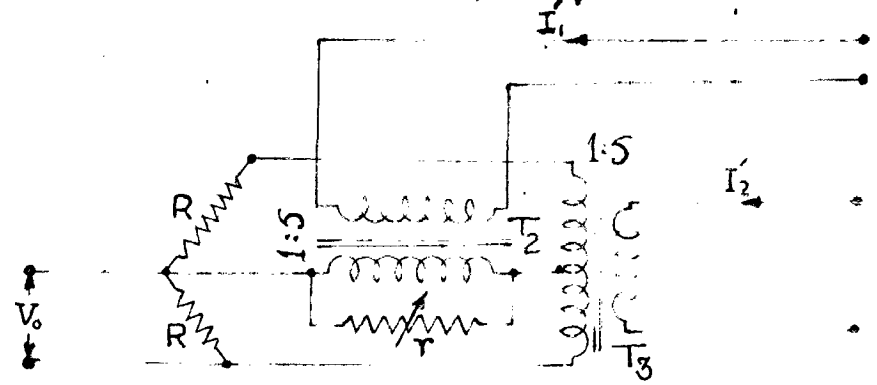


Fig A·22 Combined Negative and Positive Sequence Output

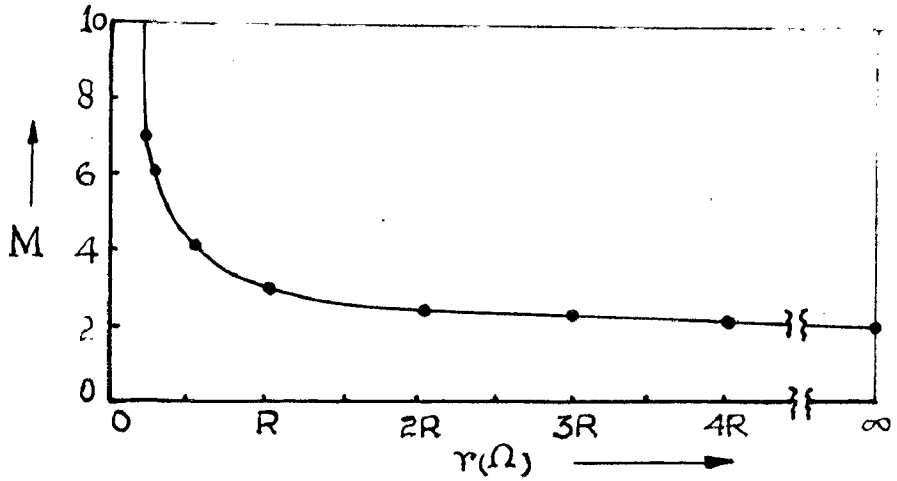


Fig A·23 Variation of M with r.

used here so that the feedback between the positive and negative sequence outputs is avoided.

Refering to the Fig.(A.2.2.), we find that for any value of r connected across the secondary winding of T_2, output voltage V_o is given by-

$$V_o \propto I_2' R + I_1' \cdot \frac{rR}{R+2r}$$

or $$V_o \propto (2 + \frac{R}{r}) I_2' + I_1' \quad \ldots \quad \ldots \quad \text{(iii)}$$

where I_1 and I_2 are the currents on the secondary side of the current transformers as shown in Fig.(A.2.2.)

In Equation (iii) we can write M = (2 + R/r) for the coefficient of I_2,

$$\therefore V_o \simeq MI_2 + NI_1 \quad \ldots \quad \ldots \quad \text{(iv)}$$

Graphic plot of equation M = 2 + R/r has been shown in Fig.(A.2.3.) from which we find that M can have values between 2 and infinity depending on the values of r and that in turn varies the output voltage V_o accordingly.

A.3. FILTERING OF THE COMBINED SEQUENCE OUTPUT VOLTAGE

As described previously, the positive half cycle is used for local tripping whereas the negative half cycle is used for the transmission of blocking carrier. By refering to Fig.(A.3.2.) it is clear that the presence of negative d.c. transient will reduce the duration of normally positive half cycle by the angles θ and ϕ, while a positive d.c. transient will increase it by the angles θ and ψ .

For external faults, the fault currents are approximately the same at both ends of the line, and owing to the phase reversal

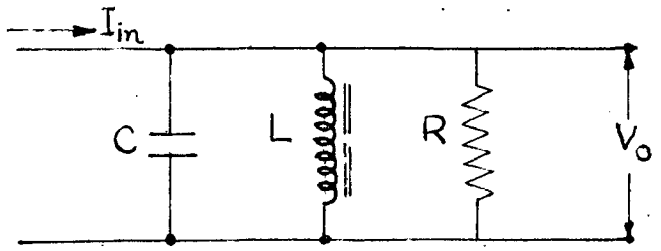


Fig A.3.1 D.C Transient Filter

L=1H, R=400Ω, C=10μF.

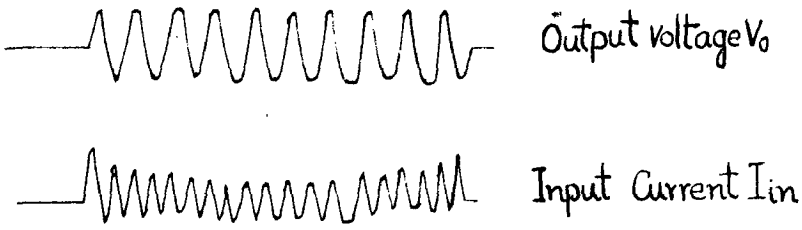


Fig A.3.2 Performance of D.C Filter.

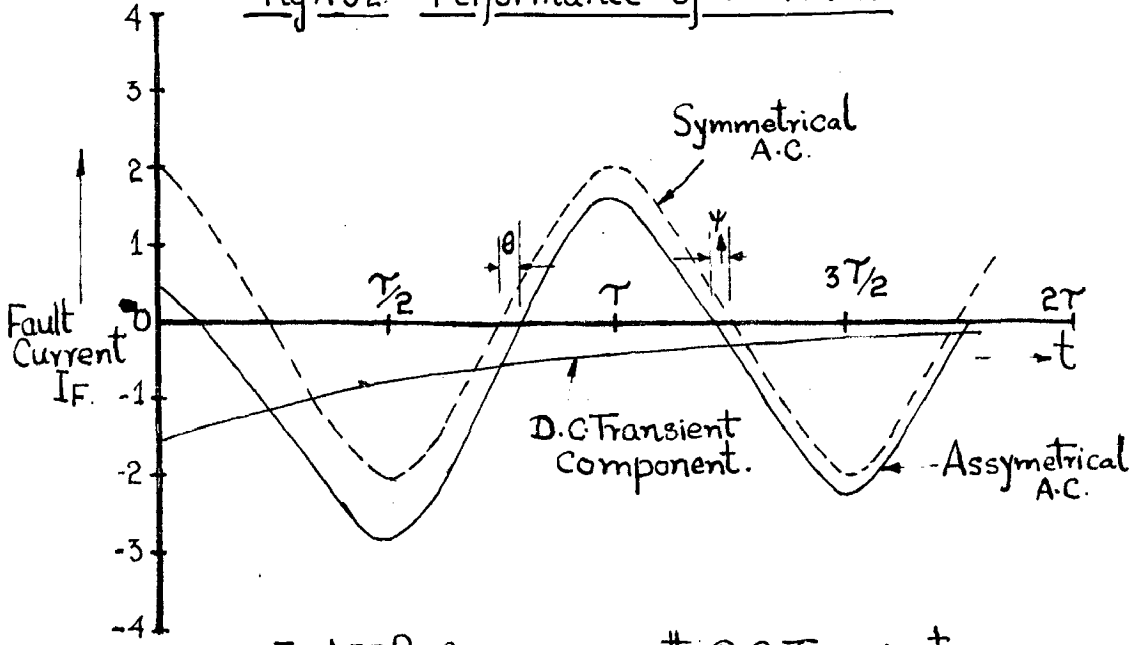


Fig A.3.3 Performance with D.C Transient

of the C.Ts at one end, the d.c. offset, if positive at one end will be negative at the other, and vice-versa. Consequently the total sum of the shift angles will be zero and hence the operation would not be affected.

For internal faults the d.c. offsets at the two ends of the line may be of different magnitudes and polarity. The worst condition can arise when the d.c. offsets at both ends are negative and it may cause a delay in the operation for one complete cycle. However, since the relaying system is intended for fast operation, such a probability of time delay may be undesirable and hence we must eliminate this d.c. transient by using a filter network.

Fig.(A.3.1.) shows the circuit diagram of the d.c. transient filter and Fig.(A.3.3.) shows its performance in the experimental circuit.

REFERENCES

1. C. Adamson and E.A. Talkhan,
"The Applications of Transistors to Phase Comparison Carrier Protection",
Proceedings I.E.E., 106, Part A, No.25, Feb. 1959.

2. C.G. Deway and M.E. Hedges,
"Transistorised Phase Comparison Relaying Principles and Circuits",
Trans. A.I.E.E., 1960, 79 Part III, p.373.

3. S.H. Horowitz, A.J. McConnel and H.T. Seeley,
"Transistorised phase comparison Relaying- Applications and Tests",
Trans. A.I.E.E., 1960, 79, Part III, p.381.

4. W.C. Feaster and E.E. Scheneman,
"Applications of Transistors in Power Line Carrier-Relaying"
Trans. A.I.E.E., 73, 1956, pp.976-979.

5. A.J. McConnel, T.A. Cramer and H.T. Sheeley,
"Phase Comparison Carrier Current Protection",
Trans. A.I.E.E., 64, 1945, pp.825-833.

6. F.M. Rives,
"Application of Carrier to Power Lines",
Trans. A.I.E.E., 1943, Vol.62, pp.835-44.

7. A.F. Drompp, H.W. Lensner, S.L. Goldsborough, T.R. Halmann,
"A new Carrier Relaying System",
Trans.A.I.E.E., Vol.63, 1944, pp.568-572.

8. R.C. Cheek and J.L. Blackburn,
"Considerations in Selecting a Carrier Relaying System",
Trans.A.I.E.E., 1952, Vol.71, page 10-15.

9. H.W. Lensner,
"Protective Relaying over Microwave channels",
Trans. A.I.E.E., 1952, Vol.71, p.240-4.

10. J.R. Nowichi,
"Phase Operated Relay using Transistors for Power System Protection",
Mullard Tech.Commun., 4, July 1958, p.7-13.

11. H.W. Lensner,
"Operation of Power Line Carrier Channels",
Trans. A.I.E.E. 1947, Vol.66, p.888-93.

12. Some recent developments in the Protection of E.H.V. O/H networks,
C.I.G.R.E. 1946, Vol.3,
report 338, 26 pp.
Phase Comparison Scheme.

13. E.W. Kimbark,
"Power System Stability - Power Circuit Breakers and Protective Relays",
Vol.II, Print July 1962, p.114.

14. H. Pender, W.A. Delmar and K. Mcilwain,
"Electrical Engineers Hand Book".