Design and Performance of an Automatic Synchronising Unit for Synchronous Machines

A Dissertation
submitted in partial fulfilment
of the requirements for the Degree
of
MASTER OF ENGINEERING
in
POWER SYSTEM ENGINEERING

By

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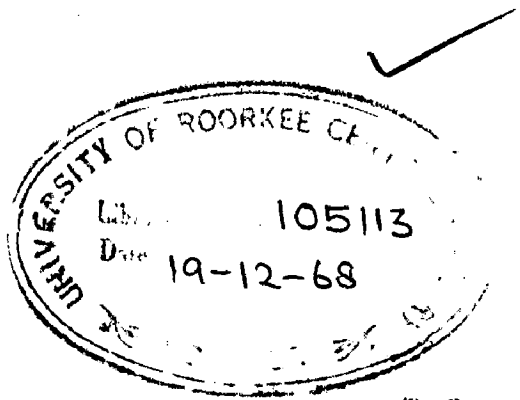

DEPARTMENT OF ELECTRICAL ENGINEERING
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ROORKEE

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C E R T I F I C A T E

Certified that the dissertation entitled "DESIGN AND PERFORMANCE OF AN AUTOMATIC SYNCHRONISING UNIT FOR SYNCHRONOUS MACHINES", which is being submitted by Shri Narsingh Dass Batra in partial fulfilment for the award of the Degree of Master of Engineering in "Power System Engineering" of University of Roorkee is a record of student's own work carried out by him under my supervision and guidance. The matter embodied in this dissertation ~~has~~ has not been submitted for the award of any other Degree or Diploma.

This is further to certify that he has worked for a period of 9 months from January to September 1968 for preparing dissertation for Master of Engineering Degree at the University.

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Dated October 20, 1968

A C K N O W L E D G E M E N T

The author wishes to express his deep sense of gratitude and indebtedness to his guide Dr. T.S.M. Rao, Professor and Head of Electrical Engineering Department, University of Roorkee, Roorkee for suggesting the problem, valuable advice and for providing all possible facilities for fabrication and testing of the Automatic Synchronising Unit, without which it would have been impossible to complete this work.

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C O N T E N T S

I N T R O D U C T I O N

A number of synchronising relays are manufactured commercially, most of which use dynamic relaying elements. They have employed electrically interlocked relays which operate each time the phase angle between the machine and line voltages becomes zero. These automatic synchronisers have given excellent service in a variety of applications. However, it has become evident that faster and more accurate synchronising could be obtained if the interlocking relays were eliminated and their functions performed by electronic means. The present trend has been to investigate the possibilities of applying transistors and semiconductor components to the problems of an entirely static synchronising relay. All the necessary functions of voltage regulation, phase and slip measurements can be achieved successfully using static relaying principles. The automatic transistorised synchroniser described in the dissertation permits taking advantage of faster circuit breaker closing speeds and provides more accurate synchronising then the equipment with mechanical interlocking relays.

S Y M B O L S

Unless otherwise stated, following notations will be used.

S_1, S_2	=	Control signals derived from sources to be synchronised
w_1, w_2, f_1, f_2	=	Frequencies of sources to be synchronised rad/sec and c/second.
f_s	=	Slip frequency ($f_1 - f_2$) c/s
δf and δV	=	deviations in frequency and voltage which are permissible for synchronisation
δ_s	=	Angular displacement at which closure is initiated.
S_a, S_b, S_c and S_d	=	Slip frequency control signals
α	=	phase displacement between slip frequency control signals.
τ	=	Width of slip frequency wave form
τ_c	=	Minimum width of slip frequency waveform for synchronisation.
R	=	Load resistance in diode modulator
R_a	=	Armature resistance
R_b	=	Input resistance of Transistor
r_b	=	Base emitter impedance of Transistor
δ	=	Torqiie or power angle
V	=	Terminal voltage
E	=	Voltage induced
P	=	Power
T	=	Torqie

T_1, T_2, T_3	=	Transistors
X	=	Reactance
X_d	=	Direct axis reactance
X'_d	=	Direct axis transient reactance
X''_d	=	Direct axis subtransient reactance
X_q	=	Quadrature axis reactance
I_d	=	Direct axis current
I_q	=	Quadrature axis current
X_s	=	Synchronous reactance
X_2	=	Negative sequence reactance
I_b	=	Base current
α''	=	Amplification factor
Z'_d	=	$(R + j X'_d)$
n	=	total number of alternators including the incoming one

CHAPTER - I

S Y N C H R O N I S E R S

1.1 INTRODUCTION

Success of connecting two a.c sources in parallel depends upon securing small and diminishing deviations in the magnitude, phase and frequency of the two sources. In order that two sources of high power ratings and low internal impedances can be connected in parallel, some limitations must be imposed on the phase and frequency of the incoming source, so that no disturbance or discontinuity of power takes place. At the moment of synchronisation i.e. when circuit breaker connecting the incoming voltage source to the running supply should complete the circuit, three conditions must be fulfilled.

1. The difference in time phase between the incoming and running voltages must be small and decreasing with time.

2. The difference in the frequency between two voltage supplies should be small i.e. slip frequency of 0.5% of the supply source frequency.

3. The difference in magnitude between two voltages must be small. The permissible difference will depend upon the characteristics of the incoming system and the running one. The difference, however should not increase 5%.

For successful parallel operation of the alternators, there are many synchronisers available such as

(1) Lamp Synchronisers
  (a) Dark lamp method
  (b) Bright lamp method

But they are only suitable for small low-voltage machines.

1.2 SYNCHROSCOPE

For large machines a rotary synchroscope is almost invariably used. This synchroscope, which is based on the rotating field principle, consists of a small motor with both field and rotor wound two phase. The stator is supplied by a pressure transformer connected to two of the main bus-bars while the rotor is supplied through a P.T. connected to the corresponding pair of terminals on the incoming machine. This instrument indicates the difference in phase between two electromotive forces at every instant. By it, one can see whether the incoming machine is running fast or slow, what the difference in speed is and the exact instant when synchronism occurs. It has a pointer which shows the phase angle between the running and incoming machines. When the frequencies of two machines are equal, the pointer stops at some position on the scale and when the machines are in phase, the pointer coincides with the marker at the top of the scale.

1.3 FREQUENCY MATCHING

A simple method of bringing the incoming machine to the same frequency as the bus is to provide the Diesel engine governor with a speed matcher. This consists of two-three phase squirrel cage induction motors, and a differential gear mechanism. The horizontal shaft of the differential gear mechanism acts through a suitable gearing on the speed adjuster of the governor. One motor is connected to the bus and the other to the incoming machine, the first increases the engine speed and the second reduces it. The speed matcher may be put into operation either by a manual switch or by a relay of an automatic synchroniser. Since the motors act in opposition to each other, any difference in speed between the two machines will cause the horizontal shaft of the differential gear mechanism to set the governor speed adjuster so as to bring the speeds parallel as nearly as possible. When the frequencies are equal, the shaft of differential gear will stop operation and remain stationary. After the frequencies have been matched, it is necessary, that before the two machines are put in parallel operation, to see that their voltages are approximately equal and to wait until the synchronising lamps or synchroscope shows that machines are exactly in phase.

1.4 SPECIAL SYNCHRONISING TRANSFORMER

The figure 1.1 is a special type of transformer for use in connection with a single synchronising lamp. If the voltages of the bus bars and the incoming generator are in phase with respect to the external load circuit, then appropriate connections to the exciting windings on the two outer legs of the core will cause their fluxes to neutralise in the middle leg. A lamp connected to the middle winding will then be dark. If there is any phase difference between the voltages of the two machines to be synchronised, some flux will pass through the middle core and the lamp will glow.

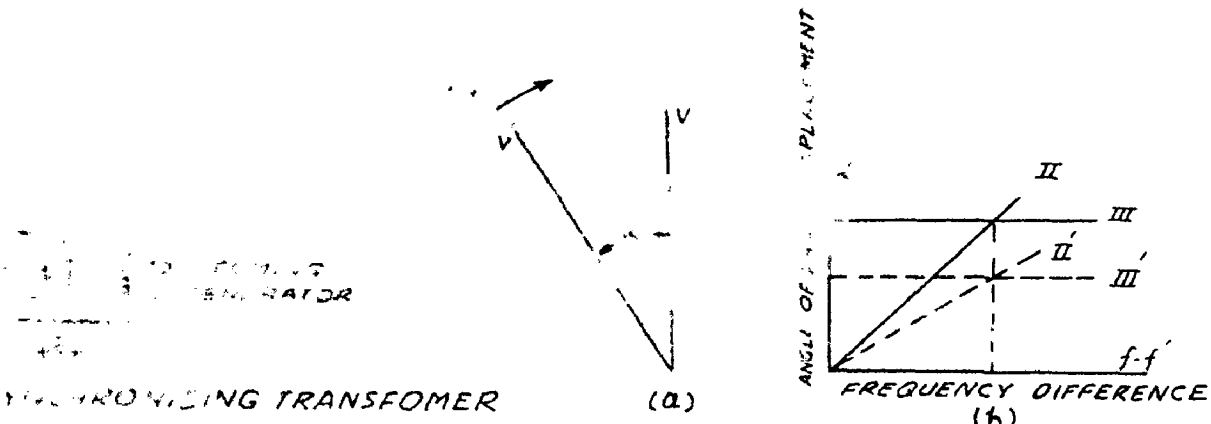
1.5 AUTOMATIC SYNCHRONISING

Synchronisation by means of manually operated switching served well when individual generators were relatively small, but with the growth of system capacity and ratings of the generating units themselves, it has become essential to adopt automatic devices to ensure the closing of the main switch of the incoming machine at the proper instant. Because of the size and inertia of the moving parts of the circuit breaker, and the time delay in its control mechanism, a finite time, varying from 0.2 to 0.8 seconds is required for the closing of the main contacts after the triggering of its actuating mechanism. So unless the

closing coil of the relay which actuates the circuit breaker, is energised at the right moment, the main contacts may close when the voltages V and V' (Fig. 1.2a) are so far from phase coincidence that a very large equalizing current may flow to cause a serious system disturbance.

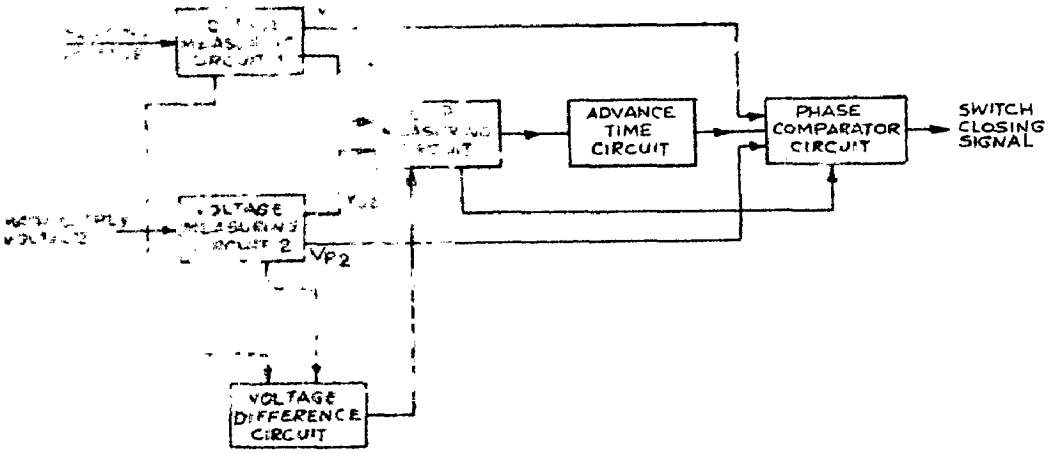
Let V and V' be the assumed equal voltages of the bus bar and of the incoming machine. V alternates at frequency f and V' at frequency f' such that $f' < f$. Phaser V' is rotating slowly in clockwise direction relative to the stationary phaser V at a frequency f - f' and angle $\alpha = 2\pi(f - f')t$, where t is the time required for two voltages to be coincident. If t is the overall time lag of the circuit breaker, then for a given frequency difference f-f' the angle α is the phase displacement between V and V' at the moment when the closing relay should be initially started.

In order to design the equipment which will automatically close the main circuit breaker at the moment when V and V' are in phase (with respect to the external circuit), there must be provided two contact making relays II and III, such that one of them, say III operates only when angle α has a predetermined value and the other operates only when f-f' has such a value that $t = \frac{\alpha}{2\pi(f-f')}$ is the



SYNCHRONISING TRANSFOMER

FIG 1.2 ADJUSTABLE SETTINGS OF RELAYS



BLOCK DIAGRAM OF AUTOMATIC SYNCHRONISING RELAY

time lag of the main breaker. The contacts of relays II and III, connected in series, will then serve to energise the closing coil of the main circuit breaker only when α and f-f' are simultaneously at the correct values.

Relay III is designed so that it may be set to close its contacts when the phase angle α lies anywhere between definite limits as shown in fig. 1.2b, but in such a way that the closure is independent of the frequency difference f-f' on the other hand relay II is designed to give a response proportional to f-f' but its slope in the graph is adjustable. Simultaneous operation is then determined by the point of intersection of the lines marked II and III.

1.5.1 AMPLITUDE COMPARISON SYNCHRONISER

Amplitude comparison underlays the derivation of slip and phase displacement checking signals. The techniques involved would be dealt in detail in the proceeding chapters.

The overall requirements are indicated in fig. 1.3. The two voltage measuring circuits each supply two outputs, V_{s1}, V_{p1} and V_{s2}, V_{p2}. V_{s1} and V_{s2} are supplied to circuits which measure the slip, with the provision that if initial voltage difference is too great, the slip measuring arrangement will give

no output. The outputs V_{p1} and V_{p2} are applied to phase measuring circuits with the provision that there will be no output if the slip is too great. Control from the slip measuring circuit is exerted through a time advance arrangement which ensures that any output signal for closure of the circuit making switch occurs at a time T_c before the precise instant of phase coincidence of the incoming and main supply voltages, T_c is thus time from the issue of a closing signal from the synchronising equipment to the instant that the closing switch effectively makes the circuit.

1.5.2 PHASE COMPARISON METHOD

In this frequency and phase displacement derivations are assessed using methods of phase comparison. The derivation of slip dependent control signals using a balanced bridge ring modulator is developed. Two methods of indicating the instant of zero phase displacement to allow for the operating time of the connecting circuit breaker are available.

1). This interprets the required period as an angle deviation and is accurate at one slip frequency, while the advanced time features of the second method more accurately match the fixed delay of the circuit breaker, at least over the frequency spectrum for which synchronisation is to be allowed. This employs logical circuits

for automatic synchronisation shown in block diagram 1.4. A signal is generated which causes closure of the circuit breaker when each is simultaneously within a specified limit and separate control signals, which are used for manual or automatic adjustment of voltage and speed of the incoming machines until they have attained values essential for synchronisation. To allow for the circuit breaker operating time, the final closure pulse should anticipate the instant of zero phase displacement between the two sources and the function of the time compensation is to allow for this, the allowance ideally being independent of slip frequency whereas the phase displacement measurement is instantaneous. The measurement once obtained is stored until phase conditions are correct for operation of the connecting circuit breaker. Separate stores are shown in the slip frequency and amplitude measurements. The outputs are given to "and" gate from which the circuit breaker closure pulse is given under conditions permissible for synchronisation. The arrangement is, in general, one of the repeated measurements in each slip cycle, but they may take place at or during different intervals in the cycle and thus requires time coordination, shown in the form of information stores.

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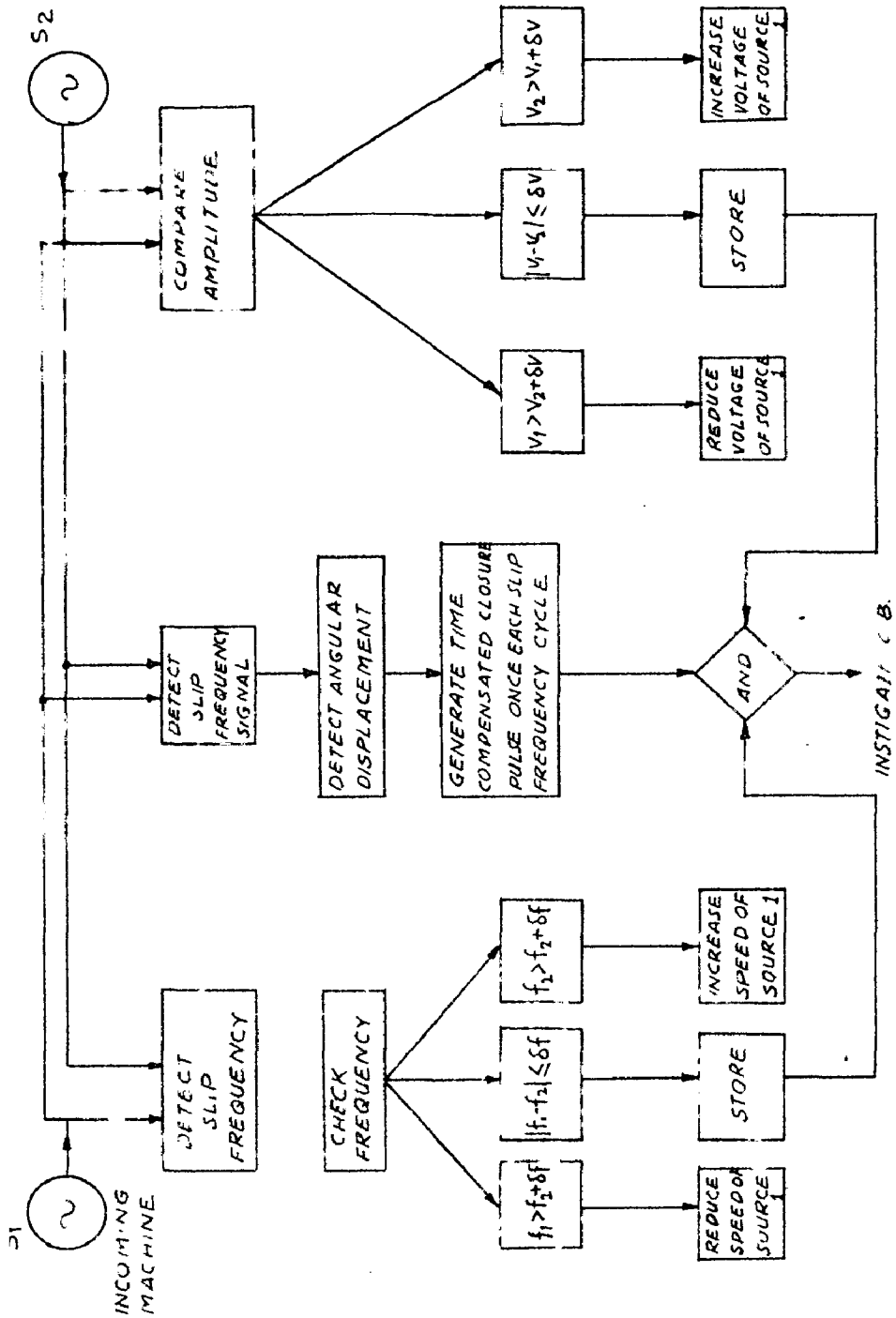


FIG 1·4 LOGICAL STEPS FOR SYNCHRONISATION

CHAPTER - II

CHARACTERISTICS DURING SYNCHRONISATION

2.1 If a generator is paralleled with a machine of identical characteristics when its voltage is exactly equal to and in phase with the bus bar voltage of the one already under load, it will not relieve the latter of any of its load provided the speeds are exactly equal. It will merely continue to run without either supplying any current to the bus bars or taking any current from them. Under these conditions, voltages V_1 and V_2 measured at their point of connection at switch S in figure 2.10 are equal in magnitude and in exact phase opposition with respect to the local circuit in which they have a series relation.

Suppose that at the moment of synchronising generator G_2 its terminal voltage V_2 while numerically equal to the bus bar voltage V_1 is not exactly opposite in phase to V_1 but falls short of complete opposition because G_2 is at the moment is running slightly slower than G_1. This condition is shown in figure b. There is a resultant voltage E_c which sets up current I_c lagging behind E_c by an angle ϕ_s such that

$$\tan \phi_s = \frac{X_{s1} + X_{s2}}{R_{a1} + R_{a2}} \quad \ldots \quad \ldots \quad (2.1)$$

where $X_{s1} = X_{s2} = X_s$ is the synchronous reactance of each of the two identical machines and $R_{a1} = R_{a2} = R_a$ is

their common armature resistance.

$$\text{Current } I_c = \frac{E_c}{2Z_s} = \frac{E_c}{2(R_a + JX_s)} \quad \ldots \quad (2.2)$$

from figure2.4(b) it is evident that the circulating current I_c which is in addition to the load current already being supplied by G_1, has a component in phase with V_1 and hence implies an additional load on G_1, which tends to slow it down. I_c has a component in opposition to V_2, machine G_2 develops motor action which tends to raise its speed. If on the other hand, G_2 is running slightly faster than G_1, voltage V_2 will be somewhat ahead of V_1 as in figure c and the resultant circulating current will cause G_2 to develop generator power, tending to reduce its speed while G_1 develops motor action to raise its speed.

Another aspect of this interchange of generator and motor action is evident from a consideration of the case of two identical generators running in exact synchronism with equal excitations and voltages V_1 and V_2 in exact phase opposition. Hence no circulating current and the machines will divide the external load equally. Any change in load, say, a sudden increase, will cause a momentary slowing down of both machines, but even a slight difference in the sensitivity of their governing mechanisms will cause one of the two machines to take more than its share of load increment

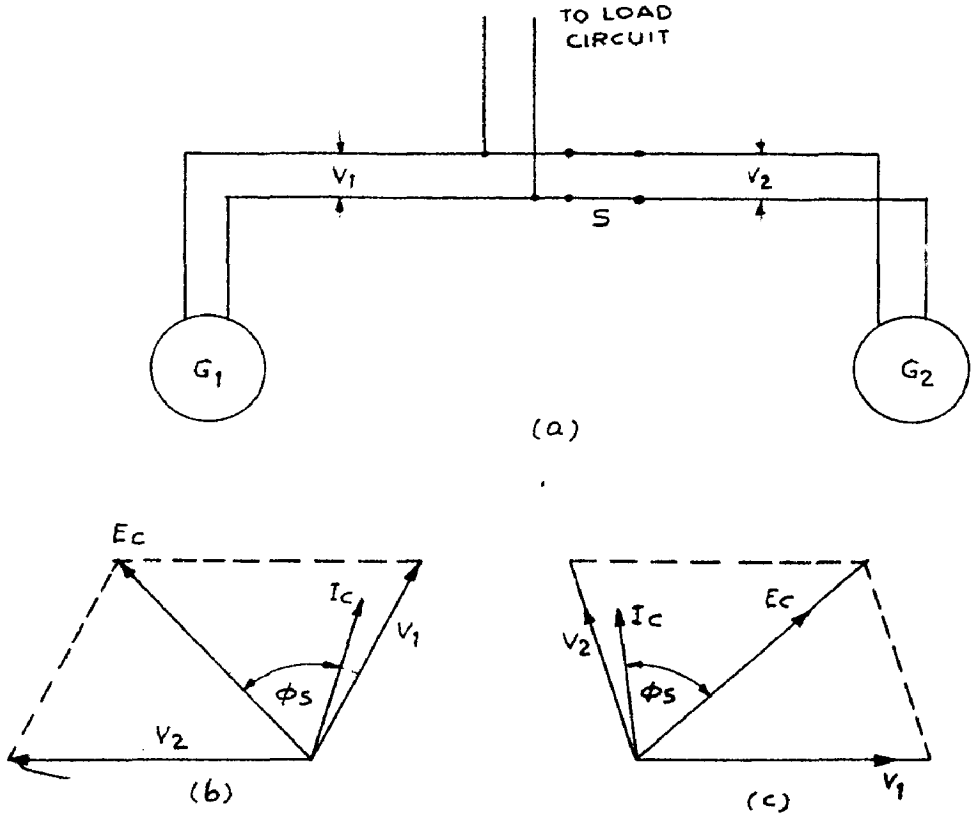

TO LOAD
CIRCUIT
V1
V2
S
G1
G2
(a)
Ec
Ic
V1
φs
V2
(b)
V2
Ic
Ec
φs
V1
(c)

FIG. 2.1

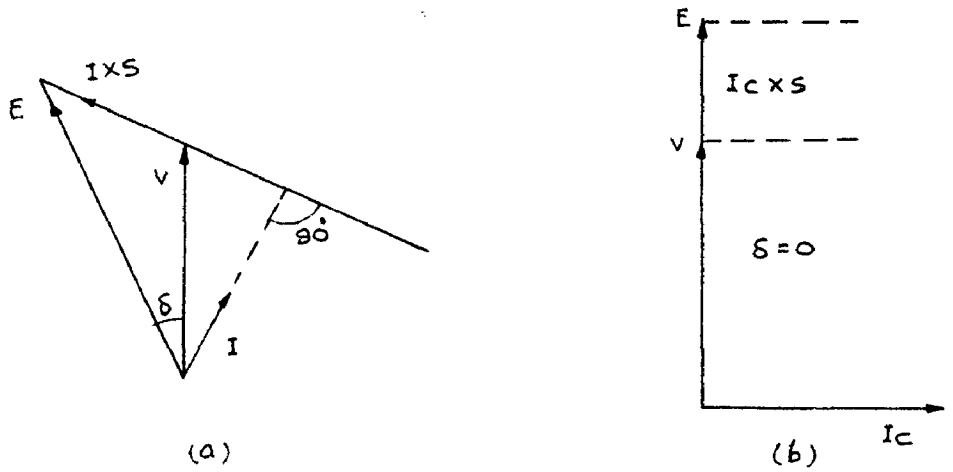

IXS
E
V
90°
δ
I
(a)
E
Ic x s
V
δ=0
Ic
(b)

FIG. 2.2

for instance, G_1 takes the greater part of the increased load, so causing it to slow down relative to G_2 so that G_2 will relatively pull ahead until V_1 and V_2 assume the positions indicated in fig. C. The resultant generator action of G_2 will then tend to restore the original equal division of the load.

So there is an automatic synchronising action which tends to hold the mechanism in step. This inherent synchronising power is primarily due to the elastic reaction between the magnetic fields of the stator and rotor of each machine, which may be assumed as due to a tension acting along the lines of magnetic induction in the air gaps. The synchronising power vanishes at the stability limit, so that if the two machines swing too far apart, they will fall out of step.

2.2 POWER OUTPUT OF GENERATORS IN PARALLEL

In accordance with the synchronous reactance theory, the power developed by a cylinderical rotor machine is given by

$$P = \frac{VE \cos (\phi_s - \delta)}{Z_s} - \frac{E^2 \cos \phi_s}{Z_s} \quad .. \quad (2.3)$$

where $Z_s = R_a + JX_s$

and $\phi_s = \tan^{-1} \frac{X_s}{R_a}$

Power developed by a salient-pole machine is given by

$$P = \frac{VE}{Xd} \text{ Sin } \delta + \frac{V^2(\lambda_d - \lambda_q)}{2X_d \lambda_q} \text{ Sin } 2\delta \quad \ldots \quad (2.4)$$

δ = torque or power angle

= angular displacement between V and E

V = terminal voltage

E = voltage induced by excitation

If R_a is very small in comparison with X_s, then

$$\phi_s = \tan^{-1} \alpha = 90°$$

and $$P = \frac{VE \text{ Cos } (90 - \delta)}{X_s} - \frac{E^2 \text{ Cos } 90°}{X_s}$$

$$= \frac{VE \text{ Sin } \delta}{X_s} \quad \ldots \quad \ldots \quad \ldots \quad (2.5)$$

and if in equation 2.4, $X_d = X_q = X_s$ then it becomes

$$P = \frac{VE}{X_s} \text{ Sin } \delta \quad \ldots \quad \ldots \quad (2.5)$$

which is the characteristic of a cylindrical rotor. In order that the generator may supply power to the line, the angle δ must take such a value as to satisfy the equation $P = \frac{VE}{X_s} \text{ Sin } \delta$ which means that for given excitation (i.e. for given value of E), the rotor of generator must be forced ahead of the position of the field structure of a hypothetical generator which maintains the terminal voltage V and which rotates at constant angular velocity. It means that if the

load carried by a synchronous generator is to be increased when it is operating in parallel with others which maintain constant terminal voltage, additional power must be supplied to it by its prime mover.

2.3 EFFECT OF VARYING THE EXCITATION

(a) Excitation E is in phase with V but E > V. Neglecting the resistance, the voltage difference E - V will cause a circulating current I_c in quadrature with both E and V. This current lags behind E and so exerts a demagnetising action to counter act the excessive field excitation.

(b) When E < V and $\delta = 0$, circulating current I_c leads E and exerts a magnetising action to compensate for the deficient excitation.

But inneither case is there any power developed. So the adjustment f the field excitation of an alternator will not affect its output when running in parallel with other machines which maintain constant bus voltage, but it will result in the circulating current which is undesirable because of its heating effect.

2.4 SYNCHRONISING DISTURBANCES

The alternator in its simplest aspects is an ideal voltage source feeding its load through a variable impedance.

Under balanced conditions only one phase need be considered. Figures 2.3a and b show the equivalent circuit of a phase diagram of a non salient pole alternator and fig 2.3c, a phasor diagram of a salient pole machine

From fig 2.3(a) and (b) the terminal voltage of a non salient machine is

$$V = E - I(R + JX_d) \quad \ldots \quad \ldots \quad (2.6)$$

and from fig 2.3c that of a salient pole alternator is

$$V = E - JI_qX_q - JX_dI_d \quad \ldots\ldots \quad (2.7)$$

Improper synchronizing of alternators results in dips in the system voltage and a large interchange of powers between the incoming and the system. If the effect of saliency is neglected and values are substituted for δ(torque angle) along with values of resistance and reactance, the loci of the power phasor are two families of ellipses :-

2.4.1 DERIVATION OF POWER EQUATIONS

Consider an unloaded bus supplied by (n-1) alternators and to which an alternator 1 is connected when its voltage leads that of the bus by the angle δ.

Let the voltages be expressed

$$E_n = |E| + J0$$

$$E_1 = |E| (\text{Cos } \delta + J \text{ Sin } \delta)$$

If the effect of saliency is neglected, the current is given by

$$I = \frac{\left[|E| + J0\right] - \left[|E|\ (\text{Cos}\ \delta + J\ \text{Sin}\ \delta)\right]}{Z'_d + \frac{Z'_d}{n-1}} \quad \ldots (2.8)$$

$$= \frac{|E|\ (1 - \text{Cos}\ \delta - J\ \text{Sin}\ \delta)}{Z'_d + \frac{Z'_d}{n-1}}$$

where

n = total number of alternators including the incoming alternator

$Z'_d = R + JX'_d$

R = Resistance of the armature plus that of the leads to the bus.

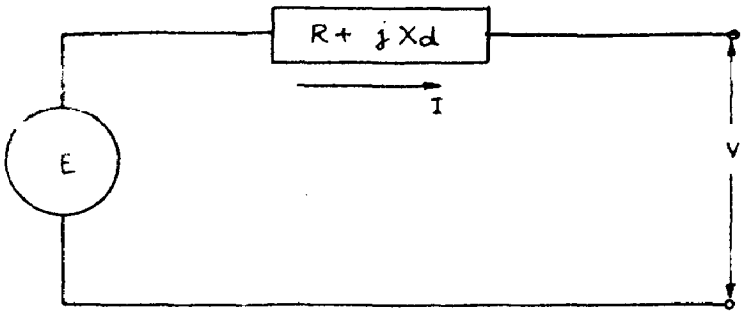
X'_d = transient reactance of the alternator plus the reactance of the leads to the bus

The terminal voltage V in terms of |E| and δ is

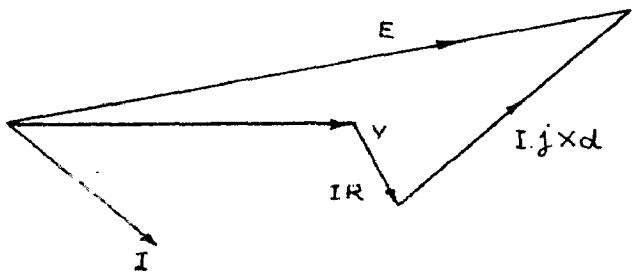
$$V = E_n - \frac{Z'_d}{n-1} I = |E| \left[1 - \frac{1 - \text{Cos}\ \delta}{n} + J \frac{\text{Sin}\delta}{n}\right] \quad (2.9$$

The equations for the real and reactive power delivered by the incoming alternator are respectively

Power = I x conjugate of V

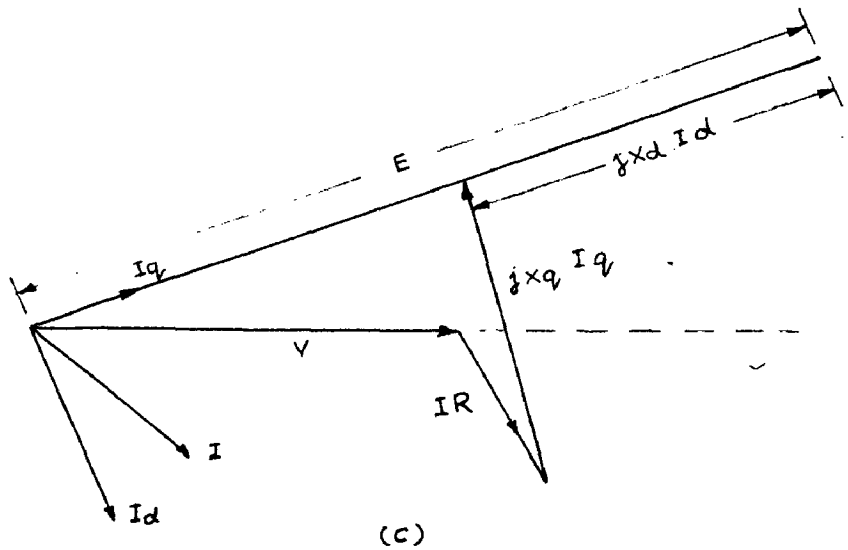


(a)



(b)

3 a & b. PHASE DIAGRAM OF NON SALIENT POLE MACHINE



(c)

FIG. 2.3C. FOR SALIENT POLE MACHINE

$$= \frac{|E|(1 - \cos\delta - J\sin\delta)}{Z_d' + \frac{Z_d'}{n-1}} |E| \times \frac{\wedge}{1 - \frac{1-\cos\delta}{n} + J\frac{\sin\delta}{n}}$$

$$= \frac{|E|(1 - \cos\delta - J\sin\delta)}{Z_d'(\frac{n}{n-1})} \times |E|\left[1 - \frac{1-\cos\delta}{n} - J\frac{\sin\delta}{n}\right]$$

$$= \frac{|E|^2}{|Z_d'|^2}(\frac{n-1}{n})\left[1 - \frac{1-\cos\delta}{n} - J\frac{\sin\delta}{n}\right] \times$$

$$\left[1 - \cos\delta - J\sin\delta\right]\ (R + JX_d')$$

$$= \frac{n-1}{n}\ \frac{|E|^2}{|Z_d'|^2}\left[\frac{n-1+\cos\delta}{n} - J\frac{\sin\delta}{n}\right] \times$$

$$\left[R(1-\cos\delta) + X_d'\sin\delta - JR\sin\delta + JX_d'(1-\cos\delta)\right]$$

$$\text{Power} = \frac{n-1}{n}\frac{E^2}{Z_d'^2}\ \frac{n-1+\cos\delta}{n} - J\frac{\sin\delta}{n}$$

$$\left[R(1-\cos\delta) + X_d'\sin\delta + \quad\quad -J(X_d'\overline{1-\cos\delta} - R\sin\delta)\right]$$

Separating this into its real and imaginary parts

$$\text{Real power } P_1 = \frac{n-1}{n}\frac{|E|^2}{|Z_d'|^2}\left[\left(\frac{n-1+\cos\delta}{n}\right)\right.$$

$$\left.\left(R\overline{1-\cos\delta} + X_d'\sin\delta\right) + \frac{\sin\delta}{n}(X_d'\overline{1-\cos\delta} - R\sin\delta)\right]$$

$$= \frac{n-1}{n} \frac{|E|^2}{|Z_d'|^2} \frac{1}{n}\left[nR - nR\,\cos\delta - R(\cos^2\delta+\sin^2\delta)\right.$$

$$\left. - R + 2R\,\cos\delta + nX_d' \sin\delta\right]$$

$$= \frac{n-1}{n} \frac{|E|^2}{|Z_d'|^2} \frac{1}{n}\left[nR(1-\cos\delta) - 2R + 2R\,\cos\delta + nX_d' \sin\delta\right]$$

$$= \frac{n-1}{n} \frac{|E|^2}{|Z_d'|^2} \frac{1}{n}\left[(1-\cos\delta)(-nR + 2R) + nX_d' \sin\delta\right]$$

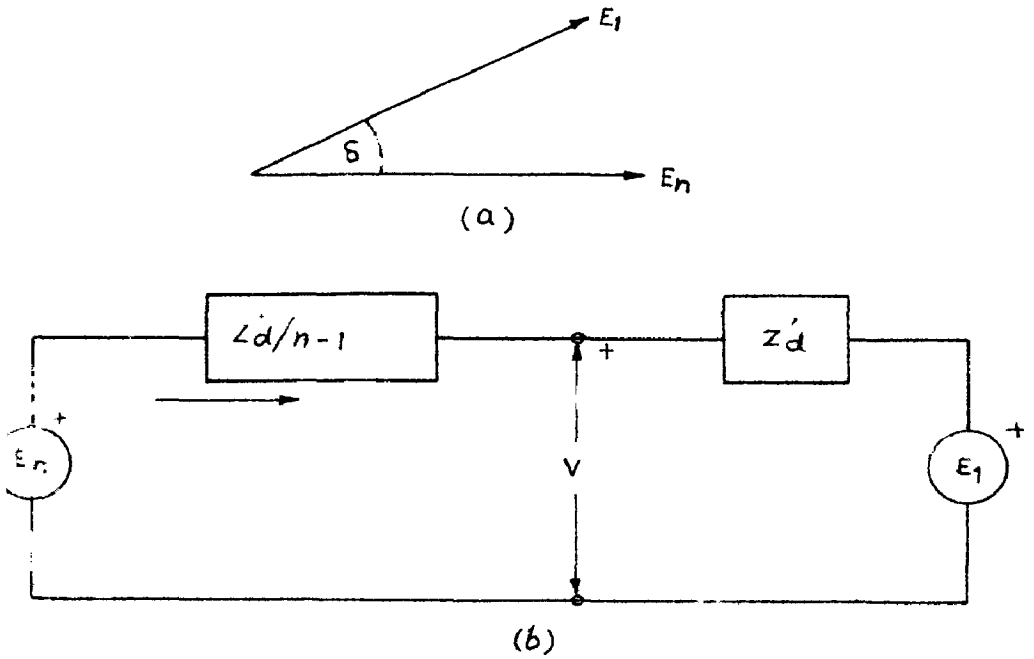
$$= -\frac{n-1}{n} \frac{|E|^2}{|Z_d'|^2}\left[R(1-\cos\delta)\frac{n-2}{n} - X_d' \sin\delta\right] \quad \ldots (2.10)$$

Similarly the imaginary part i.e. reactive power

$$Q_1 = -\frac{(n-1)}{n} \frac{|E|^2}{|Z_d'|^2}\left[X_d' \frac{n-2}{n}(1-\cos\delta) + R \sin\delta\right] \quad (2.11)$$

The dotted ellipses represent the loci of the power phase for each of the (n-1) alternators already on the bus and the solid ellipses are the loci for the incoming alternator. Fig 2.5

For a 2 - alternator system n = 2, the two ellipses become one straight line through the origin.
For an alternator synchronised to an infinite bus bar, $n = \infty$ the ellipse for the incoming alternator becomes a circle and that for any of the other alternators, the maximum reactive power which an incoming alternator may deliver is small compared to that which it may draw from the system.



G. 2.4. CONDITIONS AT TIME OF SYNCHRONISING
(a) VOLTAGE RELATIONSHIP
(b) EQUIVALENT CIRCUIT

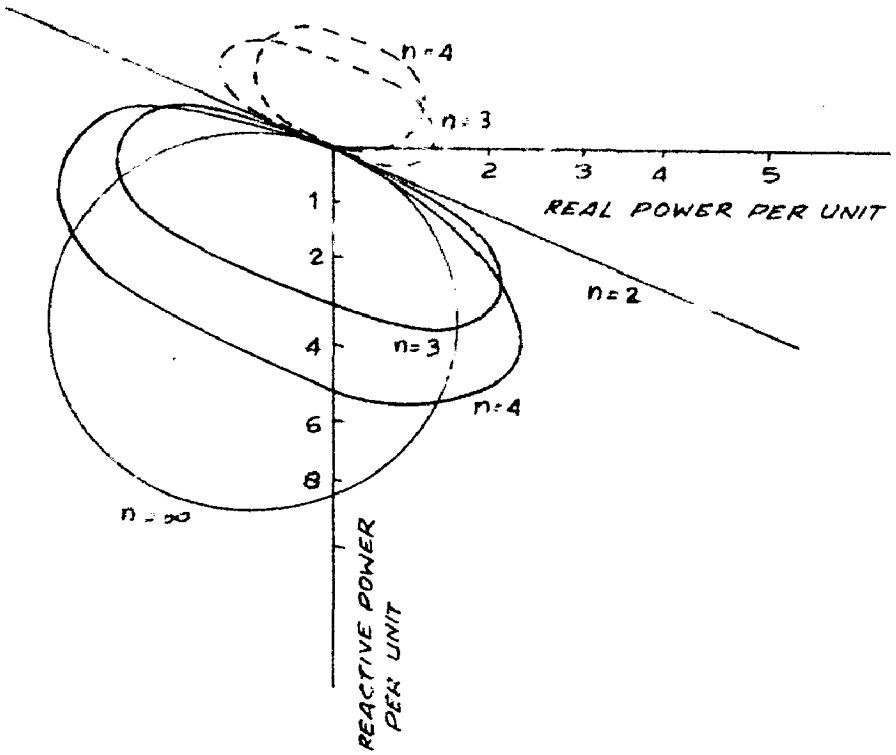


FIG 2.5

However, large swings of the real power may result depending upon the value of δ at the time of synchronising.

If n = 2 and the alternators are synchronised out of phase then for an alternator having R = 0.043 and X'_d=0.15 per unit values,
the ratio of P to Q from equations (2.1o) and (2.11) becomes

$$P/Q = \frac{X'd}{R} = \frac{0.15}{0.043} = 3.5$$

but from the oscillograms, it is found to be slightly higher
Equation (2.9) for the bus voltage shows that the power oscillations are accompanied by a reduction in the bus voltage. For the most severe condition when 180° out of phase, the bus voltage goes to zero and the armature current from equation (2.8) is

$$I = \frac{|E'| (1-\cos\delta - J \sin\delta)}{Z'_d + \frac{Z'_d}{n-1)}} \quad \ldots \quad (2.8)$$

Now $\delta = 180 \quad \therefore \cos\delta = 1, \quad \sin\delta = 0$

$$Z'_d = R + JX'_d = \frac{0.043 + J.\ 0.15}{\sqrt{(0.043)^2+(0.15)^2}} = 0.156$$

for n = 2

$$I = \frac{|E| (1 + 1 - 0)}{0.156 + \frac{0.156}{2-1}} = |E| \frac{1}{.156} = |E| 6.5$$

Hence armature current for a 2-alternator system is 6.5 times per unit. For an infinite system the bus voltage is uneffected but the current in the incoming alternator becomes for $n = \infty$

$$I = \frac{|E|\,(1+1-0)}{0.156 + \frac{0.156}{\infty}} = \frac{|E| \times 2}{0.156} = |E| \times 13.0$$

is 13.0 per unit or twice the available 3 phase. Short circuit current

Such an extreme transient current as 13.0 per unit would cause the exciter to reverse its polarity which causes the stabilising transformer in the voltage regulating circuit of malfunction.

2.5 LOSS OF FIELD EXCITATION

An alternator may lose its field of excitation as a result of an open circuit or complete short circuit in either its own field circuit or in the exciter field circuit.

The expressions for the real power delivered to and the reactive power drawn from the system for an alternator having zero excitation are as follows.

The power developed by a salient pole machine is

$$P = \frac{VE}{X'_d} \text{ Sin } \delta + \frac{V^2(X_d - X_q)}{2X_dX_q} \text{ Sin } 2\delta$$

and where $E = 0$

$$P = \frac{X_d - X_q}{2X_dX_q} |V|^2 \text{ Sin } 2\delta \quad \ldots \quad \ldots \quad (2.12)$$

$$\text{and } Q = \frac{|V|^2}{2X_dX_q} \left[X_d + X_q - (X_d - X_q)\text{Cos}2\delta \right] \ldots (2.13)$$

If the prime mover input to the unexcited machine exceeds the maximum electrical power given by equation (2.12) (plus the rotational losses) the alternator will be driven above synchronous speed. The equation for the real power under this condition is expressed by

$$P = \frac{X_d - X_q}{2X_d X_q} |V|^2 \text{ Sin } 2 \left[2\pi (f_1 - f)t + \delta_0 \right] \quad (2.14)$$

where f is the system frequency, f_1 is the frequency corresponding to the speed of the unexcited alternator, and δ_0 is the value of δ at the instant when the field excitation becomes zero.

2.6 CONCLUSIONS

1. When an alternator is synchronised when its voltage is quite out of phase with the bus voltage, a large interchange of real power may occur.

2. The incoming machine may draw reactive power when connected out of phase to a bus supplied by two or more alternators, whereas the maximum reactive power it can deliver to the system is relatively small. Severe reduction in bus voltage results depending upon the number of alternators on the system when the angle between the bus voltage and that of the incoming alternator approaches 180°.

3. An armature current equal to twice the available 3 phase short circuit current results from synchronising an alternator to an infinite bus. The operator may synchronise the machine atrandom and the phase displacement between voltages may have any value from 0° to 180°. Automatic synchronising is necessary so that voltage dips and power swings afe negligible.

4. When an alternator loses its field of excitation while operating in parallel, it draws a large amount of reactive power from the system and causes the system voltage to ab normal and even to oscillate.

So the alternator with the open field circuit should be immediately disconnected from the system.

TRANSIENT ELECTRICAL TORQUES OF TURBINE

2.7 Generators During Synchronising

The calculation of shaft and frame stresses in turbine generators during synchronising is dependent upon the knowledge of electrical torque developed at the rotor air gap. This torque generally contains unidirectional, fundamental frequency and second harmonic components, all of which are damped. Steady components of torque are of interest in the calculation of system stability.

For the calculation of torque, a synchronous machine should have the following assumptions :-

(a) Air gap is uniform i.e. the presence of slots on the quadrature axis of the machine and none on the direct axis does not invalidate this assumption.

(b) Saturation and hysteresis are neglected in calculating the alternating components of torque.

(c) The field has distributed symmetrical windings on both axes. (In the actual machine, there is no winding on the quadrature axis.

(d) The stator has a sinusoidally distributed three phase winding.

(e) The air gap flux is sinusoidally distributed in space.

Now if a machine is synchronised out of phase with a low reactance system, the resulting torques may attain values even greater than those encountered during a short circuit. If the synchronising takes place with all the three circuit breakers closing at the same instant there will exist unidirectional synchronising and loss torques and in addition a fundamental frequency torque resulting from the trapped armature flux. However, if only two of the poles close (the other pole not closing at all) there will be, in addition to the above torques a double frequency torque developed by the negative sequence armature current.

1. For faulty synchronising, the loss torque is generally much less than the synchronising torques and may be neglected.

2. If synchronising takes place with the machine either leading or lagging the system, the armature current will have a direct axis component which will tend to demagnetize the main poles causing the direct axis rotor flux to decay. This gives rise to the problem of calculating the current in a circuit having one voltage

fixed (source) and one voltage varying with time. But in many mechanical systems, the maximum stresses are reached in the first or second cycle, so we can simplify the problem by neglecting rotor decrements.

3. It is assumed that the angle between the system and the machine remains sufficiently unchanged during the first two or three cycles to permit the calculation of the synchronising currents without having to take into account the oscillations of the machine with respect to the system. (If it is desired to calculate the torque beyond two or three cycles, the decrements of rotor flux will be considered).

In Fig. 2.6 there are shown the electrical torques for a line to line short circuit and two conditions of synchronising. Though the three phase synchronising torques does not reach as high a peak as the line to line short circuit torque, its components are only unidirectional and fundamental frequency ones. These components will produce much more serious shaft stresses than the second harmonic torque.

From Fig. 2.7 it is evident that synchronising considerably out of phase is dangerous. All conditions being equal, electrical torque for single-phase synchronising (only two poles closing) is not as severe as for three phase synchronising.

Equations for the single-phase synchronising and for three phase synchronising are given in App. 2.

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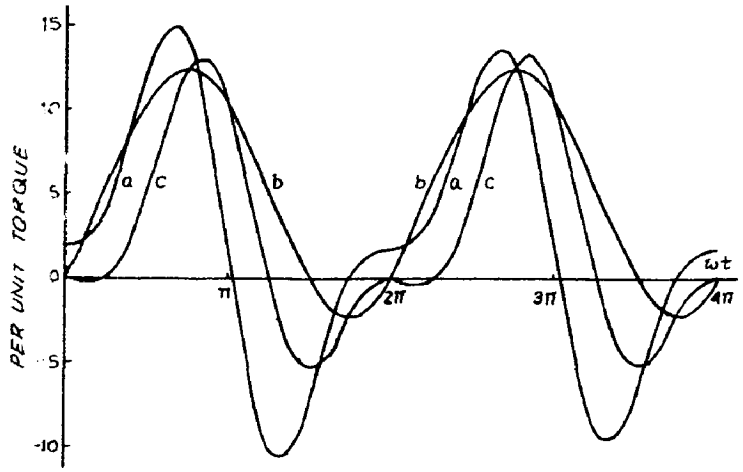


FIG 2 6. SHORT-CIRCUIT AND SYNCHRONISING TORQUES

(a). LINE TO LINE SHORT CIRCUIT, $\alpha = 0°$

(b). THREE-PHASE SYNCHRONISING, $\delta = 90°$, $X_s = X_d''$

(c). SINGLE-PHASE SYNCHRONISING, $\delta = 90°$, $\alpha = 135°$, $\beta = 45°$, $X_s = X_d''$

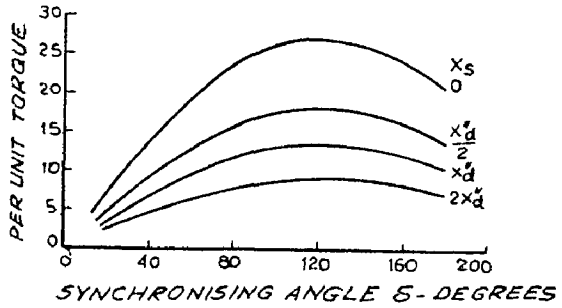


FIG 2 7. CREST ELECTRICAL TORQUE DURING THREE PHASE SYNCHRONISING AS A FUNCTION OF SYNCHRONISING ANGLE AND SYSTEM REACTANCE

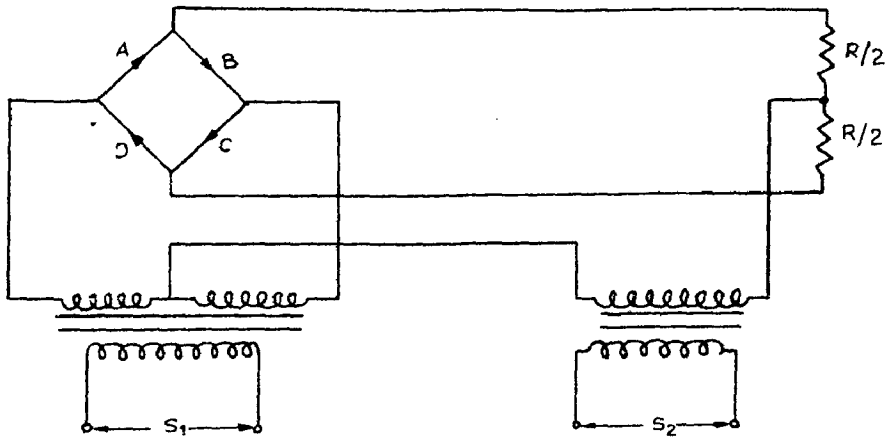
CHAPTER - III

MEASUREMENT OF FREQUENCY AND PHASE BETWEEN TWO SIGNALS BASED ON PHASE COMPARISON METHODS

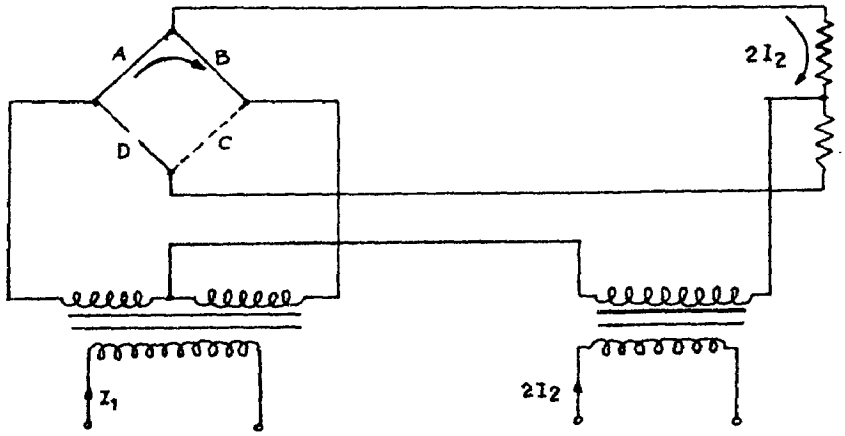
3.1 DERIVATION OF SLIP FREQUENCY SIGNALS

Two a.c. signals having different frequencies are fed to a bridge ring modulator for deriving a difference frequency signal as shown in circuit 3.1a. Two of the four diodes are maintained in the conduction at anyone time by one input signal and these provide a transmission path into the bridge load resistor for the second signal. For this two conditions are shown. In Fig. 3.1b the input signal $I_1 > I_2$ flows through diodes A and B and the second current input $2I_2$, after dividing at the centre tap of the input transformer, adds to the current flowing through diode A and subtracts from diode B but I_1 must be able to sustain the conduction of diode B then the two parts of the input signal recombine to flow through the upper half of the bridge resistance load. The same relative signal polarities are maintained in fig. 3.1c but now $I_2 > I_1$. The signal current I_1, after flowing through diode A is unable to return through the now reverse biased diode B and flows instead through both sections of the bridge load and through diode C.

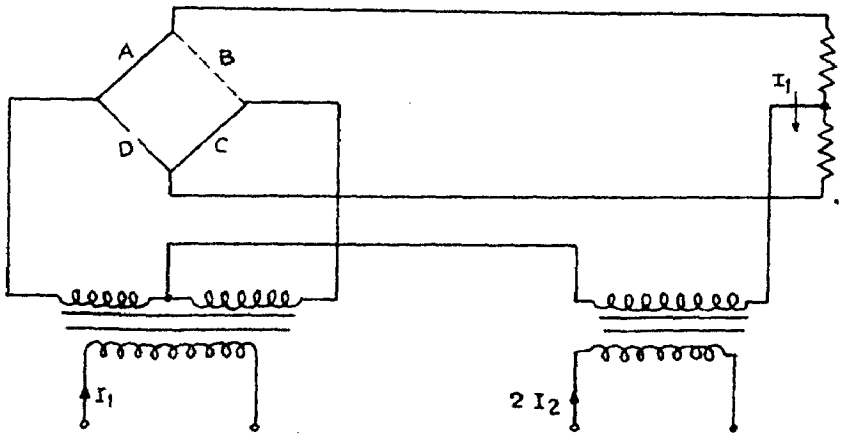
Similar signal transmission paths may be made for other combinations of the polarity and the relative amplitude of the input signals, giving eight different static conditions as follows :-



(a)



(b) WHEN $I_1 > I_2$



(C) WHEN $I_2 > I_1$

FIG 3.1 DERIVATION OF SLIP FREQUENCY SIGNALS

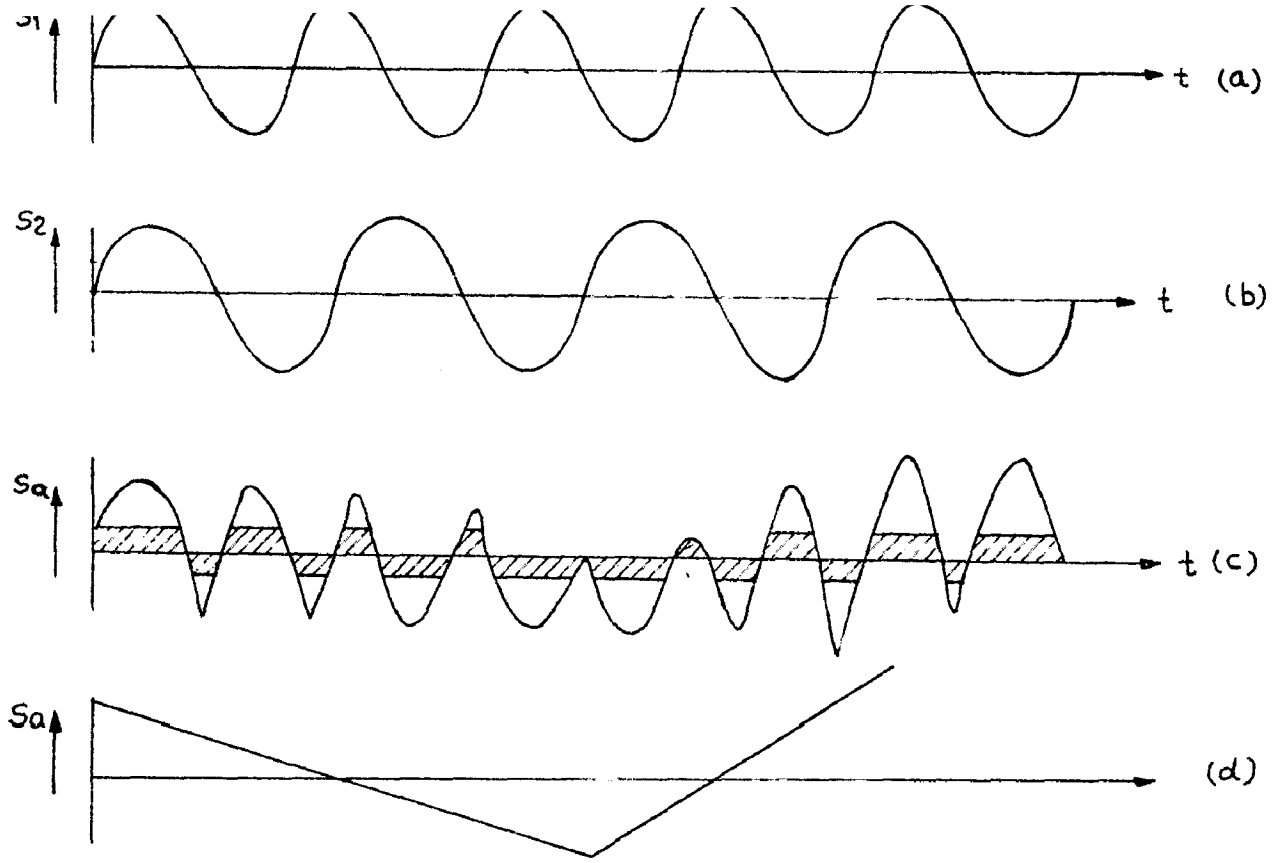


FIG. 3.2 - WAVE FORMS IN DIODE MODULATOR

(a) - 50 C/S INPUT

(b) - 40 C/S INPUT

(c) - BRIDGE OUTPUT

(d) - BRIDGE OUTPUT AFTER FILTERING

3.1.1 SUMMARY OF STATIC CONDITIONS IN DIODE MODULATOR

No.	I_1		I_2		Diodes conducting.	Output	Diode limiting current
	Relative amplitude	Polarity	Relative amplitude	Polarity			
1	Larger	+	Smaller	+	A&B	I_2R	C
2	Smaller	+	Larger	+	A&C	I_1R	B
3	Larger	+	Smaller	-	A&B	$-I_2R$	D
4	Smaller	+	Larger	-	B&D	$-I_1R$	A
5	Smaller	-	Larger	-	B&D	I_1R	C
6	Larger	-	Smaller	-	C&D	I_2R	B
7	Larger	-	Smaller	+	C&D	$-I_2R$	A
8	Smaller	-	Larger	+	A&C	$-I_1R$	D

The table shows that the greater current inputs control the transmission path to the bridge output, but it is the smaller input that appears there.

Applying these conditions to the signals having frequencies of 50 c/s and 40 c/s respectively, it will give the output as shown in fig. 3.2c. Both upper and lower side-bands of the modulation process are present and the unwanted component is to be removed

by using a low pass-filter to get the wanted frequency signal. The output waveform is shown in fig.3.2.c while the frequency of the output after filtering is shown in fig. 3.2d.

3.2 LOGIC TEST OF SLIP FREQUENCY

To test whether the slip frequency is equal to or less than a predetermined value, two slip frequency waveforms are derived with a controlled and constant phase shift between them, a width modulator wave form is generated from them by initiating an "and" comparison which detects the time for which coincident positive going signals are present. It is shown in fig. 3.3 that if the phase displacement α between slip frequency signals is independent of the slip, width τ of the wave form after comparison is a measure of the slip frequency given by

$$\tau = \frac{\alpha}{360\, f_s} \quad \ldots \quad \ldots \quad (3.1)$$

If δf is the small slip frequency for which synchronism is permitted, the width τ_c of the waveform corresponding to the frequency derivation taking the limiting value for synchronisation is given by

$$\tau_c = \frac{\alpha}{360 \cdot \delta f} \quad \ldots \quad \ldots \quad (3.2)$$

A pulse indicating that the condition

$$(f_1 - f_2) \leqslant \delta f \quad \ldots \quad (3.3)$$

is satisfied, may be produced by comparing the width varying waveform with a waveform having a fixed duration τ_c . The logic diagram is shown in fig. 3.4. The leading edges of the width varying waveform and the interrogation waveform are cynchronised, and the latter is generated once each slip frequency cycle. A confirmatory pulse is derived from their "and" comparison and stored for a time long enough to allow for the measurement of phase displacement. If circuit breaker reclosure does not take place even though the slip test is within limits, the store is reset each cycle until the closure is initiated.

3.3 PHASE CONTROL OF SLIP FREQUENCY SIGNAL

A phase α between slip frequency signals is introduced deliberately and it is independent of slip frequency. The required phase shift is inserted into one of the signals Say S_1 before modulation in the ring bridge modulator.

If for modulator A in fig. 4, the input signals are

$$S_1(A) = A_1 \sin (w_1 t + \phi_1) \quad \ldots \quad .. \quad (3.4)$$

$$S_2(A) = A_2 \sin (w_2 t + \phi_2) \quad \ldots \quad .. \quad (3.5)$$

and for modulator B

$$S_1(B) = B_1 \sin (w_1 t - \alpha + \phi_1) \quad \ldots \quad .. \quad (3.6)$$

$$S_2(B) = B_2 \sin (w_2 t + \phi_2) \quad \ldots \quad .. \quad (3.7)$$

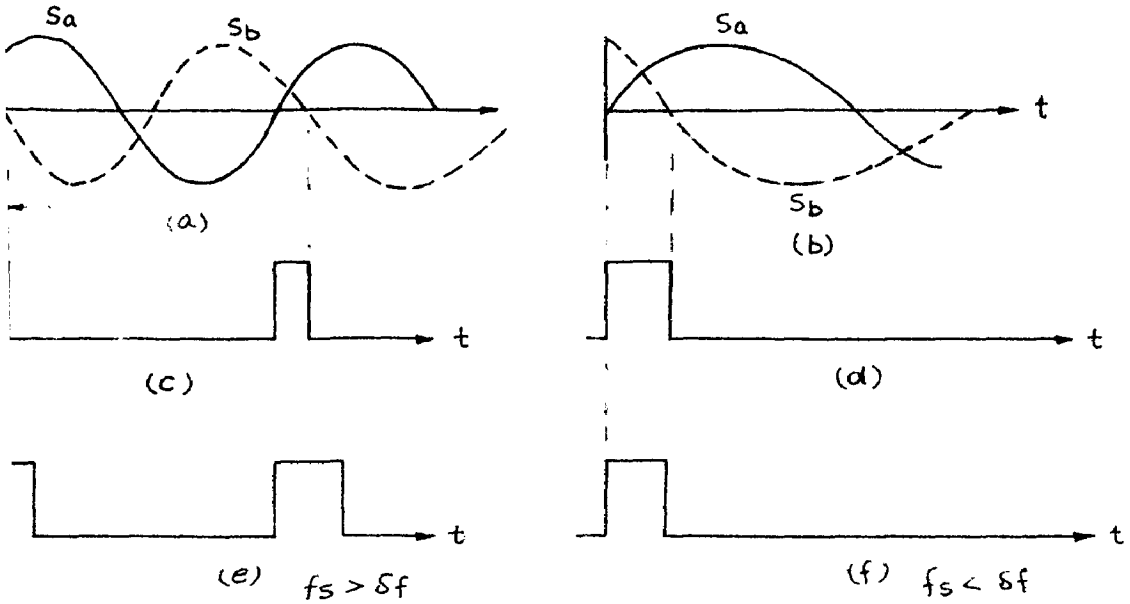
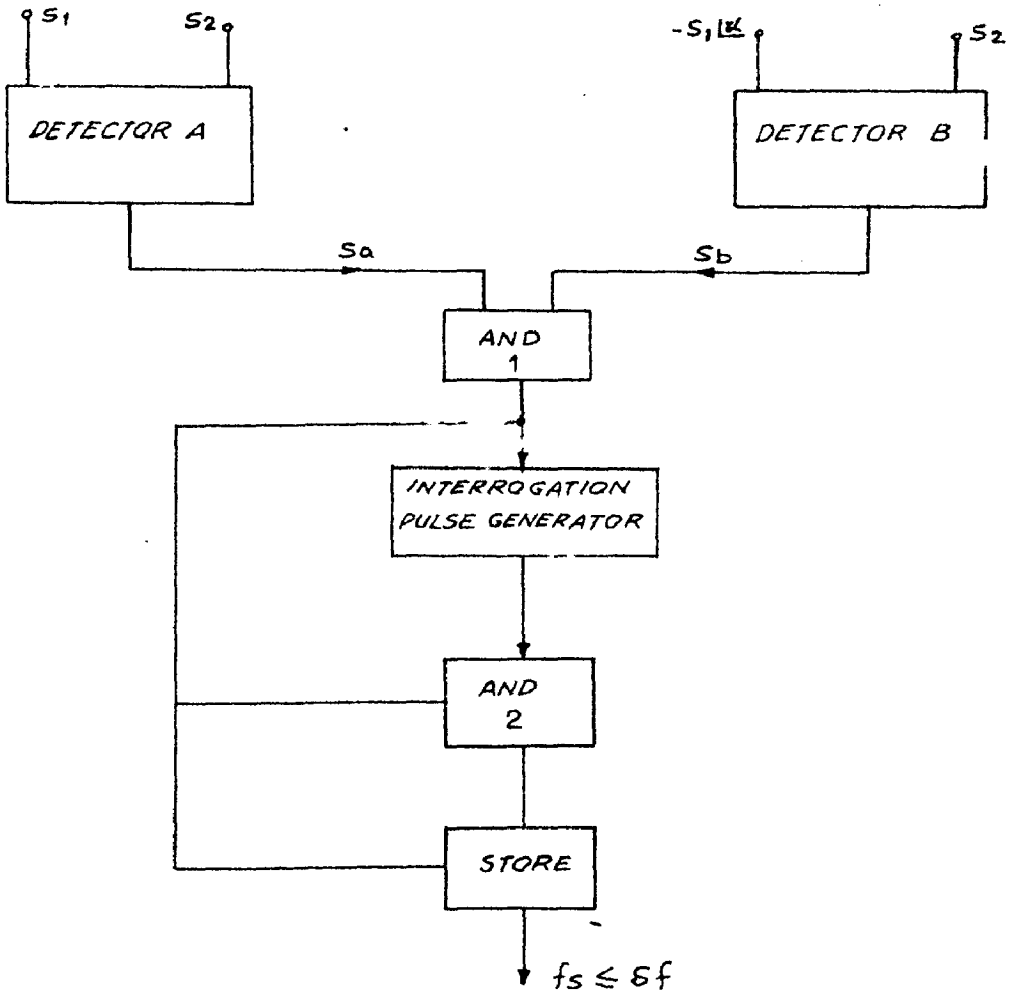


FIG. 3 3. WAVE FORMS IN SLIP FREQUENCY CHECK

), (b). SLIP FREQUENCY SIGNALS Sa AND Sb
', (d). OUTPUT OF 'AND' GATE
', (f). INTERROGATION PULSE



4. LOGIC DIAGRAM OF SLIP FREQUENCY MEASUREMENT

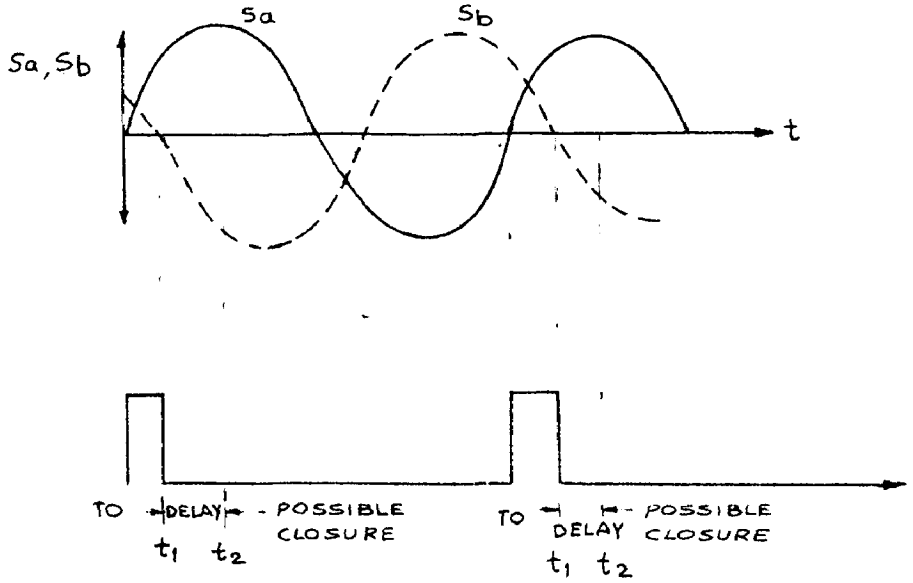
The outputs of modulators A and B are

$$S_a = A_3 \cos \left[(w_1 - w_2)t + \phi_1 - \phi_2 \right] \quad \ldots \quad (3.8)$$

$$S_b = B_3 \cos \left[(w_1 - w_2)t + \phi_1 - \phi_2 - \alpha \right] \quad (3.9)$$

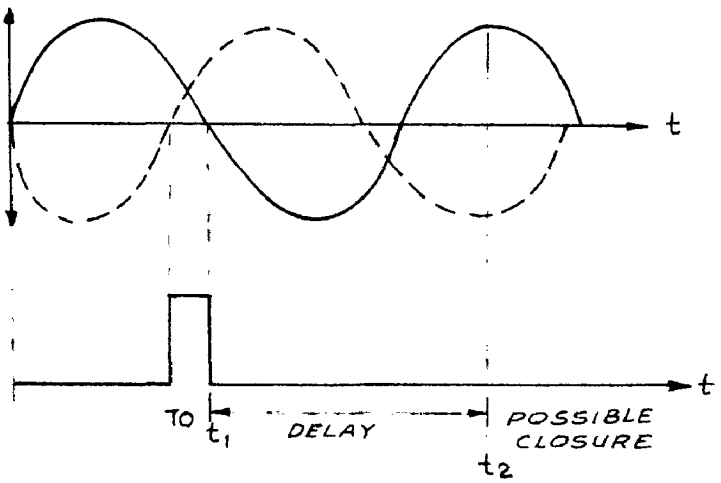
Thus if w_2 w_1, S_b leads S_a by phase α and
if w_1 w_2, S_b lags S_a by phase α

the "and" comparison of S_a and S_b yields a rectangular wave form the width of which is inversely proportional to slip frequency, irrespective of whether the incoming machine is running slow or fast in relation to the system speed. The slip is assessed by measuring the time taken for the phase displacement to change by a given amount α (slip in each slip frequency cycle). The angular range of measurement should be small so as to minimise the errors caused by changes in phase displacement during the sample period. Angular range corresponds to the phase shift α introduced into one of the signals. A value of 20° is sufficient, and this is shown in fig.35 which shows the conditions when approaching synchronism at speeds greater and less than the nominal speed.
In case of $w_1 > w_2$ and $w_1 - w_2 < 2\pi\delta f$, a confirmatory pulse from the slip test circuit is generated at time t_1 in fig.35a and closure should take place at t_2 if the amplitude condition is met $t_2 - t_1$ should be small to reduce the effect of speed changes during the period. Delay may not be acceptable for the condition $w_2 > w_1$



WHEN $\omega_1 = \omega_2$

FIG. 3.5(a)



WHEN $\omega_2 > \omega_1$

FIG. 3.5(b)

as shown below in fig. 3.5b because whereas speed confirmation is given just before the instant of zero phase displacement when w_1 w_2, it is given just after when w_2 w_1. The figures are for delays in effecting closure on completion of slip frequency measurement. (Diode modulator gives maximum output when phase displacement between the input signals is zero).

Now it becomes necessary to determine, once in each slip cycle the instant of zero angular displacement between the incoming machine and the supply system and to generate a circuit breaker closure pulse in advance of zero displacement condition being reached. This is known as "fixed angle compensation". This compensation to allow for the delay in the circuit breaker can be expressed in terms of an angular displacement so that the pulse should be generated when the displacement is and the symmetry should be maintained about the in phase condition for the incoming machine running either fast or slow with respect to the system.

is related to slip frequency in such a way that at the maximum permissible frequency, closure is effected at the correct instant. The waveforms in 3.6b narrate the method of compensation and the way in which error may arise from it.

The peak in the slip frequency signal output from ring modulator takes place when the two inputs

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are in phase. This condition is attained by "and" logic circuit as in figure 3.6b. In the diagram, slip frequency selected for complete compensation is the maximum permissible frequency for synchronisation but the principle of compensation can be applied whatever the frequency is selected. As at this frequency, the advance time is designed to be equal to the circuit breaker operating time.

Errors will take place as in figure 3.6b at slip frequencies different from that selected for compensation. Particular combination of variables gives the variation of timing errors with slip frequency as in figure 3.7a.

The circuit breaker operating time is 0.3S and correct compensation has been arranged at maximum permissible slip frequency of 0.5 c/s. Time compensation period is given by

$$\tau_s = \frac{90^\circ - \alpha_s}{360\,\delta f}$$

whereas the phase shift α_s in the control signals is obtained from the limiting value $\tau_s = 0.3S$ when $\delta f = 0.5$ c/s.

Corresponding errors in phase displacement are shown in figure 3.7b as a function of slip frequency when f_s takes the limiting value of 0.5 c/s, phase displacement at closure is zero, while at smaller frequencies, the phase errors can be high.

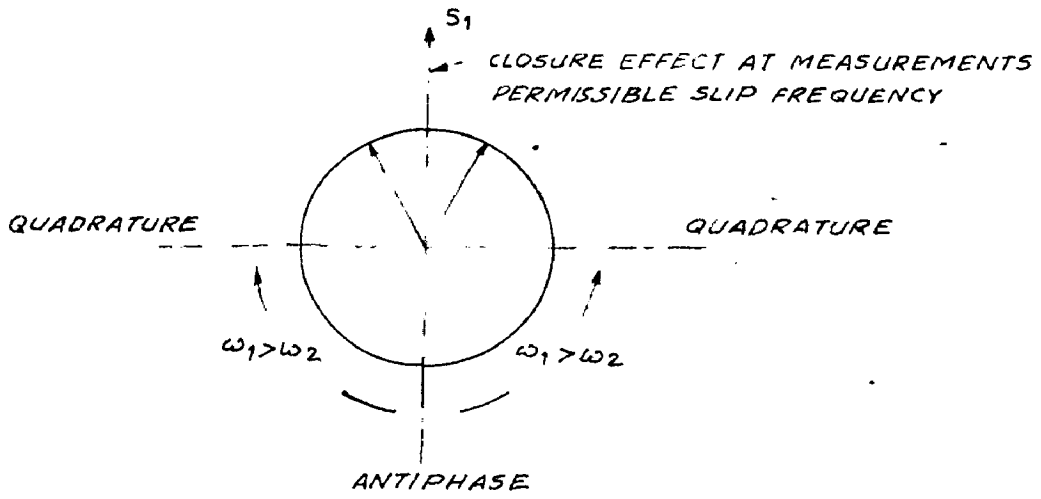
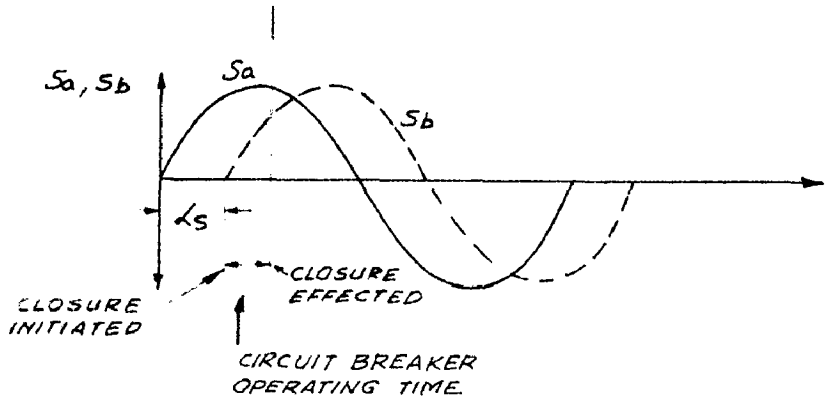
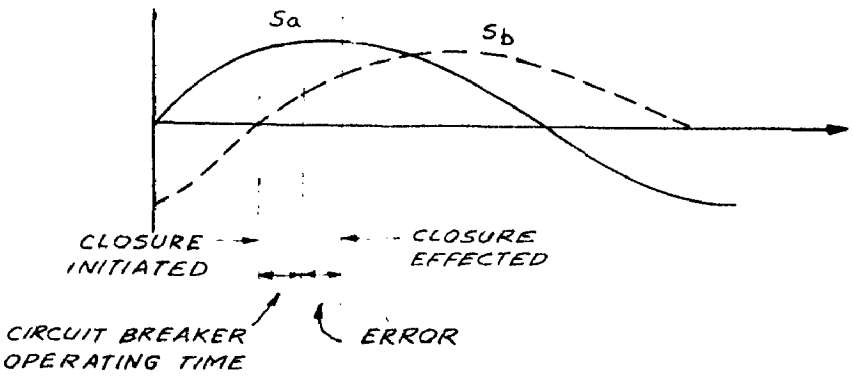


FIG. 3.6(a)-MEASUREMENT OF PHASE DISPLACEMENT

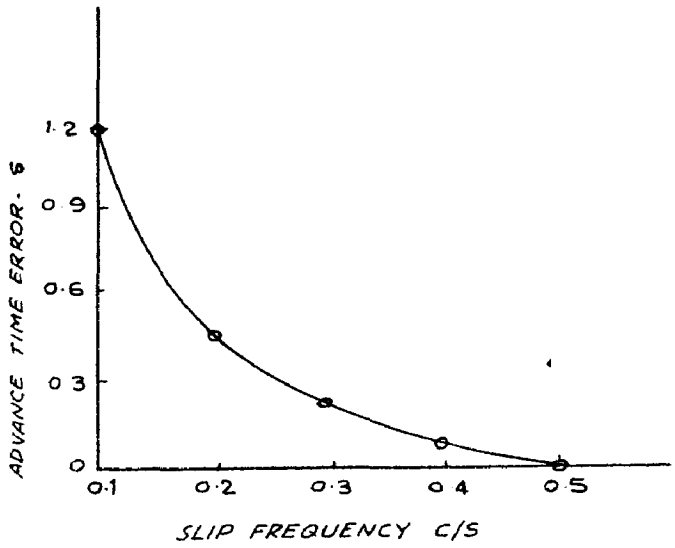


$\omega_1 - \omega_2 = 2\pi\delta$

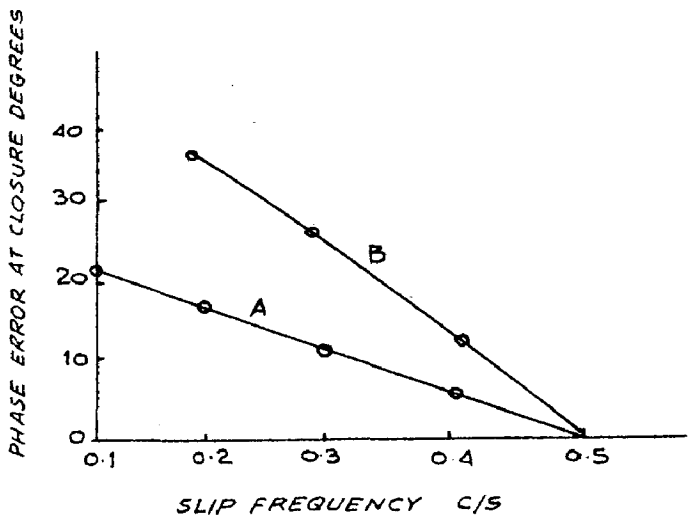


$\omega_2 - \omega_1 < 2\pi\delta f$

3(b) WAVE FORMS IN PHASE MEASUREMENT



(a)



(b)

FIG. 3·7. ADVANCE TIME CIRCUIT ERRORS

(a). VARIATION IN ADVANCE TIME WITH SLIP FREQUENCY CB OPERATING TIME 0 3S

(b) - VARIATION OF PHASE ERRORS WITH SLIP FREQUENCY CB OPERATING (A) = 0 15 S (B) = 0.3 S

For example, in the case of a circuit breaker operating time of 0.15 sec. and maximum frequency duration of 0.5", the angular deviation for a 50 c/s supply can take the limiting value of 13.5° when synchronisation is effected close to zero slip conditions.

****

CHAPTER - IV

DESIGN OF THE CHECK SYNCHRONISING RELAY

Amplitude comparison underlays the derivation of slip and phase displacement checking signals using modern static relaying techniques of transistors. The unit consists of four parts each with a different function.

(1) Slip frequency measuring arrangement

(2) Phase indicator

(3) Voltage Comparator with the control of permissible voltage variations

(4) Sequential Control Circuits

Part 1 is a combination of an electromagnetic circuit of transformers and resistors and rectifier bridges for signal rectification with a filtering circuit.

Part 2, 3 and 4 are all transistorised circuits. Part 3 is achieved as an auxiliary function of one of the sequential control units.

4.1 SLIP MEASURING CIRCUIT

This is an electromagnetic slip frequency measuring device and gives a sinusoidal output wave, the frequency of which is the difference between the frequencies of the two applied voltages.

The running and incoming voltages are connected to the primary windings of the two transformers A and B. (A is designed as a ratio of primary to secondary voltage of 10:2 and B of 10:1).

Their secondary windings are so connected as to add and subtract the two voltages. Outputs are taken across the two rectifier bridges. Secondary windings of transformer A is centre tapped and the centre point is connected to one side of the secondary winding of transformer B.

The voltage applied across each half of the secondary winding of transformer A is equal to that across the secondary winding of transformer B. When the two input voltages on the primary sides are equal then considering two voltage waveforms :-

Running supply voltage $V_R = V_1 \text{ Sin } w_1 t$

Incoming " " $V_G = V_2 \text{ Sin } w_2 t$

Assuming $V_1 = V_2 = V$. This condition is to be satisfied for permissible limits otherwise no synchronising signal would be issued.

$$V' = V_R + V_G = V_1 \text{ Sin } w_1 t + v_2 \text{ Sin } w_2 t$$

$$= V(\text{Sin } w_1 t + \text{Sin } w_2 t)$$

$$= 2V \sin \frac{w_1 + w_2}{2} t \cos \frac{w_1 - w_2}{2} t \quad .. \quad (4.1)$$

and $V'' = V_R - V_G = V(\sin w_1 t - \sin w_2 t)$

$$= 2V \cos \frac{w_1 + w_2}{2} t \sin \frac{w_1 - w_2}{2} t \quad .. \quad (4.2)$$

Equations 4.1 and 4.2 give forms of shape shown in fig. b. The period of oscillation is proportional to $w_1 - w_2$, the slip frequency.

SUBTRACTION OF VOLTAGES

$$V'' = V_R - V_G = \sqrt{V_1^2 + V_2^2 - 2V_1V_2 \cos \alpha}$$

when $V_1 = V_2 = V$

$$\therefore V_R - V_G = V'' = 2V \sin \alpha/2 \quad \ldots \quad \ldots \quad (4.3)$$

This shows that the resultant voltage V" is proportional to the sine of the phase displacement.
Equation 4.3 shows that when the two signals are in phase and of the same voltage magnitude, the resultant voltage is zero.
When they are out of phase by 180°, the resultant voltage is maximum i.e. $V'' = 2V \sin 180^\circ/2 = 2V$.
Hence subtraction of voltages gives rise to a sine waveform.

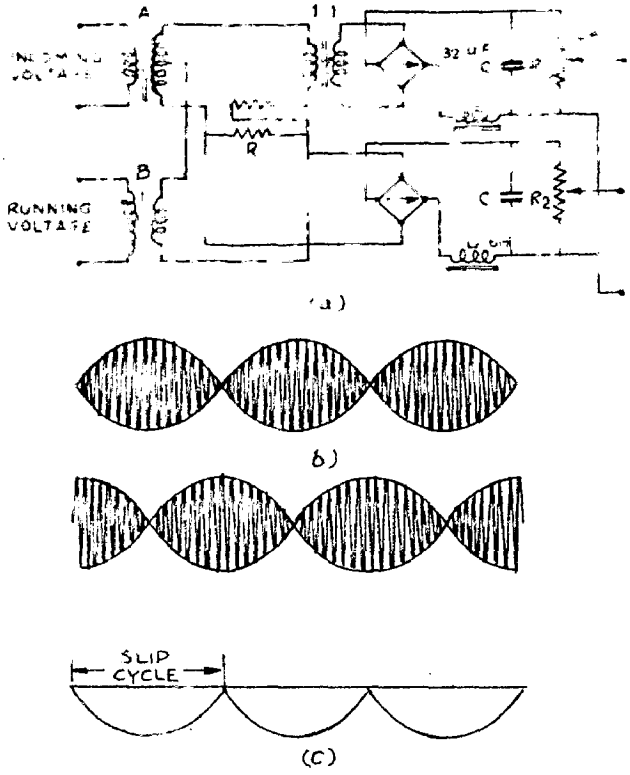


FIG. 41. CIRCUIT ARRANGEMENTS AND WAVEFORMS OF SLIP-FREQUENCY MEASURING DEVICE

GENERAL ARRANGEMENT

WAVEFORMS OF SIGNALS ACROSS R AND THE 1:1 TRANSFORMER FOR THE CASE OF $V_1 = V_2$

RECTIFIED OUTPUT WAVESHAPE AVAILABLE AT R_1 AND R_2

SUMMATION AND SUBTRACTION OF VOLTAGES

ADDITION OF VOLTAGES

$$V' = V_R + V_C = \sqrt{V_1^2 + V_2^2 + 2V_1V_2 \cos\alpha}$$

when $V_1 = V_2 = V$

$$V' = 2V \cos\alpha/2 \quad \ldots \quad (4.4)$$

when phase difference is 0°

$$V' = 2V \quad \text{maximum}$$

when phase difference is 180°

$$V' = 0$$

This gives a cosine wave of the slip frequency, having its zero potential at 180° electrical degrees displacement and its maximum at phase coincidence. These are shown in fig. 4.1b.

The two wave forms given by equations 4.1 and 4.2 are rectified to give negative half cycle output. This wave is smoothed and freed from ripples in an L-C filter circuit (Low freqeuncy pass circuit) using L=6 henries and C = 32 μ Farads.

The outputs appearing across the two potentiometers R_1 and R_2 (using two carbon variable resistors each of 2 K. ohms) are shown in fig. 4.1c. These two waveforms are fed to the pulse circuits.

A bridge connection is employed to avoid feed back between the two voltages. The 1:1 isolating transformer in one arm of the bridge is used to make it possible for the rectified output signals to have a common point.

4.2 PRINCIPLE OF OPERATION OF THE CIRCUIT (BLOCK DIAGRAM)

Slip signal having its zero at the point of phase coincidence from the slip measuring circuit is given to pulse circuit 1. The pulse circuit is such that when the input signal from the slip measuring circuit becomes zero, a conduction which lasts for a very short of time then a negative pulse is produced as shown in fig. 4.3a and 4.3b. Signal from pulse circuit 1 is fed to a monostable timing circuit. This is designed to give a negative output square wave of duration equal to the time of operation T_c of the circuit making switch. The pulse duration is variable by the R-C components (RC = Time constant = 0 to 1 second) to suit different types of circuit breakers. The output is as shown in fig. 4.3c.

4.3 PHASE INDICATION

As shown in fig. 4.2, two signals are taken from monostable timing circuit, one is fed into phase comparator 1 and other into delay circuit. Delay circuit gives a constant delay time, depending upon

the decay of the monostable pulse as in Fig. 4.3(d). Output from the delay is fed to two phase comparators. From fig. 4.2, it is evident that the output of phase comparator 1 is controlled by five signals i.e. running and incoming voltages, monostable pulse output, delay output and Bistable 3. If anyone of these five signals is negative, it gives zero output. Output signals of monostable timing and delay circuit are so arranged that they permit phase comparator only during the limited period τ = (Delay time - T_c) as shown in fig. 4.3e. This means that the voltages of running and incoming supplies can only be compared in phase, in phase comparator 1 during this restricted period. When the two voltages are in phase during the time τ , a negative going signal is produced which is fed to a level detector through an integrating circuit within the phase comparator. The function of the integrator and level detector is to guarantee that only if two source signals are in phase during the period then an output signal will be produced to operate bistable circuit 1 as in fig. 4.2.

Now phase coincidence of the two voltage signals to be synchronised takes place on numerous occasions, but phase coincidence should take place only when the slip frequency is very small. This can be

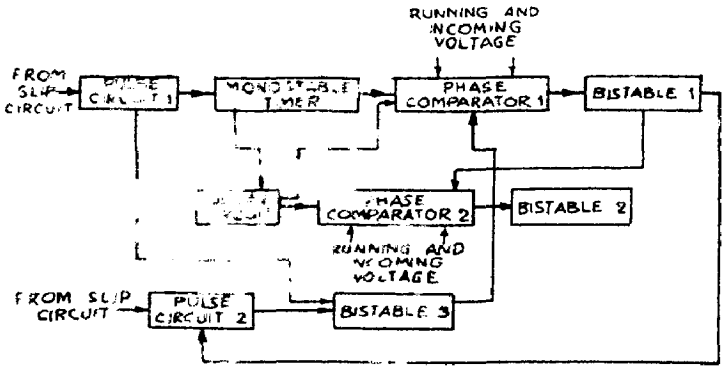
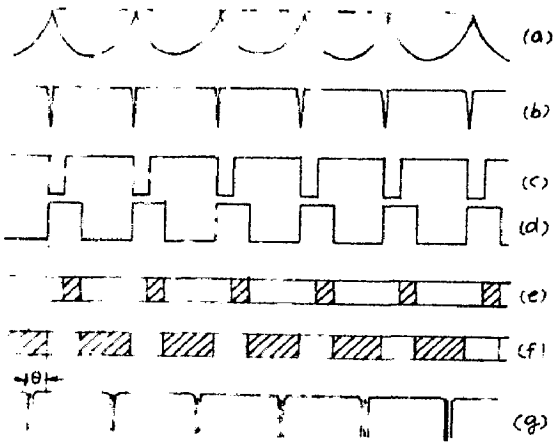


FIG 4.2. BLOCK SCHEMATIC OF STATIC SYNCHRONISING RELAY



SEQUENTIAL OPERATION OF STATIC SYNCHRONISING RELAY

T FROM SLIP MEASURING CIRCUIT
T FROM PULSE CIRCUIT 1
JT FROM MONOSTABLE TIMING CIRCUIT
JT FROM DELAY CIRCUIT
ATING PERIOD OF PHASE COMPARATOR 1
ING PERIOD OF PHASE COMPARATOR 2 IF BISTABLE CIRCUIT 2 PICKS UP
TRIPPING SIGNAL AT SPECIFIED ANGLE

achieved by limiting the phase comparator operating time and also the operation of level detector should take place only when the two signals are in phase during this restricted period. When the signal from phase comparator 1 switches on Bistable 1, this circuit together with the delay circuit, will in turn switch on phase comparator 2, which will again measure the phase angle between two source voltages, when the phase difference attains angle θ, corresponding to the time delay T_c of the monostable timing circuit, a signal is produced to trigger bistable circuit 3 which controls the circuit breaking operating mechanism at the correct instant.

As it makes the system operate only when the slip frequency is too low. To overcome this, pulse circuit 2 and bistable circuit 3 have been added as in Fig. 4.2.

Bistable 3 is set by pulse circuit 2 and reset by pulse circuit 1. If slip frequency is near synchronism and phase comparator 1 picks up at the angle θ in the first half cycle, correct operation results with pulse circuit 2 and bistable circuit 3 both maintained in operative by a signal from bistable circuit 1.

On the other hand if operation is not obtained in the first half of the slip cycle, the system will be maintained in operative during the second half cycle by a signal from bistable circuit 3. At the end of the cycle, the system is reset by pulse circuit 1 to start the sequence of operation all over again.

4.4 TRANSISTOR CIRCUITS

4.4.1 PULSE TRIGGER CIRCUIT

This is a common emitter circuit, having only one transistor, the input is a slip voltage signal. It will conduct when the input signal of base is negative with respect to the emitter voltage. Output at the collector will have the same potential as the emitter, if the signal at the base is equal to positive with respect to the emitter, the transistor will not conduct and voltage at the collector will fall. Hence for a short instant when the slip voltage to the pulse circuit is zero, a sharp negative pulse is obtained at the collector output terminal. When the two applied voltages are not equal in magnitude, the slip voltage will not attain zero and no output pulse will be obtained. This means that no operation takes place unless the two applied voltages are of the same magnitude.

4.4.2 MONOSTABLE TIMING CIRCUIT

Monostable multivibrator circuit, when triggered by a small pulse, generates a large pulse.

the width of which can be controlled by either changing the potential at the base with the variable resistance V_s or by an RC circuit connected between the collector of transistor T_1 and base of transistor T_2. R is a variable resistance. A triggering circuit is needed to bring out transition from its stable to semistable. The time of quasistable state is very large compared with the time of transition between the two stages.

This is a common emitter type as shown in fig.4.5 . In the stable state, transistor T_2 is conducting as its base takes current from the negative supply, transistor T_2 is biased to cut off by a resistance R_e in the common emitter. When the signal at the base of T_1 causes the transition from the stable to the quasistable state, T_2 cuts off, T_1 starts conducting and an emitter current I_1 flows in T_1. This current is dependent on setting of V_s.

After the trigger pulse has been applied the collector voltage of T_2 falls and with this base voltage of T_2 all starts to fall exponentially towards V_{cc}, are the other voltages remain constant until the base voltage of T_2 falls to pick up voltage. At this the quasistable state terminates and the voltage finally stabilizes to the level $I_2 R_e$. The circuit produces a positive pulse at the collector of T_1 and a negative pulse at the collector of T_2, each with a duration depending upon the time constant and of RC coupling

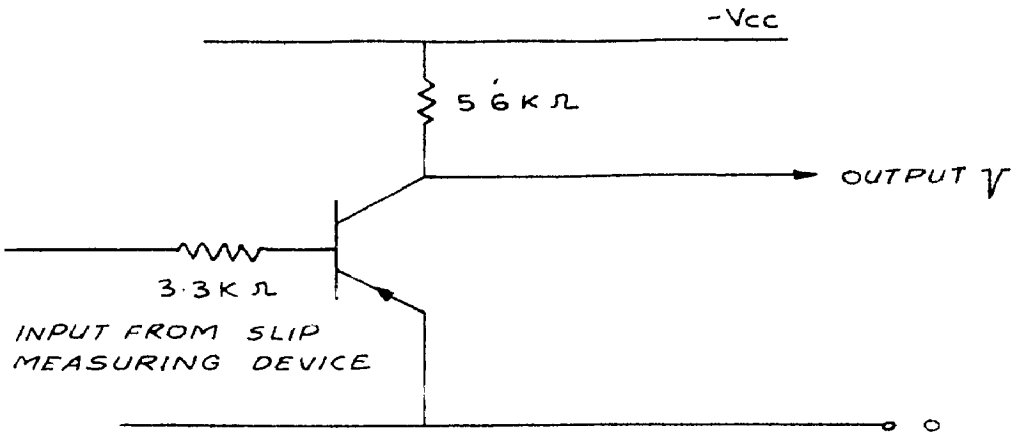


FIG. 4 4(a)

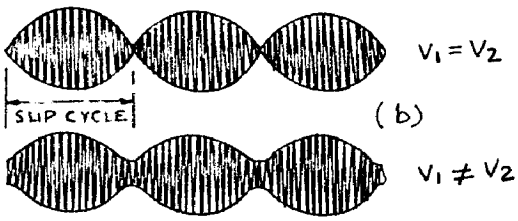


FIG. 4·4 (b) - SLIP WAVEFORMS PRIOR TO RECTIFICATION

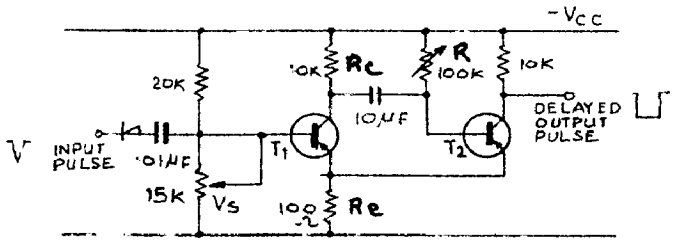


FIG. 4 5 - MONOSTABLE TIMING CIRCUIT

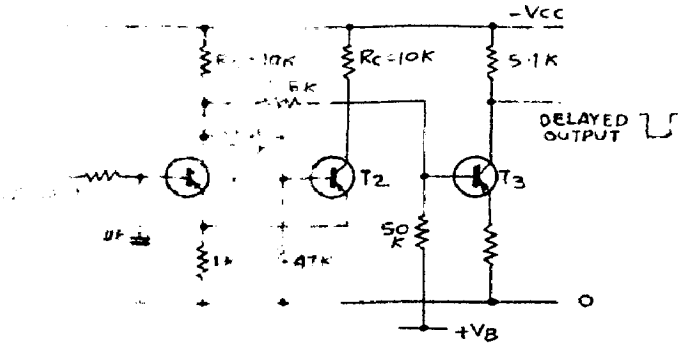
4.4.3 DELAY CIRCUIT

The circuit in figure 4.6 consists of a level detector shunted at its input by a capacitor C_d, when the starting signal is applied to its input, a delayed step function going from zero voltage to $-V_{cc}$ is produced at the collector of T_3 and a pulse with the same delay is produced at the collector of T_2.

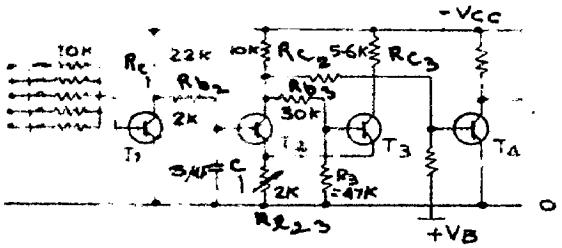
4.4.4 PHASE COMPARATOR DESIGN

Phase comparator is the main relaying element in the synchronising relay. It consists of a coincidence stage (phase comparing element) controlled by pulse circuits from monostable timing circuit, from delay circuit, from bistable circuit 3 and from two source voltages to be compared in phase. It is followed by an integrating and level detector output stages.

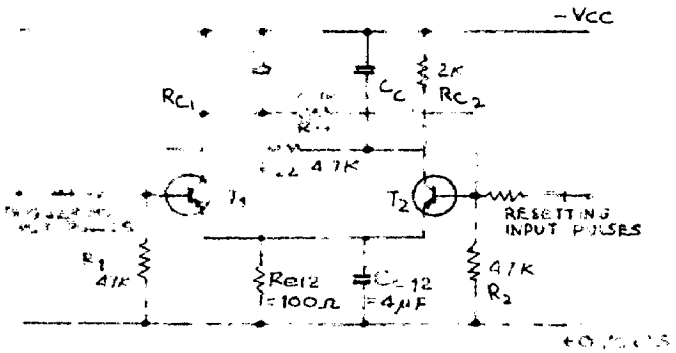
Coincidence circuit will allow operation only if all its inputs are zero or positive at the same time. If any of these signals is negative, no operation takes place as the collector voltage of the circuit will be at zero voltage i.e. the transistor will be conducting. The integrating circuit is an arrangement of a capacitor C_1 charging through a resistor R_{c1} and R_{b2}, when the coincidence transistor is cut off. In fact the function of the integrator and level detector circuits is to ensure that only if two source signals are in phase during the whole of operating time of the phase



4 TIME DELAY CIRCUIT



17 MULTIPLE INPUT PHASE COMPARATOR



5 ASYMMETRICAL BISTABLE TRIGGER CIRCUIT

comparator than only an output will be obtained to operate bistable circuit 1 as shown already. In the figure 4.7 emitters of transistors T_2 and T_3 are connected through the common resistor R_{e23}. As long as the voltage V_c is lower than certain value V_p (pick up voltage) transistor T_3 is fully conducting due to negative voltage applied to its base, while transistor T_2 is biased to cut off by the voltage drop across the common resistor R_{e23}. T_3 will conduct till $R_{e23} I_3 = V_c$.

The input voltage to the coincidence circuit is obtained from the five signals being fed to it such that the operating current makes the base of T_1 positive with respect to the emitter when base of T_1 is zero or positive, transistor T_1 stops conduction and the voltage V_{cc} starts to charge the condenser C and V_c starts to rise exponentially depending upon the time constant, $C(R_{b2} + R_{c1})$ of charging circuit.

As soon as the voltage reaches the pickup value, T_2 starts to conduct and its collector voltage starts to rise. This rise of voltage is transferred to the base of T_3 and reduces its emitter and collector currents. This reduction in emitter current of T_3 pushes T_2 to further conduction with rise in its collector current which is again transferred to the base of T_3 and the cycle is repeated. If during this action gain is greater than unity the circuit will

suddenly change to other state of stability where T_2 is fully conducting T_3 is cut off when T_3 is cut off, a negative voltage appears across the collector and emitter of transistor T_3 which is applied to bistable circuits.

For the design, take voltage as 25 V.D.C.

Now when transistor T_3 is conducting due to a bias given by R_{c2}, R_{b3} potential divider as shown in figure 4.7. A current I_3 flows through the collector and common emitter resistance R_{e23} and R_{e3}. At this time T_2 is not conducting and when T_1 is not conducting, the capacitor is charged to $V_c = V_p$. When the conduction of T_3 ceases, T_2 starts conducting. Let us assume the voltage drop across R_{e23} be $V = V_p = V_c$ so that capacitor can charge upto this voltage easily. Now at critical condition

$$R_{e23} I_3 = V_c = V_p = 8.0 \text{ volts}$$

$$\text{Choosing } R_{e23} = 2.5 \text{ K. Ohms}, \quad I_3 = \frac{8.0}{2.5 \times 10^{-3}}$$

$$= 3.2 \text{ mA}$$

Now when T_3 is conducting T_2 is not conducting. Rest of the voltage i.e. 25 - 8 = 17 volts should be across the collector resistance.

$\therefore$ Collector resistance

$$R_{c3} = \frac{17}{3.2 \times 10^{-3}} = 5.6 \text{ K. Ohms.}$$

Now as the voltage drop across R_{e23} biases the T_2 to cut off so logically that the current through T_2 should be less than T_3 to reduce the voltage across R_{e23}. Therefore choosing a higher resistance in the collector circuit of T_2, we can achieve this by choosing R_{c2} = 10 K. ohms.

Current in $T_2 = \frac{25}{10 + 2.5}$ = 2.0 mA.

NOW FOR TRANSISTOR T_1

As T_1 is off, the capacitor charges to V_p with a time constant $C(R_{c1} + R_{b2})$. Now time taken is about 1.2 m sec to charge the capacitor to 8 volts. Assuming C = 0.5 μ Farads, $(R_{c1} + R_{b2})$ is determined by the formula

$$t = C(R_{c1} + R_{b2}) \log \frac{E - V_p}{E}$$ where E is supply voltage.

If we do not go to a rigorous solution, we have to charge the condenser to about 8 volts.
Time constant is $(R_{c1} + R_{b2})C$ which is time taken to raise the voltage upto 70%.

Roughly $12 = (R_{c1} + R_{b2})C$

$$\therefore R_{c1} + R_{b2} = \frac{12 \times 10^{-3}}{0.5 \times 10^{-6}} = 24 \text{ K. ohms.}$$

Choose R_{c1} = 22 K. ohms.

and R_{b2} = 2 K. ohms

While discharging the capacitor through R_{b2} and transistor T_1 when T_1 is conducting, lesser resistance should be there for quick discharging

$$\therefore \quad R_{b2} < R_{c1}$$

Hence the current while T_1 is conducting through collector and emitter is 25/22 = 1.14 mA which is within safe limits.

R_{b3} should be chosen high so that while T_3 is conducting, no current should flow through base and emitter. Choosing R_{b3} = 30 K. ohms and R_3 = 47 K. ohms.

SUMMARY OF DESIGNS

R_{c1} = 22 K. ohms,		R_{b1} = 2 K. ohms	
R_{c2} = 10 K. ohms.		R_{b2} = 2 K. ohms	
R_{c3} = 5.6 K. ohms.		R_{b3} = 30 K. ohms	
R_3 = 47 K. ohms.		R_{e23} = 2.5 K. ohms (variable)	

R_{e23} is a variable resistor for fine adjustment of the phase comparator circuit.

A SYMMETRICAL BISTABLE TRIGGER CIRCUIT

It is used as a slave element in relaying operations. It responds to an input pulse or pulses

and produces a continuous output signal which is used to control the tripping coil of a circuit breaker. The circuit 4.8 has two transistors T_1 and T_2 with their emitters connected to the zero voltage line through a common emitter resistance R_{e12} shunted by a capacitor C_{e12}. The signal at the collector of each transistor is fed to the base of the other transistor through coupling resistors R_{11} and R_{22} and R_1 and R_2. The circuit possesses two conditions of stable equilibrium, in either of which one transistor is fully conducting and the other is cut off and can remain in one of these stages indefinitely unless it is forced to other state by some internal means. The capacitor is connected to determine the behaviour of the circuit during the transition from one state to another. The circuit is triggered by a negative pulse applied to the base of T_1 through a diode D in series with a capacitor to cancel any d.c. component. If after the circuit has been triggered, the h.t. supply is switched off and then on again, the circuit will assume its original state of stability with T_2 fully conducting and T_1 cut off. It remains in this state until again triggered to the other state. The circuit may be triggered from one stage to the other state by applying either a positive pulse to the base of conducting transistor to turn it off or a negative pulse to the base of nonconducting transistor to turn it on. The later usually demands loss of energy. Initially in the above circuit transistor T_1 is cut off and

T_2 is conducting. The time constant of T_1 circuit is made larger than that of T_2 circuit so that the collector voltage of T_2 will rise at higher rate than that of T_1. This is necessary because when supply is on, both transistor T_1 and T_2 race in conduction. The rise of T_2 is transferred to T_1 and oppose its tendency to conduct. This further reduces the rate of rise of T_1 and the process is commulation with the result that T_2 will be driven rapidly for full conduction while T_1 remains to cut off. When the negative pulse is applied to the base of T_1 the circuit is triggered to other state i.e. T_1 the conducting and T_2 is cut off. To reset, h.t. supply is switched off and then switch on again. The whole trigger circuit will be triggered when the positive half of the input wave is more than 12 m Sec.

DESIGN

When T_2 is conducting the potential of cathode of T_2 will increase which will be transferred to the base of T_1 through resistance R_{22} and T_1 will be biased to cut off by R_1. Now neglecting C, for the time being which is provided for stability.

When T_2 is conducting and R_{c2} and R_{e12} will act as a potential divider and total current through the collector and emitter should be about 8 mA. Whereas most of the resistance should be in collector circuit.

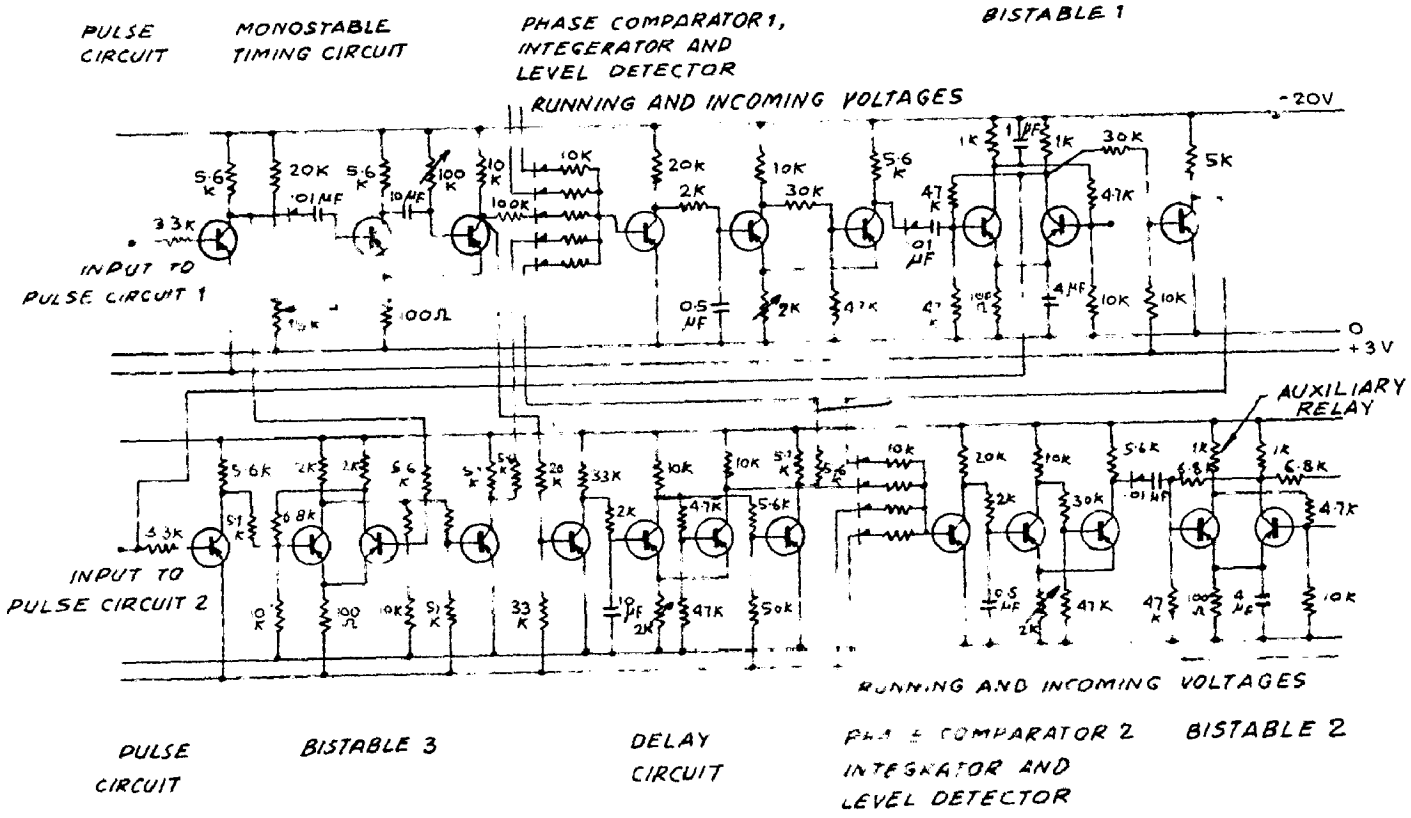


FIG. 4·9_ COMPLETE CIRCUIT OF AUTOMATIC CHECK SYNCHRONISING RELAY

Also current through R_{22} and R_1 should be minimum i.e. R_1 and R_{22} should be high as compared to R_{e12}.

Total circuit voltage supplied = 25 volts.

when T_2 is conducting $(R_{c2} + R_{e12})$ is $= \frac{25}{8} = 3.15$ K.ohm

Choosing R_{c2} = 3 K. ohms and R_{e12} = 150 ohms (used 100 ohms

R_1 is taken to be 47 K. ohms and R_{22} = 4.7 K. ohms.

The coupling capacitor C_c = 0.01 μ Farads.

The capacitor C_{e12} connected in parallel with R_{e12} is taken as 4 μFarade for the purpose of stability.

Semiconductor is provided for blocking purpose.

4.4.6 POWER SUPPLIES

The power supply requirements for the relay are a negative direct voltage of 25 volts capable of delivering upto 100 mA and a 5 volts positive bias of very little current drain. The bias voltage, although it can be provided by the power unit which supplies the main h.t. voltage was supplied by a d.c. variable source since its current is very small and the voltage level required is not critical.

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CHAPTER - V

EXPERIMENTAL PERFORMANCE

5.1 SLIP LIMITATIONS

The combination of the monostable, delay and phase comparator I circuits are such that the relay does not start operating until the slip frequency has been reduced below 0.4 c/s, though other choices of slip frequency limitations can be attained as required.

After this has been achieved, incoming generators have to make one complete revolution before the final closing signal to the circuit breaker operating mechanism can be produced. The period of this slip cycle will be more than 2.5 seconds and the generator must pass slowly through synchronism.

If for any reason, the circuit making switch fails to close at the required synchronous speed, a safe guard is used to ensure that no operation takes place beyond 0.4 c/s above synchronous speed. For this, a resetting signal has been added to bistable circuit I at the end of each slip cycle, the arrangement becomes ready again by the pulse from phase comparator I. This means that relay would operate only between the selected limits of $\pm$ 0.4 c/s.

5.2 UNBALANCE IN SOURCE VOLTAGES

Unbalance voltages upto ± 5% are allowed, otherwise pulse circuit I is not able to trigger the monostable circuit, and hence prevents operation. This is due to the slip cycle not attaining zero voltage with unbalance in the source voltages. This limit can be further reduced slightly by having a small resistance in the emitter circuit of the pulse circuit, which will reduce the cut off voltage.

5.3 ADVANCE TIME SETTING

It is not completely independent of the slip. The advance time is set to give a correct value at 0.3 c/s so that the circuit making switch closes slightly after phase coincidence of the two source signals between 0.4 c/s and 0.3 c/s slip frequency. Also the switch would close slightly in advance for slip frequencies between 0.3 c/s and zero.

5.4 TEMPERATURE CONSIDERATIONS

The transistor circuits are very temperature sensitive. Large changes in junction temperature will change its characteristics. As the collector power dissipation in switching circuits is negligible, the junction temperature remains almost the same as the ambient temperature.

5.5 TEST ARRANGEMENT

In the initial stages of construction, the slip frequency measurement method, pulse circuits, monostable, delay circuit, phase comparators and bistables were tested individually and were found to be working satisfactorily within the specified limits. Then the synchronising relay was tested by simulating the incoming generator by a source variable in both voltage and frequency (i.e. by changing the speed of the prime mover and the excitation of the generator), the reference source being the mains supply obtained by another generator).

The equipment was tested by synchronising experiment on two 3 phase generators as in the case of parallel operation of two 3 phase alternators. In these tests, the manual control was exercised over the excitation current of the incoming generator. Its performance was tested on an actual synchronising method used for parallel operation. It was found to conform with the synchroscope method. Synchronising took place only when the two machines were in phase, running at equal speeds and with almost equal voltages.

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CHAPTER - VI

C O N C L U S I O N

As shown by the successful operation of the automatic transistorised synchronising relay, the junction-transistor circuits can be reliably used in relaying and control problems. They give reliable and consistent operation and have all the advantages gained by having no moving parts.

The relay imposes a low burden on the voltage transformers to which it is connected.

The relay advance time setting is chosen deliberately over wide limits to cover the range 100-450 ms, which relates to making-switch closing times of 5-12 c/s at 50 c/s. The advance time setting includes the time from the instant when the circuit breaker operating mechanism becomes energised to the successful completion of the synchronising operation. The relay is calibrated to give a correct advance time at 0.4 c/s. If the relay operates at a lower slip, a slight inaccuracy in time setting will be there, but in any case the out of phase switching angle will not exceed 5^{o}. This deviation is of no consequence as no instability or damage to the incoming machine can be caused.

The maximum slip can be decreased or increased within certain limits. The maximum slip setting should not exceed 0.75-1 c/s even with the most accurate time

setting. The limit of voltage unbalance has been set for 5%.

The automatic-check synchronising relay is a useful application in the rapidly growing use of automation in power systems, since interconnected systems introduce many operating problems which make it undesirable to depend solely on human factors.

*****

APPENDIX I

ADVANTAGES OF JUNCTION TRANSISTORS IN ELECTRONIC RELAYS

It is a three terminal semi conductor device, three terminals being called, collector, emitter and base. Provided that the transistor is considered as a current operated device, these 3 terminals have functions similar to the anode, grid and cathode. When transistors are used as a two terminal network, there are three useful confugrations.

1. Earthed Collector
2. Earthed base
3. Earthed emitter

for large inputs, the earthed emitter arrangement behaves as a relay in which a small input power effects a change from a very high to a very low resistance in the output circuit.

EARTHED-EMITTER CHARACTERISTICS OF A JUNCTION TRANSISTOR

Fig. (b) shows the circuit arrangement and fig. (c) shows the static characteristic curves for the earthed emitter confugration. A load line AB is drawn on the characteristic, having slope $-\frac{1}{R_A}$ and intersecting the V_{ce} axis at $-V_e$ volts. If the input resistance R_b of the transistor is made large with respect to the base emitter impedance r_b of the

transistor (usually of the order of 400-700Ω), the base current to a first approximation will be

$$I_b = \frac{V_{in}}{R_b} \quad \text{when } V_{in} \text{ is negative}$$

when V_n is positive, no base current will flow and the transistor will be cut off so that the output voltage will be constant at V_0. When V_{in} is negative, base current starts to flow and the output potential falls along the load line until the point C is reached. At this point no further reduction in output voltage can occur, the only effect being an increase in the base current.

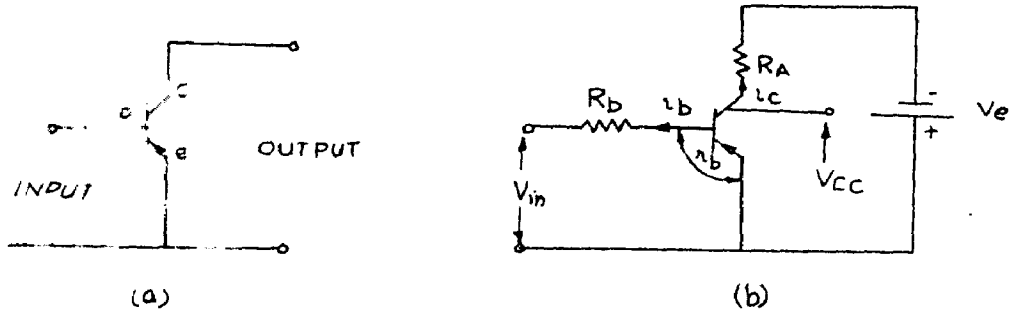
It is convenient to introduce α'', the large signal amplification factor or the ratio of collector current to base current at the point C.

$$\alpha'' = \frac{I''_c}{I''_b} = \frac{2mA}{40\mu A} = 50$$

At the point C, the output potential is so small that to a first approximation, it can be assumed to be zero, therefore at that point,

$$I''_c = \frac{V_c}{R_A}$$

$$I''_b = \frac{V_e}{\alpha'' R_A}$$



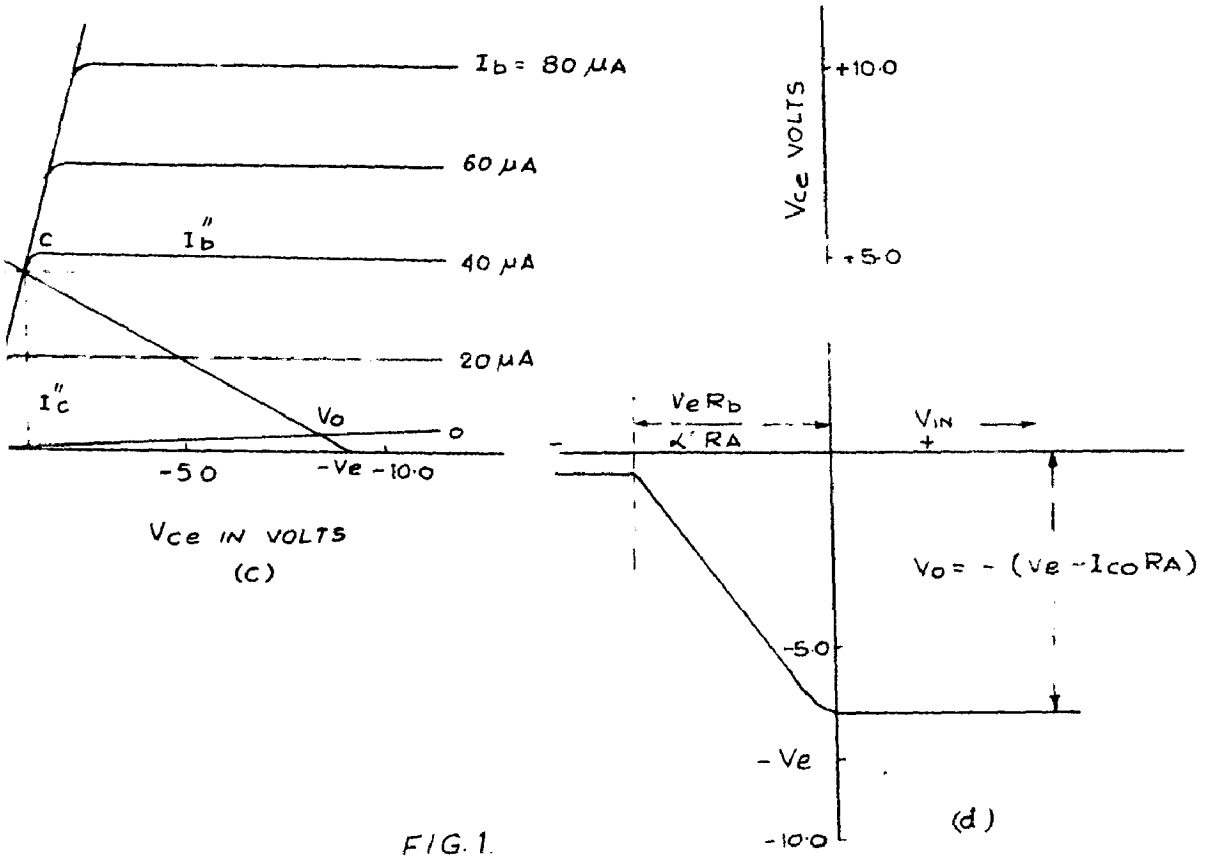


FIG. 1.

1. BASIC EARTHED EMITTER CONFUGRATION
2. BASIC TRANSISTOR AMPLIFIER
3. EARTHED EMITTER CHARACTERISTIC CURVES
4. SWITCHING CHARACTERISTICS OF JUNCTION TRANSISTOR

$$\text{and } V_{in} = I''_b R_b = \frac{V_e R_b}{\alpha'' R_A}$$

Thus the behaviour of this circuit may be summarised as follows :

$$\text{for } V_{in} \geqslant 0, \; V_{ce} = V_0 = -(V_e - I_{c0} R_A)$$

$$\text{for } V_{in} \leqslant -\frac{V_e R_b}{\alpha'' R_A}, \quad V_{ce} = 0$$

The overall characteristics are shown in fig. (d)

The transition from the cut off to the fully conducting condition takes place for a very small change of input voltage.

Typical figures are as follows :-

$V_e = 10$ volts

$R_b = 10$ K. Ω

$R_A = 20$ K. Ω

$= 30$

$$\therefore -\frac{V_e R_b}{\alpha'' R_A} = -0.17 \text{ volts}$$

Thus to a first approximation, the circuit behaves as a switch, it is in the "OFF" condition for positive

inputs and in the "ON" condition for negative inputs. This argument holds for a large signal conditions. Assumption is justified for the relay circuits which have been developed since the input voltages are taken directly from the 110 volt test transformer secondry windings.

APPLICATION OF JUNCTION TRANSISTORS

Junction transistor can be applied to relays in place of

(1) thermionic valves as it needs no special power supplies as in valve heaters.

(2) The provision of appreciable voltages in case of valve anodes and electrode bias is eliminated.

APPENDIX 2

Derivation of Single-phase Synchronising Out of Phase

During single phase synchronising, the sequence components of armature currents can be found by connecting the sequence networks as shown above in Fig. 8(b).

From the positive and negative-sequence components of current, the armature current is determined. Neglecting all rotor decrements, the instantaneous phase voltages during the transient can be written

$$e_a = E \cos (wt + \alpha)$$

$$e_s = E \cos (wt + \beta)$$

from which the a.c. symmetrical components of armature current can be solved.

$$i_{a1} = -i_{a2} = \frac{2E \sin\frac{(\alpha-\beta)}{2}}{X''_d + X_2 + 2X_s} \times \sin\left(wt + \frac{\alpha+\beta}{2}\right) \text{ per unit amperes}$$

The alternating phase currents are

$$i_b = -i_c = \frac{2/3\ E \sin\frac{\alpha-\beta}{2}}{X''_d + X_2 + 2X_s} \times \sin\left(wt + \frac{\alpha+\beta}{2}\right)$$

Since the currents must start from zero, there is a d.c. component present in the current. The total phase currents are therefore

$$i_b = -i_c = \frac{2\sqrt{3}\ E \sin\frac{(\alpha-\beta)}{2}}{X''_d + X_2 + 2X_s} \times \left[\sin\left(wt + \frac{\alpha+\beta}{2}\right) - \sin\left(\frac{\alpha+\beta}{2}\right)\right]$$

The instantaneous power is

$$P = \frac{2}{3}\left(i_a e_a + i_b e_b + i_c e_c\right)$$

$$= \frac{2}{3}\left[i_b(e_b - e_c)\right] = \frac{2}{3}\,\frac{2\sqrt{3}E\,\sin\left(\frac{\alpha-\beta}{2}\right)}{X_d'' + X_2 + 2X_s} \times$$

$$\left[\sin\left(\omega t + \frac{\alpha+\beta}{2}\right) - \sin\left(\frac{\alpha+\beta}{2}\right)\right] \times \sqrt{3}E\,\sin(\omega t+\alpha)$$

Since in per unit the rotor torque is equal to the power transferred across the gap

$$T = P = \frac{E^2 \sin\delta}{(X''_d+X_2+2X_s)}\left[1 - \cos 2(\omega t + \alpha) - \tan\frac{\delta}{2}\sin(\omega t+\alpha\right.$$

$$\left. -2\,\frac{\sin\left(\frac{\alpha+\beta}{2}\right)}{\cos\left(\frac{\alpha-\beta}{2}\right)} \times \sin(\omega t + \alpha)\right]$$

where $\delta = (\alpha - \beta)$

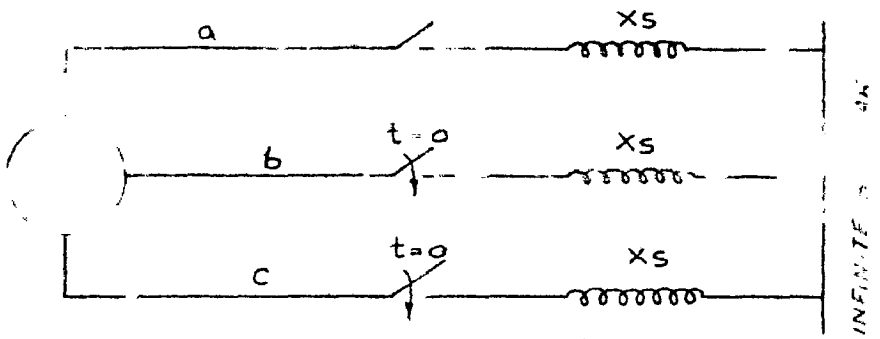
and (per phase machine constants in per unit)

X''_d = Direct axis sub transient reactance

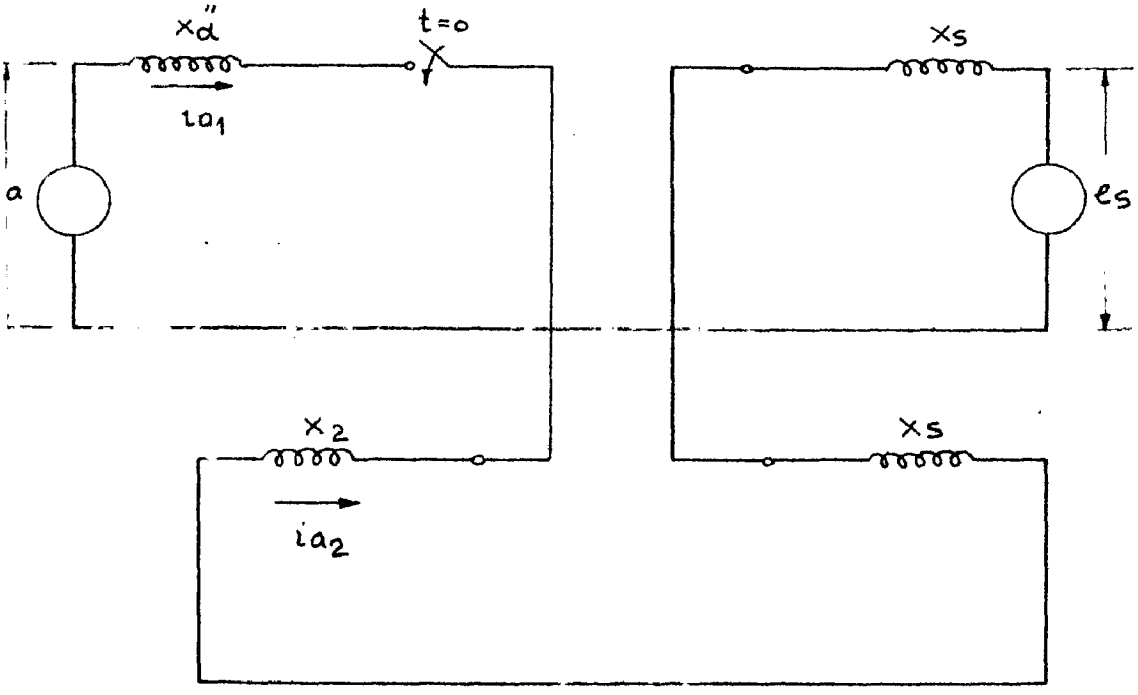
X_2 = Negative sequence reactance

E = Effective machine (or system) voltage

X_s = system reactance



(a)



(b)

SINGLE PHASE SYNCHRONISING

Similarly

equation of three phase Synchronising Torque Out Of Phase

$$T = \frac{E^2 \text{ Sin } \delta}{X''_d + X_s} \left[1 - \text{Cos wt} + \tan \frac{\delta}{2} \text{ Sin wt} \right]$$

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