DESIGN, FABRICATION AND TESTING OF A DIGITAL I.D.M.T. OVERCURRENT RELAY

A DISSERTATION

Submitted in partial fulfilment of the requirements for the award of the degree of

MASTER OF ENGINEERING

IN

ELECTRICAL ENGINEERING

(Power System)

By

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CERTIFICATE

Certified that the dissertation entitled "Design, Fabrication and Testing of a Digital IDMT Overcurrent Relay", which is being submitted by Shri Mrityunjai Prasad in partial fulfilment of the requirements for the award of the Master of Engineering in Electrical Engineering (Power System) of the University of Roorkee, Roorkee is the record of student's own work carried out by him under my supervision and guidance. The matter embodied in this dissertation has not been submitted for the award of any other degree or diploma.

It is to further certify that he has worked for the period of five months, i.e. 1.08.86 to 3.11.86 and 1.08.88 to 1.10.88 for preparing this dissertation.

6/5/89

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Dated: 06.05.89

(MRITYUNJAI PRASAD)

CONTENTS

CHAPTER - 1

1. INTRODUCTION

Basic idea of protection is to ensure the availability of electrical energy without interruption to every load connected to the system. Protective relays and relaying systems detect abnormal conditions like faults in electric circuits and operate automatic switchgear to isolate faulty equipment from the system as quickly as possible, to limit the damage at the fault location and to present the effects of the fault spreading into the system. Thus the main function of a protective relay is to isolate a faulty section as quickly as possible with the least interruption to service by controlling the circuit breaker, when abnormal condition develop. So, the relay may be designed to detect and to measure abnormal conditions and close the contacts in the tripping circuit.

With the developments in large scale integrated technology sophisticated and fast microprocessors are coming up.[6] With the growing complexity of modern power networks fast, accurate and reliable schemes are becoming necessary. Microprocessor based protective schemes can easily fulfil these requirements at competitive price. These schemes offer attractive compactness and flexibility. They reduce the number and types of relaying units. Here an interface employing operational amplifiers, A/D converter has been developed to obtain the relaying characteristic. Moreover the static form offers the following advantages over the electromagnetic form:[4]

i) Low burden on CT, so that smaller CT's are required.

ii) Compactness of the unit and reduction in panel space.

iii) Instantaneous reset possible because of the absence of moving parts, which facilitates the application of automatic reclosing of breakers.

iv) Less maintenance, long life shock and vibration proof.

v) No. over reaching tendencies and great accuracy of the characteristics.

CHAPTER - 2

2. CONVENTIONAL O/C RELAYS[5]

Over current relays are generally used on circuit breakers over 1000 V and to some extent on low voltage circuit breakers where greater accuracy is required than can be provided by certain direct acting trip coils on the circuit breakers.

2.1 Principle and Construction of Overcurrent Relays

The over current relays used in the industry are mainly of the electromagnetic attraction and induction type. Solid state overcurrent relays have become available in recent years. Their characteristics are generally comparable to induction relays, except that they can provide faster reset times and have inherently reduced overtravel. The simplest over current relay using the electromagnetic attraction principle is the solenoid type. The basic elements of this relays are a solenoid and a movable plunger.

When the circuit is energized with current at or above the minimum pick up value, the coil raises the plunger up into the operated position which closes the contracts in the trip

circuit. A calibration screw is provided to adjust the initial position of the plunger.

2.1.1 Induction Type Time Delay Over Current Relay

The most commonly used time-delay relays for system protection use the induction disc principle. The same principle is used on alternating current watt hour meters and when applied to relay construction, it provides many varieties of time characteristics, depending on minor differences in electrical and mechanical design. The principle components parts of an induction type over current relay are shown in fig. No. 1. The elements of an induction disc type relay are shown in fig. 2. The disc is mounted on a retating shaft restrained by a spring. The moving contact is fastened to the shaft. The operating torque on the disc is produced by an electromagnet. A damping magnet provides restraint after the disc starts to move. This feature provides the desired time characteristic. The time scale indicates the initial position of the moving contact when the relay is de-energized. Its setting controls the time necessary for the relay to close its contact. A relay constructed on these principles has an inverse time characteristic. This means the relay operates slowly on small values of over current, but as the over current increases, the time of operation decreases. There is a limit to the speed at which the disc can travel. If the current continues to increase, the time curve of the relay will tend to reach a constant value. Different time current curves of relays can be obtained by minor modifications of electromagnetic design.

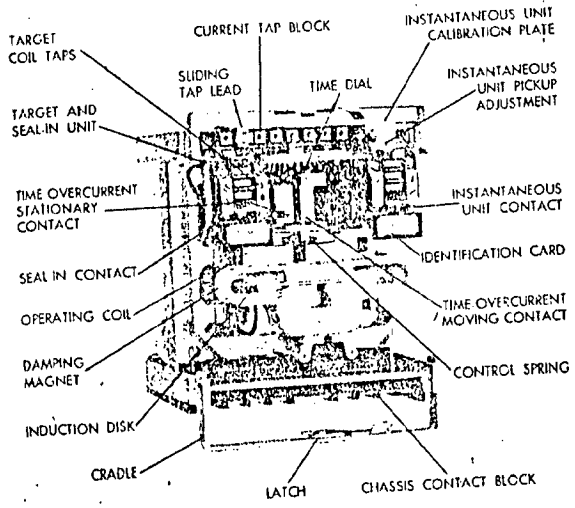


FIG. 1

INDUCTION DISC OVERCURRENT RELAY WITH INSTANTANEOUS ATTACHMENT

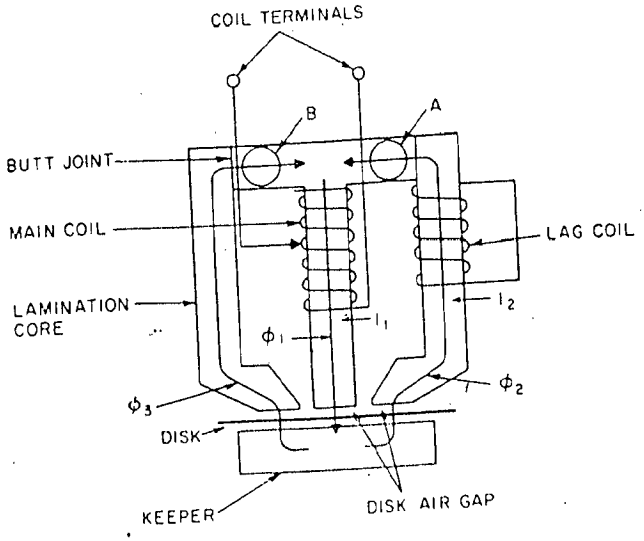


FIG. 2.

ELEMENTARY INDUCTION TYPE RELAY

An auxiliary seal in relay is incorporated into the relay case to lighten the current carrying duty of the moving contact. It also operates the target indicator.

2.2 Instantaneous Trip Attachments

The induction relay is generally provided with an auxiliary alternating current operated instantaneous clapper-type current element. This element is provided with an adjustable calibrated range of 1:4 and is set for a current higher than that which should operate the time delay element. The contacts of this elements are either connected in parallel with the contacts of the time delay element or they are connected to separate terminals.

2.3 Solid State Over Current Relay

Some new over-current relay designs utilize solid state technology. Time current curves are obtained through the use of RC timing circuits. Time current characteristic curves and tap ranges are similar to those provided in induction relays. Solid state over current relays have the same applications as induction relays and are particularly useful in certain sever environmental conditions or where fast reset is required.

2.4 Over Current Relay Types and Their Characteristic Curves[4]

The operating time of all over current relay tends to become asymptatic to a definite minimum value with increase in valve of the current. This is inherent in electromagnetic relays due to saturation of the magnetic circuit. So by varying the point of saturation different characteristics are obtained these are:

(a) Definite time

(b) Inverse definite minimum time (IDMT)

(c) Very inverse

(d) Extremely inverse

The above said characteristics are obtained by induction disc and induction relays. The torque of these relays is proportional to $\Phi_1 \Phi_2 \sin\alpha$ where Φ_1 and Φ_2 are the two fluxes cutting the disc or cup and α is the angle between them. Where both fluxes are produced by the same quantity, as in current or voltage operated relays, then below saturation, the torque is proportional to I^2, the coil current or $T = KI^2$. If the core is made to saturate at a very early stage with the result that by increasing I, K decreases so that the time of operation remains same over the working range. The characteristic is shown by curve (a) in fig. (3) and is known as definite time.

If the core is made to saturate at a later stage, the characteristic assume the shape shown by curve (b) known as IDMT. At low values of operating current the shape of curve is determined by the effect of restraining force of the control spring, while at high values the effect of saturation predominates. Different time multiplier settings (TMS) are obtained by varying the travel of the disc or cup required to close the contacts.

It the saturation occurs at a still later stage the characteristic assume the shape shown by curve (c) in fig. (3) known as very inverse. The time current characteristic is inverse over a greater range and after saturation tend to definite time.

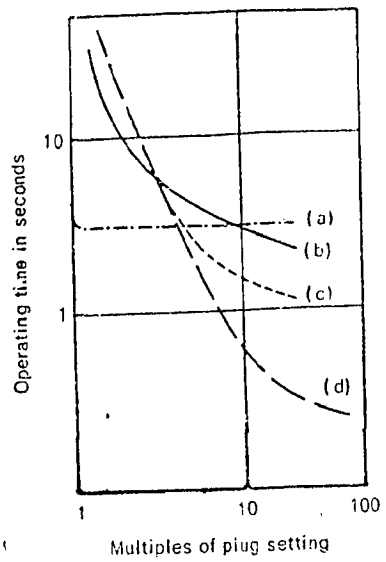


FIG. 3

CHARACTERISTICS OF VARIOUS OVER CURRENT RELAYS:

(a) DEFINITE TIME (b) IDMT

(c) VERY INVERSE (d) EXTREMELY INVERSE

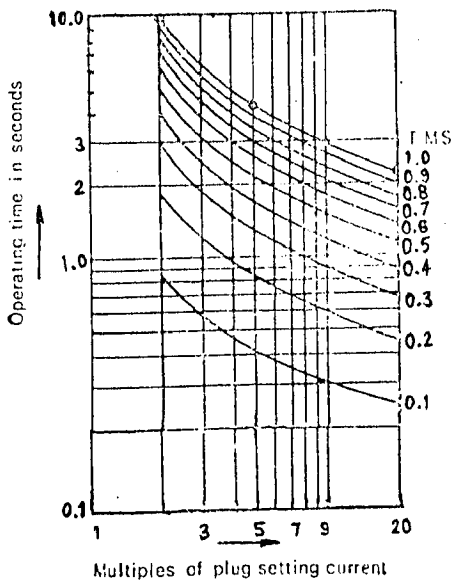


FIG. 4.

TYPICAL IDMT CHARACTERISTICS WITH DIFFERENT TIME MULTIPLIER SETTINGS

The curve (d) in fig. (3) shows extremly inverse characteristic i.e. the saturation occurs at a very late stage and the equation of the curve is roughly of the form $I^2t = K$ where I is the operating current and t is the time of operation.

However, a general expression for the operating time of a time current relay is

$$t = \frac{KM}{I^n - I_p^n}$$

where t = time of operation in seconds

K = design constant

M = time multiplier setting (TMS)

I = multiple of tap current

I_p = multiple of tap current at which pickup occurs

n = index number which is empirical

The nature of curves and their degree of inverse characteristics have been standardized. According to British standards following are the specified curves:

Standard inverse (IDMT) : $t = \frac{0.14}{I^{0.02}-1}$

Standard very inverse : $t = \frac{13.5}{I - 1}$

Standard extremely inverse $t = \frac{80}{I^2 - 1}$

Out of all these characteristic IDMT is the only characteristic which is specified by (IS : 3231 - 1965) the rest are all relative curves. Following table shows the time current characteristic of an IDMT relay

Operating current expressed as a multiple of the setting	Operating time in sec. at the max. time setting (TMS = 1.0)
20	2.2
10	3.0
5	4.3
2	10.0

The time current characteristic is conveniently plotted on a log-log scale. Fig. 4 shows the IDMT characteristic with different time multiplier settings (TMS).

Fig. 6 compares the characteristic of the various types of inverse relays referred above[1]. It should however, be noted that all these curves are shown at unit time multiplier setting. The time current characteristics for a variety of relay are shown in fig. 7 to fig. 13. These characteristics give the contact closing times for the various time dial settings when the indicated multiples of tap current are applied to the relay.[5]

2.5 Special Types of Over Current Relays[5]

By adding different elements to the basic over current relays as discussed above, several special types of O/C relays are derived.

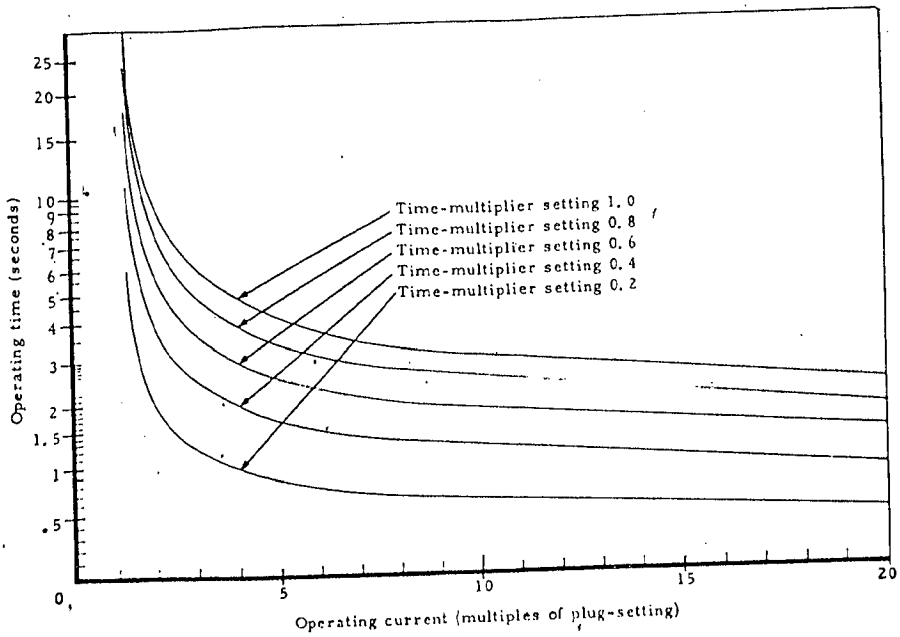


FIG. 5. I.D.M.T. OVERCURRENTS/ RELAY TIME/CURRENT CHARACTERISTICS

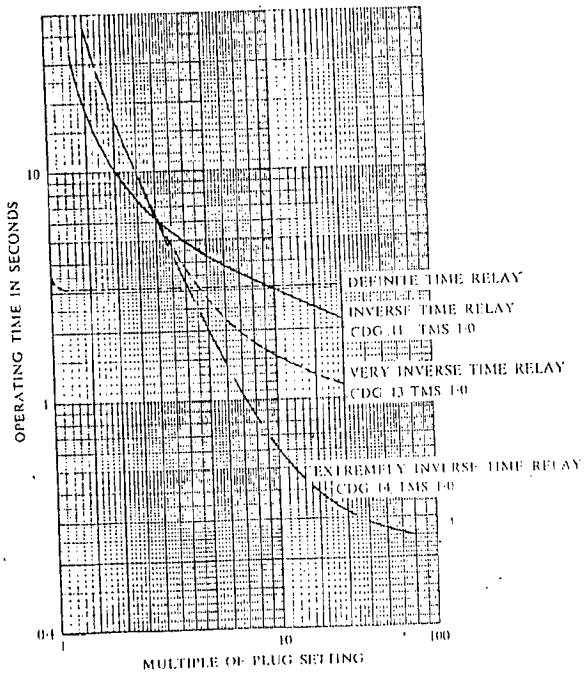


FIG. 6. COMPARISON BETWEEN CHARACTERISTICS OF THE VARIOUS TYPES OF OVERCURRENT RELAYS

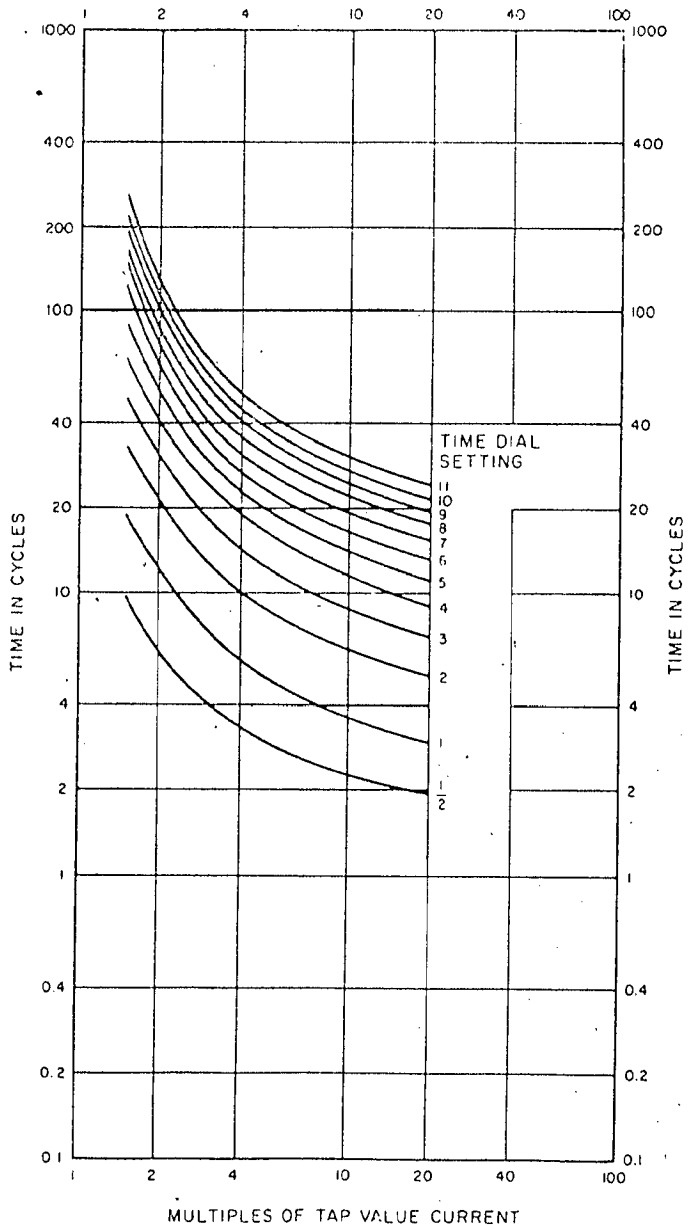


FIG. 7

TYPICAL TIME - CURRENT CURVES FOR SHORT TIME RELAY

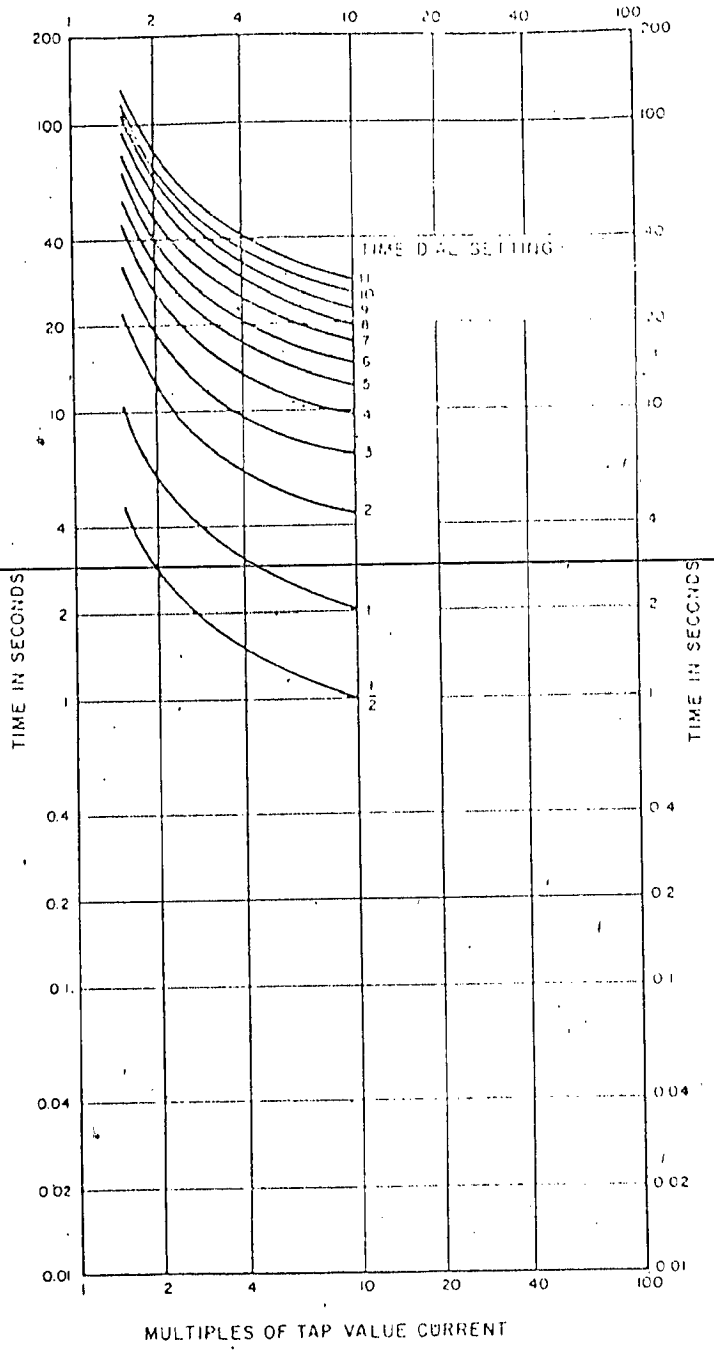


FIG. 8

TYPICAL TIME - CURRENT CURVES FOR LONG-TIME RELAY

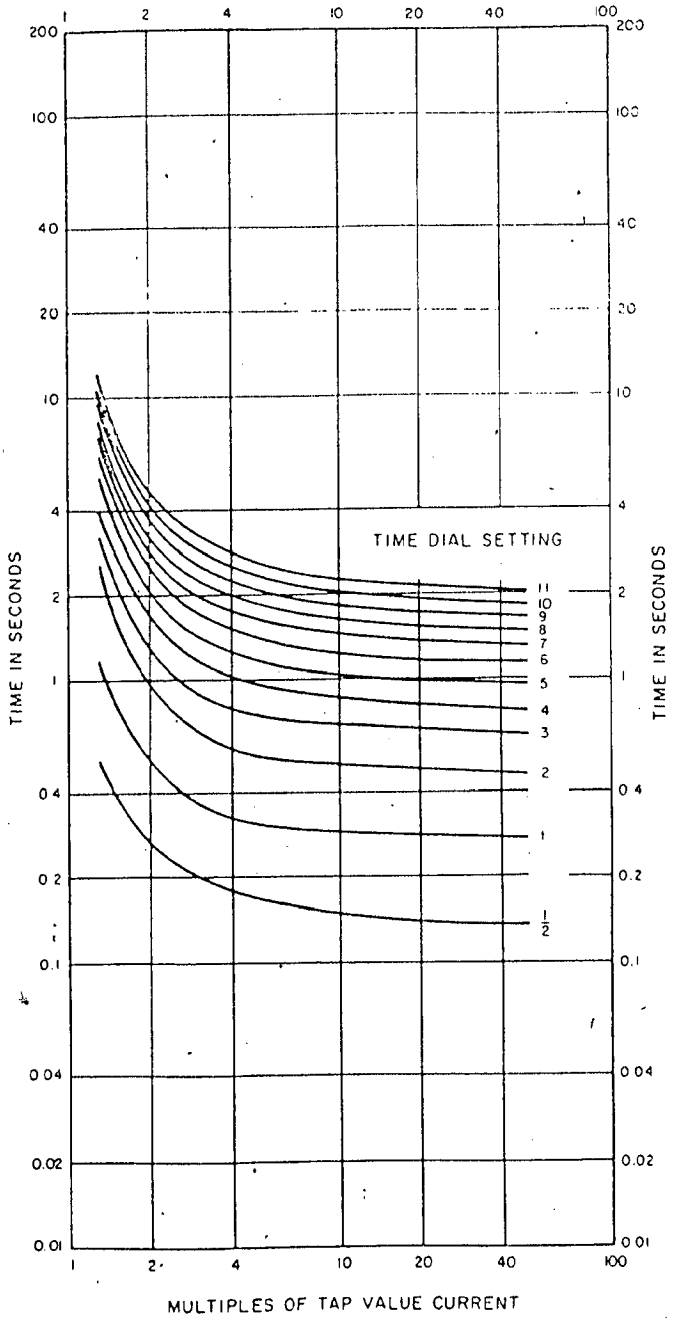


FIG. 9

TYPICAL TIME-CURRENT CURVES FOR DEFINITE MINIMUM-TIME RELAY

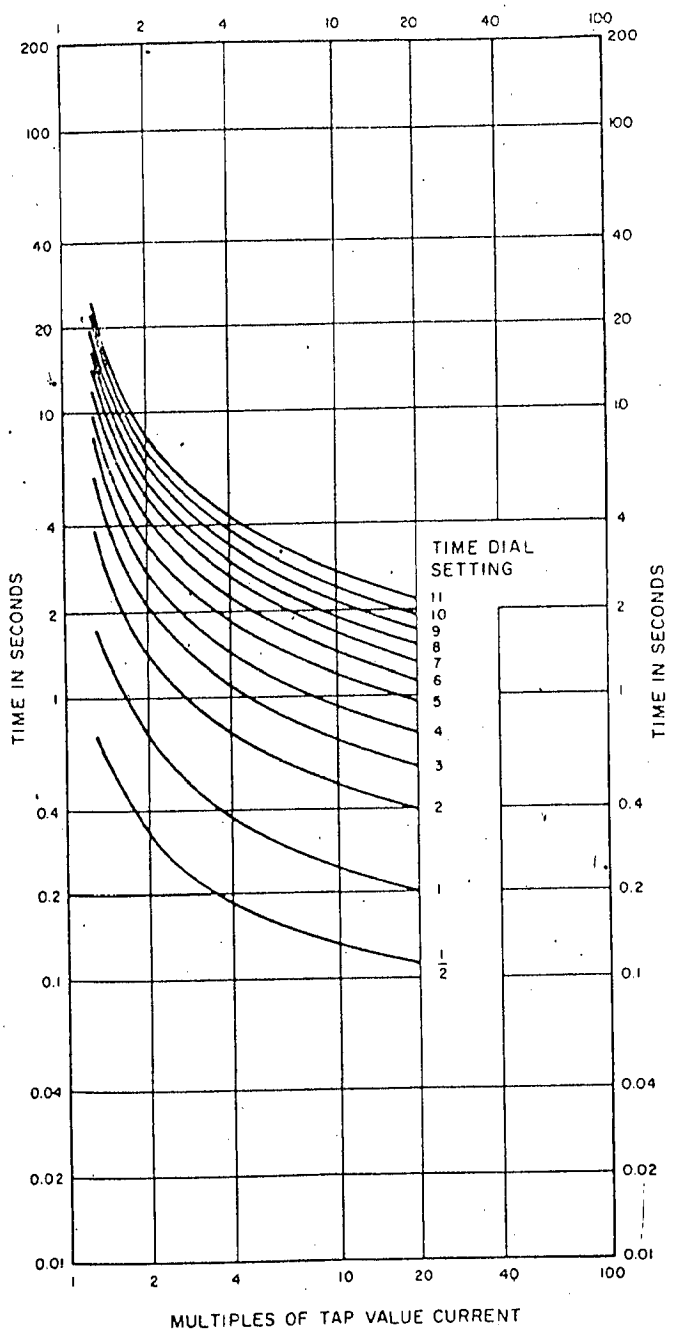


FIG. 10

TYPICAL TIME - CURRENT CURVES FOR MODERATELY INVERSE - TIME RELAY

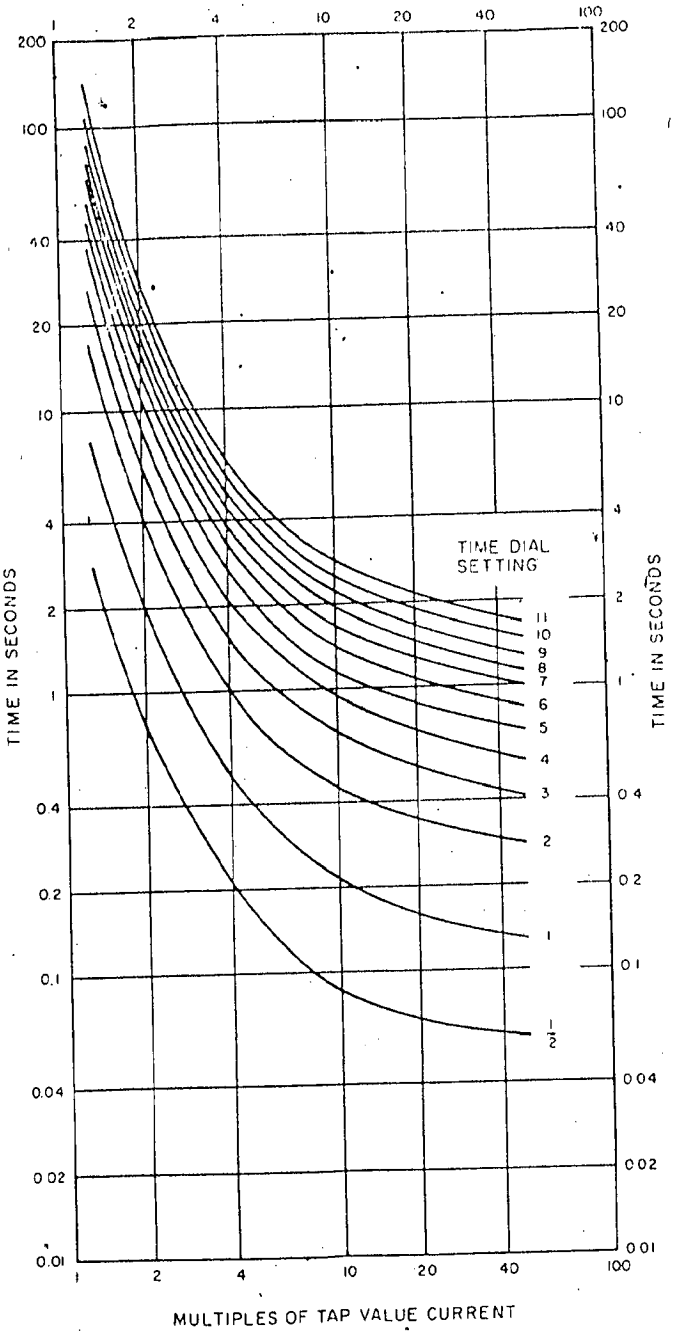


FIG. 11

TYPICAL TIME - CURRENT CURVES FOR INVERSE - TIME RELAY

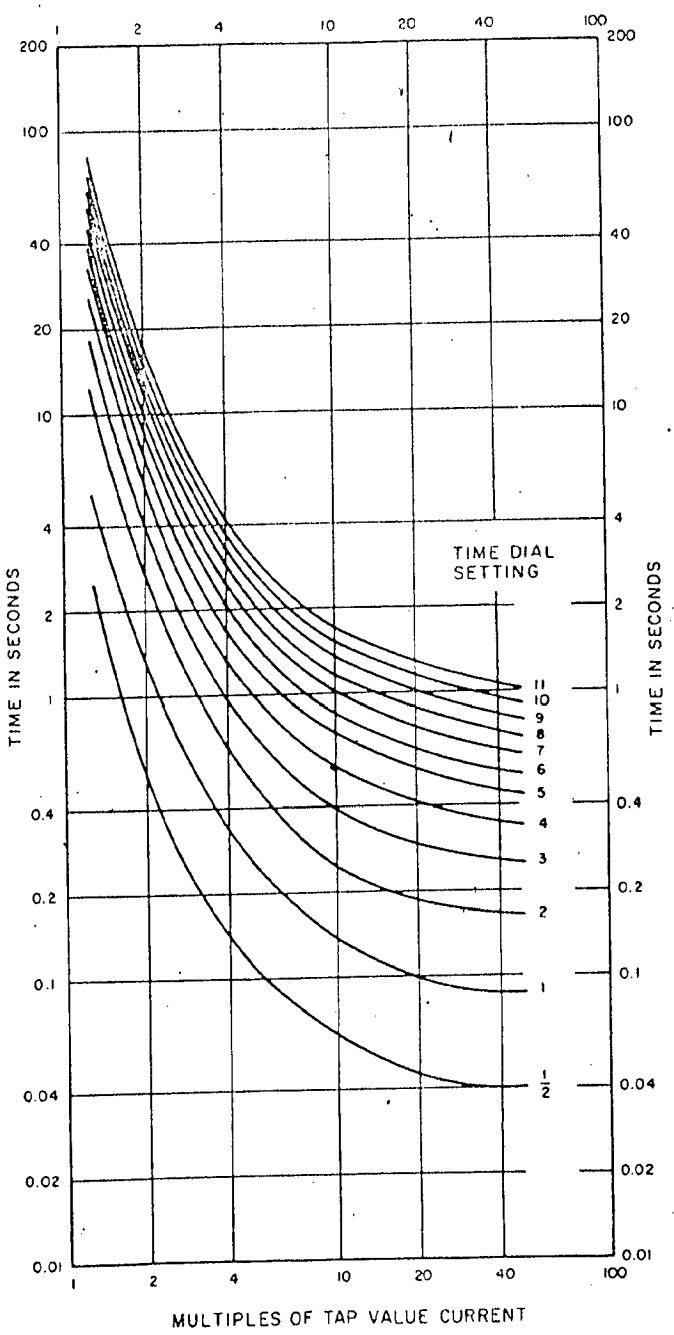


FIG. 12

TYPICAL TIME - CURRENT CURVES FOR VERY-
- INVERSE TIME RELAY

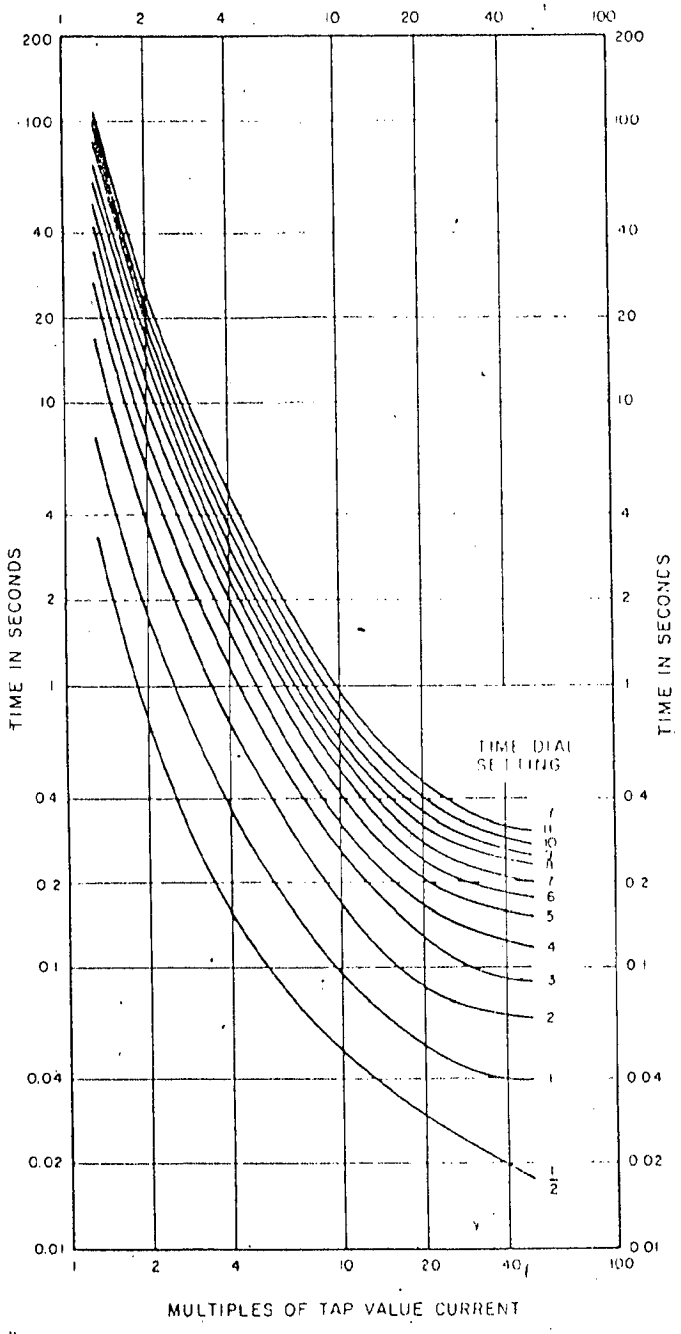


FIG. 13

TYPICAL TIME - CURRENT CURVES FOR EXTREMELY INVERSE TIME RELAY

2.5.1 Voltage Controlled (Restrained) Over Current Relay

When a fault occurs, the system voltage collapses to a relatively low value, but when an overload occurs, the voltage drop is relatively small. If an overcurrent relay is provided with a restraining torque proportional to voltage, it will recognize the difference between a fault where the voltage drops and an overload where the voltage is maintained. Such relays will provide sensitive fault protection without tripping on small overloads. They are used for generator circuits for back up for external faults.

2.5.2 Directional Over Current Relay

This relay consists of two units, an over current element and a directional element. The contact circuits are arranged in such a way that tripping occurs only when current has proper relationship to the voltage with power flow in the tripping direction. The same function is also obtained by the use of a single element that combines a suitable time delay and directional characteristic. The directional element is somewhat similar in principle to a contact making wattmeter, held in the open position by a spiral spring when de-energized. This element is designed with high sensitivity to assure positive operation over the widest range of current and voltage relations encountered during a fault.

The actual tripping of the circuit is done by a contact on the over current element. With the directional control element, the over current element does not operate until the current

is flow in the proper direction and is above the pick up setting. The over current element can not operate on a fault in the nontripping direction. (Fig. 14).

2.5.3 Directional Over Current Relay with Voltage Restraint

Sometimes it is desirable to restrain the directional element from closing its contacts on normal load current flow in the tripping direction by using voltage to restrain the operation of the directional element. The use of voltage restraint can allow a wider choice of relay settings to fit the requirements of systems which have wide variations between minimum and maximum fault conditions.

The voltage restraint is greatly reduced when there is a phase-to-phase or a three phase fault. Proper relay operation during a three-phase fault will depend on the sensitivity of the relay.

2.5.4. High Speed Directional Over Current Relay

A high speed directional element and an overcurrent element are coordinated to operate upon the occurance of a short circuit that reverses the normal flow of current. Proper co-ordination of elements requires that a contact on one high speed element open before the contact on another can close when the relay is suddenly de-energized or a quick reversal in power flow occurs.

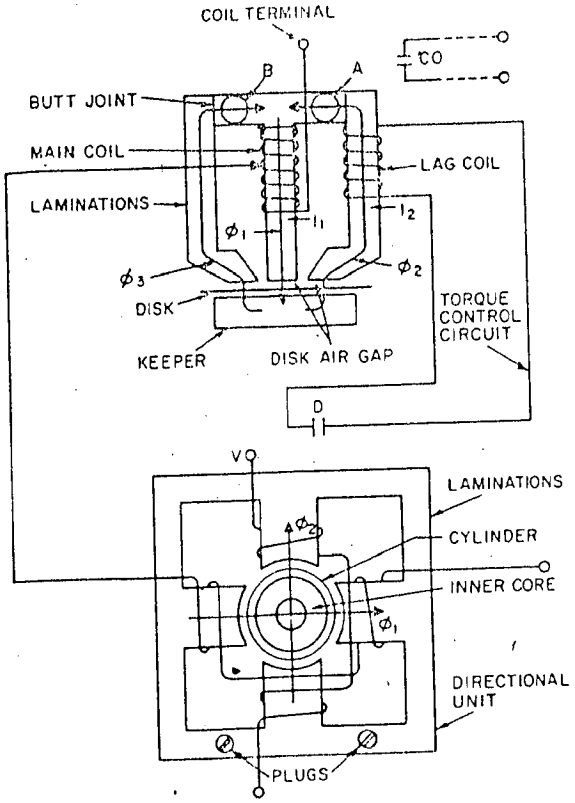


FIG. 14

DIRECTIONALLY CONTROLLED OVER CURRENT RELAY

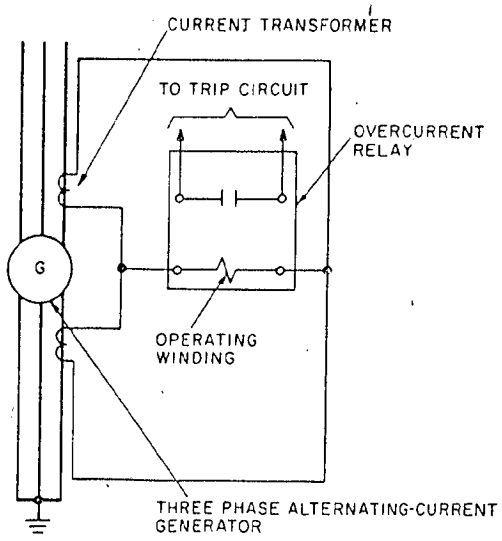


FIG. 15

OVERCURRENT RELAY USED FOR DIFFERENTIAL PROTECTION OF A GENERATOR

2.6 APPLICATION OF OVER CURRENT RELAYS[5]

2.6.1 Differential Protection

Differential protection operates by comparing the current flowing into a circuit with the current flowing out of the circuit, Normally the currents are the same and difference between them is zero. If a fault occurs in the circuit, part of the current flowing out will be deflected into the fault, and a differential current will flow. Differential protection may be applied to any section of a circuit and is used extensively to protect motors, generators and transformers against internal faults. It detects internal faults immediately and is not affected by overloads or faults outside the differentially protected section. Fig. 15 shows an overcurrent relay used for differential protection of a Generator.

2.6.2 Overload Protection of Rotating Apparatus

In installations where some scheme of overload protection is desired, an appropriate type of overcurrent relay is a time delay relay. An instantaneous relay would require a setting above the maximum momentary peak loads. Since the short circuit current as determined by the synchronous reactance may be of the order of full load, the over current protection of generators can be as satisfactory as the overcurrent protection for motors.

Fig. 16 shows overload protection combined with instantaneous short circuit protection for motors using long time delay overcurrent relays.

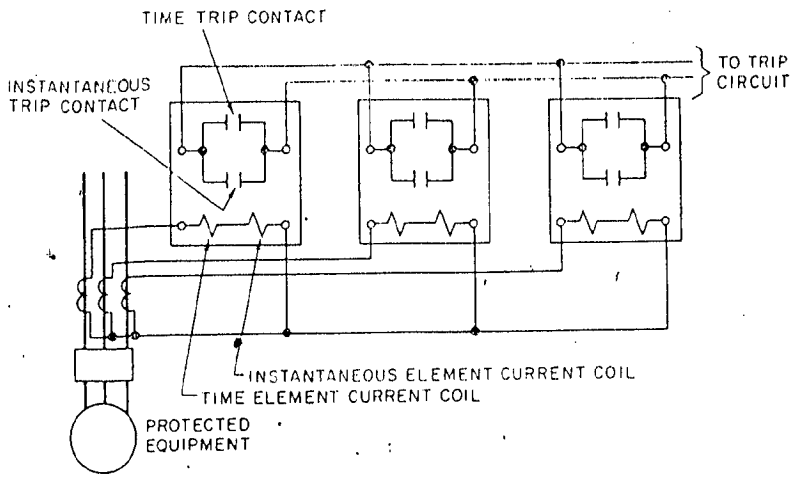


FIG. 16

OVERLOAD PROTECTION COMBINED WITH INSTANTANEOUS SHORT CIRCUIT PROTECTION FOR MOTORS USING LONG TIME DELAY OVERCURRENT RELAYS

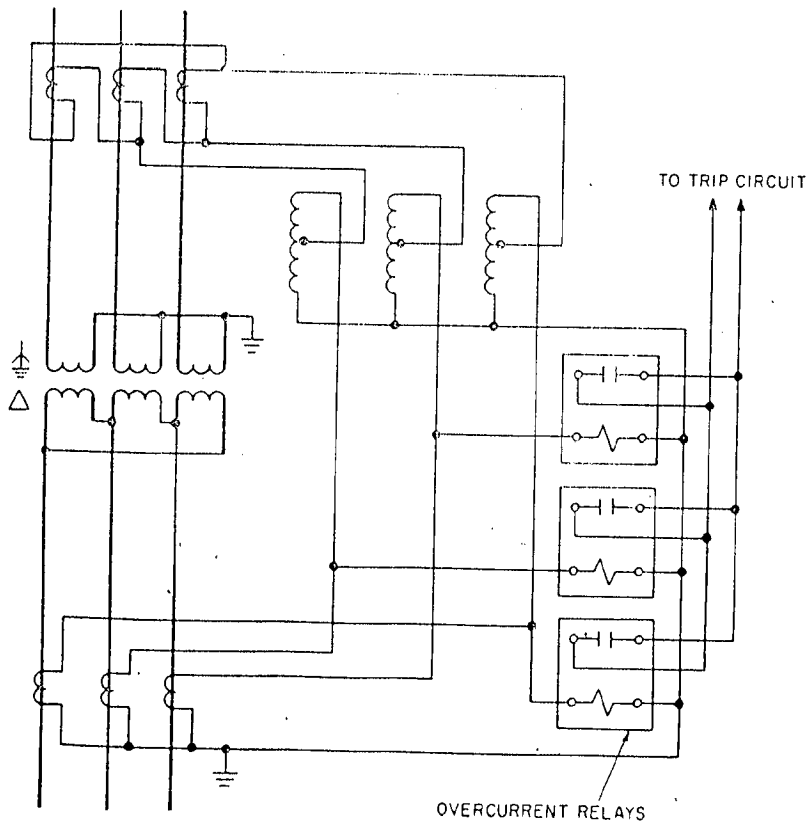


FIG. 17

DIFFERENTIAL PROTECTION OF TWO WINDING Y-Δ TRANSFORMER BANK USING INDUCTION TYPE OVERCURRENT RELAYS

2.6.3 Differential Protection of two Winding Y-Δ Transformer Bank

When differential relays are used for the transformer protection, the inherent characteristics of the power transformers introduce a number of problems which do not exist in the protection of generators and motors. Magnetizing inrush current in the transformer bank appears to the relay as an internal fault. The voltage transformation of the power transformer may not be exactly matched in the current transformer circuit so that unequal secondary currents occur on through faults.

If the secondary currents on the two sides of the transformer differ in magnitude, the relay currents can be matched by means of a current balancing auto transformer. If the high voltage and low voltage line currents are not in phase due to Y-Δ connection in the transformer, the secondary currents can be brought into phase by connecting the current transformer in Δ on Y side and in Y on the Δ side.

Since the current transformers on the two sides of a power transformer bank will have different ratios and may be of different types, the differential current caused by dissimilar ratio characteristics will be considerably greater than in the case of generator protection. This is the reason why ordinary overcurrent relays can not be given sensitive settings and transformer differential relays are generally used instead. Fig. 17 shows differential protection of two winding Y-Δ transformer bank using induction type overcurrent relay.

2.6.4 Protection Against Phase to Phase Faults Within a Zig-Zag Connected Transformer

When a zig-zag connected grounding transformer is used to provide a source of ground current for a system where the power transformers are not grounded, overcurrent relays are sometimes used for protection against phase to phase faults within the transformer, while a differential relay may be used to secure protection against phase to ground faults. To protect against ground faults elsewhere on the system, which may fail to be automatically cleared and which will eventually overheat the grounding transformer, a thermal relay can be used. However, to provide faster protection against more severe faults of this nature a long time delay overcurrent relay is usually used instead of the thermal relay.

2.6.5 Protection of Distribution Lines

A radial system is one having a single source of power with feeders leaving the source bus, each feeder in turn being subdivided into a number of smaller feeders. The protection of such a system against short circuits may be obtained by overcurrent protective relays. The circuit breaker near the source as well as the intermediate circuit breaker must be equipped with the time delay relays. The time interval required between successive relays must be long enough to assure selective operation and relays at the source bus will have the highest time settings. The most remote relays will have an instantaneous setting. Fig. 18 shows phase and ground over current protection to a circuit phase induction type overcurrent relays.

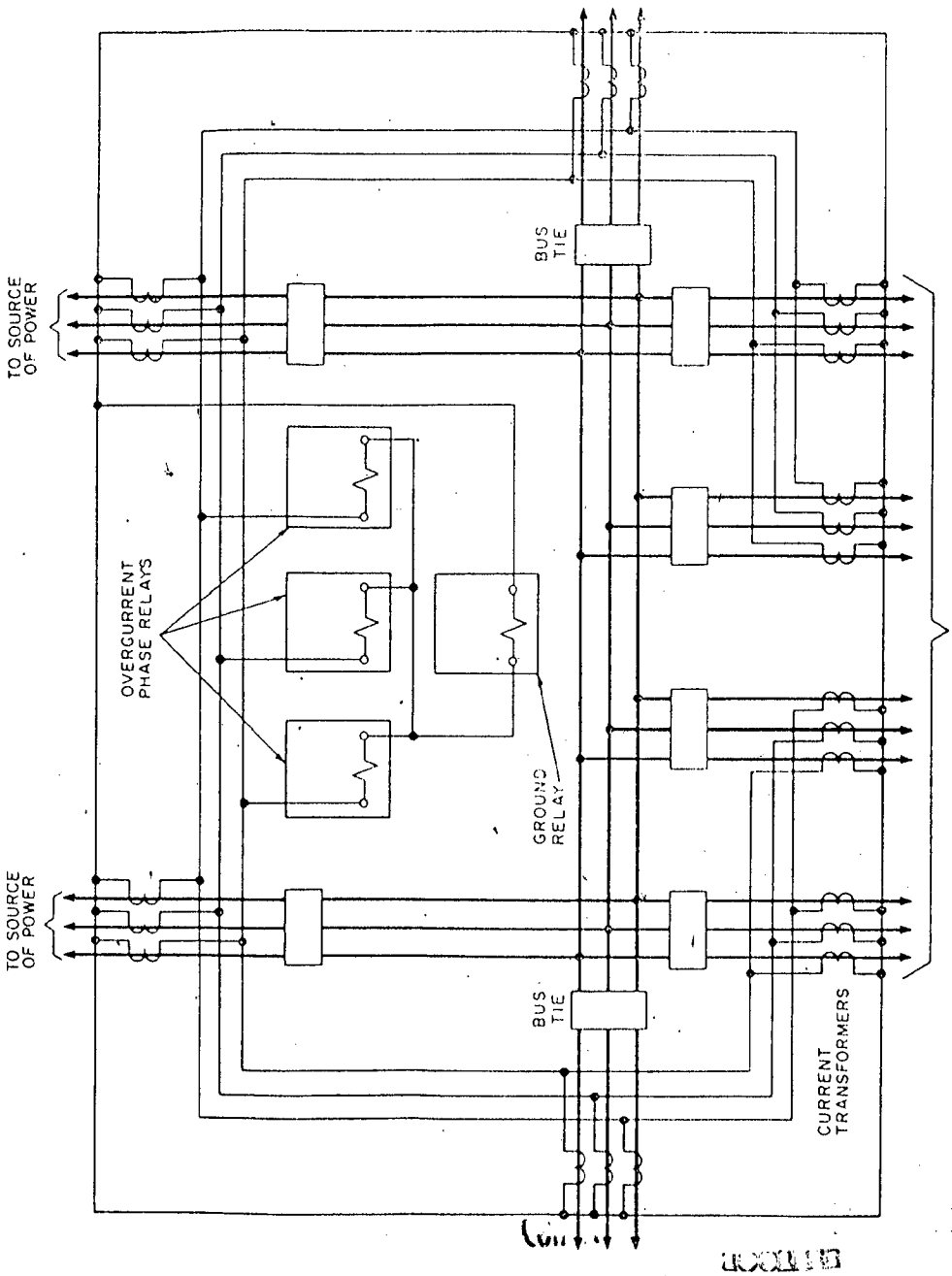


FIG. 18
PHASE AND GROUND OVERCURRENT PROTECTION OF EIGHT CIRCUIT BUS USING INDUCTION TYPE OVERCURRENT RELAYS

2.6.6 Ground Fault Protection

Overcurrent protection for ground faults, using time as the means of selectivity, follows the same principle as outlined for phase protection. Settings can be made if the short circuit magnitudes are known. The connections for a ground overcurrent relays are shown in fig. 19.

2.7 TIME MULTIPLIER SETTING AND PLUG SETTING MULTIPLIER IN INVERSE RELAYS[4]

There are two basic adjustable settings on all inverse relays; one is the time multiplier settings (TMS) and the other is the current setting usually known as the plug setting multiplier (PSM).

The time setting is adjustable from 0 to 1.0, the value selected being a multiple of the operating time shown on the time/ current characteristic curve, which is drawn for a time setting of 1.0 (TMS) shown in the fig. 20.

The time multiplier setting for an inverse time relay is defined as

$$TMS = \frac{T}{T_m}$$

where T = the required time of operation

and T_m = the time obtained from the relay

Characteristic curve at TMS = 1.0, and using the PSM equivalent to maximum fault current.

Thus, if the TMS is 0.1 and the time obtained from the

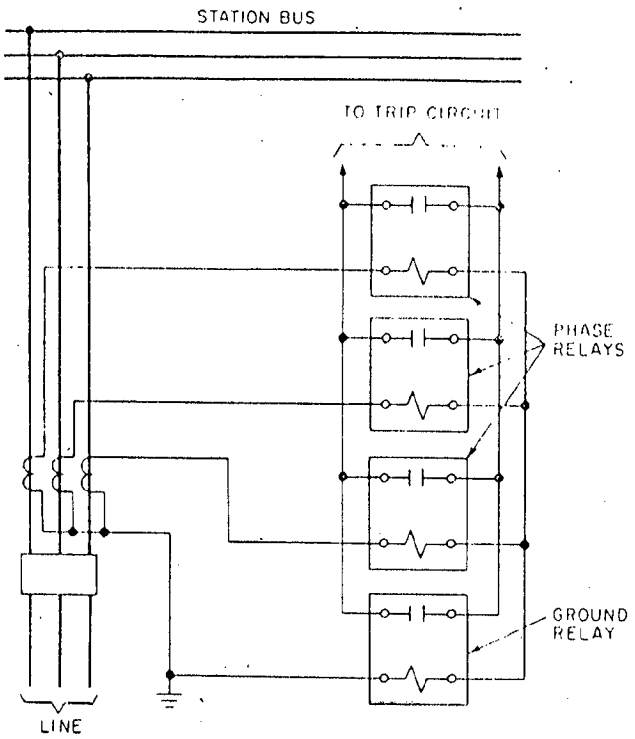


FIG. 19

PHASE AND GROUND OVERCURRENT PROTECTION OF A CIRCUIT USING INDUCTION TYPE OVER CURRENT RELAYS

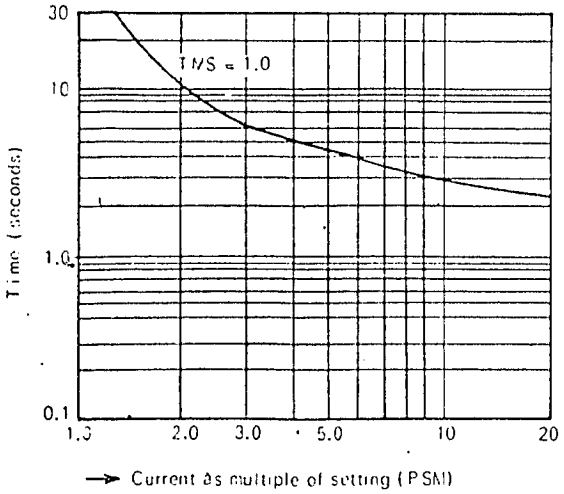


FIG. 20.
STANDERD IDMT CURVE

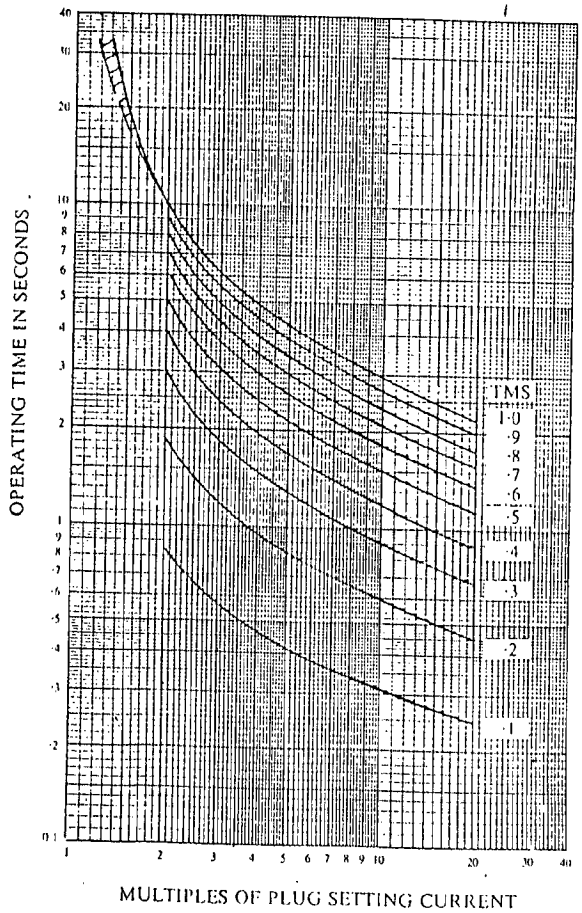


FIG. 21

TYPICAL TIME/CURRENT CHARACTERISTICS
FOR 3 SECOND INVERSE TIME RELAY

curve, for a particular current is 4.0 seconds, the actual operating time will be 4.0 x 0.1 = 0.4 second. In other words, if the time from the curve is 4.0 seconds and the operating time required is 0.4 second the TMS should be 0.4/4.0 = 0.1. Increasing the TMS has the effect of moving the curve higher on the time scale.

Current setting is adjusted by means of a tapped plug bridge hence known as PSM.

$$PSM = \frac{\text{Primary Current}}{\text{Primary Setting Current}}$$

$$= \frac{\text{Primary Current}}{\text{Relay Current Setting x CT ratio}} = \frac{\text{Primary Current}}{\text{Primary Operating Current}}$$

Where, as is usually the case, the rated current of the relay is equal to the rated secondary circuit of the C.T. For example, if the maximum fault current that can flow through the relay location is 3000 A and relay is set to operate at 200 primary amperes, then $PSM = \frac{3000}{200} = 15$, or if the primary current is 3000 A and relay current setting is 50% and the C.T. ratio is 400/5 then

$$PSM = \frac{3000}{2.5 \times 80} = 15$$

for the same primary current and a relay current setting of 200%

$$PSM = \frac{3000}{10 \times 80} = 3.75$$

CHAPTER - 3

3. PROPOSED OVER CURRENT RELAY SCHEME

In the proposed scheme an IDMT over current relay is being developed which is microprocessor based. The load current/ fault current is being reduced almost 10 times with the help of a current transformer and a current to voltage converter has been developed to give an output voltage proportional to the load current. This is necessary because the microprocessor can receive signals only in voltage form. The voltage which is proportional to the current signal is converted into direct voltage using precision rectifier. This rectified current is fed to the Analoge/Digital (A/D) converter. Then the microprocessor sends a signal to the A/D converter for starting the conversion. The microprocessor examines whether the conversion is over or not. As soon as the conversion is over the A/D converter sends a signal to the microprocessor. After receiving the end of conversion signal the microprocessor read the current signal in digital form and examines whether it is more than the pick up value . If the current exceeds the pick up value the microprocessor sends the tripping signal to the circuit breaker depending upon the value of current. The Fig. 22 shows the proposed scheme.

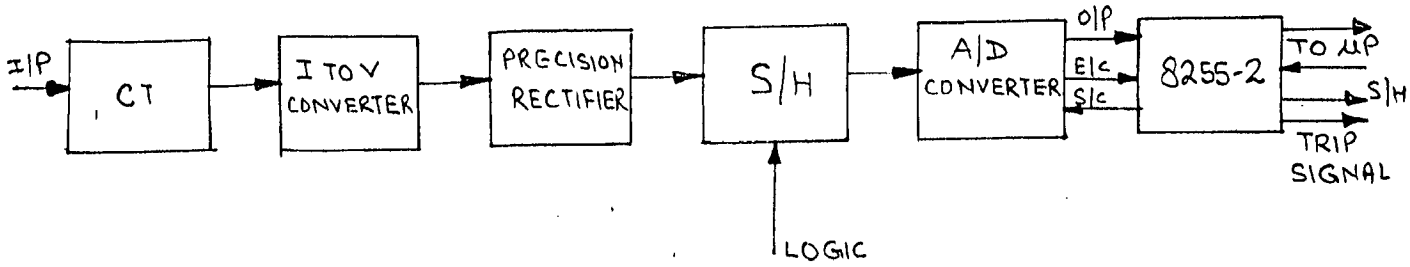


FIG. 22

Detailed proposed scheme is shown in Fig. 23

3.1 Current Transformers[2,4]

Protection is concerned with fault current in various system components with their detection and measurement. This measurement would be dangerous and expensive to achieve if the actual load and fault currents, often very large, and at a very high voltage had to be taken through the measuring relays. A practical way of overcoming these difficulties is to use current transformers. These make available on their secondary sides currents of manageable proportions which are replicas of the current in the primary windings which carry the actual power system current (normal and fault).

The construction of current transformers in general follows the pattern of having a core of ferrous material

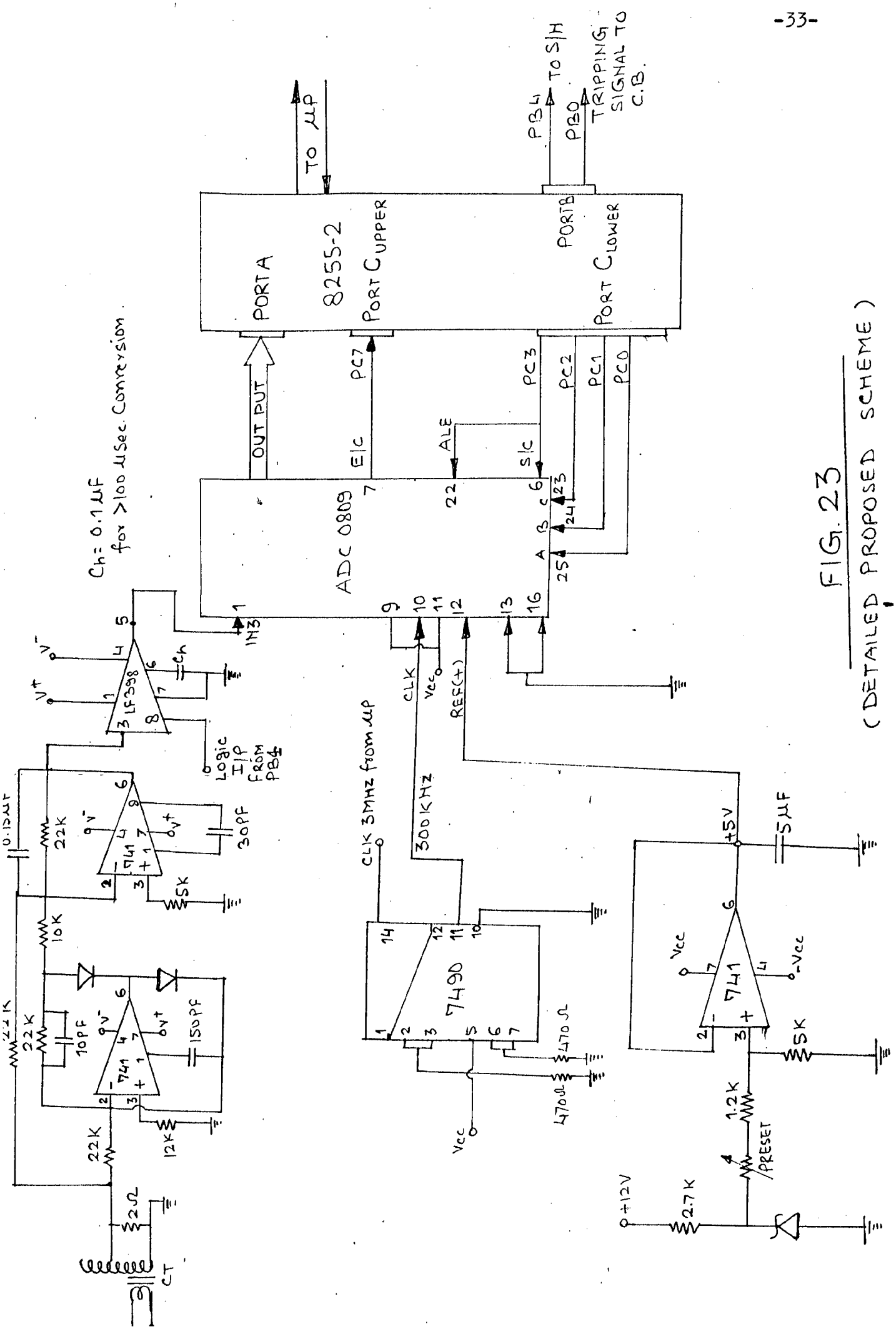


FIG. 23
(DETAILED PROPOSED SCHEME)

which is magnetised by the current in the primary winding insulation appropriate for the system voltage is used between primary winding and core and secondary winding inducing a current in a secondary winding with an appropriate number of turns. The primary winding of C.T. is connected in series with the load and carries the actual power system current whether it is normal or fault current. The secondary is connected to the relay which together with the winding impedance of the transformer and the load resistance constitutes the burden of the transformer. Current transformers for protection are essentially similar to those used for the operation of ammeters, watt-hourmeters and other instrument. In the interests of standardisation nearly all such transformers are designed for a rated secondary current of either 5 A or 1 A, thus enabling standard, relays to be matched to any power system.

The current transformer is similar in operation to any other transformer so that the primary current consists of two components, i.e. the secondary current which is transformed in the inverse ratio of the turns ratio and the exciting current which magnetizes the core, The later current is not transformed and is the cause of transformer errors. It is because of this

reason that certain values of secondary current could never be produced, whatever the value of primary current. This happens when the core saturates and disproportionate amount of primary current is required to magnetize the core.

Fig. 24 shows the general shape of a CT magnetization curve[4]. The shape will change for different core materials. The characteristic is divided into three regions defined by the ankle point and the knee point. The boundary between the saturated and unsaturated regions is marked by the knee point which is defined as the point at which a 10% increase in secondary voltage produces a 50% increase in exciting current. The other characteristic curve shown in fig. 24 is the phase angle of exciting current which is not of much importance for protection C.T's. It may however, be noted that the working range of a protective CT extends over the full range between the ankle and the knee points and keyond where as the measuring CT usually operates in the region of the ankle point. Measuring CT's require comparatively high accuracy over the range of 10% to 120% rated current and it is an advantage if the CT's saturate for currents above this range in order to protect the instruments. Protection CT's require linear characteristic upto the secondary voltage corresponding to maximum fault current flowing in the connected burden.

Fig. 25 shows the characteristics of two CTs both for the same rated burden, but one for protection and the other for measurement. It is quite obvious that a core of large cross-section would be required for a protective CT is the material has to be the

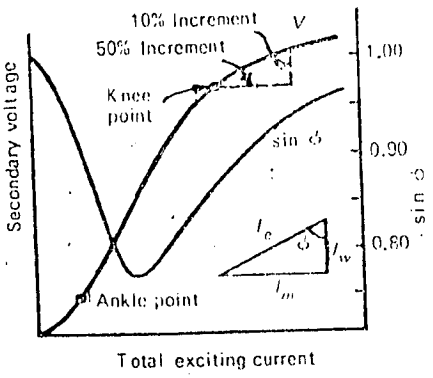


FIG. 24

CURRENT TRANSFORMER MAGNETIZING CHARACTERISTICS

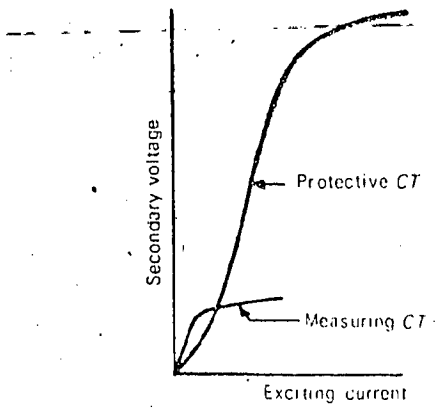


FIG. 25

PROTECTIVE AND MEASURING CT's.

same. Grain oriented steels having high saturation levels are used as core materials for protective CT's and Ni-Fe alloys having low exciting ampere-turns per unit length of the core are used for measuring CTs and the knee point occurs at a relatively low flux density.

3.1.1 Basic Transformer Principles[2]

A transformer, consisting of a core of magnetic material on which are wound two windings, can be operated in two basic modes, shunt and series. In power and voltage operation it is used in shunt mode. In the series mode, that is, in current operation, the primary winding is connected in series with the power system whose relatively high impedance determines the magnitude of the primary current, and a component of this current excites the core to the flux density necessary to induce in the secondary winding an e.m.f. sufficient to drive the secondary current through the total impedance of the secondary-circuit.

In current transformers, the core flux density is dependent on the magnitude of the primary current and the impedance of the secondary circuit.

Fig. 26 shows a simplified equivalent circuit for a two winding transformer of 1/1 turns ratio, the leakage inductances having been omitted. In current operation we are interested in relationship between the primary current I_p and the secondary current I_s, not in magnitude and phase differences between the

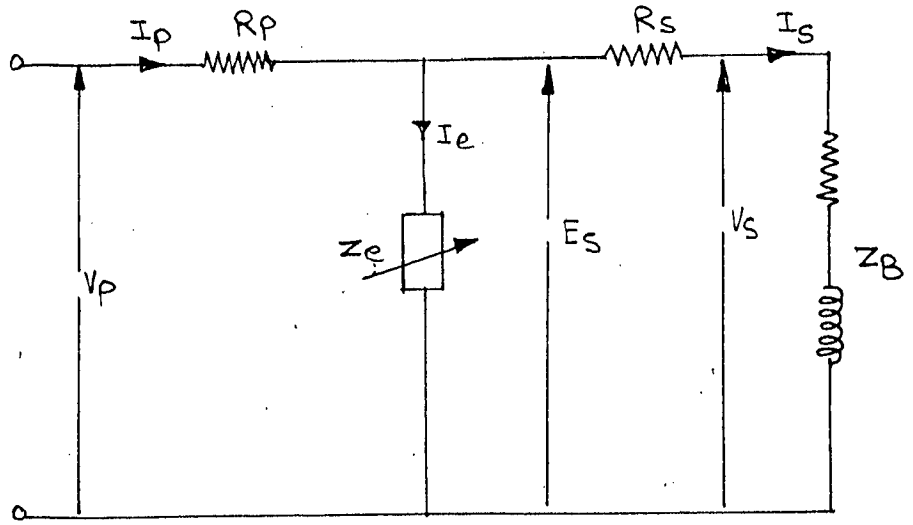


FIG.26

EQUIVALENT CIRCUIT FOR A TRANSFORMER OF 1|1 TURNS RATIO AND NEGLIGIBLE LEAKAGE FLUX

primary and secondary voltages V_p and V_s causes by I_p and I_s. It will be noted that these currents differ by the amount of the core exciting current I_e which is, of course, a component of I_p.

3.2 Precision Rectifier[3]

Fig. 27 shows a precision-rectifier using operational amplifiers. In ordinary bridge rectifier there is a voltage drop in the diodes. Thus the output of the rectifier is not exactly proportional to the input signal. A precision rectifier using IC packages 741 is very accurate in this respect.

3.3 A/D Converter[3,23]

IC package 0809 data acquisition component is a monolithic CMOS device with an 8-bit analog to digital converter 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance

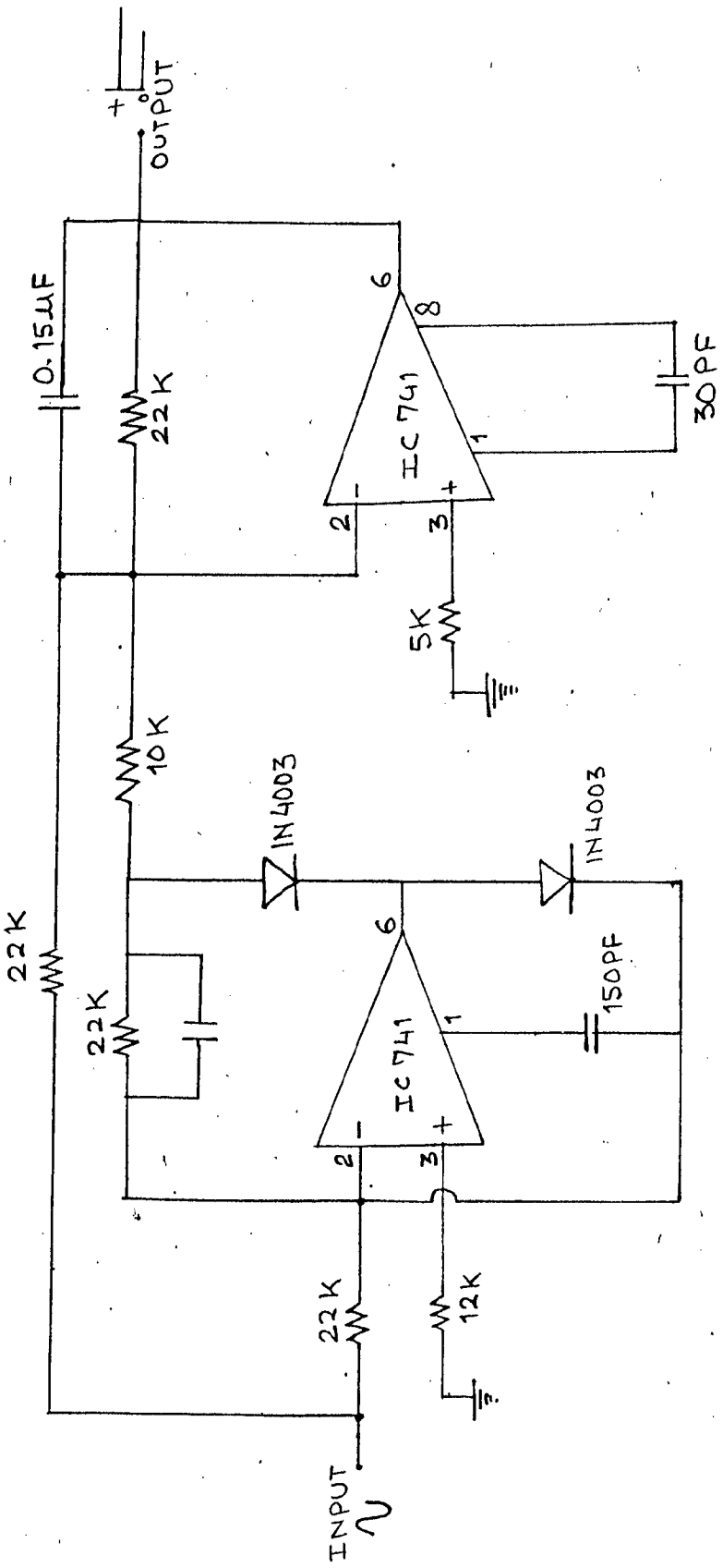


FIG. 27

PRECISION RECTIFIER

chopper stabilized comparator, a 256 R voltage divider with analog switchtree and successive approximation register. The 8-channel multiplexer can directly access any of 8, single ended analog signals. The device eliminates the need for external zero and full scale adjustments. Easy interfacing is provided by the latched and decoded multiplexer address inputs and latched TTL TRI state. outputs, The design of ADC 0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC 0809 offers high speed, high accuracy, minimal temp. dependence, excellent long term accuracy and repeatability and consume minimal power. These features make this device ideally suited to applications from process and m/c control to consumer and automotive applications. Fig. 28 and 29 shows schematic Diagram of ADC 0809 and timing diagram of 0809 respectively. Some important characteristics of A/D converter 0809 are as follows:

Min. start pulse width	=	100 ns
Min. ALE pulse width	=	100 ns
Clock frequency	=	10 to 1280 KHz
Conversion time	=	100 uS at 640 KHz
Resolution	=	8-bits
Error	=	$\pm$ 1 LSB

Ref (+) should not be more positive than supply

Ref (-) should not be more negative than ground

Single supply	=	5 V d.c.
Low power consumption	=	15 mW
Temp. range	=	$-40^{\circ}C$ to $+85^{\circ}C$

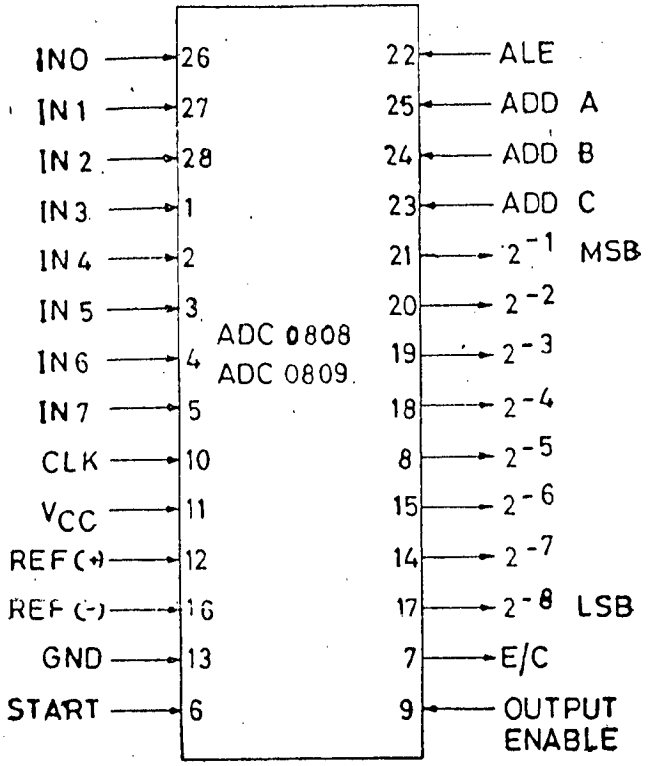


FIG. 28

SCHEMATIC DIAGRAM OF ADC 0808/0809

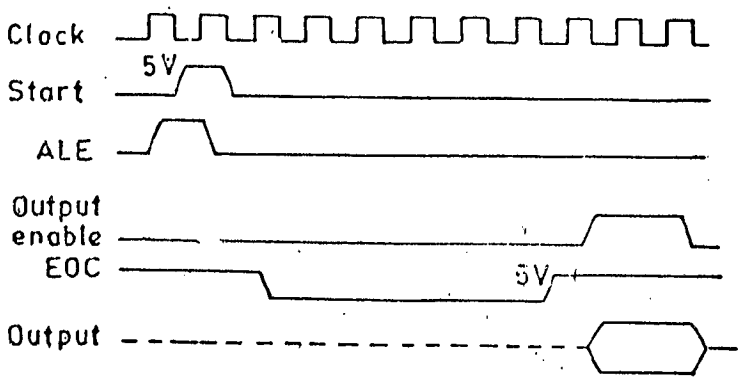


FIG. 29

TIMING DIAGRAM OF ADC 0809

3.4 Sample and Hold Circuit[3]

The signal that is fed to an A/D converter should be maintained constant during the conversion period. In case of an a.c. signal, its instantaneous value is applied to A/D converter and converted into digital quantity. A sample and hold circuit samples the instantaneous value of a.c. signal and maintains it at a constant level. It makes available this constant voltage for A/D converter which require a constant input during the conversion period.

LF.398: LF 198/LF 298/LF 398 are monolithic sample and hold circuits of national semiconductor. They utilise BI-FFT technology to obtain high accuracy, fast aquisition of signal and low droop rate. In the output amplifier P-channel junction FFTs are combined with bipolar devices to give very low droop rate. The droop rate is the rate at which the output of S/H circuit decreases. To make the output practically constant this rate should be very small. An external capacitor known as hold capacitor is used with LF 398 or any other S/H circuit to hold the voltage impressed upon it.

A droop rate as low as 5 mV/min. is obtained with a 1 μF hold capacitor. Fig. 30 shows the schematic diagram of LF 398. C_h is the hold capacitor which is to be selected by the user. From the graph shown in fig. 31 the aquisition time corresponding to the value of the hold capacitor is determined. When the logic becomes high the input voltage is applied to the hold capacitor

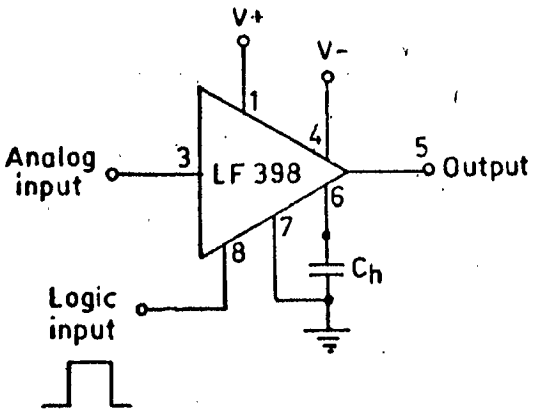


FIG. 30
SCHEMATIC DIAGRAM OF LF 398

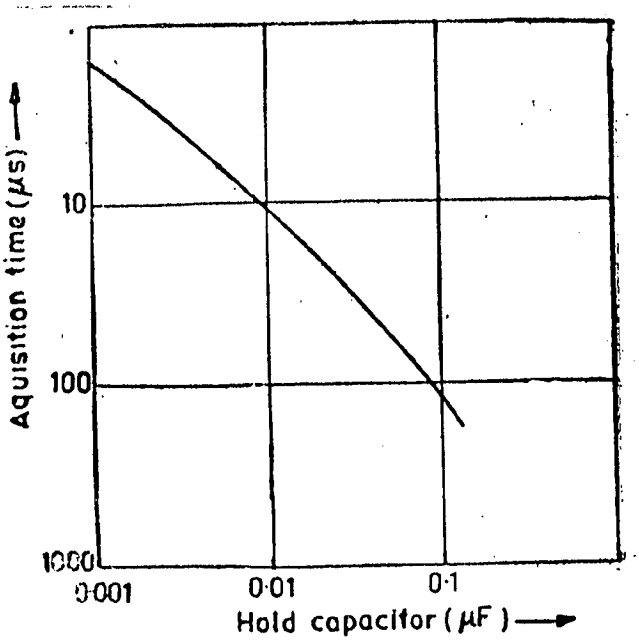


FIG. 31
AQUISITION TIME FOR LF 398

and it is charged to the instantaneous value of the input voltage. The input voltage is switched off when the logic goes low. The hold capacitor is isolated from any load through op-amp. incorporated in S/H circuit for this very purpose. Thus the hold capacitor holds the instantaneous value of the input voltage impressed upon it. LF-398 operates at supply voltage ±5 V to ±18 V d.c.

3.4.1 Aquisition Time

The aquisition time is the time taken by S/H circuit for the capacitor to change from one level of holding voltage to the new value of input voltage after the input voltage is applied to the hold capacitor.

3.4.2 Aperture Time

The aperture time is the delay between the hold command and the moment at which the input voltage is applied to the hold capacitor. It is of the order of nano seconds.

3.4.3 Selection of the Hold Capacitor

The hold capacitors should be made of dielectrics having low hysterisis such as polysterene, polypropylone and teflon. The aquisition time depends on the value of hold capacitor for example for 0.047 μF the aquisition time is 40 μ sec.

3.5 Clock[3]

The clock frequency required for A/D converter lies in the range of 50 KHz to 800 KHz for ADC 0800 and 10 KHz for ADC 0808

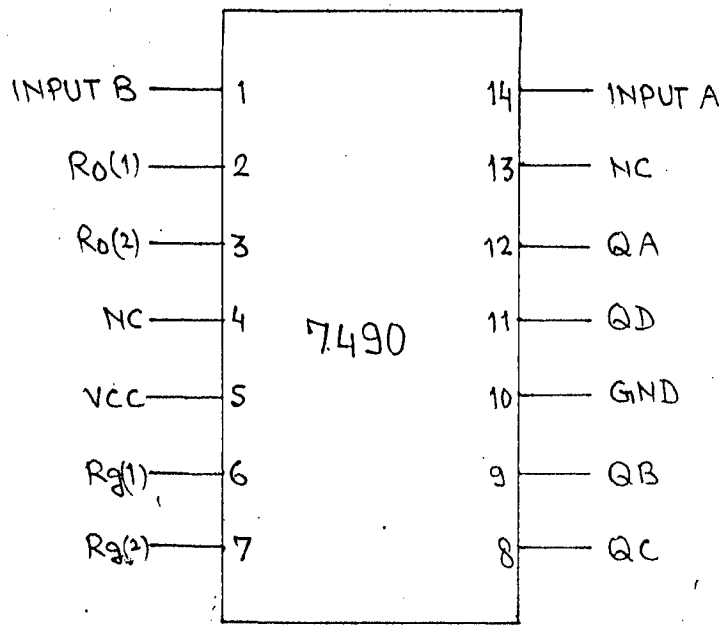


FIG. 32
PIN DIAGRAM OF 7490

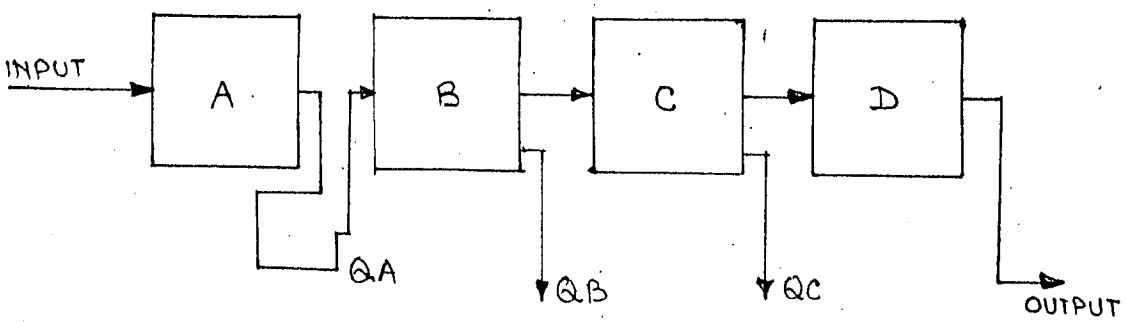


FIG. 33
CONNECTION DIAGRAM FOR 7490

to 1280 KHz for ADC 0808, ADC 0809, ADC 0816 and ADC 0817. The clock frequency for users is about 3 MHz. In some kits 1.5 MHz is also available. This can be reduced to a suitable value using IC package 7490 to get a clock for A/D converter. IC 7490 is a monolithic decade counter. Pin diagram of IC 7490 has shown in Fig. 32 and connected diagram in Fig. 33.

It contains 4 master-slave flip flops. The unit A divide the frequency by 2. If the output is taken at QA the frequency will be half of the input frequency. The unit B, C and D combined together divide by 5. If the input is at B and output is taken at QD the frequency will be reduced 5 times. If all four units are connected as shown in Fig. 33 the frequency will be reduced 10 times.

CHAPTER - 4

4. INTERFACING OF A/D 0809[3]

Fig. 34 shows interfacing of ADC 0809 to Intel 8085 microprocessor. An analog input is connected to IN3 i.e. Pin No. 1 of 0809. 5V d.c. applied to Pin No. 12 of ADC 0809 i.e. Ref. (+) should be very accurate. It should not be given from stabilised power units which are generally available in the laboratory. A circuit shown in Fig. 36 should be developed to obtain 5V d.c. (V_{ref}). This 5V d.c. (V_{ref}) should be connected to Pin No. 12. Pin No. 9 is for output enable and may be connected with Pin No. 11 of V_{cc} and this may be connected to 5V d.c. supply of the stabilised supply unit available in the laboratory. A clock from IC 7490 is applied to Pin No. 10 of ADC 0809. Pin No. 23, 24, 25 are connected to port C-lower of 8085 microprocessor. Pin No. 6 and 22 shorted and connected with PC3. Pin No. 7 for E/C is connected with PC 7, port C upper, of 8085 microprocessor. Output of 0809 is connected to port 'A', Logic to LF 398 at Pin No. 8 is given from PB_4. For output tripping command to the circuit breaker the PB_0 has been used.

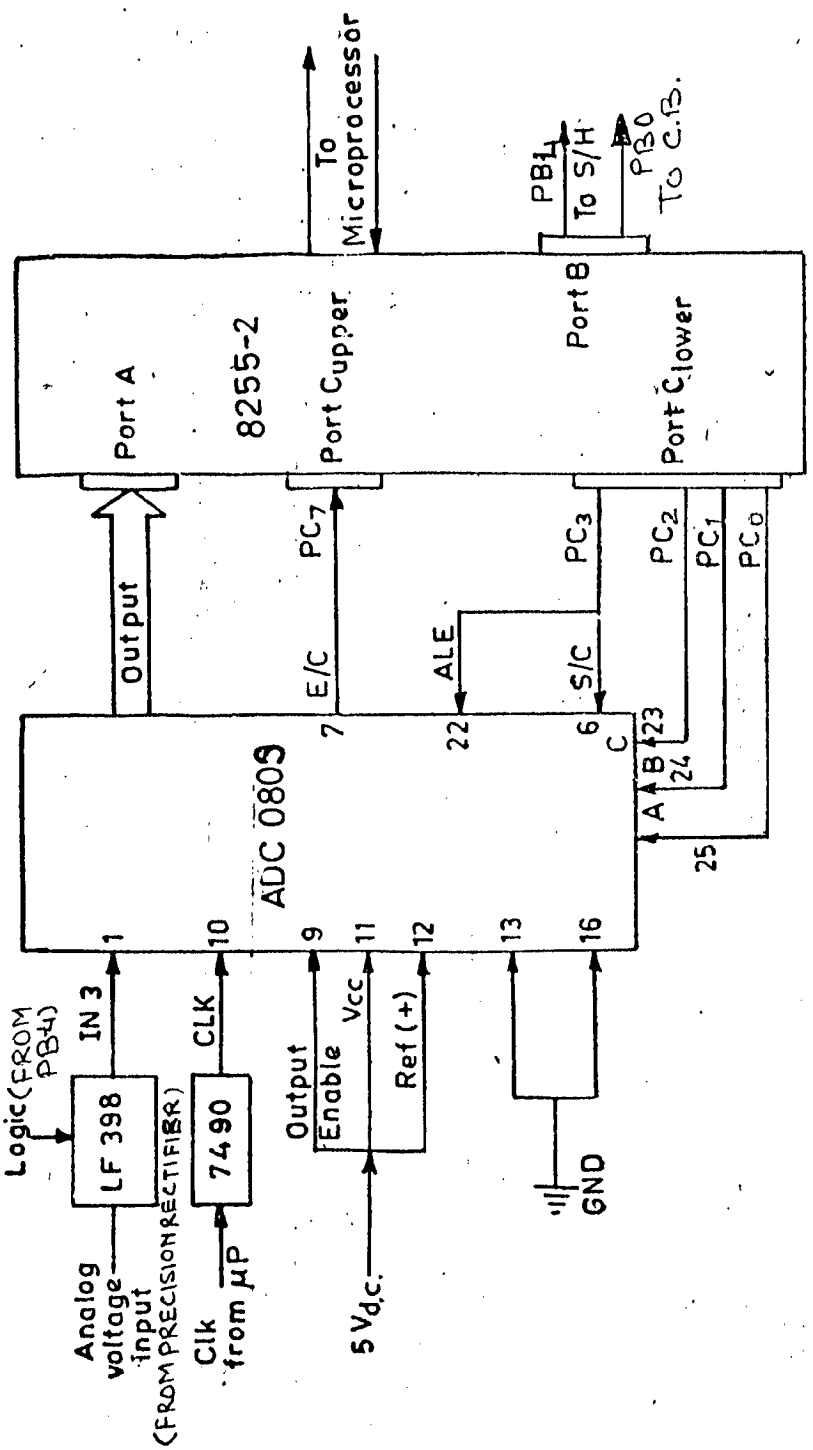


FIG. 34

INTERFACING OF ADC 0809 AND LF 398 WITH INTEL 8085

CHAPTER - 5

5. DESIGN FEATURES

In this chapter design, feature of current transformer, precision rectifier, and V_{ref}. has been carried out.

5.1 Current Transformer

There are some design features which help to minimize the errors in current transformer.

5.1.1 Design Features[22] Core

In order to minimize the errors the magnetizing current I_m and loss component I_e must be kept to a low value. This means that the core must have a low reluctance and a low core loss. The reduction of reluctance of flux path can be brought about by using materials of high permeability, short magnetic paths, large cross section of core and a low value of flux density. The C.T's are designed for much lower flux densities than that for power transformers. This is especially important for C.T. used for protective relays which are frequently required to have a fair accuracy at currents many times the rated current, in order that the relay operation may be correct in the event of a short circuit on the

system. The number of joints in building up cores should be minimum is far as possible because joints produce air gaps which offer path of high reluctance. The mmf consumed by joints can be reduced by properly lapping the joints and tightly binding the core. The core loss is reduced by choosing materials having low hystersis and low eddy current losses, and by working the core at low flux densities.

Present-day magnetic materials used in CT are divided into three categories:

i) Hot rolled silicon steel
ii) Cold rolled grain oriented silicon steel
iii) Ni-Fe alloys

In CT practice hot rolled silicon steels (4% silicon) are used in a variety of forms. For ring type CT ring stampings are used. For wound type, T-V, L or E and I stampdings are used. An alternative method employes cores that are made of strip wound in spiral form like a clock spring. These are called toroidal cores.

The later method is much to be preferred when grain oriented magnetic materials are being as it ensures that the flux path is along the grains and hence there is minimum reluctance. Another advantage of spiral type of cores is that the joints are entirely eliminated.

5.1.2 Leakage Reactance

Leakage reactance tends to increase ratio error. Therefore, the two windings, primary and secondary should be close together

to reduce the secondary leakage reactance. Use of ring shaped cores arround which toroidal windings are uniformly distributed also leads to low leakage reactance.

5.1.3 Turns Compensation

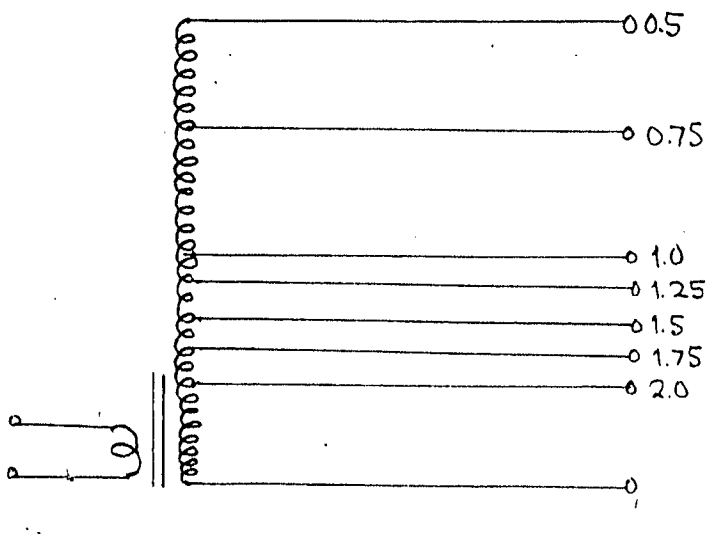
Actual transformation ratio,

$$R = n + \frac{I_e}{I_s}$$

Thus if we make the nominal ratio equal to the turns ratio the actual transformation ratio becomes more than the nominal ratio.

How if we reduce the turns ratio and keep the nominal ratio equal to the earlier value, the actual transformation ratio will be reduced. This would make actual transformation ratio nearly equal to the nominal ratio.

Here we are using toroidal core of diameter (inner) 5 cm. and outer diameter 10 cm. with 2 turns of 14 SWG wire on primary side and 96 turns on secondary side. Tappings at the secondary has been provided at turn no. 24, 30, 36, 42, 48 and 68 turns to work as PSM 2.0, 1.75, 1.5, 1.25, 1.0, 0.75 respectively and 0.5 at 96 turns.



In lab. we assumed the fault current 50 Amp. which will be flowing through primary. Then current flowing through secondary of CT will be

$$\frac{N_1}{N_2} = \frac{I_2}{I_1}$$

$$I_2 = I_1 \times \frac{N_1}{N_2}$$

$$= 50 \times \frac{2}{96} = 1.04 \text{ A}$$

In normal condition the 5 Amp. current would be flowing through the C.T. primary. In this case the secondary current would be

$$I_2 = \frac{5 \times 2}{96} = 0.104 \text{ A}$$

5.2 Design of a Precision Rectifier[13]

In the fig. 35, section A works as a precision rectifier and section B as a low pass filter.

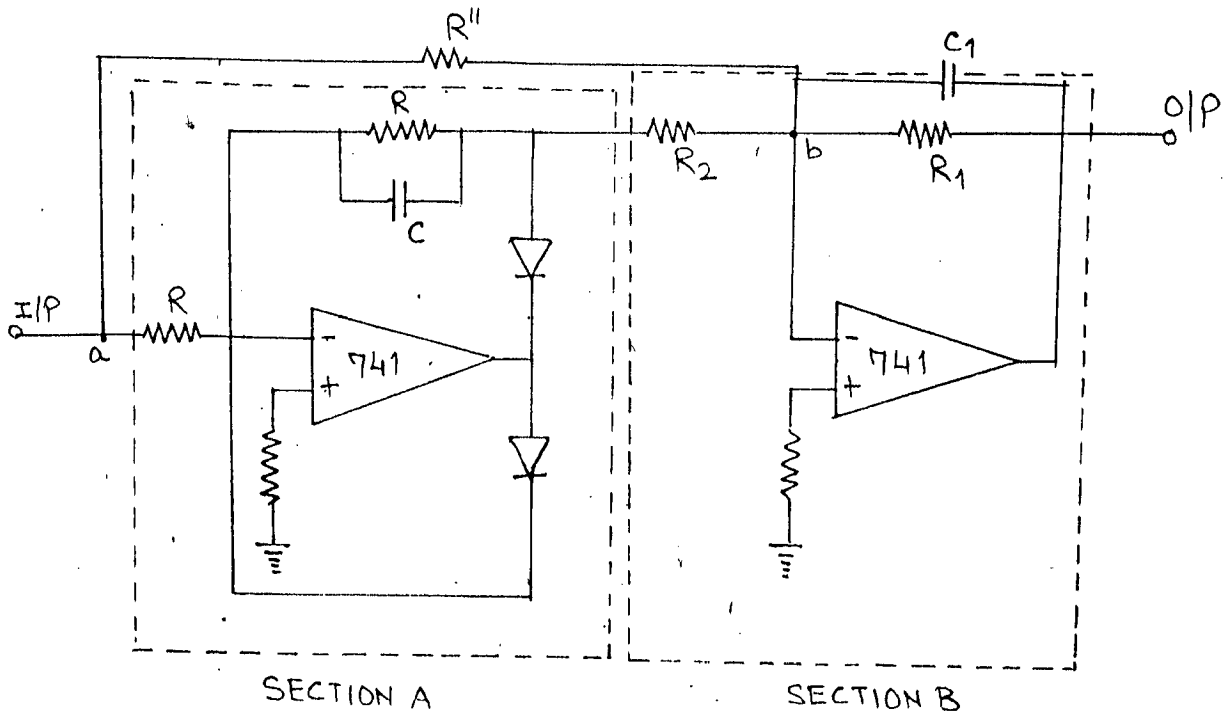


FIG. 35

In section A, the capacitor C work as a speed up capacitor, means any fast change in input signal the speed up capacitor will immediately give it is the output therefore speeding up the process, which may be keft of pF range. Section A may be seen as in the following fig. 35.1.

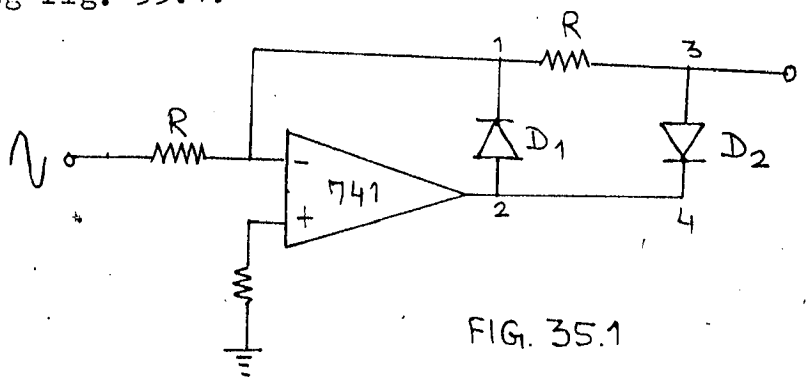


FIG. 35.1

When positive half cycle is applied at input, output will be negative then point no. 1 and 2 are open and diode D_1 cut off and diode D_2 becomes forward bias. So point no. 3 and 4 are short circuited. In this case the circuit becomes as in fig. 35.2.

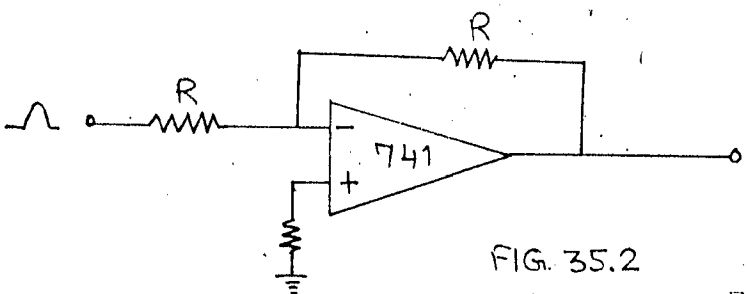
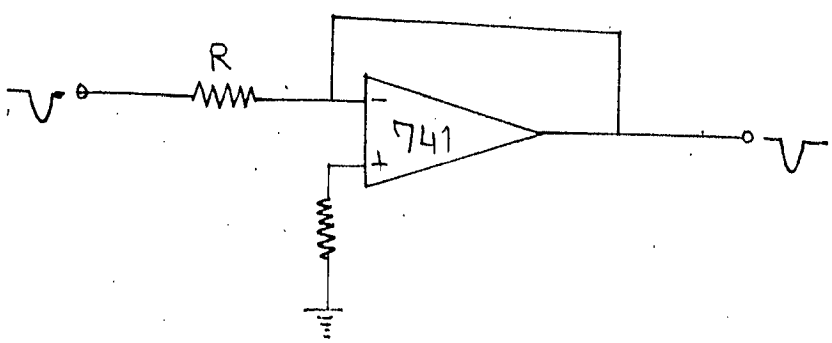


FIG. 35.2

So the output is inverted 1/2 cycle. For input of negative 1/2 cycle the point 2 is more positive than 1 in fig.35.1hence diode D_1 is forward biased and diode D_2 open. Now in this case the circuit becomes as shown in Fig. 35.3 and it is simply a voltage follower.



Here we see that for a complete one cycle at input the output is ~ in this form.

The above output is fed into the section B which is simply a integrater/low pass filter circuit. The value of R in the above circuit is kept between 10 K ohm and 50 K ohm because if we go above 50 K ohm, it may be above internal impedance of Op-amp. If R is below 10 K ohm it may load the source., Here we have selected the resistance R = 22 K ohm for the uniformity as the value of resistance is comes out to be 22 K ohm in low pass filter circuit. Resistance R" is to reduce the effect of noise or other frequences which are not required and its value is choosen 22 K ohm as the same current will be flowing in this as in the R'.

5.2.1 Low Pass Filter/Integrator Circuit

Section B of Fig. 35 works as an integrator/Low pass filter Fig. 35.4 shows the integrator circuit.

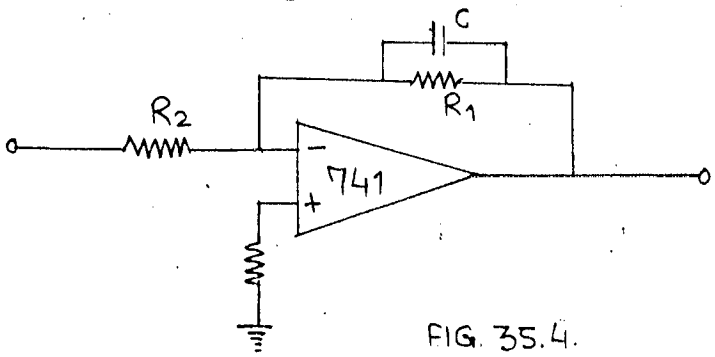


FIG. 35.4.

Low Pass Filter : Fig. 35.5 shows an active low pass filter. At low frequencies the capacitor appears open, and the circuits

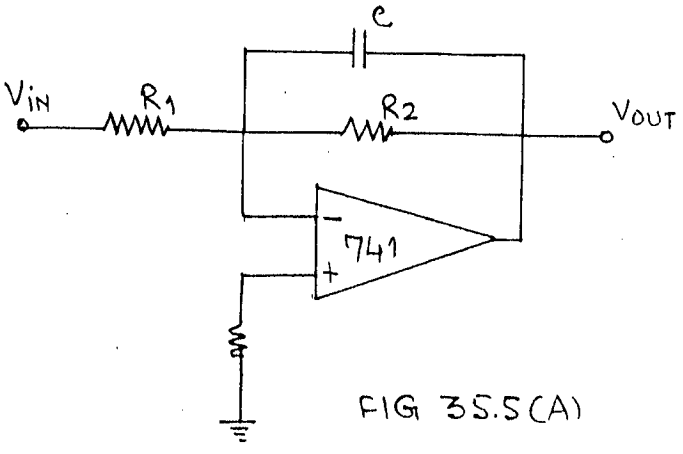
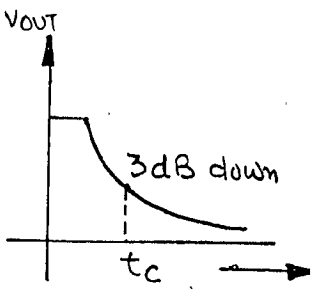


FIG 35.5(A)



OUTPUT RESPONSE

FIG. 35.5 (B)

acts like an inverting amplifier with a voltage gain of $-R_2/R_1$. As the frequency increases, the capacitive reactance decreases, causing the voltage gain to drop off. As the frequency approaches infinity, the capacitor appears shorted and voltage gain approaches zero.

In Fig. 35.5(B) the O/P signal is maximum at low frequencies when the frequency reaches the critical or cut off frequency. The O/P is down 3dB. Beyond this frequency the gain rolls off at an ideal rate of 20dB/decade or 6dB/octave.

$$V_{in} = I_{in} Z_1$$

$$V_{out} = -I_{in} Z_2$$

$$\text{Voltage gain } \frac{V_{out}}{V_{in}} = -\frac{Z_2}{Z_1}$$

where (-) sign stands for phase inversion. The complex admittance of the feedback network is

$$Y_2 = \frac{1}{R_2} + j\omega C = \frac{1 + j\omega R_2 C}{R_2}$$

$$Z_2 = \frac{R_2}{1 + j\omega R_2 C}$$

$$\text{Ratio of Impedance } \frac{Z_2}{Z_1} = \frac{R_2}{R_1(1+j\omega R_2 C)}$$

$$\text{So, magnitude is } = \frac{R_2}{R_1} \cdot \frac{1}{\sqrt{1 + (\omega R_2 C)^2}}$$

The 3dB corner frequency occurs when

$$\omega R_2 C = 1$$

$$f_c = \frac{1}{2\pi R_2 C}$$

If C is 0.15 μF then R_2 = 21.22 K ohm $\cong$ 22 K ohm

Low frequency gain $A = \frac{R_2}{R_1}$

for gain of 2, $R_1 = \frac{R_2}{2} = \frac{22}{2}$ = 11 k ohm

5.3 Design of Voltage Regulator[13]

The simple zener diode regulator is designed to minimize the effects of supply voltage fluctuation and load current variation on the load voltage. By using a high gain amplifier much better regulation can be obtained.

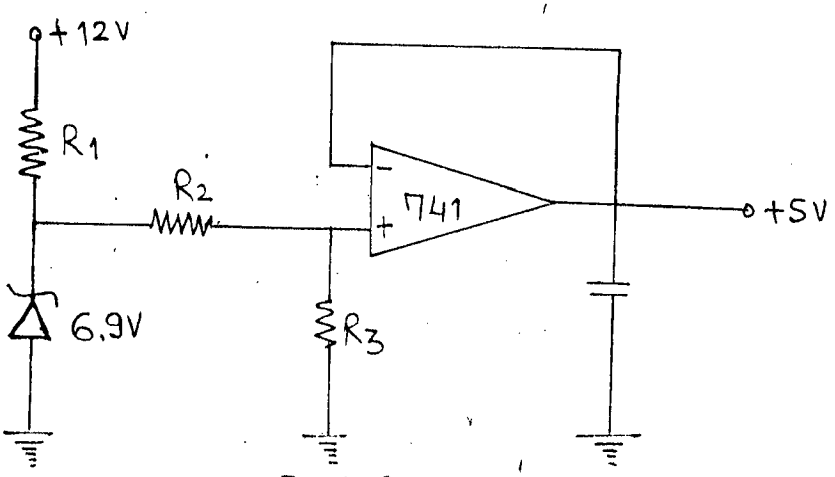


FIG.36

Maximum 2 mA can flow through zener, so the value of R_1 should be such that in any case the current flowing through the zener could not be more than 2 mA. If we choose, R_1 = 2.7 K ohm, the current will be = $\frac{5.1\ V}{2.7K\ ohm}$ = 1.88 mA

For zener diode to be in break down region, the 1 mA current

should flow through zener. So, now; the circuit becomes as

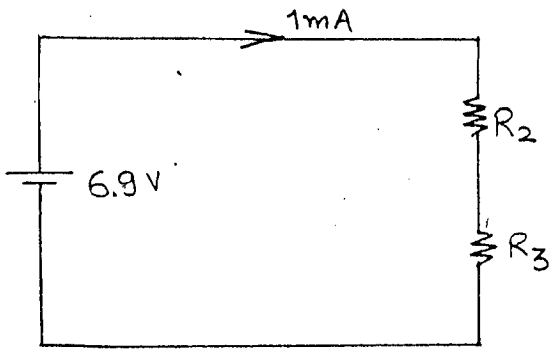


FIG. 36.1

i.e. $R_2 + R_3 = 6.9$ K ohm

The best combination is 1.9 K ohm + 5 K ohm i.e. $R_3 = 5$ K ohm

For $R_2 = 1.9$ K ohm, it may be kept as 1.2 K ohm in series with the preset of 1 K ohm.

CHAPTER - 6

6. OBSERVATIONS TAKEN IN THE LABORATORY

48 turns of secondary side of current transformer were used for PSM = 1 and following voltages were measured across a 2 ohm resistance.

TABLE - 1

Current (In Amp.)	Voltage (In Volts.)
1.0	0.084
2.0	0.175
3.0	0.24
4.0	0.3
5.0	0.4
6.0	0.49
7.0	0.57
8.0	0.67
9.0	0.76
10.0	0.85
12.0	1.04
14.0	1.21

16.0	1.44
18.0	1.60
20.0	1.68

The above voltage were rectified with the help of precision rectifier and analog signals were converted into digital form with the help of A/D converter IC 0809 by using following microprocessor programme 6.1.

6.1

Address	M/c Codes	Mnemonics	
2000	3E, 98	MVI A, 98H	Control word
2	D3, 03	OUT 03	
4	3E, 10	MVI A, 10	Logic 1 to LF 398
6	D3, 01	OUT 01	
8	3E, 01	MVI A, 01	IN 3 Channel $PC_0 = 1$ $PC_1 = 1$ $PC_2 = 0$
200 A	D3, 03	OUT 03	
C	3E, 03	MVI A, 03	
E	D3, 03	OUT 03	
10	3E, 04	MVI A, 04	
2012	D3, 03	OUT 03	
14	3E, 06	MVI A, 06	PC_3 low
16	D3, 03	OUT 03	
18	3C	INR A	PC_3 high
19	D3, 03	OUT 03	
1B	3D	DCR A	PC_3 low
1C	D3, 03	OUT 03	
201E	DB, 02	IN 02	E.O.C.check
20	E6 80	ANI 80	
22	CA.1E 20	JZ 201E	

Address	M/c Code	Mnemonics	
25	DB, 00	IN 00	Data IN
27	32 F6 27	STA 27 F6	For continuous Display
202A	CD FA 06	CALL Display	
2D	11, 22, 01	LXI D 0122	
30	CD BC 03	CALL Display	
33	C3 00 20	JMP 2000	

By using above programme following values were displayed at microprocessor for different value of current.

TABLE - 2

Current(In Amp)	Display (In Hex.)
0.0	00
1.0	03
1.3	05
2.0	08
2.5	0A
3.0	0D
3.5	0F
4.0	11
4.5	14
5.0	16
5.5	19
6.0	1B
7.0	20
8.0	24
9.0	29
10.0	2E
11.0	33
12.0	38
13.0	3E
14.0	43
15.0	48

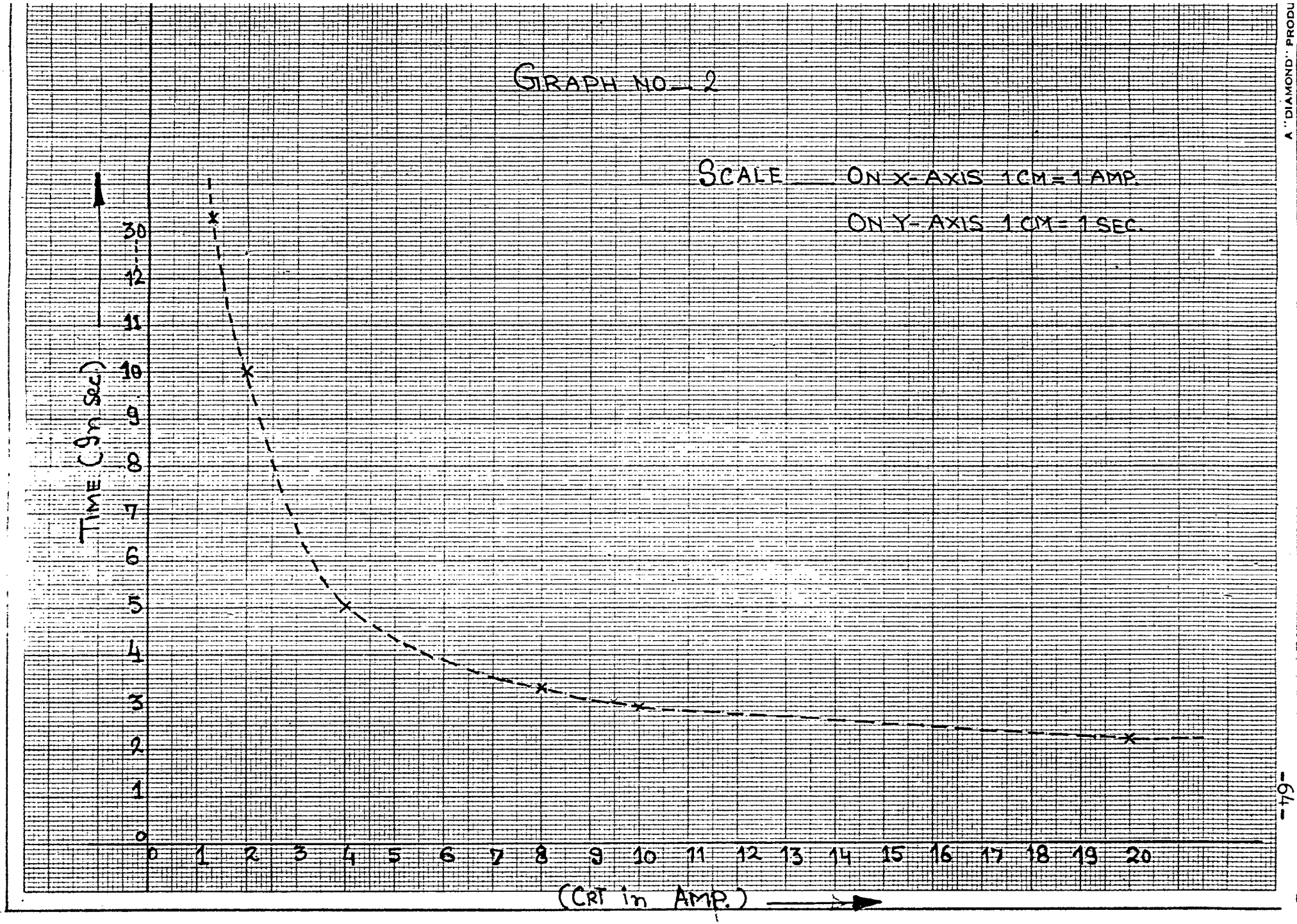
Current (In Amp.)	Display (In Hex.)
16.0	4D
17.0	52
18.0	57
19.0	5C
20.0	61
21.0	66

The above displayed value were plotted against the current in graph no. 1 to get the corresponding value of current for each bit. Following table shows the corresponding value of current at each bit step from the graph no. 1.

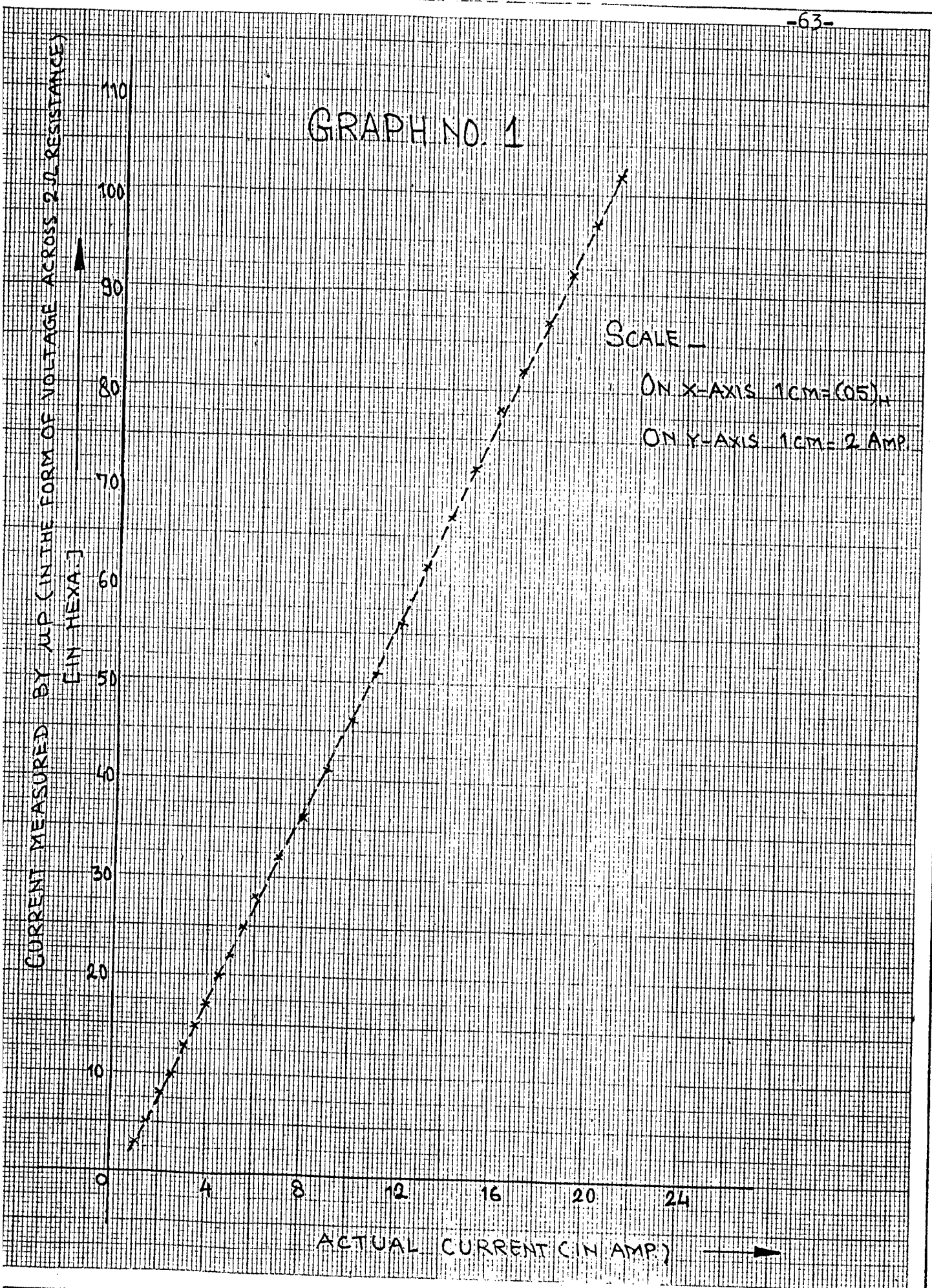
TABLE - 3

01	0.6 Amp	14	4.5 A
02	0.8 A	15	4.7 A
03	1.0 A	16	5.0 A
04	1.2 A	17	5.1 A
05	1.3 A	18	5.3 A
06	1.6 A	19	5.5 A
07	1.8 A	1A	5.7 A
08	2.0 A	1B	6.0 A
09	2.2 A	1C	6.2 A
0A	2.5 A	1D	6.4 A
0B	2.6 A	1E	6.6 A
0C	2.8 A	1F	6.8 A
0D	3.0 A	20	7.0 A
0E	3.3 A	21	7.2 A
0F	3.5 A	22	7.4 A
10	3.7 A	23	7.6 A
11	4.0 A	24	8.0 A
12	4.1 A	25	8.2 A
13	4.3 A	26	8.4 A

27	8.6 A	4A	15.4 A
28	8.8 A	4B	15.6 A
29	9.0 A	4C	15.8 A
2A	9.2 A	4D	16.0 A
2B	9.4 A	4E	16.2 A
2C	9.6 A	4F	16.4 A
2D	9.8 A	50	16.6 A
2E	10.0 A	51	16.8 A
2F	10.2 A	52	17.0 A
30	10.4 A	53	17.2 A
31	10.6 A	54	17.4 A
32	10.8 A	55	17.6 A
33	11.0 A	56	17.8 A
34	11.2 A	57	18.0 A
35	11.4 A	58	18.2 A
36	11.6 A	59	18.4 A
37	11.8 A	5A	18.6 A
38	12.0 A	5B	18.8 A
39	12.2 A	5C	19.0 A
3A	12.3 A	5D	19.2 A
3B	12.4 A	5E	19.4 A
3C	12.6 A	5F	19.6 A
3D	12.8 A	60	19.8 A
3E	13.0 A	61	20.0 A
3F	12.2 A	62	20.2 A
40	13.4 A	63	20.4 A
41	13.6 A	64	20.6 A
42	13.8 A	65	20.8 A
43	14.0 A	66	21.0 A
44.	14.2 A		
45	14.4 A		
46	14.6 A		
47	14.8 A		
48	15.0 A		
49	15.2 A		



GRAPH NO. 1


CURRENT MEASURED BY JUP (IN THE FORM OF VOLTAGE ACROSS 2Ω RESISTANCE) (IN HEXA.)
110
100
90
80
70
60
50
40
30
20
10
0
4
8
12
16
20
24
ACTUAL CURRENT (IN AMP.)
SCALE –
ON X-AXIS 1 CM = (05)H
ON Y-AXIS 1 CM = 2 AMP.

For above values of the current, the corresponding time was taken from the standard IDMT curve (Graph No. 2). This time is converted into milisecond and its Hexa values were stored at address 2200 in microprocessor. Following table shows the Hexa-values of time to the corresponding current.

TABLE - 4

Address	Current in (Hexa)	Current (In Amp.)	Corresponding Time from Graph No.2(x 1000)	Hexa Value of time
2200	01	0.6 Amp.	33 sec.	80E8
	02	0.8 A	33 sec.	80E8
	03	1.0 A	33 sec.	80E8
	04	1.2 A	33 sec.	80E8
	05	1.3 A	33 sec.	80E8
	06	1.6 A	11.3 sec.	2C24
	07	1.8 A	10.5 sec.	2904
	08	2.0 A	10.0 Sec.	2710
	09	2.2 A	9.1 sec.	238C
	0A	2.5 A	8.0 sec.	1F40
	0B	2.6 A	7.6 sec.	1DB0
	0C	2.8 A	7.2 sec.	1C20
	0D	3.0 A	6.7 sec.	1A2C
	0E	3.3 A	6.1 sec.	17D4
	0F	3.5 A	5.7 sec.	1644
	10	3.7 A	5.4 sec.	1518
	11	4.0 A	5.0 sec.	1388
	12	4.1 A	4.85sec.	12F2
	13	4.3 A	4.8 sec.	12C0
	14	4.5 A	4.7 sec.	125C
	15	4.7 A	4.5 sec.	1194
	16	5.0 A	4.35sec.	10FE
	17	5.1 A	4.3 sec.	10CC

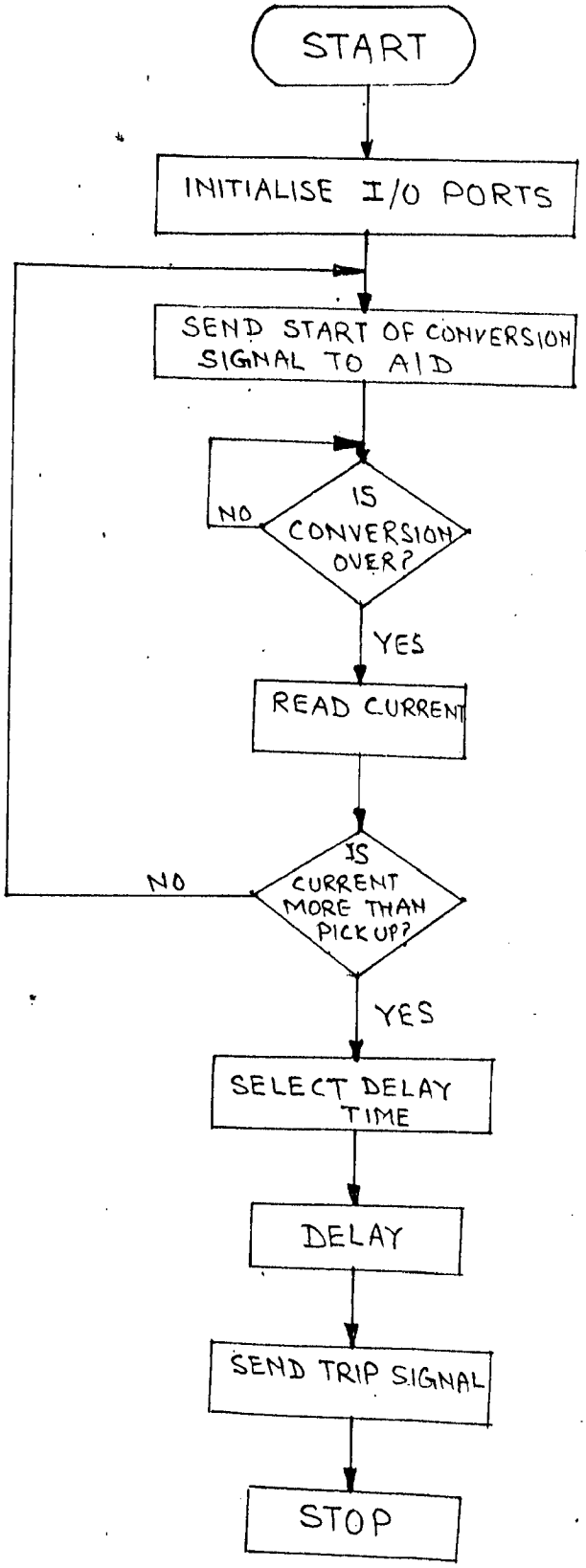
18	5.3 A	4.2 sec.	1068
19	5.5 A	4.1 sec.	1004
1A	5.7 A	4.0 sec.	0FA0
1B	6.0 A	3.9 sec.	0F3C
1C	6.2 A	3.8 sec.	0ED8
1D	6.4 A	3.75 sec.	0EA6
1E	6.6 A	3.65 sec.	0E42
1F	6.8 A	3.6 sec.	0E10
20	7.0 A	3.55 sec.	0DDE
21	7.2 A	3.50 sec.	0DAC
22	7.45A	3.4 sec.	0D7A
23	7.6 A	3.4 sec.	0D48
24	8.0 A	3.3 sec.	0CE4
25	8.2 A	3.25 sec.	0CB2
26	8.4 A	3.2 sec.	0C80
27	8.6 A	3.1 sec.	0C1C
28	8.8 A	3.09 sec.	0C12
29	9.0 A	3.05 sec.	0BEA
2A	9.2 A	3.04 sec.	0BE0
2B	9.4 A	3.02 sec.	0BCC
2C	9.6 A	2.98 sec.	0BA4
2D	9.8 A	2.95 sec.	0B86
2E	10.0 A	2.9 sec.	0B54
2F	10.2 A	2.88 sec.	0B40
30	10.4 A	2.86 sec.	0B2C
31	10.6 A	2.84 sec.	0B18
32	10.8 A	2.82 sec.	0B04
33	11.0 A	2.8 sec.	0AF0
34	11.2 A	2.79 sec.	0AE6
35	11.4 A	2.78 sec.	0ADC
36	11.6 A	2.77 sec.	0AD2
37	11.8 A	2.76 sec.	0AC8
38	12.0 A	2.75 sec.	0ABE
39	12.2 A	2.74 sec.	0AB4
3A	12.3 A	2.73 sec.	0AAE
3B	12.4 A	2.73 sec.	0AAA

3C	12.6	A	2.72	0AA0
3D	12.8	A	2.71	0A96
3E	13.0	A	2.7 sec.	0A8C
3F	13.2	A	2.68	0A78
40	13.4	A	2.66	0A64
41	13.6	A	2.64	0A50
42	13.8	A	2.62	0A3C
43	14.0	A	2.6 sec.	0A28
44	14.2	A	2.59	0A1E
45	14.4	A	2.58	0A14
46	14.6	A	2.57	0A0A
47	14.8	A	2.56	0A00
48	15.0	A	2.55 sec.	09F4
49	15.2	A	2.54	09EC
4A	15.4	A	2.53	08E2
4B	15.6	A	2.52	09D8
4C	15.8	A	2.51	09CE
4D	16.0	A	2.5 sec.	09C4
4E	16.2	A	2.48	09B0
4F	16.4	A	2.46	099C
50	16.6	A	2.44	0988
51	16.8	A	2.42	0974
52	17.0	A	2.40 sec.	0960
53	17.2	A	2.39	0956
54	17.4	A	2.38	094C
55	17.6	A	2.37	0942
56	17.8	A	2.36	0938
57	18.0	A	2.35 sec.	0926
58	18.2	A	2.34	0924
59	18.4	A	2.33	091A
5A	18.6	A	2.32	0910
5B	18.8	A	2.31	0906
5C	19.0	A	2.30 sec.	08FC
5D	19.2	A	2.28	08E8
5E	19.4	A	2.26	08D4
5F	19.6	A	2.24	08C0

60	19.8 A	2.22	sec.	08AC
61	20.0 A	2.2	sec.	0898
62	20.2 A	2.2	Sec.	0898
63	20.4 A	2.2	Sec.	0898
64	20.6 A	2.2	Sec.	0898
65	20.8 A	2.2	Sec.	0898
66	21.0 A	2.2	See.	0898

6.2 Microprocessor programme to get IDMT curve is as follows

Address	M/c Code		Mnemonics
2000	3E, 98		MVI A, 98
02	D3, 03		OUT 03
04	3E, 01		MVIA, 01
06	D3, 03		OUT 03
08	3E, 03		MVIA, 03
0A	D3, 03		OUT 03
0C	3E, 04		MVIA, 04
0E	D3, 03		OUT 03
10	CD, 00, 21	LP1	CALLADC
13	3A, 00, 24		LDA 2400
16	FE, 05		CP1(05)H corresponding to 1.3A
18	DA, 10, 20		JC LP1
1B	87		ADD A
1C	6F		MOVL, A



PROGRAM FLOW CHART FOR OVER CURRENT RELAY

1D	26, 22		MVI H, 22
1F	5E		MOVE, M
20	23		INXH
21	56		MOV D, M
22	EB		XCHG
23	CD, 50, 23	LP2	CALL DELAY
26	2B		DCX H
27	7D		MOV A, L
28	B4		ORA H
29	C2, 23, 20		JNZ LP2
2C	3E, 01		MVI A, 01
2E	D3, 01		OUT 01
30	EF		RST 5

Subroutines used in above programme are 6.2.1 and 6.2.2.

6.2.1 Subroutine for ADC

Address	M/c Code	Mnemonics	
2100	3E, 10	MVI A, 10	Logic 1 to 398
2	D3, 01	OUT 01	
4	3E, 06	MVI A, 06	PC_3 low
6	D3, 03	OUT 03	
8	3C	INR A	PC_3 high
9	D3 03	OUT 03	
0B	3D	DCR A	PC_3 low
0C	D3, 03	OUT 03	

0E	DB, 02	Check	IN 02	
10	E6, 80		ANI 80	EOC check
12	CA, 0E, 21		JZ Check	
15	DB, 00		IN 00	
17	32, 00, 24		STA 2400	
1A	3E, 00		MVI A, 00	
1C	D3, 01		OUT 01	
1E	C9		RET	

6.2.2 Subroutine for DELAY

Address	M/c Code	Mnemonics
2350	06, EA	MVI B, EA
52	05	LOOP DCR
53	C2, 52, 23	JNZ LOOP
56	C9	RET

6.3 Different programs may be used to obtain the various relaying characteristics.

For instantaneous O/C relay the programme is as follows:

Say I_{set} = 10.0 Amp.

The Hex. Display corresponding to 10.0 Amp. is 2E

The software for this type of relay will be as follows:

Address	M/c Code		Mnemonics
2000	3E, 98		MVI A, 98
2	D3, 03		OUT 03
4	3E, 01		MVI A, 01
6	D3, 03		OUT 03
8	3E, 03		MVI A, 03
A	D3, 03		OUT 03
C	3E, 04		MVI A, 04
E	D3, 03		OUT 03
10	CD, 00, 21	LP1	CALL ADC
13	3A, 00, 24		LDA 2400
16	FE, 2E		CPI (2E) H
18	DA, 10, 20		JC 'LP1'
1B	D3, 01		OUT 01
1D	EF		HLT

Subroutine 6.2.1. used in above programme.

6.4 For definite time O/c relay the programme will be

For definite time O/c relay, t = 2.2 sec. The software of this type of relay will be as follows:

Address	M/c Code	Mnemonics
2000	3E, 98	MVI A, 98
2	D3, 03	OUT 03
4	3E, 01	MVI A, 01
6	D3, 03	OUT 03
8	3E, 03	MVI A, 03

A	D3, 03	OUT 03
C	3E, 04	MVI A, 04
E	D3, 03	OUT 03
10	CD, 00, 21	CALL ADC
13	3A, 00, 24	LDA 2400
16	FE,(05) H	CPI (05) H
18	DA, 10, 20	JC to 2010
1B	21, 98, 08	LXI H 0898 Corresponding to 2.2 sec.
1E	CD, 50, 23	CALL DELAY
21	2B	DCXH
22	7D	MOV A, L
23	B4	ORA H
24	C2, 1E, 20	JNZ
27	3E, 01	MVI A, 01
29	D3, 01	OUT 01
2B	EF	HALT

Subroutine 6.2.1 and 6.2.2 are used in above programme.

6.5 By british standard following curve equations were given for very inverse and extremely inverse O/C characteristics

For very inverse, $t = \frac{13.5}{I-1}$

For extremely inverse $t = \frac{80}{I^2-1}$

6.5.1 Following software have been developed for very inverse characteristic

Address	M/c Code		Mnemonics	
2000	3E, 98		MVI A, 98	
2	D3, 03		OUT 03	
4	3E, 01		MVI A, 01	
6	D3, 03		OUT 03	
8	3E, 03		MVI A, 03	
0A	D3, 03		OUT 03	
C	3E, 04		MVI A, 04	
E	D3, 03		OUT 03	
10	CD, 00, 21	LP1	CALL ADC	
13	3A, 00, 24		LDA 2400	
16	FE,(05) H		CPI(05)H	Corresponding to 1.3 A
18	DA, 10, 20		JC 'LP1'	
2B	5F		MOVE, A	
2C	3A, 00, 24		LDA 2400	
2F	D6, 01		SUI 01	
31	21, BC, 34		LXI H, 34 BC	
34	CD, 50, 22		CALL DIV	
37	2A, 03, 25		LHLD 2503	
3A	CD, 50, 23		CALL DELAY	
3D	2B		DCX H	
3E	7D		MOV A, L	
3F	B4		ORA H	
40	C2, 3A, 20		JNZ LP2	

43	3E, 01		MVI A, 01
45	D3, 01		OUT 01
46	EF		HLT

Subroutines 6.2.1, 6.2.2 and 6.5.1.2 are used in the above programme.

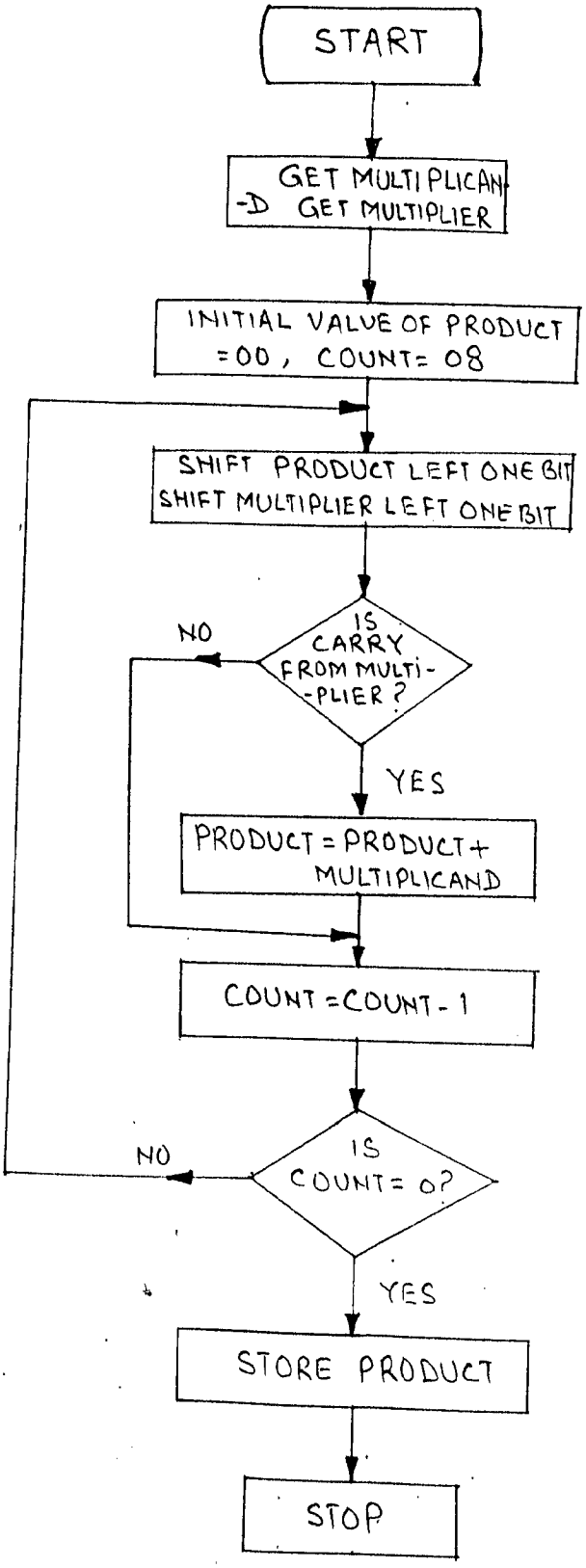
6.5.1.1 Subroutine for ADC and time Delay are same as used in IDMT programme.

Subroutine for Multiplication are as follows:

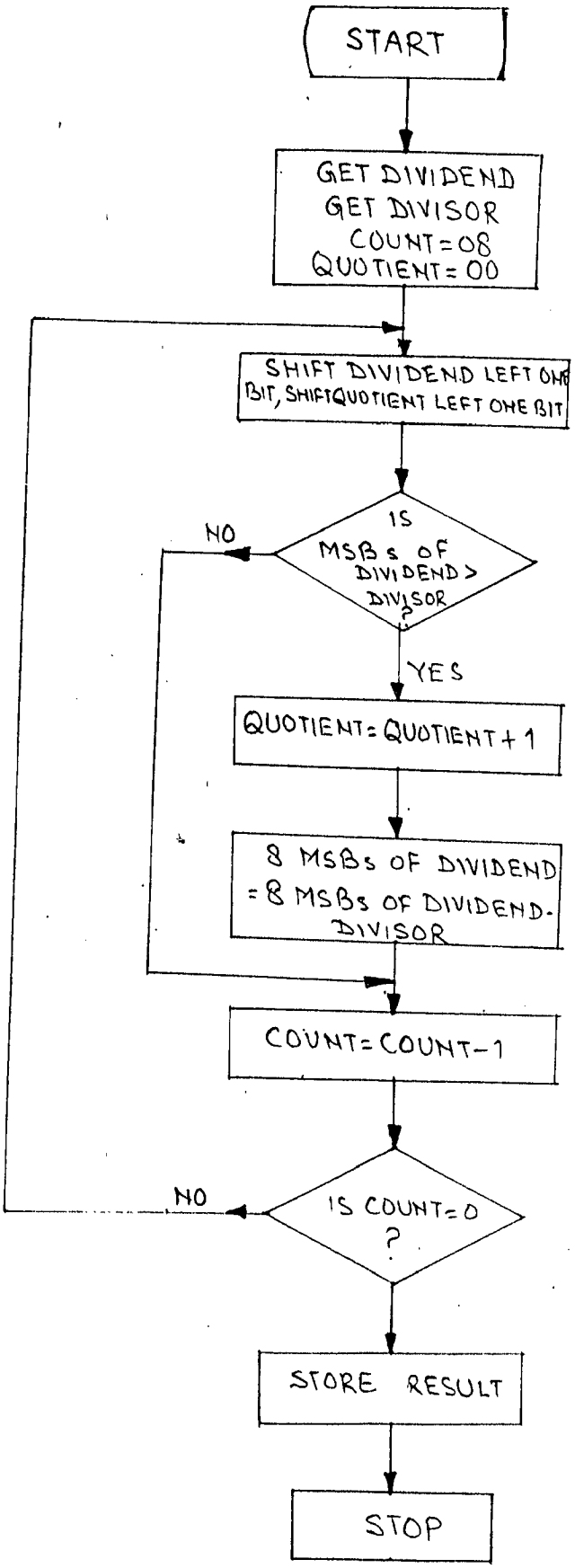
Address	M/c Code		Mnemonics
2300	21, 00, 00		LXI H, 0000
3	16, 00		MVI D, 00
5	00, 08		MVI B, 08
7	29	TOP	DAD H
8	17		RAL
9	D2, OD, 23		JNC LOOK
C	19		DAD D
D	05	LOOK	DCR B
E	C2, 07, 23		JNZ 'TOP'
11	7D		MOV A, L
12	32, 02, 25		STA 2502
15	C9		RET

6.5.1.2 For Division Subroutine is as follows:

2250	3A, 02, 25		LDA 2502
3	47		MOV B, A
4	OE, 08		MVI C, 08



PROGRAM FLOW CHART FOR 8 BIT MULTIPLICATION



PROGRAM FLOW CHART FOR 8 BIT DIVISION

56	29	DIV.	DAD H
7	7C		MOV A, H
8	90		SUB B
9	DA, 5E, 22		JC AHEAD
5C	67		MOV H, A
5D	2C		INR L
5E	OD		DCR C
5F	C2, 56, 22		JNZ DIV
62	22, 03, 25		SHLD 2503 A (Quotient in 2503)
65	C9		RET

6.5.2 Following software have been developed for extremely inverse characteristic

Address	M/c Code		Mnemonics
2000	3E, 98		MVI A, 98
2	D3, 03		OUT, 03
4	3E, 01		MVI A, 01
6	D3, 03		OUT 03
8	3E, 03		MVI A, 03
OA	D3, 03		OUT 03
C	3E, 04		MVI A, 04
E	D3, 03		OUT 03
10	CD, 00, 21	LP1	CALL ADC
13	3A, 00, 24		LDA 2400
16	FE,(05) H		CPI(05)H - Corresponding to 1.3 A

18	DA, 10, 20		JC LP1
2B	5F		MOV E, A
2C	CD, 00, 23		CALL MULT
2F	3A, 00, 24		LDA 2400
32	D6, 01		SUI, 01
34	21, E2, 04		LXIH 04 E2
37	CD, 50, 22		CALL DIV
40	2A, 03, 25		LHLD 2503
43	29		DAD H
44	29		DAD H
45	29		DAD H
46	29		DAD H
47	29		DAD H
48	CD, 50, 23	LP2	CALL DELAY
4A	2B		DCX H
4B	7D		MOV A, L
4C	B4		ORA H
4D	C2, 48, 20		JNZ LP2
50	3E, 01		MVI A, 01
52	D3, 01		OUT 01
54	EF		HLT

Subroutines used in the above programme are 6.2.1, 6.2.2, 6.5.1.1 and 6.5.1.2.

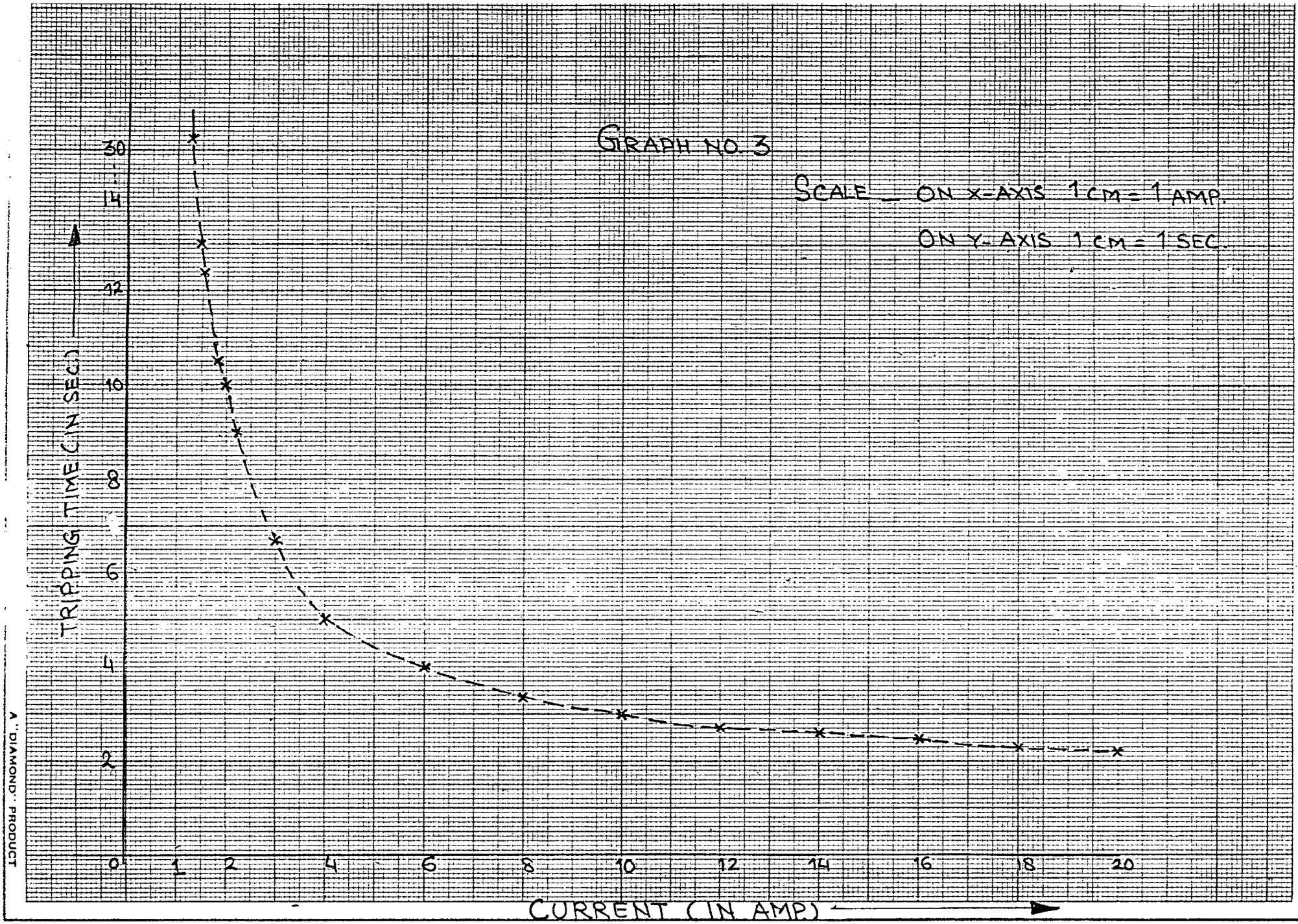
CHAPTER - 7

7. TEST RESULTS:

When microprocessor programme for IDMT was run, the following tripping timing were recorded for the different current. The tripping time was recorded with the help of a stop watch.

Current (In Amp.)	Tripping Time in sec.
1.3 A	33 sec..
1.4 A	13 sec.
1.5 A	12.4 sec.
1.8 A	10.5 sec.
2.0 A	10.0 sec.
2.2 A	9.0 sec.
3.0 A	6.8 sec.
4.0 A	5.0 sec.
6.0 A	4.0 sec.
8.0 A	3.4 sec.
10.0 A	3.0 sec.
12.0 A	2.7 sec.
14. 0 A	2.6 sec.
16.0 A	2.5 sec.
18.0 A	2.3 sec.
20.0 A	2.2 sec.

The above tripping time has been plotted against the current in graph no. 3 to get IDMT characteristic. Similarly other programme for different overcurrent relays were checked and found satisfactory.



CHAPTER - 8

8. CONCLUSION

The performance of the microprocessor based overcurrent relays is quite satisfactory. The IDMT characteristic plotted by using test results is quite satisfactory. Microprocessor based overcurrent relays offer attractive compactness and flexibility. With the help of the same program any kind of time-current characteristic of IDMT, very inverse, extremely inverse, definit time instantaneous overcurrent relay can be obtained. The microprocessor being very fast can sense the fault currents of a number of circuits using multiplexers and send the tripping signal to the circuit breaker of the faulty circuit. It means microprocessor is capable to handle number of circuits at a time. As the use of IC's is more economical and fast so in near future the protection of distribution lines, industrial motors and other electrical equipment of much importance will be encouraged by the use of integrated circuits.

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