"DEVELOPMENT OF MICROPROCESSOR BASED COMMUTATORLESS CONSTANT POWER KRAMER DRIVE"

A DISSERTATION

Submitted in partial fulfilment of the requirements for the award of the degree of

MASTER OF ENGINEERING

in

ELECTRICAL ENGINEERING

(Power Apparatus and Electric Drives)

By

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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the dissertation entitled DEVELOPMENT OF MICROPROCESSOR BASED COMMUTATORLESS CONSTANT POWER KRAMER DRIVE, in partial fulfilment of the requirement for the award of the degree of Master of Engineering in Electrical Engineering, University of Roorkee, Roorkee, is an authentic record of my own work carried out for a period of about seven months from August, 1988 to Feb - ruary 1989 under the supervision of Dr. S.P.Gupta, Reader and Dr. Bhim Singh, Reader, Department of Electrical Engineering, University of Roorkee, Roorkee,India.

The matter embodied in the dissertation has not been submitted by me for the award of any other degree or diploma.

Dated June 23,1989

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ABSTRACT

The dissertation concerns the Development of Micro - processor Based Commutatorless Constant Power Kramer Drive which consists of a wound rotor Induction motor and a commutatorless motor. The slip power extracted from the ~~sta~~rotor terminals of the induction motor is rectified and converted to mechanical power by the commutatorless motor which is coupled mechanically to the induction motor shaft forming a constant power drive. The d.c. link consists of a rectifier, a chopper, and a commutated inverter. The d.c. link inverter and synchronous machine with synchronised firing circuit is popularly known as commutatorless motor (CLM). The CLM is among the earliest attempts to replace the mechanical commutator of D.C.motor.

Speed control in the entire sub-synchronous region is accomplished by either varying the field current of the CLM, or the duty cycle of the chopper. By reducing the duty cycle of the chopper, the effective armature voltage of the CLM and hence the speed of the drive is reduced.

The firing pulses of the thyristors of LCI and chopper are generated by the microprocessor. The firing angle of LCI is kept constant through out the operation. The system description, principle of operation and imple - mentation of the system software and flowcharts are presented.

The performance characteristics of chopper controlled commutatorless Kramer drive are studied on a laboratory size experimental set up. It is shown that the voltage and current waveforms obtained with this scheme are sinusoidal and are almost free from harmonics.

CONTENTS

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CHAPTER - 1

INTRODUCTION

1.1 GENERAL

Variable speed drives may be realised by using d.c. motor or a.c. motor as the drive motor. A d.c. motor offers simpler means for stepless speed control below and above the base speed in comparison with a.c. motor. However, the d.c. motor suffers from the disadvantages, listed below, on account of its commutator.

(a) It limits the power rating and speed of the machines that can be built,

(b) It imposes restrictions on the ambient conditions,

(c) It prevents full torque at standstill for more than a few seconds.

(d) It increases the length, weight and inertia of the motor which are the disadvantages for several applications such as traction, servo drives etc.

Furthermore, D.C. machines are of complicated mechanical construction and hence more expensive. For these reasons engineers have investigated for a long time, the possibilities of variable-speed drives which use A.C. motors.

Some of the advantages of A.C. motors over D.C. motors are -

(i) simple and robust construction.

(ii) no commutator and hence sparking problems are not present. Hence, a.c. motors can perform much better in explosive atmospheric conditions.

(iii) higher power/weight ratio.

(iv) less maintenance and hence running cost.

(v) Though a.c. motor is considerably cheap compared to D.C.motor, cost of static inverter is comparatively much higher than converter. In general, above 50 KVA, the difference in cost of motors is more dominating and hence now-a-days a.c. drives are recommended on economic considerations.

With numerous other merits available with a.c. drives, present trend is to use a.c. drives [1-3].

Two basic modes of operation of variable speed a.c. drives have been identified as synchronous and non-synchronous and two basic methods of control namely frequency control and control of rotor voltage, Synchronous motor drives can only be frequency controlled. Now - synchronous drives can be controlled by either method.

The induction machine is most commonly used in adjustable speed a.c. drive system. Between the two classes of induction machines- squirrel cage and wound rotor, the former is always preferred, because the wound rotor machine is more bulky and expensive and has the additional disadvantages due to the

presence of slip-rings and brushes. The wound rotor machines had long been used for inexpensive speed control by mechanically varying the rotor circuit rheostats. One advantage of this type of machines is that slip power becomes available which can be controlled to control the speed of the machine. For limited range speed-control applications, where the slip power is only a fraction of the total power of the machine, the converter cost reduction may be substantial. The advantage of this system is that the slip power can be controlled to flow either out of the rotor or to the rotor and thus super-synchronous regions with motoring can also be achieved.

ROTOR-RESISTANCE CONTROL

The speed of a wound rotor machine can be varied by varying the rotor circuit resistance through an externally connected resistor bank. Also thyristor chopper circuit is used [4-15] on the rotor side for the speed control of slip-ring induction motor drive. This control scheme provides contactless and continuous variation of rotor resistance. Rotor resistance control is very inefficient because the slip-energy is wasted in the rotor circuit resistance.

SLIP POWER RECOVERY

Instead of wasting the slip-power in the rotor circuit resistance, it can be either converted to a.c. and pumped back to the supply lines forming a constant torque type

system or used more directly by converting it into mechanical power and adding the same to the main shaft, thus forming a constant power type system.[6,7]. The former method, where the slip power is recovered back to the line through a converter cascade is known as static Kramer drive [8-11].

The original ~~digital~~ Kramer drive system used a rotory converter instead of a diode rectifier and fed power to a d.c. motor coupled to the Induction machine shaft. After the second world war, a modified Kramer Revival' using a transformer/mercury-arc rectifier combination as a converter was successfully applied to several mine ventillating fan drives [12-14].This drive system is not only efficient but the converter power rating is low, because it has to handle only the slip power. This power rating becomes lower for a more restricted speed range near the synchronous speed. The additional advantages are that the drive system has characteristics like d.c. machine and the control circuit is simple. These advantages off set to some extent the disadvantages of the wound-rotor machine and poor power factor characteristics.

The static Kramer systems do not have the regenerative mode of operation. This feature requires that the slip power in the rotor should flow in the reverse direction. If the diode bridge rectifier is replaced by thyristor bridge, the slip power flow can be controlled in either direction. Such a static Kramer system with a bi-directional slip-power flow

can be controlled for motoring and regeneration both in sub-synchronous and super-synchronous ranges of speed. The dual converter system in a static Kramer drive can be replaced by a single-phase controlled line commutated cycloconverter to permit the slip-power flow in either direction, such a scheme is known as a Static Scherbius drive. This type of drive has poor power factor characteristics.

The use of inverter circuits [16-18] so far reported for speed control of induction motor are ussually of forced commutated type and the risk of commutation failure is more because of high instantaneous currents and steep rise in voltages at the time of commutation. The use of cyclo-converter circuits gives limited variations in frequency and requires complicated trigger circuits. Because of these limitations, these circuits are not reliable in case of group drive applications, such as intraction system and textile industry. To overcome some of these disadvantages of forced commutated inverter circuits, a d.c. link inverter consisting of inverter - synchronous machine combination as a variable frequency source is been discussed by Ranganadhachari et.al. [19]. The d.c. link inverter and synchronous machine combination is popularly known as commutatorless D.C. machine (CLM). This drive system is comparable to the variable speed d.c. drive and some of the limitations of variable speed d.c.

machines that is, commutator effect at higher speed can be overcome in this system.

A scheme for power factor improvement for very high power applications is known as the commutatorless Kramer system [20-25] for large capacity induction motors. The speed and torque of the drive system are controlled by the inverter firing angle and field current so that the line commutation of the inverter is possible at optimum firing angle on different speeds. As a characteristic of the line commutated inverter drive, speed control is not possible at a low value of speed because of insufficient counter emf.

To reduce the speed of the drive down to almost zero a chopper is included in the armature circuit of the D.C. motor of the Kramer drive. The use of thyristor chopper is very favourable because of high efficiency, flexibility in control, small size and quick response to very low speeds. The output voltage of the chopper can be controlled by using thyristor firing techniques to produce time ratio control or current limit control. The chopper may then be operated either at a constant frequency or at a constant ON or OFF time abd variable frequency. Between the different methods of time-ratio control, the one with variable ON-time and constant frequency is preferable because it permits a choice of frequency suitable to the supply. The commutation circuit, the filter circuit and the load ensuring fast response.

By controlling the duty cycle of the chopper, the effective armature voltage of the d.c. motor is controlled and it is possible to reduce the speed of the drive down to almost zero [26-28].

The firing circuit for a 3-phase variable frequency thyristor bridge is developed by Naik et.al [29]. The microprocessor has opened up an existing range of opportunities to the variable speed drives [31-35]. In the present work, a microprocessor based chopper controlled commutatorless Kramer drive is considered to study the performance of the drive system.

1.2 LITERATURE SURVEY

A larger volume of research work has been published on the Kramer drive. From the literature review it is found that not much work has so far been reported on chopper controlled commutatorless Kramer drive. Bose [1] reviewed the present status of ac drive technology in which the salient technical features of ac machines, converters, controls and performances of the integrated drive systems are described. Jones and Brown [2] outlined the control of speed of electrical machines from the earlier methods to their modern equivalents using electronic control.

The variable speed ac drives are identified as Induction motors and synchronous motor drives. The wound rotor machines were long been used for speed control by

varying the rotor circuit rheostats. The speed control of slip ring induction motor is also reported using thyristor chopper controlled resistance in the rotor circuit [4 and 5]. This control scheme provides contactless and continuous variation of rotor resistance.

Instead of wasting the power in the rotor circuit as heat, the slip power may be either returned to the shaft of the main motor or returned to the supply after modifying its frequency to be equal to supply frequency. Shepherd and Khalil [6] investigated the improvement of the power factor using capacitor in the rotor circuit of slip energy recovery system and also using two sets windings in the rotor [7]. Mittle and Venkatesan [8 and 9] determined stability and instability region of a static slip region of a static slip-power recovery drive. Doradla et.al.[11] investigated a new slip-power recovery scheme with a PWM converter with the improved supply power factor. The speed and torque characteristics of this drive were similar to those of a separately excited d.c. motor.

The basic Kramer combination developed some 80 years ago, used a rotary converter to provide the necessary slip-frequency ac to dc conversion. But the cost of providing, maintenance, multiplicity of machines and brush gear naturally told rather heavily against this type of drive. Clapham and Griffin [12] have described the usefulness of modified Kramer system

for large power outputs using a transformer/mercury arc rectifier combination as a converter. The only limitation is that the rectifier in the Kramer combination constitutes a non-return valve and this prevents the bi-directional power flow possible in the a.c. commutator motor. In consequence, power can be abstracted (only) from the rotor and not supplied to it and thus the speed range is extended from just under synchronous speed down to half synchronous speed and below [13 and 14].

When the applications of conventional d.c. machines are limited by their commutator they can be replaced by an equivalent system of a static convertor and an a.c. machine the combination of a synchronous motor and a load commutated inverter is well adopted to high power levels and is popularly known as commutatorless motor (CLM). The inverter circuit is a fully controlled thyristor bridge [16-18], triggered synchronously with the revolution of the rotor of the machine. Ranganadhachari et al [19] attempted for the feasibility of a CLM as a variable frequency source to the induction motor. The main feature of this variable frequency operation of induction motor is that it provides continuous control over a wide range of speed and is efficient. Okuyama [21] has discussed the effects of machine constants on steady state and transient characteristics of commutatorless motors. Nacto [22] discussed the effect of field current fluctuations on operating performance of the CLM.

Kuniomi Oguchi [24] proposed the speed control of a brushless static Kramer system. He discussed the various control methods such as field control method, chopper control method, and advance angle control method on the drive system. He showed that the smooth speed variation is possible by chopper control. Wakabayashi [25] described the commutatorless Kramer control system and applied commercially for driving large capacity pumps. Venkatesan and Gupta [26 and 28] suggested a method to extend the speed range in the sub synchronous region down to almost zero by including a chopper in the modified Kramer system. The steady state performance of this system is also discussed [27].

A firing circuit for the 3-phase variable frequency thyristor bridge inverter is given by Naik et.al. [29].The firing pulses for the thyristors of the LCI and the chopper are generated by a microprocessor. Richter [34] have discussed the microprocessor controlled inverter-fed synchronous motor. The important advantage of microprocessor control is that of flexibility. No hardware changes are required if it is desirable or necessary to make control modifications. Chakaraborty [35] has discussed the microprocessor controlled commutatorless d.c. series motor by using induced voltage commutated inverter along with the induced voltage sensor.

In the present work, a microprocessor based chopper controlled commutatorless constant power Kramer drive is fabricated and experimental performance characteristics are obtained.

1.3 SCOPE OF THE PRESENT WORK

The present work is concerned with the development of the microprocessor based commutatorless constant power Kramer drive. Which consists of a wound rotor induction motor (main motor) and a synchronous motor (auxiliary motor) mechanically coupled to the same shaft of the main motor and load. The slip power extracted from the ~~stator~~ rotor terminals of the induction motor is rectified by an uncontrolled rectifier bridge. The d.c. link consists of a d.c. chopper and an inductor which are connected to the load commutated inverter which supplies power from the d.c. source to the synchronous motor. The d.c. link inverter-synchronous motor combination is popularly known as commutatorless d.c. motor (CLM). This drive system is comparable to the variable speed d.c. drive and some of the limitations of variable speed d.c. machines, namely, the commutator effect at higher speed can be overcome in this system. The function of the inductor on the dc side is to smooth out current undulations and to make the current continuous in the circuit.

The speed of the drive system can be either varied by varying the duty cycle of the chopper thus varying the

d.c. link voltage or by varying the field excitation of the synchronous motor. Speed control in a wide range from synchronous down to almost zero could be obtained. However, the field weakening of the CLM causes commutation failure due to insufficient induced emf available at synchronous motor terminals. So field current should not be reduced to very low values.

A simple microprocessor based firing control scheme using reduced hardware components are designed, fabricated and tested. The no load test is carried out on the chopper controlled commutatorless constant power Kramer drive by varying the field current of the separately excited CLM with constant duty cycle of the chopper & varying the duty cycle with constant field current of the CLM. The load test is performed on the drive at different duty cycle and field current settings and the steady state performance of the drive is obtained experimentally. The waveforms and oscillograms at different points of the control circuit and power circuit are recorded and discussed.

1.4 OUTLINE OF THE CHAPTERS

In chapter II, the complete hardware of the present scheme is discussed in detail. The design of power circuit, microprocessor based firing control circuit using less hardware componebts, pulse amplifier and ADC circuits are presented in this chapter.

The implementation of software and flowcharts of the chopper controlled commutatorless Kramer drive is discussed in Chapter III. The various subroutines used in conjunction with the main program such as ADC, subroutine, MULT subroutine, IR_0, IR_2 and IR_5 interrupt subroutine are also developed in this chapter.

Chapter IV deals with the experimental steady state performance of the drive system. Conclusions and suggestions for further work are discussed in chapter V.

The rating of the machine pin details and connection diagram of ADC chip and assembly language program for steady state performance of the drive are given in APPENDICES.

CHAPTER - II

DESCRIPTION OF THE SYSTEM

2.1 GENERAL

A chopper controlled commutatorless kramer drive system presents a constant power type slip energy recovery drive, which is different with respect to the conventional Kramer drive, in that the d.c. motor is replaced by commutatorless d.c. motor. The commutatorless d.c. motor is obtained by feeding a synchronous motor from a 3-phase inverter whose firing constants are synchronized with its speed and which is naturally commutated by the 3-phase voltages available at its output terminals in the form of induced emf of the synchronous motor. A chopper is included in the d.c. link to effectively control armature voltage of the d.c. motor and thereby control the shaft speed in sub-synchronous region. A microprocessor based control scheme for line commutated inverter and the time ratio control of the chopper is described in detail.

2.2 PRINCIPLE OF OPERATION

A block diagram of the system considered is shown in Fig. 2.1. It consists of a wound rotor Induction motor, an uncontrolled diode bridge rectifier, a smoothening d.c. link inductor, a series connected chopper, a line commutated inverter and a synchronous motor whose field is separately excited. The rectifier bridge along with the d.c. chopper

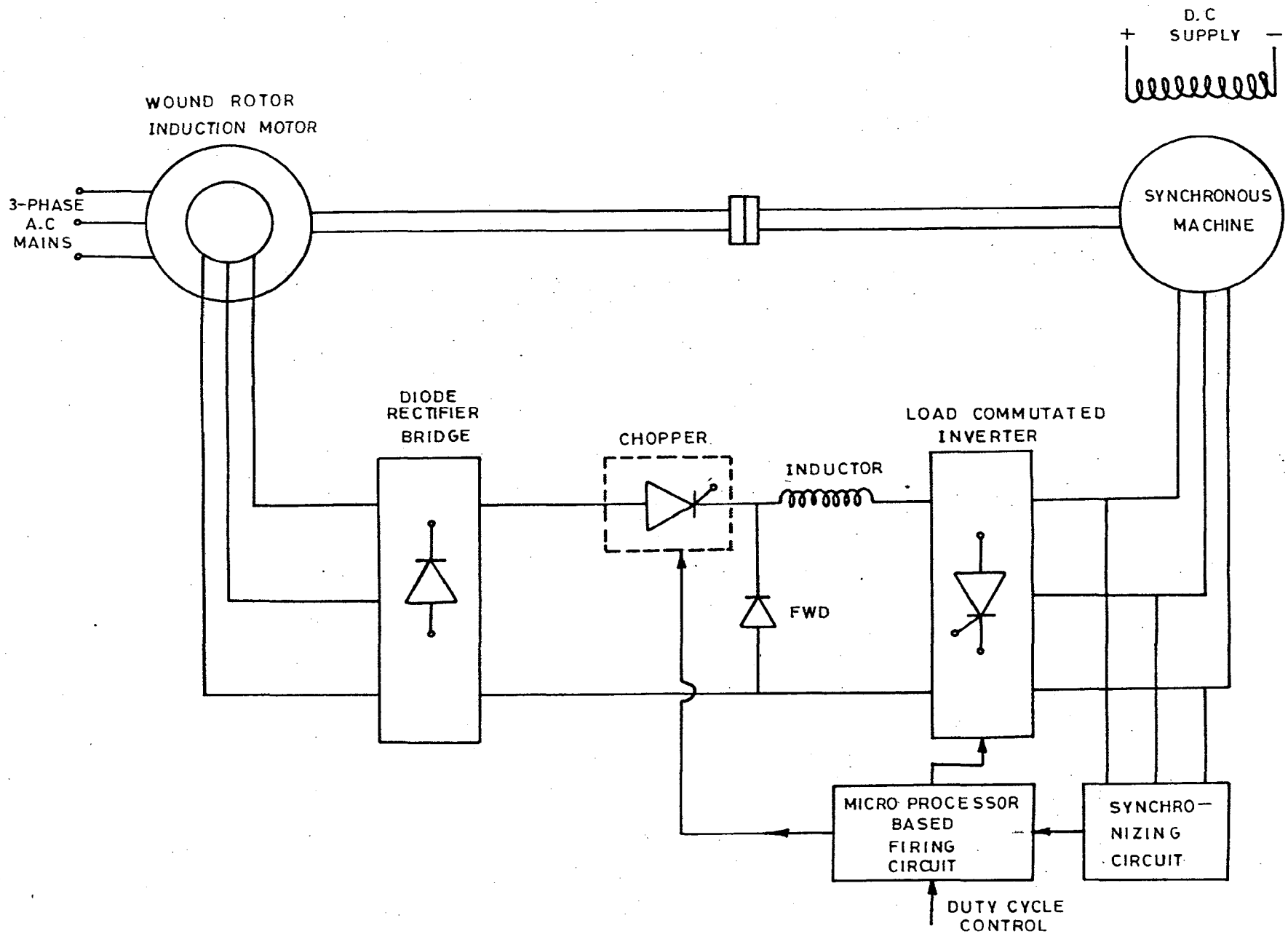


FIG. 2·1—BLOCK DIAGRAM OF CHOPPER CONTROLLED COMMULATORLESS KRAMER DRIVE

and the d.c. link inductor forms the variable d.c. source. The variable d.c. voltage is impressed at the d.c. input terminals of the line commutated inverter (LCI). The LCI supplies power from the D.C. source to the synchronous machine. It is a three phase fully controlled SCR bridge and can be operated in an inverter mode by suitably chosing the firing angle between 90^{o} and 180^{o}. The synchronous machine is a conventional one. The inverter-synchronous machine along with the synchronising gating circuit constitutes a commutatorless d.c. motor (CLM)

The system is started by running the synchronous machine as a synchronous generator with Induction motor acting as prime mover and the firing pulses for invertor thyristors are derived from the generated emf of the synchronous machine stator by the induced voltage sensor. The firing pulses are generated by means of microprocessor to the thyristors of the inverter and the chopper. The input power to LCI is increased by duty cycle so that the inverter input d.c. voltage increases and power is pushed through LCI from d.c. side to a.c. side. The synchronous machine now operates as a motor offering characteristics of a separately excited d.c. motor. The speed control of this commutatorless Kramer drive is obtained either by varying the d.c. input voltage which is achieved by varying the duty cycle of the chopper or by changing the field excitation of the synchronous motor. By controlling the duty cycle of the chopper, it is possible to reduce the speed of the drive down to very close to zero.

2.3 SYSTEM DESCRIPTION

The schematic diagram of the chopper controlled commutatorless Kramer drive using induced voltage commutation along with the voltage sensor for synchronization is shown in Fig. 2.2. The major components comprising the system are briefly discussed as under.

(i) Three-phase wound rotor Induction motor.

It is a conventional Induction motor whose slip-rings are connected to an uncontrolled diode rectifier bridge. The slip power is extracted and then rectified supply is fed to the commutator less machine which is coupled to the same shaft of the Induction motor, thus obtaining a constant power drive system.

(ii) Uncontrolled diode bridge rectifier.

The function of the diode rectifier is to rectify the rotor frequency ac voltage to a dc voltage and the bridge configuration gives better utilization of the motor giving a six pulse output.

(iii) D.C.Chopper

Choppers are widely used for speed control of separately excited D.C.motor as they offer high efficiency quick response, wide speed control range down to very low speeds. The firing pulses are generated by the microcomputer to trigger the main and auxiliary thyristors TH_1 and Th_2, of

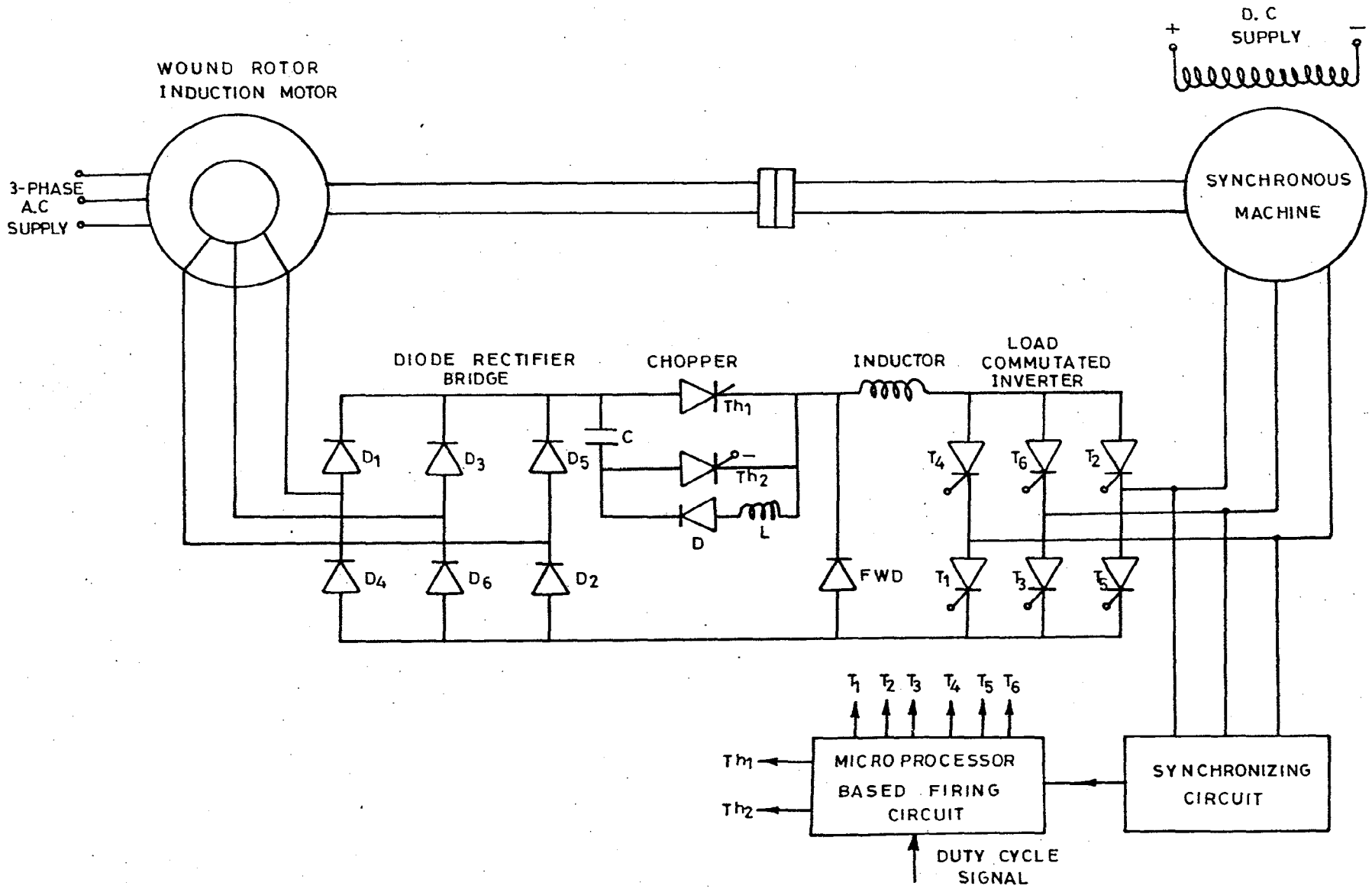


FIG. 2·2 — SCHEMATIC DIAGRAM OF CHOPPER CONTROLLED COMMUTATORLESS KRAMER DRIVE

the chopper. The main thyristor in a chopper has to be turned off by auxiliary commutation circuitary. The voltage commutation circuit comprises an auxiliary thyristor Th_2, a diode D, an inductor I, and capacitor C. To start the circuit, capacitor C is initially charged by firing the thyristor Th_2, charging is now from the source via Th_2 and load with the charging thyristor turning off as the charging current decays to zero. Fig 2.3 shows the voltage commutated chopper. The output voltage of chopper is usually controlled either by using time ratio control(TRC) or by using current limit control (CLC). In TRC, the ON to OFF time ratio is adjusted. The chopper may then be operated either at a fixed frequency and variable ON or OFF time ar at a variable frequency and fixed ON or OFF time. In CLC, the load current is restricted between specified maximum and minimum values by using suitable firing techniques Although both the schemes have relative advantages and limitations, choppers with variable ON time and fixed frequency are preferable because these are simple and provide flexibility in control.

(iv) D.C. link inductor.

The function of the D.C. link inductor is to smooth out the current undulations and to make the current continuous in the circuit. Hence a large value of inductance is connected in the d.c. link of the system.

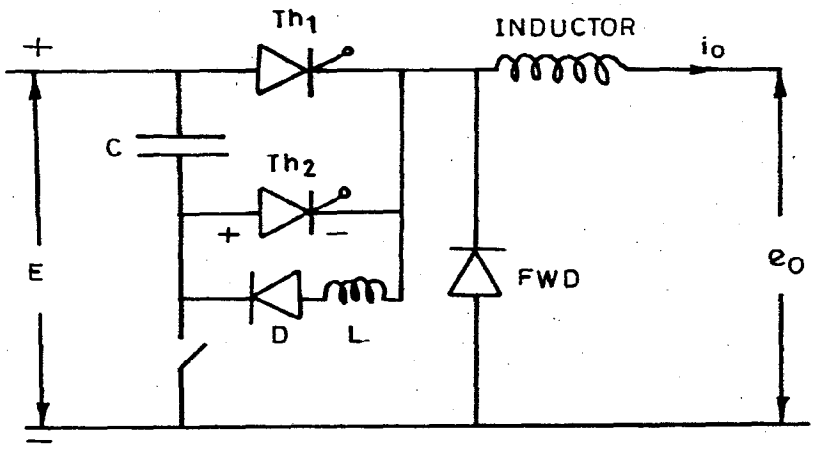


FIG. 2·3 (a)—VOLTAGE COMMUTED CHOPPER

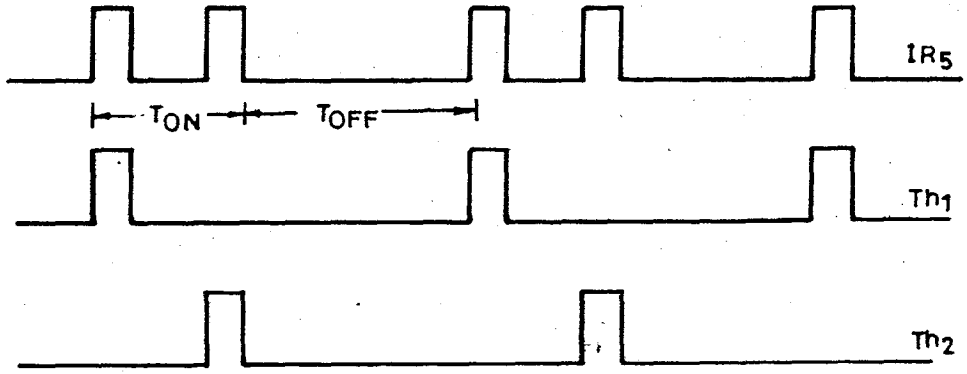


FIG. 2·3 (b)—WAVE FORMS OF THE INTERRUPT IR_5 AND THE FIRING PULSES FOR MAIN AND AUXILIARY THYRISTORS

(v) Line commutated inverter (LCI)

It is a simple three phase thyristorized inverter bridge. It converts the d.c. voltage into ac voltage of variable amplitude and frequency. The induced voltage in the stator of the synchronous machine is utilised to gene - rate the firing pulses for inverter thyristors. The relationship between line to line and line to neutral voltages at synchronous machine terminals along with the firing instants of the thyristors are shown in Fig. 2.4. The thyristors T_1, T_3, T_5 are called positive group since they are turned on when the machine terminal voltages are positive, similarly the thyristors T_4, T_6, T_2 are called negative group SCRs. Since they are triggered when the machine voltages are negative. The firing angle of the inverter is always greater than 90° and measured from the instant o. crossing point of two phase voltages as shown in Fig. 2.4. In the normal operation, always two thyristors one from positive group and another from negative group will remain in conduction. Thyristors are triggered at 60° interval with respect to the terminal voltage frequency. Each thyristor conducts for a period of 120° and the frequency of current is same as that of machine terminal voltage. In case of LCI, machine current always leads the corresponding phase voltage. The d.c. output voltage of a fully controlled converter is given by the following equation.

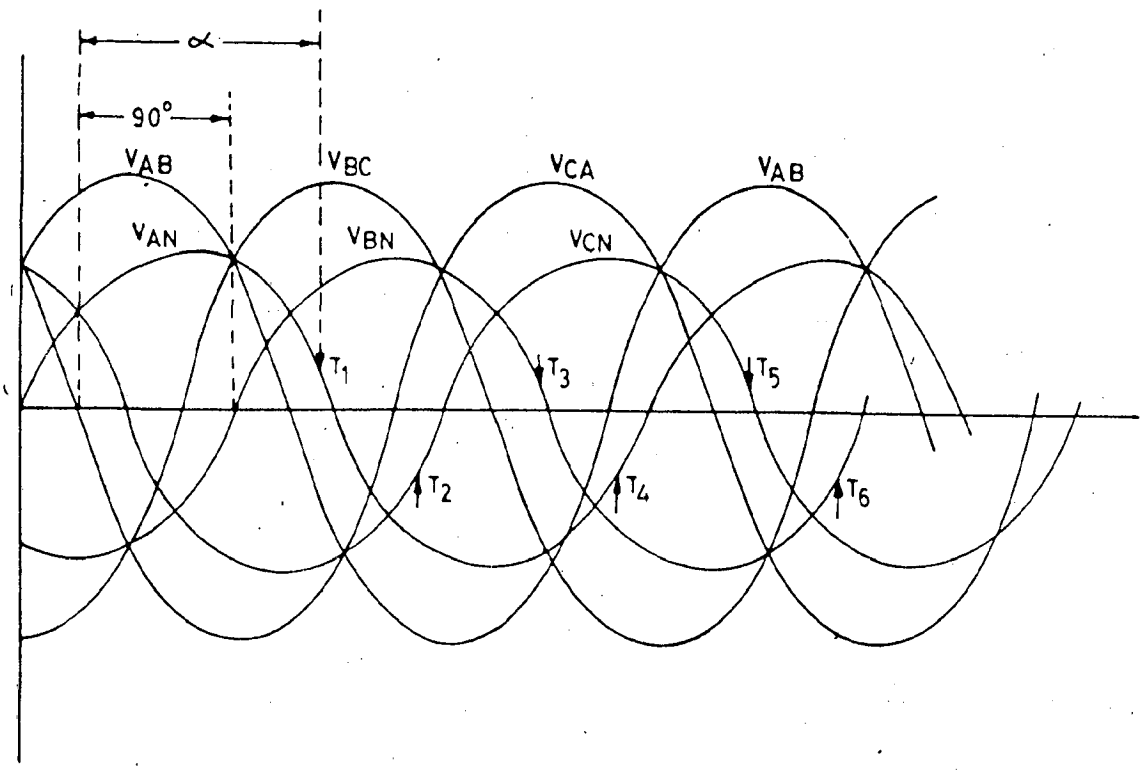


FIG. 2.4 – RELATIONSHIP BETWEEN LINE TO LINE AND LINE TO NEUTRAL VOLTAGE ALONG WITH INSTANT OF FIRING

TABLE 2·1

CONDUCTION DURATION	0°– 60°	60°–120°	120°–180°	180°–240°	240°–300°	300°–360°
FIRING SEQUENCE	1	2	3	4	5	6
THYRISTOR PAIR TO BE FIRIED	6 , 1	1 , 2	2 , 3	3 , 4	4 , 5	5 , 6

$$V_{dc} = \frac{3\sqrt{6}}{\pi} V \cos \alpha = Em \cos \alpha$$

where V = per phase ac voltage.

If a d.c. voltage source is connected to the inverter bridge in proper polarity and magnitude (> V_{dc}) then it will feed the power to the A.C. system through the controlled circuit.

(vi) Synchronous motor

It is a conventional synchronous motor and operated as a variable speed motor. The back emf of synchronous motor is used for natural commutation of the inverter thyristors. The frequency of the inverter is a function of the motor speed.

(vii) Synchronizing circuit

It consists of step down transformers, comparator, switching transistor, and AND gate. Synchronizing signal is derived from the line to line terminal voltages of the synchronous machine V_{AC} and V_{CB} and it is of 60° pulse width of the machine frequency at every cycle. This signal gives information about the operating frequency of the machine terminal voltage and 60° delay count.

Fig. 2.5 shows a zero-crossing detector circuit using IC 741.IC 741 is a voltage comparator. The output of which is a square wave on the principle of voltage comparison, that is the output swings ideally between +12V and -12V at every zero crossing of machine voltage frequency. The output of comparator

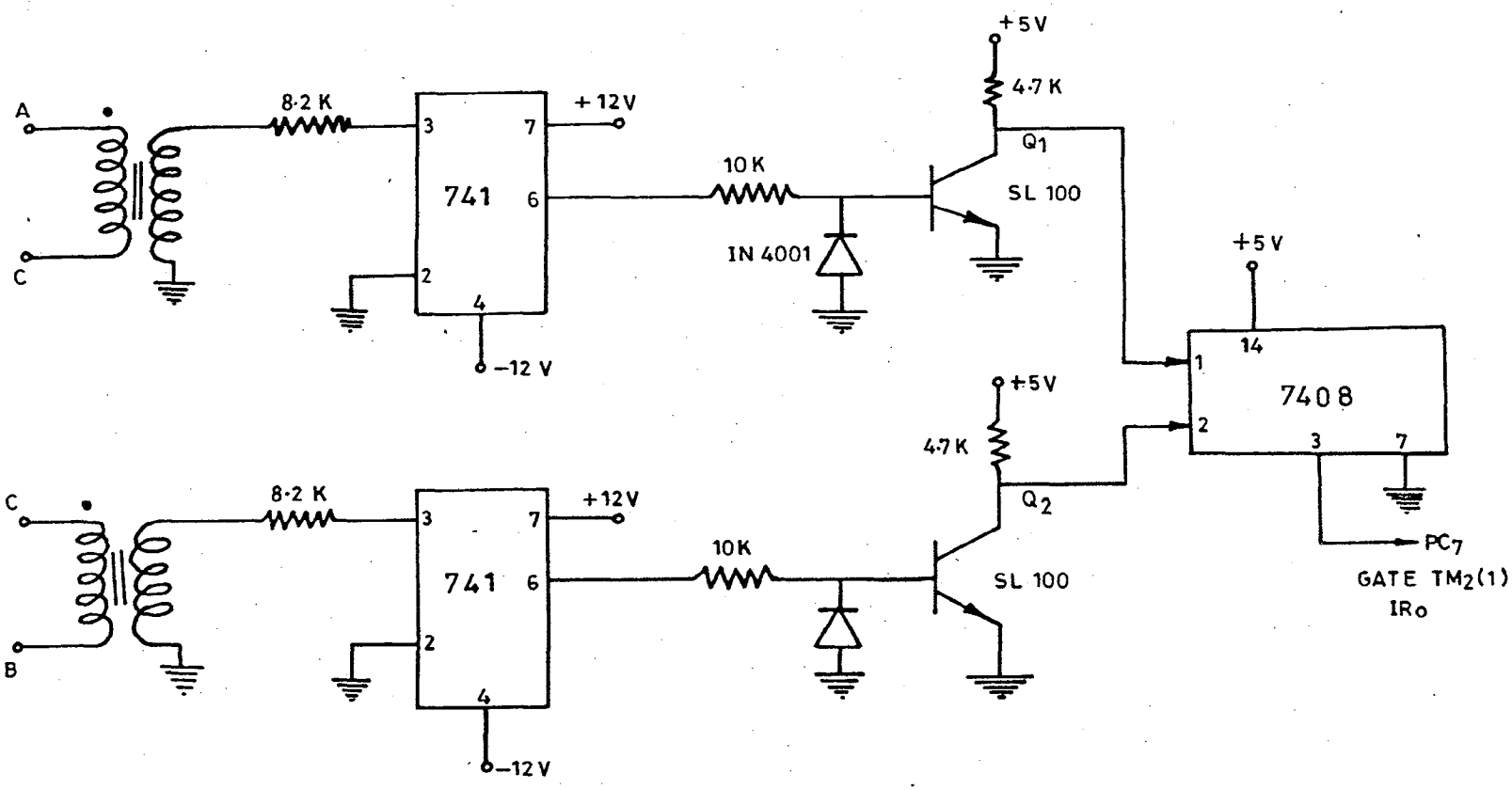


FIG. 2·5 — SYNCHRONIZING CIRCUIT

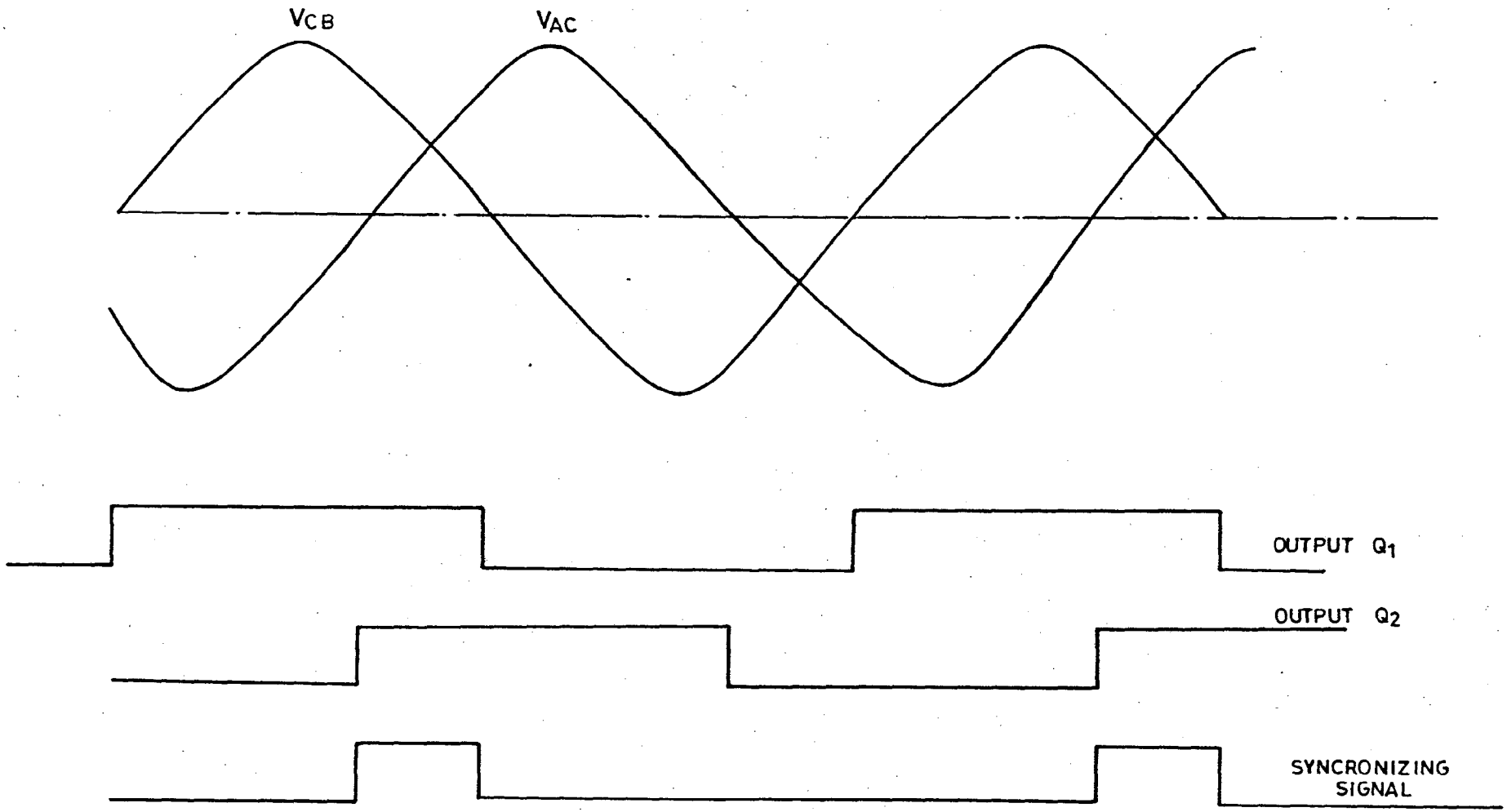


FIG. 2·6—VOLTAGE WAVESHAPES AT DIFFERENT POINTS OF SYNCHRONIZING CIRCUIT

is reduced to a lower voltage by a series connected resistor at the base of the transistor. The positive swing drives the transistor in to saturation producing a TTL input of approximately 0 volts and the negative swing drives the transistor in to cut-off producing an input of +5 volts. Thus the transistor inverts the input control signal. The diode in the base circuit protects the base against excessive reverse voltage as the negative output of the comparator approaches -12 volts. The two output signals of the transistor are ANDed in two input AND gate, IC 7408. It gives the required synchronizing signal of 60° pulse width as shown in Fig. 2.6 which is used to generate the firing pulses by the microprocessor.

(viii) Microprocessor based control circuit

The control circuit to generate the firing pulses for thyristors of LCI and chopper has two programmable interval timer (PIT-8253A), one programmable interrupt controller (PIC-8259) which is shown in Fig. 2.7. The synchronizing signal derived from machine terminal voltages is inputted to PC_7 of programmable peripheral interface (PPI-8255), gate of $counter_2(1)$ and IR0 pin of 8259A. The status of PC_7 is checked at every instant by the microprocessor to load the counter $TM_2(1)$ with FFFF H for the calculation of 60° count. A clock of 511.67 KHz is generated by operating $TM_1(1)$ in mode 2 from a clock of 1.535 MHz. This clock is provided to the $TM_2(1)$ and $TM_1(2)$. All the counters except $TM_1(1)$

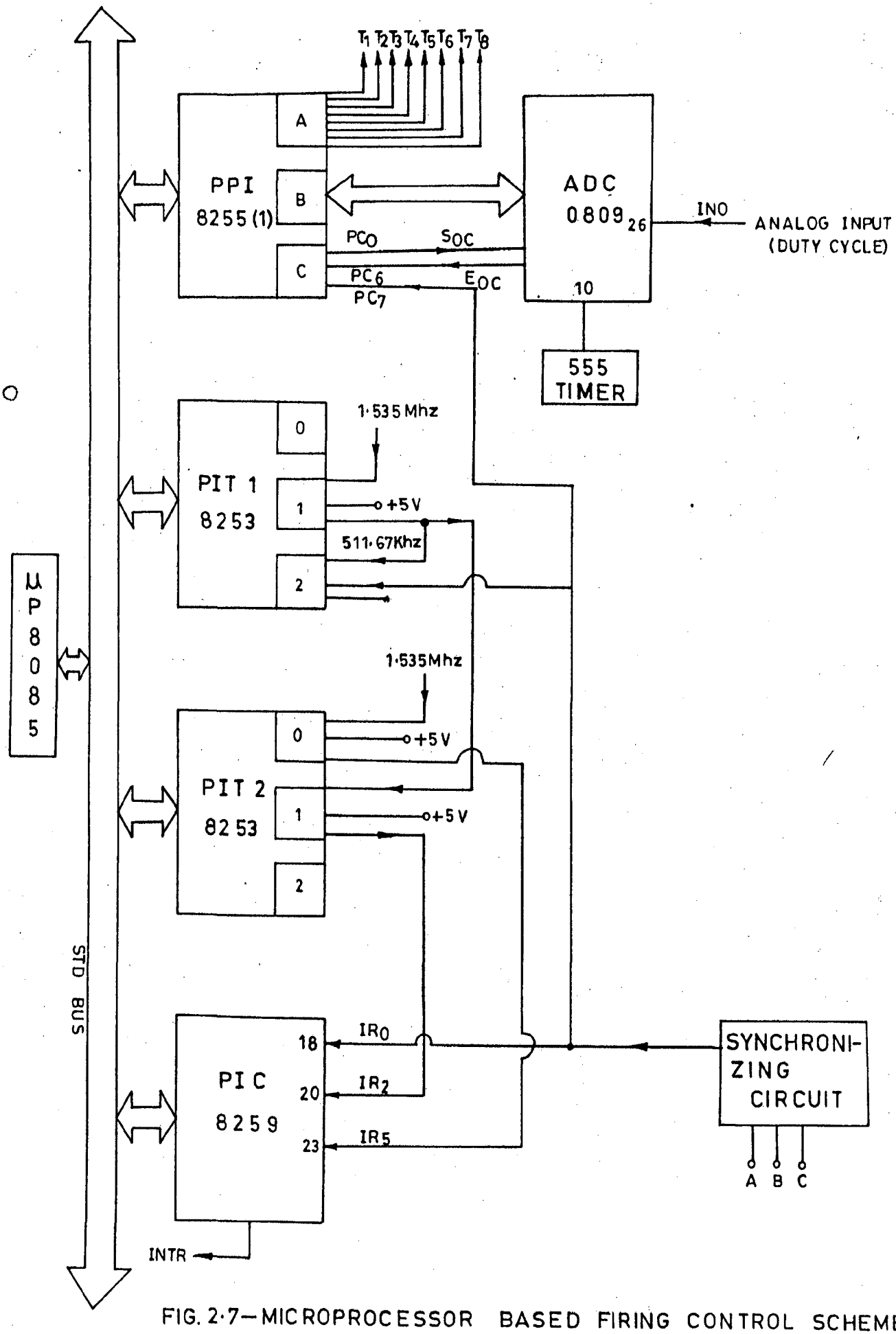


FIG. 2·7—MICROPROCESSOR BASED FIRING CONTROL SCHEME FOR CHOPPER CONTROLLED COMMUTATORLESS KRAMER DRIVE

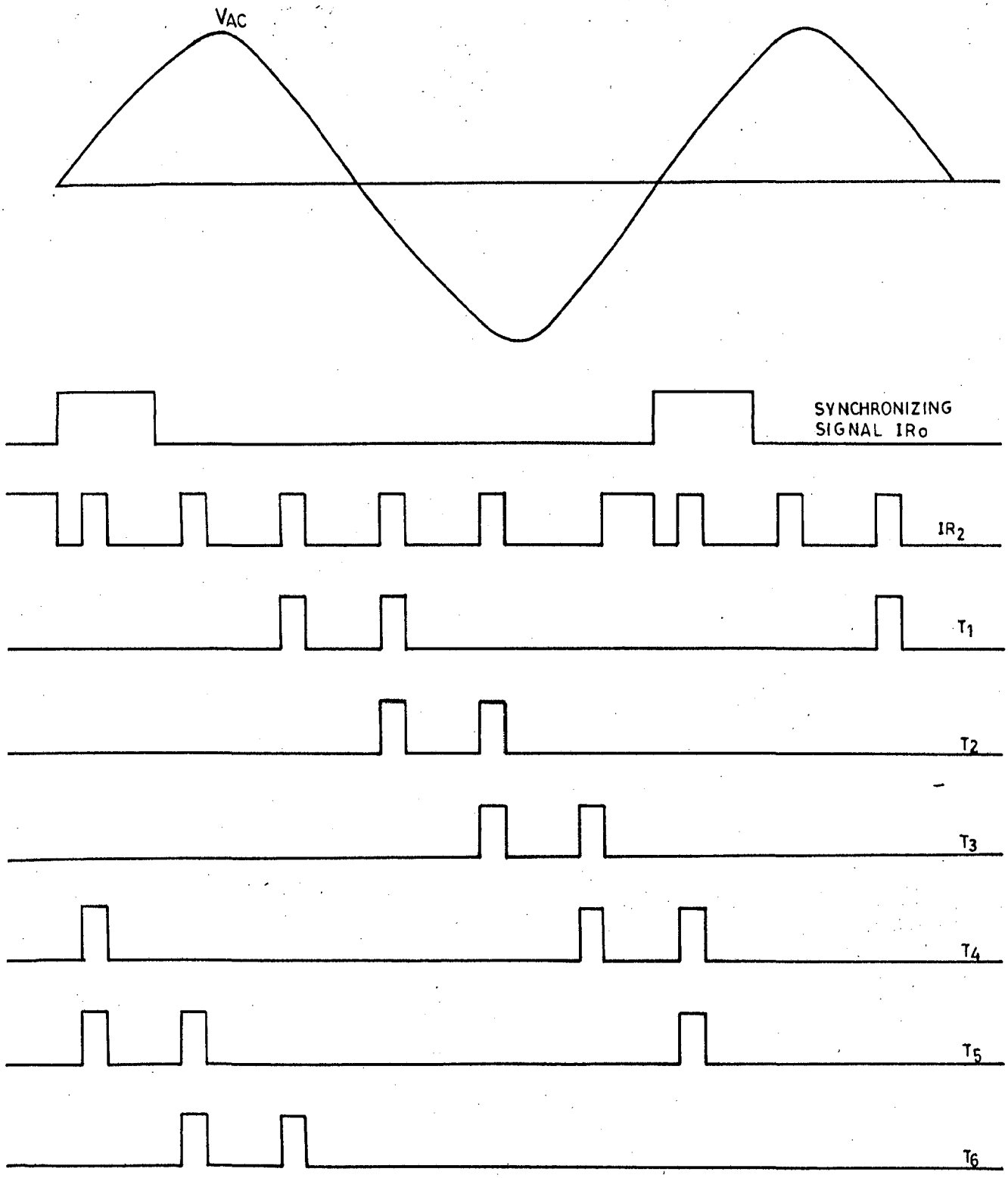


FIG. 2·8—SYNCHRONIZING SIGNAL, IR_2, FIRING PULSES IN PROPER SEQUENCE OF SIX CHANNELS

are programmed in mode 0. Counter $TM_1(2)$ is used to load $(\alpha-120^{\circ})$ count for the first time to generate firing pulses for (4,5) thyristors of the inverter and then the same counter $TM_1(2)$ is used to load 60° count to generate firing pulses for the other next five pairs of thyristors of the inverter. Counter $TM_0(2)$ is used to load $T_{ON}/(T_{OFF})$ period in mode 0, at the clock frequency of 1.535 MHz to fire the auxiliary and main thyristors of the chopper accordingly. ADC 0809 is interfaced to the microprocessor through port B and port C of 8255A. ADC provides information about duty cycle of the chopper. The duty cycle can be changed linearly by varying analog input to the ADC through a 4.7K pot connected in series to a 8.2 K resistor. The firing pulses for the Thyristors are outputted through port A of 8255A as per the firing command word. The output of counter $TM_1(2)$, synchronizing signal and generation of firing pulses are shown in Fig. 2.8. The duration of firing pulses generated by the microcomputer via 8255A is very small. The firing pulse duration is increased to 0.72 m seconds through a monostable multivibrator circuit. These firing pulses are amplified using a pulse amplifier circuit which is described in the following section.

2.4 POWER AMPLIFIER CIRCUIT

Fig. 2.9 shows the power amplifier circuit for one channel. It consists of

(a) Monostable multivibrator

(b) Oscillator

(c) AND gate

(d) Pulse amplifier.

(a) Monostable multivibrator

An output pulse of 0.73 in seconds width is produced by a 74123 retriggerable monostable multibrator. This pulse width is decided by the externally connected R and C which is given by the formula

$$T_w = 0.33\ Rc$$

where, R and C are selected as 22 K ohm and 0.1 uF.

(b) Oscillator

IC 555 timer is used as oscillator. The frequency of timer is given by

$$f = \frac{1.44}{(R_A + 2R_B)\ CT}$$

where

R_A = 1K, R_B = 4.7 K and CT = 0.01 uF which gives a frequency of 14 KHz.

(c) AND gate

The output pulses from the monostable multivibrator are at low frequency, hence they are ANDed with a high frequency modulating signal obtained from IC 555 oscillator with a frequency of 14 KHz. This prevents the saturation of pulse transformer in the pulse amplifier circuit.

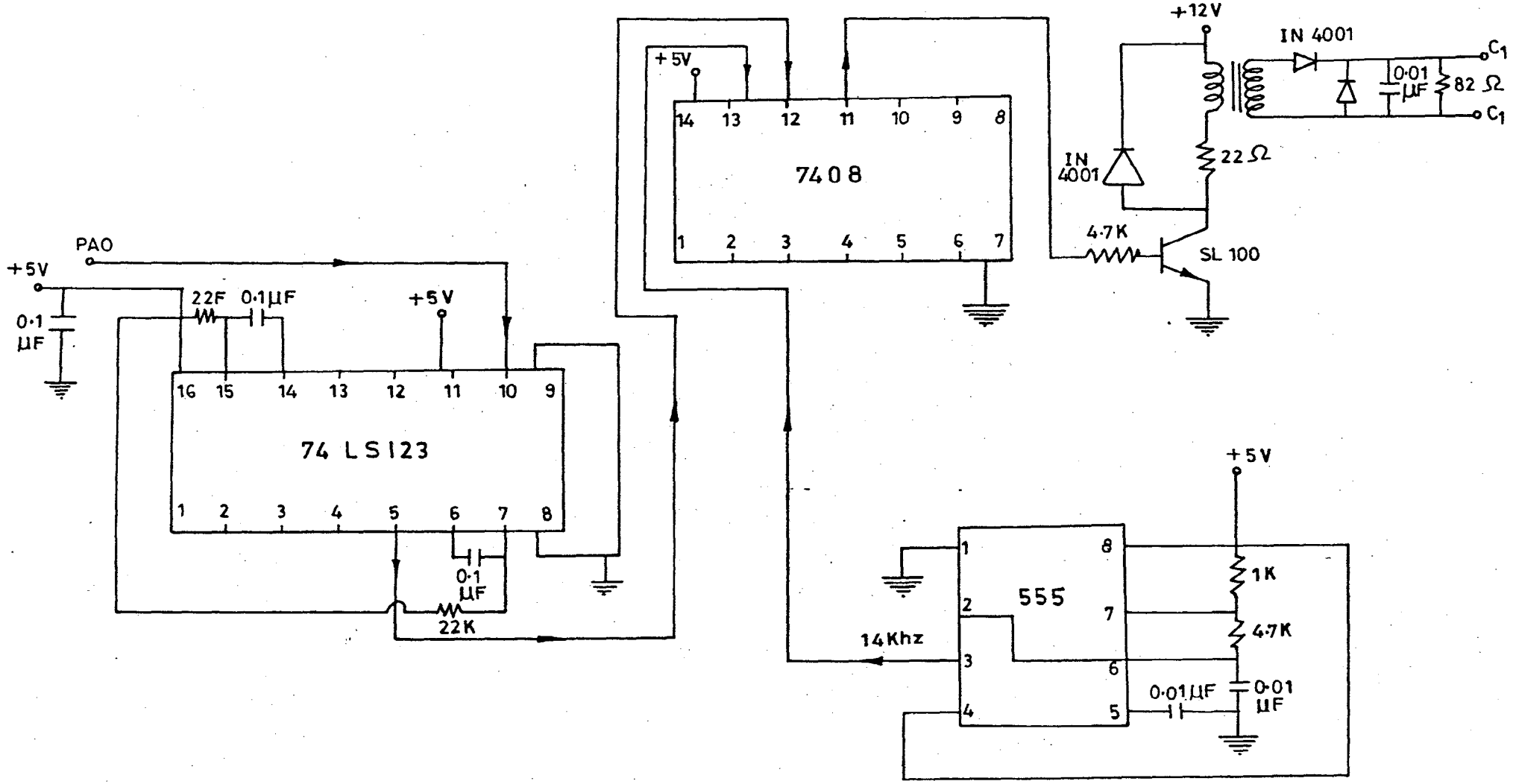


FIG. 2·9 — PULSE AMPLIFIER CIRCUIT FOR ONE CHANNEL

(d) Pulse amplifier

The strength of the AND gate output pulses is amplified using the pulse amplifier circuit. A pulse transformer is used for electrical isolation between control circuit and power circuit as shown in Fig. 2.9. The diode across the primary windings of the transformer avoids the saturation of the pulse transformer, and also protects the transistor. A diode in series with the secondary winding blocks the negative pulse. A diode across the secondary of the transormer protects the gate of the thyristor from long reverse voltages. The capacitor across the secondary prevents any spurious high frequency from triggering the thyristors.

2.5 INTERFACING OF PROGRAMMABLE INTERVAL TIMER8253A

Fig. 2.10 shows the interfacing of PIT 8253A. It consists of a 3 line to 8 line decoder 74LS138 which derives the the chip select $\overline{CS}$ signal to 8253A. The select inputs A_0 and A_1 are connected to the A_0 and A_1 address bus signals of the CPU respectively. $\overline{RD}$, $\overline{WR}$ and $I_O/\overline{M}$ control signals are derived directly from the control bus of the microprocessor. The port addresses for the 8253A are selected as under.

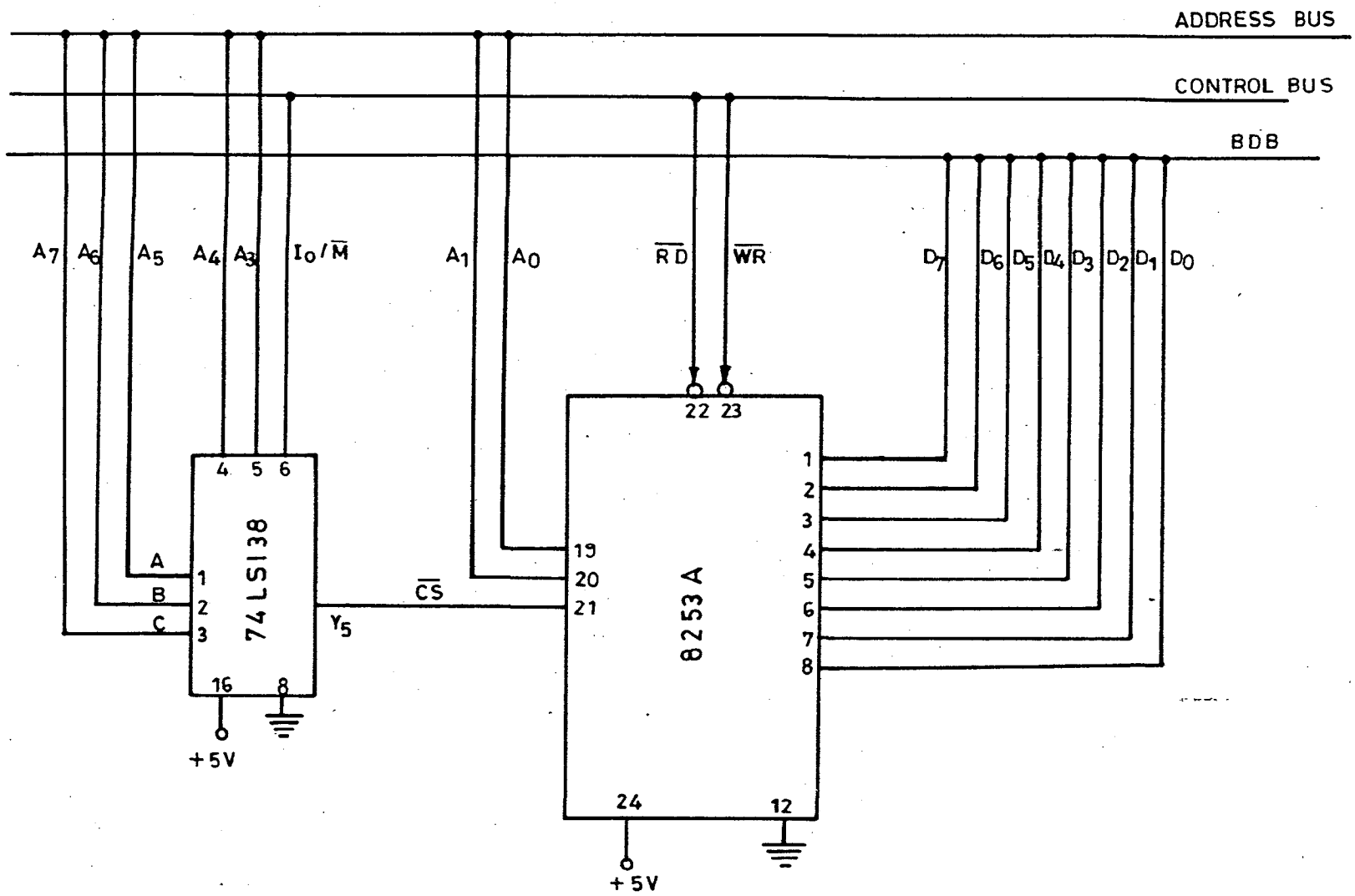


FIG. 2·10 — INTERFACING OF PIT — 8253 A

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	0	1	0	0	0	0	0	A_0	TM_0
1	00	1	0	0	0	0	1	A_1	TM_1
1	0	1	0	0	0	1	0	A_2	TM_2
1	0	1	0	0	0	1	1	A_3	CONTROL WORD
1	0	1	0	0	1	0	0	A_4	TM_0
1	0	1	0	0	1	0	1	A_5	TM_1
1	0	1	0	0	1	1	0	A_6	TM_2
1	0	1	0	0	1	1	1	A_7	CONTROL WORD

Thus the interfacing circuit meets the requirement of the extra counters other than from the µP 8085 system.

2.6 INTER FACING OF ADC CIRCUIT

Fig. 2.11 shows ADC 0809 interfacing circuit. The ADC 0809 is an 8 bit A/D converter with 8 channel multiplexer operating with a single +5 volts d.c. An analog input of 4.7 K potential divider connected in series to a 8.2 K resistor is connected to IN0 of ADC. A suitable clock of 125 KHz for conversion time is obtained from an oscillator IC 555. The firing pulses for the thyristors are outputted through port A of 8255A as per firing command word. The duty cycle of chopper can be changed linearly by varying the analog input to the ADC. The details of pin configuration of 0809 is given in Appendix - I.

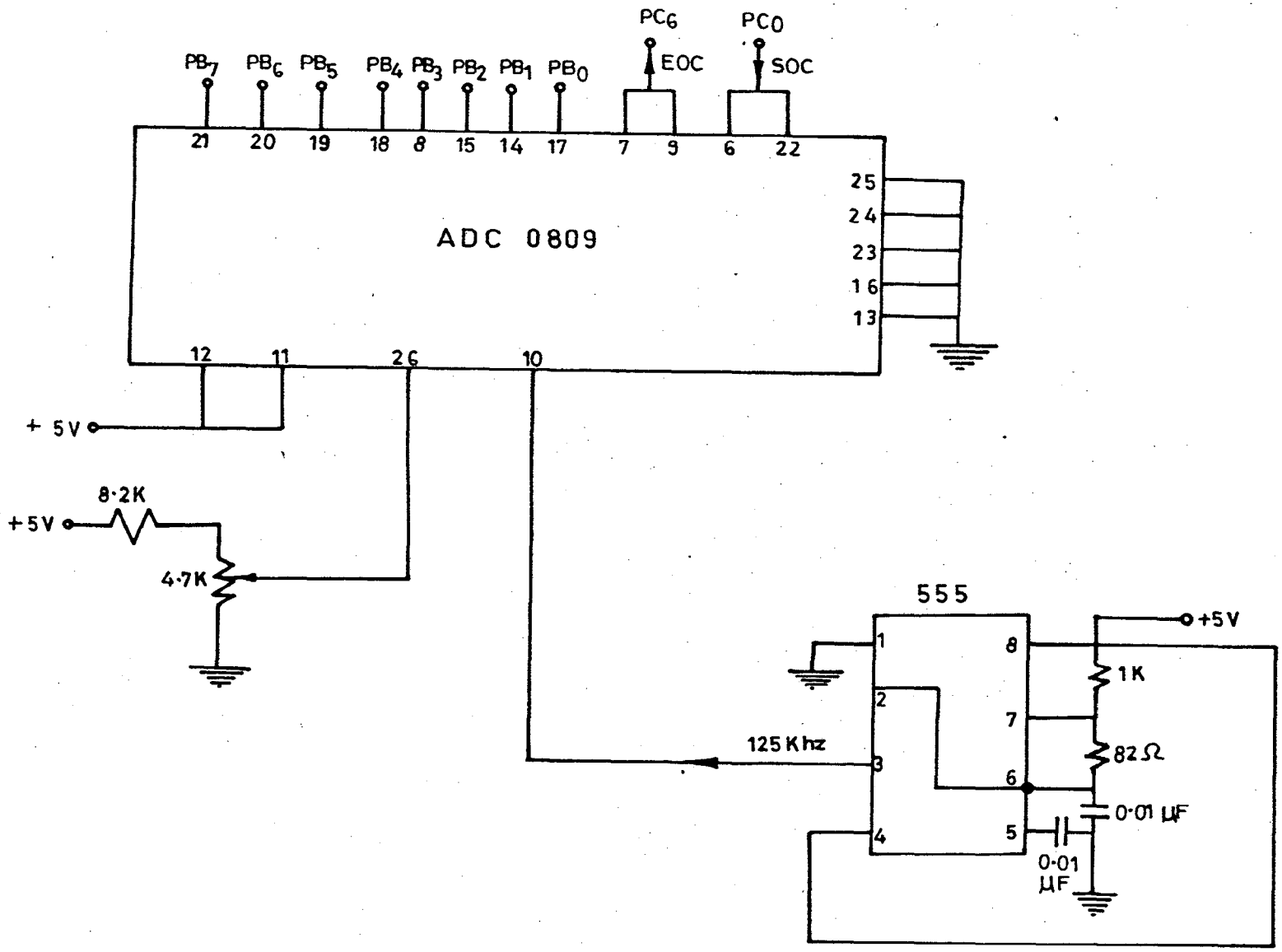


FIG. 2·11—INTERFACING OF 0809 ADC

2.7 DESIGN OF POWER CIRCUIT

The power circuit for the proposed scheme consists of the following parts.

i. Three-phase diode bridge.

ii. Three-phase fully controlled LCI.

iii. D.C.chopper

iv. D.C.LINK inductor

The design ratings of SCRs and diodes for the bridges must be such that they should not be exceeded when maximum power is being delivered by the circuit.

i. Choice of ratings of rectifier bridge diodes.

The power circuit has been designed to supply an active load of I_{RMS} = 10 A. at voltage = 400V input to the bridge rectifier. Thus the d.c. link current for this a.c. current can be obtained from

$$I_{RMS} = 1.22\ I\ dc$$

$$\therefore I_{DC} = 0.816\ I_{RMS}$$

$$I_{DC} = 8.16\ A$$

The voltage rating of diodes of the uncontrolled bridge have to be selected with the considerations of the peak inverse voltage appearing across the devices, this in turn depends upon the maximum three phase input line voltage to the bridge.

Therefore the PIV across each diode is

$$V_{PIV} = \frac{\pi}{3} \times \frac{3\sqrt{6}}{\pi} V_{LN}$$

$$= 2.45\ V_{LN}$$

$$V_{PIV} = 2.45 \times \frac{400}{\sqrt{3}} = 566\ V$$

A safety factor of 2 is kept, so that the diodes can easily take reasonable over voltages. Thus the diodes of rating 16A, 1200 PIV can be selected to meet the requirements.

(ii) Selection of rating of thyristors

For a 3-phase bridge the ratio of PIV and line to neutral voltages is given by

$$\frac{E_{PIV}}{E_{LN}} = 2.45$$

$$E_{PIV} = 2.45 \times E_{LN} = 2.45 \times \frac{400}{\sqrt{3}}$$

$$= 566\ V$$

As the rated current of a synchronous motor is 10A, we have

$$\frac{I_{RMS}}{I_{DC}} = 1.22$$

$$\therefore I_{DC} = 0.816 \times 10 = 8.16\ A$$

Allowing a safety factor 2, a rating of 16A, 1200 P_{IV} can be used.

(iii) Selection of commutating capacitor and Inductor of chopper.

The rated rotor voltages of the WRIM = 140 V.

Rated rotor current = 22A.

At rectifier output the voltage = 1.35 x 140

= 189 V

and I_{dc} the current = 1.28 x 22

= 28 A

Taking Turn off time = 20 micro secs

$$C = \frac{2I_{dc}\ T_{OFF}}{V_R}$$

where V_R= average value for rectified slip voltage

$$V_R = \frac{189 + \frac{189}{2}}{2} = 141.75 \text{ V}$$

$\therefore C = 7.9$ micro. F $\simeq$ 8 micro.F.

$$V_R \propto \sqrt{C/L} = \frac{I_{dc}}{2}$$

$\therefore L = 0.81$ mH

Hence a capacitor of 8 micro Farads and an inductor of 0.81 milli Henry are used in the auxiliary circuit of voltage commutated chopper.

2.8 CONCLUSIONS

The details of the microprocessor based firing control scheme for the inverter bridge and the firing pulses for chopper thyristors has been discussed in this chapter. The design of power circuit and synchronising circuit are also developed. The interfacing of ADC circuit and PIT -8253A has also been described.

CHAPTER - III

IMPLEMENTATION OF SYSTEM SOFTWARE AND FLOWCHARTS

3.1 GENERAL

In this chapter, mainly, the development of system software and flowcharts is described. The complete logic of the control scheme is discussed in the main program routine. The other subroutines along with the main programme are also given in this chapter.

3.2 MAIN PROGRAM ROUTINE

The flow chart for the main program is shown in Fig. 3.1. The program is started with the initialization of programmable peripheral devices in suitable mode according to the requirements for the present scheme. The port A of 8255A (the programmable peripheral interface) is programmed in output mode for outputting the firing pulses as per the firing command word. The port B is the input mode for inputting the data from ADC output. The port CL is in output mode and port Cu is in input mode.

In the uP 8085 system, two counters of programmable interval timer (PIT-8253A) are available for the user through connector J_1. Counter $TM_1(1)$ is programmed in mode 2 for generating the clock of 511.67 KHz by using the clock of 1.535 MHz and all the other counters are in mode (0.) $TM_2(1)$ is used for providing count corresponding to 60° with a clock of 511.67 KHz.

$T_{MO}(2)$ of the interfaced PIT -8253A is used for providing T_{ON} C and T_{OFFC} for the chopper and $TM_1(2)$ is used for providing count for 30° initially and then count for 60° delay to generate the firing pulses in sequence with 60° delay for inverter thyristors. The output of $TM_1(2)$ and $TM_0(2)$ are used as IR_2 and IR_5 interrupt request for gene - rating the firing pulses.

The programmable interrupt controller (PIC -8259A) is initialized in fully nested mode, in which IRo has the highest priority and IR_7 has the lowest priority. In the present scheme three interrupt lines IR_o, IR_2 and IR_5 are used.

After the initialization of 8253(1), the $TM_1(1)$ is loaded with a count 03H to generate a clock of 511.67 KHz. Continuously. The microprocessor checks the status of the synchronizing signal imported through PC_7. If it is found to be low then FFFF H is loaded into the $TM_2(1)$. The synchronizing signal is also inputted continuously to the Gate of $TM_2(1)$ and counting becomes enable as soon as the digitized signal goes to high. The counter starts decrementing the count value (FFFF H) as long as the synchronizing signal remains high and counting becomes disable as soon as the synchronizing signal goes to low. Now the count value for 60° duration of terminal voltage of synchronous machine is calculated. Then the 30° count value is calculated and loaded in to the $TM_1(2)$ whose gate is made permanently high. After

calculating the count for 60° and 30°, the programme jumps to ADC subroutine. ADC converts a particular analog input to it through the channel IN_0 into its equivalent digital signal and this output is stored in the memory location address (Add 6). This digital output contains the information about the duty cycle of the chopper. Next, the programme moves to multiplication subroutine. In this subroutine the value of K in hexadecimal is multiplied by the ADC output for calculation of TON_c and T_{OFFc} as shown below.

$$T_{ON_c} = ADC \times K \tag{3.1}$$

where $$K = \frac{1}{f_{CH}} \times \frac{\text{clock frequency}}{100}$$

$$K = \frac{1}{300} \times \frac{1.5 \times 10^6}{100}$$

$$K = (50)_{10} = (32)_H \tag{3.2}$$

$$T_{OFF_c} = (64_H - ADC)\ K \tag{3.3}$$

where the frequency of the chopper

f_{CH} is considered as 300 hz.

The equation (3.1) and (3.3) clearly indicates that by varying analog input to the ADC, the duty cycle of the chopper can be controlled easily during the operation of the system. After calculating the T_{ON_c} and T_{OFF_c} the interrupt system is made enable and $TM_0(2)$ is loaded initially with T_{OFF_c} to generate IR_5 interrupt. Then the microprocessor waits in the Halt state for the interrupt signal IR_5, as only IR_5 is unmasked in the begining, when IR_5 is saved the programme

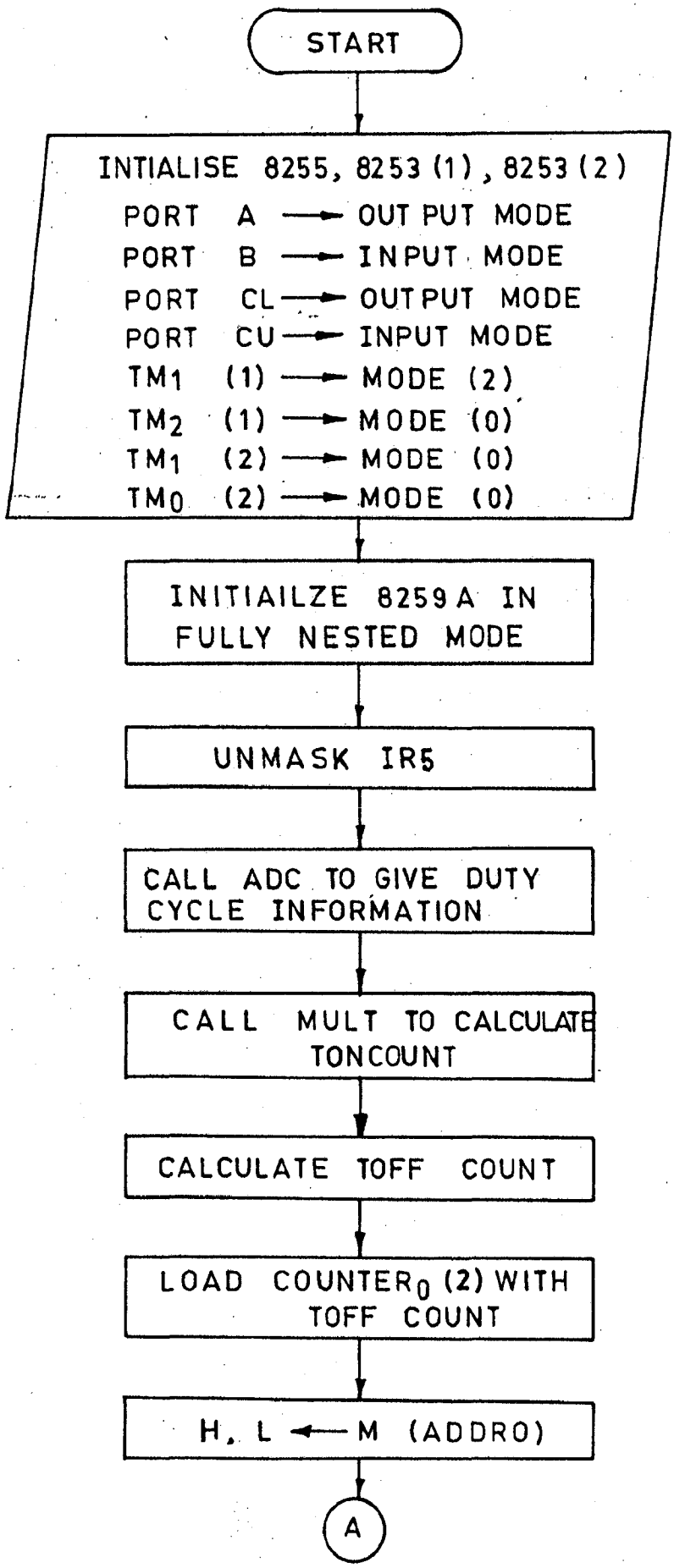


FIG. 3·1 — FLOW CHART FOR MAIN PROGRAM

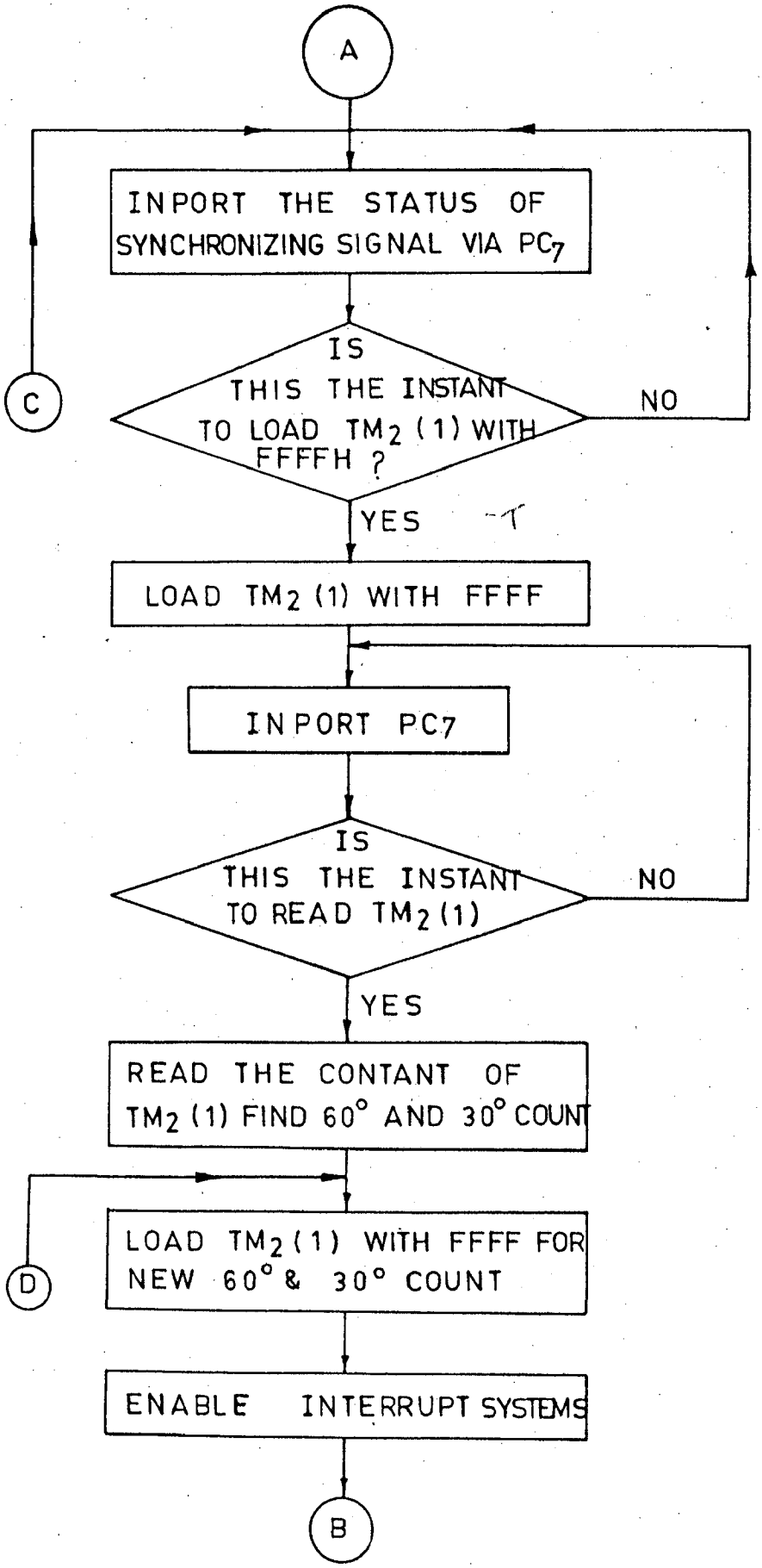

A
INPORT THE STATUS OF SYNCHRONIZING SIGNAL VIA PC7
IS THIS THE INSTANT TO LOAD TM2 (1) WITH FFFFH ?
NO
C
YES
LOAD TM2 (1) WITH FFFF
INPORT PC7
IS THIS THE INSTANT TO READ TM2 (1)
NO
YES
READ THE CONTANT OF TM2 (1) FIND 60° AND 30° COUNT
LOAD TM2 (1) WITH FFFF FOR NEW 60° & 30° COUNT
D
ENABLE INTERRUPT SYSTEMS
B

FIG. 3·1— CONTD.

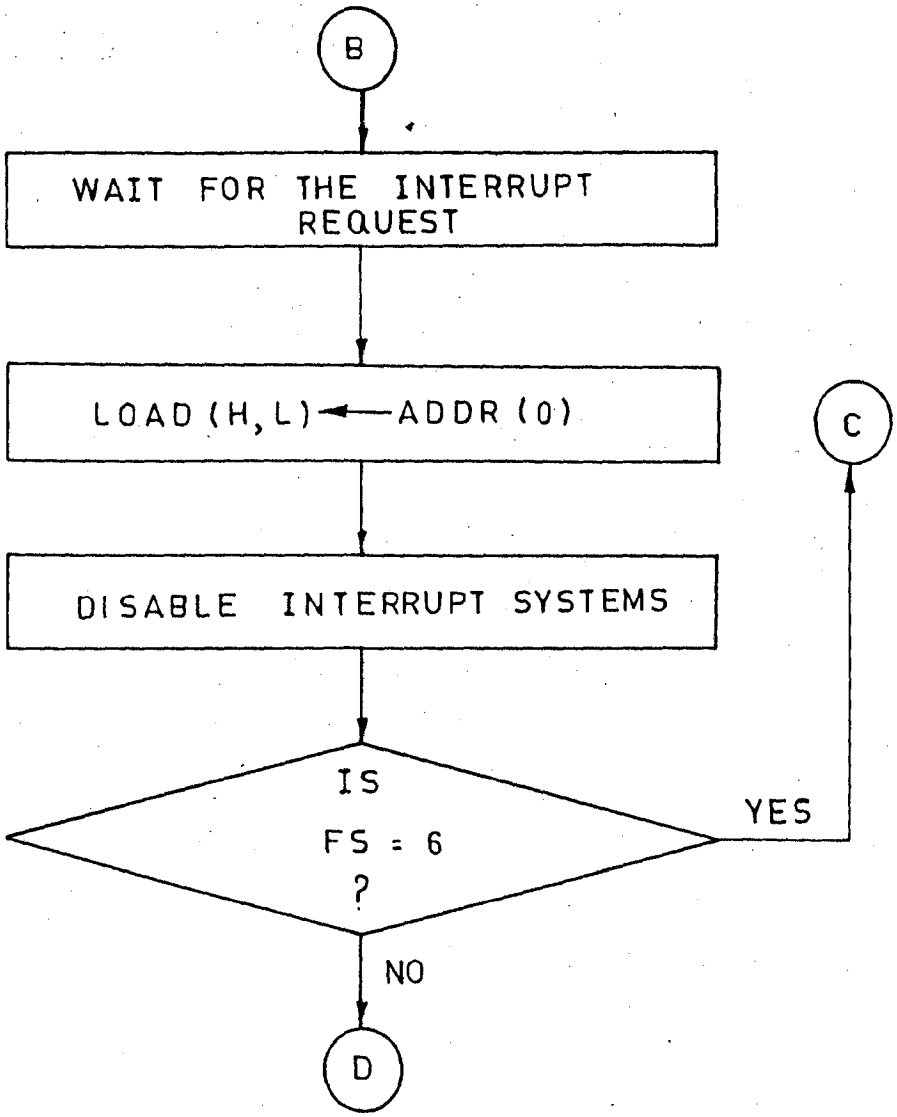

B
WAIT FOR THE INTERRUPT REQUEST
LOAD (H, L) ← ADDR (0)
C
DISABLE INTERRUPT SYSTEMS
IS FS = 6 ?
YES
NO
D

FIG. 3·1—CONTD.

moves to enable IRo interrupt as IRo, IR_2 and IR_5 are unmasked. After all the interrupts are served, the interrupt system is made disabled and the firing sequence is tested. If the firing sequence '6' is over then the microprocessor reads the content of $counter_2$(1) for new 60^o and 30^o count and goes to Halt state after enabling interrupt system.

3.3 ADC SUBROUTINE

This subroutine is used to provide duty cycle infor - mation for the chopper. This is executed once in every cycle of the machine frequency. ADC converts the analog input to its digital equivalent at the instant, when the start of conversion (SOC) bit of ADC goes from low to high. SOC pulse is issued by the microprocessor through PC_0 bit of 8255A. The duty cycle can be changed by varying the analog input to ADC through a potential divider. The flow chart for ADC subroutine is shown in Fig. 3.2. ADC clock in is given from an oscillator developed with 555 timer at 125 KHz. The digital output is stored in memory location Add 6 and displayed in data field by the microprocessor.

3.4 MULT SUBROUTINE

The flow chart for MULT subroutine is shown in Fig.3.3. In this subroutine the value of K is multiplied by the digital output of the ADC for T_{ONc} and (64H - ADC) for T_{OFFc}. The register pair (DE) contains the multiplicand which is the value of the K = 32H corresponding to the clock of 1.535 MHz. Register B contains the multiplier and Register C

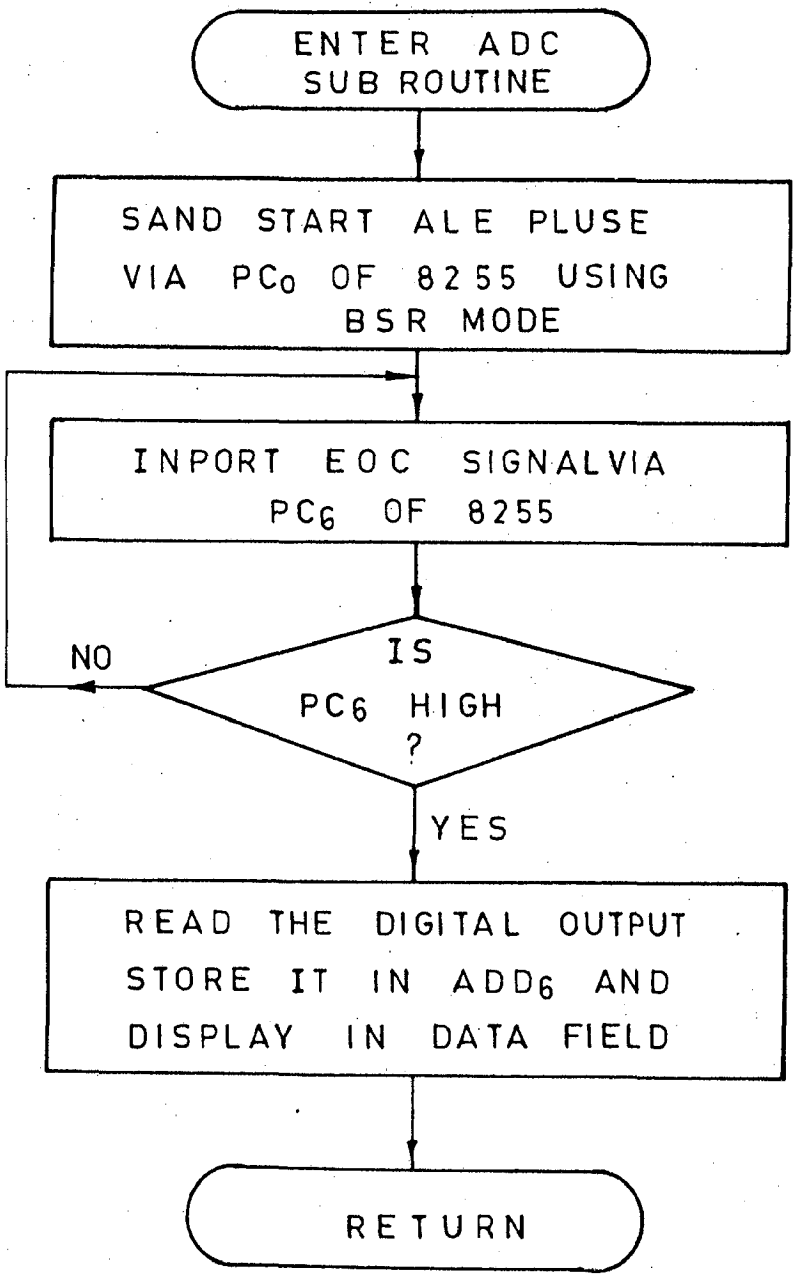


FIG. 3·2—FLOW CHART FOR ADC SUBROUTINE

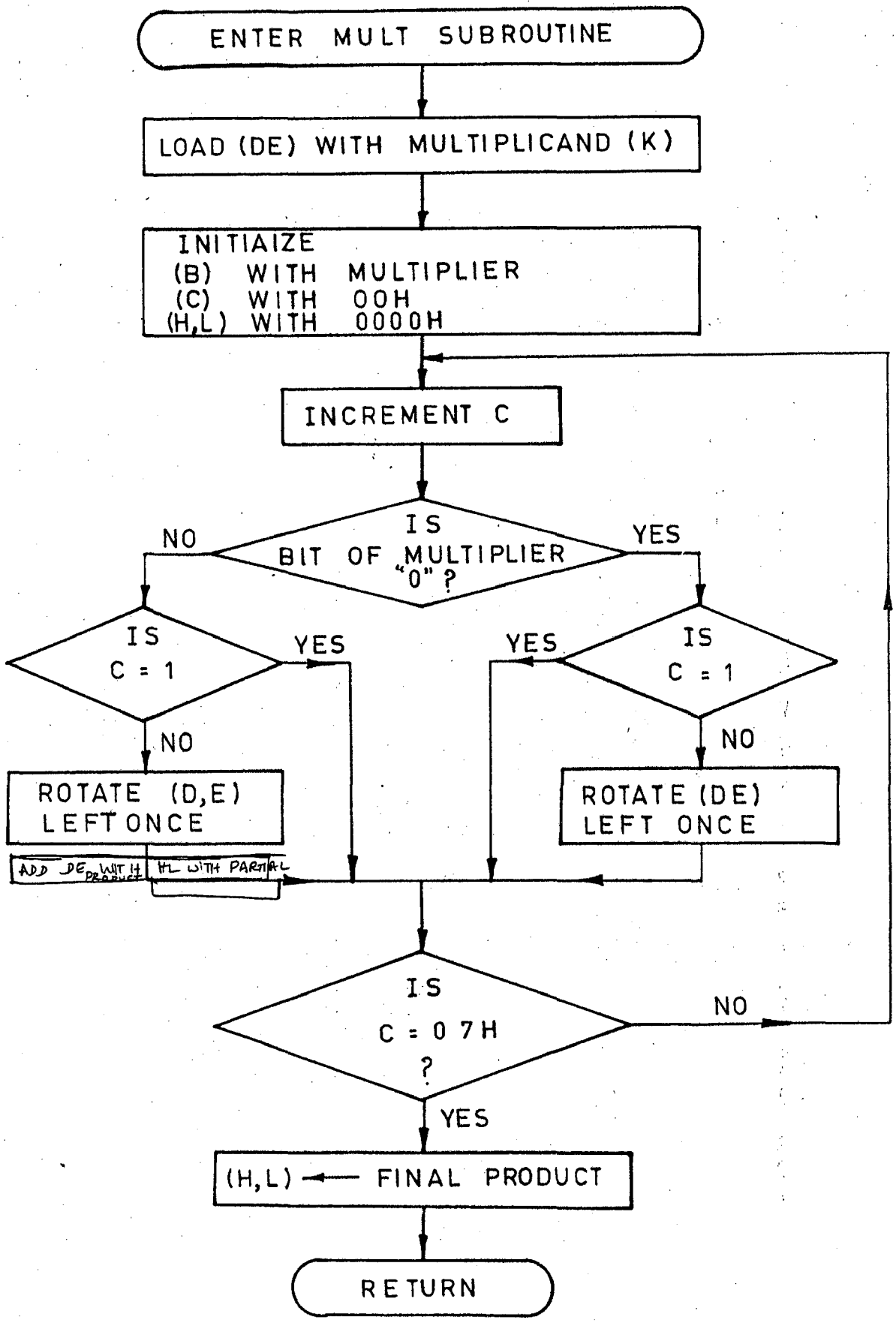


FIG. 3·3— FLOW CHART FOR MULT SUB ROUTINE

is used to indicate the bit position of multiplier. Register pair HL will contain the partial product or final product. Since the binary digits may be either 1 or 0, the multiplier may be examined on a bit by bit basis for 1 or 0, starting from right to left. If a 1 is found the multiplicand is shifted in proper position and added to the accumulating result. If a 0 is found nothing is added to the partial product. In the present case all bits of multiplier are to be tested and the product is stored in HL pair.

3.5 IRO INTERRUPT SUBROUTINE

Fig. 3.4 shows the flow chart of IR_0 interrupt service subroutine. In this subroutine 30^0 count corresponding to 511.67 KHz. is loaded in to the $counter_1(2)$ to trigger the (4,5) pair of thyristors of the load commutated inverter. The $TM_1(2)$ is loaded with a count for 30^0 once in every cycle. Counter output goes high on the terminal count and this output is used as IR_2 interrupt request input. The microprocessor enables the interrupt systems at the end of subroutine before returning to the main programme.

3.6 IR_2 INTERRUPT SUBROUTINE

Fig. 3.5 shows the flow chart for IR_2 service routine. HL is loaded directly with the firing command address to point the correct address to fire (4,5) thyristor pair and incremented with a count for 60^0 delay loaded in the same

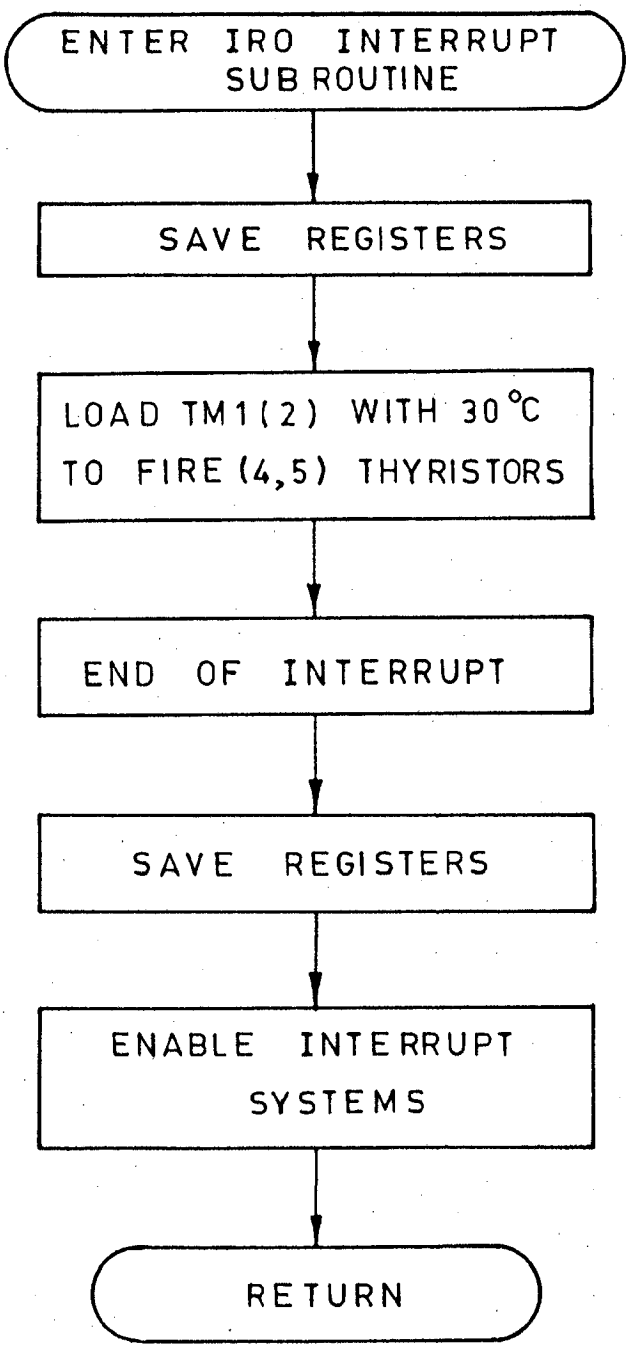


FIG. 3·4 — FLOW CHART FOR IRO INTERRUPT SERVICE ROUTINE

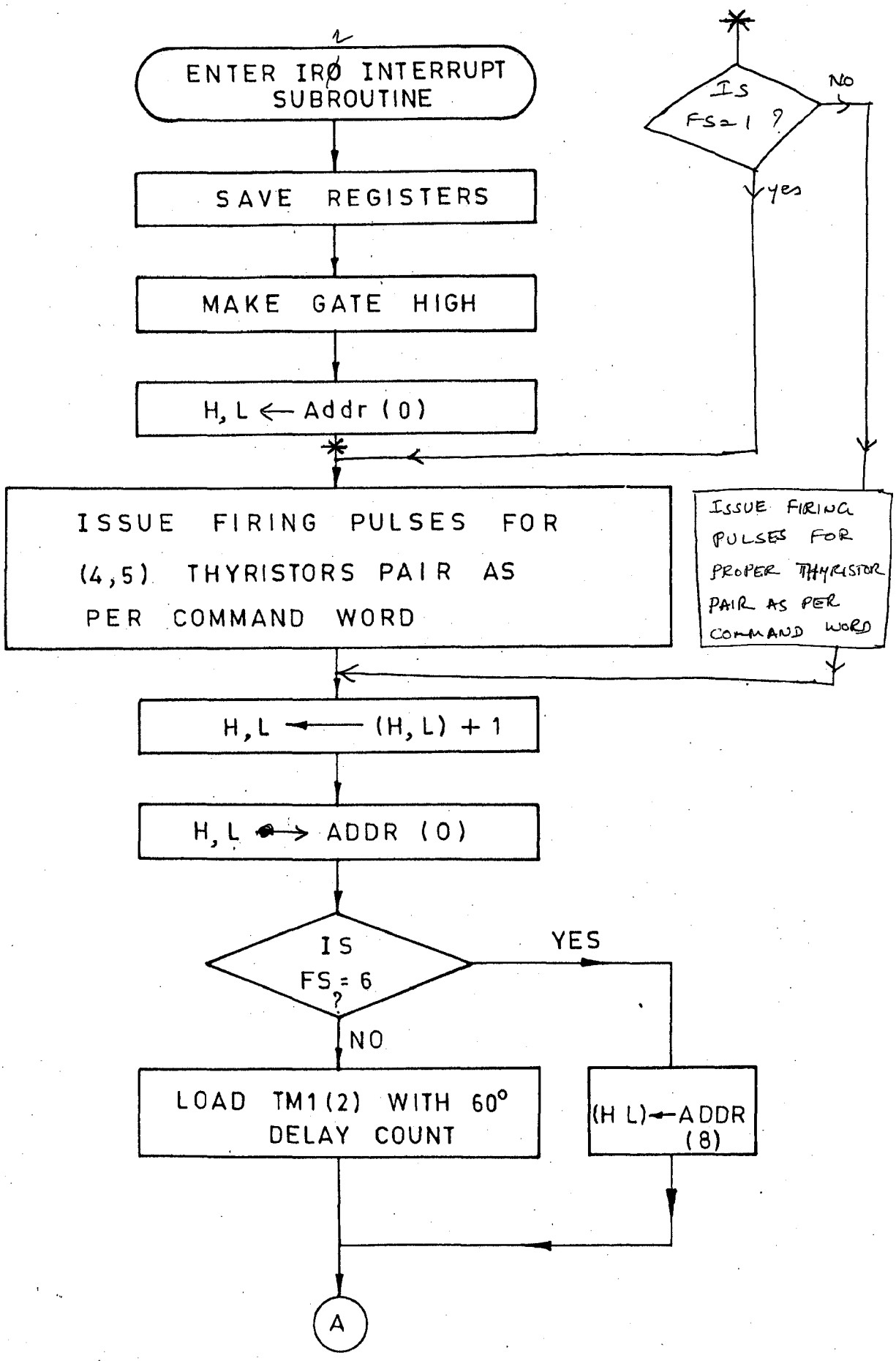


FIG. 3·5 — FLOW CHART FOR IR2 INTERRUPT SUBROUTINE

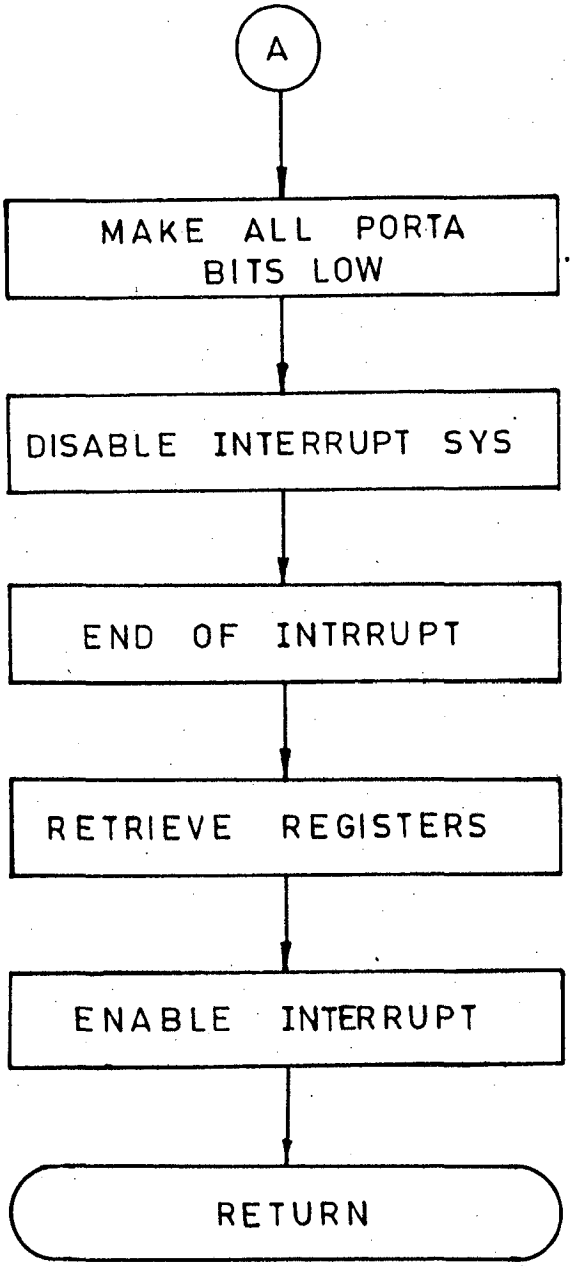

A
MAKE ALL PORTA BITS LOW
DISABLE INTERRUPT SYS
END OF INTRRUPT
RETRIEVE REGISTERS
ENABLE INTERRUPT
RETURN

FIG.3·5 – CONTD.

$TM_1(2)$. Then the firing sequence 6 is over, then HL is reloaded with the starting address of the firing command table. The microprocessor retrieves the registers and enables interrupt systems at the end of the subroutine before retur - ning to the interrupted programme.

3.7 IR_5 INTERRUPT SUBROUTINE

Fig. 3.6 shows the flow chart for IR_5 interrupt sub-routine. This subroutine is used to generate firing pulses for the main and auxiliary thyristors of the chopper. At the begining of the subroutine, the registers are saved and firing index (FI) is checked for 00. If it is 00, the auxiliary thyristor is fired by loading the $TM_0(2)$ with $T_{OFF\ c}$. If the (FI) is found to be 01 then the main thyristor is fired by loading $TM_0(2)$ with $T_{ON\ c}$ and making the particular bit high. The $TM_0(2)$ is loaded once with $T_{OFF\ c}$ and next with T_{ONc} once in every cucle. The microprocessor retrieves the registers and enables the interrupt system after calculating the new $T_{ON\ c}$ and T_{OFFC} for the next cycle before retrieving to the interrupted main programme. The output of $TM_0(2)$ on the terminal count is used as IR_5 interrupt request.

3.8 CONCLUSIONS

In this chapter the main program with various sub - routines have been discussed in detail.

Subroutines discussed are ADC, MULT, IR_0, IR_2 and IR_5 subroutines.

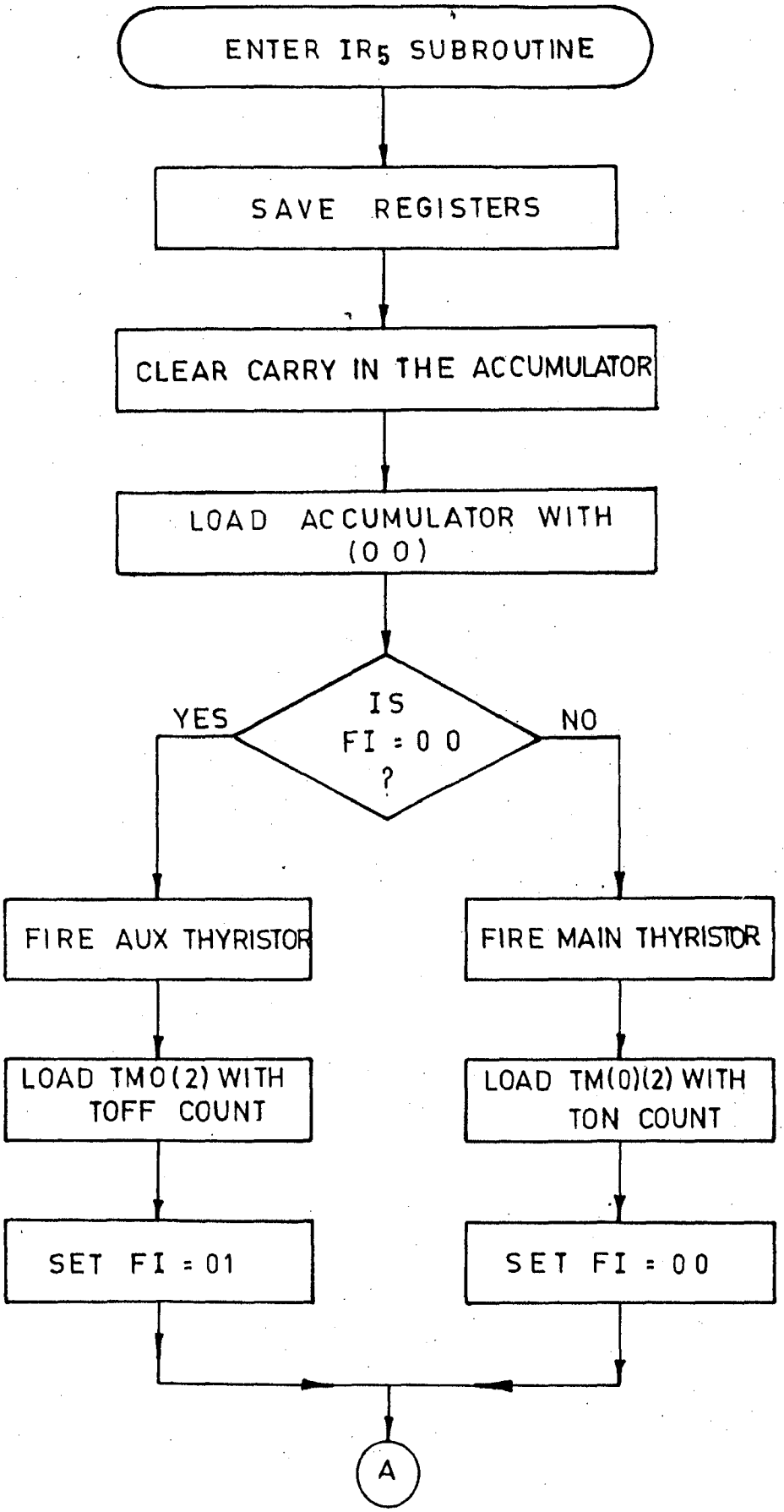


FIG. 3·6-FLOW CHART FOR IR5 INTERRUPT SUBROUTNE

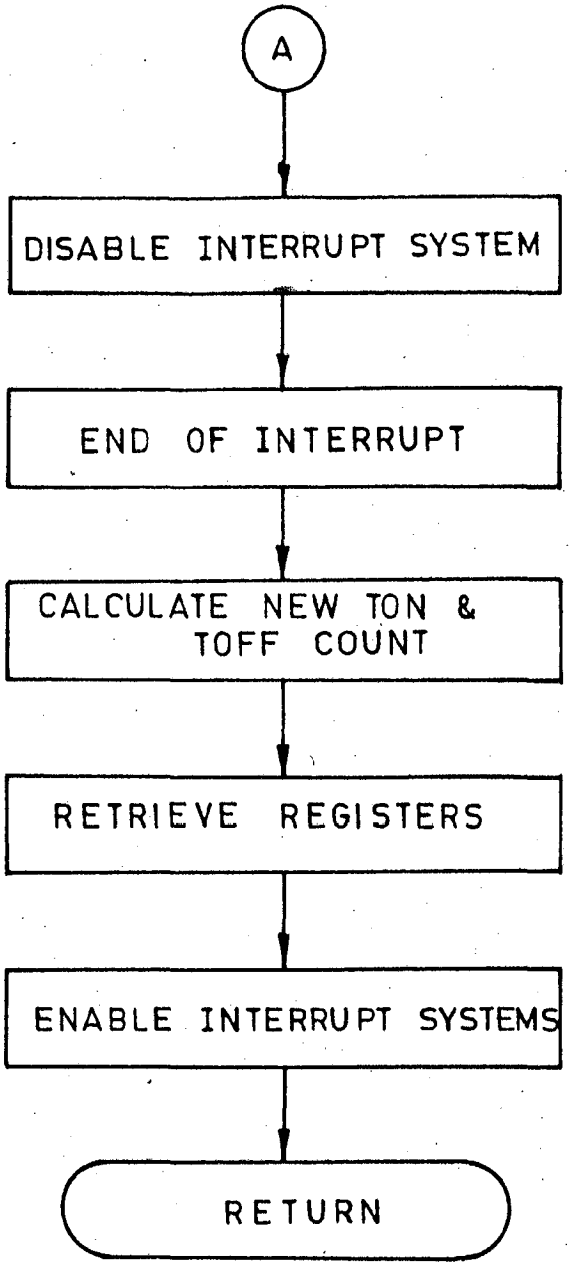

A
DISABLE INTERRUPT SYSTEM
END OF INTERRUPT
CALCULATE NEW TON &
TOFF COUNT
RETRIEVE REGISTERS
ENABLE INTERRUPT SYSTEMS
RETURN

FIG. 3·6–CONTD.

ADC subroutine provides the duty cycle information for the chopper. MULT subroutine performs the calculations for $T_{ON\ c}$ and T_{OFFc}. IR_0 interrupt subroutine is used to load the $TM_1(2)$ with a count for 30^0 and IR_2 interrupt subroutine is used to generate the firing pulses for the thyristor of inverter in proper sequence with a count of 60^0 delay. IR_5 interrupt subroutine is used to generate the firing pulses for the main and auxiliary thyristors of chopper by loading the $TM_0(2)$ with $T_{ON\ c}$ and $T_{OFF\ c}$ respectively.

The main routine and various software subroutine programs have been tested individually and altogether on microprocessor 8085 based system for implementing the present scheme.

CHAPTER - IV

STEADY STATE PERFORMANCE OF THE DRIVE SYSTEM

4.1 GENERAL

This chapter deals with the experimental studies on the microprocessor based chopper controlled commutatorless Kramer drive. The steady state performance of this drive system have been studied on no load and on load. The speed control is obtained by varying the field current and duty cycle of the chopper. The oscillograms of the induction machine terminal voltage, stator current, d.c. link voltage and current, synchronous machine voltage and current and voltage waveforms at different points of the firing control circuit are also given.

4.2 EXPERIMENTAL INVESTIGATIONS

The main objective of the experimental investigations is to study the steady state performance characteristics of the chopper controlled commutatorless Kramer drive. The details of the machines used in the system i.e. the induction motor, synchronous motor and d.c. generator used for loading are given in Appendix-I. To obtain the steady state performance of the drive system, the various tests have been performed on no load and on load.

4.2.1 Starting of the chopper controlled commutatorless Kramer drive

Under stand still conditions, synchronous machine terminal voltage is zero and therefore firing pulse generation for load commutated inverter (LCI) is not possible. The d.c. supply is given to the field of the synchronous machine and it is run as a generator by means of the wound rotor Induction motor by closing switch S_1 in Fig. 4.1. The voltage induced at the stator terminals of the synchronous machine is used to generate the firing pulses for the thyristors of LCI by microprocessor. In the present work, a manual starting method shown in Fig. 4.1 is adopted. The manual method of starting chopper controlled commutatorless Kramer system involves the following steps.

(i) The induction motor is started to drive the synchronous machine as a generator at a very low speed. At low speed, the electromotive force of the synchronous machine is small. So proper synchronizing signal will not be generated from this low voltage.

(ii) A variable resistor, R shown in Fig. 4.1 is connected across the bridge rectifier to accelerate the motor upto a speed where the voltage induced at the stator terminals of the synchronous machine is sufficient to generate the firing pulses for the thyristors of the LCI by the microprocessor.

(iii) Also the firing pulses for the main and auxiliary thyristors of the chopper are generated by the microprocessor. The output voltage of the chopper is varied by varying the duty cycle of the chopper with the help of the ADC input.

(iv) The starting Rheostat R is gradually cut out from the circuit and switch S_1 is opened.

(v) The upper terminal of the D.C. link is positive and the lower one negative when sufficient power is being pushed from d.c. side to the a.c terminals of the synchronous motor (V_R becoming greater, than the V_{dc}).

(vi) A series resistor connected in series with the inductor (not shown in Fig. 4.1) is gradually reduced to the minimum value to enhance the power to the motor. This resistor is placed in the circuit to reduce the speed of operation to a value which gives sufficient slip voltage SE_2 which is necessary for commutation of the chopper.

(vii) A very low value of capacitor (not shown in Fig. 4.1) is placed at the ac terminals of the inverter bridge to improve the reactive power.

(viii) The slip power from the rotor of the wound rotor Induction motor flows from the d.c side to the synchronous motor when the bridge rectifier voltage

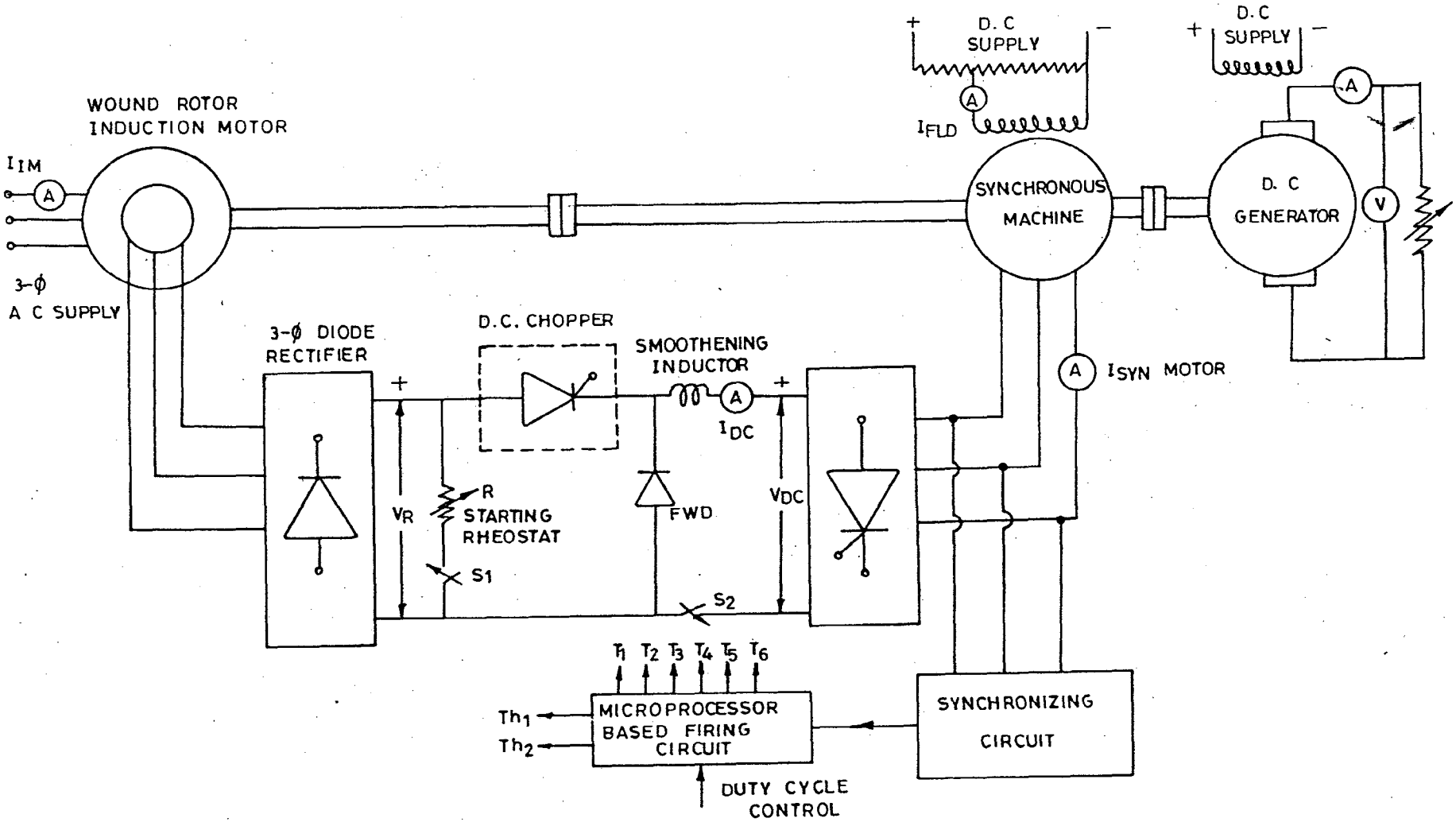


FIG. 4.1 — EXPERIMENTAL SET UP OF CHOPPER CONTROLLED COMMUTATORLESS KRAMER DRIVE

becomes greater than the inverter dc voltage thus following the Kramer operation.

4.2.2 Tests at no load

These tests are carried out by varying the chopper duty cycle with constant field current and changing field current with constant duty cycle. The firing angle of the LCI has been chosen to be 150^{o} through out the operation. From the results of no load tests the following no-load steady state characteristics are obtained.

(i) Speed vs field current for different duty cycles of the chopper.

(ii) Speed vs duty cycle of the chopper for different values of the field current.

4.2.3 Tests at load

The experimental performance under load of the commutatorless Kramer system is obtained with the help of a coupled d.c. machine running as a separately excited generator. Load test is carrie d out by varying the load on the drive system at a field current with constant duty cycle. From the experimental results the following characteristics are obtained.

(i) Speed vs load current.

(ii) Input current of the induction motor vs the load current.

(iii) Synchronous motor current vs load current.

(iv) D.C. link current vs load current.

(v) Net power output vs load current.

4.3 RESULTS AND DISCUSSIONS

The experimental characteristics of chopper controlled commutatorless Kramer drive at no load and load conditions are shown in Figs. 4.2 to 4.7. The oscillograms of the waveshapes at different points of the control circuit for inverter bridge and chopper, machine terminal voltage and current, chopper input voltage and current, chopper output voltage and current, D.C. link voltage and current after the smoothening inductor are recorded at no load and loaded conditions and are shown in Figs. 4.8 to 4.12.

The following salient features on the performance of chopper controlled commutatorless Kramer drive are observed from the results.

(i) The effect of field current on speed is shown in Fig. 4.2 for three settings of chopper duty cycle which are 20 percent, 50 percent and 80 percent. It is observed that speed falls as field current increases. Further, at a given field current setting, speed rises with increase in chopper duty cycle Fig. (4.3). The maximum speed with δ = 80 percent is seen from Fig. 4.2 to be around 1000 rpm. Normally, the speed should approach synchronous speed (1500 rpm in present case)

δ = 1.0 and I_f = 0.0. However, it is due to inclusion of a resistance in series with the d.c. link inductor. The reason for including the resistor has already been explained.

(ii) It is observed from Fig. 4.4 that the commutatorless Kramer drive exhibits similar drooping load current vs speed characteristics like a conventional d.c. motor. Also that the characteristic shifts upword as the duty cycle is increased. The load current (d.c. generator armature current) is proportional to load torque since field current of d.c. generator is kept constant. The load current is therefore chosen as independent variable in plotting the characteristic.

(iii) It is observed from the Fig.4.5 and 4.6 for duty cycle settings of 60 percent and 80 percent respectively that the variation of d.c. link current with load current is similar to the armature current vs load current characteristic of a conventional d.c. motor. D.C. link current increases almost linearly with the load current.

Synchronous motor current also shows the rising trend which is almost linear. This is expected on account of the rising trend of the d.c. link current.

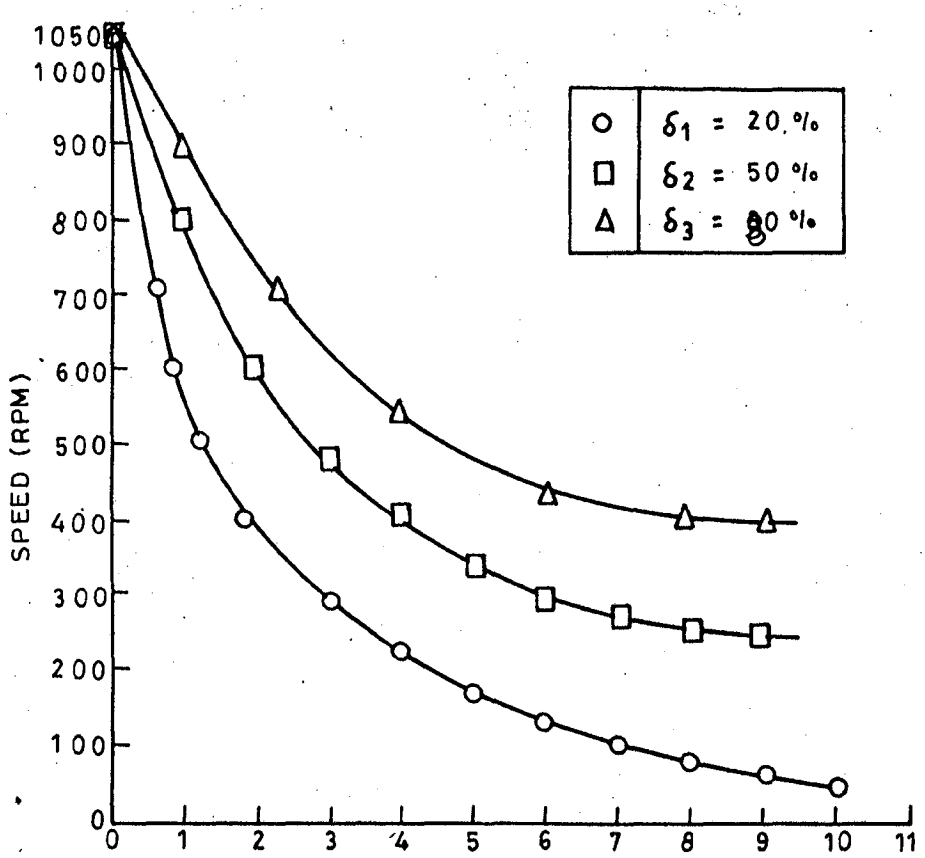


FIG. 4·2 — NO LOAD SPEED Vs FIELD CURRENT

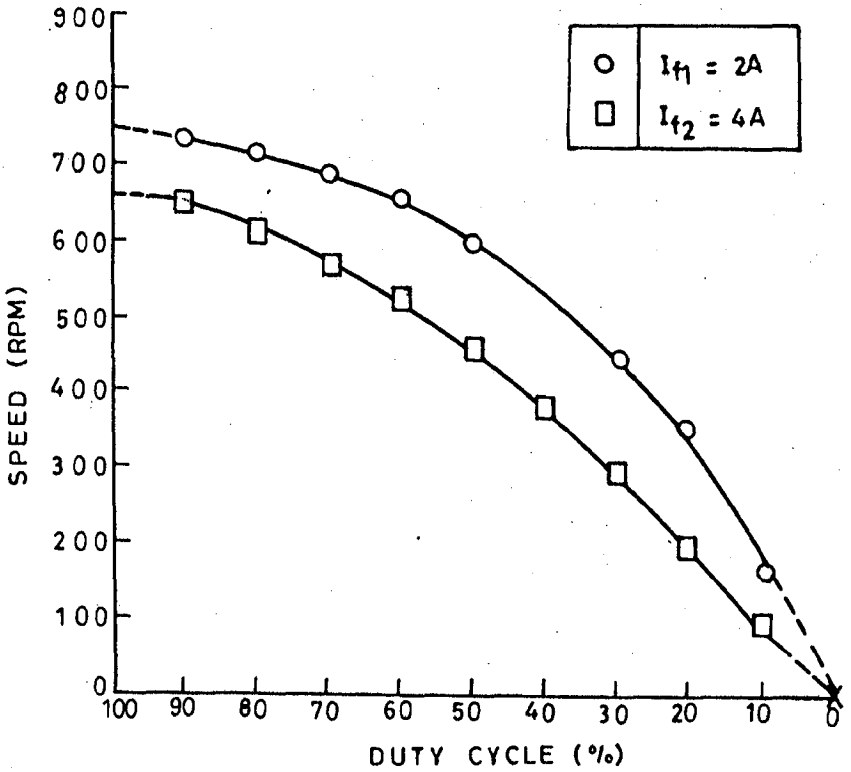


FIG. 4·3 — NO LOAD SPEED Vs DUTY CYCLE

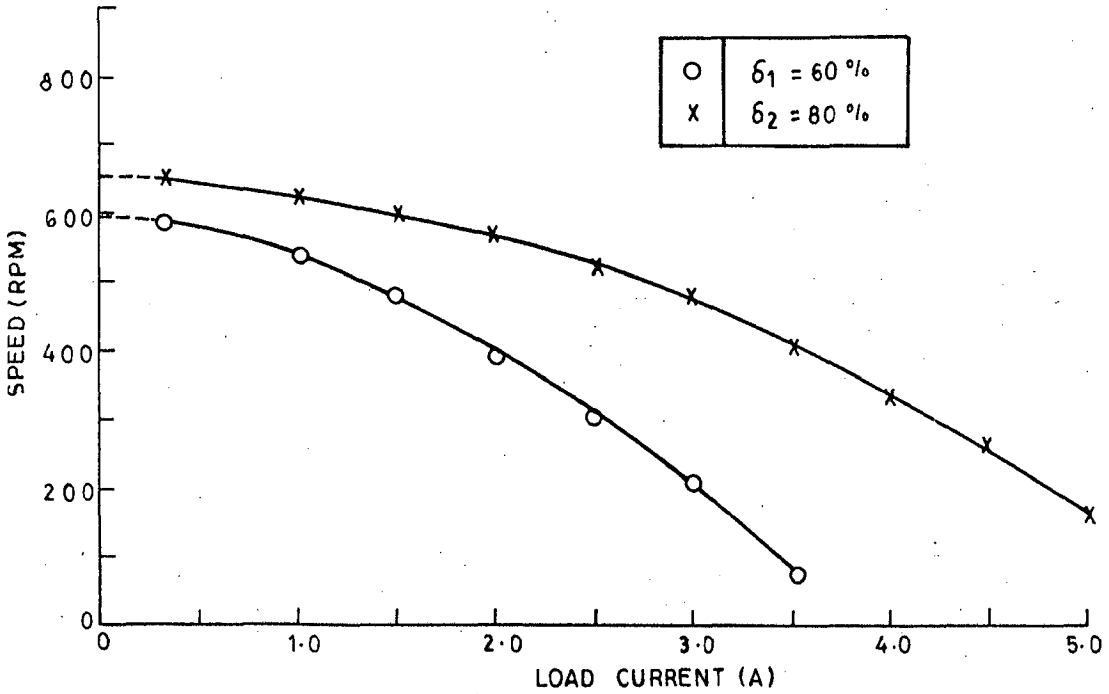


FIG. 4·4—SPEED Vs LOAD CURRENT

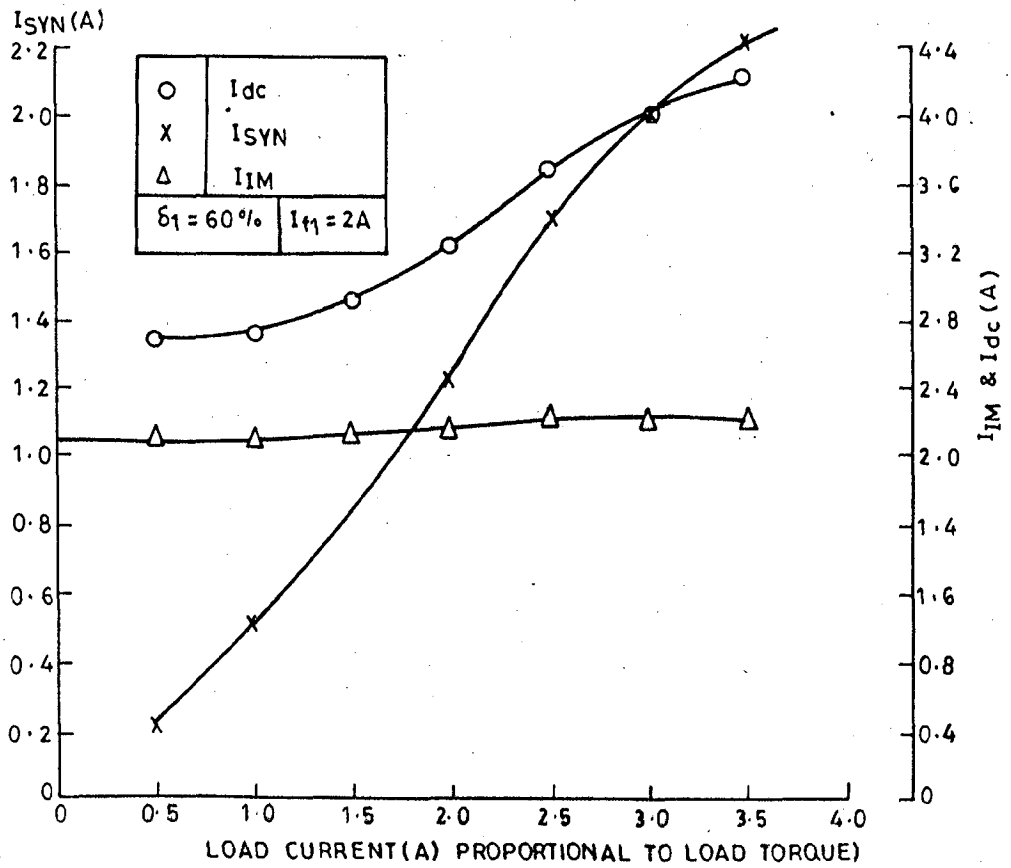


FIG. 4·5—LOAD CURRENT Vs INDUCTION MOTOR INPUT CURRENT, D. C. LINK CURRENT AND SYNCHRONOUS MACHINE CURRENT

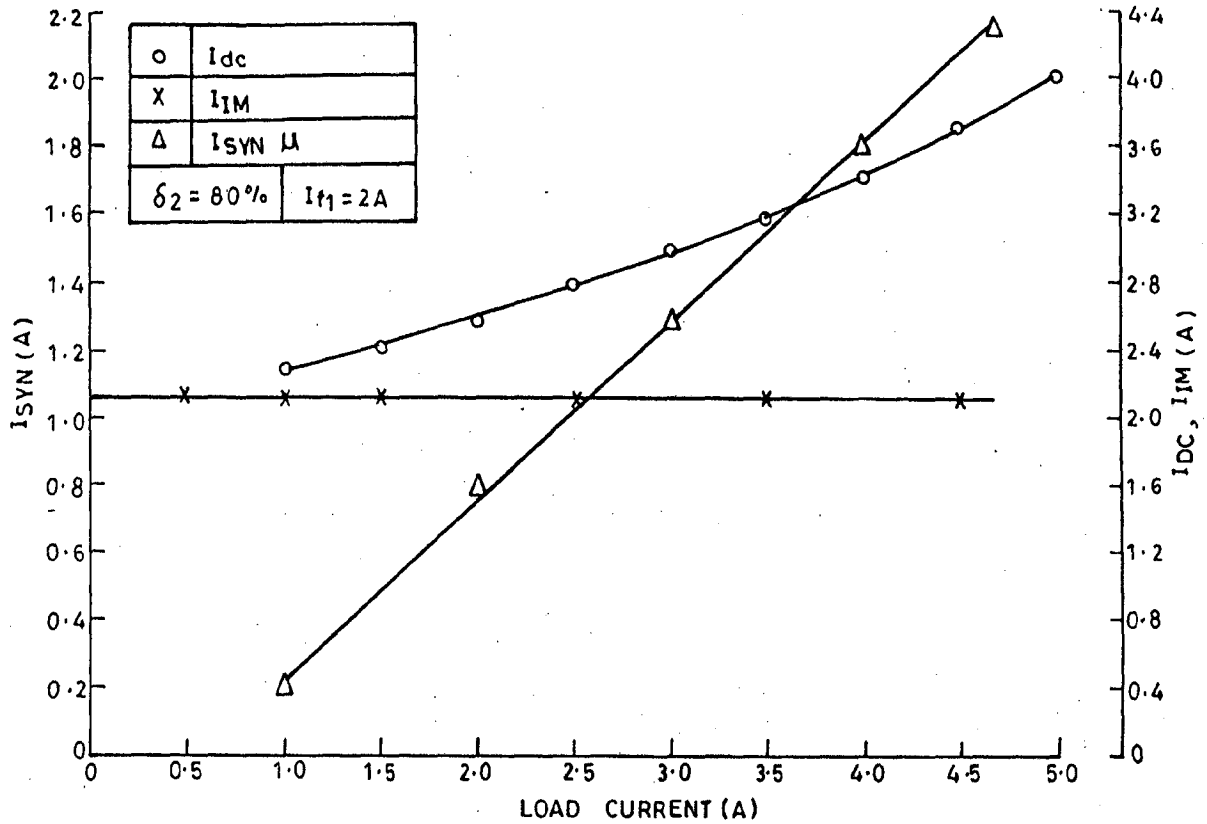


FIG. 4·6—LOAD CURRENT Vs INDUCTION MOTOR CURRENT, D. C. LINK CURRENT & SYNCHRONOUS MACHINE CURRENT

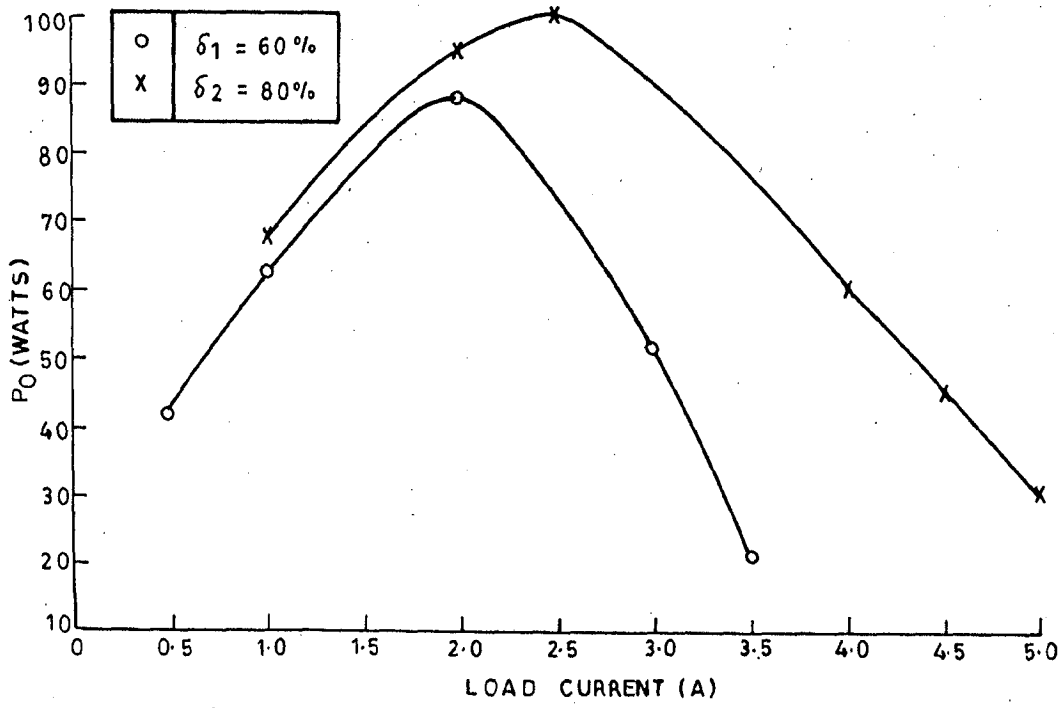


FIG. 4·7—LOAD CURRENT Vs NET POWER OUTPUT

It is observed that the induction motor current remains almost constant with increase of load current. This is due to the fact that amount of loading is rather low (about 100 w only) and therefore the current drawn by the Induction motor increases only marginally.

(iv) The loading is done by a direct coupled fully excited d.c. generator, its armature voltage drops significantly under load conditions due to fall in speed. Its power output therefore falls at high load current. The power output is already low for low load currents. Thus the loading ability of the arrangement is as depicted in Fig. 4.7 for a field current set at 2 Amps and the chopper duty cycle set at (i) 60 % (ii) 80 % .

(v) The oscillograms of synchronous machine terminal voltage V_{AC}, the two output signals of the voltage comparator, the synchronizing signal of 60° pulse width are shown in Fig. 4.8.

(a) They are exactly similar to the theoretical ones given in Chapter II. Fig. 4.8(b) shows the terminal voltage V_{AC}, synchronizing signal, the output of $TM_1(2)$ and the firing pulses for Th_1 of LCI. Fig. 4.8(c and d) shows the terminal voltage V_{AC} and the firing pulses for LCI thyristors in proper sequence at an interval of 60° for the six channels. Fig. 4.8(e) shows the output of $TM_0(2)$ and the firing pulses of the main and auxiliary thyristors of the chopper at $\sigma = 70\%$.

(iv) The oscillograms of stator input voltage and current of induction motor at no load and loaded conditions of the drive are shown in Figs. 4.9(a) to 4.9(d) for two different values of field currents. I_{f_1} and I_{f_2} respectively. Chopper duty cycle is set at 50 percent that the current waveform is very nearly sinusoidal with super posed notches, 6 per cycle.

The rotor voltage (at slip frequency) and current of wound rotor Induction motor under no load and loaded conditions at the field currents I_{f_1} and I_{f_2} respectively are shown in Figs. 4.9(e),(f),(g) and (h) chopper duty cycle is set at 50 percent. The voltage waveforms are sinusoidal with notches at 60° interval due to the commutation of thyristors. The current waveform is quasi-square with 120° pulse width due to the diode bridge rectifier.

(vii) The oscillograms of the voltage and current under no load and load are shown in Fig. 4.10(a) and (b). The field current is set at I_{f_1} at a duty cycle of 50%..

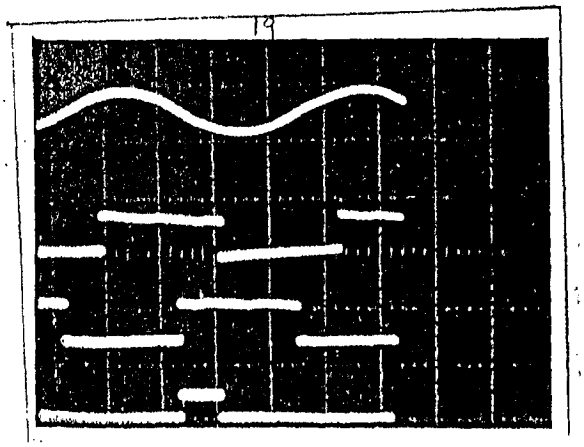
(viii) The oscillograms of d.c. link voltage and current under no load and loaded conditions with two values I_{f_1} and I_{f_2} are shown in Figs. 4.11 (a),(b),(c) and (d).

(ix) The stator current and voltage of synchronous motor under no load and loaded conditions are shown in Figs. 4.12(a), (b), (c) and (d). The voltage and current waveforms of synchronous motor are almost sinusoidal because of the capacitor at the input terminals of the motor.

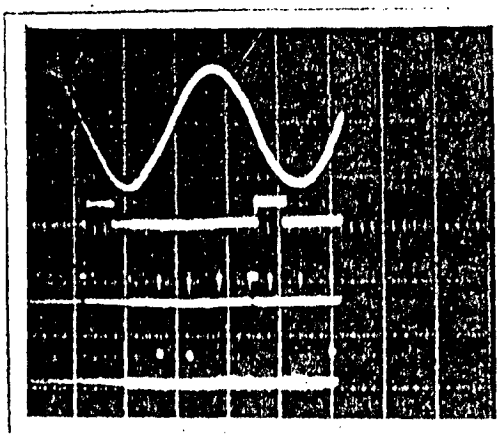
The chopper controlled commutatorless Kramer drive at no load and load conditions works satisfactorily and will find good applications in various industries for wide speed range of sub-synchronous region.

4.4 CONCLUSIONS

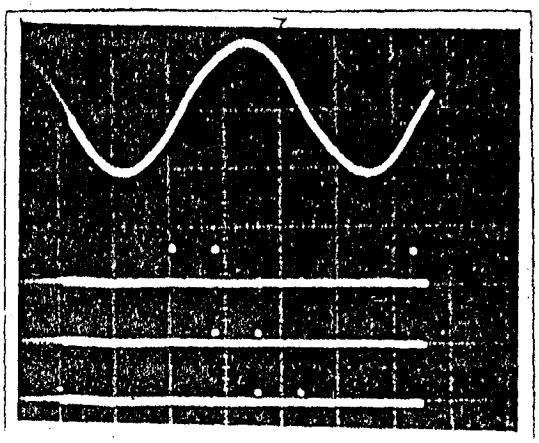
The present scheme works satisfactorily at no load and loaded conditions. Microprocessor based firing controlled circuit generates firing pulses for thyristors of ICI and the chopper in proper sequence and the duty cycle of the chopper. through ADC has been achieved. The commutatorless D.C.motor behaves exactly similar in its characteristics of that of a conventional d.c. motor in the Kramer system.



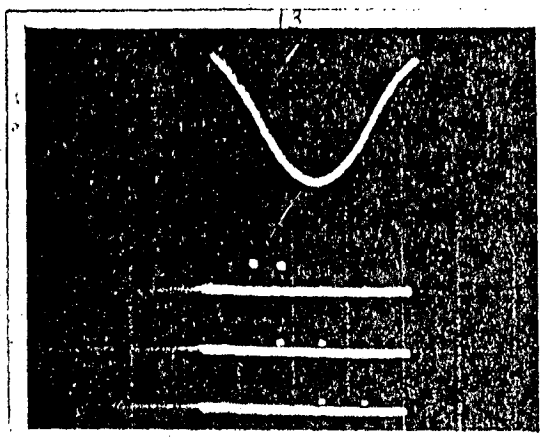
4.8(a) WAVEFORMS OF MACHINE TERMINAL VOLTAGE VAC, OUTPUTS OF THE VOLTAGE COMPARATORS AND THE SYNCHRONIZING SIGNAL.



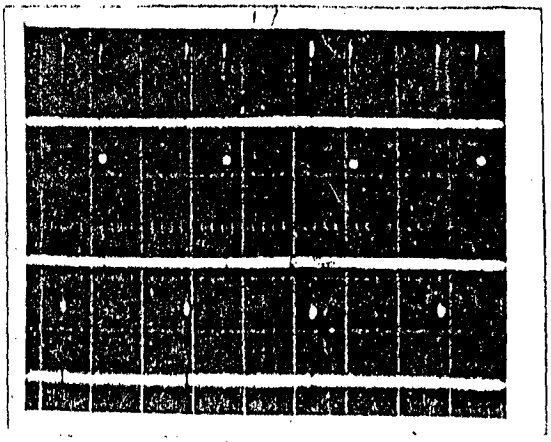
4.8(b) WAVEFORMS OF SYNCHRONOUS MACHINE TERMINAL VOLTAGE VAC, SYNCHRONIZING SIGNAL, OUTPUT OF TM_1(2 AND FIRING PULSES OF T1.



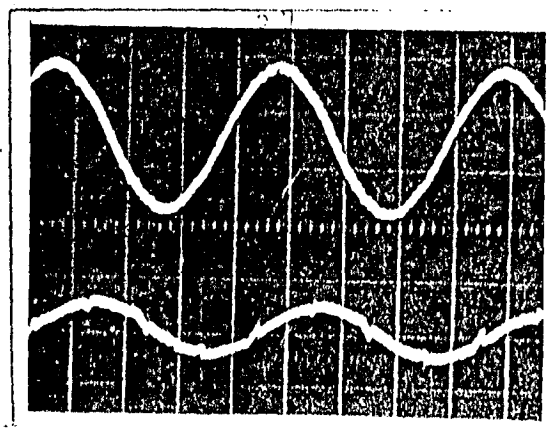
4.8(c) WAVEFORMS OF SYNCHRONOUS MACHINE TERMINAL VOLTAGE VAC, FIRING PULSES OF T1, T2 and T3.



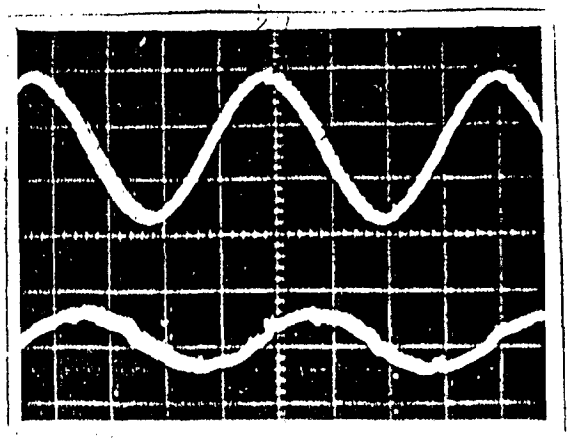
4.8(d) WAVEFORMS OF SYNCHRONOUS MACHINE TERMINAL VOLTAGE, FIRING PULSES OF T4, T5, and T6.



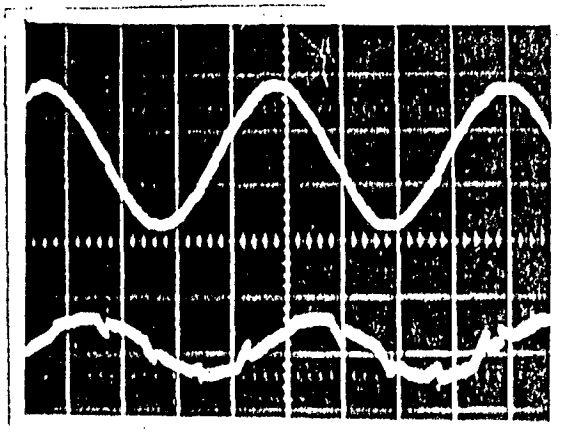
4.8(e) WAVEFORMS OF OUTPUT OF TM_o(2), FIRING PULSES OF Th_{MAIN} and Th_{AUX} FOR CHOPPER



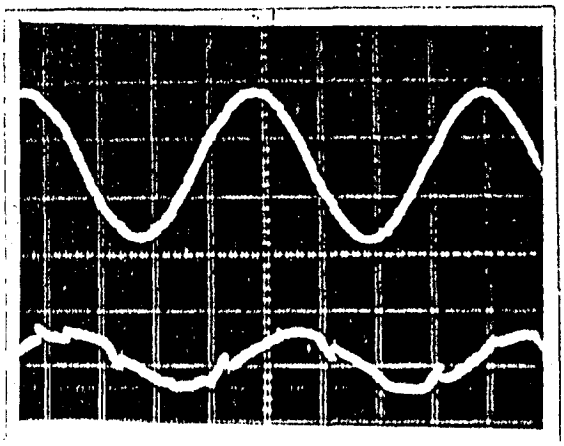
4.9(a) WAVEFORMS OF STATOR VOLTAGE (400V) AND CURRENT (2.1A) OF WRIM AT NOLOAD, SPEED (580 RPM) AND FIELD CURRENT (I_{f_1} = 2A)



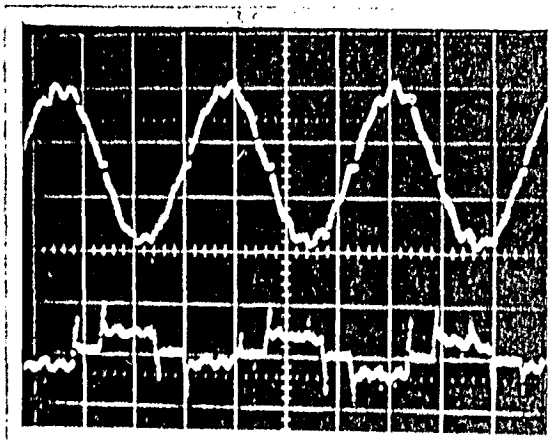
4.9(b) WAVEFORMS OF STATOR VOLTAGE (400V and CURRENT (2.2A) OF WRIM AT IOAD, SPEED (520 RPM) AND CLM FIELD CURRENT (I_{f_1}=2A).(δ=50 %.)



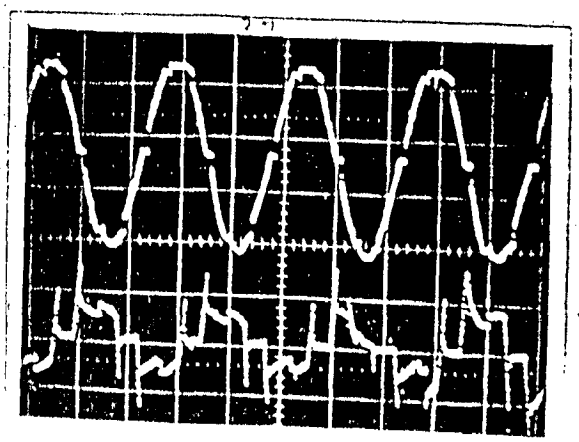
4.9(d) WAVEFORMS OF STATOR VOLTAGE (400V) AND CURRENT (2.2A) OF WRIM AT IOAD, SPEED (430 RPM) AND CLM FIELD CURRENT (I_{f_2}=4A).



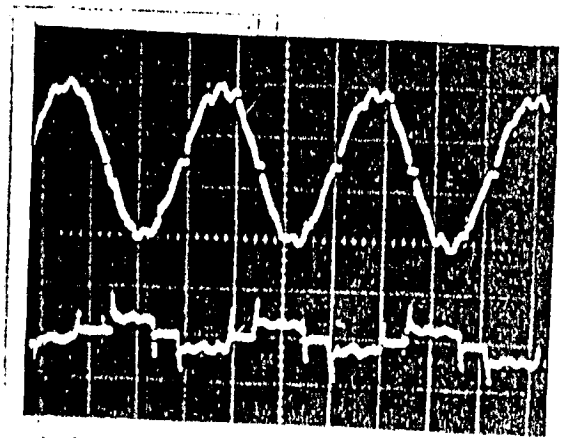
4.9(c) WAVEFORMS OF STATOR VOLTAGE (400V) AND CURRENT (2.1A) OF WRIM AT NOLOAD, SPEED (480 RPM) AND FIELD CURRENT (I_{f_2}=4A), δ=50 percent.



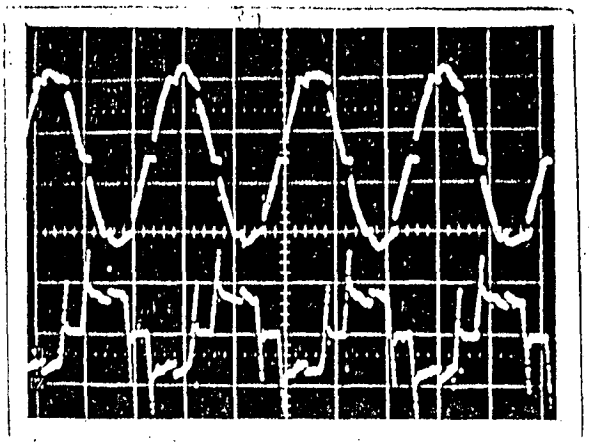
4.9(e) WAVE FORMS OF ROTOR VOLTAGE (88V) AND CURRENT (1.0A) OF WRIM AT NOLOAD, SPEED (530 RPM) AND FIELD CURRENT (I_{f_1}=2A)



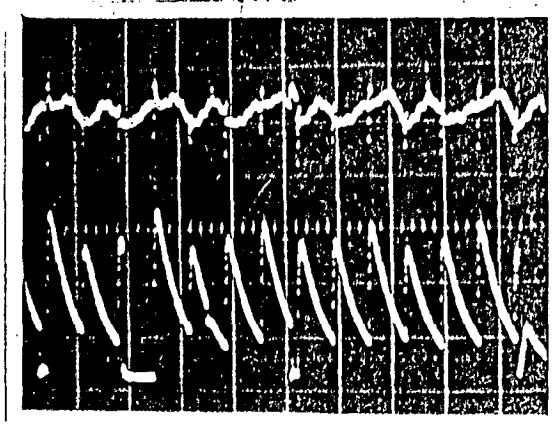
4.9(f) WAVEFORMS OF ROTOR VOLTAGE (116V) AND CURRENT (2.5A) OF WRIM AT IOAD, SPEED (300 RPM) AND(I_{f_1}=2A).



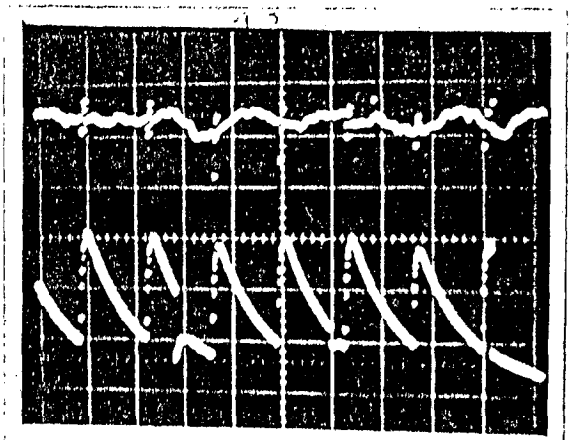
4.9(g) WAVEFORMS OF ROTOR VOLTAGE (124V) AND CURRENT (1.4A) OF WRIM AT NOLOAD, SPEED (500 RPM) AND (I_{f_2}= .4A).



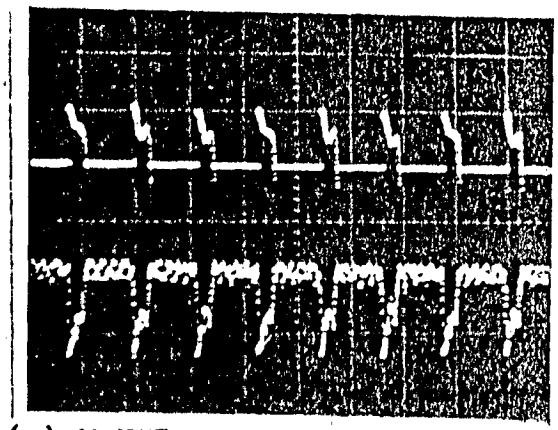
4.9(h) WAVEFORMS OF ROTOR VOLTAGE (132V) AND CURRENT (3.0A) OF WRIM AT LOAD, SPEED (300 RPM) AND I_{f_2}=4A.



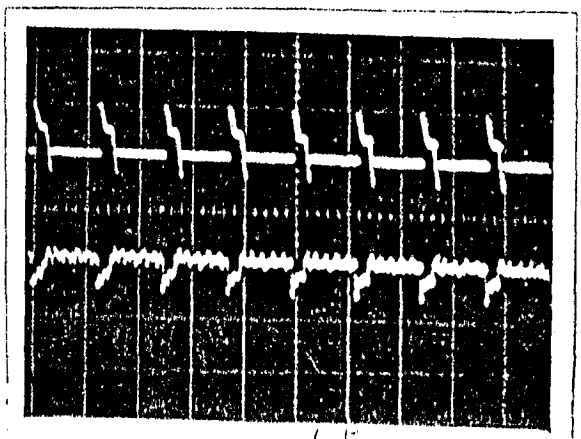
4.10(a) WAVEFORMS OF CHOPPER INPUT VOLTAGE (130V) AND CURRENT (1.1A) AT NO LOAD, SPEED (540 RPM) AND I_{f_1} (2A) WITH DUTY CYCLE (50 percent), 2 msec/div (SCALE)



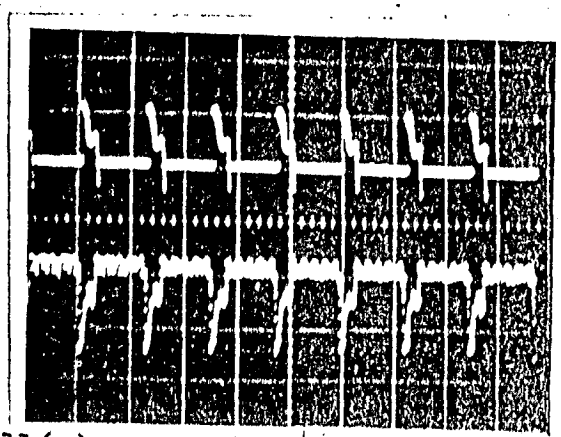
4.10(b) WAVEFORMS OF CHOPPER INPUT VOLTAGE (140V) AND CURRENT (1.4A) AT LOAD, SPEED (500 RPM) AND I_{f_1} (2A), 2 msec/div (SCALE)



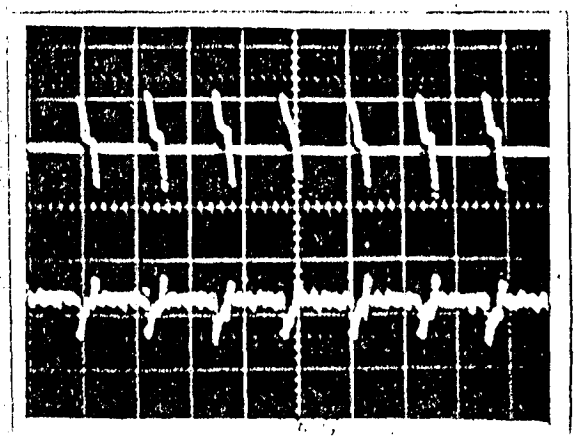
4.11(a) WAVEFORMS OF DC LINK VOLTAGE (30V) AND CURRENT (1.1A) AT NOLOAD SPEED (520 RPM) AND I_{f_1} (2A), SCALE (50 m secs/div.)



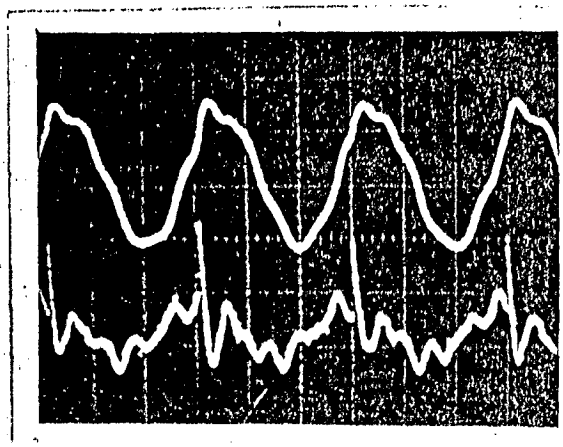
4.11(b) WAVEFORMS OF D.C.LINK VOLTAGE (25V) AND CURRENT (2.1A) AT LOAD SPEED (520 RPM) AND I_{f_1} (2A) SCALE (50 m secs/div.)



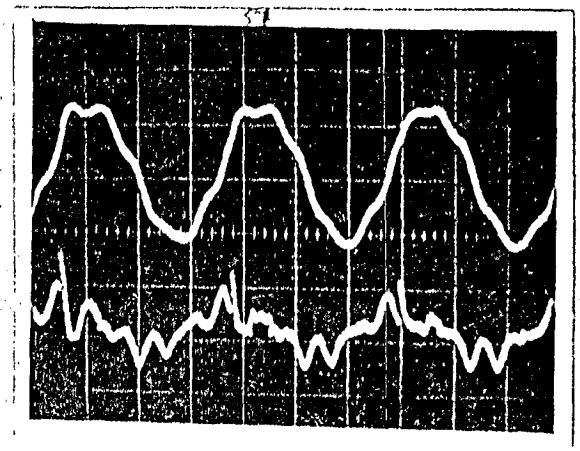
4.11(c) WAVEFORMS OF D.C.LINK VOLTAGE (25V) AND CURRENT (1.1A) AT NO LOAD, SPEED (495RPM) and I_{f_2} (4A), SCALE (50 m sec/div).



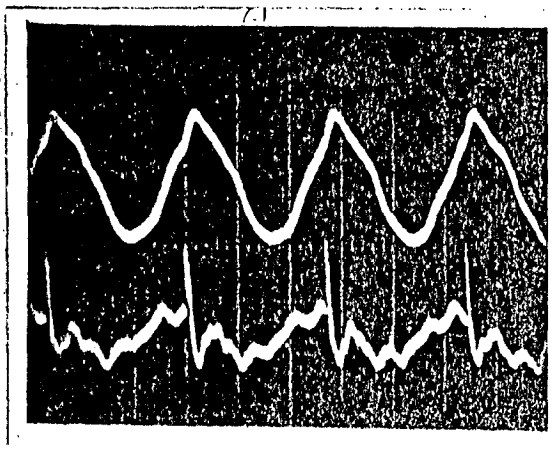
4.11(d) WAVEFORMS OF D.C.LINK VOLTAGE (20V) AND CURRENT (2.2A) AT LOAD, SPEED (470 RPM) AND I_{f_2} (4A), SCALE(50 msecs/div.)



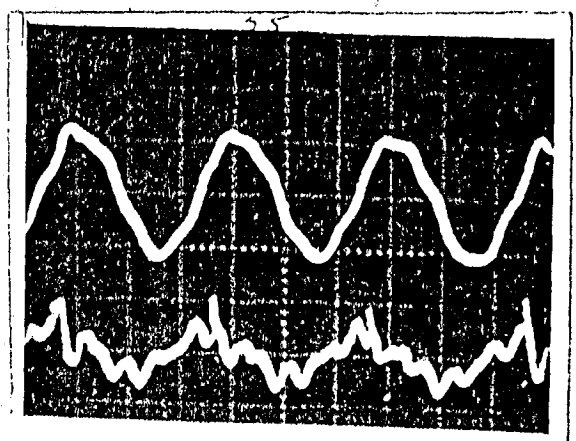
4.12(a) WAVEFORMS OF SATOR VOLTAGE (72V) AND CURRENT (0.6A) OF SYNCHRONOUS MACHINE AT NOLOAD, SPEED (560 RPM) AND I_{f_1} (2A).



4.12(b) WAVEFORMS OF STATOR VOLTAGE (95V) AND CURRENT (1.5A) OF SYNCHRONOUS MACHINE AT LOAD, SPEED (520 RPM) AND I_{f_1} (2A).



4.12(c) WAVEFORMS OF STATOR VOLTAGE (85V) AND CURRENT (0.5A) OF SYNCHRONOUS MACHINE AT NO LOAD, SPEED (520 RPM) AND I_{f_2} (4A)



4.12(d) WAVEFORMS OF STATOR VOLTAGE (92V) AND CURRENT (1.85A) OF SYNCHRONOUS MACHINE AT LOAD, SPEED (475 RPM) AND I_{f_2} (4A).

CHAPTER - 5

CONCLUSIONS AND SUGGESTIONS FOR FURTHER WORK

5.1 CONCLUSIONS

The work presented in this thesis covers the design and fabrication of a microprocessor controlled firing schemes for line commutated inverter, d.c. link ~~the~~ chopper and the experimental investigations on the performance of chopper controlled commutatorless Kramer drive. The main conclusions of the present work are summarized as follows.

1. The power circuits and an open loop firing angle control scheme using only few hardware components have been designed and fabricated. The firing circuits works satisfactorily despite the presence of commutation spikes in the terminal voltage of the synchronous machine.

2. The terminal voltage of synchronous motor is observed sinusoidal under all conditions with small notches spaced at 60° interval occuring due to the commutation of the thyristors of load commutated inverter. The duration of the spikes is equal to the commutation over lap angle and is quite small.

3. From the experimental investigations, it is observed that the system is stable at no load as well as loaded conditions. The variation of speed beyond half-synchronous speed is obtained by reducing duty cycle of the chopper, which is equivalent to reducing armature voltage of the commutatorless motor. It is also verified that commutationless dc motor exhibits the characteristics similar to the conventional D.C.motor.

4. The main advantage of the present work with the microprocessor control over the analogue control is that of flexibility, saving in cabling by use of twisted pairs, easier fault diagnostics, as well as remote information is available to the microprocessor allowing a decision and display to take place, easier sequence modifications without hardwire changes and longer life of hardwire as these equipments are completely solid state.

Compared with other systems of speed control of would rotor, Induction motor, the preferred system is commutatorless and therefore has advantage of less maintenance, higher reliability and also of causing fewer of the harnful effects that harmonic currents and the reactive power of the inverter have on power supplies. The experimental results are obtained on a laboratory size chopper

controlled commutatorless Kramer drive which verifies the Kramer principle. This system is suitable for applications such as large pump and fan type of drives which have a limited speed control range.

5.2 SUGGESTIONS FOR FURTHER WORK

During the course of investigations, some problems have arisen which would require further investigations. Therefore this work can be extended, on following aspects.

1. The synchronous machine in the present work is basically a slipring induction motor run ~~such~~ as a synchronous machine. Hence better performance of the drive system may be expected by using a conventional synchronous machine.
2. The steady state analysis of the drive may be developed to correlate the experimental results.
3. A dynamic model may also be developed to study the transient and dynamic performance of the drive.
4. The speed control of the would rotor induction motor may also be attempted by varying the firing angle of the inverter bridge.

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APPENDIX - I

DETAILS OF THE MACHINES USED

i) 3-phase wound rotor Induction motor.

230/400V, 3 phase, 50 hz, Δ/Y, 3.75 kw (5 HP)

1440 RPM, 7.5A, 140 Rotor Volts, 22 Rotor Amps.

ii) Slip ring Induction motor used as Synchronous motor.

3.75 KW, 3 phase, 50 hz, ,440V, 8 Amps,

Rotor volts 146, Rotor current 16.2 Amps.

Cos 0 = 0.8

iii) D.C.Compound generator (loading machine)

220V, 5 HP.

APPENDIX- II

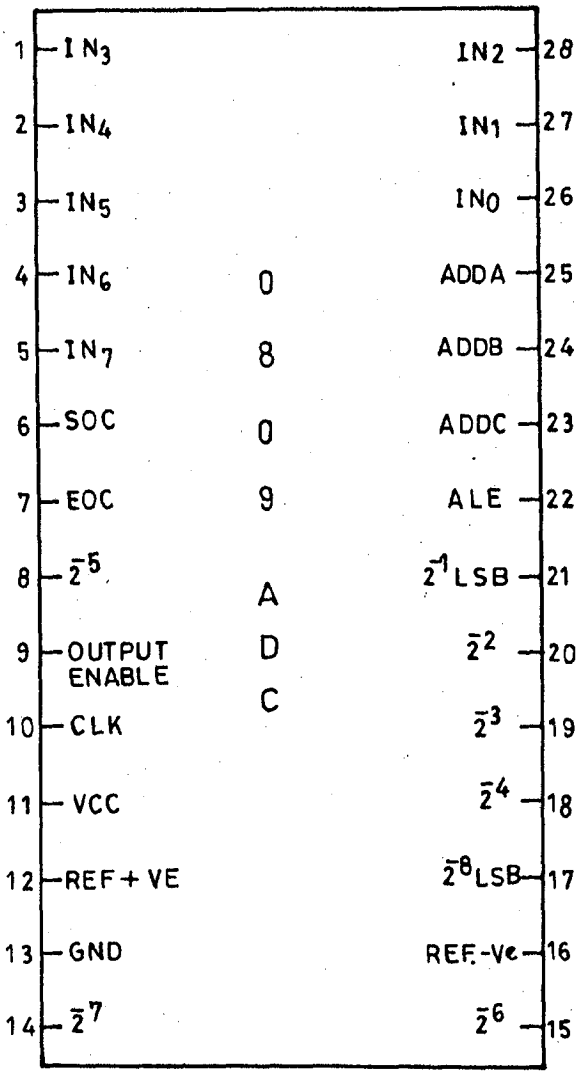

FIG. — DETAILS OF ADC 0809 PIN CONFIGURATION

APPENDIX - III

MAIN PROGRAM

LABEL	ADDRESS	CONTENTS	MNEMONICS	COMMENTS
	6000	31,FF,7F	LXI SP	INITIALIZE STACK POINTER
	6003	3E,8A	MVIA,8A	INITIALIZE 8255(1) IN MODE 0
	6005	D3,03	OUT 03	
	6007	3E,00	MVI A,00	MAKE ALL BITS OF PORT A LOW
	6009	D3,00	OUT 00	
	600B	3E,54	MVIA,54	INITIALIZE TM1 OF 8253(1) IN MODE 2
	600D	D3,13	OUT 13	
	600F	3E,03	MVIA,03	LOAD TM_1(1) FOR 511.67 KHz OUTPUT
	6011	D3,11	OUT 11	
	6013	3E,B0	MVIA,B0	INITIALIZE TM2(1)
	6015	D3,13	OUT 13	IN MODE 0
	6017	3E,70	MVIA 70	INITIALIZE TM1(2)
	6017	D3,A3	OUT A3	IN MODE 0
	6018	3E,30	MVIA,30	INITIALIZE TM_0(2)
	601D	D3,A3	OUT A3	IN MODE 0
	601F	3E,56	MVIA,56	INITIALIZE 8259
	6021	D3,28	OUT 28	IN FULLY NESTED
	6023	3E,61	MVIA,61	MODE E
	6025	D3,29	OUT 29	
	6027	F3	DI	DISABLE INTERRUPT SYSTEMS
	6028	3E DA	MVI A,DA	UNMASK IRO, IR_2 AND
	602A	D3,29	OUT 29	IR5, INT CHANNELS

contd....

LABEL	ADDRESS	CONTENTS	MNEMONICS	COMMENTS
	602C	CD,70,62	CALL ADC	GET THE INFORMATION
	602F	CD,B0,62	CALL MULT	OF DUTY CYCLE TO CALCULATE TONC
	6032	22,7C,61	SHLD ADDR(11)	STORE TONC IN ADDR11
	6035	3A,72,61	LDA ADD(6)	CALCULATE TOFFC
	6038	47	MOV B,A	
	6039	3E,64	MVIA,64	TOFFC=[64_H- ADC OUTPUT] XK
	603B	90	SUB,B	
	603C	32,72,61	STA,ADDR(6)	
	603F	CD,B0,62	CALL MULT	SAVE TOFFC
	6042	22,7F,61	SHLD ADDR(12)	IN ADDR 12
	6045	3A,7C,61	LDA ADDR(11)	LOAD $TM_0(2)$ WITH
	6048	D3,A0	OUT A0	TON C
	604A	3A,7D,61	LDA ADDR(11+1)	
	604D	D3,A0	OUT A0	
	604F	21,60,61	LXI H 6160	LOAD HL WITH FIRING COMMAND
	6052	22,66,61	SHLD ADDR(0)	ADDRESS
S_1	6055	DB,02	INPORT C	INPORT PC_7BIT
	6057	17	RAL	IN CARRY
	6058	DA,55,60	JC,S1	IS PC7=0 NO JUMP TO S_1.
	605B	3E, FF	MVIA, FF	LOAD $TM_2(1)$ WITH FFFF H
	605D	D3, 12	OUT 12	
	605F	3E,FF	MVIA, FF	
	6061	D3,12	OUT 12	

contd...

LABEL	ADDRESS	CONTENTS	MNEMONICS	COMMENTS
S_2	6063	DB,02	IN PORT C	INPORT PC7 BIT
	6065	17	RAL	
	6066	D2,63,60	JNC S_2	IS PC_7=1 NO, JUMP TO S_2
S_3	6069	DB,02	INPORT C	INPORT PC_7 BIT
	606B	17	RAL	
	606C	DA,69,60	JC S_3	IS PC_7=0 NO JUMP TO S_3
N W	606F	DB,12	IN 12	INPUT LOWER BYTE OF TM_2(1)
	6071	4F	MOV C,A	GET LOWER BYTE IN REGISTER C
	6072	DB,12	IN 12	INPUT HIGHER BYTE OF TM_2(1).
	6074	47	MOV B,A	
	6075	21,FF,FF	IXIH,FFFF	LOAD HL WITH FFFF
	6078	08	DSUB	SUBTRACT CONTENT OF BC PAIR IN CONTENT OF HLPAIR
	6079	22,68,61	SHLD ADDR(1)	SAVE 60° IN ADDRI
	607C	AF	XRA A	CLEAR CARRY
	607D	7C	MOV A,H	CALCULATE 30° COUNT
	607E	1F	RAR	
	607F	57	MOV D,A	
	6080	7D	MOV A,L	
	6081	1F	RAR	
	6082	5F	MOV E,A	
	6083	EB	XCHG	

contd.....

LABEL	ADDRESS	CONTENTS	MNEMONICS	COMMENTS
	6084	22,6A,61	SHLD ADDR(2)	SAVE COUNT FOR 30°
	6087	3E,FF	MVI A,FF	LOAD TM_2(1) WITH
	6089	D3,12	OUT 12	FFFF FOR NEW
	608B	3E,FF	MVI A,FF	60° COUNT
	608D	D3,12	OUT 12	
WAIT	608F	Fb	EI	ENABLE INTERRUPT
	6090	76	HLT	SYSTEMS
	6091	2A,66.61	LHLD ADDR(0)	LOAD HL PAIR WITH MEMORY POINTER ADDR (0)
	6094	F3	DI	
	6095	7D	MOV A,L	
	6096	FE,66	CPI 66	IS FS = 6
	6098	CA,6F,60	JZ NEW	IF YES, JUMP TO NEW
	609B	C3,8F,60	JMP WAIT	IF NO, JUMP TO WAIT.

LABEL	ADDRESS	CONTENTS	MNEMONICS	COMMENTS
	6180	F5	PUSH PSW	SAVE PSW
	6181	3E,02	MVI A,02	MAKE PC_1 HIGH
	6183	D3,02	OUT,02	
	6185	3E,DA	MVI A,DA	UNMASK IR_0, IR_2 AND IR_5 INTERRUPT CHANNELS
	6187	D3,29	OUT 29	
	6189	3A,6A,61	LDA ADDR(2)	LOAD TM_1(2) WITH 30^0 COUNT
	618C	D3,A1	OUT A1	
	618E	3A,6B,61	LDA ADDR(2+1)	
	6191	D3,A1	OUT,A1	
	6193	F3	DI	DISABLE INTERRUPT SYSTEMS
	6194	3E,60	MVI A,60	END OF INTERRUPT
	6196	D3,28	OUT,28	IRO
	6198	F1	POP PSW	
	6199	Fb	EI	ENABLE INTERRUPT SYSTEMS
	619A	C9	RET	RETURN TO THE MAIN PROGRAM→

IR 2 INTERRUPT SUBROUTINE

LABEL	ADDRESS	CONTENTS	MNEMONICS	COMMENTS
	61D0	F5	PUSH PSW	SAVE PSW
	61D1	3E,02	MVI A,02	MAKE PC_1 HIGH
	61D3	D3,02	OUT,02	
	61D5	3E,DA	MVI A,DA	NUMASK IR_0, IR_2
	61D7	D3,29	OUT 29	AND IR_5 INTERRUPT CHANNELS
	61D9	2A,66,61	LHLD ADDR(0)	LOAD HL WITH MEMORY POINTER
	61DC	7E	MOV A,M	GET FIRING PULSE
	61DD	D3,00	OUT PORT A	COMMAND IN A MAKE PARTICULAR BIYS HIGH
	61DF	23	INX H	INCREMENT HI PAIR
	61E0	22,66,61	SHLD 6166	
	61E3	7D	MOV A,L	
	61E4	FE,66	CPI 66	IS FS=6 IF NO, JUMP
	61E6	CA,FF,61	JZ AGAIN	TO AGAIN
	61E9	3A,68,61	LDA 6168	LOAD TM_1(2)
	61EC	D3,A1	OUT,A1	WITH 60° DELAY COUNT
	61EE	3A,69,61	LDA 6169	
	61F1	D3,A1	OUT A1	
NO LOAD	61F3	3E,00	MVI A,00	MAKE ALL THE
	61F5	D3,00	OUT 00	PORT A BITS LOW
	61F7	F3	DI	DISABLE INTERRUPT SYSTEMS
	61F8	3E,62	MVI A,62	END OF INTERRUPT SYSTEMS
	61FA	D3,28	OUT 28	
	61FC	F1	POP PSW	

contd.....

LABEL	ADDRESS	CONTENTS	MNEMONICS	COMMENTS
	61FD	FB	EI	ENABLE INTERRUPT SYSTEMS
	61FE	C9	RET	RETURN TO THE MAIN PROGRAM
A GAIN	61FF	21,60,61	LXI H 6160	LOAD HL WITH ADDR(0)
	6122	22,66,61	SHLD 6166	
	6125	C3,F3,61	JMP NOLOAD	JUMP TO NOLOAD
			IR_5 INTERRUPT SUBROUTINE	
	6210	F5	PUSH PSW	SAVE PSW
	6211	3E, DA	MVIA DA	UNMASK IR_0, IR_2
	6213	D3,29	OUT 29	AND IR_5 INTERRUPT CHANNELS
	6215	AF	XRA A	CLEAR CARRY
	6216	3A,7A,61	LDA ADDR 10	LOAD ACCUMULATOR WITH FIRING INDEX = 0
	6219	E6,01	ANT 01	CHECK FI=00
	621B	C2,34,62	JNZ 51	IF NO, JUMP TO SI
	621E	3E,40	MVI A,40	MAKE PA_6 BIT HIGH
	6220	D3,00	OUT,00	
	6222	3A,7E,61	LDA, ADDR(12)	LOAD COUNTER
	6225	D3,A0	OUT A0	TM_0(2) WITH TOFFC
	6227	3A,7F,61	LDA ADDR(12+1)	
	622A	D3,A0	OUT A0	
	622C	3E,01	MVI A,01	LOAD ACCUMULATOR WITH FI=01
	622E	32,7A,61	STA ADDR (10)	
	6231	C3,47,62	JMP EOI	

contd...

LABEL	ADDRESS	CONTENTS	MNEMONICS	COMMENTS
S1	6234	3E,80	MVIA,80	MAKE PA_7 BIT HIGH
	6236	D3,00	OUT 00	
	6238	3A,7C,61	LDA ADDR(11)	LOAD COUNTER TM_0(2) WITH TOFFC
	623B	D3,A0	OUT A0	
	623D	3A,7D,61	LDA ADDR(11+1)	
	6240	D3,A0	OUT A0	
	6242	3E,00	MVIA,00	LOAD ACCUMULATOR WITH FI=00.
	6244	32,7A,61	STA ADD 10	
EOI	6247	3E,00	MVIA,00	MAKE ALL THE PORT BITS LOW
	6249	D3,00	OUT 00	
	624B	3E,65	MVI A,65	EOI
	624D	D3,28	OUT 28	
	624F	F1	POP PSW	
	6250	Fb	EI	ENABLE INTERRUPT SYSTEMS
	6251	C9	RET	RETURN TO THE MAIN PROGRAM

ADC SUBROUTINE

LABEL	ADDRESS	CONTENTS	MNEMONICS	COMMENTS
	6270	3E,01	MVIA,01	LOAD BYTE IN ACCUMULATOR TO SET PC_0
	6272	D3,02	OUT PORT C	SET PC_0
	6274	11,01,00	LXID COUNT	LOAD (D,E) WITH DELAY COUNT
	6277	CD BC,03	CALL DELAY	THIS IS A DELAY
	627A	3E,00	MVIA,00	LOAD BYTE IN ACCUMULATOR
	627C	D3,02	OUT PORT C	TO RESET PC_0
READ	627F	DB,02	INPORT C	INPORT EOC SIGNAL
	6280	17	RAL	
	6281	17	RAL	GET PC_6 IN CARRY
	6282	D2,7E,62	JNC READ	IS CONVERSION OVER NO JUMP TO READ
	6285	DB,01	INPORT B	GET THE DATA.IN ACCUMULATOR
	6287	32,72,61	STA ADDR(6)	SAVE A DC OUTPUT
	628A	32,F6,27	STA 27F6	
	628D	06,00	MVIB,00	
	628F	CD,FA,06	CALL MODDT	DISPLAY ADC OUTPUT IN DATA FIELD
	6292	09	RET	RETURN TO THE MAIN PROGRAM.

MULT SUBROUTINE

LABEL	ADDRESS	CONTENTS	MNEMONICS	CONTENTS
	62B0	2A,6E,61	LHLD ADDR(4)	LOAD (HL) WITH MULTIPLICAND
	62B3	EB	XCHG	GET MULTIPLICAND IN (DE)
	62B4	21,00,00	LXIH 0000H	INITIALIZE (HL) WITH 0000 H
	62B7	3A,72,61	LDA ADDR(6)	LOAD ACCUMULATOR WITH MULTIPLIER
	62BA	47	MOV B,A	
	62BB	0E,00	MVIC,00	INITIALIZE COUNTER C WITH 00H
NEXT	62BD	0C	INR C	
	62BE	78	MOV A,B	
	62BF	iF	RAR	PUT LSB INTO CARRY
	62C0	47	MOV B,A	
	62C1	D2,D0,62	JNC TEST	IS CY=1 NO JUMP TO TEST
	62C4	79	MOV A,C	
	62C5	FE,01	CPI 01H	
	62C7	CA,CC,62	JZ UPDATE	IS Z=1 YES JUMP TO UPDATE
	62CA	AF	XRAA	CLEAR CARRY
	62CB	18	RDLC	ROTATE (DE) LEFT BY ONE BIT
UPDATE	62CC	19	DADD	UPDATE THE PARTIAL PRODUCT
	62CD	C3,D8,62	JMP FINISH	

contd.....

LABEL	ADDRESS	CONTENTS	MNEMONICS	CONTENTS
TEST	62D0	79.	MOV A,C	
	62D1	FE,01	CPI 01H	
	62D3	CA,D8,62	JZ FINISH	IS Z=1 YES JUMP TO FINISH
	62D6	AF	XRAA	CLEAR CARRY
	62D7	18	RDLC	ROTATE LEFT BY ONE BIT
FINISH	62D8	79	MOV A,C	
	62D9	FE,07	CPI 07 H	
	62DB	C2,BD,62	JNZ NEXT	IS Z=1 NO, JUMP TO NEXT
	62DE	C9	RET	RETURN TO MAIN PROGRAM.

FIRING PULSE COMMAND TABLE

ADDRESS	CONTENT	THYRISTOR PAIR TO BE FIRED	FIRING SEQUENCE
6160	18	(4,5)	1
6161	30	(5,6)	2
6162	0C	(6,1)	3
6163	06	(1,2)	4
6164	03	(2,3)	5
6165	21	(3,4)	6

MEMORY LOCATIONS

Address of command word = 6166 → ADDR 0

60° Count value = 6168 → ADDR 1

30° Count value = 616A→ ADDR 2

Quotient = 616E→ ADDR 4

ADC OUTPUT = 6172→ ADDR 6

FIRING INDEX = 617A→ ADDR 10

TON COUNT = 617C → ADDR 11

TOFF COUNT = 617E → ADDR 12

VALUE OF K

616E 32

616F 00

VECTOR ADDRESSES

6140 → CD, 80, 61 → IR_0
C9

6144 → CD, 00, 61 → IR_1
C9

6148 → CD, D0, 61 → IR_2
C9

614C → CD, 00, 61 → IR_3
C9

6150 → CD, 00, 61 → IR_4
C9

6154 → CD, 10, 62 → IR_5
C9

6158 → CD, 00, 61 → IR_6
C9.

615C → CD,00,61 → IR_7
C9

NON SPECIFIC EOI

6100	FS	PUSH PSW	INITIALIZATION OF 8259 WITH OCW2
6101	3E,20	MVI A,20	
6103	D3,28	OUT 28	
6105	F1	POP PSW	
6106	Fb	EI	ENABLE INTERRUPT SYSTEMS
6107	C9	RET	RETURN TO THE MAIN PROGRAM.

APPENDIX - IV

FIG - PHOTOGRAPHS OF THE EXPERIMENTAL SET UP.