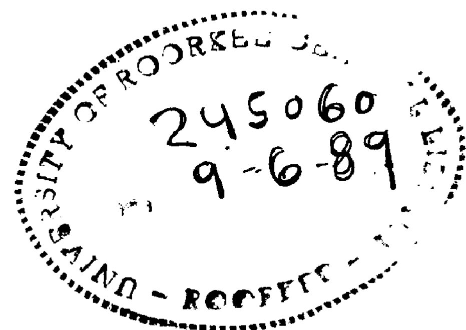
RELIABILITY EVALUATION OF POWER ELECTRONIC CIRCUITS

A DISSERTATION

submitted in partial fulfilment of the
requirements for the award of the degree
of
MASTER OF ENGINEERING
in
ELECTRICAL ENGINEERING
(With Specialization in System Engineering & Operations Research)

By

AJAY TALEGAONKAR



DEPARTMENT OF ELECTRICAL ENGINEERING
UNIVERSITY OF ROORKEE
ROORKEE-247 667 (INDIA)

MARCH, 1989

DEDICATED

TO

MY PARENTS

CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the dissertation entitled, "**RELIABILITY EVALUATION OF POWER ELECTRONIC CIRCUITS**", in partial fulfilment of the requirements for the award of the degree of MASTER OF ENGINEERING in ELECTRICAL ENGINEERING with specialization in SYSTEM ENGINEERING AND OPERATIONS RESEARCH, submitted in the Department of Electrical Engineering, University of Roorkee, Roorkee, is an authentic record of my own work carried out during the period from August 1988 to March 1989 under the supervision of Dr. H.O.Gupta, Reader, Department of Electrical Engineering, University of Roorkee, Roorkee, India.

The matter embodied in this dissertation has not been submitted by me for the award of any other degree or diploma.

Dated: March 23 ,1989

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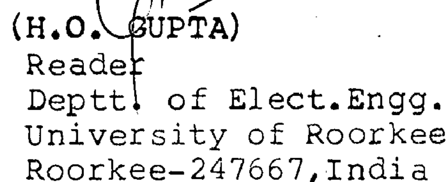

(H.O. GUPTA)
Reader
Deptt. of Elect.Engg.
University of Roorkee
Roorkee-247667,India

ABSTRACT

With the development in the field of electronics, the complexity and power handling capability of electronic circuits have increased many fold. Failures, specially drift failures, in power electronic circuits, is a major problem. This necessitates the reliability analysis of the circuit during design process, prior to fabrication.

An effort has been made to evaluate the component failure rate of power electronic circuits with database structures of failure rate data. Part stress analysis method is most suited and has been used for failure rate evaluation. The electrical and thermal stress for each component is obtained from circuit analysis. Models for Silicon controlled rectifier, diac and triac have been developed and incorporated in the circuit analysis program for d.c. and transient analysis. The models of these devices for transient analysis simulate off-state, on-state, turn-on period and turn-off period. This furnishes the data of current and voltage transients, and rate of change of voltage and current, which is very important from reliability view-point but not used in part stress analysis. The dBASE III PLUS package for reliability evaluation stores the component failure rates in a database structure. Two examples are reported.

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NOTATIONS

C	capacitor
C_t	junction transition capacitance
C_d	junction diffusion capacitance
C_{tc}	collector transition capacitance
C_{te}	emitter transition capacitance
DIDT	rate of fall of current in thyristor when forward current is equal to holding current
D_f, D_g	parameters associated with forward & gate characteristics respectively, SCR
G_f, G_f	incremental conductances of Gate-cathode and Anode-cathode portions respectively, SCR
i	node current
i_C	current through the capacitor
i_L	current through the inductor
i_{RC}	current through parallel resistance R_{PC}
i_{RL}	current through parallel resistance R_{PL}
I_s	Saturation current of diode
I_d	junction current of diode
I_{cs}	reverse saturation current, collector
I_{es}	reverse saturation current, emitter
I_{fo}, I_{go}	currents associated with forward and gate characteristics of thyristor
I_{RM}	Maximum value of reverse current in thyristor during turn-off period

I_t	time dependent current source
i_f	forward current of thyristor
I_H	holding current for thyristor
i_g	gate current of thyristor
I_{bc}	base collector current
I_{be}	base emitter current
I_c	collector current
I_e	emitter current
I_b	base current
I_B, I_C, I_E	node current at base, collector and emitters
I_R	current through resistor
K_d	proportionality constant, diode
k	Boltzman's constant (1.38×10^{-23} J/k)
L	inductance
m	curvature constant
N	junction grading constant
q	electronic charge (1.602×10^{-19} coloumbs)
R_{SL}	series resistance, inductor
R_{SK}	series resistance, capacitor
R_{PL}	parallel resistance, inductor
R_{PC}	parallel resistance, capacitor
R_{sd}	leakage resistance, diode

R_{se}	emitter leakage resistance
R_{sc}	collector leakage resistance
R	resistor
R_g	gate-cathode bulk resistance, SCR
R_f	anode-cathode bulk resistance, SCR
T	absolute temperature
T_d	diffusion capacitance time constant, diode
T_c	collector diffusion capacitance constant
T_e	emitter diffusion capacitance constant
T_{hd}	diode constant(= $1/V_T$)
T_{hc}	collector constant
T_{he}	emitter constant
t_r	rise time, SCR
t_{rr}	reverse recovery time, SCR
t_d	delay time, SCR
V_c	voltage across capacitor
V_L	voltage across inductor
V_d	junction voltage, diode
V_T	voltage equivalent of temperature, diode
V_Z	junction contact potential
V_{zc}	collector junction contact potential
V_{ze}	emitter junction contact potential

V_B, V_C, V_E	terminal voltage at base, collector and emitter respectively
V_b, V_c, V_e	junction voltage at base, collector and emitter respectively
V_{AK}	anode-cathode voltage, SCR
V_{gk}	gate-cathode voltage, SCR
V_{gd}	voltage across gate-cathode equivalent diode of SCR
V_{fd}	voltage across anode-cathode equivalent diode of SCR
β_f	forward short circuit current gain
β_r	reversed short circuit current gain
τ	time constant

CHAPTER-1

INTRODUCTION

1.1 NECESSITY :

Today electronic devices are finding their use in almost every field of life. From household goods to medical, industrial, space and defence equipments, all have their heart made by electronic circuits. Even so electronics is a technology under revolution.we may call - it exploding technology. Every year number of electronic devices are invented and thrown into market. This makes ratio of new to tried and true portions of electronic circuit very high and hence its reliability must be suspected. Power electronic circuits, because of their peculiar operating conditions such as higher currents and temperature ,and stresses due to rapid turn-on and turn-off of circuit elements are more vulnerable to failure. Thus it is necessary to design the circuit in such a way that atleast reasonable theoretical reliability is achieved.

The circuit design process in general has following separate but interacting stages :

(i) In the first stage, initial structure of the circuit is obtained based on required objectives. This in turn gives the components necessary for the circuit. The circuit is now tested for certain loose specifications and if these specification are not satisfied the initial structure may be modified.

(ii) In the second stage, the circuit is tested for a set of tighter and complete design specifications. These specifications include environmental performance, operational requirements under normal and abnormal conditions and cost etc.

(iii) Third stage of design include determination of mechanical layout of circuits on P.C.B., with mechanical and electrical constraints.

(iv) Last stage of design consists of reliability evaluation. This gives an estimate of theoretically achievable reliability and also furnishes knowledge of parts in the circuit having high failure rates.

1.2 RELIABILITY EVALUATION :

The two methods for reliability prediction of electronic components are discussed in MIL-HDBK-217D; Military Handbook : Reliability prediction of electronic equipment. |1|. These methods are easy to apply and the data required is available in MIL-HDBK-217D itself.

These two methods are :

(i) Parts count method

(ii) Part stress analysis.

These methods vary in degree of information needed to apply them. The parts count method is applicable in early design phase and requires less information. The information required to apply this method is (1) generic part types (including complexity) and quantities (2) Part quality level (3) Equipment environment. The part stress analysis requires great deal of information and is applicable during later design phase, where actual hardware and circuits are being designed. The information required generally include electrical stress, temperature, quality level, application, degree of complexity, environment, rating, construction class etc.

1.3 CIRCUIT ANALYSIS :

For determination of electrical and thermal stresses in various components of circuit, circuit analysis has to be carried out. D.C. and transient analysis are used to determine these stresses. Modified Newton's method |2| is used for d.c. analysis to solve non-linear circuit equations. For transient analysis, non-linear differential equations are converted into non-linear algebraic equation |3| by discretization using Euler's method. This set of algebraic equations is solved by modified Newton's method.

1.4 AUTHOR'S CONTRIBUTION :

In this dissertation models for silicon controlled rectifier, diac and triac have been developed and the FORTRAN IV package CKTAN|4| has been modified to incorporate these devices for circuit analysis. A separate subroutine to calculate electrical stress of each component is added in CKTAN.

The dBASE III PLUS package RELCKT|5| is modified such that it is able to calculate the reliability of circuits containing SCRS, diacs, triacs, inductors and transformers in addition to resistors, capacitors, diodes and transistors. This package takes the data necessary for reliability evaluation from the circuit analysis package CKTAN. Failure rate is determined for each component of circuit, for given environment and electrical stress, using database files storing failure rates. These database files have been prepared as per MIL-HDBK-217D.

The results for few circuits are reported and discussed.

CHAPTER-2

DEVICE MODELLING AND CIRCUIT ANALYSIS

For reliability evaluation of electronic circuits using part stress analysis, electrical and thermal loading of each component is required. The definition of loading differs from component to component. Loading is defined as average value of current for diodes and thyristors, maximum voltage across the terminals for capacitors and power dissipation for resistors and transistors. For determination of these quantities circuit analysis must be carried out. In the present work d.c. analysis and transient analysis of the electronic circuits are carried out to determine loading of different components. D.C. analysis furnishes initial value of circuit voltages and currents and after this, transient analysis is performed for a pre-specified period.

2.1 POWER ELECTRONIC CIRCUIT ANALYSIS :

In most of the analytical solutions of power electronic circuits, thyristors are assumed as ideal switches. This assumption gives only approximate results and for accurate analysis there is a need for more realistic model of thyristors.

Tamer Kutman|6| used binary logic model to represent on and off states of SCR. The resistances offered by thyrister during on-and off-state were obtained by piece-wise linearization of characteristic curve. J. McGHEE |7| proposed a

SCR model based on Ebers -Moll model of transistor. The biggest drawback of this model was that model parameters had to be determined by performing experiments on thyristor. In most of the cases what is required is that the model parameters should be easily obtainable from data-sheets only.

Most of the methods using numerical integration technique for solution of circuit equations and considering only two states of thyristors namely on-state and off-state suffer from numerical instability because of sudden change in device resistance when it changes its state |8|. To overcome this problem transition state models should be incorporated in the circuit analysis.

G.Karady and T. Gilsig |9| used the turn-on model of SCR, based on the profile of voltage fall during this period, for the calculation of turn-on overvoltages in a high voltage d.c. thyristor valve. G.N. Revankar and Pradeep K. Srivastava |10| proposed a turn-off model of SCR based on reverse recovery time and stored charge data.

In present work models for SCR, diac and triac have been developed for on-state, off-state, turn-on time and turn-off time. Inclusion of transition state models is advantageous in two ways :

(i) Problem of numerical instability as mentioned above do not arise due to sudden change of conditions and

(ii) data of peak inverse current, di/dt and dv/dt is obtained which is very important from reliability view-point.

The off-state model based on leakage current, on-state model based on exponential characteristics in this state, turn-on period model based on profile of voltage fall during this period and turn-off model based on reverse-recovery time and profile of current during this period are developed and successfully tested.

2.2 D.C. ANALYSIS

The d.c. analysis of circuit envolves the solution of the circuit equation (2.1), iteratively.

$$H.\Delta V = B \qquad .. (2.1)$$

where H is the node-admittance matrix

and B is the current vector

H and B are calculated at each iteration using solution obtained at previous iteration (or using initial guess in first iteration).

At each iteration correction vector ΔV is obtained and node voltages are updated. The d.c. solution is said to be obtained if correction in each node voltage is less then a specified value (tolerance).

2.2.1 DEVICE MODELS FOR D.C. ANALYSIS

Diode model : The circuit model |2| representing semi-conductor diode is shown in Fig. 2.1. The diode current I_d depends on junction voltage V_d and is given by following relation

$$I_d = I_s\left[\exp\left(\frac{V_d}{V_T}\right) - 1\right] \quad .. (2.2)$$

where $V_T = \frac{mKT}{q}$

Linearizing the nonlinear equation (2.2), we get

$$I_d(V_d + \Delta V_d) = I_d(V_d) + g_d.\Delta V_d \quad .. (2.3)$$

or $$\Delta I_d(V_d) = g_d.\Delta V_d \quad .. (2.4)$$

where $g_d = I_s \exp(V_d/V_T)/V_T$

This equation is represented by a linear model of diode shown in Fig. 2.2

Bipolar Transistor Model : Ebers-Moll model is used to represent a transistor. This model is valid for all regions of operation of transistor namely saturation, inverse, normal and off. The Ebers Moll model for NPN transistor is shown in Fig. 2.3 .

The current equation for this model (Fig.2.3) can be written as

$$I_b = I_{cd} + I_{ed} \quad \text{.. (2.5)}$$

$$I_c = \beta_f I_{ed} - (1+\beta_r) I_{cd} \quad \text{.. (2.6)}$$

$$I_e = \beta_r I_{cd} - (1+\beta_f) I_{ed} \quad \text{.. (2.7)}$$

where

$$I_{cd}(V_j) = I_{cs}\left[\exp(-V_{cb}/V_T)-1\right]/(1+\beta_r) \quad \text{.. (2.8)}$$

$$I_{ed}(V_j) = I_{es}\left[\exp(-V_{eb}/V_T)-1\right]/(1+\beta_f) \quad \text{.. (2.9)}$$

where j indicates the iteration number

Linearizing the equations (2.5-2.7) about V_j, we get

$$\begin{bmatrix} g_{cd}+g_{ed} & -g_{cd} & -g_{ed} \\ -(1+\beta_r)g_{cd}+\beta_f g_{ed} & (1+\beta_r)g_{cd} & -\beta_f g_{ed} \\ -(1+\beta_f)g_{ed}+\beta_r g_{cd}-\beta_r g_{cd} & -\beta_r g_{cd} & (1+\beta_f)g_{ed} \end{bmatrix} \begin{bmatrix} \Delta V_b \\ \Delta V_c \\ \Delta V_e \end{bmatrix} = \begin{bmatrix} I_b^j \\ I_c^j \\ I_e^j \end{bmatrix}$$

.. (2.10)

where

$$g_{cd} = \frac{\partial I_{cd}}{\partial V_{cb}} = I_{cs} \exp(-V_{cb}/V_T)/\left[V_T(1+\beta_r)\right] \quad \text{.. (2.11)}$$

$$g_{ed} = \frac{\partial I_{ed}}{\partial V_{eb}} = I_{es} \exp(-V_{eb}/V_T)/\left[V_T(1+\beta_f)\right] \quad \text{.. (2.12)}$$

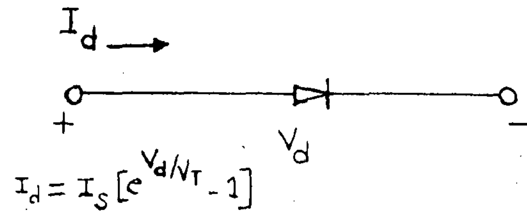


Fig.2.1 : Diode model for d.c. analysis.

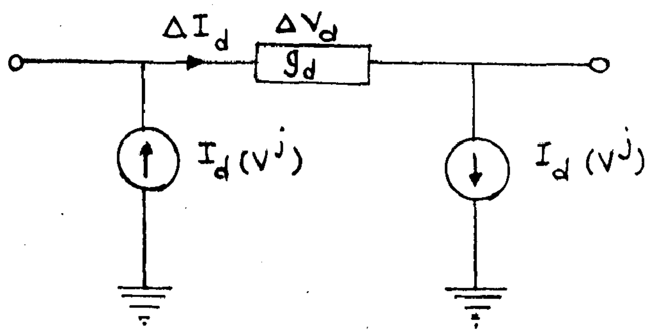


Fig.2.2:Linear equivalent of diode model for d.c. analysis..

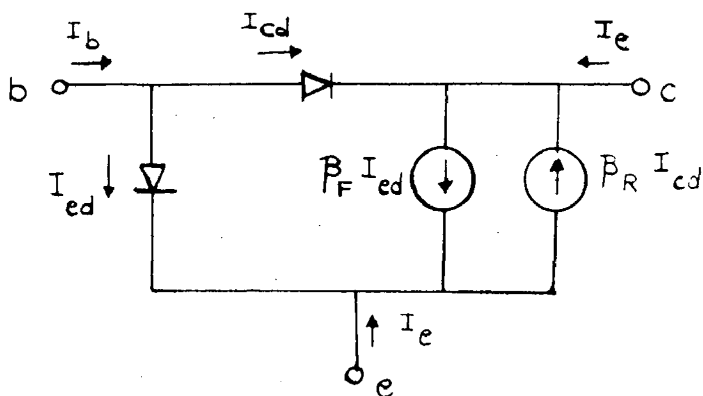


Fig. 2.3 : Ebers-Moll model of transistor for d.c. analysis.

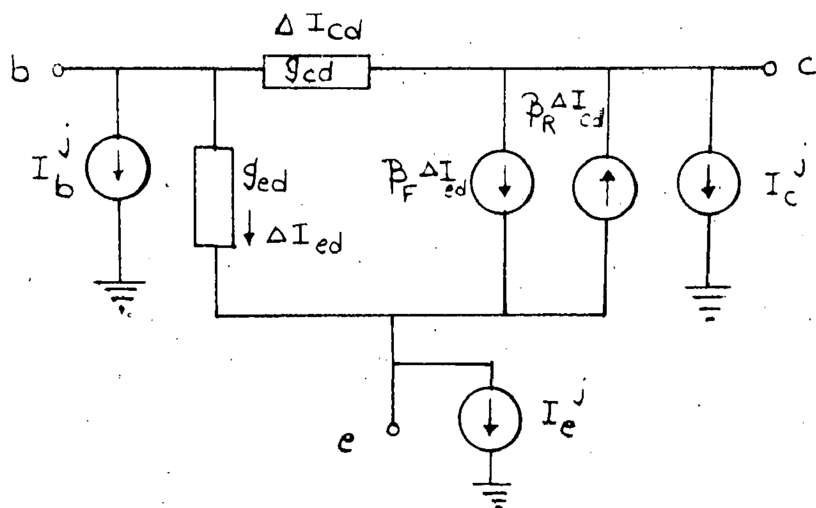


Fig. 2.4 : Linear equivalent of transistor model for d.c. analysis.

equation (2.10) can be written as

$$\Delta H . \Delta V = \Delta B \qquad .. (2.13)$$

where ΔH is a matrix giving contributions of transistor model to admittance matrix

ΔB is vector giving contribution of transistor model to current vector

and ΔV is a vector giving voltage corrections.

Linearized equivalent of Ebers Moll model is shown in Fig. 2.4

Silicon controlled rectifier model : SCR has been modelled separately for on-and off-states. Gate-cathode portion of SCR is modelled as diode. The anode-cathode model for the two states are described below :

(i) Off-state model : From the characteristics curve of SCR shown in Fig.2.6 it is clear that the small current flowing through SCR in off-state varies linearly with anode-cathode voltage. The SCR is modelled as a resistance during off-state, value of this resistance is equal to slope of the characteristic curve in off-state. The contribution of SCR to node-admittance matrix and current vector is determined by the method described while discussing resistance model later in this section.

(ii) On-state model : In on-state SCR characteristic is similar to forward biased diode characteristic.

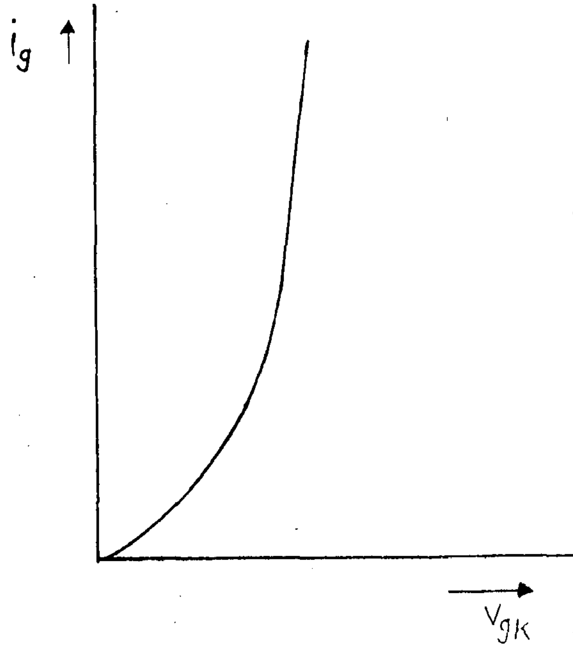


Fig.2.5 : Gate-cathode characteristics of SCR

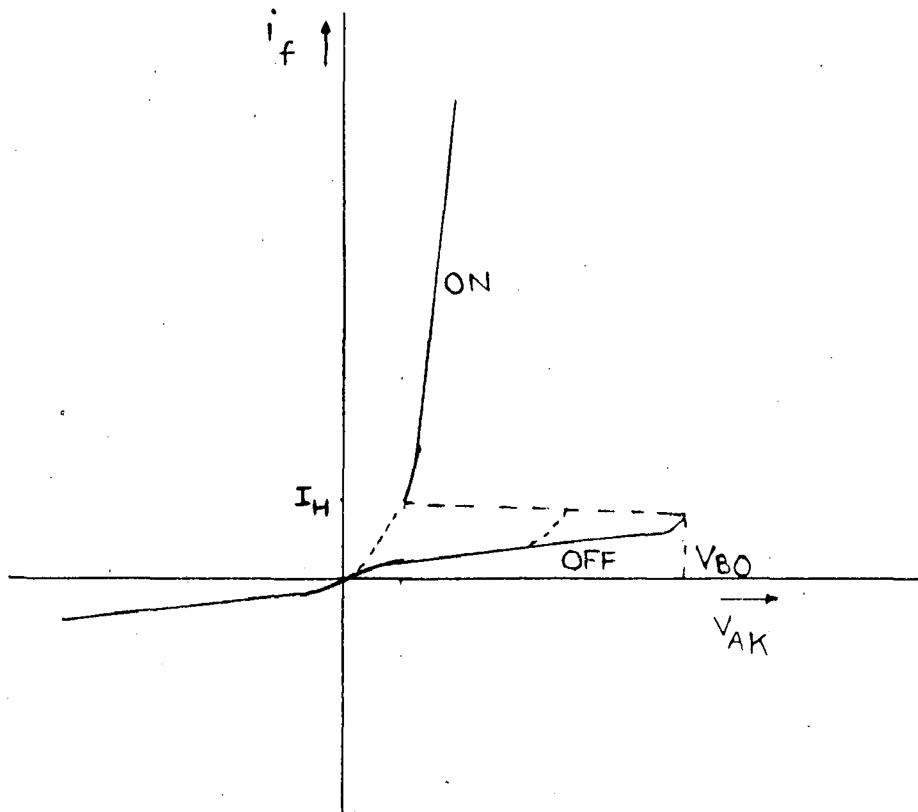


Fig.2.6 : Anode-cathode characteristics of SCR

Current varies exponentially with voltage, governed by the relation :

$$I = I_{fo}[\exp(D_f \cdot V_{fd}) - 1] \quad .. (2.14)$$

where I_{fo} and D_f are the constants and value of these parameters can be found from the characteristic curve.

Thus the contribution of SCR in on-state to node admittance matrix H and current vector B can be found in a way similar to diode except V_T is replaced by $1/D_f$.

Diac Model : Diac is a two terminal device and unlike SCR, it conducts in both directions. Shape of its characteristic is similar to forward characteristic of SCR and is symmetrical for voltage of either polarity. Diac is modelled similar to anode-cathode model of SCR.

Triac Model : Triac is equivalent to two SCR's connected back to back or anti-parallel. It conducts for voltages of both polarity and taking this fact into account the SCR model is slightly modified to get Triac model.

Resistance model : The model for the resistance is shown in Fig. 2.7 .

The current through resistor at j^{th} iteration is given as :

$$I_R^j = \frac{V_R^j}{R}$$

The admittance contribution matrix of the resistance is given by

$$\Delta H = \begin{bmatrix} 1/R & -1/R \\ -1/R & 1/R \end{bmatrix} \quad .. (2.15)$$

The current contribution vector ΔB is given as

$$\Delta B = \begin{bmatrix} -V_R{}^j/R \\ V_R{}^j/R \end{bmatrix} \quad .. (2.16)$$

Capacitor model : Ideal capacitor has infinite impedance to d.c. However small current flows because of leakage. Thus capacitor model for d.c. analysis is taken as resistance whose value equals the leakage resistance of capacitor.

Inductor Model : Ideal inductor offers no resistance to d.c. but in actual practice it has very small resistance because of leads and material of the wire. Thus inductor can be modelled as a resistance for d.c. analysis.

2.2.2 METHOD :

Circuit equations of electronic circuits are highly non-linear due to non-linear characteristic of semiconductor devices. Newton's method which uses only first order derivatives does not give good result and problems like overflow and very slow convergence are encountered. In present work modified Newton's method |2| is used to overcome these problems. Corrections to voltages are

determined by Newton's method but their values are modified when necessary, by exploiting the properties of semiconductor devices.

The non-linear algebraic equations of the electronic circuit are of the form

$$G(X) = 0 \qquad .. (2.17)$$

Where $G:R^n$, R^n is a vector function in the real n-dimensional field.

Expanding (2.17) by Taylor series.

$$G(X_o+\Delta X) = G(X_o) + [G'(X_o)]\Delta X$$
$$+ \text{ high order derivative terms.}$$

Where X_o is the initial value of X

$G'(X_o)$ is Jacobian matrix of $G(X_o)$

Newton's correction vector is obtained by neglecting high order terms and setting $G(X_o+\Delta X)= 0$. By doing so we get

$$\Delta X = -[G'(X_o)]^{-1} \cdot G(X_o) \qquad ..(2.18)$$

With this correction vector $G(X_o+\Delta X)$ is not zero since high order derivative terms have been neglected. To overcome this difficulty, the modified correction vector $\Delta X'$ is obtained such that

$$G(X_o+\Delta X') = G(X_o) + [G'(X_o)]\Delta X = 0 \qquad .. (2.19)$$

The modified correction vector $\Delta X'$ for bipolar devices can be obtained as follows :

Consider a simple diode circuit shown in Fig.2.8. The circuit equation is

$$(V_d - V_s)/R + I_s(e^{V_d/V_T} - 1) = G(V_d) = 0 \quad .. (2.20)$$

From (2.19) and (2.20) we have

$$(V_d + \Delta V_d' - V_s)/R + I_s[e^{(V_d+\Delta V_d')/V_T} - 1]$$

$$= (V_d - V_s)/R + I_s[e^{V_d/V_T} - 1] + (1/R + I_s e^{V_d/V_T}/V_T)\Delta V_d$$

or

$$(\Delta V_d' - \Delta V_d)/R + I_s e^{(V_d+\Delta V_d')/V_T}$$

$$= I_s e^{V_d/V_T}(1 + \Delta V_d/V_T) \quad .. (2.21)$$

where $\Delta V_d = -G(V_d)/G'(V_d)$

Forward biased junction: If the junction voltage is greater than 10 V_T, exponential terms in (2.21) are much more prominent than linear terms. Thus by neglecting $(\Delta V_d' - \Delta V_d)/R$, we get

$$\Delta V_d' = V_T \ln(1+\Delta V_d/V_T)$$

Thus

$$V_d' = \begin{cases} V_T \ln(1+\Delta V_d/V_T) & \text{if } (1+\Delta V_d/V_T) > \epsilon \text{ and } V_d + \Delta V_d > 10V_T \\ \Delta V_d & \text{otherwise} \end{cases}$$

where $0 < \epsilon < V_T$

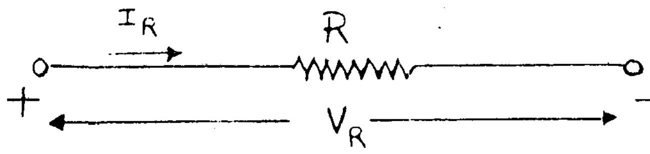


Fig.2.7 : Resistance model

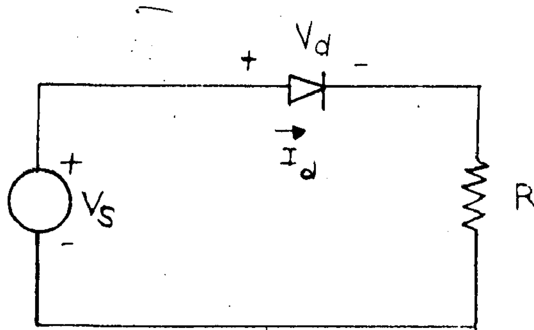


Fig. 2.8 : Diode circuit

Reverse biased junction : The change in junction current is very small for change in junction voltage in the reverse biased diode. Therefore

$$\Delta V_d' = \Delta V_d$$

2.2.3 ALGORITHM :

The stepwise procedure for d.c. analysis of electronic circuit is as follows :

1. Read network topology and device parameters. Give initial estimate for node voltages (The first n_1 nodes are the nodes corresponding to junctions of diodes and transistors).

2. Calculate junction voltages of diodes and transistors and set them appropriately.

3. Generate nodal matrix using linearized circuit equations. Only non-zero terms are stored.

4. Solve linearized circuit equations using sparse matrix technique to calculate correction vector ΔV.

5. Set $j = 1$

6. If $(V_j + \Delta V_j) > 10V_T$ and $(1 + \Delta V_j/V_T) \geq \epsilon$, set

$$\Delta V_j = V_T(1 + \Delta V_j/V_T)$$

7. Set $j = j+1$. If $j < n_1$, go to step 6.

8. Set $V_k = V_k + \Delta V_k$, $[K = 1,2, \ldots n]$

9. If ΔV_{max} = Max $[\Delta V_K]$, K = 1,... n. is less than a specified value, stop. Otherwise go to step 2.

2.3 TRANSIENT ANALYSIS :

Most of the electronic components have non-linear characteristics. Circuit equations for the transient analysis are algebraic and differential equations. Because of the presence of non-linearity, for most of the electronic circuits these equations are stiff i.e. the time constants of the circuit are widely separated. These equations are discretized at each time instant and then solved by modified Newton-Raphson method|3|. Also time step during solution process is adjusted so as to limit truncation error.

The correction voltage Δ V is calculated using the relation

$$H.\Delta V = B$$

H and B matrices are generated at each iteration of each time step using the device models described in the following section.

2.3.1 DEVICE MODELS FOR TRANSIENT ANALYSIS :

Resistance Model : Fig. 2.9 shows the model|3| of resistance

The current for a Newton-Raphson iteration is given by

$$i^o = (V_j - V_k)/R \quad .. (2.22)$$

From above equation, contribution of resistance to node-admittance matrix H and current vector B can be written as

$$\Delta H_{jj} = 1/R$$

$$\Delta H_{jk} = -1/R$$

$$\Delta H_{kk} = 1/R$$

$$\Delta H_{kj} = -1/R$$

$$\Delta B_j = -i^o$$

$$\Delta B_k = i^o$$

Capacitance Model : Fig. 2.10 shows the capacitor model. This model|3| takes into account the losses in the capacitor.

To remove the internal node created due to series resistance R_{SK}, the internal equations are solved. Derivatives of capacitor current are approximated by trapezoidal integration.

Following are the current equations :

$$\dot{V}_C = i_C/C = (i - V_C/R_{PC})/C \quad .. (2.23)$$

$$\dot{V}_C(-1) = (i(-1) - V_C(-1)/R_{PC})/C \quad .. (2.24)$$

$$\Delta V_C = V_C - V_C(-1) \quad .. (2.25)$$

$$V_C = V_j - V_K - R_{SK} . i \quad .. (2.26)$$

$$V_C(-1) = V_j(-1) - V_K(-1) - R_{SK} . i(-1) \quad .. (2.27)$$

Now

$$C \, d \, V_C/dt = \text{capacitor current}$$

i.e.

$$C . \Delta V_C/\Delta T = \frac{1}{2} (i_C + i_C(-1))$$

$$\therefore \Delta V_C = V_C - V_C(-1) = \frac{1}{2} \left[(i - V_C/R_{PC}) + (i(-1) - V_C(-1)/R_{PC}) \right] . \frac{\Delta T}{C} \quad .. (2.28)$$

Rearranging above equation

$$(2C + \frac{\Delta T}{R_{PC}}) V_C = (2C - \Delta T/R_{PC}) V_C(-1) + \Delta T (i + i(-1)) \quad .. (2.29)$$

Substituting values of V_C and $V_C(-1)$ from (2.26) and (2.27) the current for a Newton-Raphson iteration can be obtained as :

$$i^o = a_2 a_4 (V_j - V_k) - a_3 a_4 [V_j(-1) - V_K(-1) + a_5] \quad .. (2.30)$$

where,

$$a_1 = \Delta T/R_{PC}$$

$$a_2 = 2C + a_1$$

$$a_3 = 2C - a_1$$

$$a_4 = 1/(\Delta T + R_{SK} \cdot a_2)$$

$$a_5 = i(-1) \cdot (\Delta T/a_3 - R_{SK})$$

Current through capacitor

$$i = a_2 a_4 (\Delta V_j - \Delta V_K) + i^o$$

from above equation, contribution of capacitor model to node-admittance matrix H and current vector B can be written as :

$$\Delta H_{jj} = a_2 a_4$$

$$\Delta H_{KK} = a_2 a_4$$

$$\Delta H_{jk} = -a_2 a_4$$

$$\Delta H_{kj} = -a_2 a_4$$

$$\Delta B_j = -i^o$$

$$\Delta B_k = i^o$$

Inductor model : Fig. 2.11 shows the realistic model for the inductor |3|. In this model one additional node has been created due to internal voltage V_L. By solving the internal equations this node can be eliminated. Proceeding in a manner similar to capacitance model, we get current for a Newton-Raphson iteration as

$$i^o = a_2(a_1 + \Delta T)(V_j - V_k) - a_3[V_j(-1) - V_k(-1) + a_4] \quad .. (2.31)$$

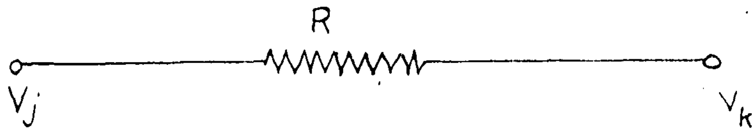


Fig.2.9 : Resistance model.

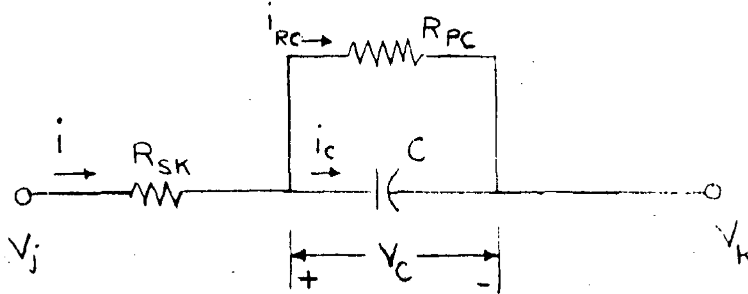


Fig.2.10 : Capacitor model.

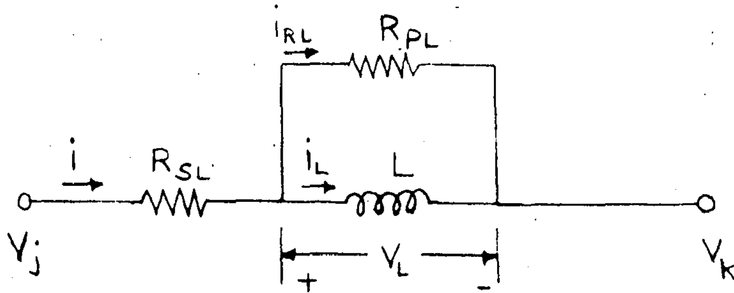


Fig.2.11 : Inductor model

where

$$a_1 = 2L/R_{PL}$$

$$a_2 = 1/(2L+R_{SL}.\Delta T + R_{SL}.\ a_1)$$

$$a_3 = -a_2(\Delta T - a_1)$$

$$a_4 = (2L/(\Delta T - a_1) - R_{SL})\ i(-1)$$

and the current i is given as

$$i = \Delta H(\Delta V_j - \Delta V_k) + i^o$$

where $\Delta H = a_2(a_1 + \Delta T)$

Contribution of this model to node-admittance matrix H and current vector B are given by

$$\Delta H_{jj} = a_2(a_1+\Delta T)$$

$$\Delta H_{KK} = a_2(a_1+\Delta T)$$

$$\Delta H_{jk} = -a_2(a_1+\Delta T)$$

$$\Delta H_{kj} = -a_2(a_1+\Delta T)$$

$$\Delta B_j = -i^o$$

$$\Delta B_k = i^o$$

Diode Model : Fig. 2.12 shows large signal model |3| for semiconductor diode.

Current I_d is given by

$$I_d = I_s[\exp (V_d.\ q/mkT) - 1] \quad .. (2.32)$$

In the model R_{sd} is the leakage resistance of diode and its value is equal to slope of voltage-current characteristic for large negative voltage.

C_d is the junction diffusion capacitance and C_t is junction transition capacitance. Value of the transition capacitance C_t varies with the junction voltage and is given by

$$C_t = C_T (1 - V_d/V_z)^{-N} \qquad \text{for } V_d \leq 0.9\, V_z$$

$$= C_T (0.1)^{-N} \qquad \text{for } V_d > 0.9 V_z \qquad .. (2.33)$$

where C_T is the value of transition capacitance at $V_d = 0$

Diffusion capacitance varies with junction current governed by following the relation

$$C_d = K_d (I_d + I_S) \qquad .. (2.34)$$

where K_d is a constant for a particular diode.

The internal equations of this model are as follows :

$$i_d = C_d \frac{dv_d}{dt} = C_d . \frac{dv_d}{dI_d} . \frac{dI_d}{dt} = T_d . \frac{dI_d}{dt} \qquad .. (2.35)$$

from (2.34) and (2.35)

$$T_d = K_d\, I_S \left[\exp\left(\frac{V_d . q}{mkT}\right)\right] . \frac{mkT}{q\, I_s \left[\exp\left(\frac{V_d . q}{mkT}\right)\right]}$$

i.e.

$$T_d = K_d . \frac{mkT}{q} \qquad .. (2.36)$$

$$i_1 = I_d + T_d \; dI_d/dt$$

$$= I_d + T_d \left[(I_d - I_d(-1))/\Delta T \right]$$

i.e. $$i_1 = I_d(1 + T_d/\Delta T) - I_d(-1). T_d/\Delta T \qquad .. (2.37)$$

$$i_2 = C_t \left[(V_d - V_d(-1))/\Delta T \right] \qquad .. (2.38)$$

$$i_3 = V_d/R_{sd} \qquad .. (2.39)$$

Total current

$$i = i_1 + i_2 + i_3$$

$$= I_d(1 + \frac{T_d}{\Delta T}) + C_t\left[\frac{V_d - V_d(-1)}{\Delta T} \right] + V_d/R_{sd} - I_d(-1).T_d/\Delta T$$

$$.. (2.40)$$

Current for a Newton-Raphson iteration becomes

$$i^o = I_d(1 + T_d/\Delta T) + C_t . V_d/\Delta T + V_d/R_{sd}$$

$$- \left[C_t . V_d(-1)/\Delta T + I_d(-1) . T_d/\Delta T \right]$$

$$.. (2.41)$$

and diode current is given by

$$i = \Delta H . \Delta V_d + i^o \qquad .. (2.42)$$

where

$$\Delta H = (1 + T_d/\Delta T).GD + C_t/\Delta T + 1/R_{sd}$$

$$GD = T_{hd} \cdot I_s \cdot \text{Exp}\,(V_d \cdot T_{hd})$$

$$T_{hd} = q/mkT$$

The contribution of the diode model to node-admittance matrix H and current vector B is given as

$$\Delta H_{jj} = \Delta H$$

$$\Delta H_{kk} = \Delta H$$

$$\Delta H_{jk} = -\Delta H$$

$$\Delta H_{kj} = -\Delta H$$

$$\Delta B_j = -i^{o}$$

$$\Delta B_k = i^{o}$$

Transistor Model : A transistor resembles two closely spaced diode junctions, namely the emitter base junction and base collector junction. Fig. 2.13 shows the model |3| for NPN transistor.

Proceeding in a manner similar to diode, we get current equations at three terminal nodes of transistor for a Newton-Raphson iteration as :

$$I_B^{\circ} = (1/(1+\beta_f) + T_e/\Delta T) I_e + C_{te} \cdot V_e/\Delta T + V_e/R_{se}$$
$$-(T_e\, I_e(-1)/\Delta T + C_{te} V_e(-1)/\Delta T) + (1/(1+\beta_r) + T_c/\Delta T) I_c$$
$$+ C_{tc} \cdot V_c/\Delta T + V_c/R_{sc} - (T_c \cdot I_c(-1)/\Delta T + C_{tc} \cdot V_c(-1)/\Delta T) \quad .. \; (2.43)$$

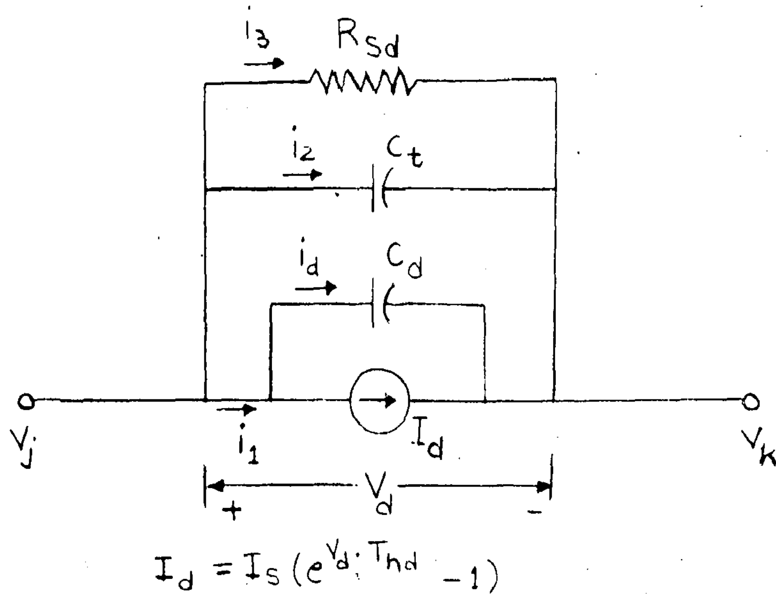


Fig. 2.12 : Large signal model for the diode

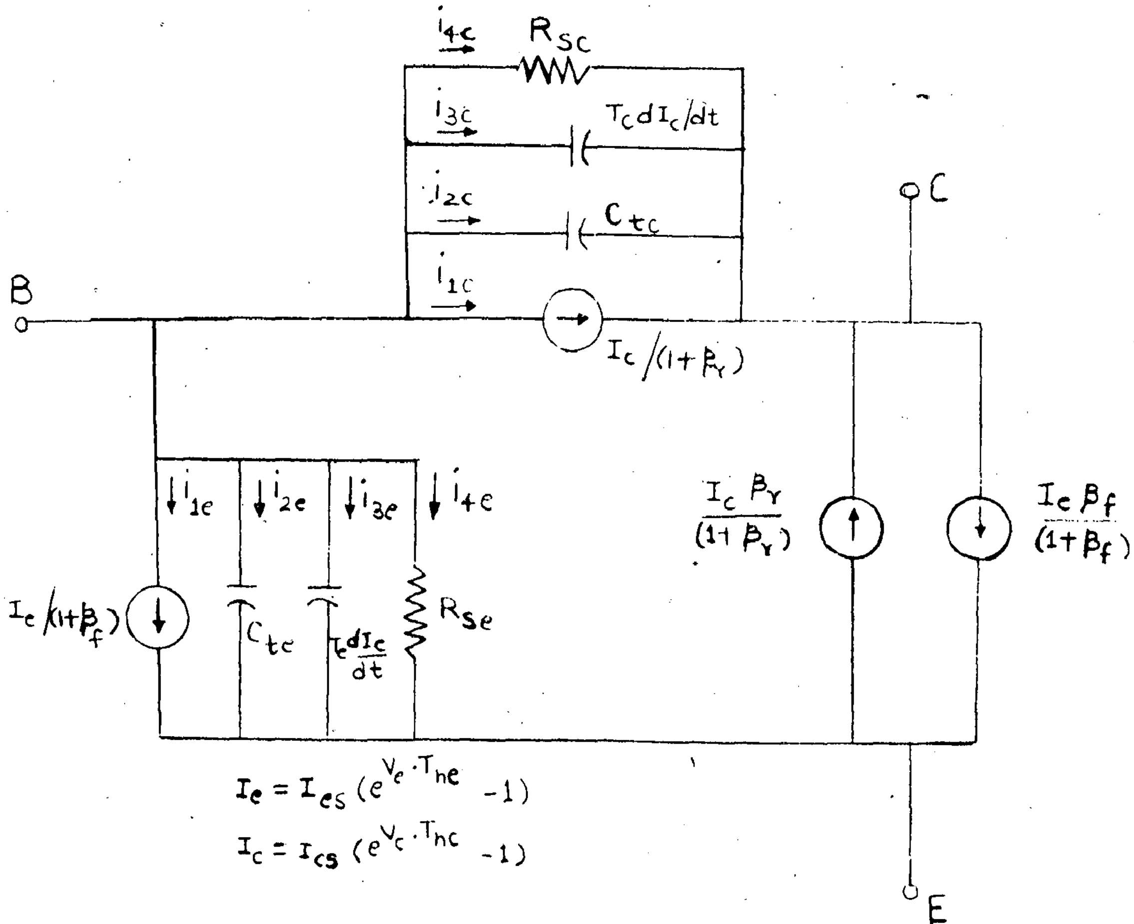


Fig.2.13 : Large signal model for NPN transistor

$$I_C^O = I_e\,\beta_f/(1+\beta_f) - I_c\beta_r/(1+\beta_r) - (1/(1+\beta_r) + T_c/\Delta T)I_c$$

$$- C_{tc}\cdot V_c/\Delta T - V_c/R_{sc} + (T_c\cdot I_c(-1)/\Delta T + C_{tc}\cdot V_c(-1)/\Delta T) \quad \text{.. (2.44)}$$

$$I_E^O = I_c\,\beta_r/(1+\beta_r) - I_e\,\beta_f/(1+\beta_f) - (1/(1+\beta_f) + T_e/\Delta T)I_e$$

$$- C_{te}\ V_e/\Delta T - V_e/R_{se} + (T_e\cdot I_e(-1)/\Delta T + C_{te}\ V_e(-1)/\Delta T) \quad \text{.. (2.45)}$$

Linearizing above equations we have

$$I_B = DERE\,.\Delta V_e + DERC\,.\Delta V_C + I_B^O \quad \text{.. (2.46)}$$

$$I_C = -DERC\,.\Delta V_C - G_c.\Delta V_c\cdot\beta_r/(1+\beta_r) + [\beta_f/(1+\beta_f)]G_e.\Delta V_e + I_C^O \quad \text{.. (2.47)}$$

$$I_E = -DERE.\Delta V_e - [\beta_f/(1+\beta_f)]\ G_e.\Delta V_e + G_c.\Delta V_c.\beta_r/(1+\beta_r) + I_E^O \quad \text{.. (2.48)}$$

where

$$DERE = (1/(1+\beta_f) + T_e/\Delta T)G_e + C_{te}/\Delta T + 1/R_{se}$$

$$DERC = (1/(1+\beta_r) + T_c/\Delta T)G_c + C_{tc}/\Delta T + 1/R_{sc}$$

$$G_e = T_{he}\cdot I_{es}\cdot Exp(V_e\cdot T_{he})$$

$$G_c = T_{hc}\cdot I_{cs}\cdot Exp(V_c\cdot T_{hc})$$

In terms of node voltages these equation can be represented as :

$$I_B = (DERE + DERC).\Delta V_B - DERC.\Delta V_C - DERE.\Delta V_E + I_B^o \quad .. (2.49)$$

$$I_C = (-DERC - \beta_r G_c/(1+\beta_r) + \beta_f G_e/(1+B_f)).\Delta V_B$$
$$+(DERC + G_c \beta_r/(1+\beta_r).\Delta V_C - (\beta_f G_e/(1+\beta_f)).\Delta V_E + I_c^o \quad .. (2.50)$$

$$I_E = (-DERE - \beta_f G_e/(1+\beta_f) + \beta_r G_c/(1+\beta_r)).\Delta V_B$$
$$+(DERE + G_e \beta_f/(1+\beta_f)).\Delta V_E - (\beta_r G_c/(1+\beta_r)).\Delta V_c + I_E^o \quad .. (2.51)$$

Contribution of transistor model to H and B matrices is given as :

$$\Delta H_{BB} = DERE + DERC$$
$$\Delta H_{BC} = -DERC$$
$$\Delta H_{BE} = -DERE$$
$$\Delta H_{CB} = \beta_f Ge/(1+\beta_f) - \beta_r G_c/(1+\beta_r) - DERC$$
$$\Delta H_{CC} = \beta_r G_c/(1+\beta_r) + DERC$$
$$\Delta H_{CE} = -\beta_f G_e/(1+\beta_f)$$
$$\Delta H_{EB} = -\beta_f G_e/(1+\beta_f) + \beta_r G_c/(1+\beta_r) - DERE$$
$$\Delta H_{EC} = -\beta_r G_c/(1+\beta_r)$$
$$\Delta H_{EE} = \beta_f G_e/(1+\beta_f) + DERE$$

$$\Delta B_B = -I_B^o$$

$$\Delta B_C = I_C^o$$

$$\Delta B_E = I_E^o$$

Contribution of PNP transistor to H and B matrices can be determined similarly, the only difference is that the direction of currents and voltages are reversed.

Silicon controlled Rectifier Model :

(i) Gate-cathode Model : In the transient analysis, to determine the instant at which SCR will fire, Gate-cathode modelling is necessary. Fig.2.5 shows the Gate-cathode characteristic of SCR.

This characteristic is similar to that of diode and current varies exponentialy with the voltage,governed by the relation

$$i_g = I_{go}(e^{D_g \cdot V_{gd}} - 1) \qquad .. (2.52)$$

The parameters I_{go} and D_g are found out from the characteristic.

Thus gate-cathode portion of SCR is modelled as a diode with a series resistance which represents the bulk resistance. This is shown in Fig. 2.14a

Linearizing the equation (2.52) we have

$$i_g = i_g(-1) + D_g \cdot I_{go} \cdot \exp(D_g \cdot V_{gd}) \cdot \Delta V_{gd}$$

or $$i_g = i_g(-1) + G_g \cdot \Delta V_{gd} \qquad .. (2.53)$$

Thus gate-cathode model can be represented as in Fig. 2.14b.

The Norton's equivalent of the above model gives the final model shown in Fig. 2.14c

In Fig. 2.14c

$$G_{geg} = G_g(-1)/(1+R_g \cdot G_g(-1))$$

$$I_{geq} = \left[i_g(-1) - G_g(-1) \cdot V_{gd}(-1) \right] / (1+R_g \cdot G_g(-1))$$

Now current for a Newton-Raphson iteration is given as

$$i_g^{o} = G_{geg}(V_g - V_k) + I_{geq} \qquad .. (2.54)$$

Contribution of gate-cathode model to H and B matrices is given as

$$\Delta H_{gg} = G_{geq}$$

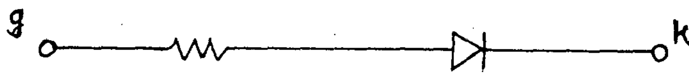
$$\Delta H_{kk} = G_{geq}$$

$$\Delta H_{gk} = -G_{geq}$$

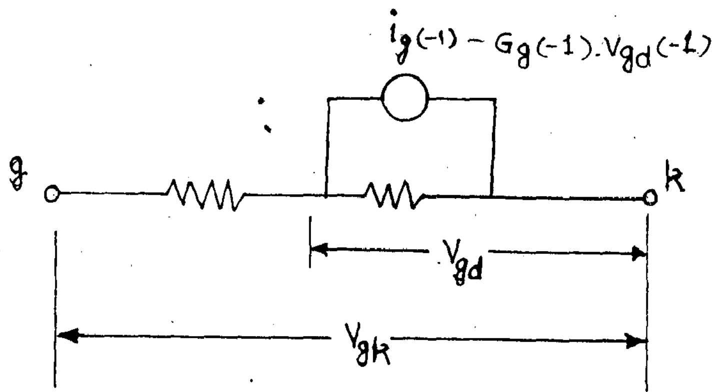
$$\Delta H_{kg} = -G_{geq}$$

$$\Delta B_g = -i_g^{o}$$

$$\Delta B_k = i_g^{o}$$

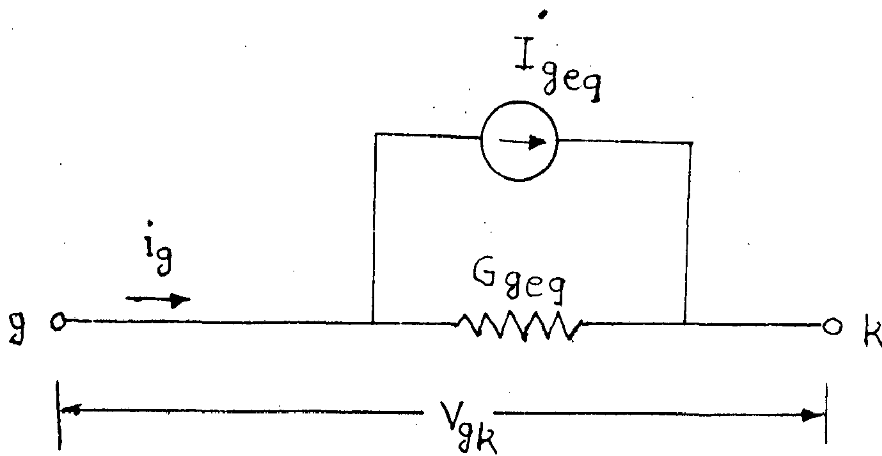


(a)



(b)

Fig 2.14 : GATE - CATHODE MODEL OF SCR



$$I_{geq} = [\, i_g(-1) - G_g(-1) . V_{gd}(-1)] / [1 + R_g . G_g(-1)]$$

$$G_{geq} = G_g(-1) / [1 + R_g . G_g(-1)]$$

(C)

Fig 2.14 (CONTINUED)

After determining new value of V_{gk}, value of V_{gd} is updated as follows :

$$V_{gd} = V_{gk} - i_g . R_g$$

Substituting i_g from (2.53)

$$V_{gd} = V_{gk} - R_g . (i_g(-1) + G_g(-1).(V_{gd} - V_{gd}(-1)))$$

or $$V_{gd} = [V_{gk} - R_g.(i_g(-1) - G_g(-1).V_{gd}(-1)]/(1+R_g.G_g(-1)) \quad .. (2.55)$$

Because of the presense of exponential non-linearity convergence may be slow. To improve the behaviour of Newton-iteration the advantage of exponential characteristic is taken as follows |11|.

Instead of calculating new value of i_g from equation (2.52), it is calculated by

$$i_g = i_g(-1) + G_g(-1) [V_{gd} - V_{gd}(-1)] \quad .. (2.56)$$

and after this value of V_{gd} is modified as

$$V_{gd} = \frac{1}{D_g} . \ln(I_g/I_{go} + 1) \quad .. (2.57)$$

and G_g is obtained as

$$G_g = D_g . (i_g + I_{go}) \quad .. (2.58)$$

Iteration begins by choosing V_{gd} and calculating G_g and i_g. Using these values G_{geq} and i_{geq} are determined. Using H and B matrices correction vector is

obtained. After applying correction new value of V_{gk} is obtained. Using eq. (2.55) V_{gd} is evaluated. Equations (2.56), (2.57) and (2.58) are then used to calculate i_g, modified V_{gd} and G_g.

This gate-cathode model is applicable to all states of SCR, namely on, off, turn-on period and turn-off period.

(ii) Anode-cathode model : Fig. 2.6 shows anode-cathode characteristic of SCR. For each working state of SCR, a different model has to be used. In present work four different models have been used to represent these working states. These states are :

i) Off-state
ii) Turn-on period
iii) On -state
iv) Turn-off period

(i) Off-state : Small leakage current flows through SCR in off-state and is modelled as a high resistance. Value of the resistance offered in this state is equal to slope of anode-cathode characteristic in off-state. Thus contribution of SCR during off state is found out in a way described in resistance model.

(ii) Turn-on period : Fig. 2.15 shows the anode-cathode characteristic during turn-on period |12|. V_o is the anode-cathode voltage at the instant at which turn-on process begins i.e. when gate current reaches trigerring value. During the delay time t_d, this voltage remains constant. After this voltage falls exponentially. During this period current increases exponentially. t_r represents rise time.

Thus anode-cathode model during turn-on time is taken as time dependent voltage source. Since with ideal voltage source, the calculation of contributions to H and B matrices is impossible, a small resistance r is added in series with time dependent voltage source. Fig. 2.16 shows the model.

Now current for a Newton-Raphson iteration is written as

$$i_f^o = (V_A - V_K - V_t)/r \qquad .. (2.59)$$

and current through SCR

$$i_f = \Delta H \cdot (\Delta V_A - \Delta V_K) + i_f^o \qquad .. (2.60)$$

where $\Delta H = 1/r$

The contribution of this model to H and B matrices is given as :

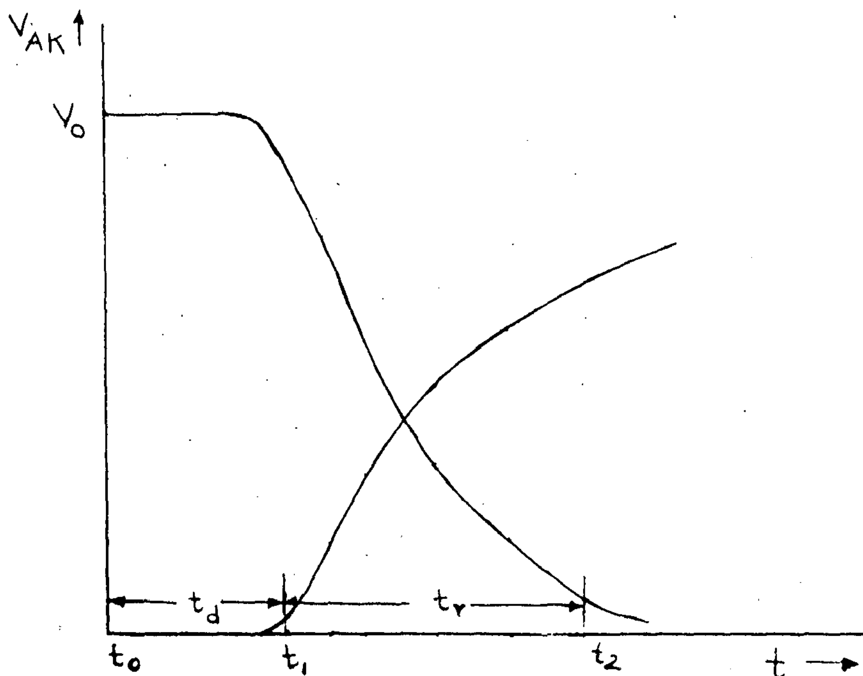


Fig.2.15 : Turn-on characteristic of SCR

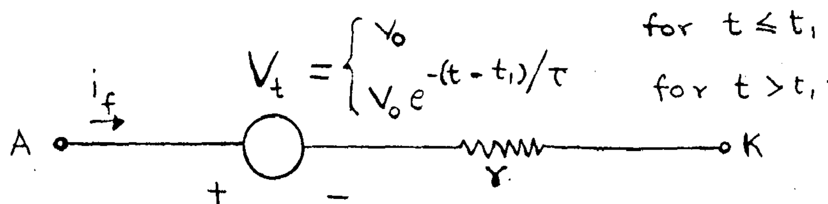


Fig. 2.16 : Anode-cathode model of SCR for turn-on period

$$\Delta H_{AA} = \Delta H$$

$$\Delta H_{KK} = \Delta H$$

$$\Delta H_{AK} = -\Delta H$$

$$\Delta H_{KA} = -\Delta H$$

$$\Delta B_{A} = -i_f^{o}$$

$$\Delta B_{K} = i_f^{o}$$

(iii) On-state : During fully on condition anode-cathode characteristic is exponential.

Fig. 2.17a shows the model of SCR in on condition. R_f is the bulk resistance.

The current i_f is given by

$$i_f = I_{fo} \, (e^{D_f \cdot V_{fd}} - 1) \quad .. \, (2.61)$$

D_f and I_{fo} are parameters associated with exponential characteristic.

This model is analyzed similar to gate-cathode model.

Fig. 2.17b show the equivalent model derived by using linearized version of equation (2.61)

In this model

$$G_f = D_f \cdot I_{Fo} \cdot \text{Exp}(D_f \cdot V_{fd}) \quad .. \, (2.62)$$

The model of Fig.2.17b is further simplified using its Norton equivalent. Fig. 2.17c shows this model which is used to calculate contributors to H and B matrices.

For the model of fig. 2.17c

$$G_{feq} = G_f(-1)/(1+R_f \cdot G_f(-1)) \quad .. (2.63)$$

$$I_{feq} = [i_f(-1) - G_f(-1).V_{fd}(-1)]/(1+R_f \cdot G_f(-1)) \quad .. (2.64)$$

Current for a Newton-Raphson iteration is given as

$$i_f^{o} = G_{feq}(V_A - V_K) + I_{feq} \quad .. (2.65)$$

and the forward current

$$i_f = G_{feq}(\Delta V_A - \Delta V_K) + i_f(-1) \quad .. (2.66)$$

Contributing of anode-cathode model to H and B matrices is given as

$$\Delta H_{AA} = G_{feq}$$

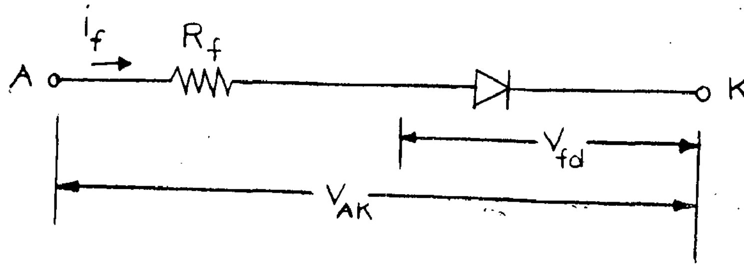
$$\Delta H_{KK} = G_{feq}$$

$$\Delta H_{AK} = -G_{feq}$$

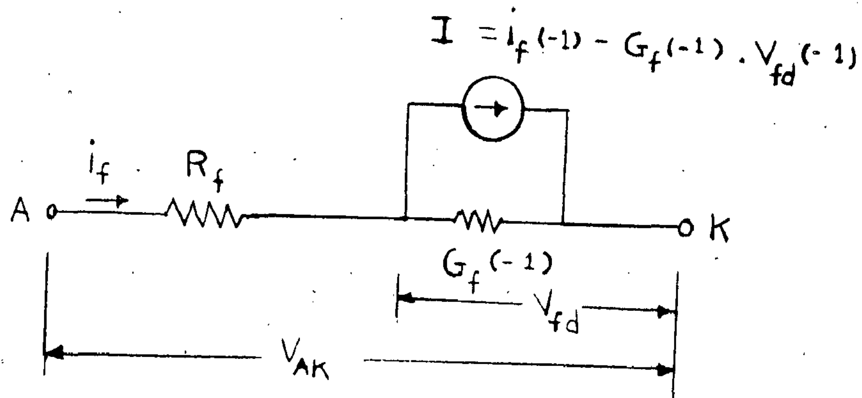
$$\Delta H_{KA} = -G_{feq}$$

$$\Delta B_A = -i_f^{o}$$

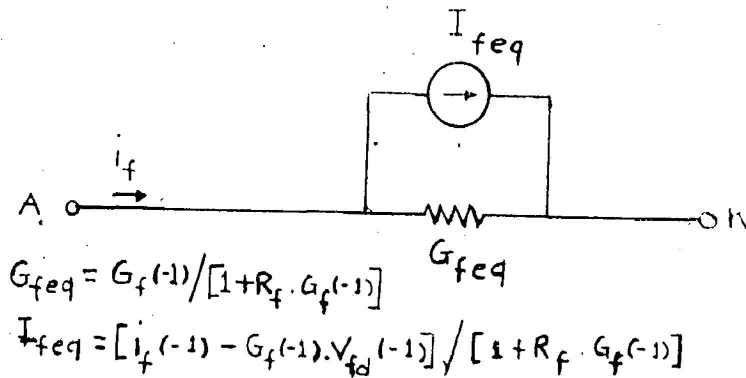
$$\Delta B_K = i_f^{o}$$



(a)



(b)



(c)

Fig.2.17 : Anode-cathode model of SCR for on-state.

After determining new value of V_{AK}, value of
is updated using.

$$fd=[V_{AK}-R_f.(i_f(-1)-G_f(-1).V_{fd}(-1)]/(1+R_f.G_f(-1)) \quad .. (2.67)$$

nprove the behaviour of Newton-Raphson method, V_{fd} is
fied in the following steps.

$$i_f = i_f(-1) + G_f(-1).\ [V_{fd}- V_{fd}(-1)] \quad .. (2.68)$$

$$V_{fd} = \frac{1}{D_f} . l_n (i_f/I_{fo} + 1) \quad .. (2.69)$$

value of G_f is obtained by

$$G_f = D_f.\ (i_f+ I_{fo}) \quad .. (2.70)$$

Turn-off period : Fig.2.18 shows anode-cathode
acteristic of SCR during turn-off period.

The turn-off process starts when forward current falls
w holding current I_H. The change in carrier densities
he inner p and n layer will follow the current decay
a certain delay |12|. Even though supply voltage
rses at t_1, the conductivity of the junctions are kept
y the carriers stored in the layer. Thus current may
in the reverse direction without changing its rate of
ge. Removal of carriers by reverse current reduces carrier
ity to such an extent that reverse voltage build up starts
instant t_2 on, and current falls exponentially.

Emprically|10|, it has been found for most of the SCR's

$$t_s = (t_2 - t_1) = 0.6\ t_{rr} \qquad \text{.. (2.71)}$$

where

t_s is storage time

and t_{rr} is reverse recovery time.

Thus SCR, during turn-off period, is modelled as time dependent current source. This model is shown in Fig. 2.19.

$$I_t = \begin{cases} I_H - DIDT * (t - t_o) & \text{for } t \leq t_2 \\ I_{RM} e^{-t/\tau} & \text{for } t > t_2 \end{cases}$$

where DIDT is rate of change of current at t_o.

IRM is maximum value of reverse recovery current

and $\tau = 0.1820\ t_{rr}$.

Now current at a Newton-Raphson iteration can be written as

$$i_f^o = I_t \qquad \text{.. (2.72)}$$

Hence contribution of this model to H and B matrices can be given as

$$\Delta H_{AA} = 0$$

$$\Delta H_{KK} = 0$$

$$\Delta H_{AK} = 0$$

$$\Delta H_{KA} = 0$$

$$\Delta B_A = -i_f^o$$

$$\Delta B_K = i_f^o$$

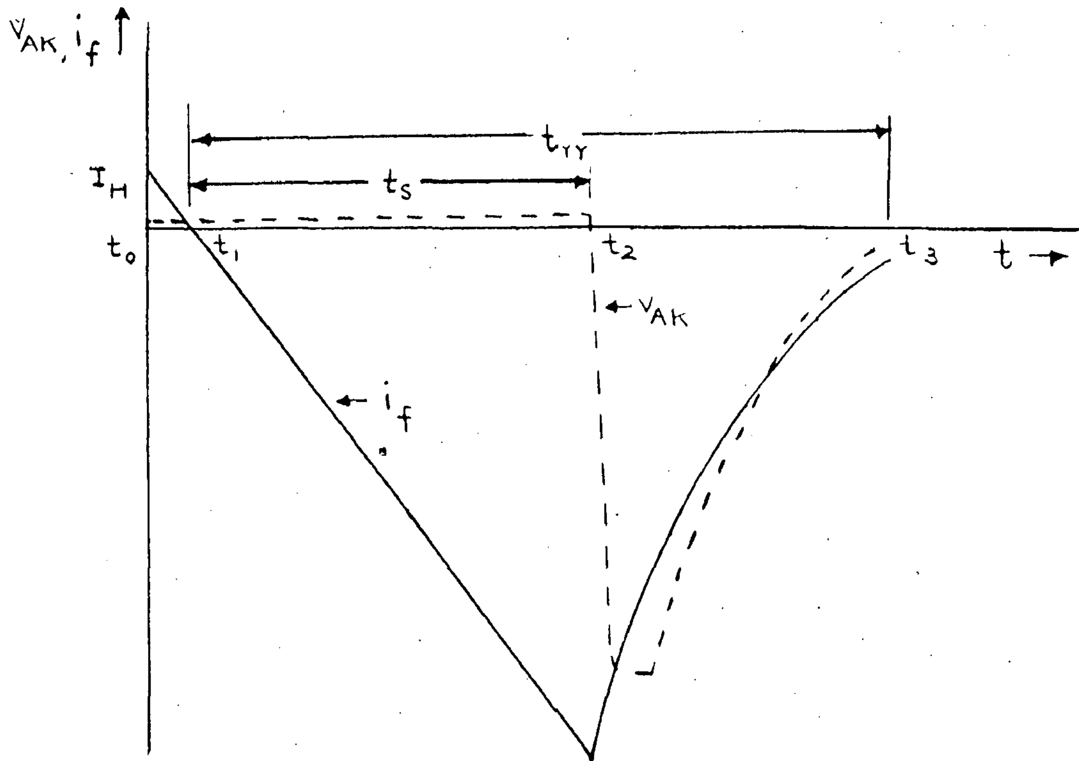


Fig.2.18 : Turn-off characteristics of SCR.

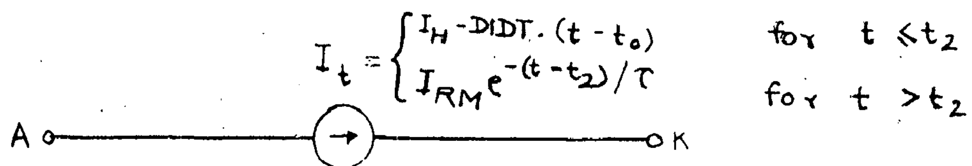


Fig.2.19 : Anode-cathode model of SCR for turn-off period

Triac Model : Triac is a three terminal device and conducts in both directions, unlike SCR. Infact it is equivalent to two SCR's connected in anti-parallel or back to back. Fig. 2.20a shows characteristic of Triac.

The characteristics in the two directions are symmetrical. Triac can be turned on by one of the following ways :

i) V_{AK} positive and i_g positive

ii) V_{AK} negative and i_g positive

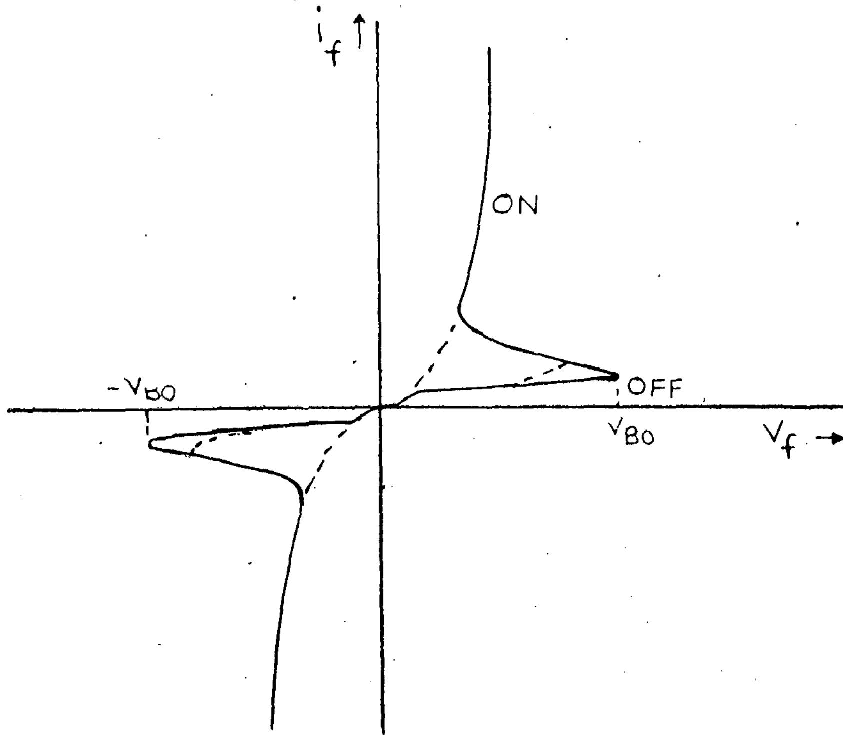
iii) V_{AK} positive and i_g negative

iv) V_{AK} negative and i_g negative

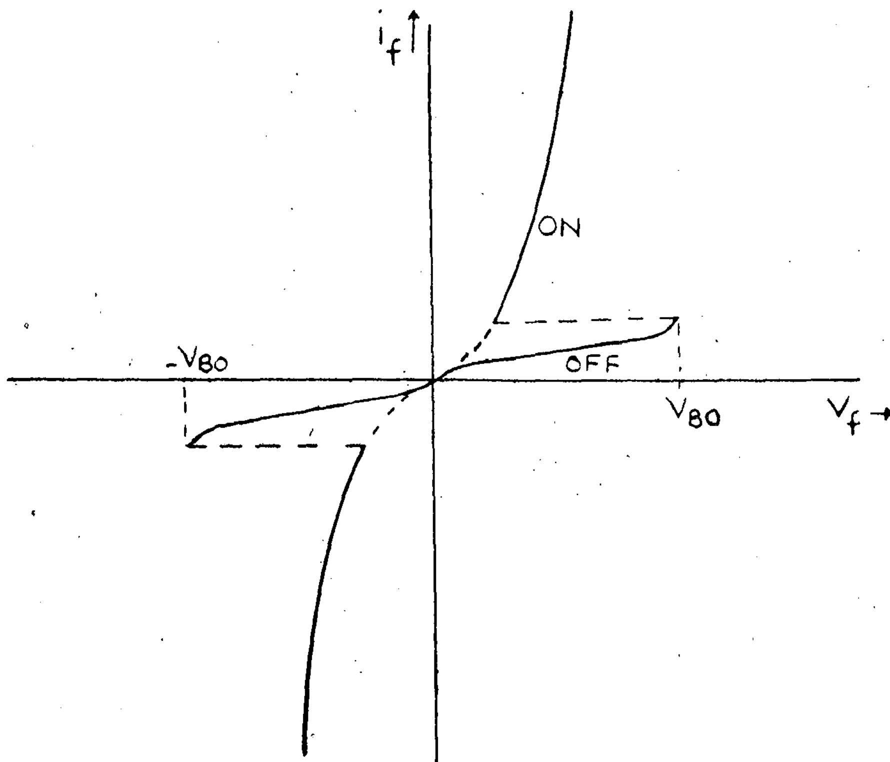
The models derived for SCR are used for triac also with minor modifications. I_{go} and D_g becomes negative when V_{GK} is negative. Similarly I_{fo} and D_f becomes negative when V_{AK} is negative.

Diac Model : Diac is a two terminal device and it starts conducting when voltage of either polarity across its terminals cross a particular value. Fig. 2.20b shows its characteristic.

Diac is modelled **similar** to anode-cathode model of SCR. However condition for the turn-on is different here and since it conducts in both directions the parameters associated with exponential characteristic changes its sign according to polarity of applied voltage.



(a) Characteristic curve of Triac



(b) Characteristics curve of diac

Fig.2.20 : Triac and diac characteristics

2.3.2 METHOD :

Due to presence of non-linearity in the characteristics of most of the electronic devices, circuit equations of electronic circuits are highly non-linear. The degree of non-linearity present causes Newton's method, in which second and higher order derivatives are neglected, to give slow convergence and sometimes overflow. However inclusion of second and higher order derivatives makes solution procedure complex.

The algebric and differential equations representing transient behaviour of circuit are of the form

$$G(W, q, \dot{q}, t) = 0 \qquad .. (2.73)$$

The vector G comprises Kirchhoff's voltage and current equations, and the branch constitutive equations. Circuit analysis involves computation of vectors $W(t)$ and $q(t)$ by solving (2.73), for time interval $t_o \leqslant t \leqslant t_{max}$.

For most of the electronic circuits, these equations are stiff i.e. their time constants are widely separated. For such equations ordinary solution methods are not applicable. In present work implicit numerical integration method, which involves discretization of differential equations, is used to solve circuit equations |3|.

The interval $[t_o, t_{max}]$ is divided by non-uniform time steps $h_j = t_j - t_{j-1}$ into discrete points $t_o, t_1, t_2 .. t_N$

and $\dot{q}(t)$ at each time step is discretized. $\dot{q}_i(t_j)$ is discretized by backward Euler method as

$$\dot{q}_i(t_j) = \frac{q_i(t_j) - q_i(t_{j-1})}{h_j} \quad .. (2.74)$$

and truncation error is

$$T_E = h_j[q_i(t_j) - q_i^p(t_j)]/(h_j+h_{j-1}+h_{j-2}) \quad .. (2.75)$$

where

$$q_i^p(t_j) = \gamma_1 q_i(t_{j-1}) + \gamma_2 q_i(t_{j-2}) + \gamma_3 q_i(t_{j-3}) \quad .. (2.76)$$

$$\gamma_1 = (h_j+h_{j-1})(h_j+h_{j-1}+h_{j-2})/(h_{j-1})(h_{j-1}+h_{j-2}) \quad .. (2.77)$$

$$\gamma_2 = h_j(h_j+h_{j-1}+h_{j-2})/(-h_{j-1})(h_{j-2}) \quad .. (2.78)$$

$$\gamma_3 = h_j(h_j+h_{j-1})/(h_{j-2})(h_{j-1}+h_{j-2}) \quad .. (2.79)$$

Thus discretizing each component of $\dot{q}(t_j)$ at each time point t_j, the circuit equation become :

$$G(W(t_j), q(t_j)) = 0 \quad .. (2.80)$$

This is a set of non-linear equations to be solved for $W(t_j)$ and $q(t_j)$. For sufficiently small step size h_j, the solution of eq. (2.80) is in general very close to the solution at preceeding time step i.e. at each point previous solution gives a good estimate of the current solution.

From the device models H and B matrices are computed and correction vector ΔV is calculate using

$$H \cdot \Delta V = B \qquad .. (2.81)$$

If the correction at each node is less than a specified value the process is terminated and solution at that time point is said to be obtained. Otherwise H and B matrices are again computed using corrected value of node voltages.

Time step is adjusted according to value of truncation error.

2.3.3 ALGORITHM :

The stepwise procedure for transient analysis |14| can be written as.

1. Given the initial time t_o and initial conditions, $W(t_o)$ and $q(t_o)$ are determined. Select initial step size h and set $i = 1$.
2. Set $t_i = t_{i-1} + h_i$
3. Discretize $\dot{q}(t_i)$
4. Solve the non-linear circuit equations (2.80) for $W(t_i)$ and $q(t_i)$ using modified Newton's method.
5. Estimate the truncation error in the discretization. If truncation error is more than pre-specified value set $h_i = h_i/2$ and go to step 2. Else compute new time step h_{i+1}, such that h_{i+1} is the maximum value for which the corresponding

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truncation error is comensurate with the used specified error.

6. If $t_i < t_{max}$, set i = i+1 and go to step 2. Else stop.

EXAMPLES :

EXAMPLE 2.1 : Fig. 2.21 shows a simple series inverter circuit. This circuit is analyzed with $L_1 = L_2 = 0.05$ mH, C = 1.25 uF , R = 1 ohm. and V = 10V. Fig. 2.22a and 2.22b show voltage and current profiles obtained for TH1, during turn-on period. Fig. 2.23a and 2.23b show the voltage and current profiles obtained for TH2, during turn-off period. Fig. 2.24a and 2.24b show the gate signals and output current of inverter for one cycle. Circuit analysis was carried out for two cycles of inverter output and the loadings obtained for different components are as follows :

Capacitor C	:	Max. voltage across terminals = 15.81V
Inductor L1	:	Power dissipation = 0.036 watts
Inductor L2	:	Power dissipation = 0.039 watts
Resistor R	:	Power dissipation = 0.84 watts
Thyristor TH1	:	Average current = 0.35 Amp.
Thyristor TH2	:	Average current = 0.39 Amps.

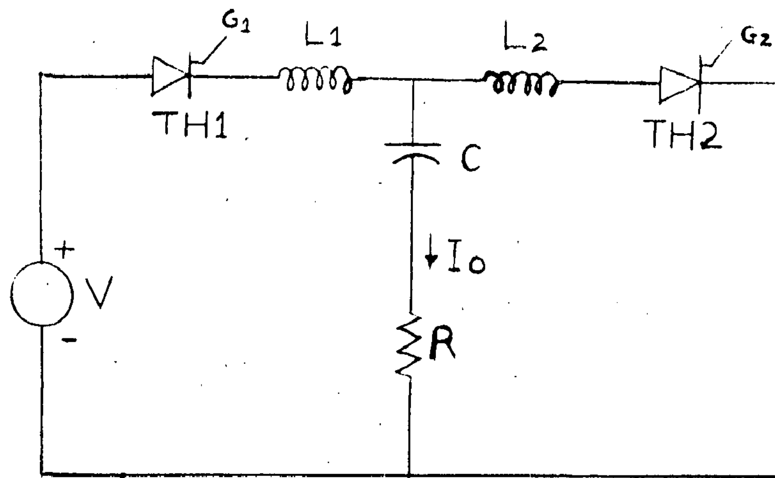
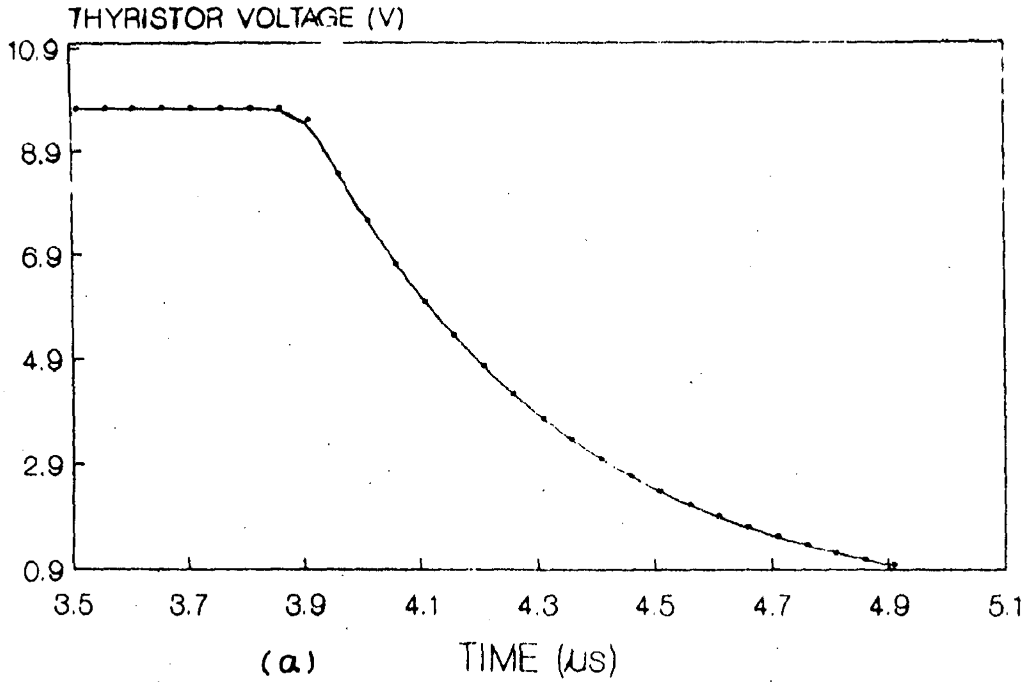


Fig.2.21 : Series inverter circuit (example 2.1)



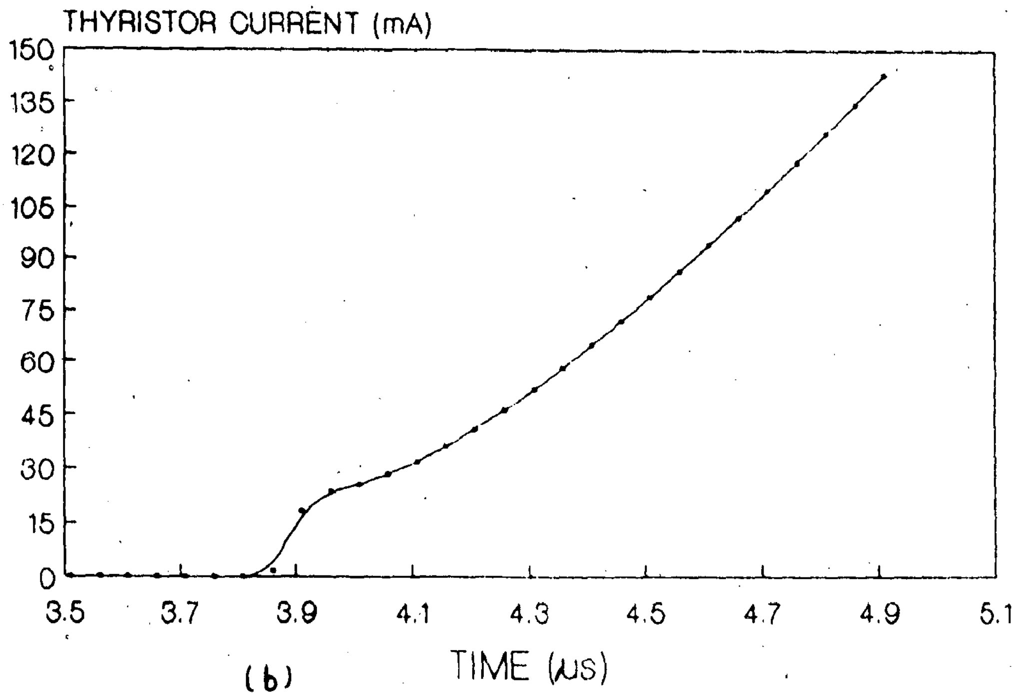
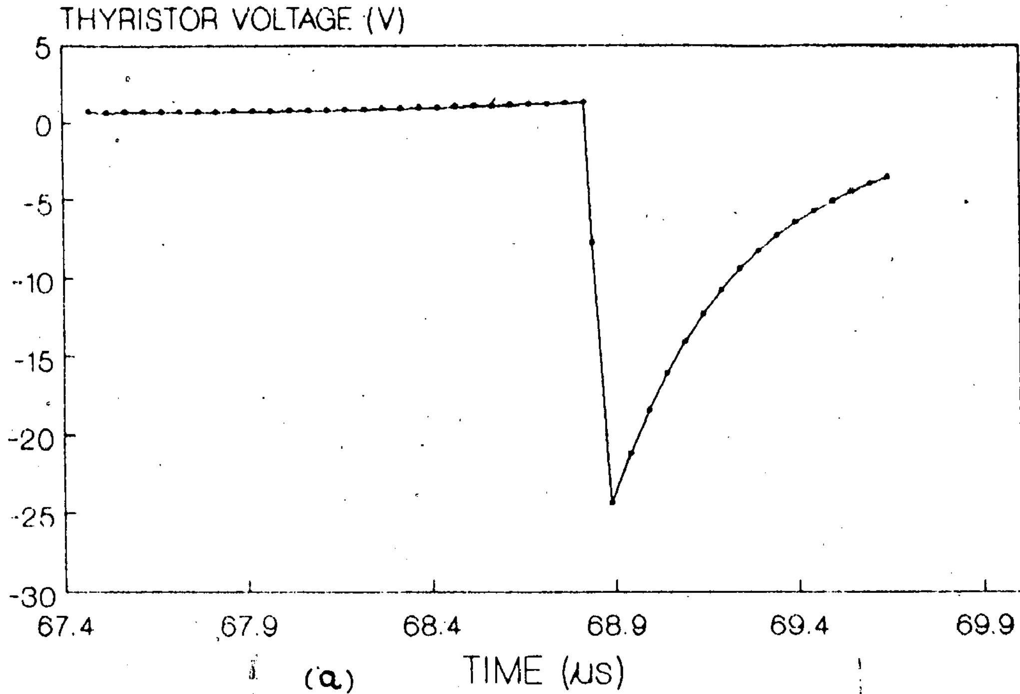


Fig. 2.22 : Turn-on characteristics of TH1(Example 2.1)



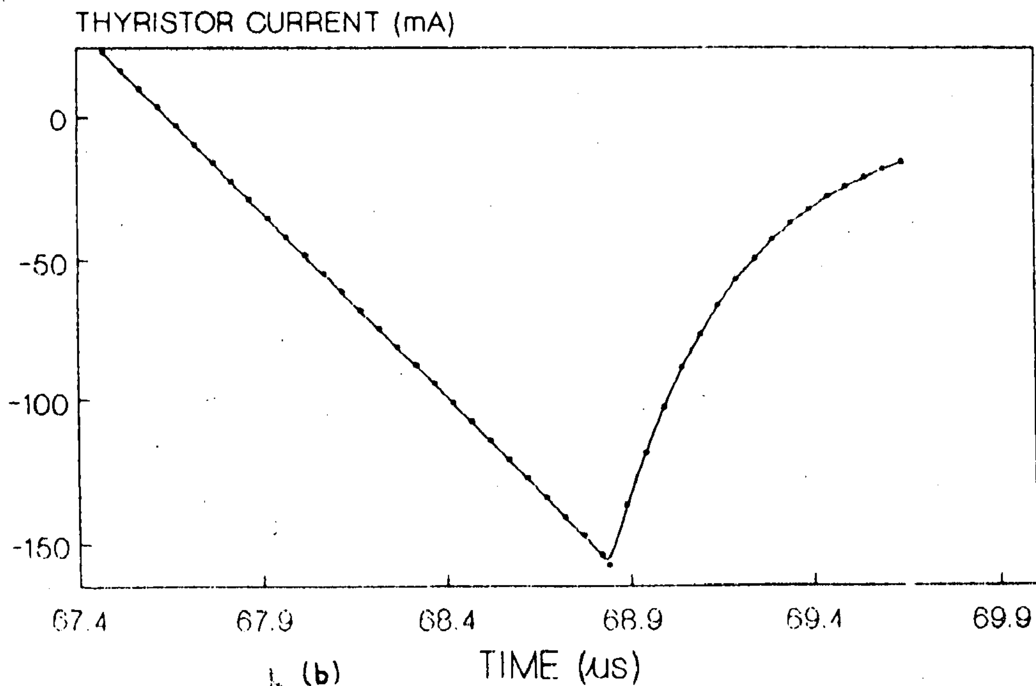
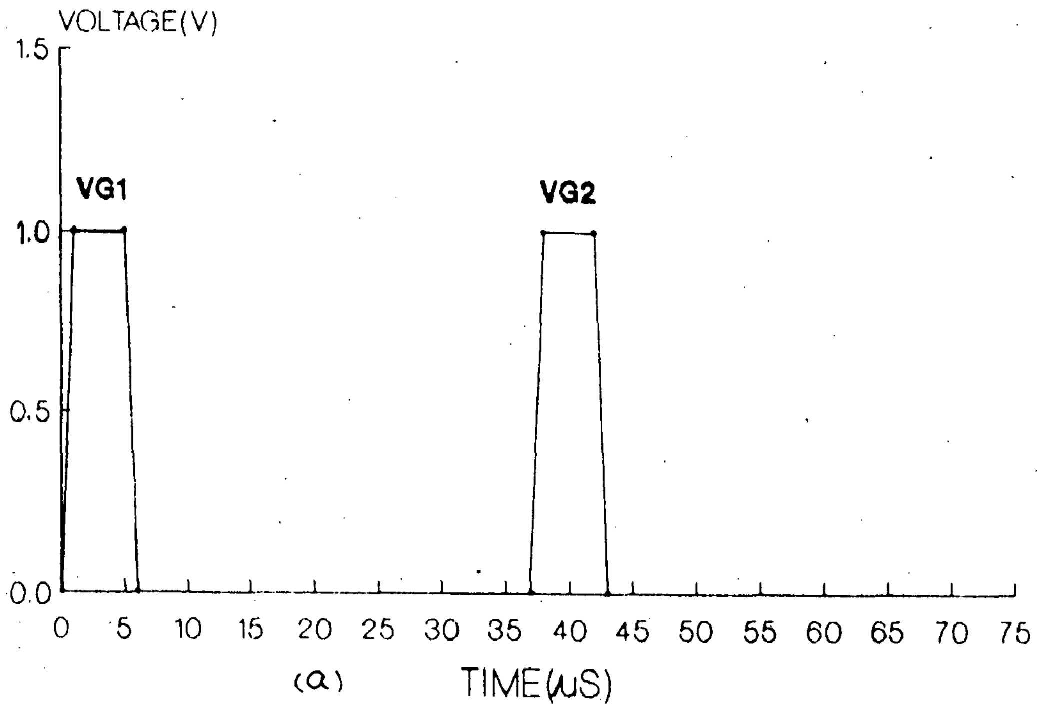


Fig.: 2.23: Turn-off characteristics of TH2 (example 2.1)



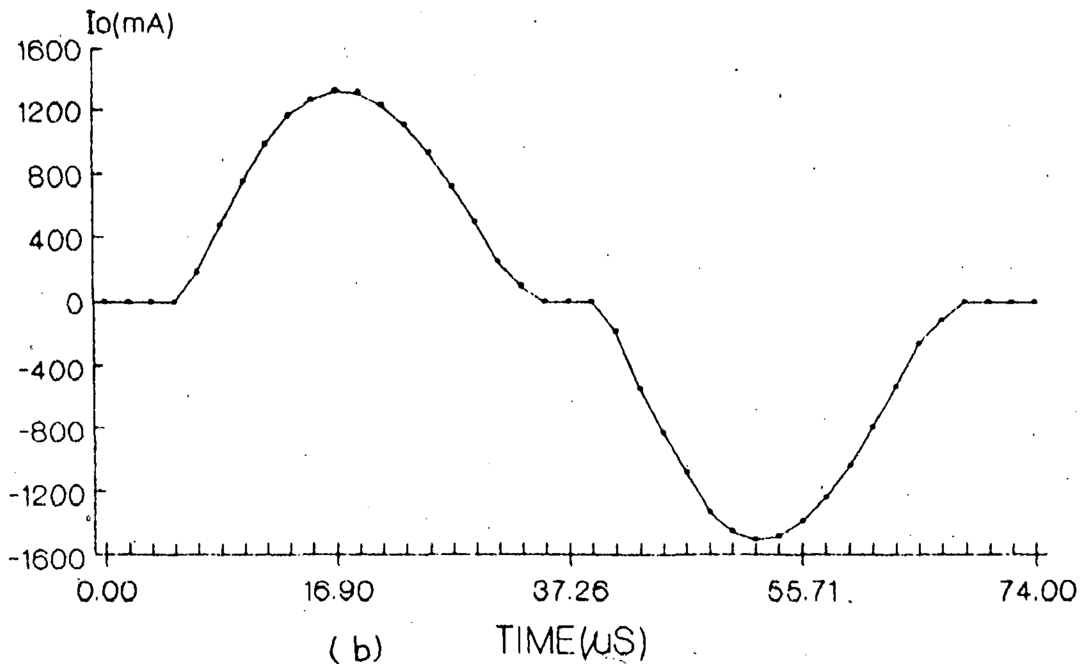


Fig.2.24 : Gate signals and output current of inverter circuit (example 2.1)

EXAMPLE 2.2 :

A bipolar ECL Schmitt trigger circuit shown in Fig. 2.25 is considered for circuit analysis. The input is set to a trapezoidal function as shown in Fig. 2.26. The transient analysis is performed for 100 ns. The output waveform is shown in Fig. 2.26, Loadings of different components are as follows :

Resistor R_1 : Power dissipation = 0.0605 watts
Resistor R_2 : Power dissipation = 0.032 watts
Resistor R_3 : Power dissipation = 0.011 watts
Resistor R_4 : Power dissipation = 0.0051 watts
Resistor R_5 : Power dissipation = 0.086 watts
Transistor T_1 : Power dissipation = 0.0604 watts
collector-emitter voltage = 2.65V
Transistor T_2 : Power dissipation = 0.0124 watts
collector-emitter voltage = 2.51V

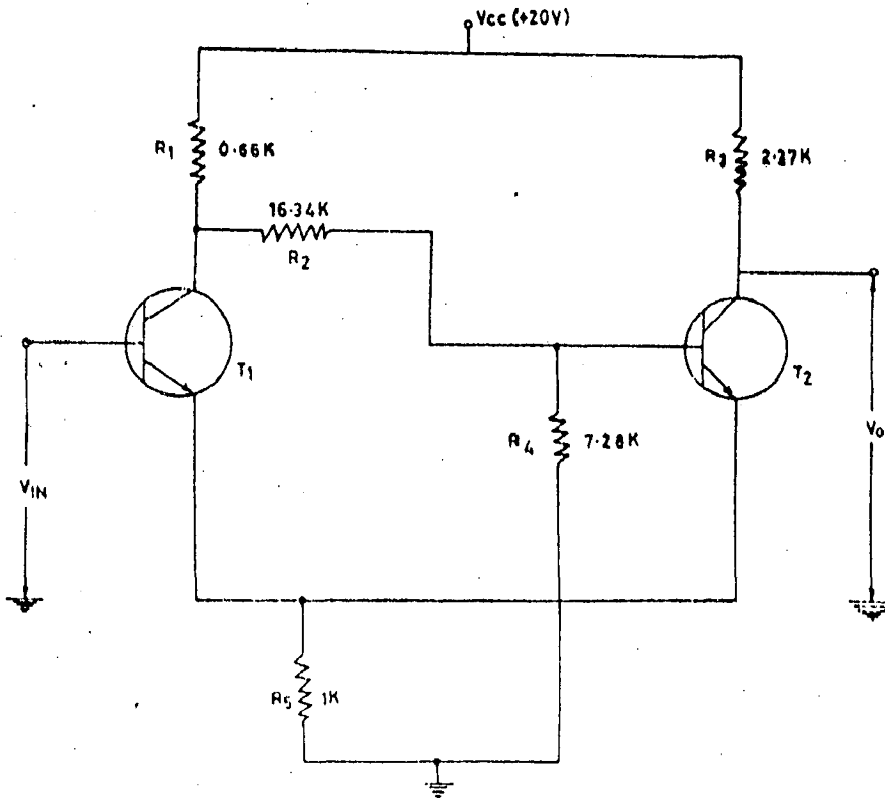


Fig.2.25 : ECL Schmitt trigger circuit(Example 2.2)

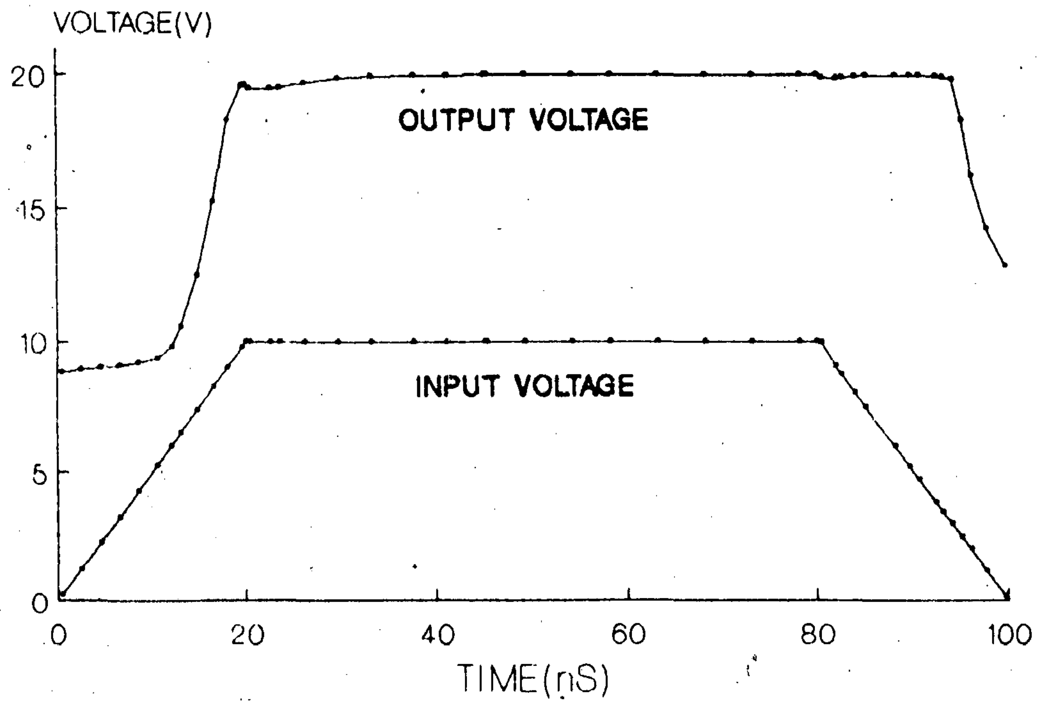


Fig.2.26 : Input-output characteristics of ECL Schmitt trigger circuit (example 2.2)

CHAPTER-3

RELIABILITY EVALUATION OF ELECTRONIC CIRCUITS

3.1 INTRODUCTION :

With growing use of electronic circuits at sensitive places, where their failure may paralyze a system of great importance, reliability is fast emerging as an important attribute of electronic circuits. Now-a-days it is a standard practice to incorporate reliability considerations at design stage. The circuit reliability analysis furnishes the designer an estimate of the theoretically achievable reliability and points out areas of high-failure rate concentration in large circuits. The areas of high failure rate may then be eliminated either by using highly reliable components, derating, or redundancy techniques.

In this chapter two methods of reliability prediction for electronic circuits are discussed. These methods are as per MIL-HDBK-217D|1|. These methods are :

(i) Parts count method

(ii) Part stress analysis.

Neither of the above methods applies to nuclear environment nor do they consider the effects of ionizing radiation. Also failures due to secondary breakdown which are quite common in power electronic circuits are not covered by these methods. These secondary failures take place in due

course of time (few days to few months) and are caused by overstress due to high di/dt, dv/dt and electrical transients. In the absence of reliability data for secondary failures, normal practice is to determine maximum di/dt, maximum dv/dt, peak voltage and current and keep them much below specified value. In developing countries this aspect at analysis level has not been taken care in most of the cases, resulting in enormous failures in the field of power electronic circuits. Developed countries do not report the technology status on these stresses.

In present work the stresses are determined from circuit analysis. The reliability is determined using part stress analysis.

3.2 PARTS COUNT METHOD :

This method is generally applied during early design phase. The information needed to apply this method is (1) generic part types and quantities (2) part quality levels and (3) equipment environment.

Failure rate in this method is expressed as

$$\lambda_{total} = \sum_{i=1}^{n} N_i (\lambda_G . \pi_Q)_i \qquad .. (3.1)$$

for a given equipment environment.

where :

λ_{total} = total equipment failure rate (failures/10^6hrs)

λ_G = generic failure rate for i^{th} generic part (failures/10^6hrs).

π_Q = quality factor for i^{th} generic part

N_i = quantity of ith generic part

n = number of different generic part categories.

However if different parts of the equipment operate in different environments than equation (3.1) is applied to each portion of equipment under a specific type of environment. These failure rates are now added to get equipment failure rate. Various types of environments are listed in table 3.1.

The quality factors to be used with each part type are available with applicable λ_G tables in MIL-HDBK-217D.

3.3 PART STRESS ANALYSIS :

This method is applicable when most of the design is finalized and part list with part stressesis available. Besides this, method may require information such as part quality level, environment, application, temperature, frequency, level of complexity, construction class, rating etc.

TABLE 3.1 : ENVIRONMENTAL SYMBOL AND DESCRIPTION

ENVIRONMENT	π_E SYMBOL	DESCRIPTION
Ground, Benign	G_B	Nonmobile, laboratory environment readily accessible to maintenance
Ground, Fixed	G_F	Conditions less than ideal such as in unheated building
Ground, Mobile	G_M	Conditions with vibrations and shocks
Space, Flight	S_F	Earth orbital, includes satellites and Shuttles
Manpack	M_p	Portable equipment, transported manually while in operation.
Naval, Sheltered	N_S	Sheltered or below deck conditions, protected from weather conditions
Naval, unsheltered	N_U	Shipborne equipment exposed to weather conditions
Naval, undersea, unsheltered	N_{UU}	Equipment immersed in salt water
Naval, Submarine	N_{SB}	Equipment installed in submarines.
Naval, Hydrofoil	N_H	Equipment installed in hydrofoil vessel
Air borne, Inhabited, Transport	A_{IT}	Conditions in transport or bomber compartments without environmental extremes of pressure, temperature or shock
Airborne, Inhabited, Fighter	A_{IF}	Same as A_{IT} but installed on high performance aircraft
Airborne, uninhabited, Transport	A_{UT}	Condition with extreme pressure, vibration and temperature, installed on long mission aircraft.

Table 3.1 (contd.)

ENVIRONMENT	π_E SYMBOL	DESCRIPTION
Airborne, uninhabited, Fighter	A_{UF}	Same as A_{UT} but installed on high performance aircraft
Airborne, Rotary, Winged	A_{RW}	Equipment installed on helicopters.
Missile, Launch	M_L	Severe conditions related to missile, space vehicle launch and landing by parachute
Cannon, Launch	C_L	Extremely severe conditions related to cannon launching
Undersea, Launch	U_{SL}	Conditions related to undersea torpedo and missile launch
Missile, Free Flight	M_{FF}	Missiles in non-powered free flight
Airbreathing Missile, Flight	M_{FA}	Conditions related to powered flight of air breathing missile

3.3.1 PART QUALITY :

The quality of the part directly affects the part failure rate. This fact is taken into account in failure rate model by a factor π_Q. Table 3.2 shows various parts with their quality designators. This table do not cover the parts with older specification known as Non-ER. Under this specification, a part has one of two quantity designators namely "MIL.SPEC" and "Lower". If the part is procured in complete accordance with the applicable specification, the quality designator "MIL.SPEC." should be used. If any requirements are waived, or if commercial part is procured, the quality designator "Lower". should be used.

For discrete semiconductors, sealed or encapsulated with organic materials, another quality designator "PLASTIC" is used.

3.3.2 ENVIRONMENT :

To take environmental stresses into account, all part reliability models use the environmental factor, π_E. Table 3.1 gives description of these environments. If an equipment experiences more than one environment during its use, reliability analysis should be segmented.

3.3.3 PART FAILURE RATE MODELS :

Part failure rate model for most of the electronic devices is of the type

$$\lambda_p = \lambda_b \cdot \prod_{i=1}^{n} \pi_i$$

where

λ_p is the part failure rate

λ_b is the base failure rate usually expressed by a model relating the influence of electrical and thermal stresses on the part.

π_i is i^{th} type of π factor that modifies the base failure rate for a parameter affecting part reliability.

n is no. of π factor to be used for the part.

π_E, the environmental factor and π_Q, the quality factor are used with all parts. Other π factors differ from one part to other.

Base failure rate models for different electronic components are described below. These models include both catastrophic and drift failures. Failures associated with connection of parts into circuit assemblies are not included in these models.

(a) Resistor failure rate model : The general model for resistors is as follows :

$$\lambda_p = \lambda_b(\pi_E \cdot \pi_R \cdot \pi_Q) \qquad \text{failures}/10^6 \text{ hrs.}$$

For variable resistors the model is :

$$\lambda_p = \lambda_b(\pi_{TAPS} \cdot \pi_R \cdot \pi_V \cdot V_C \cdot \pi_E \cdot \pi_Q)$$

failures/10^6 hrs.

The π factors for resistors are defined in table 3.3.

The general model for base failure rate of resistors is as follows :

$$_b = Ae^{B\left(\frac{T+273}{N_T}\right)^G} e^{\left[\left(\frac{S}{NS}\right)\left(\frac{T+273}{273}\right)^J\right]^H}$$

where

A is an adjustment factor for each type of resistor to adjust the model to the appropriate failure rate level.

e is the natural logarithm base

T is the ambient operating temperature (degrees C)

N_T is a temperature constant

B is a shaping parameter

H,H,J are acceleration constants

N_S is a stress constant

S´ is the electrical stress and is the ratio of operating power to rated power.

(b) Capacitor failure rate model :

The general model for capacitors is as follows :

$$\lambda_p = \lambda_b(\pi_E . \pi_{CV} . \pi_{SR} . \pi_Q . \pi_C) \text{ failures}/10^6 \text{ hrs.}$$

where λ_b is base failure rate and λ_p is part failure rate. Various π factors used in the model are defined in table 3.3.

For capacitors the general model of base failure rate (λ_b) is as follows :

$$\lambda_b = A\left[\left(\frac{S}{NS}\right)^H + 1\right] e^{B\left(\frac{T+273}{NT}\right)^G}$$

where

A is an adjustment factor to adjust the model to the proper failure rate. Its value is different for different type of capacitors.

S is the ratio of operating to rated voltage, operating voltage is the sum of the applied D.C. voltage and the peak a.c. voltage.

NS is the stress constant

e is the natural logarithm base

T is the operating ambient temperature in degree centigrade.

N_T is a temperature constant

B is a shaping parameter

G and H are acceleration constants.

(c) Inductor failure rate model :

The general model for inductors is as follows :

$$\lambda_p = \lambda_b(\pi_E \cdot \pi_Q \cdot \pi_c) \quad \text{failures}/10^6 \text{ hrs}$$

where

λ_p = part failure rate

λ_b = base failure rate

π_E = Environmental factor

π_Q = Quality factor

π_c = construction factor (fixed or variable)

The general model for base failure rate is :

$$\lambda_b = Ae^X \text{ where } X = \left(\frac{T_{HS} + 273}{N_T}\right)^G$$

where

T_{HS} = Hot spot temperature in degree centigrade

e = Natural logarithm base

N_T = Temperature constant

G = Acceleration constant

A = Adjustment factor for different insulation classes.

(d) Transformer failure rate model :

The general model for transformers is :

$$\lambda_p = \lambda_b(\pi_E \cdot \pi_Q) \quad \text{failures}/10^6 \text{ hrs}$$

where

λ_p = part failure rate

λ_b = base failure rate

π_E = Environmental factor

π_Q = Quality factor.

The general model for base failure rate is :

$$\lambda_b = Ae^X \quad \text{where} \quad X = \left(\frac{T_{HS} + 273}{N_T}\right)^G$$

where

T_{HS} = Hot spot temperature in degree centigrade

N_T = Temperature constant

e = Natural logarithm base

G = Acceleration constant

A = Adjustment factor for different insulation class.

Hot spot temperature of transformers and inductors is predicted using :

$$T_{HS} = T_A + 1.1(\Delta T)$$

Where

T_{HS} is hot spot temperature in degree centigrade

T_A is ambient temperature in degree centigrade

ΔT is average temperature rise in degree centigrade.

Average temperature rise can be estimated using any of the following three equations given in MIL-HDBK-217D

(i) $\Delta T = 125 \; W_L/A$

where W_L = Power loss in watts

A = Radiating area in in^2

(ii) $\Delta T = 11.5 \; W_L/(W_T)^{0.6766}$

where

W_L = Power loss in watts

W_T = weight in lbs.

(iii) $\Delta T = 2.1 \; W_i/(W_T)^{0.6766}$

where

W_i = input power in watts

W_T = weight in lbs.

This equation is based on 80% efficiency.

Since weight of transformer is generally available, in the present work (ii) of the above methods has been used to predict hot spot temperature.

(e) Discrete semiconductor device model :

This category consists of diodes, thyristors and transistors.

The general failure rate model for these devices is.

$$\lambda_p = \lambda_b(\pi_E \cdot \pi_A \cdot \pi_Q \cdot \pi_R \cdot \pi_{S2} \cdot \pi_C)$$

failures/10^6 hrs

Various π factors used in the this model are defined in table 3.3

The equation for the base failure rate λ_b, is

$$\lambda_b = Ae^X$$

where

$$X = \left(\frac{N_T}{273+T+(\Delta T)S}\right) + \left(\frac{273+T+(\Delta T)S}{T_M}\right)^P$$

A is a failure rate scaling factor

e is the natural logarithm base

N_T, T_M & P are shaping parameters

T is the operating temperature in degree centigrade

ΔT is the difference between typical maximum allowable temperature with no junction current or power (total derating) and the typical maximum allowable temperature with full rated junction current or power.

S is the ratio of operating electrical stress to rated electrical stress.

TABLE 3.2 : PARTS WITH MULTI-LEVEL QUALITY SPECIFICATIONS

PART	QUALITY DESIGNATORS
Discrete semiconductors	JANXV, JANTX, JAN
Capacitors, Established Reliability(ER)	L,M,P,R,S
Resistors, Established Reliability (ER)	M,P,R,S
Inductors	M,P,R,S

TABLE - 3.3 : π FACTORS FOR PART FAILURE RATE MODELS

π FACTOR	DESCRIPTION
Common Factors - used in all parts categories :	
π_E	Environment : Accounts for effects of environmental factors other than temperature
π_Q	Quality : Accounts for effects of different quality levels
Discrete semiconductors :	
π_A	Application : Accounts for effect of application in terms of circuit function.
π_R	Rating : Accounts for effect of maximum power or current rating
π_C	Complexity : Accounts for effect of multiple devices in a single package

Table 3.3 (contd.)

π FACTOR	DESCRIPTION
π_{S2}	Voltage stress : Accounts for a second electrical stress (application voltage) in addition to wattage included within λb
Resistors :	
π_R	Resistance : Adjusts model for the effect of resistor ohmic value
π_C	Construction class : Accounts for influence of construction class of variable resistors
π_V	Voltage : Adjusts the model for effect of applied voltage in variable resistors in addition to wattage included within λ b
π_{TAPS}	Tap connections on potentiometers : Accounts for effect of multiple taps on resistance element
Capacitors :	
π_{SR}	Series Resistance : Adjusts model for the effect of series resistance in circuit application of some electrolytic capacitors.
π_{CV}	Capacitance value : Adjusts model for effect of capacitance
π_C	Construction : Accounts for effect of hermetic and non-hermetic seals.
π_{CF}	Configuration : Accounts for effects of fixed and variable construction

Table 3.3 (contd.)

π FACTOR	DESCRIPTION
Transformers and Inductors	
π_Q	Family : Adjusts model for influence of family type
π_C	Construction : Accounts for effects of fixed and variable constructions.

3.3.4 STRESS CALCULATION :

The stress ratio for various devices is calculated as follows :

(i) Transistors

(a) Single device in case

For silicon, $S = \frac{P_{OP}}{P_{MAX}}$ (C.F.)

For Germanium, $S = \frac{P_{OP}}{P_{MAX}}$

where

P_{OP} = actual power dissipated

P_{MAX} = maximum rated power at T_S (Temperature at which derating begins)

C.F. = Stress correction factor

(ii) Dual device in single case (equally rated)

$$S = \left[\frac{P_1}{P_S} + P_2\left(\frac{2P_S - P_T}{P_T \cdot P_S}\right)\right] \text{ (C.F.)}$$

where :

S = Stress ratio of side being evaluated

P_1 = Power dissipation in side being evaluated

P_2 = Power dissipation in other side of device

P_S = Maximum rating at T_S on one side of the dual device with the other side not operating (one side rating)

P_T = maximum rating at T_S with both sides operating (both side rating)

(ii) General purpose Diodes and Thyristors :

For Silicon, $S = \frac{I_{OP}}{I_{MAX}}$ (C.F.)

For Germanium, $S = \frac{I_{OP}}{I_{MAX}}$

where,

I_{OP} = operating average forward current

I_{MAX} = maximum rated average forward current at T_S

C.F. = Stress correction factor

(iii) Zener Diodes

Zener diodes are rated for maximum current or power or both. Either rating may be used as follows :

$S = \frac{P_{OP}}{P_{MAX}}$(C.F.) or $S = \frac{I_{Z(OP)}}{I_{Z(MAX)}}$ (C.F.)

Where

P_{OP} = actual power dissipated

P_{MAX} = maximum rated power at T_S

$I_{Z(OP)}$ = actual operating zener current.

$I_{Z(MAX)}$ = maximum rated zener current at T_S

C.F. = stress correction factor.

Stress correction factor (C.F.) and temperature correction for Silicon devices are given as follows :

(a) Device with $T_S = 25$ degree C and $T_{MAX} = 175$ degree C to 200 degree C.

$$CF = 1$$

where T_S = Maximum ambient or case temperature at which 100% of the rated load can be dissipated without causing the specified maximum junction temperature to be exceeded.

T_{MAX} = Maximum possible junction temperature.

(b) Devices with $T_S > 25$ degree C & $T_{MAX} = 175$ degree C to 200 degree C

$$C.F. = \frac{175 - T_S}{150}$$

(c) Devices with $T_S = 25$ degree C & $T_{MAX} < 175$ degree C

$$C.F. = \frac{T_{MAX} - 25}{150}$$

and λb tables should be entered using

$$T = T_A + (175 - T_{MAX})$$

(d) Devices with $T_S > 25$ degree C and $T_{MAX} < 175$ degree C

$$C.F. = \frac{T_{MAX} - T_S}{150}$$

and λ_b tables should be entered using $T = T_A + (175 - T_{MAX})$

EXAMPLES :

EXAMPLE 3.1 : The series, inverter circuit shown in Fig.2.21(page No.52) is considered for reliability **evaluation**. The results obtained by the two methods are as follows:

(i) Parts count Method : The general expression for circuit failure rate using parts count method is given by equation(3.1). The generic failure rates(λ_G) for various components are obtained using tables 5.2-10, 5.2-12, 5.2-13 and 5.2-15 given in MIL-HDBK-217D. π_Q values are obtained using tables 5.2-11, 5.2-14 and 5.2-16 given in MIL-HDBK-217D.

The specifications of the components of the circuit are listed in table 3.4. Following are the calculation for G_B environment.

1. For Resistor R(Fixed, Wirewound)

λ_G = 0.0085 failures/10^6 hours

π_Q = 3.0

N = 1

2. For capacitor C (paper)

$\lambda_G = 0.0021$ failures/10^6 hours

$\pi_Q = 3.0$

$N = 1$

3. For Inductors L_1 and L_2 (fixed)

$\lambda_G = 0.0016$ failures/10^6 hours

$\pi_Q = 10.0$

$N = 2$

$$\lambda_{circuit} = 1 \times 0.0085 \times 3 + 0.0021 \times 3$$

$$+ 2 \times 0.0016 \times 3 + 2 \times 0.0022 \times 10$$

$$= 0.4814 \text{ failures}/10^6 \text{ hrs}$$

(ii) Part stress Analysis : For Part stress analysis, the loadings of the components obtained in example 2.1 (Page No. 51) are used. The specifications of the components are listed in table 3.4. Table 3.5 shows the failure rates of various components obtained by assuming ambient temperature to be 30°C.

Since failure of any of the component results in failure of the circuit, circuit failure rate is obtained by adding failure rates of all the components.

TABLE 3.4 : SPECIFICATION OF COMPONENTS FOR EXAMPLE 3.1

COMPONENT	COMPONENT TYPE	VALUE	RATING	QUALITY LEVEL	MIL.-SPEC.	COMP-LEXITY	WEIGHT	T_S	T_{MAX}
CAPACITOR, C	Paper capacitor	1.25µF	20V	LOWER	MIL-C-14157	-	-	-	85^oC
RESISTOR, R	Wirewound, Accurate	1.0ohm	1 W	LOWER	MIL-R-39005	-	-	-	-
INDUCTOR L1	Fixed	0.05mH	-	LOWER	MIL-C-15305	-	0.3 lb.	-	105^oC
INDUCTOR L2	Fixed	0.05mH	-	LOWER	MIL-C-15305	-	0.3 lb.	-	105^oC
THYRISTOR TH1	-	-	1.0A	PLAS-TIC	MIL-STD-19500	-	-	30^oC	180^oC
THYRISTOR TH2	-	-	1.0A	PLAS-TIC	MIL-STD-19500	-	-	30^oC	180^oC

TABLE 3.5 FAILURE RATE OF CIRCUIT OF EXAMPLE 3.1 OBTAINED BY PART STRESS ANALYSIS
(Ambient Temperature = 30°C)

COMPONENT	LOAD RATIO S	ENVIRON-MENT	BASE FAILURE RATE λ_b (failures/10^6 hours)	π_E	π_Q	π_C	π_R	C.F.	π_{CV}	PART FAILURE RATE λ_p (failures/10^6 hours)
CAPACITOR C	0.79	G_B	0.01900	1.0	30.00	-	-	-	1.63	0.93389
RESISTOR, R	0.84	G_B	0.00900	1.0	15.00	-	1.0	-	-	0.13500
INDUCTOR, L1	-	G_B	0.00040	1.0	20.00	2.0	-	-	-	0.01600
INDUCTOR L2	-	G_B	0.00040	1.0	20.00	2.0	-	-	-	0.01600
THYRISTOR, TH1	0.35	G_B	0.00330	1.0	50.00	-	1.0	1.0	-	0.16500
THYRISTOR, TH2	0.39	G_B	0.00330	1.0	50.00	-	1.0	1.0	-	0.16500
									circuit failure rate	1.43087

EXAMPLE 3.2 : The ECL Schmitt trigger circuit shown in Fig. 2.25(page No. 57) is considered for reliability evaluation. The results obtained by the two methods are as follows :

(i). Parts count Method : Specifications of the various components of the circuit are listed in table 3.6. The generic failure rates (λ_G) for various components are obtained using tables 5.2 - 10 and 5.2 - 12 given in MIL-HDBK-217D. π_Q values are obtained using tables 5.2 - 11 and 5.2 - 14 given in MIL-HDBK-217D. Following are the calculations for G_B environment.

1. For Resistor R_1 (fixed, Wirewound)

λ_G = 0.0085 failures/10^6 hours

π_Q = 1.0

N = 1

2. For Resistor R_2 (fixed, Film)

λ_G = 0.0014 failures/10^6 hours

π_Q = 1.0

N = 1

3. For Resistor R_3 (fixed, Wirewound)

λ_G = 0.0085 failures/10^6 hours

π_Q = 3.0

N = 1

4. For Resistor R_4 (composition)

λ_G = 0.0051 failures/10^6 hours

π_Q = 0.3

N = 1

5. For Resistor R_5 (fixed, Film)

λ_G = 0.0012 failures/10^6 hours

π_Q = 0.3

N = 1

6. For Transistors T_1 & T_2 (Si, NPN)

λ_G = 0.0025 failures/10^6 hours

π_Q = 1.0

N = 2

$$\lambda_{Circuit} = 1 \times 1.0 \times 0.0085 + 1 \times 1.0 \times 0.0014 + 1 \times 3.0 \times 0.0085 + 1 \times 0.3 \times 0.0051 + 2 \times 1.0 \times 0.0025$$

$$= 0.04193 \text{ failures}/10^6 \text{ hours}$$

(ii) Part Stress Analysis : For part stress analysis the loadings of the components obtained in example 2.2 (page no.56) are used. The specifications of the components are listed in table 3.6. Table 3.7 shows the failure rate of various components at 30°C (ambient temperature). Circuit failure rate is obtained by adding failure rates of all the components.

TABLE 3.6 SPECIFICATION OF COMPONENTS FOR EXAMPLE 3.2

COMPONENT	COMPONENT TYPE	VALUE (K-OHM)	RATING	QUALITY LEVEL	MIL.-SPEC.	COMPLEXITY	T_S	T_{MAX}
RESISTOR R_1	Fixed, Wirewound	0.66	0.2W	M	MIL-R-39005	-	-	-
RESISTOR R_2	Fixed, Film	16.34	0.1 W	M	MIL-R-55182	-	-	-
RESISTOR R_3	Fixed, Wirewound	2.37	0.1 W	LOWER	MIL-R-39005	-	-	-
RESISTOR R_4	Composition	7.28	0.1 W	P	MIL-R-39008	-	-	-
RESISTOR, R_5	Fixed, Film	1.0	0.1 W	P	MIL-R-39017	-	-	-
TRANSISTOR, T_1	Si, NPN	-	0.15 W, 5 V	JAN	MIL-S-19500	Single	25°C	175°C
TRANSISTOR T_2	Si, NPN	-	0.15 W, 5 V	JAN	MIL-S-19500	Single	25°C	175°C

TABLE 3.7 FAILURE RATE OF CIRCUIT OF EXAMPLE 3.2 OBTAINED BY PART STRESS ANALYSIS (Amb. Temp. = 30°C)

COMPONENT	LOAD RATIO S	VOLTAGE RATIO S2	ENVI-RON-MENT	APPLI-CATION	BASE FAILURE RATE b (Failures/ 10^6hrs)	π_E	π_Q	π_A	π_R	π_{S2}	CF	PART FAILURE RATE p (Failures/ 10^6hrs
RESISTOR, R_1	0.30	-	G_B	-	0.00400	1.0	1.0	-	1.0	-	-	0.00400
RESISTOR, R_2	0.32	-	G_B	-	0.00110	1.0	1.0	-	1.0	-	-	0.00110
RESISTOR, R_3	0.11	-	G_B	-	0.00370	1.0	15.0	-	1.0	-	-	0.05550
RESISTOR, R_4	0.05	-	G_B	-	0.00022	1.0	0.3	-	1.0	-	-	0.00006
RESISTOR, R_5	0.86	-	G_B	-	0.00180	1.0	0.3	-	1.0	-	-	0.00054
TRANSISTOR, T_1	0.40	0.53	G_B	Linear	0.00120	1.0	1.2	1.5	1.0	0.7	1	0.00151
TRANSISTOR, T_2	0.08	0.50	G_B	Linear	0.00070	1.0	1.2	1.5	1.0	0.64	1	0.00080
											Circuit failure rate	0.06351

CHAPTER-4

PROGRAM DESCRIPTION

4.1 CIRCUIT ANALYSIS PROGRAM : CKTAN

For the circuit analysis CKTAN, a package written in FORTRAN IV is used. This package, which originally was capable of simulating resistors, capacitors, diodes, inductors and transistors , is modified so that now it can also simulate SCR'S, diacs and triacs. The input data to this program includes the topology of the circuit, device parameters, initial estimate of voltages at various nodes, time limit for transient analysis and initial time step for transient analysis. This time step may be modified by the program itself to limit truncation error. If any of the thyristor is in transition state (i.e. during turn-on time or turn-off time). The time step is automatically set by program to 10^{-2} µs. This is necessary to simulate successfully the transition periods which are of the order of few microseconds.

For the solution of linear equations, 1971 version of ZOLLENKOF'S algorithm is used. This method is very efficient for sparse matrices that have non-zero digonal terms and are either strictly symmetrical or asymmetrical in element value but with symmetrical sparcity structure.

Fig. 4.1 to Fig. 4.4 shows the structure of the program. CKTAN.

In the following section various subroutines used in CKTAN are described.

Subroutine INAN : This subroutine reads the data required for circuit analysis.

Subroutine PRDATA : This subroutine prepares data required for the D.C. and transient analysis by arranging unknown node voltages in the last.

Subroutine PRPDAT : Prepares the arrays which dipict the structure of the node admittance matrix.

Subroutine DCAN1 : This is the main subroutine which performs D.C. analysis of electronic circuits.

Subroutine TRAN1 : This is main subroutine for the transient analysis of electronic circuits.

Subroutine BAKDAT : This subroutine converts the data prepared by PRDATA in the original form after transient analysis is complete.

Subroutine TOPRE : This subroutine updates the topology of the network by including the branches corresponding to resistors.

Subroutine TOPIN : This subroutine updates the topology of the network by including the branches corresponding to inductors.

Subroutine TOPCA : This subroutine updates the topology of the network by including the branches corresponding to capacitors.

Subroutine TOPDI : This subroutine updates the topology of the network by including the branches corresponding to diodes.

Subroutine TOPTR : This subroutine updates the topology of the network by including the branches corresponding to transistors.

Subroutine TOPTH : This subroutine updates the topology of the network by including the branches corresponding to SCR's and triacs.

Subroutine TOPDIC : This subroutine updates the topology of the network by including the branches corresponding to diacs.

Subroutine VJNDIN : This subroutine calculates junction voltages of diodes and set them appropriately.

Subroutine YMATDN : This subroutine modifies elements of admittance matrix and current vector to include diodes in the circuit equations for the D.C. analysis.

Subroutine VJNTRN : This subroutine determines junction voltages of transistors and set them appropriately.

Subroutine YMATTN : This subroutine includes transistor in the linearized circuit equations for d.c. analysis.

Subroutine YAMATRN : This subroutine include resistances in linearized circuit equations for d.c. analysis.

Subroutine YMATCN : This subroutine includes the capacitors in the linearized circuit equations for d.c. analysis.

Subroutine YMATIN : This subroutine includes the inductors in the linearized circuit equations for d.c. analysis.

Subroutine YMATTH : This subroutine includes the SCRS and triacs in the linearized circuit equations for d.c. analysis.

Subroutine OUTDC : This subroutine types out all the results of D.C. analysis.

Subroutine YMADI : This subroutine includes diacs in the linearized circuit equations for d.c. analysis.

Subroutine RETRA : This subroutine determines the contribution of each resistor to node-admittance matrix and current vector for transient analysis.

Subroutine INDTRY : This subroutine determines the contribution of each inductor to node-admittance matrix and current vector for transient analysis.

Subroutine CAPTRY : This subroutine determines the contribution of each capacitor to node-admittance matrix and current vector for transient analysis.

Subroutine DDY : This subroutine determines the contribution of each diode to node-admittance matrix and current vector for transient analysis.

Subroutine DMOD : This subroutine is called in subroutine DDY for transient analysis.

Subroutine TNY : This subroutine determines the contribution of each transistor to node-admittance matrix and current vector for transient analysis.

Subroutine TMOD : This subroutine is called in TNY for the transient analysis.

Subroutine THY : This subroutine determines the contribution of each SCR and triac to node-admittance matrix and current vector for transient analysis.

Subroutine DIC : This subroutine calculates the contribution of each diac to node-admittance matrix and current vector for transient analysis.

Subroutine IPUT : This is a user defined subroutine for giving input signals at various nodes of circuit in transient analysis.

Subroutine TJNDIN : This subroutine applies logarithmic correction to junction voltage of diodes in transient analysis.

Subroutine TJNTRN : This subroutine applies logarithmic correction to junction voltages of transistors in transient analysis.

Subroutine TJNTH : This subroutine modifies the SCR and triac voltages after applying corrections in its terminal voltages.

Subroutine TJNDI : This subroutine modifies diac voltages after applying corrections in its terminal voltages.

Subroutine LOAD : This subroutine calculates the loadig of each component and is called in subroutine TRAN1.

Subroutine SOLSP : This subroutine calls all subroutines used for the solution of linear equations using bi-factorization technique.

Subroutine CALNXT : This subroutine prepares various arrays required for solution of equations.

Subroutine CAREAR : Preapers the array which stores the off-digonal term of node-admittance matrix row-wise.

Subroutine ORDER : This subroutine orders and performs gaussian elimination.

Subroutine REDUCT : This subroutine performs reduction of a nonsymmetrical matrix.

Subroutine SOLV : This subroutine solve the linear equations by a sequence of matrix multiplication.

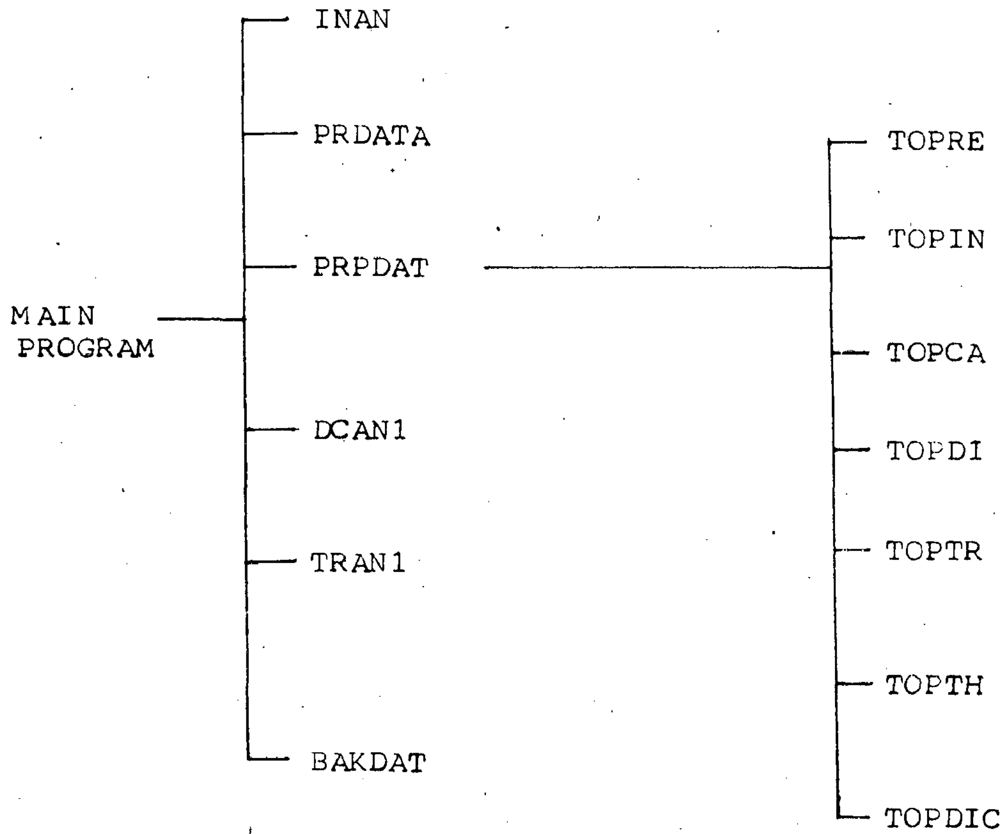


Fig.: 4.1 Structure of the subroutines for CKTAN

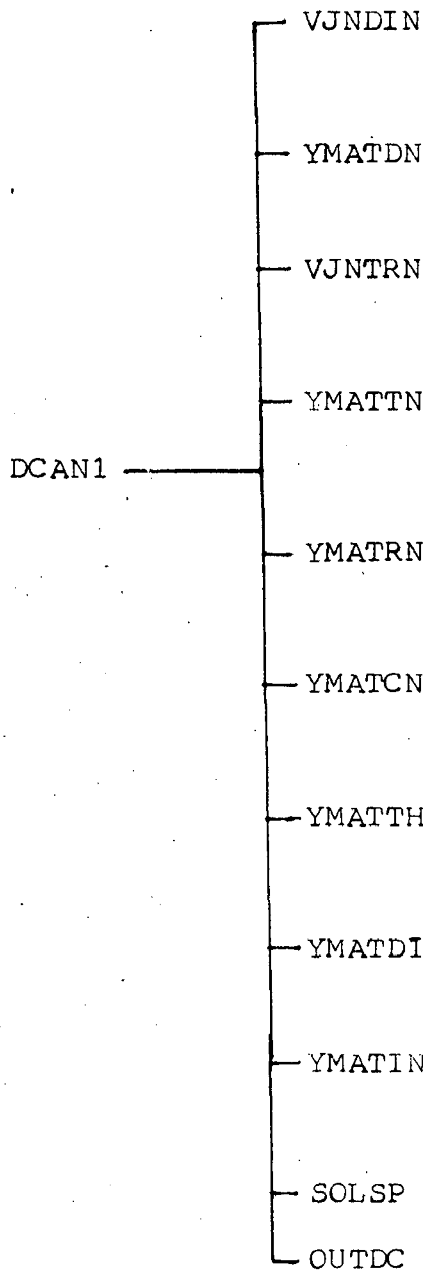


Fig 4.2 : Structure of subroutines for the subroutine DCAN1

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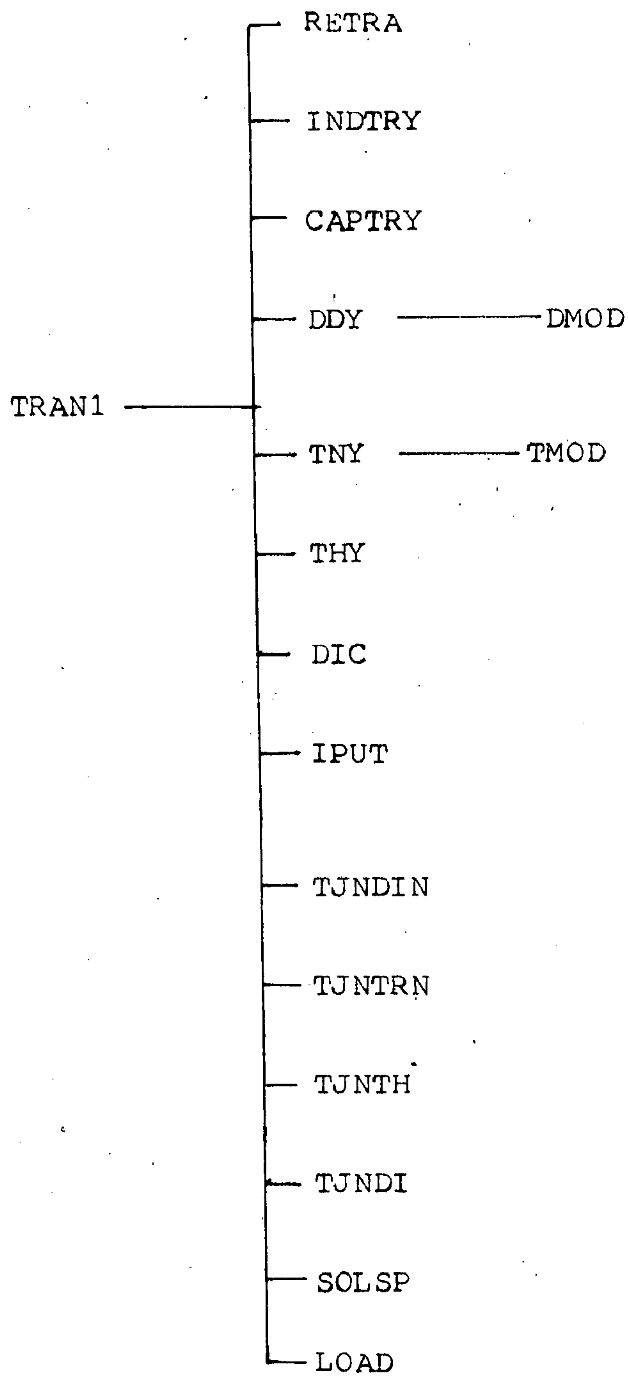

Fig.4.3 : Structure of the subroutines for subroutine TRAN1

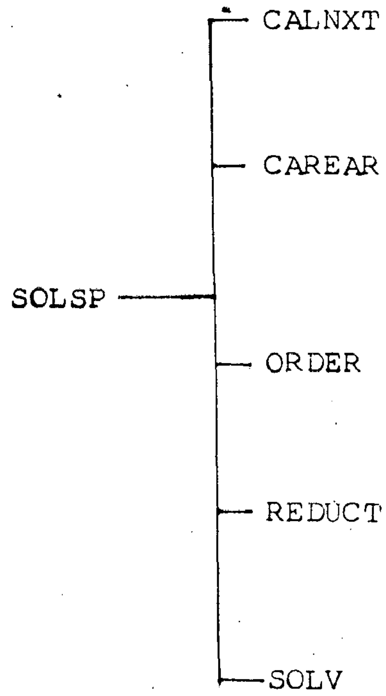

Fig.4.4 : Structure of subroutines for subroutine SOLSP

4.2 RELIABILITY EVALUATION PROGRAM : RELCKT

For the reliability evaluation of electronic circuits dBASE PLUS package RELCKT has been updated and used. This program takes data from a database file CKT.DBF. Results are stored in a database flie OUT.DBF.

Table 4.1 shows the description of input to various fields of CKT.DBF.

Fig. 4.5 shows the organization of the computer program for reliability evaluation of electronic circuits. The brief description of various subprograms is given below.

RELCKT : This is the main program for reliability evaluation of electronic circuits.

CAPREL : This sub-program calls various subprograms to calculate failure rates of capacitors depending on the type of capacitor.

RESREL : This sub-program calls various subprograms to calculate failure rates of resistors depending on the tape of resistor.

INDREL : This subprogram calculates the failure rates of inductors.

TRANREL : This sub-program calculates the failure rates of transformers.

THYREL : This sub-program calculates the failure rates of thyristors.

DIODREL : This sub-program calls other sub-programs depending on type of diode to calculate failure rate of diodes.

TRNREL : This sub-program calls other subprograms depending on type of transistor, to calculate failure rates of transistors.

CREL1 : This sub-program is called by CAPREL to calculate failure rate of paper and plastic film capacitor. It uses database CAP1 if $T_{MAX} \leq 65^{\circ}C$, CAP2 if $65^{\circ}C < T_{MAX} \leq 85^{\circ}C$ and CAP3 if $T_{MAX} > 85^{\circ}C$ for finding base failure rate λb. Record number 18 in database file MODE corresponds to π_E values for different type of environment.

CREL2 : This sub-program is called by CAPREL to calculate failure rate of mica capacitor. Database files CAP4 and CAP5 are used to read base failure rates depending on whether T_{MAX} is less than or more than $125^{\circ}C$. Record Number 18 in MODE corresponds to TT_E values for different environments.

CREL3 : This sub-program is called by CAPREL for failure rate calculation of Glass capacitor. Database file CAP6 or CAP7 is used to read base failure rate depending on whether temperature is less than or more than $125^{\circ}C$. For π_E values, record number 20 of MODE is used.

CREL4 : This sub-program is called by CAPREL for failure rate calculation of ceramic capacitors. For $T_{MAX} \leqslant 85^{o}$, CAP8 and for $T_{MAX} > 85^{o}C$, CAP9 is used for λ_b calculation. Record number 21 in MODE is used to define π_E values for different environments.

CREL5 : This sub-program is called by CAPREL for failure rate calculation of Tantalum electrolytic capacitor. CAP10 is used for λ_b calculation. π_E values are stored in record number 22 in MODE.

CREL6 : This sub-program is called by CAPREL for failure rate calculation of Aluminium electrolytic capacitor. File CAP11 is used for λ_b calculation. π_E values are stored in record number 23 in file MODE.

CREL7 : This sub-program is called by CAPREL for failure rate calculation of ceramic capacitors. If $T_{MAX} \leqslant 85^{o}$, file CAP12 else file CAP13 is used for λ_b calculation. π_E values are stored in record number 24 in file MODE.

CREL8 : This sub-program is called by CAPREL for failure rate calculation of Piston- type capacitor. If $T_{MAX} \leqslant 125^{o}$, file CAP14 else file CAP15 is used to find λ_b . Record number 25 in file MODE is used to define π_E values for different environments.

CREL9 : This sub-program is called by CAPREL for failure rate calculation of Air Trimmer capacitor. File CAP16 is used to find λ_b. Record number 26 in file MODE gives π_E value.

CREL10 : This subprogram is called by CAPREL for failure rate calculation of vacuum or Gas capacitor. If $T_{MAX} \leq 85^{o}C$, file CAP17 else CAP18 is used to find λ_b. Record number 27 in file MODE defines π_E values for different environments.

RREL1 : This sub-program is called by RESREL for failure rate calculation of composition resistor. Database file TRES1 is used to find λ_b. Record number 1 in file MODE defines the π_E value for various environments.

RREL2 : This sub-program is called by RESREL for failure rate calculation of Film resistor. If the MIL-specification is either MIL-R-39017 or MIL-R-22684, file TRES2 is used to find λ_b. Otherwise file TRES3 is used for this purpose. π_E values for various environments are defined in record number 2 of file MODE.

RREL3 : This subprogram is called by RESREL for failure rate calculation of Power Film resistor. File TRES4 is used to find λ_b. Record number 3 in file MODE defines values of π_E for various environments.

RREL4 : This sub-program is called by RESREL for failure rate calculation of Resistor network (film type). File TREST is used to find the temperature factor π_T. Record no.4 in MODE file gives π_E values for different environments.

RREL5 : This sub-program is called by RESREL for failure rate calculation of wirewound, accurate resistor. File TRES5 is used to find λ_b. Record no.5 in MODE gives π_E values for various environments.

RREL6: This sub-program is called by RESREL for failure rate calculation of variable, wirewound resistor. File TRES8 is used to find λ_b. Record no.6 in file MODE define the value of π_E for different environments. File TRPTF is used to find π_{TAPS}.

RREL7 : This subprogram is called by RESREL for failure rate calculation of variable, Precision resistor. File TRES9 is used to find λ_b. Record no.7 in MODE gives the π_E values for different environments. File TRPTF is used to find π_{TAPS}.

RREL 8 : This subprogram is called by RESREL for failure rate calculation of wirewound, semiprecision resistor. File TRES10 is used to find λ_b. Record no.8 in file MODE defines π_E value. TRPTF is used to find π_{TAPS}.

RREL9 : This sub-program is called by RESREL for failure rate calculation of wirewound Power resistor. File TRES11 is used to find λ_b. Record no.9 in file MODE gives π_E value. TRPTF is used to find π_{TAPS}.

RREL10 : This sub-program is called by RESREL for failure rate calculation of variable nonwire-wound resistor. File TRES12 is used to find λ_b. Record no.10 in MODE gives π_E value. TRPTF is used to find π_{TAPS}.

RREL11 : This sub-program is called by RESREL for failure rate calculation of variable composition resistor. File TRES13 is used to find λ_b. Record no.11 in MODE gives π_E value. File TRPTF is used to find π_{TAPS}.

DREL1 : This sub-program is called by DIODREL and calculates the failure rate of general purpose (Silicon or Germanium) diodes. For silicon diodes file DIOD1 and for Germanium diodes file DIOD2 is used to find λ_b. Record no.16 in file MODE gives π_E value.

DREL2 : This sub-program is called by DIODREL for calculation of failure rates of Avalanche and Zener diodes. File DIOD3 is used to find λ_b. Record no.17 in file MODE gives π_E value.

TREL1 : This sub-program is called by TRNREL for calculation of failure rates of conventional transistors. For Si,NPN transistor file TRAN1, for Si, PNP transistor file TRAN2, for Ge, NPN transistor file TRAN3 and for Ge,PNP transistor file TRAN4 is used to find λ_b. Record no. 13 in file MODE gives π_E value.

TREL2 : This sub-program is called by TRNREL for failure rate calculation of Field effect transistors. File TRAN5 is used to find λ_b. Record no. 14 in file MODE gives π_E value.

TREL3 : This subprogram is called by TRNREL for failure rate calculation of unijunction transistor. File TRAN6 is used to find λ_b. Record no. 15 in file MODE gives π_E value.

The values of π factors and failure rates for all the components of the circuit are stored in a database file named OUTPUT.

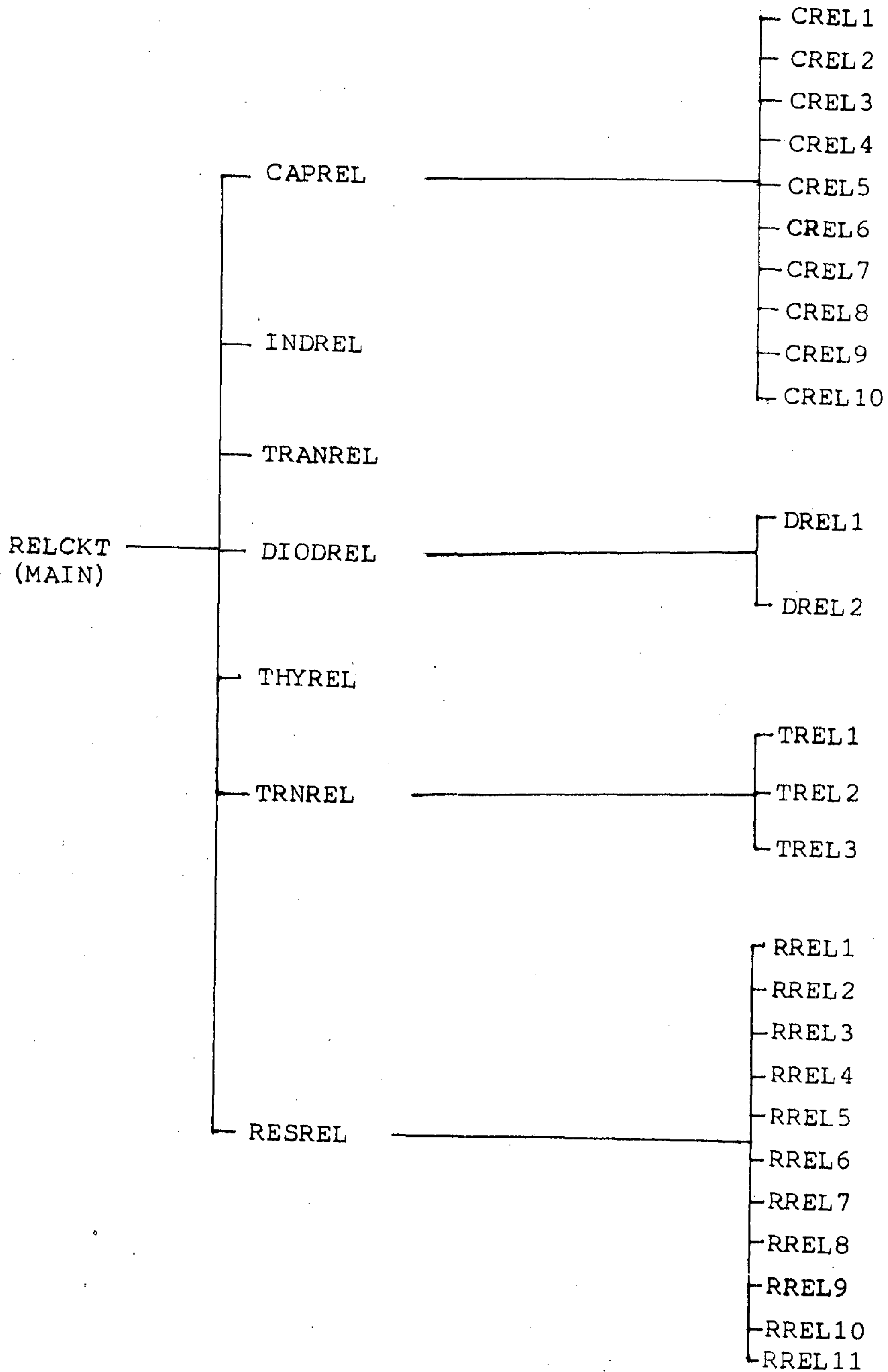

Fig.4.5 : Organigation of Subprograms for Reliability evaluation of Power Electronic Circuits.

TABLE 4.1 : Input information to be stored in CKT.DBF for reliability evaluation of circuits.

Field Name	Type	Description
COMPONENT	Character	Name of component in capital, use TRANFORMER for transformer.
TYPE	Numeric	Used with resistors, capacitors, diodes and transistor. Various types of component with the input to be used are as follows : Resistors : 1. Composition resistor 2. Film resistor 3. Power Film resistor 4. Resistor Network (Film type) 5. Wirewound, Accurate resistor 6. Variable Wirewound resistor 7. Variable Wirewound, Precision resistor 8. Variable wirewound, semiprecision resistor. 9. Variable wirewound, Power resistor. 10. Variable Nonwirewound, Power resistor. 11. Variable composition resistor. Capacitors : 1. Paper & Plastic Film Capacitor 2. Mica capacitor 3. Glass capacitor 4. Ceramic capacitor 5. Tantalum Electrolytic capacitor 6. Aluminium Electrolytic capacitor 7. Variable ceramic capacitor 8. Variable Piston Type capacitor 9. Variable Air Trimmer capacitor 10. Vacuum or Gas Capacitor

Field Name	Type	Description
		Diodes : 1. General purpose diode 2. Avalanche & Zener diode Transistors : 1. Conventional transistor 2. Field effect transistor 3. Unijunction transistor
CLASS	CHARACTER	Construction class or MIL specification for various components. The components with which this field is used and the inputs are described below : Film resistor : Give MIL-specification (i) MILR-39017 for MIL-R-39017 (ii) MILR-22684 for MIL-R-22684 (iii) MILR-55182 for MIL-R-55182 (iv) MILR-10509 for MIL-R-10509 Variable Film and precision resistor: Give MIL-specification (i) MILR-23285 for MIL-R-23285 (ii) MILR-39023 for MIL-R-39023 Paper and plastic Film capacitor : Give MIL-specification (i) MILC-14157 for MIL-C-14157 (ii) MILC-19978 for MIL-C-19978 Vacuum or Gas capacitor: Give type of construction : (i) FIXED (II) VARIABLE

Field Name	Type	Description
		General purpose diode : Give contact construction : (i) Si MBOND for silicon Matallurgically Bonded (ii) Si NMBOND for Silicon Non-metallurgically Bonded (iii) Ge MBOND for Germanium Matallurgically Bonded. (iv) Ge NMBOND for Germanium Non-matallurgically Bonded. Conventional transistor : Give material and type : (i) Si PNP for Silicon, PNP (ii) Si NPN for Silicon, NPN (iii) Ge PNP for Germanium, PNP (iv) Ge NPN for Germanium, NPN Transformer : Give family type (i) PULSE for Pulse transformer (ii) AUDIO for Audio transformer (iii) POWER for Power transformer (iv) RF for RF transformer Inductor : Give construction (i) FIXED (ii) VARIABLE
LOSSES	Numeric	Power loss in watts, used for inductors and transformers.
LOADING	Numeric	Ratio of operating load to rated load, used with all components except inductors and transformers.
VRATIO	Numeric	Ratio of operating voltage to rated voltage, used with variable resistors, and conventional transistors.

Field Name	Type	Description
TEMP	Numeric	Ambient temperature in ^{o}C, used with all components.
RATING	Numeric	Rated load of component, used with resistors, diodes, thyristors and transformers.
QUALITY	Character	Quality level or failure rate level, used with all components.
ENVIRON-MENT	Character	Environment symbol, used with all components.
WEIGHT	Numeric	Weight of component in lbs., used with inductor and transformer.
TMAX	Numeric	Maximum rated operating temperature of divce, used with inductors, transformers and silicon semiconductor devices.
TS	Numeric	Temperature in ^{o}C at which derating begins, used with silicon semiconductor devices.
NOTAPS	Numeric	Number of tappings, used with variable resistors.
APPLI-CATION	Character	Field of application such as LINEAR,SWITCH, POWER, HF, RF, used with transistors and SWITCH, ANALOG, RECTIFIER with diode.
COMPLE-XITY	Character	Level of complexity, used for transistors, use SINGLE for single transistor, DUALMATCH for dual (matched), DUALNMATCH for dual (unmatched), DARLINGTON for darlington, DUALEMITER for dual emitter, and COMP for complementry pair.
RESCKT	Numeric	Resistance in series in ohms, used with Tantalum electrolytic capacitors.

CHAPTER-5

CONCLUSION AND SUGGESTIONS FOR FURTHER WORK

5.1 CONCLUSION :

Increase in power handing capability and complexity of electronic circuits have aggravated the problem of failures in the electronic circuits. Most of the failures in power electronic circuits are due to poor design. Thus reliability analysis must be incorporated in the circuit design process.

Data useful to design of electronic circuits; for selection, specification and use of components, are scattered. But by thorough study of the circuit, various stresses are calculated. These stresses cause the degradation and failure of components. The military handbook MIL-HDBK-217D is used for reliability analysis based on part stresses.

For determination of component loading, required in part stress analysis for reliability evolution, circuit analysis is to be carried out. Models for SCR, diac and triac have been developed and the results obtained by circuit analysis are shown in Chapter 2. These models in addition to on-state and off-state of thyristors, simulate turn-on and turn-off periods also, giving the picture of electrical transients experienced by the devices. The on-state model is based on the exponential characteristic of thyristors

instead of conventionally used linear approximation. To avoid the convergence problem due to non-linear (exponential) characteristics, corrections obtained by Newton's method are modified taking advantage of shape of characteristic.

MIL-HDBK-217D methods of reliability prediction are used and results are shown in chapter 3. Failure rate of each component is obtained by applying parts count method and part stress analysis using computer program. The results obtained by the two methods differ considerably. This difference is due to difference in amount of information needed to apply them. Since part stress values are not available during early design phase, Parts count method is suitable for this phase. During later design phase, Part stress analysis is used.

There are few limitations of the two methods of reliability prediction. Neither method applies to a nuclear environment nor they consider effect of ionizing radiation. Also the secondary failures due to current and voltage transients, and high rate of change of current and voltage are not taken into account by these methods. This is a major limitation as far as power electronic circuits are concerned, where these transients are quite common due to turn-on and turn-off of devices. To overcome this limitation, peak values of currents and voltages, and their rate of change is determined from circuit analysis and are kept below specified value.

5.2 SCOPE FOR FURTHER WORK :

As already mentioned failure rate data due to secondary failures is not available. There is need for extensive research work for quantative analysis of effect of stresses due to electrical transients on failure rates.

The reliability analysis predicts the areas of high failure rates. To improve the performance of system these high failure rates should be brought down by using suitable reliability improvement methods incorporating cost considerations, such as proper component derating, simplification of circuits and redundancy (standby/active) etc. This requires the development of suitable optimization methods and computer packages.

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