DEVELOPMENT OF MICROPROCESSOR CONTROLLED LOAD COMMUTATED INVERTER FED SINGLE-PHASE INDUCTION MOTOR DRIVE

A DISSERTATION

submitted in partial fulfilment of the
requirements for the award of the degree
of
MASTER OF ENGINEERING
in
ELECTRICAL ENGINEERING
(Power Apparatus & Electric Drives)

By
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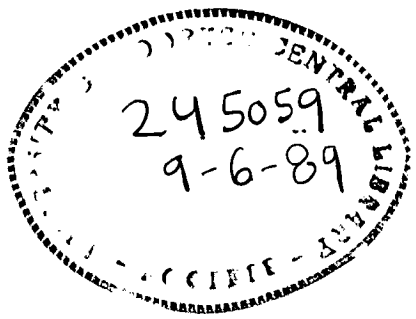

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DEDICATED

TO

MY

WIFE

VANDANA

CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the dissertation entitled ,"DEVELOPMENT OF MICROPROCESSOR CONTROLLED LOAD COMMUTATED INVERTER FED SINGLE-PHASE INDUCTION MOTOR DRIVE ", in partial fulfilment of the requirements for the degree of MASTER OF ENGINEERING in ELECTRICAL ENGINEERING with specialization in POWER APPARATUS AND ELECTRIC DRIVES submitted in the Department of Electrical Engineering, University of Roorkee, Roorkee, is an authentic record of my own work carried out for a period of about seven months, from August 1988 to Febraury 1989 under the supervision of Dr. Bhim Singh, Reader in Electrical Engineering Department, Univerisity of Roorkee, Roorkee.

The matter embodied in this dissertation has not been submitted elsewhere for the award of of any other degree or diploma .

(PAPPU RAM)

This is to certify that the above statement made by the candidate is correct to the best of my knowledge .

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ABSTRACT

The dissertation deals with the design, performance analysis and experimental studies of a microprocessor controlled load commutated inverter fed single-phase induction motor drive. In this scheme single-phase ac supply is converted into variable dc supply using a fully controlled rectifier and fed to load commutated inverter . Commutation of inverter thyristors is achieved using terminal capacitor which is charged by back emf of motor. Speed of drive is controlled by varying capacitor value in open loop control and by varying current through thyristor controlled inductor in closed loop control .

The whole work of dissertation has been catagorised as introduction,description of the system,system software implementation,performance analysis of the drive,performance of close loop system and conclusions and suggestions for further work . In chapter 1, introduction and literature survey is given. In chapter 2,system hardware is described . Chapter 3 deals with system software implementation . Chapter 4 deals with performance analysis of the drive in open loop control . In chapter 5 , experimental performance of the drive in closed loop control is discussed . In chapter 6 , main conlusions and suggestions for further work are given .

CONTENTS

CHAPTER 1

INTRODUCTION

1.1 GENERAL

DC motors are being used in most of the variable speed applications, irrespective of higher cost of these as compared to ac motors of same size and ratings. The reason beihind this is that dc motor speed can be controlled over the wide range. The dc motors are fed by solid state rectifiers.[1,3]. The use of dc motors has a number of mechanical and electrical limitations caused by mechanical commutator. The modern trend in the industries is towards the replacement of dc drives by ac drives in many applications because of comparative adavantages of ac drives, particularly ,squirrel cage induction motor. Its construction is simple and robust. It has lesser cost, higher power to weight ratio and maintenence free operation as compared to dc motors. Presently , most of the variable speed ac drives use solid state con-verters [2,4,5].

Frequency control method is becoming popular day by day in ac drives, which uses the solid state frequency converters for obtaining wide range speed control. The solid state frequency converters are cycloconverters and dc link converters. In cycloconverter [2,3] the alternating voltage of fixed frequency is converted directly to a lower frequency output voltage without an intermediate dc link. The cycloconverter consists of a number of phase contrtolled rectifier circuits connected to an ac supply system which provides the voltage necessary for delayed phase commutation. The individual circuits are controlled so that a low frequency output vlotage wave form is fabricated from segments of the poly phase input voltage. The output frequency is limited to one third of the input supply frequency and , therefore, the drives employing the cycloconverter are suitable for low speed applications. The cycloconverter works by means of phase commutation and no auxiliary forced commutation circuit is required. This results in an more compact power circuit and also eliminates the circuit losses associated with forced commutation circuits in forced commutated converters. The cycloconverter is inherently capable of power transfer in either direction between source and load and can,therefore, supply ac power to load of any power factor. It is capable of operating in four quadrants. At low frequency, harmonic contents in output are minimum. Drawbacks of cycloconverter are that its output frequency range is limited to one third of input supply frequency and it requires a large number of thyristors. The expensive circuitry is not justified in small installations, but the cycloconverter is economical for units of 200 KVA or more. It has low input power factor particularly at reduced output voltage.

DC link conveters[2,4,5] are two stage conversion devices in which power from ac source is first converted into dc cupply and then inverted to get variable voltage variable frequency output. These types of inverters can operate over wide frequency range and are suitable for wide range speed control of ac motors. The votlage source inverters use either an uncontrolled rectifier and dc chopper or a controlled rectifier to get variable dc link voltage which is fed to a forced commutated inverter. Voltage source inverter are classified into two types: one is square wave inverter and the other is pulse width modulated (PWM) inverter. Square wave inverter consists of a controlled rectifier to get variable dc link voltage. Square wave inverter has a number of disadvantages. In this inverter the commutating capacitor is charged by the dc link voltage and hence the commutating capability deteriorates under low speed operation of the drive requiring low dc link voltage. Further it requires large value of dc filter components consisting dc link inductor and filter capacitor. This type of inverter generates a square wave output with high value of lower order harmonic contents which cause harmonic losses and torque pulsation in the drive. The pulse width modulated inverter generally consists of a diode rectifier to provide constant dc link voltage. The inverter controls both vlotage and frequency of the output. There are many techniques to get PWM. Sinusoidal pulse width modulation is most common. This technique reduces hamonic losses to a great extent but the inverter efficiency is reduced due to increased commutation losses as a result of high rate of commutaion. In addition, PWM inverters require sophisticated control to achieve desired performance. The PWM inverters have nearly unity power factor due to diode rectifier input.

A current source inverter [5,6] unlike a voltage source inverter works with a stiff dc current source. The current source inverter fed drive has the ability to control the motor current which results in complete torque control. Regeneration is possible in current source inverter , commutation losses are lower, efficiency is higher as compared to voltage source inverter . However, the current controlling characteristics of the drive necessiates a large filter inductor. Its frequency range is lower it and cannot operate at no load . The drive has instability problem and sluggish response at light loads and higher speeds. The current source inverter has a limited scope of applications in multi-motor drive system.

The load commutated inverter (LCI), also called by several names as self-commutated inverter (SCI), machine commutated inverter (MCI), line commutated inverter (LCI) [4,5] overcomes some of the difficulties associated with cycloconverter and forced commutated inverters. A load commutated inverter is simply a converter bridge operating in continous current mode with firing angle between 90 deg and 180 deg. The load commutated inverter requires leading reactive power for commutation. In LCI fed synchronous motor drive, synchronous motor is operated at

leading power factor, but in LCI fed induction motor drive leading reactive power requirement may only be met by terminal capacitor economically so that the overall power factor is leading. In LCI, commutating components are not required as a result of it, inverter weight, volume and cost are reduced.Harmonics in the output voltage waveform are also reduced.The triggering circuit requirements are comparatively simple.Commutation losses are reduced and consequently inverter efficiency is increased. The LCI has some disadvantages too.LCI fed drive is not self-starting. Hence extra starting arrangements are required to start the drive. It also requires a large dc link inductor.

In the present work,a load commutated inverter is proposed to obtain the variable frequency operation of a single-phase induction motor above the base speed.Single-phase induction motor is mostly used in numerous low power applications.It is rugged and simple in construction, cheap in cost and robust in nature and having maintainance free operation.At present,universal motor is used for high speed low power applications in the speed range of 1500 RPM to 15000 RPM. At higher speeds, the universal motor suffers from commutation problem.Commutator and brushes require regular maintainance.The power to weight ratio of universal motor is low as compared to induction motor of same size and rating. Above the base speed, the operation of the single-phase induction motor fed from LCI is similar to field weakening method of speed control of dc motors. At higher speeds the flux requirement is low and consequently motor draws less magnetizing current. Moreover, it also results in reduction of core loss in the motor. The copper losses are also reduced due to decrease in magnetizing current.Moreover,cooling is better at higher speed.Thus,the motor can develop more output for the same amount of losses and temperature rise. So a LCI fed single-phase induction motor can be competible with universal motor for high speed applications.

PROPOSED APPLICATIONS

The LCI fed induction motor operates as constant power drive above base speed . The scheme for three-phase induction motor is similar to that of single-phase induction motor.For a fly wheel energy storage system which is used for passenger car,computer no break power supply, LCI fed induction motor can be used. In this system the LCI will feed the machine while inputting the energy into the flywheel,the machine will be used as a self (capacitor) excited generator.Both experimental and theoritical works on such a system will be required before field applications.LCI fed induction motor can also be used in portable equipments such as mining drills in place of universal motor.In such applications,closed loop control can avoid breakage of tools under fault conditions by limiting the torque developed to the capacity of drill.The machine also becomes reliable for use in

inflammable atmosphere such as mines, chemical plants etc.The LCI fed three phase cage induction motor can be used in railway traction in place of dc series motor.

1.2 LITERATURE SURVEY

In industries, dc drives are being replaced by variable speed ac drives fed from solid state converters [1-6].Variable frequency converters fed ac motors are capable of giving performance similar to that of dc drives.A large volume of research work is available on the load commutated inverter fed synchronous motor drive [2,4,5,7-14] .Using the LCI,the characteristics of synchronous motor are obtained similar to that of dc motors, thus this system is also known as commutatorless dc motor (CLM). Tadakuma etal [7] have described the driving characteristics of commutatorless dc motor controlled by induced voltage detector.Rosa [8] has described the utilization and rating of machine commutated inverter fed synchronous motor drive. In which he has analyzed the operation of machine commutated thyristor inverter and the characteristics of the synchronous motor.Takeda etal [9] have discussed the generalized analysis for steady state performance characteristics of dc commutatorless motors.The variation of commutation angle and demagnetisation due to armature reaction, safety margin angle,average torque and speed with mean input current are discussed quantitatively for windings and saliency.

Tasucharya etal [10] and Ajay Kumar etal [11] have reported that the LCI along with the synchronous machine may give the performance like dc series motor and is called commutatorless dc series motor. But the scheme suffers from the disadantage of commutation failure due to increase in overlap angle of LCI and /or armature reaction of syschronous motor specially at higher loads .

Brockhoust [12] has described performance equation for dc commutatorless motor using salient pole type synchronous machine.In wnich,the development of design oriented aigebraic expressions of machine performance measures in terms of machine inductances is given.

In the recent past, few attempts have also been made for LCI fed three phase induction motor drive [15-24]. Rangandhachari etal [13,14] provided the synchronous machine along with LCI as a commutatorless shunt motor and variable frequency source to feed induction motor.This scheme has the disadvantage of using an extra synchronous machine,which not only affects the system efficiency and cost but also demands a separate dc source for excitation of synchronous machine.

Laithwaite etal [15-17] have described development of an induction machine commutated thyristor inverter for traction drives. In this scheme the leading reactive power requirement of

inverter is met by changing the design of machine such that it runs at leading power factor.The required modification in the machine causes the derating of it and extra cost of fabrication due to involved complexity in commutated.

Watson [18,19] has reported the work on self-commutated inverter fed induction motor drive.But it was limited to the feasibility of F.H.P. motor system. Moreover an extra transformer was used in the system.

Singh etal [20] have also described the feasibility of dc link self-commutated inverter fed induction motor system for its variable speed operation and its steady state behaviour.The active power is fed by a variable dc source.The leading reactive power requirement of the system is met by connecting a capacitor bank at the motor terminals.

Emil Levi [21,22] has proposed a three phase cage motor drive using resonant parallel inverter which is similar to LCI.In his first attempt he has described the characteristics of the three phase resonant parallel inverter fed induction motor drive. In his second paper, he has discussed the modelling and digital simulation of three phase resonant parallel inverter fed cage induction motor drive.

Fukao etal [23,24] in their first paper, they have described a high power high speed drive circuit using dual load commutated convertor and cage motor. In this drive circuit, the excitation current of inducton motor is provided and reverse emf is establised by the capacitors connected across the motor terminals. Relationship between the motor rating and capacitor size and operating frequency is derived. In their second paper, they have given analysis and characteristics of high speed drive using cage induction motor.

From the available literature [15-24], it is revealed that a good amount of work is done on load commutated inverter fed poly phase cage motor. But no single attempt is made on the LCI fed single phase induction motor, although it is also of much interest because of its various low power applications such as drive for mixer, grinder, drilling machine, blower etc. specially for replacing the troublesome universal motor. An attempt is, therefore, made in this investigation to obtain high speed maintainance free constant power drive using load commutated inverter fed single-phase cage induction motor.

1.3 SCOPE OF PRESENT WORK

The exhaustive literature survey reveals that no research work has been reported on the performance of load commutated inverter fed single-phase induction drive.In the present work, an attempt has been made to investigate the performance and closed loop control of LCI fed single-phase induction motor drive. The system consists of two single-phase fully controlled thyristor

bridge converters one for obtaining a variable dc voltage from fixed frequency ac supply to feed other convertor operating as LCI at variable frequency for cage motor. The capacitor alongwith controlled inductor is used to meet the variable leading reactive power requirement of LCI and cage induction motor over the wide range of frequency control. Various control singals for drive are obtained using microprocessor based system.

The present work has the following objectives:

1. Design and fabrication of two single-phase fully controlled converters, one acting as a rectifier and the other as an inverter.

2. Design and fabrication of thyristor circuit for phase controlled inductor.

3. Development of microprocessor control scheme.

4. Development of system software .

5. To develop an analytical model of the system to compute the no load and on load performance of the drive using equivalent circuit approach and the suitable numerical technique in open loop control.

6. The experimental investigation of open loop and closed loop performance of the system under steady state and dynamic conditions.

The whole scheme has been fabricated in a laboratory and the performance of the motor is obtained experimentally to verify the results obtained analytically.

Outline of the Chapters

In chapter 1, an introduction to the system is given.Solid state frequency converters to obtain speed control of ac drives are discussed. Exhaustive literature survey on the similar work is given.

In chapter 2, the complete hardware of the present scheme is discussed in detail. The design and selection of power modules,microprocessor based control scheme and firing circuits are described.

Chapter 3 deals with the implementation of system software. Flowcharts for different subroutines in conjunction with main program are given.

In chapter 4, an attempt is made on performance analysis of the drive. The mathematical equations for steady state

analysis are obtained using equivalent circuit approach. The computed results are given along with corresponding experimental results.

In chapter 5, steady state and dynamic performance of closed loop system, obtained experimentally is given along with the performance under open loop control of drive.

In last chapter, main conclusions along with salient features of the drive are discussed and suggestions for further work are enlisted.

The details of machines used, developed system software in machine language, developed computer program for analysis and pin details of different ICs used are given in appendices.

CHAPTER 2

DESCRIPTION OF THE SYSTEM

2.1 GENERAL

In this chapter, complete scheme of load commutated inverter fed single-phase induction motor drive is described. A microprocessor based control scheme is discussed together with hardware requirements. The synchronizing signals for converters are obtained by sensing terminal ac voltages . These signals are used as interrupts and at the same time to determine the frequency information of the machine terminal voltage . An eight bit eight channel analog to digital converter (ADC 0809) interfacing is given to convert required four analog signals into digital signals for control purpose of microprocessor based drive. The complete drive system is fabricated and the recorded waveforms of control signals at relevant points are also given.

2.2 PRINCIPLE OF OPERATION

The block diagram of the load commutated inverter fed single-phase induction motor drive is shown in Fig.2.1 . It basically consists of two single-phase fully controlled converters, one acting as a converter and other as a load commutated inverter, dc link inductor, single-phase induction motor, terminal capacitor, thyristor controlled inductor, a microprocessor based control scheme and a tachogenerator coupled with motor shaft. The fully control rectifier together with dc link inductor acts as a current source. DC link inductor suppresses harmonics in rectifier output and makes dc link current continuous. The rectifier is controlled to maintain constant terminal voltage of the motor. The inverter thyristor pairs are fired in alternate half cycles. Commutation of inverter thyristors is achieved by back emf of machine established with the help of terminal capacitor. Firing angle of the inverter is adjusted between 90 and 180deg. Capacitor provides leading reactive power which is essential for the system. The frequency of inverter output ac voltage is determined by capacitor value, inverter firing angle and terminal voltage. In the present scheme, for the operation of the drive above base speed, terminal voltage and inverter firing angle are kept constant. In open loop control of drive, speed is varied by varying terminal capacitor which supplies reactive power (leading) necessary for inverter and motor. Under steady state condition the leading reactive power supplied by capacitor must be equal to the sum of lagging reactive power of motor and inverter. If the capacitor value is decreased, leading reactive power will also be decreased, but the system will maintain the balance of reactive

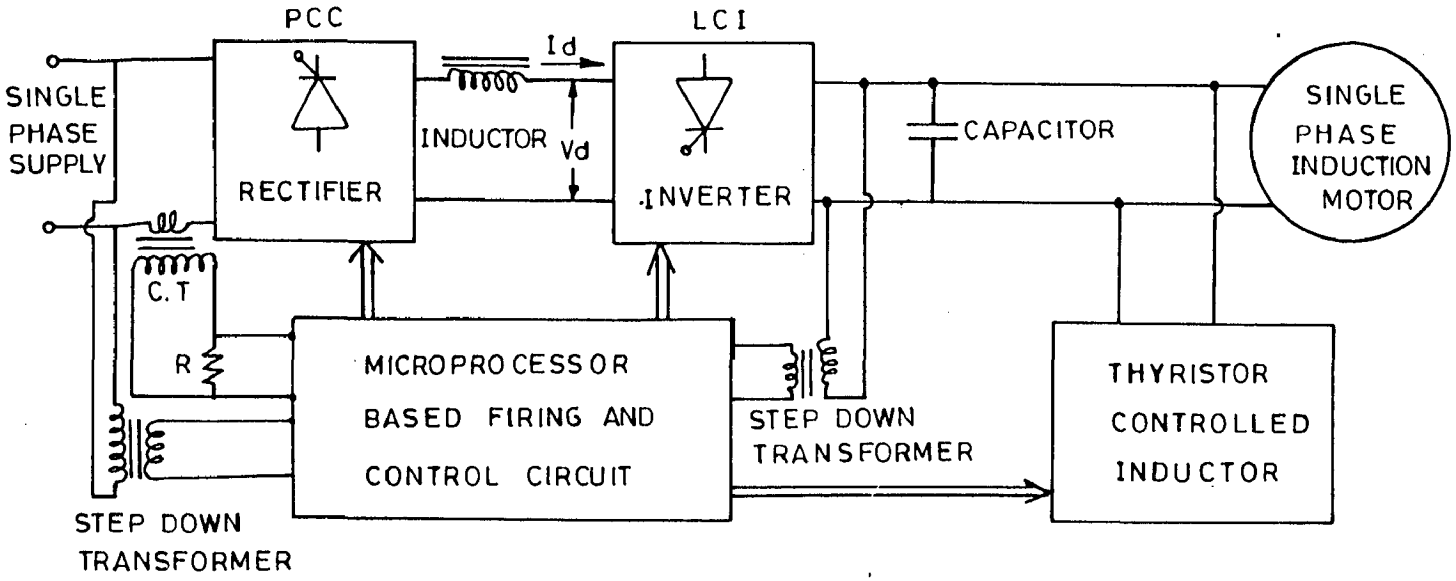


FIG. 2·1 — BLOCK DIAGRAM OF LCI FED SINGLE-PHASE INDUCTION MOTOR DRIVE

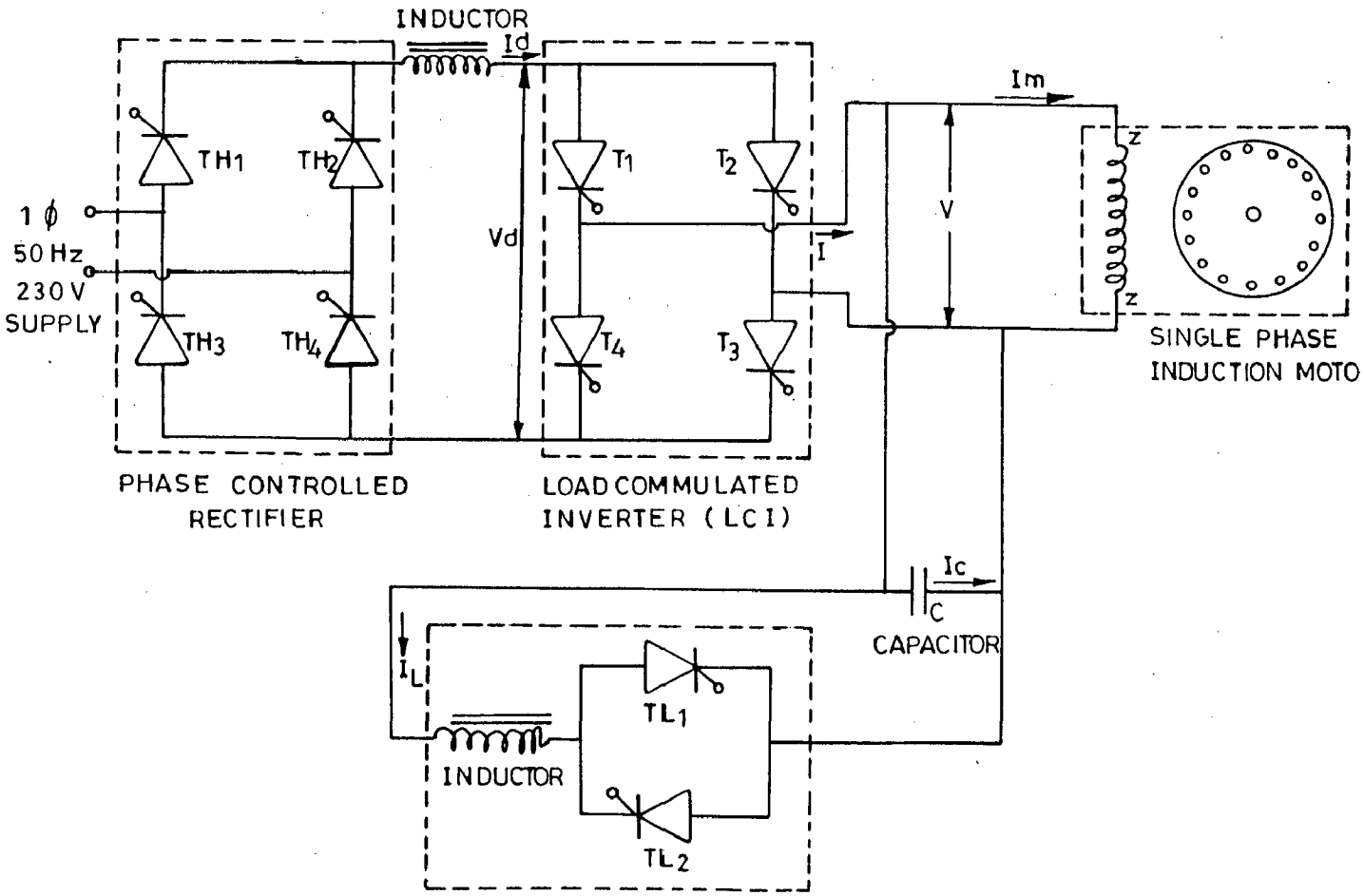


FIG. 2·2 — DETAILED POWER CIRCUIT DIAGRAM OF LCI FED SINGLE PHASE INDUCTION MOTOR DRIVE

power by increasing the frequency so that leading reactive power (proportional to frequency) becomes equal to the sum of lagging reactive power consumed by inverter and motor. Similarily the frequency of the system will decrease if the capacitor value is increased. The speed of the motor can be controlled by varying the capacitor value. The effective capacitor value can be varied either by varying the capacitor value itself or by varying lagging reactive power on the inverter ac side by keeping capacitor value fixed. In open loop control of the system, first method i.e. varying capacitor value can be used, but for closed loop operation of the drive, speed of motor can be controlled effectively by varying external lagging power source at machine terminals with fixed value of capacitor. The variable external lagging reactive power source may be as:

(a) Saturable core reactor

(b) Thyristor controlled inductor, and

(c) Use of static VAR generator

In the present scheme, thyristor controlled inductor is used for closed loop speed control. An inductor is connected in series with back to back connected thyristors. By varying firing angle of back to back connected thyristors, the effective inductor value or lagging reactive power is varied. The firing angle of controlled inductor thyristors is varied from 90 to 180 deg and firing is synchronized with inverter firing. The firing angle is adjusted to maintain speed constant in closed loop manner.

2.3 DESIGN AND SELECTION OF POWER MODULES

Fig. 2.2 shows the detailed power circuit diagram of the system. The power circuit is designed to meet requirements of the induction motor (details of which are given in Appendix-A). The power circuit for the proposed scheme consists of following parts:

(i) fully controlled rectifier bridge

(ii) dc link inductor

(iii) fully contolled converter as inverter (LCI)

(iv) thyristor controlled inductor

(v) terminal capacitor

Selection of thyristor ratings:

The following factors have to be considered for selection

of rating of thyristors:-

(a) Maximum peak inverse voltage (PIV) appearing across the thyristor

(b) Power circuit configuration

(c) Conduction angle of thyristor

(d) Average current and current waveform

For a single-phase bridge circuit PIV is twice the maximum value of terminal voltage . For terminal voltage of 230 V, PIV is 650 V . Taking a suitable safety factor, 1200 PIV thyristors are taken. Motor rated current is 7.1 A. Since each thyristor can conduct for 180 deg in each cycle, current through it is taken 3.55 A. Allowing a suitable safety factor and availability, thyristors are taken of 1200 PIV and 12 A for all parts of power circuit.

The value of controlled inductor is taken of reactance 30 ohms at 50Hz'. The value of dc link inductor is taken quite high so that dc link current becomes continous. The maximum value of variable terminal capacitor is taken 80 uf.

2.4 DESIGN OF MICROPROCESSOR CONTROL SCHEME

An eight bit 8085A microprocessor based scheme is used for the system development. The block diagram of the scheme is shown in Fig.2.3. In this scheme input output ports of a PPI 8255A (i) at J2 space are used. PCu is used for ADC interfacing and timer TM1 (11H) gate control. Port C lower is used for inputting square wave signals of rectifier and inverter and ADC end of conversion (EOC) signal. Port A is used for inputting eight bit digital output of ADC and port B is used for firing of thyristors, and controlling gate of timer TM2' (A2H). The interfacing circuit of 8253 is given in Fig. 2.7. Timer TM1 (11H) is used for loading the firing angle of rectifier thyristors. Timer TM2 (12H) is used for measurement of half cycle period of inverter output voltage . ~~Timer TM2 (A2H) is used for loading the firing angle of rectifier thyristors.~~ Timer TM2'(A2H)is used for loading the firing of thyristors of controlled inductor. Programmable interrupt controller (PIC 8259A) is used for managing five interrupts, two for rectifier and three for inverter and controlled inductor as shown in Fig. 2.3.

2.4.1 ADC Interfacing

ADC 0809 is interfaced for converting four analog quantities into digital quantities. These quantities are reference speed, actual speed, terminal voltage of motor and dc link current. Reference speed signal is given to IN0 channel (Pin No. 26), actual speed signal to IN2 channel (Pin NO. 28),

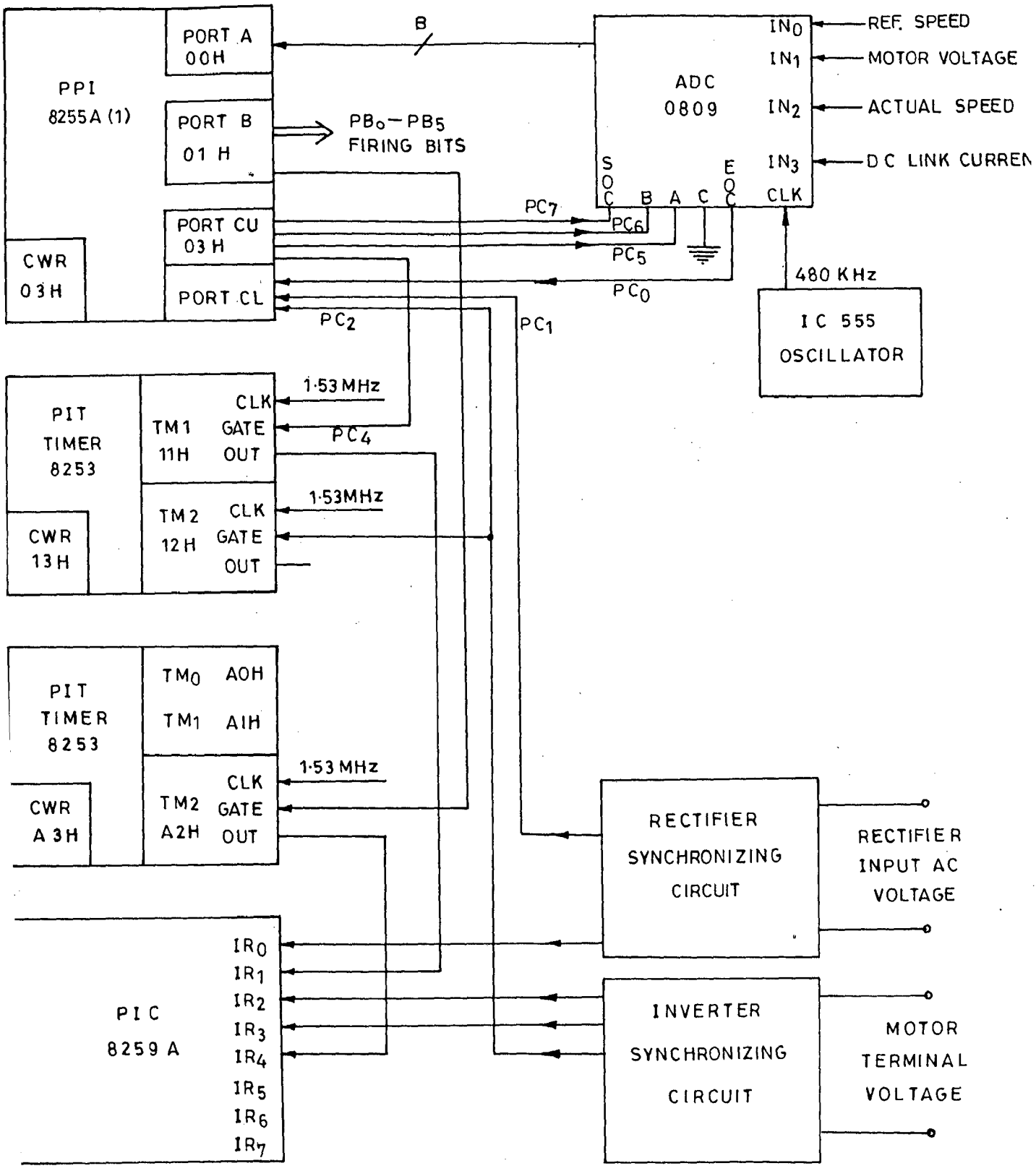


FIG. 2·3 – MICROPROCESSOR BASED SYSTEM CONFIGURATION

terminal voltage signal to IN1 channel (Pin No. 27) and dc current signal to IN3 channel (Pin No. 1) of ADC. Actual speed signal is obtained from ac techogenerator coupled with motor shaft. The output of techogenerator is reduced from zero to five voltage range, rectified by a diode bridge rectifier, filtered by a capacitor filter and connected to ADC channel through a variable potential divider. Motor terminal voltage signal is obtained by filtering the rectified output of step-down transformer and it is connected to ADC channel via variable potential divider. DC link current signal is obtained by sensing rectifier input supply current by a current transformer (CT).The output of CT is rectified and filtered. It is connected to ADC channel via variable potential divider. Reference speed signal is given by a variable potential divider. ADC channels are selected through PC5 and PC6 bits of port C upper. Start of conversion (SOC) signal for ADC is given via PC7 bit of port C upper. End of conversion (EOC) of ADC is inputted via PC0 bit of port C lower. Clock for the ADC is generated by a 555 timer of 480 KHz.

2.4.2 Synchronizing Circuit and Generation of Interrupt Signal (IR0) for Rectifier

For a converter the thyristor firing must be synchronized with the input ac voltage . For a single-phase rectifier, synchronizing signal is required at each zero-crossing of input ac voltage . This signal at each zero-crossing of supply voltage is considered as the IR0 interrupt signal. Fig. 2.4a shows the circuit diagram of synchronizing circuit for the rectifier. In this figure, the step-down transformer is a centre tapped one. The ac voltage output of step-down transformer is rectified by two diodes and is given to comparator(I) (realised through 741 operational amplifier). Reference input to this comparator is given a small positive voltage (0.25V). The comparator output is inverted using a transistor invereter to get output of +5V magnitude. Fig. 2.4b shows the theoritical expected waveforms at different points in this circuit. The output of transistor inverter goes high just before the actual zero crossing of input ac voltage . This signal is given to IR0 interrupt channel of PIC (Pin No. 18 of 8259A). The output of step-down transformer is also given to another comparator (II), reference input(Pin No. 2 of 741) of which is grounded. Output of this comparator is a square wave which is reduced to +5V magnitude by a transistor inverter. This signal is used to decide the rectifier index R (to be used for discriminating the thyristor pairs).

2.4.3 Synchronizing Circuit and Generation of Interrupt Signals (IR2 and IR3) for Inverter and Controlled Inductor

The inverter synchronizing circuit shown in Fig. 2.5a is similar to Fig. 2.4a used for rectifier except that the comparator (I) output is inverted twice so that it goes high just

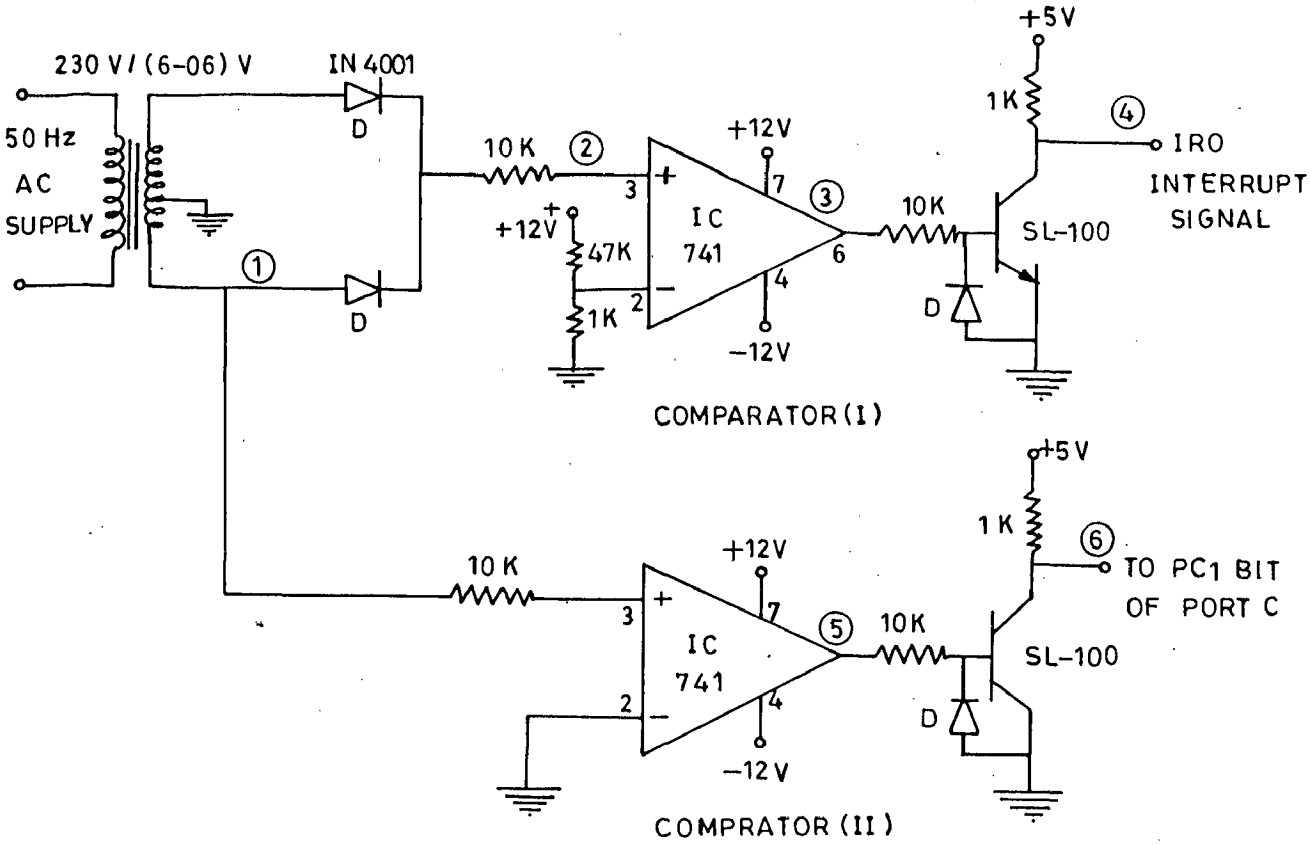


FIG. 2·4 (a)–SYNCHRONIZING CIRCUIT FOR RECTIFIER

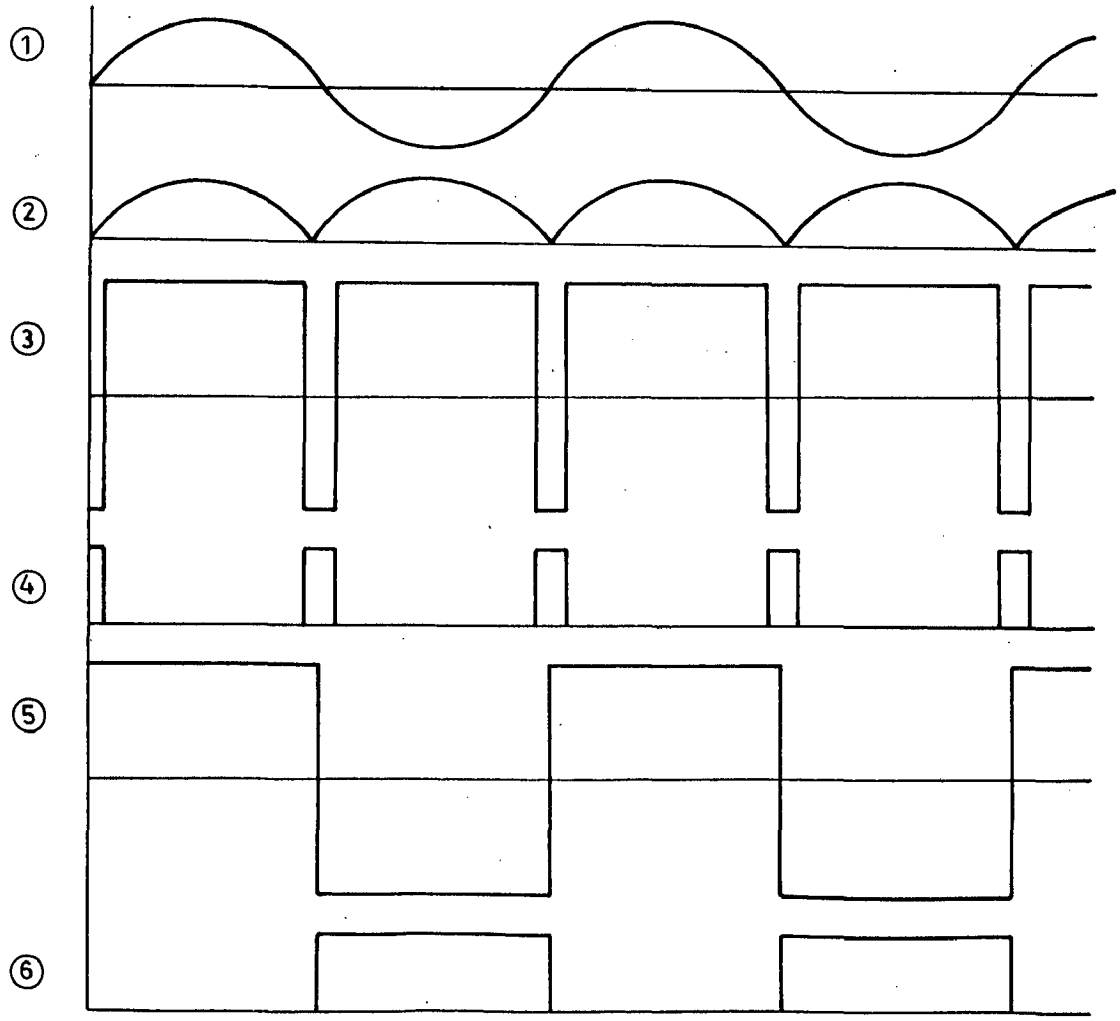


FIG. 2·4 (b) – THEORITICAL WAVE FORMS AT DIFFERENT POINTS IN SYNCHRONIZING CIRCUIT OF FIG. 2·4 (a)

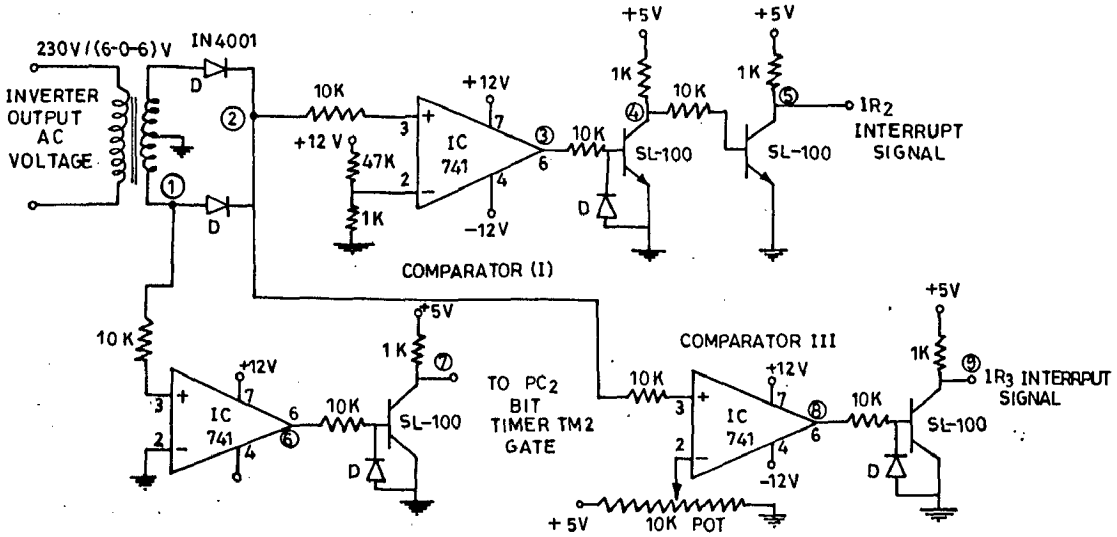


FIG. 2·5(a)—SYNCHONIZING CIRCUIT FOR INVERTER

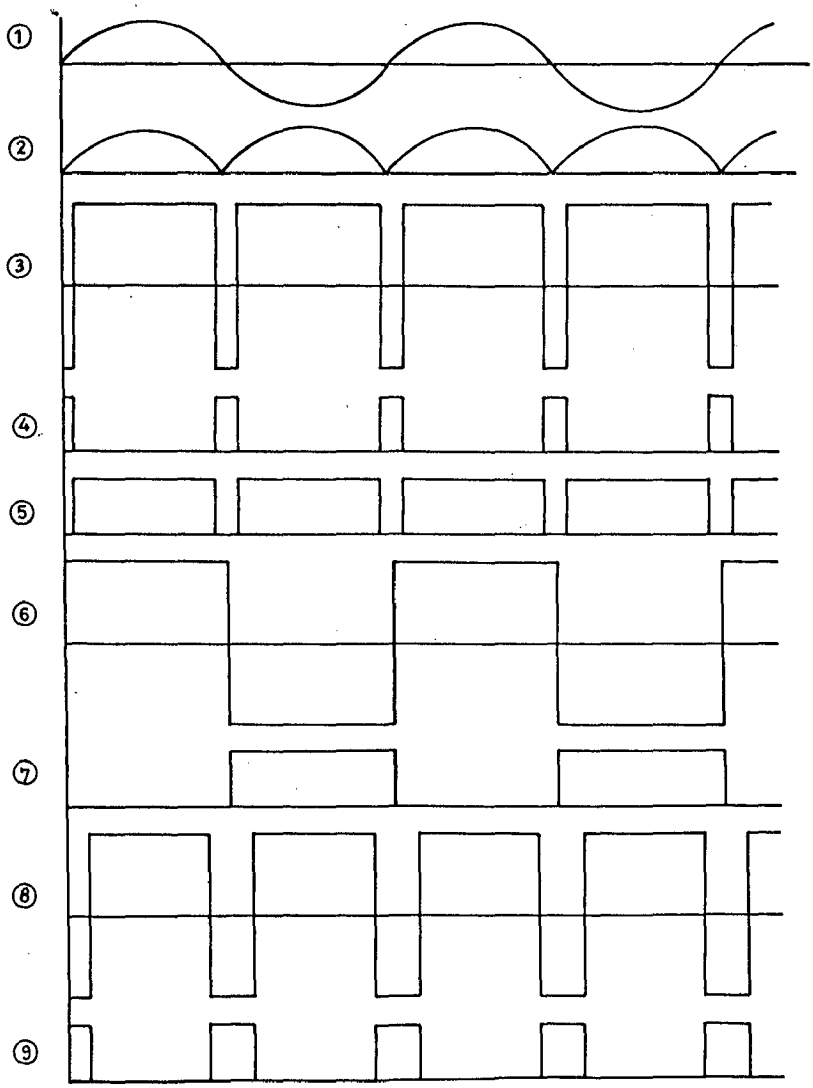


FIG. 2·5(b)—THEORITICAL WAVE FORMS AT DIFFERENT POINTS IN SYNCHRONIZING CIRCUIT OF FIG. 2·5(a)

after the actual zero crossing of inverter output ac voltage . It is used as IR2 interrupt signal to PIC (Pin No 20 of 8259A). The square wave signal is generated to decide inverter index I in similar manner as in Fig. 2.4a. For that purpose this signal is connected to PC2 bit of port C lower . This signal is also used to determine 180 deg count of motor voltage through timer TM2(12H) . In Fig. 2.5a, the circuit for generating interrupt signal (IR3) for firing of inverter thyristors is also shown. The rectified voltage signal is given to comparator(III), reference to this comparator is given by a potential divider. The output of comparator (III) is inverted by a transistor inverter to obtain IR3 interrupt signal for PIC(Pin No. 21 of 8259A). The IR3 interrupt signal goes high after firing angle of inverter which is adjustable between 90 and 180 deg. Fig. 2.5b shows the theoritical waveforms at different points of the circuit given in Fig. 2.5a. ,

2.4.4 Pulse Amplifier Circuits

Fig. 2.6 shows the pulse amplifier circuit of one channel for thyristor firing. The firing command from microprocessor system through port B bit is ANDed with high frequency (16KHz) generated by a 555 timer to avoid saturation in pulse transformer. Pulse transformer is used to isolate control circuit from power circuit. The high frequency ANDed pulse is amplified by a transistor amplifier (SL-100) and fed to pulse transformer primary which is connected in collector circuit. Gate protection is required for over voltage and over current . Over voltage protection is achieved by connecting a diode across gate and cathode. For over current protection a series resistance is connected in gate circuit. A capacitor is connected across gate and cathode to bypass noise or spurious pulses.

2.5 RESULTS AND DISCUSSIONS

The complete scheme for microprocessor based drive is fabricated and tested with the developed software (given in next chapter). The various waveforms in the control circuit for rectifier, inverter and controlled inductor are recorded by X-Y recorder and shown in Fig. 2.8. The recorded waveforms are similar to the theoritical expected waveforms. The entire control scheme shows the satisfactory performance with power circuit .

2.6 CONCLUSIONS

The complete hardware scheme of load commutated inverter fed single-phase induction motor drive is described in detail. Microprocessor based control scheme consisting of ADC interfacing, synchronizing circuits and amplifier circuits is tested with developed software . The power circuit consisting of two fully controlled converters, thyristor controlled inductor

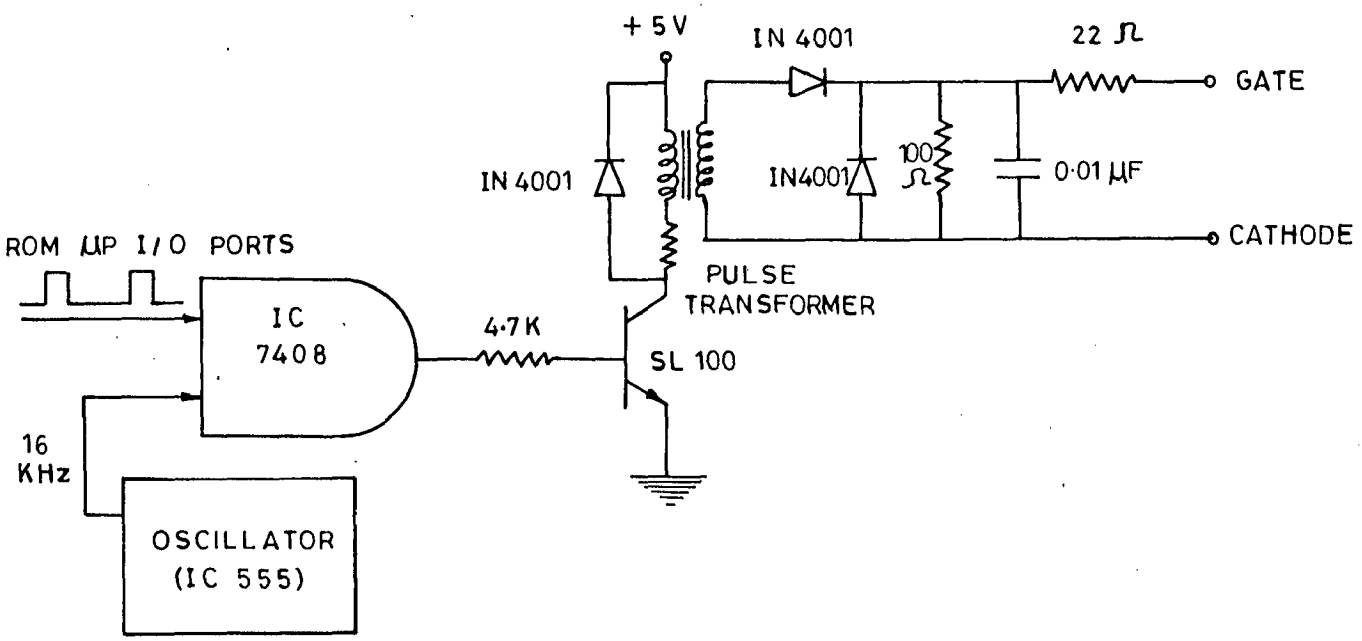


FIG. 2·6—PULSE AMPLIFIER CIRCUIT

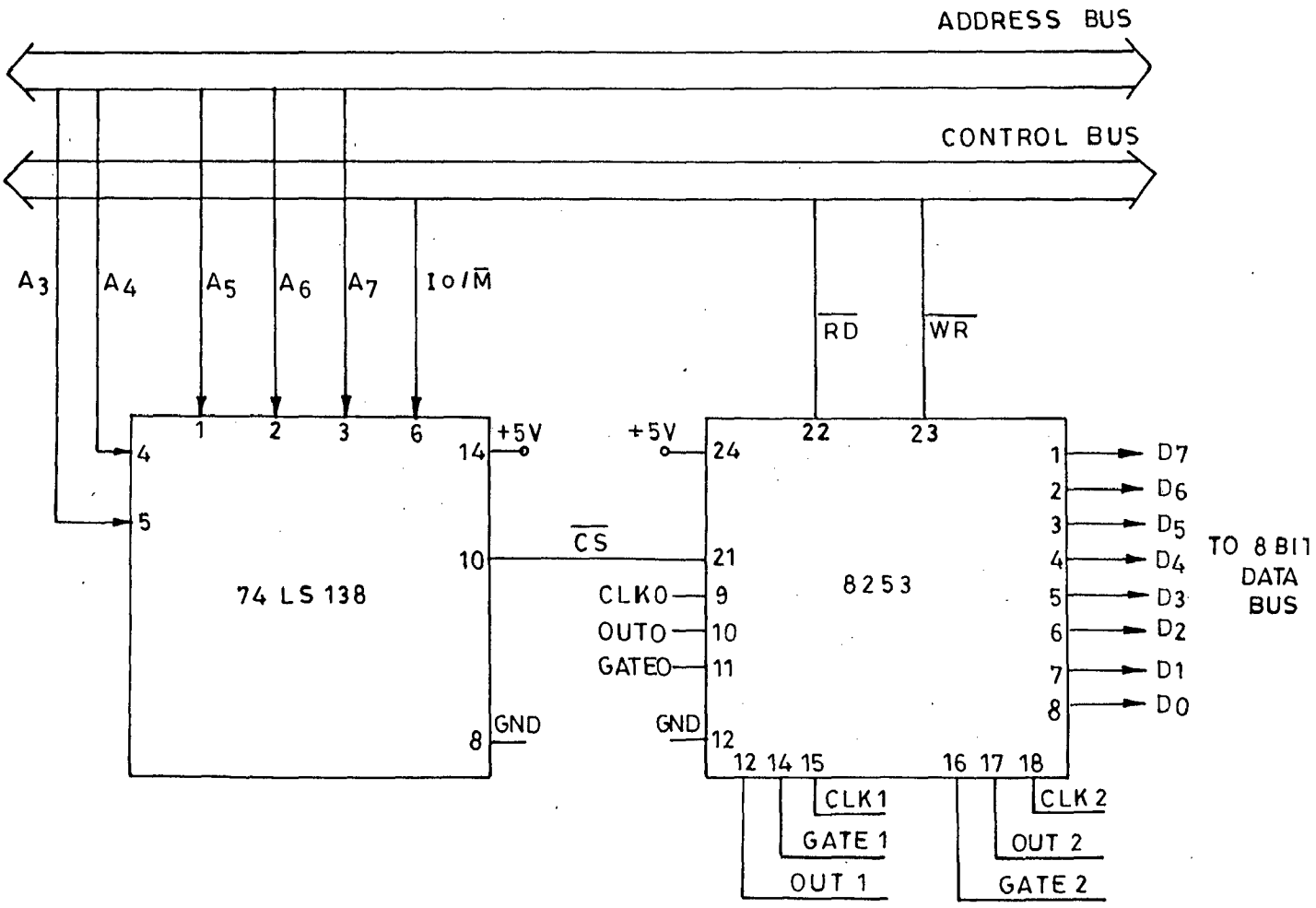
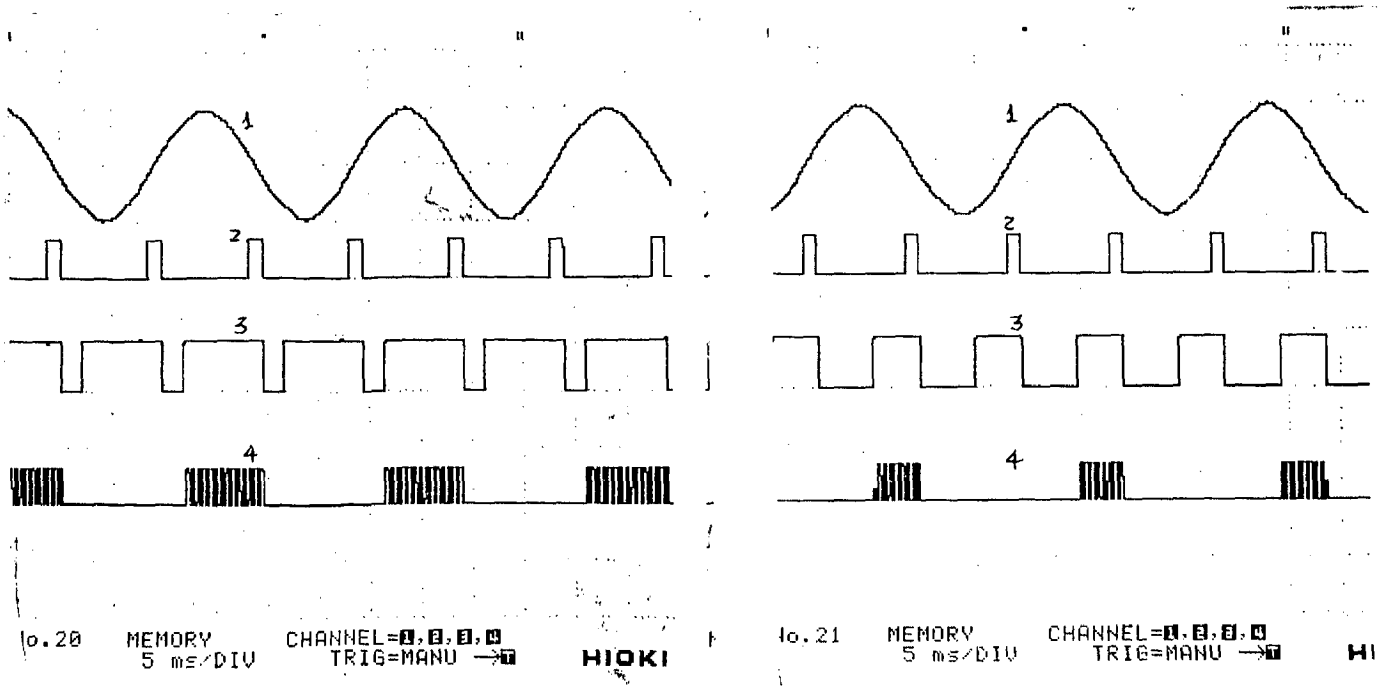
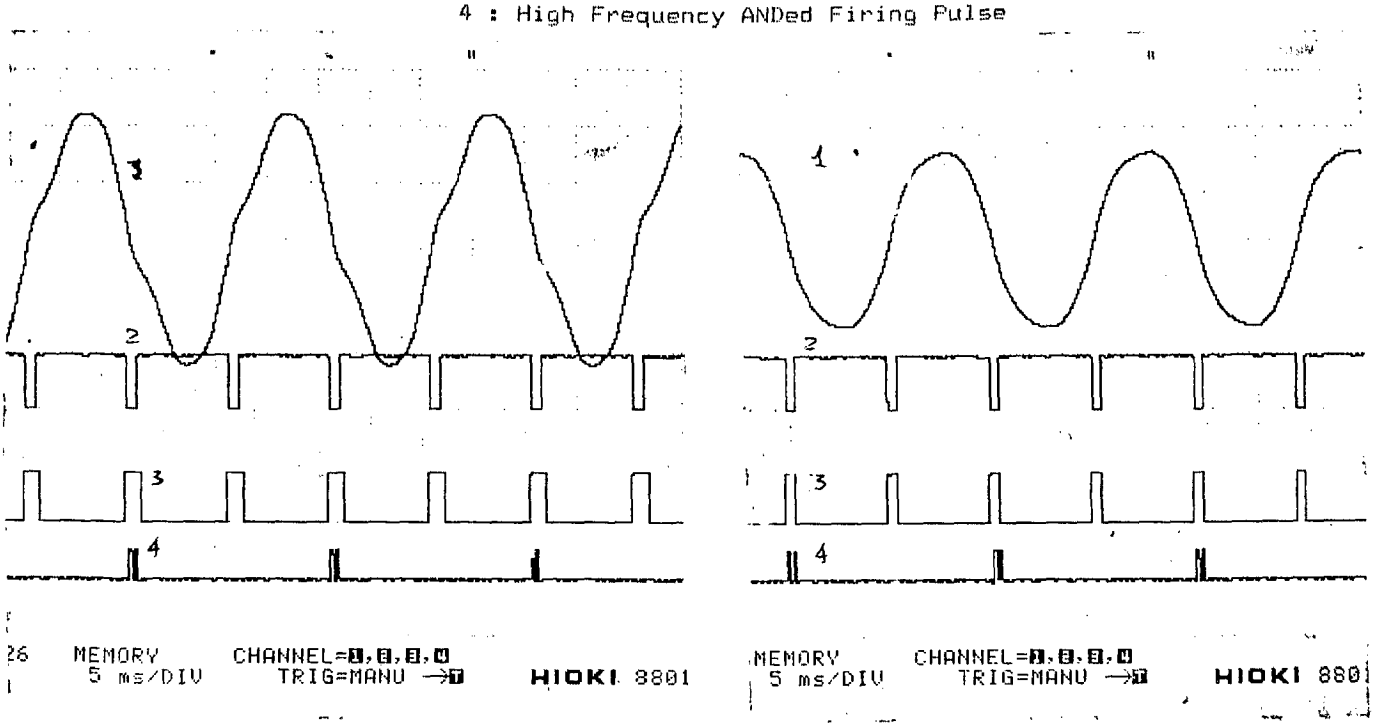


FIG. 2·7—TIMER 8253 INTERFACING CIRCUIT



(a), (b) 1 : Voltage Signal
2 : IRO Interrupt Signal
3 : IR1 Interrupt Signal
4 : High Frequency ANDed Firing Pulse



(c) 1 : Voltage Signal
2 : IR2 Interrupt Signal
3 : IR3 Interrupt Signal
4 : High Frequency ANDed Firing Pulse

(d) 1 : Voltage Signal
2 : IR2 Interrupt Signal
3 : IR4 Interrupt Signal
4 : High Frequency ANDed Firing Pulse

Fig.2.8 CONTROL CIRCUIT WAVEFORMS OF [(a),(b)] RECTIFIER CIRCUIT, (c) INVERTER CIRCUIT AND CONTROLLED INDUCTOR CIRCUIT RECORDED BY X-Y RECORDER

and terminal capacitor works satisfactorily with the microprocessor based control scheme. The various control signals are observed similar to the desired ones.

CHAPTER 3

SYSTEM SOFTWARE IMPLEMENTATION

3.1 GENERAL

In this chapter, microprocessor and its peripheral devices are described. The required software for speed control scheme of LCI fed single-phase induction motor drive is discussed. Flow-charts for the main program along with various subroutines are given. These subroutines are ADC subroutine, IR0 interrupt subroutine, IR1 interrupt subroutine, IR2 interrupt subroutine, IR3 interrupt subroutine, IR4 interrupt subroutine. IR0 and IR1 subroutines deal with operation of rectifier and IR2, IR3 and IR4 subroutines are for inverter and thyristor controlled inductor. In IR0 subroutine, firing angle of rectifier is adjusted to maintain inverter output voltage (motor terminal voltage) constant and IR2 subroutine is for firing angle control of thyristors of controlled inductor which is used to regulate the speed of motor.

3.2 MICROPROCESSOR AND ITS PERIPHERALS

The digital control scheme for the load commutated inverter fed single-phase induction motor drive has been developed using microprocessor 8085A system. An 8085A is 8 bit INTEL'S most popular microprocessor. In this system, the programmable interrupt controller(PIC) 8259A, programmable interval timer(PIT) 8253 and the programmable peripheral interface (PPI) 8255A are interfaced. The system has the provision of interfacing some more peripherals too.

Peripherals are used to facilitate parallel data transfer between microprocessor and input output devices. These devices can act as input port which is tri-stated buffer to read data from inputting devices. They can act as output port to latch data sent by the microprocessor for output device. These devices can generate an interrupt signal and receive/transmit certain control signals for data communication between microprocessor and input-output devices.

The 8255A is a programmable peripheral interface (PPI). It can be programmed to transfer data under various conditions. It has 24 I/O pins, that can be grouped primarily in to 8 bit parallel ports, port A, port B and remaining 8 bits as port C. Eight bits of port C can be used individually or be grouped in two 4 bit ports. Port C upper (PCu) and port C lower (PCl). The functions of these ports are defined by writing a control word in control word register, format of which is shown in Fig. 3.1. Functions of the 8255A are classified according to two modes: the Bit Set/Reset (BSR) mode and the I/O mode . The BSR mode is to set

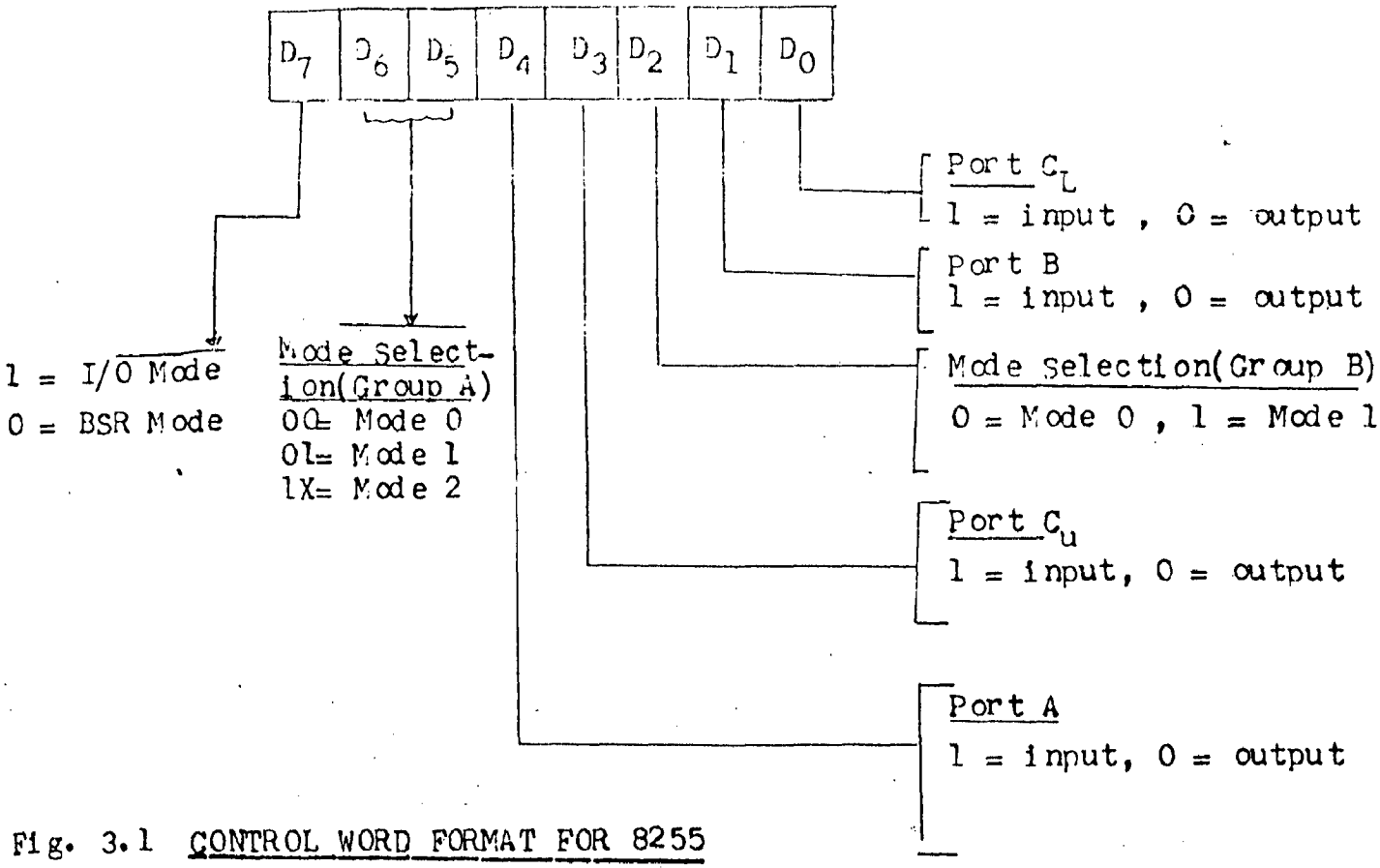


Fig. 3.1 CONTROL WORD FORMAT FOR 8255

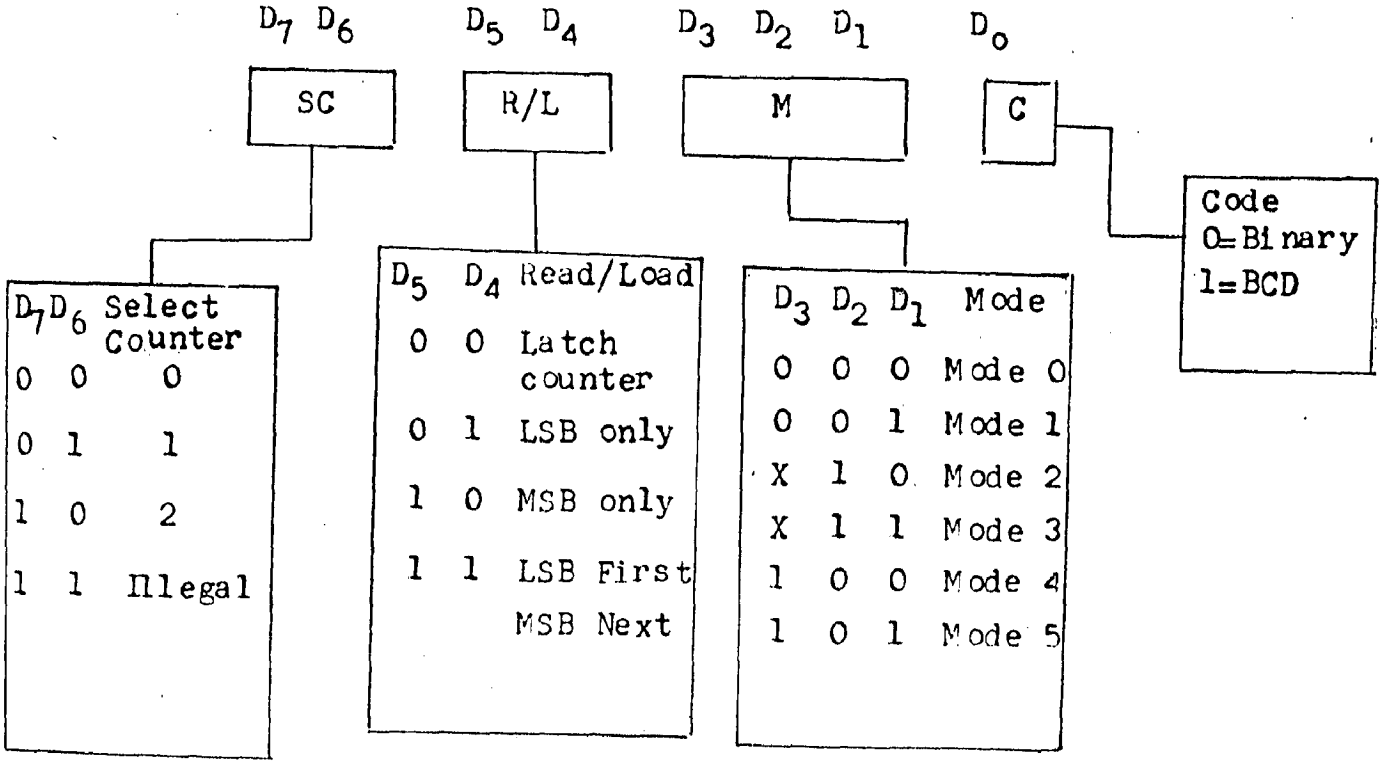


Fig. 3.2 : CONTROL WORD FORMAT OF 8253

or reset the bits of port C.The I/O mode is further divided into three modes:Mode 0,Mode 1 and Mode 2.In Mode 0 all ports function as simple input output ports . In Mode 1 port A and/or port B use bits from port C as hand shaking signals that is why this mode is named as hand-shake mode . In hand-shake mode , two types of input/output data transfer can be implemented : status check and interrupt.In Mode 2 ,port a can be set for by directional data transfer using hand-shake signals from port C , and port B can be set up either in Mode 0 or in Mode 1 .

The 8253 programmable interval timer (PIT)is a support chip to the system. The 8253 includes three identical 16 bit counters that can operate independently in any one of the six modes. Each counter has two input signals CLOCK and GATE and one output signal OUT.The CLOCK input pin is connected to a clock of suitable frequency . To operate a counter , a 16 bit count to be loaded in its register and depending upon the mode of the timer , logic high voltage or low to high voltage transition at GATE initiates or enables counting process .The different six mode of operation are Mode 0-interrupt on terminal count, mode 1-programmable mono shot, Mode 2-rate generater or divide by counter,Mode 3- square wave generater,Mode 4-software triggered strobe,Mode 5 hardware triggered strobe.The control word format of 8253 is shown in Fig. 3.2.

The 8259A is a programmable interrupt controller (PIC) designed to work with Iintel microprocessor 8080A, 8085A, 8086 and 8088.The 8259 A can manage eight interrupts according to the instructions written into its control word registers. This is equivalent to providing eight interrupt pins on the processor in place of one INTER/INT pin. It can vector an interrupt request anywhere in the memory map . However , all eight interrupts are spaced at the interval of either eight or four locations . It can resolve eight levels of interrupt priorities as a variety of modes, such as fully nested mode , automatic rotation mode and specific rotation mode. It can mask each interrupt request individually .The 8259 A can read status of pending, in-service interrupts and masked interrupts . It can accept either the level-triggered or the edge -triggered interrupt request . It can be expanded to 64 priority levels by cascading additional 8259's. To implement interrupts, the interrupt enable flip-flop in the microprocessor should be enabled by writing the EI instruction and the 8259 should be initialized by writing control words in the control word register. The 8259 requires the two types of control words:initialization command words (ICWS) and operation command words (OCWS). The 8259 can be initialized with four ICWS; the first two are essential , and the other two are optional.Based on the modes being used,these words must be issued in a given sequence .Once initialized, the 8259 can be set-up to operate in various modes by using three different OCWS; however , they no longer need to be issued in a specific sequence.

3.3 MAIN PROGRAM

The flow chart of the main program is shown in Fig. 3.3. The program is started with initialization of STACK pointer and the input-output ports . In the 8085 system ,two timers and six input output ports available to the user at J1 , J2 and J3 space (details are given in Appendix-D).In the present work, three timers are used. They are TM1 (11H),TM2 (12H) of 8085 system and TM2'(A2H) of extra timer 8253 chip interfaced with the system.The timer TM2'(A2H) of extra timer chip is used for loading firing angle of thyristor controlled inductor.The TM1(11H) of the system is used for loading the firing angle of the rectifier. The timer TM2(12H) of the system is used to count 180 deg of the inverter output ac voltage.Out of six input output ports,three input/output ports of 8255 (1) are used in the present work. It is initialized as follows:

8255(1) (CWR=03H)

PORT A	PORT B	PORT Cu	PORT Cl	
IN	OUT	OUT	IN	1001001 = 91H

FIG 2.3, given in the last chapter, shows the configuration of the microprocessor control scheme. Port A is used for inputing digital output of ADC,port B is used for firing the rectifier thyristors (Bits PB0 and PB1), firing inverter thyristors (Bits PB2 and PB3), firing thyristors of controlled inductor (Bits PB4 and PB5) and controlling the gate of timer TM2' (A2H) (Bits PB6). Port C is used for generating hand shaking signals, controlling timer TM1 (11H) gate (Bit PC4) and inputing synchronizing singnals of rectifier and inverter.

The timers are intialized as follows:

TM1 (11H) in mode zero

TM1	R/L	MODE O	CODE	
01	11	000	0	= 70H

TM2 (12H) in mode zero:

TM2	R/L	MODE O	CODE	
10	11	000	0	= B0H

TM2'(A2H) in mode zero:

TM2'	R/L	MODE O	CODE	
10	11	000	0	= B0H

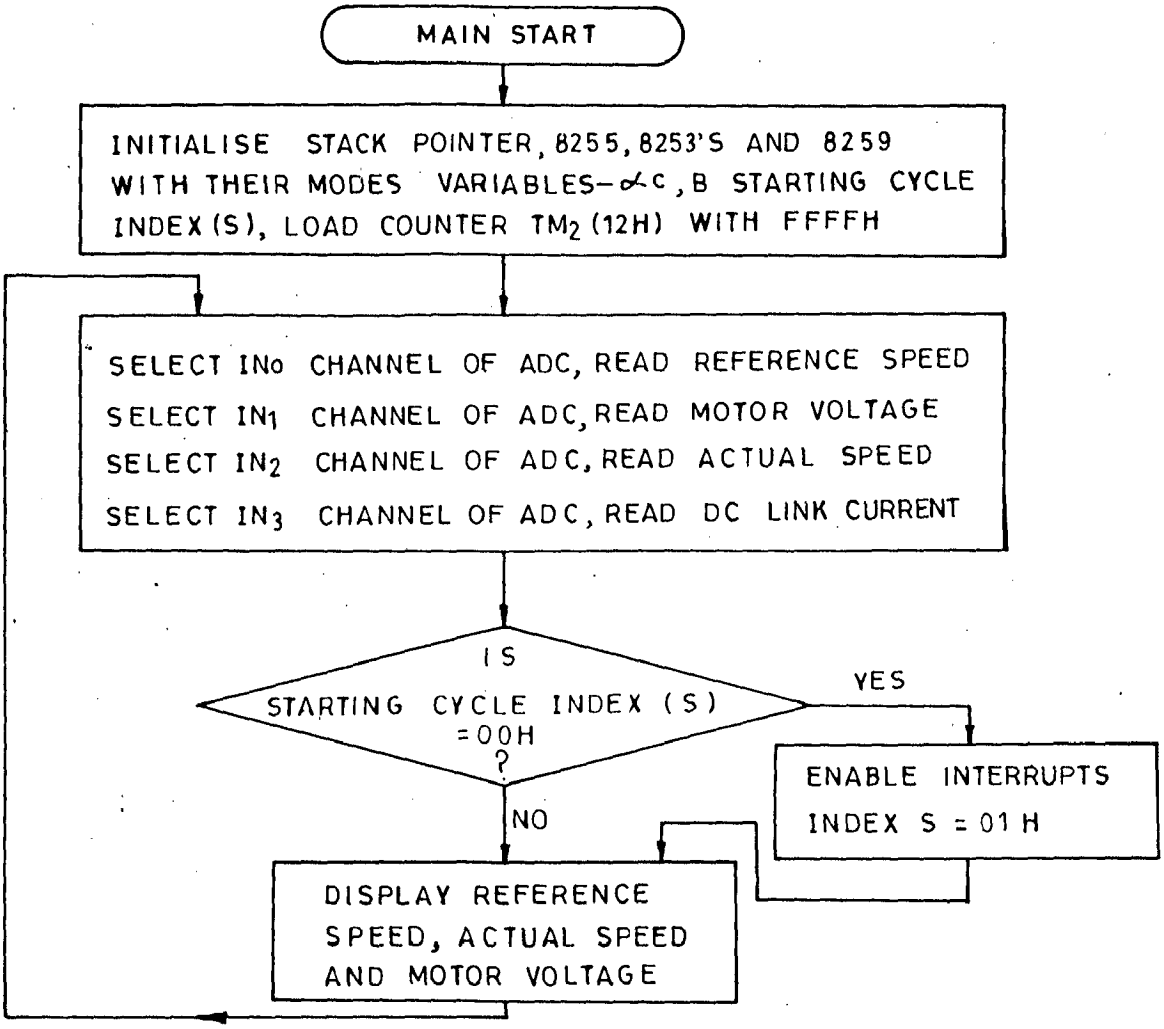


FIG.3·3—FLOW CHART OF MAIN PROGRAM

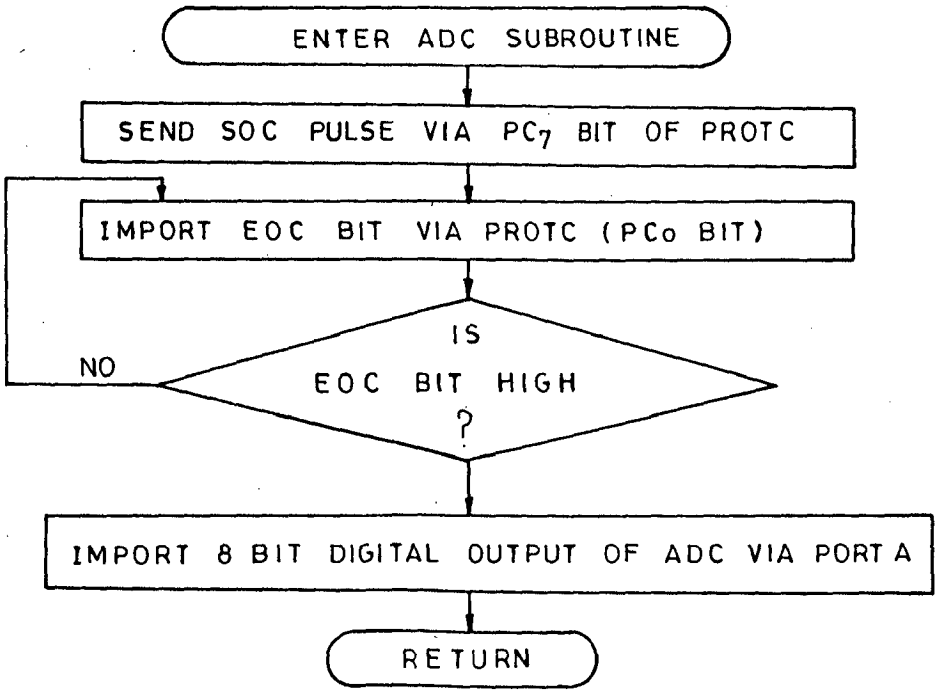


FIG.3·4—FLOW CHART OF ADC SUBROUTINE

After initialization of all the necessary chips all firing bits are made low and the status of output ports are stored. Initial value of rectifier firing angle is stored and starting index S is stored as 00H and initial value of B, to be explained later is stored. The PIC is intialized next for the vector addresses of the interrupts IR0, IR1, IR2, IR3, IR4. All interrupts are edge triggered.

After initialization process is over, four ADC channels are inputted one by one by selecting channels through port Cu. Reference speed is inputted by selecting IN0 channel of ADC, inverter output voltage is inputted by selecting IN1 channel, actual speed is inputted by selecting IN2 channel and dc link current is inputted by selecting IN3 channel. After inputting all four channels starting index S is checked. If it is zero, then the interrupts are enabled and the index S is incremented and stored. If the starting index S is one then it displays reference speed, actual speed, (in address field of kit) and inverter output voltage (in data field of kit) and the execution is transferred back to input ADC data.

3.4 ADC SUBROUTINE

Reference speed, actual speed, inverter output voltage and dc link current are measuerd and stored through this subroutine. The reference speed is set to a value from a variable potential divider and fed to ADC via IN0 channel. The inverter output voltage signal is given to IN1 channel of the ADC. The actual speed signal is given to IN2 channel and dc link current to IN3 channel. The ADC converts the analog quantities into digital data. The analog to digital conversion of all four quantities is done in every looping of main program. Clock to the ADC is given from a oscillator (555 timer) of frequency 480 KHz. The ADC starts converting the analog input signal into digital data at the instant, when the start of conversion (SOC) bit of ADC goes from low to high to low. ADC sends end of conversion (EOC) signal to the input, output port through the PC0 bit, indicating that the conversion process is over. The digital value is read through port A. Channel selection is done in main program. The flow-chart is shown in Fig.3.4. The scale factors are:

2V = 01H for IN1 channel, 1A = 14H for 2N3 channel and

12RPM = 01H for IN0 and IN2 channels

3.5 IR0 INTERRUPT SUBROUTINE

Fig. 3.5 shows the flow-chart of IR0 interrupt subroutine. IR0 interrupt occurs at each zero crossing of rectifier input voltage signal. Program is entered by saving the registers. Firing

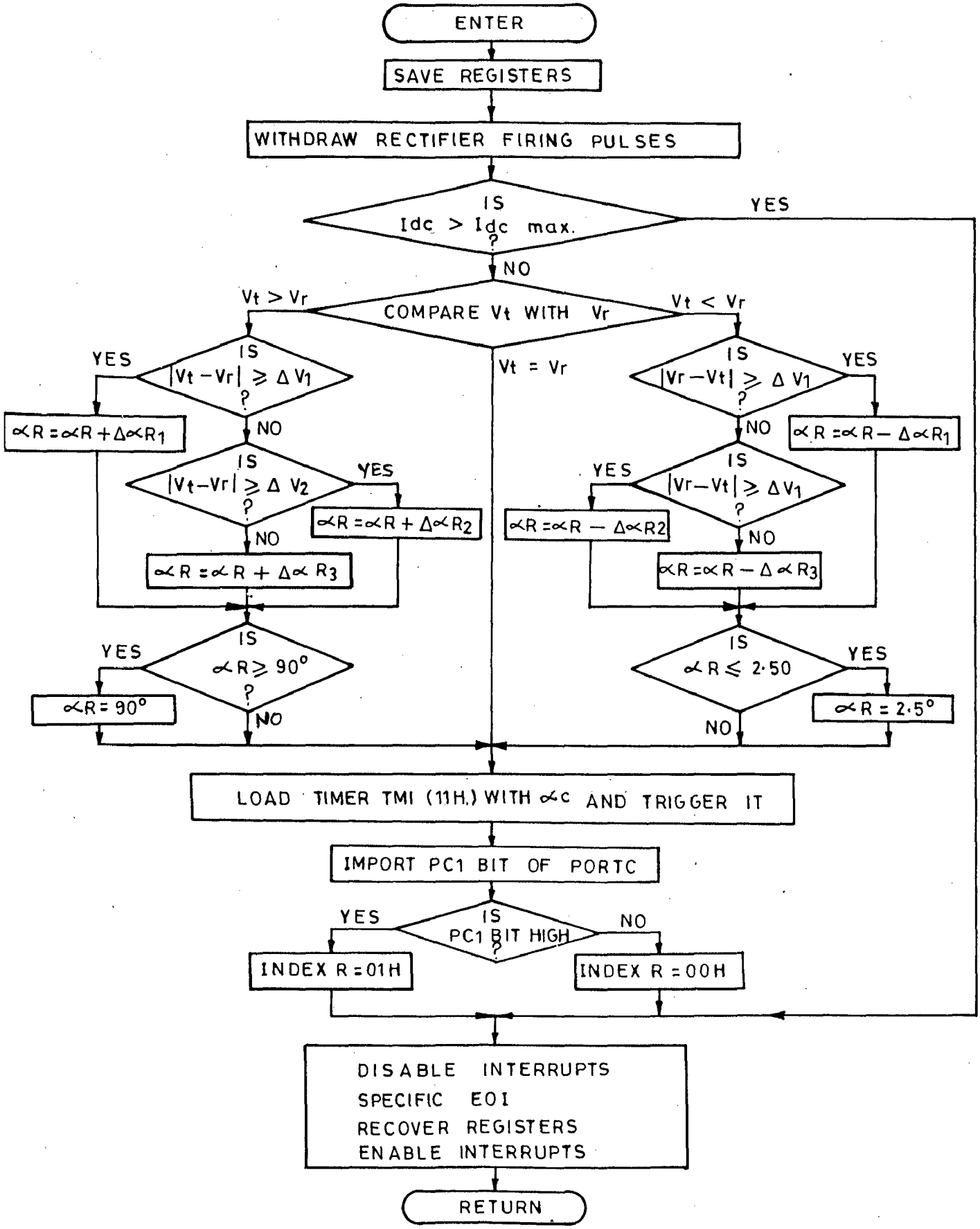


FIG. 3·5 — FLOW CHART OF IRo INTERRUPT SUBROUTINE

bits of rectifier are made low.The dc link current is checked, if it exceeds its maximun limit (Idc max) then the rectifier firing is stopped. If the dc link current is lesser than its limit then inverter output voltage is checked.If the inverter output voltage is less than the rated voltage of the motor,then rectifier firing angle is decreased. If the inverter output voltage is more than the rated value, then rectifier firing angle is increased. If it is equal to rated value then there is no change in firing angle. The change in the firing angle is decided according to the difference in inverter output voltage and rated voltage of motor. If difference is large, then the change in count corresponding to firing angle is taken more, if difference is small, then change in the count is taken less. The firing angle (count) is adjusted on the every IR0 interrupt to keep inverter output voltage equal to rated voltage of the motor. Timer TM1 (11H) is loaded with firing angle (count) and triggered through PC4 bit of port Cu. The rectifier indexRis decided depending upon the status of PC1 bit of port C1. If it is low then index R is set to 00H. If it is high then R is set to 01H, program returns after issuing specific end of interrupt command (EOI) and recovering registers.

3.6 IR1 INTERRUPT SUBROUTINE

Fig. 3.6 shows the flow-chart of IR1 interrupt sobroutine. This IR1 interrupt occurs when timer TM1(11H) count value becomes equal to zero. This subroutine is used to fire a next pair of thyristors of rectifier after each half cycle.The program is entered by saving registers. After it, rectifier firing index R is checked. If this index R is 00H, then thyristor pair (1,3) of rectifier is fired.If index R is 01H then thyristor pair (2,4) is fired.After firing particular pair timer TM1(11H) gate is made low. Program returns after issuing specific end of interrupt command and recovering registors.

3.7 IR2 INTERRUPT SUBROUTINE

Fig.3.8 shows the flow-chart of this subroutine. IR2 interrupt occurs at each zero crossing of inverter output voltage signal. Program is entered by saving the registors. Firing bits for thyristors of inverter and controlled inductor are made low. Synchronizing signal is checked via PC2 bit of port C1 to decide inverter index I. If the status of PC2 bit is low then the inverter index is set to 00H and then timer TM2 (12H) is read and loaded by FFFFH for next cycle. 180 deg and 90 deg counts are calculated and stored. Now the actual speed is compared with the reference speed. If the actual speed is lesser than the reference speed then B (α L = 180 deg - B, α L is thyristor's firing angle of controlled inductor) is increased and if actual speed is greater than reference speed then B is decreased. If both are equal then no change is done in B. The change in B is decided

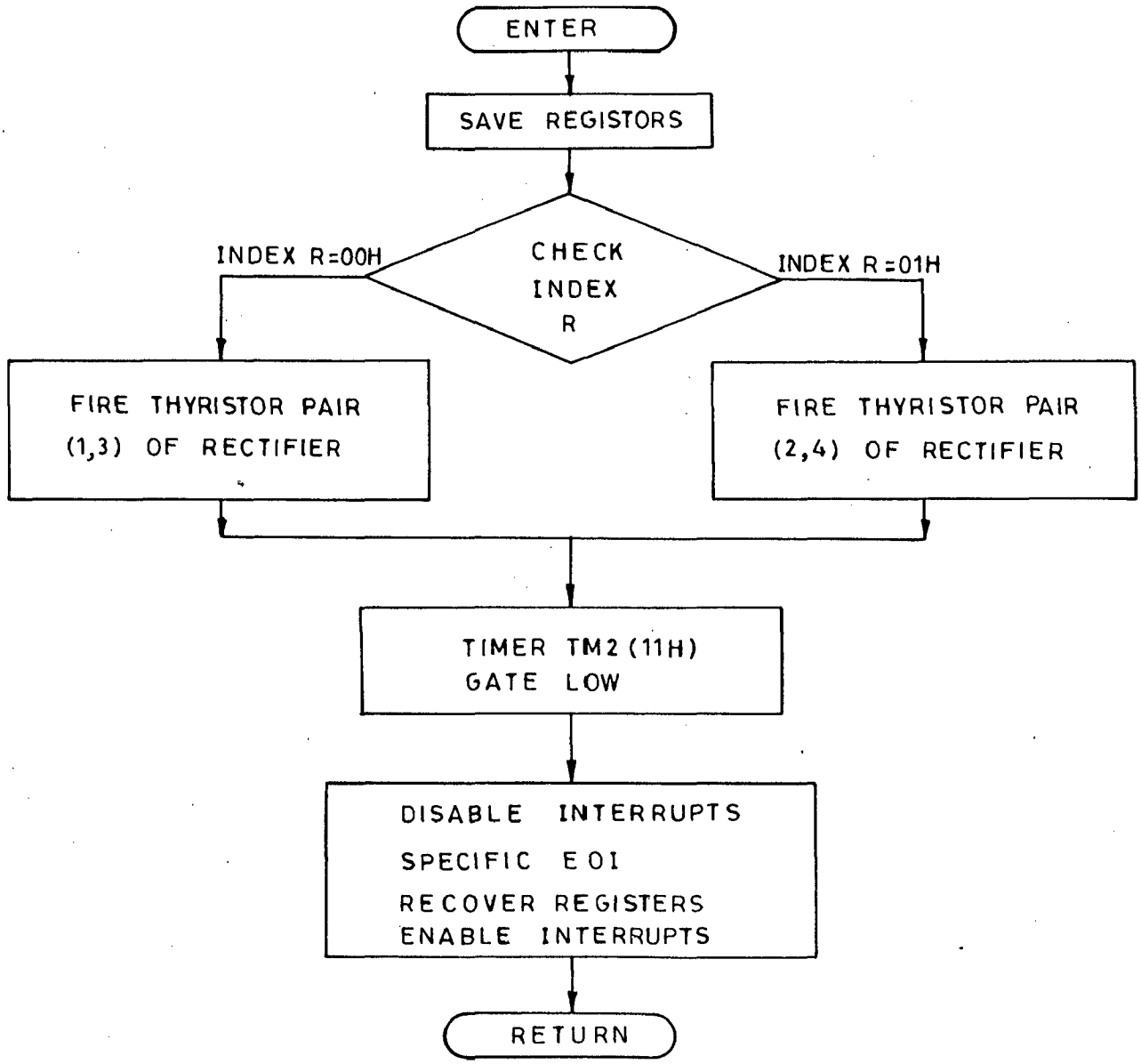


FIG. 3.6—FLOW CHART OF IR_1 · INTERRUPT SUBROUTINE

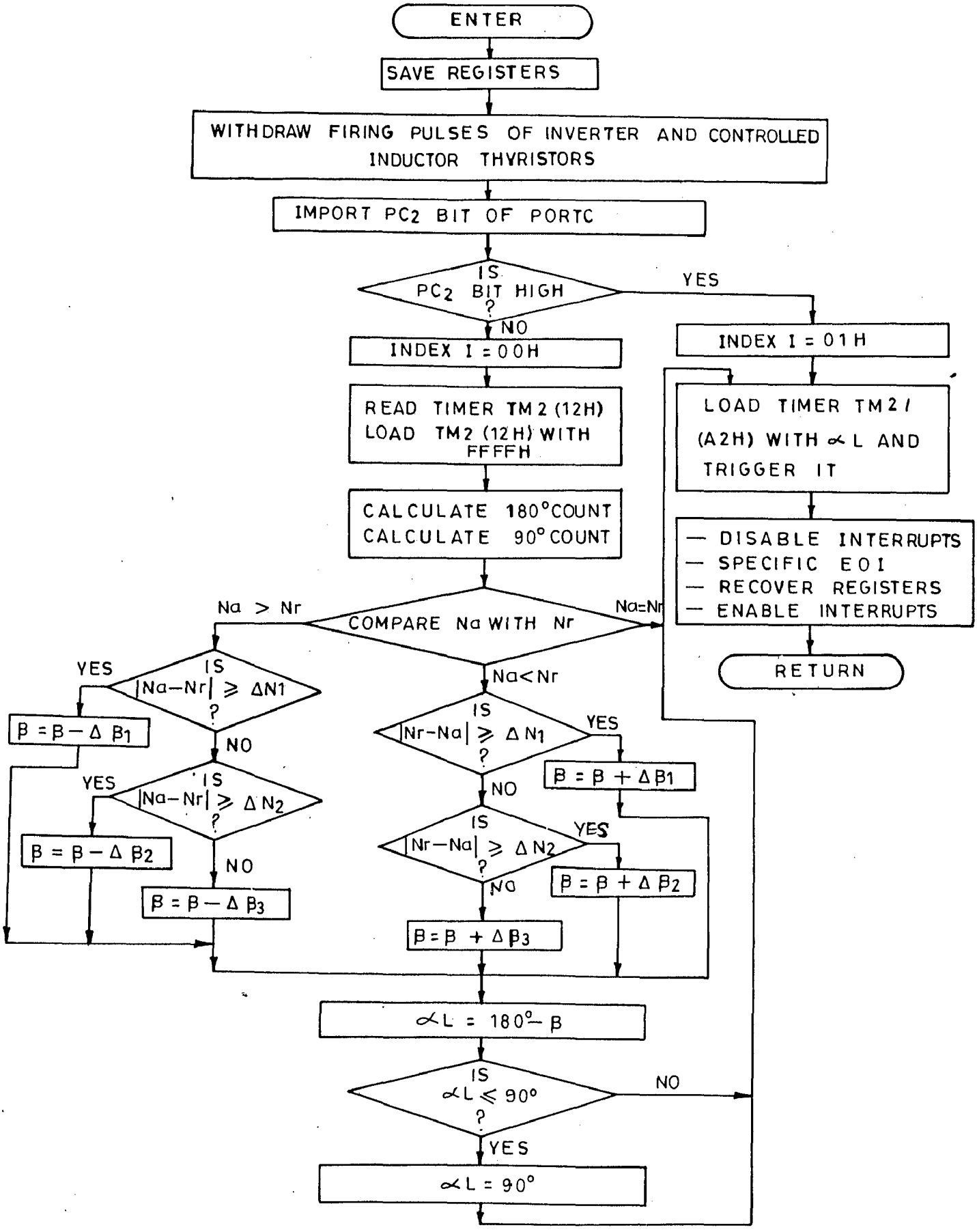


FIG. 3·7—FLOW CHART OF IR_2 INTERRUPT SUBROUTINE

according to the difference between the actual and reference speed. If this difference is large, then change in B is taken more and vice versa. Now this B is subtracted from 180 deg count to calculate firing angle count (CX L) for thyristors of controlled inductor.This firing angle count is checked so that it remains between 90 deg and 180 deg of inverter output ac voltage. If the status of PC2 bit is high, then the inverter index I is set to 01H. . After making decision on the basis of PC2 bit, the firing angle (count) CX L is loaded in timer TM2' (A2H) and this timer is triggered. Program returns after issuing end of interrupt command and recovering registors.

3.8 IR3 INTERRUPT SUBROUTINE

Flow-chart for this subroutine is shown in Fig.3.8. The interrupt IR3 occurs after firing angle of inverter from zero crossing of inverter output voltage signal.In this subroutine, next inverter thyristor pair is fired. Program is entered by saving registors. Inverter index I is checked. If this index is 00H, then pair (1,3) of inverter thyristors is fired. If index I is 01H then thyristor pair (2,4) is fired. Program returns after issuing end of interrupt command and recovering registors.

3.9 IR4 INTERRUPT SUBROUTINE

Fig. 3.10 shows the flow-chart of this subroutine. This IR4 interrupt occurs on terminal count of timer TM2'(A2H). Program is entered by saving registers. Index I is checked. If this index is 00H then thyristor (1) is fired. If it is 01H then thyristor (2) is fired. Timer TM2'(A2H) gate is made low, specific end of interrupt command is issued and program returns after recovering registers.

3.10 CONCLUSIONS

In this chapter, the complete system software implementation is discussed. The various subroutines, used in conjunction with main routine, are discussed. The various subroutines discussed are ADC subroutine, IR0 interrupt subroutine, IR1 interrupt subroutine, IR2 interrupt subroutine, IR3 interrupt subroutine and IR4 interrupt subroutine. The various subroutine software programs are developed and tested individually and all together Tte system has worked satisfactorily with the developed software in a microprocessor 8085 system. All the programs have worked satisfactorily with the developed hardware of the system, discussed in chapter 2. Machine language programs are given in appendix C.

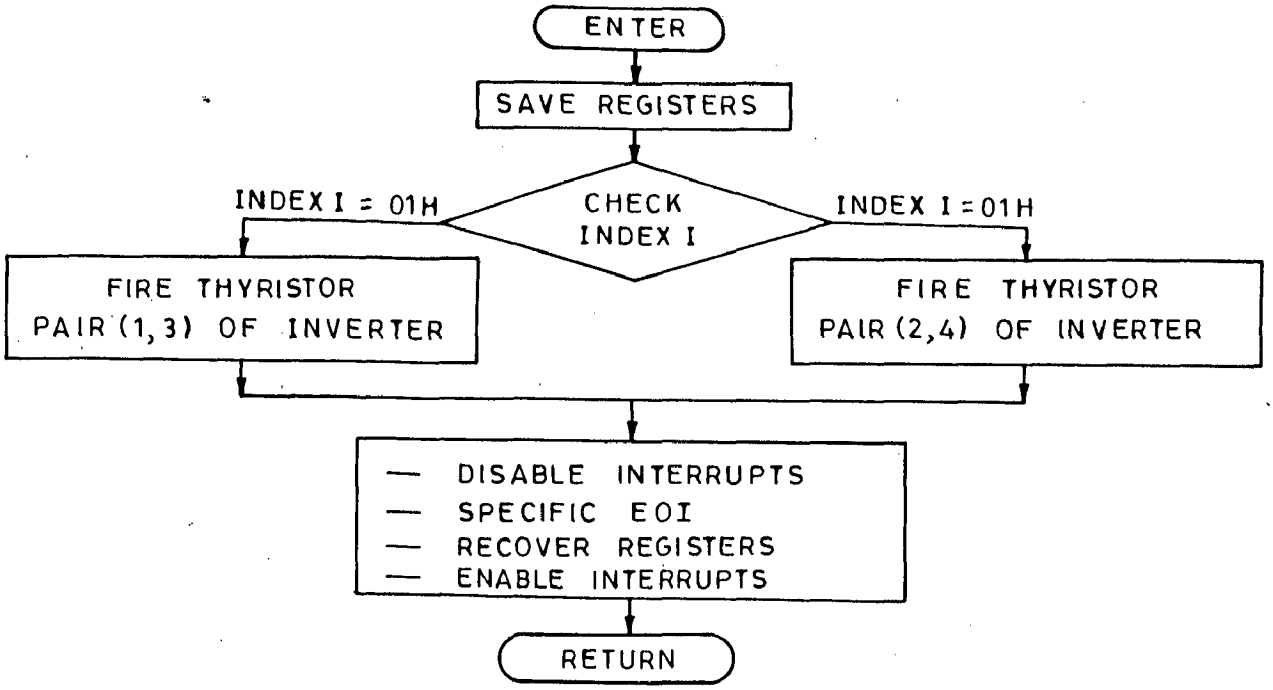


FIG. 3·8—FLOW CHART OF IR_3 INTERRUPT SUBROUTINE

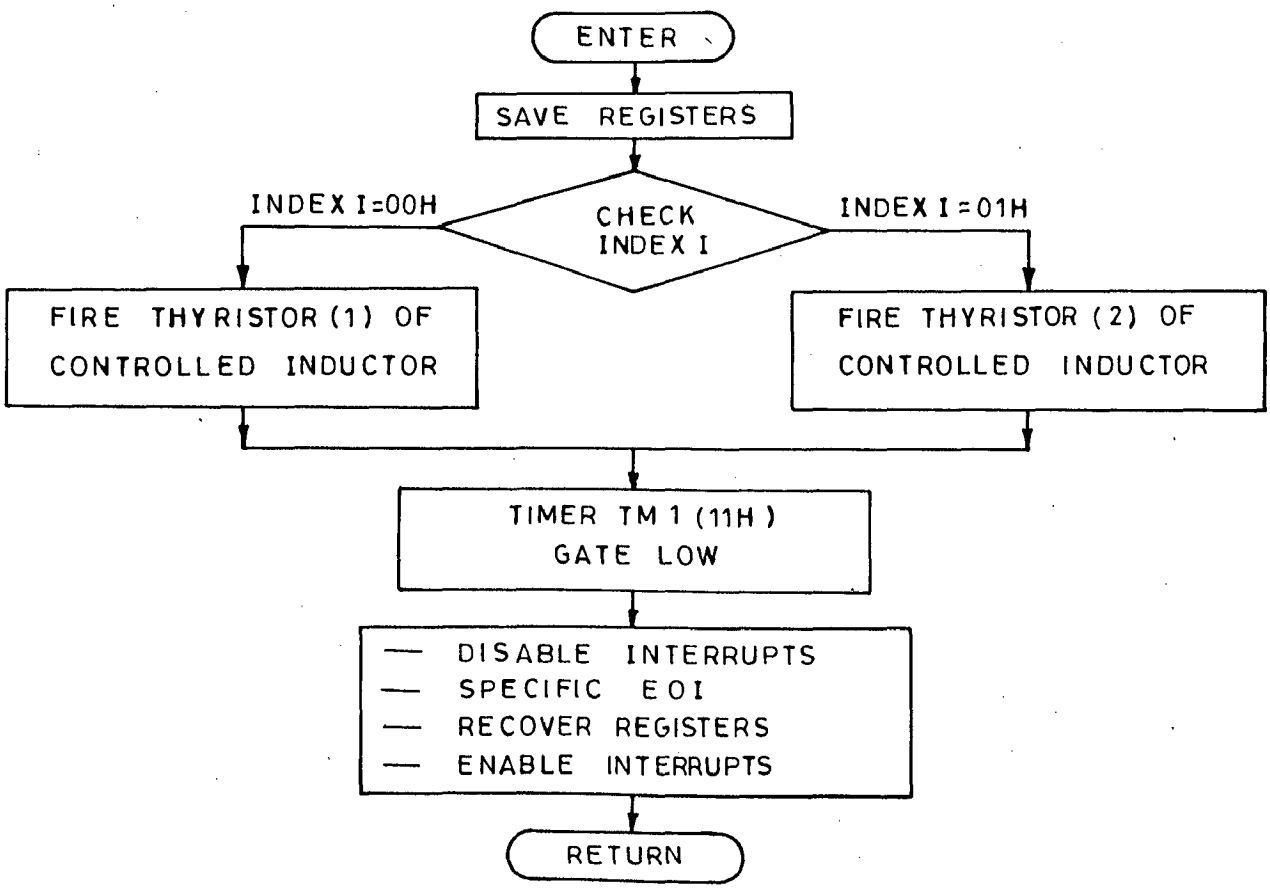


FIG. 3·9—FLOW CHART OF IR_4 INTERRUPT SUBROUTINE

CHAPTER 4

PERFORMANCE ANALYSIS OF THE DRIVE

4.1 GENERAL

In this chapter, an attempt is made on the steady state analysis of a single-phase induction motor drive fed from load commutated inverter. The analytical model is developed using equivalent circuit approach. The steady state performance of the motor is computed using developed algorithm based on proposed analytical model. The model is valid for no load as well as loaded condition of the motor. At no load, the effect of variation of terminal capacitor on speed motor current and no load loss of the motor is studied. Steady state performance of the drive, at load, is presented in terms of efficiency , speed, power factor and currents with respect to output power. The corresponding experimental results on the test motor (details are given in appendix-A) are presented along with computed results to justify the validity of developed model.

4.2 THEORY

An analytical model is developed to obtain steady state performance of load commutated inverter fed single-phase induction motor drive. Performance is computated for open loop system. In open loop system, speed of the motor is controlled by varying terminal capacitor value. The analytical model is developed by making active and reactive power balance using equivalent circuit of single-phase induction motor.

For simplifying the analysis, the following assumptions are taken:-

(i) The forward drop of thyristors and their circuit losses are neglected.

(ii) The effect of space and time harmonics are neglected.

(iii Leakage inductances and resistances of motor windings are assumed constant.

(iv) The losses in capacitor are neglected.

(v) No load losses excluding copper losses (Core loss + Friction and winding loss) of motor are assumed constant.

(vi) The overlap angle of converter is neglected.

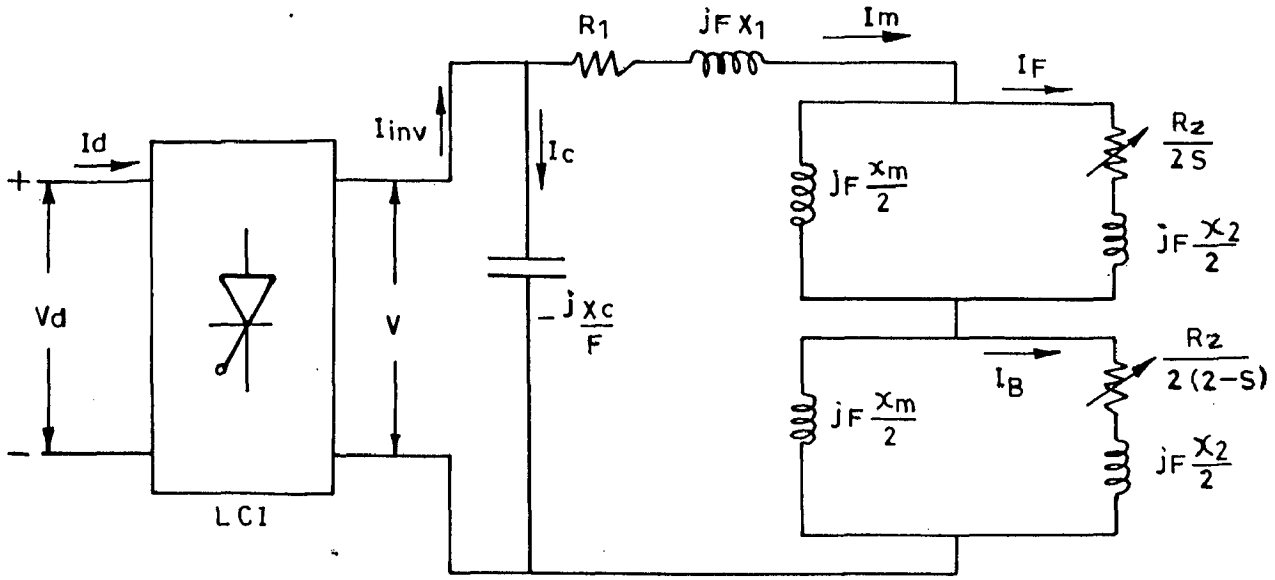


FIG. 4·1—EQUIVALENT CIRCUIT OF LCI FED SINGLE PHASE INDUCTION MOTOR DRIVE

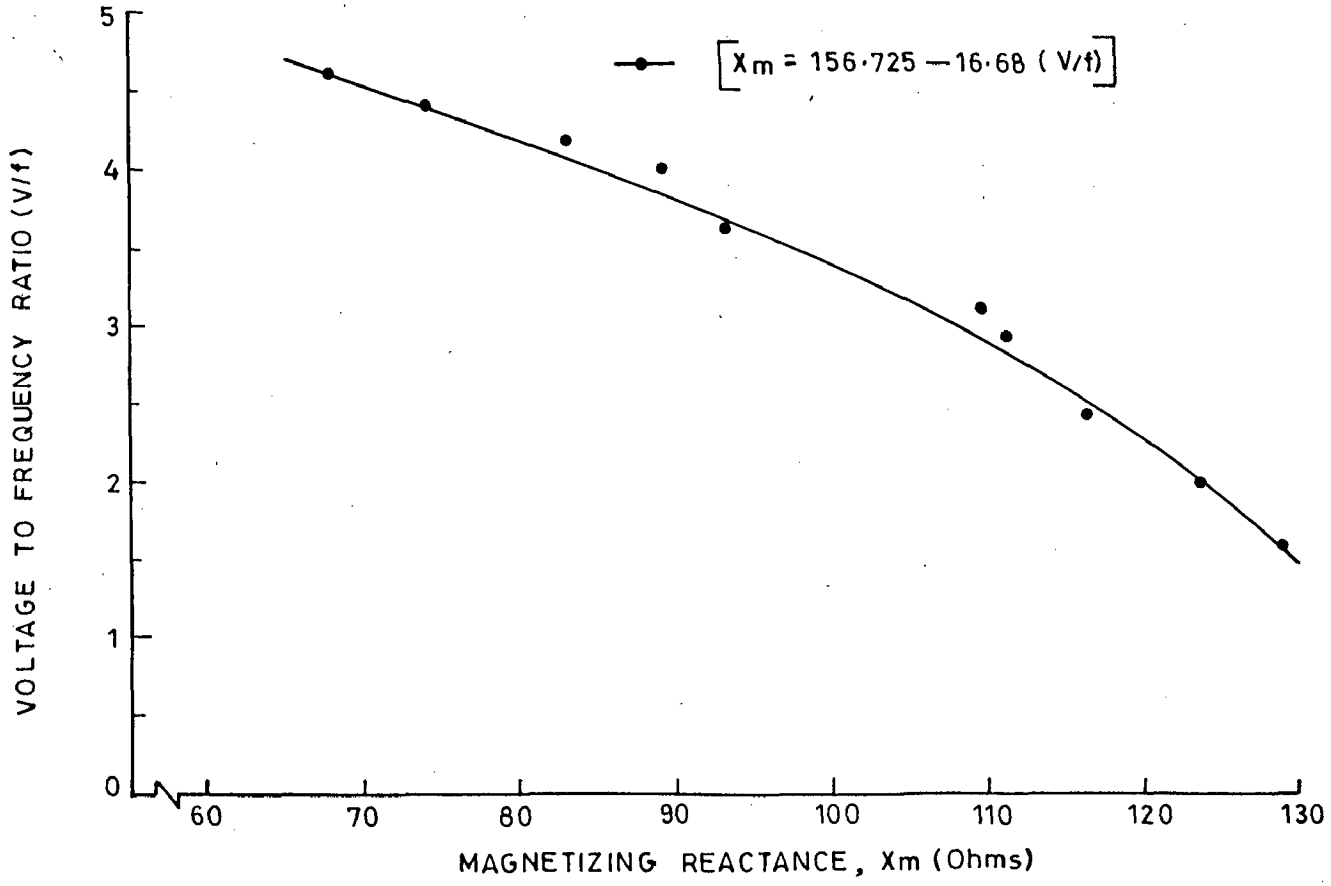


FIG. 4·2—VARIATION OF MAGNETIZING REACTANCE (Xm) WITH VOLTAGE TO FREQUENCY RATIO (V/f)

Analytical Model:-

Fig. 4.1 shows the equivalent circuit of the system at any per unit frequency "F" and slip "S" . In this equivalent circuit for a given capacitace "C" (Xc reactance at rated frequency), the p.u. frequency F is the unknown variable to be determined. The magnetising reactance (Xm) depends upon the voltage to frequency ratio (v/f). The core loss of the motor decrease with increase in frequency of terminal voltage but friction and windage loss of motor increases, therefore, no load losses (core loss + F&W loss) can be assumed to remain constant over wide range of speed (frequency). For obtaining magnetizing reactance (Xm) and constant losses , no load test on the motor is carried out at rated frequency (i.e. p.u. frequency, F = 1.0) and at various values of supply voltage. The variation of Xm with voltage to frequency ratio (v/f) is obtained using experimental data and is shown in Fig. 4.2. For simplifying the analysis, Xm is linearised in the functional form as

$$Xm = Ak0 - Ak1(v/f) \quad \text{---------- (4.1)}$$

where Ak0 and Ak1 are constants

From Fig. 4.2, the other parameters referred to stator are

stator independence $Zs = R1 + jF*X1 = Zsr + jZsi$

where $Zsr = R1$; $Zsi = F*X1$ ----------(4.2)

Rotor forward impedence $Zf' = R2/(2s) + jF*X2/2$

Rotor backward impedence $Zb' = R2/[(2 - S) 2] + jF*X2/2$

$$Zf = (jF*Xm/2) \;//\; (R2/(2S) + jF*X2/2) = Zfr + Zfi$$

where $Zfr = F**2*R2*Xm**2/[(2S)\ ((R2/S)**2 + F**2(X2 + Xm)**2)]$ ---(4.3a)

and $Zfi = F*Xm[(R2/S)**2 + F**2 * X2(X2 + Xm)]/[2((R2/S)^2 + F^2(X2 + Xm))]$ ----------(4.3b)

$$Zb = (jF*Xm/2) \;//\; [R2/(2(2 - S)) + jF*X2/2] = Zbr + Zbi$$

where $Zbr = F^2*R2*Xm^2/[2(2 - S)\ ((R2/(2 - S))^2 + F^2(X2 + Xm)^2)]$ ---(4.4a)

and $Zbi = F*Xm[((R2/(2 - S))^2 + F^2*X2(X2 + Xm)]/[2((R2/(2 - S))^2 + F^2(X2 + Xm)^2)]$ ----------(4.4b)

Let $Z = Zs + Zb + Zf = Zr + jZi$

$$Zr = Zsr + Zfr + Zbr \text{----------(4.5a)}$$

$$Zi = Zsi + Zfi + Zbi \text{----------(4.5b)}$$

$$Z = (Zr^2 + Zi^2)^{.5},\ \cos\phi = Zr/Z,\ \sin\phi = Zi/Z \text{-------(4.6)}$$

To obtain an expression being function of frequency (F) the active and reactive power balance of the system is considered.

(i) Active power balance

Power supplied by inverter Pi = V*Iinv*Cos(Y)

Y is angle of advance of inverter.

Power required for the motor Pm = V*Im*Cosø
= V**2*Cosø/Z

Constant losses = WRO

Equating active power supplied to the consumed value,

V*Iinv*Cos(Y) = V**2*Cosø/Z + WRO----------(4.7)

(ii) Reactive power balance

Reactive power needed for inverter,

Qi = V*Iinv*Sin(Y)

Reactive power required by motor,

Qm = V*Im*Sin(ø) = V**2*Sinø/Z

Reactive power supplied by capacitor,

Qc = V**2*F/Xc

Equating reactive power supplied by capacitor to required reactive power for motor and inverter

V**2*F/Xc = V**2*Sinø/Z + V*Iinv*Sin(Y)--------(4.8)

Eliminating Iinv in equations (4.7) and (4.8),

Tan(Y) = (F*V**2/Xc-V**2*Sinø/Z)/(V**2*Cosø/Z + WRO)--
(4.9)

This is simplified to get

G(F) = V**2[Cosø*Tan(Y) + Sinø]/Z + WRO*Tan(Y) - F*V**2/Xc--
(4.10)

The function G(F) must be ideally zero. It is a nonlinear

function of p.u. frequency F for the given value of terminal voltage (V), inverter angle of advance (Y), capacitance (Xc) and slip (S). The p.u. frequency F is obtained by minimizing function G(F) using single variable optimazation technique [22]. After finding p.u. frequency F, performance is calculated using equivalent circuit as follows

Motor current Im = V/Z----(4.11a)

Forward component of rotor current

If = Im*F*Xm/[((R2/S)**2 + F**2(X2 + Xm)**2)**.5]---(4.11b)

Backward component of rotor current

Ib = Im*F*Xm/[((R2/(2-S))**2 + F**2(X2 + Xm)**2)**.5]--(4.11c)

Forward airgap power Pgf = If**2*R2/(2S)

Backward airgap power Pgb = Ib**2*R2/[2(2-S)]

Resultant airgap power Pg = Pgf - Pgb------(4.12)

Synchronous speed in RPM Ns = 30fb*F, -------(4.13)

where fb is base frequency (50Hz)

Rotor speed in RPM N = Ns(1-S), --------(4.14)

Rotor cupper loss Plcur = S Pgf + (2-S) Pgb

Stator cupper loss Plcus = Im**2R1

Total cupper loss Plcu = Plcur + Plcus

Total power loss Pl = Plcu + WRO

Output power PO = Pg-WRO-Plcur

Input power Pin = PO + Pl

Motor efficiency in percentage ηm = (PO/Pin)*100

Motor power factor pfm = Pin/(V*Im)

Frequency fs = fb*F

4.3 COMPUTATION OF PERFORMANCE

The equations presented in section 4.2 for single-phase induction motor drive fed from LCI are complex. Here a general computer algorithm is developed for no load as well as loaded

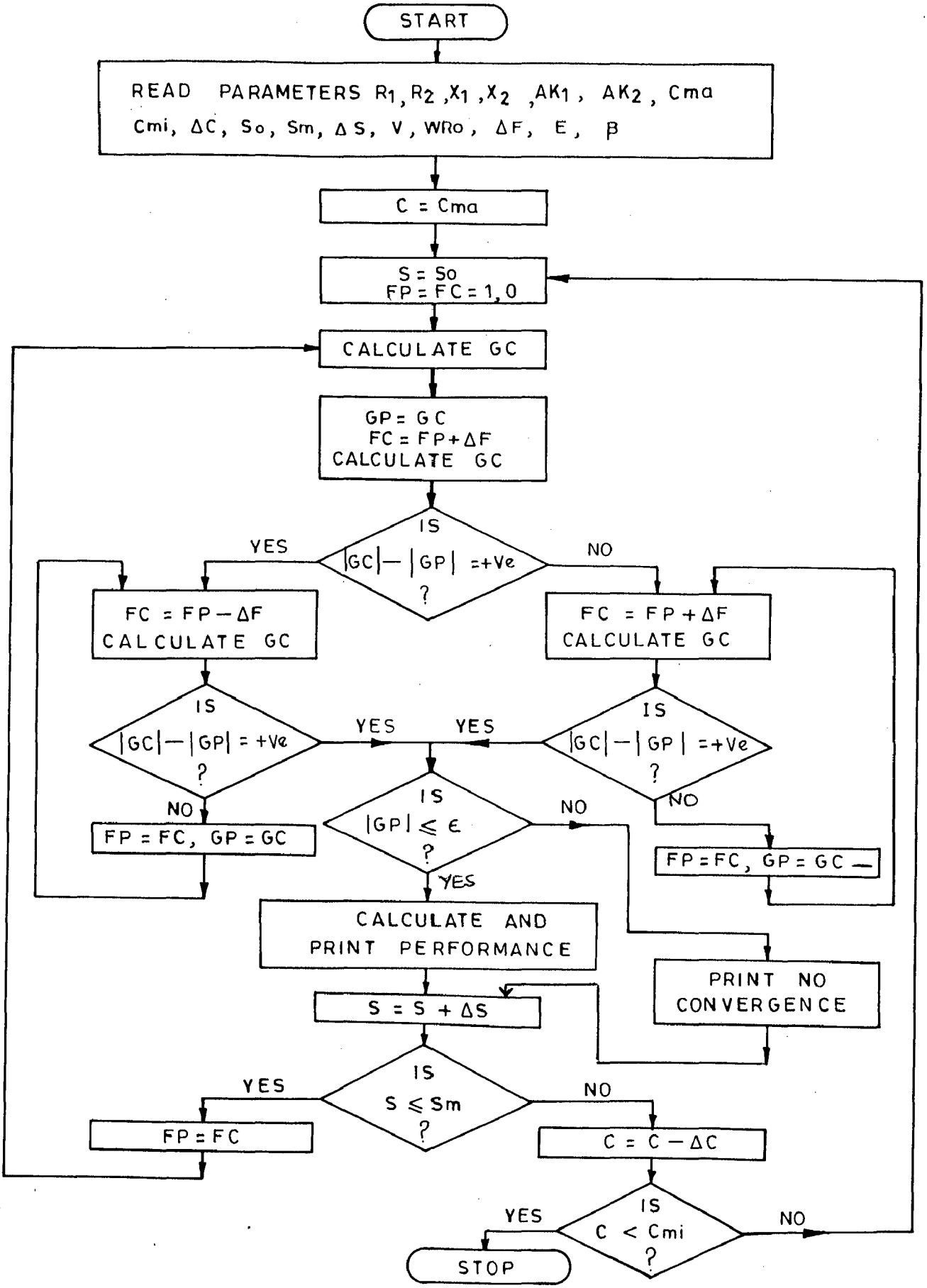


FIG. 4·3—FLOW CHART OF COMPUTER PROGRAM

conditions of the motor. The flow chart of computer program is shown in Fig. 4.3. At the starting of the program required parameters are read and initial value of capacitor (C) is taken equal to maximum value (Cmax). Initial slip is taken equal to no load slip (So). The p.u. frequency F is named for two values , current per unit frequency [FC] and previous p.u. frequency [FP], both are initialized equal to unity. Now power balance function G(F) is calculated. For FC it is defined as GC and for FP as GP. GP is taken equal to GC. Now FC is obtained by adding a small amount dF in previous frequency FP and again GC is calculated. Now magnitude of GC and GP are compared. If mod GC > mod GP then search for F is made in lower side of FP otherwise search is made on higher side of FP by decreasing or increasing current value of p.u. frequency respectively. When function G(F) is minimized and its value mod GP is found less than a small specified quantity ϵ, then performance is calculated taking p.u. frequency F as FP. Now slip (S) is increased by a small amount dS and function G(F) is minimized in similar way as described above. When slip (S) becomes equal to its given limit Sm (slip for maximum torque), then new capacitance value is taken by decreasing C by an amount dC and function G(F) is minimized for slip varying from So to Sm. Capacitance is varied from its maximum value (Cmax) to its minimum value (Cmin). After performing computation for all values of capacitor, C (Cmin $\leq$ C $\leq$ Cmax) execution of program stops. The computed performance of motor under no load and loaded conditions are given in Fig. 4.4 and Fig. 4.5 respectively.

4.4 EXPERIMENTATION

The steady state performance of the drive motor is also obtained experimentally by performing various tests on open loop system for the value of capacitor considered in computation of performance . The experimental results are presented along with computed results to justify the validity of computer algorithm based on developed analytical model. The no load computed results along with experimental tests points are shown in Fig. 4.4. Motor performance at load is given in Fig. 4.5 in terms of speed, motor current, power factor and efficiency.

4.5 DISCUSSIONS OF RESULTS

Fig. 4.4 shows the no load characteristics of the motor, both computed and experimental at rated terminal voltage. It may be observed from Fig. 4.4a that no load speed of the motor varies with change in capacitor value. Motor speed increases with the decrease in capacitor value and vice versa. Variation in speed are more for lower values of capacitor. Speed is nearly equal to rated speed for capacitor value of 75 uf. Fig. 4.4b shows the variation in motor current and input power at no load. It may be observed that both no load curret and input power decrease with increasing speed due to reduction in magnetizing current. It may

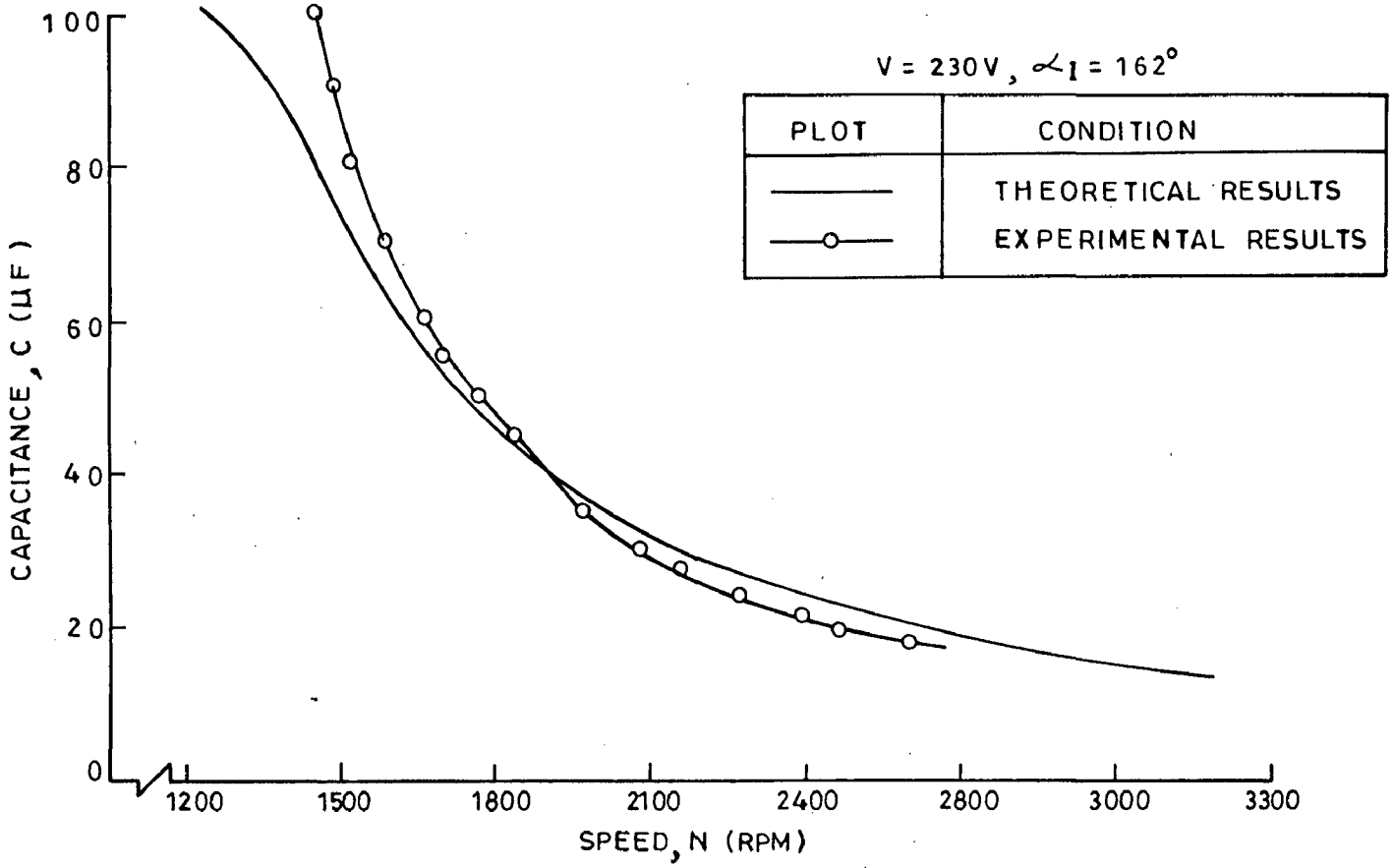


FIG. 4·4(a)—VARIATION OF CAPACITANCE WITH SPEED AT NO LOAD

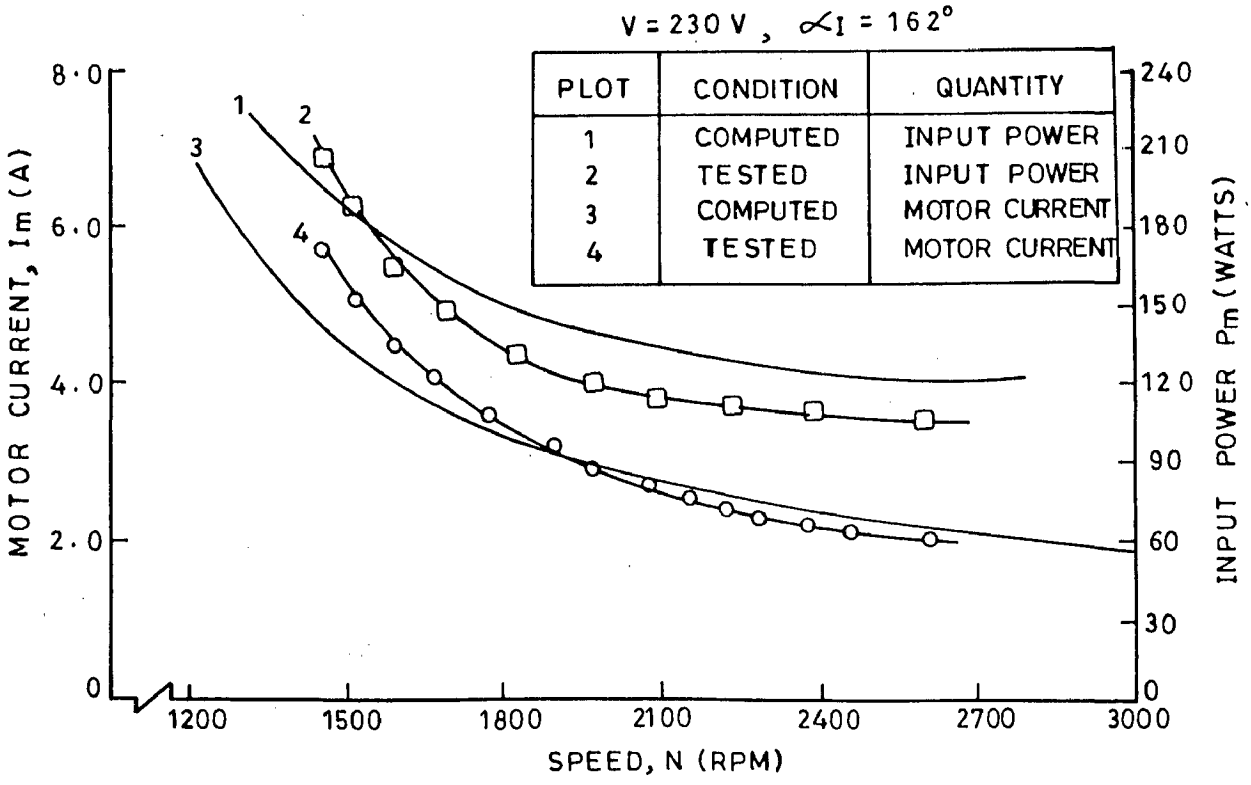


FIG. 4·4(b)—VARIATION OF MOTOR CURRENT AND INPUT POWER WITH SPEED AT NO LOAD

also be observed from Fig. 4.4 that the computed results show good correlation with experimental one, thus establishing the validity of model for no load operation of motor. A little deviation in the results may be observed from Fig. 4.4 and it is because the capacitor is not ideal and its effective value may be different from the value considered in computation. Further, the harmonics are neglected in computation while harmonics are always present in a real system.

Fig. 4.5a shows the output power vs speed characteristics for different values of capacitor at rated terminal voltage of motor. It is observed that speed rises with the rise in output power. This rise in speed is greater for lower values of capacitor. For higher values of capacitor (more than 70 μf) the speed decreases with the increasing output power as evident from experimental results. Computed results show that motor speed rises for all values of capacitor with increasing output power. It is due to increased requirement of reactive power in the motor at load and which may only be met by increasing the frequency at constant voltage for particular value of terminal capacitor. The reason for fall in speed with load for higher value of capacitor (at lower speed) is that the magnetic circuit of motor is saturated. When load is increased, drop in stator impedence increases due to which the magnetizing current decreases nonlinearly. This decrease in magnetizing current is more than increase in reactive component of rotor current, therefore, the resultant lagging reactive power drawn by motor decreases. Because of decreased lagging reactive power requirement of motor, frequency is decreased so that leading reactive power of capacitor (V**2*F/Xc) becomes equal to that required for motor and inverter. Fig. 4.5b shows variation of motor current with load . From this figure it may be observed that motor current decreases for higher speeds (at lower capacitor value) due to reduced magnetizing current requirement of motor. Motor current rises with rise in load . It can be noted that computed and experimental results are identical in nature. Fig. 4.5d shows the variation of motor efficiency with output power. It can be observed that the motor efficiency first increases and then decreases with increase in load. This decrease in efficiency for higher load is due to sharp increase in variable losses. The difference in experimental efficiency from computed value of efficiency is because the no load losses of motor are assumed constant. Fig.4.5c shows variation of motor power factor with load which increases with load in similar manner as that with normal supply.

It is observed that the motor could be loaded to lesser amount at higher speeds. It is due to decrease in maximum load capability of the machine because of higher values of leakage reactances of stator and rotor. It is observed practically that machine having lesser leakage reactances can be loaded more than that having larger leakage reactances. It is concluded that for such type of drive a machine having low values of leakage inductances

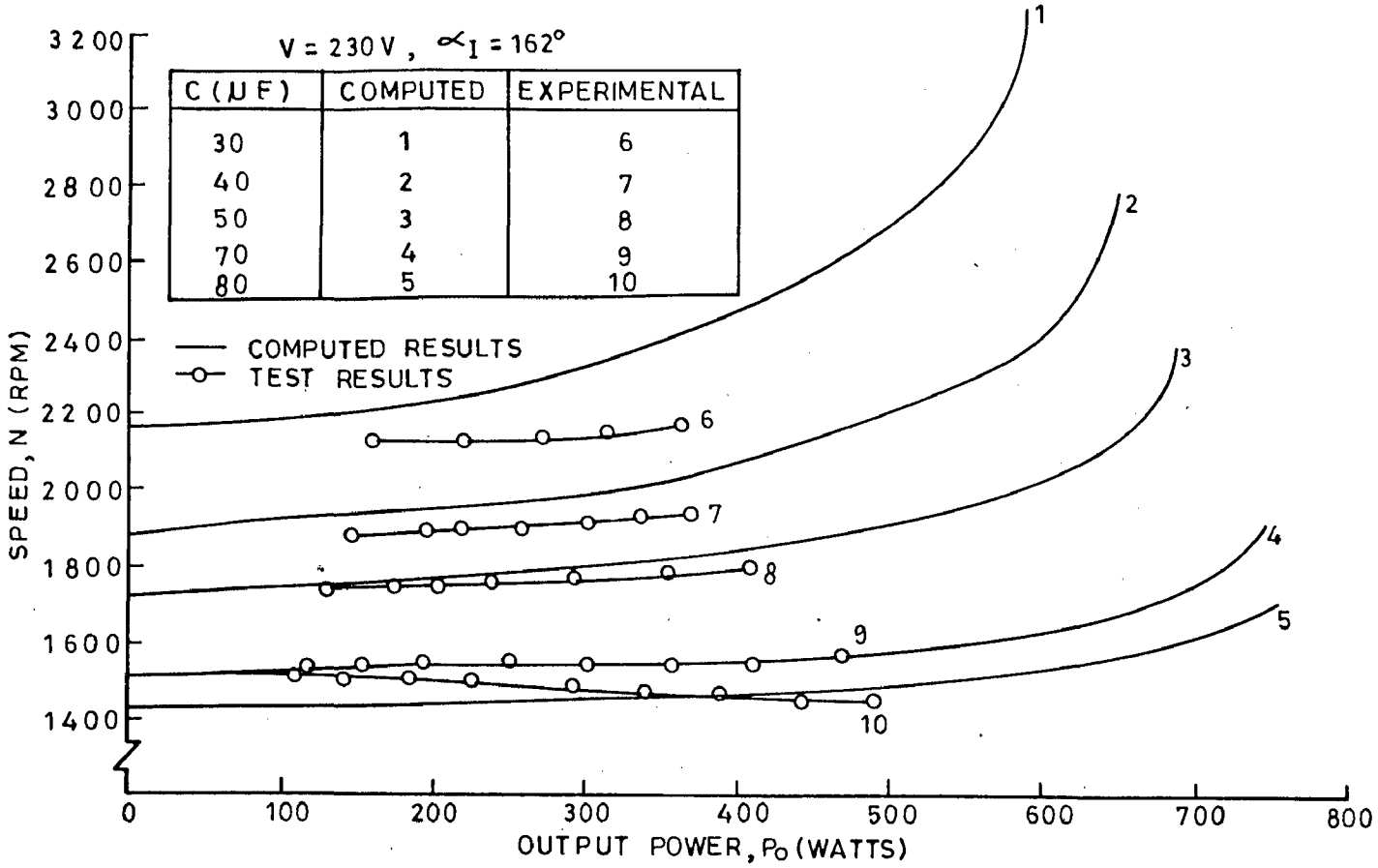


FIG. 4·5 (a)—VARIATION OF MOTOR SPEED WITH OUTPUT POWER

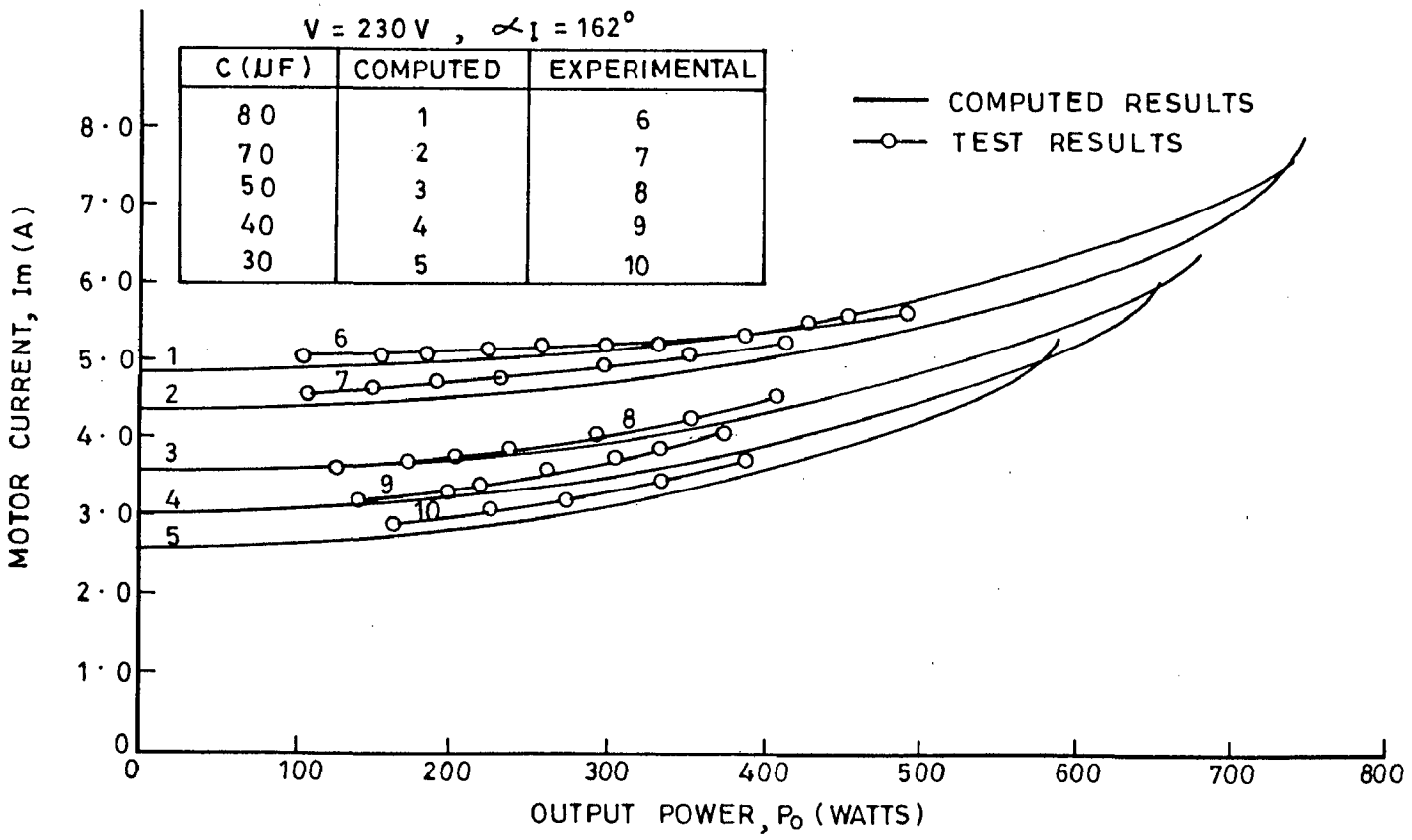


FIG. 4·5 (b)—VARIATION OF MOTOR CURRENT WITH OUTPUT POWER

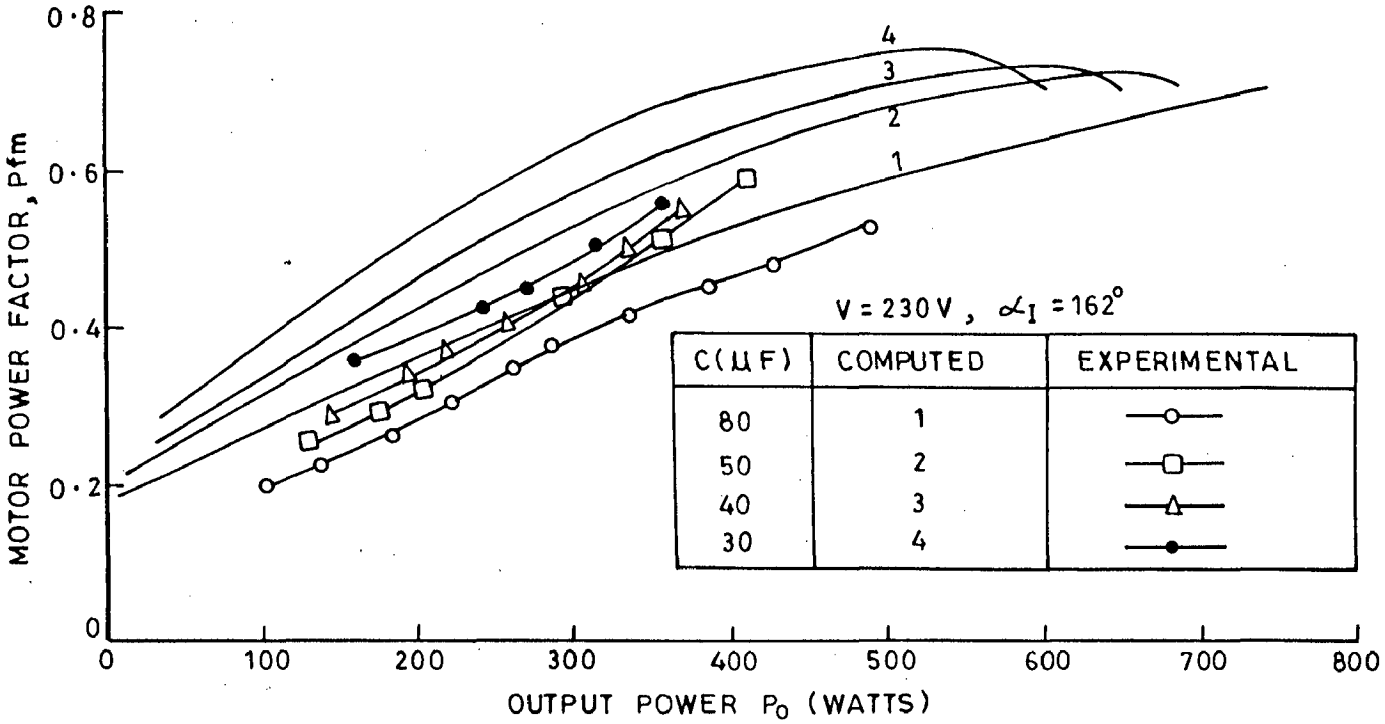


FIG. 4·5(c)–VARIATION OF MOTOR POWER FACTOR WITH OUTPUT POWER

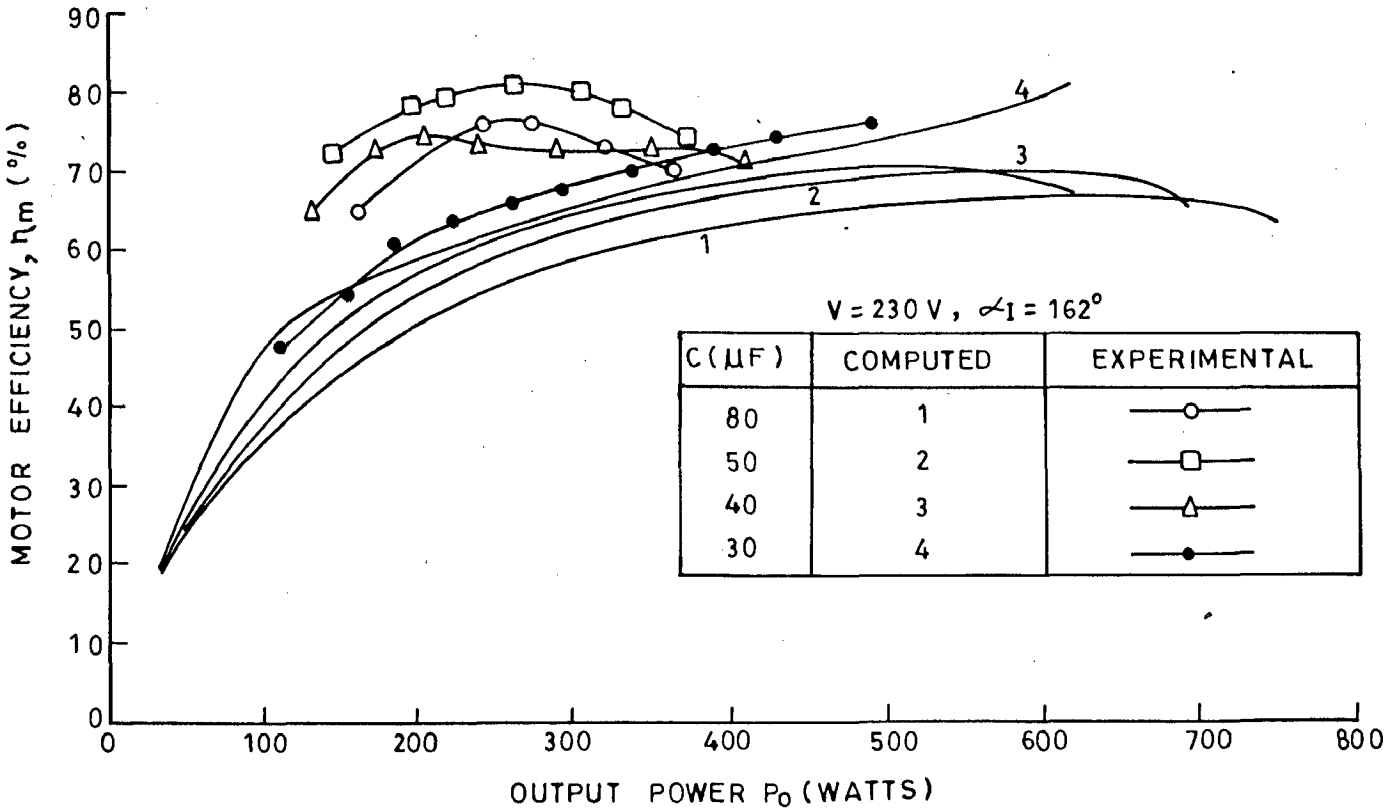


FIG. 4·5(d)–VARIATION OF MOTOR EFFICIENCY WITH OUTPUT POWER

will result in better loading capability without exceeding temperature rise of motor.

4.6 CONCLUSIONS

The performance of a variable speed, LCI fed single-phase induction motor drive with open loop control is studied. The developed analytical model for operation of motor at no load and loaded conditions, which uses equivalent circuit approach, has been found suitable for computation of performance of the drive. The test results show good corelation with computed results. Thus validating the developed model. It is concluded that load capability of motor decreases with increase in speed . It is because of large leakage inductances of motor. A machine designed for low leakage inductances will give higher output with safe temperature rise.

CHAPTER 5

PERFORMANCE OF THE CLOSED LOOP SYSTEM

5.1 GENERAL

Experimental closed loop performance of microprocessor controlled LCI fed single-phase induction motor drive is studied and compared with open loop performance of the system. The output power vs speed characteristics and performance in terms of motor efficiency, power factor and currents of motor and inverter are obtained for various speed settings in closed loop control and for different capacitor values in open loop control while maintaining the terminal voltage of motor equal to rated value. Dynamic performance of the system in open loop and closed loop control is obtained experimentally and waveforms of various control signals and system variables under dynamic condition are recorded by X-Y recorder, and discussed in detail. Oscillograms of various system variables under steady state conditions for closed loop and open loop control of the drive are presented and discussed in detail.

5.2 STARTING METHODS

As described in chapter 2, the system consists of single-phase bridge rectifier, dc link inductor, load commutated inverter, capacitor, thyristor controlled inductor and a single-phase induction motor. Fully controlled bridge rectifier provides variable dc link voltage input to bridge inverter. Since source is dc, it cannot supply lagging reactive power needed for magnetization of magnetic circuit of induction motor, therefore, induction motor cannot be started directly by this source. The capacitor connected at motor terminals is charged due to induced emf induction motor terminals and hence supplies the required reactive power for motor and inverter. This shows that if the induction motor is brought to some speed by any means so that capacitor, reactive power is enough to provide magnetization of motor and to commutate thyristors of the inverter, the system will start working and draw active power from dc sorce while reactive power from capacitor.

Following two methods can be used to start the drive.

5.2.1 Starting by a Coupled dc Motor

In this method, induction motor is brought at proper speed by a coupled dc machine operating as a motor. Terminal capacitor provides self excitation to the induction machine. As a result of this, voltage builds up at the machine terminals (working as a generator). Now power is fed to dc input of inverter, motor draws

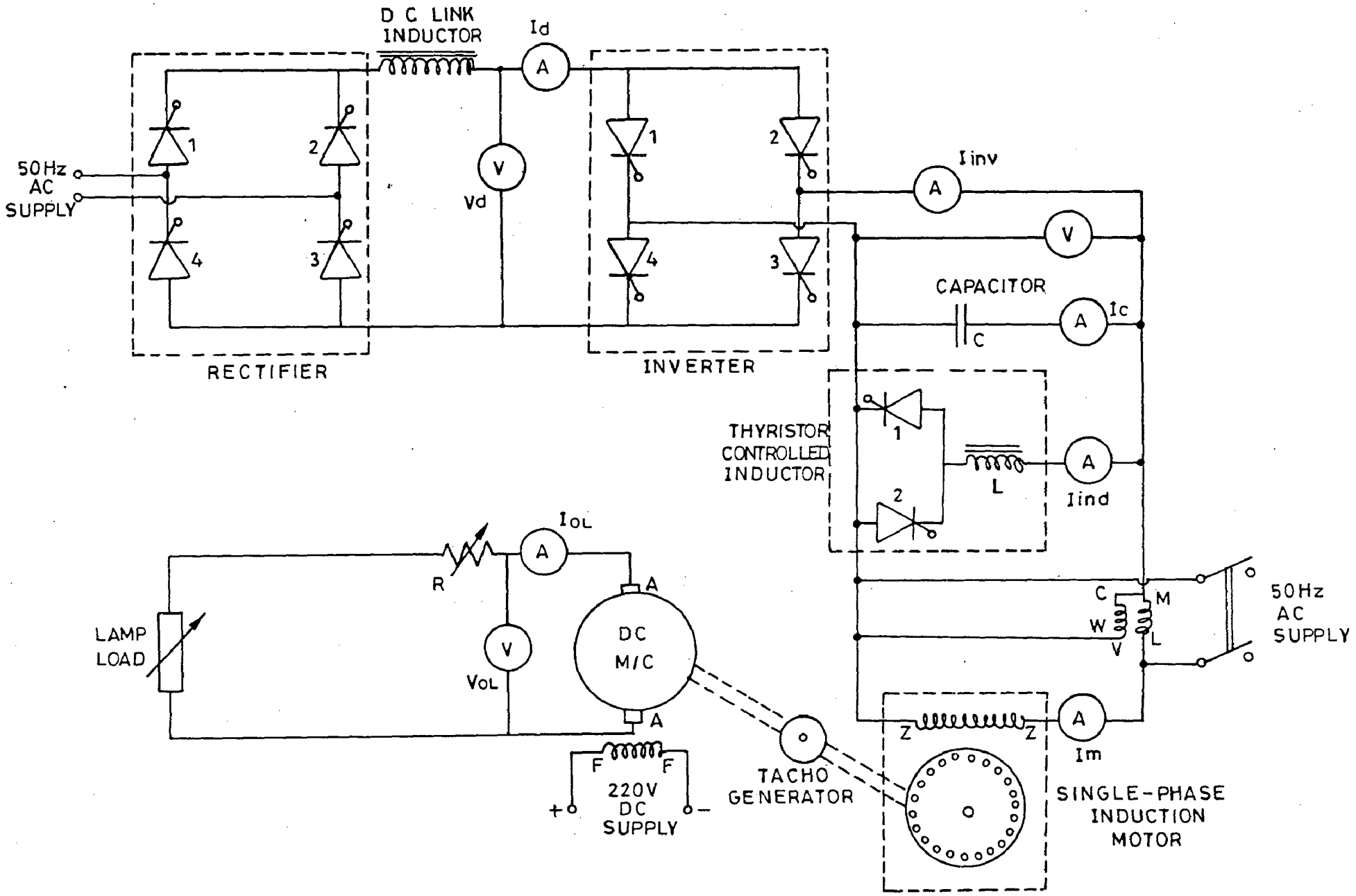


FIG. 5·1—EXPERIMENTAL SET UP OF LCI FED SINGLE-PHASE INDUCTION MOTOR DRIVE

active power from rectifier. The power fed by dc machine reduces slowly and active power drawn from rectifier increases gradually. With this the induction machine changes its mode of operation gradually from generating to motoring mode at a frequency which is set itself by system parameters. When power supplied by dc machine becomes neglible, it is disconnected from dc supply.

5.2.2 Starting by a Single Phase supply

This method is used in the present work to start single-phase induction motor. Fig.. 5.1 shows circuit diagram of the sytem to be started by this method. To start the operation of the system, first the induction motor is connected to single-phase supply (50Hz) and is brought upto no load (rated) speed. With capacitor connected across the motor terminals, dc input to inverter is given from rectifier, the power flow through inverter is established and adjusted so that power drawn from ac supply by motor is almost zero. Now ac supply (50Hz) is disconnected from motor terminals. The induction motor is continued to run taking active power from dc link through inverter and its frequency is decided by capacitor, margin angle of inverter and terminal voltage.

5.3. PERFORMANCE OF THE DRIVE

Fig. 5.1 shows the experimental setup to obtain performance of LCI fed single-phase induction motor drive. The motor is loaded by a dc machine coupled with it. The dcmachine operates as a separately excited generator. Details of motor and dc machine are given in Appendix-A.

Various tests are conducted to obtain the following performance of the drive in open loop and closed loop control.

(i) Steady state performance,

(ii) Dynamic performance, and

iii) Steady state waveforms of voltage and current of inverter, motor, capacitor and inductor.

To obtain open loop steady state performance of the drive the controlled inductor is disconnected and load tests are performed for different capacitor values. For obtaining closed loop steady state performance controlled inductor is connected in circuit and load tests are conducted for different reference speed settings. From the tests, results are taken through meters connected in the circuit shown in Fig. 5.1. The drive performance is given in terms of speed, motor current, inverter current, motor efficiency and power factor with variation of load (output power). Fig. 5.2 shows the various curves pertaining performance of the drive for the closed loop as well as open loop condition. Fig. 5.2a shows variation of motor speed with output power for

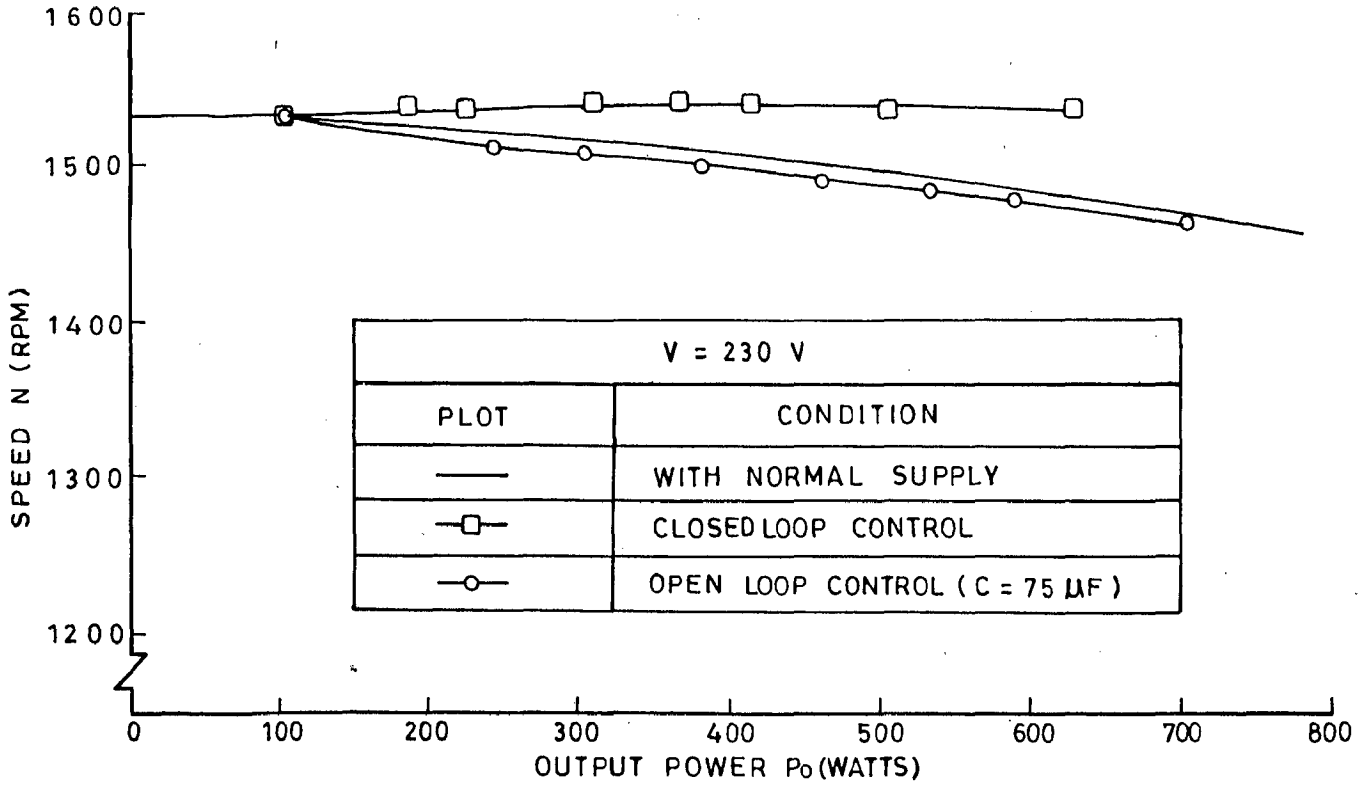


FIG. 5·2 (a)—VARIATION OF SPEED WITH OUTPUT POWER

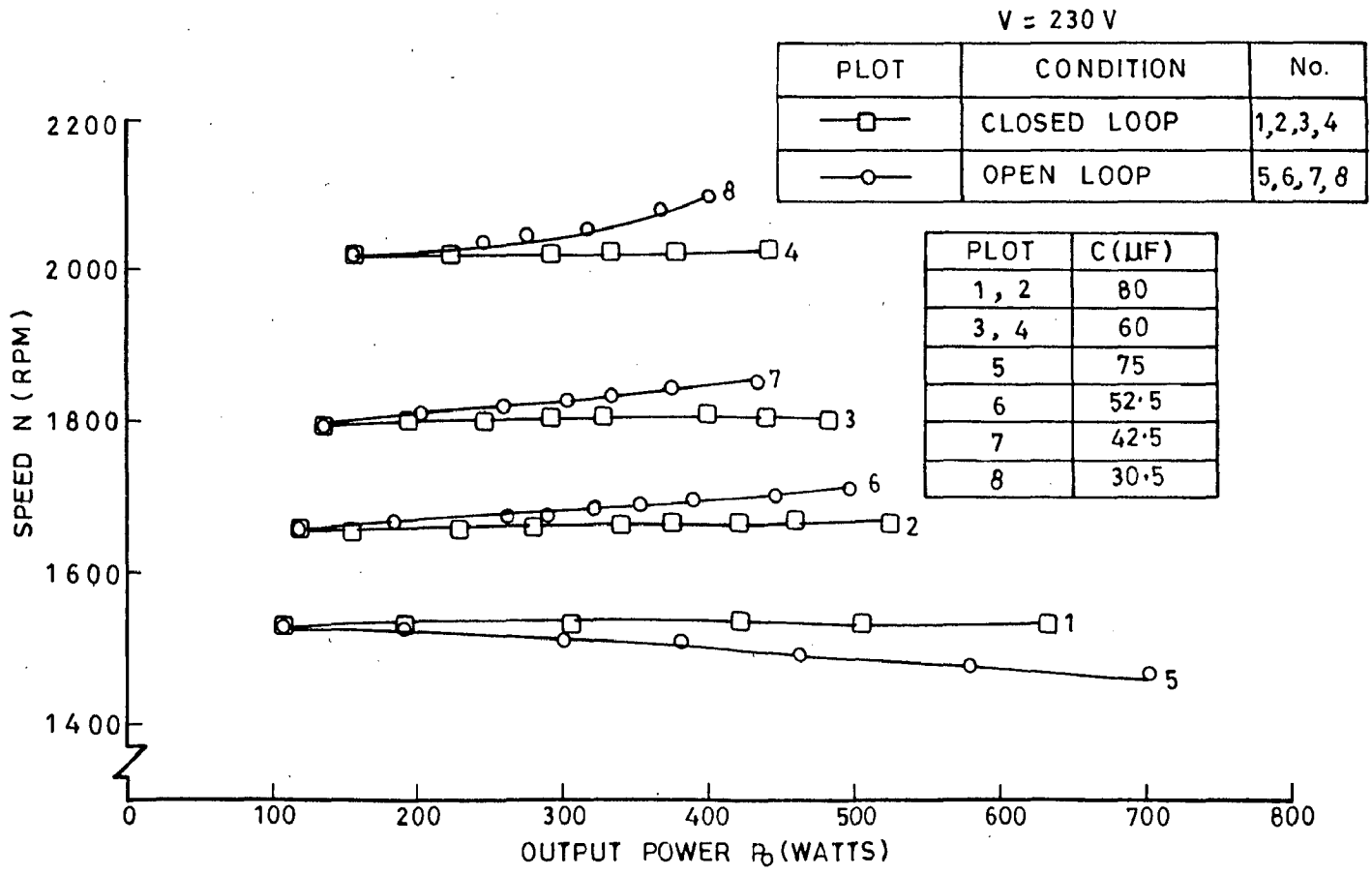


FIG. 5·2 (b)—VARIATION OF SPEED WITH OUTPUT POWER

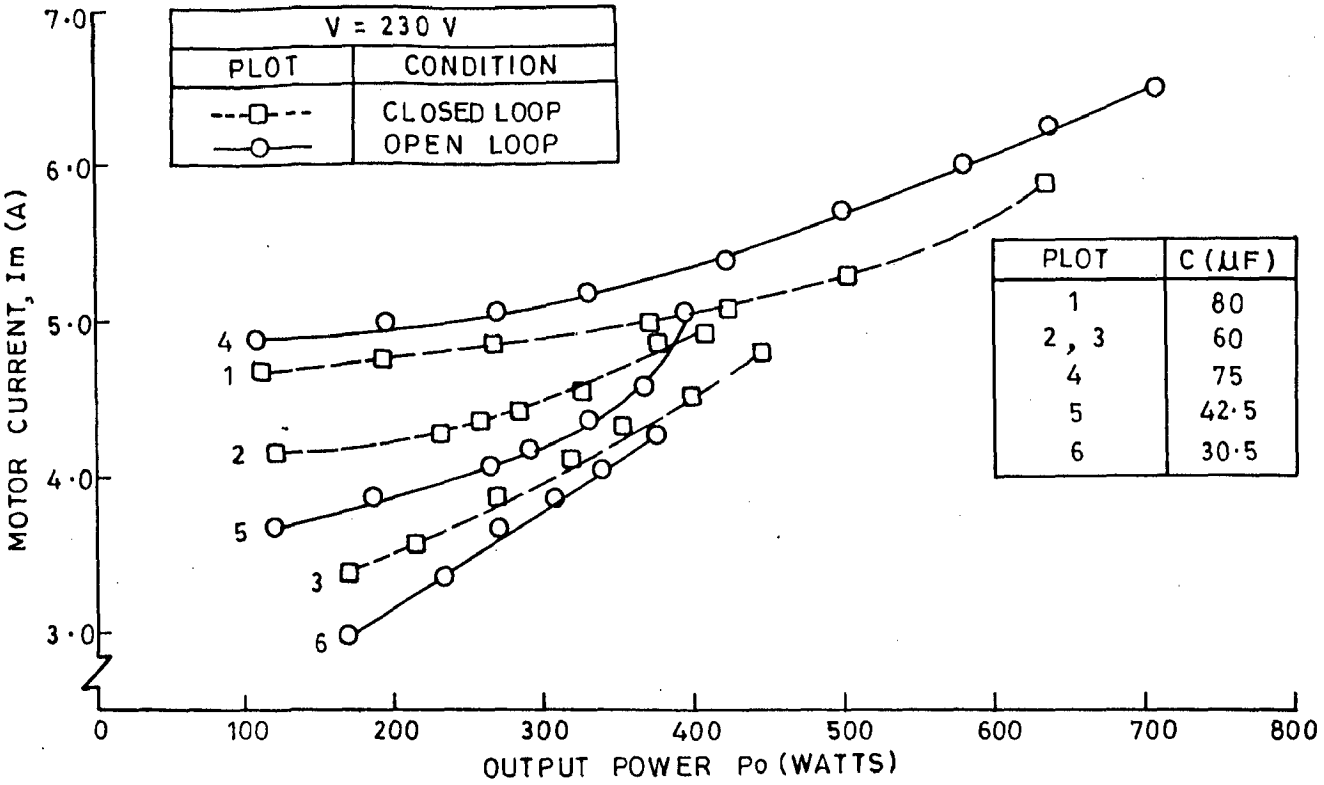


FIG. 5·2 (c)—VARIATION OF MOTOR CURRENT WITH OUTPUT POWER

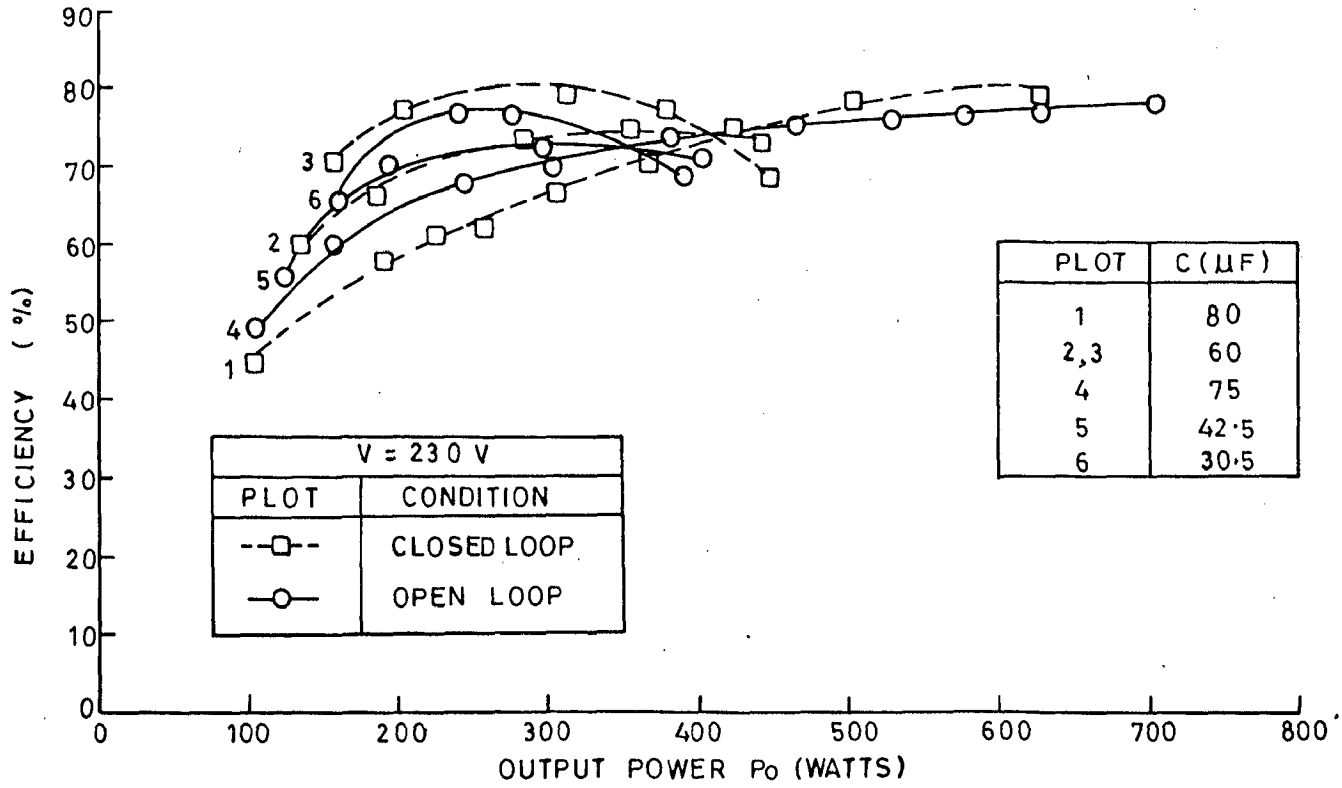


FIG. 5·2 (e)—VARIATION OF MOTOR EFFICIENCY WITH OUTPUT POWER

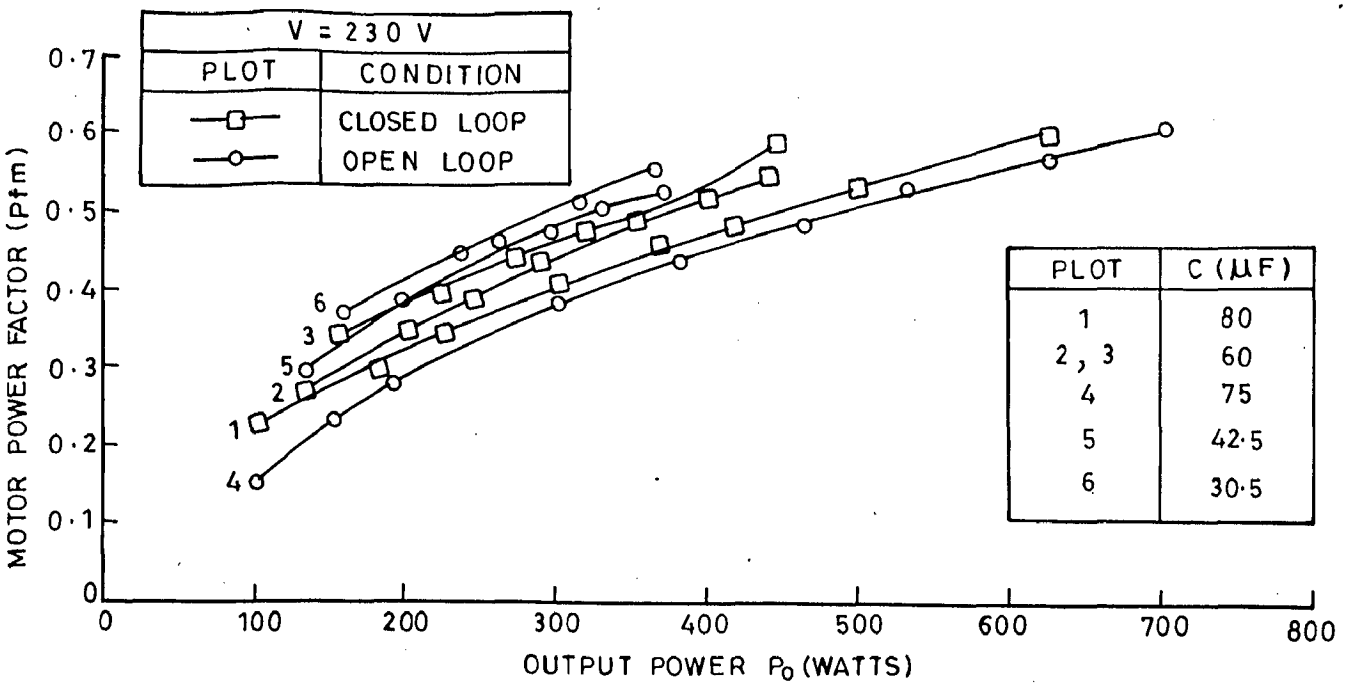


FIG. 5·2 (f)—VARIATION OF MOTOR POWER FACTOR WITH OUTPUT POWER

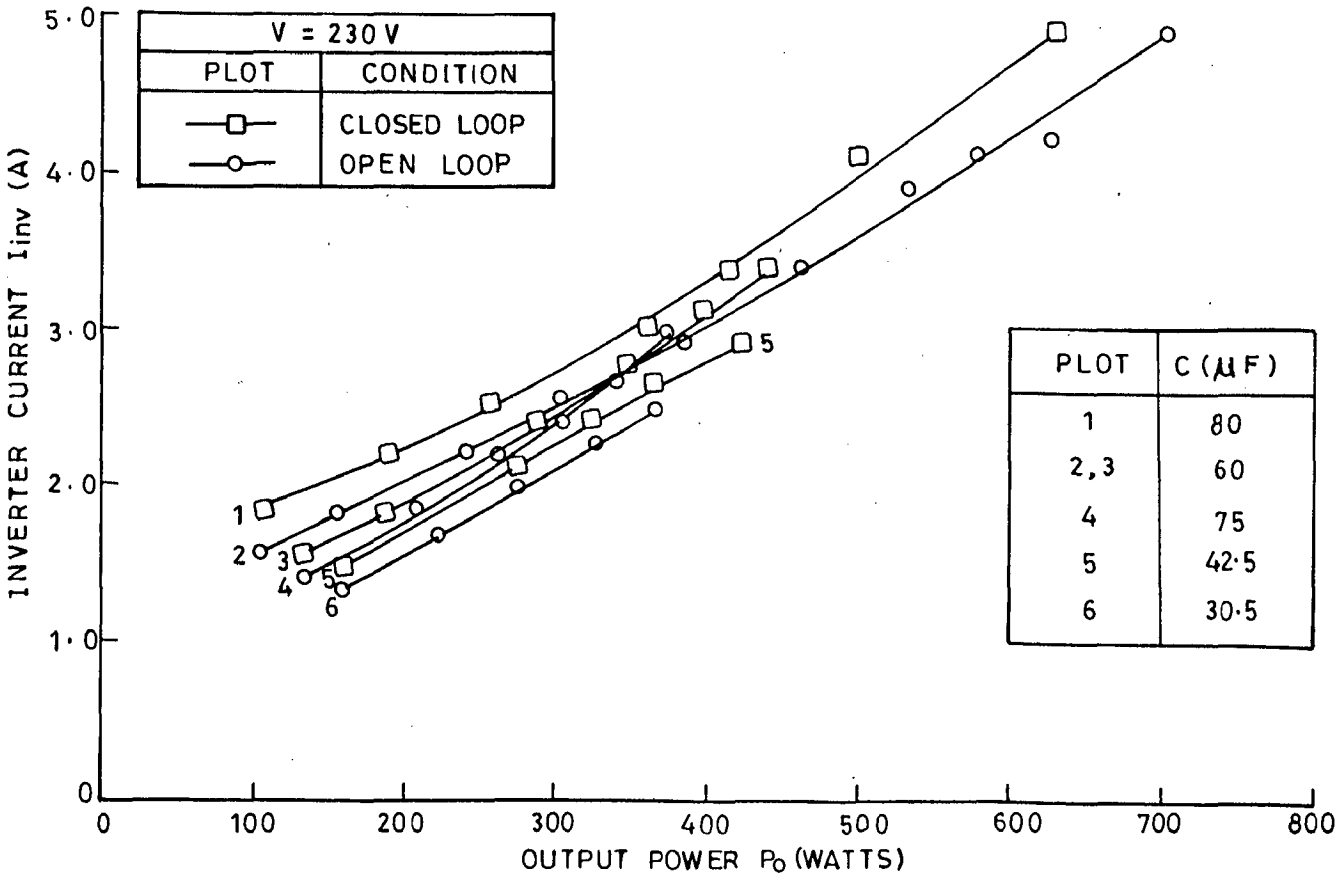


FIG. 5·2 (d)—VARIATION OF INVERTER CURRENT WITH OUTPUT POWER

three different conditions; with normal supply (50Hz), open loop and closed loop control of system. Fig. 5.2b shows variation of speed with output power for different reference speeds in closed loop control along with results of open loop control of system. Fig. 5.2c shows variation of motor current with output power for different speeds. Fig. 5.2d shows variation of inverter current with output power. Fig. 5.2e and Fig. 5.2f shows variation of motor efficiency and power factor with output power, respectively.

Dynamic performance of the drive is obtained for the following conditions:

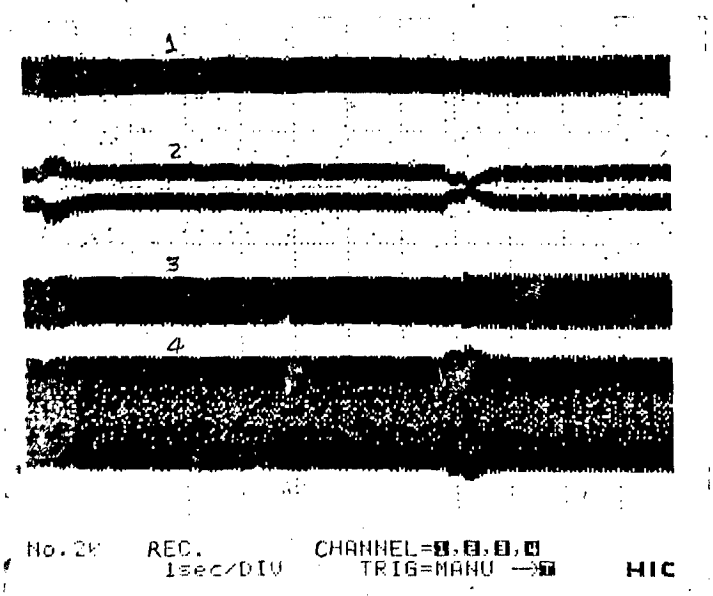
(a) Dynamic performance of the system under open loop control

(b) Dynamic performance of the system under closed loop control.

In open loop control of drive, waveforms of motor voltage, current, capacitor current, and inverter current are recorded by X-Y recorder for sudden change of capacitor value, and sudden change of load. The correspoding control circuit waveforms of speed, signal corresponding to motor terminal voltage and dc link current are also recorded. Fig. 5.3a shows the waveforms of (i) capacitor current (ii), inverter current (iii), motor current and (iv) motor terminal voltage under dynamic conditions. Fig. 5.3a,(i) shows waveforms for sudden change of capacitor value from 56μf to 40μf and again to 56μf and Fig. 5.3a,(ii) shows for a sudden change of value of capacitor from 40μf to 36μf and again to 40μf. Fig. 5.3a (iii) and (iv) show waveforms under sudden change of load for capacitor values of 56μf and 40μf respectively. Fig. 5.3b shows control circuit waveforms of (i) speed (ii) terminal voltage and (iii) dc link current for the same circuit conditions of Fig. 5.3a.

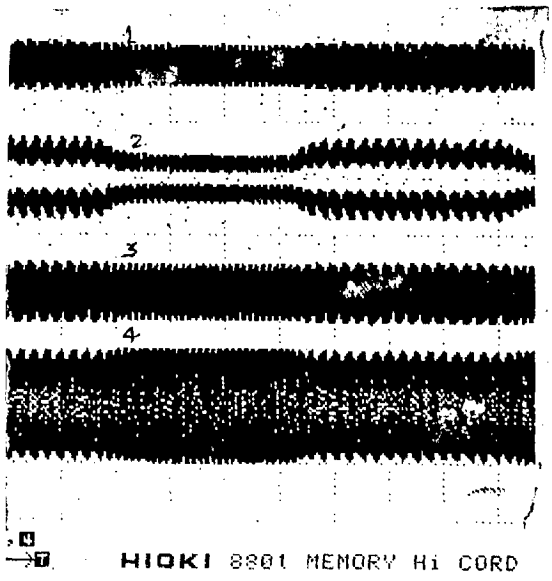
For the closed loop control of drive, waveforms of voltage and currents of motor, inverter and inductor are recorded for sudden change of load and sudden change of reference speed. The corresponding recordings are shown in Fig. 5.3c.The control circuit waveforms of reference speed, actual speed,, signal corresponding to motor voltage and dc link current are also recorded and shown in Fig.5.3d in similar circuit conditions of Fig.5.3c.

Steady state oscillograms of motor voltage and currents of inverter, motor and capacitor for open loop control of drive are recorded using digital storage cathode ray oscilloscope for no load as well as loaded condition of drive for different capacitor values (56μf and 40μf). These oscillograms are shown in Fig. 5.4a. For the closed loop control of drive, oscillograms of motor voltage and currents of inverter, motor, capacitor and controlled inductor are taken for no load as well as loaded conditions of drive for different values of reference speeds (1660RPM and



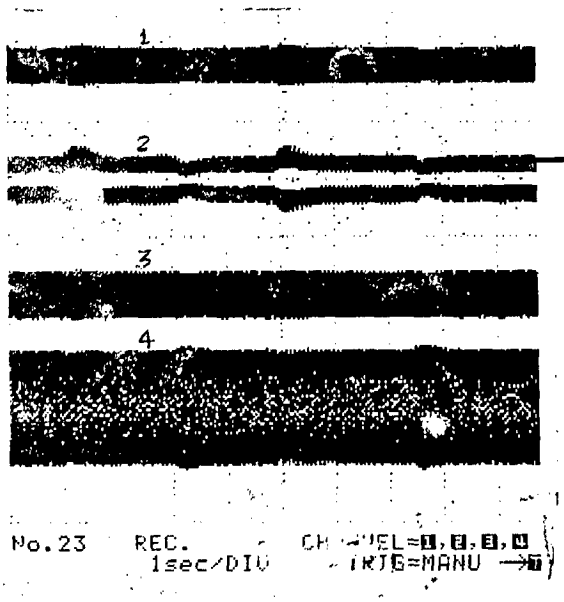
(i)

Capacitance change 56 μF – 40 μF – 56 μF
Speed change 1660 RPM – 1845 RPM – 1660 RPM



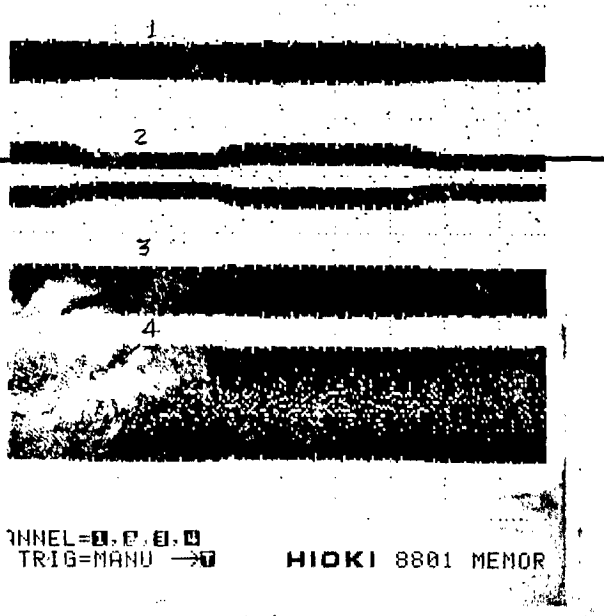
(ii)

Capacitance = 56 μF, Speed = 1660 RPM,
Load change = 170 Watts



(iii)

Capacitor change 40 μF – 36 μF – 40 μF
Speed change 1845 RPM – 1925 RPM – 1845 RPM

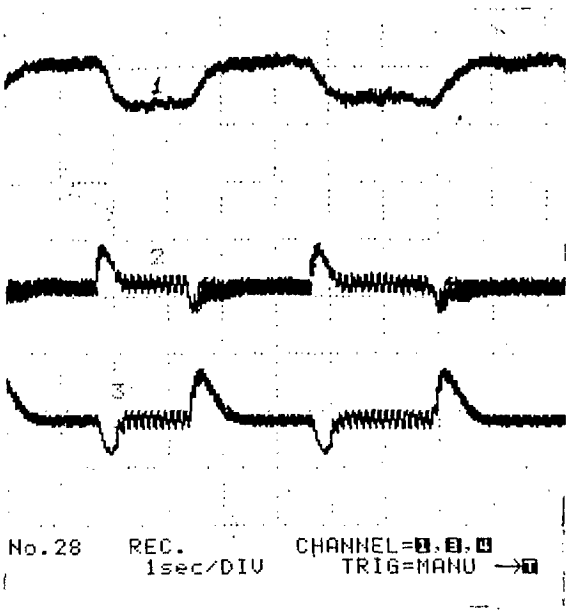


(iv)

Capacitance = 40 μF, Speed = 1845 RPM,
Load change = 120 Watts

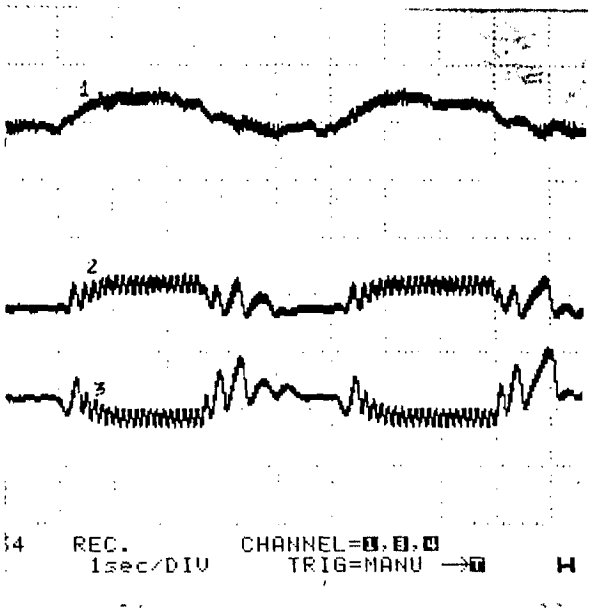
Fig 5.3a OPEN LOOP DYNAMIC PERFORMANCE OF THE SYSTEM UNDER SUDDEN CHANGE OF CAPACITANCE (i), (iii) LOAD (ii), (iv) POWER CIRCUIT WAVEFORMS OF,

1: Capacitor Current
2: Inverter Current
3: Motor Current
4: Terminal Voltage



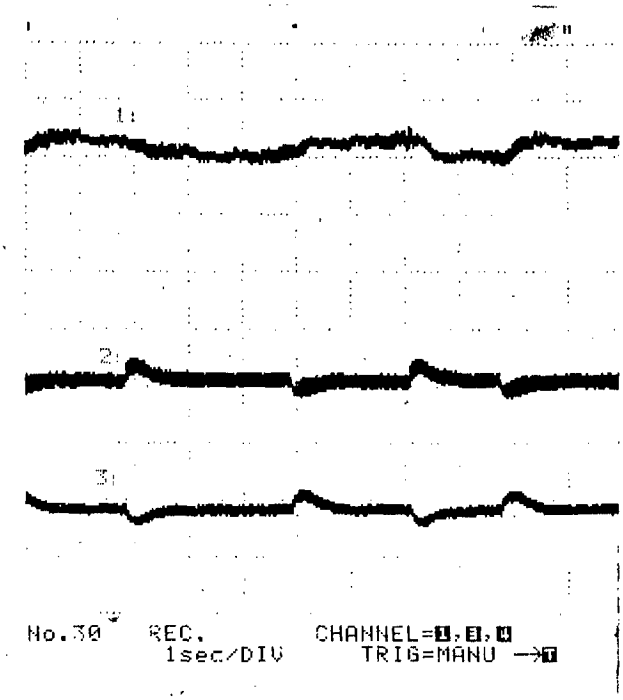
(i),

Capacitance change 56 μF - 40 μF - 56 μF
Speed change 1660 RPM - 1845 RPM - 1660 RPM



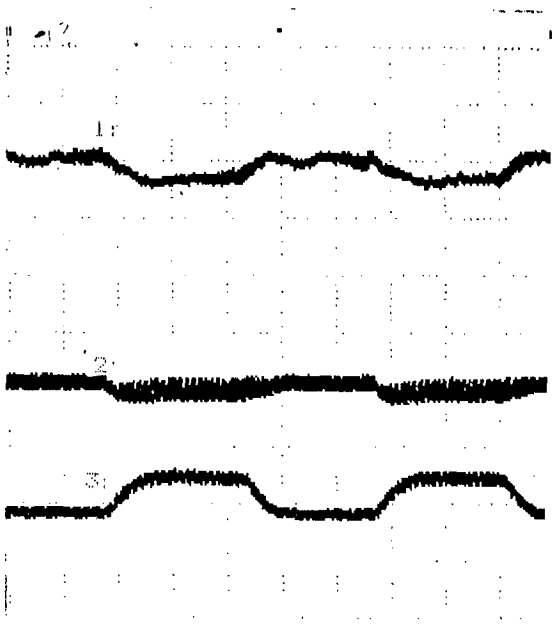
(ii)

Capacitance = 56 μF, Speed = 1660 RF
Load change = 170 Watts



(iii)

Capacitor change 40 μF - 36 μF - 40 μF
Speed change 1845 RPM - 1925 RPM - 1845 RPM



,(iv)

Capacitance = 40 μF, Speed = 1845 RF
Load change = 120 Watts

Fig.5.3b OPEN LOOP DYNAMIC PERFORMANCE OF THE SYSTEM UNDER SUDDEN CHANGE OF CAPACITANCE (i),(iii) LOAD (ii),(iv)
CONTROL CIRCUIT WAVEFORMS OF
1: Motor Speed
2: Terminal Voltage
3:DC Link Current

2030RPM) and corresponding oscillograms are shown in Fig. 5.5 (a),(b),(c) and (d) respectively.

5.4 DISCUSSIONS OF RESULTS

5.4.1 Effect of Variation of Load on Speed

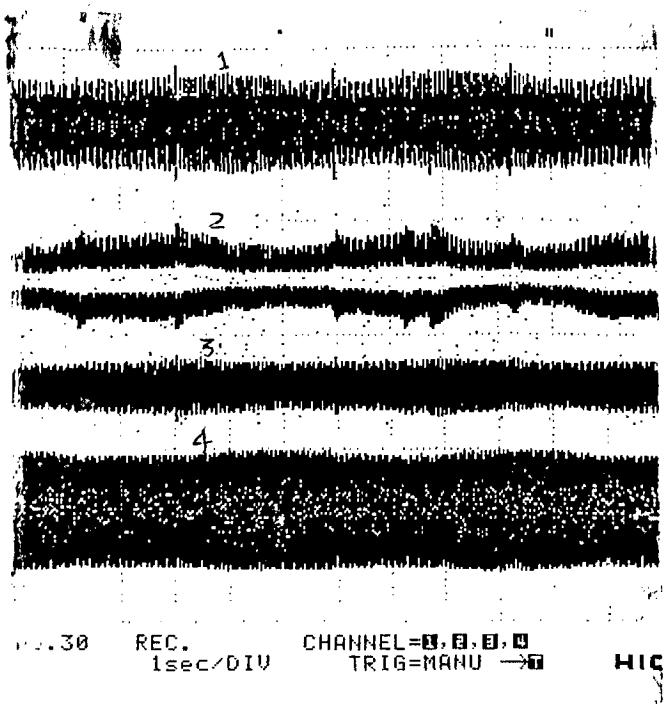
In Fig. 5.2a, variation of speed with output power is shown for three different operational conditions as with normal supply (50Hz), with open loop control of drive and with closed loop control of drive. It is observed that open loop characteristic is similar to that with normal supply but in closed loop control of speed, speed remains constant irrespective of load. Fig.5.2b shows speed variation with output power for different reference speeds. It is observed that in open loop control, speed rises with load for speeds above the base speed and falls for speeds below the base speed. The rise in speed with load above base speed is due to the fact that lagging reactive power of motor increases with load which is balanced by increasing frequency at constant terminal voltage with unsaturated magnetic circuit of motor for fixed capacitor value. It may be observed from Fig.5.2b that for higher speeds machine could be loaded to the lesser extent, it is because of higher value of stator and rotor leakage reactances which further increase with increase in speed (frequency). A machine having low leakage inductances would give better loading capability.

5.4.2 Effect of Load on Other Parameters

It may be observed from Fig. 5.2c that current at no load reduces for higher speeds it is due to the reduction in magnetizing current of motor and it rises with increasing load. As shown in Fig.5.2d, inverter current rises more with load than motor current. It is because of the constant power factor of inverter, however, motor power factor increases with load as evident from Fig.5.2f. It may be observed from Fig.5.2e and Fig.5.2f that variation of motor efficiency and power factor for open loop and closed loop control of drive are almost similar.

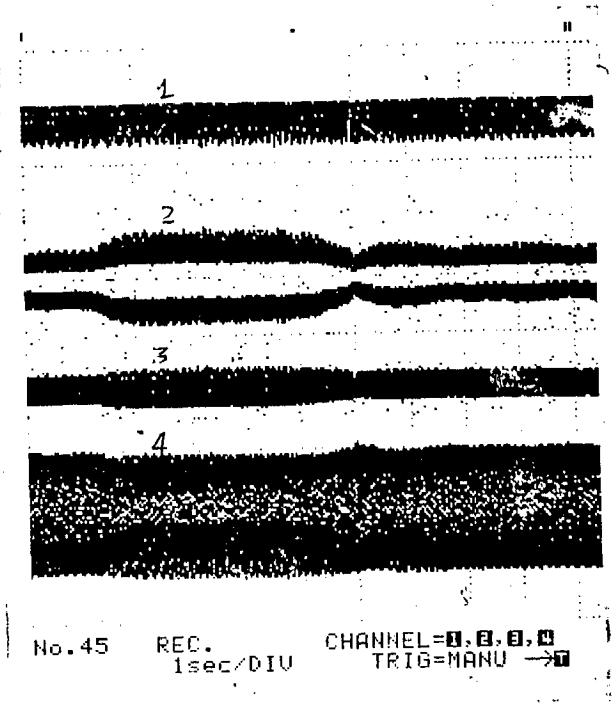
5.4.3 Dynamic Performance of the System

It can be noted from waveforms of Fig.5.3a for open loop control of drive that capacitor current and motor current decrease with reduction in capacitor value. Terminal voltage falls slightly and inverter current rises momentarily. When capacitor value is reduced, speed of motor rises requiring accelerating power due to that inverter current rises momentarily. The observed fall in terminal voltage is due to sudden increase in inverter current. The reverse phenomenon occurs when capacitor value is increased. It is also observed that for a sudden change of load, inverter current, motor and capacitor current increase but terminal voltage falls slightly



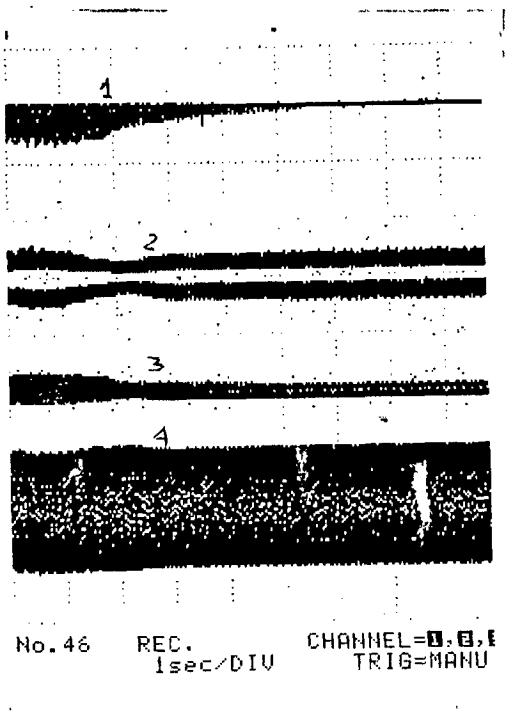
(i)

Reference Speed=1660 RPM, Capacitance=65 μF,
Load Change=110 Watts



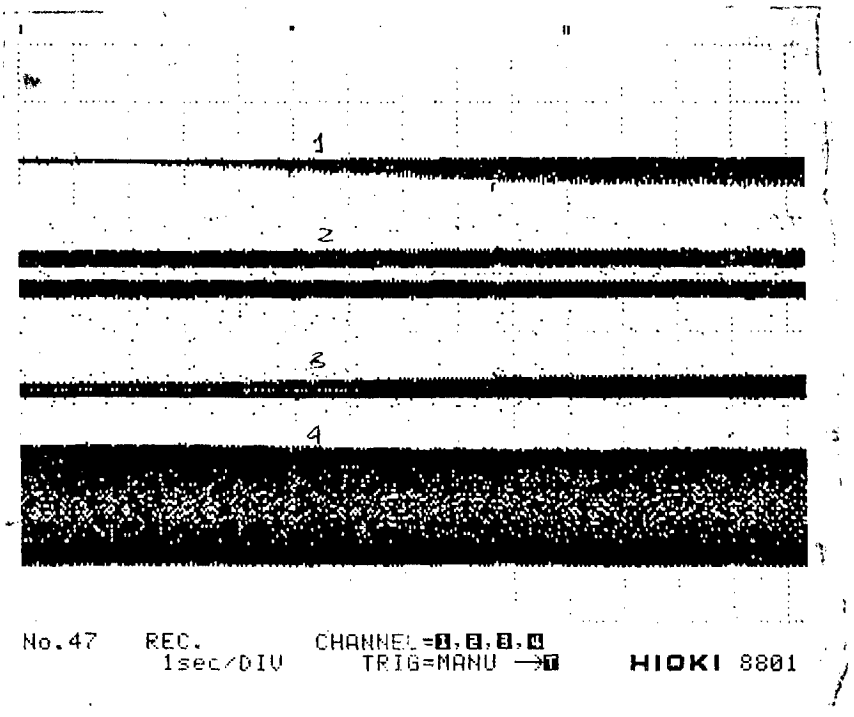
(ii)

Reference Speed=2030 RPM, Capacitance=40 μ
Load Change=116 Watts



(iii)

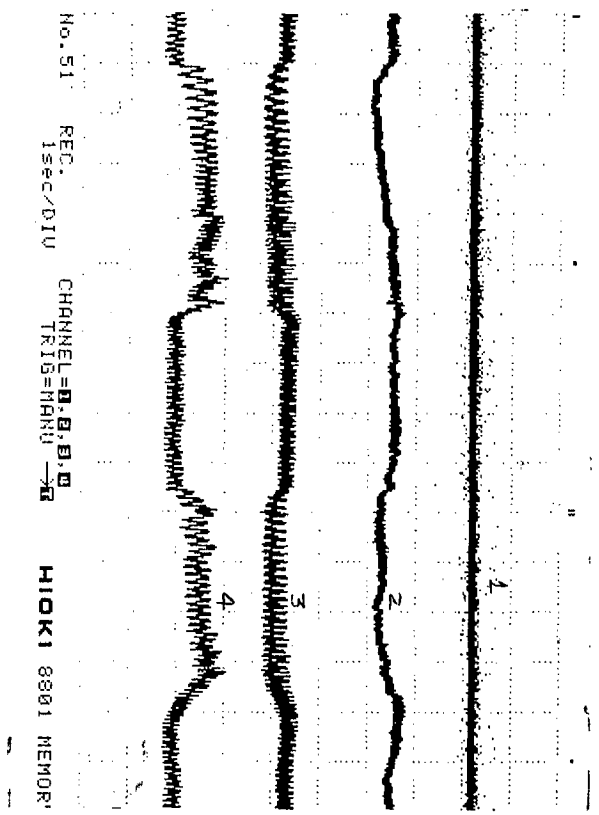
SPEED CHANGE FROM 2050 RPM TO 1660RPM



(iv)

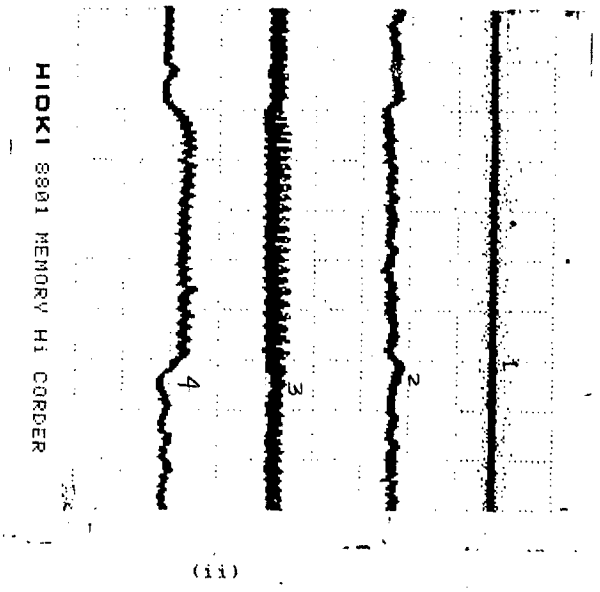
SPEED CHANGE FROM 1660 RPM TO 2050 RPM

Fig.5.3c CLOSED LOOP PERFORMANCE OF THE SYSTEM UNDER SUDDEN CHANGE OF LOAD (i),(ii) REFERENCE SPEED (iii)(iv)
POWER CIRCUIT; WAVEFORMS OF 1: Inductor Current
2: Inverter Current
3: Motor Current
4: Terminal Voltage



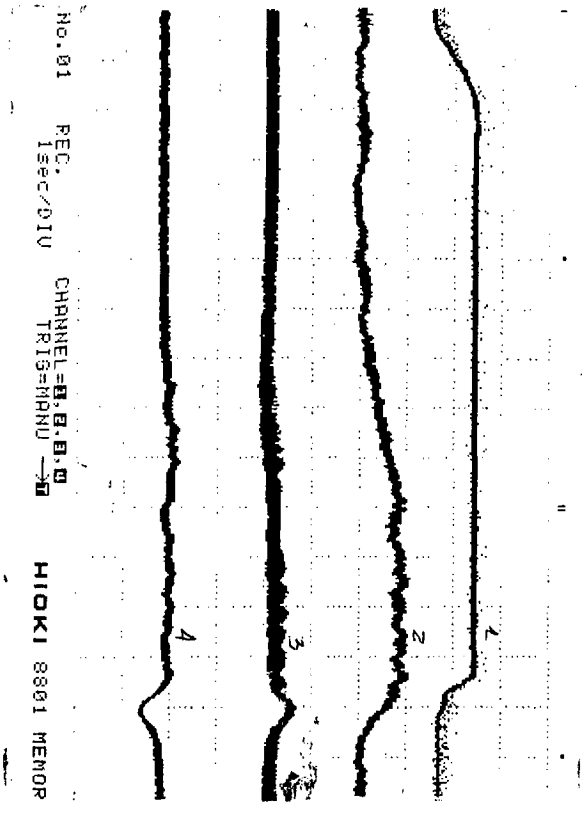
(i).

Reference Speed=1660 RPM, Capacitance=65 μF,
Load Change=110 Watts



(ii)

Reference Speed=2030 RPM, Capacitance=40 μF,
Load Change=116 Watts



(iii).

SPEED CHANGE FROM
1660 RPM TO 2030 RPM TO
1660 RPM

Fig.5.3d CLOSE LOOP DYNAMIC PERFORMANCE UNDER SUDDEN CHANGE OF REFERENCE SPEED (iii) LOAD (i), (ii) CONTROL CIRCUIT WAVEFORMS OF

1: Reference Speed
2: Actual Speed
3: Terminal Voltage
4: DC Link Current

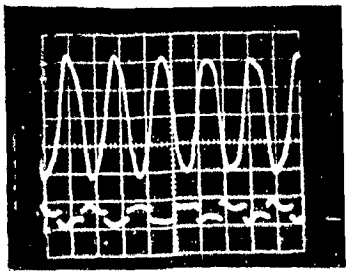
due to increased value of various currents. From the control circuit waveforms of speed, motor voltage and dc link current of Fig.5.3b, it may be observed that speed rises when the capacitor value is reduced, dc link current increases to supply accelerating power and increased rotational losses and results in fall of voltage. For a sudden change of load speed falls slightly due to increased slip and finally approaches to steady state value.

It is concluded from Fig.5.3c that for a closed loop control of drive a suden change in load causes to increase motor and inverter currents and fall in terminal voltage with a neglible change in inductor current. It is also observed that for a sudden increase in reference speed there is no change in inverter current and terminal voltage but there is increase in motor and inductor currents. From the Fig.5.3d, it is observed that speed decreases slightly with sudden change of load and then approach to its steady state value. DC link current increases to meet load requirement and terminal voltage falls slightly due to momentarily increased dc link curent. It is observed that motor speed rises slowly to reach steady state value when reference speed is increased suddenly. There is no much change in terminal voltage but dc link current increases slightly to supply increased rotational losses at no load. It is also observed that with a sudden decrease in reference speed, dc link current decreases and terminal voltage rises momentarily, inductor current reduces.

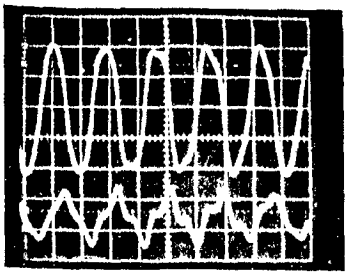
5.4.4 Discussions of Oscillograms

Fig.5.4a and Fig.5.4c show oscillograms of terminal voltage and currents of (i) inverter , (ii) motor and (iii) capacitor, under open loop condition for two different capacitor values at no load. It is observed that at no load, voltage waveform is almost sinusoidal and the inverter current is continuous. Fig.5.4c and Fig.5.4d show the same waveforms at load for the two different capacitor values. It is clear from these figures that voltage waveform also contains some harmonics which are more for higher speed. Harmonic contents of motor current are increased with load. The inverter current waveform at load is similar to that at no load. There is no much change in capacitor curent waveform from no load to loaded condition of motor.

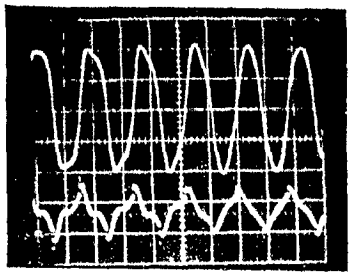
Fig.5.5a and Fig.5.5c show waveforms of voltage and currents of (i) inverter, (ii) motor, (iii) capacitor and (iv) controlled inductor for closed loop control of system at no load and reference speed of 1660 RPM and 2030 RPM respectively. It is observed from these figures that voltage and motor current waveforms contain harmonics and inverter current is continuous but inductor current is discontinuous. Harmonics in the motor voltage are larger for higher reference speeds. It may be observed from voltage waveforms that overlap angle is negligible.



(i) Iinv = 1.45 A

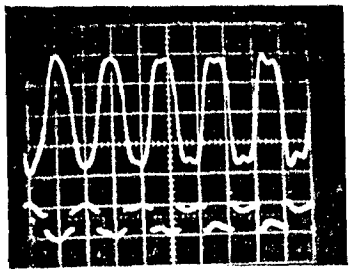


(ii) Im = 5.0 A

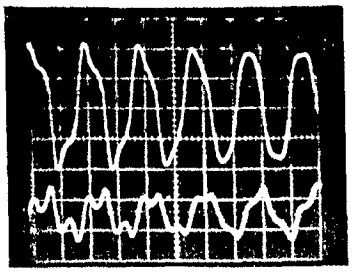


(iii) Ic =4.5 A

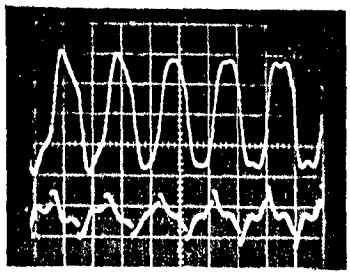
Fig.5.4a Terminal Voltage = 230 V, Capacitance = 56 μF, Speed = 1660 RPM, at no load



(i) Iinv = 4.15 A

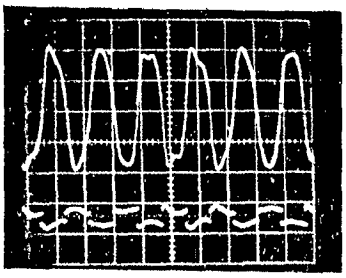


(ii) Im = 5.2 A

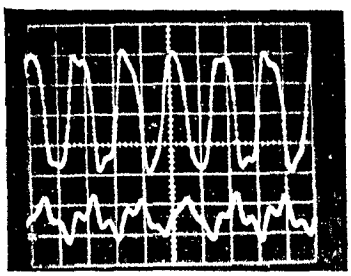


(iii) Ic = 4.7 A

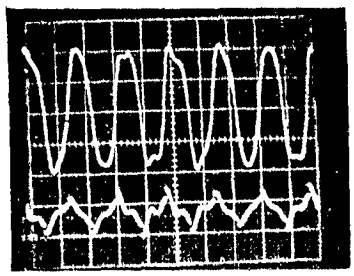
Fig.5.4b Terminal Voltage =230 V. Capacitance = 56 μF, Speed = 1680 RPM, at load (Po = 280 Watts)



(i) Iinv = 1.4 A

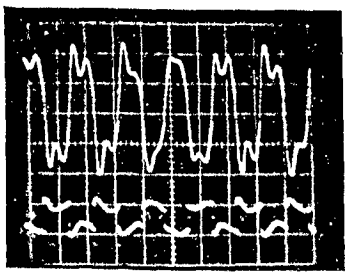


(ii) Im = 3.2 A

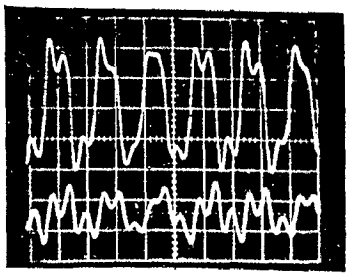


(iii) Ic = 3.8 A

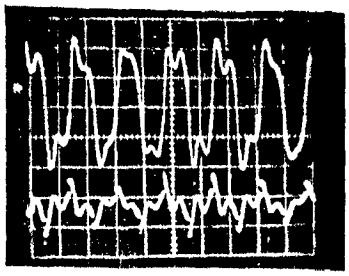
Fig.5.4c Terminal Voltage = 230 V, Capacitance = 40 μF, Speed = 1845 RPM, at no load



(i) Iinv = 2.6 A



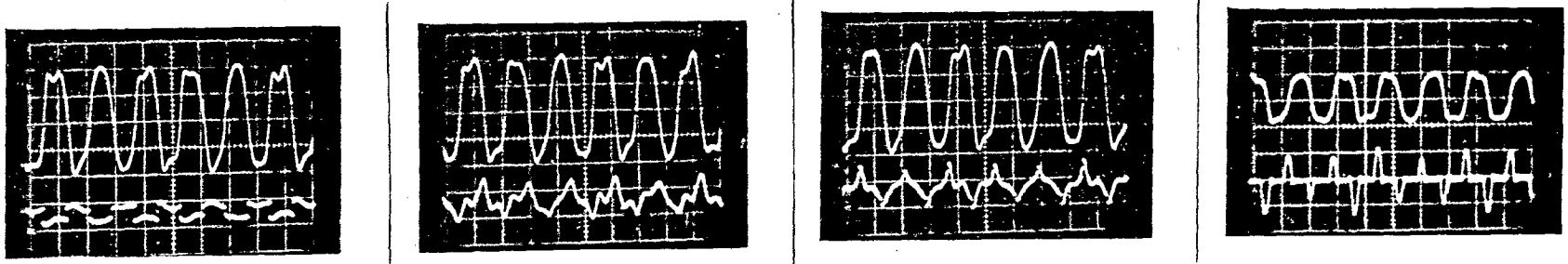
(ii) Im = 4.0 A



(iii) Ic = 3.9 A

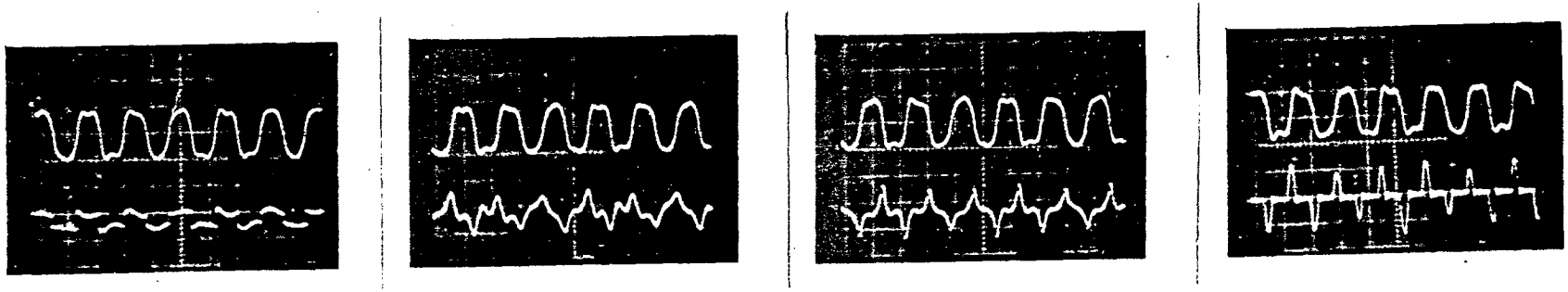
Fig.5.4d Terminal Voltage 230 V, Capacitance = 40 μF, Speed = 1845 RPM, at load (Po = 340 Watts)

Fig.5.4 OSCILLOGRAMS OF TERMINAL VOLTAGE (UPPER) AND CURRENT (LOWER) OF (I) INVERTER (Iinv), (II) MOTOR (Im), (III) CAPACITOR (Ic) UNDER OPEN LOOP CONTROL



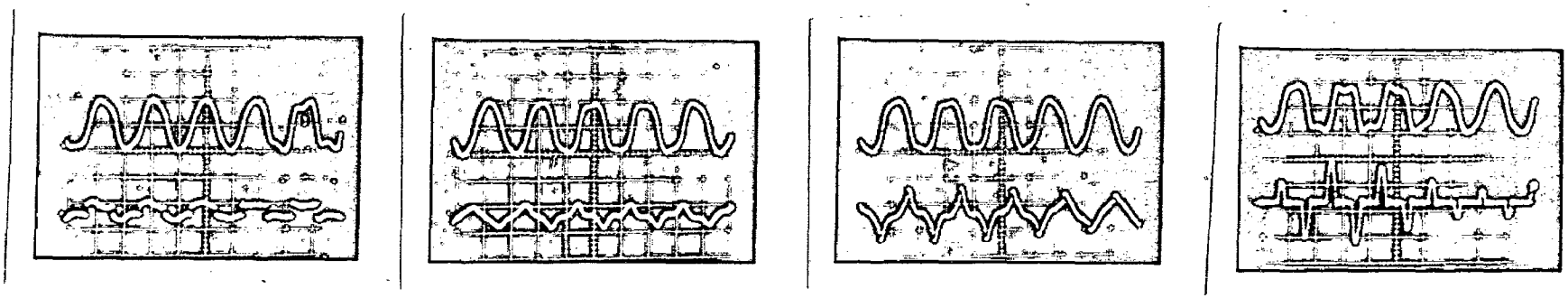
(i) Iinv = 1.8 A (ii) Im = 4.3 A (iii) Ic = 4.6 A (iv) Iind = 1.0 A

Fig.5.5a Terminal Voltage = 230 V, Capacitance = 65 μF, Reference Speed = 1660 RPM, at no load



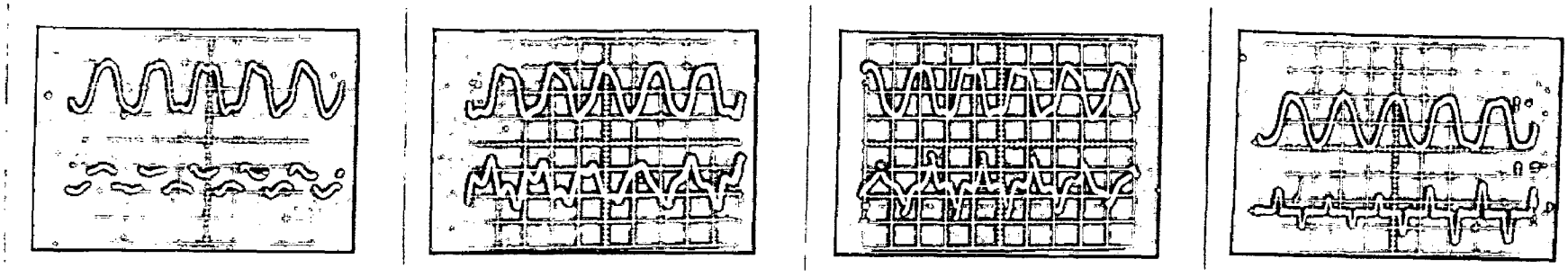
(i) Iinv = 1.7 A (ii) Im = 5.3 A (iii) Ic = 5.6 A (iv) Iind = 0.9 A

Fig.5.5b Terminal Voltage = 230 V, Capacitance = 65 μF, Reference Speed = 1660 RPM, at load (Po = 480 Watts)



(i) Iinv = 1.45 A (ii) Im = 3.1 A (iii) Ic = 3.2 A (iv) Iind = 1.3 A

Fig.5.5c Terminal Voltage = 230 V, Capacitance = 40 μF, Reference Speed = 2030 RPM, at no load



(i) Iinv = 2.8 A (ii) Im = 4.3 A (iii) Ic = 3.9 A (iv) Iind = 1.1 A

Fig.5.5d Terminal Voltage = 230 V, Capacitance = 40 μF, Reference Speed = 2030 RPM, at load (Po = 360 Watts)

...ONS OF TERMINAL VOLTAGE (UPPER) AND CURRENT
...NVERTER (Iinv), (II) MOTOR (Im), (III) CAPACITOR
...TOR (Iind) UNDER CLOSED LOOP CONTROL

Fig.5.5b and Fig.5.5d show waveforms at load for the similar conditions of Fig.5.5a and Fig.5.5c. It may be observed that inductor current is discontinuous at load too. Harmonics in voltage are more and the motor current contains more harmonics. There is no much change in capacitor and inverter current waveforms.

5.5 CONCLUSIONS

The various starting methods of drive are described which may be used for starting of the motor. The steady state performance of the motor for closed loop control under loaded condition has been studied in detail and compared with performance of the drive in open loop control. Dynamic performance of the system under open and closed loop control has been studied and it is observed that system is stable under sudden change in capacitor value, load and reference speed. It is seen that the inverter current is continuous and voltage waveform is very close to sinusoidal. Motor current is also found nearly sinusoidal. Moreover, the overlap angle is observed neglible for the proposed drive. It is also concluded from results that loading capability of drive decreases with increasing the speed.

CHAPTER 6

CONCLUSIONS AND SUGGESTIONS FOR FURTHER WORK

6.1 MAIN CONCLUSIONS

The main objectives of this investigation were to design, fabricate and determine performance of microprocessor controlled load commutated inverter fed single-phase induction motor drive for variable speed operation above base speed. The drive system is developed and the following main conclusions are made on the basis of experimental and computed results.

(i) For the scheme two fully controlled converters are fabricated, one acting as rectifier and other as load commutated inverter. Thyristor controlled inductor is used for controlling the speed of motor in closed loop manner. The required hardware along with software is developed for microprocessor controlled drive.

(ii) It is observed from the experimental results that the system is stable at no load as well as loaded condition of the motor. It is concluded that a desired range of speed can be achieved by varying terminal capacitor value in open loop control and by varying current through controlled inductor in closed loop control. In closed loop control of the drive, speed remains constant irrespective of load.

(iii) The computed results under no load as well as loaded condition of the motor show good correlation with experimental results, thus establishing the validity of developed model.

(iv) The machine could be loaded for lesser values of load at higher speeds. Loading capability of the machine reduces with increase in speed. A machine designed for lower values of leakage inductances would be loaded to greater extent.

(v) The system is found stable at load and reference perturbation in closed loop control. The dynamic response of the system shows the satisfactory operation of the drive.

(vi) From oscillograms of voltage and currents of inverter, motor, capacitor and inductor, it is concluded that voltage waveform is almost sinusoidal and motor current contains harmonics. However, harmonic contents in motor current are lesser as compared to VSI or CSI. Inverter current is continuous even at no load and the current of controlled inductor is discontinuous. It is also concluded that overlap angle is negligible.

The conclusions mentioned above show that the system has worked satisfactorily under steady state and dynamic conditions.

Due to higher leakage inductances of the motor loading capability of the drive is lower at higher speeds. For such a drive, machine having lower leakage inductances would give better results.

6.2 SUGGESTIONS FOR FURTHER WORK

The basic objectives of present scheme has been achieved successfully, but certain problems have arisen during the course of investigation. The problems arisen during present work may be intersting for further investigations. They are as

(i) In the present scheme the field weakening method is used to control the speed of motor above base speed. The drive features may be extended for speed control below base speed of motor.

(ii) Here only single quadrant operation of the drive is obtained . The drive may be investigated for four quadrant operation.

(iii) The machine could be loaded for lesser value of load at higher speeds. It was due to higher leakage inductances of the machine. The drive may be investigated using a machine designed for low values of leakage inductances.

(iv) A 16 bit microprocessor system along with improved control techniques such as adaptive controller etc. may be used to improve system accuracy and fast response.

(v) In the present scheme, the speed of drive is controlled with the help of thyristor controlled inductor. However saturable core reactor or static VAR generator can be used in place of thyristor controlled inductor for improved performance of drive.

(vi) A general computer algorithm may be developed to compute the performance in steady state as well as in dynamic conditions of the drive in open loop and in closed loop control.

(vii) For a cheap drive, a diode rectifier can be used instead of fully controlled rectifer.

(viii) The drive is not self starting, better starting methods may be developed to start it at no load as well as on load.

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APPENDIX-A

DETAILS OF MACHINES USED

(I) Single-Phase Induction Motor

Voltage		230	V
Current		7.1	A
Speed		1440	RPM
H.P.		1.0	
Frequency		50	Hz
Stator Reactance	X1	3.6753	OHM
Stator Resistance	R1	1.9460	OHM
Rotor Reactance	R2	3.7784	OHM
Rotor Resistance	X2	3.6753	OHM

(II) DC Machine

Voltage	440	V
Current	8.5	A
Speed	2850	RPM
Horse Power	3.0	
Armature Resistance	5.2	OHM

(III) Tachogenerator

0 - 10,000 RPM
20 V per 1000 RPM

APPENDIX-B

PROGRAM FOR PERFORMANCE COMPUTATION

```
5 PRINT CHR$(12)
10 READ R1,X1,R2,X2,AK1,AK2,CMA,CMI,DC,SO,SM,DS,V,WRO,DF,E,B
20 FC=1:FP=1
30 FOR I=1 TO 70
40 C=CMA-(I-1)*DC
50 K=0
60 FOR J=1 TO 30
70 S=SO+(J-1)*DS
80 GOSUB 5000
85 AP=AC
100 FC=FP+DF
101 GOSUB 5000
120 IF ABS(AC) > ABS(AP) THEN 410
140 FC=FP+DF
150 GOSUB 5000
151 PRINT AC,AP,FC,FP
160 IF ABS(AC) < ABS(AP) THEN FP=FC:AP=AC:GOTO 140
170 IF ABS(AP) < E THEN 200
180  PRINT TAB(10);"No Convergence "
190 GOTO 480
200 PGF=CIF^2*R2/(2!*5)
210 PGB=CIB^2*R2/(2!*(2!-S))
220 PG=PGF-PGB
230 F=FP
240 SNS=1500!*F
250 SNR=(1!-S)*SNS
260 WS=2!*3.14*SNS/60!
270 WR=(1!-S)*WS
280 PO=PG-WRO
290 TSH=PO/WR
300 TINT=PG/WS
310 PLR=SPGF+(2!-S)*PGB
320 PLS=CL1^2*(R1)
330 PLCU=PLR+PLS
340 PL=WRP+PLCU
350 PI=PO+PL
360 ETA=PO/PI*100!
370 PF=PI/(V*(I1))
380 FR=50!*F
390 PRINT TAB(10);C;S;SNR;SNS;FR;F;TSH;TINT;PO;PI;ETA;PF;PL;CI1
400 GOTO 470
420 FC=FP-DF
430 GOSUB 5000
440 IF ABS(AC) > ABS(AP) THEN 100
460 GOTO 420
470 FP=F
480 NEXT J
```

```
490 NEXT I
500 END
600 DATA 1.9460,3.6753,3.7784,3.6753,156.73,16.68,70.0,1.00,1.00
610 DATA 0.0050,0.1500,0.005,230.00,104.82,1.0,6.0,20
1001 PRINT F(1)
5000 XC=1!/(314.14*C)*1000000#
5010 XM=AK1-AK2*V/(FC*50!)
5020 ZSR=R1
5030 ZSI=X1*FC
5040 ZFR=((FC^2*(XM)^2*R2)/(2!*S))/((R2/S)^2+(FC*(X2+XM))^2)
5050 ZFI=FC*XM*((R2/S)^2+FC^2*X2*(X2+XM))*.5/((R2/S)^2+(FC*(X2+XM))^2)
5055 ZBR=R2*(FC*XM)^2/((2*(2-S))*(R2/(2-S))^2+(FC*(X2+XM))^2)
5060 ZBI=FC*XM/2!*((R2/(2!-S))^2+FC^2*X2*(X2+ XM))/((R2/(2!-S))^2+(FC*(X2+
5070 ZR=ZSR+ZFR+ZBR
5080 ZI=ZSI+ZBI+ZFI
5090 Z=(ZR^2+ZI^2)^.5
6100 Y1=ZR/Z
6110 Y2=ZI/Z
6120 AC=(V*Y1+TAN(B)+V*Y2)/Z+(WRO+(TAN(B)/V))-(V*FC/XC)
6130 CI1=V/Z
6140 CIF=CI1*FC*XM/((R2/S)^2+(FC*(X2+XM))^2)^.5
6145 CIB=CI1*FC*XM/((R2/(2-S))^2+(FC*(X2+XM))^2)^.5
 150 RETURN
```

APPENDIX-C

SYSTEM SOFTWARE IN MACHINE LANGUAGE

(1) MAIN PROGRAM

LEBEL 1	ADDRESS 2	MACHINE CODE 3	INSTRUCTIONS 4	COMMENTS 5
	2050	31 00 27	LXISP,2700	initialise STACK POINTER
	2053	3E 91	MVIA,91H	initialise 8255(1)
	2055	D3 03	OUT 03H	PA;IN,PB:OUT,PCu:OUT,PC1:IN
	2057	AF	XRA	make all firing bits low
	2058	D3 01	OUT01H	timer TM1, TM2' gates low
	205A	D3 02	OUT02H	
	205C	32 18 20	STA 2018H	store Port C status
	205F	32 19 20	STA 2019H	store Port B status
	2062	32 09 20	STA 2009H	store index S (00H)
	2065	3E 70	MVIA,70H	initialize timers TM1
	2067	D3 13	OUT 13H	TM2 of up kit
	2069	D3 A3	OUT A3H	and TM',TM2' of extra timer
	206B	3E 80	MVIA,80H	in mode zero
	206D	D3 13	OUT 13H	
	206F	D3 A3	OUT A3H	
	2071	3E FF	MVIA,FFH	load TM2 of up kit with
	2073	D3 12	OUT 12H	FFFFH
	2075	D3 12	OUT 12H	
	2077	21 D5 00	LXIH00D5H	store initial rectifier
	207A	22 03 20	SHLD 2003H	firing angle αc
	207D	21 28 00	LXIH 0028H	store initial B
	2080	22 14 20	SHLD 2014H	
	2083	3E 16	MVIA,16H	initialize PIC
	2085	D3 28	OUT 28H	ICW1
	2087	3E 2B	MVIA,2BH	
	2089	D3 29	OUT 29H	ICW2
	208B	3E E0	MVIA,E0H	OCW1,unmask IR0,IR1,
	208D	D3 29	OUT 29H	IR2,IR3,IR4
MEM3	208F	3A 18 20	LDA 2018H	load PortC status
	2092	E6 90	ANI 906	Select IN0 channel for
	2094	D3 02	OUT02H	inputting ref. speed
	2096	32 18 20	STA 2018H	store part C status
	2099	CD 20 20	CALL ADCSR	call ADC subroutine
	209C	32 00 20	STA 2000H	store ref. speed
	209F	3A 18 20	LDA 2018H	load part C status
	20A2	E6 90	ANI 90H	select IN1 channel
	20A4	F6 20	ORI 20H	of ADC for
	20A6	D3 62	OUT 02H	inputting terminal voltage
	20A8	32 18 20	STA 2018H	store Port C status
	20AB	CD 20 20	CALL ADCSR	call ADC subroutine
	20AE	32 02 20	STA 2002H	store terminal voltage

```
        20b1    3A 18 20  LDA 2018H     load port C status
        20B4    F6 60     ORI60H       select IN3 channel
        20B6    D3 02     OUT 02H      for inputting dc link current
        20B8    32 18 20  STA 2018H    store port C status
        20BB    CD 20 20  CALL ADCSR   call ADC subroutine
        20BE    32 0C 20  STA 200CH    store dc link current
        20C1    3A 18 20  LDA 2018H    load port C status
        20C4    E6 90     ANI 90H      select IN2 channel
        20C6    F6 40     ORI 40H      for  inputting  actual speed
        20C8    D3 02     OUT02H
        20CA    32 18 20  STA 2018H    store port C status
        20CD    CD 20 20  CALL ADCSR   call ADC subroutine
        20D0    32 01 20  STA 2001H    store actual speed
        20D3    3A 09 20  LDA 2009H    load index S
        20D6    FE 01     CPI 01H      compare with 01H
        20D8    DA DE 20  JC MEM1      if carry jump to MEM1
        20DB    C3 E3 20  JMP MEM2     jump to MEM2
MEM1    20DE    3C        INRA         increament accumulator
        20DF    32 09 20  SIA 2009H    store index S
        20E2    FB        EI           enable interrupts
MEM2    20E3    3A 01 20  LDA 2001H    load actual speed
        20E6    32 FU 27  STA27FUH     store actual speed
        20E9    3A 00 20  LDA 2000H    load reference speed
        20EC    32 F5 27  STA 27F5H    store reference speed
        20EF    CD E3 06  CALL MODAD   display  ref.& actual speed
        20F2    3A 02 20  LDA 2002H    load terminal voltage
        20F5    32 F6 27  STA 27F6H    store terminal voltage
        20F8    CD FA 06  CALL MODAD   display terminal voltage
        20FB    C3 BF 20  JMP MEM3     jump to MEM3
```

---

(2) ADC SUBROUTINE

1	2	3	4	5
	2020	3A 18 20	LDA 2018H	load port C status
	2023	E6 7F	ANI 7FH	make SOC bit low
	2025	D3 02	OUT 02H	via PC7 bit of port Cu
	2027	F6 80	ORI 80H	make SOC bit high
	2029	D3 02	OUT 02H	via PC7 bit of port Cu
	202B	00	NOP	no operation
	202C	E6 7F	ANI 7NFH	make SOC Pin low
	202E	D3 02	OUT 02H	via PC7 bit of port Cu
READ	2030	DB 62	IN 02H	in port C1
	2032	E6 01	ANI 01H	check PC0 bit
	2034	CA 30 20	JZ READ	jump to READ if zero
	2037	DB 00	IN 00H	in port A
	2039	C9	RET	return

(3) IRO-ISS

1	2	3	4	5
	2100	C5	PUSH B	save registers
	2101	D5	PUSH D	
	2102	E5	PUSH H	
	2103	F5	PUSH PSW	
	2104	3A 19 2C	LDA 2019H	make rectifier firing
	2107	E6 FC	ANI FCH	bits PB0 & PB1 low
	2109	03 01	OUT 01H	
	2108	32 19 20	STA 2019	
	210E	3A 0C 20	LDA 200CH	load dc link current Idc in A
	2111	FE 8C	CPI80H	compare Idc with Idcmax(=80H)
	2113	DA 1C 21	JC MEM01	if Idc<Idcmax jump to MEM01
	2116	00 00 00	NOP	no operation
	2119	C3 AB 21	JMP MEM02	jump to MEM02
MEM01	211C	3A 02 20	LDA2002H	load terminal voltage(Vt) in A
	211F	FE 70	CPI 70H	compare Vt with Vr
	2121	DA 5A 21	JC MEM03	if Vt<Vr jump to MEM03
	2124	CA 8C 21	JZ MEM04	if Vt=Vr jump to MEM04
	2127	DE 70	SBI 70H	if Vt>Vr,calculate Vt-Vr
	2129	FE 15	CPI 15H	compare Vt-Vr with 15H
	212B	DA 34 21	JC MEM05	if Vt-Vr<15H jump to MEM05
	212E	21 80 00	LX1H0080H	if Vt-Vr>15H,dαc c = 0080H
	2131	C3 42 21	JMP MEM06	jump to MEM06
MEM05	2134	FE 03	CPI03H	compare Vt-Vr with 03H
	2136	DA 3F 21	JC MEM07	if Vt-Vr<03H jump to MEM07
	2139	21 10 00	LX1H0010H	if Vt-Vr>03H,dαc=0010H
	213C	C3 42 21	JMP MEM06	jump to MEM06
MEM07	213F	21 01 00	LX1H0001H	if Vt-Vr<03H,dαc=0001H
MEM06	2142	EB	XCHG	dαc ⇒ (DE)
	2143	2A 03 20	LHLD 2003H	load αc in HL pair
	2146	19	DADD	αc = αc + dαc
	2147	22 03 20	SHLD 2003H	store αc
	214A	EB	XCHG	
	214B	21 00 1F	LX1H1F00H	check if αc>90deg
	214E	CD C5 04	CALL H1LO	
	2151	DA 89 21	JC MEM08	if αc<90° jump to MEM08
	2154	22 03 20	SHLD 2003H	if αc>90°, αc = 90° and store
	2157	C3 8F 21	JMP MEM04	jump to MEM02
MEM03	215A	47	MOV B,A	
	215B	3E 70	MVIA	if Vt<Vr
	215D	90	SUBB	calculate Vr-Vt

```
          215E    FE 15     CPI15H          compare Vr-Vt with 15H
          2160    DA 69 21  JC MEM09        if Vr-Vt<15H  jump  to
                                            MEM09
          2163    21 80 00  LX1H0060H       if Vr-Vt>15H,d acc=0060H
          2166    C3 77 21  JMP MEMO 10     jump to MEMO 10
MEM09     2169    FE 03     CPI 03H         compare Vr-Vt with 03H
          216B    DA 74 21  JC MEMO 11      if Vr-Vt<03H jump to
                                            MEMO 11
          216E    21 20 00  LX1H0010H       if Vr-Vt>03H,dacc= 0010H
          2171    C3 77 21  JMP MEMO 10     jump to MEMO10
MEMO11    2174    21 01 00  LXIH 0001H      if Vr-Vt<03H,d acc=0001H
MEMO10    2177    EB        XCHG            (DE)=d acc
          2178    2A 03 20  LHLD 2003H      Load HL with  acc
          217B    EB        XCHG            (DE) → (HL)
          217C    CD C5 04  CALL HILO       Calculate acc = acc - d acc
          217F    21 D5 00  LXIH 00D5H      compare o c with 2.5
          2082    CD C5 04  CALL HILO
          2085    DA 89 21  JC MEM08        If acc < 2.5 , acc = 2.5
          2088    19        DADD            (DE)+(HL) → (HL)
MEM08     2089    22 03 20  SHLD 2003H      load acc in HL pair
          2146    19        DADD            acc = acc + d acc
          2147    22 03 20  SHLD 2003H      store acc
          214A    EB        XCHG
          214B    21 00 1F  LXIH 1F00H      check if acc >90°
          214E    CD C5 04  CALL HILO
          2151    DA 89 21  JC MEM08        if acc <90° jump to MEM08
          2154    22 03 20  SHLD 2003H      if acc >90°, acc =90°
          2157    C3 8F 21  JMP MEM04       jump to MEM04
MEM03     215A    47        MOV B,A
          215B    3E 70     MVI A,70H
          215D    90        SUB B           calculate Vt-Vr
          215E    FE 15     CPI 15H         compare Vt-Vr with 15H
          2160    DA 69 21  JC MEM09        if Vt-Vr<15H jump to
                                            MEM09
          2163    21 60 00  LXIH 0060H      if Vt-Vr>15H,dacc =0060H
          2166    C3 77 21  JMP MEM010      jump to MEM010
MEM09     2169    FE 03     CPI 03H         compare Vr-Vt with 03H
          216B    DA 74 21  JC MEM011       if Vr-Vt<03H jump to
                                            MEM011
          216E    21 10 00  LXIH 0010H      if Vr-Vt>03H,  dacc  =
                                            0010H
          2171    C3 77 21  JMP MEM010      jump to MEM010
MEM011    2174    21 01 00  LXIH 0001H      if Vr-Vt<03H,dacc= 0010H
MEM010    2177    EB        XCHG            dacc → (DE)
          2178    2A 03 20  LHLD 2003H      load HL with acc
          217B    EB        XCHG            (DE) → (HL)
          217C    CD C5 04  CALL HILO       calculate acc=acc -dacc
          217F    21 D5 00  LXIH 00D5H      compare acc with 2.5
          2082    CD C5 04  CALL HILO
          2085    DA 89 21  JC MEM08        if acc <2.5 , acc=2.5
          2088    19        DADD            (DE)+(HL) → (HL)
MEMO 8    2089    22 03 20  SHLD 2003H      store acc
MEM04     218C    2A 03 20  LHLD 2003H
```

```
        218F    7D          MOV  A,L        load timer TM1(11H)
        2190    D3 11       OUT  11H        with rectifier firing
        2192    7C          MOV  A,H        angle ∝c
        2193    D3 11       OUT  11H
        2195    3A 18 20    LDA  2018H      make timer TM1(11H) gate
        2198    F6 10       ORI  10H        high via PC4 bit of
        219A    D3 02       OUT  02H        Port Cu
        219C    32 18 20    STA  2018H
        219F    DB 02       IN   02H        in Port C in A
        21A1    E6 04       ANI  04H        check PC2 bit
        21A3    CA AB 21    JZ   MEM012     if low jump to MEM012
        21A6    3E 01       MVIA , 01H      if high make index R
MEM012  21A8    32 0A 20    STA  200AH      as 01H and store
MEM02   21AB    F3          DI              disable interrupts
        21AC    3E 60       MVIA , 60H      issue specific EOI
        21AE    D3 28       OUT  28H        command
        21B0    F1          POP  PSW        recover registers
        21B1    E1          POP  H
        21B2    D1          POP  D
        21B3    C1          POP  B
        21B4    FB          EI              enable interrupts
        21B5    C9          RET             return to main program
```

(IV) IR1-ISS

1	2	3	4	5
	2280	F5	POP PSW	push PSW into STACK
	2281	3A 0A 20	LDA 200AH	check index R
	2284	FE 01	CPI 01H	
	2286	DA 95 22	JC MEME1	if index is 00H jmp to MEME1
	2289	3A 19 20	LDA 2019H	if index is 01H, fire
	228C	E6 FC	ANI FC H	1;3 pair of thyristers
	228E	F6 02	ORI 02H	via bit PB1 bit of PorB
	2290	D3 01	OUT 01H	
	2292	C3 9E 22	JMP MEME2	jump to MEME2
MEME1	2295	3A 19 20	LDA 2019H	fire 2;4 pair of thyrt.
	2298	E6 FC	ANI FCH	via bit PB0 of Port B
	229A	F6 01	ORI 01H	
	229C	D3 01	OUT 01H	
MEME2	229E	32 19 20	STA 2019H	
	22A1	3A 18 20	LDA 2018H	make timer TM1 (11H)
	22A4	E6 EF	ANI EFH	gate low
	22A6	D3 02	OUT 02H	
	22A8	32 18 20	STA 2018H	
	22AB	F3	DI	disable interrupts
	22AC	3E 61	MVI A,61H	issue specific EOI
	22AE	D2 28	OUT 28H	command
	22B0	F1	POP PSW	recover registers
	22B1	FB	EI	enable interrupts
	22B2	C9	RET	return to main

(V) IR2-ISS

1	2	3	4	5
	23C0	C5	PUSH B	save registers
	23C1	D5	PUSH D	
	23C2	E5	PUSH H	
	23C3	F5	PUSH PSW	
	23C4	3A 19 20	LDA 2019H	make inverter & inductr
	23C7	E6 C3	ANI C3H	firing bits low, timer
	23C9	F6 C0	ORI C0H	TM2(A2H) gate high
	23CB	D3 01	OUT 01H	
	23CD	32 19 20	STA 2019H	
	23D0	DB 02	IN 02H	in PC1 bit of port C1
	23D2	E6 02	ANI 02H	check PC1 bit
	23D4	CA 55 24	JZ MEMY2	if zero jump to MEMY2
	23D7	3E 01	MVI A,01H	make index I as 01H
	23D9	32 0B 20	STA 200BH	
	23DC	DB 12	IN 12H	read timer TM2(12H)
	23DE	6F	MOV L,A	
	23DF	DB 12	IN12 H	
	23E1	67	MOV H,A	
	23E2	3E FF	MVI A,FFH	load timer TM2 (12H)
	23E4	D3 12	OUT 12H	with FFFFH
	23E6	D3 12	OUT 12H	
	23E8	57	MOV D,A	calculate 180 deg count
	23E9	5F	MOV E,A	and store
	23EA	CD C5 04	CALL HILO	
	23ED	EB	XCHG	
	23EE	22 12 20	SHLD 2012H	
	23F1	AF	XRA	calculate 90 deg count
	23F2	1F	RAR	
	23F3	7C	MOV A,H	
	23F4	1F	RAR	
	23F5	67	MOV H,A	
	23F6	7D	MOV A,L	
	23F7	1F	RAR	
	23F8	6F	MOV L,A	
	23F9	EB	XCHG	
	23FA	21 00 09	LXIH 0900H	check 90 deg count
	23FD	CD C5 04	CALL HILO	
	2400	DA 5A 24	JC MEMY3	if 90 deg count<0900H jump to MEMY3
	2403	19	DADD	
	2404	22 10 20	SHLD 2010H	store 90 deg count
	2407	00 00 00	NOP	
	240A	00 00	NOP	
	240C	2A 14 20	LHLD 2014H	load B in HL pair
	240F	3A 00 20	LDA 2000H	load ref speed in A
	2412	4F	MOV C,A	move ref speed Nr in C
	2413	3A 01 20	LDA 2001H	load actual speed Na

```
         2416    B9          CMP C           compare Na  & Nr
         2417    CA 30 24    JZ MEMY4        if Na=Nr jump to MEMY4
         241A    DA 2B 24    JC MEMY5        if Na<Nr jump to MEMY5
         241D    EB          XCHG            else find dB
         241E    C3 6E 24    JMP MEMY6       B=(BdB)
MEMY11   2421    CD C5 04    CALL HILO
         2424    DA 30 24    JC MEMY4        jump to MEMY4
         2427    EB          XCHG
         2428    C3 30 24    JMP MEMY4
MEMY5    242B    EB          XCHG
         242C    C3 8B 24    JMP MEMY7       find dB
MEMY14   242F    19          DADD            B=B+dB
MEMY4    2430    22 14 20    SHLD 2014H
         2433    EB          XCHG
         2434    2A 10 20    LHLD 2010H      check B
         2437    CD C5 04    CALL HILO
         243A    DA 43 24    JC MEMY8
         243D    22 14 20    SHLD 2014H
         2440    C3 46 24    JMP MEMY9
MEMY8    2443    2A 14 20    LHLD 2014H      calculate o l=180B
MEMY9    2446    EB          XCHG
         2447    2A 12 20    LHLD 2012H
         244A    EB          XCHG
         244B    CD C5 04    CALL HILO
         245E    EB          XCHG
         244F    22 05 20    SHLD 2005H      store  o l
         2452    C3 5A 24    JMP MEMY2       jump to MEMY2
         2455    3E 00       MVIA,00H        if PC1 bit if low store
         2457    32 0B 20    STA 200BH       index I as 00H
MEMY3    245A    2A 05 20    LHLD 2005H      load o l in timer
         245D    7D          MOV A,L         TM2'(A2H)
         245E    D3 A2       OUT A2H
         2460    7C          MOV A,H
         2461    D3 A2       OUT A2H
         2463    F3          DI              disable int.
         2464    3E 62       MVI A,62H       specific EOI
         2466    D3 28       OUT 28 H
         2468    F1          POP PSW         recover registers
         2469    E1          POP H
         246A    D1          POP D
         246B    C1          POP B
         246C    FB          EI              enable int.
         246D    C9          RET             return to main prog
MEMY6    246E    91          SUB C           calculate NaNr
         246F    FE 20       CPI 20H         compare NaNr with 20H
         2471    DA 7A 24    JC MEMY10       NaNr<20H,jump to MEMY10
         2474    21 15 00    LXIH 0015H      NaNr>20H,dB=0015H
         2477    C3 21 24    JMP MEMY11      jump to MEMY11
MEMY10   247A    FE 05       CPI 05H         Compare NaNr with 05H
         247C    DA 85 24    JC MEMY12       NaNr<05H,jump to MEMY12
         247F    21 08 00    LXIH 0008H      dB=0008H
         2482    C3 21 24    JMP MEMY11      jump to MEMY11
MEMY12   2485    21 01 00    LXIH 0001H      dB=0001H
```

```
        2488    C3 21 24  JMP MEMY11      jump to MEMY11
MEMY7   248B    47        MOV B,A
        248C    79        MOV A,C
        248D    90        SUB B           calculate NrNa
        248E    FE 20     CPI 20H         compare NrNa with 20H
        2490    DA 99 24  JC MEMY13       NrNa<20H,jump to MEMY13
        2493    21 15 00  LXIH 0015H      NrNa>20H,dB=0015H
        2496    C3 2F 24  JMP MEMY14      jump to MEMY14
MEMY13  2499    FE 05     CPI 05H         Compare NrNa with 05H
        249B    DA A4 24  JC MEMY15       NrNa<05H,jump to MEMY15
        249E    21 08 00  LXIH 0008H      NrNa>05H,dB=0008H
        24A1    C3 2F 24  JMP MEMY14      jump to MEMY14
MEMY15  24A4    21 01 00  LXIH 0001H      NrNa<05H,dB=0001H
        24A7    C3 2F 24  JMP MEMY14      jump to MEMY14
```

(VI) IR3-ISS

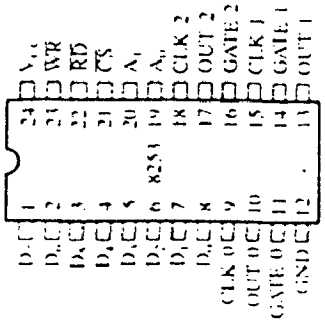
1	2	3	4	5
	2380	F5	PUSH PSW	save registers
	2381	3A 0B 20	LDA 200BH	load inverter index I
	2384	FE 01	CPI 01H	check index I
	2386	DA 95 23	JC MEME1	if 00H, jump to MEME1
	2389	3A 19 20	LDA 2019H	if index is 01H then
	238C	E6 F3	ANI F3H	fire SCR pair 1,3 of
	238E	F6 08	ORI 08H	inverter via PB3 bit
	2390	D3 01	OUT 01H	of port B
	2392	C3 9E 23	JMP MEME2	jump to MEME2
MEME1	2395	3A 19 20	LDA 2019H	if index I is 00H then
	2398	E6 F3	ANI F3H	fire SCR pair 2,4 of
	239A	F6 04	ORI 04H	inverter via PB2 bit of
	239C	D3 01	OUT 01H	port B
MEME2	239E	32 19 20	STA 2019H	
	23A1	F3	DI	disable interrupts
	23A2	3E 63	MVIA,63H	specific EOI command
	23A4	D3 28	OUT 28H	
	23A6	F1	POP PHW	recover registers
	23A7	FB	EI	enable interrupts
	23A8	C9	RET	return to main program

(VII) IR4-ISS

1	2	3	4	5
	24C0	F5	PUSH PSW	save registers
	24C1	3A 0B 20	LDA 200BH	load index I
	24C4	FE 01	CPI 01H	check index I
	24C6	DA D5 24	JC MEMA1	if zero, jump to MEMA1
	24C9	3A 19 20	LDA 2019H	if index is 01H, fire
	24CC	E6 4F	ANI 4FH	SCR1 of controlled
	24CE	F6 20	ORI 20H	inductor via PB4 bit
	24D0	D3 01	OUT 01H	of port B
	24D2	C3 DE 24	JMP MEMA2	jump to MEMA2
MEMA1	24D5	3A 19 20	LDA 2019H	if index is 00H fire
	24D8	E6 4F	ANI 4FH	SCR2 of controlled
	24DA	F6 10	ORI 10H	inductor via PB5 bit
	24DC	D3 01	OUT 01H	of port B
MEMA2	24DE	32 19 20	STA 2019H	
	24E1	F3	DI	
	24E2	3E 64	MVI A,64H	specific EOI
	24E4	D3 28	OUT 28H	
	24E6	F1	POP PSW	recover registers
	24E7	FB	EI	enable int.
	24E8	C9	RET	return to main

APPENDIX-D

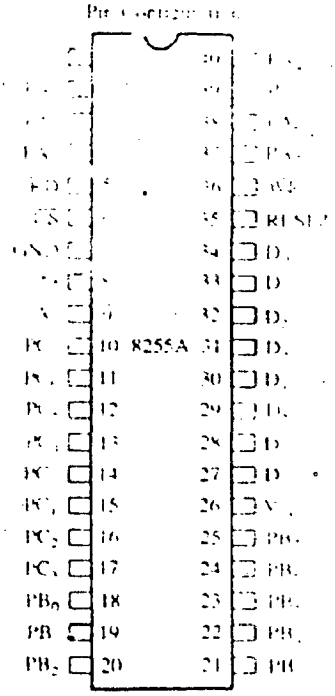
Pin Details of Different IC Chips used in Present Work



Pin Names

D_7–D_0	Data Bus (8 Bit)
CLK N	Counter Clock Inputs
GATE N	Counter Gate Inputs
OUT N	Counter Outputs
$\overline{RD}$	Read Counter
$\overline{WR}$	Write Command or Data
$\overline{CS}$	Chip Select
A_0–A_1	Counter Select
V_{CC}	+5 Volts
GND	Ground

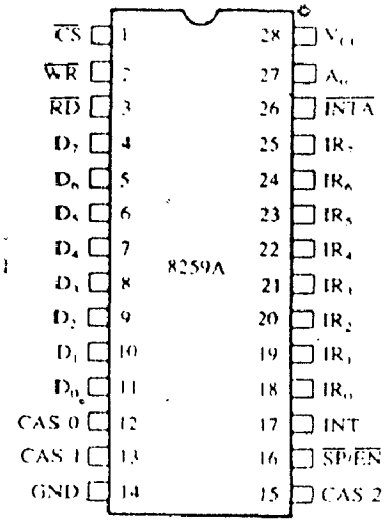
Fig.D.1 TIMER 8253



Pin Names

D_7–D_0	Data Bus (Bidirectional)
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0–A_1	Port Address
PA_7–PA_0	Port A (Bit)
PB_7–PB_0	Port B (Bit)
PC_7–PC_0	Port C (Bit)
V_{CC}	+5 Volts
GND	0 Volts

Fig.D.2 PPI 8255A



Pin Names

D_7–D_0	Data Bus (Bidirectional)
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0	Command Select Address
$\overline{CS}$	Chip Select
CAS_2–CAS_0	Cascade Lines
$\overline{SP/EN}$	Slave Program/Enable Buffer
INT	Interrupt Output
$\overline{INTA}$	Interrupt Acknowledge Input
IR_0–IR_7	Interrupt Request Inputs

Fig.D.3 PIC 8259A

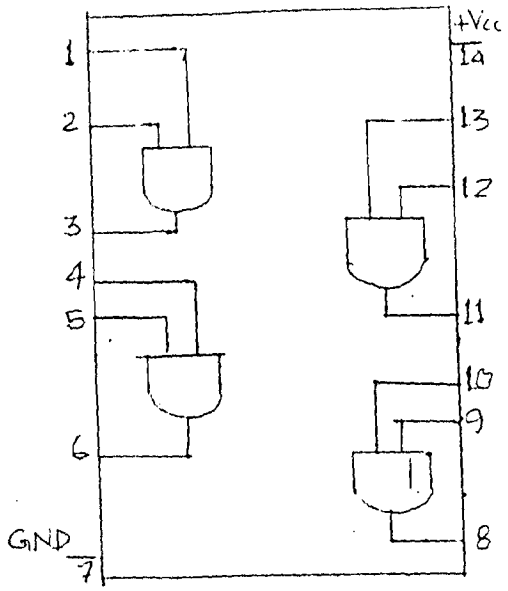


Fig.D.4 AND GATE (IC 7408)

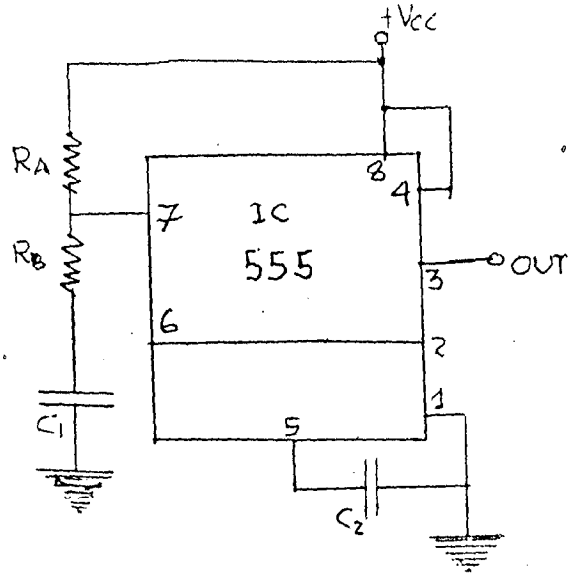


Fig.D.6 IC 555 AS OSCILLATOR

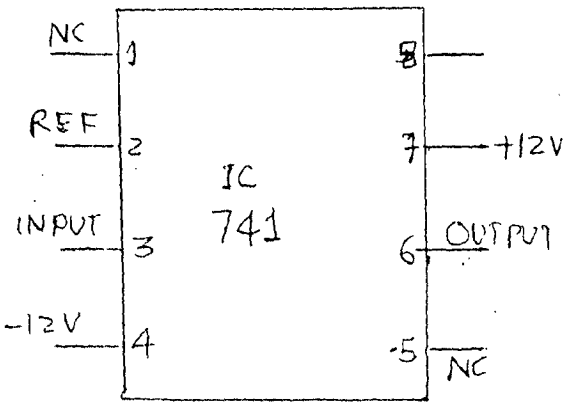


Fig.D.5 IC 741 AS COMPARATOR

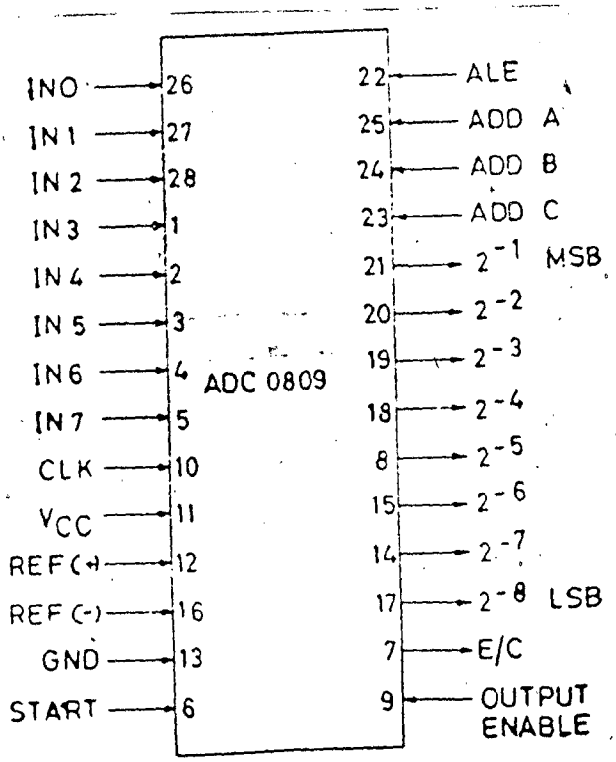


Fig.D.7 ADC 0809

PORT ADDRESS OF VARIOUS PERIPHERALS

PPI 8255A (1)

PORT	PORT ADDRESS
PORT A	00H & 04H
PORT B	01H & 05H
PORT C	02H & 06H
CWR	03H & 07H

PIT 8253-1

COUNTER	PORT ADDRESS
COUNTER 0	10H & 14H
COUNTER 1	11H & 15H
COUNTER 2	12H & 16H
CWR	13H &17H

PIT 8253-2

COUNTER 0	A0H
COUNTER 1	A1H
COUNTER 2	A2H
CWR	A3H

PIC 8259A

DATA WORD	28H & 2CH
COMMAND WORD	29H & 2DH

SIGNALS AT CONNECTORS J1, J2 AND J3

PIN NO.	J1 SPACE	J2 SPACE	J3 SPACE
1	CAS0	P1C4	P2C4
2	CAS1	P1C5	P2C5
3	CAS2	P1C2	P2C2
4	SP/EN	P1C3	P2C3
5	IR0	P1C0	P2C0
6	IR1	P1C1	P2C1
7	IR2	P1B6	P2B6
8	IR3	P1B7	P2B7
9	IR4	P1B4	P2B4
10	IR5	P1B5	P2B5
11	IR6	P1B2	P2B2
12	IR7	P1B3	P2B3
13	CLK0	P1B0	P2B0
14	GATE0	P1B1	P2B1
15	OUT0	P1A6	P2A6
16	CLK1	P1A7	P2A7
17	GATE1	P1A4	P2A4
18	OUT1	P1A5	P2A5

19	CLK2	P1A2	P2A2
20	GATE2	P1A3	P2A3
21	OUT2	P1A0	P2A0
22	RST7.5	P1A1	P2A1
23	RST6.5	P1C6	P1C6
24	MP	P1C7	P2C7
25	GND	GND	GND
26	GND	GND	GND