RECORDING OF SURGES IN POWER SYSTEM

A DISSERTATION

submitted in partial fulfilment of the
requirement for the award of the degree
of
MASTER OF ENGINEERING
in
ELECTRICAL ENGINEERING
(Power System Engineering)

By

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April, 1987

DEDICATED

TO

MY FATHER

AND

BELOVED WIFE NEERU

CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the dissertation entitled RECORDING OF SURGES IN POWER SYSTEM in partial fulfilment of the requirements for the degree of MASTER OF ENGINEERING in ELECTRICAL ENGINEERING with specialisation in POWER SYSTEM ENGINEERING submitted in the department of Electrical Engineering, U.O.R, ROORKEE, is an athentic record of my own work carried out during a period of about $7\frac{1}{2}$ months, from September 1, 1986 to April 10,1987 under the supervision of Dr.(Mrs.) K.P. Suleebka, Reader, and Shri Vinay Pant, Lecturer, Electrical Engineering Department, UNIVERSITY OF ROORKEE, ROORKEE(INDIA).

The matter embodied in this dissertation has not been submitted for the award of any other degree or diploma.

Jaya Prakash

Dated: April 15 , 1987. (JAYA PRAKASH)

This is certified that the above statement made by the candidate is correct to the best of my knowledge.

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DATE: 15-4-1987

ABSTRACT

This dissertation work describes the recording of surge in power system by microprocessor based surge recorder.

Various types of overvoltages, their influence on the selection of insulation levels of power system components and overvoltage limiting devices, their measuring or recording methods, have been highlighted in the introductory chapter. A brief review of the available literature on measuring or recording the surges has been given in chapter 2.

The third chapter deals with the simulation of switching surges to check the correctness of the surge recorder developed. The work has been carried out on low voltage, hence instead of spark gap a debounced switch has been used in surge generator.

The fourth chapter deals with the developmental stages of microprocessor based surge recorder. The first stage of development is to record the magnitude and time of the surge generated from microprocessor itself. The second stage of surge recorder is the recording of the externally generated surge on receiving signal from microprocessor to generate the surge. The third stage is final stage which is on-line surge recorder.

The fifth chapter deals with the results and discussion of the all three developmental stages of surge recorder. A comparative study has been made between the

surges recorded by microprocessor based surge recorder and the surges stored on storage cathode ray oscilloscope.

The last chapter sixth is the concluding chapter in which many conclusions derived from the work done in third, fourth and fifth chapter have been discussed.

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CHAPTER 1

INTRODUCTION

The development in the field of electrical engineering during the present century have been tremendous. Increase in power demand at longer distances has forced the transmission voltages to be higher and higher from economics point of view. In world 1100 KV transmission lines are already in operation and in India 400 KV lines have been built.

A large number of expensive electrical equipments are used for high and extra high voltages transmission lines. It is necessary to ensure that such costly equipments are capable of withstanding the over voltages which are met due to lightning and switching transients.

The trend toward increasingly high transmission voltages has made insulation design and application an extremely dynamic subject. A key element in this area is the nature of transient phenomena found on extra high voltage networks. The majority of information available today has been obtained through either simulation (e.g. transient network analysis) or staged system tests of relatively short duration. There is a growing need for continuous monitoring of power line transients both in terms of developing improved equipment designs and in terms of analyzing component failures.[1]

High voltage surges in power system influence the selection of insulation levels of the power system components

and of over voltage limiting devices. The two types of surges (1) lightning surge and (2) switching surges play an important role in selection of insulation levels. It is difficult to measure these surges in the system and they are often calculated theoretically only. The action of over voltage limiting devices however may not turn out to be satisfactory as their selection is invariably based upon the calculated over voltages rather than on measured ones. Thus, improper action of over voltage limiting devices (e.g. surge diverter)or improper selection of insulation levels can result in - i) damage to equipment, ii) large number of outages, iii) low reliability and (iv) Consequent economic loss. If it were possible to measure the overvoltage at selected points in power system, a better understanding of overvoltages will result and it will help in selecting proper insulation levels and overvoltage limiting devices, in proper operation of the system, in high reliability and in consequent economy. So the availability of reliable information on overvoltages is of prime importance for the technical and economic improvement of high and extra high voltage power lines. The overvoltage characteristics are determined by means of special experiments or automatic recording. The most reliable data can be produced on direct measurement in operating networks.

Switching surges have been recorded by extensive equipment, which is manufactured only in foreign countries. In 1985, CPRI, Banglore, has acquired one such mobile unit at

great expense. Since 1930, the recording of lightning surges was done by the use of an oscilloscope in many countries. On the Indian System though, neither the lightning surges nor the switching surges have yet been recorded. The studies on TNA and by computer programme also have been made extensively in foreign countries.

With the help of microprocessor many a dedicated tasks can be achieved cheaply. Thus, it should be possible to record voltage surges with the help of microprocessor on magnetic tapes, discs or other storing devices. The power consumption would be low, the whole system would be light weight and cost will also be much lesser than other methods. A low voltage signal of the high voltage surge could be obtained by a capacitive voltage devider, and could be transmitted over optical fibre cable which is immune to electromagnetic disturbances which are invariably present in a power system.

CHAPTER 2

METHODS FOR RECORDING OF SURGES IN POWER SYSTEM

System disturbances in the public electricity supply system can lead to faulty operation of computers and computer based equipment with consequent financial loss and damage to electronic equipment and components.[2] Two sets of recording equipment for recording these disturbances were compared. One set was a microprocessor controlled digital waveform recorder mounted in a special shielding enclosure developed at the Hydro Quebec Research Institute, the other was a National Research Council of Canada Oscilloscope whose performance had been demonstrated in work on high voltage impulse measuring standards. The relative accuracy of the two sets had been measured by parallel connection to a resistor divider[3].

Recording of unreproducible transients with unknown amplitudes (e.g. lightning or switching overvoltages) requires automatic adaption of the measuring range during the signal recording. This can be realized with digital transient recorders in a continuous manner using automatically switched dividers.[4]

Waveform digitisation is the most sophisticated technique currently available for measuring analogue signals whether they be fast, slow, continuously varying, repetitive or single shot. Indeed, it is the only technique available for single shot measurements.[5]

Multipoint data recorders are ideal for recording several slowly varying signals symultaneously, since they offer multiplexing facilities for a number of lines. Microprocessor based recorders also offer signal digitizing capability so that the data tabulation is possible as well as chart recording.[6]

2.1 TECHNIQUES FOR MEASURING OR RECORDING IMPULSE VOLTAGES OR CURRENT

2.1.1 SPARK GAPS:

First attempts were made to measure lightning impulses with the help of a crude device consisting of parallel gaps with different spacings. To prevent the first gap to break down from short circuiting the others and to prevent the system outage, a relatively high resistance was placed in series with each gap. The measure of the voltage is the maximum gap which has broken down. Peek used sphere gaps and needle gaps in parallel to obtain a measure of waveshape.[9].

2.1.2 CATHODE-RAY-OSCILLOGRAPHS

To measure the voltages on transmission lines a capacitance divider is generally used, and for surge currents a resistance shunt,the voltage across the resistance is applied to the oscilloscope plates. A non-linear shunt can be used to cover wider current range.

Modern oscillographs are sealed tube hot cathode oscilloscopes with photographic arrangement for recording the

waveforms. Normally 5mV/cm to about 20V/cm is the input voltage range for cathode ray oscilloscope (CRO). There are probes and attenuators to handle signals upto 600 V (peak to peak). The rise time and bandwidth of oscilloscope should be adequate. Oscilloscopes are fitted with good cameras for recording purposes.

For rapidly changing signals, it is necessary to initiate the oscilloscope time base before the signal to be measured reaches the deflecting plates of oscilloscope, otherwise a portion of the signal may not be recorded. So accurate initiation of horizontal time base known as triggering is necessary for such measurements. For the recording of impulses external triggering is used, in which the signal is directly fed to actuate the time base and then applied to the vertical or Y deflecting plates through a delay line. The delay is usually .1 to .5 μ Sec. which is obtained by -

(1) A 20 to 50 m long interconnecting coaxial cable is used. The required triggering is obtained from an antenna whose induced voltage is applied to the external trigger terminal.

(2) Delay is obtained by an externally connected coaxial long cable and the measuring signal is transmitted to CRO by normal coaxial cable.

2.1.3 MEASUREMENT OF HIGH IMPULSE CURRENT USING MAGNETIC POTENTIOMETERS (Rogowski Coils)

The coil is wound on a non magnetic former of toroidal shape and is coaxially placed surrounding the current carrying conductor. In order to get enough signal induced, a large number of turns on the coil are used. Output signal voltage proportional to the current to be measured is obtained by using an integrating circuit. The arrangement is shown in fig.1.1

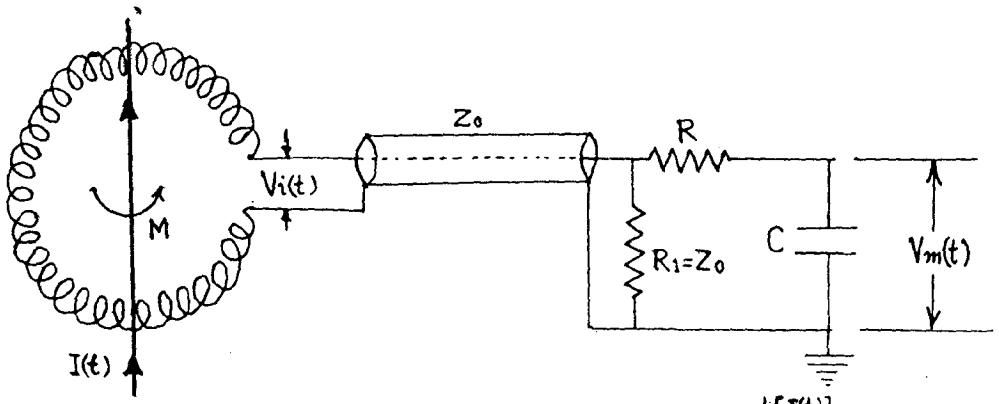
$$V_m(t) = \frac{1}{CR} \int_0^t V_i(t) = \frac{M}{CR} I(t)$$

Rogowski coils with electronic or active integrator circuits have large bandwidth (about 100 MHz) [10]

2.1.4 MEASUREMENT OF HIGH IMPULSE CURRENTS USING MAGNETIC LINKS

Magnetic links are short high retentivity steel strips arrnaged on a circular wheel or drum. The property of such strips is that the remanent magnetism for a current pulse of 0.5/5 μSec. is the same as that caused by d.c. current of same value. The strips are placed at a known distance from current carrying conductor and parallel to it. In the laboratory special instrument measures the remanent magnetism from which the peak value of the current is estimated.

Magnetic link are useful for the estimation of lightning currents on transmission lines or towers. By using a number of links accurate measurement of crest value, polarity



Vi(t) - INDUCED VOLTAGE IN THE COIL = $M\frac{d[I(t)]}{dt}$

Z_0 - SURGE IMPEDANCE OF COAXIAL CABLE

R-C - INTEGRATING NETWORK

FIG. 1·1 ROGOWSKI COIL FOR HIGH IMPULSE CURRENT MEASUREMENT

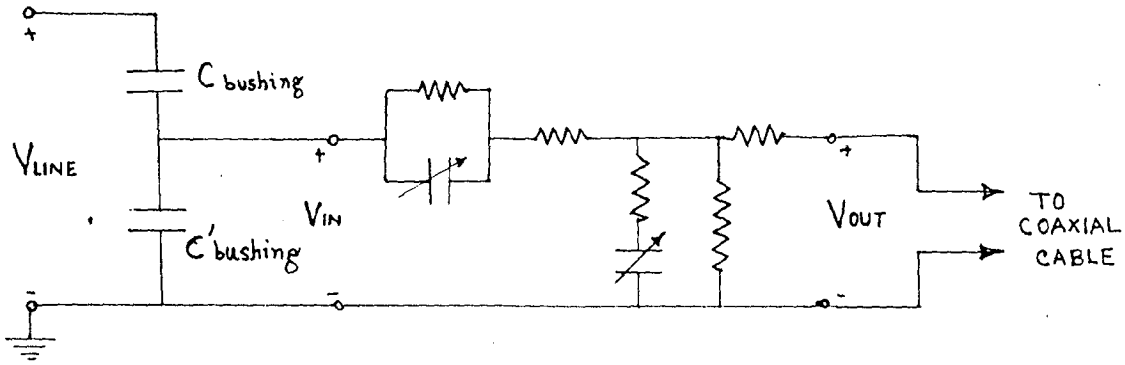


FIG. 1·2 TYPICAL POTENTIAL DIVIDER NETWORK, USING PASSIVE PROBE, CONNECTED TO BUSHING CAPACITANCE TAP.

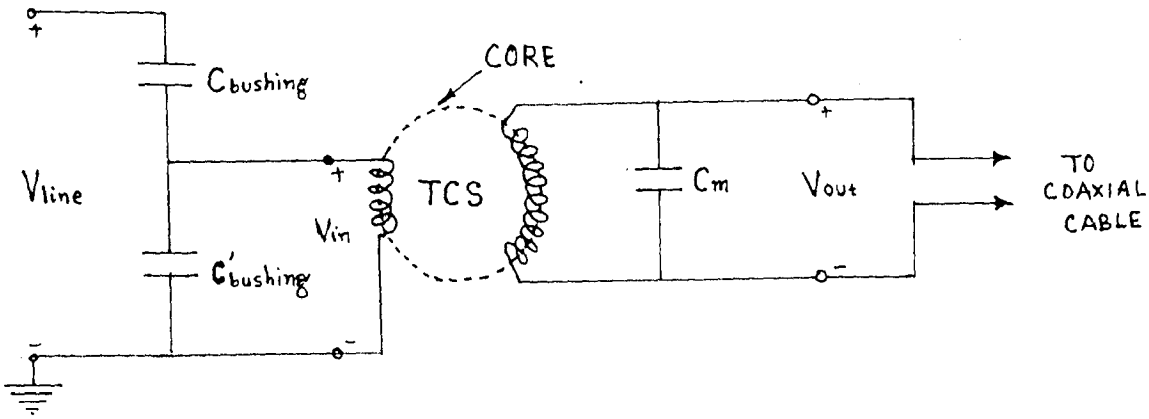


FIG. 1·3 BUSHING CAPACITANCE TAP DIVIDER NETWORK UTILIZING TRANSIENT COUPLING SENSOR (TCS)

and percentage oscillations in lightning currents can be made[10].

2.1.5 MEASUREMENT OF SWITCHING IMPULSE VOLTAGES USING TRANSIENT COUPLING SENSOR(TCS)

Capacitance voltage divider is the conventional means of measuring and recording voltage transients on high tension lines. In recent years the internal capacitance structures of high voltage bushings have served this purpose very well. Special passive probes with large input impedance have been used as an interface between the bushing capacitance tap and the recording cathode ray oscilloscope. These probes have very good response over a wide range of frequencies, but they are somewhat bulky in size for extensive use throughout a large transmission system on a continuing basis:and they comprise a relatively large number of sensitive elements which when exposed to harsh station environ-ments could be expected to require considerable maintenance over a long period of time. One other disadvantage of these probes is that the output is directly connected to the high voltage divider through impedance elements as shown in figure 1.2.

This limited isolation between primary and secondary represents a potentially hazardous condition.

An attractive alternative to the passive probe is the current transformer specially designed to provide a very low burden and to display excellent voltage transfer response over

a wide range of frequencies. The relative simplicity of this transient coupling sensor (TCS) is indicated in figure 1.3.

From the fig. 1.3 it can be seen that the output is completely isolated from the input. It is an important advantage from the point of view of equipment and personnel safety over extended period of operation. TCS has 3 inch length and $1\frac{1}{2}$ inch diameter. Because of its small size the TCS can be made an integral part of the bushing capacitance tap housing.[1].

2.1.6 DIGITAL IMPULSE RECORDER

Recording of non repetitive randomly occuring events is a major problem in high voltage measurements. Digital techniques potentially offer a convient solution to the problem. Specialized digital recorders can wait for a transient and, when it arrives, they will convert the analog signal into a series of digital words, store them in memory and again become ready for recording the next signal. The signal converted into digital form can be processed.

The recorder is designed as a mobile unit comprising an input attenuator compatible with impulse voltage dividers, an analog-to-digital converter Biomation 8100, an interface and a graphic computer terminal Tektronic 4051. The recorded impulses are displayed and can be printed or stored on magnetic tape. One of the main difficulties in applying digital instruments to measurement in H.V. laboratories and substations is the high electromagnetic interference of high voltage test areas, which

usually saturates the input circuits and erases the memory registers of commercially available A/D converters. This difficulty is overcome by using electromagnetic shielding.

This new apparatus has a sufficiently high time resolution to record the fastest microsecond impulses used for H.V. testing and also allows slower switching transients to be monitored.

The A/D converter offers some useful operating modes which are not available in impulse oscilloscopes;

(1) Pretriggering, which allows for recording the transients preceding the trigger signal.

(2) Double time base for recording at two different time sweeps changed at a selected instant, (e.g. expansion of an impulse superimposed on a power frequency signal).

(3) Time expanded display of an initial part of the recorded impulse, which eleminates the need for two measuring channels to display the lightning impulse front and tail with an adequate resolution.

The analog output of the converter can be displayed on a monitor screen in the form of curve.

2.1.7 AUTOMATIC OVERVOLTAGE RECORDER

The automatic over voltage recorders designed by Leningrad Polytechnical Institute, consisting of an electronic

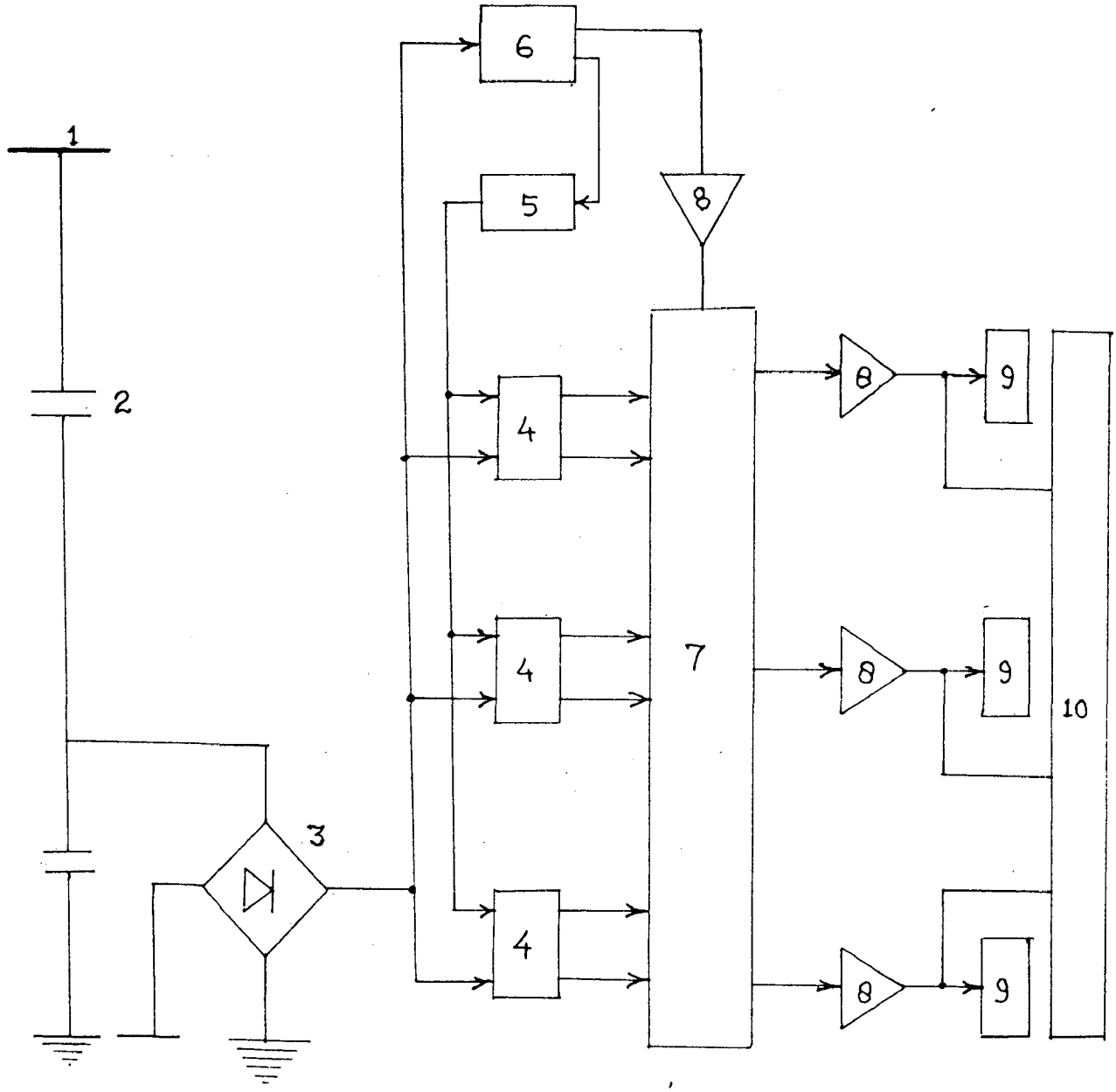


FIG. 1·4 BLOCK-DIAGRAM OF AUTOMATIC RECORDER OF OVERVOLTAGE LEBELS

oscillograph connected through a voltage divider and started by an overvoltage pulse are currently available. However, these recorders have a complicated design, they are not reliable in operation, require periodic maintenance, and do not meet the requirements of automatic recording. So these recorders are not oftenly used on 6-330 KV networks.

AzNITE has developed a reliable recorder for overvoltage pulses. The block diagram of the recorder is shown in fig.1.4.

1. High voltage conductor
2. Voltage divider
3. Rectifier
4. Adjustable trigger
5. Differential circuit
6. Monostable multivibrator
7. Decoder
8. Amplifier
9. Counter.

The recorder is powered by rectified voltage. The recording reliability is provided by the stability of the response elements, adjustable triggers as well as by recording selectivity of pulses.

The introduction of the recorder and the discrimination unit between the triggers and counters contributes the convenient interpretation of recorder indications, since the

overvoltage amplitude is recorded only when voltage exceeds the threshold.

The operating principles of the recorder are as follows. The recorder is set at the rated working voltage When an overvoltage pulse occurs on the conductor, the signal passes through the divider and bridge to enter the recorder input, causing a trigger. The threshold of triggers are set so that the trigger of each channel responds to the higher pulse of a higher amplitude than the other channels. The multivibrator, which interrogates the trigger, also starts from the overvoltage pulse. The interrogation pulse from multivibrator enters through the amplifier into the docoder and depending upon the quantity of operated triggers i.e. depending on the amplitude of the input pulse at the corresponding output of the decoder, the output pulse that is amplified by the amplifier appears and is sent to the counter of overvoltage level. The drop of the triggers to the reference position 0 , takes place on the falling edge of the pulse from the triggers from the multivibrator through the differentiating circuit.

2.1.8 MICROPROCESSOR BASED SURGE RECORDER:

In B.E. Project of university of Roorkee, only the magnitude of surge has been recorded. The surge of amplitude 4 volts has been generated from microprocessor. The block diagram of the arrangement is given in fig.1.5.

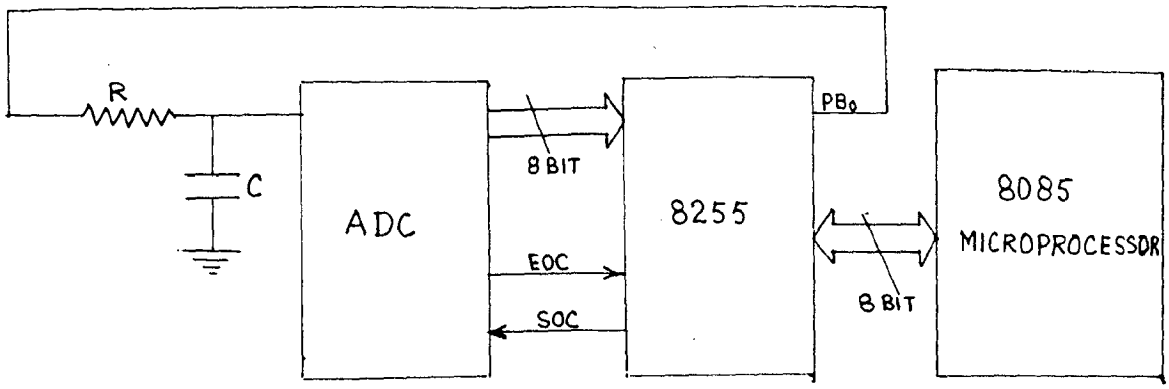


FIG.1·5 BLOCK DIAGRAM OF MICROPROCESSOR BASED SURGE MAGNITUDE RECORDER

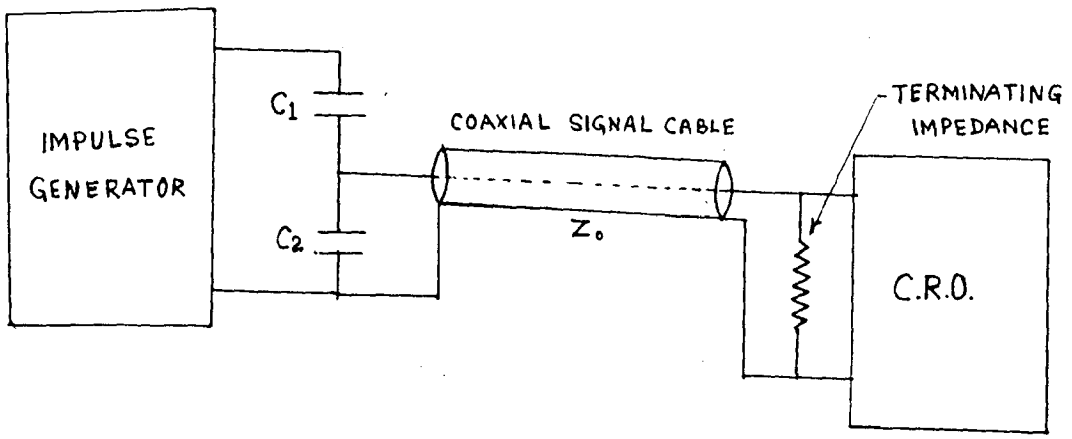


FIG.1·6 IMPULSE MEASUREMENTS USING C.R.O.

2.2 APPLICATION AND RESULTS OF THE VARIOUS TECHNIQUES OF MEASURING IMPULSE VOLTAGES

2.2.1 CATHODE RAY OSCILLOSCOPE:

To avoid from the induced voltages and stray pick-ups due to electromagnetic interference, it is necessary to arrange leads, layout and connections from the signal source to the CRO. For fast rising signals, the cables have to be accounted as transmission lines with distributed parameters. Cable has to be terminated by connecting a resistance equal to surge impedance of the cable in order to avoid from unnessary reflections at cable ends.

Oscilloscopes have finite impedance usually about 1 to 10M.Ohm resistance in parallel with a 10 to 50 PF capacitance. This impedance at high frequencies ($f \approx 100$ MHz) is about 80 ohms and thus acts as a load at the end of a surge cable. This load attenuates the signal at C.R.O. end.

The arrangement of the C.R.O. for measuring impulse signal is shown in fig.1.6.

2.2.2 DIGITAL IMPULSE RECORDER

For the simplification of the operation the program is divided into a few subroutines entitled "Impulse parameters", "Reading A/D converters", "Mag-tape storage", "Insert data" etc. which are called up by the user-definable keys of the terminal. For specialized tests new subroutines are developed, such as

"peak value," which displays the recorded peak values in digital from without retracing the same impulse form each time, or "curve smoothing," which eleminates the digitalization error on display.

The important advantages of digital recorders are the continuous display of single-shot transients, measurement of peak values, pretriggering, storage on magnetic tape. The most important characteristic of the digital recorder is its data processing capability. In addition, the computer terminal of the recorder can also be used for control of the impulse generator as well as for a variety of calculations such as field plotting and specification of the impulse generator parameters for a required impulse form.

Electromagnetic interference induced by impulse generators is the most important difficulty with these recorders.

2.2.3 AUTOMATIC SURGE RECORDER:

Automatic surge recorder is used to record the lightning as well as switching surges. The recorders can record the overvoltages on commutations in nearby substations when the direction of the power over current changes. Overvoltage caused by thunder storms, the during of which is sufficient for the start of recorders, can comprise the number of recorded ones; the amplitude of these voltages.

The device developed can record overvoltages of

six adjustable levels in the range (1.25 -7.5)U_f. These recorders are highly sensitive, fast in operation and reliable, so these can be used for the continuous over-voltage recording during a long period on a wide frequency range with high resolution.

2.2.4 MICROPROCESSOR BASED SURGE RECORDER

A surge of amplitude 4V, rise-time 1 ms and a tail time of 4 ms was generated. It was successfully stored in the memory of 8085A microprocessor after converting it to digital signals by analog to digital converter(ADC). It was possible to get 8-10 points on the front of the wave form and about 20-25 on the tail of the wave form.

With the help of microprocessor, the storing of switching surge magnitude has been carried out successfully.

CHAPTER 3

SIMULATION OF SURGES

Lighting surge is a natural phenomenon, while switching surges originate in the power system itself as a consequence of connection and disconnection of circuit breaker contacts or due to initiation or interruption of faults. Switching surges are highly damped short duration surges. Power frequency over voltage may also occur due to switching and fault clearing processes in power system. Although both switching and power frequency over-voltages have no common origin, they may occur together, and their combined effect is important from the point of view of insulation coordination.

Switching surges may be caused due to any of the following reasons -

(i) Deenergizing the transmission lines, cables, shunt capacitor banks etc.

(ii) Disconnection of unloaded transformers.

(iii) Reclosing of lines and reactive loads.

(iv) Sudden switching off of loads.

(v) Short circuits and fault clearances.

(vi) Resonance phenomenon like ferroresonence, arching grounds etc.

Magnitude, rise and fall time of overvoltage depends upon the system voltage, cause of over voltage. The magnitude of over voltage may go as high as six times the normal power frequency voltage. In circuit breaking operation, switching

surges with a high rate of rise of voltage may cause repeated restriking of the arc between circuit breaker contacts.[10]

Switching surges are irregular (oscillatory or unipolar) and can be of high frequency or power frequency with its harmonics. These may also be considered as a slow rising impulse having a wave front time of .1 to 10 m sec. and tail time of one to several m seconds.

Impulse and high frequency a.c. measurements are done with the help of potential dividers. For power frequency a.c. measurements the divider may be pure resistance divider, but due to power loss in resistance divider, capacitor voltage divider is preferred, moreover for high resistances, the variation of resistance with temperature is a problem. High resistance units for high voltages have stray capacitances. So for the measurement of high frequency voltages capacitor voltage dividers are used extensively. For recording fast and slow transients the damped capacitive divider (series resistance-capacitance divider) obtained by adding resistor units in series with capacitor units is used.

3.1 SIMULATION OF SWITCHING SURGES

Now a days in extra high voltage transmission lines and power system, switching surge is an important factor from the point of view of insultation design of various equipments. The waveform of such surges is not unique. Several circuits have been adopted for simulating switching surges. They are grouped

as (i) impulse generator circuit modified to give longer duration wave shapes, (ii) power transformers or testing transformers excited by d.c. voltages giving oscillatory waves.[10]

Figure 3.1 shows the impulse generator circuit modified to give switching surges. The values of R_1 and R_2 are increased to several Kiloohms to give surge having long duration waveshape of the order of miliseconds. Generally, for a given impulse generator, capacitance C_1 and load capacitance C_2 will be fixed depending on the design of the generator and the test object. By controlling the values of R_1 and R_2, desired waveshape is obtained. To calculate the wave front and wavetail times the following approximate analysis is used.

The resistance R_2 will be large. Taking the circuit inductance to be negligible during charging, C_1 charges the load capacitance C_2 through R_1. Then the time taken for charging is approximately three times the time constant of the circuit and is given by

$$t_1 = 3.0\, R_1 \frac{C_1 C_2}{C_1 + C_2} = 3\, R_1 C_e$$

where $$C_e = \frac{C_1 C_2}{C_1 + C_2} .$$

For tail time calculation, capacitances C_1 and C_2 may be considered to be in parallel and discharging occurs

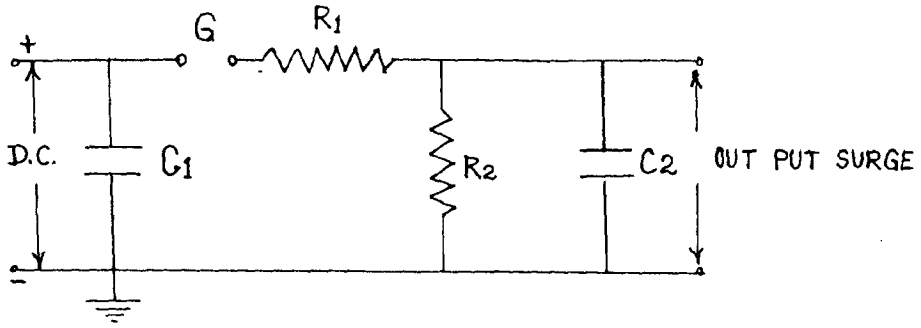


FIG. 3·1 CIRCUIT FOR PRODUCING SWITCHING SURGE

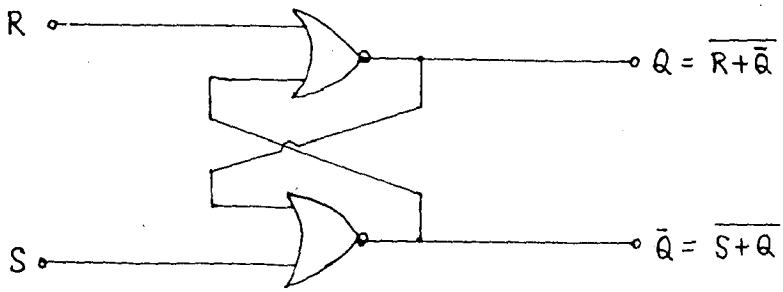


FIG. 3·2 RS FLIP-FLOP USING NOR GATES

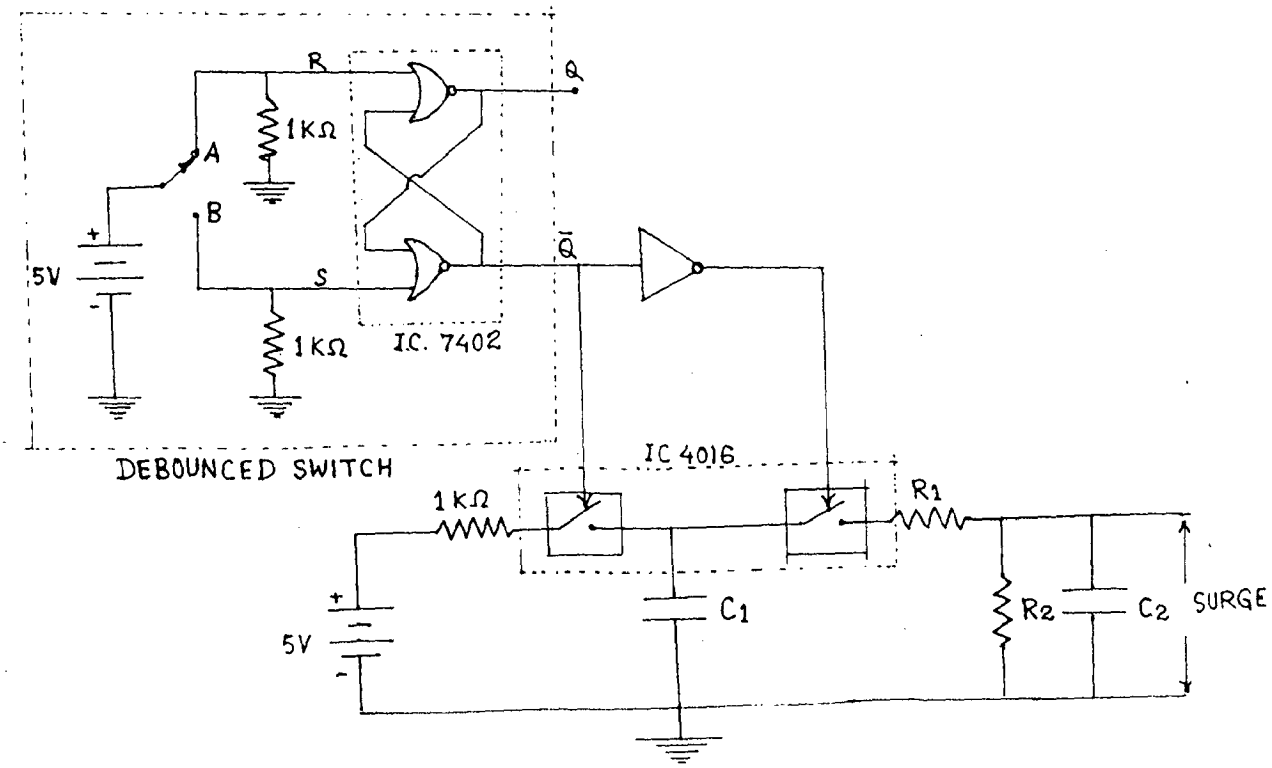


FIG. 3·3 SWITCHING SURGE GENERATOR USING DEBOUNCED SWITCH

through R_1 and R_2. The approximate tail time is given by

$$t_2 = 0.7(R_1 + R_2)(C_1 + C_2)$$

With these approximate formulae, the wave front and wave tail times can be estimated to within ± 20 percent.

In figure 3.1 G stands for spark gap. To avoid from the high voltage work, the switching surge is simulated at low voltage impulse generator. Input voltage to Analogue to Digital converter can be upto 5 volts. Spark gap can not be used at such low voltage.[10].

In hand-operated push-button switch, there is bouncing which effects the output of impulse generator. So it is necessary to use debounced switch.

3.1.1 DEVELOPMENT OF DEBOUNCED SWITCH:

A hand-operated switch can be debounced using RS flip flop. The two terminals of RS flip flop are called the SET S and RESET R inputs. The signals applied to the S and R terminals are control inputs (often called data inputs). The circuit diagram of RS flip flop using NOR gates is given in Fig 3.2.

The truth table for this flip flop is given below

	S	R	Q_{n+1}
	0	0	Q_n
Reset state →	0	1	0
set state →	1	0	1
	1	1	Not allowed

Consider that S = R = 0, as in the first row of the truth table. For these particular inputs the circuit has two stable states, $Q = 1(\bar{Q} = 0)$ or $Q = 0(\bar{Q} = 1)$ and as long as S = R = 0, the NOR gates are not affected by the control inputs and the state of RS flip-flop will not change. In the truth table notation is to be interpreted as follows

Q_n = Value of Q before S = R = 0 condition was imposed.

Q_{n+1} = Value of Q after S = R = 0 condition was imposed.

The subscripts n and n+1 are used because there will in general numerous times during which the control inputs will change.

Now assume that S = 0 and R = 1, from the circuit we see that the output of the upper NOR gate will be

$$Q = \overline{R + \bar{Q}} = \overline{1 + \bar{Q}} = \bar{1} = 0$$

Since the two inputs to the lower NOR gate are 0, that is, Q = 0 and S = 0, its output is

$$\bar{Q} = \overline{S + Q} = \overline{0 + 0} = 1$$

Thus the only possible state for this combination of control inputs is $Q = 0$ $(\bar{Q} = 1)$. This stat is called the reset state.

In order to achieve the set state we must have S = 1 and R = 0. Then since S = 1, the output of lower NOR gate will be

$$\bar{Q} = \overline{S + Q} = \overline{1 + Q} = 0$$

and the output of the upper NOR gate will be

$$Q = \overline{R + \overline{Q}} = \overline{0 + 0} = 1$$

3.1.2 GENERATION OF SWITCHING SURGE USING DEBOUNCED SWITCH:

Fig.3.3 shows the complete circuit diagram of surge generator. The pin configuration of I.C. 7402 and 4016 is given in appendix 1. 7402 is a Quad two input NOR gate and 4016 is a Quad bilateral switch. The output of RS flip flop is directly connected to the I.C. 4016 as control signal to control the bilateral switch used for charging the capacitance C_1 and to control the switch used for discharging the capacitance C_1 in load capacitance C_2, the control signal is achieved by NOT gating the R.S. flip flop output.

CHAPTER 4

MICROPROCESSOR BASED SURGE RECORDING

As the process of miniaturisation of electronic components proceeded, the microprocessor came into being, with the help of which we can achieve difficult tasks at low cost. So it should be possible to record voltage surges in power system with the help of microprocessor based surge recorder.

4.1 DEVELOPMENT OF MICROPROCESSOR BASED SURGE RECORDER

In B.E. project of this university, only the magnitude of the switching surge generated from microprocessor itself has been recorded. The proposed work for this thesis is to record the magnitude and time of surges generated in power system. For this purpose a microprocessor based on-line surge recorder has been developed.

4.1.1 RECORDING OF SURGE GENERATED FROM MICROPROCESSOR

The hardware and software for recording the magnitude and time of the surge has been developed. The surge is generated by integrating the pulse generated from microprocessor. The block diagram for recording such surge is given in fig.4.1. Analogue voltage is converted in to digital wave by analogue to Digital Converter ADC 0809.

8255 Chip: It is a programmable peripheral interface designed to use with 8085 microprocessor. This basically acts as a general purpose I/O component to interface peripheral equipments

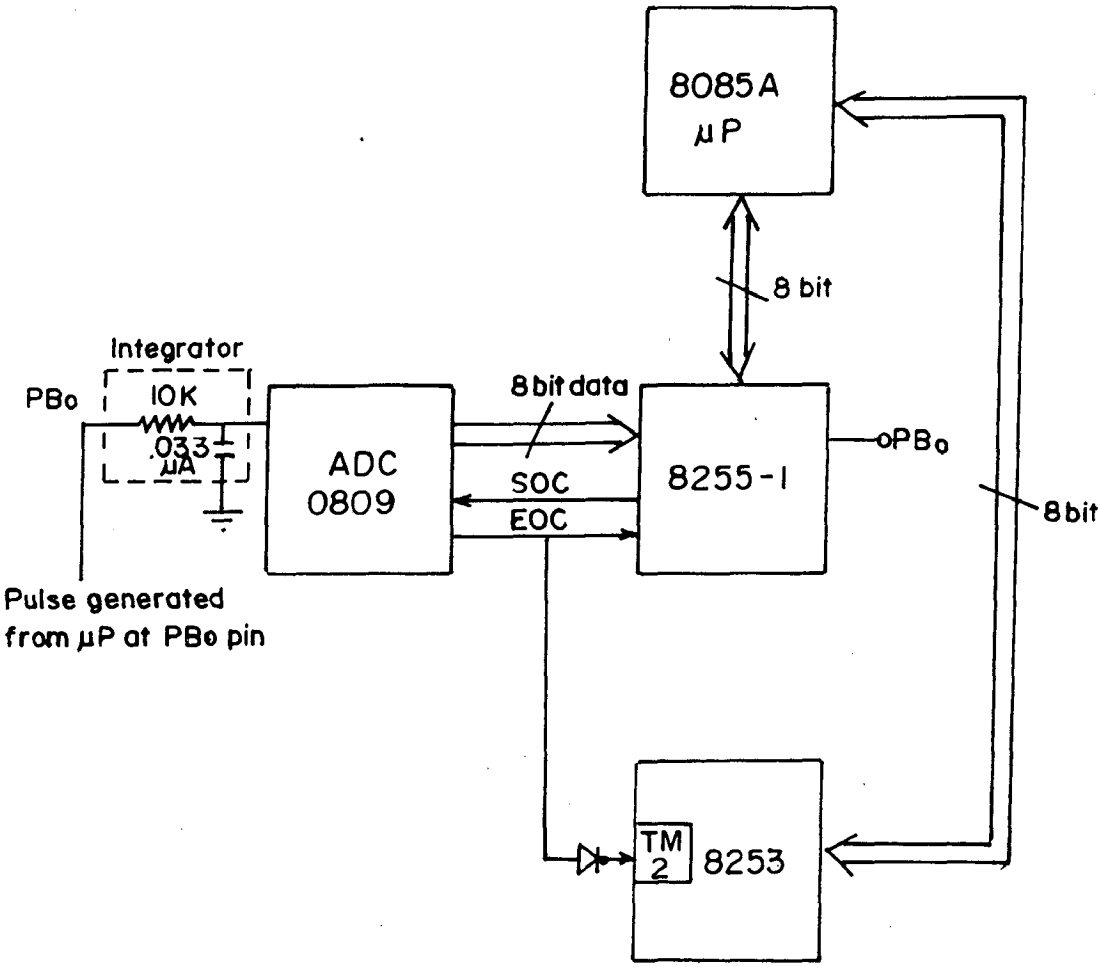
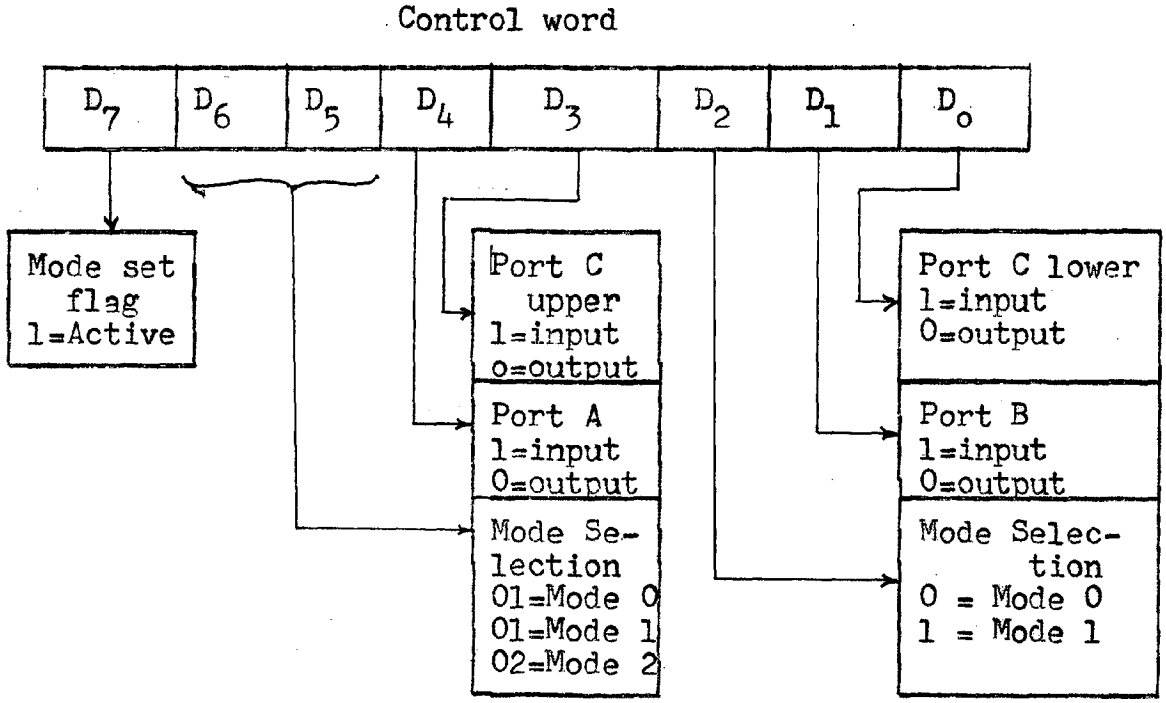


FIG.4.1 BLOCK DIAGRAM FOR RECORDING SURGE GENERATED FROM MICROPROCESSOR ITSELF.

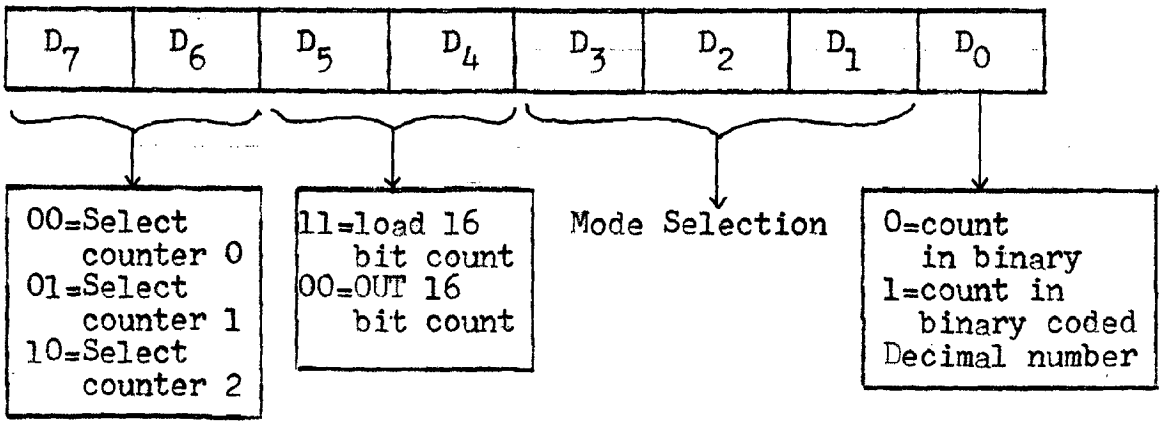
to the system bus. It is not necessary to have an external logic to interface with peripheral devices since the functional configuration of 8255 is programmed by system software. It has three I/O ports of 8 lines each (Port A, Port B and Port C). Port C can be divided into two ports of 4 lines each named as Port C upper and Port C lower. Any I/O combination of these ports can be defined using the appropriate soft ware commands. Mode Defination format for 8255 chip is given.



Various port addresses for different port numbers of 8255 chip are given below

Port/Register	Address
Port A	00
Port B	01
Port C	02
Control word Register (CWR)	03

8253 Chip : This chip is a programmable interval timer/counter and can be used for the generation of accurate time delays under software control. Various other functions that can be implemented with this chip are programmable rate generator. Event counter, Binary rate multiplier, real time clock etc. This chip has got three independent 16 bit counters each having a count rate of upto 2 MHz. The first timer/counter (i.e. counter 0) is being used for single step operation. The second timer/counter (i.e. counter 1) is being used for generating programmable band rate while using 8251. However, its connections are also brought at connector J_1. The third timer/counter (counter 2) is brought at connector space J_2. For single step operation CLK 0 signal of counter 0 is getting a clock frequency of 1.535 MHz. To facilitate the use of timer/counter-2 of 8253, CLK0, GATE0, CLK2 and GATE2 are brought out on board of VMC-85/9 alongwith the V_{cc} and GND. Using jumpers a 1.535 MHz clock can be assigned to CLK2 and GATE2 can also be connected to V_{cc} or GND. Mode defination format for 8253 is given below -



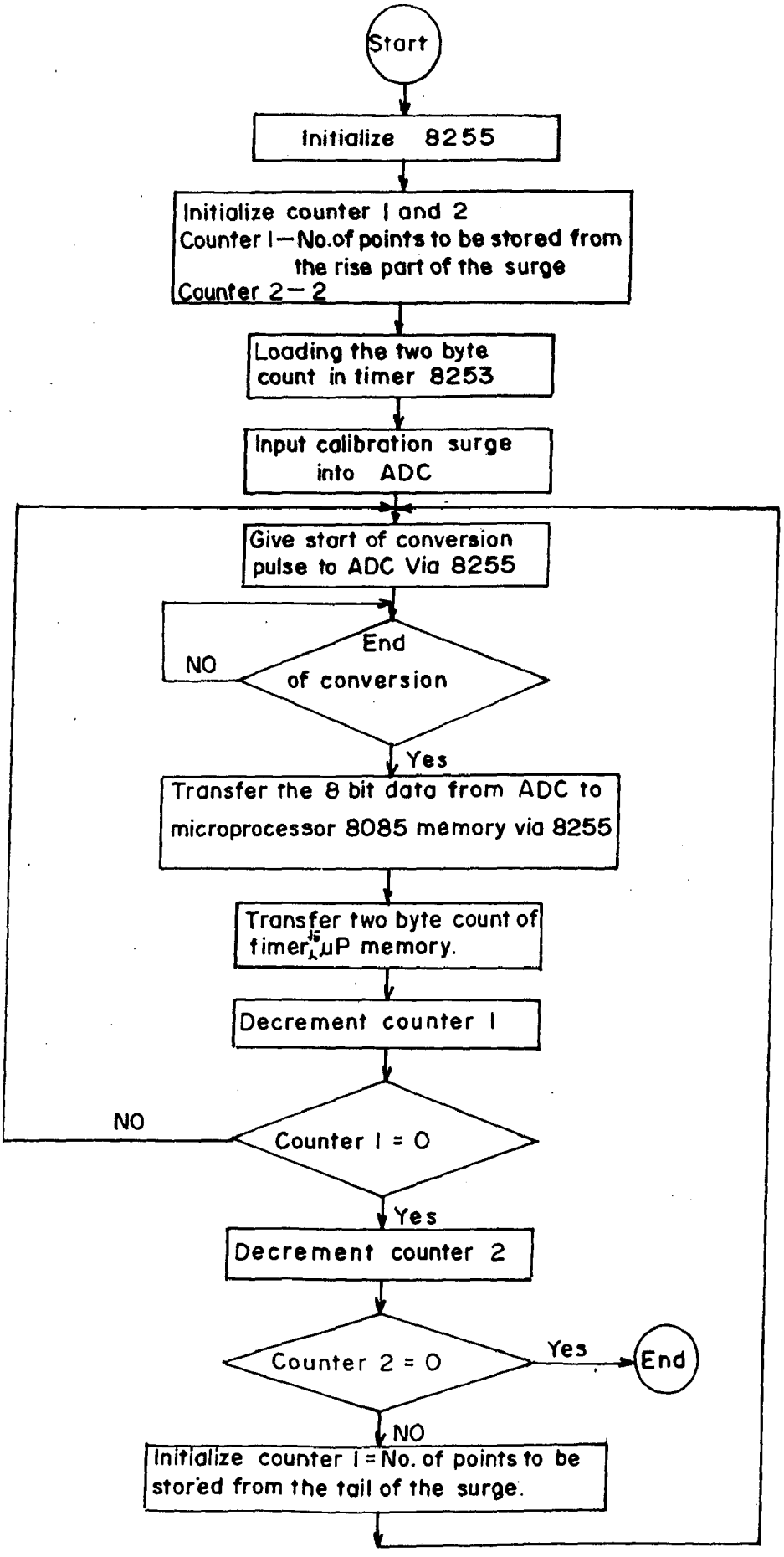


FIG.4.2 FLOW CHART FOR RECORDING SURGE GENERATED FROM MICROPROCESSOR ITSELF.

Various addresses for different timer/counter are given below -

Timer/Counter	Address
0	10 H
1	11 H
2	12 H
Control word Register (CWR)	13 H

The pin configuration of 8255 and 8253 and the pin numbers at connector J_1 and J_2 are given in Appendix 2. The flow diagram of the software implemented for recording the surge is given in fig. 4.2. The software implemented is given below -

Lebel	Address	Contents	Mnomenic and operand field	Comment field
	2000	21 70 20	LXI H,2070	To lead HL register pair with 2070 H
	2003	3E 98	MVI A,98H	To initialize 8255
	2005	D3 03	OUT 03H	
	2007	0E 02	MVI C,02H	Counters initialization
	2009	06 0A	MVI B,0AH	
	200B	3E BD	MVI A,BO	load the timer 2
	200D	D3 13	OUT 13H	with 6978 H
	200F	3E 78	MVI A,78H	BO→Control word
	2011	77	MOV M,A	12H→Address of Timer 2
	2012	23	INX H	13 →Address of
	2013	D3 12	OUT 12H	control word
	2015	3E 69	MVI A,69H	Register
	2017	77	MOV M,A	
	2018	23	INX H	
	2019	D3 12	OUT 12H	

	201B	3E 00	MVI A,00	PB_0 is made low to
	201D	D3 01	OUT 01	high to generate the
	201F	3C	INR A	surge
	2020	D3 01	OUT 01	
LP3	2022	3E 00	MVI A,00	Start of Conversion
	2024	D3 02	OUT 02	pulse at PC0.
	2026	3C	INR A	
	2027	D3 02	OUT 02	
	2029	3D	DCR A	
	202A	D3 02	OUT 02	
LP1	202C	DB 02	IN 02	
	202E	E6 10	ANI 10	End of conversion
	2030	C2 2C 20	JNZ LP1	pulse at PC4
LP2	2033	DB 02	IN 02	
	2035	E6 10	ANI 10	
	2037	CA 33 20	JZ LP2	
	203A	DB 00	IN 00	Loading of
	203C	77	MOV M,A	digital waveform
	203D	23	INX H	in memory of μP
	203E	3E 80	MVI A,80	
	2040	D3 13	OUT 13H	Loading of two
	2042	DB 12	IN 12H	byte count of
	2044	77	MOV M,A	Timer 2 in
	2045	23	INX H	memory of μP
	2046	DB 12	IN 12H	
	2048	77	MOV M,A	
	2049	23	INX H	
	204A	05	DCR B	Decrement counter B
	204B	C2 22 20	JNZ LP3	
	204E	0D	DCR C	
	204F	CA 5B 20	JZ LP4	
	2052	3E 00	MVI A,00	PB_0 made
	2054	D3 01	OUT 01	low
	2056	06 50	MVI B,50H	
	2058	C3 22 20	JMP LP3	
LP4	205B	EF	RST 5	

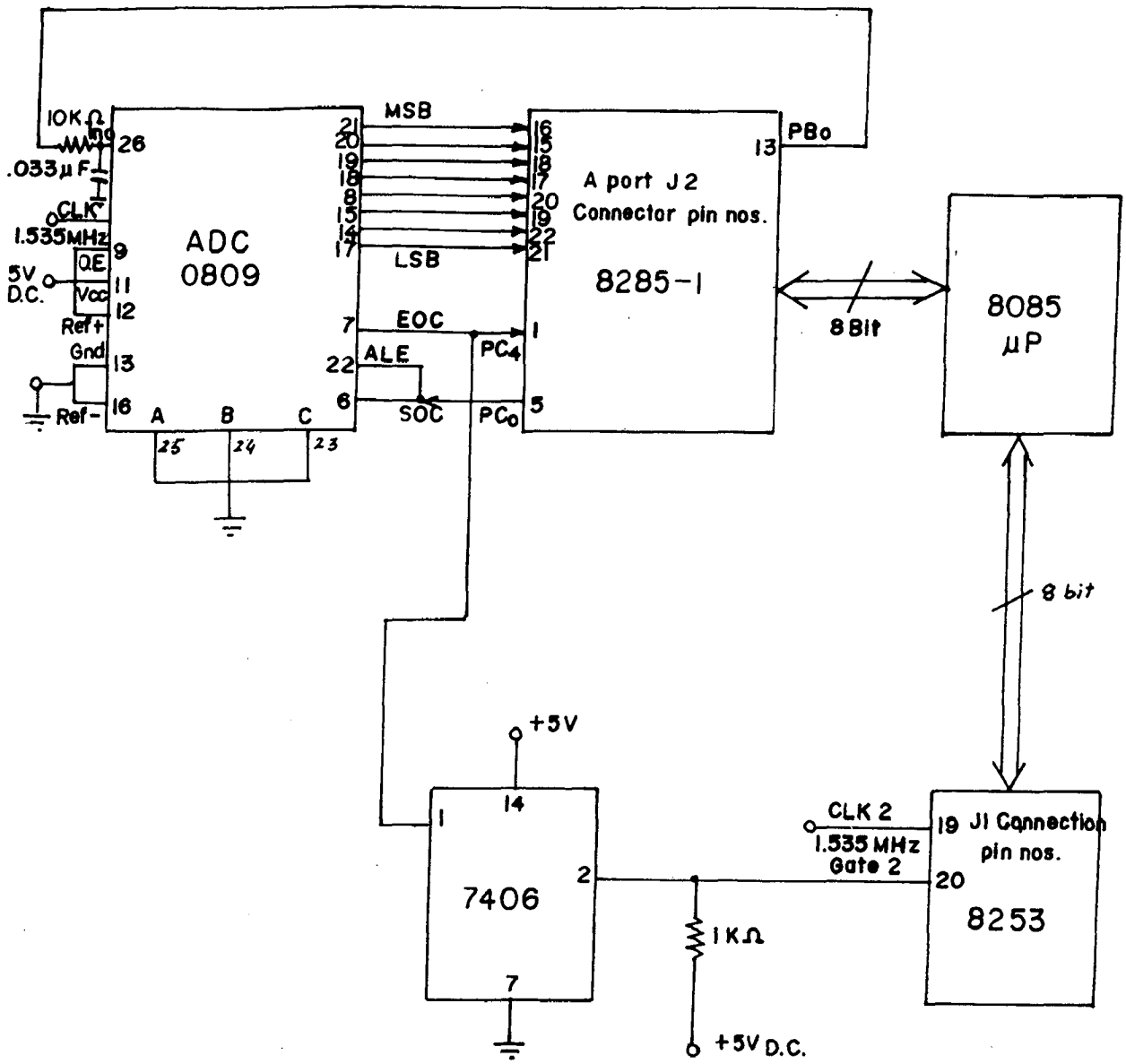


FIG.4.3 CIRCUIT DIAGRAM OF SURGE RECORDER WITH SURGE GENERATION BY MICROPROCESSOR.

Complete circuit diagram of surge recorder is given in fig 4.3. Observations and results of this recorder are given in next chapter.

4.1.2 RECORDING OF SURGE GENERATED BY IMPULSE GENERATOR ON RECEIVING SINGAL FROM MICROPROCESSOR

In the last section, surge was generated from microprocessor and then recorded, since the surges generated in power system are to be recorded, the next developmental stage is to record the surge generated externally (by impulse generator). Surge has been generated by impulse generate as it receives signal from microprocessor, and then recorded by microprocessor based surge recorder. The block diagram of this type of surge recording process is given in fig.4.4. In figure 4.4, surge generator receives signal from the microprocessor and then it generates the surge. The generated surge is converted in to digital wave by ADC 0809 and then recorded. To record the time, 8253 chip is used.

The flow diagram of software implemented is given in fig. 4.5. The software is given below -

Lebel	Address	Contents	Mnemonic and Operand field	Comments
	2000	21 70 20	LXI H,2070	
	2003	3E 98	MVI A,98H	To initialize
	2005	D3 03	OUT 03H	8255
	2007	3E B0	MVI A,B0	
	2009	D3 13	OUT 13H	

	200B	3E FF	MVI A,FF	To load the counter 2 with
	200D	77	MOV M,A	FFFFH
	200E	23	INX H	12H→address of Timer/counter 2
	200F	D3 12	OUT 12H	13H→address of CWR
	2011	3E FF	MVI A,FF	
	2013	77	MOV M,A	
	2014	23	INX H	
	2015	D3 12	OUT 12H	
	2017	3E 01	MVI A,01	
	2019	D3 01	OUT 01	
	201B	06 FF	MVI B,FF	To generate the surge
LP1	201D	05	DCR B	
	201E	C2 1D 20	JNZ LP1	
	2021	3E 00	MVI A,00	
	2023	D3 01	OUT 01	
LP4	2025	3E 00	MVI A,00	
	2027	D3 02	OUT 02	Start of conversion pulse
	2029	3C	INR A	at PC_0
	202A	D3 02	OUT 02	
	202C	3D	DCR A	
	202D	D3 02	OUT 02	
LP2	202F	DB 02	IN 02	
	2031	E6 10	ANI 10	End of conversion pulse
	2033	C2 2F 20	JNZ LP2	at PC_4
LP3	2036	DB 02	IN 02	
	2038	E6 10	ANI 10	
	203A	CA 36 20	JZ LP3	
	203D	DB 00	IN 00H	Transfer of 8 bit data to
	203F	77	MOV M,A	μP memory
	2040	23	INX H	
	2041	3E 80	MVI A,80	Loading of two byte count
	2043	D3 13	OUT 13H	of timer/counter 2 in to
	2045	DB 12	IN 12H	memory of microprocessor
	2047	77	MOV M,A	
	2048	23	INX H	
	2049	DB 12	IN 12H	
	204B	77	MOV M,A	
	204C	23	INX H	
	204D	C3 25 20	JMP LP4	

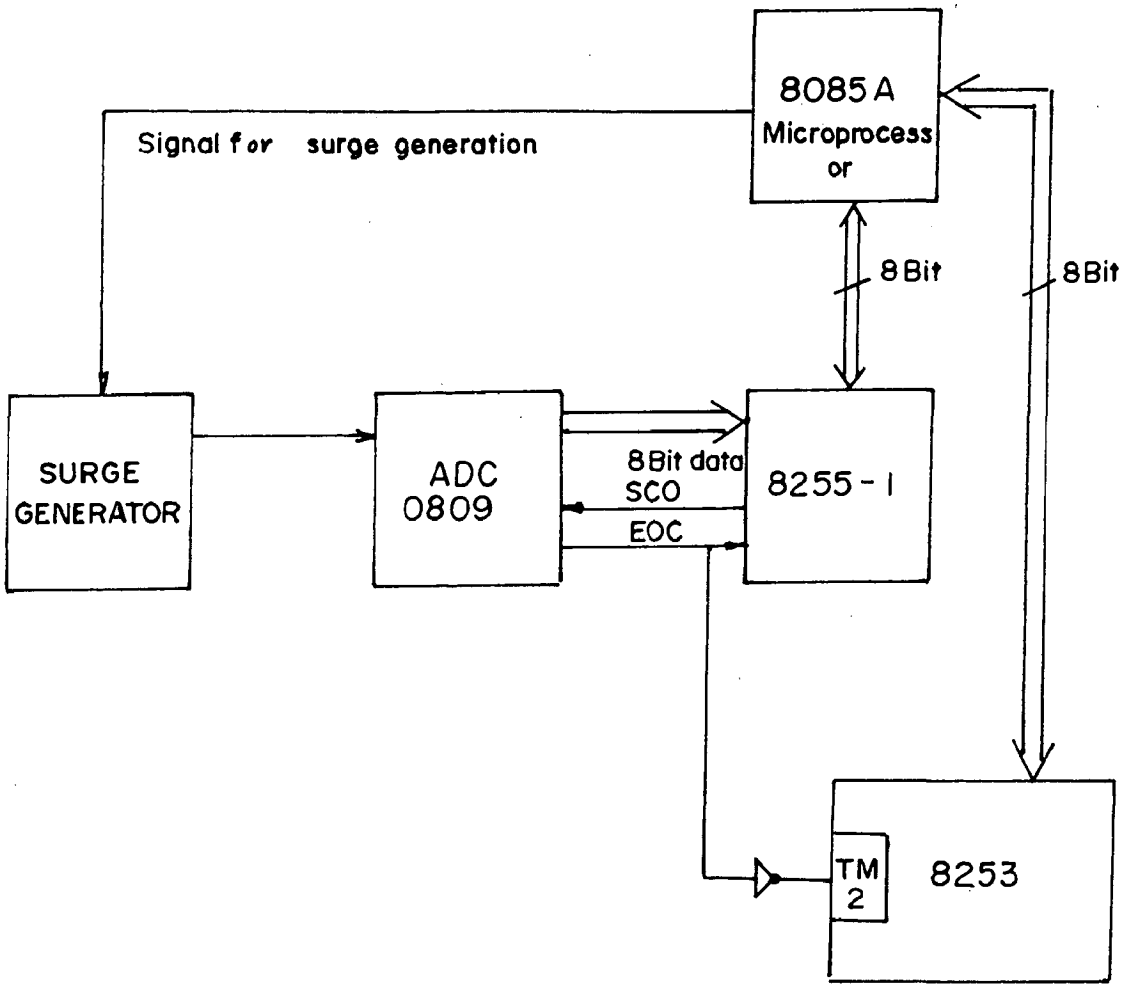


FIG.4.4 BLOCK DIAGRAM OF SURGE RECORDER WHEN SURGE GENERATOR RECEIVES SIGNAL FROM MICROPROCESSOR TO GENERATE THE SURGE.

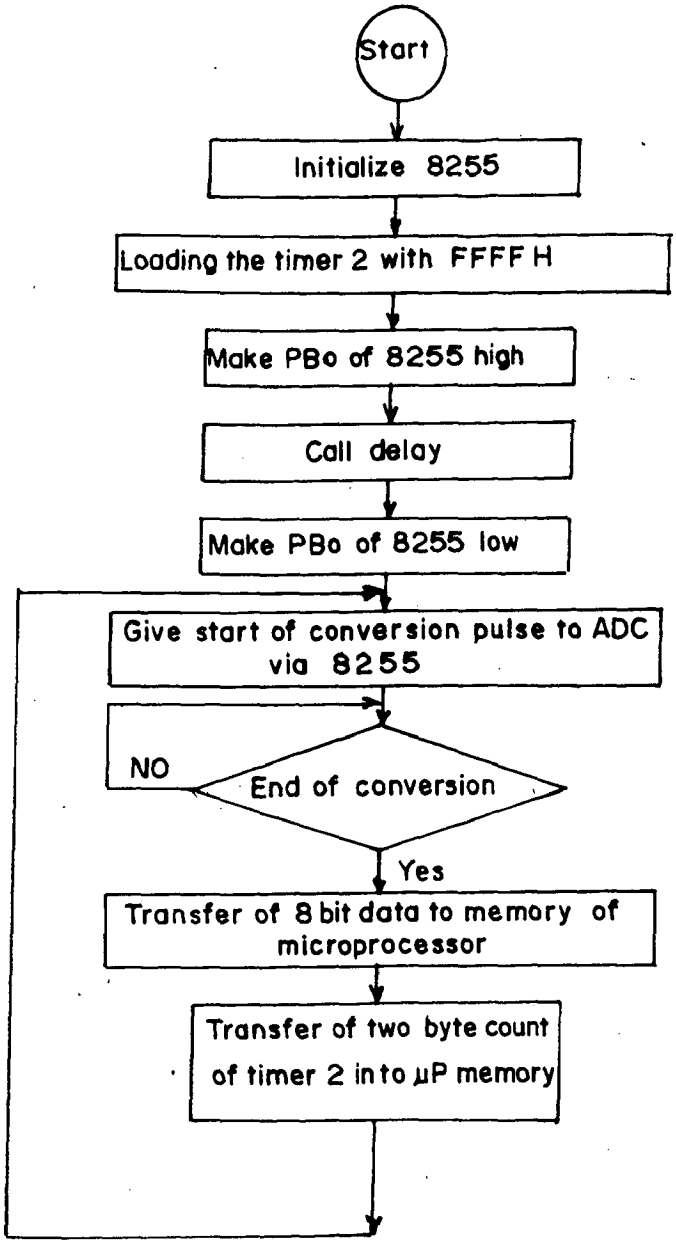


FIG.4.5 FLOW CHART OF SURGE RECORDING WHEN SURGE GENERATOR RECEIVES SIGNAL FROM MICRO-PROCESSOR TO GENERATE THE SURGE.

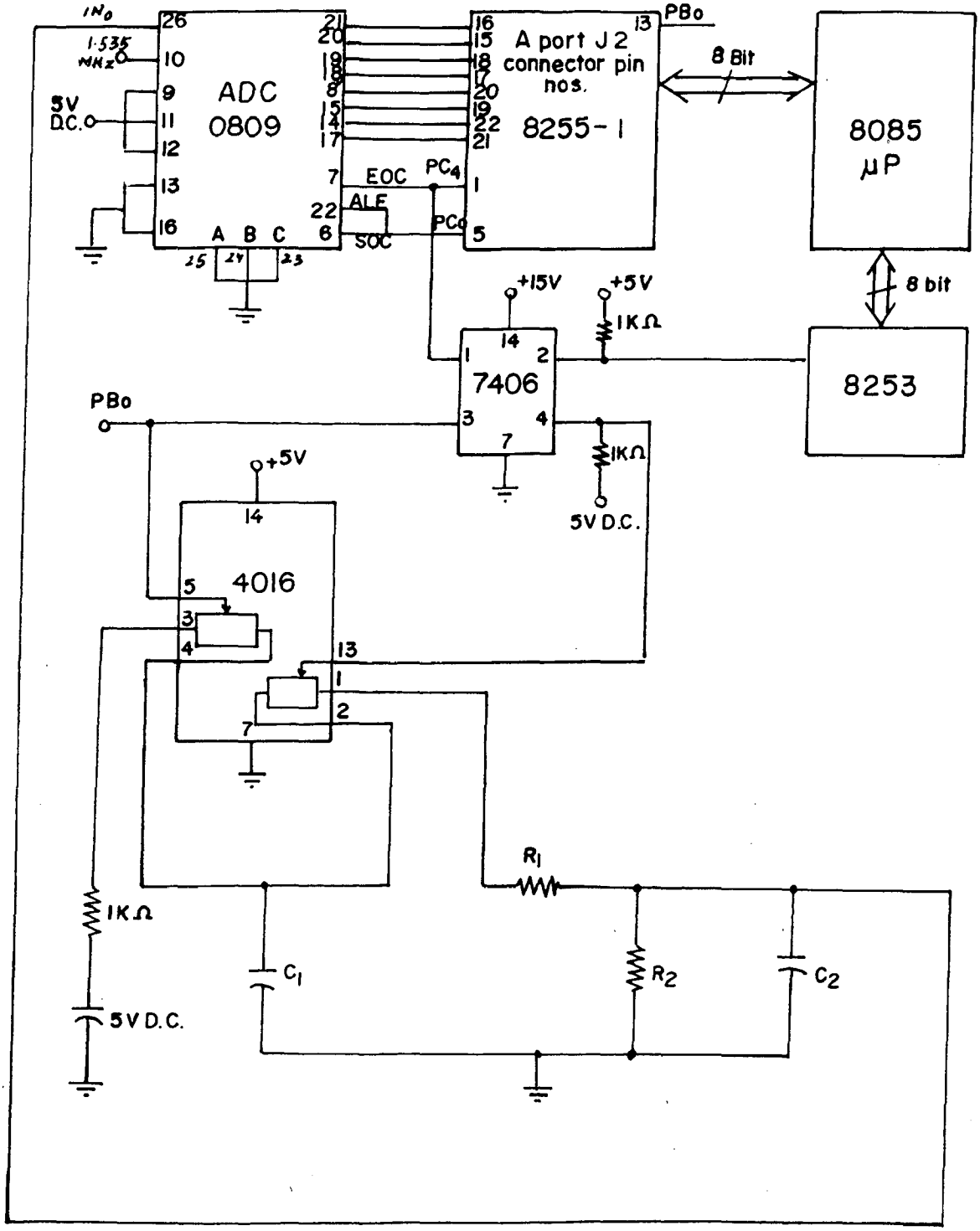


FIG.4.6 CIRCUIT DIAGRAM OF SURGE RECORDER WHEN SURGE GENERATOR RECEIVES SIGNAL FROM MICROPROCESSOR TO GENERATE THE SURGE.

The complete circuit diagram is given in fig 4.6. Observations and results are given in next chapter.

4.1.3 ON-LINE SURGE RECORDING

The next developmental stage of surge recorder is to record the surge generated by surge generator. Surge generator gives signal to microprocessor that surge has been generated. As the microprocessor receives signal it starts recording. So it is called on-line surge recording. On line surge recorder has been developed, the block diagram of which is given in fig 4.7.

In the surge recorders developed in last sections there was provision only for counter to down count during the conversion period of the analogue to digital converter (ADC). The time lost during the execution of the statements was not considered. But in on line surge recorder there is continuous down counting of timer as soon as microprocessor enters the interrupt subroutine. Fig 4.8 shows the flow diagram of the software implemented for on line surge recording. The software is given below -

Lebel	Address	Contents	Mnemonic and Operand field	Comments
	2000	21 70 20	LXI H,2070	
	2003	3E 98	MVI A,98	To initialize
	2005	D3 03	OUT 03H	8255
	2007	3E B0	MVI A,B0	
	2009	D3 13	OUT 13H	Loading of two byte count
	200B	3E FF	MVI A,FF	FFFF in Timer 2

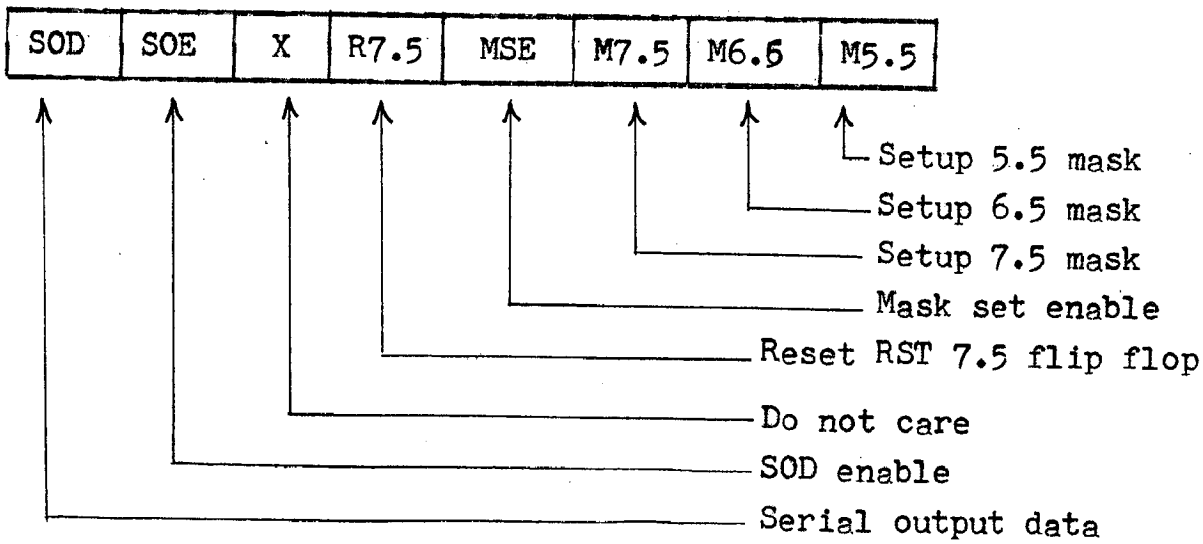
	200D	77	MOV M,A	
	200E	23	INX H	B0 → control word
	200F	D3 12	OUT 12H	12H→ Address of timer 2
	2011	3E FF	MVI A,FF	13H→ Address of CWR.
	2013	77	MOVE M,A	
	2014	23	INX H	
	2015	D3 12	OUT 12H	
	2017	3E 0D	MVI A,0D	Unmask RST 6.5
	2019	30	SIM	
LP1	201A	FB	EI	Enable interrupt
	201B	76	HLT	
	201C	C3 1A 20	JMP LP1	
				INTERRUPT SUBROUTINE STARTS
	0034	C3 B7 27	JMP 27B7	
	2787	C3 30 20	JMP 2030	
	2030	3E 01	MVI A,01	To make PB_0 high
	2032	D3 01	OUT 01	
	2034	3E 00	MVI A,00	
	2036	D3 02	OUT 02	Start of conversion pulse
	2038	3C	INR A	at PC_0
	2039	D3 02	OUT 02	
	203B	3D	DCR A	
	203C	D3 02	OUT 02	
LP2	203E	DB 02	IN 02 H	
	2040	E6 10	ANI 10	End of conversion pulse at
	2042	C2 3E 20	JNZ LP2	PC_4
LP3	2045	DB 02	IN 02H	
	2047	E6 10	ANI 10	
	2049	CA 45 20	JZ LP3	
	204C	DB 00	IN 00H	
	204E	77	MOV M,A	Transfer of 8 bit data to
	204F	23	INX H	µPmemory
	2050	3E 80	MVI A,80	
	2052	D3 13	OUT 13H	Loading of two byte count of
	2054	DB 12	IN 12H	timer in to µP memory
	2056	77	MOVE M,A	
	2057	23	INX H	

2058	DB 12	IN 12H	
205A	77	MOV M,A	
205B	23	INX H	
205C	C9	RET	Return

Complete circuit diagram of on line surge recorder is given in fig 4.8.

RST 6.5: The RST 6.5 input is connected directly to AND gate. Therefore, we need a sustained high level at pin no.8 of 8085 microprocessor to enable the RST 6.5 AND gate When RST 6.5 goes high, microprocessor enters the interrupt subroutine programme. RST 6.5 is maskable interrupt.

SIM Instruction: It is an interrupt instruction stands for set interrupt mask. To use this instruction we have to first load the accumulator as shown below -



By executing SIM instruction accumulator contents will be transferred to the appropriate locations.

In our on line surge recording software we have to

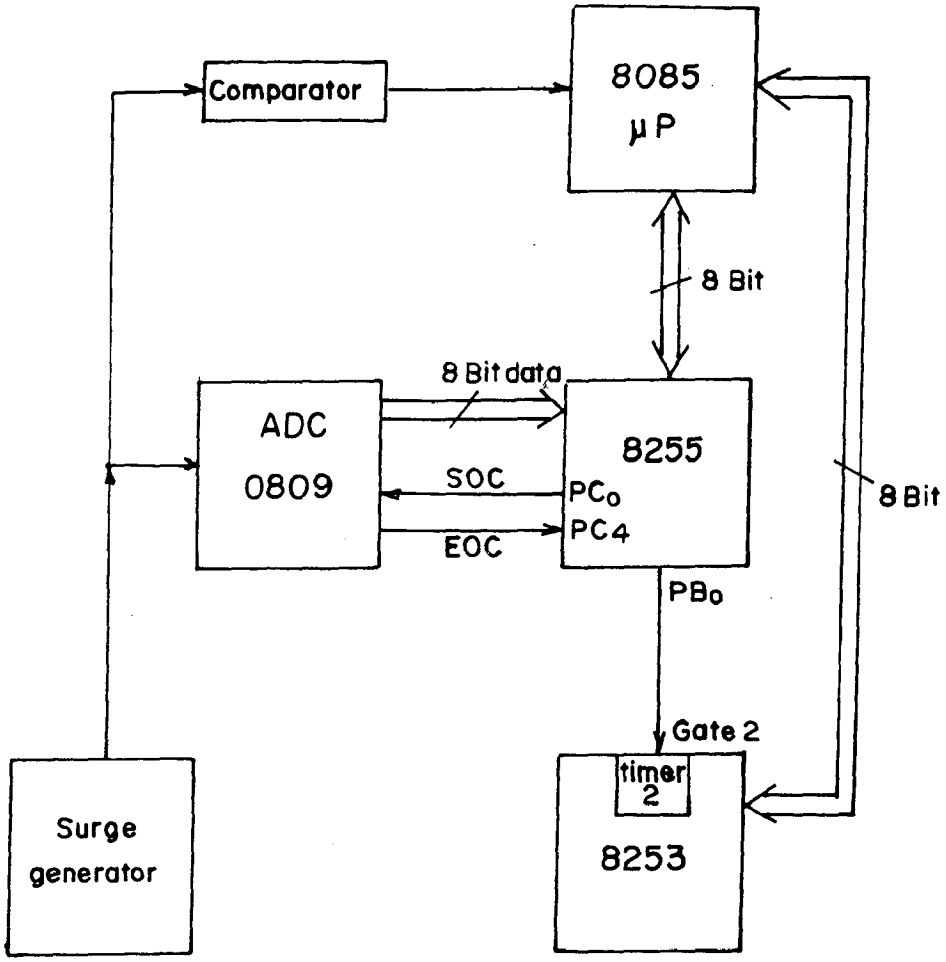


FIG.4.7 BLOCK DIAGRAM OF ON-LINE SURGE RECORDER.

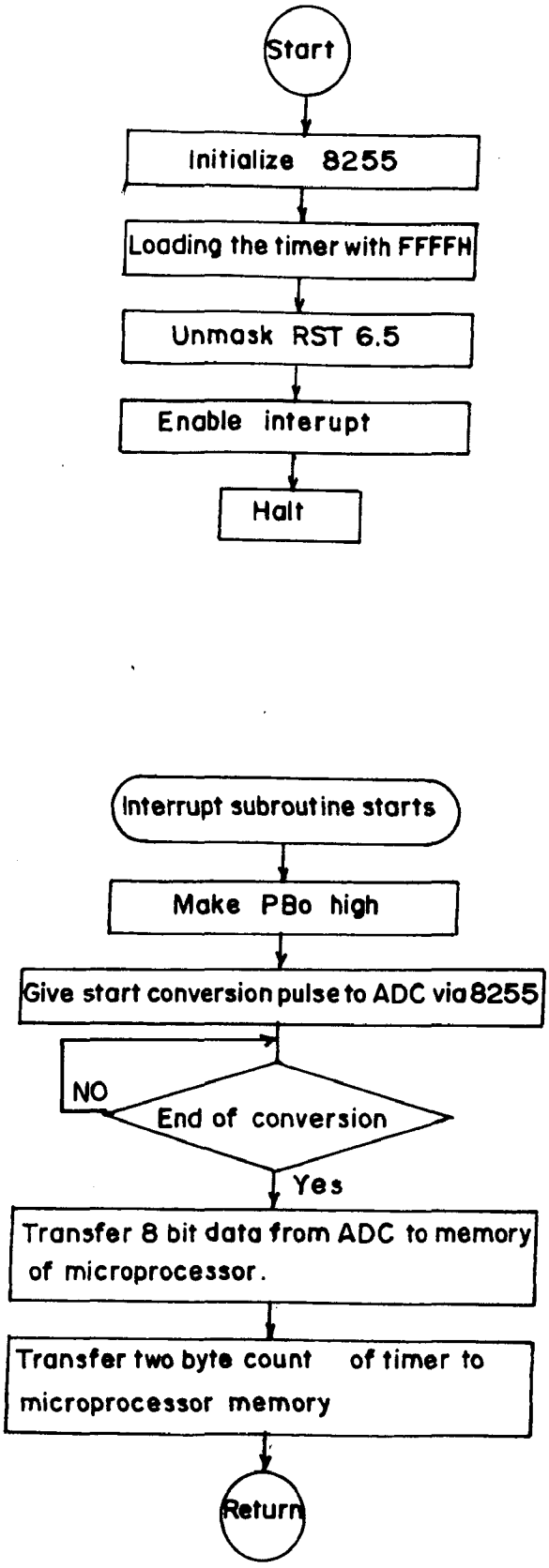


FIG.4.8 FLOW CHART OF ON-LINE SURGE RECORDING.

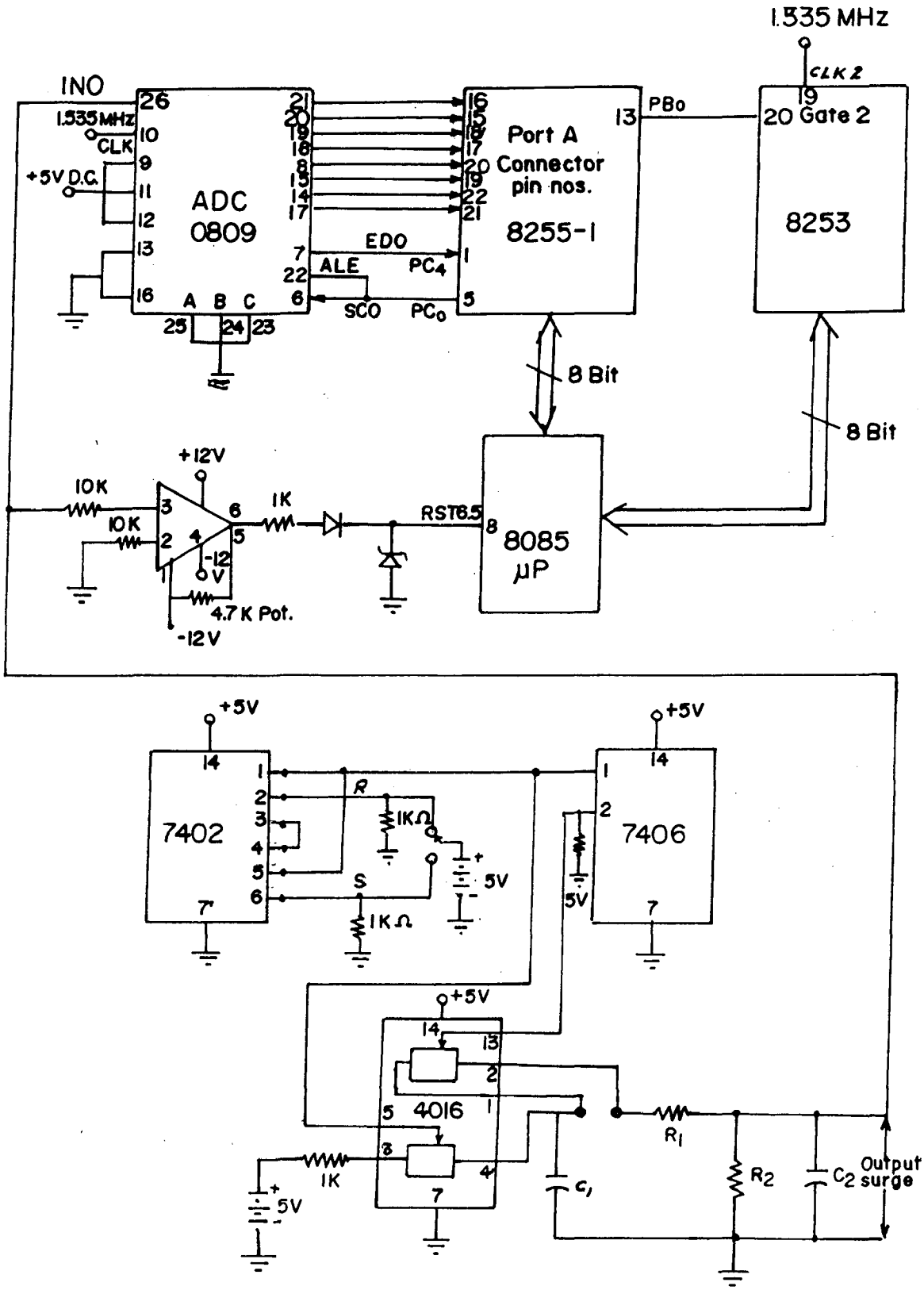


FIG.4.9 CIRCUIT DIAGRAM OF ON-LINE SURGE RECORDER.

unmark RST 6.5. So we have to load the accumulator with ODH

0	0	0	0	1	1	0	1

4.2 CALIBRATION OF ANALOG TO DIGITAL CONVERTER

Analog voltage is converted into digits by analog to digital converter. The recorded magnitude of voltage by surge recorder is in terms of hexadecimal numbers. To plot the wave or to know the actual magnitude of voltage it is necessary to calibrate the analog to digital converter(ADC).

Stabilized voltage supply is used to calibrate ADC. The software used for calibration is given below.

Lebel	Address	Contents	Mnemonic and Operand field	Comments
	2000	3E 98	MVI A,98H	To initialize
	2002	D3 03	OUT 03H	8255
LP3	2004	3E 00	MVI A,00	
	2006	D3 02	OUT 02H	Start of conversion
	2008	3C	IN RA	pulse at PC_0
	2009	D3 02	OUT 02 H	
	200B	3D	DCR A	
	200C	D3 02	OUT 02 H	
LP1	200E	DB 02	IN 02 H	End of conversion
	2010	EC 10	ANI 10	pulse at PC_4
	2012	C2 0E 20	JNZ LP1	
LP2	2015	DB 02	IN 02H	
	2017	E6 10	ANI 10	
	2019	CA 15 20	JZ LP2	
	201C	DB 00	IN 00H	For continuous
	201E	32 F6 27	STA 27F6	display of the
	2021	CD FA 06	CALL 06 FA	digital data
	2024	C3 04 20	JMP LP3	

OBSERVATIONS

Analog Voltage (voltage)	OUTPUT VOLTAGE OF ADC	
	In Hexadecimal	In equivalent decimal number
0.0	00	00
0.5	18	24
1.0	33	51
1.5	4E	78
2.0	65	101
2.5	82	130
3.0	9B	155
3.5	B4	180
4.0	CE	206
4.5	EA	234
5.0	FF	255

So it is clear that for each 1 volt increment, there is increment of 51 in decimal equivalent number approximately. So, by dividing equivalent decimal voltage by 51, we can achieve the analog voltage.

The next chapter deals with the results and discussion for different types of surge generation method and recording.

CHAPTER 5

RESULTS AND DISCUSSION

Voltage magnitude and time of switching surges have been recorded by microprocessor based surge recorder. Observations of voltage magnitude and time have been taken. From the observations obtained by microprocessor, equivalent decimal values have been calculated and then the equivalent decimal values are converted in to equivalent analog values.

Table 5.1 shows the surge recorded by microprocessor when the surge is generated by microprocessor itself. Fig 5.1 shows the plot of surge recorded.

TABLE 5.1

Initial timer count is 6978 H

Observations (in Hexa Decimal		Equivalent Decimal Values		Equivalent analog Values	
VOLTAGE	TIMER Count	VOLTAGE	TIMER Count	VOLTAGE (Volts)	TIME (m s)
1	2	3	4	5	6
23	692C	35	26924	0.686	.049
57	68E1	87	26849	1.70	.098
67	6895	103	26773	2.02	.147
87	684A	135	26698	2.64	.196
97	67FE	151	26622	2.96	.246
9F	6783	159	26547	3.11	.295
A1	6767	161	26471	3.15	.344
A7	671C	167	26396	3.27	.393
B4	66D0	180	26320	3.54	.443
BF	6685	191	26245	3.74	.491

1	2	3	4	5	6
A0	6639	160	26169	3.15	.541
70	65EE	112	26094	2.19	.590
50	65A2	80	26018	1.56	.639
30	6557	48	25943	0.94	.688
20	650B	32	25867	0.62	.738
20	64C0	32	25792	0.62	.786
16	6474	22	25716	0.43	.836
10	6429	16	25641	0.31	.885
09	63DD	09	25565	0.17	.934
08	6392	08	25490	0.15	.983
07	6346	07	25414	0.13	1.033
07	62FB	07	25339	0.13	1.082
06	62AF	06	25263	0.11	1.131
05	6264	05	25188	0.09	1.18
05	6218	05	25112	0.05	1.230
04	61CD	04	25037	0.07	1.278
04	6181	04	24961	0.07	1.328
04	6136	04	24886	0.07	1.377
04	60EA	04	24810	0.07	1.426
04	609F	04	24735	0.07	1.475
04	6053	04	24659	0.07	1.525
04	6008	04	24584	0.07	1.573
04	5FBC	04	24508	0.07	1.623
04	5F71	04	24433	0.07	1.672
04	5F25	04	24357	0.07	1.721
04	5EDA	04	24282	0.07	1.770
04	5E8E	04	24206	0.07	1.820
04	5E43	04	24131	0.07	1.869
04	5DF7	04	24055	0.07	1.918
04	5DAC	04	23980	0.07	1.967
04	5D60	04	23904	0.07	2.016
04	5D15	04	23829	0.07	2.065
04	5CC9	04	23753	0.07	2.115

1	2	3	4	5	6
04	5C7E	04	23678	0.07	2.164
04	5C32	04	23602	0.07	2.213
04	5BE7	04	23527	0.07	2.262
04	5B96	04	23451	0.07	2.312
04	5B50	04	23376	0.07	2.360
04	5B04	04	23300	0.07	2.450
04	5AB9	04	23225	0.07	2.459
03	5A6D	03	23149	0.05	2.508
03	225A	03	23074	0.05	2.557
03	59D6	03	22998	0.05	2.607
03	598B	03	22923	0.05	2.656
03	593F	03	22847	0.05	2.709
03	58F4	03	22772	0.05	2.754
03	58A8	03	22696	0.05	2.803
03	585D	03	22621	0.05	2.852
03	5811	03	22545	0.05	2.902
03	57C6	03	22470	0.05	2.951
03	577A	03	22394	0.05	3.000
03	572F	03	22319	0.05	3.049
03	56E3	03	22244	0.05	3.099
03	5698	03	22168	0.05	3.147
03	564C	03	22093	0.05	3.197
03	5601	03	22017	0.05	3.246
03	55B5	03	21942	0.05	3.295
03	556A	03	21866	0.05	3.344
03	551E	03	21791	0.05	3.394
03	54D3	03	21715	0.05	3.442
03	5487	03	21640	0.05	3.492
03	543C	03	21564	0.05	3.541
03	53F0	03	21489	0.05	3.590
03	53A5	03	21413	0.05	3.639
03	5359	03	21338	0.05	3.689
03	530E	03	21262	0.05	3.738
03	52C2	03	21187	0.05	3.787

1	2	3	4	5	6
03	5277	03	21111	0.05	3.836
03	522B	03	21036	0.05	3.885
03	51E0	03	20960	0.05	3.934
03	5194	03	20885	0.05	3.984
03	5149	03	20809	0.05	4.033
03	50FD	03	20734	0.05	4.082
03	50B2	03	20658	0.05	4.131
03	5066	03	20583	0.05	4.181
03	501B	03	20507	0.05	4.229
03	4FCF	03	20432	0.05	4.279
03	4F84	03	20356	0.05	4.328
03	4F38	03	20281	0.05	4.377
03	4EED	03	20205	0.05	4.426

In the next developmental stage the externally generated surge is recorded by microprocessor. The designed surge generator has the following values of parameters

$C_1 = .22\ \mu F$

$C_2 = .04\ \mu F$

$R_1 = 2.2\ K$

$R_2 = 4.7\ K$

From these parameters the calculated values of the rise time and the tail time are 0.223 ms and 1.255 ms respectively. Table 5.2 shows the observations taken for recording this surge. From the observations taken, the surge has been plotted which is shown in fig.5.2. The recorded surge has rise time and tail time of .2 ms and 1.0 ms respectively.

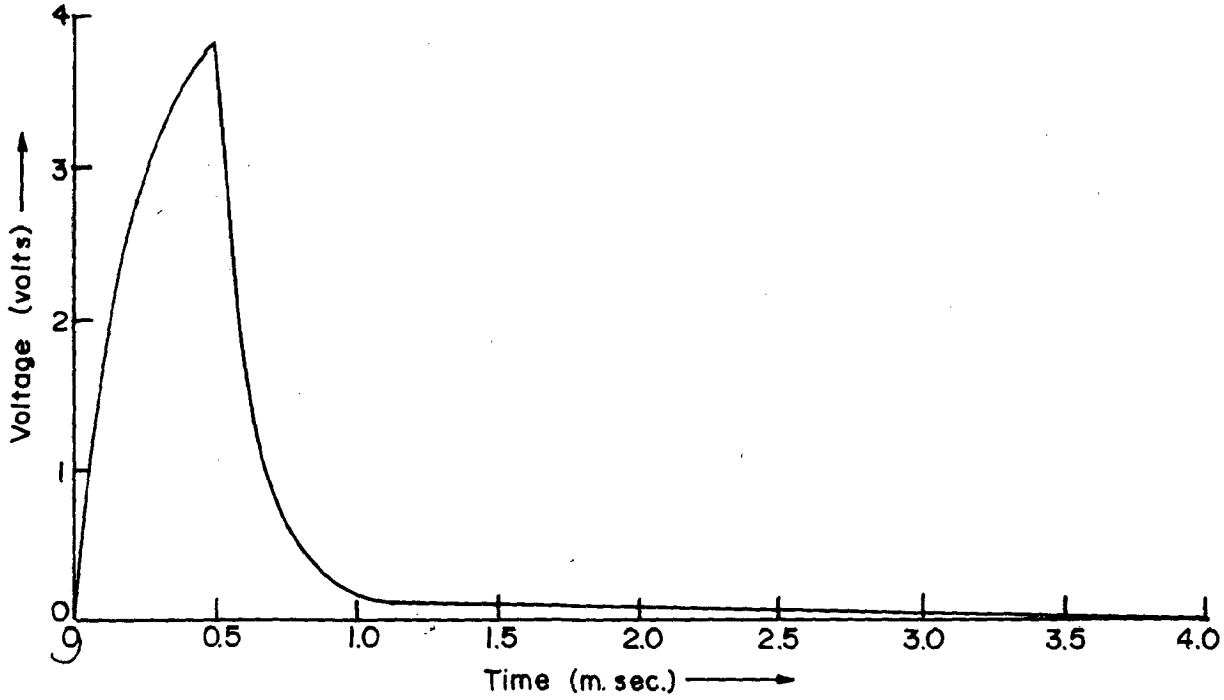


FIG.5.1 SURGE GENERATED FROM MICROPROCESSOR.

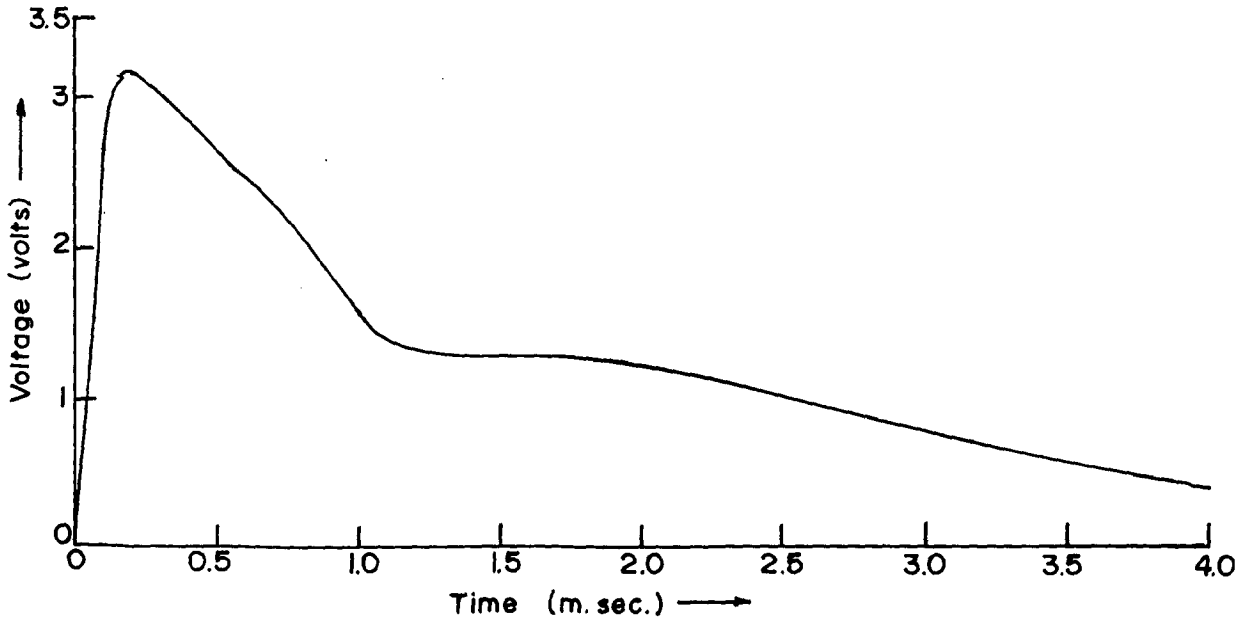


FIG.5.2 SURGE GENERATED BY SURGE GENERATOR ON RECEIVING SIGNAL FROM MICROPROCESSOR.

TABLE 5.2

Initial timer count is FFFFH

OBSERVATIONS(IN HEXA-DECIMAL)		EQUIVALENT DECIMAL VALUES		EQUIVALENT ANALOG VALUES	
VOLTAGE	TIMER COUNT	VOLTAGE	TIMER COUNT	VOLTAGE	TIME (m sec.)
1	2	3	4	5	6
3F	FF97	63	65431	1.23	.067
8F	FF4B	143	65355	2.80	.117
9F	FF00	159	65280	3.11	.166
A0	FEB4	160	65204	3.13	.215
9D	FE69	157	65129	3.07	.264
99	FE1D	153	65053	3.00	.314
94	FDD2	148	64978	2.90	.362
90	FD86	154	64902	2.82	.412
8B	FD3B	139	64827	2.72	.461
86	FCEF	134	64751	2.62	.510
82	FCA4	130	64676	3.55	.559
7D	FC58	125	64600	2.45	.609
78	FC0D	120	64525	2.35	.657
74	FBC1	116	64449	2.27	.707
70	FB76	112	64374	2.19	,756
69	FB2A	105	64298	2.05	.805
64	FADF	100	64223	1.96	.854
5C	FA93	92	64147	1.80	.904
54	FA48	84	64072	1.64	.953
4E	F9FC	78	63996	1.53	1.002
49	F9B1	73	63921	1.43	1.051
46	F965	70	63845	1.37	1.100
44	F91A	68	63770	1.33	1.149
43	F8CE	67	63694	1.31	1.199
42	F883	66	63619	1.29	1.248
41	F837	65	63543	1.27	1.297
40	F7EC	64	63468	1.25	1.346

1	2	3	4	5	6
40	F7A0	64	63392	1.25	1.390
40	F755	64	63317	1.25	1.444
40	F709	64	63241	1.25	1.495
40	F6BE	64	63166	1.25	1.543
40	F672	64	63090	1.25	1.592
40	F627	64	63015	1.25	1.641
40	F5DB	64	62939	1.25	1.691
3F	F590	63	62864	1.23	1.740
3F	F544	63	62788	1.23	1.789
3F	F4F9	63	62713	1.23	1.838
3F	F4AD	63	62637	1.23	1.888
3F	F462	63	62562	1.23	1.936
3F	F416	62	62486	1.21	1.986
3E	F3CB	62	62411	1.21	2.035
3D	F37F	61	62335	1.19	2.084
3C	F334	60	62260	1.17	2.133
3B	F2E8	59	62184	1.15	2.183
3A	F29D	58	62109	1.13	2.231
39	F251	57	62033	1.11	2.281
38	F206	56	61958	1.09	2.330
37	F1BA	55	61882	1.07	2.379
36	F16F	54	61807	1.05	2.428
35	F123	53	61731	1.03	2.478
33	F0D8	51	61656	1.00	2.527
32	F08C	50	61580	0.98	2.576
31	F041	49	61505	0.96	2.625
30	EFF5	48	61429	0.94	2.675
¢E	EFAA	46	61354	0.90	2.723
2D	EF5E	45	61278	0.88	2.773
2C	EF13	44	61203	0.86	2.822
2B	EEC7	43	61127	0.84	2.871
2A	EE7C	42	61052	0.82	2.920
29	EE30	41	60976	0.80	2.970

1	2	3	4	5	6
28	EDE5	40	60901	0.78	3.018
26	ED99	38	60825	0.74	3.068
25	ED4E	37	60750	0.72	3.117
24	ED02	36	60674	0.70	3.166
23	ECB7	35	60599	0.68	3.215
22	EC6B	34	60523	0.66	3.265
21	EC20	33	60448	0.64	3.314
20	EBD4	32	60372	0.62	3.363
20	EB89	32	60297	0.62	3.412
1F	EB3D	31	60221	0.60	3.461
1E	EAF2	30	60146	0.58	3.510
1D	EAA6	29	60070	0.56	3.560
1C	EA5B	28	59995	0.54	3.609
1B	EA0F	27	59919	0.52	3.658
1B	E9C4	27	59844	0.52	3.707
1A	E978	26	59768	0.50	3.757
19	E92D	25	59693	0.49	3.805
18	E8E1	24	59617	0.47	3.855
18	E896	24	59542	0.47	3.904
17	E84A	23	59466	0.45	3.953
16	E7FF	22	59391	0.43	4.002
16	E7B3	22	59315	0.43	4.052
15	E768	21	59240	0.41	4.100

On line surge recording has been done for three surges having different rise and tail times. Table 5.3 shows the parameter values of surge generator, rise and tail times of surge for three different sets of observations.

TABLE 5.3

Set number	C_1 μF	C_2 μF	R_1 (K Ohm)	R_2 (K.Ohm)	Rise time t_1(msec.)	Tail time t_2(ms)
Set 1	0.22	0.04	10	22	1.015	5.824
Set 2	0.22	0.04	4.7	10	0.477	2.675
Set 3	0.22	0.04	1	4.7	0.101	1.037

The observations for set 1, 2 and 3 are given in tables 5.3.1, 5.3.2 and 5.3.3 respectively.

TABLE 5.3.1

Initial timer count FFFFH

OBSERVATIONS (IN HEXA DECIMAL)		EQUIVALENT DECIMAL VALUES		EQUIVALENT ANALOG VALUES	
VOLTAGE	TIME	VOLTAGE	TIMER COUNT	VOLTAGE (IN VOLTS)	TIME (in ms)
37	FF87	55	65415	1.07	.078
5B	FED1	91	65233	1.78	.196
6F	FE1B	111	65051	2.17	.314
7F	FD65	127	64869	2.49	.433
87	FCAF	135	64687	2.64	.551
8B	FBF9	139	64505	2.72	.670
8D	FB43	141	64323	2.76	.788
8E	FA8D	142	64141	2.78	.907
8D	F9D7	141	63959	2.76	1.025
8C	F921	140	63777	2.74	1.144
8B	F86B	139	63595	2.72	1.263
8A	F7B5	138	63413	2.70	1.382
88	F6FF	136	63231	2.66	1.500
86	F649	134	63049	2.62	1.619

1	2	3	4	5	6
84	F593	132	62867	2.58	1.738
83	F4DD	131	62685	2.56	1.856
81	F427	129	62503	2.52	1.975
80	F371	128	62321	2.50	2.093
7D	F2BB	125	62139	2.45	2.212
7C	F205	124	61957	2.43	2.330
7A	F14F	122	61775	2.39	2.449
78	F099	120	61593	2.35	2.568
76	EFE3	118	61411	2.31	2.686
74	EF2D	116	61229	2.27	2.805
72	EE77	114	61047	2.23	2.923
71	EDC1	113	60865	2.21	3.042
6F	ED0B	111	60683	2.17	3.160
6D	EC55	109	60501	2.13	3.279
6C	EB9F	108	60319	2.11	3.398
6A	EAE9	106	60137	2.07	3.516
68	EA33	104	59955	2.03	3.635
66	E97D	102	59773	2.00	3.753
65	E8C7	101	59591	1.98	3.872
63	E811	99	59409	1.94	3.990
61	E75B	97	59227	1.90	4.109
60	E6A5	96	59045	1.88	4.228
5D	E5EF	93	58863	1.82	4.346
5B	E539	91	58681	1.78	4.465
59	E483	89	58499	1.74	4.583
56	E3CD	86	58317	1.68	4.702
53	E317	83	58135	1.62	4.820
4F	E261	79	57953	1.54	4.939
4B	E1AB	75	57771	1.47	5.057
48	E0F5	72	57589	1.41	5.176
45	E03F	69	57407	1.35	5.295
42	DF89	66	57225	1.29	5.413
41	DED3	65	57043	1.27	5.532
40	DE1D	64	56861	1.25	5.650

1	2	3	4	5	6
3E	DD67	62	56679	1.21	5.769
3D	DCB1	61	56497	1.19	5.887
3D	DBFB	61	56315	1.19	6.006
3C	DB45	60	56133	1.17	6.125
3C	DA8F	60	55951	1.17	6.243
3B	D9D9	59	55769	1.15	6.362
3B	D923	59	55587	1.15	6.480
3B	D86D	59	55405	1.15	6.599
3B	D7B7	59	55223	1.15	6.717
3B	D701	59	55041	1.15	6.836
3B	D64B	59	54859	1.15	6.955
3B	D595	59	54677	1.15	7.073
3B	D4DF	59	54495	1.15	7.192
3B	D429	59	54313	1.15	7.310
3B	D373	59	54131	1.15	7.429
3B	D2BD	59	53949	1.15	7.547
3B	D207	59	53767	1.15	7.666
3B	D151	59	53585	1.15	7.785
3B	D09B	59	53403	1.15	7.903
3B	CFE5	59	53221	1.15	8.022
3B	CF2F	59	53039	1.15	8.140
3B	CE79	59	52857	1.15	8.259
3B	CDC3	59	52675	1.15	8.377
3A	CD0D	58	52493	1.13	8.469
3A	CC57	58	52311	1.13	8.614
3A	CBA1	58	52129	1.13	8.733
3A	CAEB	58	51947	1.13	8.852
3A	CA35	58	51765	1.13	8.907
3A	C97F	58	51583	1.13	9.089
39	C8C9	57	51401	1.11	9.207
39	C813	57	51219	1.11	9.326
39	C75D	57	51037	1.11	9.444

1	2	3	4	5	6
38	C6A7	56	50855	1.09	9.563
38	C5F1	56	50673	1.09	9.682
38	C53B	56	50491	1.09	9.800
37	C485	55	50309	1.07	9.919
36	C3CF	54	50127	1.05	10.037
36	C319	54	49945	1.05	10.156
35	C263	53	49763	1.03	10.274
35	C1AD	53	49581	1.03	10.393
34	C0F7	52	49399	1.01	10.512
34	C041	52	49217	1.01	10.630
33	BF8B	51	49035	1.00	10.749
32	BED5	50	48853	0.98	10.867
32	BE1F	50	48671	0.98	10.986
31	BD69	49	48489	0.96	11.104
31	BCB3	49	48307	0.96	11.223
30	BBFD	48	48125	0.94	11.342
2F	BB47	47	47943	0.92	11.460
2F	BA91	47	47761	0.92	11.579
2E	B9DB	46	47579	0.90	11.697
2E	B925	46	47397	0.90	11.816
2D	B86F	45	47215	0.88	11.934
2C	B7B9	44	47033	0.86	12.053
2C	B703	44	46851	0.84	12.171
2B	B64D	43	46669	0.82	12.290
2B	B597	43	46487	0.82	12.409
2A	B4E1	42	46305	0.80	12.527
29	B42B	41	46123	0.78	12.646
29	B375	41	45941	0.78	12.764
28	B2BF	40	45759	0.76	12.883
28	B209	40	45577	0.76	13.001
27	B153	39	45395	0.74	13.120
27	B09D	39	45213	0.74	13.239

1	2	3	4	5	6
26	AFE7	38	45031	0.72	13.357
26	AF31	38	44849	0.72	13.476
25	AE7B	37	44667	0.70	13.594
25	ADC5	37	44485	0.70	13.713
24	AD0F	36	44303	0.68	13.831
24	AC59	36	44121	0.68	13.950
23	ABA3	35	43939	0.66	14.069
23	AAED	35	43757	0.66	14.187
22	AA37	34	43575	0.64	14.306
22	AA37	34	43393	0.64	14.424
21	A8CB	33	43211	0.62	14.543
21	A815	33	43029	0.62	14.661
20	A75F	32	42847	0.60	14.780
20	A6A9	32	42665	0.60	14.899
20	A5F3	32	42483	0.60	15.017
1F	A53D	31	42301	0.58	15.136
1F	A487	31	42119	0.58	15.254
1E	A3D1	30	41937	0.56	15.373
1E	A31B	30	41755	0.56	15.491
1D	A265	29	41573	0.54	15.610

TABLE 5.3.2

Initial timer Count FFFFH

OBSERVATIONS (IN HEXADECIMAL)		EQUIVALENT DECIMAL VALUES		EQUIVALENT ANALOG VALUES	
VOLTAGE	TIME	VOLTAGE	TIMER COUNT	VOLTAGE (Volts)	TIME (m.sec.)
1	2	3	4	5	6
4F	FF87	79	65415	1.54	.078
77	FED1	119	65233	2.33	.196
85	FE1B	133	65051	2.60	.314

1	2	3	4	5	6
87	FD65	135	64869	2.64	.433
86	FCAF	134	64687	2.62	.551
82	FBF9	130	64505	2.55	.670
80	FB43	128	64323	2.50	.7880
7B	FA8D	123	64141	2.41	.907
77	F9D7	119	63959	2.33	1.025
73	F921	115	63777	2.25	1.144
6F	F86B	111	63595	2.17	1.263
6B	F7B5	107	63413	2.09	1.382
67	F6FF	103	63231	2.01	1.500
63	F649	99	63049	1.94	1.619
5E	F593	94	62867	1.84	1.738
5A	F4DD	90	62685	1.76	1.856
54	F427	84	62503	1.64	1.975
4E	F371	78	62321	1.52	2.093
47	F2BB	71	62139	1.39	2.212
41	F205	65	61957	1.27	2.330
3D	F14F	61	61775	1.19	2.449
3B	F099	59	61593	1.15	2.568
39	EFE3	57	61411	1.11	2.686
38	EF2D	56	61229	1.09	2.805
37	EE77	55	61047	1.07	2.923
37	EDC1	55	60865	1.07	3.042
36	EDOB	54	60683	1.05	3.160
36	EC55	54	60501	1.05	3.279
36	EB9F	54	60319	1.05	3.398
36	EAE9	54	60137	1.05	3.516
36	EA33	54	59955	1.05	3.635
36	E97D	54	59773	1.05	3.753
36	E8C7	54	59591	1.05	3.872
36	E811	54	59409	1.05	3.990
36	E75B	54	59227	1.05	4.109
36	E6A5	54	59045	1.05	4.228

1	2	3	4	5	6
35	E5EF	53	58863	1.03	4.346
35	E539	53	58681	1.03	4.465
34	E483	52	58499	1.01	4.583
34	E3CD	52	58317	1.01	4.702
33	E317	51	58135	1.01	4.820
32	E261	50	57953	0.98	4.939
31	E1AB	49	57771	0.96	5.057
30	E0F5	48	57589	0.94	5.176
30	E03F	48	57407	0.94	5.295
2E	DF89	46	57225	0.90	5.413
2D	DED3	45	57043	0.88	5.532
2C	DE1D	44	56861	0.86	5.650
2B	DD67	43	56679	0.84	5.769
2A	DCB1	42	56497	0.82	5.887
29	DBFB	41	56315	0.80	6.006
28	DB45	40	56133	0.78	6.125
26	DA8F	38	55951	0.74	6.243
25	D9D9	37	55769	0.72	6.362
24	D923	36	55587	0.70	6.480
23	D86D	35	55405	0.68	6.599
22	D7B7	34	55223	0.66	6.717
21	D701	33	55041	0.64	6.836
20	D64B	32	54859	0.62	6.955
20	D595	32	54677	0.62	7.073
1E	D4DF	30	54495	0.58	7.192
1E	D429	30	54313	0.58	7.310
1D	D373	29	54131	0.56	7.429
1C	D2BD	28	53949	0.54	7.547
1B	D207	27	53767	0.53	7.666
1A	D151	26	53585	0.50	7.785
1A	D09B	26	53403	0.50	7.903
19	CFE5	25	53221	0.49	8.022
18	CF2F	24	53039	0.47	8.140

1	2	3	4	5	6
17	CE79	23	52857	0.45	8.259
17	CDC3	23	52675	0.45	8.377
16	CDOD	22	52493	0.43	8.496
15	CC57	21	52311	0.41	8.614
15	CBA1	21	52129	0.41	8.733
14	CAEB	20	51947	0.39	8.852
13	CA35	19	51765	0.37	8.970
13	C97F	19	51583	0.37	9.089
12	C8C9	18	51401	0.35	9.207
12	C813	18	51219	0.35	9.326
11	C75D	17	51037	0.33	9.444
11	C6A7	17	50855	0.33	9.563
10	C5F1	16	50673	0.31	9.682
10	C53B	16	50491	0.31	9.800
0F	C485	15	50309	0.29	9.919
0F	C3CF	15	50127	0.29	10.037
0E	C319	14	49945	0.27	10.156
0E	C263	14	49763	0.27	10.274
0E	C1AD	14	49581	0.27	10.393
0D	C0F7	13	49399	0.25	10.512
0D	C041	13	49217	0.25	10.630
0C	BF8B	12	49035	0.23	10.749
0C	BED5	12	48853	0.23	10.867
0C	BE1F	12	48671	0.23	10.986
0B	BD69	11	48489	0.21	11.104
0B	BCB3	11	48307	0.21	11.223
0B	BBFD	11	48125	0.21	11.342
0A	BB47	10	47943	0.19	11.460
0A	BA91	10	47761	0.19	11.579
0A	B9DB	10	47579	0.19	11.697
09	B925	9	47397	0.17	11.816
09	B86F	9	47215	0.17	11.934
09	B7B9	9	47033	0.17	12.053

1	2	3	4	5	6
09	B703	9	46851	0.17	12.171
08	B64D	8	46669	0.15	12.290
08	B597	8	46487	0.15	12.409
08	B4E1	8	46305	0.15	12.527
08	B42B	8	46123	0.15	12.646
07	B375	7	45941	0.13	12.764
07	B2BF	7	45759	0.13	12.883
07	B209	7	45577	0.13	13.001
07	B153	7	45395	0.13	13.120
07	B09D	7	45213	0.13	13.239
06	AFE7	6	45031	0.11	13.357
06	AF31	6	44849	0.11	13.476
06	AE7B	6	44667	0.11	13.594
06	ADC5	6	44485	0.11	13.713
06	AD0F	6	44303	0.11	13.831
05	AC59	5	44121	0.09	13.950
05	ABA3	5	43939	0.09	14.069
05	AAED	5	43757	0.09	14.187
05	AA37	5	43575	0.09	14.306
05	A981	5	43393	0.09	14.424
05	A8CB	5	43211	0.09	14.543
05	A815	5	43029	0.09	14.661
04	A75F	4	42847	0.07	14.780
04	A6A9	4	42665	0.07	14.899
04	A5F3	4	42483	0.07	15.017
04	A53D	4	42301	0.07	15.136
04	A487	4	42119	0.07	15.254
04	A3D1	4	41937	0.07	15.373
04	A31B	4	41755	0.07	15.491
04	A265	4	41573	0.07	15.610
03	A1AF	3	41391	0.05	15.728

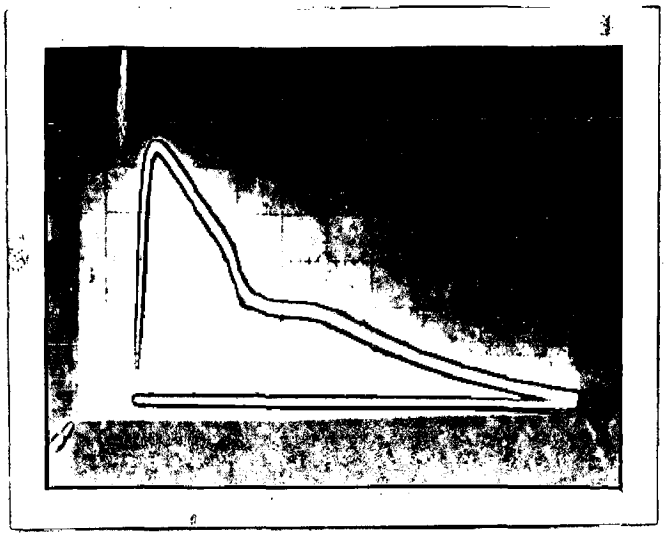
TABLE 5.3.3

Initial timer count FFFFH

OBSERVATIONS(IN HEXADECIMAL)		EQUIVALENT DECIMAL VALUES		EQUIVALENT ANALOG VALUES	
VOLTAGE	TIME	VOLTAGE	TIMER COUNT	VOLTAGE (Volts)	TIME (m Sec.)
1	2	3	4	5	6
7F	FF87	127	65415	2.49	.078
94	FED1	148	65233	2.90	.196
8A	FE1B	138	65051	2.70	.314
80	FD65	128	64869	2.509	.433
70	FCAF	112	64687	2.19	.551
61	FBF9	97	64505	1.90	.670
50	FB43	80	64323	1.56	.788
46	FA8D	70	64141	1.37	.907
40	F9D7	64	63959	1.25	1.025
3E	F921	62	63777	1.21	1.144
3C	F86B	60	63595	1.17	1.263
3B	F7B5	59	63413	1.15	1.382
3A	F6FF	58	63231	1.13	1.500
3A	F649	58	63049	1.13	1.619
3A	F593	58	62867	1.13	1.738
3A	F4DD	58	62685	1.13	1.856
39	F427	57	62503	1.11	1.975
38	F371	56	62321	1.09	2.093
37	F2BB	55	62139	1.07	2.212
35	F205	53	61957	1.03	2.330
33	F14F	51	61775	1.00	2.449
30	F099	48	61593	0.94	2.568
2E	EFE3	46	61411	0.90	2.686
2B	EF2D	43	61229	0.84	2.805
28	EE77	40	61047	0.78	2.923
26	EDC1	38	60865	0.74	3.042
24	ED0B	36	60683	0.70	3.160

1	2	3	4	5	6
21	EC55	33	60501	0.64	3.279
1F	EB9F	31	60319	0.60	3.398
1D	EAE9	29	60137	0.56	3.516
1B	EA33	27	59955	0.52	3.635
19	E97D	25	59773	0.49	3.753
18	E8C7	24	59591	0.47	3.872
16	E811	22	59409	0.43	3.990
14	E75B	20	59227	0.39	4.109
13	E6A5	19	59045	0.37	4.228
12	E5EF	18	58863	0.35	4.346
10	E539	16	58681	0.31	4.465
0F	E483	15	58499	0.29	4.583
0E	E3CD	14	58317	0.27	4.702
0D	E317	13	58135	0.25	4.820
0C	E261	12	57953	0.23	4.939
0B	E1AB	11	57771	0.21	5.057
0B	E0F5	11	57589	0.21	5.176
0A	E03F	10	57407	0.19	5.295
09	DF89	9	57225	0.17	5.413
08	DED3	8	57043	0.15	5.532
08	DE1D	8	56861	0.15	5.650
07	DD67	7	56679	0113	5.769
07	DCB1	7	56497	0.13	5.887
06	DBFB	6	56315	0.11	6.006
06	DB45	6	56133	0.11	6.125
05	DA8F	5	55951	0.09	6.243
05	D9D9	5	55769	0.09	6.362
05	D923	5	55587	0.09	6.480
04	D86D	4	55405	0.07	6.599
04	D7B7	4	55223	0.07	6.717
04	D701	4	55041	0.07	6.836
03	D64D	3	54859	0.05	6.955
03	D595	3	54677	0.05	7.073
03	D4DF	3	54495	0.05	7.192

2	3	4	5	6
D429	3	54313	0.05	7.310
D373	3	54131	0.05	7.429
D2BD	2	53949	0.03	7.547
D207	2	53767	0.03	7.666
D151	2	53585	0.03	7.785
D09B	2	53403	0.03	7.903
CFE5	2	53221	0.03	8.022
CF2F	2	53039	0.03	8.140
CE79	2	52857	0.03	8.259
CDC3	1	52675	0.01	8.377
CD0D	1	52493	0.01	8.496
CC57	1	52311	0.01	8.614
CBA1	1	[illegible]	0.01	[illegible]



VOLTAGE SCALE - 0·5 V/cm

TIME SCALE - 2 ms/cm

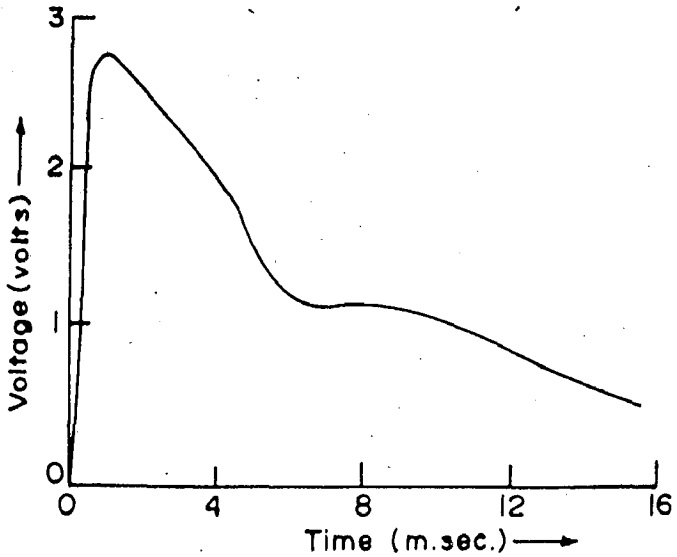
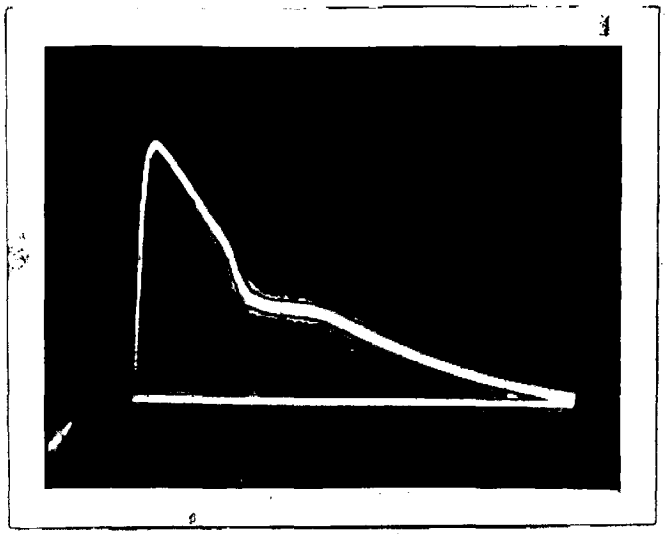


FIG.5.3.1 ON-LINE SURGE RECORDED BY MICROPROCESSOR WITH R_1=10KΩ AND R_2=22KΩ

1	2	3	4	5	6
03	D429	3	54313	0.05	7.310
03	D373	3	54131	0.05	7.429
02	D2BD	2	53949	0.03	7.547
02	D207	2	53767	0.03	7.666
02	D151	2	53585	0.03	7.785
02	D09B	2	53403	0.03	7.903
02	CFE5	2	53221	0.03	8.022
02	CF2F	2	53039	0.03	8.140
02	CE79	2	52857	0.03	8.259
01	CDC3	1	52675	0.01	8.377
01	CD0D	1	52493	0.01	8.496
01	CC57	1	52311	0.01	8.614
01	CBA1	1	52129	0.01	8.733
01	CAEB	1	51947	0.01	8.852
01	CA35	1	51765	0.01	8.970
01	C97F	1	51583	0.01	9.089
01	C8C9	1	51401	0.01	9.207
01	C813	1	51219	0.01	9.326
01	C75D	1	51037	0.01	9.444
01	C6A7	1	50855	0.01	9.563
01	C5F1	1	50673	0.01	9.682
01	C53B	1	50491	0.01	9.800
01	C485	1	50309	0.01	9.919
00	C3CF	0	50127	0.00	10.037

For on-line surge recording, the recorded surges are plotted in fig.5.3.1, 5.3.2 and 5.3.3. The corresponding photographs have been also taken on storage cathode ray oscilloscope and are given along with the recorded surges for comparision.



VOLTAGE SCALE - 0·5 V/cm

TIME SCALE - 2 ms/cm

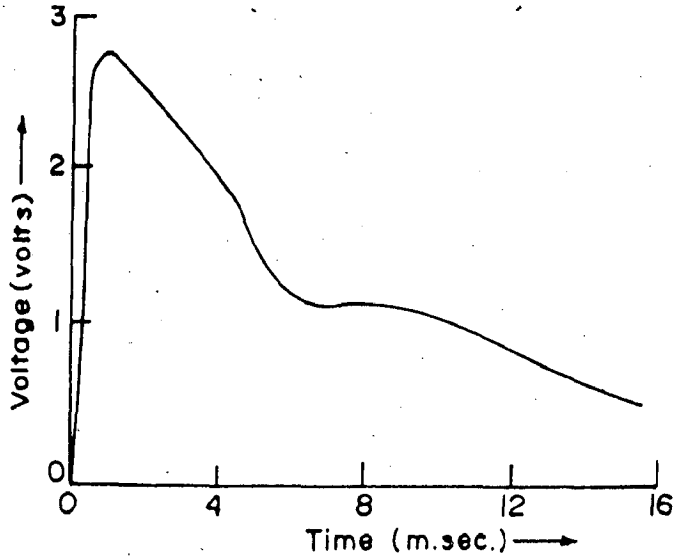
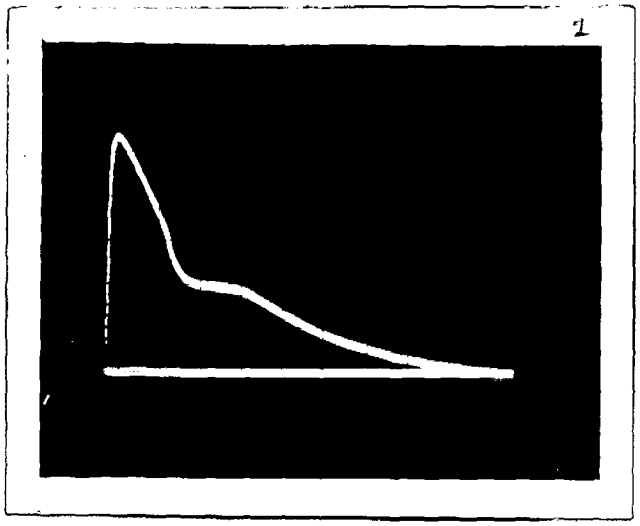


FIG.5.3.1 ON-LINE SURGE RECORDED BY MICROPROCESSOR WITH R_1=10KΩ AND R_2=22KΩ



VOLTAGE SCALE. 0·5 V/cm

TIME SCALE. 1 ms/cm

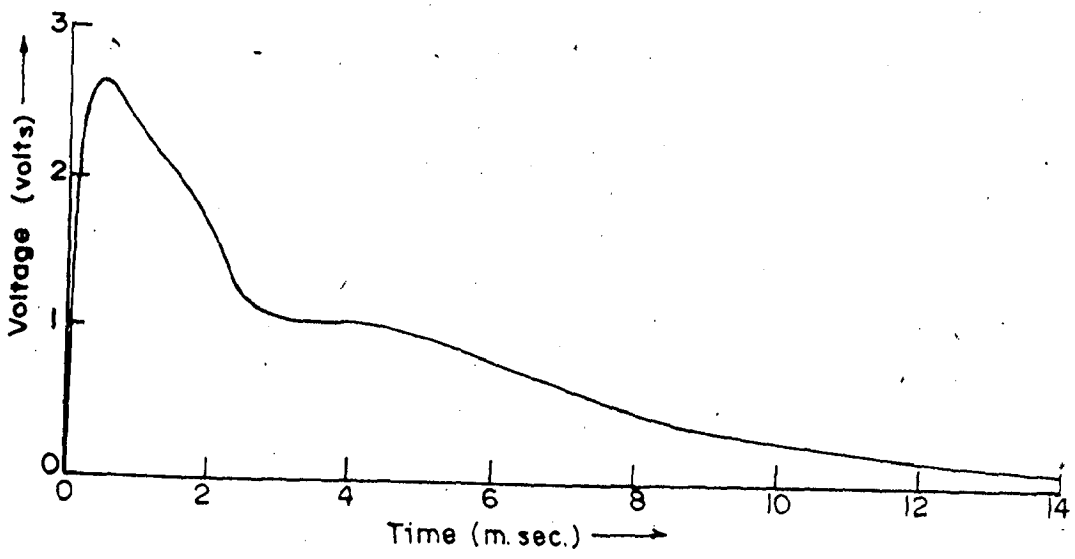
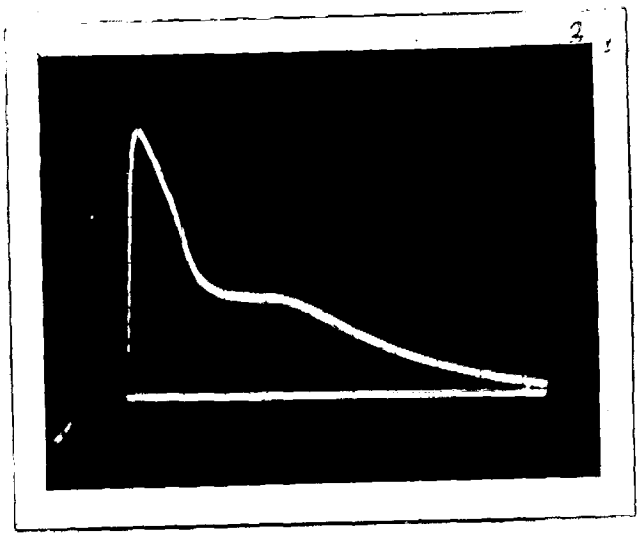


FIG. 5.3.2 ON-LINE SURGE RECORDED BY MICROPROCESSOR WITH $R_1 = 4.7K\Omega$ AND $R_2 = 10K\Omega$



VOLTAGE SCALE - 0·5 v/cm

TIME SCALE - 0·5 ms/cm

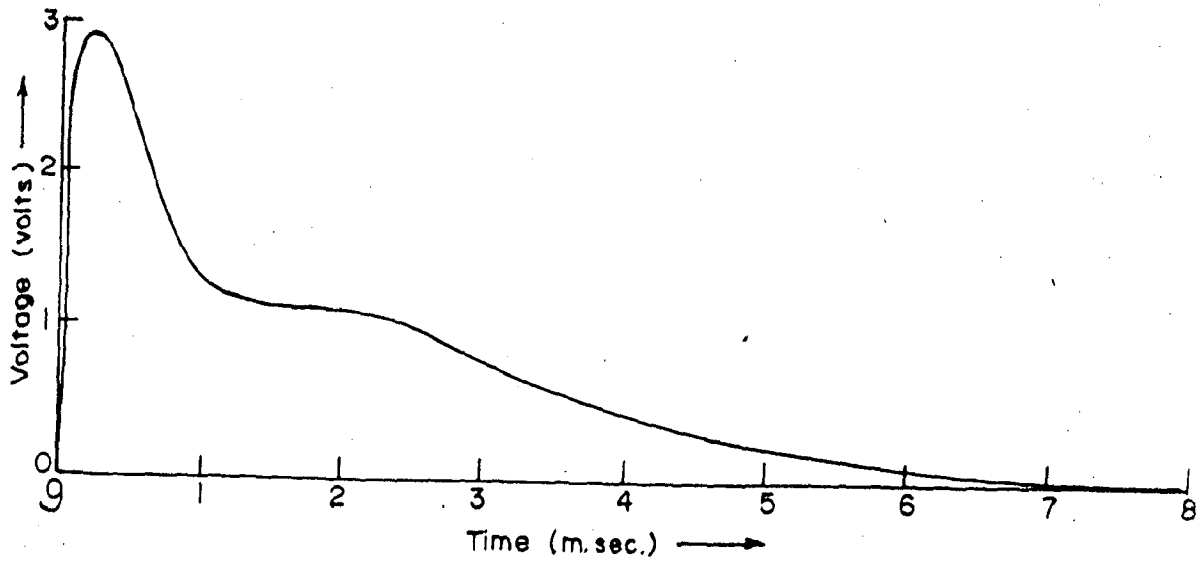


FIG.5.3.3 ON-LINE SURGE RECORDED BY MICROPROCESSOR WITH R_1=1KΩ AND R_2=4.7KΩ

The peak voltage magnitude, rise time and tail time for the different surges are given in table 5.4 from the point of view of comparative study.

TABLE 5.4

Sl. No.	Values from Photographs			Values from the plot of Surge		
	Peak Voltage (Volts)	Rise time (ms)	Tail time (ms)	Peak Voltage (Volts)	Rise time (m/s)	Tail time (m/s)
Set 1	2.75	1.0	4.85	2.78	1.0	5.2
Set 2	2.65	0.5	2.00	2.64	0.5	2.2
Set 3	2.90	0.2	0.80	2.90	0.2	0.85

From the table 5.4 it can be concluded that the surges recorded by microprocessor based surge recorder are almost identical to the surge recorded on storage oscilloscope. Slight difference in magnitudes and tail times may be due to inaccuracy of C.R.O. Chances of this difference are also caused by the estimation of surge magnitude, rise time and tail time from the photographs taken on C.R.O.

Microprocessor based surge recorder has very high accuracy of recording. But it can only record the surges of mili-second duration. Lighning surge can not be recorded by microprocessor based recorder due to time lost in -

(i) Conversion of analog signal to digital signal by ADC.

(ii) execution of the statements of the programme.

Lightning surge is a very short duration surge having rise time of the order of 1.2 μs and tail time of 50 μs. The conversion period of ADC is about 50 μs using clock of 1.535 MHz. Hence such fast surges can not be properly recorded.

In the present work on-line recording of surges was envisaged, and for this purpose the surge recorder was to be interfaced with 150 KV high voltage impulse generator of H.V. lab. via the capacitive voltage divider. But since the impulse generator was not in the working condition, this work was not carried out. Hence this work was carried out on a low voltage surge generator designed for this purpose to verify the correctness of the developed surge recorder. In the surge generator debounced switch has been used to avoid the distortions in the surge due to bouncing of simple switch. The results obtained reflect the correctness of the surge recorder.

For recording high voltage surges damped capacitive divider is used because of its good response on fast and slow transients. This divider will give some output voltage at normal power frequency voltage. In order to record the surges superimposed with normal power frequency voltage, the reference voltage to the comparator will have to be chosen accordingly. The low and voltage surge obtained from the capacitive divider is to be transmitted to the surge recorder through a shilded coaxial cable to avoid the distortions of the surge due to ordinary cable.

CHAPTER 6

CONCLUSIONS

In the present work, a microprocessor based on-line surge recorder has been developed. It has three developmental stages. The first stage has been developed to see whether the magnitude and time will be recorded simultaneously or not. The second stage of surge recorder was developed to check the ability of microprocessor to record the externally generated surge. The third stage of recorder (on-line) is the final stage by which the surges generated by surge generator have been recorded successfully.

It is not possible to record very fast surges like lightning surges by the developed surge recorder due to time resolution of the recorder.

Switching surges have been simulated by surge generator using debounced switch. Microprocessor based surge recorder has successfully recorded these surges.

Comparision has been made between the surges recorded by the developed microprocessor based recorder and the surges recorded on C.R.O. The comparative study shows that the microprocessor based surge recorder has a high accuracy of recording.

FUTURE SCOPE OF THE WORK

To obtain the print out of the datas stored in the memory of microprocessor, a transient printer can be interfaced.

The possibility of storing the recorded surge on magnetic tapes, discs may be explored. This will help the design engineers in detailed analysis of the system conditions leading to overvoltage generation and proper insulation co-ordination. It is possible to interface the surge recorder to the system via fibre optics transducer.

- o -

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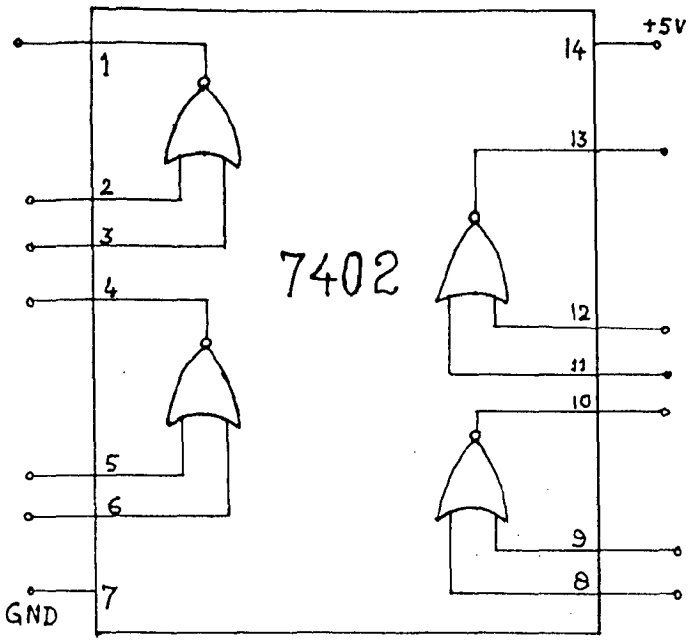
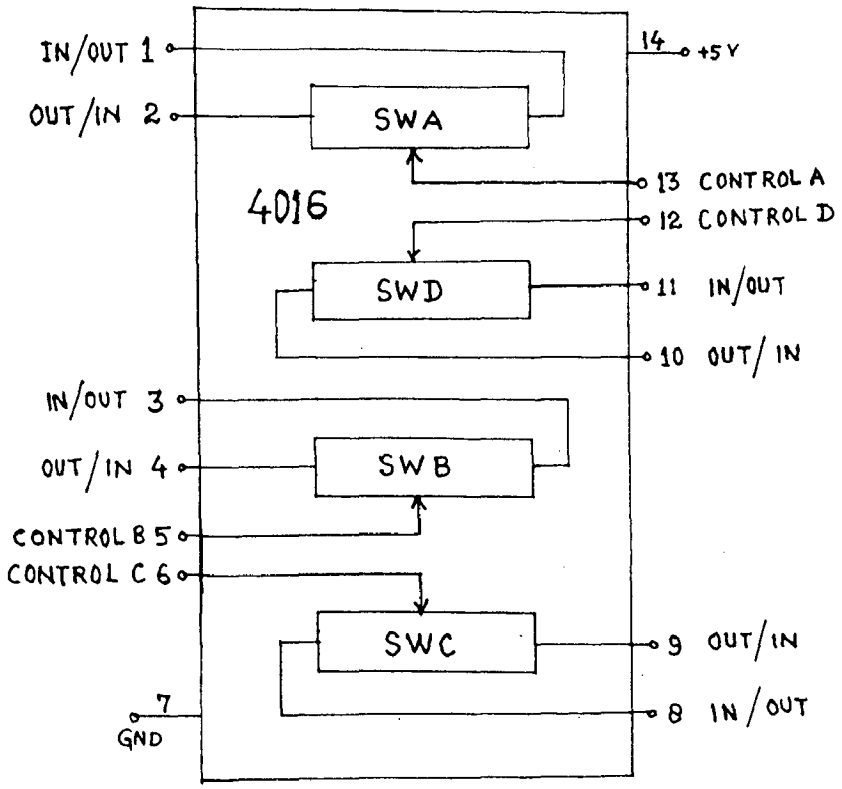
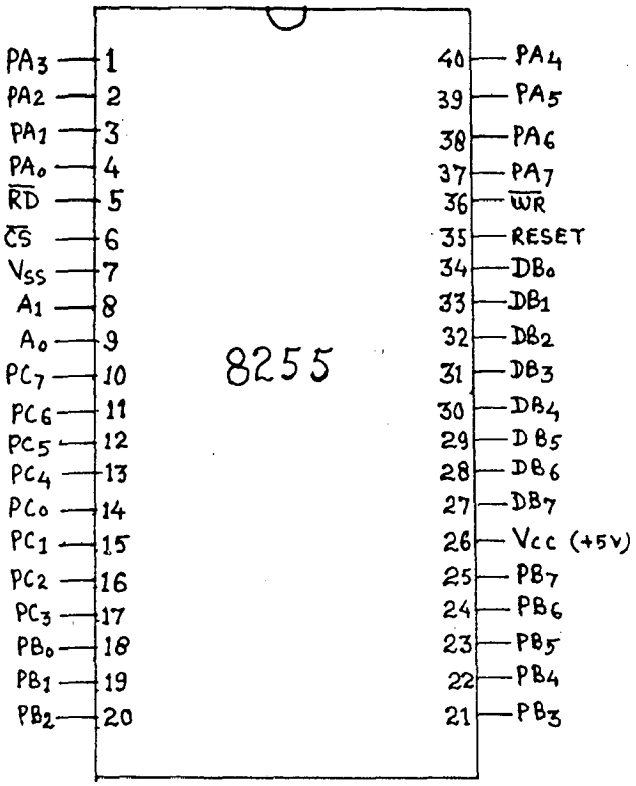
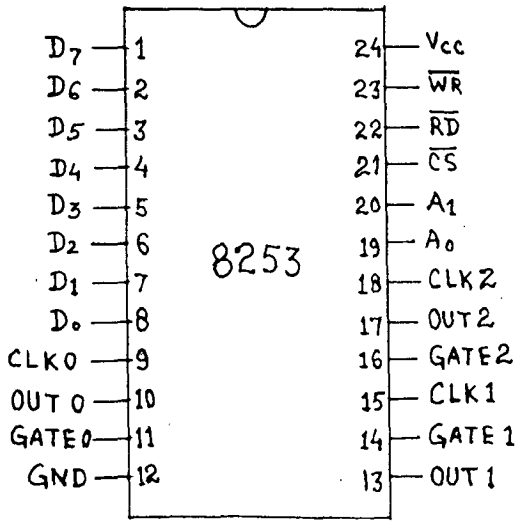
APPENDIX 1


7402
+5V
14
1
2
3
4
5
6
7
GND
13
12
11
10
9
8


4016
IN/OUT 1
OUT/IN 2
IN/OUT 3
OUT/IN 4
CONTROL B 5
CONTROL C 6
7
GND
14 +5V
13 CONTROL A
12 CONTROL D
11 IN/OUT
10 OUT/IN
9 OUT/IN
8 IN/OUT
SWA
SWB
SWC
SWD

APPENDIX 2


8255
PA3 1
PA2 2
PA1 3
PA0 4
RD 5
CS 6
VSS 7
A1 8
A0 9
PC7 10
PC6 11
PC5 12
PC4 13
PC0 14
PC1 15
PC2 16
PC3 17
PB0 18
PB1 19
PB2 20
40 PA4
39 PA5
38 PA6
37 PA7
36 WR
35 RESET
34 DB0
33 DB1
32 DB2
31 DB3
30 DB4
29 DB5
28 DB6
27 DB7
26 Vcc (+5V)
25 PB7
24 PB6
23 PB5
22 PB4
21 PB3


8253
D7 1
D6 2
D5 3
D4 4
D3 5
D2 6
D1 7
D0 8
CLK 0 9
OUT 0 10
GATE 0 11
GND 12
24 Vcc
23 WR
22 RD
21 CS
20 A1
19 A0
18 CLK 2
17 OUT 2
16 GATE 2
15 CLK 1
14 GATE 1
13 OUT 1

Signals at Connector J_2:

24 I/O lines of 8255-1 are brought out at this connector.

Connector pin number	I.C. pin number	Connector pin number	I.C. pin number
1	PC_4	14	PB_1
2	PC_5	15	PA_6
3	PC_2	16	PA_7
4	PC_3	17	PA_4
5	PC_0	18	PA_5
6	PC_1	19	PA_2
7	PB_6	20	PA_3
8	PB_7	21	PA_0
9	PB_4	22	PA_1
10	PB_5	23	PC_6
11	PB_2	24	PC_7
12	PB_3	25	GND
13	PB_0	26	GND

Signals at Connector J_1:

Connector pin number	Signal	Connector pin number	Signal
1	CAS 0	14	GATE 0
2	CAS 1	15	OUT 0
3	CAS 2	16	CLK 1
4	$\overline{SP}/\overline{EN}$	17	GATE 1
5	IR_0	18	OUT 1
6	IR_1	19	CLK 2
7	IR_2	20	GATE 2
8	IR_3	21	OUT 2
9	IR_4	22	RST 7.5
10	IR_5	23	RST 6.5
11	IR_6	24	MP
12	IR_7	25	GND
13	CLK 0	26	GND