FABRICATION AND EXPERIMENTAL INVESTIGATIONS ON MICROPROCESSOR BASED SELF CONTROLLED SYNCHRONOUS MOTOR DRIVE

A DISSERTATION

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the requirements for the award of the degree
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MASTER OF ENGINEERING
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ELECTRICAL ENGINEERING
(Power Apparatus and Electric Drives)

By

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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the dissertation entitled 'FABRICATION AND EXPERIMENTAL INVESTIGATIONS ON MICROPROCESSOR BASED SELF CONTROLLED SYNCHRONOUS MOTOR DRIVE' in partial fulfilment of the requirements for the award of the Degree of **Master of Egineering** in **Electrical Engineering** with **Specialization** in **POWER APPRATUS AND ELECTRICAL DRIVES**, submitted in the Department of Electrical Engineering, University of Roorkee, Roorkee (India), is an authentic record of my own work carried out for a period of about six months, from August 1987 to January 1988 under the supervision of **Dr. V.K.VERMA**, Professor and **Dr. BHIM SINGH**, Lecturer, Department of Electrical Engineering, University of Roorkee, Roorkee, India.

The matter embodied in this dissertation has not been submitted by me for the award of any other degree or diploma.

Dated : Feb. 6th 1988

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This is to certify that the above statement made by the candidate is correct to the best of our knowledge.

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SYNOPSIS

This dissertation deals with the experimental studies on a microcomputer based Line-Commutated inverter fed synchronous motor drive system.

Two three phase fully controlled thyristor bridges, one for rectifier and another for inverter, microprocessor controlled firing circuits, zero crossing circuits and digital speed measurement circuit have been designed, fabricated and tested.

Chapter 1 consists of introduction, literature review and brings out the different methods of starting of Line-commutated Inverter fed synchronous motor drive. In Chapter 2, the princile of operation of LCI synchronous motor drive, philosophy of its speed control and system hardware have been discussed. Chapter 3 describes the system software and the various flow charts. Chapter 4 deals with the experimental results. Conclusions and scope of future work have been given in Chapter 5.

CONTENTS

CHAPTER - 1

INTRODUCTION

1.1 GENERAL

Variable speed d.c. drives used in most of the cases are being fed by static converters using rectifier bridges. The use of d.c. motors in these drives has a number of mechanical and electrical limitations caused by the necessity of fitting a mechanical commutator.

The construction of the mechanical commutator has to be extremely delicate and finally the actual power is limited in the region of 10 MW for rated speed of 1,000 RPM and 500 KW for 500 RPM. The use of these machines is absolutely impossible in explosive, corrosive, or dust-filled atmosphere [1]. The cage induction motor on the other hand, has the robust rotor construction which permits reliable and almost maintenance free operation. Inspite of these advantages the inherent limitation of constant speed of operation has been the main bottleneck in its widespread use as a variable speed drive.

Of the various methods of a.c. motor speed control, its operation at variable frequency is becoming more and more popular, since it is possible to obtain variable speed as well as good regulation and high efficiency. The static variable frequency converters are expensive but are advantageous interms of accuracy and reliability. The current research in adjustable speed a.c. drives is focussed on the cost reduction of the converter and control equipment [2]. The

variable frequency a.c. drives becomes particularly attractive in multimotor drive. Such multimotor drives find applications in textiles, synthetic fibre, paper industries, traction etc.

The solid state variable frequency sources for a.c. drives can be broadly classified into two types :

(i) Cycloconverters

(ii) D.C. link converters which include

a) Voltage source inverters (VSI)

b) Current source inverters (CSI)

c) Line commutated inverters (LCI)

1.2 CYCLOCONVERTERS

A cycloconverter [2] converts a.c.supply of fixed frequency to a lower output frequency through a one step conversion process. The output frequency range is limited to about one third of the supply frequency and therefore the drives employing cycloconverters are suitable only for operation at lower frequency. The output voltage of cycloconverter contains complex harmonic patterns. However, one advantage of cycloconverter drives is that the SCRs are naturally commutated and regeneration is simple. The system can be easily designed for four quadrant operation. The cost and complexity of power and control circuits however, make them uncompetitive with other classes of drives. Two prominent applications of cycloconverter are traction vehicles and gearless rotary kilns.

1.3 VOLTAGE SOURCE INVERTER (VSI)

The VSI's are generally classified into two types, square wave inverters and pulse width modulated inverters. The square wave output voltage leads to a number of undesirable effects, such as additional harmonic power losses and torque pulsations in motors. The harmonic currents flowing in stator and rotor contribute to extra copper losses and some amount of iron losses. The commutating capacitor in the voltage source inverter is usually charged by the d.c. link voltage; hence, commutating capability decreases as the d.c. link voltage decreases. The inverter requires six commutating cycles per cycle of fundamental, leading to increased commutation losses and requires complex control circuitry.

The voltage fed square wave inverter drives are normally used in low to medium horse power ratings where speed ratio is usually limited to 10:1. This type of drive has been largely superceded by PWM drives.

In PWM inverters the thyristors are switched on and off many times within a half cycle to generate a variable voltage output which is normally low in harmonic contents. Among the PWM techniques sinusoidal PWM technique reduces the harmonic losses but it suffers from low inverter efficiency [3].

1.4 CURRENT SOURCE INVERTER (CSI)

The current source inverter converts power between an adjustable current source and a single or three phase a.c. load. Since

the primary input power is usually supplied at a constant voltage, the inverter system consists of two stages:

(i) The 'current source' which receives the power from a fixed voltage a.c. or d.c. and supplies an adjustable d.c. current at the output terminals.

(ii) The CSI is connected in cascade with the current source. It converts the d.c. current at the input to an a.c. current at the output terminals.

The CSI drives has many good features. They are [4]:

(i) Regeneration is possible.

(ii) There is no possibility of shoot through fault

(iii) The fault current on the inverter side rises very slowly

(iv) Commutation losses are less

(v) The inverter can be designed with low speed SCRs.

Against the above merits, the CSI drives have the following limitations :

(i) The frequency range of inverter is lower and it cannot operate on no load,

(ii) The large size of d.c. link inductor and the commutating capacitor makes the inverter expensive,

(iii) The drive has instability problems and sluggish response at light loads and high speeds.

A line-commutated inverter is obtained by operating an SCR bridge in continuous current mode with firing angle greater than 90°. The sequential commutation of SCR is obtained with the help of three phase line voltages.

The line commutated inverter overcomes all the problems of forced commutated inverters as well as cycloconverters. Some of the characteristic features of LCI are :

(i) No harmonics in the output voltage waveform

(ii) Commutating components are not required

(iii) The firing circuit requirements are simpler.

1.5 LCI SYNCHRONOUS MOTOR SYSTEM (CLM)

The Line Commutated Inverter (LCI) Synchronous machine combination gives the characteristics of a d.c. motor. The commutation of SCRs is controlled by the sinusoidal induced voltage in stator due to rotating field of rotor. This combination is popularly known as the commutatorless d.c. motor (CLM). This type of drives is used for starting of large rating gas turbine sets, boiler feed pumps etc. Where precise simultaneous speed control of a number of motors is required, a system using a synchronous motor offers a practical approach. Further, a synchronous machine responds more quickly than an induction machine to change in load torque. Also a variable frequency synchronous motor drive offers the possibility of simple precise position control [4].

The commutatorless motor has been generally used by industry in following cases :

(i) When high speeds upto 7,000 RPM are required

(ii) When high ratings upto 10,000 KW are required

(iii) When high efficiency is required.

1.6 LITERATURE SURVEY

Extensive literature is available on LCI-Synchronous machine system operating as a commutatorless motor. GORDON and S.B. DEWAN [4] have described the steady state properties of a variable speed drive using a synchronous motor fed by a controlled current source inverter. The performance is evaluated using equivalent circuit model and results are confirmed by experiment. They also discussed the advantages of LCI fed synchronous machine system.

Hoang Le Huy, Jakubowicz and Perret [5] have discussed a current source self controlled synchronous motor drive, in which the motor terminal voltage is used to synchronize the inverter triggering pulses. The implementation of microprocessor based control system is also described.

In the paper by R. Venkataraman and B. Ramaswamy [6] the authors described the development, design and construction of a variable speed drive using a synchronous motor. The operation of motor with a current-fed motor-emf commutated inverter is explained. It has also been shown that the digital simulation based on simplified block diagram is accurate enough for obtaining the responses of the system to step changes in speed reference and load on motor.

Ranganadhachari, B.P. Singh et al presented a paper [7] which describes the operation principle, characteristics and limitations of variable frequency source in which a line commutated thyristor bridge inverter acts in combination with a synchronous machine as a variable frequency source. Experimental results and performance curves are also discussed.

Peichang Tang, Snui-Snong Lu, and Yung-Chun Wu [8] presented a paper describing a firing scheme based on a microprocessor to control an antiparallel connected three phase thyristor dual feed converter. Using table look-up algorithm to speed up the response, a full range control of firing angle between 0° to 180° for both positive and negative current control is achieved. The maximum time delay required to correct the firing angle is one sixth period of the a.c. power source. The firing angle between 120° and 180° is used for the regeneration braking to achieve the required dynamic performance in four quadrants. Together with software algorithm in microprocessor, the digitised a.c. power signals are used to find the correct firing output signals. This scheme uses less hardware components and has higner dynamic performance in four quadrant operation.

A.C. Williamson and K.M.S. Al-Khalidi [9] describe the naturally commutated converter fed synchronous machine drive of very high rating. At standstill and at very low speeds commutation is achieved by pulsing the current in the d.c. link between the supply and the machine converters. However, this gives rise to significant low frequency disturbances to the supply system. The paper also describes an alternative

method using a discontinuous current mode of operation, which gives smoother operation and less disturbance to the system. An analysis is given which shows that this starting method can give an average torque as high as 1.0 per unit.

Gerson H. Pfitscher has given [11] the microprocessor based scheme that generate the necessary synchronization signals for 3 phase static power converter control system. The problem of detecting the phase to phase voltage zero crossing in presence of noise generated by thyristor commutation in constant and variable frequency supplies is discussed, and a microcomputer software solution is proposed.

Chandrasekhar Namuduri and P.C. Sen presented a paper [13] which describes a digital simulation method for the self controlled synchronous motor in time domain. They also discussed the performance of the synchronous machine with non-sinusoidal voltage and currents under both steady state and transient conditions. The effect of the damper winding, and saliency on the torque, and voltage and current wave forms are also discussed using the digital simulation technique when the machine is operated from a voltage source inverter and a current source inverter.

Mario Beneditti and Carlos F. Christiansen presented a paper which describe the design of a trigger system [16] for full or half controlled thyrister converters of up to 6 pulses, using 8 bit micro processor. The device is independent from the sequence of the main voltage and from the circuit configuration of the system. The trigger angle may take any value from $\gamma = 0°$ to $\alpha = 180°$ between pulses, thus achieving the maximum possible rate of change of the output voltage.

An outstanding aspect of the design described here is the new method of obtaining the synchronization signal.

1.7 DIGITAL CONTROL AND ITS MERITS

The result of rapid progress in semiconductor technology by planar processing and LSI has made digital electronics devices much smaller in size and cheaper. The drastic advance in semiconductor technology have made smaller and faster microprocessors available at lower costs, thereby increasing the number of industrial applications in which they can be used. In industrial process control, it is at time necessary to adjust a motor's speed over a wide range with good resolution and reproducibility. They also require to have fewer components, to cost less, to be maintained easily, and to be more generally applicable. In order to achieve the above needs microprocessor is more suitable [19]. A closed loop control is usually necessary to often the necessary speed accuracy. It is possible to obtain greater accuracy, improved dynamic response and reduced effect of disturbances such as loading in closed loop or feedback systems.

A speed regulating system with a fast response can be realized by speeding up the current controller and speed controller with the use of microprocessor based system. In driving a.c. motor with a three phase bridge inverter, control processing must be performed during extremely short periods. Such a fast processing can be realized with certain modifications in the existing microprocessor software. The control algorithms are simple and can be easily implemented in real time on a microcomputer [20]. The analog control methods have several

disadvan tages, such as nonlinearity in the analog speed transducer, difficulty in accurately transmitting the analog signal errors due to temperature, component aging and so on.

A digital control system on the other hand is free from above disadvantages. A microprocessor based control system for motor drives promises several distinct advantages such as flexibility, improved performance, and economic viability. Foremost among these is the flexibility. The control scheme is implemented in the software Therefore, to change the control scheme in order to obtain a different drive characteristic or introduce a new control function only software needs to be modified, with minimal or no change in the hardware. A microprocessor based control system can be completely digitalised, with its sensitivity to external influence thereby decreased. A microprocessor based control system requires few discrete components and less wiring, which will improve the reliability of the system. A microprocessor based drive is expected to give high accuracy, better time response, and better speed regulation provided advanced control technique is adopted. As the cost of microprocessors and their associated peripherals continue to fall, microprocessor based control system will become cost competitive. In the near future micro-processors will be incorporated in industrial drives requiring high levels of performance.

1.8 REVIEW OF STARTING OF SYNCHRONOUS MOTOR

The major drawback with the CLM is its inability to start from standstill because the gating signals of inverter SCRs are controlled

by the synchronous motor itself, and the commutation voltage necessary for machine commutation of LCI is not available. Hence, some other methods of commutation of current from one SCR to another is necessary. Several methods are known for this purpose. Some of these methods are discussed here.

Low Speed Operation

The machine-converter thyristor firing angles can be controlled by reference to either a.c. terminal voltages or rotor position or a combination of each, altnough the latter has advantages at low speeds, with the usual limit on current capability when inverting as dictated by device recovery time. The machine, when motoring, always takes a fundamental current at leading power factor.

The major difficulty during starting may be solved by application of forced commutation or by a cycloconverter. However, both these schemes involve complicated circuits and hence demand a large number of thyristors.

A usual technique to overcome this is to pulse the input direct current.

When the input d.c. voltage is chopped by inactivating the gate signal or by increasing the control delay angle by more than 90 degree, a negative voltage is applied to the ON thyristors, and the current decreases to zero [22]. After a short time, the thyristor will obtain a forward blocking ability. The relevant pair of thyristors at machine inverter will go off due to link current being zero. The

supply side rectifier will be refired and the next cycle pair of thyristors of machine-side converter will be fired. By repeating such a process several times, the motor will be accelarated to a speed sufficient to produce commutation EMF.

Low Speed commutation by Field Pulsing

A new method of low speed commutation of an inverter fed synchronous motor (CLM) makes use of transformer action between rotor and stator, the rotor being supplied from halfwave rectified a.c. commutation is automatic and require simple control circuits.

With reference to the Fig. 1.1 consider a particular stator winding current conduction pattern with field winding axis at angle 'θ' to that at phase a, and the link current I_d conducting through thyristers T_1 and T_6, so that $i_1 = -i_b = I_d$ and $i_c = 0$. It is required to commutate from T_6 to T_2 so that $i_a = -i_c = I_d$ and $i_b = 0$. For starting and low speeds this new scheme utilizes halfwave rectification of the field current if from an alternating voltage v_f. A typical waveform is shown in Fig. 1.2.

The process of commutation is achieved automatically when the firing pulses (derived from rotor position in the usual manner) are applied to the machine inverter thyristors. No additional control components are required, and only simple power electronic components are required in the field circuit [21].

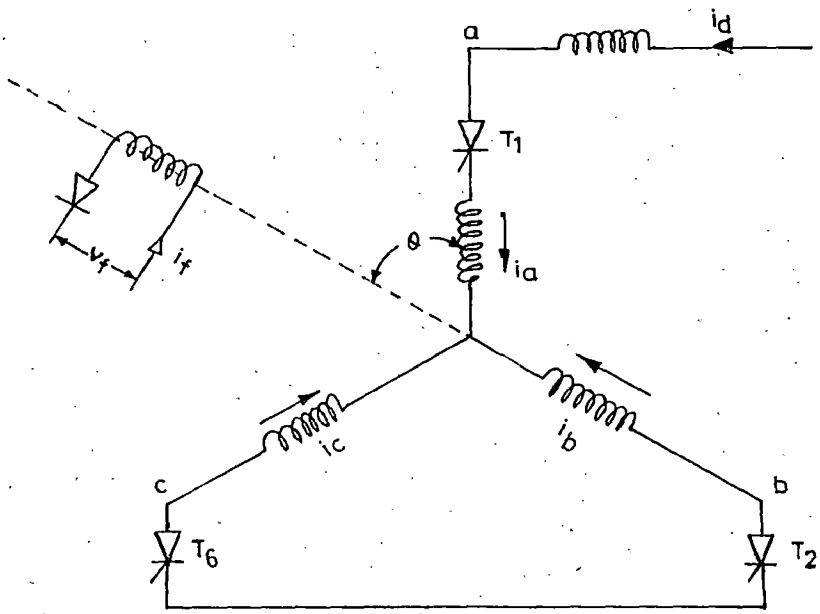


FIG.1·1—TYPICAL COEFFICIANT ON FOR COMMUTATION PERIOD

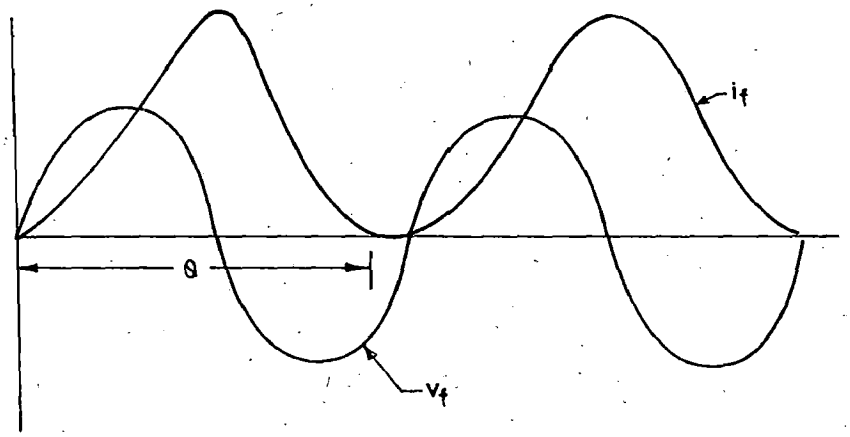


FIG.1·2—TYPICAL WAVEFORMS OF HALF RECTIFIER FIELD CURRENT

Stand Still Rotor Position Detection

As explained above, at low speed (upto about 10% of the rated speed) the natural commutation cannot be applied because of lack of sufficient induced emf developed. Problem also arises to start the motor. In these drives a shaft position sensor is usually required for synchronizing the inverter triggering pulses to the rotor position. The stand-still rotor position provides the correct initial firing order for starting in the desired direction with maximum torque. Several methods can be applied i.e. (1) adding a simple optical or Hall effect position detector which is used only for initial position sensing, (2) injecting a signal of some KHz is an auxiliary winding and analyzing the induced stator voltage.

Lately a method has been developed in which the induced emf in stator is analyzed when a step voltage is applied to the field winding. After a field supply is applied, the microcomputer sequentially samples the three stator induced voltages every 25 μs so as to obtain their peak values and polarities. The rotor position is determined by the phase voltage with highest peak value and by the polarity of this voltage. This is sufficient to determine the correct thyristor pair to be triggred in order to create maximum torque in the desired direction.

Starting Without an Auxiliary SCR

In this method, commutation is accomplished by forcing the rectifier bridge in to inverter mode during a short instant so as to interrupt the d.c. link current and reduce it to zero. The terminal

voltage is sensed and at each interval forced commutation is obtained as follows:

(i) Inverter triggering pulses are stopped

(ii) Rectifier (3 phase) firing is fixed at an angle greater than 90°

(iii) D.C. link current is monitored till it becomes zero

(iv) Rectifier normal operation is then reestablished and the following SCR pair is triggered.

The main advantage of this technique is that no additional commutating component is required. However, during each commutation interval the motor current reduced to zero, so that instantaneous torque is zero during this period. This method is undesirable in case of high starting torque requirements.

Starting with an Auxiliary SCR

This method of automatic starting is simplified when micro-computer control scheme is implemented. It requires two fully controlled 3 phase bridges and an additional SCR in parallel with d.c. link inductor. Forced commutation during each commutation cycle is achieved from the following steps :

(i) Firing pulses to the two fully controlled bridges are inhibited.

(ii) The auxiliary SCR is gated.

(iii) The current in the DC link is deviated through the auxiliary SCR and thus forced commutation at LCI SCRs is achieved[9].

The method overcomes the disadvantage of zero torque during commutation interval. In the present thesis an attempt has been made to start the motor using this method. The detail of the method is discussed in the Chapter-2.

1.9 SCOPE OF PRESENT WORK

In the present work an attempt has been made in the investigation to study the steady state performance of a synchronous motor fed from an LCI with a microcomputer control scheme. In this scheme a 3 phase a.c. supply of fixed frequency and voltage is converted into variable voltage d.c. supply to feed LCI using a fully controlled 3 phase bridge rectifier.

The present work has the following objectives:

(i) Design and fabrication of two fully controlled converters, one acting as a rectifier and other as an inverter.

(ii) Development of microcomputer base firing scheme for both converters.

(iii) Design and Development of zero crossing scheme for both converters.

(iv) An attempt to self starting of the line commutated synchronous motor.

(v) Experimental investigation of LCI synchronous motor system performance under steady state conditions.

CHAPTER - 2

PRINCIPLE OF OPERATION

2.1 GENERAL

This chapter mainly deals with the principle of operation of power and control circuits. The design of rectifier-inverter circuits, firing circuits and zero crossing circuits is also given in this chapter. The advantages of the microcomputer based control circuit, the determination of conduction intervals of individual SCRs for both converters and the sequence of firing is also clearly discussed for both starting and running modes of the drive.

2.2 PRINCIPLE OF OPERATION OF CLM

A commutatorless motor (CLM) consists of the following essential parts. The block diagram of CLM is as shown in Fig. 2.1.

(i) A rectifier (fully controlled) (CS)

(ii) An inverter (LCI) (CM)

(iii) A d.c. link inductor (L)

(iv) A link thyristor (T_L)

(v) A synchronous motor (over excited) (SM)

(vi) Firing and control circuits for both converters.

Rectifier (supply) CS

This is a 3 phase fully controlled SCR bridge converter. The main function of the bridge is to supply variable d.c. link voltage from

a three phase a.c. supply. The output voltage of the converter is carried by changing the firing angle (α) in case of fully controlled converters. The advantage of fully controlled operation of two bridges is that regeneration is possible by exchanging the mode of operation of the two bridges i.e. rectifier becomes inverter and inverter becomes rectifier.

Inverter (Machine Converter) CM

Inverter is also a 3 phase fully controlled bridge. It is used to convert d.c. power into a.c. power at desired output voltage and frquency. The output voltage can be changed by changing the firing angle (α) and frequency by changing the gating frequency of SCRs.

D.C. Link Inductor

The inductor plays the role of smoothening out the ripples in the d.c. voltage of inverter input terminals. The value of the inductor plays a decisive role on the system performance. If the value of the link inductance is sufficiently high then the current becomes continuous under LCI operation.

Synchronous Motor SM

The LCI and synchronous motor constitutes a commutatorless d.c. motor. The synchronous motor is overexcited and supplies leading reactive power to the inverter. The inverter provides the active power to the synchronous motor for the load applied to it, and to overcome its losses.

The CLM motors can be realised, depending upon the placement of the field winding as :

(a) Series CLM

(b) Shunt CLM, or

(c) Separately excited CLM

2.3 SPEED CONTROL OF CLM

The speed of the drive can be changed by varying any one of the following parameters:

(i) d.c. link voltage; V_{dc}

(ii) inverter firing angle; 'α'

(iii) synchronous motor field current; I_f

The frequency of the output terminal voltage of the inverter can be given by

$$f = k.V_{dc}/I_f \cos\alpha$$

In the present work control of firing angle and the d.c. link voltage is obtained with the help of microcomputer based firing scheme.

The digital control scheme based on microcomputer is used because the analog firing schemes have the following demerits:

(i) Variation of firing angle α is limited to 90° by using cosine firing angle.

(ii) The harmonic content of the voltage wave forms can disturb the firing pulse instants, leading to misfiring of SCRs.

(iii) Hard wired logic circuitry fixes the firing scheme philosophy and any change, if necessary, cannot be included without changing the circuit.

2.4 STARTING OF COMMUTATORLESS MOTOR

Variable speed drives (VSDs) using the synchronous motor as prime mover have several advantages in their favour compared with VSDs employing other types of motors. Firstly, the synchronous motors are rugged, reliable and free from troublesome commutator maintenance problems. Secondly, the power circuit configuration for a.c. to d.c. conversion and variable frequency generation needs no more than twelve thyristors of converter grade and is quite simple in structure. Thirdly, the drive can be operated at high speeds, an advantage not possessed by drives with other types of motor [6].

Synchronous motor drives have a few draw backs :

(i) Starting of the drive needs some types of auxiliary arrangement

(ii) If the motor emf is to be used for commutation of inverter thyristors, then the inverter must be current - fed and this necessitates use of a large link inductance.

The automatic starting of CLM is more simplified when the microcomputer control is implemented. This method of starting requires two fully controlled bridges, one operating as a fully controlled rectifier supplying D.C. link voltage to CLM and another as a machine commutated inverter (LCI).

The automatic starting schemes can be broadly classified into two types :

(i) Starting without an auxiliary thyristor across D.C. link inductor.

(ii) Starting with an auxiliary SCR across D.C. link inductor.

2.5 STARTING WITHOUT AN AUXILIARY SCR

In this method, commutation is accomplished by forcing the rectifier bridge into inversion mode during a short instant so as to interrupt the d.c. link current and reduce it to zero. The terminal voltage is sensed and at each interval forced commutation is obtained as follows :

(i) Inverter triggering pulses are stopped.

(ii) Rectifier firing is fixed at $\alpha = 150°$

(iii) D.C. link current is monitored till it becomes zero.

(iv) Rectifier normal operation is then re-established and the following SCR pair is triggered.

The main advantage of this technique is that no additional commutating component is required. However, during each commutation interval the motor current is reduced to zero, so that instantaneous torque is zero during this period. This method is undesirable in case of high starting torque requirements.

2.6 STARTING WITH AN AUXILIARY SCR IN PARALLEL WITH D.C. LINK INDUCTOR

This method of automatic starting also requires two fully

controlled three phase bridges and an additional SCR in parallel with d.c. link inductor as shown in Fig. 2.2.

The naturally commutated, converter fed synchronous machine is being used for drives at very high rating and speed in which range there are only mechanical alternatives. At standstill and at very low speed, commutation is achieved by pulsing the current in the d.c. link between the supply and the machine converters [9], and this gives rise to significant low frequency disturbance to the supply system. Forced commutation during each commutation cycle is achieved as follows :

(i) Firing pulses to the two fully controlled bridges i.e. rectifier and inverter are inhibited.

(ii) The auxiliary SCR is gated, and

(iii) The current through the d.c. link is deviated through the auxiliary SCR and thus forced commutation of LCI SCRs is achieved.

This method overcomes the disadvantage of zero torque during commutation interval obtained in the previous method.

During normal operation, converter (CS) and d.c. link choke(L) provide a controlled current source for the machine converter (CM), which absorbs the link power by operating in the inversion mode, and is naturally commutated by the machine winding voltage at rotational frequency. Natural commutation is possible provided that the firing angle of converter CM is suitably controlled and the winding voltages are adequate, however, such operation is not possible at standstill and very low speeds.

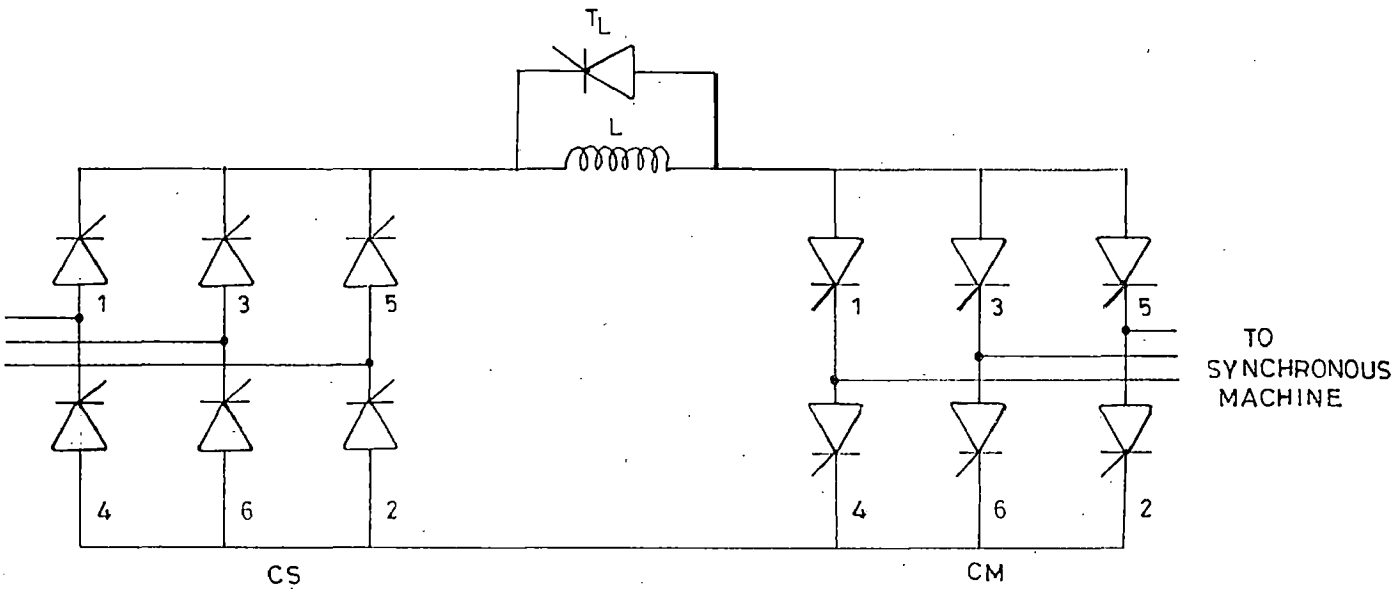


FIG. 2·1 — POWER COMPONENTS OF CIRCUIT

CS = SUPPLY CONVERTER (RECTIFIER)
CM = MACHINE CONVERTER (INVERTER)

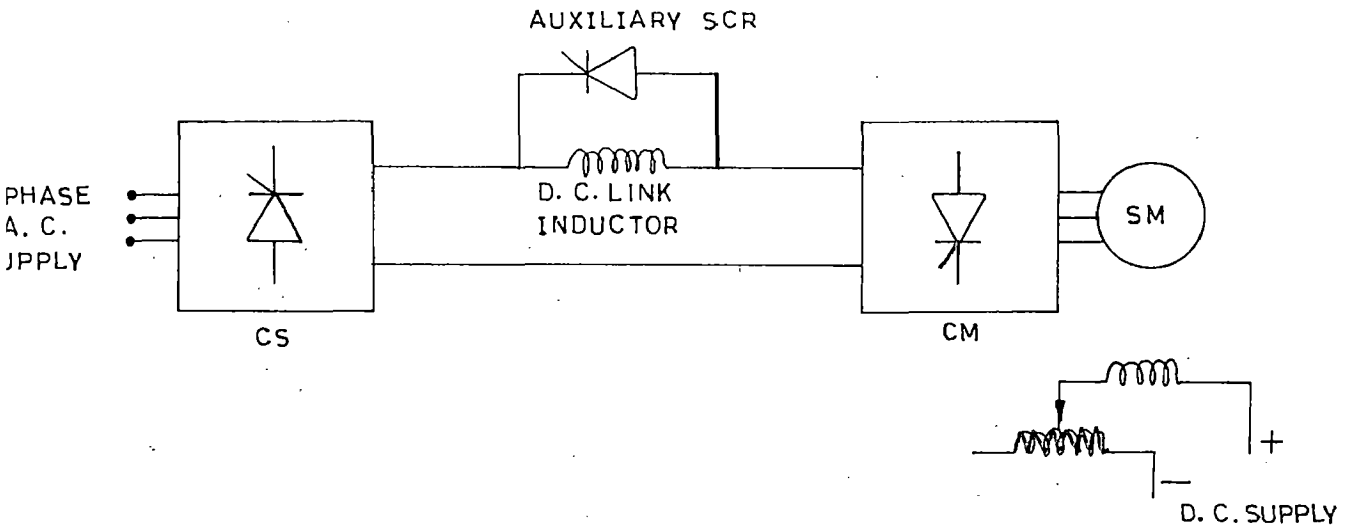


FIG. 2·2 — POWER CIRCUIT FOR AUTOMATIC STARTING OF SYNCHRONOUS MOTOR USING AUXILIARY SCR IN D.C. LINK

2.7 DISCONTINUOUS LINK CURRENT MODE OF OPERATION

At very low machine speeds, the average link voltage is very low, and consequently the converter CS output voltage contains a high ripple at six times supply frequency. With no link inductance, the voltage ripple would be applied directly line to line across the machine winding through two triggered thyristors of converter CM. The effective circuit inductance would be low and the current discontinuous for high average values [9].

If the link current is discontinuous, pulsating at six times supply frequency, the all devices of converter CM will be reverse biased at the same frequency. Consequently, a change in firing pattern will result in automatic change in conduction pattern at the next ripple.

Such conditions can be approached if the link thyristor (T_L) is triggered continuously during the starting period, and this is easily effected without great control complexity. In this way the choke protects against rapid rate of rise of average link current.

Analysis of Current Ripple

The circuit of Fig. 2.1 can be approximated to the equivalent circuit of Fig. 2.3 for the case where the machine winding frequency is much less than the supply frequency. If the thyristor T_L is triggered continuously during the starting mode, it will behave as a diode across the choke (of inductance L and resistance R) as shown in Fig. The inductance λ is that presented by the machine to current variations at six times supply frequency, flowing through two phases, with the rotor

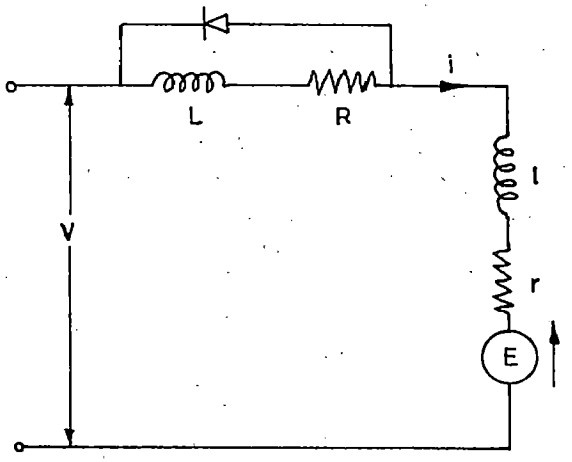


FIG. 2·3 — EQUIVALENT CIRCUIT

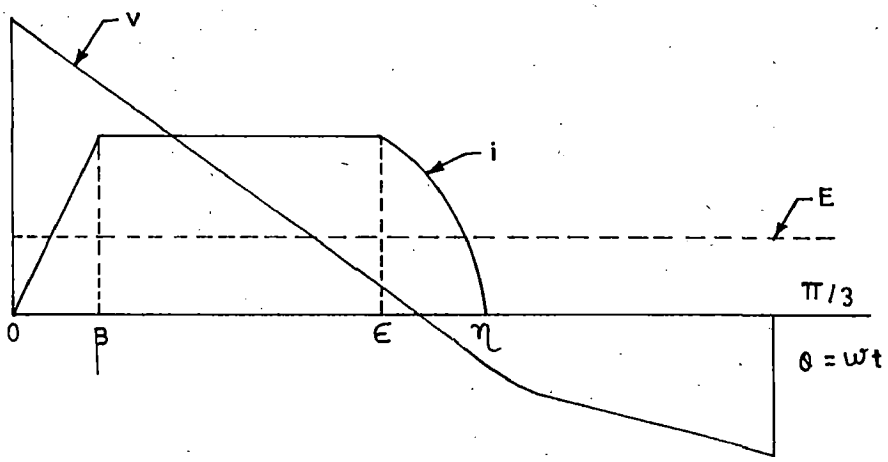


FIG. 2·4 — EXPECTED VARIATION OF CURRENT IN LINK

at low speed. The machine converter will show a voltage E, which is assumed constant at this stage.

The voltage v, of output of the supply converter, will vary with converter firing angle α. Assuming the overlap in the supply converter to be negligible, v will be given by

$$v = V \cos(wt + \alpha - \pi/6) \text{ for } 0 < wt < \pi/3$$

where,

V = peak line-line supply voltage = $\sqrt{2}\ V_L$

w = 2π*supply frequency, and this repeats at six times per cycle.

In a steady state condition, therefore, the behaviour shown by Fig.2.4 can be expected, assuming current i to be discontinuous.

If $\theta = wt$ then, at $\theta = 0$, i = 0, and the choke current is freee wheeling. The voltage v-E, being effectively applied to inductance 1, causes i to increase rapidly. At $\theta = \beta$, i becomes equal to the choke current, the thyristor blocks and any further rise in current i is opposed by inductance 1. At $\theta = \epsilon$, the voltage across the thyristor reverses, it conducts, and i drops to zero at $\theta = \eta$, with $\eta < \pi/3$ for discontinuous current.

2.8 THREE-PHASE SCR BRIDGE (LCI)

A three phase SCR bridge has been used as a line commutated inverter. The commutation of the bridge is achieved by the back emf of the synchronous machine connected to the 3 phase output of the bridge.

The firing angle of the bridge is adjusted between 90° to 180° so as to obtain the inverter mode of operation. In the inverter mode, the direction of current flow through the bridge remains the same however, the d.c. terminal voltage of the bridge reverses polarity. Thus, the LCI is nothing but a three phase fully controlled converter with firing angle between 90° to 180°. The sequence of firing of SCRs and the conduction intervals can be explained with the help of a detailed description of 3 phase fully controlled converter.

The thyristors T_1, T_3 and T_5 are called positive group SCRs because they are connected to the positive terminal of the d.c. link supply. While the thyristors. T_4, T_6, T_2 are called negative groups SCRs because they are connected to the negative terminal of the d.c. link supply.

In one cycle of the a.c. supply wave there are six conducting intervals, each of 60° in which a pair of SCRs conducts. These intervals are as given in Table 2.1.

TABLE 2.1

Time in degrees;	0°	60°	120°	180°	240°	300°
Firing sequence;	1	2	3	4	5	6
Conducting SCRs;	6,1	1,2	2,3	3,4	4,5	5,6

2.9 SYNCHRONIZATION AND ZERO CROSSING DETECTION FOR CM CONVERTER

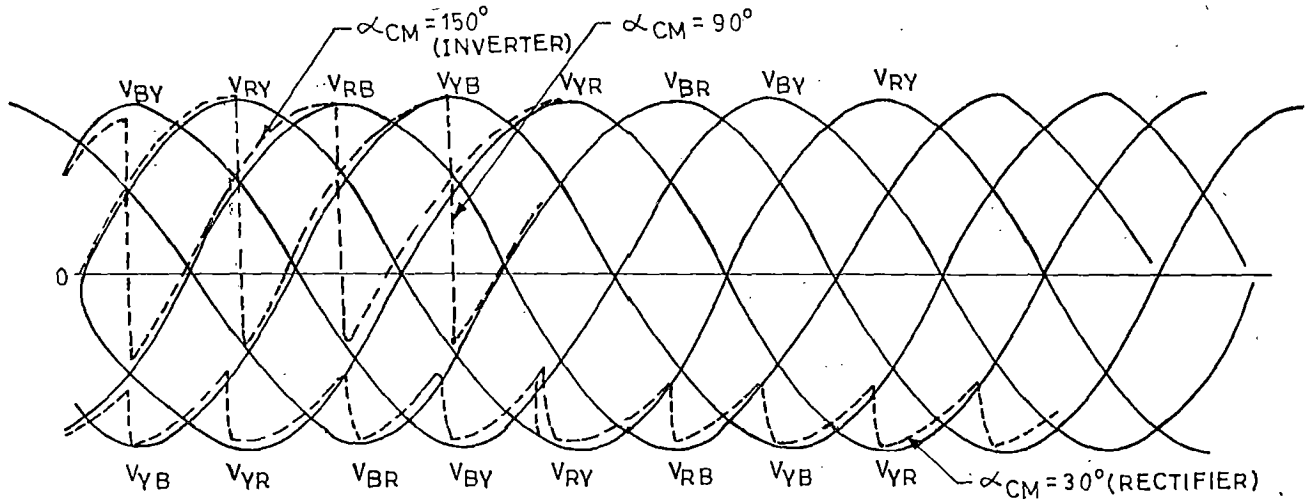
Independently of the method or algorithm used to control thyristors firing of a three phase static power converter, the signals

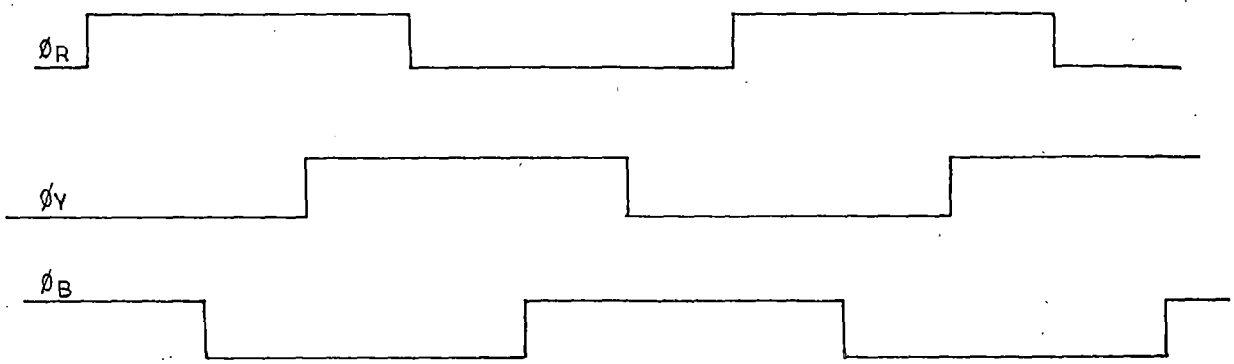
that synchronize them with the alternating supply voltages are always necessary. For a three phase fully controlled converter there are six such logical signals each one associated with a thyristor and defined from the natural commutation instant, i.e. at the intersection of the two line to line voltages, which coincides with the zero crossing of another one. The zero voltage detector fulfils two different functions; the synchronization of the thyristor firing circuit to the input line frequency and the phase sequence identification.

The synchronous machine terminal voltage is isolated and fetched by three single phase transformers. From the secondary winding of these step-down control transformers, the digitized three phase power signals, $\emptyset_R$, $\emptyset_Y$ and $\emptyset_B$ are obtained. These $\emptyset_R$, $\emptyset_Y$ and $\emptyset_B$ signals are copnasal to the machine line voltages V_{RY}, V_{YB} and V_{BR} respectively, and these three signals are displaced by 120° from each other. These digitised signals are sent to the microcomputer. The relationships between line voltages V_{RY}, V_{YB}, V_{BR} and these digitised signals are snown in Fig. 2.5.

Taking into account the digitised power signals, for a full 360° time range of synchronous machine a.c. cycle, a firing command data table is prepared on the basis of the number of the thyristors that are to be fired, for an α_{CM} firing angle in 120° to 180° range, or 90° to 120° range. This firing command data table denotes the numbers of thyristors that are to be fired, for a particular type of digitised power signals which are high in a particular time interval.

The quantization signal $\emptyset_R$, $\emptyset_Y$ and $\emptyset_B$ will be read via bits PA_2, PA_1 and PA_0 of part A (8255-2). In the table 2.2, the quantizer signals are arranged in increasing order (001 at lowest address and





QUANTIZED SIGNALS	101	100	110	010	011	001	101	
SCRs TRIGGERED	2, 3	3, 4	4, 5	5, 6	6, 1	1, 2	→	WHEN α_{CM} IS 0° to 60° (CM IS RECTIFIER)
SCRs TRIGGERED	1, 2	2, 3	3, 4	4, 5	5, 6	6, 1	→	WHEN α_{CM} IS 60° to 120°
SCRs TRIGGERED	1, 6	1, 2	2, 3	3, 4	4, 5	5, 6	→	WHEN α_{CM} IS 120° to 180° (CM IS INVERTER)

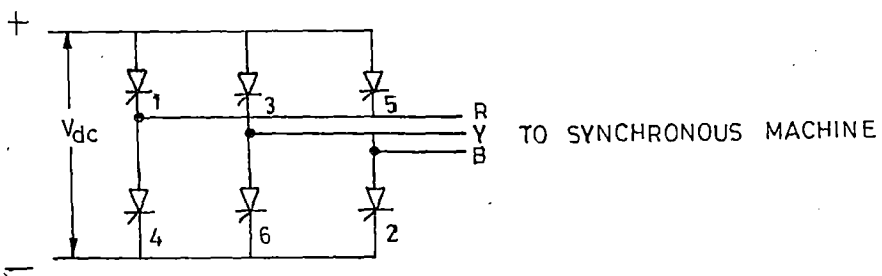


FIG. 2·5— SYNCHRONIZANG SIGNALS (QUANTIZERS) AND FIRING SEQUENCE OF CM CONVERTER

110 at the highest address). Thus, for a given firing angle range of α_{CM} and the quantization signal read, the address of the firing command is easily determined and the same is tabulated in Table 2.2.

TABLE 2.2: FIRING COMMAND DATA FOR CM CONVERTER

(A) FOR α_{CM} IN THE RANGE OF 120° TO 180° (AS INVERTER)

$\emptyset_R$	$\emptyset_Y$	$\emptyset_B$	Quantizer	SCRs to be fired	Firing command
0	0	1	1	5,6	30H
0	1	0	2	3,4	0CH
0	1	1	3	4,5	18H
1	0	0	4	1,2	03H
1	0	1	5	6,1	21H
1	1	0	6	2,3	06H

(B) FOR α_{CM} IN THE RANGE OF 90° TO 120° (AS INVERTER)

0	0	1	1	1,6	21H
0	1	0	2	4,5	18H
0	1	1	3	5,6	30H
1	0	0	4	2,3	06H
1	0	1	5	1,2	03H
1	1	0	6	3,4	0CH

The circuit diagram for zero crossing detection (Base interrupt) and synchronization ($\emptyset_R$, $\emptyset_Y$, $\emptyset_B$) is given in Fig. 2.6. An I.C. 741 is used as a comparator. It compares the stepped down voltages obtained from synchronous machine terminals connected to pin No. 2.

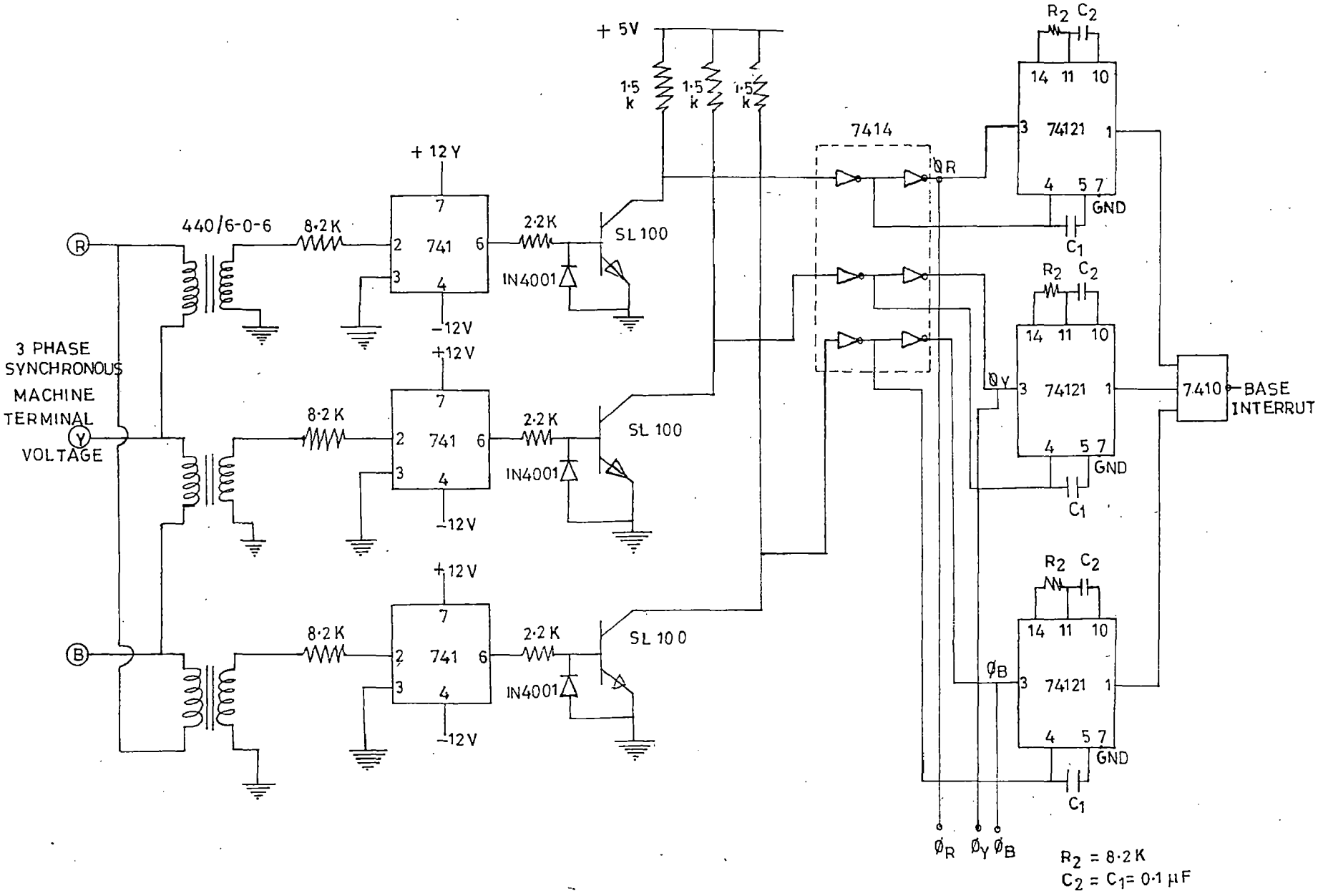


FIG. 2·6 — CIRCUIT DIAGRAM FOR GENERATING THE BASE INTERRUT AND SYNCHRONIZING SIGNALS

A manostable multivibrator is used to produce two pulses, one at the rising edge and another at the falling edge of each digitized signal. Combining these sets of pulse signals from the three phases, a base interrupt signal, B.I. is obtained. The base interrupt signal, B.I. has a frequency six times that of synchronous machine frequency. The interrupt signal occurs at each of six phase angles, 0°, 60°, 120°, 180°, 240° and 300° of the a.c. voltage of synchronous machine. A new firing cycle is started at the falling edge of the base interrupt signal, B.I. The utilization of the base interrupt signal for interrupting the CPU and for generation of firing pulses for the correct thyristors is explained in the system software implementation. The theoretical waveforms for base interrupt circuit are given in Fig. 2.7.

2.10 GATING FOR THREE PHASE FULLY CONTROLLED THYRISTOR CONVERTER

The operation of the three-phase bridge converter is explained earlier. There are six thyristors T_1 to T_6 which have to be triggered into conduction in a particular sequence. If the output current is assumed constant, the output voltage at any instant is equal to one of the six line to line voltages; V_{RY}, V_{RB}, V_{YB}, V_{YR}, V_{BR}, V_{BY}. This requires that two thyristors one in the positive group (T_1, T_3, T_5) and one in the negative group (T_4, T_6, T_2) be gated simultaneously. In order to vary the average value of the output dc voltage, the instant of gate pulses to thyristor pairs must be controlled. Fig. 2.8 shows the phasor relation ship between the voltages and gating signals[1]. The line voltages are displaced from each other by 60°. The thyristors are gated in pairs forming six groups, i.e. (T_1, T_2), (T_2, T_3), (T_3, T_4), (T_4,T_5), (T_5,T_6) and (T_6, T_1). The interval for each group is 60° and each thyristor

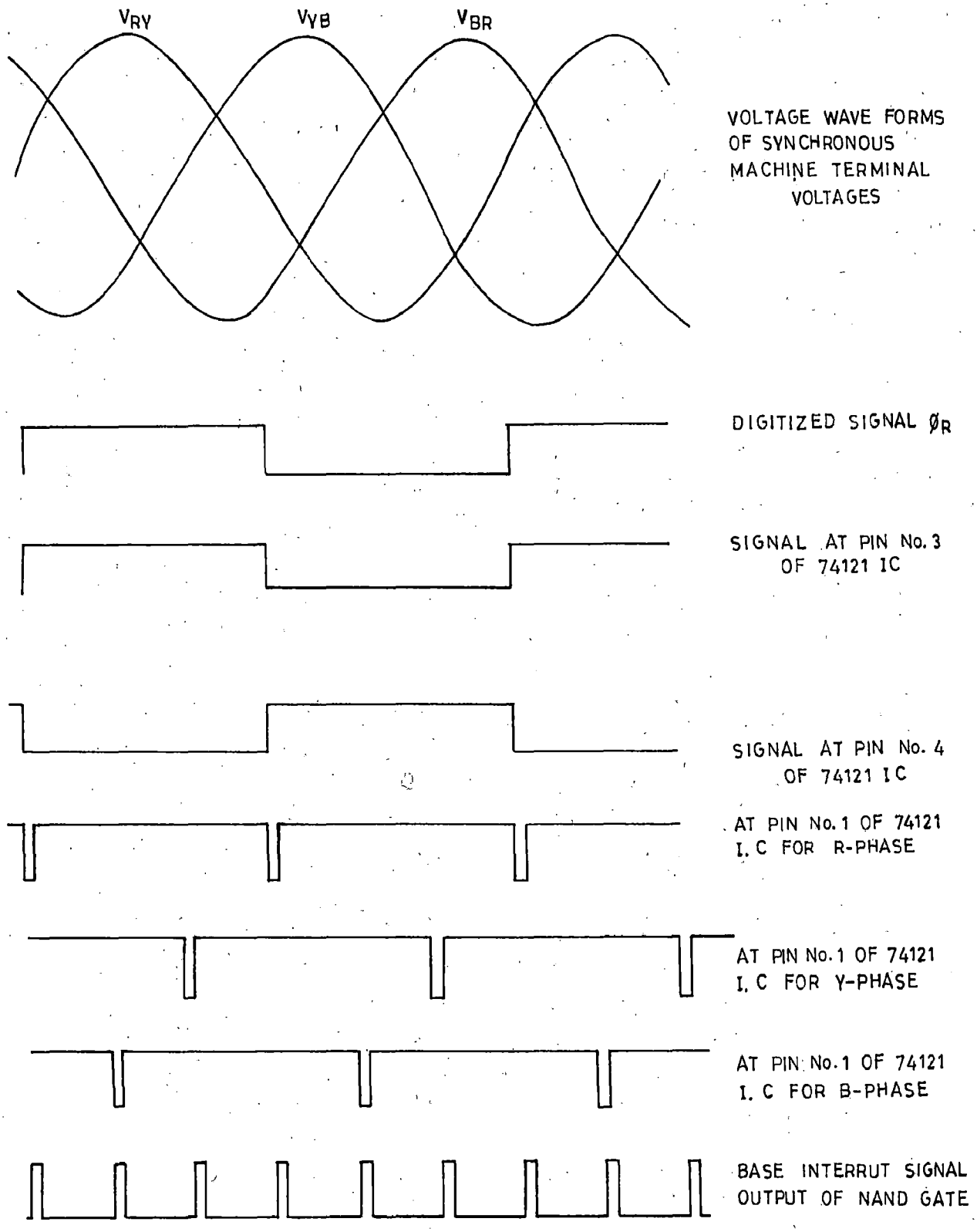


FIG. 2·7—THEORITICAL WAVEFORMS FOR BASE INTERRUT GENERATION CIRCUIT

conducts for two periods. The thyristor T_6 is gated α° after the zero crossing of V_{RY} voltage; T_1 is gated 60° after gating of T_6 and so on.

For satisfactory performance of the converter at firing angles varying from 0 to 90°, the gate pulses of 120° width are considered in the control circuit over the entire range of the firing angle. A control transformer is used to obtain an isolated, low level synchronizing signal which is in phase with the R-Y line to line voltage. It should be noted that the gating signals are sensitive to the phase sequence of the synchronizing signal. Therefore care must be taken in connecting the a.c. line to the synchronizing transformer in the correct phase sequence.

2.11 ZERO CROSSING CIRCUIT FOR CS CONVERTER

There are numerous approaches of designing gate pulses at the required delay angle. The Fig. 2.9 shows the zero crossing circuit for CS rectifier operation. The synchronizing line voltage V_{RY} is quantized to logic voltage level. A rectangular pulse is produced at the output of the comparator The output of the comparator is given to the transistor base. The quantizer obtained from the transistor collector is directly given to the gate of the timer TM_2 (5 AH) loaded with α count. The output of the down counter gives an out pulse (interrupt) after the counting is completed. This is the instant for firing the SCR pair 5 and 6. Since the input of the rectifier is operated with fixed frequency, only one synchronizing signal is sufficient to produce the instants to fire a certain pair (5 & 6) of SCRs. The other pairs of SCRs will be find at every 60 degree subsequently by another timer TM_2 (59 H) working in mode '0' (interrupts on termianl count). The firing pulses are kept

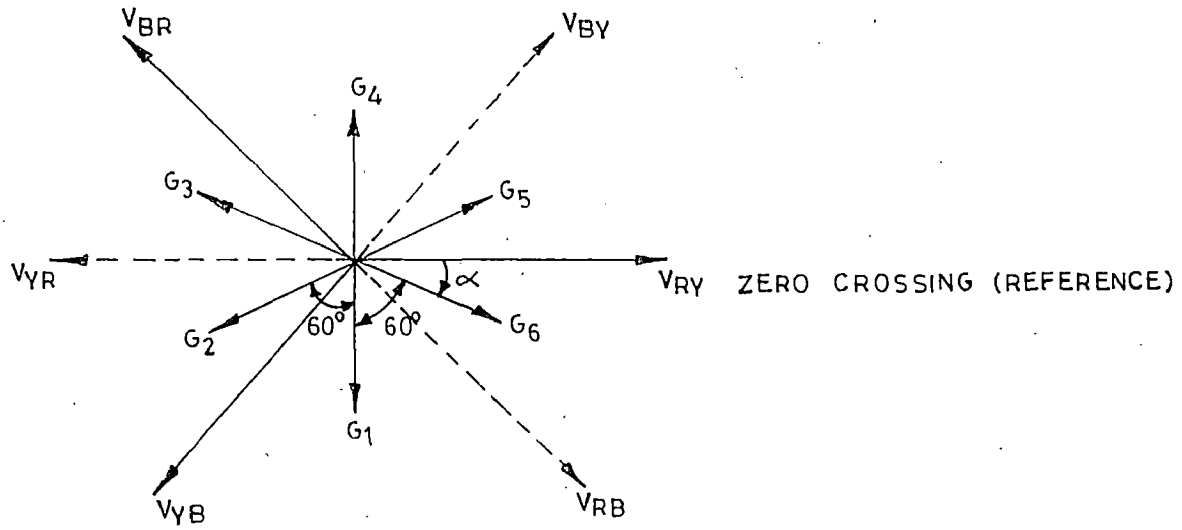


FIG. 2·8—PHASOR RELATIONSHIP OF LINE VOLTAGES (ZERO CROSSINGS) AND GATING INSTANTS

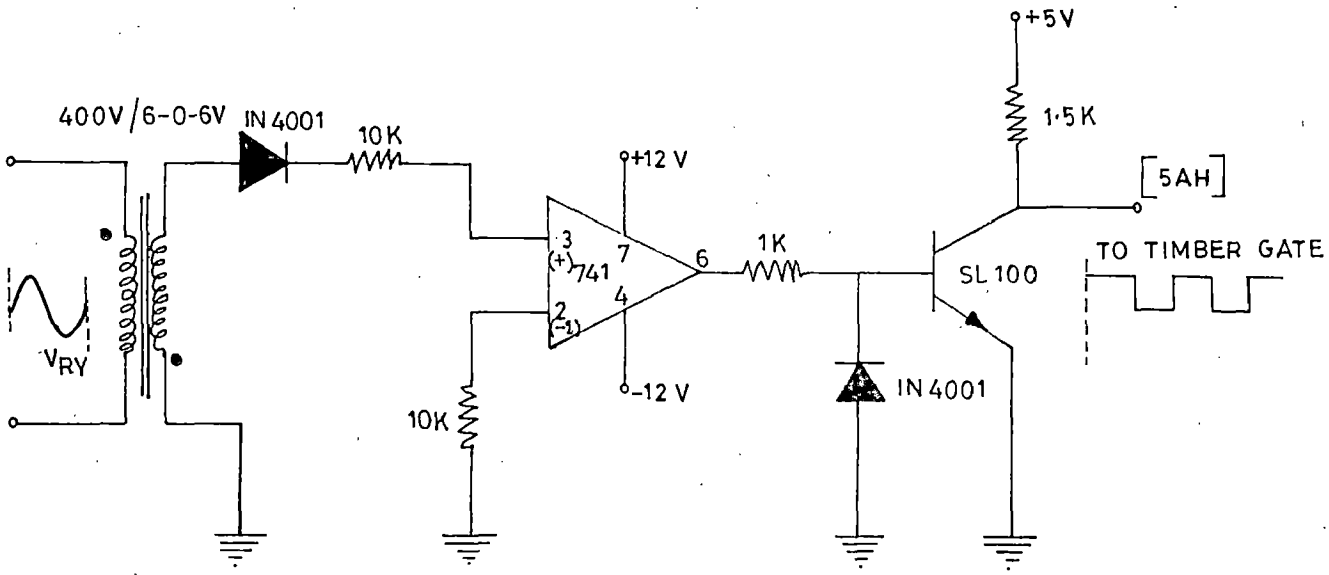


FIG. 2·9—ZERO CROSSING CIRCUIT FOR RECTIFIER CS

120° wide through software. With bits 0 to 5 of part B (8255-1) for firing SCRs 1 to 6 of the CS converter (rectifier) and bit 7 (Part B) for firing the d.c. link SCR (T_L), the sequential firing command, FS=1 to 6 are as follows :

Fs	1	2	3	4	5	6
Firing Command in (Hex)	B0	A1	83	86	8C	98

A bit is 'high' for issuing the firing signal.

2.12 DESIGN OF FIRING CIRCUIT

The pulses issued from the microcomputer I/O part may not be strong enough to turn on an SCR. Besides the gate and cathode terminals of the SCR are at higher potentials of power circuit, and the control circuit should not be directly connected to the power circuit. A pulse transformer is used to provide physical isolation between the control circuit and the power circuit. The firing pulse from the I/O part and an all time high signal (i.e. +5VDC) are 'ANDED' (to avoid µp loading), amplified and fed to the pulse transformer. For the inverter µp firing command is ANDED with high frequency. This modulated pulse reduces the gate dessipation in the SCR. A diode is connected across the pulse transformer primary, to avoid the saturation of pulse transformer.

Gate protection is required for over voltage and over current. Because of the low power level of the control circuitry, this protection can be provided by simple means. The gate can be protected against over voltage by connecting a diode across gate and cathode and against overcurrent by connecting a resistance in series with the pulse transformer

input. A common problem encountered in the SCR circuitry is spurious firing of the device. Trigger pulses may be induced at the gates due to turn on or turn off of a neighbouring SCR or transients in the power circuit. These undesirable trigger pulses may turn on the device, thus causing improper operation of the circuit. Gates are protected against such spurious firing by using shielded cables or twisted gate lead connections. A capacitor is connected across the gate to cathode to bypass the noise pulses. The pulse amplifier circuit is shown in Fig. 2.10.

2.13 DIGITAL SPEED MEASUREMENT SYSTEM

In industrial process control it is frequently necessary to adjust a motor's speed over a wide range with good speed resolution and reproducibility. Conventional analog control methods suffer on several accounts, including nonlinearity in the analog speed transducer and difficulty in accurately transmitting the analog signal after it has been obtained from the transducer. Errors also occured due to temperature, component aging and extraneous disturbances.

A digital speed measurement and control is superior in that there is no nonlinearity in the speed transducer, the digital signal representing speed can be transmitted long distances with no degradation of the original accuracy, and the digitally developed control signal is not subjected to temperature variations, component changes, or noise.

In the present thesis the actual speed is measured through an a.c. tachogenerator which is coupled to the motor. The a.c. voltage available through the tachogenrator is converted in to d.c. voltage

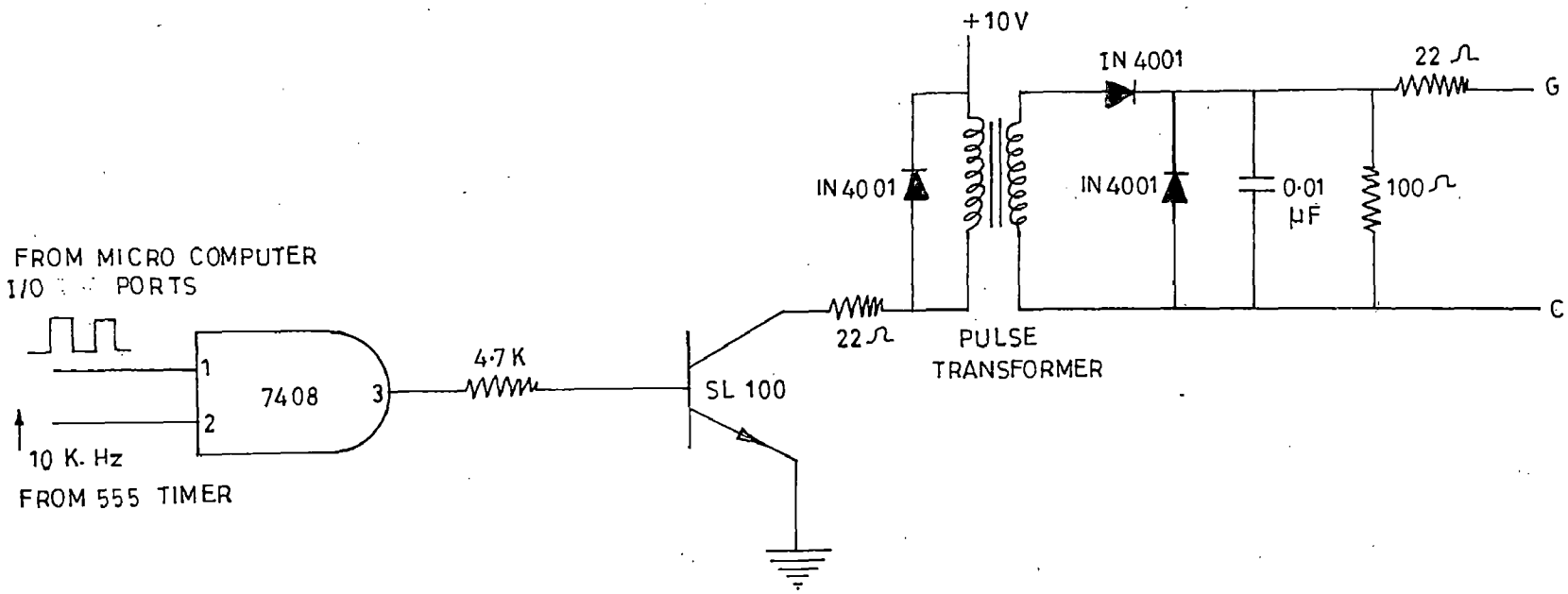


FIG. 2·10— PULSE AMPLIFIER CIRCUIT

using a bridge rectifier and filter. The filtered d.c. voltage is reduced to a range of 5 volts (for max speed) using resistor and variable potential divider. The ADC interfacing directly displays the speed in HEX in the address field of the µp trainer via IN_1 channel by implementation of software.

This digital speed measurement system is fabricated and tested individually. The scale is adjusted such that one bit represents 8 rpm. It shows satisfactory accuracy of the speed measurement by µp programme.

2.14 MICROCOMPUTER BASED CONTROL SCHEME

The VMC-85/9 microprocessor trainer is used for the system development. The various I/O parts and timer or counters, and their configuration are shown in Fig. 2.11

The scheme used for generating the firing pulses is shown in block diagram of Fig. 2.11. It consists of following parts :

(a) Four signal transformers, each single phase 400 V/6 V

(b) Two zero crossing circuits, one for rectifier (CS) and other for inverter (CM)

(c) Timer card

(d) Pulse amplifier circuits

(e) ADC interfacing circuit

(f) Digital speed measurement system

2.15 CONCLUSION

In this chapter the complete philosophy of microprocessor based speed control of self controlled synchronous motor drives is

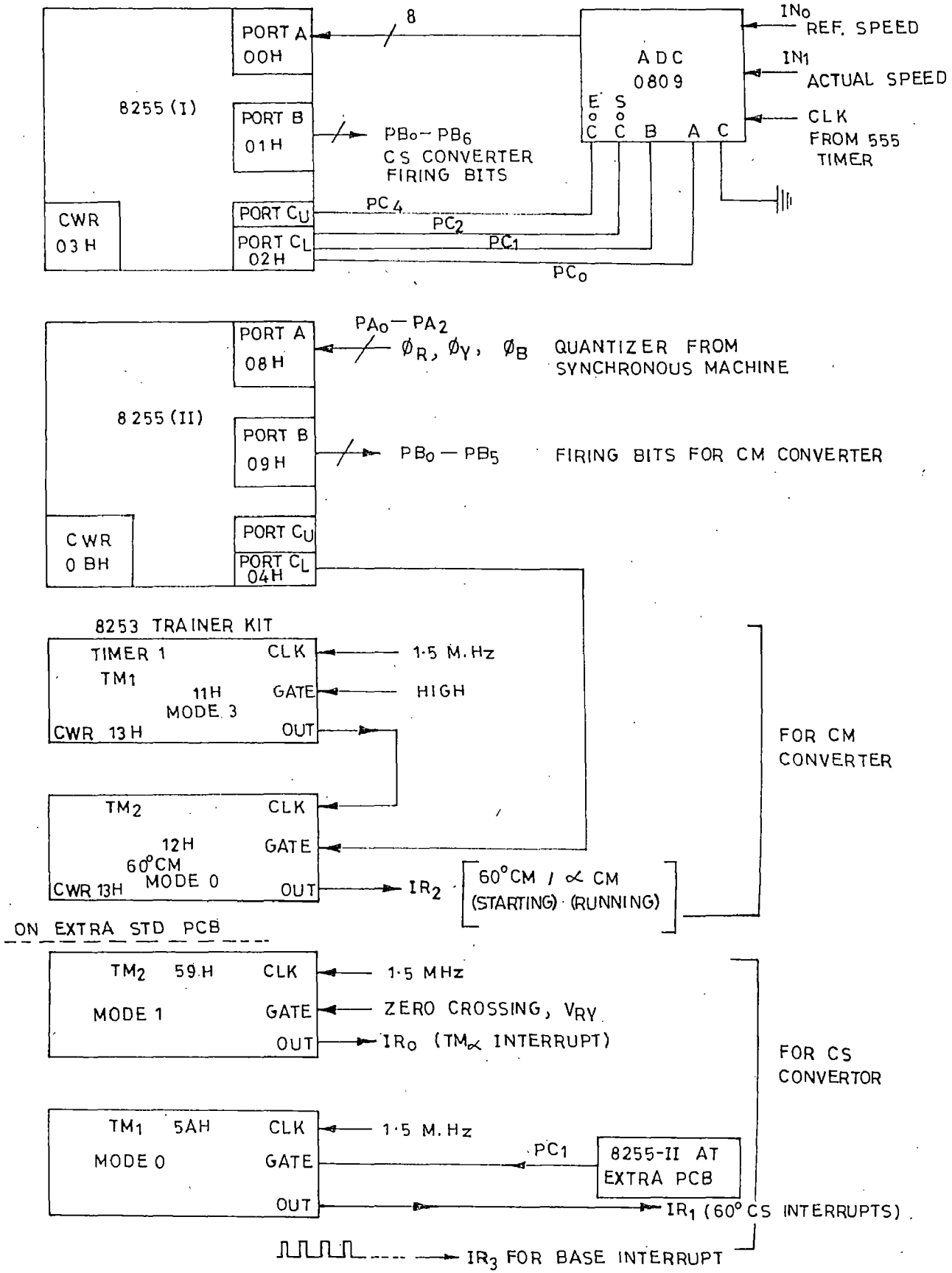


FIG. 2·11 — MICROPROCESSOR BASED SYSTEM CONFIGURATION

discussed. The power circuit, i.e. two three-phase fully controlled converters, the microprocessor based firing scheme, digital speed measurement, zero crossing circuits and ADC interfacing have been fabricated and tested.

CHAPTER - 3

SYSTEM SOFTWARE IMPLEMENTATION AND FLOW CHARTS

3.1 GENERAL

In this chapter mainly the overview of the microprocessor, its peripheral I.C. chips, development of system software and necessary flowcharts are described. The complete logic of speed control scheme of the self controlled synchronous motor drive is discussed in the main programme. The various subroutines used in conjuction with the main programme are also discussed.

Overview of Microprocessor

The digital control scheme for the synchronous motor drive has been developed using Vinytics Microprocessor Development System VMDS-85/9. This system is based on INTEL'S most popular microprocessor, the 8085. It is available in a 19" card cage having the facility of interfacing a number of STD Bus based cards. The three basic cards on which the VMDS-85/9 system is based are:

(i) CPU card

(ii) RAM Card

(iii) EPROM Card

The system can be easily expanded to accomodate some special purpose STD Bus based cards, e.g. Input-output and Timer card.

3.2 GENERAL PURPOSE PROGRAMMABLE PERIPHERAL DEVICES

To facilitate parallel data transfer between μp and I/O devices, certain programmable, general purpose devices (support chips) are used. These devices can act as an output port latching the data sent by the μp for the output device. They can act as an input port which is a tri-stated buffer to read data from the inputting device. These devices can generate an interrupt signal and receive/transmit certain control signals for data communicating between μp and I/O devices.

The 8255, a programmable peripheral interface (PPI) is one supporting device by INTEL. It can be programmed to transfer data under various conditions, from simple I/O to interrupt I/O. It has 24 I/O pins that can be grouped primarily in two 8 bit parallel ports: A and B, with the remaining eight bits as port C. The eight bits of port C can be used as individual bits or be grouped in two 4 bit ports : C_{upper} (Cu) and C_{lower} (C_L). There are 3 major modes of operation. In the first mode (Mode 0), each group of 12 I/O pins may be programmed in sets of 8 pins (port A or B) and 4 pins (half port) to be input or output. In Mode 1, the second mode, each group may be programmed to have 8 lines of input or output with the remaining 4 pins, 3 are used for hand shaking and interrupt control signals. The third mode of operation (Mode 2) is a bidirectional bus mode.

The control word format of 8255 is as shown in Fig. 3.1.

Another often used support chip is the 8253 programmable Interval Timer. It is a programmable counter/timer chip having 3 indepen-

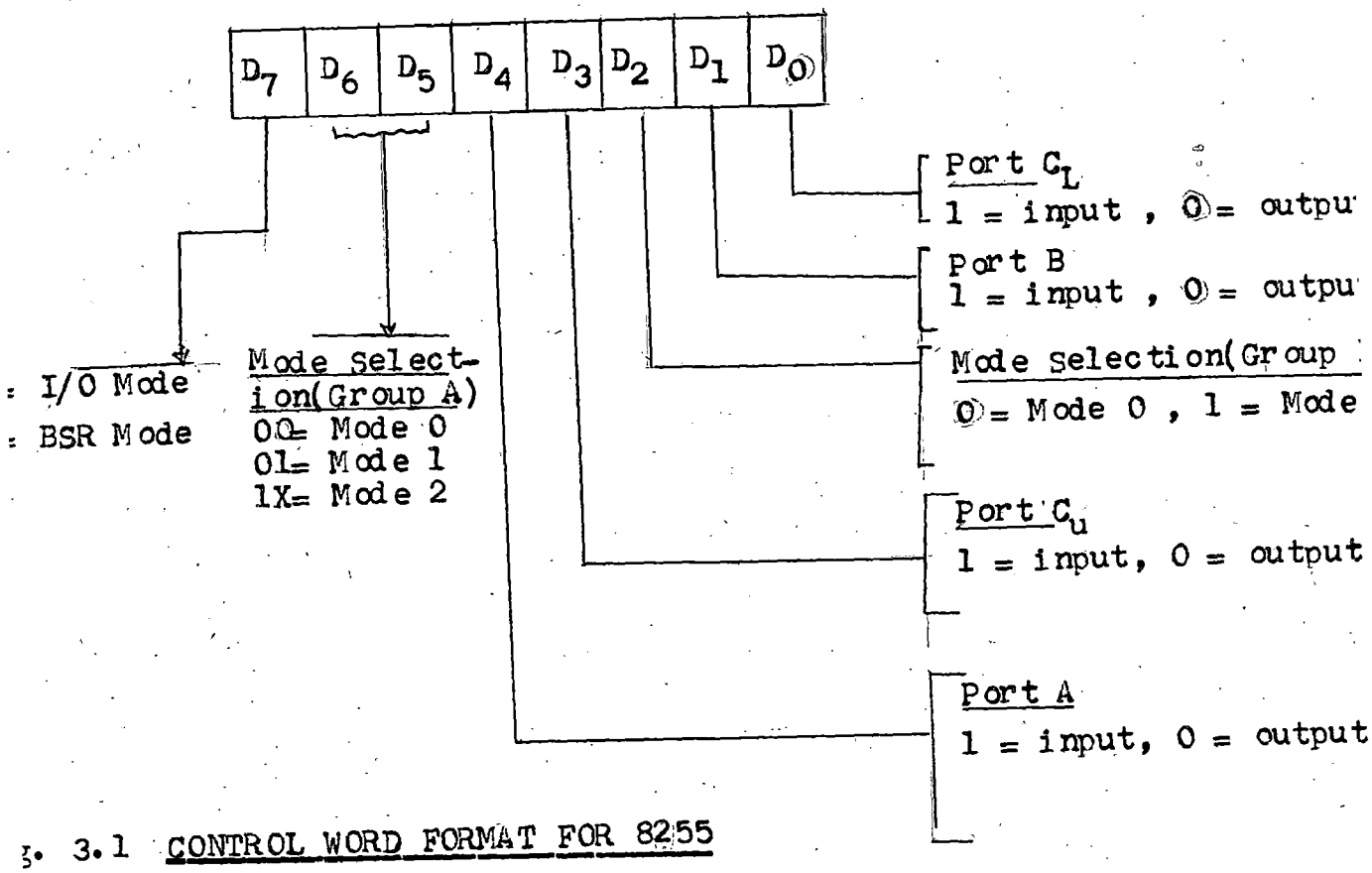


Fig. 3.1 CONTROL WORD FORMAT FOR 8255

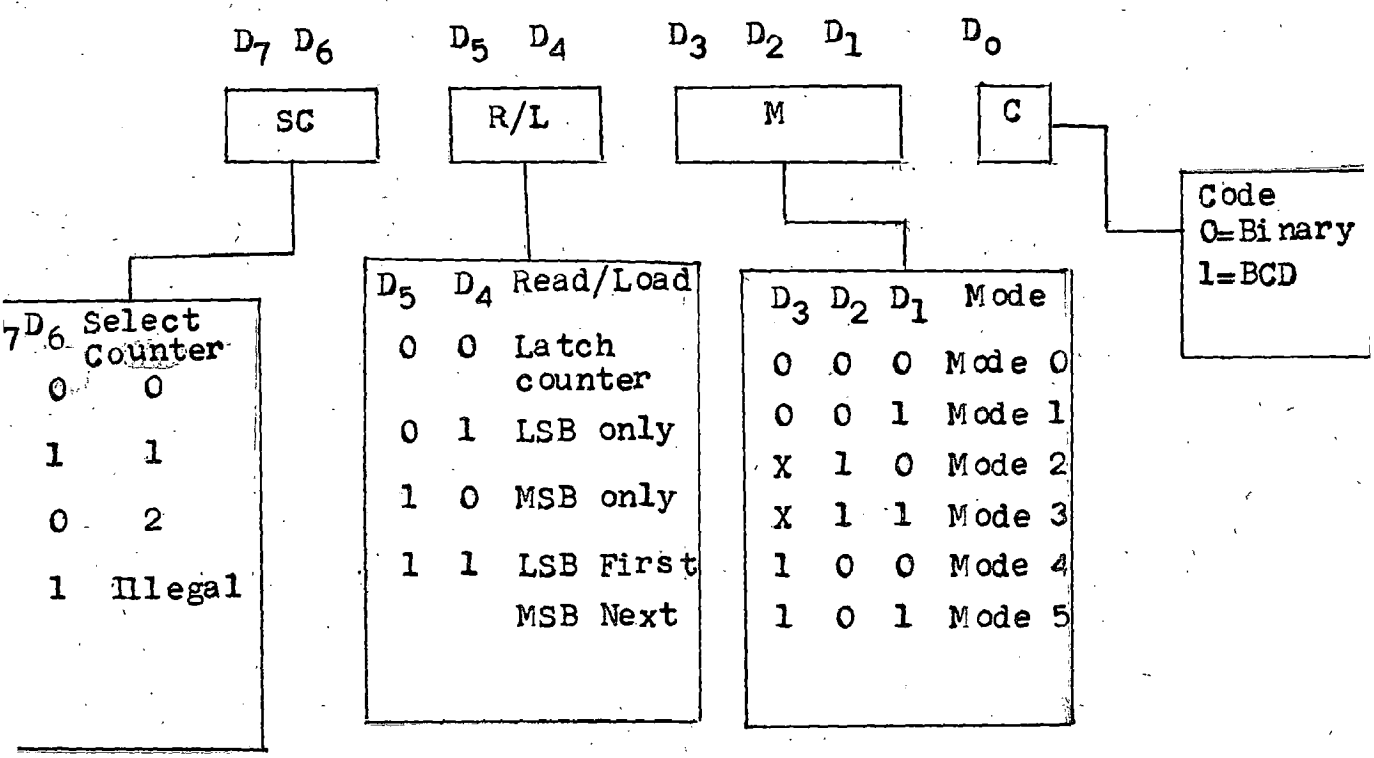


Fig. 3.2 : CONTROL WORD FORMAT OF 8253

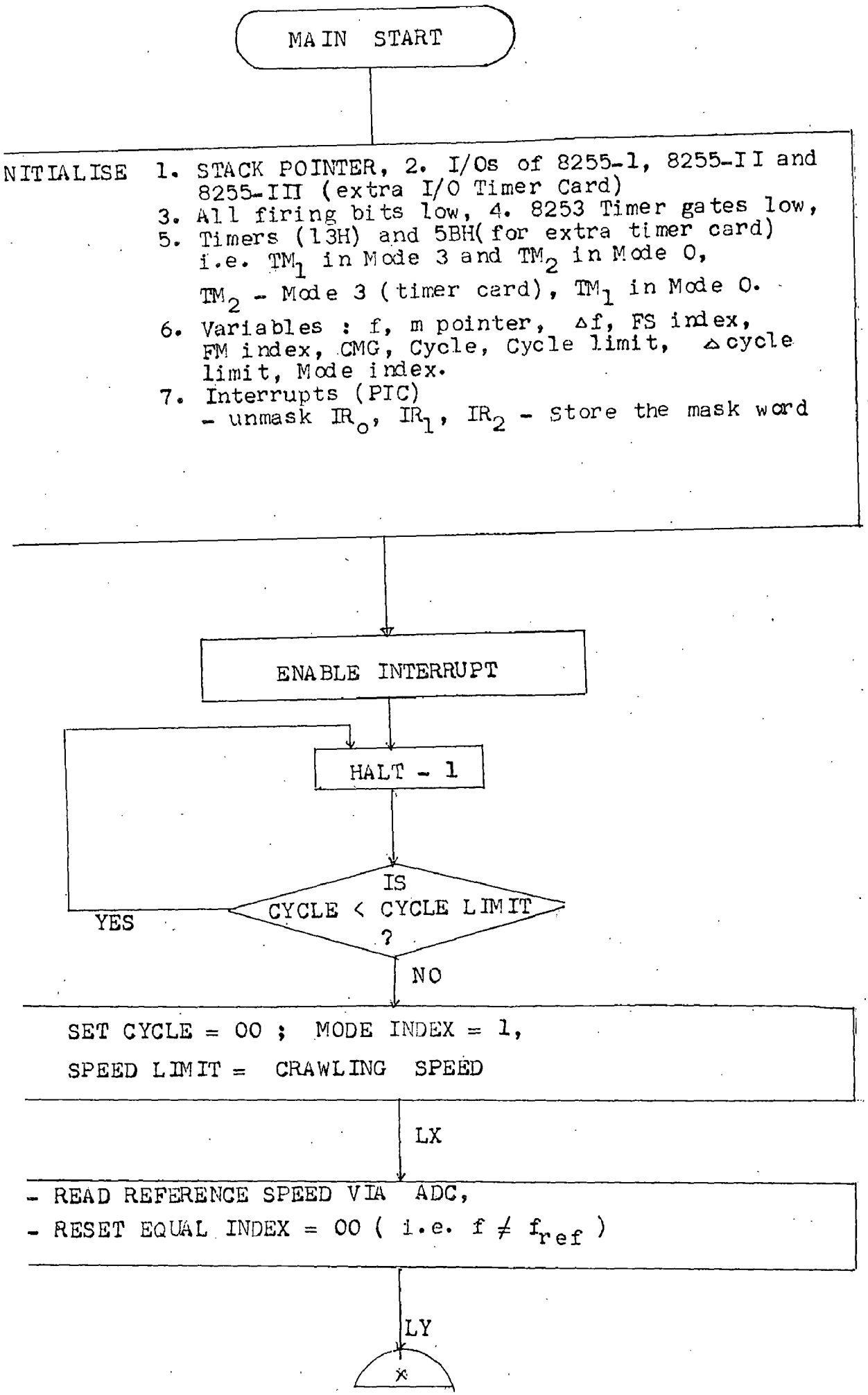
dent 16 bit counters, each with a count rate of upto 2 MHz. The counter can count either in binary or BCD. Each counter has two input signals CLOCK and GATE, and one output signal OUT. At the CLOCK input pin is connected a clocking signal of suitable frequency. Depending upon the mode of operation of the timer/counter, logic high voltage or low to high voltage transition at gate initiates or enables counting process. Each counter can be programmed in any one of 6 possible modes of operation. These modes are : Mode 0 - Interrupt on terminal count, Mode 1 - programmable one shot, Mode 2 - Rate generator or divide by N counter, Mode 3 - Square wave generator, Mode 4 - Software triggered strobe, Mode 5 - Hardware triggered strobe.

The control word format of 8253 is as shown in Fig. 3.2.

The 8259 is a programmable interrupt contoller (PIC) designed to work with 8085/8086. The 8259 can manage eight interrupts according to instructions written in the control word register. It can also mask/unmask each interrupt request individually. To implement interrupts, the Interrupt Enable flip-flop in the microprocessor should be enabled by writing the EI instruction, and the 8259 should be initialised by writing control words in the control register. The 8259 requires two types of control words: Initialization command words (ICWS) and operational command words (OCWS). The ICWS are used to setup the proper conditions and specify RST vector addresses. The OCWS are used to perform functions such as masking interrupts.

3.3 MAIN PROGRAMME

The flow chart of the main programme is shown in Fig. 3.3 Usually the program is started with the initialization of I/O ports,


MAIN START
NITIALISE 1. STACK POINTER, 2. I/Os of 8255-1, 8255-II and 8255-III (extra I/O Timer Card)
3. All firing bits low, 4. 8253 Timer gates low,
5. Timers (13H) and 5BH(for extra timer card) i.e. TM1 in Mode 3 and TM2 in Mode 0,
TM2 - Mode 3 (timer card), TM1 in Mode 0.
6. Variables : f, m pointer, Δf, FS index, FM index, CMG, Cycle, Cycle limit, Δcycle limit, Mode index.
7. Interrupts (PIC)
- unmask IR0, IR1, IR2 - store the mask word
ENABLE INTERRUPT
HALT - 1
IS CYCLE < CYCLE LIMIT ?
YES
NO
SET CYCLE = 00 ; MODE INDEX = 1,
SPEED LIMIT = CRAWLING SPEED
LX
- READ REFERENCE SPEED VIA ADC,
- RESET EQUAL INDEX = 00 (i.e. f ≠ fref)
LY

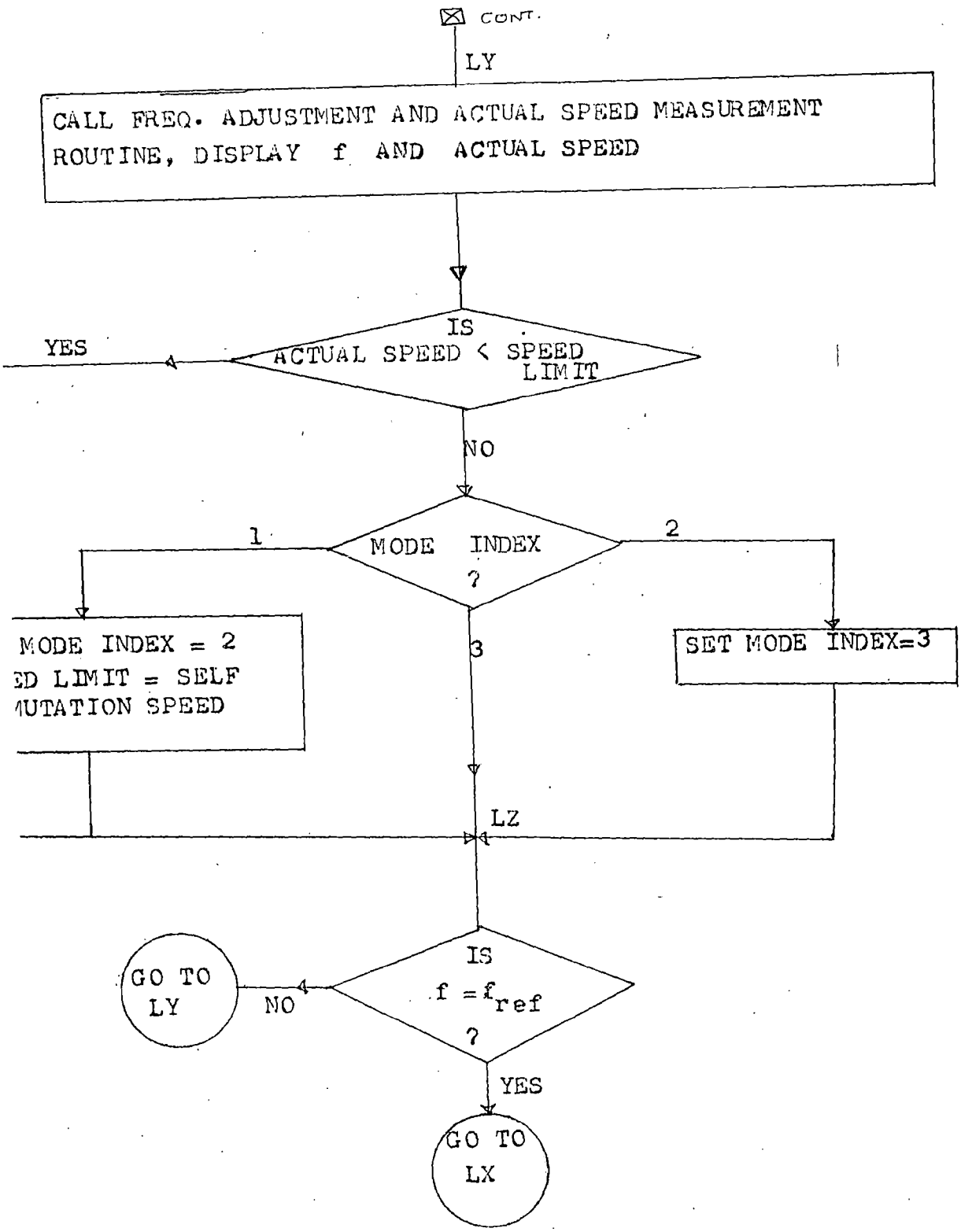


Fig. 3(3) : Flow Chart of Main Programme

which can be programmed as input parts or output parts according to the requirements.

In the VMC 85/9 Vinytic Kit 3 timers and 6 I/O ports are available to the user at space J_1, J_2 and J_3 respectively. In the present work 4 timers are used, they are TM_1, TM_2 of μp trainer kit and TM_1 and TM_2 of extra I/O timer card interconnected via the STD Bus of the kit. The TM_1 and TM_2 of extra I/O timer card are used in control scheme of rectifier and TM_1 and TM_2 of μp kit for inverter operation. The 8255s are initialised as follows:

8255-1 (CWR=03H)

i.e PORT A	PORT B	C_U	C_L	
IN	OUT	IN	OUT	1001 1000=98H

8255-2 (CWR=0BH)

PORT A	PORT B	C_U	C_L
IN	OUT	x	OUT = 1001 0000 = 90H

8255-3 (CWR=87H in extra I/O timer card)

PORT A	PORT B	C_U	C_L
x	x	x	OUT = 1000 0000 = 80H

The Fig. 2.11 given earlier show the configuration of system hardware. In 8255-I, port A is for inputting the ADC data, port B is used for firing the CS converter (rectifier) thyristors and port C is for generating handshaking signals. In 8255-II, port A is for inputting quantizers, port B for firing CM converter (inverter) thyristors and port C for timer gate. The other 8255-III is used for giving gate signal for timer as shown in the diagram.

The timers are initialised as follows:

TM_1(11H) (μp trainer) in Mode 3, because this timer acts as a frequency divider. This can be moded as

TM_1	R/L	Mode 3	Code	
0 1	1 1	0 1 1	0	= 76H

TM_2 (12H) (μp trainer) is in Mode 0 to generate an interrupt on terminal count. This can be moded as

TM_2	P/L	Mode 0	Code	
1 0	1 1	0 0 0	0	= BØH

This timer is used to load 60° to trigger CM group SCRs.

TM_1 (extra timer card) (59H) can be initialised in Mode 0 as follows :

TM_1	R/L	Mode 0	Code	
0 1	1 1	0 0 0	0	= 70H

This timer will create an IR_0 interrupt, which is the first interrupt in the system due to L-L-zero crossing of a.c. supply. This timer is loaded with the α count of the CS converter (rectifier).

TM_2 (extra card) (5AH) is initialised in Mode 1 (programmable one-shot) :

TM_2	R/L	Mode	Code	
1 0	1 1	0 0 1	0	= 82H.

This timer will creat IR_1 interrupt and timer is loaded by 60° to trigger CS converter group thyristors.

After initialization of all the necessary chips, all firing bits are first made low. Some of the values for which the processing is done during the program execution are also to be initialised with suitable values namely initial frequency (f_{start}), m-pointer, small incremental frequency (Δf), firing sequence index of both converter and inverter, (FS and FM index), Inverter group change index (CMG), first time start, cycle limit, Δ cycle limit, mode index, value of the firing angle 60° etc. Meaning of these terms is explained later in detailed flow charts. The PIC is next initialised for the vector address of the interrupts IR_0, IR_1 and IR_2. All interrupts are edge triggered.

After initialization process is over, interrupts are enabled and the processor comes to HALT state. Here it waits for first interrupt, IR_0 to occur. After the HALT (after returning from IR_0) it compares the real time measured in number of power frequency periods termed here as 'cycle' with a certain maximum value called 'cycle limit'. If 'cycle' is less than the 'cycle limit' program goes back to HALT state and waits. If it is greater, it will set real time 'cycle' = 0 0 and mode index = 1 (i.e. asynchronous starting). The upper limit of the speed a 'speed limit' in asynchronous mode is called crawling speed and is initialised to about 2Hz synchronous speed value. The reference speed is then read via ADC. The programme now calls the frequency adjustment and actual speed measurement sub-routine which includes displaying the actual inverter frequency under starting

(transients) conditions or reference frequency under steady state and the actual motor speed. Both actual (or reference) frequency and the actual speed are displayed in the data field and address field respectively. If the actual speed is less than the speed limit then programme will directly compare the actual frequency. if both are not equal then again it jumps to frequency adjustment and speed measurement subroutine. If the actual speed is more than the speed limit, then it will check the mode index. If mode index earlier was one, it set mode index as 2 with new speed limit set equal to self commutation speed. In mode 2, the motor is running synchronously but its speed is less than the required speed for self commutation of inverter SCRs.

If the mode is already two then it set mode index as three (LCI mode). Again actual frequency is compared with the reference frequency. Thus, whatever be the set value of frequency through the reference pot, the program keeps on increasing drive frequency till both are equal. If once both are equal then the new reference frequency, is re-read and the program adjusts the actual frequency to the new reference value.

3.4 ADC SUBROUTINE

Actual speed and reference frequency are measured and stored in memory through this subroutine. The reference frequency is set to a value from the pot and fed to ADC via the input channel I_{NO}. The actual speed signal is fed via channel I_{N1} of the ADC. The ADC converts analog voltage into a digital count. The reference

frequency measurement is done once in every looping of the main programme. The ADC clock-in is given from a 555 timer of 100 KHz frequency. ADC starts converting the analog input signal into digital value at the instant, when the start of conversion (SOC) bit of ADC goes from LOW to HIGH to LOW. ADC sends a signal to I/O port through END OF CONVERSION (EOC) bit going high, indicating that the conversion process is over. The digital value is read and stored. The channel selection is always done in the calling programme. The flow diagram is shown in Fig. 3.4

NAME OF SUBROUTINE	ADC SR
INPUTS	Input to ADC through I_{No}/I_{N1} channel
OUTPUTS	Reference frequency or actual speed in Hex in reg A.
CALLS	None
Destroys	All
Description	This subroutine measures the reference frequency via I_{No} channel and actual speed via IN_1 channel. The channel selection is done in the calling program.
NOTE	(1) ADC clock-in of 100 KHz is given from 555 timer. (2) Scale factor are: 1 Hz : 04H for reference frequency; 8 RPM=01H for actual speed.

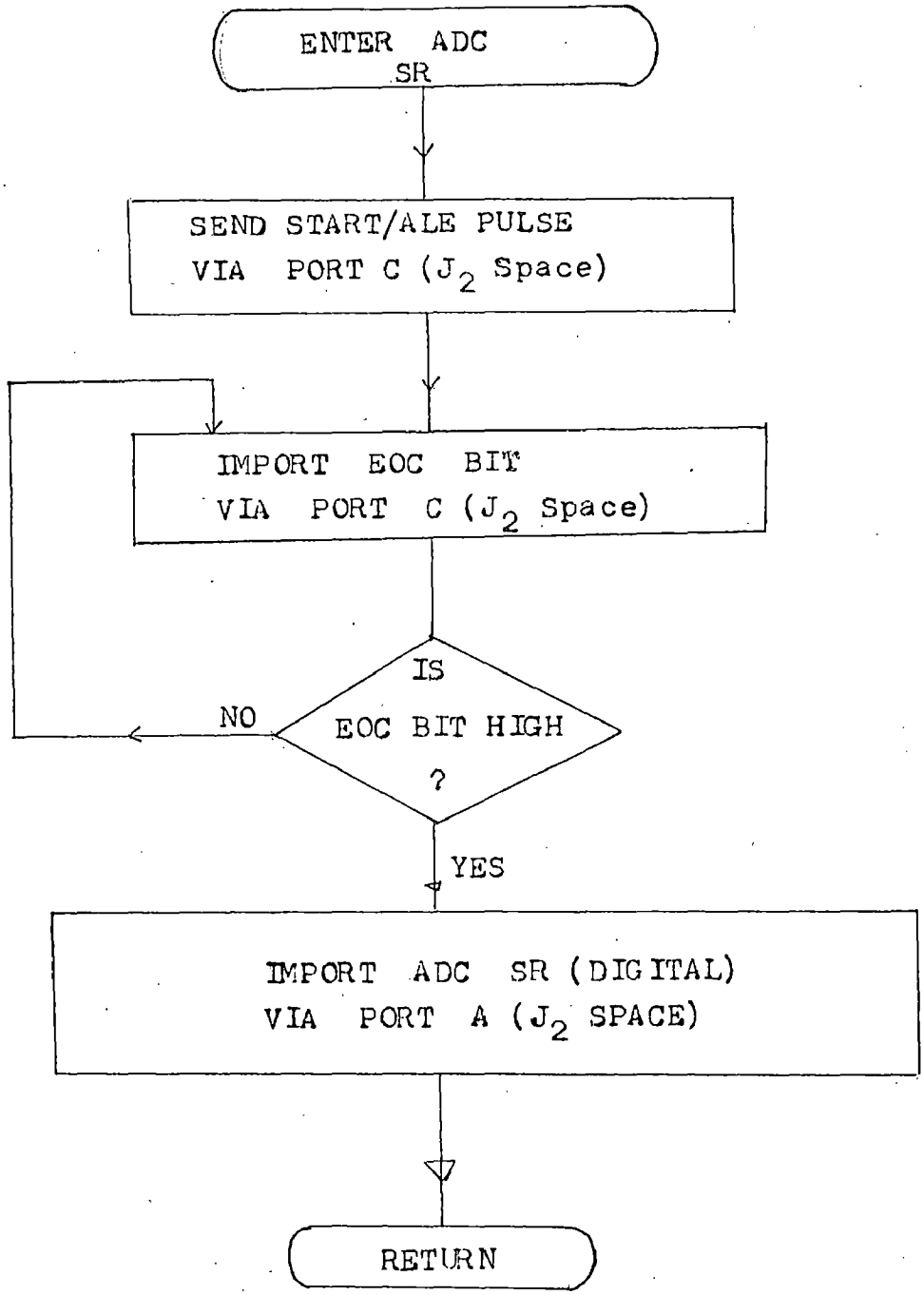


Fig. 3.4 : FLOW CHART FOR ADC SR.

3.5 FREQUENCY ADJUSTMENT AND ACTUAL SPEED MEASUREMENT SUBROUTINE

This subroutine mainly adjusts the actual inverter frequency to the reference frequency. It also measures the actual speed and display the actual speed, and actual frequency under non-LCI modes (or ref. freq. under LCI mode) in the address field and data field respectively. The flow chart is shown in the Fig. 3 [5].

The reference frequency is earlier measured before calling this subroutine; it is compared with actual frequency. If the actual frequency is less than reference frequency then the actual frequency is incremented by a small value Δf and then again compared with reference frequency to check whether actual frequency has become greater than reference frequency. If it is less, it is stored in actual frequency address. If it is greater than reference frequency, then it is limited to the reference frequency value and stored at the actual frequency address. Now the program jumps to read actual speed (by calling the ADC S.R.) and displays the actual speed.

If the actual frequency when compared to reference frequency is found more, then the actual frequency is decremented by a small incremental value Δf. Now this new actual frequency is once again compared with the reference frequency to check whether the actual frequency has gone less than reference frequency. If the actual frequency has become less than reference frequency, then the actual frequency is limited to reference frequency and stored. This logic is to prevent the oscillations in a actual frequency about the reference frequency.

After correcting the actual frequency towards the reference value, the firing angle α CS of the rectifier is determined via a

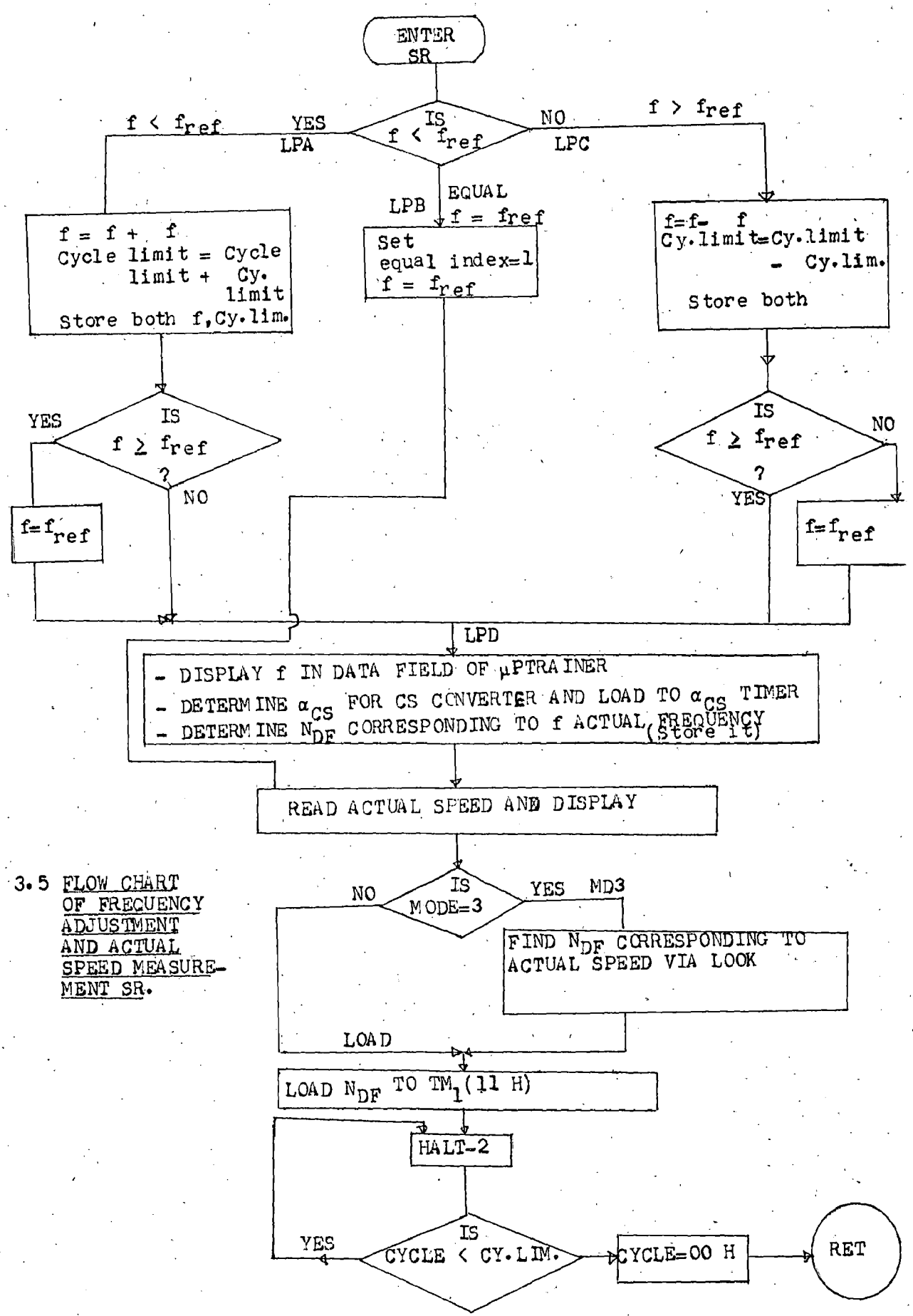


Fig. 3.5 FLOW CHART OF FREQUENCY ADJUSTMENT AND ACTUAL SPEED MEASUREMENT SR.

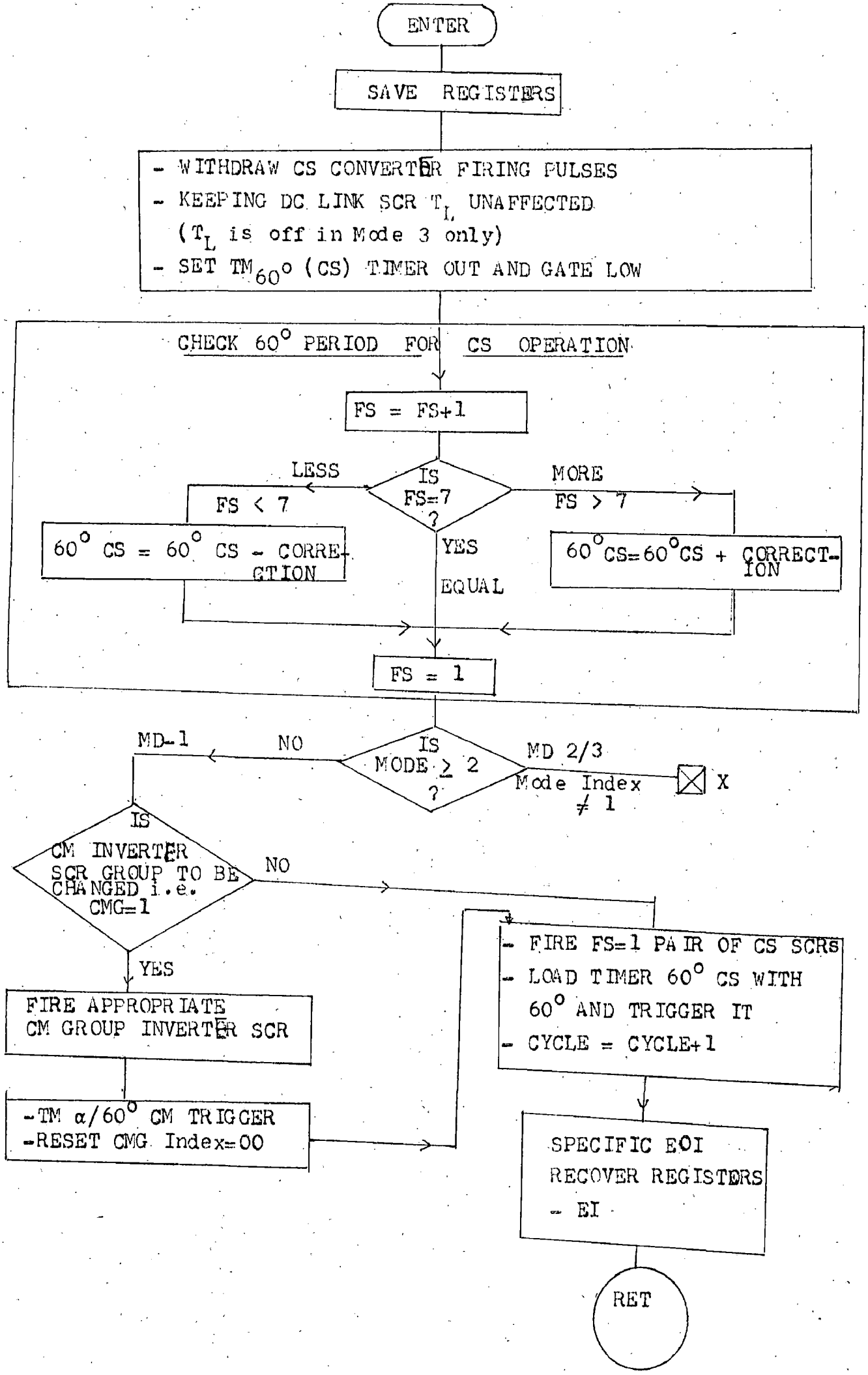
Look-up table to maintain V/f ratio constant under starting conditions. Furtner the division factor N_{DF} is also determined via Look up table; N_{DF} acts as loading to the variable frequency timer where frequency is always maintained proportional to the actual frequency of motor.

After the above frequency adjustment is over, program reads the actual speed and displays both. If drive is in mode 3 (LCI mode) then it will determine the N_{DF} factor from actual motor speed via the Look up table and load it to the timer for variable frequency generator. Program now comes to HALT state. Here it compares real time 'cycle' with cycle limit. If cycle is less than cycle limit, again it will go to HALT state or else it sets cycle = 0 0 and returns.

3.6 IR_0 (αCS) INTERRUPT ROUTINE

This is the first interrupt occuring in the control scheme. The flow chart is shown in Fig. 3.6. This interrupt subroutine starts with saving the registers. The interrupt is used to serve the first firing command to the CS converter after α angle from the zero-crossing of RY line voltage of ac power source. It withdraws first all the firing pulses and sets the GATE and 'OUT' of timer TM_1 (59 H in mode 0) low. The 60° count for rectifier (CS) operation is corrected. The firing commands are already stored in sequential memory locations and picked up properly with the help of firing index FS. Firing index points to the address of the firing command to be next executed. Once the proper firing command is picked up, the microprocessor outputs the firing command through six bits of port B (8255-1).

In this SR, FS is set = 1 (to tne SCR pair 4 & 5 of CS), the program checks up the mode index. If mode index is one, it will


ENTER
SAVE REGISTERS
- WITHDRAW CS CONVERTER FIRING PULSES
- KEEPING DC LINK SCR T_L UNAFFECTED
(T_L is off in Mode 3 only)
- SET TM_{60^o} (CS) TIMER OUT AND GATE LOW
CHECK 60° PERIOD FOR CS OPERATION
FS = FS+1
IS FS=7 ?
LESS
FS < 7
60° CS = 60° CS - CORRECTION
YES
EQUAL
MORE
FS > 7
60°CS=60°CS + CORRECTION
FS = 1
IS MODE ≥ 2 ?
NO
MD=1
MD 2/3
Mode Index ≠ 1
X
IS CM INVERTER SCR GROUP TO BE CHANGED i.e. CMG=1
NO
YES
FIRE APPROPRIATE CM GROUP INVERTER SCR
-TM α/60° CM TRIGGER
-RESET CMG Index=00
- FIRE FS=1 PAIR OF CS SCRs
- LOAD TIMER 60° CS WITH 60° AND TRIGGER IT
- CYCLE = CYCLE+1
SPECIFIC EOI
RECOVER REGISTERS
- EI
RET

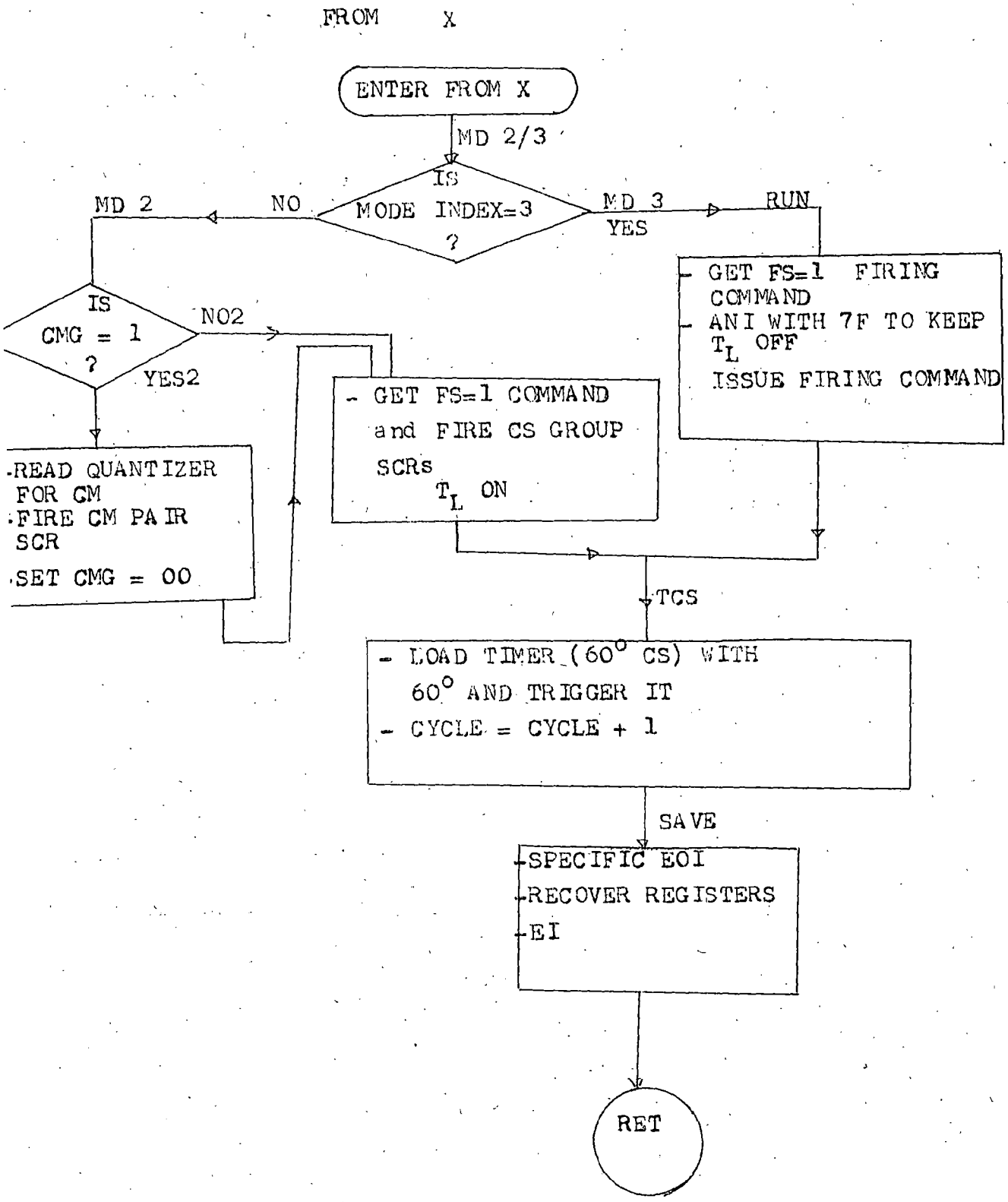


Fig. 3.6 : FLOW CHART OF IR_0 SR

set the inverter group change index = 1 and fire the appropriate CM group SCRs. The timer TM_2 (12H) is loaded with 60° (CM) value and triggered. The program jump to issue a firing command to CS converter (rectifier) and loads the timer TM_1 (59H) with 60° and triggers it. Afterwards 'cycle' (i.e. the real time index)is incremented and stored. The end of the interrupt command is issued and the program returns after recovering the registers.

If Mode index is either 2 or 3 then it checks the mode index whether it is three or not. If it is three, then it issues the firing command (FS = 1) to CS group thyristors. In mode 2, it asks if the CMG index is one (i.e., if new pair of CM group thyristers are to be fired) . If CMG index = 1, the three quantizers from synchronous machine terminal voltages are read and appropriate CM Group SCRs are fired. The CMG index is now set as CMG = 0 0. Then program jumps to issue the firing command for CS group. If the CMG index earlier was zero, CM group thyristor pair firing is not changed. Now 60° is loaded to the timer TM_2 (5AH) program returns after ,incrementing the 'cycle', recovering the registers and issuing the end of interrupt command.

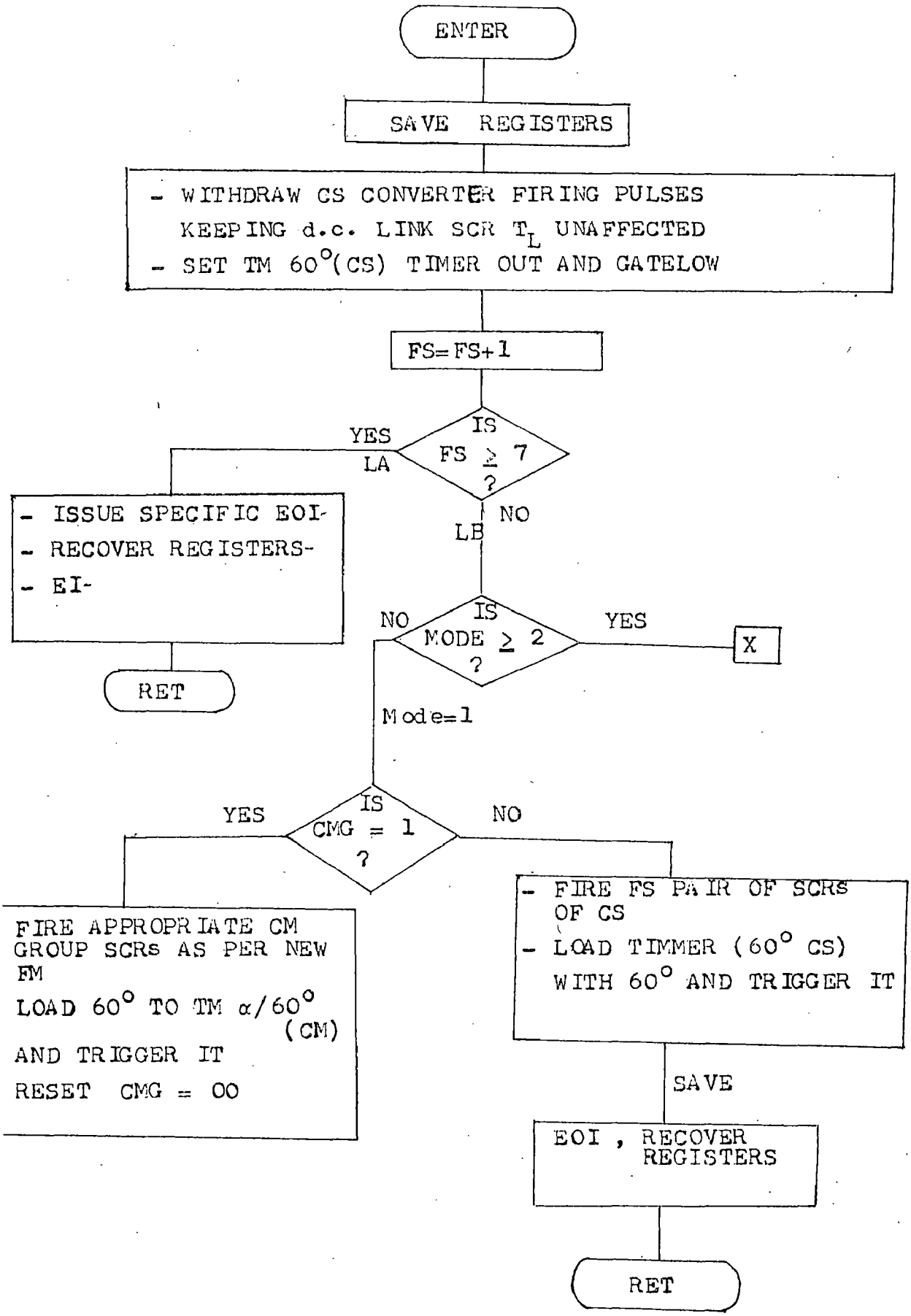
NAME OF SR	IR_0 ISS
INPUTS	power frequency zero crossing signals from R to Y line voltage is inputted through gate of TM_2 (5 AH) and quantizer signals are also inputted to port A of 8255-2 , for reading the quantizer value.
OUTPUTS	The 60° CS timer is loaded and triggered to generate the interrupt signal IR_1 at

every 60° for CS operation. FS=1 firing command for CS converter is issued. If required, CM inverter new SCR pair is also triggered and action is taken to set next 60° (CM) instants.

CALLS	None
Destroys	PSW, B, C, H, L
Description	This subroutine issues the firing command to SCR pair 4 and 5 of CS converter after α° from the zero crossing of R-Y voltage of 50 Hz power supply. It loads the timer TM_1 (59H) with 60° for next firing instants. If required, it also fires appropriate SCR pair of CM inverter and loads TM_2 (timer) (α/60° CM timer) to identify next instants for firing CM group SCRs.

3.7 IR_1 (60° CS) INTERRUPT SUBROUTINE

The flow chart of this interrupt subroutine is shown in Fig. 3.7. This interrupt SR is used to fire a new pair thyristors of CS converter at every 60° after the IR_0 interrupts. The program is entered by saving the registers. It first withdraws all the firing pulses to thyristors of CS converter (rectifier). Here the firing commands are always stored in sequential memory locations. After incrementing the old firing index FS, check is first made if it is an invalid command (FS > 7). In case of valid FS commands (FS < 7)


ENTER
SAVE REGISTERS
- WITHDRAW CS CONVERTER FIRING PULSES KEEPING d.c. LINK SCR T_L UNAFFECTED
- SET TM 60°(CS) TIMER OUT AND GATELOW
FS=FS+1
IS FS ≥ 7 ?
YES
LA
NO
LB
- ISSUE SPECIFIC EOI-
- RECOVER REGISTERS-
- EI-
RET
IS MODE ≥ 2 ?
NO
YES
X
Mode=1
IS CMG = 1 ?
YES
NO
FIRE APPROPRIATE CM GROUP SCRs AS PER NEW FM
LOAD 60° TO TM α/60° (CM)
AND TRIGGER IT
RESET CMG = 00
- FIRE FS PAIR OF SCRs OF CS
- LOAD TIMMER (60° CS) WITH 60° AND TRIGGER IT
SAVE
EOI , RECOVER REGISTERS
RET

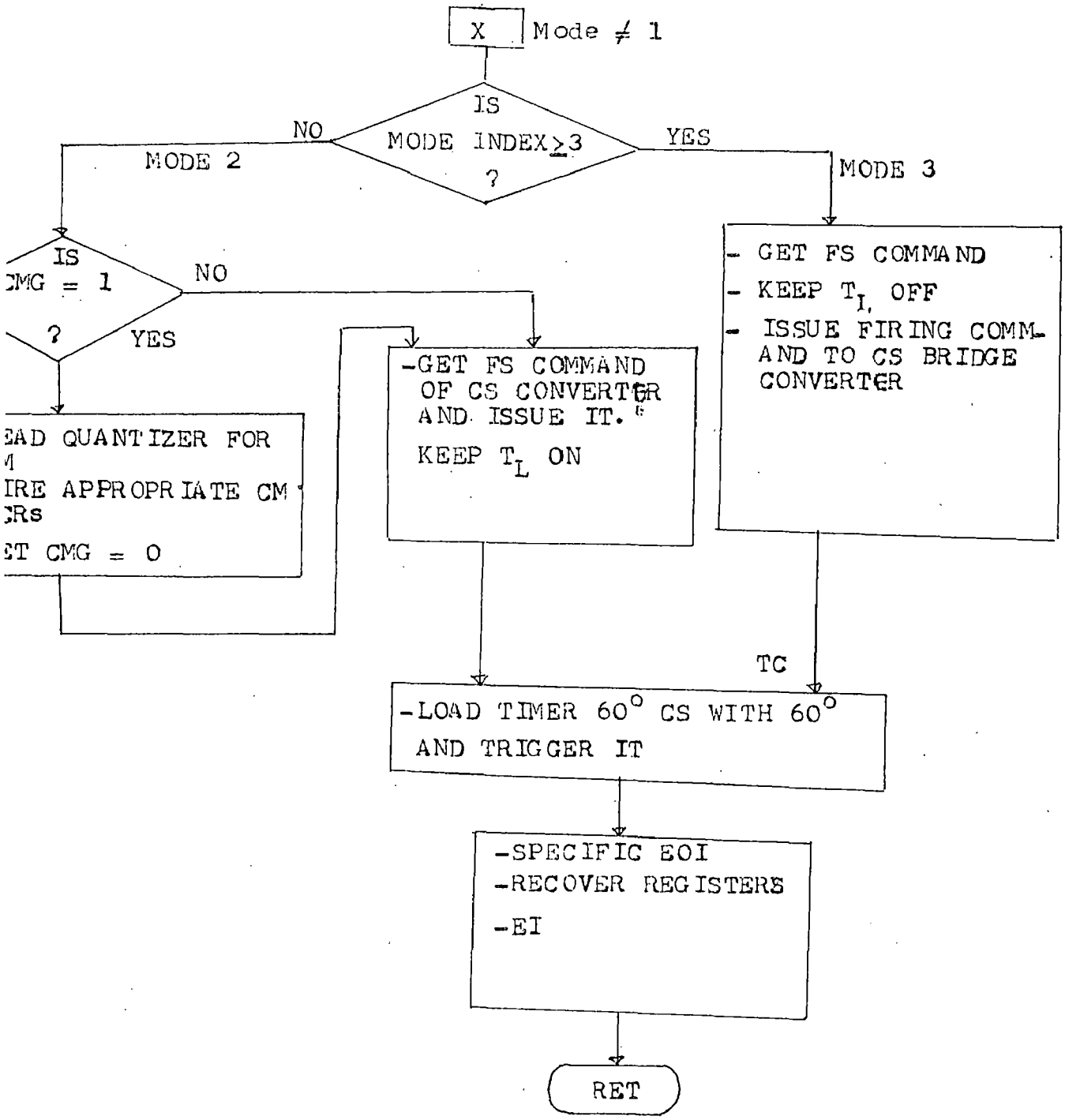


Fig. 3.7 : FLOW CHART OF IR_1 SR

the mode is next determined. If mode is 1, the CMG index is checked. If CMG is one then the appropriate CM group SCRs are fired, and the timer TM_2 (12H) is loaded with 60° (CM) and triggered. The CMG Is reset as CMG = 0 0. If CMG is not one then it will issue the command to fire CS group SCRs only. The timer TM_1 (59H) is reloaded with 60° and triggered to generate next IR_1 interrupts.

If mode index is 2 or 3 , then the program jumps ahead to determine the mode index. If mode is two, it checks if CMG = 1. If CMG = 1 it reads the quantizers and fire the appropriate CM group thyristors. The CMG is reset as CMG = 0 0 and the firing command is issued to fire the CS converter group as per FS index. The timer TM_1 (59 H) with 60° and triggered. If the mode index is already three, then it will issue the firing command to fire only CS grtoup thyristors as per FS index. After issuing the EOI instruction and recovering the registers the program returns.

NAME OF SR	IR_1(60° CS) ISS
INPUTS	3 phase zero crossing quantizers are inputted via port A (8255-2).
OUTPUTS	Firing command to valid pair of CS converter (rectifier) is issued. If required, the next SCR pair of CM inverter are also fired. The 60° CS timer is reloaded to given the next IR_1 interrupt.
CALLS	None

DESTROYS	PSW, H, L, B, C
Description	This interrupt regenerate IR_1 interrupt signal and issues a firing command to fire CS group rectifier . If required, CM group thyristor pair is also fired.

3.8 IR_2 INTERRUPT SUBROUTINE

This interrupt is used to issue the firing command for CM converter (Inverter). The flow diagram of the SR is shown in Fig. 3.8. The interrupt is generated at every 60° of actual operating frequency via the TM_2 (12 H) out in modes 1 and 2, and at commutation margin angle γ in mode 3 (LCI mode). The program is entered through saving the registers. It withdraws the firing pulses of the inverter i.e. all firing bits of CM are set low. It next loads the timer TM_2 (12H) by its mode and sets CMG=1 (i.e. group change for CM is required). The program jumps to check the mode index. If mode is one (motor speed below crawling value), it will determine the next (new) command for CM inverter and the program then returns. If mode is 2, (speed not sufficient for LCI operation), then it unmasks the IR_3 interrupt and jumps to determine next command for CM. If mode index is three, it will read the quantizers of the synchronous machine, and fire the CM group SCRs. Note the CM group SCRs are fired in the subroutine only if mode = 3 (LCI mode); otherwise the firing of CM group SCRs is done in the IR_0 and IR_1 ISS (i.e. when the new pair of CS group SCRs are to be fired, the d.c. link current being in discontinuous mode). The program returns after recovering registers and issue the EOI.

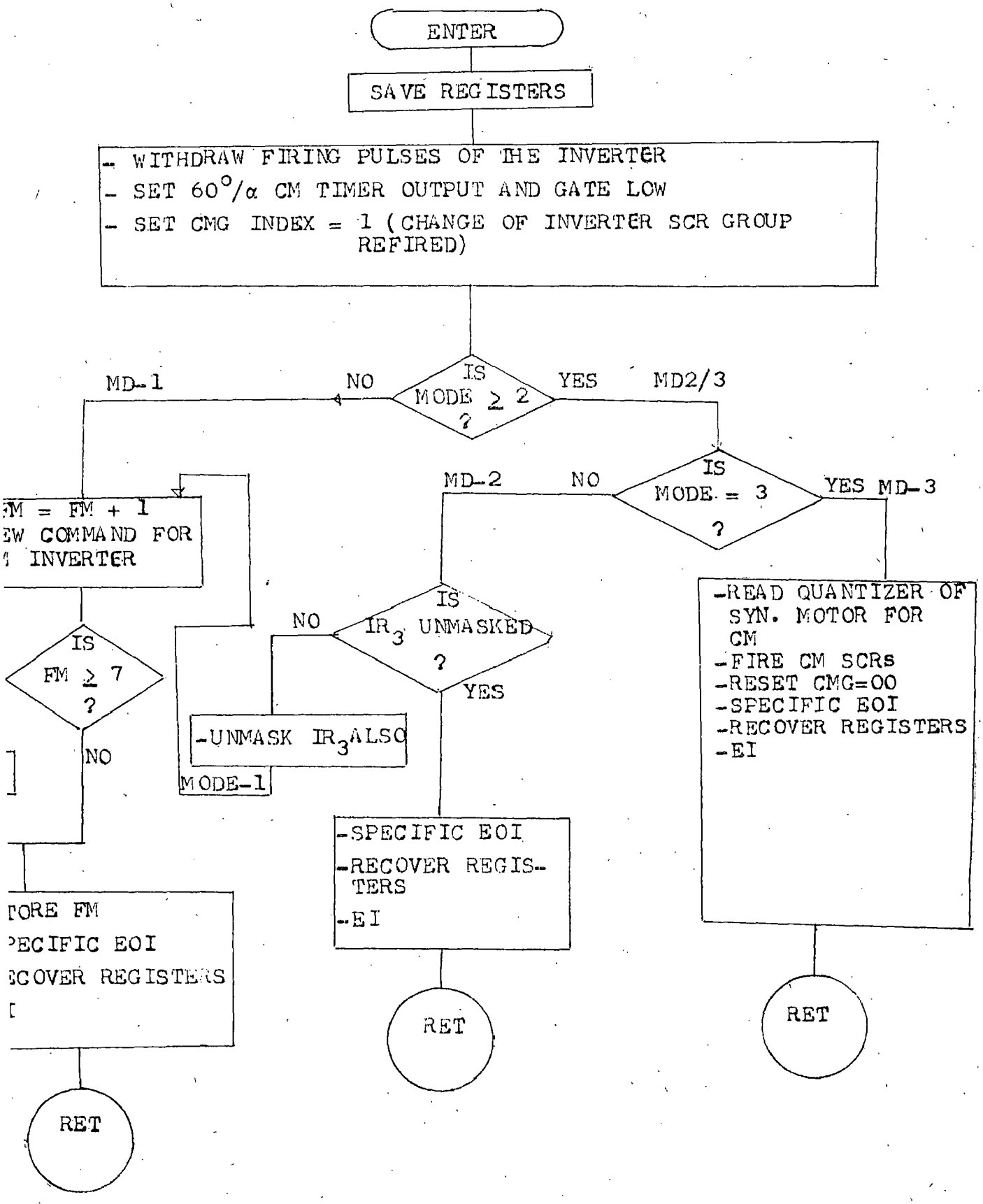


Fig. 3.8 : FLOW CHART OF IR_2 INTERRUPT SUBROUTINE

NAME OF SR	IR_2 ISS
Inputs	3 phase zero crossing quantizers are inputted through port A (8255-2).
Outputs	Issues the firing command to the CM converter (Inverter) in LCI mode; unmask IR_3 interrupt; sets up the CMG index as 1 (CM SCR pair to be fired in IR_0/IR_1) in other modes of drives.
CALLS	None
Destroys	PSW, B, C, H, L

NOTE: The CM group SCRs are fired in this subroutine only if mode = 3 (LCI), otherwise the firing of CM group SCRs is done in the IR_0 or IR_1 ISS depending upon whether IR_0 or IR_1 comes next to this particular IR_3 interrupt.

3.9 IR_3 (3 PHASE SYNCHRONOUS MACHINE ZERO CROSSING) ISS (BASE INTERRUPTS)

This subroutine is needed to generate subsequent interrupts IR_2 to fire, in LCI mode, a pair of thyristors of CM inverter. The flow chart is shown in the Fig. 3.9. The subroutine is entered with saving of registers. Base interrupt signal obtained from the frequency doubler circuit has a frequency of 6 times that of the motor actual frequency. This interrupt signal appears at each of phase angles, 0°, 60°, 120°, 180°, 240° and 300° of tne synchronous motor a.c. voltage period.

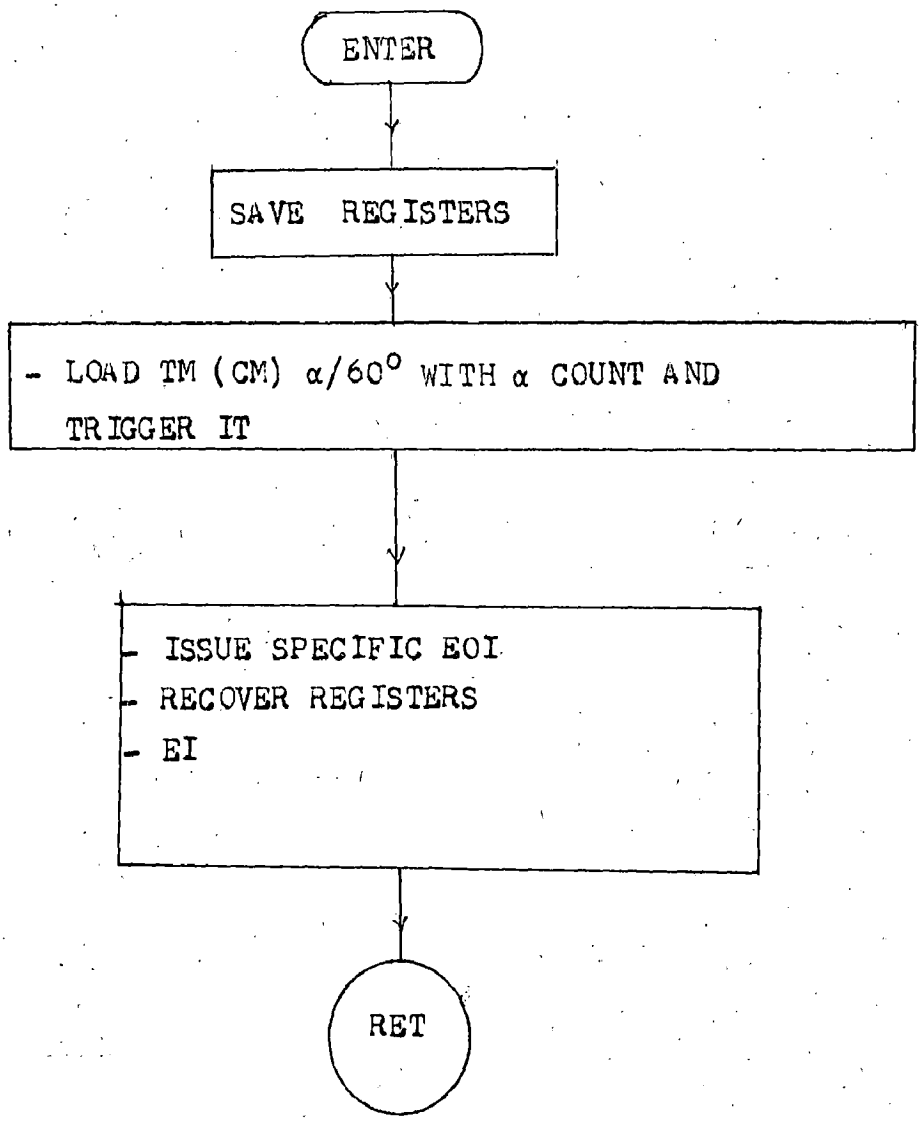


Fig. 3.9 : FLOW DIAGRAM OF IR_3 INTERRUPT SUB ROUTINE

The timer TM_2 (12H) is loaded with a count to identify the margin angle 'γ' instants for firing CM. It starts down counting, when it is triggered. When the down counting is over, it releases the timer interrupt IR_2. The registers are recovered with the previous data and end of interrupt command is issued. The interrupt is enabled, before it returns to the main program.

NAME OF SR	IR_3 ISS
Inputs	None
Outputs	None
CALLS	None
Destroys	PSW, H, L
Description	This interrupt is generated at every 60° period of motor a.c. cycle when drive is in mode 2 (starting) or mode 3 (LCI mode). It loads CM α/60 timer with appropriate count to generate subsequently an IR_2 interrupt to identify CM group firing instants in LCI mode.

3.10 'LOOK' SUBROUTINE

With the software implementation, a new value of d.c. link voltage (V_{dc}) correponding firng angle α (αCS) is determined for a command , from look subroutine.

The initialization of old value of V_d, its corresponding firing angle and m pointer from look up table, is done at the starting

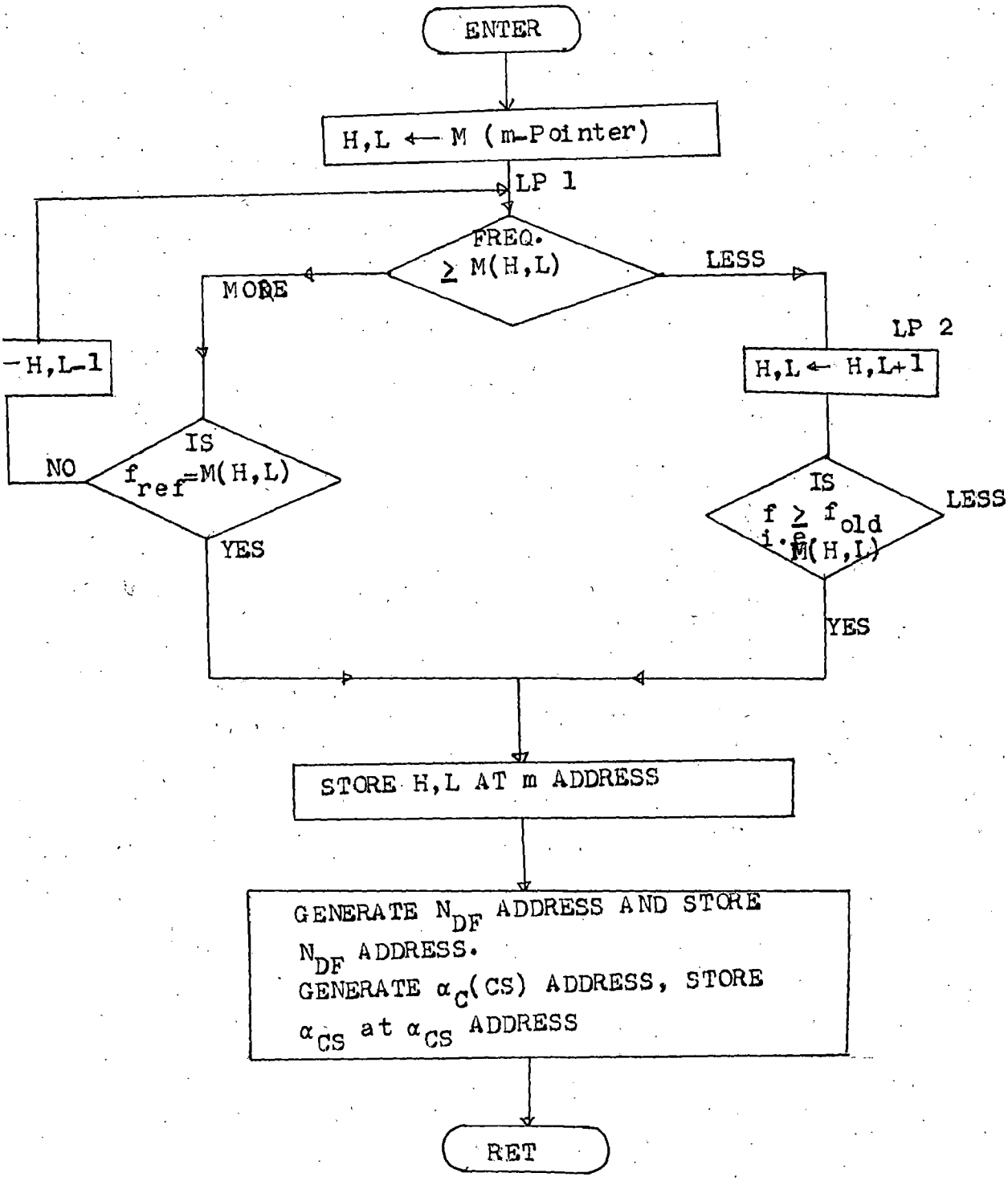


Fig. 3.10 : FLOW DIAGRAM OF "LOOK UP" SUB ROUTINE

of the main programme. The value of m pointer corresponding to the new frequency gets adjusted from the old m pointer, through the look subroutine. At the end of this subroutine, the m pointer of new frequency is stored at a certain address location and the two byte firing angle ' α ' corresponding to frequency command is also stored at α_n low address location, and at α_n high add. location. The flow chart is given in Fig. 3.10.

Look Up Table

While microprocessors potentially offer more flexibility and economy than the analog circuits, their relatively limited real time capabilities restrict their functions, to table lookups and simple arithmetic operations. The determination of the necessary control requires only table lookup operations and computations are kept to a minimum. The control algorithm using the table lookup, becomes simple, meets the real time requirement, and its implementation is well with in the capability of the present day microprocessors.

3.11 DETERMINATION OF LOOK UP VALUES

For a 3 phase fully controlled converter (CS)

$$V_{dc} = V_{max} \cos[\alpha^\circ (CS)]$$

$$V_{dc}/V_{max} = \cos [\alpha^\circ CS]$$

(V_{dc}/V_{max}) is varies from 0 to 1 in normalised from and 01 Hex to FF Hex in digitised value.

The reference frequency scale is

1 Hz = 04 Hex

(5 V d.c. ref = 64 Hz)

The $\alpha°$(CS), for any V_{dc}, is worked out and corresponding time in milli second is calculated for 50 Hz nominal power frequency. The α count for $\alpha°$ is determined on the basis of 1.5 MHz 'CLK IN' to the timers measuring $\alpha°$ or 60°. Hence, at 50 Hz

$$\alpha°(\text{at 50 Hz}) = \frac{\alpha}{360} \times \frac{20}{1000} \text{ sec}$$

$$= \frac{\alpha}{360} \times \frac{20}{1000} \times 1.5 \times 10^6 \text{ counts}$$

$$= \frac{250}{3} \alpha \text{ counts}$$

In case of Inverter, the angles are to be determined at variable frequency, since the synchronous motor runs at different speeds. If the angle is counted by a timer with constant CLK-IN frequency, the count, corresponding to angle, will have to be continuously changed as drive frequency changes. This is most inconvenient. To solve this problem, a variable frequency timer [TM_1 (11H)] is used to generate a frequency at its 'OUT' terminal which is directly proportional to the machine actual speed (or frequency). This arrangement is shown in Fig. 3.11.

The TM_1 works in mode 3 (divide by N, N = division factor N_{DF}), while TM_2 is in mode 0. The variable frequency out from TM_1 is

$$f_{out} = 1.5 \times 10^6 / N \text{ Hz}$$

The constant proportionality between f_{out} and actual operating frequency 'f' is kept high for accurate angle measurement. It is equal to 1500.

Thus for an angle α °, the count loading of TM_2 timer will be

$$\alpha_C = \frac{\alpha}{360} \cdot \frac{1}{f} \quad \frac{1.5 \times 10^6}{N} \text{ counts}$$

$$= \frac{\alpha}{360} \times 1500 \text{ counts}$$

$$= \frac{25}{6}\alpha \text{ count}$$

with $$\frac{1.5 \times 10^6}{f\ N} = 15000$$

Here, N (i.e. division factor N_{DF}) = 1000/f

where,

f is in Hz or

N_{DF} = 4000/f counts here f is in Bits.

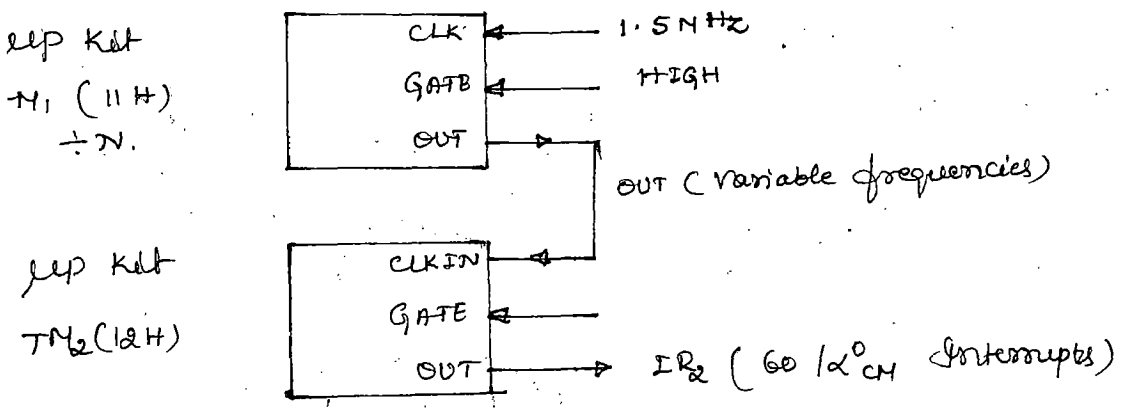


Fig 3.11

3.12 CONCLUSION

In this chapter the complete software flow routine and the various subroutines used in the main routine implementation, have been discussed in detail. The various subroutines discussed are ADC subroutine, frequency adjustment and speed measurement subroutine, IR_0 subroutine, IR_1 subroutine, IR_2 subroutine, and IR_3 subroutine.

The various subroutine software programs have been tested individually in a VMC 85/9 µp trainer.

CHAPTER - 4

SYSTEM PERFORMANCE AND EXPERIMENTAL RESULTS

4.1 GENERAL

This chapter describes the various steady state investigations carried out on the microprocessor based LCI-synchronous motor drive under variable frequency operation. Experiments are performed on the drive and the results of these tests are presented. Photographs of the various control signals and operating variables are also given in this chapter.

4.2 EXPERIMENTAL INVESTIGATIONS FOR STEADY STATE PERFORMANCE OF LCI-SYNCHRONOUS MOTOR DRIVE

The experimental investigations to obtain the steady state performance of LCI-SM system have been carried out in two parts:

(i) No load tests

(ii) Load tests

As it has been explained earlier, the speed of the commutatorless motor is given by

$$N_{sy} = K.V_{dc}/(\cos \alpha)I_f \qquad (4.1)$$

From the above equations it is clear that the motor speed is a function of three independent variables. They are :

(i) The d.c. link voltage, V_{dc}

(ii) The firing angle of the inverter,

(iii) The field current of the synchronous motor, I_f

In the experimental work carried out, one of the three control parameters is varied keeping the other two parameters constant, and the effect of this single parameter on motor speed, power factor, torque etc. is observed.

The specifications of the motors, i.e., synchronous motor and loading machine on which the experiments are carried out are given in Appendix - 'A'. The detailed layout of the experimental setup including the instrumentation is shown in Fig. 4.1.

4.3 AUTOMATIC STARTING OF THE LCI-SYNCHRONOUS MOTOR SYSTEM

The method of starting of LCI-SM drive involves the following steps:

(i) The microcomputer system is fed the value of the desired speed through the reference pot. The microcomputer is commanded to execute the software program for control of firing angles of both CS and CM converters.

(ii) The three phase a.c. supply is given as the input to the rectifier (CS) through the autotransformer. It is maintained at rated voltage. The reference speed ADC pot is kept to low speed setting. The rectifier operates in the discontinuous mode. In this mode of operation, the discontinuous d.c. link current will be fed as the input to the inverter. The motor starts crawling. Now the reference speed is slowly increased (this increases the d.c. link voltage) till motor gets to about 20% of the rated speed.

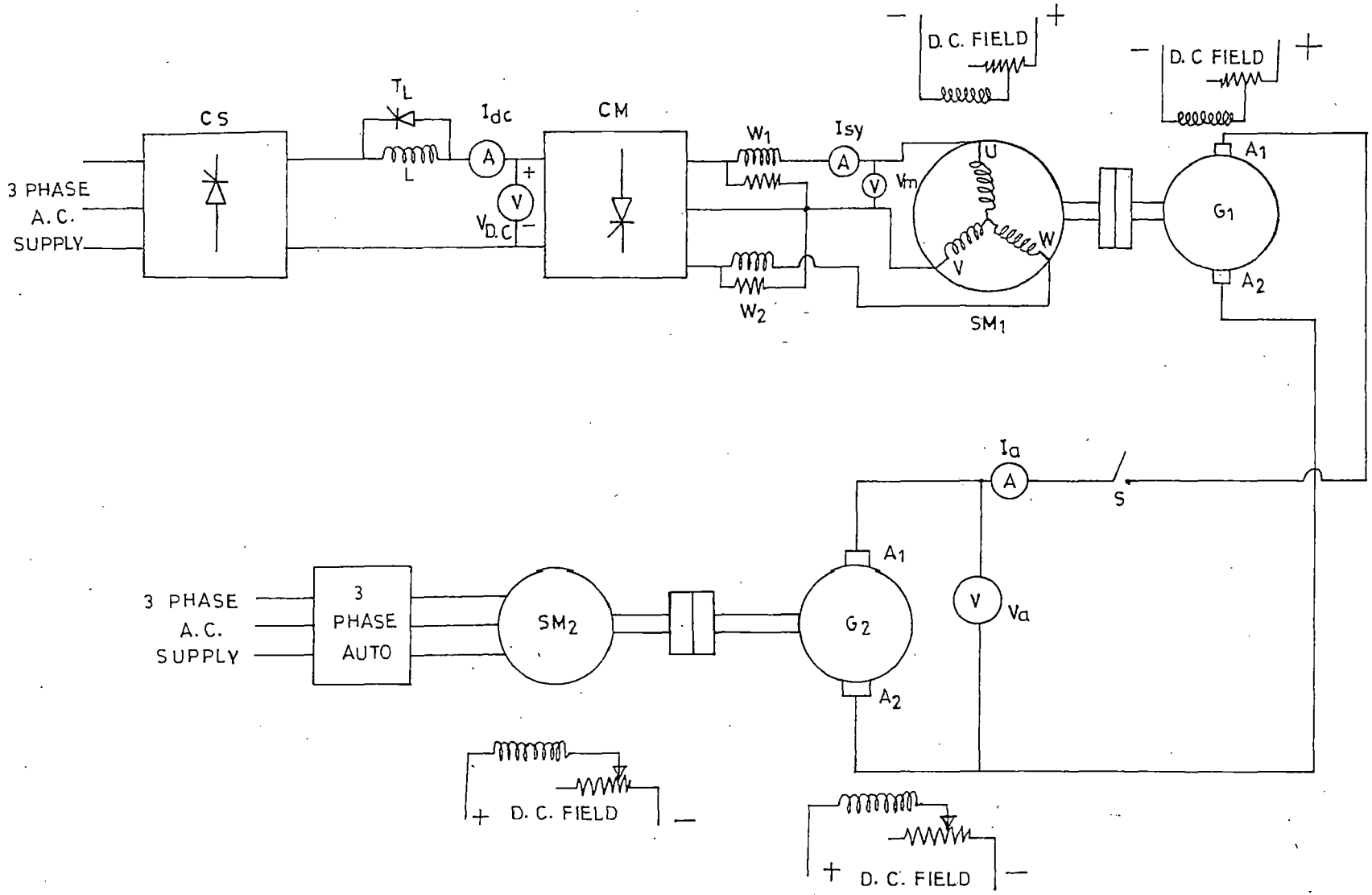


FIG. 4·1— EXPERIMENTAL SETUP OF LCI – SYNCHRONOUS MACHINE SYSTEM

(iii) After motor speed is sufficiently high (about 20% of rated speed), the synchronous motor terminal voltage is sufficient for line commutation of inverter. The program now jumps to LCI mode, the d.c. link current may become continuous now.

(iv) By adjusting the reference speed, firing angle of the rectifier gets varied from 90° to smaller values to control the speed of synchronous motor upto its rated or even higher value. In the present work the inverter has been operated at few selected settings of the commutation margin angle(γ). During the starting and run-up operation, the synchronous motor field current is adjusted to such a value that the synchronous motor develops sufficient starting torque and then runs in over-excited state drawing armature current at leading power factor.

In the present work, an attempt has been made to start the synchronous motor by above described method. The major problem is that this synchronous motor demands a starting current of nearly 10 A. The thyristors in the drive have the rating of 10 A; hence fuse (of 7 A rating) used to protect thyristors for over load current blows. However, the motor crawls and runs at only low speeds (about 100 RPM order) could be achieved. If the current rating of thyristors could be increased to at least 15 A, the smooth starting and running to higher speeds can be possible. The experiments are carried out by starting the motor in LCI mode directly with the help of a Ward-Leonard system as described below.

4.4 STARTING OF THE LCI-SYNCHRONOUS MOTOR SYSTEM

The laboratory method of starting of LCI-SM system involves the following steps:

(i) The microcomputer system is fed a low desired speed through the reference pot and commanded to execute the program.

(ii) Now start the synchronous motor (prime mover) of the Ward-Leonard system (SM_2) with the help of a 3 phase autotransformer and synchronize it by injecting d.c. field current. Initially the switch 'S' is in open position.

(iii) The generator G_2 field is un-excited before closing the switch 'S'. Now close the switch 'S' and slowly excite the generator (G_2). The voltage developed at the terminals of the generator are fed to the G_1 d.c. machine armature with proper polarity. The G_1 machine (which acts as a motor) starts to run slowly Its speed can be adjusted by adjusting the field of the G_2 machine for the desired initial speed.

(iv) Slowly increase the voltage to the input of the rectifier to its rated value. By proper changing the reference speed potentiometer, the LCI drive starts feeding power to the coupled d.c. machine. Now observe the reading of the ammeter (I_a) If ammeter reads zero, we can open the switch 'S', the synchronous motor runs in the LCI mode by receiving supply

from the inverter. The drive is now operating under no load. By slowly increasing or decreasing the reference speed pot, it is possible to get a new desired no load speed. The drive can be loaded by keeping the switch 'S' closed and reducing the field current of the d.c. machine G_2. The LCI-SM drive's power is pumped to the AC system via the Ward-Leonard drive.

4.5 RESULTS AND DISCUSSIONS

The no load characteristics of the drive are studied as follows:

(i) Keeping field current I_f and inverter firing angle α (margin angle $\delta = (180 - \alpha)$ constant, the d.c. link voltage V_{dc} is varied.

(ii) Keeping V_{dc} and α constant, the field current I_f is varied.

(iii) Keeping field current I_f constant and varying V_{dc} for different values of firing angle of inverter.

The first experimental investigation above is the armature voltage control of the speed of the CLM. The d.c. link voltage V_{dc} has been varied from 100 V to 450 V. The second study concerns the speed control under variation of the field current of the CLM. The field current has been varied from 0.1 A to 0.4 A.

4.5.1 Effect of Variation of D.C. Link Voltage on Speed

The speed versus d.c. link voltage characteristics at different field currents and firing angles (i.e. margin angle $\delta = 30°$,

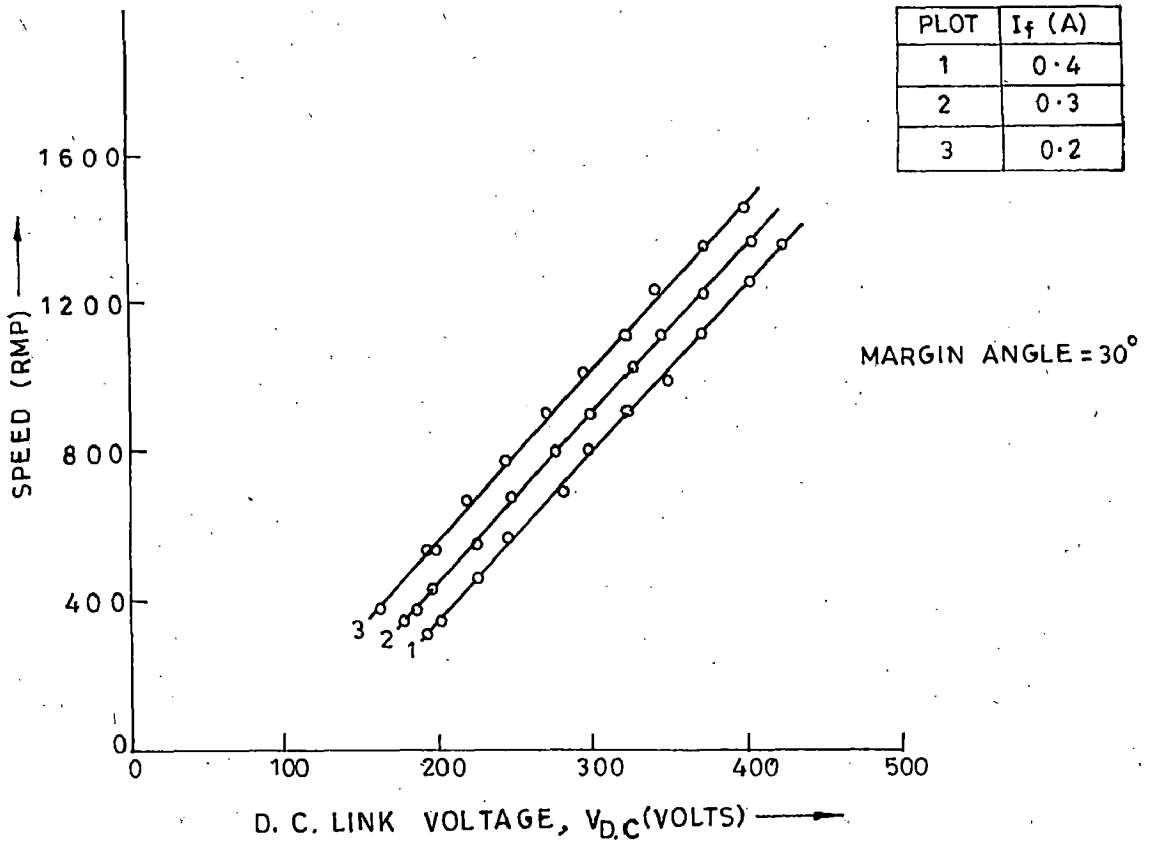


FIG. 4(a)—VARIATION OF SPEED WITH D.C. LINK VOLTAGE AT NO LOAD

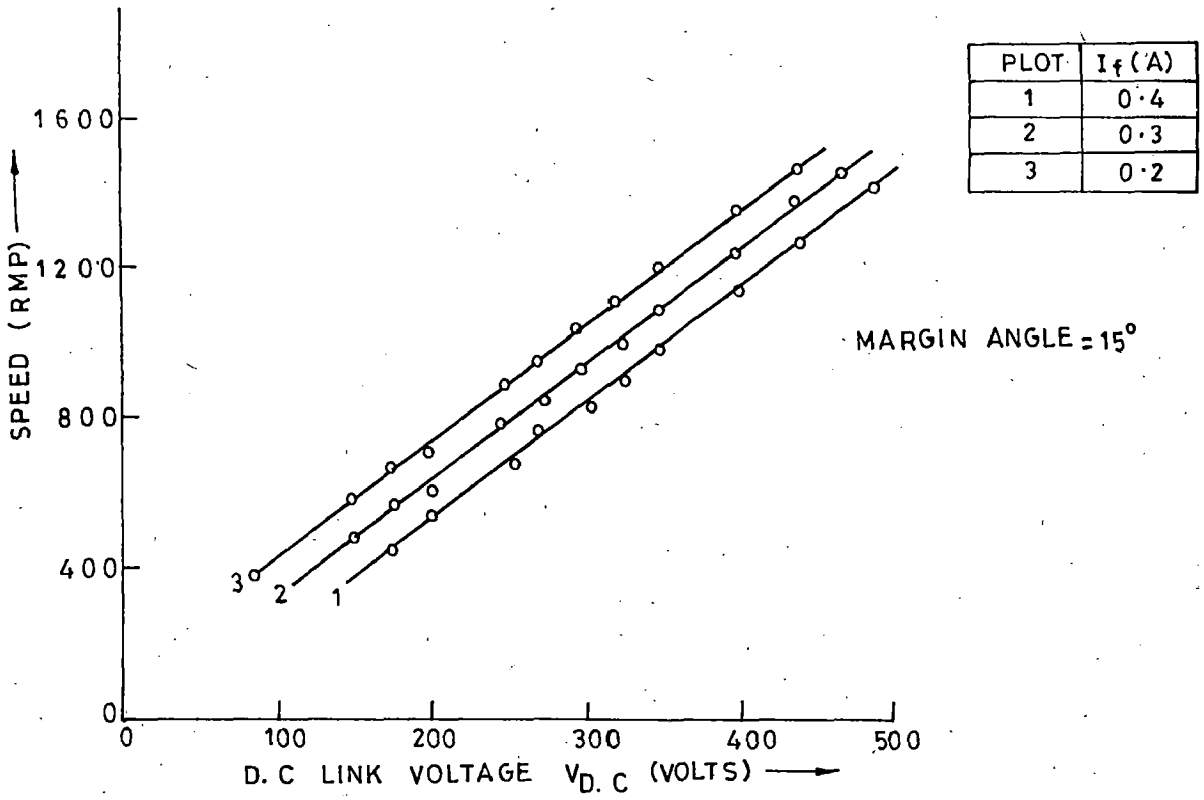


FIG. 4(b)—VARIATION OF SPEED WITH D.C LINK VOLTAGE (V_{dc}) AT NO LOAD

and 15°) are given in Figs. 4(a) and 4(b). From these figures it is clear that as the d.c. link voltage increases up to the rated value, the speed also gradually increases from about 300 RPM to 1450 RPM. The effect of field current is also shown in this figure. If the field current setting is low, the speed slightly increases. It has been observed experimentally that if the field current setting is sufficiently decreased, the motor deaccelarates and slows down, because electromagnetic torque produced by motor with weakened flux is insufficient to overcome the losses.

The curves in Figs. 4(a) and 4(b) give the change in speed of CLM with d.c. link voltage at different firing angle (i.e. γ = 30° and γ = 15°). Comparing the two characteristics, it can be concluded that comparatively higher speed and range of speed control are obtained at higher value of margin angle γ . This is because the speed is inversely proportional to $\cos\alpha$ (or $\cos\gamma$) with other parameters kept constant.

4.5.2 Effect of Variation of Field Current I_f on Speed

The speed versus field current characteristics at different d.c. link voltages and firing angles are given in Figrs. 4(c) and 4(d). From these figures it is concluded that as the field current is decreased gradually , the speed gradually increases.

The range of speed control by variation of field current is again dependent upon the d.c. link voltage V_{dc}; it increases with the increase in V_{dc} for a constant value of margin angle .

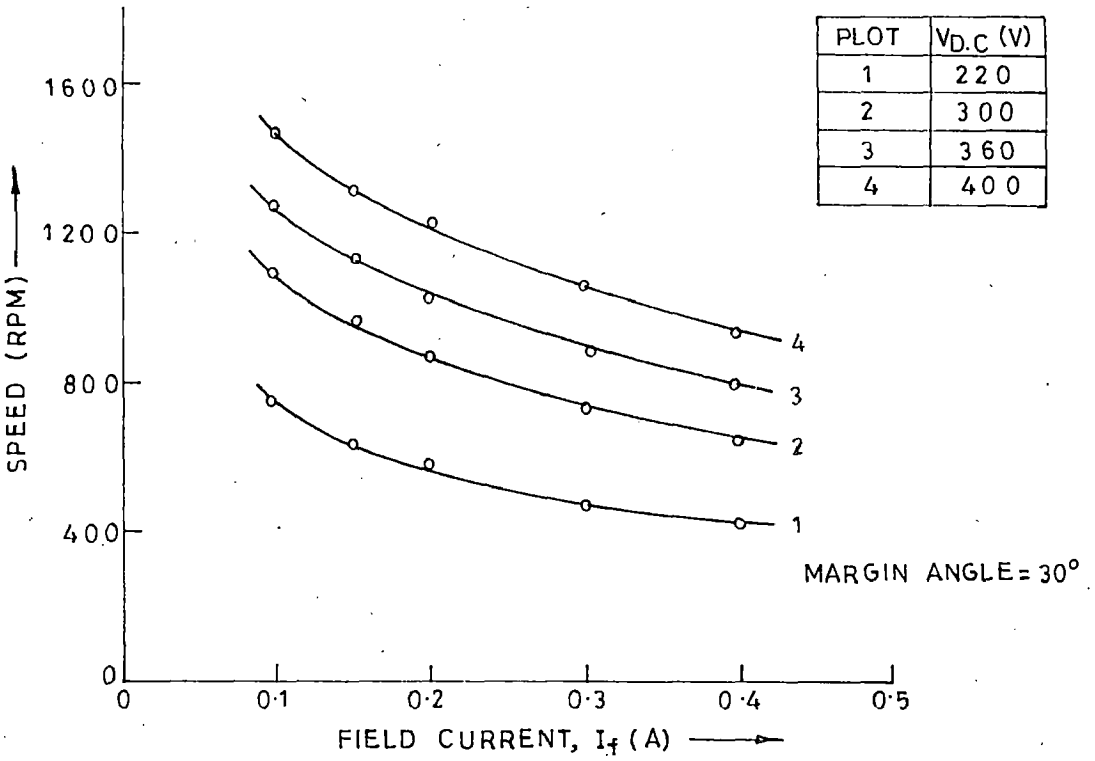


FIG. 4(c)—VARIATION OF SPEED WITH FIELD CURRENT (I_f) AT NO LOAD

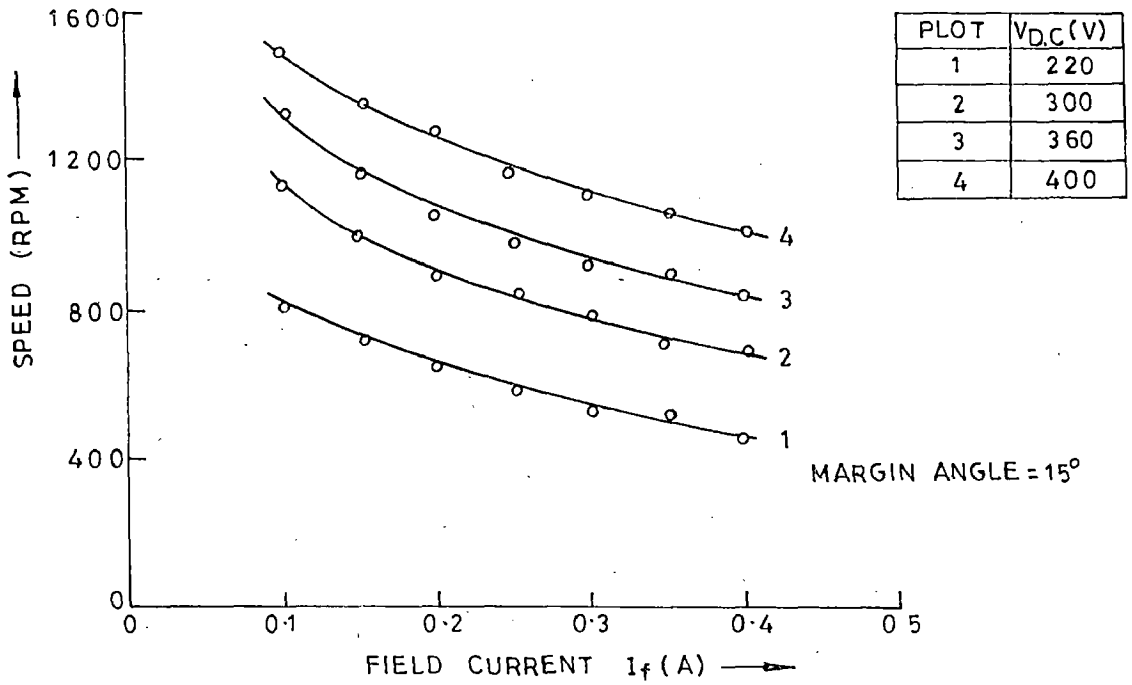


FIG. 4(d)—VARIATION OF SPEED WITH FIELD CURRENT AT NO LOAD

4.5.3 Effect of Variation of Torque on Speed

The torque versus speed characteristics are shown in Fig. 4(e). The load characteristics of the commutatorless motor is same as that of a separately excited d.c. motor. In the Fig. 4(e), it is clearly observed that for a sufficient change of load torque, the speed approximately remains constant. Thus, the characteristic is shunt in nature.

4.5.4 Effect of I_{dc} on Active and Reactive Power

The characteristics of d.c. link current versus active and reactive powers are shown in Fig. 4(f). It is noted from the figure that both the active and reactive powers increase with increase in the d.c. link current (i.e., as the drive is loaded). It is because the power factor of drive is nearly constant since the margin angle has been kept constant here.

4.5.5 Load Current Efficiency and Powerfactor Versus DC Link Current Characteristics

The characteristics of efficiency, load current, and powerfactor with respect to d.c. link current are given in Figs. 4(g) and 4(h) for different V_{dc}. It can be observed from these figures that the variation of power factor with d.c. link current is marginal. If the link current (i.e. load) is increased, the powerfactor improves very slightly. This is again due to the margin angle being kept constant.

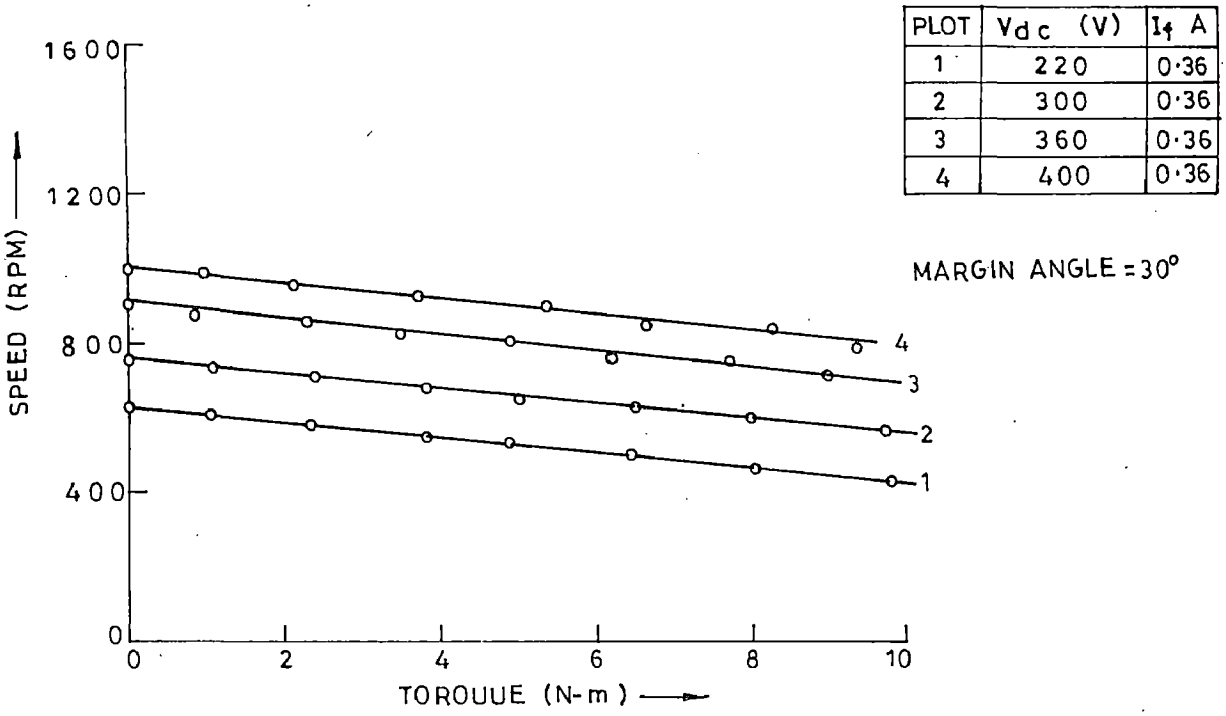


FIG 4 (e) VARIATION OF SPEED WITH TOROUUE AT LOAD TEST

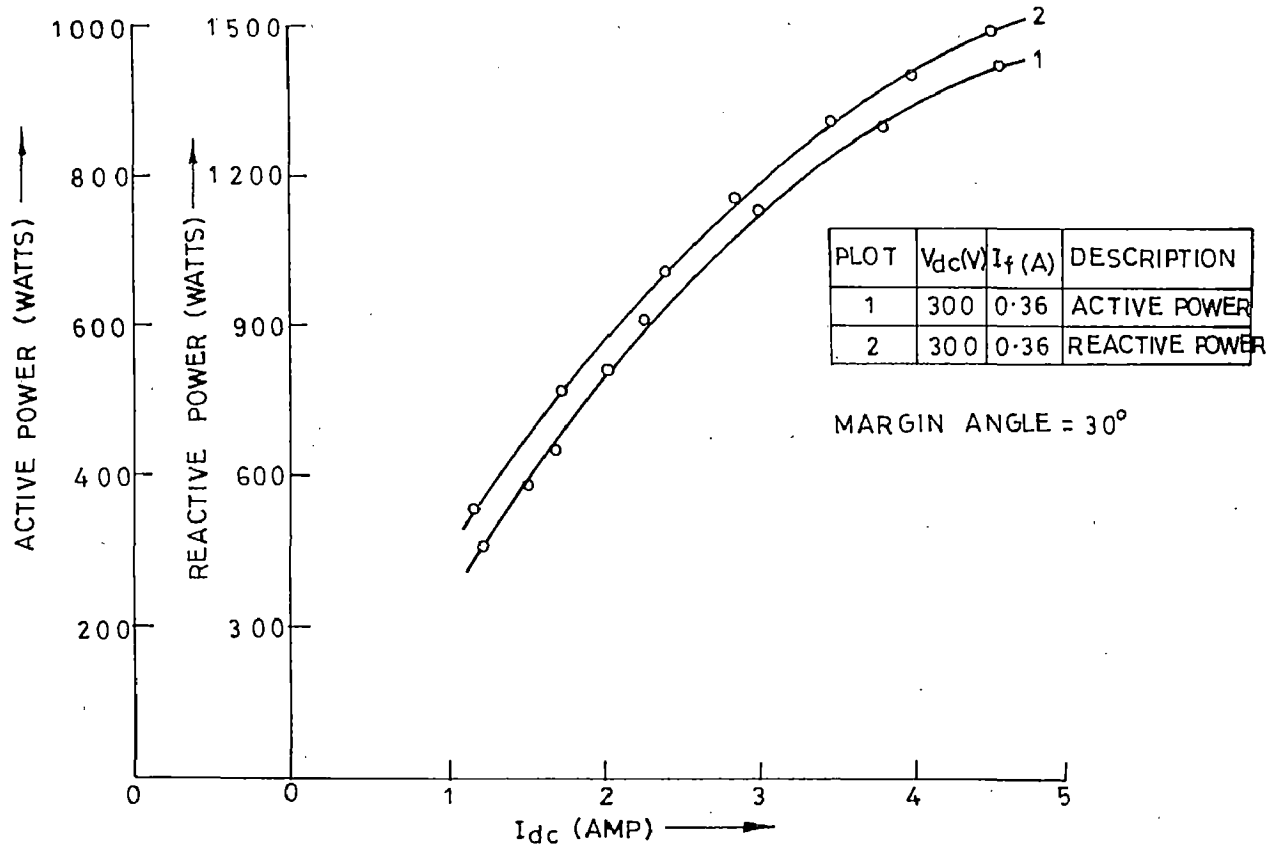


FIG. 4 (f)—VARIATION OF ACTIVE AND REACTIVE POWER WITH D. C. LINK CURRENT AT LOAD TEST

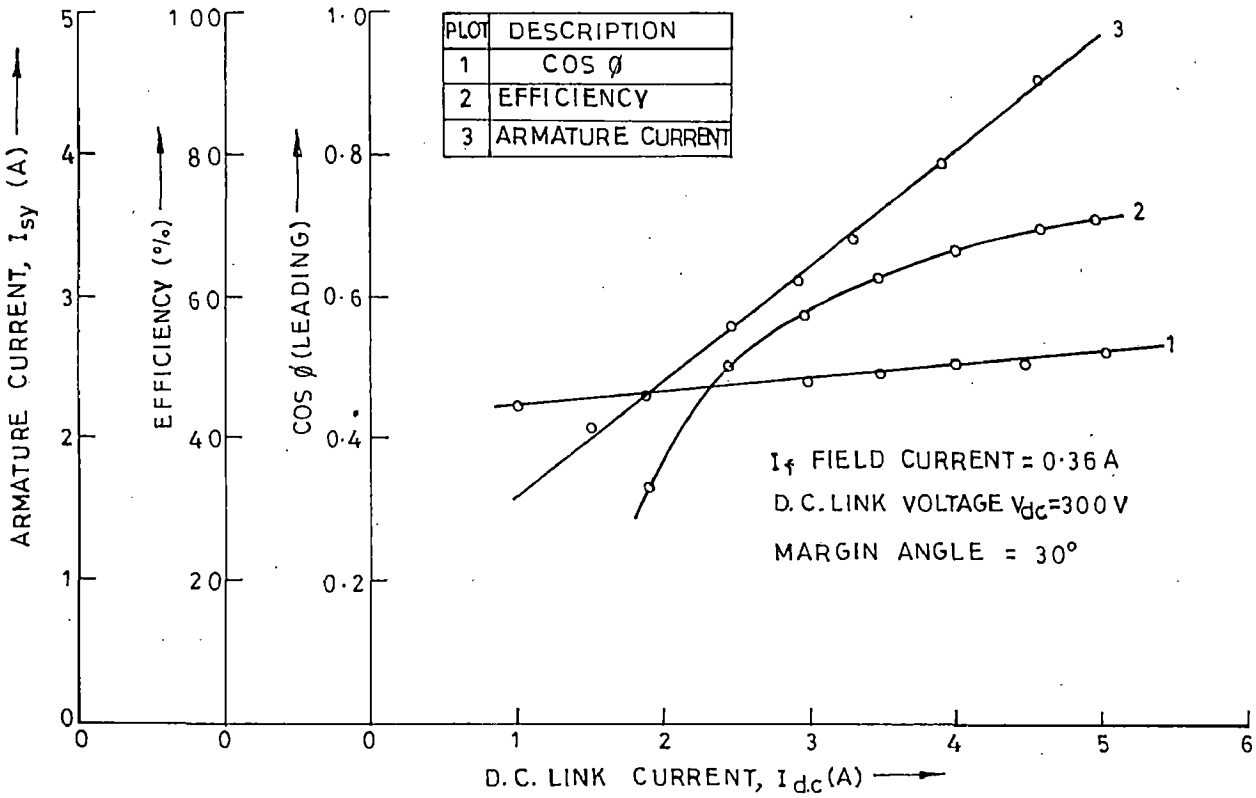


FIG. 4 (g) — VARIATION OF POWER FACTOR, EFFIENCY, ARMATURE CURRENT WITH D. C. LINK CURRENT AT LOAD

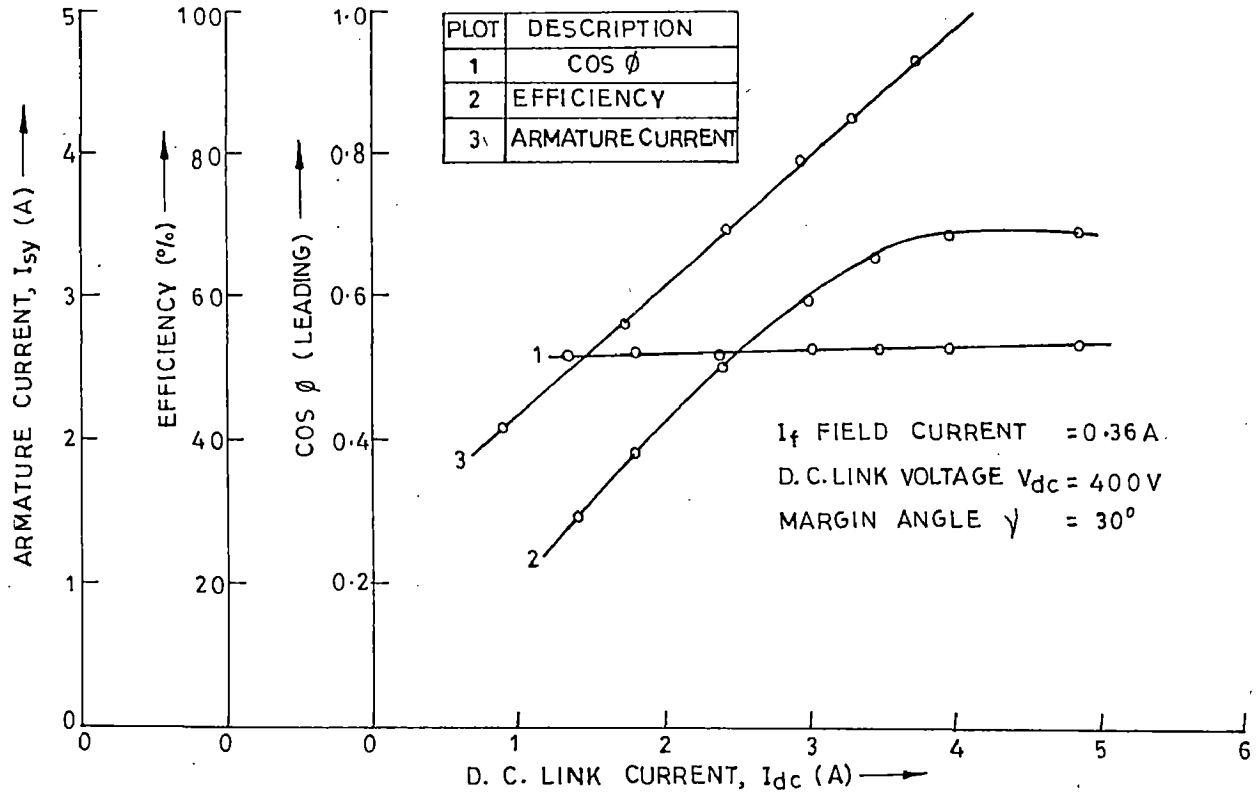


FIG. 4 (h) — VARIATION OF POWER FACTOR, EFFIENCY, ARMATURE CURRENT WITH D. C. LINK CURRENT AT LOAD

In order to calculate the gross mechanical power output of the synchronous motor, the set is earlier calibrated for its friction and windage losses, and the armature resistance of the coupled d.c. machine is also determined. The efficiency is thus calculated on the basis of the gross power output for the synchronous motor. With increase in the d.c. link current I_{dc} , efficiency is noted to increase upto certain extent (i.e. upto 70%), afterwards, it remains nearly constant. The efficiency is noted to be slightly better if drive is operated at higher value (near rated value) of d.c. link voltage, V_{dc}.

The synchronous motor armature current (I_{syn}) depends upon the d.c. link current. If the load is increased, the d.c. link current and the synchronous motor armature current increase. In the present work, the coupled d.c. machine is loaded up to 8 A through the Ward-Leonard system (because the LCI-synchronous motor rated armature current is 3.45 amp only). The variations are clearly observed from the characteristic curves.

4.6 DESCRIPTION OF PHOTOGRAPHS FOR NO LOAD AND LOAD CONDITIONS

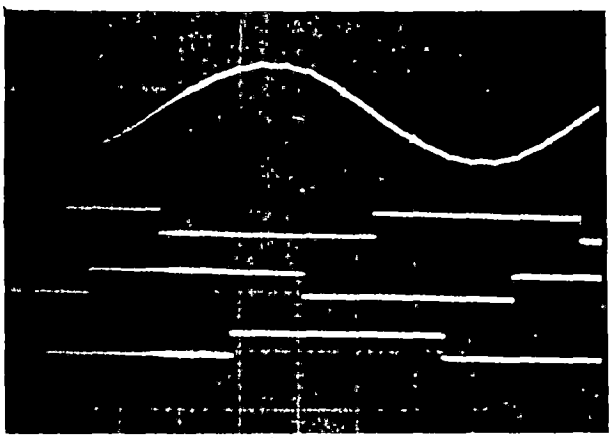
The actual waveforms of various control signals and drive's electrical variables have been shown in photographs 4(i) to 4(iv), which are similar to theoretical waveforms.

The photographs of Fig. 4(i) show the sinewave voltage 180° out of phase to the synchronous machine terminal voltage (V_{RY}) picked up from secondary of control transformer, with three quantizer signals ($\emptyset_R$, $\emptyset_Y$) inputted to the microcomputer. The photographs of Fig. 4(ii) show the 180° out of phase sinewave to the synchronous machine terminal voltage (V_{RY}) with

the quantizer signal ($\emptyset_R$), base interrupt (IR_3) and firing pulse of the Th_1 thyristor of inverter (CM). The base interrupt occurs at every 60° degree in one cycle of machine voltage. The $\emptyset_R$ quantizer is in phase with the synchronous machine R-Y terminal voltage.

The photographs of Fig. 4(iii) and 4(iv) shows one quantizer signal ($\emptyset_R$) along with all the six firing pulses (for thyristors, Th_1, Th_2, Th_3, Th_4, Th_5 and Th_6) of the inverter. Each pulse clearly has 120° duration and is displaced by 60° from one to another. These waveforms are similar to theoretical waveforms. The photographs of Fig. 4(v) shows a signal 180° out of phase to R-Y line voltage (from secondary of stepdown control transformer) with square wave (zero crossing), IR_o interrupt and IR_1 interrupt. These interrupts are used to give control signal to the rectifier circuit. The photographs of Fig. 4(vi) and 4(vii) shows the zero crossing square wave with all the six firing pulses of rectifier thyristors (Th_1, Th_2, Th_3, Th_4, Th_5 and Th_6); each has 120° duration and they are displaced by 60° from one another.

The d.c. link voltage waveform and the d.c. link current waveform at starting i.e. under discontinuous mode of operation are shown in the photographs of Fig. 4(viii) and 4(ix) under different reference speed setting. The d.c. link current I_{dc} is discontinuous in starting. The photographs of Fig. 4(x) to 4(xii) show the waveforms of d.c. link voltage V_{dc} and d.c. link current I_{dc} for different reference speed setting at no load under LCI mode of operation. The photographs of Fig. 4(xiii) to 4(xv) show the waveform of the machine terminal voltage and the current (armature current) under different operating conditions at load under LCI mode of operation. The various observations taken during these settings are noted below the waveforms.



ig.4(i) : 180° out of synchronous achine terminal voltage waveform V_{RY}) and three quantizer signals ϕ_R, ϕ_Y and ϕ_B respectively.

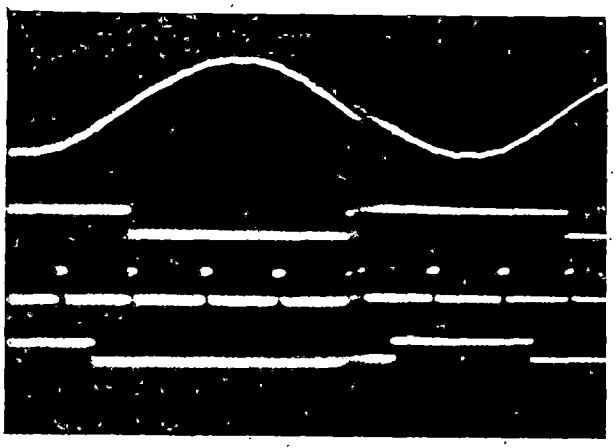
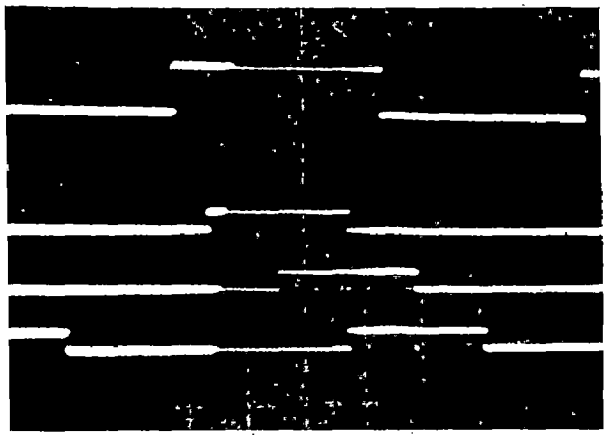


Fig. 4(ii): 180° out of synchronous machine terminal voltage waveform (V_{RY}), quantizer signal (ϕ_R), Base interrupts (IR_3) and firing pulse of Th_1 of inverter (CM).



ig.4(iii): The quantizer signal ϕ_R) and three firing pulses of he inverter (to Th_1, Th_2, Th_3).

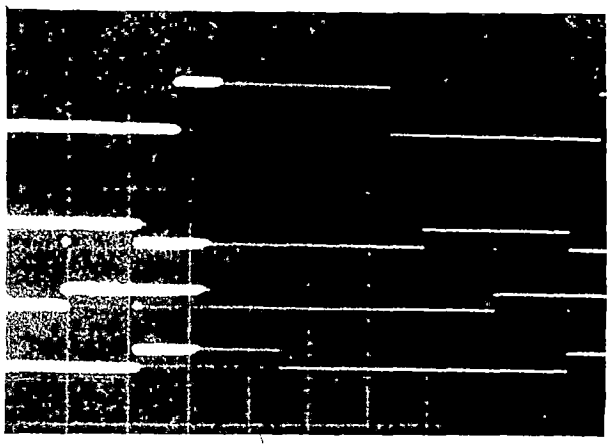


Fig.4(iv): The quantizer signal (ϕ_R) and three firing pulses of the inverter (to Th_4, Th_5, Th_6).

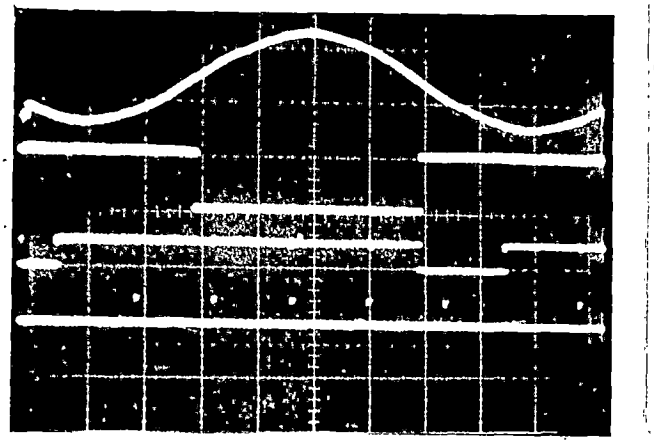


Fig.4(v): Waveform of 180° out of voltage to rectifier (V_{RY}), square-wave, signals of IR_o interrupt and IR_1 interrupt.

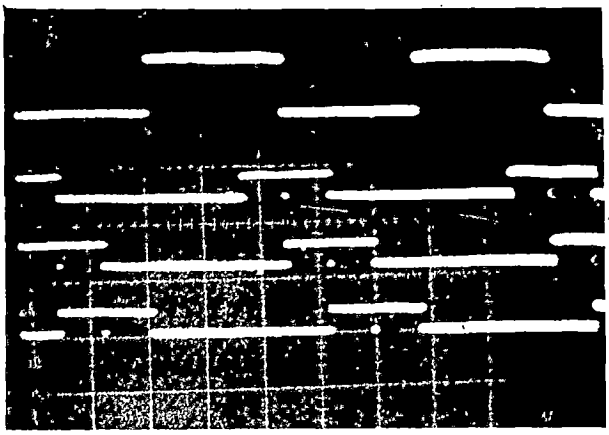


Fig.4(vi): Zero crossing square-wave and the signals of three firing pulses (Th_1, Th_2, Th_3) of rectifier (CS).

Fig.4(vii): Zero crossing squarewave and three firing pulses (Th_4, Th_5, Th_6) of rectifier (CS).

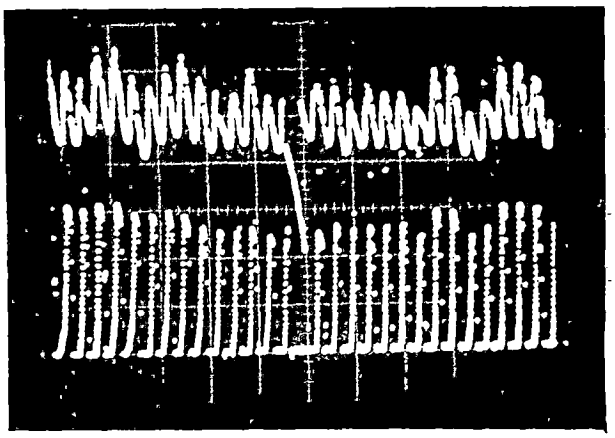
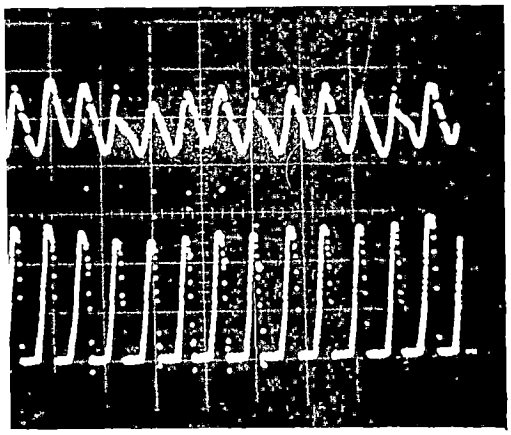


Fig. 4(viii): Waveform of D.C. link voltage and D.C. link current at starting. Speed equals 40 rpm, V_{dc}= 30 V.



Waveforms of D.C. link vol-
.C. link current at start-
80 rpm, V_{dc} = 90V, I_{dc}=1A.

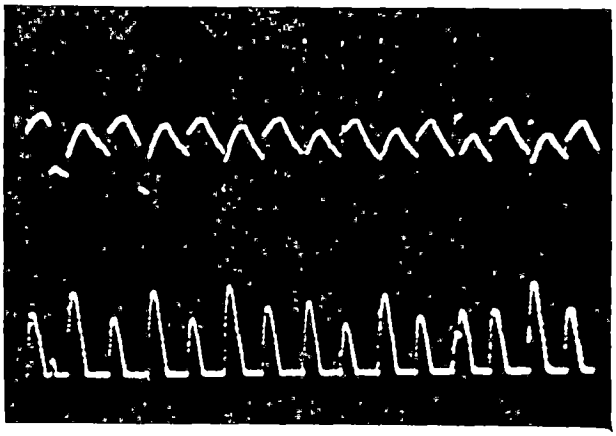
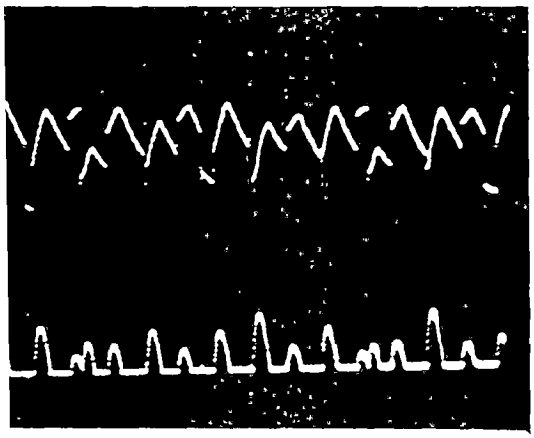


Fig.4(x): Waveforms of D.C. link voltage and the D.C. link current under No load LCI Mode, V_m = 160V, I_{sy}=1.3A, V_{dc} = 230V, I_{dc}=1A, N = 575 rpm.



Waveforms of D.C. link vol-
ne D.C. link current under
I Mode, V_m = 245V, I_{sy}=1.7A,
, V_{dc}= 280V, N = 920 rpm.

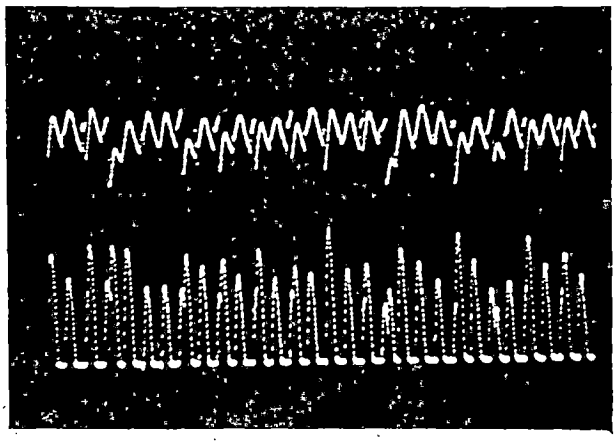
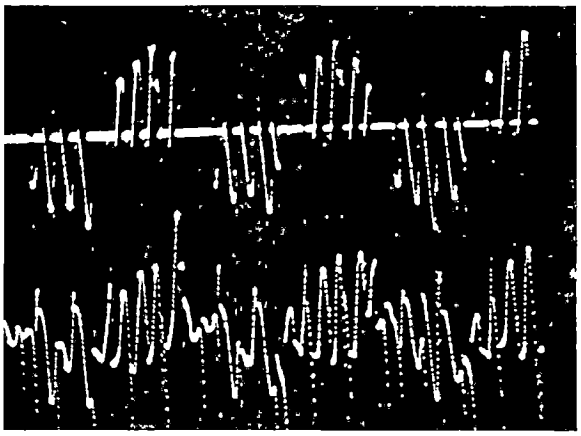


Fig.4(xii): Waveforms of D.C. link voltage and D.C. link current at load, V_{dc} = 325V, V_m = 255V, I_{sy} = 3A, I_{dc} = 2.4A, V_a = 125V, I_a=2.6A, N = 800 rpm.



4(xiii): Waveforms of machine
minal voltage (V_m) and arma-
e current (I_{sy}) at load
reference speed setting
rpm, V_m = 245V, I_{sy}=3A,
=2.4A, V_{dc}= 325V.

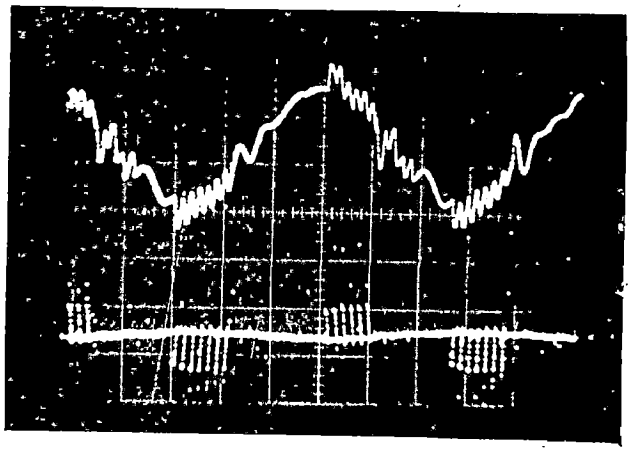
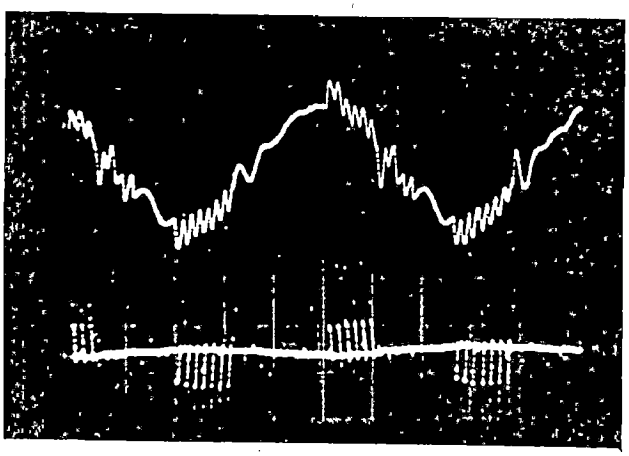


Fig. 4(xiv): Waveforms of machine terminal voltage (V_m) and armature current (I_{sy}) at No load for the speed setting 715 rpm, V_{dc}=330V, V_m = 250V, I_{sy}= 1.4A, I_{dc}= 1A.



4(xv): Waveforms of machine terminal voltage and armature current
reference speed setting, N=1067 rpm, V_{dc} = 390V, I_{dc} = 1.4A,
= 345V, I_{sy} = 2.2 A.

4.7 CONCLUSIONS

The experimental performance of the microprocessor based steady state performance of LCI-SM system under no load and loaded conditions extensively described in this chapter. It is seen that the drive works satisfactorily as a variable speed drive. It is found that the torque of the synchronous machine is dependent on (i) D.C. link current, (ii) commutation margin angle, and (iii) field current. The speed of the synchronous machine can be controlled by varying (a) The d.c. link voltage V_{dc} (b) The margin angle of inverter (γ) and (c) Field current I_f. The drive's characteristics are similar to a separately excited d.c. motor.

It is practically observed that the µp-controlled drive can be operated over a wide range of speed, ranging from 300 RPM to 1500 RPM, and can be loaded to the limit determined by the thyristors used. At reduced field currents, the drive fails to operate in LCI mode successfully. The load characteristics are almost shunt in nature. The power factor is nearly constant at a constant margin angle γ . Efficiency of the drive is better at higher value of d.c. link voltage. The waveforms are similar to the theoretical waveforms.

CHAPTER - 5

CONCLUSIONS

5.1 MAIN CONCLUSIONS

In this investigations, the design and development of micro-computer based self controlled synchronous motor drive has been carried out for its starting and wide range speed control. For these purposes, two fully controlled thyristor converters have been fabricated, one to work as rectifier (CS) and another as inverter (CM) with proper protection. An 8085 microprocessor based system alongwith interfacing for inputting the reference speed, the speed measurement, firing angle control of both converters, has been developed. The automatic starting of LCI-synchronous motor drive has been only partly successful.

The power circuit is a three-phase fully controlled converter bridges. The firing angle for the rectifier can be varied from 0° to 90° to get the required d.c. link voltage so that there can be wide range of speed control of synchronous motor. In this present work, the inverter is operated with a certain fixed firing angle setting.

The firing of thyristors is controlled by microprocessor. The synchronization and zero crossing detection is achieved by hardware cum software scheme through microcomputer. With this scheme, the thyristors are fired at the appropriate instants for the required firing angles.

The developed LCI-synchronous motor have works under an open loop control scheme. A remarkable improvement in performance of the system interms of stability and reliability of firing pulses is obtained by adopting microcomputer based firing scheme. The software based scheme

provides an added flexibility interms of accurate firing angle setting. The necessary firing commands have been generated through software. The ADC interfacing to measure the drive frequency and actual speed has been developed through microprocessor control scheme, to achieve the drives control accurately; both of these variables are also continuously displayed.

Steady State Performance of LCI-SM System

The steady state characteristics of LCI-SM system has shown that it works satisfactorily as variable speed drive popularly known as the DC commutatorless motor. Some vital observations based upon the experiments carried out on the LCI-SM system are as follows:

(i) It is found that the torque of the synchronous machine depends upon

(a) the d.c. link current

(b) the margin angle of inverter,

(c) the field current.

(ii) It is clearly observed that the variation of speed with DC link voltage, V_{dc}, results in precise control of speed of CLM. A speed variation from 20% to almost 100% of rated speed has been practically obtained through the control of d.c. link voltage.

(iii) The field current and the margin angle provide limited speed variation under reduced field currents, the drive fails to operate.

(iv) The terminal voltage output of LCI is almost sinusoidal except for the six notches corresponding to the six commutation overlap region. The line current of the inverter is alternating in nature.

The complete system consisting of zero crossing and synchronization circuits, thyristorized fully controlled power converters, digital speed and drive frequency measurement scheme circuit, pulse amplifier circuit, and interfacing of μp with the system, has been fabricated, and the performance of the drive is evaluated. The experiments are performed on a 3 hp synchronous motor.

It is evident from the experimental studies that the microprocessor based open loop control scheme provides satisfactory performance, and the speed of the drive can be varied over a wide range. The speed regulation of μp controlled drive is quite superior to that of the natural machine.

5.2 SUGGESTIONS FOR FURTHER WORK

Though the basic objectives of the investigation have been brought to a successful conclusion, certain problems have arisen during the course of investigation which would require further work. These problems with some other interested objections are given here for further investigations:

(i) In this work only the armature control is adopted using microcomputer, however, the machine field control may also be included using some extra digital scheme.

(ii) The reported work was only limited to one quadrant operation of the drive and needs further work to extend its operation

for four quadrant operations.

(iii) The closed loop control of the drive for constant h.p. operation and constant torque operation may also to be investigated.

(iv) For a precise speed control of the drive, an improved speed sensing system alongwith a higher bit microcomputer may be adopted to achieve better speed regulation using a good control algorithm with closed loop implementation.

(v) The work with closed loop microcomputer control may also be extended for permanent magnet synchronous motor to result in a complete brushless and robust structured drive.

(vi) The analysis and modelling of the drive for closed loop control scheme may also to be investigated.

(vii) Work needs also to be done on the analysis for investigation of frequency and flux at starting and improvement of the starting method of the drive for higher starting torque with lower value of current from supply.

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APPENDIX A

RATINGS OF MOTOR USED FOR EXPERIMENTAL WORK

SYNCHRONOUS MACHINE (SM_1)

3Ø, 230V, 3HP, 1500 RPM

COSØ = 0.8, CYCLES = 50, EXC: 230V

DC MOTOR (G_1)

230V, I=19.8A, 5 HP

RPM = 1500

SYNCHRONOUS MACHINE (SM_2)

3Ø, 400V, 5HP

SPEED=1500 RPM, CYCLES=50

RATING CONSTANT

DC MOTOR (G_2)

220V, AMPS;13.6

COMPOUND WINDING, SPEED 1500 RPM

3 KW, RATING CONSTANT

APPENDIX B

GENERAL DESCRIPTION OF µp KIT

VMC 85/9 is a single board MICROPROCESSOR TRAINING/DEVELOPMENT KIT. This provides 2K bytes of RAM and 4K bytes of EPROM. The total on board memory can be very easily expanded to 64 K bytes in an appropriate combination of RAM and ROM.

The input/output structure of VMC-85/9 provides 24 programmable I/O lines expandable to 48 I/O lines. It has got 16 bit programmable Timer/Counter for generating any type of counting etc. The on board 8255 provides 8 levels of interrupts.

SYSTEM SPECIFICATIONS

CPU	8 bit Microprocessor, the 8085A
MEMORY	Total on board capacity 64K bytes
RAM	2K bytes (6116), space for furtner expansion
ROM	4K bytes of EPROM loaded with powerful monitor program (2732)
TIMER	16 bit programmable timer/counter using 8253

I/O - 24 I/O lines expandable to 48 I/O using 8255 PPI

INTERRUPTS	8 different level interrupts through 8259
POWER SUPPLY	+5V, 1.5A for the kit
OPERATING TEM.	0 to 50°C.

B.1 ADDRESSES OF VARIOUS PERIPHERAL DEVICES AND I/O PORTS

SELECTED DEVICE : 8255 (PPI)-1

PORT ADDRESS (H)	PORT
00 and 04	Port A
01 and 05	Port B
02 and 06	Port C
03 and 07	Control word

SELECTED DEVICE : 8255 (PPI)-2

08 and 0C	Port A
09 and 0D	Port B
0A and 0E	Port C
0B and 0F	Control word

SELECTED DEVICE: 8253 (PIT)

10 and 14	Counter 0
11 and 15	Counter 1
12 and 16	Counter 2
13 and 17	Control word

SELECTED DEVICE: 8259 (PIC)

28 and 2C	Data word
29 and 20	Command word

EXTRA TIMER CARD PORT AND COUNTERADDRESSES

8255-1	50-Port A
	51-Port B
	52-Port C
	53-Control word
8255-2	54-Port A
	55-Port B
	56-Port C
	57-Control word
8253	58-Counter-0
	59-Counter 1
	5A-Counter 2
	5B-Command word

SIGNAL AT CONNECTORS J1, J2 AND J3

J1:SPACE	J2:SPACE	J3:SPACE
(1) CAS0	(1) P1C4	(1) P2C4
(2) CAS1	(2) P1C5	(2) P2C5
(3) CAS2	(3) P2C2	(3) P2C2
(4) SP/EN	(4) P1C3	(4) P2C3
(5) IR0	(5) P1C0	(5) P2C0
(6) IR1	(6) P1C1	(6) P2C1
(7) IR2	(7) P1B6	(7) P2B6

(8) IR3	(8) P1B7	(8) P2B7
(9) IR4	(9) P1B4	(9) P2B4
(10) IR5	(10) P1B5	(10) P2B5
(11) IR6	(11) P1B2	(11) P1B2
(12) IR7	(12) P1B3	(12) P2B3
(13) CLK-0	(13) P1B0	(13) P2B0
(14) GATE-0	(14) P1B1	(14) P2B1
(15) OUT-0	(15) P1B6	(15) P2B6
(16) CLK-1	(16) P1B7	(16) P2B7
(17) GATE-1	(17) P1A4	(17) P2A4
(18) OUT-1	(18) P1A5	(18) P2A5
(19) CLK-2	(19) P1A2	(19) P2A2
(20) GATE-2	(20) P1A3	(20) P2A3
(21) OUT-2	(21) P1A0	(21) P2A0
(22) RST 7.5	(22) P1A1	(22) P2A1
(23) RST 6.5	(23) P1C6	(23) P2C6
(24) MP,	(24) P1C7	(24) P2C7
(25) GND	(25) GND	(25) GND
(26) GND	(26) GND	(26) GND

APPENDIX-C

PIN CONNECTION DIAGRAMS OF VARIOUS IC CHIPS USED BY THE AUTHOR IN THE PRESENT WORK ARE GIVEN AS FOLLOWS.

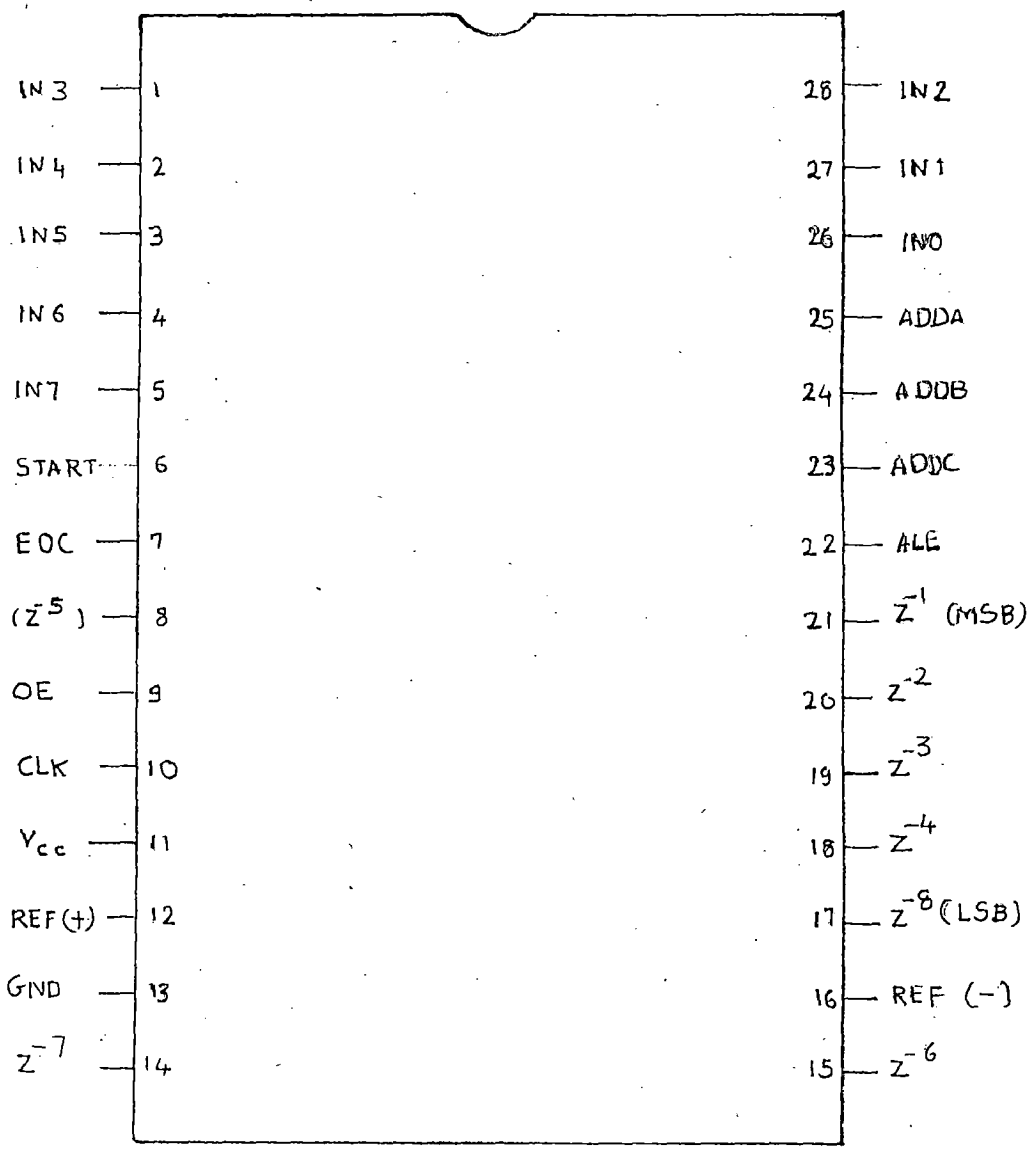


FIG. C.1. 0809 (ADC) PIN CONNECTION

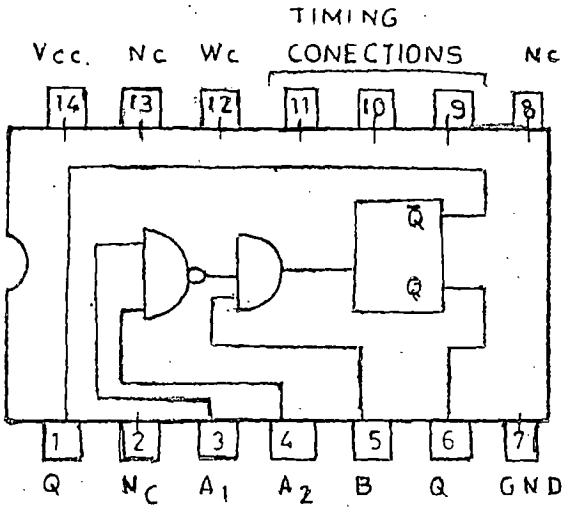


FIG. C·2 74121 MONOSTABLE MULTIVIBRATOR) PIN CONFIGURATION

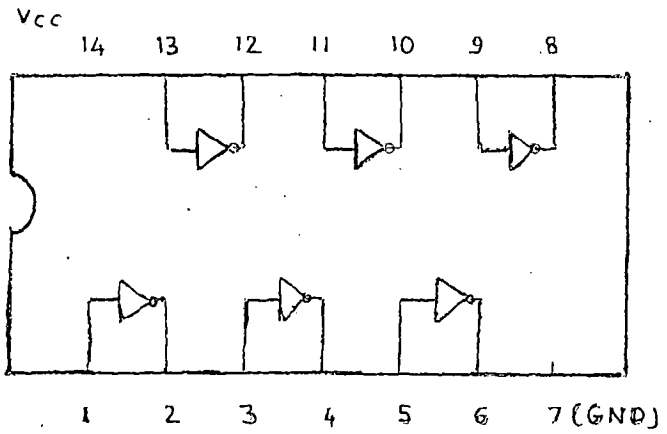


FIG. C·3 7404 (HEXINVERTER) PIN CONFIGURATION

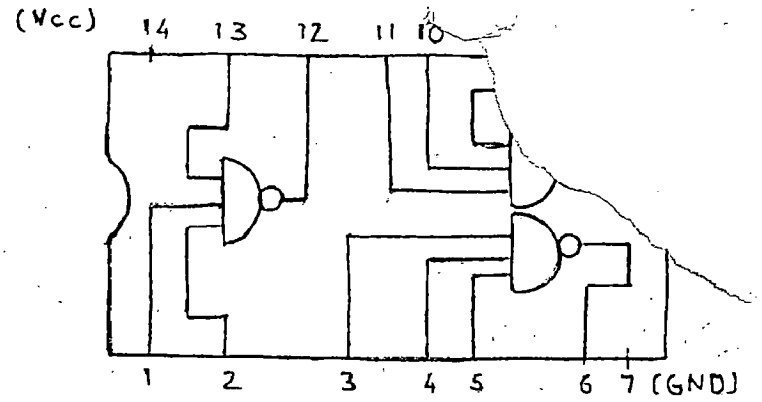


FIG. C-4 7410 (TRIPLE-INPUT NAND GATE) PIN CONFIGURATION

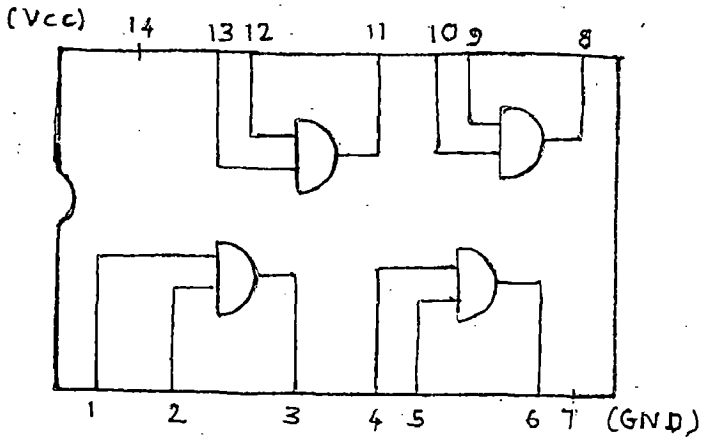


FIG. C-5 7408 (QUAD 2-INPUT NAND GATE) PIN CONFIGURATION

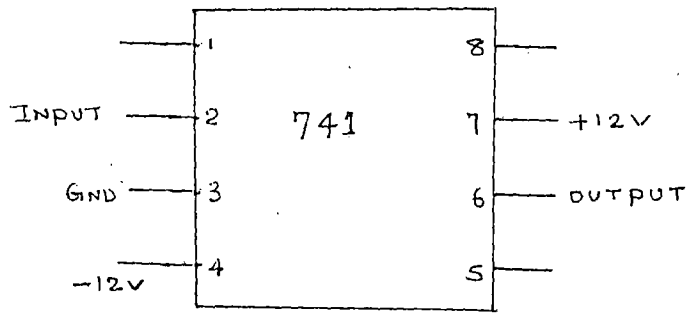


FIG C 6. 741 I C (AS COMPARATOR)

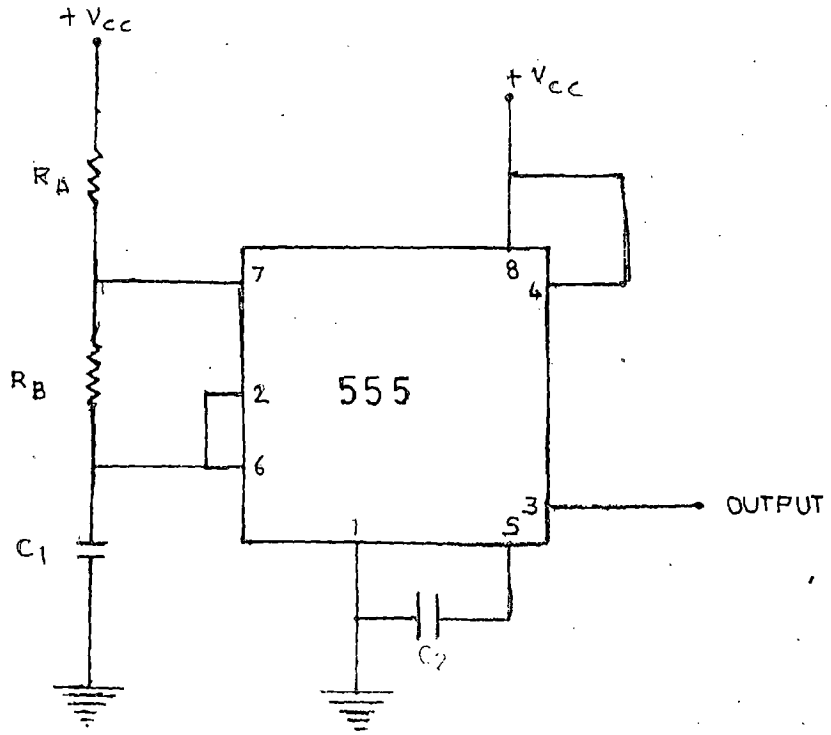
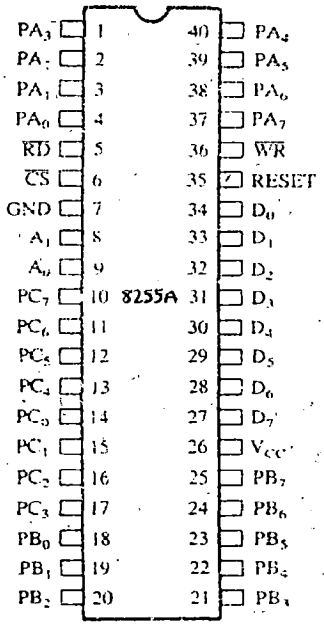


FIG C.7. 555 TIMER (AS AN OSCILLATOR)
PIN CONNECTION DIAGRAM

Pin Configuration

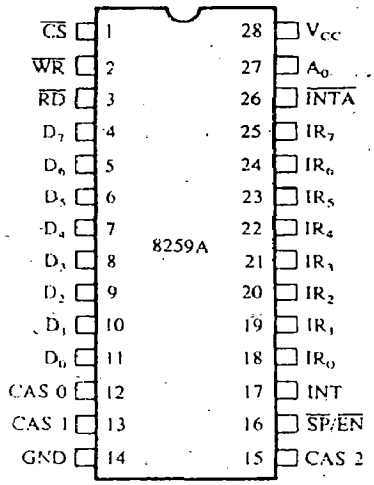


Pin Names

D_7–D_0	Data Bus (Bidirectional)
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0, A_1	Port Address
PA_7–PA_0	Port A (Bit)
PB_7–PB_0	Port B (Bit)
PC_7–PC_0	Port C (Bit)
V_{CC}	+5 Volts
GND	0 Volts

FIGURE C·8 8255A Block Diagram

Pin Configuration

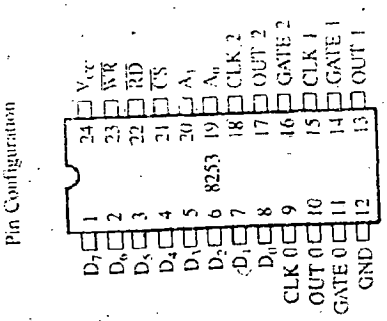


Pin Names

D_7–D_0	Data Bus (Bidirectional)
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0	Command Select Address
$\overline{CS}$	Chip Select
CAS_2–CAS_0	Cascade Lines
$\overline{SP}$/$\overline{EN}$	Slave Program/Enable Buffer
INT	Interrupt Output
$\overline{INTA}$	Interrupt Acknowledge Input
IR_7–IR_0	Interrupt Request Inputs

FIGURE C·10
The 8259A Block Diagram

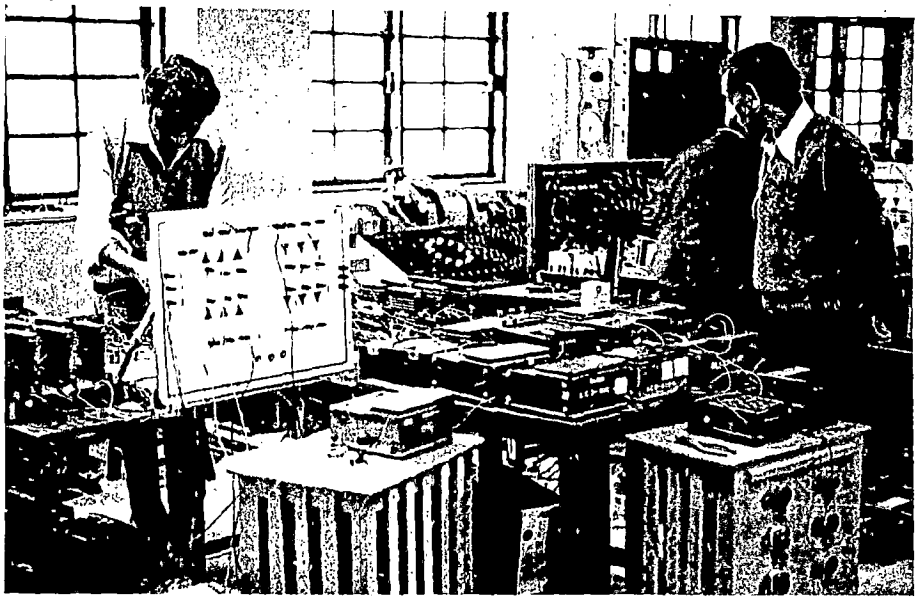
Pin Configuration

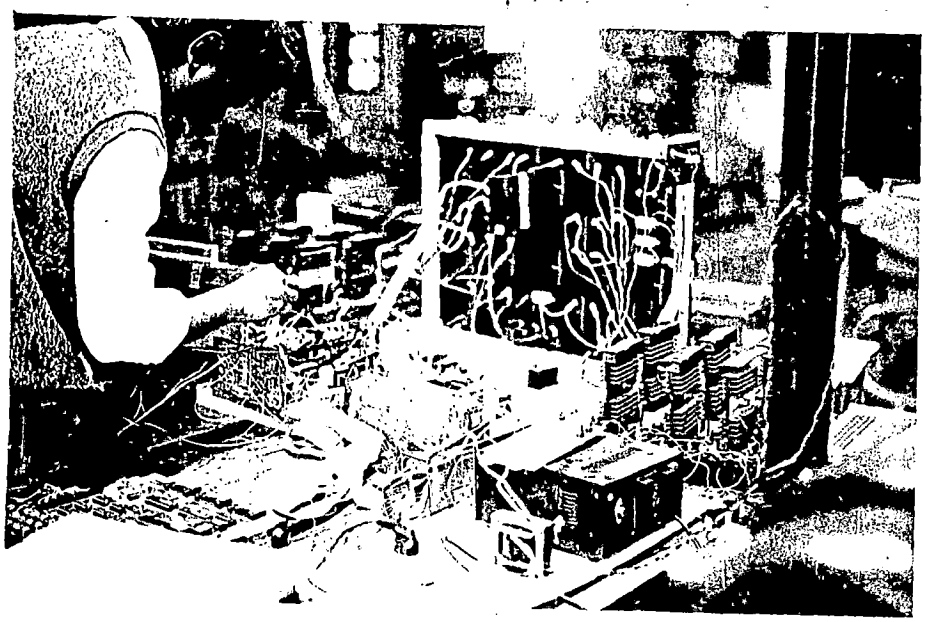


Pin Names

D_7–D_0	Data Bus (8 Bit)
CLK N	Counter Clock Inputs
GATE N	Counter Gate Inputs
OUT N	Counter Outputs
$\overline{RD}$	Read Counter
$\overline{WR}$	Write Command or Data
$\overline{CS}$	Chip Select
A_0–A_1	Counter Select
V_{CC}	+5 Volts
GND	Ground

FIGURE C·9
8253 Block Diagram





TWO VIEWS OF EXPERIMENTAL SETUP

(8) IR3	(8) P1B7	(8) P2B7
(9) IR4	(9) P1B4	(9) P2B4
(10) IR5	(10) P1B5	(10) P2B5
(11) IR6	(11) P1B2	(11) P1B2
(12) IR7	(12) P1B3	(12) P2B3
(13) CLK-0	(13) P1B0	(13) P2B0
(14) GATE-0	(14) P1B1	(14) P2B1
(15) OUT-0	(15) P1B6	(15) P2B6
(16) CLK-1	(16) P1B7	(16) P2B7
(17) GATE-1	(17) P1A4	(17) P2A4
(18) OUT-1	(18) P1A5	(18) P2A5
(19) CLK-2	(19) P1A2	(19) P2A2
(20) GATE-2	(20) P1A3	(20) P2A3
(21) OUT-2	(21) P1A0	(21) P2A0
(22) RST 7.5	(22) P1A1	(22) P2A1
(23) RST 6.5	(23) P1C6	(23) P2C6
(24) MP,	(24) P1C7	(24) P2C7
(25) GND	(25) GND	(25) GND
(26) GND	(26) GND	(26) GND