

OPTIMAL COMPONENT PLACEMENT ON PRINTED CIRCUIT BOARDS

A DISSERTATION

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the requirements for the award of the degree
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MASTER OF ENGINEERING
in
ELECTRICAL ENGINEERING
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By

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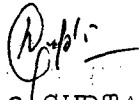
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CERTIFICATE

Certified that the dissertation entitled 'OPTIMAL COMPONENT PLACEMENT ON PRINTED CIRCUIT BOARDS' being submitted by Shri Manoj Jain in partial fulfilment of the requirements for the award of the degree of MASTER OF ENGINEERING in ELECTRICAL ENGINEERING with specialization in SYSTEM ENGINEERING AND OPERATIONS RESEARCH of the University of Roorkee, Roorkee [India], is an authentic record of his own work carried out by him under our supervision and guidance. The matter embodied in this dissertation has not been submitted for award of any other Degree or Diploma.

This is to further certify that he has worked for a period of about six months from August 1987 to January 1988 for preparing this dissertation.


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A B S T R A C T

The circuit layout problem is an important facet of physical design of electrical circuits as the cost, performance, maintenance and reliability of any electronic circuit also depend on the placement of circuit components on the printed circuit board. The partitioning and layout of printed circuit boards is a very important phase in making a good physical design of an electronic system.

In this dissertation methods have been developed to obtain optimal component placement on double and multilayer printed circuit boards. The component placement is obtained such that the design avoids the congested area, excess cross-overs or holes, long etches, strong capacitance, temperature rise of components due to thermal coupling and improves the reliability of the circuit. An efficient iterative algorithm based on sensitivity analysis is presented to achieve optimal placement of circuit components (similar or dissimilar in size). A technique for obtaining a good initial placement of components is also developed. The formulation of via assignment problem for multilayer printed circuit board has been dealt with and a refined heuristic algorithm is developed for its solution.

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4.1 Conclusions

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LIST OF SYMBOLS

A initial via column matrix defined as

$$a_{ij} = \begin{cases} 1, & \text{if net } N_j \text{ contains a pin in row } i \\ 0, & \text{otherwise} \end{cases}$$

A_0 final via column matrix

a number of horizontal divisions on the board

b number of vertical divisions on the board

c connection matrix of order $N \times N$ defined as

$$c_{ij} = \begin{cases} k, & \text{if components } E_i \text{ and } E_j \text{ are} \\ & \text{connected by } k \text{ wires} \\ 0, & \text{otherwise} \end{cases}$$

C_p vector to indicate whether a component is placed on the board such that

$$c_{p_i} = \begin{cases} 1, & \text{if } E_i \text{ is placed on the board} \\ 0, & \text{otherwise} \end{cases}$$

E_i component i , $i=1,2,\dots,N$

E_{N+i} fictitious component placed in empty cell

$$i=1,2,\dots,ab-N$$

e_a activation energy

F objective function to be minimized for placement

F_h number of holes

F_l wiring function related to the length of etches

F_d wiring function related to the interconnection densities, in horizontal and vertical sections of the board

F_c wiring function related to the stray capacitance

F_r objective function related to the temperature rise of components due to thermal coupling between them

$\Delta F_i(s,t)$ increment in function F_i due to interchange of components E_s and E_t in the placement matrix P [G,H] matrix obtained from connection matrix C and placement matrix P, such that

$$\varepsilon_{ij} = \sum_{k=1}^b c_{i,P_{jk}} \quad \begin{array}{l} i=1,2,\dots,N \\ j=1,2,\dots,a \end{array}$$

$$h_{km} = \sum_{k=1}^a c_{k,P_{km}} \quad \begin{array}{l} i=1,2,\dots,N \\ j=1,2,\dots,b \end{array}$$

K Boltzmann's constant

L net matrix defined as

$$L_{i,j} = \begin{array}{l} N_k, \text{ if } j\text{th pin of component number } i/2 \\ \text{(or } (i+1)/2) \text{ of the lower (or upper)} \\ \text{pin row is connected to the net } N_k \\ 0, \text{ otherwise} \end{array}$$

λ_b length of printed circuit board

λ_c length of the cell i.e. λ_b/b

M matrix of the order $NT \times NT$ defined as

$$m_{ij} = \text{distance between components } E_i \text{ and } E_j$$

N number of components to be placed

N_j net, $j=1,2,\dots,NN$

NN total number of nets in the circuit

NP number of pins in each row of a component

NR total number of pin rows equal to $(2 \times a)$

NT total number of slots on the board $(a \times b)$

P placement matrix of order $a \times b$ and defined as

$$P_{ij}=k, \text{ if component } E_k \text{ is placed in position } (i,j)$$

Q_i	set of components excluding fictitious components placed in rows 1,2,...,i
R_i	thermal resistance of component E_i when circuit board is assumed to be perfect insulator
R_{ie}	thermal resistance of component E_i when heat transfer in circuit board is taken into account
R_{ij}	coupling thermal resistance between component E_i and E_j
S_i	set of components excluding fictitious components placed in columns 1,2,...,a
T_a	absolute ambient temperature in $^{\circ}\text{K}$.
T_i	absolute junction temperature of component E_i in $^{\circ}\text{K}$
W_i	power dissipation of component E_i
W_{h_i}	interconnection leads passing through ith horizontal section of the board
W_{v_i}	interconnection leads passing through ith vertical section of the board
w_{h_i}	interconnection density in ith horizontal section of the board i.e. W_{h_i}/l_b
w_{v_i}	interconnection density in ith vertical section of the board i.e. W_{v_i}/w_b
w_b	width of the board
w_c	width of the cell i.e. w_b/a
$\lambda(T)$	failure rate of a component at absolute junction temperature T

CHAPTER - 1

INTRODUCTION

1.1 Overview

In the design of present day large scale electronic systems, high density packaging is achieved by proper design and interconnection of its subsystems. The design involves placement of components and interconnections at three different levels. At the lowest level, logic elements are to be placed and routed on a semiconductor wafer. A printed circuit board is used at the second level with ICs and other components instead of logic elements. Set of PCBs form the backplane which is the third level of the layout problem.

Printed circuit boards are certainly a very important element in the fabrication of electronic equipment. It is the design of properly laid out PCBs that determine many of the limiting properties with respect to noise immunity, fast pulse, high frequency and low level characteristics of the equipment. High power PCBs in their turn require a special design strategy. The design of PCB forms a distinct factor in electronic circuit performance and reliability. The producibility of a PCB and its assembly and serviceability also depend on the design. All these factors finally get reflected in the price for the electronic equipment, because PCBs constitute about 20 percent of the cost.

1.2 Printed Circuit Board Design

The magnitude and complexity of the PCB design problem is too large to solve ~~en~~ mass. Thus attempts are made to divide the problem into distinct phases which are individually handled. The circuit diagram of a particular electronic system is assumed to be available in the form of design diagrams. An independent physical component is considered as a module and each module has several pins which are to be connected electrically. Each such connection is said to form a Signal Net. A collection of such signal nets describing a complete layout is called a Net list. The individual components are given physical locations on the board surface, so that the electrical connections between them can be done. The positioning of the components can be done to optimize certain characteristics of the layout, such as total wire length, board area, total number of holes, expected congestion, time delay, maximum length of an etch, stray capacitance temperature rise due to thermal coupling etc. Goto and Kuh [4], Patnaik et.al.[10], Quinn and Breuer [11] and many authors use only total wire length as the optimization criterion for the placement of components. Gupta [5] has developed a refined iterative multicriteria optimization placement algorithm based on

1. criterion related to the length of etches,
2. minimization of interconnection wiring density,
3. minimization of stray capacitance,

4. minimization of the effect on the electrical performance and reliability of circuit due to thermal coupling between components.
5. minimization of total number of holes required for the realization of the circuit.

A placement problem is said to be solved if such an optimum physical positioning is achieved for all the components. Having assigned physical locations to electrical pins to be connected, the actual physical laying of conductor patterns is to be attempted. This problem is referred to as the routing problem. The interconnections must again be obtained satisfying certain physical constraints. For example the number of conductor patterns per unit area is limited by the available technology. Also, the number of tracks per unit area must be more or less same throughout the board. To provide the required interconnections between the circuit modules for assembling digital systems, multilayer printed wiring boards (PWB) are used very often. The design rules for these PWB's have been revolutionized with the recent advances in the micro electronics technology. In an ordinary dual in line package the number of etch paths between two consecutive pins is restricted. Kuh et.al [8] have derived necessary and sufficient conditions for minimum street congestion in single row routing. Tsukiyama et.al [16] have described an efficient routing algorithm for special cases of upper and lower street congestions upto two. The studies of single-row routing problems by Kuh et.al.[8]

and Tsukiyama et.al.[16] have been restricted to minimization of the total number of horizontal tracks needed for the realization of a given set of nets. Therefore it has been assumed that enough space exists between adjacent nodes to allow for the wiring. Due to this assumption, realizations obtained from these algorithms require a large number of vertical tracks between adjacent nodes. Du et.al [3] have discussed the single-row routing problem when the number of vertical tracks available between adjacent nodes is bounded by a positive integer called the cross-over bound.

The connections between the different layers in a multilayer wiring board is achieved by plated through holes, also called Vias. Ting et.al.[14] have suggested that a multilayer problem can be reduced to several single line single layer problems by the proper usage of vias. They have also discussed the via assignment problem with the objective of minimizing via columns. Some algorithms for its solution are also proposed. Tsukiyama et.al.[15] have formulated an optimization problem for finding the via assignment. A heuristic algorithm to this optimization problem is also proposed by them. The essence of the via assignment phase is to establish the fact, that the interconnections are feasible. This is accomplished by assigning appropriate vias in order to determine connection patterns of all the nets. A principal objective in this phase is to minimize the number of via columns, thus reducing the size of the board or alternatively increasing the routing area. A set of pins which belong to

the same net and which are located on the same row is called a Generalized pin. Thus individual pins which belong to a generalized pin of a net can be connected without use of vias. The connections for the generalized pins are made first, for the remaining interconnections vias must be used. The manner in which vias are selected is important. After the connection patterns are obtained, the problem of routing is reduced to much simpler problems with routing specifications on a single line basis.

After the preliminary realization one has the choice of perturbing the realization as long as the connection patterns are not disturbed. Because of the fixed placement, the pin locations can not be altered. However the via columns are less rigidly located. Patnaik et.al.[10] have stated the problem as finding the optimum placement of via columns for a given via assignment of a unidirectional routing so that the maximum number of horizontal tracks is minimized. Several available strategies for permuting via columns are also suggested by Patnaik et.al.[10].

After via assignment and linear placement of via columns is carried out, the routing problem reduces to the much simpler problem of single line routing. At this stage the track availability must be considered. The objective of layering is to allow more layers for the purpose of evenly distributing the number of connecting wires on different layers. Chang and Du [2] and Han and Sabnis [6] have discussed some algorithms for the layering problem that arises when the single row routing approach of wire layout is used.

1.3 The Author's Contributions

The goals of this dissertation were to develop more realistic mathematical models and efficient methods for performance optimization of physical design of electronic circuits at various stages of the design process.

The algorithm proposed by Gupta [5] does not include any method for constructive initial placement. The initial placement has to be decided arbitrarily and then the algorithm iteratively optimizes the placement. For different initial placement different local optimal solutions may be obtained. The algorithm also does not incorporate the edge connector which is an important part of a printed circuit board. One of the assumptions made for the algorithm proposed by Gupta [5] is that all the components are similar, and dimensions of the components are such that all components require same area for their placement. This assumption poses severe limitations on the design. In this dissertation all these drawbacks have been taken into account and the algorithm proposed by Gupta [5] is modified.

The important problem of multilayer PCB design has also been taken up for this dissertation. The heuristic algorithm for via assignment problem proposed by Tsukiyama et.al [15] assumes that the placement of pins is fixed. It finds the optimal assignment of via columns by repeated application of the process of column merging and column decomposition. This

algorithm has been modified to find the best placement of pins (or components). The best placement is achieved by the iterative algorithm using sensitivity analysis for which expressions have been derived with a view to reduce the computational effort. The algorithm proposed by Tsukiyama et.al [15] is modified such that an iteration is performed with a view to achieve best results in two consecutive iterations.

1.4 Organization of the dissertation

The problem of component placement on double layer printed circuit board has been dealt with in Chapter 2. Chapter 3 describes the problems associated with multilayer printed circuit boards. Finally Chapter 4 offers general conclusions and suggestions for further research work in this field. Computer programs in FORTRAN-IV have been developed on DEC-2050 which are briefly described in the Appendices.

CHAPTER - 2

COMPONENT PLACEMENT ON DOUBLE LAYER PRINTED CIRCUIT BOARD

2.1 Introduction

The layout design of electronic circuits on printed circuit board is one of the most important and time consuming phases during equipment design process in all electronic industries. The problem of layout design is being made more and more complicated day by day with the advances in the electronics technology. The functional capabilities, speed, frequency and accuracy of electronic circuits have been increasing exponentially. On the other hand, with the increase in all these the electronic components are being miniaturized and made more complex.

Allocation, placement and Routing are the three phases into which laying out of electronic circuits has been divided [5]. The partitioning of circuit components into groups and assignment of these groups to boards or modules is called allocation. To facilitate the routing, the circuit components are assigned to specific locations on the board, this is termed as placement. Routing is the process of laying out of etches on the board to make the interconnections between the individual circuit components. The interrelated problems of allocation, placement and routing are usually solved independently to ease the complex problem of laying out of electronic circuit.

The cost, performance, reliability and maintenance of any electronic circuit depend upon the placement of circuit components on the printed circuit board. The factors which

directly effect the performance of electronic circuits are the interconnection length in high speed circuits, mutual interference and the thermal coupling between components.

The components are to be uniquely placed in an available location on the board. This placement is done in view of some objective function which is to be minimized. The total weighted routing length has been used by many authors [1,4,10,11] as a norm for minimization. The layout of the circuit having large number of holes, has poor reliability and high cost [5]. Therefore minimization of holes criterion is also used for placement of components. Interconnection density or the number of etches passing through a unit space is another factor which effect performance of the circuit. The placement based on this criteria avoids the congested area on the board, provides more space between etches which reduces stray capacitance. The stray capacitance and temperature rise due to thermal coupling between components should be minimum for better performance of a circuit. So placement of components should be achieved by using a combination of the following criteria [5].

1. Minimization of length of etches
2. Interconnection density minimization
3. Stray capacitance minimization
4. Minimization of the effect of thermal coupling between components on the electrical performance and reliability of the circuit.
5. Minimization of the number of holes.

In this chapter the iterative algorithm proposed by Gupta [5] based on the above criteria is discussed. The algorithm is extended for the placement of components which are not similar in size. A technique for a good initial placement of components is also developed.

2.2 The Placement Problem

The individual components are placed at appropriate locations on the board, such that the interconnection can be done easily. The locations assigned to the components on the board are called 'SLOTS'. The components contain pins for connection by physical wires to form SIGNAL SETS. A signal set is a set of pins which must be interconnected to have the same potential. On the basis of a given interconnection the signal sets must be interconnected to form NETS. For the purpose of the placement problem, the pin locations on the components are ignored, and therefore, the signal set becomes a subset of the components. Since a component contains a number of connection pins, it may belong to more than one signal set. The complete interconnection is said to be specified, if all the signal sets have been specified.

So, given a set of components with signal sets defined on subsets of these components, and a set of slots, finding the optimal placement of all modules on the slots, with respect to some norm defined on the interconnections, is the definition of the placement problem.

2.3 Assumptions

1. The printed circuit board is rectangular and divided into $a \times b$ cells of equal size with coordinates (i, j) , $[i=1, 2, \dots, a, j=1, 2, \dots, b]$.
2. (NT-N) fictitious components with zero dissipation and no connection with any other component are also placed on the board. These components are not interchangeable with each other.
3. The input and output terminals appear on a specified edge (vertical) of the board. The position of required terminals on the edge is also determined iteratively with the placement of other components. The edge connector is divided in 'a' parts and each part is treated as a component. First 'a' components E_1, E_2, \dots, E_a correspond to the parts of the edge connector.
4. The components are of two sizes. Dimension of the first type of components is such that each component require one and only one slot for its placement. The other type of component is double in size, that is they require two adjacent slots for their placement. The double sized components are treated as two different components with very high connectivity between them.

2.4 Approach to the placement problem

Following steps are followed for solving a complex placement problem.

2.4.1 Initial Placement

The constructive initial placement methods selects components, one at a time based on an evaluation function which measures signal set connectivity to components already selected and then decides which slot the components belong to. More specifically, a module is selected from the remaining components which has the maximum number of the interconnections with the components which are already selected. Next we assign the component to be a member of a row and a column. The first 'a' components corresponding to the edge connector are placed before placing the other components. Dummy components are assigned to the vacant slots after placement of all the components.

The steps of constructive algorithm to determine the initial placement configuration are as follows.

1. Find the initial placement of the first 'a' components corresponding to the edge connector by the following method.

(i) Initialize the vector $C_p \leftarrow 0$.

(ii) Find maximum connectivity between any two of first 'a' components

$$c_{k, \ell} = \max_{\substack{i=1, a \\ j=1, a}} [c_{i, j}]$$

(iii) Place the corresponding components in the centre of the connector.

$$IR = \begin{cases} a/2 & , \text{ if } a \text{ is even} \\ (a+1)/2 & , \text{ if } a \text{ is odd} \end{cases}$$

$$P_{IR,b} \leftarrow k, P_{(IR+1),b} \leftarrow \lambda$$

enter E_k and E_λ in C_p

$$c_{p_k} \leftarrow 1, c_{p_\lambda} \leftarrow 1$$

Set $IK \leftarrow 0$

(iv) If all of first 'a' components are placed

$$\text{i.e. } c_{p_i} \Big|_{i=1,a} = 1$$

Stop

(v) $IK \leftarrow IK+1$

(vi) Find

$$c_{m,k} = \max_{i=1,a} [c_{i,k}]$$
$$c_{p_i} \neq 1$$

$$P_{(IR-1K),b} \leftarrow m, k \leftarrow m, c_{p_m} \leftarrow 1$$

(vii) If all of first 'a' components are placed

$$\text{i.e. } c_{p_i} \Big|_{i=1,a} = 1$$

Stop

(viii) Find

$$c_{m,\lambda} = \max_{i=1,a} [c_{i,\lambda}]$$
$$c_{p_i} \neq \lambda$$

$$P_{(IR+1+1K),b} \leftarrow m, \lambda \leftarrow m, c_{p_m} \leftarrow 1$$

(ix) Return to step (iv).

2. Find the component which has maximum connectivity with the components already placed.

i.e. find k and ℓ such that

$$c_{k,\ell} = \max_{\substack{i=1,N \\ j=1,N \\ c_{pi} \neq 1 \\ c_{pj} = 1}} [c_{ij}]$$

3. Place E_k in the slot nearest to the slot containing E_ℓ by following the method given below

(i) Initialize P_h and P_v , $ph_i \leftarrow 0$ and $pv_i \leftarrow 0 \mid i=1 \dots \max[a,b]$

(ii) Find m,n such that $p_{m,n} = \ell$

(iii) For all $i=1$ to $\max[a,b]$ repeat steps (iv) to (xii)

(iv) $ph_1 \leftarrow m$, $ph_{2q} \mid_{q=1,i} \leftarrow m-q$, $ph_{(2q+1)} \mid_{q=1,i} \leftarrow m+q$

(v) For all $j=1$ to $(2i+1)$ repeat steps (vi) to (xii)

(vi) $p \leftarrow ph_j$

(vii) If $p < 1$ or $p > a$, return to step (v)

If $p = (m-i)$ or $p = (m+i)$, goto step (ix)

If $(n-i) < 1$ or $p_{p,(n-i)} \neq 0$, goto step (viii)

$p_{p,(n-i)} \leftarrow k$

Stop.

(viii) If $(n+i) > b$ or $p_{p,(n+i)} \neq 0$, return to step (v)

$p_{p,(n+i)} \leftarrow k$

Stop

(ix) $pv_1 \leftarrow n$, $pv_{2q} \mid_{q=1,i} \leftarrow n-q$, $pv_{(2q+1)} \mid_{q=1,i} \leftarrow n+q$

(x) For all $q = 1$ to $(2i+1)$ repeat steps (xi) to (xii)

(xi) $q \leftarrow Rv_0$

(xii) If $q < 1$, $q > n$ or $p_{p,q} \neq 0$, return to step (x)

$p_{p,q} \leftarrow k$

stop

4. If $c_{p_i | i=1, N} = 1$, return to step 2.

5. Place dummy components in the remaining slots.

For $k = (N+1)$ to NT

If $p_{i,j} = 0$, $i=1 \dots a$, $j=1, \dots, t$

$p_{ij} \leftarrow k$

The constructive algorithm suggested above is a quick and straight forward method whose solution is not optimum but may be close to it. This method gives good results for many applications. This placement configuration is changed in iterative fashion to give better solutions.

Example 2.1 Consider that the board divided in 4 horizontal and 4 vertical divisions and there are six components to be placed with connection matrix as,

$$C = \begin{bmatrix} 0 & 3 & 4 & 2 & 4 & 0 & 0 & 3 & 2 & 1 \\ 3 & 0 & 0 & 1 & 0 & 2 & 1 & 0 & 0 & 4 \\ 4 & 0 & 0 & 2 & 3 & 0 & 9 & 1 & 5 & 6 \\ 2 & 1 & 2 & 0 & 1 & 7 & 1 & 4 & 0 & 0 \\ 4 & 0 & 3 & 1 & 0 & 4 & 8 & 0 & 0 & 3 \\ 0 & 2 & 0 & 7 & 4 & 0 & 0 & 2 & 4 & 0 \\ 0 & 1 & 9 & 1 & 8 & 0 & 0 & 0 & 2 & 1 \\ 3 & 0 & 1 & 4 & 0 & 2 & 0 & 0 & 1 & 2 \\ 2 & 0 & 5 & 0 & 0 & 4 & 2 & 1 & 0 & 9 \\ 1 & 4 & 6 & 0 & 3 & 0 & 1 & 2 & 9 & 0 \end{bmatrix}$$

C_{ij} for $i=1,4$ and $j=1,4$ represent the components corresponding to the edge connector. So in effect there are 10 components to be placed out of which first 4 constitute the edge connector.

Solution

1. (i) $C_p = (0, 0, 0, 0, 0, 0, 0, 0, 0, 0)$

$$P = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}$$

(ii) $c_{k\ell} = c_{13} = 4$

(iii) $IR \leftarrow 2, P_{2,4} \leftarrow 1, P_{3,4} \leftarrow 3, IK \leftarrow 0$

$$C_p = (1, 0, 1, 0, 0, 0, 0, 0, 0, 0),$$

$$P = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 3 \\ 0 & 0 & 0 & 0 \end{bmatrix}$$

(v) $IK = 1$

(vi) $c_{mk} = c_{2,1} = 3, P_{1,4} \leftarrow 2, k \leftarrow 2$

$$C_p = (1, 1, 1, 0, 0, 0, 0, 0, 0, 0)$$

$$P = \begin{bmatrix} 0 & 0 & 0 & 2 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 3 \\ 0 & 0 & 0 & 0 \end{bmatrix}$$

(viii) $c_{m\ell} = c_{4,3} = 2, P_{4,4} \leftarrow 4, \ell \leftarrow 4$

$$C_p = (1, 1, 1, 1, 0, 0, 0, 0, 0, 0)$$

$$P = \begin{bmatrix} 0 & 0 & 0 & 2 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 3 \\ 0 & 0 & 0 & 4 \end{bmatrix}$$

2. $c_{k\lambda} = c_{7,3} = p_9, \quad C_p = (1,1,1,1,0,0,1,0,0,0)$

3. (ii) $m=3,$
 $n=4$

(iii) $\max [a,b] = 4, i=1$

(iv) $Ph_1 \leftarrow 3, \quad Ph_2 \leftarrow 2, \quad Ph_3 \leftarrow 4$

(v) $j = 1$

(vi) $p \leftarrow Ph_1 = 3$

(vii) $p_{3,3} = 7$

$$P = \begin{bmatrix} 0 & 0 & 0 & 2 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 7 & 3 \\ 0 & 0 & 0 & 4 \end{bmatrix}$$

2. $c_{k\lambda} = c_{5,7} = 8, \quad C_p = (1,1,1,1,1,0,1,0,0,0)$

3. (ii) $m = 3,$
 $n = 3$

(iii) $i \leftarrow 1$

(iv) $Ph_1 \leftarrow 3, \quad Ph_2 \leftarrow 2, \quad Ph_3 \leftarrow 4$

(v) $j \leftarrow 1$

(vi) $p \leftarrow Ph_1 = 3$

(vii) $p_{3,2} \leftarrow 5$

$$P = \begin{bmatrix} 0 & 0 & 0 & 2 \\ 0 & 0 & 0 & 1 \\ 0 & 5 & 7 & 3 \\ 0 & 0 & 0 & 4 \end{bmatrix}$$

2. $c_{k\ell} = c_{6,4} = 7, C_p = (1, 1, 1, 1, 1, 1, 1, 0, 0, 0)$

3. (ii) $m = 4$
 $n = 4$

(iii) $i \leftarrow 1$

(iv) $Ph_1 \leftarrow 4, Ph_2 \leftarrow 3, Ph_3 \leftarrow 5$

(v) $j \leftarrow 1$

(vi) $p \leftarrow Ph_1 = 4$

(vii) $p_{4,3} \leftarrow 6$

$$P = \begin{bmatrix} 0 & 0 & 0 & 2 \\ 0 & 0 & 0 & 1 \\ 0 & 5 & 7 & 3 \\ 0 & 0 & 6 & 4 \end{bmatrix}$$

2. $c_{k\ell} = c_{10,3} = 6, C_p = (1, 1, 1, 1, 1, 1, 1, 0, 0, 1)$

3. (i) $m=3,$
 $n=4$

(iii) $i \leftarrow 1$

(iv) $Ph_1 \leftarrow 3, Ph_2 \leftarrow 2, Ph_3 \leftarrow 4$

(v) $p \leftarrow Ph_1 = 3$

(v) $j \leftarrow 1$

(vi) $p \leftarrow Ph_1 = 3$

(vii) $P_{3,3} = 7 \neq 0$

(viii) $(n+1) = 5 > b$

(v) $j = 2$

(vi) $p \leftarrow Ph_2 = 2$

(vii) $p = 2 = (m-i)$

(ix) $Pv_1 \leftarrow 4, Pv_2 \leftarrow 3, Pv_3 \leftarrow 5$

(x) $o \leftarrow 1$

(xi) $q \leftarrow Pv_1 = 4$

(xii) $P_{pq} = P_{2,4} = 1 \neq 0$

(x) $o \leftarrow 2$

(xi) $q \leftarrow Pv_2 = 3$

(xii) $P_{2,3} \leftarrow 10$

$$P = \begin{bmatrix} 0 & 0 & 0 & 2 \\ 0 & 0 & 10 & 1 \\ 0 & 5 & 7 & 3 \\ 0 & 0 & 6 & 4 \end{bmatrix}$$

2. $c_{k\ell} = c_{9,10} = 9, C_p = (1,1,1,1,1,1,1,0,1,1)$

3. (ii) $m=2, n=3$

(iii) $i \leftarrow 1$

(iv) $Ph_1 \leftarrow 2, Ph_2 \leftarrow 1, Ph_3 \leftarrow 3$

(v) $j \leftarrow 1$

(vi) $p \leftarrow Ph_1 = 2$

(vii) $P_{2,2} \leftarrow 9$

$$P = \begin{bmatrix} 0 & 0 & 0 & 2 \\ 0 & 9 & 10 & 1 \\ 0 & 5 & 7 & 3 \\ 0 & 0 & 6 & 4 \end{bmatrix}$$

2. $c_{k\ell} = c_{8,2} = 5$, $C_p = (1, 1, 1, 1, 1, 1, 1, 1, 1, 1)$

3. (ii) $m=1$, $n=4$

(iii) $i \leftarrow 1$

(iv) $Ph_1 \leftarrow 1$, $Ph_2 \leftarrow 0$, $Ph_3 \leftarrow 2$

(v) $j \leftarrow 1$

(vi) $p \leftarrow Ph_1 = 1$

(vii) $P_{1,3} \leftarrow 8$

$$P = \begin{bmatrix} 0 & 0 & 8 & 2 \\ 0 & 9 & 10 & 1 \\ 0 & 5 & 7 & 3 \\ 0 & 0 & 6 & 4 \end{bmatrix}$$

5. $P_{1,1} \leftarrow 11$, $P_{1,2} \leftarrow 12$, $P_{2,1} \leftarrow 13$, $P_{3,1} \leftarrow 14$, $P_{4,1} \leftarrow 15$, $P_{4,2} \leftarrow 16$

$$P = \begin{bmatrix} 11 & 12 & 8 & 2 \\ 13 & 9 & 10 & 1 \\ 14 & 5 & 7 & 3 \\ 15 & 16 & 6 & 4 \end{bmatrix}$$

2.4.2 Iterative placement improvement

2.4.2.1 Same sized components

For this phase it is assumed that dimension of the components are such that each component requires one and only one cell for its placement. In other words, the size of the components is practically the same. In this step, the placement configuration is changed in iterative fashion. A new placement configuration with a lower wiring function is obtained after each iteration.

Gupta [5] has derived expressions for calculating the wiring function F based on length of etches, interconnection density, stray capacitance, thermal coupling between components and number of holes. Expressions to determine an incremental set $\Delta F = [\Delta F(s, t), s=1, 2, \dots, N-1, t=(s+1), (s+2), \dots, NT]$ from sensitivity analysis are also derived. The strategy adopted to change the placement configuration in the iteration is to calculate ΔF until the first negative element is encountered and corresponding components are interchanged.

The expressions derived by Gupta [5] are stated below. The matrix $[G:H]$ is formed as

$$[G:H] = \left[\begin{array}{cccc|cccc} g_{11} & g_{12} & \dots & g_{1a} & h_{11} & h_{12} & \dots & h_{1b} \\ \vdots & & & & \vdots & & & \\ g_{N1} & g_{N2} & \dots & g_{Na} & h_{N1} & h_{N2} & \dots & h_{Nb} \end{array} \right]$$

where $g_{i,j} = \sum_{k=1}^b c_{i,p_{jk}}$, $h_{i,m} = \sum_{k=1}^a c_{i,p_{k,m}}$

$$\forall i \in I_3, \forall j \in I_1 \text{ and } \forall m \in I_2$$

$$I_1 = (1, 2, \dots, a), I_2 = (1, 2, \dots, b)$$

and I_3 is a set of components $(1, 2, \dots, N)$

g_{ij} gives the total number of wires connecting E_i with the components in the j th row of placement matrix P . h_{im} gives the number of wires connecting components E_i with the components in the m th column of the matrix P .

Objective function (F)

$$F = n_h F_h + n_l F_l + n_d F_d + n_c F_c + n_r F_r \quad (2.4.2.2)$$

where n_h, n_c, n_d, n_l, n_r are the weightage given to the functions F_h, F_l, F_d, F_c and F_r respectively.

$\Delta F(s, t)$ represents the increment in function F due to interchange of components E_s and E_t in the placement matrix.

$$\begin{aligned} \Delta F(s, t) = & n_h \Delta F_h(s, t) + n_l \Delta F_l(s, t) + n_d \Delta F_d(s, t) \\ & + n_c \Delta F_c(s, t) + n_r \Delta F_r(s, t) \end{aligned} \quad (2.4.2.3)$$

Calculation of number of holes (F_h)

For X-Y coordinate wiring, the number of holes which are formed from wires connecting $E_s(j, k)$, to the row $t (t \neq j)$ is given by.

$$HR(s) = \sum_{t=1}^a (g_{st} - c_s, p_{tk}) - g_{sj} \quad s=1, 2, \dots, N$$

Then, total number of holes to minimize becomes

$$F_h = \frac{1}{2} \sum_{s=1}^N HR(s) \quad (2.3.2.4)$$

Theorem 1 When $E_s(j, k)$ and $E_t(l, m)$ are interchanged in the matrix P , the elements which change in matrix $[G:H]$ are $g_{ij}, h_{ik}, g_{il}, h_{im}, [i=1, 2, \dots, N]$. Their modified values become

$$\begin{array}{l} g'_{ij} = g_{ij} + A \\ h'_{ik} = h_{ik} + A' \\ g'_{il} = g_{il} - A \\ h'_{im} = h_{im} - A' \end{array} \quad (2.4.2.5)$$

$$\text{where } A = \begin{cases} c_{it}^{-c_{is}} & , \text{ if } j-\ell \neq 0 \\ 0 & , \text{ if } \ell-j = 0 \end{cases}$$

$$A' = \begin{cases} c_{it}^{-c_{is}} & , \text{ if } k-m \neq 0 \\ 0 & , \text{ if } k-m = 0 \end{cases}$$

Theorem 2 When $E_s(j,k)$, $E_t(\ell,m)$ are interchanged, the increment in wiring function F_h is given by

$$\Delta R_h(s,t) = g_{sj} + h_{sk} - (g_{st} + h_{sm} - Z c_{st}) + g_{t\ell} + h_{tm} - (g_{tj} + h_{tk} - Z c_{ts})$$

(2.4.2.6)

$$s=1,2,\dots,N, \quad t=s+1, s+2,\dots,ab$$

where,

$$Z = \begin{cases} 1, & \text{if } (j-\ell)(k-m) = 0 \\ 2, & \text{otherwise} \end{cases}$$

Theorem 3 When $E_s(j,k)$ and $E_t(\ell,m)$ are inter changed at iteration $(i-1)$, $\Delta F_h^i(u,v)$ is given by

$$\Delta F_h^i(u,v) = \begin{cases} \Delta F_h^{i-1}(u,v) & \text{if } n,q \neq j,\ell \text{ and } p,r \neq k,m \\ \Delta F_h^{i-1}(u,v) + (c_{ut} - c_{us} - c_{vt} + c_{vs})(x_1 - x_2 + x_3 - x_4), & \\ \text{otherwise} & \end{cases}$$

(2.4.2.7)

$$u = 1,2,\dots,N; \quad u \neq s,t$$

$$v = u+1, u+2,\dots, ab, \quad v \neq s,t$$

where E_u , E_v are occupying position (n,p) and (q,r) respectively

$$x_1 = \begin{cases} 1, & \text{if } n=j \\ -1, & \text{if } n=\ell \\ 0, & \text{otherwise} \end{cases}$$

$$x_2 = \begin{cases} 1, & \text{if } q=j \\ -1, & \text{if } q=\ell \\ 0, & \text{otherwise} \end{cases}$$

$$x_3 = \begin{cases} 1, & \text{if } p=k \\ -1, & \text{if } p=m \\ 0, & \text{otherwise} \end{cases}$$

$$x_4 = \begin{cases} 1, & \text{if } r=k \\ -1, & \text{if } r=m \\ 0, & \text{otherwise} \end{cases}$$

Calculation of length of etches (E_{λ})

Symmetrical matrix M of the order ab X ab can be determined as

$$m_{ij} = \ell_c |k-p| + w_c |\ell - q| \quad \text{Manhattan (rectilinear) distance between components } E_i(k, \ell) \text{ and } E_j(p, q) \quad (2.4.2.8)$$

The total routing length is equal to

$$\frac{1}{2} \sum_{i=1}^N \sum_{k=1}^N c_{ik} m_{ki} \quad (2.4.2.9)$$

Total rectilinear weighted wiring length can also be determined from matrix [G:H]. Number of interconnection leads passing through ith horizontal and ith vertical sections are

$$W_{h_i} = \sum_{k=i+1}^a \sum_{j \in Q_i} g_{jk}, \quad i=1,2,\dots,a-1 \quad (2.4.2.10)$$

$$W_{v_i} = \sum_{k=i+1}^b \sum_{j \in S_i} h_{jk}, \quad i=1,2,\dots,b-1 \quad (2.4.2.11)$$

where

Q_i is the set of components excluding fictitious components placed in rows 1,2,...,i.

S_i is the set of components excluding fictitious components placed in columns 1,2,...,i.

L_x and L_y are the total wiring length parallel to X-axis and Y-axis respectively, then total rectilinear wiring length is given by,

$$F_{\lambda} = L_x + L_y = w_c \sum_{i=1}^{a-1} w_{h_i} + \ell_c \sum_{j=1}^{b-1} w_{v_j} \quad (2.4.2.12)$$

Theorem 4 When components $E_s(j,k)$ and $E_t(\lambda,m)$ are interchanged, the increments $\Delta W_{h_i}(s,t)$ and $\Delta W_{v_i}(s,t)$ in w_{h_i} and w_{v_i} respectively are given by

$$\Delta W_{h_i}(s,t) = \begin{cases} K_1 \left[\sum_{p=1}^i (g_{sp} - g_{tp}) + \sum_{q=i+1}^a (g_{tq} - g_{sq}) \right] + 2c_{st}, & \text{if } \forall i \in I_1 \\ 0 & \text{otherwise} \end{cases} \quad (2.4.2.13)$$

$i=1,2,\dots,a-1.$

and

$$\Delta W_{v_i}(s,t) = \begin{cases} K_2 \left[\sum_{p=1}^i (h_{sp} - h_{tp}) + \sum_{q=i+1}^b (h_{tq} - h_{sq}) \right] + 2c_{st}, & \text{if } \forall i \in I_2 \\ 0, & \text{otherwise} \end{cases} \quad (2.4.2.14)$$

$i=1,2,\dots,b-1$

where

$$s=1,2,\dots,N \text{ and } t=s+1, s+2,\dots,ab$$

$$I_1 = [\min(j,\lambda), \min(j,\lambda)+1, \dots, \max(j,\lambda)-1]$$

$$I_2 = [\min(k,m), \dots, \max(k,m)-1]$$

$$K_1 = \begin{cases} 1, & \text{if } \lambda > j \\ -1, & \text{if } \lambda < j \\ 0, & \text{if } m=j \end{cases}$$

$$K_2 = \begin{cases} 1, & \text{if } m > k \\ -1, & \text{if } m < k \\ 0, & \text{if } m = k \end{cases}$$

With the help of this theorem $\Delta F_{\lambda}(s,t)$ can be written as

$$\Delta F_{\lambda}(s,t) = w_c \sum_{i \in I_1} \Delta W_{h_i}(s,t) + \ell_c \sum_{j \in I_2} \Delta W_{v_j}(s,t) \quad (2.4.2.15)$$

$s=1,2,\dots,N$
 $t=s+1, s+2, \dots, ab$

Theorem 5

If components $E_s(j,k)$ and $E_t(\ell,m)$ are interchanged in placement matrix P at iteration $(y-1)$, the values of $\Delta W_{h_i}^y(u,v)$ and $\Delta W_{v_i}^y(u,v)$ in terms of $\Delta W_{h_i}^{y-1}(u,v)$ and $\Delta W_{v_i}^{t-1}(u,v)$ can be given by

$$\Delta W_{h_i}^y(u,v) = \begin{cases} \Delta W_{h_i}^{y-1}(u,v) + 2K_1 B_1 (c_{ut} - c_{us} + c_{vs} - c_{vt}), & \text{if } i \in I_3 \\ \Delta W_{h_i}^{y-1}(u,v), & \text{otherwise} \end{cases} \quad (2.4.2.16)$$

$i=1,2,\dots,a-1$

and

$$\Delta W_{v_i}^y(u,v) = \begin{cases} \Delta W_{v_i}^{(y-1)}(u,v) + 2K_2 (c_{ut} - c_{us} + c_{vs} - c_{vt}) B_2, & \text{if } i \in I_4 \\ \Delta W_{v_i}^{(y-1)}(u,v), & \text{otherwise} \end{cases} \quad (2.4.2.17)$$

where

$$u=1,2,\dots,N, v=u+1, u+2,\dots,ab$$

$$v, u \neq s, t$$

$$I_3 = [\max[\min(j,\ell), \min(n,q)], \dots, \min[\max(j,\ell), \max(n,q)]]$$

$$I_4 = [\max[\min(k,m), \min(p,r)], \dots, \min[\max(k,m), \max(p,r)]]$$

$$1, \text{ if } \ell > j$$

$$1, \text{ if } m > k$$

$$B_1 = \{-1, \text{ if } \ell < j$$

$$, B_2 = \{-1, \text{ if } m < k$$

$$0, \text{ if } \ell = j$$

$$0, \text{ if } m = k$$

E_u and E_v are occupying the positions (n,p) and (q,r) respectively.

From theorems 4 and 5

$$\Delta F_{\ell}^y(u,v) = \Delta F_{\ell}^{y-1}(u,v) + (c_{ut} - c_{us} + c_{vs} - c_{vt}) (2K_1 B_1 w_c |I_3| + 2K_2 B_2 \ell_c |I_4|) \quad (2.4.2.18)$$

$$u=1,2,\dots,N, v=(u+1),\dots,ab$$

$$u,v \neq s,t$$

where, $|X|$ is the number of elements in the set X.

Calculation of interconnection densities (F_d)

Wiring function (F_d) is taken as weighted average interconnection density on the board.

$$F_d = \frac{1.0}{\ell_b(a-1) + w_b(b-1)} \left[\sum_{i=1}^{a-1} \beta_{h_i} W_{h_i} + \sum_{j=1}^{b-1} \beta_{v_j} W_{v_j} \right] \quad (2.4.2.19)$$

for even distribution of etches in horizontal and vertical sections of the board, $\beta_{h_i} = W_{h_i}$, $[i=1,2,\dots,a-1]$ and

$$\beta_{v_j} = W_{v_j} [j=1,2,\dots,b-1]$$

$$\Delta F_d(s,t) = \frac{1.0}{\ell_b(a-1) + w_b(b-1)} \left[\sum_{i=1}^{a-1} \beta_{h_i} \Delta W_{h_i}(s,t) + \sum_{j=1}^{b-1} \beta_{v_j} \Delta W_{v_j}(s,t) \right] \quad (2.4.2.20)$$

$$s=1,2,\dots,N, t=s+1, s+2,\dots,ab$$

If the components $E_s(j,k)$ and $E_t(l,m)$ are interchanged at iteration $(i-1)$, the value of $\Delta F_d^i(u,v)$ in terms of $\Delta F_d^{i-1}(u,v)$ is given by

$$\Delta F_d^i(u,v) = \Delta F_d^{i-1}(u,v) + (c_{ut} - c_{us} + c_{vs} - c_{vt}) \left[\frac{K_1 B_1 \sum_{n \in I_3} \beta_{h_n} + K_2 B_2 \sum_{n \in I_4} \beta_{v_n}}{\ell_b(a-1) + w_b(b-1)} \right] \quad (2.4.2.21)$$

$$u=1,2,\dots,N, v=(u+1), (u+2), \dots, ab, u,v \neq s,t.$$

Calculation of Stray Capacitance (F_c)

In X-Y coordinate wiring, total stray capacitance in the circuit will be minimized by minimizing.

$$w_c \sum_{i=1}^{a-1} W_{h_i} w_{hi} + \lambda_c \sum_{j=1}^{b-1} W_{V_j} w_{V_j}$$

or,

$$\min F_c = \frac{w_c}{\lambda_b} \sum_{i=1}^{a-1} W_{h_i}^2 + \frac{\lambda_c}{w_b} \sum_{j=1}^{b-1} W_{V_j}^2 \quad (2.4.2.22)$$

$$\begin{aligned} \Delta F_c(s, t) = & \frac{w_c}{\lambda_b} \sum_{i=1}^{a-1} [2 \cdot W_{h_i} \Delta W_{h_i}(s, t) + [\Delta W_{h_i}(s, t)]^2] \\ & + \frac{\lambda_c}{w_b} \sum_{j=1}^{b-1} [2 \cdot W_{V_j} \Delta W_{V_j}(s, t) + [\Delta W_{V_j}(s, t)]^2] \end{aligned} \quad (2.4.2.23)$$

$$s=1, 2, \dots, N, \quad t=s+1, s+2, \dots, ab$$

Calculation of temperature function (F_r)

The failure rate of semiconductor devices is defined via an Arrhenius relation

$$\lambda(T) = \lambda(T_a) \exp[(T_a^{-1} - T^{-1}) e_a/k] \quad (2.4.2.24)$$

Components E_i and E_j are placed in slots having coordinates (k, λ) and (p, q) respectively. The distance between components

E_i and E_j is

$$m_{ij} = [\lambda_c^2 (k-p)^2 + w_c^2 (\lambda-q)^2]^{1/2} \quad (2.4.2.25)$$

The temperature function F_r is written as

$$F_r = \sum_{i=1}^N \sum_{j=1}^N R_{ie} R_{je} W_j \gamma_i / R_{ij} \quad (2.4.2.26)$$

where,

$$\gamma_i = (R_{ie} \cdot W_i)^n, \quad 0.5 \leq n \leq 2. \text{ value of } n \text{ decided from experience.}$$

$$R_{ij} = r_{ij} (m_{ij})^n, \quad 0.4 \leq n \leq 2.5$$

Value of n depends upon the thermal conductivity and dimensions of the board, and heat transfer coefficient of the surface of circuit board.

Theorem 6

When E_s and E_t are interchanged in the matrix P, the only elements which change in matrix M are m_{si} , m_{ti} , m_{is} and m_{it} , $[i=1,2,\dots,ab]$. These modified entries will be

$$\left. \begin{aligned} m_{ts} &= m'_{st} = m_{st} \\ m'_{it} &= m'_{ti} = m_{si} \\ m'_{si} &= m'_{is} = m_{ti} \end{aligned} \right\} \quad i=1,2,\dots,ab \quad (2.4.2.27)$$

Theorem 7

When components E_s and E_t are interchanged in matrix P, the change in function F_r will be equal to

$$\Delta F_r(s,t) = \begin{cases} \sum_{\substack{i=1 \\ \neq s \\ \neq t}}^N \{f^{-1}(m_{it}) - f^{-1}(m_{is})\} \{ \gamma_i(K_{is} - K_{it}) + \gamma_s K_{si} - \gamma_t K_{ti} \}, & \text{if } t \leq N. \\ \sum_{\substack{i=1 \\ \neq s}}^N \{ (f^{-1}(m_{it}) - f^{-1}(m_{is})) \} \{ \gamma_i K_{is} + \gamma_s K_{si} \}, & \text{if } t > N \end{cases} \quad (2.4.2.28)$$

$$s=1,2,\dots,N, \quad t=(s+1), (s+2), \dots, NT$$

$$f(m_{ij}) = (m_{ij})^n, \quad 0.4 \leq n \leq 2.5$$

Theorem 8

If components E_s and E_t have been interchanged in iteration i, the value of $\Delta F_r^{i+1}(u,v)$ in terms of $\Delta F_r^i(u,v)$ is given by

$$\Delta F_r^{i+1}(u,v) = \Delta F_r^i(u,v) + (J_s - J_t) [f^{-1}(m_{tv}^i) - f^{-1}(m_{tu}^i) - f^{-1}(m_{sv}^i) + f^{-1}(m_{su}^i)]$$

$$u=1,2,\dots,N, \quad v=(u+1), (u+2), \dots, NT \quad (2.4.2.29)$$

$$\neq s, t \quad \neq s, t$$

where,

$$J_s = \gamma_s K_{su} + \gamma_u K_{us} - \delta_1 (\gamma_s K_{sv} + \gamma_v K_{vs})$$

$$J_t = 2[\gamma_t K_{tu} + \gamma_u K_{ut} - \delta_2 (\gamma_t K_{tv} + \gamma_v K_{vt})]$$

$$\delta_1 = \begin{cases} 1, & \text{if } v \leq N \\ 0, & \text{otherwise} \end{cases}$$

$$\delta_2 = \begin{cases} 1, & \text{if } t \leq N \\ 0, & \text{otherwise} \end{cases}$$

Algorithm

- (i) Calculate matrix [G.H] using (2.4.2.1), calculate functions F_h^i , F_λ^i , F_d^i , F_c^i and F_r^i by equations (2.4.2.4), (2.4.2.12), (2.4.2.19), (2.4.2.22) and (2.4.2.26) respectively, set $i=1$.
- (ii) Calculate multi criteria function $F^i = n_h F_h^i + n_\lambda F_\lambda^i + n_c F_c^i + n_d F_d^i + n_r F_r^i$ by equation (2.4.2.2).
- (iii) Set $s \leftarrow 0$
- (iv) $s \leftarrow s+1$
- (v) Set $t = s+1$
- (vi) If $(s \leq a \text{ and } t > a)$ or $(s > a \text{ and } t \leq a)$ go to step (xiii)
- (vii) Calculate $\Delta F_h^i(s, t)$, $\Delta F_\lambda^i(s, t)$, $\Delta F_d^i(s, t)$, $\Delta F_c^i(s, t)$, $\Delta F_r^i(s, t)$ if $i=1$ by equations (2.4.2.6), (2.4.2.15), (2.4.2.20), (2.4.2.23), (2.4.2.28) and for $i > 1$ by equations (2.4.2.7), (2.4.2.18), (2.4.2.21), (2.4.2.23) and (2.4.2.29) respectively.
- (viii) Calculate $\Delta F^i(s, t)$ by equation (2.4.2.3).

- (ix) If $\Delta F^i(s, t)$ is not negative goto step (xiii).
- (x) Find the matrix P^i after interchanging components E_s and E_t .
- (xi) Set $i = i+1$ and calculate F^i .
- (xii) Calculate $(G:H)^i$ with the help of equation (2.4.2.5) and matrix M^i with the help of equation (2.4.2.27) and goto step (iii).
- (xiii) Set $t = t+1$.
- (xiv) If t is not greater than NT go to step (vi)
- (xv) If s is less than N go to step (iv).
- (xvi) Stop

2.4.2.2 Components of different sizes

One of the assumptions while stating the placement problem is that the components are of two different sizes. Dimensions of first type being such that each component requires one and only one slot on the printed circuit board, and the second type of components are double the size of the first type. In other words, a double sized component requires two adjacent slots for its placement. The double sized component, for solving the placement problem are treated as two distinct components with very high connectivity between them. After performing the iterative improvement algorithm with all the components treated as occupying one slot, irrespective of the initial placement, it has been observed that the two components which correspond to a double sized component come closer and are placed in adjacent slots, because of the

high connectivity between them. But the position of the slots occupied by the two components depend largely on the initial placement. Once the two components have come close in the adjacent slots during the iterative procedure it is not possible to move the two components to any other slot to improve the objective function, unless the pair is moved together. That is, the position of the pair of components corresponding to double sized components are inter changed with another pair of components placed in some other slots.

The two slots occupied by the pair corresponding to the double sized components may be adjacent in either the same row or in the same column. So this phase of iterative improvement procedure is carried out in two stages. In the first stage all the possible pairs of components in a column can be interchanged with another pair of adjacent components in a column. For different combinations of two pairs that can be inter changed the objective function value is calculated using the equation (2.4.2.2). The pairs are interchanged if there is any improvement in the value of total objective function. For this stage the various combinations possible are-

$(p_{i_1, j_1}), (p_{i_2, j_2})$ interchanged with $(p_{k_1, l_1}), (p_{k_2, l_2})$

for all

$$i_2 = 2, a$$

$$i_1 = i_2 - 1$$

$$j_1 = j_2 = 1, b-1$$

for all

$$\left[\begin{array}{l} k_1 = i_1 \\ k_2 = i_2 \\ l_1 = l_2 = j_1 + 1, b-1 \end{array} \right]$$

, if $j_1 < b-1$

and

$$\left[\begin{array}{l} k_2 = i_2 + 1, a \\ k_1 = k_2 - 1 \\ l_1 = l_2 = 1, b-1 \end{array} \right]$$

, if $i_2 < a$

The second stage is similar to the first stage except the possible pairs of components in a row are interchanged with another pair of adjacent components in a row, i.e.

$(p_{i_1, j_1}), (p_{i_2, j_2})$ can be interchanged with any of

$(p_{k_1, l_1}), (p_{k_2, l_2})$

where

where,

$$j_2 = 2, b-1$$

$$l_1 = j_1$$

$$j_1 = j_2 - 1$$

$$l_2 = j_2, \text{ if } i_1 < a$$

$$i_1 = i_2 = 1, a$$

$$k_1 = k_2 = i_1 + 1, a$$

and

$$l_2 = j_2 + 1, b-1$$

$$l_1 = l_2 - 1, \text{ if } j_2 < b-1$$

$$k_1 = k_2 = 1, a$$

Example 2.2

Consider a circuit containing 14 components. The components are to be placed on the printed circuit board of size 15 X 23 cms. As many as 36 components can be placed on the board. The board is divided into 6 horizontal and 6 vertical divisions. In all 20 components (14 plus 6 corresponding to the edge connector) are to be placed on this board. Thermal resistances of all the components are 400°C/W . Failure rate of each component at 100°C (junction temperature) is 0.025 per 1000 hrs. Ambient temperature is 27°C . The power dissipation of each component is given in Table 2.1. Thermal resistance (R_{ij}) due to thermal coupling between two components E_i and E_j

is assumed to be $5000 m_{ij}$, where m_{ij} is in cms, and $\gamma_i = R_{ie} W_i [i=1,2,\dots,20]$. The values of weightages for different functions are taken as

$$n_h=1, n_f=0.05, n_d=20.0, n_c=0.015, n_r=0.015$$

Non zero elements of connection matrix C are $c_{2,1}=1$,
 $c_{3,1}=1, c_{4,1}=1, c_{6,2}=2, c_{7,2}=1, c_{8,2}=2, c_{6,3}=2, c_{7,3}=3$,
 $c_{8,3}=2, c_{5,4}=1, c_{9,5}=1, c_{10,5}=4, c_{11,5}=3, c_{9,6}=2, c_{9,7}=100$,
 $c_{10,7}=1, c_{11,8}=5, c_{12,9}=3, c_{3,10}=3, c_{14,11}=4, c_{15,12}=3$,
 $c_{20,12}=100, c_{16,13}=4, c_{17,14}=100, c_{18,15}=1, c_{19,16}=5$,
 $c_{20,17}=6$

Table 2.1

Power dissipation of components of example 2.2

Component	1	2	3	4	5	6	7	8	9	10
Power dissipation in mw	-	-	-	-	-	-	160	170	180	80
Component	11	12	13	14	15	16	17	18	19	20
Power dissipation in mw	85	120	130	140	150	160	170	60	80	130

Initial placement obtained by the constructive algorithm.

$$P = \begin{bmatrix} 0 & 19 & 16 & 13 & 10 & 5 \\ 7 & 9 & 0 & 8 & 11 & 2 \\ 15 & 12 & 20 & 17 & 14 & 6 \\ 18 & 0 & 0 & 0 & 0 & 3 \\ 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 4 \end{bmatrix}$$

Placement obtained by iteratively interchanging two individual components at a time (stage one) in 22 iterations

$$P = \begin{bmatrix} 13 & 7 & 16 & 19 & 8 & 3 \\ 10 & 9 & 12 & 0 & 11 & 5 \\ 0 & 0 & 20 & 0 & 17 & 6 \\ 0 & 0 & 0 & 0 & 14 & 2 \\ 0 & 0 & 0 & 0 & 0 & 1 \\ 18 & 0 & 15 & 0 & 0 & 4 \end{bmatrix}$$

After iteratively interchanging a pair of components in same column with another pair of components in same column (stage two), the placement after two iterations is

$$P = \begin{bmatrix} 7 & 19 & 16 & 13 & 8 & 3 \\ 9 & 0 & 12 & 10 & 11 & 5 \\ 0 & 0 & 20 & 0 & 17 & 6 \\ 0 & 0 & 0 & 0 & 14 & 2 \\ 0 & 0 & 0 & 0 & 0 & 1 \\ 18 & 0 & 15 & 0 & 0 & 4 \end{bmatrix}$$

There is no further improvement by interchanging a pair of component in same row with another pair in same row (stage three).

The function values at the end of each stage is compiled in Table 2.2.

Table 2.2

Results of example 2.2

	Number of Iterations	Number of Holes	Avg. Wiring Density (ET/CM)	Total Wiring Length (CM)	Capacitance Factor	Mean Temperature (°C)	Failure Rate (per 1000 hrs)	Total Value of Function
Constructive Placement	-	12	2.68	1542.67	10141.00	44.34	0.238	395.60
Stage one	22	6	2.12	1215.67	4717.50	43.65	0.211	266.90
Stage two	2	6	2.09	1204.33	4669.46	43.61	0.197	262.66
Stage three	0	6	2.09	1204.33	4669.46	43.61	0.197	262.66

CHAPTER - 3

MULTILAYER PRINTED CIRCUIT BOARD

3.1 Introduction

The sophisticated Integrated Circuit technology has facilitated the fabrication of complex circuits within small chips. For designing complex large scale electronic systems using these semiconductor chips as basic building blocks, multilayer printed circuit (MPC) boards are used as a medium for interconnecting these blocks. The components are mounted on top of the MPC board with terminals inserted in the drilled through holes called Pins. The blocks are interconnected by means of printed wires on different layers. Plated through holes called Vias, are used for inter layer connections, in order to connect wires on different layers. Determination of via locations and physical routes of printed wires for making the interconnections of the circuit constitute a MPC routing problem.

The routing of MPC boards is restricted by some physical constraints namely the size of the multilayer board, the feasible number of layers, the minimum width of conductor path and the necessary separation between two adjacent parallel conductor paths. The basic assumptions as proposed by Ting et.al [14] for solving MPC routing problem are:

1. The geometrics of the pins and vias are at fixed locations.
Vias appear only columnwise.

2. Only points (pins and/or vias) on the same line can be connected directly and the physical routes must be confined within the channels on both sides of the line.
3. Connections for holes in a column are on one layer and for points (pins or vias) in a row are in other layers.

The problem of interconnection of circuit on different layers can be divided into three interrelated phases [15]. First to decompose the whole interconnection into the portions of each layer, second assignment of vias for each net. and finally laying out the wire patterns on each layer. Many algorithms have been developed [3,6,8,16] for solving single row (or unidirectional) routing problem. Based on the assumptions made above, the multilayer routing problem can be reduced to several single line routing problems [14]. From a general multilayer problem, several single line single layer routing problems can be obtained by following three basic steps, firstly assigning vias to form connections with pins on the board, secondly assignment of connection patterns to various layers, and finally realization of all the connections on the basis of single line, single layer problems.

While assigning vias to form connections with pins two main objectives are to be kept in mind [14], minimization of via usage and the minimization of via columns. Each additional via reduces the reliability of the circuit and via column adds to the size of the board and if the board size is kept constant, the area available for routing is reduced.

In this chapter the problem of component placement on multilayer printed circuit boards is discussed. The via assignment problem has also been described in detail. The formulation of optimization problem has been dealt with and then a refined heuristic algorithm is developed.

3.2 Component Placement on MPC Boards

For solving the problem of MPC board routing the first assumption is that, the geometries of the pins are at fixed locations, which means that the pin locations have to be decided prior to solving the actual routing problem. In other words the component placement has to be fixed based on some optimization criteria. For the component placement on multilayer circuit boards also the same set of criteria are used as for the double layer PCBs (chapter-2). The criteria used for optimizing the component placement on MPC boards also is, a combination of length of etches, Inter-connection density, Stray capacitance, effect of thermal coupling between components, and total number of holes. But the method of calculating the number of holes required for realizing a circuit on multilayer PCB is different from what it is for double layer PCBs. Since the need of multilayer PCBs arose from the development of components in DIP packages it is assumed that the pins of each components are in two horizontal rows.

From the definition of the matrix A it is evident that the non zero entries in a column of A represent that pins belonging to the net corresponding to the column are present

in a row. Further if the pin belonging to a net are present in more than one row vias are required for its realization. So the total number of vias required for the realization of the whole circuit is calculated by counting the total number of vias needed for realizing each net. That is if a column of A has more than one non-zero entries then that number of holes are required for the realization of the corresponding net. So the total number of holes to be minimized becomes

$$F_h = \sum_{\substack{j=1, NN \\ i=1, NR}} a_{ij} \quad \text{if} \quad \sum_{k=1}^{NR} a_{kj} \geq 2$$

During the iterative procedure for finding the best component placement it is required to find the A matrix for each iteration. To avoid the calculation of whole of the A matrix the following approach can be used to modify the matrix A and hence save the computation time.

When $E_s(j, n)$ and $E_t(\ell, m)$ are inter changed in the matrix P then the matrix A can be modified as follows.

no change if $j = \ell$

otherwise,

$$a_{(2j-1), L(2s-1), k} \Big|_{k=1, NP} = 0, \text{ if } L(2s-1), k \neq L(2xP_j, o-1), p$$

$$\Big| \begin{array}{l} p=1, NP \\ o=1, b \\ o \neq n \end{array}$$

= 1, otherwise.

$$a_{2j, L_{2s, k} |_{k=1, NP}} = 0, \text{ if } L_{2s, k} \neq L(2xP_{j, o}), p \begin{cases} p=1, NP \\ o=1, b \\ o \neq n \end{cases} \\ = 1, \text{ otherwise}$$

$$a_{(2j-1), L(2s-1), k |_{k=1, NP}} = 1$$

$$a_{2j, L_{2s, k} |_{k=1, NP}} = 1$$

$$a_{(2j-1), L(2t-1), k |_{k=1, NP}} = 0, \text{ if } L(2t-1), k \neq L(2xP_{j, o-1}), p \begin{cases} p=1, NP \\ o=1, b \\ o \neq m \end{cases} \\ = 1, \text{ otherwise}$$

$$a_{2j, L_{2t, k} |_{k=1, NP}} = 0, \text{ if } L_{2t, k} \neq L(2xP_{j, o}), p \begin{cases} p=1, NP \\ o=1, b \\ o \neq m \end{cases} \\ = 1, \text{ otherwise}$$

$$a_{(2s-1), L(2t-1), k |_{k=1, NP}} = 1$$

$$a_{2s, L_{2t, k} |_{k=1, NP}} = 1$$

The nets associated with the components going out of the row are compared with other pins of the same row. If another pin in the row is belonging to the same net then the element of A corresponding to the row and the net is not changed other wise it is made zero. And the element of A corresponding to the row to which the component is entering and the corresponding nets is made equal to one.

3.3 The via Assignment Problem

For a circuit, one possible realization on a multi-layer board is done by drawing the conductor paths connecting vias in the same column on one layer. Interconnections between pins and vias in the same row are drawn on the other

layers. This scheme of connecting pins or vias in the same row or column is termed as the single row single layer routing. This can be conducted only after determination of via assignment for each net.

If vias are assigned in a slightly different way, a totally different realization of the circuit on the board is obtained. Thus increase or decrease in the number of via columns is achieved by assigning vias to the nets differently. Hence it is very important to assign the vias for each net under the criteria that the number of via columns is reduced as much as possible.

In a circuit if there is a net with all the pins placed in the same row, then no vias are required for the interconnection of this net. So it is assumed that for the via assignment problem the circuit does not contain any such net.

For a given net list $L = \{N_1, N_2, \dots, N_n\}$ of n nets. Matrix A is defined as $A = [a_{ij}] = [\bar{a}_1, \bar{a}_2, \bar{a}_3 \dots \bar{a}_n]$ where each column \bar{a}_j corresponds to a net N_j of the net list such that

$$a_{ij} = \begin{cases} 1, & \text{if net } N_j \text{ contains a pin in row } i \\ 0, & \text{if net } N_j \text{ does not contain a pin in row } i \end{cases}$$

It is not possible to connect two pins of a net, if they are placed in different rows by laying the connecting path on one layer when single-row single-layer routing is used.

If there is a nonzero entry in the i th row of the column a_j of the matrix A , that is $a_{ij}=1$ then at least one via in the i th row is required for interconnecting the net N_j , corresponding to the column \bar{a}_j . Hence it is deduced that the minimum number of via columns necessary for realizing a given net list L , if q is the maximum number of ones in a row of A , is q .

If the rows i_1, i_2, \dots, i_k of the column \bar{a}_j have non zero elements, vias are assigned in the rows i_1, i_2, \dots, i_k , for the net N_j , in the same via column, then all these vias are connected by single row single layer routing. Hence, if the number of columns of A is equal to n then maximum number of via columns that are sufficient for the realization of all the nets, is n .

3.3.1 Column Merging

Consider there are non zero elements in distinct rows of the columns \bar{a}_j and \bar{a}_ℓ or in other words the scalar product of the columns \bar{a}_j and \bar{a}_ℓ is equal to zero i.e. $(\bar{a}_j, \bar{a}_\ell) \triangleq \sum_k a_{kj} a_{k\ell} = 0$. The matching, M , is defined as the total number of nonzero elements in the two columns \bar{a}_j and \bar{a}_ℓ . Vias in the same via column are assigned for nets N_j and N_ℓ corresponding to \bar{a}_j and \bar{a}_ℓ respectively. Thus if $(\bar{a}_j, \bar{a}_\ell) = 0$ for two columns \bar{a}_j and \bar{a}_ℓ in A , then vias in the same via column are assigned for the corresponding nets N_j and N_ℓ .

The vias for any net are chosen from one single via column, but a via column may contain vias for more than one net. Hence the problem of assigning vias for each net with the minimum number of via columns may be stated as [15].

For a given 0-1 matrix $A = [\bar{a}_1, \bar{a}_2, \dots, \bar{a}_n]$ minimize the number of columns in the matrix A by repeated application of the column merging process to A.

Column Merging - For a pair of columns \bar{a}_i and \bar{a}_j such that $(\bar{a}_i, \bar{a}_j) = 0$, merge \bar{a}_i and \bar{a}_j into a new column $\bar{a}_{ij} = \bar{a}_i + \bar{a}_j$. Delete \bar{a}_i and \bar{a}_j from the matrix A and add column \bar{a}_{ij} to it.

After repeated application of column merging process on A, till no further merging is possible, the number of columns in the reduced A matrix is the upper bound on the number of via columns which have to be used for the assignment of vias for each net.

3.3.2 Column Decomposition

The vias for a net are alternatively chosen from $p (\geq 2)$ different via columns also. Consider a column \bar{a}_j of A corresponding to the net N_j having ones in rows i_1, i_2, \dots, i_k . Denote $I \triangleq \{i_1, i_2, \dots, i_k\}$, and decompose I into I_1 and I_2 such that $I_1 \cup I_2 = I$ and $I_1 \cap I_2$ has exactly one row i_a . Then for net N_j the vias in rows of I_1 in one via column j_1 and those in rows of I_2 in another via column j_2 , such that two different parts of routing for N_j , one in via column j_1 and other in via column j_2 are finally connected by means of two vias in row i_a . A different way for the assignment of

vias in two different via columns for net N_j is to decompose I into two disjoint subsets J_1 and J_2 and then by adding some row $i_p \in I$ to J_1 and J_2 , respectively for getting two sets I_1 and I_2 . Then vias for N_j can be assigned in two via column j_1 and j_2 .

The process of column decomposition for a column \bar{a}_j of A is described as follows. The column \bar{a}_j is decomposed into \bar{a}_{j1} and \bar{a}_{j2} where \bar{a}_j has ones in rows of I and \bar{a}_{j1} and \bar{a}_{j2} have ones in the rows of I_1 and I_2 , respectively, such that $I \subset I_1 \cup I_2$ and $|I_1 \cap I_2| = 1$, respectively. Then each of such decomposed columns, \bar{a}_{j1} and \bar{a}_{j2} are merged with other columns to give single columns through the process of column merging.

Column Decomposition - For a proper integer $p(j)$, decompose a column a_j of A into $\bar{a}_{j1}, \bar{a}_{j2}, \dots, \bar{a}_{jp(j)}$ such that

- i) $\bar{a}_j \leq \bar{a}_{j1} + \bar{a}_{j2} + \dots + \bar{a}_{jp(j)}$
- ii) for any K ($2 \leq K \leq p(j)$), there exists a column \bar{a}_{jh} ($1 \leq h < k$) satisfying $(\bar{a}_{jk} \cdot \bar{a}_{jh}) = 1$, then replace \bar{a}_j by matrix $[\bar{a}_{j1} \bar{a}_{j2} \dots \bar{a}_{jp(j)}]$ composed of the $p(j)$ columns.

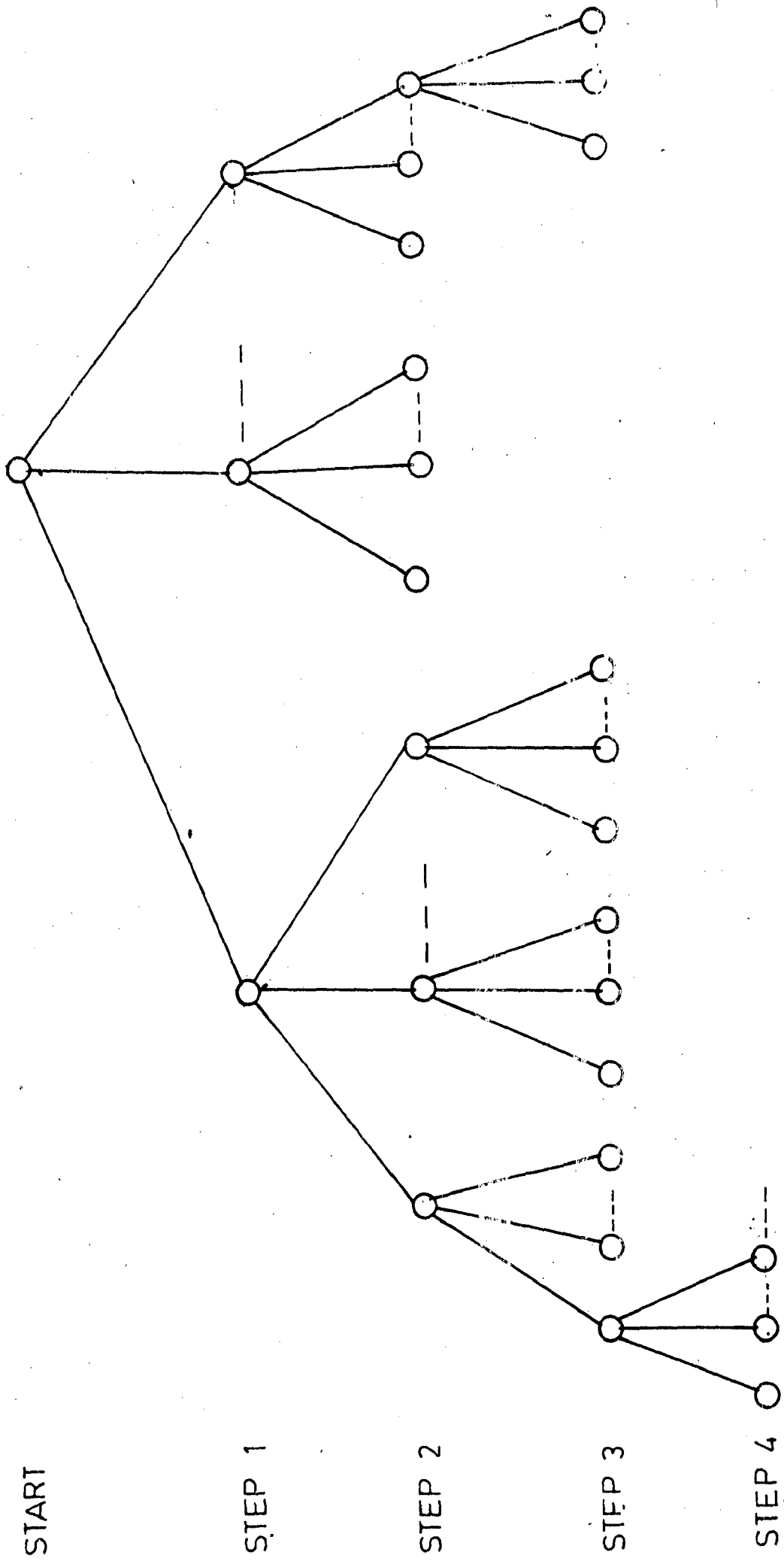
The replacement of \bar{a}_j by $[\bar{a}_{j1}, \bar{a}_{j2}, \dots, \bar{a}_{jp(j)}]$ indicates the decomposition of the net N_j into $p(j)$ subnets $N_{j1}, N_{j2}, \dots, N_{jp(j)}$, where each N_{jk} corresponds to \bar{a}_{jk} . These N_{jk} are realized in different via columns and are later interconnected by means of single row single layer routing.

With the introduction of the process of column merging and column decomposition the problem of minimization of via columns while assigning vias is stated as [15].

Given a 0-1 matrix $A = [\bar{a}_1 \bar{a}_2 \dots \bar{a}_n]$, by applying the process of column merging and column decomposition to A , minimize the number of columns in A .

3.4 Heuristic Algorithm

The proposed heuristic algorithm is split up into two different phases. The first phase constitutes the forming of undirected graphs for A such that each vertex corresponds to a column of A and each edge corresponds to a pair of columns \bar{a}_i and \bar{a}_j such that $(\bar{a}_i \cdot \bar{a}_j) = 0$. A sequence of column merging process is applied to the columns corresponding to the edges till no more column merging is possible. The resultant matrix A after this phase depends largely upon the starting pair of columns. The pair which leads to maximum matching, after all the steps of merging are carried out, is the best choice for the starting pair. Determination of the starting pair of columns for merging process is a complex and time consuming problem in itself. If all the options at each step, as shown in figure (3.1) are tried out the total number of combinations to be considered becomes exceptionally large if the total number of nets in the circuit is sufficiently big. To simplify the problem the matching in only first two steps is considered. In the second step the pairs are chosen on the basis of maximum matching, giving least preference to the merging that leaves only one zero in the resultant column.



○ Represents probable pairs of matched columns.

FIGURE 3.1 OPTIONS FOR MERGING AT EACH STEP.

Based on the maximum total matching in first two steps, the choice of the pair of columns is made. Once the starting pair of column are decided, the pairs corresponding to the maximum matching in two steps are merged and the graph is constructed afresh. This is continued till there are no edges in the constructed graph. The second phase is to decompose unmerged columns in the remaining matrix A, one at a time, such that each of the decomposed columns is then to be merged with a proper mate into a new column by the process of column merging.

3.4.1 Outline of the algorithm

Phase 1:

1. Find the matrix $A = [\bar{a}_1 \bar{a}_2 \dots \bar{a}_n]$, put $k = 1$
2. For each $V_j \in V$ corresponding to \bar{a}_j and $(V_i, V_j) \in E$ if and only if $(\bar{a}_i \cdot \bar{a}_j) = 0$, construct a unidirected graph $G = [V, E]$. Delete all the vertices that do not have any connection with any vertex from the graph and obtain the graph $G_k = [V_k, E_k]$.
3. If $E_k = \emptyset$ goto Phase 2.
4. Find the maximum matching $M = M_1 + M_2$ in two consecutive steps.
5. Delete \bar{a}_i and \bar{a}_j corresponding to $(V_i, V_j) \in M_1$ from the matrix A and add them to a column defined by $(\bar{a}_i + \bar{a}_j)$, and make this new column inadmissible.
6. Modify graph G_k , delete the vertices V_i and $V_j \in M$.
7. Find the maximum matching M_1 in the remaining graph giving least preference to the matching equal to $(NR-1)$.

8. Delete \bar{a}_k and \bar{a}_l corresponding to $(V_k, V_l) \in M1$ from the matrix A and add them to a column defined by $(\bar{a}_k + \bar{a}_l)$, make this column also inadmissible.
9. Goto Step 2, $k = k+1$.

Phase 2

1. Denote the solution matrix by A_0 and initialize it to zero.
2. Delete all the columns having less than or equal to one zero from A and add them to the solution matrix A_0 . If A satisfies any one of the following conditions then add all columns of A to the solution matrix A_0 and stop.
 - (i) There is a row in the matrix A which does not contain any zero.
 - (ii) Each one of the rows of the matrix A have exactly one zero.
 - (iii) There is no admissible column left.
3. Select a column \bar{a}_l in A which has the minimum number of ones among all the columns.
4. For this \bar{a}_l construct a graph $G=[X, Y; E]$ whose vertices are partitioned into two disjoint sets X and Y with the properties.
 - (i) no two vertices in X are adjacent in E and
 - (ii) no two vertices in Y are adjacent in E.such a graph is called a Bipartite graph [7]. The bipartite graph is constructed in the following way.

- (i) each $x_i \in X$ corresponds to row i of A such that $a_{i\ell} = 1$,
- (ii) each $y_j \in Y$ corresponds to column \bar{a}_j of A .
- (iii) $(x_i, y_j) \in E$ if and only if \bar{a}_j corresponding to $y_j \in Y$ has a zero in the i th row corresponding to $x_i \in X$.

If any one of the vertex of X is not contained in a connected component of G find the column \bar{a}_ℓ with next minimum number of ones and go to 4.

5. Find a tree $T = [X, Z; D]$ spanning X in $G = [X, Y; E]$ such that the sum of zeros in the columns corresponding to $y, \in Z$ is minimum among all the possible trees, that can be found from the bipartite graph G .
6. For each $(x_i, y_j) \in D$, $a_{ij} = 1$ and make \bar{a}_j corresponding to $y_j \in Z$ inadmissible, delete \bar{a}_ℓ from the matrix A .
7. Go to Step 2.

The tree constructed in phase 2 gives an information as to how the columns are to be decomposed and then merged with other columns. For each $y_j \in Z$, define a column vector

$$\bar{a}_\ell^{(j)}(i) = [a_{1\ell}^{(j)} \ a_{2\ell}^{(j)} \ \dots \ a_{r\ell}^{(j)}]^t \text{ such that}$$

$$a_{i\ell}^{(j)} = \begin{cases} 1, & \text{if } (x_j, y_j) \in D \\ 0, & \text{if } (x_i, y_i) \notin D. \end{cases}$$

then \bar{a}_ℓ can be decomposed in to all such $\bar{a}_\ell^{(j)}$ with $y_j \in Z$, by using the process of column decomposition. Each of the decomposed columns $\bar{a}_\ell^{(j)}$ are merged with the column \bar{a}_j using the process of column merging, giving a new column.

Example 3.1

For a circuit containing 9 nets, to be realized in 6 rows consider the matrix A to be

$$A = \begin{matrix} & \bar{a}_1 & \bar{a}_2 & \bar{a}_3 & \bar{a}_4 & \bar{a}_5 & \bar{a}_6 & \bar{a}_7 & \bar{a}_8 & \bar{a}_9 \\ \begin{matrix} 1 \\ 2 \\ 3 \\ 4 \\ 5 \\ 6 \end{matrix} & \left[\begin{array}{ccccccccc} l_1 & 0 & 0 & l_4 & 0 & l_6 & 0 & 0 & l_9 \\ 0 & l_2 & l_3 & l_4 & l_5 & 0 & 0 & l_8 & 0 \\ 0 & l_2 & l_3 & 0 & 0 & 0 & l_7 & 0 & l_9 \\ l_1 & 0 & 0 & l_4 & l_5 & l_6 & 0 & l_8 & 0 \\ l_1 & 0 & 0 & 0 & l_5 & 0 & l_7 & l_8 & l_9 \\ 0 & l_2 & 0 & l_4 & 0 & 0 & l_7 & 0 & 0 \end{array} \right. \end{matrix}$$

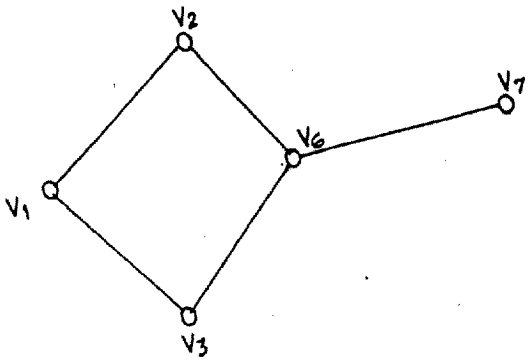
where the subscript of each one indicate the net number.

The problem is to minimize the number of columns by repeated processes of column merging and decomposition.

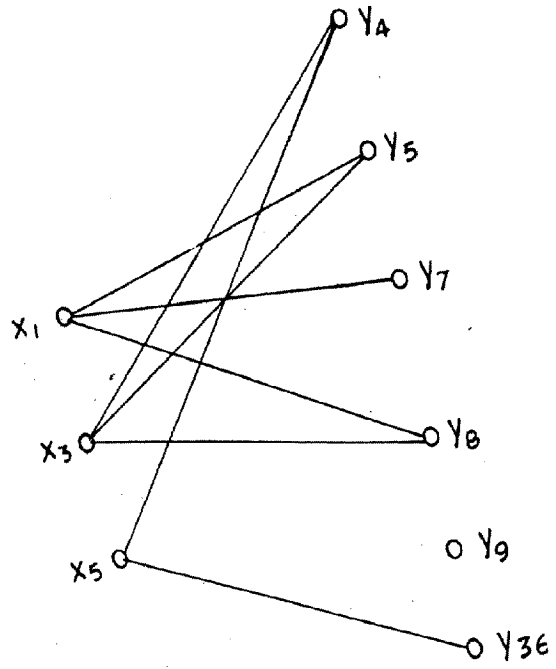
Phase 1-

1. G_1 is a graph with five vertices v_1, v_2, v_3, v_6 and v_7 as shown in figure 3.2(a).
2. Combinations for merging of pairs in first two steps are
 - i. $(v_6, v_7), (v_1, v_2)$, matching $M = M_1 + M_2 = 5 + 6 = 11$.
 - ii. $(v_3, v_6), (v_1, v_2)$, matching $M = M_1 + M_2 = 4 + 6 = 10$
 - iii. $(v_2, v_6), (v_7, v_3)$, matching $M = M_1 + M_2 = 5 + 5 = 10$
 - iv. $(v_6, v_7), (v_1, v_3)$, matching $M = M_1 + M_2 = 5 + 5 = 10$

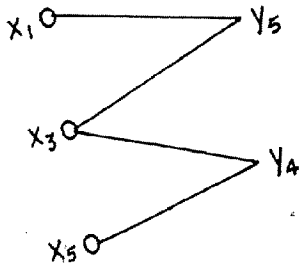
here maximum total matching in two steps is 11 for $(v_6, v_7), (v_1, v_2)$, but since $M_1 = 5 = NR - 1$, choose the set $M = \{(v_3, v_6), (v_1, v_2)\}$ as a maximum matching in G_1 .



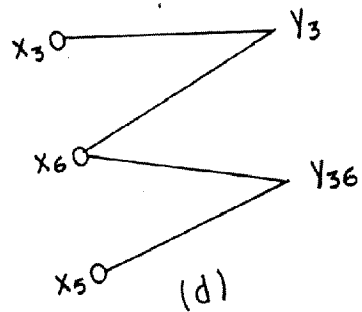
(a)



(b)



(c)



(d)

- (a) $G_1 = [V_1, E_1]$
- (b) $G = [X, Y, E]$ for \bar{a}_9
- (c) Tree $T = [W, Z, D]$
- (d) $G = [X, Y, E]$ for \bar{a}_7

FIGURE 3.2

3. Columns \bar{a}_3 and \bar{a}_6 are merged into $\bar{a}_{36} \triangleq \bar{a}_3 + \bar{a}_6$,
and \bar{a}_1 and \bar{a}_2 into $\bar{a}_{12} \triangleq \bar{a}_1 + \bar{a}_2$. Thus we have

$$A = \begin{matrix} & \bar{a}_4 & \bar{a}_5 & \bar{a}_7 & \bar{a}_8 & \bar{a}_9 & \bar{a}_{12} & \bar{a}_{36} \\ \begin{matrix} 1 \\ 2 \\ 3 \\ 4 \\ 5 \\ 6 \end{matrix} & \begin{bmatrix} 1_4 & 0 & 0 & 0 & 1_9 & 1_1 & 1_6 \\ 1_4 & 1_5 & 0 & 1_8 & 0 & 1_2 & 1_3 \\ 0 & 0 & 1_7 & 0 & 1_9 & 1_2 & 1_3 \\ 1_4 & 1_5 & 0 & 1_8 & 0 & 1_1 & 1_6 \\ 0 & 1_5 & 1_7 & 1_8 & 1_9 & 1_1 & 0 \\ 1_4 & 0 & 1_7 & 0 & 0 & 1_2 & 0 \end{bmatrix} \end{matrix}$$

where new columns \bar{a}_{12} and \bar{a}_{36} are inadmissible.

4. $E_2 = \emptyset$, hence go to phase 2.

Phase 2

1. Delete \bar{a}_{12} from A and add it to the solution matrix A_0 .

$$A = \begin{matrix} & \bar{a}_4 & \bar{a}_5 & \bar{a}_7 & \bar{a}_8 & \bar{a}_9 & \bar{a}_{36} \\ \begin{matrix} 1 \\ 2 \\ 3 \\ 4 \\ 5 \\ 6 \end{matrix} & \begin{bmatrix} 1_4 & 0 & 0 & 0 & 1_9 & 1_6 \\ 1_4 & 1_5 & 0 & 1_8 & 0 & 1_3 \\ 0 & 0 & 1_7 & 0 & 1_9 & 1_3 \\ 1_4 & 1_5 & 0 & 1_8 & 0 & 1_6 \\ 0 & 1_5 & 1_7 & 1_8 & 1_9 & 0 \\ 1_4 & 0 & 1_7 & 0 & 0 & 0 \end{bmatrix} \end{matrix} \quad A_0 = \begin{matrix} & \bar{a}_{12} \\ \begin{matrix} 1 \\ 2 \\ 3 \\ 4 \\ 5 \\ 6 \end{matrix} & \begin{bmatrix} 1_1 \\ 1_2 \\ 1_2 \\ 1_1 \\ 1_1 \\ 1_2 \end{bmatrix} \end{matrix}$$

2. Select \bar{a}_9 as \bar{a}_f

The bipartite graph G for \bar{a}_9 is constructed as shown in figure 3.2(b).

3. The trees $[X, Z; D]$ spanning X in $G = [X, Y; E]$ are

i) $[W, Z; D] \triangleq [\{x_1, x_3, x_5\}, \{y_4, y_5\}, \{(x_3, y_4), (x_5, y_4), (x_1, y_5), (x_3, y_5)\}]$

total number of zeros in y_4 and $y_5 = 3+2=5$

ii) $[W, Z; D] \triangleq [\{x_1, x_3, x_5\}, \{y_4, y_3\}, \{(x_3, y_4), (x_5, y_4), (x_1, y_8), (x_3, y_8)\}]$

total number of zeros in y_4 and $y_8 = 3+2 = 5$

4. Choose the tree $[W, Z; D] \triangleq [\{x_1, x_3, x_5\}, \{y_4, y_5\}, \{(x_3, y_4), (x_5, y_4), (x_1, y_5), (x_3, y_5)\}]$

as shown in figure 3.2(c).

5. From this tree^{it} is evident that $\bar{a}_4 = \bar{a}_9$ is decomposed into $\bar{a}_9^{(4)} = [001010]^t$ and $\bar{a}_9^{(5)} = [101000]^t$ columns $\bar{a}_9^{(4)}$ and \bar{a}_4 are merged into a new inadmissible column \bar{a}_{49} and columns $\bar{a}_9^{(5)}$ and \bar{a}_5 into \bar{a}_{59} . Resultant A and A_0 become

$$A = \begin{matrix} & \bar{a}_7 & \bar{a}_8 & \bar{a}_{36} \\ \begin{matrix} 1 \\ 2 \\ 3 \\ 4 \\ 5 \\ 6 \end{matrix} & \begin{bmatrix} 0 & 0 & 1_6 \\ 0 & 1_8 & 1_3 \\ 1_7 & 0 & 1_3 \\ 0 & 1_8 & 1_6 \\ 1_7 & 1_8 & 0 \\ 1_7 & 0 & 0 \end{bmatrix} & & \end{matrix} \quad A_0 = \begin{matrix} & \bar{a}_{12} & \bar{a}_{49} & \bar{a}_{59} \\ \begin{matrix} 1 \\ 2 \\ 3 \\ 4 \\ 5 \\ 6 \end{matrix} & \begin{bmatrix} 1_1 & 1_4 & 1_9 \\ 1_2 & 1_4 & 1_5 \\ 1_2 & 1_9 & 1_9 \\ 1_1 & 1_4 & 1_5 \\ 1_1 & 1_9 & 1_5 \\ 1_2 & 1_4 & 0 \end{bmatrix} & & \end{matrix}$$

6. In the bipartite graph constructed for \bar{a}_8 , X is not contained in a connected component, so \bar{a}_7 is selected as \bar{a} and the bipartite graph is obtained as shown in figure 3.2(d).

7. G itself forms the required tree. Hence, \bar{a}_8 is decomposed into $\bar{a}_7^{(8)} = [001001]^t$ and $\bar{a}_7^{(36)} = [000011]^t$

8. After merging $\bar{a}_7^{(8)}$ with \bar{a}_8 and $\bar{a}_7^{(36)}$ with \bar{a}_{36} ,

A is transformed into

$$A = \begin{matrix} & \bar{a}_{78} & \bar{a}_{367} \\ \begin{matrix} 1 \\ 2 \\ 3 \\ 4 \\ 5 \\ 6 \end{matrix} & \begin{bmatrix} 0 & 1_6 \\ 1_8 & 1_3 \\ 1_7 & 1_3 \\ 1_8 & 1_6 \\ 1_8 & 1_7 \\ 1_7 & 1_7 \end{bmatrix} \end{matrix}$$

9. Adding \bar{a}_{78} and \bar{a}_{367} to A_0

$$A_0 = \begin{matrix} & \bar{a}_{12} & \bar{a}_{54} & \bar{a}_{49} & \bar{a}_{367} & \bar{a}_{78} \\ \begin{matrix} 1 \\ 2 \\ 3 \\ 4 \\ 5 \\ 6 \end{matrix} & \begin{bmatrix} 1_1 & 1_9 & 1_4 & 1_6 & 0 \\ 1_2 & 1_5 & 1_4 & 1_3 & 1_8 \\ 1_2 & 1_9 & 1_9 & 1_3 & 1_7 \\ 1_1 & 1_5 & 1_4 & 1_6 & 1_8 \\ 1_1 & 1_5 & 1_9 & 1_7 & 1_8 \\ 1_2 & 0 & 1_4 & 1_7 & 1_7 \end{bmatrix} \end{matrix}$$

Thus the circuit is realized in 5 via columns.

CHAPTER - 4

CONCLUSIONS AND SUGGESTIONS

4.1 Conclusions

Extensive investigations have been carried out, in recent years on the design of electronic circuits with reference to performance, maintainability, cost, reliability, etc. The aim of this dissertation has been to develop efficient methods and more realistic mathematical models for performance optimization of the physical design of electronic circuits. The main conclusions of the present investigations are summarized below.

An improved iterative algorithm for optimally placing the components on the double layer printed circuit board has been developed. The components that are placed using this algorithm may be similar or dissimilar in size. The algorithm also incorporates the edge connectors which is an important part of every printed circuit board. The strategy adopted for iterative placement improvement is to calculate the change in function till the first improvement is encountered and the corresponding components are interchanged while solving the problem on a computer, this strategy requires considerably lesser amount of computer memory than the other strategy to calculate the change in function for all possible pairs and then interchanging the components corresponding to the maximum improvement.

This has facilitated the solution of larger problems, i.e. for circuits with more number of components.

A constructive algorithm has been developed which gives a good initial placement for the iterative procedure. The problems solved using the placement obtained by this constructive algorithm, as the initial placement for the iterative procedure are found to be requiring less number of iterations and hence lesser time for converging to a better local optimal, than those solved with an arbitrary initial placement.

For multilayer printed circuit board the component placement is obtained using a similar algorithm as that for double layer printed circuit board. A set of equations have been derived for the calculation of number of holes or vias for realizing a circuit on multilayer printed circuit board. It has been assumed that the routing of etches is done using a series of single row single layer routing procedures. An improved algorithm for via assignment has also been developed. This heuristic algorithm applies the processes of column merging and column decomposition to minimize the number of via columns necessary for the realization of the circuit. The columns to be merged are selected keeping in view the best merging in two consecutive steps.

Efficient computer programs have been developed for optimal component placement on double layer printed circuit boards and for placement and via assignment on multilayer printed circuit boards.

4.2 Suggestions For Future Research

Expressions are yet to be derived for sensitivity analysis in iterative placement improvement of different sized components. In this dissertation placement of components of only two different sizes is taken up. The algorithm may be extended to deal with various sized components.

Associated with the problem of via assignment on multilayer printed circuit board, the problems of how to order the via columns and that of layering, are also interesting, which also require further investigations.

One extremely useful area for future research is the natural combination of allocation, placement and routing problems. This combined problem, although large, should provide very useful results. Apart from this, more work must be done in the direction of global optimization of the placement problem.

APPENDIX - A

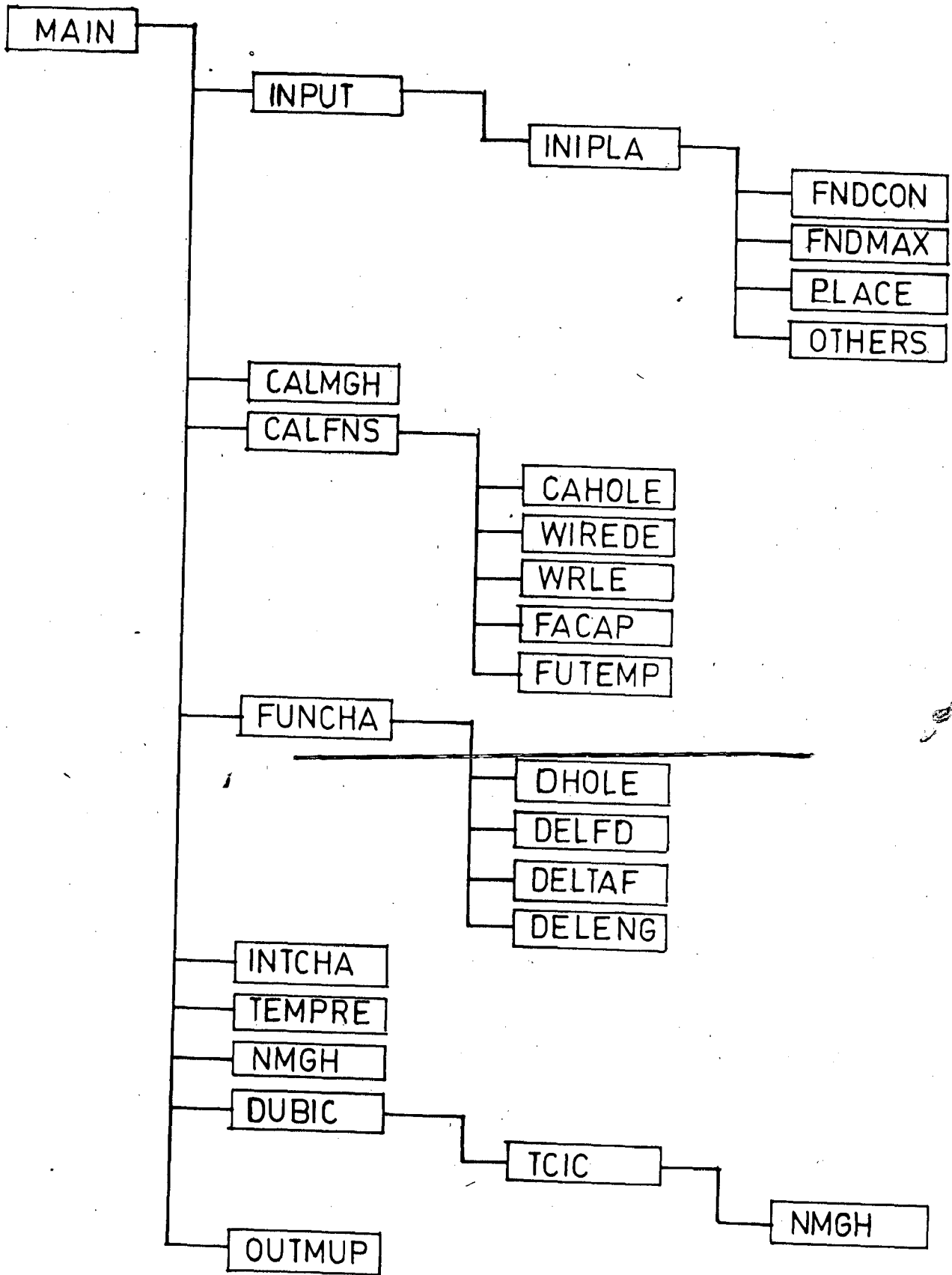
A computer program is written in FORTRAN-IV to implement the multicriteria optimal placement of components on double layer printed circuit board (MOPCOD.FOR). The overall organisation of the program is shown in Figure A1. A brief description of various subroutines is given below.

1. CAHOLE This subroutine is used for calculating the number of holes required for realizing the circuit using X-Y coordinate wiring on a double layer printed circuit board. It is called in subroutine CALFNS.
2. CALFNS This subroutine calculates the values of functions F_h , F_d , F_c and F_r . It is called in the main program and calls subroutines CAHOLE, WIREDE, WRLE, FACAP, FUTEMP.
3. CALMGH This subroutine calculates the matrix $[G:H]$. It is called in the MAIN program.
4. DELENG This subroutine is used to calculate the change in wiring length due to change in placement. It is called in subroutine FUNCHA.
5. DELFD This subroutine calculates the change in horizontal average density and vertical average density due to the change in placement. It is called in subroutine FUNCHA.

6. DELTAF This subroutine calculates the change in temperature rise function due to change in the placement. It is called in subroutine FUNCHA.
7. DHOLE This subroutine calculates the change in number of holes due to the change in placement. It is called in subroutine FUNCHA.
8. DUBIC This subroutine performs iterative improvement procedure on the placement by interchanging the pairs with components in same column (stage two) and then the pairs with components in same row (stage three). It is called in the MAIN program and calls the subroutine TCIC.
9. FACAP This subroutine calculates the function which is proportional to the stray capacitance. It is called by subroutine CALFNS.
10. FNDCON During the constructive initial placement procedure, this subroutine finds the placement of first 'a' components that correspond to the edge connector. It is called by the subroutine INIPLA.
11. FNDMAX This subroutine finds the component which has maximum connectivity with the components already placed during the constructive initial placement. It is called in the subroutine INIPLA.

12. FUNCHA This subroutine calculates the change in functions due to change in placement. It is called in the MAIN program and calls subroutines DHOLE, DELFD, DELTAF, DELENG.
13. FUTEMP This subroutine calculates temperature rise, mean temperature rise, mean failure rate and reliability of the circuit. It is called in the subroutine CALFNS.
14. INIPLA This subroutine finds the initial placement by performing the constructive algorithm. It is called in the subroutine INPUT and it calls subroutines FNDCON, FNDMAX, PLACE and OTHERS.
15. INPUT This subroutine reads the input data required for the program. The data that is number of horizontal and vertical divisions of the board, number of elements in the circuit, weightages corresponding to each optimization function, ambient temperature, thermal resistance, power dissipation, failure rate of each component, connectivity matrix and the thermal coupling coefficient matrix are given in the file Y.DAT. This subroutine is called in the MAIN program. If constructive initial placement is to be done it calls the subroutine INIPLA, otherwise the initial placement is read from X.DAT.
16. INTCHA This subroutine finds the new values of the functions after interchanging the components. It is called in the MAIN program.

17. NMGH This subroutine modifies the matrix [G:H] for the new placement. It is called in the MAIN program.
18. OTHERS The subroutine places the dummy components while doing the constructive placement. It is called in the subroutine INIPLA.
19. OUTMUP This subroutine outputs the results in the file Z. DAT. It is called in the MAIN program.
20. PLACE This subroutine places a component in a slot which is nearest to the position of a component during the constructive algorithm. It is called in the subroutine INIPLA.
21. TCIC This subroutine interchanges two pairs of components and calculates new function values. It is called in the subroutine DUBIC and it calls the subroutine NMGH.
22. TEMPRE This subroutine calculates the temperature rise and the circuit reliability. It is called in the main program.
23. WIREDE This subroutine calculates the average wiring density and is called in the subroutine CALFNS.
24. WRLE This subroutine calculates the total wiring length and is called in the subroutine CALFNS.



ORGANISATION OF THE PROGRAM MOPCOD. FOR
FIGURE A1

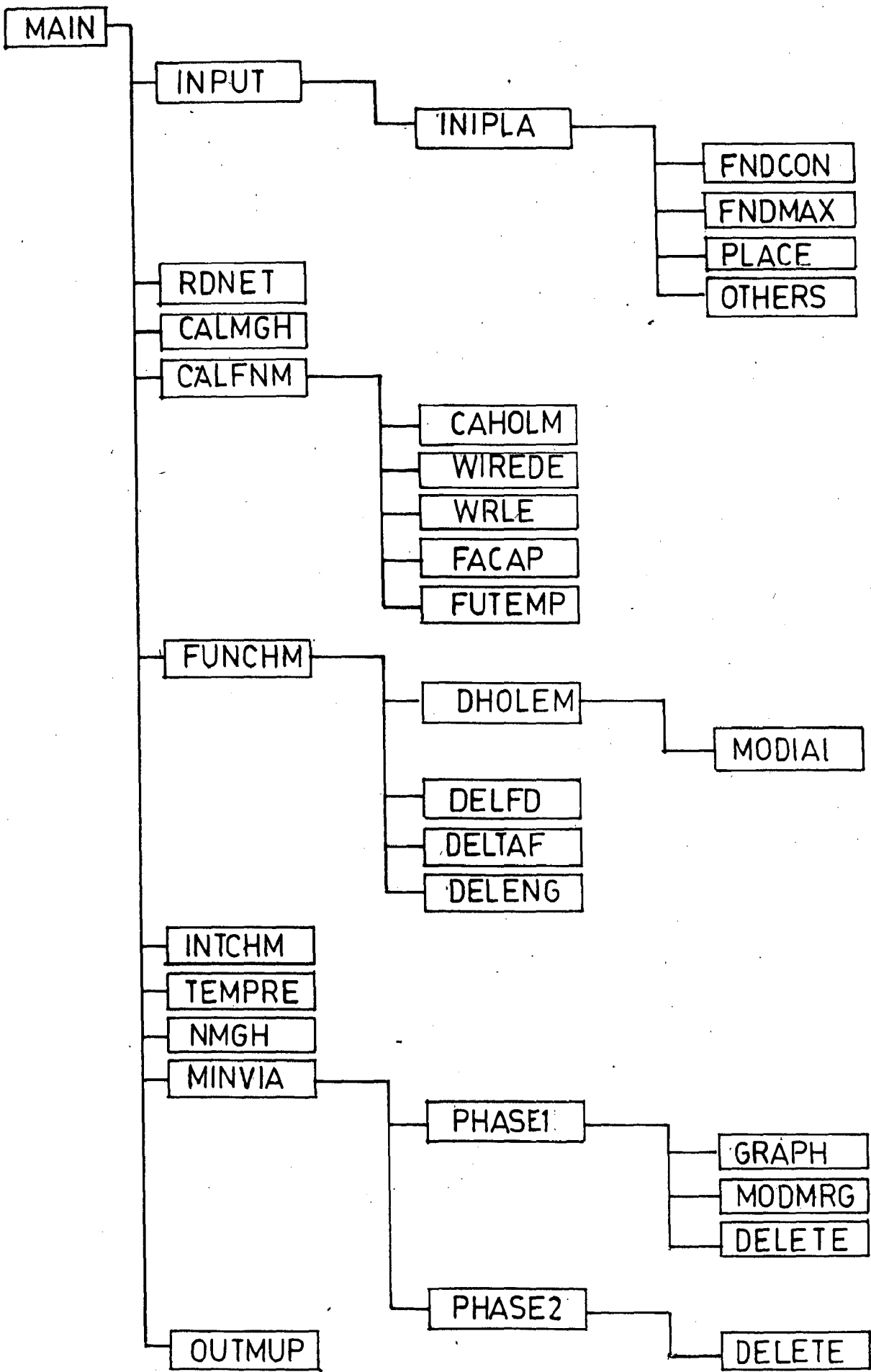
APPENDIX - B

For the implementation of component placement and via assignment on multilayer printed circuit board, a computer program in FORTRAN-IV is written. The overall organisation of the program called COPVAM. FOR is given in Figure B1. The subroutines CALMGH, DELENG, DELFD, DELTAF, FACAP, FNDCON, FNDMAX, FUTEMP, INIPLA, INPUT, NMGH, OTHERS, OUTMUP, PLACE, TEMPRE, WIREDE and WRLE perform the same functions as described in Appendix A. A brief description of other subroutines is given below.

1. CAHOLM This subroutine finds the total number of vias required for the realization of circuit with initial placement of components. The initial A matrix is also calculated. It is called in the subroutine CALFNM.
2. CALFNM This subroutine calculates the values of functions F_n , F_λ , F_d , F_c and F_r . It is called in the MAIN program and calls the subroutines CAHOLM, WIREDE, WRLE, FACAP, FUTEMP.
3. DELETE(I) This subroutine deletes the I th column from the matrix A. It is called in the subroutines PHASE1 and PHASE2.
4. DHOLEM This subroutine calculates the change in number of vias due to change in placement. It is called in the subroutine FUNCHM and calls the subroutine MODIAI.

5. FUNCHM This subroutine calculates the change in the functions due to change in the placement. It is called in the MAIN program and calls the subroutines DHOLEM, DELFD, DELTAF and DELENG.
6. GRAPH This subroutine finds the graph with vertices corresponding to the columns of A that can be merged with another column. It is called in the subroutine PHASE1.
7. INTCHM This subroutine finds the new values of the functions and the new matrix A after interchanging two components. It is called in the MAIN program.
8. MINVIA This subroutine minimizes the number of via columns required on the board after the optimal component placement is achieved. It is called in the MAIN program and calls the subroutines PHASE1 and PHASE2.
9. MODIAI This subroutine modifies the matrix A after interchanging two components. It is called in the subroutine DHOLEM.
10. MODMRG(I,J) This subroutine modifies the graph and merges the columns I and J of the matrix A. It is called in the subroutine PHASE1.
11. PHASE1 This subroutine performs the phase one of the minimization of via columns process by repeatedly merging the columns. It is called in the subroutine MINVIA and it calls the subroutines GRAPH, MODMRG and DELETE.

12. PHASE2 This subroutine performs the second phase of minimization of via columns by column decomposition. It is called in the subroutine MINVIA and calls the subroutine DELETE.
13. RDNET This subroutine reads the nets connected to each component from the file W.DAT. It is called in the MAIN program.



ORGANISATION OF THE PROGRAM COPVAM. FOR
FIGURE B1

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