MICROPROCESSOR CONTROLLED COMMUTATORLESS DC SERIES MOTOR DRIVE

A DISSERTATION

submitted in partial fulfilment of
the requirements for the award of the degree
of
MASTER OF ENGINEERING
in
ELECTRICAL ENGINEERING
(Power Apparatus and Electric Drives)

By

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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the dissertation entitled, MICROPROCESSOR CONTROLLED COMMUTATORLESS DC SERIES MOTOR DRIVE, in partial fulfilment of the requirements for the award of the degree of MASTER OF ENGINEERING IN ELECTRICAL ENGINEERING with specialization in POWER APPARATUS AND ELECTRIC DRIVES, submitted in the Department of Electrical Engineering, University of Roorkee, Roorkee, is an authentic record of my own work carried out for a period of about seven months, from August, 1987 to February, 1988 under the supervision of Dr. S.P.Gupta, Reader and Dr. Bhim Singh, Lecturer, Department of Electrical Engineering, University of Roorkee, Roorkee, India.

The matter embodied in the dissertation has not been submitted by me for the award of any other degree or diploma.

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ABSTRACT

The dissertation concerns the design, fabrication and performance of the microprocessor controlled commutatorless d.c. series motor by using induced voltage commutated inverter along with induced voltage sensor. The firing pulses for thyristors of the inverter are generated by the microprocessor in proper sequence with the help of synchronizing signal derived from the terminal voltages of the synchronous machine. A three-phase synchronous motor supplied by a line commutated inverter (LCI) with the excitation winding connected in series to the d.c. link becomes equivalent to a simple commutatorless d.c. series motor which gives excellent d.c. series motor characteristics.

The steady state analytical model of the drive is developed by using steady state equivalent circuit and performance is computed therefrom. The performance is obtained experimentally also using the fabricated system and the experimental results have shown a good correlation with the computed results. The configuration of the firing angle control scheme used in present work is comparatively simple and requires less software and hardware in comparison to the earlier schemes.

NOMENCLATURE

E_{sy}	The rms value of line to neutral no load terminal voltage
V_{sy}	The rms line to neutral machine terminal voltage.
I_{sy}	The rms value of the fundamental component of the machine line current.
I_{syd}	Direct axis component of I_{sy}
I_{syq}	Quadrature axis component of I_{sy}.
I_{dc}	DC link current.
P_{ac}	Real a.c. power fed to the machine.
P_{dc}	DC power fed to the LCI.
V_d	Average d.c. output voltage of the rectifier.
V_{dc}	Average d.c. input voltage to the LCI.
X_d	Direct axis synchronous reactance.
X_q	Quadrature axis synchronous reactance.
X_c	Commutating reactance.
X	Adjusted direct axis synchronous reactance.
q	Ratio of adjusted quadrature to direct axis synchronous reactance.
ϕ	Flux per pole.
N	Machine speed in rpm.
N_s	Machine speed in rps.
R_f	Resistance of field winding of synchronous machine.
R_d	Resistance of the d.c. link inductor.

R_{sy} Stator resistance of synchronous machine.

α Inverter firing angle in electrical degrees.

β Inverter lead angle in electrical degrees.

μ Commutation overlap angle in electrical degrees.

β' Supplementary displacement angle of I_{sy} with respect to V_{sy} in electrical degrees.

γ Supplementary displacement angle of I_{sy} with respect to E_{sy} in electrical degrees.

δ Thyristor turn-off angle in electrical degrees.

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CHAPTER - I

INTRODUCTION

1.1 GENERAL

Many modern variable speed drives require a precise and smooth control of speed with Long term stability and good transient performance. From the very beginning, the conventional D.C. motors have been used as variable speed drives in many industrial applications. However, for reliable operation of the system, the D.C. motor drives are not advisable in many cases due to the following drawbacks [1]:

i) Mechanical commutator needs regular maintenance.

ii) The commutator construction increases the cost of the Drive.

iii) Power/weight ratio is reduced.

iv) Brush and commutator wear occurs due to sparking and friction.

v) The mica insulation limits the voltage between the segments.

vi) Unsuitable to operate in dusty and explosive environments.

Commutatorless D.C. motor [2-13] drives which uses synchronous motor can be used most economically as variable speed drives in place of conventional D.C. motor drives, over a wide range of speed. Synchronous motor fed by a line commutated inverter (LCI) acts like a commutatorless

D.C. motor. This drive has several advantages in their favour compared with variable speed drives using other types of motors. Synchronous motors are rugged reliable and free of trouble some commutator maintenance. Power circuit and firing circuit configuration of LCI are quite simple in structure. Moreover, this drive provides the variable speed characteristics like those of conventional D.C. motor [5,7].

Forced commutated inverters have been widely used as variable frequency source for speed control of synchronous machine. However, this scheme needs complicated power and control circuits [14]. As a result of availability of improved voltage and current rating thyristors and with their prices coming down, people have shown considerable interest in synchronous type machines used as commutator-less D.C. motors instead of conventional D.C. motor for variable speed drives.

The rotating type of frequency converters were used previously to obtain variable frequency output from fixed frequency source, but now they are absolete at the advent of silicon-controlled rectifier and are replaced by the solid state frequency converters [1]. The solid state variable frequency source available at present for A.C. drives can be classified into three categories:

i) cycloconverter
ii) voltage source inverter
iii) current source inverter

A cycloconverter converts a.c. power of fixed frequency to a lower output frequency in a single conversion step. The output frequency range is preferably limited to one third of the supply frequency [15] and therefore the drives employing cycloconverters are suitable only for operation at low frequency. It can be designed to produce variable frequency, variable voltage power to drive a.c. motors. It is inherently capable of power transfer in either direction between source and load. The cycloconverter delivers a high quality sinusoidal waveform at low output frequencies. One important advantage of cycloconverter drive is that regeneration is simple and the system can be designed for four quadrant operation. The commutation of SCRs in a cycloconverter is natural but it requires a large number of thyristors and its control circuit is more complex. The cycloconverter has a low input power factor. Such drives are normally used in very large power applications. But the cost and complexity of power and control circuits make them uncompetitive with other classes of drives. Voltage source inverters are generally clasified into two types:

a) Square wave inverters

b) Pulse width modulated (PWM) inverters

Square wave inverter drive utilizes a controlled rectifier to transform the incoming a.c. voltage to variable D.C. voltage. This is followed by an inverter section. The frequency of the output is controlled by

sequentially switching the transistors or thyristors in the inverter section in six discrete steps. Square wave inverter has a number of undesirable effects such as additional harmonic power losses and torque pulsations in the motors. It requires large amount of d.c. filter components. which consists of the d.c. inductors and filter capacitors. The commutating capacitor in the VSI is usually charged by the d.c. link voltage, hence commutating capability decreases as the D.C. voltage decreases [16]. This type of inverter causes increased commutation losses and requires complex firing control circuitry.

The PWM drive generally utilizes, a diode rectifier to provide a constant D.C. voltage. The inverter section in this type of drive therefore controls both voltage and frequency. In PWM inverters, thyristors are switched on and off many times in each half cycle to generate avariable voltage output. There are many techniques to achieve PWM. But sinusoidal PWM techniques [1] is most common. This technique reduces the harmonic losses to a great extent but it suffers from low inverter efficiency. Since a PWM inverter presents a closer simulation of sine wave power to the motor, less power filter components are required [16]. However, the complex switching waveforms in the inverter require the most complex regulator and losses due to switching can be high.

The commutating circuitry increases the cost of the inverters. The PWM drive has near-unity power factor due to the diode rectifier input and constant patential d.c. link.

A current source inverter drive also uses a controlled rectifier to convert a.c. to variable patential d.c. The inverter section produces variable frequency six-step current and the voltage follows the current with commutation spikes due to thyristor firing. The current source inverter fed a.c. drive has the following favourable features [17,18]:

i) This drive has the ability to control the motor current which results in complete torque control.

ii) Commutation losses are lower than in VSI drives

iii) Regeneration is possible

iv) The inverter can be designed with low speed SCRs.

v) Fault current on the inverter side rises very slowly.

vi) The CSI controller tends to maintain a higher level of efficiency than that in VSI drive.

However, against the above mentioned features, the CSI fed drives have the following draw backs:

i) The current controlling chanacteristic of the drive necessitates a large filter inductors due to the necessity of controlling the motor solely by current.

ii) The frequency range of inverter is lower and it can not operate at no load condition.

iii) The drive has instability problems and sluggish response at light loads and high speeds.

iv) The commutation is dependent upon the machine subtransient inductance which adds large transient over voltages at machine terminals.

The line commutated inverter overcomes all the problems of forced commutated inverters (VSI or CSI) as well as cycloconverters. A line commutated inverter is obtained by operating an SCR bridge in continuous current mode with firing angle greater than 90°. The sequential commutation of SCRs is performed naturally with the help of terminal voltages of the synchronous machine connected on a.c. side of the inverter. The line commutated inverter requires reactive power for commutation. This reactive power is supplied by the synchronous machine operating at leading power factor. Some of the favourable characteristics features of LCI are [14,19]:

i) Commutating components are not required. As a result inverter cost is reduced to a great extent.

ii) Harmonics in the output voltage wave form are reduced.

iii) The triggering circuit requirements are comparatively simple.

iv) Commutation losses are reduced.

v) Line commutated inverter fed synchronous motor can be efficiently used as a variable frequency source to drive other a.c. motors.

vi) LCI drives provide stable operation within the desired range of speed.

Against the above mentioned features, line commutated inverter fed synchronous motor drive has the following limitations [17,20]:

i) It is not self starting. Extra starting arrangements are required to start the synchronous motor which increase the cost of the drive.

ii) Commutation failure occurs at lower speed and the range of speed is therefore limited by this factor.

iii) Since the sinusoidal emf of the synchronous machine is available at the a.c. terminals of the inverter for commutation of inverter thyristors, the inverter must be current fed and this necessitates the use of large link inductance.

iv) The inverter can not recover after a commutation failure.

In the present work, a line commutated inverter has been proposed to realize the commutatorless D.C. series motor drive.

The commutatorless D.C. motor system uses a conventional synchronous motor which is interfaced to

a d.c. power supply by a variable frequency thyristorized inverter. The inverter switches the power to the appropriate stator windings of the machine. The inverter firing is controlled by the synchronizing signals obtained from an induced voltage sensor or a rotor position sensor. Induced voltage sensor uses a step down transformer for sensing the terminal voltage of the synchronous motor and it is simple as compared to rotor position sensor. The combination of sensor and inverter replaces the commutator of conventional d.c. motor and inverter frequency is a function of the motor speed. Thus the synchronous motor itself is the controller, much the same as a conventional d.c. motor.

Starting of commutatorless motor is another important factor to be considered. Commutatorless motor is unable to start from standstill condition. Extra starting arrangements are necessary to start the motor from standstill. This is the major drawback of LCI fed synchronous motor drives. Several methods are known for starting purpose. Some of these techniques [20] reported so far are as follows:

i) Starting with an auxiliary thyristor in parallel with D.C. link inductor.

ii) Starting without an auxiliary thyristor

iii) Starting using an auxiliary motor.

Since the combination of LCI and synchronous motor constitute a commutatorless d.c. motor, hence three types of CLM can be realized by placing the field winding in different positions.

i) Separately excited commutatorless d.c. motor
ii) Shunt commutatorless d.c. motor
iii) Series commutatorless d.c. motor

The commutatorless motor of induced voltage commutation type is very practical due to its simple structures. However, in case of shunt type CLM the commutation angle increases with the load current resulting in the decrease of margin angle (δ) which often causes commutation failure [13]. This type of commutatorless motor has limited overload capacity as compared to the series type CLM [5]. In series type CLM, the field winding of the synchronous machine is connected in series with the d.c. link. Commutatorless D.C. series motor exhibits the characteristics [5,7] similar to that of a conventional d.c. series motor. In case of series type CLM using natural commutation, overlap angle (μ) and commutation margin angle (δ) are independent of both the load current and machine speed provided the magnetic saturation and armature reaction are negligible [4,5,7]. For this reason, it operates without commutation problems even in overload condition [5].

In the present work, microprocessor based commutatorless d.c. series motor has been designed, fabricated and tested.

1.2 LITERATURE SURVEY

A large volume of research has been done on the shunt type commutatorless d.c. motors. From literature review, it is found that not much work has so far been reported in the field of series commutatorless d.c. motor. Kenji Watanabe, Katsuji Oyamori and Noriaki Sato [4] have discussed the effect of magnetic saturation on the operating characteristics of series commutatorless motor. They have also verified that operating region of the CLM can be widened by attaching compensating winding.

F.C.Brockhurst [5] has sestablished performance equation for D.C. commutatorless motors using salient-pole synchronous-type machines in terms of machine inductances. Speed independent equations for commutation angle, commutating current, critical angle, safety angle, torques and instantaneous damper currents have been developed G.H. Pfitscher [21] has developed a microprocessor based scheme that generates the necessary synchronization logical signals for three phase static power converter control systems. The problem of detecting the phase-to-phase voltage zero-crossing in presence of noise generated by thyristor commutations in constant and in variable frequency

voltage and from the circuit configuration of the system. The firing angle may take any value from 0^{o} to 180^{o}. Ajay Kumar, R. Anbarsu and B.P.Singh [7] have analyzed the steady state performance of series commutatorless D.C. motor using induced voltage sensor. It has been experimentally verified that overlap angle, power factor and armature reaction angle are independent of frequency and load current.

H. Naito, K. Iwamoto and Funio Harashima [12] has determined analytically and verified the dynamic characteristics of lead angle controlled commutatorless motor and have pointed out the instability problems, associated with this type of control method. Tokeda, S.Monimoto and T.Hirasa [13] have discussed the generalized analysis for steady state characteristics of D.C. commutatorless motor. The variation of commutation angle, shift angle, demagnetization due to armature reaction, safety margin angle, average torque and speed with mean input current are examined quantitatively for cylindrical and salient pole motors.

M.V.S.S. Ranganadhachari, B.P. Singh, R. Anbarasu and R. Arockiasamy [14] have presented experimental investigation on line commutated inverter synchronous machine as a variable frequency source. It has been verified experimentally that inverter synchronous machine scheme works quitesatisfactorily as a variable frequency source for both

static and dynamic loads. Chandrasekhar Namuduri and P.C. Sen [25] have described a digital simulation method for the self controlled synchronous motor in time domain. The effects of damper windings and saliency on the torque, and voltage and current waveforms are also studied using digital simulation technique wh n the machine is operated from a voltage power inverter and a current source inverter. Performance of the synchronous machine with nonsinusoidal voltages and currents is simulated under both steady state and transient conditions.

In 1983, J. Davoine, R. Perret and Hoang-Le-Huy [1] have discussed the microcomputer controlled operation of self-controlled synchronous motor employing terminal voltage sensing technique. In this scheme the standstill position of rotor is computed by microcomputer by analysing and sampling the induced voltage in the stator when a step voltage is applied to the field winding. The microcomputer also takes care of starting the motor from standstill by using auxiliary thyristor in parallel of D.C. link inductor.

1.3 SCOPE OF PRESENT WORK

A salient type synchronous motor fed from a machine voltage commutated inverter is considered for realizing a series type commutatorless D.C. motor. Three phase uncontrolled rectifier, thyristorized line commutated inverter

and a simple microprocessor based firing control scheme using less hardware components are designed, fabricated and experimentally tested.

An interfacing circuit of the programmable interval timer 8253A is designed and fabricated for using in the present scheme. A look up table method for displaying speed in the address field without any extra hardware is developed. The system software is implemented and tested.

The steady state analysis of the commutatorless D.C. series motor is developed by using equivalent circuit and vector diagram of the drive. The steady state performance characteristics of the drive are computed such as machine terminal voltage, machine current, power factor, commutation angle, safety margin angle, active and reactive power, speed and torque by varying D.C. link current at different D.C. link voltage and firing angle using DEC-2050 mainframe digital computer.

The performance of the line commutated inverter is investigated. The no load test is carried out on the SCLM system by varying D.C. link voltage with constant firing angle or varying firing angle with constant D.C. link voltage. The load test is performed on the drive at different D.C. link voltage and firing angle and the steady state performance of the drive is obtained experimentally. The experimental results are compared with the theoretical

ones and the discrepancies between the two are discussed.

The oscillograms of machine terminal voltage, machine current, D.C. link voltage, D.C. link current at no load and load conditions and waveshapes at different points of the firing circuit are recorded and discussed.

Outline of Chapters:

In chapter II, the complete hardware of the present scheme is discussed in detail. The design of power circuit, microprocessor based firing control circuit using less hardware components and pulse amplifier circuit are presented in this chapter. The interfacing technique of the programmable interval timer 8253A is also discussed.

The implementation of software and flowcharts of the commutatorless D.C. series motor is discussed in chapter III. The various subroutines used in conjunction with the main program such as ADC subroutine, DIVISION subroutine, MULT subroutine, IR_0 interrupt subroutine, IR_2 interrupt subroutine, IR_4 interrupt subroutine and SPEED subroutine are also developed in this chapter.

Chapter IV deals with the steady state analysis of the drive. The mathematical equations for steady state analysis are obtained by using equivalent circuit and vector diagram of the SCLM system. The results of experimental investigation of the fabricated system are

presented in chapter V. In the last chapter, main conclusions and suggestions for further works are discussed.

The ratings of the machine, pin details and connection diagrams of different IC chip, assembly language program for firing control of LCI and fortran program for steady state analysis of the drive are given in Appendices.

CHAPTER - II

DESCRIPTION OF THE SYSTEM

2.1 GENERAL

The complete scheme for realizing a commutatorless D.C. series motor is described in this chapter. A microprocessor based LCI firing angle control scheme philosophy is discussed in depth together with the hardware requirements. The synchronizing signal is generated by sensing two line to line voltages from synchronous machine terminals. This signal is used as an interrupt and at the same time to store the frequency information of the machine voltage. The interfacing technique of the programmable interval timer 8253A is also given in this chapter.

2.2 PRINCIPLE OF OPERATION

The block diagram of the commutatorless d.c. series motor is shown in Fig. 2.1. It basically consists of an autotransformer, an uncontrolled rectifier bridge, d.c. link smoothing inductor, series field winding, line commutated inverter and a 3-phase synchronous machine. The uncontrolled rectifier, together with the smoothing inductor, acts as a d.c. current source. Its output I_{dc} is impressed at the d.c. input of the machine voltage commutated inverter.

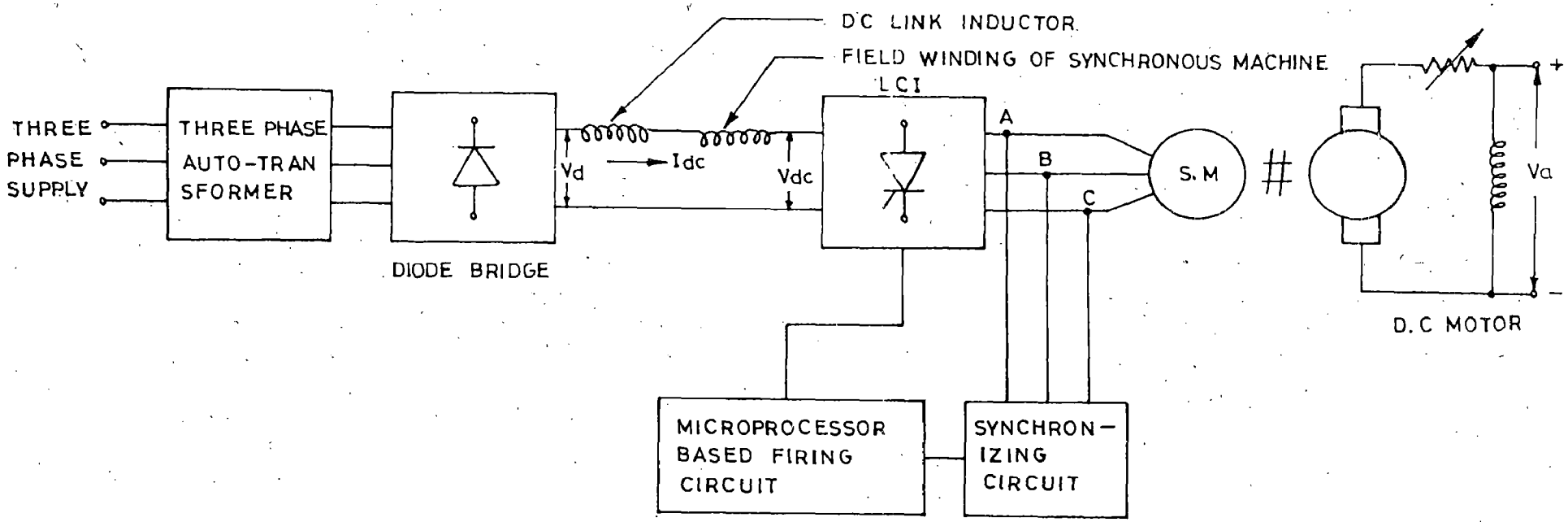


FIG. 2·1 – BLOCK DIAGRAM OF COMMUTATORLESS DC SERIES MOTOR

The synchronous machine is interfaced with a d.c. power supply by a variable frequency static inverter which switches the power to the appropriate stator windings of the synchronous machine. The excitation winding of the synchronous motor is connected in series to the input of the inverter and therefore the excitation current is directly proportional to the load current like a conventional d.c. series motor.

A synchronizing signal of 60^{o} pulse width of the machine voltage is generated from the terminal voltage of the synchronous machine. This synchronizing signal is inputted to the port C of 8255, Gate of TM2 of PIT 8253A(1) and IRO interrupt pin of PIC 8259A for generating firing pulses for the inverter thyristors. The firing angle of line commutated inverter is always kept between 90^{o} to 180^{o} and is approximately equal to the power factor of the synchronous machine. The triggering angle of the inverter can be adjusted at any valve between 90^{o} to 180^{o} by changing ADC output. In this scheme, the terminal voltage of the synchronous machine commutate the thyristor of LCI with the help of firing pulses in sequence provided by the trigger circuit. The three-phase autotransformer provides variable a.c. input voltage to the uncontrolled bridge rectifier to produce variable d.c. output voltage. This controlled d.c. source supplies active power required for the synchronous machine.

The speed of commutatorless D.C. series motor may be expressed as [7]

$$N = \frac{V_d - I_{dc} R_{dc}}{K_N I_{dc} \cos\beta}$$

where V_d = dc link voltage, I_{dc} = dc link current and

β = Lead angle = $\pi - \alpha$

The frequency of the inverter output is controllable and is given by.

$$= \frac{P}{120} \quad \frac{V_d - I_{dc} R_{dc}}{K_N I_{dc} \cos\beta}$$

Since the combination of inverter and synchronous motor with field winding connected in series to the d.c. link works as a series commutatorless D.C. motor, its speed can be varied in the following ways:

I) Varying the input d.c. voltage to the inverter like a d.c. series motor

II) Changing the trigger angle of the line commutated inverter just like the speed change of a conventional d.c. series motor by shifting the brush position.

2.3 SYSTEM DESCRIPTION

The schematic diagram of the commutatorless D.C. series motor using induced voltage commutation along with the voltage sensor for synchronization is shown in

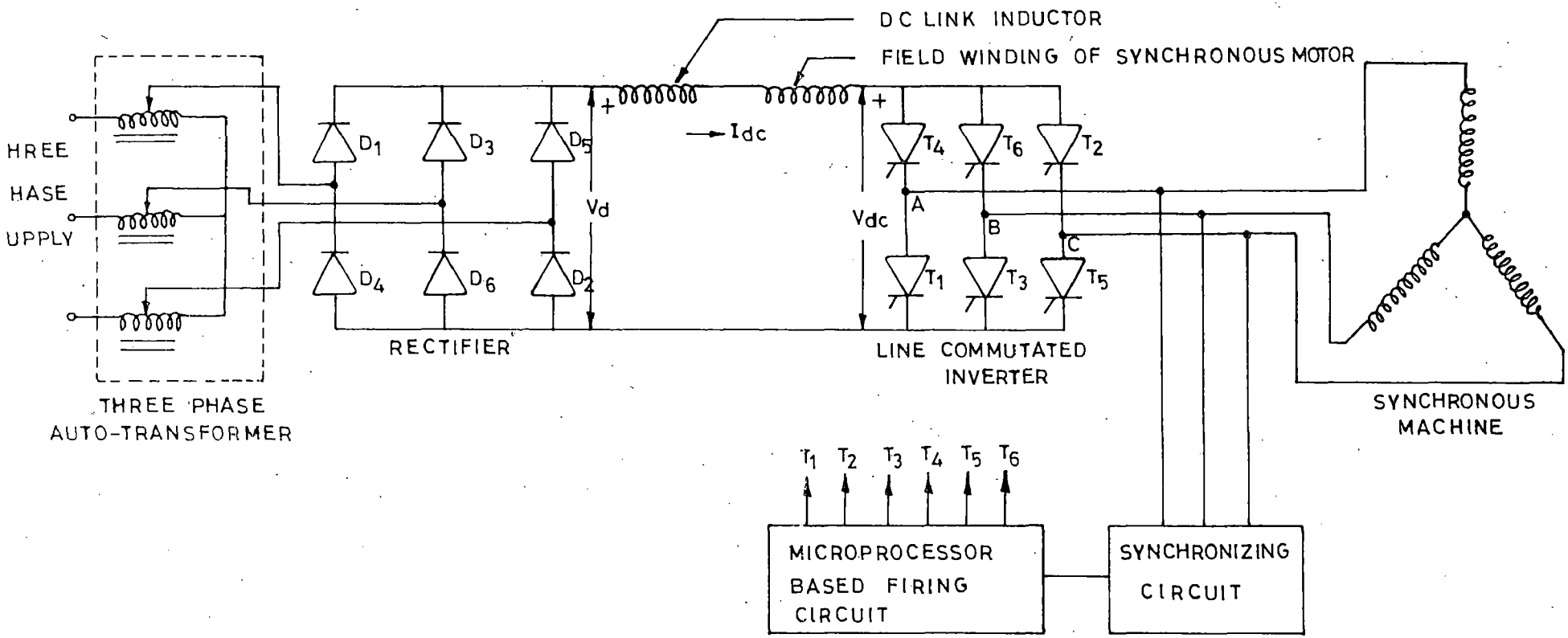


FIG. 2·2—SCHEMATIC DIAGRAM OF COMMUTATORLESS DC SERIES MOTOR

Fig. 2.2. This type of series motor makes use of conventional three-phase synchronous machine. The well known equation relating commutation lead angle (β), commutation overlap angle (μ) and input d.c. link current is given by

$$\text{Cos}\ (\beta - \mu) - \text{Cos}\beta = \sqrt{\frac{2}{3}}\ \frac{I_{dc}\ X_c}{E_{sy}}$$

where X_c = Commutating reactance.

For commutationless d.c. series motor the resultant flux is proportional to input d.c. current (I_{dc}) of the inverter and therefore internal induced voltage E_{sy} is proportional to the product of I_{dc} and N . Hence the above equation can be rewritten as

$$\text{Cos}\ (\beta - \mu) - \text{Cos}\beta = K_s\ L_c$$

Where K_s is a constant. This equation indicates that commutation overlap angle varies with firing angle and commutation inductance which is fixed by the design of the synchronous machine and it is independent of input d.c. current and motor speed. This is an important feature of the commutatorless d.c. series motor. For better understanding of the system operation, the major components are discussed briefly as under:

(I) Uncontrolled Diode Bridge:

The function of the diode bridge is to rectify the fixed frequency a.c. supply to a d.c. voltage and supply the

It is a three phase full wave diode bridge rectifier and its output is controlled by using an auto transformer at the a.c. supply. The active power requirements of the synchronous machine is met by this controlled d.c. source.

(II) D.C. Link Inductor:

The function of the d.c. link inductor is to suppress the harmonics contained in the output of the bridge rectifier. The combination of uncontrolled rectifier and D.C. link inductor acts as a current source. Its output is fed to the d.c. input of the line commutated inverter and excitation winding of the synchronous motor. For this purpose, choke is required to be of large inductance and keep the current continuous in the circuit.

(III) Line Commutated Inverter:

It is a simple three-phase thyristorized inverter bridge. The function of the inverter is to convert the d.c. voltage into a.c. voltage of variable amplitude and frequency. The commutation of inverter thyristor is performed by the voltage induced in the stator winding of the synchronous machine, which is seen by the inverter as a three-phase a.c. source of terminal voltage V_{sy}. For clear understanding of the line commutated inverter, the relation-ship between line to line voltages and line to neutral voltages of synchronous machine terminal along with firing instants

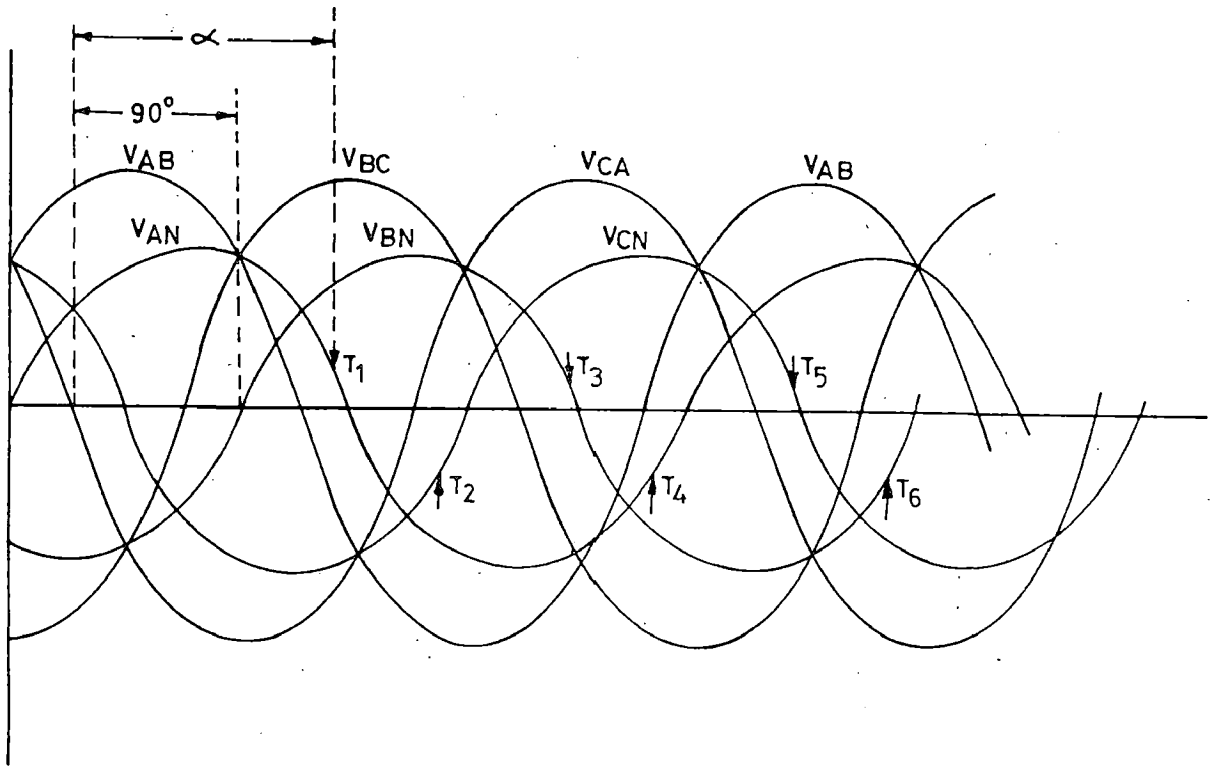


FIG. 2·3—RELATIONSHIP BETWEEN LINE TO LINE AND LINE TO NEUTRAL VOLTAGE ALONG WITH INSTANT OF FIRING

TABLE 2·1

CONDUCTION DURATION	0°—60°	60°—120°	120°—180°	180°—240°	240°—300°	300°—360°
FIRING SEQUENCE	1	2	3	4	5	6
THYRISTOR PAIR TO BE FIRIED	6 , 1	1 , 2	2 , 3	3 , 4	4 , 5	5 , 6

of the thyristors is shown in Fig. 2.3.

The thyristors T_1, T_3, T_5 are called positive group SCR since they are turned on when the machine terminal voltages are positive similarly the thyristors T_4, T_6, T_2 are called negative group SCRs. Since they are triggered when the machine voltages are negative. The firing angle of the inverter is always greater than 90° and measured from the instant of crossing point of two phase voltages as shown in Fig. 2.3. The firing angle for the thyristor T_1 is measured from the crossing point of positive going phase voltage V_{AN} and negative going phase voltage V_{CN}. The zero crossing instant of positive going line to line voltage V_{AC} coincides with the crossing point of V_{AN} and V_{CN}. Therefore, the zero crossing of V_{AC} may also be considered as reference for measuring firing angle of the thyristor T_1 and similarly for other thyristors. During normal operation, always two thyristors one from positive group SCR and another from negative group SCR will remain in conduction. Thyristors are triggered at 60° interval of terminal voltage frequency. Each thyristor conducts the positive current for 120° and negative current for 120° and the frequency of the current is same as that of machine terminal voltage. In case of line commutated inverter, machine current always leads the corresponding phase voltage. Let us consider the commutation phenomenon from T_1 to T_3 to make clear about the induced voltage commutation. When

thyristor T_3 from positive group is fired, thyristor T_1 gets reverse biased by the voltage, $V_{AB} = V_{AN} - V_{BN}$ and current is commutated from T_1 to T_3.

The presence of large source inductance many result in an appreciable modification in the process of commutating current from one thyristor to the other. When thyristor becomes turn off or turn on, current can not decay to zero or increase to a certain valve instantaneously due to presence of inductance. So in the process of commutation both incoming and outpgoing thyristor remain in conduction simultaneously for some moment. The period during which both thyristor remain in conduction is known as overlap period. The firing angle of the inverter is limited to a valve such that the angle $o = (\beta - \mu)$ is enough for proper commutation. Angle $(\pi - o)$ is referred to as the extinction angle of the inverter. The angle b is known as Turn off angle or safety margin angle. The firing is adjusted to a suitable value and normally keep constant through out the operation. The inverter normally operates at a constant margin angle.

The d.c. output voltage of a fully controlled converter is related to firing angle α by the following equation:

$$V_{dc} = \frac{3\sqrt{6}}{\pi} V \cos\alpha = V_{do} \cos\alpha$$

where V = per phase a.c. voltage

For firing angle between 0° to 90°, average d.c. voltage across the bridge is positive. If the firing angle α for the line commutated inverter is more than 90°, the d.c. voltage across the bridge will be negative. Thus, if a D.C. voltage source is connected across the inverter bridge in proper polarity and the d.c. voltage induced across the inverter bridge is less than the applied D.C. source, it will feed power to the A.C. system through the controlled circuit. For LCI, the waveform for the alternating line current closely resembles a rectangular wave. The output power factor angle will be approximately $(\beta - \mu/2)$ leading and the output power factor will be close to $\cos(\beta - \mu/2)$ or $-\cos(\alpha + \mu/2)$.

(IV) Synchronous Motor:

The synchronous motor is a conventional one and it is operated as a variable speed motor. The field winding of the machine is connected in series to the input of the LCI for realizing commutatorless D.C. series motor. The motor runs at synchronous speed corresponding to the frequency of the motor terminal voltage. The inverter a.c. terminals are connected to the synchronous machine and therefore, back emf of synchronous motor is available for natural commutation of the inverter thyristors. In the present scheme, the inverter switching is essentially controlled by the synchronous motor itself and the inverter frequency is a function of the motor speed. In series CLM, power factor

is independent of load and speed. It only depends on the firing angle of the line commutated inverter. The torque developed by the synchronous motor is directly proportional to the square of the d.c. link current for constant firing angle operation just like a conventional d.c. series motor.

(V) Synchronizing Circuit:

Synchronizing Circuit consists of step down transformer, comparator, switching transistor and AND gate. Synchronizing signal is of 60° pulse width of the machine frequency and derived from two line to line terminal voltages. The signal is fed to microcomputer for firing pulse generation in proper sequence and trigger angle control. The details of synchronizing circuit has been given later on.

(VI) Microprocessor Based Firing Circuit:

The synchronizing signal derived from the machine terminal voltages is fed to microcomputer for firing control of the inverter thyristors in proper sequence. This scheme uses less hardware components and overcomes most of the drawbacks of the analog firing scheme. The details of microprocessor based firing circuit has been discussed later on. The details of conduction duration, firing sequence and conducting thyristors are shown in Table 2.1.

2.3.1 Design of Power Circuit:

The power circuit is designed to meet the require-

ments of synchronous machine whose ratings are given in Appendix-I. The power circuit for the proposed scheme consists of the following parts:

i) Three phase diode bridge

ii) Three phase fully controlled line commutated inverter

iii) D.C. link inductor

CHOICE OF RATINGS OF DIODES

The voltage rating of the diodes of the uncontrolled bridge have to be selected with the consideration of the peak inverse voltage appearing across the devices, this in turn depends upon the maximum three phase input line voltage to the bridge. For a three phase bridge, the ratio of peak inverse voltage to line to neutral voltage is calculated as [26]

$$V_{PIV} = \frac{\pi}{3} V_{do}$$

where $V_{do} = \frac{3\sqrt{2}}{\pi} V_{L-L} = \frac{3\sqrt{2}}{\pi} \cdot \sqrt{3} \cdot V_{LN}$

$$= \frac{3\sqrt{6}}{\pi} V_{LN}$$

Therefore $\frac{V_{PIV}}{V_{LN}} = \frac{\pi}{3} \times \frac{3\sqrt{6}}{\pi} = 2.45$

For input line voltage 400V at 50Hz, peak inverse voltage across the diode is

$$V_{PIV} = 2.45\ V_{LN} = 2.45 \times \frac{400}{\sqrt{3}} = 566 \text{ volts}$$

A safety factor of 2 is allowed so that the diode can easily take reasonable over voltage.

The diode bridge has to supply 7 KW for the proposed synchronous machine

$$V_d I_{dc} = 3 V_{sy} I_{sy} \cos\beta' = 7000$$

$$I_{dc} = \frac{7000}{V_d}$$

The output average d.c. voltage of a full wave diode bridge is given by

$$V_d = \frac{3\sqrt{6}\, V}{\pi}$$

where V is the per phase rms input voltage. For 400V, 50Hz input voltage, the output of diode bridge becomes

$$V_d = \frac{3\sqrt{6}}{\pi} \times \frac{400}{\sqrt{3}} = 540 \text{ Volts}$$

$$\text{i.e. } I_{dc} = \frac{7000}{540} = 12.96 \approx 13 \text{ Amp.}$$

The current through the diode is given by

$$I_d = \frac{12.96}{3} = 4.32 \approx 5 \text{ Amp.}$$

Allowing a safety factor of 2, the diode current rating can be taken as

$$I_d = 5 \times 2 = 10 \text{ Amp.}$$

So the diode of rating 12 Amp, 1200 PIV can be selected to meet the requirements.

SELECTION OF RATINGS OF THYRISTOR

The following factors have to be considered for selecting the ratings of SCR.

i) Maximum PIV appearing across thyristor

ii) Power circuit configuration

iii) Conduction angle of individual thyristor

iv) Current wave form

v) Average current

For a three phase bridge, the ratio of PIV and line to neutral voltage is given by

$$\frac{E_{PIV}}{E_{LN}} = 2.45$$

$$E_{PIV} = 2.45 \times E_{LN} = 2.45 \times \frac{400}{\sqrt{3}}$$

$$= 566 \text{ V}$$

Taking a safety factor of 2, a 1200 PIV SCR is required.

For 7KW, 400V, 0.8 p.f synchronous motor, stator current is

$$I_A = \frac{7000}{\sqrt{3} \times 400 \times 0.8} = 12.63 \approx 12 \text{ Amp.}$$

Since each SCR conducts for 120° in each cycle, current through SCR is

$$I_T = \frac{12.63}{3} = 4.2098 \approx 5 \text{ Amp.}$$

Allowing a safety factor of 2, current rating of thyristor can be taken as $5 \times 2 = 10$ Amp.

So thyristor of Rating 12 Amp, 1200 PIV can be selected for this purpose. Each thyristor should be provided with over current, over voltage, $\frac{di}{dt}$ and $\frac{dv}{dt}$ protections. Over current protection can be made by connecting a fuse or a circuit breaker in series with the thyristor. Over voltage protection can be provided by using the thyrector diode across the thyristor. A voltage suppression network, commonly called a snubber circuit, consists of a series-connected resistor and a capacitor connected across the SCR, is used for protection against large $\frac{dv}{dt}$. $\frac{di}{dt}$ protection can be provided by placing a inductor having very low inductance in series with the thyristor.

2.3.2 Programmable Peripheral Devices:

Peripheral devices are required for organizing a microcomputer system. These components are organized around a common communication path called system bus which carry bits between the microprocessor and peripheral devices. The present microprocessor based control system makes use of 8253A interval timer, 8255A peripheral interface and 8259A interrupt controller. These are widely used general purpose programmable peripheral devices and completely compatible with any microprocessor. For better understanding and programming of these peripheral devices, a brief description is given below:

8253A PROGRAMMABLE INTERVAL TIMER

Intel 8253A is a very popular device specially designed for microcomputer applications which require timing and counting operation. This device can be used for application such as an event counter, a real time clock, a programmable one shat, a square wave generator and a complex wave form generator. The 8253A has three identical and independent 16 bit counters which may be operated in various modes by proper software programming. The counter can count either in binary or BCD and in addition a count can be read by the microprocessor while the counting is going on. Each counter is a negative edge-triggered down counter. Each counter has two input signals-clock (CLK) and GATE and one output signal - OUT.

Address line A_0 and A_1 of the microprocessor are connected to lines A_0 and A_1 of the 8253 and $\overline{CS}$ is tied to a decoded address. A_0 and A_1 input signals, in conjunction with the status of RD and WR inputs, control the selection of counter or the control word register.

CS	$\overline{RD}$	$\overline{WR}$	A_1	A_0	
0	1	0	0	0	LOAD TM0
0	1	0	0	1	LOAD TM1
0	1	0	1	0	LOAD TM2
0	1	0	1	1	DATA BUS → CONTROL
0	0	1	0	0	READ TM0
0	0	1	0	1	READ TM1
0	0	1	1	0	READ TM2

0	0	1	1	1	DATA BUS TRISTATE
1	x	x	x	x	DATA BUS TRISTATE
0	1	1	x	x	DATA BUS TRISTATE
0	0	0	x	x	ILLEGEL CONDITION

Each counter is initialized by writing a proper control word in the control word register. The control word includes the following important features:

i) Mode of operation

ii) 16 bit or 8 bit data to be read or write

iii) 16 bit binary counter or 4 digit BCD counter operation.

The control word format for choosing the above features is given below:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RL1	RL2	M2	M1	M0	BCD

SC1	SC0	
0	0	Select counter 0
0	1	Select counter 1
1	0	Select counter 2
1	1	Illegel condition

RL1	RL0	
0	0	Counter latching operation
0	1	Read/load least significant byte only
1	0	Read/load most significant byte only
1	1	Read/load least significant byte first, then the most significant byte.

M_2	M_1	M_0	
0	0	0	Mode 0
0	0	1	Mode 1
x	1	0	Mode 2
x	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD

0	16 bit binary counting
1	4 digit BCD counting

8255A PROGRAMMABLE PERIPHERAL INTERFACE

Intel 8255A is a widely used general purpose programmable parallel input/output device. It can be programmed to transfer data under various conditions, from simple I/O to interrupt I/O. It is fexible, versatile, economical and can be used with almost any microprocessor. 8255A has three 8 bit parallel ports : PORTA, PORTB & PORTC. The eight bit of port C can be used as individual bits or be grouped in two 4 bit ports : C_{upper} (C_u) and C_{lower} (C_L).

A_0 and A_1 input signals, in conjunction with the RD and WR inputs, control the selection of one of the three prrts or the control word register as follows:

M_2	M_1	M_0	
0	0	0	Mode 0
0	0	1	Mode 1
x	1	0	Mode 2
x	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD

0	16 bit binary counting
1	4 digit BCD counting

8255A PROGRAMMABLE PERIPHERAL INTERFACE

Intel 8255A is a widely used general purpose programmable parallel input/output device. It can be programmed to transfer data under various conditions, from simple I/O to interrupt I/O. It is fexible, versatile, economical and can be used with almost any microprocessor. 8255A has three 8 bit parallel ports : PORTA, PORTB & PORTC. The eight bit of port C can be used as individual bits or be grouped in two 4 bit ports : C_{upper} (C_u) and C_{lower} (C_L).

A_0 and A_1 input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word register as follows:

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	
0	0	1	0	0	PORTA → DATA BUS
0	0	1	0	1	PORTB → DATA BUS
0	0	1	1	0	PORTC → DATA BUS
0	1	0	0	0	DATA BUS → PORTA
0	1	0	0	1	DATA BUS → PORTB
0	1	0	1	0	DATA BUS → PORTC
0	1	0	1	1	DATA BUS → CONTROL
0	x	x	x	x	DATA BUS → TRISTATE
0	0	1	1	1	ILLEGEL CONDITION
0	1	1	x	x	DATA BUS → TRISTATE

Each of the ports of 8255A can be initiatized in various mode by writing a proper control format in the control word register.

8259A PROGRAMMABLE INTERRUPT CONTROLLER

The intel 8259A programmable interrupt controller can manage eight interrupts according to the instruction written into its control registers. 8259A is designed to minimize the software and real time overhead in handling multi-level priority interrupts.

For programming, 8259A requires two types of command words. Initialization command words (ICWS) and operational command words (OCWS). The 8259A can be initialized with four ICWS; the first two are essential, and the other two are optional based on the modes being used. These words must be issued in a given sequence. Once initialized,

the 8259A can be set up to operate in various modes by using three different OCWS. These modes are:

i) Fully rested mode
ii) Rotating priority mode
iii) Specified mask mode
iv) Polled mode.

If the 8259A is programmed in fully rested mode, IR_0 has the highest priority and IR_7 has the lowest priority.

2.3.3 Interfacing of Programmable Interval Timer 8253A:

The present scheme requires four counters. In the vinytics VMC-85 trainer kit, two counters of 8253A are available to the user through connector J_1. An intel 8253A programmable interval timer is therefore interfaced with 8085A microprocessor using minimum hardware components to meet the requirements of the counters. The interfacing circuit is shown in Fig. 2.4. The $\overline{CS}$ signal is derived from a 3 line to 8 line decoder 74LS138. The A_3, A_4, A_5, A_6 & A_7 address lines of 8085A are connected directly to the required pins of 74LS138. The $\overline{RD}$, $\overline{WR}$ and IO/$\overline{M}$ control signals are derived directly from the control bus of the microprocessor. The select inputs A_0, A_1 are connected to the A_0, A_1 address bus signals of the CPU. The ports addresses for the 8253A are selected as follows:

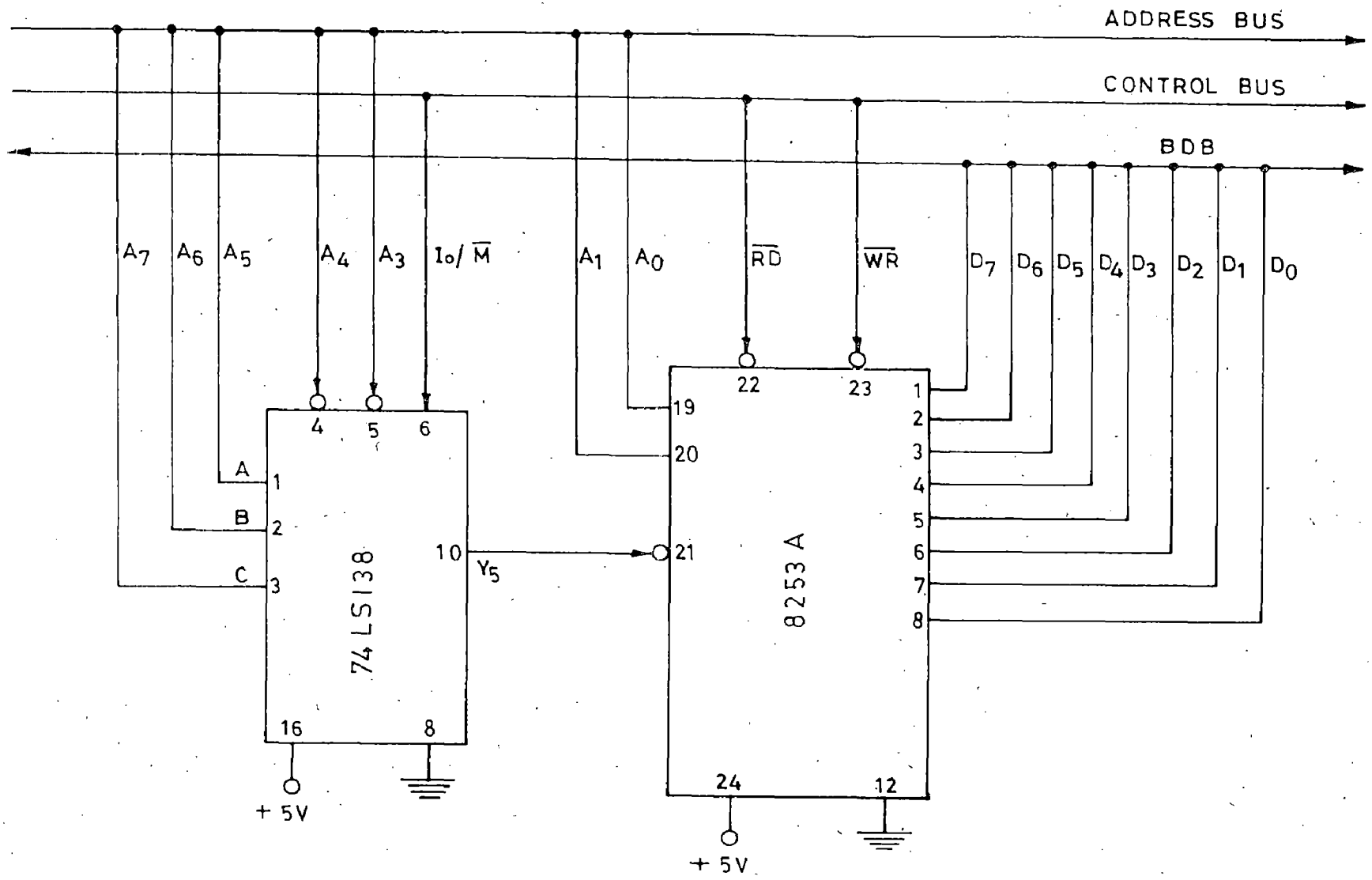


FIG. 2·4—INTERFACING OF PROGRAMMEABLE INTERVAL TIMER 8253 A

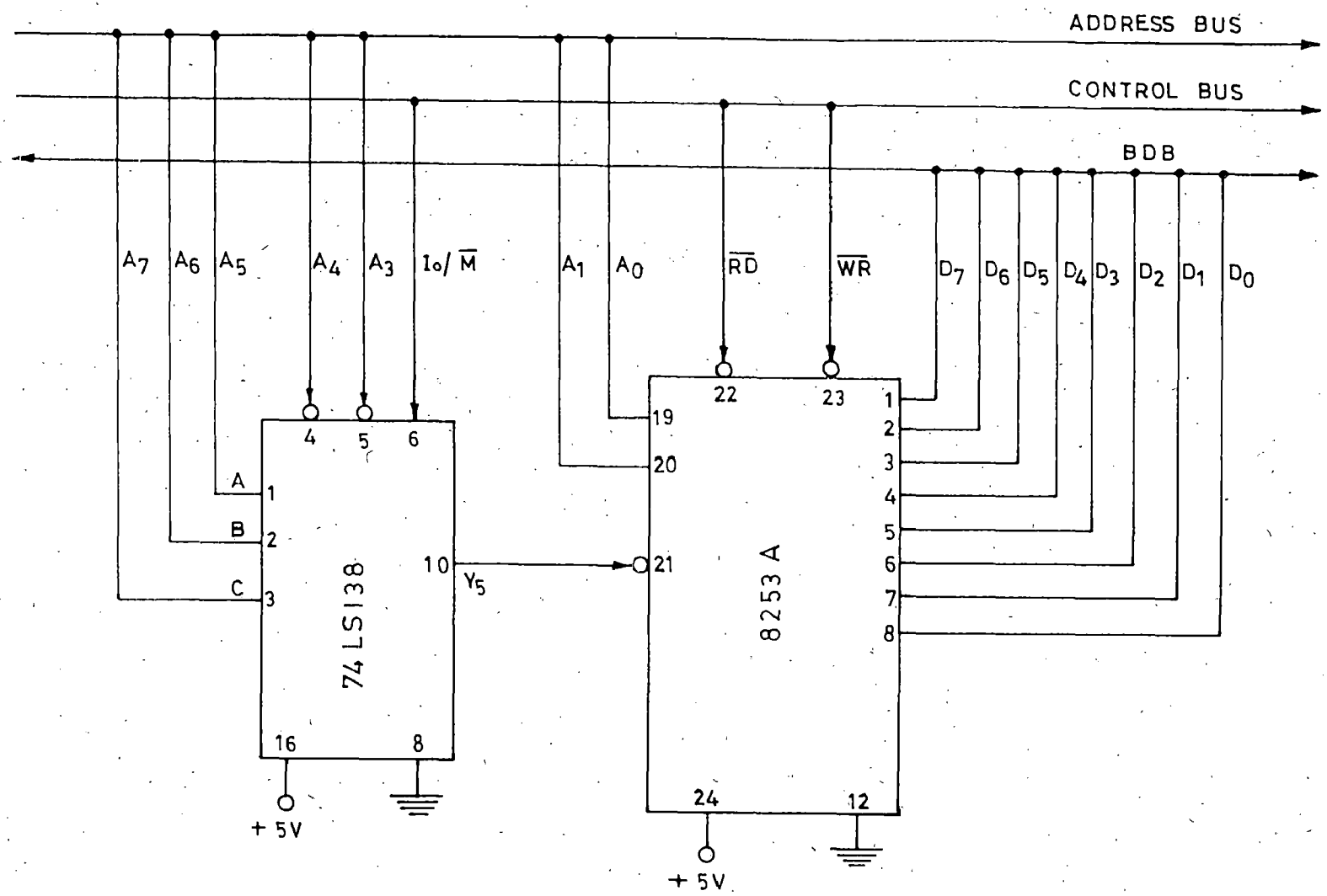


FIG. 2·4—INTERFACING OF PROGRAMMEABLE INTERVAL TIMER 8253 A

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	0	1	0	0	0	0	0	A0	TM0
1	0	1	0	0	0	0	1	A1	TM1
1	0	1	0	0	0	1	0	A2	TM2
1	0	1	0	0	0	1	1	A3	CONTROL WORD
1	0	1	0	0	1	0	0	A4	TM0
1	0	1	0	0	1	0	1	A5	TM1
1	0	1	0	0	1	1	0	A6	TM2
1	0	1	0	0	1	1	1	A7	COUNTROL WORD

PORT ADDRESS

A0 and A4 → TM0
A1 and A5 → TM1
A2 and A6 → TM2
A3 and A7 → CONTROL WORD

2.3.4 Synchronizing Technique:

Synchronizing signal is generated by sensing line to line voltages V_{AC} and V_{CB} of the synchronous machine terminals. This signal has pulses of 60° duration corresponding to machine voltage frequency at every 360° interval. This signal provide the informations about frequency of the machine voltage, direct 60° delay count and instant of loading a counter of 8253A with firing angle delay count. Synchronizing signal is required for generating firing pulses for inverter thyristors in proper sequence. Synchronizing circuit uses less no of components and is shown in Fig. 2.5. This circuit consists of the following components.

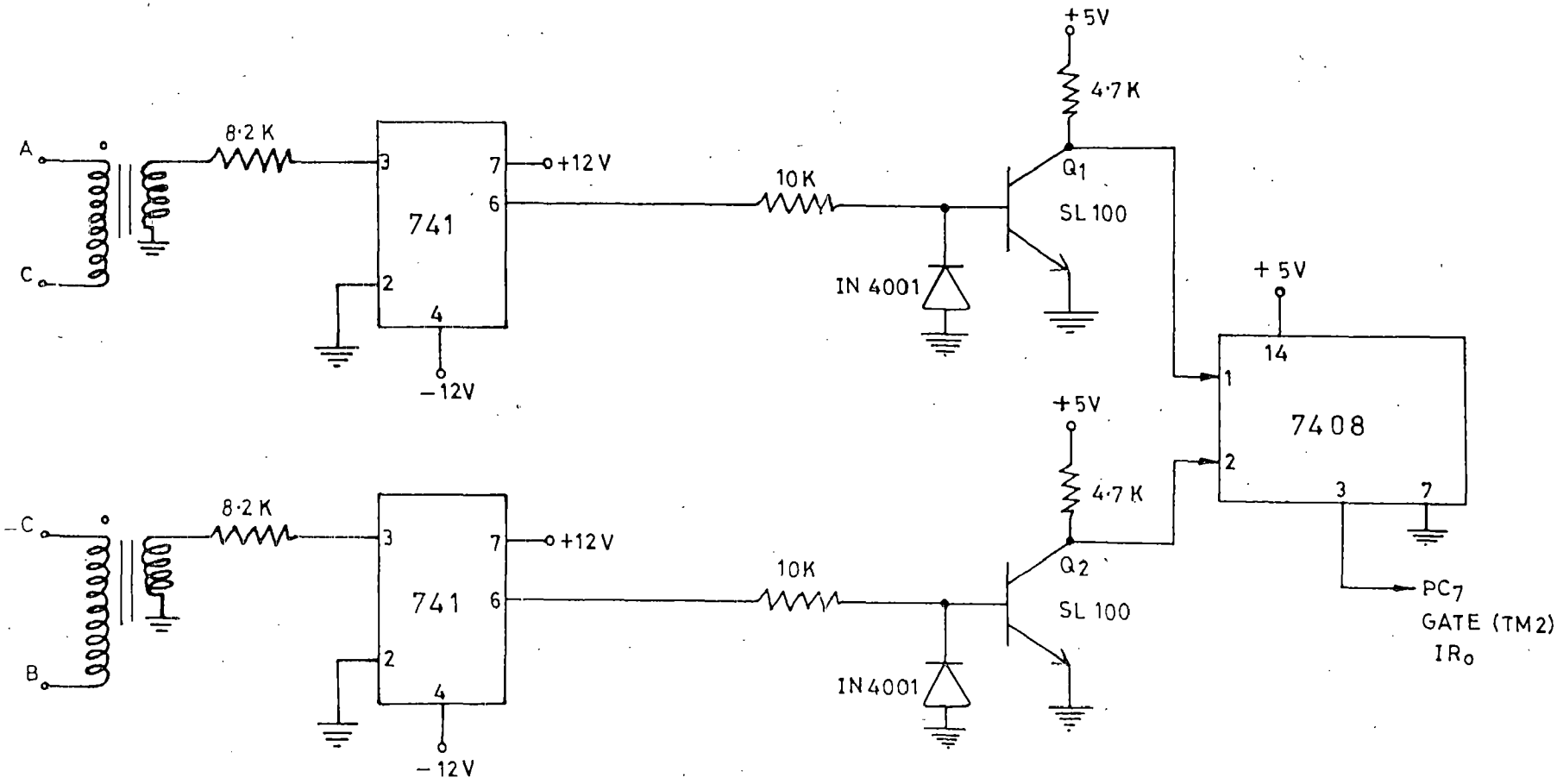


FIG. 2·5—SYNCHRONIZING CIRCUIT

i) Step down transformer

ii) Comparator

iii) Transistor drive

iv) AND gate

(i) Step Down Transformer:

This is a single phase 440/6V transformer to realize voltage sensor for a wide range of frequency. The primary winding is connected directly to the machine terminals and secondary goes to non-inverting terminal of the comparator. Primary and secondary connections are made in such a way so that secondary voltage is 180^{o} out of phase with respect to primary voltage. One terminal of the secondary of both transformer is connected to system ground.

(ii) Comparator:

Comparator circuit has been made with the help of operational amplifier IC 741. The inverting terminal of IC 741 is connected to common ground. The output of the comparator ideally swings between +12 to -12V at every zero crossing of machine terminal voltages and output frequency is the same as the machine voltage frequency. The output of comparator is reduced to a lower voltage by a series connected register and applied to the base of the transistor.

(iii) Transistor Drive:

The stage is very important and required to interface the analog system to a digital system. Transistor

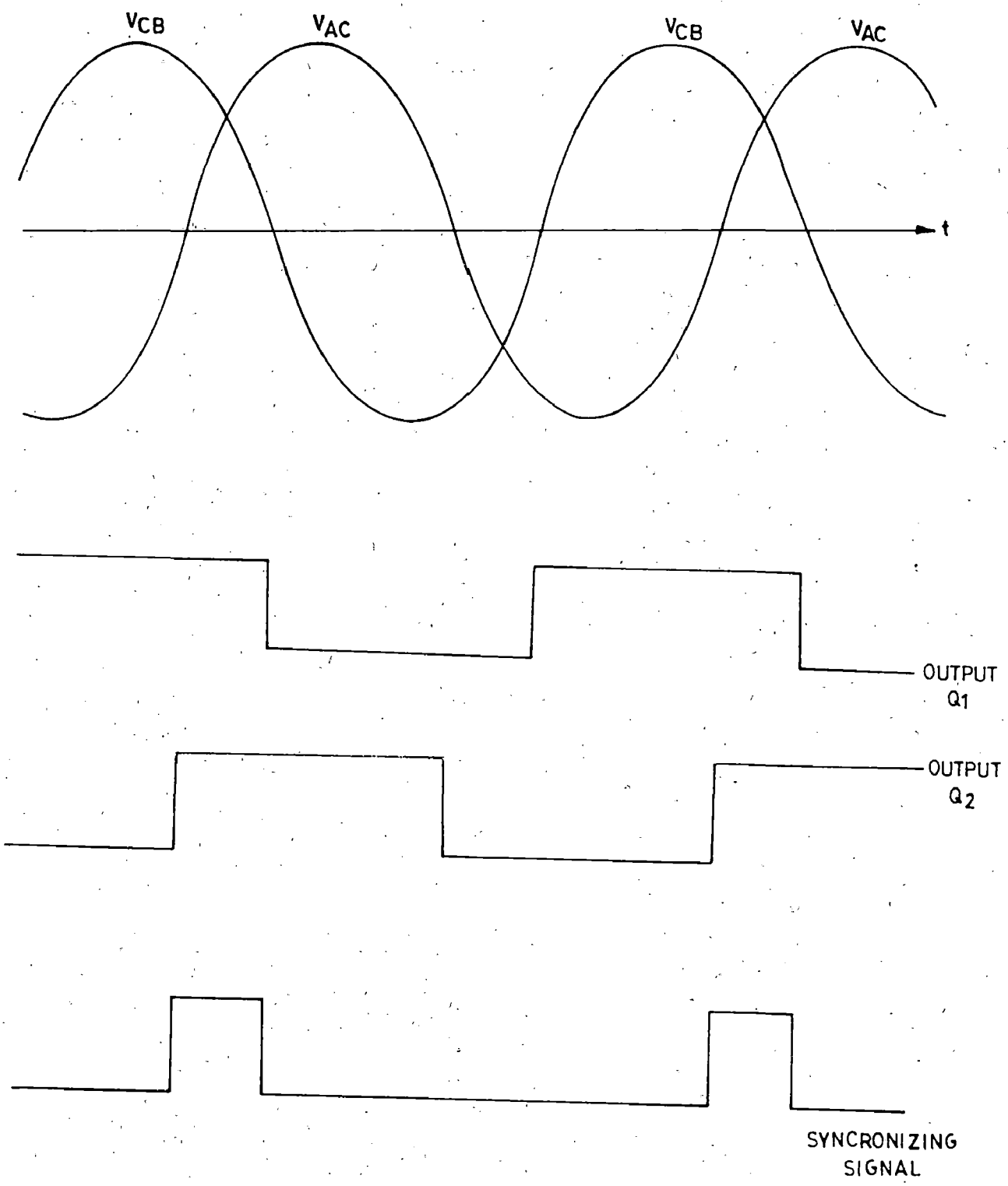


FIG. 2-6—VOLTAGE WAVE SHAPES AT DIFFERENT POINTS OF SYCHRONIZING CIRCUIT.

is used to control the state of the TTL input. The output of the op amp swings from +12V to -12V. The positive swing drives the transistor into saturation, producing a TTL input of approximately OV. The negative swing drives the transistor into cut-off, producing a TTL input of +5V. Thus the transistor inverts the input control signal. TTL outputs of transistors are shown in Fig. 2.6.

The diode in the base circuit protects the base against excessive reverse voltage. Since the negative output of the comparator approaches -12V, we need to use a protective diode as shown in Fig. 2.5 between the base and ground. This diode clamps the base voltage at approximately -0.7V on the negative swing.

(iv) AND Gate:

IC 7408 two input AND gate is used for necessary AND operation. The synchronizing signal is obtained after ANDING two output signals of the transistors. The microcomputer makes use of this signal for generating firing pulses in proper sequence and firing angle control.

2.3.5 Microprocessor Based Firing Control Scheme:

Microprocessor based firing scheme is used for generating the firing pulses for inverter thyristors in proper sequence decided by the control circuit and system software. This scheme has several advantages over the analog

firing control scheme. An analog firing scheme using voltage sensor used for the line commutated inverter fed synchronous machine has the following disadvantages:

i) Non-linear variation of firing angle using cosine wave crossing firing control.

ii) The commutation spike in the machine terminal voltages can generate additional firing pulses leading to mis-firing of thyristor.

iii) Variation of firing angle is limited to 90^{o} by using cosine firing scheme.

iv) Hard wired logic circuitry fixes the firing scheme philosophy and any change, if necessary, cannot be made without changing the circuit.

These drawbacks of the analog firing scheme can be overcome by using a microprocessor based firing control scheme. The hardware configuration of the microcomputer based scheme is shown in Fig. 2.7. This scheme is developed using vinytics VMC-85 trainer kit. This scheme requires less number of hardware components and simple synchronizing technique. The microcomputer uses two programmable interval timers 8253A, one programmable peripheral interface 8255A and one programmable interrupt controller 8259A. The synchronizing signal derived from machine terminal voltages is inputted to PC7 of 8255A, Gate2 of 8253A(1) and IR0 pin of 8259A. Microprocessor checks up the status of the synchronizing signal through PC7 bit just after the initialization of all programmable peripheral devices such as 8253A,

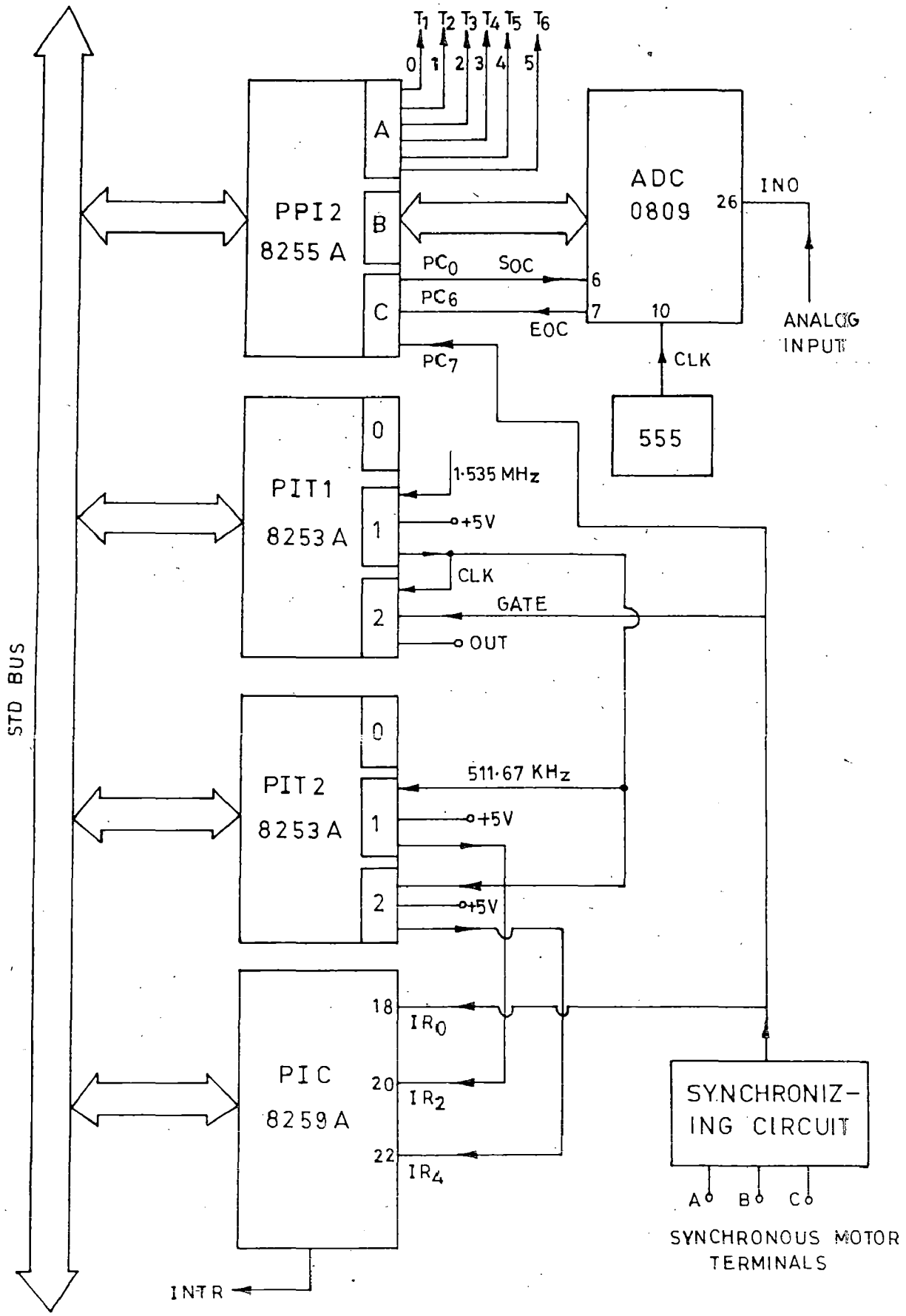


FIG. 2·7—MICROPROCESSOR BASED FIRING CONTROL SCHEME FOR COMMUTATORLESS DC SERIES MOTOR

8255A and 8259A to fix up the proper instant of loading the counter TM2 of PIT1 with FFFFH during the execution of the main program.

Counter TM2(1), TM1(2) and TM2(2) get the same clock of 511.67 KH_Z. This clock is obtained by operating the counter TM1(1) in mode 2 from a clock of 1.535 MH_Z. ADC 0809 is interfaced to the microprocessor through port B and port C of 8255A. ADC provides information about firing angle of the inverter. The details of ADC 0809 interfacing have been given in Appendix - II. The firing pulses for the inverter thyristors are outputted through port A of 8255A as per firing command word. The firing angle can be changed linearly by varying analog input to the ADC through a 4.7K pot connected in series to a 8.2K resistor.

All the counters except TM1(1) are programmed in mode 0. TM2(1) provides the 60° count corresponding to the clock 511.67 KH_Z. Counter TM1(2) is used to load firing angle delay count and its output provides the IR_2 interrupt control signal input. Counter TM2(2) is loaded with 60° delay count at proper instant by software control and its output on the terminal count is used as IR_4 interrupt signal input for 8259A. The outputs of counter TM1(2) and TM2(2), synchronizing signal and generation of firing pulses are shown in Fig. 2.8. The duration of firing pulses generated by the microcomputer via 8255A is very small. The firing pulse duration is increased to 0.72 ms through a monostable

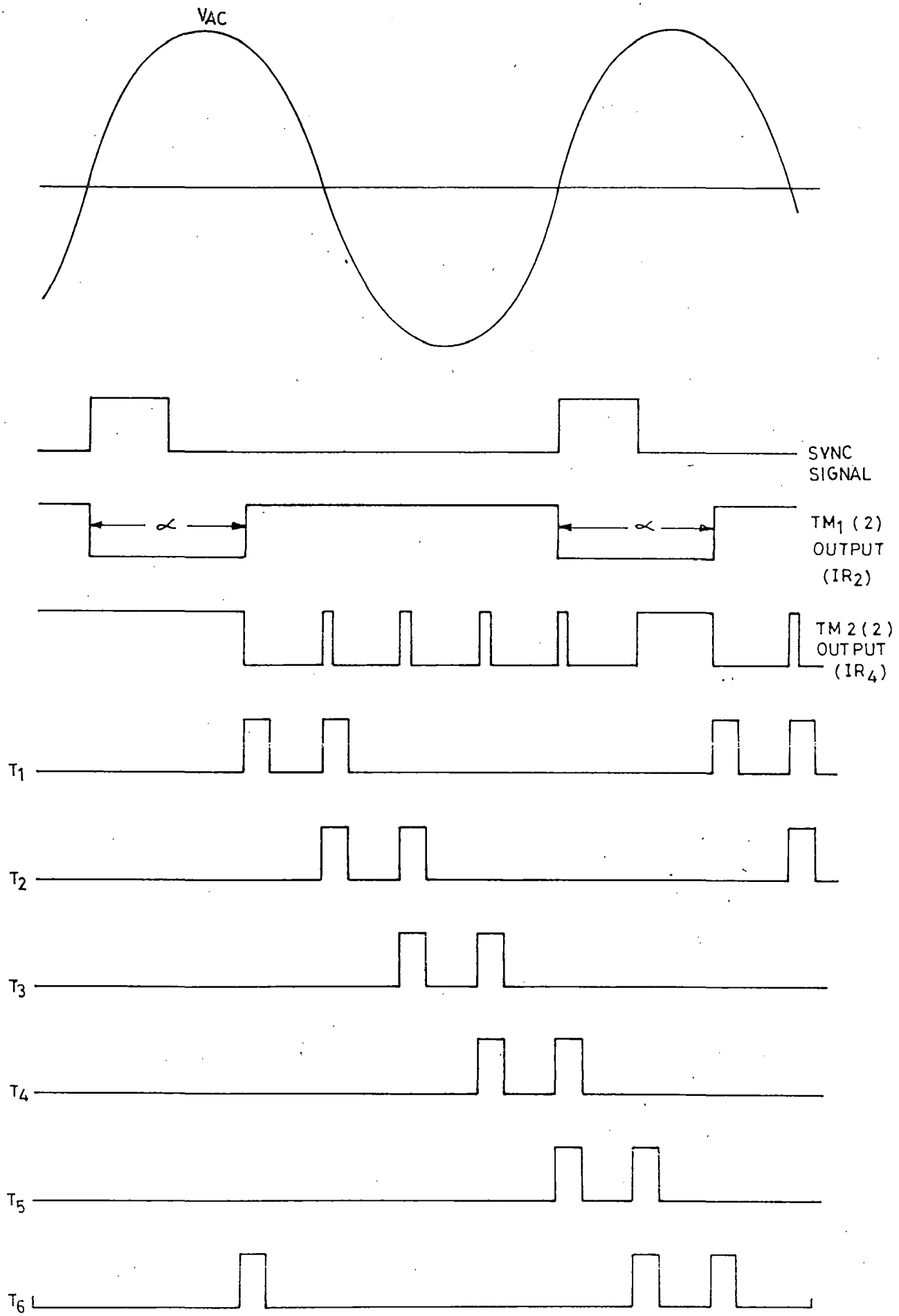


FIG. 2·8–SYNCHRONIZING SIGNAL, IR_2 & IR_4 INTERRUPT SIGNALS AND FIRING PULSES IN PROPER SEQUENCE

circuit. These firing pulses are amplified using a pulse amplifier circuit which is described in the following section. In LCI, each thyristor has to conduct for two consecutive modes of 60° duration. This scheme uses gating of each SCR twice at the interval of 60°. This avoid the possibility of failure of inverter operation in the presence of discontinuous operation.

2.3.6 Design of Pulse Amplifier Circuit:

The duration of firing pulses generated by the microprocessor via port A of 8255A is not sufficient to trigger inverter thyristors. The required pulse width is obtained using monostable circuit. If the firing pulse width is programmed to be 0.73 ms through software, microprocessor will remain in the delay routine for this duration and therefore in the higher frequency, it may not be able to execute the whole program. This difficulty is over-come by using monostable circuit. The output of the monostable is applied to the pulse amplifier circuit. Pulse amplifier circuit consists of the following components:

i) Monostable multivibrator
ii) Oscillator
iii) AND gate
iv) Pulse amplifier

Pulse amplifier circuit for one channel is shown in Fig. 2.9.

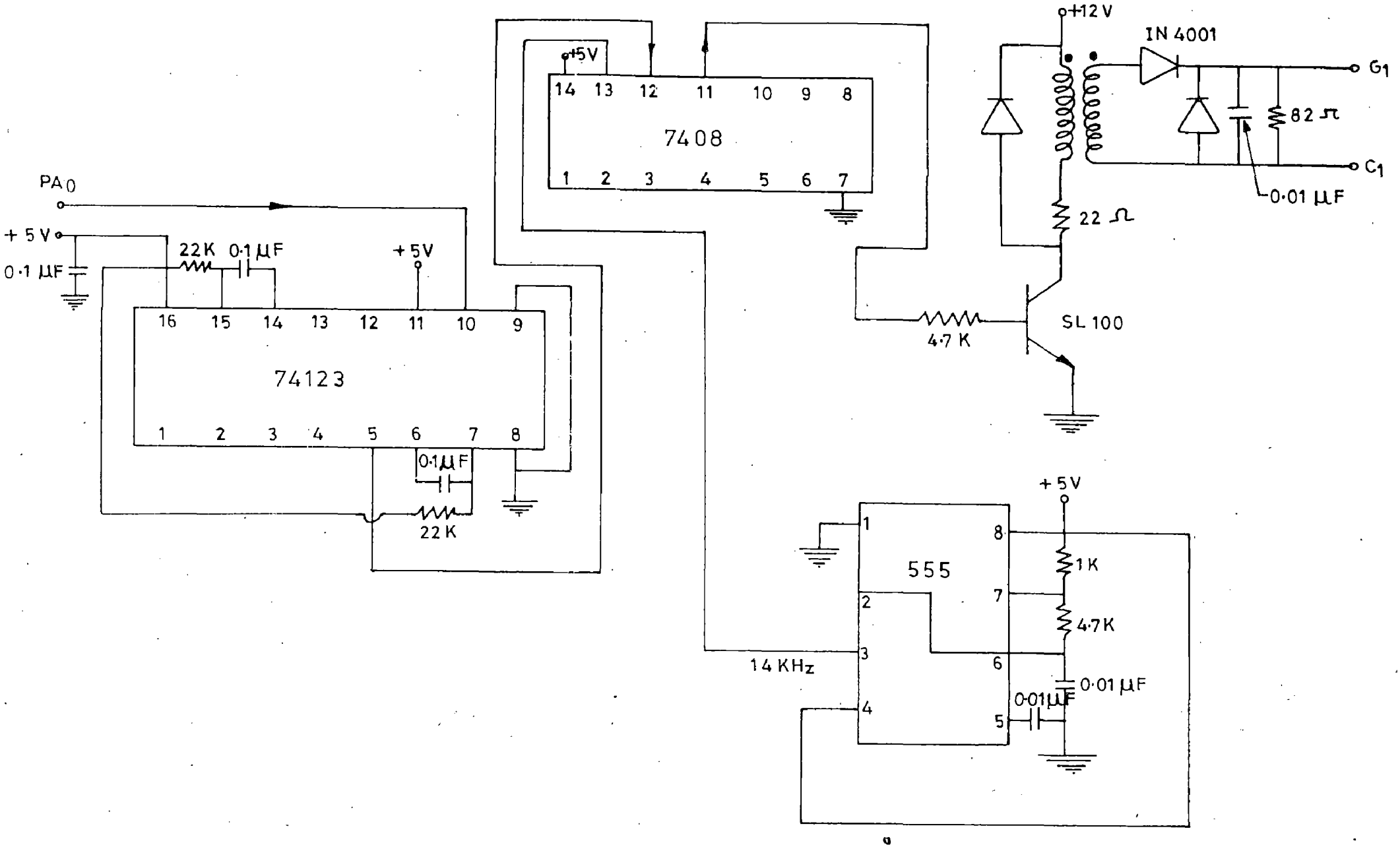


FIG. 2·9 – PULSE AMPLIFIER CIRCUIT FOR ONE CHANNEL

(i) Monostable Multivibrator:

A 74123 retriggerable monostable multivibrator is used to produce an output pulse of 0.73 m sec. The values of the externally connected elements R and C of the pulse forming circuit of 74123 determine the pulse width. The monostable is designed to operate in rising edge triggering mode. For 74123, the pulse duration is given by

$$T_W = 0.33\ RC$$

The elements R and C are selected as 22K ohm and 0.1 uF respectively to give a pulse width of 0.72 m sec.

(ii) Oscillator:

IC 555 timer is used for oscillator. The external capacitor and resistor R_A and R_B determine the frequency of oscillation. The duty cycle may be set precisely by the ratio of these two resistors. For IC 555 timer frequency is given by

$$f = \frac{1.44}{(R_A + 2R_B)\ C_T}$$

Let the oscillator frequency be 14 KH_Z taking $C_T = 0.01\ \mu F$, the values of R_A and R_B are obtained as follows:

$$R_A = 1K \text{ and } R_B = 4.7K$$

(iii) AND Gate:

The output of the monostable multivibrator and oscillator is ANDED in the AND gate. IC 7408 two input

AND gate is used for AND operation. The reason for high frequency modulation is obvious. If the pulse is long, they may saturate the pulse transformer and the firing pulse may be distorted. The duty cycle is kept less than 50 percent, so that flux in the transformer can reset. The modulated pulse also reduces the gate dissipation.

(iv) Pulse Amplifier:

The output of the AND gate is applied to the base of the transistor through 4.7K resistor. The input signal is amplified through the amplifier as shown in Fig. 2.9.

The gate and cathode terminals of SCR are connected to the power circuit of higher patentials. Therefore, the control circuit should not be directly connected to the power circuit. A pulse transformer is used for electrical isolation between control circuit and power circuit as shown in Fig. 2.9. The pulses at the transistor collector is the amplified inverted form of the input signal. But the isolating transformer connection are made in such a way so that the final firing pulse has no phase shift with respect to input pulse. A diode is connected across the transformer primary to avoid saturation of the pulse transformer. Another diode is connected in series with secondary of pulse transformer to block negative pulse. The diode across the primary also serves to protect the transistor. The capacitor at the secondary prevents any spurious high

frequency from triggering the thyristor. The gate of the thyristor can be protected from long reverse voltage by connecting a diode across the gate.

2.4 STARTING METHOD OF COMMUTATORLESS D.C. SERIES MOTOR

Under standstill condition, synchronous motor terminal voltage is zero and therefore firing pulse generation is not possible. So the synchronous motor is unable to start from standstill condition. Extra starting methods are necessary to start the synchronous machine from standstill. This is the major drawback of induced voltage commutated inverter fed synchronous motor drives. For commutatorless d.c. series motor, field winding is connected in series with the d.c. link inductor. So d.c. link current and machine speed must be necessary to induce sufficient voltage in the stator winding for generating firing pulses. Several methods are known for starting purpose. But in the present work, a manual starting method shown in Fig. 2.10 has been adopted. The manual method of starting commutatorless D.C. series motor involved the following steps:

i) A D.C. motor is started to drive the synchronous machine as a generator at a lower speed of about 1000 r.p.m. Now d.c. link current is zero and the induced voltage due to residual magnetism is very small. So proper synchronizing signal will not be generated from this low voltage.

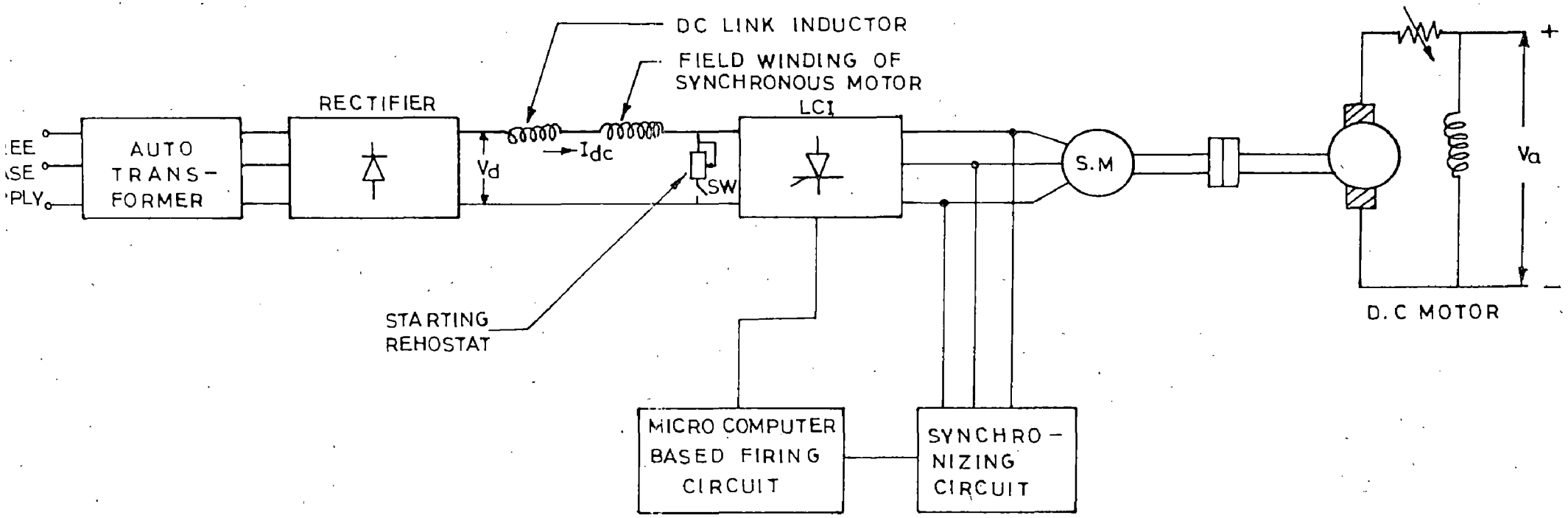


FIG. 2·10 – STARTING OF COMMUTATORLESS DC SERIES MOTOR

ii) A variable resistor as shown in Fig. 2.10 is connected across the inverter to allow current flowing through the field winding of the synchronous motor during starting. Now switch SW is closed and some d.c. current is passed through field winding by controlling d.c. link voltage by a three phase auto transformer.

iii) Synchronizing signal is now generated from the no load induced emf of the generator. Microcomputer proceeds to execute the software program for generating firing pulses according to firing command word.

iv) A d.c. voltage is produced at the d.c. terminal of the inverter bridge. As the firing angle is greater than 90^{o}, upper terminal is positive and lower one is negative. The D.C. link voltage is increased gradually and power flows from d.c. side to the synchronous machine when the bridge rectifier voltage becomes greater than the inverter output voltage.

v) The current flowing into the inverter is indicated by the D.C. link ammeter, Thus the synchronous machine starts drawing active power from the D.C. link resulting in a corresponding decrease of D.C. motor current.

vi) Power supply to the D.C. motor is switched off and the resistance of the starting resistor is gradually increased. The switch SW is made off later on and the system works as a commutatorless D.C. series motor.

In this scheme, the no load induced voltage is always greater than the terminal voltage of the synchronous machine. Therefore, the synchronous motor operates like an over excited mode drawing current at leading power factor.

2.5 CONCLUSIONS

The details of microcomputer based firing control scheme for the commutatorless D.C. series motor using induced voltage commutation technique has been discussed in this chapter. The design of power circuit and synchronizing circuit are also developed. A special explanation of interfacing a programmable interval timer 8253A has been given in this chapter. The manual method of starting commutatorless D.C. series motor is also discussed.

CHAPTER - III

IMPLEMENTATION OF SYSTEM SOFTWARE AND FLOW CHARTS

3.1 GENERAL

The development of system software and flow-charts for the microprocessor based firing control scheme is discussed in this chapter. The complete logic of the scheme is described in the main program, routine. The various subroutines used in conjunction with the main program are also discussed in this chapter.

3.2 MAIN PROGRAM ROUTINE

The flow-chart for the main program is shown in Fig.3.1. The program is started with the initialization of programmable peripheral interface 8255A. The ports of 8255A are programmed as input mode or output mode according to the requirements for the present scheme. The port A is programmed for outputting firing pulses as per firing command word. The port B is programmed to import the ADC output. The port C_L is selected as output mode and port C_U as input mode. The counters of programmable interval timer 8253A also are to initialized in the suitable mode as required by the user. In the vinytics VMC-85 up trainer, one counter of 8253A is used for single step operation and two other counters are available to the user through connector J1. Out of

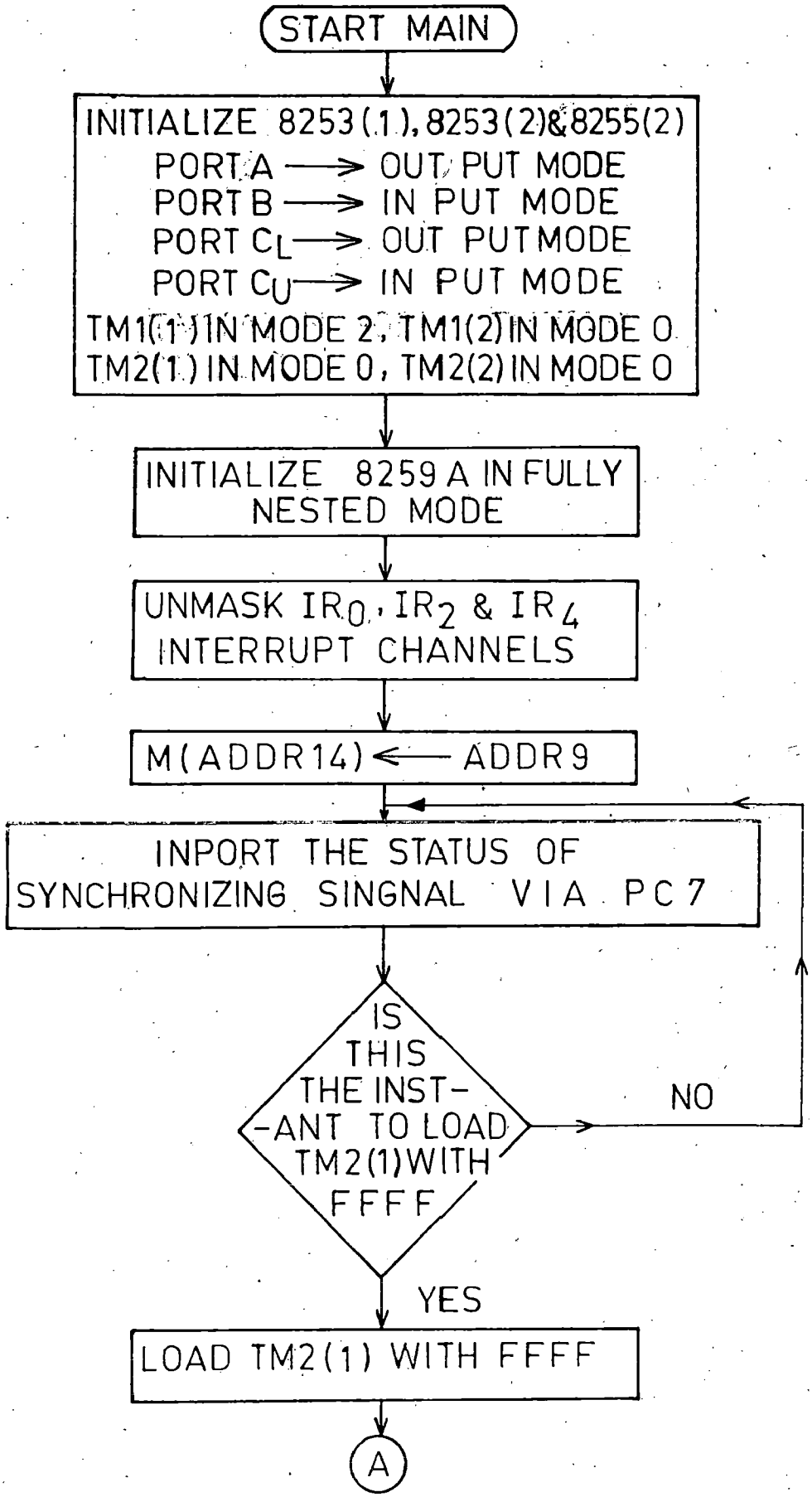
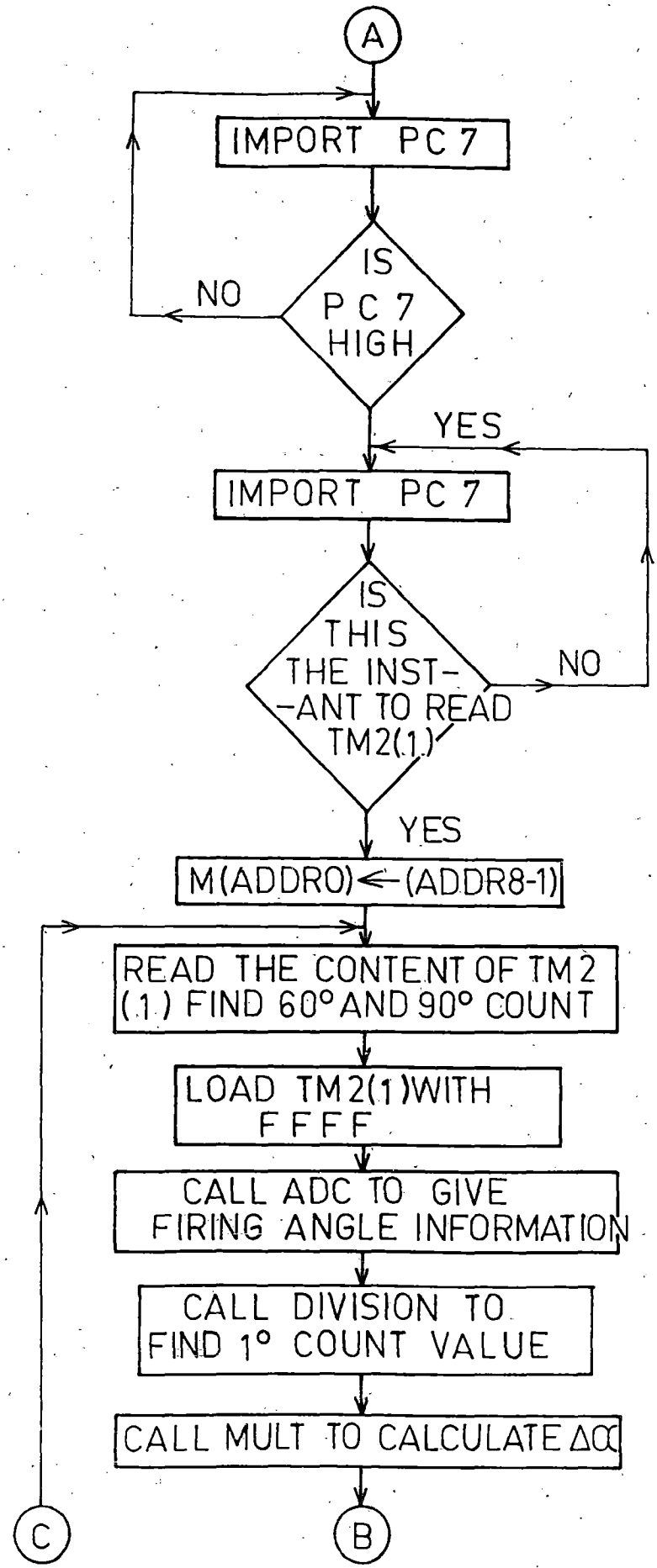
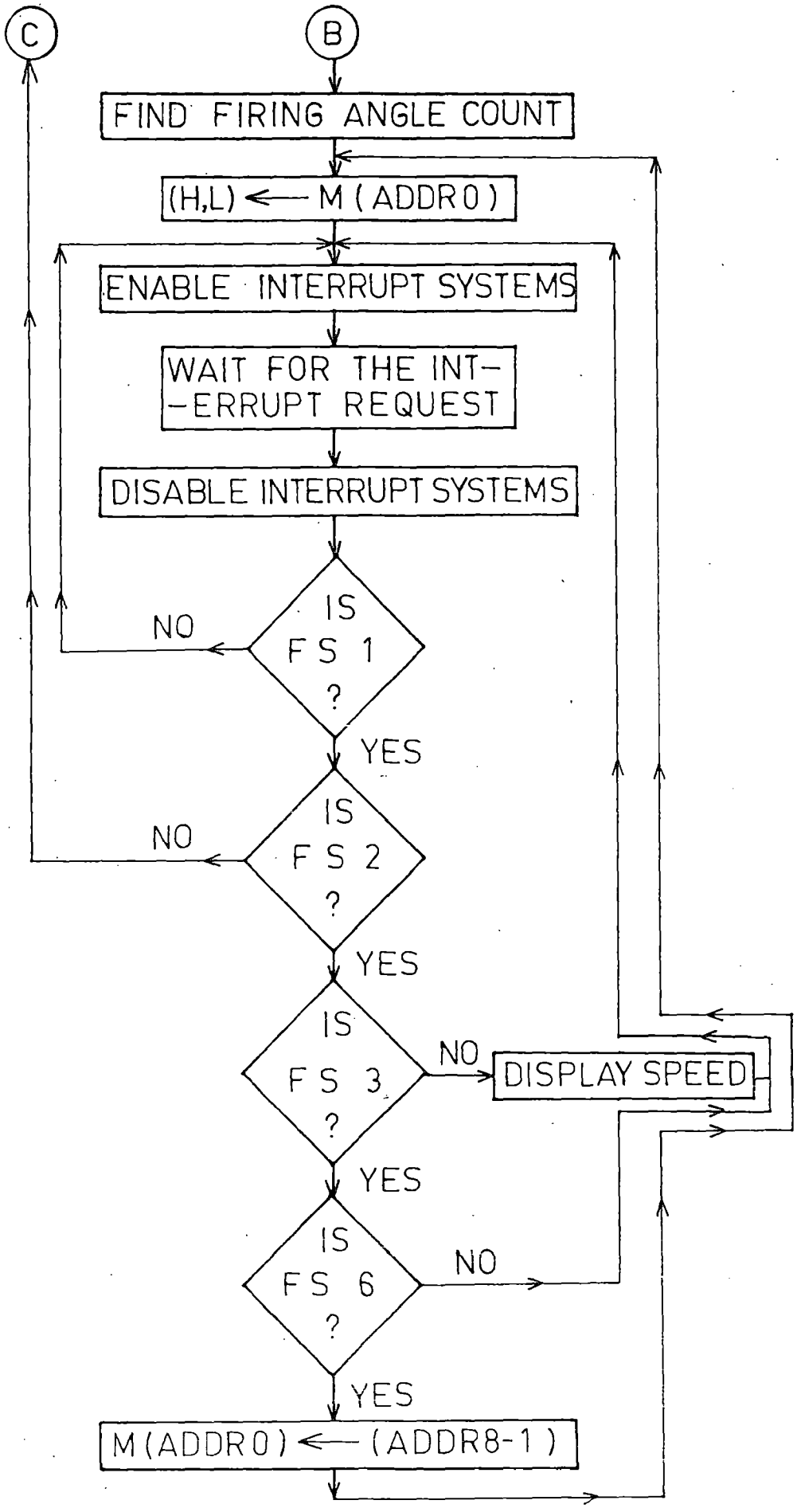


FIG. 3.1 FLOW CHART FOR MAIN PROGRAM


A
IMPORT PC 7
IS PC 7 HIGH
NO
YES
IMPORT PC 7
IS THIS THE INST--ANT TO READ TM2(1)
NO
YES
M(ADDR0)←(ADDR8-1)
READ THE CONTENT OF TM2 (1) FIND 60° AND 90° COUNT
LOAD TM2(1)WITH FFFF
CALL ADC TO GIVE FIRING ANGLE INFORMATION
CALL DIVISION TO FIND 1° COUNT VALUE
CALL MULT TO CALCULATE Δα
C
B


C
B
FIND FIRING ANGLE COUNT
(H,L) ← M (ADDR 0)
ENABLE INTERRUPT SYSTEMS
WAIT FOR THE INT-
-ERRUPT REQUEST
DISABLE INTERRUPT SYSTEMS
IS
F S 1
?
NO
YES
IS
F S 2
?
NO
YES
IS
F S 3
?
NO
DISPLAY SPEED
YES
IS
F S 6
?
NO
YES
M(ADDR 0) ← (ADDR 8-1)

these counters, TM1(1) is programmed in mode 2 for generating the clock of 511.67 KH_z by using the clock of 1.535 MH_z and other counter TM2(1) programmed in mode 0 for providing 60^o count corresponding to clock 511.67 KH_z. The counter TM1(2) and TM2(2) of another programmable interval timer 8253A interfaced by the author are initialized in mode 0. The output of TM1(2) and TM2(2) are used as IR_2 and IR_4 interrupt requests for generating firing pulses.

After the initialization of 8255A in simple input/output mode and counters of 8253A(1) and 8253A(2) in mode 0, all port bits and counter outputs become low. After the initialization of 8253(1), the counter TM1(2) is loaded with count 03H to generate the clock of 511.67 KH_z continuously and this clock remains at a constant frequency of 511.67 KH_z duration the operation of the system.

The programmable interrupt controller 8259A is initialized in fully nested mode. All the interrupt input pins of 8259A are available to the user through the connector J_1. In fully nested mode IR_0 has the highest priority and IR_7 has the lowest priority. In the present scheme three interrupt lines: IR_0, IR_2 and IR_4 are used. After the initialization of 8255, 8253 and 8259, three interrupt input channels are enabled through operational control word 1 (OCW1).

Now the microprocessor checks the status of the synchronizing signal imported via PC_7. If it is found

to be low then $FFFF_{16}$ is loaded into the counter TM2 of 8253A(1). Synchronizing signal is inputted continuously to the gate of TM2(1) and counting becomes enable as soon as the digitized signal goes to high. The counter starts decrementing the count value FFFFH with respect to the clock of 511.67 KH_z. The counter continues counting as long as synchronizing signal remains high and counting becomes disable as soon as synchronizing signal goes to low. Under this condition counter output remains low.

The address, ADDR8-1 is stored in the memory location ADDR0 where ADDR8 is the starting address of the firing command table. Now the present content of the counter TM2(1) is read and the count value for 60^o duration of terminal voltage of the synchronous machine is calculated. The 30^o count value is found by rotating right the 60^o count value by one bit in register pair HL. The 90^o count value is calculated by adding 30^o count value with 60^o count value. These 60^o and 90^o counts exactly correspond to the 60^o and 90^o durations of the synchronous machine terminal voltage. Memory location ADDR1 and ADDR2 are used to store the 60^o and 90^o count value respectively which will be used later on. The counter TM2(1) is reloaded with FFFFH for the next synchronizing pulse of 60^o duration. The firing angle delay count is calculated according to the following equation:

$$\alpha = 90^{\circ} \text{ count} + \frac{90^{\circ} \text{ Count} \times \text{ADC output}}{5\text{ AH}} \quad \ldots.(3.1)$$

or $\alpha = 90^{\circ}$ count + 1°count x ADC output ....(3.2)

or $\alpha = 90^{\circ}$ count + $\Delta\alpha$ ....(3.3)

where $\Delta\alpha = 1^{\circ}$ count x ADC output

The 1° count is obtained by DIVISION subroutine. The multiplication of 1° count value and ADC output is performed by MULT subroutine.

After calculating 60° and 90° count, the program jumps to ADC subroutine. During the execution of this subroutine, ADC converts a particular analog input to it through the channel IN0 into its equivalent digital signal and this output is stored in the memory location ADDR6. This digital output contains the information about the firing angle of the inverter thyristors. ADC output is allowed to vary from 00H to 5AH. If the ADC output varies from 00H to 5AH, the corresponding firing angle changes linearly from 90° to 180°.

The program moves to DIVISION subroutine. During the execution of this program, the 90° count value is divided by 5AH. Thus this subroutine provides the 1° count value. This count exactly corresponds to 1° of the machine terminal voltage. Now the program jumps to the MULT subroutine. In this subroutine, the count value for 1° is multiplied by the ADC output. Thus this subroutine

gives the count value above the 90^{o} count for a particular setting of firing angle of the inverter. The exact count value for the firing angle is calculated by adding 90^{o} count with the product obtained from MULT subroutine and it is stored in the memory location ADDR7. The equation (3.2) indicates that by varying analog input to the ADC, the firing angle can be controlled easily during the operation of the system. In this control scheme, firing angle remains constant with the variation of synchronous motor speed provided the analog input is set at a fixed value.

After calculating the firing angle count, the interrupt system is made enable by executing the instruction EI and CPU waits in the HALT state for the interrupt signal IR_0. The synchronizing signal is also used as IR_0 interrupt signal. The low to high transition of the synchronizing pulse interrupts the microprocessor. As a result the microprocessor branches to the IR_0 interrupt service routine saving return address on the top of the stack upto which it is full. In this service routine, the firing angle count is loaded into the counter TM1(2) and after that microprocessor returns to the main program.

After returning to the main program, the interrupt system is made disabled by executing DI instruction and the firing sequence is tested. If the firing sequence '1' is not completed, the processor enables interrupts and goes to HALT state for the IR_2 interrupt request. The

output of the counter TM1(2) goes to high on the terminal count. This high going signal interrupts the microprocessor and the program is transferred to the IR_2 interrupt service routine. In this service routine, firing pulses for thyristor pair (6,1) are generated by the firing command word and 60^{o} delay count is loaded into the counter TM2(2). After that program returns to the interrupted routine and checks the firing sequence. If the firing sequence '2' is not over, microprocessor reads the content of the counter TM2(1) for new 60^{o} count and calculates the new firing angle count and goes to HALT state after enabling interrupt systems.

The output of the counter TM2(2) becomes high on terminal count and interrupts the microprocessor. The program jumps to the IR_4 interrupt service routine. During the execution of this service routine, the appropriate pair of thyristors are triggered by issuing the proper firing pulses as per command word from its respective firing command address. The counter TM2(2) is reloaded with 60^{o} delay count and the processor returns to the main program.

In the main program, microprocessor checks the firing sequence. If the firing sequence '3' is not over, the program is transferred to the SPEED subroutine for displaying machine speed in the address field. After executing the SPEED subroutine, the microprocessor returns to the main program where it was interrupted and waits

in the HALT state for interrupt requests.

After returning from the interrupt service routine, every time microprocessor checks up the firing sequence. If all firing commands are executed that means one cycle of inverter operation is over then the memory location ADDRO is initializal with the address ADDR8-1 and microprocessor goes to HALT state after enabling interrupt systems and same process is repeated. IR_0 and IR_4 interrupt request may occur simultaneously. In this case, first the microprocessor branches to the IR_0 interrupt service routine and after completing IR_0 service routine, it will service IR_4 interrupt request.

3.3 ADC SUBROUTINE

This subroutine is used to provide firing angle information for the line commutated inverter. This subroutine is executed once in every cycle of the machine frequency. The firing angle can be changed by varying analog input to ADC. ADC converts the analog input into its digital equivalent. The flow chart for the ADC subroutine is shown in Fig. 3.2. The ADC starts converting the analog signal into digital signal at the instant, when the start of conversion (SOC) bit of ADC goes from low to high. Start of conversion pulse is issued by the microprocessor through PC_0 bit of 8255A.

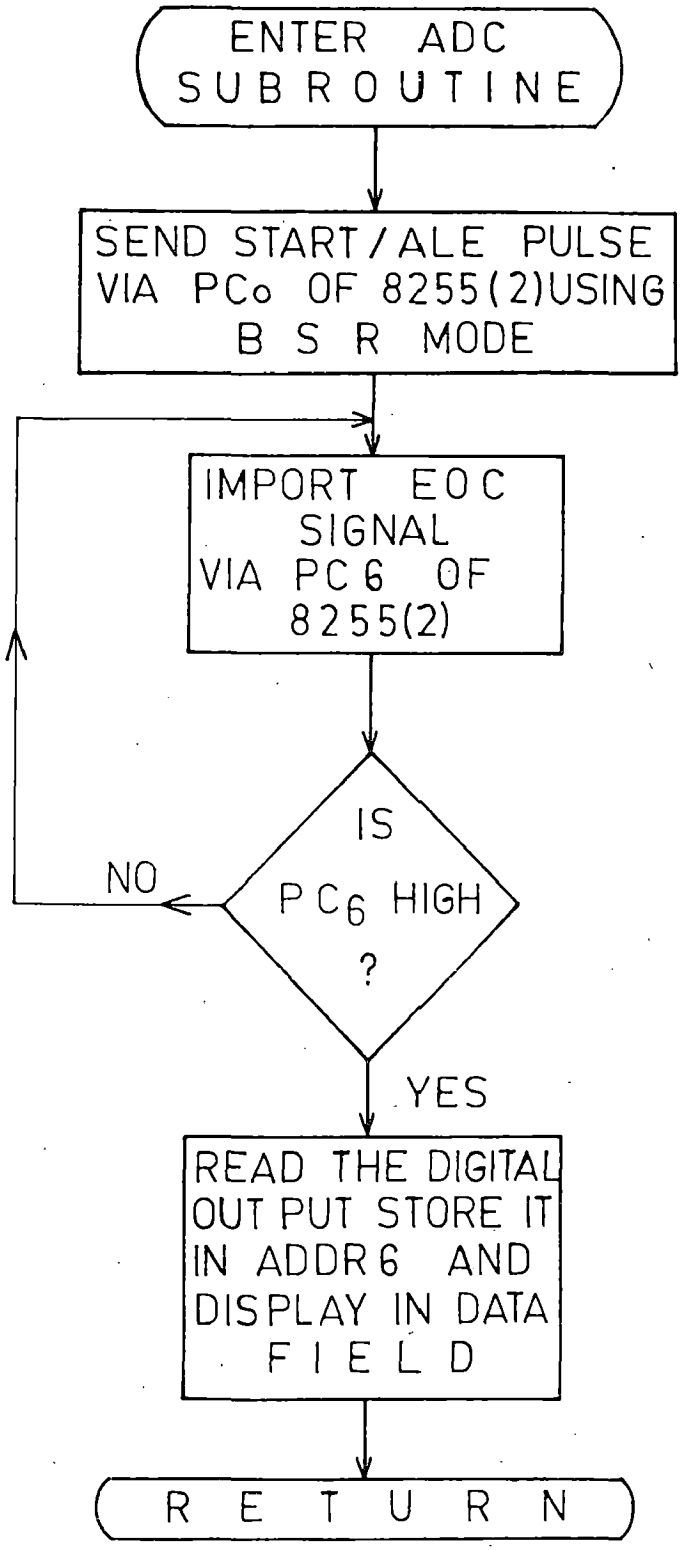


FIG. 3.2 FLOW CHART FOR ADC SUBROUTINE

The ADC clock-in is given from a 555 timer at 125 KH_Z. ADC issues an end of conversion signal indicating that the conversion process is over. Then the digital equivalent of the analog signal is inputed by the microprocessor through the 8 bits of port B of 8255A functioning as input port and this digital output is stored in the memory location ADDR6 and displayed in the data field of VMC-85 trainer kit. In this case, the digital output of ADC is varied from 00H to 5AH. If the ADC output becomes 00H, firing angle will be 90^o and 180^o when digital output is 5AH.

NAME OF THE SUBROUTINE	:	ADC
INPUT	:	Input to ADC through ADC pot via channel IN0 which is selected by hardware.
OUTPUT	:	Digital equivalent to the analog input in memory location ADDR6
CALLS	:	DELAY and MODDT
DESTROYS	:	PSW, B, D, E
DESCRIPTION	:	This subroutine provides the information about the firing angle for a particular setting of ADC pot. The digital output is stored in the memory location ADDR7 and displayed in the data field.

3.4 DIVISION SUBROUTINE

The flow chart for DIVISION subroutine is shown in Fig. 3.3. This subroutine is used to divide the 90^{o} count stored in the memory location ADDR2 by 5AH (90_{10}). Therefore, this routine calculate the count value corresponding to 1^{o}. A faster algorithm has been adopted for this division purpose which needs less execution time. The divident is 90^{o} count stored in memory location ADDR2 and divisor 5AH in register pair BC. In the present method of division, the divisor is substracted from the first bit of the divident. If a borrow occurs as a result of substraction, a '0' is entered in the quotient and the divisor is added to the result of the substraction so that the original value of the divident is restored. If no borrow occurs during the substraction operation, a '1' is entered into and the result of the substraction is used for the next substract and test process. 16 shifts and substractions are required to complete the division operation with the quotient in memory location ADDR4. The documentation of the subroutine is given below:

NAME OF THE SUBROUTINE : DIVISION

INPUT : Memorylocation ADDR2 contains the divident. BC register pair contains the divisor. Memory location ADDR5 is used as 16-bit counter.

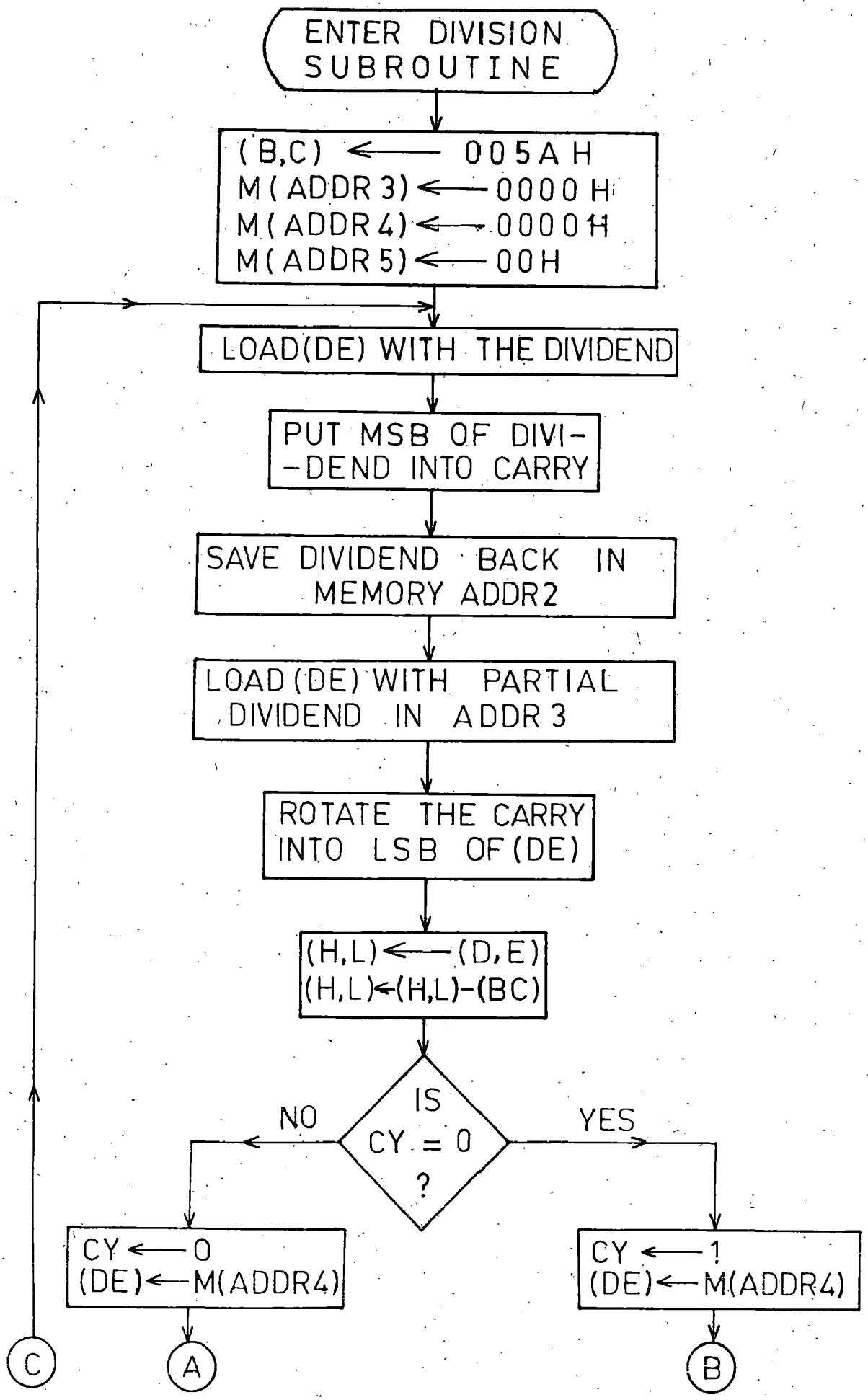
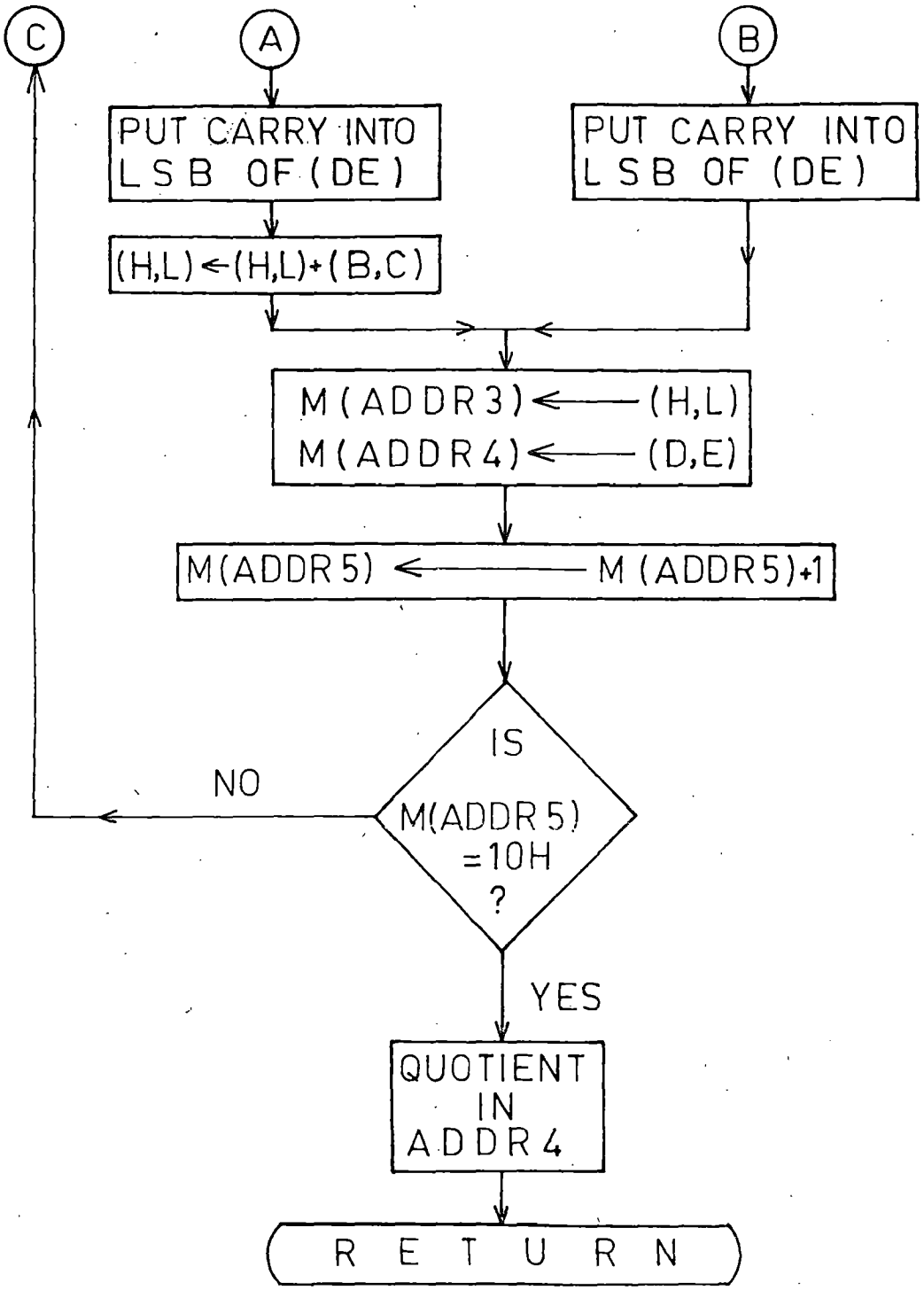


FIG. 3.3 FLOW CHART FOR DIVISION SUBROUTINE.


C
A
B
PUT CARRY INTO LSB OF (DE)
PUT CARRY INTO LSB OF (DE)
(H,L)←(H,L)+(B,C)
M(ADDR3)←(H,L)
M(ADDR4)←(D,E)
M(ADDR5)←M(ADDR5)+1
IS M(ADDR5) =10H ?
NO
YES
QUOTIENT IN ADDR4
RETURN

OUTPUT	:	The quotient is stored in the memory location ADDR4.
CALLS	:	NONE
DESTROYS	:	ALL
DESCRIPTION	:	This subroutine divides the 90^{o} count by 5AH to determine the count value corresponding to 1^{o}. After division is completed, the quotient is returned to the memory location ADDR4. This result is used in the MULT subroutine to calculate the count value above 90^{o} count for a particular firing angle.

3.5 MULT SUBROUTINE

In this subroutine, the count value corresponding to 1^{o} is multiplied by the digital output of the ADC. In ordinary multiplication process, two numbers can be multiplied by performing successive additions. If the number becomes large then this simple process is not used because of the long program execution time. Therefore, a more sophisticated multiplication subroutine is to be used. Here a faster algorithm for multiplication of two large numbers is implemented. The flow chart for MULT subroutine is shown in Fig. 3.4. Register pair DE contains the multiplicand which is 1^{o} count value corresponding to the clock 511.67 KH_{z}. Register B contains the multiplier and register C is used

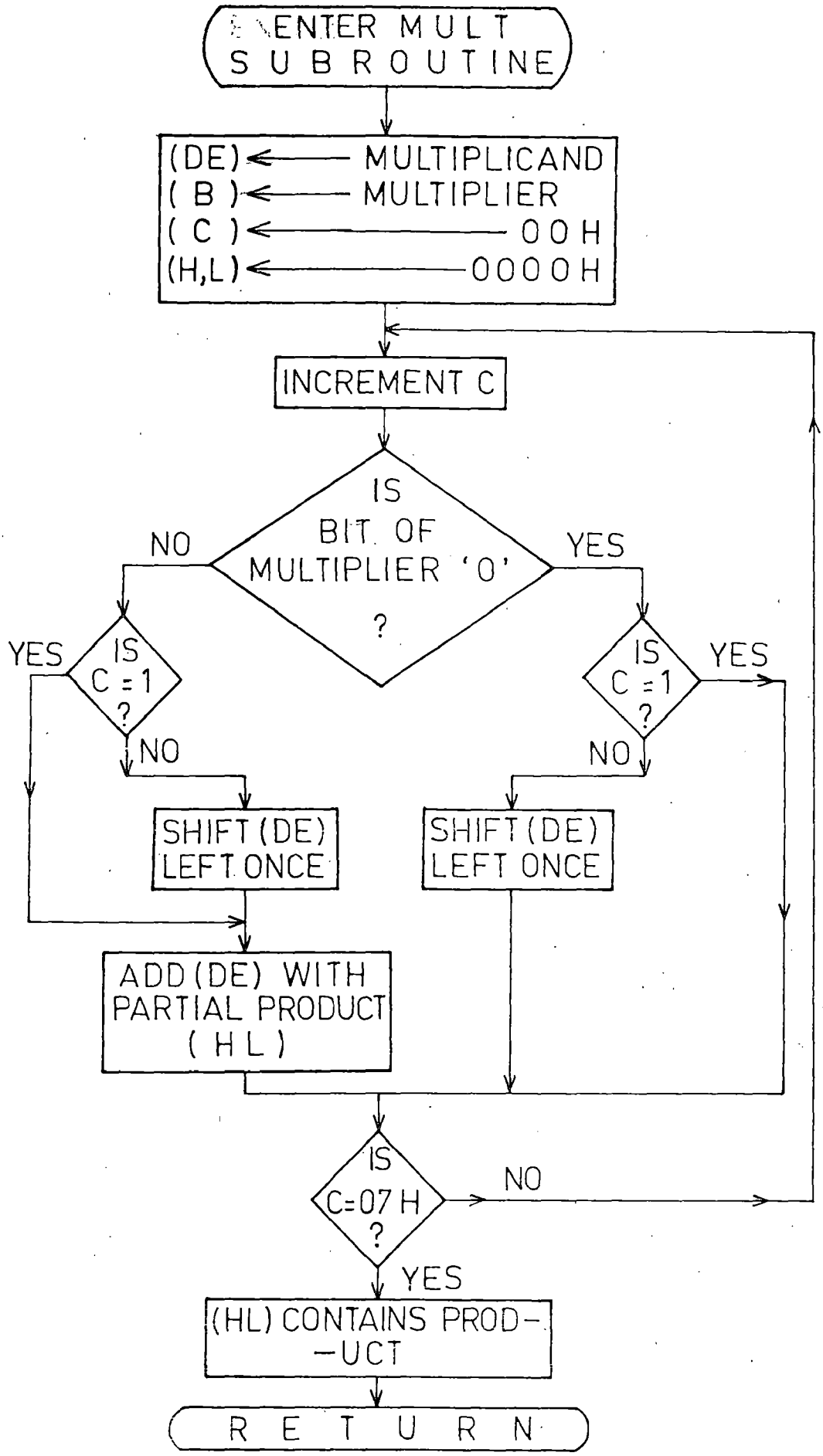


FIG. 3.4 FLOW CHART FOR MULT SUBROUTINE

to indicates the bit position of the multiplier. Register pair HL will contain the partial product or final product.

The clock 511.67 KH_z has been selected in such a way so that the 180^o count would not exceed FFFFH provided the machine speed is more than 120 rpm. If the machine speed is 120 rpm then 1^o count value can be calculated as follows:

$$T_{60} = \frac{T}{6} = \frac{120}{6\ PN} = \frac{120}{6 \times 4 \times 120} = 0.01416666 \text{ Sec.}$$

$$60^o \text{ count} = \frac{T_{60}}{1/511.67 \times 10^3} = \frac{0.01416666}{1/511.67 \times 10^3} = 21319_{10}$$

$$90^o \text{ count} = 60^o \text{ count} + \frac{60^o \text{ Count}}{2} = 31978_{10}$$

$$1^o \text{ count} = \frac{31978}{90} = 355_{10} = 163_{16}$$

$$= 0000000101100011_2$$

All the bits from A_9 to A_{15} of the 16 bit multiplicand are always '0'. Since the ADC output is allowed to vary from OOH to 5AH, B_7 bit of multiplier is always '0'. Since the binary digits may be either 1 or 0, the multiplier may be examined on a bit by bit basis for a '1' or a '0'. Starting from right to left, the multiplier is examined one bit at a time. If a '1' is found, the multiplicand is shifted in proper position and added to the accumulating result. If a '0' is found, nothing is added to the partial product. In the present case, 7 bits of the multiplier

are to be tested and the product is stored in HL register pair.

NAME OF THE SUBROUTINE	:	MULT
INPUT	:	Register pair DE contains 16-bit multiplicand. Register B contains multiplier.
OUTPUT	:	Register pair HL contains the the product.
CALLS	:	NONE
DESTROYS	:	ALL
DESCRIPTION	:	This subroutine is used to multiply 1^{o} count value as multiplicand with digital output of ADC. This multiplication is done once in every cycle of the machine frequency. This subroutine provides the count value above the 90^{o} count for a particular firing angle of the inverter.

3.6 IR_0 INTERRUPT SUBROUTINE

The flow chart of IR_0 interrupt service subroutine is shown in Fig. 3.5. At the beginning of the subroutine, the processor saves registers. In this service routine, the firing angle count is loaded into the counter $TM_1(2)$ from the memory location ADDR7. This firing angle count

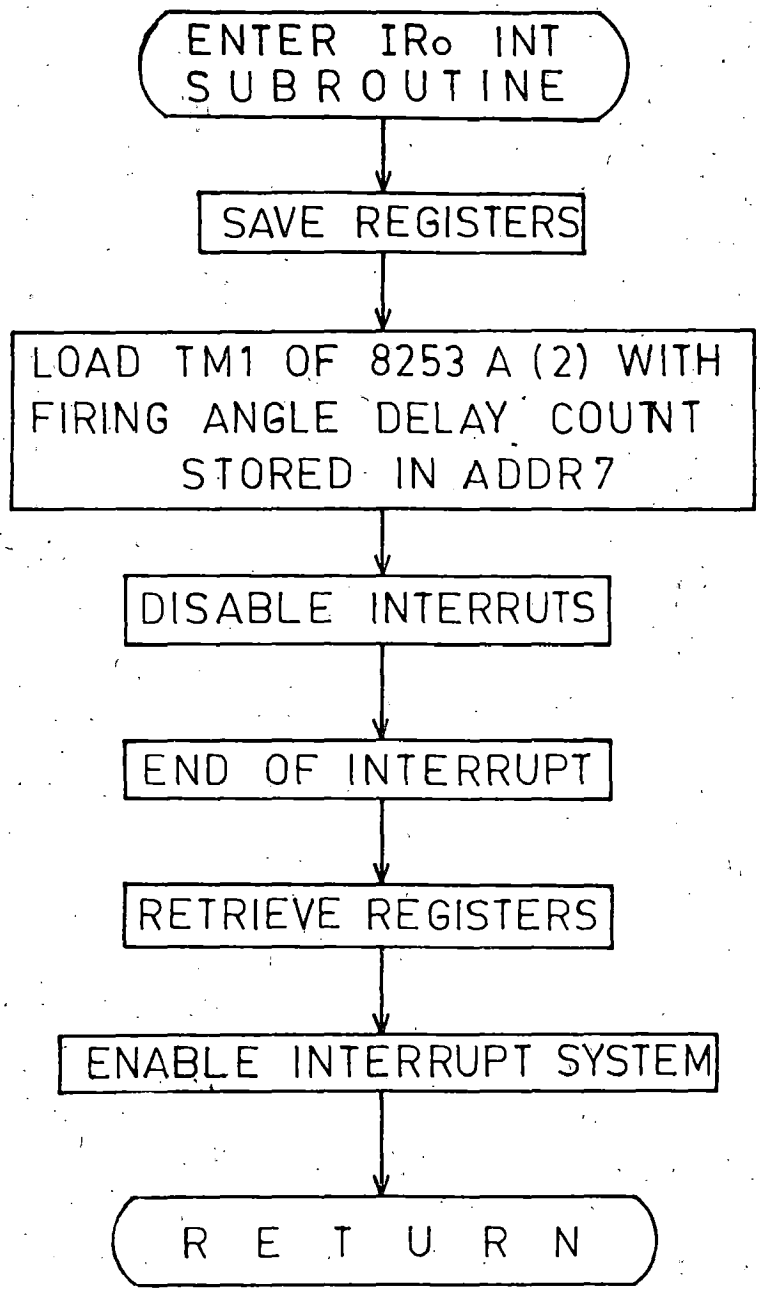


FIG. 3.5 FLOW CHART FOR IRo INTERRUPT SUBROUTINE.

is calculated just after triggering the thyristor pair (6, 1) by issuing proper firing pulses. Firing angle is computed at every cycle of the machine frequency. The counter TM1(2) is loaded with firing angle count once in every cycle. The microprocessor retrieves the registers and enables interrupt systems at the end of the subroutine before returning to the interrupted main program.

NAME OF THE SUBROUTINE	:	IR_0 INTERRUPT
INPUT	:	Firing angle count from the memory location ADDR7.
OUTPUT	:	The output of the counter TM1(2) on terminal count is used as IR_2 interrupt request input.
CALLS	:	NONE
DESTROYS	:	PSW
DESCRIPTION	:	This subroutine loads the counter TM1(2) with the firing angle count corresponding to the clock 511.67 KHz. Counter output goes to high on the terminal count. This output is used as the IR_2 interrupt request input.

3.7 IR_2 INTERRUPT SUBROUTINE

The flow chart for IR_2 service routine is shown in Fig. 3.6. Microprocessor starts executing of the subroutine with saving registers. (H, L) is incremented by one to

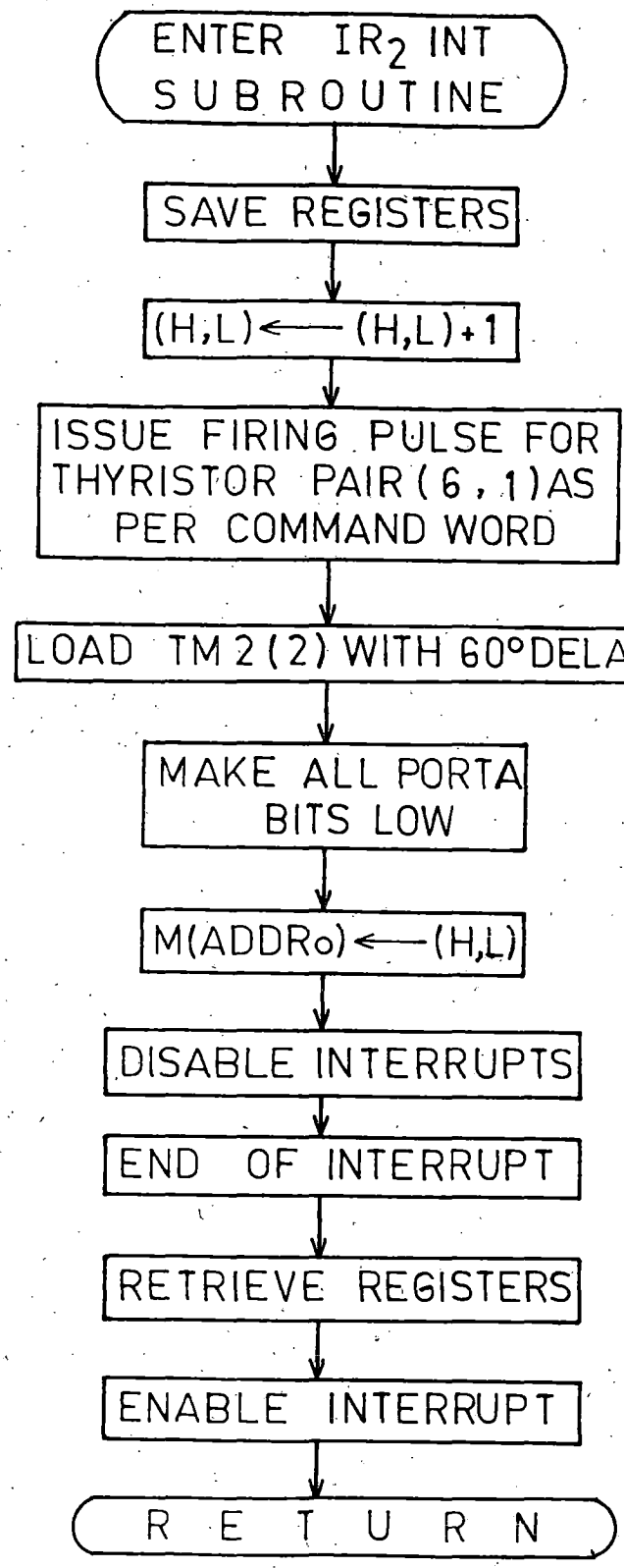


FIG. 3.6 FLOW CHART FOR IR_2 INTERRUPT SUBROUTINE.

points correctly the firing command word for the thyristor pair (6, 1). The microprocessor issues the firing pulses for the thyristor pair (6, 1) via port A of 8255A and 60° delay count is loaded into the counter TM2(2). The address of the command word is saved in the memory location ADDR0. The processor returns to the main program after retrieving registers and enabling interrupt systems.

NAME OF THE SUBROUTINE	:	IR_2 INTERRUPT
INPUT	:	Firing command word in memory location ADDR8.
OUTPUT	:	Outputs firing pulses for the thyristor pair (6, 1) via port A of 8255A as per firing command word in ADDR8.
CALLS	:	NONE
DESTROYS	:	PSW, H, L
DESCRIPTION	:	In this subroutine, the microprocessor issues firing pulses for the thyristor pair (6,1) through port A of 8255A with the firing command word in the memory location ADDR8. The 60° delay count is loaded into TM2(2). The output of TM2 on terminal count is used as IR_4 interrupt request.

3.8 IR_4 INTERRUPT SUBROUTINE

This subroutine is used to generate firing pulses for all thyristor pairs except the thyristor pair (6,1) . The flow chart for the IR_4 interrupt subroutine is given in Fig. 3.7. At the beginning of the subroutine, all the necessary registers are saved and register pair HL is incremented by one to points exactly the address of the firing command word for the required thyristor pair. The microprocessor outputs firing pulses according to command word for the required thyristor pair. If the firing sequence six is not over, 60^{o} delay count is reloaded into the counter TM2(2). The address of the firing command word is saved in the memory location ADDRO. The program is transferred to the interrupted routine after retrieving registers and enabling interrupt systems.

NAME OF THE SUBROUTINE	:	IR_4 INTERRUPT
INPUT	:	Firing pulse command in the command table whose starting address is ADDR8. 60^{o} delay count from memory location ADDR1 is loaded into TM2(2).
OUTPUT	;	Outputs firing pulses according to the command word from the table for the particular pair of thyristor.

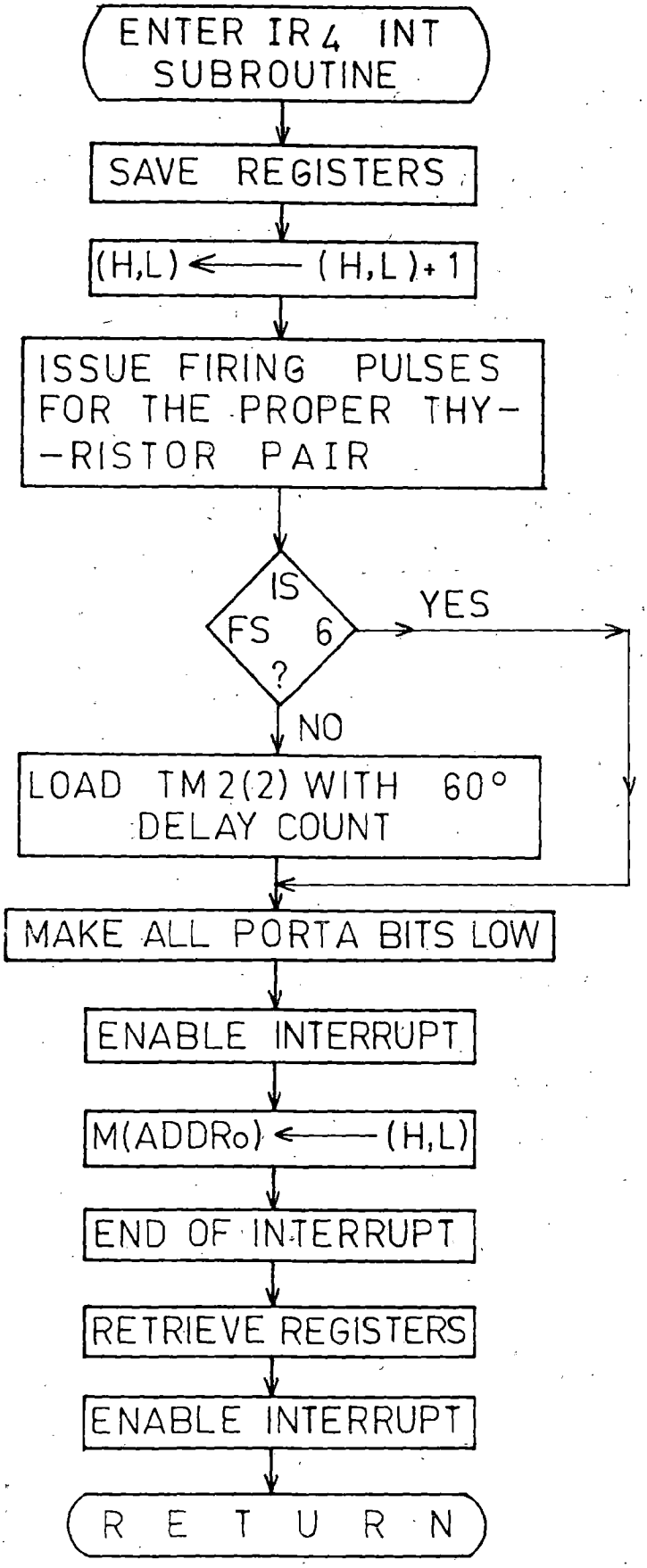


FIG. 3.7 FLOW CHART FOR IR4 INTERRUPT SUBROUTINE.

CALL	:	NONE
DESTROYS	:	PSW, H, L
DESCRIPTION	:	In this interrupt subroutine, the microprocessor issues firing pulses for all thyristor pairs except the pair (6,1). The 60^{o} delay count is reloaded into TM2(2) and the output of TM2(2) on the terminal count is used as IR_4 interrupt request.

3.9 SPEED SUBROUTINE

The flow chart for SPEED subroutine is given in Fig. 3.8. This subroutine is used to display the synchronous motor speed in the address field of vinytics VMC-85 uP trainer kit. The motor always runs at synchronous speed corresponding to the machine frequency. In every cycle, the 60^{o} count value is calculated and stored in the memory location ADDR1.

A look up table containing motor speed and corresponding 60^{o} count value has been prepared by using fortran program given in Appendix-V. Microprocessor follows a simple method to find out the machine speed from the look up table corresponding to the measured 60^{o} count stored in ADDR1. For example, if the 60^{o} count is 5347_{16} with the clock of 511.67 KH_z then the speed will be 120 rpm. In the Ist cycle, the measured 60^{o} count is compared with the

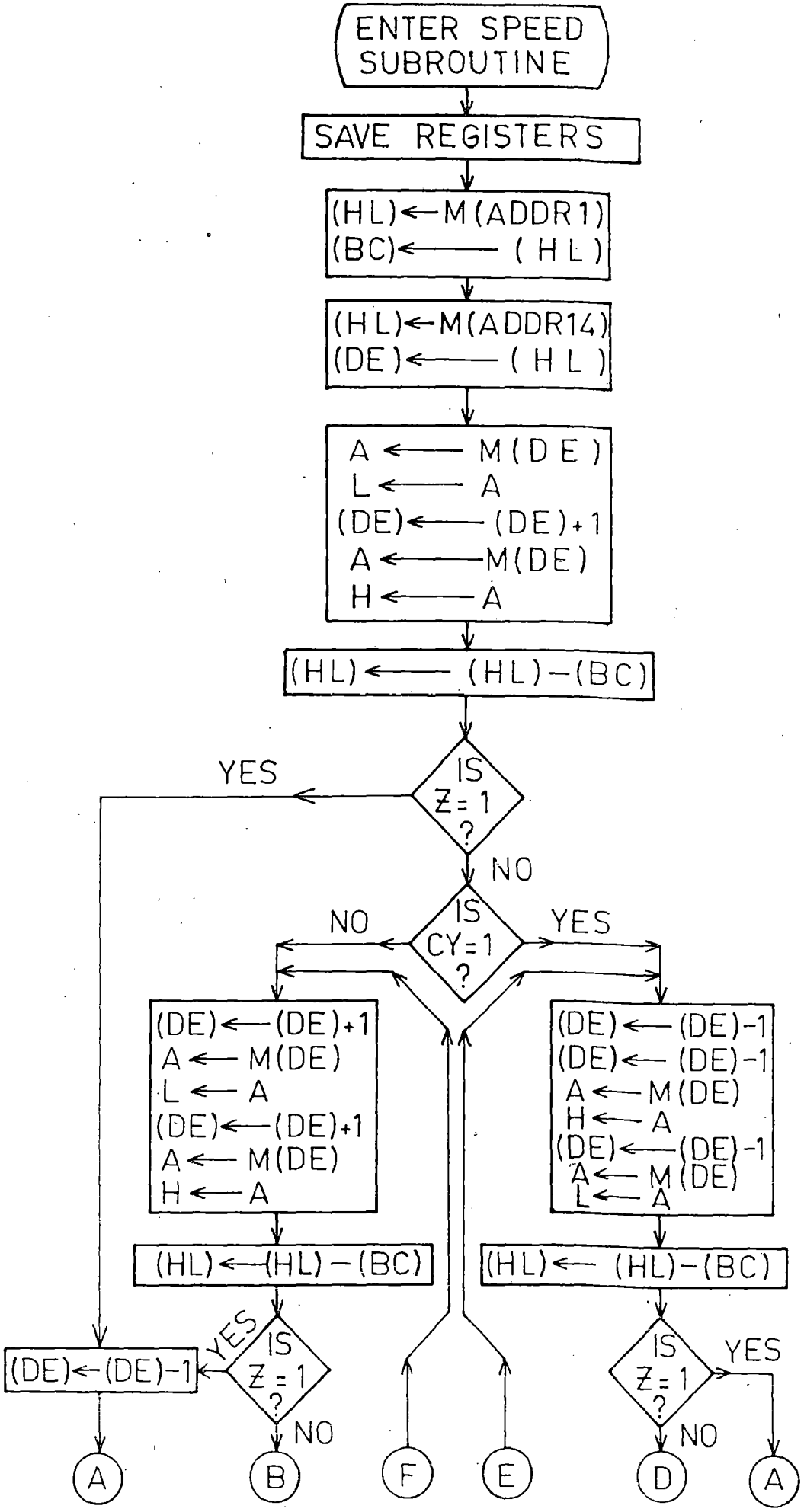
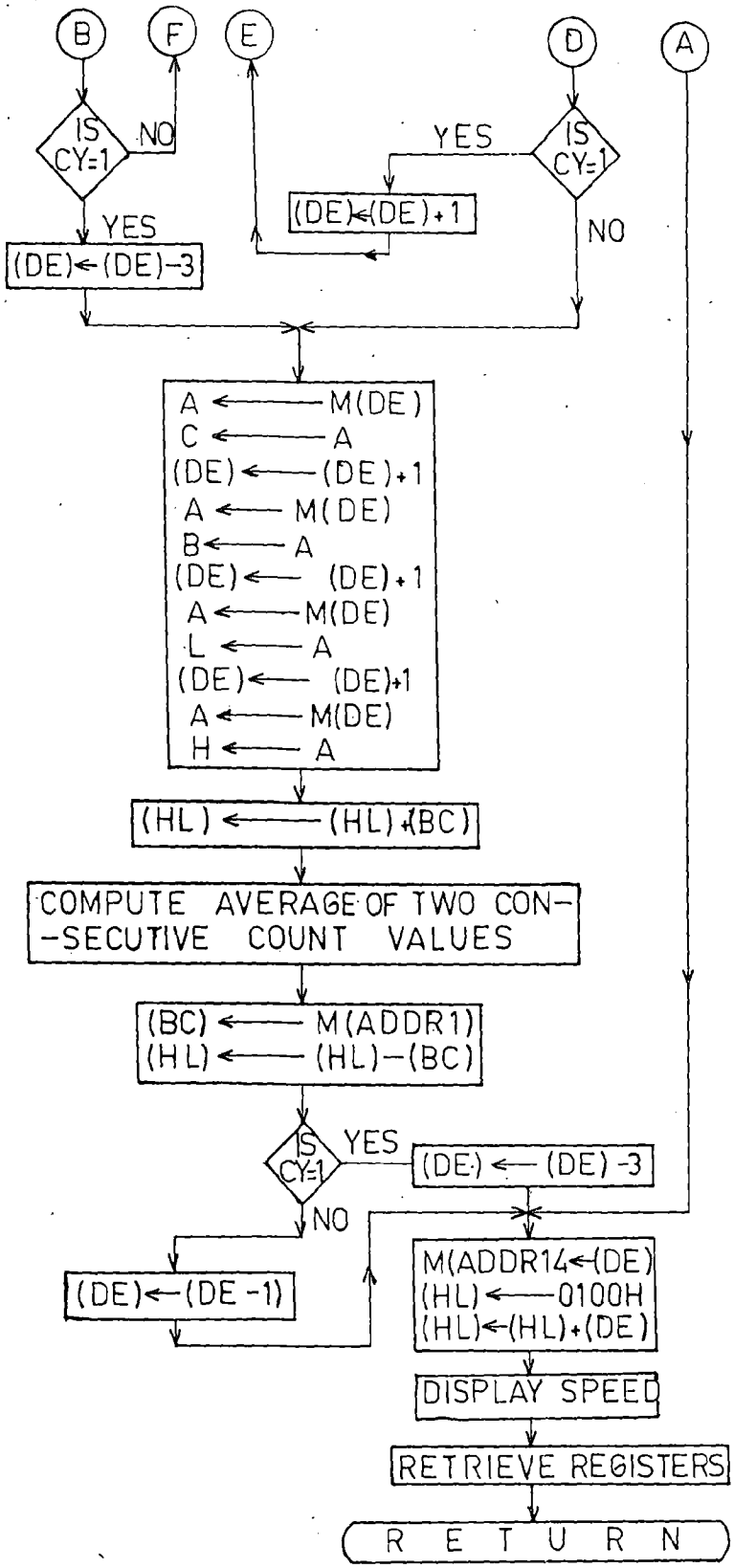


FIG. 3.8 FLOW CHART FOR SPEED SUBROUTINE


B
F
E
D
A
IS CY=1
NO
YES
(DE)←(DE)-3
(DE)←(DE)+1
IS CY=1
YES
NO
A ← M(DE)
C ← A
(DE) ← (DE)+1
A ← M(DE)
B ← A
(DE) ← (DE)+1
A ← M(DE)
L ← A
(DE) ← (DE)+1
A ← M(DE)
H ← A
(HL) ← (HL)+(BC)
COMPUTE AVERAGE OF TWO CON-SECUTIVE COUNT VALUES
(BC) ← M(ADDR1)
(HL) ← (HL)-(BC)
IS CY=1
YES
(DE) ← (DE)-3
NO
(DE)←(DE-1)
M(ADDR14←(DE)
(HL) ← 0100H
(HL)←(HL)+(DE)
DISPLAY SPEED
RETRIEVE REGISTERS
R E T U R N

middle value of the look up table to decide which half of the table contains this value. If the 60^{o} count is in the Ist half then comparison is carried out in upward direction from the bottom data in the Ist half of the look up table. On the other hand, if the measured 60^{o} count value becomes less than the middle value of the look up table, the motor speed is found out by comparing the measured value with the calculated values starting from the top data in the 2nd half of the look up table. The address of the 60^{o} count which is found to very close to the measured 60^{o} value is stored in the memory location ADDR14. In the next cycle, microprocessor searches out the value from the look up table which is very close to measured 60^{o} count with respect to the value whose address is available in memory location ADDR14 and the corresponding speed is displayed in the address field. The address of the present count is again stored in ADDR14 for using in the next time. The speed is displayed at every cycle of the inverter operation. The major advantage of this method is that it does not require any extra hardware components.

NAME OF THE SUBROUTINE : SPEED

INPUT : 60^{o} count corresponding to the clock 511.67 KH_{Z} in the memory location ADDR1.

OUTPUT	:	Display synchronous motor speed in the address field.
CALLS	:	NONE
DESTROYS	:	ALL
DESCRIPTION	:	This subroutine measures the machine speed and displays speed directly in decimal form in the address field. This subroutine mak s use of look up table prepared analytically to search out the motor speed directly corresponding to measured 60° count value stored in memory location ADDR1.

3.10 CONCLUSIONS

In this chapter, the main program and the various subroutine used in the main routine implementation have been described in detail. The various subroutine discussed are ADC subroutine, DIVISION subroutine, MULT subroutine, IR_0 interrupt subroutine, IR_2 interrupt subroutine, IR_4 interrupt subroutine and SPEED subroutine.

ADC subroutine provides on line firing angle information for the line commutated inverter. DIVISION subroutine is used to calculate 1° count and MULT subroutine performs the multiplication of 1° count and ADC output.

In the present scheme, three interrupt requests handled by 8259A are used. They are IR_0, IR_2 and IR_4

interrupt requests. IR_0 interrupt request is used to load the firing angle delay count into TM1(2) and IR_2 and IR_4 interrupt request have been used for generating firing pulses for the thyristors of the inverter in proper sequence.

The main routine and various subroutines software programmes have been tested individually on a VMC-85 uP trainer for implementing in the present scheme.

CHAPTER - IV

STEADY STATE ANALYSIS OF THE DRIVE

4.1 GENERAL

The steady state performance equations of a commutatorless d.c. series motor (SCLM) drive are developed systemtically in this chapter. Simple effective equivalent circuits are presented for the SCLM system during conduction and commutation interval. With the help of equivalent circuit and vector diagram, the performance equations of the commutatorless d.c. series motor are derived. A computer algorithm is developed for steady state analysis of the drive.

4.2 ANALYSIS

4.2.1 System Considered:

The schematic diagram of the system considered for steady state analysis is shown in Fig. 2.1. The system comprises of an auto-transformer, an uncontrolled bridge rectifier, a d.c. link inductor, a machine voltage commutated inverter and a conventional synchronous machine. The average d.c. output voltage of the rectifier is controlled by changing the a.c. voltage input to the diode bridge rectifier. This three phase uncontrolled bridge rectifier and d.c. link inductor combine to form a d.c.

current source for the line commutated inverter. The synchronizing signal is obtained by sensing two line to line voltages; V_{AC} and V_{CB} from the synchronous motor terminals. This synchronizing signal is inputed to the microcomputer for generating firing pulses for the thyristors of the bridge inverter in proper sequence. The loading arrangement of the commutatorless d.c. motor is performed by a separately excited d.c. generator coupled to synchronous motor.

4.2.2 Analytical Model:

The steady state analysis of commulatorless d.c. series motor is based on several assumptions to simplify the derivations. These assumptions are as follows:

i) The d.c. link current I_{dc} is assumed to be ripple free.

ii) The stator winding resistance drop I_{sy} R_{sy} of synchronous machine is neglected.

iii) The effect of magnetic saturation on the performance of synchronous motor is neglected.

iv) The voltage commutated inverter operation is assumed to be lossless and free from harmonics.

v) A gating signal for the SCR is available at the inverter lead angle .

vi) Damper windings of the synchronous machine are neglected.

vii) Flux linkage is assumed to be constant during commutation period of thyristors.

viii) Mechanical moment of inertia of the motor is assumed to be so large that the motor speed remains constant during commutation period.

ix) Terminal voltages of synchronous machine are assumed to be balanced and sinusoidal.

There are two modes of operation of the inverter in commutatorless d.c. series motor system. These are conduction and commutation modes. The equivalent circuit [19] of the synchronous machine during the commutation is shown in Fig. 4.1. In this circuit, each phase of the machine is represented by a voltage source (line to neutral terminal voltage) in series with a commutating reactance X_c. The negative sequence reactance due to line-to-line short circuit between any two terminals of the synchronous machine is considered as commutating reactance which is seen by the current during the commutation period.

Line commutation of the thyristors of inverter is made possible by the fact that its a.c. terminals are connected to the synchronous machine which is seen by the inverter as a three-phase a.c. source of terminal voltage V_{sy} (line-to-neutral) and commutating reactance X_c (source reactance).

Three-phase bridge rectifier with auto-transformer and d.c. link inductor acts together as a variable d.c.

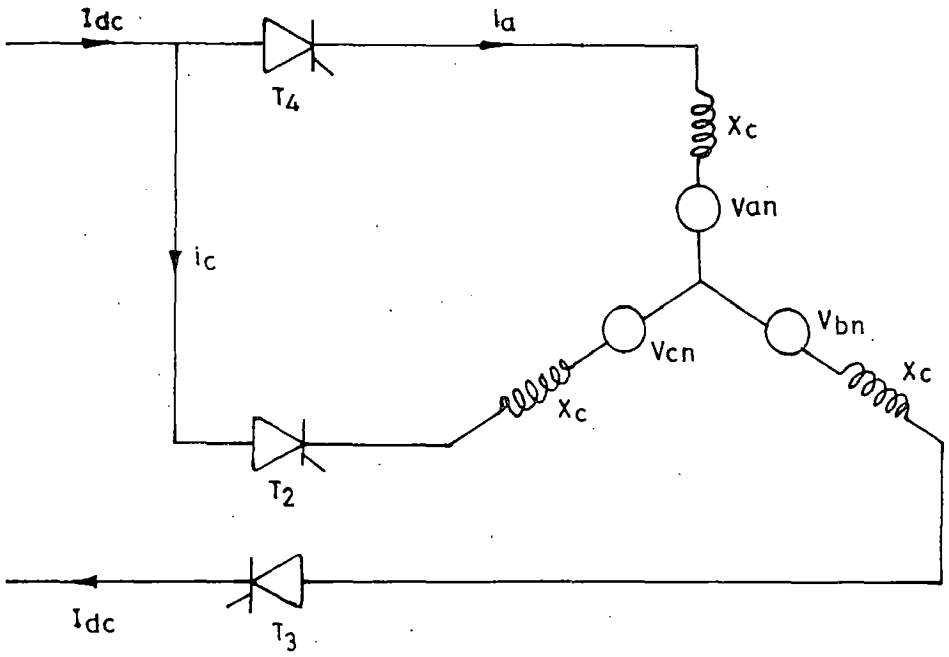


FIG. 4·1 – EQUIVALENT CIRCUIT DIAGRAM DURING COMMUTATION FROM THYRISTOR T_2 TO THYRISTOR T_4

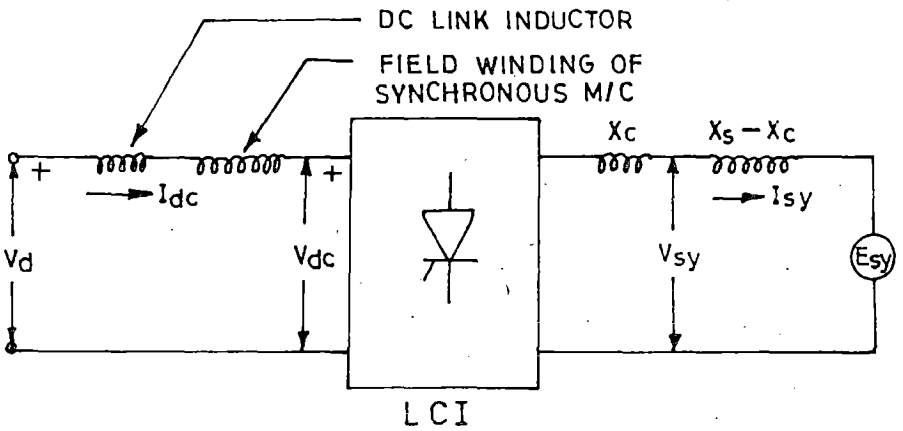


FIG. 4·2 – EQUIVALENT CIRCUIT DIAGRAM OF COMMUTATORLESS DC SERIES MOTOR

current source for the line commutated inverter. The d.c. link current is cyclically distributed into the three a.c. lines in the form of rectangular a.c. currents of I_{dc} amplitude. The fundamental components I_{sy} of these three a.c. line current are 120^{o} displaced. They lead their respective line-to-neutral motor terminal voltage by displacement angle $\beta' + 180^{o}$, where β' is the supplementary angle between V_{sy} and I_{sy}.

If the reactance X_c is connected in series with the line to act like a source reactance of the three-phase a.c. voltage source of rms value V_{sy} (line-to-neutral voltage), the fundamental component of the machine current also flows through X_c. Therefore , the synchronous reactance must be reduced to $X_s - X_c$ so that total effect of I_{sy} is unchanged. The effective equivalent circuit for commutatorless d.c. series motor is shown in Fig. 4.2 which is derived with the help of equivalent circuits given by Hoanglethy [19], John Rosa [23] and Ajay Kumar [7] with some modifications, which take care of the fact that excitation winding now appears series connected with the d.c. link.

The fundamental current I_{sy} results in a sinusoidal voltage drop $I_{sy}(X_s - X_c)$ across the adjusted synchronous reactance $(X_s - X_c)$ resulting in sinusoidal voltage V_{sy} behind the reactance X_c, where the interface between machine and line commutated inverter is assumed to lie.

The phasor diagram of the commutatorless d.c. series motor is shown in Fig. 4.3 which is same as the phasor diagram derived by John Rosa [23] for machine commutated inverter fed synchronous machine. The machine current I_{sy} leads the loaded terminal voltage V_{sy} at an supplementary angle β' . Terminal voltage V_{sy} leads the no load voltage E_{sy}, which in turn is induced by pole flux ϕ by an angle $r - \beta'$ where r is the supplementary displacement angle of I_{sy} with respect to E_{sy}.

The no load terminal voltage (excitation voltage) of the synchronous machine is given by

$$E_{sy} = 4.44\ K_w\ \phi f\ T_{ph} \qquad \ldots\ldots(4.1)$$

where K_w = distribution factor

T_{ph} = Turn per phase

ϕ = flux per pole

The relationship between flux per pole and excitation current is described by

$$\phi = K_f\ I_f \qquad \ldots\ldots(4.2)$$

Thus with the use of (4.1) and (4.2), we get

$$E_{sy} = 4.44\ K_w\ K_f\ I_f\ f\ T_{ph}$$

$$\text{or} \quad E_{sy} = (4.44\ K_w\ K_f\ T_{ph})\ I_f\ f$$

$$\text{or} \quad E_{sy} = K_e\ I_f . f \qquad \ldots\ldots(4.3)$$

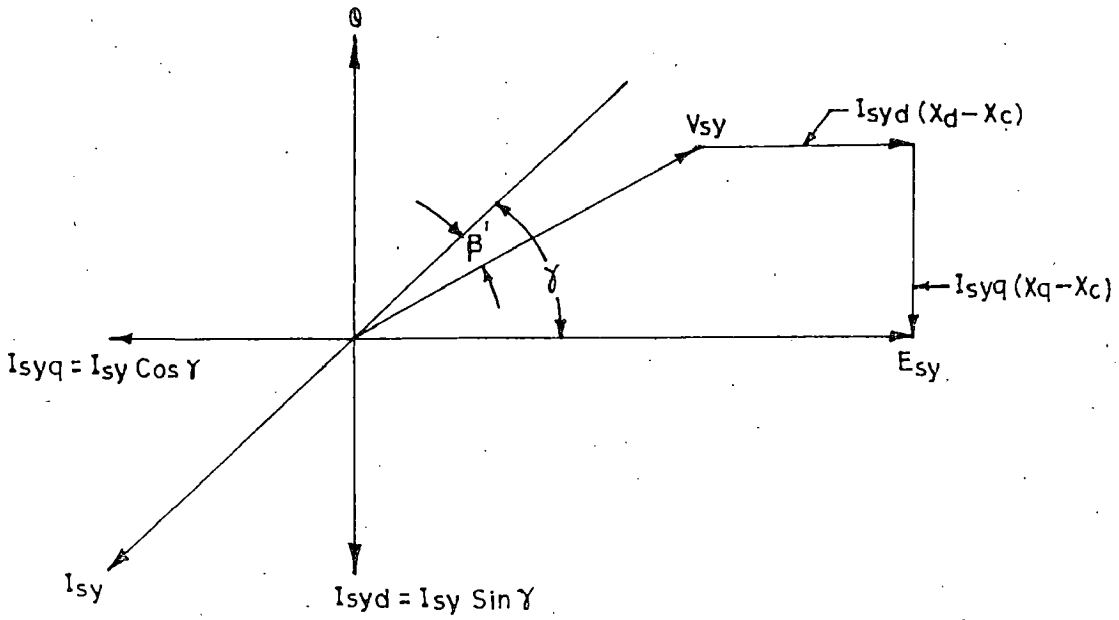


FIG. 4·3-PHASOR DIAGRAM OF COMMUTATORLESS DC SERIES MOTOR

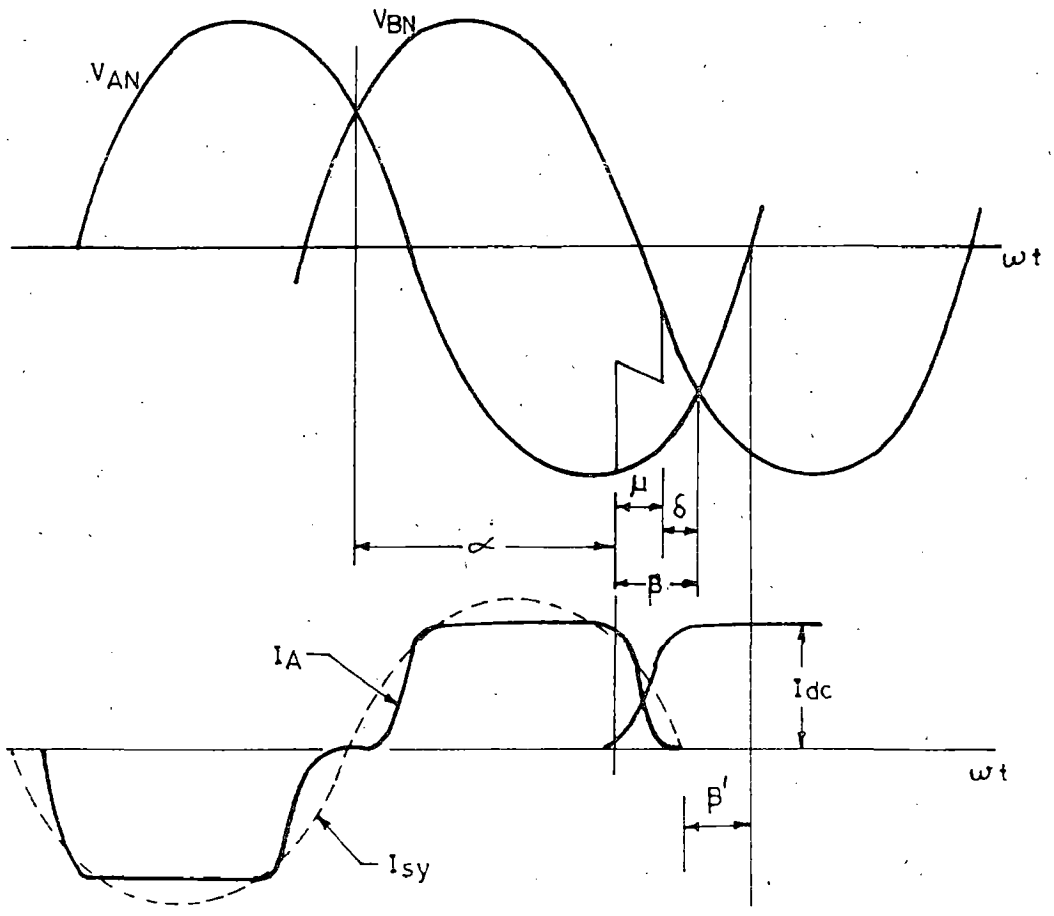


FIG. 4·4—COMMUTATION EVENT FROM THYRISTOR T_1 TO THYRISTOR T_3

where $K_e = 4.44\ K_w\ K_f\ T_{ph}$

For commutatorless d.c. series motor, the excitation current is given by

$$I_f = K\ I_{dc} \qquad \ldots.(4.4)$$

where $K = \frac{R_h}{R_f + R_h}$ and its value becomes 1.0 if no field divertor is connected across the field winding of synchronous machine.

where R_f = Resistance of excitation winding of synchronous machine.

R_h = Resistance of field diverter, substituting (4.4) for I_f into (4.3), we get

$$E_{sy} = K\ K_e\ I_{dc} f \qquad \ldots.(4.5)$$

The fundamental component I_{sy} (rms value) of the rectangular wave a.c. line current of amplitude I_{dc} is found in [23].

$$I_{sy} = \frac{\sqrt{6}}{\pi}\ I_{dc} \qquad \ldots.(4.6)$$

with the use of equation (4.5) and (4.6),

$$E_{sy} = K_1\ I_{sy}\ f \qquad \ldots.(4.7)$$

where $K_1 = K\ K_e \frac{\pi}{\sqrt{6}}$

or $E_{sy} = K_2\ I_{dc}\ N \qquad \ldots.(4.8)$

where $K_2 = \frac{K K_e P}{120}$

The loaded terminal voltage V_{sy} is obtained from the phasor diagram as the vector difference between E_{sy} and reactive voltage drop $I_{syd}(X_d - X_c)$ and $I_{syq}(X_q - X_c)$, each leading the respective current component I_{syd} and I_{syq} by 90^o. Where I_{syd} and I_{syq} are the direct and quadrature axis components of I_{sy} with respect to ϕ (direct axis).

With the help of vector diagram, the relationship between V_{sy}, E_{sy}, I_{syd}, I_{syq}, X_d and X_q is described by

$$V_{sy}^2 = [E_{sy} - I_{syd}(X_d - X_c)]^2 + [I_{syq}(X_q - X_c)]^2 \quad ....(4.9)$$

Let us assume $X_d - X_c = X$

$$X_q - X_c = qX \quad ....(4.10)$$

The direct and quadrature axis components of I_{sy} are

$$I_{syd} = I_{sy} \text{ Sin}r$$

$$I_{syq} = I_{sy} \text{ Cos}r \quad ....(4.11)$$

Now substituting equations (4.10) & (4.11) into (4.9), we get

$$V_{sy}^2 = [E_{sy} - I_{sy} \text{ Sin}r \, X]^2 + [I_{sy} \text{ Cos}r \, qX]^2$$

$$= E_{sy}^2 - 2E_{sy}I_{sy} \text{ Sin}r \, X + I_{sy}^2 \text{ Sin}r \, X^2 + I_{sy}^2 \text{Cos}^2 r \, q^2 X^2$$

$$= E_{sy}^2 \left[1-2\frac{I_{sy}X}{E_{sy}}\text{Sinr} + \left(\frac{I_{sy}X}{E_{sy}}\right)^2 (\text{Sin}^2 r+q^2\text{Cos}^2 r)\right] \quad ..(4.12)$$

$$\text{or } V_{sy} = E_{sy}\left[1-2\frac{I_{sy}X}{E_{sy}}\text{Sinr} + \left(\frac{I_{sy}X}{E_{sy}}\right)^2 (\text{Sin}^2 r+q^2\text{Cos}^2 r)\right]^{\frac{1}{2}} \quad ..(4.13)$$

Substituting equation (4.7) for E_{sy} into (4.13), we have

$$V_{sy} = K_1 I_{sy} f \left[1-2\frac{I_{sy}X}{K_1 I_{sy} f}\text{Sinr} + \left(\frac{I_{sy}X}{E_{sy}}\right)^2 (\text{Sin}^2 r+q^2\text{Cos}^2 r)\right]^{\frac{1}{2}}$$

$$= K_1 I_{sy} f \left[1-2\frac{2\pi(L_d-L_c)}{K_1}\text{Sinr} + \frac{4\pi^2(L_d-L_c)^2}{K_1^2}\right.$$

$$\left.(\text{Sin}^2 r + q^2\text{Sin}^2 r)\right]^{\frac{1}{2}}$$

$$\text{or } V_{sy} = K_1 I_{sy} f \left[1-2K_d\,\text{Sinr} + K_d^2(\text{Sin}^2 r + q^2\text{Cos}^2 r)\right]^{\frac{1}{2}} \quad ..(4.14)$$

$$\text{where } K_d = \frac{2\pi(L_d - L_c)}{K_1}$$

The supplementary displacement angle r between I_{sy} and E_{sy} depends on machine parameters and firing angle of the line commutated inverter. Therefore if the firing angle is maintained constant then the expression within the bracket in the right hand side of (4.14) also remains constant. So under this condition, equation (4.14) is reduced to

$$V_{sy} = K_m I_{sy} f \quad ..(4.15)$$

$$\text{where } K_m = K_1\left[1-2K_d\,\text{Sinr} + K_d^2(\text{Sin}^2 r+q^2\text{Cos}^2 r)\right]^{\frac{1}{2}}$$

$$\text{or} \quad V_{sy} = K_m\left(\frac{\sqrt{6}}{\pi} I_{dc}\right) f$$

$$= K_m \frac{\sqrt{6}}{\pi} I_{dc} f$$

$$V_{sy} = K_p I_{dc} f \quad \text{where } K_p = K_m \frac{\sqrt{6}}{\pi} \qquad \ldots.(4.16)$$

The commutation phenomena from thyristor T_1 to T_3 in conjunction with firing angle, commutation angle, lead angle, margin angle and power factor angle are shown in Fig. 4.4.

From the vector diagram, we get the following relations :

$$\text{Cos}(r - \beta') = \frac{E_{sy} - I_{sy} X \text{ Sin}r}{V_{sy}} \qquad \ldots.(4.17)$$

$$\text{Sin}(r - \beta') = \frac{q\, I_{sy} X \text{ Cos}r}{V_{sy}} \qquad \ldots.(4.18)$$

Equations (4.17) and (4.18) can be rewritten as

$$\text{Cos}r.\text{Cos}\beta' + \text{Sin}r.\text{Sin}\beta' = \frac{E_{sy} - I_{sy} X \text{ Sin}r}{V_{sy}} \qquad \ldots.(4.19)$$

$$\text{Sin}r.\text{Cos}\,\beta' - \text{Cos}r.\text{Sin}\,\beta' = \frac{q\, I_{sy} X \text{ Cos}r}{V_{sy}} \qquad \ldots.(4.20)$$

Solving equation (4.19) and (4.20), expression for power factor of the machine is obtained as

$$\text{Cos}\ \beta' = \text{PF} = \frac{E_{sy}}{V_{sy}} \left[1 - \frac{I_{sy} X \text{ Sin}r}{E_{sy}} + \frac{q I_{sy} X \text{ Sin}r}{E_{sy}}\right] \text{Cos}r$$

$$\text{or } \cos\beta' = \frac{E_{sy}}{V_{sy}}\left[1 - \frac{I_{sy}\,X}{E_{sy}}(1-q)\sin r\right]\cos r \qquad \ldots.(4.21)$$

With the use of equation (4.7), (4.15), (4.10) and (4.21), we get PF as follows:

$$\cos\beta' = \frac{K_1\,I_{syf}}{K_m\,I_{syf}}\left[1 - \frac{I_{sy}\,X}{K_1\,I_{syf}}(1-q)\sin r\right]\cos r$$

$$\cos\beta' = K_c\left[1 - K_d(1-q)\sin r\right]\cos r \qquad \ldots.(4.22)$$

where $K_c = \dfrac{K_1}{K_m}$

$$K_d = \frac{2\pi\,(L_d - L_c)}{K_1}$$

This relationship indicates that power factor of the synchronous machine is independent of load and speed.

The well known relationship between quantities V_{sy}, V_{dc}, I_{dc}, X_c and angles β, μ, δ are found in [11].

$$V_{dc} = \frac{3}{\pi}\left(\sqrt{6}\,V_{sy}\cos\beta + I_{dc}\,X_c\right) \qquad \ldots.(4.25)$$

$$\cos(\beta-\mu) = \cos\delta = \cos\beta + \sqrt{\frac{2}{3}}\cdot\frac{I_{dc}\,X_c}{V_{sy}} \qquad \ldots.(4.26)$$

D.C. power input to the inverter must equal to the real a.c. power fed to the synchronous motor, neglecting the losses in the inverter system.

$$P_{dc} = P_{ac}$$

$$V_{dc}\,I_{dc} = 3\,V_{sy}\,I_{sy}\cos\beta' \qquad \ldots.(4.27)$$

Where V_{dc} = DC voltage appearing at the input of the inverter

I_{dc} = DC link current

β' = Phase shift between I_{sy} and V_{sy}

Substituting equation (4.21) and (4.25) into (4.27), we get

$$\frac{3}{\pi}(\sqrt{6}\ V_{sy}\ \text{Cos}\beta + I_{dc}X_c)I_{dc} = 3\ E_{sy}\left[1 - \frac{I_{sy}X}{E_{sy}}(1-q)\ \text{Sin}r\right] \text{Cos}r\ I_{sy} \qquad \ldots.(4.28)$$

With the help of equation (4.6), this equation becomes

$$3V_{sy}I_{sy}\ \text{Cos}\beta + \frac{\pi}{2}\ I_{sy}^2X_c = 3E_{sy}I_{sy}\left[1 - \frac{I_{sy}X}{E_{sy}}(1-q)\text{Sin}r\right]\text{Cos}r$$

$$\text{or Cos}\beta = \frac{\left[1 - \frac{I_{sy}X}{E_{sy}}(1-q)\text{Sin}r\right]\text{Cos}r - \frac{\pi}{6}\cdot\frac{I_{sy}X_c}{E_{sy}}}{V_{sy}/E_{sy}} \qquad \ldots.(4.29)$$

Substituting (4.7), (4.10) and (4.15) into (4.29), we have the following expression of Cos β.

$$\text{Cos}\beta = \frac{\left[1 - 2\pi(L_d-L_c)/L_c(1-q)\text{Sin}r\right]\text{Cos}r - \frac{\pi}{6}\cdot\frac{2\pi L_c}{K_1}}{K_m/K_1}$$

$$\text{Cos}\ \beta = \frac{\left[1 - K_d(1-q)\text{Sin}r\right]\text{Cos}r - K_aL_c}{1/K_c} \qquad \ldots.(4.30)$$

where $K_d = \dfrac{2\pi(L_d-L_c)}{K_1}$

The details of computing r for a lead angle β is given in Appendix-IV.

$$K_c = K_1/K_m$$

$$K_a = \frac{\pi 2}{3K_1}$$

Equation (4.30) states the relationship between inverter lead angle β and the phase displacement angle r.

Now substituting (4.29) for $\cos\beta$ into (4.26), the relationship between r and turn off angle δ is also obtained.

$$\cos\delta = \frac{[1 - I_{sy} X/E_{sy}(1-q)\sin r]\ \cos r - \frac{\pi}{6} \cdot \frac{I_{sy}X_c}{E_{sy}}}{V_{sy}/E_{sy}}$$

$$+ \sqrt{\frac{2}{3}} \cdot \frac{\pi \cdot I_{sy}X_c}{\sqrt{6} \cdot V_{sy}} \qquad \ldots.(4.31)$$

$$= \frac{[1 - I_{sy}X/E_{sy}(1-q)\sin r]\cos r}{V_{sy}/E_{sy}} + \frac{\pi}{6} \frac{I_{sy} X_c}{V_{sy}}$$

$$\text{or } \cos\delta = \frac{[1 - I_{sy}X/E_{sy}(1-q)\sin r]\cos r + \frac{\pi}{6} \cdot \frac{I_{sy}X_c}{E_{sy}}}{V_{sy}/E_{sy}} \ldots.(4.32)$$

Thus with the use of equation (4.7), (4.10) and (4.15), equation (4.32) is simplified into

$$\cos\delta = \frac{[1 - K_d(1-q)\sin r]\cos r + K_a L_c}{1/K_c} \qquad \ldots.(4.33)$$

D.C. power input to the inverter is given by

$$P_{dc} = V_{dc}\, I_{dc} \qquad \ldots.(4.34)$$

Substituting (4.25) for V_{dc} into (4.34), we get

$$P_{dc} = \frac{3\sqrt{6}}{\pi} V_{sy} \cos\beta\ I_{dc} + \frac{3}{\pi} I_{dc}^2 X_c \qquad \ldots.(4.35)$$

Equation (4.16) is substituted into (4.35) to yield

$$P_{dc} = \frac{3\sqrt{6}}{\pi} (K_p I_{dc} f)\ I_{dc} \cos\beta + \frac{3}{\pi} I_{dc}^2 X_c \qquad \ldots.(4.36)$$

After doing some algebraic operations, the desired relationship is obtained

$$P_{dc} = K_{dc} I_{dc}^2 N \qquad \ldots.(4.37)$$

where $K_{dc} = \frac{\sqrt{6}}{40\pi} PK_p \cos\beta + \frac{P}{20} L_c$

P = No of pole of the synchronous machine

N = Speed of the synchronous motor in RPM

The electromagnetic torque developed by the synchronous motor is given by

$$T = \frac{3\ V_{sy}\ I_{sy} \cos\beta'}{w} \qquad \ldots.(4.38)$$

where $w = 2\pi N_s = 2\pi \frac{2f}{P} = \frac{4\pi}{P} f$

N_s = Machine speed in r.p.s.

Substituting equation (4.15) into (4.38), we get the following expression for the torque

$$T = \frac{3.K_m.\frac{\sqrt{6}}{\pi} I_{dc}.f \cdot \frac{\sqrt{6}}{\pi} \cdot I_{dc}.\cos\beta'}{4\pi f/P}$$

or $T = K_T I_{dc}^2$ ....(4.39)

where $K_T = \frac{9}{2\pi^3} P K_m \cos\beta'$

K_T is constant if the firing angle remains at a fixed value. Thus the torque developed by the synchronous motor is directly proportional to the square of the d.c. link current like a conventional d.c. series motor.

The relationship between V_d, V_{dc}, R_{dc} and I_{dc} is given by

$$V_{dc} = V_d - I_{dc} R_{dc} \quad ....(4.40)$$

where $R_{dc} = R_d + R_f$

and R_d = Resistance of the d.c. link inductor

R_f = Resistance of the excitation winding of the synchronous motor.

V_d = Average d.c. voltage output of the bridge rectifier.

The d.c. voltage output of the machine converter is given by

$$V_{dc} = \frac{3\sqrt{6}}{\pi} V_{sy} \cos\beta \quad ....(4.41)$$

After substituting (4.16) into (4.41), the relationship between V_{dc}, N, and I_{dc} is obtained.

$$V_{dc} = \frac{3\sqrt{6}}{\pi} K_p I_{dc} f \cos\beta$$

$$= \frac{3\sqrt{6}}{\pi} K_p I_{dc} \cdot \frac{PN}{120} \cos\beta$$

or $$V_{dc} = K_N N I_{dc} \cos\beta \quad \ldots.(4.42)$$

where $$K_N = \frac{\sqrt{6}}{40\pi} P K_p$$

The equation (4.40) is substituted into (4.42) to yields the expression for speed in terms of V_d, β & I_{dc}.

$$N = \frac{V_d - I_{dc} R_{dc}}{K_N I_{dc} \cos\beta} \quad \ldots.(4.43)$$

Thus the speed of the synchronous motor can be changed by varying either d.c. link voltage or firing angle of the inverter.

4.3 COMPUTER ALGORITHM

The mathematical equation derived in the previous section are used for computing analytically the performances of the commutatorless d.c. series motor drive on a digital computer. The flow chart for calculating the performances of the drive is given in Fig. 4.5. At the beginning of the program, drive parameters such as X_d, X_q X_c, K_e, R_d, R_f, P, K & q are inputted to the computer. The initial values : V_{do}, I_{dco} and α_o are also supplied to the computer. Initially the firing angle of line commulated inverter is incremented by $\Delta\alpha$ and the displacement

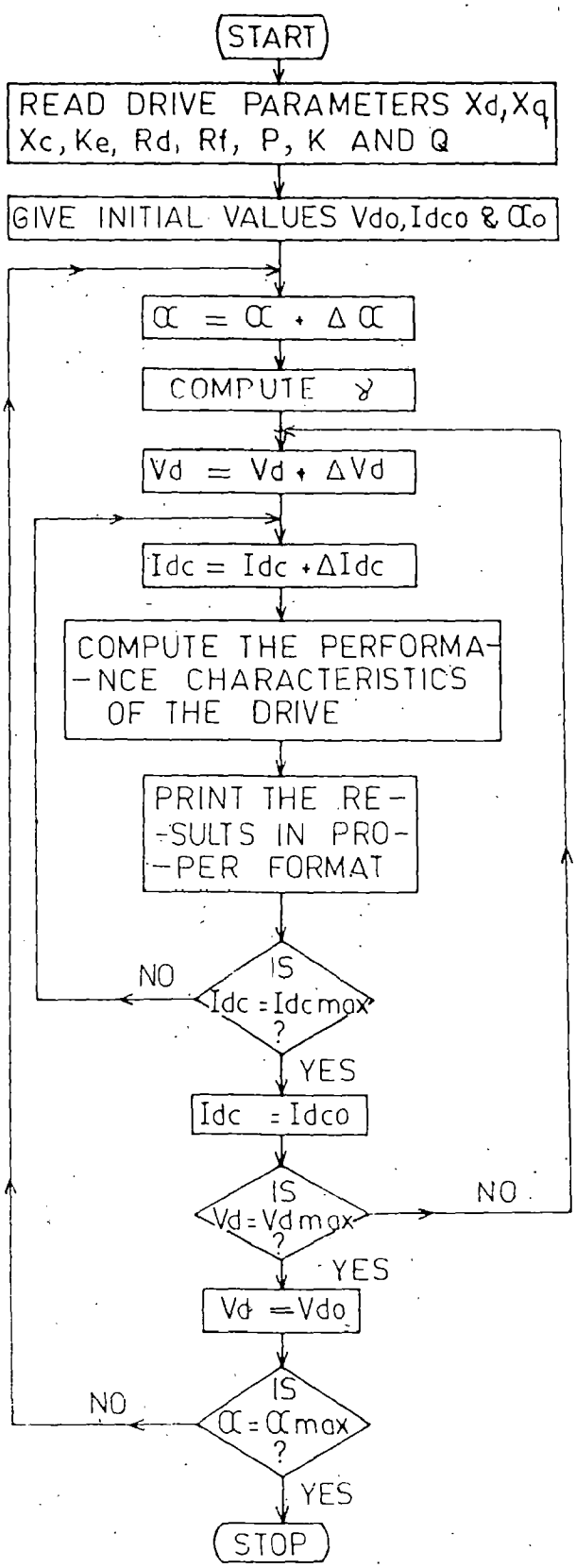


FIG. 4.5 FLOW CHART FOR COMPUTING PERFORMANCE CHARACTERISTICS OF SCLM

angle r is calculated by using the equation (4.30). The d.c. link voltage is increased by a step of ΔV_d and the characteristics of the drive is computed by varying the d.c. link current in step of ΔI_{dc}. The turn off angle and power factor are calculated by using equation (4.33) and (4.22) respectively. The commutation angle μ is found from equation (4.26).

The machine loaded terminal voltage V_{sy} and current I_{sy} are computed with the help of equation (4.15) and (4.6) respectively after calculating speed from (4.43). The power input to the machine and torque developed by the synchronous motor are determined from (4.37) and (4.39). This computation process is repeated for different combination of firing angle and d.c. link voltage until they exceed the maximum values.

4.4 CONCLUSIONS

The complete steady state performance equations of commutatorless d.c. series motor have been derived in this chapter. The no load induced voltage and terminal voltage are found in terms of machine speed and d.c. link current. The power factor of the synchronous motor is derived in terms of machine parameter and supplementary displacement angle r between no load induced voltage and machine current. The power factor, commutation over-lap angle and margin angle are found to be independent of d.c. link current

and machine speed.

The expressions for speed, torque developed and input power for commutatorless d.c. series motor indicate the similar characteristics like a conventional d.c. series motor. A computer algorithm for computing the performance characteristics of a SCLM system has also been discussed in this chapter.

CHAPTER - V

STEADY STATE PERFORMANCE OF THE SYSTEM

5.1 GENERAL

This chapter deals with the steady state performance characteristics of the commutatorless d.c. series motor, computed from the mathematical equations derived in the previous chapter. The performance is calculated for several values of d.c. link voltage and firing angle of the line commutated inverter (LCI).

This chapter also deals with the experimental studies on the microprocessor controlled commutatorless d.c. series motor drive. The results obtained from the experimental investigations have been compared with the analytical ones and the discrepancies between the two are discussed. The oscillograms of the machine terminal voltage, stator current, d.c. link voltage, d.c. link current and voltage waveforms at different points of the firing control circuit are also given.

5.2 COMPUTATION OF PERFORMANCE CHARACTERISTICS AND THEIR EXPERIMENTAL VERIFICATIONS

5.2.1 Computation of Characteristics:

The steady state performance of the commutatorless d.c. series motor is computed by using the mathematical equations derived in the previous chapter on a digital computer. Fortran

program is developed for the computation of characteristics of the drive, whose parameters have been given in Appendix-I, with the help of algorithm discussed in chapter IV, The computer program is given in Appendix-IV. Various performance characteristics of the drive viz, Torque Vs. speed, Torque Vs. d.c. link current, speed Vs. d.c. link current, Terminal voltage Vs. machine current, power factor Vs. d.c. link current, commutation angle Vs. d.c. link current, d.c. link voltage Vs. d.c. link current, machine current Vs. d.c. link current and real & reactive power Vs. d.c. link current are computed and are shown in Figs. 5.3 to 5.11. These characteristics are discussed along-with corresponding experimental results in section 5.3.

5.2.2. Experimental Investigations:

The objectives of the experimental investigation are to study the steady state performance characteristics of the series commutatorless d.c. motor (SCLM) drive. The details of the synchronous machine and d.c. machine on which the experiments are carried out, are given in Appendix-I. The experimental investigations to obtain the steady state performance of the SCLM system have been studied in two parts:

i) No load tests

ii) Load tests

A manual starting procedure discussed in chapter-II

has been adopted to start the commutatorless d.c. series motor. No load tests are carried by varying d.c. link voltage with constant firing angle and changing firing angle with constant d.c. link voltage. From the results of no load tests, following no load steady state characteristics are obtained

(a) Speed Vs. d.c. link voltage for different values of firing angles.

(b) Speed Vs. firing angle for different values of d.c. link voltages.

The experimental performance of the SCLM system under load is obtained with the help of coupled d.c. machine running as separately excited d.c. generator. Load tests are carried out on the commutatorless d.c. series motor by varying the load on the synchronous motor with d.c. link voltage and firing angle kept constant. From the experimental results, following characteristics are obtained:

i) Torque Vs. speed

ii) Torque Vs. D.C. link current

iii) Speed Vs. D.C. link current

iv) Inverter d.c. terminal voltage Vs. d.c. link current characteristics

v) Active and reactive power Vs. D.C. link current

vi) Power factor & efficiency Vs. D.C. link current

vii) Terminal voltage Vs. D.C. link current

viii) Turn-off angle & commutation over lap angle Vs. D.C. link current.

5.3 RESULTS AND DISCUSSIONS.

The experimental characteristics of commutatorless d.c. series motor at no load and loaded conditions are shown in Figs. 5.1 to 5.11. The computed characteristics of the SCLM system are also given with the experimental characteristics. The oscillograms of the waves-shapes at different points of the firing circuit, machine terminal voltage and current, d.c. link voltage and current are recorded at no load and loaded conditions and are shown in Figs. 5.12 to 5.13.

The following salient features on the performance of series commutatorless d.c. motor may be observed from the results.

1. It can be observed from Fig. 5.1 that under no load condition synchronous motor speed increases with the increase of d.c. link voltage with constant firing angle of the line commutated inverter. The motor speed rises almost linearly with the d.c. link voltage. The speed of the motor is seen to be highly sensitive with the variation of d.c. link voltage compared to that with firing angle change. It is also observed that the characteristic curve moves upward with the decrease of inverter firing angle.

Fig. 5.2 shows the variation of no load motor speed with firing angle at constant d.c. link voltage. The firing angle must be within the safe region to avoid commutation failure. So large range of speed variation is not possible

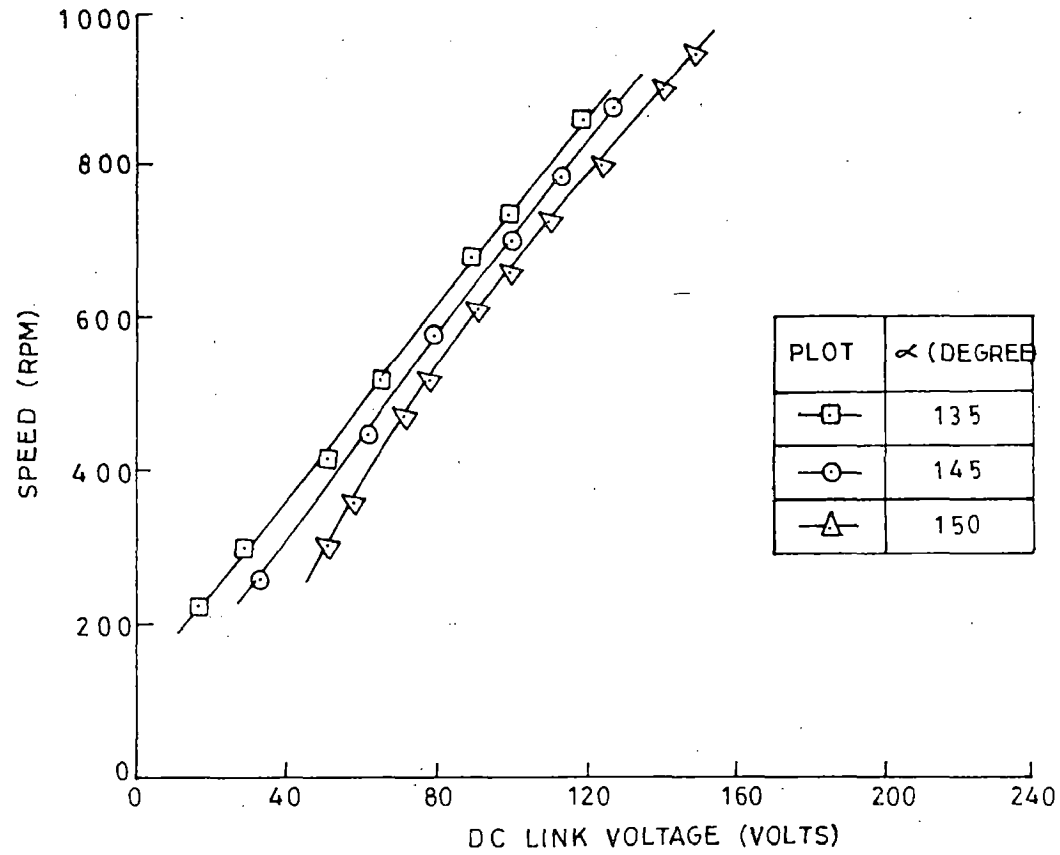


FIG. 5·1—NO LOAD SPEED Vs. DC LINK VOLTAGE CHARACTERISTIC

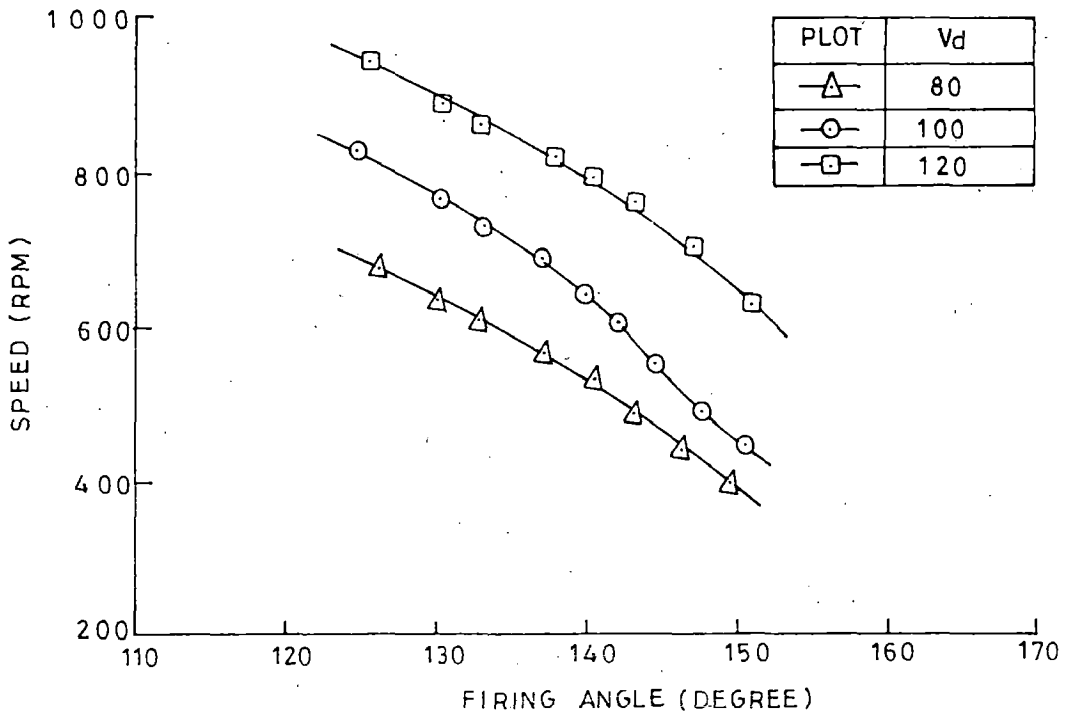


FIG. 5·2—NO LOAD SPEED Vs. FIRING ANGLE CHARACTERISTIC

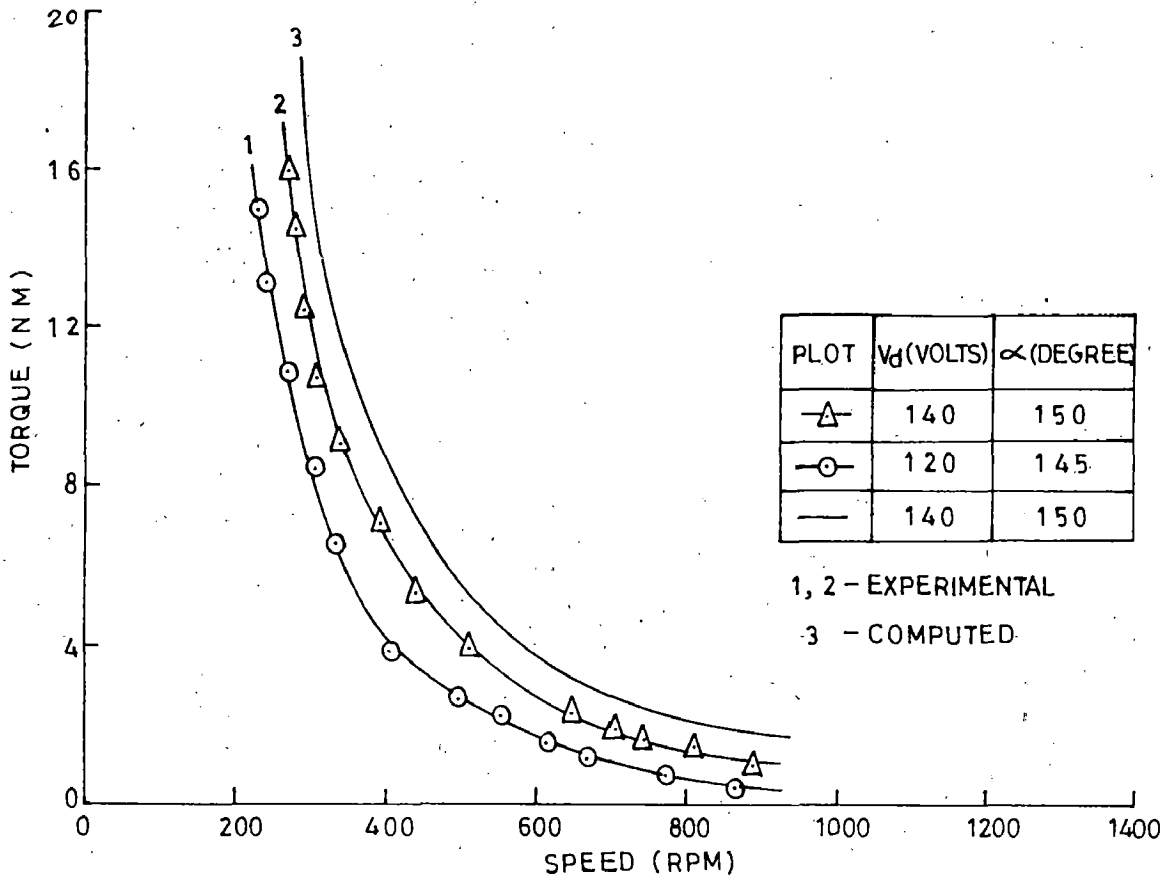


FIG. 5·3–TORQUE Vs. SPEED CHARACTERISTICS

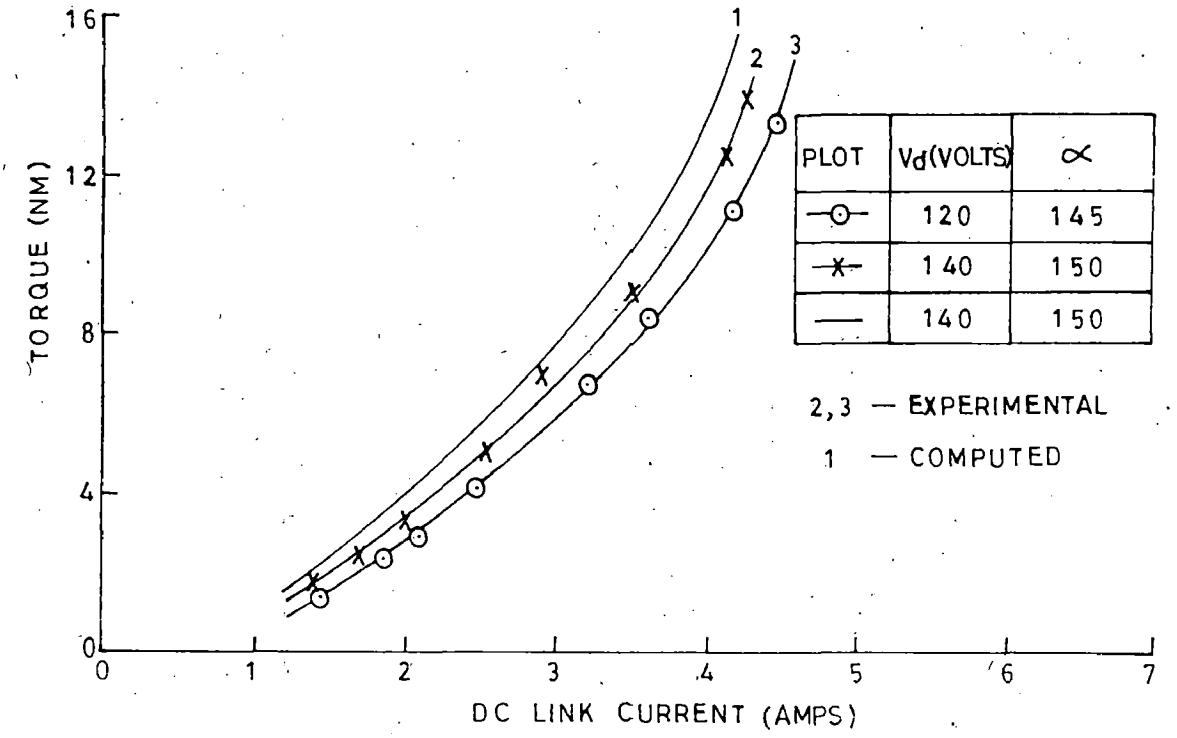


FIG. 5·4– TORQUE Vs. DC LINK CURRENT CHARACTERISTICS

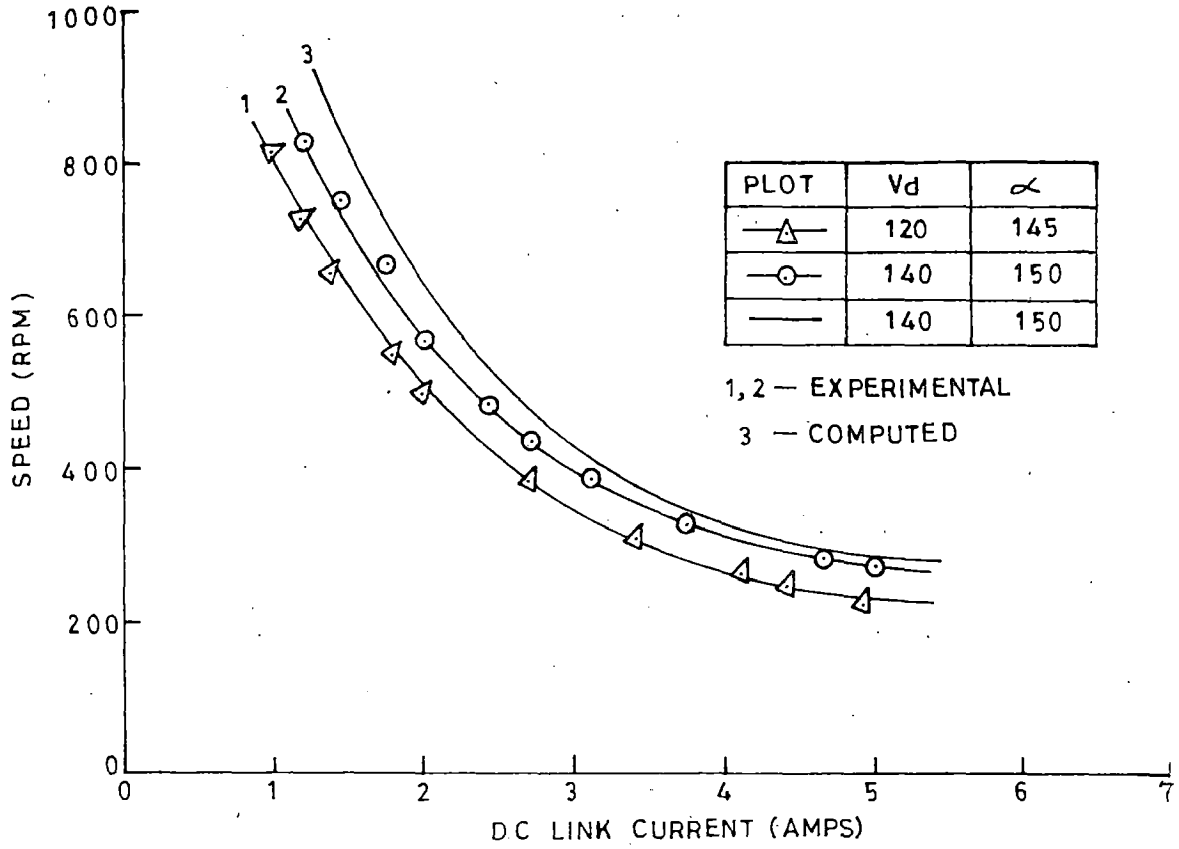


FIG 5 5 SPEED Vs. DC LINK CURRENT CHARACTERISTICS

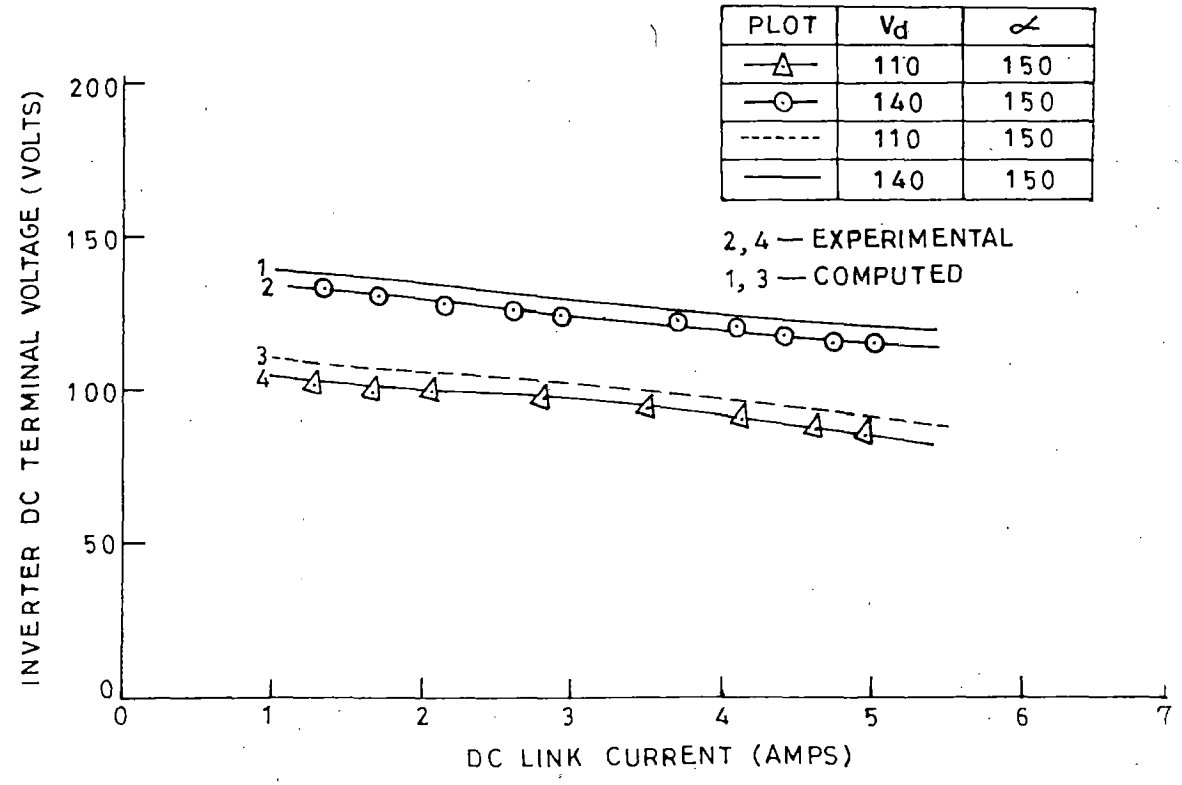


FIG. 5·6 — INVERTER DC TERMINAL VOLTAGE Vs. DC LINK CURRENT CHARACTERISTICS

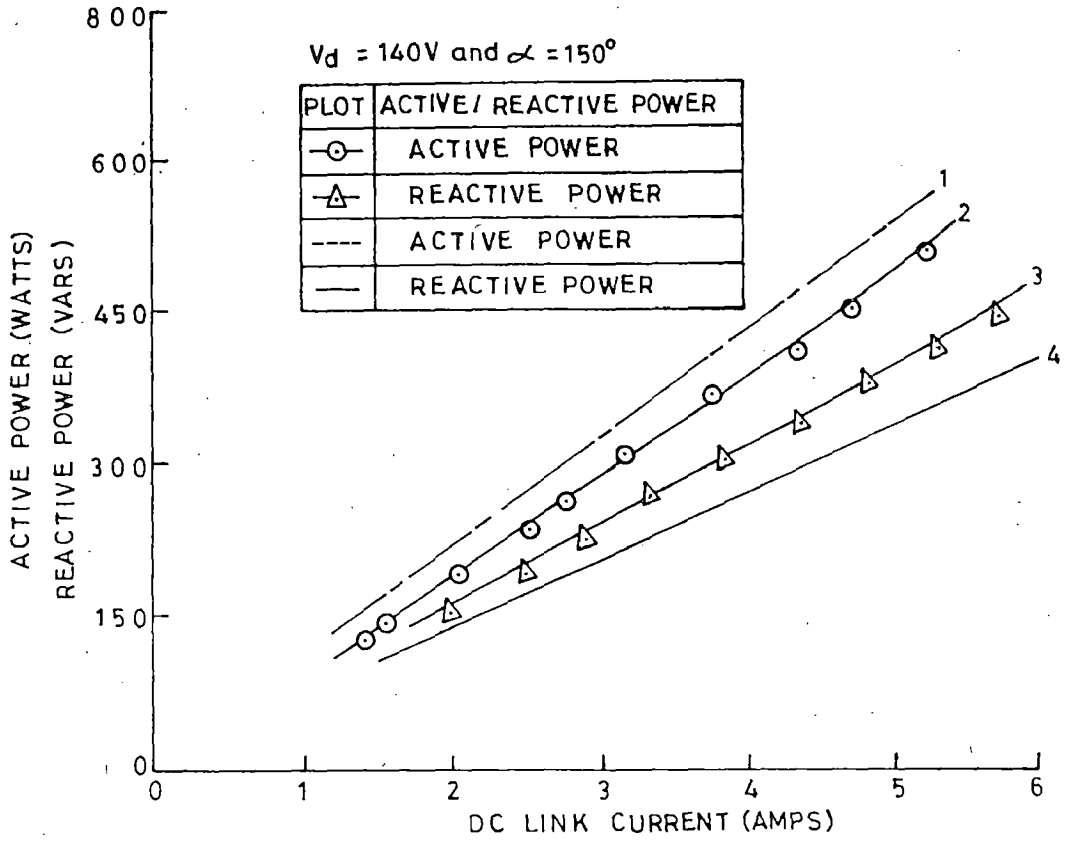


FIG. 5·7—ACTIVE AND REACTIVE POWER Vs. DC LINK CURRENT CHARACTERISTICS

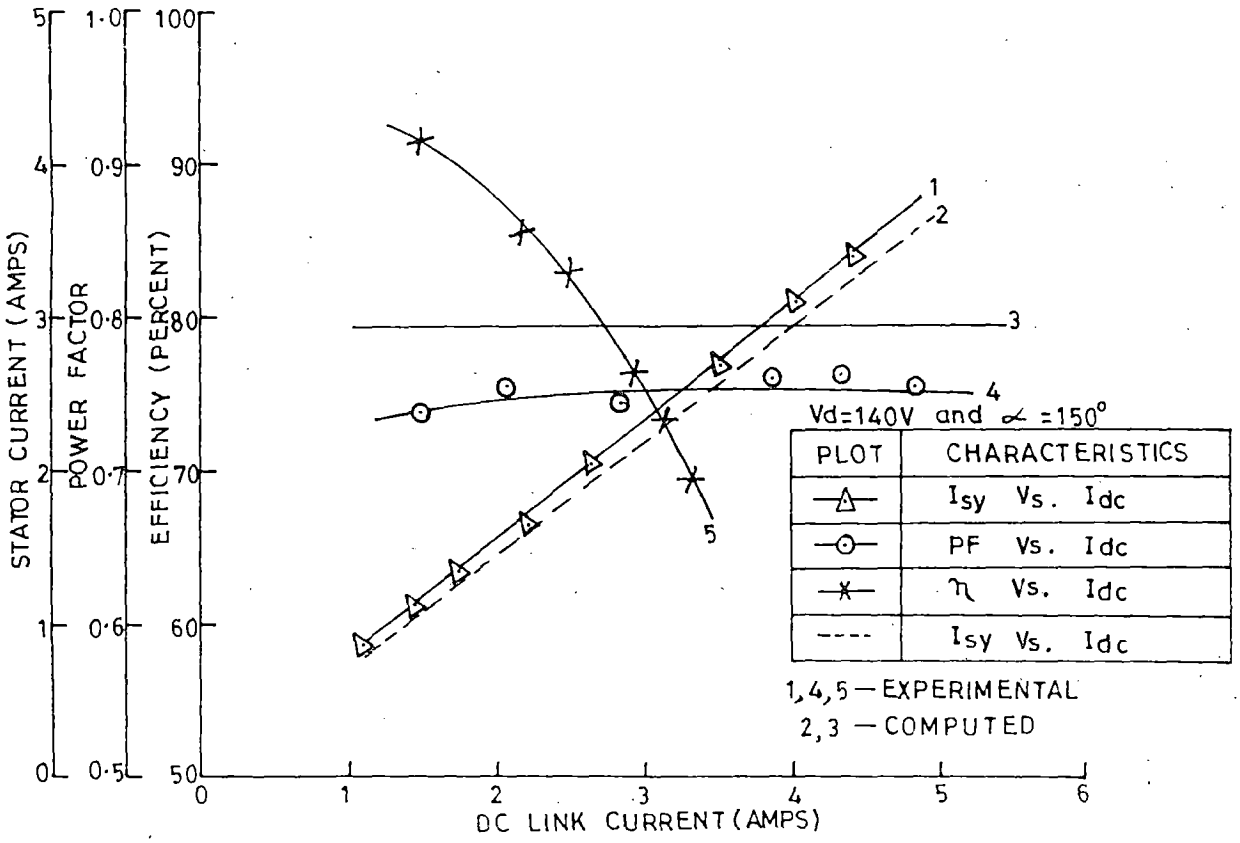


FIG. 5·8—STATOR CURRENT, POWER FACTOR AND EFFICIENCY Vs. DC CURRENT CHARACTERISTICS

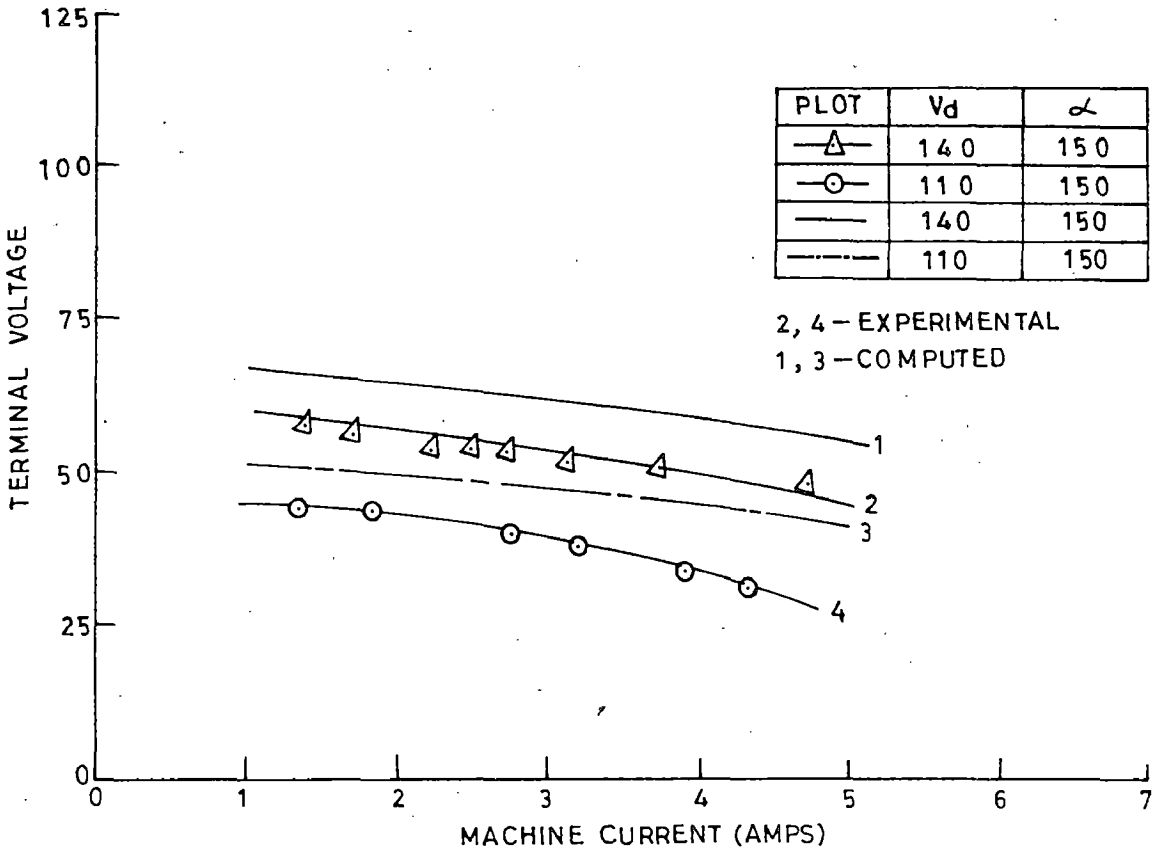


FIG. 5·9 — TERMINAL VOLTAGE Vs. MACHINE CURRENT CHARACTERISTICS

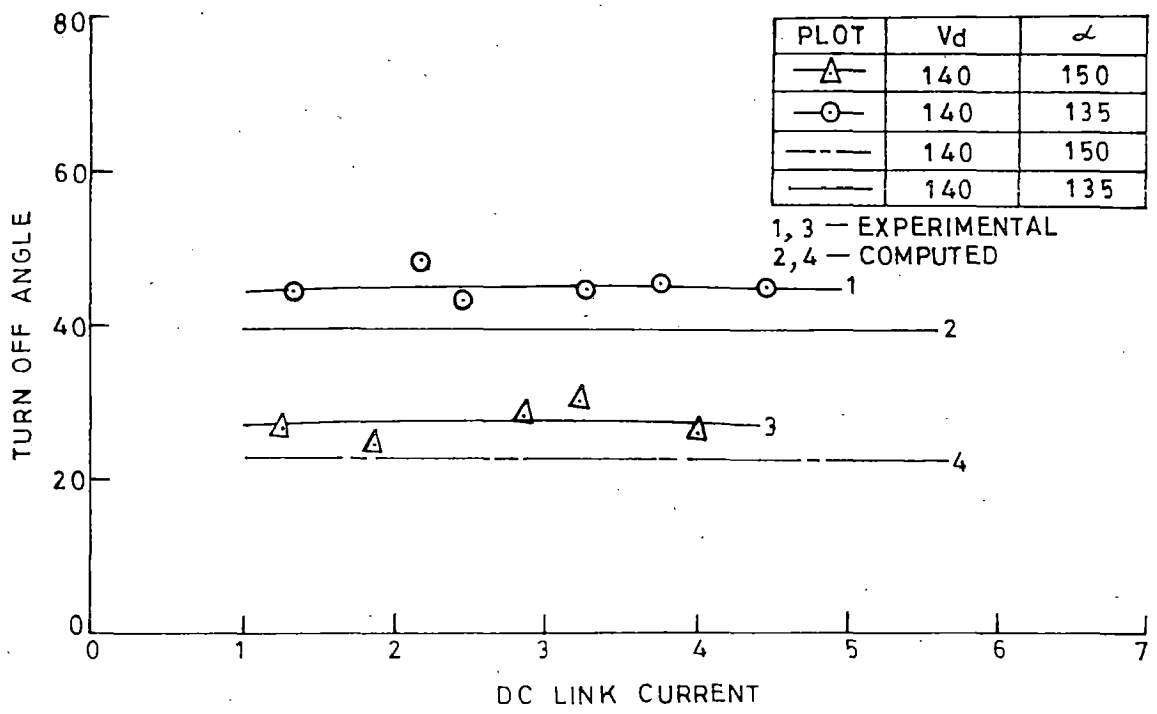


FIG. 5·10 — TURN OFF ANGLE Vs. DC LINK CURRENT CHARACTERISTICS

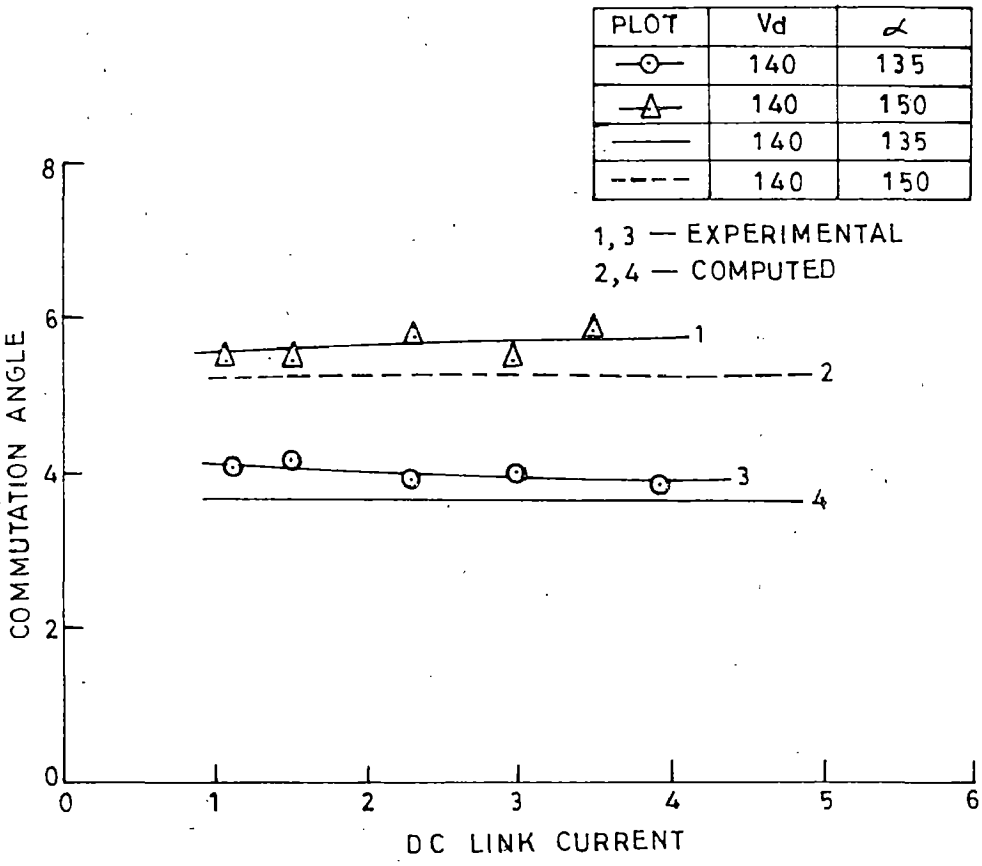


FIG. 5·11 – COMMUTATION ANGLE Vs. DC LINK CURRENT CHARACTERISTICS

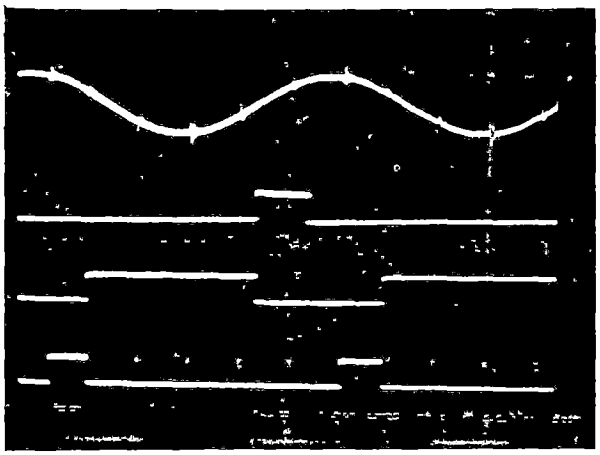


Fig. 5.12(a) Waveforms of machine terminal voltage V_{AC}, synchronizing signal, counter TM1(2) output & counter TM2(2) output.

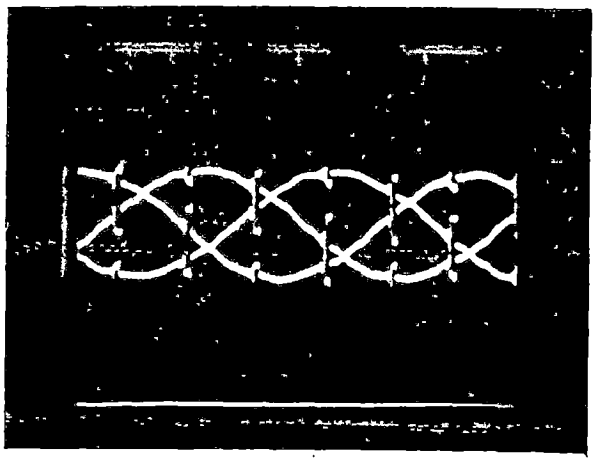


Fig. 5.12(b) Waveforms of terminal voltages V_{AB}, V_{BC} & V_{CA}

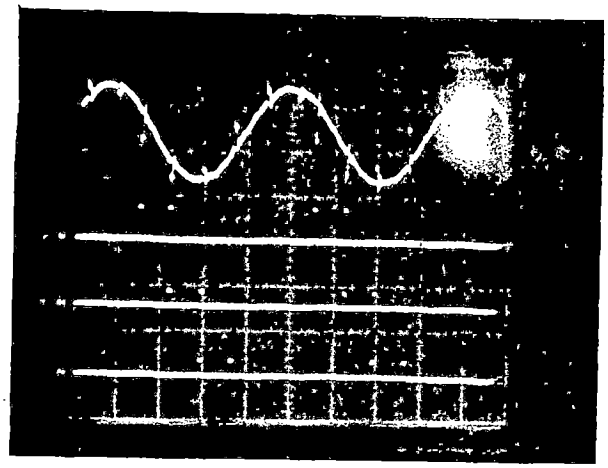


Fig. 5.12(c) Oscillograms of V_{AC} and firing pulses of channels 1, 2 & 3.

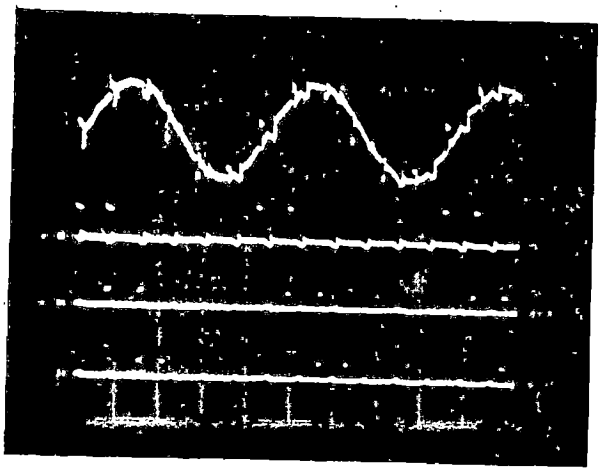


Fig. 5.12(d) Oscillograms of V_{AC} and firing pulses of channels 4, 5 & 6.

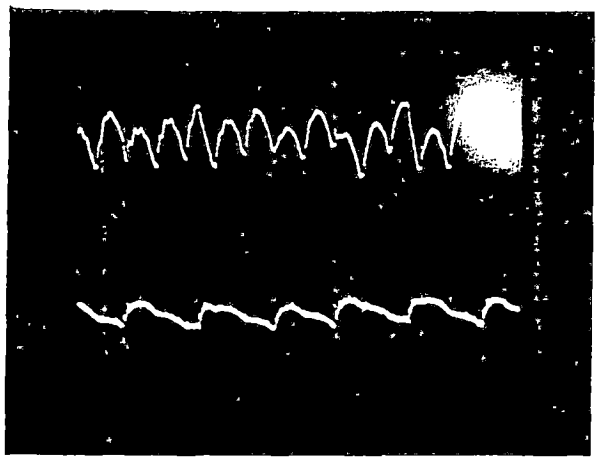


Fig. 5.13(a) Waveforms of d.c. link voltage and current at no load condition when V_d=90V, I_{dc}=1.2 amps. & N=550 rpm.
Time/div : 1ms

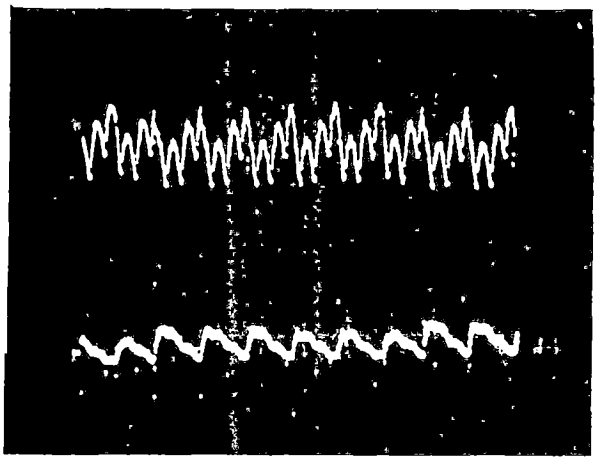


Fig. 5.13(b) Waveforms of d.c. link voltage and current at loaded condition when V_d=90V I_{dc}= 1.5 amps.& N=490 rpm
Time/div : 10ms

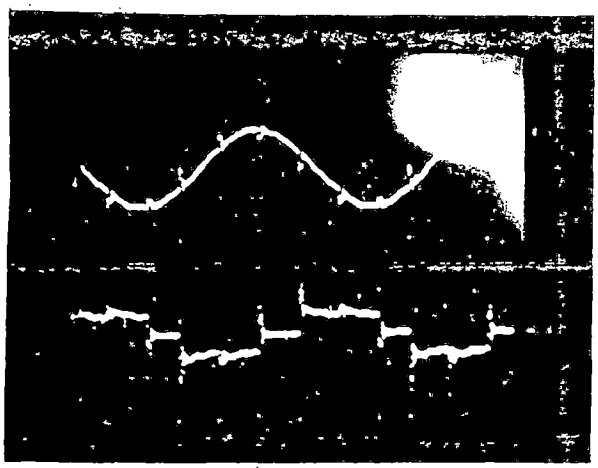


Fig. 5.13(c) Machine terminal voltage and current waveforms at no load condition when V_{sy}=60V I_{sy}=0.9 amps & N=560rpm
Time/div : 1ms

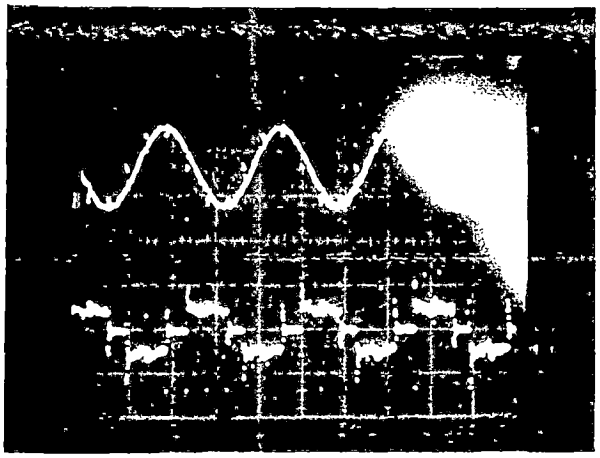


Fig. 5.13(d) Machine voltage and current waveforms at loaded condition when V_{sy}=58V, I_{sy}=1.3 amps & N=460 rpm
Time/div : 10ms

by firing angle change as may be observed from Fig. 5.2.

2. It is observed from Fig. 5.3 that the SCLM system exhibits similar torque Vs. speed characteristic like a conventional d.c. series motor. It is obvious that at lower motor speed, torque is very high and becomes low at higher speed.

Torque Vs. speed characteristic curve is shifted upward with increase in firing angle. From Fig. 5.3, it is also observed that a good correlation exists between experimental and computed results. The computed torque is found to be slightly more than the experimental ones. It is due to neglecting power losses in the line commutated inverter section and friction and windage losses in the rotating machines.

3. The variation of torque with the d.c. link current for different combination of d.c. link voltage and firing angle is shown in Fig. 5.4. This characteristic exactly correlates with that of conventional d.c. series motor. The computed torque is observed to be slightly more than the torque obtained experimentally due to neglecting power losses as mentioned earlier.

4. It is observed from Fig. 5.5 that the synchronous motor speed changes with load like a conventional d.c. series motor. In Fig. 5.5, good correlation is observed between experimental and theoretical results. Fig. 5.6

shows the variation of inverter d.c. terminal voltage with d.c. link current at different setting of V_d. It is observed that this voltage decreases slightly with the increase of d.c. link current. Computed characteristic is very close to the experimental ones.

5. From Fig. 5.7 it may be observed that active and reactive power increase almost linearly with the increase of d.c. link current. It is due to fact that the power factor remains constant with the variation of load and the motor terminal voltage decreases very slowly with the increase of d.c. link current. Good correlation is observed between measured and computed results.

6. It is observed from Fig. 5.8 that the stator current of the synchronous motor changes linearly with d.c. link current. The power factor of the synchronous motor is found to be independent of d.c. link current. Motor efficiency decreases with the increase of d.c. link current.

7. Fig. 5.9 shows the variation of terminal voltage with stator current. This voltage decreases slowly with machine current. Terminal voltage depends upon load current and speed of the synchronous machine. If the d.c. link current increases then speed decreases and therefore the terminal voltage does not change to a great extent. It is clear from Fig. 5.10 and 5.11 that turn off angle and commutation overlap angle are independent of d.c. link current.

8. The oscillograms of machine terminal voltage V_{AC}, synchronizing signal, output of counter TM1(2) and output of counter TM2(2) are shown in Fig. 5.12(a). These are exactly identical to the theoretical ones given in Chapter-II. The waveforms for machine terminal voltages V_{AB}, V_{BC} & V_{CA} are given in Fig. 5.12(b) in which the commutation spikes are clearly visible at 60^{o} interval. Fig. 5.12(c) & 5.12(d) show the waveforms of V_{AC} and firing pulses for all six channels. The oscillograms of d.c. link voltage and current at no load and loaded conditions of the drive are given in Fig. 5.13(a) and 5.13(b) respectively. It is observed that the ripples content in d.c. link current is small due to high inductance in the d.c. link.

9. The voltage and current waveforms at motor terminals under no load and loaded conditions are shown in Fig. 5.13(c) and 5.13(d). The voltage waveforms are sinusoidal with notches at 60^{o} interval due to commutation of the thyristors. But the motor currents are of rectangular shape and rich in harmonics as expected for continuous d.c. link current.

The SCLM system works satisfactorily at no load and loaded conditions and will find good applications in various industries in place of conventional d.c. series motor.

5.4 CONCLUSIONS

The present scheme works satisfactorily at no load as well as at loaded conditions. Microprocessor based firing

control circuit generates reliable firing pulses for thyristors of the inverter in proper sequence in presence of commutation spikes in the terminal voltage of the synchronous machine and on line firing angle control has been achieved. The series commutatorless motor has same characteristics as exhibited by a conventional d.c. series motor. Good correlation has been observed between the experimental and the computed results, thus establishing the validity of developed analytical model. The SCLM system provides excellent performance due to reliable firing pulses generated by the microcomputer and will find good applications like traction, drilling, lifting and hoisting, etc. in place of conventional d.c. series motor.

CHAPTER - VI

CONCLUSIONS AND SUGGESTIONS FOR FURTHER WORK

6.1 MAIN CONCLUSIONS

The work presented in this thesis covers the design and fabrication of a microprocessor controlled firing scheme for line commutated inverter, experimental investigations on the performance of commutatorless d.c. series motor and also the steady state analysis of the drive. The main conclusions of the present work are summarised as follows:

(i) The power circuits and an open loop firing angle control scheme using less hardware components have been designed and fabricated. This firing circuit works satisfactorily in presence of commutation spikes in the terminal voltage of the synchronous machine. The recorded waveforms at the different points of firing circuit are observed identical to the theoretical ones. Linear on line firing angle control is achieved with this scheme.

(ii) From the experimental investigations, it is observed that the system is stable at no load as well as loaded conditions. The variation of speed has been obtained with the help of d.c. link voltage and firing angle. It is also verified that commutatorless d.c. series motor exhibits characteristics similar to conventional d.c. series motor. The power factor, commutation over lap angle and turn off

angle are found to be independent of load and machine speed.

(iii) The computed results under loaded condition of the drive shows the good correlation with test results, thus estabilishing the validity of developed analytical model. Moreover the developed analytical technique based on equivalent circuit approach requires small computational time and marginal memory storage of computer.

(iv) The terminal voltage of the synchronous motor is observed sinusoidal under all conditions with small notches spaced at 60^{o} interval occuring due to the commutation of the thyristors of line commutated inverter. The duration of the spike is equal to the commutation over lap angle and is quite small.

(v) The stator current of the synchronous motor is not sinusoidal. The current is of rectangular waveforms with little commutation spike at 60^{o} interval. The current waveforms are rich in harmonics.

The microcomputer based firing control scheme works satisfactorily. The commutatorless d.c. series motor gives excellent performance due to reliable firing pulses generated by the microcomputer and will find good applications like traction, drilling, lifting and hoisting etc. in place of conventional d.c. series motor.

6.2 SUGGESTIONS FOR FURTHER WORK

The main objectives of this dissertation have been successfully realized. During the course of investigation, some problems have arisen which would require further investigation. Therefore this work can be extended on the following aspects:

i) Series commutatorless motor is not self starting hence it is an important need to develop suitable starting method for the system.

ii) In the present work steady state analysis of the drive has been developed using steady state equivatent circuit. So a dynamic model may be derived to study the transient and dynamic performance of the system.

iii) The entire work was in open loop form however, for fast response and better stability, tne closed loop control system may be deviced for the drive.

iv) The present work ignores magnetic saturation effect, inverter losses and no load losses to simplify the derivations for steady state analysis of the drive. The effects of these factors on the drive performance may also be studied.

v) An analytical model may be developed for the analysis of starting performance of the drive.

vi) The stability analysis of the system should be carried out for designing closed loop system.

vii) The effect of harmonics on the steady state performance of the drive may be studied.

viii) Investigations on the series commutatorless motor using higher rating synchronous machine should be carried out to generalize the analysis approach and to explore this type of drive for various industrial applications.

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APPENDIX - I

DETAILS AND PARAMETERS OF MACHINES USED

Details of Machines used

Synchronous motor:

Elektromotoren Werke Kaiser, Berlin

3 ph, Y, 400V, 10.8A, 7.5 KVA, Cosϕ = 0.8

1500 rpm, 50 Hz.

Exc. 40V, 8A

D.C. Motor:

Elektromotoren Werke Kaiser, Berlin

220V, 42A, 8KW, 1500 rpm.

Parameters of Machines Used

Synchronous motor:

X_d = 21.51 ohms/phase, X_q = 13.87 ohms/phase

X_2 = 3.84 ohms/phase, R_{sy} = 1.88 ohms/phase

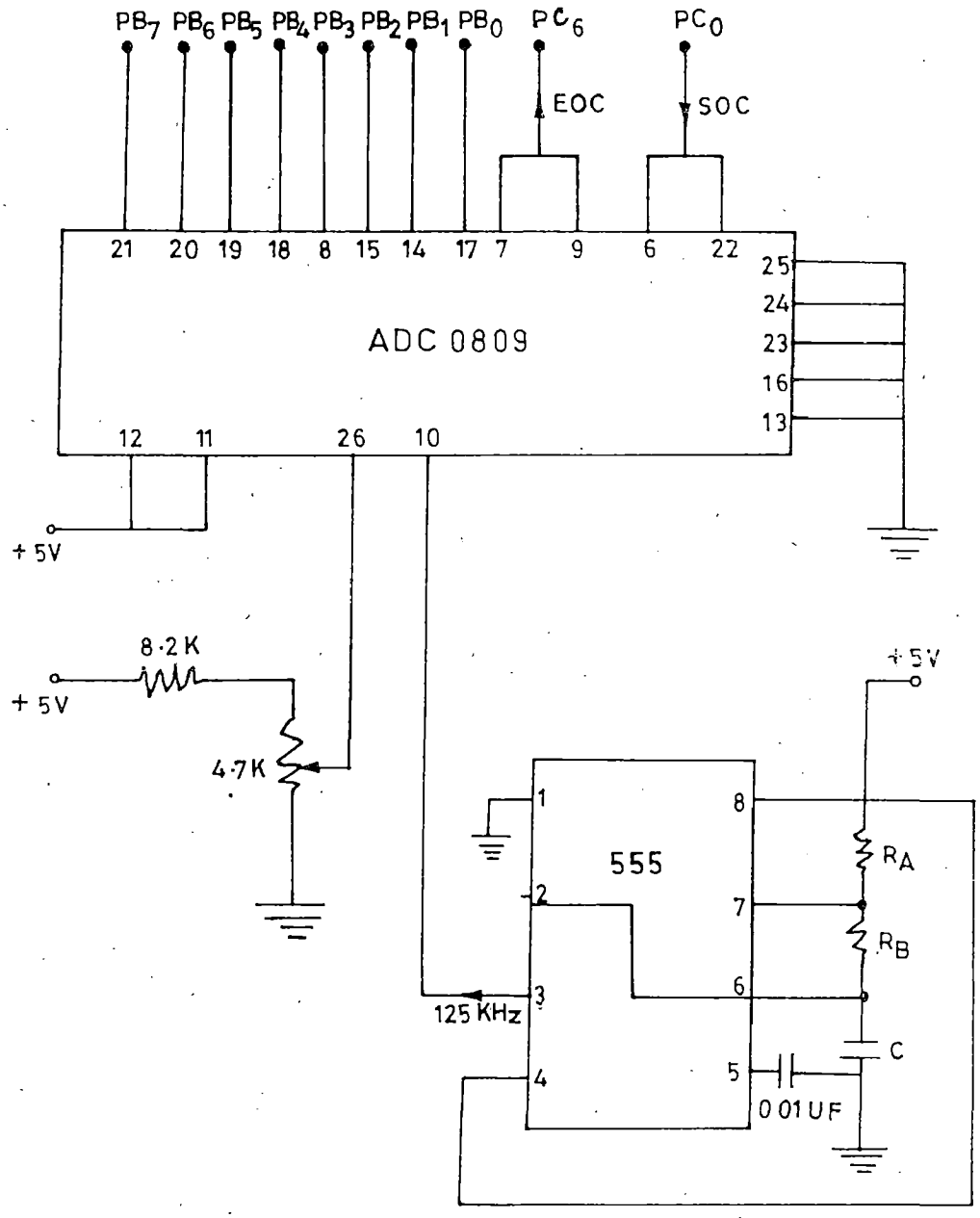
R_f = 3.67 ohms

D.C. motor:

R_a = 2.12 ohms

APPENDIX-II

DETAILS OF ADC 0809 INTERFACING CIRCUIT



R_A = 1K

R_B = 82

C = 0·01 μF

APPENDIX - III

MAIN PROGRAM

LEBEL	ADDRESS	CONTENTS	MNEMONICS	COMMENTS
	6000	31, FF, 7F	LXI SP STACK	INITIALIZE STACK POINTE
	6003	3E, 8A	MVI A, 8AH	INITIALIZE 8255(2) IN
	6005	D3, 0B	OUT 0BH	MODE '0'
	6007	3E, 00	MVIA, 00H	MAKE ALL BITS OF
	6009	D3, 08	OUT 08H	PORTA LOW
	600B	3E, 54	MVIA, 54H	INITIALIZE TM1 OF
	600D	D3, 13	OUT 13H	8253(1) IN MODE 2
	600F	3E, 03	MVIA, 03H	LOAD TM1 OF 8253(1)
	6011	D3, 11	OUT 11H	FOR 511.67 KH_Z OUTPUT
	6013	3E, B0	MVI a, B0H	INITIALIZE TM2 OF
	6015	D3, 13	OUT 13H	8253(1) IN MODE '0'
	6017	3E, 70	MVI A, 70H	INITIALIZE TM1 OF
	6019	D3, A3	OUT A3H	8253(2) IN MODE '0'
	601B	3E, B0	MVI A, B0H	INITIALIZE TM2 OF
	601D	D3, A3	OUT A 3H	8253(2) IN MODE 0
	601F	F3	DI	DISABLE INTERRUPT SYSTEMS
	6020	3E, 56	MVI A, 56H	INITIALIZE 8259
	6022	D3, 28	OUT 28H	IN FULLY NESTED
	6024	3E, 61	MVI A, 61H	MODE
	6026	D3, 29	OUT 29H	
	6028	3E, EA	MVI A, EAH	UNMASK IR_0, IR_2 & IR_4 INT CHANNELS
	602A	D3, 29	OUT 29H	
	602C	21, 70, 64	LXI H ADDR9	
	602F	22, 78, 61	SHLD ADDR14	

START1	6032	DB, 0A	IN PORTC	IMPORT THE PC7 BIT
	6034	17	RAL	PC7 BIT IN CARRY
	6035	DA, 32, 60	JC START1	IS PC7=0? No, JUMP TO START1
	6038	3E, FF	MVI A, FFH	LOAD TM2(1) WITH
	603A	D3, 12	OUT 12H	FFFFH
	603C	3E, FF	MVI A, FFH	
	603E	D3, 12	OUT 12H	
START2	6040	DB, 0A	IN PORTC	IMPORT PC7 BIT
	6042	17	RAL	
	6053	D2, 40, 60	JNC START2	IS PC7=1? NO, JUMP TO START2
START3	6046	DB, 0A	IN PORTC	IMPORT PC7 BIT
	6048	17	RAL	
	6049	DA, 46, 60	JC START3	IS PC7=0? No, JUMP TO START3
	604C	21, 5F, 61	LXI H,(ADDR8-1)	
	604F	22, 66, 61	SHLD ADDR0	
NEW	6052	DB, 12	IN 12H	INPUT LOWER BYTE OF TM2(1)
	6054	4F	MOV C, A	GET LOWER BYTE IN REGISTERS C
	6055	DB, 12	IN 12H	INPUT HIGHER BYTE OF TM2(1)
	6057	47	MOV B, A	GET THE BYTE IN REGISTER B
	6058	21, FF, FF	LXI H, FFFF	
	605B	08	DSUB	
	605C	22, 68, 61	SHLD ADDR1	SAVE 60^{o} IN ADDR1
	605F	AF	XRA A	CLEAR CARRY
	6060	7C	MOV A, H	

	6061	1F	RAR	ROTATE RIGHT
	6062	57	MOV D, A	GET ROTATED BYTE IN D
	6063	7D	MOV A, L	
	6064	1F	RAR	ROTATE RIGHT
	6065	5F	MOV E, A	GET ROTATED BYTE IN E
	6066	19	DAD D	ADD 60° WITH 30°
	6067	22, 6A, 61	SHLD ADDR2	SAVE 90° IN ADDR2
	606A	22, 76, 61	SHLD ADDR13	
	606D	3E, FF	MVI A, FFH	LOAD TM2(1)
	606F	D3, 12	OUT 12H	WITH FFFFH
	6071	3E, FF	MVI A, FFH	
	6073	D3, 12	OUT 12H	
	6075	CD, 20, 62	CALL ADC	GET FIRING ANGLE INFORMATION
	6078	CD, 50, 62	CALL DIVISION	DIVIDE 90° COUNT BY 5AH
	607B	CD, B0, 62	CALL MULT	
	607E	EB	XCH G	GET THE PRODUCT IN (D,E)
	607F	2A, 76, 61	LHLD ADDR13	GET 90° IN (H,L)
	6082	19	DAD D	(H,L)CONTAINS FIRING ANGLE DELAY
	6083	22, 74, 61	SHLD ADDR7	SAVE FIRING ANGLE DELAY IN ADDR7
REPEAT	6086	2A, 66, 61	LHLD ADDR0	LOAD (H,L)WITH FIRING PLUSE COMMAND ADDRESS
WAIT	6089	FB	ET	ENABLE INTERRUPT SYSTEMS
	608A	76	HLT	WAIT FOR THE INTERRUPT
	608B	F3	DI	
	608C	00, 00, 00	NOP	

```
          608F    7D          MOV A, L
          6090    FE, 60      CPI 60H
          8092    D2, 9C, 60  JNC INTR2     IS F5=1? YES JUMP
                                            TO INTR2
          6095    00  00      NOP
          6097    00  00      NOP
          6099    C3, 89, 60  JMP WAIT
INTR2     609C    FE, 61      CPI 61H
          609E    D2, A8, 60  JNC INTR3     IS FS=2? YES. JUMP
                                            TO INTR3
          60 A1   00  00      NOP
          60 A3   00  00      NOP
          60A5    C3, 52, 60  JMP NEW
INTR3     60A8    FE,  2      CPI 62H
          60AA    DA, BF, 60  JC DISPLAY    IS FS=3? NO JUMPT
                                            TO DISPLAY
          60AD    FE, 65      CPI 65H
          60AF    C2, C2, 60  JNZ UNMASK    IS FS COMPLETED? NO,
                                            JUMP  TO UNMASK
          60B2    21, 5F, 61  LXI H,(ADDR8-1)
          60B5    22, 66, 61  SHLD ADDR0
          60B8    00  00      NOP
          60BA    00  00      NOP
          60BC    C3, 86, 60  JMP REPEAT
DISPLAY   60BF    CD, F0, 62  CALL SPEED    DISPLAY SPEED
UNMASK    60C2    00  00      NOP
          60C4    00  00      NOP
          60C6    C3, 89, 60  JMP WAIT
```

IR_0 INTERRUPT SUBROUTINE

6180	F5	PUSH PSW	SAVE PSW
6181	00,00,00	NOP	
6184	3A, 74, 61	LDA ADDR7	LOAD TM1(1)
6187	D3, A1	OUT, A1H	WITH FIRING
6189	3A, 75, 61	LDA ADDR7+1	ANGLE DELAY
618C	D3, A1	OUT A1H	
618E	F3	DI	DISABLE INTERRUPT SYSTEMS
618F	3E, 60	MVI A, 60H	END OF INTERRUPT IR_0
6191	D3, 28	OUT 28H	
6193	F1		
6194	FB	EI	ENABLE INTERRUPT
6195	C9	RET	RESUME THE WORK

IR_2 INTERRUPT SUBROUTINE

61A0	F5	PUSH PSW	
61A1	00,00,00	NOP	
61A4	23	INX H	
61A5	7E	MOV A, M	GET FIRING PLUSE COMMAND IN A
61A6	D3, 08	OUT PORT A	MAKE PARTICULAR BITS HIGH
61A8	3A, 68, 61	LDA ADDR1	LOAD TM2(2)
61AB	D3, A2	OUT A2H	WITH 60°
61AD	3A, 69, 61	LDA ADDR1+1	DELAY
61B0	D3, A2	OUT A2H	

	61B2	3E, 00	MVI A, 00H	MAKE ALL BITS
	61B4	D3, 08	OUT PORT A	OF PORT A LOW
	61B6	22, 66, 61	SHLD ADDR0	SAVE (H,L)
	61B9	F3	DI	DISABLE INTERRUPT SYSTEMS
	61BA	3E, 62	MVI A, 62H	END OF INTERRUPT
	61BC	D3, 28	OUT 28H	IR_2
	61BE	F1		
	61BF	FB		
	61C0	C9	RET	RETURN TO MAIN PROGRAM

IR_4 INTERRUPT SUBROUTINE

	61D0	F5	PUSH PSW	SAVE PSW
	61D1	00, 00, 00	NOP	
	61D4	23	INX H	
	61D5	7E	MOV A, M	MAKE SPECIFIED BITS
	61D6	D3, 08	OUT PORT A	HIGH
	61D8	7D	MOV A, L	
	61D9	FE, 65	CPI 65H	
	61DB	CA, E8, 61	JZ NOLOAD	IS FIRING SEQUENCE SIX? YES, JUMP TO NOLOAD
	61DE	3A, 68, 61	LDA ADDR1	LOAD TM2(2)
	61E1	D3, A2	OUT A2H	WITH 60° DELAY
	61E3	3A, 69, 61	LDA ADDR1+1	
	61E6	D3, A2	OUT A2H	
NOLOAD	61E8	3E, 00	MVI A, 00H	MAKE ALL PORT A
	61EA	D3, 08	OUT PORT A	BITS LOW

	61EC	FB	EI	ENABLE INTERRUPT
	61ED	22, 66, 61	SHLD ADDR0	SAVE (H,L) IN ADDR0
	61F0	F3	DI	DISABLE INTERRUPT SYSTEM
	61F1	3E, 64	MVI A, 61H	END OF
	61F3	D3, 28	OUT 28H	INTERRUPT IR_4
	61F5	F1	POP PSW	
	61F6	FB	EI	ENABLE INTERRUPT
	61F7	C9	RET	RETURN

ADC SUBROUTINE

	6220	3E, 01	MVI A, 01H	LOAD BYTE IN ACCUMULATOR TO SET PC_0
	6222	D3, 0A	OUT PORT C	SET PC_0
	6224	11, 01, 00	LXI D, COUNT	LOAD (D,E)WITH DELAY COUNT
	6227	CD, BC, 03	CALL DELAY	THIS IS A 12uS DELAY
	622A	3E, 00	MVI A, 00	LOAD BYTE IN ACCUMULATOR TO RESET PC_0
	622C	D3, 0A	OUT PORT C	RESET PC_0
READ	622E	DB, 0A	IN PORTC	IMPORT EOC SIGNAL
	6230	17	RAL	
	6231	17	RAL	GET PC_6 IN CARRY
	6232	D2, 2E, 62	JNC READ	IS CONVERSION OVER? NO, JUMP TO READ
	6235	DB, 09	IN PORT B	GET THE DATA IN ACCUMULATOR
	6237	32, 72, 61	STA ADDR6	SAVE ADC OUTPUT
	623A	32, F6, 27	STA 27F6H	
	623D	06, 00	MVI B, 00H	

	623F	CD, FA, 06	CALL MODDT	DISPLAY ADC OUTPUT IN DATA FIELD
	6242	C9	RET	RETURN TO MAIN PROGRAM

DIVISION SUBROUTINE

	6250	21, 00, 00	LXI H,0000H	LOAD(HL)WITH 0000H
	6253	22, 6C, 61	SHLD ADDR3	INITIALIZE THE
	6256	22, 6E, 61	SHLD ADDR4	MEMORY LOCATIONS
	6259	22, 70, 61	SHLD ADDR5	WITH 0000H
	625C	01, 5A, 00	LXI B,005AH	LOAD (BC) WITH 5AH
CONTINUE	625F	2A, 6A, 61	LHLD ADDR2	LOAD(HL)WITH DIVIDENT
	6262	EB	XCHG	GET DIVIDENT IN(DE)
	6263	18	RDLC	GET MSB IN THE CARRY
	6264	EB	XCHG	
	6265	22, 6A, 61	SHLD ADDR2	SAVE(HL)
	6268	2A, 6C, 61	LHLD ADDR3	GET PARTIAL DIVIDENT IN (HL)
	626B	EB	XCHG	
	626C	18	RDLC	ROTATE CARRY IN LSB OF (DE)
	626D	EB	XCHG	
	626E	08	DSUB	
	626F	D2, 80, 62	JNC LOAD	IS CY=1? NO, JUMP TO LOAD
	6272	3F	CMC	COMPLEMENT THE CARRY
	6273	3A, 6E, 61	LDA ADDR4	
	6276	5F	MOV E, A	GET LOWER BYTE OF PARTIAL QUOTIENTINE
	6277	3A, 6F, 61	LDA ADDR4+1	

	627A	57	MOV D, A	GET HIGHER BYTE OF PARTIAL QUOTIENTIN D
	627B	18	RDLC	PUT CARRY IN LSB OF (DE)
	627C	09	DAD B	ADD DIVISOR WITH (HL)
	627D	C3, 8A, 62	JMP SAVE	
LOAD	6280	3F	CMC	COMPLEMENT CARRY
	6281	3A, 6E, 61	LDA ADDR4	GET PARTIAL
	6284	5F	MOV E, A	QUOTIENT IN
	6285	3A, 6F, 61	LDA (ADDR4+1)	(DE)
	6288	57	MOV D, A	
	6289	18	RDLC	PUT CARRY INTO LSB OF (DE)
SAVE	628A	22, 6C, 61	SHLD ADDR3	SAVE (HL) IN ADD R3
	628D	EB	XCHG	
	628E	22, 6E, 61	SHLD ADDR4	SAVE PARTIAL QUOTIENT IN ADDR4
	6291	3A, 70, 61	LDA ADDR5	LOAD ACCUMULATOR WITH BIT COUNT
	6294	3C	INR A	UPDATE BIT COUNT
	6295	32, 70, 61	STA ADDR5	SAVE BIT NO IN ADDR5
	6298	FE, 10	CPI 10H	
	629A	02, 5F, 62	JNZ CONTINUE	ARE ALL BITS OF DIVIDENT TESTED? NO, JUMP TO CONTINUE
	629D	C9	RET	RETURN TO MAIN PROGRAM

MULT SUBROUTINE

	62B0	2A, 6E, 61	LHLD ADDR4	LOAD(HL)WITH MULTIP - LICAND
	62B3	EB	XCHG	GET MULTIPLICAND IN (DE)

	62B4	21, 00, 00	LXI H,0000H	INITIALIZE (HL) WITH 0000H
	62B7	3A, 72, 61	LDA ADDR6	LOAD ACCUMULATOR WITH MULTIPLIER
	62BA	47	MOV B, A	
	62BB	0E, 00	MVI C,00H	INITIALIZE COUNTER C WITH 00H
NEXT	62BD	0C	INR C	
	62BE	78	MOV A, B	
	62BF	1F	RAR	PUT LSB INTO CARRY
	62C0	47	MOV B, A	
	62C1	D2, D0, 62	JNC TEST	IS CY=1? NO, JUMP TO TEST
	62C4	79	MOV A, C	
	62C5	FE, 01	CPI 01H	
	62C7	CA, CC, 62	JZ UPDATE	IS Z=1? YES, JUMP TO UPDATE
	62CA	AF	XRA A	CLEAR CARRY
	62CB	18	RDLC	ROTATE(DE)LEFT BY ONE BIT
UPDATE	62CC	19	DAD D	UPDATE THE PATIAL PRODUCT
	62CD	C3, D8, 62	JMP FINISH	
TEST	62D0	79	MOV A, C	
	62D1	FE, 01	CPI 01H	
	62D3	CA, D8, 62	JZ FINISH	IS Z=1? YES JUMP TO FINISH
	62D6	AF	XRA A	CLEAR CARRY
	62D7	18	RDLC	ROTATE LEFT BY ONE BIT

FINISH	62D8	79	MOV A, C	
	62D9	FE, 07	CPI 07H	
	62DB	C2, BD, 62	JNZ NEXT	IS Z=1? NO, JUMP TO NEXT
	62DE	C9	RET	RETURN TO MAIN PROGRAM

SPEED SUBROUTINE

	62F0	E5	PUSH H	
	62F1	2A, 68, 61	LHLD ADDR1	
	62F4	4D	MOV C, L	
	62F5	44	MOV B, H	
	62F6	2A, 78, 61	LHLD ADDR14	
	62F9	EB	XCHG	
	62FA	1A	LDAX D	
	62FB	6F	MOV_L, A	
	62FC	13	INXD	
	62FD	1A	LDAX D	
	62FE	67	MOV H, A	
	62FF	08	DSUB	
	6300	CA, 27, 63	JZ LOOP1	
	6303	DA, 16, 63	JC MORE	
LESS	6306	13	INX D	
	6307	1A	LDAX D	
	6308	6F	MOV L, A	
	6309	13	INX D	
	630A	1A	LDAX D	
	630B	67	MOV H, A	
	630C	08	DSUB	

```
        630D    CA, 27, 63   JZ LOOP1
        6310    DA, 2F, 63   JC LOOP3
        6313    C3, 06, 63   JMP LESS
MORE    6316    1B           DCX D
        6317    1B           DCX D
        6318    1A           LDAX D
        6319    67           MOV H, A
        631A    1B           DCX D
        631B    1A           LDAX D
        631C    6F           MOV L, A
        631D    08           DSUB
        631E    CA, 58, 63   JZ RPM
        6321    DA, 2B, 63   JC LOOP2
        6324    C3, 32, 63   JMP LOOP4
LOOP1   6327    1B           DCX D
        6328    C3, 58, 63   JMP RPM
LOOP2   632B    13           INX D
        632C    C3, 16, 63   JMP MORE
LOOP3   632F    1B           DCX D
        6330    1B           DCX D
        6331    1B           DCX D
LOOP4   6332    1A           LDAX D
        6333    4F           MOV C, A
        6334    13           INX D
        6335    1A           LDAX D
        6336    47           MOV B, A
        6337    13           INX D
```

```
        6338    1A          LDAX D
        6339    6F          MOV L, A
        633A    13          INX D
        633B    1A          LDAX D
        633C    67          MOV H, A
        633D    09          DAD B
        633E    AF          XRA A
        633F    7C          MOV A, H
        6340    1F          RAR
        6341    67          MOV H, A
        6342    7D          MOV A, L
        6343    1F          RAR
        6344    6F          MOV L, A
        6345    3A, 68, 61  LDA ADDR1
        6348    4F          MOV C, A
        6349    3A, 69, 61  LDA (ADDR1+1)
        634C    47          MOV B, A
        634D    08          DSUB
        634E    DA, 55, 63  JC LOOP5
        6351    1B          DCX D
        6352    C3, 58, 63  JMP RPM
LOOP5   6355    1B          DCX D
        6356    1B          DCX D
        6357    1B          DCX D
RPM     6358    7B          MOV A, E
        6359    32, 78, 61  STA ADDR14
        635C    7A          MOV A, D
        635D    32, 79, 61  STA (ADDR14+1)
```

6360	21, 00, 01	LXI H 0100H
6363	19	DAD D
6364	7E	MOV A, M
6365	32, F4, 27	STA 27F4
6368	23	INX H
6369	7E	MOV A, M
636 A	32, F5, 27	STA 27F5
636D	06, 00	MVI B,00H
636F	CD, E3, 06	CALL MODAD
6372	E1	POP H
6373	C9	RET

FIRING PLUSE COMMAND TABLE

ADDRESS	CONTENT	THYRISTOR PAIR TO BE FIRED	FIRING SEQUENCE
6160	21	(6,1)	1
6161	03	(1,2)	2
6162	06	(2,3)	3
6163	0C	(3,4)	4
6164	18	(4,5)	5
6165	30	(5,6)	6

MEMORY LOCATIONS

Address of command word	=	6166 → ADDR0
60^{o} count value	=	6168 → ADDR1
90^{o} count value	=	616A → ADDR2
Partial divident	=	616C → ADDR3
Quotient	=	616E → ADDR4
ADC output	=	6172 → ADDR6
Firing angle count	=	6174 → ADDR7
Starting address of command table	=	6160 → ADDR8

APPENDIX IV

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00100 C       STEADY STATE PERFORMANCE ANALYSIS OF COMMUTATORLESS
00200 C       DC SERIES MOTOR DRIVE
00300 C       ALFA=INVERTER FIRING ANGLE
00400 C       BETA=INVERTER LEAD ANGLE
00500 C       GAM=DISPLACEMENT ANGLE BETWEEN ESY AND ISY
00600 C       AMU=OVER LAP ANGLE
00700 C       DEL=TURN OF ANGLE
00800 C       REA=ARMATURE REACTION ANGLE
00900 C       PP=NO OF MACHINE POLE
01000 C       VSY=SYNCHRONOUS MOTOR TERMINAL VOLTAGE
01100 C       AISY=MACHINE CURRENT
01200 C       VD=DC LINK VOLTAGE
01300 C       AIDC=DC LINK CURRENT
01400 C       SP=SPEED OF SYNCHRONOUS MOTOR
01500 C       PDC=INPUT POWER TO SYNCHRONOUS MOTOR
01600         DIMENSION DASH(81)
01700         OPEN(UNIT=1,DEVICE='DSK',FILE='SM.OUT')
01800         DATA ALD,ALQ,ALC,RF,RD/0.0684,0.044,0.0122,3.67,0.26/
01900         DATA AKE,PP,AK,Q/1.620,4.0,1.0,0.57/
02000         DATA DASH/81*'-'/
02100         VD=80.0;AIDC=00.0;ALFA=130.
02200         AK2=AKE*AK*PP/120.0
02300         AK1=1.28*AKE*AK
02400         AKD=6.28*(ALD-ALC)/AK1
02500         DO 10 I=1,5
02600         ALFA=ALFA+5.0
02700         BETT=180.0-ALFA
02800         BETA=BETT/57.295
02900 C       COMPUTE DISPLACEMENT ANGLE GAM
03000         GAM=0.0
03100 60      A=GAM
03200         X=COS(BETA)*SQRT(1.0-2.0*AKD*SIN(A)+AKD**2*(SIN
03300         1(A)*SIN(A)+Q**2*COS(A)*COS(A)))
03400         Y=1.0-AKD*(1.0-Q)*SIN(A)
03500         GAM=ACOS((X+3.289*ALC/AK1)/Y)
03600         YY=GAM-A
03700         IF(YY .LE. 0.001) GO TO 70
```

APPENDIX IV

```
03800          GO TO 60
03900 70       AKM=AK1*SQRT(1.0-2.0*AKD*SIN(GAM)+AKD**2*(SIN(GAM)*SIN
04000          1(GAM)+Q**2*COS(GAM)*COS(GAM)))
04100          DO 20 J=1,10
04200          VD=VD+10.0
04300          WRITE(1,40) VD,ALFA
04400 40       FORMAT(15X,'DC LINK VOLTAGE=',F7.2,10X,'FIRING ANGLE
04500          1 =',F7.2/3X,'DCLINK',3X,'MACHINE',2X,'MACHINE',2X,
04600          1'POWER',3X,'COMMU',2X,'TURN',3X,'REACT',2X,'POWER',2X,
04700          1'M/C',8X,'M/C'/3X,'CURRENT',2X,'VOLTAGE',2X,'CURRENT
04800          1',2X,'FACTOR',2X,'ANGLE',2X,'ANGLE',2X,'ANGLE',2X,
04900          1'INPUT',2X,'SPEED',6X,'TORQUE')
05000          DO 30 K=1,16
05100 C        COMPUTE SYNCHRONOUS MACHINE CHARACTERISTICS
05200          AIDC=AIDC+0.5
05300          AISY=0.7796*AIDC
05400          RDC=RD+RF
05500          AKN=0.0151*PP*AKM
05600          SP=(VD-AIDC*RDC)/(AKN*AIDC*COS(BETA))
05700          IF(SP .GT. 1800.) GO TO 30
05800          VSY=6.497E-03*AKM*AIDC*PP*SP
05900          IF(VSY .GT. 250.) GO TO 30
06000          AKC=AK1/AKM
06100          PF=AKC*(1.0-AKD*(1.0-Q)*SIN(GAM))*COS(GAM)
06200          XX=(1.0-AKD*(1.0-Q)*SIN(GAM))*COS(GAM)
06300          DEL=ACOS(AKC*(XX+3.289*ALC/AK1))
06400          AMU=BETA-DEL
06500          BET=ACOS(PF)
06600          REA=GAM-BET
06700          VDC=VD-AIDC*RDC
06800          PDC=VDC*AIDC
06900          AKT=0.1451*PP*AKM*PF
07000          TOR=AKT*AIDC**2
07100          ADEL=DEL*57.295
07200          AAMU=AMU*57.295
07300          AREA=REA*57.295
07400          APDC=PDC/1000.0
```

APPENDIX IV

```
07500          WRITE(1,50) AIDC ,VSY,AISY,PF,AAMU,ADEL,
07600          1AREA,APDC,SP,TOR
07700 50       FORMAT(5X,F5.2,3X,F6.2,4X,F5.2,3X,F5.3,2X,F5.2,
07800          12X,F5.2,2X,F5.2,2X,F5.3,2X,F7.2,3X,F7.2)
07900 30       CONTINUE
08000          AIDC=0.0
08100          WRITE(1,80) DASH
08200 80       FORMAT(3X,81A1)
08300 20       CONTINUE
08400          VD=80.0
08500 10       CONTINUE
08600          STOP
08700          END
08800
```

COMPUTATION OF SUPPLEMENTARY DISPLACEMENT ANGLE r

The relationship between firing angle and supplementary displacement angle **r is described by**

$$\text{Cos}\beta = \frac{[1-K_d(1-q)\text{Sin}r]\,\text{Cos}r - \frac{\pi^2 L_c}{3K_1}}{K_m/K_1} \qquad (1)$$

$$\text{or Cos}\beta = \frac{K_1[1-K_d(1-q)\text{Sin}r]\,\text{Cos}r - 3.289L_c}{K_m} \qquad (2)$$

where $K_m = K_1[1-2K_d\text{Sin}r + K_d^2(\text{Sin}^2r+q^2\text{Cos}^2r)]^{\frac{1}{2}}$

Equation **(2)** can be rewritten as

$$K_1[1-2K_d\text{Sin}r+K_d^2(\text{Sin}^2r+q^2\text{Cos}^2r)]^{\frac{1}{2}}\,\text{Cos}\beta =$$

$$K_1\{[1-K_d(1-q)\text{Sin}r]\,\text{Cos}r - \frac{3.289L_c}{K_1}\}$$

Therefore $[1-K_d(1-q)\text{Sin}r]\text{Cos}r = [1-2K_d\text{Sin}r+K_d^2(\text{Sin}^2r$

$$+ q^2(\text{Sin}^2r+q^2\text{Cos}^2r)]^{\frac{1}{2}}\,\text{Cos}\beta + \frac{3.289L_c}{K_1}$$

$$\text{Hence Cos}r = \frac{\text{Cos}\beta[1-2K_d\text{Sin}r+K_d^2(\text{Sin}^2r+q^2\text{Cos}^2r)]^{\frac{1}{2}} + \frac{3.289L_c}{K_1}}{1-K_d(1-q)\,\text{Sin}\,r} \qquad (3)$$

Using notations

$$X = \text{Cos}\beta[1-2K_d\text{Sin}r+K_d^2(\text{Sin}^2r+q^2\text{Cos}^2r)]^{\frac{1}{2}} \qquad (4)$$

and $Y = 1 - K_d(1-q)\,\text{Sin}r \qquad (5)$

We obtain the following equation

$$\text{Cos}r = \frac{X + \frac{3.289L_c}{K_1}}{Y}$$

$$\text{or } r = \text{Cos}^{-1}\left[\frac{X + 3.289L_c/K_1}{Y}\right] \qquad (6)$$

Now for a particular value of firing angle, displacement angle r is found by trial and error method using equations (4), (5) and (6).

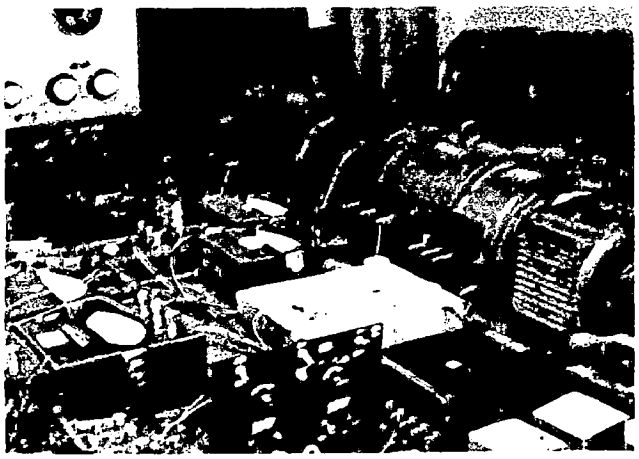
APPENDIX V

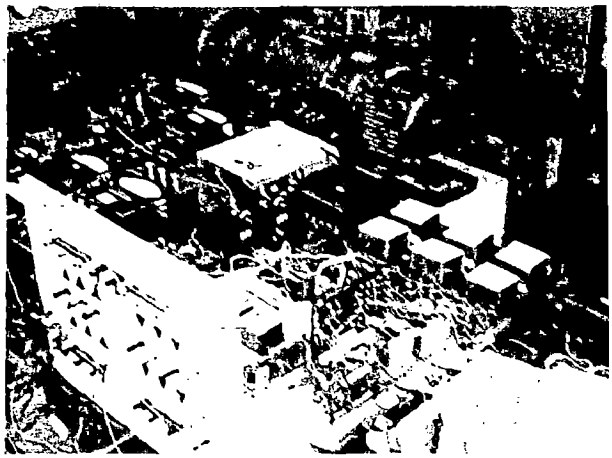
```
00100 C       TO PREPARE A LOOK UP TABLE FOR SYNCHRONOUS MOTOR SPEED
00200 C       MEASUREMENT DONE BY T.K.CHAKRABORTY
00300 C       SP=SPEED OF THE SYNCHRONOUS MOTOR
00400 C       DECM(60)=NO OF CLOCK CYCLE IN 60 DEGREE OF POWER CYCLE
00500 C       HEX(60)=HEXA EQUIVALENT TO DECM(60)
00600 C       SPEED(DECM)=SPEED IN DECIMAL
00700 C       SPEED(HEX)=SPEED IN HEXADECIMAL
00800         DIMENSION H(16),A(4),B(4),DASH(61)
00900         DATA(H(II),II=1,8)/'0','1','2','3','4','5','6','7'/
01000         DATA (H(JJ),JJ=9,16)/'8','9','A','B','C','D','E','F'/
01100         DATA DASH/61*'-'/
01200         OPEN(UNIT=1,DEVICE='DSK',FILE='TAP.OUT')
01300         F=1.5
01400         WRITE(1,10)
01500 10      FORMAT(3X,'FREQUENCY',5X,'DECM(60)',6X,'HEX(60)',6X,
01600        1'SPEED(DEC)',6X,'SPEED(HEX)'/)
01700 20      I=1
01800         J=1
01900         F=F+0.5
02000         SP=30.0*F
02100         T60=1.0/(F*6.0)
02200         DECM=T60*511.67E+03
02300 C       FIND HEXA EQUIVALENT TO DECM NUMBER
02400         N1=IFIX(DECM)
02500         P1=FLOAT(N1)
02600 30      X1=P1/16.0
02700         M1=IFIX(X1)
02800         Y1=FLOAT(M1)
02900         Q1=X1-Y1
03000         X=Q1*16.0
03100         N=IFIX(X)
03200         N=N+1
03300         A(I)=H(N)
03400         IF(I.EQ.4) GO TO 40
03500         I=I+1
03600         P1=Y1
03700         GO TO 30
```

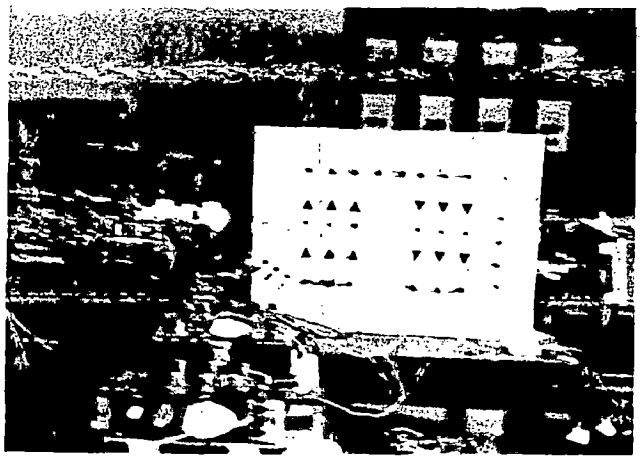
APPENDIX V

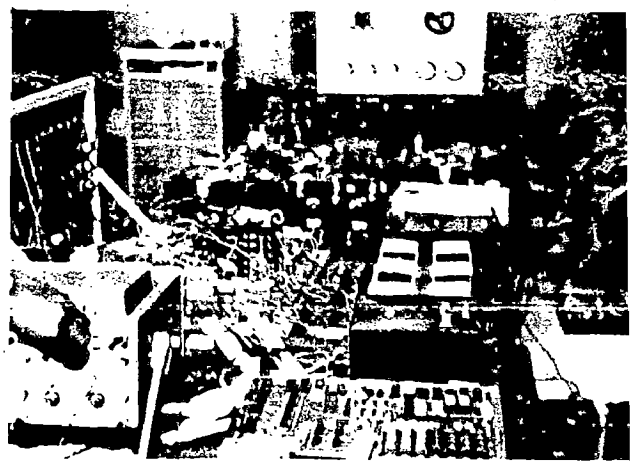
```
03800 C       FIND HEXA EQUIVALENT TO SPEED OF SYNCHRONOUS MOTOR
03900 40      N2=IFIX(SP)
04000 50      X2=SP/16.0
04100         M2=IFIX(X2)
04200         Y2=FLOAT(M2)
04300         Q2=X2-Y2
04400         Y=Q2*16.0
04500         M=IFIX(Y)
04600         M=M+1
04700         B(J)=H(M)
04800         IF(J.EQ.4) GO TO 60
04900         J=J+1
05000         SP=Y2
05100         GO TO 50
05200 60      WRITE(1,70) F,N1,A(4),A(3),A(2),A(1),N2,B(4),B(3),B(2),
05300         1B(1)
05400 70      FORMAT(5X,F5.2,9X,I6,8X,4A1,10X,I5,10X,4A1)
05500         WRITE(1,80) DASH
05600 80      FORMAT(6X,61A1)
05700         IF(F.EQ.60.0) GO TO 90
05800         GO TO 20
05900 90      STOP
06000         END
```

APPENDIX - VI









Photographs of the experimental set up