# 2 BITS/STEP SAR ADC WITH SELF-COMPENSATING COMPARATOR

**A DISSERTATION**

*Submitted in partial fulfillment of the requirements for the award of the degree of*

**MASTER OF TECHNOLOGY**

**in**

**ELECTRONICS AND COMMUNICATION ENGINEERING**

**(With Specialization in Semiconductor devices & VLSI Technology)**

**By**

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JUNE, 2011

# CANDIDATE'S DECLARATION

I hereby declare that the work presented in this dissertation report entitled, **"2bits/step SAR ADC with self-compensating Comparator"** towards the partial fulfillment of the requirements for the award of **Master of Technology in Electronics and Communication Engineering** with specialization in **Semiconductor Devices and VLSI Technology (SDVT),** submitted in the Department of Electronics and Computer Engineering, Indian Institute of Technology Roorkee, is an authentic record of my own work carried out during the period from July 2010 to May 2011, under the guidance of **Dr. Sudeb Dasgupta, Department of Electronics and Computer Engineering, Indian Institute of Technology Roorkee.**

The content of this dissertation has not been previously submitted for examination as part of any academic qualifications.

Date : 26/06/2011

Place : Roorkee

Ravinder Jakkidi

## CERTIFICATE

This is to certify that the statement made by the candidate is correct to best of my knowledge and belief.

**Dr. Sudeb Dasgupta**

Assistant Professor

# Acknowledgments

First of all I would like to thank Dr. Sudeb Dasgupta, Assistant professor, Department of Electronics and Computer Engineering at Indian Institute of Technology Roorkee, for supervising my thesis.

I owe my deepest gratitude to Sandeep Miryala and Kumar NVSS for their guidance and help; especially I'm deeply indebted to Kumar NVSS for his moral support during my odd times at IIT Roorkee.

I would like to extend my gratitude to these 'edaboard' members, Lamoun, Braski, Bharat and Erikl, without whom it would have next to impossible to write my thesis. I appreciate their time and patience in guiding me throughout the project. Every time I used to learn something new from the discussions they have made with me.

It's a pleasure to thank Sandeep Vundavalli and Durga Prasad for their help during my project and for making my days at IIT Roorkee most joyful.

Last but not the least I'm always grateful to my family members especially my sisters, Naveena and Neeraja, for their financial and moral support. And also I would like to extend my thanks to all those people who directly or indirectly helped me.

Ravinder Jakkidi.

# Abstract

Now-a-days High speed, Low resolution ADCs are of utmost concern because of continues growth in demand of UWB appliances. As process scales down many traditional ADC architectures, mostly relying on analog feedback will not perform well in scaled process, necessitating a change in ADC architecture. ADC architecture used in current work is hybrid version of Flash ADC and SAR ADC which has an inherent advantage of reduced normalized conversion (conversion energy/No. bits) energy.

This hybrid structure is expected to replace Flash ADC in the upcoming years. Another advantage of present architecture is that the output code conversion block is outside the SAR loop enhancing the speed of ADC.

SAR loop delay is reduced, thereby increasing the speed, by optimizing each block that comes along the critical path. Various optimization techniques of each block have been studied and well suited method has been used in their implementation.

Next a self-compensating comparator has been proposed. The proposed comparator uses a Novel method of 'back-gate biasing' technique to reduce the offset of the comparator. Then the proposed comparator has been deployed in SAR ADC and evaluated its dynamic performance.

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# Chapter 1
# Introduction

## 1.1 Motivations

Single chip integration is of main concern these days in consumer electronic products as integration reduces cost. Nanoscale digital circuits benefit from continuous scaling in terms of speed, silicon area and power efficiency. Analog-to-digital converter (ADC) circuits also benefit a lot from scaling, due to the reduced parasitic capacitances and increased element matching for same physical dimension.

On the other side, the intrinsic gain ($g_m/g_{ds}$), as well as the linearity of transistors has degraded (Fig. 1.1(a) [1]).

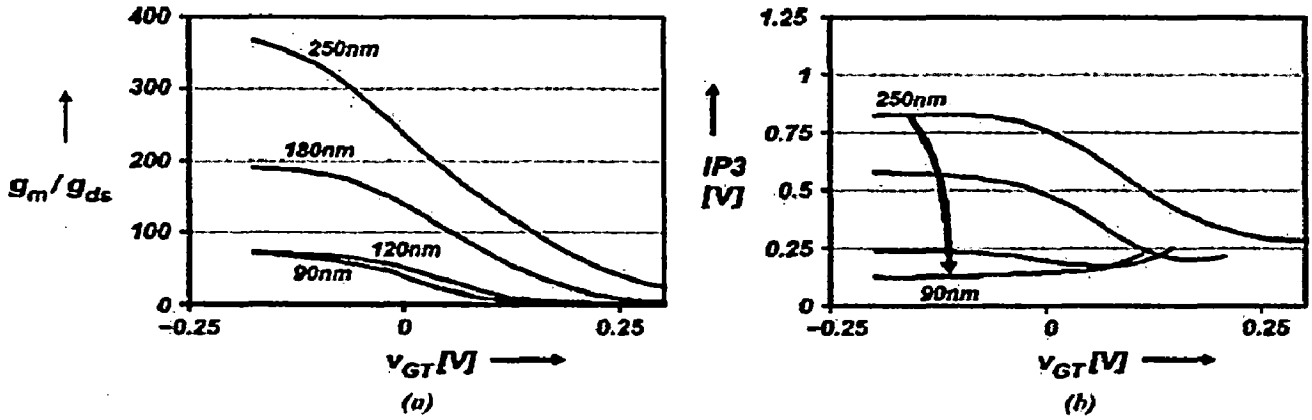


**Fig. 1.1** Intrinsic gain **(a)** and output-referred third order inter-modulation intercept point (IP3) **(b)** vs. gate-overdrive voltage for various CMOS technology nodes with L = 1μm

The speed of scaled-down MOS transistors depends on thin gate oxide, which however limits the maximum safe voltage that can be applied on the gate of the transistor. The reduced power supply voltage makes it difficult to use traditional analog structures such as cascode to increase amplifier gain with little impact on stability. Hence we are forced to cascade multiple stages of amplifiers to obtain adequate open-loop gain. However, cascading introduces more poles or more signal delay, demanding complicated compensation schemes to make the amplifier

stable in feedback. These frequency compensation schemes often require large compensation capacitors hence chip area, increase power consumption, and compromise circuit speed.

For the above reasons, many traditional analog circuits which rely on analog feedback to achieve accuracy no longer perform as well in scaled processes, facilitating change of ADC architectures toward those that are more acquiescent to nanoscale CMOS. ADC architectures such as 'two-step sub-ranging' and 'successive approximation (SA)' are being given more attention in recent years. These architectures do not rely on accuracy of feedback based analog signal processing to achieve accuracy of A/D conversion.

As process scales down, the problems faced by medium and high resolution ADCs are power consumption and area. Since conversion error due to element mismatch can be mitigated by various circuit techniques, signal-to-noise ratio (SNR) in high resolution ADCs are usually limited by thermal noise. If signal swing reduces by half due to supply voltage scaling, signal power reduces by four times. Hence four times as large capacitance is needed to reduce kT/C noise by the same amount to keep the same SNR. This requires four times large opamps transconductance to keep the same operation speed which means the bias current of the opamp and in turn its size must be increased four times. While the rest of the chip scales down, capacitors, whose size is limited by the kT/C noise requirement cannot be reduced.

Telecommunication standards have been moving from narrow band to wide band, from lower to higher carrier frequencies. While bandwidth allocated for AM used to be only 10 kHz for each channel with a carrier frequency of several hundred kHz, UWB receivers would use more than 500 MHz per each channel with a carrier frequency of 2~3GHz, and 60 GHz in the near future. As bandwidth widens more thermal noise fall in-band and since transmission power is limited, inevitably the SNR reduces

High resolution ADCs are needed in conventional narrowband wireless standards to move more baseband filtering functions from analog to digital domain, and it is predicted that the demand for high-speed, low-resolution ADCs will increase in the future. The flash architecture has been enormously used for these ADCs. However, due to the requirement of many parallel comparators and preceding pre-amplifiers to reduce offset and load capacitance at output of

DAC, the lowest reported power consumption for 6-bit GS s flash ADC that does not require on chip calibration is about 160 mW [2].

My work includes a new type of ADC that takes advantage of the high speed digital logic and highly matched small capacitors in standard nanoscale digital CMOS processes to achieve 500MSPS, 6-bit performance with much lower power consumptions and smaller die area than flash ADCs.

## 1.2 A Review of Existing ADC Architectures

### 1.2.1 Flash

The simplest of ADC architectures is the flash ADC. For N bit resolution $2^N$ comparators positioned in parallel and weigh against the input voltage with reference voltages generated by a resistor ladder (Fig. 1.2[3]).

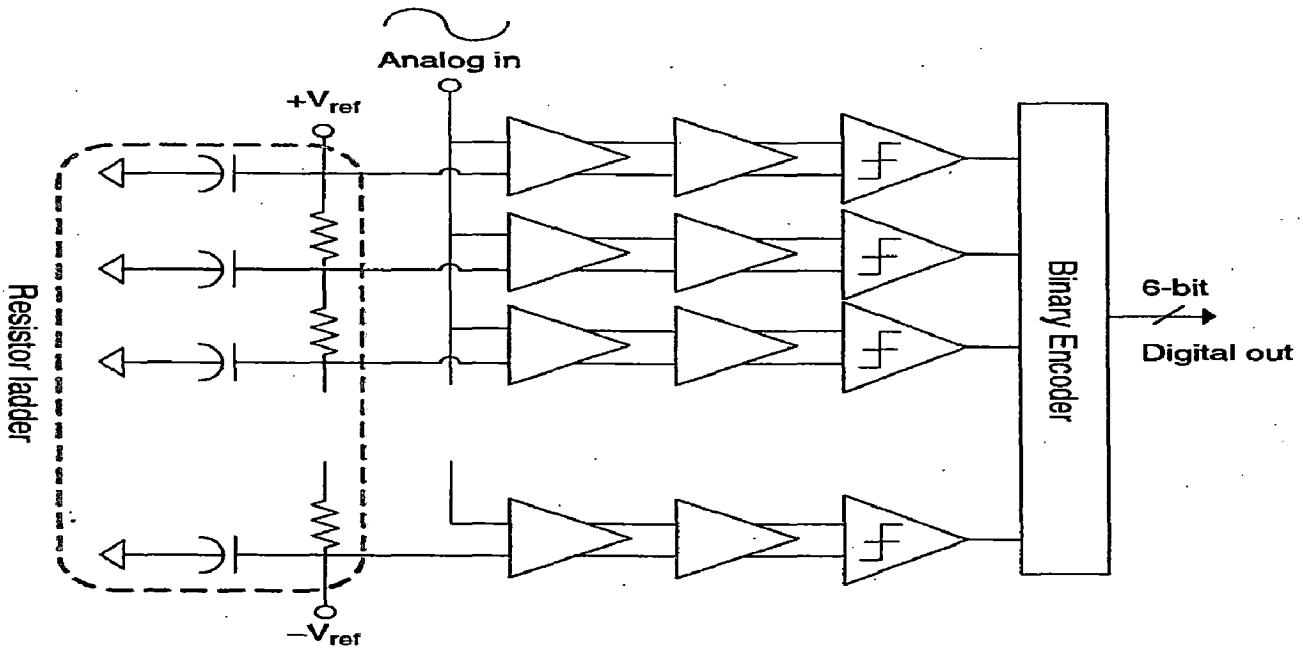


**Fig. 1.2** Basic structure of a flash ADC

Two major drawbacks of flash ADC is its large silicon area and input capacitance, the latter also limits the maximum signal bandwidth it can operate. To increase number of bits(N) by 1, not only must the number of comparators be doubled, but also the size of each comparator

must be quadrupled(as offset due to $V_{th}$ mismatch is inversely proportional to root of gate area) in order to reduce its input referred offset voltage by half to retain the same DNL/INL. Techniques such as pre-amplification, offset averaging and interpolation greatly help reducing both silicon area and input capacitance, but they are still much larger when compared with other architectures. However, the flash architecture has been exclusively used for high-speed ADCs with conversion rate above 500 MHz.

### 1.2.2 Pipeline

Pipeline is the most widely used architecture for high performance Nyquist-rate ADCs. Instead of digitizing all the bits at once, in the first stage, the most significant bits are digitized with a small flash ADC, then a feedback DAC is used to subtract in analog domain, producing the residue voltage, which is amplified and digitized by subsequent stages while the first stage handles the next sample (Fig. 1.3[3]). If each stage digitizes 1 bit, only N comparators are required rather than $2^N$ comparators (in reality redundancy is provided and each stage digitize 1.5 bit or more, leading to at least 2N comparators.) Because of the pipelining, the sampling frequency can also be high.

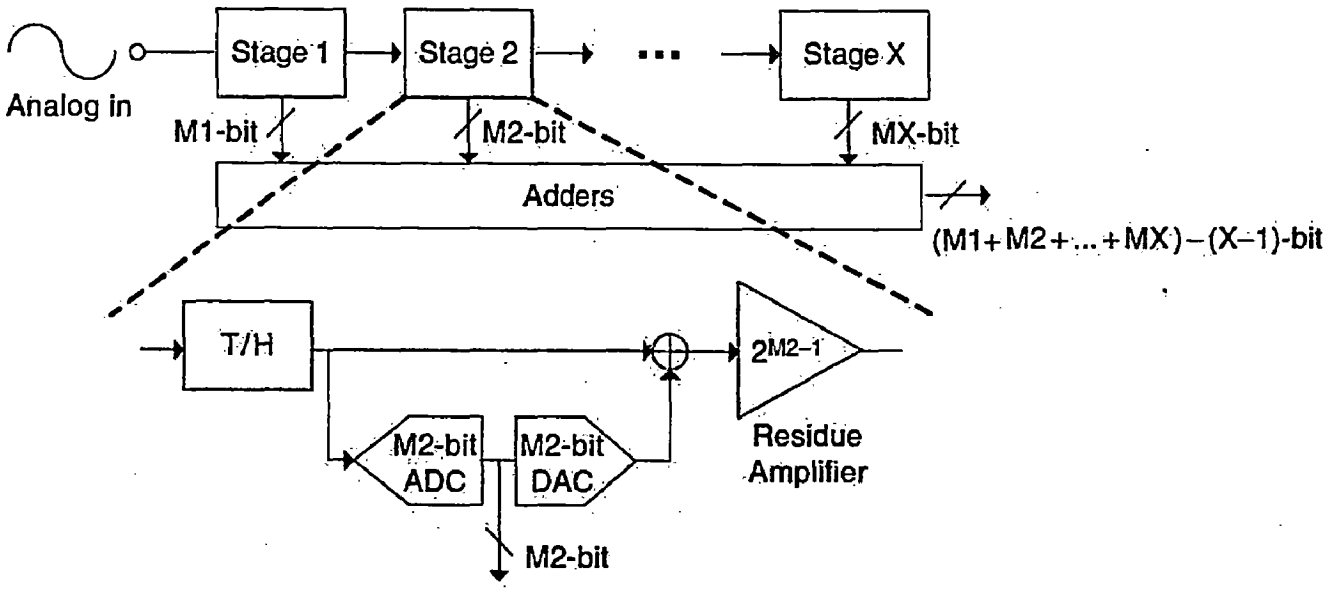


**Fig. 1.3** Block diagram of a typical X-bit pipelined ADC

The linearity of pipelined ADC relies on precise amplification of residue therefore high gain OTA is necessary. The accuracy requirement on the OTA can be relaxed by digitizing more

bits in the first stage, but the area of the flash ADC and the DAC increases. Also, the OTA must provide larger closed loop gain (which is inversely proportional to resolution), therefore its bandwidth reduces. Various digital calibration methods that correct errors or non-linearity due to inadequate closed loop gain of OTA have been actively researched in recent years and good results are reported. By using these techniques the OTA closed loop gain requirements can be relaxed, and even open loop residue amplification becomes possible.

Major factor limiting the use of pipelined ADC is its intricacy and power consumption since either accurate residue amplification or complicated digital calibration is necessary. However, it is the most common Nyquist ADC architecture for resolution less than 0.4% of $V_{FS}$ [4].

### 1.2.3 Sub-ranging

Sub-ranging is an architecture that was developed to reduce the number of comparators compared with flash ADC (Fig. 1.4[3]). A coarse flash ADC first determines a "rough" estimation of the input voltage and then a "fine" ADC (usually of Flash architecture) digitizes the input voltage using reference voltages that are chosen to enclose the rough range.

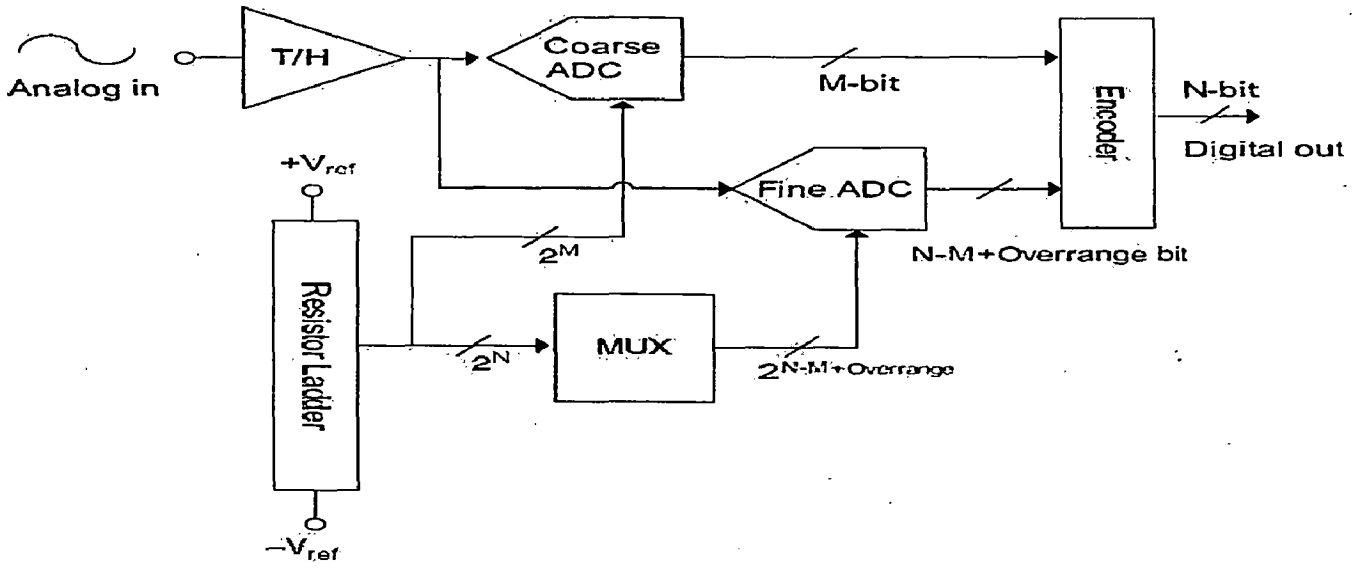


**Fig. 1.4** Basic structure of a two-step sub-ranging ADC

Although the "fine" ADC needs to have resolution same as that of whole ADC, it only needs to digitize the chosen range, therefore the number of comparators is greatly reduced (e.g.

flash ADC would require 256 comparators, but around 32 comparators are required for the fine ADC).

Unlike pipelined ADC, there is no residue signal amplification involved. Analog Amplification by the pre-amplifier before the comparators of the fine ADC need not be linear and accurate, since only sign of the comparison matters. Therefore pre-amplifiers, operated in open loop, of low-gain amplifiers can be cascaded to get reasonable gain and therefore can completely eliminate the use of feedback to stabilise. This property made sub-ranging increasingly popular these days.

Since a large number of pre-amplifiers are required for the fine ADC when the resolution exceeds 8-bit, large die area is still a problem as in case of flash ADC. A 12-bit sub-ranging ADC in 90 nm CMOS reported in [5] has an active area of 4.7 $mm^2$.When the area of digital portion of the chip shrink to half for every technology node, this kind of area becomes prohibitive in terms of cost.

### 1.2.4 Successive Approximation

Successive approximation (SA) is one of the earliest ADC architecture. Fig. 1.5[3] shows the basic structure of a conventional N-bit SA ADC. First the input voltage ($V_{in}$) is sampled on all capacitors. Then the bottom plate of the first capacitor ($2^{N-1}Cu$) is connected to $+V_{ref}$ whiles the rest to $-V_{ref}$, and the top plate switch turns off. The comparator determines sign of the voltage on the top plate, if positive (negative), then the MSB of $V_{in}$ is determined to be zero(one), and in the next clock cycle, the first capacitor is connected to $-V_{ref}$ ($V_{ref}$ ) and the same process continues until all the bits are determined. In the end the digital output will switch each capacitor in such a way that the voltage input of comparator will be very close (close by less than 1LSB) to zero.

The SAR ADC is a very hardware efficient architecture. Although N clock cycles are required to convert N-bit, only one comparator is needed and the rest is digital logic and capacitors, without any linear amplifier. The conversion process can be seen as "digital feedback" as opposed to analog feedback to achieve desired accuracy. All the problems

associated with analog feedback, such as phase margin, gain margin and linearity do not exist in "digital feedback", since we have complete control over the process to avoid any oscillation.

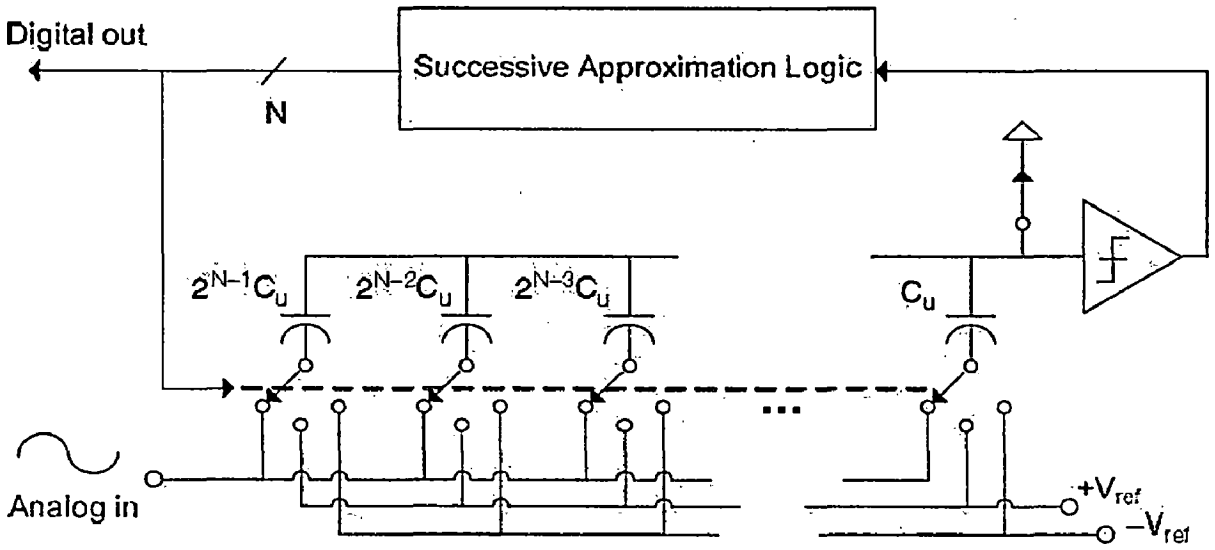


**Fig. 1.5** Basic structure of a conventional *N*-bit successive approximation ADC

The settling of the passive switch-capacitor network can be made much faster than that in OTA-based switched-capacitor circuits [3], which are used to implement residue amplifiers in CMOS pipelined ADCs and analog loop filters in ΔΣ ADCs. Figure 1.6 compares the settling time constant τ for the two cases.

Except for the sampling switches, all switches are connected to reference voltages that are close to the supply rails. Therefore the gate overdrive voltages of these switches are very large ($V_{dd} - V_{th}$ is around 1.0 V if low-$V_{th}$ transistors are used) making their $f_T$ very close to the maximum value (close to 60 GHz in 90nm CMOS) available for the process. On the other hand, due to signal swing constraints, the speed of settling that involves operational amplifiers is much slower because the gate overdrive of the op-amp input devices must be set to 0.1 ~ 0.2 V.

Other than settling another delay that limits the speed of "digital feedback" is the SA logic delay. However, in 90nm CMOS a FO4 inverter delay is close to 20ps and will further improve in finer technologies. One problem with successive approximation is the large size of the capacitor network when the number of bit is large, because the ratio between the largest

capacitor and the smallest one becomes so huge. C-2C ladder can be used to reduce the ratio, but it introduces errors due to the parasitic capacitances errors due to the parasitic capacitances.

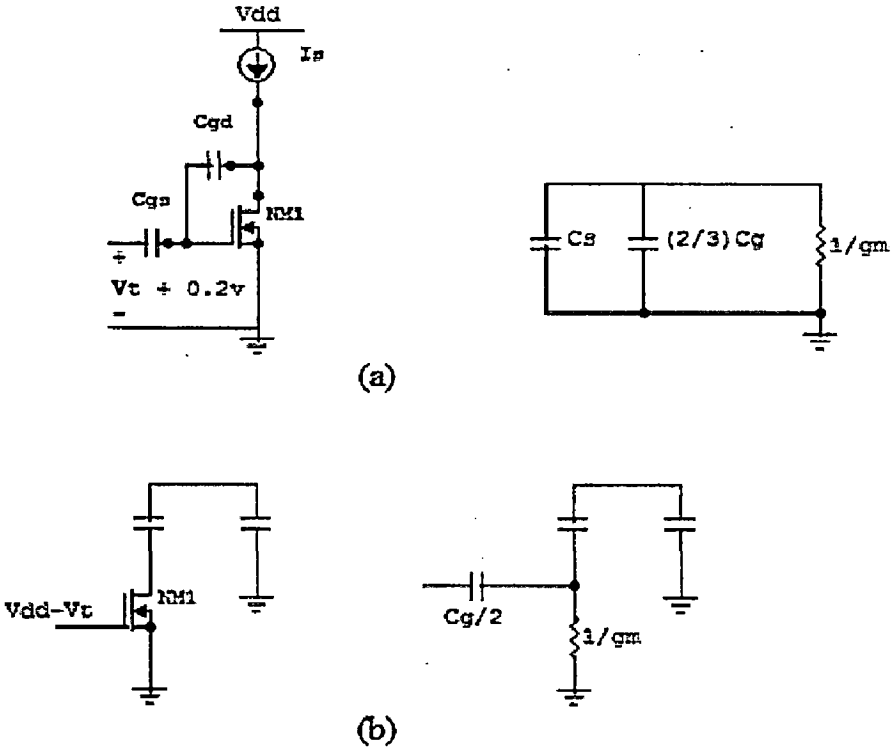


**Fig. 1.6** Settling time-constant comparison between **(a)** conventional OTA-based switched-capacitor circuits and **(b)** passive switched-capacitor network [3]

SA ADCs that do not use pre-amplifiers expose the offset of the comparator as the offset of the ADC (can be eliminated using initial adjustments) which is not a problem unless time-interleaving is used. But if time-interleaving is used to increase the sampling frequency as in pre-amplifiers must be used to reduce the offset mismatch among channels in which case mismatch between offsets of comparators in parallel channels results in INL/DNL and can't be eliminated.

### 1.2.5 ΔΣ ADCs

For medium and high resolution, low speed applications, ΔΣ ADC (Fig. 1.7[3]) is probably the best solution. More than 14-bit resolution can be easily achieved in nanometer CMOS processes whereas complicated digital calibration techniques must be used for other ADC

architectures such as pipeline. The over-sampling nature of ΔΣ ADCs reduces anti-aliasing filter requirement and capacitors sizes.

Compared with other ADCs, ΔΣ ADCs rather require gigantic digital decimation filter with many taps to filter out the shaped quantization noise. This causes more signal delay than other architectures which is unacceptable for some applications.

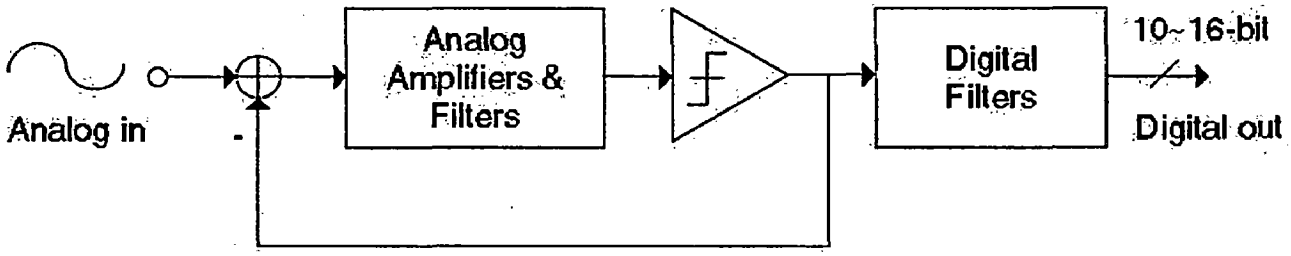


**Fig. 1.7** Block diagram of a single-bit ΔΣ ADC

ΔΣ ADCs and SA ADCs are similar in principle because they both use "digital feedback", but the difference is that more analog signal processing is involved in the loop filter for ΔΣ ADCs. When multi-bit feedback and single-loop feed-forward architecture are used, the signal swing inside the loop filter can be reduced and the loop filter linearity requirement becomes much more relaxed. Therefore, nanoscale CMOS transistors with poor open loop gain can be used to obtain high linearity and SNR without any digital calibration. In fact, recent years have seen a steady trend of ΔΣ ADC design moving from single-bit feedback architecture to multi-bit ones, and from high order analog loop filters to lower order, simpler ones such as [6]. The SA ADC can be seen as an ultimate form of this trend, where the digital feedback covers the entire ADC resolution and the analog loop filter disappears completely.

# Chapter 2
# 2bits/step SAR ADC

## 2.1 Architecture

In chapter1 advantages of SAR ADC was explained. The energy per conversion of SAR ADCs is approximately varies linearly with the resolution while that of flash ADC it is exponentially dependence [7]. This entails that SAR is more energy efficient than flash only when the number of bits (5 from Fig. 2.1) is larger than a certain threshold, below which flash becomes more efficient. When the clock frequency is close to the maximum attainable in that process the energy per conversion increases dramatically and speed can be traded for large power savings.

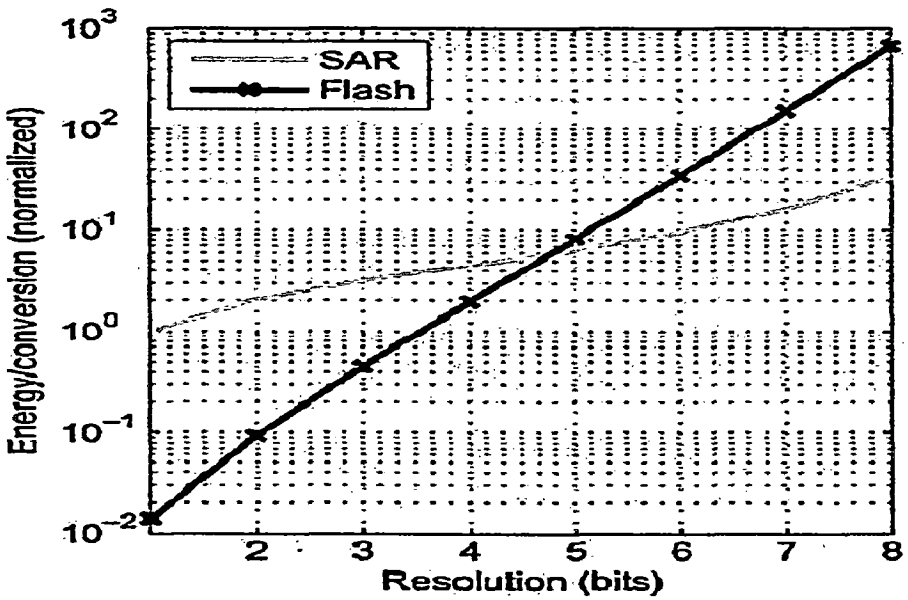


**Fig. 2.1** Modeled SAR and flash ADC energies vs. resolution (Copy of Fig. 4a in [7])

When these factors are considered, for small number of bits it may be less efficient to use SAR with a very high internal clock frequency than to use flash.

If we view one SAR conversion process as a cascade of multiple SAR conversion processes with a smaller number of bits, we can see the possibility of increasing sampling

frequency and/or power efficiency by replacing each sub-conversion process with the flash architecture.

Fig. 2.2 illustrates an example conversion process [3] of the architecture that combines SAR and flash. Suppose analog input "39" was sampled on all capacitors. The next phase 3 reference levels for the flash are generated by (001), (011) and (111) inputs to the capacitors sized "16" (and (110), (100), (000) on the negative side).

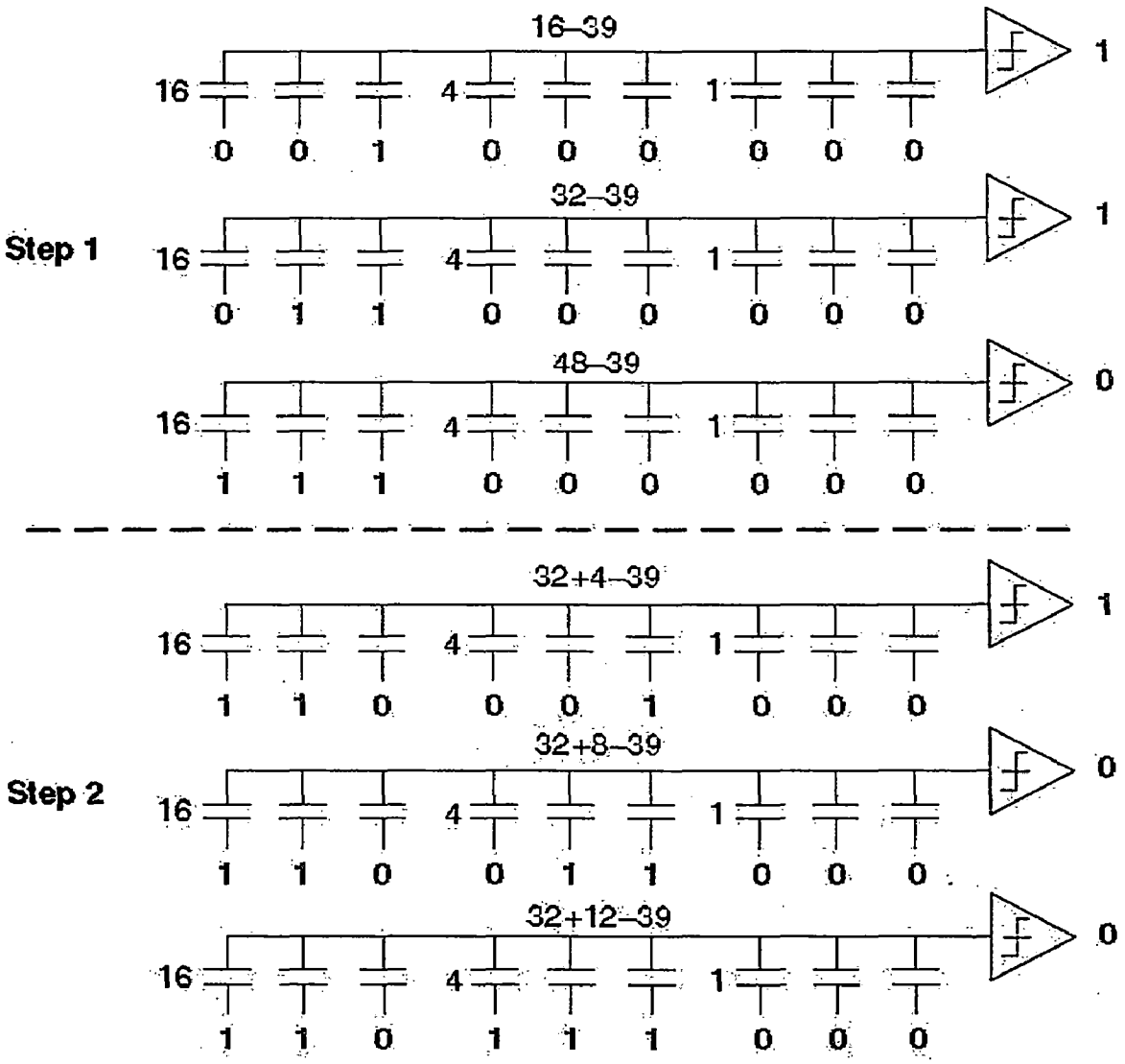


**Fig. 2.2** An example conversion of analog input "39" by combined flash and SAR

All the other capacitors are connected to 0 (and 1 on the negative side). As a result, the top 2 bits are converted by the 3 comparators. In the 2nd conversion step, the previous

comparator outputs are connected to each "16" capacitor, and the 3 reference levels are generated by the "4" capacitors, converting the middle 2 bits.

It continues and finally the 6-bit ADC output is obtained by simply using 3 full adders to convert each step's 3 comparators' outputs to 2-bit wide binary format, which is a much simpler process than in a traditional 6-bit flash ADC where 65 comparators' outputs need to be converted into binary format.

Implemented in gpdk_90 CMOS, each SAR ADC is clocked at 500MHz, and two bits are determined per each cycle. Three clock cycles are required to convert 6 bits.

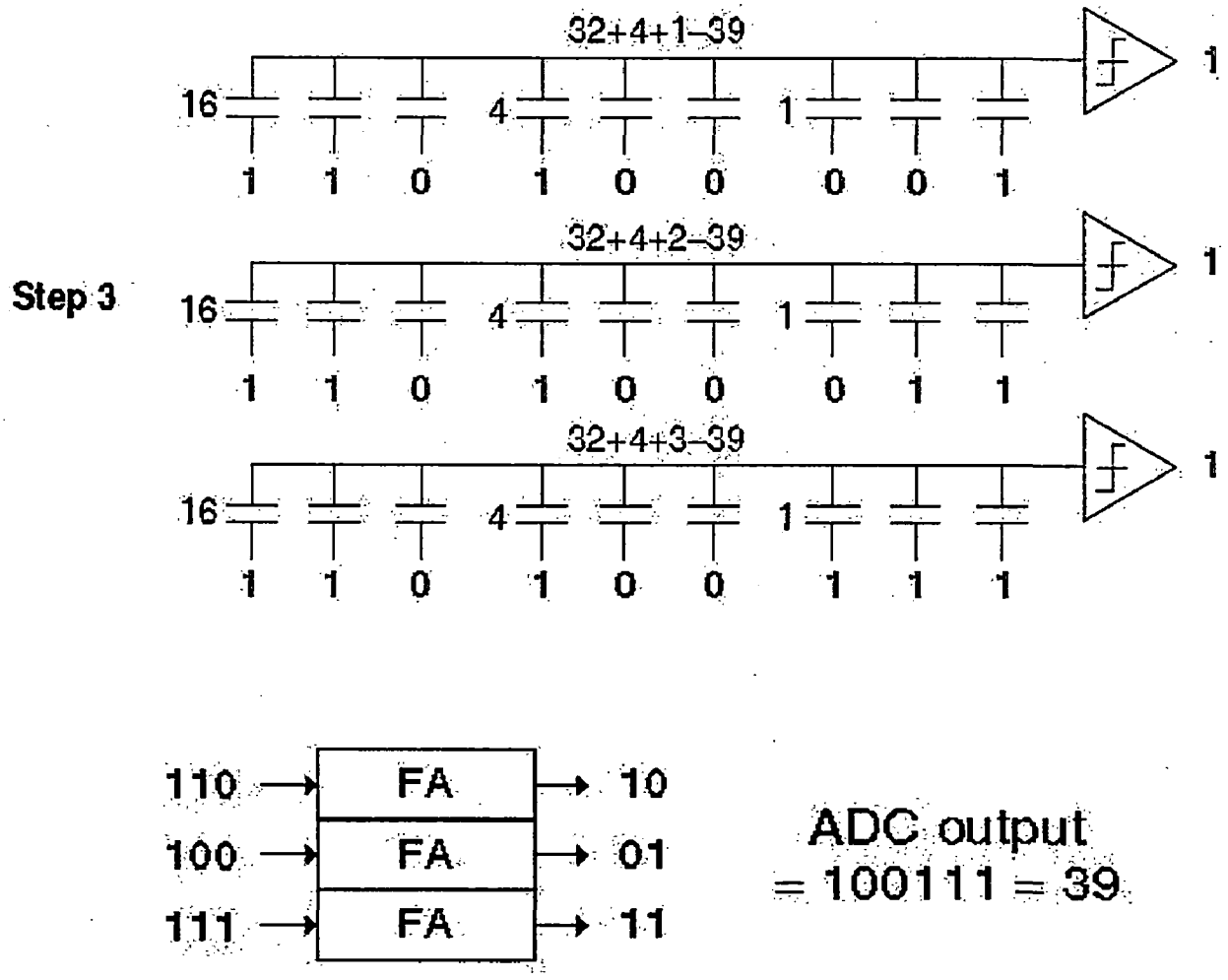


**Fig. 2.2** An example conversion of analog input "39" by combined flash and SAR (contd...)

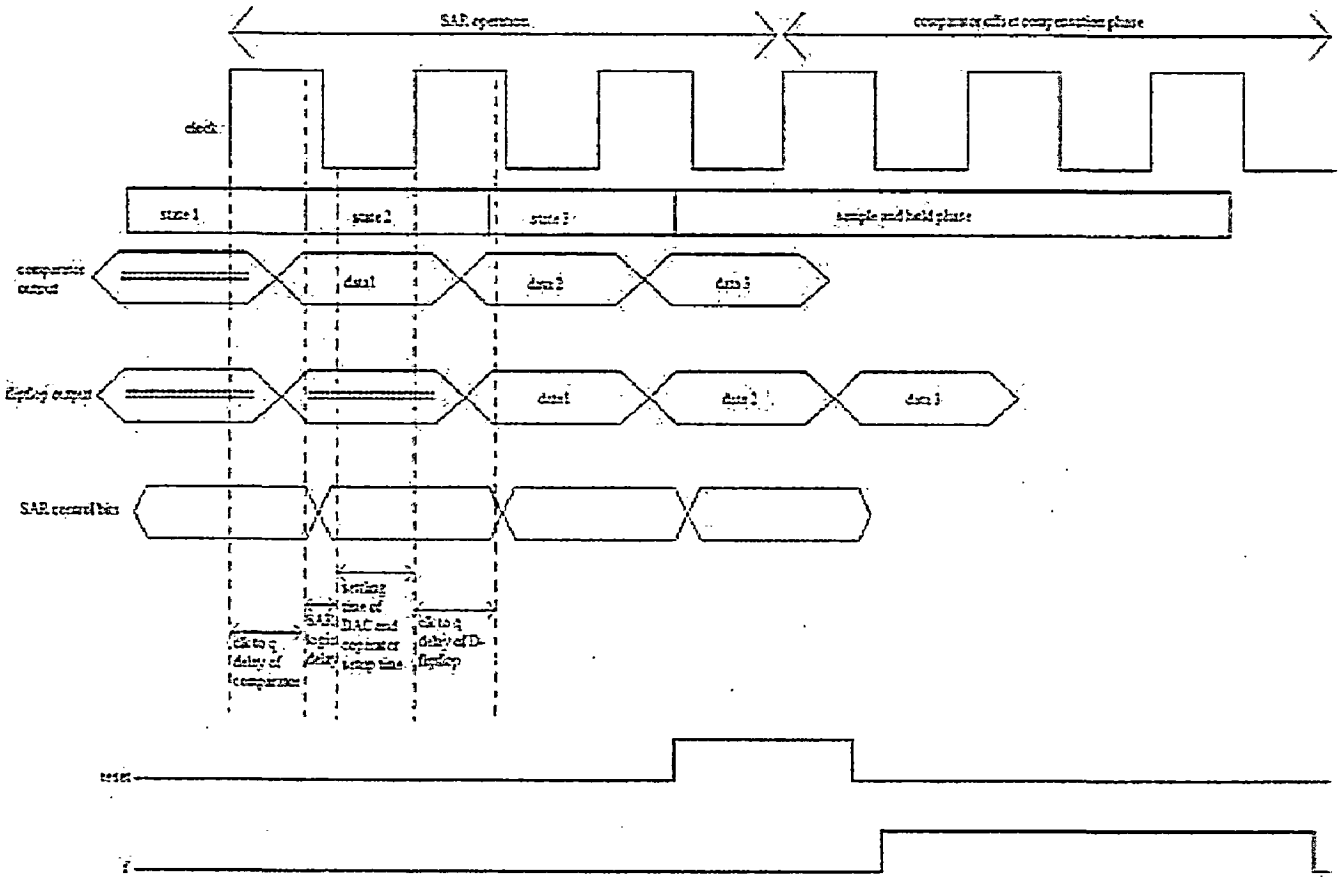

**Fig. 2.3** Timing diagram of SAR operation

## 2.2 Charge Redistribution DAC

An effective circuit implementation of the successive approximation algorithm is the so called charge redistribution scheme. The name of the method comes from the fact that the charge sampled at the beginning of the conversion cycle is properly redistributed on the sampling array to obtain a top plate voltage close to zero at the end of the conversion cycle.

It consists of a Comparator and a binary bank of capacitors. In this example a 5-bit capacitor bank is selected for a 5-bit AD Conversion. It uses 3 phases, i.e. the sample mode, the hold mode and the bit cycling phase.

In the sample mode, all bottom plates of the capacitors are connected to the input voltage $V_{in}$. All capacitors thus sample the input voltage $V_{in}$.

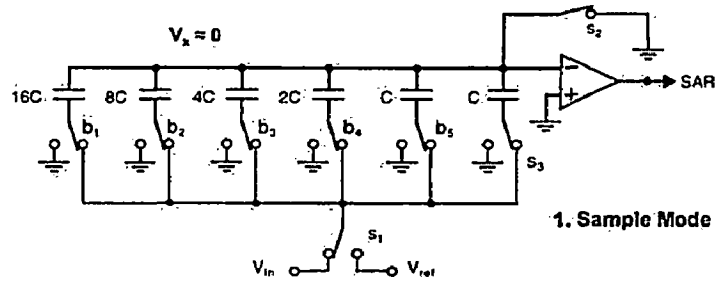


**Fig. 2.4** Operation of Charge-redistribution DAC **(a)** Sample mode [8]

In hold mode capacitors top plates are left floating and hence can assume any value. The bottom plates of the capacitors are now all connected to ground, pushing $V_x$ to $-V_{in}$.

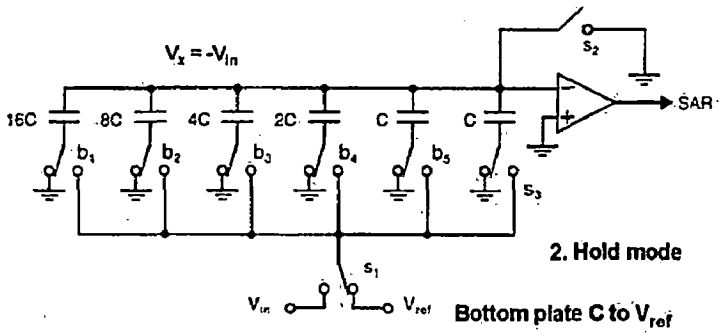


**Fig. 2.4** Operation of Charge-redistribution DAC **(b)** hold mode [8]

The successive approximation algorithm now takes place. It starts with the MSB by switching the bottom plate of the largest capacitor (16C) to the reference voltage. As the sum of all other capacitors 8C, 4C, 2C ... equals 16C, only half of the reference voltage $V_{ref}$ is added to the $-V_{in}$ voltage. If the $V_{in}$ is larger than $V_{ref}/2$, then $V_x$ is negative. In this case, the SAR register stores a digital 1; switch b1 remains as shown. If, however, $V_{in}$ is smaller than $V_{ref}/2$ then $V_x$ is positive. In this case the SAR register stores a digital 0; switch b1 is switched back, the bottom plate of capacitor 16C goes back to ground.

The sequence is now repeated with switch b2: the bottom plate of capacitor 8C is connected to $V_{ref}$. As a result, an additional $V_{ref}/4$ is added to $V_x$ for comparison. This sequence is continued until all capacitors have been switched in, until all bits have been cycled through.

Charge redistribution DAC is quite simple as it consists of one single comparator and a capacitor bank and some logic.

Because of the capacitor bank, the accuracy is limited by its matching, which is 10–12 bit, depending on the sizes of the capacitors. Its speed is limited by the speed of comparator and the RC time constants of the switches, as in any switched-capacitor system.

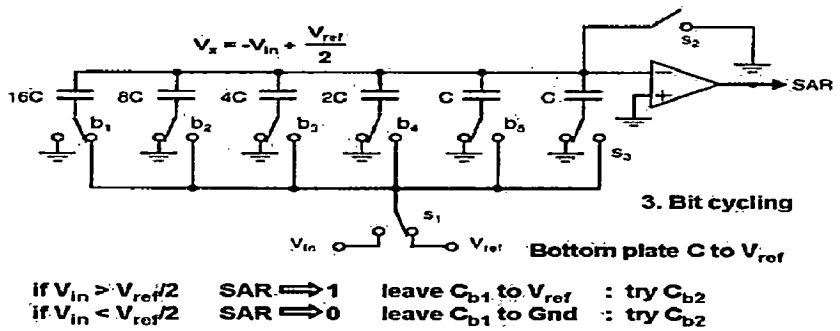


**Fig. 2.4** Operation of Charge-redistribution DAC **(c)** Bit cycling or redistribution mode [8]

## 2.3 MOS Switches

MOS transistors used as switches for sampling the input signal and in Charge scaling DACs suffer from three main physical phenomenon

1. Charge injection

2. Clock-feed through

3. Signal dependent ON resistance

4. kT/C Noise

### 2.3.1 Charge injection

When a MOS switch is on, it operates in the triode region and has a very small voltage drop across the drain and source. When the switch is turned off, a finite amount of left over charge in the inverted channel underneath the gate is dispersed into the drain, source, and substrate.

The charge injected into the input junction (when the switch is turned off) has no effect on the held voltage, and hence it can also be ignored. The charge, dependent on input voltage that flows in the opposite direction is not negligible for it introduces a gain error to the held voltage given by

$$V_{out} = V_{in}(1+\frac{WLC_{ox}}{C_H}) - \frac{WLC_{ox}}{C_H}(V_{DD} - V_{TH}) \quad \text{.....2.1}$$

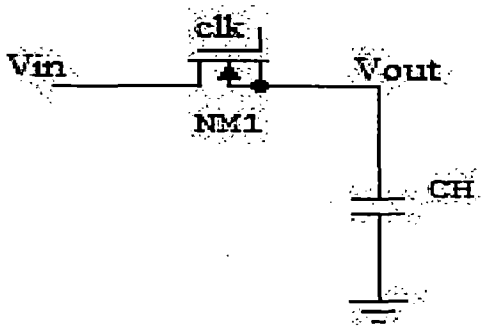


**Fig. 2.5** Operation of NMOS FET as Sampling Switch

The total channel charge is divided between the source and drain of the switch is depends on multiple parameters such as the clock turnoff slope, the ratio of the input capacitance to the output capacitance and the drain-source voltage ($V_{ds}$) [9]. The basic idea is that when the clock waveform has a steep turnoff slope, the channel is cut off before $V_{ds}$ gets a chance to weigh in; consequently, the channel charge is equally divided between the drain and source terminals. On the other hand, a slow falling clock signal gives rise to a capacitive voltage divider where $V_{ds}$ distributes the channel charge based on the capacitor ratio ($C_{in}$ /$C_{out}$).

The use of a CMOS transmission gate is one option, but it usually requires the input signal to stay at or near $V_{dd}$/2.Another plausible solution is to use the method of bottom plate sampling.

Concept is illustrated in Fig. 2.6 where transistor NM1B is turned off before transistor NM1.The charge injection due to NM1B isn't significant as it introduces only fixed charge independent of input level and can be treated as offset which can be eliminated. The charge

injected by NM1 can't flow into output node as it is floating and hence presents infinite impedance (if parasitic capacitance at that node is neglected).

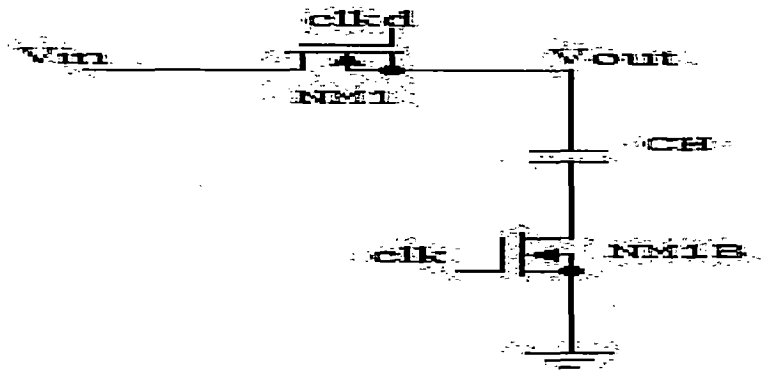


**Fig 2.6** Conceptual diagram of bottom-plate sampling method

### 2.3.2 Clock feedthrough

Clock feed through is due to the gate-to-source overlap capacitance of the MOS switch. For the S/H circuit of Fig. 2.5 the voltage change at $V_{out}$ due to the clock feed through is given by Eqn. 2.2

$$\Delta V = V_{clk} \frac{WC_{ov}}{WC_{ov} + C_H} \quad \text{.....2.2}$$

Where $C_{ov}$ is overlap capacitance of sampling gate. The error introduced by clock feed through is usually very small compare to charge injection. Also, notice that clock feed through is signal-independent which means it can be treated as signal offsets that can be removed by most systems. Thus, clock feed through error is typically less important than charge injection

Fig. 2.7 shows sound method to rectify clock feedthrough effect using dummy switch, added next to the main switch. As shown in Fig.2.7, the size of the dummy switch is set as one-half that of the main switch, and the dummy's drain and source are shorted.

According to the preceding discussion, when the main switch is turned off, half of the charge due to coupling flows through the dummy switch toward the hold capacitor ($C_H$). Note that the signal applied to the dummy's gate is complementary to Clk, and also, it should be

slightly delayed as compared to Clk so that when the dummy is turned off, the main switch is already on, and as a result, the injected charge by the dummy will be overpowered by the input signal ($V_{in}$).

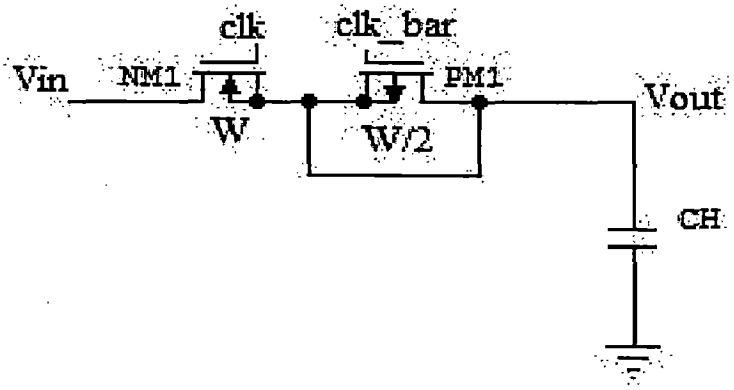


**Fig 2.7** NMOS Sampling transistor with dummy transistor

### 2.3.3 kT/C Noise

During the "on" phase, the switch can be modelled as a resistor [10] and the equivalent thermal noise of this resistor ($R_{on}$) has a one-sided, white-noise-like power spectral density given by

$$\frac{\overline{V_n^2}}{\Delta f} = 4kTR_{on} \quad \text{.....2.3}$$

As the switch is used in a sampling network where a sampling capacitor ($C_H$) is charged by the input signal through the switch during the ON phase, the thermal noise is processed by a first-order low-pass filter composed of $R_{on}$ and $C_H$, whose transfer function is given by

$$H(j\omega) = \frac{1}{1 + j\omega R_{on} C_H} \quad \text{.....2.4}$$

Thus, the total noise power at the filter's output is computed by integrating the filtered (or band limited) noise power spectral density from dc to infinity and we have

$$\overline{V_{out}^2} = \frac{kT}{C_H} \quad \text{.....2.5}$$

Interestingly it is independent of switch ON resistance $R_{on}$. Hence the value of capacitor solely determines the SNR of ADC. The capacitance of minimum capacitor that should be used can be obtained from the following inequation

$$C \geq 12k_B T\left(\frac{2^B - 1}{V_{FS}}\right)^2 \quad \text{.....2.6}$$

For 6 bit ADC operating at $V_{FS}$=1, C should be greater than or equal to 3fF. As process scales down, the problems faced by medium and high resolution ADCs are power consumption and area. Since conversion error due to element mismatch can be mitigated by various circuit techniques, signal-to-noise ratio (SNR) in high resolution ADCs is mainly limited by thermal noise.

If signal swing reduces by half due to supply voltage scaling, signal power reduces by four times. Hence four times as large capacitance is needed to reduce kT/C noise by the same amount to keep the same SNR. This requires four times large opamps transconductance to keep the same operation speed which means the bias current of the opamp and in turn its size must be increased four times. While the rest of the chip scales down, capacitors, whose size is limited by the kT/C noise requirement cannot be reduced.

### 2.3.4 Signal dependent ON resistance ($R_{on}$)

Signal dependent ON resistance of switch introduces input dependent phase shift and hence distortion. To avoid this $V_{GS}$ of sampling switch should be held constant and this can be done voltage boot-strapping. The method is conceptually based on the scheme of Fig. 2.8 that uses a charged capacitor to sustain the gate-to-source voltage of MS during the on-phase.

The switch S5 grounds the gate of the switch NM2 during Clkbar and, at the same time, switches $S_1$ and S3 charge the boosting capacitance C1 to the supply voltage. The switches S2 and $S_4$ connect C1 between the source and drain of NM2 during Clk to obtain gate boosting.

Fig. 2.9 shows the actual bootstrap circuit [11]. It operates on a single phase clock that turns the switch NM3 on and off. During the off phase, Clk is low.

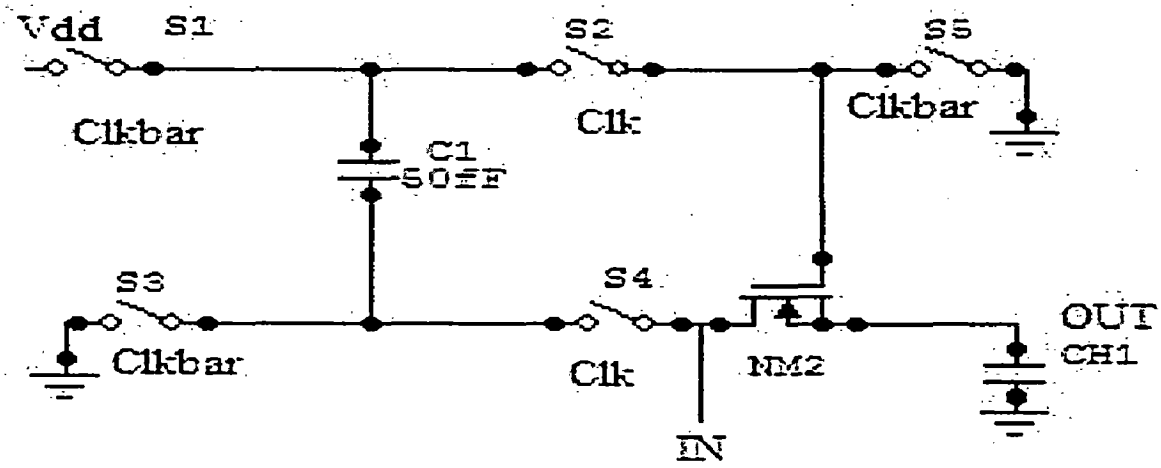


**Fig. 2.8** Conceptual Boot-strapped NMOSFET as Sample & Hold switch

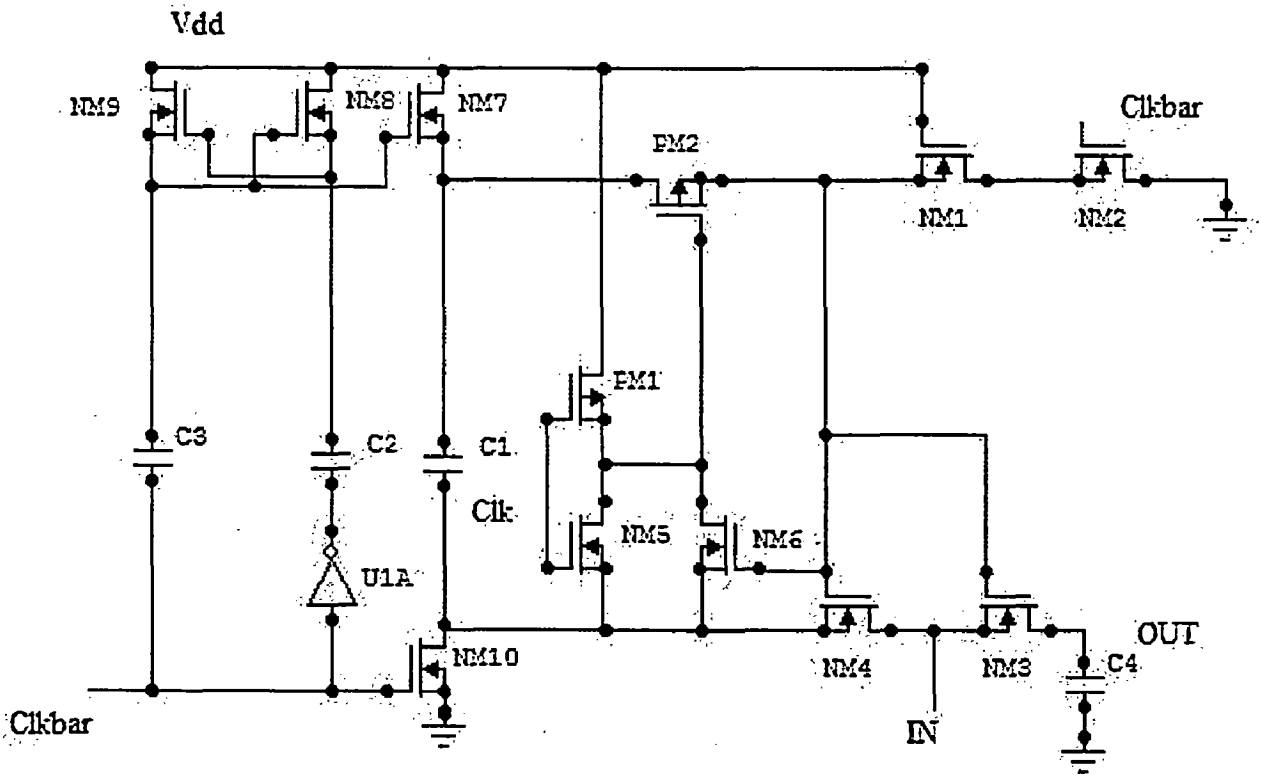


**Fig 2.9** Bootstrapped switch implemented using MOSFETs (a) Schematic

Devices NM1 and NM2 discharge gate of NM3 to ground. At the same time, $V_{dd}$ is applied across capacitor C1 by NM7 and NM10. This capacitor will act as the battery across the gate and source during the "on" phase. NM4 and PM2 isolate the switch from C1 while it is charging. When Clk goes high, NM5 pulls down the gate of PM2, allowing charge from the battery capacitor C1 to flow onto gate of NM3. This turns on both NM3 and NM4.

NM4 enables gate of NM3 to track the input voltage IN shifted by $V_{dd}$, keeping the gate-source voltage constant regardless of the input signal. For example, if the source IN is at $V_{dd}$, then gate of NM3 is at $2V_{dd}$ ; however $V_{gs}=V_{dd}$ Because the body (n-well) of NM10 is tied to its source, latch-up is suppressed.

Two devices are not functionally necessary but improve the circuit reliability. Device NM1 reduces the $V_{ds}$ and $V_{gd}$ experienced by device NM2 when 'Clk'=0. The channel length of NM1 can be increased to further improve its punch-through voltage. Device NM6 ensures that $V_{gs8}$ does not exceed $V_{dd}$.

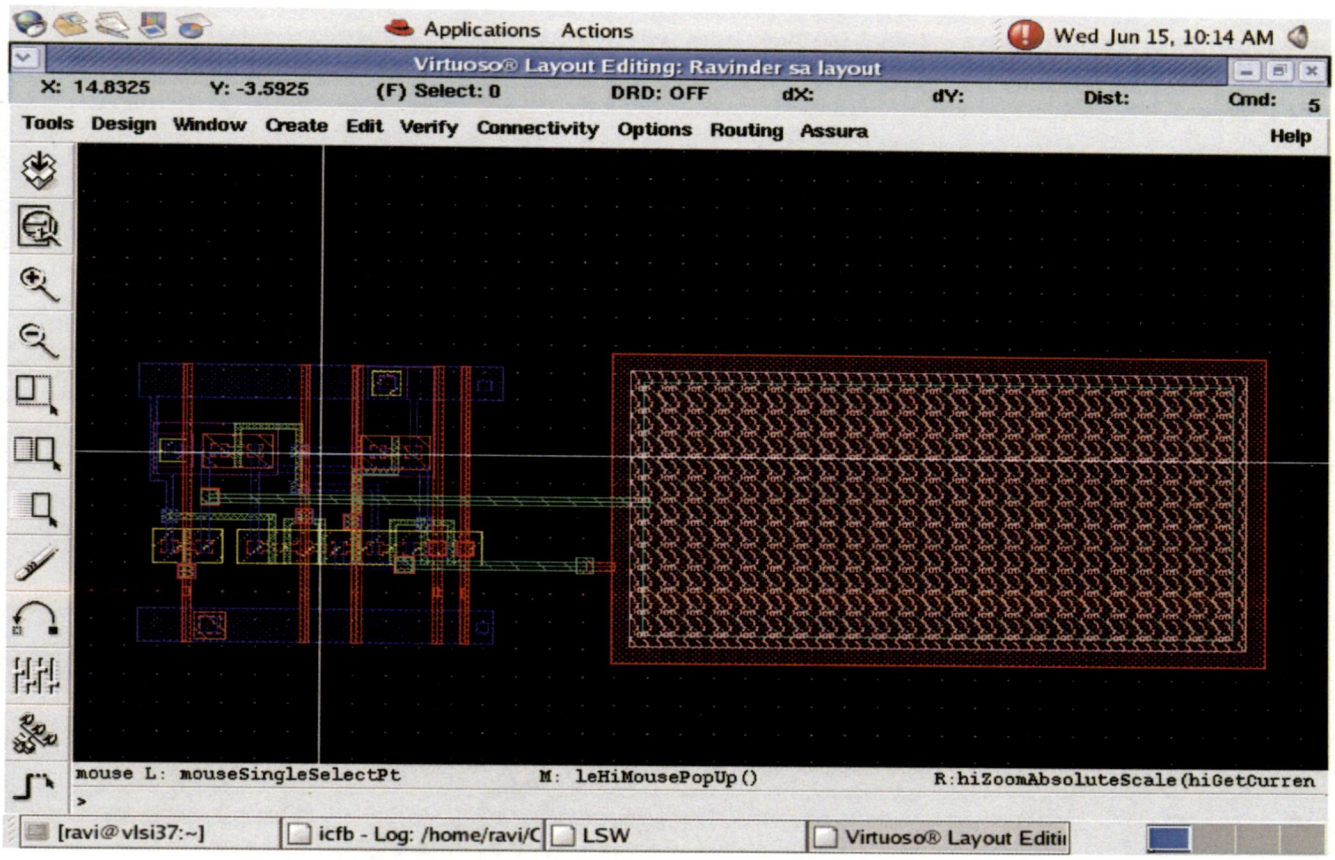


**Fig 2.9** Bootstrapped switch implemented using MOSFETs **(b)** Layout

C1 must be sufficiently large to supply charge to the gate of the switching device in addition to all parasitic capacitances in the charging path. Otherwise, charge sharing will significantly reduce the boosted voltage according to Eq. 2.7, where $C_p$ is the total parasitic capacitance connected to the top plate of C1 while it is across the main switching device NM4.

$$V_g = V_s + \frac{C1}{C1 + C_p} V_{dd} \quad \text{.....2.7}$$

NM8, NM9, C3, and C2 form a clock multiplier that enables NM7 to charge (unidirectional) C1 during the off phase. This entire circuit was carefully designed such that no device experiences a relative terminal voltage greater than. This circuit is similar to previous low-distortion sampling switch approaches that provide a constant across the switching device. In this case, however, there is the added constraint of device reliability.

The switch linearity is also improved, and signal-dependent charge injection is reduced. Variations in on-resistance due to body effect, however, cannot be eliminated.

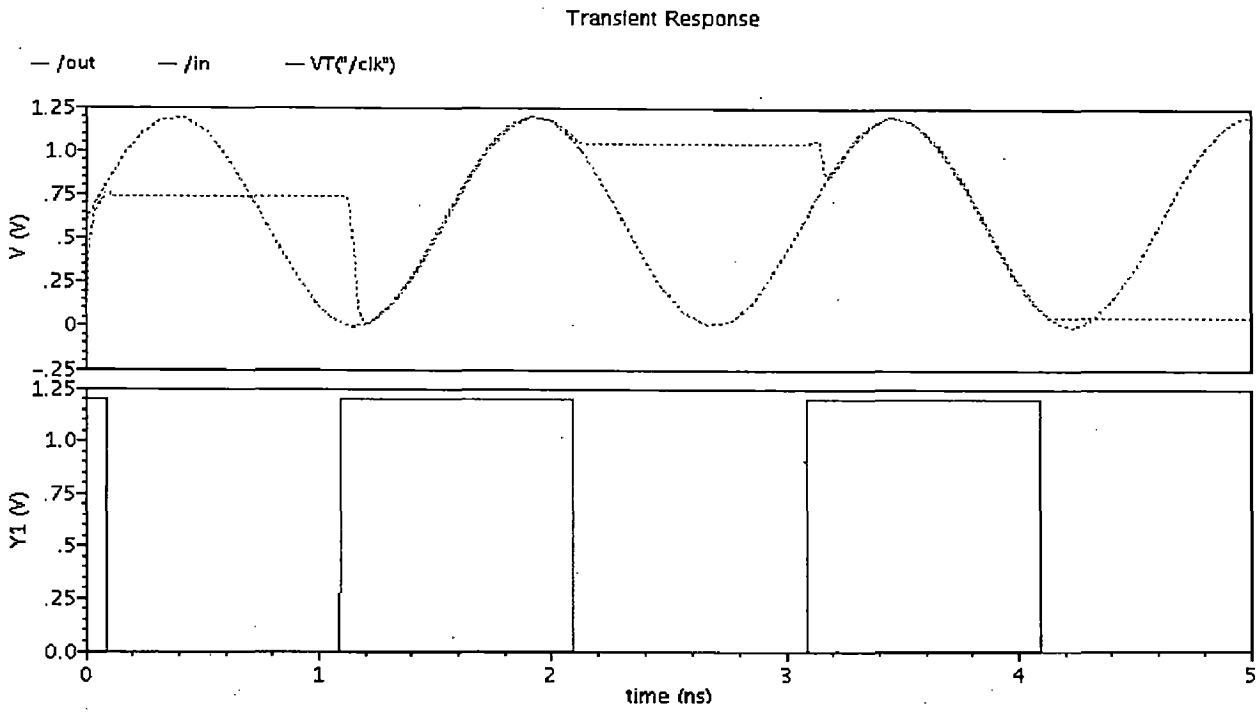


**Fig 2.9** Bootstrapped switch implemented using MOSFETs **(c)** Output

One potential transient reliability problem exists for this circuit. If the rise time of the voltage at the gate of NM3 is too fast, a large voltage could exist across the oxide of the switching device before a channel is formed to equalize the potential between the source and drain. Consider the case where the switching device's source is driven $V_{dd}$ and the drain is attached to a large sampling capacitor discharged to ground. As the switching device turns on, a voltage of approximately $2V_{dd}$ will be generated on the gate. Before a channel is formed and before the sampling capacitor is charged to $V_{dd}$ an excessive voltage greater than $V_{dd}$ may exist across the gate-to-drain terminals. This effect could create an oxide reliability problem. One solution would be to reduce the rise time by decreasing the W/L of PM2 and/or NM10. It should also be noted that the lifetime of gate oxide is roughly inversely proportional to the voltage-stress duty cycle. Therefore, such transient stress is less harmful than dc stress.

Using the ideas just stated a 6 bit DAC (with 9 capacitors) has been designed and simulated. Conceptual DAC with only one capacitor looks as shown in Fig. 2.10 .Since the speed DAC (in 'redistribution phase') depends only on parasitic capacitances at the output of DAC the size of transmission gate, with 'Clk' as control signal, should be minimised but if the size is so small the settling time of DAC in 'sampling phase' will be high and hence the size of transmission gate should be optimised and careful layout will minimise parasitic capacitance at the output node.

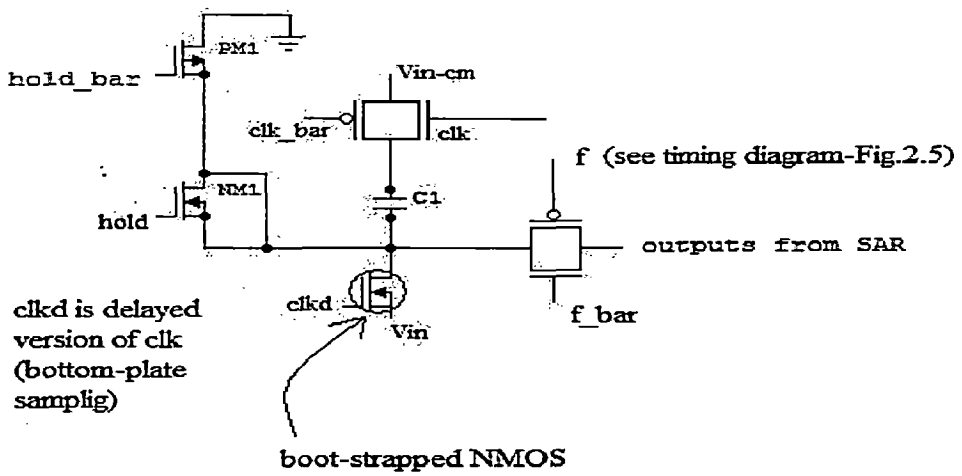


**Fig. 2.10** 1-bit Charge redistribution DAC

Fig. 2.11 shows output of 6 bit DAC, observe step size of stair-case is 18mV which is resolution of DAC for 1.2 $V_{ref.}$ Settling time of DAC in redistribution phase is around 50ps. From timing diagram (Fig. 2.5) maximum speed of ADC is 500MHz.

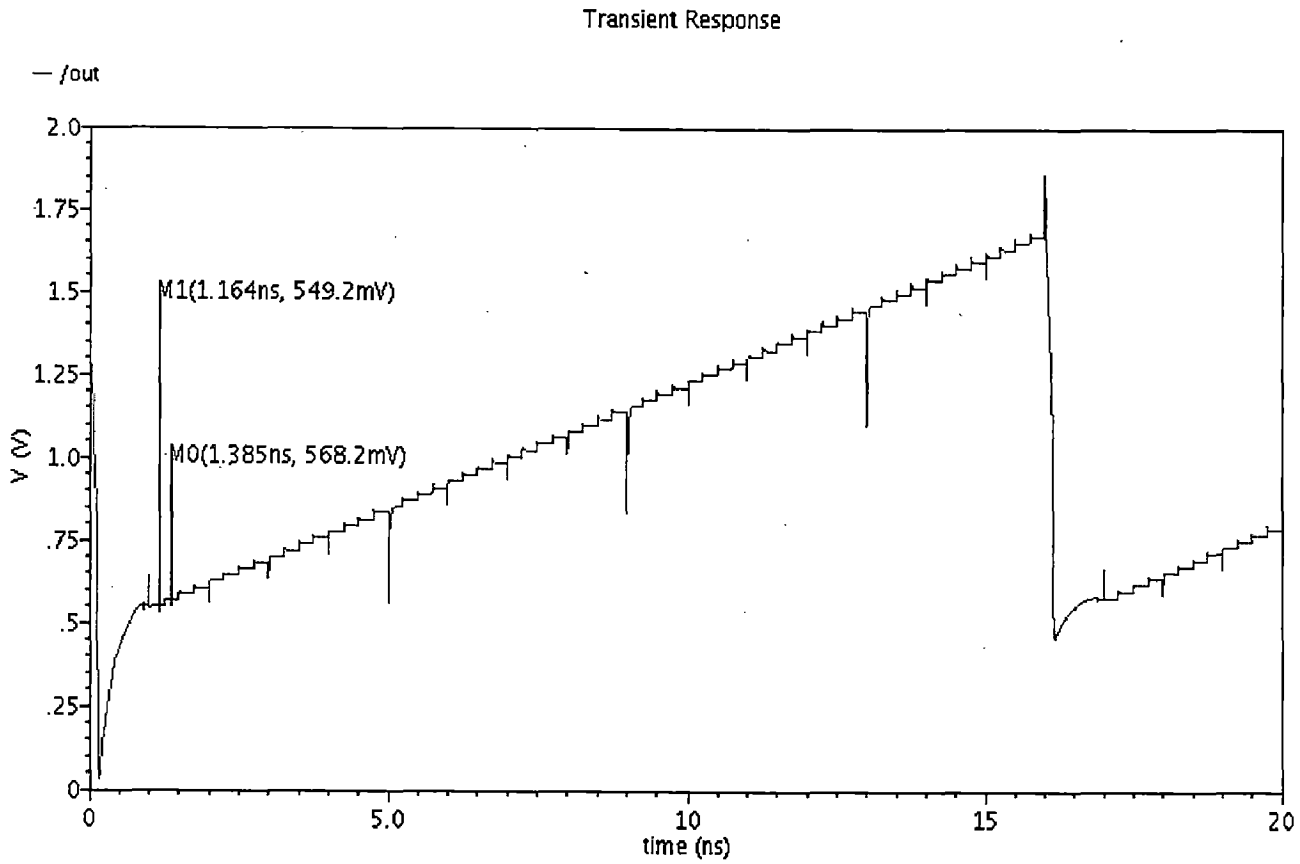


**Fig. 2.11** 6-bit DAC output

## 2.4 Comparator

The comparator in the present architecture must be both high speed and should have very little hysteresis, i.e. its offset mostly being static and not affected by the previous comparison. Since the clock frequency is 500MHz and 1ns has been allocated for sample and hold phase, max(delay of comparator, delay of flip-flop), SAR logic delay and settling time of DAC should all up to less than 333ps(1n/3 as 3 clock cycles are needed for generating 6 bits code).

Figure 2.12 shows the schematic diagram (a) and layout (b) of the high-speed, low hysteresis comparator [12], which consists of dynamic comparator and static CMOS latch (cross coupled NAND).

To reduce hysteresis, extra 'pre-charge' transistors have been added to make that every node in the master dynamic comparator is completely precharged to $V_{dd}$ before the 'Clk' signal goes high. Because of the way the SAR logic works, the comparator must hold the decision until the next 'Clk' edge, therefore a slave latch, in general realized by cross-coupled NAND gate for this type of comparator, must be used.

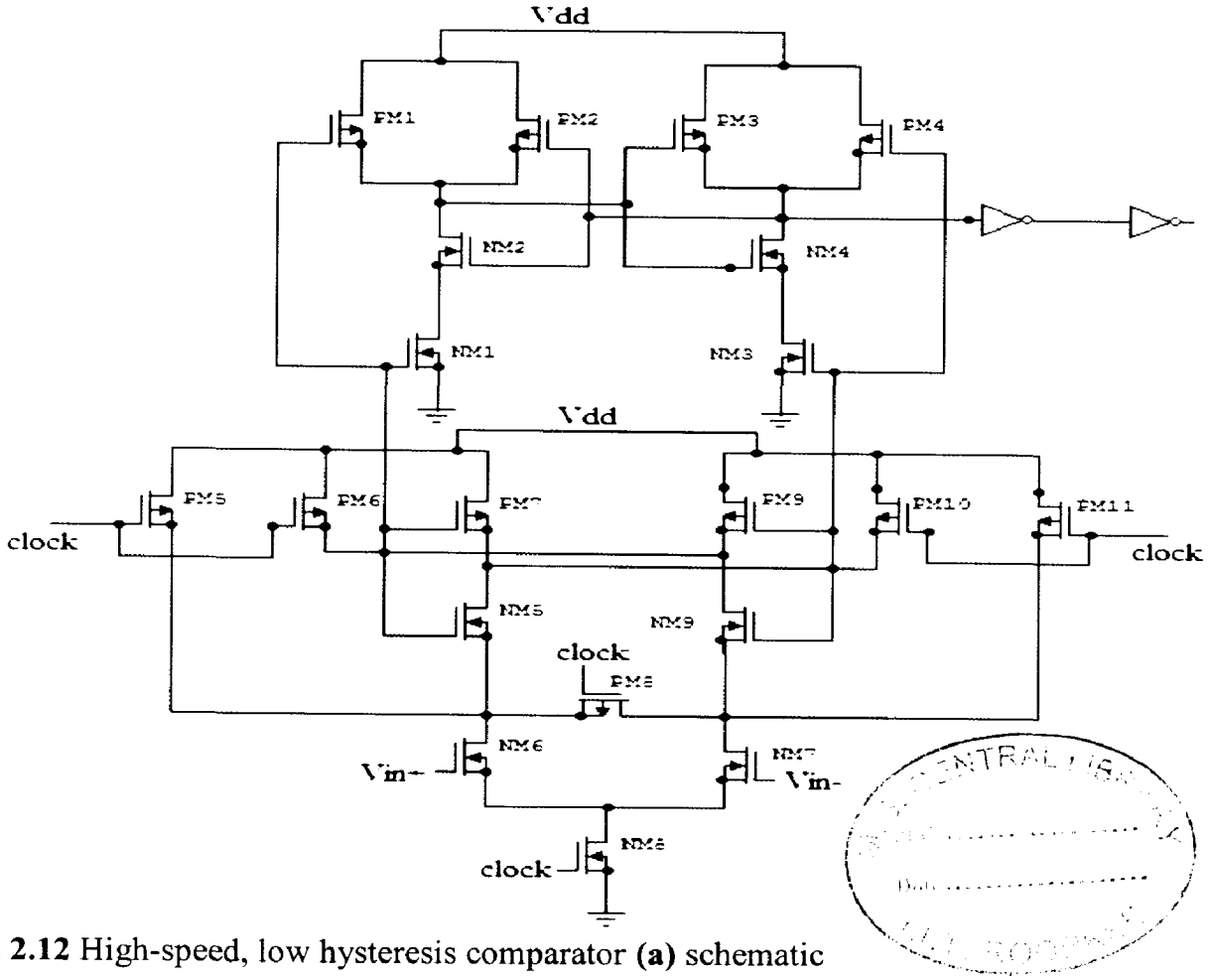


**Fig. 2.12** High-speed, low hysteresis comparator **(a)** schematic

The outputs of the dynamic comparator were connected to the bottom NMOS rather than top NMOS that is exposed to NAND gate outputs. This is because depending on the NAND gate output being high (low) i.e. the previous comparison, the channel is not completely formed (with drain = $V_{dd}$ and source = $V_{dd}$-$V_{th}$) (formed) and hence presenting different load capacitance (as capacitance of gate is different in different regions) to the dynamic comparator, resulting in hysteresis. On the other hand, if they are connected to the bottom NMOS, the channel is always formed there regardless of the latched state, since drain/source are shorted to ground with the top

NMOS turned off. The PMOS of the NAND gate is completely off, hence does not present much data dependent load capacitance.

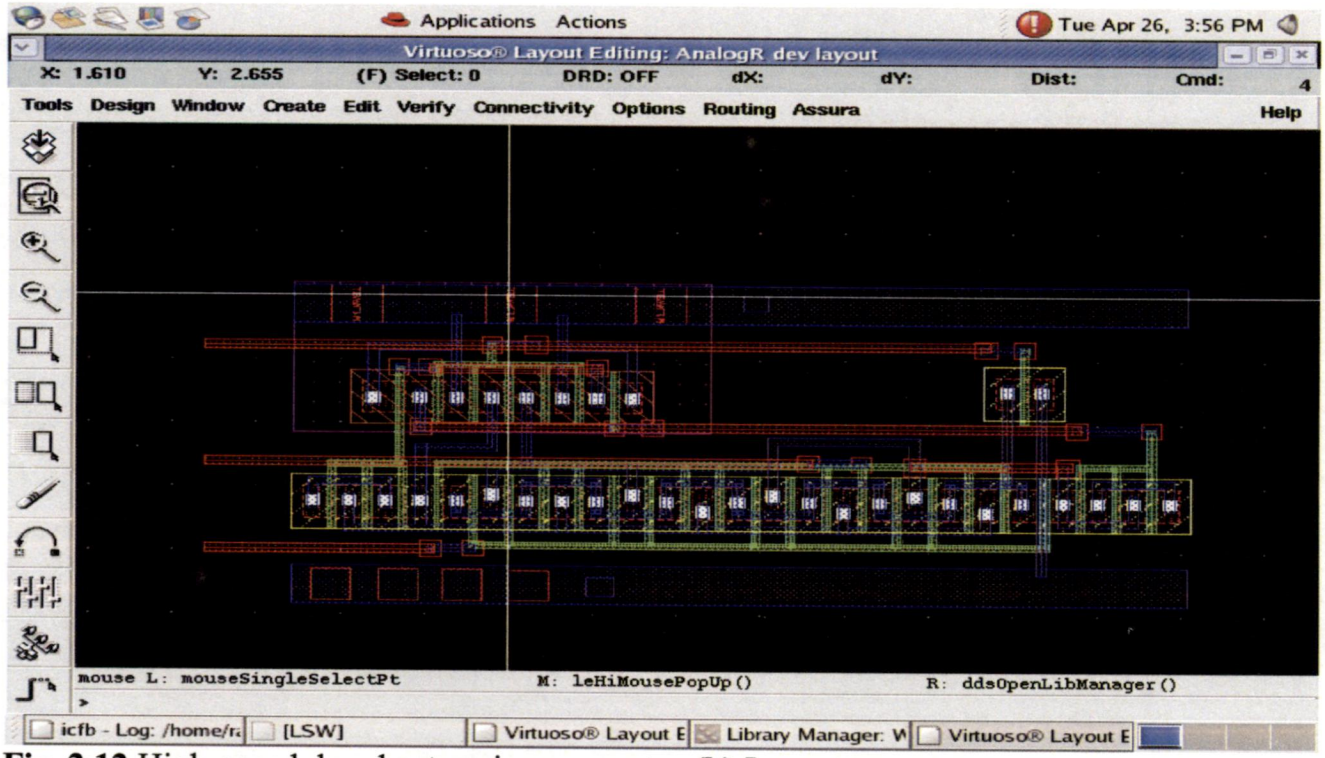


**Fig. 2.12** High-speed, low hysteresis comparator **(b)** Layout

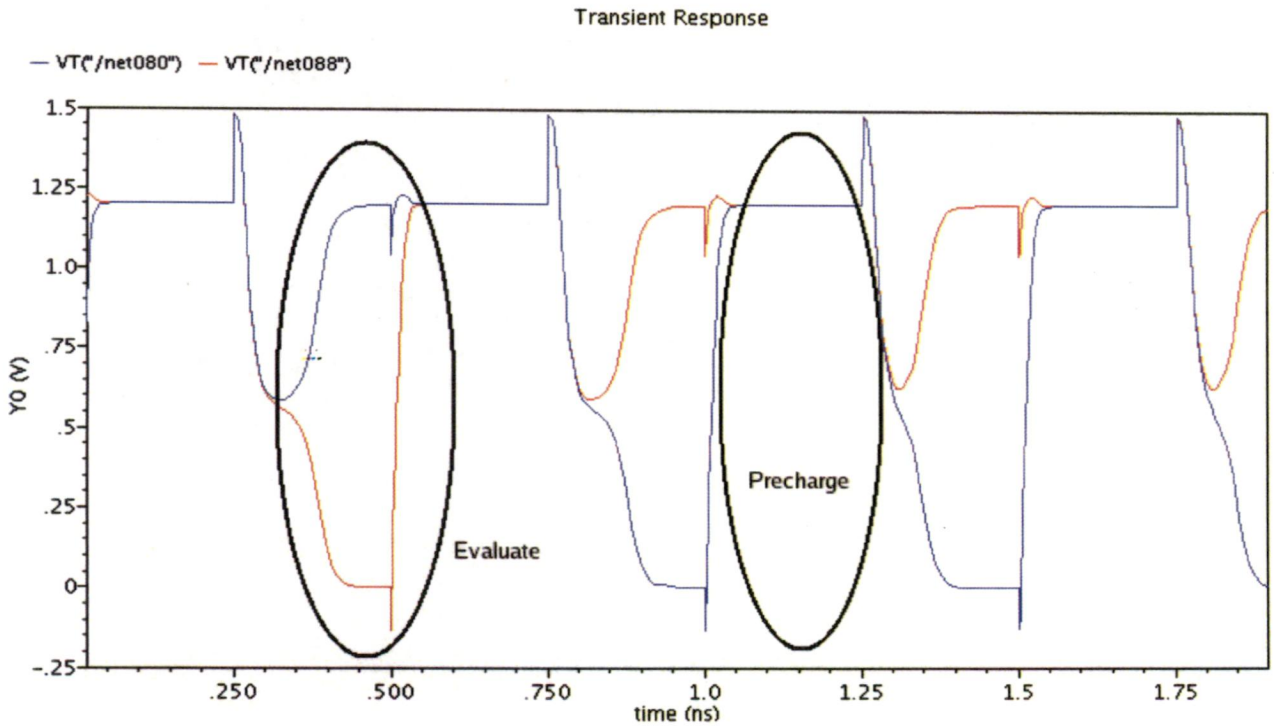


**Fig. 2.12** High-speed, low hysteresis comparator **(c)** Output

However, the offset of comparators, which for conventional SAR architecture results in DC offset of whole ADC (and isn't issue), becomes an issue in time interleaved SAR ADC. Mismatch between offsets of comparators lead to nonlinearity in ADC transfer curve and hence degrades INL/DNL. Mismatch among offsets should be less than half of the LSB so that there are no missing codes in ADC output.

$V_{th}$ mismatch between NM6 and NM7 is plotted as shown in Fig. 2.13 using Monte-Carlo analysis with 1000 runs in Cadence spectre for gpdk090 technology. From plot it can be observed that $\sigma_{Vth}$=5.95mV hence if we take $3\sigma_{Vth}$~18mV (99% confidence level) will be the offset of comparator.

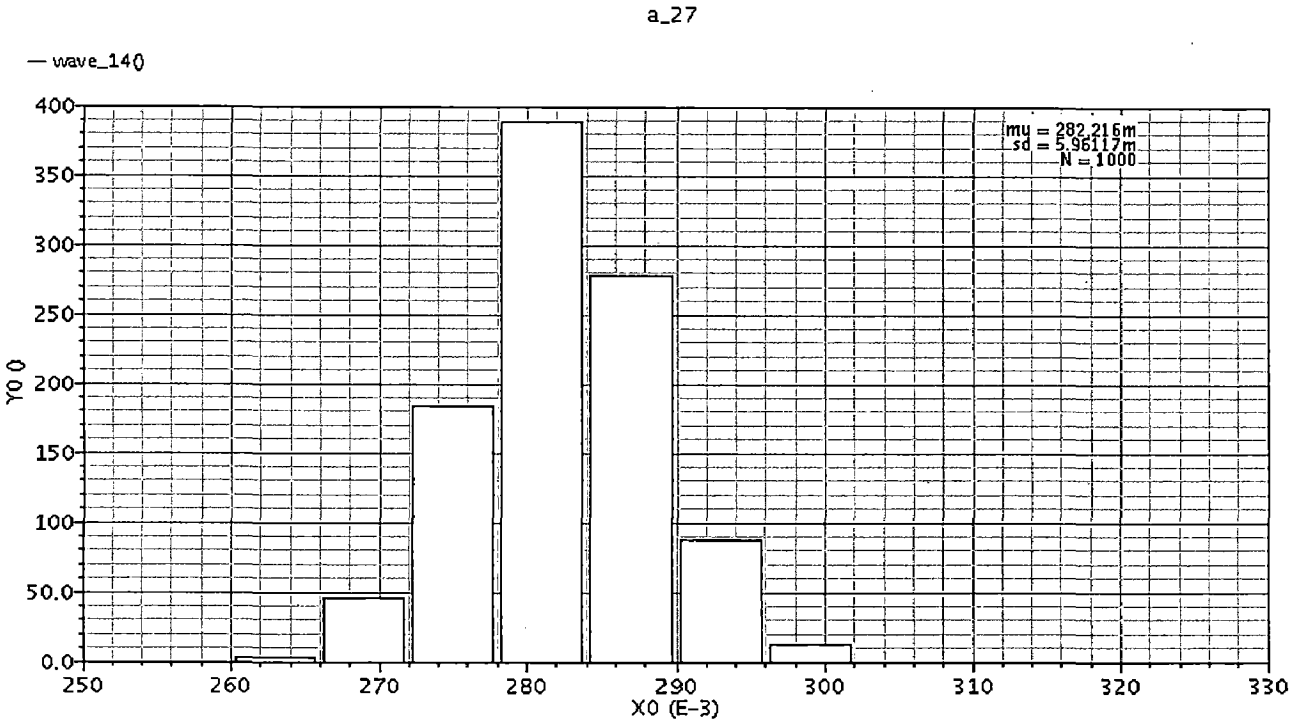


**Fig. 2.13** Monte-Carlo simulation of Offset of comparator (due to PVT and Mismatch)

In order to reduce the offset there are techniques like adding pre-amplifier with some gain or overdesigning (increasing size of transistors) comparators is usually done. Placing of pre-amplifier before comparator also reduces kickback noise but delay of the pre-amplifier adds to loop delay of SAR architecture hence reduces speed of ADC.

My work includes novel method of reducing offset of comparator by 'back-gate biasing'. Offset of comparator is due to $V_{th}$ due to PVT. $V_{th}$ mismatch in NMOS differential pair (NM6,

NM7) is most important contributor to offset of comparator. Hence comparator can be made immune to process variations by compensating process variations in NMOS differential pair.

Extra circuitry is added to existing comparator to make it process variation resilient. Fig. 2.14 shows modified comparator with additional control signals.

The operation of comparator is compromised of two phases, Comparison phase and offset compensation phase. During offset compensation phase 'f' is high, capacitors C1 (and C2) are charged through NM6, NM15 and NM10 (NM7, NM18 and NM21)

If there is mismatch ($V_{th}$ and W/L) between NM6 and NM7 voltage across capacitors C1 and C2 will different. If $V_{th}$ of NM6 is greater than that of NM7 then due to difference in currents from NM6 and NM7 C2 will be charged more than C1

During Comparison phase voltage across C1 (and C2) is connected to body of NM6 (and NM7).Since $V_{th}$ is dependent on $V_{SB}$ through following relation

$$V_{th}=V_{th0}+\gamma\left(\sqrt{(|2\phi_f+V_{SB}|)}-\sqrt{2\phi_f}\right) \quad \text{.....2.8}$$

More voltage across on C1 (because of less $V_{th}$) results in more $V_{SB}$ and hence $V_{th}$ of NM6 is increased. Thus $V_{th}$ mismatch between NM6 and NM7 is reduced. The value of C1, C2 W/L of NM6 and NM7 and pulse width of 'f' should be carefully chosen so that current through C1, C2 during compensation should be linear function of time.

Capacitors (C1 and C2) are discharged, before every 'offset compensation phase', to ground through NM12 and NM17, controlled by 'reset' signal. Major limitation of this type comparator is it demands twin-tub (or even PWELL) process where we are free to connect bulk of NMOS to any potential in the circuit.

Similar Monte-Carlo analysis on this comparator shows comparator offset of 7.98mV, less than half the LSB of ADC (=9mV). Note the increase in mean value $V_{th}$ this may increase the Clk-Q delay of comparator but as there is no pre-amplifier before comparator delay due to pre-amplifier won't add to loop delay of SAR ADC.

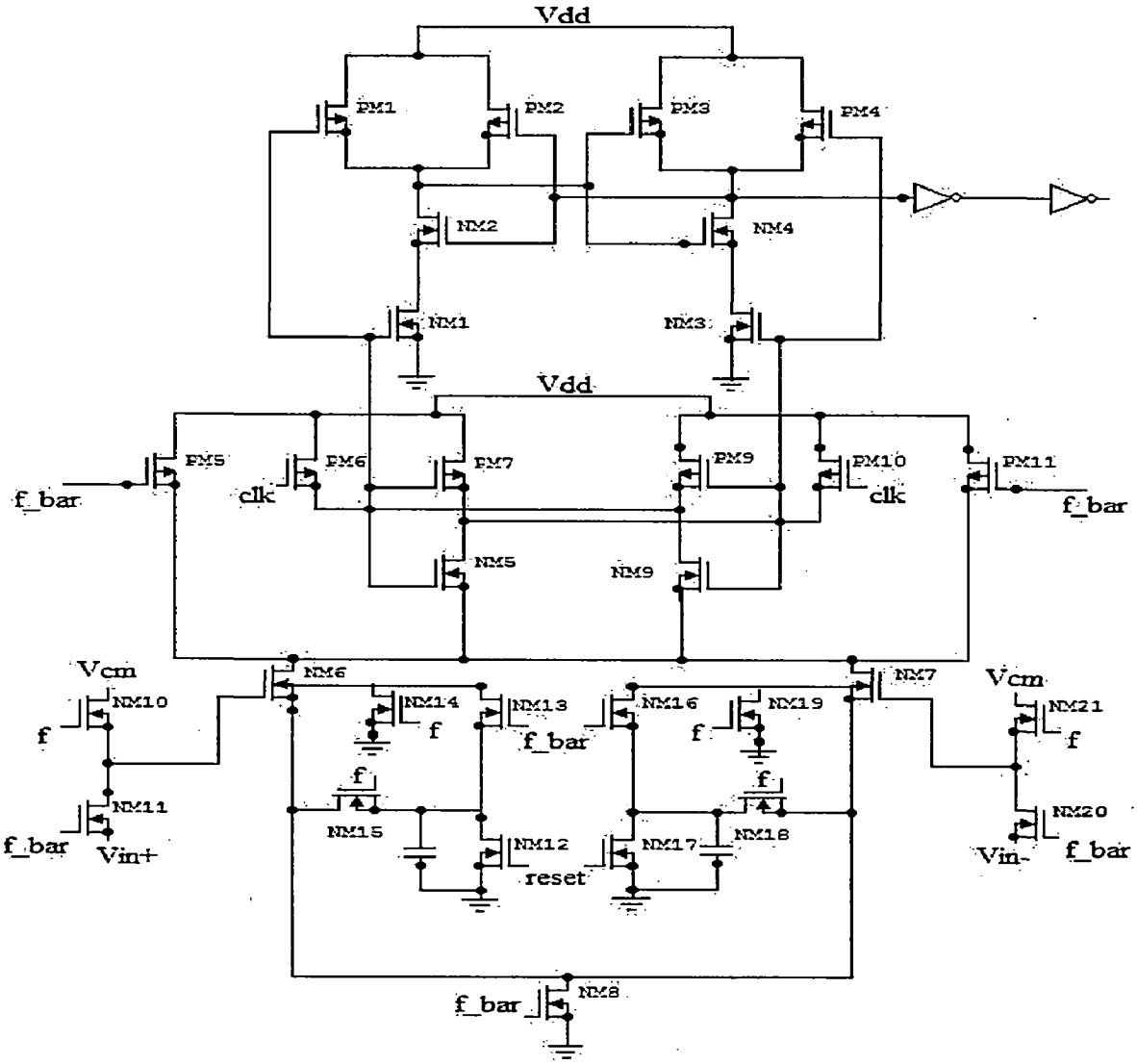


**Fig. 2.14** Proposed self-compensating Comparator schematic

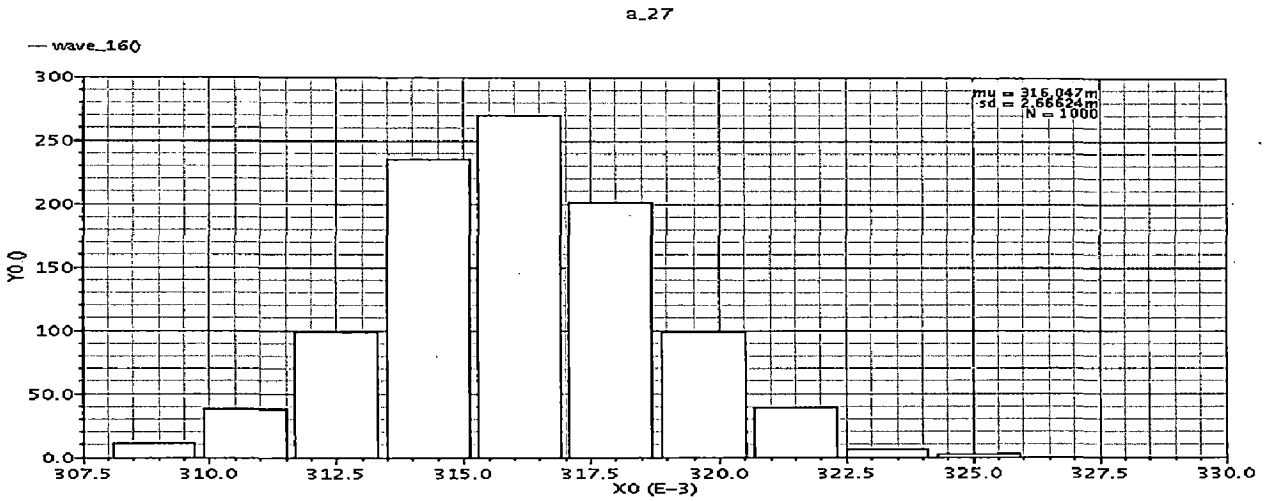


**Fig. 2.15** Monte-Carlo simulation of Offset of Self-compensating comparator

## 2.5 Successive approximation Register (SAR)

Combinational part of SAR is implemented using transmissions gates (multiplexers), static CMOS gates (logic) and TSPC D flip-flops (Register). Multiplexers are highly optimised for less propagation delay, minimum glitch size and area as first two will affect the speed of DAC and three fold effect on speed of entire ADC. Fig. 2.16 shows layout (b) and sample output (c) of SAR combinational block.

| | State 1 | State 2 | State 3 |
|---|---|---|---|
| a1~a3 | (001)/(011)/(111) | Pass quantizer outputs | Pass D-FF output |
| b1~b3 | (000) | (001)/(011)/(111) | Pass quantizer outputs |
| c1~c3 | (000) | (000) | (001)/(011)/(111) |

**Table 2.1** SAR logic operation

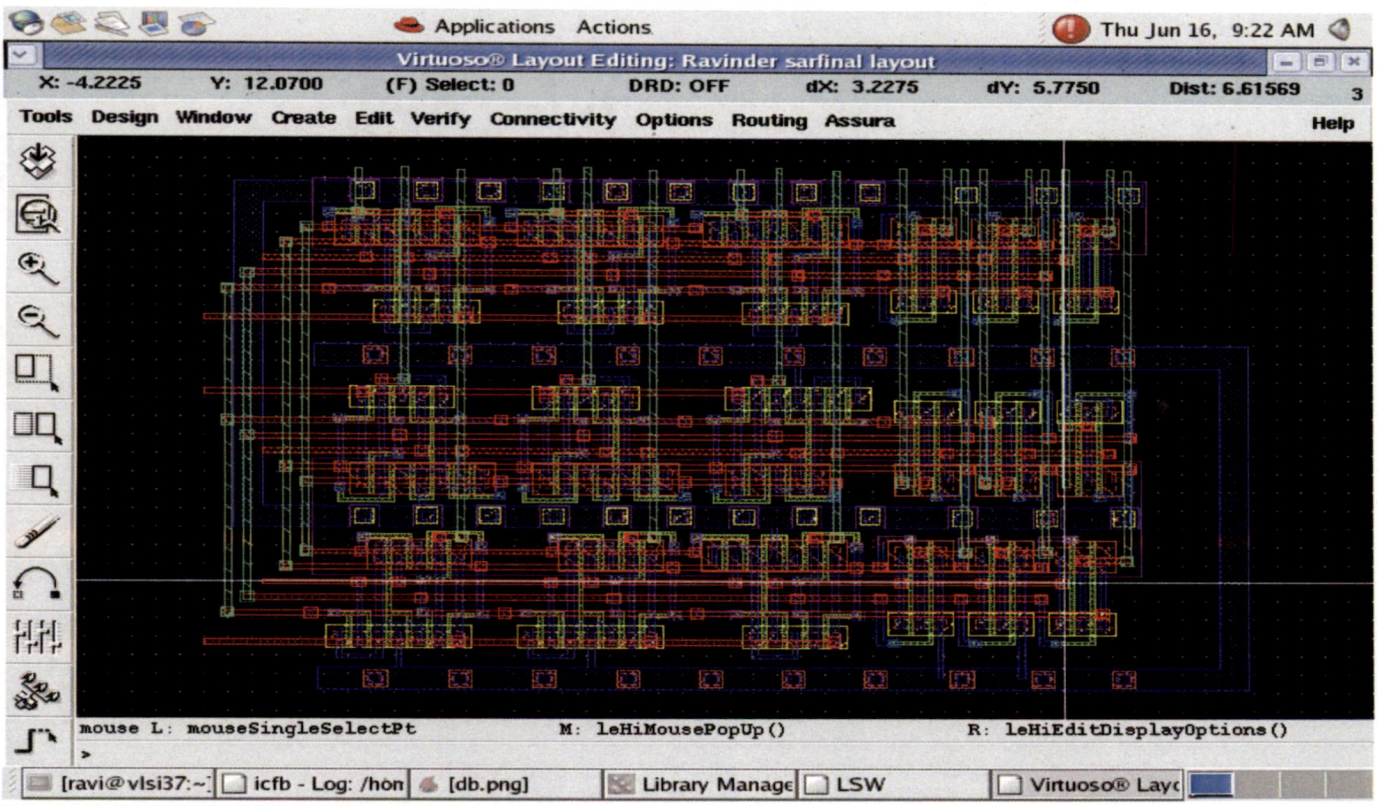

Fig. 2.16 SAR logic **(a)** Layout

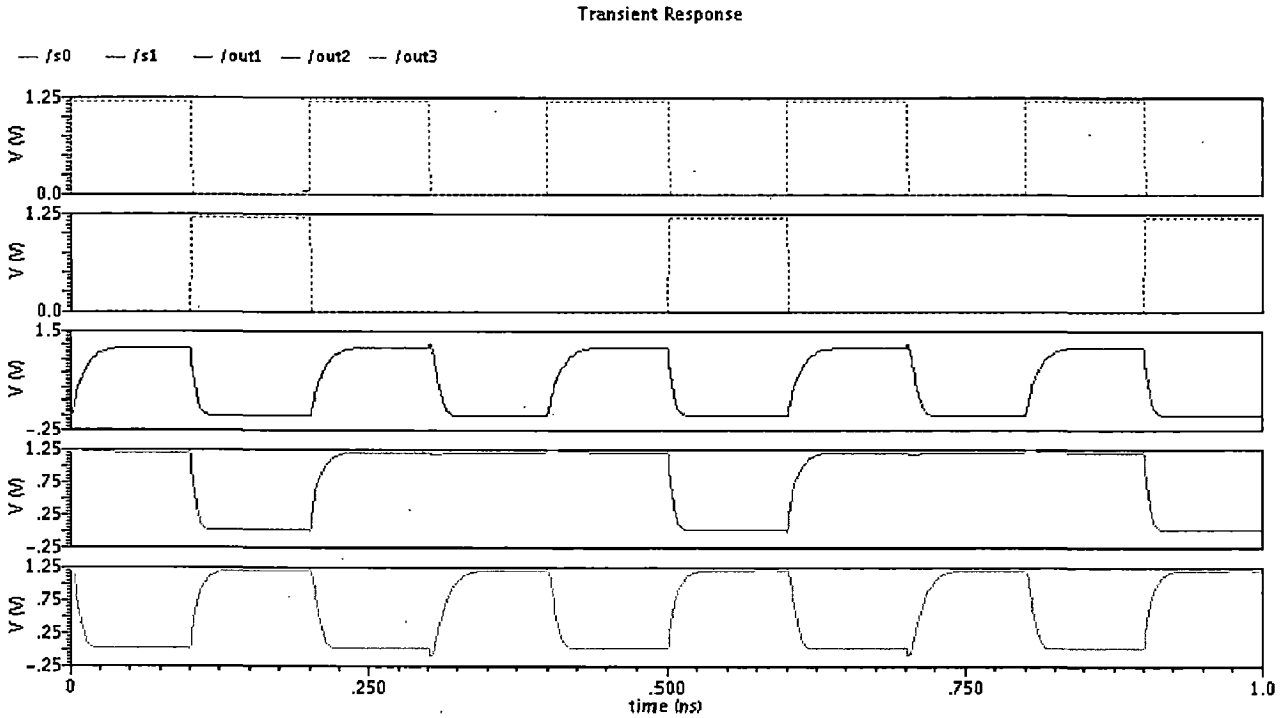


Fig. 2.16 SAR logic **(b)** Output

### 2.5.1 Glitch free TSPC D-flip-flop

The true single-phase clocking scheme has the inherent advantage of immunity to clock skew problems as it operates at only one clock phase. TSPC achieves race-free clocking by using the complementary nature of N and P transistors in CMOS to simulate the effect of two-clock phases. TSPC flip-flops find their applications operating at very high speed.

The TSPC 9-transistor D-FF in Fig. 2.17 has a glitch at the output QB. Depending on the transistor dimensions, the size of the glitch can become very serious indeed. Glitches at the output of flip-flop lead to slower settling at the output of Capacitive DAC and hence speed is deteriorated.

The sequence of logic transitions that lead to the glitch is as follows. If input D = 0 when clk = 0, node output of first dynamic comparator will be $V_{dd}$ while second inverter will be precharged to $V_{dd}$. During the evaluation phase, clk = 1, which turns off PM2 and turns on NM4. Node y2 cannot discharge instantly and remains high for a short time, which can be long enough to cause QB to discharge. This may lead to discharge of output node of second inverter and

eventually go below the threshold of the inverter formed by PM5 and NM3, causing QB to move up again to the correct output of logic 1.

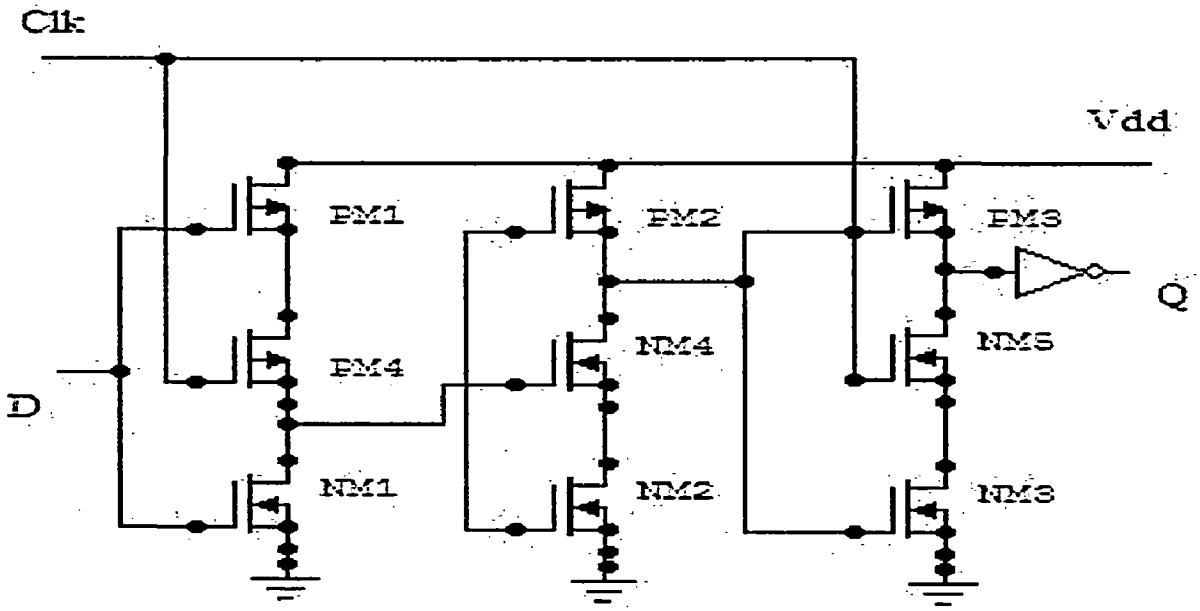


**Fig. 2.17** Conventional TSPC D Flip-flop

The glitch-free D-FF with feedback transistor, to minimize the internal glitch, has been shown in Fig. 2.18 (a) [13] (layout in 2.19 (b)). The speed of flip flop is slower than conventional but we need to introduce buffer at the output of conventional latch so as to filter glitches and hence the total Clk-Q delay will be more than glitch-free version.

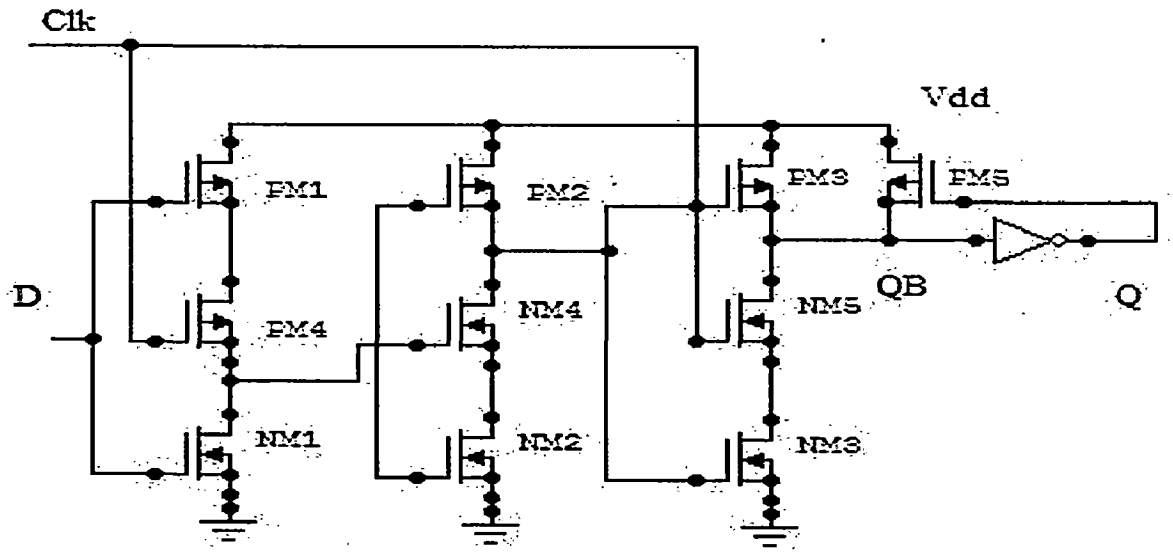


**Fig 2.18** Glitch-free TSPC D Flip-flop **(a)** Schematic

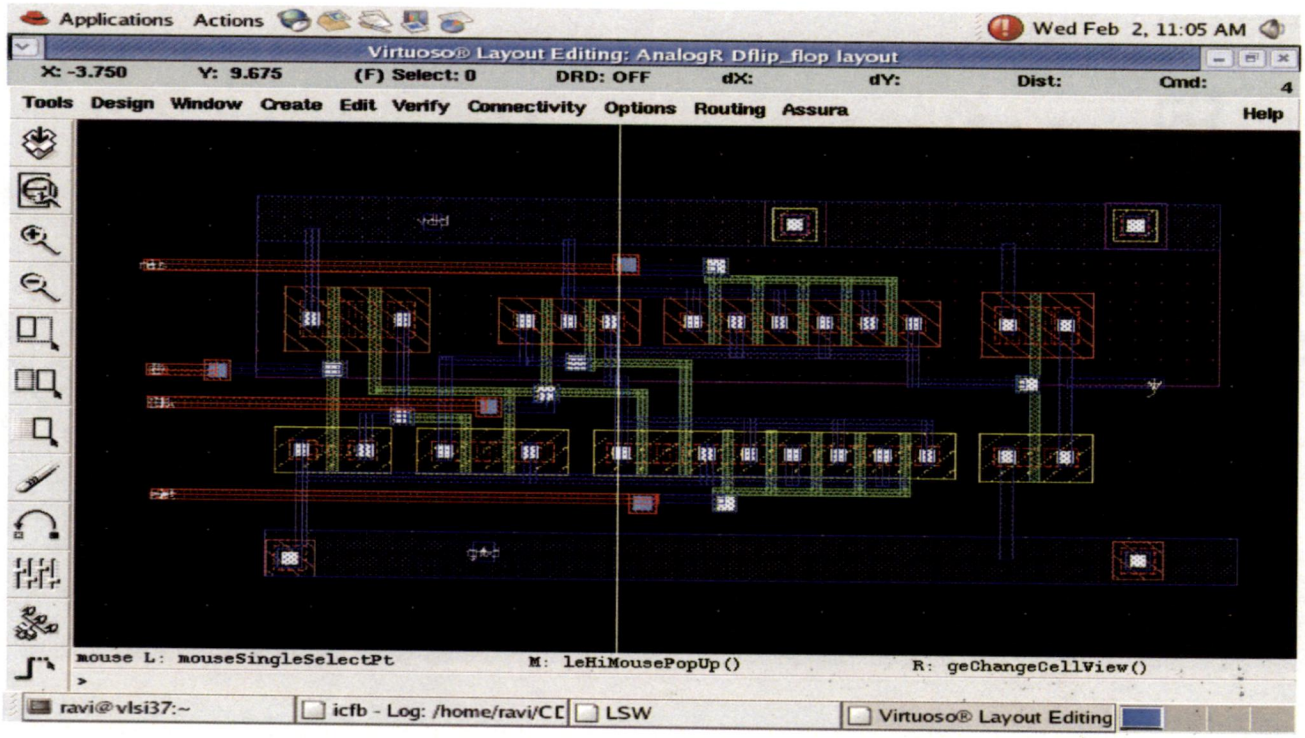


**Fig 2.18** Glitch-free TSPC D Flip-flop **(b)** Layout

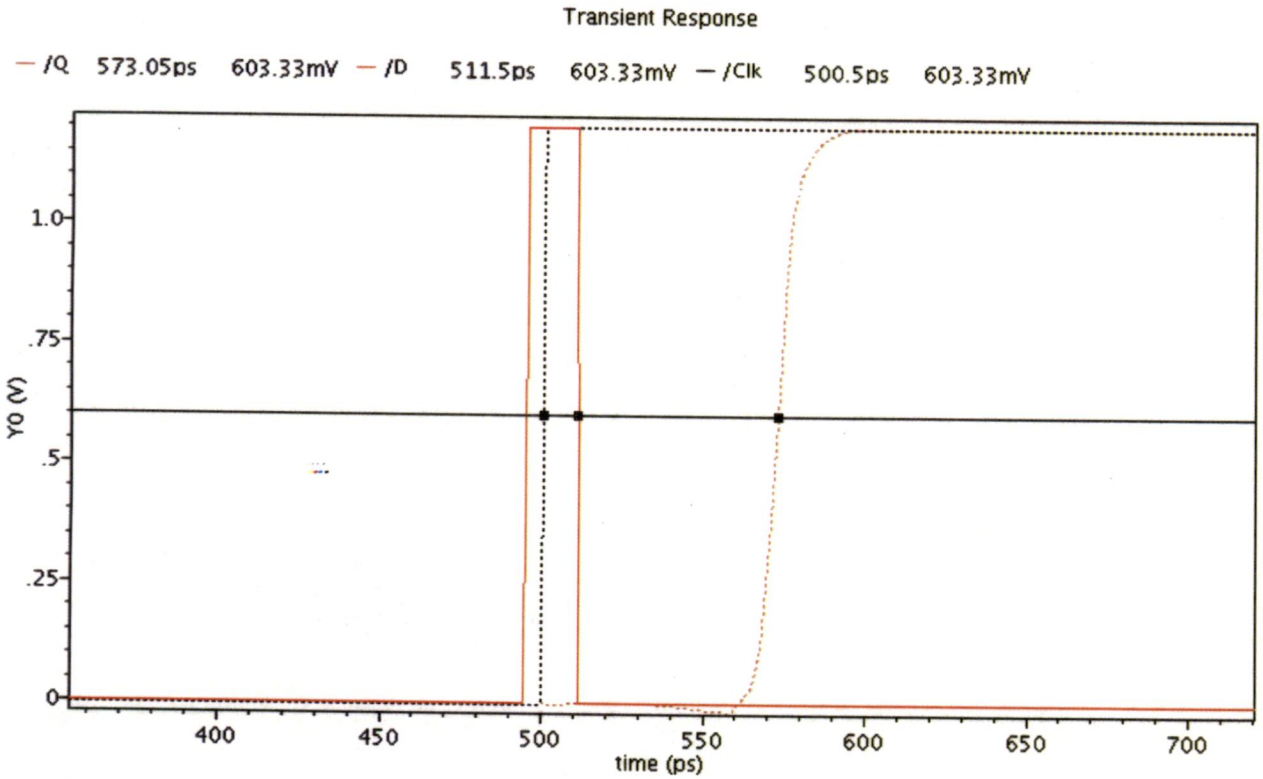


**Fig 2.18** Glitch-free TSPC D Flip-flop **(c)** Output

## 2.6 Simulation Results

Fig 2.19 shows outputs of DACs for 600mV input. Observe that at the end of each conversion process (22ns and 24ns) DAC outputs will be close to 600mV (=Comparator second input)

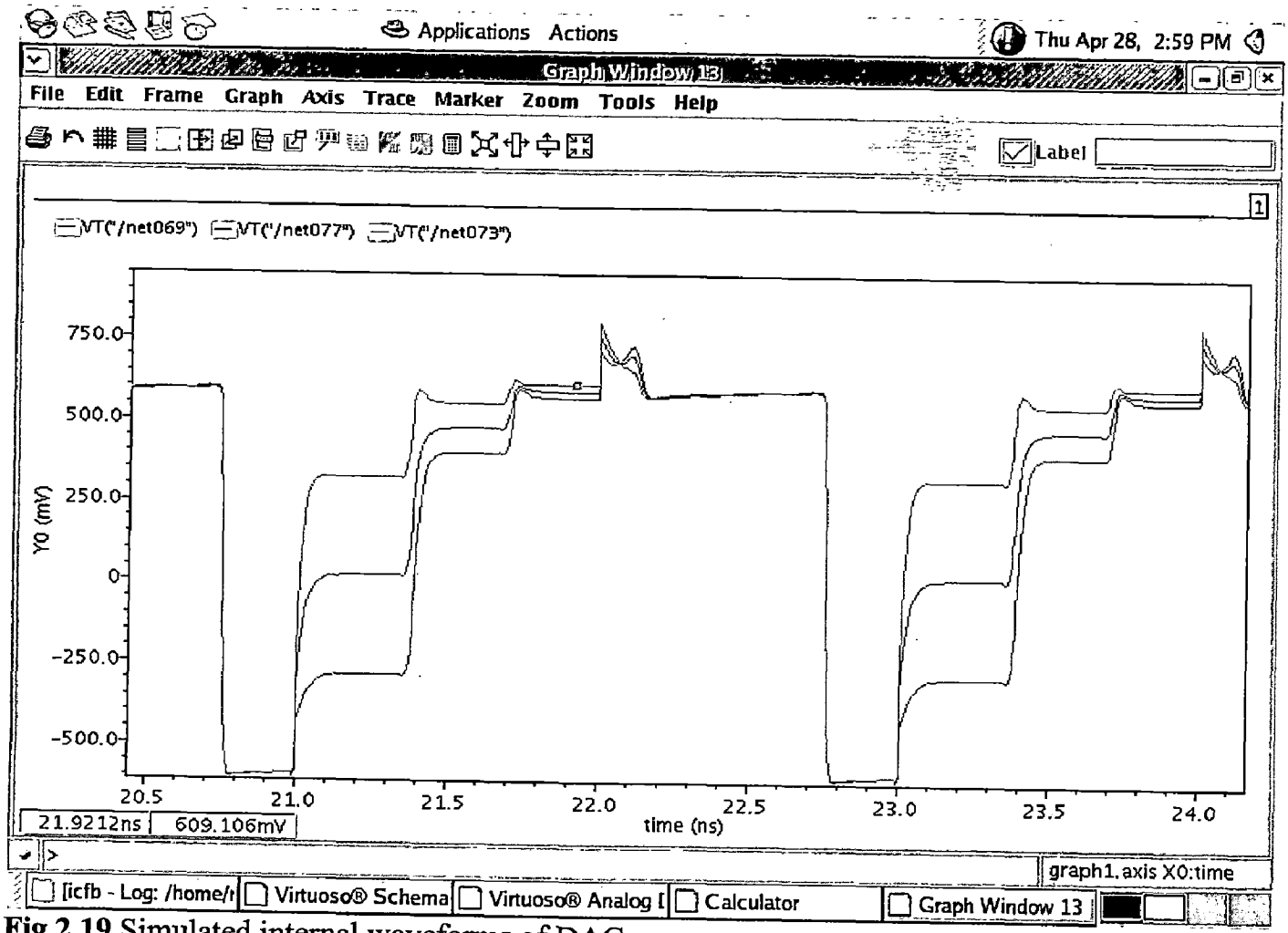


**Fig 2.19** Simulated internal waveforms of DACs

For evaluating dynamic performance of ADC a sine wave (101.5625MHz frequency, 600mV ac and 600mV DC) is given as input to ADC. Transient analysis is run for 140ns (=64*(1/500MHz) + 12ns (initial settling time)). A 64 point FFT of the output transient plot is taken. The final FFT plot is shown in Fig. 2.20.

Spectrum at 101.5625M represents input signal, second harmonic (HD2) is 40dB below input signal

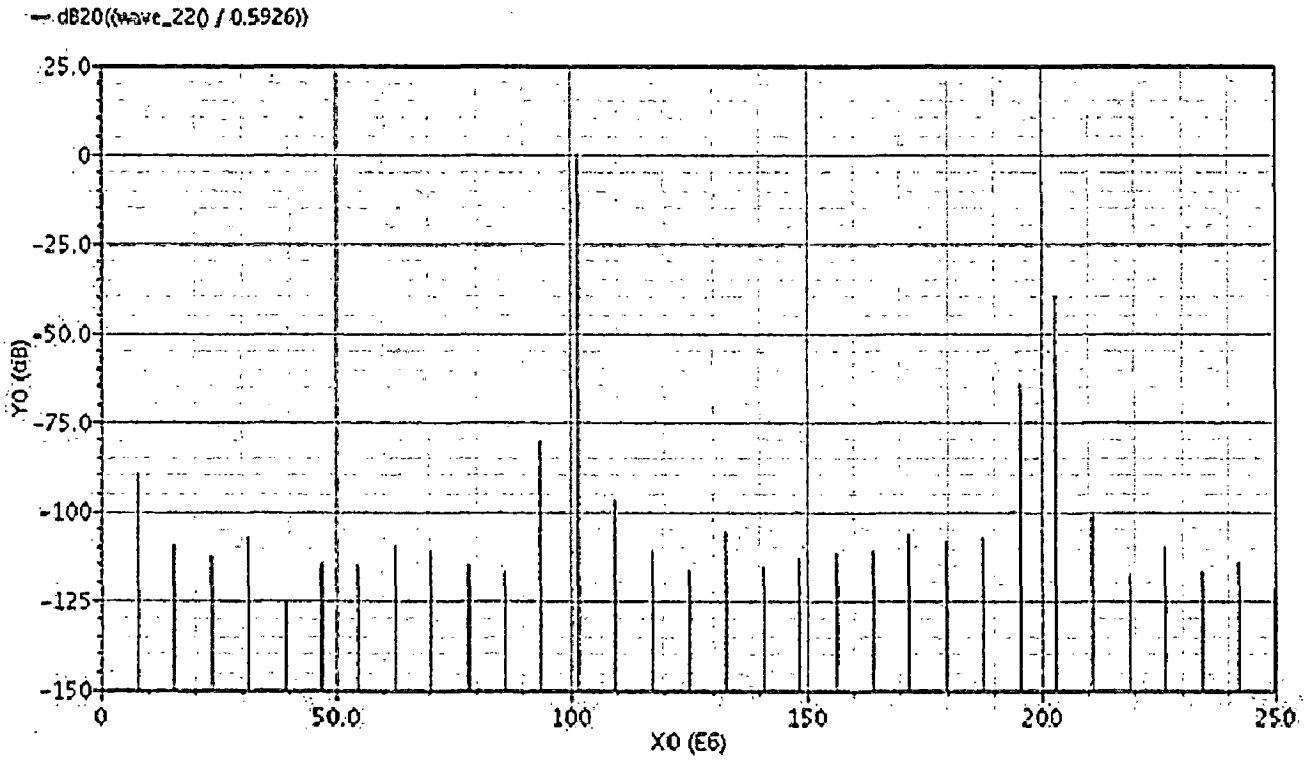


**Fig. 2.20** 64point FFT of ADC output (@ 101.5625M input frequency)

# Chapter3
# Conclusion and Future Scope

In summary this work mainly focuses at designing low power ADC operating at very high sampling rate and with reasonable resolution. Low power consumption is the direct result of more than 10 times less comparators and much simpler thermometer-to- binary encoders than conventional 6b flash architectures (3 full-adders versus 57 full-adders in a 6b Wallace-tree encoder).

Performance of ADC relies on matched capacitor networks and as the lithography process improves very high SNDR ADCs can be realized even in scaled process.

The measured offset of 'self-compensating' comparator is around 8mV and can be reduced further in future by improving 'back-gate biasing' technique, so as to use it in high resolution ADCs.

Summary of ADC specifications:

| | | |
|---|---|---|
| No. bits | : | 6 |
| Sampling rate | : | 500 KSPs |
| Input signal range | : | 0~1.2 V |
| SNDR | : | >30dB |

# References


1 A.-J. Annema, B. Nauta, R. van Langevelde, and H. Tuinhout, "Analog circuits in ultra-deep-submicron CMOS," *IEEE J. Solid-State Circuits*, vol.40, pp.132–144, Jan. 2005.

2 C. Sandner, M. Clara, A. Santner, T. Hartig, and F. Kuttner, "A 6bit, 1.2GSps low-power flash-ADC in 0.13μm digital CMOS," *IEEE J. Solid-State Circuits*, vol.40, pp.1499–1505, July 2005.

3 Behzad Razavi, *Principles of Data Conversion System Design*, IEEE Press,1995

4 A. Varzaghani and C.-K. K. Yang, "A 600-MS/s 5-bit pipeline A/D converter using digital reference calibration," *IEEE J. Solid-State Circuits*, vol.41, pp.310–319, Feb. 2006.

5 Y. Shimizu, S. Murayama, K. Kudoh, H. Kohhei, and A. Ogawa, "A 30mW 12b 40MS/s subranging ADC with a high-gain offset-canceling positive-feedback amplifier in 90nm Digital CMOS," in *IEEE ISSCC Dig. Tech. Papers*, pp.218–219, 2006.

6 Y. Choi, J. Koh, and G. Gomez, "A 66dB-DR 1.2V 1.2mW single-amplifier double-sampling 2nd-order ΔΣ ADC for WCDMA in 90nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, pp.170–171, 2005.

7 B. P. Ginsburg and A. P. Chandrakasan, "Dual time-interleaved successive approximation register ADCs for Ultra-Wideband receiver," *IEEE J. Solid-State Circuits*, pp.247–257,Feb. 2007.

8 F.Maloberti, *Data Converters*, springer, 2007.

9 G. Wegmann, E.A Vittoz, and F.Rahali, "Charge Injection in Analog MOS Switches," *IEEE J. Solid-State Circuits*, vol.SC-22, pp.1091-1097, Dec. 1987.

10 J.H. Fisher, "Noise Sources and Calculation Techniques for Switched Capacitor Filters," *IEEE J. Solid-State Circuits*, vol.17, pp.742-752, Aug. 1982.

11 A. Abo et al, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," *IEEE J. Solid-State Circuits*, vol.34, pp. 599, May 1999.

12 Z. Cao, S. Yan, and Y. Li, "A 32 mW 1,25 GS/s 6b 2b/step SAR ADC in 0.13 um MOS," *IEEE J. Solid-State Circuits*, vol. 44, No. 3, March 2009

13 T.Burd, Low-power CMOS Library design methodology, MS thesis, ERL, University of California, Berkeley, August 1994.