"DEVELOPMENT OF ELECTRONIC LOW FREQUENCY MEASURING INSTRUMENT"

A DISSERTATION

Submitted in partial fulfilment of the
requirements for the award of the degree
of
MASTER OF ENGINEERING
in
ELECTRICAL ENGINEERING
(Measurements and Instrumentation)

By

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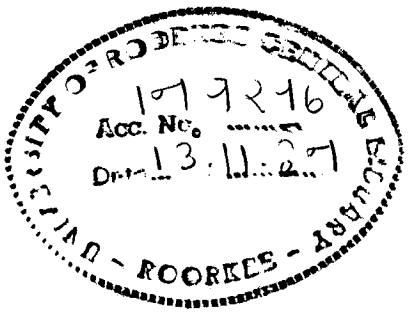

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D E C L A R A T I O N

I hereby certify that the work which is being presented in the thesis entitled "DEVELOPMENT OF ELECTRONIC LOW-FRRQUENCY MEASURING INSTRUMENT" in partial fulfilment of the requirement for the award of the Degree of MASTER OF ENGINEERING in Electrical Engineering with the specializati zation in " Measurements and Instrumentation," submitted in the Department of Electrical Engineering, University of Roorkee, is an authentic record of my own work carried-out during the period: Jan'86 to Jan'87

Under the supervision of Dr.R.N.Mishra and Sri S.Mukherjee.

The matter embodied in this thesis has not been submitted by me for the award of any other degree.

DATE 2.1.1987

(A.K. JAIN)
SIGNATURE OF THE CANDIDATE

This is to certify that the above statement made by the Candidate is correct to the best of my knowledge, and belief.

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A C K N O W L E D G E M E N T

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DATED - JANUARY 1987

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A B S T R A C T

Low Frequencies are, generally, measured by using period measurement. The method, however, inherits inaccuracy as one have to take reciprocal of time period to measure frequency. Here frequency multiplying technique using PLL is used to multiply the low frequency and this multiplied frequency is, then, counted using frequency comparision scheme.Thus display counters will display directly in terms of frequency.with proper decimal adjustment.

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C O N T E N T S

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LIST OF FIGURES

CHAPTER-1

INTRODUCTION

Frequency Measurements has always been an interesting problem. ~~problem.~~ Simplest frequency measurement was started by counting the number of cycles of given operation e.g. slow swing of pendulam. With the progress in Science a number of new techniques of frequency measurement has come into existence Now-a-days digital techniques have evolved out which are highly accurate so far. Digitally frequency can be measured in two mode mode (1) Frequency comparision mode (2) Period measurement made.

Till now, the simplest technique of low frequency (below-20H_z) measurement was period measurement. But this, was at the cost of accuracy. However, the accuracy could be improved by using more gate opening period but then, at the cost of time i.e. process becomes quite slow.

Now, there is no need of using period measurement scheme for low frequency comparision scheme. Here input frequency, which is quite low (e.g. 1-6H_z), is moltiplied by some suitable multiplying factor N (Here N = 1000) and then this multiplied frequency is conunted by the same frequency comparision scheme.

The meter should find application in measuring physiological pulse rates, slow moving physical systems (such as low shaft speed measurement).

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C H A P T E R- 2

MEASUREMENT OF LOW FREQUENCY SIGNAL: A REVIEW

Following are the few general techniques when we go for frequency measurements:

(a) ANALOG TECHNIQUES-

1- Mechanical Resonance type or Vibrating reed type.

2- Electrical Resonance type.

3- Electro Dynamo meter type.

4- Weston type.

5- Ratio meter type.

6- Saturable Core type.

7- Frequency bridges.

8- Stroboscopic Methods.

9- C.R.O. Methods.

(b) DIGITAL TECHNIQUES OF FREQUENCY MEASUREMENTS

But for measurement of low frequency there are some well known methods which can be categorized in two main categories.

(a) Analogue Techniques

(b) Digital Techniques.

(a) ANALOG TECHNIQUES-

2.1 AN ACTIVE FREQUENCY METER [1]

Principle - Ref.Fig. (2.1-a)

Here the basic scheme employs frequency selective bridge which uses a quadrature amplifier (QA). The emplifier provides an output voltage which is equal to the input voltage

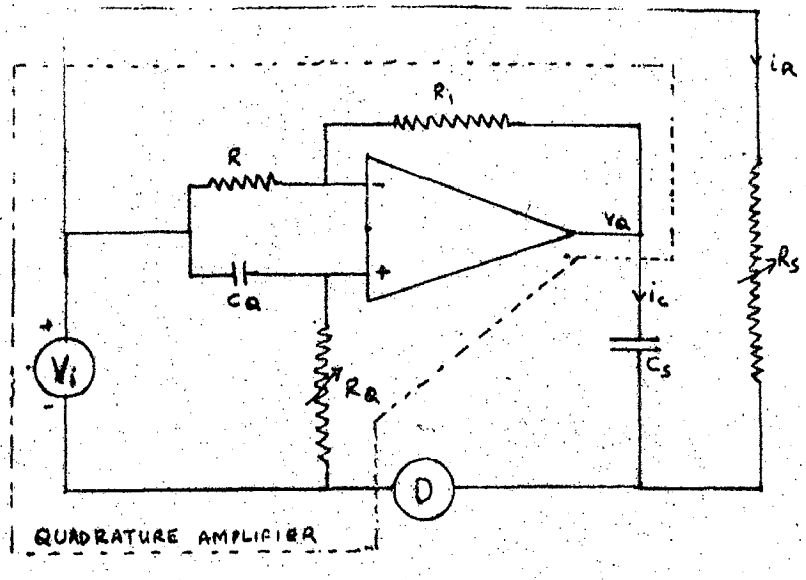


FIG. (2.1 a) Frequency selective bridge using active RC quadrature amplifier

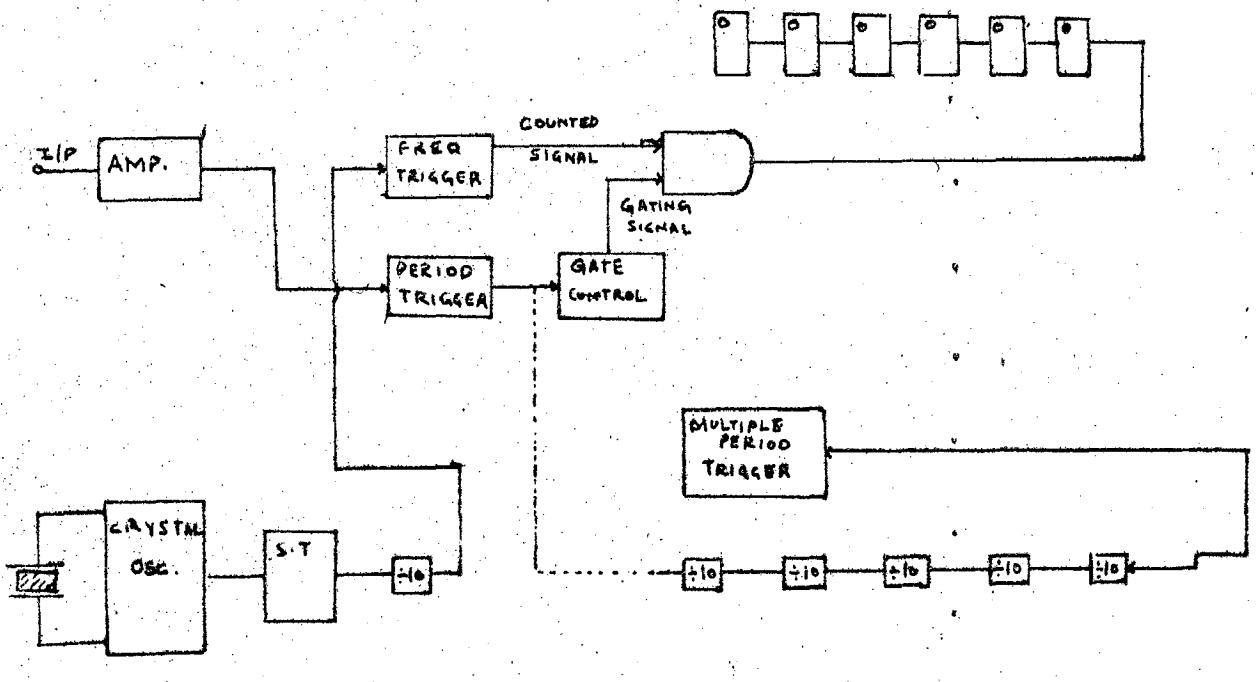


FIG. (2.2 - a)
Block diagram of single & multiple period Measurement.

in magnitude but 90^{o} out of phase. The standard resistor (R_s) and capacitor C_s are compared. A low impedance current detector D is used in the frequency meter. At balance resistive and capacitive current i_c and i_R must balance each other and current through detector should be zero i.e.

$$i_c + i_R = 0 \qquad \text{---} \qquad (2.1.1)$$

$$\frac{jV}{-j/\omega C_s} \quad \frac{V}{R_s} = 0 \qquad \text{---} \qquad (2.1.2)$$

On solving equation (2.1.2) we find the final balance condi-as -

$$\omega C_s R_s = 1 \qquad \text{--} \qquad (2.1.3)$$

The equation (2.13) shows that the frequency can be measured in terms of the resistance and capacitance.

COMMENTS: -

1) This frequency selective bridge using an RC active QA can be used to measure frequency in the range of 10 H_z - 100 KH_z in four decade ranges.

2) It has low component count.

3) It requires only one adjustment for balance.

4) Basically being an RC type bridge errors due to skin effect and eddy current are absent.

5) It has higher current sensitivity than Wein's bridge.

6) The shielding arrangement used is simple and perfect. Most of the stray capacitances among the Shields and

earths appear either across supply or detector, where as in Wein's bridge these appear across ratio arms.

7) With resistor and capacitor of tight tolerance the frequency meter can give accuracy of measurement better than 0.1% in the entire frequency range.

8) It can also be used for frequency control.

-****-

[b] DIGITAL METHODS

2.2 PERIOD MEASUREMENT [2]

One of the basic technique used in low frequency measurement is period measurement instead of frequency, as measurement of frequency in low frequency range leads to low accuracy results.

We know, period of un known signal (with Frequency f) can be written as $T = \frac{1}{f}$. Therefore, what we do in period measurement, we simply interchange the function of the two input signals (namely standard and unknown) coming to the main gate. i.e.unknown frequency signals now determines duration of the signal (standard) in other words unknown frequency signal now acts as gating signal or Gate control element. On the other hand known frequency or standard frequency is allowed to pass through the gate under the control of gate control.

COMMENTS:

Here the main draw back in using period measurement is that to get accuracy at low frequencies. One must take reciprocal of the answer displayed by the display counters if he wants to know the input frequency. Also, at low frequencies reciprocal of a quantity does not produce accurate results i.e. 0.33 sec.will give a frequency as 3 H_z, which should be more/than 3 H_z similar is case with 7 H_z period,measurement process will give us result as 0.14 sec.and reciprocal of this will be more than 7 H_z. However, the accuracy

of the scheme described above can be greatly increased by using multiple period average mode of operation. Here main gate is held open for more than one period of the unknown signal This can be done by using decade dividers. So that unknown frequency is divided by 10 or 100 or more. In other words period can be extended by a factor of 10, 10^2 or more depending upon the requirement.

COMMENTS:

(1) The main drawback of the system lies in the fact that to open gate for 10 or 100 of cycles of unknown will take considerable time and signal might change (if our unknown signal frequency is not steady enough)during this time.

(2) Here digital display on the counter will show more digits of information thus increasing the accuracy. However, the decimal point location and measurement units are usually changed each time on additional decade divider is added so that display is always in terms of period of 1 cycle of input signal.

[3]

2.3. COUNTER INVERTS PERIOD TO MEASURE LOW FREQUENCY-

The method described for one period measurement was less accurate and method described for multiple period measurement was more accurate but it is slow and there is problem to invert period also. Here is a scheme, where reciprocal of measured period is taken by means of standard binary and BCD (binary coded decimals) counters.)

Principle: - We must have four counters, A,B,C, and D numbers. The counter A measures the period of unknown

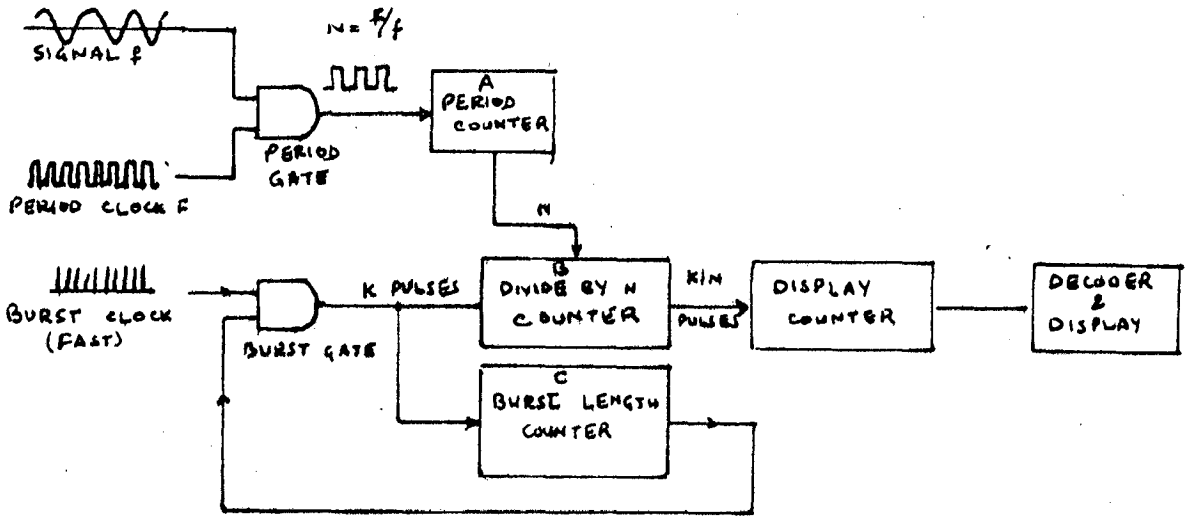


FIG (2.3-a)

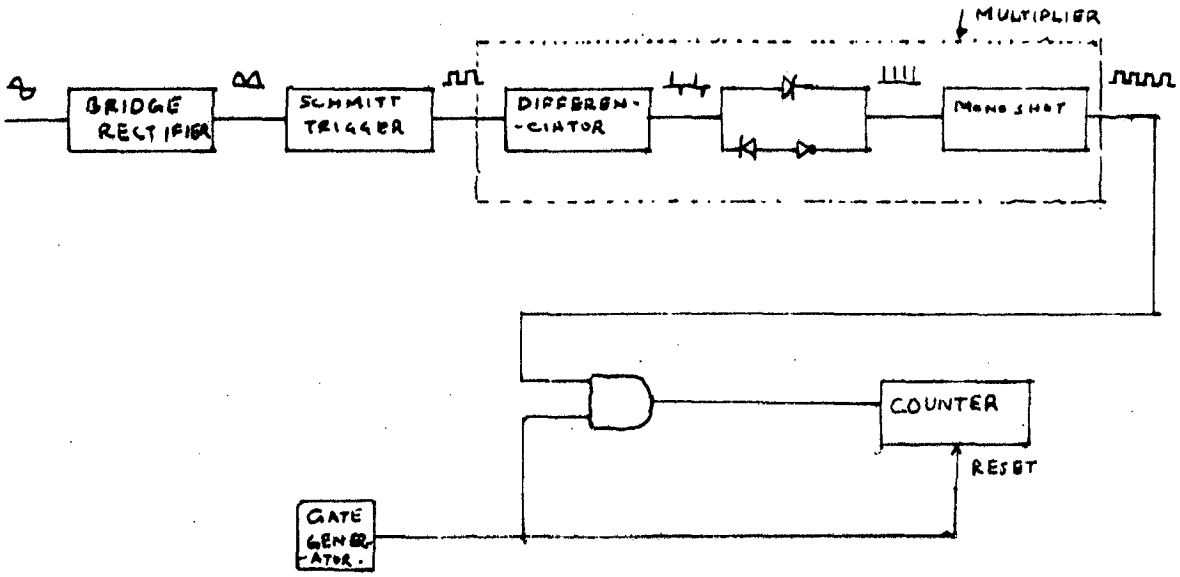


FIG (2.4-a)

signal by counting number of clock pulses, N, during a cycle. The number N programs.counter B which is programmable divide by N unit. Counter C creates a burst with a fixed number of pulses K.

This burst is applied to counter B which computes a number K/N, Thus taking reciprocal of period N and producing a number of pulses proportional to unknown signal frequency. Finally counter D accummulates these pulses to display the frequency.

COMMENTS:

1) Circuit can measure frequency within a cycle of input and hence cycle to cycle variation of input can be observed.

2) There are six steps in functioning of this counter. The The counter is not simple enough.

2.4 A DIGITAL FREQUENCY METER FOR MEASURING LOW FREQUENCY: [4]

Ref. Fig. (2.4.a)

Here is another simple scheme which converts one input cycle into four pulses and therefore keeping the measurement time of signal to one cycle and increasing accuracy to four times. Here sinusoidal input is rectified and then shaped into square pulses with the help of schmitt trigger circuit. Here we will get two square pulses.per input cycle. This square signal is differenciated by differenciator and then all differenciated pulses are made positive. impulses with the help of network of diodes and

invertors. So that, at the output of net work we are left with four positive impulses per input cycle. Each impulse is used to trigger mono shot multivibrator and hence for each impulse, there is one pulse of fixed predetermined duration say, δ and therefore, for every one cycle there are four pulses of duration δ such that $\delta \leq T/4$. In 1(one) sec there are 4 f pulses of duration δ and thus a gate can be made to open for 4 fδ second in 1 sec. If gate is fed a signal of N, H_z frequency. We can have 4 fδN pulses to pass through gate in 1 sec., which can be fed to counter. Reading of the counter can be interpreted directly in terms of input frequency.

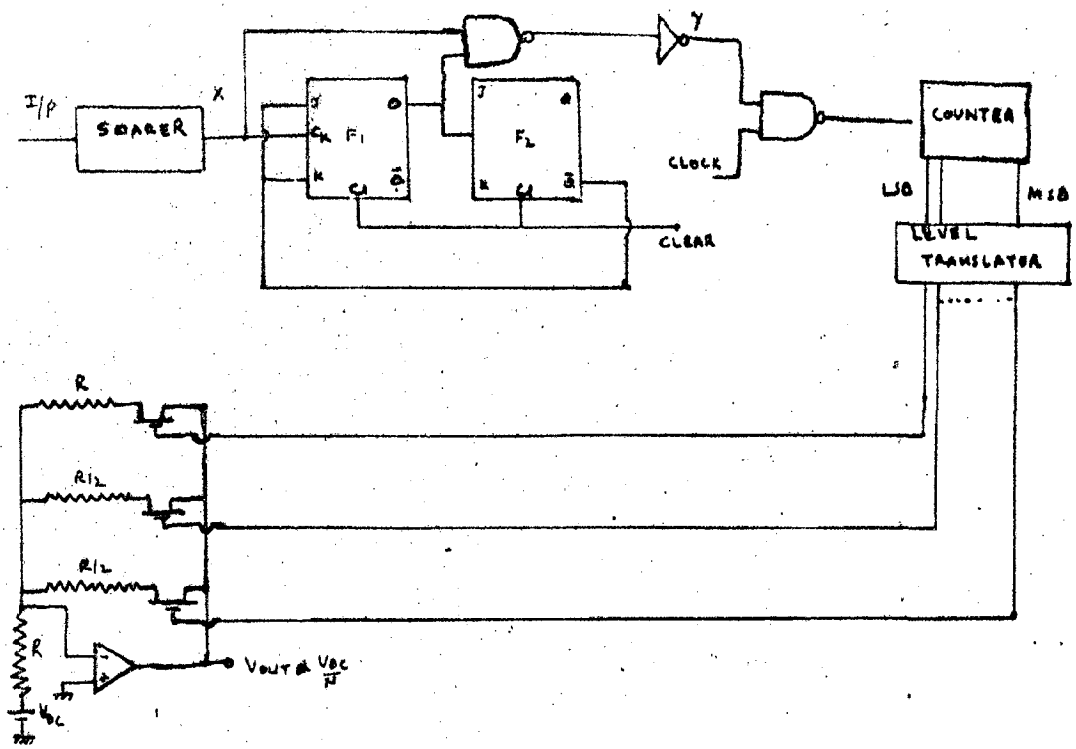
COMMENTS:

1- Accuracy is four times increased without increasing the gate opening period.

2- Accuracy can be further increased if the same frequency multiplier is used to multiply input frequency.

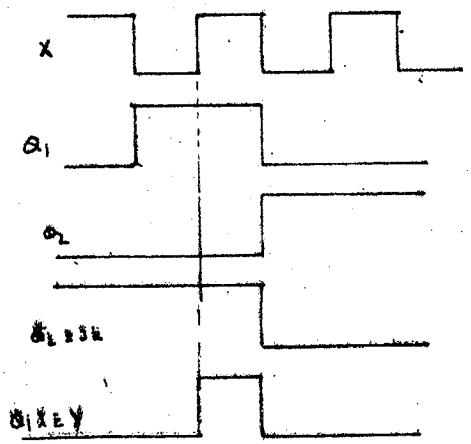
2.5 A MEASUREMENT TECHNIQUE FOR LOW FREQUENCY [5]

One more quite simple method to measure low frequency has been proposed in paper from T.V.R.Murthy and M.K. Kumar. This technique measures the frequency within a cycle of periodic input and is quite useful in quicker measurement for low frequencies.



LOW FREQUENCY MEASUREMENT CIRCUIT

Fig. (2.5-a)



WAVE FORM DIAGRAM AT DIFFERENT POINTS

Fig. (2.5-b)

METHOD:

The major difficulty in measuring low frequency is to obtain reciprocal of period. The proposed method combines period measurement and reciprocating circuit.

The circuit diagram is shown in Fig.(2.5.a) Flip Flop F_1 and F_2 are initially cleared, The input waveform is converted to a square wave by a squarer. Initially J & K of F_1 are set to logic (1). Hence the input at Clock terminal of F_1 will set F_1. The output of F_1 is fed as clock to F_2. The falling edge of Q of F_1 will set F_2 thereby resetting F_1. The output of the inverter can be seen to be a single input pulse.

The signal pulse selected will enable the clock pulses to a counter which will store a number proportional to the period of the input. The counter output controls the ON-OFF states of the switches in the feedback path of the amplifier. If, for example the counter output is 01011, then R, R/2 and R/8 will be connected in parallel, giving an output of VDC/11, which is proportional to frequency, the general the output voltage is VDC/N, where N is decimal equivalent of counter D/P. The output can be fed to a digital voltmeter for the measurement of frequency. Waveform diagrams are given in Fig.(2.5.b). A fair child 3701 mos monolithic six channel switch offers typical ON resistance of 200 Ω and OFF resistance at 200 GΩ providing OFF/ON resistance ratio of 10^9. frequency measurements for a decade range with a resolution of 1 in 100, with an error of less than 1% can be achieved.

CONCLUSION

Here main advantage of this type of circuit is completing measurement within a cycle of input and hence the cycle to cycle variation in input frequency, can be displayed.

2.6 A DIGITAL INSTANTANEOUS FREQUENCY METER [6]

Here is a technique which describes a low frequency meter in which reciprocal of the time elapsed between successive pulses is continuously evaluating digitelly, and then sampled and held at the and of each cycle.

Digital Reciprocal Time Generator.

The digital reciprocal time generator (D.R.T.G.). design is based on implementation of non linear differential equation-

$$\frac{dx}{dt} + Kx^2 = 0 \qquad -- \qquad (2.6.1)$$

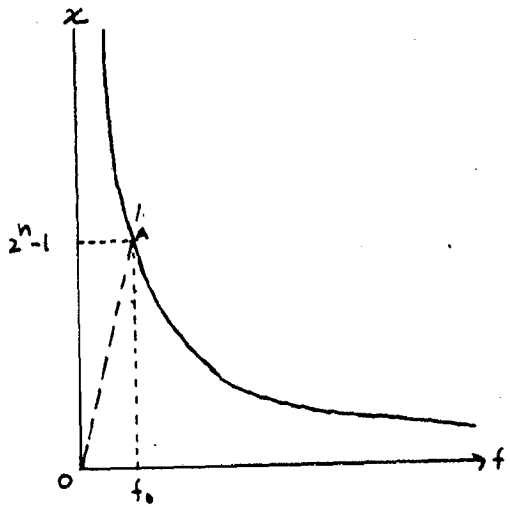
The solution of this is

$$x = \frac{1}{Kt + \frac{1}{x_0}} \qquad -- \qquad (2.6.2)$$

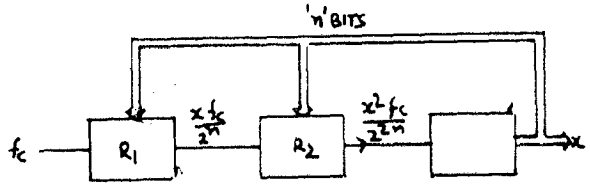
where x_0 is the initial value of $x, > 0$, let $x_0 \rightarrow \infty$

(Fig.2.6a)

$$x = \frac{1}{Kt} \qquad -- \qquad (2.6.3)$$



RECIPROCAL OF TIME CURVE
FIG (2.6-a)



FIG(2.6-B) BASIC DIGITAL RECIPROCAL OF TIME GENERATOR

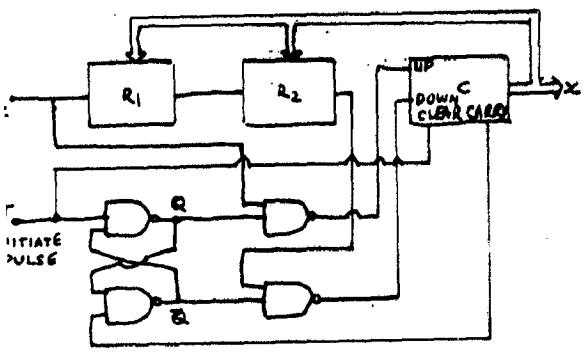


FIG (2-6-C) DIGITAL RECIPROCAL OF TIME GENERATOR WITH UP/DOWN COUNTING

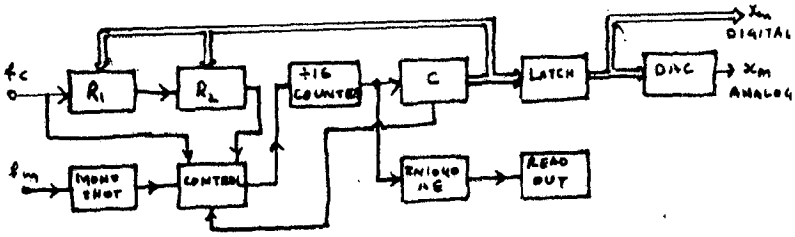


FIG (2.6-d) FUNCTIONAL BLOCK DIAGRAM OF COMPLETE FREQUENCY METER

A pulse rate technique implementations or 2.6.1 using two binary rate multipliers (R_1, R_2) and a down counter (C) is shown in Fig.(2.6.b). The output of a binary rate multiplier is a frequency f_o, the average value of which is proportional to the product of a input frequency f_i and an 'n' bit parallel binary number y as follows:

$$f_o = \frac{y}{2^n} f_i \qquad -- \qquad (2.6.4)$$

Thus for Fig.(2.6-b) we can write

$$\frac{dx}{dt} + \frac{x^2 f_c}{2^{2n}} = 0 \qquad -- \qquad (2.6.5)$$

where f_c dock frequency. Therefore, assuming $x_0 = \infty$

$$x = \frac{2^{2n}}{f_c t} \qquad -- \qquad (2.6.6)$$

Clearly for low values of t, the max. counter output $x = 2^n - 1$ will be exceeded. Therefore, hyperbola must start at (A) in Fig.(2.6.a), and value of t must be ~~or~~ greater than t_o.

For large " n "

$$t_o = \frac{2^{2n}}{(2^n - 1) f_c} = \frac{2^n + 1}{f_c} = \frac{2^n - 1}{f_c} \qquad -- \qquad (2.6.7)$$

Thus starting point A can be app. established by counting up from zero at rate f_c until the counter is full. The

counter "carry " pulse can then be used to initiate the down counting. The corresponding block diagram is shown in Fig.(2.6.8).where the counter C now has an up/down counting facility.

The "initiate" pulse corresponding to t = 0, clears the counter and sets the Q output of Flip Flop HI. Thus the pulse rate f_c is routed to the UP count terminal of the counter via NAND gate. When counter is full, the'carry' pulse causes the flip flop $\bar{Q}$ output to go HI thus, routing the gate output from R_2 to the DOWN count terminal. The hyperbolic down count continues until the next "initiate" pulse occurs and the process is repeated. In practice, in order to prevent the counter from over-flowing and resetting tozero due to propagation delays, a delayed version of the "carry" pulse is used to set all the counters output HI thus ensuring that the down count always starts from the counter full state.

Meter Frequency Range and Accuracy-

Clearly the absolute max.value of measured frequency is given by max. $f_m = \frac{1}{t_c} = \frac{f_c}{2^n}$ - 2.6.8

Theoretically there is no limit, but in practice poor resolution obtaining as the period increases becomes the limiting factor. For n = 12, the theoritical accuracy is ± 0.025% FSD, i.e. ± 1 count. The accuracy expressed as percentage of reading decreases with f_m. Thus for an accuracy better than 0.25 percent of reading, the range of f_m

is from $0.1\ f_c \times 2^{-n}$ to $f_c \times 2^{-n}$.

PERFORMANCE - Theoritical accuracy of this instrument is ± 1 count. To this must be added in-accuracies due to variation in clock frequency. To test the meter highly stable measured and clock signals are required. The accuracy obtained was only ± several counts. This was primarily due to approximate method for setting point A on reciprocal time curve Fig. (2.6-a) The problem was readily over come by including a further 4 bit counter and increasing the clock frequency by a factor of 16. This in effect made the meter a 16 bit device, with the four best significant bits discarded. Tests now showed that the accuracy of the meter was ± 1 count cover the entire range.

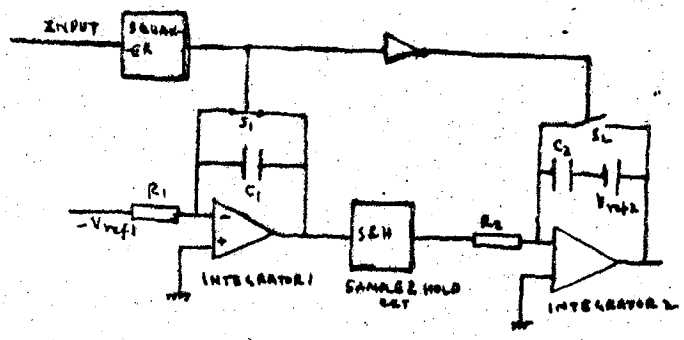
The meter should find application in measurement of frequencies e.g.low shaft speed, physiological pulse rates etc..

2.7 A DUAL SLOPE BASED DIGITAL FREQUENCY METER [7]

The Fig.(2.7-a) shows the basic configuration for digital frequency meter. In first interval, the first integrator I, is allowed to integrate the DC voltage V_{ref}, therefore, the output of this integrator at the and of cycle is given by -

$$V_{01} = \frac{-1}{R_1 C_1} \int_0^T -V_{ref1}\,dt.$$

$$= \frac{V_{ref1}}{R_1 C_1} \qquad -- \quad (2.7.1)$$



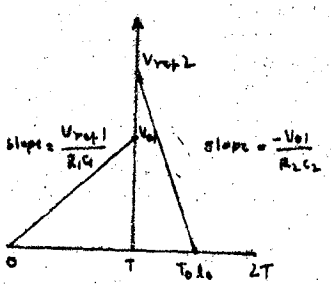


FIG (2.7-a) :: BASIC CONFIGURATION FOR A DUAL SLOPE BASED DIGITAL FREQUENCY METER

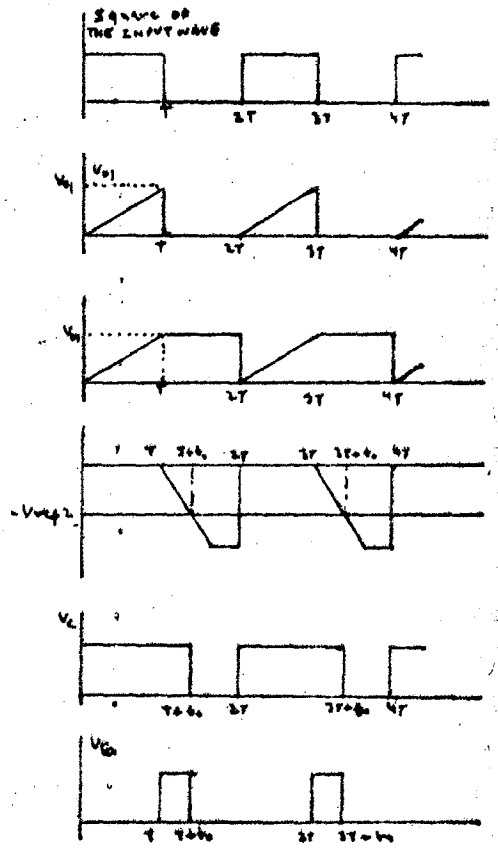


FIG (2.7-c)
WAVEFORMS AT VARIOUS POINTS OF FIG (2.7 b)

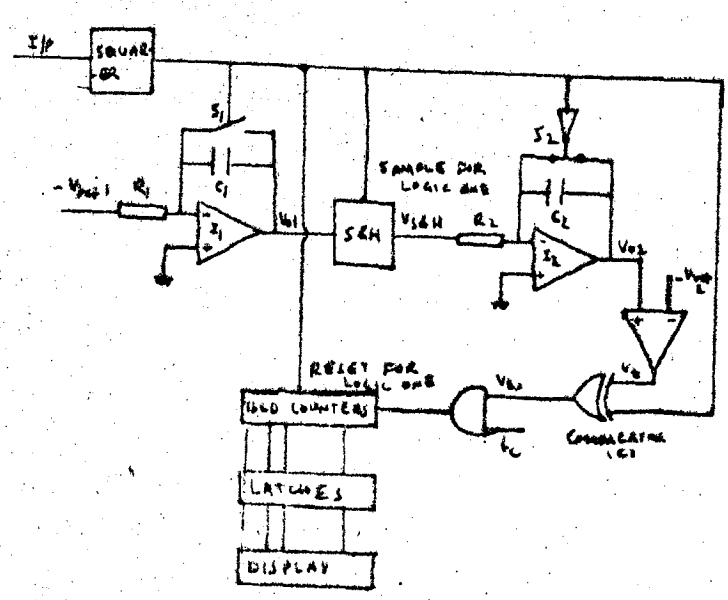


FIG (2.7-b) : COMPLETE CKT DIAGRAM OF THE DIGITAL FREQUENCY METER

Through the second interval, the second integrator is allowed to discharge, starting from another DC voltage V_{ref2}. The input for this integrator is made equal to V_{01}, therefore, the output of the second integrator I_2 is given by-

$$V_{o2} = V_{ref2} - 1/R_2C_2 \int_{T}^{T+t} V_{o1}\,dt.$$

$$= V_{ref2} - \frac{V_{o1}}{R_2C_2}t$$

at $t = to$, $V_{o2} = 0$

Therefore,

$$t_o = \left(\frac{V_{ref2}}{V_{ref1}}\right) R_1C_1R_2C_2 \frac{1}{T}$$

$$= Kf \qquad -- \quad (2.7.2)$$

where $K = \left(\frac{V_{ref\ 2}}{V_{ref1}}\right) R_1C_1R_2C_2$

Using a BCD counter to count through the period (T, T+to) will produce a number given by-

$$N = to\ f_c$$

Where f_c is the clock freq. applied to counter-

$$N = f_c\ Kf. \qquad -- \quad (2.7.3)$$

Therefore, output number of counter is proportional to frequency of input.

RESULTS AND DISCUSSION

The CKt shown in Fig.(2.7.b) uses 741 OP-Amp for comparator, 4 x SN7490 as the four digital decade counter, 8 x SN74175 as the latches, SG173 as single pole single through analog switch and SHM LM-2 as the S/Hckt.

This meter has been tested by measuring frequency between 1-10 Hz. For this range R_1 = 1 M R_2 = 10K, $C_1=C_2=1\mu F$ $V_{ref1} = V_{ref2} = 2.5V$, f_c = 200KHz. This meter shows accuracy of 0.2%.

Range of measurement can be changed by changing R_1C_1 (i.e.time constant) since saturation should not occur in 1st.interval, the lowest frequency that can be measured ($f_{min.}$) is given by-

$$V_{o1} = \frac{1}{R_1C_1} \quad \frac{V_{ref\ 1}}{fmin} = V_{cc}$$

or

$$f_{min} = \frac{1}{R_1C_1} \left(\frac{V_{ref1}}{V_{cc}}\right)$$

Where V_{cc} is supply voltage:

However in 2nd interval, second integrator should reach a value less than V_{ref2} therefore, the highest frequency that can be measured is given by-

$$V_{ref2} = \frac{1}{R_2C_2} V_{o1} \quad \frac{1}{f_{max}}; \quad \text{but } V_{o1} = \frac{1}{R_1C_1} \quad \frac{V_{ref1}}{f_{max}}$$

$$\text{or } f_{max} = \sqrt{\frac{V_{ref1}}{V_{ref2}} \cdot \frac{1}{R_1C_1R_2C_2}}$$

Accuracy of this instrument is mainly dependent on integrators used for dual slope operation. It is a fast digital freq.meter and suitable for measuring low frequency such as those in audio frequency and power frequency range.

2.8 LOW FREQUENCY METER WITH LINEAR READ OUT: [8]

PRINCIPLE: The easiest way to obtain an exponential law from period is to measure the decay of a capacitor. In this circuit, it is achieved by charging, decaying, sampling and recharging a capacitor. Calibration can be achieved by adjusting the FSD pot and then setting the decay preset, then resetting the FSD and so on until the scale gives the correct law. Then, it is only necessary to trim the other range presets.

This circuit is capable of measuring very low frequency and it resolves after one cycle without drifting.

COMMENTS-

1- It can be used for many applications such as pulse rate monitoring.

2- The components marked with an asterisk should be low leakage polycarbonate or tantalum type capacitors.

C H A P T E R - 3

FREQUENCY MULTIPLYING TECHNIQUES-- A REVIEW

The frequency multiplication techniques have been described in many papers. The most common technique, however, is the use of phase lock loops (PLLs). Some of the main techniques are reviewed here as under:

3.1 A METHOD FOR FREQUENCY MULTIPLICATION OF SQUARE WAVE: [9]

PRINCIPLE -

The method of multiplying the frequency by 2 (or powers of 2) is indicated in Fig (3.1-a). The system Fig (3.1-a) comprises a square generator integrator I, amplifier A, comparator C, averager A and an Exclusive OR gate G. The integrator provides an output which is propertional to the time integral of the input square wave signal.

The wave shape at the output of this integrator is triangular as shown in Fig.(3.1-b). This triangular wave is amplified to the required amplitude by the amplifier A., the output of which is the input to comparator C. The other reference input to the comparator is the averaged output of the input square waveform. The two inputs to the exclusive OR Gate appear as shown in Fig.(3.1-a). The output of the Ex-OR gate corresponds to the frequency which is twice the input frequency (without any loss synchronization). The timing diagrams are as shown in Fig.(3.1-b).

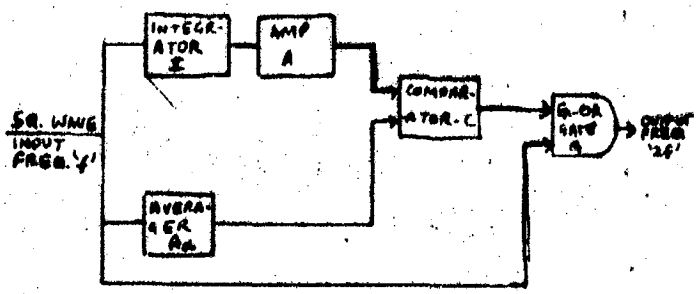


FIG (3.1-a) BLOCK DIAGRAM OF THE FREQUENCY DOUBLER

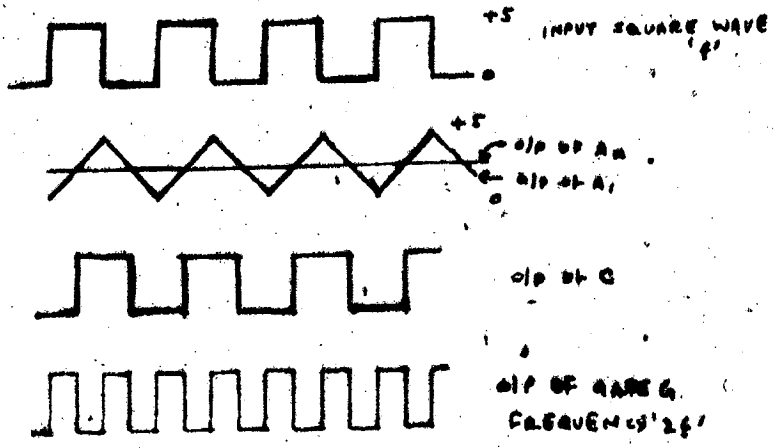


FIG (3.1-b) TIMING DIAGRAMS OF THE FREQUENCY DOUBLER

COMMENTS:

1) If input is sinusoisdal instead of square wave, a ∅ ZCD will have to be used to provide square wave for the CKt.

2) To multiply frequency by 2, if triangular wave input at comparator is made to vary from -3V to +3 V, then the reference voltage to the comparator is not required, if (reference point) may be earthed.

3) For satisfactory control over pulse width, the reference voltage in both the circuits may be derived from a dc voltage (A potentio meter adjust is preferable.).

4) This principle may be used for multiplying frequency by any number, subject of course to practical limitations such as those imposed by IC elements particularly integrator.

3.2 FREQUENCY MULTIPLIER USES COMBINATIONAL LOGIC [10]

Relying on a technique that uses digital logic rather than high speed system clocks or non linear generators to perform frequency multiplication, these circuits derive square wave with an O/P frequency of up to four times that of the input signal.

Since the frequency doubler circuits are relatively simple and well known configurations exists, the logic technique is shown in Fig.(3.2-a) for frequency tripler. For frequency to be tripled input should travel three full cycles or six-half cycles (represented by states (101010) during the time of one input cycle (represented by 111000) at V. Thus the circuit must detect six different logic sta-

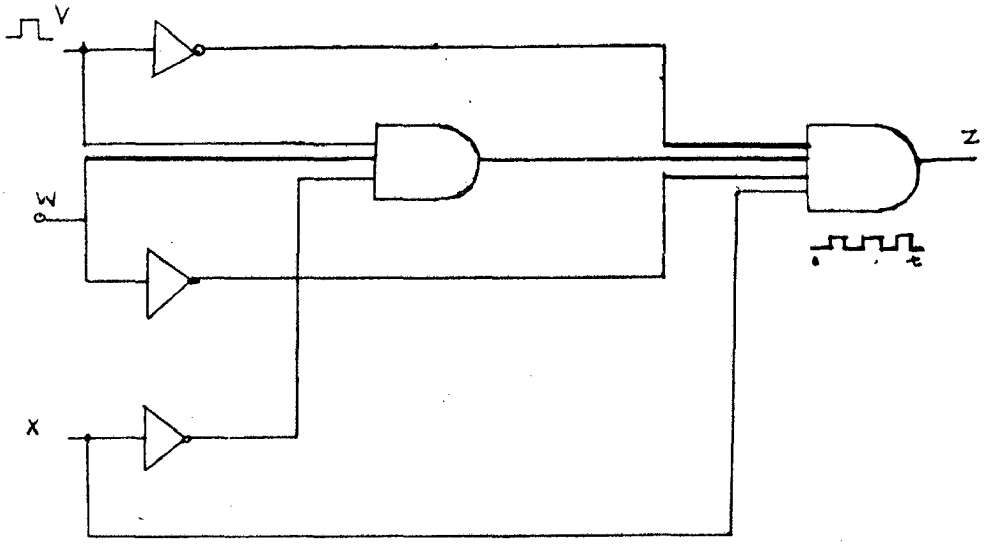


FIG. (3.2.a)

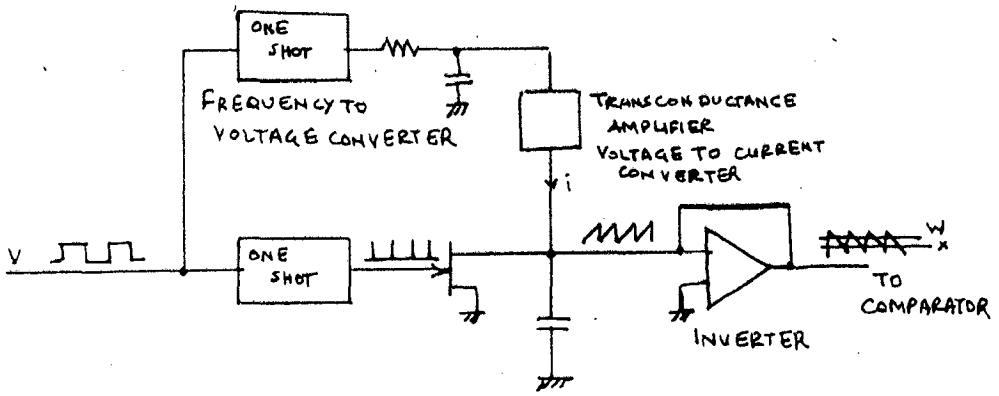


FIG (3.2.b)

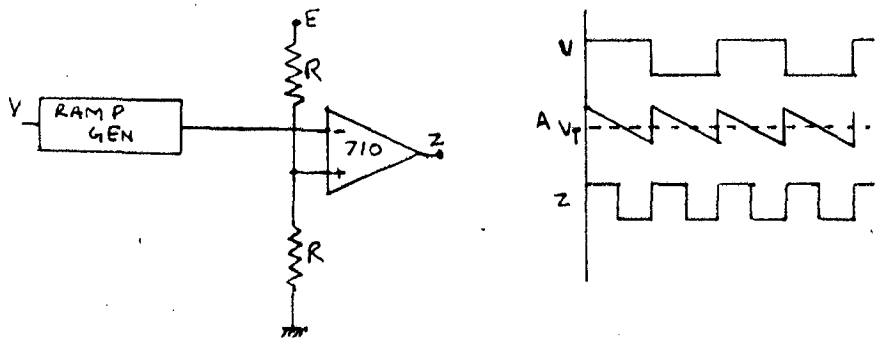


FIG (3.2.c)

tes, and so a minimum of three input variables V, W and X, is required.

Note, however, that the input signal at port V is the only waveform available, and therefore, signals W and X whose logic states for a particular V are not yet known, must be derived from V itself. The particular values of W and X may be assigned to the truth table once it is realized that that the duty cycle of the three input variables are different and that the logic states of the dependent variables, W and X, must change at a faster rate than the independent variable, V. Once the logic states are assigned, the Boolean equation may be determined and the CKt synthesized with simple logic gates. Although several combinations of W and X may be assigned to a given V, the end result should be virtually the same in the Boolean Expression. However, it is important to assign the logic 1 states to W and X. Before the 0 states are assigned to them, because variables W and X not only change with the state of V but also vary with time when V is constant, as shown. Therefore, W and X can't be derived directly from V in the digital domain. However, a negative going ramp voltage whose sweep rate is equal to twice the input frequency can with the aid of Op-Amp. threshold detectors, synthesize the digital signals required at W and X for the doubler, quatripler, quadrupler etc. (Fig. 3.1-c).

COMMENTS-

There are several ways to generate the negative ramp voltage required, many of them constructed with multivibrators and Op-Amps.

The use of linear ramp (as shown in Fig. (3.2-b) allows easy determination of the threshold levels that must be detected in order to switch the logic elements at the proper times. Generally the number of comparator in the ckt will be equal to N-1, where N is multiplication factor. Whose max.practical value is 8. The threshold voltage will be equally spaced if a linear ramp is used each voltage being equal to ME/N, where M is the comparator number and E is supply voltage:

3.3 FREQUENCY MULTIPLICATION USING FETS [11]

This method is based around the nonlinearities of a matched FETpair, involves forcing a ckt on the verge of regeneration into oscillation by injection of the I/P signal.

Here is a scheme for frequency multiplication using FET. Here positive feedback is applied Via two similar b and pass filters centred at the desired output frequency (K (W) in fig.(3.3-a)] If the input signal is square wave, then the modulated collector current of transistor Q_1 is represented by the series:

$$I_{ac} = G_m \sum h_n e^{jnwt} \qquad n = 1,3,5 \qquad \text{-- (3.3.1)}$$

Where G_m is the trans-conductance of the bipolar transistor Q_1. Since the gate sourcevoltage is related to the root of the drain current in the junction f.e.t, the change

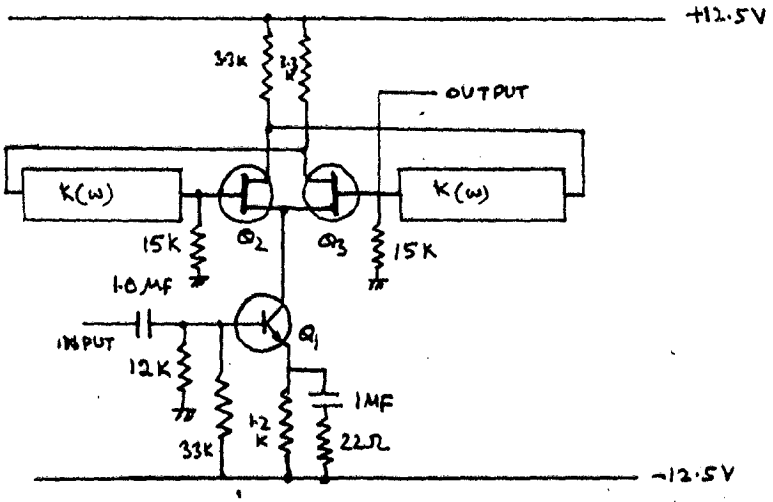


FIG (3-3 a) CIRCUIT SCHEMATIC OF MULTIPLIER

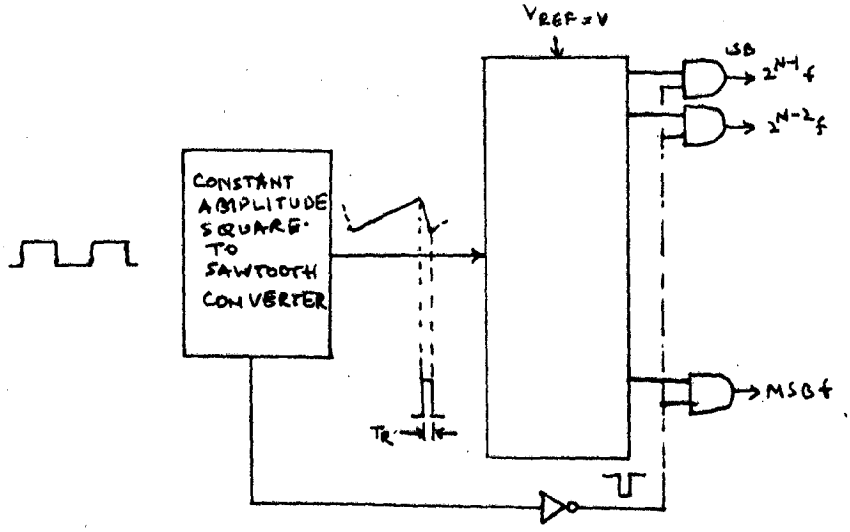


FIG (3-4-a) JAMMING CIRCUIT DURING RESET TIME

in the common source voltage V may be represented by a Taylor series expanded about the d.c. biasing current of the form -

$$U = AI_{ac} + BI_{ac}^2 + CI_{ac}^3 1 \qquad -- (3.3.2)$$

Where A, B, C are related to the 1st., 2nd and 3rd. order derivatives, the higher order terms being ignored. Substitution of equ.(3.3.1) into the above relationship yields-

$$U = \frac{AG_M}{2} \sum h_n e^{jn\omega t} + \frac{BG^2 M}{4} \left[\sum h_n e^{jn\omega t}\right]^2 + \frac{CG^3 M}{8} \left[\sum h_n e^{jn\omega t}\right]^3 \qquad n = 1,3,5,7$$

$$= \sum a_m e^{jm\omega t} \qquad m = 0,1,2 .. \qquad -- (3.3.3)$$

It is clear that, although the input signal contains only odd harmonics, both even and odd harmonics are present at the common source point. Expension of equation (3.3.3) shows that the even components are only generated by the squared term, while the odd components are produced by the linear and cubic terms. Note that each component a_m at the frequency $m\omega$ is a series in which there are contributions from one or more of the three terms.

Suitable manipulation of the mesh equations for the ckt leads to a condition for regeneration at the O/P frequency $m\omega$, as given in (3.3.4).

$$1 = \left\{ g_m + \tfrac{1}{2} D(a_2 m + a_0) \right\} K(\omega) R_L \qquad -- (3.3.4)$$

Where D is a constant and g_m is the trans-conductance of thef.e.t. If the gain of the two filters is adjusted simultaneously, to a value just below the threshold of oscillation, in the absence of an input signal, then the application of an input signal will force the ckt into regeneration, due to the contribution of the a_2m and a_0 terms in equation (3.3.4). since the input signal contains odd harmonies of the input frequency, regeneration at odd multiples is further aided by the amplifying action of these input signal components, while regeneration at even multiples occurs only because of the variations in trans-conductance caused by the presence of the input signal. Larger output signals should thus be obtained for odd multiples of the input frequency due to this amplifying action within the oscillator.

COMMENTS:-

1) A sinusoidal frequency multiplier, capable of operation at large multiples of the input frequency, has been constructed using the square low characteristics of a differential f.e.t.pair. As well as the advantage of sinusoidal output, high multiplication ratios and low jitter concontent, the ckt also offers high input sensitivities e.g. the multiplier has been operated at signal levels as low as 5 mV(p-p).

2) Examination of the condition for regeneration shows that this excitation threshold may be reduced even further by selecting matched f.e.t.s with low pinch off voltages.

3) The synchronization band width of the ckt depends strongly on the characteristics of the filters. A larger synchronizing Band width may be obtained by use of wider pass band higher selectivity filters, although this is not recommended for higher multiplies where two higher order harmonics are closely spaced in the frequency domain.

4) Demerit of the ckt is that, in the lock range phase of O/P depends on the I/P frequency. This is primarily due to the phase variations in the filter, as the required multiple deviates from the centre frequency, of the filters. Filter designs where phase variations in the pass band are minimised may be used to construct a multipliers where both frequency and phase remain synchronized to the I/P over its tracking range.

3.4 A SYNCHRONIZED BROAD BAND SQUARE WAVE FREQUENCY MULTIPLIER [12]

Here a circuit is described which produces simultaneous output square wave whose frequencies are 2^{i-1} ($1 \leq i \leq N$) times higher than the frequency of the original clock signal and are synchronized with it.

PRINCIPLE: Pl. ref. Fig. (3.4-a)

The input square wave of frequency f is first converted into a constant amplitude saw-tooth of the same frequency. This sawtooth is then fed into a comparator type (no clock) A/D converter. Each time the ramp is generated the MSB output changes state once at the mid time and once at the end time period to produce a symmetrical square wave of the

same frequency f as the input wave.

The (MSB-1) output changes state at each quarter time period to produce a symmetrical square wave of frequency, 2f. Thus N simultaneous output signals are generated each having a frequency 2^{i-1} ($1 \leq i \leq N$) times higher then incoming signal.

A finite duration reset pulse available from constant amplitude sawtooth wave generator is used as the jamming signal to eliminate undesirable change of states at the O/P of the A/D converter during the finite time: It is to be noted that reset time t_R should be smaller than LSB O/P (period of highest frequency output).

COMMENTS:

1) To speed up multiplication, sawtooth generator can be replaced by triangular, wave generator.(Fig.3.4-b), Advantage of triangular wave is that no rapid transition is required from the maximum to/the minimum value. When the triangular wave reaches its maximum value the input square wave (50% duty cycle)inverts the O/P states of the A/D converter. The result is same as if the ramp had been reset to zero with advantage of N bit A/D converter, the maximum frequency i.e.maximum frequency is increased or infact doubled.

2) By adding divide by N-counter at the proper O/P of the A/D converter some unusual multiplication factors can be obtained e.g.a divide by 3 counter is inserted on the

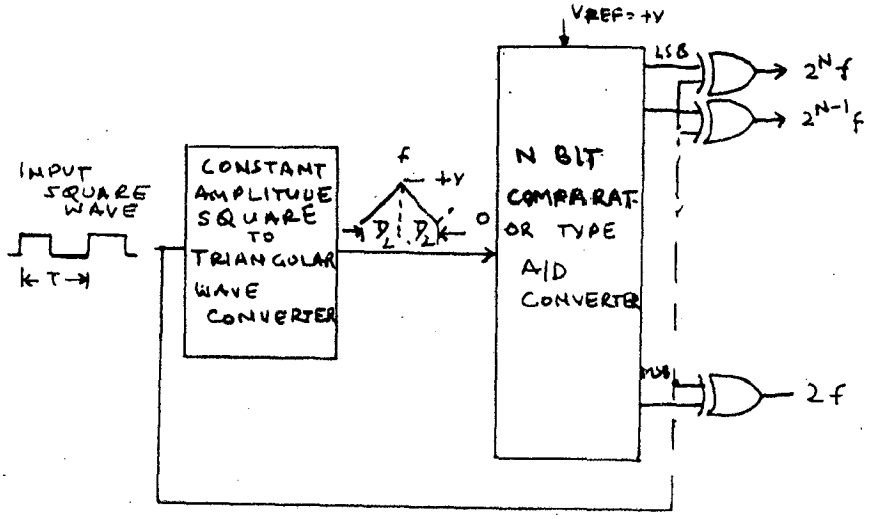


FIG (3.4.b) HIGH SPEED FREQUENCY MULTIPLIER

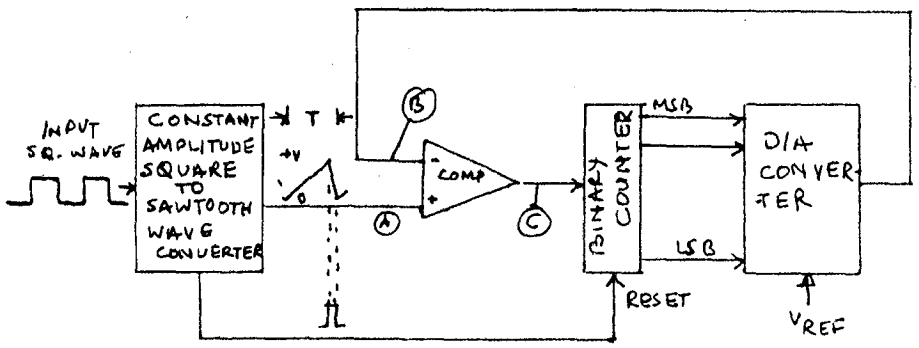


FIG (3.5.a) BLOCK DIAGRAM OF THE NEW FREQUENCY MULTIPLIER

multiply by 8 O/P. The frequency at the O/P of the counter is now 8/3 times that of input signal.

-3.5 -

MODIFICATION [13]

Comparator type A/D converter is not a common building block. This difficulty can be eliminated if we use D/A converter instead of A/D converter, i.e. The input square wave of frequency f is first transformed into sawtooth wave form of frequency f from the constant amplitude square to sawtooth wave converter as in Fig.(3.4-a). This sawtooth is then fed to comparator (Non-converting input) Comparator O/P is fed to Binary counters and outputs of binary counters are fed to D/A converters. The O/P of D/A converter is fed as feed-back signal to inverting input of comparator.(Fig.3.5-a).

"****"

3.6 A SIMPLE DESIGN FOR A DIGITAL PROGRAMMABLE- FREQUENCY-MULTIPLIER [14]

Here frequency multiplication is carried out by multiplying counters IC_5, IC_6, IC_7 (SN 74192) at the upper part and by the control counters IC_2, IC_3, IC4(SN7473) and SN-74192) at the lower part. The multiplying factor n can take values from 2 to 99 and can be extended to any value if the specification of the elements allow.

SEQUENCE OF OPERATION:

1- Frequency to be multiplied (f_s) is generated by the square wave generator. The leading edge of the square-wave triggers a one shot multivibrator, IC_1 (SN 74123). A very narrow negative pulse is produced by the O/P of Q ($P_{in}4$) to initiate the ckt operation. Simultaneously three actions occur.

(a) The O/P IC_2 from $P_{in}9$ is initiated from reset '0 ' to logic '1' state by this negative clock pulse, which can be used as a synchronizing signal and a check pulse for every cycle.

(b) The multiplying counters IC_5, IC_6, IC_7 are loaded with this negative pulse as they are previously preset to a value of the pins 9, 10, 1 and 15 in each decade counter. This preset value can be expressed as $T_s/2n$ where T_s is

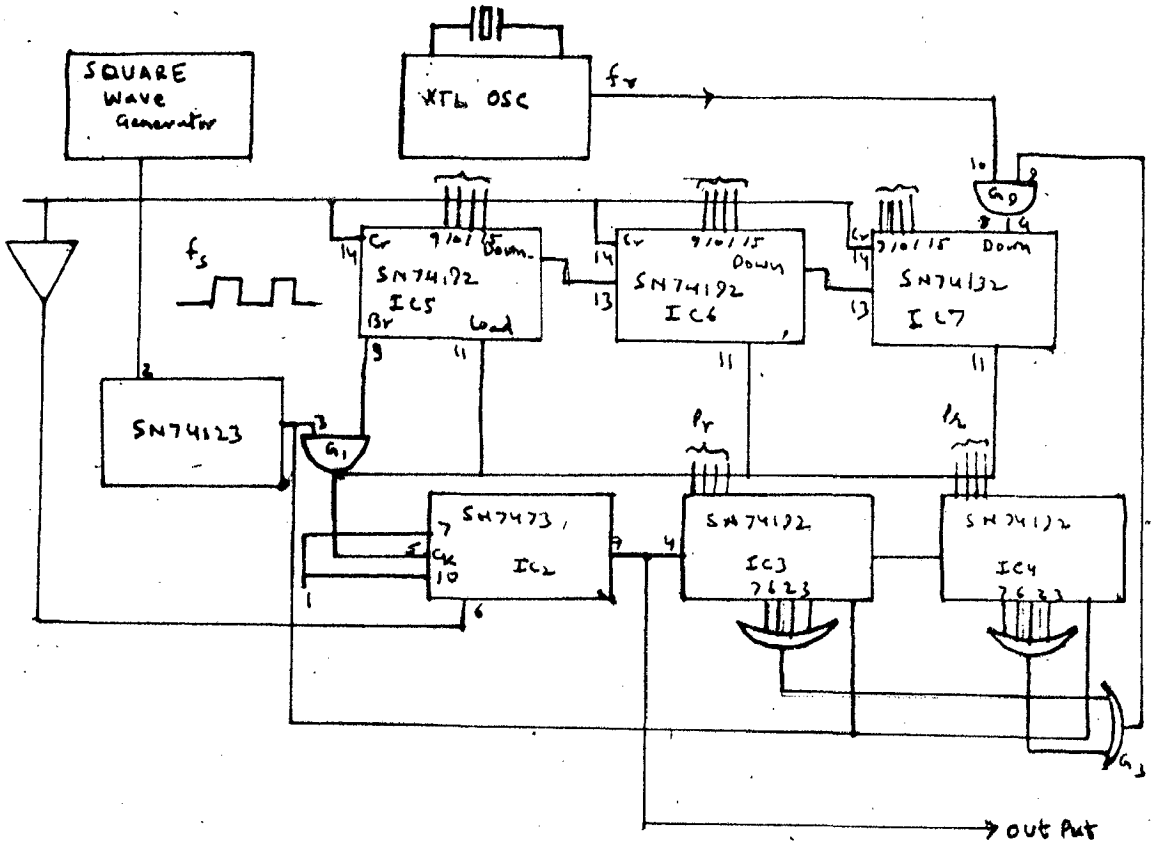


FIG. (3.6.a)

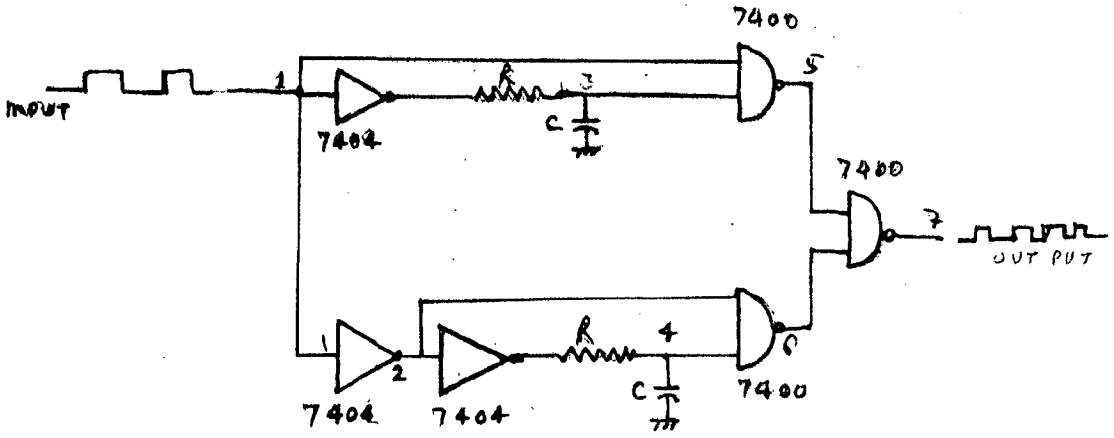


FIG (3.7.a) Simple Frequency Doubler

the period of the input frequency f_s and n, the factor of the desired multiplication.

(c) The control counters IC_2, IC_3, and IC_4 are also loaded with this signal to the previously preset value of n, where n has the same value as above.

2- As soon as the multiplying counters and control counters are loaded the multiplying counter begins to count down from the present value to zero. Since at this moment the AND gate G_2 is enabled by the OR gate G_3.

3- When the contents of the decade counters of the multiplying counter reach/zero, a negative pulse is produced by the O/P borrow (B_r) from the last stage of the decade counter. The O/P IC_2 from pin 9 is again changed from logic '1' to logic '0' state by this negative pulse, which, however, only loads the multiplying counter.

4- The contents of the control counters IC_3 and IC_4 will be decreased by one of the output IC_2 completes one cycle. These processes will be repeated until the contents of the control counters reach zero, when the/output IC_2 completes n cycles. Then gate G_2 is inhibited by gate G_3 since, the O/P G_3 is logic '0' as soon as the contents of all decade counters are zero.

5- The operation of the ckt is restarted by the input of a/synchronous pulse which is produced by the leading edge of the source square wave. Even if, this synchronous signal is not coincident with the inhibited action, the inhibited state will be

held until the synchronous pulse occurs. Therefore, there is no accumulated error in this system.

COMMENTS-

1) Reference frequency should be generated from crystal oscillator to get good accuracy.

2) Reference frequency (f_r) should be sufficiently higher than f_s. Higher the frequency f_r the greater the accuracy of O/P frequency f_o, Generally, $f_r \geq 100\, f_s$.

3) When the input square wave has disappeared, this system is always inhibited by Gate G_2 and no output wave form is produced from IC_2.

4) The multiplication factor n can take non integral values, such as n = 1.5, 2.5.

5) The elements of the ckt are simple and cheap, no linear devices are involved.

6) The hardware of the ckt does not change if n is changed.

7) The preset values for the multiplier n are easy and can be programmable. No reference voltages are required.

8) The errors of the O/P wave forms are not accummulated. because a Synchronizing signal is produced in every cycle to check and initiate and multiplyin frequency.

9) The system can be extended by any number of multipliers subject to practical limitation such as the frequency response imposed by the I.C. elements.

3.7 A SIMPLE DIGITAL 2^n FREQUENCY MULTIPLIER [15]

PRINCIPLE -

When the pulse input at point 1 is in the LOW state, the capacitor C at point 3 gets charged through a resistors R to HIGH level and the point 5 continues to be at logic level HIGH. As the pulse input under-goes transition from LOW to HIGH level, the point 5 changes to logic level LOW, meanwhile the capacitor C at point 3 starts discharging through resistor R, and as soon as potential at point 3 reaches VIL which is the maximum voltage level considered as as LOW at the input of TTL devices, point 5 goes to lotic level HIGH. Thus at point 5, a negative pulse of duration corresponding to the discharge time of capacitor C to V_{IL} is produced and the cycle continues. The voltage pulse available at point 2 is 180° out of phase with that at the point 1. A similar sequence of operations produces negative pulse at point 6 but out of phase by 180° with those at point '5'. The output at point 7 is a combination of the pulse produced at point 5, and point 6 but with reversed polarity. Thus the O/P pulses have been produced at the leading as well as at the trailing edge of the input square wave, whereby frequency doubling is achieved. The pulse width and duty cycle of output pulses can be simply controlled by suitably selecting the resistance and capacitance values Fig.(3.7-a). We can obtain upto 50% duty cycle by choosing appropriate values of R and C for any given frequency. For Symmetrical output, R and C should have equal value.

COMMENTS:-

1) Frequency quadrupling can be achieved by feeding the input square wave directly to a frequency doubler, phase shifting the doubler O/P by 90^{0} and combining the phase shifted output with doubler output in an Exclusive- OR gate. By varying R_T and C_T of the monoshot, the phase shift can be set according to $180^{0}/2^{n-1}$ at any desired value. [15]

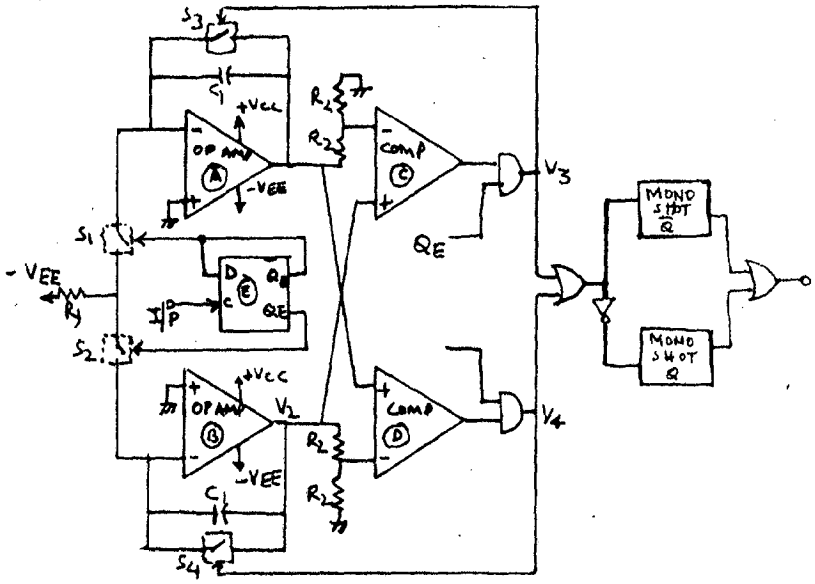
2) Such a multiplier was tested over a frequency range of 1.5 KH_z-10 MH_z with R= 1K(pot); C = 470 PF, monoshot timing resistor R_T = 5 K(Pot) and C_T = 200PF. Output train of pulses of variable duty cycle (upto 50%) were obtained at twice and four times the input signal frequency over this frequency range.

3) RC time constant has to be $\geq T/2^{n+1}$ and RT $C_T \leq T/2^{n}$ where T is the time period of the input square wave. These constraints decide the limit of the operating frequency range of the multiplier.

4) This ckt can operate over a very wide frequency range and upto 50% duty cycle of the output pulses is achieved.

3.8 A FREQUENCY DOUBLER FOR RECTANGULAR INPUT [16]

The main drawback of method described in [15], is that values of R and C should be critical to obtain a square wave O/P from each stage. This restricts use of such multiplier to one single input frequency.



FIG(3.8.a) CIRCUIT SCHEMATIC OF FREQUENCY DOUBLER

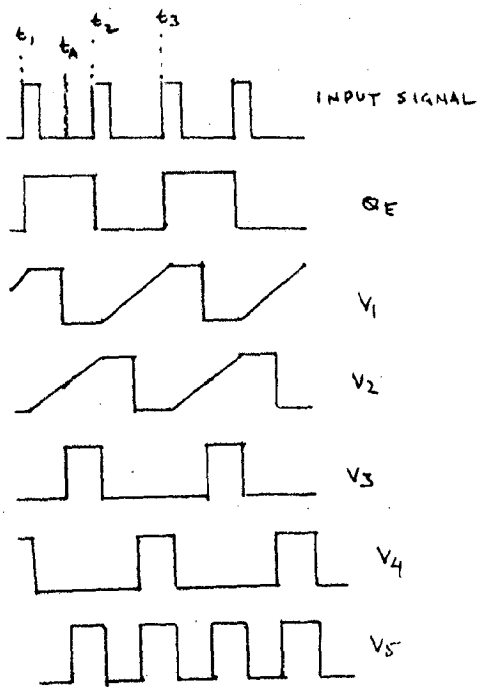


FIG (3.8.b) WAVE FORMS PERTAINING TO OPERATION OF CIRCUIT.

This paper describes frequency doubler which first converts a given rectangular input signal to a square wave whose frequency can then be doubled easily. Hence the difficulty faced in [15] is eliminated.

PRINCIPLE:

The first part of the ckt converts the rectangular input into a square wave Fig.(3.8-a). This part consists of two OP AMP integrators A and B, which alternately measure and store the period information of the input signal.

Referring to Fig.(3.8-b), the interval t_1 to t_2 represents one typical cycle of the input signal, whose period is T. During the interval between t_1 and t_2, the Q O/P of the toggle flip flop E is high and consequently the switch S_1 is opened and S_2 is closed.

At the instant t_1, the O/P voltage V_2 of the integrator B is zero, where-as the O/P V_1 of the integrator A is equal to the voltage integrated during the previous cycle and is given by-

$$V_1(t_1) = \frac{T}{R_1C_1} V_{EE} \qquad -- \qquad (3.8.1)$$

During the interval t_1 to t_2, the voltage V_1 remains constant whereas V_2 increases linearly as given by--

$$V_2(t) = \frac{(t-t_1)}{R_1C_1} V_{EE} \qquad -- \qquad (3.8.2)$$

In the beginning of this cycle V_2 being small, the O/P of the comparator C is low and consequently V_3 and V_5 are

also low. As soon as V_2 becomes more than $V_1/2$, the O/P of the comparator C becomes high, thus making V_5 to go high. The time constant t_A at which this happens is obviously given by (from equation (3.8.1) and (3.8.2):

$$t_A = t_1 + \frac{T}{1} \qquad -- \qquad (3.8.3)$$

In other words t_A is the midpoint in the cycle. It is thus seen that V_5 is low during the first half of the cycle and high, during the second half. Immediately after t_A, the switch S_3 is closed, thus discharging the integrating capacitor of the integrator B.

During the next cycle (the interval t_2 to t_3) the Q O/P of the F/F, E goes low. Consequently, S_2 is opened and S_1 is closed. The voltage V_1 now increases linearly whereas V_2 retains the value integrated during the previous cycle (given by right hand side of equation (3.8.1).During this cycle the comparator D delivers a pulse of width T/2 to V_5.

It is thus seen that the comparators C and D alternately deliver pulses of width T/2 to V_5, thus generating a square wave at a frequency equal to the input signal frequency. The frequency of this square wave is doubled using two monoshots, one triggered by its leading edge and the other by its trailing edge. The O/Ps of the two monoshots are combined in an OR gate to generate the frequency doubled signal. The duty cycle of this signal will be a function of the monoshot's period and the input signal period. This O/P can be converted into a square wave if necessary by

using any frequency doubling techniques; such as described in [157].

COMMENTS:

1) Here values of R and C are not critical.

2) R_1C_1 time constant should be such that the maximum value attained by V_1 and V_2 is below the positive supply voltage even at the lowest frequency of the operation.

3) The maximum speed of operation of the ckt is determined by the (gain X band- width) products of the OP- AMPs and and the sensitivity of the comparators.

4) The duty cycle of the square wave at V_5 can be trimmed by inserting two small variable resistors, one in series with S_1 and the other in series with S_2 (in fact only one of these resistors need be variable. The other can be a fixed resistor with a value equal to mid value of variable resistor). This trimming will compensate for /between the two integrators capacitors and also any mis-match/in the two matched resistors pairs R_2.

5) This type of frequency doubler was fabricated and tested. The OP- AMP used are IC 741 and comparator are IC 710. The switches used are CMOS switches and of CD4016 type. The logic gates and the monoshots are of the standard TTL-type. The time constant of the two integrators was set to around 15 ms. The resistor R_2 were 10 Kr. The ckt was tested in range of 100 H_z- 20 KH_z satisfactorily.

6) This ckt works independently of the frequency and duty cycle of the input signal and does not need critical adjustment of the components. This makes the ckt versatile and useful in a wide range of applications.

7) A 2^n frequency multiplier can be constructed by cascading n such doublers.

3.9. SIMPLE FREQUENCY DOUBLING SCHMITT TRIGGER CKT [17]

(Ref. Fig. (3.9-a)

Here in this circuit voltage comparison and frequency doubling functions are combined in an extremly simple circuit realization. Since only three transistors are required, it can be constructed with a single integrated nPn transistor array, such as the CA3086. With this ckt a sinusoidal input voltage is converted to a digital pulse train with one half the input period; or twice the frequency.

PRINCIPLE:

Here input stage is a full wave rectifier. Transistor T_1 is biased with V_B such that it is saturated. With R_1 and R_2 equal, symmetrical V_{CC} and V_{EE}, and a sinusoidal input V_{IN}, the voltage on collector of T_1, V_A, will be a full wave rectified sine wave. As sinusoidal V_{IN} goes positive, T_1 will be driven further into saturation. If we assume the collector emitter and base-emitter voltages in saturation to be nearly constant, then V_A will be approximately V_{IN}. As V_{IN} goes negative, T_1 will be driven out of saturation and V_A will be approximately the magnitude of V_{IN} since R_1 and R_2 are equal. Thus,

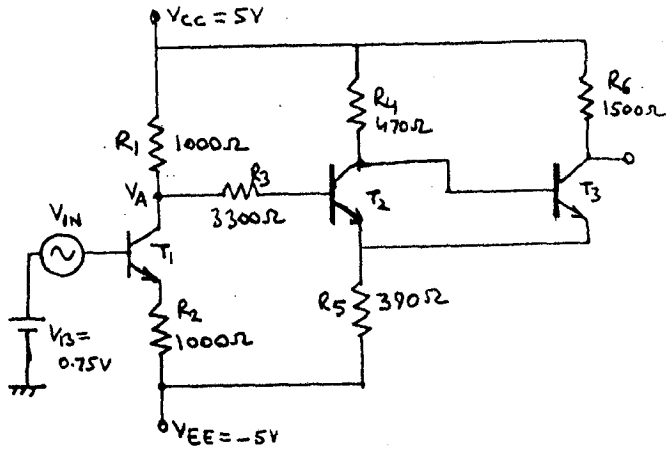


FIG.(3.9.a) FREQUENCY DOUBLING SCHMITT TRIGGER SCHEMATIC.

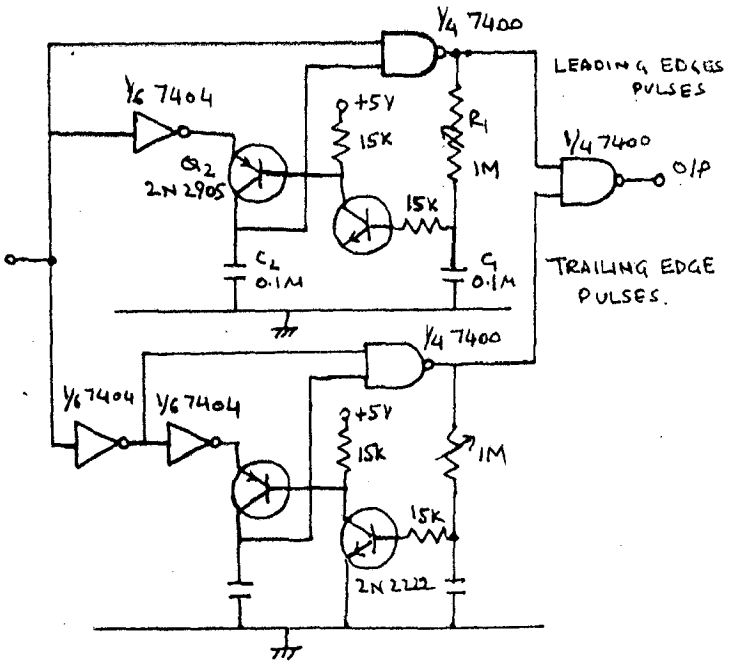


FIG.(3.10.a) CONSTANT DUTY CYCLE DIGITAL FREQUENCY DOUBLER

a full wave rectified sine wave will be developed at V_A. Distortion in the rectified waveform from the ideal due to the variations in V_{BE} and V_{CE} in saturation with input signal amplitude, resistor mismatch, finite β and temperature dependence of function voltage and currents will be present but is not considered significant in this digital application. Transistors T_2 and T_3 form a simple schmitt trigger. Resistors R_4, R_5 and R_6 are selected to yield the desired threshold voltages and hysteresis. For a voltage input V_A less than either threshold, T_2 will be cut off and T_3 will be operated in the forward active region or in saturation such that the low output state is TTL voltage compatible with V_{OUT} 0.4V. As the voltage V_A increases above the upper threshold, T_2 is turned on to the extent that T_3 is cut off, and V_{OUT} goes to its high state, V_{CC}. The upper threshold is approximately-

$$V_{TH_U} = V_{EE} + V_{BE} + \frac{(V_{CC}-V_{EE})R_6}{R_6 \frac{R_4R_5}{R_4+R_5}} \qquad -- \qquad (3.9.1)$$

As the input continues through its cycle and decreases below the upper threshold, T_2 is again cut off and T_3 saturated when the lower threshold is encountered. The lower threshold is approximately -

$$V_{TH_L} = \frac{V_{CC}R_6 + V_{EE}R_4}{R_4 + R_6} + V_{BE} \qquad -- \qquad (3.9.2)$$

Thus this simple three transistor circuit can develop a TTL voltage compatible digital pulse train with twice the frequency of the input.

COMMENTS:-

Choosing power supply voltage and resistor values 10% shown in Fig.(3.9-a), we obtain measured threshold voltages of about 0.6V and 0.9V and a TTL compatible output voltage swing of 0-5V. Typical wave forms are shown in Fig.(3.8-b) The centre wave form is the 2.4V peak to peak 2.5 KH_z sinusoidal input, V_{IN}, The top trace is 1.1V peak-peak rectified waveform V_A. The bottom trace shows the approximately 0V- 5V, 5 KH_z O/P pulse train.

Thus this technique for developing a doubled pulse rate is effective and completely integrable in standard bipolar technologies. It can also be realized with a single integrated npn transistor array since only three transistors are required.

3.10 A SIMPLE CONSTANT-DUTY- CYCLE DIGITAL FREQUENCY DOUBLER [18]

PRINCIPLE - (3.10-a)

It consists of two units. The upper unit produces output pulses at the leading edges of the input pulses and the lower unit at the trailing edges. These two output pulse trains are then combined in a NAND gate. The duty cycle of the output pulses can be easily set at any desired value upto 50% by properly adjusting the potentiometers R_1.

COMMENTS:

1- Such frequency doubler modules having a constant duty cycle over large frequency range can be easily cascaded to obtain a higher order of frequency multiplication.

2- The transistor types and other values used are not critical.

3.11 A SYNCHRONIZED FREQUENCY MULTIPLIER FOR SQUARE WAVES [19]

PRINCIPLE -

The monoshot pulse generator is adjusted for a quarter wave delay that given an O/P which is double the input frequency. The input is generated from 555 timer using as an astable multivibrator having a frequency of 1 KH_z and the tuning components carefully choosen to obtain a duty cycle of 50%.

The scheme consists of square wave generator, an inverter (using a silicon npn transistor) two RC differenciating networks, an OR gate (Using two silicon diodes) and a monoshot pulse generator having a pulse width of T/4 where T is the period of the input square wave. The time constant of each R-C differentiating network should be much smaller than T. The O/P of the OR Gate is negative going trigger pulses (spikes) with a period of T/2 as shown in Fig. (3.11-b) and these are used as the external trigger pulse required to operate the monoshot pulse generator. The letter

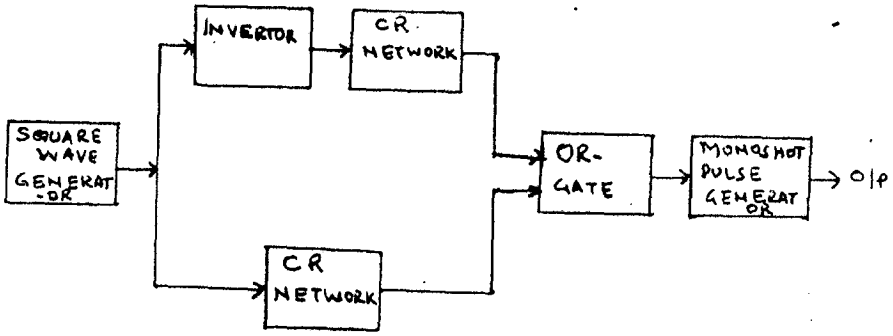


FIG.(3.11.a) BLOCK DIAGRAM OF THE FREQUENCY DOUBLER

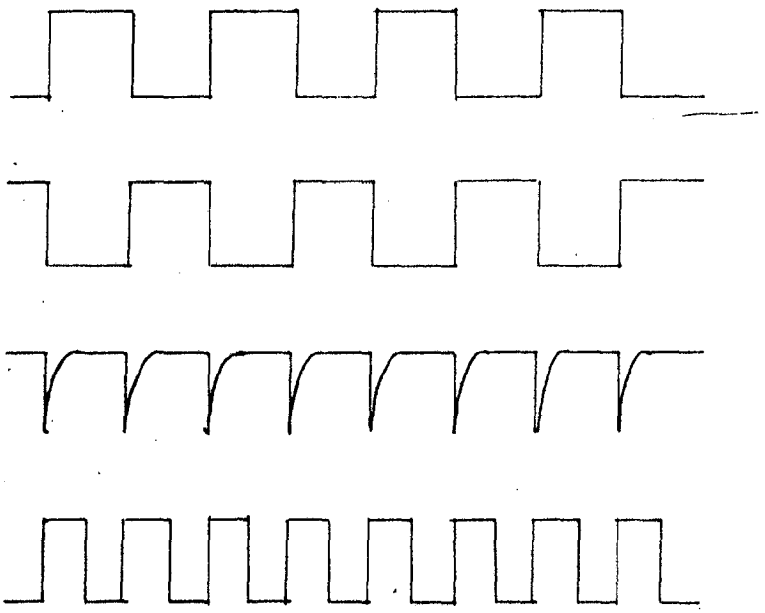


FIG.(3.11.b) TIMING DIAGRAMS OF THE FREQUENCY DOUBLER

has a square wave O/P with a frequency which is double the input frequency (Without loss of Synchronizations).Higher multiplication can also be achieved subject to the frequency limitations imposed by the 555 timer.

COMMENTS:-

1) The circuits were tested for input frequency of $1KH_z$.

2) The circuits were tested as doubler and tripler and satisfactory results were achieved.

[20]

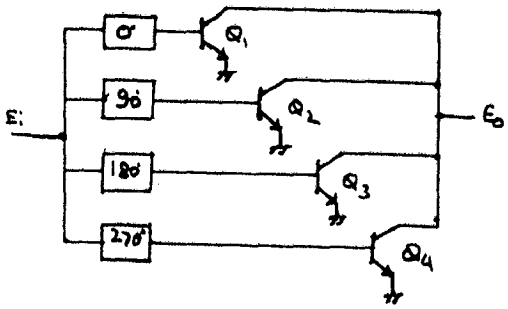
3.12 PHASE SHIFTER SIMPLIFY FREQUENCY MULTIPLIER DESIGN

PRINCIPLE - (Ref. FIG. 3.12-a)

The phase shift frequency multipliers, unlike conventional multipliers can produce a spectrally pure O/P without filtering. However, by using wide band phasedifference network for phase splitting, frequency independent multipliers over many octaves may be obtained. The Fig.(3.12-a) shows sine wave frequency is multiplied/N timesby dividing input into N different phases that are equally spaced through 360^{o}.These N phase drive N class C transistrs whose outputs are combined to deliver a pulse every $360^{o}/N$.The use of N transistors allows the input power to the circuit to be N times as high as without saturating the transistors.

COMMENTS -

1) The phase shift frequency multipliers are superior to conventional multipliers at high frequencies in subharmonic suppression. A high frequency version of this



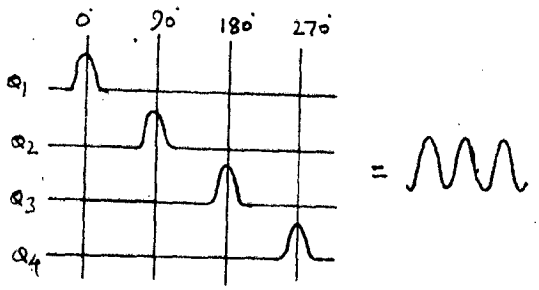


FIG.(3.12.a) QUADRUPLER.

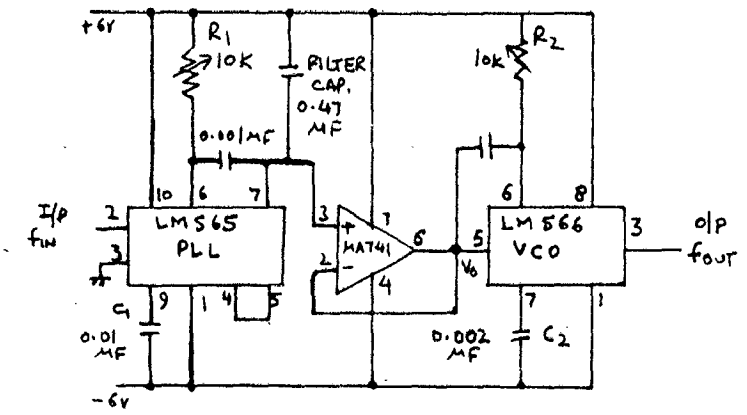


FIG.(3.13.a) FRACTIOAL FREQ. MULTIPLIER.

type of multiplier and quadrupler has also been given in [20]

2) An interesting property of this type of net-work is that when rectances are made equal, the phase shift between the input and output ports will always be 90^0, regardless of the value of R. This property allows both amplitude (varying R) and phase (varying L OR C) control.

3) The inductance L is created by the primary winding of T_1, the secondary windings delivers a 90^0 and 270^0 phase shift of Q_1 and Q_2 respectively. The 0^0 and 180^0 phase shifts are provided by T_2 to Q_3 and Q_4.

4) In addition, the L-P_i network at the O/P provides an optimum match to a 50r load and a little attenuation of subharmonics. This multiplier, unlike conventional ones, is capable of suppressing subharmonies and therefore, does not require O/P filtering.

5) A spectrum analyser display showed that the second and third harmonies could easily be reduced by more than 50 decibels below the desired fourth harmonies.

3.13 JOINING A PLL AND VCO FORMS PRACTIONAL FREQUENCY MULTIPLIER: [21]

The conventional multiplication ckts employing PLL use either harmonic locking or a frequency divider between its VCO and phase comparator. Thus the O/P is only an integer multiple of the input. As a result if certain O/P frequency is desired, the input frequency must be carefully selected. Such exact choosing is no longer needed because this circuit

can multiply pulse frequencies by any real number through the simple adjustment of two potentiometers. In addition, it operates over a wide input frequency range and has a more stable O/P than do conventional multipliers.

PRINCIPLE-

The design combines a PLL frequency to voltage converter and an external VCO for pulse frequency multiplication.

A PLL connected as a frequency demodulator, generates voltage Vd that is related to the input frequency by $V_d = Kf_{in}$, where K is a constant and fin is the frequency of the input signal. In addition, the input frequency of the internal VCO (contained in the PLL) is $f_{in} = \frac{V_d}{VR_1C_1}$ where R_1 and C_1 are the frequency determining components of the internal VCO and V is the supply voltage.

Demodulated voltage V_d is fed to the control voltage input of the external VCO whose O/P frequency is $f_o = V_d/VR_2C_2$ where R_2, C_2 are frequency determining components of the external VCO. Solving for the O/P frequency, $f_o = f_{in} R_1C_1/R_2C_2$ and thus $n = \frac{R_1C_1}{R_2C_2}$. The multiplication factor n is only decided by the externally connected resistors and capacitors and therefore can be choosen for any value.

The ckt uses National Semi-conductor's general Purpose LM565 and LM 566 as PLL and VCO respectively. OP AMp µA741 serves as buffers between the two.

COMMENTS -

1) Circuit with multiplication factor of 6.15 is tested for input frequency in the range of 2-6 KH_z.

2) For stable operation R_1 and C_1 should be selected according to input frequency and R_2C_2 should be choosen to general desired multiplication factor.

3.14 A SYNCHRONOUS FREQUENCY MULTIPLIER USING PLL [22]

PRINCIPLE-

PLL are the lower cost approach to frequency multiplication using a divide by n counter in the feedback part as shown in figure (3.14-a). In this arrangement, there is usually a phase difference between inputs 1 and 2 of the PLL. This difference does not have long time stability and may change because of the amplitude and the frequency variation of the input signal. That is why the PLL does not provide a synchronized O/P in this system.

To obtain a synchronized O/P one can consider a system like in Fig.(3.14-b). This uses a second counter equal to first one in the feedback loop and a pulser which produces pulse at the negative going edge of the input square wave.

The operation of the ckt can be explained as follows w.r. to Fig.(3.14-C). Let t_1 is the instant when a_1, b_1, c_1 all go to negative simultaneously and t_2 where a_2, b_2, c_2 all go to negative simultaneously by the reset pulse coming from the pulser. As can be seen, t_2 is always closer than t_1 to the negative going edge of the input with an error T_o. which is the period

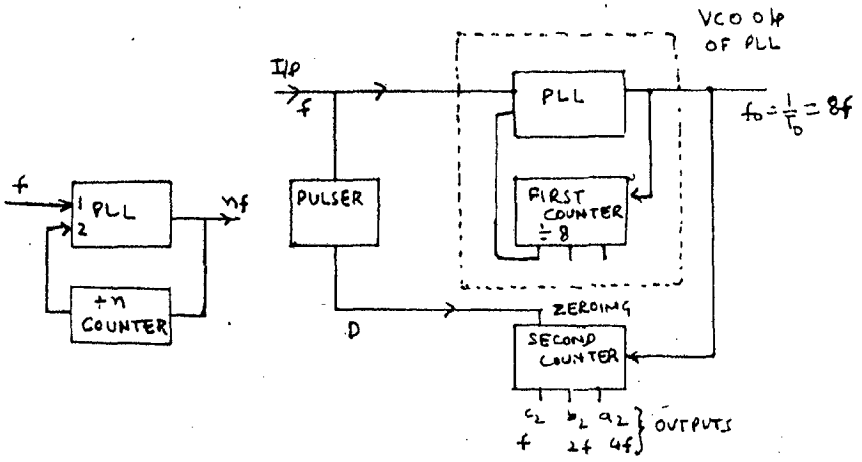


FIG.(3.14.a) CONVENTIONAL FREQ. MULTIPLIER USING PLL

FIG.(3.14.b) SYNCHRONOUS FREQ. MULTIPLICATION BY FACTORS 1, 2, & 4.

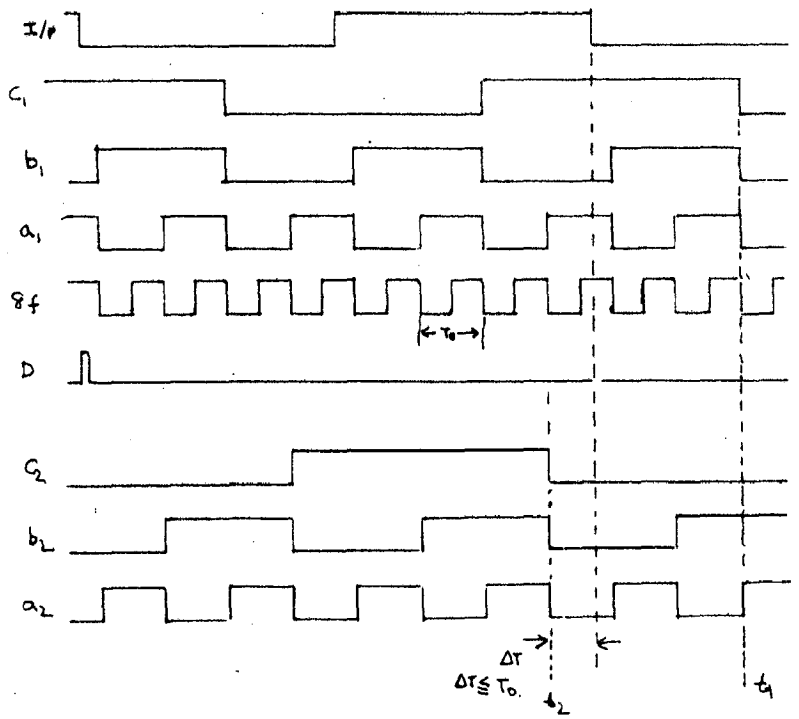


FIG.(3.14.c) WAVEFORMS AT VARIOUS POINTS OF CKT (3.14.b)

of the VCO O/P of the PLL. We thus can consider the O/Ps a_2, b_2 c_2 coarsely or with an error-

$$t \leq t_0 \qquad -- \quad (3.14.1)$$

synchronized with the input. It is to be noted C_2 has smaller relative error than the O/Ps b_2, a_2. If we make-

$\Delta T \ll$ The multiple output period -- (3.14.2)

or equal practically to zero we may accept the O/P synchronized with the input. The Fig.(3.14-d) shows PLL, divide by n counter and two equal divide by m counters and a pulser. Since the PLL has jitter, an undesirable change may occur every time the reset pulse is applied to the counter. The absolute error or jitter width is given by-

$$\Delta t \leq \text{the period of the VCO O/P} = \frac{1}{mnf} \qquad -- \quad (3.14.3)$$

according to the above mentioned result (3.14.1). The max. relative error at the O/P can be expressed by -

$$e_r = \frac{t_{max}}{1/nf} = \frac{1}{m} \qquad -- \quad (3.14.4)$$

It is obvious that this error can be minimized by choosing m large enough. But because of the maximum frequency (f_{max})of VCO characteristics m is limited such that-

$$mnf \leq f_{max} \qquad -- \quad (3.14.5)$$

By using(3.14.4) and (3.14.5) one can determine the maximum multiplication rate for a given frequency.

COMMENTS:

1) The ckt was tested for f_{in} = 50 H_z, n =12 and m = 256. In these measurements jitter width has never exceeded 6.5 μS. This result satisfies the error equation(3.14.4). The maximum relative error at the O/P is 0.4%. It can be made even smaller by choosing a proper PLL.

2) The synchronization is only achieved in the tracking range of the PLL. The tracking range is $\mp$30% of the input frequency in the practical ckt.

3) The method can be regarded as a convenient one for low frequency synchronous frequency multiplication with an acceptable error.

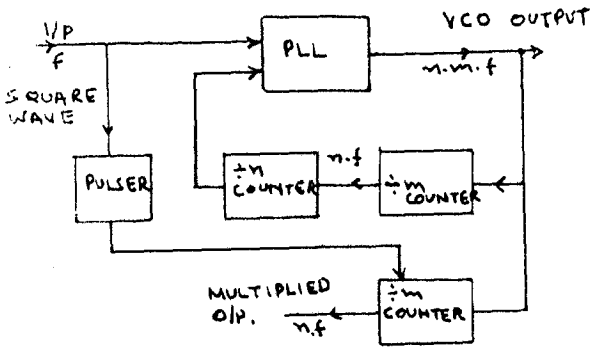
4) The maximum multiplication ratio is limited by the maximum operating frequency of VCO characteristics and the given error limit.

5) The transient response to changes in the input frequency will be dependent on characteristics of the filter used in PLL.

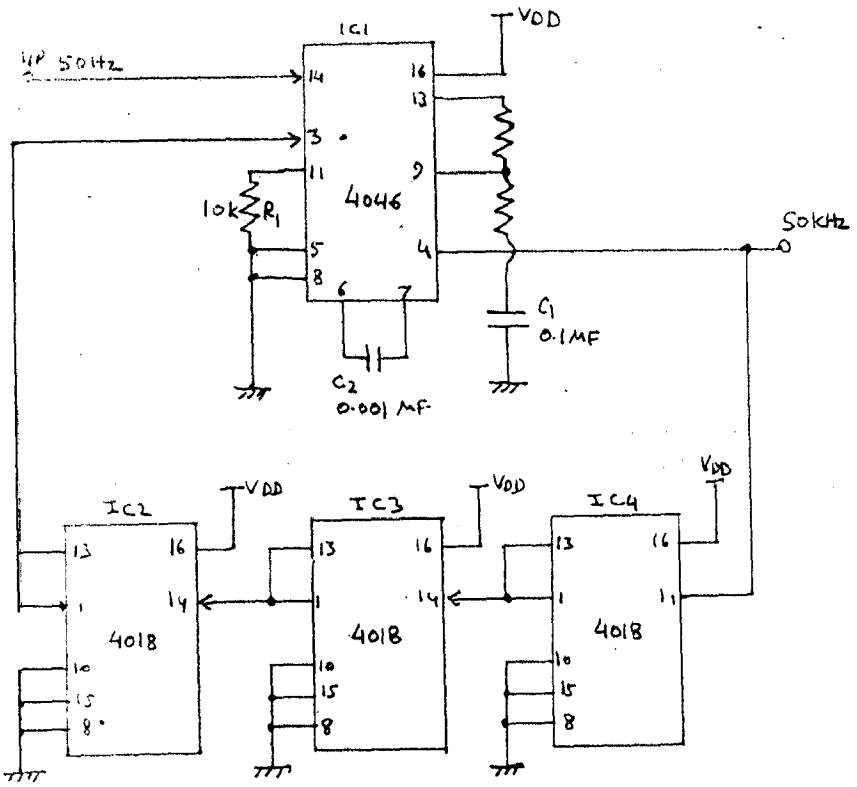
3.15 A HIGH RESOLUTION FREQUENCY METER FOR 50H_z [23]

PRINCIPLE -

The input signal (a sine wave of nominal frequency 50H_z is amplified and limited to produce a square wave. This signal is applied to an inexpensive CMOS (PLL)IC (CD 4046)



FIG(3.14.a) THE BLOCK DIAGRAM OF SYNCHRONOUS FREQUENCY MULTIPLIER.



Fig(3.15.a) FREQUENCY MULTIPLIER

which contains a controlled oscillator. The oscillator output is divided and is applied to the PLL comparator input. The PLL will lock when the signal at the comparator input is in phase with the input signal to the PLL. Hence, if the input frequency is $50H_z$, the oscillator frequency will be 50 x 1000 =$50KH_z$ The 50 KH_z signal may be applied to a conventional frequency counter which, by programming the decimal point, may be made to display the input frequency as 50000 with a gate time of 1 sec., the resolution is however 1 part in 50,000 (0.002%).

The Fig.(3.15-a) shows the practical realization of the above. The PLL is a CMOS 4046 and the dividers are 3 x CMOS 4018. With the component values shown and a supply voltage of 5V, the circuit had a locking range of app.30-$70H_z$.

3-16 FREQUENCY MULTIPLIER FOR YOUR COUNTER [24]

PRINCIPLE AND WORKING

It is basically a PLL (phase lock loop) circuit it has X 10 and X 100 outputs. Low frequency signal appearing at the input pass through the GAIN potentiometer, which permits the frequency multiplier to handle a very wide range of signal levels. Then, the attenuated signal drives IC_1, which shapes it into a square wave. That signal drives phase detector IC_2.

Another part of the same IC also serves as a VCO (voltage controlled oscillator). It accepts a DC Voltage from the phase detector and generates a square wave signal.The VCO can generate signals ranging from under 100 H_z to over 400 KH_z without any switching. From the VCO, the signal-path branches out.

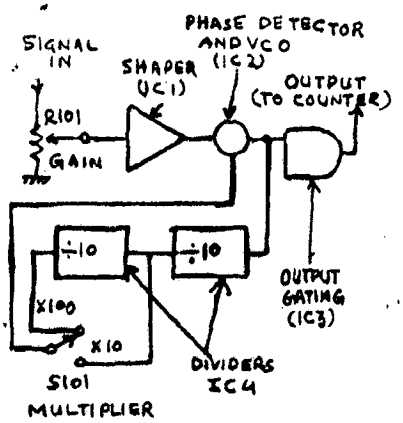
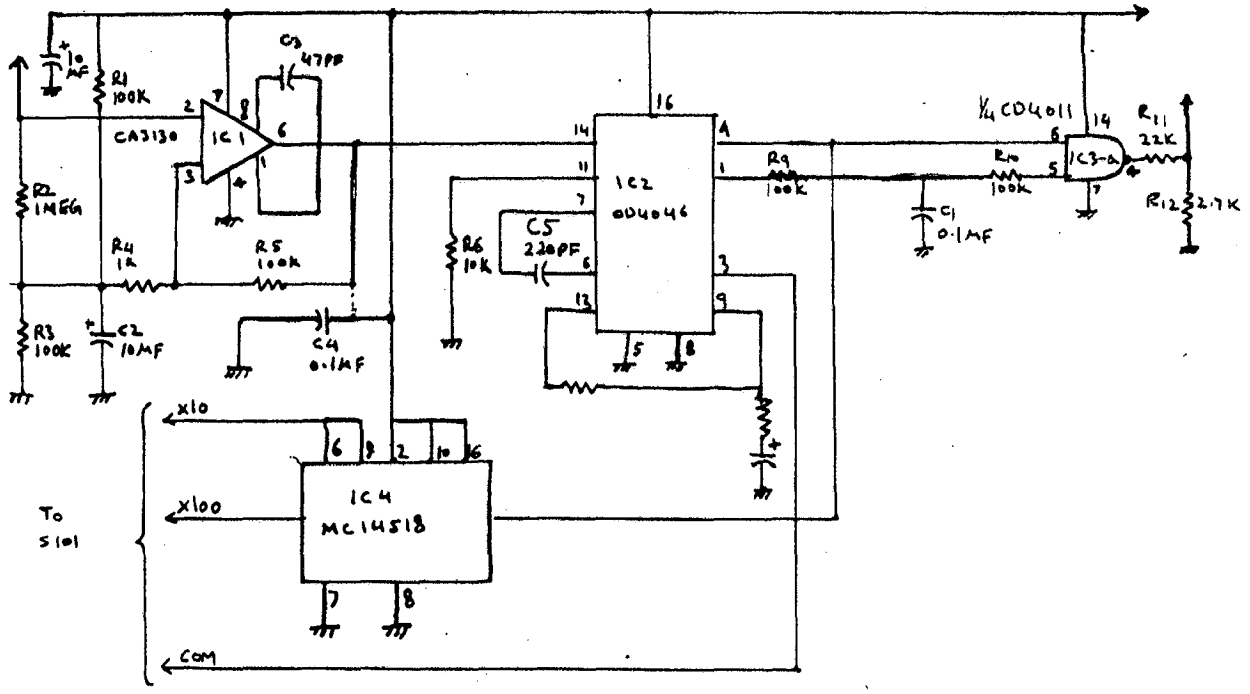


FIG (3.16.a) MULTIPLICATION FACTOR is determined by number of divide by ten counters used.



A LOGIC HIGH OUTPUT from Pin 1 of IC_2 indicates that the PLL is Locked

FIG. (3.16.b) :- FREQUENCY MULTIPLYING SCHEME.

One branch takes the signal to IC3, a NAND gate, that gate acts as a switch and allows signal to pass to the frequency counter only when the PLL is locked on to a good signal. That suppresses the stray readings one can normally get without an input signal, or with signals the device can't handle.The output from the VCO also drives two divide by ten counters, both or which are contained in IC4. The outputs from the dividers are selected by S101 the MULTIPLIER switch. The output selected drives the phase detector, which generates the DC control voltage for VCO. Thus a simple PLL circuit, that can generate frequencies ten times or a hundred times .the input frequency, is formed.

ICI, the shaper amp consists of a fast CMOS CA3130 OP-AMP Its high frequency response is reduced by C_3 so the circuit won't oscillate. You will have flat gain over its 10Hz to 40KHz input range. The inputs of the OP-Amp are biased to half the supply voltage by R_1 and R_3, eliminating the need for a split (positive and negative voltages) power supply.

Resistors R_4 and R_5 set the hystersis or "trip " point for the circuit, which is about 350 mV. The output signal is a 9.0 Volts square wave that drives the phase detector portion of IC_2. The phase detector compares the signal with that from the MULTIPLIER switch, and outputs a DC voltage at pin 13 of the IC. That drives a network known as loop filter, which smooths out the pulses from the phase detector, giving a clean DC signal.

The VCO input is at pin 9 of IC2 and the timing capacitor that sets the frequency range is 65. The VCO output appears at pin 4, and drives both IC 3 and IC4. Resistors R_9 and capacitor C7 form another filter to "debounce" the signal from pin 1 of IC2 (which indicates that the PLL is locked on to the signal.). so that it can enable IC3-a's NAND gate whenever a good signal is present at pin 4 of IC2. Resistor R10 is included so that the charge on C7 won't blow IC3 when the power is turned off. The output of IC3 is reduced by R_{11} and R_{12} about 900 mV peak to peak, which is a comfortable level for most counters. The remaining circuitry consists of a standard CMOS dual divide by 10 counter IC4.

COMMENTS -

1) One has to remember to mentally shift the decimal point one place to the left while using the X 10 range and two places to the left while using the X 100 range.

2) VCO range of unit is 100 H_z - 40 KH_2 MULTIPLIER Switch set at (X 10) position mean one can measure in the range of $10H_z$ $4KH_z$ and MULTIPLIER (Switch Set) at (X 100) position means again one can measure in the range of $10H_z$ - $4KH_z$.

3) Gain can be increased by reducing R_4.

[25]

3.17 LOW FREQUENCY MEASURING CIRCUIT USING PLL

PRINCIPLE-

A PLL with a 3 decade dividers inserted into its feedback path creates a frequency multiplier that allows us to measure low (e.g.power line) frequencies accurately and quickly.

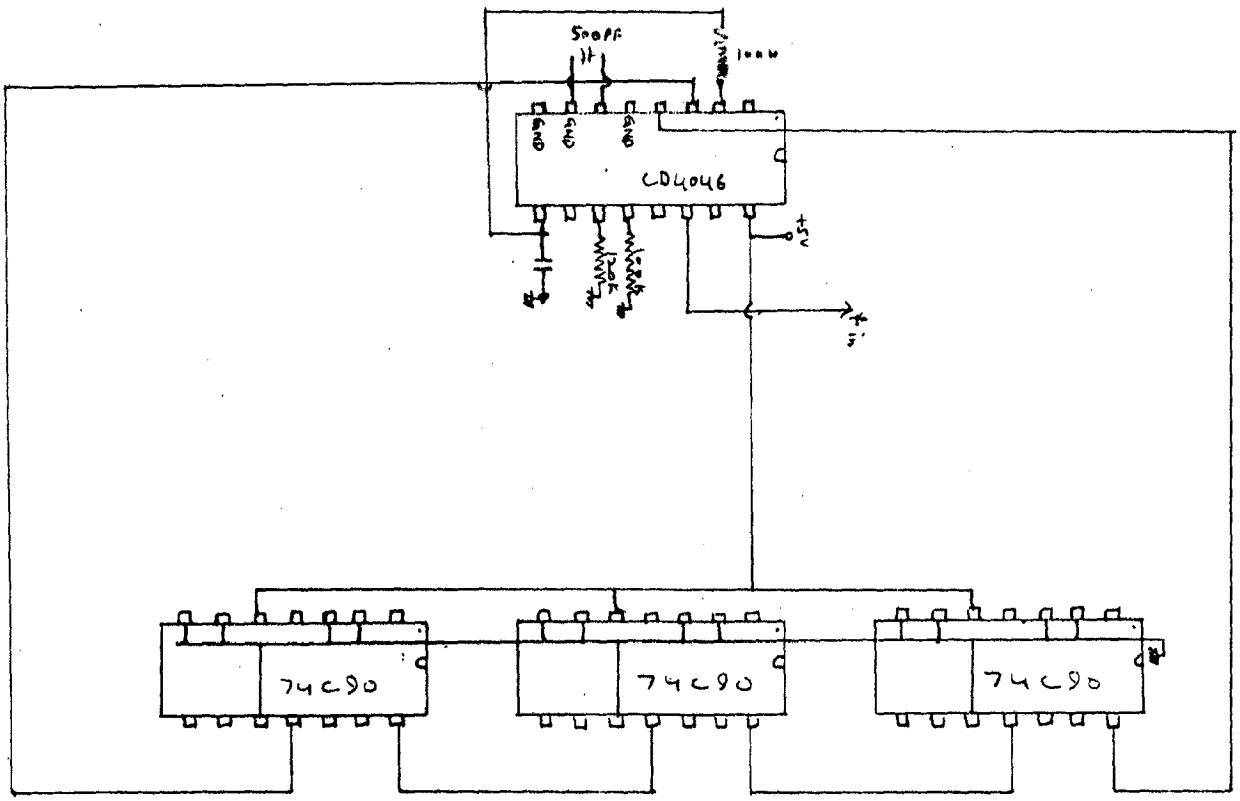


FIG. 3.17.(a)

The circuit in figure is set for $50H_z$ and can be adjusted by R_1, R_2 and C_1 to match power lime frequency.

The VCO in ICI produces an output whose frequency is determined by the time constant of R_1 and R_2 (about 50 KH_z for given component values), IC_4's phase comparator modulates this frequency. The 3 decade counter comprising IC_2 through IC_4 divides the VCO'S O/P by 1000 and applies its output to one of the PLL'S phase comparator input; the input signal to be measured is applied to the other phase comparator input.

The VCO'S frequency is thus the input frequency X 1000 and this frequency can be measured using conventional methods.

****

CHAPTER - 4

PLL - THEORY AND DESCRIPTION

4.1 BASIC PRINCIPLE - [26], [27] [28] [29] [34] [35] [36]

The phase lock loop is basically an electronic feed back loop system consisting of:

1- A phase detector or comparator

2- A low pass filter

3- A Voltage controlled Oscillator (VCO). (Ref. FIG.4.1-a)

The VCO is a free running oscillator, the frequency of which is normally determined by an external resistor-capacitor or an inductor-capacitor network. The VCO frequency f_o is fed back to the phase detector where it is compared with the frequency of the input signal (f_i). The output of the phase detector is the error voltage, which is an average dc voltage proportional to the difference in frequency($f_i - f_o$) and phase ϕ of the input and VCO.

The error voltage is then filtered, thus removing traces of higher frequency noise. This, in turn, is then fed to the VCO to complete the loop. In addition, the error voltages forces the frequency of VCO to change in a direction that reduces the frequency difference between the input and the VCO. Once the VCO starts to change frequency, the loop is in the capture range. This process continues until the VCO and the input frequencies are exactly the same. At this point, the loop is synchronized, or phase locked. During phase lock, the VCO frequency is identical to the input of the loop, ex-

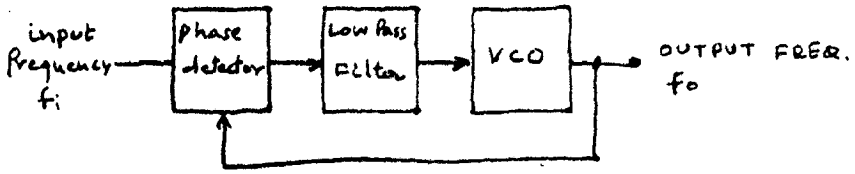
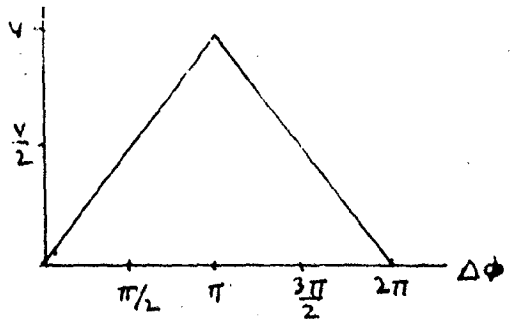
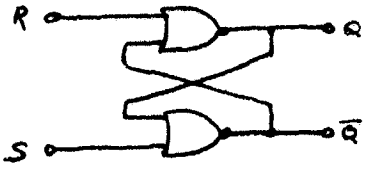


FIG (4.1.a) BASIC PHASE LOCK LOOP SCHEME.

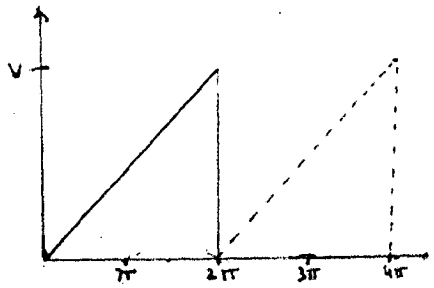
(i) TWO INPUT EX-OR GATE



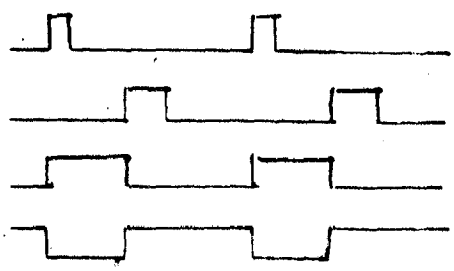
(ii) EX-OR PHASE DETECTOR INPUT/OUTPUT CHARACTERSTICS.



(iii) The R-S FLIP FLOP



(iv) EDGE TRIGGERED PHASE DETECTOR I/O Characteristics



(v) INPUT/OUTPUT WAVEFORM FOR THE EDGE TRIGGERED P.D.

FIG (4.2.a) PHASE DETECTORS

except for a finite phase difference, which is required to generate the necessary error voltage that shifts the VCO frequency, keeing the loop in phase lock. This repetitive action of the loop system then tracks, or follows, any change in the input frequency while phase locked. We can say that the phase locked loop has three distinct states:

1- Free running

2- Capture

3- Phase lock.

The range over which the loop system will follow changes in the input frequency is called the lock range. On the other hand, the frequency range in which/the loop acquires phase lock is the capture range, and is never greater than the lock range. The dynamic characteristics of the phase lock loop are controlled primarily by Low Pass Filter. If the difference between the input and VCO frequencies is significantly large, the resultant signal may be too high to be passed by the filter. Consequently, the signal is out of the capture range of the loop. Once the loop is phase locked, the filter only limits the speed of the loop's ability to track changes in the input frequency. In addition, the loop filter provides a sort of short term memory, ensuring a rapid recapture of the signal if the system is thrown out of the lock by a noise transient.

4.2 THE PHASE DETECTOR

All phase locked loop systems use a circuit called a phase detector or phase comparator. The phase detector

generates an average, or dc, output voltage that is proportional to the phase difference between the input of phase - locked loop and VCO. The output voltage is often referred to as the error voltage .The factor that convert phase difference into voltage is called the phase detector conversion gain, so that-

$$V_D = K\emptyset \, \Delta \emptyset \qquad -- \qquad (4.2.1)$$

Where, V_D is the average output voltage of the phase detector (V)

$K\emptyset$ is the phase detector conversion gain in volts/radin,

$\emptyset$ is the input phase difference in radians.

NOTE - When working with PLL, it is customary to express phase difference in terms of radians.

In digital phase locked loops we use either exclusive-OR or some type of edge triggered phase detector. Digital PLL most commonly used is CD 4046, it has both type of detectors. Phase detector I (Exclusive OR gate type) and phase detector II(Edge triggered type). Both phase detectors have same input i.e. both input of the I.C.CD4046 are in parallel, The outputs, however, are brought out separately.

Phase detector-I (The Ex- OR phase detector).

This type uses a Two input exclusive -OR-gate logic and symbolic Ex-OR with two inputs is given in Fig.(4.2-a). A truth table for this gate is given in Table (4.2).

TABLE 4.2 TRUTH Table for Fig.(4.2-a) -

INPUTS		OUTPUT
A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

Because of this truth table, exclusive OR type phase detectors (or some times referred as the low noise detector) are used for input and VCO wave forms that must have a 50%, duty cycles i.e.symmetrical.

By plotting the average output voltage of the exclusive OR phase detector as a function of the phase difference of its two inputs, a triangular characteris results Fig.(4.2-a) The slope of the rising line of this characteristics is called as phase detector conversion.gain ($K\emptyset$) and is expressed in units of volt/radian. Also slope of characteric from II to III is also phase Detector Conversion gain ($K\emptyset$). The TTL EX- OR gate is the 7486 integrated circuit, while the CMOS equivalent is 4030 or 74C 86.

Phase detector-II - A second type of digital phase detector is the edge triggered type (or sometimes referred the wide band phase detector.). One of the simplest type of edge triggered detector is Set-Reset or R-S flip flop. Fig(4-2-a.).

The two basic rules governing the operation of RS flip flop as an edge triggered phase detector are as follows:

1) If the set or S input is at logic '1', the Q output goes to or stay at logic '1', while the $\bar{Q}$ output goes to or stays at logic '0' (ground).

2) If the reset or R input is at logic '1', the Q output goes to or stay at logic '0', while the $\bar{Q}$ output goes to or stay at logic '1'.

As shown in the timing diagram Fig.(4.2-a), the NOR gate RS flip flop is triggered on the positive leading edge of the two inputs. For the R-S flip flop, as well as other types of edge triggered detectors, the input pulses are usually of short duration rather than the symmetrical 50% duty cycle pulses associated with the exclusive-OR detector. Similar to the exclusive OR gate, average output voltage of the edge triggered detector varies proportionately as the phase difference between the input and VCO varies. By plotting the average output voltage as a function of the phase difference betweenthe S & R inputs, a sawtooth shaped characteristic is obtained as shown in Fig. (4.2-a). Consequently, the edge triggered type detector has twice the linear range as the double valued triangular wave of the Ex-OR detector. In addition, the edge triggered detector will posses significantly better capture, tracking and locking characteristic than the exclusive OR detector.

Phase detector-II (sometimes referred as the wide band detector) is an edge triggered digital type, which triggers on the positive leading edges of the inputs. If the input

signal which can be pulse train having any duty cycle, is lower than the VCO frequency, the output is at logic '1' ($+V_{DD}$) If both frequencies are same, the output of phase detector-II is a pulse whose width is proportional to the phase difference Fig.(4.2-a), this output pulse is positive when VCO signal lags the input and negative when the VCO leads the input, the main advantage of the phase detector-II over Phase detector -I is that phase detector-II is insensitive to harmonics, while phase detector-I may lock onto harmonic multiplies of the input frequency.

4.3 THE VCO

The voltage controlled oscillator is the second integral building block of the PLL. Its output frequency is directly proportional to its input control voltage. (Fig.4.3-a). The VCO can also be termed a voltage to frequency converter, so that mathematically -

$$w_o = K_o V_f \qquad -- \qquad (4.3.1)$$

Where, w_o is the VCO output frequency (rad/S).

V_f is the VCO input control voltage from the loop filter.

K_o is the VCO conversion gain (rad/S/V).

The VCO conversion gain (K_o) is the proportionality constant that converts the input control voltage to frequency. In PLL literature, w is used to represent the frequency, in units of

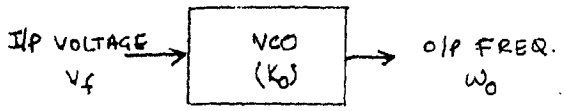


FIG. (4.3.a) (BLOCK DIAGRAM OF BASIC VCO.)

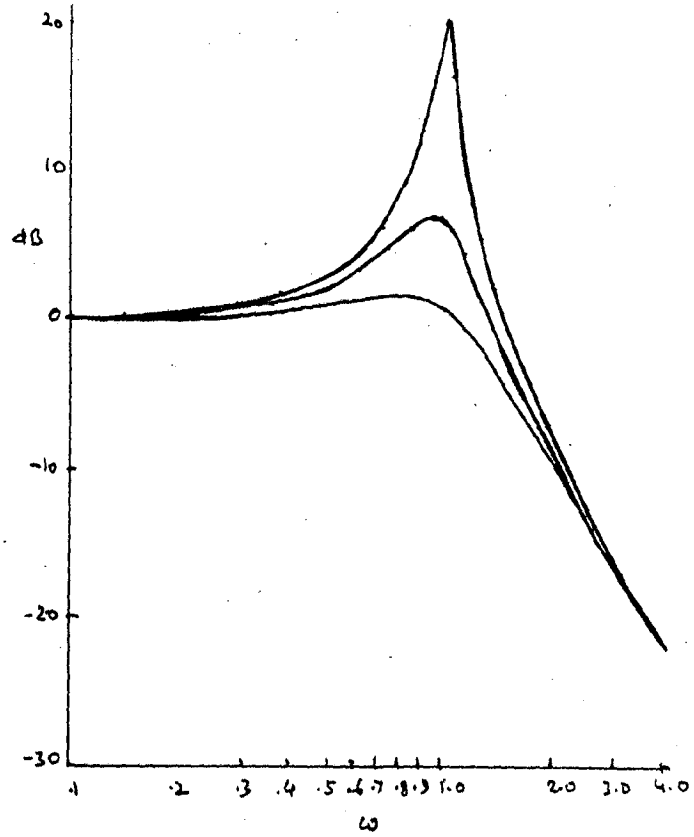
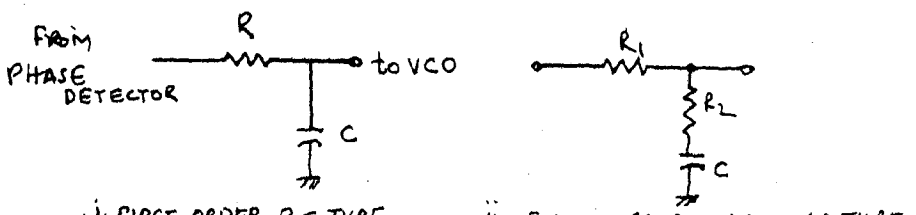
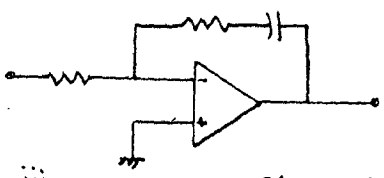


FIG.(4.4.a) EFFECT OF DAMPING ON FREQUENCY RESPONSE OF SECOND ORDER SYSTEM.



(i) FIRST ORDER R-C TYPE (ii) FIRST ORDER LAG-LEAD TYPE.



(iii) ACTIVE LOW PASS TYPE.

FIG.(4.4.b) LOW PASS FILTERS.

radians/second. During phase lock, the ouput frequency of the VCO will be exactly equal to the input frequency of the loop, ~~ex~~ except for a constant finite phase difference. Since the radian frequency is the time derivative of phase,

$$w = \frac{d}{dt}(\Delta\emptyset) \quad \text{rad/S} \qquad (4.3.2)$$

The phase difference between the VCO output frequency and the loop input frequency is really proportional to the integral of the input control voltage, which is the average or dc voltage from the phase detector and the loop filter. Any ac signal superimposed on the dc control voltage will, in turn, vary the VCO frequency.

4.4 LOOP FILTER -

The loop filter controls the lock, capture, bandwidth and transient response of the loop. The loop filter is essentially a low pass filter network used in phase locked loop.

This performs two major functions:-

1) It removes any noise and high frequency components from the output voltage of the phase detector, thus giving an average (dc) voltage.

2) It is the primary building block that determines the dynamic performance of the loop, which includes the following factors:

   * Capture range.
   * Band width.
   * Transient response.

The loop filter may either be passive or active. The complete phase-locked loop system exhibits the characteristics of a second order system (analogous to a swinging pendulam or vibrating string).

The response of a second order system in terms of frequency is given as -

$$\frac{V_{out}}{V_{in}}\ (dB) = -20\log\left[w^4 + 2w^2(2\zeta^2-1) + 1\right]^{\frac{1}{2}} \qquad -- (4.4.1)$$

Where V_{in} = loop input voltage, V_{out} = loop output voltage,

ζ = damping factor (dimensionless).

w = ratio of the input frequency (w_1) to the undamped natural frequency (w_n).

By plotting (4.4.1), as shown in Fig.(4.4a) the single parameter that governs the overall shape of the response V/S frequency curve of a second order system is the damping factor(ζ) or damping ratio. For a given value of damping, the frequency at which the response is a maximum is the undamped natural frequency. For a lesser amount of damping we have a greater amount of peaking at natural frequency. The frequency at which the response is/3dB less than the maximum response is called the bandwidth of the system. The parameters such a damping factor and the undamped natural frequency are primarily controlled by the loop filter i.e depending upon the filter design we are able to control the loop response.

Low pass filter circuits - In PLL there are a number of popular low pass filter circuits but only the following three

types are common:

i) First order RC low pass filter.

ii) First order, lag lead low pass filter.

iii) Active low pass filter.

i) The first order RC low pass filter - Here a simple RC network is placed between the phase detector and VCO. The cut-off frequency is given by -

$$\omega_{LPF} = \frac{1}{RC} \text{ (rad/S)} \qquad \text{-- (4.4.2)}$$

Also, loop natural frequency can be expressed in terms of ω_{LPF} so that-

$$\omega_n = (K_\phi K_o \omega_{LPF})^{\frac{1}{2}} \qquad \text{-- (4.4.3)}$$

The damping factor 3 can be expressed as -

$$3 = \frac{1}{2} \cdot \left(\frac{\omega_{LPF}}{K_\phi K_o} \right) \qquad \text{-- (4.4.4)}$$

ii) First Order, Lag Lead Low Pass Filter (Fig.4.4-b)

This type of filter is useful for the faster locking of signal. Here cut off frequency is given by

$$\omega_{LPF} = \frac{1}{(R_1 + R_2)C} \text{(Yad/S)} \qquad \text{-- (4.4.5)}$$

The natural frequency w_n is given as -

$$w_n = (K_\phi K_o w_{LPF})^{\frac{1}{2}} \text{ Yad/S} \quad -- \quad (4.4.6)$$

and the damping factor is given by --

$$3 = \frac{w_n}{2}\left[R_2C + \frac{1}{K_\phi K_o}\right] \quad -- \quad (4.4.7)$$

(iii) The passive lag-lead network can be used with an Op-amp to form an active filter circuit. The cut off frequency is then written as -

$$w_{LPF} = \frac{1}{R_1C}(\text{Yad/S}) \quad -- \quad (4.4.8)$$

While the loop natural frequency and damping factor are found from -

$$w_n = (K_\phi K_o w_{LPF})^{\frac{1}{2}} \text{ rad/S} \quad -- \quad (4.4.9)$$

$$\text{and } 3 = \left(\frac{R_2C}{2}\right) w_n \quad -- \quad (4-4-10)$$

It is to be noted that the natural frequency of the loop depends entirely on the product $K_\phi K_o$ (often referred to as the (dc loop gain) and the filter cut off frequency.

The Transient Response:

When an underdamped second order system ($3 < 1$) encounters a sudden change at its input, such as the phase lock loop shifting from one frequency (f_1) to another (f_2), the output of the VCO tries to follow this change but oscillates about the value of f_2 for a time and eventually settles out at the new frequency

(i.e.steady state) Fig.4.4-c. How fast this process is completed depends on the loop damping factor, which, in turn, is controlled by the loop filter. In case of simple passive RC filter of Fig.(4.4-b_2) it takes longer for the oscillations to settle down to the steady state value as the damping factor is decreased. To reasonably pick values of 3 and w_n, one method is to design for a specified amount of overshoot within a given settling time.

As a general rule, the damping factor is chosen to be between 0.5 to 0.8. The amount of overshoot and settling time, one can decide as per the design requirements.

From the transient response of the loop, the damping factor can be easily estimated simply by knowing the peak amplitude of two consecutive positive peaks which are exactly 1 cycle apart, the damping factor can, therefore, be expressed as-

$$3 = \frac{Y}{(1+Y^2)^{\frac{1}{2}}} \qquad -- \quad (4.4.11)$$

$$\text{Where } Y = \frac{1}{2\pi} \ln \frac{y_A}{y_B}.$$

y_A, y_B are maximum amplitude of two consecutive peaks which are exactly one cycle apart. So, if a filter, RC type or lag lead type, is placed between phase detector and VCO. The respose of the system will be periodic oscillation with a fixed frequency w_d, so that -

$$w_d = \frac{2\pi}{T} \qquad -- \quad (4.4.12)$$

w_d is called as damped natural frequency of the system, and T is the period of oscillation. However, the damped natural frequency depends on the damping factor and the natural frequency of the loop, so that ---

$$w_d = w_n(1- 3^2)^{\frac{1}{2}} \qquad -- \quad (4.4.13)$$

Consequently, the damped natural frequency is always less than the loop natural frequency. However, the amount of difference will depend on damping factor.

LOCK AND CAPTURE:

The lock range ($2w$) of the PLL is the frequency range over which the loop system will follow changes in the input frequency. several writers uso the term tracking range and hold in range. The hold in range refers to how far the input frequency cam deviate from the VCO free running frequency, w_0, and is numerically one half the lock, or tracking range.

On the other hand the range over which the PLL acquires phase lock is the capture range ($2w_c$). Several writers use the term lock in range, which refers to how chose an input frequency must be to the VCO free running frequency before the loop acquires phase lock. The lock in range is numerically one half the capture range.

The Fig.(4.4-d) shows the general frequency to voltage transfer characteristics of a PLL. In the top characteristic,

the input frequency (w_i) is gradually increased so that the loop does not respond until w_i equals w_1, which is the lower edge of the capture range. The loop is then phase locked onto the input frrquency, causing the loop error voltage to go negative. As the input frequency is increased, further the error voltage increases linearly with a slope equal to the reciprocal of the VCO conversion gain, or $1/K_0$ (V/rad/S). When the input frequency equals the VCO free running frequency, the error voltage is zero. The loop continues to tract the input until w_2, the upper edge of the lock range. For input frequencies greater than w_2, the loop is unlocked, the error voltage is zero, and the VCO is at its fre running frequency. When the input frequency decreases, the process is repeated, except that now the error voltage goes positive at, w_3, the upper edge of the capture range. So, we have following relationships:-

Lock range: $2w_L = w_2 - w_4$ -- (4.4.14)

Hold in range: $w_L = w_2 - w_0$ -- (4.4.15)

$= w_0 - w_4$

Capture range: $2w_c = w_3 - w_1$ -- (4.4.16)

Lock in range: $w_c = w_0 - w_1$ -- (4.4.17)

$= w_3 - w_0$

In terms of loop parameters, the hold in range is numerically equal to the dc loop gain (K), so that -

$w_L = K \emptyset K_0 (rod/s)$ -- (4.4.15)

$=$

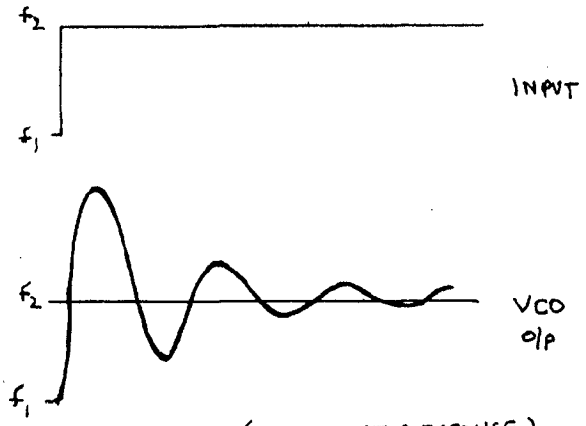
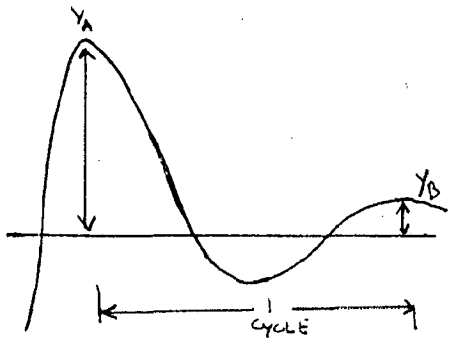


FIG.(4.4.c) (TRANSIENT RESPONSE.)



DAMPING FACTOR DETERMINATION

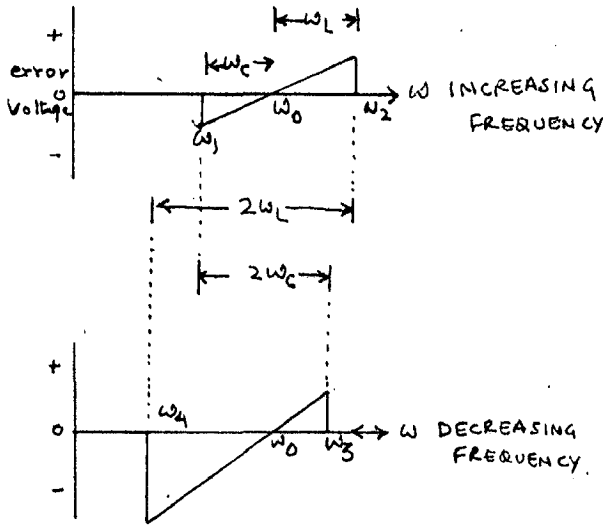
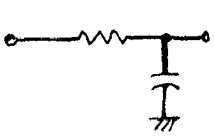
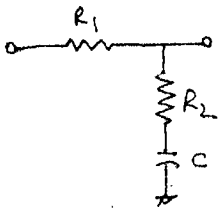


FIG.(4.4.d) PHASE LOCKED LOOP, FREQUENCY TO VOLTAGE TRANSFER CHARACTERSTICS.



FIG(4.5.b) PASSIVE LOW PASS FILTER



FIG(4.5.c) PASSIVE LAG LEAD TYPE.

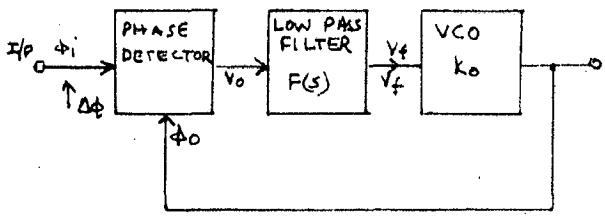


FIG.(4.5.a) BLOCK DIAGRAM OF BASIC PLL.

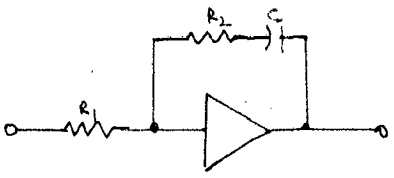


FIG.(4.5.d) ACTIVE PHASE LAG. FILTER

i.e.this range does not depend on the parameters of the low pass filter. However, the filter does limit the maximum rate at which phase lock can occur, since the voltage across the filter capacitor (S) cannot charge instantaneously.

The following are the approximate expressions for the lock in range based on the type of filter used:

(i) RC Filter

$$w_c = \left(\frac{w_L}{R_C}\right)^{\frac{1}{2}} \text{ rad/S} \qquad \text{--(4.4.18)}$$

(ii) Passive lag- Lead Network:

$$w_c = w_L \left(\frac{R_2}{R_1+R_2}\right) \qquad \text{--(4.4.19)}$$

(iii) For Active Filter:

$$w_C = w_L \frac{R_2}{R_1} \qquad \text{--(4.4.20)}$$

By making use of the equations for the loop damping factor and natural frequency, the lock in range can be further approximated by --

$$w_c = 23 w_n \qquad \text{--(4.4.21)}$$

4.5 D E R I V A T I O N S:

4.5A The Basic Transfer Function:

For the basic PLL shown in Fig.(4.5-a), we have a phase detector, a low pass filter, and a voltage controlled oscillator

The equation (4.5.3) can now be written as-

$$\frac{d\phi}{dt} = \frac{K_o V_f(S)}{\qquad} \qquad -- \qquad (4.5.5)$$

Taking the replace transform of equation (4.5.5)-

$$\phi_o(S) = \frac{K_o V_f(S)}{S} \qquad -- \qquad (4.5.6)$$

So that the output signal of the VCO is proportional to the integral of the VCO input voltage. Using the equation(4.5.1) (4.5.2) and (4.5.6), we can solve for the transfer function,

$$T.F = T(S) = \frac{\phi_o(S)}{\phi_i(S)} = \frac{K_\phi K_o F(S)}{S+K_\phi K_o F(S)} \qquad -- \qquad (4.5.7)$$

whose final form, of course, depends on F(S) or in other words, type of filter used:

4.5-B- Loop Filter-A - For the simple, passive, low pass filter shown in Fig.(4.5-b), the T.F. of the network can be written as-

$$F_A(S) = \frac{1}{1+T_s} \qquad \text{---------} \qquad -- \qquad (4.5.8)$$

Where, T = RC, the substitution of equation (4.5.8) into equation (4.5.7) gives-

$$T_A(S) = \frac{K_\phi K_o/T}{S^2+(1/T)S+(K_\phi K_o/T)} \qquad -- \qquad (4.5.9)$$

i.e. this range does not depend on the parameters of the low pass filter. However, the filter does limit the maximum rate at which phase lock can occur, since the voltage across the filter capacitor (S) cannot charge instantaneously.

The following are the approximate expressions for the lock in range based on the type of filter used:

(i) RC Filter

$$w_c = \left(\frac{w_L}{R_C}\right)^{\frac{1}{2}} \text{ rad/S} \qquad \text{--(4.4.18)}$$

(ii) Passive lag- Lead Network:

$$w_c = w_L \left(\frac{R_2}{R_1+R_2}\right) \qquad \text{--(4.4.19)}$$

(iii) For Active Filter:

$$w_C = w_L \frac{R_2}{R_1} \qquad \text{--(4.4.20)}$$

By making use of the equations for the loop damping factor and natural frequency, the lock in range can be further approximated by --

$$w_c = 23 w_n \qquad \text{--(4.4.21)}$$

4.5 D E R I V A T I O N S:

4.5A The Basic Transfer Function:

For the basic PLL shown in Fig.(4.5-a), we have a phase detector, a low pass filter, and a voltage controlled oscillator

or VCO. For a phase difference ($\Delta\phi$) between the input signal and the output of the VCO, the output voltage of the phase detector is proportional to this phase difference so that-

$$V_o = K\phi \Delta\phi \qquad -- \qquad (4.5.1)$$

where the constant, $K\phi$, is the conversion gain of the phase detector in V/rad.

In turn, the output voltage of the phase detector is filtered by the low pass filter, which also determines the dynamic characteristics of the loop. For the time being, the transfer function of the low pass filter is represented by F(S)-
In general the output of the filter is-

$$V_f(S) = V_0 F(S) \qquad -- \qquad (4.5.2)$$

The output voltage of the filter then controls the output frequency of the VCO. Depending on this voltage, the VCO frequency will have deviation (Δw) from its centre frequency (w_o) so that--

$$\Delta w (S) = K_o V_f(S) \qquad -- \qquad (4.5.3)$$

Where K_0 is the conversion gain of the VCO in Yad/S/V. Since frequency is the time derivative of phase-

$$w = \frac{d\phi}{dt} \qquad -- \qquad (4.5.4)$$

The equation (4.5.3) can now be written as-

$$\frac{d\phi}{dt} = \frac{K_o V_f(S)}{} \quad -- \quad (4.5.5)$$

Taking the replace transform of equation (4.5.5)-

$$\phi_o(S) = \frac{K_o V_f(S)}{S} \quad -- \quad (4.5.6)$$

So that the output signal of the VCO is proportional to the integral of the VCO input voltage. Using the equation(4.5.1) (4.5.2) and (4.5.6), we can solve for the transfer function,

$$T.F = T(S) = \frac{\phi_o(S)}{\phi_i(S)} = \frac{K_\phi K_o F(S)}{S+K_\phi K_o F(S)} \quad -- \quad (4.5.7)$$

whose final form, of course, depends on F(S) or in other words, type of filter used:

4.5-B- Loop Filter-A - For the simple, passive, low pass filter shown in Fig.(4.5-b), the T.F. of the network can be written as-

$$F_A(S) = \frac{1}{1+T_s} \quad \text{---------} \quad -- \quad (4.5.8)$$

Where, T = RC, the subetitution of equation (4.5.8) into equation (4.5.7) gives-

$$T_A(S) = \frac{K_\phi K_o/T}{S^2+(1/T)S+(K_\phi K_o/T)} \quad -- \quad (4.5.9)$$

Equating the terms of the denominator of equation (4.5.9) with the basic characteristic equation of second order system-

$$s^2 + 23w_n + w_n^2 \quad -- \quad (4.5.10)$$

Where, 3 = damping factor

w_n = loop natural frequency,

We find that-

$$3 = \frac{1}{2}\left(\frac{1}{K_\phi K_o T}\right)^{\frac{1}{2}} \quad -- \quad (4.5.11)$$

and $$w_n = \left(\frac{K_\phi K_o}{T}\right)^{\frac{1}{2}} \quad -- \quad (4.5.12)$$

So that the equation (4.5.9) can be written in a more convenient form,

$$T_A(S) = \frac{w_n^2}{S^2 + 23w_n S + w_n^2} \quad -- \quad (4.5.12)$$

LOOP Filter B For the passive phase-lag lead type filter, [4.5-C] The following T.F.can be written Fig. (4.5.C).

$$F_B(S) = \frac{T_2(S) + 1}{(T_1+T_2)S+1} \quad -- \quad (4.5.14)$$

Where, T_1 $T_1 = R_1C$

$T_2 = R_2C$

Substitution of equation (4.5.14) into the equation (4.5.7) yields:-

$$T_B(S) = \frac{K_\phi K_o\left[(T_2 S+1)/(T_1+T_2)\right]}{S^2+\left[(1+K_\phi K_o T_2)/(T_1+T_2)\right]S+K_\phi K_o/(T_1+T_2)} \quad --(4.5.15)$$

Equating like terms of equation (4.5.15) with equation (4.5.10) We obtain,

$$w_n = \left(\frac{K_\phi K_o}{(T_1+T_2)}\right)^{\frac{1}{2}} \quad -- \quad (4.5.16)$$

$$3 = \tfrac{1}{2}\left(\frac{K_\phi K_o}{T_1+T_2}\right)^{\frac{1}{2}}\left[T_2+\left(\frac{1}{K_\phi K_o}\right)\right] \quad -- \quad (4.5.17)$$

So that the equation (4.5.15) can be re-written as-

$$T_B(S) = \frac{w_n\left(23-\frac{w_n}{K_\phi K_o}\right)S+w_n^2}{S^2+23w_n S+w_n^2} \quad -- \quad (4.5.18)$$

4.5D Loop Filter C - For the active filter version of loop filter B, shown in Fig.(4.5-a), the T.F.can be written as-

$$F_C(S) = \left(\frac{T_2 S+1}{ST_1}\right) \quad -- \quad (4.5.19)$$

Where, $T_1 = R_1 C_1$

$T_2 = R_2 C_1$

Assuming the amplifier gain to be very high. Substitution of equation (4.5.19) into equation (4.5.7) gives-

$$T_c(S) = \frac{\frac{K_\phi K_c(1+sT_2)}{T_1}}{S^2+\left(\frac{K_\phi K_c T_2}{T_1}\right)S+\left(\frac{K_\phi K_o}{T_1}\right)} \quad -- \quad (4.5.20)$$

Equationg like terms of equation (4.5.20) with the equation (4.5.10) we obtain-

$$w_n = \left(\frac{K_\phi K_o}{T_1}\right)^{\frac{1}{2}} \quad -- \quad (4.5.21)$$

$$\zeta = \frac{T_2}{2}\left(\frac{K_\phi K_o}{T_1}\right)^{\frac{1}{2}} \quad -- \quad (4.5.22)$$

So that the equation (4.5.20) can be rewritten as-

$$T_c(S) = \frac{2\zeta w_n S + w_n^2}{S^2 + 2\zeta w_n S + w_n^2} \quad -- \quad (4.5.23)$$

Which is equal to equation (4.5.18) if $w_n / K_\phi K_o << 2\zeta$

By setting ζ equal to zero (no damping), and taking the inverse Laplace transform of equation (4.5.13), (4.5.18) & (4.5.23), we find that-

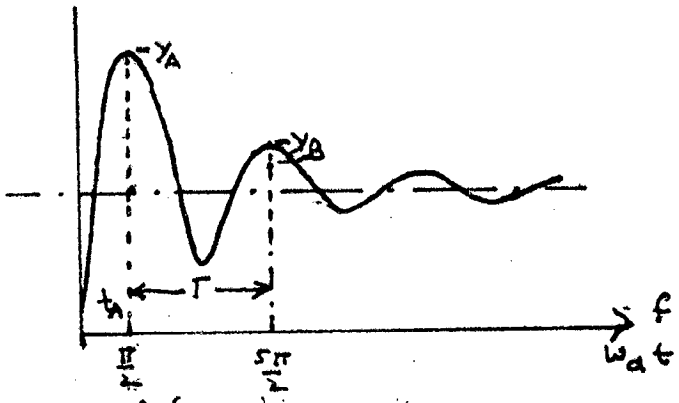
$$T_A(t) = T_c(t) = \left(\frac{B^2 + w_n^2}{w_n}\right)^{\frac{1}{2}} \sin(w_n t + \theta) \quad -- \quad (4.5.24)$$

Where, $B = K_\phi K_o$

$$\theta = \tan^{-1}\left(\frac{B}{w_n}\right)$$

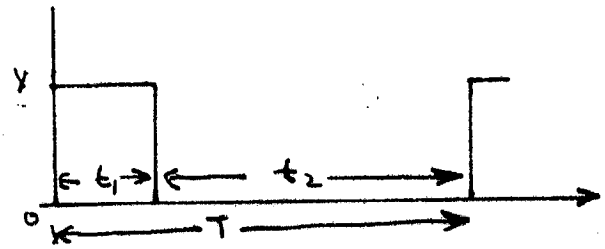
and- $$T_\theta(t) = w_n \sin(w_n t) \quad -- \quad (4.5.25)$$

For all three loop filters, the PLL system degenerates into a sinusoidal oscillator having a natural frequency of w_n.



Eq(4.5.e)

$f(t)$



4.5.f Periodic Pulse Train

4.5E Derivation of Loop Band Width:

Assuming the type B loop filter, the substitution of $s = jw$ into equation (4.5.18) yields-

$$T_B(w) = \frac{w_n^2 + j2\zeta w_n w}{(w_n^2 - w^2) + j2\zeta w_n w} \quad -- \quad (4.5.26)$$

To determine the 3 db band width ($w = w_{3db}$), we set-

$$|T_B(jw)|^2 = \frac{1}{2} \quad -- \quad (4.5.27)$$

so that, $w^4 - w^2 \left[2w_n^2 (2\zeta^2 + 1)\right] - w^4 = 0$ -- (4.5.28)

Since $w = w_{3dB}$ theequation (4.5.28) can be factored, giving:-

$$\frac{w_{3dB}}{w_n} = \left[2\zeta^2 + 1 + \left[(2\zeta^2+1)^2 + 1\right]^{\frac{1}{2}}\right] \quad -- \quad (4.5.29)$$

4.5F- Graphical Determination of Damping Factor-

The function with time of the damped sinuscidal wave form shown in Fig.(4.5.) can be expressed as -

$$y(t) = \left(\frac{y_o}{w_d}\right) e^{-\zeta w_n t} \sin(w_d t) \quad -- \quad (4.5.30)$$

Where,

y_o = y intercepts at t = 0

w_n = undamped natural frequency,

w_d = damped natural frequency

$= w_n(1-3^2)^{\frac{1}{2}}$

Equation (4.5.30) can be written in terms of the damped natural frequency, so that-

$$y(t) = \left(\frac{y_o}{w_d}\right) e^{-\left[3/(1-3^2)^{\frac{1}{2}}\right] w_d t} \sin(w_d t) \quad -- \quad (4.5.31)$$

At time $t = t_A$, $w_d t = (\pi/2)$ radians (90°), so that

$$y_A = \left(\frac{y_o}{w_d}\right) e^{-\left[3/(1-3^2)^{\frac{1}{2}}\right] (\pi/2)} \sin(\pi/2) \quad -- \quad (4.5.32)$$

Likewise at time $t = t_B$, $w_d t = 5\pi/2$ radians (450°), so that

$$y_B = \left(\frac{y_o}{w_d}\right) e^{-\left[3/(1-3^2)^{\frac{1}{2}}\right] (5\pi/2)} \sin(5\pi/2) \quad -- \quad (4.5.33)$$

dividing the equation (4.5.32 by the equation (4.5.33)

$$\frac{y_A}{y_B} = e^{\left[3/(1-3^2)^{\frac{1}{2}}\right](2\pi)}$$

Since $\sin(\pi/2) = \sin(5\pi/2)$. Taking the natural logarithm of equation (4.5.34), we obtain-

$$\ln(y_A/y_B) = (2\pi)\left[\frac{3}{(1-3^2)^{\frac{1}{2}}}\right]$$

Solving for 3, we find-

$$3 = \frac{Y}{(1+Y^2)^{\frac{1}{2}}} \quad (4.5.36)$$

Where, $\gamma = (\frac{1}{2\pi})\ln(y_A/y_B)$

Therefore, the damping factor can be determined solely by knowing the peak amplitude of two consecutive positive peaking which are exactly one cycle apart.

4.5.G- Average Value of A Pulse Train-

The average (dc) value of any periodic waveform is given:

$$\text{by average value} = \frac{1}{T}\int_0^T f(t)\,dt \qquad -- \quad (4.5.37)$$

For the periodic pulse train shown in Fig.(4.5.f), we have

$$\text{average value} = \frac{1}{T}\left(\int_0^{t_1} V\,dt + \int_{t_1}^{t_2} 0\,dt\right) \qquad -- \quad (4.5.38)$$

$$= \left(\frac{t_1}{T}\right)V \qquad -- \quad (4.5.39)$$

However, the ratio t_1/T is the duty cycle ( ) of the pulse train, so that the equation (4.5.39) can be restated as-

$$\text{Average value} = VD \qquad -- \quad (4.5.40)$$

So that the average value of a periodic pulse train is directly proportional to the waveform's duty cycle.

-****-

C H A P T E R - 5

L O W F R E Q U E N C Y M E T E R
(DESIGN, FABRICATION & TESTING)

[5.1] General-

As mentioned in Chapter-2, the frequency can generally, be measured digitally in two ways (1) Frequency comparision scheme (2) Period measurement Scheme.

Period measurements are preferred and used if frequency to be measured is low (e.g. below audio frequency) but the period measurements become quite inaccurate when frequency to be measured is below 15 to 10 H_z.[ ]. To eliminate this difficulty, one might think of the scheme of period measurement with more gate opening period and then divide the results accordingly. [ ]. No doubt, accuracy of the measurement is improved but at the cost of time i.e. measurements become quite slow. There are some other schemes also but having associated problems in one way or other.

Secondly, one may think of the scheme where low frequency can be measured by the general frequency comparision technique, however, with little modification.

Modification- The low frequency to be measured can be multiplied by some suitable factor such that it may come in the range where frequency comparision technique can be suitablly employed. The scheme is absolute and only limitations of multipliers will be the limitation of whole scheme. A number of frequency multiplying circuits are discussed in Chapter-3 [ ] to [ ]. The one

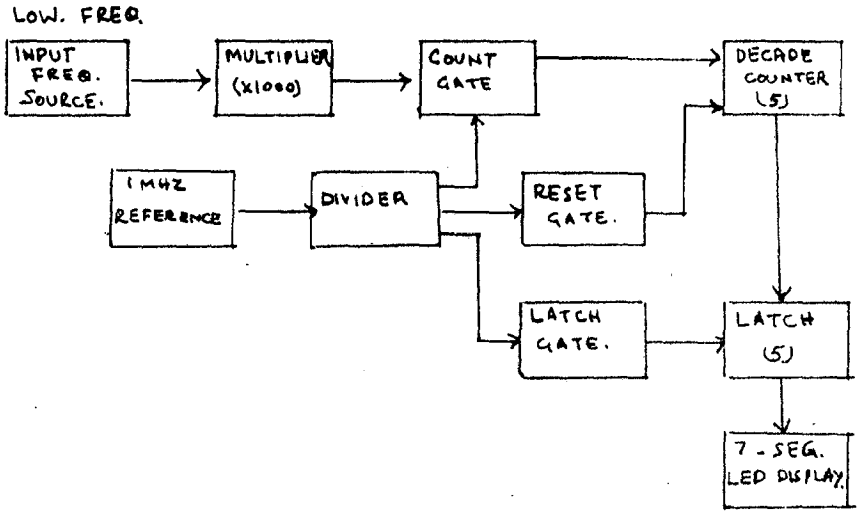


FIG.(5.1.a) BLOCK DIAGRAM OF BASIC SCHEME OF LOW FREQUENCY MEASUREMENT.

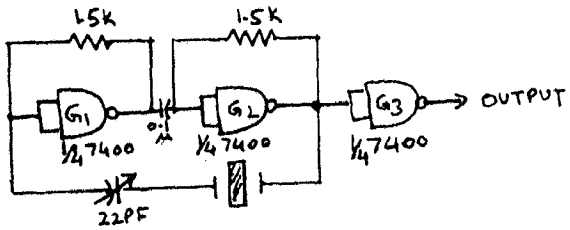


FIG. (5.2.a) CRYSTAL OSCILLATOR CIRCUIT.

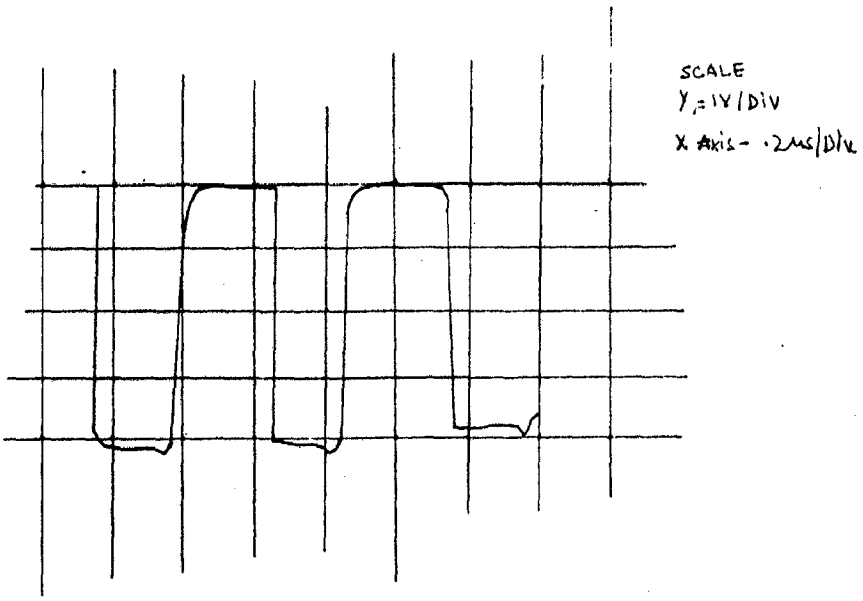


FIG. (5.2.b) CRYSTAL OSCILLATOR OUTPUT

major technique of frequency multiplication is the use of phase lock loop (PLL). [21] [22] [23] [24] [25]
The technique is quite accurate as in PLL input and output are continuously compared and then output is corrected after each comparision (by feedback process ; till both the input and output does not become equal. At this point, the loop is synchronized, or phase locked. During phase lock, the VCO frequency is identical to the input of the loop, except for a finite phase difference, which is required to generate the necessary error voltage that shifts the VCO frequency, keeping the loop in phase lock. Therefore, PLL frequency multiplying is the most suitable scheme as far as low frequency measurements are concerned.

A frequency multiplier of this type has been designed, fabricated and tested, the output of which can be used as unknown signal in the conventional digital frequency measurement scheme. The range of the input tested is 1-6H_z

The Fig.(5.1-a) illustrates a block diagram of digital frequency measurement scheme using multiplier. Here if the multiplier circuit is removed, the circuit left is general frequency comparision technique. The heart of the frequency counter is the frequency reference, which is frequently called a Time-Base. This is a very stable, fixed frequency clock signal that controls the internal operation of the counter circuitary. This stable signal is then seperated into three other signals that till the circuitary to:-

1) First reset all decade counters to zero,
2) Then count the number of pulses of unknown frequency for a fixed amount of time.

3) then latch (store) this count to-update the digital display. After the circuit complete these three sequences, this cycle begins all over again.

Here we are merely counting the number of input pulses (of course multiplied) for a given amount of time. Since this time window is typically 1 sec.long, the number of input pulses for each 1 sec.of time is the multiplied frequency of that signal and by proper decimal placement the reading can be displayed in H_z.

[5.2] Frequency Reference:-

The basic S.I Unit of time 'ATOMIC TIME' is defined by the frequency of oscillation generated in the C_s atom. Though C_s beam resonator is available commercially having an uncertainty of 10^{-10} to 10^{-11}. For precision measurements in Labs. quartz frequency standard provides reference frequency.

As a result of the piezoelectric effect existing in certain crystals particularly in quartz, an alternating polarity voltage impressed across the crystal produces mechanical dimensional changes. Thus, the force existing from such motion produces electrical change. With appropriate feedback an oscillator can be made the frequency of which is equal to the mechcanical resonance frequency of the quartz crystal. Normally, crystal is operated between its series resonant and antiresonant frequency. It allows the generation of a more stable and accurate train of clock pulses. Since the output frequency is set by the crystal, changes in frequency due to timing compo-

nents, supply voltage and temperature variations are minimized. In general, crystal controlled astable multivibrators are used for crystal frequencies in the range of 1 to 10 MH_z. A quartz crystal oscillator placed in a thermostatted enclosure can yield a short term stability of about 10^{-10}.

The crystal controlled TTL astable multivibrator can be built using three inverters of IC 7404(Hex inverter) or three gates of IC 7400(Quad Nand gate). The variable capacitor is used to trim or adjust the output frequency so that it is equal to the crystal frequency. Such an adjustment can be used to vary the frequency of oscillation by several percent of crystal frequency.

Two gates are used with crystal and third is used as buffer to isolate the oscillator from the possible loading effect of additional circuitary connected with its output.

A crystal oscillator is designed. The two gates of IC7400 are used as two inverters. Two resistances R_1 and R_2 of equal value are connected across the gate 1 and gate 2 respectively. A small capacitor is connected between two gates called as"By pass capacitor". The crystal and a small trimmer are connected in the series and then connected across these gates G_1 and G_2 as shown in the Fig.(5.2-a). The third gate G_3 is connected to output of crystal oscillator to avoid possibility of loading due to other parts of the circuitary. The Fig.(5.2-b) shows the waveshape obtained as output of crystal.

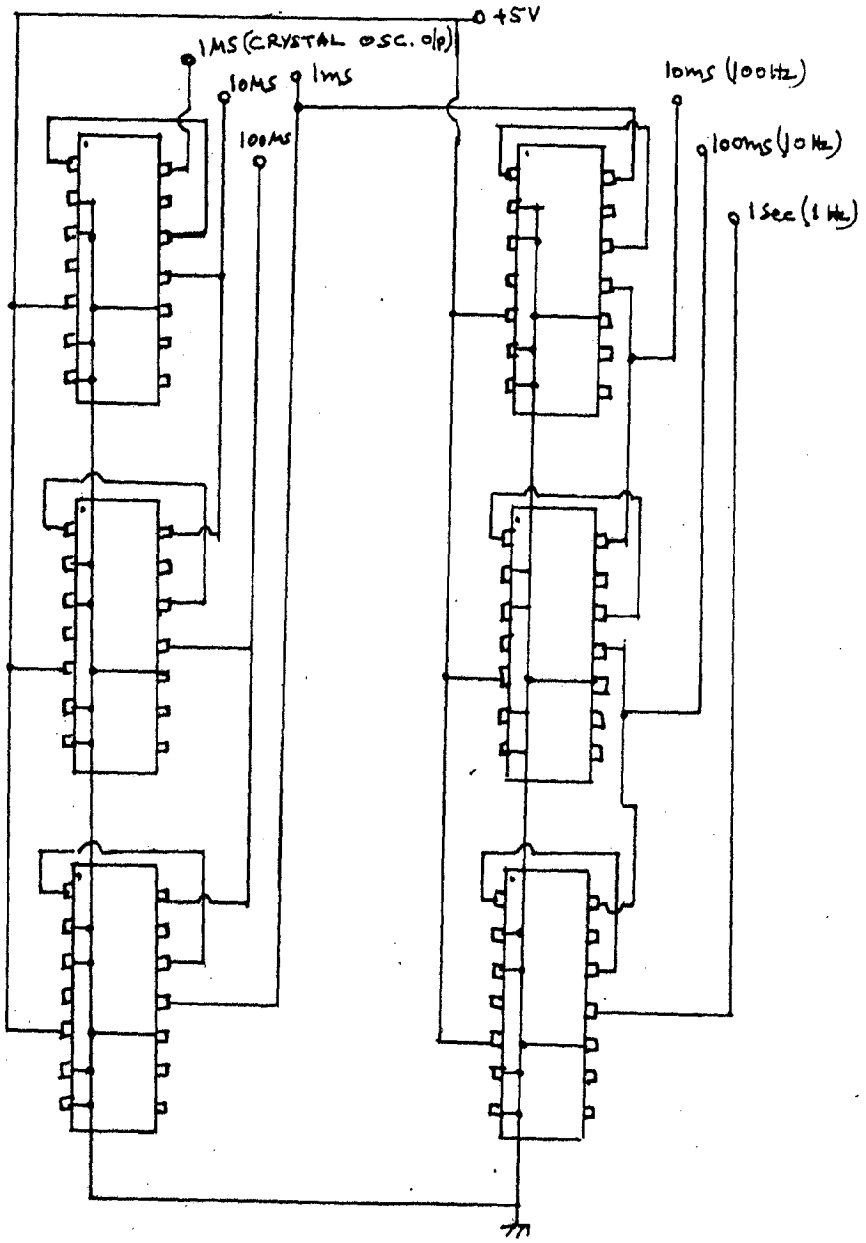


FIG. (5.3.a) FREQUENCY DIVIDERS.

ALL IC's are (SN7490.)

5.3 - Divide by 10 Units:

As Crystal Oscillator cricuit has been fabricated using TTL IC SN7400. TTL divide by 10 I.C.(SN7490) can be used as divide by 10. Since the Oscillator frequency is 1MH$_z$, 5 or 6 SN7490 I.C. will be required to get 10H$_z$ or 1 H$_z$ signal respectively. 10H$_z$ reference signal can be used to give COUNT, RESET and LATCH signal by using circuit . shown in Fig.(5.4-a) A PCB of this with six cascaded SN7490 has been fabricated and tested.

5.4 COUNT RESET AND LATCH TIMING:

The circuit shown in Fig.(5.4-a) is used for proper sequence of COUNT, RESET and LATCH timing signals from the 10H$_z$ reference. The IC SN 7493 divides the 10H$_z$ reference by 12 to control COUNT gate, the RESET gate and the LATCH gate. It can be seen from the timing diagram Fig.(5.4-b) that the RESET gate output first is at logic 1 for 0.5Sec. then the COUNT gate is enabled for 1 sec., allowing the unknown input frequency to pass through.

Finally the LATCH gate is disabled to freeze the display until the next cycle is completed. A PCB of this circuit has been fabricated and tested. All the three signals COUNT, LATCH and RESET are present.

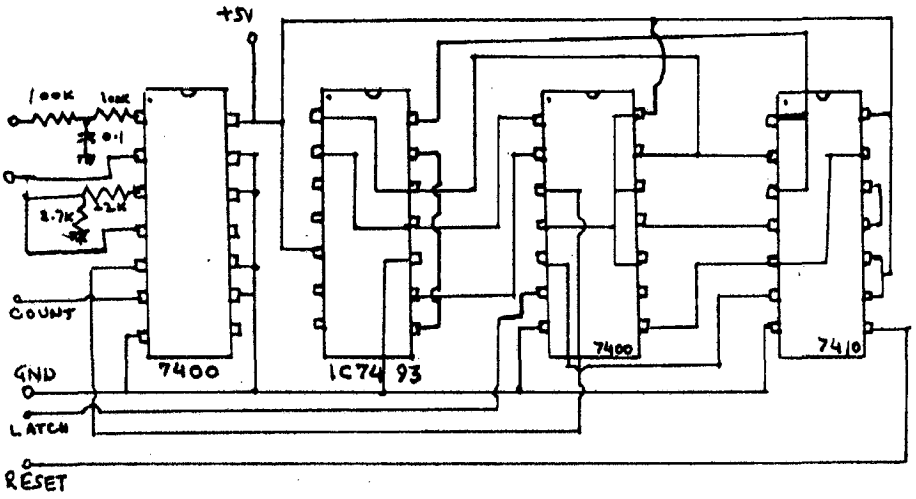


FIG.(5.4.a) SIGNALS FOR COUNT, LATCH, RESET.

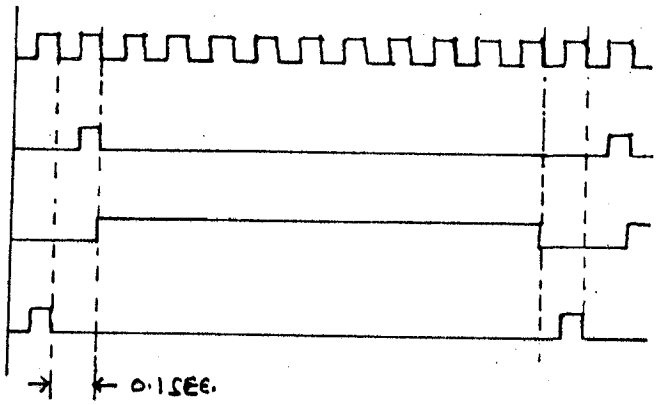


FIG.(5.4.b) TIMING DIAGRAM.

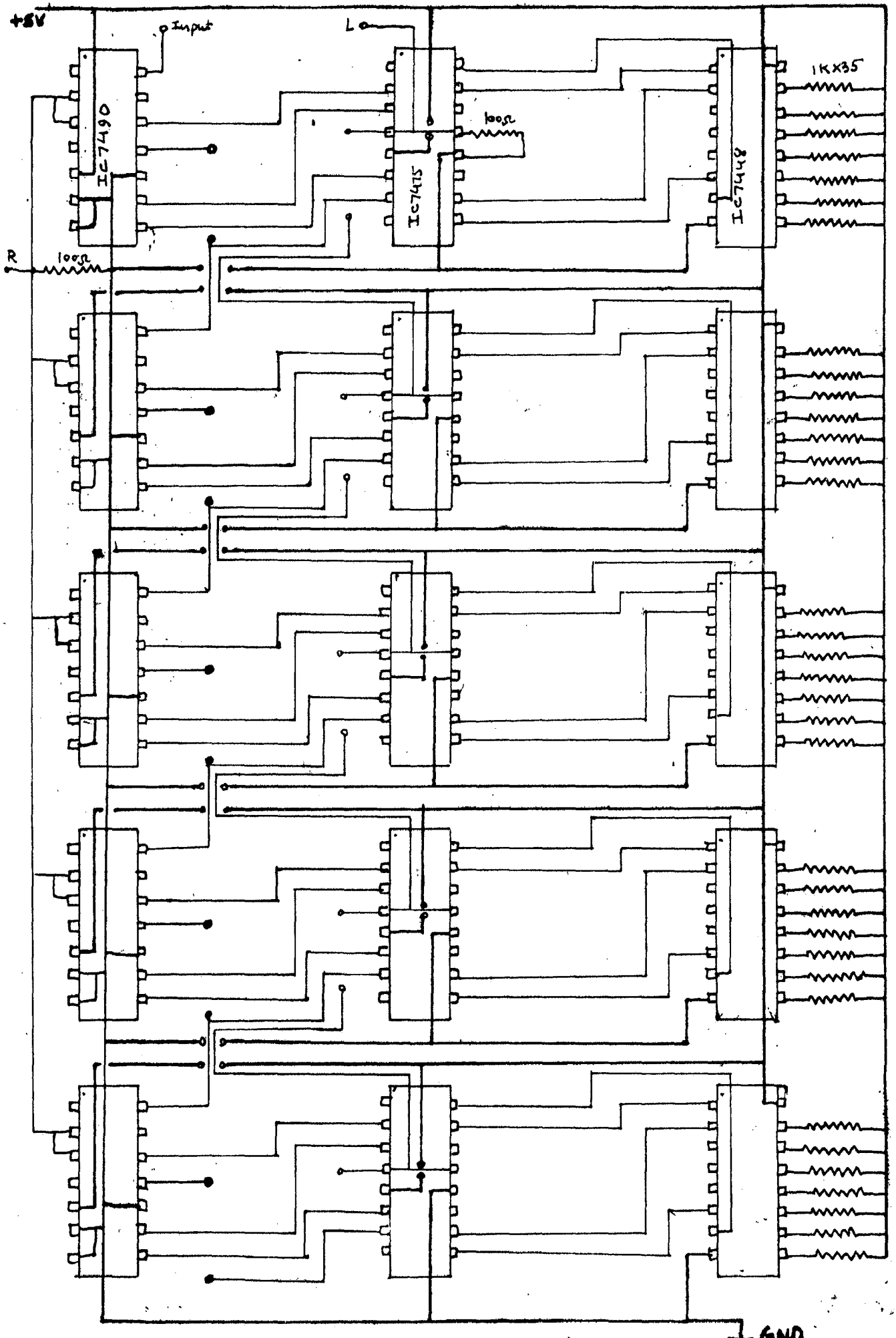


Fig. (5.5.a) Counter, Latch & Display circuit

5.5 COUNT LATCH AND DISPLAY DECADES:

The counter LATCH and Display circuit of Fig.(5.5-a) is a five decade display. A decimal is adjusted at second phase from the left to get maximum display of 99.999 H_z.

The arrangement is a straight forward approach IC 7490 is a decade counter with four outputs. These four outputs are connected with 4D-Flip Flop(Latch) and output of those Flip-Flops is connected to 4-7 sequent decoder. Those 7 output of decoder are connected to seven diodes of seven segment LED. Fig.5.5-b shows the pin connections of IC's used. A PCB of this circuit was fabricated with five SN 7490, five ISN7475 and five SN7448 and five seven segment LED's.

5.6- STANDARD FREQUENCY SOURCE:

A 555 timer circuit is used as Astable multivibrator' this astable multivibrator is so designed so as to give $1KH_z$-6 KH_z frequency output in six ranges i.e. $1KH_z$, $2KH_z$, $3KH_z$, 4 KH_z, $5KH_z$, $6KH_z$,. This output is connected to a series of IC7490$ casceded as divide by the each. So that final output of this circuit is $1\text{-}6H_z$ in step of $1H_z$.

The value of resistance can be calculated from the following formula:

$$f = \frac{1.433}{(R_1+2R_2)C}$$

A PCB is fabricated and tested to have this range of input.

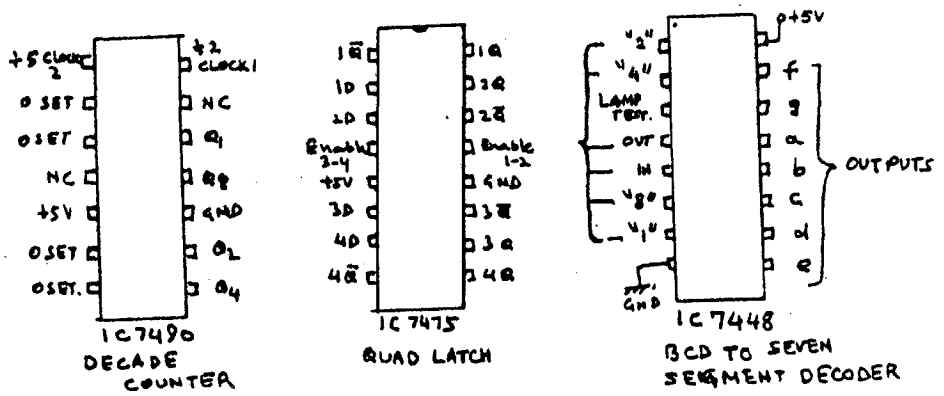


FIG. (5.5.b) PIN CONNECTIONS OF 7490, 7475, 7448 IC's.

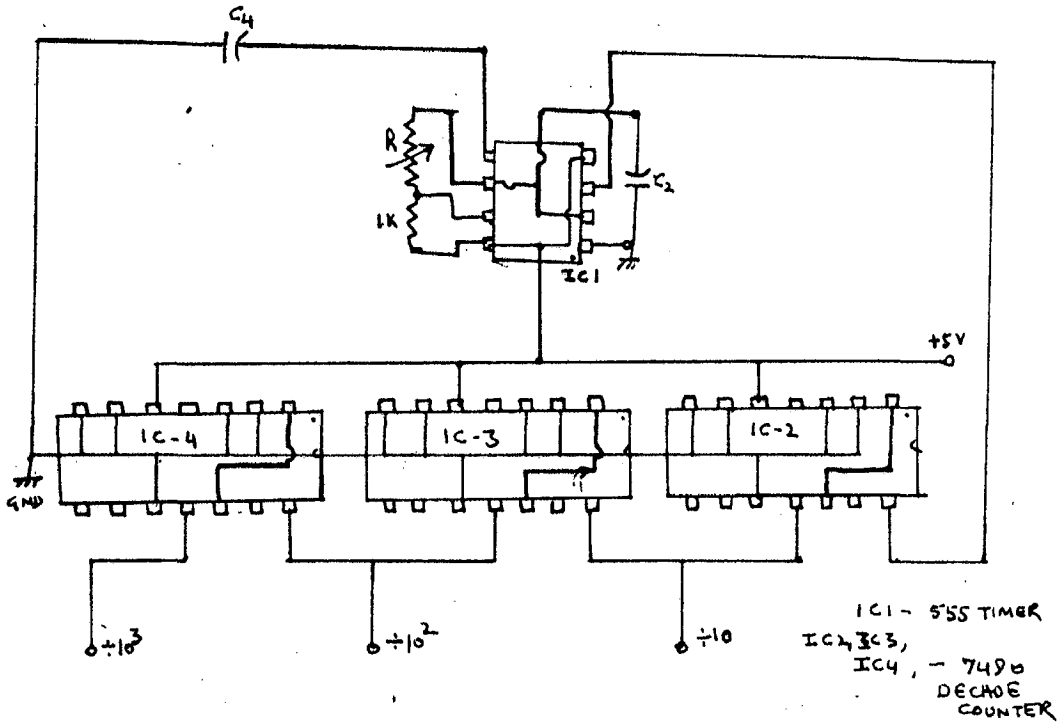


FIG. (5.6.a) STANDERD FREQUENCY SOURCE.

5.7- Frequency Multiplier:

Here is a popular digital PLL 16 pin IC CD4046 is used. Fig(5.7-a). It consists of a low power, linear voltage controlled oscillator (VCO), and two different phase comparators having a common signal input amplifier and a common comparator input. A 5.2 V-Zener diode is provided for supply regulation if necessary. The CD 4046 is supplied in a 16 lead dual in time ceremic package, plastic package flat-package or in chip form also.

VCO Section:

The VCO requires one external capacitor C_1(between pins 6 and 7) and two external resistors R_1 and R_2 at pin 11 and 12 respectively). The R_2 determines the amount of offset required for VCO. It frequency is to be varied from zero to maximum range i.e.no offset is required. The pin 12 can be left open i.e. $R_2 = \infty$.

The high input impedance ($10^{12}\Omega$) of the VCO simplifies the design of low pass filters as designer is having a wide choice of resistor to capacitor ratios. In order not to load the low pass filter, a source follower output of the VCO input voltage is provided at pin 10(DEMODULATED OUTPUT). If this pin is used, a load resistor (R_s) of 10KΩ or more should be connected from this point to V_{SS} (4 ND). If unused this terminal should be left open. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. A full COS/MOS logic swing is available

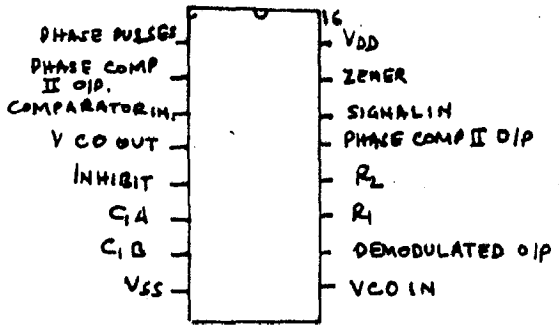


FIG.(5.7.a) TOP VIEW : CD4046. (PLL)

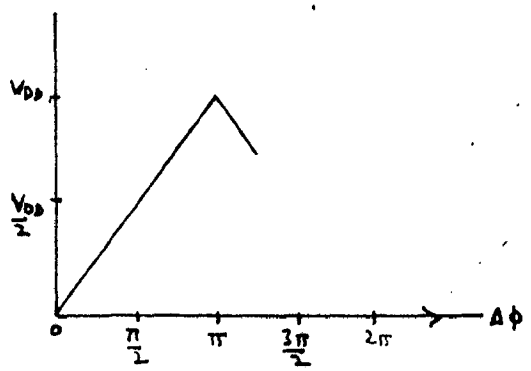


FIG.(5.7.b) PHASE TO OUTPUT RESPONSE CHARACTERSTICS.

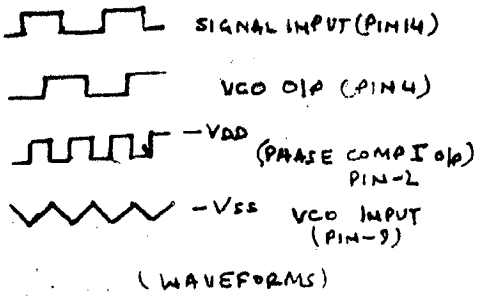
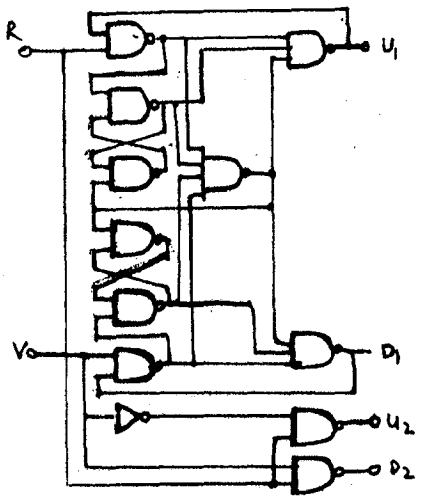


FIG.(5.7.c) PHASE COMPARTOR I CHARACTERSTICS.



FIG(5.7.d) CIRCUIT DIAGRAM OF PHASE DETECTOR II

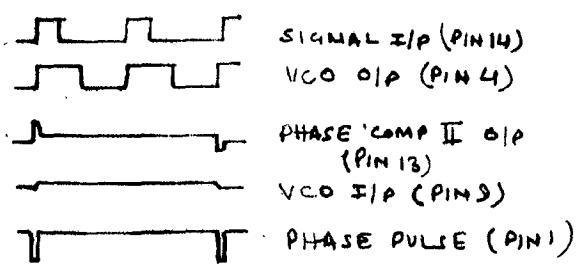


FIG.(5.7.e) PHASE COMP. II WAVEFORMS

at the output of the VCO and allows direct coupling to COS/MOS frequency dividers such as the RCA-CD 4024, CD4018, CD-4020, CD4022, CD4029, and CD 4059. One or more CD4018 (Presettable divide by N Counter) or CD4029 (Presettable UP/Down counter), or CD4059A programmable divide by 'N' counter), together with the CD4046 PLL IC can be used to build a micropower power low frequency synthesizer. A logic 0 on the INHIBIT input "enables" the VCO and the source follower, while, a logic 1 "terms Off" both to minimize standby power consumption.

Phase Comparators:

The phase comparator signal input (terminal 14) can be directly coupled provided the signal swing is within COS/MOS logic levels [logic "0" ≤30% (V_{DD} V_{SS})Logic "1" ≥70% (V_{DD}-V_{SS})] For smaller swings the signal must be capacitively coupled to the to the self biasing amplifier at the signal input.

The phase comparator 1 is an exclusive OR network; it operates analogously to an overdriven balanced mixer. To maximize the lock range, the signal and comparator input frequencies must have 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to $V_{DD}/2$. The low pass filter connected to the output of phase comparator I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the centre frequency (f_o).

The frequency range of input signals on which the PLL will lock, if it was initially out of lock, is defined as the

frequency capture range ($2f_c$). The frequency range of input signals on which the loop will stay locked, if it was initially in lock, is defined as the frequency lock range($2f_2$). The capture range $\leq$ the lock range.

With phase comparator 1 the range of frequencies over which the PLL can acquire lock (capture range)is dependent on the low pass filter characteristics, and can be made as large as the lock range. Phase comparator 1 enables a PLL system to remain in lock inspite of high amount of noise in the input signal. Or- one characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to VCO centre frequency. A second characteristic is that the the phase angle between the signal and the comparator input varied between 0° and 180° and 90° at the Centre frequency. The Fig.(5.7-b) shows the phase to output response characteristics of phase comparator 1. The typical waveforms for a COS/MOS PLL employing phase comparator I locked condition of f_o is shown in Fig.(5.7.C).

Phase comparator-II is an edge controlled digital memory network (Fig.5.7-d). It consists of four flip flop stages, control gating and a three state output ciruit comprising p- and n- type drivers having a common output node. When the p-mos or n-mos drivers are ON they pull the output upto V_{DD} or down to V_{SS}, respectively. This type of phase comparator acts only on the positive edges of the signal and comparator inputs. The duty cycle of the signal and comparator inputs are not important since positive transitions control the PLL

system utilizing this type of comparator:-

1) If the signal input frequency is higher than the comparator input frequency, the p type output d iver is maintained ON most of the time, and both n and p drivers OFF (3 state) the reminder of the time.

2) If the signal input frequency is lower than the comparator input frequency, the n type output driver is maintained ON most of the time, and both the n and p drivers OFF(3state) the remainder of the time.

3) If the signal and comparator input frequencies are the same, but the signal input lags the comparator input in phase, the n type output driver is maintained ON for a time corresponding to the phase difference.

4) If the signal and comparator input frequencies are the same, but the comparator input lags the signal in phase the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the capacitor voltage of the low pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At the comparator inputs are equal in both phase and frequency. At this stable point both p and n type output drivers drivers remain OFF and thus the phase comparator output becomes an open circuit and holds the voltage on the capacitor of the low pass filter constant.

Moreover, the signal at the phase pulses " output is a high level which can be useo for indicating a locked condition. Thus, for phase comparator-II, no phase differenceexists between signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the low pass filter is reduced when this type of phase comparator is used because both the p and n type output drivers are off for most of the signal in-put cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low pass filter. With no signal present at the signal input, the VCO is adjust is adjusted to its lowest frequency for phase comparator-II. The Fig.(5.7-e) shows typical waveforms for phase comparator-II in a locked condition.

D E S I G N -

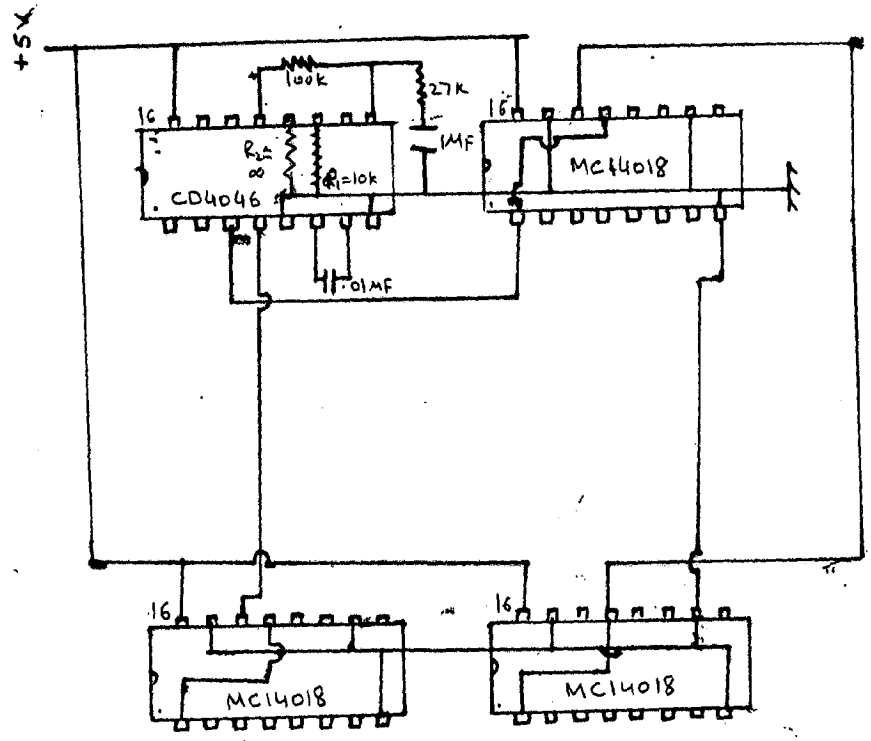
Let VCO is oscillating at f_o frequency. If this frequency divided by N such that f_o/N and f_{in} (unknown signal) be compared. Here N = 1000 is taken, also f_{in} is 1-6H_z therefore, VCO must be able to oscillate at 1-6 KH_z frequency, not only this it must be able to lock the frequency, of input signal. Therefore I.C.CD4046 is used as PLL with the following components value:-

$$f_{min} = \text{zero}$$

$$f_{max} = 8\ KH_z$$

$$f_o = \frac{f_{max}}{2} = 4\ KH_z$$

So keeping C_1 = .01 uF and R_1 = 10K



FIG(5.7.4) FREQUENCY MULTIPLIER CIRCUIT

FILTER DESIGN -

The output of the comparator is filtered by low pass filter such that it should be lessthan cut off frequency of the filter. If the difference of input frequencies to the comparator is too large. The resultant signal may be too high to be passed by the filter.

Though the simple RC filter can be used as low pass filter but for faster locking process lag lead type filter is used.

Keeping -

$\tau_1 = (R_1 + R_2)$ = τ_1 = (100K+27K) X1uF

= 127 ms

$w_1 = \frac{1000}{127}$ = 7.84 rad/sec.

= 27K X 1 uF = 27 ms

$w_2 = \frac{1000}{27}$ = 37 rad/sec.

A PCB of this circuit was fabricated and tested. The IC's used for frequency division is CD4018(which is presettable, divide by 10 counter). This ICccan be used with any division factor upto ten.

5.8 POWER SUPPLY UNIT -

A stablized power supply regulated with IC 723 has been fabricated for approximate load current of 2.0 Amp. Fig.(5.8-a) shows the circuit used.

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CHAPTER-6

RESULTS

Table 6-1 shows the results obtained from the meter:

TABLE-6-1

THEORETICAL	PRACTICAL
6	6.086
5	5.084
4	4.065
3	3.065
2	2.112
1	1.134.

The inaccuracies obtained are due to the tolerance of the components.

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C H A P T E R -7

CONCLUSIONS AND SCOPE OF FURTHER WORK

A frequency meter has been developed to measure frequency in the range of 1-6 H_z. Here square wave input is used but that does not restrict use of other waveforms. Any waveform can be used in such type of circuit.

The following are the salient features of the meter:

1- The crystal used for crystal Oscillator has given very stable output.

2- The accuracy of the circuit is upto the third place of decimal.

3- The circuit is not expensive as it requires only one PLL I.c, few divide by ten I.C.(Hire-3) as extra in conventional frequency comparision scheme.

4- The multiplying circuit is quite simple and requires few resistances and capacitances only.

5- The power supply used does not contain any ripple.

The following changes can be made in order to modify the circuit:-

1- The counting and display circuit could be well replaced by ZN1040E or TIL 306 I.Cs.

2- The crystal Oscillator and divider circuits can be well merged into one IC chip circuit only if CMOS IC (CD 4020, CD4040 or CD 4060) is used instead of TTL IC.

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