ULTRA-LOW POWER FLIP-FLOPS USING CLOCK GATING AND SINGLE PHASE QUASI-STATIC ENERGY RECOVERY LOGIC

A DISSERTATION

Submitted in partial fulfillment of the requirements for the award of the degree of

MASTER OF TECHNOLOGY

in

ELECTRONICS AND COMMUNICATION ENGINEERING

(With Specialization in Microelectronics and VLSI Technology)

By

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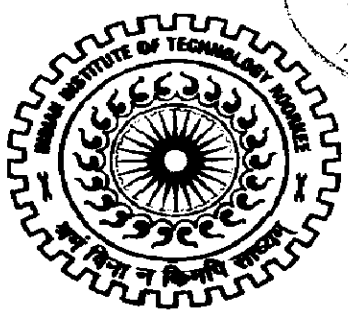

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JUNE, 2011

CANDIDATE'S DECLARATION

I hereby declare that the work, which is being reported in this dissertation report, entitled **"Ultra-Low Power Flip-Flops Using Clock Gating And Single Phase Quasi-Static Energy Recovery Logic"**, is being submitted in partial fulfillment of the requirements for the award of the degree of **Master of Technology** in **Microelectronics and VLSI Technology**, in the Department of Electronics and Computer Engineering, Indian Institute of Technology, Roorkee is an authentic record of my own work, carried out from June 2010 to June 2011, under guidance and supervision of **Dr. Ashok Kumar Saxena,** Professor and **Dr. Sudeb Dasgupta**, Assistant Professor, Department of Electronics and Computer Engineering, Indian Institute of Technology, Roorkee.

The results embodied in this dissertation have not been submitted for the award of any other Degree or Diploma.

Date : 29/06/2011
Place : Roorkee

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CERTIFICATE

This is to certify that the statement made by the candidate is correct to best of my knowledge and belief.

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ACKNOWLEDGEMENT

At the outset, I express my heartfelt gratitude to Dr. Ashok Kumar Saxena and Dr. Sudeb Dasgupta, Department of Electronics and Computer Engineering at Indian Institute of Technology Roorkee, for their valuable guidance, support, encouragement and immense help. I consider myself extremely fortunate for getting the opportunity to learn and work under their able supervision. Working under their guidance will always remain a cherished experience in my memory and I will adore it throughout my life.

My sincere thanks to the faculty of Microelectronics and VLSI Technology group, Department of Electronics and Computer Engineering at Indian Institute of Technology Roorkee, for the technical knowhow and analytical abilities they have imbibed in us which have helped me in dealing with the problems I encountered during the thesis.

I want to thank each member of my beloved joint family for their love and support, without which I wouldn't have made it this far in my academic career.

I am thankful to all Ph.D. scholars specially, Jitendra Kanungo, of Microelectronics and VLSI Technology group and the VLSI Lab staff for their help in learning different tools and my friends, who have graciously applied themselves to the task of helping me with ample morale support and valuable suggestions.

Finally, I would like to thank all my batch-mates, my seniors and friends at Ravindra Bhawan of IIT Roorkee, whose constant presence made my work enjoyable.

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ABSTRACT

In this work, we considered circuit level techniques for low energy computation using the principles of adiabatic and clock gating technique. This work presents ultra low power clock gating adiabatic D flip-flop, SR flip-flop and JK flip-flop using single phase sinusoidal power clock adiabatic scheme. Proposed flip-flops are realized with clock gating and single phase Quasi-Static Energy Recovery Logic in TSMC 90nm CMOS technology. In the previously proposed QSERL, two phase sinusoidal power clocks were used that required overhead of multiple clock generator circuit. In this work, single phase QSERL is used to reduce loss in the circuit. The proposed clock gating technique works efficiently for adiabatic flip-flops during idle periods to reduce undesired dynamic power dissipation. All the simulations have been performed using 90nm CMOS technology CADENCE spectre simulator. The use of clock gating and adiabatic technique simultaneously saves power dissipation of around 80% over conventional static CMOS technique at 100MHz.

The 4-bit shift register has been designed using proposed single phase QSERL D flip-flop and compared with the conventional static CMOS 4-bit shift register circuit. The clock gating QSERL shift register can save approximately 82% of power dissipation over conventional CMOS shift register at 100MHz.

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CHAPTER 1

MOTIVATION OF THESIS

1.1 Introduction

Power dissipation has become a critical issue in high performance application, especially in portable and battery operated ASIC systems [1]. With technology scaling, the impact of power dissipation is expected to gain significance. In order to minimize the power dissipation, research at various levels of design, abstraction has been started and achieved ultra low power with optimum performance.

The dynamic energy dissipation in a circuit is due to charging and discharging for its node capacitance. The charging and discharging paths are different, causing energy to be dissipated in the form of heat. An adiabatic switching technique reduces the dynamic energy dissipation by recycling the charge stored in the node capacitance in circuits. This recycling is achieved by using an AC power source instead of the traditional DC power source. The energy dissipation is reduced by maintaining a very low potential difference across the two terminals of turn-on MOS transistors [2, 3].

In the widely used static CMOS circuits, negligible dynamic power loss occurs as long as input signal does not switch. But, clock generator circuit continuously provides clock signal resulting in dynamic power dissipation. The clock gating is most efficient way to reduce power dissipation in clock generator circuit. This technique detaches the clock generator circuit from the logical circuit when this circuit is idle. It also reduces the load on clock generator circuit. However, in adiabatic circuits, energy dissipation occurs even for constant input signals since their output nodes are always charged and discharged by their power clocks [4]. Similar to power gating and clock gating techniques of conventional CMOS

circuits, adiabatic units can also be shut down by switching off their power clocks to reduce energy loss during idle periods. Several clock gating schemes for adiabatic circuits have been proposed and achieved considerable energy savings [5].

It is reported that, previously described clock gating adiabatic flip-flop is designed using the multi-phase clock schemes. This report presents clock gating flip-flops using single-phase quasi-static energy recovery scheme. Basic flip-flops have been designed using adiabatic logic, clock gating technique and to achieve ultra low power circuit both techniques have been used simultaneously.

1.2 Thesis Organization

Chapter 2 presents a brief overview of adiabatic logic, clock gating, quasi-static energy logic and proposed technique

In chapter 3, implementation of D flip-flop, SR flip-flop, JK flip-flop and shift register using proposed technique are presented along with the simulation results. These results are compared with conventional static CMOS method to show power efficiency of the circuit.

Chapter 4 presents design of shift register using proposed D flip-flop with simulations results. All simulations have been done on 90nm CMOS technology CADENCE spectre simulator.

Finally, conclusions and recommendations for future work are outlined in chapter 5.

CHAPTER 2

ADIABATIC LOGIC

2.1 Overview

Interest in low energy is growing as the cost of power dissipation becomes preposterous. It is desirable to restore the delivered energy back to the power supply for effective energy management. Adiabatic computing is an attractive approach from this point of view. In recent years, several adiabatic logic families have been proposed for low power systems. In order to realize a complete system such as a microprocessor, it is necessary to use large macro blocks as building blocks. The flip-flops are one of the most useful in digital circuits. An adiabatic flip-flop offers low power and direct interface to other adiabatic circuit families as well.

Most research has focused on building adiabatic logic out of CMOS. However, current CMOS technology, though fairly energy efficient compared to similar technologies, dissipate energy as heat, mostly when switching. In order to solve this problem, there are two fundamental rules CMOS adiabatic circuits must follow. The first is never to turn on a transistor when there is a voltage difference between the drain and source. The second says never to turn off a transistor that has current flowing through it [3].

CMOS transistors dissipate power when they switch. The main part of this dissipation is due to the need to charge and discharge the gate capacitance C through a component that has some resistance R. The energy dissipated during charging of the gate is

$$E = \frac{RC}{T} CV^2 \qquad (2.1)$$

where T is the time it takes the gate to charge or discharge. In non-reversible circuits, the charging time T is proportional to RC. Reversible logic uses the fact that a single clock cycle is much longer than RC and thus attempts to spread the charging of the gate over the whole cycle and thus reduces the energy dissipation. In order to extend the charging time of the gate we make sure never to turn on a transistor that has a potential difference between source and drain, and furthermore, once the transistor is turned on, energy flows through it in a gradual and controlled manner.

The second rule that adiabatic circuits must follow is never to turn off a transistor when there is current flowing through it. The reason for this follows from the fact that transistors are not perfect switches going from on to off instantly. Instead, it gradually changes from on to off when the gate voltage changes. Furthermore, the change is proportional to the speed at which the gate voltage changes. A fact when combined with the previous constraint, implies that the transistor is in an "in between" state for a long period of time. During this time, the voltage drop across the transistor greatly increases yet the resistance is not high enough to bring power dissipation to zero.

Adiabatic Charging (AC) and Energy Recovery (ER) are two circuit methods used to reduce the energy dissipation by the system. Typically these techniques are most effective at reducing dissipation for charging high capacitance loads or loads that require high voltage. Other load types can usually be charged more efficiently by employing voltage-scaling techniques [1].

2.2 Energy-Dissipation

Energy dissipation is calculated for three different charging sources: a conventional step, a ramp, and a sinusoidal. To evaluate the theoretical efficiency of a waveform shape for charging a capacitive load, the simple RC circuit charged by a voltage source is examined in Fig.2.1.

The energy being drawn from the voltage supply is

$$E_s = \int_0^\infty V_s(t)\, I_s(t)\, dt \qquad (2.2)$$

The energy delivered to the capacitor is

$$E_s = \int_0^{\infty} V_c(t)\, I_c(t)\, dt \tag{2.3}$$

which is always equal to $\frac{1}{2}CV^2$ if the capacitor charged from ground to V. Therefore, the energy dissipated in the resistor, E_{diss} is

$$E_{diss} = E_s - E_c = E_s - \frac{1}{2}CV^2 \tag{2.4}$$

$$E_{diss} = \int_0^{\infty} I_s^2\, R\, dt \tag{2.5}$$

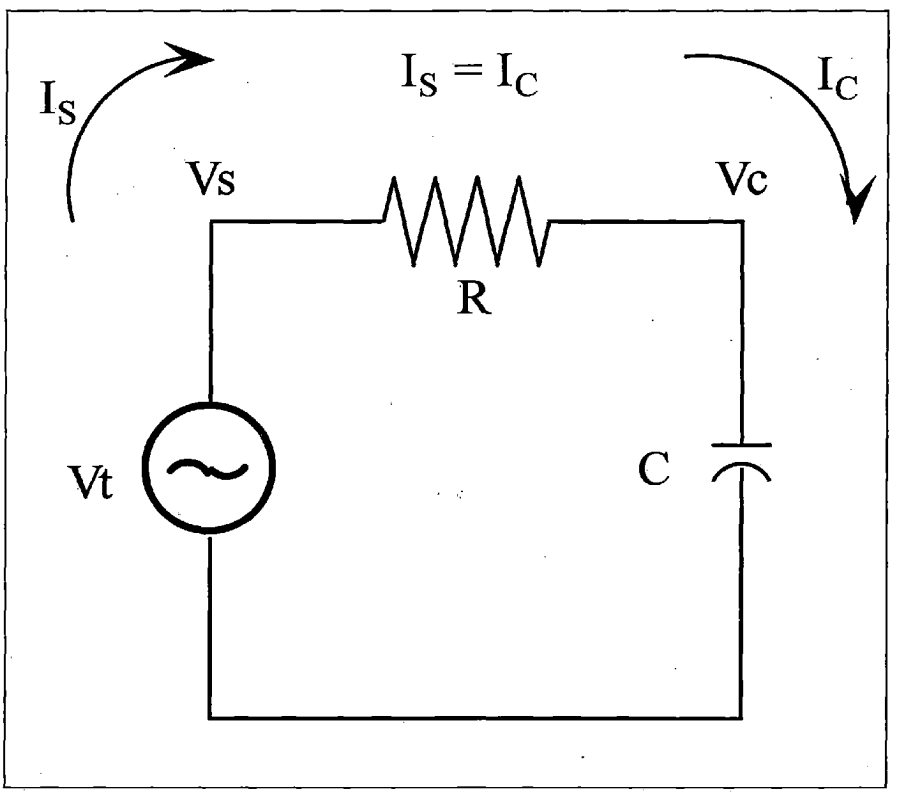

Fig. 2.1: Simple RC circuit

In Fig. 2.1, if we apply charging source to RC circuit which is step waveform varying from 0 to V_{dd}, then initially voltage at V_s=0 and V_c=0. Then if we apply step input, it varies from 0 to V_{dd} in one step so the voltage at V_s=V_{dd} and capacitor opposes sudden changes, hence voltage at V_c is still zero and starts charging slowly. So at this point, the voltage difference across resistance is V_{dd} and current is flowing through the resistance. Hence power dissipation is equal to $\frac{1}{2}CV^2$.

If the charging source is linear ramp varying slowly from 0 to V_{dd} over time interval 'T', where T is very much greater than time constant RC, then initially the voltage at V_s and V_c equal to zero. And if we apply a linear ramp which rises slowly from 0 to V_{dd}, then voltage at V_s and V_c also starts rising. This means the voltage across capacitor exactly follows the input voltage and at any point of time, the voltage difference across resistor is very small or ideally zero. Hence the power dissipation is small which is $\frac{RC}{T}CV^2$ and ideally it is zero.

The charging source is sinusoidal wave adjusted to resonate between 0 and V_{dd} volts with a charging time of T. It has been used in place of a linear ramp because it is simple to generate with a resonating inductor and capacitor circuit, then power dissipation becomes $(\pi^2/8)(RC/T)CV^2$. That is, the sine wave is much more efficient than a step input if period is sufficiently slow, but only 81% efficient compared to a ramp with same rise time. Hence sine wave, easier to generate, is more efficient than the step but less efficient than the ramp.

2.3 Conventional Charging and Adiabatic Charging

Adiabatic charging is achieved when a charging waveform is more efficient than $\frac{1}{2}CV^2$ such as with the ramp or sine wave. Energy recovery is achieved when some of the $\frac{1}{2}CV^2$ of energy stored on the charged capacitive load is recovered and reused for later charging. In order to evaluate the merits of AC and ER, a comparison is made to conventional charging and discharging methods using Equations 2.2 through 2.5.

Conventional charging, also known as switching method, is used by standard CMOS gates. To charge a load to a voltage, the load is connected through a resistive switch to a voltage source that is biased at V. To discharge a load to ground, it is connected through a resistive switch to the ground node. These transitions can be modelled as step inputs because the

transition times of the switch input are smaller than the RC time constant of the switch and load.

In this conventional charging example,

- When charging a load with a step input, a large voltage drop across the resistor results in energy dissipation as heat equal to $\frac{1}{2}CV^2$. In addition $\frac{1}{2}CV^2$ has been transferred to the capacitor.
- When discharging the load with a step input, again there is a large voltage drop across the resistor and the $\frac{1}{2}CV^2$ that was stored on the capacitor is dissipated. Here, the entire CV^2 that began in the voltage supply has been dissipated as heat in the resistor [2].

A similar procedure is applied to a charge and discharge cycle of adiabatic charging. A linear ramp is used (in place of dc supply) for the adiabatic source. The ramp transition time (t_c) must be much larger than the RC time constant of the load and switch resistance.

- When the load is charged slowly by the ramp, the dissipation in the resistor is $\frac{RC}{t_c}CV^2$, which less than the charging case. However, just as in the conventional case, $\frac{1}{2}CV^2$ is transferred to the capacitor. If the ramp transition time is infinitely long, then $\frac{RC}{t_c}$ is approximately zero and only $\frac{1}{2}CV^2$ is drawn from the voltage supply.

- When discharging the load slowly with a ramp input, again there is a small instantaneously voltage drop across the resistor, so the dissipation in the resistor is $\frac{RC}{t_c}CV^2$. The capacitor begun with $\frac{1}{2}CV^2$ and only $\frac{RC}{t_c}CV^2$ is dissipated in the resistor, so $\left(\frac{1}{2}-\frac{RC}{t_c}\right)CV^2$, is returned to the supply.

A typical voltage supply will shunt any returned energy to ground, dissipating it across some resistance and rendering an adiabatic discharging no more energy efficient than the conventional case. However, if the supply is a resonant source, it will be able to reclaim the returned energy and use it for subsequent charging.

Typically, energy recovery has some overhead either in the form of increased circuit complexity or power supply complexity. In addition, the requisite adiabatic charging time is slower than combinational switching, so the system must usually be designed around the adiabatically charged nodes. Thus, energy recovery is often only used when the $\frac{1}{2}CV^2$ of the load is a significant percentage of system energy dissipation. It is often simpler to reduce the voltage, V, or reduce the switched capacitance, C, in order to save power. However when the limits of C and V have been reached (or they are fixed), adiabatic charging and energy recovery can be powerful technique for reducing the dissipation below $\frac{1}{2}CV^2$.

2.4 Adiabatic Logic Families

Adiabatic logic, which utilizes AC power supplies to recycle the energy of node capacitance, is a promising low power design approach. Over the past decade, several adiabatic logic families, such as PAL-2N, ECRL , 2N-2N2P , CPAL etc, were proposed and achieved considerable energy savings over conventional CMOS ones. However, these circuits require multi-phase AC power-clocks. The problems of multi-phase clocking schemes include the complicated clock tree, clock skew, and multiple power-clock generators that increase more energy dissipation. Moreover, adiabatic circuits with multi-phase power-clocks require insertion of some buffers in circuits for maintaining proper pipeline operation, which cause extra energy dissipation and area overhead.

Over the past decade, several memory designs based on adiabatic logic, such as ECRL (efficient charge recovery logic), PAL-2N (pass-transistor adiabatic logic with NMOS pull-down configuration), and CPAL (complementary pass-transistor adiabatic logic) etc, have been reported and achieved considerable energy savings over conventional CMOS ones.

A few adiabatic logic families using a single-phase power-clock have been reported, which have easier generator. TSEL and SCAL circuits use a single-phase power-clock, but the additional reference voltage and current increase the design complexity, since they are difficult to design due to the optimal value of reference voltage concerning about clock frequency. The CAL (Clocked Adiabatic Logic) circuits can also use a single-phase power-clock by introducing an auxiliary clock signal. Because of the simple structure, CAL circuits are easy to design for realizing complicated circuits. However, the auxiliary clock signal doesn't work in an adiabatic manner, resulting in large energy loss because of large switching capacitance on auxiliary clock lines. QSERL scheme is very simple similar to static CMOS logic. But this is two phase adiabatic process. This scheme can be made simpler by removing one phase supply of previously reported design. This proposed circuit will also be suitable to work with clock gating technique which is explained in next chapter.

2.5 An Overview of Quasi-Static Energy Recovery Logic (QSERL)

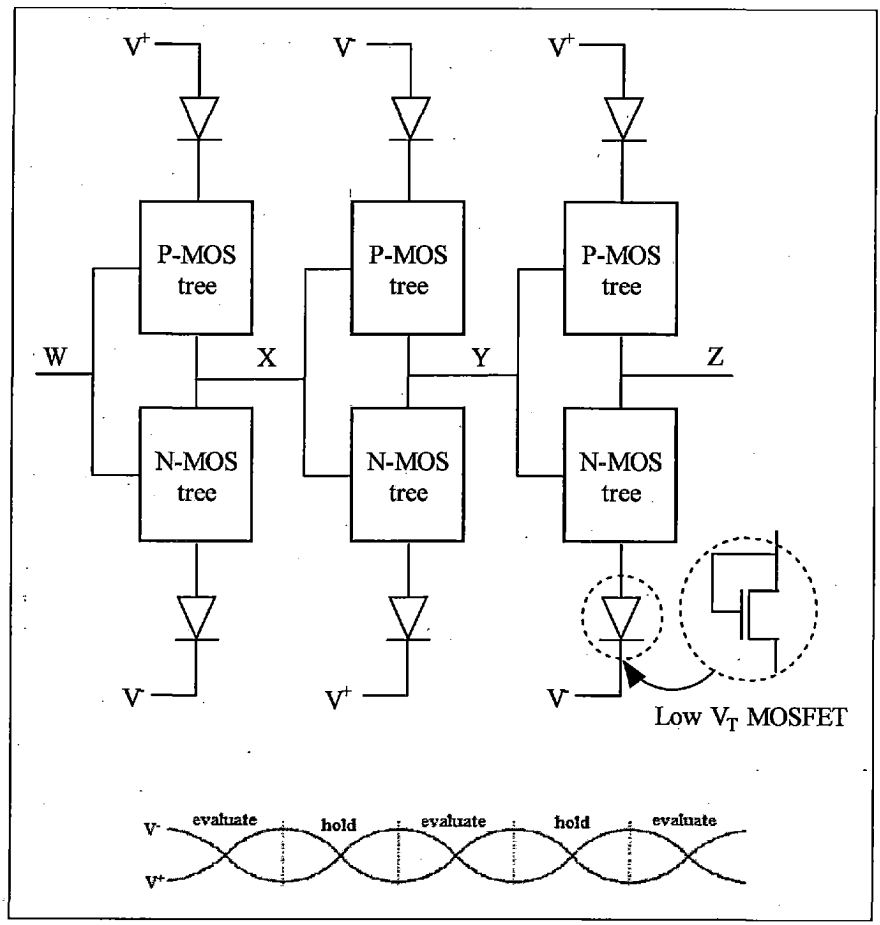

Fig. 2.2: Two-Phase QSERL [6]

Here V^+ is φ and V^- is $\bar{\varphi}$.

QSERL scheme is shown in Fig. 2.2 that resembles the static CMOS logic. QSERL uses two additional diodes and two sinusoidal clocks in complementary phases. Hence it is called as 2-phase QSERL. In this technique instead of ground one ac sinusoidal supply in series with diode is used which is in complementary phase with upper sinusoidal voltage supply. The diode on the top of PMOS tree controls the charging path, while other diode at the bottom of NMOS tree controls the discharging path. Note that cascaded gates are in alternate phases. The second gate in Fig. 2.2 evaluates its logic while first one is in hold phase [6, 7].

Consider the case of cascaded inverters connected in series. Now consider the case that φ is increasing and $\bar{\varphi}$ is decreasing, diode connected at the top of PMOS will be forward biased and diode connected at bottom of NMOS will be reverse biased. Suppose initially input is switching from logic '1' to logic '0', PMOS of first stage will get turned-on and output will follow φ supply. But there will be some threshold drop from V_{DD} to $V_{DD} - V_T$ for logic '1' as diode is connected. Where V_T is threshold voltage of diode. Now for second stage as input is rising so NMOS of this stage will get turned-on and PMOS will get turned-off. But for this case only upper diodes are on and lower are off, so this second stage will not change its state or we can say it is at hold state.

Now consider the case when φ is decreasing and $\bar{\varphi}$ is increasing, diode connected at top will get reverse biased and diode connected at bottom will be forward biased.. So second stage will be at evaluate phase and first stage will be at hold phase. Hence output of this stage will be logic '0'. But instead of ground sinusoidal supply is connected so output will follow φ. Here logic '0' will not be at zero voltage but it will be slightly higher than threshold voltage due to diode drop. Therefore in 2-phase QSERL output will swing from V_T to $V_{DD} - V_T$. Hence alternate phases will be at evaluate phase and next alternate phase will be at hold phase.

MOSFETs with gate and drain shorted having low-threshold voltage can be used instead of diodes used for controlling the charging and discharging paths. It has advantage of increasing speed of circuit as MOSFET has highest switching speed. Also we can obtain lower threshold MOSFET which results in lower power dissipation across it.

2.6 Clock Gating

Energy recovery technique is originally developed for low power digital circuits. It achieves low power dissipation by restricting current across devices with low voltage drop and by recycling energy stored on load capacitors by using an AC supply voltage. Major portion of total power dissipation in synchronous systems is on the clock circuit. Hence clock gating is the most efficient technique to reduce power dissipation in clock generator circuit [8-10].

In static CMOS circuits, negligible dynamic power loss occurs as long as input signal does not switch. But, clock generator circuit continuously provides clock signal resulting in dynamic power dissipation. The clock gating is most efficient way to reduce power dissipation in clock generator circuit. This technique detaches the clock generator circuit from the logical circuit when this circuit is idle. However, in adiabatic circuits, energy dissipation occurs even for constant input signals since their output nodes are continuously charged and discharged by their power clocks [4]. Similar to power gating and clock gating techniques of conventional CMOS circuits, adiabatic units can also be shut down by switching off their power clocks to reduce energy loss during idle periods. This work presents clock gating flip-flops using single-phase quasi-static energy recovery scheme.

When input signal is not changing i.e. logical circuit is idle, clock generator circuit continuously provide clock to logical circuit which results in loss of power. Clock gating is one of the most efficient way to reduce power dissipation in the clock generator circuit. It detaches clock generator circuit from logical circuit during idle periods.

Here clock of an adiabatic circuit is synchronized with the clock generator circuit. But the frequency of adiabatic clock circuit is kept around four times or more as that of clock generator circuit. So that all operations of adiabatic circuit should be done during required clock period of signal and input signal is reliably sampled at the output.

When output of logical circuit is changing its state from logic '0' to logic '1', we can see that pull-up network of p-MOS is on and voltage drop across it is almost zero. Clock signal of adiabatic circuit has just started rising when logical circuit is triggered so there will be zero voltage drop across pull-up transistors and hence power dissipation is zero while output signal is switching from logic '0' to logic '1'. Also we can say that logical circuit is following adiabatic logic. In an adiabatic circuit when output is at logic '1', charge stored at output node is continuously recovered by the supply ac battery. As we have introduced both

techniques i.e. adiabatic and clock gating simultaneously, charge stored at output node will not be recovered by an ac supply since output has been detached from ac supply using clock gating technique. So while switching logic '1' to logic '0' at the output node, logical circuit will not work adiabatically and there will be large voltage drop across pull-down network which results in power dissipation. Hence in 2-phase QSERL, it is worth to use 2 phases of the supply. It will be advantage to use only one phase. Hence one supply with diode place at the bottom of circuit is removed to reduce extra power loss.

2.7 Proposed Single Phase QSERL

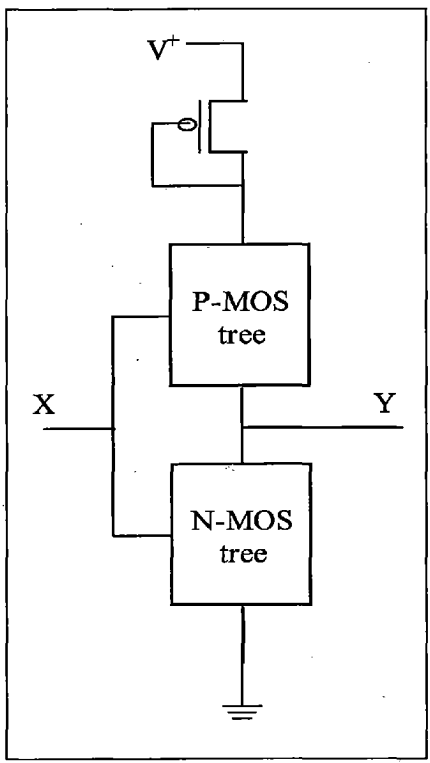

Fig. 2.3: Proposed Single-Phase QSERL

The QSERL as shown in Fig. 2.2 uses two phase power clocks in which output voltage does not gain full voltage swing i.e. 0 to V_{DD}. However the problems of multi-phase clocking adiabatic circuits include clock skew, complicated power clock tree and multiple power clock generators, which results in extra area overhead and increase in the complexity of the layout place and route [11]. There is V_T threshold drop from upper as well as lower side in output voltage in QSERL which results in output swing from V_{DD}-V_T to V_T. In this work, single-phase QSERL circuit (Fig.2.3) is used that avoids overhead of multi-phase power clock generator circuit and hence reduces power dissipation. In single phase QSERL, one power clock with NMOS transistor placed at the bottom has been removed. It results in increase in output voltage swing i.e. from 0 to V_{DD}-V_T. An advantage of this circuit is that it increases output voltage swing and also reduces power dissipation.

When output of logical block is switching from logic 0 to logic 1, voltage across turned-on PUN is zero or minimum. So minimum power is dissipated while switching from logic '0' to logic '1'. But for logical switching from logic '1' to logic '0', it will not work adiabatically. Therefore this single phase QSERL is quasi-adiabatic circuit.

In static CMOS circuit, dynamic loss does not occur as long as input signal is constant. But in adiabatic circuits, there will be continuous dynamic power dissipation even for constant input signal because energy stored at output node is continuously being recovered [12-16]. So to avoid this loss, an adiabatic logic block should be detached from energy recovery supply. One PMOS transistor is introduced to detach logic block from energy recovery supply when input signal is not changing.

2.8 Single Phase Power Clock Generator Circuit

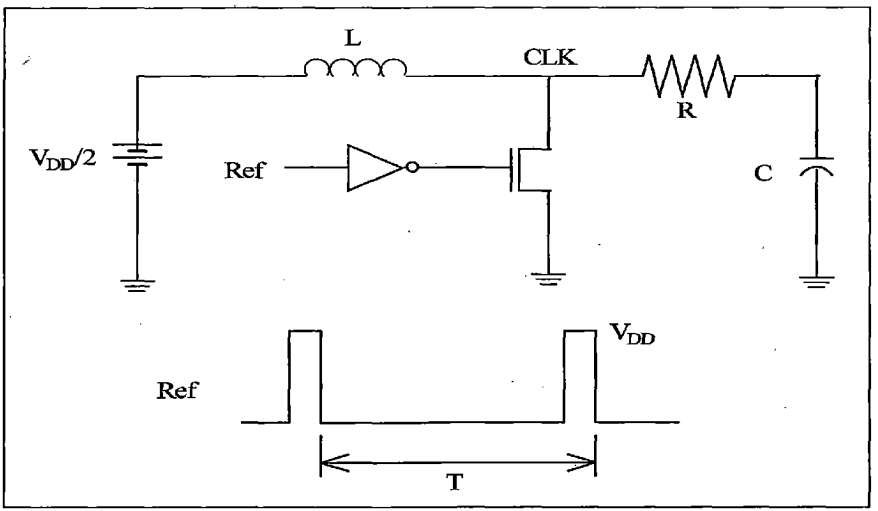

Fig. 2.4: Resonant energy recovery power clock generator circuit [18, 19]

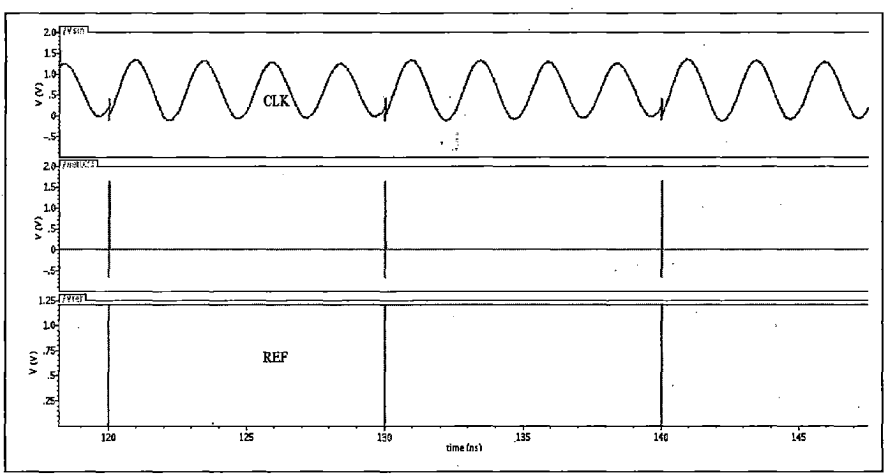

Fig. 2.5: Output waveform of power clock generator circuit

The energy recovery power clock generator circuit is a single phase resonant clock generator as shown in Fig. 2.4 [18, 19]. A reference signal is applied to NMOS transistor. Transistor pulls clk to ground when the reference signal reaches its minimum value, thereby maintaining the oscillations of the resonant circuit. This size of transistor is large and hence driven by the chain of progressively sized inverters. The natural oscillating frequency of this oscillating circuit is given by

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{2.6}$$

where C is the total capacitance connected to the clock-tree including parasitic capacitances of the clock-tree and gate capacitances associated with clock inputs of all flip-flops. In order to have an efficient clock generator, it is important that the frequency of the reference (REF) signal be the same as the natural oscillation frequency of the resonant circuit [18]. In order to calculate the value of capacitance C, first with a given value of inductor L and with the REF signal at zero, the whole system, including the flip-flops, is simulated. The clock signal shows a decaying oscillating waveform settling down to $V_{DD}/2$. From this waveform, the natural decaying frequency is measured, and then by using Equation 2.6, the value of C is calculated. Having the value of C, the value of L for the frequency of 400 MHz can again be determined from Equation 2.6.

Obtained output waveform of power clock generator circuit having frequency of 400MHz with R, L and C are 1.25KΩ, 40.7μH and 3.5fF respectively is shown in Fig. 2.5. Power consumption of the resonant energy recovery clock generator circuit is calculated for different loads which are mentioned in Table 2.1. It is observed that with increase in load capacitance of the clock generator circuit, power consumption of circuit will also increase. Hence it is necessary to reduce load capacitance of clock generator circuit which is done by gating method, so that it can drive maximum circuit with less power dissipation. In the next section, we have calculated power consumption for different flip-flops which does not include the power consumption of resonant energy recovery clock generator circuit.

Table 2.1: Power consumption of clock generator circuit for different load

Inductor (μH)	Load Capacitance (fF)	Power Consumption (nW)
142.5	1	263
57	2.5	271
28.5	5	277
19	7.5	290
14.25	10	296

CHAPTER 3

FLIP FLOP DESIGN

3.1 Introduction

In digital circuits, a flip-flop or latch is a circuit that has two stable states and can be used to store state information. These two states are logic '1' and logic '0'. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. Flip-flops and latches are a fundamental building block of digital electronics systems used in computers, communications, and many other types of systems. To reduce power consumption of digital system, it is necessary to reduce power dissipation of basic flip-flops.

Flip-flops and latches are used as data storage elements. Such data storage can be used for storage of state, and such a circuit is described as sequential logic. When used in a finite-state machine, the output and next state depend not only on its current input, but also on its current state (and hence, previous inputs). It can also be used for counting of pulses, and for synchronizing variably-timed input signals to some reference timing signal.

Flip-flops can be either simple (transparent or opaque) or clocked (synchronous or edge-triggered). The simple ones are commonly called latches. Latches are level triggered also we called it as transparent latch. Output will change its state only when clock is at logic '1'. Flip-flops are edge triggered. It will change its output state only when it senses edge of clock signal. The word latch is mainly used for storage elements, while clocked devices are described as flip-flops.

Flip-flops can be divided into common types: the D ("data" or "delay"), SR ("set-reset"), T ("toggle"), and JK types are the common ones. The behaviour of a particular type can be described by what is termed the characteristic equation, which derives the "next" (i.e., after the next clock pulse) output, Q_{next}, in terms of the input signal(s) and/or the current output, Q.

3.2 D-Flip Flop

3.2.1 Introduction

The D flip-flop shown in Fig. 3.1 is the most common flip-flop in use today. It is better known as data or delay flip-flop (as its output Q looks like a delay of input D). D flip-flop consists of two latches and pass-transistor MOS logic is used to design it. The Q output takes on the state of the D input at the moment of a positive edge at the clock pin (or negative edge if the clock input is active low). Since the output takes the value of the D input or data input, and delays it by one clock cycle hence it is called as D flip-flop. The D flip-flop can be interpreted as a primitive memory cell, or delay line. Whenever the clock pulses, the value of Q_{next} is D otherwise it holds its previous state Q_{prev}.

Clock gating method can be used in D flip-flop to reduce load on clock circuit. The reliable D flip-flop is realized using clock gating and single phase QSERL method simultaneously which is shown in Fig. 3.2. Clock gating method is implemented using comparator and gating circuits. In D flip-flop, comparator includes XOR gate which compares *D* and *Q*, while the gating logic includes simple AND gate at the input of which *ck* signal and comparator output is applied.

Comparator circuit continuously compares input data with output, if both data are same then it will not trigger D flip-flop. But if both signals are different then it will make output of comparator high. This high signal is applied to gating circuit, if *ck* is high then it will trigger to D flip-flop.

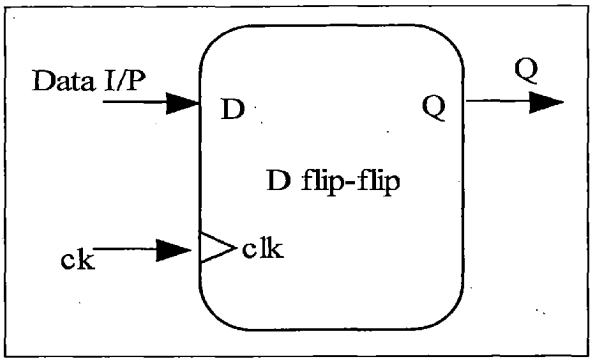

Fig. 3.1: D flip-flop

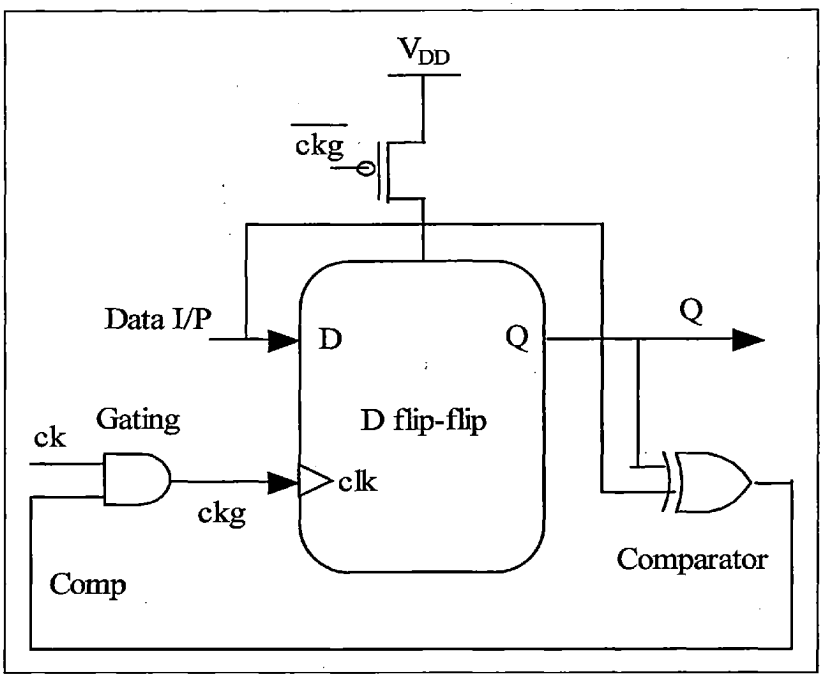

Fig. 3.2: D flip-flop with clock gating

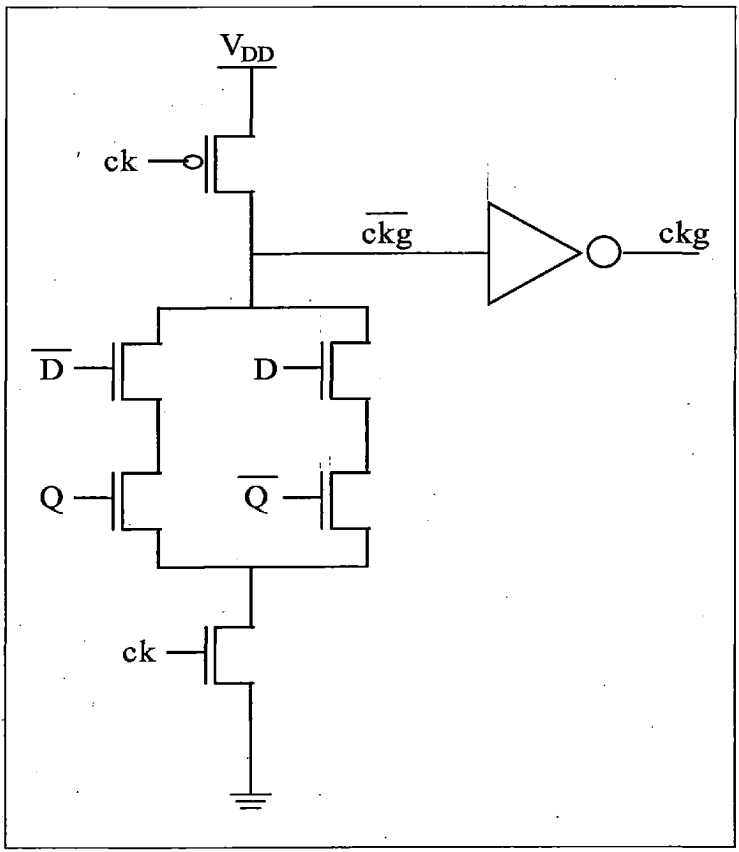

Fig. 3.3: NC²MOS gating for negative edge triggered D flip-flop [8]

When *ck=0*, node $\overline{ckg}$ is pulled high. During the subsequent high level of the *ck* signal, two different situations are possible [7].

As *D* is different from *Q*, *comp* becomes equal to 1 and node $\overline{ckg}$ is pulled down. Afterward when *ck* goes to 0, a positive edge of $\overline{ckg}$ is produced.

Suppose *comp* is always equal to 0 and *ck=1*, $\overline{ckg}$ node is not pulled down and hence no active edge of *ck* is produced even when *ck* goes to 0. For *ck=1* and *comp=0* the gating logic is in a memory state.

As D flip-flop consist of two latches, so clock gating technique can be divided into two types. They are

1) Double Clock Gating and
2) NC^2MOS Clock Gating

In double clock gating technique, two gating techniques are used for two different latches in D flip-flop whereas in NC^2MOS clock gating technique, only one gating method is used for both latches. So numbers of transistors required for double gating are more as compared to NC^2MOS gating. Power dissipation curve with switching activity rises rapidly for double gating as compared to NC^2MOS gating [8]. Hence double gating requires large circuit and dissipates more power as compared to NC^2MOS gating technique. Hence it is advantage to use NC^2MOS gating technique.

In this work, NC^2MOS Gating is used which uses only one gating logic for the whole flip-flop and hence reduces the gating logic overhead. The schematic of NC^2MOS gating logic for negative edge triggered flip-flop is shown in Fig. 3.3. The structure uses a pull-up net, for $\overline{ckg}$ node, realized by only one PMOS driven by *ck* signal. In this way only the clock *ck* and not *comp* can drive negative edge on *ckg*, so that the flip-flop can be activated only by *ck*.

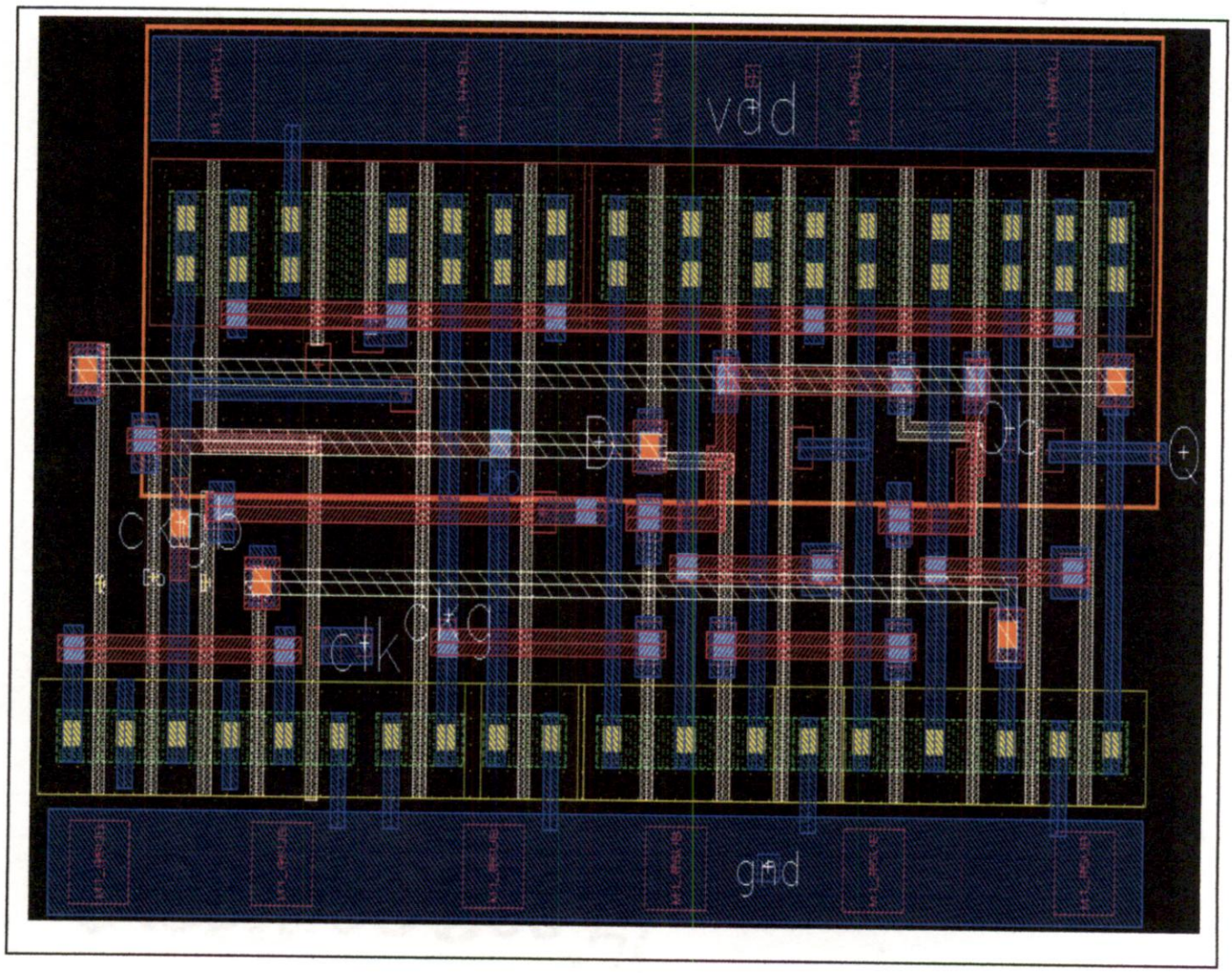

Fig. 3.4: Layout of clock gating single phase QSERL D flip-flop

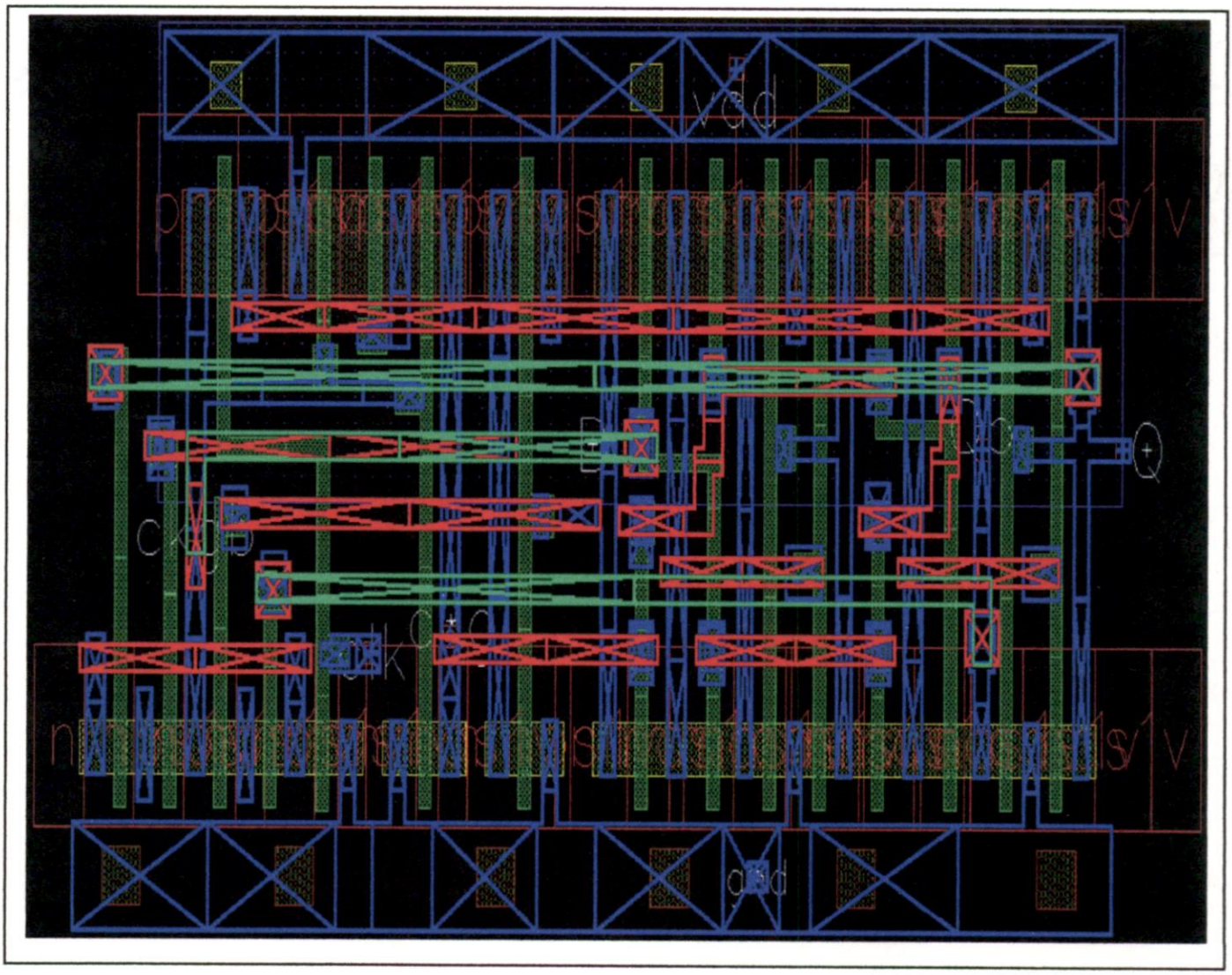

Fig. 3.5: RCX extracted view of clock gating single phase QSERL D flip-flop layout

The schematic for positive edge triggered flip-flop is quite similar. The difference is in pull-down net, which is composed of a single NMOS driven by *ck* and in the pull-up net which presents two series PMOS, one driven by *ck* and other by $\overline{comp}$ [8].

Above explained gating method was for clock generator circuit. Same gating method can also be used for power supply of D-ff. PMOS transistor is connected between power supply and inverters of D-ff which acts as gating for power supply. Output of clock gating circuit i.e. $\overline{ckg}$ is connected to the gate of this PMOS transistor. So this PMOS switch is turned-on only when D-ff is triggered by clock gating circuit.

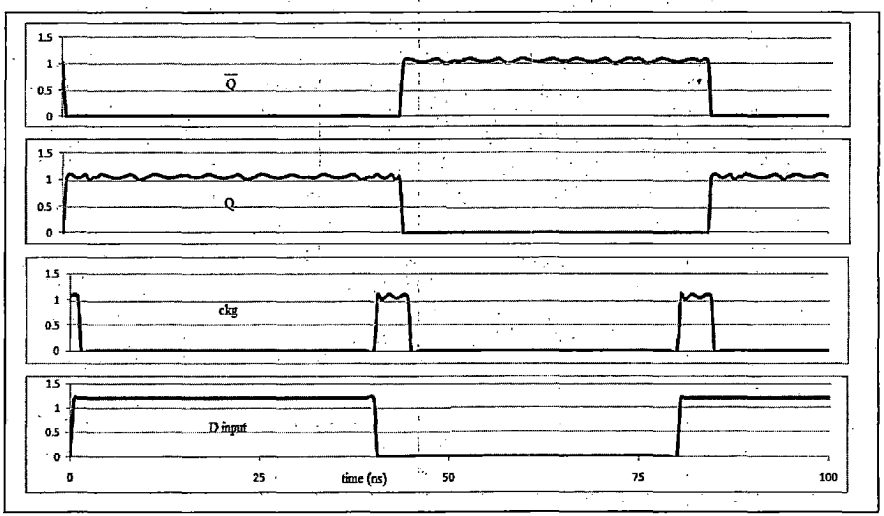

Fig. 3.6: Simulated waveform of clock gating single phase QSERL D flip-flop

3.2.2 Simulations and Results:

Layout of clock gating adiabatic D flip-flop and its RCX extraction is shown in Fig. 3.4 and Fig. 3.5. Fig. 3.6 shows the simulated output waveform of single phase QSERL clock gating D flip-flop. From output waveform it is observed that logic '1' is somewhat lower than V_{DD} i.e. lower by threshold of PMOS as it is working as diode. Also it is observed that logic '1' is somewhat sinusoidal which is due to linear operation of PMOS. Voltage applied at the gate of PMOS is not equal to V_{DD} but is lower than threshold voltage hence this PMOS is operating in linear region or we can say that it is lightly on.

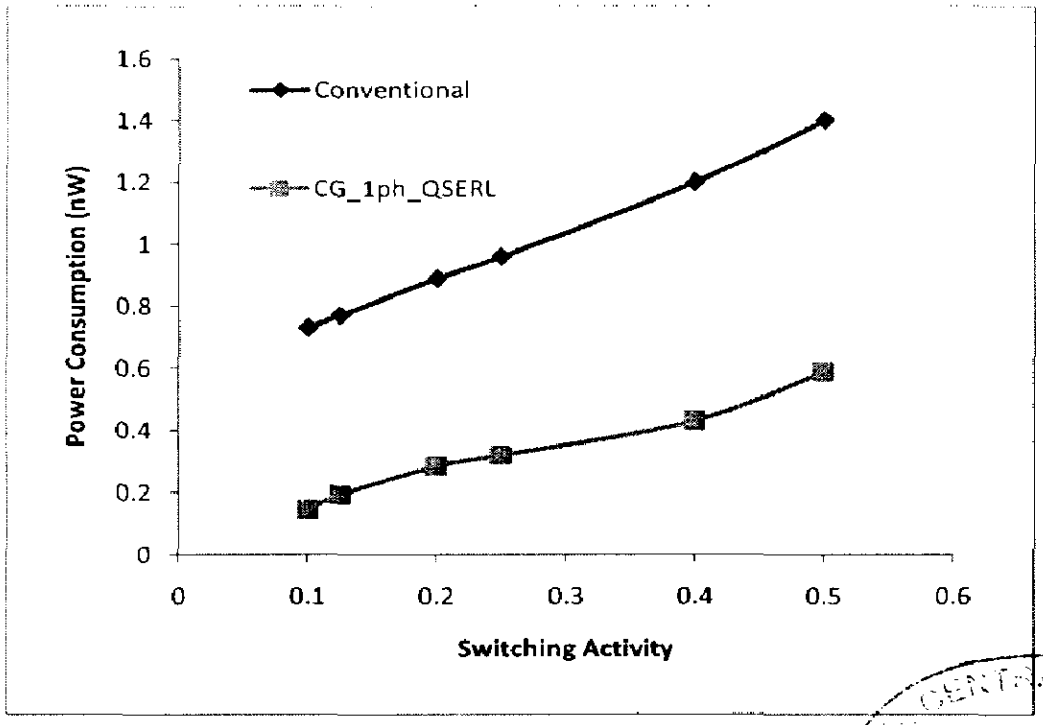

Fig. 3.7(a): For clock supply

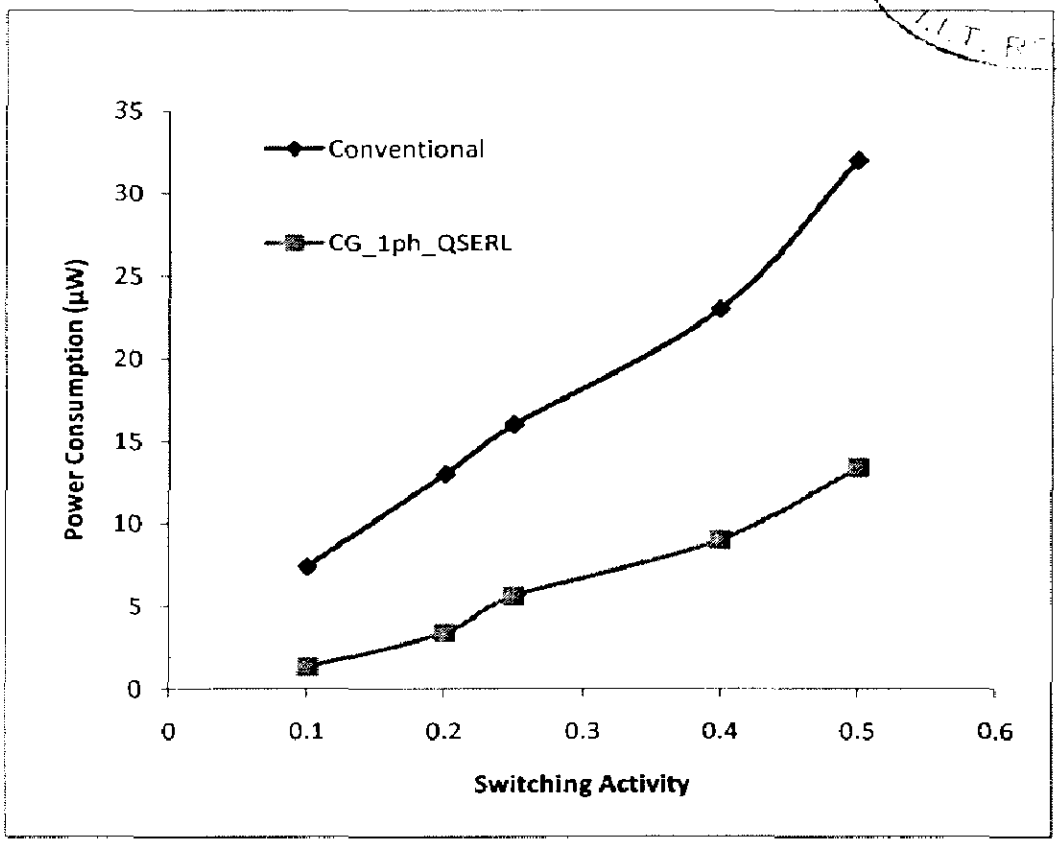

Fig. 3.7(b): For power supply

Fig. 3.7: Power consumption as a function of input switching activity for D-ff at clock frequency of 100MHz

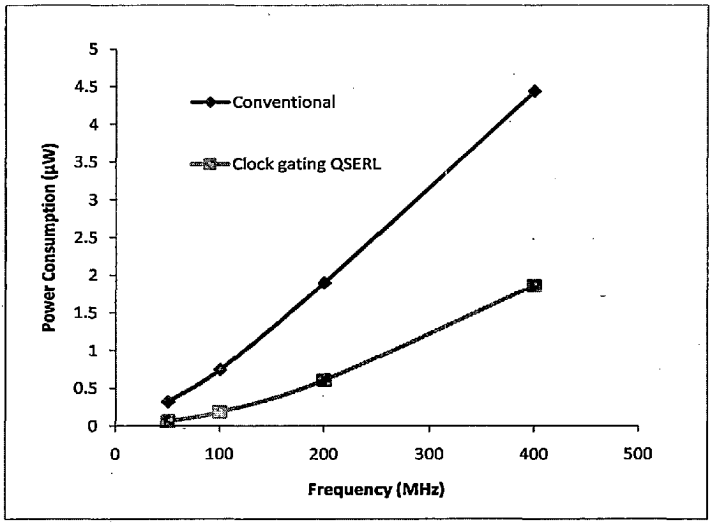

Fig. 3.8(a): For clock supply

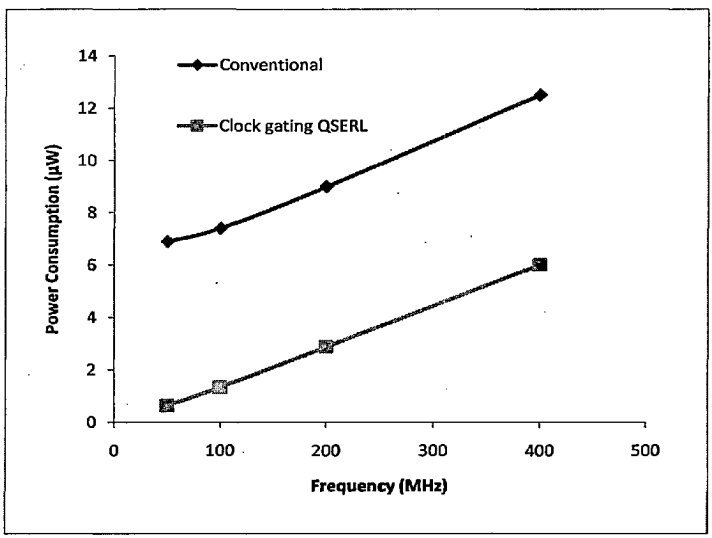

Fig. 3.8(b): For power supply

Fig. 3.8: Power consumption of D-ff as a function of frequency at switching activity of 0.1

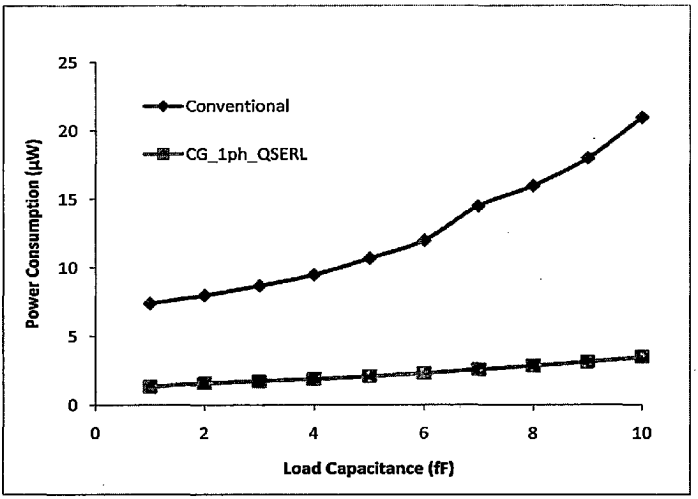

Fig. 3.9: Power consumption for different load at switching activity of 0.1

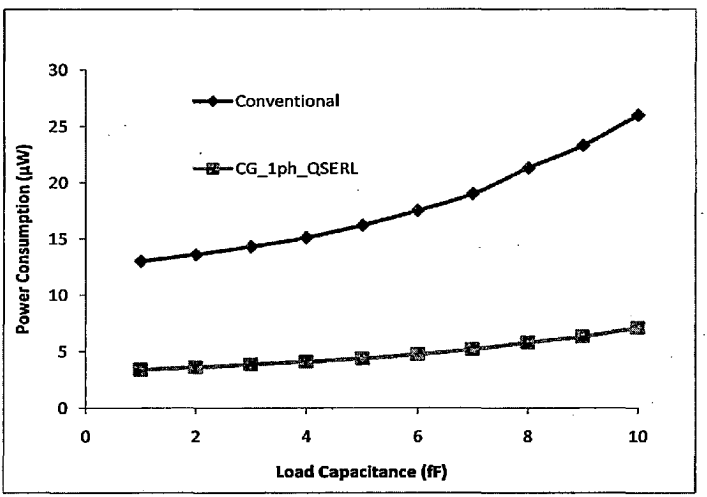

Fig. 3.10: Power consumption for different load at switching activity of 0.2

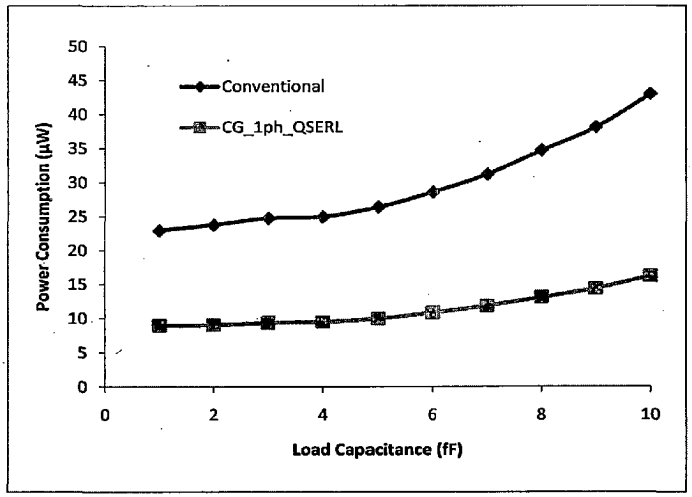

Fig. 3.11: Power consumption for different load at switching activity of 0.4

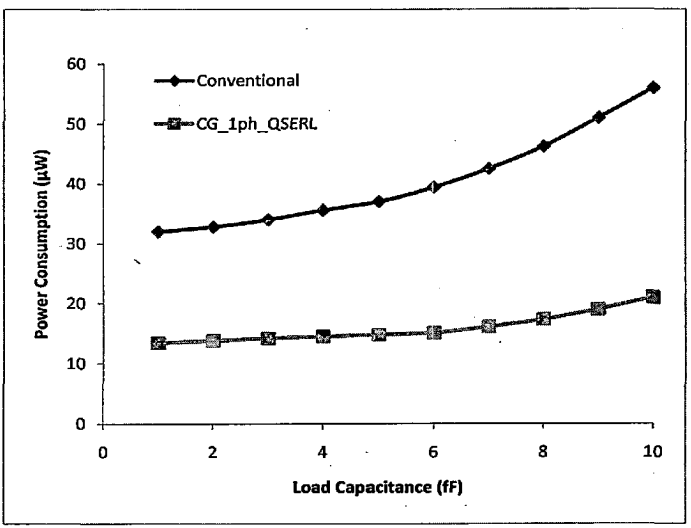

Fig. 3.12: Power consumption for different load at switching activity of 0.5

Table 3.1: Power consumption at switching activity = 0.5 and C_L = 5fF

Clock Frequency (MHz)	Conventional Static CMOS (µW)	Clock Gating 1ph-QSERL (µW)	Adiabatic Gain
50	33	13.5	2.44
100	37	14.8	2.5
200	42	17	2.47
300	49	20.1	2.45
400	59	25	2.36

Table 3.2: Power consumption at switching activity = 0.5 and f = 400MHz

Load Capacitance (fF)	Conventional Static CMOS (µW)	Clock Gating 1ph-QSERL (µW)	Adiabatic Gain
1	46	20	2.3
3	51	22	2.32
5	59	25	2.36
7	70	30	2.33
10	85	38	2.24

Power consumption comparison between conventional D flip- flop and clock gating QSERL D flip-flop method with operating frequency and switching activity of the circuit is shown in Fig. 3.7 and Fig. 3.8 respectively. If we increase the load capacitance of the circuit then power consumption of power clock supply will also increases and its graph for different switching activity is also shown in Fig. 3.9-3.12. Gap between the plotted line of conventional and clock gating QSERL method is increasing which is clearly observed in graphs. In adiabatic circuit, this gap reduces with increase in frequency and after a particular frequency both lines get crossed. This is because power dissipation of adiabatic circuit is more at higher frequency as compared to conventional CMOS method i.e. for higher frequencies adiabatic circuit will not be useful. It is worth to use adiabatic logic for the circuit having higher operating frequency.

Table 3.1 and 3.2 shows the power consumption of power clock supply of circuit of conventional static CMOS and clock gating single-phase QSERL circuit at the load capacitance of C_L = 5fF and input clock frequency of 400MHz respectively at 50 % switching activity. In this table adiabatic gain has also been calculated which is equal to ratio of conventional static CMOS power consumption to clock gating single phase QSERL power consumption. From the obtained results of an adiabatic gain, it can be concluded that with an increase in operating frequency of circuit adiabatic gain will get reduced.

From the plotted graph it is observed that power dissipation of conventional static CMOS and clock gating single phase QSERL D flip-flop is increasing linearly with frequency. Gap between these two plots are almost same but if we observe percentage wise then it is clear that percentage of power saving is reducing with increasing frequency. Clock gating single phase QSERL D flip-flop shows a power reduction of around 82% as compared to that of conventional static CMOS at frequency of around 100MHz. At higher frequency or if switching activity of the circuit is high, power dissipation of the proposed circuit will be equal to or higher than conventional method. This is because for higher frequencies, idle period of the circuit will be shorter or negligible so it is worth to use gating method. These results indicate that use of proposed circuit can be advantageous when applied to the frequency range of around up to hundreds of mega Hertz.

3.3 SR Flip-Flop

3.3.1 Introduction

An SR flip-flop is an arrangement of logic gates that maintains a stable output even after the inputs are turned off. The simple filp-flop has a set input (S) and reset input (R). It is also called as set reset flip-flop. The set input causes output Q set to logic '1' whereas the reset input causes output Q reset to logic '0'. Truth table of SR flip-flop is shown in Table 3.3. Its circuit diagram is shown in Fig. 3.13. This is clocked SR flip-flop. Clock signal works as enable signal to the circuit i.e. circuit will get on when clock signal is logic '1' for high level trigger.

Table 3.3: Truth table of SR flip-flop

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	Invalid

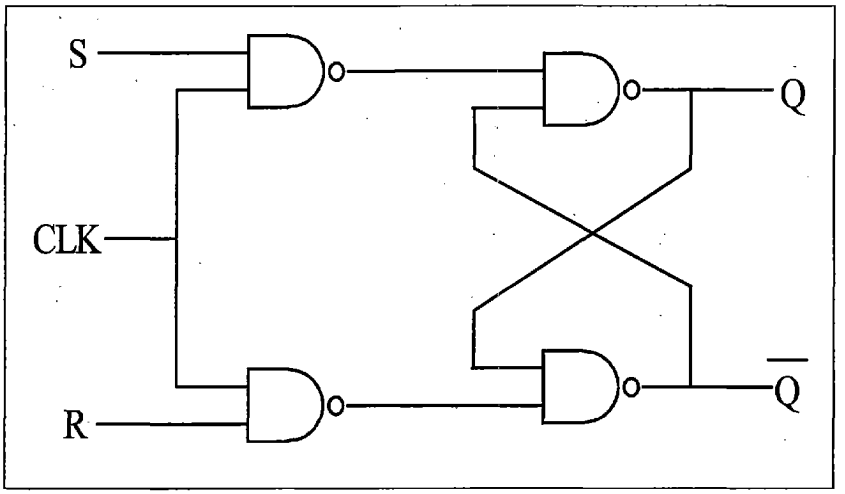

Fig. 3.13: SR flip-flop using NAND gate

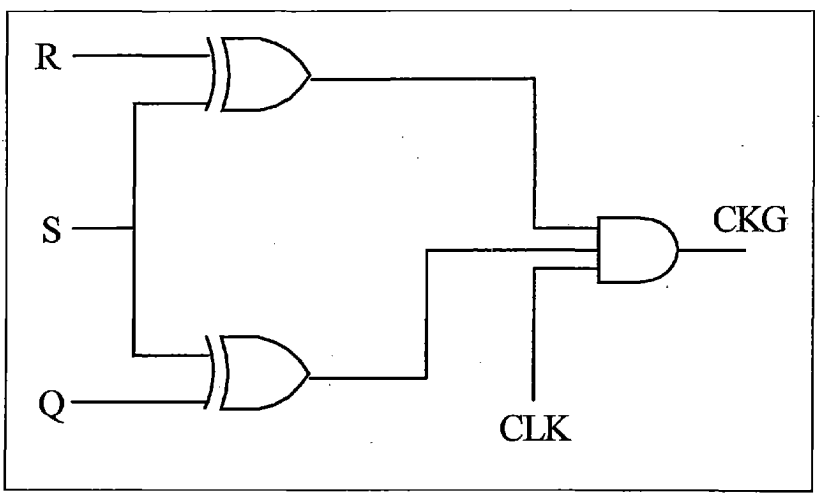

Fig. 3.14: Clock gating circuit for SR flip-flop

Clock gating circuit for SR flip-flop is shown in Fig. 3.14. As we can see from truth table, SR flip-flop will change its state only when inputs S and R are different. When both inputs are same clock signal will continuously trigger the circuit. Due to large capacitance load on clock, there will be large dissipation of energy. So to reduce capacitance load on clock signal clock generator circuit is used to turn off when both input signals are same.

It includes two EX-OR gates and one AND gate. One EX-OR gate is used to compare two input signals S and R. If both input signals are different, signal is passed then input S is compared with output Q using second EX-OR gate. These two EX-OR gates are called as comparator circuit. At the input of AND gate output of EX-OR gates and clock signal are applied which conditionally trigger the SR flip-flop. This AND gate is called as gating.

Clock gating circuit for SR flip-flop can be simplified to equation

$$ckg = (\bar{S}RQ + S\bar{R}\bar{Q})clk \tag{3.1}$$

As previously mentioned single phase quasi-static energy recovery logic and clock gating are simultaneously used to design low power SR flip-flop circuit. One PMOS transistor is used as gating for power clock to reduce dynamic power dissipation in adiabatic circuit. At the input of this PMOS transistor $\overline{ckg}$ signal is applied. This PMOS transistor is used as switch between power clock supply and adiabatic logical block. So that power clock supply will supply energy to circuit only when SR flip-flop is changing its output state.

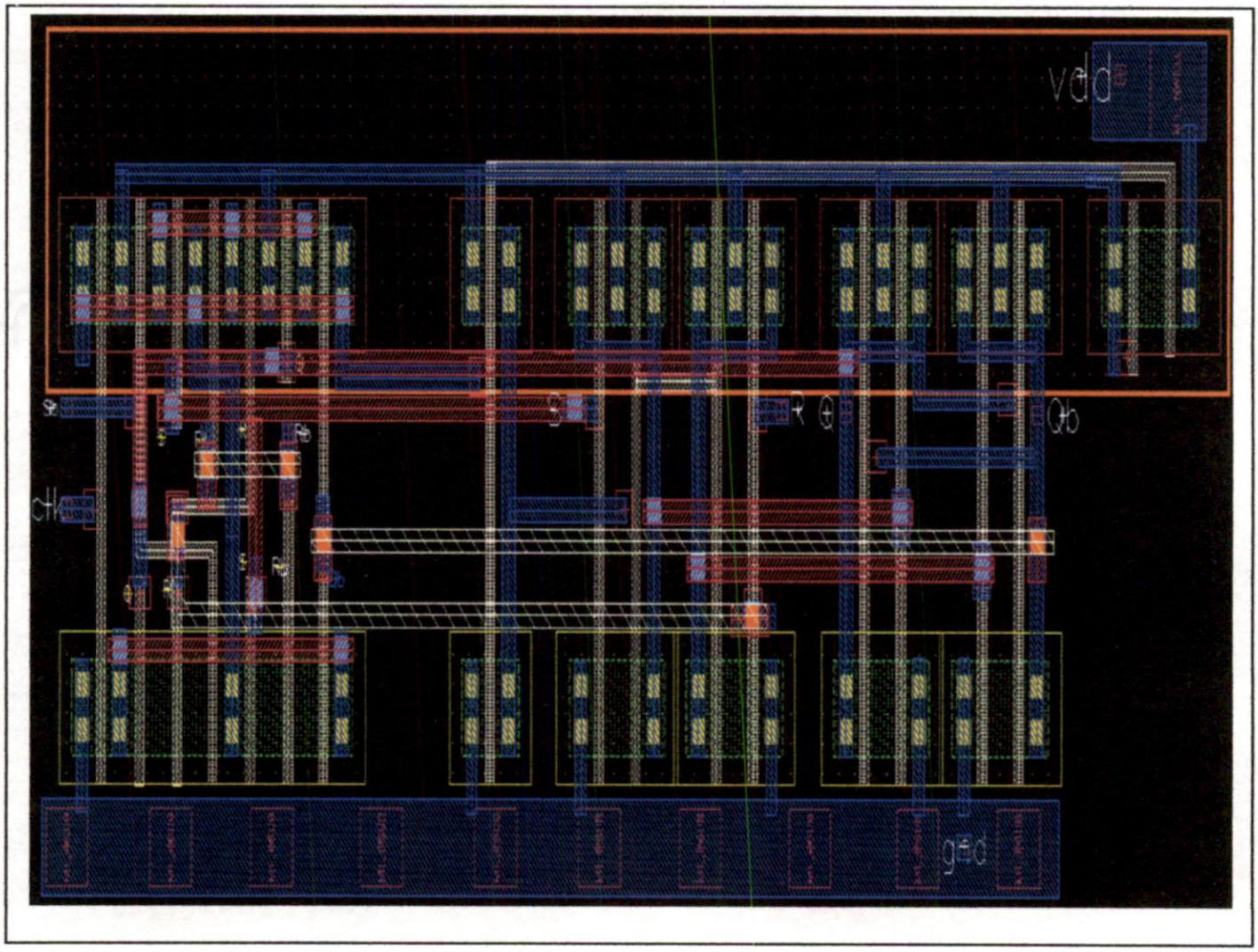

Fig. 3.15: Layout of clock gating single phase QSERL SR flip-flop

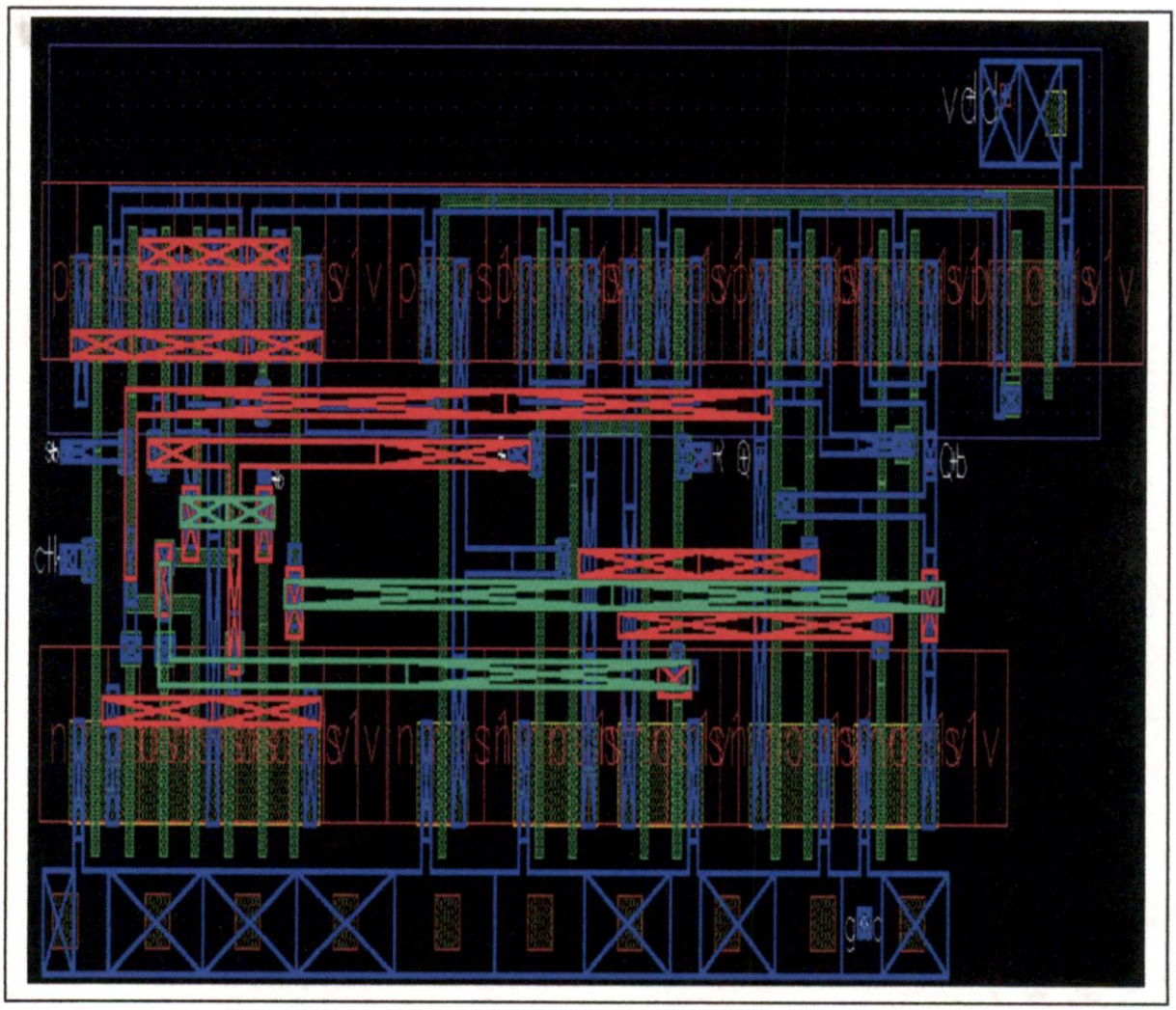

Fig.3.16: RCX extraction of layout of clock gating single phase QSERL SR flip-flop

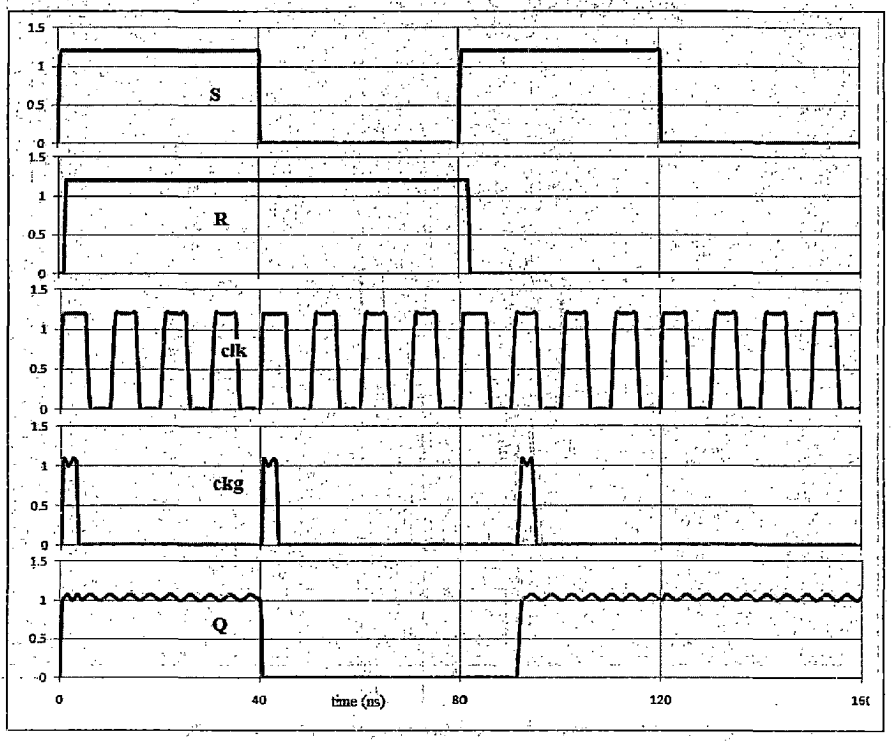

Fig.3.17: Output simulated waveform of SR flip-flop

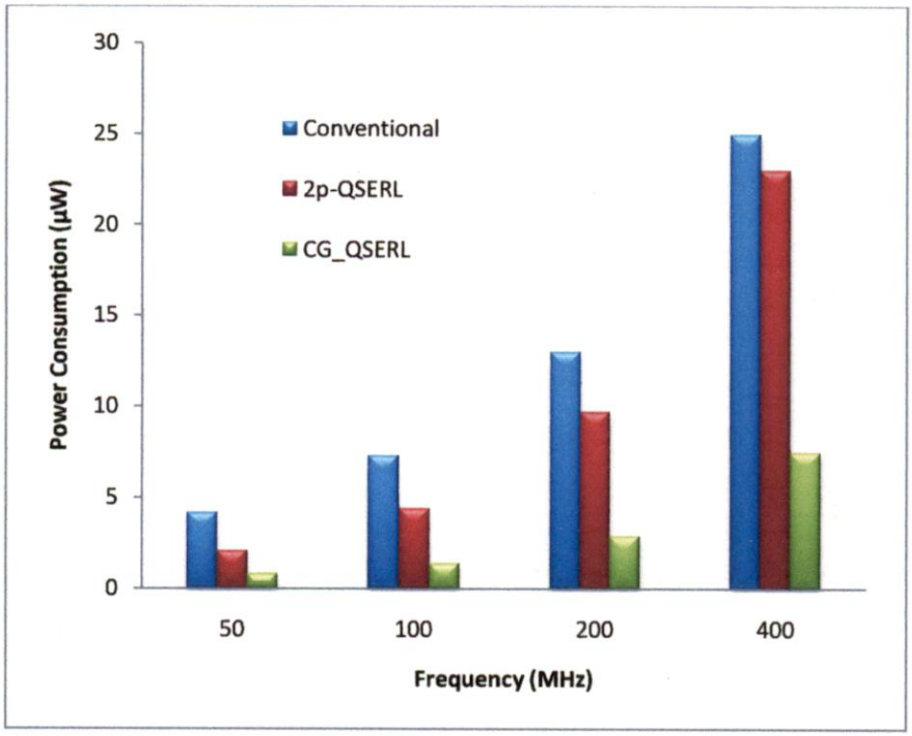

Fig. 3.18(a): For power clock supply

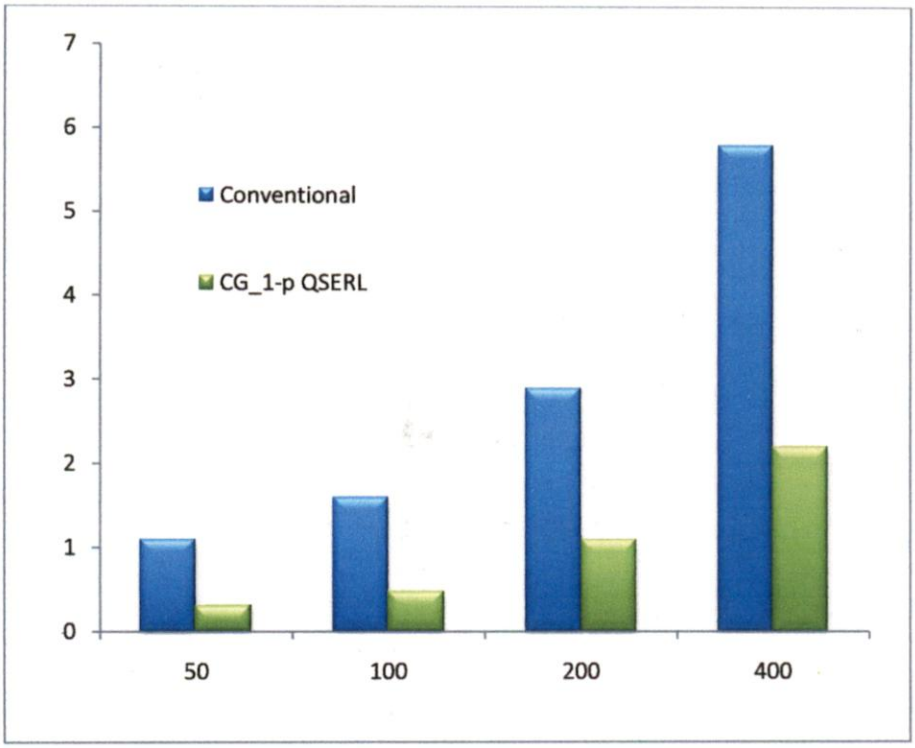

Fig. 3.18(b): For clock generator circuit

Fig. 3.18: Comparison of power consumption of SR flip-flop against frequency

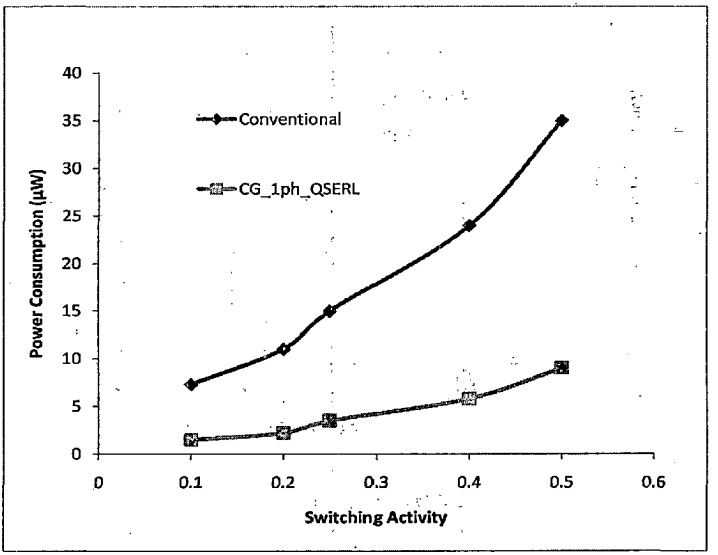

Fig. 3.19(a): For power clock supply

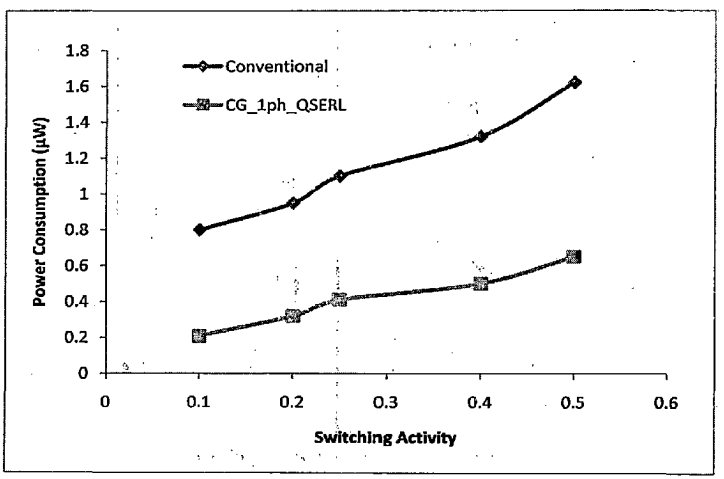

Fig. 3.19(a): For clock generator circuit

Fig. 3.19: Power consumption versus switching activity at C_L = 1fF and f = 100MHz

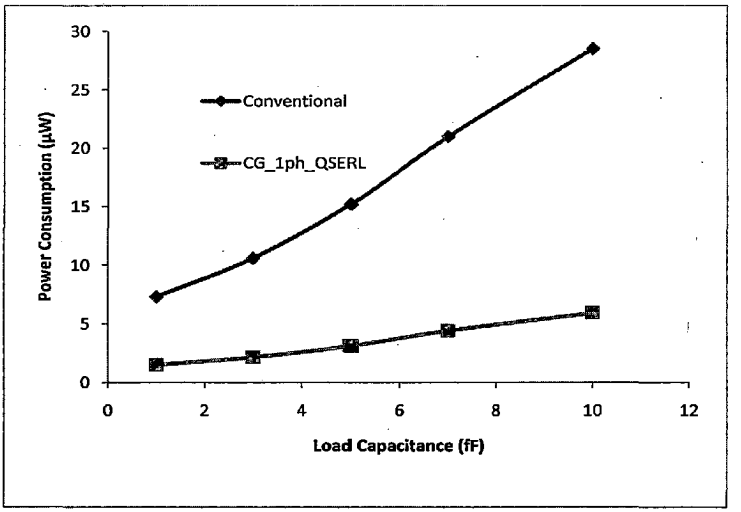

Fig. 3.20: Power consumption versus C_L at switching activity = 0.1 at f = 100MHz

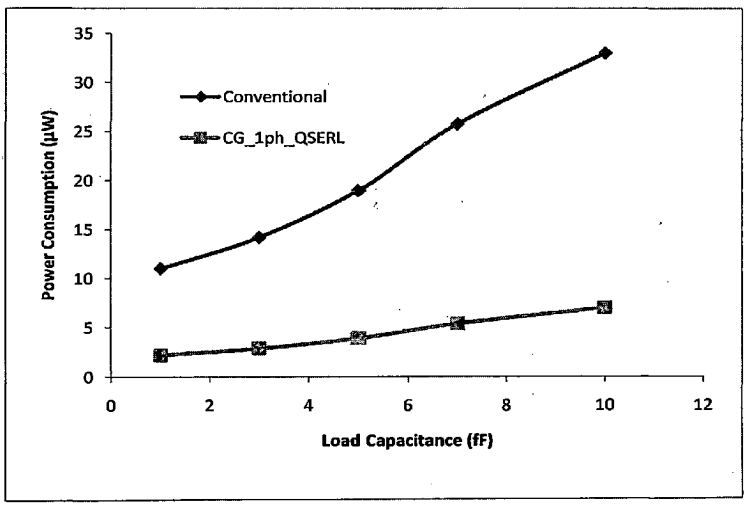

Fig. 3.21: Power consumption versus C_L at switching activity = 0.2 at f = 100MHz

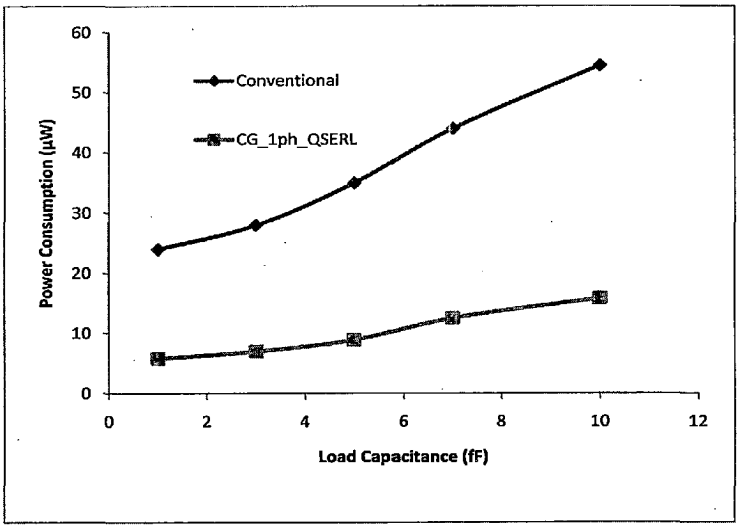

Fig. 3.22: Power consumption versus C_L at switching activity = 0.4 at f = 100MHz

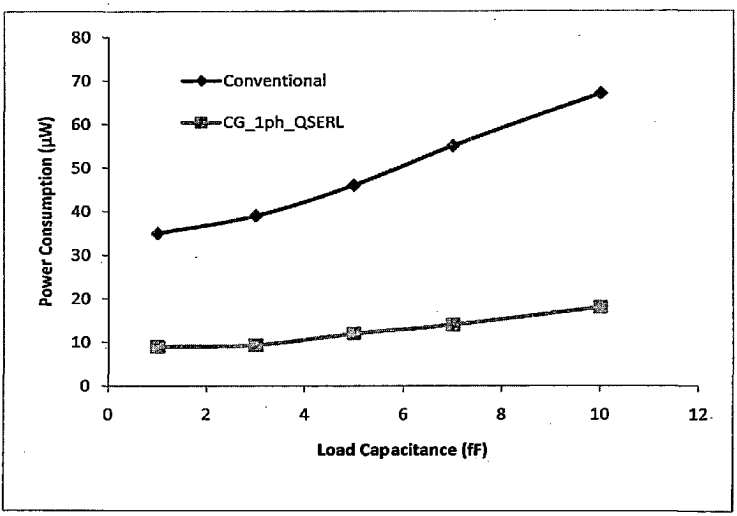

Fig. 3.23: Power consumption versus C_L at switching activity = 0.5 at f = 100MHz

Table 3.4: Power consumption at switching activity = 0.5 and C_L = 5fF

Clock Frequency (MHz)	Conventional Static CMOS (μW)	Clock Gating 1ph-QSERL (μW)	Adiabatic Gain
50	41.5	10.3	4
100	46	12	3.83
200	55	14.5	3.8
300	68	19	3.6
400	86	24.5	3.5

Table 3.5: Power consumption at switching activity = 0.5 and f = 400MHz

Load Capacitance (fF)	Conventional Static CMOS (μW)	Clock Gating 1ph-QSERL (μW)	Adiabatic Gain
1	77.5	19.8	3.9
3	81.2	22.6	3.6
5	86	24.5	3.5
7	91.8	26.9	3.41
10	97	29.4	3.3

3.3.2 Simulations and Results:

Fig. 3.15 and 3.16 shows the layout of clock gating single phase QSERL SR flip-flop and its RCX extracted view respectively obtained from CADENCE virtuoso. Simulated output waveform of this circuit is shown in Fig. 3.17. From obtained output waveform it is observed that clock gating circuit is turned off for idle states or as soon as logical circuit attains its required output state for given inputs.

Comparison of power dissipation versus frequency for SR flip-flop is shown in Fig. 3.18. This comparison is between conventional static CMOS, two phase quasi-static energy recovery and clock gating single phase QSERL methods used for SR flip-flop. As switching activity of the circuit is increased, circuit will not remain idle for long time and clock gating circuit will also consume more power. Hence with increase in switching activity, there will be sharp increase in curve of conventional as well as clock gating adiabatic circuit which is observed in Fig. 3.19. Power consumption of power clock supply of the circuit increases with increase in load capacitance and its graph for different switching activity is also shown in Fig. 3.20-3.23.

Table 3.4 and 3.5 shows the power consumption of power clock supply of circuit at load capacitance C_L = 5fF and input clock frequency of 400MHz respectively at 50 % switching activity. In this table adiabatic gain has also been calculated which is equal to ratio of conventional static CMOS power consumption to clock gating single phase QSERL power consumption. From the obtained results of adiabatic gain, it can be concluded that there will be decrease in adiabatic gain with an increase in operating frequency of the circuit.

From the plotted graph it is observed that power dissipation of conventional static CMOS and 2-phase QSERL SR flip-flop is increasing drastically with frequency. Also the gap between these two plots is decreasing with frequency which concludes that 2-phase QSERL will not work for higher frequency due to higher power dissipation of adiabatic circuit. Plot of clock gating single phase QSERL SR flip-flop is linearly increasing with frequency. Clock gating single phase QSERL SR flip-flop shows a power reduction of around 80% as compared to that of conventional static CMOS at frequency of around 100MHz. These results indicate that use of proposed circuit can be advantageous when applied to the frequency range of around up to hundreds of Mega Hertz.

3.4 JK Flip-Flop

3.4.1 Introduction

The JK flip-flop is the most versatile of the basic flip-flops. It has input following characteristic similar to clocked D flip-flop but has two inputs, traditionally labelled as J and K. Clocked JK flip-flop latch is shown in Fig.3.15. It is implemented just using NAND gates. If J and K are different then output Q takes the value of J at the next clock edge. If J and K are both low then no change occurs in the output state. If J and K are both high at the clock edge, then output will continuously toggle from one state to other. This condition is called as race around condition. Truth table of JK flip-flop is shown in Table 3.2. To remove this race condition, master slave JK flip-flop is used. In this circuit two latches of JK flip-flop are connected in series i.e. one followed by other. First latch is master and second is slave. NOT gate is used between the clock lines of master and slave latches. This master slave JK flip-flop is edge triggered flip-flop.

Table 3.6: Truth table for JK flip-flop

J	K	Q_{n+1} (JK ff)	Q_{n+1} (Master slave JK ff)
0	0	Q_n	Q_n
0	1	0	0
1	0	1	1
1	1	Toggle	Qn

Clock gating circuit for JK flip-flop is shown in Fig. 3.16. As we can see from truth table, JK flip-flop will change its state only when inputs J and K are different or both inputs are logic high. When both inputs are low clock signal will continuously trigger the circuit. Due to large capacitance load on clock, there will be large dissipation of energy. So to reduce capacitance load on clock signal, clock generator circuit is used to turn off when both input signals are low or output is idle for long time. Clock gating will remove undesired power dissipation in clock generator circuit.

Clock gating for JK flip-flop consists of comparator and gating circuit. Comparator compares two inputs and output J, K and Q using EX-OR gate. It also includes OR gate which compares two inputs. Gating circuit consists of AND gate at the input of which clock signal and output of comparator is applied.

Clock gating circuit for JK flip-flop can be simplified to equation

$$ckg = (\bar{J}KQ + J\bar{K}\bar{Q} + JK)clk \tag{3.2}$$

Similar to clock gating method used for D flip-flop, NC^2MOS gating can be used in gating for JK flip-flop [8] i.e. PMOS tree in gating circuit is replace by single PMOS which is controlled by clock signal. As previously mentioned single phase quasi-static energy recovery logic and clock gating are simultaneously used to design low power JK flip-flop circuit. Similar to SR flip-flop one PMOS transistor is used as gating for power clock to reduce dynamic power dissipation in adiabatic circuit. At the input of this PMOS transistor $\overline{ckg}$ signal is applied. This PMOS transistor is used as switch between power clock supply and adiabatic logical block. So that power clock supply will supply energy to circuit only when JK flip-flop is changing its output state.

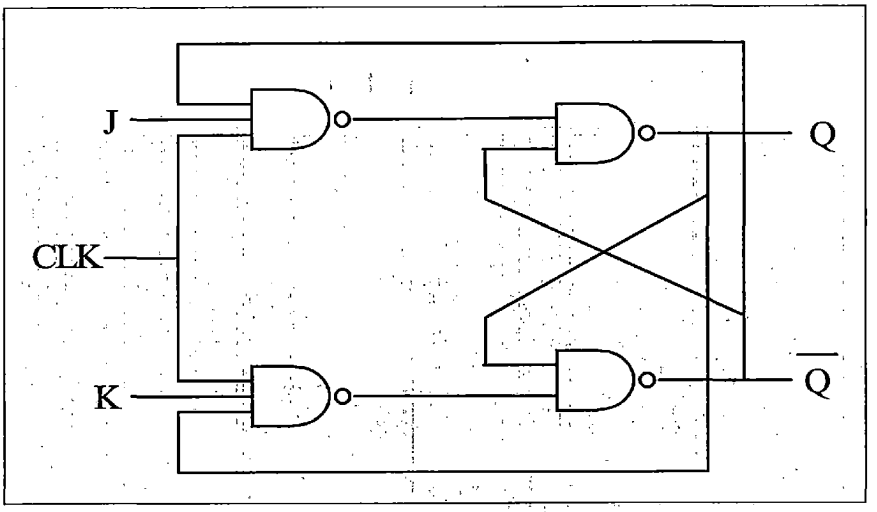

Fig. 3.24: Clocked JK flip-flop

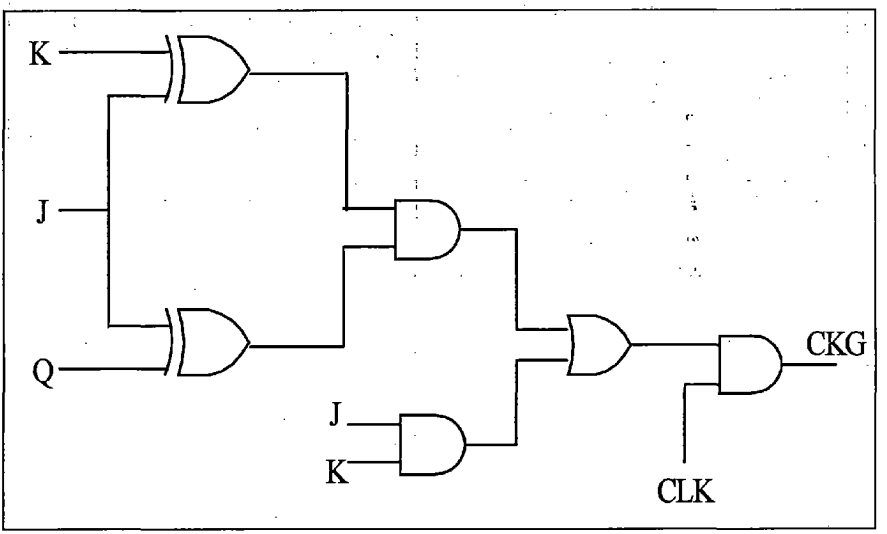

Fig. 3.25: Clock gating for JK flip-flop

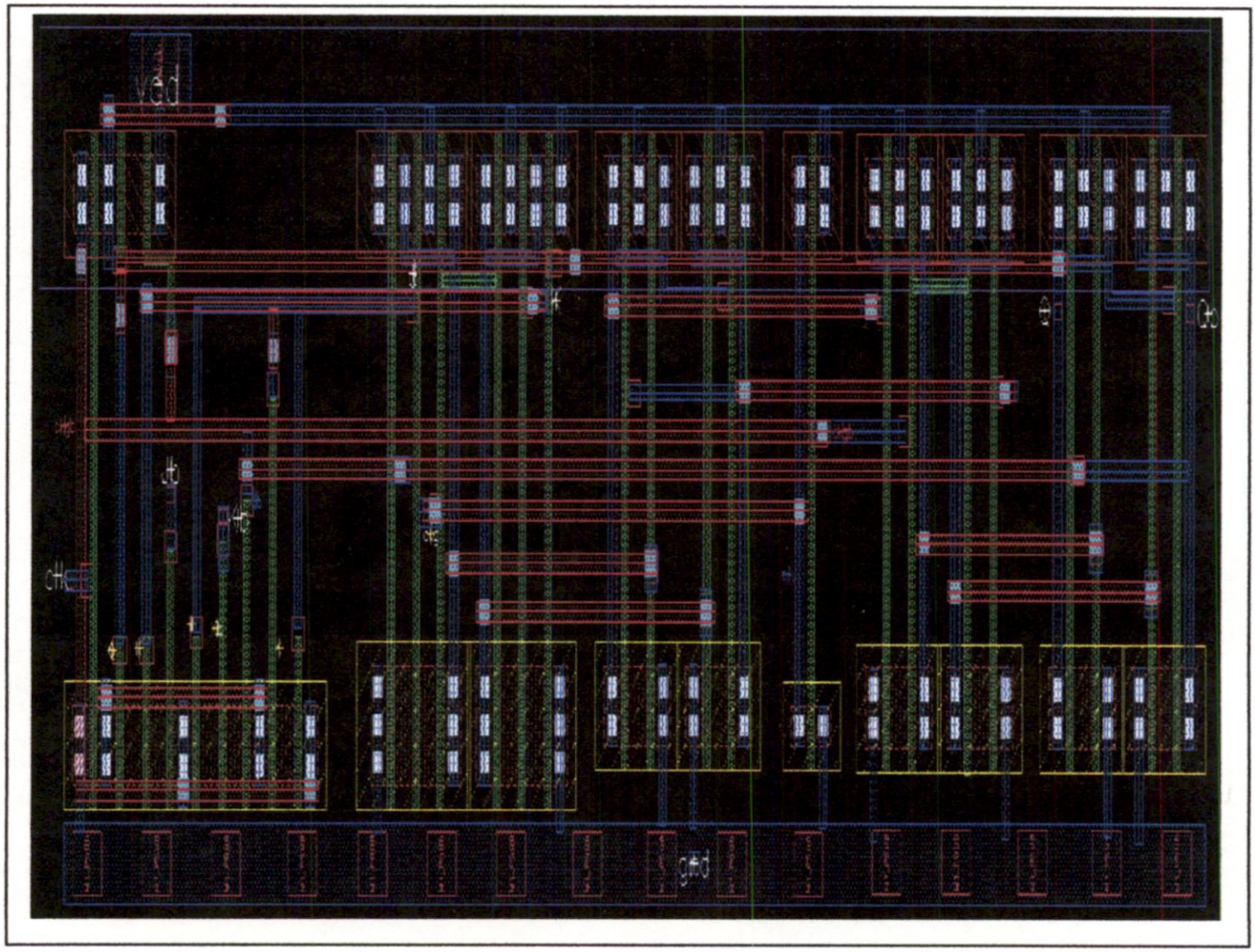

Fig. 3.26: Layout of clock gating single phase QSERL JK flip-flop

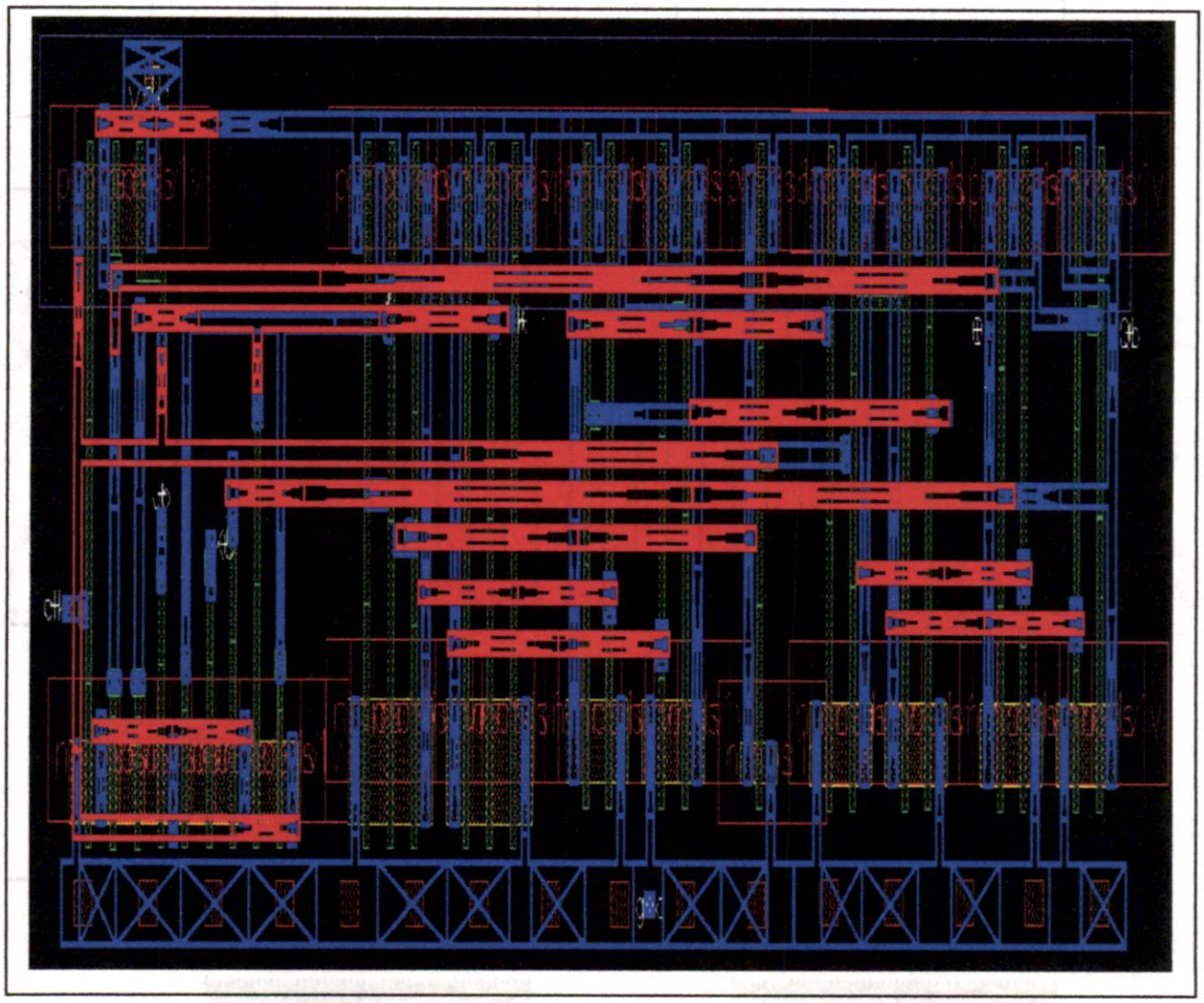

Fig. 3.27: RCX extraction of clock gating single phase QSERL JK flip-flop layout

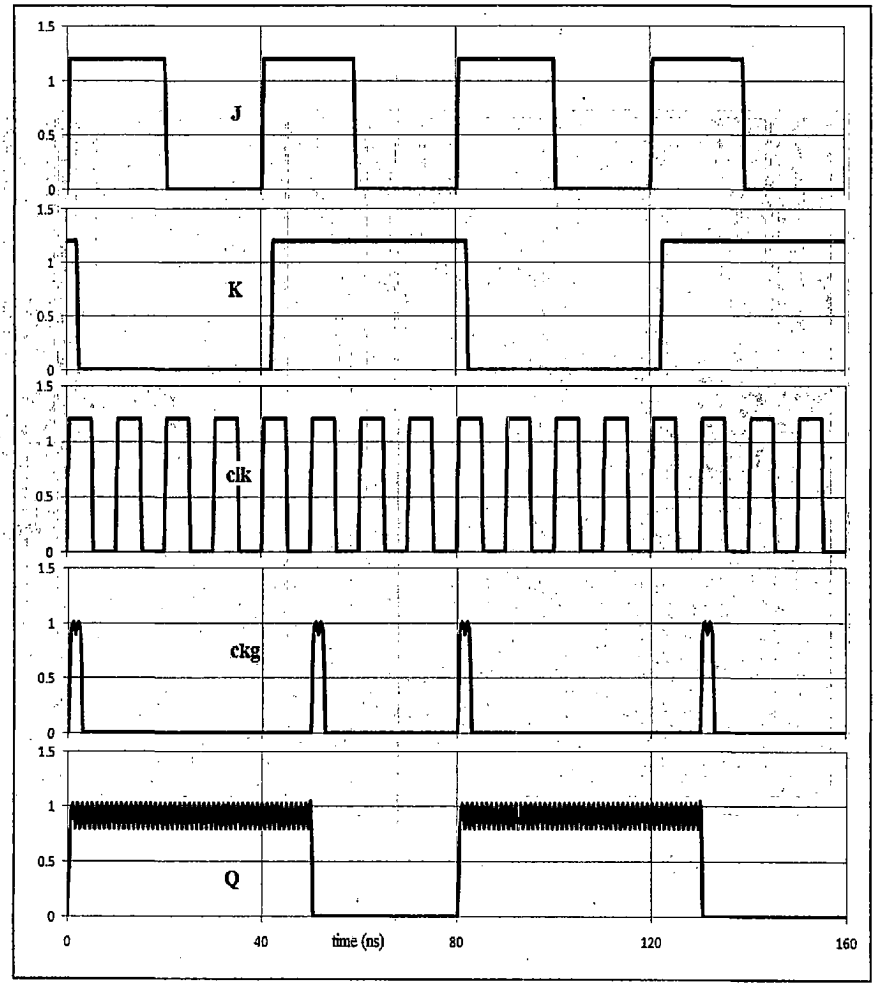

Fig. 3.28: Output waveform of clock gating single phase QSERL JK flip-flop

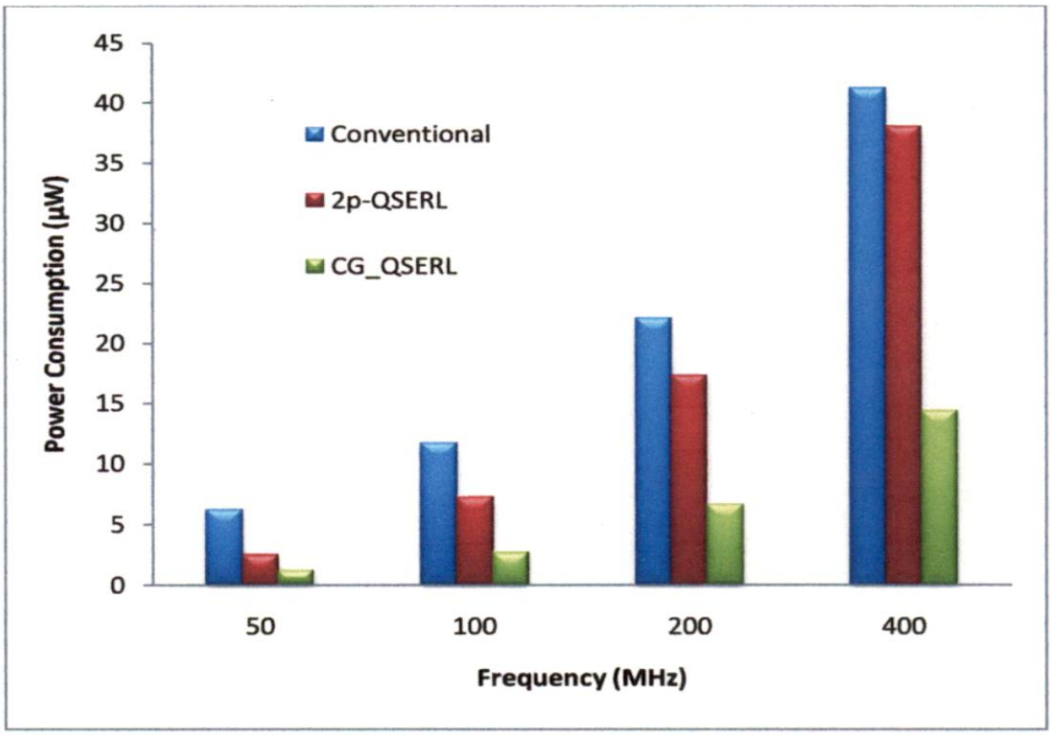

Fig. 3.29(a): For power clock supply

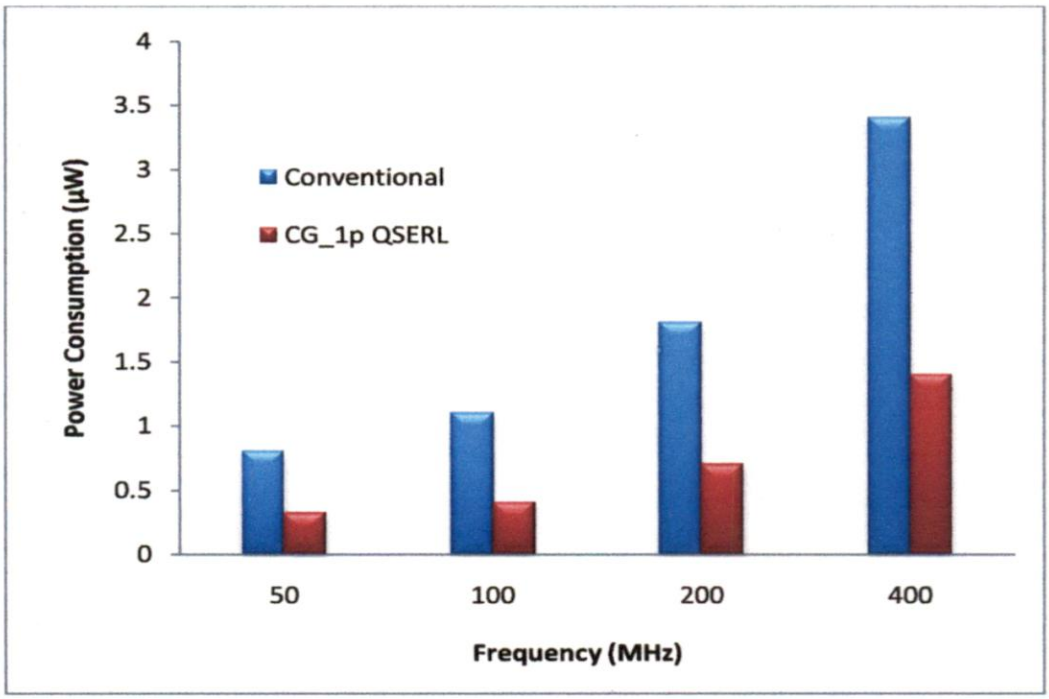

Fig. 3.29(b): For clock generator

Fig. 3.29: Comparison of power consumption of JK flip-flop against frequency

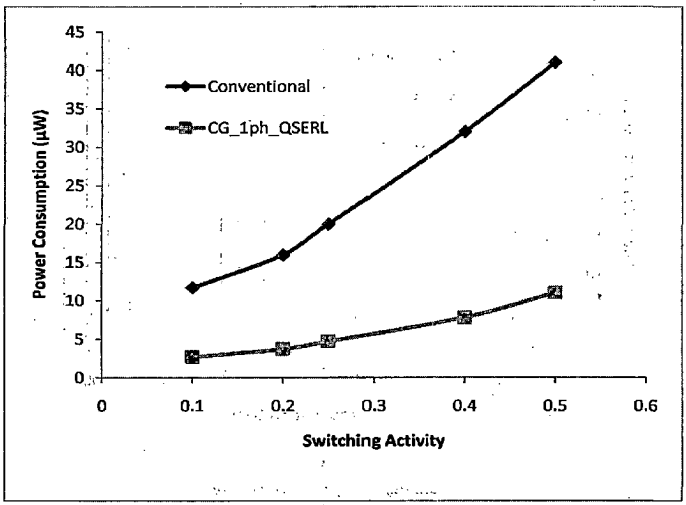

Fig. 3.30(a): For power clock supply

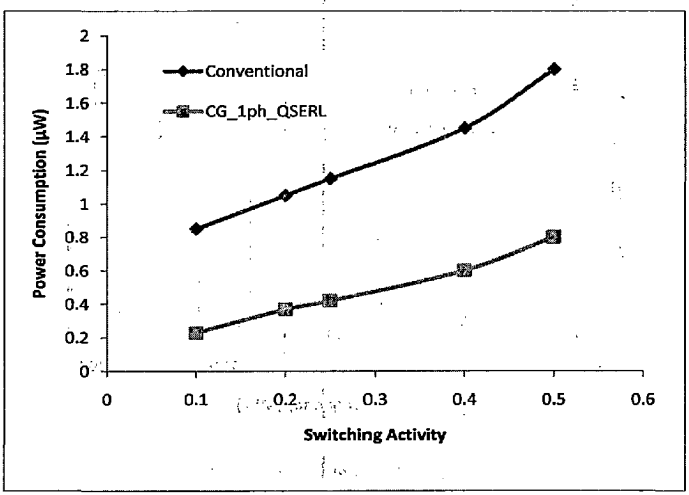

Fig. 3.30(b): For clock generator

Fig. 3.30: Power consumption with switching activity at C_L = 1fF and f = 100MHz

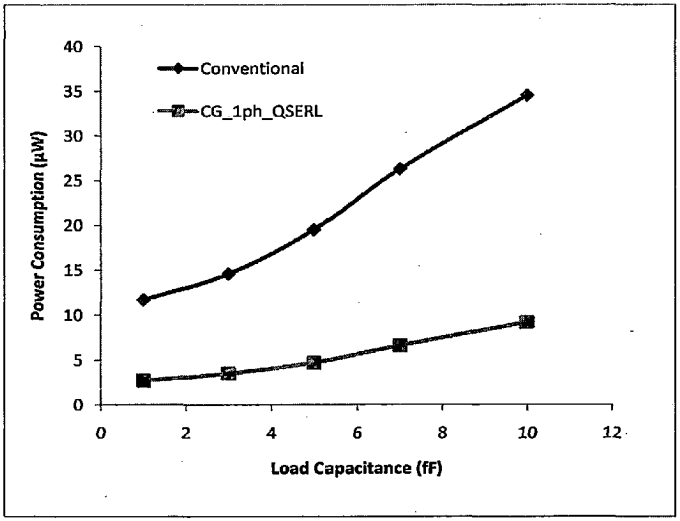

Fig. 3.31: Power consumption for different C_L at switching activity = 0.1

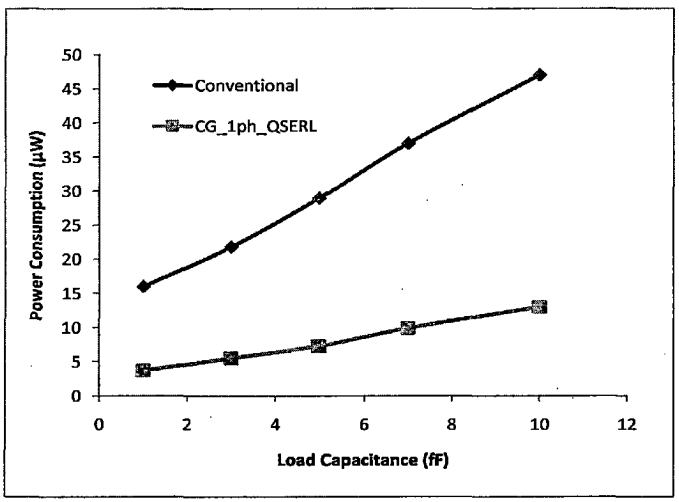

Fig. 3.32: Power consumption for different C_L at switching activity = 0.2

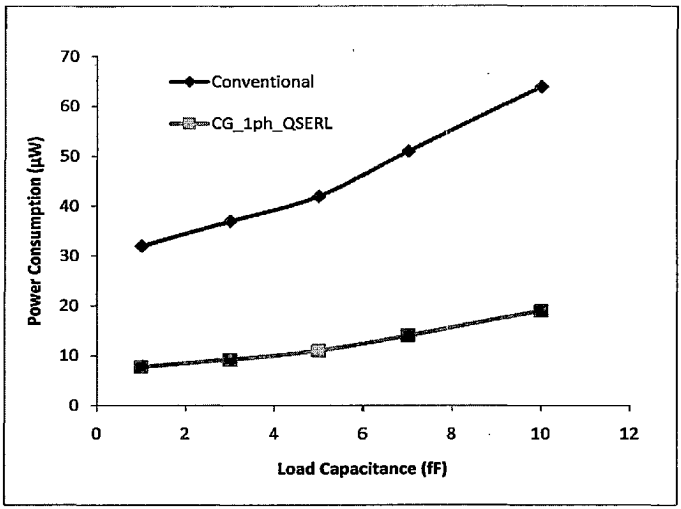

Fig. 3.33: Power consumption for different C_L at switching activity = 0.4

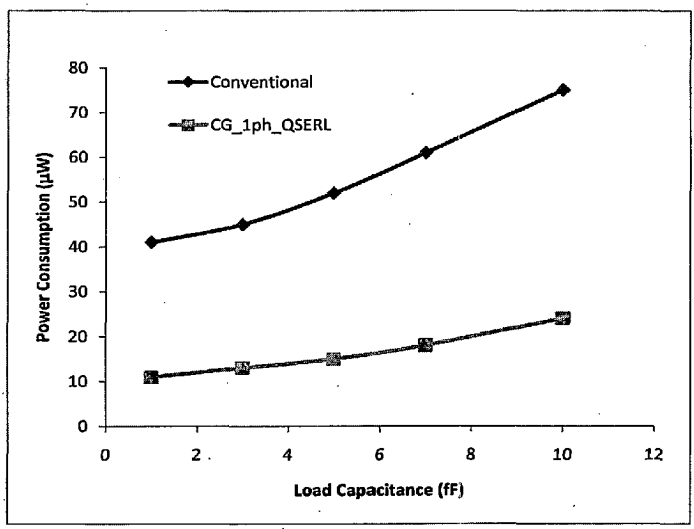

Fig. 3.34: Power consumption for different C_L at switching activity = 0.5

Table 3.7: Power consumption at switching activity = 0.5 and C_L = 5fF

Clock Frequency (MHz)	Conventional Static CMOS (μW)	Clock Gating 1ph-QSERL (μW)	Adiabatic Gain
50	37	9.7	3.2
100	41	11	3.7
200	48	14	3.4
300	59	18	3.3
400	71	24	3

Table 3.8: Power consumption at switching activity = 0.5 and f = 400MHz

Load Capacitance (fF)	Conventional Static CMOS (μW)	Clock Gating 1ph-QSERL (μW)	Adiabatic Gain
1	59	16	3.7
3	64	19	3.4
5	71	24	3
7	81	27	3
10	96	34	2.8

3.4.2 Simulations and Results:

Layout of clock gating single phase QSERL JK flip-flop and its RCX extracted view shown in Fig. 3.26 and 3.27 respectively obtained from CADENCE virtuoso. Simulated output waveform of this circuit is shown in Fig. 3.28. From obtained output waveform it is observed that clock gating circuit is turned off for idle states or as soon as logical circuit attains its required output state for given inputs to save loss of energy. Fig. 3.29 shows the comparison of power dissipation versus frequency for JK flip-flop. This comparison is between conventional static CMOS, two phase quasi-static energy recovery and clock gating single phase QSERL methods used for JK flip-flop. As switching activity of the circuit is increased, circuit will not remain idle for long time and clock gating circuit will also consume more power. Hence with increase in switching activity, there will be sharp increase in curve of conventional as well as clock gating adiabatic circuit which is observed in Fig. 3.30. If we increase the load capacitance of the circuit then power consumption of power clock supply of circuit will also increases and its graph for different switching activity is also shown in Fig. 3.31-3.34.

Table 3.7 and 3.8 shows the power consumption of power clock supply of circuit at the load capacitance of C_L = 5fF and input clock frequency of 400MHz respectively at 50 % switching activity. In this table adiabatic gain has also been calculated which is equal to ratio of conventional static CMOS power consumption to clock gating single phase QSERL power consumption. It is also concluded that an adiabatic gain decreases with increase in operating frequency of the circuit.

From the plotted graph it is observed that power dissipation of conventional static CMOS and 2-phase QSERL SR flip-flop is increasing drastically with frequency. Also the gap between these two plots is decreasing with frequency which concludes that 2-phase QSERL will not work for higher frequency due to higher power dissipation of adiabatic circuit. Plot of clock gating single phase QSERL JK flip-flop is linearly increasing with frequency. Clock gating single phase QSERL JK flip-flop shows a power reduction of around 80% as compared to that of conventional static CMOS at frequency of around 100MHz. These results indicate that use of proposed circuit can be advantageous when applied to the frequency range of around up to hundreds of Mega Hertz.

CHAPTER 4

SHIFT REGISTER

4.1 Introduction

Shift register is a cascade of flip-flops which shares the same clock and shifts data by one bit after sensing a clock signal. Shift registers can have both parallel and serial inputs and outputs. These are often configured as serial-in parallel-out (SIPO) or as parallel-in serial-out (PISO). There are also types that have both serial and parallel input and types with serial and parallel output. There are also bi-directional shift registers which allow shifting in both directions: L→R or R→L. The serial input and last output of a shift register can also be connected together to create a circular shift register.

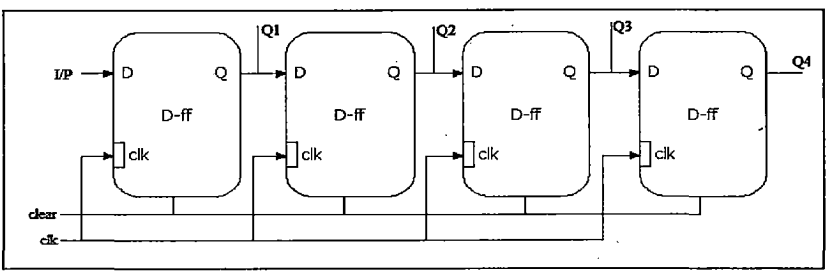

Fig. 4.1: 4-bit Shift Register

In this work, 4-bit serial-in serial-out shift register has been designed using clock gating and single phase QSERL adiabatic technique to show the power saving of D flip-flop. It consists of four D flip-flops connected in series as shown in Fig. 4.1. Its simulated output waveform

is shown in Fig. 4.2 which is obtained through CAEDENCE simulator. As we can see input data is shifted by 1 clock cycle after each flip-flop with the output data of previous flip-flop.

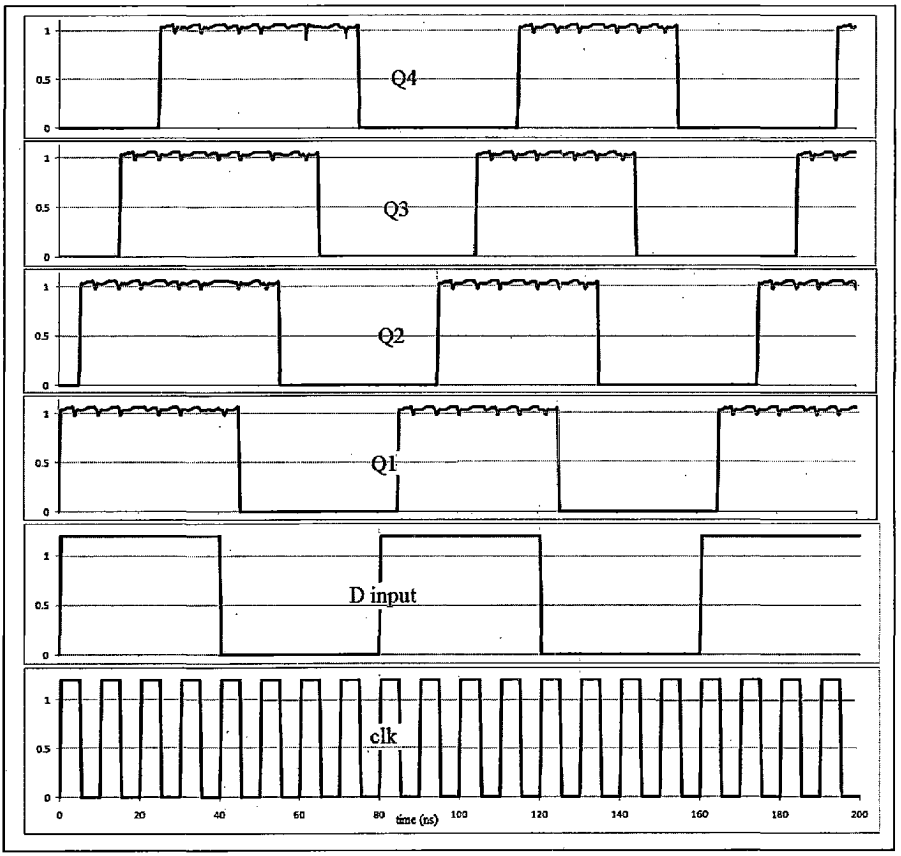

Fig. 4.2: Simulated waveform of 4-bit shift register

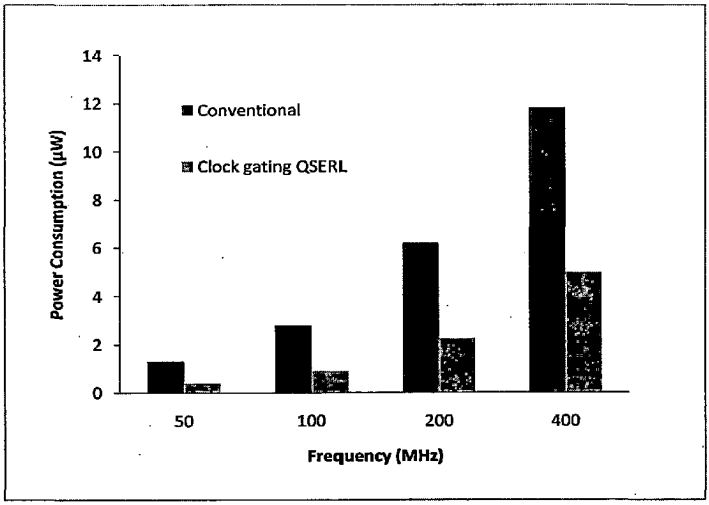

Fig. 4.3(a): For clock supply

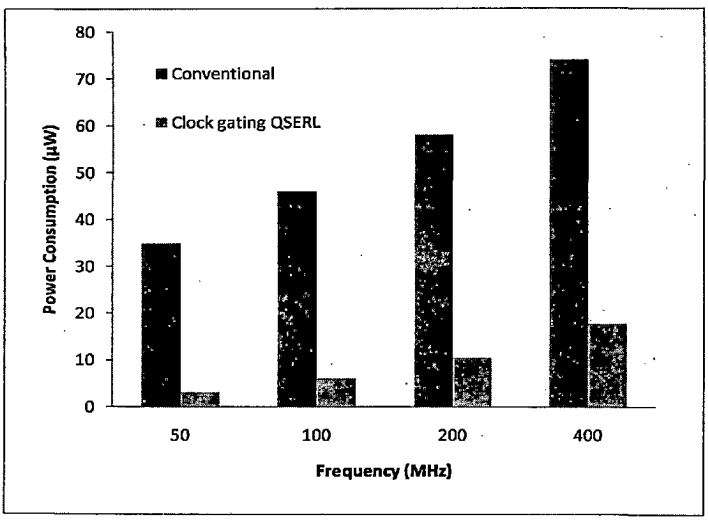

Fig. 4.3(b): For power supply

Fig. 4.3: Comparison of power consumption of clock gating QSERL with conventional 4-bit shift register

Table 4.1: Power consumption at switching activity = 0.5 and C_L = 5fF

Clock Frequency (MHz)	Conventional Static CMOS (µW)	Clock Gating 1ph-QSERL (µW)	Adiabatic Gain
50	87	15.5	5.6
100	94	19.7	4.8
200	106	25	4.2
300	126	34	3.7
400	143	45	3.2

Table 4.2: Power consumption at switching activity = 0.5 and f = 100MHz

Load Capacitance (fF)	Conventional Static CMOS (µW)	Clock Gating 1ph-QSERL (µW)	Adiabatic Gain
1	76	15	5
3	83	17	4.9
5	94	19.7	4.8
7	107	22.4	4.8
10	126	27	4.7

4.2 Simulations Results and Discussions

We have designed SIPO 4-bit shift register as shown in Fig. 4.1 based on the clock gating and single phase QSERL technique to show an efficiency of the proposed technique. Its simulated waveform is shown in Fig. 4.2. Comparison of power consumption of 4-bit shift register using clock gating and single phase QSERL with conventional static CMOS method at different frequency is shown in Fig. 4.3. It is observed that power saving of the proposed shift register is about 70% for clock supply and it is about 82% for power supply at frequency of 100MHz.

As operating frequency of circuit increases, switching activity of the circuit also increased and circuit will not remain idle for long time and clock gating circuit will also consume more power. Hence with increase in switching activity, there will be sharp increase in curve of conventional as well as clock gating adiabatic circuit which is observed in Fig. 4.3.

Table 4.1 and 4.2 shows the power consumption of conventional static CMOS and clock gating single phase QSERL circuit at the load capacitance of C_L = 5fF and input clock frequency of 100MHz respectively at 50 % switching activity. Adiabatic gain has also been calculated shown in above table which is equal to ratio of conventional static CMOS power consumption to clock gating single phase QSERL power consumption. As frequency and capacitance load of the circuit is increases, adiabatic gain goes on decreasing.

CHAPTER 5

CONCLUSIONS AND FUTURE SCOPE

5.1 Conclusions

The sequential circuits such as D flip-flop, SR flip-flop, JK flip-flop and shift register are designed using clock gating and single phase quasi-static energy recovery logic to achieve ultra low power circuits. The clock gating logic succeeds in disabling flip-flop during idle periods and does not exhibit timing problems. Dynamic power consumption during idle periods has been reduced to a large extent. Reliable flip-flops and sequential circuits can be realized with clock gating and single phase QSERL method.

Undesired dynamic power dissipation of an adiabatic circuit has been reduced. Proposed clock gating single phase QSERL technique increases operating range of circuit. This technique shows a power reduction of approximately 80% as compared to that of conventional static CMOS at frequency of around 100MHz. These results indicate that use of proposed circuit can be advantageous when applied to the frequency range of around up to hundreds of Mega Hertz.

We have presented low power clock gating quasi-static energy recovery logic with true single-phase power clock. The clock gating and quasi-static nature of this logic leads to less switching activity and low power consumption. Also the single-phase power clock makes it easier to design the clock network for synchronous systems.

5.2 Future Scope

This work can be continued by implementation different counters, complex sequential and combinational circuits. Also the effect of timing issues, clock skews, glitches etc can be studied with more complex circuits. These obtained results can also be compared with HSPICE simulation results. Another potential application of this work is to improve delay with power consumption of the circuit by minimizing delay of gating circuit or using some other logic.

PUBLICATIONS

[1] R. Kumbhare, J. Kanungo, A. K. Saxena and S. Dasgupta, "Design of Ultra Low Power Clock Gating D Flip-Flop using Quasi-Static Energy Recovery Logic", communicated to *IEEE International Conference on Multimedia, Signal Processing and Communication Technologies (IMPACT'11)*, 2011.

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ANNEXURE

Fig. No.	Aspect Ratio (W_p/W_n)
3.4	2.5:1
3.15	2:2
3.26	2:1 (For inverter)
	2:2 (For others)
4.1	2.5:1