MICROPROCESSOR CONTROL OF LINE COMMUTATED INVERTER FED INDUCTION MOTOR DRIVE

A DISSERTATION

Submitted in partial fulfilment of the requirements for the award of the Degree

of

MASTER OF ENGINEERING

in

ELECTRICAL ENGINEERING

(Power Apparatus and Electric Drives)

By

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CANDIDATE'S DECLARATION

I hereby, certify that the work which is being presented in the dissertation entitled, MICROPROCESSOR CONTROL OF LINE COMMUTATED INVERTER FED INDUCTION MOTOR DRIVE in partial fulfilment of the requirements for the award of the degree of MASTER OF ENGINEERING in ELECTRICAL ENGINEERING with specialization in POWER APPARATUS AND ELECTRIC DRIVES, submitted in the Electrical Engineering Department, University of Roorkee, Roorkee[India], is an authentic record of my own work carried out for a period of about six months from September,1986 to March 1987, under the supervision of Dr. D.R. Kohli, Professor, Electrical Engineering Department, University of Roorkee and Sh. M.K. Vasantha, Reader, Electrical Engineering Department, University of Roorkee, Roorkee, India.

The matter embodied in this dissertation has not been submitted by me for the award of any other degree.

Dated [ANIL BHATIA]

This is to certify that the above statement made by the candidate is correct to the best of our knowledge.

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ABSTRACT

The line commutated inverter and synchronous motor system have the characteristic of a D.C. motor. This combination is popularly known as the commutatorless D.C. motor. The LCI-SM system can be used as a variable frequency source for induction motor Drive.

In the present thesis work the line commutated inverter has been fabricated and a microcomputer based firing scheme has been developed. The steady state performance characteristics of the LCI-SM system have been obtained using both analog and microcomputer based firing scheme. Finally, the feasibility of microcomputer controlled LCI-SM system as a variable frequency source for induction motors has been experimentally investigated.

From extensive tests carried out on the experimental setup of LCI-SM-IM system, it has been observed that the LCI-SM system works satisfactorily as a variable frequency source. The microcomputer control improves the system performance of the system by improving the stability and reliability of firing pulses.

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CHAPTER I

INTRODUCTION

1.1 GENERAL:

D.C. machines have been the work horses in industry for variable speed applications since they satisfy the requirements of a wide range of speed control. However, it has the disadvantages inherent with a mechanical commutator.

The commutator limits the maximum power of the D.C. machine to 10,000 K.W. at 1000 RPM and to 500 KW at 5000 RPM. The brushes and the commutator not only limit the power output but also make it unsuitable for dusty and explosive environment. The induction motor on the other hand, has a robust rotor construction which permits a reliable and almost maintenance free operation. Inspite of these advantages the inherent limitation of constant speed of operation has been the main bottleneck in its widespread use as a variable speed drive.

The advent of semiconductor technology led to the development of solid state adjustable speed A.C. drives in 1960[ ]. Since then many innovations in devices, circuits, control theory, and signal electronics have made a considerable contribution to this technology. Of the various methods of A.C. motor speed control, its operation at variable frequency is becoming more and more popular, since it is possible to obtain variable speed as well as good regulation and efficiency. The static variable frequency converters are expensive but are

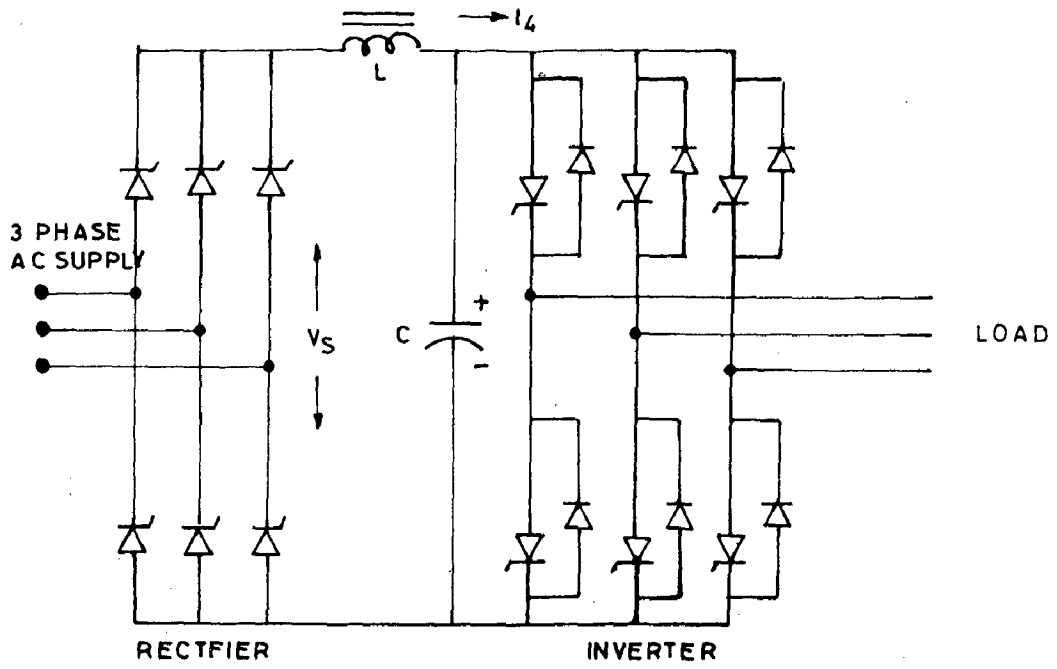


FIG. 1.1 DC LINK VOLTAGE-FED INVERTER (VSI)

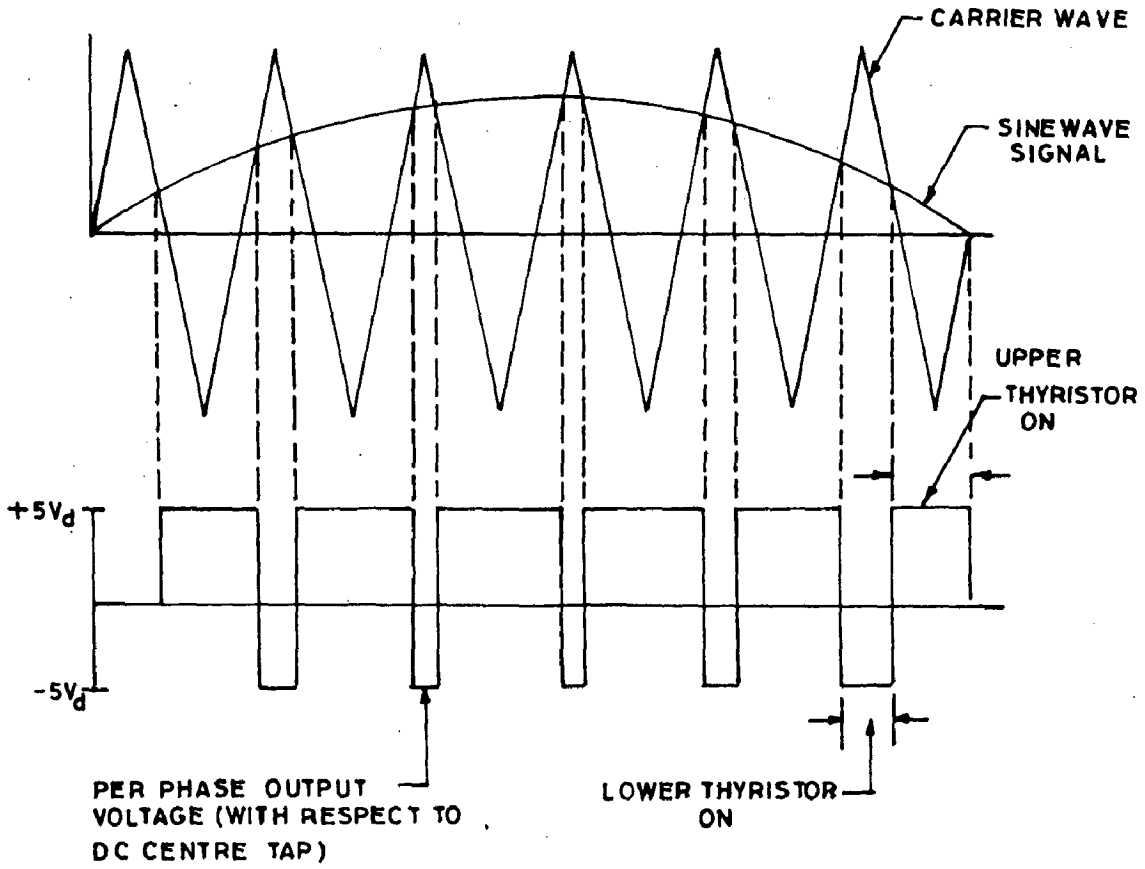


FIG. 1.2 PRINCIPLE OF PWM
(SINUSOIDAL PWM TECHNIQUE)

advantageous in terms of accuracy and reliability. The current research in adjustable speed A.C. drives is focussed on the cost reduction of the converter and control equipment. The variable frequency A.C. drives becomes particularly attractive in multimotor drive systems where a large number of small motors are supplied from one source. Such multimotor drives find applications in textile, synthetic fibre, paper making industries, traction, and in processing lines where exact sheed coordination is essential in order to maintain the quality of the product.

The solid state variable frequency sources for A.C. drives can be broadly classified into two types,

1. Cycloconverters,
2. D.C. Link converters which include,
   (a) Voltage source inverters(VSI)
   (b) Current source inverters(CSI).

1.2 VOLTAGE SOURCE INVERTER(VSI):

The VSI's are generally classified into two types, square wave inverters and pulse width modulated inverters. These type of inverters were introduced from the beginning of 1960's when a forced commutation technique was introduced[ ]. Fig 1.1 shows the conventional power circuit of a voltage source inverter. The squarewave output voltage leads to a number of undesirable effects, i.e. additional harmonic power losses and torque pulsuations in motors. The harmonic currents

flowing in stator and rotor contribute to extra copper losses and some amount of stray iron losses. The lopwer order of harmonics of the inverter. Voltage waveform can be eliminated by multiphasing. However, such an expensive technique is not justified for normal applications. The commutating capacitor in the voltage source inverters is ussually charged by the D.C. link voltage hence commutating capability decreases as the D.C. voltage decreases. The inverter requires six commutating cycles per cycle of fundamental, leading to increased commutation losses and requiring complex control circuitary as well as fast switching SCRs.

The voltage fed square wave inverter drives are normally used in low to medium horse power ratings where speed ratio is usually limited to 10:2. This type of drive has been largely superceded by PWM drives.

In PWM inverters the thyristors are switched on and off many times within a half cycle to generate a variable voltage output which is normally low in harmonic contents. Among the PWM techniques sinusoidal PWM technique is common and is shown in Fig 1.2. This technique reduces the harmonic losses but it suffers from low inverter efficiency. In low and medium power applications the thyristors in the inverter can be replaced by transistors leading to elemination of commutation and higher prequencies of operation.

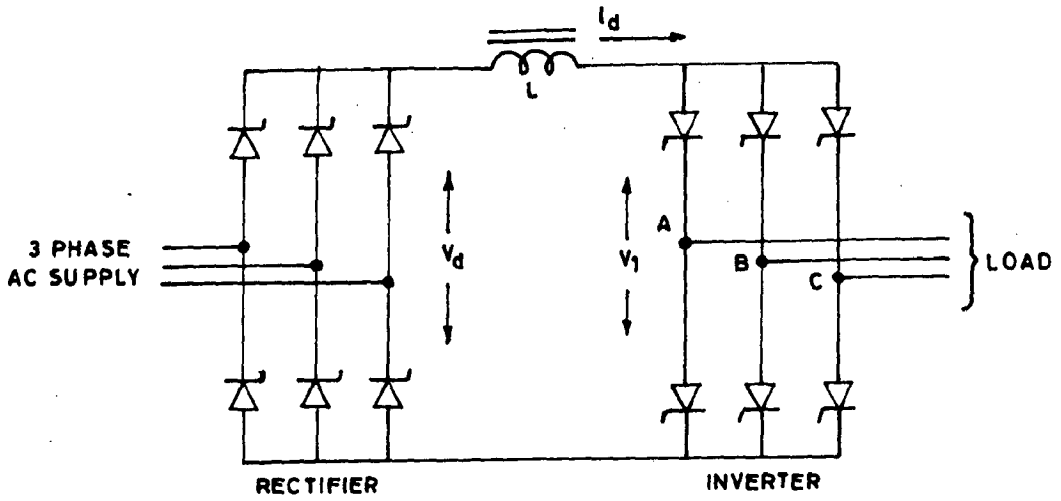
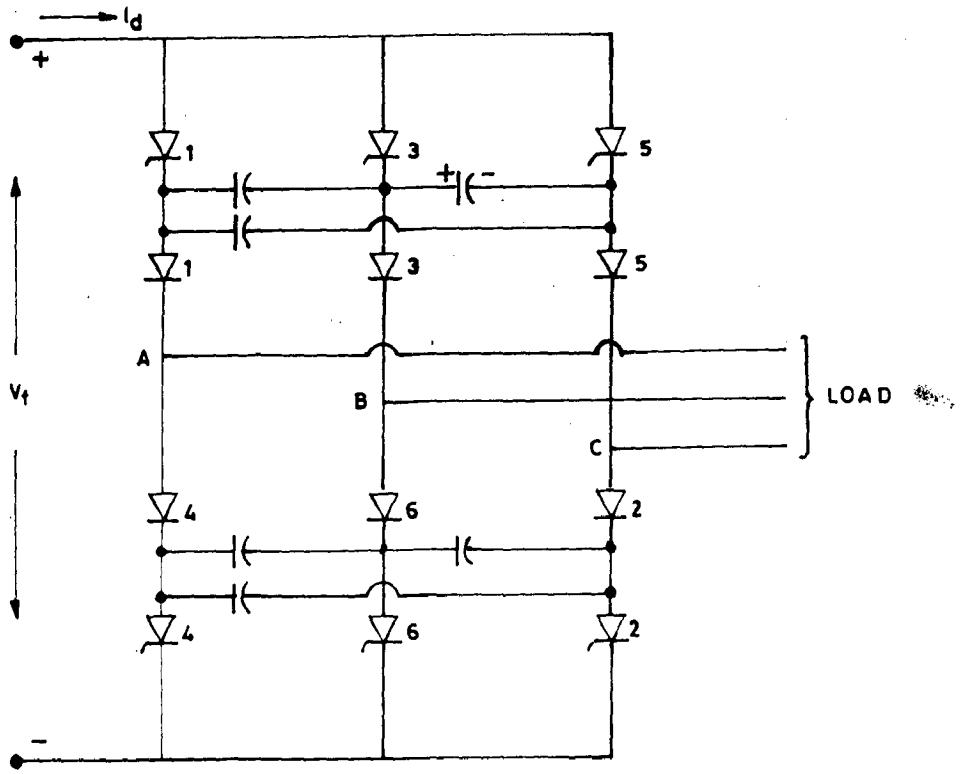


FIG. 1.3 DC LINK CURRENT-FED INVERTER



(C51)

FIG. 1.3 CURRENT-FED INVERTER
(AUTO SEQUENTIALLY COMMULATED)

1.3 CURRENT SOURCE INVERTER(CSI):

The current source inverter circuit is as shown in Fig 1.3. The CSI drive has many good features which can be summarised as follows:

1. Regeneration is possible,
2. There is no possibility of shoot through fault,
3. The fault current on the inverter side rises very slowly,
4. Commutation losses are lower than in VSI drives,
5. The inverter can be designed with low speed SCRs.

Against the above mentioned merits, the CSI drives have the following limitations:

1. The frequency range of inverter is lower and it cannot operate on no load,
2. The large size of D.C. link inductor and commutating capacitor make the inverter expensive,
3. The commutation is dependent upon machine subtransient inductance which adds large transient over voltages at machine terminals,
4. The drive has instability problems and sluggish response at light loads and high speeds.

These factors limit the use of CSI to single motor, medium or high power drives. A line commutated inverter is obtained by operating an SCR bridge in continuous current mode with firing

angle α greater than 90^{o}. The sequential commutation of SCRs is obtained with the help of three phase line voltages. The line commutated inverter requires reactive power for commutation. The reactive power required depends upon the firing angle of the inverter. The reactive power can be supplied by the following:

1. Line voltages,
2. Capacitors connected at the output of LCI,
3. Overexcited synchronous motor connected to the three phase output terminals of LCI.

The line commutated, inverter overcomes all the problems of forced commutated inverters as well as cyclo-converters. Some of the characteristic features of LCI are:

1. No harmonics in output voltage waveform,
2. Commutating components are not required,
3. The triggering circuit requirements are comparitively simple.

1.4 LCI-SYNCHRONOUS MOTOR SYSTEM(CLM):

The advent of SCRs in sixties led to the development of a static commutator for the D.C. machine using line commutated inverters. The LCI-synchronous machine combination gives the characteristics of a D.C. motor. The commutation of SCRs is controlled by the sinusoidal induced voltage in stator due to rotating field of rotor. This combination is is popularly known as the commutatorless D.C. motor. A large

number of such drives have been commissioned by Siemens for starting of 80 MVA gas turbine generating sets, boiler feed pumps etc.

The commutatorless motor has been generally used by industry in following cases:

1. When high speeds upto 7,000 RPM are required,
2. When high ratings up to 10,000 H.P. are required.
3. When high efficiency is required.

The possible use of LCI and synchronous motor as a variable frequency source for induction motors was first reported by Brader[9] with possibility of applications in the field of traction and group drives, etc. Ranganadhachari[32] investigated the performance of synchronous machine and LCI combination as a variable frequency source for multi induction motor drive and for static loads and has demonstrated the viability of the scheme. For the firing and control circuitary of LCI Ranganadhachari has used analog schemes.

1.5 SCOPE OF WORK IN THE PRESENT THESIS:

In the present work an attempt has been made to compare and experimently verify the performance of a system consisting of LCI and synchronous motor combination, used as a variable frequency source feeding induction motors as a load with two types of firing schemes:

1. Analog firing scheme.
2. Digital scheme using microcomputer.

The present work has the following objectives:

1. Design and fabrication of converter inverter power circuit,
2. Performance testing of LCI - synchronous motor system using analog firing scheme,
3. Development of micro computer based firing scheme for LCI,
4. Operation and testing of LCI synchronous motor system using digital scheme,
5. Performance of LCI - synchronous motor system as a variable frequency source for induction motor.

1.6 LITERATURE SURVEY:

Extensive literature is available on LCI-synchronous machine system operating as a commutator-less motor. Tadakuma, Tamura and Tanaka[11] have described the driving characteristics of commutator-less motor controlled by induced voltage detectors. Rosa[12] has analysed a d.c. link type variable frequency synchronous motor drive, and discussed the utilization and ratings of such drives. Brochurst[19] presented the performance equations of D.C. commutatorless motor using salient pole type synchronous machine.

Tokeda, Morimoto and Hirasa[39] have discussed the generalised analysis for steady state characteristics of D.C. commutatorless motor. The variation of commutation angle, shiftangle, demagnetisation due to armature reaction, safety margin angle, average torque, and speed; with mean input current

are examined quantitatively for cylindrical and salient pole motors.

Katoka[17] has given the steady state characteristics of current source inverter/ double wound synchronous motor system as a variable frequency A.C. power supply, with the help of an equivalent circuit. A method to keep output voltage and frequency constant has been discussed. A simple dynamic model of current fed synchronous motor operating with a constant angle between motor back e.m.f and input current is given by A. Jakubowicz[15]. This mode includes only two time constants, associated with rotor inertia and D.C. link inductance. Akagi and Nabae[30] have presented a control scheme for compensating the torque transfer function of CLM. In this scheme the armature voltage phase and amplitude are altered during transients to compensate for slow response of the field current. H. Naito[28] has determined analytically and verified the dynamic characteristics of lead angle controlled commutatorless motor and has pointed out the instability problems associated with this type of control method. He has taken up a constant δ-controlled CLM provided with a firing angle control scheme in which the leading firing angle is advanced according to the increase of load. A concept of commutation equivalent resistance has been introduced to show that the resistance will become negative in constant δ-control scheme leading to instability and lag of response and it has been pointed out that the feedback of D.C. link current is a counter measure for the above mentioned problem.

In 1983 microcomputer controlled operation of self-controlled synchronous motor employing terminal voltage sensing technique has been studied by Davoine and Perret[38]. In their scheme the standstill position of rotor is computed by microcomputer by analysing and sampling the induced voltage in stator when a step voltage is applied to the field winding. The microcomputer also takes care of starting the motor from standstill by using auxiliary thyristor in parallel of O.C. link inductor.

An attempt was made by Loreth to reduce the cost of CLM so as to make it suitable for low and medium power application by suggesting a novel type of CLM using slip ring induction motor. In this case the rotor is connected to the LCI. The stator windings perform the function of magnetising winding and damper winding.

Emil Levi[37] designed and tested a three phase resonant parallel inverter for induction motors. The commutation of thyristor after every 60^{o} is achieved by the resonance in R-L-C network formed by D.C. link inductor and resistance, parallel capacitor, motor resistance and equivalent inductance.

A design of an induction machine having torque speed characteristics of an induction motor but leading power factor operating capability like an over excited synchronous motor, has been developed by Laithwaite[23], this being known

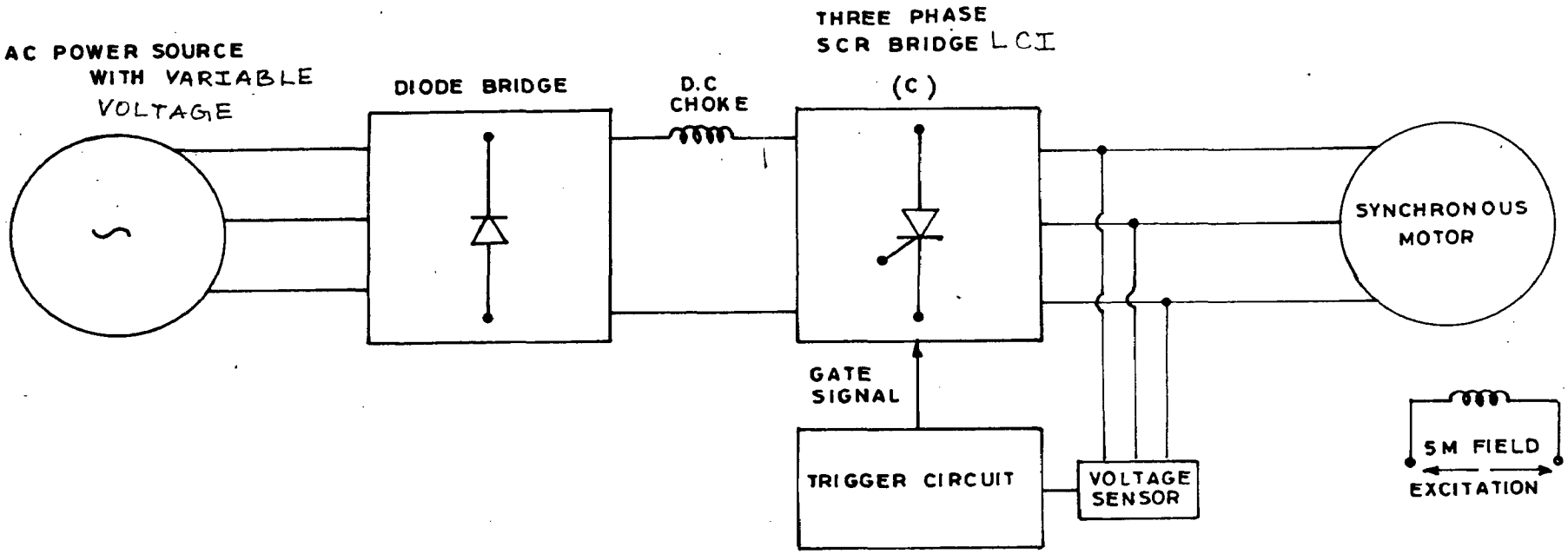


FIG. 1.4 SCHEMATIC DIAGRAM OF LINE COMMULATED INVERTER (LCI)-SYNCHRONOUS MACHINE SYSTEM (COMMULATORLESS D.C. MOTOR)

as θ pinch machine.

An LCI based induction motor drive using capacitors as reactive power sources has been fabricated and tested by B. Singh . The capacitor bank however becomes a source of constant KVAR, thus making the control of reactive power troublesome.

1.7 PRINCIPLE OF OPERATION OF CLM

A commutatorless motor consists of the following essential parts. The block diagram of CLM is as shown in Fig.1.4.

1. A converter (controlled or uncontrolled)
2. An inverter (LCI).
3. A D.C. link inductor.
4. A synchronous motor (overexcited).
5. Firing and control circuits for converter and inverter.

CONVERTER:

This is a 3 phase diode or SCR bridge depending upon whether it is controlled, uncontrolled or semicontrolled. The main function of the bridge is to supply variable D.C. link voltage. The output voltage of converter is varied by changing the firing angle α in case of semi or fully controlled converters, and with an input auto transformer in case of uncontrolled bridge. The advantage of fully controlled operation of the two bridges is that regeneration

is possible by exchanging the mode of operation of the two bridges i.e. rectifier becomes inverter and inverter becomes rectifier. In the present work a 3 phase uncontrolled bridge with an input auto transformer has been used.

D.C. LINK INDUCTOR

This inductor plays the role of smoothening out the ripples in the D.C. link current. The value of this inductor plays a decisive role in the system performance.

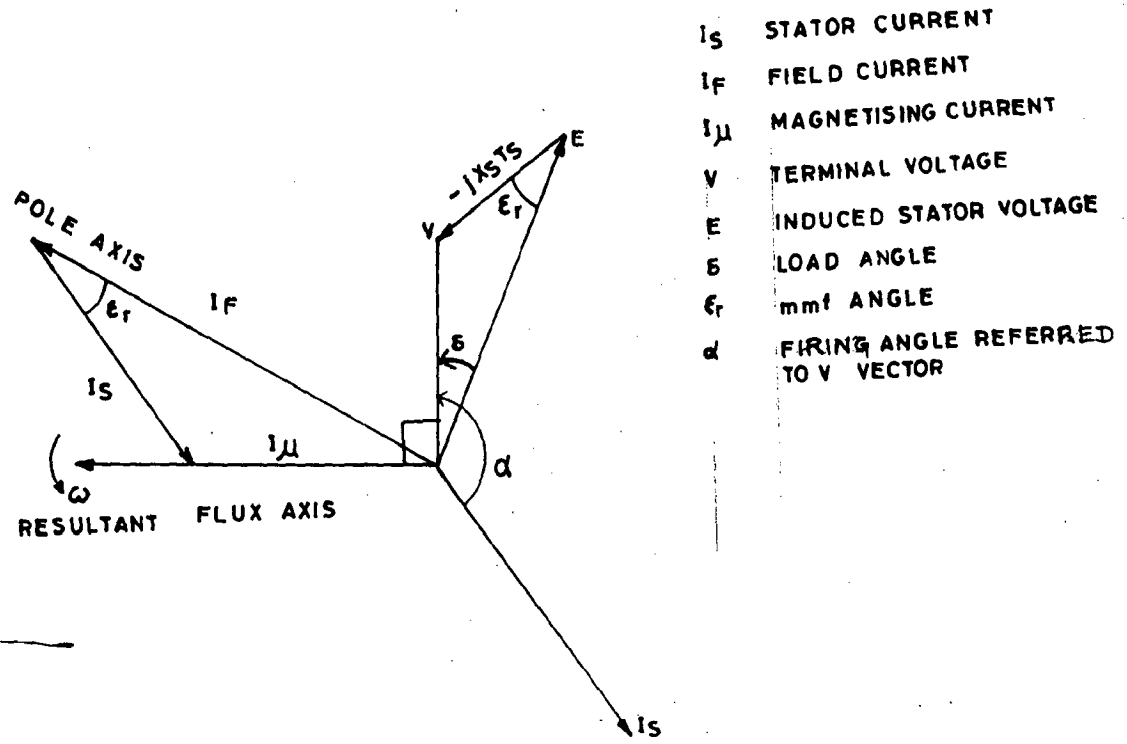
The LCI and synchronous motor constitute a commutatorless D.C. motor. The synchronous machine is over excited and supplies leading reactive power to the inverter. The inverter provides the active power to the synchronous motor for the load connected to it, and to overcome the friction and windage losses.

The firing of inverter SCRs has to be controlled in such a manner that the stator flux maintains a constant angle with rotor mmf. The firing pulses for the SCRs therefore can be derived from the synchronous motor. This can be done in two ways:

1. Rotor position sensor method.
2. Stator terminal voltage sensor method.

ROTOR POSITION SENSOR METHOD

In this method the switching of D.C. link current from one stator phase to another is controlled by motor flux vector. This is dermined by a motor position sensor using optical encoder and a toothed disc mounted on the rotor shaft.



I_S	STATOR CURRENT
I_F	FIELD CURRENT
I_μ	MAGNETISING CURRENT
V	TERMINAL VOLTAGE
E	INDUCED STATOR VOLTAGE
δ	LOAD ANGLE
ϵ_r	mmf ANGLE
α	FIRING ANGLE REFERRED TO V VECTOR

FIG. 1.5 VECTOR DIAGRAM FOR CYLINDRICAL ROTOR SYNCHRONOUS MOTOR

The characteristic feature of this method is that the angle between field mmf and stator mmf vector normally remains fixed. The vector diagram in Fig 1.5 shows the relationship between the firing angle α and rotor angle δ (angle between terminal voltage of stator and induced e.m.f. in stator) from this vector diagram the inverter firing angle is obtained as,

$$\alpha = 90^{o} + \varepsilon_{r} + \delta$$

where, ε_{r} is the angle between field mmf vector and stator m.m.f. vector.

A major drawback of this method is that as the load increases the rotor angle δ increases hence firing angle increases by an equal amount. Thus there exists a possibility of the inverter crossing the inversion limit. This necessiates the fixing of upper limit of α. This leads to poorer utilisation of inverter and motor. The rotor position sensors are also liable to be affected by the environment such as dust, etc. These disadvantages are not present in stator terminal voltage sensor method.

1.7.4 STATOR TERMINAL VOLTAGE SENSOR METHOD:

In this method the firing instants are derived from the terminal voltage of the synchronous machine. Except for the over lap angle effect this method is independent of the operating state of the machine in terms of load current etc.

The only drawback of this method is the inability to determine the firing pulse sequence at the starting instant,

when there is no voltage induced in the stator windings. In case automatic starting of the CLM is required then a number of techniques have been proposed. Some of these are:

1. Addition of a simple Hall effect position detector which is used only for initial position sensing.
2. Injecting a signal of KHz frequency range in a auxilliary winding and analysing the induced stator voltages.
3. Analysing the induced voltages in the stator winding when a step voltage is applied to the field winding.

Since the combination of LCI and synchronous motor constitutes a CLM D.C. motor, hence three types of CLM D.C. motors can be realised depending upon the placement of the field winding

1. Series CLM [33]
2. Shunt CLM
3. Seperately excited CLM.

1.7.5 SPEED CONTROL OF CLM:

The speed of this drive can be changed by varying any one of the following parameters:

1. D.C. link voltage, VdC,
2. Inverter firing angle, α,
3. Synchronous motor field current, I_f.

Thus, the frequency of the output terminal voltage of the

inverter can be given by

$$f = \frac{K\ Vdc}{I_f \cos \alpha}$$

In the present work control of firing angle α is obtained with the help of both type of schemes;

1. Analog firing scheme,
2. Microcomputer based firing scheme.

STARTING OF COMMUTATORLESS MOTOR:

The major drawback with the CLM is it's inability to start from standstill because the gating signals of inverter SCRs are controlled by the synchronous motor itself, and the commutation voltage necessary for machine commutation of LCI is not available. Hence, some other method of commutation of current from one SCR to another is necessary. Several methods are known for this purpose. Some of these techniques are listed by Perret[38].

The automatic starting of CLM is more simplified when microcomputer control is implemented. This method of starting requires two fully controlled SCR bridges. One operating as a machine commutated inverter and one as a fully controlled rectifier supplying D.C. link voltage, Vdc to LCI. The field current control with the help of a single phase converter is optional.

The automatic starting schemes can be broadly

classified into two types:

1. Starting with out an auxiliary thyristor accross D.C. Link inductor,
2. Starting with an auxiliary SCR accross D.C. link inductor.

1.7.7 STARTING WITHOUT AN AUXILIARY SCR:

In this method, commutation is accomplished by forcing the rectifier bridge into inverter mode during a short instant so as to interrupt the D.C. link current and reduce it to zero. Standstill rotor position is sensed by using any one out of the three techniques described earlier. The terminal voltage is sensed and at each interval forced commutation is obtained as follows:

1. Inverter triggering pulses are stopped,
2. Rectifier (three phase) firing is fixed at $\alpha = 150^{\circ}$,
3. D.C. link current is monitored till it becomes zero,
4. Rectifier normal operation is then reestablished and the following SCR pair is triggered.

The main advantage of this technique is that no additional commutating component is required. However, during each commutation interval the motor current is reduced to zero, so that instantaneous torque is zero during this period. This torque zero period is fixed by the machine and converter circuit dynamics, and is undesirable in case of high starting torque requirements.

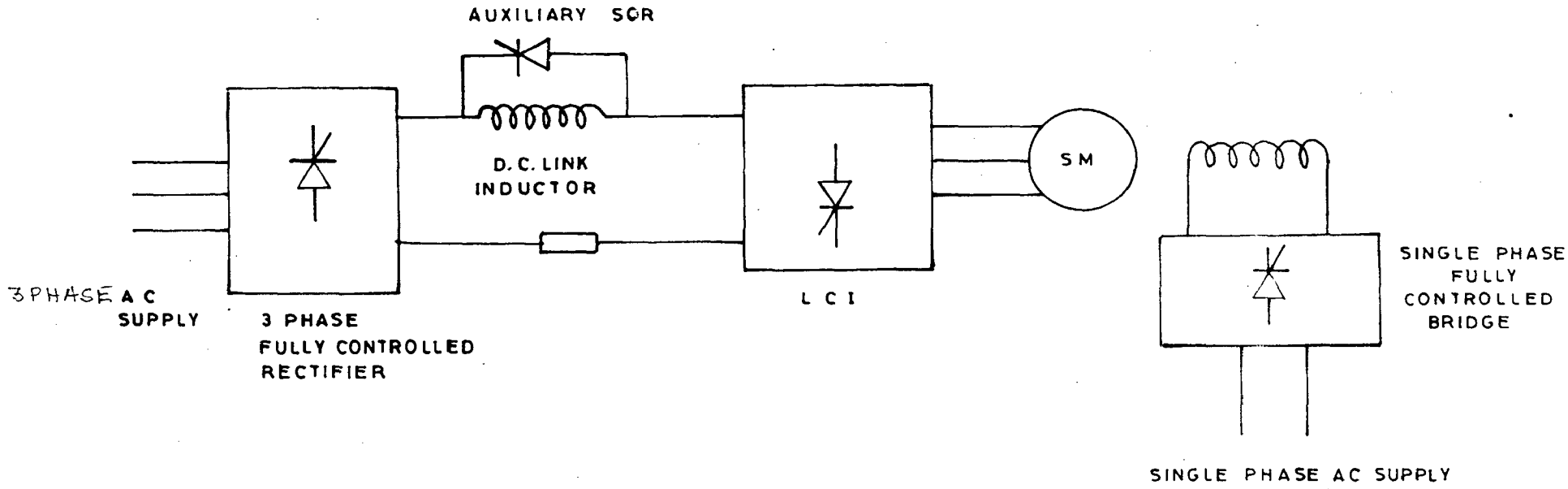


FIG.1.7 POWER CIRCUIT FOR AUTOMATIC STARTING OF CLM USING AUXILIARY SCR IN D.C. LINK

1.7.8 STARTING WITH AN AUXILIARY SCR IN PARALLEL WITH D.C. LINK INDUCTOR:

This method of automatic starting also requires two fully controlled three phase bridges and an additional SCR in parallel with D.C. link inductor as shown in Fig.1.7. Forced commutation during each commutation cycle is achieved following steps:

1. Firing pulses to the two fully controlled bridges i.e. rectifier and inverter are inhibited.
2. The auxiliary SCR is gated.
3. The current through D.C. link is deviated through the auxiliary SCR and thus forced commutation of LCI SCRs is achieved.

This method has been used by Ventatraman[21] with the help of analog control circuitary.

This method overcomes the disadvantage of zero torque during commutation interval obtained in the previous method.

The manual method of starting involves the running of synchronous motor using an auxiliary motor and the gating signals for inverter SCRs are derived from generated e.m.f. of synchronous machine. The auxiliary motor is later cutoff as its current reduces to zero when active power is drawn by the synchronous motor from the LCI.

In the experimental work manual procedure of starting the CLM has been used.

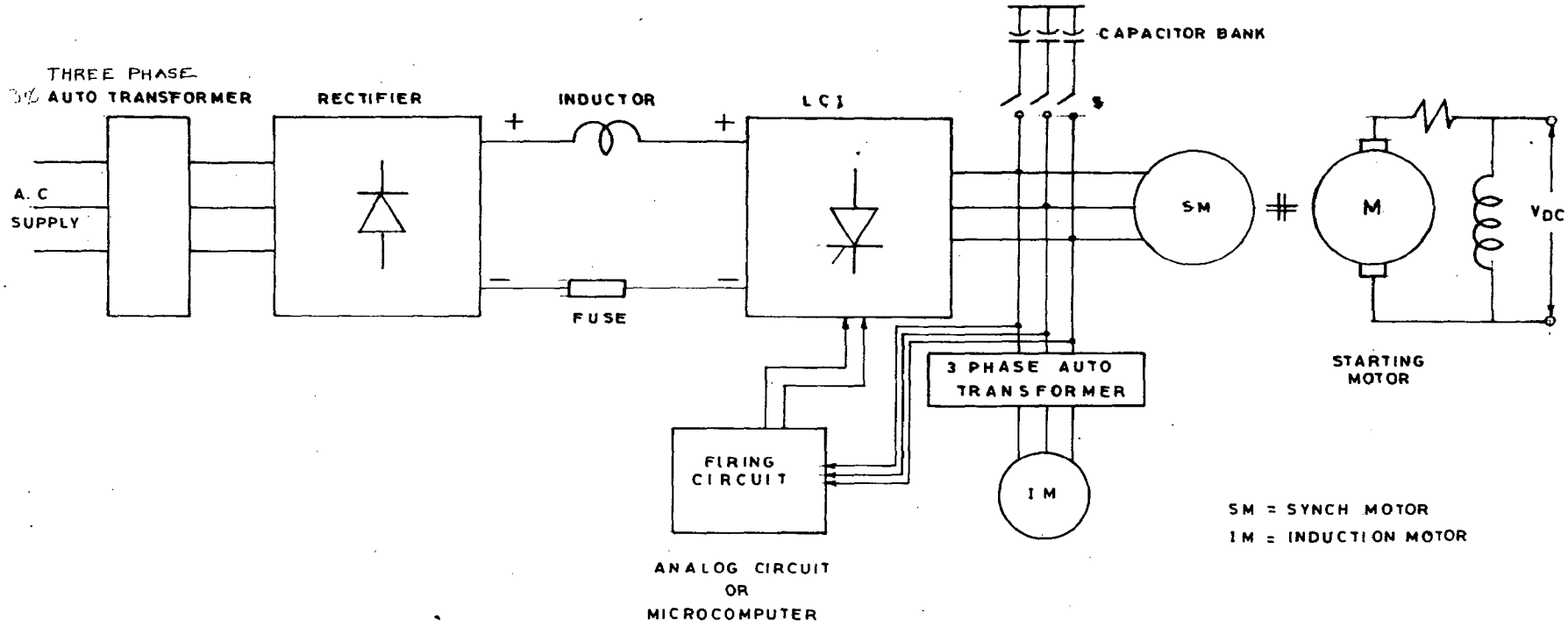


FIG. 1.6 BLOCK DIAGRAM OF CLM - INDUCTION MOTOR SYSTEM

1.8 DESCRIPTION OF CLM - INDUCTION MOTOR SYSTEM:

The block diagram of the experimental system that has been designed, fabricated and tested, is as given in Fig.1.6. Two types of firing and control circuitry have been developed. These are:

1. Analog firing circuit,
2. Microcomputer based firing circuit.

As shown in the Fig 1.6 an auto transformer has been used to connect the induction motor to the 3 phase output of line commutated inverter. This transformer helps in improving the stability of the system by enabling reduced voltage starting of the induction motor. A 3 phase star connected capacitor bank can be connected in parallel with the synchronous machine by closing the switch S. The role of this capacitor bank is only to add investigative flexibility in the system. Otherwise the system can work without this capacitor bank as well. The LCI, D.C. link inductor, converter, synchronous machine, etc. forming the CLM have been described earlier.

1.9 CONCLUSION:

The design and description of the analog and micro-computer based firing circuits, the steady state performance of results of the LCI-SM system and LCI-SM-IM system are given in the following chapters.

CHAPTER II

DESIGN OF ANALOG FIRING AND POWER CIRCUIT

2.1 GENERAL:

This chapter mainly deals with the analog firing circuit design. The design of converter-inverter power circuit also forms an important part of this chapter. The determination of conduction intervals of individual SCRs of the LCI, and the sequence of firing is also discussed.

2.2 THREE PHASE SCR BRIDGE (LCI):

A three phase SCR bridge has been used as a line commutated inverter the commutation of the bridge SCRs is achieved by the back e.m.f of the synchronous motor connected to the three phase output of the bridge as shown in Fig.2.1. The firing angle of the bridge is adjusted between. 90^{o} to 180^{o} so as to obtain the inverter mode of operation. In the inverter mode the direction of current flow through the bridge remains the same however the D.C. terminal voltage of the bridge reverses polarity.Thus,the LCI is nothing but a three phase fully controlled converter with firing angle between 90^{o} to 180^{o}. The sequence of firing of SCRs and the conduction intervals can be explained with the help of a detailed description of 3 phase fully controlled converter.

The power circuit for a three phase fully controlled bridge is same as that of LCI in Fig.2.1. The advantage of the bridge configuration is that it does not place any restriction

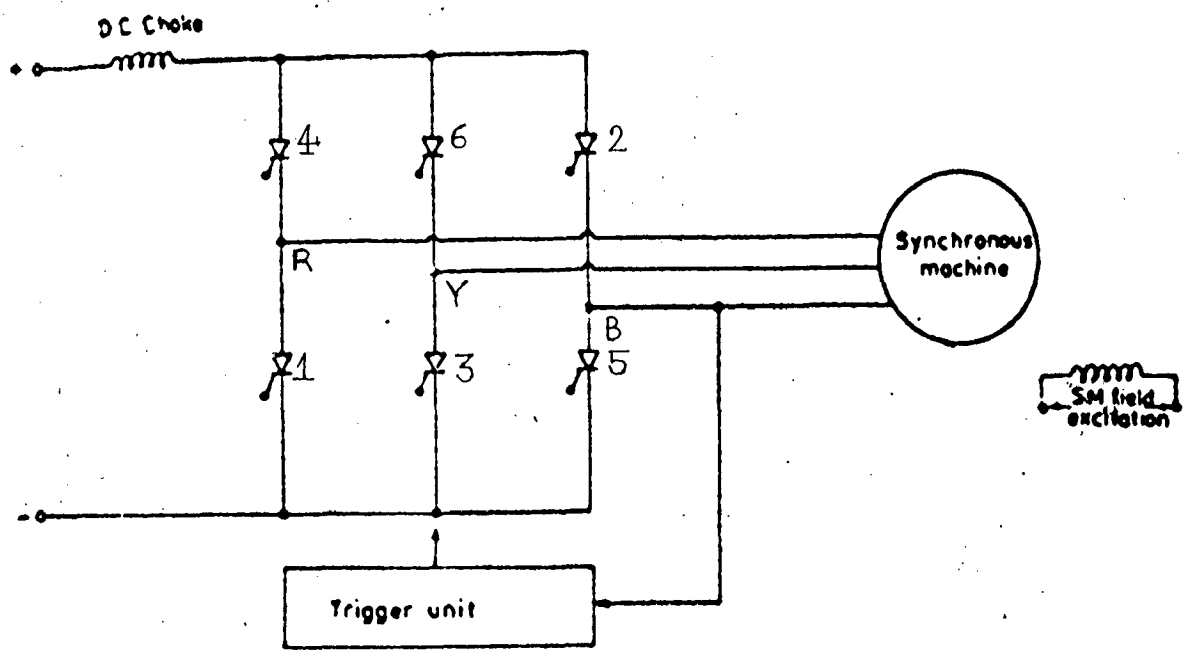


Fig 2.1 Three phase SCR bridge (line commutated inverter)

Table 2.1

Time in degrees	0	60	120	180	240	300
Firing sequence	1	2	3	4	5	6
Conducting SCRs	6,1	1,2	2,3	3,4	4,5	5,6

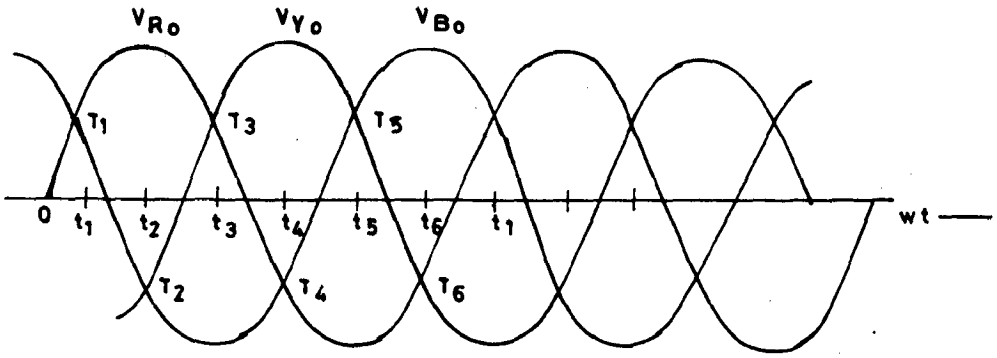


FIG. 2.3 3 PHASE VOLTAGE WAVEFORMS

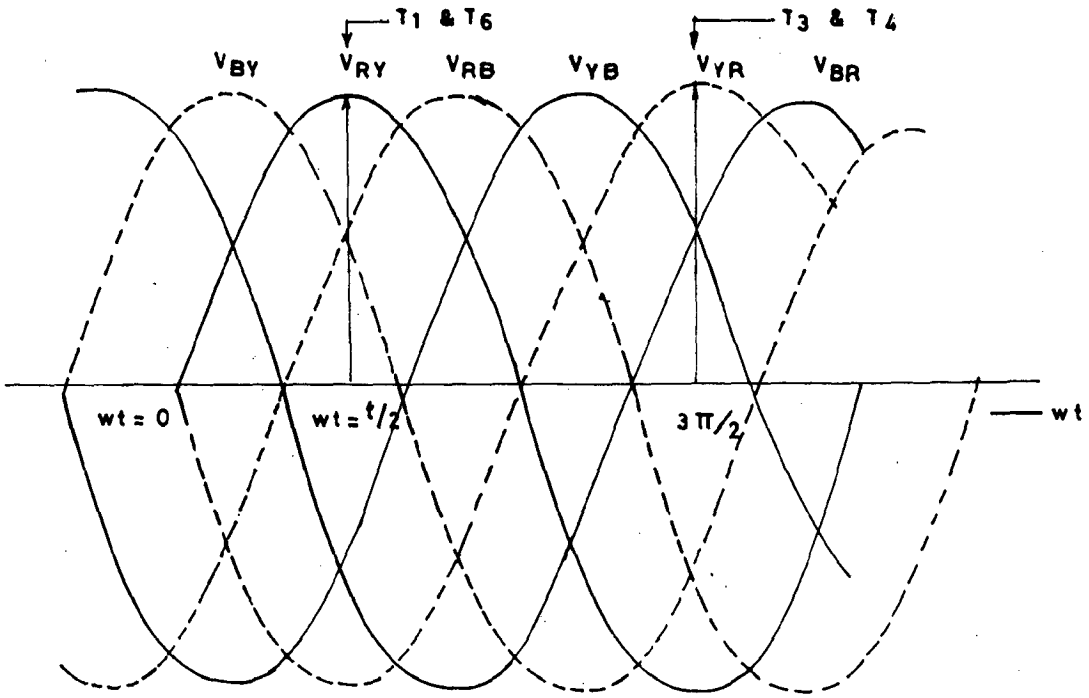


FIG. 2.2 3 PHASE LINE VOLTAGES

S.NO.	wt = 0	SCR TO BE TRIGGERED	MAX. VALUE LINE VOLTAGE
1	t_1	T_1	V_{RY}
2	t_2	T_2	V_{RB}
3	t_3	T_3	V_{YB}
4	t_4	T_4	V_{YR}
5	t_5	T_5	V_{BR}
6	t_6	T_6	V_{BY}

TABLE NO. 2.2

on the connections of the windings of the three phase source (i.e. if it should be star connected or detta connected).

The thyristors T_1, T_3 and T_5 are called positive group SCRs because they conduct when the A.C. supply phase voltage are positive, while the thyrestors T_4, T_6, T_2 are called negative group SCRs because they conduct when the supply phase voltages are negative.

In one cycle of the A.C. supply wave there are six conducting intervals each of 60° in which a pair of SCR conducts. These intervals are as given in Table No.2.1.

The line to line voltages are as shown in the Fig.2.2. When V_{RY} is at its positive maximum i.e. at wt = 90° SCRs T_1 and T_6 are conducting giving

$$V_o = VRY \quad \text{at wt} = \pi/2$$

when V_{RY} is at the negative maximum then SCRs T_3 and T_4 are conducting giving $V_o = -$ VRY at wt = $3\pi/2$. If the other line voltages are also considered then the appropriate pairs of SCRs as given in table 2.1 will be conducting when any one of the six line voltages will be having a greater value than the other five voltages.

From the Fig 2.3 it is clear that the phase voltage VRN is more positive then any other phase voltage in the range of $30^\circ \leq w_t \leq 150^\circ$ i.e. between the two cross over points of V_{RN} and V_{BN} and V_{RN} and V_{yN}. The SCR in the positive

group and in the red phase arm i.e. the T_1 can conduct in this interval. If the SCR is replaced by a diode then it would start conduction from $\omega t = 30^\circ$; hence t_1 point is the reference point for firing angle α of SCR T_1. The reference points for other SCRs are also determined in the same manner and are as given in Table no.2.2. The table also lists the line voltage having zero magnitude at each reference point. Thus, the reference point for measuring firing angle can either be taken as cross over points of phase voltages or the zero crossing points of line voltages.

The firing angle of the converter can be varied from 0° to 180°, however practically it is varied from the minimum value of 10° to the maximum value of 165°. There are two modes of operation of the fully controlled three phase bridge converter depending upon value of load inductance.

1. Discontinuous current mode,
2. Continuous current mode.

2.3 DISCONTINUOUS CURRENT MODE:

The converter in this mode operates only as a rectifier. The load is generally resistive i.e. with low inductance. The rectifier operation starts from $\alpha = 0^\circ$ upto $\alpha = 120^\circ$, when the output voltage becomes zero. The voltage Vdc versus firing angle α plot for resistive load is as shown in Fig.2.4. The D.C. output voltage upto $\alpha = 60^\circ$ is same as in case of continuous conduction mode of operation, this is due to the fact that the upto $\alpha = 60^\circ$ the output voltage of converter even in case of

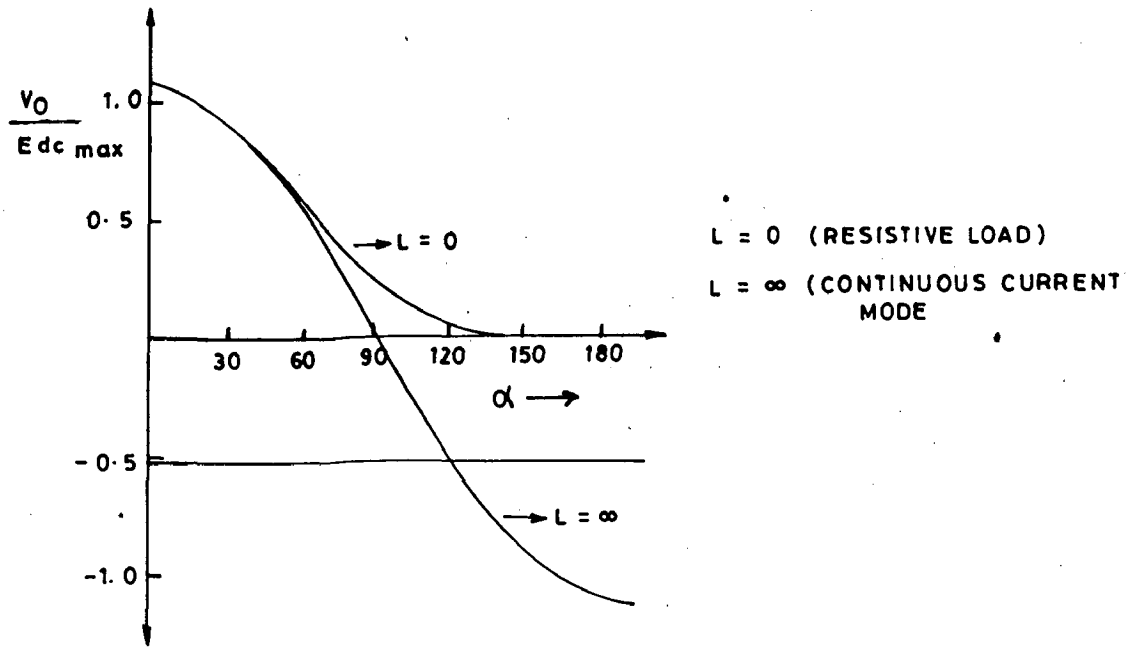


FIG. 2.4 OUTPUT VOLTAGE OF THREE PHASE FULLY CONTROLLED BRIDGE AS A FUNCTION OF FIRING ANGLE

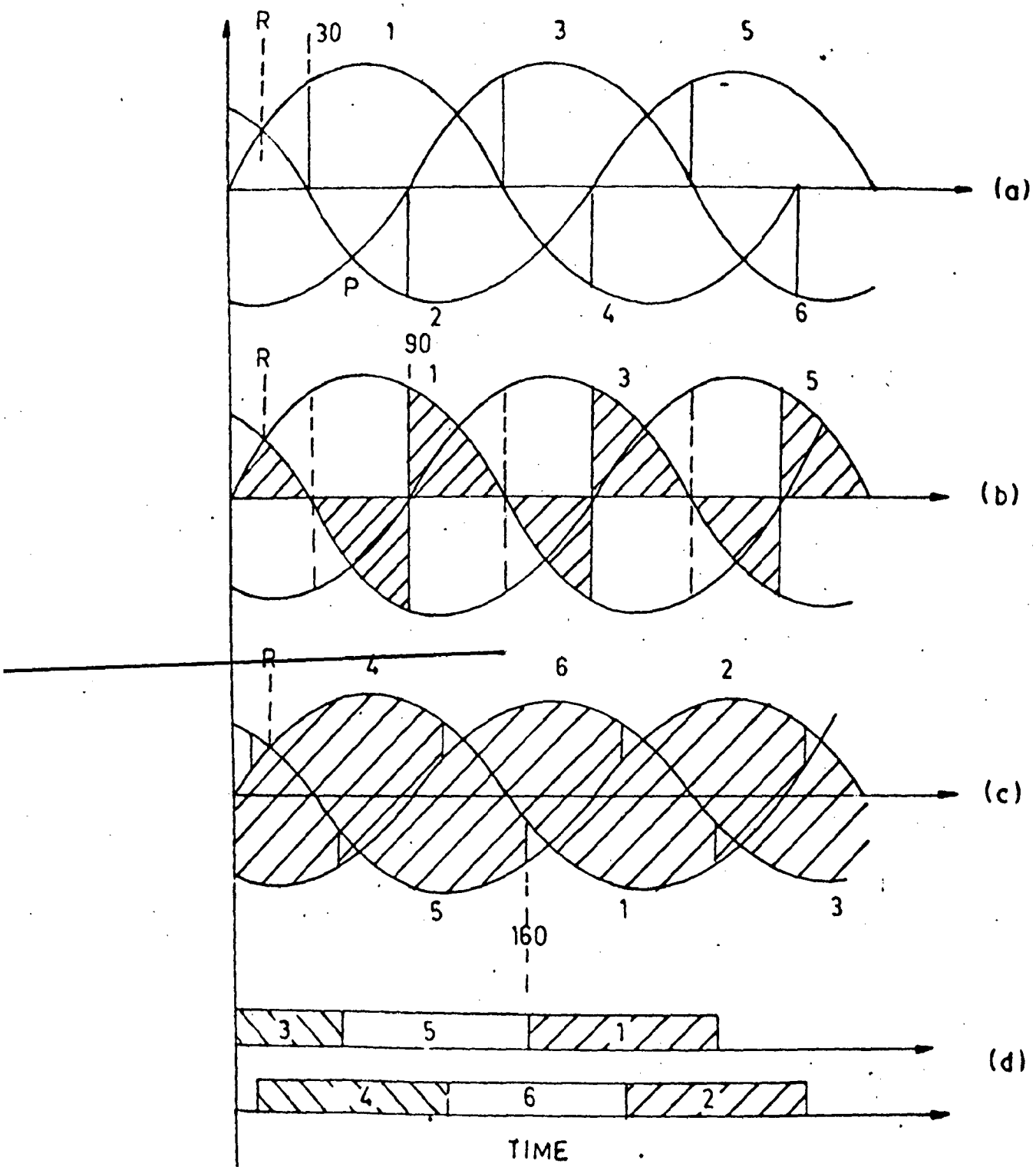


FIG-2.5 Theoretical waveform of voltage across the bridge

(a) Firing angle 30 degrees

(b) Firing angle 90 degrees

(c) Firing angle 160 degrees

(d) Conducting SCRs

continuous conduction, does not become negative hence the D.C. output of both discontinuous conduction and continuous conduction modes are the same. As the load is almost purely resistive with negligeble value of inductance hence when α becomes greater then 60° the bridge voltage output is unable to become negative because of low load inductance the load current almost follows the voltage waveform. Hence the converter operates upto $\alpha = 120^{\circ}$ as rectifier with resistive load. After $\alpha = 120^{\circ}$ the output voltage of the bridge becomes zero.

2.4 CONTINUOUS CURRENT MODE:

In this mode of operation the load current of the bridge is maintained constant by the large value of load inductance. Thus, in this mode of operation the current will be maintained constant even if the output voltage becomes negative. The relation,

$$V_{dc} = \frac{3\sqrt{3}}{\pi} \text{ Emph cos } \alpha \qquad \ldots \qquad (2.1)$$

gives the output voltage for a particular value of firing angle, for this mode of operation. The Fig 2.4 gives the output voltage variation with firing angle α. Fig. 2.5 give, the output voltage wave forms of the converter for $\alpha = 30^{\circ}$, $\alpha = 160^{\circ}$ and $\alpha = 90^{\circ}$, in continuous current mode of operation. It is evident from these waveforms that as firing angle α reaches 90° the output voltage reduces to zero. As the firing angle α is increased above 90° then the output

voltage becomes negative. Thus now the converter starts operating in the inverter mode i.e. if a D.C. source of proper polarity is connected accross its D.C. terminals then power will be delivered from the D.C. source to the three phase side. This mode of operation (i.e. the line commutated inverter mode) is of special interest in the thesis work.

Finally it is clear that for continuous load current there are two modes of operation depending upon value of α they are,

(1) Rectifier $0 \leq \alpha \leq 90$,

(2) inverter $90 \leq \alpha \leq 180^{\circ}$.

2.5 EFFECT OF SOURCE INDUCTANCE ON THREE PHASE BRIDGE CONVERTER(F.C):

The discussion upto now was based on the assumption that the source inductance is absent, however this is rarely true. The source normally has some inductance, this does not allow instantaneous current commutation in SCRs. The commutation of SCR T_5 is explained with the help of Fig.2.6, when an SCR i.e. T_5 is the positive group is undergoing commutation, the incoming SCR i.e. T_1 of positive will also start conducting resulting in conduction of three total SCRs. Two in positive group and one in negative group. The effective result is that a commutation over lap region is obtained. The current in the outgoing SCR T_5 reduces to zero and the current in the incoming SCR i.e. T_1 gradually rises to the full value

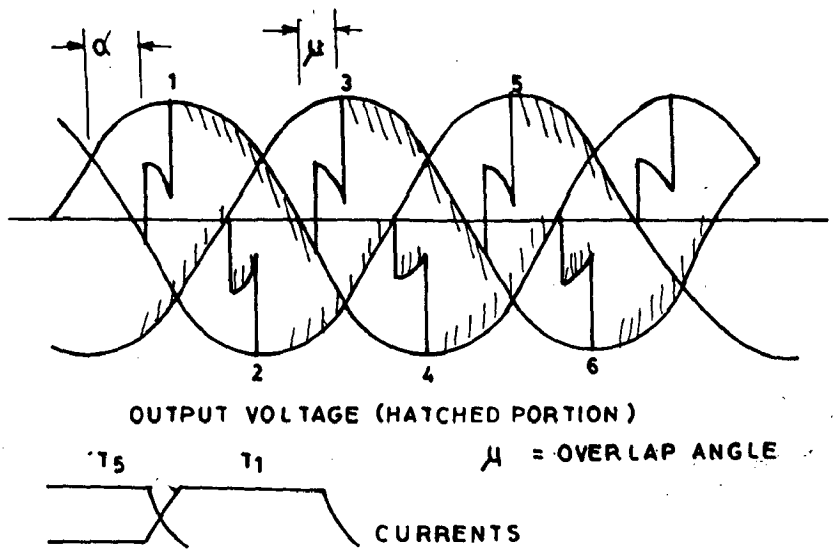


FIG. 2.6 VOLTAGE AND CURRENT WAVEFORMS OF A 3 PHASE f.c. BRIDGE WITH COMMUTATION OVERLAP ANGLE

as shown in Fig 2.6. This figure also gives the output voltage waveform including commutation overlap regions. In case of three phase bridge converter there will be six commutation overlap regions in one cycle.

The reduced output voltage due to commutation overlap is given by equation 2.2 [ ]

$$V_{dc} = \left[\frac{3\sqrt{3}}{\pi} E_{mph} \cos \alpha - \frac{3wL_s I_L}{\pi} \right]$$

The overlap angle is generally represented by the symbol μ it depends up,

1. Number of phases,
2. Load current,
3. Source inductance.

Depending upon the value of commutation overlap angle there are three modes of operation[1] of the fully controlled three phase bridge.

1.	Mode I	$\alpha < 60^{\circ}$	two and three SCRs conducting
2.	Mode II	$\alpha = 60^{\circ}$	three SCRs conducting
3.	Mode III	$\alpha \geq 60^{\circ}$	three and four SCRs conducting

normally the bridge operates in the mode I.

The commutation overlap angle effects the performance of the converter is a number of ways[3] they are,

(i) The wave shape of the output voltage is altered. The

output voltage during overlap is the mean of voltages of out going and in coming phases,

(2) The reduction in output voltage is proportional to load current giving a sort of regulation property to the converter, and can be considered as a equivalent resistance in series,

(3) The input current waveforms are rounded at edges this results into the reduction of harmonic currents. The individual current segments are streched,

(4) At the input to the converter commutation notches are produced in the line and phase voltages, subjecting the thyristors to excessive dv/dt,

(5) In the inverter operation the commutation of SCRs depends upon the negative voltage of mains. The overlap reduces the negative voltage interval necessiating the reduction of maximum delay angle i.e. α.

2.6 DESIGN OF FIRING CIRCUIT FOR LCI:

It has been discussed in the preceeding section that the six SCRs T_1 to T_6 are to be fired sequencially at an interval of 60° in one cycle of A.C. wave. Each SCR conducts for an interval of 120° and with two SCRs of opposite group and of the remaining two phases. It has earlier also been explained that the reference points for SCR firing angle α, can either be obtained from the cross over points of phase voltages or the zero crossing points of the line voltages.

In the analog firing circuit developed the synchronous

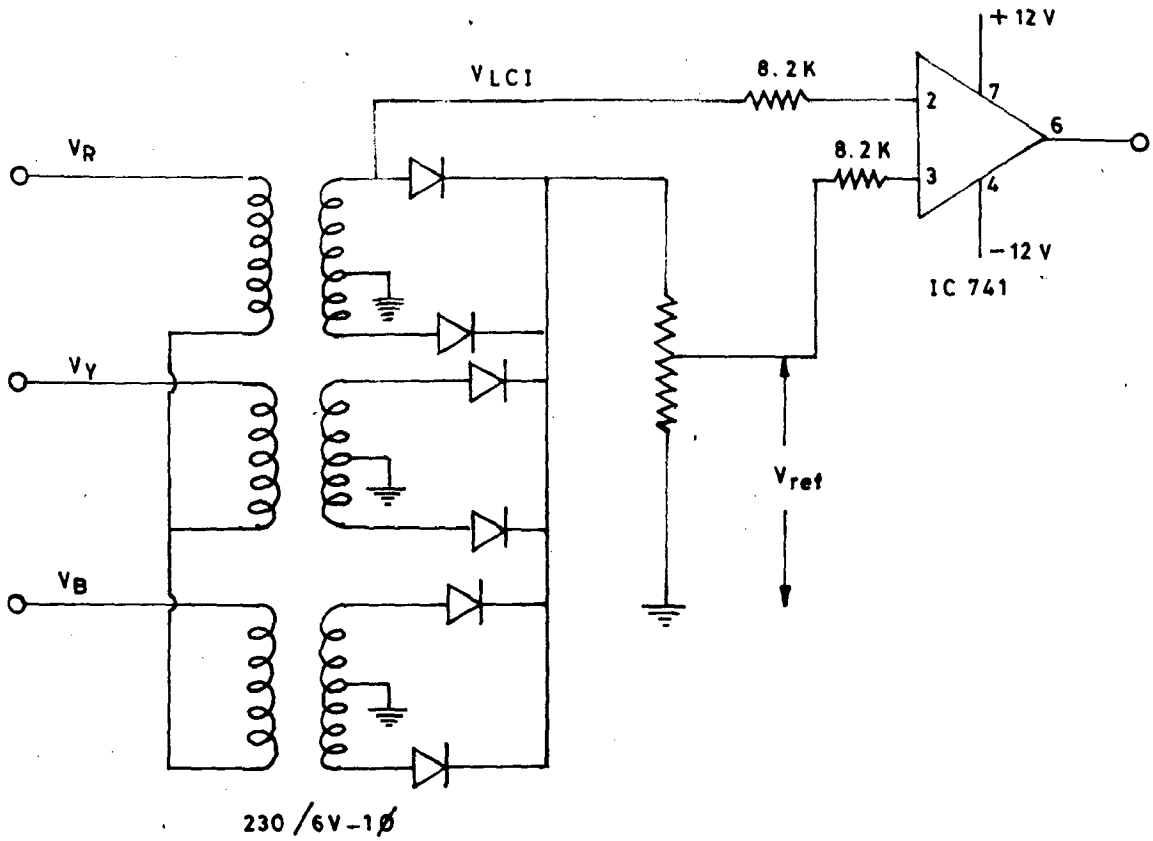


FIG. 2.7 COSINE FIRING SCHEME TO OBTAIN FIRING ANGLE α AT VARIABLE FREQUENCY

motor terminal voltages or the LCI output voltages are stepped down using a three phase^{Y} connected, 230 /6V transformer, and then compared with a D.C. reference voltage V_{ref} for obtaining the firing angle α as shown in Fig 2.7.

The output voltage and frequency of LCI are not constant and the voltage waveforms have to be sensed to derive the firing pulse for the control of commutator less motor (LCI-SM). Since the frequency and voltage magnitude are changing continuously, it is not possible to obtain the same value of firing angle α with a constant value of V_{ref}. Thus in order to maintain α constant at different operating frequencies, V_{ref} signal should be derived in such a way, that it's value is frequency independent. This is achieved by deriving the V_{ref} signal from the variable output of a pot. The voltage input to the pot is the rectified stepped down output of LCI. Thus now as the frequency of LCI output signal changes for a constant excitation of S.M., then the LCI terminal voltage will also change proportionally, changing the value of V_{ref} in the same ratio. It can be analytically shown that firing angle α becomes frequency independent when V_{ref} is derived from LCI voltage.

$$V_{LCI} = KxfxCos\ wt \qquad \ldots \qquad (2.3)$$

$$V_{ref} = K_1'xf \qquad \ldots \qquad (2.4)$$

K and K' are constants

$$Cos\ wt = \frac{K'}{K}$$

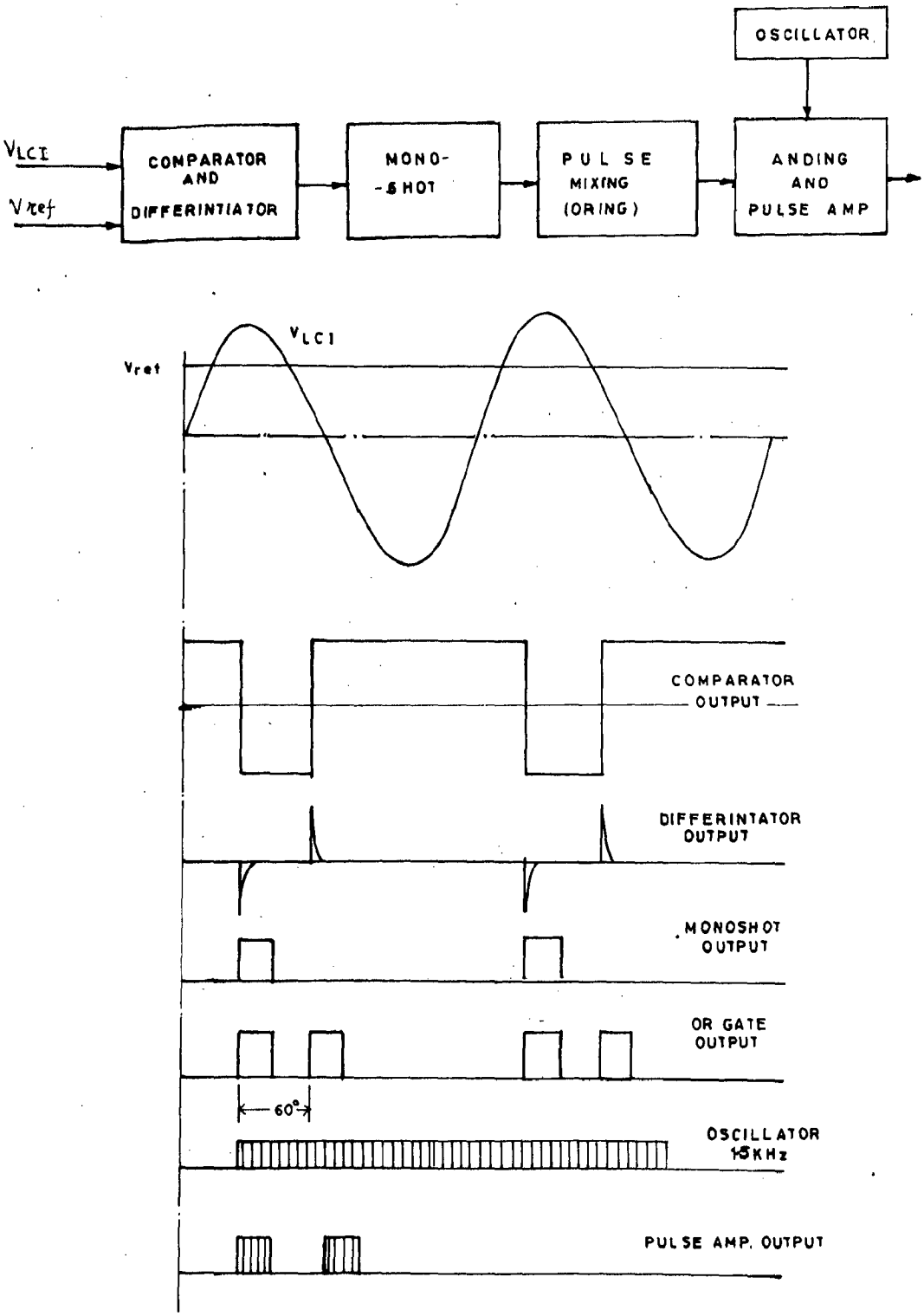


FIG. 2.8 BLOCK DIAGRAM OF ANALOG FIRING CIRCUIT

Now $wt = \alpha \quad \therefore \quad \alpha = \cos^{-1}\left(\frac{K'}{K}\right)$ ... (2.5)

The block diagram of the firing circuit is shown in Fig.2.8. It consists of following parts:

1. 3 phase signalling, Y/Y connected transformers,
2. Comparators,
3. Differentiator,
4. Monoshot,
5. OR gates,
6. AND gates,
7. Pulse amplifiers,
8. High frequency oscillator.

2.6.1 SIGNAL TRANSFORMERS:

Three single phase, 240/6V transformers with centre tapped secondaries are connected in Star/star configuration. The six phase voltage waveform required for comparison with V_{ref} are obtained from the centre tapped secondaries.

2.6.2 COMPARATOR:

IC 741 is used as a comparator. It compares the stepped down phase voltage connected to its pin, number 2 with V_{ref} applied to its pin No.3. The output waveform of comparator is shown in Fig.2.8.

2.6.3 DIFFERENTIATOR:

The output of the comparator is differentiated with the help of simple R C differentiator the RC components are

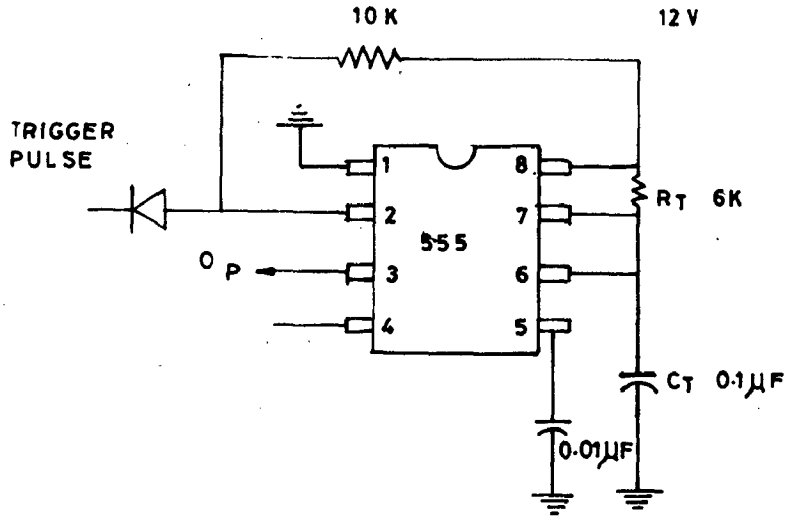


FIG. 2.9 MONO STABLE MULTIVIBRATOR USING IC 555 TIMER

designed with suitable valves so that it can work satisfactorily in the frequency range of 5 to 100 Hz

$R = 10K$ $\qquad C = 0.01\ \mu F$

2.6.4 MONOSHOT:

A negative edge tuggered monoshot has been fabricated using IC 555 timer in monostable configuration the value of various components and the circuit are given in Fig 2.9. The value of the timing components R_{ex} and C_{ex} is selected on bases of the required pulse width of monoshot output that would be sufficient to trigger the thyristor to ON state

$$T_{ON} = 1.1\ R_{ex}\ C_{ex}$$

taking $T_{ON} = 600\ \mu$ Sec $\qquad C = 0.1\ \mu F$

$R_{ex} = 6$ K Ohms

2.6.5 OR GATING:

The six pulses for triggering the individual SCRs can be obtained from the monoshot outputs. However, in a three phase bridge an SCR conducts with two SCRs of opposite group for an interval of 120°. The turning on of the conducting SCR is ensured by oring the pulse of the conducting SCR with the pulse of the in coming SCR, coming after an interval of 60°. The second pulse is known as the slave pulse and the first pulse is the master pulse. The oring sequence of pulses

$$T_1+T_2,\quad T_2+T_3,\quad T_3+T_4,\quad T_5+T_4,\quad T_6+T_5,\quad T_6+T_1$$

in terms of phase voltages the sequence can be given as

$$V_R^+ + V_B^-,\quad V_B^- + V_Y^+,\quad V_Y^+ + R^-,\quad R^- + B^+,\quad B^+ + Y^-,\quad Y^- + R^+$$

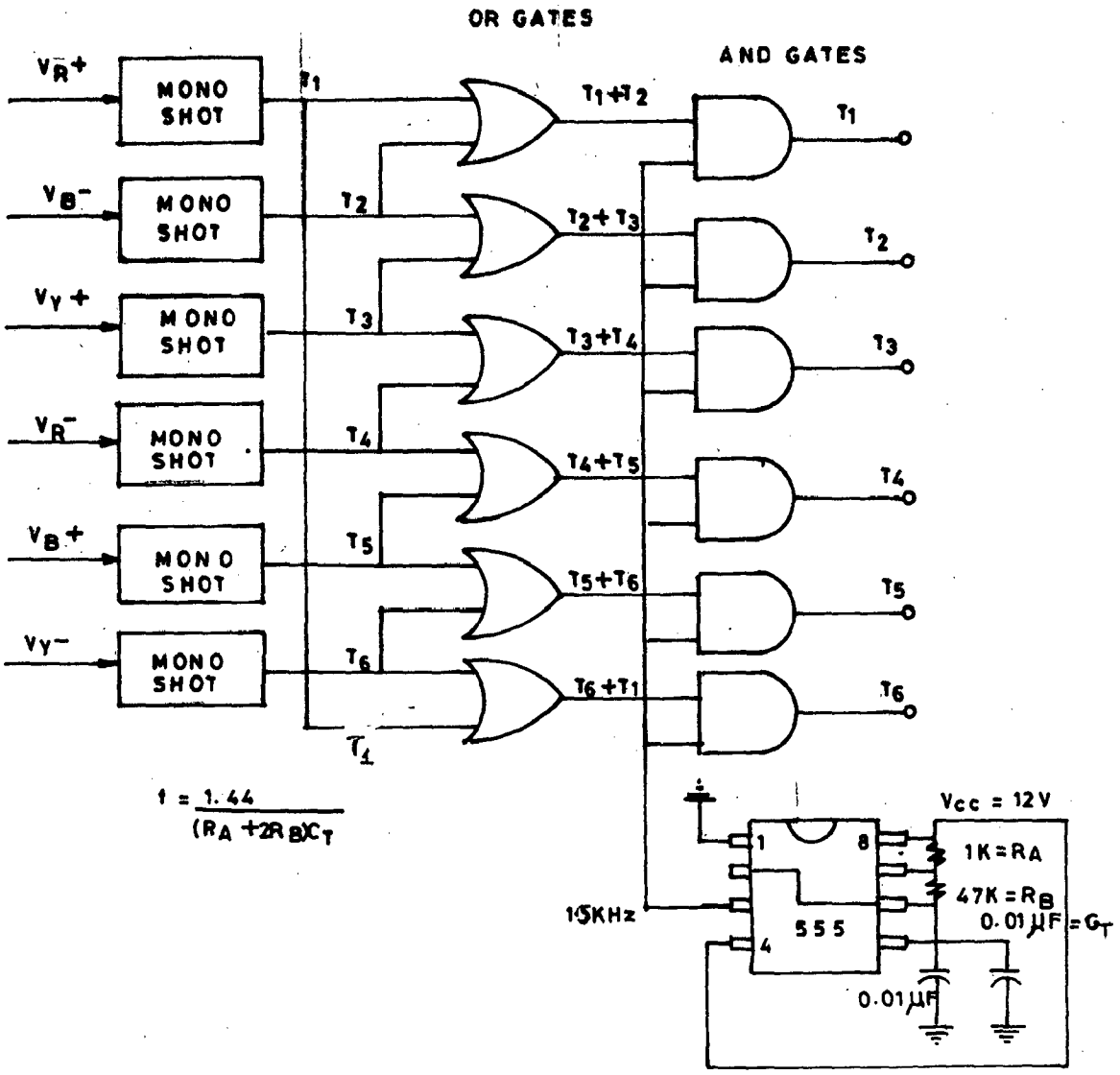


FIG. 2.10 PULSE MIXING OF SIX MONOSHOT OUTPUTS

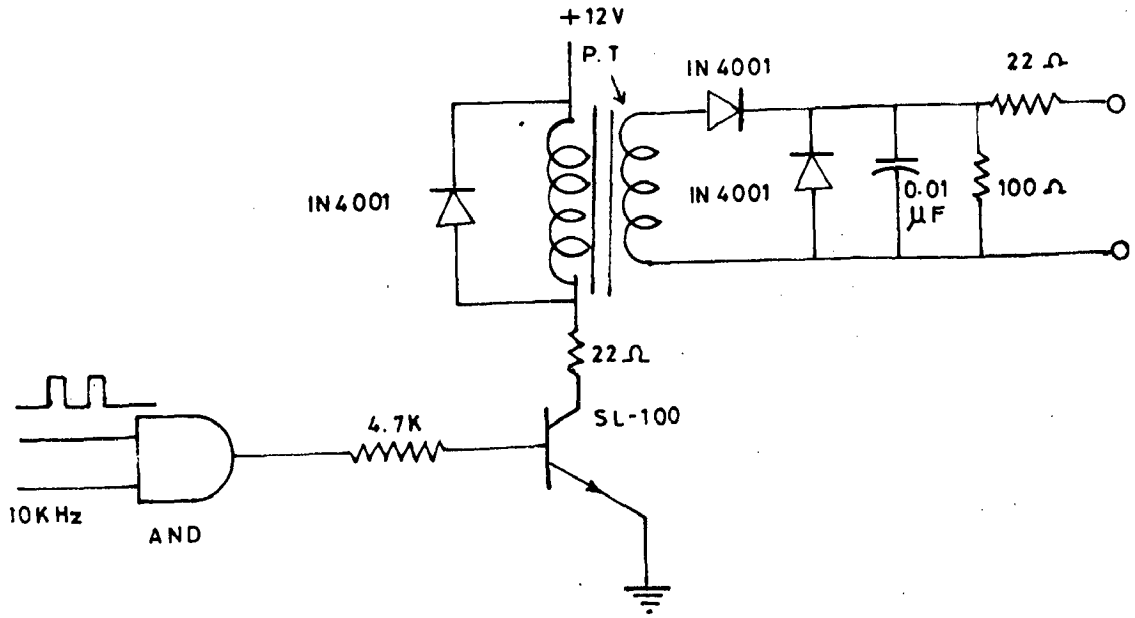


FIG. 2.11 PULSE AMPLIFIER

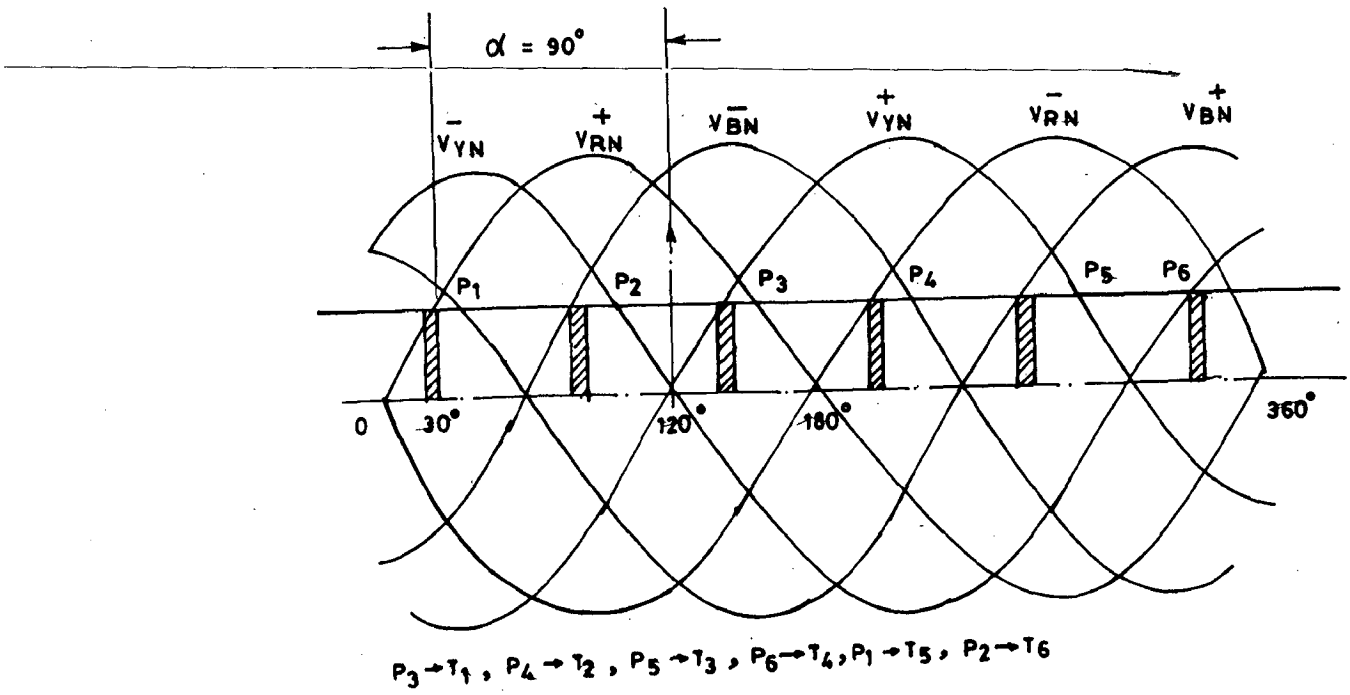


FIG. 2.12 PHASE ADVANCING TECHNIQUE IN CASE OF Y/Y CONNECTED ANALOG FIRING SCHEME

The pulses derived from the indicated phase voltages are OR gated using IC 7432.

2.6.6 AND GATING:

The master slave output of the six OR gates become the six firing channels as shown in Figure. The Fig 2.10 gives the OR gated signals and with the SCR number to which it is to be given. These OR gate outputs are low frequency outputs hence they are ANDED with a high frequency modulating signal obtained from IC 555 oscillator with a frequency of 1.5 K Hz., this prevents the saturation of pulse transformers in the pulse amplifier circuits.

2.6.7 PULSE AMPLIFIER:

The strength of the AND gate output pulses is amplified using the pulse amplifier circuit shown in Fig 2.12. A pulse transformer is used for isolating the power circuit from the firing circuit. The diode connected accross the primary winding provides the path for free wheeling of stored inductor energy of transformer is off state.

2.7 DESIGN OF POWER CIRCUIT:

The power circuit for the present work consists of the following parts:

1. Three phase fully controlled bridge(LCI),
2. Three phase diode bridge,
3. D.C. link inductor.

A power circuit panel board has been fabricated to house the

converter, inverter bridges. The design ratings of SCRs and diodes for the bridges must be such that they should not be exceeded when maximum power is being delivered by the circuit.

2.7.1 CHOICE OF RATING OF RECTIFIER BRIDE DIODES:

The power circuit has been designed to supply an active load of I_{RMS} = 25 A at V = 400V input to the three phase bridge. Thus the D.C. link current for this A.C. current can be obtained from the relation,

$$\frac{I_{RMS}}{I_{dc}} = 0.816 \qquad \text{(for three phase bridge)}$$

$$I_{dc} = 0.816 \times I_{RMS}$$

$$= 30.63 \text{ Amp.}$$

The voltage rating of the diodes of the uncontrolled bridge have to be selected with the consideration of the peak inverse voltage appearing accross the device, this in turn depends upon the maximum three phase input line voltage to the bridge. The maximum line voltage is 400V at 50 Hz. Therefore the PIV accross each diode is

$$\frac{V_{PIV}}{V_{LN}} = 2.45 \quad (120^{\circ} \text{ conduction, three phase bridge})$$

$$V_{PIV} = 2.45 \times \frac{400}{\sqrt{3}}$$

$$= 566 \text{ Volts}$$

A safety factor of 2 is kept so that the diodes can easily take reasonable transient over voltage. Thus, diodes having a

PIV rating of 1200V are selected. The ratings of the diodes selected are listed below.

1. Mean forward current = 25 Amps.
2. Type = HR/HN D-25
3. Maximum case to stud
4. temperature = 120°C
4. Maximum junction temperature = 150°C
5. Repetative peak value of current = 130 Amps
6. Thermal resistance junction to case = 1.3°C/W

2.7.2 SELECTION OF RATINGS OF SCR FOR LCI BRIDGE:

The following below given factors have to be considered for selecting the ratings of the SCR

1. The power circuit configuration.
2. Conduction angle of individual SCR.
3. Current waveform.
4. Average current.
5. Maximum PIV appearing accross the device.

A three phase SCR bridge has been chosen as the line commutated inverter. The maximum value of line voltage accross the SCRs of the bridge is governed by the maximum voltage rating of the synchronous motor which is 400V for the present thesis work.

For a three phase bridge the ratio of peak reverse voltage to line to neutral voltage is given by

$$\frac{E_{PIV}}{E_{LN}} = 2.45$$

$$E_{PIV} = \frac{400}{\sqrt{3}} \times 2.45$$

$$= 566 \text{ V}$$

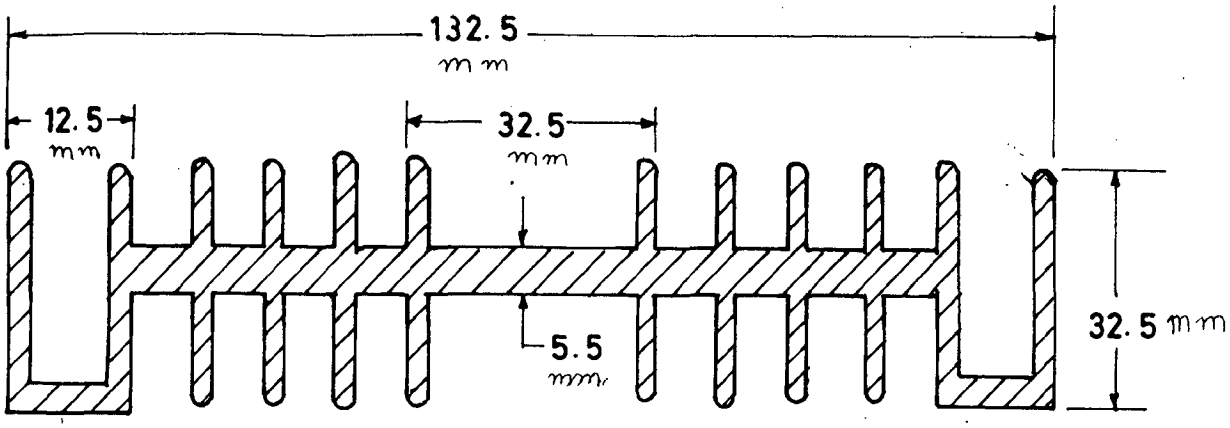
Taking a safety factor of 2, a 1200 V SCR is required. Hence, BTW -39 has been selected. The RMS current rating of the SCR is 25 Amps. The detailed ratings of the SCRs are as given:

1. Manufacturer = Solid state Electronic Pvt. Ltd
2. PIVs = 1200 V
3. I_{rms} = 25 Amps
4. T_{jm} = 125°C
5. V_{GT} = 3.0 Volts
6. I_{GT} = 80 mA
7. $I_{T(av)}$ = 16 Amps.
8. P_D = 30 W
9. dV/dt = 200V/ μS (minimum)
10. di/dt = 100A/ μS (maximum)
11. I^2t = 200 A^2Sec (t < 10mS)

Hence under full load conditions the SCR and diode bridges can deliver a maximum value of I_{dc} = 30.6 Amps.

The power circuit diagram for the panel board is as shown in Fig 2.14(b). The power dissipation of the individual thyristors at a conduction angle of 120° is 30 Watts. The maximum allowable temperature of the device is 120°C. Assuming an average ambient temperature of 40°C, the maximum temperature rise allowable will be

$$120^\circ\text{C} - 40^\circ\text{C} = 80^\circ\text{C}$$



SH - 132

1. HIGH GRADE ALUMINIUM ALLOY
2. ANODISED BLACK
3. THERMAL RESISTANCE
   a) NATURALLY COOLED = 1.2 °C / WATTS
   b) FORCED COOLING (5 M/SEC) 0.35°C / WATTS

FIG. 2.13 SECTIONAL PLAN OF HEAT SINK

Thus the total thermal impedance from the thyristor to ambient should not exceed $80^{\circ}C/30W = 2.66^{\circ}C/W$

Let,

R_{CH} = Thermal impedance case to heatsink

R_{HA} = Thermal impedance heatsink to ambient.

R_{CA} = Thermal impedance case to ambient

$$R_{CA} = R_{CH} + R_{HA}$$

$$R_{HA} = R_{CA} - R_{CH}$$

$$= 2.66 - 0.3$$

$$R_{HA} \leq 2.36^{\circ}C/W.$$

Thus the thermal impedance for the heat sink should be less than 2.36 $^{\circ}C/W$. Heat sinks with $R_{HA} = 1.2^{\circ}C/W$ (natural cooling), have been selected. The sectional diagram of heat sink and its ratings are as given in Fig 2.13.

2.8 CONCLUSION:

The range of firing angle α obtained by adopting the sequence of firing discussed in this chapter. In case of Y/Y connection is from 150 to 160 and from 0 to 60 i.e. 30° in inversion range and 60° in rectifier range. Hence to obtain α in the range of 90° to 180 a pulse advancing technique is used The pulses and the phase voltages are as given in Fig 2.12. From the Fig 2.12 it is clear that if the pulse derived from Y + phase voltage is used to fire the T_1 SCR (i.e. all the SCRs are given pulses 120° behind their original pulses) a full variation of α from 90 to 180° may be obtained for V_{ref} changing from 0 to V_{ref} max.

Even after phase advancing the analog firing scheme using Y/Y connected signal transformers has a number of disadvantages. They are

1. Non-sinusoidal voltages due to Y/Y connection., These may lead to shifting of firing pulses leading to commutation failure and instability,
2. Non-linear variation of firing angle with the change in reference Voltage V_{ref}.

Due to these disadvantages the micro computer scheme for control of firing angle was preferred.

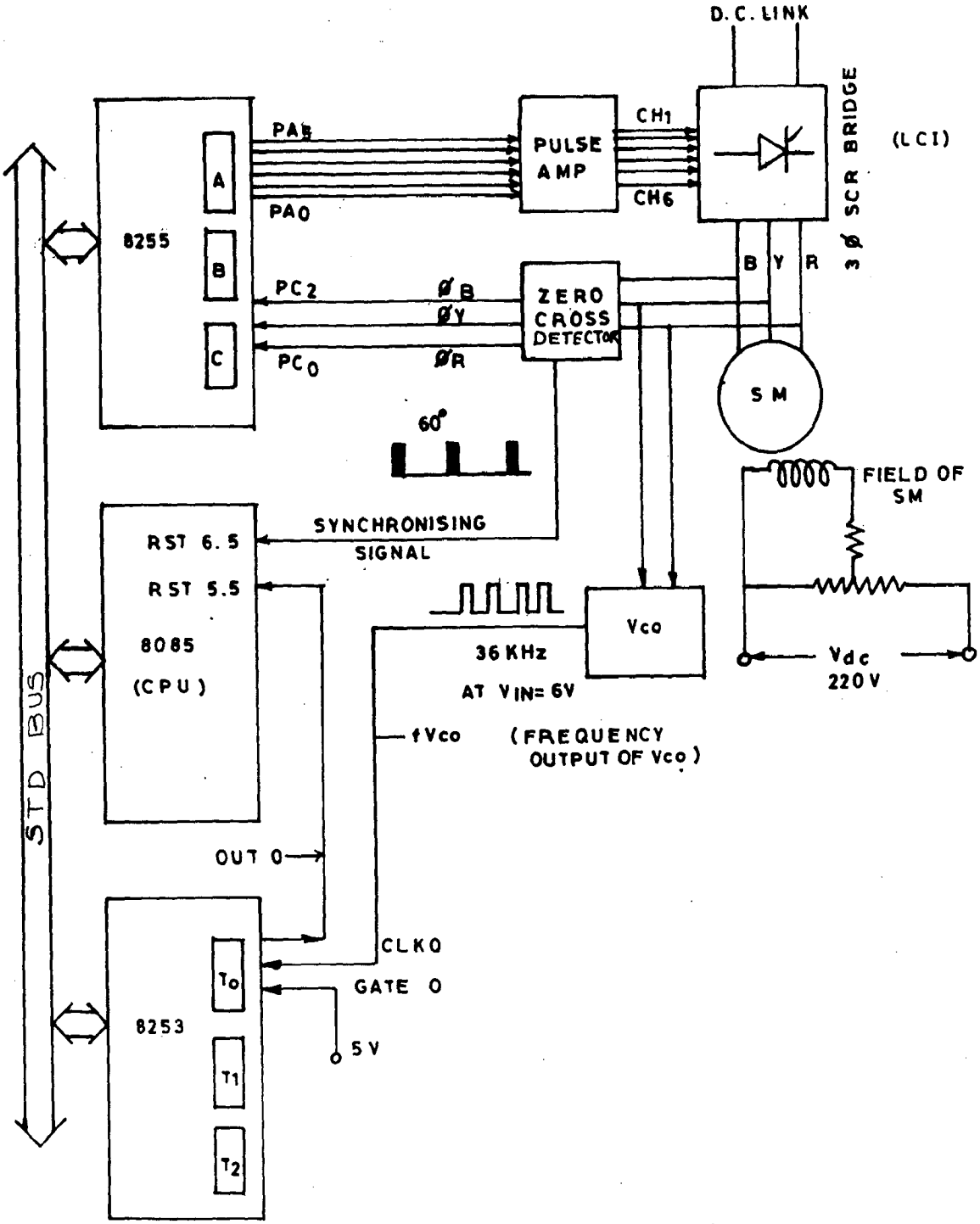


FIG. 3.1 BLOCK DIAGRAM OF LCI FIRING ANGLE CONTROL SCHEME

CHAPTER III

MICROCOMPUTER BASED FIRING SCHEME FOR LCI

3.1 GENERAL:

In this chapter the microcomputer based LCI firing angle control scheme philosophy has been explained. Further, the development of software for the scheme is explained with the help of flow charts.

The disadvantages of analog firing scheme used for control of LCI-SM system are as follows:

1. Variation of firing angle α is limited to 90° by using cosine firing scheme,
2. The harmonic content of the voltage waveform of LCI can disturb the firing pulse instants, leading to misfiring of LCI,
3. The firing sequence of SCRs is different for rectifier and inverter operations,
4. Hard wired logic circuitry fixes the firing scheme philosophy and any change, if necessary, cannot be included without changing the circuit,

These drawbacks of the analog scheme can be overcome using a a microcomputer based firing angle control scheme for LCI.

The scheme used for generating the firing pulses is

shown in block diagram form in Fig 3.1. It consists of following parts:

1. Three signal transformers, single phase 440/6V, Δ/Y connected,
2. Zero crossing detector circuit,
3. Voltage controlled Oscillator,
4. Timer Card,
5. Pulse amplifier Circuit.

The microcomputer has to execute the following tasks sequentially after every 60° interval:

1. Compute the range of the given firing angle value i.e. 0°-60°, 60°-120°, 120°-180°,
2. Depending upon the range and value of the given firing angle load the delay word into the 8253 counter 0, to generate a delay proportional to the valve of firing angle α,
3. Check the status of three digital signals ϕ_R, ϕ_y, ϕ_B, these signals are in phase with the line voltages V_{RY}, V_{yB}, V_{BR},
4. Depending upon the firing angle α and the status of ϕ_R, ϕ_Y, ϕ_B a firing command word is selected from the firing command table,
5. The two SCRs as selected by high bits of firing command word are fired.

Irrespective of the algorithm used by the micro computer for the

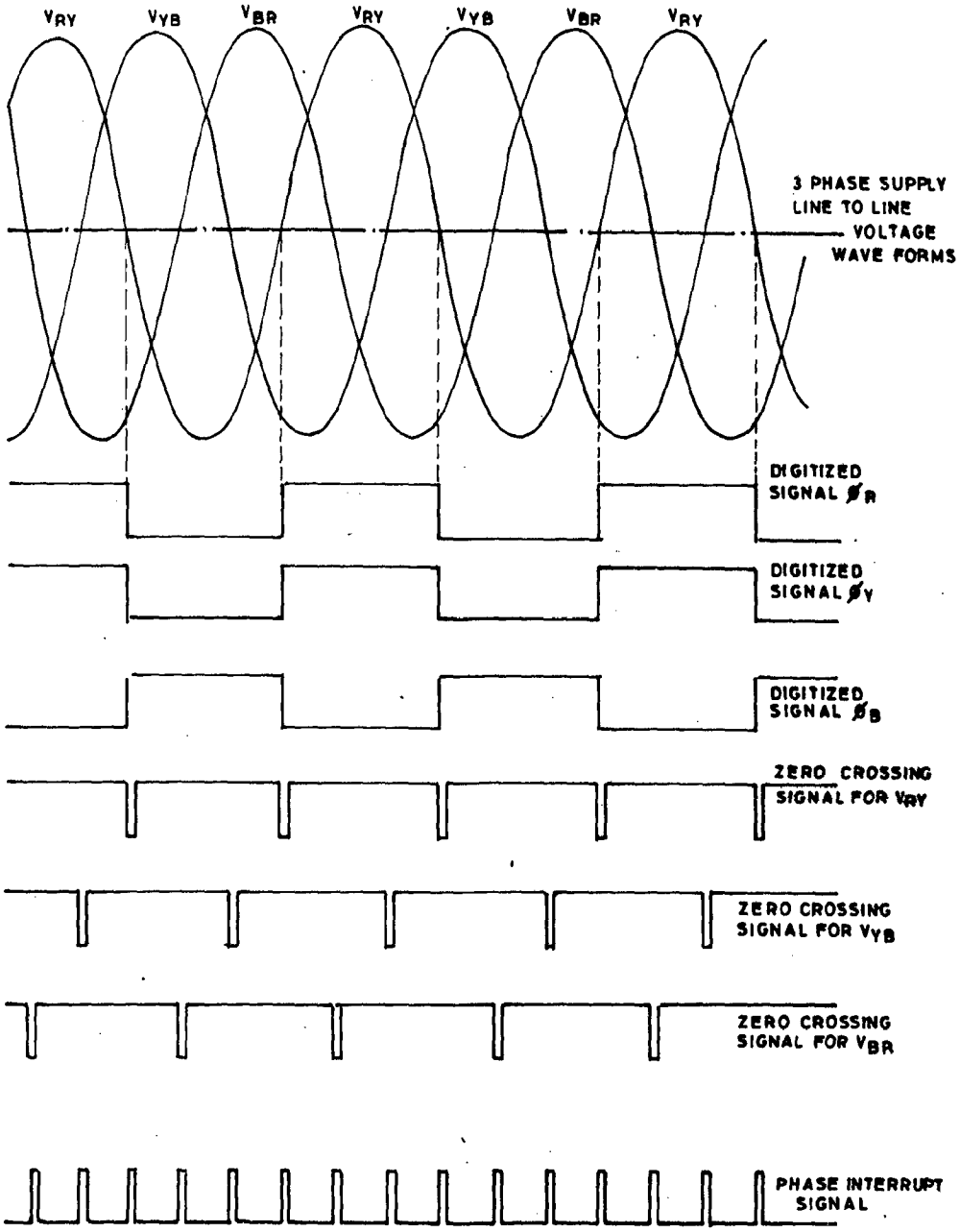


FIG. 3·2. THEORETICAL WAVE FORMS FOR BASE INTERRUPT GENERATION CIRCUIT

(REFER TO FIG. 3·5)

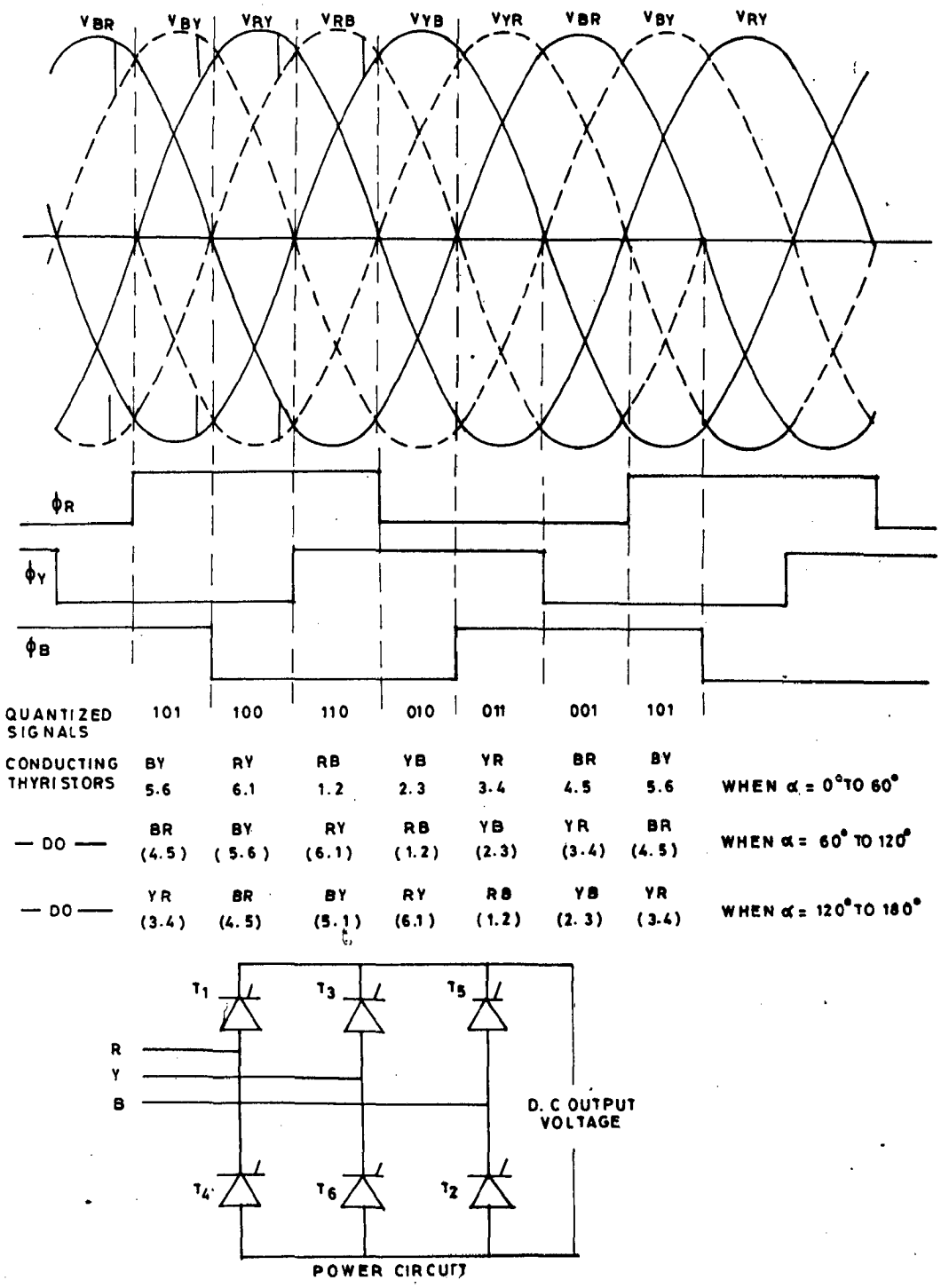


FIG. 3.3 SYNCHRONIZING SIGNALS

control of α, the signals that synchronise with the input supply voltages are very necessary. The six pulse bridge circuit will require six such signals in one cycle. These signals are the zero crossing signals of the line voltages. These are used by the microcomputer to programme a delay proportional to α. The zero crossing circuit derives a train of these pulses as shown in Fig 3.2, these signals are displaced by 60° interval. They are used as base interrupt signals to interrupt the microprocessor after every 60° interval. Three digitalised power signals are also obtained from the zero crossing detector circuit. These signals ϕ_R, ϕ_Y, ϕ_B are in phase with supply line voltages, V_{RY}, V_{YB}, V_{BR}. The status of these signals is inputted by microprocessor in every 60°. These signals have 6 distinct values for each 60° interval. The thyristor pair to be treggered in a particular 60° interval depends upon the status of signals ϕ_R, ϕ_B, ϕ_Y. Hence firing tables as shown in Fig 3.3 giving the status word of the signals in increasing order and the SCR pair to be fired for the given status word for 3 ranges of values of firing angle i.e. α = 0 to 60°, 60° to 120°, 120 to 180° have been prepared i.e. Table 3.1.

The microcomputer uses a programmable interval timer chip 8253 to produce the delay required for given value of α. The PIT 8253 consists of 3 counters (16 bit). These counters when loaded start down counting on negative edge of each clock pulse. There are six modes of operation of 8253 counters, in

all these modes of operation the output of the counters changes status on the terminal count. In the thesis work the counter zero has been used in the mode zero. In this mode - the counter output becomes low as soon as the count is loaded and goes high on terminal count. The down counting is enabled by the high status of gate. The clock pulses to the Timer To are derived from the voltage controlled oscillator.

The high going output of the counter T_0 interrupts microprocessor via RST 5.5. The firing command is outputted via 8255 port pins PA_0 to PA_5. The firing pulse duration is programmed to be 180 μS. These firing pulses are amplified using a pulse amplifier circuit which is same as described in the analog firing circuit scheme.

3.2 ROLE OF VCO IN VARIABLE FREQUENCY MICROCOMPUTER BASED FIRING SCHEME FOR LCI:

The LCI output voltage and frequency can be changed proportionally by,

1. Controlling D.C. link voltage
2. Cos α

The field current has been assumed constant in both the above cases. As explained earlier the firing angle α is fixed by the delay word loaded in counter 0 of 8253. A delay word table giving delay words for different firing angle α, is as given in Table 3.2 is loaded in the memory of the microcomputer from memory address CF00 to CF77. This table is

prepared for a fixed value of operating frequency and voltage and also a fixed value of clock frequency of timer counter T_o.

In case of variable frequency operation of LCI single delay word will not be able to maintain firing angle constant, for a constant frequency of clock.

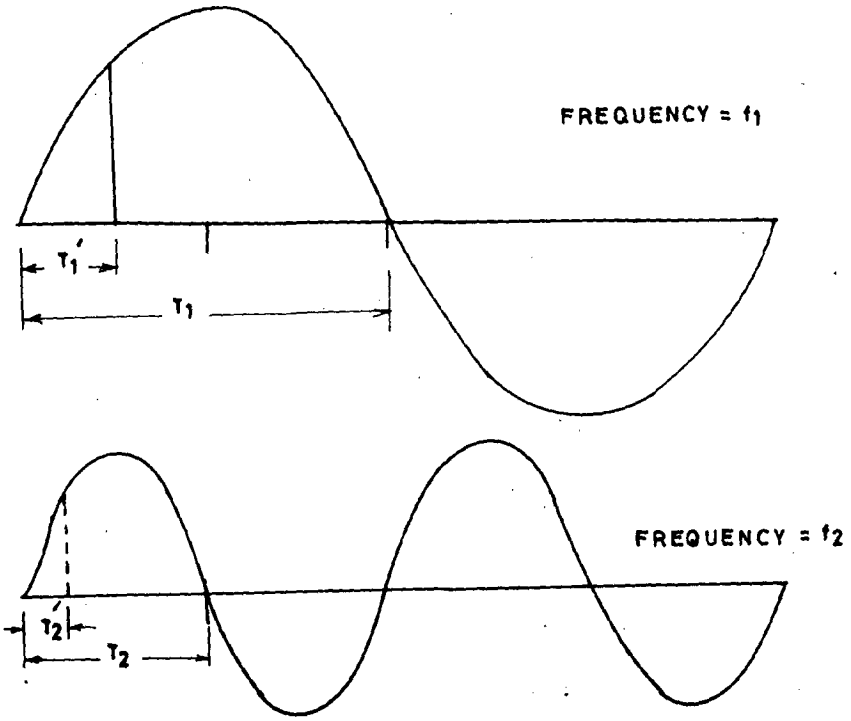
Thus there are two alternatives possible,

(1) Change delay word loaded keeping clock input frequency of 8253 constant,

(2) Change the clock input frequency of 8253 proportionally with the LCI frequency keeping, delay word loaded constant.

The first alternative requires a large no of delay tables, one for each operating frequency of LCI. Thus, this will require a large memory space of microcomputer and also cause a jerky transition from one operating point to other. The disadvantage of excessive memory space required can be overcome by computing the delay word-in each cycle from the operating frequency of LCI. This will again require much CPU time which could be usefully utilized in some other important control action.

In the second method a single delay word table is required. The clock frequency of timer counter is the output frequency of a VCO, which is proportional to the input voltage of VCO. This input voltage if it is derived from the LCI voltage, then LCI voltage changes with LCI frequency which in turn changes the clock input frequency. Thus, a constant



FIRING ANGLE α REMAINS CONSTANT FOR f_1 AND f_2

IF $T_1'/T_1 = T_2'/T_2$

BUT $T_1 = 2T_2$

$\therefore T_1' = 2T_2'$

$\therefore \frac{1}{f_1 V_{co}} = \frac{2 \times 1}{f_2 V_{co}}$ FOR CONSTANT DELAY WORD = N

FIG. 3.4 PRINCIPLE OF FIRING ANGLE CONTROL WITH Vco

firing angle will be obtained at variable frequencies with the help of a single delay word as explained in the Fig 3.4. The basic advantages of this method are,

1. Only one delay word table is required, designed at a particular operating frequency i.e. 50Hz and V/f ratio i.e. 8. The VCO output frequency is 36 K Hz at these operating conditions which is well within the operating frequency range of 8253,

2. The real time of CPU is saved and can be used for other control actions since it is free from the frequency instrumentation problems.

The only disadvantage is that the delay words will have to be modified if the excitation current (i.e. V/f ratio) is changed. This can be easily accomplished through software by sensing the field current and modifying the delay word proportionally. However in the thesis work the synchronous machine is operated in hard saturation region hence change in field current would not cause a considerable error in the set value of α.

It can be shown analytically that value of firing angle remains constant in this method.

The firing angle α will remain constant at two frequencies if the ratio of -T' (i.e. the time delay for α) and T the time period of the LCI voltage remains constant as shown in Fig 3.4.

i.e. α is constant if,

$$\frac{T'}{T} = \text{constant (at } f_1 \text{ and } f_2)$$

or T'/T is frequency independent

f_{VCO} = Output frequency of VCO

V_{IN} = input voltage to VCO.

K_o = transfer function of VCO

= f_{VCO}/V_{IN}.

K_1 = constant of proportionally for V_{LCI} output voltage, and frequency i.e. $K_1 = V_{LCI}/f$.

K_2 = constant of proportionallity for V_{IN} to V_{CO}, and V_{LCI}.

= V_{IN}/V_{LCI}

N = Delay word for timer 8253

If the field current of synchronous motor is kept constant then

$$V_{LCI} = K_1 x f \quad \ldots \quad (3.1)$$

$$V_{IN} = K_2 V_{LCI} \quad \ldots \quad (3.2)$$

Combining equations (3.1) and (3.2) we get

$$V_{IN} = K_1 \times K_2 \times f \quad \ldots \quad (3.3)$$

$$f_{VCO} = K_o \, V_{IN}$$

$$f_{VCO} = K_o \times K_1 \times K_2 \times f \quad \ldots \quad (3.4)$$

Let $K' = K_1 x \, K_o \times K_2$

= constant

$$\therefore \quad T' = N \times \left(\frac{1}{f_{VCO}}\right) \quad \ldots \quad (3.5)$$

TABLE 3.1

FIRING COMMAND DATA

Range of firing angle $\alpha = 0^{\circ}$ to 60°

ϕ_R	ϕ_Y	ϕ_B	I quantizer	Address of firing command	ON SCRS	Firing Command
1	2	3	4	5	6	7
0	0	1	1	D000+01	4,5	00011000 (PA7-PA0) i.e.18H.
0	1	0	2	D000+02	2,3	00000110 i.e. 06H
0	1	1	3	D000+03	3,4	00001100 i.e. 0CH
1	0	0	4	D000+04	6,1	00100001 i.e. 21H
1	0	1	5	D000+05	5,6	00110000 i.e. 30H
1	1	0	6	D000+06	1,2	00000011 i.e. 03H

Range of firing angle $\alpha = 60^{\circ}$ to 120°

1	2	3	4	5	6	7
0	0	1	1	D000+07	3,4	0C H
0	1	0	2	D000+08	1,2	03 H
0	1	1	3	D000+09	2,3	06 H
1	0	0	4	D000+0A	5,6	30 H
1	0	1	5	D000+0B	4,5	18 H
1	1	0	6	D000+0C	6,1	21 H

Range of firing angle $\alpha = 120^{\circ}$ to 180°

1	2	3	4	5	6	7
0	0	1	1	D000+0D	2,3	06 H
0	1	0	2	D000+0E	6,1	21 H
0	1	1	3	D000+0F	1,2	03 H
1	0	0	4	D000+10	4,5	18 H
1	0	1	5	D000+11	3,4	0C H
1	1	0	6	D000+12	5,6	30 H

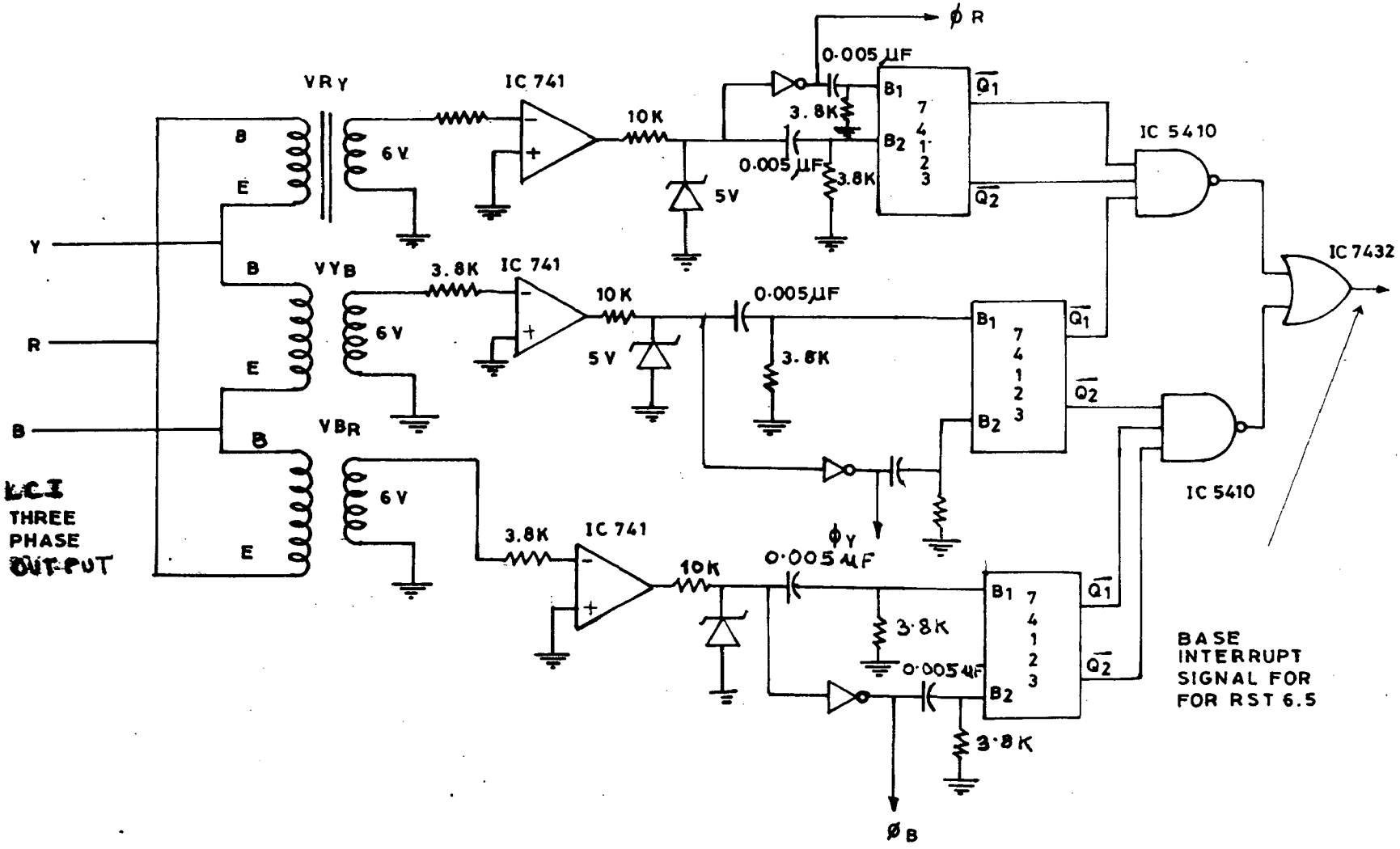


FIG. 3.5 BLOCK DIAGRAM OF ZERO CROSSING CIRCUIT

$$T = \frac{1}{f} \qquad \ldots \qquad (3.6)$$

$$\frac{T'}{T} = \frac{N(\frac{1}{K'f})}{1/f} = \frac{N}{K'} \qquad \ldots \qquad (3.7)$$

From the equation 3.7, it is clear that ratio of T' and T is only dependent on N i.e. delay word and is totally independent of frequency for constant value of field current of SM. The relation of output frequency versus input voltage of the LM 331. VCO is as given in Fig 3.7. It is clear that a linear relation exists between f_{VCO} and voltage input to VCO.

3.3 DESIGN OF ZERO CROSSING DETECTOR CIRCUIT:

The six synchronising signals required by the microprocessor for controlling the firing angle of a three phase bridge are generated by this circuit. The synchronising signals are nothing but the zero crossing points of the six line voltages. The zero crossing points are detected by the comparator as given in the Fig 3.5.

A monoshot is triggered at each zero crossing point. The output pulse width of monoshot should be have a pulse width of at least 20 μs in order to effectively interrupt the microprocessor via R_{ST} 6.5 interrupt. A pulse train of these synchronising signals displaced at 60^{o} is obtained by logically combining the outputs of all the monoshots.

The block diagram of the zero crossing circuit is as given in Fig 3.5.

The zerocrossing detector consists of the following:

1. Signal transformers,
2. Comparators,
3. Differentiator,
4. Monoshots,
5. Logic NAND and OR gates.

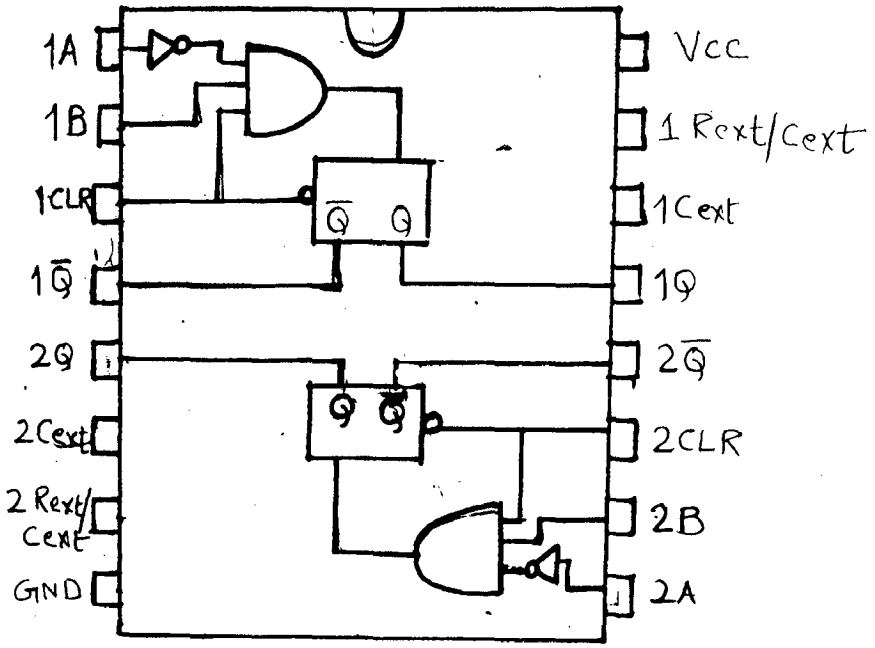
3.3.1 SIGNAL TRANSFORMERS:

The stepped down line voltages of LCI are obtained from these transformers. Three single phase transformers of 440/6V, have been used. The primary windings of these transformers are connected in delta. The advantage of this connection is that the secondary output voltages will be in phase with the LCI line voltages; This enables the derivation of synchronising signals from line voltage zero crossing points.

3.3.2 COMPARATOR:

The IC 741 is used as a comparator to compare the A.C. line voltage signals with 0V. The output signal of the comparator is a square wave. These signals are in phase with the line voltages. The signals are reduced to digital TTL level with the help of 5V zener diodes. The digital square wave outputs of 3 comparators which are in phase with V_{RY}, V_{YB}, V_{BR}, are sensed by microprocessor to determine the pair of SCR to be turned on for the particular 60^{o} interval. The selection of SCR pair based on status of ϕ_R, ϕ_Y, ϕ_B signals has already been explained.

(a) INTERNAL BLOCK DIAGRAM 74123



FUNCTIONAL TABLE TABLE 3.6(a)

SNO	CLR	A	B	Q	Q̄
1	L	X	X	L	H
2	X	H	X	L	H
3	X	X	L	L	H
4	H	L	↑	⊓	⊔
5	H	↓	H	⊓	⊔
6	↑	L	H	⊓	⊔

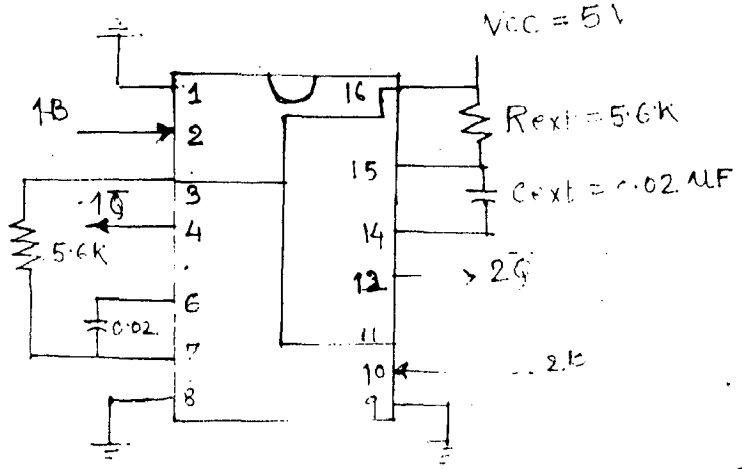


FIG. 3.6(b) CIRCUIT DIAGRAM OF MONOSHOT 74123

3.3.3 INVERTER:

In order to obtain 6 signals from the 3 digital power signals ϕ_R, ϕ_Y, ϕ_B, these signals are inverted using 7404 hex inverter to get $\bar{\phi}_R$, $\bar{\phi}_Y$, $\bar{\phi}_B$. The rising edge of these 6 signals are used to trigger 6 monoshots. The rising edges are obtained by differentiating the square wave signals with a RC differentiator with a very small time constant RC = 10 μS.

3.3.4 MONOSHOT:

The six monoshots have been obtained by using 74123 IC in positive edge triggered mode. The functional table, Internal block diagram of the chip with pin assignment and circuit diagram, all are shown in Fig.3.6. The output pulse width of monoshot is desided by the external timing capacitor and Resistance and is given by,

$$t_w = 0.45\ R_{ext}\ C_{ext}$$

where

R_{ext} = in K

C_{ext} = in picofarads

t_w = in nano seconds

The designed value of R_{ext} and C_{ext} are

R = 5.64 K , C = 0.002 μF

giving t_w = 50.4 micro seconds

A pulse train of all the synchronising signals spaced at 60° is obtained as shown in Fig 3.3 by logically combining them with the help of digital logic gates. The pulse train forms

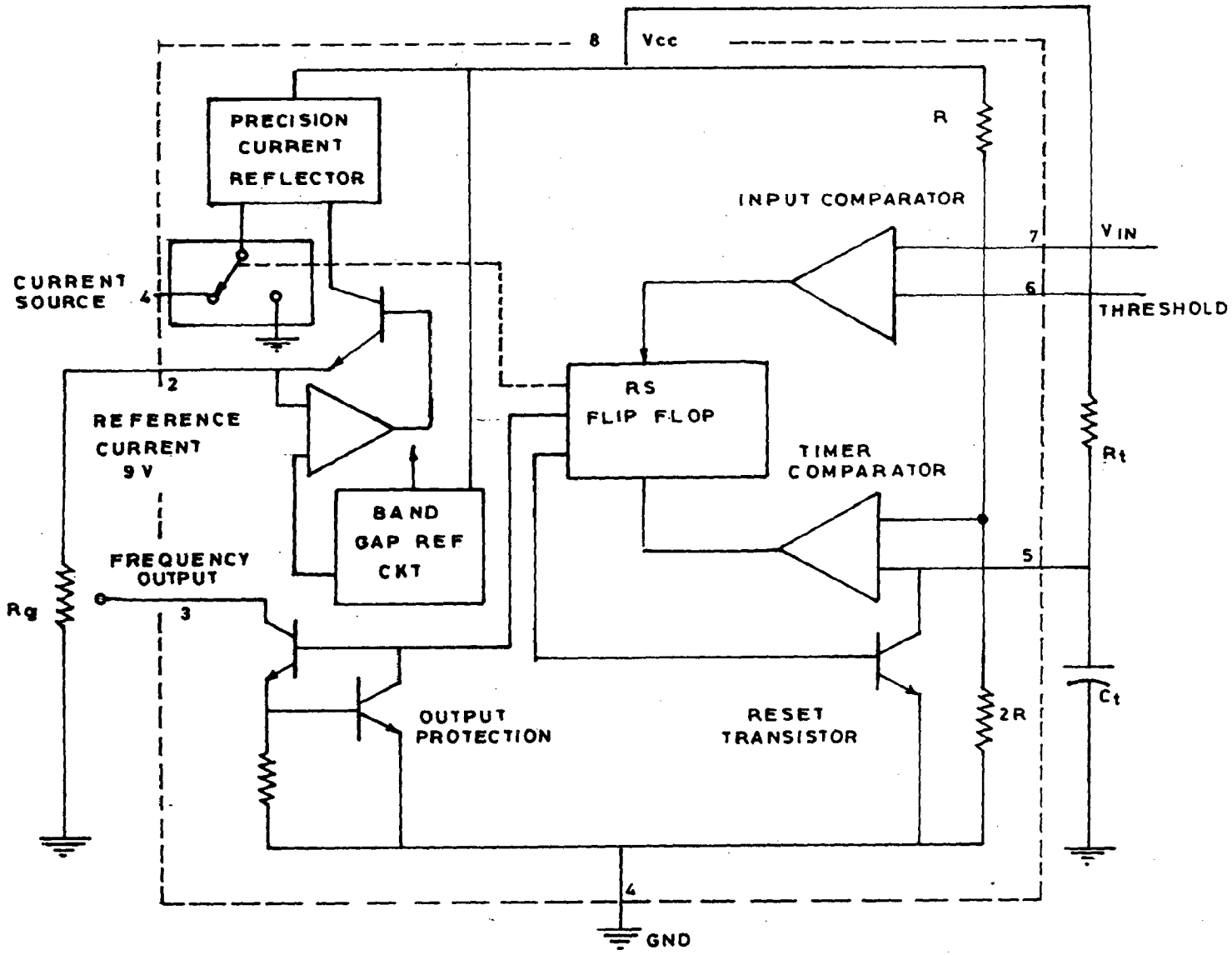


FIG. 3.8. BLOCK DIAGRAM OF VCO→LM 331

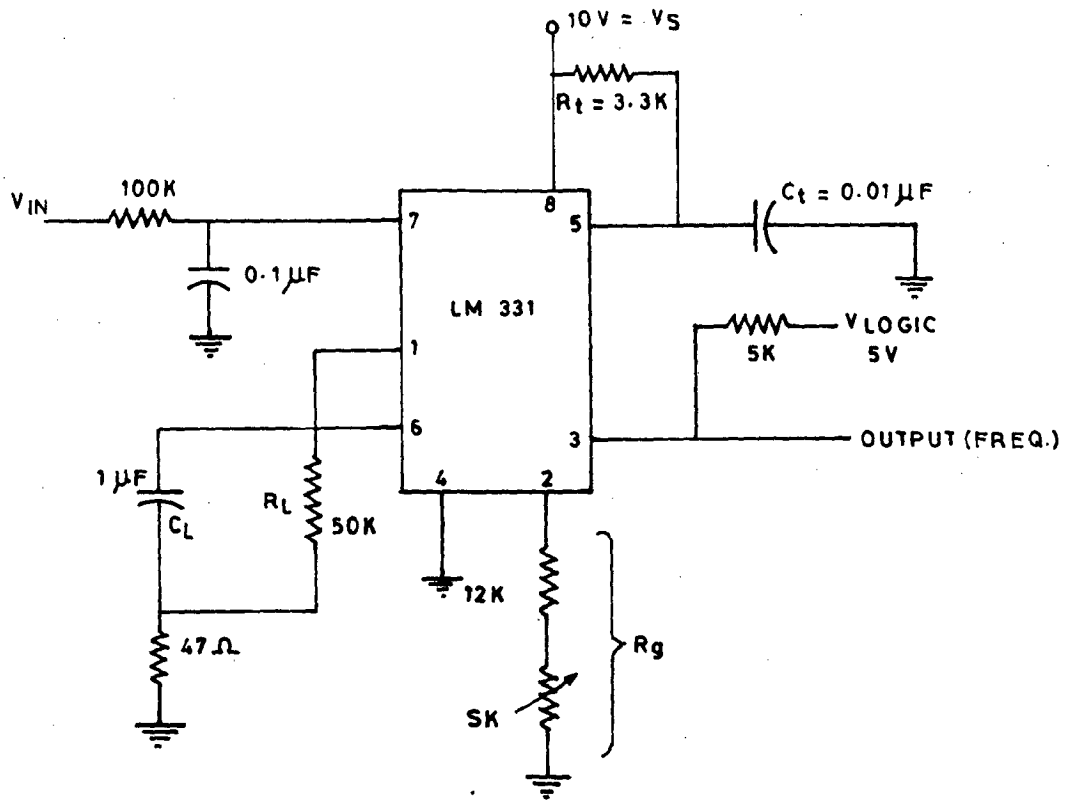


FIG. 3.8 CIRCUIT DIAGRAM OF Vco

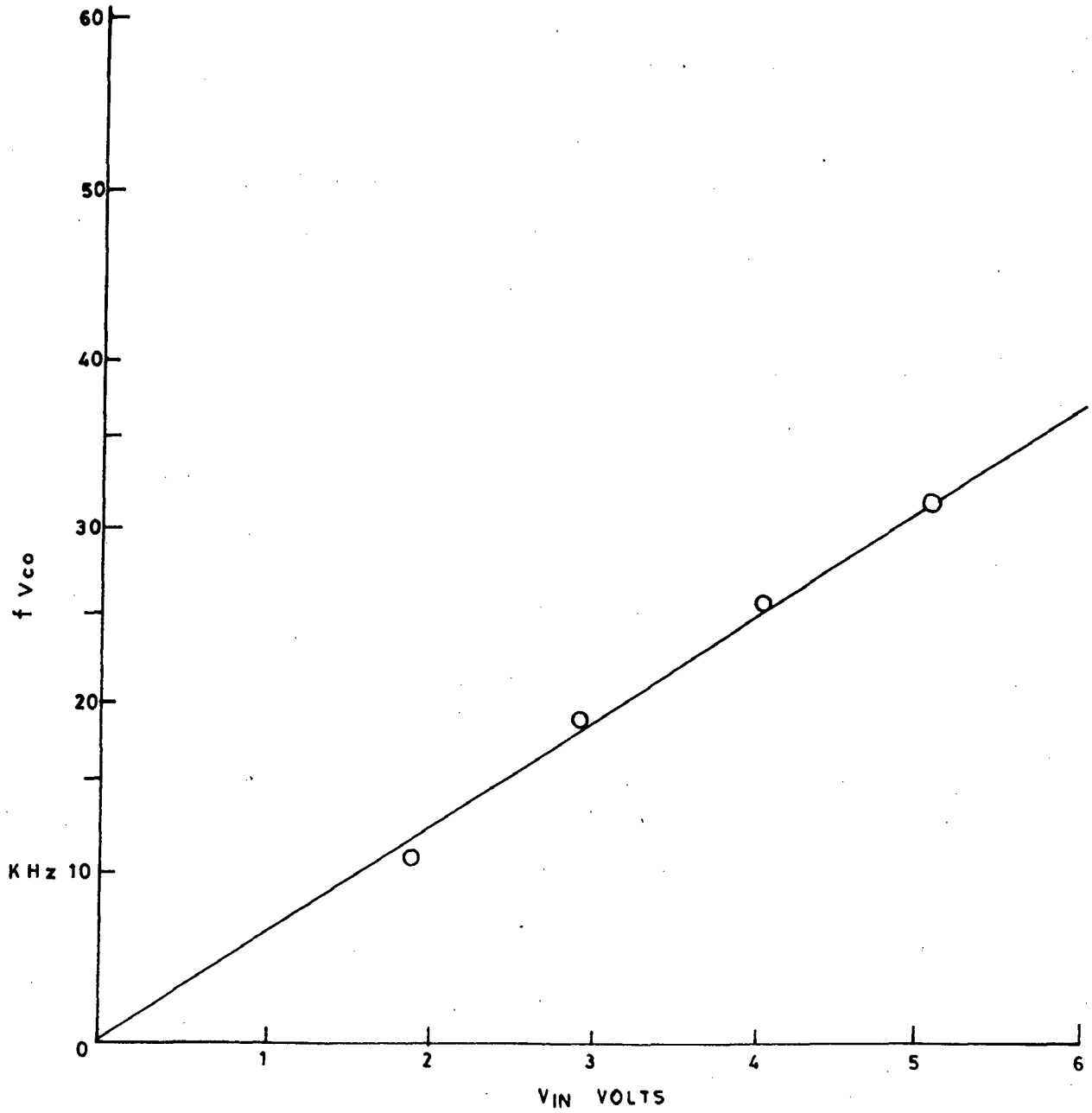


FIG. 3.9 RELATION BETWEEN FREQUENCY OUTPUT OF Vco AND INPUT VOLTAGE

the base interrupt signals for RST 6.5 interrupt.

3.4 VOLTAGE CONTROLLED OSCILLATOR:

The VCO is designed using IC LM 331 from National Semiconductors. It is a precision voltage to frequency converter. The pin out diagram of this 8 pin DIP IC and it's internal functional block diagram is as shown in Fig 3.7. The circuit diagram of voltage to frequency converter is as given in Fig 3.8.

The frequency output of VCO is given by the relation

$$f_{out} = \frac{V_{IN}}{2.00} \times \frac{R_g}{(R_L \times R_t).C_t}$$

where R_g, R_L, R_t, C_t are the symbolic names of the components as given in Fig 3.8. The VCO LM 331 operates from a single 5V power supply. The full scale frequency range of output is 1 KHz to 100 KHz.

It is clear from the block diagram that the VCO consists of a switched current source, input comparator, and a 1 shot timer. The comparator compares a positive input voltage V_{IN} at the pin 7 with the voltage V_x accross the capacitor at pin 6. If V_{IN} is greater then the comparator triggers the one shot timer.The output of the one shot timer will turn on both the frequency output transistor as well as the switched current source for a time period of $t = 1.1R_tC_t$ i.e. up to the time when the voltage at pin 5 rises to 2/3 V_{CC} then the timer comparator causes the R-S flip flop

to reset. This causes the reset transistor to turn on and the current source is switched off.

As the current source is switched off therefore the capacitor C_L now discharges through R_L until the voltage V_X at pin 6 fall below V_{IN}. Then the comparator will again trigger on the 1 Shot timer and another cycle of operation begins.

The current flowing into C_L is $I_{av} = i \times (1.1 R_t C_t) f$ and the current flowing out of C_L is $V_X/R_L \approx V_{IN}/R_L$

$\therefore I_{av} = V_{IN}/R_L$ thus if the input voltage is doubled then the frequency has to double to maintain the charge balance.

A characteristics feature of this chip is the current pump circuit which forces the voltage at pin 2 to be at 1.9V and causes a current $i = 1.9/R_g$ to flow out of pin 2. The precision current reflector provides a current equal to i (i.e. it reflects the current at pin 2 into the current source) to the current source. Thus the charging current is controlled by R_g.

The designed values of various components to obtain a frequency output of 36 KHz for V_{IN} of 6 Volts are as given

R_t = 3.3 K $\qquad$ R_L = 50 K

C_t = 0.01 μF $\qquad$ C_L = 1 μF

R_g = 12 K + 5 K (Variable).

TABLE 3.2

Table fo firing angle α and delay words for counter T_o of 8253.

V_{LCI} = 400V, f = 50 Hz, f_{clock} = f_{VCO} = 36 KHz.

S.NO.	MEMORY ADDRESS	DELAY COUNT	S. NO	MEMORY ADDRESS	DELAY COUNT	S. NO.	MEMORY ADDRESS	DELAY COUNT
1	CF00	00	35	CF22	22	70	CF45	00
2	CF01	00	36	CF23	00	71	CF46	46
3	CF02	02	37	CF24	24	72	CF47	00
4	CF03	00	38	CF25	00	73	CF48	48
5	CF04	04	39	CF26	26	74	CF49	00
6	CF05	00	40	CF27	00	75	CF4A	4A
7	CF06	06	41	CF28	28	76	CF4B	00
8	CF07	00	42	CF29	00	77	CF4C	4C
9	CF08	08	43	CF2A	2A	78	CF4D	00
10	CF09	00	44	CF2B	00	79	CF4E	4E
11	CF0A	0A	45	CF2C	2C	80	CF4F	00
12	CF0B	00	46	CF2D	00	81	CF50	50
13	CF0C	0C	47	CF2E	2E	82	CF51	00
14	CF0D	00	48	CF2F	00	83	CF52	52
15	CF0E	0E	49	CF30	30	84	CF53	00
16	CF0F	00	50	CF31	00	85	CF54	54
17	CF10	10	51	CF32	32	86	CF55	00
18	CF11	00	52	CF33	00	87	CF56	56
19	CF12	12	53	CF34	34	88	CF57	00
20	CF13	00	54	CF35	C0	89	CF58	58
21	CF14	14	55	CF36	36	90	CF59	00
22	CF15	00	56	CF37	00	91	CF5A	5A
23	CF16	16	57	CF38	38	92	CF5B	00
24	CF17	00	58	CF39	00	93	CF5C	5C
25	CF18	18	59	CF3A	3A	94	CF5D	00
26	CF19	00	60	CF3B	00	95	CF5E	5E
27	CF1A	1A	61	CF3C	3C	96	CF5F	00
28	CF1B	00	62	CF3D	00	97	CF60	60
29	CF1C	1C	63	CF3E	3E	98	CF61	00
30	CF1D	00	64	CF3F	00	99	CF62	62
31	CF1E	1E	65	CF40	40	100	CF63	00
32	CF1F	00	66	CF41	00	101	CF64	64
33	CF20	20	67	CF42	42	102	CF65	00
34	CF21	00	68	CF43	00	103	CF66	66

TABLE 3.2 (CONTD.)

S.NO.	MEMORY ADDRESS	DELAY COUNT	S.NO.	MEMORY ADDRESS	DELAY COUNT
105	CF68	68	113	CF70	70
106	CF69	00	114	CF71	00
107	CF6A	6A	115	CF72	72
108	CF6B	00	116	CF73	00
109	CF6C	6C	117	CF74	74
110	CF6D	00	118	CF75	00
111	CF6E	6E	119	CF76	76
112	CF6F	00	120	CF77	00

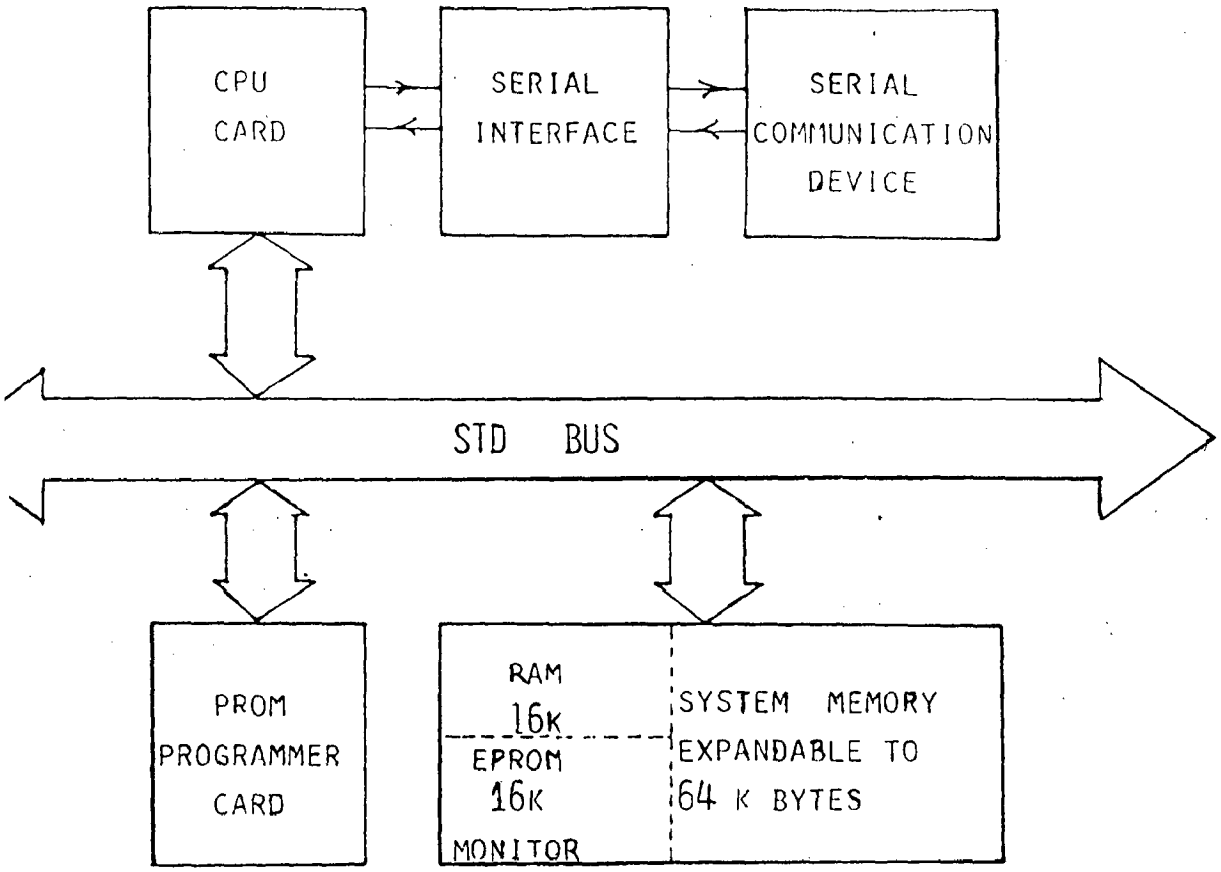


FIG 3.10 BLOCK DIAGRAM OF VMDS - 85

3.5 DESCRIPTION OF MICROPROCESSOR DEVELOPMENT SYSTEM (VMDS-85):

The digital control scheme for the LCI firing angle has been developed using the Vinytics Microprocessor Development System -VMDS-85. This system is based on Intel's most popular microprocessor, the 8085. It is available in a 19" card cage having the facility of interfacing a number of STD Bus based cards. The three basic cards on which the VMD5-85 system is based are:

1. CPU card
2. RAM card
3. EPROM card

The system can be easily expanded to accommodate some special purpose STD Bus based cards, e.g. Input-output and Timer Card.

3.5.1 SYSTEM CONFIGURATION:

The block diagram of the system is as given in Fig.3.10. The VMDS-85 system can be interfaced to the CRT via 20mA or RS-232-C interface. The TTY can be interfaced to the system via 20 mA loop. The total memory area in the system can be expanded up to 64K. An EPROM programming module can be connected to the system with the help of an I/O Timer card. The address, data and control signals of the STD bus are TTL compatiable and have been brought out to the edge connector at STD Bus.

A brief description of the individual cards used in VMDS-85 is given below:

3.5.2 CPU CARD (VCP-85):

The CPU card is a micro-computer card based on Intel 8085 microprocessor. The card is configured around the internationally accepted STD Bus. This card provides the following facilities:

1. 4K byte of CMOS RAM using two 6116.
2. 4K/8K bytes of EPROM using two 2716/2732 EPROMs, through Jumper selection,
3. 24 programmable input output lines using 8255,
4. Buffered data, address and control lines, available at STD Bus.

The memory map for VCP-85 is given as

S.No	Addresses	RAM/ROM	Remarks
1	0000-0FFF	EPROM	-
2	1000-EFFF	RAM/ROM	Area for expansion
3	F000-FFFF	RAM	-

In case 2732 ICs are used, the addresses for EPROMs will be 0000-1FFF and then the expansion area will be from 2000-EFFF. For further memory expansion the 16K CMOS RAM/ROM Card has been provided.

The programmable input output ports in the card are I/O mapped.

All the interrupts have been pulled down using 5.6 K resistance. TRAP and INTR are buffered and brought out on the

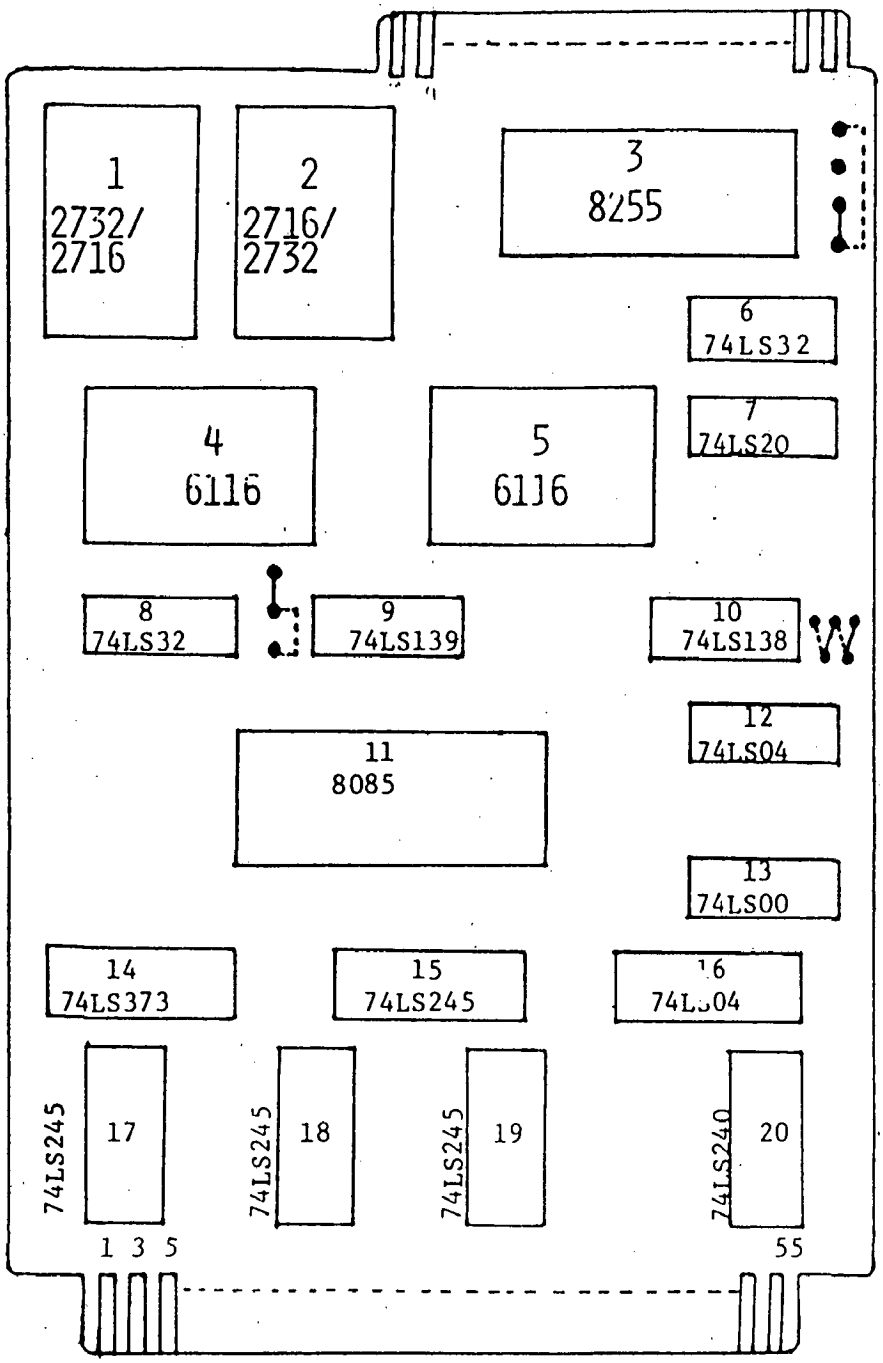


FIG. 3.11 LAYOUT OF THE VCP-85 CARD

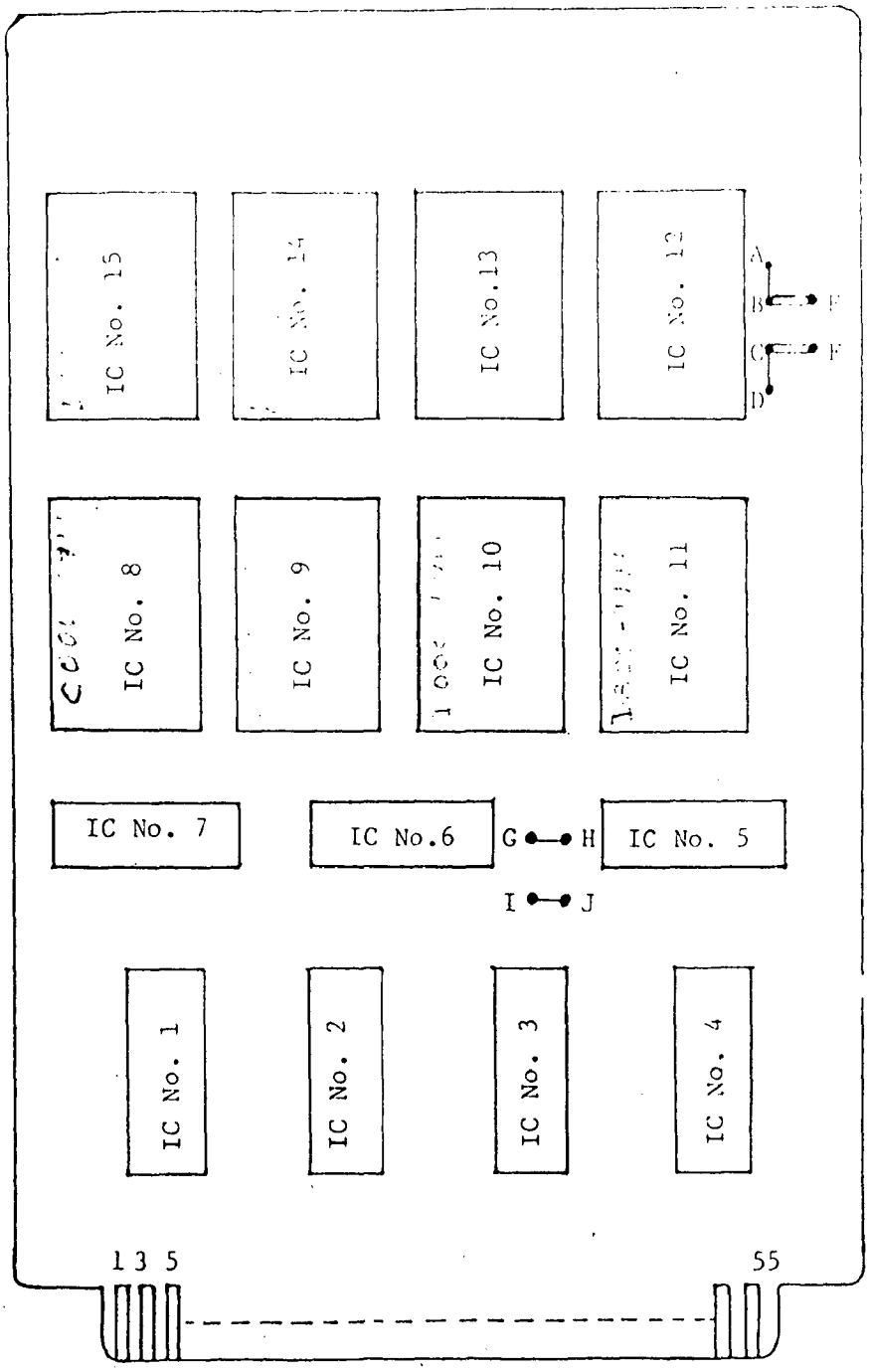


FIG. 3.12 LAYOUT OF VMR-85 CARD

STD bus where as RST 7.5, 6.5, 5.5 interrupts are brought out on the 44 pin edge connector. The Appendix gives the pin assignment of 44 pin edge connector.

The component layout of VCP-85 card is as given in Fig.3.11.

3.5.3 MEMORY CARD (VMR-85)

The VMR-85 is an STD bus based card. The component layout of this card is as given in Fig.3.12. This card can be configured in three ways as (i) 16 K bytes EPROM Card, (ii) 8 K byte EPROM with 8K bytes RAM Card; (iii) 16 K byte RAM card by suitably selecting the jumper connections.

Thus, this card can be utilised for secondary storage in an 8 bit system where memory to be used is more than 64 K byte.

3.6 SYSTEM SOFTWARE

The communication with the CRT is made through SID and SOD lines. As mentioned earlier an RS-232-C and 20 mA current loop interface is provided on the memory card. The CRT terminal or Tele-typewriter is to be connected in Asynchronous ASCII, one start bit, two stop bits and parity off format.

The system can communicate with the CRT at a baud rate of 75 to 9600 bauds. The system on resetting displays a sign-on message AM02 with a promt sign. On the starting of the

TABLE 3.4

REAR CONNECTOR DETAILS

1	-	GND	33	-	PAII4
2	-	GND	34	-	PAII5
3	-	VCC	35	-	PAII6
4	-	VCC	36	-	PAII7
5	-	PAI0	37	-	PBII0
6	-	PAI1	38	-	PBII1
7	-	PAI2	39	-	PBII2
8	-	PAI3	40	-	PBII3
9	-	PAI4	41	-	PBII4
10	-	PAI5	42	-	PBII5
11	-	PAI6	43	-	PBII6
12	-	PAI7	44	-	PBII7
13	-	PBI0	45	-	PCII0
14	-	PBI1	46	-	PCII1
15	-	PBI2	47	-	PCII2
16	-	PBI3	48	-	PCII3
17	-	PBI4	49	-	PCII4
18	-	PBI5	50	-	PCII5
19	-	PBI6	51	-	PCII6
20	-	PBI7	52	-	PCII7
21	-	PCI0	53	-	CLK0
22	-	PCI1	54	-	OUT0
23	-	PCI2	55	-	GATE0
24	-	PCI3	56	-	CLK1
25	-	PCI4	57	-	OUT1
26	-	PCI5	58	-	GATE1
27	-	PCI6	59	-	CLK2
28	-	PCI7	60	-	OUT2
29	-	PAII0	61	-	GATE2
30	-	PAII1	62	-	
31	-	PAII2	63	-	
32	-	PAII3	64	-	

next line. Thus signifies that system is waiting for valid command to be inputted.

The command recogniser compares the command alphabets with a stored table..The comparison continues till a match is found or FF is encountered. If match is not encountered and FF is found then the system displays an error by giving : on the terminal and a .. On a next line to wait for a valid command. Thus the recogniser is not limited by any number, but by the memory area left for the command. Each command requires five memory locations out of which two are required for the command name and three locations for jump to service routines instruction. The command table is allotted RAM area from 8600 to 8FFF, such that about 100 commands can be incorporated in the system. Each command consists of two alphabets. The command recogniser takes in last two alphabets before carriage return. This allows the user to correct any error made in entry.

The total no of commands of AM02 is 69. A MENU command has been developed to display the command groups and the commands in a particular command through the MENU.

The resident system firmware is divided into seven groups, listed below:

1. Monitor
2. Relocate object program,
3. Documentation,

4. PROM,
5. Assembler,
6. Auxiliary storage,
7. Miscellaneous.

The capabilities of individual groups are briefly given below.

1. The monitor group can input/ modify a program or data, introduce a break point; restore a break point Execute a program/subroutine with a symbolic name or address; memory compare; Fill and block move the memory; Tape read/write etc.

2. The relocate group can modify code/address with or without print out; Relocate and link the program; Relocate multiprogram; Reverse relocate; insert and delete with relocation etc.

3. In documentation group the program can be documented by taking a listing of ASCII/Hex data, or by listing the program in assembly language on VDU/TTY with or without comments.

4. The assembler group allows the entry of a program in assembly language. It allows relocation of programs with or with-out labels. Labels can be entered, modified, removed and listed independent of program entry.

5. Pseudo commands like Data ASCII, Data Byte, Data word Data storage, End of Assembly, End intermediate,

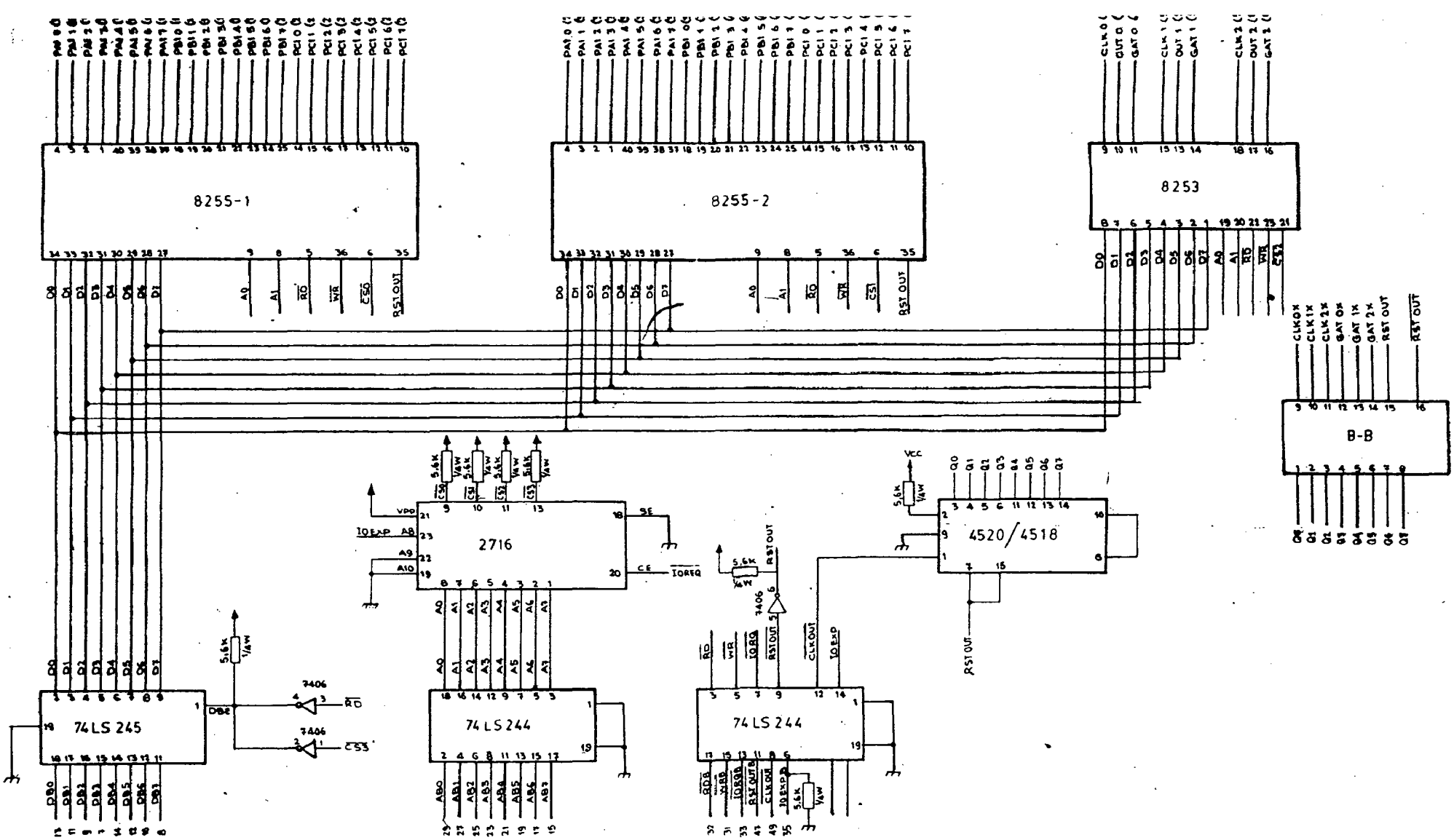


FIG 3.13 CIRCUIT DIAGRAM FOR TIMER & I/O CARD

: Go back in program to cancel N number of instructions, help in the entry of an assembly language program.

6. The optional PROM programmer group can program most popular NMOS (except 2708, 1702) EPROM, list its data, verify blank check, etc.

7. The MENU helps the user in selecting a particular group and then enter a specific command within the group.

3.7 I/O AND TIMER CARD:

A role of prime importance is played by the Digital I/O and timer card in any process control application using the microcomputer. This card is based on programmable peripheral interface, the 8255 and programmable timer/counter, the 8253. The main features of the card are;

1. Six programmable input/output ports through two 8255,
2. Three sixteen bit timer/counter implemented through 8253,
3. Input/output mapped,
4. Programmed address decoding through EPROM 2716,
5. Single + 5V power supply,
6. Based on STD bus.

3.7.1 CIRCUIT DESCRIPTION:

The circuit diagram of the timer card is as given in Fig.3.13. The data bus has been buffered with a bidirectional bus buffer, the 74LS245. The direction control signal is used

to read/write the input output digital signals through 8255. The 74LS244 is used as buffer for address and control signals.

All the desired address, data and control signals are connected to two 8255. The chip selection for 8255-1, 8255-2, 8255 and card select signals are generated through EPROM decoding techniques.

The clock(CLK), gate(GATE) and output(OUT) signals of the three timers of 8253 are brought out on the back connector. The clock inputs can be connected to any of the internal clocks or any external clocks. The gate of 8253's timers can be made high by connecting them to the RST OUT, which goes low only during resetting. The internal selection of gate and clock are through the connection adaptor. The details of the connection adaptor are as given in the Table no 3.5.

The card is input/output mapped and can be selected by any port address defined from 00-FF. This is achieved by EPROM decoding technique. The port address lines A_0 to A_7 are connected to EPROM 2716 and the output lines 00, 01, 02, and 03 are connected with a proper circuit to 8255-1, 8255-2, 8253 and card select line. In order to select any I/O device the particular output line should be low along with the card select line i.e.(03) at the desired port address location. The table in 3.3 shows the code number to select the desired input output device.

TABLE 3.3

DETAILS OF PORT ADDRESS OF I/O AND TIMER CARD

8255-1	$\overline{CS0}$	at	50	Port A
			51	Port B
			52	Port C
			53	Control word.
8255-2	CS1		54	Port A
			55	Port B
			56	Port C
			57	Control word.
8253	$\overline{CS2}$		58	Counter 0
			59	Counter 1
			5A	Counter 2
			5B	Command word.

TABLE 3.5

DETAILS OF CONNECTION ADAPTOR OF I/O AND TIMER CARD

1. Q_o = (Microprocessor clock/2)
2. $Q_1 = Q_o/2$
3. $Q_2 = Q_1/2$
4. $Q_3 = Q_2/2$
5. $Q_4 = Q_3/2$
6. $Q_5 = Q_4/2$
7. $Q_6 = Q_5/2$
8. $Q_7 = Q_6/2$
9. CLOCK 0
10. CLOCK 1
11. CLOCK 2
12. GATE 0
13. GATE 1
14. GATE 2
15. RESET OUT
16. RESET OUT

At the device port address, the code for the device to be selected is programmed. Each device requires four port addresses. The table 3.3 gives the port address for the individual ports of all the devices. The details of the timer card 64 pin rear connector are as given in table 3.4.

3.8 DATA TERMINAL(VDT-85):

The VDT-85 is an interactive terminal designed with a full 12" diagonal non glare CRT screen having a capability of displaying full 24 lines of 80 characters. The characters are formulated using a TV raster scan technique with 5x7 dot matrix character window to provide a crisp and clear display VDT-85 provides a detachable keyboard which transmits ASCII standard code on a serial link. The keyboard uses mechanical switches under software control to provide user's definable codes. It has numeric key pad, edit key pad, function keypad cursor control keypad etc. The effective keyboard design provides a three wire communication between the keyboard and the display unit.

The terminal interacts with computer systems through EIA-RS-232C or 20mA current loop interface at band rates that are programmable. The band rate, bit structure, half/full duplex, parity etc. are selectable by the keyboard. The top line(25th) displays the mode of the terminal. The ESC commands provides efficient management and editing such as cursor address, insert/delete character or line, mode of transmission to character/line/page, intensity control etc.

The optional parallel printer port and Aux RS-232-C port facilitates the interfacing of hard copy printers, magnetic storage devices or chaining of terminals.

3.9 ESCAPE SEQUENCE:

VDT-85 provides escape sequence for full cursor control and editing. This allows it to be used with word processing and editing systems which requires an ANSI standard terminal. The functions provided by escape sequences. can be invoked in the off line mode from keyboard or in the on line mode from keyboard or in on line mode from the host computer connected to LINE port.

The escape commands are given in the following format .

ESC PARAMETERS COMMAND CHARACTER 1B (Single ASCII CH)

The parameters have a general format as given below,

P_1; P_2; P_3; ....; P_n

These parameters are optional. Defaults values are assumed if some of them are not specified. The number of parameters is dependent upon the type of command. ASCII ; separates two parameters. Start of parameter field is indicated by a [and P_1; P_2; P_3;....; P_n are sequences of ASCII encoded BCD digits.

The monitor program uses Editing functions type of

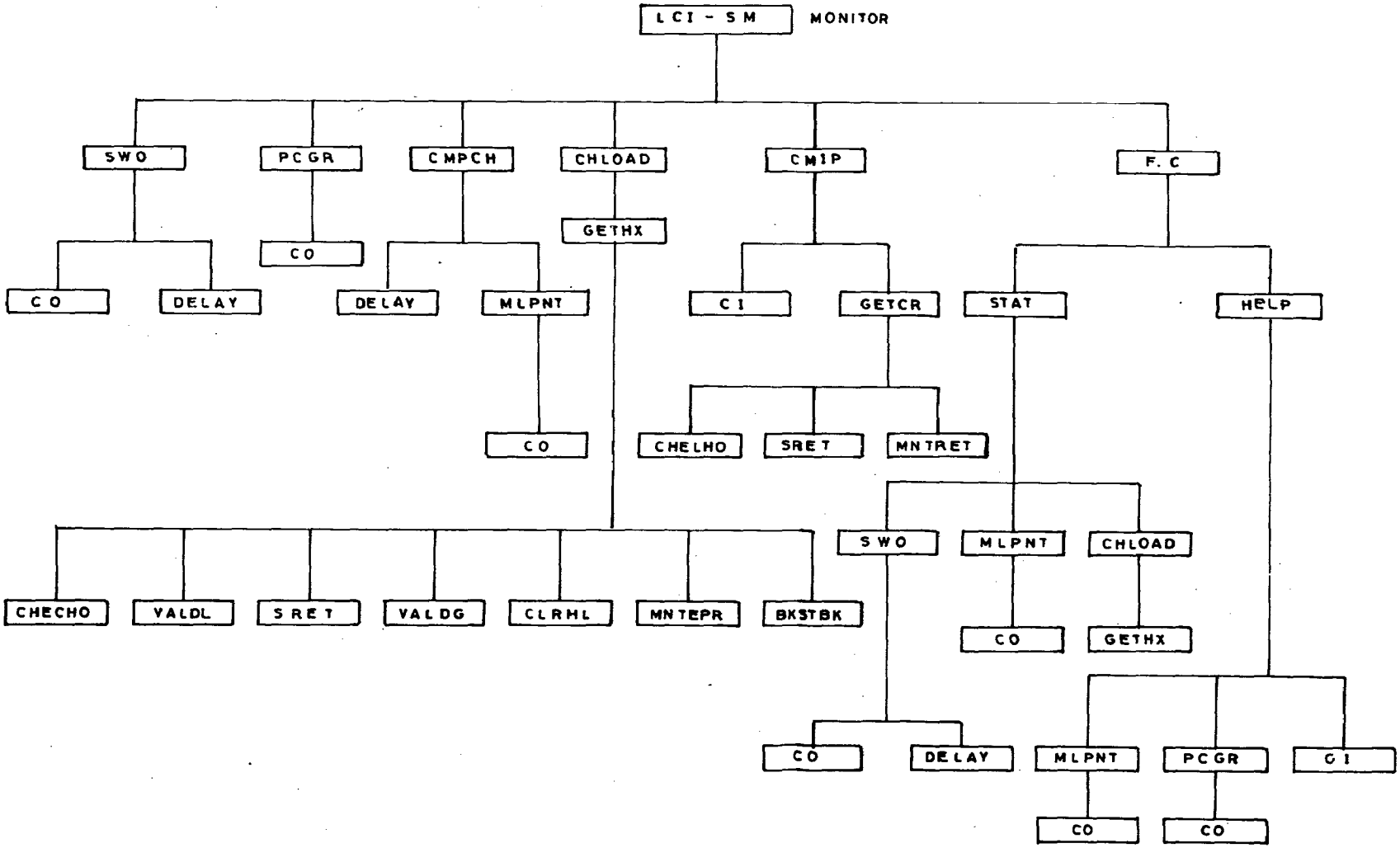


FIG. 3.14 LCISM MONITOR SOFTWARE TREE

one escape command as discussed in the fundtional command development section, to erase the entire screen. The format of the command is as

ESC [2 J

The LCI-SM monitor program outputs the ASCII codes of all the above command characters to the CRT, in a sequence. This clears the entire screen and cursor returns to the home position.

3.10 FUNCTIONAL COMMAND DEVELOPMENT:

The communication of microcomputer with the operator is kept via the CRT(VDT-85). Hence it was thought necessary to develop a dedicated monitor program assisting the operator in his communication with the microcomputer. A monitor program which will be further called asLCI-SM has been developed. The LCI-SM Monitor software tree is as shown in Fig 3.10. The monitor program takes four charactered commands from the operator via the CRT. If the command is found valid the functional command routine is executed or else the monitor program flashes an error message on the terminal requesting the user to call HELP command and then waits for another command.

In the present work, two functional commands have been developed. The design of software is such that the functional command should be a four lettered command. A functional command table containing the list of all valid commands has been developed in the RAM memory area. The table

starts from the memory having address D530 and extends upto D54B memory location. Each command occupies 7 byte memory locations. The four memory locations contain the command character ASCII codes for each command, and the remaining three locations have a jump instruction to the starting address of the command routine. Thus four commands can be developed in the specified memory area reserved for the command table.

The two commands that have been developed are:

(1) STAR,

(2) HELP.

A number of subroutines have also been developed and these are frequently called by the functional commands or the LCI-SM monitor. Some of the standard routines available in VMDS-85 system monitor such as character in, character out, generation of delay etc. are also used in the software development. A brief description of these routines is also given at a later stage.

3.11 LCI-SM MONITOR ROUTINES

1. FUNCTION : SWO

   INPUTS : Memory locations, D54B-D54F,

   OUTPUTS : None

   CALIS : CO

   DESTROYS : H,L,B,C,A,

   CALLINGADDRESS : C095.

DESCRIPTION : This routine wipes out the entire screen and the cursor returns to the home position on the screen The use of

escape command sequence as explained earlier has been made in this routine.

2. FUNCTION : PCGR
   INPUTS : NONE
   OUTPUTS : NONE
   DESTROYS : C, B, A
   CALLS : CO
   CALLING ADDRESS : C080

DESCRIPTION : This routine generates a prompt character for the LCI-SM monitor. This character is .

3. FUNCTION : CMIP
   INPUTS : NONE
   OUTPUTS : Memory locations D505-D508
   DESTROYS : A,B,H,L
   CALLS : CI, GETCR
   CALLING ADDRESS : C0A7

DESCRIPTION: This routine inputs four characters from the terminal and stores their ASCII codes in the RAM area from D505 to D508. If more than 4 characters are inputted before CR then the ASCII codes of first four characters will be transferred to the RAM area. After inputting the four characters, the routine waits for CR to be pressed otherwise it ignores any other character.

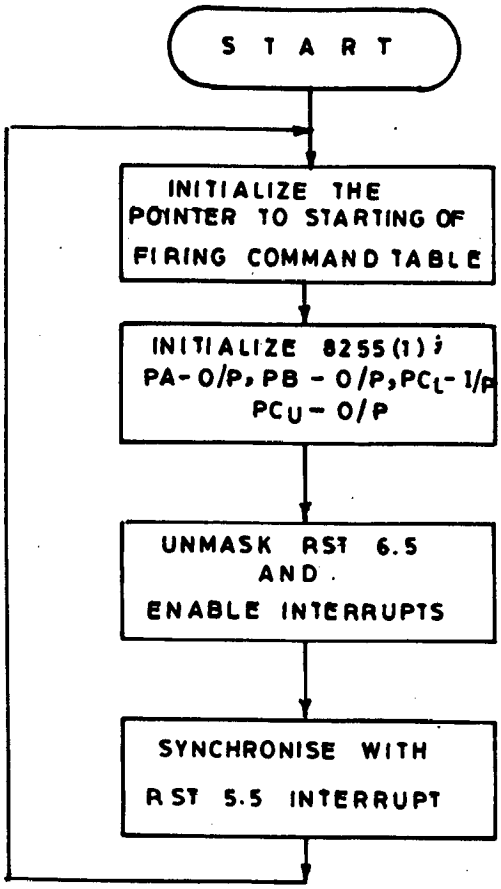


FIG. 3.15. FLOW CHART FOR LCI - FA MAIN PROGRAM

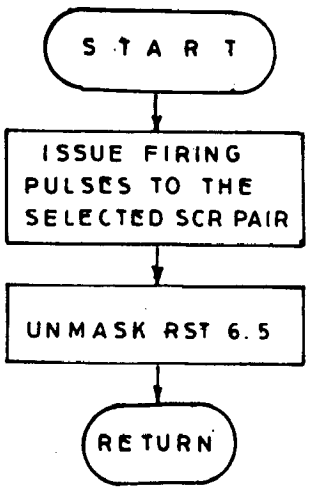


FIG. 3.16. FLOW CHART FOR RST 5.5 I.S.S

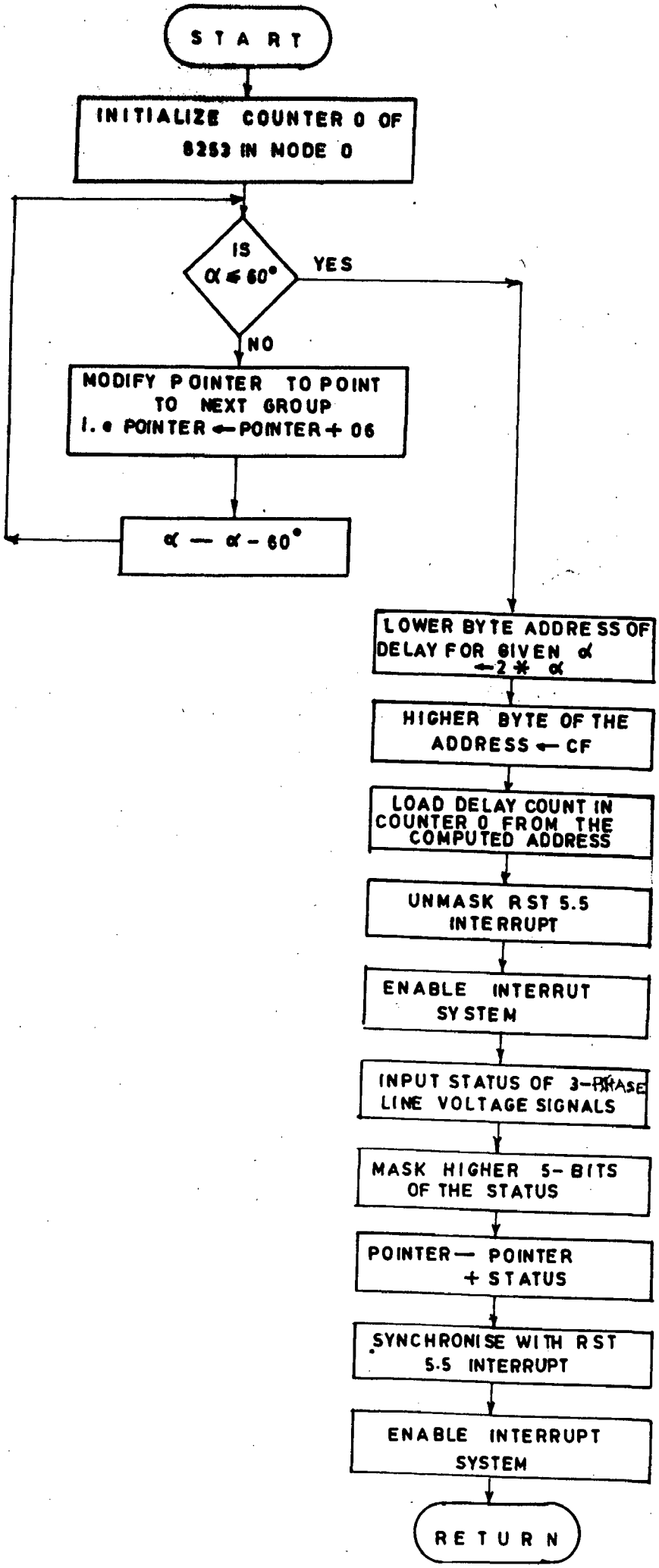


FIG. 3.17. I.S.S FOR RST 6.5 INTERRUPT

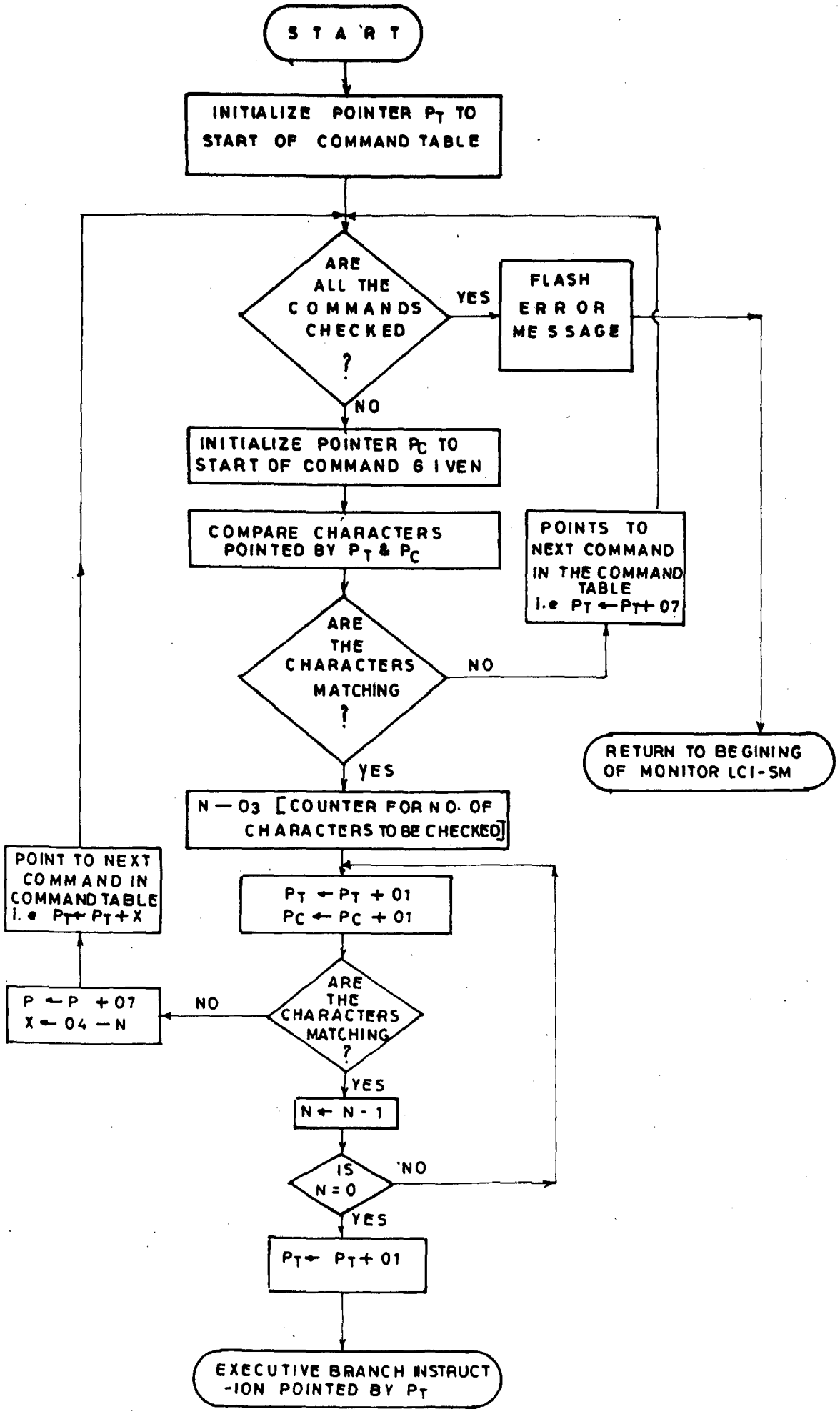


FIG. 3.18. FLOW CHART FOR THE ROUTINE CMPCH

4. FUNCTION : CMPCH

INPUTS : Memory locations D530-D54B,D505-D508.

OUTPUTS : NONE

CALLS : MLPNT

DESTROYS : A,B,C,D,E,H,L

CALLING ADDRESS : C0FA

DESCRIPTION: This routine compares the previously stored command character ASCII codes in location D505-D508 with the command ASCII codes in the command table stored in locations D530-D54B. If the inputted command matches any command in the command table then the program jumps to the starting address of command service subroutine and if no match is found for the command after having searched the entire table a message of ERROR b CALL b HELP , is flashed on the CRT and the routine returns to LCI-SM monitor. The number of commands to be compared from the table is indicated by the contents of register C i.e.

number of commands = Content of C Register-1.

5. FUNCTION : CHLOAD

INPUTS : NONE

OUTPUTS : D,E, carry flag, Memory location DD501,D502

DESTROYS : B,C,D,E

CALLS : GETHX

CALLING ADDRESS : C070

DESCRIPTION: This routine stores the value of firing angle α input from the terminal. A string of hex digits are accepted from the input stream and their value is returned as a 16 bit

binary in register pair BC. If more than four hexadecimal digits are entered only the last four before the valid delimeter are accepted. The valid delimeters are CR, b. Comma. The delimeter is also returned as a count on D register. Illegal character (i.e. not hex digit or delimeter) causes an error indication by printing * blank. In case ESC is entered, the control is returned to the VMDS-85 monitor by printing a ? and *

The least significant two digits are stored in the memory location D501 as the new firing angle value and the content of memory location D502 are made 3C i.e. hexa-decimal equivalent of 60 in decimal system.

6. FUNCTION : CI
   INPUTS : NONE
   OUTPUTS : A
   CALLS : Delay
   DESTROYS : A, Flags
   CALLING ADDRESS : 814 F

DESCRIPTION: Interrupt is disabled in this routine. CI waits until a character has been entered at the terminal and then returns the character via register A tocalling routine

7. FUNCTION : CO
   INPUTS : C
   OUTPUTS : NONE
   CALLS : Delay
   DESTROYS : A,
   CALLING ADDRESS : 8187

DESCRIPTION: This routine sends its input argument to I/O

device. Interrupts are disabled .

8. FUNCTION : DELAY

INPUTS : D,E

OUTPUTS : NONE

CALLS : NONE

DESTROYS : A,D,E.

CALLING ADDRESS : 81C0

DESCRIPTION: Delay does not return to the caller centil input argument is counted down to zero. The delay equation is (24N+17)x320 n sec where N is count in Registar pair,D E.

9. FUNCTION : GETHX

INPUTS : NONE

OUTPUTS : B,C,D,E, carry flag

CALLS : CHECHO, VALDL, SRET, FRET, VALDG, CNVEN, BKSTBK, MNTERR, CLRHL

DESTROYS : A,B,C,D,E, flags

CALLING ADDRESS : 81EA

DESCRIPTION: It accepts a string of hex digits from the the input stream and returns their values as a 16 bit binary integer in registar pair BC. If more than four hex digits are entered, only last four are used. The number terminates when a valid delimites is encountered. The valid delimeters are CR;b; comma. The delimeter is also returned as an output in registar D. Illegal characters (not hex digits and delimeter) causes an error indication by printing blank* blank. If the first character encountered in the input stream is

not a delimeter, GETHX will return with carry bit set to 1 otherwide the carry bit is set to zero and the contents of BC are made zero. In case ESC is entered the routine is interrupted and the control is returned to monitor of VMDS-85 by printing a 9 and '*' on the terminal.

10. FUNCTION : MLPNT
INPUTS : B.H,L
OUTPUTS : NONE
CALLS : CO
DESTROYS : A,B,C,H,L
CALLING ADDRESS : 82F5

DESCRIPTION: The block of ASCII masked parity characters pointed by Register pair HL is printed up to the n^{th} position where as n is defined by Registar B.

11. FUNCTION : GETCR
INPUTS : NONE
OUTPUTS : NONE
CALLS : CHELHO, SRET, MNTRET
DESTROYS : A,B,C
CALLING ADDRESS : 82E5

DESCRIPTION: The routine remains in a loop ful a the CR is encountered. In case of ESC the control goes to the VMDS-85 monitor.

12. FUNCTION : STAR

INPUTS : Memory locations D54B-D54F,B,H,L

OUTPUTS : D,E,Carry flag, Memory locations D501, D502

CALLS : SWO, MLPNT, CHLOAD

DESTROYS : A,B,C,H,L,D,E

CALLING ADDRESS : CODO

DESCRIPTION: The STAR functional command has been developed enables the operator to order the microcomputer to execute the main program of LCI firing angle control (α control).

The command has to be given in following format.

FORMAT : STAR CR

The command will cause the execution of the following steps

1. The CRT screen will be cleared. The cursor will return to the home position on the screen.

2. Displays of sign-on message, i.e., the name of the thesis and of the guides will be displayed on the CRT in the following format.

   MICROCOMPUTER ∅ CONTROL ∅ OF ∅ ICI ∅ FOR
   INDUCTION ∅ MOTOR ∅ DRIVE CR LF LF

   GUIDED∅BY - 1. DR.D.R.KOHLI∅2. MR. M.K. VASANTHA
   CRLF

   FIRING ANGLE XXXX.

3. After the question mark the program waits for the firing angle to be inputted from the terminal. Any value of firing angle from 0 to 180^{o} can be

entered in hexa-decimal form. The program will accept the last four digits before CR. The two Least significant digits will be transferred to the predetermined location in RAM area as the firing angle of LCI. The two most significant digits will be converted to 3C (i.e. hexa decimal equivalent of 60 in decimal system) this will be again loaded in the succeeding memory location and then utilised by the program as a reference value of 60^{o}.

4. After having inputted firing angle value command is transferred to the LCI firing angle control program.

13 FUNCTION : HELP

INPUTS : B,H,L,

OUTPUTS : A,

CALLS : MLPNT, PCGR, CI, Delay

DESTROYS : A, Flags, C,B,H,L.

CALLING ADDRESS : COBA

DESCRIPTION: In order to help a new operator having no prior knowledge of the commands developed a command named as HELP Command has been developed. When ever the operator gives an invalid command, the LCI-SA-monitor program will flash on the CRT terminal a message 'ERROR␣CALL␣HELP'

The format of the HELP command is as given

FORMAT : HELP CR

1. HELP - COMMAND␣LIST CR LF

2. STAR - STARTING OF PROGRAM OR LF COMMAND NO x .

The operator can call the STAR functional command by inputting its command number from the table list displayed on the CRT.

If any other command number is given an error message will be flashed on CRT and the program will return to the ICI-SM monitor, waiting again for another valid command.

3.1.2 CONCLUSION:

Thus in this chapter the LCI firing scheme software using 8085 based microcomputer has been discussed. A special explanation has been given for the role of VCO in the above scheme. The functional commands that have been developed to simplify the work of an operator controlling the system have also been discussed.

CHAPTER IV

STEADY STATE CHARACTERISTICS OF LCI AND SYNCHRONOUS MACHINE

4.1 GENERAL

In this chapter an attempt has been made to predict and verify experimentally the performance of LCI-synchronous motor under variable frequency operation. Steady state equations governing the performance of LCI-SM have been established by Ranganadhachari[29] using the equivalent circuit model. These equations give the interdependence of performance parameter of machine on the control variables such as firing angle α. These performance equations have been given in this chapter and **are** used to explain the practical observations drawn out of the extensive tests carried out on the laboratory setup of LCI-SM.

4.2 ANALYSIS OF LCI-SYNCHRONOUS MACHINE SYSTEM OPERATING AS A VARIABLE SPEED DRIVE:

Hirara and Takeda[39] have given a generalised analysis in terms of machine inductances and other basic parameters of the motor. This analysis gives a clear picture of effect of damper windings, compensating windings, and saliency on machine performance. Although this approach gives good results, it is relatively complex since many parameters are needed or the fluxes on the two axis must be known. The computations for machine performance evaluation are quite involved. Hence the simple equivalent circuit method of obtaining performance equations given by Ranganadhachari[29] has been used in the present computations of performance.

The LCI-synchronous motor combination has two operating modes,

1. Conduction mode,
2. Commutation overlap mode.

The conduction mode corresponds to the period when current flows through the two phases of the armature winding. The effective equivalent circuit for this mode is a voltage source E (i.e. no load induced emf)in series with synchronous reactance).as shown in Fig.4.1.

The commutation mode corresponds to the period during which the current flows through all three phases of armature winding resulting in a line to line short circuit. The effective equivalent circuit for this mode of operation is voltage E in series with the commutating reactance X_c which is equal to negative sequence reactance of synchronous machine. The negative sequence reactance X_c is equal to the mean of the direct axis and quadrature axis subtransient reactances

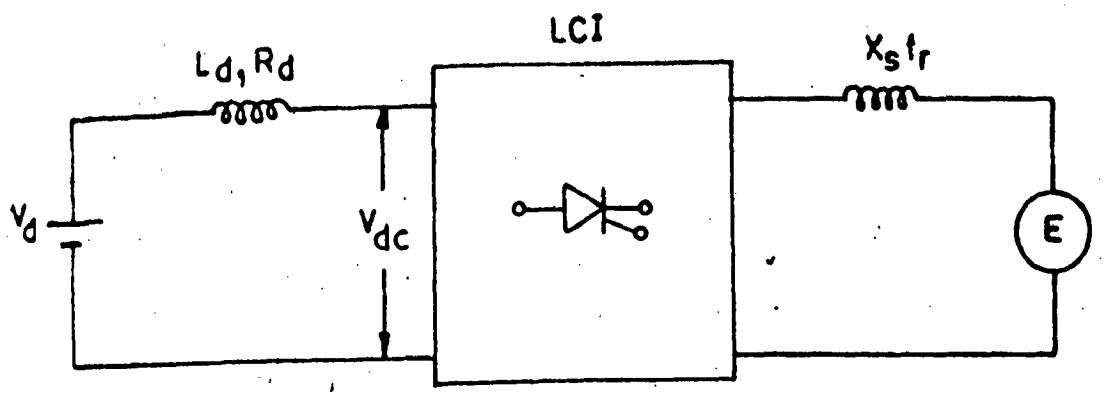
$$\text{i.e.} \quad X_c = \frac{X_d + X_q}{2}$$

These two equivalent circuits are used to derive the performance equations.

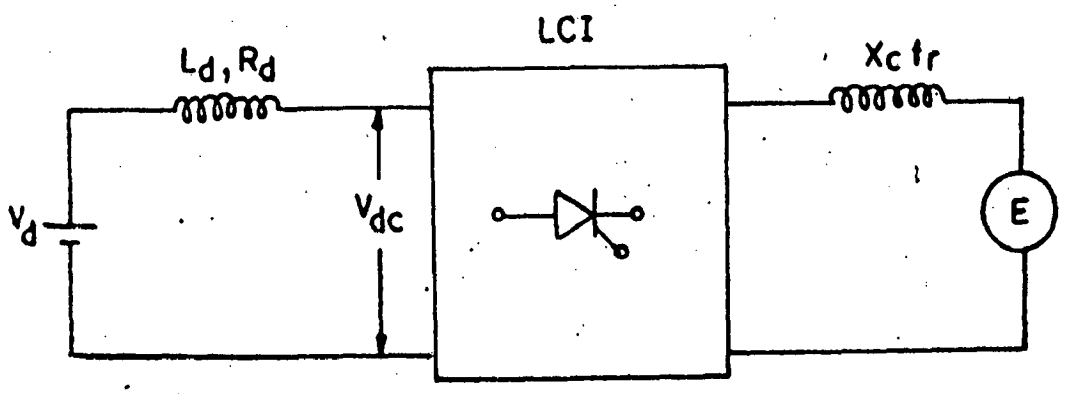
4.2.1 ASSUMPTIONS

The following simplifying assumptions have been made in obtaining the performance equations:

1. Magnetic saturation of the synchronous machine



(a) Conduction period



(b) Commutation period

Fig 4.1 Equivalent circuits of LCI-synchronous machine for conduction period and commutation period

for all operating conditions is neglected,

2. No load losses of synchronous machine i.e. iron losses, friction and windage losses, etc are neglected,

3. The resistive drop $I_{sy}R_{sy}$ in the winding resistance R_{sy} is neglected,

4. Voltage drop accross diodes and SCRs in conduction mode are neglected,

5. The D.C. link current is assumed ripple free,

6. The current harmonics of the LCI are negligible.

4.2.2 EQUATIONS FOR CONDUCTION PERIOD

From the equivalent circuit for the conduction period as given in Fig 4.1, the synchronous machine operation can be represented by a phasor diagram as shown in Fig 4.2.

Since the synchronous motor is operated in an over excited mode, it operates at a leading power factor Thus the synchronous machine current I_{sy} always leads the terminal voltage V by a given supplementary displacement angle β', and the induced voltage E by an angle γ. The terminal voltage V can be obtained as a phasor difference between the induced e.m.f. E and the reactive voltage drops. $I_{syd}x_d f_r$ and $I_{syq}X_q f_r$ these reactive voltage drops lead their respective current components I_{syd} and I_{syq} by 90^o. In this case X_d and X_q are the direct axis and the quadrature axis reactances at base frequency of 50 Hz, and f_r is the

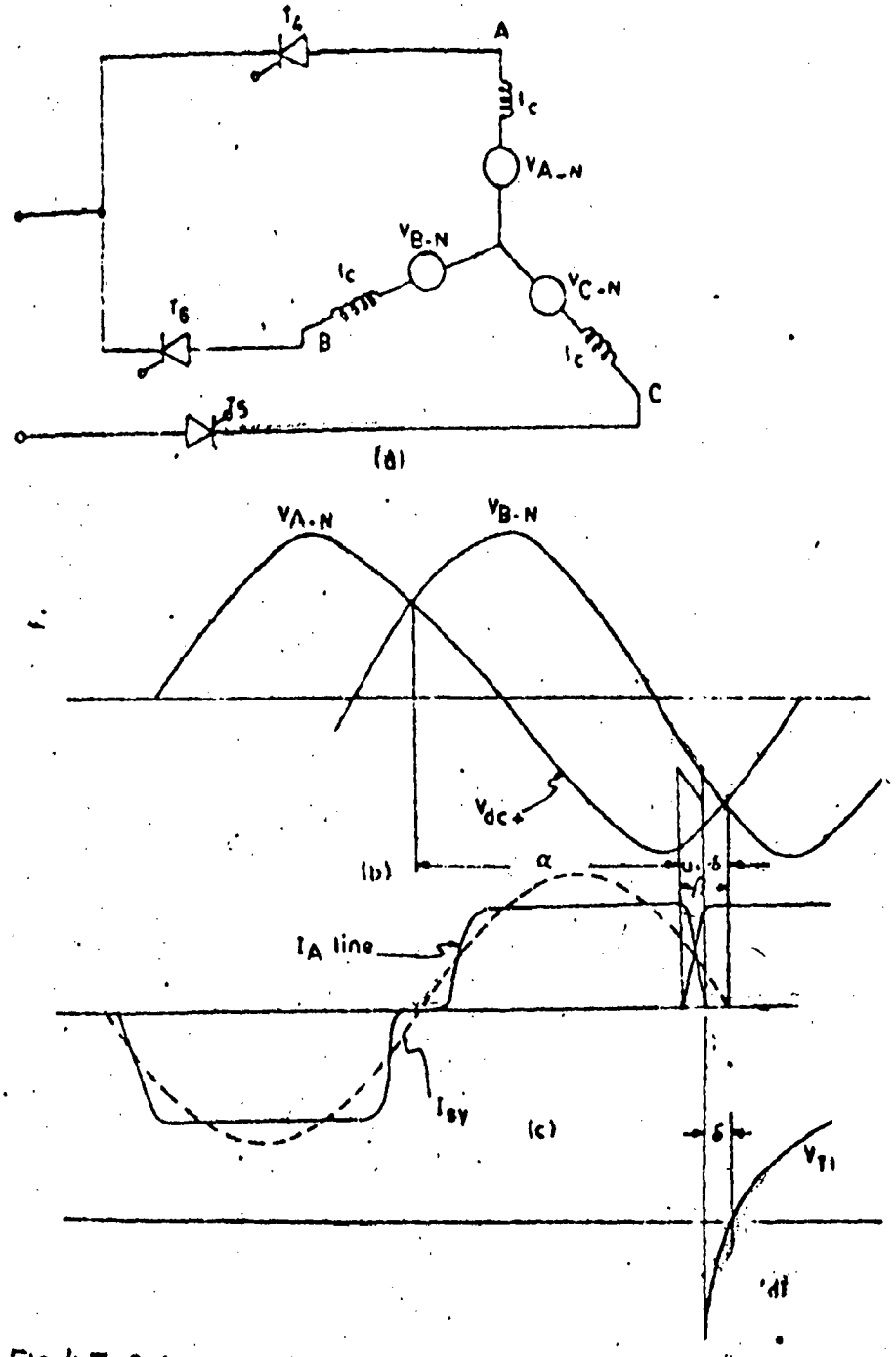


Fig 4.3 Definition of SCR commutating terms

ratio of the angular frequency at a given speed to angular frequency at base speed. For a set speed and field excitation, ϕ and E are constant. The relationship between V,E, I_{sy}, I_{syq}, $X_d f_r$, $X_q f_r$ is as described by,

$$V^2 = [E - I_{syd}(X_d f_r)]^2 + [I_{syq}(X_q f_r)]^2 \qquad \ldots \quad (4.1)$$

Using the following relationships

$$X_q = q X_d \quad , \quad I_{syd} = I_{sy} \sin Y$$

$$I_{syq} = I_{sy} \cos Y,$$

The ratio of V and E is given by

$$\frac{V}{E} = \left[1 - \frac{2I_{sy}X_d f_r}{E} \sin Y + \left(\frac{I_{sy}X_d f_r}{E}\right)^2 (\sin^2 Y + q^2 \cos^2 Y)^2\right]^{1/2} \qquad \ldots \quad (4.2)$$

The relationship between angle Y and β' can be defined from phasor diagram as

$$\left.\begin{aligned} \cos (Y-\beta') &= \frac{E - I_{sy} X_d f_r \sin Y}{V} \\ \sin (Y-\beta') &= \frac{q\, I_{sy} X_d\, f_r \cos Y}{V} \end{aligned}\right| \qquad \ldots \quad (4.3)$$

4.2.3 EQUATIONS FOR COMMUTATION PERIOD

The commutation period as well as the D.C. and A.C. side relationship of the converter are discussed with the help of Fig.4.1. This figure shows the commutation event from SCR T_4 in line A to SCR T_6 in line B. The instant of starting of commutation is defined by the firing angle α

or the supplementry commutation lead angle $\beta = (\pi-\alpha)$ Prior to the instants defined by these angles, the SCR T_4 is conducting. The amplitude of line current equals the amplitude of D.C. link current I_{dc}. When the SCR T_6 is fired, the conduction in line B is initiated, also the SCR T_4 current starts reducing. Due to the presence of source reactance or commutating reactance $X_c f_r$. Commutation of out going SCR does not take place instanteneously resulting in a commutation over lap angle μ . The current in SCR T_6 gradually rises to the value of I_{dc} while the current of T_4 reduces to zero, depending upon the voltage difference $V_{BA} = V_{A\,N} - V_{BN}$ At any instant in commutation overlap region $I_{syA}(\text{line}) + I_{syB}(\text{line}) = I_{dc}$. At the instant marked as the commutation margin angle or the turn off angle δ the SCR T_4 ceases to conduct and becomes reverse biased for an angle δ as shown in Fig 4.3. This angle δ should be greater than the turn off time of SCR for fail proof commutation. Although the commutation is initiated at β the time for which the reverse recovery voltage is available to SCR for supporting the forward voltage is defined by overlap angle μ . Also the voltage drop on the D.C. side due to commutation overlap is given as $\frac{3}{\pi} X_c f_r I_{dc}$.

The output D.C. voltage of bridge is given by equation 4.3(b), considering the effect of sequence inductance into account

$$V_{dc} = \frac{3}{\pi} (\sqrt{6}\, V \cos \beta + I_{dc} X_c f_r) \qquad \ldots \qquad 4.3(b)$$

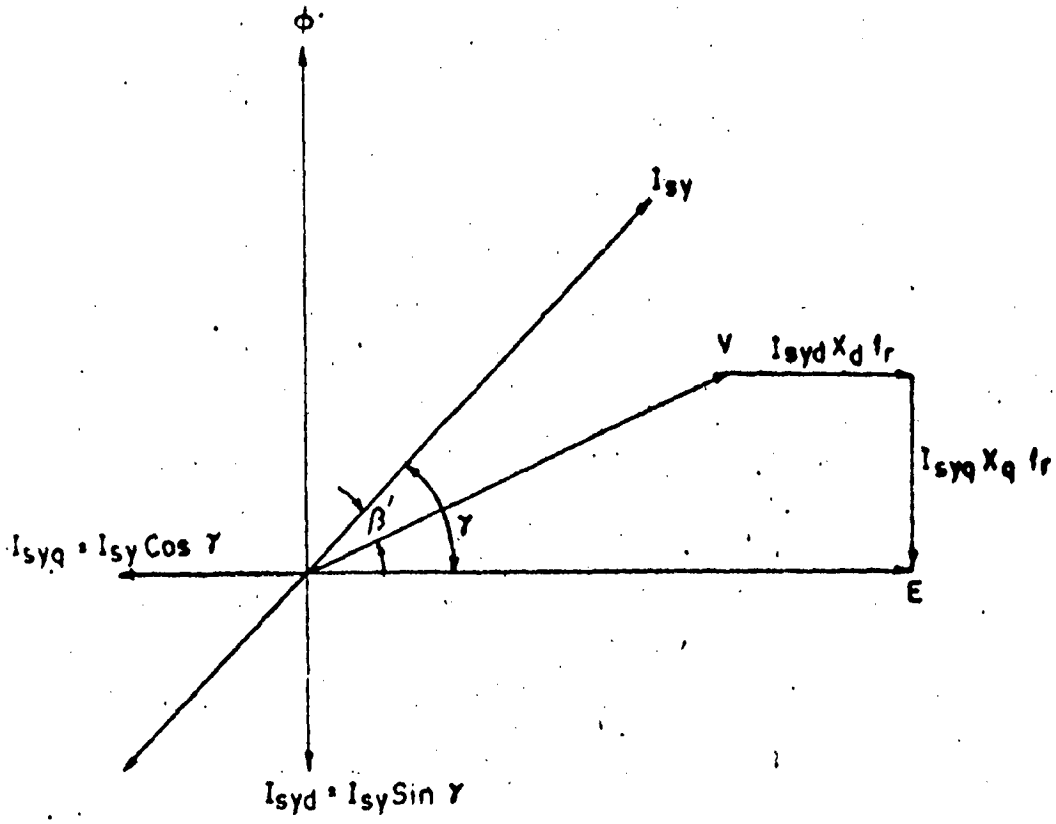


Fig 4.2 Phasor diagram of LCI - synchronous machine (CLM) system

4.2.4 TORQUE EXPRESSION

The electromagnetic torque developed by the synchronous machine can be obtained from the vector diagram of Fig 4.2. The torque is given by

$$T = \frac{3VI_{sy} \cos \beta'}{w_{sy}} \quad \ldots \quad (4.4)$$

where w_{sy} is the speed of the synchronous motor and is given by

$$w_{sy} = \frac{V_d - I_{dc} R_d}{K W_1 \cos \beta} \text{ rad/sec} \quad \ldots \quad (4.5)$$

V_d = D.C. link voltage.

K_{w1} = Speed constant of synchronous machine expressed in volts/rad/sec.

From equations 4.4 and 4.5 it is clear that the electromagnetic torque can be controlled by controlling the following three independent variables.

1. D.C. link current, I_{dc},
2. Commutation lead angle β,
3. Field current which determines the ratio of E/f

4.3 EXPERIMENTAL INVESTIGATIONS FOR STEADY STATE PERFORMANCE OF LCI-SYNCHRONOUS MOTOR SYSTEM:

The experimental investigations to obtain the steady state performance of LCI-SM system have been carried out in two parts.

1. No load tests.
2. Load tests.

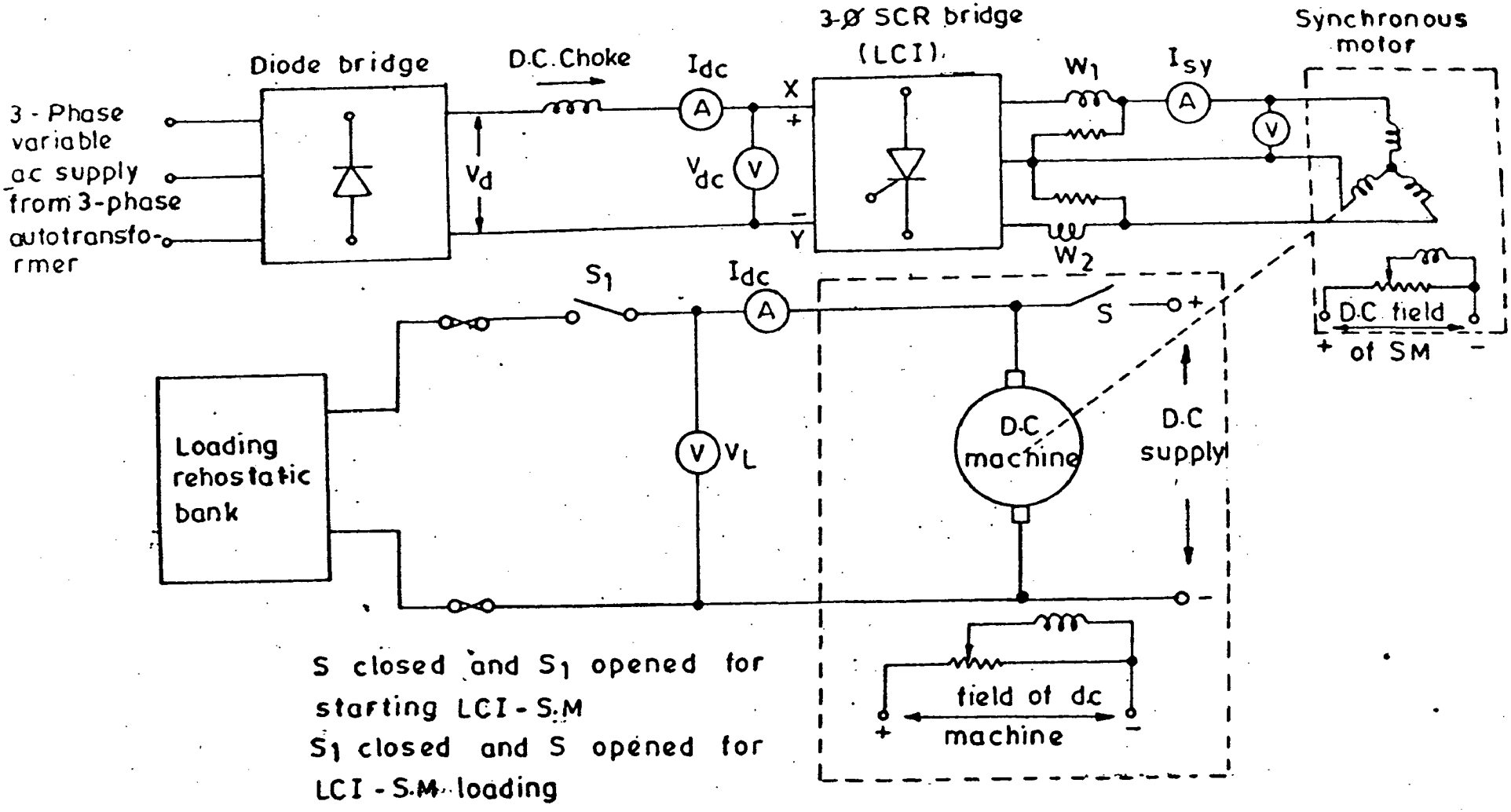


FIG. 4.4 Experimental set-up of LCI-synchronous machine system

As it has been explained earlier the speed of commutatorless motor is given by

$$N_{sy} = K \frac{V_{dc}}{(\cos \alpha) I_f} \quad \ldots \quad (4.6)$$

From the above equation 4.6 it is clear that motor speed is a function of three independent variables.

They are;

1. D.C. link voltage, I_{dc},
2. Cos α, i.e. firing angle of LCI,
3. I_f, field current of synchronous motor

In the experimental work carried out, one out of the three control parameter is varied keeping the other two parameters constant, and the effect of this single parameter on motor speed, power factor, torque etc is observed. The no load experimental investigations are further divided into three parts, in each part one out of the three parameters is varied keeping the other two constant.

The details of the motors i.e. D.C. synchronous and induction motors on which the experiments are carried out, are given in Appendix I . The detailed layout of the experimental setup including the instrumentation is shown in Fig 4.4.

Since no automatic starting scheme could be developed due to short span of the thesis period a manual starting procedure is used.

4.4 STARTING OF THE LCI-SYNCHRONOUS MOTOR SYSTEM:

The laboratory method of starting of LCI-SM system involved the following steps:

1. The microcomputer is given the value of firing angle α. Then the microcomputer proceeds to execute the software program for control of firing angle of LCI. The sequential triggering of SCR pairs by the microcomputer depends upon the status of terminal (line) voltage of synchronous motor.

2. While starting from the stand still position, there is no possibility of sensing the terminal voltage, hence a D.C. motor of small rating is used to drive the synchronous motor as a generator. The no load generated e.m.f. of the generator is used by microcomputer for sequential firing of SCRs. Depending upon the firing angle a D.C. terminal voltage will be produced at the D.C. terminal output of SCR bridge. If the firing angle is greater than 90^{o} then the terminal X as shown in the Fig 4.4 is positive and the terminal Y as shown in Fig 4.4 is negative. (i.e. the bridge is working in inverter mode), ready to draw power from the D.C. side, provided a source of proper polarity and magnitude is connected.

3. The D.C. output of three phase rectifier is connected to the inverter D.C. terminals. The

terminals of same polarity of both the bridges are connected together. Power can flow from the three phase rectifier to the synchronous motor via the LCI only when the rectifier bridge voltage is greater than the inverter output voltage.

4. The input voltage to the rectifier bridge is increased with the help of a three phase auto transformer. The current starts flowing into the LCI as indicated by the D.C. link ammeter. Thus the synchronous machine starts drawing active power from the D.C. link resulting in a corresponding decrease of D.C. motor current.

5. As the D.C. link voltage is increased the speed of synchronous motor increases. At a particular value of V_{dc} the power drawn by the D.C. motor reduces to zero. Thus the synchronous machine can now be operated as a CLM by disconnecting the D.C. motor.

In the above starting operation the synchronous motor field current is adjusted to such a value that the synchronous machine operates in an overexcited state i.e. drawing current at leading power factor.

The operation of commutatorless motor having been achieved, extensive tests i.e. no load tests and load tests were carried out on the system to obtain the performance characteristic of the CLM.

4.5 RESULTS AND DISCUSSIONS:

With the aim of obtaining the output speed and frequency range of LCI-SM system controlled by the three independent variables i.e. (I_f, cos α, V_{dc}) no load tests have been carried out on the system.

The no load characteristics are obtained in three parts:

1. Keeping V_{dc} and cos α constant and I_f is varied.
2. Keeping I_f and cos α constant and V_{dc} is varied.
3. V_{dc} and I_f are kept constant cos α is varied.

The first part of experimental investigation is devoted to practically find out the effect of field current on speed of CLM with V_{dc} = constant and cos α = constant. Field current has been varied from 8 Amps to 3 Amps below this value of field current, it has been observed that commutation failure occurs. This is due to the inability of synchronous motor to operate in an over excited mode at reduced value of field current.

The effect of field current variation has been studied on number of system performance parameters such as,

1. No load speed,
2. No load power factor,
3. Terminal voltage of synchronous motor.

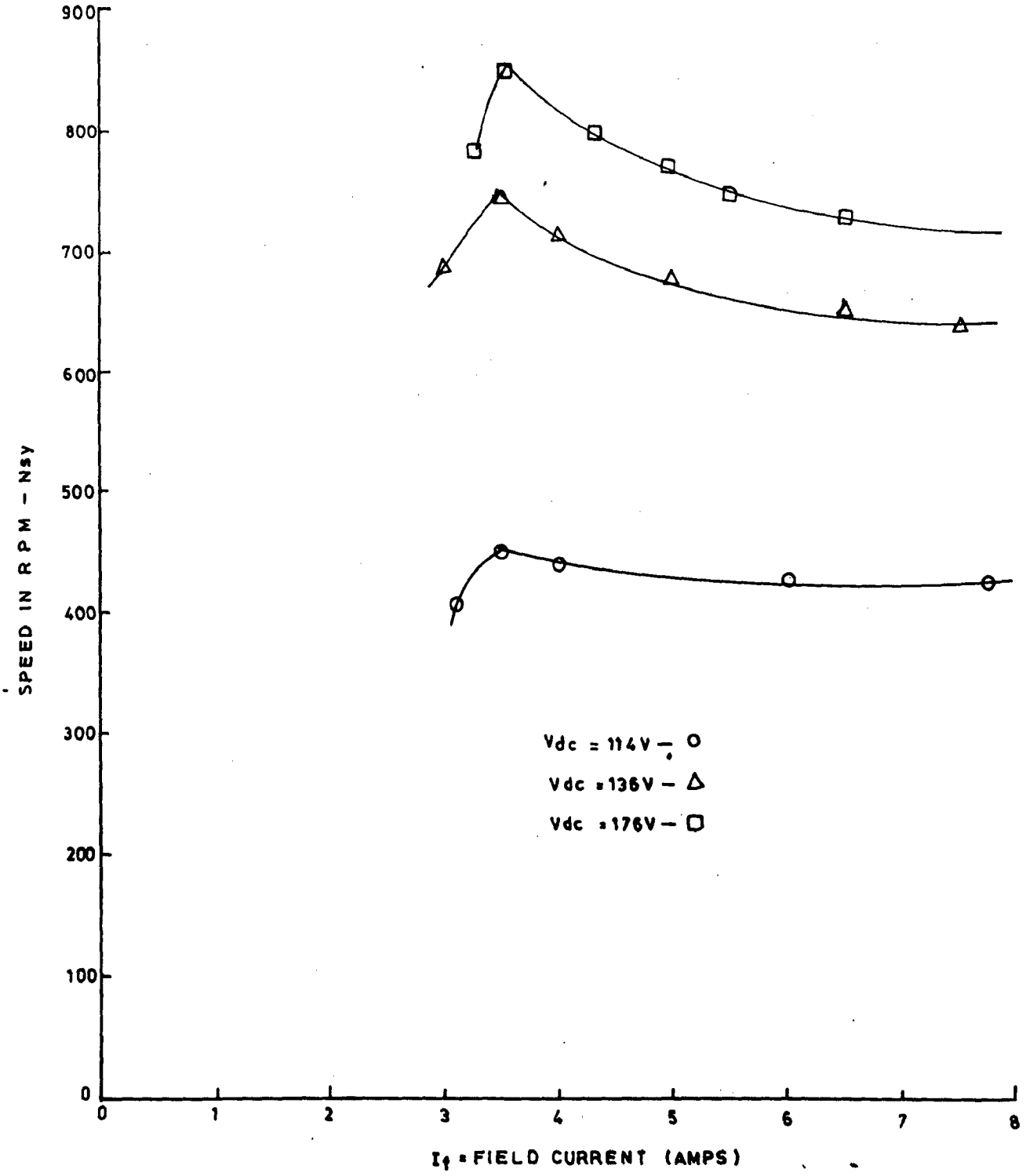


FIG. 4.5 SPEED-FIELD CURRENT (I_f) CHARACTERISTICS FOR CONSTANT VALUE OF α AND DIFFERENT VALUES OF D.C. LINK VOLTAGE Vdc

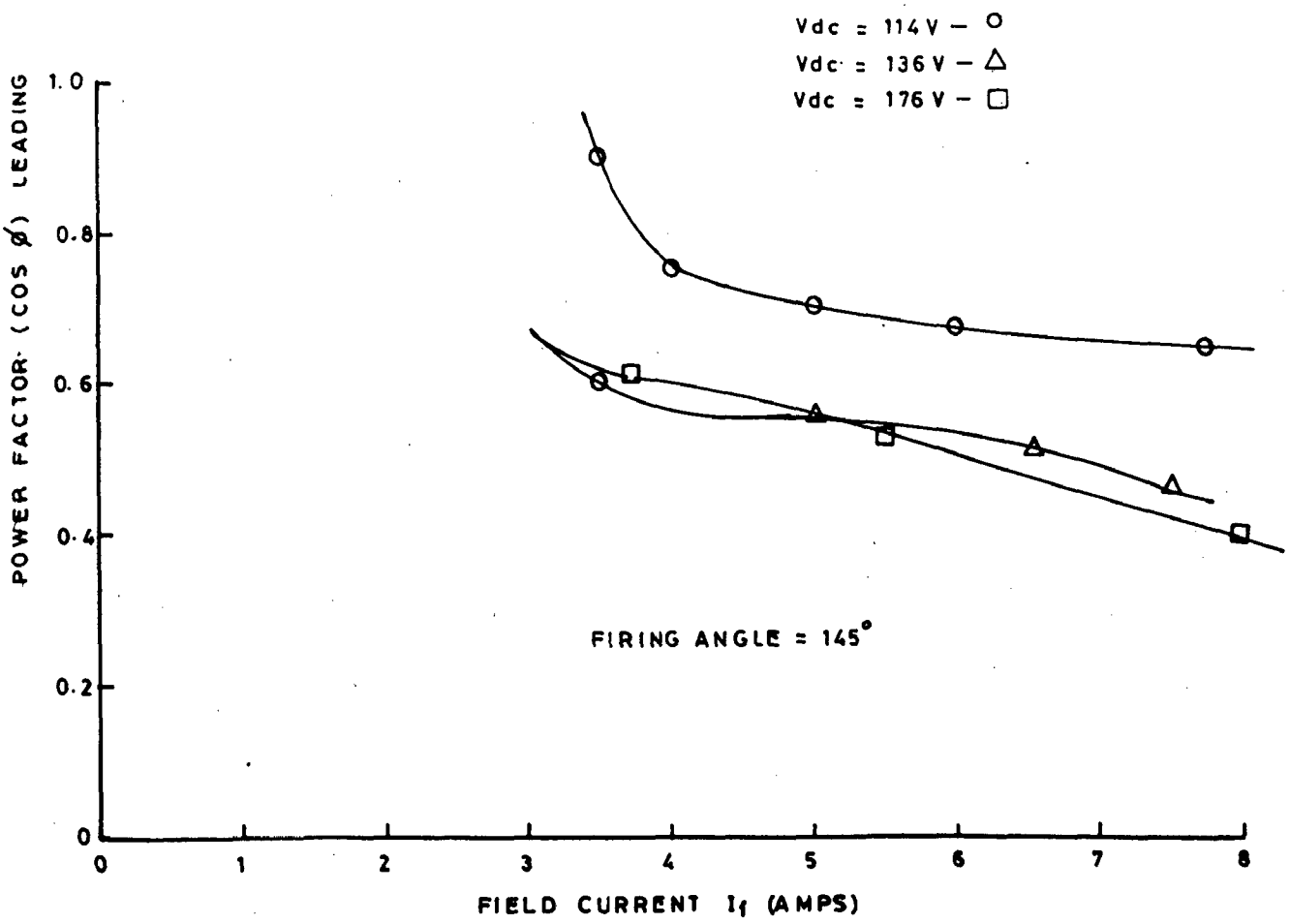


FIG. 4.7 SYNCHRONOUS MOTOR POWER FACTOR (COS Ø) FIELD CURRENT (I_f) CHARACTERISTICS

4.5.1 EFFECT OF VARIATION OF I_f ON SPEED

The speed versus field current characteristics at different voltages and a constant firing angle $\alpha = 145^{\circ}$ are given in Fig 4.5. From the figure it is clear that as the field current decreases gradually from 8A to 3A, the speed gradually increases upto a critical value of field current, if the field current is further decreased then the motor deaccelerates and slows down, because electromagnetic torque produced by motor with weakened flux is insufficient to overcome the losses. The critical value of field current is a function of D.C. link voltage, firing angle α and the load torque.

The range of speed controlled by variation of field current is again dependent upon the D.C. link voltage V_{dc}, it increases with the increase in V_{dc} for a constant value of α i.e. 145°.

The curves in Fig 4.5 and 4.9 give the change in speed of CLM with field current at $V_{dc} \pm 114$ V and $\alpha = 145^{\circ}$ and $\alpha = 125^{\circ}$. Comparing the two characteristics it can be concluded that comparatively higher speeds and range of speed control with change in I_f are obtained at lower value of firing angle i.e. $\alpha = 125^{\circ}$. Than for $\alpha = 145^{\circ}$.

4.5.2 POWER FACTOR VERSUS FIELD CURRENT CHARACTERISTICS (NO-LOAD):

The variation of power factor on no load, with field current at constant V_{dc} and α is given in Fig.4.7.

From the figure it is clear that weakening of field improves power factor. The improvement is again a function of V_{dc} i.e. smaller the value of V_{dc}, the larger or more better will be the power factor improvement with field current weakening.

The value of power factor at a particular value of I_f and V_{dc} is again a function of firing angle. The smaller the angle the more leading will be the power factor.

The improvement in power factor with poorer excitation can be explained from the

V = terminal voltage of synchronous machine

E = Back e.m.f or generated e.m.f.

δ = load angle

β' = Synchronous motor power factor angle

I_{sy} = Synchronous motor current

Now $V = \sqrt{2}\ \pi\ K\ \phi\ f\ N_{ph}$ ... (4.7)

ϕ = flux

f = frequency

N_{ph} = number of turns per phase

K = constant

$\therefore$ $= V/f = \sqrt{2}\ \pi\ K\ \phi\ N_{ph}$ (4.8)

From the above equation (4.8) we get that as field flux is reduced V/f ratio reduces.

$$E = K\ w\ L_{md}\ I_f \quad \ldots \quad (4.9)$$

$$E/f = K \times 2\pi\ L_{md} I_f \quad \ldots \quad (4.10)$$

Hence E/f also reduces with I_f

Power delivered

$$P_{sy} = \frac{V\ E \sin \delta}{X_s} \quad \ldots \quad (4.11)$$

$$T_e = \frac{P_{sy}}{w_s} \quad \ldots \quad (4.12)$$

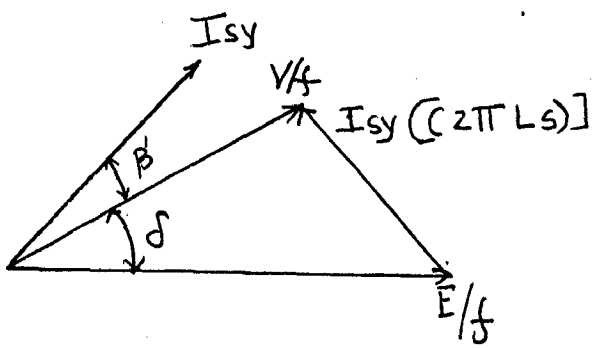
$$= \frac{V\ E \sin \delta}{2\pi f \times (2\pi f \times L_s)} \quad (4.13)$$

$$= \frac{V \times E \times \sin \delta}{4\ \pi^2\ f^2 \times L_s} \quad \ldots \quad (4.14)$$

$$T_e = \left(\frac{V}{f}\right) \times \left(\frac{E}{f}\right) \times \frac{\sin \delta}{4\pi^2 L_s} \quad \ldots \quad (4.15)$$

The two terms in the brackets of the equation 4.15 decrease with reduced field excitation hence to produce constant torque or the load torque, the only alternative is to increase δ i.e. load angle.

If the voltage vectors in the figure are divided by frequency then we get a vector diagram shown below.



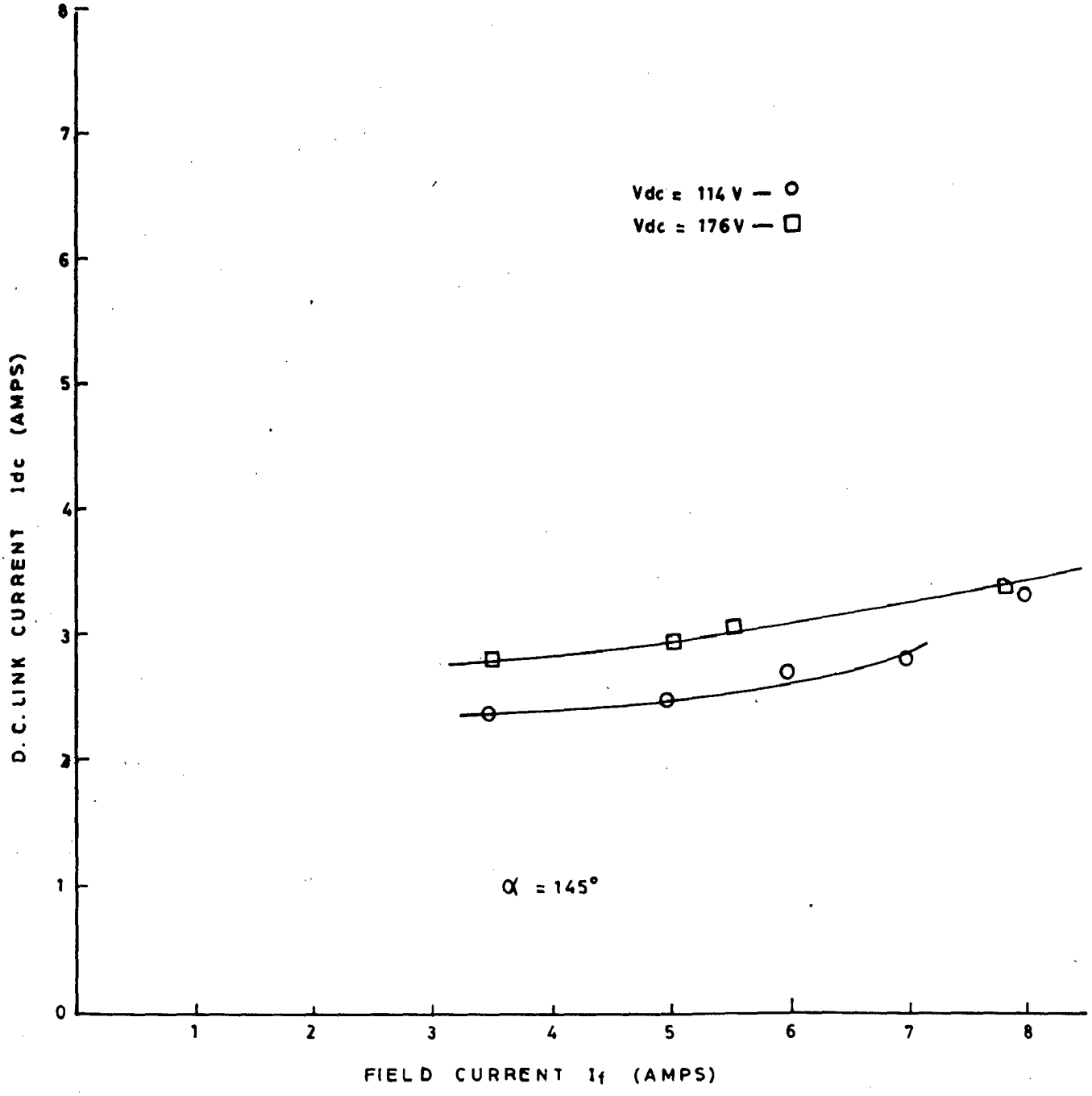


FIG. 4.6 D.C. LINK CURRENT - FIELD CURRENT CHARACTERISTICS AT α = CONSTANT AND DIFFERENT VALUES OF Vdc - LINK VOLTAGE Vdc

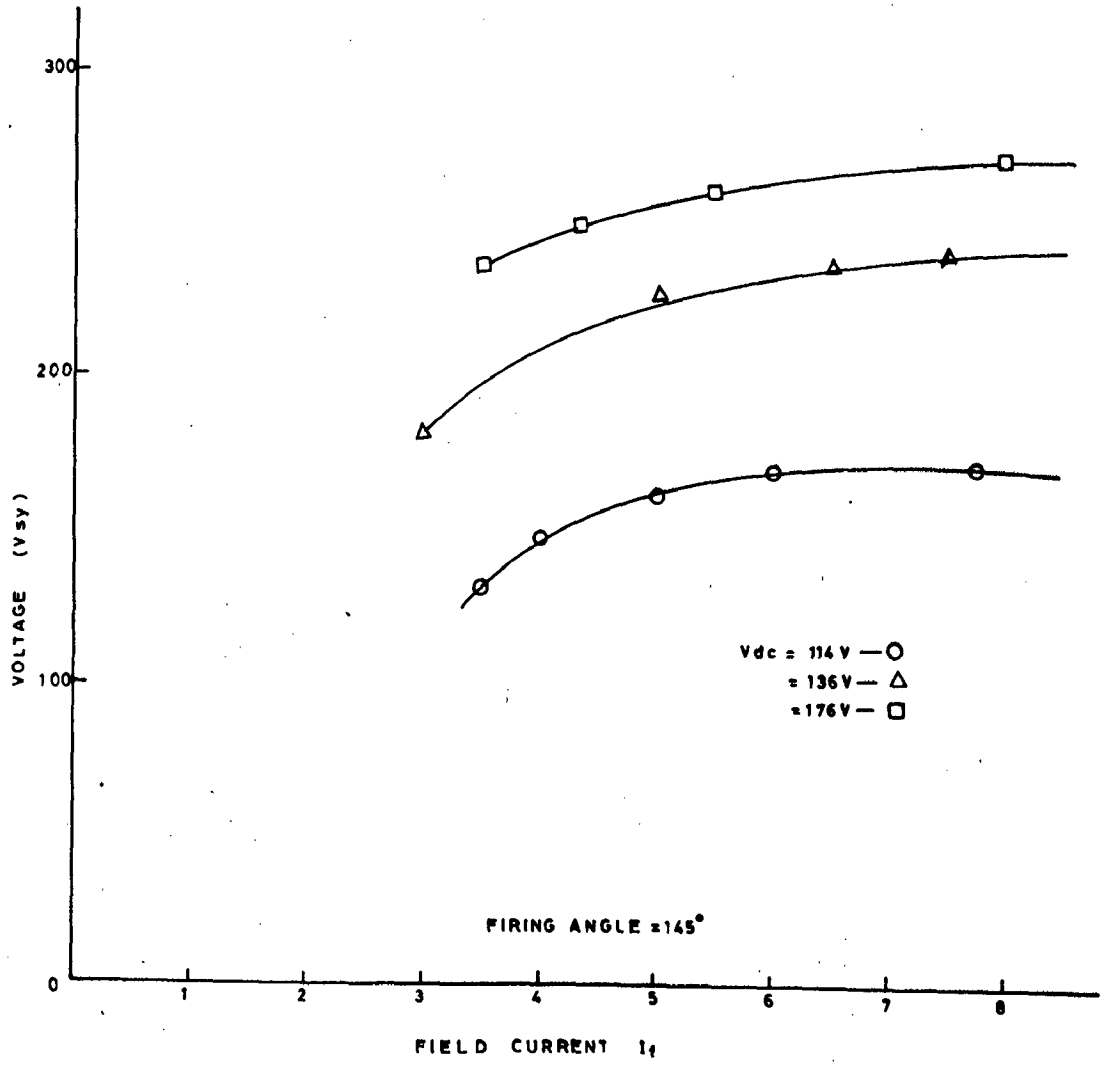


FIG. 4.8 TERMINAL VOLTAGE OF SYNCHRONOUS MOTOR (Vsy) VS FIELD CURRENT (If) CHARACTERISTICS AT $\alpha = 145^{\circ}$ AND FOR DIFFERENT VALUES OF D.C. LINK VOLTAGE Vdc

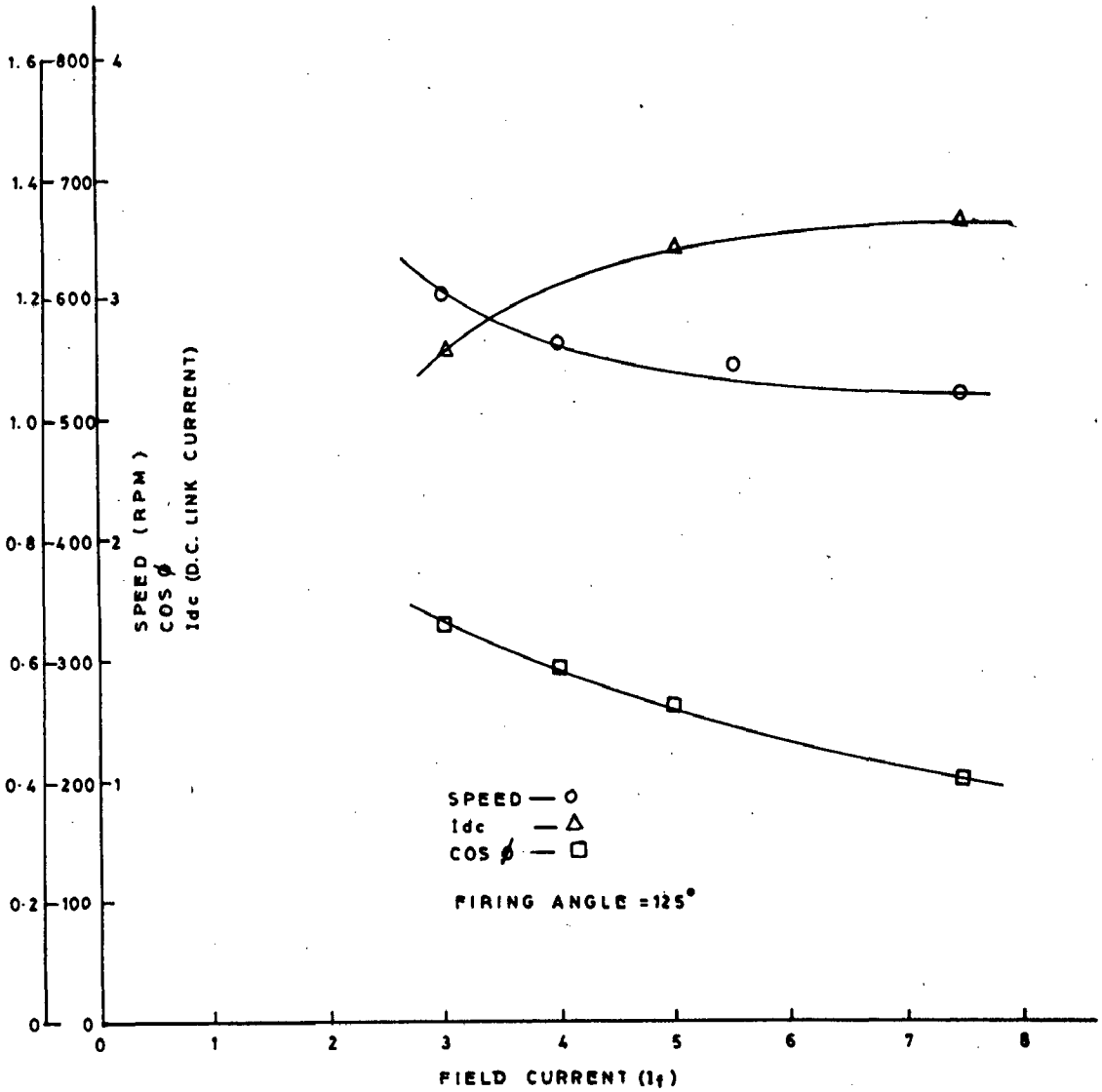


FIG. 4.9 VARIATION OF SYNCHRONOUS MOTOR POWER FACTOR (COS ϕ), SPEED AND D.C. LINK CURRENT WITH FIELD CURRENT (I_f) AT α = 125° AND D.C. LINK VOLTAGE Vdc = 114 V

The δ angle being increased and the two voltage vectors V/f and E/f, decreased proportionally. The third vector i.e. $I_{sy}(2\pi L_s)$ being independent of flux.(i.e. field current) has to balance the voltage vector triangle the only possible way is to improve the power factor angle β'. Thus with reduced excitation the machine power factor improves.

4.5.3 DC LINK CURRENT AND FIELD CURRENT CHARACTERISTICS

From the Fig 4.6 it can be seen that the D.C. link current decreases with corresponding decrease in motor field current at a constant value of D.C. link voltage V_{dc}, and firing angle α. The magnitude of D.C. link current is directly proportional to the magnitude of D.C. link voltage at a particular value of field current. The reduction of link current can be explained from the fact that, reduction of excitation causes the improvement of power factor. To maintain the same load torque, since power factor has improved synchronous motor current should decrease resulting in a corresponding decrease in D.C. link current. This fact can be shown with the below given relation.

$$T = \frac{3\ V\ I_{sy}\ \cos\beta}{w_s} \qquad \ldots \qquad (4.16)$$

$$= \frac{3}{2\pi}\left(\frac{V}{f}\right) I_{sy} \cos\beta' \qquad \ldots \qquad (4.17)$$

$V/f \ \alpha \ \phi$

$$\therefore \quad T_L = \frac{3}{2\pi} \times \phi \times I_{sy} \cos\beta' \qquad \ldots \qquad (4.18)$$

Now reduction in ϕ causes improvement of cos β' hence, to

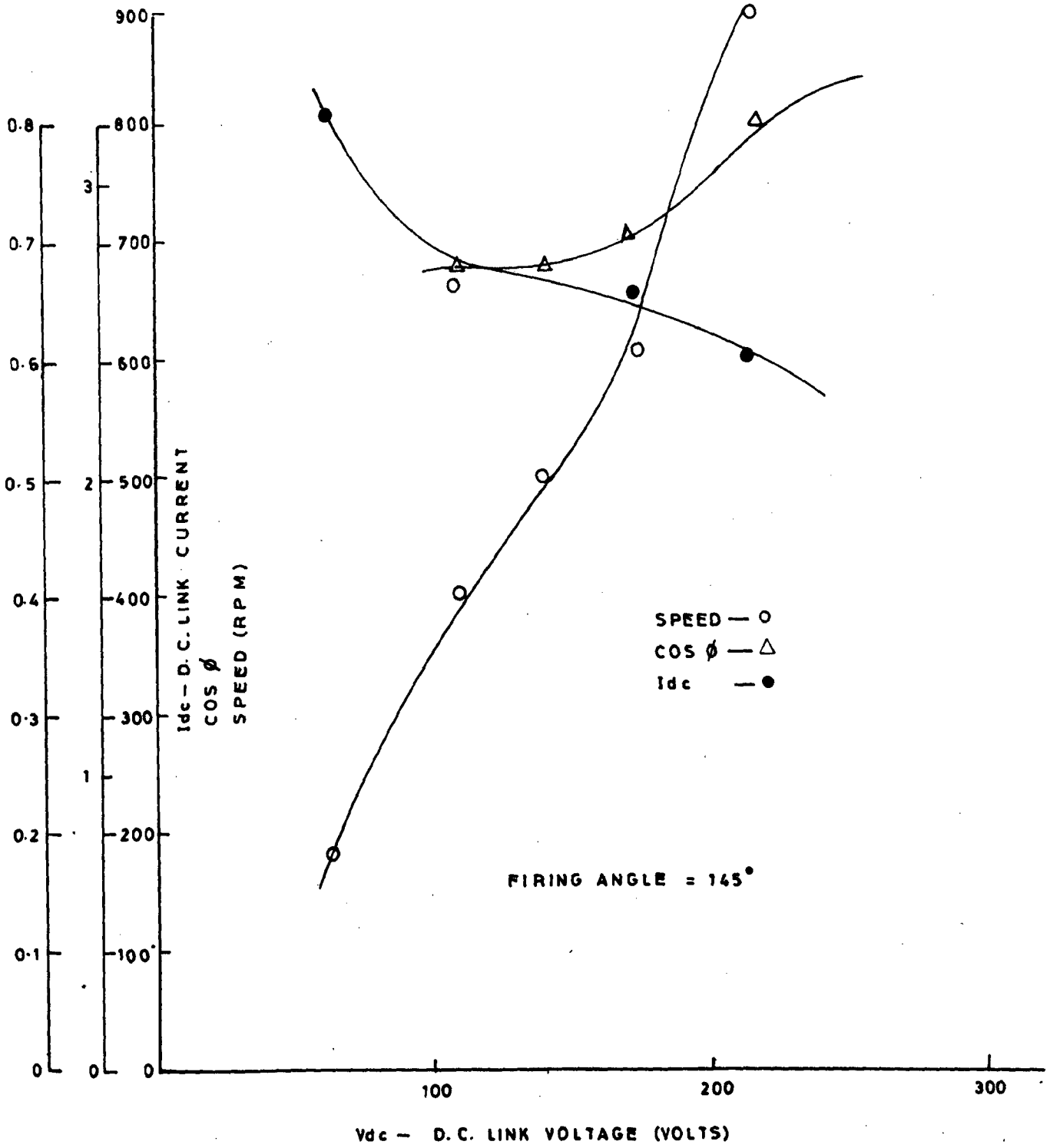


FIG. 4.10 VARIATION OF SYNCHRONOUS MOTOR SPEED, POWER FACTOR AND D.C. LINK CURRENT WITH D.C. LINK VOLTAGE Vdc AT If=8A AND $\alpha = 145^{\circ}$

produce same load torque the D.C. link current decreases by a small margin.

4.5.4 NO LOAD SPEED AND DC LINK VOLTAGE CHARACTERISTICS:

This part of no load tests were carried out by varying V_{dc} and keeping I_f and cos α constant. The speed and V_{dc} characteristics are as shown in Fig 4.10. The synchronous motor speed could be varied from maximum value of 900 RPM to a minimum value of 90 RPM by changing D.C. link voltage from 260 V to 60 V. Thus output frequency range from 46.5 Hz to 4.5 Hz has been obtained. The synchronous motor terminal voltage also changes proportionally from 330V to 40V. The V/f ratio is maintained almost constant through-out the entire range (i.e. an approximate value of 8). At speeds below 90 RPM commutation failure occurs. This is due to the fact that the back e.m.f. of synchronous motor is not sufficient for commutation of SCRs, 900 RPM is the upper maximum speed value above which commutation failure occurs. It can also been seen from the Fig 4.10 that the D.C. link current decreases with increase in speed. A slight improvement in power factor is also observed at increased speeds. Hence if LCI-synchronous motor system is to be used as a variable frequency source for induction motors then control of frequency can be most stably obtained by changing D.C. link voltage. At reduced frequency operations both V_{dc} and I_f control can be used to obtain stable operations. Control of firing angle for controlling frequency is inheritently

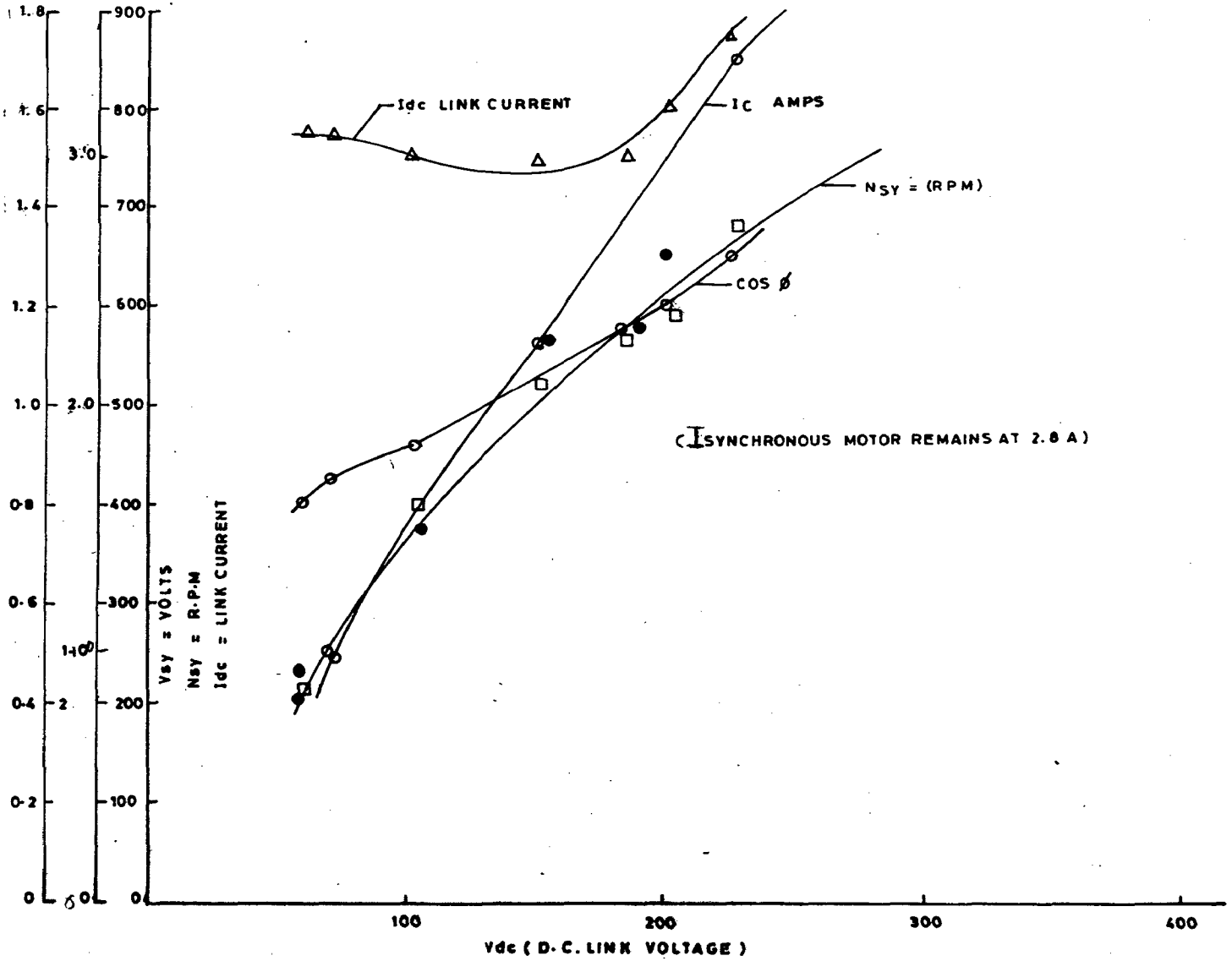


FIG. 4.14 NO LOAD SPEED IN RPM AND D.C. LINK VOLTAGES VOLTS CHARACTERISTICS AT CONSTANT I_f AND α

unstable. This can be implemented only for maintaining a constant safety margin angle[ ] i.e. $(\beta - \mu)$. The constant margin angle method involves the reduction of α proportionally with increase in μ to keep $(\beta - u)$ = constant

$$\beta = (\pi - \alpha) \quad \ldots \quad (4.19)$$

μ increases with D.C. link current or load current. Thus method of constant safety margin angle has got some seriously stability problems. Hence control of CLM is generally obtained by. V_{dc} control or I_f control.

4.5.5 NO LOAD SPEED AND V_{dc} CHARACTERISTIC WITH CAPACITOR BANK (Y-CONNECTED) IN PARALLEL OF SM:

No load speed versus D.C. link voltage characteristics is also obtained with a star connected Capacitor bank connected in parallel with the synchronous motor as shown in Fig 4.14.

Following important conclusions can be drawn from the Fig 4.14.

1. The range of speed obtained for same I_f and cos α and V_{dc} varying, is smaller than the range obtained with out capacitors for the same operating conditions.
2. At higher frequencies the capacitor delivers more reactive power than that is required by LCI hence, the synchronous motor operates at a lagging power factor to compensate for the exessive reactive power delivered by capacitors.

3. The power factor of synchronous motor becomes leading at lower speeds when the capacitive reactive power decreases.

4. Though connection of capacitor reduces the speed range obtainable at no load however, the capacitor are an attractive source of reactive power for full load conditions or when a large no of inductions motors are to be connected to the system.

4.5.6 DESCRIPTION OF PHOTOGRAPHS FOR NO LOAD CONDITIONS:

1. In the photograph 4 the terminal voltage of LCI is seen to be almost sinusoidal except for the six notches seen at a interval of 60^{o} in each cycle. These notches are due to the commutation overlap region. These notches produce high dv/dt accross SCRs. Hence while operating at higher voltages RC snubber circuits become inevitable. The notches can be reduced by reducing the commutation reactance $x_c = \frac{X''_d + X''_q}{2}$

2. The commutation overlap angle can be approximately estimated from the photograph no 10 giving an enlarged view of the overlap notch obtained in the terminal voltage of LCI.

3. The nature of D.C. link current for different values of D.C. link inductance are as shown in photographs numbered 17,18.

The D.C. link current in case of L_d = 12 mH is

pulsuating and almost reaches zero value at every 60^{o} interval. It has been verified experimentally that inductance of still lower value producesdiscontinous current in D.C. link and thus resulting in oscillations in the torque produced, leading to instability. Also it has been experimentally found that though large value inductances, having allarge time constant, give: stable operation for a no load D.C. link current of 2 Amperes however, it is not possible to increase the D.C. link current by loading the synchronous motor because commutation failure occurs. The nature of D.C. link current for this high value of D.C. link Inductance is shown in photograph no 18 , it is almost continuous.

The critical value of L_d = 12 mH has been experimentally found. This value allows a stable no load and full load operation with D.C. link current of upto 8 Amps.
Thus it is infered that the D.C. link inductance value, and time constant,play a decesive role in determining the stable operation of the system. No analytical expressions or treatment has yet been published, giving the effect of D.C. link inductance upon system performance and stability.

4. The synchronous motor current on no load is shown in photograph no 7 . It consists of two 60 pulses in positive half cycle and two in negative half cycle.

5. The reduction of commutation overlap angle is quite evident from the photograph 11 showing the terminal voltage of LCI with capacitors connected in parallel.

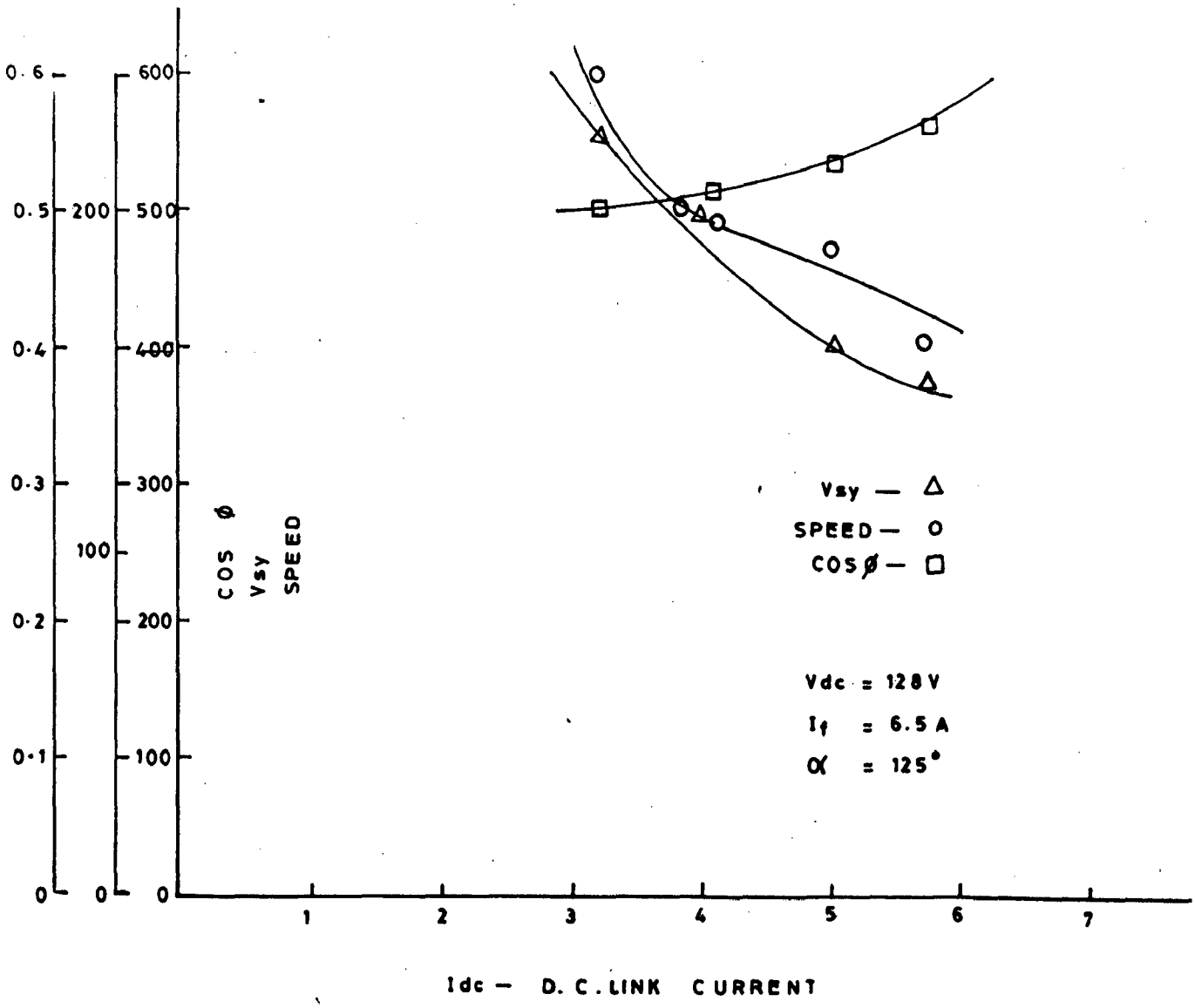


FIG. 4.11 VARIATION OF SYNCHRONOUS MOTOR SPEED, POWER FACTOR AND TERMINAL VOLTAGE WITH D.C. LINK CURRENT

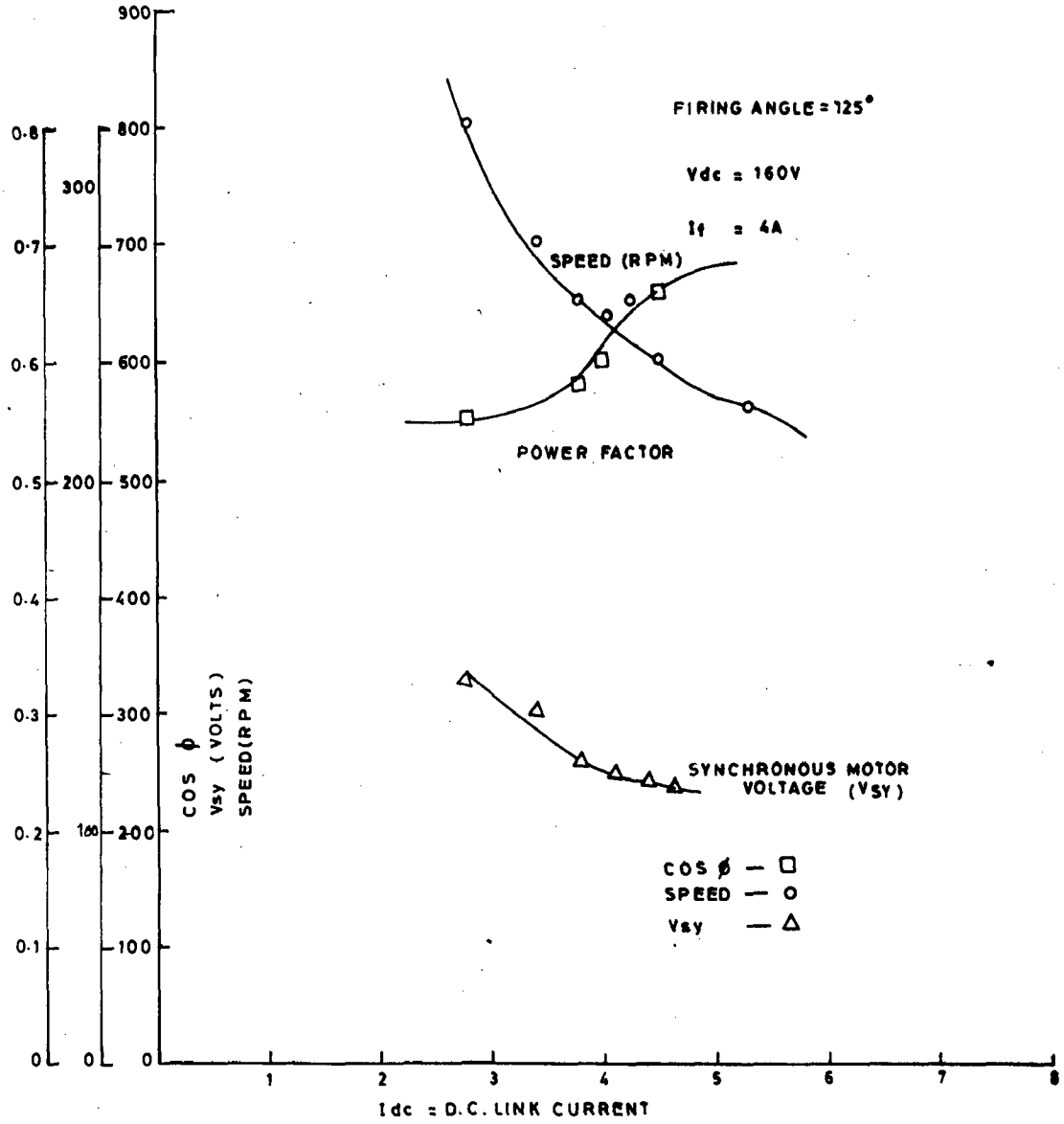


FIG. 4.12 VARIATION OF SYNCHRONOUS MOTOR POWER FACTOR, SPEED, AND TERMINAL VOLTAGE WITH D.C. LINK CURRENT

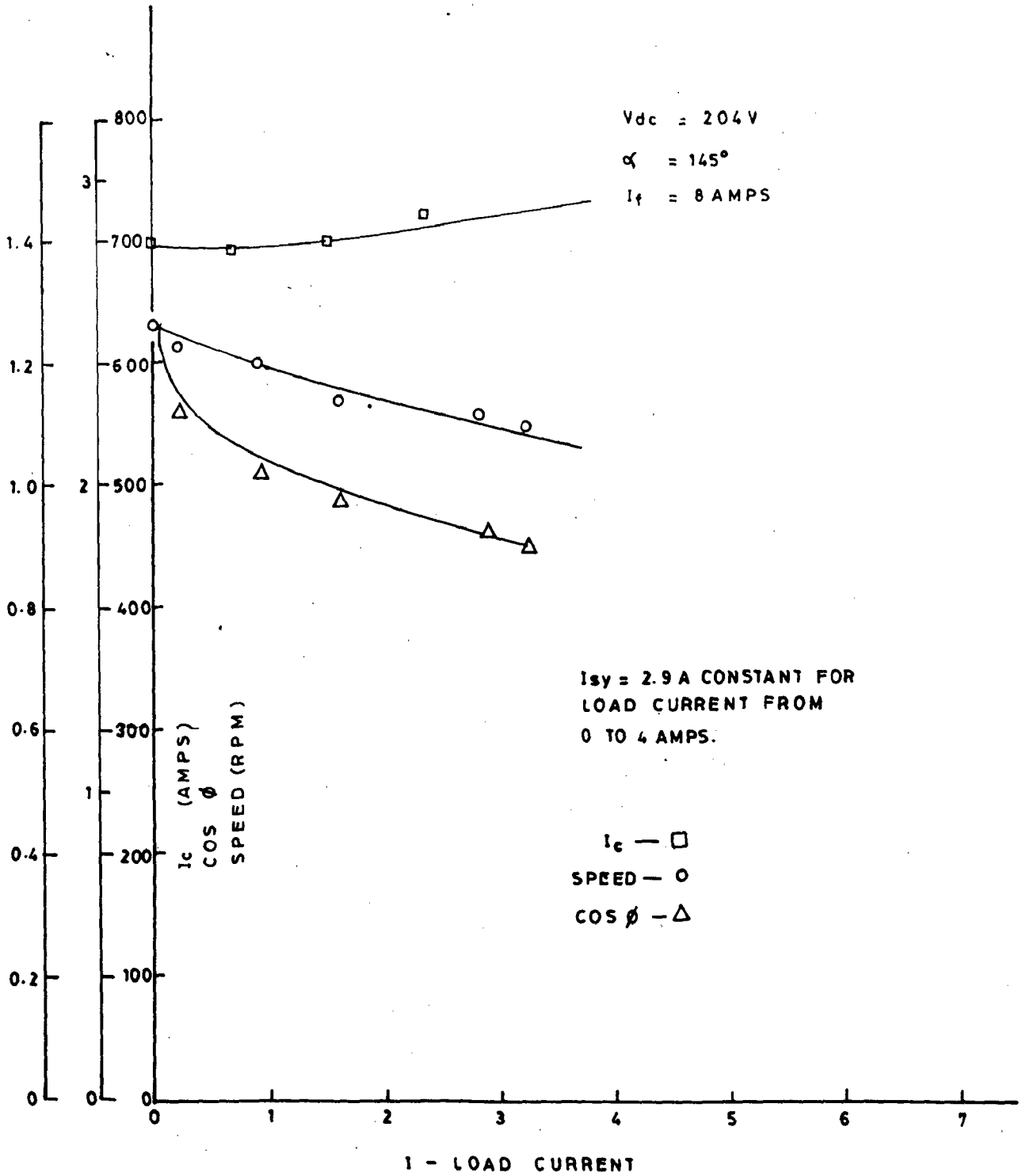


FIG. 4.13 LOAD CHARACTERISTICS OF CLM WITH CAPACITORS CONNECTED IN PARALLEL WITH SYNCHRONOUS MOTOR

4.5.7 LOAD TESTS OF CLM:

Two types of load tests were carried out on the CLM:

1. Without Y connected capacitor bank in parallel.
2. With Y connected capacitor bank in parallel.

From the two types of load tests carried out, a number of peculiar observations have been obtained:

1. The machine speed reduces drastically i.e. by about 30 to 50 RPM from the no load value, when some initial load is applied,
2. Further reductions in speed with increased load are comparatively smaller. The operating power factor of motor is also observed to be improving. This is due to the effect of increase of overlap angle μ, with load. The machine power factor is given by

$$\text{Cos } \beta' = \text{Cos } (\beta - \frac{\mu}{2}) \qquad \ldots \qquad (4.20)$$

The improvement in power factor of motor is responsible for the marginal speed reductions at higher loads.

3. The load characteristics of the commutatorless motor is same as that of seperately excited motor. Thus two control strategies can be adopted.
   i. Constant torque operation.
   ii. Constant horsepower operation.

(a) Constant torque operation mode is adopted for speeds lower than the rated speed. The field current and

the firing angle are maintained constant. The motor torque is controlled by D.C. link current.

(b) Constant horse power operation mode is adopted for speeds above the base speed value. The motor torque is varied by changing the field current and keeping V_{dc} and α constant. The characteristics obtained by varying the field current are constant horse power characteristics. The constant horse power mode of operation can also be achieved by suitably varying the firing angle α, but for the instability associated with this method of control.

(c) The CLM draws lagging current even under over excited state at high speeds and light loads with a Y connected capacitor bank in parallel. The lagging power (reactive power) compensates for the excessive capacitive KVAR supplied by the capacitor. With the increase in load the power factor changes from reactive to capacitive to supply the increased demand of reactive power of the line commutated inverter. Thus the capacitor connected in parallel can be used as an additional source of reactive power enabling the reduction in rating of synchronous motor required for a given load. Also adding capacitors to the system increases the rating of the system at a particular operating point.

(d) The addition of capacitors help in maintaining

the V/f ratio constant specially at reduced frequencies. The expression for the terminal voltage V of LCI without capacitor can be written as

$$V = E - j\, I_{sy}\, X_s f_r \qquad \ldots \qquad (4.21)$$

where I_{sy} is the current of the synchronous motor. The change in synchronous motor current is caused by the variation of the reactive power supplied by the synchronous machine to the LCI. Hence the reactive component is more than the active component at no load. The quadrature axis component of the armature reaction forms the major part of the synchronous reactance Voltage drop.

The terminal voltage V can be written for the case with capacitor as follows:

$$V = E - j\, I_{sy}(cap)\, X_s f_r \qquad \ldots \qquad (4.22)$$

where $I_{sy}(cap)$ is the synchronous machine current, when the capacitor is connected at the LCI terminals. The capacitor partially supplies the reactive power to the LCI. This reduces the reactive power supplied by the synchronous machine. The capacitor reduces the VAR component of machine current and compensates the quadrature axis component of the armature reaction. It also changes the power factor angle of synchronous machine.

The reactive power balance equation for LCI-SM-capacitor system is given as follows:

$$Q_{sy} + Q_{cap} = Q_{LCI} \qquad \ldots \qquad (4.23)$$

i.e.

$$3V\, I_{sy}(cap)\sin\beta' + 3V^2wC = 3VI_{LCI}\sin\beta \qquad \ldots \quad (4.24)$$

from the above equation it is clear that the addition of capacitor reduces synchronous motor rating.

(e) The photograph number 11 shows the LCI terminal voltage with reduced notches obtained with a star connected capacitor bank connected at its ouput terminals. The reduced notch widths signify the reduced overlap angle as compared to the case without capacitor bank and at same operating conditions. The decrease in over lap angle can be proved analytically as follows:

The relationship between the angles β, μ, δ, I_{dc} and X_c is given by

$$\cos(\beta - \mu) = \cos\beta + \sqrt{\frac{2}{3}}\,\frac{I_{dc}\,X_c}{E} \qquad \ldots \quad (4.25)$$

Without capacitor, the effective reactance during commutation period is the negative sequence reactance. However, with the addition of the capacitor, the value of X_c is modified to $\dfrac{-jX_c\,X_{cap}}{(X_{cap} - X_c)}$ where $X_{cap} = \dfrac{1}{wC}$ hence from equation 4.25 it is seen that the capacitive reactance reduces the over lap angle and increases the commutation margin angle.

CONCLUSIONS

The study of steady state performance characteristics of LCI-SM system under no load and loaded conditions shows that it works satisfactorily as a variable speed drive popularly known as the CLM. It is found that the torque of the synchronous machine is dependent on, (i) D.C. link current, (ii) commutation lead angle, and (iii) field current. similarly the speed of the synchronous machine can be controlled by varying:

(1) The D.C. link voltage, V_{dc},

(2) The commutation lead angle, (β),

(3) Field current, I_f.

It is practically observed that adjustment of the D.C. input voltage to LCI, results in a precise control of its speed upto the maximum value while the control of either the field current or the commutation lead angle provides only a limited speed variation. The effect of D.C. link inductor value upon system performance and nature of D.C. link current is practically verified and photographs of D.C. link current for different values of inductance are given. The non availability of any analytical expresion or relation giving optimum value of inductance for D.C. link is remarked. The advantages of connecting a capacitor network in parallel with CLM are also studied.

Finally it is felt that the system is feasible for being used as a variable frequency source with constant V/f for multi induction motor drives.

CHAPTER V

STEADY STATE PERFORMANCE OF LCI-SYNCHRONOUS MACHINE - INDUCTION MOTOR SYSTEM

5.1 GENERAL:

In this chapter, the steady-state performance of LCI- synchronous machine - induction motor system has been studied experimentally. An attempt has also been made to explain and correlate the experimental results with the computed steady state performance as obtained from equations derived by Ranganadhachari[29]for the LCI-SM-IM model. In order to simplify the understanding of system, the equivalent circuit model given by Rangnadhachari[29] has also been given.

Experiments were carried out on LCI-SM-Induction motor system to verify the feasibility of LCI-SM as a variable frequency source for induction motor drive. The method of determining the active and reactive powers of synchronous motor, LCI and induction motor practically, is also explained.

5.2 DEVELOPMENT OF ANALYTICAL MODEL

The schematic diagram of the system is shown in Fig 5.1. The LCI-synchronous motor combination is used as a variable frequency source for induction motor. The equivalent circuit of induction motor is added to the equivalent circuits of LCI-SM system developed earlier.

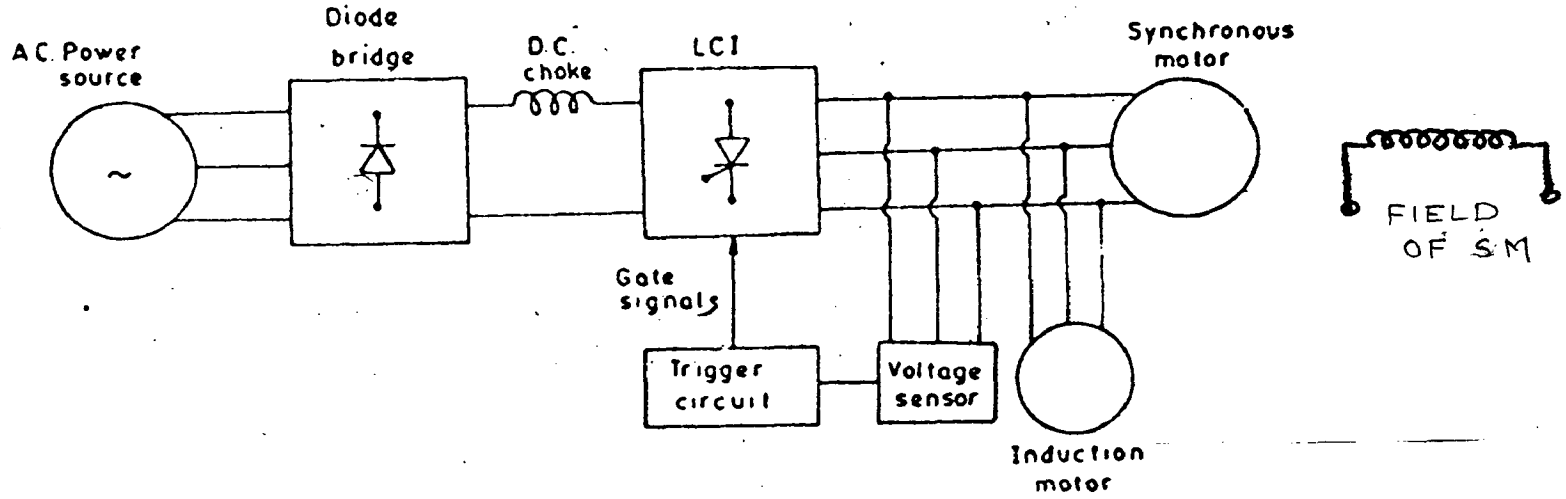
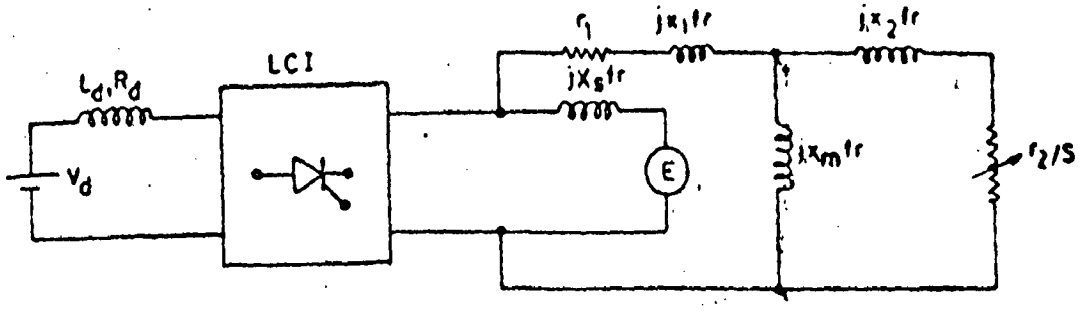
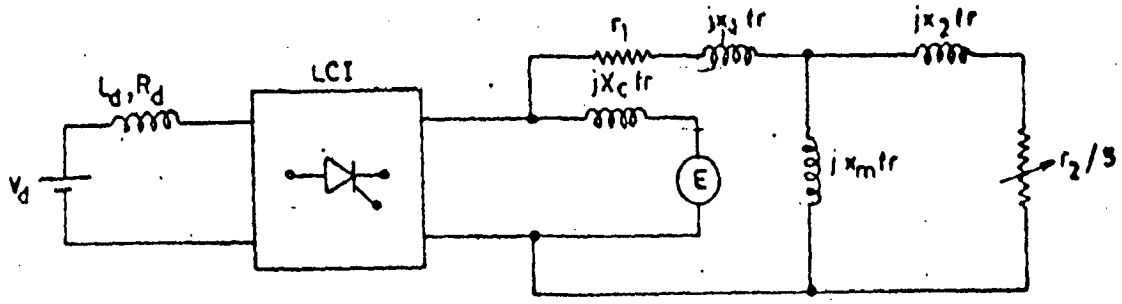


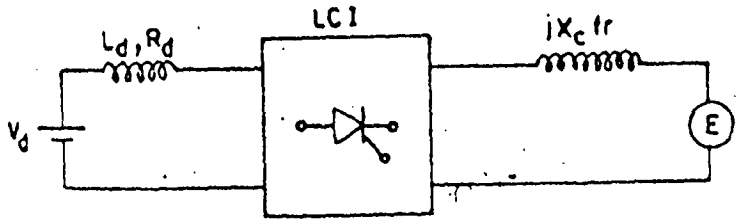
Fig 5.1 Schematic diagram for LCI-SM induction motor system



(a) Conducting period

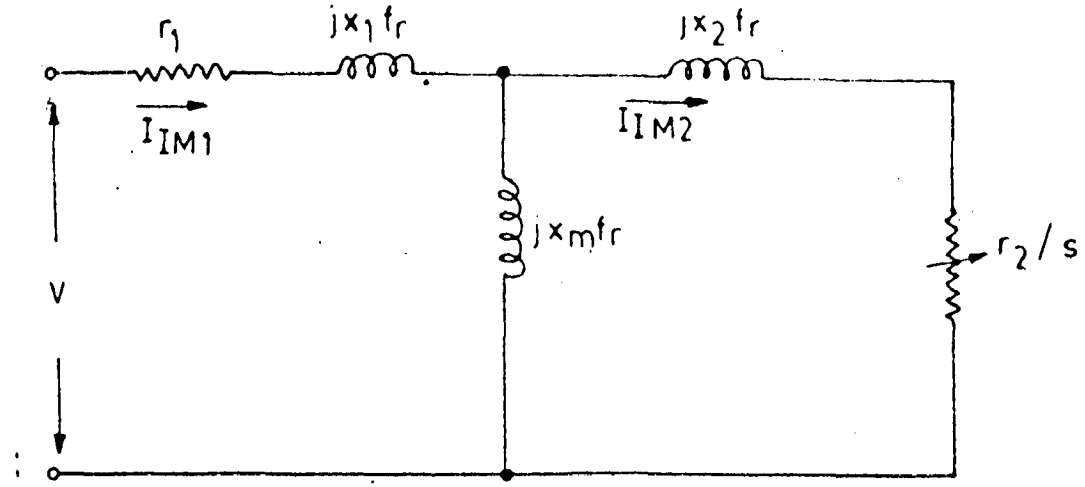


(b) Commutation period



(c) Simplified representation for commutation period

Fig 5.2 Equivalent circuit diagrams of the LCI-SM- induction motor system



Equivalent circuit of the Induction Motor

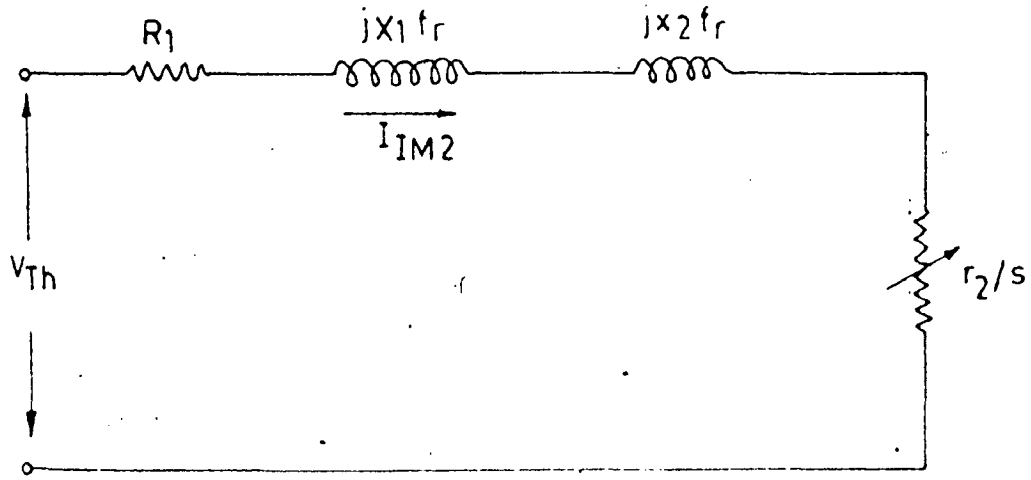


Fig 5.3 (b) Thevenins equivalent circuit

Thus the equivalent circuits for the system for conduction and commutation modes are as shown in Fig 5.2. The D.C. voltage drop due to the reactances of induction motor during commutation period is neglected in analysis as X_c which has a small value comes in parallel with these reactances during the commutation period. Thus the simplified equivalent circuit of the system is as shown in Fig 5.2(c). The performance equations of the induction motor along with the performance equations interlinking the operation of the LCI, synchronous machine, and induction motor are obtained in the following section.

5.3 DERIVATION OF STEADY STATE EQUATIONS OF THE SYSTEM: ASSUMPTIONS:

The LCI output voltage is more or less sinusoidal because of the presence of back emf of the synchronous machine.

Following simplifying assumptions have been made in the analysis:

1. The commutation lead angle β of the LCI is assumed to be constant.
2. The assumptions that have been made in case of LCI-SM system are also applicable in this case.

5.3.1 PERFORMANCE EQUATION OF INDUCTION MOTOR:

The equivalent circuit of induction motor when operating from given LCI-SM system is as shown in the Fig.5.3.

The reactance values are shown at the base frequency f_o and f_r is the ratio of operating frequency f_1 to base frequency f_o. In addition to the assumptions listed earlier, the following assumptions are also made for the performance equations of induction motors.

1. The stator and rotor windings are identical and distributed sinusoidally. These windings are represented by equivalent lumped parameters.

2. The parameters of winding represent the actual values of steady state . hot conditions.

3. The iron loss component, friction and windage losses are neglected.

Thevenins' transformation of the equivalent circuit is as shown in the Fig 5.3 where,

$$V_{Th} = \frac{V\, x_m f_r}{[r_1^2 + (x_1+x_2)^2 f_r^2]^{1/2}} \quad \ldots \quad (5.1)$$

$$R_1 = \frac{f_r^2\, x_m^2\, r_1}{[r_1^2 + f_r^2\,(x_1 + x_m)^2]} \quad \ldots \quad (5.2)$$

and

$$X_1 = x_m \frac{r_1^2 + f_r^2\, x_1 (x_1 + x_m)}{[r_1^2 + f_r^2\,(x_1 + x_m)^2]} \quad \ldots \quad (5.3)$$

where

V = applied voltage

r_1 = stator resistance per phase

x_1 = stator leakage reactance per phase

x_2 = rotor leakage reactance

x_m = magnetising reactance.

Since in all induction motor designs $r_1 < (x_1 + x_m)$ and f_r is usually not lower than 0.1 in practical variable frequency schemes, V_{TH}, R_1, X_1 could be approximated to CV, $C^2 r_1$, $C.X_1$, without much error, where $C = (\frac{x_m}{x_1 + x_m})$ is a fraction approaching unity.

The basic equations applicable to induction motors when connected to the LCI-SM source with V volts/phase frequency f_1 and operating at a fractional slip S are given by.

The stator current

$$I_{1M} = \frac{CV[(\frac{r_2}{S})^2 + (x_2 + x_m)^2 f_r^2]^{1/2}}{X_m f_r[(R_1 + \frac{r_2}{S})^2 + (X_1 + x_2)^2 f_r^2]^{1/2}} \quad \ldots (5.4)$$

The rotor current

$$I_{IM_2} = \frac{CV}{[(R_1 + \frac{r_2}{S})^2 + (X_1 + x_2)^2 f_r^2]^{1/2}} \quad \ldots (5.5)$$

the electromagnetic torque

$$T_{IM} = (\frac{3}{f_r w_o}) \frac{C^2 V^2 r_2/S}{[(R_1 + r_2/S)^2 + (X_1 + x_2)^2 f_r^2]} \quad \ldots (5.6)$$

Internal power

$$P_{IM} = \frac{3C^2V^2 \frac{r_2}{S}(1-S)}{[(R_1 + r^2/S)^2 + (X_1 + x_2)^2 f_r^2]} \quad \ldots \quad (5.7)$$

5.4 PERFORMANCE EQUATIONS INTERFACING THE OPERATION OF THE LCI-SYNCHRONOUS MACHINE AND THE INDUCTION MOTOR:

The calculations of active and reactive power flow in the system can be done as:

The induction motor active and reactive powers are given by,

$$P_{IM} = 3\ VI_{1M} \cos \theta \quad \ldots \quad (5.8)$$

$$Q_{IM} = 3\ VI_{1.M} \sin \theta \quad \ldots \quad (5.9)$$

The phase angle of LCI is almost equal to its lead angle of commutation. In LCI-SM-induction motor system the D.C. source supplies active power to the induction and synchronous machine. While the reactive power to the LCI is supplied by the synchronous machine. Considering the above aspects, the following equations are written:

$$I_{LCI} \cos \beta = I_{SY} \cos \beta + I_{1M} \cos \theta \quad \ldots \quad (5.10)$$

$$I_{LCI} \sin \beta = I_{SY} \sin \beta - I_{1M} \sin \theta \quad \ldots \quad (5.11)$$

where β' is the power factor angle of synchronous machine.

5.5 EXPERIMENTAL SET UP

The detailed layout for the experimental setup

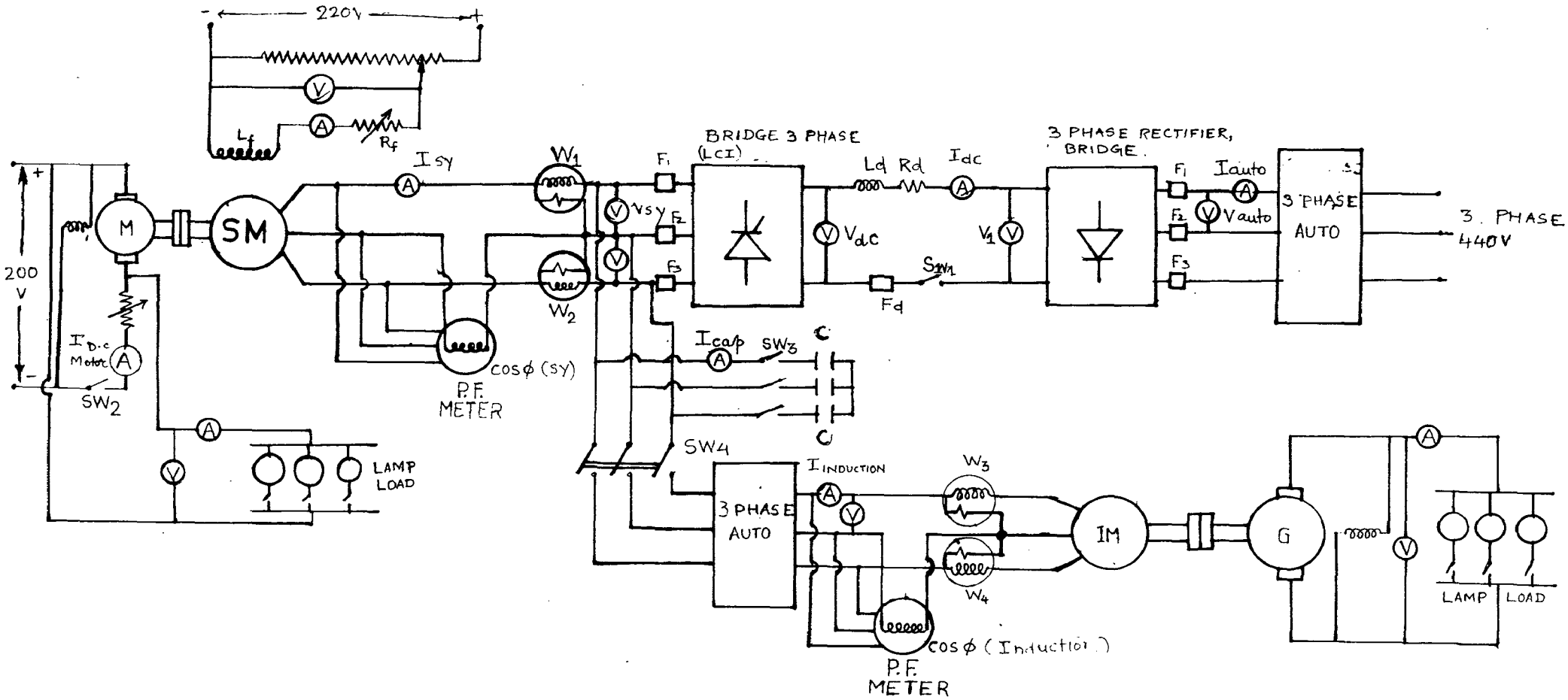


FIG 5.4. COMPLETE SYSTEM CIRCUIT DIAGRAM
LCI- SM - INDUCTION MOTOR SYSTEM

including the instrumentation is shown in Fig.5.4. From the Fig 5.4, it is clear that the induction motor is connected to the output of LCI through an auto transformer. The reason for connecting the auto transformer is given in the next section. The induction motor shaft is coupled with a D.C. generator. This generator is used to load the induction motor. The experimental investigations are carried out on the LCI-SM-induction motor system in two parts.

1. no load test of induction motor with and without capacitor.
2. Load tests of induction motor with and without capacitor.

The no load tests are carried out on the 3HP induction machine the ratings of which are given in Appendix I . The load tests are carried out on 3 phase 1/2 HP induction motor again the ratings of this motor generator set are given in Appendix I .

5.5.1 STARTING METHOD FOR THE LCI-SM-INDUCTION MOTOR SYSTEM

The LCI-SM system is started by adopting the same procedure as described in chapter 4. When the LCI-SM system reaches steady state speed. The speed of the synchronous machine is so adjusted as to obtain the starting frequency and voltage of induction motor. Normally the induction motor is started at low frequency with a reduced v/f ratio. The induction motor is started using the autotransformer. This procedure is adopted to avoid the starting current in rush of

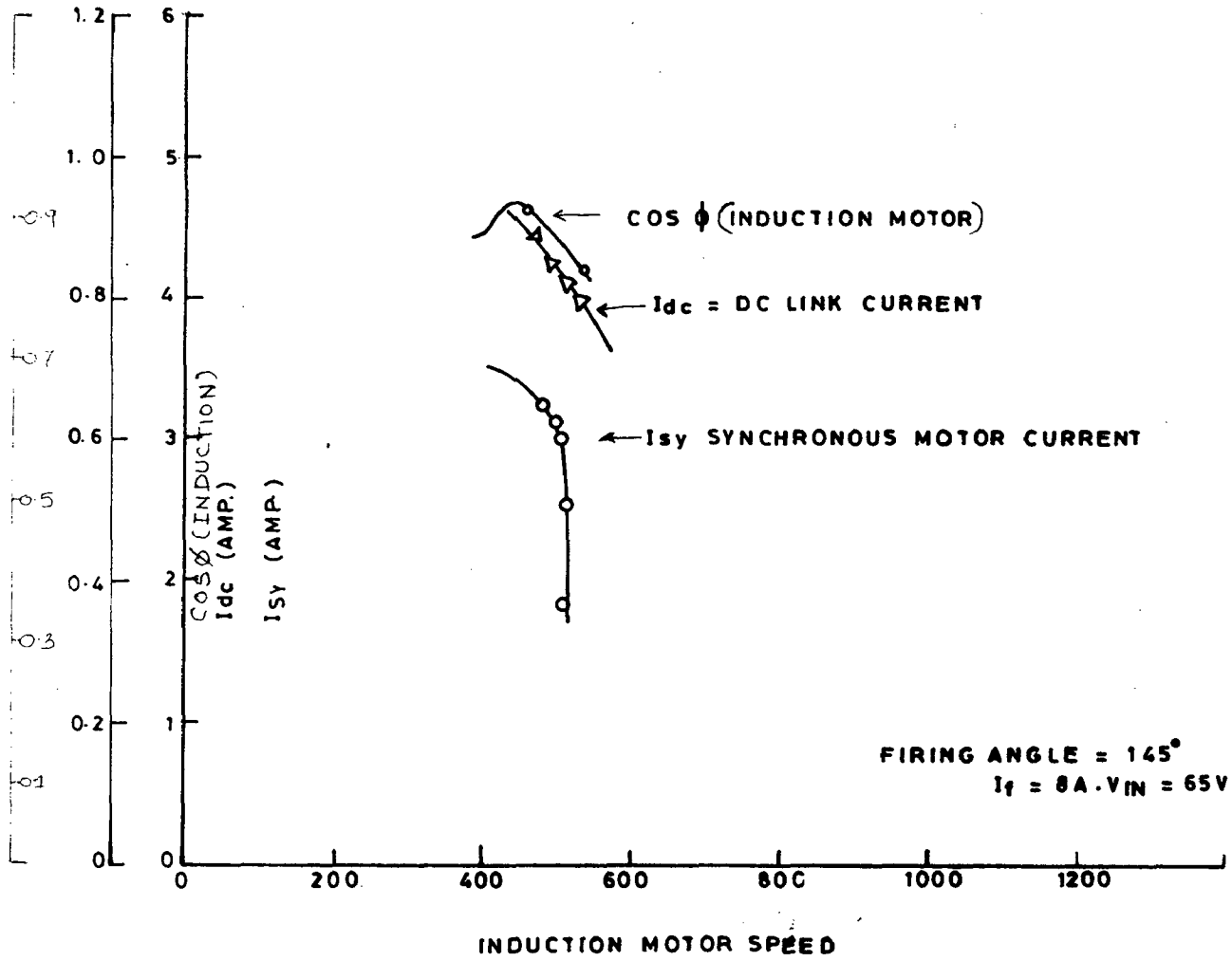


FIG. 5.5 LOAD CHARACTERISTICS OF INDUCTION MOTOR WITHOUT CAPACITOR IN PARALLEL OF LCI

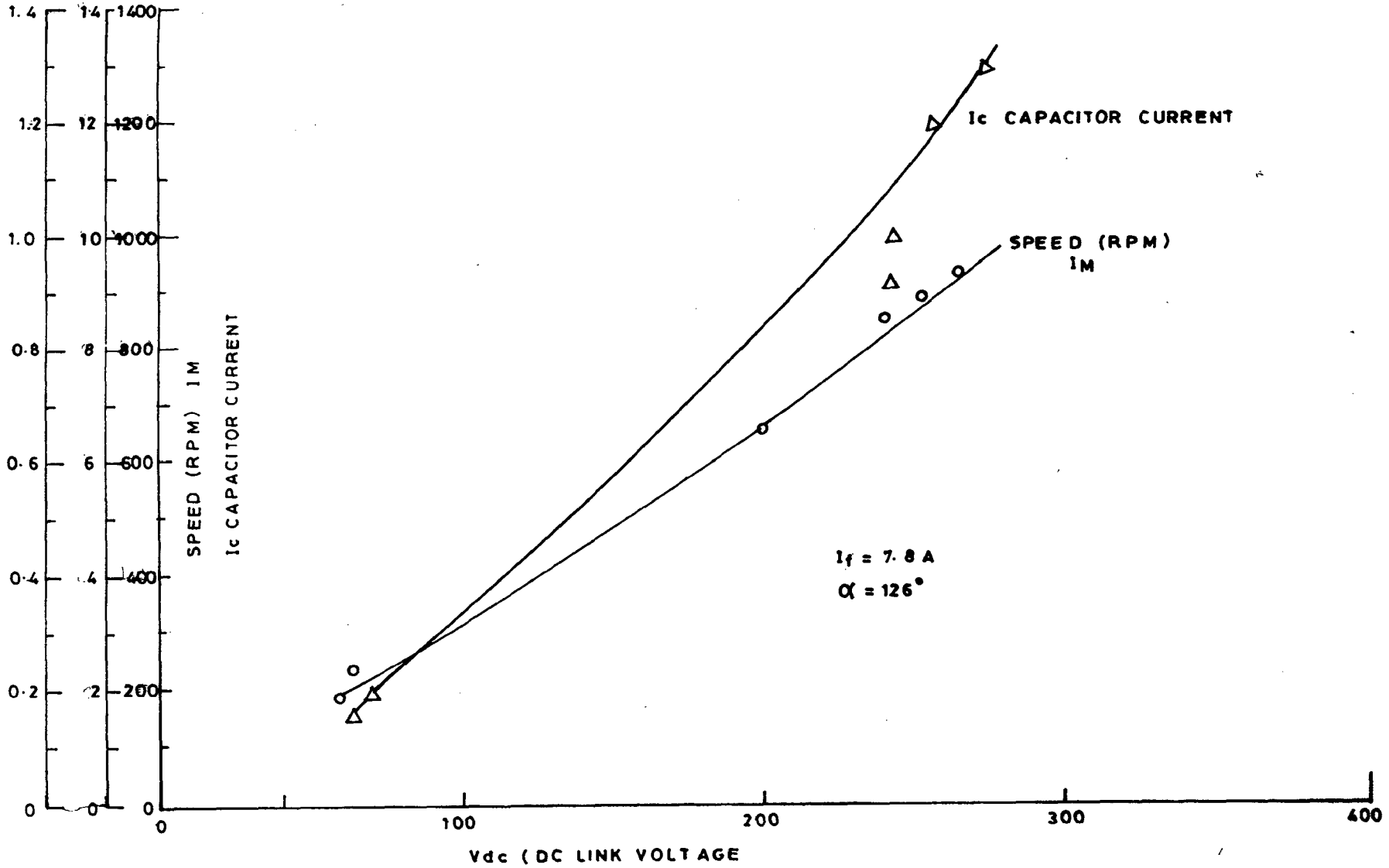


FIG. 5.6 NO LOAD SPEED OF INDUCTION MOTOR, CAPACITOR CURRENT VS V_{dc} AT CONSTANT I_f AND α.

induction motor. This starting current can cause instability to the LCI-SM system. The voltage accross the induction motor is gradually increased with the autotransformer, till the rated voltage is obtained.

5.6 RESULTS AND DISCUSSIONS

The no load speed control of induction motor has been studied. The speed versus D.C. link voltage characteristics for a 3 HP induction motor is as given in Fig 5.6. In this experiment the Y connected capacitor bank is put in parallel with the synchronous motor. A speed variation of 800 RPM is obtained i.e. the speed changes from 900 RPM to 90 RPM. The capacitor current increases from a value of 2A at 190 RPM to 13 A at 920RPM. The synchronous machine power factor is leading and improves with increase in speed. Thus it is verified that the a LCI-SM system can be used as a source of variable frequency for induction motors.

5.6.1 LOAD TEST OF INDUCTION MOTOR:

The load tests were carried out on 1/2 HP induction motor D.C. generator set to obtain following characteristics -

5.6.2 STATOR CURRENT-SPEED CHARACTERISTIC:

The stator current speed characteristics of induction motor is as shown in Fig 5.5. It is observed that stator current increases with the decrease in speed.

5.6.3 POWERFACTOR-SPEED CHARACTERISTICS

Fig.5.5 shows the variation of the power factor of induction motor with the speed. From these curves it can be seen that the power factor of induction motors improves as the motor speed decreases from its no load speed value.

5.6.4 BALANCE OF ACTIVE AND REACTIVE POWER OF THE SYSTEM:

From the experimental investigations carried out on CLM-induction motor system, it is evident that the active power supplied by LCI increases with decrease in the speed of the induction motor. As the load on the induction motor increases, there is an increase in active power with the decrease in the speed of induction motor. The change in active power of LCI depends only on the load of induction motor as the active power drawn by synchronous motor is small. It is also observed that the reactive power supplied by the synchronous motor equals the sum of reactive power of the induction motor and LCI. The VAR change of the induction motor is small when compared with the VAR change of LCI. The VAR change of the induction motor is small due to the power factor improvement with decrease in speed and increase in load. The change in VAR of the LCI is high because of the corresponding increase in current component of LCI. Hence the reactive power supplied by the synchronous machine increases with the decrease in speed of induction motors with increase in load.

5.6.5 DESCRIPTION OF OSCILLOGRAPHS

The photograph no 11 shows the terminal voltage of the induction motor. It can be seen that it is essentially sinusoidal under all conditions with small notches spaced at 60^{o} interval occuring due to the commutation of the SCRs of LCI. The duration of the notch is equal to the over lap angle and is quite small. The voltage waveform can thus be assumed to be sinusoidal.

The induction motor current is shown in photograph no 14 . It is clear that the current waveforms are not exactly sinusoidal. This discrepancy is due to the way the current is supplied to the induction motor Whenever an SCR of phase B (say phase B) is conducting the LCI supplies the phase currents of both the induction and synchronous motor. When the phase B is off the current to the induction motor phase is supplied by the synchronous machine. Since the internal source impedance of the synchronous machine is large compared to the LCI, the induction motor current is not a sine wave. Thus, the voltage and current waveforms in this scheme are nearly sinusoidal and relatively free from harmonics unlike the force commutated inverter.

The synchronous motor current is shown in the photograph no 13 . A peculiar feature of this current waveform is, the two sixty degree pulses in positive and negative half cycle drawn by the synchronous motor without any induction motor connected in parallel with it, are still

seen but are now superimposed on a sinewave. This is due to the fact that the synchronous motor is supplying current to induction motor when individual phase SCRs of LCI are not conducting.

The capacitor current waveform is as shown in the photograph no 16 .

5.7 CONCLUSIONS:

The LCI-synchronous machine combination meets the basic requirements of a variable frequency source and provides effectively the variable speed operation of induction motor. The capacitor network connected in parallel with the synchronous machine add stability to the system. They maintain v/f ratio constant also at reduced frequency operation.

CHAPTER VI

CONCLUSION

6.1 GENERAL:

The work presented in this thesis covers the design and fabrication of a microcomputer based firing scheme for LCI, experimental investigations on steady state performance of LCI-SM system, and feasibility of LCI-SM system as a variable frequency source for induction motor drives.

6.2 MICROCOMPUTER BASED FIRING SCHEME:

An open loop firing angle control scheme has been developed. A remarkable improvement in performance of the system in terms of stability and reliability of firing pulses is obtained by adopting the microcomputer based firing scheme. The software based scheme provides added flexibility in terms of accurate firing angle setting.

The voltage controlled oscillator used in the firing scheme spares the microcomputer from the task of computation of frequency of LCI output voltage in every cycle. Though it enables obtaining a constant firing angle at variable frequency with a single delay word, The change in excitation of synchronous machine may cause a minor error in firing angle value. This error can be taken care of through software by sensing the field current of synchronous machine and making a proportionate change in the delay word depending upon magnitude of field current.

6.3 STEADY STATE PERFORMANCE OF LCI-SM SYSTEM:

The study of steady state characteristics of LCI-SM system has shown that it works satisfactorily as variable speed drive popularly known as the D.C. commutatorless motor. Some vital observations based upon the experiments carried out on the LCI-SM system are:

1. It is found that the torque of the synchronous machine depends upon (i) the D.C. link current (ii) the commutation lead angle (iii) field current.

2. It is observed that the variation of D.C. link voltage V_{dc} results in precise control of speed of commutatorless motor. A speed variation from 10 % to 95 % of rated speed has been practically obtained through the control of D.C. link voltage. The control of D.C. link voltage gives a constant torque operation.

3. The field current and commutation lead angle provide only limited speed variation.

4. A constant horse power mode of operation is obtained by controlling the speed by varying the field current. Only the speed above the base speed can be obtained. The range of speed obtainable by field excitation control is also found to be a function of D.C. link voltage and the commutation lead angle. Improvement in power factor of synchronous machine is obtained with reduction in field current.

5. The value of D.C. link inductor and the D.C. link time constant have a significant effect on system performance and nature of D.C. link current. A large value of inductance does not allow the D.C. link current to increase above a maximum value or else commutation failure occurs. The nature of D.C. link current was found to be continuous when the inductance value is large. The system performed well with such a value of inductance which gives pulsuating and discontinuous D.C. link current.

6. The terminal voltage output of LCI is almost sinusoidal except for the six notches corresponding to the six commutation overlap regions. A constant V/f ratio is maintained except for the drop accross the commutating inductance X_c. This drop is a function of the load current and also leads to commutation failures at full loads. The commutation overlap angle can be reduced by addition of damper windings.

7. Various firing angle control scheme can be realised to maintain one or the other performance parameters constant, these are:

(a) Safety margin angle δ = constant: Control can be implemented to maintain δ at a minimum safe value compatible with the given thyristor. With this type of operation the machine will give the highest possible power factor and yield the highest possible power with the given current. This control scheme results in the

most efficient use of the synchronous machine.

(b) β=constant: This scheme of firing angle control keeps the commutation lead angle constant at a value such that the resultant δ turn off angle is in the safe minimum level when machine is delivering maximum power, then the turn off angle at lighter loads will be large and will fall in safe region.

(c) V_{dc}/E = constant: The firing angle control scheme is based upon the principle of maintaining V_{dc}/E at constant value. Where E is the no load terminal voltage of synchronous machine. The relationship between V_{dc}/E ratio and supplementary displacement angle γ i.e. the angle between the current and back emf of synchronous machine is given by the relation

$$\frac{V_{dc}}{E} = \frac{3\sqrt{6}}{\pi} \cos \gamma$$

This relation is valid for the cylindrical rotor machines only. It can be seen that the value of γ remains constant regardless of the motor current.

6.4 STEADY STATE PERFORMANCE OF LCI-SM-INDUCTION MOTOR SYSTEM

The experimental investigations on LCI-SM fed induction motors have shown that the induction motor works satisfactorily in the variable speed mode when fed from the LCI-SM based variable frequency source.

In the LCI-SM-Induction motor system, the synchronous machine works as a capacitor, i.e. a motor with out any mechanical load and supplies reactive power to the LCI and induction motor. The D.C. source supplies through the LCI the active power to the induction motor and the synchronous machine. The voltage and current of induction motor are found to be nearly sinusoidal. The commutation being natural, high instanteneous currents and steep rise in voltages which are common in case of forced commutated inverter circuits do not occur in this case. Thus low speed converter grade SCR's can be used.

6.5 EFFECT OF CAPACITOR ON SYSTEM PERFORMANCE:

The observations obtained after extensive tests carried out on the LCI-SM-IM system with capacitor bank in parallel show that the addition of capacitors helps in keeping the V/f ratio constant. The KVAR rating of the synchronous machine is also reduced. The commutation limit of LCI-SM-system is also improved.

6.6 SCOPE OF FURTHER WORK

The objectives set forth at the outset of this thesis have been successfully realised within the limited time available. The implementation of microcomputer control can overcome the drawbacks of the system and can popularise this system as a variable speed drive in industry. Various drawbacks such as inability of the system to start from standstill by itself and cummutation failures can be easily taken care of by

the microcomputer control. A precise balance of reactive power of LCI-SM-IM depending upon the load of induction motors can be realised through computerized control. The LCI-SM system in present investigation has been used as a variable frequency source to drive the induction motors for variable speed operation. There is a possibility of using this scheme in power system applicationsespecially in D.C. distribution systems. This possibility needs further investigation. An attempt can also be made to examine the possibility of modifying the design of synchronous motor with a view to improve the cost benefit ratio. The regenerative aspect of induction motor operation can also be studied.

APPENDIX-I

RATINGS OF MOTOR USED FOR EXPERIMENTAL WORK

Induction Motor 1

3ϕ, 220V, 1/2 HP, 1500 RPM

2.1 Amps, No Load Current = 1.5A.

Induction Motor 2

2.2 KW, 3HP, 4.5 Amps, 1430 RPM

Kirloskar Electric Company,

Rating-CR, 415V, Δ connected

D.C. Generator

Kirloskar Electric Company

1.5 KW, 1460 RPM, 220V, 6.9 Amps.

Compound., B Class, Exc Volt = 220V

R_{X-XX} = 305 Ohm, R_{Y-YY} = 0.3 Ohm, R_{H-HH}= 1.0 Ohm

Synchronous Motor Rating

Electromotoren Werke Kaiser, Berlin

3Ph,Y, 400V, 10.8A,7.5 KVA, cosϕ=0.8

1500 RPM, 50 Hz, Exc Volt = 40V, 8A.

Capacitor Rating

Capacity = 5KVAR,

50 Hz, 415V, 12.1 Amps. Single Phase.

D.C. Motor

220V, 8KW, 42A, 1500 RPM,

Induction motor -3

Kirloskar Electric Company

415V, 50 Hz, 4.9A, 2.2 KW, 1000 RPM.

APPENDIX II

Pin No.	Description	Pin No.	Description
1	PA3	23.	PCO
2.	PA4	24	PC1
3.	Not used.	25.	VCC.
4.	RST 7.5	26.	PC2
5.	Not used.	27.	PB7
6.	SOD	28.	PC3
7.	PA2	29.	PB6
8.	PA5	30.	PB5
9.	PA1	31.	PB0
10.	PA6	32.	PB1
11.	PA0	33.	PB2
12.	PA7	34.	PB4
13.	Not used	35.	PC6
14.	Not used	36.	PB3
15.	Not used	37.	PC7
16.	Not used	38.	RST 6.5
17.	Not used	39.	Not used.
18.	Not used	40	Not used.
19.	Not used	41.	Not used.
20.	SID	42.	Not used.
21.	PC5	43.	Not used.
22.	PC4	44.	RST 5.5

Pin assignment of the 44 pin edge connector on the VCP-85 card.

APPENDIX-III

FUNCTION NAME : LCI-SM MONITOR PROGRAM

INPUT : RAM MEMORY LOCATIONS

INPUT : CF00 TO CF78, D000 TO D012, D503 TO D504
D530 TO D613

OUTPUT : MEMORY LOCATIONS ADDRESS D501 TO D502, D505 TO D508

CALLS : SWO, PCGR, CMIP, CMPCH

DESTROYS : ALL

DESCRIPTION : THE LCI-SM MONITOR WIPES OUT THE ENTIRE SCREEN AND THEN DISPLAYS THE PROMT CHARACTER ON SCREEN. IF VALID COMMAND (4 CHARACTERED) FOLLOWED BY CR IS GIVEN THEN THE MONITOR BRANCHES TO FUNCTIONAL COMMAND ROUTINE OR ELSE FLASHES ERROR CALL HELP WAITS FOR ANOTHER COMMAND AFTER THAT

LEBEL	ADDRESS	CONTENTS	MNEMONICS AND OPERANDS	COMMENTS
LCI-SM	COE1	CD 95 CO	CALL SWO	WIPES OUT CRT SCREEN
	COE4	CD 80 CO	CALL PCGR	OUTPUTS * ON CONSOLE
	COE7	CD A7 CO	CALL EMIP	TAKES 4 CHARACTERED FUNCTION COMMAND FROM CRT
	COEA	C3 FA CO	JMP CMPCH	COMPARES THE INPUT COMMAND WITH COMMANDS IN THE COMMAND TABLE

FUNCTION NAME : SWO

INPUT : MEMORY LOCATIONS D54C TO D54F

OUTPUT : NONE

CALLS : CO, DELAY

DESTROYS : A,B,C,H,L

DESCRIPTION : THIS ROUTINE WIPES OUT THE ENTIRE CRT SCREEN
THE CURSER RETURNS TO THE HOME POSITION ON
THE SCREEN

LEBEL	ADDRESS	CONTENTS	MNEMONICS AND OPERANDS	COMMENTS
	C095	21 4C D5	LXI H,D54C	SET P_E AS POINTER FOR ESC
	C098	06 04	MVI B,04	COMMAND CHARACTER CODES
				N- NO OF CHARACTER
LO	C09A	4E	MOV C,M	OUT PUT THE CHARACTER POINTED
	C09B	CD 87 81	CALL CO	BY PE TO CRT
	C09E	23	INX H	$P_E \leftarrow P_E+1$
	C09F	05	DCR B	$N \leftarrow N-1$
	C0A0	CA EE C0	JZ COEE	IFN = 0
	C0A3	C3 EE C0	JMP Lo	
	C0A6			
	COEE	11 00 80	LXI D 8000	WAIT TILL THE SCREEN IS
	COF2	CD C0 81	CALL DELAY	WIPED OUT AND THEN RETURN
	COF5	C9	RET	

FUNCTION NAME : PCGR

INPUT : NONE

OUTPUT : NONE

CALLS : CO (CHARACTER OUT)

DESTROYS : A,B,C

DESCRIPTION : THIS ROUTINE SENDS A PROMT CHARACTER(*.) TO THE CONSOLE

LEBEL	ADDRESS	CONTENTS	MNEMONICS AND OPERANDS	COMMENTS
PCGR	C080	0E 0A	MVI C,0A	OUT PUT LF
	C082	CD 8781	CALL CO	
	C085	0E 0D	MVI C,0D	OUT PUT CR
	C087	CD 8781	CALL CO	
	C08A	0E 2A	MVI C,2A	OUT PUT *
	C08C	CD 8781	CALL CO	
	C08F	0E 2E	MVI C,2E	OUT PUT .
	C091	CD 8781	CALL CO	
	C094	C9	RET	RETURN

FUNCTION NAME : CMIP

INPUT : NONE

OUTPUT : MEMORY LOCATIONS FROM D505 TO D508

CALLS : CI,GETCR

DESTROYS : B,H,L,A,C

DESCRIPTION : INPUTS 4 CHARACTERS FROM THE TERMINAL AND THEN WAITS FOR CR IT LOADS THE ASCII CODES OF FIRST 4 CHARACTERS IN MEMORY LOCATIONS FROM D505 TO D508 IN ASCENDING ORDER

LEBEL	ADDRESS	CONTENTS	MNEMONICS AND OPERANDS	COMMENTS
	C0A7	06 04	MVI B 04	SET NO OF CHARACTER TO BE INPUTTED
	C0A9	21 05 05	LXI H, 0505	TO N ← 04; P_C AS POINTER
	C0AC	CD 4F 81	CALL CI	FOR STORING CHARACTERS IN MEMORY
	C0AF	77	MOV M,A	STORE THE CHARACTER
	C0B0	23	INX H	$P_C \leftarrow P_{C+1}$
	C0B1	05	DCR B	$N \leftarrow N-1$
	C0B2	C2 AC C0	JNZ C0AC	IF $N \neq 0$, INPUT NEXT CHARACTER
	C0B5	CD E5 82	CALL GETCR	WAIT FOR CR
	C0B8	C9	RET	RETURNS

FUNCTION NAME : CMPCH

INPUT : MEMORY LOCATIONS D530 TO D54B, D505 TO D508, D550 TO D562

OUTPUT : NONE

CALLS : MLPNT

DESTROYS : A,B,C,D,E,H,L etc.

DESCRIPTION : THIS ROUTINE COMPARES THE PREVIOUSLY STORED COMMAND CHARACTER ASCII CODES IN-D505-D508 WITH THE COMMAND TABLE ASCII CODES (STORED IN DS30 TO D54B). IF THE COMMAND MATCHES WITH ANY COMMAND IN THE LIST JHE CONTROL IS TRANSFERED TO COMMAND SERVICE SUBROUTINE

LEBEL	ADDRESS	CONTENTS	MNEMONICS AND OPERANDS	COMMENTS
CMPCH	C0FA	0E 03	MVI C,03	INITIALISE NO OF COMMANDS TO BE CHECKED
	C0FC	11 30 05	LXI D,D530	INITIALISE P_T POINTER OF COMMAND TABLE
	C0FF	0D	DCR C	
	C100	CA 31 C1	JZ C131	CHECKED
	C103	21 05 05	LXI H,D505	INITIALISE P_C<-POINTER OF COMMAND
	C106	A	LDAX D	
	C107	BE	CMP M	COMPARE IST COMMAND CHARAC-TER
	C108	CA 12 C1	JZ C112	
	C10B	7B	MOV A,E	$P_T \leftarrow P_T + 07$
	C10C	C6 07	ADI 07	POINTER POINTS TO START OF
	C10E	5F	MOV E,A	NEXT COMMAND IN TABLE
	C10F	C3 FF C0	JMP C0FF	
	C112	06 03	MVI B,03	INITIALISE NO OF 1 CHARAC:-TERS TO BE COMPARED AFTER 1ST CH = N
	C114	23	INX H	$P_T \leftarrow P_T + 1$
	C115	13	INX D	$P_C \leftarrow P_{C+1}$

IF COMMAND DOES NOT FOUND SUITABLE MATCH THEN A ERROR MESSAGE WILL BE FLASHED AND ROUTINE RETURNS TO LCI-SM MONITOR.

```
C116  1A        LDAX D      COMPARE CHARACTER
                            POINTED BY
C117  BE        CMP M       P_T AND P_C
C118  CA 29 C1  JZ C129
C11   7B        MOV A,E     X = 04-N
C11C  C6        ADI 07      P_T ← P_T + 07
C11E  5F        MOV E,A     P_T ← P_T + X
C11F  3E 04     MVI A,04    POINTER OF TABLE
C121  90        SUB B       POINTS TO NEXT COMMAND
C122  47        MOV B,A     STARTING CHARACTER.
C123  7B        MOV A,E
C124  90        SUB B
C125  51        MOV E,A
C126  C3 FF C0  JMP COFF
C129  05        DCR B       N ← N-1
C12A  C2 14 C1  JNZ C114    IS N = 0
                            ARE ALL CHARACTERS
                            COMPARED
C12D  13        INX D       P_T ← P_T+1
C12E  EB        XCH G       P_C ← P_T
C12F  E9        PCHL        P_C ← P_C
                            BRANCH TO FUNCTION
                            ROUTINE
C130  C9        RET
C131  21 50 D5  LXI H,D505  FLASH A
                            MESSAGE ERROR CALL HELP
C134  06 12     MVI B,12    ON CRT FOR 028
C136  C0 F5 82  CALL 82F5
C139  11 00 50  LXI D,5000
C13C  CD 10 81  CALL 8100
C13F  C3 E1 C0  JMP LCI-SM  RETURN TO
                            LCI-SM MONITOR
```

FUNCTION NAME : CHLOAD

INPUT : NONE

OUTPUT : MEMORY LOCATIONS D501 AND D502

CALLS : GETHX

DESTROYS : BC,, DE, HL, A

DESCRIPTION : LOADS VALUE OF FIRING ANGLE INPUTTED FROM THE TERMINAL IN MEM.LOCATION D501 THE VALUE OF 60°=3C IS STORED IN LOCATION D502, BEFORE RETURNING.

LEBEL	ADDRESS	CONTENTS	MNEMONICS AND OPERANDS	COMMENTS
ACH LOAD	C070	21 01 D5	LXI H D501	MOVE α IN REG C
	C073	CD EA 81	CALL GETHX	TO D501
	C076	71	MOV M,C	
	C077	06 3C	MVI B,3C	STORE 3C
	C079	23	INX H	(ie 60° DECIMAL)
	C07A	70	MOV M,B	IN D502
	C07B	C9	RET	RETURN

FUNCTION NAME : STAR

INPUT : MEM. LOCATIONS D562 TO D564

OUTPUT : MEM. LOCATION D501

CALLS : SWO, MLPNT, CHLOAD

DESTROYS : A,B,C,H,L
MEM. LOCATION D501

DESCRIPTION : THIS ROUTINE CLEARS THE WHOLE SCREEN AND DISPLAYS THE SIGN-ON MESSAGE AS DISCUSSED EARLIER. THEN IT ASKS FOR FIRING ANGLE TO BE INPUTTED IN BINARY AND STORES THE VALUE IN D501. THE ROUTINE THEN BRANCHES TO LCI-FA ROUTINE

LEBEL	ADDRESS	CONTENTS	MNEMONICS AND OPERANDS	COMMENTS
STAR	COD0	CD 95 C0	CALL SWO	WIPES OUT THE CRT SCREEN
	COD3	21 62 D5	LXI H,ØD562	DISPLAYS SIGN ON MESSAGE
	COD6	06 72	MVI B,72	
	COD8	CD F5 82	CALL 82F5	
	CODB	CD 70 60	CALL CHLOAD	WAITS FOR α TO BE INPUTTED
	CODE	C3 00 C0	JMP ØC000	BRANCH FOR EXECUTION OF LCI-FA

FUNCTION NAME : HELP

INPUT : MEMORY LOCATIONS D504 TO D513

OUTPUT : NONE

CALLS : MLPNT, PCGR, CI

DESTROYS : A,B,C,D,H,L,

DESCRIPTION : THIS ROUTINE DISPLAYS THE LIST OF VALID COMMANDS AS -

1) HELP

2) STAR

INPUT COMMAND NO.X

THIS ROUTINE IS ALREADY DESCRIBED EARLIER

LEBEL	ADDRESS	CONTENTS	MNEMONICS AND OPERANDS	COMMENTS
HELP	C0BA	27 D5 D5	LXI H,D5D5	OUTPUT THE COMMAND
	C0BD	06 3E	MVI B,3E	LIST
	C0BF	CD F5 82	CALL MLPNT	
	C0C2	CD 80 C0	CALL PCGR	WAIT FOR COMMAND NUMBER
	C0C5	CD 4F 81	CALL CI	TO BE INPUTED FROM CRT
	C0C8	D6 01	SUI 01	
	C0CA	C2 31 C1	JNZ C1 31	IF COMMAND NO ≠ 1 THEN FLASH ERROR RETURN TO LCI-SM
	C0CD	C3 D0 C0	JMP STAR	EXECUTE STAR COMMAND

FUNCTION NAME : LCI-FA

INPUT : MEM. LOCATION D501, CF00-CF77,D000-D012

OUTPUT : NONE

CALLS : DELAY

DESTROYS : A,B,C,D,E,H,L

DESCRIPTION : THIS PROGRAM CONTROLS THE FIRING ANGLE α OF LCI AND THE SEQUENCE OF THE FIRING PULSES TO THE VARIOUS SCR ARE ALSO DETERMINED.

LEBEL	ADDRESS	CONTENTS	MNEMONICS AND OPERANDS	COMMENTS
LCI-FA	C000	21 00 D0	LXI H,D000	
	C003	22 03 D5	SHLD D503	
	C006	3E 81	MVI A,81	INITIALISE 8255(1)
	C008	D3 53	OUT 53	PA-O/P,PB-O/P,PC_L-I/P PC_U-O/P
	C00A	3E 0D	MVI A,0D	UNMASK RST6.5
	C00C	30	SIM	
	C00D	FB	EI	ENABLE INTERRUPT SYSTEM
	C00E	76	HLT	SYNCHRONISE WITH RST5.5
	C00F	C3 00 C0	JMP C000	
RST6.5	C012	3E 30	MVI A,30	INITIALISE 8253
	C014	D3 5B	OUT 5B	COUNTER 0 MODE 0
	C016	21 01 D5	LXI H,D501	
	C019	7E	MOV A,M	
	C01A	23	INX H	
	C01B	46	MOV B,M	
	C01C	23	INX H	
	C01D	B8	CMP B	IS $\alpha \leq 60^{\circ}$
	C01E	DA 20 C0	JC C02D	YES, BRANCH
	C021	5F	MOV E,A	NO, MODIFY THE POINTER
	C022	3E 06	MVI A,06	OF FIRING COMMAND
	C024	86	ADD M	WORD TO POINT TO THE NEXT COMMAND GROUP
	C025	00	NOP	ie GROUP NO 2

	C026	M77	MOV M,A	POINTER ← POINTER + 06
	C027	7B	MOV A,E	α<- α - 60°
	C028	90	SUB B	
	C029	00	NOP	
	C02A	C3 1D C0	JMP C01D	AGAIN CHECK VALUE OF α IF LESS THAN 60°
	C02D	87	ADD A	α ← α + α
	C02E	5F	MOV E,A	COMPUTE ADDRESS OF DELAY WORD FOR α ie
	C02F	16 CF	MVI D,CF	ADDR ← CF2α
	C031	1A	LDAX D	LOAD DELAY
	C032	03 58	OUT 58	WORD IN COUNTER 0
	C034	13	INX D	C
	C035	1A	LDAX D	
	C036	D3 58	OUT 58	
	C038	3E 0E	MVI A,0E	UNMASK RST 5.5
	C03A	30	SIM	
	C03B	FB	EI	ENABLE INTERRUPTS SYSTEM
	C03C	00	NOP	
	C03D	00	NOP	
	C03E	DB 52	IN 52	STATUS OF 3ϕ LINE VOLTAGES
	C040	E6 07	ANI 07	MASK HIGHER 5 BITS
	C042	86	ADD M	COMPUTE THE
	C043	4F	MOV C,A	FIRING COMMAND WORD ADDRESS FOR CURRENT
	C044	23	INX H	60° INTERVAL
	C045	66	MOV H,M	POINTER STATUS OF 3ϕ LINE
	C046	69	MOV L,C	VOLTAGES + POINTER
	4047	7E	MOV A,M	
	4048	76	HLT	SYNCHRONISE WITH RST 5.5
	4049	FB	EI	INTERRUPT
	404A	C9	RET	RETURN FROM RST6.5 I.S.S.
ISS RST5.5	C04B	03 50	OUT 50	OUT PUT FIRING
	404D	11 17 00	LXID 0017	PULSES FOR 180 μS DURATION

APPENDIX - IV

SYSTEM SPECIFICATIONS (VMDS-85) :

CPU -	- 8 bit Microprocessor, the 8085.
MEMORY	- Can be expended upto 64K byte.
RAM	- 16K byte (8 Nos. of CMOS RAM. 6116).
ROM	- 16K byte loaded with powerful monitor.
I/O Lines	- 24 Programmable input/output lines can be incorporated in the CPU Card.
Interface	- TTY (20mA current loop).
	- CRT (20mA or RS-232-C interface).
BUS	- STD Bus. All address, data and control signals. (TTL compatible) available at edge connector.
Power Supply Requirement.	- 230 V, $\pm$ 10%, 50Hz.
Operating Temp.	- 0 to 50^{o} C.

APPENDIX V

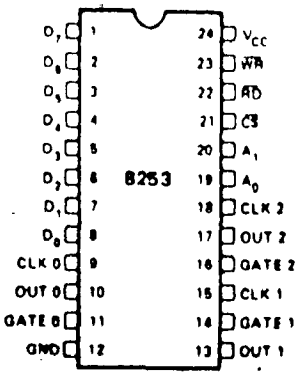
SYSTEM SPECIFICATIONS: VDT-85

DISPLAY UNIT	:	12" nonglare screen.
Screen Capacity	:	25 lines X 80 characters (Including status line).
Character Display	:	5 X 7 dot matrix light character with dark background or dark characters with light background.
Character Set	:	96 ASCII characters with lower case.
Refresh Rate	:	50 Hz.
Bit structure	:	Data : 5,6,7 or 8 bits. Start.- 1 bit. Stop : 1, 1.5 or 2 bits. parity : 1 bit.
Parity	:	Odd/Even or no parity.
Baud rate	:	75, 110, 150, 300, 600, 1200, 2400, 4800, 9600, 19.2K (Software selectable).
Transmit/Receive mode:		Half/Full duplex.
Visual Attributes	:	Normal, Blinking, Reverse Video, Underline and Reduced intensity.
Memory	:	Multi page memory (upto 4 pages).
Keyboard	:	111 keys keyboard communicate with the display unit through three wire transmission.
Cursor Movement	:	Cursor up, cursor down, cursor home, cursor right, cursor left, cursor right up, cursor right down, cursor left up, cursor left down.
Cursor Addressing	:	Director cursor addressing.
Display Movements	:	Roll up/Roll down. Next page/Previous page. Row swap.

TRANSMIT/ERASE	:	a) Entire memory (all four pages). b) The current displayed page. c) The line on which the cursor is located. d) The character on which the cursor is located. e) From cursor position to end of page. f) From start of page to current cursor position. g) From cursor position to end of line. h) From start of line to current cursor position. i) P1 characters from current cursor position.
Tabulation	:	Tab set/Clear facility.
User Definable Keys	:	10 keys F0 to F9.
Escape Sequences	:	Full cursor Control, Memory erase, Tab facility Editing functions, provided through escape sequence.
Interfaces	:	RS-232-C, 20mA current loop. Printer interface (Optional). Aux RS-232-C (Optional).
Power Input	:	230V, $\pm$ 10%, 50Hz.
Power Consumption	:	60 Watts, nominal.
Operating Temperature	:	0 to 45^{o}C.

APPENDIX VI

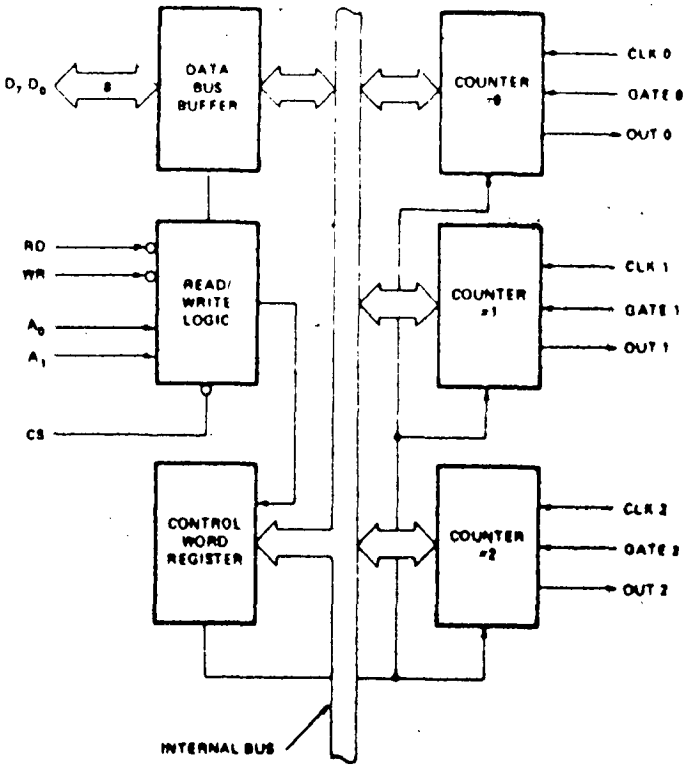
PIN CONFIGURATION



PIN NAMES

D_7 D_0	DATA BUS (8 BIT)
CLK N	COUNTER CLOCK INPUTS
GATE N	COUNTER GATE INPUTS
OUT N	COUNTER OUTPUTS
$\overline{RD}$	READ COUNTER
$\overline{WR}$	WRITE COMMAND OR DATA
$\overline{CS}$	CHIP SELECT
A_0, A_1	COUNTER SELECT
V_{CC}	+5 VOLTS
GND	GROUND

BLOCK DIAGRAM



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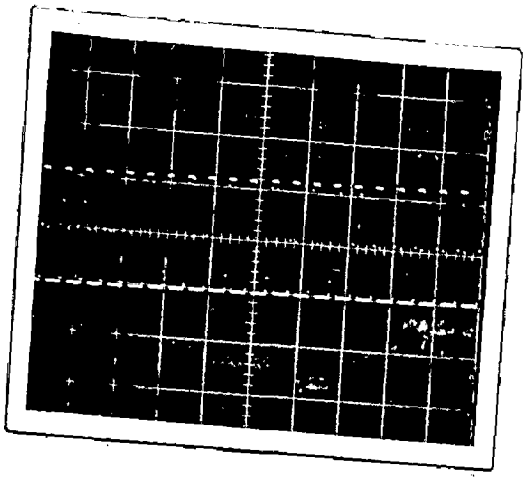
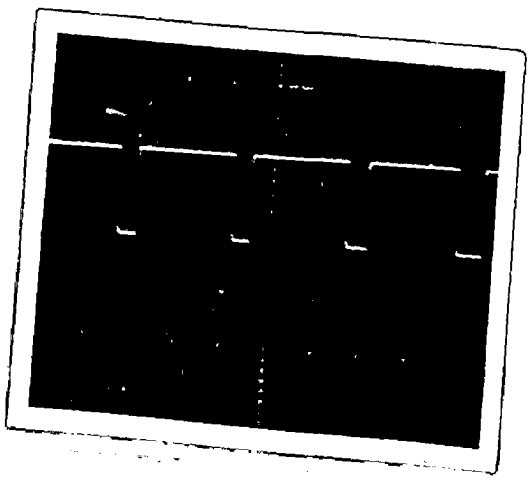
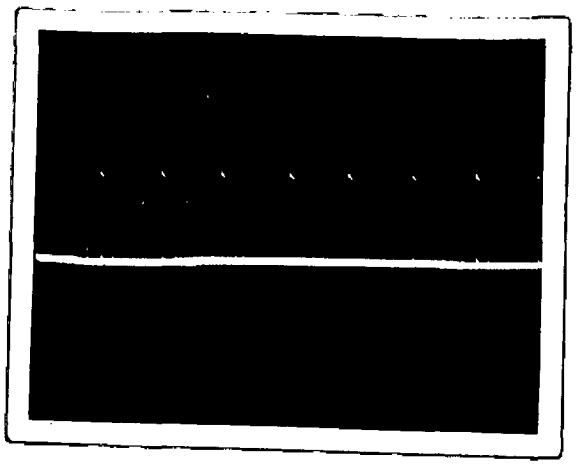


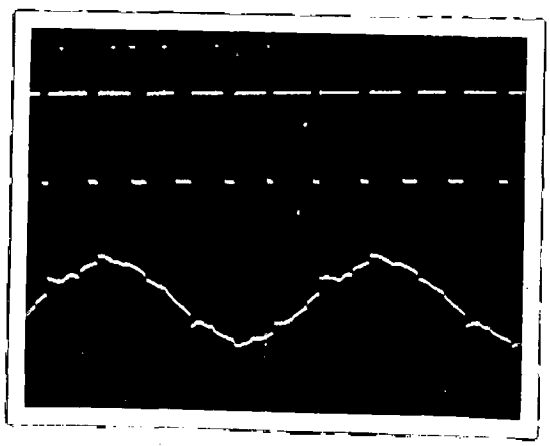
1. OUTPUT FREQUENCY OF VOLTAGE CONTROLLED OSCILLATOR LM 331.



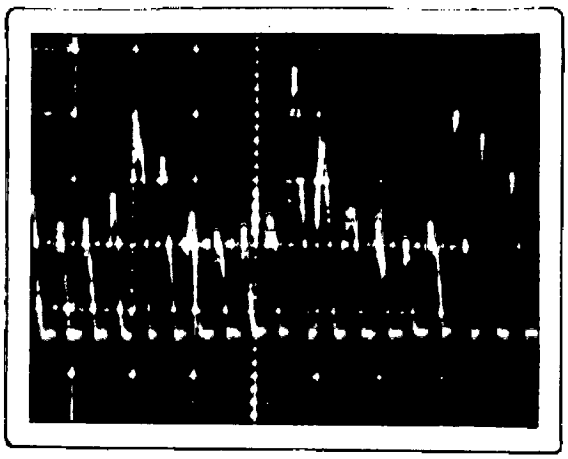
2. OUTPUT OF TIMER 0 OF 8253, USED AS RST 5.5 INTERRUPT SIGNAL



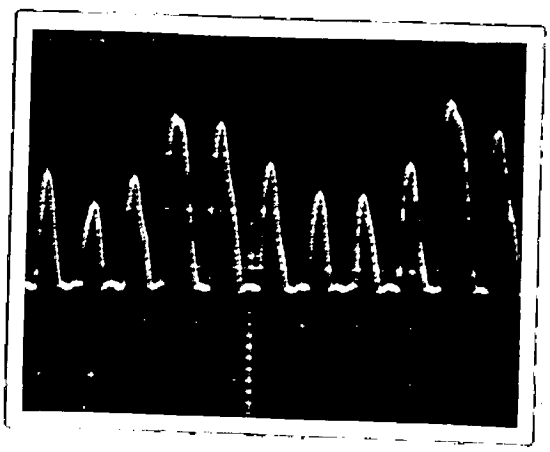
3. ZEROCROSSING CIRCUIT OUTPUT VOLTAGE WAVEFORM RST 6.5 INTERRUPT SIGNALS



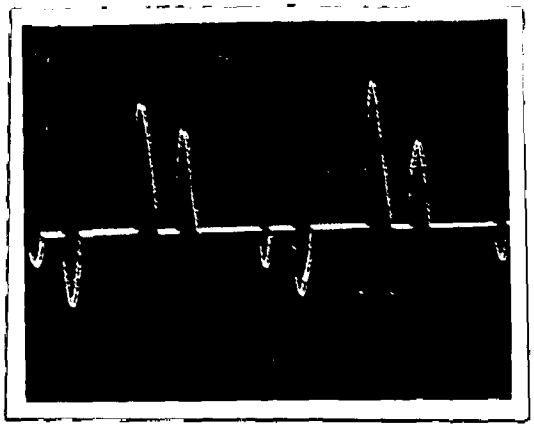
4. LCI OUTPUT TERMINAL VOLTAGE WITH SYNCHRONOUS MOTOR RUNNING ON NOLOAD AND OUTPUT OF TIMER 0 OF 8253 i.e. RST 5.5 SIGNAL



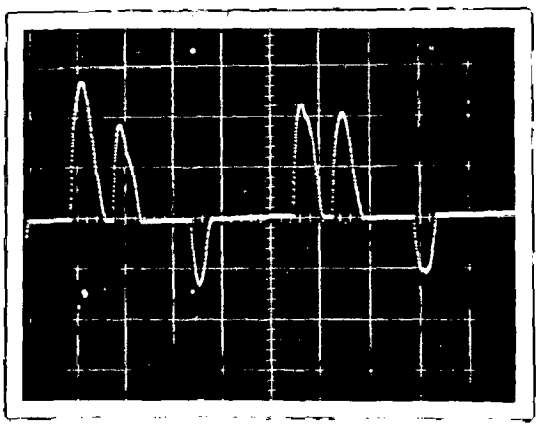
5. D.C.LINK CURRENT WAVEFORM WITH 12mH D.C. LINK INDUCTOR AND THE SYNCHRONOUS MOTOR RUNNING ON NOLOAD.



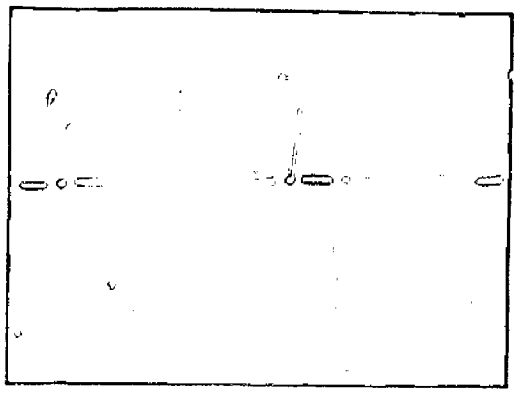
6. ENLARGED VIEW OF D.C.LINK CURRENT WAVEFORM FOR A 12mH D.C.LINK INDUCTOR AND SYNCHRONOUS MOTOR RUNNING ON NOLOAD.



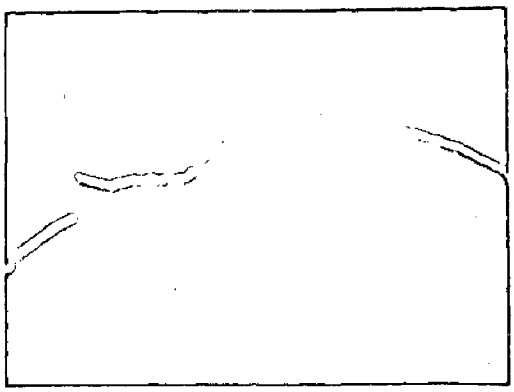
7. SYNCHRONOUS MOTOR CURRENT ON NOLOAD FOR 12mH D.C.LINK INDUCTOR



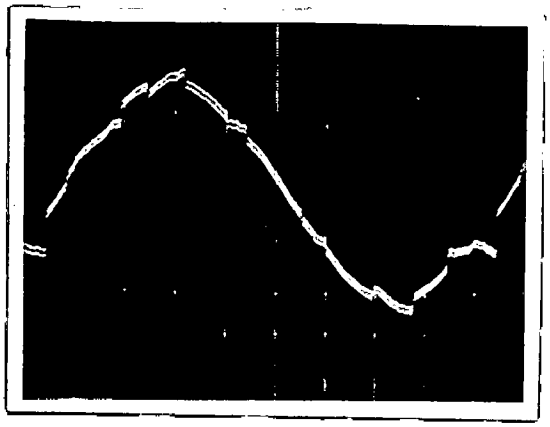
8. SYNCHRONOUS MOTOR CURRENT ON LOAD



9. SYNCHRONOUS MOTOR NOLOAD CURRENT WAVE [illegible] CAPACITOR IN PARALLEL.



10. ENLARGED VIEW OF THE COMMUTATION OVERLAP REGION IN THE TERMINAL V[illegible] OF LCI WHEN INDUCTION MOTOR IS LOADED.

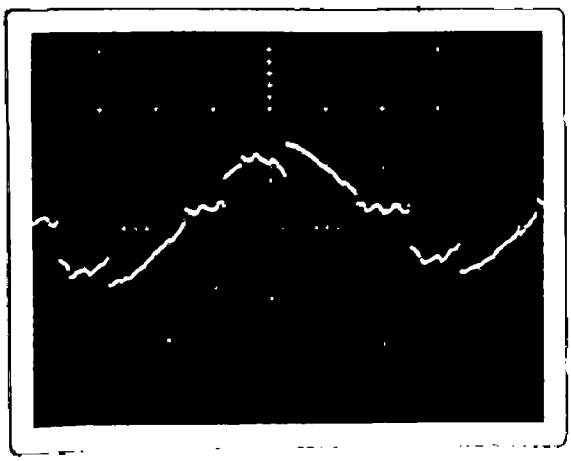


12. LCI OUTPUT VOLTAGE WAVEFORM WITHOUT CAPACITORS CONNECTED IN PARALLEL.

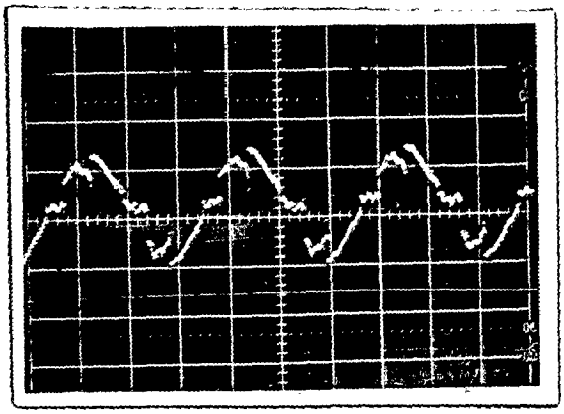
11

LCI OUTPUT VOLTAGE WAVEFORM WITH CAPACITORS CONNECTED IN PARALLEL .

13. SYNCHRONOUS MOTOR CURRENT WITH INDUCTION MOTOR CONNECTED IN PARALIEL

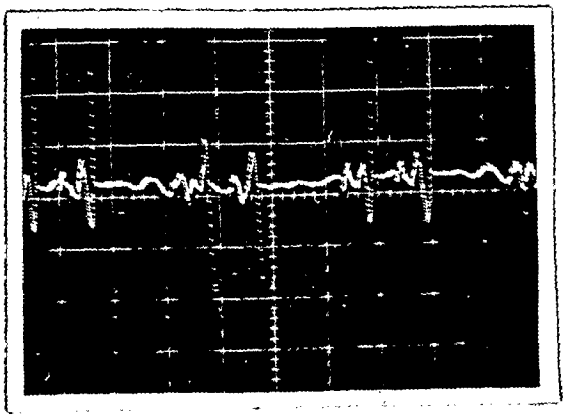


14. INDUCTION MOTOR CURRENT

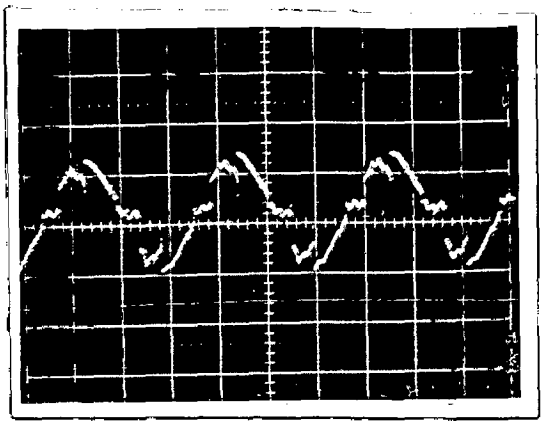


15.

INDUCTION MOTOR CURRENT UNDER LOADED CONDITION

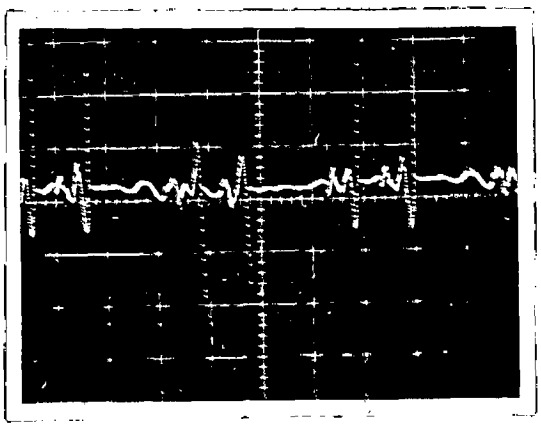


16. CAPACITOR CURRENT WAVEFORM

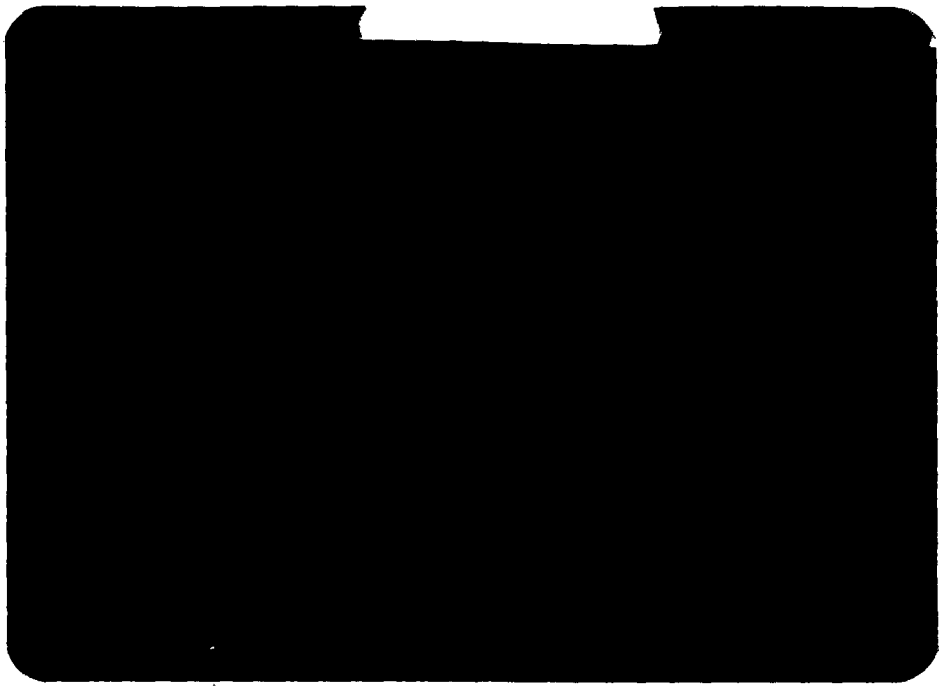


15.

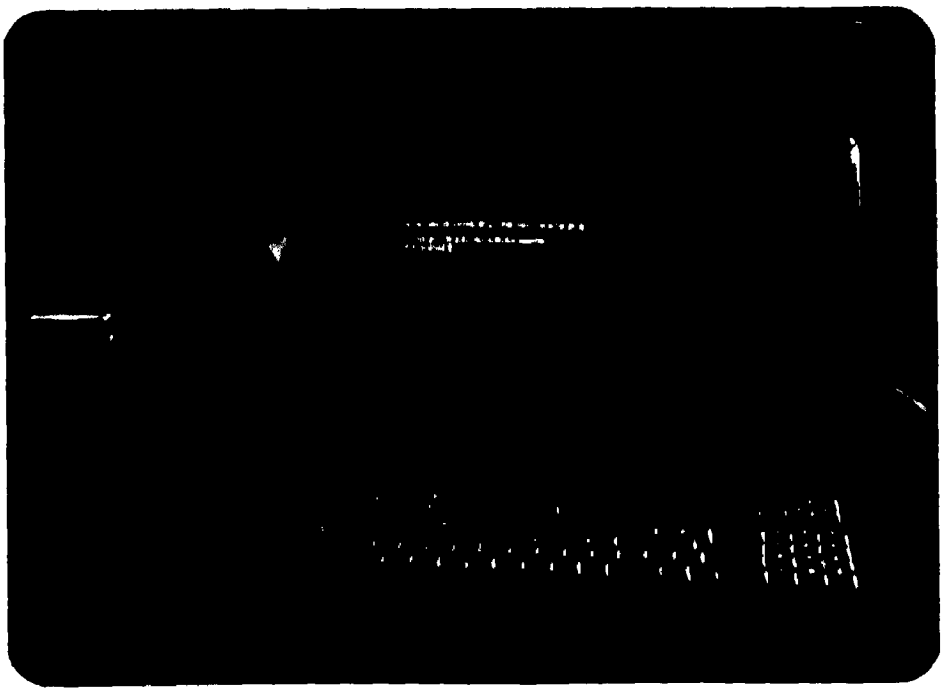
INDUCTION MOTOR CURRENT UNDER LOADED CONDITION



16. CAPACITOR CURRENT WAVEFORM



18. D.C.LINK CURRENT WITH LARGE IRON CORE INDUCTOR IN D.C.LINK.



17 D.C.LINK CURRENT WITH112mH D.C.LINK INDUCTOR.