DESIGN AND DEVELOPMENT OF 150 KV IMPULSE VOLTAGE DIVIDER

A DISSERTATION

submitted in partial fulfilment of the
rquirements for the award of the degree
of
MASTER OF ENGINEERING
in
ELECTRICAL ENGINEERING
(Power System Engineering)

By

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CERTIFICATE

Certified that the dissertation entitled "Design and Development of 150 KV Impulse Voltage Divider" being submitted by Mr. S.K. Goel in partial fulfilment for the award of the degree of Master of Engineering in Electrical Engineering(Power System Engineering) of the University of Roorkee, Roorkee is a record of the student's own work carried out by him under my supervision and guidance. The matter embodied in this dissertation has not been submitted for the award of any other degree or diploma.

This is to further certify that he has worked for a minimum period of $4\frac{1}{2}$ months from Jan. 1981 to May 1981 for preparing this dissertation at this University.

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Dated: October 7 , 1982.

SUMMARY

The measurement of high impulse voltages necessiates the use of a suitable voltage divider in order to determine the peak voltage and the waveshape of the impulse. Resistance, capacitance or mixed (R-C in series or in parallel) dividers are used for this purpose. The present thesis is a report on the work carried out on the design and development of a 150 KV damped capacitive (series mixed type) voltage divider in order to be able to measure the output of 150 KV impulse voltage generator already developed in the H.V. laboratory of the department.

In designing the divider, its parameters have been fixed by treating it as a transmission line since the high voltage arm is made up of many series elements of resistance and capacitance. The matching of the low voltage arm and the high voltage arm is also looked into to achieve divider response without oscillations and without reflections. The design ratio has been fixed at 1250, its capacitance being 35 pf and resistance being 115 ohms.

The performance of the divider response is studied with rectangular low voltage signals and with step function. The divider ratio measured at low input voltage is 1500. The rise time of the divider was less

than 30 ns and overshoot was less than 2% when a rectangular pulse of rise time less than 100 ns was applied to it. For an input of step function having a rise time of less than 10 ns, the response time of the divider was less than 10 ns. The divider was tested at 50 KV impulse voltage which it withstood successfully.

CONTENTS

LIST OF PHOTOGRAPHS

1. INTRODUCTION

The developments in the field of electrical engineering during the present century have been tremendous. Phenomenal increase in power demand at longer distances has forced the transmission voltages to be higher and higher from economics point of view. In the world 1100 K.V. transmission lines are already in operation and in India 400 K.V. lines have been built.

A large number of expensive electrical equipments are used for high and extra high voltages transmission lines. It is necessary to ensure that such costly equipments are capable of withstanding the overvoltages which are met due to lightning and switching transients.

The power transmission lines and their associated equipments are therefore frequently subjected to the high impulse voltage tests which are performed by the use of impulse generator.

Impulse generators upto 10 MV have been fabricated for research, development, training and testing purposes. The measurement of such high voltages is carried out by dividing the voltage with the help of impulse voltage divider and measuring the divided low voltage by C.R.O. or by peak voltmeter.

Impulse voltages dividers are of many types; the simplest being a resistance divider and is often used for recording the sstandard lightning impulse. For recording fast and slow transients a pure capacitive divider is used, the advantage being that its ratio is independent of frequency. However residual inductances and capacitances of the divider frequently introduce oscillations. Also its high cost prohibits its use. A mixed divider of parallel arrangements obtained by adding capacitors in parallel with resistor units behaves as a resistance divider for slow transients and capacitor divider for fast transients. The damped capacitive divider (series resistance - capacitance divider) obtained by adding resistor units in series with capacitor units is used for measurement of impulses of higher voltages (>1 MV) because of better response than the above mentioned dividers. It also enables the measurement of super imposed impulse and power frequency voltages.

There was a need of building of a voltage divider of 150 KV impulse voltage because an impulse generator of 150 KV was designed and developed in High Voltage Lab. of this department for teaching, training and research work. This dissertation pertains to design, development and fabrication of 150 KV damped resistance-capacitance divider.

In India only very recently high voltage components such as low loss capacitors, low tolerance and high stability resistors are being manufactured. Even then the main difficulty for this work was the acquisition of high voltage components.

In testing the impulse divider the main difficulty come of the nonavailability of a single shot C.R.O.

1.1 Arrangement of the Thesis

The thesis is divided in eight sections which are arranged in the order in which the work was done.

Section 1 gives the introduction which explains the nature of the problem and the arrangement of the thesis.

Section 2 gives the basic definitions used in impulse technology.

Section 3 gives the literature survey which includes the various types of dividers and the review of the work done by other research workers in field of impulse voltage measurement. The various sources of error in the divider and methods suggested by researchers to eliminate these errors are discussed in this chapter.

Section 4 gives the design of 150 KV impulse voltage divider. Firstly the general design considerations

of a damped capacitive divider are discussed. Secondly the actual design of the H.V. arm and L.V. arm of 150 KV impulse voltage divider is given.

Section 5 gives the fabrication of the divider.

Section 6 gives the experimental results and the analysis of the performance of the divider at low voltage signals and at high impulse voltage.

Section 7 gives the discussion of the experimental results.

Section 8 gives the conclusion in which suggestions are also put up for future work.

At the end references [redacted] are given.

2. DEFINITIONS AND STANDARDS OF WAVESHAPES

Before discussing the impulse voltage divider it is necessary to describe some important definitions related with the impulse wave.

2.1 Full Impulse Voltage [1][2][3]

Ideally an aperiodic transient voltage which rises rapidly to a maximum value and falls usually less rapidly to zero. In fig. 1. a OCD is the full impulse voltage wave.

2.2 Chopped Impulse Voltage

A transient voltage derived from a full impulse voltage which is interrupted by a disruptive discharge causing a sudden collapse in the voltage practically to zero value. The collapse may occur on the front, at the peak or on the tail. In fig. 1. b and c the chopped impulse voltage waveshapes have been shown. In fig. 1 b it is chopped on front and is shown by point X. In fig. 1. c it is chopped on tail and is shown by point Y.

2.3 Peak Value

The maximum amplitude of the impulse is called the peak value and the impulse voltage is specified by this value. In fig. 1. a OE is the peak value.

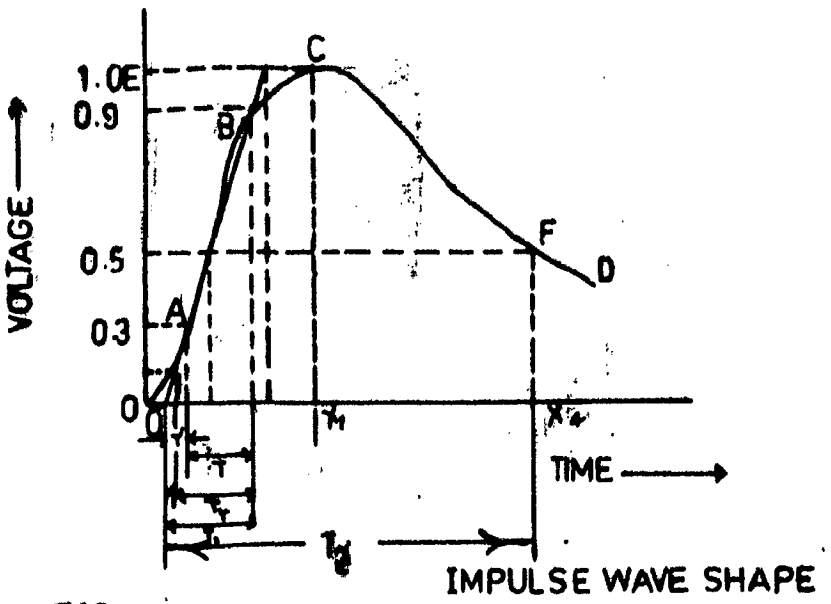


FIG 1a :

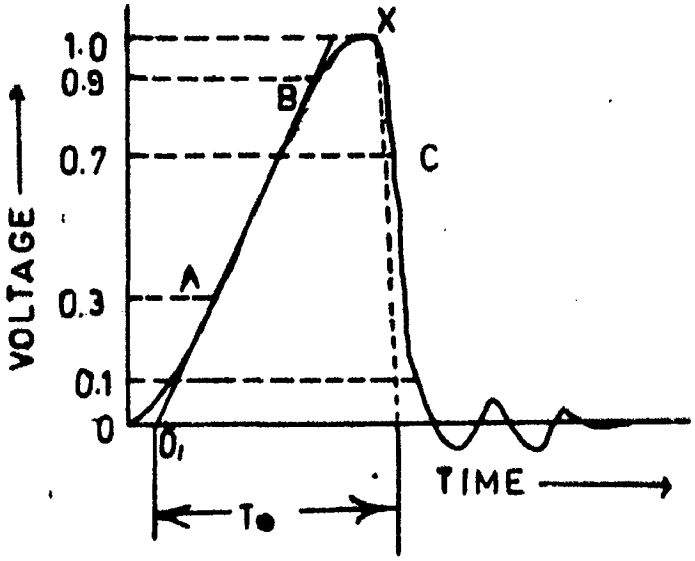


FIG 1b: IMPULSE VOLTAGE CHOPPED ON THE FRONT

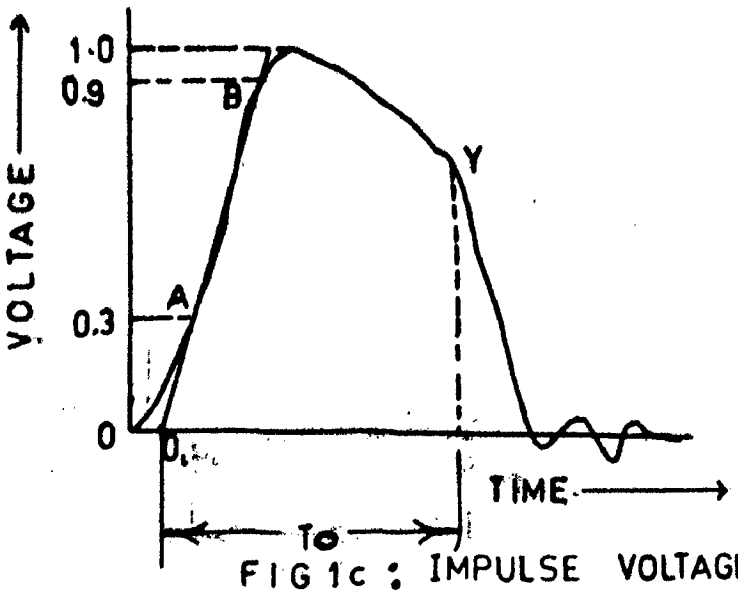


FIG 1c : IMPULSE VOLTAGE CHOPPED ON THE TAIL

2.4 Virtual Peak Value

In some impulse voltage waveshapes oscillations or overshoot may be present on the voltage time characteristic. If the amplitude of oscillations is not greater than 5 % of the peak value and the frequency is at fast .5 Mc/s, or alternatively, if the amplitude of the overshoot is not greater than 5 % of the peak value and the duration not longer than 1 μs, then for the purpose of measurement a mean curve may be drawn, as shown in fig. 2, the maximum amplitude of which is defined as the virtual peak value. In fig. 2 it is shown by OE.

2.5 Wave Front

It is the rising portion of the voltage time characteristic of the impulse voltage. In fig. 1 a it is shown by the portion OC.

2.6 Wave Tail

It is the falling portion of the voltage time characteristic of the impulse voltage. In fig. 1 a it is shown by CD.

2.7 Definitions Applic-able to Full Impulses

For these definitions fig. 1 a is referred.

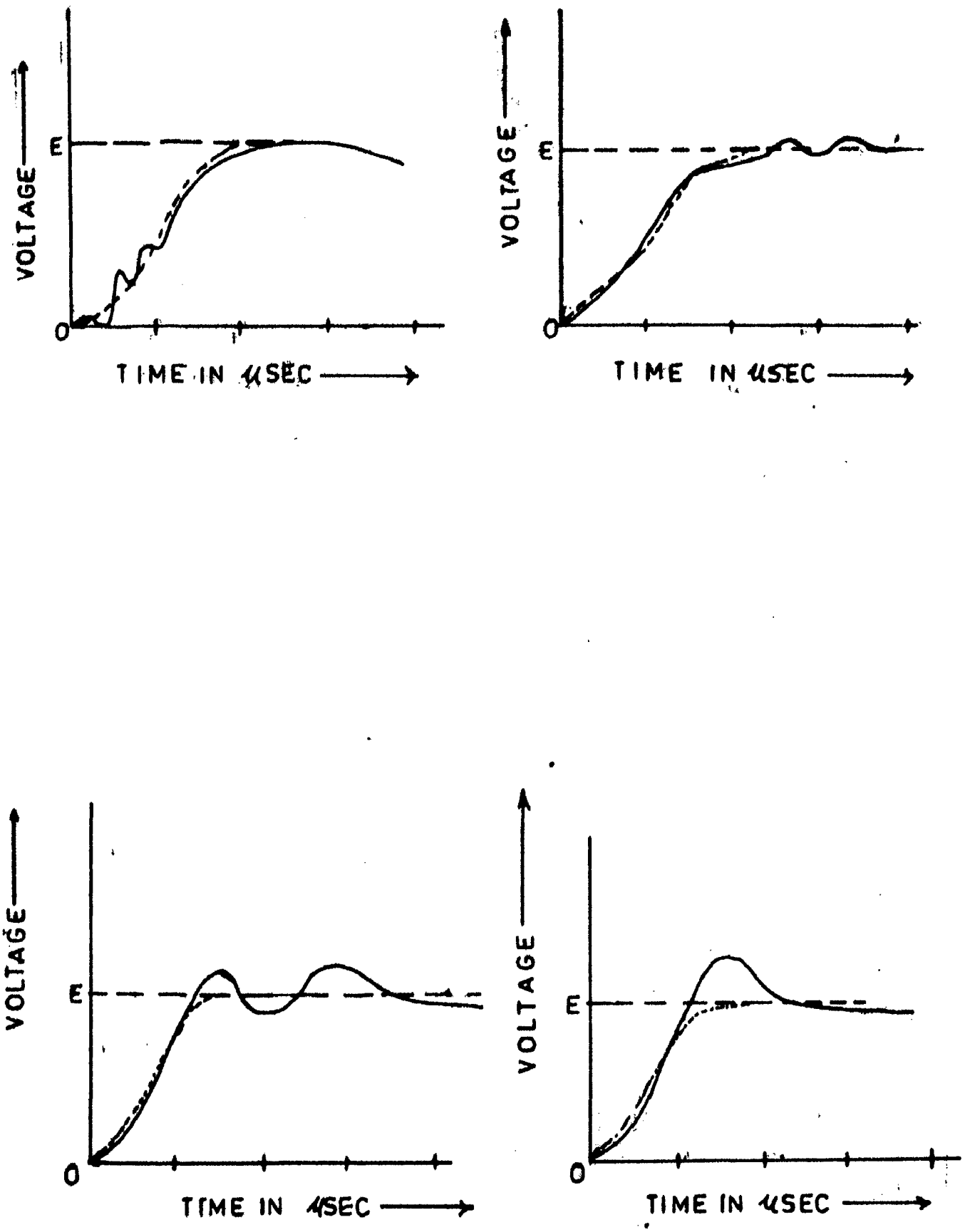


FIG 2 : DERIVATION OF VIRTUAL PEAK

2.7.1 Virtual front time(T_1)

It is defined as 1.67 times the time interval T between the instants where the impulse is 30 percent and 90 percent of the peak value. If oscillations are present on the front, the points A and B should be taken on the mean curve drawn through these oscillations.

2.7.2 Virtual Origin of an Impulse Wave (O')

It is defined as the instant preceding that corresponding to point A by a time $0.3T_1$. For oscillograms having linear time sweeps, this is the intersection with the X-axis of a straight line drawn through the reference points A and B on the front.

2.7.3 Virtual Steepness of the Front

The virtual steepness of wavefront of an impulse voltage is the average rate of rise of voltage measured between the points on the wavefront where the voltage is 30 % and 90 % of peak value

2.7.4 Virtual Time of Half Value(T_2)

The time interval between the virtual origin and the instant on the tail when the voltage was decreased to half the peak value. In fig. it is shown by point F. O'F

2.8 Lightning and Switching Impulses

A distinction is made between lightning impulses and switching impulses on the basis of the duration of the wavefront. Impulses with front durations from one upto some tens of microseconds are in general considered as lightning impulses and those having front durations of some tens upto hundreds of microseconds, as switching impulses. In general switching impulses are characterized by considerably longer total durations than those of lightning impulses.

2.8.1 Standard Lightning Impulse

It is characterized by 1.2/50 μ sec. wave.

Tolerances:	Peak value	± 3 %
	Front time	± 30 %
	Tail time	± 20 %

2.8.2 Standard Switching Impulse

It is characterized by a 250/2500 μ sec. wave.

Tolerances:	Peak value	± 3 %
	Front time	± 20 %
	Tail time (Time to half value)	± 60 %

2.9 Rise Time

The high frequency characteristics of a measuring system are described principally by Bandwidth B, by rise time T_r, or, in high voltage terminology, by response-time Tres. Rise time has prevailed particularly in the field of pulse techniques. The rise time of a voltage or current pulse is defined as the time required for the quantity to increase from 10 % to 90 % of its final value. In fig. 1 a it is shown by T_r.

Rise time of a system e.g. that of a C.R.O. is defined as the rise time of the output voltage if an infinitely step voltage step is applied across its input - in other words the rise time of systems step response.

Until the term 'rise time' was introduced, the quality of voltage dividers was commonly described by their time constant. Small time constants insured a high upper frequency limit.

A close relation exists between the rise time T_r and the time constant T of the exponential rise for a measuring signal. Applying a voltage step $v_1(t) = V_o.u_1(t)$ to the input terminals of an RC circuit, shown in fig. 3 a, results in an exponential rise of the output voltage:

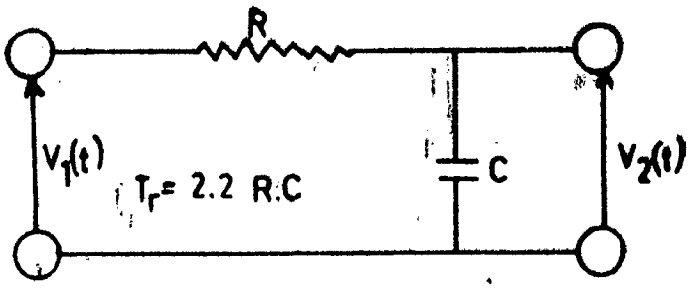


FIG 3a: RC TWO-PORT RELATIONSHIP BETWEEN RISETIME Tr AND TIME CONSTANT T_c

$T_c = RC$

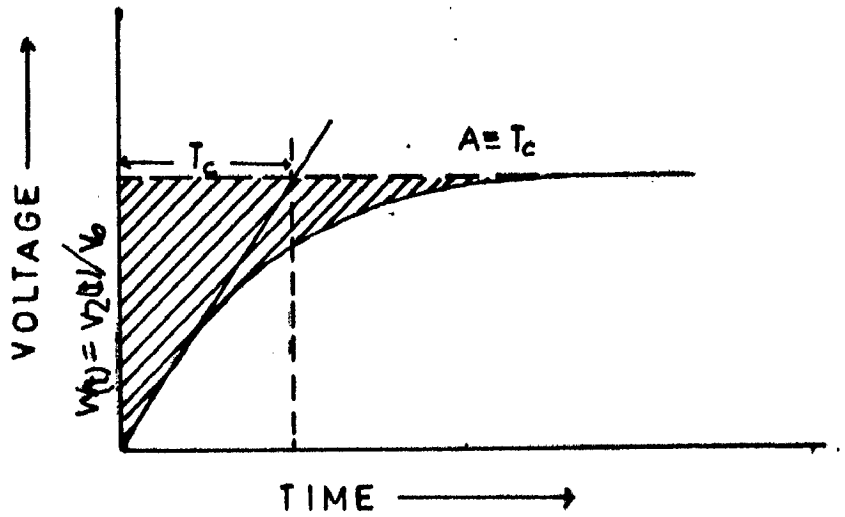


FIG 3b: TIME CONSTANT DEFINITIONS FOR STEP RESPONSE CURVES

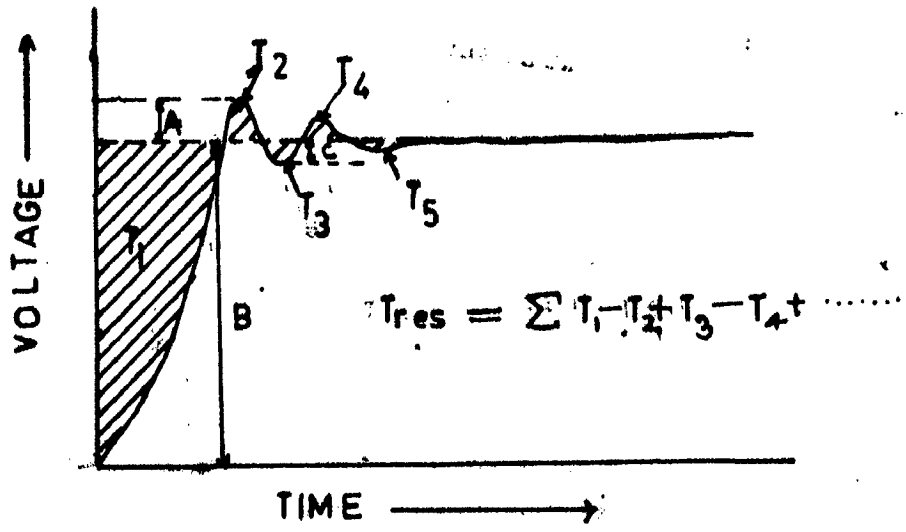


FIG 3c : RESPONSE TIME DEFINITION

The rise time of the RC circuit is

$$T_r = 2.2 RC = 2.2\, T_c$$

Referring to fig. 3 b the time constant of the step response may be evaluated by means of the tangent at the origin as well as from the integral

$$T_c \equiv S = \int_0^\infty [\,1 - w(t)\,]\, dt$$

$$= \int_0^\infty e^{-t/RC}\, dt$$

$$= \left[- RC\, e^{-t/RC} \right]_0^\infty$$

$$= -RC \left[\frac{1}{e^{t/RC}} \right]_0^\infty$$

$$= -RC \left[\frac{1}{e^\infty} - \frac{1}{e^0} \right]$$

$$= -RC \,[\, 0 - 1 \,]$$

$$= RC$$

Here S corresponds to the shaded area.

2.10 Response Time

When the step function rings or exhibits significant overshoot, time constant evaluation by tangent method is questionable.[5] Because of the large dimensions in high voltage test arrangements considerable lead industances and stray capacitances are present and often cause superposition of troublesome oscillations upon an exponential rise. A step response of this type is shown in fig. 3 c.

In order that these cases may be described by a time constant, the term response time was defined to represent the area enclosed by the normalised step response, its final value 1 and the axis t = o.-

$$T_{res} = \int_0^\infty [\, 1 - h(t)] \, dt$$

$$= T_1 - T_2 + T_3 - T_4 + \ldots\ldots$$

2.11 Overshoot

When the step function rings, it is settled after some time to a value known as settling value. The amplitude of the wave above this settling value is known as overshoot and is defined in percentage. In fig. 3 o percentage overshoot is A/B x 100.

2.12 Undershoot

Similarly undershoot is defined as the amplitude below the settling value. In fig.3c percentage undershoot is defined as C/B x 100.

3. LITERATURE SURVEY

In the measurement of high voltages, it is usually not possible to measure the voltages by direct connection of a voltmeter, because conventional voltmeters are to a great extent, incapable of measuring such high voltages. In general some indirect methods are used and the devices are calibrated in such a way that the accurate voltage measurement may be obtained in practice. Indirect methods generally used are sphere gap method and potential divider method. Sphere gap method has certain disadvantages over potential divider method:

1. By this continuous record of voltage can not be obtained.
2. It takes into account humidity, pressure, temperature, proximity of earthed objects to the testing site etc. which are of statistical nature. These statistical factors introduce some errors in the voltage measurement.

Potential dividers used for the measurement of impulse voltages are of many types.

3.1 Potential Divider

Potential Divider is basically a series combination of a high and low impedance. The voltage to be measured is

applied across the combination and a drop across the low impedance section is measured.

The simplest potential divider[4] can be represented as shown in fig. 4.

Let V_1 = Total voltage across the potential divider.

V_2 = Sample voltage to be measured.

$$V_2 = \frac{Z_2}{Z_1 + Z_2} \cdot V_1$$

If only pure resistance dividers are used it becomes a resistance divider,

and $$V_2 = \frac{R_2}{R_1 + R_2} V_1$$

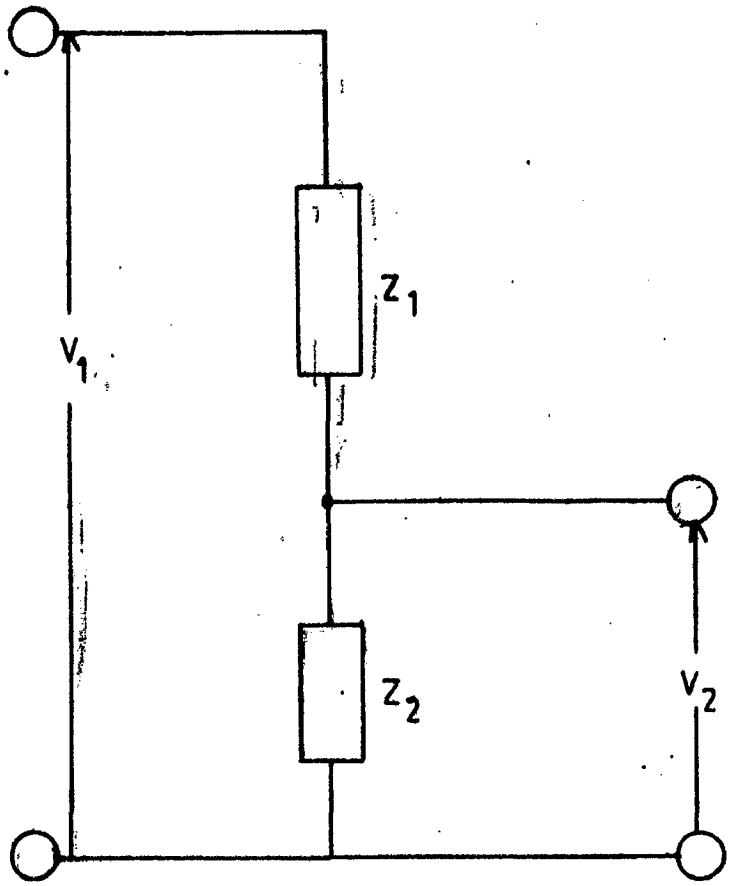
If only pure capacitors are used it becomes a purely capacitive divider, and

$$V_2 = \frac{C_1}{C_1 + C_2} V_1$$

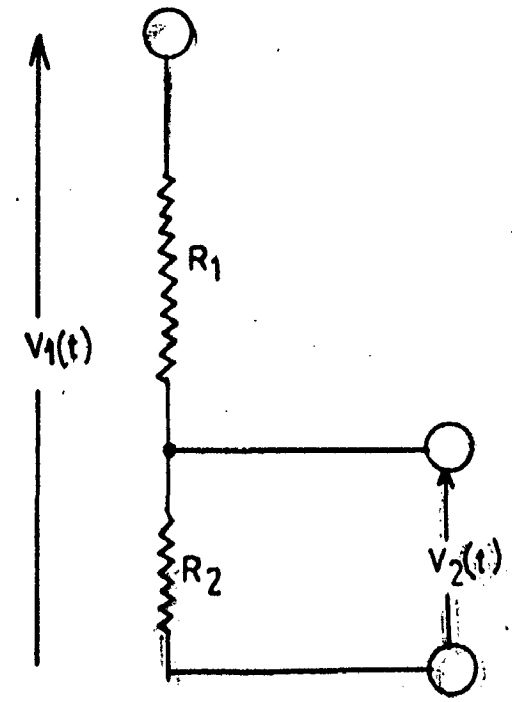
The sample voltage is normally a few hundred volts while the total voltage V_1 is of the order of hundred of KV's. Thus most of the applied voltage V_1 is dropped across the high voltage arm impedance Z_1 of the potential divider.

3.2 Types of Potential Dividers

There are mainly four types of dividers used for the measurement of impulse voltages depending upon the



F.I G 4 : SIMPLE VOLTAGE DIVIDER



F I G 5 : SIMPLE RESISTANCE VOLTAGE DIVIDER

rating of the voltage to be measured and its frequency.

(A) Resistance potential divider

(B) Mixed resistance - capacitance divider(Parallel-RC)

(C) Pure capacitor divider

(D) Damped capacitive divider. It is also called mixed series resistance capacitance divider.

3.2.1 Resistance Potential Divider[5]

They are of two types. For lower voltages resistor divider is analysed by neglecting the residual inductances and distributed stray ground capacitances. For higher voltages the high voltage arm of the divider becomes bigger in size and the distributed ground capacitances are also taken into account. Therefore two types of resistor dividers are -

(i) Voltage dividers neglecting stray inductance and capacitances.

(ii) Voltage dividers including their distributed stray ground capacitances.

3.2.1.1 Resistance Voltage Divider Neglecting Stray Ground Capacitance.

A resistive voltage divider consists of two resistors R_1 and R_2 in series where ordinarily R_1 is large compared to R_2[fig.5].

The divider's attenuation factor is the ratio of the voltage to be divided $V_1(t)$ and the measuring signal $V_2(t)$ that occurs across the low voltage terminals of the divider -

$$\text{Attenuation factor } a = \frac{V_1(t)}{V_2(t)} = \frac{R_1 + R_2}{R_2}$$

For measurements of fast impulse voltages the measuring signal is transmitted from the divider to a C.R.O. through a terminated coaxial cable. If very rapid transients exist and if the resistances have no distributed capacity and no self inductance, the voltages will divide proportionately, but it is necessary in order to avoid reflections at the oscillograph end of the cable to have a terminating resistor as the oscillograph end equal to the surge impedance of the cable. Extra resistances in series with the delay cable may be connected from the impedance matching point of view.

Fig. 6[a,b,c]shows the circuits under three different positions of impedance matching. Let us analyse the cct of fig. 6a.

$$\text{attenuation factor } a^{[4]} = \frac{R_1 + R_2}{R_2}$$

$$\text{or} \qquad \text{voltage divider ratio} = \frac{R_2}{R_1 + R_2}$$

The condition for impedance matching is -

$$Z_o = R_3 + \frac{R_1 * R_2}{R_1 + R_2} \qquad \ldots\ldots(1)$$

when $R_1 > R_2$

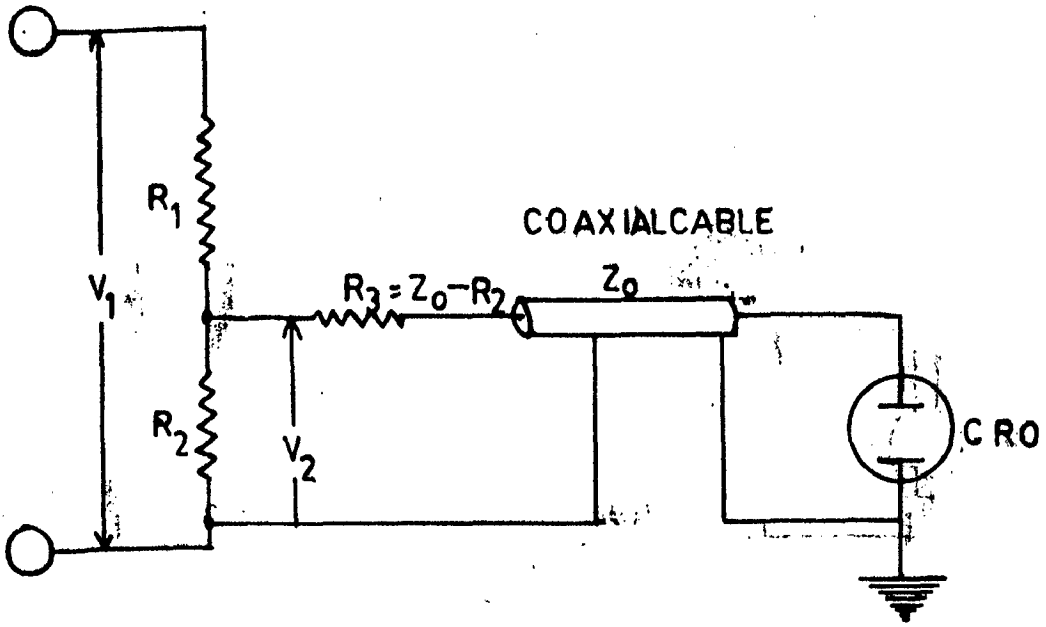


FIG 6a : IMPEDENCE MATCHING AT THE INPUT OF COAXIAL CABLE

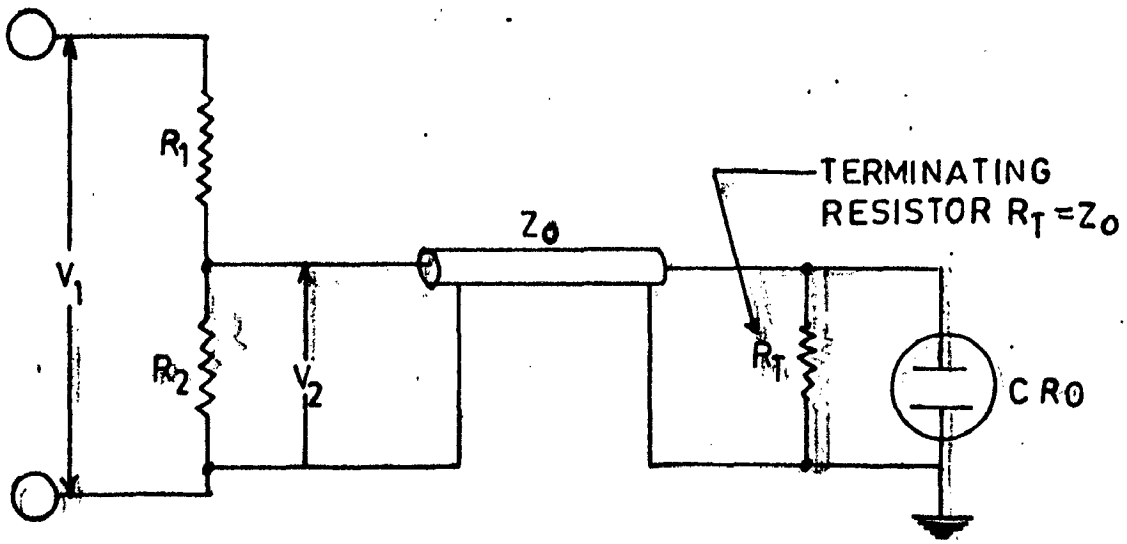


FIG 6b : IMPEDENCE MATCHING AT CRO END

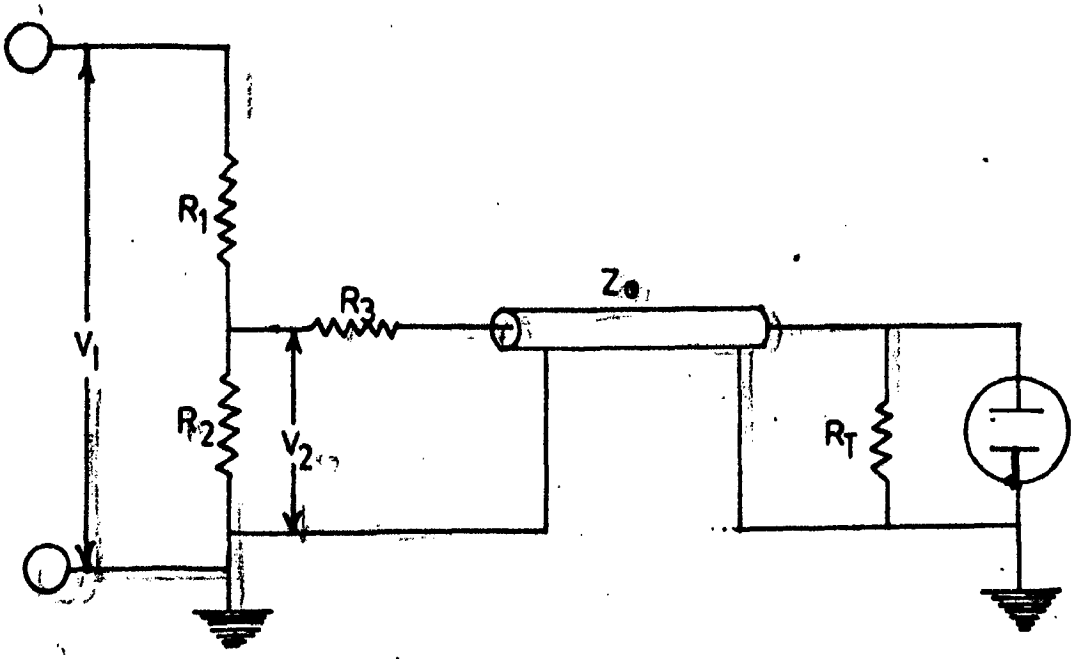


FIG 6c : IMPEDENCE MATCHING AT BOTH ENDS

$$Z_o = R_3 + \frac{R_2}{1 + \frac{R_2}{R_1}} \qquad \ldots\ldots(2)$$

or $$Z_o \simeq R_3 + R_2 \qquad \ldots\ldots(3)$$

$$\therefore \quad R_3 \simeq Z_o - R_2 \qquad \ldots\ldots(4)$$

equation(4) gives the value of the impedance for termination at the input of cable.

Let the Voltage across R_2 is be V_2

$$\therefore \quad V_2 = \frac{Z_1}{Z_1 + R_1} V_1 \qquad \ldots\ldots(5)$$

where $$Z_1 = \frac{R_2(Z_o + R_3)}{Z_o + R_2 + R_3}$$ [$(Z_o + R_3)$ and R_2 being in Parallel]

i.e. $$Z_1 = \frac{R_2}{2Z_o}(Z_o + R_3)$$

from eq.5

$$V_2 = \frac{R_2(Z_o + R_3)}{2Z_o(Z_1 + R_1)} V_1 \qquad \ldots\ldots(6)$$

Let the voltage travelling towards the delay cable be V_3

$$V_3 = \frac{Z_o}{Z_o + R_3} V_2 \qquad \ldots\ldots(7)$$

Putting the value of V_2 from eq.(6) in eq.(7)

$$V_3 = \frac{Z_o}{(Z_o + R_3)} \cdot \frac{R_2(Z_o + R_3)}{2Z_o(Z_1 + R_1)} \cdot V_1$$

$$V_3 = \frac{R_2}{Z_o(Z_1 + R_1)} \cdot V_1$$

i.e. voltage arriving at the open C.R.O. plates

$$V_3 = \frac{1}{2}\left(\frac{R_2}{Z_1 + R_1}\right) V_1 \qquad \ldots\ldots(8)$$

Since at the C.R.O. plates, electrically it is open circuited, the total voltage across the plates would be $2V_3$. i.e.

$$V_3\,(\text{total}) = \frac{R_2}{Z_1 + R_1} \cdot V_1 \qquad \ldots\ldots(9)$$

The reflected wave is almost completely absorbed at the potential divider end. In practice

$$Z_1 + R_1 \simeq R_1$$

$\therefore$ Voltage across deflecting plates $\simeq \frac{R_2}{R_1} \cdot V_1$

For Circuit b [4]

For this circuit

$$Z_o = R_4 \text{ and } m = \frac{Z_o R_2}{Z_o(R_1 + R_3) + R_1 R_2}$$

For Circuit c

It is observed that for impedance matching at both ends -

$$Z_o = R_4 \; R_T$$

also $$Z_o \simeq R_3 + R_2$$

and $$m = \frac{R_2}{R_1 + R_2}$$

i.e. when cable is terminated at C.R.O. end with a value of resistance equal to surge impedance of cable, the amplitude of the divided wave will be reduced to half.

When the duration of the surge is less than 1 μ sec. a resistor divider may give large errors due to stray capacitance. Therefore it is necessary to analyse the effect of distributed ground capacitance.

3.2.1.2 Resistance Dividers Including Stray Ground Capacitances[5] [6]

At higher voltages the dimensions of R_1 are significantly increased and the effect of distributed stray ground capacitances can not be ignored. If the potentiometers have distributed capacity, they will not divide the voltage proportionally at all instants.

These capacitances cause the step response to possess a gradual approach to its final value, i.e. inherently large rise-times and response times. The equivalent cct for a divider with extended dimensions is shown in fig. 7.

(1) The high voltage arm is assumed to consist of N elementary resistors $R_1' = \frac{R_1}{N}$.

(2) Each of these elements possesses its own parallel stray capacitance $C_p' = C_p \cdot N$.

(3) The undesired elementary stray ground capacitances $C_g' = C_g/N$ arise from the inherent electric field between each element and the environment (floor, walls, nearly high voltage equipment) at ground potential.

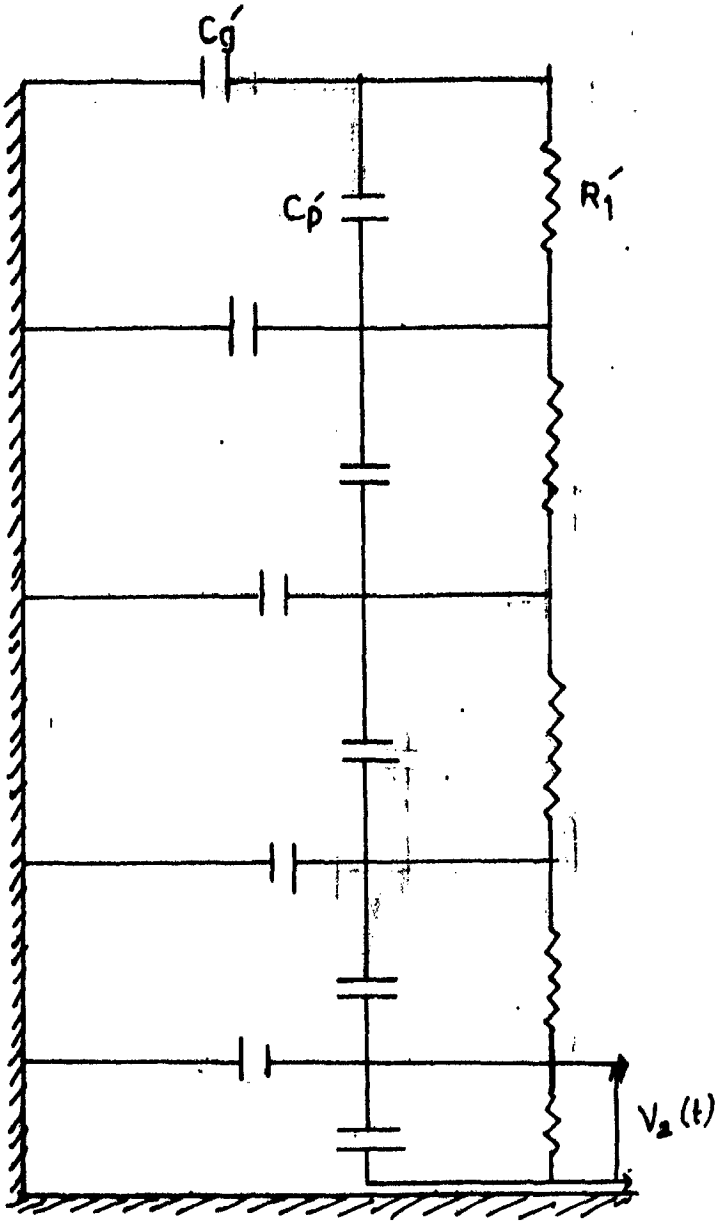


FIG 7 : EQUIVALENT CCT OF RESISTANCE VOLTAGE DIVIDER WITH DISTRIBUTED STRAY GROUND AND PARALLEL CAPACITANCES

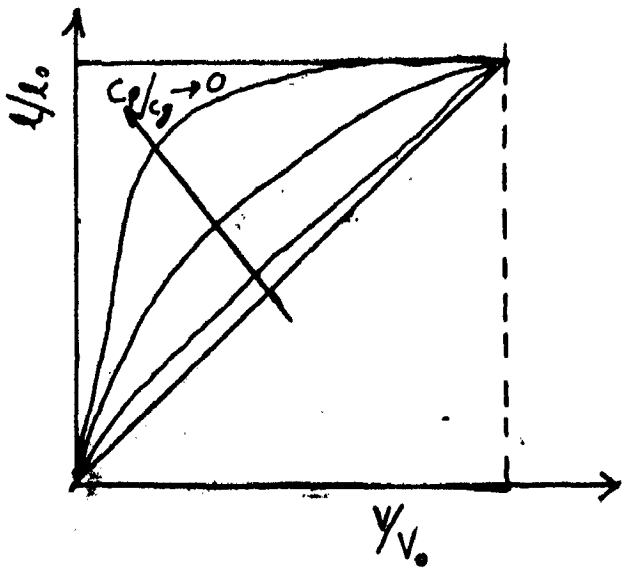


FIG 8 : FREQ-DEPENDENT NON LINEAR VOLTAGE DISTRIBUTION

The values of distributed ground capacitance are 10 to 20 PF/m in general.[5] In reality the ground capacitance per unit length will decrease from the top to the bottom of the divider, but, as theoretical and experimental investigations have shown, an uniform distribution may frequently be assumed without excessive error even for dividers of some meter's length.

A voltage step arriving at the divider must charge the ground capacitances Cg/N. The required charging current delivered from the source diminishes from the divider top to its grounded end. This loss produces a non-linear voltage distribution that is frequency dependent along the divider becoming more non-linear as the ratio Cp/Cg grows more unfavourable i.e. smaller as shown in fig.8.

After a period during which all ground capacitances are charged, a linear voltage distribution occurs in accordance with the ohmic resistance per unit length. The divider acts like a ripple reducing RC filter chain which attenuates especially the high frequencies, thereby increasing the output voltage rise-time.

To avoid this detrimental influence, the capacitive voltage distribution must be adapted to the ohmic voltage distribution or vice verca. These measures lead to resistive capacitance mixed voltage dividers.

3.2.2 Mixed Resistive - Capacitive Voltage Dividers

It has been noted that dividers with extended dimensions exhibit a nonlinear frequency dependent voltage distribution because of the diminishing charging current for the distributed stray ground capacitances. According to Elsner[5] the influence of distributed ground capacitances may be eliminated by enlarging the parallel capacitances C'_p. This is achieved by connecting additional capacitors in parallel with the elementary stray parallel capacitances C'_p. From fig. [8] it is observed that an ideal frequency response is achieved if the ratio C'_p/Cg becomes infinite[5], but in that case the divider would be useless because of its high loading effects. Elsner assumes a ratio $C'_p/Cg > 3$ to be sufficient. Thus a divider consisting of ten stages each having a ground capacitance $Cg = 10$ PF requires a total parallel capacitance $C'_p = 300$ PF and hence an elementary parallel capacitance $C'_p = 3000$ PF per stage. This comparatively high parallel capacitance may cause serious loading effects which restrict the application of resistive - capacitive mixed dividers. In addition, high voltage capacitors in order of 1000 PF exhibit large stage inductances which can not be neglected.

A mixed parallel RC arrangement divider behaves as a resister divider for slow transients and as a pure capacitive divider for fast surges. The parallel capa-

citances branch provides the path for most of the current flow at high frequencies. Hence it is natural to consider the divider when ohmic branch is not there at all i.e. to consider the dividers which are purely capacitive for fast surges.

3.2.3 Capacitance Voltage Divider

These dividers are of great advantage with systems for very high voltages and high source impedances because capacitance divider can be made of high impedance so that loading of the source may be negligible. The typical potential divider of capacitance type is shown in fig. 9 a.

$$\text{The divider ratio} = n = \frac{C_1}{C_1 + C_2 + C_k}$$

where C_k = capacitance of the delay cable.

When C_k is negligible in comparison with C_1 or C_2

$$n = \frac{C_1}{C_1 + C_2}$$

The voltage across the delay cable is $\frac{C_1}{2(C_1 + C_2)} V_1$. By doubling of the voltage wave at the open circuited end of the C.R.O., we have the voltage across the C.R.O. plates equal to $\frac{C_1}{C_1 + C_2} V_1$. The reflected wave is absorbed with negligible reflection at the input end. After infinite time, the system behaves as a pure capacitance and voltage across

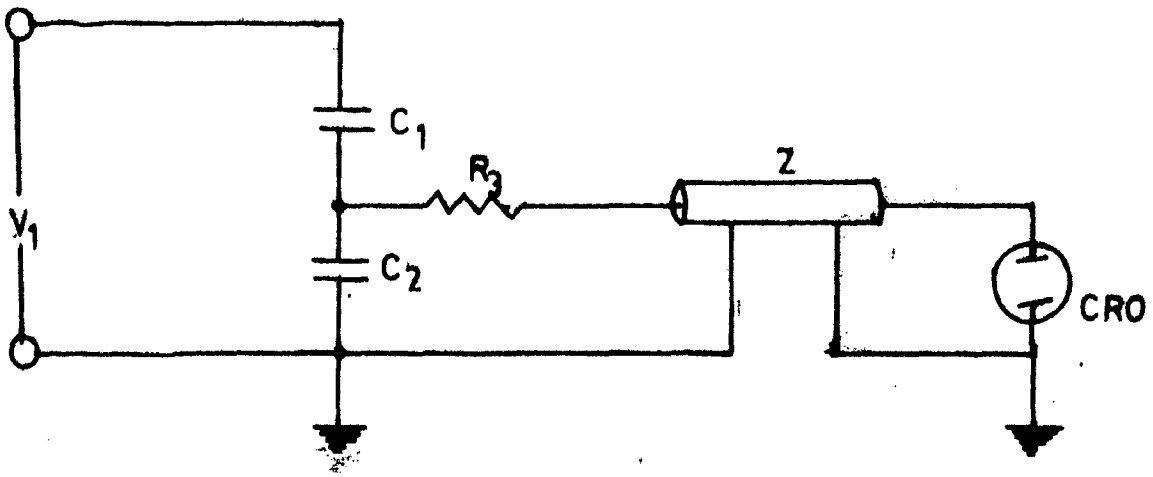


FIG 9a:CAPACITANCE DIVIDER

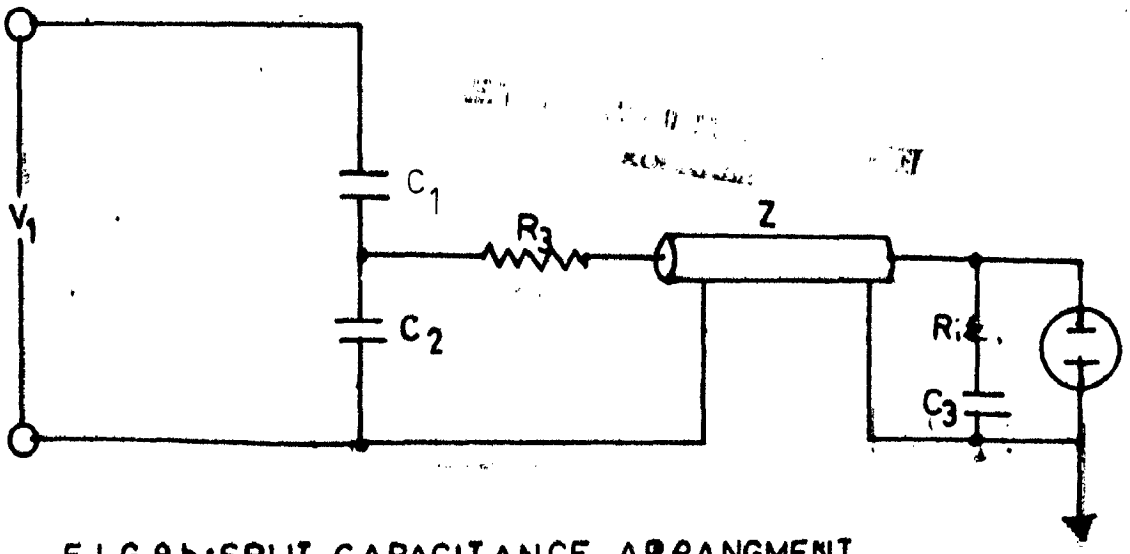


FIG 9b:SPLIT CAPACITANCE ARRANGMENT

the capacitance C_g gets stabilized. The ultimate value of the voltage across the deflecting plates of C.R.O. would be given by $\left[\frac{C_1}{C_1+ C_2+C_k} \right]V_1$ because of the delay cable. Thus the delay cable introduces a voltage difference equal to -

$$V_2- V_3 = \frac{C_1}{C_1+ C_2} V_1 - \frac{C_1}{C_1+ C_2+ C_k} V_1$$

$$= \frac{C_1C_kV_1}{(C_1+ C_2)(C_1+ C_2+ C_k)}$$

where V_3 = voltage across the deflecting plates of C.R.O.

If $C_2 >> C_1 >> C_k$

$$V_2- V_3 = \frac{C_1C_kV}{C_2^2}$$

The voltage error $\left[\simeq \frac{C_1C_kV_1}{C_2^2} \right]$ would be reduced by transferring part of the low voltage capacitor to the C.R.O. end and connecting it in series with a resistance equal to surge impedance of the delay cable. This is known as the split capacitor arrangement.[7]

The condition for splitting the capacitor is -

$$C_1+ C_2 = C_3+ C_k$$

For this condition, the initial and final ratios would be the same.

For capacitive dividers and for very high voltages, the primary capacitance can not be assumed a lumped element but must instead be treated as transmission line.[22]

An eq. circuit is shown in fig. 10 in which the high voltage capacitance C_1 consists of a large number of elementary capacitors in series. The distributed ground capacitances cause a ratio error in capacitance dividers also, but this is constant rather than freq. dependent as in resistive dividers.

The attenuation factor for rapid transients as well as for steady state may be calculated as[5]

$$\frac{V_1(t)}{V_2(t)} \simeq \frac{C_1 + C_2}{C_1}\left[1 + \frac{C_g}{6C_1}\right]$$

This ratio exhibits a constant frequency independent error. For example when $C_1 = 3C_g$ there will be a 5 % error compared to the given nominal ratio.[5]

1. The above equation is valid only upto 1/MHz freq.

2. At higher frequencies residual inductances can not be neglected.

3. At higher frequencies ratio of capacitive divider is influenced by environmental effects, including divider height, diameter and distance from a grounded wall.

The capacitor divider's ratio is independent of frequency and thus appears to represent the ideal voltage divider for fast pulses. This is true only for the pure divider. But the dividers are usually connected to the source by leads that have inherent residual

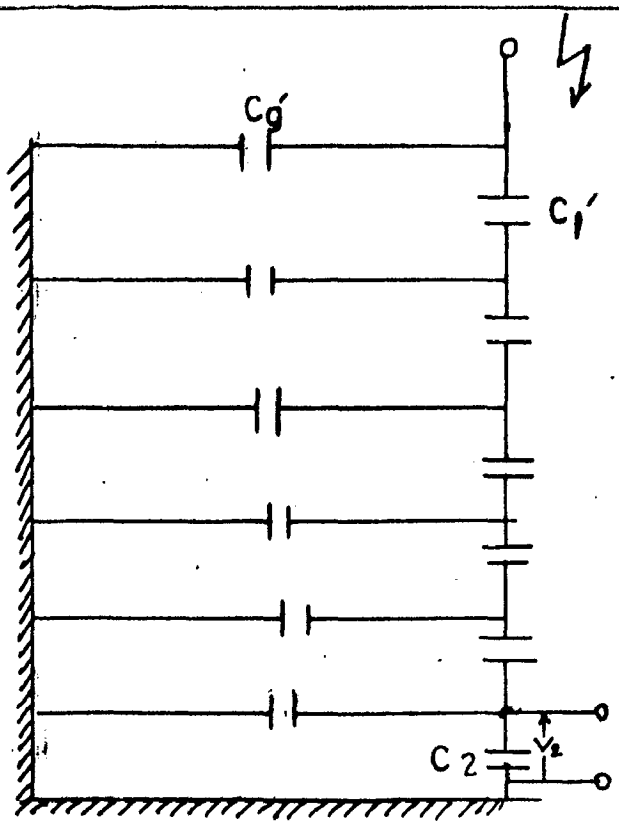


FIG 10 : PURE CAPACITANCE DIVIDER

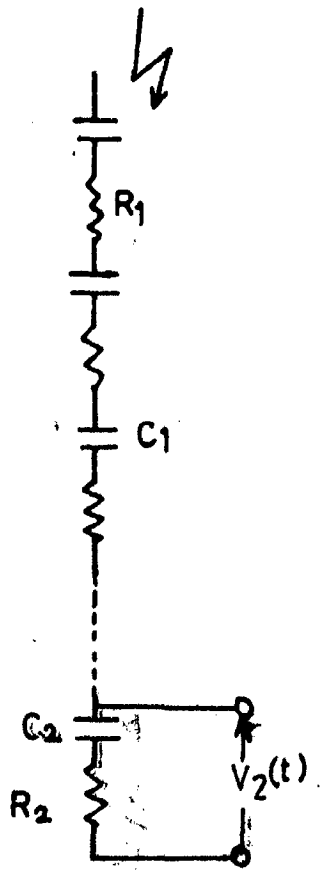


FIG 11 : DAMPED CAPACITIVE DIVIDER

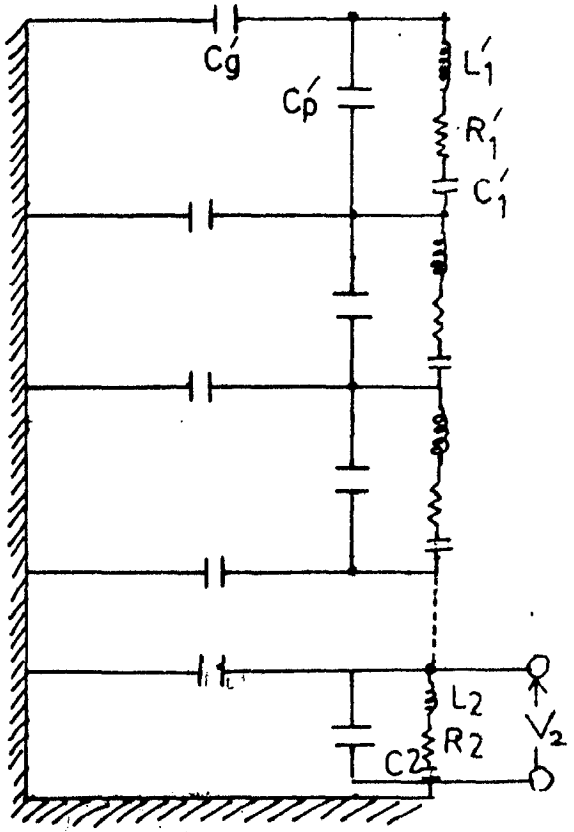


FIG 12 : DAMPED CAPACITIVE DIVIDER WITH STRAY INDUCTANCE AND CAPACITANCE

inductances. These inductances together with the capacitances of the divider, form a series rasonent circuit, causing excessive oscillations in the step response. At relatively low voltages upto some 10 KV, lead inductance may be kept very low by using minimum lead lengths and coaxial lead design. The natural frequencies then occur far beyond the upper freq. limit of the oscilloscope and may thus be neglected. Of course, medium and high voltages do not permit coaxial leads. Oscillations free behaviour may then be achieved by inter connecting damping resistors in series with the high voltage leads and the divider. However, this attenuated not only oscillating frequencies but also high freq. components necessary for short response time.

Because of the low losses in the divider, reflections at both of its ends cause travelling wave oscillations that cannot be attenuated by a lumped damping resistor at the high voltage terminal.[18] Until recently, existance of travelling wave oscillations limited the use of pure capacitance impulse dividers. But by distributing the lumped damping resistor uniformly along the high voltage arm, these oscillations and the ringing caused by the lead inductances may be sufficiently attenuated without affecting the excellent high frequency properties of the original pure capacitive divider.

3.2.4 Damped Capacitive Divider

The circuit of a damped capacitive divider is shown in fig. 11 in which the damping resistors are distributed along the various capacitance units. This arrangement is suitable for tests involving super imposed power frequency and surge voltage measurements[7]. It has the advantage of having finite impedance at infinite frequency. The response of such an arrangement on fast surges corresponds to that of a pure resistor divider.

The equivalent circuit of a damped capacitive divider considering the residual inductances and stray ground capacitances may be shown as in fig. 12.

3.3 Sources of Error and their Elimination

The essential requirements for the divider is that the wave-shape of the voltage to be measured should be faithfully reproduced on the oscillograph with a reduction ratio which can be accurately determined.

The chief sources of error common to all types of dividers are[6]- [Refer Fig 13]

(1) Residual inductance in any resistance or capacitance element. Oscillations in wavefront are caused by residual inductance in the H.V. arm and inductance loops in the connecting leads between the low and high voltage arms of the dividers. [$L_{R'_1}$ and $L_{e'_1}$ in Fig 13]

(2) Stray capacitance:

(a) From any section of the divider to ground. [$C_{g'}$]

(b) From any section of the divider to the high voltage lead. [C_{h_1}, C_{h_2} ---]

(c) Between sections of the divider.

(3) Impedance drop in the ground return lead from the divider resulting from extraneous ground currents flowing in this field.

(4) Impedance drop in the connecting lead between the dividers and test object.

(5) Attenuation and distortion errors due to measuring cable.

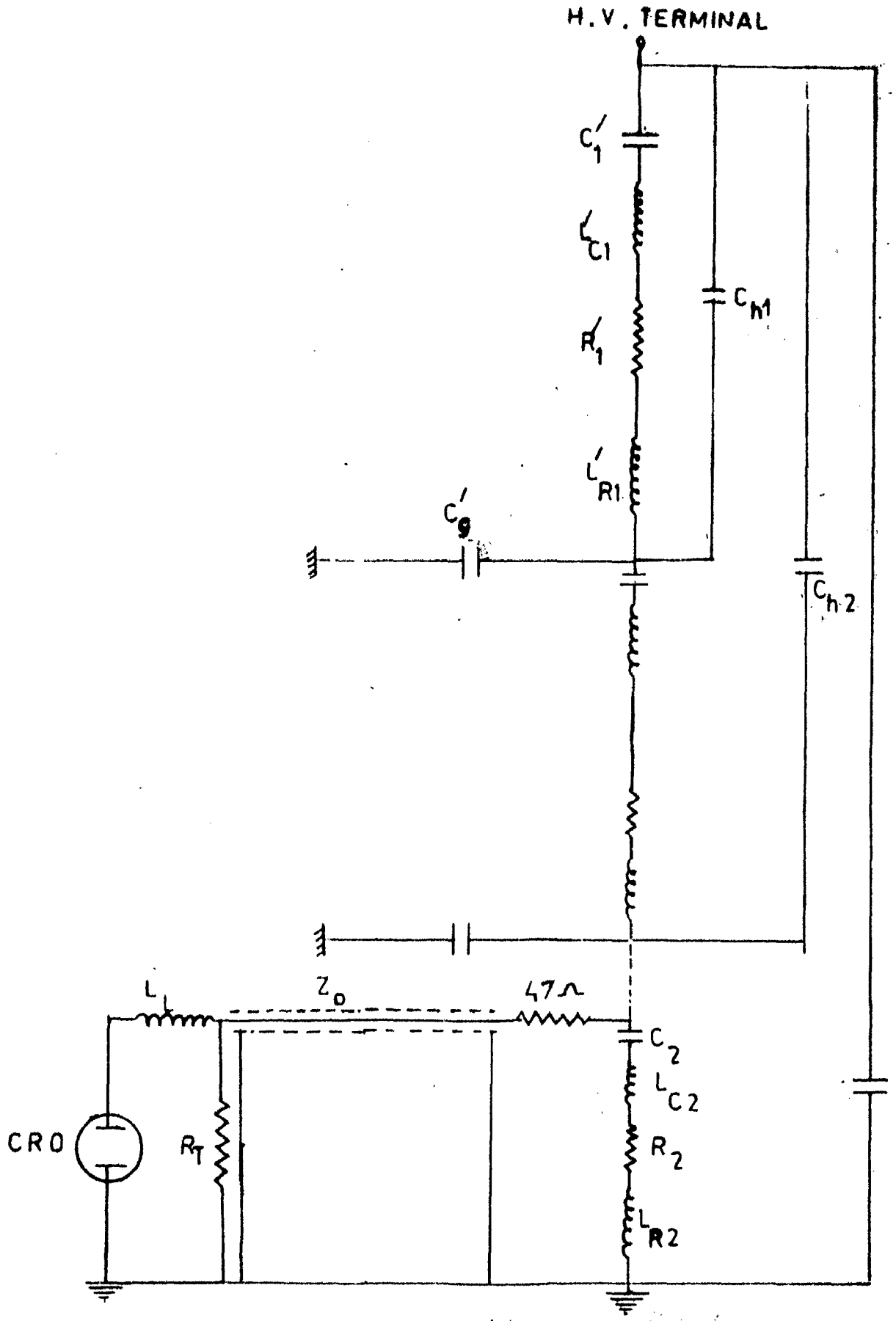


FIG 13: COMPONENTS GIVIGING ERROR TO THE DIVIDER RATIO

(6) Errors due to cable termination.

(7) Errors due to layout of test set-up. The test object is generally located not very close to the divider in order to avoid the possibility of the divider distorting the field near the object. Under these circumstances the inductance of the loop formed by the divider and the connections to the test object may cause considerable errors.

(8) In practical impulse testing facilities, there is an interaction between the generating system and the measuring system that precludes the possibility of generating an impulse voltage of simple shape across a test object. The actual test voltage will have some distortion[12][13]. This change is due to the interactions of the generator impedance and the reflections from the impulse voltage divider[14].

(9) Location of the cathode ray oscillograph near the divider for direct connection across the low voltage arm is undesirable[15], since this introduces stray capacitance and inductive effects on the cathode ray beam.

3.3.1 Effect of Earth Capacitance

Davis and Boudler[7][8] have studied the performance of a resistive divider on impulse voltages and have shown the effect of the stray capacitance on the recorded wave shape. Referring to fig. 7 the effect of earth capacitance is twofold -

(1) The effect of increasing time constant R_1C_g is to lengthen the 'front' and 'tail' and to reduce the peak amplitude.

(2) For a given value of R_1C_g, the error in the maximum amplitude increases as the tail length decreases.

Earth capacitance effect is shown in fig. 14 which is self explanatory.

The influence of earth capacitance on the response of a resistive divider may be removed by placing the divider in a uniform field. This may be accomplished by -

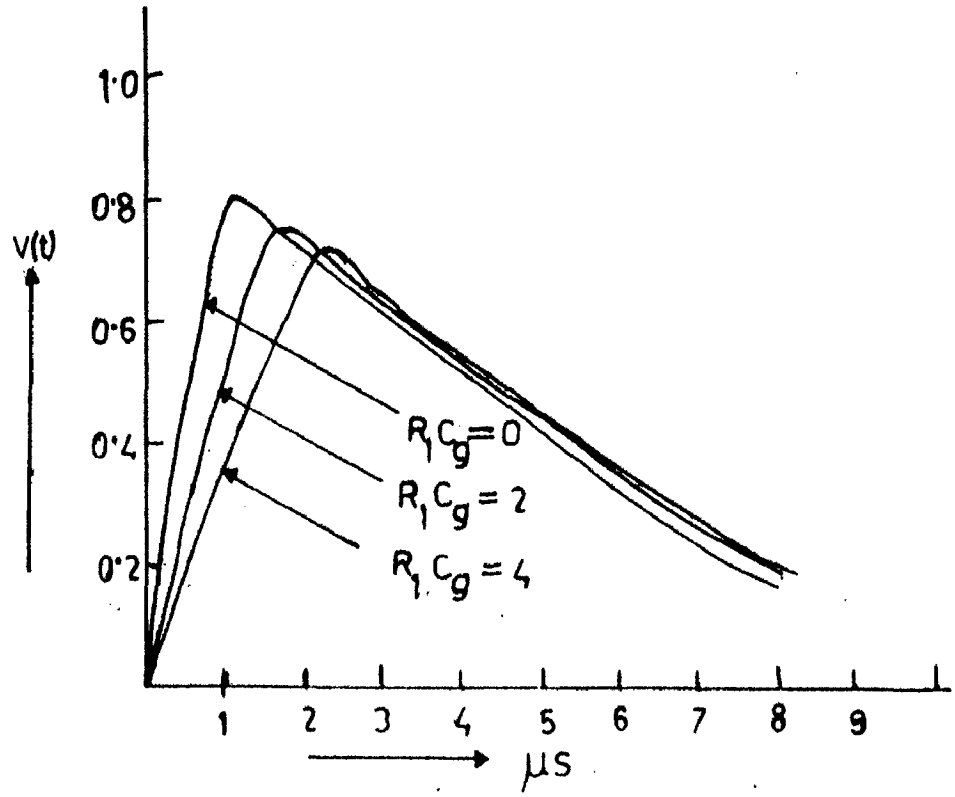
(i) Locating the divider in close proximity to the surge generation.

(ii) Surrounding the divider with a resistive screen.[20]

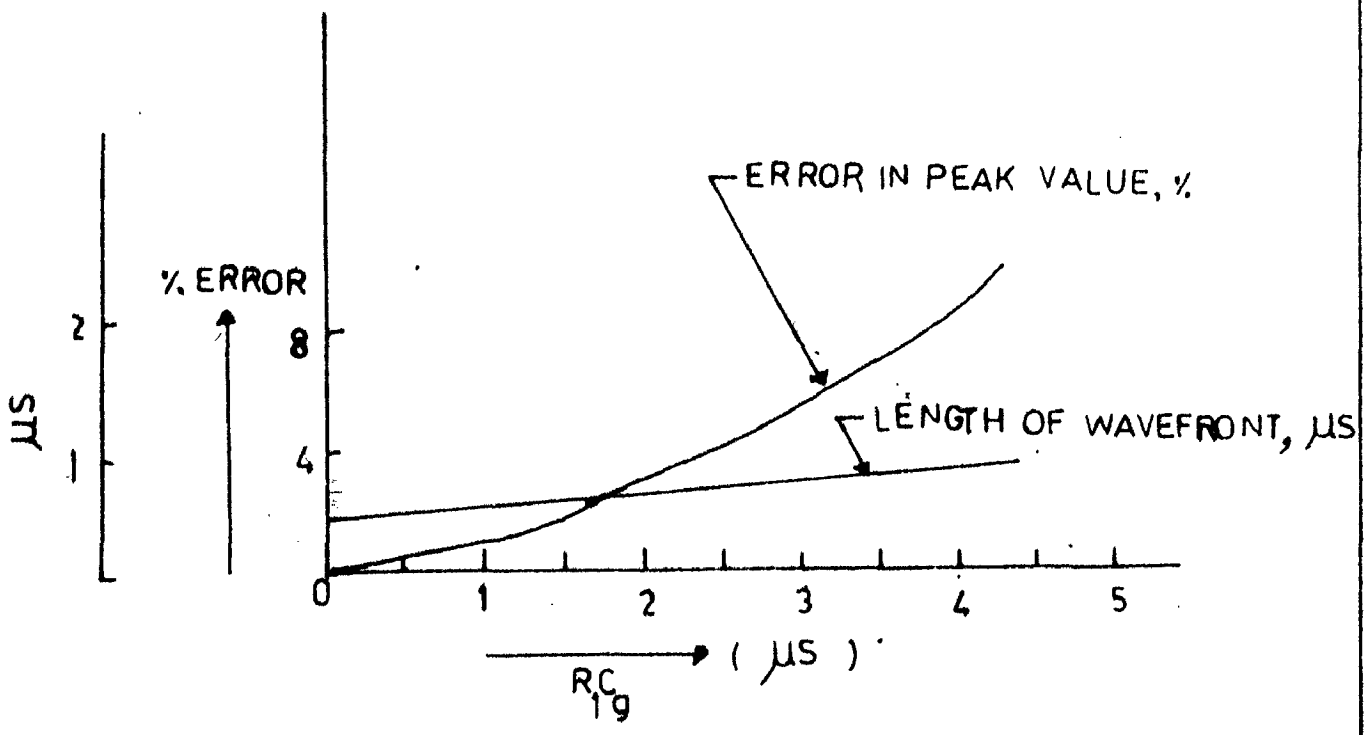
(iii)Providing a capacitive screen from an extended metal electrodea at the high voltage end.

3.3.2 Effect of Inductance of Resistance and Capacitance Elements and Connecting Leads.

Fisher[10] has described methods for improving the response of practical dividers. These include the use of compensatory devices in the H.V. arm and wave-shaping networks in the L.V. arm. Fig. 15 shows the improvements obtained in the step response of a 21000 ohms resistance



(a)



(b)

FIG 14 : EFFECT OF EARTH CAPACITANCE ON DIVIDER RESPONSE

divider by using a line shield and a damping resistor. The low voltage arm was the 75 ohm deflection cable and its non inductive terminating resistor.

In the response with a simple shield (fig. 15b) severe oscillations are produced by the inductance of the connecting lead and the terminal capacitance of the shield and the H.V. arm. In fig. c these oscillations have been damped out by connecting a 500 ohms resistor at the test piece end of the line lead while in fig. (d) the oscillations are damped out by placing the 500 ohms resistor between the H.V. arm and the shield. Best results are obtained in the arrangement of fig. (d) as only the capacitance of the shield is fed through the resistor and in this position the damping resistor has no effect on the divider ratio. By arranging the shield in the manner shown in fig. (d), the rise time was improved from .091 μ sec. to .023 μ sec.

The response of a divider can also be improved by using a suitable wave-shaping network in the low voltage arm. If the response voltage, as developed across a non inductive resistor, rises exponentially as in fig. 16a the step response may be improved by adding an inductor in series with the low voltage resistor. Fig. 16 (a) and (b) show the response of a 10000 ohms divider suitable for 3.5MV. The H.V. arm consisted of sixty seven resistor cards each holding 8 inch of resistance windings. The total inductance of the H.V. section was about 270 μH

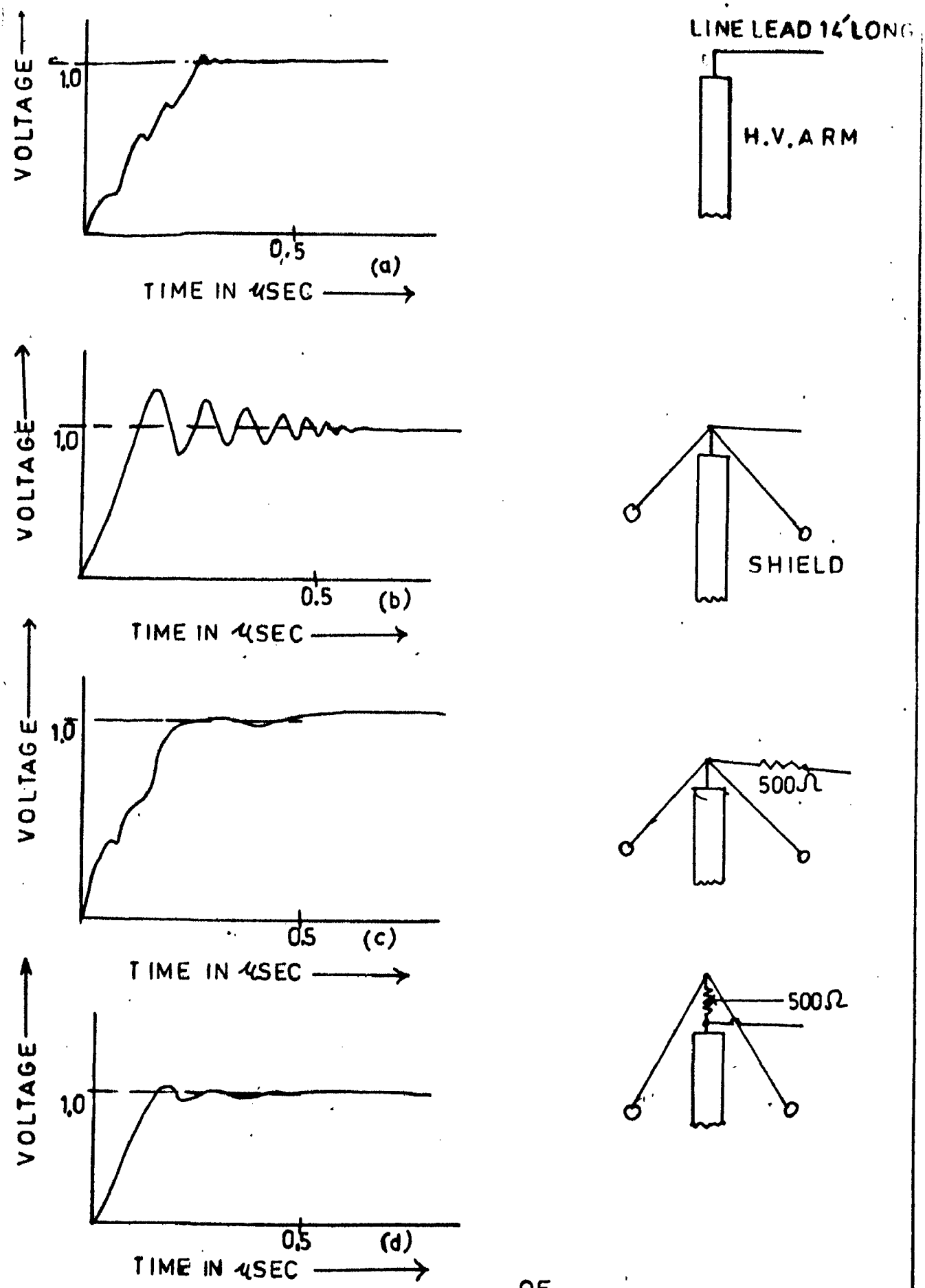
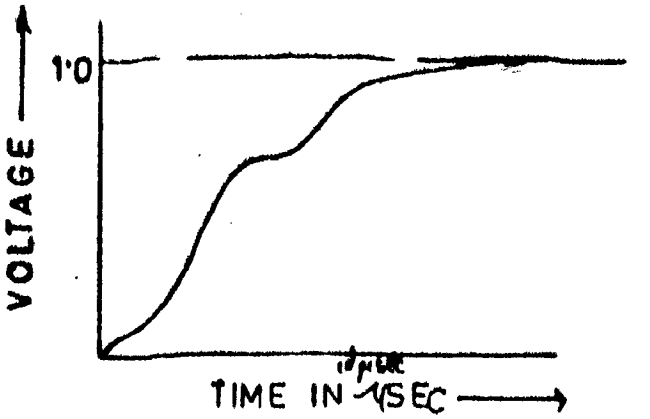


FIG 15 : EFFECT ON STEP RESPONSE OF LINE SHIELD CONNECTIONS



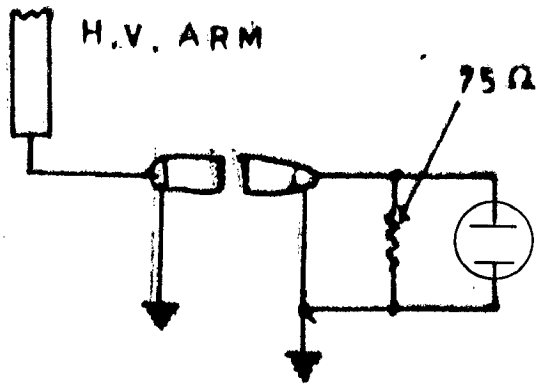
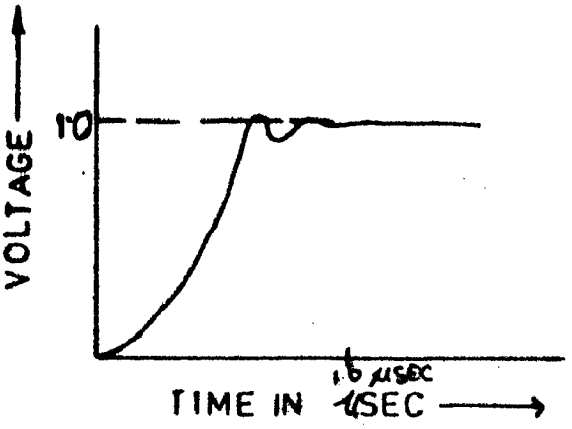


FIG 16a: NON INDUCTIVE VOLTAGE ARM



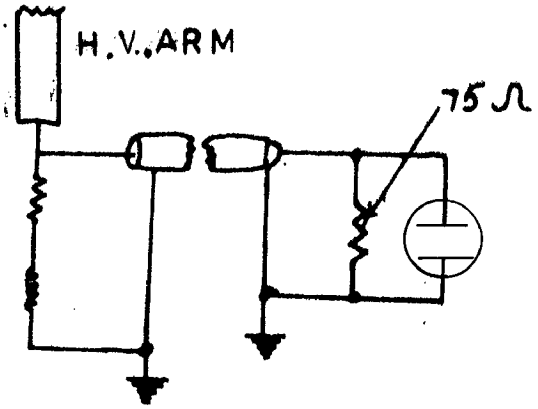
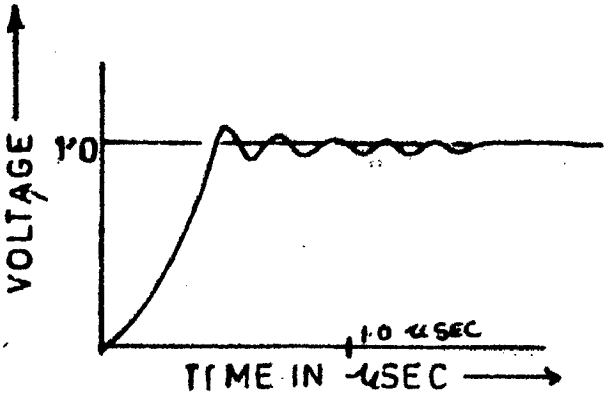


FIG 16b: INDUCTIVE LOW VOLTAGE ARM



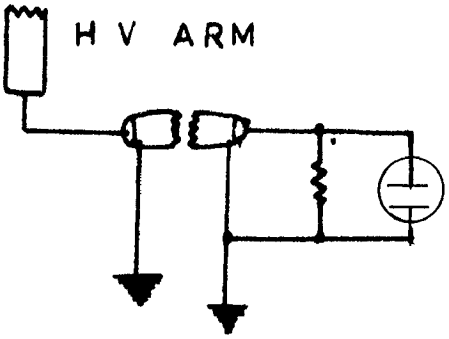
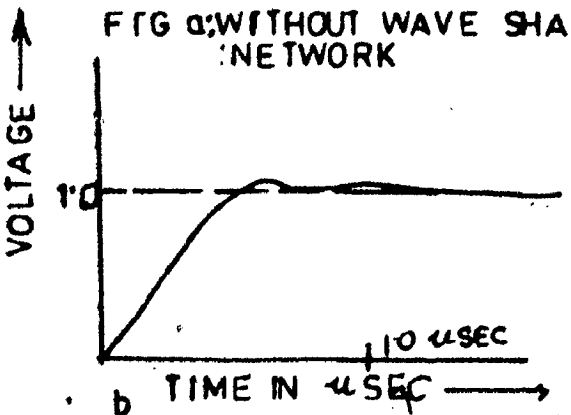


FIG a: WITHOUT WAVE SHAPING NETWORK



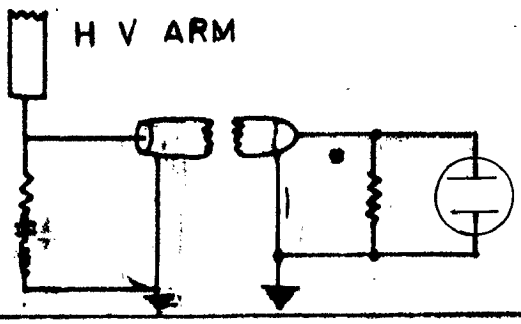


FIG 17: b WITH WAVE SHAPING NETWORK

and the total capacitance to ground was about 150 μμF Fig.(b) shows the response where a 5 ohms non inductive resistor in series with an inductance of .4 μH was used as the low voltage arm. This arrangement improved the rise time of the response from .33 μ sec. to .14 μ sec. If the divider was an oscillatory step response improvement in the general shape of the response (not in the rise time) can be obtained by the circuit shown in fig. 17.

3.3.3 Effect of Source Impedance of Step Voltage Generator.

The output voltage of a pulse generator under capacitive loading depends upon its internal impedance.[5] For a very small source resistor R_i (fig. 16 A) the voltage step will be affected by ringing, whereas a very high value increases the rise-time of the output voltage. Therefore we must have a critical value of source impedance so that neither there are any oscillations nor any dropping in the output. If the function generator output is critically damped, error in the response of the divider will be minimised.

3.3.4 Errors due to Cable

An ideal cable is one which has no losses and whose surge impedance does not vary with frequency[11]. However all cables have some attenuation and their surge impedance varies with frequency. The sources of cable

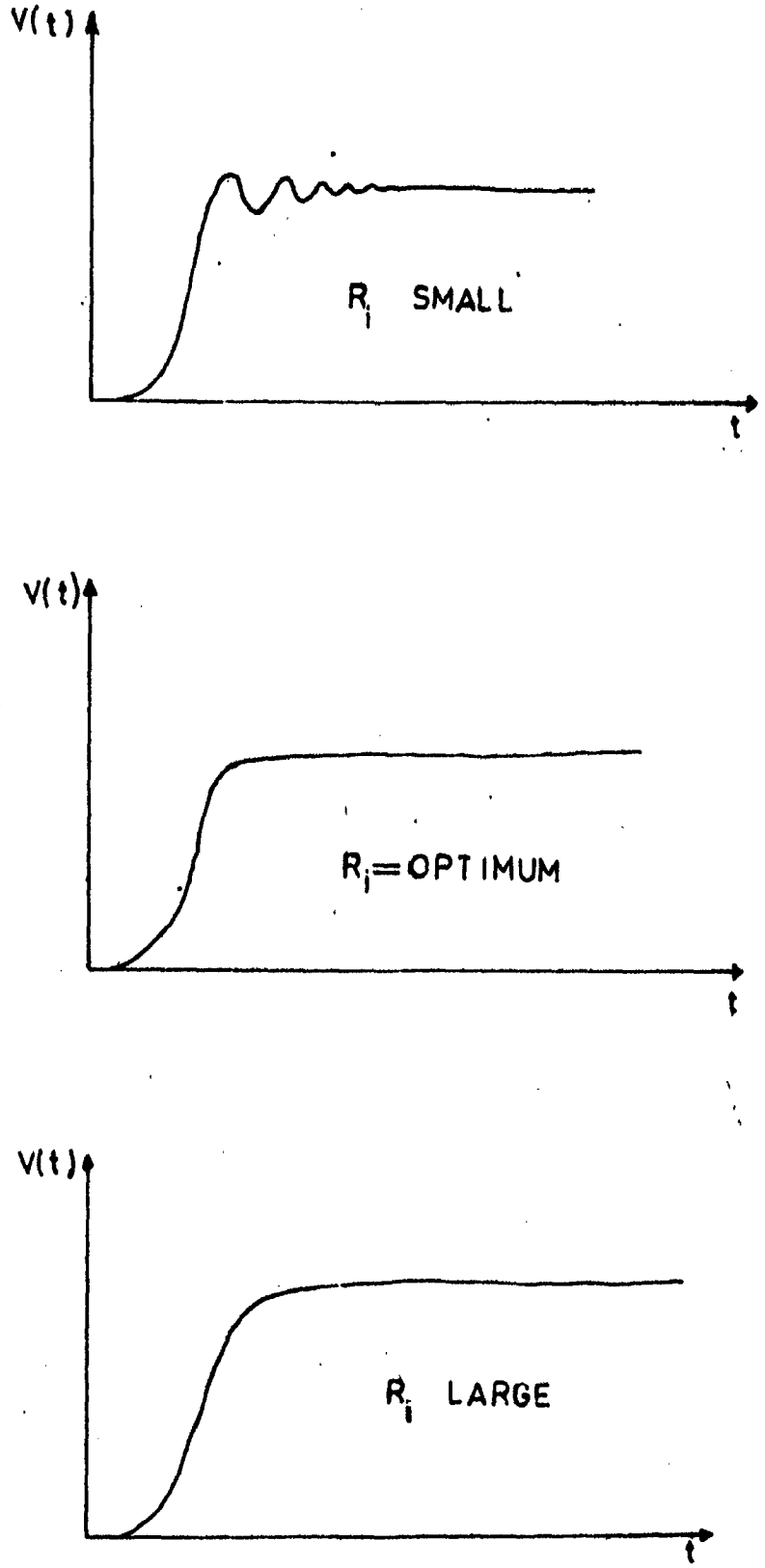


FIG 18A : OUTPUT-VOLTAGE OF PULSE GENERATOR AS A FUNCTION OF SOURCE IMPEDANCE

losses are the resistance of the central conductor and outer sheath of conductance and dielectric hysteresis in the insulating medium used. Losses are usually expressed as attenuation in decibles per 100 ft. at a fixed frequency and in general the logarithm of attenuation increases directly with the logarithm of freq.

The error in the peak value and the waveform caused by the cable attenuation can be calculated by computing the correction factor for the error in peak measurements by measuring values of peak voltage at three different lengths L, 2L and 3L. The decrease ΔV in peak voltage when the length is changed from L to 2L should be the same as that obtained when the cable length is increased from 2L to 3L. The average of the two values of ΔV is added to the peak voltage obtained when a cable of length L is used.

Bemley[9][18] has studied the effect of cable termination. When the terminating resistor R_T is not equal to the surge impedance of the cable (neglecting C) the voltage across R_T is [fig. 6b]

$$V_3 = \frac{2R_T}{R_T + Z_o} \left[1 + (a_1 a_2)\, 2T + (a_1 a_2) + 4T^2 \right] \quad \ldots(10)$$

where $a_1 = \dfrac{R_1 - Z_o}{R_1 + Z_o} \simeq 1$ If $R_1 \gg Z_o$

~~If $R_1 \gg Z_o$~~

$$a_2 = \frac{R_T - Z_o}{R_T + Z_o}$$

V_1 = applied voltage

V_2 = voltage at the input end of the cable

T = delay cable length in micro-seconds

(A) When $R_T = Z_o$

Then $a_2 = 0$, there are no reflections and $V_2 = V_3$.

(B) When $R_T \neq Z_o$

Then $a_2 \neq 0$ and there will be reflections and consequent error which will be a function of Z/R_T. Equation 10 is plotted in fig. 18 for the three first reflections as functions of Z/R_T.

The cable surge impedance varies with frequency and a fixed value terminating resistor cannot prevent reflections[11] due to different types of surge. The change in impedance with freq. is introduced by the change in cable inductance caused by non uniform distribution of current in the central conductor and the sheath as the freq. is increased. This is called skin effect which also courses a change in resistance with freq. Thurston show that the surge impedance of a nominal 50 ohms polythene cable has a constant value of 55 ohms for frequencies 100 kc/s and below. Between 100 kc/s and 10 Mc/s there is a gradual change in its impedance from 55 ohms to 50 ohms and the impedance remains at this value for higher frequencies. If such a cable is terminated in a 50 ohms for

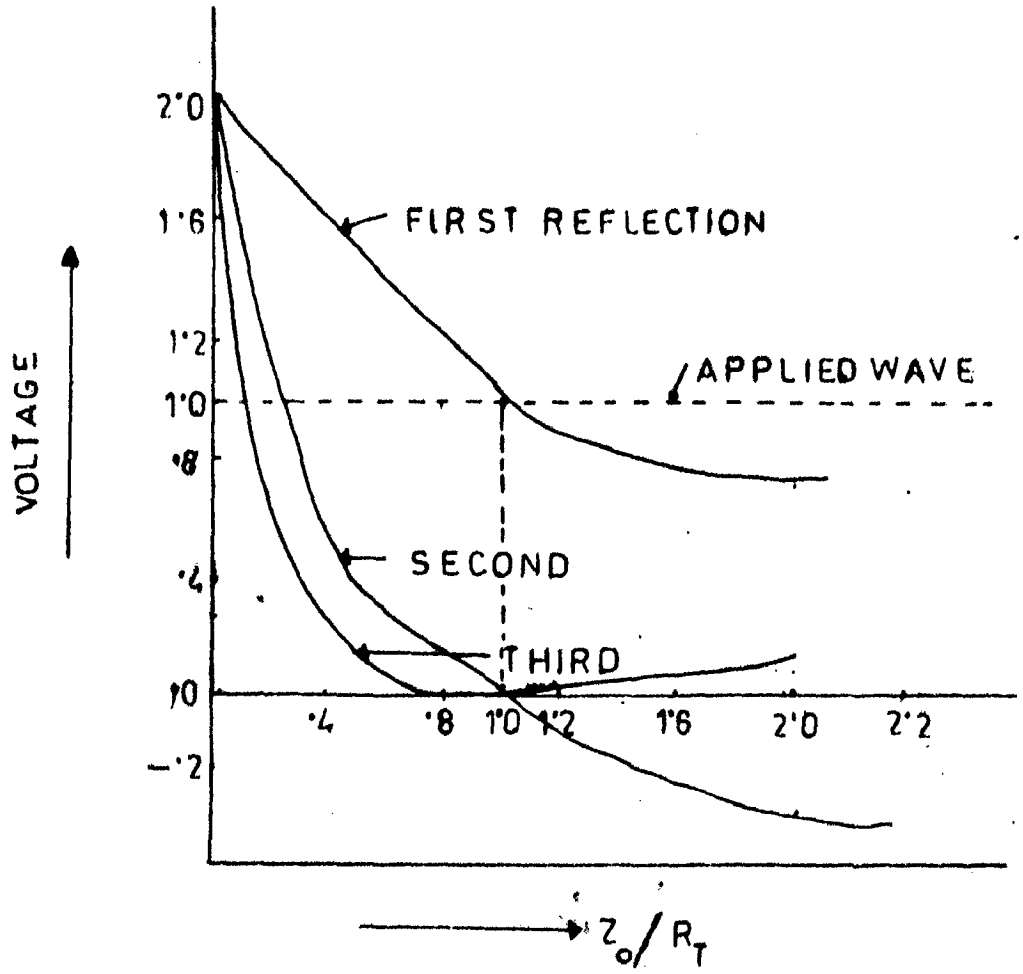


FIG 18B; EFFECT OF TERMINATION

resistance, there is a mis-match of 5 ohms for all frequencies below 100 kc/s and an error of about 5 %, would be introduced when measuring slowly rising surges, square waves or 1.5/40 μ sec. full surge waves. If, say, a 55 ohms terminal resis-tance is used, the error in the measurement of slowly rising surges or full waves would be reduced, but an error of about 5 % would be introduced when measuring steeply rising chopped waves.

4. DESIGN OF THE DIVIDER

4.1 General Design Aspects

Since the high voltage arm of capacitance dividers designed for very high voltages consists of many single capacitors with relatively large capacitance values, considerable stray inductance must be assumed to occur.[5] Although the high voltage arm is frequently treated as a lumped pure capacitance, it is actually a transmission line. As is well known from transmission line theory, travelling wave oscillations resulting from multiple reflections will occur if the line has low attenuation and unterminated ends.[11] Both conditions are fulfilled in capacitive dividers there is little attenuation in the line by losses in the single capacitance and their leads, and one end of the line is short circuited by C_2 while the other end is at least badly matched. Thus a voltage step at the high voltage terminal will travel through the high voltage arm, be reflected at the short circuited end, travel back to the high voltage terminal, be reflected again and so on. Depending on the losses of the line, more or less attenuated travelling wave oscillations will occur. The fundamental frequency of the oscillations, which may be of the order of 10 MHz is calculated. Because these oscillations may not be attenuated by lumped resistors at the input of the divider, the continuously damped capacitive voltage divider as shown in fig. 11 is used.

Suitable attenuation is achieved if the travelling waves that enter the high voltage terminal decay to negligible value during their first transit so that they cannot cause serious reflections. Zaengle evaluated the required attenuation experimentally and theoretically as [5]

$$R = 3 \text{ to } 4\sqrt{\frac{L}{C_g}}$$

Hence, the total ohmic resistance of the divider should be 3 to 4 times greater than the surge impedance $Z_0 = \sqrt{L/C_g}$ of the divider's transmission line representation. At very high frequencies the capacitive reactance of the high voltage arm is greatly decreased, permitting the divider to act like a pure low ohmic voltage divider. The minimum upper freq. limit may then be calculated from the eqn. for the bandwidth of resistive voltage divider

$$B = \frac{1.46}{R.C_g}$$

which assumes an exponential rise of step response. However, since attenuation will be chosen for the critically damped case, a slightly greater bandwidth is found in practice. The bandwidth can be accurately determined from the rise time of the experimentally measured response to a step input.

The practical realization of impulse voltage dividers requires components with low residual inductance

exclusively (non-helical and fabric woven resistors, broad band contactors and disc type capacitors and so on). Total inductance must be reduced by skillful arrangement of the system and by series parallel connections of components. In [redacted] fig. 11 the elementary damping resistors between capacitors consist of about ten parallel individual resistors. In addition the low voltage capacitance C_2 is composed of several tens of parallel individual capacitors that provide roughly equal inductive time constants for the high and low voltage arms.

The design aspects are considered separately for H.V. arm and L.V. arm.

4.2 Design of H.V. Arm

With reference to fig. 11 b of damped capacitive divider, the design of the H.V. arm is carried out on the following lines.

1. Determination of value of capacitance C_1
2. Evaluation of stray ground capacitance C_g
3. Residual inductance L_1
4. Surge impedance Z_o
5. Damping resistor R_1
6. Damping resistance of each unit R_1'
7. Value of each resistance in parallel arrangement of a unit.

Uniform distribution of the elements has been assumed over the whole length of the network, so that it can be considered as a transmission line of finite length earthed at one end.

4.2.1 Determination of value of C_1

The capacitance of the divider should be very low s o that it does not give any loading effect to the capacitance of the test object.

The fig. 18c gives the simple electrical circuit of the impulse generator, test object and potential divider.

Let C_i = Discharge capacitor of impulse generator

R_1 = Resistance for control of wavefront

R_2 = Resistance for control of wavetail

C_L' = Capacitance of test object

C_D = Capacitance of divider

C_L = Capacitance of test object + divider

$= C_L' + C_D$

Let The total capacitance of the generator be C_L

C_L = .01 uF. [Taken from existing impulse generator] 25

[In the existing impulse generator two capacitors of .1uF are connected in series and there are five stages. The total capacitance becomes in series when they are discharging and therefore

$$C_i = \frac{.1}{2 \times 5} = .01 \text{ uF}]$$

efficienty $\eta = \frac{V_o}{V_i} = \frac{C_i}{C_i + C_L}$

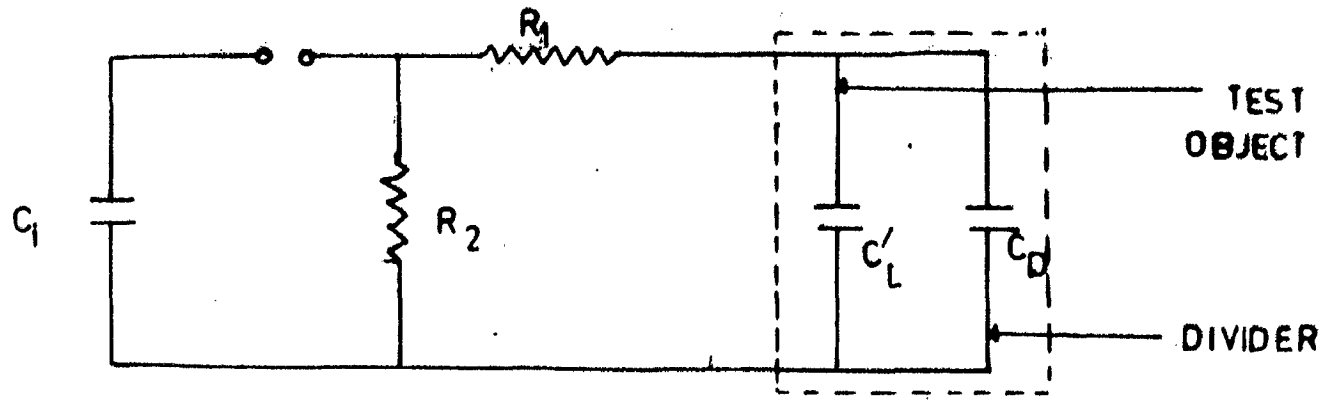


FIG 18 C

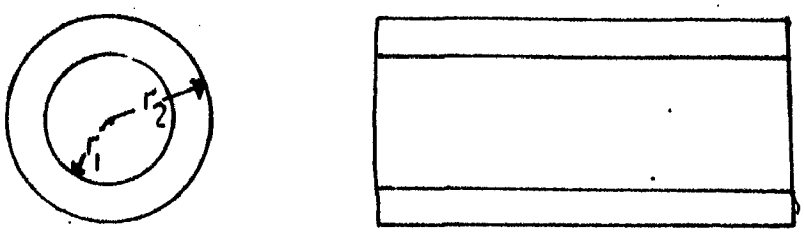


FIG 19 : COAXIAL TRANSMISSION LINE OF FINITE LENGTH

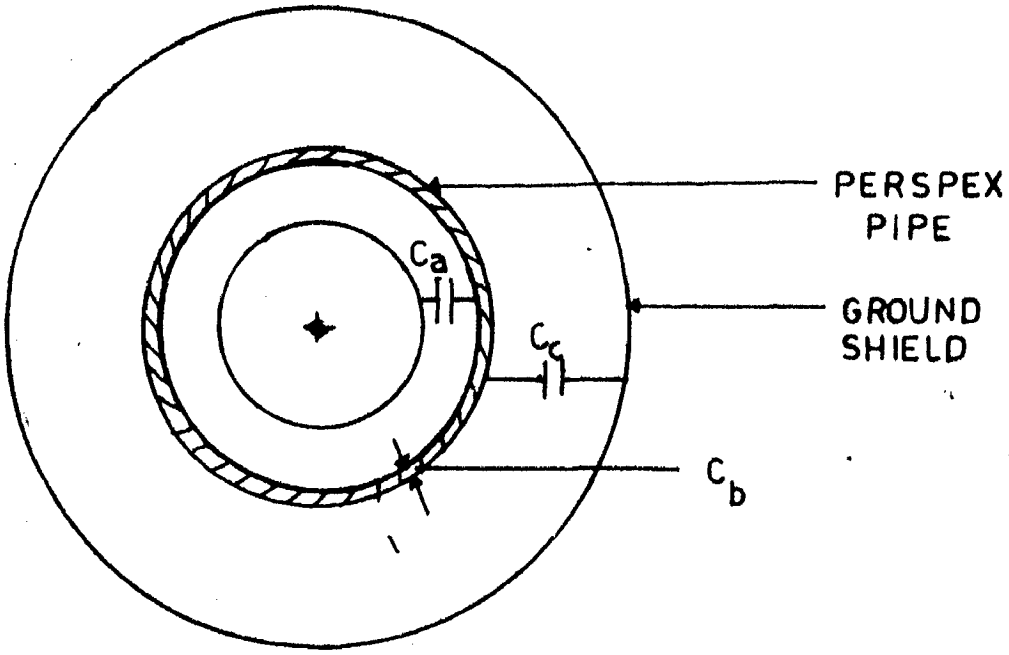


FIG 20

where V_o = Output voltage across the test object

V_i = Inpulse generator input

$.85 = \frac{C_i}{C_i + C_L}$ (Assuming impulse generator efficiency to be 85%)

or $.85\ C_i + .85\ C_L = C_i$

$C_i = 5.66 C_L$

i.e. the capacitance of load which can be tested on the existing impulse generator must be about $\frac{1}{6}$ th of the capacitance of the impulse generator, for 85 % of efficiency of the generator

i.e. $C_L = \frac{C_i}{5.66} = \frac{.01}{5.66} = 1.76 \times 10^{-3}\ \mu F$

$= 1760$ p.f.

From the loading effect point of view the capacitance of the divider may be chosen to be 1/50th of the total load capacitance.

Capacitance of the divider

$C_D = \frac{1760}{50} = 35.2$ p.f.

This capacitance C_D consists of high voltage capacitance C_1 and low voltage capacitance C_2 in series. Voltage across the low voltage arm is only a few hundred volts. Therefore the capacitance of the L.V. arm is very high in composition to the capacitante of H.V. arm. Assuming that the attenuation from 150 KV is 150 volts is enough, We have a divider ratio of $\frac{150 \times 1000}{150} = 1000$.

If we assume the voltage across C_2 is V_2 and voltage across the divider input = V_1, we have

$$\text{Attenuation} = \frac{C_1 + C_2}{C_1} = 1000$$

Or $$C_2 = 1000\, C_1$$

Also $$C_D = \frac{C_1 C_2}{C_1 + C_2} = 35.2$$ (As C_1 and C_2 are in series)

$$\frac{C_1 \cdot 1000 C_1}{C_1 + 1000 C_1} = 35.2$$

or $$1000 C_1 = 1000 \times 35.2$$

$$C_1 = 35.23 \text{ p.f.}$$

$$C_2 = 35230 \text{ p.f.}$$

Low inductance high tolerance ceramic capacitances of voltage rating upto 20 KV are available. The number of stages for 150 KV impulse voltage divider was chosen to be 15 including the L.V. arm. This will give voltage rating of the divider to be 280 KV which has been chosen purposely as the voltage rating of the generator is expected to be raised to 250 KV. Therefore the capacitance value of each unit could be 14 x 35.23 = 494.62 i.e. in the range of 500 to 550 p.f.

The actual values of the various ceramic capacitors of 500 p.f. have been tested on LCR bridge. [redacted] All the capacitor have values in the range of 475 to 510 P.F.

The average value of 14 capacitances

= 490 P.F.

and therefore capacitance $C_1 = \frac{490}{14}$

$= 35$ P.F.

4.2.2 Calculation of Inductance L_1

Each unit consisting of a capacitor and a damped resistance is considered as a transmission line. The oscillations due to stray inductances can be sufficiently reduced by arranging a number of resistance in parallel. This can be treated as a thin cylindrical conductor. The ground shield is considered as the return conductor. The equivalent circuit becomes that of a coaxial transmission line as shown in fig. 19.

Using the formula for calculating the inductance of a coaxial transmission line of two cylindrical shells. [26] [27]

$$L = 2 \times 10^{-7} \ln \frac{r_2}{r_1}$$

where L = inductance of transmission line

r_1 = radius of inner thin cylindrical conductor in the form of shell.

r_2 = radius of outer cylindrical shell.

r_1 and r_2 are selected keeping in mind the supporting structure & physical mounting of resistances and capacitances as well as the high voltage insulation level.

Let $r_1 = 30$ mm.

$r_2 = 80$ mm.

$L = 2 \times 10^{67} \quad \frac{80}{30}$

(2) Capacitance C_b of the thickness of perspex pipe.

[redacted].

(3) Capacitance C_c between the outer of perspex pipe a ground shield with air as medium.

All three capacitances are in series. Capac tance between two cylindrical shell is given by [26]

$$C = \frac{.024\ \epsilon_\gamma}{\log_{10} \frac{r_2}{r_1}}$$

Where ϵ_γ = relative permittivity of the medium between two shells.

r_2 = inner radius of the outer shell.

r_1 = radius of inner shell.

The inner diameter and thickness of the perspex pipe is selected to be 76 mm. and 8 mm. keeping in mind the supporting structure.

$$C_a = \frac{.024 \times 1}{\log_{10} \frac{38}{30}}$$ [as medium is air and relative permitting for air = 1.]

$$= .233\ \mu F/Km.$$

$$C_b = \frac{.024 \times 30}{\log_{10} \frac{42}{38}}$$ [medium being perspex for which $\epsilon_\gamma = 3.0$] [28]

$$= 1.656\ \mu F/Km.$$

$$C_c = \frac{.024}{\log_{10} 80}$$

$= .086\ \mu F/Km.$

C_g = (C_a and C_b in series) in series C_c

$= \frac{C_a C_b}{C_a + C_b}$ in series C_c

$= \frac{.233 \times 1.656}{.233 + 1.656}$ in series C_c

$= .204$ in series $.086$

$= \frac{.204 \times .086}{.204 + .086} = .0853\ \mu F/Km.$

$= 85.3$ pf/m.

Here length of divider = 1 meter

Capacitive C_g = 85.3 p.f.

4.2.4 Surge Impedance Z_o

Surge impedance Z_o is given by

$$Z_o = \sqrt{\frac{L}{C_g}}$$

$$= \sqrt{\frac{.11 \times 10^{-6}}{85.30 \times 10^{-12}}}$$

$= 35.91$ ohm.

4.2.5 Selection of R

$$R = 3 \text{ to } 4 \sqrt{\frac{L}{C_g}}$$

$= 107.7$ to 143.6 ohms.

Dividing this resistance into 14 units we have the resistance of each unit.

$$= \frac{107.7}{14} \text{ to } \frac{143.6}{14}$$

$$= 7.69 \text{ to } 10.23$$

Therefore we can have 6 resistances of 47 ohms each in parallel in one unit.

The total resistance of H.V. arm will be

$$= \frac{47}{6} \times 14$$

$$= 109.6 \text{ ohms.}$$

4.3 Design of Low Voltage Arm

Careful design and construction of the low voltage arm of capacitive divider is required to reduce the errors.[7] Because it is necessary to use only a L.V. signal at the input terminals of the oscilloscope the voltage divider ratio becomes very high and the capacitance of the low voltage arm is therefore high. There is a discontinuity at the junction of high and low voltage arm due to different impedances and when the signal travels through this junction, reflections occur giving errors in the measurement.

Error can be eliminated by terminating the cable at the input, at the C.R.O. end by a resistor equal to surge impedance of cable and by equalising [redacted] time constants for H.V. arm and L.V. arm. For same time constants we must have

$$R_1 C_1 = R_2 C_2$$

$$R_2 = \frac{R_1 \cdot C_1}{C_2}$$

$$= \frac{R_1}{C_2/C_1}$$

$$= \frac{R_1}{\text{Divider ratio}}$$

Divider ratio being very high the resistance R_2 has a very small value but compensates the large time constant and response time that would be introduced by the resistor R_1. By adding separate resistors in series with each of the parallel capacitors forming the low voltage arm the individual resistor value becomes in the order of a few ohms and is readily available.

The value of resistance R_2 obtained in the manner as above is not enough to damp out the oscillations in the low voltage arm.[17] To reduce the oscillations -

(1) Inductance of the low voltage arm is reduced by having a large number of resistances and capacitances in parallel.

(2) Resistance R_2 has got to be increased and optimised keeping same inductive time constants and same capacitive time constants of the high and low voltage arm.

(3) The connection of the output cable to the terminals of the low voltage arm should not allow magnetically induced voltages to appear in the loop across the terminals of the output cable. This is the reason to use coaxial cables.[17]

The capacitance of the L.V. arm has been calculated in the design part of H.V. arm which should be around 35 nF for a divider ratio of 1000. The inductance of the L.V. arm is equal to the inductance per unit of high

voltage arm which is equal to .0078 μH.

To make the RC time constants of both the arm equal, we must have

$$R_2 = \frac{R_1}{\text{Divider ratio}}$$

$$= \frac{109.6}{1000} = .11 \text{ ohm}$$

with this low value of resistance R_2 the oscillations due to the inductance of L.V. arm will not be suppressed. From suppressing point of view of the oscillations we must have roughly their inductive time constants equal.

i.e. $$\frac{L_1}{R_1} = \frac{L_2}{R_2}$$

or $$\frac{L_1}{L_2} = \frac{R_1}{R_2}$$

Therefore $$\frac{R_1}{R_2} = \frac{.11}{.0078}$$

$$= 14.1$$

or $$R_2 = \frac{R_1}{14.1} = \frac{109.6}{14.1}$$

$$= 7.77 \text{ ohms.}$$

Therefore to match the two controversial condition R_2 has got to be optimised between .11 ohm and 7.77 ohms.

After fabrication [redacted] R_2 value of 2.5 ohms was decided by trial and error method during the testing of the equipment.

Practically the values of low voltage capacitors which we have used, are such that total C_2 is obtained 44 μF giving a divider

$$\text{ratio} = \frac{44000}{35.0} = 1257$$

4.3.1 Matching of Delay Cable

The effect of the length of delay cable has been discussed in literature survey. For our purpose we have selected a coaxial cable of 50 ohms surge impulse of 2.5 m. length approx, which has hardly any effect on divider ratio.

It is terminated at input by a resistance equal to $(Z_o - R_2)$ ohms.

Let The input resistance $= R_3$

$$R_3 = Z_o - R_2$$
$$= 50 - 2.5$$
$$= 47.5 \text{ ohms.}$$

At the end it should be terminated by a resistance equal to 50 ohms. By adding this terminating resistance the response would be halved.

5. FABRICATION AND CONSTRUCTIONAL DETAILS

After having arrived at the design values of resistances and capacitances, the fabrication of them was undertaken to be 14 units in series. Perspex was chosen due to its good insulation and surface tracking properties.

5.1 Fabrication of H.V. Arm

The supporting structure for H.V. arm is a 44 mm. dia and 3 mm. thick perspex pipe which was cut into 15 pieces of 56 mm. length. After finishing the surfaces the length of one piece was left 53 mm. This gives us the spacing for mounting the capacitors and resistors. At the two ends of this piece two brass rings were fitted of 3 mm. width and 1.5 mm thickness. The resistances and capacitances were fabricated in parallel. A unit is shown in fig. 21 (a) in which various components are marked by alphabets.

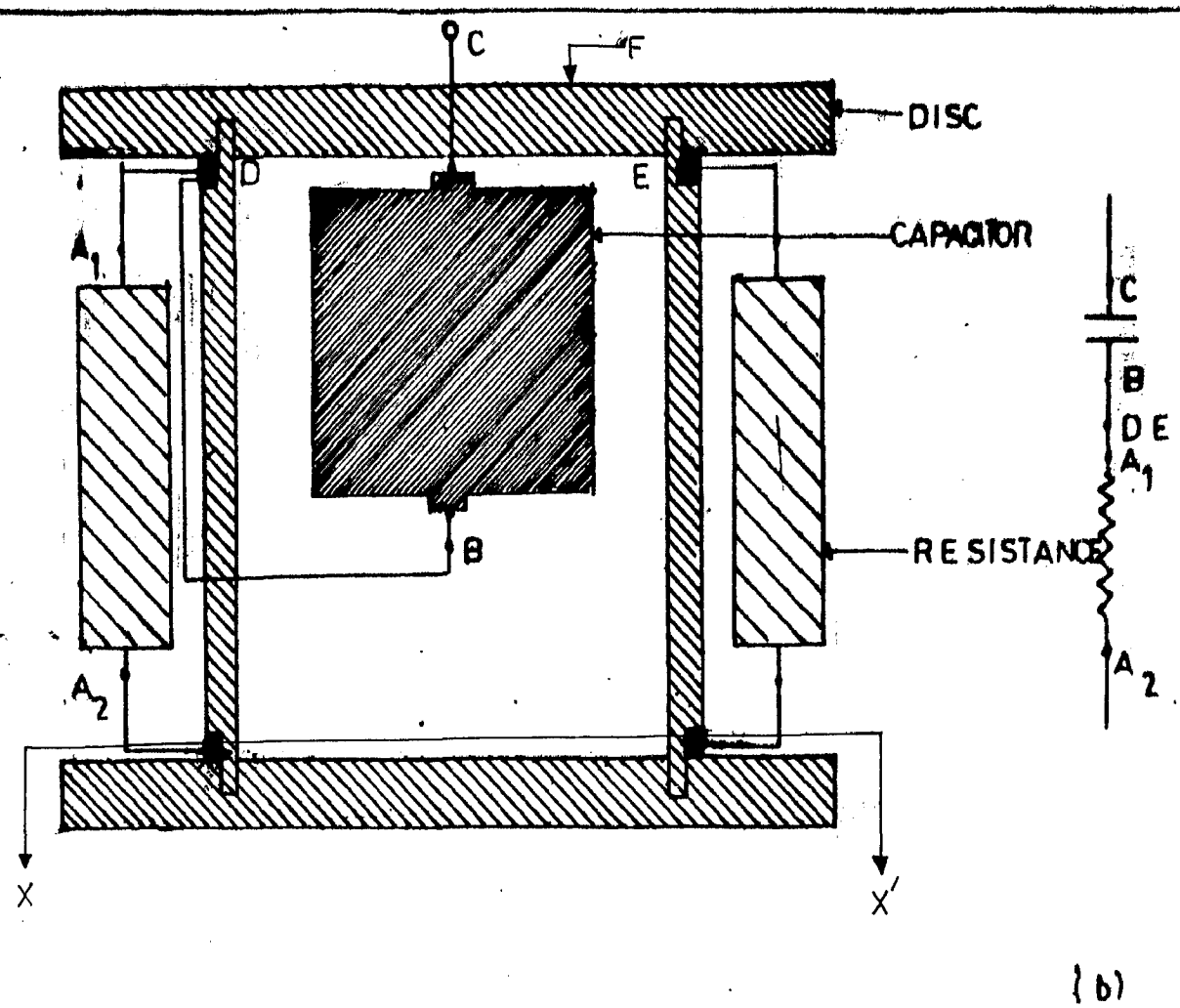
A_1, A_2 = Resistance terminals

B, C = Capacitance terminals

D_1, E_2 = Brass ring

An equivalent electrical circuit is shown in fig. 21 b. to make the physical structure more clear.

Inter-connection of units is made by 5mm. thick perspex discs, with the help of these discs all units are connected in series. One such disc is shown in fig. (a) by point F.



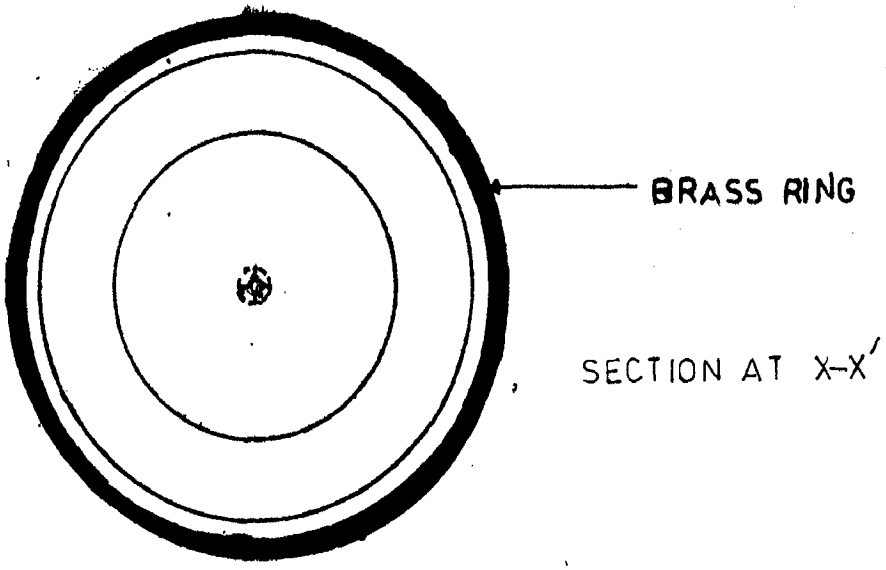


FIG 21 : CONSTRUCTIONAL DETAILS OF A UNIT OF H.V. ARM

This fabrication was achieved to minimise the length at the same time meeting the surface breakdown criterion. The overall length of H.V. arm consisting of 14 units is 1 meter. The assembly is put inside a perspex tube which gives it mechanical support, high insulation, shielding from dust as well as to enable further developmental work.

The high voltage terminal is made of 9 cm. dia aluminium cup of rounded cornors to avoid corona. Ideally it should be a sphere. The high voltage terminal can be seen in photograph no.1.

5.2 Fabrication of L.V. Arm

L.V. arm consist of similar one unit. Here the capacitances are fabricated in parallel at the outer periphery of perspex unit having resistances in series of each capacitance. The high voltage arm is electrically connected in series to L.V. arm. The connections are made such that they are easily approachable. The junction point is connected to central terminal of a BNC connector through a resistance of 47 ohms and is fitted on a PVC pipe piece. The lower end of L.V. arm is connected to the metal surface of BNC connector.

The signal cable of 2.5 meter length and surge impedance of 50 ohms connects the BNC connector to C.R.O.

A photograph of the divider is shown in photograph No. 1

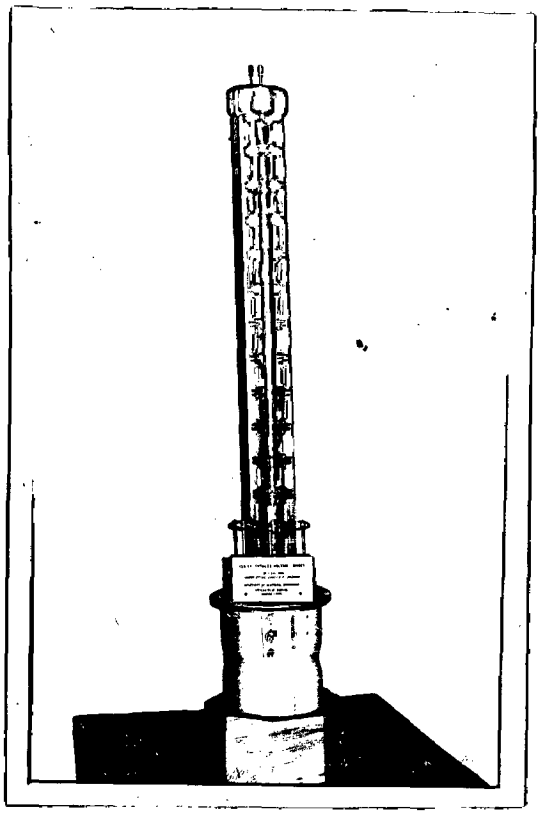


PHOTO 1: 150 KV IMPULSE VOLTAGE DIVIDER

6. PERFORMANCE CHARACTERISTICS

Accurate calibration of the output signal of a voltage divider can be made, provided the waveform of the input voltage is given. Generally input waveform is not known. Therefore one should proceed in the reverse sequence.[2-3] From a given, possibly distorted, waveform of the output voltage measured by means of a C.R.O., the actual waveform of the input voltage has got to be determined. Obviously this calculation will only be practical for output waveforms that can be described analytically in a comparatively simple manner. An idealized input waveform, such as a step function or a rectangular pulse or a square wave is generally employed to evaluate peak value and risetime errors. The pulse should reach its peak as rapidly as possible and have negligible drop on the tail. In general the rise time of the testing pulse should be five to ten times as fast as the expected rise time of the divider system under test. The pulse should last at least as long as it takes for the divider to obtain the steady state conditions.

After discussing the performance at low voltage and measures to be taken to improve the response, divider is tested at high impulse voltage by the use of impulse generator.

6.1 Low Voltage Perfofmance

At low voltages the divider has been tested with two low voltage signals of different rise time.

(1) With rectangular wave input of 80 ns rise-time.

(2) With repetitive square pulses of 10 ns risetime.

6.1.1 Rectangular Wave Input Response

The circuit was arranged as shown in fig. 22a and 22c to see the response of the pulse generator as well as of the divider respectively.

6.1.1.1 Input

10 volts input of the pulse generator was fed directly across the C.R.O. plates through the 50 ohms coaxial cable. The waveshape recorded on the C.R.O. is traced in fig. 22b. A photograph of input was also taken and is shown in photograph no. 2.

The details of the input are as follows.

Sweep	=	200 ns/cm
Pulse match	=	1.2 us
Rise time	=	80 ns
Amplitude	=	10 volts

6.1.1.2 Output

The above low voltage signal of pulse generator is fed to the divider through the coaxial cable as shown in fig. 22c. The sample voltage across the L.V. arm of the

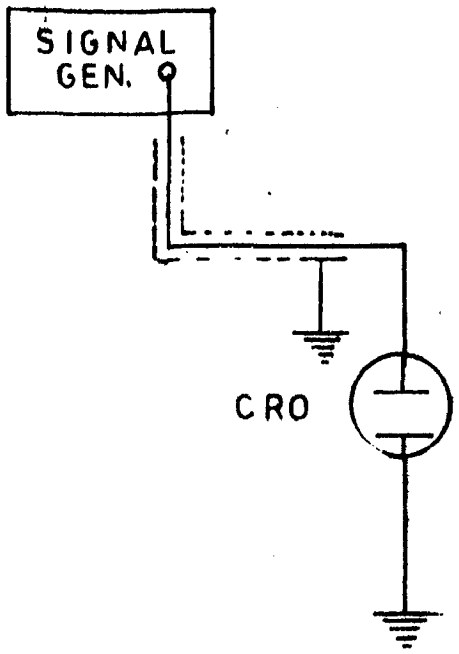


FIG 22a : MEASUREMENT OF INPUT

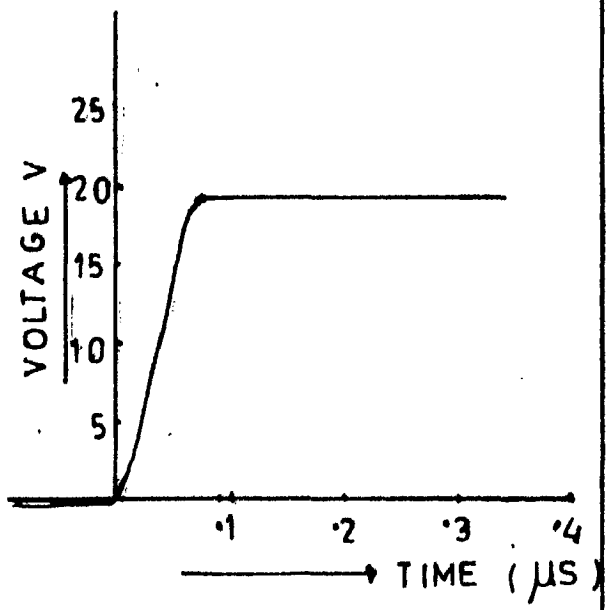


FIG 22b : INPUT WAVEFORM

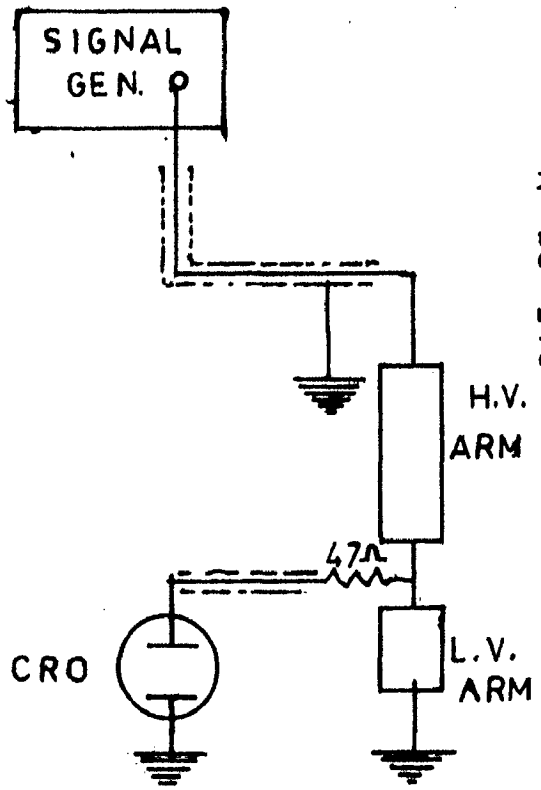


FIG 22c : MEASUREMENT OF OUTPUT

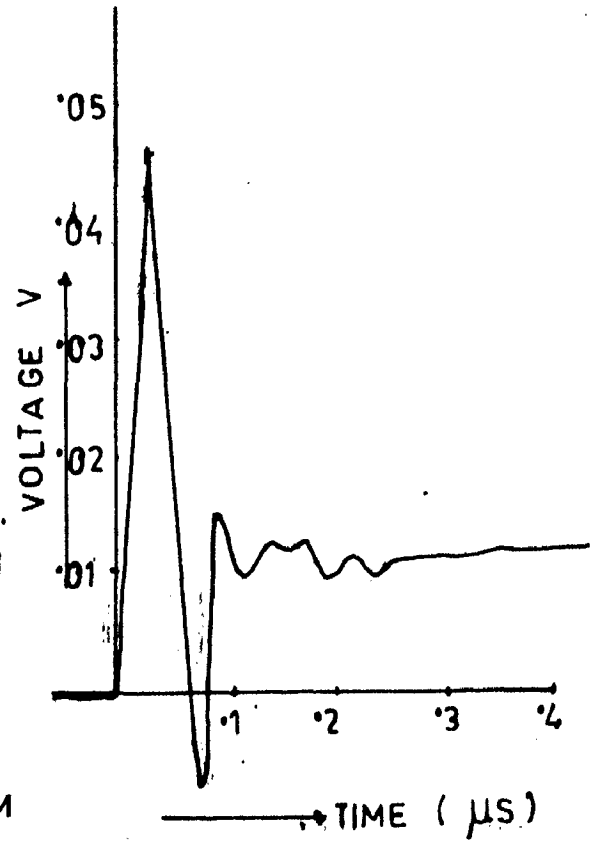


FIG 22d : OUTPUT WAVEFORM

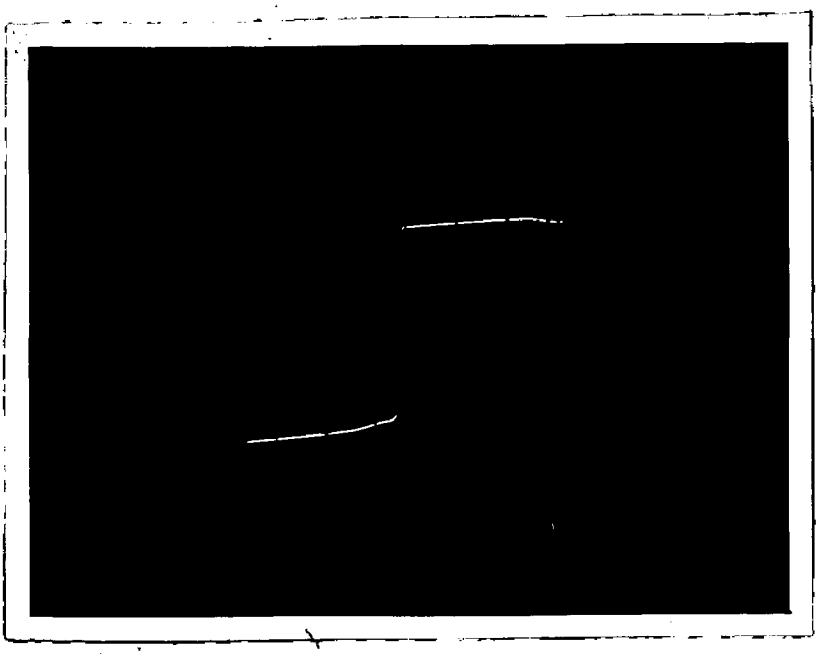


PHOTO 2 : INPUT WAVEFORM

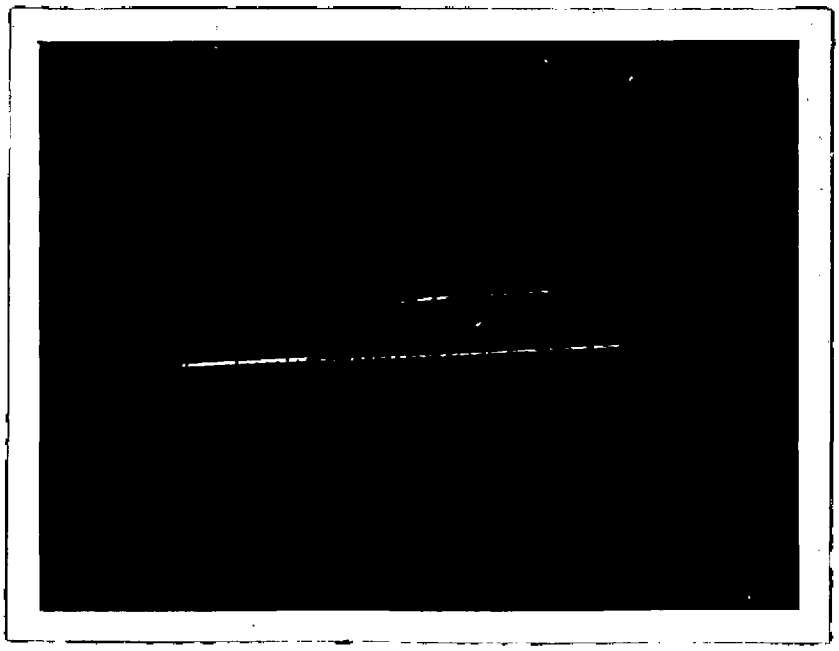


PHOTO 3: DIVIDER RESPONSE

divider is fed to C.R.O. plates through the same 50 ohms.coaxia cable. The output waveform recorded on C.R.O. is shown in fig. 22d. Output is also shown by actual photograph No.3.

The following observations are made from this output.

(1) Oscillations are produced which are due to residual inductances and lead inductances and due to mismatching of pulse generator output impedance.

(2) Overshoot of the order of 5 times the amplitude of the divided wave is obtained.

(3) Under shoot is double the amplitude.

(4) Sweep = 100 ns/cm.

Pulse width = 1.2 μs.

Rise time = 30 ns.

Amplitude = .007 volts

Divider ratio = $\frac{10}{.007}$

= 1430

Theoretical calculated divider ratio = .1257

6.1.1.3 Measures taken to improve the response

As shown in fig. 23 this response can be improved by considering three factors -

(1) Source input impedance R_1.

(2) Damping resistor R_D.

(3) Parallel termination at C.R.O. end.

6.1.1.4 Effect of Source Impedance R_i

(A) R_i = 33 ohms

The over shoot and under shoot both are decreased nominally. [Fig. 24a].

(B) R_i = 50 ohms

Overshoot decreases slowly and the undershoot diminishes to a greater extent. [Fig. 24b]

(C) R_i = 100 ohms

There is no change in the overshoot while undershoot gets reduced further. [Fig. 24c]

(D) R_i = 470 ohms

Overshoot is reduced to half and the undershoot also gets reduced to a very low value. [Fig. 24d]

(E) R_i = 1000 ohms

At higher values of [R_i > 470 ohms] the wave front becomes dropping and rise time is increased. [Fig.24e]

6.1.1.5 Effect of Damping Resistors

The oscillations can be reduced further by using damping resistances R_D. The performance is observed at different values of R_D.

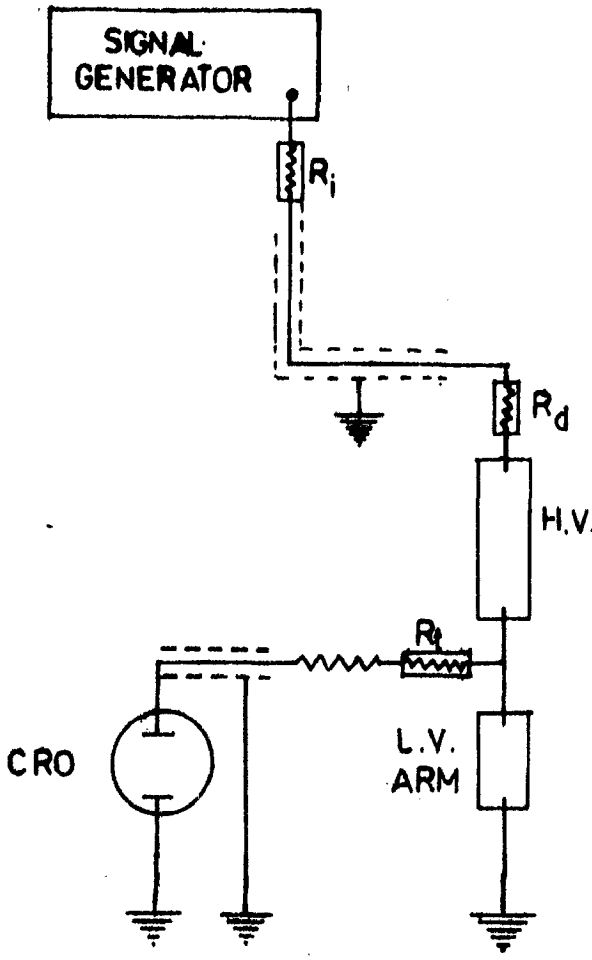
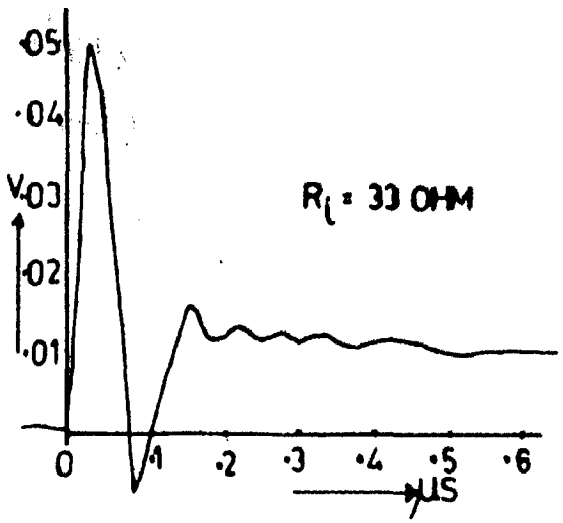
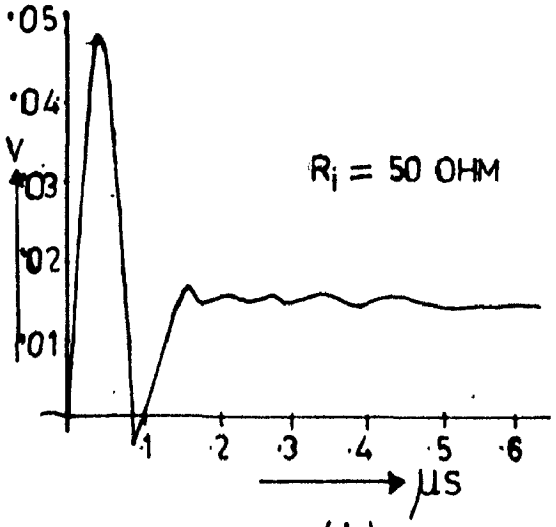


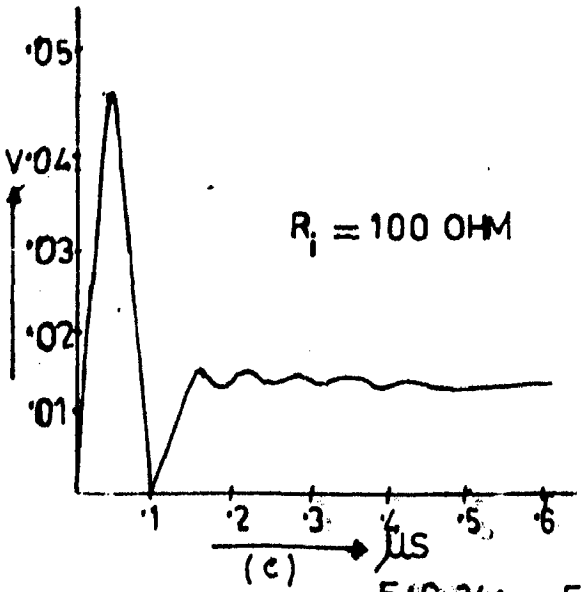
FIG 23



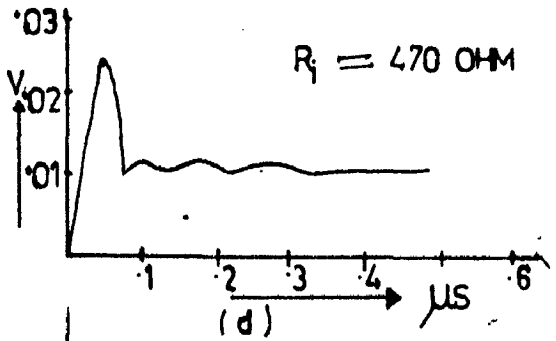
(a)



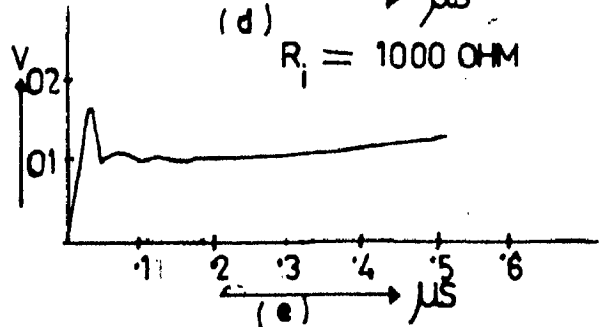
(b)



(c)



(d)



(e)

FIG 24: EFFECT OF SOURCE IMPEDANCE R_i

A. R_d = 1K ohm

From fig. 25a it is observed that overshoot is reduced too much and performance becomes better.

B. R_d = 1470 ohms

The overshoot, undershoot and oscillations are reduced to a great extent. The shape becomes almost a replica of the input. [Fig. 25b]

C. R_d = 2K ohm

The front of the wave is lengthened and becomes drooping. It is a case of over damping. [Fig. 25c].

The details of the output observed are

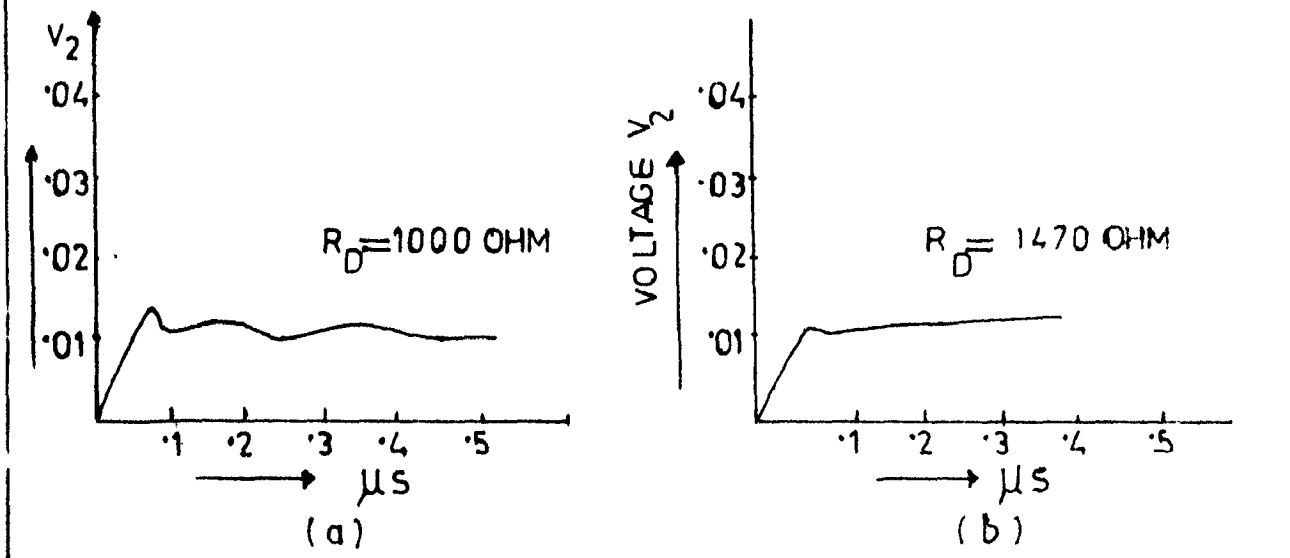
Sweep	= 100 ns/cm
Pulsewidth	= 1.2 μ sec.
Rise time	= 30 ns
Overshoot	= 2 %
Undershoot	= 2 %

6.1.1.6 Effect of Parallel Termination at C.R.O.

If the cable at the C.R.O. end is terminated by a resistance $R_T = Z_o$, the voltage amplitude is halved. [Fig. 25d].

6.1.1.7 Effect of Mismatching of Cable Input Termination

The best performance[fig. 25c] is obtained when the meas-uring cable is terminated at the input by



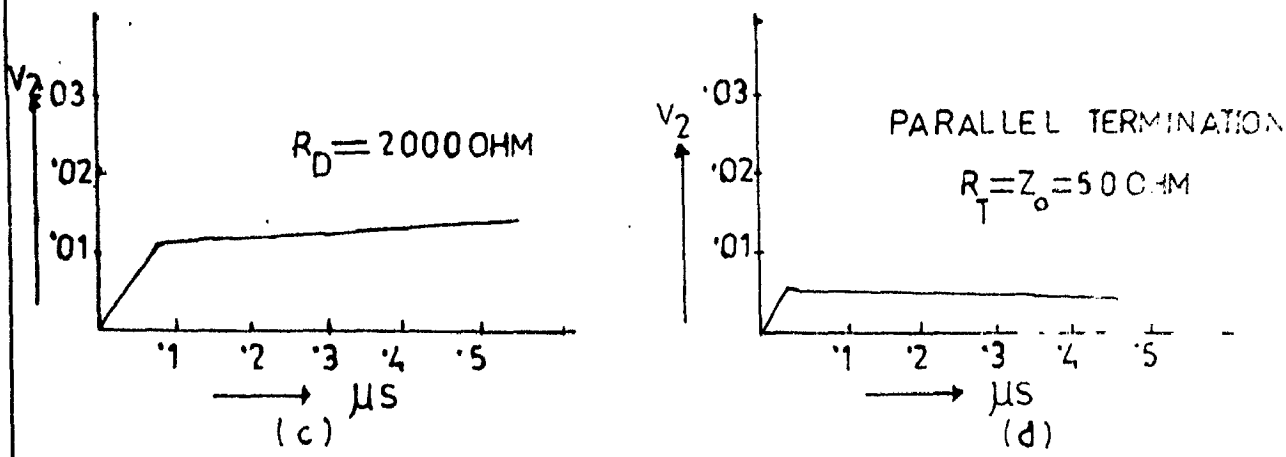


FIG 25 : EFFECT OF DAMPING RESISTOR

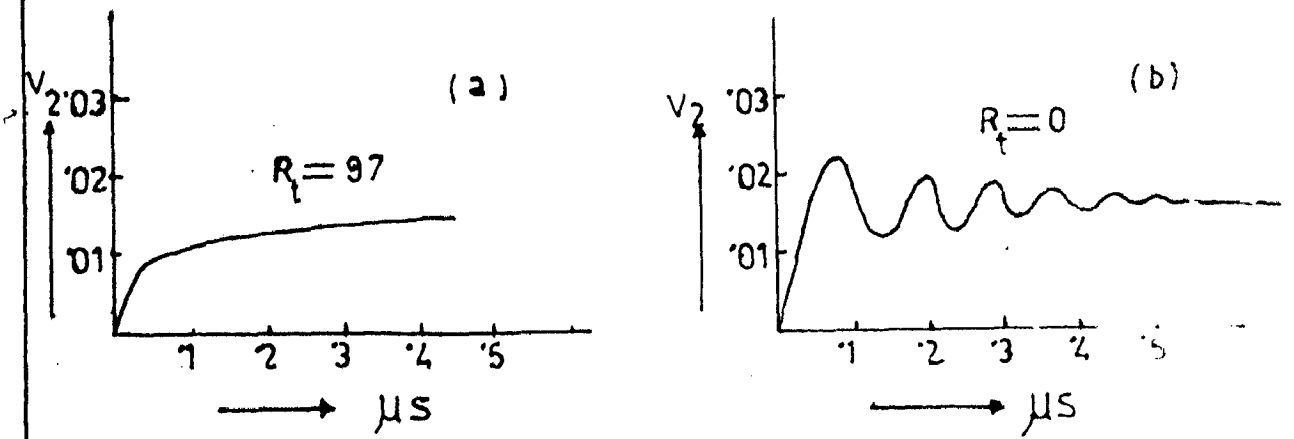


FIG 26 : EFFECT OE MISMATCHING

a resistance of 47 Ω. This is the matched condition of the L.V. arm with the cable. If this is mismatched the performance becomes very poor as shown in fig. 26. The performance is observed with two valuesof R_t.

(A) $R_t > 47$ ohms

From fig. 26a it is seen that when R_t is increased from 47 ohms to 97 ohms by adding one more resistance of 50 ohms in series of 47 ohms, the wave form becomes drooping and rise time is increased, No overshoots and undershoots are observed.

(B) $R_t = 0$

Too much oscillations are observed and the performance becomes very much poor. [Fig. 26b].

6.1.2 Step Response

The actual step function is one having rise time of the order of 1 ns. We have used repetitive square pulses of rise time 10 ns, by a pulse generator available in the Electronics and Communication Engineering Department, University of Roorkee, Roorkee. The response was recorded on a tektronix C.R.O. of the same department. The input wave applied to the divider is shown in fig. 27a. Input has the following characteristics -

Sweep	= 20 ns/cm
Pulsewidth	= 10 μs
Rise time	= 10 ns
Amplitude	= 9 volts

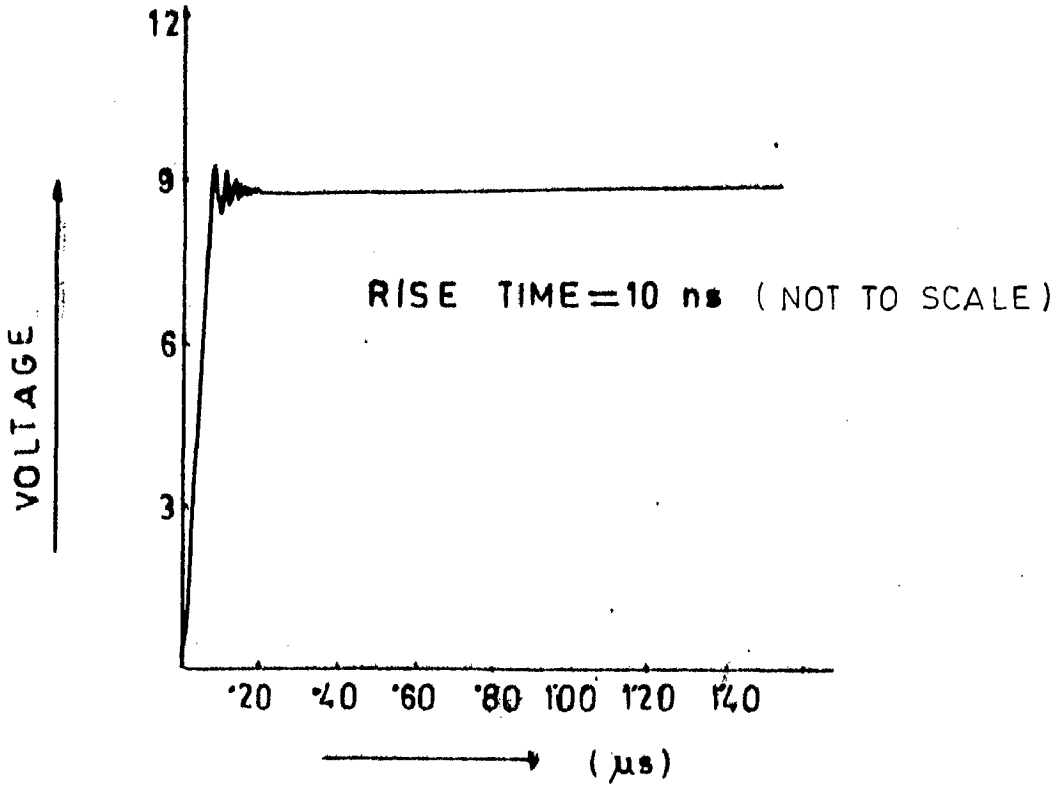


FIG 27a: STEP INPUT

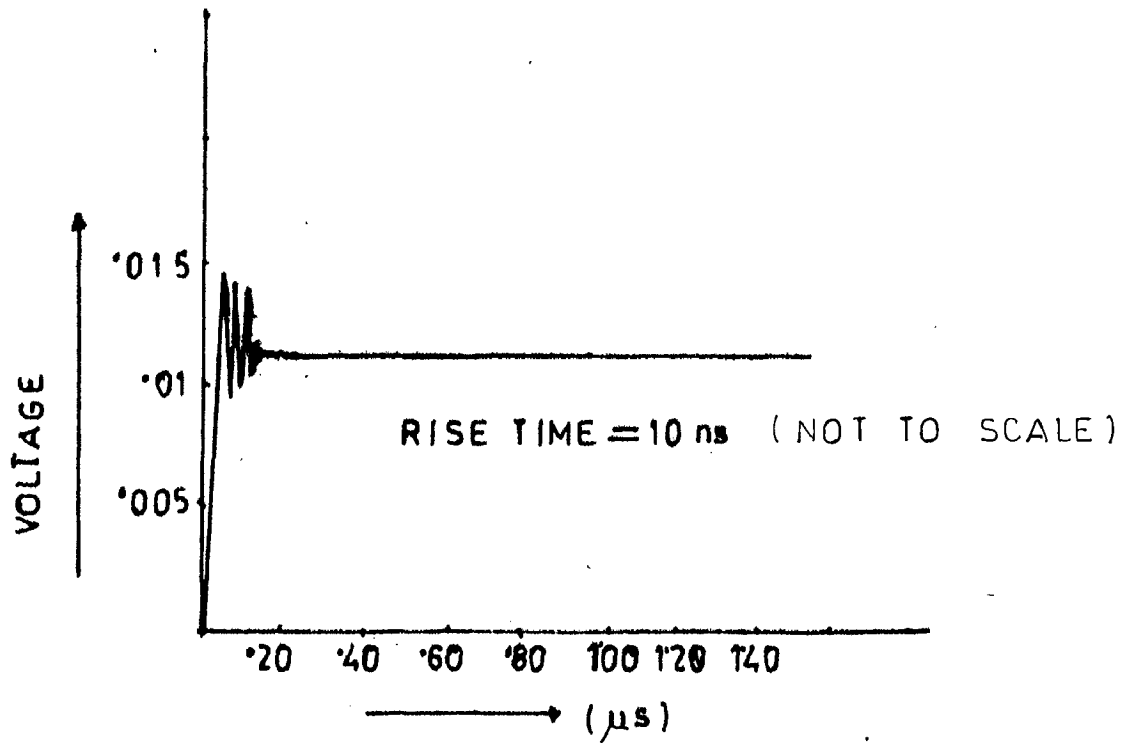


FIG 27b: DIVIDER RESPONSE

Oscillations in the input are observed for a period of 100 ns as marked in fig. 27a.

The output waveform using a damping resistor of 2K ohm is shown in fig. 27 b.

Its characteristics are

Sweep	= 20 ns/cm
Pulse width	= 10 μs
Rise time	= 10 ns
Period of oscillation	= 100 ns as shown in fig. 27 b.
Amplitude	= .006 volts
Overshoot	= 25 %
Undershoot	= 15 %
Divider ratio	$= \frac{9}{.006}$
	= 1500

The following points are observed.

(1) The rise time of the input signal and the output is same.

(2) The period of oscillation is same for input and output which shows the performance of the divider is quite satisfactory.

(3) The overshoot and undershoot of oscillations are increased as compared to rectangular input signal of 80 ns rise time to a value to 25 percent and 15 percent respectively.

(4) The divider ratio obtained with this signal of 10 ns rise time/1μs 1500 which is very close to the ratio obtained with the signal of 80 ns rise time which is 1430.

Since the measurement of divider ratio was done by visual observation and not by taking photographs, it may contain large errors.

6.2 High Voltage Performance

Having analysed the low voltage performance of the divider it is subjected to high impulse voltage by impulse generator available in the high voltage lab. of the department. The block diagram of the test set-up is shown in fig. 28. A.C. input of 230V, 50 Hz is given to a charging cct. which gives high d.c. voltage of the order of 30 KV. This voltage charges the capacitors of impulse generator cct. giving the sparking across the sphere gaps resulting impulse voltage across the divider and the sample voltage across the low voltage arm of the divider appears on the C.R.O. which is measured for its amplitude and rise time. Actual test set up is shown by photograph No.4.

The operation of charging set and impulse generator is discussed here in brief.

6.2.1 Operation of Charging Circuit

The circuit for charging the capacitors of impulse generator is shown in fig. 29.

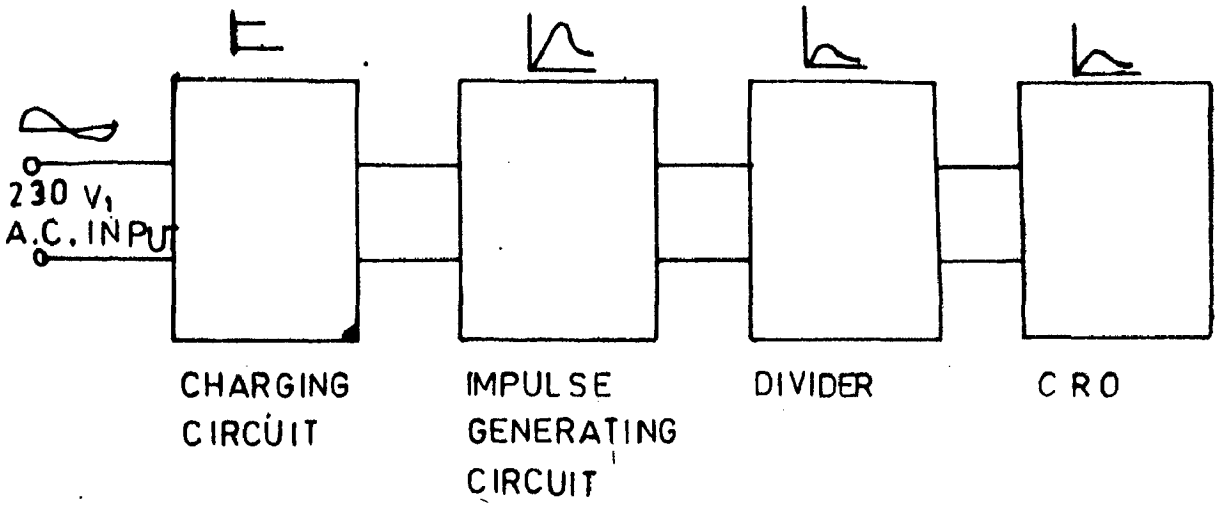


FIG 28 : BLOCK-DIAGRAM OF TEST SET-UP

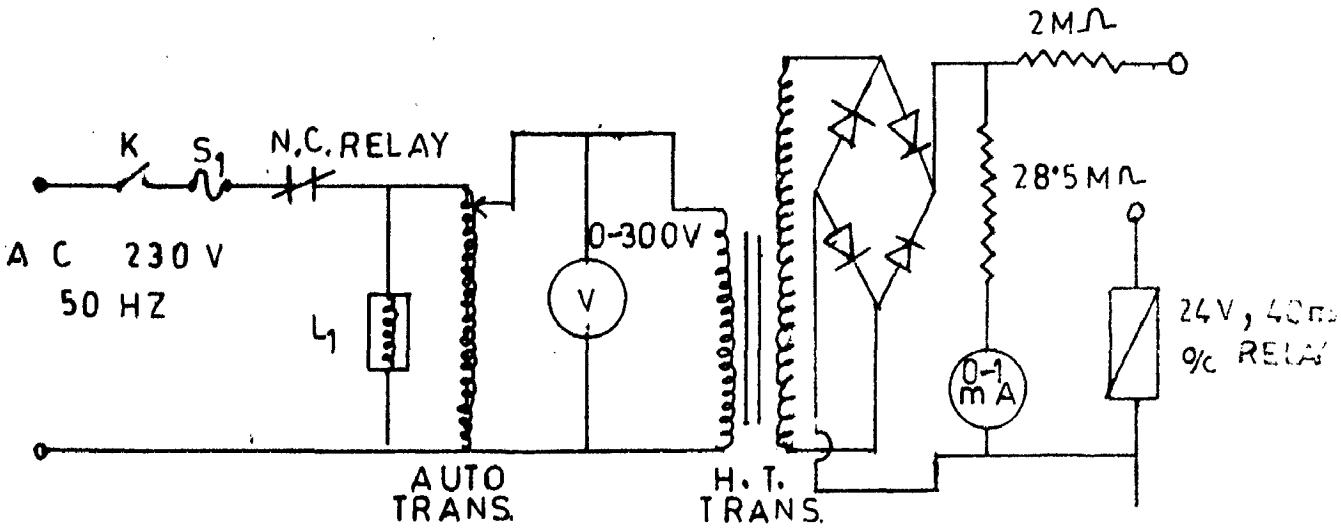


FIG 29 : CHARGING CIRCUIT

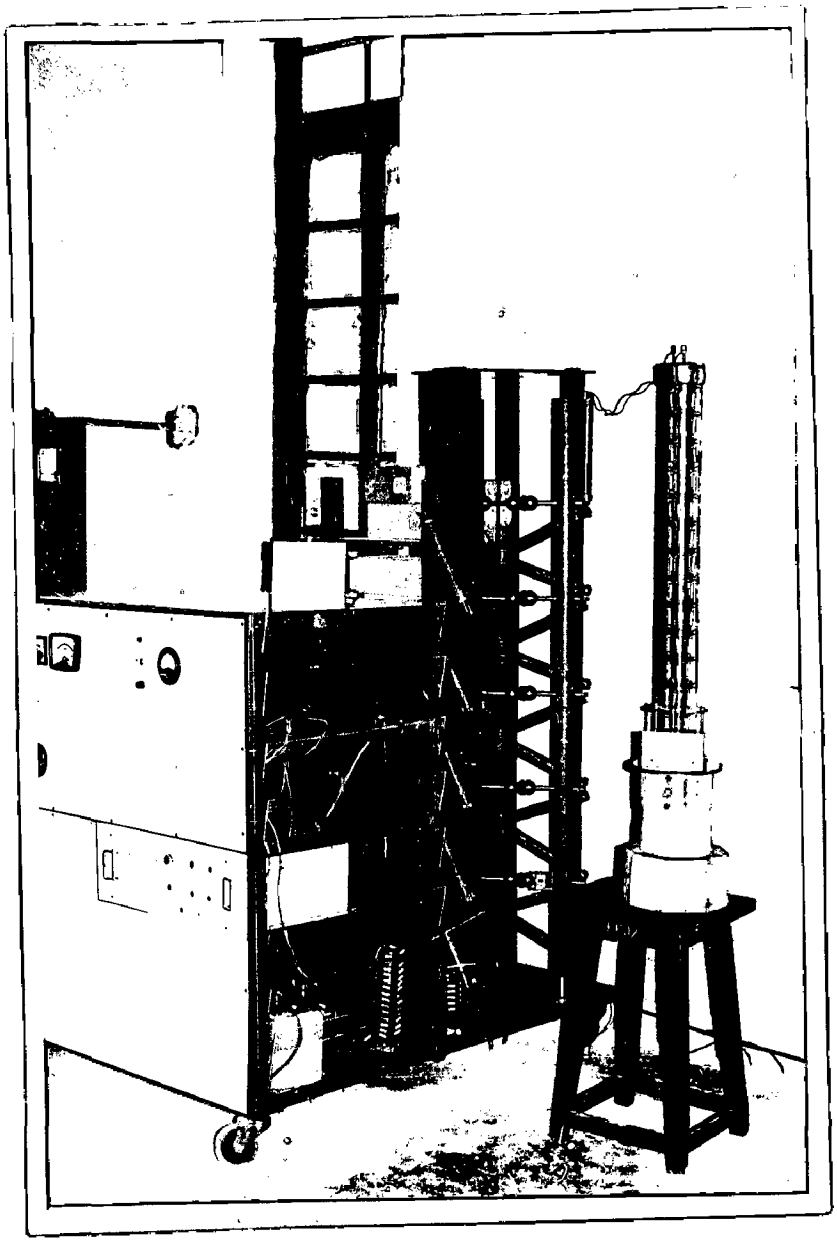


PHOTO 4 : HIGH IMPULSE VOLTAGE TESTING SET-UP

Since the need high voltage D.C. supply we have to have rectification techniques i.e. high voltage D.C. is obtained with the help of rectifiers from a.c. voltage. We have option to use half wave rectifier cct. or voltage doubler cct. or Cockroft Walton cct etc. Each type has its own advantages and disadvantages. For instance a bridge rectifier needs 4 diodes and transformers, while voltage doubler cct needs only two diodes(different rating than used in bridge rectifier cct.). Similarly the rating of transformer is also different for the same D.C. output in both cases. Seeing the overall economy i.e. in transformers and rectifiers, ~~we have selected a bridge rectifier~~, we have selected a bridge rectifier configuration for 30 KV D.C. charging set.

When the switch K is pressed, the supply voltage of 230 volts comes to the primary of low voltage auto transformer, which is indicated by a red neon lamp L_1. The output of the variaf is directly fed to the primary of high voltage transformer, and the voltage fed is shown by voltmeter. In order to measure high voltage of secondary side a miliameter is provided in series with a high resistance. Its 1 mA full scale deflection represents 28.5 KV for the existing cct. over current relay in the load circuit, has been provided for the safety. When the current in the load

cct. exceeds the present value, the normally closed contact N.C. gets open and thus the supply to the primary side of varial is automatically switched off.

6.2.2 Operation of Impulse Generator cct.

In impulse generator cct the capacitances are charged in parallel through resistances and discharged in series through spark gaps. The equivalent circuit of available generator is presented in fig. 30. The stage capacitors C are charged in parallel through high value charging resistors R_3. At the end of the charging period, the points A, B,.....E will be at the potential of the d.c. source, e.g. +V with respect to earth and the points F, G,.....L will remain at earth potential. The discharge of the generator is initiated by the breakdown of the spark gap AF which is followed by simultaneous breakdown of all the remaining gaps. When the gap AF breaksdown, the potential on the point A changes from +V to zero and that on point G swings from zero to -V owing to the change on capacitor AF. The potential on B remains +V during the interval the gap AF sparks over. A voltage 2V, therefore appears across the gap BG which immediately leads to its breakdown. This breakdown creats a potential difference of 3V across CM; the breakdown process, therefore, continuous and finally the potential on L attains a value of 5V.

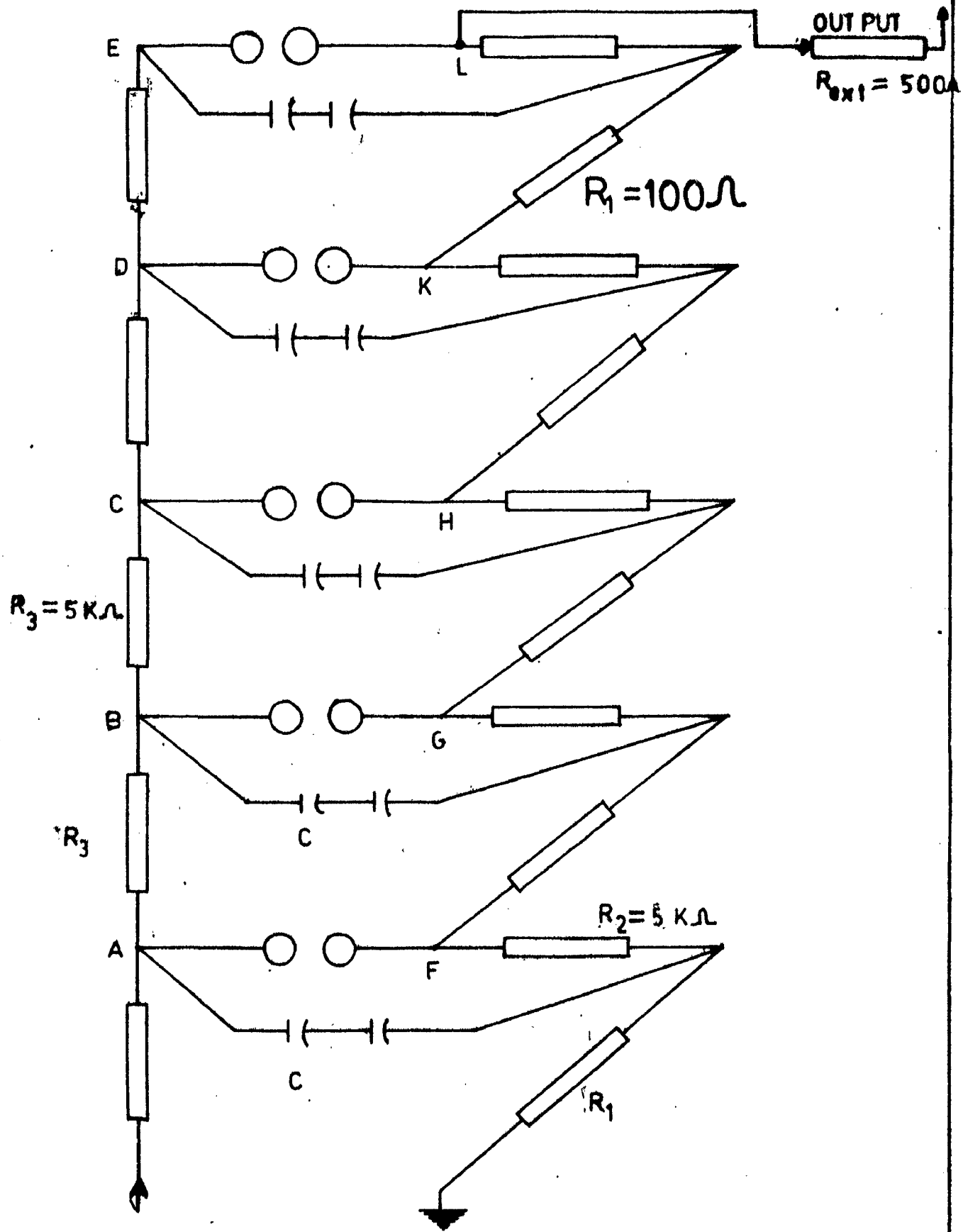


FIG 30: IMPULSE GENERATOR CIRCUIT

The measurement by high voltage is done in two steps.

(1) Measurement with sphere gap taking into account the atmospheric pressure and temp. and neglecting humidity effect.

(2) Measurement with impulse potential divider.

6.2.2.1 Measurement with Sphere Gap

The impulse generator output is applied across the two spheres which are used as voltmeter. One s-phere is at high voltage and the other is earthed. Available Sphere of ~~available~~ 5 cm. diameters were used. The tests cct. is shown in fig. 31.

Taking air density factor into account and neglecting humidity breakdown voltage V_B is given by

$$V_B = \delta V$$

where $$\delta = \frac{P}{760} \cdot \frac{293}{273+t}$$

The P is atmosphere pressure in mm. of Hg and t is temp. in ^{o}c.

V_B = Breakdown voltage at pressure p and temp. t.

V = Breakdown voltage at which the sphere gap setting gives 50 % breakdown at normal pressure and $20^{o}c$ temp.

The experimental readings for one value of high impulse voltage are given in table 1.

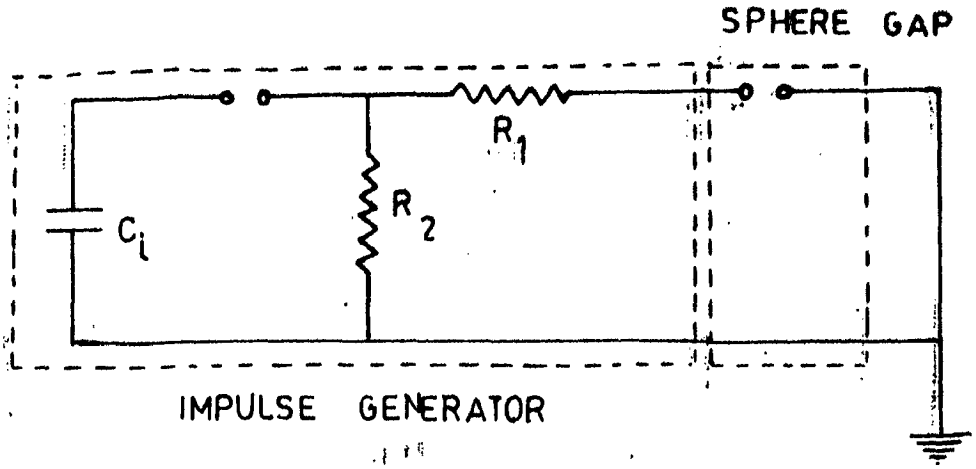


FIG 31: MEASUREMENT OF IMPULSE VOLTAGE BY SPHERE GAP

Table 1

S.No.	D.C. Charging Voltage in KV.	Nominal output in KV	Gap Setting
1.	.38 x 28.5 = 10.83	10.83x 5 = 54.15	.61''

50% Breakdown voltage in KV* (Measured)	Air density factor.	50% Breakdown Voltage. (Actual)
47.6	.928	47.6 x .928 = 44.17 KV.

* The standard calibration table of KV peak versus the sphere gap has been taken from the book by 'Abdullah and Kuffel'.[7]

6.2.2.2 Measurement With Divider

The actual output voltage 44.17 KV is applied to the divider for its calibration. It was observed that divider withstood 44.17 KV impulse in respect of insulation etc., but we could not record the output wave due to very low intensity of the response. The photograph was also not possible on a simple C.R.O. Use of a single shot C.R.O. would have made it possible to have the photograph but nonavailability of single shot C.R.O. was a handicap for recording the high voltage response. Also, the present impulse generator was not in a position

produce voltage above 50KV due to the slow PIV rating of the diodes used in the H.V. D.C. supply.

7. DISCUSSION

7.1 Low Voltage Performance

In order to evaluate the performance of the divider its response towards a L.V. step function was necessary. Since the internal resistance of the step function generator R_i influences the response characteristics as discussed in 3.3.2, it was necessary to find the critical internal resistance of the source which experimentally is found to be 470 ohms. In fig. 24 the response characteristics for various values of R_i are shown. It can be seen from fig. 24 d that R_i = 470 ohms is the value of the critical internal resistance of the ~~signal of the~~ pulse generator.

In fig. 24 d in which the response of the divider is given for R_i = 470 ohms, it can be seen that there are oscillations of the order of the response magnitude which were further reduced by putting damping resistance. For the best performance the value of damping resistance was 1470 ohms. Actually from the design considerations point this value should have been very small as the damping resistors are already put in the divider throughout its length in series with the capacitances. But practically it is more due to the fact that in the design considerations we have chosen an earth shield near the divider giving to equalise the earth capacitances

from top to bottom. Practically we have not used the shield and thus ground capacitances have reduced to a large extent, the earth now being at quite large distance, and from $R_1 = \sqrt{\frac{L}{C_g}}$, the value of the damping resistor R_1 will increase correspondingly.

The contribution of the residual industance is expected to be the same as calculated with a ground shield because the measured value of the inductance without the ground shield was .14 μH as compared to the calculated value of .11 μH.

Therefore high voltage of damping resistors used practically to damp-out oscillations is in agreement with theoretical predictions.

It can be seen from fig. 25 and 26 that 47 ohms is the optimum termination to be used at the input of cable which confirms the theoretical value and the mismatching of the cable termination results in poor performance of the divider confirming the theoretical considerations outlined in design aspects.

The overshoot and undershoot observed are of the order of 2% which are tolerable.

The divider is supposed to be subjected to lightning impulses of the rise time of 1.2 μs ± 30 %.

Its performance is found quite satisfactory for the signals of having the risetime of 80 ns and 10 ns as can be seen from fig. 25b and 27b. Therefore it can be predicted that its performance for the impulse wave, for which it has been fabricated will be better than the performance for 80 ns and 10 ns rise time waveforms.

The divider ratio for rectangular low voltage signal is found to be 1430 and with a step function is found 1500 from fig. 25 b and 27 b respectively while theoretically it is 1257. The assumptions, made in calculating the theoretical ratio, and the inherent recording error of the C.R.O. [Least count of C.R.O. being .002 volts] account for this difference. Other sources of errors discussed in the chapter of literature Survey are also responsible for the difference.

Another limitation of this technique is the risetime of oscilloscope amplifier which is in the range of 10 - 20 ns. It is possible that the rise time of the divider is short compared to the rise time of the amplifier or the applied step voltage in which case its high frequency response should be considered very good. However the analysis of the response characteristics at high voltage would give a more true picture of performance.

High Voltage Performance

The impulse generator output was calibrated at
t 50 KV as given in article 6.2.2.1. An impulse of
/ was applied to the divider.

The divider successfully withstood the voltage
neither the response was successfully observed visually
lue to low intensity of impulse it could be photo-
ned on a simple C.R.O. With a simple C.R.O. recording
mpulse wave of 1.2 us rise time is not easy and it
lres sophisticated single shot C.R.O. which has proper
natic preset adjustments to take the photographs as
as the divided wave appears on C.R.O. Therefore the
voltage calibration could not be carried out.

8. CONCLUSION

1. The 150 KV impulse voltage divider will enable the measurement of output impulses of the 150 KV impulse voltage generator.

2. The rating of the impulse voltage divider can be increased to at least 250 KV.

3. The L.V. performance analysis indicates that the divider performance at high voltage will be acceptable for lightning and switching surges.

4. From low voltage performance it is observed that an external damping resistance would be desirable for high voltage performance. The values of this resistance could be decided by further developmental work.

5. The high voltage calibration of the divider should be carried out using single shot C.R.O.

6. Measures can be found to improve the high voltage response.

7. With the help of the measured response characteristic for a step function input and the actual measured divided wave analysis could be carriedout to arrive at the actual input waveform.

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