DESIGN, ANALYSIS AND IMPLEMENTATION OF CONCURRENT DUAL BAND (2.4/5.2 GHz) WIRELESS TRANSCEIVER

A DISSERTATION

Submitted in partial fulfillment of the requirements for the award of the degree of

MASTER OF TECHNOLOGY

in

ELECTRONICS AND COMMUNICATION ENGINEERING

(With Specialization in RF and Microwave Engineering)

By

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Candidate's Declaration

I hereby declare that the work, which is being presented in the dissertation entitled, ***"Design, Analysis and Implementation of Concurrent Dual-band (2.4/5.2 GHz) Wireless Transceiver "***, which is submitted in the partial fulfillment of the requirements for the award of degree of ***Master of Technology*** in ***RF & Microwave Engineering***, submitted in the Department of Electronics and Computer Engineering, ***Indian Institute of Technology***, Roorkee (INDIA), is an authentic record of my own work carried out under the guidance of **Dr. N.P. Pathak**, Assistant Professor, Department of Electronics and Computer Engineering, Indian Institute of Technology, Roorkee.

I have not submitted the matter embodied in this dissertation for the award of any other degree or diploma.

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Place: Roorkee **Enrol. No: 09533015**

Supervisor's Certificate

This is to certify that this dissertation entitled, ***"Design, Analysis and Implementation of Concurrent Dual-band (2.4/5.2 GHz) Wireless Transceiver"***, which has been submitted by Zubair Akhter is record of his own work carried out by him under my supervision. I also certify that the above statement made by the candidates is correct to the best of my knowledge and belief.

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This dissertation reports the design and development of concurrent dual-band wireless transceiver for 2.4/5.2 GHz wireless applications. Design issues related to front end elements such as Low noise amplifier (LNA), antenna, power combiner, and band pass filters are discussed in details. Simulated gain and noise figure of low noise amplifier reported in this thesis is 11.72dB & 0.3 dB at 2.44 GHz and 6.92dB & 0.46 dB and 5.25 GHz respectively. The measured bandwidth of microstrip based monopole antenna having Omni-directional radiation pattern are: 950MHz at 2.4 GHz and 720 MHz at 5.2 GHz bands. The other designed components are dual band power combiner and band pass filters. The designed front end elements meet the requirements of concurrent dual band system. Concurrent dual band transmitter characteristics were measured in the laboratory with the help of indigenously designed components along with available power amplifier, mixer and synthesizer.

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Review of Literature

1.1. Introduction

The trend in wireless communications is toward creating a network-ubiquitous era in the years to come. It will not be surprising that the next-generation mobile devices will become a universal multi-service wireless terminal. Yet, to operate a wireless device under different network protocols, a multi-standard transceiver is mandatory [1]. Although a multi-standard design can be achieved simply by duplicating more than one transceiver; this does not appear as an economical choice for manufacturing and further development. On the other hand, a fully reconfigurable transceiver (e.g., software-defined radio) befitting the wanted standards via block reconfiguration can effectively minimize the cost. The associated challenge is, of course, a wide-range tunable performance in each building block. These design considerations constitute a hard tradeoff between cost and design efficiency. For obtaining a fine compromise requires not only the extensive understanding of the basic transceiver architectures and standard requirements, but also an adequate knowledge of the state-of- the-art devices that have already hinted at many practical problem solving solutions [2].

The evolution of wireless networks involves enormous complexity and rapid changes between different generations as well as different applications. If we take mobile communications as an example. It is one of the fastest growing areas over the past decade. The first-generation mobile communication systems are analog systems designed to carry the voice traffic. The rapid growth in the number of subscribers and the proliferation of incompatible first-generation systems drove the evolution toward second-generation (2G) cellular systems. Multiple access techniques such as time division multiple access (TDMA), code division multiple access (CDMA), and global system for mobile communications (GSM) are used in the 2G systems [3]. Again, the spectrum shortage of current 2G communication systems results in a revolutionary instead of evolutionary approach to increase system capacity and support innovative broadband multimedia services. Third–generation (3G) mobile communication systems, which GSM and CDMA converge into a

single, official, globally roamable system, provide not only voice service but also data delivery. Therefore realizing multi-standard transceivers with maximum hardware reuse amongst the given standards is of great importance to minimize the manufacturing cost of emerging multiservice wireless terminals. A well-defined architecture in conjunction with a reconfigurable building-block synthesis is essential to formulate such a kind of tunable transceiver under a wide range of specifications. In this chapter, we present both fundamental and state-of-the-art techniques that help selecting transceiver architecture for single/multi-standard design. We begin by reviewing the basic schemes and examining their suitability for use in modern wireless communication systems (IEEE 802.11, Bluetooth, and ZigBee).

Similarly, in the short-distance wireless data communications, the wireless local access network (WLAN) as per IEEE 802.11 specifications has become the mainstream technology. The WLAN operates at the 2.4 and 5.2 GHz frequency bands with maximum network range of 150 ft and maximum theoretical data transmission rate of 54 Mb/s. Several standard versions coexist in IEEE 802.11 standard representing different generations of technological evolution. IEEE 802.11b specifies radios transmitting at 2.4 GHz and at speeds up to 11 Mb/s using direct sequence spread spectrum (DSSS) technology. Different carrier modulation methods ranging from BPSK, QPSK, 16QAM, to 64QAM were implemented in IEEE 802.11a using an orthogonal frequency division multiplexing (OFDM) technique. OFDM allows close-packed signal transmission for better channel utilization. The IEEE 802.11g standard is a high-speed standard at 2.4 GHz and is backward compatible with 802.11b. Other LAN or personal access networking (PAN) standards such as Bluetooth, HyperLAN, and IEEE 802.15 are among the wireless standards that are expected to be deployed and will use the unlicensed national information infrastructure (UNII) frequency band.

1.2. Need of Research

The worldwide demand for wireless service is experiencing explosive growth. Today there is an increasing demand for additional services along with the traditional and standard wireless services. With the rapid increase in the use of mobile terminals for wireless

communication, research on mobile terminal operating at multiple communication protocols has been attracting more and more interest. Moreover a user wants to make the best use of the available wireless device and expects the device to provide him with multiple services at the same time. A single device providing multiple functionalities reduces the burden of carrying multiple devices. Conventionally, a wireless device operates in a specific frequency band as required for some specific application. Moreover, a radio transceiver is designed for a narrow bandwidth which restricts its functioning at other frequencies for other applications. Most of the research efforts performed during the last few years dealt with issues related to the physical layer of the communication stack. However, despite the growing interest in multi-standard operation, less attention has been devoted to the radio-frequency front-end, which therefore remains one of the most challenging parts of a multi-band radio transmitter.

During the recent years, network providers have come out with support to a variety of communication access technologies to offer different wireless services. These access technologies need to be broadcast at different frequency bands. So a multi-band wireless device is needed to support these different access technologies from the same device. Providing such multi-band facilities in a single device results in high complexity and cost. During the recent years, the focus of RF designers has moved from providing the highest possible performance to providing the most affordable and cost-effective solution. Providing a cost effective solution for the design of such a multi-band transceiver front end is a challenging task.

A wireless transceiver is generally composed of two major building blocks. The Base-Band (BB) processor and the Radio Frequency (RF) front-end. The base-band processor is responsible for digital modulation and channel coding and it is relatively easy to configure the BB processor through software reprogramming to support multi-band operation. However, it is much more difficult to configure the RF front-end for multi-band operation to provide optimal network usage as it is composed of analog blocks like filters and amplifiers whose performance is frequency dependant.

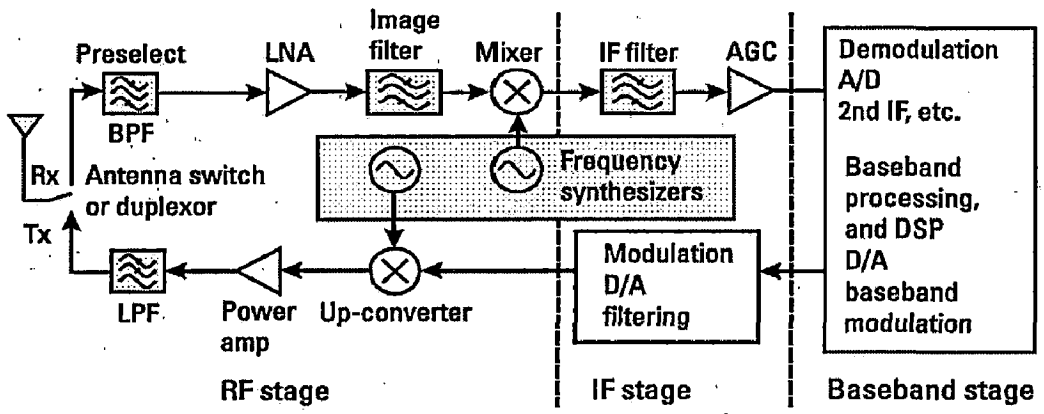

Figure 1.1: Typical Transceiver Block Diagrams [4]

One main reason for the delay in effectively implementing multi-band RF transceivers can be attributed to the implementation of the multiband matching networks. Figure 1.1 shows a block diagram of a typical communication transceiver. It consists of a transmit side and a receiver side. Power Amplifier is used in the transmit side of the transceiver in order to successfully transmit data over large distances through the lossy media. A power amplifier amplifies the signal to be transmitted so that it can be successfully received at the receiver end after traveling large distances through the atmosphere. All building blocks are generally designed for a single-band or a wide-band operation. Multiband design of these blocks is open for research.

Multiband and multi-standard architectures have revolutionized the field of communication since their arrival in the field. They became all the more important as communication technologies advanced in leaps and bounds over the years and wireless technology made its presence felt in a huge way. The advent of the wireless systems as well as their evolution over the years has acted as a catalyst to develop and then enhance multiband networks. Therefore Radio Frequency Integrated Circuits (RFICs), form a major part of the wireless communication systems [5].

1.2.1. *Different Approaches Used in Concurrent Systems*

A literature review is the first step to any design. A comprehensive literature review reveals different possible ways in which dual band operation can be achieved in a circuit. Dual band operation has been achieved in passive as well as active devices. In active devices, dual band performance has been achieved in linear as well as the non-linear mode of operation [6-9]. Entire receiver and even transceiver chips have been designed to operate in dual band. The following types of architectures have been used to design dual band circuits.

(A) Parallel Architecture

In this conventional approach, the receiver has different paths for each individual frequency. Therefore, each frequency band has its own matching circuit and transistor for an LNA, mixer etc. This kind of architecture occupies a lot of die area since it is equivalent to combining the components of different receivers on a single chip [6, 10]. This architecture has the advantage of low interference and each stage can be optimized separately. However, owing to the large die area it occupies, the layout and PCB designing becomes difficult.

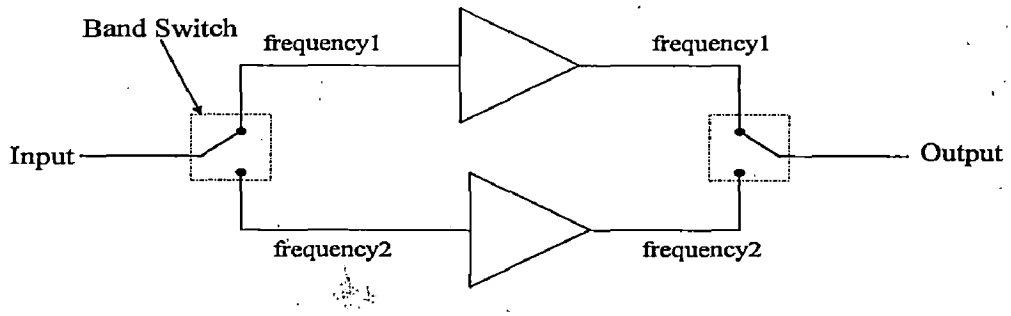

Figure 1.2: Parallel Architectures

(B) Switched Network Architecture

A variation to the parallel architecture can be having a switched network which chooses the path corresponding to the incoming RF frequency. The switch at the input of the circuit performs selection between the parallel paths for the incoming frequencies. Also, switched inductor networks have been used in practice which do away with the parallel paths but use the transistor model to change the equivalent value of the lumped components in the matching network such that, the same matching network can serve for both the incoming

frequencies. For example, a FET maybe a part of the matching network so that the transistor gets switched on for only one of the incoming frequencies. The capacitance of the FET model i.e. C_{ds} and C_{gs} can change the equivalent capacitance in the matching network. However, this method is effective for the operation of dual band networks but not for tri band etc [7, 11].

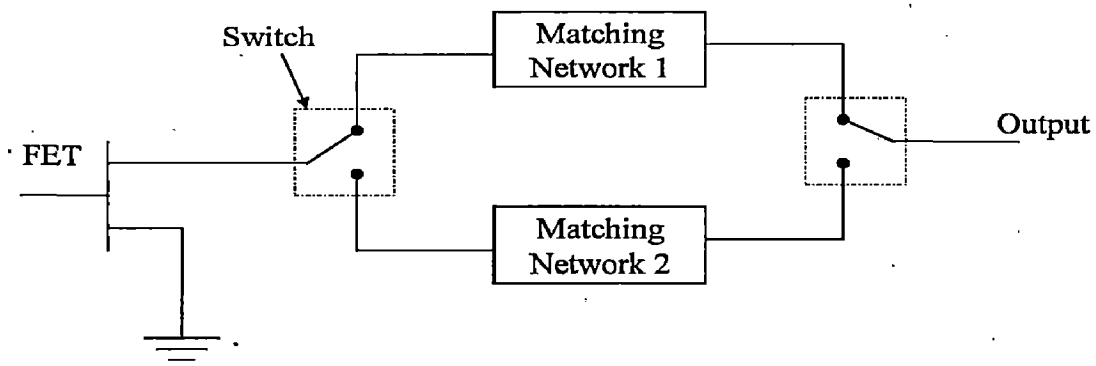

Figure 1.3: Switched Network Architectures

(C) Concurrent Architecture

In this architecture, the same receiver architecture is designed in a way to receive more than one frequency simultaneously. This architecture can result in a very compact die area. For example, a concurrent LNA can simultaneously amplify two or more incoming bands. However, the design of such architecture is extremely challenging and an optimum gain cannot be achieved for all the bands. In other words, a compromise has to be made in the amount of gain achieved [12-14].

(D) Wideband Architecture

This is strictly not dual band architecture. In this architecture, the matching networks are designed to function over an entire frequency range. The matching network is first designed at the centre frequency and then optimized to operate over the entire frequency range. The challenge is to optimize the wideband network in such a way that acceptable if not optimum performance can be achieved over the entire range of frequencies [6].

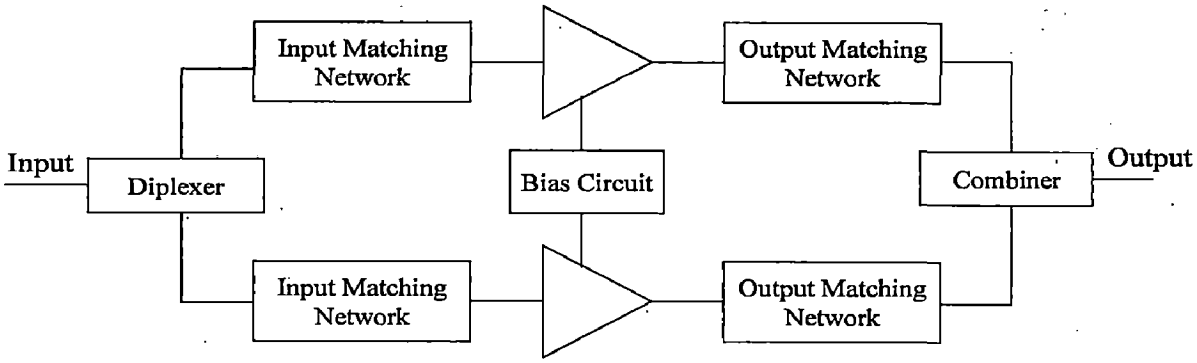

Figure 1.4: Concurrent Dual-band Architecture

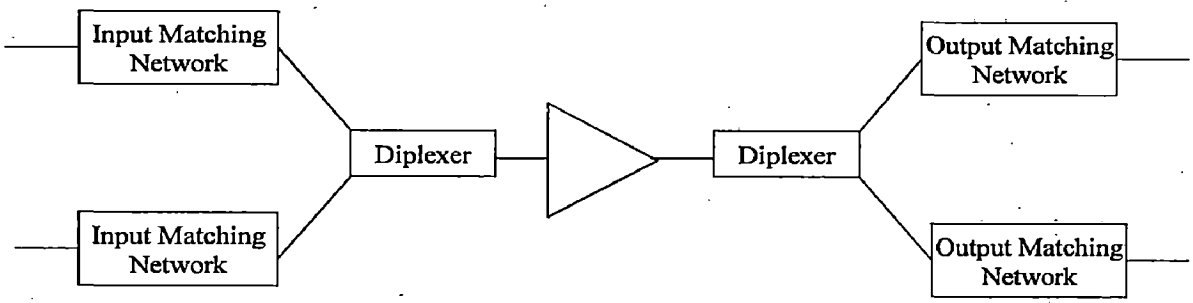

Figure 1.5: Concurrent Dual-band Parallel Architecture

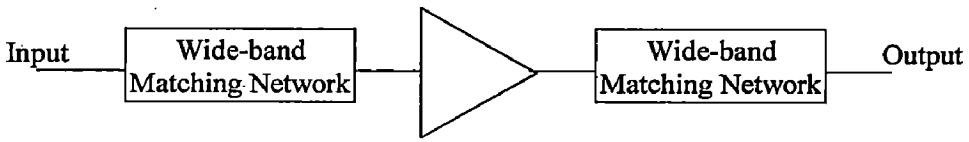

Figure 1.6: Wideband Architecture

Each of the architectures has its own advantages and disadvantages. However, concurrent and wideband architectures have been used extremely efficiently in circuits where the space constraints are at a maximum. However, some tradeoff in terms of the gain has to be made as it is virtually impossible to obtain optimal performance at both the frequencies. The basic design aim is to achieve acceptable performance at both the desired frequencies of operation. This has been achieved in passive networks like couplers, power dividers etc. As for the circuits using active devices tremendous success has been achieved in designing LNA especially in all the different kinds of architectures.

1.3 Problem Statement

The investigation reported in this dissertation are aimed to

(a) Develop a concurrent Dual-band transmitter RF front-end for 2.4/5.2 GHz wireless application.

(b) Develop a concurrent Dual-band receiver RF front-end for 2.4/5.2 GHz wireless application.

1.4 Organization of the Dissertation

This dissertation is organized as follows:-

Chapter 1 explains a literature survey of the work reported on multi-band communication system and its advantages, and different schemes for achieving multiband response.

Chapter 2 presents fundamentals of transceiver design. This includes basic design considerations of transmitter and receiver followed by issues related to standard architectures like superheterodyne, homodyne. This also includes a brief review of concurrent architectures. And after that proposed architecture for transmitter and receiver RF front-end discussed.

Chapter 3, in this chapter all passive components (i.e. filters, dual-band power combiner, dual frequency antenna) that are design and implemented in this work are discussed in details i.e.

Chapter 4 deals with a development of concurrent dual-band low noise amplifier designs and focus on some dual- matching network design.

In *Chapter 5*, finally development of Dual-band transmitter's RF front-end and receiver's RF front-end discussed. This is also includes the experimental setup for measurement of various characteristic of transceiver.

Finally, *Chapter 6* summarizes a conclusion/discussion of the work done and suggests scope for future work on the "Analysis, design and implementation of concurrent dual-band (2.4/5.2GHz) wireless transceiver" used in the dissertation.

Fundamentals of Transceivers Architectures

2.1 Introduction

It basically composed of transmitter as well as receiver module and their operation may be share by a device known as duplexer or may not be share, In case of independent, individual antenna must be required.

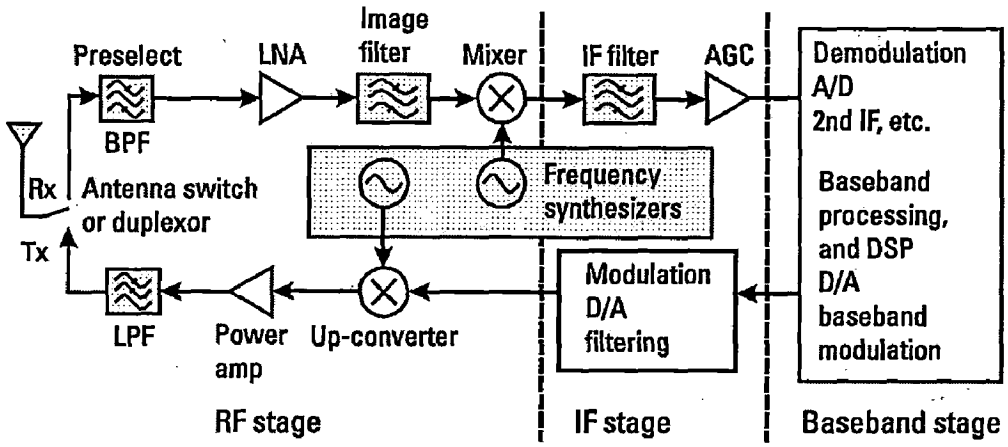

Figure 2.1: Basic Transceiver Architecture

Basic transceiver components are low noise amplifiers (LNA), power amplifiers (PA), mixers (up-converters and down-converters), filters, Oscillators and transmit/receive switches etc.

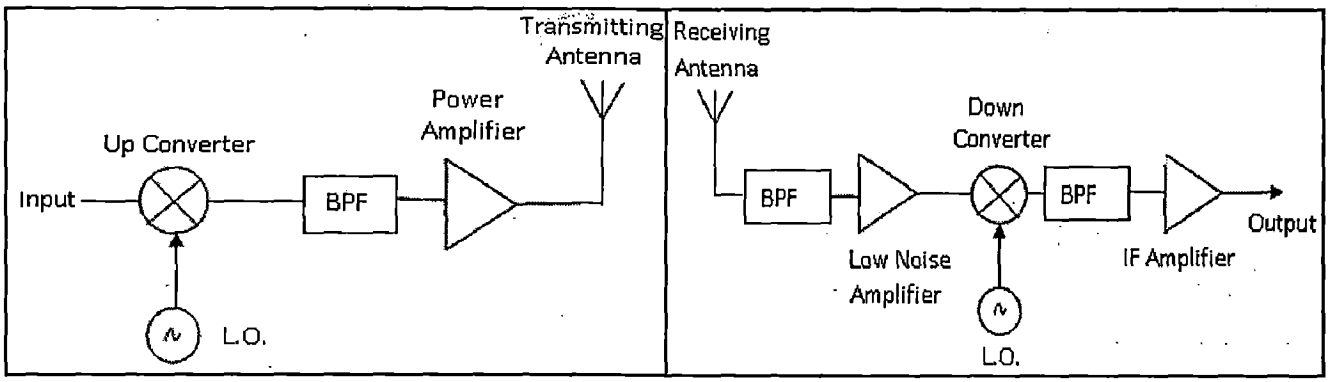

Figure 2.2: Basic Transmitter and Receiver RF front-end

2.2 Basic Design Considerations

2.2.1 Receiver Architectures

2.2.1.1 Super heterodyne Receiver

The high reliability of super-heterodyne receiver has made it the dominant choice for many decades. Its generic scheme is shown in figure 2.3. With a band-selection filter rejecting the out-of-band interference, the in-band radio frequency (RF) channels are free from amplification by a low-noise amplifier (LNA). A high-Q off-chip image-rejection filter prevents the image channel from being superimposed into the desired channel in the RF-to-intermediate frequency (IF) downconversion. The channel selection requires a voltage-controlled oscillator (VCO) driven by an RF frequency synthesizer and a high Q off-chip surface-acoustic-wave (SAW) channel-selection filter (CSF). The signal level of the selected channel is properly adjusted by a programmable-gain amplifier (PGA) prior to the IF-to-baseband (BB) quadrature downconversion. This downconversion requires another phase-locked loop (PLL) and a quadrature VCO (QVCO) for generating the in-phase (I) and quadrature-phase (Q) components.

The baseband (BB) low pass filters (LPFs) are of low-Q requirement but high in filter order for ultimate channel selection. The BB PGAs adjusts the signal swing for an optimum-scale analog-to-digital (A/D) conversion. The superior I/Q matching because of low operating frequency, as well as the avoidance of dc-offset and $1/f$ noise problems, are the pros of super-heterodyne. On the other hand, the low integration level and high power consumption for the on/off-chip buffering are the major constraints.

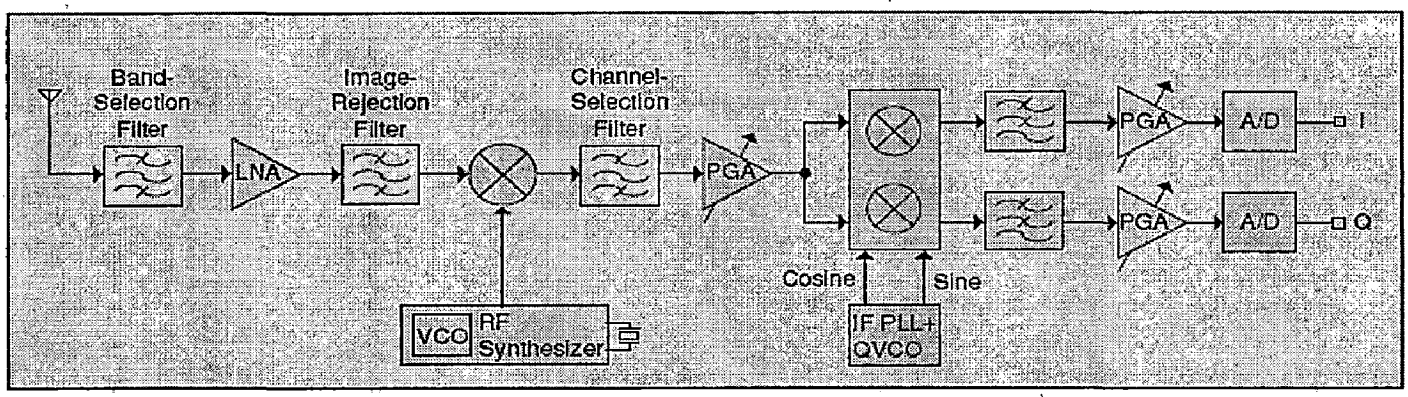

Figure 2.3: Super heterodyne Receiver [2]

There also exists a tradeoff in IF selection, a high IF (e.g. ~70 MHz) improves the sensitivity due to higher attenuation can be offered by the image-rejection filter, while a low IF (e.g., ~10 MHz) enhances the selectivity due to a lower Q requirement from the SAW filter. On the other hand, due to the restricted IF choice of 10.7 or 71 MHz for commercial filters, a multi-standard design normally constitutes a high cost for filtering at different IFs.

2.2.1.2 Image Reject RX: Hartley and Weaver

The principle of image-rejection RX is to process the desired channel and its image in such a way that the image can be eliminated eventually by signal cancellation. Hartley [15] proposed such an idea with the architecture shown in figure 2.4 (a). The RF signal in the downconversion is split into two components by using two matched mixers, a QVCO and an RF frequency synthesizer. The outputs, namely in-phase (I) and quadrature- phase (Q), are then filtered by the LPFs. With a 90^0 phase-shifter added to the Q channel, the image can be canceled after the summation of I and Q outputs. In practice, a perfect-quadrature downconversion and a precise 90^0 phase-shifter cannot be implemented in an analog domain, especially at high frequency. The practical values of static gain/phase mismatches are 0.2 to 0.6 dB /1^0 to 5^0, corresponding to an image rejection of roughly 30 to 40 dB.

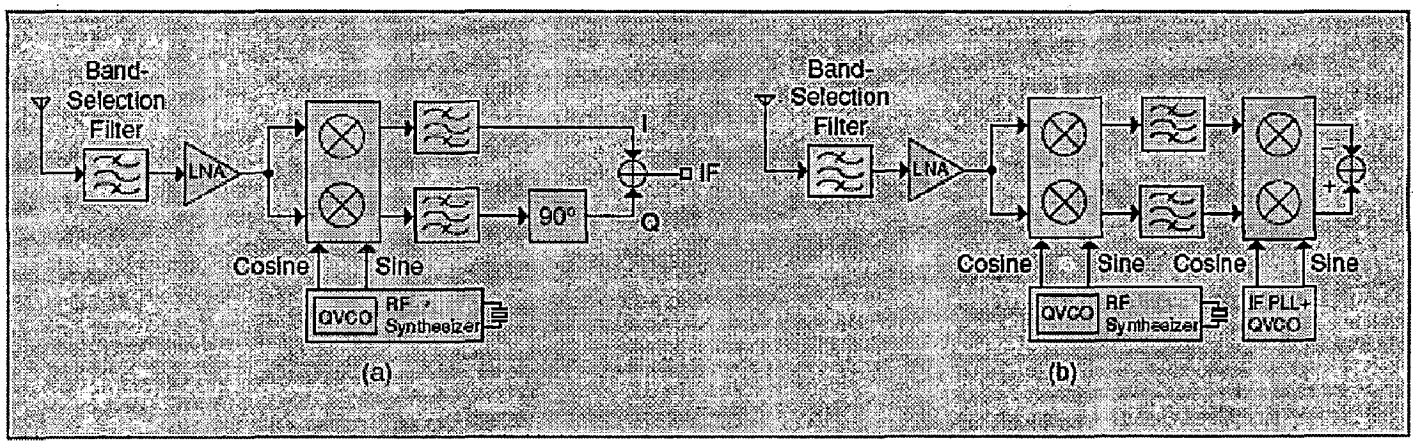

Figure 2.4: Image Rejection Receiver [2] (a) Hartley (b) Weaver

The Weaver [16], as shown in Figure 2.4 (b), is identical to Hartley's one except that the 90^0 phase-shifter is replaced by a quadrature downconverter. The key advantage of such a replacement is related with the fact that a downconverter can realize relatively much

wideband quadrature matching. The overheads are the additional IF mixers, PLL and QVCO. Both Hartley and Weaver schemes feature high integratability and are convenient to use in multi-standard design.

2.2.1.3 Zero-IF Receiver

Similar to an image-reject RX, a zero-IF RX obviates the need to use any off-chip component. As shown in figure 2.5, the desired channel is translated [17] directly to dc through the I and Q channels. The image is eliminated through signal cancellation rather than filtering. Since the image is the desired channel itself, the demanded I/Q matching is practically achievable for most applications. The fundamental limitation of the zero-IF RX is its high sensitivity to low-frequency interference, i.e., dc offset and $1/f$ noise. With them superimposed on the desired channel, a substantial degradation in signal-to-noise ratio (SNR) or complete desensitizing (unable to receive a weak radio signal) of the system due to a large baseband gain may result. A capacitive coupling and a servo loop are common choices to improve this problem, but at the expense of long settling time and large chip area for realizing the very low cutoff frequency high-pass pole.

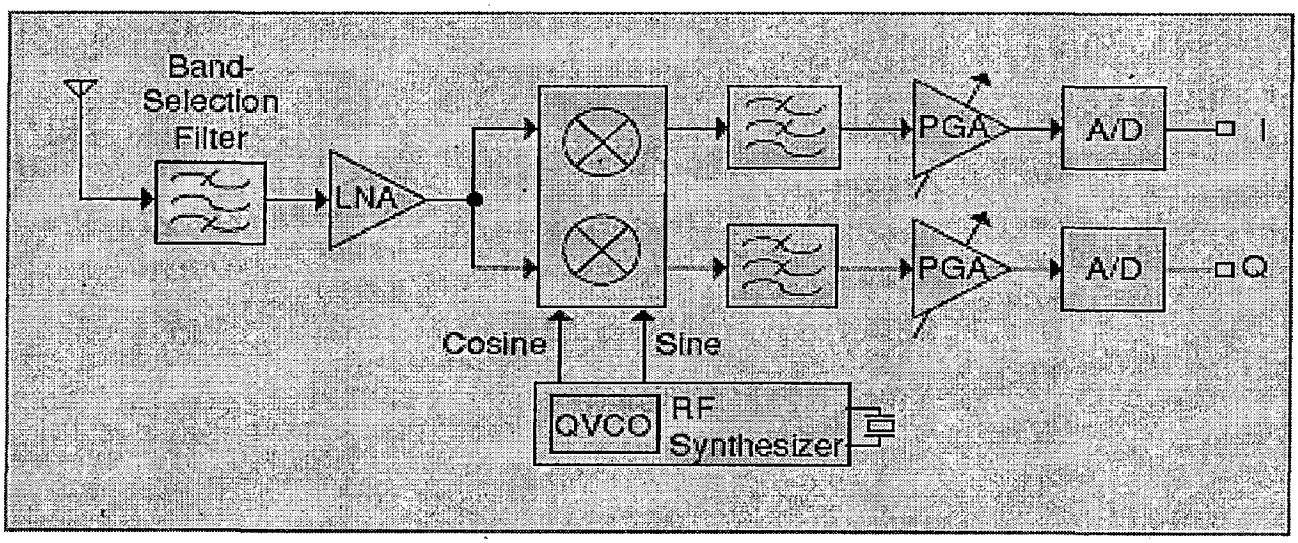

Figure 2.5: Zero IF Receiver [2]

2.2.1.4 Low-IF Receiver

The Low-IF RX [18] features a similar integratability as the zero-IF one but is less prone to the low-frequency interference. The desired channel is down-converted to a very low-frequency bin around dc, typically ranging from a half to a few channel spacing. Unlike the zero-IF RX, the image is not the desired channel itself. The required image rejection is normally higher as the power of the image can be significantly larger than that of the desired channel. Depending on the variation of the building blocks, a low-IF RX can have four different architecture, as shown in, Figure 2.6, (a) to (d).

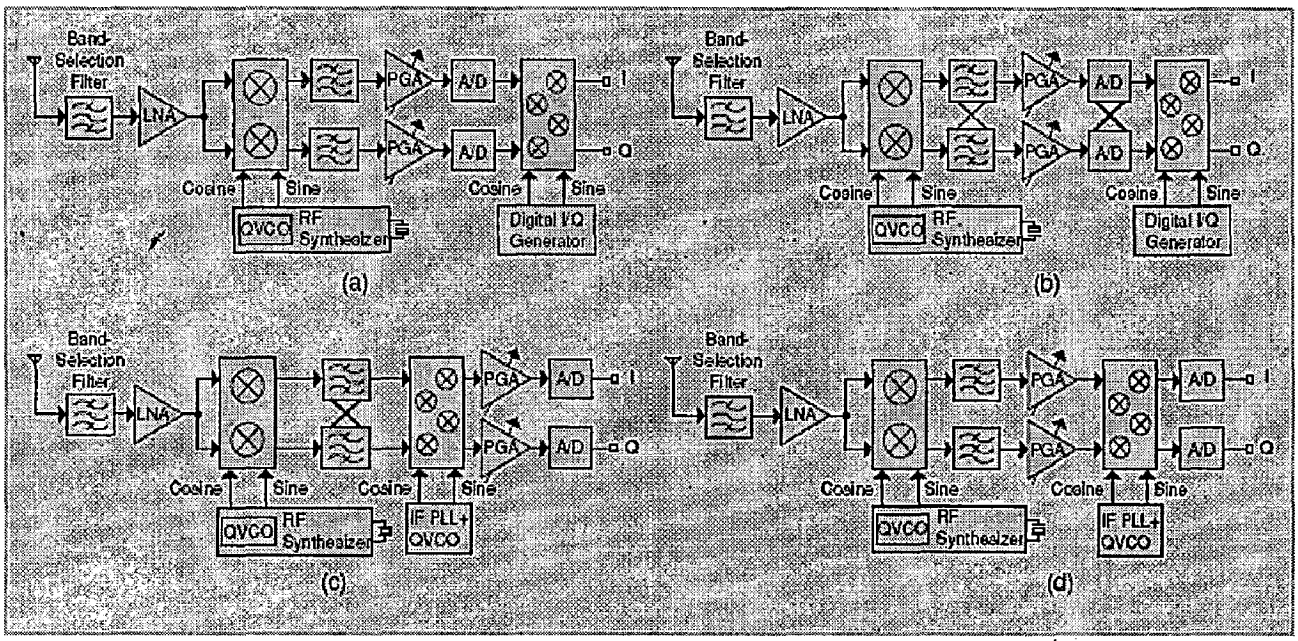

Figure 2.6: Low-IF Receiver [2](a) Case-1 (b) Case-2 (c) Case-3 (d) Case-4

Case-1: Performs the IF-to-BB downconversion digitally, eliminating the secondary image problem while permitting a pole-frequency relaxed dc-offset cancellation adopted in the analog BB. The disadvantages are a higher bandwidth requirement (compared with the zero-IF) from the LPFs and PGAs, and a higher conversion rate required from the A/Ds.

Case-2: Identical to Case-1 except the LPFs are replaced by a pair of filters operating in the complex domain, namely a polyphase filter or complex filter. Such a filter performs not only channel selection, but also relaxes the I/Q matching requirement from the PGAs and A/Ds.

Case-3: Another combination employing a complex filter together with an analog IF-to-BB downconverter for doubling the image rejection. With such a structure, the I/Q matching required from the following PGA and A/D is very relaxed. The bandwidth of the PGAs and the conversion rate of the A/Ds are reduced to their minimum like zero-IF. The associated overhead is a low cutoff frequency high-pass pole in the dc-offset cancellation that is necessary in the PGAs due to the high baseband gain. The chip area impact is therefore very significant since the systems containing I and Q channels are typically differential (i.e., four high-pass poles).

Case-4: Positions an analog IF-to-BB downconverter prior to the A/Ds such that the conversion rate of the A/Ds can be minimized. Unlike in Case-3, the pole-frequency of the dc offset cancellation circuit can be relaxed. Comparing with the zero-IF RX, the low-IF RX is less sensitive to $1/f$ noise and dc offset at the expense of a higher image rejection requirement.

Table 2.1: Comparison of Different RX Architectures

RX arhcitecture	Advantages	Disadvantages
Superheterdyne	-Reliable performance -Flexible frequency plan -No DC-offset and 1/f noise	-Expensive and bulky, high power -Difficult to share the SAW filter for multiband
Image-Reject (Hartley and Weaver)	-Low cost -No DC-offset and 1/f noise -High integratbility	-Quadrature RF-to-BB down-conversion -Suffer from first and secondary images -Narrow band (Hartley) -High I/Q matching
Zero-IF	-Low cost -Simple frequency plan for multistandard -High integratability -No image problem	-Quadrature RF-to-BB downconversion -DC-offset and 1/f noise problem
Low-IF	-Low cost -High integratability -Small DC-offset and 1/f noise	-Image is a problem -Quadrature RF-to-IF and double quadrature IF-to-BB downconversion

2.2.2 *Trasmitter Architecture*

2.2.2.1 Super-heterodyne Transmitter

Architecturally, the superheterodyne TX, Figure 2.7 is a reverse of operation from its RX counterpart with the A/D conversion replaced by a digital-to-analog (D/A) conversion. However, they are very different in the design specification. For instance, in transmission, only one channel will be up-converted in the TX. Its power level is well-determined throughout the TX path. There are differences in the signal reception, the power of the incoming signals is variable and the desired channel is surrounded with numerous unknown-power in-band and out-of-band interferences. Thus, PGAs is essential for the RX to relax the dynamic range of the A/D converter, but can be omitted in the TX if the power control could be fully implemented by the power amplifier (PA). Similarly, since the channel in the TX is progressively amplified toward the antenna and finally radiated by a PA, the linearity of the whole TX is dominated by the PA. Whereas it is the noise contribution of the LNA that dominates the whole RX noise figure.

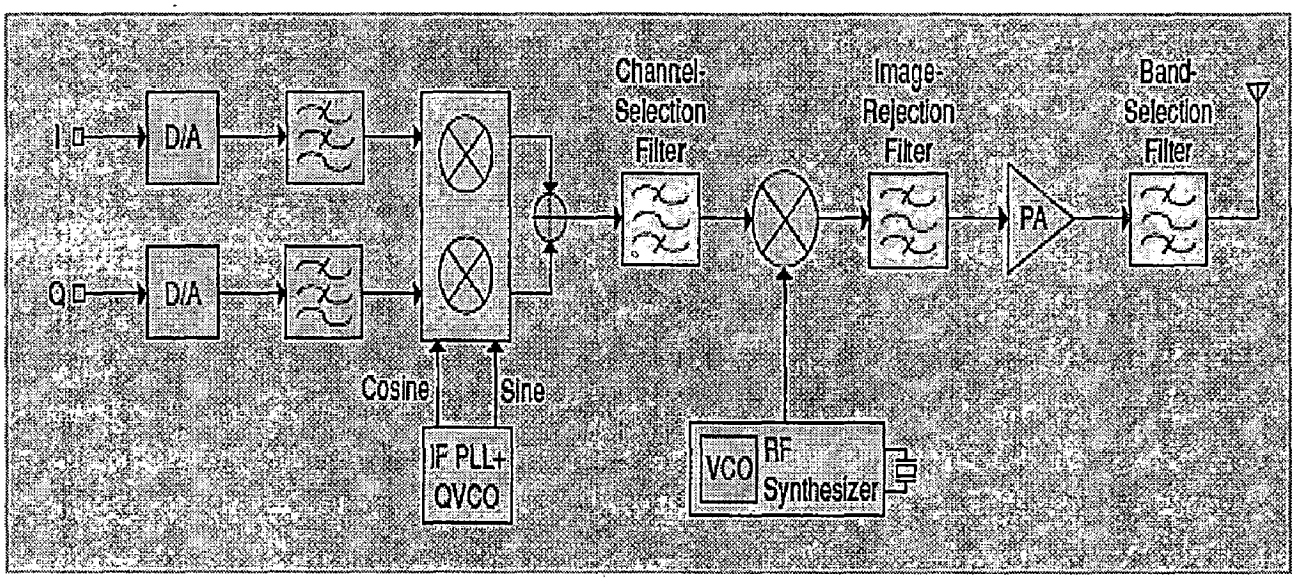

Figure 2.7: Super-heterodyne Transmitter[2]

2.2.2.2 Direct-up Transmitter

The direct-up TX (Figure 2.8) features an equal integratability as the zero-IF RX, but is limited by the well-known LO pulling. To meet the standard required modulation mask, techniques such as offset VCO and LO-leakage calibration are somehow necessary. Again, it is noteworthy that albeit the functional blocks in RX and TX are identical, their design specifications are largely different. For instance, the receivers LPF's has to feature a high

out-of-band linearity due to the co-existence of adjacent channels, whereas it is not demanded from Transmitter LPF.

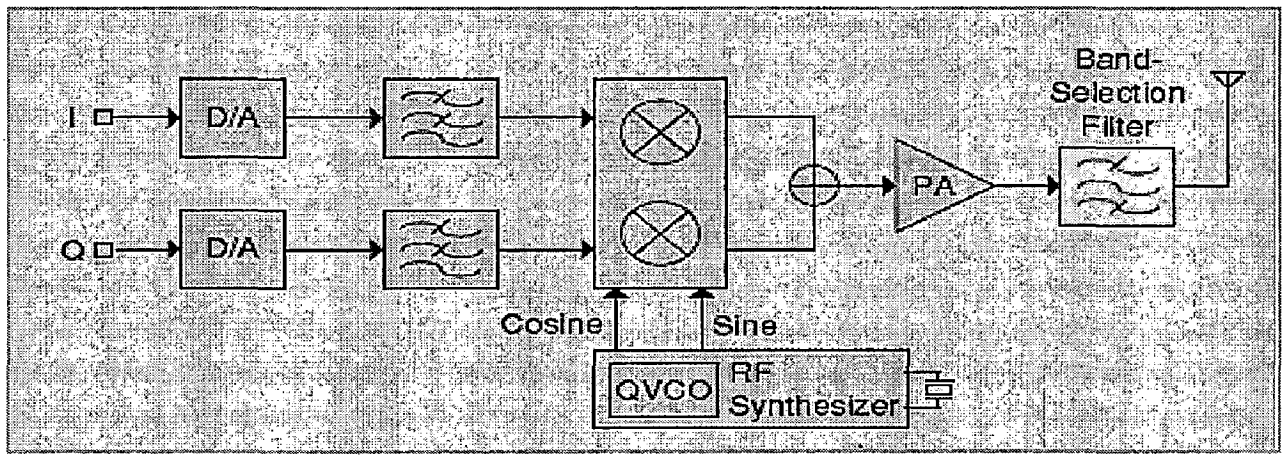

Figure 2.8: Direct-up Transmitter[2]

2.2.2.3 Two-step Transmitter

Similar to the low-IF RX, two-step-up TXs can be structured into four possible schemes as shown in Figure 2.9 (a) to (d).

Case-1: Frequency-up-translates the desired channel digitally prior to digital to analog D/A conversion such that the low frequency interference from the D/A and LPF can be canceled by means of an ac-coupling or a servo loop, avoiding the transmission of DC-to-LO-mixing products. In this case, the required conversion rate of the D/A and the bandwidth of the LPF must be increased.

Case-2: Employs complex filters to reject the image resulting from I/Q mismatch between I and Q, digital to analog convertors and filters to improve the purity of the output spectrum. Other properties are similar to Case-1.

Case-3: Alternatively employs an analog BB-to-IF up-converter to reject the image. With such a variation, only an LPF would be required and the output spectrum is purified.

Case-4: Locates the analog BB-to-IF up-converter between the D/A converter and complex filters, delivering doubled image rejection and allowing a capacitive coupling (or by a servo loop) between the up-converter and filter, and between the filter and IF-to-RF up-converter.

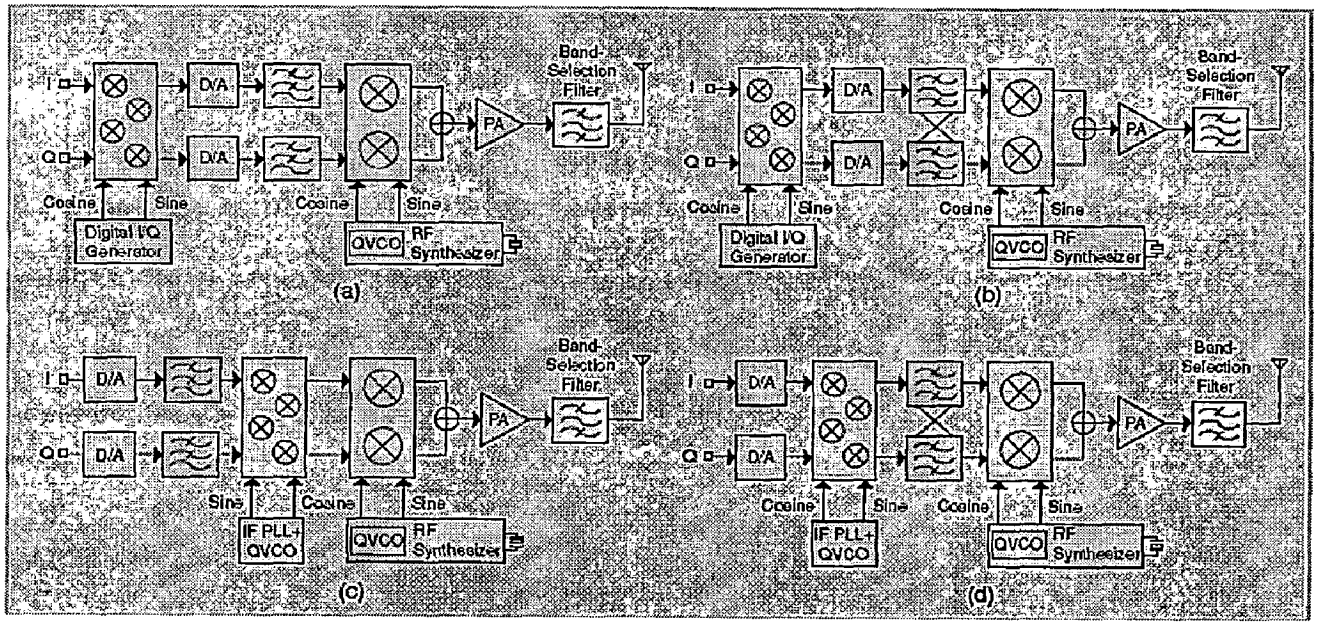

Figure 2.9: Two step-up Transmitter[2] (a) Case-1 (b) Case-2 (c) Case-3 (d) Case-4

One key advantage of this scheme is the allowance of independent dc biasing for each block. Compared with the direct-up TX, the LO feedthrough is reduced (of course, the amount depends on the selected IF and port-to-port isolation) as the first and second VCOs can be offset from each other (i.e., LO = VCO1 + VCO2). The overheads are the additional power and area consumption required for the mixing, filtering and frequency synthesis.

Table 2.2: Comparison of Different TX Architectures

TX arhcitecture	Advantages	Disadvantages
Superheterdyne	-Reliable performance -Flexible frequency plan -No LO leakage -simple DC-offset cancellation at BB	-Expensive and bulky, high power -Difficult to share the SAW filter for multiband
Direct up	-Low cost -No image problem -High integratbility -Simple frequency plan for multistandard	-Quadrature RF-to-BB downconversion -LO leakage -DC-offset cancellation is difficult at BB
Two-step Up	-Low cost -High integratability -Simple DC-offset cancellation at BB	-Quadrature IF-to-RF and double quadrature BB-to-IF downconversion -LO leakage -Image problem

2.3 Concurrent Transmitter Architectures

Transmitter architectures for concurrent multi-band applications will primarily depend on how concurrent transmission is defined. In one scenario, same signal needs to be sent over multiple frequency bands so as to ensure reliable communication through the use of frequency diversity scheme. On the other hand, a more probable case demands for the transfer of two or more different data signals over their respective multiple frequency bands.

2.3.1 Same Data on All Supportable Frequency Bands

Dual-band implementation of such a system simultaneously up-converts single baseband data signal to two different frequency bands. High immunity to both the frequency pulling and the LO (local oscillator) leakage to output makes the two-step up-conversion scheme preferable over the homodyne solution for such a case. Below-mentioned Figure 2.10 depicts a possible concurrent dual-band transmitter implementation, using two-step conversion method.

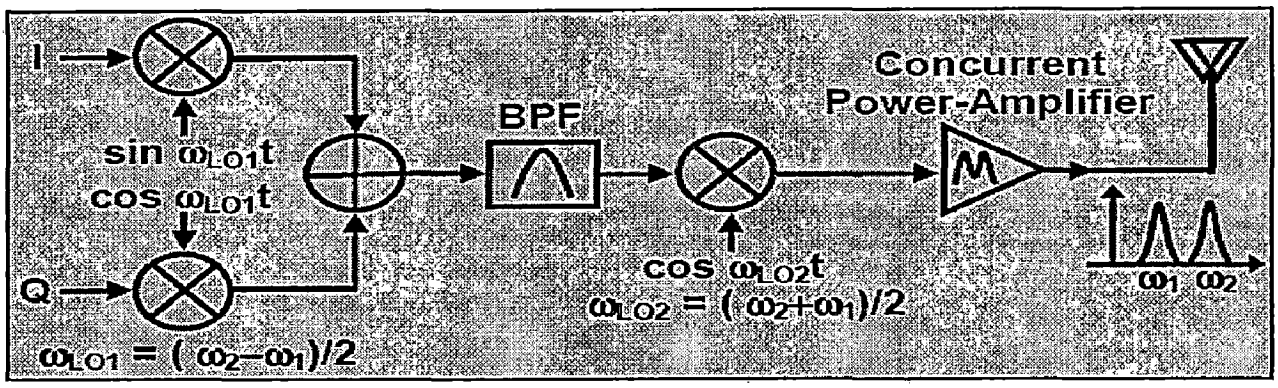

Figure 2.10 : Concurrent Dual-band Transmitter (Same data on both the frequency bands) [18]

2.3.2 Different Data on their Respective Different Frequency Bands

A most likely commercial situation may demand for simultaneous transmission of different data at their respective different frequency bands, e.g., transmitting voice and internet data at two different bands and the operation each component is same as dicussed in previous sections.

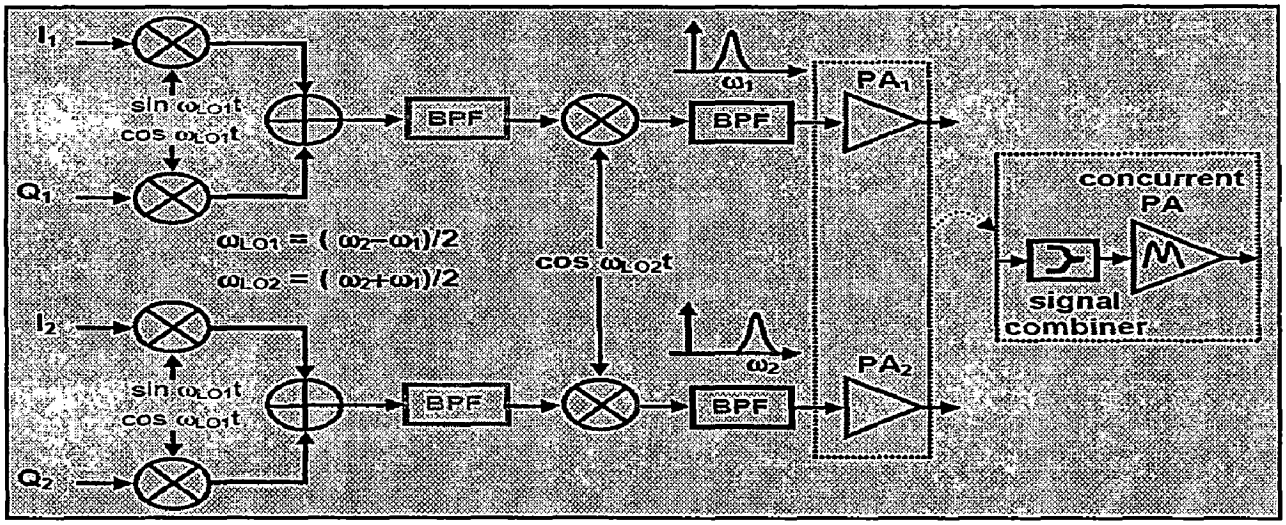

Figure 2.11: Concurrent Dual-band Transmitter (Different Data on different bands) [18]

2.4 Concurrent Receiver Architectures

It is well-known for portable hand-held device design of receiver architectures that target smaller chip area and low power consumption for long battery life. Therefore, throughout this section, the architectures are presented by designers based on their success in achieving the aforementioned desired goals.

2.4.1 Parallel Single-Band Receivers

Parallel combination of a number of single-band receivers, each supporting a different frequency band, seems the most trivial design scheme for the implementation of a concurrent multi-band receiver.

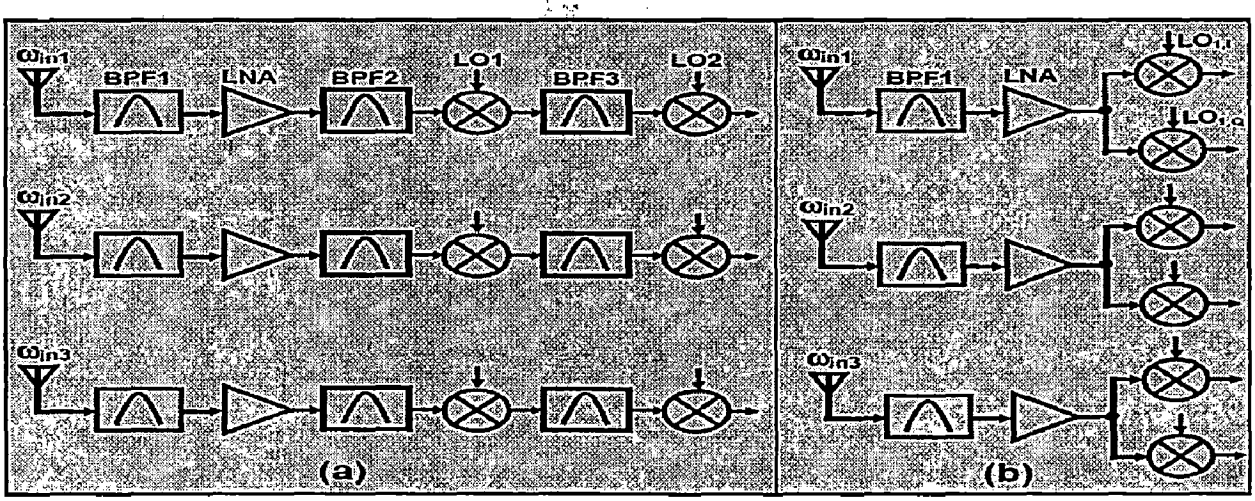

Figure 2.12: Concurrent Receiver Implementations Using Multiple Parallel Single-Band Receivers (a) Heterodyne (b) Direct Down-Conversion Architectures [18]

2.4.2. Parallel Receivers with a Wide-Band Front-End

This type of architecture employs a wide-band front-end followed by a number of parallel down-converters. The wide-band front-end consists of an antenna and a low-noise amplifier (LNA), both of which allow collection of signal powers from a large range of frequencies. Thereafter, subsequent parallel down-converter stages are used to receive any number of frequency bands within that range. The figure 2.13 depicts a broadband front-end followed by separate down-conversion parallel paths for each frequency band.

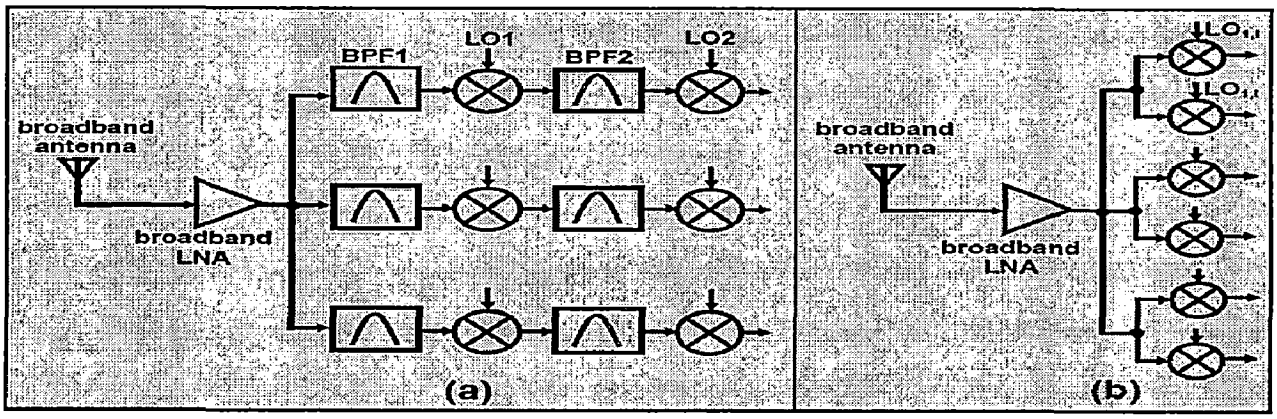

Figure 2.13: Concurrent Receiver Implementation using Wide-Band front-end (a) Heterodyne (b) Direct Down-Conversion Architectures [18]

In comparison with the previously mentioned method, sharing of front-end elements seems to be advantageous in terms of chip area and/or power consumption. In actuality, this depends on the implementations of the wide-band LNA. In addition, the antenna size can also play a critical role, since it usually increases with the required bandwidth.

Furthermore, the scheme exhibits a serious deficiency of amplifying undesirable frequencies and noise along with the frequency bands of interest. Due to inherent nonlinearities in any system, the receiver's potential dynamic range can be limited by these unwanted signals, particularly by those that have large signal powers.

2.4.3 Parallel Receivers with a Multi-Band Front-End

An enhanced version of the wide-band front-end based concurrent architecture redesigns the front-end components to support multiple narrow frequency bands of interest.

Figure 2.14 indicates examples of such a scenario. The scheme was first proposed by Hashemi et. al. [19, 20] wherein the multi-band front-end incorporated a multiband antenna, followed by a multiband filter and a concurrent multiband LNA. The LNA was designed so

as to provide simultaneous gain and narrow-band input matching with a low added noise at multiple frequency bands of interest. The architecture provided concurrent operation at the desired multiple frequency bands.

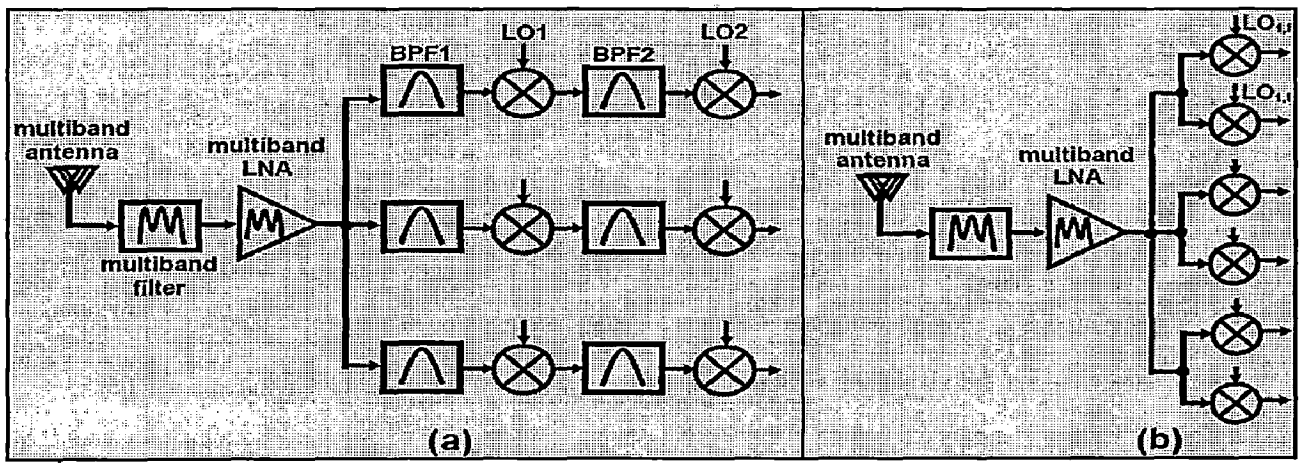

Figure 2.14: Concurrent Receiver Implementation Using Multi-Band front-end (a) Heterodyne (b) Direct Down-Conversion Architectures [19]

Such a scheme naturally filters out unwanted frequencies at the front-end itself, thus, relieving the architecture of (potentially) limited dynamic range. Moreover, similar to the previous scheme, the architecture eliminates an extra antenna, a front-end filter and an LNA, which in turn results in savings in power and area footprint.

2.4.4. Sharing Down-Converting Mixers among the Supportable Frequency Bands

The work in reference [20] implements a concurrent dual-band receiver, capable of simultaneous operation at 2.4 GHz and 5.2 GHz WLAN frequency bands so that it can be used to enhance data-rate and robustness of the wireless communication. It proposes an enhancement over the previously mentioned architecture in that it shares the mixer components so as to reduce required number of LO frequencies and external filters. Figure 2.15 depicts the proposed enhancement.

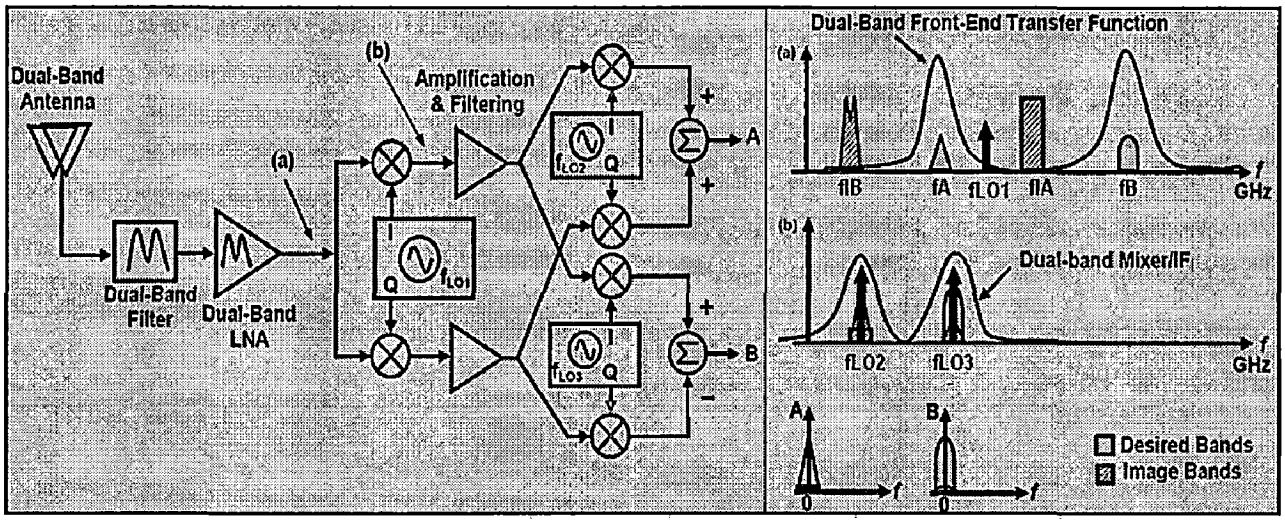

Figure 2.15: Architecture and Frequency Domain Signal Evolution [20]

Using a quadrature first LO makes the stage fit to act as the first half of any single-sideband image-reject architecture, similar to that proposed by Weaver [16]. Since the receiver has to demodulate two bands concurrently and independently, two separate paths must be used eventually. Each path comprises of the second half of the image-reject architecture, which provides further image rejection. The frequency of the first local oscillator (LO) that appears after the LNA and performs the first down-conversion determines the image frequency (.ies). The LO frequency is offset from the midpoint of the two bands of interest (f_A and f_B) in such a way that the image of the first band at f_A falls at the notch of the front-end transfer function at f_{IA}. In this way, attenuation at f_{IA} is determined by the combined attenuation of the dual-band antenna, the filter, and the LNA. Simultaneously, the image of the second band at f_B should fall outside the pass-band of the front-end, so that f_{IB} is attenuated appropriately.

In comparison to the previous scheme, the architecture eliminates an extra pair of high-frequency mixers. In addition to the novel concurrent image-reject architecture, diligent frequency planning, as indicated in figure 2.16, allows the use of only one frequency synthesizer for the entire receiver, thereby further reducing chip area and power consumption.

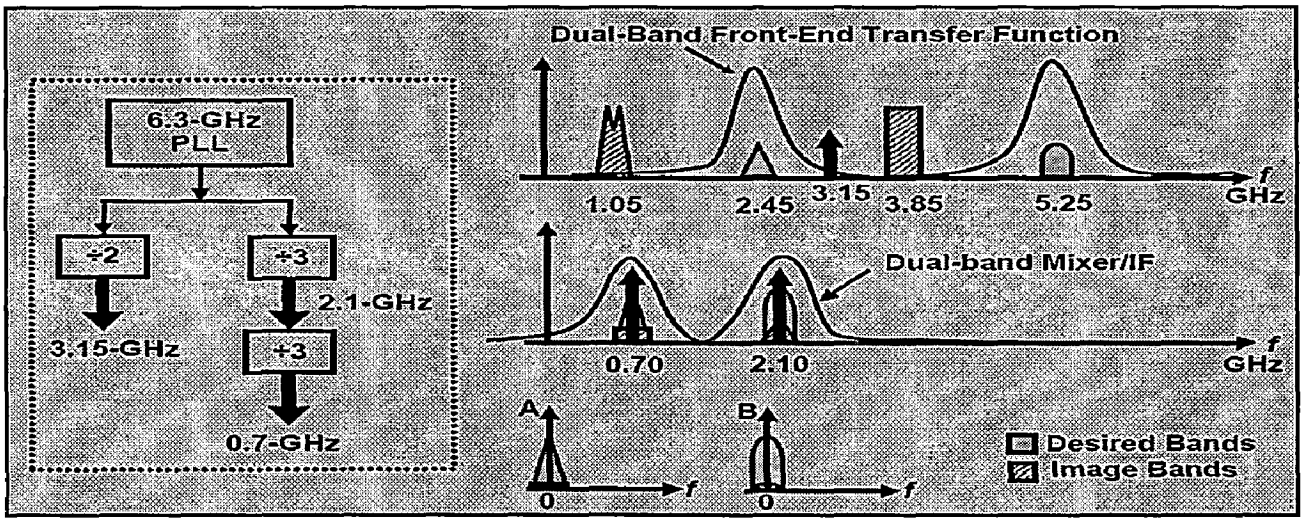

Figure 2.16: Frequency Planning in Concurrent Dual-Band Receiver [20]

Another approach, proposed by Chen et. al., [21] claims that when the two bands of interest are close enough, an integrated hybrid receiver architecture can be enhanced to one's own advantage. An example of such a scenario of close-by frequency bands can be found in dual-band GPS application. A dual-band GPS receiver can highly improve the positioning accuracy.

By comparing the two signals received at two different supportable frequency bands of L1 (1575.42-MHz) and L2 (1227.6-MHz). For such dual-band GPS application, the work proposes a concurrent receiver design that combines the low-IF and the Weaver architectures, by sharing their functional blocks, as shown in figure 2.16. In this way, not only hardware complexity but also circuit size and power consumption are reduced in comparison to conventional architectures with similar performances. The proposed receiver includes a common LNA, two mixers for I and Q paths and two frequency synthesizers, using same reference signal frequency.

In particular, the receiver uses the low-IF architecture to obtain L1 C/A code signals and the Weaver image-rejection architecture to obtain L2 carrier P code signals. The hybrid architecture employs a part of the Weaver architecture with a low-pass filter and a variable gain amplifier (VGA) to form the low-IF architecture that receives L1 signals for C/A codes. Simultaneously, full Weaver architecture receives L2 signals for precision P codes. The frequency is planned in such a way that center frequencies of final output signals for the L1- and the L2-band signals are positioned at 1.18-MHz and 12.114-MHz, respectively. This

requires local oscillator frequencies of 1574.24-MHz and 334.526-MHz for the first and the second mixers, respectively. Since the architecture simultaneously manipulates both the L1- and the L2-band signals, therefore, no changes are required in the oscillation frequencies (and, hence, locking times) for switching between the receiving paths. However, a crucial issue with the design is that the L2-band signal exhibits worse linearity and noise figure than the L1-band signal. This is because of the fact that the L2-band signal is required to go through one more step of down-conversion than the L1 -band signal.

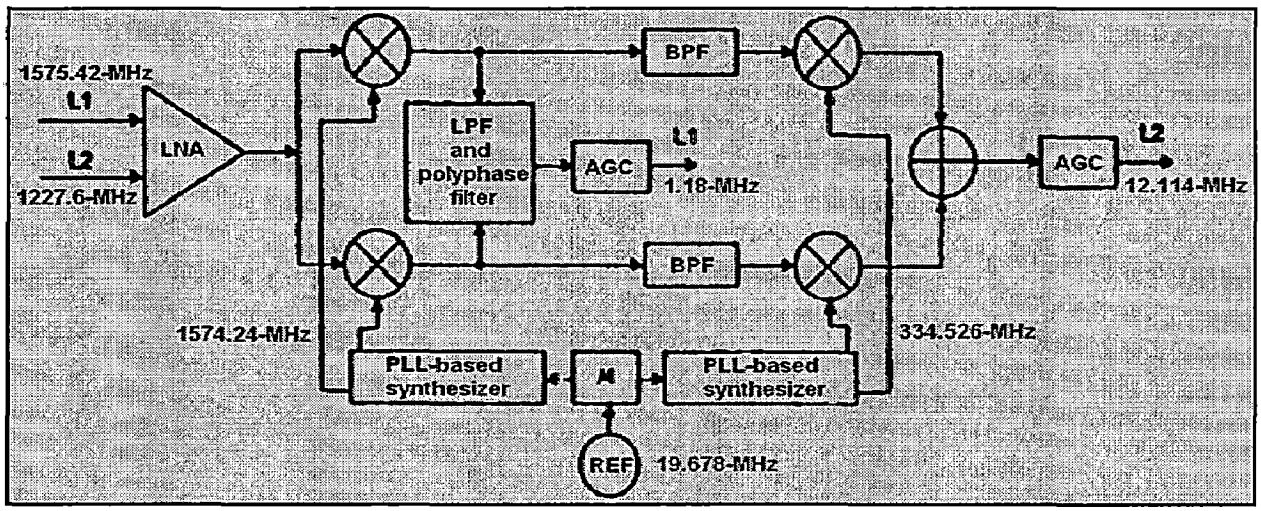

Figure 2.17: Concurrent L1 and L2 Bands GPS Receiver using An Integrated Low-IF and Weaver Architecture [21]

2.4.5. Multi-Band Sub-Sampling Receiver

The scheme proposes band-pass sub-sampling of the multi-band signals, as shown in figure (2.7). This provides the advantage of very low sampling rates, in comparison to any of the carrier frequencies of input signals. A major concern with the process involves careful estimation of permissible sampling rates, so that the shifted versions of the multi-band signals do not overlap. Besides it, increase in in-band noise, due to noise-folding, plays a critical role in selection of an appropriate sampling frequency. Generally, the frequency bands of interest in concurrent multi-band applications may neither exhibit equal spacing in frequency domain nor possess equal bandwidth. This necessitates very low sampling rates, which, in turn, results in an increase in-band noise. The issue can be tackled by employing front-end multi-band filtering to limit the effect of out-of-band noise. In addition, by giving

preference to multi-band filtering over a wide-band front-end, one reduces the effect of undesirable interferences on the receiver's dynamic range

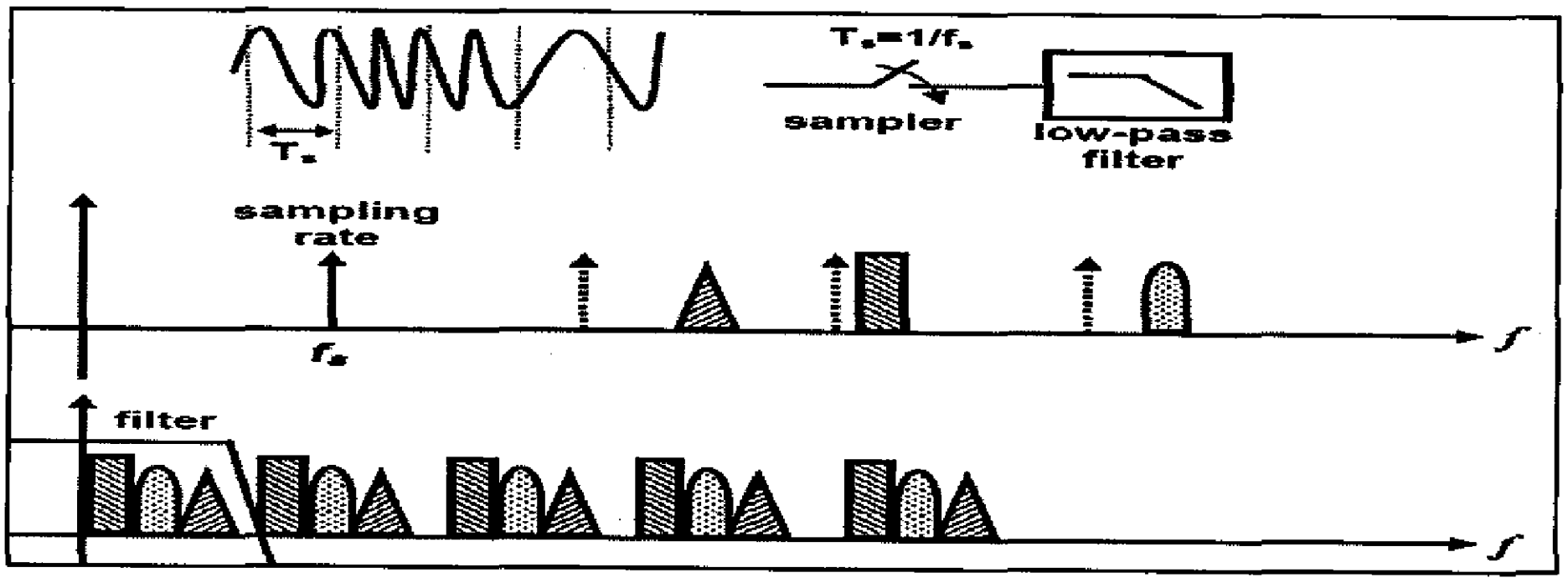

Figure 2.18: Frequency Domain Representation of Multi-Band Sub-Sampling [19]

2.4.6. System-level Approach for Multiple Applications: Sharing Same Band

All the above-mentioned concurrent architectures tend to select applications that occupy non-overlapping frequency bands. Such selection automatically avoids any degradation in system performance due to intra-band interference from the bands of interest, themselves. Nevertheless, it is possible to efficiently support multiple applications, sharing same frequency band, by employing a system level solution to the afore-mentioned problem. As a design example of the approach Kim et. al., [22] proposes a concurrent radio-frequency (RF) receiver to support the Bluetooth and the WLAN (IEEE 802.11b) signals. As it is clear by now, a radio capable of concurrent handling of these two standards will provide access to two different applications at the same time. For instance, a user in a "hotspot" while communicating with peers using Bluetooth in a piconet can, simultaneously, surf the internet and download files using Wi-Fi in an airport lounge, a university campus or in an office. Yet, a major hurdle in their concurrent reception is the fact that both the standards share the same 2.4-GHz ISM frequency band. A Bluetooth signal hops in the 2.4-GHz ISM band including the Wi-Fi channel. As mentioned earlier, such band-sharing may result in degradation of the quality of service (QoS) for both the WLAN and the Bluetooth applications in a concurrent scenario.

Adaptive frequency hopping (AFH) is proposed as a system level solution to the problem. The scheme allows coexistence of the Bluetooth and the WLAN standards without any degradation in the bit error rate (BER). This is made possible because the AFH frees Bluetooth and Wi-Fi of any interferers. Herein, receiver controls the hopping sequence in Bluetooth and prevents it from occupying the Wi-Fi channel. The scheme is figuratively depicted in figure 2.19

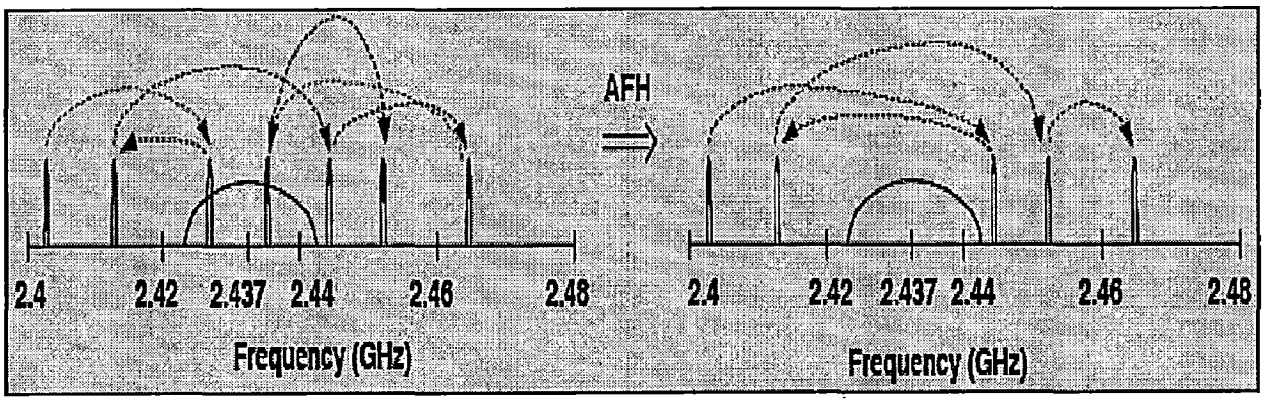

Figure 2.19: Frequency Hopping Sequence Controlled by AFH [23]
(WLAN channel occupies 22 MHz bandwidth around 2.437-GHz)

Whenever the Bluetooth receiver detects a WLAN signal, it requests its transmitter not to hop in the detected WLAN's 22-MHz wide channel so as to avoid interference. This implies that once AFH is employed, the Wi-Fi 22-MHz is free of Bluetooth signals and vice-versa. Hence, concurrent reception is achieved without degrading QOS. It is clear that the scheme will require some form of communication between the receiver and the transmitter. This is mitigated in the present work as it implements both the transmitter and the receiver on the same chip and utilizes digital circuitry for AFH implementation. As far as the receiver architecture is concerned it is similar to the second method of parallel receiver paths with a wide-band front-end. It employs a single RF front-end LNA, followed by two independent paths that work at the same time. As shown in figure 2.20, a low-IF path and a two-step down-conversion path are utilized for Bluetooth and the WLAN, respectively. Since the two standards occupy the same frequency band, therefore, just a single LNA is required to amplify the entire band without differentiating between the two standards.

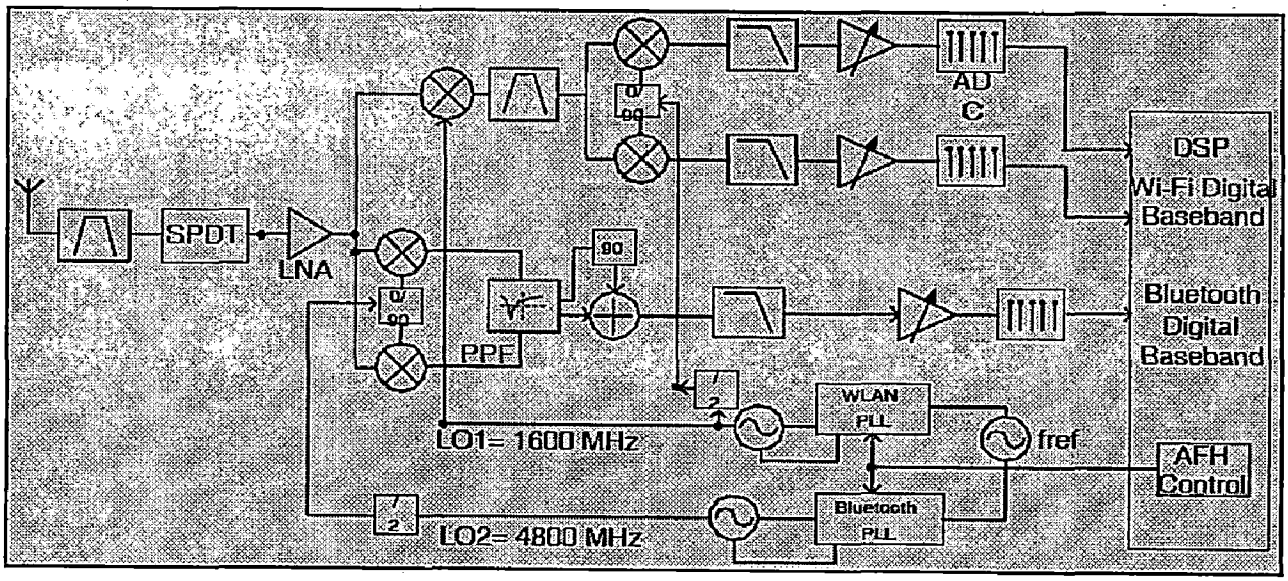

Figure 2.20: A 2.4 GHz Concurrent RF Receiver Architecture for Bluetooth and WLAN [22]

2.5 Implemented Transmitter Architecture

The architecture in Figure 2.21 is the implemented dual-band wireless transmitter. In this we concentrate only on the RF front-end sections i.e. dual-band mixing and amplification in addition with transmission via antenna. Baseband processing describes modulation scheme in WLAN, *i.e.*, Orthogonal Frequency-Division Multiplexing (OFDM). For designing RF-front end of the transmitter, we assume that maximum analog signal BW of 30MHz, which is obtained after digital-to-analog conversion from aforementioned modulation scheme. In order to get RF signal, the baseband (BB) signal has been up-converted with the help of mixers.

The dual band mixer up-converted the signal received from BB to be transmitted in the desired band of 2.4 and 5.2 GHz with the help of two different LOs. To combine two different bands contents dual-band power combiner is used, which combines the parallel components of the architecture, *i.e.*, two different band contents.

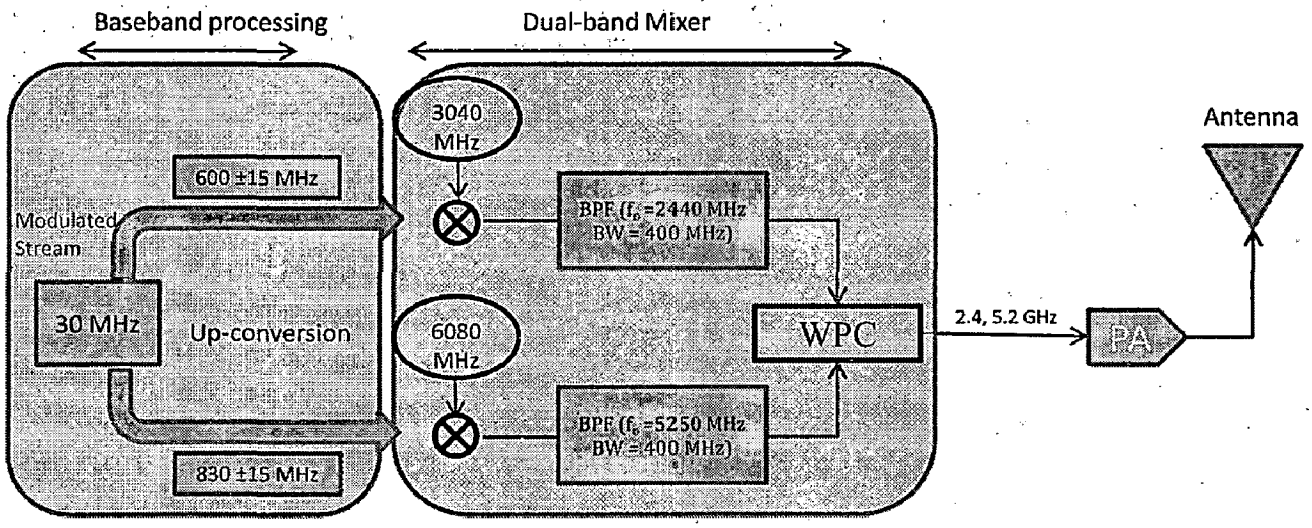

Figure 2.21: Implemented Concurrent Dual Band Transmitter Architecture

2.6 Implemented Receiver Architecture

The proposed architecture acts as Dual-band concurrent receiver's RF front-end. The received spectra from antenna get amplified by dual band LNA. Thus resultant signal is having both frequency contents i.e. 2.4 GHz and 5.2 GHz. This is further separated by power divider into two streams that are individually filtered with the help of band-pass filters. First one of the parallel components is down-converted with the help of mixer and LO (3040MHz). Mixed content has sum and difference of (LO±2.4GHz) two input frequency to mixer, which gives 600 MHz and 5480 MHz that is further filtered with the help of LPF. Similarly on the other hand we have 830 MHz and 11330 MHz that is also filtered with the help of another LPF. The individual building blocks are further discussed in details. This architecture and frequency planning for Up/Down conversion is basically selected because of simplicity in design the system from the available facility in laboratory.

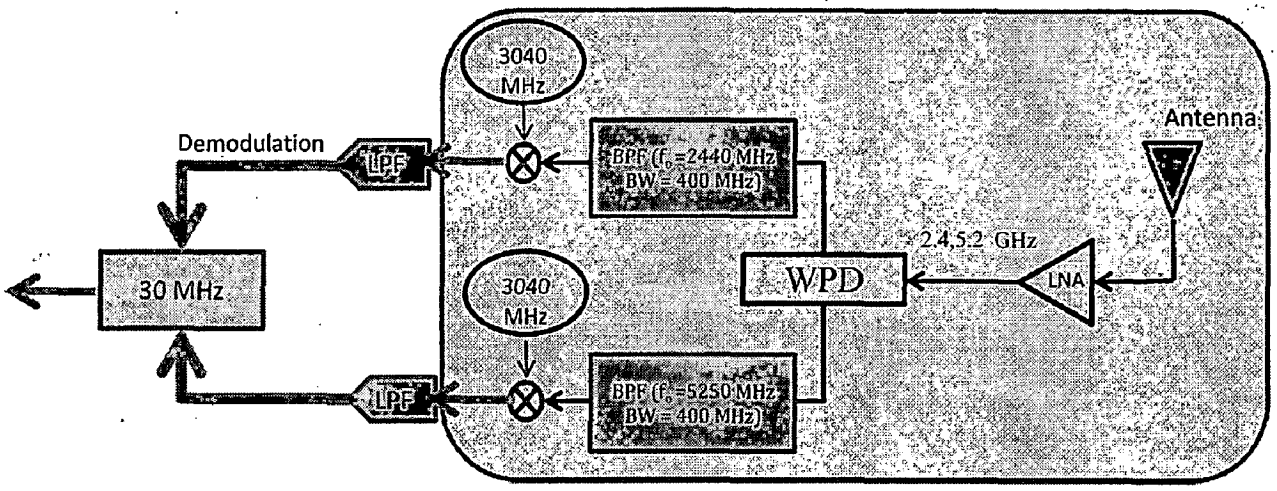

Figure 2.23: implemented Concurrent Dual Band Receiver Architecture

2.7 Conclusion

In this chapter we studied the basic design consideration of transmitter and receiver architectures separately. Standard receiver architecture (super-heterodyne, image reject, Zero IF or homodyne and low-IF) have been discussed in details and finally compare all architectures in form of table, which shows the relative merit and demerit of each architecture. Similarly for transmitter architecture (super-heterodyne, direct-up, two-step) also discussed, how concurrency achieved in such architectures. After the knowledge of all pros and cons we proposed the architecture for dual band transmitter and receiver.

Design and Implementation of Passive of Dual-band Circuit Elements

3.1. Introduction

Filters, power combiner and antenna are the basic building blocks of transceiver. They can active or passive. The designs presented in this chapter are passive. As per requirement of the implemented transmitter / receiver, filters can be single band but Power combiner and antenna must have dual band support to the system. In this chapter design methodology of filter, power combiner and antenna discussed.

3.2 Filters Design

Filters are very important components of telecommunication system. They are required to perform different functions like impedance matching or signal selection. Although similarities exist between impedance matching circuits and filter circuits just by looking at their schematics, there are distinct differences between these functions.

Filters for Impedance Matching: In RF systems the optimum power transfer is one of the important design considerations. The power transfer needs to be maximized from one system block to another. This is achieved by means of matching networks. Matching networks are some type of electrical interconnections that are required between each building block. They are realized using strictly reactive and lossless components in order to achieve power conservation and to achieve usable gain from the active device (transistors) at microwave frequencies.

Filters for Signal Selection: The functions of filters in wireless circuits are mostly to reject the unwanted signal frequencies, while permitting a good transmission of the wanted ones. Depending on the circuit requirements, these filters can be designed as low-pass, high-pass, band-pass, or band-stop.

For the optimal operation of transceivers the isolation of both the transmitter and receiver have to be very large (e.g. 120 dB).The isolation between both the chains can be done using a duplexer (filter consisting of two band pass circuits), or a switch. Switches are mechanical, electrical, or electronic devices that open or close circuits, complete or break an electrical path, or select paths or circuits. The losses of a switch are usually less than those of a duplexer.

Filters in a transmitter chain are needed to meet the output noise requirements of the transmitter, since in some cases the transmitter noises can leak into the receiver via the duplexer and destroy the receiver sensitivity. The technology of choice for filters preceding the power amplifier (PA) is SAW (Surface Acoustic Wave). For output duplexers, ceramic Band pass filters are also used. Ceramic filters have lower insertion loss and thus have less effect on the transmitter efficiency.

RF Preselect Filters: The purpose of RF preselect filters in receivers is to select the desired frequency band to be received, and to eliminate any undesired signal. These filters are typically realized in the form of a diplexer or duplexer. Duplexer connects the antenna to the transmitter (TX) and receiver (RX) and provides isolation between the RX and TX chains. These filters protect the receiver from saturation by interfering signals at the antenna and determine the receiver selectivity. Without the duplexer, the strong transmitted signal would leak into the receiver section and saturate the low-noise-amplifier, causing the receiver to lose sensitivity to the weak receive signal. Diplexers connect the antenna to a dual band transceiver and allow one frequency band to pass between the antenna and transceiver (e.g., connection of a GSM-800 and PCS-1900dual band transceiver with antenna).Ceramic coupled-resonator filters are commonly used for front-end receiver filters or duplexers. Lower-cost discrete LC filters are also used, especially in half-duplex transceivers where strong interference from the system's own transmitter is not an issue, and thus lower out of band rejection is acceptable.

Image Reject Filters: Image-reject filters placed after the LNA are used to protect the RF mixer from out-of band interferer signals as well as to reject the undesired signals, generated by the RF mixer and other components. Without image rejection filtering, any signal present at the image frequency will be down converted to the same intermediate frequency (IF) and will corrupt the desired signal.

The bandwidth of IR filters, centered at the carrier frequency (fc), must be sufficiently wide to pass the modulation sidebands in the desired channel without distortion. The image frequency has to be suppressed by at least 10 dB in order to meet the system noise figure (NF). To meet the system requirements, RF receivers generally need about 65 dB of image rejection. SAW (Surface Acoustic Wave) filters are typically used to provide image rejection. Low-cost LC filters can also be used at the expense of lower rejection levels.

Intermediate Frequency (IF) Filters: Intermediate frequency filters (IF Filter) are designed to receive the entire RF pass-band and to reject spurious frequencies and image frequencies in particular. These IF filters narrow in and select the desired channel from the entire pass band; they provide thereby additional selectivity to the receiver. These filters help to prevent out-of-channel noise and help to minimize the loss, thus improving the sensitivity of receivers. SAW filters are the components of choice for most IF filter applications. They provide the best out-of-band rejection at reasonable size and cost. Crystal and LC filters can also be used at the expense of lower performance.

Base Band Channel Filters: In baseband sections of wireless transceivers, filters for signal selection are required, e.g. anti- aliasing filters located before the A/D converter (C Filter in fig) and reconstruction filters after the D/A converters. These kinds of filters are generally low pass and remove the unwanted channels appearing at higher baseband frequencies, after down conversion. These filters are typically realized on-chip using silicon or GaAs-technologies, for example. As can be seen throughout this section, many filters are required in wireless transceiver circuits, and particularly in the analog RF section. Since many of these filters are discrete or surface mounted, integrating them will lead to a substantial reduction in board size as well as in weight. For a successful integration however, efficient design and analysis methods are required.

3.2.1 Fundamentals of Filter Design using Insertion Loss Method

Generally a low pass filter prototype is in general defined as the low pass filter, whose element values are normalized to make the source resistance or conductance equal to one,denoted by $g_0 = 1$, and the cutoff angular frequency to be unity, denoted by $\Omega_c = 1$(rad/s).

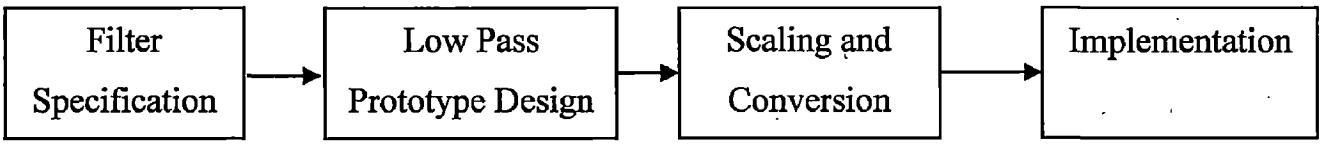

Figure 3.1: The Process of Filter Design using Insertion Loss Method [23]

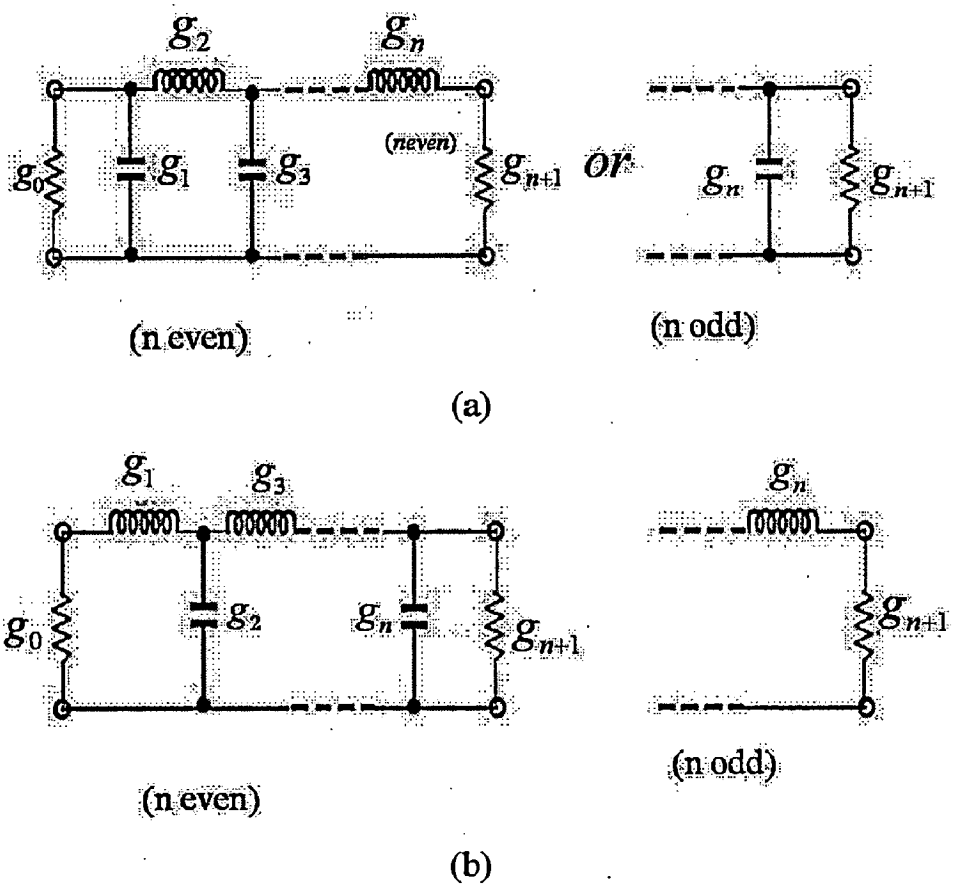

Figure 3.2: Low Pass Prototype Filters with Ladder Network Structure and its Dual [24]

(A) Butterworth Low Pass Prototype Filter

For Butter worth response

$$L_A(\omega^1) = 10\log_{10}(1+\left(\frac{\omega^1}{\omega_1^1}\right)^{2n}) \text{ dB} \tag{3.1}$$

The 'g' notation used in figure signifies roots of an nth order transfer function that governs its characteristics. These represent the normalized values of filter elements with a cut off frequency of Ω_c= 1(rad/s).Element values for normalized Butterworth low pass prototype filter are

$$g_0 = 1$$

$$g_k = 2*\sin\left(\frac{(2k-1)\pi}{2n}\right), \quad k = 1, 2 \ldots .n \tag{3.2}$$

$$g_{n+1} = 1$$

To determine the order of a Butterworth low pass prototype filter, the specification that usually given is the stop band attenuation(L_{As} in dB)at $\Omega = \Omega_s$ for $\Omega_s > 1$.

$$n \geq \frac{\log(10^{\frac{L_{As}}{10}}-1)}{2\log\Omega_s} \tag{3.3}$$

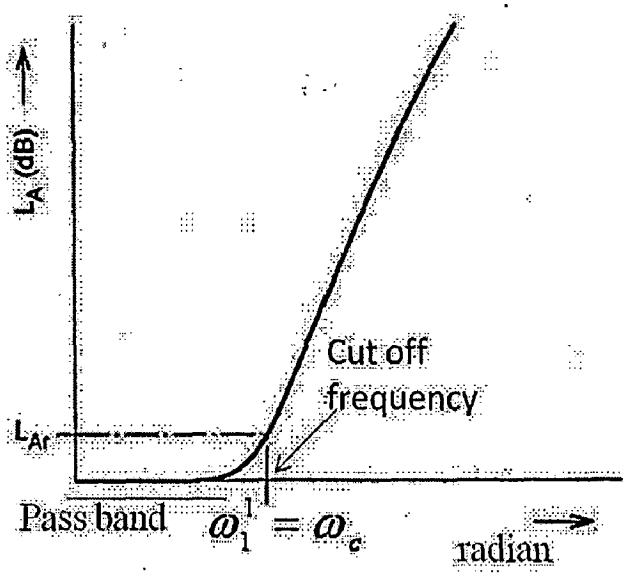

Figure 3.3: Butterworth (Maximally flat) Response [24]

(B) Chebyshev Low Pass Prototype Filters

For Chebyshev low pass prototype filters having a transfer function given in

$$\text{ripple constant} = \varepsilon = \sqrt{10^{\frac{L_{Ar}}{10}} - 1} \tag{3.4}$$

Where L_{Ar} is the pass band ripple in dB.

The element values of the two port network of may be computed using the following formulas:

$g_0 = 1.0$

$$g_1 = \frac{2}{\gamma}\sin\left(\frac{\pi}{2n}\right) \tag{3.5}$$

$$g_i = \frac{1}{g_{i-1}} \frac{4 \sin\left(\frac{(2i-1)\pi}{2n}\right) * \sin\left(\frac{(2i-3)\pi}{2n}\right)}{\gamma^2 + \sin^2\left(\frac{(i-1)\pi}{n}\right)} \qquad \text{for } i = 2, 3 \ldots n \tag{3.6}$$

$g_{n+1} = 1.0$ For n odd

$\coth^2\left(\frac{\beta}{4}\right)$ For n even (3.7)

$$\beta = \ln\left[\coth\left(\frac{L_{Ar}}{17.37}\right)\right] \tag{3.8}$$

$$\gamma = \sinh\left(\frac{\beta}{2n}\right) \tag{3.9}$$

for the required pass band ripple ,minimum stop band attenuation the order of the chebyshev lowpass filter is found by

$$n \geq \frac{\cosh^{-1}\sqrt{\frac{10^{0.1L_{As}} - 1}{10^{0.1L_{Ar}} - 1}}}{\cosh^{-1}\Omega_s} \tag{3.10}$$

Where L_{As} is the stop band attenuation at Ω_s

For 'n' odd, we have equal source and load impedances, but for 'n' even we have unequal source and load impedances. If design leads to 'n'=even and we need equal source and load impedances increase either 'n' by one or put a impedance matching network at the load end.

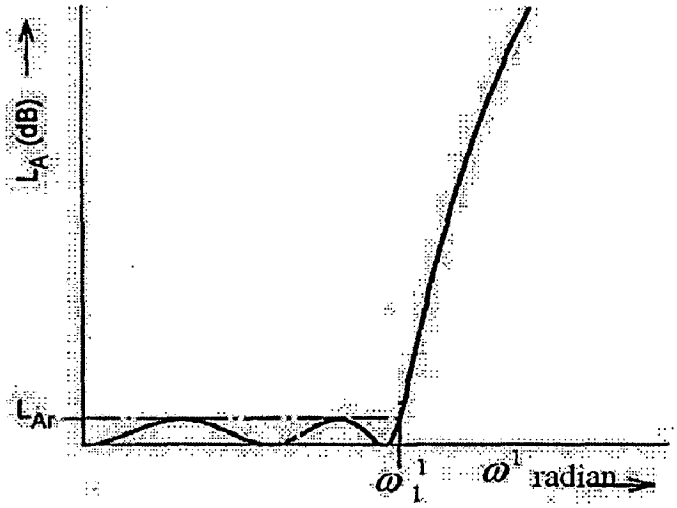

Figure 3.4: Chebyshev Attenuation Characteristics [24]

L_{Ar} Is the maximum attenuation (dB) in the pass-band

ω_1^1 = Equal ripple band edge

For $\omega^1 < \omega_1^1$

$$L_A(\omega^1) = 10\log_{10}(1 + \epsilon\cos^2(n\cos^{-1}(\frac{\omega^1}{\omega_1^1})) \quad (3.11)$$

and$\omega^1 > \omega_1^1$

$$L_A(\omega^1) = 10\log_{10}(1 + \epsilon\cosh^2(n\cos^{-1}(\frac{\omega^1}{\omega_1^1})) \quad (3.12)$$

For both maximally flat as well as Chebyshev type response, "n" is the order or number of reactive elements present in the circuit.

For a low-pass Chebyshev response, if n=even, there are $(\frac{n}{2})$frequencies where L_A=0 while if n= odd there will be $(\frac{n+1}{2})$where L_A= 0

(C) Impedance and Frequency Scaling [23]

Impedance scaling

In the prototype design, the source and load resistances are unity .A source resistance of R_0 can be obtained by multiplying the impedances of the prototype design byR_0. Let prime denotes impedance scaled quantities. New filter component values are given by

$$L^1=R_0L \tag{3.13}$$

$$C^1=\frac{c}{R_0} \tag{3.14}$$

$$R_s^1= R_0 \tag{3.15}$$

$$R_L^1= R_0R_L \tag{3.16}$$

L, C and R_L are the component values for the original prototype filter.

Frequency scaling

For changing the cutoff frequency of a low pass prototype from unity to Ω_c requires the scaling of frequency by the factor of $\frac{1}{\omega_c}$ which is accomplished by replacing ω by $\frac{\omega}{\omega_c}$. Thus new elements values are obtained by applying the substitution of $\omega \longrightarrow \frac{\omega}{\omega_c}$to the series reactances and shunt susceptance of the prototype filter.

Thus

$$jX_k=j\frac{\omega}{\omega_c}L_k=j\omega L_k^1 \tag{3.17}$$

$$jB_k=j\frac{\omega}{\omega_c}C_k=j\omega C_k^1 \tag{3.18}$$

When both impedance and frequency scaling is done then the new element values then obtained are

$$L_k^1=\frac{R_0L_k}{\omega_c} \tag{3.19}$$

$$C_k^1=\frac{C_k}{R_0\omega_c} \tag{3.20}$$

(D) Filter Transformations

Low pass to high pass transformation

The frequency substitution where $\omega \longrightarrow \frac{-\omega_c}{\omega}$ can be used to convert a low pass response to a high pass response. So the basic element of the low pass elements like inductor is converted to capacitor and capacitor is converted into inductor in high pass filter transformation.

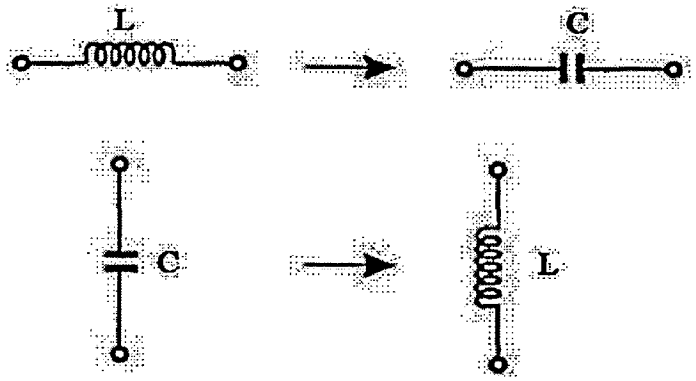

Figure 3.5: Low pass to High pass Transformation [24]

Low pass to band pass transformation

The frequency substitution where $\omega \longrightarrow \frac{\omega_0}{\omega_2 - \omega_1}\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right) = \frac{1}{\Delta}\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)$

Where Δ is fractional bandwidth of the pass band ω_1 and ω_2 denote the edges of the pass band and the centre frequency $\omega_0 = \sqrt{\omega_1 * \omega_2}$.

In this transformation series inductor of low pass filter is converted to series LC circuit and shunt capacitor of low pass filter is converted to parallel LC circuit

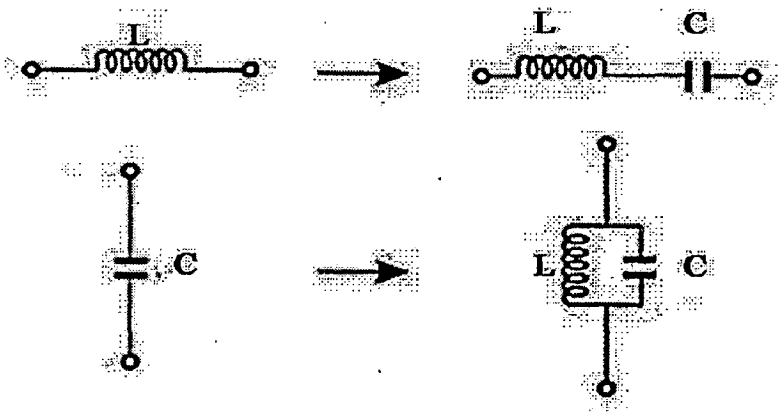

Figure 3.6: Low Pass to Band Pass Transformation [24]

3.2.2 Coupled line Filter Design

When two unshielded transmission lines are close together, power can be coupled between the lines due to the interaction of the electromagnetic fields of each line. Such lines are referred to as coupled transmission lines .Coupled transmission lines are usually assumed to operate in TEM mode, which is rigorously valid for stripline structures and approximately valid for microstrip structures. Coupled line structures can be used to implement directional couplers, hybrids, and filters.

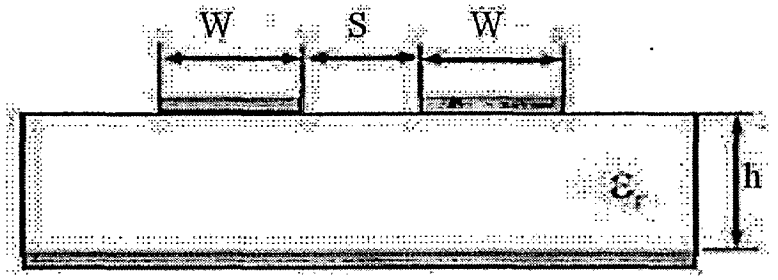

Figure 3.7: Cross-section view of Coupled Microstrip Lines [11]

(A) Coupled Line Theory

The coupled lines or any other three wire line, can be represented by the structure shown in fig.. If we assume TEM mode of propagation, then the electrical characteristics of the coupled lines can be completely determined from the effective capacitances between the lines and the velocity of propagation on the line.

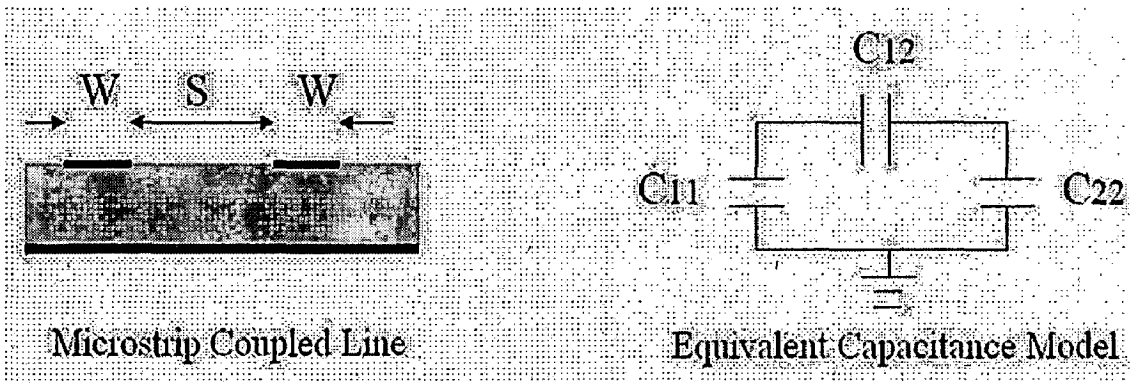

Figure 3.8: Microstrip Coupled Lines and its Equivalent Capacitor Model

(B) Types of Excitations for the Coupled Line

Even mode of excitation

Odd mode of excitation

For the even mode of excitation the currents in the strip conductors are equal in amplitude and in the same direction, and the odd mode, where the currents in the strip conductors are equal in amplitude but in opposite direction.

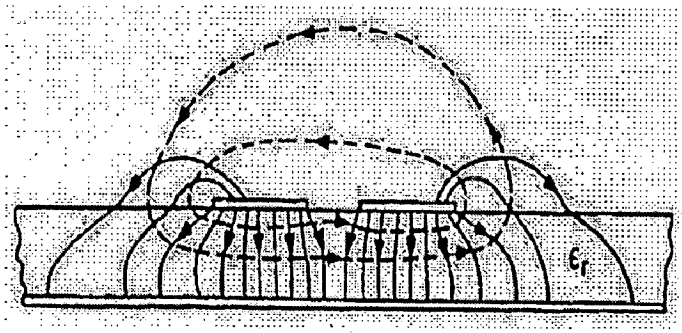

Figure 3.9: E and M Field Lines of a Coupled Line (Even Mode)

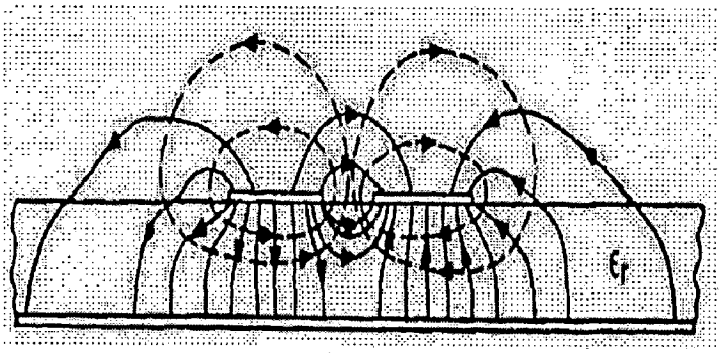

Figure 3.10: E and M Field Lines of a Coupled Line (Odd Mode)

For the even mode, the electric field has even symmetry about the center line, and no current flows between the two strip conductors. This leads to the equivalent circuit shown, whereC_{12} is effectively open circuited. Then the resulting capacitance of either line to ground for the even mode is $C_e = C_{11} = C_{22}$. Characteristic impedance for the even mode is $Z_{0e} = \frac{1}{V_p C_e}$ where V_p is the phase velocity of propagation on the line.

For the odd mode, the electric field lines have an odd symmetry about the centre line, and a voltage null exists between the two strip conductors. We can imagine this as a ground plane through the middle ofC_{12}. In this case, the effective capacitance between strip conductor and ground is

$$C_0 = C_{11} + 2C_{12} = C_{22} + 2C_{12} \tag{3.21}$$

Characteristic impedance for the odd mode is $Z_{0o} = \frac{1}{V_p C_0}$, Where V_p is the phase velocity of propagation on the line. An arbitrary excitation of a coupled line can always be treated as a superposition of approximate amplitudes of even and odd modes.

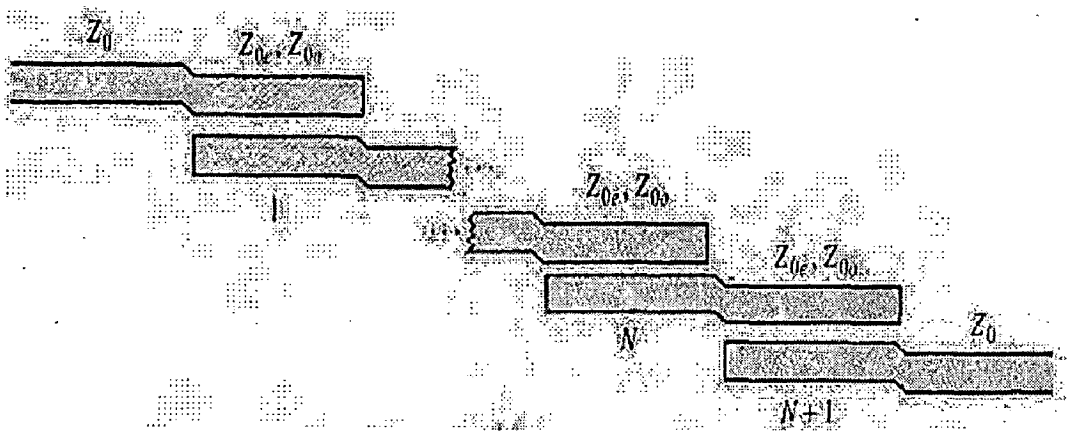

Figure 3.11: Coupled line Filter Structure

We design these filter with the help of coupled line with small modification i.e. coupled line Figure 3.11 are appear in zigzag manner. By this we can possibly reduce the length of the filter. The design equations have been taken from [23] to design the filter given below.

$$Z_0 J_1 = \sqrt{\frac{\nabla\pi}{2g_1}} \tag{3.22}$$

$$Z_0 J_n = \frac{\nabla\pi}{2\sqrt{g_{n-1}g_n}} \tag{3.23}$$

$$Z_0 J_{N+1} = \sqrt{\frac{\nabla\pi}{2g_N g_{N+1}}} \tag{3.24}$$

$$Z_{0e} = Z_0\{1 + JZ_0 + (JZ_0)^2\} \quad (3.25)$$

$$Z_{0o} = Z_0\{1 - JZ_0 + (JZ_0)^2\} \quad (3.26)$$

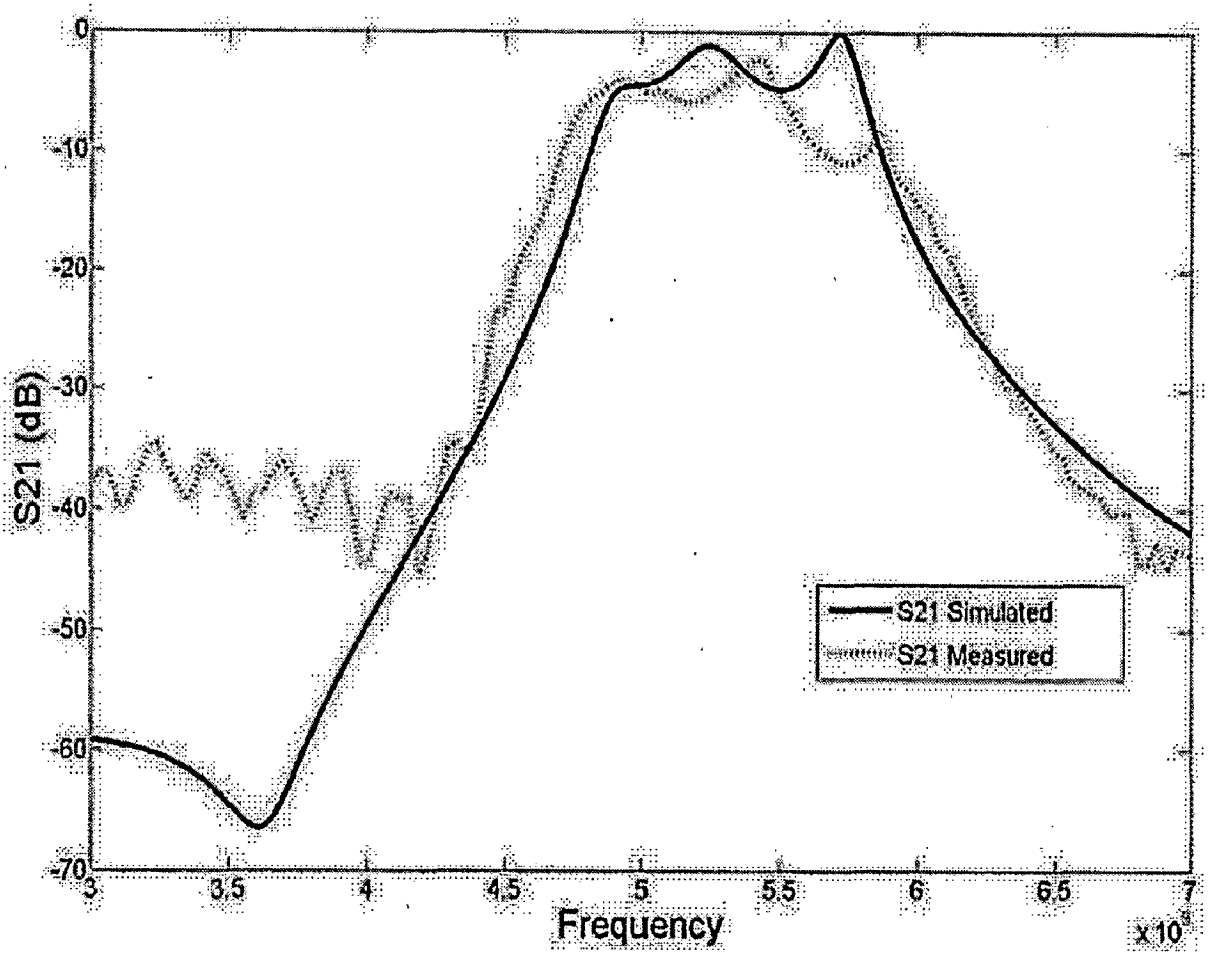

Figure 3.12: Implemented Band-pass Filter Response 5250 MHz

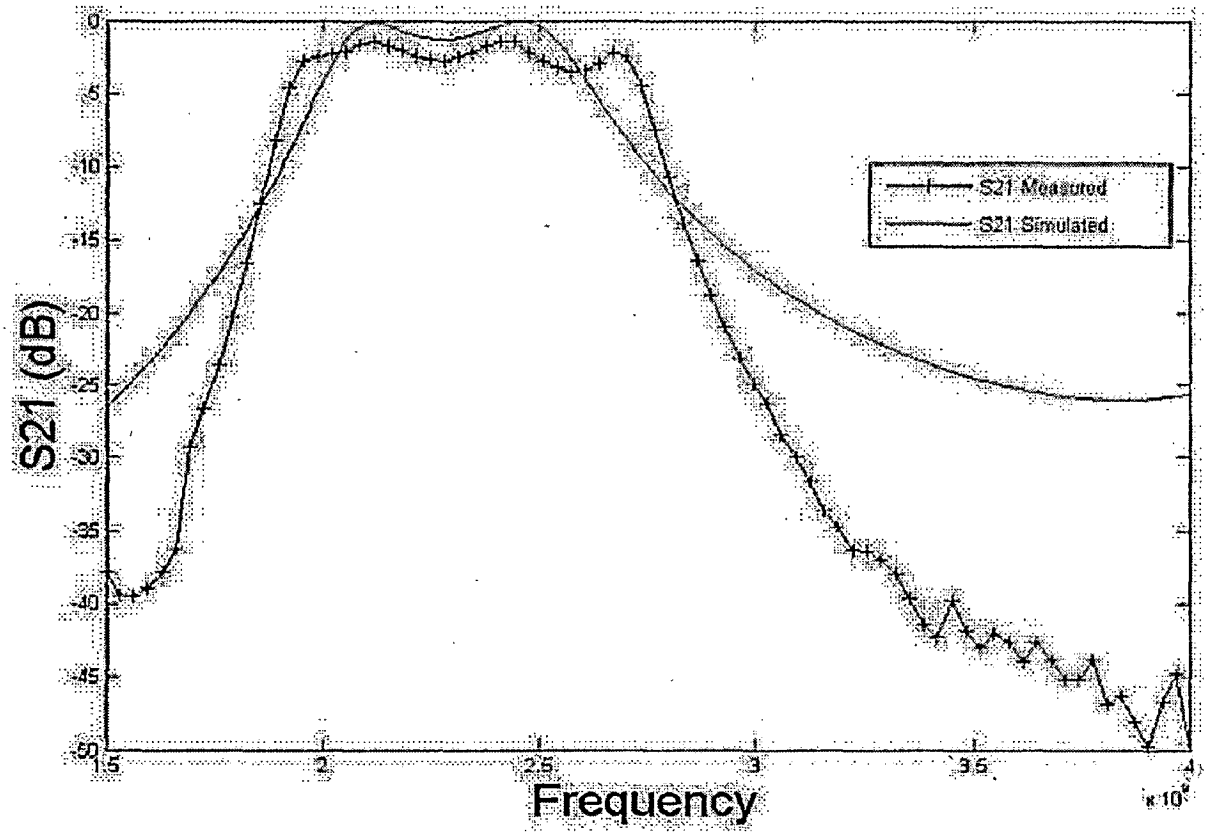

Figure 3.13: Implemented Band-pass Filter Response 2440 MHz

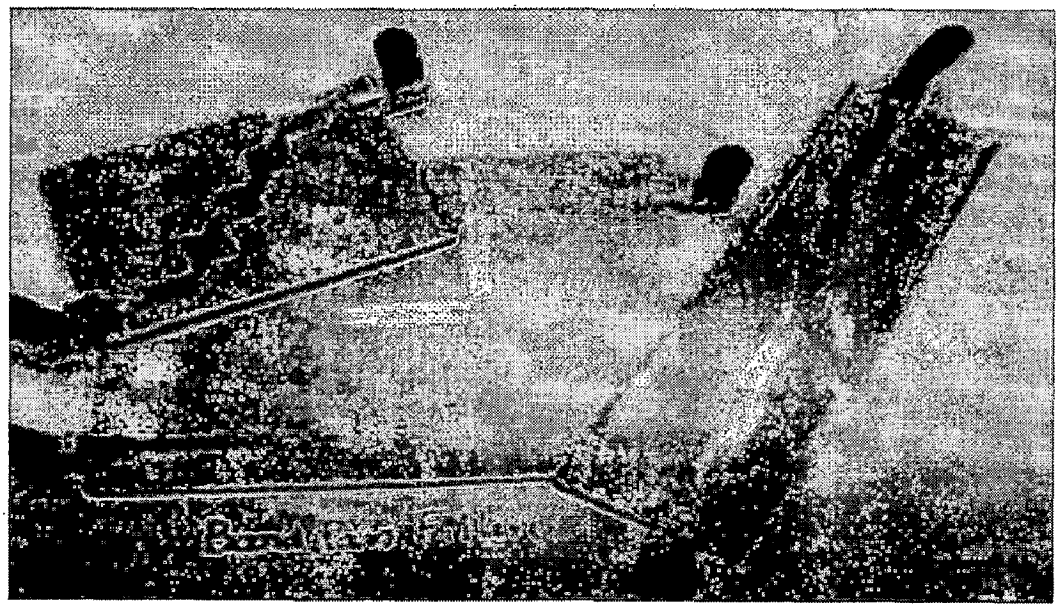

Figure 3.14: Implemented Band-pass Filter (2.4 GHz and 5.25 GHz)

3.3 Dual band Power Combiner Design

This power divider is consists π-section which is replacing each (λ/4) transmission line of the conventional Wilkinson power divider. This π-section has been designed such that the power divider operates at two arbitrary frequencies. The objective is to obtain the characteristic impedances of each transmission line section of the equivalent π-section as a function of their electrical lengths at one of the desired operation frequencies [27] .The equivalent π-section consists of two identical open stubs connected by a series transmission line as shown in Figure 3.15

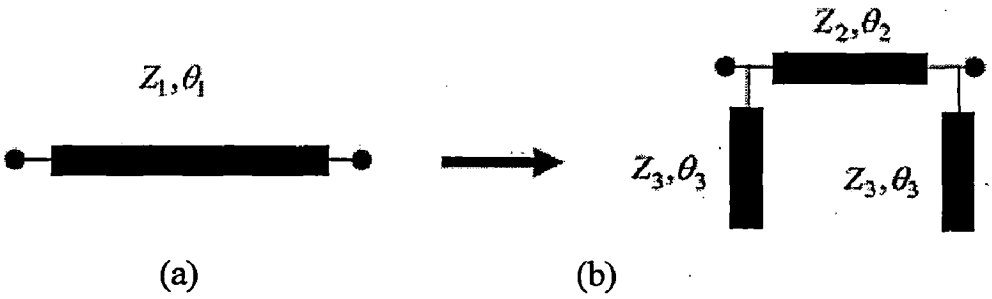

Figure 3.15: (a) Transmission line (b) Equivalent π-section.

The equivalence between the two sections can be seen by using the ABCD matrices of both the sections. The ABCD matrix of Figure3.15 (a) is

$$[T_1] = \begin{bmatrix} \cos\theta_1 & jZ_1\sin\theta_1 \\ jY_1\sin\theta_1 & \cos\theta_1 \end{bmatrix} \quad (3.27)$$

When $l = \lambda/4$ then $\theta_1 = \frac{\pi}{2}$

$$[T_1] = \begin{bmatrix} 0 & jZ_1 \\ jY_1 & 0 \end{bmatrix} \quad (3.28)$$

Where $Z_1 = \sqrt{2}\, Z_0$ as in the conventional Wilkinson power divider. The ABCD matrix of the π-section of Figure3.15 (b) is calculated as

$$[T_3] = \begin{bmatrix} 1 & 0 \\ jY_3\tan\theta_3 & 1 \end{bmatrix} \quad (3.29)$$

$$[T_2] = \begin{bmatrix} \cos\theta_2 & jZ_2\sin\theta_2 \\ jY_2\sin\theta_2 & \cos\theta_2 \end{bmatrix} \tag{3.30}$$

Where T_2 is the ABCD matrix of the series transmission line of Figure3.150(b) and T_3 is the ABCD matrix of the shunt stubs of Figure3.15 (b) and θ_2 and θ_3 are the electrical lengths of the transmission lines with characteristic impedances Z_2 and Z_3 as shown in Figure3.15 (b) respectively.

The equivalent ABCD matrix of the π-section $[T_t]$ is then given by

$$[T_t] = [T_3].[T_2].[T_3]$$

$$[T_t] = \begin{bmatrix} 1 & 0 \\ jY_3\tan\theta_3 & 1 \end{bmatrix}\begin{bmatrix} \cos\theta_2 & jZ_2\sin\theta_2 \\ jY_2\sin\theta_2 & \cos\theta_2 \end{bmatrix}\begin{bmatrix} 1 & 0 \\ jY_3\tan\theta_3 & 1 \end{bmatrix}$$

$$[T_t] = \begin{bmatrix} \cos\theta_2 - \frac{Y_3}{Y_2}\sin\theta_2\tan\theta_3 & \frac{j\sin\theta_2}{Y_2} \\ jY_3\tan\theta_3\cos\theta_2 - \frac{Y_3^2\tan\theta_3^2\sin\theta_2}{Y_2} & -\frac{Y_3}{Y_2}\tan\theta_3\sin\theta_2+\cos\theta_2 \end{bmatrix} \tag{3.31}$$

Equating element A from matrices,

$$\cos\theta_2 - \frac{Y_3}{Y_2}\sin\theta_2\tan\theta_3 = 0$$

That gives

$$\tan\theta_3 = \frac{Y_2}{Y_3}\cot\theta_2 \tag{3.32}$$

Equating element B from matrices,

$$\frac{j\sin\theta_2}{Y_2} = jZ_1$$

or

$$Z_1 = \frac{\sin\theta_2}{Y_2} \tag{3.33}$$

For dual band operation Eq. (3.33) must be modified as:

$$Z_2 \sin\theta_{2f1} = \pm Z_1 \tag{3.34a}$$

$$Z_2 \sin\theta_{2f2} = \pm Z_1 \tag{3.34b}$$

Where f_1 and f_2 are the two operating frequencies and θ_{2f1}, θ_{2f2} are the electrical lengths of the transmission line of characteristic impedance Z_2 at frequencies f_1 and f_2 ($f_2 > f_1$) respectively. From (3.34a) and (3.34b)

$$\theta_{2f1} = n\pi - \theta_{2f2} \quad ; \text{where } n = 1,2,3,4 \ldots\ldots \tag{3.35}$$

Since a compact size is always preferred, n = 1 is chosen so that the relation between the electrical lengths and dual operation frequencies f_1 and f_2 is obtained as:

$$\frac{\theta_{2f2}}{\theta_{2f1}} = \frac{f_2}{f_1} = R \tag{3.36}$$

$$\theta_{2f1} = \frac{n\pi}{R+1} \tag{3.37}$$

$$\theta_{2f2} = \frac{Rn\pi}{R+1} \tag{3.38}$$

$$\theta_{3f1} = \frac{m\pi}{R+1} \tag{3.39}$$

$$\theta_{3f2} = \frac{Rm\pi}{R+1} \tag{3.40}$$

The following steps are followed to design the dual band Wilkinson power divider

Step 1: Select the two frequencies for which the operation is desired.

Step 2: Find the value of R using Eq. (3.36).

Step 3: Calculate the values of θ_{2f1} and θ_{3f1} using Eq. (3.37) and Eq. (3.39) or calculate the values of θ_{2f2} and θ_{3f2} using Eq. (3.38) and Eq. (3.40) with m = n = 1.

Step 4: If (3.37) and (3.39) have been used, calculated the values of impedances Z_2 and Z_3 shown below

$$Z_2 = \frac{Z_1}{sin\theta_{2f1}} \tag{3.41}$$

$$Z_3 = Z_2 tan\theta_{2f1} tan\theta_{3f1} \tag{3.42}$$

Table 3.1: Numerical Analysis and Momentum Simulation

Software Used	ADS (Advance design system) Agilent 2008
Technology	Microstrip(ε_r=3.38, h=1.524mm, tanδ =0.0025, t =15μm , σ = 5.8e7)
Application Used	Momentum RF
Design frequency	2.4 GHz and 5.2 GHz
Design parameter	$R = 2.16, \theta_{2f1} = \theta_{3f1} = 0.99208, Z_2 = 84.46\Omega, \quad Z_3 = 197\Omega$

Table 3.2: Dimensions of Microstrip (calculated)

Dimensions in mm	Characteristics impedance of i/p and o/p lines	Characteristics impedances of π-section	
	Z_0=50	Z_2=84	Z_3=197
Width , W (mm)	3.5076	1.3196	0.06291
Length , L(mm)	19.20	12.46	13.16

Since the value W_3 (0.06291mm) is very small easily fabricated at laboratory and this is because of the value of R, Thus we are compromising at the ratio of two frequencies and we design this at 2.0 GHz and 5.2GHz instead of 2.4 and 5.2 GHz. Thus final optimized dimensions

are given below that are realizable at laboratory level. Thus we have R=2.6, θ=0.872 rad, Z_2=92.30Ω, Z3=130.74Ω.

Table 3.3: Dimensions of Microstrip (Used in fabrication)

Dimensions in mm	Characteristics impedance of i/p and o/p lines	Characteristics impedances of π-section	
Width , W (mm)	3.5076	1.046690	0.31493
Length , L(mm)	19.2	11.91	13.6

These dimensions are arbitrarily chosen so as to maximize the performance of coupler better. These are obtained from tuning length and width of transmission lines of π-section.

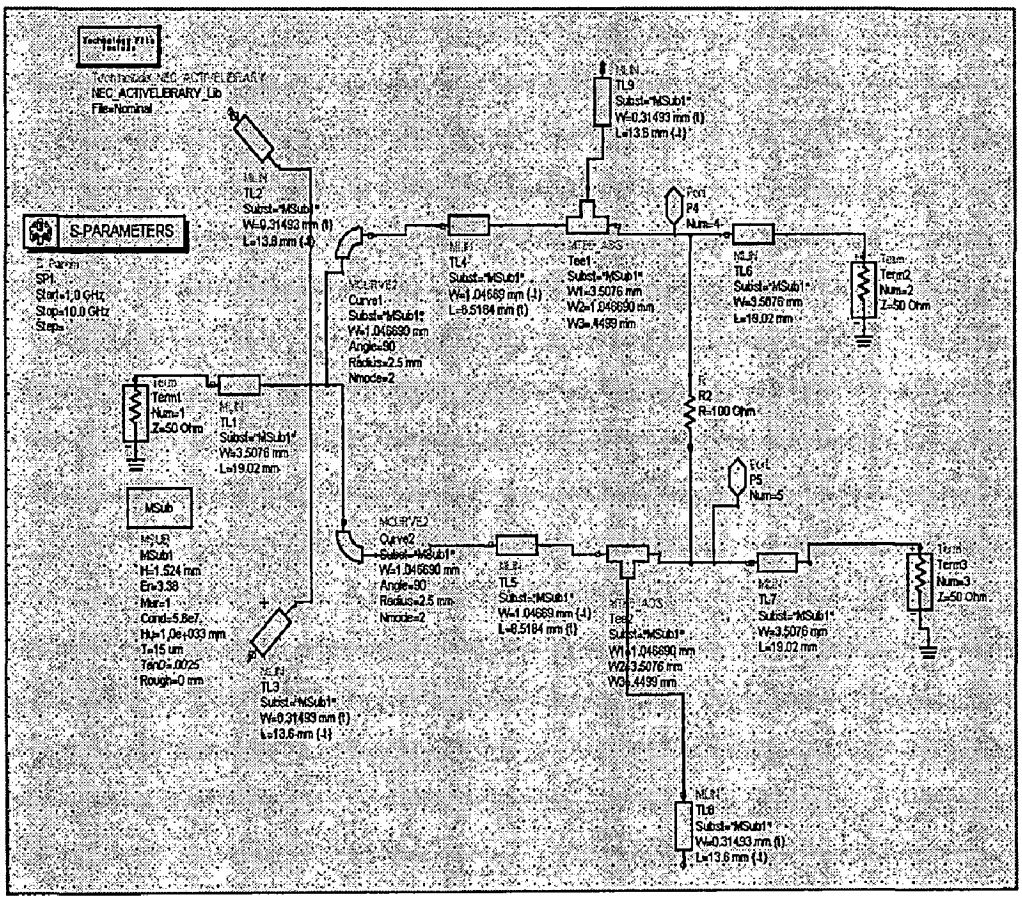

Figure 3.16: Schematic Analysis Concurrent Dual-band Power Combiner

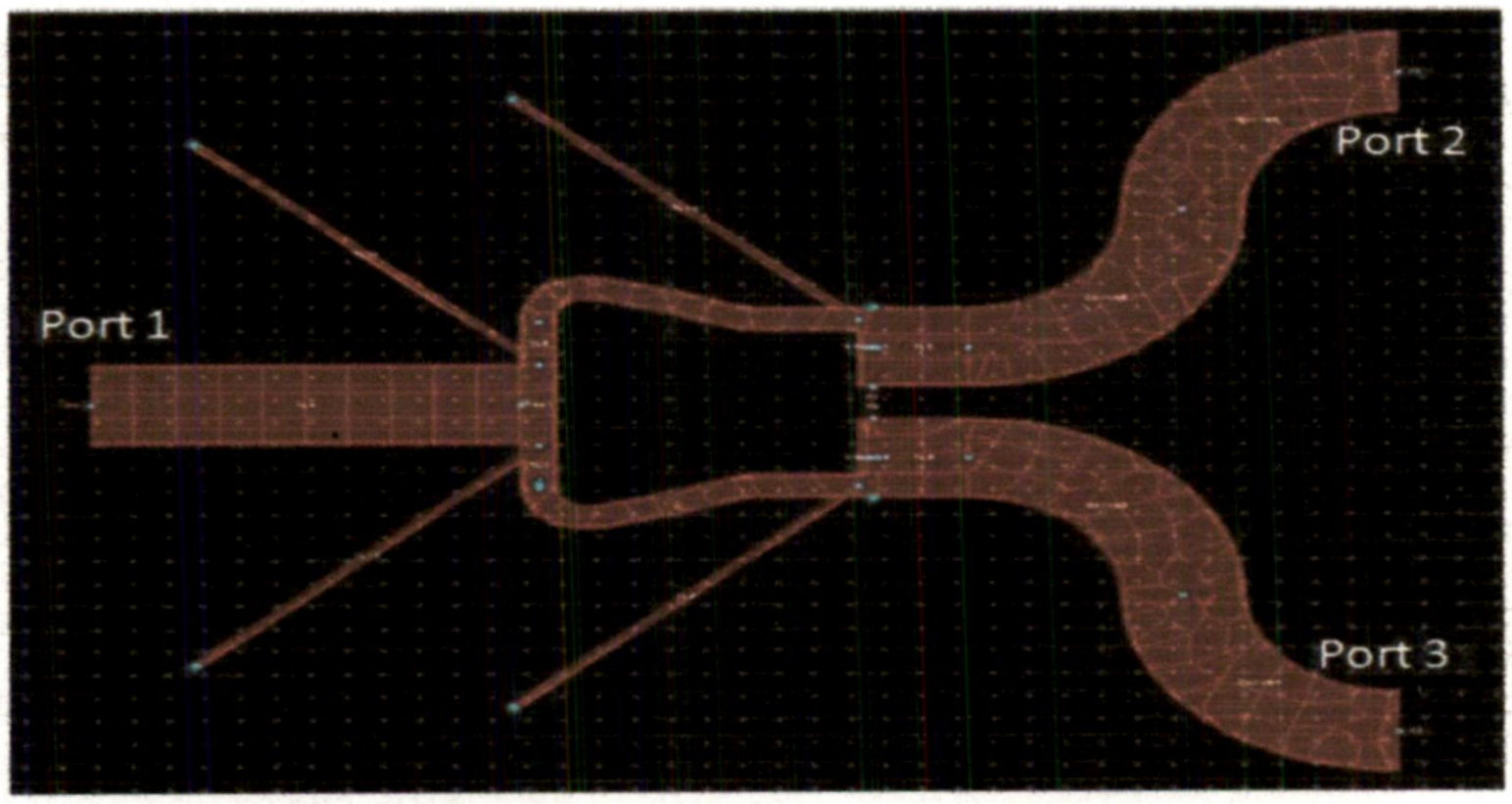

Figure 3.17: Momentum Layout of Concurrent Dual-band Power Combiner

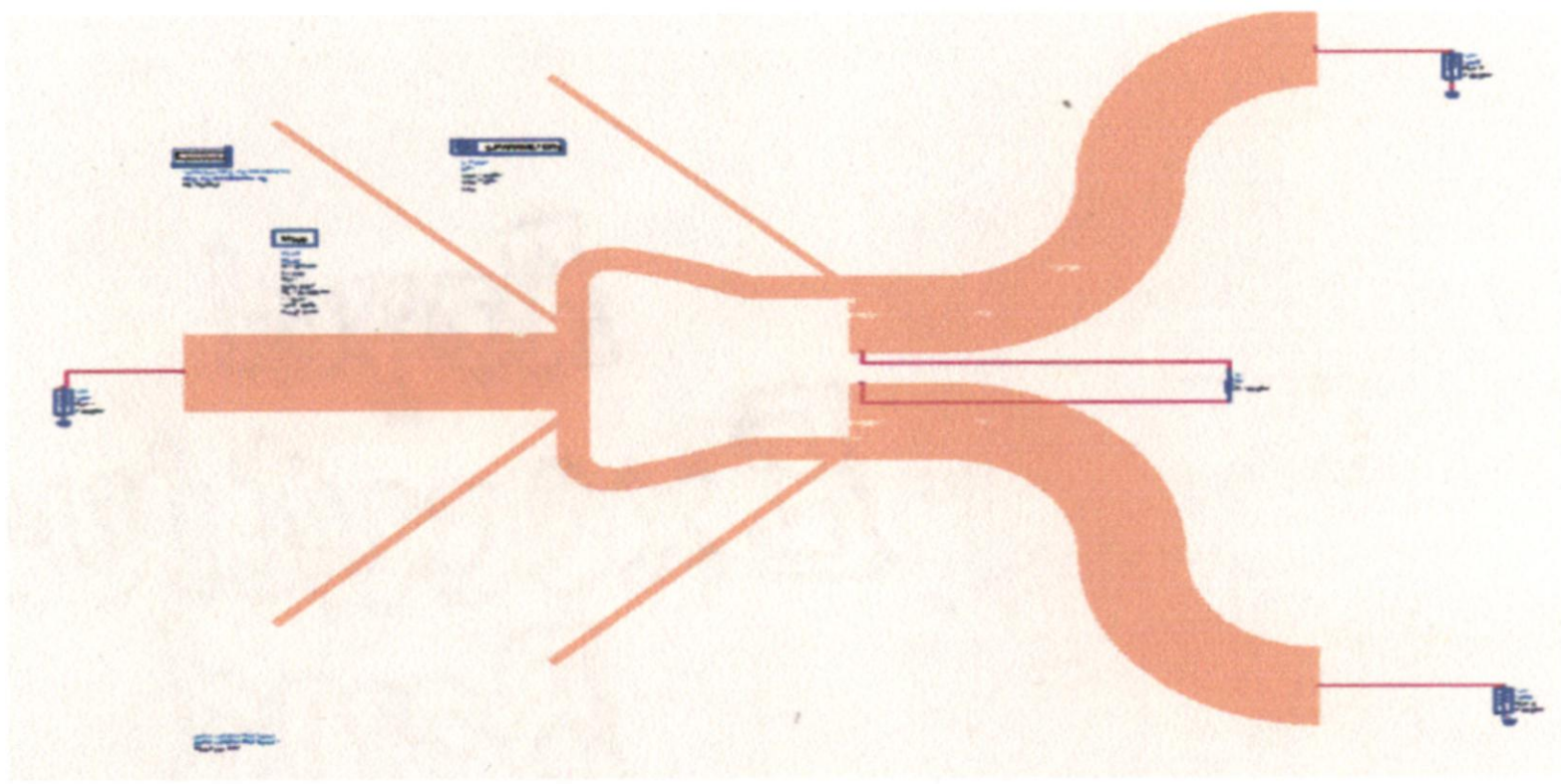

Figure 3.18: Co-simulation of Concurrent Dual-band Power Combiner

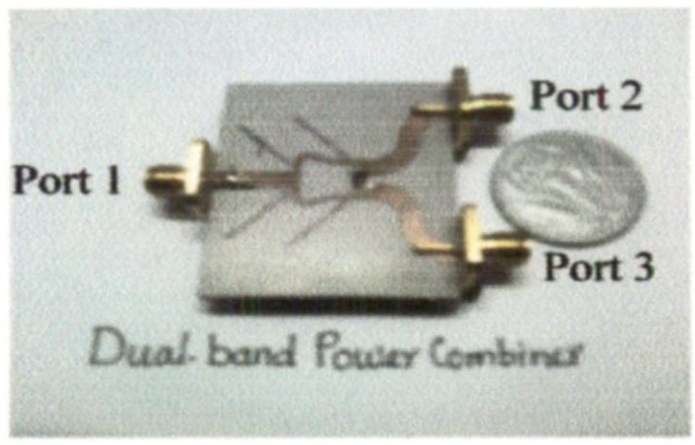

Figure 3.19: Fabricated π-Section Concurrent Dual-band Power Combiner

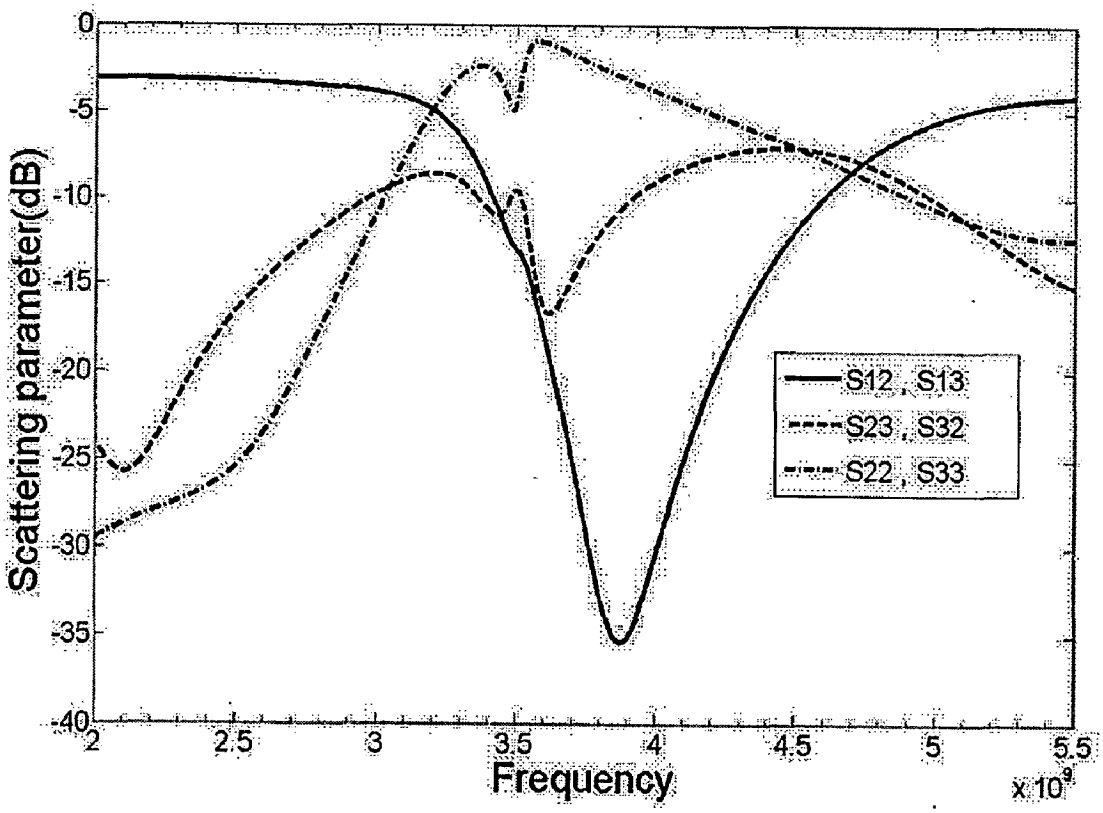

Figure 3.20: Simulated S-parameter of Concurrent Dual-band Power Combiner

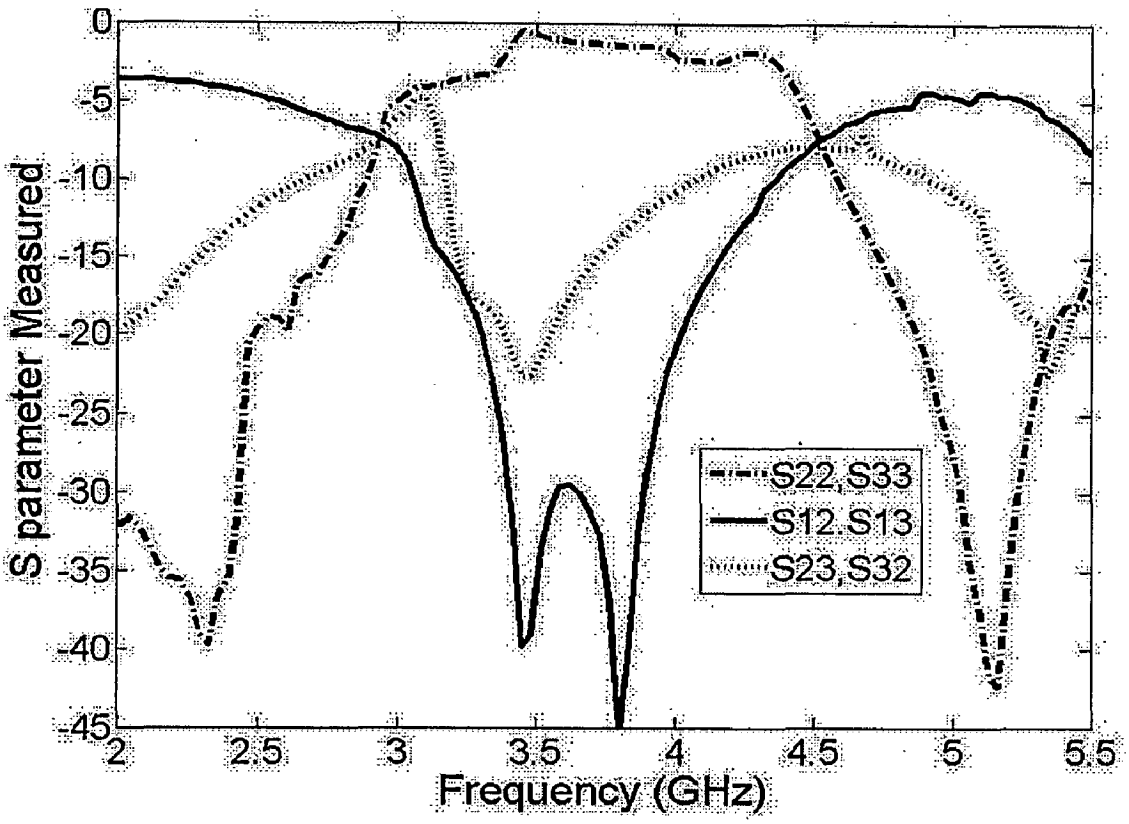

Figure 3.21 Measured S-parameter of Concurrent Dual-band Power Combiner

Table 3.4: Measured S-parameter through hp-8720B Network Analyzer

S-parameter		Frequency(2.4GHz)		Frequency(5.2GHz)	
		Measured	Simulated	Measured	Simulated
Reflection Parameter	S_{11}	-11.50 dB	-14.60 dB	-8.70 dB	-16.6 dB
	S_{22}	-19.60 dB	-21.08 dB	-19.60 dB	-21.08 dB
	S_{33}	-19.30 dB	-21.08 dB	-19.30 dB	-21.08 dB
Transmission Parameter	S_{12}	-3.80dB	-3.29 dB	-4.20dB	-3.25 dB
	S_{13}	-3.75dB	-3.29 dB	-4.50dB	-3.25 dB
Isolation Parameter	S_{23}	-15.10dB	-17.33 dB	-14.7dB	-21.60 dB
	S_{32}	-15.10dB	-17.33 dB	-14.7dB	-21.60 dB

The results differ to some extent in the actual fabrication circuit. The losses may be attributed to fabrication errors. Thus, the π-section WPC has been designed and implemented successfully and the satisfactory results are obtained.

3.4 Dual-band Antenna Design

A monopole antenna is a class of radio antenna consisting of a conductor usually mounted perpendicularly over some type of conductive surface, called a ground plane. The driving signal from the transmitter is applied, or for receiving antennas the output voltage is taken, between the lower end of the monopole and the ground plane. One side of the antenna feed line is attached to the lower end of the monopole, and the other side is attached to the ground plane. Common types of monopole antenna are the whip, rubber ducky, helical, random wire, mast radiator, and ground plane antennas.

A monopole can be visualized as being formed by replacing one half of a dipole antenna with a ground plane at right-angles to the remaining half. If the ground plane is large enough, the radio waves reflected from the ground plane will seem to come from an image antenna forming the missing half of the dipole, which adds to the direct radiation to form a dipole radiation pattern, because it radiates only into the space above the ground plane, or half the space of a dipole antenna, a monopole antenna will have a gain of twice the gain of a similar dipole antenna, and a radiation resistance half that of a dipole.

Some mobile wireless communication applications (cell phone, pager) printed monopole antennas also evolved. Now days multiband or wide band wireless communication systems are becoming more popular and have been developed rapidly. As with developments, there has been an increased demand for high data rate and reduced size antenna. The printed monopole become more popular because of its low cost factor and fabrication simplicity, easily integrated in communication systems. One of the most popular emerging technologies is WLAN where standard specify two operating frequency (2.4-2.48 GHz) and (5.15-5.35 GHz). Especially in cases of devices like laptop move from one cell to other with different operating frequency band where a dual band antenna can be very useful. And these antennas are concealed antenna for the system i.e. there is no protruded portions in appearance for antenna. These antennas require a small volume of the system is very useful / attractive for wireless LAN or Bluetooth applications.

In this chapter, printed monopole antenna evolution and design discussed, followed by design of Dual-band monopole antenna. Printed monopole antennas reported in [28-30] are capable of single band of operation only, and the printed dual-band inverted-F monopoleantenna shown [31] requires shorting pin for ground connection, which increase the antenna complexity

and fabrication cost as well. In addition to the design using the printed monopole antenna, the printed dipole antenna for dual-band operation has also been introduced in [32]. It also has been seen that dual band monopoles such as U-shaped monopoles [33], ring monopole [34] and L-shaped monopole [35] also appeared in literature.

3.4.1 Design Methodology

The implemented antenna is monopole because these antennas are concealed antenna for the system and can be obtained without any protruded portion in appearance as well as occupying a small volume of the system are very useful for wireless LAN or Bluetooth application. As shown in Figure 5.1 the proposed antenna has two rectangular elements having different shapes which are stacked on each other and fed by a 50Ω microstrip line of width W_f=3.5mm and length L_f = 10mm. These rectangular monopole elements were printed on one side having. L=45mm, width W=35mm and thickness h=1.5224 mm over substrate NH9338 substrate of ε_r=3.38.

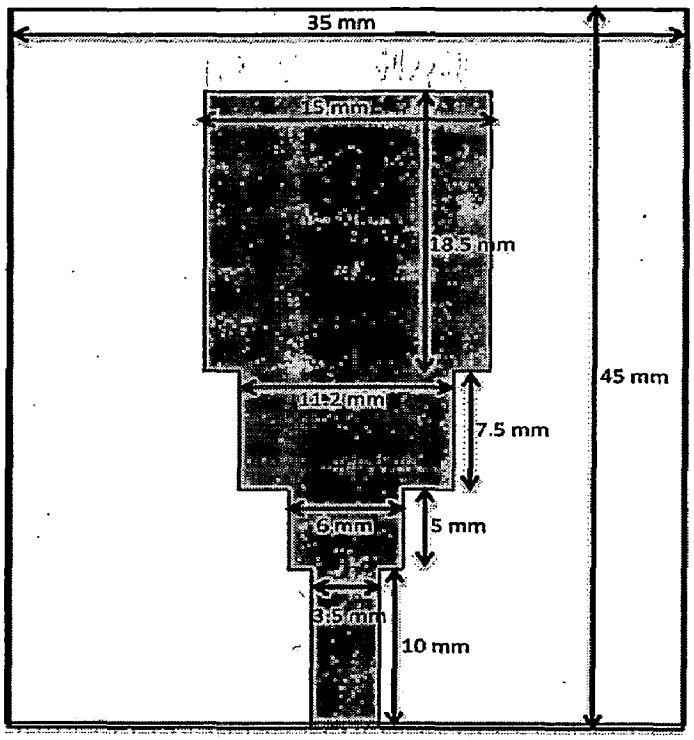

Figure 3.22: Dual band Monopole Antenna

The ground plane is printed on the other side of the substrate with length L_g=9.2mm and width W_g=35mm in this antenna design the smaller rectangular monopole element controls the higher order operating mode of the proposed antenna. Smaller rectangular monopole has a widthof W_s= 11.2mm and length of L_s=7.5mm. The bigger rectangular monopole element is used to control the lower order operating mode of the antenna with W_b=15mm and L_b=17.5mm. There is another element is used to improve the return loss at both frequencies having width W_e=6mm and L_e=5mm. One thing to note that operating frequency and operating BW is very sensitive to change in the size of ground plane.

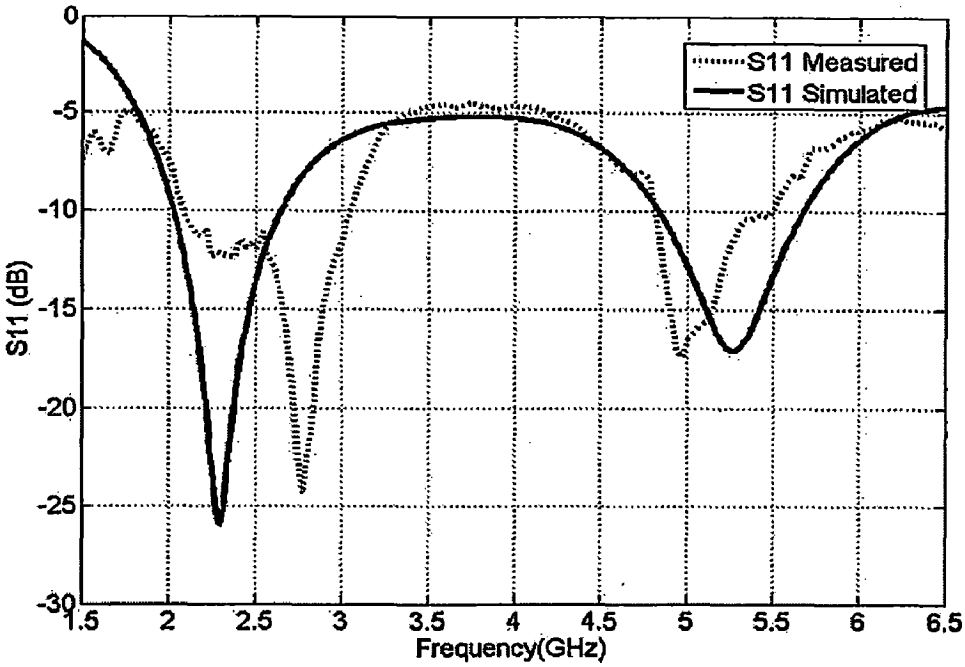

Figure 3.23: Simulated and Measured Return loss Characteristic of the Proposed Antenna

The structure proposed by [36] is also uses the small metallic strip in right hand of the element to improve the return loss response but we can also improve the return loss response by increasing the length of bigger patch relatively to smaller patch. As we see mismatch in the response which may be due to fabrication tolerance.

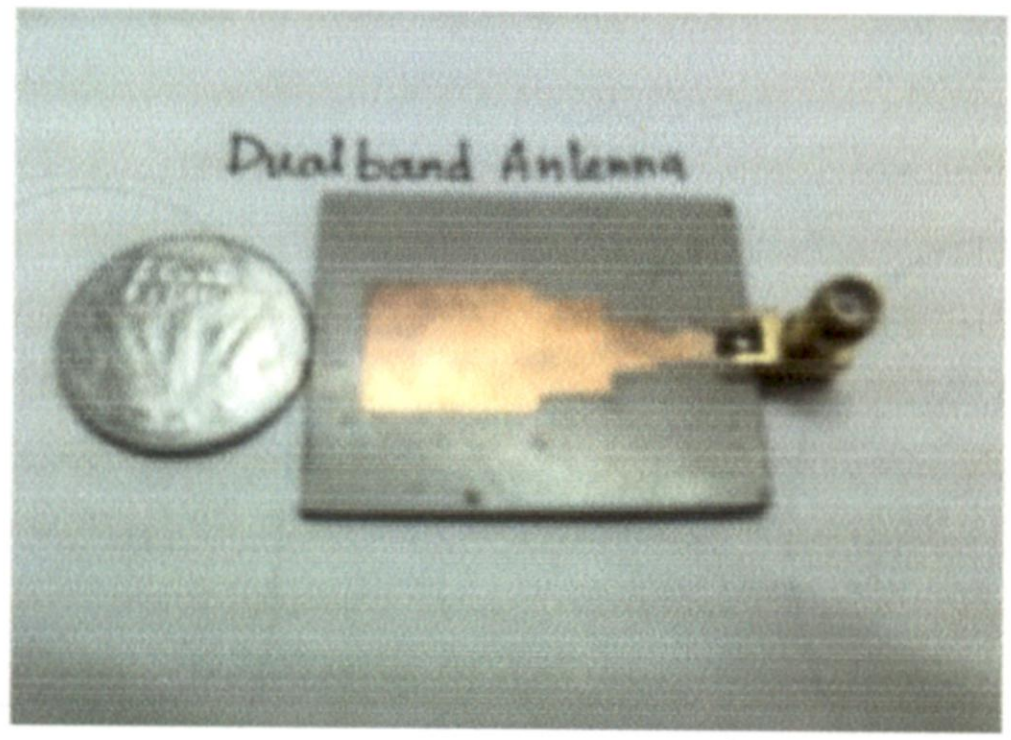

Fig 3.24: Implemented Dual-band Monopole Antenna

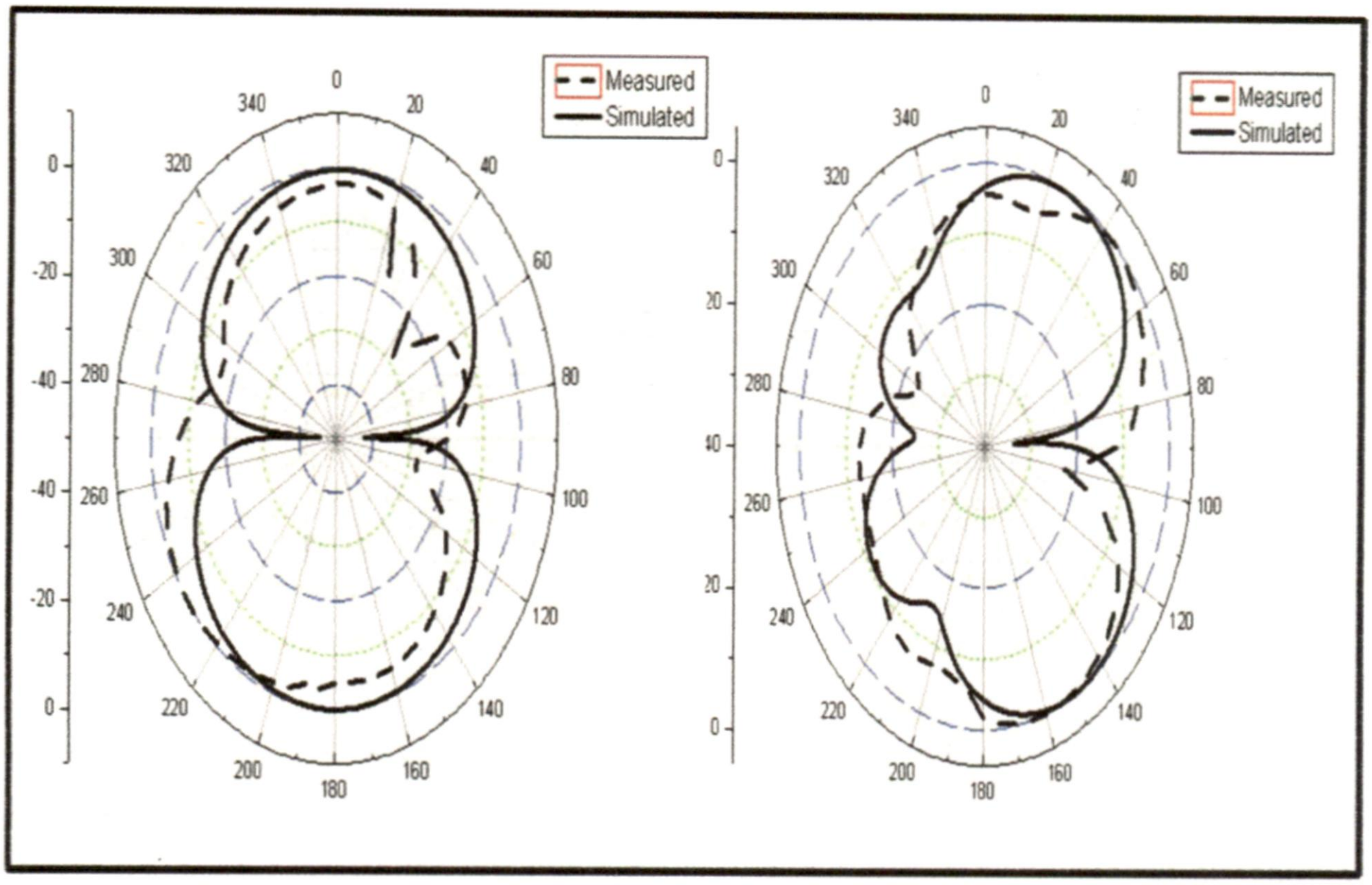

Figure 3.25: Measured and Simulated E-plane Radiation Pattern at 2.4(L) and 5.2(R) GHz

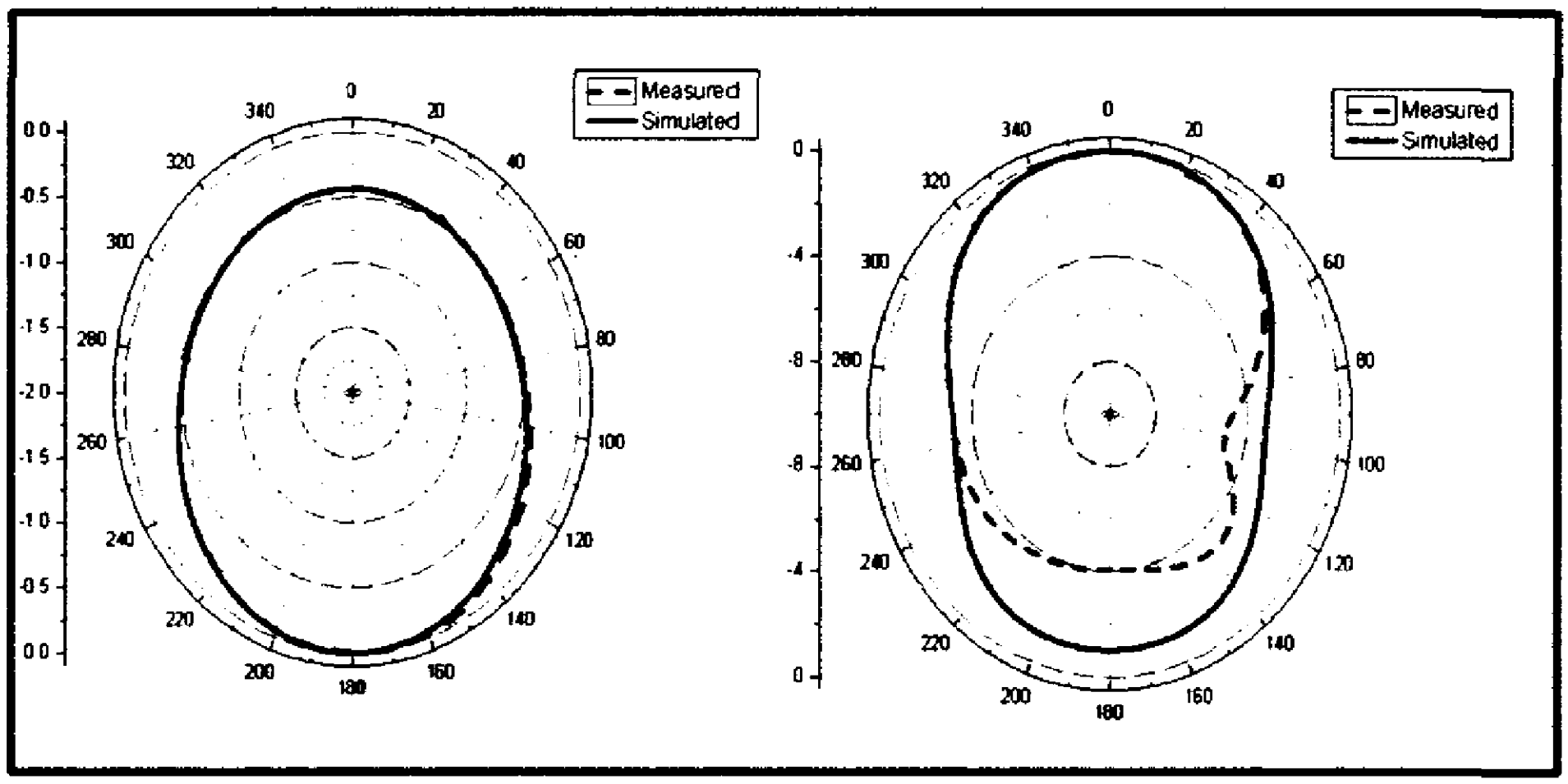

Figure 3.26: Measured and Simulated H- plane Radiation Pattern at 2.4(L) and 5.2(R) GHz

Table 3.5:Comparison of Proposed Antenna with some Standard Printed Monopole Antenna

@	BW	
	f_c @2.44GHz	f_c @ 5.25GHz
Reference [34]	760 MHz	720MHz
Reference [30]	570MHz	310MHz
Proposed	950MHz	720MHz

3.3 Conclusion

This chapter presented the design of all passive components in the proposed architecture. The filter design procedure here presented for microstrip coupled-line filter, and help taken from the filter design guide of Agilent ADS (Advance design System). The Dual band power combiner design is also completed based on π-section microstrip line. The dual-band antenna simulation was performed in CST Microwave studio. These all passive components are giving satisfactory response that is already mention in form of figures and tables.

Design and implementation of concurrent Dual-Band LNA

4.1 Introduction

The low noise amplifier is the first active block of RF receiver front-end. Commercially, several implementations propose dual-band LNA's covering the whole WLAN b/g/a standards. However, they mostly use two parallel LNA's, which is obviously not a cost-efficient solution. A concurrent LNA is most suited because it enables saving die area (~25%) and power consumption (~ 40%) compared to the parallel LNAs approach [37].

4.1.1 A Review of Single-Band LNA Design Issues

Being the first active element in the receiver chain, the noise figure (NF) of an LNA plays a significant role in the overall NF of the receiver, which controls its sensitivity and output signal-to-noise ratio (SNR) [38]. Before exploring the design details of concurrent multiband LNAs, it is helpful to review some of the existing technological and topological choices for single-band LNAs.

(A) Technology

The bipolar junction transistor was the first solid-state active device to provide practical gain and NF at microwave frequencies [39]. In the seventies, breakthroughs in the development of field-effect transistors (FETs) (e.g., GaAs MESFET) led to higher gain and lower NF than bipolar transistors for the frequencies in the range of several giga hertzes. Currently, advanced FETs and bipolar transistors still compete for lower NF and higher gain at frequencies in excess of 100 GHz. Examples are the high electron-mobility transistors (HEMTs), such as pseudomorphic high electron-mobility transistors (pHEMTs) , metamorphic high electron-mobility transistors (MHEMTs) [40], as well as heterojunction bipolar transistors (HBTs) , built using a variety of semiconductor materials (e.g., GaAs, InP, Si, SiGe). Traditionally, very low-

noise amplifiers at high frequencies have been made using transistors with high electron mobility and high saturation velocity on high-resistivity substrates for the following principal reasons.

1) Higher carrier mobility and peak drift velocity result ina higher transistor transconductance and shorter carrier transit time for a given current, thus allowing for the reduction of the dc current for the same transconductance (gain) in transistors which lowers the input-referred noise and, hence, the NF. This gives compound semiconductors a significant advantage over silicon, as for instance, the electron mobility and the peak drift velocity are typically six and two times larger, respectively, for GaAs when compared to silicon .

2) Higher carrier mobility also results in lower parasitic drain and source series resistors. The parasitic source resistance can be a major contributor to the overall NF of certain LNAs, such as those used for satellite communications.

3) Due to mostly technological limitations, the series input resistance of silicon-based transistors is usually higher than those of compound semiconductors. In particular, the lower resistance of the metal gate of GaAs MESFETs compared to higher resistance of the poly-silicon gate in MOSFETs and thin bases in bipolar transistors, result in a lower NF for GaAs transistors.

4) The loss properties of on-chip passive components can have a significant effect on the noise and gain performance of the LNAs. High-resistivity substrates minimize the substrate loss components. As the loss and noise are closely related through the fluctuation-dissipation theorem of statistical physics [41], [42], the energy loss reduction translates to a lower NF for the amplifier.

Despite the above mentioned limitations of silicon technologies, several silicon LNAs have been reported. Meyer *et al.* reported one of the early LNAs made on a low-resistivity (i.e., lossy) silicon substrate using bipolar junction transistors for commercial cellular applications [43], where very low NF is not needed. Recently, a large number of efforts have been reported to use the advanced digital CMOS processes for single-chip implementation of the complete radio transceiver [44], [45].

(B) Topology

Although several different topologies have been proposed to implement LNAs, we will only focus on two most common single-stage1 LNAs, the common-gate topology and inductively degenerated common-source stage. The common-gate configuration uses the resistive part looking into the source of the transistor to match the input to well-defined source impedance (e.g., 50). In a common-source LNA, inductive degeneration is used to generate the real part needed to match the LNA input to the preceding antenna or filter. The ideal lossless inductive feedback moves the source impedance for optimum NF toward the optimum power match with a minor increase in the minimum NF. It should be mentioned that in these cases cascode configuration can be used to enhance the stability and reverse-isolation of the amplifier.

An approach is to use Smith charts to find the optimum impedance for noise and power matching at the input of the amplifier for given active device. Although the Smith chart is a very convenient tool for seeing how close we are to the minimum NF and the maximum gain of a given device, it does not show the effect of individual noise sources on the total NF. This is particularly important for a concurrent multiband LNA, since different noise sources behave differently at different frequencies. Unlike bipolar transistors whose dc current sets the trans-conductance and minimum noise-figure, MOSFETs offer extra degrees of freedom in choosing the device width and length. In the next section, we present a general approach for the design of concurrent multiband LNAs which are important building blocks in concurrent receivers.

4.1.2 A Review of Concurrent Multiband LNA

In conventional dual-band LNAs, either one of the two single-band LNAs is selected according to the instantaneous band of operation, or two (three) single-band LNAs are designed to work in parallel using two (three) separate input matching circuits and two (three) separate resonant loads .The former approach is non-concurrent, while the latter consumes twice (three times) as much power if used in a concurrent setting. The other existing approach is to use a wide-band amplifier in the front-end. Unfortunately, in a wide-band LNA, strong unwanted blockers are amplified together with the desired frequency bands and significantly degrade the receiver sensitivity. To design multiband LNA, requirement of multi-band matching network is

necessary that capable of simultaneous match transistor's complex (i/p and o/p) impedances to source and load at multiple frequencies. In next section we discuss some reported multi-band matching techniques.

4.2 Design of Dual-band Matching Network

4.2.1 Concurrent Dual-Band Microstrip Matching Network

There is a lot of contribution of researcher's in micro-strip dual band matching network design and started from [25]. The concept is arise from the fact that a transmission line can be represented by an equivalent T and π-network and T and π network itself transferable. Before going look into problem our motive is to match the input and output complex impedances of transistor at two different frequencies. The problem of matching frequency-dependent complex impedances was first discussed [46] where the impedances were assumed to be unequal in both frequencies. A three section impedance transformer is also proposed by Liu. X. et al.[47] to match to complex impedance. Another approach was also discussed in [48] using four section are using two achieve matching and finally [49] uses a T-section to achieve matching.

$$Z_3 = \sqrt{R_{Li}R_{L2} + X_{L1}X_{L2} + \frac{X_{L1}+X_{L2}}{R_{L2}-R_{L1}}(R_{L1}X_{L2} - R_{L2}X_{L1})} \tag{4.1}$$

$$L_3 = \frac{n\pi + arctan\left(\frac{Z_c(R_{L1}-R_{L2})}{R_{L1}X_{L2}-R_{L2}X_{L1}}\right)}{(m+1)\beta_{31}} \tag{4.2}$$

Where $m=f_2/f_1$ and $\beta_{31} = \frac{\theta_3}{L_3}$ and n is an arbitrary integer that should be chosen minimum andsome design equation to design dual band T-matching network are given as

$$Z_1 = \sqrt{\frac{Z_0(1 - Z_0 G_{right} + tan^2(\theta_1)}{G_{right} tan^2(\theta_1)}} \tag{4.3}$$

$$Z_2 = \begin{cases} \frac{-tan(\theta_2)}{(B_{right}+B_{left})}, & openstub \\ \frac{cot(\theta_2)}{(B_{right}+B_{left})}, & shortedstub \end{cases} \tag{4.4}$$

Where $\theta_2 = \frac{\pi}{1+m} and \theta_1 = \frac{\pi}{1+m}$

4.2.2 Design Tools

The primary simulation tool used for the design is Agilent's Advanced Design System (ADS). The enhancement mode p-HEMT ATF-54143 BLKG has been used for the design and fabrication. The substrate used has a dielectric constant of 3.32. An ADS-model for the used transistor ATF-54143 was obtained and has been used for all simulations in ADS. The large signal circuit performance has been simulated using the Harmonic Balance Simulation in ADS. It combines frequency domain analyses of linear elements with time domain analyses of nonlinear elements to iteratively converge on a steady state solution at the fundamental frequency and a pre-determined number of harmonics. In this way the simulator can generate a periodic steady state time domain response of a nonlinear circuit more quickly than a standard time domain simulator would.

In addition to harmonic balance simulation and other simulation tools in ADS, EMDS simulations have been used to accurately model the input and output matching networks.

4.3 Design Procedure

The whole design procedure in ADS consists of the following major steps:

1. DC Bias Simulation and Bias Network Design
2. S-Parameter Simulation to find out the S-Parameters for the transistor.
3. Harmonic Balance Simulations and Optimization
4. Generation of EMDS Layout for the designed matching network
5. Simulation and Optimization of the layout in EMDS.

4.3.1 DC Bias Simulation

First of all a DC Bias Simulation was performed in ADS using the ADS model for the used transistor ATF-54143. From the FET Curve Tracer template, an operating quiescent point was selected for linear operation of the transistor in the active region given in Table 4.1. The DC Bias simulation setup in ADS has been shown in figure 4.1.

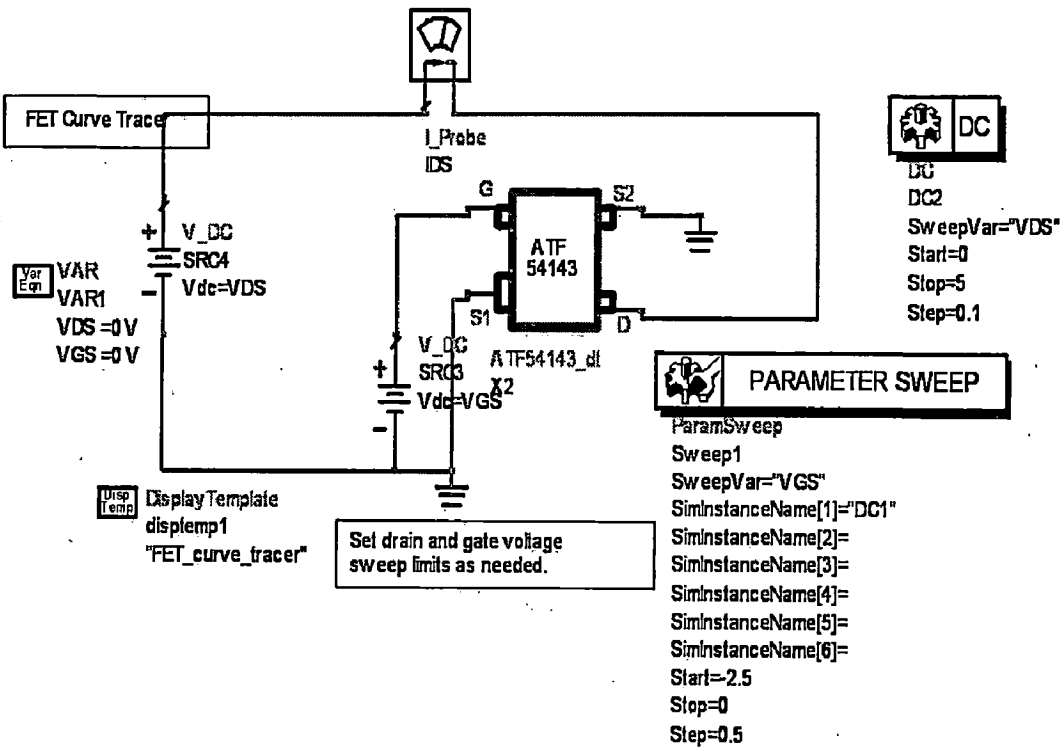

Figure 4.1 DC Bias Simulation Setup in ADS for ATF 54143

Table 4.1: Operating Quiescent Point of Transistor ATF 54143 BLKG

Symbol	Parameter	Value
V_{ds}	Operational Drain to Source voltage	3.0 volts
I_{ds}	Operational Drain to Source current	60 mA
V_{gs}	Operational Gate to Source voltage	0.6 volts

4.3.2 S-Parameter Simulation

To a circuit designer transistor is looked upon as a two port network described by its S-Parameters. The S-Parameters of a transistor directly relate to the characteristics of the transistor and are required for any design that uses the transistor.

The S-Parameters for the transistor at the specified bias have been obtained using the S-Parameter Simulation in ADS for the used transistor model. The circuit simulation setup has been shown in figure 4.2

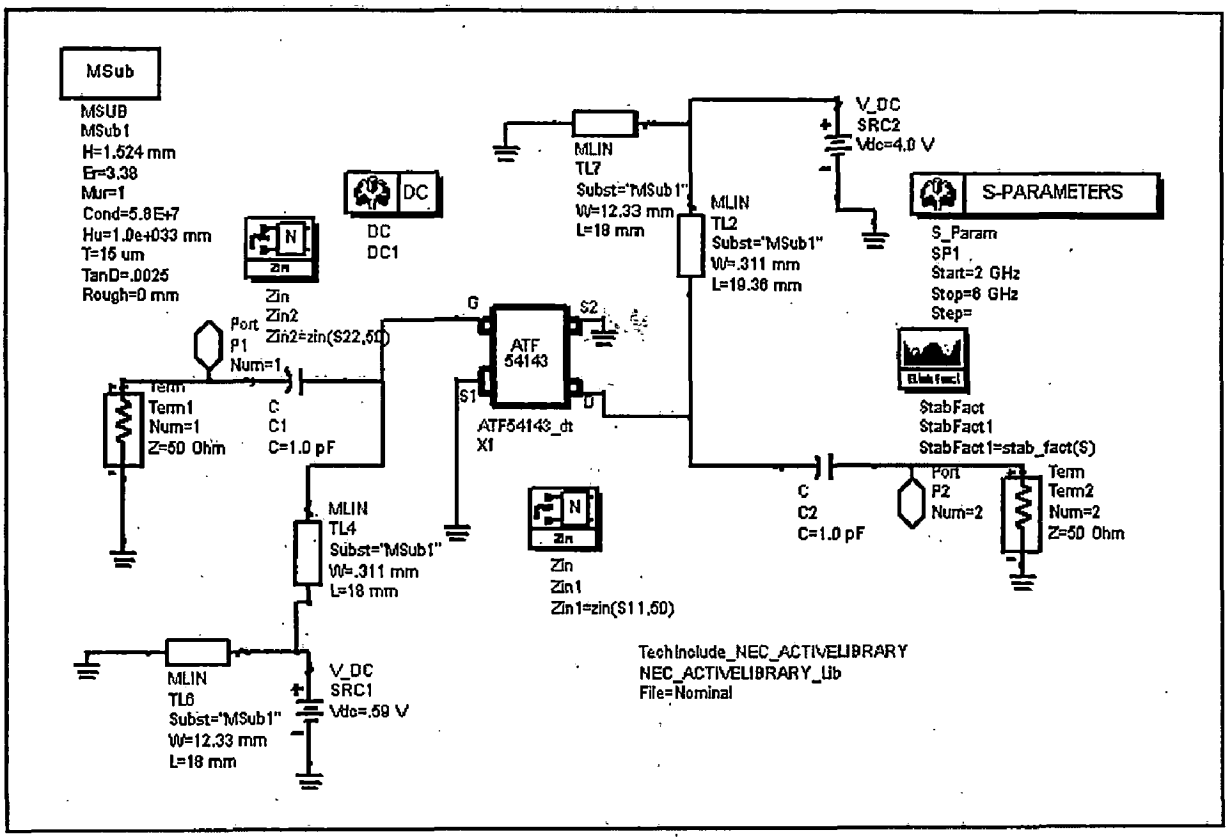

Figure 4.2: S-Parameter Simulation Setup in ADS

4.3.3 Harmonic Balance Simulations and Optimization

Harmonic-balance simulation calculates a circuit's steady-state response. It is well-suited for simulating analog RF and microwave circuits, since these are most naturally handled in the frequency domain. It calculates the magnitude and phase of voltages or currents in a potentially nonlinear circuit and uses it to generate the output spectrum.After the design of the complete circuit for the Dual-Band Low Noise Amplifier, harmonic balance simulations were performed in ADS to analyze the output. Tuning and optimization tool in ADS was used for the optimization of the final output. The Harmonic Balance simulation setup has been shown in figure 4.3.

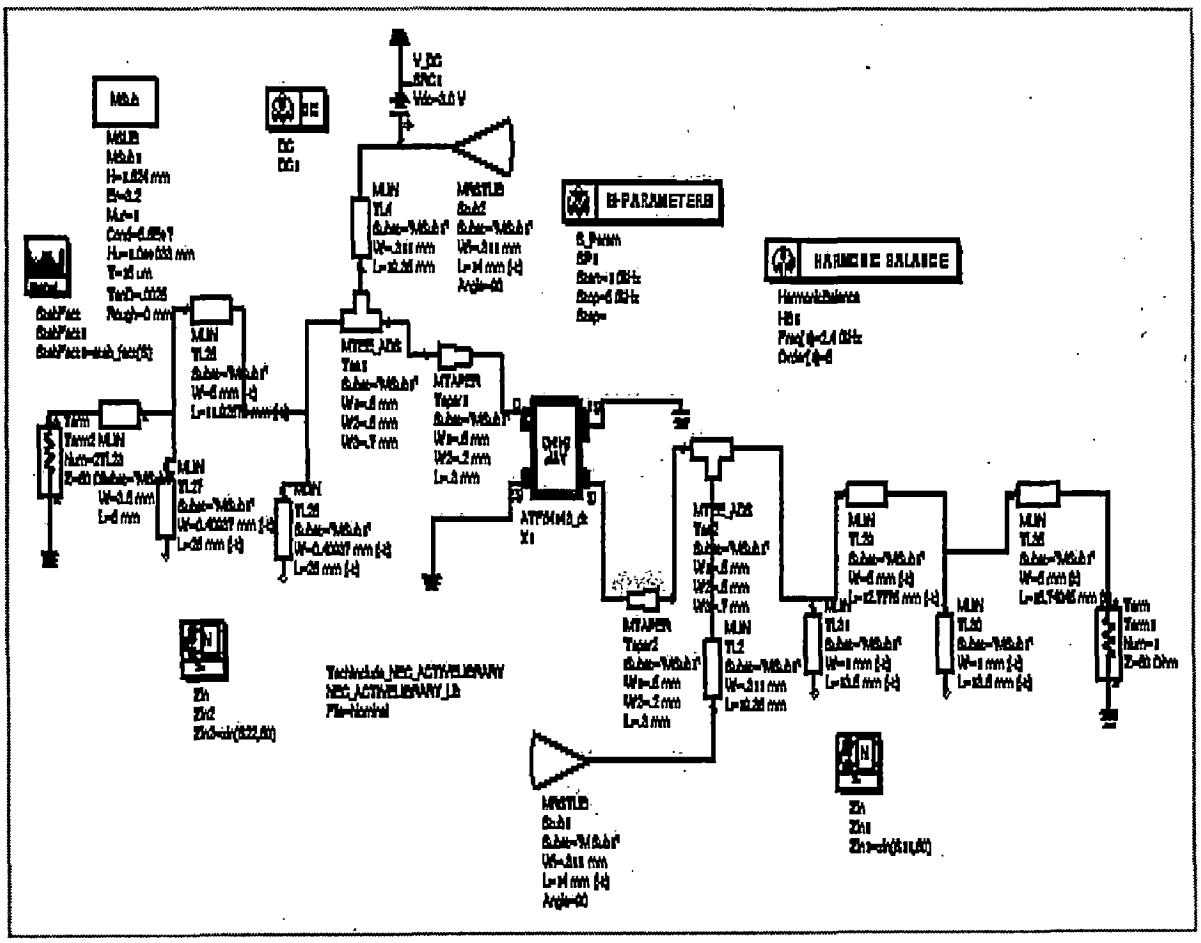

Figure 4.3: ADS Harmonic Balance Simulation Setup

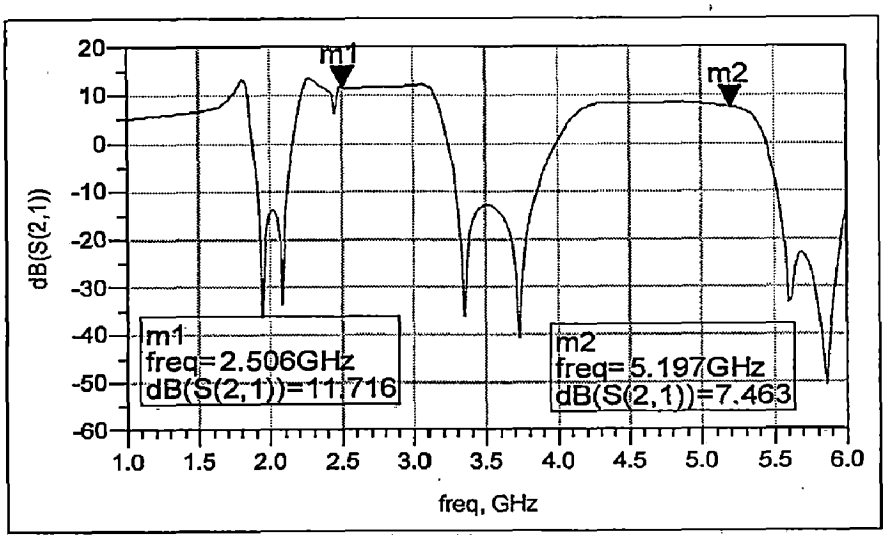

Figure 4.4: S-Parameter S_{21} Response of LNA after HB Simulation

4.3.4 Design of EMDS Layout for the LNA

EMDS is an electromagnetic simulator that computes S-parameters for general planar circuits, including microstrip, slot line, stripline, coplanar waveguide, and other topologies. Multilayer RF/microwave printed circuit boards, hybrids, multichip modules, and integrated circuits can be simulated using EMDS.

After successful Harmonic Balance Simulation in ADS for the designed circuit, a Layout is created for the input and output matching network in EMDS. Ports are placed at the input and output of the network, as well as at every point that an external lumped element device would interface with the network. The matching network in ADS Circuit is then replaced with this EMDS Layout and Co-Simulations are performed. The Co-Simulation uses EMDS Simulations for the analysis of the layout.

After successful layout creation, the layout model was created in EMDS and this layout was then simulated in ADS using Co-simulations that use the EMDS model for the layout. The co-simulation setup in ADS has been shown in figure 4.6.

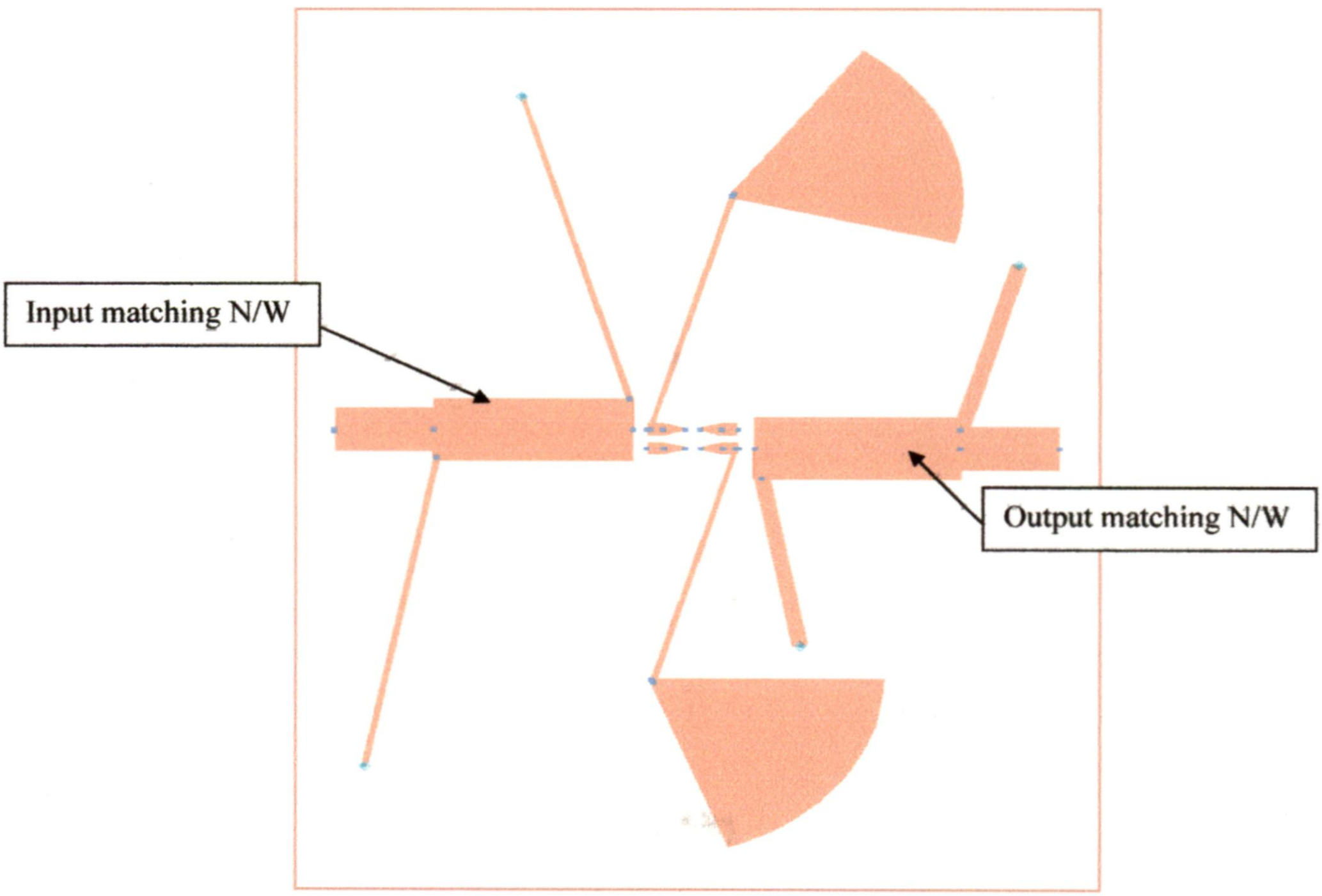

Figure 4.5: Generated Layout in EMDS for LNA

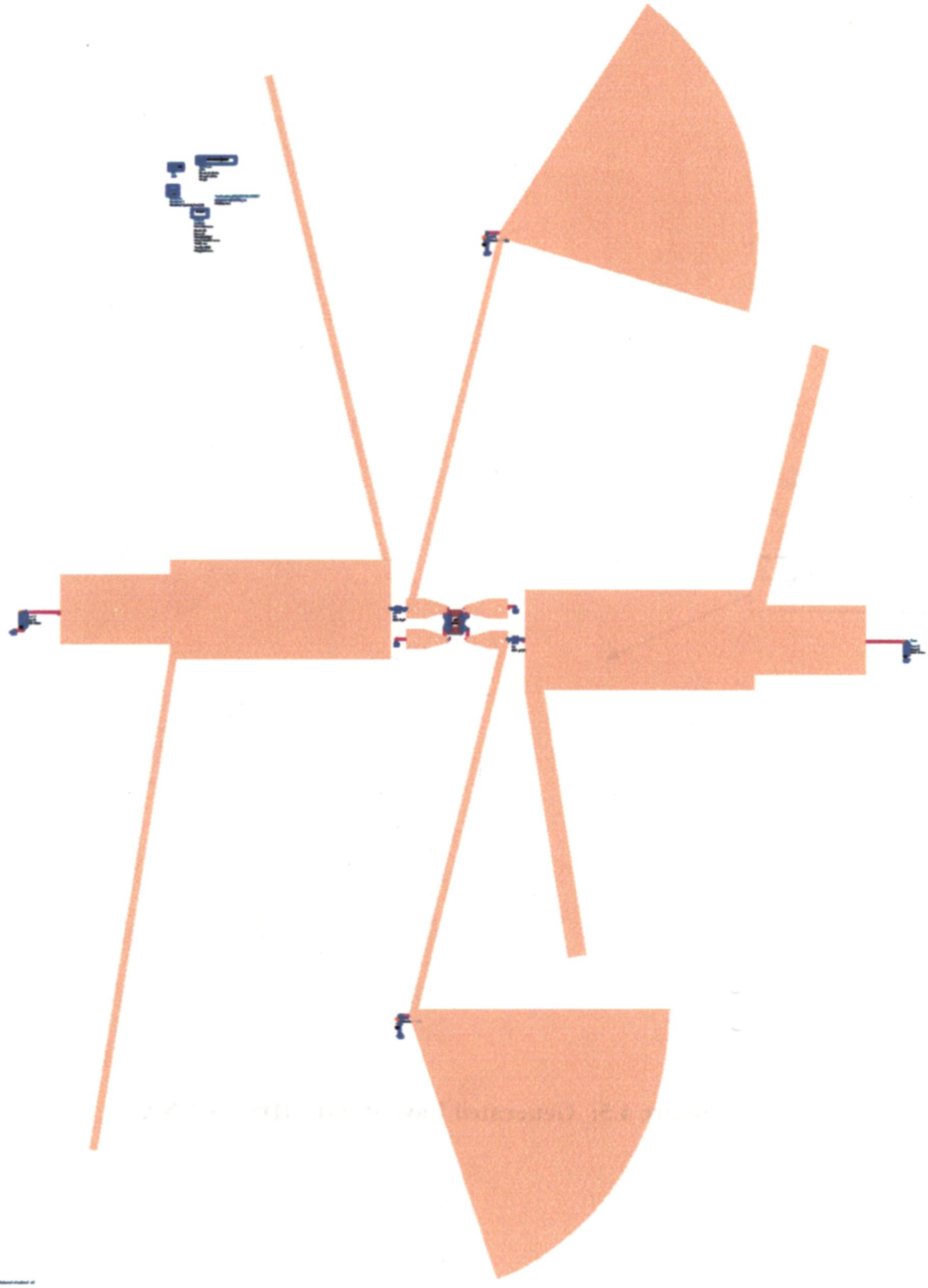

Figure 4.6: Co-simulation Setup for the Designed LNA

After further optimization in EMDS, the simulation results were found to achieve the desired dual-band response. The S-Parameter Curves obtained from the simulations.

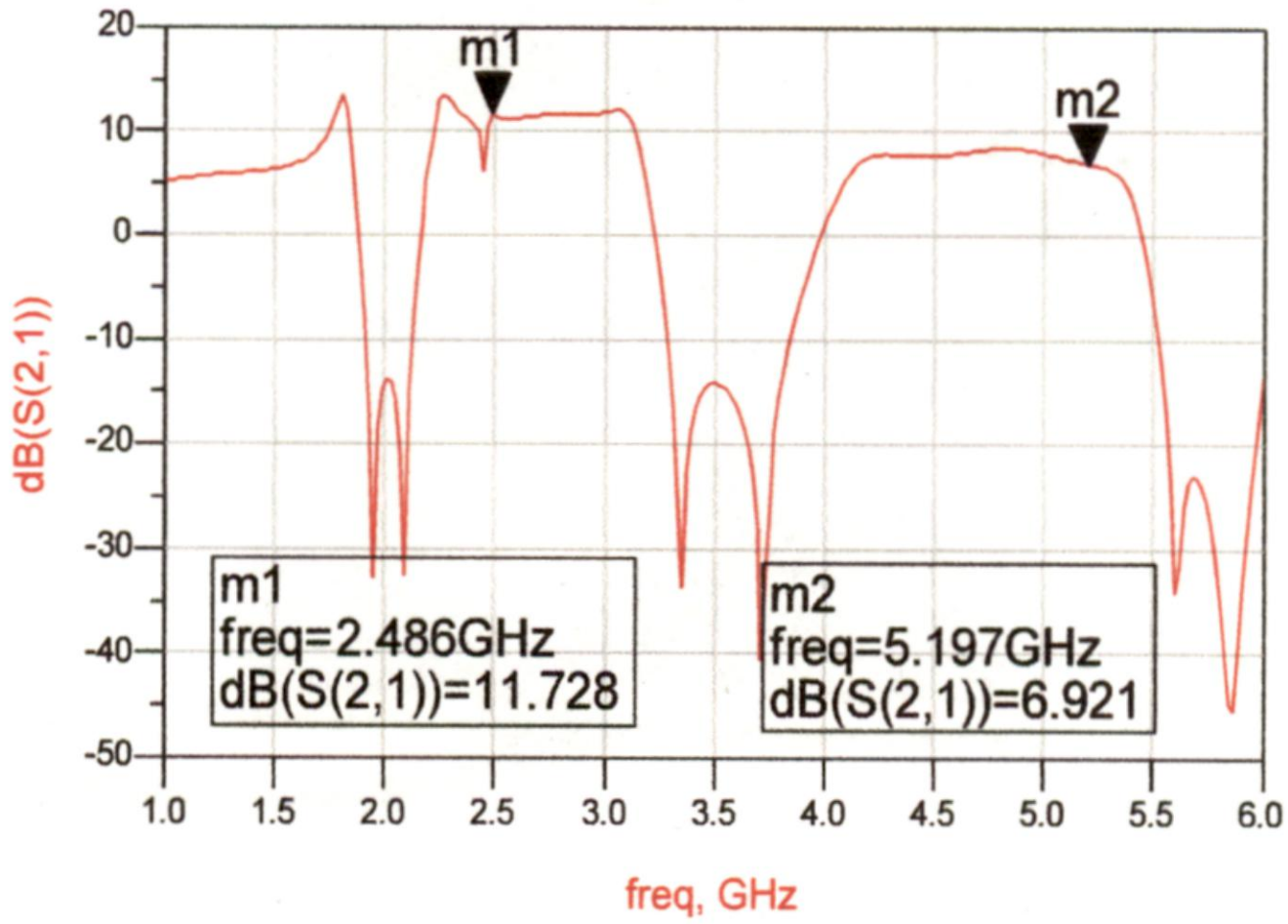

Figure 4.7: Co-Simulation S-Parameter (S_{21}) of LNA

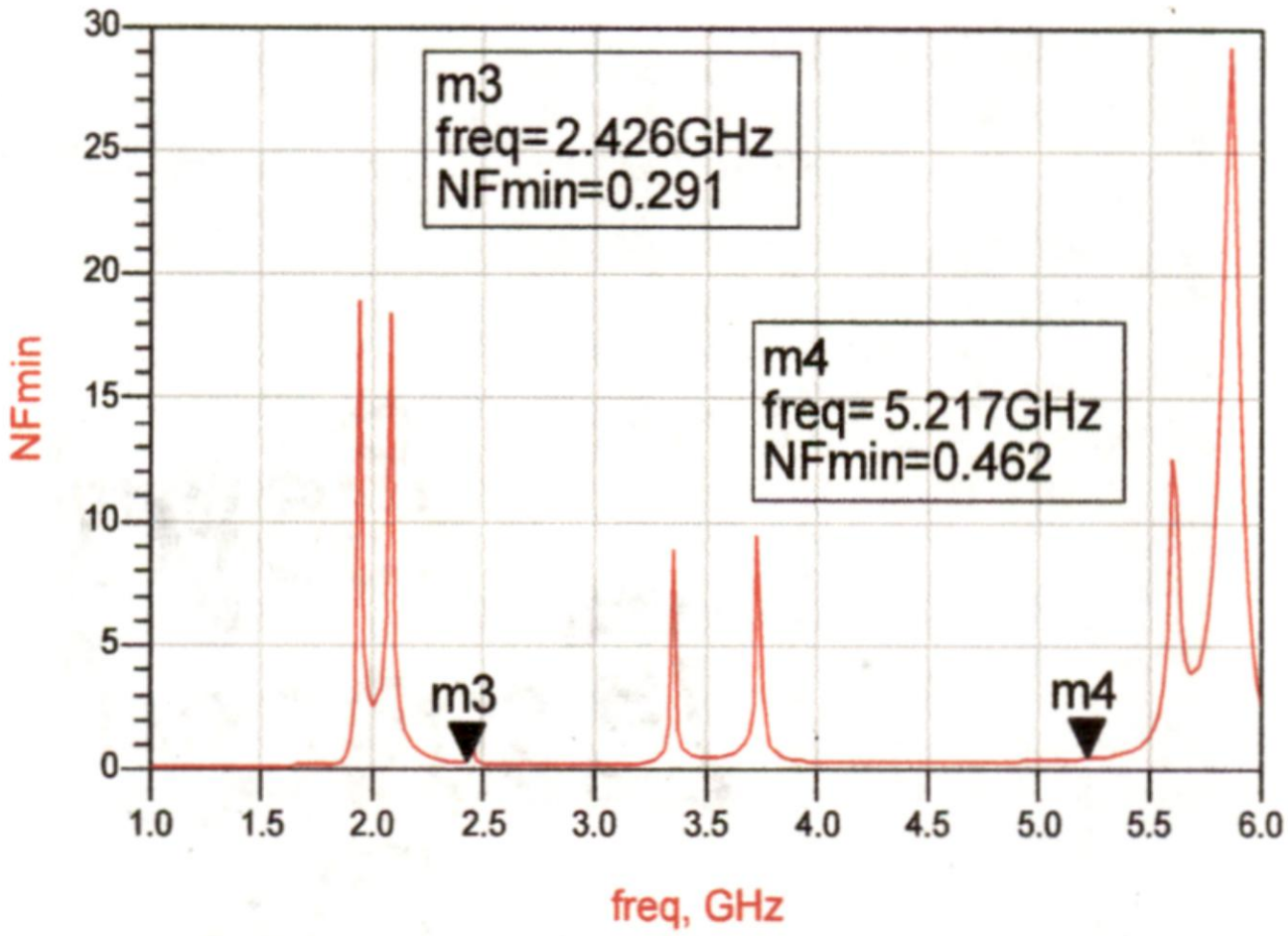

Figure 4.8: Simulated Noise Figure of LNA

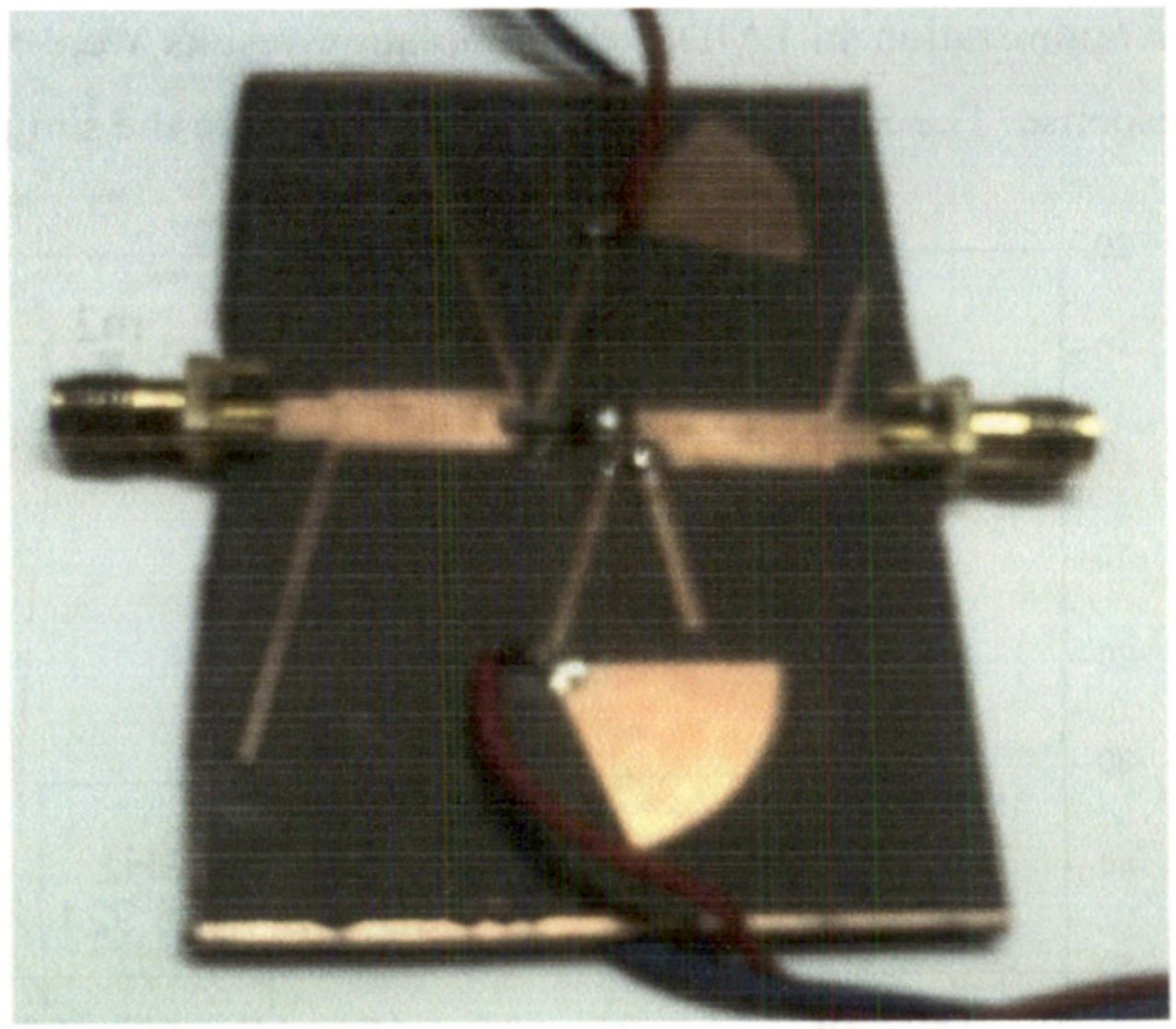

Figure 4.9: Implemented Concurrent Dual-band LNA

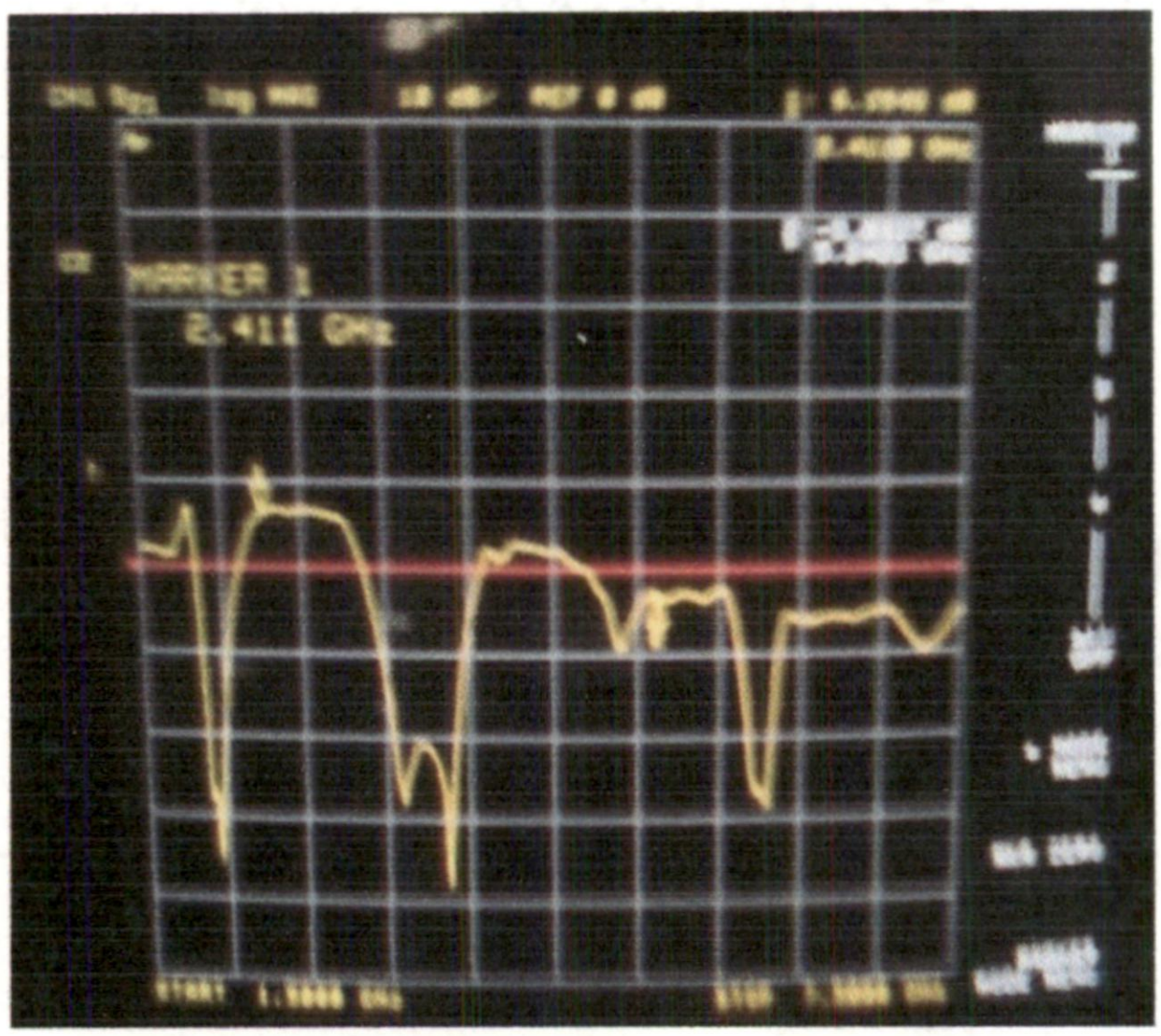

Figure 4.10: Measured S_{21} Response of LNA

4.4. Conclusion

In this chapter successfully designed and fabricated the concurrent dual band LNA with very good noise figure characteristic. However the simulation and the measured results differ that is because of fabrication error and the required biasing point is achieved during the measurement because this requires precision power supply. But the results validates the design of concurrent dual-band.

Analysis and Implementation of Dual-band Transceiver

5.1 Introduction

In this chapter steps for measurement of implemented concurrent dual band transmitter are discussed, that is composed of chain of measurement. Each step explained with the help of block and graphs. At the last, presented the layout of concurrent dual band receiver.

5.2 Design and Development of Dual-band Transmitter

The measurement of transmitter is carried out in the following steps.

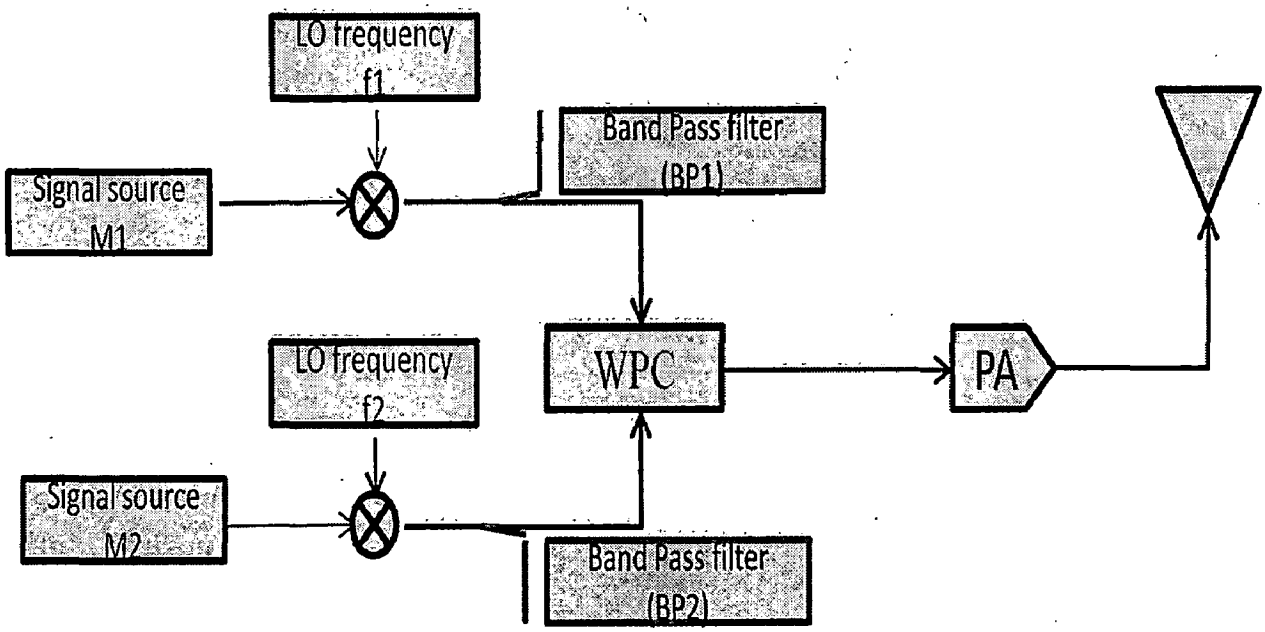

Figure 5.1: Block Setup for Measurement of Transmitter

(A) Checking Mixer Performance

First we check the mixer is performing the operation of frequency conversion. So first we check the performance of ZEM-4300MH+ under the condition f1=2.424 GHz Power = 0 dBm and M1=100 MHz and power = -5 dBm shown in figure 5.2.

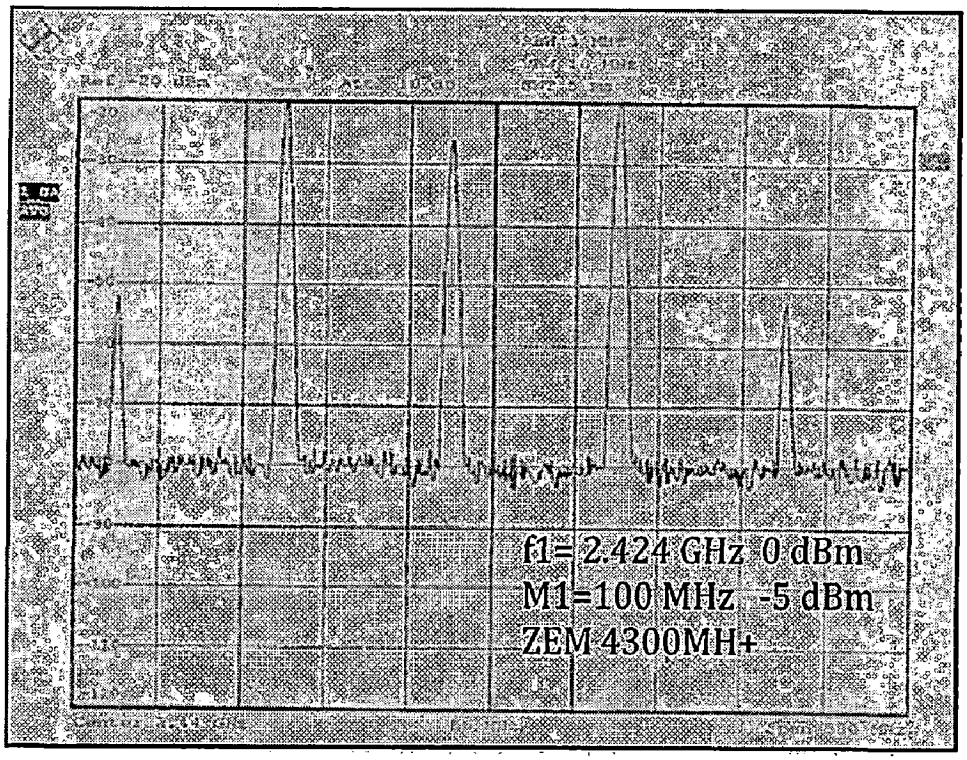

Figure 5.2: Frequency Conversion Characteristics of ZEM-4300MH+

The performance characteristic of ZMX-7GHR shown in Figure 5.3

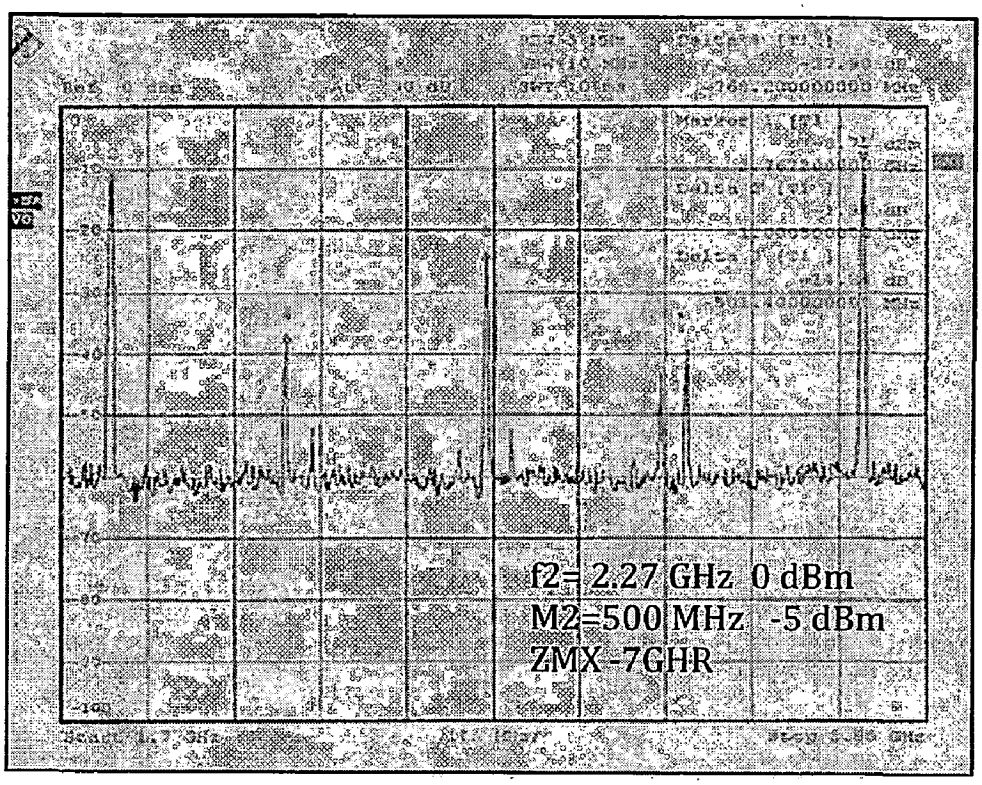

Figure 5.3: Frequency Conversion Characteristics of ZMX-7GHR

(B) Antenna Transmission and Reception in Atmosphere

In this measurement two identical antenna are using one of them is directly connected to a signal source of frequency 2.44 GHz 0dBm and another is connected to the spectrum analyzer. The received spectrum received by antenna shown in figure 5.3

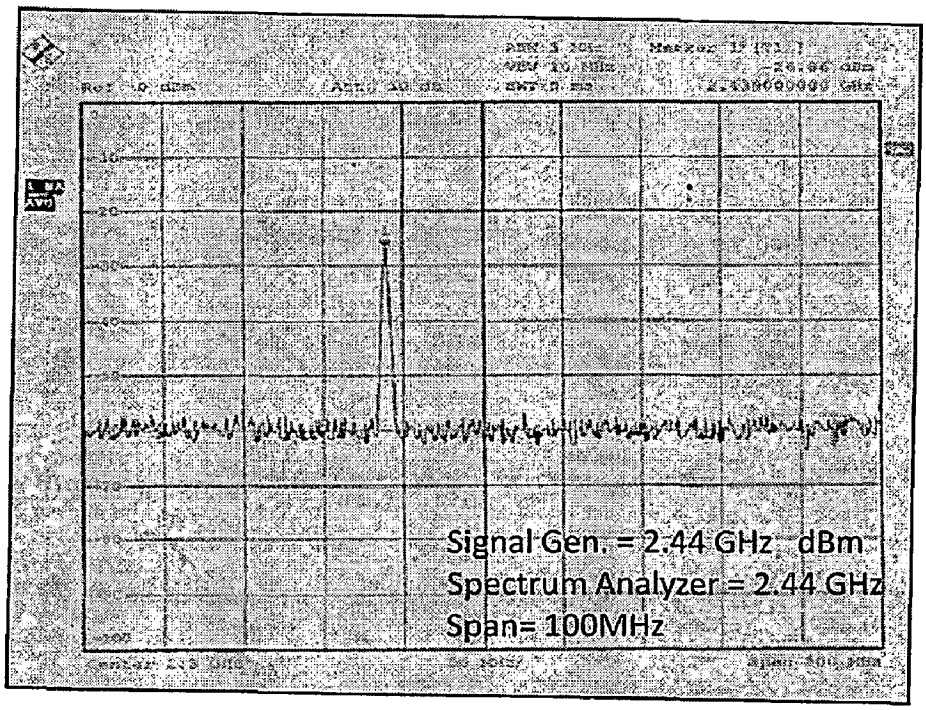

Figure 5.4: Transmission/ Reception Characteristic of Designed Dual band Monopole Antenna

(C) Power Combiner Performance at 2.4/5.2 GHz Band

The complete setup is shown in figure 5.5 and one port of dual band power combiner was fed with 2.44 GHz and another fed by 5.25 GHz and transmitted with designed monopole antenna.

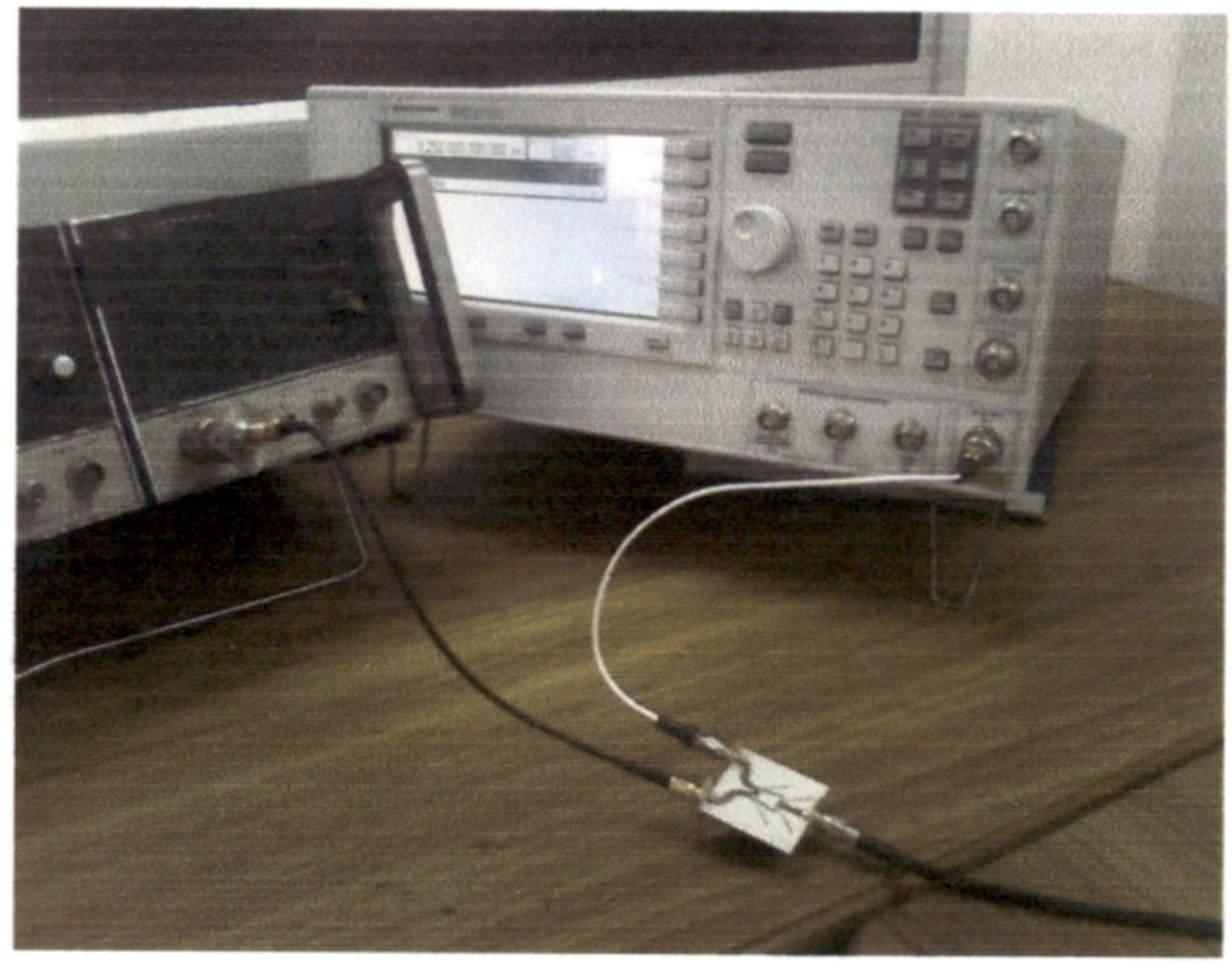

Figure 5.5: Setup for Testing the Performance of Dual-band Power Combiner

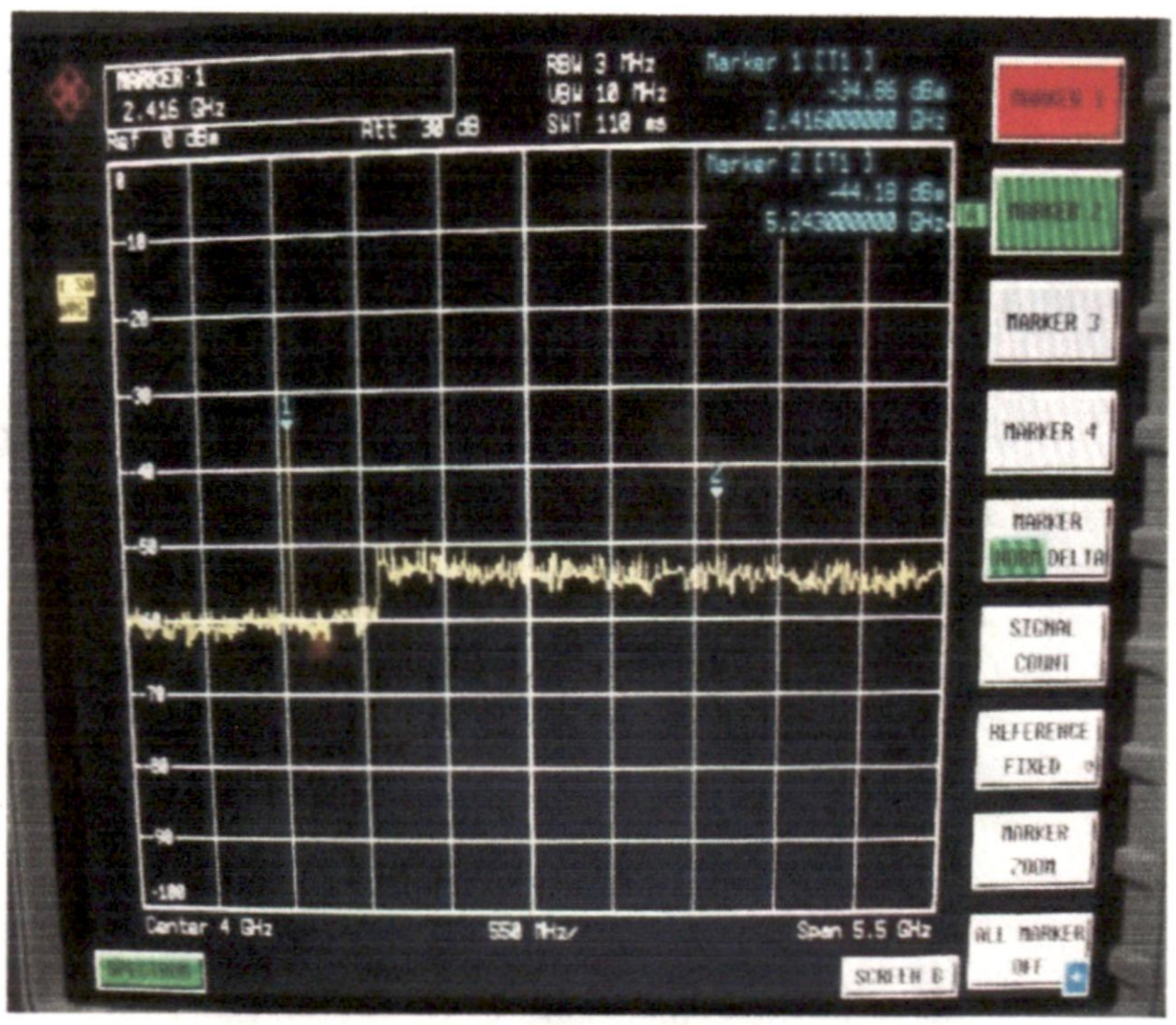

Figure 5.6: Received Spectra by Spectrum Analyzer for setup fig. 5.5

Finally the complete setup for transmitter measurement is set according to figure 5.7

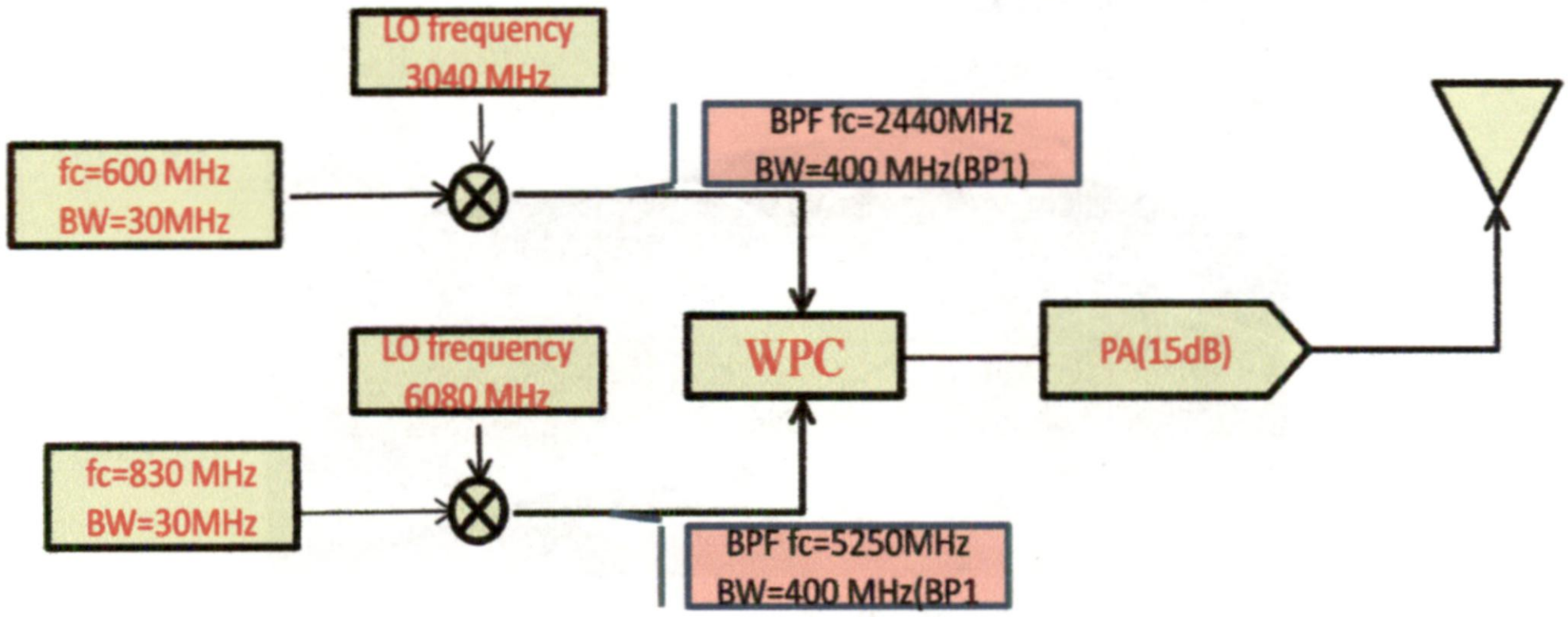

Figure 5.7: Block Presentation of Complete Transmitter Measurement Setup

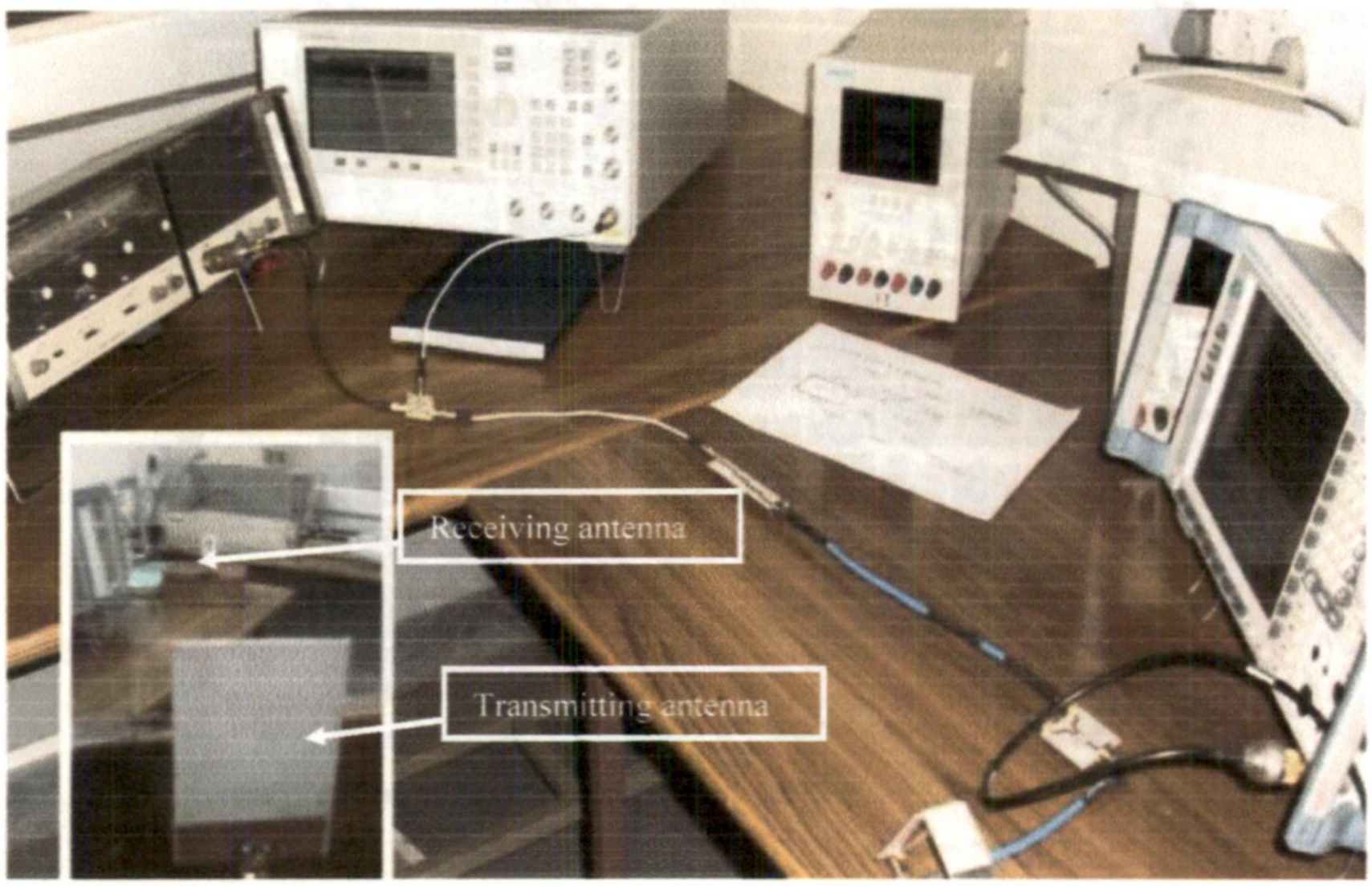

Figure 5.8: Setup for Transmitter Measurement

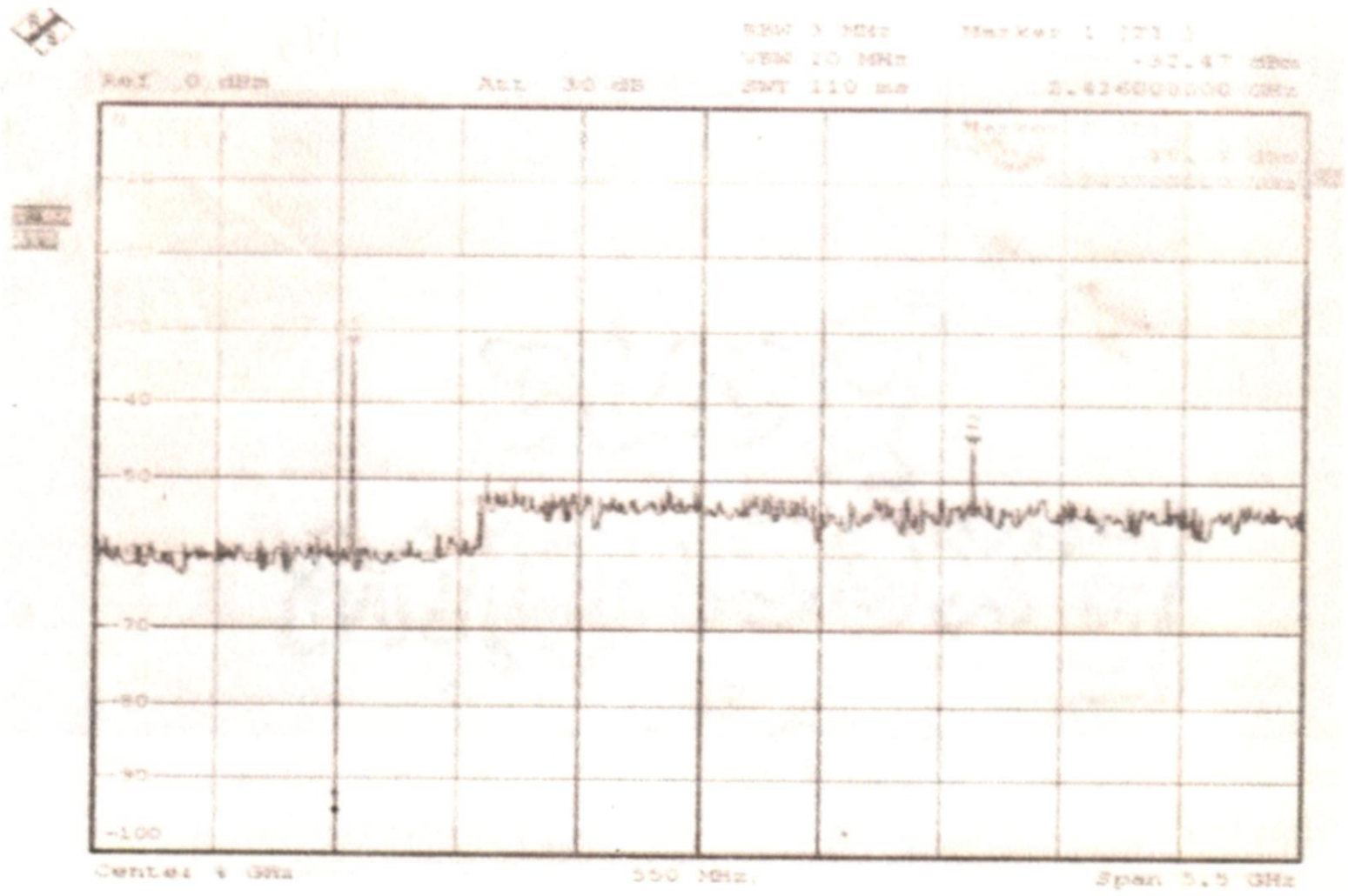

Figure 5.9: Received Spectra of Antenna Connected to Spectrum Analyzer shown in fig.5.8

Thus the concurrent dual-band transmitter is successfully tested. The difference in the power received as shown in figure 5.9 just because of the LO oscillator that generates the 3040 MHz having 10dBm power o/p and another i.e. 6080 MHz giving 5 dBm power o/p.

5.3 *Design and Development of Dual- band Receiver*

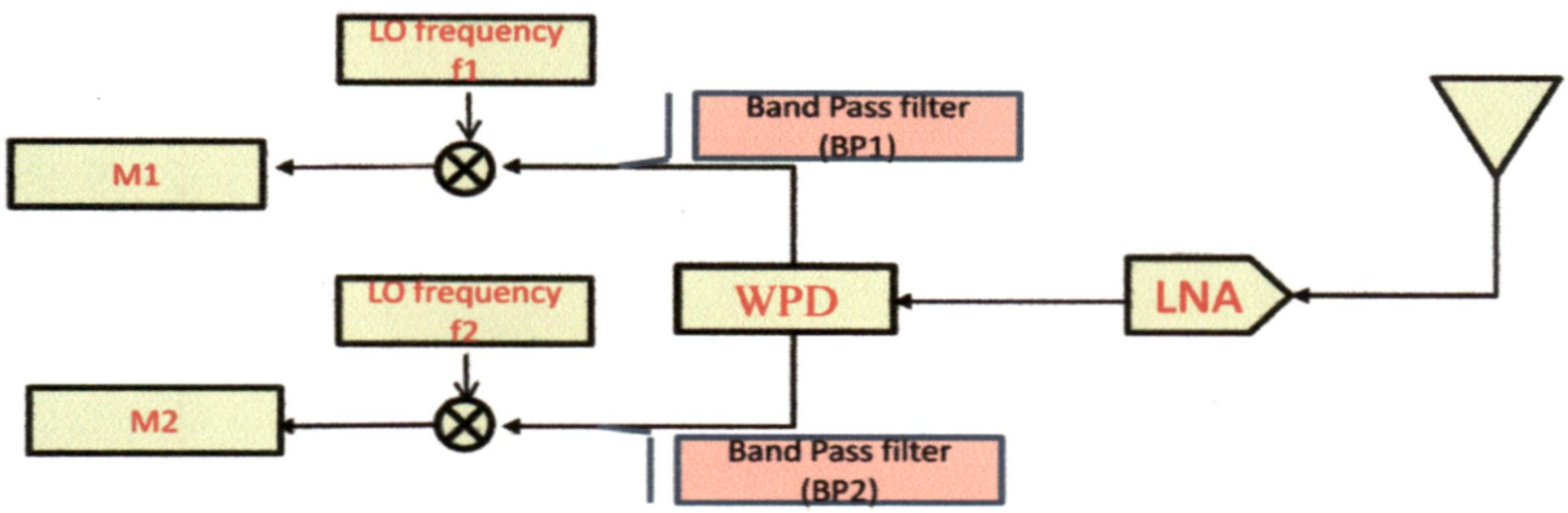

Figure 5.10: Block Representation of Concurrent Dual-band Receiver

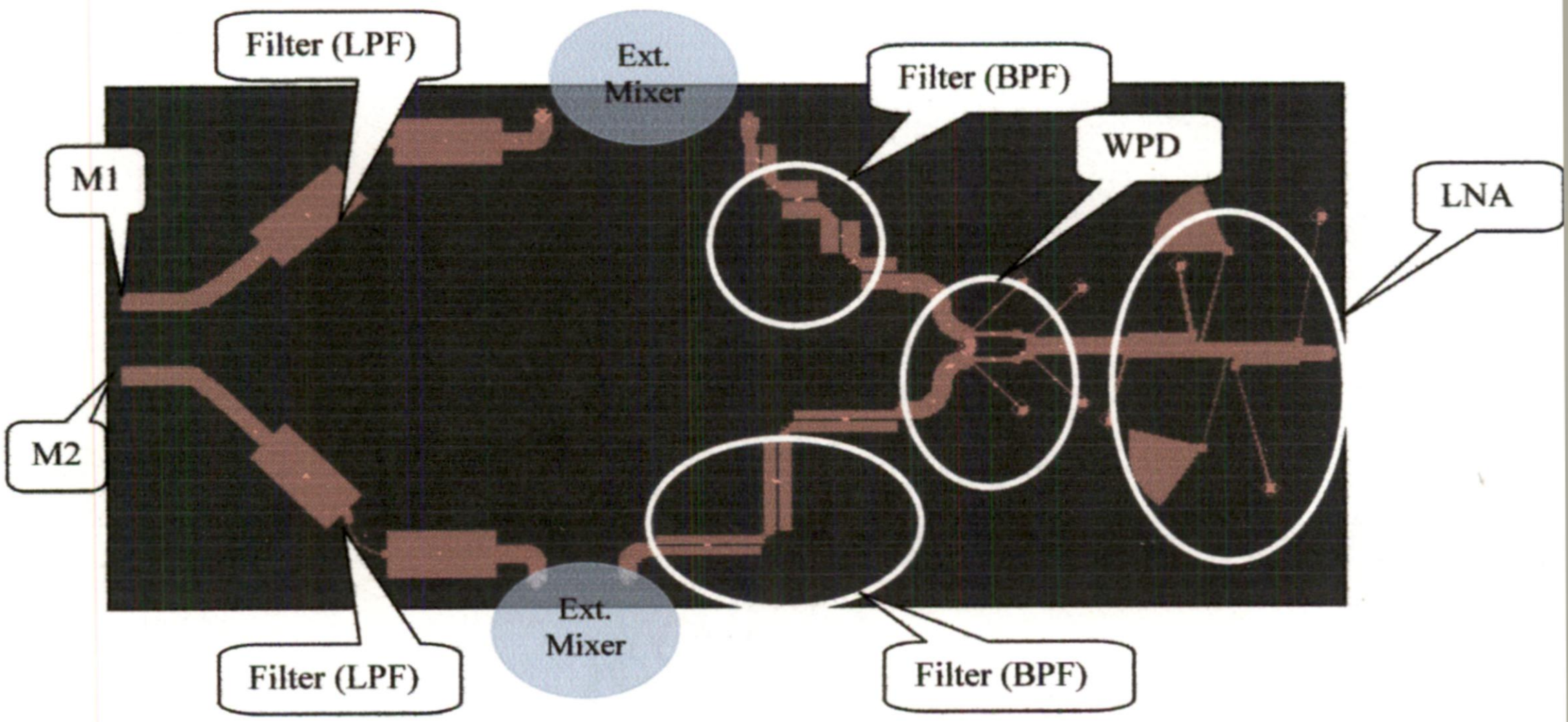

Figure 5.11: layout of Concurrent Dual-band Receiver

5.4 Conclusion

Thus we are successfully tested the concurrent dual-band transmitter front-end for 2.4/5.2 GHz. The final complete layout also generated for concurrent dual-band receiver. The measurement remains left for future work.

Conclusion and Future scope

6.1 Summary and Conclusion of the Work Done

Rigorous design procedure for concurrent dual-band (2.4/5.2 GHz) wireless RF front-end presented. Initially the individual blocks like (Power combiner, filter, Antenna, LNA) have been designed. The design of power combiner is based on π-section to achieve dual-band characteristics, filter used based on coupled line theory with small geometrical modification that microstrip coupled line appear in zigzag form. The antenna is a printed monopole having dual-band return loss characteristics and implemented microstrip technology. The LNA designed here is concurrent dual band with active element with low noise transistor (p-HEMT). And integrate all designed and readymade blocks like (Mixer, PA, LO) for successful implementation of concurrent dual band transmitter and receiver.

6.2 Future scope

This system design is basically is a mixture of designed and readymade component. All readymade blocks are also designed and that makes the system smaller and efficient.

1. Design a power amplifier (PA) dual-band or wide-band and add to the system.
2. Design of active microwave mixer for the system and add to the system.
3. Design various local oscillators and add to the system.

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Fabrication & Testing

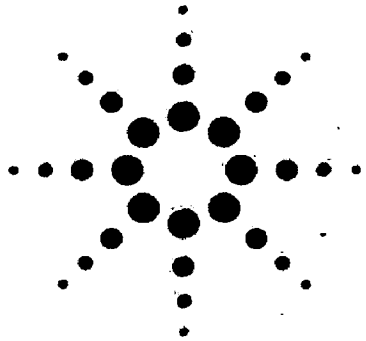
Fabrication

The Transmitter and Receiver have been fabricated and tested with the help of spectrum analyzer and network analyzer. The return loss of the antenna was measured with the HP 8720B Network Analyzer. The designed transmitter layout was fabricated on NH9338 substrate having ϵ_r =3.38 and 1.524 mm thickness (9 μm copper thickness, dissipation factor of 0.0025) using lithography techniques. While entire receiver was fabricated on NH9332 substrate having ϵ_r =3.2 and 1.524 mm thickness (15 μm copper thickness, dissipation factor of 0.0024). Lithography is typically the transfer of a layout pattern to a photosensitive material by selective exposure to a radiation source such as light. A photosensitive material is a material that experiences a change in its physical properties when exposed to a radiation source. If we selectively expose a photosensitive material to radiation (e.g. by masking some of the radiation) the pattern of the radiation on the material is transferred to the material exposed. In lithography, the photosensitive material used is typically a photo resist. When resist is exposed to a radiation source of a specific wavelength, the chemical resistance of the resist to developer solution changes. If the resist is placed in a developer solution after selective exposure to a light source, it will etch away one of the two regions (exposed or unexposed). If the exposed material is etched away by the developer and the unexposed region is resilient, the material is considered to be a positive resist. If the exposed material is resilient to the developer and the unexposed region is etched away, it is considered to be a negative resist. The photo resist used here was a negative resist.

Testing

After fabrication of the layout was completed, lumped components, supply wires and transistor were added to the matching section by soldering. For transceiver characteristics i.e. transmission / reception, we connect power supply and instrument like spectrum analyzer, signal generator. Single port calibration of the network analyzer was done before connecting the antenna. All measurement followed by printing the list values from the instrument of the measured results was taken which has been shown in form of graph in this report.

ATF 54143 BLKG transistor



Agilent ATF-54143 Low Noise Enhancement Mode Pseudomorphic HEMT in a Surface Mount Plastic Package

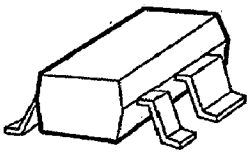
Data Sheet

Description

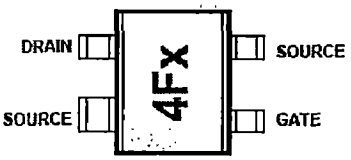
Agilent Technologies's ATF-54143 is a high dynamic range, low noise, E-PHEMT housed in a 4-lead SC-70 (SOT-343) surface mount plastic package.

The combination of high gain, high linearity and low noise makes the ATF-54143 ideal for cellular/PCS base stations, MMDS, and other systems in the 450 MHz to 6 GHz frequency range.

Surface Mount Package SOT-343



Pin Connections and Package Marking



Note:
Top View. Package marking provides orientation and identification

"4F" = Device Code
"x" = Date code character identifies month of manufacture.

Features

- High linearity performance
- Enhancement Mode Technology [1]
- Low noise figure
- Excellent uniformity in product specifications
- 800 micron gate width
- Low cost surface mount small plastic package SOT-343 (4 lead SC-70)
- Tape-and-Reel packaging option available

Specifications

2 GHz; 3 V, 60 mA (Typ.)

- 36.2 dBm output 3rd order intercept
- 20.4 dBm output power at 1 dB gain compression
- 0.5 dB noise figure
- 16.6 dB associated gain

Applications

- Low noise amplifier for cellular/ PCS base stations
- LNA for WLAN, WLL/RLL and MMDS applications
- General purpose discrete E-PHEMT for other ultra low noise applications

Note:

1. Enhancement mode technology requires positive Vgs, thereby eliminating the need for the negative gate voltage associated with conventional depletion mode devices.

Agilent Technologies

ATF-54143 Absolute Maximum Ratings[1]

Symbol	Parameter	Units	Absolute Maximum
V_{DS}	Drain - Source Voltage[2]	V	5
V_{GS}	Gate - Source Voltage[2]	V	-5 to 1
V_{GD}	Gate Drain Voltage[2]	V	5
I_{DS}	Drain Current[2]	mA	120
P_{diss}	Total Power Dissipation[3]	mW	360
$P_{in\ max}$	RF Input Power	dBm	10[5]
I_{GS}	Gate Source Current	mA	2[5]
T_{CH}	Channel Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150
θ_{jc}	Thermal Resistance[4]	°C/W	162

Notes:
1. Operation of this device in excess of any one of these parameters may cause permanent damage.
2. Assumes DC quiescent conditions.
3. Source lead temperature is 25°C. Derate 6 mW/°C for $T_L > 92°C$.
4. Thermal resistance measured using 150°C Liquid Crystal Measurement method.
5. The device can handle +10 dBm RF Input Power provided I_{GS} is limited to 2 mA. I_{GS} at P_{1dB} drive level is bias circuit dependent. See application section for additional information.

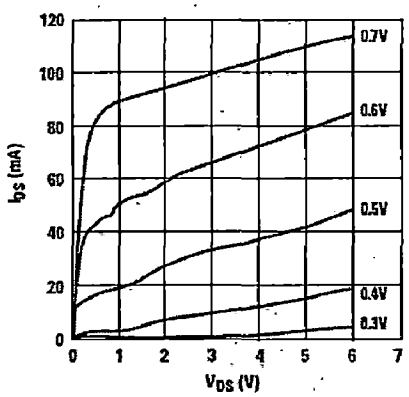


Figure 1. Typical I-V Curves.
(V_{GS} = 0.1 V per step)

Product Consistency Distribution Charts[6, 7]

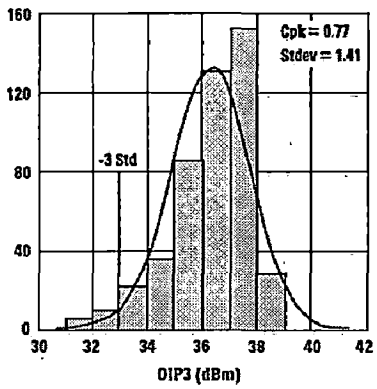


Figure 2. OIP3 @ 2 GHz, 3 V, 60 mA.
LSL = 33.0, Nominal = 36.575

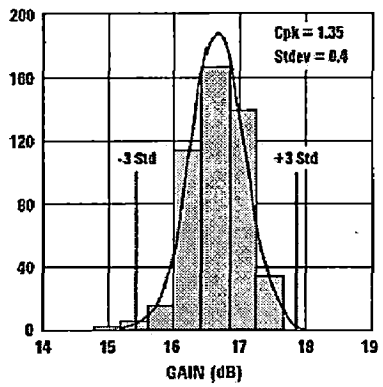


Figure 3. Gain @ 2 GHz, 3 V, 60 mA.
USL = 18.5, LSL = 15, Nominal = 16.6

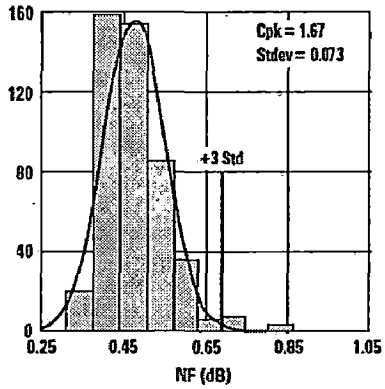


Figure 4. NF @ 2 GHz, 3 V, 60 mA.
USL = 0.9, Nominal = 0.49

Notes:
6. Distribution data sample size is 450 samples taken from 9 different wafers. Future wafers allocated to this product may have nominal values anywhere between the upper and lower limits.
7. Measurements made on production test board. This circuit represents a trade-off between an optimal noise match and a realizeable match based on production test equipment. Circut losses have been de-embeaded from actual measurements.

ATF-54143 Electrical Specifications
T_A = 25°C, RF parameters measured in a test circuit for a typical device

Symbol	Parameter and Test Condition			Units	Min.	Typ.[2]	Max.
Vgs	Operational Gate Voltage		Vds = 3V, Ids = 60 mA	V	0.4	0.59	0.75
Vth	Threshold Voltage		Vds = 3V, Ids = 4 mA	V	0.18	0.38	0.52
Idss	Saturated Drain Current		Vds = 3V, Vgs = 0V	µA	—	1	5
Gm	Transconductance		Vds = 3V, gm = ΔIdss/ΔVgs; ΔVgs = 0.75 - 0.7 = 0.05V	mmho	230	410	560
Igss	Gate Leakage Current		Vgd = Vgs = -3V	µA	—	—	200
NF	Noise Figure[1]	f = 2 GHz	Vds = 3V, Ids = 60 mA	dB	—	0.5	0.9
		f = 900 MHz	Vds = 3V, Ids = 60 mA	dB	—	0.3	—
Ga	Associated Gain[1]	f = 2 GHz	Vds = 3V, Ids = 60 mA	dB	15	16.6	18.5
		f = 900 MHz	Vds = 3V, Ids = 60 mA	dB	—	23.4	—
OIP3	Output 3rd Order Intercept Point[1]	f = 2 GHz	Vds = 3V, Ids = 60 mA	dBm	33	36.2	—
		f = 900 MHz	Vds = 3V, Ids = 60 mA	dBm	—	35.5	—
P1dB	1dB Compressed Output Power[1]	f = 2 GHz	Vds = 3V, Ids = 60 mA	dBm	—	20.4	—
		f = 900 MHz	Vds = 3V, Ids = 60 mA	dBm	—	18.4	—

Notes:
1. Measurements obtained using production test board described in Figure 5.
2. Typical values measured from a sample size of 450 parts from 9 wafers.

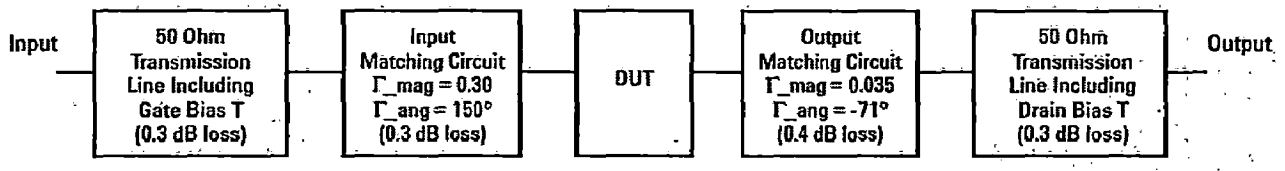


Figure 5. Block diagram of 2 GHz production test board used for Noise Figure, Associated Gain, P1dB, and OIP3 measurements. This circuit represents a trade-off between an optimal noise match and associated impedance matching circuit losses. Circuit losses have been de-embedded from actual measurements.

ATF-54143 Typical Performance Curves

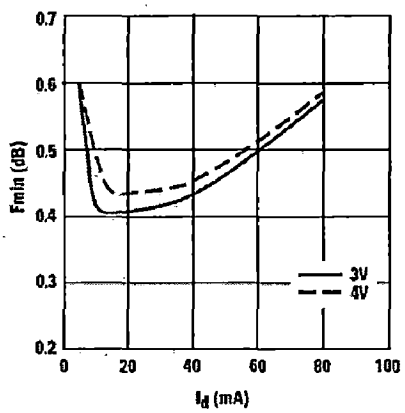


Figure 6. Fmin vs. I_{ds} and V_{ds} Tuned for Max OIP3 and Fmin at 2 GHz.

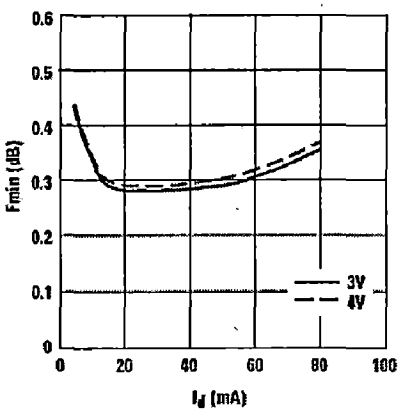


Figure 7. Fmin vs. I_{ds} and V_{ds} Tuned for Max OIP3 and Min NF at 900 MHz.

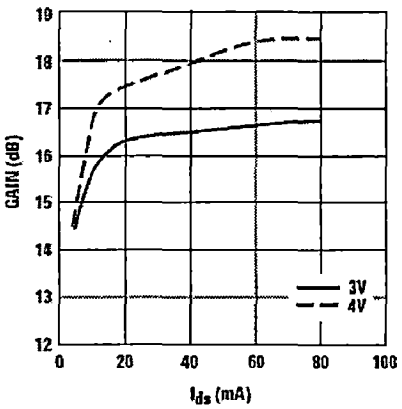


Figure 8. Gain vs. I_{ds} and V_{ds} Tuned for Max OIP3 and Fmin at 2 GHz.

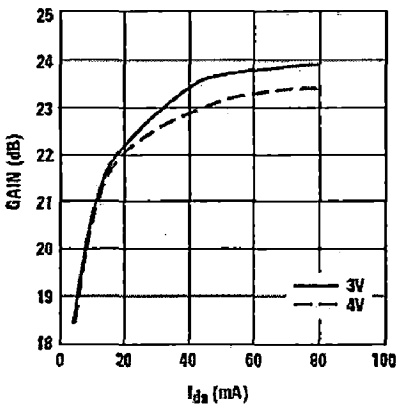


Figure 9. Gain vs. I_{ds} and V_{ds} Tuned for Max OIP3 and Fmin at 900 MHz.

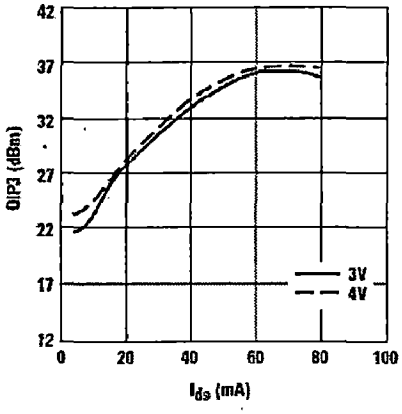


Figure 10. OIP3 vs. I_{ds} and V_{ds} Tuned for Max OIP3 and Fmin at 2 GHz.

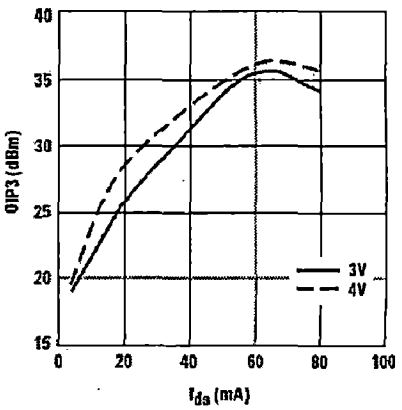


Figure 11. OIP3 vs. I_{ds} and V_{ds} Tuned for Max OIP3 and Fmin at 900 MHz.

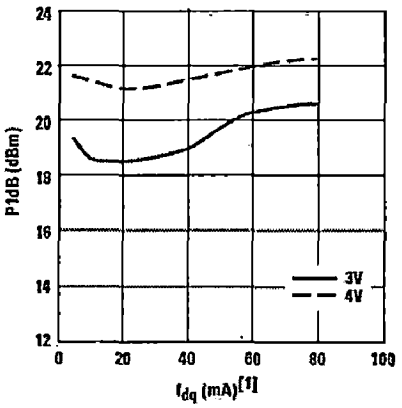


Figure 12. P1dB vs. I_{dq} and V_{ds} Tuned for Max OIP3 and Fmin at 2 GHz.

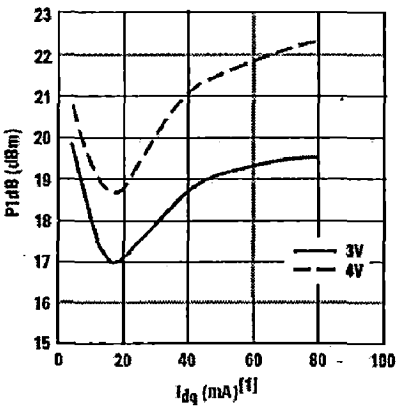


Figure 13. P1dB vs. I_{dq} and V_{ds} Tuned for Max OIP3 and Fmin at 900 MHz.

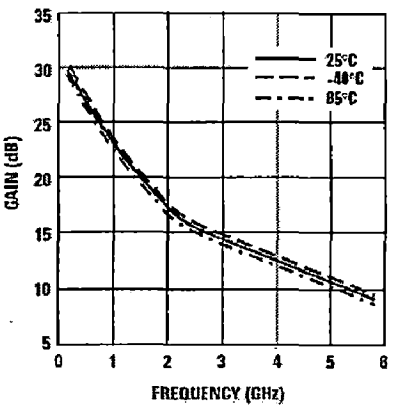


Figure 14. Gain vs. Frequency and Temp Tuned for Max OIP3 and Fmin at 3V, 60 mA.

Notes:

1. I_{dq} represents the quiescent drain current without RF drive applied. Under low values of I_{ds}, the application of RF drive will cause I_d to increase substantially as P1dB is approached.
2. Fmin values at 2 GHz and higher are based on measurements while the Fmins below 2 GHz have been extrapolated. The Fmin values are based on a set of 16 noise figure measurements made at 16 different impedances using an ATN NP5 test system. From these measurements a true Fmin is calculated. Refer to the noise parameter application section for more information.

ATF-54143 Typical Performance Curves, continued

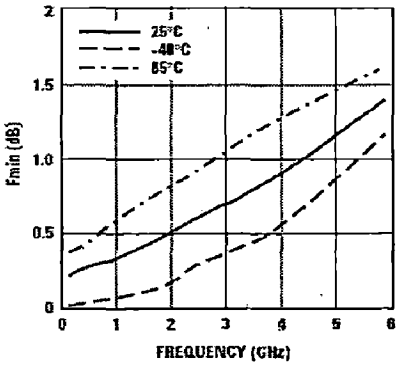


Figure 15. Fmin[2] vs. Frequency and Temp Tuned for Max OIP3 and Fmin at 3V, 60 mA.

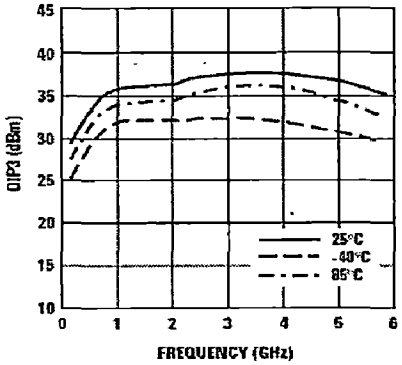


Figure 16. OIP3 vs. Frequency and Temp Tuned for Max OIP3 and Fmin at 3V, 60 mA.

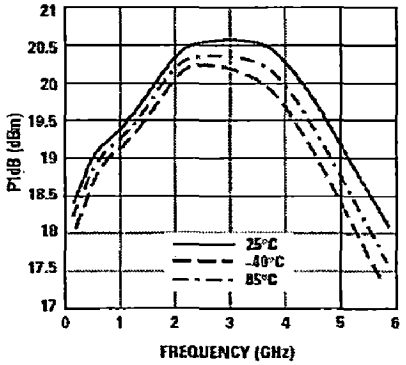


Figure 17. P1dB vs. Frequency and Temp Tuned for Max OIP3 and Fmin at 3V, 60 mA.

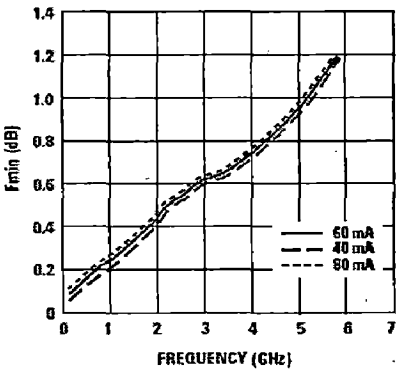


Figure 18. Fmin[1] vs. Frequency and I_{ds} at 3V.

ATF-54143 Reflection Coefficient Parameters tuned for Maximum Output IP3, V_{DS} = 3V, I_{DS} = 60 mA

Freq (GHz)	ΓOut_Mag.[1] (Mag)	ΓOut_Ang.[1] (Degrees)	OIP3 (dBm)	P1dB (dBm)
0.9	0.017	115	35.54	18.4
2.0	0.026	-85	36.23	20.38
3.9	0.013	173	37.54	20.28
5.8	0.025	102	35.75	18.09

Note:
1. Gamma out is the reflection coefficient of the matching circuit presented to the output of the device.

Note:
1. Fmin values at 2 GHz and higher are based on measurements while the Fmins below 2 GHz have been extrapolated. The Fmin values are based on a set of 16 noise figure measurements made at 16 different impedances using an ATN NP5 test system. From these measurements a true Fmin is calculated. Refer to the noise parameter application section for more information.

ATF-54143 Typical Scattering Parameters, V_{DS} = 3V, I_{DS} = 40 mA

Freq.	S_{11}		S_{21}			S_{12}		S_{22}		MSG/MAG
GHz	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	dB
0.1	0.99	-17.6	27.99	25.09	168.5	0.009	80.2	0.59	-12.8	34.45
0.5	0.83	-76.9	25.47	18.77	130.1	0.036	52.4	0.44	-54.6	27.17
0.9	0.72	-114	22.52	13.37	108	0.047	40.4	0.33	-78.7	24.54
1.0	0.70	-120.6	21.86	12.39	103.9	0.049	38.7	0.31	-83.2	24.03
1.5	0.65	-146.5	19.09	9.01	87.4	0.057	33.3	0.24	-99.5	21.99
1.9	0.63	-162.1	17.38	7.40	76.6	0.063	30.4	0.20	-108.6	20.70
2.0	0.62	-165.6	17.00	7.08	74.2	0.065	29.8	0.19	-110.9	20.37
2.5	0.61	178.5	15.33	5.84	62.6	0.072	26.6	0.15	-122.6	19.09
3.0	0.61	164.2	13.91	4.96	51.5	0.080	22.9	0.12	-137.5	17.92
4.0	0.63	138.4	11.59	3.80	31	0.094	14	0.10	176.5	16.06
5.0	0.66	116.5	9.65	3.04	11.6	0.106	4.2	0.14	138.4	14.57
6.0	0.69	97.9	8.01	2.51	-6.7	0.118	-6.1	0.17	117.6	13.28
7.0	0.71	80.8	6.64	2.15	-24.5	0.128	-17.6	0.20	98.6	12.25
8.0	0.72	62.6	5.38	1.86	-42.5	0.134	-29.3	0.22	73.4	11.42
9.0	0.76	45.2	4.20	1.62	-60.8	0.145	-40.6	0.27	52.8	10.48
10.0	0.83	28.2	2.84	1.39	-79.8	0.150	-56.1	0.37	38.3	9.66
11.0	0.85	13.9	1.42	1.18	-96.9	0.149	-69.3	0.45	25.8	8.98
12.0	0.88	-0.5	0.23	1.03	-112.4	0.150	-81.6	0.51	12.7	8.35
13.0	0.89	-15.1	-0.86	0.91	-129.7	0.149	-95.7	0.54	-4.1	7.84
14.0	0.87	-31.6	-2.18	0.78	-148	0.143	-110.3	0.61	-20.1	7.36
15.0	0.88	-46.1	-3.85	0.64	-164.8	0.132	-124	0.65	-34.9	6.87
16.0	0.87	-54.8	-5.61	0.52	-178.4	0.121	-134.6	0.70	-45.6	6.37
17.0	0.87	-62.8	-7.09	0.44	170.1	0.116	-144.1	0.73	-55.9	5.81
18.0	0.92	-73.6	-8.34	0.38	156.1	0.109	-157.4	0.76	-68.7	5.46

Typical Noise Parameters, V_{DS} = 3V, I_{DS} = 40 mA

Freq	F_{min}	Γ_{opt}	Γ_{opt}	$R_{n/50}$	G_a
GHz	dB	Mag.	Ang.		dB
0.5	0.17	0.34	34.80	0.04	27.83
0.9	0.22	0.32	53.00	0.04	23.57
1.0	0.24	0.32	60.50	0.04	22.93
1.9	0.42	0.29	108.10	0.04	18.35
2.0	0.45	0.29	111.10	0.04	17.91
2.4	0.51	0.30	136.00	0.04	16.39
3.0	0.59	0.32	169.90	0.05	15.40
3.9	0.69	0.34	-151.60	0.05	13.26
5.0	0.90	0.45	-119.50	0.09	11.89
5.8	1.14	0.50	-101.60	0.16	10.95
6.0	1.17	0.52	-99.60	0.18	10.64
7.0	1.24	0.58	-79.50	0.33	9.61
8.0	1.57	0.60	-57.90	0.56	8.36
9.0	1.64	0.69	-39.70	0.87	7.77
10.0	1.8	0.80	-22.20	1.34	7.68

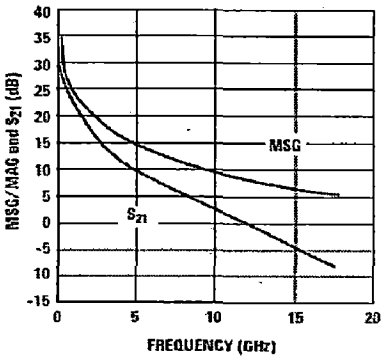


Figure 19. MSG/MAG and $|S_{21}|^2$ vs. Frequency at 3V, 40 mA.

Notes:

1. F_{min} values at 2 GHz and higher are based on measurements while the F_{mins} below 2 GHz have been extrapolated. The F_{min} values are based on a set of 16 noise figure measurements made at 16 different impedances using an ATN NP5 test system. From these measurements a true F_{min} is calculated. Refer to the noise parameter application section for more information.
2. S and noise parameters are measured on a microstrip line made on 0.025 inch thick alumina carrier. The input reference plane is at the end of the gate lead. The output reference plane is at the end of the drain lead. The parameters include the effect of four plated through via holes connecting source landing pads on top of the test carrier to the microstrip ground plane on the bottom side of the carrier. Two 0.020 inch diameter via holes are placed within 0.010 inch from each source lead contact point, one via on each side of that point.

ATF-54143 Typical Scattering Parameters, V_{DS} = 3V, I_{DS} = 60 mA

Freq.	S_{11}			S_{21}		S_{12}		S_{22}		MSG/MAG
GHz	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	dB
0.1	0.99	-18.9	28.84	27.66	167.6	0.01	80.0	0.54	-14.0	34.88
0.5	0.81	-80.8	26.04	20.05	128.0	0.03	52.4	0.40	-58.8	27.84
0.9	0.71	-117.9	22.93	14.01	106.2	0.04	41.8	0.29	-83.8	25.13
1.0	0.69	-124.4	22.24	12.94	102.2	0.05	40.4	0.27	-88.5	24.59
1.5	0.64	-149.8	19.40	9.34	86.1	0.05	36.1	0.21	-105.2	22.46
1.9	0.62	-164.9	17.66	7.64	75.6	0.06	33.8	0.17	-114.7	21.05
2.0	0.62	-168.3	17.28	7.31	73.3	0.06	33.3	0.17	-117.0	20.71
2.5	0.60	176.2	15.58	6.01	61.8	0.07	30.1	0.13	-129.7	19.34
3.0	0.60	162.3	14.15	5.10	51.0	0.08	26.5	0.11	-146.5	18.15
4.0	0.62	137.1	11.81	3.90	30.8	0.09	17.1	0.10	165.2	16.17
5.0	0.66	115.5	9.87	3.11	11.7	0.11	6.8	0.14	131.5	14.64
6.0	0.69	97.2	8.22	2.58	-6.4	0.12	-3.9	0.18	112.4	13.36
7.0	0.70	80.2	6.85	2.20	-24.0	0.13	-15.8	0.20	94.3	12.29
8.0	0.72	62.2	5.58	1.90	-41.8	0.14	-28.0	0.23	70.1	11.45
9.0	0.76	45.0	4.40	1.66	-59.9	0.15	-39.6	0.29	50.6	10.53
10.0	0.83	28.4	3.06	1.42	-78.7	0.15	-55.1	0.38	36.8	9.71
11.0	0.85	13.9	1.60	1.20	-95.8	0.15	-68.6	0.46	24.4	9.04
12.0	0.88	-0.2	0.43	1.05	-111.1	0.15	-80.9	0.51	11.3	8.43
13.0	0.89	-14.6	-0.65	0.93	-128.0	0.15	-94.9	0.55	-5.2	7.94
14.0	0.88	-30.6	-1.98	0.80	-146.1	0.14	-109.3	0.61	-20.8	7.43
15.0	0.88	-45.0	-3.62	0.66	-162.7	0.13	-122.9	0.66	-35.0	6.98
16.0	0.88	-54.5	-5.37	0.54	-176.6	0.12	-133.7	0.70	-45.8	6.49
17.0	0.88	-62.5	-6.83	0.46	171.9	0.12	-143.2	0.73	-56.1	5.95
18.0	0.92	-73.4	-8.01	0.40	157.9	0.11	-156.3	0.76	-68.4	5.66

Typical Noise Parameters, V_{DS} = 3V, I_{DS} = 60 mA

Freq	F_{min}	Γ_{opt}	Γ_{opt}	$R_{n/50}$	G_a
GHz	dB	Mag.	Ang.		dB
0.5	0.15	0.34	42.3	0.04	28.50
0.9	0.20	0.32	62.8	0.04	24.18
1.0	0.22	0.32	67.6	0.04	23.47
1.9	0.42	0.27	116.3	0.04	18.67
2.0	0.45	0.27	120.1	0.04	18.29
2.4	0.52	0.26	145.8	0.04	16.65
3.0	0.59	0.29	178.0	0.05	15.56
3.9	0.70	0.36	-145.4	0.05	13.53
5.0	0.93	0.47	-116.0	0.10	12.13
5.8	1.16	0.52	-98.9	0.18	11.10
6.0	1.19	0.55	-96.5	0.20	10.95
7.0	1.26	0.60	-77.1	0.37	9.73
8.0	1.63	0.62	-56.1	0.62	8.56
9.0	1.69	0.70	-38.5	0.95	7.97
10.0	1.73	0.79	-21.5	1.45	7.76

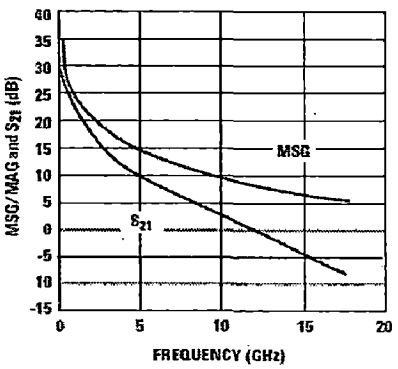


Figure 20. MSG/MAG and $|S_{21}|^2$ vs. Frequency at 3V, 60 mA.

Notes:

1. F_{min} values at 2 GHz and higher are based on measurements while the F_{mins} below 2 GHz have been extrapolated. The F_{min} values are based on a set of 16 noise figure measurements made at 16 different impedances using an ATN NP5 test system. From these measurements a true F_{min} is calculated. Refer to the noise parameter application section for more information.
2. S and noise parameters are measured on a microstrip line made on 0.025 inch thick alumina carrier. The input reference plane is at the end of the gate lead. The output reference plane is at the end of the drain lead. The parameters include the effect of four plated through via holes connecting source landing pads on top of the test carrier to the microstrip ground plane on the bottom side of the carrier. Two 0.020 inch diameter via holes are placed within 0.010 inch from each source lead contact point, one via on each side of that point.

ATF-54143 Typical Scattering Parameters, V_{DS} = 3V, I_{DS} = 80 mA

Freq.	S_{11}			S_{21}		S_{12}		S_{22}		MSG/MAG
GHz	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	dB
0.1	0.98	-20.4	28.32	26.05	167.1	0.01	79.4	0.26	-27.6	34.16
0.5	0.80	-86.9	25.32	18.45	126.8	0.04	53.3	0.29	-104.9	27.10
0.9	0.72	-123.4	22.10	12.73	105.2	0.05	43.9	0.30	-138.8	24.15
1.0	0.70	-129.9	21.40	11.75	101.3	0.05	42.7	0.30	-144.3	23.63
1.5	0.66	-154.6	18.55	8.46	85.4	0.06	38.6	0.30	-165.0	21.35
1.9	0.65	-169.5	16.81	6.92	74.9	0.07	35.7	0.29	-177.6	19.89
2.0	0.64	-172.8	16.42	6.62	72.6	0.07	35.0	0.29	179.4	19.52
2.5	0.64	172.1	14.69	5.42	61.1	0.09	30.6	0.29	164.4	18.05
3.0	0.63	158.5	13.24	4.59	50.1	0.10	25.5	0.29	150.2	16.80
4.0	0.66	133.8	10.81	3.47	29.9	0.12	13.4	0.33	126.1	14.76
5.0	0.69	112.5	8.74	2.74	11.1	0.13	1.2	0.39	107.8	13.20
6.0	0.72	94.3	7.03	2.25	-6.5	0.14	-11.3	0.42	91.8	11.96
7.0	0.73	77.4	5.63	1.91	-23.5	0.15	-24.5	0.44	75.5	10.97
8.0	0.74	59.4	4.26	1.63	-41.1	0.16	-38.1	0.47	55.5	10.14
9.0	0.78	42.1	2.98	1.41	-58.7	0.17	-51.1	0.52	37.8	9.32
10.0	0.84	25.6	1.51	1.19	-76.4	0.16	-66.8	0.59	24.0	8.60
11.0	0.86	11.4	0.00	1.00	-92.0	0.16	-79.8	0.64	11.8	8.04
12.0	0.88	-2.6	-1.15	0.88	-105.9	0.16	-91.7	0.68	-0.8	7.52
13.0	0.89	-17.0	-2.18	0.78	-121.7	0.15	-105.6	0.70	-16.7	7.12
14.0	0.87	-33.3	-3.48	0.67	-138.7	0.14	-119.5	0.73	-31.7	6.77
15.0	0.87	-47.3	-5.02	0.56	-153.9	0.13	-132.3	0.76	-44.9	6.42
16.0	0.86	-55.6	-6.65	0.47	-165.9	0.12	-141.7	0.78	-54.9	5.99
17.0	0.86	-63.4	-7.92	0.40	-175.9	0.11	-150.4	0.79	-64.2	5.55
18.0	0.91	-74.2	-8.92	0.36	171.2	0.10	-163.0	0.81	-76.2	5.37

Typical Noise Parameters, V_{DS} = 3V, I_{DS} = 80 mA

Freq	F_{min}	Γ_{opt}	Γ_{opt}	$R_{n/50}$	G_a
GHz	dB	Mag.	Ang.		dB
0.5	0.19	0.23	66.9	0.04	27.93
0.9	0.24	0.24	84.3	0.04	24.13
1.0	0.25	0.25	87.3	0.04	23.30
1.9	0.43	0.28	134.8	0.04	18.55
2.0	0.42	0.29	138.8	0.04	18.15
2.4	0.51	0.30	159.5	0.03	16.44
3.0	0.61	0.35	-173	0.03	15.13
3.9	0.70	0.41	-141.6	0.06	12.97
5.0	0.94	0.52	-113.5	0.13	11.42
5.8	1.20	0.56	-97.1	0.23	10.48
6.0	1.26	0.58	-94.8	0.26	10.11
7.0	1.34	0.62	-75.8	0.46	8.86
8.0	1.74	0.63	-55.5	0.76	7.59
9.0	1.82	0.71	-37.7	1.17	6.97
10.0	1.94	0.79	-20.8	1.74	6.65

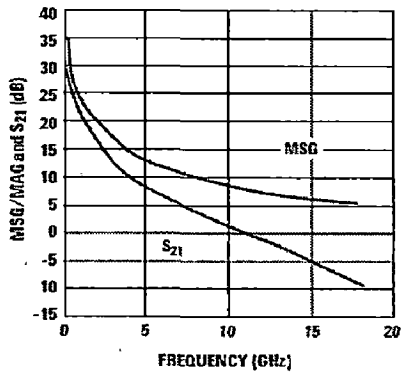


Figure 21. MSG/MAG and $|S_{21}|^2$ vs. Frequency at 3V, 80 mA.

Notes:

1. F_{min} values at 2 GHz and higher are based on measurements while the F_{mins} below 2 GHz have been extrapolated. The F_{min} values are based on a set of 16 noise figure measurements made at 16 different impedances using an ATN NP5 test system. From these measurements a true F_{min} is calculated. Refer to the noise parameter application section for more information.
2. S and noise parameters are measured on a microstrip line made on 0.025 inch thick alumina carrier. The input reference plane is at the end of the gate lead. The output reference plane is at the end of the drain lead. The parameters include the effect of four plated through via holes connecting source landing pads on top of the test carrier to the microstrip ground plane on the bottom side of the carrier. Two 0.020 inch diameter via holes are placed within 0.010 inch from each source lead contact point, one via on each side of that point.

ATF-54143 Typical Scattering Parameters, V_{DS} = 4V, I_{DS} = 60 mA

Freq.	S_{11}		S_{21}			S_{12}		S_{22}		MSG/MAG
GHz	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	dB
0.1	0.99	-18.6	28.88	27.80	167.8	0.01	80.1	0.58	-12.6	35.41
0.5	0.81	-80.2	26.11	20.22	128.3	0.03	52.4	0.42	-52.3	28.14
0.9	0.71	-117.3	23.01	14.15	106.4	0.04	41.7	0.31	-73.3	25.38
1.0	0.69	-123.8	22.33	13.07	102.4	0.04	40.2	0.29	-76.9	24.83
1.5	0.64	-149.2	19.49	9.43	86.2	0.05	36.1	0.22	-89.4	22.75
1.9	0.62	-164.5	17.75	7.72	75.7	0.06	34.0	0.18	-95.5	21.32
2.0	0.61	-167.8	17.36	7.38	73.3	0.06	33.5	0.18	-97.0	21.04
2.5	0.60	176.6	15.66	6.07	61.9	0.07	30.7	0.14	-104.0	19.64
3.0	0.60	162.6	14.23	5.15	51.1	0.07	27.3	0.11	-113.4	18.48
4.0	0.62	137.4	11.91	3.94	30.9	0.09	18.7	0.07	-154.7	16.46
5.0	0.65	115.9	10.00	3.16	11.7	0.10	9.0	0.09	152.5	14.96
6.0	0.68	97.6	8.36	2.62	-6.6	0.11	-1.4	0.12	127.9	13.61
7.0	0.70	80.6	7.01	2.24	-24.3	0.12	-12.9	0.15	106.9	12.57
8.0	0.72	62.6	5.76	1.94	-42.3	0.13	-24.7	0.17	78.9	11.67
9.0	0.76	45.4	4.60	1.70	-60.5	0.14	-36.1	0.23	56.8	10.72
10.0	0.83	28.5	3.28	1.46	-79.6	0.15	-51.8	0.32	42.1	9.88
11.0	0.86	14.1	1.87	1.24	-97.0	0.15	-65.4	0.41	29.4	9.17
12.0	0.88	-0.4	0.69	1.08	-112.8	0.15	-78.0	0.47	16.0	8.53
13.0	0.90	-14.9	-0.39	0.96	-130.2	0.15	-92.2	0.51	-1.1	7.99
14.0	0.87	-31.4	-1.72	0.82	-148.8	0.15	-107.3	0.58	-17.6	7.46
15.0	0.88	-46.0	-3.38	0.68	-166.0	0.14	-121.2	0.63	-32.6	6.97
16.0	0.88	-54.8	-5.17	0.55	179.8	0.13	-132.2	0.69	-43.7	6.41
17.0	0.87	-62.8	-6.73	0.46	168.4	0.12	-142.3	0.72	-54.2	5.85
18.0	0.92	-73.7	-7.93	0.40	154.3	0.11	-155.6	0.75	-67.2	5.54

Typical Noise Parameters, V_{DS} = 4V, I_{DS} = 60 mA

Freq	F_{min}	Γ_{opt}	Γ_{opt}	$R_{n/50}$	G_a
GHz	dB	Mag.	Ang.		dB
0.5	0.17	0.33	34.30	0.03	28.02
0.9	0.25	0.31	60.30	0.04	24.12
1.0	0.27	0.31	68.10	0.04	23.43
1.9	0.45	0.27	115.00	0.04	18.72
2.0	0.49	0.27	119.80	0.04	18.35
2.4	0.56	0.26	143.50	0.04	16.71
3.0	0.63	0.28	176.80	0.04	15.58
3.9	0.73	0.35	-145.90	0.05	13.62
5.0	0.96	0.47	-116.20	0.11	12.25
5.8	1.20	0.52	-98.80	0.19	11.23
6.0	1.23	0.54	-96.90	0.21	11.02
7.0	1.33	0.60	-77.40	0.38	9.94
8.0	1.66	0.63	-56.20	0.64	8.81
9.0	1.71	0.71	-38.60	0.99	8.22
10.0	1.85	0.82	-21.30	1.51	8.12

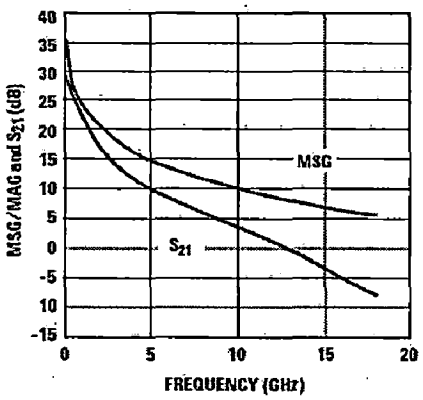


Figure 22. MSG/MAG and $|S_{21}|^2$ vs. Frequency at 4V, 60 mA.

Notes:

1. F_{min} values at 2 GHz and higher are based on measurements while the F_{min}s below 2 GHz have been extrapolated. The F_{min} values are based on a set of 16 noise figure measurements made at 16 different impedances using an ATN NP5 test system. From these measurements a true F_{min} is calculated. Refer to the noise parameter application section for more information.
2. S and noise parameters are measured on a microstrip line made on 0.025 inch thick alumina carrier. The input reference plane is at the end of the gate lead. The output reference plane is at the end of the drain lead. The parameters include the effect of four plated through via holes connecting source landing pads on top of the test carrier to the microstrip ground plane on the bottom side of the carrier. Two 0.020 inch diameter via holes are placed within 0.010 inch from each source lead contact point, one via on each side of that point.

ATF-54143 Applications Information

Introduction

Agilent Technologies's ATF-54143 is a low noise enhancement mode PHEMT designed for use in low cost commercial applications in the VHF through 6 GHz frequency range. As opposed to a typical depletion mode PHEMT where the gate must be made negative with respect to the source for proper operation, an enhancement mode PHEMT requires that the gate be made more positive than the source for normal operation. Therefore a negative power supply voltage is not required for an enhancement mode device. Biasing an enhancement mode PHEMT is much like biasing the typical bipolar junction transistor. Instead of a 0.7V base to emitter voltage, the ATF-54143 enhancement mode PHEMT requires about a 0.6V potential between the gate and source for a nominal drain current of 60 mA.

Matching Networks

The techniques for impedance matching an enhancement mode device are very similar to those for matching a depletion mode device. The only difference is in the method of supplying gate bias. S and Noise Parameters for various bias conditions are listed in this data sheet. The circuit shown in Figure 1 shows a typical LNA circuit normally used for 900 and 1900 MHz applications (Consult the Agilent Technologies website for application notes covering specific applications). High pass impedance matching networks consisting of L1/C1 and L4/C4 provide the appropriate match for noise figure, gain, S11 and S22. The high pass structure also provides low frequency gain reduction which can be beneficial from the standpoint of improving out-of-band rejection at lower frequencies.

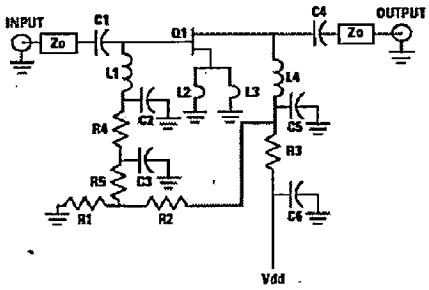


Figure 1. Typical ATF-54143 LNA with Passive Biasing.

Capacitors C2 and C5 provide a low impedance in-band RF bypass for the matching networks. Resistors R3 and R4 provide a very important low frequency termination for the device. The resistive termination improves low frequency stability. Capacitors C3 and C6 provide the low frequency RF bypass for resistors R3 and R4. Their value should be chosen carefully as C3 and C6 also provide a termination for low frequency mixing products. These mixing products are as a result of two or more in-band signals mixing and producing third order in-band distortion products. The low frequency or difference mixing products are bypassed by C3 and C6. For best suppression of third order distortion products based on the CDMA 1.25 MHz signal spacing, C3 and C6 should be 0.1 µF in value. Smaller values of capacitance will not suppress the generation of the 1.25 MHz difference signal and as a result will show up as poorer two tone IP3 results.

Bias Networks

One of the major advantages of the enhancement mode technology is that it allows the designer to be able to dc ground the source leads and then merely apply a positive voltage on the gate to set the desired amount of quiescent drain current I_d.

Whereas a depletion mode PHEMT pulls maximum drain current when $V_{gs} = 0V$, an enhancement mode PHEMT pulls only a small amount of leakage current when $V_{gs} = 0V$. Only when V_{gs} is increased above V_{to}, the device threshold voltage, will drain current start to flow. At a V_{ds} of 3V and a nominal V_{gs} of 0.6V, the drain current I_d will be approximately 60 mA. The data sheet suggests a minimum and maximum V_{gs} over which the desired amount of drain current will be achieved. It is also important to note that if the gate terminal is left open circuited, the device will pull some amount of drain current due to leakage current creating a voltage differential between the gate and source terminals.

Passive Biasing

Passive biasing of the ATF-54143 is accomplished by the use of a voltage divider consisting of R1 and R2. The voltage for the divider is derived from the drain voltage which provides a form of voltage feedback through the use of R3 to help keep drain current constant. Resistor R5 (approximately 10kΩ) provides current limiting for the gate of enhancement mode devices such as the ATF-54143. This is especially important when the device is driven to P_{1dB} or P_{SAT}.

Resistor R3 is calculated based on desired V_{ds}, I_{ds} and available power supply voltage.

$$R3 = \frac{V_{DD} - V_{ds}}{I_{ds} + I_{BB}} \quad (1)$$

V_{DD} is the power supply voltage.
V_{ds} is the device drain to source voltage.
I_{ds} is the desired drain current.
I_{BB} is the current flowing through the R1/R2 resistor voltage divider network.

The values of resistors R1 and R2 are calculated with the following formulas

$$R1 = \frac{V_{gs}}{I_{BB}} \quad (2)$$

$$R2 = \frac{(V_{ds} - V_{gs})\,R1}{V_{gs}} \quad (3)$$

Example Circuit

$V_{DD} = 5V$
$V_{ds} = 3V$
$I_{ds} = 60$ mA
$V_{gs} = 0.59V$

Choose I_{BB} to be at least 10X the normal expected gate leakage current. I_{BB} was chosen to be 2 mA for this example. Using equations (1), (2), and (3) the resistors are calculated as follows

R1 = 295Ω
R2 = 1205Ω
R3 = 32.3Ω

Active Biasing

Active biasing provides a means of keeping the quiescent bias point constant over temperature and constant over lot to lot variations in device dc performance. The advantage of the active biasing of an enhancement mode PHEMT versus a depletion mode PHEMT is that a negative power source is not required. The techniques of active biasing an enhancement mode device are very similar to those used to bias a bipolar junction transistor.

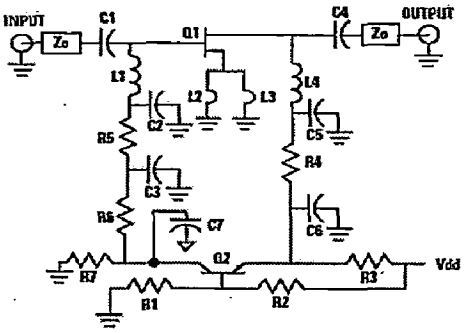


Figure 2. Typical ATF-54143 LNA with Active Biasing.

An active bias scheme is shown in Figure 2. R1 and R2 provide a constant voltage source at the base of a PNP transistor at Q2. The constant voltage at the base of Q2 is raised by 0.7 volts at the emitter, The constant emitter voltage plus the regulated V_{DD} supply are present across resistor R3. Constant voltage across R3 provides a constant current supply for the drain current. Resistors R1 and R2 are used to set the desired Vds. The combined series value of these resistors also sets the amount of extra current consumed by the bias network. The equations that describe the circuit's operation are as follows.

$$V_E = V_{ds} + (I_{ds} \cdot R4) \quad (1)$$

$$R3 = \frac{V_{DD} - V_E}{I_{ds}} \quad (2)$$

$$V_B = V_E - V_{BE} \quad (3)$$

$$V_B = \frac{R1}{R1 + R2} V_{DD} \quad (4)$$

$$V_{DD} = I_{BB}\,(R1 + R2) \quad (5)$$

Rearranging equation (4) provides the following formula

$$R2 = \frac{R_1\,(V_{DD} - V_B)}{V_B} \quad (4A)$$

and rearranging equation (5) provides the following formula

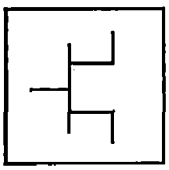
$$R1 = \frac{V_{DD}}{I_{BB}\left(1 + \frac{V_{DD} - V_B}{V_B}\right)} \quad (5A)$$

Example Circuit

$V_{DD} = 5V$
$V_{ds} = 3V$
$I_{ds} = 60$ mA
R4 = 10Ω
$V_{BE} = 0.7V$

Equation (1) calculates the required voltage at the emitter of the PNP transistor based on desired V_{ds} and I_{ds} through resistor R4 to be 3.6V. Equation (2) calculates the value of resistor R3 which determines the drain current I_{ds}. In the example R3=23.3Ω. Equation (3) calculates the voltage required at the junction of resistors R1 and R2. This voltage plus the step-up of the base emitter junction determines the regulated V_{ds}. Equations (4) and (5) are solved simultaneously to determine the value of resistors R1 and R2. In the example R1=1450Ω and R2=1050Ω. R7 is chosen to be 1kΩ. This resistor keeps a small amount of current flowing through Q2 to help maintain bias stability. R6 is chosen to be 10kΩ. This value of resistance is necessary to limit Q1 gate current in the presence of high RF drive level (especially when Q1 is driven to P_{1dB} gain compression point).

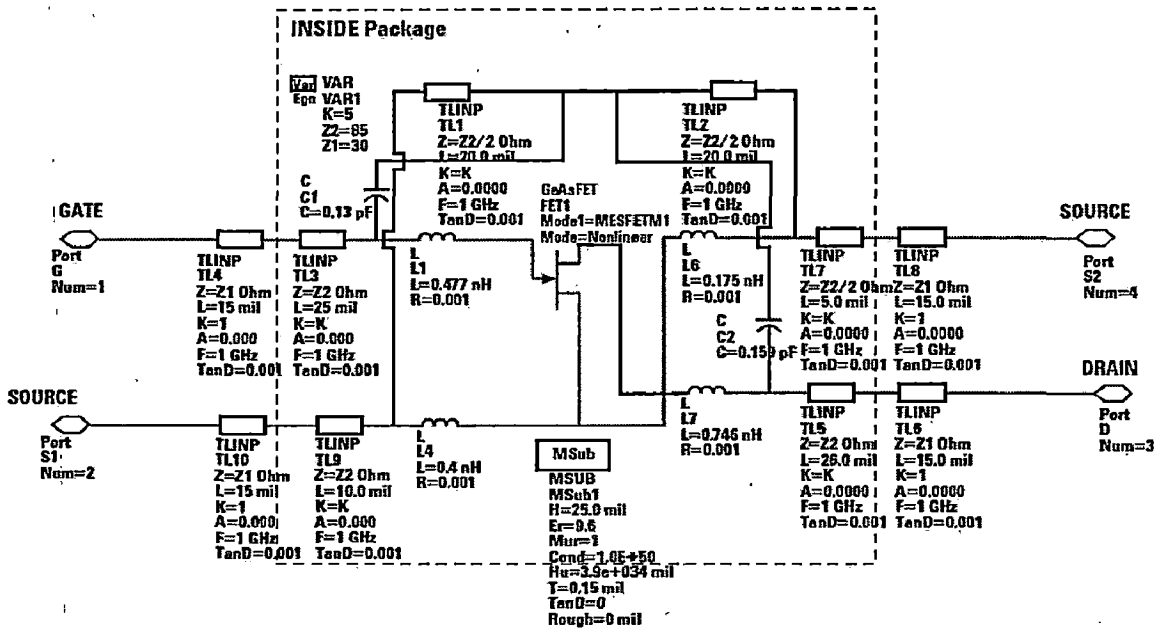
ATF-54143 Die Model



Advanced_Curtice2_Model
MESFETM1

NFET=yes	Rf=	Crf=0.1 F	N=
PFET=no	Gscap=2	Gsfwd=	Fnc=1 MHz
Vto=0.3	Cgs=1.73 pF	Gsrev=	R=0.08
Beta=0.9	Cgd=0.255 pF	Gdfwd=	P=0.2
Lambda=82e-3	Gdcap=2	Gdrev=	C=0.1
Alpha=13	Fc=0.65	R1=	Taumdl=no
Tau=	Rgd=0.25 Ohm	R2=	wVgfwd=
Tnom=16.85	Rd=1.0125 Ohm	Vbi=0.8	wBvgs=
Idstc=	Rg=1.0 Ohm	Vbr=	wBvgd=
Ucrit=-0.72	Rs=0.3375 Ohm	Vjr=	wBvds=
Vgexp=1.91	Ld=	Is=	wIdsmax=
Gamds=1e-4	Lg=0.18 nH	Ir=	wPmax=
Vtotc=	Ls=	Imax=	AllParams=
Betatce=	Cds=0.27 pF	Xti=	
Rgs=0.25 Ohm	Rc=250 Ohm	Eg=	

ATF-54143 curtice ADS Model



Designing with S and Noise Parameters and the Non-Linear Model

The non-linear model describing the ATF-54143 includes both the die and associated package model. The package model includes the effect of the pins but does not include the effect of the additional source inductance associated with grounding the source leads through the printed circuit board. The device S and Noise Parameters do include the effect of 0.020 inch thickness printed circuit board vias. When comparing simulation results between the measured S parameters and the simulated non-linear model, be sure to include the effect of the printed circuit board to get an accurate comparison. This is shown schematically in Figure 3.

For Further Information

The information presented here is an introduction to the use of the ATF-54143 enhancement mode PHEMT. More detailed application circuit information is available from Agilent Technologies. Consult the web page or your local Agilent Technologies sales representative.

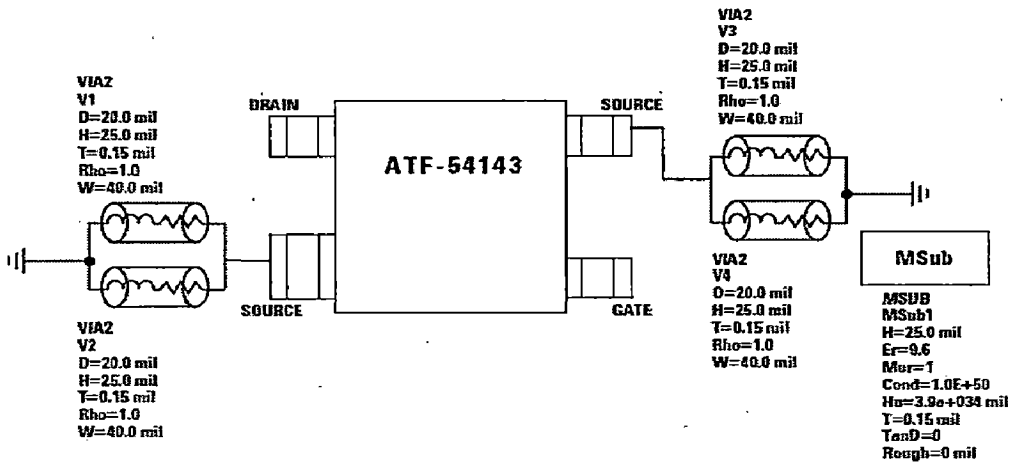


Figure 3. Adding Vias to the ATF-54143 Non-Linear Model for Comparison to Measured S and Noise Parameters.

Noise Parameter Applications Information

F_{min} values at 2 GHz and higher are based on measurements while the F_{mins} below 2 GHz have been extrapolated. The F_{min} values are based on a set of 16 noise figure measurements made at 16 different impedances using an ATN NP5 test system. From these measurements, a true F_{min} is calculated. F_{min} represents the true minimum noise figure of the device when the device is presented with an impedance matching network that transforms the source impedance, typically 50Ω, to an impedance represented by the reflection coefficient G_o. The designer must design a matching network that will present G_o to the device with minimal associated circuit losses. The noise figure of the completed amplifier is equal to the noise figure of the device plus the losses of the matching network preceding the device. The noise figure of the device is equal to F_{min} only when the device is presented with G_o. If the reflection coefficient of the matching network is other than G_o, then the noise figure of the device will be greater than F_{min} based on the following equation.

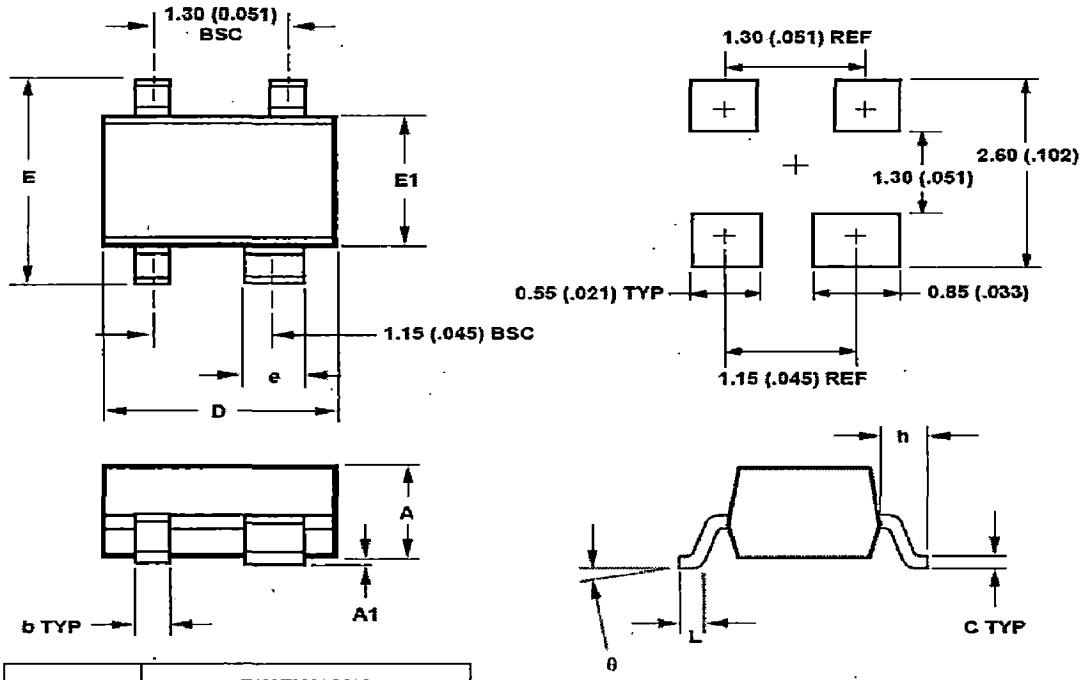
$$NF = F_{min} + \frac{4\,R_n}{Zo}\,\frac{|\Gamma_s - \Gamma_o|^2}{(|1+\Gamma_o|^2)(1-|\Gamma_s|^2)}$$

Where R_n/Z_o is the normalized noise resistance, Γ_o is the optimum reflection coefficient required to produce F_{min} and Γ_s is the reflection coefficient of the source impedance actually presented to the device. The losses of the matching networks are non-zero and they will also add to the noise figure of the device creating a higher amplifier noise figure. The losses of the matching networks are related to the Q of the components and associated printed circuit board loss. Γ_o is typically fairly low at higher frequencies and increases as frequency is lowered. Larger gate width devices will typically have a lower Γ_o as compared to narrower gate width devices. Typically for FETs, the higher Γ_o usually infers that an impedance much higher than 50Ω is required for the device to produce F_{min}. At VHF frequencies and even lower L Band frequencies, the required impedance can be in the vicinity of several thousand ohms. Matching to such a high impedance requires very hi-Q components in order to minimize circuit losses. As an example at 900 MHz, when airwwound coils (Q > 100) are used for matching networks, the loss can still be up to 0.25 dB which will add directly to the noise figure of the device. Using muiltilayer molded inductors with Qs in the 30 to 50 range results in additional loss over the airwound coil. Losses as high as 0.5 dB or greater add to the typical 0.15 dB F_{min} of the device creating an amplifier noise figure of nearly 0.65 dB. A discussion concerning calculated and measured circuit losses and their effect on amplifier noise figure is covered in Agilent Application 1085.

Ordering Information

Part Number	No. of Devices	Container
ATF-54143-TR1	3000	7" Reel
ATF-54143-TR2	10000	13"Reel
ATF-54143-BLK	100	antistatic bag

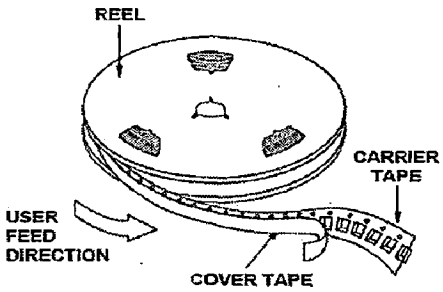
Package Dimensions
Outline 43
SOT-343 (SC70 4-lead)

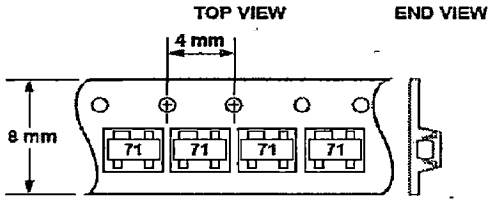


SYMBOL	DIMENSIONS	
	MIN.	MAX.
A	0.80 (0.031)	1.00 (0.039)
A1	0 (0)	0.10 (0.004)
b	0.25 (0.010)	0.35 (0.014)
C	0.10 (0.004)	0.20 (0.008)
D	1.90 (0.075)	2.10 (0.083)
E	2.00 (0.079)	2.20 (0.087)
e	0.55 (0.022)	0.65 (0.025)
h	0.450 TYP (0.018)	
E1	1.15 (0.045)	1.35 (0.053)
L	0.10 (0.004)	0.35 (0.014)
θ	0	10

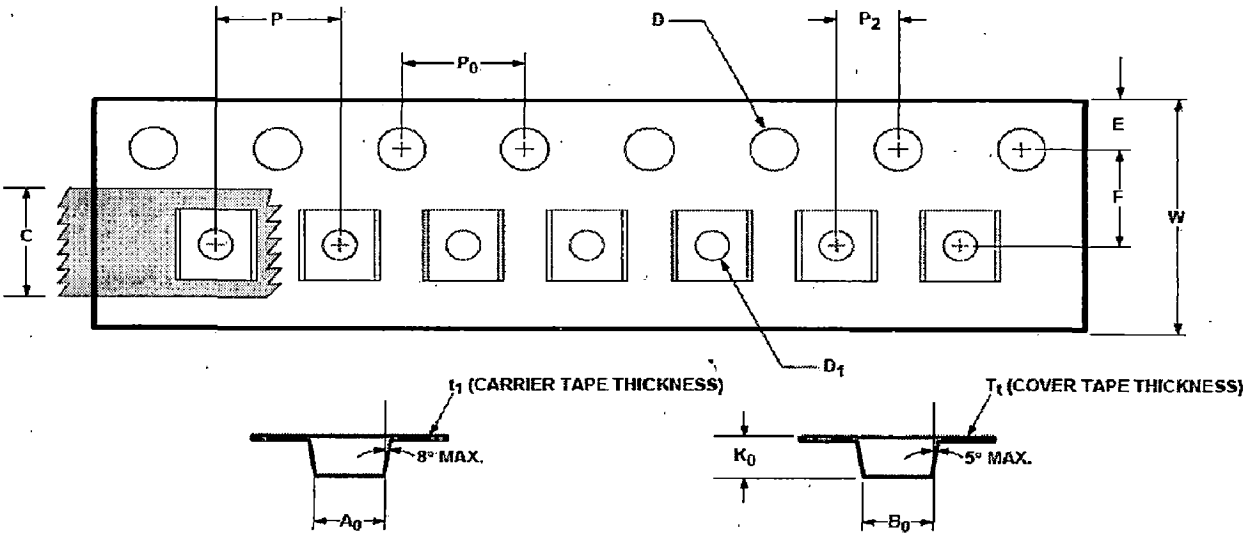
DIMENSIONS ARE IN MILLIMETERS (INCHES)

Device Orientation





Tape Dimensions For Outline 4T



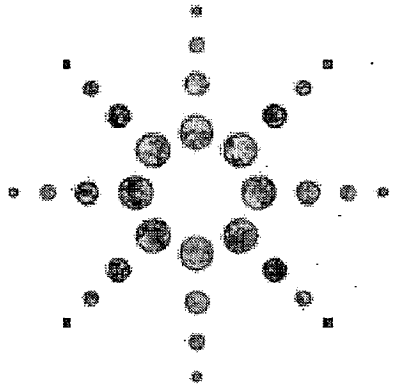
DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.24 ± 0.10	0.088 ± 0.004
	WIDTH	B_0	2.34 ± 0.10	0.092 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.255 ± 0.013	0.010 ± 0.0005
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_1	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

www.semiconductor.agilent.com
Data subject to change.

Obsoletes 5988-0450EN
May 31, 2001
5988-2722EN

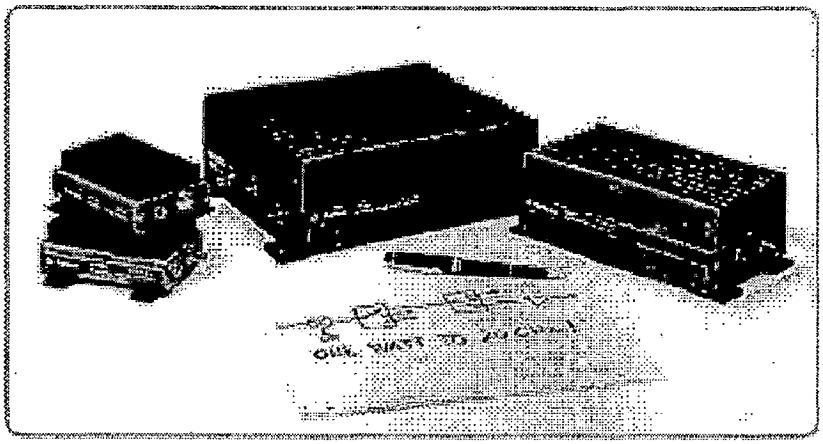
Agilent Technologies

Agilent 83000A Series Microwave System Amplifier



Agilent 83000A Series Microwave System Amplifiers

Technical Overview



Agilent Technologies Microwave System Amplifiers

83006A 10 MHz to 26.5 GHz
83017A 500 MHz to 26.5 GHz
83018A 2 to 26.5 GHz
83020A 2 to 26.5 GHz
83050A 2 to 50 GHz
83051A 45 MHz to 50 GHz

Features

- Ultra broadband to 50 GHz
- Up to 1 watt output power
- Compact size

Agilent model	Frequency (GHz)	Gain (dB)	Pout (dBm)
83006A	0.01 to 26.5	20	13
83017A	0.5 to 26.5	25	18
83018A	2 to 26.5	27	24
83020A	2 to 26.5	30	30
83050A	2 to 50	21	18
83051A	0.045 to 50	23	12*

*10 dBm 45 to 50 GHz

The Agilent microwave system amplifiers are compact, off-the-shelf amplifiers designed for system designers and integrators. This family of amplifiers provides power where you need it to recover system losses and to boost available power in RF and microwave ATE systems.

The ultrabroad bandwidth from 10 MHz to 50 GHz allows the designer to replace several narrow bandwidth amplifiers with a single Agilent amplifier, eliminating the need for crossover networks or multiple bias supplies.

The 83050A power amplifier and 83051A preamplifier expand frequency performance to 50 GHz, while the 1 Watt 83020A offers broadband power to 26 GHz. The small amplifier footprint allows for simple in-line insertion to existing system blocks that require amplification. The standard 83017A, 83018A, and 83020A include internal directional detectors for external leveling applications.

The 83020A is optionally available without the coupler-detector providing up to +30 dBm and +25 dBm, respectively. With excellent noise figure relative to their broad bandwidth and high gain, these amplifiers significantly improve system noise figure and dynamic range. These products come equipped with a low profile heat sink, an integral mounting bracket, and a two-meter DC power supply cable. Thermal and power supply design allows fast, easy integration into most measurement systems.

Applications

Small envelope size makes the Agilent Technologies family of microwave system amplifiers ideal for automated test and benchtop applications, offering the flexibility to place power where you need it.

Boost source output power

Increase output power from microwave sources to increase test system dynamic range. Drive high input power devices such as TWTs, mixers, power amps, or optical modulators. Drive test devices into compression for device characterization.

Recover systematic losses

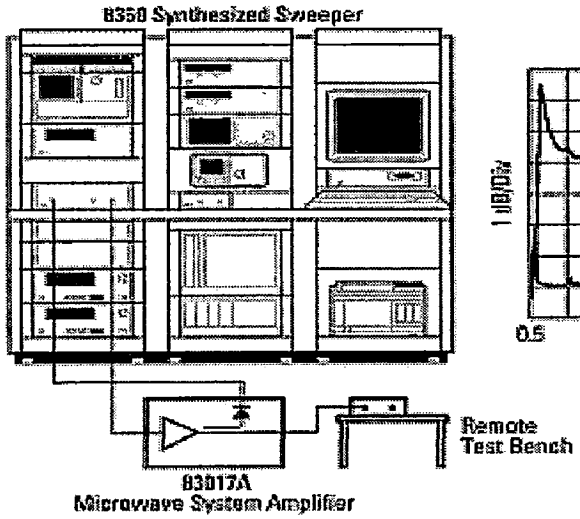
The microwave system amplifiers help solve the power loss from connectors, cables, switches, and signal routing components which consume valuable source power. Long transmission paths, common in antenna applications, are particularly susceptible to such losses.

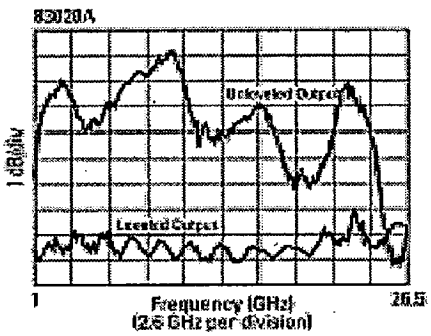
Level source power

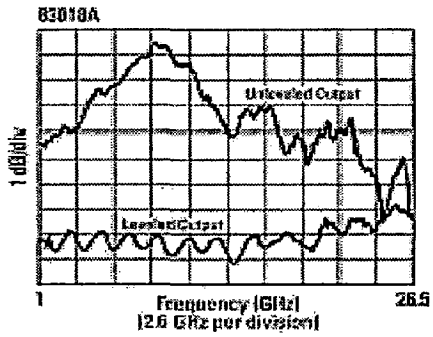
By using feedback to an external source ALC input, system designers can level output power at the test port, negating the effects of post-sweeper reflections and losses.

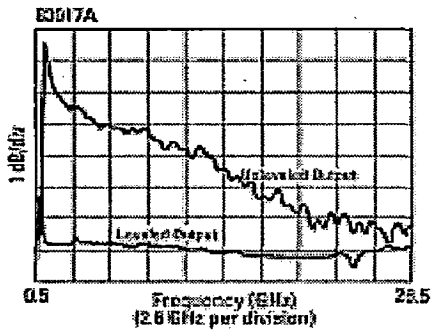
Simply route the directional detector output to the source external ALC input connector. The figures at right show typical results.

The 83020A, 83018A, and 83017A feature an integral directional detector to supply feedback. To level an 83006A amplifier, use the 0.01 to 26.5 GHz 83036C directional detector or the 1 to 26.5 GHz 87300C coupler with an 8474C detector.





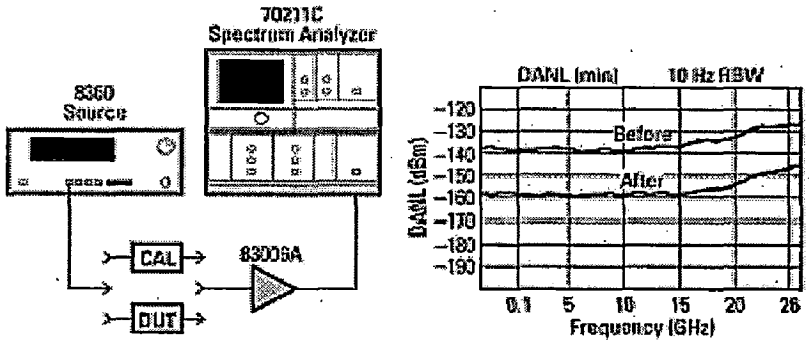




Improve Measurements

The 83006A, 83017A, and 83051A preamplifiers increase the sensitivity and dynamic range of spectrum analyzers. Add a preamplifier to noise figure measurement systems to significantly lower system noise figure. The table below shows typical system noise figure reduction achievable with these amplifiers. Note that the reduced system noise figure is dominated by the preamplifier noise figure. See Application Note 57-2, literature number 5952-3706.

SENSITIVITY IMPROVEMENT



Benchtop gain block

Benchtop microwave design tasks often require amplification to measure low level output characteristics, improve system dynamic range, perform saturation tests, or boost power levels. The Agilent family of system amplifiers offers small size and immediate, off-the-shelf solutions to microwave design, production, or test engineers.

Pulse parameter measurements

Fast rise time and multi-octave bandwidth make these amplifiers attractive for fast pulse parameter measurements. The 0.01, 0.5, and 2 GHz cutoff frequencies make them more useful for RF or impulse measurements with low duration times.

$$F_{sys} = F_{pa} + \frac{F_{sys} - 1}{G_{pa}}$$

All terms linear

Typical noise figure improvement

Amp model	Freq (GHz)	Max NF(dB)	Min gain (dB)	System noise figure (Fsys) without preamp (dB) 13	15	18	20	23	25	30
83006A	0.01–0.2	13	20	—	13.1	13.1	13.2	13.4	13.6	14.8
	0.2–18	8		8.1	8.2	8.4	8.6	9.2	9.8	12.1
	18–26.5	13		—	13.1	13.1	13.2	13.4	13.6	14.8
83017A	0.5–18	8	25	8.0	8.1	8.1	8.2	8.4	8.6	9.6
	18–26.5	13		—	13.0	13.0	13.1	13.1	13.2	13.6
83018A	1–2	10	23	10.0	10.1	10.1	10.2	10.4	10.6	11.8
	2–20	10	27	10.0	10.0	10.1	10.1	10.2	10.3	10.8
	20–26.5	13	23	—	13.0	13.1	13.1	13.2	13.3	14.0
83020A	1–20	10	30	10.0	10.0	10.0	10.0	10.1	10.1	10.4
	20–26.5	13	27	—	13.0	13.1	13.1	13.1	13.1	13.4
85050A	2–26.5	6	21	6.1	6.2	6.3	6.5	7.0	7.5	9.5
	26.5–50	10		10.0	10.1	10.1	10.2	10.4	10.6	11.8
83051A	0.045–2	12	23	12.0	12.0	12.1	12.1	12.3	12.4	13.2
	2–26.5	6		6.1	6.2	6.3	6.5	7.0	7.5	9.5
	26.5–50	10		10.0	10.1	10.1	10.2	10.4	10.6	11.8

Product specifications

Model number	83006A	83017A	83018A
Frequency range	10 MHz–26.5 GHz	0.5–26.5 GHz	2–26.5 GHz
Small signal gain	20 dB min	25 dB min	23 dB typ 1–2 GHz 27 dB min 2–20 GHz 23 dB min 20–26.5 GHz
Small signal gain flatness	±5 dB max 0.01–5 GHz ±3 dB max 5–26.5 GHz	±5 dB max 0.5–2 GHz ±5 dB max 2–26.5 GHz	±5 dB typ
Output power (At P max)	+18 dBm typ 0.01–10 GHz +16 dBm typ 10–20 GHz +14 dBm typ 20–26.5 GHz	+20 dBm typ 0.5–20 GHz +15 dBm typ 20–26.5 GHz	+23 dBm typ 1–2 GHz[2] +24 dBm min 2–20 GHz[2,3] +21 dBm min 20–26.5 GHz[2,3]
(At 1 dB compression)	+13 dBm min 0.01–20 GHz +10 dBm min 20–26.5 GHz	+19 dBm min 0.5–20 GHz +18 dBm–0.75 dB/GHz (20<f<26.5 GHz)	+22 dBm typ 1–2 GHz +22 dBm min 2–20 GHz +17 dBm min 20–26.5 GHz
Leveled output power **Flatness**[1]	N/A	±1.1 dB 0.5–26.5 GHz at 12 dBm ±1.5 dB 0.5–20 GHz at 18 dBm	±1.5 dB 1–26.5 GHz at 17 dBm
Noise figure	<13 dB typ 0.01–0.1 GHz <8 dB typ 0.1–18 GHz <13 dB typ 18–26.5 GHz	<8 dB typ 0.5–20 GHz <13 dB typ 20–26.5 GHz	<10 dB typ 1–20 GHz <13 dB typ 20–26.5 GHz
Harmonics (At spec'd value of P1 dBC)	–25 dBc 0.01–11 GHz –25 dBc typ 11–13.25 GHz	–20 dBc 0.5–11 GHz –20 dBc typ 11–13.25 GHz	–22 dBc typ 1–2 GHz –19 dBc 2–11 GHz –19 dBc typ 11–13.25 GHz
Harmonics (At spec'd max power)	N/A	N/A	–20 dBc typ 1–2 GHz –17 dBc typ 2–11 GHz –17 dBc typ 11–13.25 GHz
Input SWR	2.6:1	2.6:1	3:1 typ 1–2 GHz 3:1 2–26.5 GHz
Output SWR	2.8:1 0.01–18 GHz 3.2:1 18–26.5 GHz	2.6:1	7.0:1 typ 1–2 GHz 4.5:1 2–10 GHz 2.2:1 10–26.5 GHz
Non-harmonically related spurious	–65 dBc typ	–65 dBc typ	–65 dBc typ
Rise time	400 ps typ	310 ps typ	275 ps typ
Third order intercept (TOI)	30 dBm typ at 2 GHz 20 dBm typ at 26.5 GHz	30 dBm typ at 2 GHz 20 dBm typ at 26.5 GHz	36 dBm typ 2–20 GHz 31 dBm typ 20–26.5 GHz
Impedance	50 Ω typ	50 Ω typ	50 Ω typ
Reverse isolation (typ)	–65 dB	–65 dB	–55 dB at 1 GHz +0.95 dB/GHz
Survival input power	+23 dBm max	+23 dBm max	+23 dBm max
Power dissipation	6 W	9 W	24 W

1. At min specified P1 dBC within given frequency band

2. P max measured with 0 dBm input

3. Option 001 Pmax +25 dBm 2–20 GHz, +22 dBm 20–26.5 GHz

Product specifications (continued)

Model number	83020A	83050A	83051A
Frequency range	2–26.5 GHz	2–50 GHz	45 MHz–50 GHz
Small signal gain	30 dB typ 1–2 GHz 30 dB min 2–20 GHz 27 dB min 20–26.5 GHz	21 dB min	23 dB min
Small signal gain flatness	±5 dB typ	±3.5 dB max	±3.5 dB max
Output power (At P max)	+30 dBm typ 1–2 GHz[2] +30 dBm min 2–20 GHz[2,3] +30 dBm –0.7 dB/GHz[2,3] (20<f<26.5 GHz)	+20 dBm 2–40 GHz +19 dBm–0.2 dB/GHz (40<f<50 GHz)	+12 dBm to 45 GHz +10 dBm 45–50 GHz
(At 1 dB compression)	+28 dBm typ 1–2 GHz +28 dBm min 2–20 GHz +28 dBm–0.7 dB/GHz (20<f<26.5 GHz)	+15 dBm 2–40 GHz +13 dBm 40–50 GHz	+8 dBm 45 MHz–45 GHz +6 dBm 45–50 GHz
Leveled output power **Flatness**[3]	±1.5 dB typ 1–26.5 GHz At 23 dBm	N/A	N/A
Noise figure	<10 dB typ 1–20 GHz <13 dB typ 20–26.5 GHz	<6 dB typ 2–26.5 GHz <10 dB typ 26.5–50 GHz	<12 dB typ 45 MHz–2 GHz <6 dB typ 2–26.5 GHz <10 dB typ 26.5–50 GHz
Harmonics (At Spec'd value of P1 dBC)	–22 dBc typ 1–2 GHz –20 dBc typ 2–11 GHz –17 dBc typ 11–13.25 GHz	–20 dBc typ 2–18 GHz –18 dBc typ 18–25 GHz	–20 dBc typ 45 MHz–18 GHz –18 dBc typ 18–25 GHz
Harmonics (At Spec'd max power)	–20 dBc typ 1–2 GHz –17 dBc typ 2–11 GHz –17 dBc typ 11–13.25 GHz	N/A	N/A
Input SWR	3:1 typ 1–26.5 GHz	2.1 max	2.1 max
Output SWR	7.0:1 typ 1–2 GHz 4.5:1 2–10 GHz 2.2:1 10–26.5 GHz	2.8 max 2–18 GHz 2.1 max 18–50 GHz	2.2 max
Non-harmonically related spurious	–65 dBc typ	–50 dBc typ	–50 dBc typ
Rise time	375 ps typ	250 ps typ	225 ps typ
Third order intercept (TOI)	38 dBm typ 2–20 GHz 33 dBm typ 20–26.5 GHz	27 dBm typ	27 dBm typ
Impedance	50 Ω typ	50 Ω typ	50 Ω typ
Reverse isolation (typ)	–55 dB	–50 dB typ	–50 dB typ
Survival input power	+23 dBm max	+20 dBm max	+20 dBm max
Power dissipation	48 W	11 W	5 W

1. At min specified P1 dBC within given frequency band

2. P max measured with +5 dBm input

3. Option 001 deletes detected output, for Pmax add 0.5 dBm 1–26.5 GHz

Special Applications: Higher performance models available upon request (i.e., higher power, etc.)

Product specifications (continued)

Model number	83006A	83017A	83018A
*Bias voltage and current (nominal) mA	12 ±1 Vdc at 410 ±85 mA –12 ±1 Vdc at 10 ±5 mA	12 ±1 Vdc at 780 ±140 mA –12 ±1 Vdc at 20 ±2 mA	12 ±1 Vdc at 1940 ±123 mA –12 ±1 Vdc at 10 ±5 mA
RF connectors	3.5 mm (f)	3.5 mm (f)	3.5 mm (f)
Detector output	N/A	BNC (f)	BNC (f)
Detector sensitivity	N/A	15 µV/µW	4 µV/µW
Detector polarity	N/A	Negative	Negative
Weight: net shipping	0.64 kg (1.4 lb) 1.32 kg (2.9 lb)	0.64 kg (1.4 lb) 1.32 kg (2.9 lb)	1.8 kg (4.0 lb) 2.9 kg (6.4 lb)

*Do not apply positive voltage before negative voltage.

Environmental specifications

Temperature coefficient of gain	–0.07 dB/° C	–0.1 dB/° C	–0.13 dB/° C
Operating temperature	0 to +55° C	0 to +55° C	0 to +55° C
Storage temperature	–40 to +70° C	–40 to +70° C	–40 to +70° C

Other environmental information

EMC[1]	IEC 61326:1997/EN 61326:1997 CISPR 11:1997/EN 55011:1998, Group 1, Class A
Safety	IEC 348:1978/HD 401 S1:1981 CAN/CSA-C22.2 No. 231 (Series M-89)
Moisture resistance	65° C at 95% RH for 10 days per Mil-Std-883C method 1004.5
Random vibration	5.2 G (rms) to 2000 Hz per Mil-Std-883C method 2026 test condition 11A
Shock	1500 G (peak), 0.5 ms per Mil-Std-883C method 2002.3 test condition B
Altitude, non-operating	15,000 m per Mil-Std-883C method 1001 test condition C

1. This ISM device complies with Canadian ICES-001. Cet appareil ISM est conforme a la norme NMB-001 du Canada.

General specifications (continued)

Model number	83020A	83050A	83051A
*Bias voltage and current (nominal)	15 ±1.5 Vdc at 3200 ±800 mA –15 ±0.5 Vdc at 20 ±5 mA	12 ±1 Vdc at 900 ±110 mA –12 ±1 Vdc at 30 ±5 mA	12 ±1 Vdc at 314 ±34 mA –12 ±1 Vdc at 30 ±5 mA
RF connectors	3.5 mm (f)	2.4 mm (f)	2.4 mm (f)
Detector output	BNC (f)	N/A	N/A
Detector sensitivity	1 pV/pW	N/A	N/A
Detector polarity	Negative	N/A	N/A
Weight: net shipping	3.9 kg (8.5 lb) 5.0 kg (11 lb)	0.64 kg (1.4 lb) 1.32 kg (2.9 lb)	0.64 kg (1.4 lb) 1.32 kg (2.9 lb)

*Do not apply positive voltage before negative voltage.

Environmental specifications

Temperature coefficient of gain	–0.19 dB/° C	–0.09 dB/° C	–0.09 dB/° C
Operating temperature	0 to +55° C	0 to +55° C	0 to +55° C
Storage temperature	–40 to +70° C	–40 to +70° C	–40 to +70° C

Other environmental information

EMC[1]	IEC 61326:1997/EN 61326:1997 CISPR 11:1997/EN 55011:1998, Group 1, Class A
Safety	IEC 348:1978/HD 401 S1:1981 CAN/CSA-C22.2 No. 231 (Series M-89)
Moisture resistance	65° C at 95% RH for 10 days per Mil-Std-883C method 1004.5
Random vibration	5.2 G (rms) to 2000 Hz per Mil-Std-883C method 2026 test condition 11A
Shock	1500 G (peak), 0.5 ms per Mil-Std-883C method 2002.3 test condition B
Altitude, non-operating	15,000 m per Mil-Std-883C method 1001 test condition C

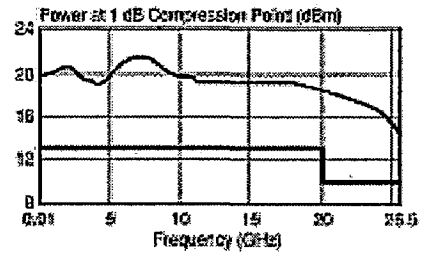
1. This ISM device complies with Canadian ICES-001. Cet appareil ISM est conforme a la norme NMB -001 du Canada.

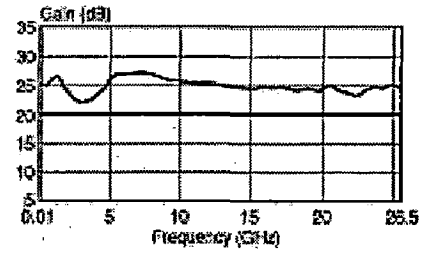
Specifications describe the instrument's warranted performance over the temperature range +20° C to +30° C (unless otherwise noted). All specifications apply after the instrument's temperature has been stabilized after one hour continuous operation. Typical characteristics are intended to provide information useful in applying the instrument by giving typical but nonwarranted performance parameters. These are denoted as "typical" or "nominal" and apply over the temperature range +20° C to +30° C.

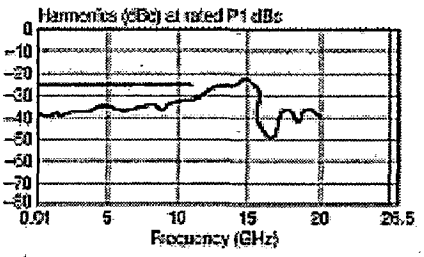
Caution on Electrostatic Discharge: Electrostatic discharge (ESD) can damage or destroy electronic components. It is recommended that these amplifiers, like other electronic components, be installed and operated at a static-free workstation or in an environment where precautions against ESD have been implemented.

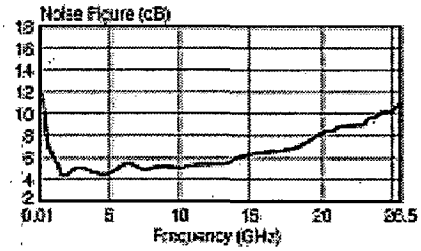
Graphical performance data

83006A Amplifier

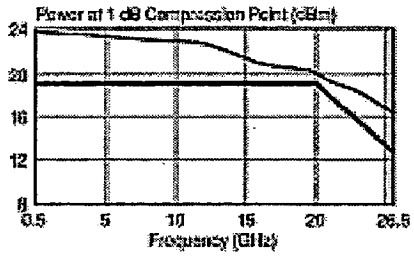


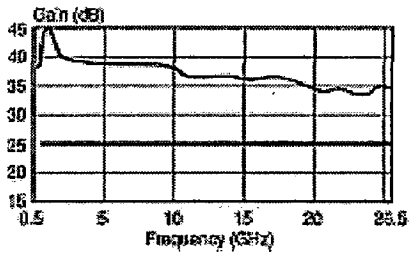


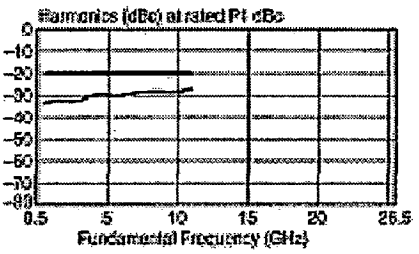


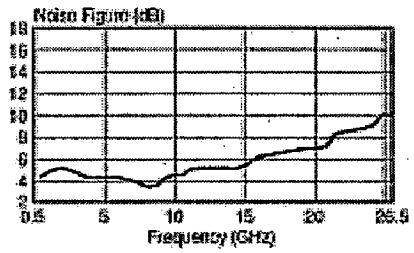


83017A Amplifier

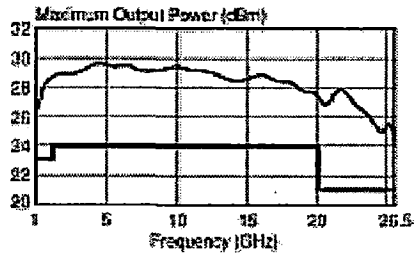


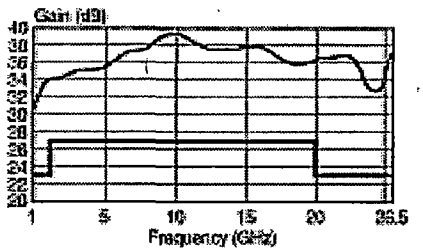


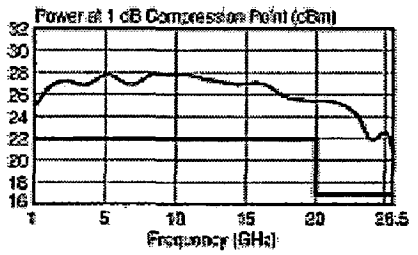


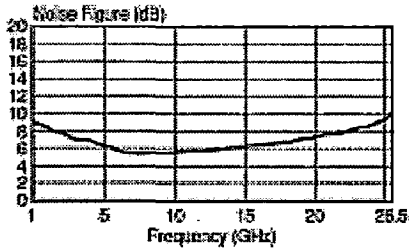


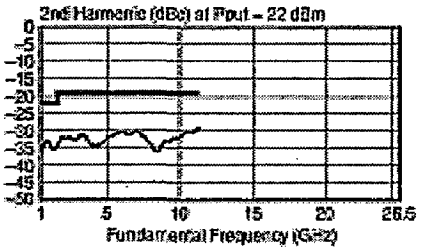
83018A Amplifier





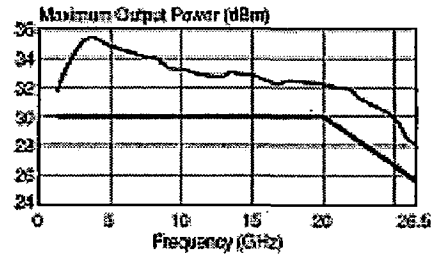


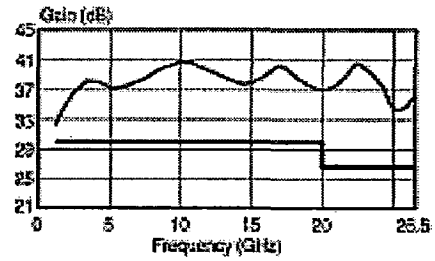


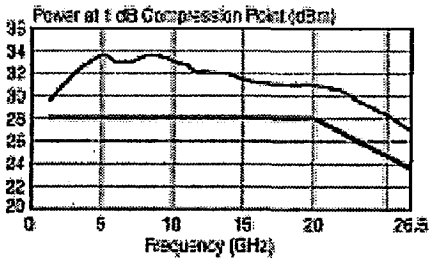


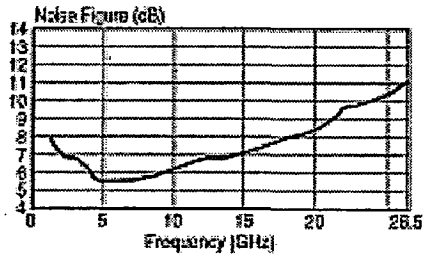
Graphical performance data (continued)

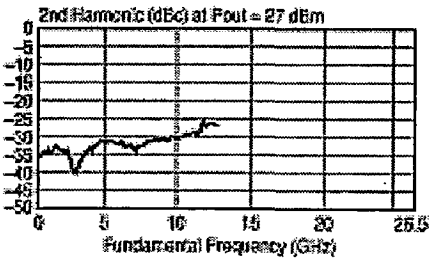
83020A Amplifier



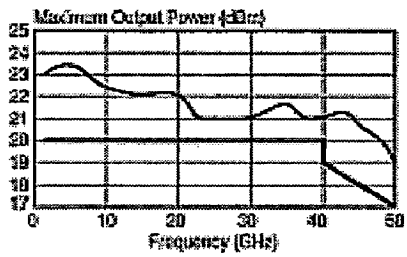


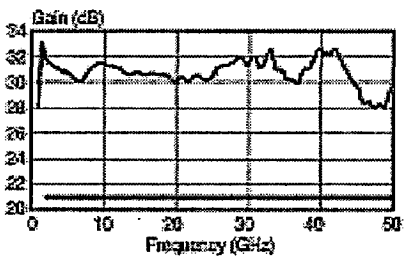


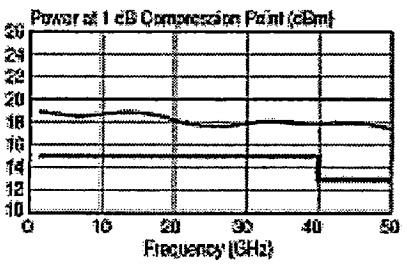


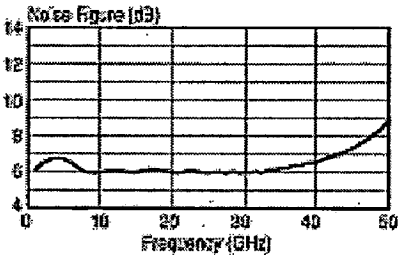


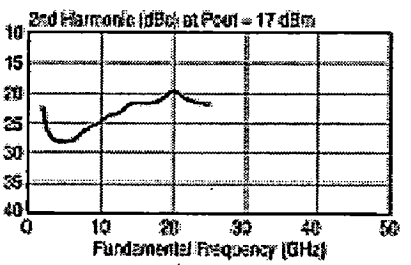
83050A Amplifier



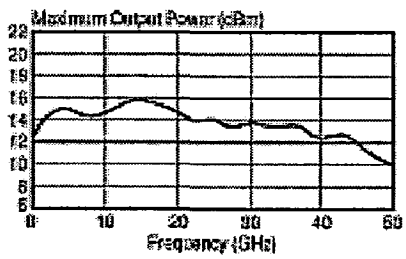


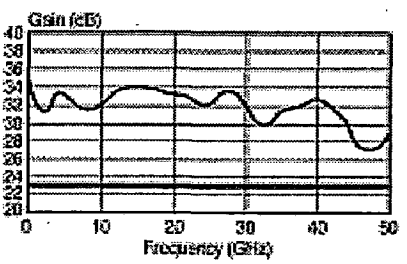


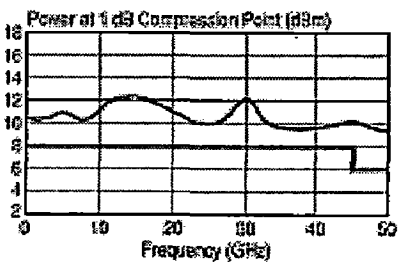


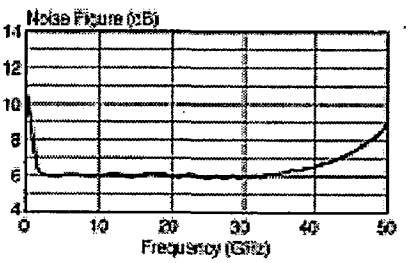


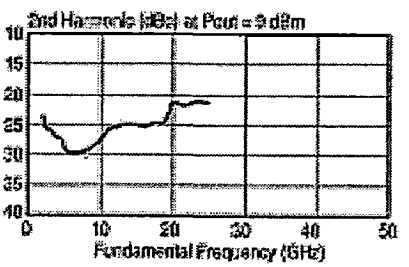
83051A Amplifier











Coaxial

Frequency Mixer

ZMX-7GHR

Level 17 (LO Power +17 dBm) 3700 to 7000 MHz

CASE STYLE: BU413

Connectors	Model	Price	Qty.
SMA	ZMX-7GHR	$84.95 ea.	(1-9)

Maximum Ratings

Operating Temperature	-55°C to 100°C
Storage Temperature	-55°C to 100°C
RF Power	200mW
IF Current	40mA

Permanent damage may occur if any of these limits are exceeded.

Coaxial Connections

LO	2
RF	1
IF	3

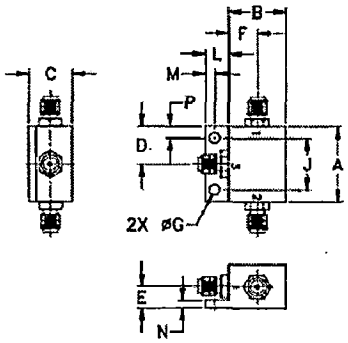
Features

- wide frequency range, 3700 to 7000 MHz
- low conversion loss, 5.3 dB typ.
- good L-R isolation, 33 dB typ., L-I, 34 dB typ.

Applications

- SATCOM
- instrumentation
- defense & federal communications
- SHF

Outline Drawing



Outline Dimensions (inch / mm)

A	B	C	D	E	F	G	H
1.00	.75	.58	.50	.29	.38	.140	–
25.40	19.05	14.73	12.70	7.37	9.65	3.56	–
J	**K**	**L**	**M**	**N**	**P**		**wt**
.687	–	.32	.13	.10	.16		grams
17.45	–	8.13	3.30	2.54	4.06		25.0

Electrical Specifications

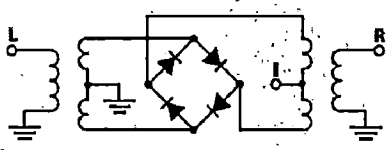
FREQUENCY (MHz)		CONVERSION LOSS (dB)			LO-RF ISOLATION (dB)		LO-IF ISOLATION (dB)	
LO/RF	IF			Total Range Max.				
f_L-f_U		$\bar{X}$	σ		Typ.	Min.	Typ.	Min.
3700-7000	DC-1000	5.3	0.30	8.5	33	20	34	20

1 dB COMP.: +14 dBm typ.

Typical Performance Data

Frequency (MHz)		Conversion Loss (dB)	Isolation L-R (dB)	Isolation L-I (dB)	VSWR RF Port (:1)	VSWR LO Port (:1)
RF	LO	LO +17dBm	LO +17dBm	LO +17dBm	LO +17dBm	LO +17dBm
3700.00	3730.00	3.95	31.94	27.92	1.61	1.71
3886.79	3916.79	4.04	29.49	29.05	1.40	1.73
4000.00	4030.00	4.07	31.32	29.24	1.88	1.81
4260.38	4290.38	4.38	38.08	31.10	2.09	1.98
4509.43	4539.43	4.80	35.04	30.94	3.21	1.73
4698.23	4728.23	5.21	31.75	31.14	2.05	1.69
4883.02	4913.02	5.30	31.22	31.93	2.73	1.61
5000.00	4970.00	5.23	32.26	32.82	2.78	1.52
5194.34	5164.34	5.41	32.90	34.00	3.05	1.36
5381.13	5351.13	5.55	31.71	34.53	3.31	1.31
5567.92	5537.92	5.73	30.38	34.48	3.64	1.33
5754.72	5724.72	5.70	31.17	34.72	4.13	1.35
6000.00	5970.00	6.11	30.09	34.77	5.23	1.17
6252.83	6222.83	6.58	29.87	34.26	5.86	1.10
6315.09	6285.09	6.91	30.08	34.24	6.08	1.13
6501.89	6471.89	6.95	30.95	33.65	6.11	1.20
6626.42	6596.42	6.82	30.68	32.90	6.05	1.23
6750.94	6720.94	6.68	29.96	32.03	6.20	1.23
6875.47	6845.47	6.55	29.25	31.16	6.04	1.23
7000.00	6970.00	6.40	28.57	30.32	5.61	1.17

Electrical Schematic



REV. OR
M93711
ZMX-7GHR
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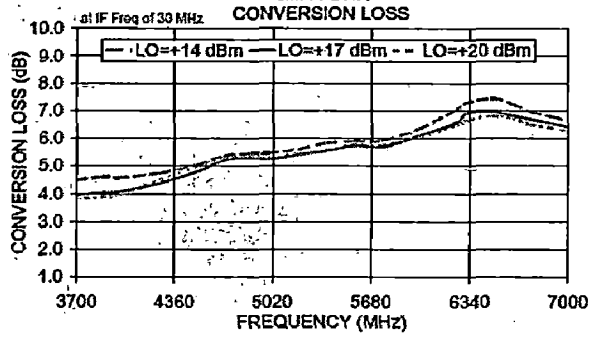
Page 1 of 2

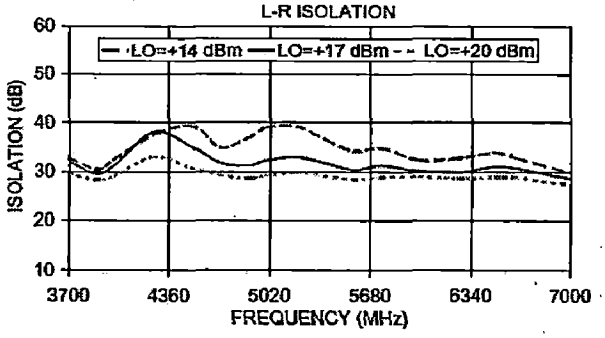
Performance Charts

ZMX-7GHR

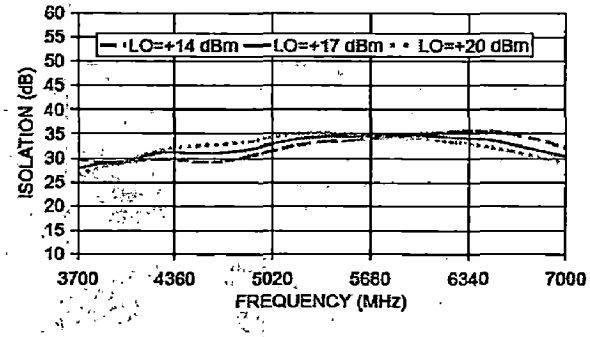
ZMX-7GHR
CONVERSION LOSS
at IF Freq of 30 MHz



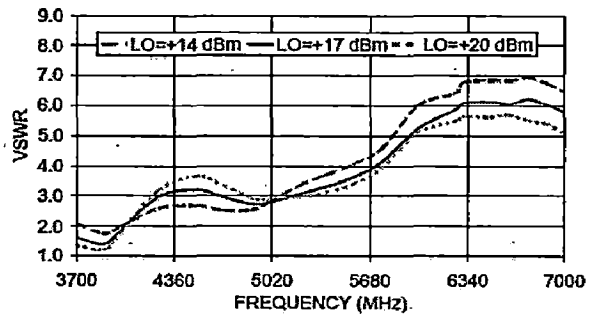
ZMX-7GHR
L-R ISOLATION



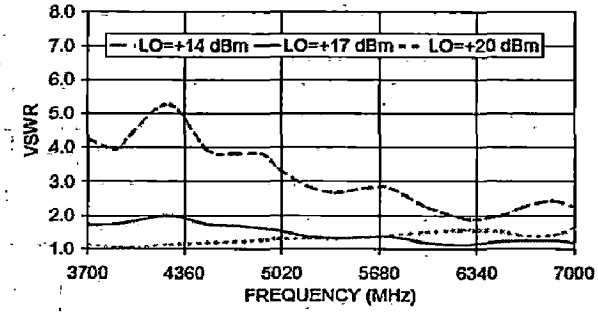
ZMX-7GHR
L-I ISOLATION



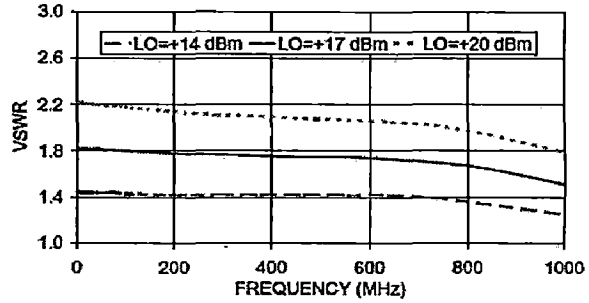
ZMX-7GHR
RF VSWR



ZMX-7GHR
LO VSWR



ZMX-7GHR
IF VSWR

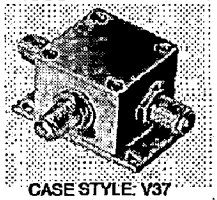


Coaxial

Frequency Mixer

Level 13 (LO Power +13 dBm) 300 to 4300 MHz

ZEM-4300MH+
ZEM-4300MH



CASE STYLE: V37

Connectors	Model	Price	Qty.
SMA	ZEM-4300MH(+)	$89.95	(1-9)

+ RoHS compliant in accordance with EU Directive (2002/95/EC)

The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications.

Maximum Ratings

Operating Temperature	-55°C to 100°C
Storage Temperature	-55°C to 100°C
RF Power	200mW
IF Current	40mA

Coaxial Connections

LO	2
RF	1
IF	3

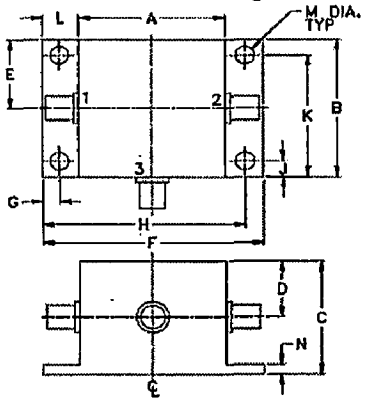
Features

- low conversion loss, 6.42 dB typ.
- broadband, 300 to 4300 MHz
- IF response to DC

Applications

- UHF/VHF
- MMDS
- ISM/GPS
- instrumentation

Outline Drawing



Outline Dimensions (inch / mm)

A	B	C	D	E	F	G
.83	.83	.75	.37	.42	1.25	.100
21.08	21.08	19.05	9.40	10.67	31.75	2.54

H	J	K	L	M	N	wt
1.150	.095	.735	.21	.106	.06	grams
29.21	2.41	18.67	5.33	2.69	1.52	34

Electrical Specifications

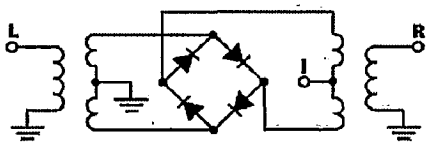
FREQUENCY (MHz)		CONVERSION LOSS (dB)			LO-RF ISOLATION (dB)				LO-IF ISOLATION (dB)			
		Mid-Band			L		U		L		U	
LO/RF	IF			Total Range								
f_L-f_U		$\overline{X}$	σ	Max.	Typ.	Min.	Typ.	Min	Typ.	Min.	Typ.	Min
300-4300	DC-1000	6.42	0.15	9.5	40	20	40	20	14	7	12	7

1 dB COMP.: +9 dBm typ. L = low range [f_L to 10 f_L] U = upper range [10 f_L to f_U]

Typical Performance Data

Frequency (MHz)		Conversion Loss (dB)	Isolation L-R (dB)	Isolation L-I (dB)	VSWR RF Port (:1)	VSWR LO Port (:1)
RF	LO	LO +13dBm	LO +13dBm	LO +13dBm	LO +13dBm	LO +13dBm
300.00	500.00	7.02	42.09	9.54	2.21	5.54
500.00	700.00	6.56	33.47	9.04	3.20	5.20
575.86	775.86	6.30	35.56	9.47	3.19	5.14
600.00	800.00	6.62	35.00	9.79	2.55	6.32
989.66	789.66	6.61	36.09	17.49	1.64	4.48
1000.00	800.00	6.53	36.06	17.37	2.66	3.06
1403.45	1203.45	6.30	32.65	14.72	5.34	2.48
1679.31	1479.31	5.89	39.70	19.11	4.31	4.59
2000.00	1800.00	6.16	34.09	23.50	2.63	2.77
2093.10	1893.10	6.43	33.26	23.82	2.48	1.88
2231.03	2031.04	6.54	32.41	25.64	2.42	1.88
2368.97	2168.97	6.30	31.34	28.66	2.35	1.89
2506.90	2306.90	6.24	29.89	27.33	2.26	1.90
2920.69	2720.69	6.23	27.73	17.77	2.30	2.41
3000.00	2800.00	6.20	26.08	16.39	2.29	2.23
3334.48	3134.48	6.22	27.73	15.67	2.29	3.01
3610.34	3410.35	6.38	30.12	13.56	1.82	2.73
4000.00	3800.00	6.47	33.12	10.27	2.35	1.84
4162.07	3962.07	6.54	35.73	10.47	2.27	2.41
4300.00	4100.00	6.83	39.65	11.87	2.30	3.08

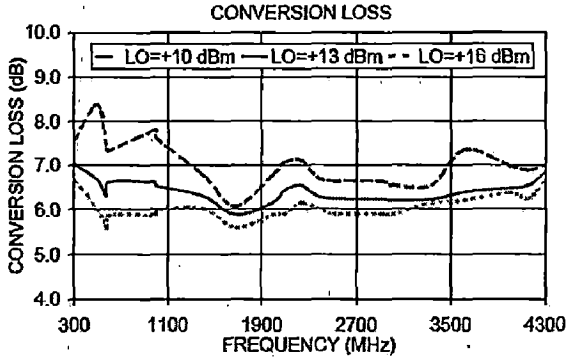
Electrical Schematic



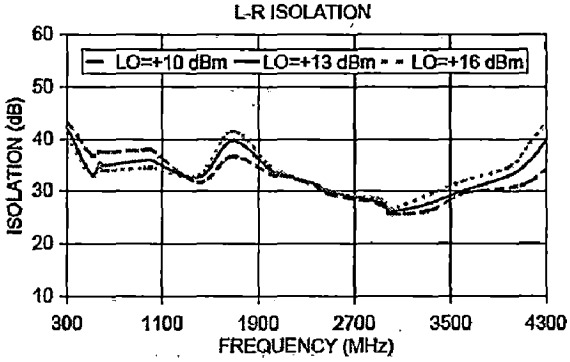
ZEM-4300MH+
ZEM-4300MH

Performance Charts

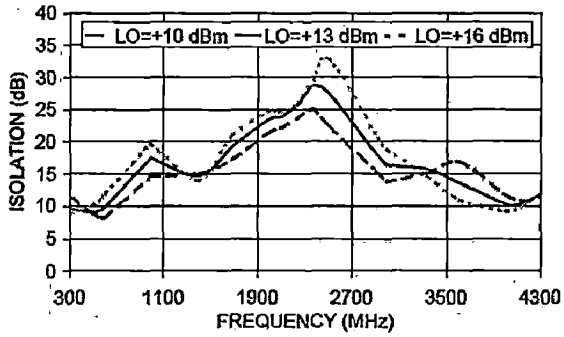
ZEM-4300MH
CONVERSION LOSS



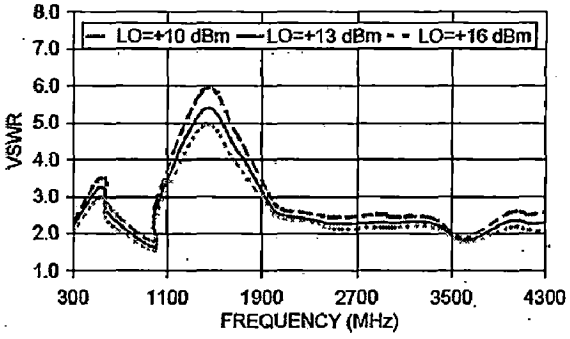
ZEM-4300MH
L-R ISOLATION



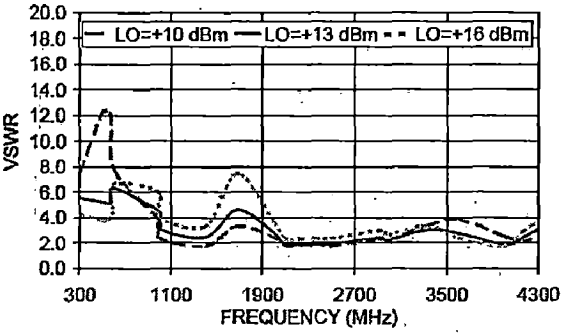
ZEM-4300MH
L-I ISOLATION



ZEM-4300MH
RF VSWR



ZEM-4300MH
LO VSWR



ZEM-4300MH
IF VSWR