OPTIMAL DESIGN OF NON-LINEAR ELECTRONIC CIRCUITS

A DISSERTATION

submitted in partial fulfilment of
the requirements for the award of the degree
of
MASTER OF ENGINEERING
in
ELECTRICAL ENGINEERING
(System Engineering & Operation Research)

by

PRADEEP KUMAR GUPTA

DEPARTMENT OF ELECTRICAL ENGINEERING
UNIVERSITY OF ROORKEE
ROORKEE-247672 (INDIA)

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C E R T I F I C A T E

Certified that the M.E.dissertation entitled, "OPTIMAL DESIGN OF NON LINEAR ELECTRONIC CIRCUTS" which is being submitted by Sri P.K.Gupta in partial fulfilment for the award of the Degree of ME in Electrical Engineering (Sysetm Engg.& Operation Research) of the University of Roorkee, Roorkee is record of students own work carried out by him under our supervision and guidance . The matter embodied in this dissertation has not been submitted for the award of any other degree or diploma.

This is further certified that he has worked for a period of 18 months from Feb.1980 to Aug.1981for preparing this dissertation for the Master of Engg.Degree at M/s Indian Telephone Industries Ltd; Naini.

(Dr.H.O.GUPTA)
Reader Elect.Engg.Deptt.
University of Roorkee
Roorkee

(A.K.VANWASI)
Senior Engineer
Research & Development Division
I.T.I. Ltd.Naini,ALLD.

A C K N O W L E D G E M E N T S

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PRADEEP KUMAR GUPTA

A B S T R A C T

Switching mode converters are basically nonlinear time varying discrete time systems. For analysing such systems either nonlinear discrete time or small scale linearization techniques are used. This work is concerned with modelling and analysis of the audiosusceptibility performance of a switching mode converter using DIDF technique.

A general method for modelling power stages of any switching mode d.c. to d.c. converter has been developed through the State-Space approach. The fundamental step is in replacement of the state space description of the two switched network by their average over the single switching period T, which results in a single continuous state space description. From state space description a canonical circuit model is developed which gives various performance characteristics of different switching converters directly.

Using this technique, a small signal average model of switching mode regulator is derived to investigate the complex interaction among input filter, output filter and control loop. Performance indices of a switching regulator have been formulated, and a comparison has been made for a series switching regulator using different input filter configurations. Basic constraints for optimal two stage input filter configuration have been discussed.

LIST OF SYMBOLS USED

T, τ	: Time period
T_{ON}	: Time when switch is ON
T_{OFF}	: Time when switch is OFF
d	: Duty cycle
Z_s	: Output Impedence of Input filter
Z_i	: Input Impedence of switching regulator
H_s	: Forward transfer function of Input filter
μ	: Transformation ratio of d.c. to d.c. transformer
W_s	: Filter cut-off frequency
F	: Switching frequency
F_c	: Duty cycle power stage gain
F_p	: Power stage transfer function
F_E	: Transfer function of Error Processor
F_M	: Transfer function of PWM
$G_T(s)$	: Open loop gain of switching regulator
$G_A(s)$	: Audiosusceptibility
α	: Attenuation of Input filter
B_F	: Resonant peaking of H_s
B_R	: Resonant peaking of Z_s

C O N T E N T S

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CHAPTER I

INTRODUCTION

1.1. Introduction

- 1.1.1 Introduction of Non-Linear Systems.
- 1.1.2 Common methods of non linear system study

1.2 Linear Power Supplies & Switching Mode Regulator

- 1.2.1 Linear Power Supply and its types
- 1.2.2 Switched Mode Power Supply
- 1.2.3 Advantages & disadvantages of Switched mode Regulators

1.3 General Circuits for Power Supply Regulators

- 1.3.1 Buck Regulator
- 1.3.2 Boost Regulator
- 1.3.3 Buck-Boost Regulator

1.4 Performance Indices of Switching Regulator

1.5 Organisation of the Thesis

1.1 INTRODUCTION

Most of the practical systems are non-linear in nature. For a nonlinear system superposition principle is no longer valid. In such systems there is no possibility of generalized form of response, as the response of such systems depends upon the magnitude and type of the input. In other words a non-linear system behaves completely differently for different type of inputs. This constitutes a fundamental and important difficulty in studying nonlinear systems.

In spite of the analytic difficulties, we have no choice but to attempt to deal in some way with nonlinear systems, because of the importance of such systems. No single method can be used for all types of nonlinear systems. The existing methods for analysing nonlinear systems are described in [9], these can be classified as under:

1. prototype test :

The most certain means of studying a system is to build one and test it. The greatest advantage of this is that it avoids the necessity of choosing a mathematical model. The disadvantages are the time required to construct a series of trial systems, the cost involved etc.

2. Closed Form Solution :

There are a number of nonlinear differential equations,

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2. Closed Form Solution :

There are a number of nonlinear differential equations,

mostly of second order, for which exact solutions have been found or for which certain properties of the solutions have been tabulated. But this is applicable only for certain special cases.

3. Phase plane Solution :

The dynamic properties of a system can be described in terms of the differential equations of state, and an attempt made to solve for the trajectories of the system in the state space.

4. Lyapunov's Direct Method :

One of the most important properties of a system, stability, can in principle, be evaluated without calculating the detailed responses of the system.

5. Series Expansion Solution :

A whole family of techniques exists which develop the solutions of nonlinear differential equations or express the dynamic properties of non-linear systems in expansion of various forms.

6. Linearization :

The problem of studying a nonlinear system can be avoided altogether by simply replacing each nonlinear operation by an approximating linear operation and

studying the resulting linear system.

7. Computer Simulation :

In the cases where manual analysis of nonlinear characteristic becomes impractical, modern computer is the only alternative. Small signal operation of semiconductor devices can be represented by linear circuit model which may be analysed through the use of well documented computational techniques.

For design and analysis of a system with multiple nonlinearities, it is separated into functional blocks, with each block containing one nonlinearity. The block is then linearized, and all linear blocks are then used jointly to arrive at an initial system design and analysis.

A switching regulator contains two major non-linearities. The first resides in the power stage, and is due to the on-off operation of the power switch and the different circuit topologies attendant to the respective time intervals. The second exists in the digital signal processor accomplishing the analog to discrete time duty cycle conversion. But before going in detail of modelling and analysis of switching mode converters and the problem arises therein we will briefly discuss in the next section the conventional power supplies and the advantages of switching mode converters over conventional linear power supplies.

1.2 Linear Power Supply & Switching Mode Converters :

A power supply equipment is defined as :

> "An item of equipment that accepts power from batteries or from the mains, and converts or modifies it for use in a particular part of equipment."

When a load requires precision control of both voltages and current and when an outside ac or dc source of energy is used, a system must incorporate a power supply using a regulator. Basically there are two types of regulators - dissipative and non-dissipative.

The dissipative regulator absorbs the difference between input voltage at the source and the regulated voltage at the load. A non-dissipative regulator stores excess power in an LC filter and delivers the power to the load in measured intervals. Non-dissipative regulators use switching devices to control output power. During the time switch is ON, power is stored in an energy storage network (the LC filter) and is delivered to the load as required. Ideally, the switching approach exhibits non power dissipation. The block diagram of linear power supply is shown in fig. 1.1.

Switched mode power supply :

The term 'Switched Mode Power Supply" covers a number of modern techniques and circuits for the conversion of a given dc voltage and current, to one or more other dc voltages and/or currents. In other words, switched mode

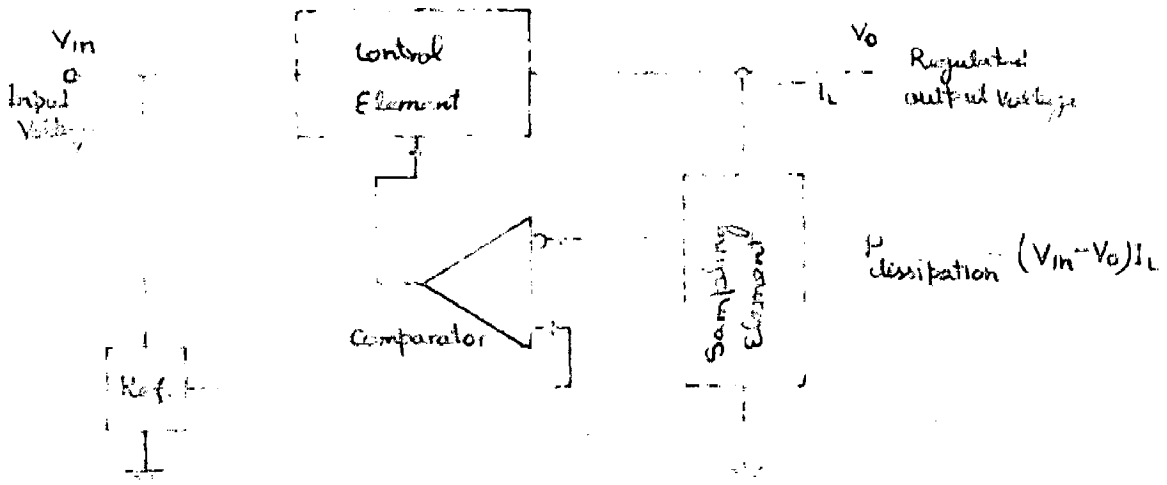


FIG 1.1 BLOCK DIAGRAM OF LINEAR POWER SUPPLY

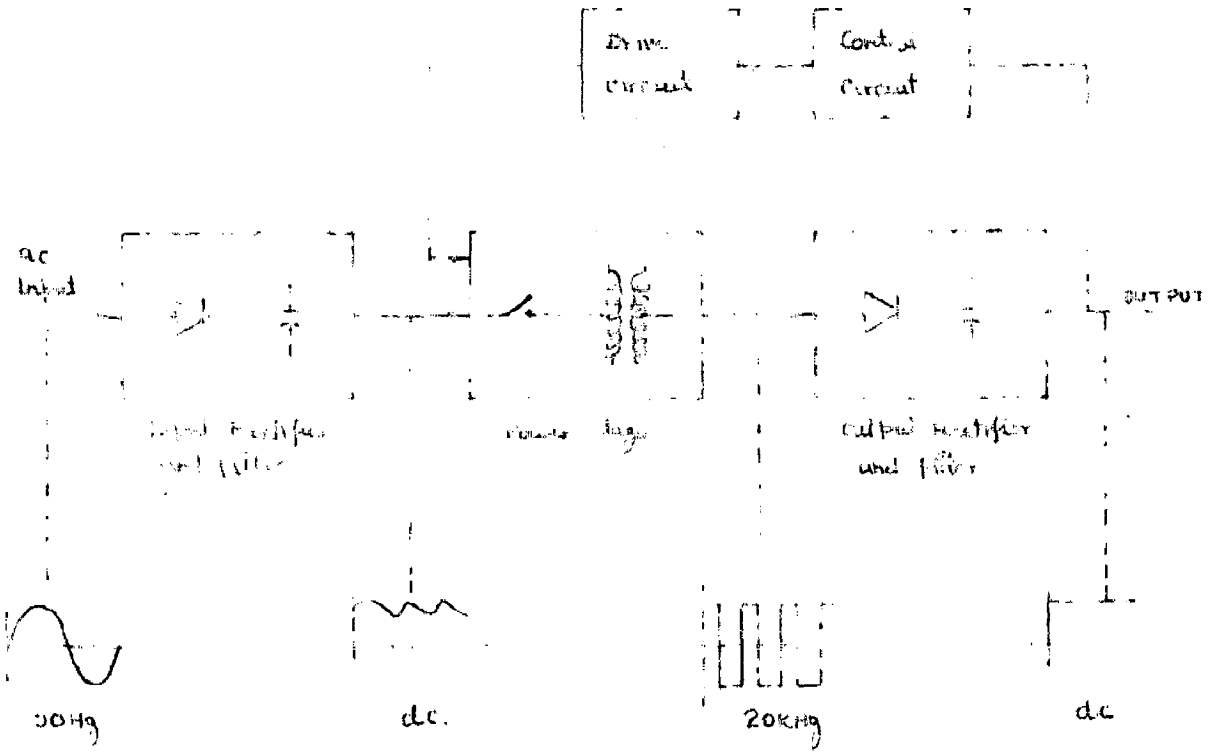


FIG 1.2 BLOCK DIAGRAM OF AN A C INPUT SWITCHED MODE POWER SUPPLY

power supplies are all d.c. to d.c. converters. The qualification "switched mode" indicates that the input voltage to the power supply is switched on and off, normally at a rate above the audible range. Thus switched moder power supply is a modern solid state version of the electromechanical vibrator.

The schematic diagram of switched mode power supply is shown in fig. 1.2. Main a.c. input of 50 Hz is rectified and smoothed by input rectifier and filter, the output of which is unregulated d.c. voltage. This d.c. voltage is chopped at high frequency by a transistor and output is fed to a transformer. The output of power stage gives high frequency pulses of 20 KHz. These are rectified and filtered by output rectifier and filter to give required d.c. output. Output is sensed by the control circuit and a correction signal is produced which is used to vary the ON/OFF ratio usually called 'Duty-Cycle' which results regulated d.c. voltage at output.

Non-dissipative components are the basis for switch mode regulation. The inductor and capacitor of switched mode regulator exhibits little d.c. resistance, hence dissipate little d.c. power. The switch, a transtor, either fully off or saturated, dissipates much less power.

Advantages of Switching Mode Regulators :

(i) Power Dissipation :

Linear dissipative series or shunt regulator dissipates large amount of power at high load currents, especially when input-output difference is large.

Since the power transistor switch is always either cut-off or saturated (except for a very brief transition between these two states) and load current flows through low resistance elements, the switch, the inductor, capacitor and the 'ON' diode, the d.c. dissipation is therefore less.

(ii) Size and Weight :

The size and weight of a power supply rated for any given output power are determined chiefly by the switching frequency, the internal power dissipation and the size of the heat exchanges. Other factors are the magnetic components - transformers, inductors and capacitors. The size of the magnetics included in the power supply is inversely proportional to the switching frequency of the regulator. For example, a typical 50 Hz transformer that can handle one kilowatt of power has volume of 160 cubic inches and weight about 10 Kg. A 20 KHz transformer, on the other hand would be about 40 cubic inches and weight just one Kg. Thus with high switching frequency there is a considerable reduction in

transformer size and weight and some reduction in the size of the smoothing components.

(iii) Efficiency :

Since power dissipation in switching regulator is less, it maintains high efficiency over wide range in load current. Moreover, with the reduction of size, the power loss to maintain the same temperature rise in the regulator box is also reduced, as cooling is proportional to surface area. This again results increase in efficiency. In general switching regulators are twice as efficient as linear supplies. The typical efficiency figures for linear power supplies are 30% to 40%, whereas, for switching mode regulator it is 60% to 90%.

Since efficiency of switching regulator is twice that of linear power supplies, therefore, input current amplitude will be half as high in case of switching regulator, which in turn, reduces the amplitude of the input current spectrum.

In addition to saving in weight, volume , power and cost, the switching power supplies offer further advantages because of its versatility. It is simple matter of changing one connection to enable a supply to operate with either 110 volt or 220 volts a.c.

Furthermore, in case of a.c. input,since smoothing is

done at 250V instead of at the low voltage, it allows further saving in capacitor size and cost. Because energy stored is proportional to cv^2, while the capacitor volume is proportion to cv.

Disadvantages :

1. The primary power source delivers current to the switching regulator in pulses which for efficiency reasons, have short rise and fall times. In these applications where a significant series impedance appears between the supply and regulator, the rapid changes in current can generate considerable noise. This problem can be reduced by reducing the series impedance, increasing the switching time, or by filtering the input to the regulator.
2. Response time to rapid changes in load current. The switching regulator will reach a new equilibrium only when the average inductor current reaches it new steady state value. In order to make this time short, it is advantageous to use low inductor values.

1.3 General Circuits for Power Supply Regulators :

There are several designs for power supply circuitory. The common names for the six most widely used circuits are -

1. Buck regulator
2. Boost regulator
3. Buck-Boost regulator
4. Full bridge regulator converter
5. Half bridge regulator converter
6. Push-Pull regulator converter.

Here we will discuss only the first three circuits which are most common.

Buck Regulator :

The circuit for this type of regulator is shown in fig. fig. 1.3(a). The control circuit causes transistor switch Q_1 to switch ON and OFF at a predetermined frequency f. During the time that Q_1 is ON, T_{on}, the input voltage, E_{in} is applied to the input of LC filter, causing current i_1 to increase. When Q_1 is OFF, the energy stored in the inductor L maintains current flow to the load, circulating through "catch" diode D_1. The input of the LC filter is now at zero volts. i_1 decreases to its original value and the cycle repeats.

The output voltage E_o, will equal the time avefage of the voltage at the input of the LC filter :

$$E_o = E_{in}\ T_{ON}/\tau$$

where $\tau = 1/f$ .....(1.1)

The control ckt. senses and regulates Eo by controlling the duty-cycle , $d = T_{on}/\tau$. If E_{in} increases, the control circuit will cause a corresponding reduction in the duty cycle as to maintain a constant E_o

$$E_o = d E_{in} \qquad .....(1.2)$$

The output voltage is controllable from zero volts to E_{in}. The voltage stress on the series switching transtor is equal to E_{in} plus the forward drop of the commutating diode. Average current through the transistor switch is equal to the load current. Current limiting is achieved by controlling the switch duty-cycle. The Buck Regulator is very efficient for simple stepdown regulation.

Boost Regulator :

It is similar to Buck regulator except that the circuit is designed to provide an output voltage that is higher than the input voltage. This circuit is shown in fig. 1.3(b).

The Boost regulator has drawbacks in some applications. It has no inherent capability to limit current and the output voltage cannot be reduced to zero. It has a minimum value equal to the input voltage.

Buck-Boost Regulator :

The circuit for Buck-Boost regulator is shown in fig. 1.3(c) It provides both regulation and isolation, if we use transformer for L. Multiple outputs are possible with just the single device. Output voltage can be either higher or lower than the input voltage.

This circuit has two characteristics. First, the use of a transformer in the circuit creates a problem of leakage inductance. Secondly, this type of regulator generates high output dynamic impedance and may generate high output ripple. A series regulator at the output may be used to reduce impedance and ripple. This approach, of course, somewhat complicated and sacrifices some efficiency.

1.4 Performance Indices of Switching Regulators :

Input Reflected Ripple :

A dc/dc converter term which describes the voltage spike resulting from switching generated transient currents as measured at the d.c. input source.

Line Regulation :

Change in DC output voltage due to variation of input voltage with all other factors held constant, expressed as a % of the nominal d.c. output voltage. Also called source voltage effect.

Load Regulation :

Change in d.c. output voltage, due to variation of external load current with all other factors held constant : expressed as a % of the nominal d.c. output voltage. Usually the external current is varied from zero to rated maximum, also called load effect.

Overall Regulation :

The percent of output voltage change resulting from a specified change of input voltage , output load, temperature or time. The resulting specifications are line regulation, load regulation, temperature coefficient and stability.

Ripple :

The periodic AC noise component present at the power source d.c. output. Unless specified separately this specification may include random voltage noise. It is usually expressed as peak, peak to peak or RMS.

Ripple and Noise (PARD) :

AC components present in the power source d.c. output that are measured within a 10 Hz to 20 MHz bandwith. Expressed as peak, peak-to-peak, or RMS, the specification is also termed Periodic And Random Deviations.

1.5 Organization of the Thesis :

In chapter II, apart from state space modelling and averaging technique, a third method for modelling switching-converter power stages is discussed, whose starting point is the unified state space representation of the switched networks and whose end result is a complete state space description and its equivalent small signal low frequency linear circuit model.

A canonical circuit model is discussed whose fixed topology contains all the essential input-output and control properties of any d.c. to dc switching converter by which different converters can be charactorized in the form of a

table conveniently stored in a computer data bank to provide a useful tool for computer aided design and optimization.

Chapter III deals with the necessity of input filter for switching regulators, its advantages-disadvantages, and effect on performance of switching regulator are discussed. The interaction between the input filter and the control loop of switching regulators often results in loop instability, transient response and audio-signal-rejection rate etc. A small signal average model is derived to investigate these effects. Design constraints of an input filter and switching regulators system are formulated.

In chapter IV, a computer program in FORTRAN is developed to analyse the switching mode converter and the effect of input filter on its performance. Different types of input filter were taken to find out the optimum design. Their comparative performance is plotted on graphs.

In last chapter, the conclusion of this work is made and scope for further work is suggested. The state space matrices for Buck type switching regulator are given in Appendix A. Appendix B gives the fundamental approximation in the state space averaging approach . In Appendix C, Dither method is discussed to obtain pulsewidth modulator signal and its describing function.

C H A P T E R - II

MODELLING OF SWITCHING MODE CONVERTER

2.1(a) Introduction

2.1.1 Small Scale Linearization method :
State Space, Averaging, State Space averaging techniques, Assumptions and Limitations.

2.1.2 Nonlinear discrete time model.

2.1(b) State Space Representation

2.2 Averaging Technique

2.3 State Space Averaging

2.3.1 Basic State Space model
2.3.2 Linearization and Final State Space Averaged Model.
2.3.3 Circuit Realization
2.3.4 Canonical Circuit Model.

2.4 Modelling of Modulator

2.1 INTRODUCTION :

The switched mode dc-dc converter can be characterized by the three basic functional blocks : power stage, analog signal processor and digital signal pressor or duty-cycle controller, as shown in fig. 2.1.1.

The power stage process the power from input to output. The analog signal processor togetherwith the digital signal processor regulates the power flow from input to output. The output of the power stage is processed by the analog signal processor for error amplification and compensation. The output from the analog signal processor is converted into a discrete time-interval by a digital signal processor, which provides the duty-cycle control of the power switch in the power stage. Such converters can be characterized as nonlinear time varying system and have presented considerable difficulties in modelling and analysis. We call these systems as time varying since duty cycle 'd' is a function of time and varies considerably in case of large scale or transient performance. Thus during turn on interval the duty cycle increases gradually as shown in fig. 2.1.2. Similarly during the transient period duty cycle d(the ratio of T_{ON}/T_{OFF}) varies with time before it reaches to its steady state value in about 1 sec. This is necessary (i) to avoid undesired over shoot

in output response (ii) to avoid saturation of magnetic components (iii) to prevent over-voltage tripping. Partially due to the nonlinear discrete nature of such system and partially due to the rapidly evolving new circuit technology, modelling and analysis of power processing systems has been constantly lagging behind the circuit development.

The different modelling techniques can be broadly classified into two categories : (1) small-scale linearization technique [1], [2] and (2) non-linear discrete time model [3] [4].

Small-scale Linearization Method :

In this technique the model of the converter is linearized about its operating point with the following assumptions :

(a) Duty cycle d is constant and only small perturbations are allowed.

(b) Inductor current is in continuous conduction mode.

(c) There are only small changes in input voltage or load.

(d) The performance is evaluated over single repetition period 'T' by averaging over two switched intervals T_d and $T(1-d)$.

The techniques in this category are averaging technique, state space modelling and state space averaging technique.

(1) State Space Modelling :

This approach remains strictly in the domain of equation manipulations and hence relies heavily on numerical methods and computerized implementations. Its primary advantage is in the unified description of all power stages regardless of the type (Buck, Boost, Buck-Boost or any other variation) through utilization of the exact state space equations of the two switched models.

(2) Averaging Technique :

This technique is based on equivalent circuit manipulations, resulting in a single equivalent linear circuit model of the power stage. This has the distinct advantage of providing the circuit designer with physical insight into the behaviour of the original switched circuit.

(3) State Space Averaging Technique :

This method bridges the gap between the state space technique and the averaging technique of modelling power stages. This model offers the advantages of both the previous methods, the general unified treatment of the state space approach, as well as an equivalent linear circuit model as its final result.

As per the assumptions, the above techniques are valid only when the inductor current is in a continuous conduction mode (explained in the next paragraph) and can not be applied for discontinuous conduction mode.

In each cycle of the converter operation, two power stage topologies can be defined. One is for the ON time interval when the power switch is "ON" and the commutating diode is "OFF" and the other is for the off time interval when the power switch is OFF and the diode is ON. These two power stage circuit topologies for Buck type dc-dc switched converter are shown in fig. 2.1.3 (a) & (b) respectively.

As we know if L is equal to or greater than the critical inductance, the current through the inductor L is always greater than zero as shown in fig. 2.1.3(c). From this figure it is clear that in this case the period of each switching cycle can be clearly divided into two time intervals. T_{ON} (switch is ON and diode is OFF) and T_{OFF} (switch is OFF and diode is ON). This mode is called continuous conduction mode and the state space averaging technique is limited to this mode only.

But if L is less than the critical inductance, a third state exists when inductor current becomes zero. During this time interval, both the power switch and the diode are in the "OFF" state. The circuit topology for this time interval consists of only the filter capacitor and the load as shown in fig. 2.1.4(a).

The inductor current for this case is shown in Fig. 2.1.4(b). In this case the current through the inductor reduces to zero and resides at zero for a time interval T_{off2}. This is called non-continuous conduction mode. To analyse such systems we have to go for non-linear discrete time model.

The linearized models as explained above are limited only to analyzing the small signal steady state operation when the duty cycle signal can be regarded as a constant. However in most applications, the converter is frequently subjected to lar signal step line/load transients, subsequently varying the duty cycle ratio to maintain input-output regulation. Due to the time varying and switching nature of the system, it is impossible to deduce the large signal performances from the above small signal linear models. Therefore to study such systems we have to go for non-linear discrete time model.

Non-linear discrete time model :

The limitations of small scale linearization method can be overcome by this nonlinear discrete time model. This method is suitable for :

(a) Generalized converters

(b) Large-scale performance

(c) Transient response

(d) Small-scale linearization can also be done.

(e) Non-continuous conduction mode.

(f) Stability can also be predicted.

(g) Large frequency range.

(h) Audio-susceptibility can be predicted.

This method is discussed in [3] & [4] in detail. In this technique, system is characterized by three piece-wise linea r state space equations. The third equation represents th behaviour of the system when inductor current is zero. A non-linear recurrent time domain equation is derived that characterizes the converter behaviour exactly. The approach discussed in [4] is generalized to include all types of power stages, all types of duty cycle, controllers with single or multiple feedback loops and both continuous and discontinuous inductor current operations. Here we will discuss small-scale linearization methods in detail.

State Space Representation :

Voltage across the capacitor and current through the inductor are selected as the state variables **X** of the system. But state variables can be choosen differently depending upon individual problem. In general **X** is an n x 1 column vector. The system representation for continuous conduction mode is

$$\dot{x} = A_1 x + b_1 u \quad \text{during } T_{on} \qquad (2.1.1)$$

$$\dot{x} = A_2 x + b_2 u \quad \text{during } T_{OFF} \qquad (2.1.2)$$

The column vector **U** is an (m x 1) input vector, containing the input voltage E_{in}, the reference E_{ref}, the

saturation voltage drop across the power transistor and the forward voltage drop across the diode etc. The n x n matrices A_1 and A_2 and the n x m matrices b_1 & b_2 are constant matrices represented by the various circuit parameters. These matrices for Buck type stage are shown in the Appendix A.

The converts, which are basically nonlinear switching circuits are accurately described by the different equations represented by (2.1.1) & (2.1.2). The solution of the linear differential equations can be expressed by the following state transition equation

$$x(t+T) = \Phi_i(T)x(t) + D_i(T)u \qquad \ldots (2.1.3)$$

where

$$\Phi i(T) = e^{A_i T} \quad ; \; i = 1, 2$$

$$Di(T) = e^{A_i T} \left[\int_0^T e^{-A_i S} \, ds \right] bi \quad ; \; i=1,2 \qquad \ldots(2.1.4)$$

$\Phi i(T)$ and $Di(T)$ for any given T can be computed either analytically or numerically. If they are computed numerically, the following Taylor series expansion is used :

$$e^{A_i T} = I + A_i T + \frac{(A_i T)^2}{2!} + \frac{(A_i T)^3}{3!} + \ldots \; ; i=1,2 \qquad \ldots(2.1.5$$

2.2. AVERAGING TECHNIQUE

This technique is based on Equivalent Circuit manipulation and is discussed in [1]. Here non-linear circuits are converted into single equivalent linear circuit by averaging the forcing functions. Here we will develop these equivalent linear circuits for the three basic power stages, Buck, Boost and Buck-Boost.

First we will take Boost power stage circuit. The general circuit and equivalent circuit of this power stage are shown in Fig.2.2.1(a) and (b) respectively. Duty cycle d(t) is defined as :

$$d(t) = \begin{cases} 1 & \text{Switch closed} \\ 0 & \text{Switch open} \end{cases} \qquad \ldots(2.2.1)$$

Since thn state variable response times are always much greater than the nominal switching period T, therefore the forcing functions (sources) may be averaged over a time interval T in the following manner :

$$\langle d \rangle (t) = \frac{1}{T} \int_{t-T}^{t} d(x)\,dx \qquad \ldots(2.22)$$

With this approximation, the time averaged model of the Boost power stage is drawn in Fig. 2.2.1(c). In these circuits circles are used to denote independent sources, whereas squares are used for dependent generators. Similarly averaged models of Buck power stage and Buck Boost power stage are developed in Fig. (2.2.2) and Fig. (2.2.3) respectively. Since generator gains of Buck power stage averaged model are unity, this wss further simplified to a linear circuit shown in Fig. 2.2.2(c).

Analysis of Response to Source Variations :

Now we will assume t.at the average duty ratio is constant and we take D as numerically equal to the dc average of d(t) i.e.

$$\langle d \rangle (t) = D \qquad \ldots (2.23)$$

When we substitute this assumption in average model of Buck power stage of Fig. 2.2.2(c) we get equivalent linear circuit shown in Fig. 2.2.4(a). This relates unspecified source variations to the corresponding output variations for the Buck power stage .

Similarly for Boost and Buck-Boost power stages we define a complementary duty ratio D' as

$$D' \equiv 1 - D \qquad \ldots (2.2.4)$$

The Averaged Boost and Buck-Boost Power Stage models after substitution of Eq. (2.2.4) are shown in Fig. 2.2.5(a) and 2.2.6(a) respectively. To eliminate dependent generators, constant generator gains must be unity. For this we divide voltage sources and impedance values by D', so that the current $\langle i \rangle$ will remain unchanged. Similarly to maintain $\langle v \rangle$ unchanged, we divide current generator gain by D' and multiply impedances by D'. The circuits, after normalizing the constant generator gains to unity, of Boost and Buck-Boost models are shown in Fig. 2.2.5(b) and Fig. 2.2.6(b). These circuits are further simplified to Fig. 2.2.5(c) and Fig. 2.2.6(c). The averaged circuits in Fig. 2.2.4(a), 2.2.5(c) and 2.2.6(c) are equivalent linear circuits for Buck, Boost and Buck-Boost power stages respectively for source variations and constant control. These circuits are useful for analysis of either transient or frequency responses caused by variations in the source voltage.

Analysis of Response to Control Variations:

We will now consider the situation when the averaged source voltage is constant

$$\text{i.e. } \langle v_s \rangle (t) = V_s \qquad \ldots (2.2.5)$$

and the averaged duty ratio $\langle d \rangle$ is fluctuating with time. Using this substitution in Average model of Buck power stage of

Fig. 2.2.2(c), we get equivalent linear circuit shown in Fig. 2.2.4(b). But when this substitution of Eq. (2.2.5) is applied in Averaged models of Boost Fig. 2.2.1(c) and Buck-Boost Fig. 2.2.3(c), these models are nonlinear for variations of the duty ratio and therefore a different approach is required.

For this approach we consider the control perturbation

$$\text{i.e. } \langle d \rangle (t) = D + \hat{d}(t) \qquad \ldots(2.2.6)$$

where $\hat{d}$ is a time varying perturbation of the duty ratio D.

$$\begin{aligned} \langle 1-d \rangle (t) &= 1 - [D + \hat{d}(t)] \\ &= 1 - D - \hat{d}(t) \\ &= D' - \hat{d}(t) \qquad \ldots(2.2.7) \end{aligned}$$

The effect on state variables due to control perturbation may be expressed as :

$$\langle v \rangle (t) = V + \hat{v}(t) \qquad \ldots(2.2.8)$$

$$\langle i \rangle (t) = I + \hat{i}(t) \qquad \ldots(2.2.9)$$

When the above perturbations are substituted in Fig. 2.2.1(c), the equivalent circuit of the averaged boost power stage becomes as shown in Fig. 2.2.7(a). To find $\hat{v}$ in terms of $\hat{d}$ we split this circuit Fig. 2.2.7(a) into unperturbed values (steady state equivalent circuit) Fig. 2.2.7(b) and perturbed values as in Fig. 2.2.7(c). This circuit can be linearized by neglecting second order terms $\hat{d}\hat{v}$ and $\hat{d}\hat{i}$ as in Fig. 2.2.8(a). After separating dependent and independent generators, this circuit becomes as in Fig. 2.2.8(b).

This circuit can further be simplified by normalizing the gains to unity as in Fig. 2.2.8(c). Fig. 2.2.8(d) shows the final equivalent circuit for variation for Boost power stage model when the averaged source voltage is constant.

The steady state equivalent circuit of Fig. 2.2.7(b) is simplified in Fig. 2.2.9. The relationship between $\hat{d}$ and $\hat{v}$ can not be obtained from Fig. 2.2.8(c) directly, due to the presence of two generators. But since this circuit is linear, Laplace transforms can be manipulated using Thevenin and Nortons equivalents to combine the generators into the single source as shown in Fig. 2.2.10.

Fig. 2.2.9(b) and Fig. 2.2.10 show the equivalent circuits of the averaged boost power stage model for small control variations and constant source for steady state and linearized for variations respectively.

Some procedure is applied for Buck-Boost power stage. When the perturbation from Eqn. (2.2.6) to (2.2.9) are substituted in Fig. 2.2.3(c), the Buck-Boost power stage model becomes as shown in Fig. 2.2.11. This circuit may be simplified as in the case of Boost power stage. The steady state equivalent circuit and its reduction is shown in Fig. 2.2.12. Similarly circuit for variations is shown in Fig. 2.2.13. Fig. 2.2.13(d) represents the equivalent linear circuit for variations for Buck-Boost power stage. As in the case of Boost power stage, since the circuit is linear, Laplace Transform can

be obtained using Thevenin and Norton equivalents to combine the generators into the single source and final linear circuit is shown in Fig. 2.2.14.

Since there is no capacitor current or Inductor voltage in the steady state, the static source to output gain of each power stage configuration can easily be derived from the averaged power stage models with static conditions :

$$\langle v_s \rangle (t) = V_s$$

$$\langle d \rangle (t) = D$$

From Averaged Buck Power stage model of Fig. 2.2.2(c), with above conditions

$$\frac{V}{DV_s} = \frac{R}{R+R_1}$$

or
$$\frac{V}{V_s} = \frac{DR}{R + R_1} \qquad \ldots(2.2.10)$$

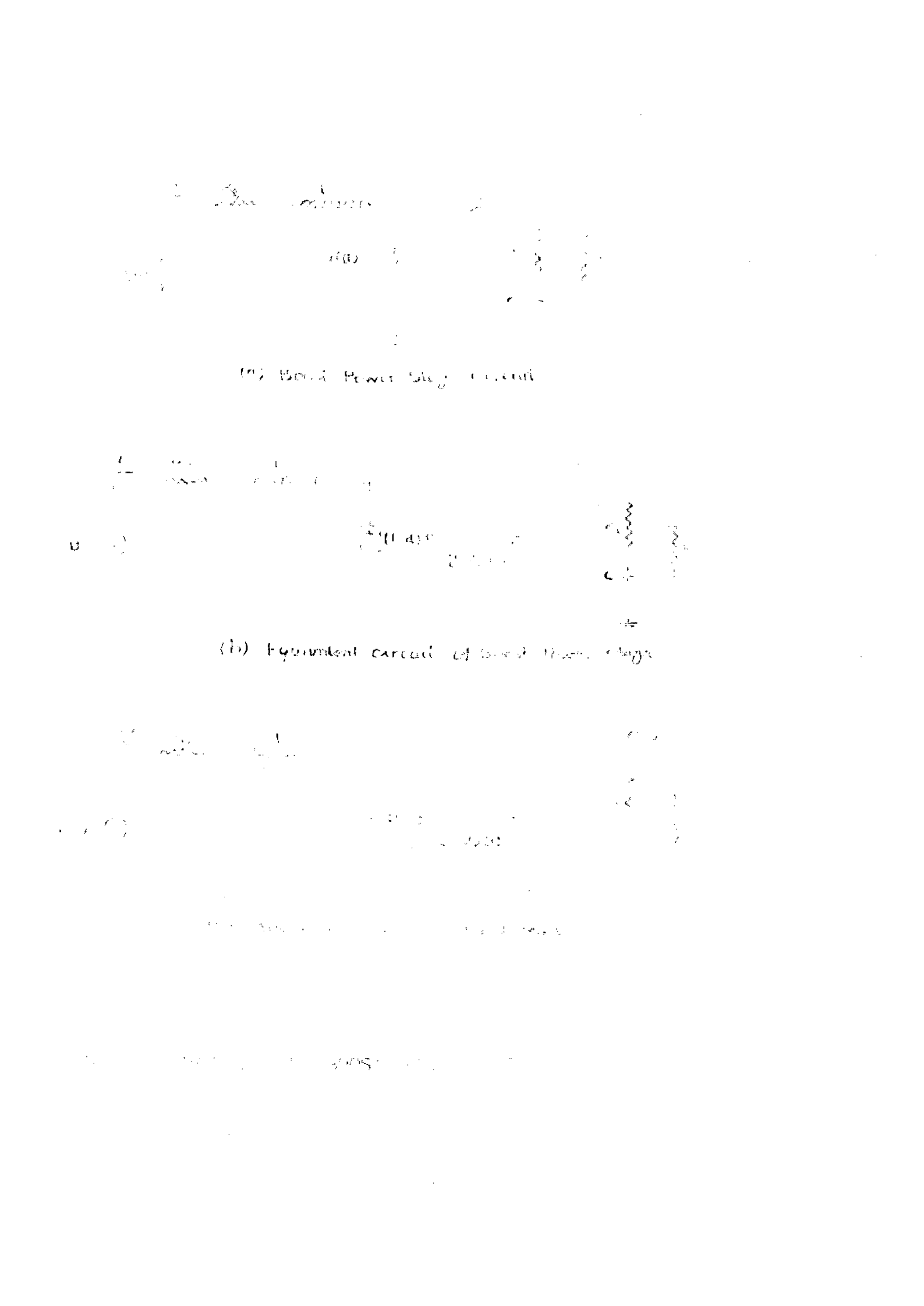
For steady state Boost Power stage model of Fig. 2.2.9

$$\frac{V}{\frac{1}{D} V_s} = \frac{D'R}{D'R + \frac{R_1}{D'}}$$

or
$$\frac{D'V}{V_s} = \frac{(D')^2 R}{(D')^2 R + R_1}$$

or
$$\frac{V}{V_s} = \frac{D'R}{(D')^2 R + R_1} \qquad \ldots(2.2.11)$$

For steady state Buck-Boost power stage model of Fig. 2.2.12(c)



$D'R_c$

$$\frac{V}{\frac{D}{D'} V_s} = \frac{D'R}{D'R + \frac{R_1}{D'}}$$

or

$$\frac{V}{V_s} = \frac{DD'R}{(D')^2R + R_1} \qquad \ldots (2.2.12)$$

Thus the Averaging technique characterizes the low frequency response of switched power stage. The above analysis reveals one interesting thing that when we consider averaged control duty cycle <d> fluctuating with time, the averaged Buck power stage circuits becomes linear whereas averaged Boost and Buck-Boost models are nonlinear for which perturbations were considered.

2.3. STATE-SPACE AVERAGING

The previous techniques, state space modelling [6] and Averaging technique [1] have little correlation between each other. The first approach is in the domain of equation manipulation whereas Averaging technique is based on equivalent circuit manipulation.

In this section the state-space averaging method is developed first in general for any dc- to - dc switching converter, and then demonstrated in detail for the particular case of the boost power stage in which parasitic effects (esr of the capacitor and series resistance of the inductor) are included General equations for both steady state (dc) and dynamic performance (ac) are obtained, from which important transfer functions are derived and also applied to the special case of the boost

power stage.

Basic State-Space Averaged Model :

The basic dc- to - dc level conversion function of switching converters is achieved by repetitive switching between two linear networks. We assume that the circuit operates in the continuous conduction mode, therefore, there are only two different 'states' of the circuit. If we take a boost power stage circuit shown in fig. 2.3.1(a), for analysis, the two linear circuit models, when switch is ON and when switch is OFF can be represented as in Fig. 2.3.1(b) & (c) respectively.

These two states may be represented by the corresponding set of state-space equations :

(i) Interval Td

$$\dot{x} = A_1 x + b_1 v_g$$
$$y_1 = C_1^T x$$

(ii) Interval Td'

$$\dot{x} = A_2 x + b_2 v_g$$
$$y_2 = C_2^T x \qquad \ldots(2.3.1)$$

where Td : interval when the switch is ON

T(1-d) $\equiv$ Td' : interval when the switch is OFF, as shown in fig. 2.3.2.

The objective now is to replace these two state space descriptions of the two successive phases of the switching cycle T by a single state space description which represents approximately the behaviour of the circuit across the whole period T. For this we take the average of both dynamic and static equations for the two switched intervals (2.3.1), in the following manner :

$$\dot{x} = d\,(A_1 x + b_1 v_g) + d'\,(A_2 x + b_2 v_g)$$

$$y = d.y_1 + d'.y_2 \qquad \ldots(2.3.2)$$

$$= (dc_1^T + d'c_2^T)\,x$$

After rearranging (2.3.2) we obtain the basic averaged state space description over a single period T :

$$\dot{x} = (dA_1 + d'A_2)\,x + (db_1 + d'b_2)\,v_g \qquad \ldots(2.3.3)$$

$$y = (dC_1^T + d'C_2^T)\,x$$

In essence, comparison between (2.3.3) and (2.3.1) shows that the system matrix of the averaged model is obtained by taking the average of two switched model matrices A_1 and A_2, its control is the average of two control vectors b_1 and b_2, and its output is the average of two outputs y_1 and y_2 over a period T.

The justification and the nature of the approximation in substitution for the two switched models of (2.3.1) by averaged model (2.3.3) is indicated in Appendix B.

If we now assume that the duty ratio d is constant from cycle to cycle, namely, d = D (steady state dc duty ratio) we get :

$$\dot{x} = Ax + bv_g \qquad \ldots(2.3.4)$$

$$y = C^T x$$

where
$$A = DA_1 + D'A_2$$
$$b = Db_1 + D'b_2 \qquad \ldots(2.3.5)$$
$$C^T = DC_1^T + D'C_2^T$$

Since (2.3.4) is a linear system, superposition holds and it can be perturbed as in Averaging technique by introduction o line voltage variations $\hat{v}_g$ as $v_g = V_g + \hat{v}_g$, where V_g is the dc line input voltage, causing a corresponding perturbation in the state vector $x = X + \hat{x}$, where X is the dc value of the state vector and $\hat{x}$ is the superimposed ac perturbation. Similarly, $y = Y+\hat{y}$. Putting these value in (2.3.4) :

$$\dot{\hat{x}} = A(X+\hat{x}) + b(V_g + \hat{v}_g)$$

$$Y+\hat{y} = C^T (X+\hat{x})$$

Or $$\dot{\hat{x}} = AX + bV_g + A\hat{x} + b\hat{v}_g \qquad \ldots(2.3.6)$$

$$Y+\hat{y} = C^TX + C^T\hat{x}$$

Separating steady state (dc) part from the dynamic (ac) part, we get :

Steady state (dc) model :

$$AX + bV_g = 0 \quad ; \quad Y = C^TX$$

or $$X = -A^{-1}bV_g \quad ; \quad Y = -C^TA^{-1}bV_g \qquad \ldots(2.3.7)$$

dynamic (ac) model :

$$\dot{\hat{x}} = A\hat{x} + b\hat{v}_g$$

$$\hat{y} = C^T\hat{x} \qquad \ldots(2.3.8)$$

From the ac model, the line voltage to state vector transfer functions can be easily derived as :

$$s\hat{x}(s) = A\hat{x}(s) + b\,\hat{v}_g(s) \qquad \ldots(2.3.9)$$

$$\hat{y}(s) = C^T\hat{x}(s)$$

or $$\frac{\hat{x}(s)}{\hat{v}_g(s)} = (sI-A)^{-1}b \qquad \ldots(2.3.10)$$

$$\frac{\hat{y}(s)}{\hat{v}_g(s)} = C^T(sI-A)^{-1}b$$

We now will include the duty ratio modulation effect into the basic averaged model (2.3.3).

Perturbation :

Now suppose the duty ratio changes from cycle to cycle, that is,

$$d(t) = D + \hat{d}$$

where $\hat{d}$ is a superimposed (ac) variation.

Put these values in (2.3.3) :

$$\dot{\hat{x}} = \{(D+\hat{d})A_1 + (1-D-\hat{d})A_2\}(X+\hat{x}) + [(D+\hat{d})b_1 + (1-D-\hat{d})b_2](V_g+\hat{v}_g)$$

$$Y+\hat{y} = \{(D+\hat{d})C_1^T + (1-D-\hat{d})C_2^T\}(X+\hat{x})$$

Or $$\dot{\hat{x}} = (DA_1+D'A_2)X + (DA_1+D'A_2)\hat{x}+(A_1-A_2)\hat{d}X + (A_1-A_2)\hat{d}\hat{x}$$

$$+ (Db_1+D'b_2)V_g + (Db_1 + D'b_2)\hat{v}_g + (b_1-b_2)\hat{d}V_g+(b_1-b_2)\hat{d}\hat{v}_g$$

$$Y+\hat{y} = (DC_1^T + D'C_2^T)(X+\hat{x}) + (C_1^T - C_2^T)\hat{d}(X+\hat{x})$$

or $$\dot{\hat{x}}=AX+bV_g + A\hat{x}+b\hat{v}_g + [(A_1-A_2)X +(b_1-b_2)V_g]\hat{d}+ [(A_1-A_2)\hat{x}+(b_1-b_2)\hat{v}_g]\hat{d}$$

dc.term; line variation; duty ratio variation; nonlinear second order term

$$Y+\hat{y} = C^T X + C^T \hat{x} + (C_1^T - C_2^T)\, x\hat{d} + (C_1^T - C_2^T)\hat{x}\,\hat{d} \quad \ldots(2.3.11)$$

d.c. term; a.c. term; a.c. term; nonlinear term

The above perturbed state space eugations are nonlinear owing to the presence of the product of the two time dependent quantities $\hat{x}$ and $\hat{d}$.

Linéarization and Final State Space Averaged Model :

Small Signal Approximation : Variations in the steady state values are negligible compared to the steady state values themselves, i.e.

$$\frac{\hat{v}_g}{V_g} << 1 \quad ; \quad \frac{\hat{d}}{D} << 1 \quad ; \quad \frac{\hat{x}}{X} << 1. \qquad \ldots(2.3.12)$$

Using above approximation we can neglect second order terms and we get

$$\dot{\hat{x}} = AX + bV_g + A\hat{x} + b\hat{v}_g + [(A_1-A_2)X + (b_1-b_2)V_g]\,\hat{d}$$

$$Y+\hat{y} = C^T X + C^T \hat{x} + (C_1^T - C_2^T) X\,\hat{d}$$

which is a linear system.

Separating steady state (d.c.) and dynamic (a.c.) part we

Steady state (d.c.) model :

$$X = -A^{-1} b V_g \quad ; \quad Y = C^T X \qquad \ldots(2.3.13)$$

$$= C^T A^{-1} b V_g$$

Dynamic (ac) model :

$$\dot{\hat{x}} = A\hat{x} + b\hat{v}_g + [(A_1-A_2)X + (b_1-b_2)V_g]\,\hat{d} \qquad \ldots(2.3.14)$$

$$\hat{y} = C^T \hat{x} + (C_1^T - C_2^T) X \hat{d}$$

Equations (2.3.13) and (2.3.14) represent the small signal low frequency model of any dc to dc switching converter working in the continuous conduction mode.

Boost Power Stage with Parasitics : We will now illustrate an example of Boost Power stage. With assumption of ideal switches, the two switched models of Fig. (2.3.1)(a) are shown in fig. 2.3.1(b) & (c). We take inductor current i and capacitor voltage v as state variables, i.e.

$$x = \begin{bmatrix} i \\ v \end{bmatrix}$$

Interval Td : Fig. 2.3.1(b)

$$v_g = R_1 i + L.\frac{di}{dt} \qquad y_1 = R.\ \frac{v}{R+R_c} \qquad v = -\frac{1}{C}\int \frac{v}{R+R_c}\,dt$$

$$\text{or} \quad \frac{di}{dt} = -\frac{R_1}{L} i + \frac{v_g}{L} \qquad \text{or} \quad \frac{dv}{dt} = -\frac{1}{C}\,\frac{v}{R+R_c}$$

$$\therefore \begin{bmatrix} \dot{i} \\ \dot{v} \end{bmatrix} = \begin{bmatrix} -\frac{R_1}{L} & 0 \\ 0 & -\frac{1}{C(R+R_c)} \end{bmatrix} \begin{bmatrix} i \\ v \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_g$$

$$\dot{x} = A_1 x + b_1 v_g$$

$$y_1 = C_1^T x$$

$$\therefore A_1 = \begin{bmatrix} -\frac{R_1}{L} & 0 \\ 0 & -\frac{1}{(R+R_c)C} \end{bmatrix} \quad b_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \quad C_1^T = \begin{bmatrix} 0 & \frac{R}{R+R_c} \end{bmatrix}$$

...(2.3.15)

Interval Td' Fig. 2.3.1(c)

$$i_1 = \frac{y_2 - v}{R_c}$$

$$y_2 = R(i-i_1) = R\left(i - \frac{y_2 - v}{R_C}\right)$$

$$= Ri - \frac{R}{R_C} y_2 + \frac{R}{R_C} v$$

or $$y_2 = \frac{RR_C}{R + R_C} i + \frac{R}{R+R_C} v = (R \parallel R_C) i + \frac{R}{R+R_C} v$$

$$v_g = R_1 i + L. \frac{di}{dt} + y_2$$

$$= R_1 i + L. \frac{di}{dt} + (R \parallel R_C) i + \frac{R}{R+R_C} v$$

or $$\frac{di}{dt} = - \frac{R_1 + R \parallel R_C}{L} i - \frac{R}{L(R+R_C)} v + \frac{1}{L} v_g$$

$$v = - \frac{1}{C} \int -i_1 dt$$

$$= \frac{1}{C} \int \frac{(R \parallel R_C)\ i + \frac{R}{R+R_C} v - v}{R_C} dt$$

or $$\frac{dv}{dt} = \frac{1}{C} \frac{R \parallel R_C}{R_C} i - \frac{1}{C(R+R_C)} v$$

$$\therefore \begin{bmatrix} \dot{i} \\ \dot{v} \end{bmatrix} = \begin{bmatrix} - \frac{R_1 + R \parallel R_C}{L} & - \frac{R}{L(R+R_C)} \\ \frac{R}{(R+R_C)C} & - \frac{1}{(R+R_C)C} \end{bmatrix} \begin{bmatrix} i \\ v \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_g$$

$$\therefore A_2 = \begin{bmatrix} - \frac{R_1 + R \parallel R_C}{L} & - \frac{R}{L(R+R_C)} \\ \frac{R}{C(R+R_C)} & - \frac{1}{C(R+R_C)} \end{bmatrix} \quad b_2 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \quad \therefore b_1 = b_2 = b$$

$$C_2^T = \begin{bmatrix} \frac{RR_C}{R+R_C} & \frac{R}{R+R_C} \end{bmatrix} \qquad \ldots(2.3.16)$$

Substitute these values in (2.3.5) we get

$$A = DA_1 + (1-D)\,A_2$$

$$= D(A_1 - A_2) + A_2$$

$$A = D\begin{bmatrix} \frac{R_c \| R}{L} & \frac{R}{L(R+R_c)} \\ -\frac{R}{(R+R_c)C} & 0 \end{bmatrix} + \begin{bmatrix} -\frac{R_1+R_c \| R}{L} & -\frac{R}{L(R+R_c)} \\ \frac{R}{(R+R_c)C} & -\frac{1}{(R+R_c)C} \end{bmatrix}$$

$$= \begin{bmatrix} -\frac{R_1}{L}(1-D) & \frac{R_c \| R}{L} & -\frac{R}{L(R+R_c)}(1-D) \\ \frac{R}{(R+R_c)C}(1-D) & & -\frac{1}{(R+R_c)C} \end{bmatrix}$$

$$C^T = DC_1^T + (1-D)\,C_2^T$$

$$= D(C_1^T - C_2^T) + C_2^T$$

$$= D\begin{bmatrix} -\frac{RR_c}{R+R_c} & 0 \end{bmatrix} + \begin{bmatrix} \frac{RR_c}{R+R_c} & \frac{R}{R+R_c} \end{bmatrix} = \begin{bmatrix} \frac{RR_c(1-D)}{R+R_c} & \frac{R}{R+R_c} \end{bmatrix}$$

$$b = b_1 = b_2 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}$$

Steady State (d.c.) model :

From eq. (2.3.13)

$$X = -A^{-1} b\, V_g$$

$$|A| = \frac{R_1+(1-D)R_c \| R}{LC(R+R_c)} + \frac{R^2(1-D)^2}{LC(R+R_c)^2} = \frac{(R+R_c)\ R_1+(1-D)R_c \| R + R^2(1-D)}{LC\ (R+R_c)^2}$$

$$A^{-1}b = \frac{LC\ (R+R_c)}{R_1+(1-D)R_c \| R + \frac{R^2(1-D)^2}{R+R_c}} \begin{bmatrix} -\frac{1}{C(R+R_c)} & \frac{R(1-D)}{L(R+R_c)} \\ -\frac{R(1-D)}{C(R+R_c)} & -\frac{R_1+(1-D)R_c \| R}{L} \end{bmatrix} \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}$$

$$= \frac{LC\ (R+R_c)}{R_1+(1-D)^2R + D(1-D)R_c \| R} \begin{bmatrix} -\frac{1}{LC(R+R_c)} \\ -\frac{R(1-D)}{LC(R+R_c)} \end{bmatrix}$$

$$X = \begin{bmatrix} I \\ V \end{bmatrix} = -A^{-1}bV_g = \frac{V_g}{R'} \begin{bmatrix} 1 \\ R(1-D) \end{bmatrix}$$

where $R' = R_1 + (1-D)^2 R + D(1-D) R_c \| R$

$$Y = -C^T A^{-1} b V_g = \frac{V_g}{R'} \begin{bmatrix} \frac{RR_c(1-D)}{R+R_c} & \frac{R}{R+R_c} \end{bmatrix} \begin{bmatrix} 1 \\ R(1-D) \end{bmatrix}$$

$$\text{or} = \frac{V_g}{R'} \left[\frac{RR_c(1-D)}{R+R_c} + \frac{R^2\ (1-D)}{R+R_c} \right]$$

$$= \frac{V_g}{R'} R\ (1-D) \qquad \ldots(2.3.17)$$

where I is the dc inductor current, V is the dc capacitor voltage, and **y** is the dc output voltage.

Dynamic (ac small signal model) :

From eq. (2.3.1.4)

$$\dot{\hat{x}} = \frac{d}{dt}\begin{bmatrix}\hat{i}\\ \hat{v}\end{bmatrix} = \begin{bmatrix} -\dfrac{R_1 + (1-D)R_c \| R}{L} & -\dfrac{R(1-D)}{L(R+R_c)} \\ \dfrac{R(1-D)}{(R+R_c)C} & -\dfrac{1}{(R+R_c)C}\end{bmatrix}\begin{bmatrix}\hat{i}\\ \hat{v}\end{bmatrix} + \begin{bmatrix}\frac{1}{L}\\ 0\end{bmatrix}\hat{v}$$

$$+ \frac{V_g \hat{d}}{R'}\begin{bmatrix} \dfrac{R_c \| R}{L} & \dfrac{R}{L(R+R_c)} \\ -\dfrac{R}{(R+R_c)C} & 0\end{bmatrix}\begin{bmatrix}1\\ (1-D)R\end{bmatrix}$$

$$= \begin{bmatrix} -\dfrac{R_1+(1-D)R_c \| R}{L} & -\dfrac{R(1-D)}{L(R+R_c)} \\ \dfrac{R(1-D)}{(R+R_c)C} & -\dfrac{1}{(R+R_c)C}\end{bmatrix}\begin{bmatrix}\hat{i}\\ \hat{v}\end{bmatrix} + \begin{bmatrix}\frac{1}{L}\\ 0\end{bmatrix}\hat{v}_g$$

$$+ \begin{bmatrix} \dfrac{R}{L} & \dfrac{D'R + R_c}{R+R_c} \\ & -\dfrac{R}{(R+R_c)C}\end{bmatrix}\frac{V_g \hat{d}}{R'}$$

$$\hat{y} = \begin{bmatrix}(1-D)(R_c \| R) & \dfrac{R}{R+R_c}\end{bmatrix}\begin{bmatrix}\hat{i}\\ \hat{v}\end{bmatrix} + \begin{bmatrix}-R \| R_c & 0\end{bmatrix}\begin{bmatrix}1\\ R(1-D)\end{bmatrix}\frac{V_g}{R'}\hat{d}$$

$$= \begin{bmatrix}(1-D)R_c \| R & \dfrac{R}{R+R_c}\end{bmatrix}\begin{bmatrix}\hat{i}\\ \hat{v}\end{bmatrix} - V_g \frac{R \| R_c}{R'}\hat{d} \qquad \ldots(2.3.18)$$

If we consider dc voltage transformation ratio from eq(2.3.1) we get

$$\frac{V}{V_g} = \frac{Y}{V_g} = \underbrace{\frac{1}{1-D}}_{\substack{\text{ideal} \\ \text{dc gain}}} \quad \underbrace{\frac{(1-D)^2 R}{(1-D)^2 R + R_1 + D(1-D) R_c \| R}}_{\text{Correction factor}} \qquad \ldots(2.3.19)$$

If all parasitics are zero i.e. $R_1 = 0$; $R_c = 0$

then dc voltage gain = $\frac{1}{1-D}$ or $\frac{1}{D'}$

And in presence of parasitics, this gain is slightly reduced since correction factor is less than 1.

From the dynamic model (2.3.18) we can find the duty ratio to output and line voltage to output transfer functions.

Circuit Realization :

By the basic averaged model given by eq. (2.3.3) we can find a useful circuit realization for any specific converter. Here we will demonstrate this circuit realization for the same boost power stage example:

Put the values of A_1, A_2, C_1 & C_2 in eqn. (2.3.3) we get

$$\begin{bmatrix} \frac{di}{dt} \\ \\ \frac{dv}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_1 + d'(R_c \| R)}{L} & -\frac{d'R}{L(R+R_c)} \\ \\ \frac{d'R}{(R+R_c)C} & -\frac{1}{(R+R_c)C} \end{bmatrix} \begin{bmatrix} i \\ \\ v \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ \\ 0 \end{bmatrix} v_g \qquad \ldots(2.3.20)$$

$$y = \begin{bmatrix} d'(R_c \| R) & \frac{R}{R+R_c} \end{bmatrix} \begin{bmatrix} i \\ \\ v \end{bmatrix}$$

$$\text{or} \quad y = d' \frac{RR_c}{R+R_c} i + \frac{R}{R+R_c} v$$

Capacitor voltage

$$v = \frac{R+R_c}{R} y - (1-d)R_c i$$

$$\text{or} \quad \begin{bmatrix} i \\ v \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -d'R_c & \frac{R+R_c}{R} \end{bmatrix} \begin{bmatrix} i \\ y \end{bmatrix} \qquad \ldots(2.3.21)$$

Substitute eqn. (2.3.21) in eq. (2.3.20) we get

$$\begin{bmatrix} \frac{di}{dt} \\ \frac{dv}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-(R_1+d'(R_c \| R)}{L} + \frac{d'd'RR_c}{L(R+R_c)} & -\frac{d'}{L} \\ \frac{d'R}{(R+R_c)C} + \frac{d'R_c}{(R+R_c)C} & \frac{1}{RC} \end{bmatrix} \begin{bmatrix} i \\ y \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_g$$

$$\text{or} \quad \begin{bmatrix} L.\frac{di}{dt} \\ C\ \frac{dv}{dt} \end{bmatrix} = \begin{bmatrix} -(R_1+dd'(R_c \| R) & -d' \\ d' & -\frac{1}{R} \end{bmatrix} \begin{bmatrix} i \\ y \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \end{bmatrix} v_g \qquad \ldots(2.3.22)$$

From the eqn. (2.3.22) we can reconstruct the circuit as in Fig. 2.3.3(a).

In this circuit realization we have taken non-perturbed values and therefore this model is valid for d.c. regime only.

The two dependent generators can be treated as an ideal d':1 transformer as shown in Fig. 2.3.3(b).

The circuit model of Fig. 2.3.3(b) reduces to switched models in fig. 2.3.1(b) and 2.3.1(c) for d=1 & d=0 respectively. If d is constant i.e. d = D, the dc regime can be found easily by considering L to be short and C to be open. Hence the dc voltage gain (2.3.19) can be directly seen from fig. (2.3.3(b).

In the ideal d':1 transformer, turn ratio changes when the duty ratio is a function of time, d(t). It is through this ideal transformer that the actual controlling function is achieved when the feedback loop is closed.

The Canonical Circuit Model :

We know that the general final state space averaged model defined in eq. (2.3.13) & (2.3.14) gives complete description of the system behaviour. But in usual practice we need a circuit model which describes the input-output and control properties of the system. The Block diagram of such model is shown in Fig. 2.3.4 i.e. from State space averaged model we will derive a circuit model which directly gives the input - output and control properties and is called as 'Canonical Circuit Model'.

Although in deriving this Canonical Model from State space averaged model, some information about the internal behaviour of some of the states will certainly be lost, but there are many advantages of this Canonical model, specially in computerization. Since Canonical Circuit Model contains

all the essential input-output and control properties of any dc - to - dc switching converter, regardless of its detailed configuration, therefore by this model different converters can be characterized in the form of a table and which can be conveniently stored in a computer data bank, which is very useful for Computer aided design and optimization.

A new Canonical Circuit Model is shown in Fig. 2.3.5. Any switching convert input-output model, regardless of its detailed configuration could be represented in this form.

Different converts are represented simply by an appropriate set of formulas for the four elements e(s), j(s), μ, He(s in the general equivalent circuit.

Derivation of the Canonical Model through State Space :

We will reproduce general state space averaged model (2.3.13) & (2.3.14) here :

$$X = -A^{-1}b\ V_g \quad ; \qquad Y = C^T X$$

$$= -C^T A^{-1} b V_g$$

$$\dot{\hat{x}} = A\hat{x} + b\hat{v}_g + \left[(A_1-A_2)X + (b_1-b_2)V_g\right] \hat{d}$$

$$\hat{y} = C^T\hat{x} + (C_1^T - C_2^T)\ X\ \hat{d}$$

Taking Laplace Transform we will get :

$$\hat{x}(s) = (sI-A)^{-1}\ b\hat{v}_g(s) + (sI-A)^{-1}\left[(A_1-A_2)X + (b_1-b_2)V_g\right]\hat{d}($$

$$\hat{y}(s) = C^T\hat{x}(s) + (C_1^T - C_2^T)X\ \hat{d}(s) \qquad \ldots(2.3.23)$$

Now, converter input-output relationship is defined as

$$\hat{y}(s) = G_{yg}\,\hat{v}_g(s) + G_{yd}\,\hat{d}(s)$$

$$\hat{i}(s) = G_{ig}\,\hat{v}_g(s) + G_{id}\,\hat{d}(s) \qquad \ldots(2.3.24)$$

In which G's are known from (2.3.23). The subscripts of G's designate the corresponding transfer functions. For example G_{yg} is the source voltage $\hat{v}_g$ to output voltage $\hat{y}$ transfer function.

For the proposed canonical circuit model in fig. 2.3.5, we directly get :

$$\hat{y}(s) = (\hat{v}_g + e(s)\hat{d})\ \frac{1}{u}\,H_e(s)$$

$$\hat{i}(s) = j(s)\hat{d} + (e(s)\hat{d} + \hat{v}_g)\cdot\frac{1}{\mu^2 Z_{ei}(s)} \qquad \ldots(2.3.25)$$

or $$\hat{y}(s) = \frac{1}{\mu}\,H_e(s)\hat{v}_g(s) + e(s)\,\frac{1}{\mu}H_e(s)\hat{d}(s)$$

$$\hat{i}(s) = \frac{1}{\mu^2 Z_{ei}(s)}\,\hat{v}_g(s) + j + \frac{e(s)}{\mu^2 Z_{ei}(s)}\,\hat{d}(s)$$

$$\ldots(2.3.26)$$

Compare (2.3.24) & (2.3.26)

$$G_{yg}(s) = \frac{1}{\mu}\,H_e(s) \qquad G_{yd} = e(s)\,\frac{1}{\mu}\,H_e(s) = e(s).G_{yg}$$

$$G_{ig}(s) = \frac{1}{\mu^2 Z_{ei}(s)} \qquad G_{id} = j(s) + \frac{e(s)}{\mu^2 Z_{ei}(s)} = j(s)+e(s)G_{ig}(s)$$

$$\therefore \quad e(s) = \frac{G_{yd}(s)}{G_{yg}(s)} \qquad j(s) = G_{id}(s) - e(s)\, G_{ig}(s) \qquad \ldots(2.3.27)$$

$$H_e(s) = \mu\, G_{yg}(s)$$

μ could be calculated from :

$$\frac{Y}{V_g} = -C^T A^{-1} b = \frac{1}{\mu} \times \text{correction factor.} \qquad \ldots(2.3.28)$$

e(s) and j(s) can be defined as

$$e(s) = E\, f_1(s)$$

$$j(s) = J\, f_2(s)$$

where $f_1(0) = f_2(0) = 1$, and E&J are the dc gains of the frequency dependent functions e(s) & j(s) respectively.

Example : Ideal Boost Power Stage -

From (2.3.18) with $R_l=0$ & $R_c=0$, the final state space averaged model for Boost Power Stage becomes :

$$\begin{bmatrix} \frac{d\hat{i}}{dt} \\ \frac{d\hat{v}}{dt} \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & -\frac{D'}{L} \\ \frac{D'}{C} & -\frac{1}{RC} \end{bmatrix}}_{A} \begin{bmatrix} \hat{i} \\ \hat{v} \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}}_{b} \hat{v}_g + \begin{bmatrix} \frac{RD'}{L} \\ -\frac{1}{C} \end{bmatrix} \frac{V_g}{D'^2 R}\, \hat{d} \qquad \ldots(2.3.29)$$

$$\hat{y} = \underbrace{\begin{bmatrix} 0 & 1 \end{bmatrix}}_{C^T} \begin{bmatrix} \hat{i} \\ \hat{v} \end{bmatrix}$$

$$\therefore\ -C^T A^{-1} b = -\begin{bmatrix} 0 & 1 \end{bmatrix} \frac{LC}{D'^2} \begin{bmatrix} -\frac{1}{RC} & \frac{D'}{L} \\ -\frac{D'}{C} & 0 \end{bmatrix} \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}$$

$$= \frac{1}{D'}$$

Put in eq. (2.3.28)

$$\boxed{\mu = 1-D}$$

$$\frac{d\hat{i}}{dt} = -\frac{D'}{L}\hat{v} + \frac{1}{L}\hat{v}_g + \frac{V_g}{LD'}\hat{d}$$

$$\frac{d\hat{v}}{dt} = \frac{D'}{C}\hat{i} - \frac{1}{RC}\hat{v} - \frac{1}{C}\frac{V_g}{D'^2 R}\hat{d}$$

Taking Laplace Transform, we get

$$s\hat{i}(s) = -\frac{D'}{L}\hat{v}(s) + \frac{1}{L}\hat{v}_g(s) + \frac{V_g}{LD'}\hat{d}(s)$$

$$s\hat{v}(s) = \frac{D'}{C}\hat{i}(s) - \frac{1}{RC}\hat{v}(s) - \frac{1}{C}\frac{V_g}{D'^2 R}\hat{d}(s) \quad \ldots(2.3.30)$$

$$\text{or}\quad \left(s + \frac{D'^2}{sCL} + \frac{1}{RC}\right)\hat{v}(s) = \frac{D'}{sCL}\hat{v}_g(s) + \frac{D'^2 R - sL}{sCL.D'^2 R}V_g.\hat{d}$$

$$e(s) = \frac{G_{yd}(s)}{G_{yg}(s)} = \frac{(D'^2 R - sL)\,V_g}{D'^3 R}$$

$$= \frac{D'^2 R - sL}{D'^2 R}V = V\left(1 - s\frac{L}{R}\right)$$

$$\therefore\ \boxed{E = V} \qquad \boxed{f_1(s) = \left(1 - s\frac{L}{R}\right)}$$

Solving eqn. (2.3.30) for i(s) we get

$$i(s) = \frac{1 + sRC}{sL(1+sRC)+D'^2R}\,\hat{v}_g(s) + \frac{2 + sRC}{D'\,sL(1+sRC)+D'^2R}\,V_g\hat{d}$$

Compare with (2.3.24)

$$G_{ig}(s) = \frac{1 + sRC}{sL(1+sRC) + D'^2R} \qquad G_{id}(s) = \frac{2 + sRC}{sL(1+sRC)+D'^2R}V$$

$$\therefore j(s) = \frac{2 + sRC}{sL(1+sRC)+D'^2R} - \frac{D'^2R - sL}{D'^2R} \cdot V \cdot$$

$$\cdot \frac{(1 + sRC)}{sL(1+sRC) + D'^2R}$$

After solving we get

$$j(s) = \frac{V}{D'^2R} \qquad \therefore \boxed{J = \frac{V}{D'^2R}} \qquad \boxed{f_2(s) = 1}$$

Expressions for the elements in the canonical equivalent circuit can be found in a similar way for any converter configuration. Results for the three common converts, the buck, boost, and buck-boost power stages are summarized in table 1.

Table 1

	$\mu(D)$	E	$f_1(s)$	J	$f_2(s)$	L_e	R_e
Buck	$\frac{1}{D}$	$\frac{V}{D^2}$	1	$\frac{V}{R}$	1	L	R_1
Boost	1-D	V	$1-s\frac{L_e}{R}$	$\frac{V}{(1-D)^2R}$	1	$\frac{L}{(1-D)^2}$	$\frac{R_1}{(1-D)^2}$
Buck-Boost	$\frac{1-D}{D}$	$-\frac{V}{D^2}$	$1-D\frac{R_e+sL_e}{R}$	$-\frac{V}{(1-D)^2R}$	1	$\frac{L}{(1-D)^2}$	$\frac{R_1}{(1-D)^2}$

The negative sign in E & J in case of Buck-Boost power stage indicates the inverting polarity of the ideal transformer. Therefore for positive input dc voltage V_g, the input dc voltage V is negative.

2.4. Modelling of Modulator :

We have discussed about the switching mode converter in the previous sections. Now a general representation of a switching mode regulator in which switching mode converter is represented by a buck-boost power stage, is shown in fig. 2.4.1.

We have already overcome the main difficulty in analysing the switching mode regulator viz. the modelling of its nonlinear part, the switching mode convert by obtaining the small signal low-frequency circuit model in the canonical circuit form.

Now in the next step we will develop a model for the modulator. This is easily done by writing an expression for the essential function of the modulator, which is to convert an (analog) control voltage V_c to theswitching duty ratio D. This expression can be written as

$$D = \frac{V_c}{V_m}$$

where V_m = Range of control signal required to sweep the duty ratio over its full range from 0 to 1.

A small variation $\hat{v}_c$ superimposed upon V_c therefore produces a corresponding variation $\hat{d} = \frac{\hat{v}_c}{V_m}$ in D, which can be

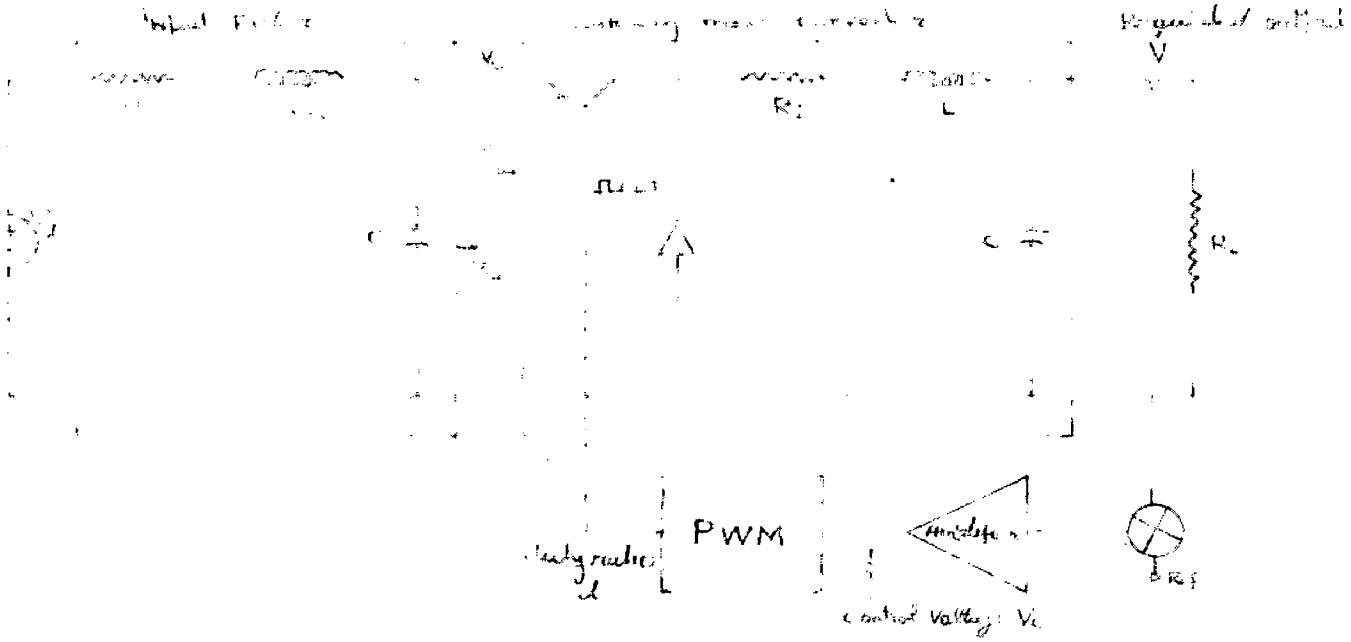
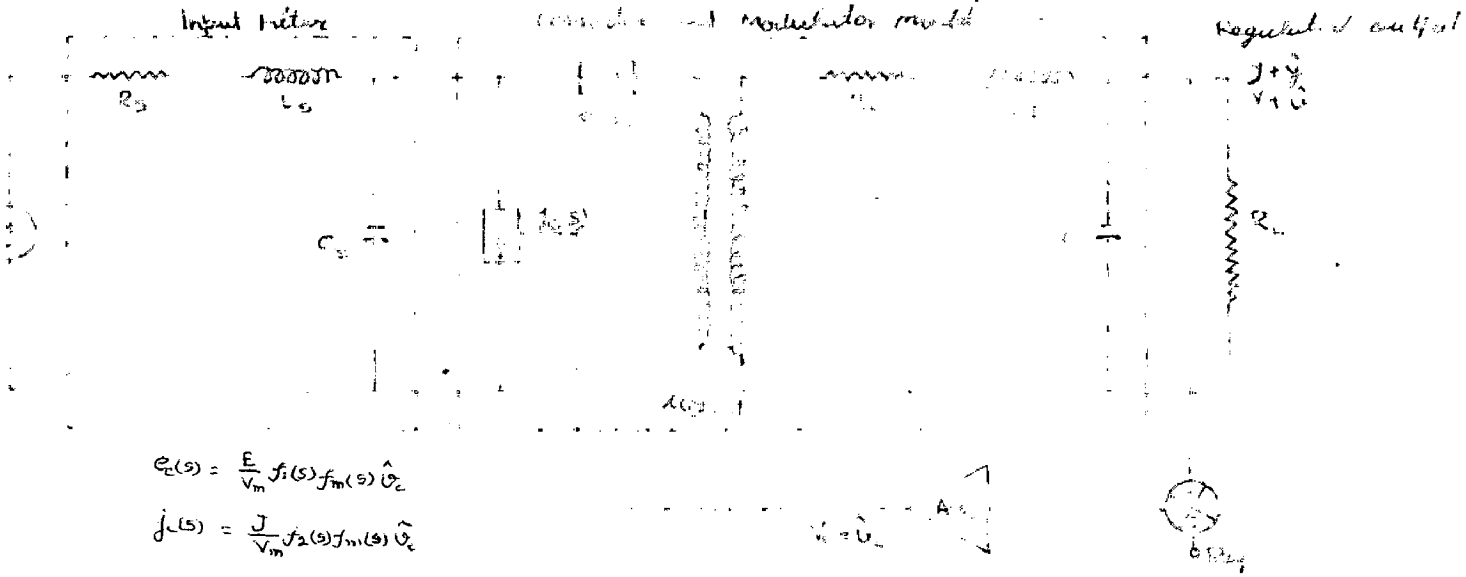


FIG. 2.4.1 BUCK SWITCHING MODE CONVERTER
WITH
INPUT FILTER & CONTROL CIRCUIT



$$e_c(s) = \frac{E}{V_m} f_1(s) f_m(s) \hat{v}_c$$

$$j_c(s) = \frac{J}{V_m} f_2(s) f_m(s) \hat{v}_c$$

FIG 2.4.2 EQUIVALENT CIRCUIT OF COMPLETE CLOSED LOOP REGULATED

generalized to account for a nonuniform frequency response as :

$$\hat{d} = \frac{f_m(s)}{V_m} \hat{v}_c \qquad f_m(o) = 1.$$

Thus, the control voltage to duty ratio small signal transmission characteristic of the modulator can be represented in general by the two parameters V_m and $f_m(s)$, regardless of the detailed mechanism by which the modulation is achieved.

Now if we substitute $\hat{d}$ from the above equation in the two generators in canonical circuit model of the switching converter, the resulting model will be expressed in terms of the ac control voltage $\hat{v}_c$. Thus the resulting model will be a linear ac equivalent circuit that represents the small-signal transfer properties of the nonlinear processes in the modulator and converte

Now if we add the linear amplifier and the input and output filters, we obtain the ac equivalent circuit of the complete closed loop regulator as shown in Fig. 2.4.2.

In the circuit the modulator transfer function has been incorporated in the generator designation and therefore in the closed loop regulator, the generators no longer are independent but are dependent on another signal in the same system.

The current generator in fig. 2.4.2 is responsible for the interaction between the switching mode regulator-converter and the input filter, thus causing performance degradation and/or stability problems when an arbitrary input filter is added. The design of the input filter will be discussed in next section.

Thus as shown in fig. 2.4.2, we have succeeded in obtainir

the linear circuit model of the complete switching mode-regulator. Hence the well known body of linear feedback theory can be used for both analysis and design of this type of regulator.

Now let us summarize the modelling aspect of switching mode regulator. A general method for modelling power stages of any switching dc- to - dc converter has been developed through state-space averaging approach. The fundamental step is in replacement of the state space descriptions of the two switched networks (2.3.1) by their average over the single switching period T, which results in a single continuous state-space equation description (2.3.3) designated the basic averaged state space model.

After some perturbation and linearization steps, a final state space averaged model is given by (2.3.13) & (2.3.14). From these equations a Canonical circuit model of fig. 2.3.5 was developed. Different converters are represented simply by an appropriate set of formulas (2.3.27) & (2.3.28) for four element in this general equivalent circuit. Besides its unified description, one of the advantages of the canonical circuit model is that various performance characteristics can be compared in a quick and easy manner.

C H A P T ER - III

DESIGN AND ANALYSIS OF SWITCHING CONVERTERS

3.1(a) Introduction

3.1(b) Input Filter Considerations in Design and Application of Switching Mode Regulators

- 3.1.1 Necessity of Input Filter
- 3.1.2 Ways of designing an Input Filter
- 3.1.3 Oscillation problem
- 3.1.4 Small Signal Average Model

3.2 Input Filter Design

- 3.2.1 Single Stage Input Filter Configurations
- 3.2.2 Input Filter Interactions
  Loop Stability & Transient Response and Audiosusceptibility.
- 3.2.3 Optimal Input Filter Configuration & Design Constraints

3.3 Analysis of Switching Mode Converters with Input Filter.

3.1 INTRODUCTION

We have discussed the modelling of switching mode converter and developed a canonical circuit model which describes the input-output and control properties of the system. Now in this section we will analyse some switching mode converters with input filters. The effect of input filter on system performance will be discussed and a comparative study will be made for switching mode converters with single stage and two stage input filter. Design constraints for optimal input filter configuration are also obtained.

In case of two stage filter, the constraints of optimal design becomes very complicated and difficult to solve. Some approximations are made to simplify these equations and the effects of these approximations on input filter and system perfonmance are also discussed.

Input Filter Considerations in Design and Application of Switching Mode Regulator

As we have discussed, at power levels above a few hundred watts, switching mode regulators are more useful because of the significantly higher efficiency than can be obtained with linear dissipative regulators. But when we use switching regulators, the regulator input current has a substantial ripple component at the switching frequency . When more than one power supplies are connected to a common main as

is shown in Fig. 3.1.1, the reflected ripple current of one of the power supplies may affect the perfomance of other power supplies, e.g. if we consider Buck type switching mode regulators of Fig. 1.3(a) its inductor current and input current is shown in Fig. 3.1.2. Fig. 3.1.2(a) & (b) show inductor ~~inductor~~ and input current respectively when L is equal to the critical inductance L_c. Fig. 3.1.2(c) & (d) show these currents when $L = 5L_c$. For battery driven systems, to meet this peak current requirement, capacity of the battery has to be increased very much. Moreover, it affects battery e.m.f. and therefore other power supplies connected to the same battery will also got affected.

Similarly, as shown in Fig. 3.1.1 when an apparatus such as a d.c. motor, a line printer etc. is connected to one of the power supplies, the noise generated in this apparatus and noise of one power supply is transmitted to the other power supplies which again affect the perfomance of other power supplies.

Therefore, to smooth the current drawn from the unregulated line supply, use of an input filter is a necessity. One function of the input filter is to present a low pass transfer characteristic to current variations in the opposite direction. A switching mode regulator may demand an input current that has a large component at the switching frequency and input filter prevents this component from

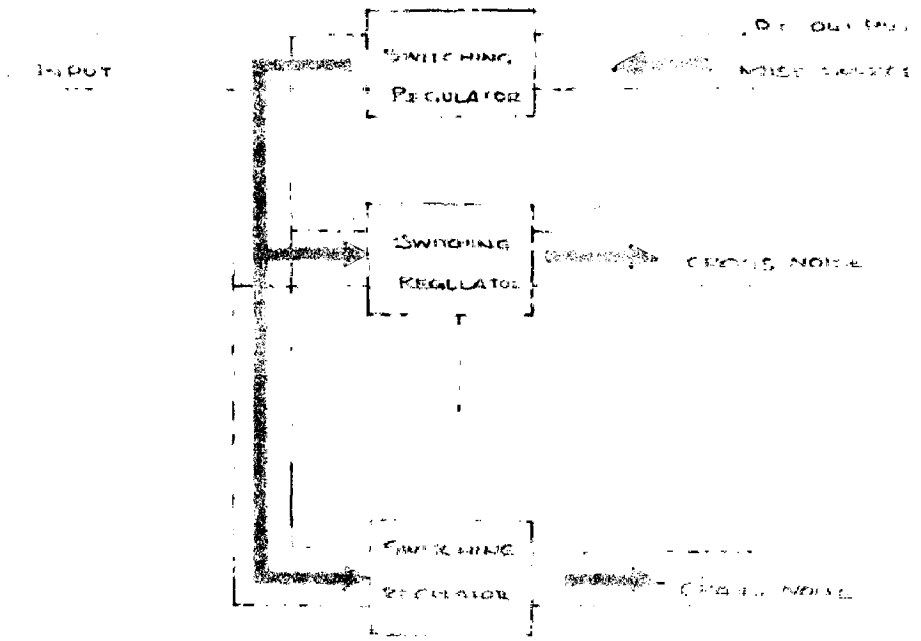
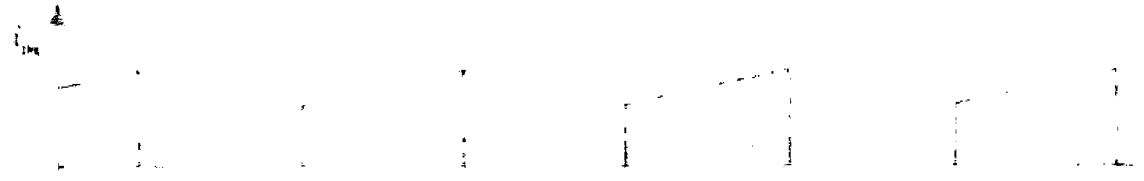


FIG. 3.11 POWER SUPPLIES CONNECTED TO COMMON MAINS

(a) INDUCTOR CURRENT WHEN $L = L_c$

(b) INPUT CURRENT WHEN $L = L_c$

(c) INDUCTOR CURRENT WHEN $L = 5L_c$



(d) INPUT CURRENT WHEN L $5L_c$

[illegible] INPUT OUTPUT CURRENT FOR BUCK TYPE SWITCHING MODE REGULATOR

flowing in the line source. Another function of the input filter is to present a low pass transfer characteristic to the unregulated line voltage V_s in Fig. 2.4.1 so that higher frequency disturbances v_s are suitably attenuated at the regulator. These functions "forward voltage transfer function", and "reverse current transfer function" are defined by H(s) [8] as shown in Fig. 3.1.3 and called Forward Transfer Characteristi of input filter. This function H(s) is defined for the "unloade filter, that is, without the regulator attached; this makes H(s) a property of the filter only, unaffected by the complex nature of the regulator input impedance.

This input filter serves to :

1) prevent the regulator switching current from being reflected back into the source;
2) to isolate source voltage transients so as not to degrade the performance of the switching regulator down-stream.

Consequently, the filter is required to provide not only high attenuation at the switching frequency but also sufficient damping against any line disturbance so that output peaking is properly controlled.

There may be two ways of designing an input filter for switching mode regulator :

(1) Design Regulator and Input Filter Simultaneously :

The preferred approach is to design the regulator

and input filter together so that the inequality condition for stability shown by equation (3.1.2) and other conditions may be satisfied.

(2) Post Facto Design :

If the regulator is a 'black box' for which no information on its internal structure is available, we have to design the input filter on the basis of direct experimental measurements of input impedance z_i of the regulator and thus maintaining the inequality condition $z_s < z_i$. But such an input filter design procedure ensures only system stability, and does not guarantee that the regulator performance will remain essentially unaffected. Another drawback of this design is that the system may oscillate because of this inadequate input filter.

Nature of the Oscillation Problem :

To understand this problem we will consider a Buck type switching regulator as shown in Fig. 2.4.1.

The switching mode converter acts as a dc transformer having some voltage conversion ratio $\mu = V_s/V$ to the extent that the conversion is 100 percent efficient, the current conversion ratio is $I_s/I = 1/\mu$ and the converter input power $P = V_s I_s$ equals the output power VI. For a given load resistance R_L, the feedback action of the regulator adjusts the conversion ratio μ to maintain constant output voltage and hence constant output power, even if the input voltage V_s

varies. It follows that if V_s increases, I_s must decrease since the input power also remains constant. Consequently the regulator exhibits a negative incremental input resistance R_i given by -

$$R_i = \frac{dV_s}{dI_s} = \frac{d}{dI_s}\left(\frac{P}{I_s}\right) = \frac{P}{I_s^2} = -\frac{V_s}{I_s} = -\mu^2 \frac{V}{I} = -\mu^2 R_L \quad (3.1.1)$$

This is the low frequency value of the regulator input impedance z_i indicated in fig. 2.4.1. For the basic Buck converter configuration shown, the conversion ratio is $\mu = 1/D$ where D is the dc duty ratio of the power switch, so that $R_i = -R_L/D^2$.

The regulator negative input resistance R_i in combinati with the input filter can under certain conditions constitutes a negative resistance oscillator, and is the origin of the system potential instability. The input filter output impedance z_s is a low (positive) resistance at dc and low frequencies, but in the neighbourhood of the filter cut-off frequency its output impedance rises to a resonant maximum $|z_s|_{max}$ which in a high Q filter may be many times the associated ohmic resistances, and if $|z_s|$ rises sufficiently that the net circuit resistance becomes negative, oscillation will occur.

To explain further, let us consider the circuit of Fig. 3.1.4.

$$\text{Equivalent impedance} = \frac{-|R_i| \cdot |z_s|}{|z_s| - |R_i|}$$

Therefore if $|R_i| < |z_s|$, the net resistance becomes negative and

oscillation will occur.

Therefore, to ensure stability the input filter must be designed to have low Q, which is in conflict with the requirement for low ohmic resistances, to maintain high efficiency. Therefore the condition for stability

$$|Z_s|_{max} < |R_i| \qquad \ldots(3.1.2)$$

For the basic single section input filter and Buck converter shown in fig.(2.4.1) the filter Q factor is

$$Q_s = \frac{\sqrt{L_s/C_s}}{R_s}$$

$$|Z_s|_{max} = Q_s^2 R_s = L_s/C_s R_s$$

so that the stability condition is

$$\frac{L_s}{C_s R_s} < \frac{R_L}{D^2} \qquad \ldots(3.1.3)$$

Therefore we have to compromise between low Q to meet the above stability condition and high Q to maintain good efficiency.

The above stability condition is not sufficiently general. The regulator input impedance Z_i is a negative resistan $R_i = -\mu^2 R_L$ only at low frequencies; at some high frequency beyond the regulator loop gain crossover freq. (the freq. at which the loop gain magnitude falls below unity), Z_i must have a positive real part. Therefore, the input impedance Z_i must begin to deviate from its negative resistance value of $-\mu^2 R_L$

at some low frequency. The stability condition (3.1.2) is therefore only correct if the frequency at which $|Z_s|$ reaches $|Z_s|_{max}$, namely the filter cut-off freq., is below the frequency at which the regulator input impedance Z_i begins to deviate from its low freq. value $-\mu^2 R_L$.

The practical design criteria for stability is : the input filter cut-off frequency should be chosen lower than the averaging filter cut-off frequency; the input filter output impedance should be made much smaller than the regulator open-loop input impedance.

Small Signal Average Model :

We have already developed a canonical model in the previous chapter, in which two lumped linear circuit topologies corresponding to the power switch ON time and OFF time were replaced by a single lumped linear average model as in Fig. 2.3.5. But in that case we did not consider the effect of input filter. Now if we consider input filter also as shown in Fig. 2.4.1 and replace input filter by its Thevenin's equivalent we will get a small signa-l averaged circuit model as shown in Fig. 3.1.5. In this circuit the effect of the input filter is characterized by two parameters H(s) and Z(s) where,

H(s) : Forward transfer characteristic of the input filter.

Z(s) : Output impedance of input filter.

The primary side (input filter side) ckt. may be transferred to secondary side (switching mode converter side) as shown in Fig. 3.1.6. With this transferring from primary to secondary side, the ckt. of Fig. 3.1.5 can be represented by a dual input describing function as shown in Fig. 3.1.7. Dual input describing functions are -

a) duty-cycle to output describing function $\hat{v}_o/\hat{d}_o$

b) Regulator input to output describing function $\hat{v}_o/\hat{v}_i$

The ckt. shown in Fig. 3.1.7 is a general small signal average model of switching mode regulator with input filter. By putting the values of μ, E, $f_1(s)$, $f_2(s)$, J etc. from Table 1 we can get the averaged ckt. for Buck, Boost or Buck-Boost power stages with input filter. From this dual input describing function, interaction of the circuit parameters between input filter, output filter and control loop can be analytically comprehended.

3.2 Single Stage Input filter configurations

An improperly designed input filter can cause interactions between the input filter and the control loop of a switching regulator and therefore can result in severe degradati of regulation perfomance such as : instability, transient respo and audio-susceptibility.

The input filter design problem is that of realization of the two functions H(s) and Z(s) to satisfy the several

performance requirements and constraints. The greater the number of elements in the filter, the more degrees of freedom there are available to optimize H(s) and Z(s), at the price of greater size, weight and cost.

Consider the single section Lc filter shown in Fig. 3.2.1(a). The series resistance R_s is always to be minimized in the interest of high efficiency, and can be considered fixed, therefore, the only remaining design degree of freedom is through the filter characteristic resistance $R_o = \sqrt{L_s/C_s}$. This parameter determines the Q factor and hence the degree of peaking of both the $|H(s)|$ and $|Z(s)|$ characteristics.

$$Z(s) = \frac{(R_s + jwL_s)\ \frac{1}{jwC_s}}{R_s + jwL_s + \frac{1}{jwC_s}}$$

At filter cut-off freq. $w_s = \frac{1}{\sqrt{L_sC_s}}$, $|Z_s|$ has a maximum value $|Z_s|_{max}$

$$\text{max. } Z(s) = \frac{\frac{R_s}{jw_sC_s} + \frac{L_s}{C_s}}{R_s} = \frac{R_o^2 - jR_s\sqrt{\frac{L_s}{C_s}}}{R_s} = \frac{R_o^2 - jR_sR_o}{R_s}$$

$$\text{or} \quad \frac{R_o^2}{R_s} = \left[1 - j\left(\frac{R_s}{R_o}\right)\right]$$

$$|Z_s|_{max} = R_m = \left(\frac{R_s^2}{R_s}\right)\sqrt{1 + \left(\frac{R_s}{R_o}\right)^2}$$

$$H(s) = \frac{\frac{1}{jwC_s}}{R_s + jwL_s + \frac{1}{jwC_s}}$$

$$\text{At } w_s \quad H(s) = \frac{\frac{1}{jw_sC_s}}{R_s} = \frac{1}{jw_sR_sC_s} \quad \text{i.e. one Pole at } w_s = 0$$

To keep $|Z_s|_{max}$ as low as possible to meet the stability condition (3.1.2), the filter characteristic resistance R_o has to made low i.e. low L_s/C_s ratio. But in actual system L_s/C_s ratio is too high to meet this requirement. Therefore the system with such type of simple input filter are prone to instability.

If L_s/C_s ratio is too high for the required $|Z_s|_{max}$ the stability can be improved by addition of extra series damping resistance. As we have discussed R_s can not be increased in the interest of high efficiency, hence a resistance R_c may be placed in series with C_s as shown in fig. 3.2.1(b).

$$Z(s) = \frac{(R_s + jwL_s)\ (R_c + \frac{1}{jwC_s})}{R_s + jwL_s + R_c + \frac{1}{jwC_s}}$$

At w_s

$$Z(s) = \frac{R_o^2 + R_sR_c + jR_o(R_c - R_s)}{R_s + R_c}$$

$$|Z(s)|_{max} = \frac{\sqrt{(R_o^2 + R_sR_c)^2 + (R_o^2(R_c - R_s)^2}}{R_s + R_c}$$

$$= \frac{R_o^2}{R_s + R_c}\sqrt{1 + \frac{R_c^2R_s^2}{R_s^4} + \frac{R_c^2 + R_s^2}{R_o^2}}$$

$$\text{or} \quad |Z_s|_{max} = \frac{R_s\sqrt{1 + (\frac{R_c}{R_o})^2}}{R_s + R_c}\ (\frac{R_o^2}{R_s})\ 1\sqrt{+\ 1 + (\frac{R_s}{R_o})^2}$$

$$= R_m \cdot \frac{R_s \sqrt{1+\left(\frac{R_c}{R_o}\right)^2}}{R_s + R_c}$$

$$H(s) = \frac{R_c + \frac{1}{j\omega C_s}}{R_s + R_c + j L_s + \frac{1}{j C_s}}$$

, at $\omega = \omega_s$

$$H(s) = \frac{1+j\omega_s R_c C_s}{j\omega_s C_s (R_s+R_c)} = \frac{\left(1+ j \frac{R_c}{R_o}\right)}{j\omega_s C_s (R_s+R_c)}$$

Thus by addition of an series resistance R_c, $|Z_s|_{max}$ is reduced by the factor $R_s \sqrt{1+(R_c/R_o)^2} / (R_s+R_c)$ from its previous value R_m, but the H(s) has been degraded by appearance of a zero at $\omega_s R_o/R_c$, so that the switching frequency attenuation is degraded. Also since most of the regulator switching frequency input current flows in C_s, there may be substantial power loss in R_c.

This can further be modified and power loss in R_c can be avoided if we add parallel damping resistance R_p across L_s as shown in Fig. 3.2.2(a).

With this configuration $|Z_s|_{max}$ is now reduced by the factor $1/ (1+R_o^2/R_s R_p)$ from R_m, but H(s) is again degraded by appearance of a zero at $\omega_s R_p/R_o$. Thus, the $|H(s)|$ and $|Z(s)|$ characteristics are the same in nature as for the series damping resistance R_c, but there is negligible power loss in the parallel damping resistance R_p.

An improvement is to place the parallel damping resistance R_p across C_s instead of across L_s as shown in fig. 3.2.2(b).

This has the same desirable effect in lowering $|Z_s|_{max}$, and does not introduce an unwanted zero in H(s).

Since there is also negligible power dissipation in R_p, this arrangement is the best so far discussed, but has the disadvantage that a large blocking capacitor is needed.

To overcome all these problems, two stage input filters are used. The details, advantages and experimental results with these input filters will be shown in subsequent sections.

Input Filter Design Constraints :

Input filter design guidelines are established to minimize the interactions among input filter, output filter and control loop.

Input filter interactions - Loop stability and transient response

The stability of a switching regulator can be examined by the open loop gain $G_T(s)$ from the fig. (3.1.7)

$$G_T(s) = F_c(s)F_p(s)F_E(s)F_m(s) \qquad \ldots(3.2.1)$$

where $F_c(s).F_p(s)$ is the duty-cycle to output describing function $\hat{v}_o/\hat{d}$, and $F_E(s)$ and $F_m(s)$ are the transfer functions for the error processor and the pulse width modulator respectively. Output impedance Z(s) of the input filter has the following effects:

1) The output impedance Z(s) is related to the duty cycle

power stage gain F_c through

$$F_c = V_I - Z(s)\ I_o D \qquad ...(3.2.2)$$

Here, V_I and I_o are regulator input voltage and output current respectively. Since at resonant frequency, Z(s) rises to $|Z(s)|$ max, it can significantly reduce F_c, therefore the regulator loop gain and the related perfomance. More severely, it can result in an unstable positive feedback system. Equation (3.2.2) can be rewritten as :

$$F_c = I_o D \left[V_I/I_o D - Z(s)\right] \qquad ...(3.2.3)$$

The first term, $V_I/I_o D \cong V_I/I_i$ is the negative resistance of the input filter as discussed in eqn. (3.1.1). Excessive output impedance Z(s) at the resonant frequency of the input filter duty-cycle power-stage gain together with the negative feedback loop will contribute to an unstable positive feedback system.

2. The output impedance Z(s) is related to the power stage transfer function $F_p(s)$ through

$$F_p(s) = (R_C+1/sC) \,||\, R_L / \left[D^2 Z(s)+Z_i(s)\right] \qquad ...(3.2.4)$$

where $Z_i(s) = R_1 + sL + (R_C + 1/sC) \,||\, R_L$

Excessive Z(s) at the resonant frequency can significantly reduce $F_p(s)$, therefore, the loop gain. Nevertheless, the degradation of $F_p(s)$ due to Z(s) can be avoided, if there is a sufficient separation of the input filter resonant frequency

$\omega_s \triangleq 1/\sqrt{L_s C_s}$ and the output filter resonant frequency $\omega_o \triangleq 1/$
The Fig. 3.2.3 shows the interaction between the input filter and the output filter.

It was seen that a maximum interaction between the input filter and the output filter occurs when ω_s coincides with ω_o. It can result in a large reduction of $F_p(s)$. Such interaction can be minimized by either decreasing ω_s or increasing ω_s as shown in fig. 3.2.3(b) and (c). Larger ω_s is desirable from the point of view of weight and size reduction. However, for higher resonant freq. ω_s the effect of peaking of Z(s) becomes more prominent since loop gain descends rapidly as freq. increases.

The effect of improperly designed input filter on duty-cycle to output transfer function is shown in fig. 3.2.4.

In this fig. the solid curve represents the transfer characteristics without an input filter and the dotted curve represents that with an input filter. A sharp reduction of the gain at the input filter resonant frequency causes loop instability and severely degrades the transient response. Computerized results are given in the last section.

Input-Filter Interaction - Audiosusceptibility :

The audiosusceptibility is defined as the closed-loop input - to output transfer function $G_A(s)$. It is employed to measure the attenuation of a sinusoidal disturbance from the input line to the regulator output. Thus this helps in switching

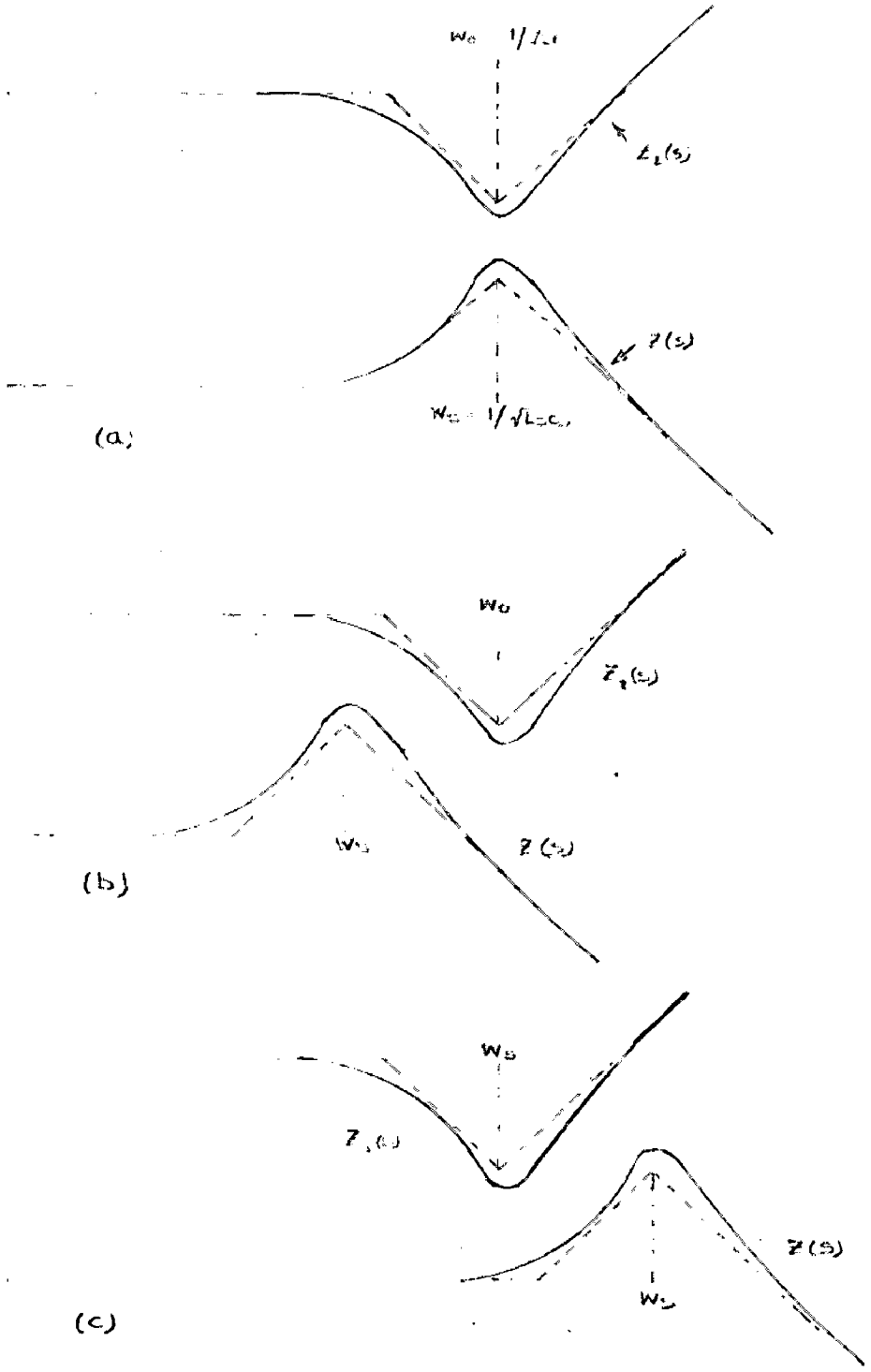
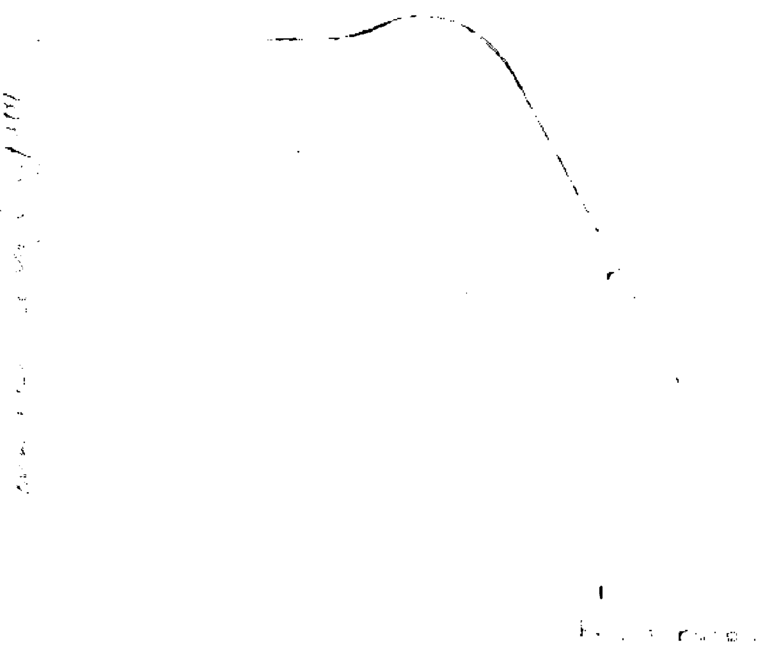
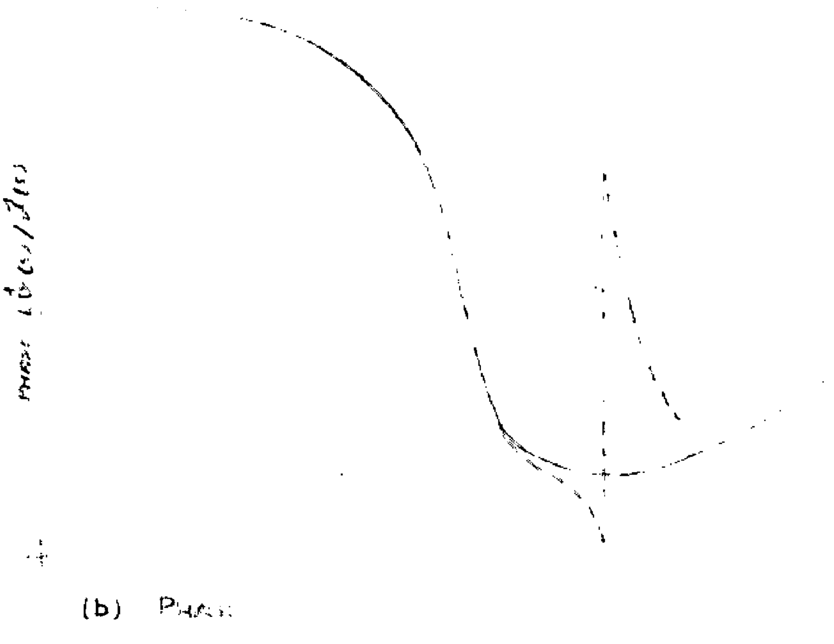


FIG. 3 2·3 INTERACTION BETWEEN OUTPUT IMPEDANCE Z (S) OF INPUT FILTER AND INPUT IMPEDANCE $Z_i(S)$ OF REGULATOR



(a) GAIN



(b) PHASE

FIG. … DUTY CYCLE TO OUTPUT VOLTAGE …

WITH AND WITHOUT …

regulators analysis when it is required to specify how a small signal audio-freq. disturbance of the input line affects the regulated. Output voltage. From fig. 3.1.7

$$G_A(s) \triangleq \frac{\hat{v}}{\hat{v}_i}$$

$$= \frac{F_I(s) \cdot F_p(s)}{i+F_c(s).F_p(s).F_E(s).F_m(s)}$$

where $F_I(s) = D.H(s)$

Therefore, excessive peaking of H(s) can result in severe degradation of the audiosusceptibility of the regulator. The effect of different input filters on audiosusceptibility is shown in Graph 6. It can be seen that peaking is considerably reduced in case of two stage Input filter.

In summary, in the designing of input filter, following conditions must be satisfied :

1. Requirement for electromagnetic interference to prevent the regulator switching current from being reflected back into the source.

2. Peaking limitations of H(s).

3. Peaking limitations of Z(s).

4. Limitations on weight and loss.

5. Nyquist stability criterion has to be satisfied.

6. Audiosuscepbibility sould not be degraded noticeably.

Out of the above conditions, the most importants are minimization of H(s) and Z(s) at filter resonance. In single stage input filter these minimizations can be done but at the cost of larger filter L or C i.e. increasing size, weight and loss. These limitations can be overcome by using two stage input filter.

Optimal Input Filter Configuration :

We have already discussed single stage input filter and its disadvantages. These problems of instability and resonance peaking can be overcome by use of two stage input filters. An optimal two stage input filter configuration is shown in fig. 3.2.5(b).

This filter configuration is capable of providing low-loss light weight high attenuation and a controlled resonant peaking of H(s) and Z(s).

This filter is particularly useful for switching regulators having stringent efficiency, attenuation, and peaking requirements that single stage input filter would simply become either in-applicable or impractical with respect to size and weight.

The first stage of two stage input filter, consisting of L_1-C_1-R_1 controls the resonant peaking of the filter. The second stage supplies most of the pulse current demanded by the switching regulator. The alternating component of the pulse current can be attenuated by the combined action of both filter stages to any desirable level. Capacitor with negligible series resistance are used for C_2, therefore, very little power is lost

due to the large amplitude alternating current in C_2.

For design of optimum weight input - filter, following basic constraints are employed :

1) Use the maximum flux capability of the magnetic core.
2) Fill the window area.
3) Control the resonant peaking of both H(s) and Z(s), designated as B_F and B_R, respectively.
4) Limit the filter loss P.
5) Specify the attenuation of the filter at the switching frec

Now designing and comparisons of single stage input filter and two stage input filter will be made in weight, efficiency and regulator loop performance. Although we will consider all the constraints i.e. full window, loss limit, resonant peaking limit, Attenuation but as we have said resonant peaking limits and attenuation are more important constraints, we will take only them in detail.

Using the toroidal core for filter inductor, the filter design variables for single stage filter are :

A_1, N_1, Z_1, Ac_1, L_1, C_1, R_1

For the two stage filter are :

A_1, N_1, Z_1, Ac_1, L_1, C_1, R_1, A_2, N_2, Z_2, Ac_2, L_2, C_2, R_2,

Where

A : Core cross sectional area

N : Number of turns

Z : mean length path for flux in the core

A_c: Cross-sectional area of one-turn conductor.

Let

ρ : Resistivity of the copper conductor

B_s: Saturation flux density of the core

D_c: Conductor density

D_i: Iron core density

F_c: ratio of one turn conductor average lengthtocore circum ference.

F_ω: Proportion of core window area actually occupied by the conductor when the window is filled.

Incorporating the design variables with the design constraints described before, the following constraints equations are formulated: For the single-stage filter, six constraints exist.

No Saturation :

i.e. core should not be saturated.

We know Flux linkage $\Psi = N.\Phi$

$$\text{or } L_1 I_{dc} = N_1 \Phi$$
$$= N_1 . B_s . A_1$$

$$\text{or } B_s N_1 A_1 - L_1 I_{dc} = 0 \qquad \ldots(3.2.5)$$

Full window :

It can be shown [7] that for toroidal core, following eq. holds good :

$$\sqrt{N_1 A_{c1}}/\pi F_w - (Z_1/2\pi) + (\sqrt{A_1}/2) = 0 \quad \ldots.(3.2.6)$$

And loss limit

$$(4 \rho F_c N_1 \sqrt{A_1}/A_{c1}) - (P/I_{dc}^2) = 0 \quad \ldots(3.2.7)$$

Required Attenuation :

For stability, attenuation 'α' should be less than or equal to E_{in}/E_o

i.e. $$\alpha \leq \frac{E_{in}}{E_o}$$

For single stage inpur filter

$$\alpha \leq \frac{R_1 + j\omega L_1 + \frac{1}{j\omega C_1}}{\frac{1}{j\omega C_1}}$$

$$\leq 1 - \omega^2 L_1 C_1 + j\omega R_1 C_1$$

$$|\alpha|^2 \leq (1 - \omega^2 L_1 C_1)^2 + \omega^2 R_1^2 C_1^2$$

At switching frequency F

$$(1 - 4\pi^2 F^2 L_1 C_1)^2 + 4\pi^2 F^2 R_1^2 C_1^2 - \alpha^2 \geq 0 \quad \ldots.(3.2.8)$$

Resonant Peaking Limit :

As we have discussed the resonat peaking of H(s) and Z(s) should be controlled

(i) We know for forward transfer function H(s)

$$H(s) = \frac{E_o}{E_{in}} = \frac{1}{\left[(1-\omega^2 L_1 C_1)^2 + \omega^2 R_1^2 C_1^2\right]^{\frac{1}{2}}}$$

At resonance frequency $\omega = \omega_o$: $1-4\pi^2 f^2 L_1 C_1 = 0$

$$B_F^2 \geq \frac{1}{4\pi^2 f^2 R_1^2 C_1^2}$$

$$\geq \frac{L_1}{R_1^2 C_1}$$

or $$L_1 - C_1 B_F^2 R_1^2 \leq 0 \qquad \ldots(3.2.9)$$

(ii) For output impedance of input filter i.e. Z(s)

$$Z(s) = \frac{\frac{1}{j\omega C_1}(R_1 + j\omega L_1)}{R_1 + j\omega L_1 + \frac{1}{j\omega C_1}}$$

$$= \frac{R_1 + j\omega L_1}{1-\omega^2 L_1 C_1 + j\omega R_1 C_1}$$

At resonance frequency $\omega = \omega_o$; $1-\omega^2 L_1 C_1 = 0$

$B_R \triangleq$ resonance peaking of Z(s)

$$\therefore \quad B_R \geq \frac{R_1 + j\omega_o L_1}{j\omega_o R_1 C_1}$$

$$\geq \frac{L_1}{R_1 C_1} - j\frac{1}{\omega_o C_1}$$

$$|B_R|^2 \geq \left(\frac{L_1}{R_1 C_1}\right)^2 + \frac{L_1}{C_1}$$

$$\text{or} \quad \geq \frac{L_1}{C_1}\left[1+\frac{L_1}{R_1^2 C_1}\right] \text{ or } \quad \frac{L_1}{C_1}\left[1+\frac{R_o^2}{R_1^2}\right]$$

Practically $\dfrac{R_o^2}{R_1^2} >> 1$

$$\therefore |B_R|^2 \geq \frac{L_1}{R_1 C_1}$$

$$\text{or} \quad L_1 - C_1 B_R R_1 \leq 0 \qquad \ldots(3.2.10)$$

For the two stage input filter, nin constraints exist:

As we have shown for single stage input filter, if core for L_1 & L_2 is not saturated, we can show

$$B_s N_1 A_1 - L_1 I_{xc} = 0 \qquad \ldots(3.2.11)$$

$$B_s N_2 A_2 - L_2 I_{xc} = 0 \qquad \ldots(3.2.12)$$

Full window for L_1 and L_2

$$(N_1 A_{c1}/\pi F_\omega)^{\frac{1}{2}} - (Z_1/2\pi)+(\sqrt{A_1}/2) = 0 \qquad \ldots(3.2.13)$$

$$(N_2 Ac_2/\pi F_\omega)^{\frac{1}{2}} - (Z_2/2\pi)+(\sqrt{A_2}/2) = 0 \qquad \ldots(3.2.14)$$

And loss limit

$$4P\ F_c\left[(N_1\sqrt{A_1}/Ac1) + (N_2\sqrt{A_2}/Ac_2)\right] - (P/I_{dc}^2) = 0 \ldots(3.2.15$$

Resonant Peaking Limits :

(i) Resonant peaking of H(s) at First stage filter.

From Fig.3.2.5(b) two loops equations will be :

$$V_i = (R_1+j\omega L_1+\frac{1}{j\omega C_1}+R_3)\,I_1-(R_3+\frac{1}{j\omega C_1})I_2$$

$$0 = (R_2+R_3+j\omega L_2+\frac{1}{j\omega C_1}+\frac{1}{j\omega C_2})\,I_2-(R_3+\frac{1}{j\omega C_1})I_1$$

$$V_o = \frac{1}{j\omega C_2} I_2$$

$$\therefore \frac{V_o}{V_i} = \frac{1/j\omega C_2 (R_3 + \frac{1}{j\omega C_1})}{\left\{j\omega C_1(R_1+R_3) + 1 - \omega^2 L_1 C_1\right\}\left\{(R_2+R_3) j\omega C_2 - \omega^2 L_2 C_2 + \frac{C_2}{C_1} + 1\right\}}$$

$$- (1 + j\omega C_1 R_3)^2 \cdot \frac{1}{(j\omega C_1)^2} \quad ..(3.2.$$

Since $R_3 >> R_1$ and $R_3 >> R_2$

And at first stage filter $1 - \omega^2 L_1 C_1 = 0$

$$\therefore H(s) = \frac{V_o}{V_i} = \frac{(1+j\omega_1 C_1 R_3)}{j\omega_1 C_1 R_3 (1 - \frac{C_2}{C_1} - \frac{L_2 C_2}{L_1 C_1}) - \frac{C_2}{C_1}}$$

$$= \frac{j + \frac{1}{\omega_1 C_1 R_3}}{j\,(1 - \frac{C_2}{C_1} - \frac{L_2 C_2}{L_1 C_1}) - \frac{C_2}{C_1} \cdot \frac{1}{R_3 \omega_1 C_1}}$$

$\therefore$ Resonant peaking of H(s) at first stage

$$B_{F_1}^2 = |H(s)|^2 \geq \frac{1 + \frac{1}{R_3^2 C_1^2 \omega_1^2}}{\left\{1 - \frac{L_2 C_2}{L_1 C_1} - \frac{C_2}{C_1}\right\}^2 + (\frac{C_2}{C_1})^2 \cdot \frac{1}{R_3^2 \omega_1^2 C_1^2}}$$

or $$(1 + \frac{L_1}{C_1 R_3^2}) \Big/ \left[(C_2/C_1)^2 \cdot (L_1/C_1 R_3^2) + (1 - C_2/C_1 - L_2 C_2/L_1 C_1)^2\right]$$

$$- B_{F1}^2 \leq 0 \qquad ...(3.2.17)$$

(ii) Resonant peaking of H(s) at secondstage filter :

For secondstage filter put $1 - \omega^2 L_2 C_2 = 0$ in eqn (3.2.16)

$$\therefore \frac{V_o}{V_i} = \frac{1 + j\omega_2 C_1 R_3}{\left\{j\omega_2 C_1 R_3 + (1-\omega_2^2 L_1 C_1)\right\}\left\{j\omega_2 C_2 R_3 + \frac{C_2}{C_1}\right\} - (1 + j\omega_2 C_1 R_3)\frac{C_2}{C_1}}$$

$$= \frac{(1+j\omega_2 C_1 R_3)}{-\omega_2^2 C_1 C_2 R_3^2 + \frac{C_2}{C_1} - \frac{L_1 C_1 C_2}{L_2 C_2 C_1} + j\omega_2 C_2 R_3 - j\omega_2 C_2 R_3 \cdot \frac{L_1 C_1}{C_2 L_2} + j\omega_2 C_2 R_3 - \frac{C_2}{C_1} + \frac{C_1^2 R_3^2}{L_2 C_2} \cdot \frac{C_2}{C_1} - 2j\omega_2 C_1 R_3 \cdot \frac{C_2}{C_1}}$$

$$= \frac{(1+j\omega_2 C_1 R_3)}{-\frac{L_1}{L_2}(1+j\omega_2 C_1 R_3)}$$

$\therefore$ Resonant peaking of H(s) at second stage

$$|H(s)| = B_{F_2} \geq \frac{L_2}{L_1}$$

$$\text{or} \quad \left(\frac{L_2}{L_1}\right) - B_{F_2} \leq 0 \qquad \ldots(3.2.1$$

(iii) Resonant peaking of Z(s) :

For simplicity we approximate the two stage input filter circuit by taking only first stage. It is shown in the computerize results in the last section that this approximation does not effect the performance of the filter at higher frequency.

$$Z(s) = -\frac{(R_1+j\omega L_1)(R_3+\frac{1}{j\omega C_1})}{R_1+R_3+j(\omega L_1-\frac{1}{\omega C_1})}$$

At resonance

$$|Z(s)|^2 = \frac{(R_1^2+\frac{L_1}{C_1})(R_3^2+\frac{L_1}{C_1})}{(R_1+R_3)^2}$$

$$\simeq\frac{(R_1^2+R_o^2)(R_3^2+R_o^2)}{(R_1+R_3)^2}$$

$$\therefore \beta_R \geq \frac{R_o^2}{(R_1+R_3)}\sqrt{1+(\frac{R_1}{R_o})^2}\cdot\sqrt{1+(\frac{R_3}{R_o})^2}$$

Practically we can neglect R_1 in comparision to R_3 and also $R_o >> R_1$

$$\text{i.e. } 1+(\frac{R_1}{R_o})^2 \simeq 1$$

$$\therefore B_R \geq \frac{R_o^2}{R_3}\sqrt{1+(\frac{R_3}{R_o})^2}$$

$$\text{or } B_R^2 \geq \frac{R_o^4}{R_3^2}\cdot\frac{R_o^2+R_3^2}{R_o^2}$$

$$\geq R_o^2\left[\frac{R_o^2}{R_3^2}+1\right]$$

$$\text{or } B_R^2 \geq \left(\frac{L_1}{C_1}\right)\left[1+\frac{L_1}{C_1}\cdot\frac{1}{R_3^2}\right]$$

$$\text{or } \left(\frac{L_1}{C_1}\right)\left[1+\left(\frac{L_1}{C_1}\right)\frac{1}{R_3^2}\right]-B_R^2 \leq 0 \qquad \ldots(3.2.19)$$

To avoid the complications in calculation, first we will consider a general network of two stage input filter as shown in Fig. 3.2.7. From this Fig. :

$$V_i = (Z_1+Z_2)\, I_1 - Z_2 I_2$$

$$0 = (Z_2+Z_3+Z_4) I_2 - Z_2 I_1$$

$$V_o = Z_4 I_2$$

$$H(s) = \frac{V_o}{V_i} = \frac{Z_4}{(Z_1+Z_2)\cdot\frac{(Z_2+Z_3+Z_4)}{Z_2} - Z_2}$$

$$= \frac{1}{Z_1Y_4+Z_1Y_2Z_3Y_4+Z_1Y_2+Z_3Y_4+1}$$

If we take the practical values of all the elements, we can very well say that

$$Z_1Y_4+Z_1Y_2Z_3Y_4+Z_3Y_4 \;>>\; 1+Z_1Y_2$$

More practically we can neglect Z_4Y_4 also. It is shown in the results in last section that these approximations do not affect our analysis :

$$\therefore H(s) = \frac{1}{Z_1Y_4+Z_1Y_2Z_3Y_4}$$

Now if we put valuesof all the impedances :

$$Z_1 = R_1 + j\omega L_1 \simeq j\,\omega\, L_1$$

$$Z_3 = R_2 + j\omega L_2 \simeq j\,\omega\, L_2$$

$$Y_4 = j\omega C_2$$

$$Z_2 = R_3 + \frac{1}{j\omega C_1} \simeq R_3$$

$$Y_2 = \frac{1}{R_3}$$

$$Z_1 Y_4 = -\omega^2 L_1 C_2$$

$$Z_1 Y_2 Z_3 Y_4 = -j\omega^3 L_1 L_2 \frac{C_2}{R_3}$$

$$\therefore \text{ Attenuation } \alpha(s) = \frac{V_i}{V_o} = -\omega^2 L_1 C_2 - j\omega^3 L_1 L_2 \frac{C_2}{R_3}$$

$$= -\frac{C_2}{C_1}\left(\frac{F}{f_1}\right)^2 - j\frac{L_2 C_2}{L_1 C_1}\left(\frac{F}{f_1}\right)^3 \frac{\sqrt{\frac{L_1}{C_1}}}{R_3}$$

Where f_1 is the first stage resonant frequency.

Now if we define G as $\frac{V_o}{V_{in}}$,

$$G \geq 1/\left[-(C_2/C_1)(F/f_1)^2 - j(L_2C_2/L_1C_1)(F/f_1)^3 \left\{(L_1/C_1)^{\frac{1}{2}}/R_3\right\}\right] \quad \ldots.(3.2.20)$$

To minimize the filter weight, the objective function is defined as :

Single-stage filter :

$$W = 4F_c D_c A_{c1} N_1 \sqrt{A_1} + D_i(A_1 Z_1) \quad \ldots(3.2.21)$$

Two stage filter:

$$W = 4F_c D_c (A_{c1} N_1 \sqrt{A_1} + A_{c_2} N_2 \sqrt{A_2}) + D_i(A_1 Z_1 + A_2 Z_2) + K_{c1} C_1 + K_{c2} C_2$$

+ negligible weight for R_3 ....(3.2.

Generally the method of Largerange Multipliers is used for closed form optimum solutions for simple optimization problems. But these well developed techniques are useless in case of switching mode regulator optimization, as both constraints and optimization criterion are highly nonlinear. It has been observed that Sequentia Unconstrained Minimization Technique (SUMT) [10], based on the penalty-function approach is most effective in achieving convergence for highly nonlinear design optimization. This technique is employed to meet all design constraints described above and concurrently minimize the input filter weight. After employing SUMT technique the results obtained in [7] are presented here in Table 2.

Table 2

e	Weight (gms)	Filter	L_1 (μH)	R_1 Ω	L_2 (μH)	R_2 Ω	C_1 (μf)	R_3 Ω	C_2 (μf)
	164	2-stage	232	0.0276	77	0.0119	100	1.73	30
	164	1-stage	77	0.0396			412		
	421	1-stage	28.2	0.0396			1124		

Some switching mode converters with above single stage and two stage input filter were analysed in digital computer EC-1010. The exact and approximate values of attenuation, forward transfer function H(s) and output Impedence of Input filter Z(s) with approximations described above were calculated and plotted on graph. The results show that these approximations hold good at switching frequency. Therefore for optimum design calculation and analysing the switching mode converters, these equations can be used directly which saves considerable and valuable computer time.

C H A P T E R - IV

PERFORMANCE COMPUTATION OF A SWITCHING MODE BUCK CONVERTER

Exercise 1

We analysed Buck type switching converter shown in Fig.2.4. with three Input filters of Table 2. Given circuit parameters of Buck type switching converter, objective and observations are discussed below.

Given

(i) Circuit parameters

V_I = 12V

V_o = 5V

R_L = 0.86 Ω

L = 200 μH

R_1 = 20 mΩ

C = 1540 uf

R_c = 7 mΩ

Switching period T_p = 50 uS or Switching freq. 20 KHz.

(ii) Error Processor

It consists of an amplifier and a lead lag compensation network with the following transfer function :

$$F_E(s) = \frac{193.3\ [(1+f/20)/(1+f/0.3)]}{(1+f/1225)\ /\ (1+f/3263)}$$

(iii) Pulsewidth Modulator :

As shown in Appendix C, the describing function of the PWM for unity pulse train be

$$K_m = \frac{1}{V_p}$$

If τ_d is the time delay from the signal d(t) to the power switch, the transfer function of PWM be

$$F_m(s) = (1/A_o T_p) e^{-j\omega\tau_d}$$

The slope A_o of the fixed ramp A(t) is given as

$$A_o = 6.25 \times 10^4 \text{ V/S}$$

and $\tau_d = 8\text{uS}$

Objective :

(1) To analyse the effect of approximations on attenuation of two stage filter.

(2) To analyse the effect of approximations on output Impedence of two stage Input filter.

(3) To analyse the effect of Input filters on Duty cycle to output voltage transfer characteristic.

(4) To analyse the effect of Input filters on Open loop transfer characteristic.

(5) To analyse the effect of Input filter on Audiosusceptibili

Observations :

(1) A computer program with the following algorithm was developed for exact and approximate value of Attenuation. See fig. 4.1.

1. Read all the input parameters.
2. Initialize Vout
3. Calculate V_I

4. Calculate Attenuation = V_{OUT}/V_I

5. Calculate approximate Attenuation from eqn. (3.2.16).

6. Increment in frequency AI = AI+50.

7. GO TO 3 if AI ≤ 5000, otherwise STOP.

A complete print-out of the program is placed in the last.

Both the values, i.e. exact attenuation and approximate attenuation are plotted in graph 1. (.) represents exact values whereas (X) represents approximate values. It can be seen from the graph that although approximate values differ greatly from exact values at low frequencies, approximate curve more or less coincides with the exact curve at higher frequencies. Therefore, the approximations in eqn. 3.2.16 holds good for higher frequencies and for analysis purposes this equation may directly be used at switching frequency.

From graph, resonant peaking of H(s) at first stage (BF_1) and second stage (BF_2) are 2.0 and 0.33 respectively.

(2) Similarly a program was developed for output impedance of input filter for approximate value by considering first stage only, exact value and approximate value from eqn. (3.2.15) by neglecting R_1. These are plotted in graph 2. (.) represents exact value, (x) represents approximate value by considering first stage only. When we neglect R_1 the resonant peaking of Z(s) comes out at 2.02. From this graph it can be seen that the exact resonant peaking of Z(s), B_{R_1} and B_{R_2} are 3.68 and 2.23 respectively whereas approximate resonant peaking BR is 2.13. It can also be seen that the peaking at first stage

resonant freq. is more than that of second stage. Therefore our approximation in peaking limit of Z(s) by considering first stage only holds good.

Duty cycle-to-output voltage transfer characteristic, open loop transfer characteristic of switching regulator and audiosusceptibility vs freq. are plotted in graph 3,4 &5 respectively for the three systems of Table 2.

(3) If we compare the duty cycle to output transfer function of two stage and single stage input filter in graph 3. We can see that a severe penalty on the regulator loop performance has to be paid in order to match the weight of a single stage filter with a two stage filter and if we match peaking constraints, filter weight has to be increased considerably.

(4) Graph 4 illustrates the open loop Bode plots for the three systems. Rather disturbed open loop gain and phase at filter resonant frequency can be seen for single stage filter which results in an unstable system for example 2. Considerably better performance is shown using the two stage filter design.

(5) Graph 5 illustrates the audiosusceptibility of the regulator for the three systems. It can be seen that even using the input filter design of example 3, there exists significant degradation effect due to the input filter resonance of H(s). Again the worst care is shown with the single stage filter design of system 2 and two stage filter gives better performance.

Duty cycle to output transfer function and open loop performance of switching regulator without any input filter are plotted on graph 6 & 7 respectively. We can see that there is no peaking in the absence of Input filter.

Exercise 2.

One more switching converter which we are using in many systems in Research and Development Division of M/s. Indian Telephone Industries Limited, Naini, was also studied. A single stage input filter, the circuit parameters of which are shown in Fig. 4.2, is used in this switching converter.

Given :

Components values as shown in Fig. 4.2

V_i = 20V

Rating 5V ; 4A $\therefore$ R_L = 1.25 Ω

$A_o = 7 \times 10^4$ V/S

T_p = 50 uS

Error processor - same as in Exercise 1.

Objective :

To analyse the effect of Input filter on system performance.

Observations :

The open loop transfer characteristic and duty cycle to output transfer function are illustrated in graph 8 & 9 respectively. We can see from the graph that since

comparatively large input filter was used, the peakings are reduced. But still in audiosusceptibility graph 10 considerable peaking is obtained which again shows the disadvantage of single stage input filter.

Exercise 3 :

Graph 11 illustrates the exact and approximate attenuatio of the two stage input filter with following parameters.

L_1 = 1.1 mH

L_2 = 0.27 mH

C_1 = 225 uf

C_2 = 20 uf

R_1 = 0.05 mΩ

R_2 = 0.02 Ω

R_3 = 3.34 Ω

From graph it can be seen that resonant peaking of H(s). BF_1 & BF_2 are 1.35 and 0.25 respectively. Again exact and approximate values are same at high frequencies.

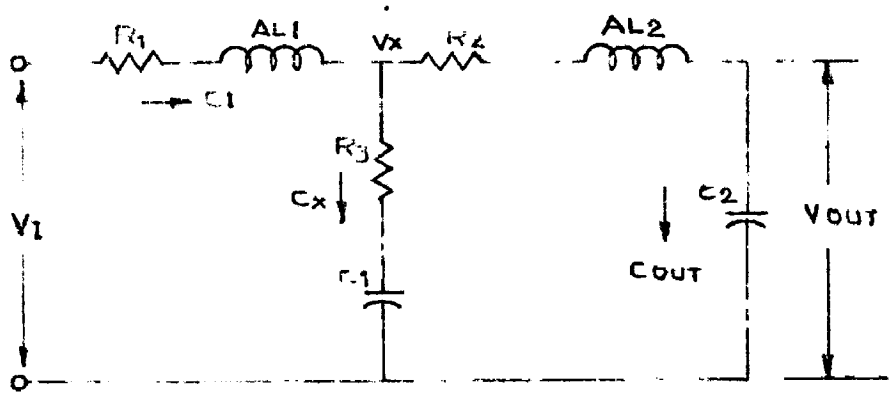


FIG. 4-1 : TWO STAGE INPUT FILTER

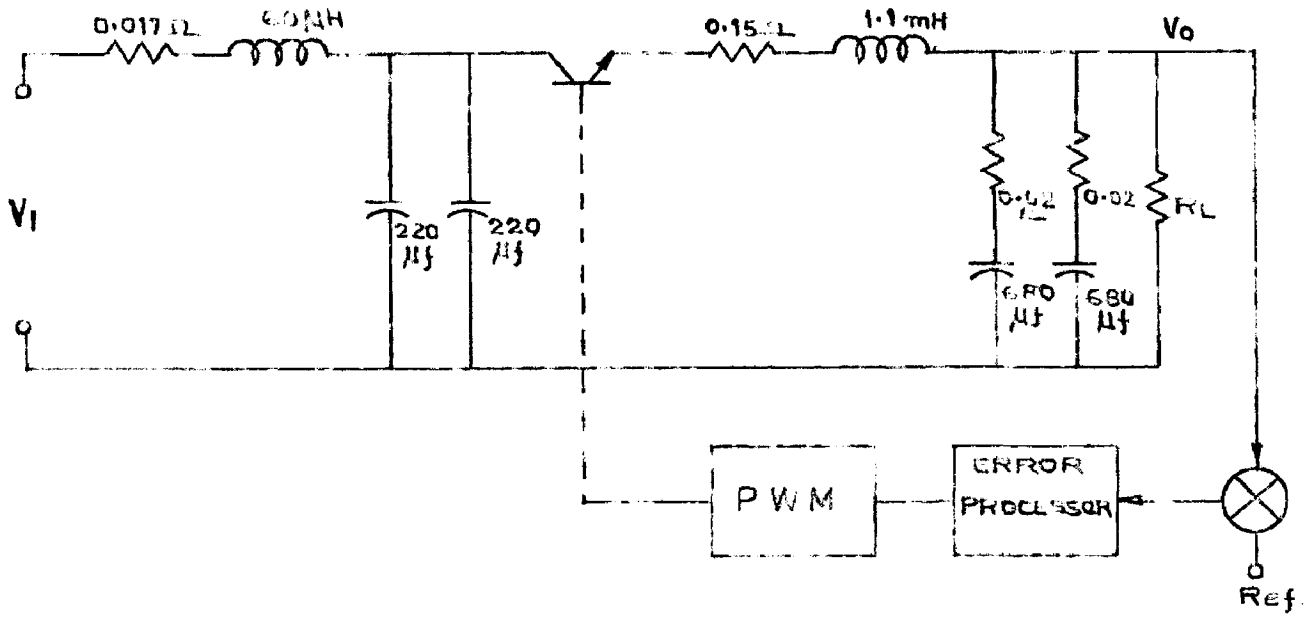
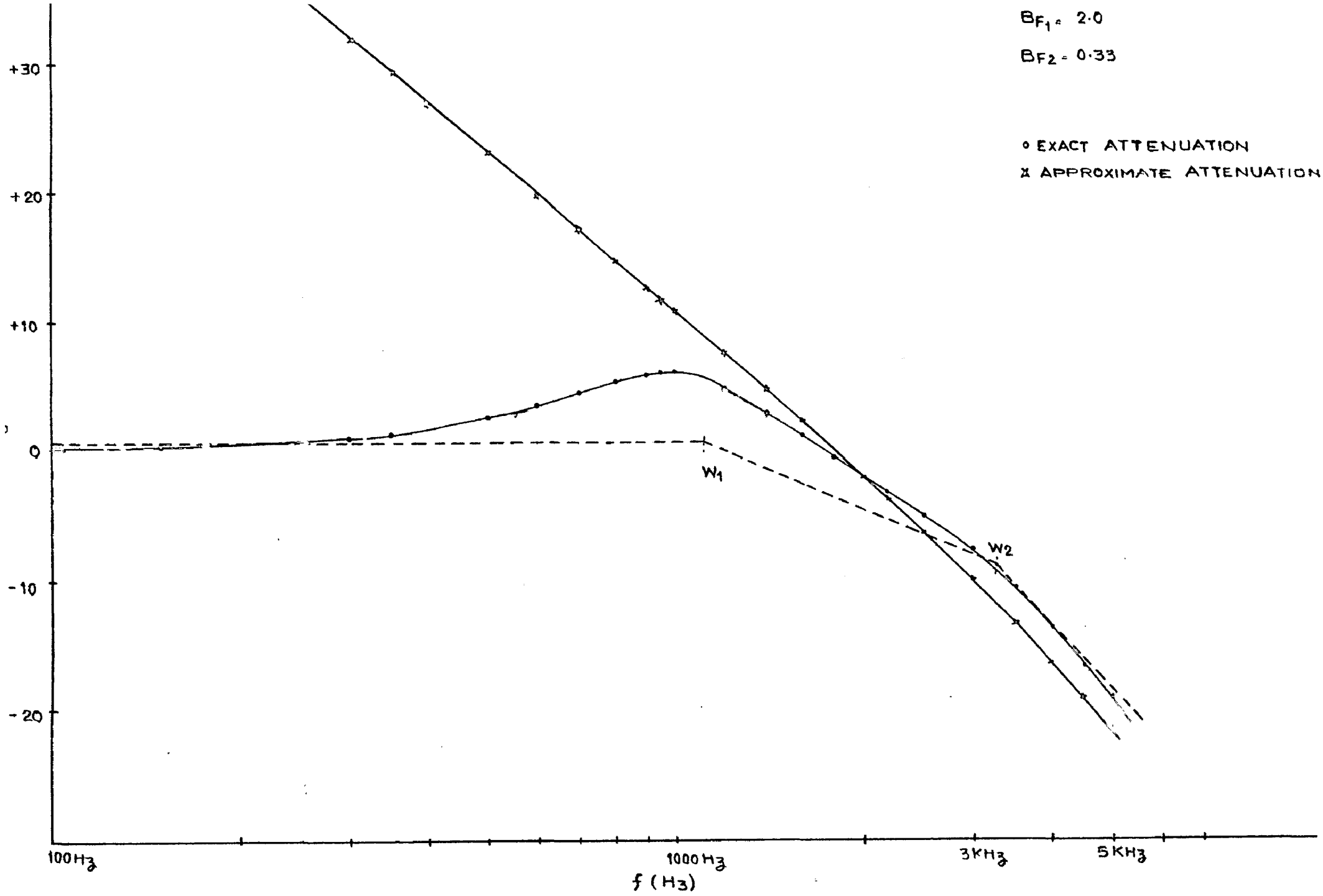
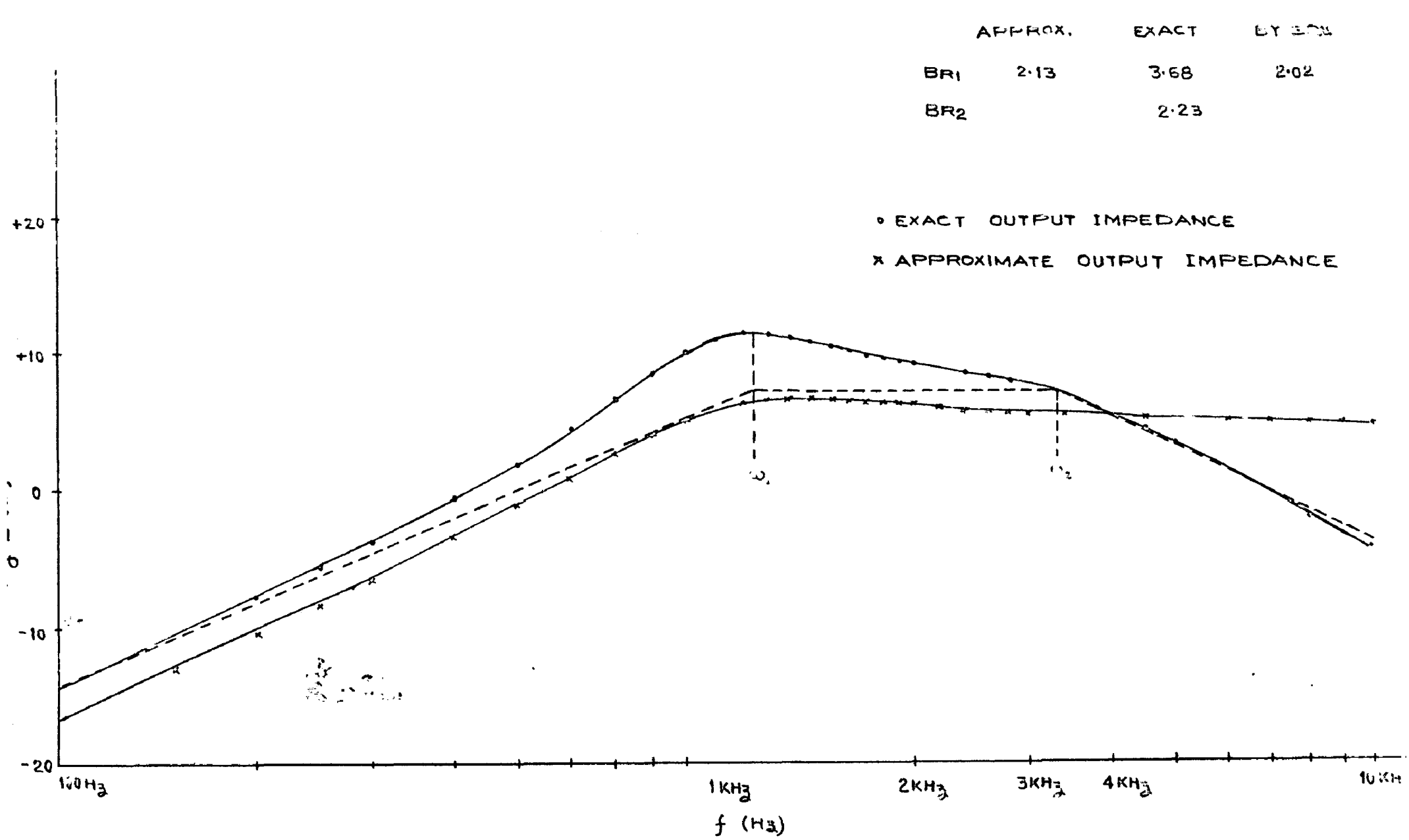
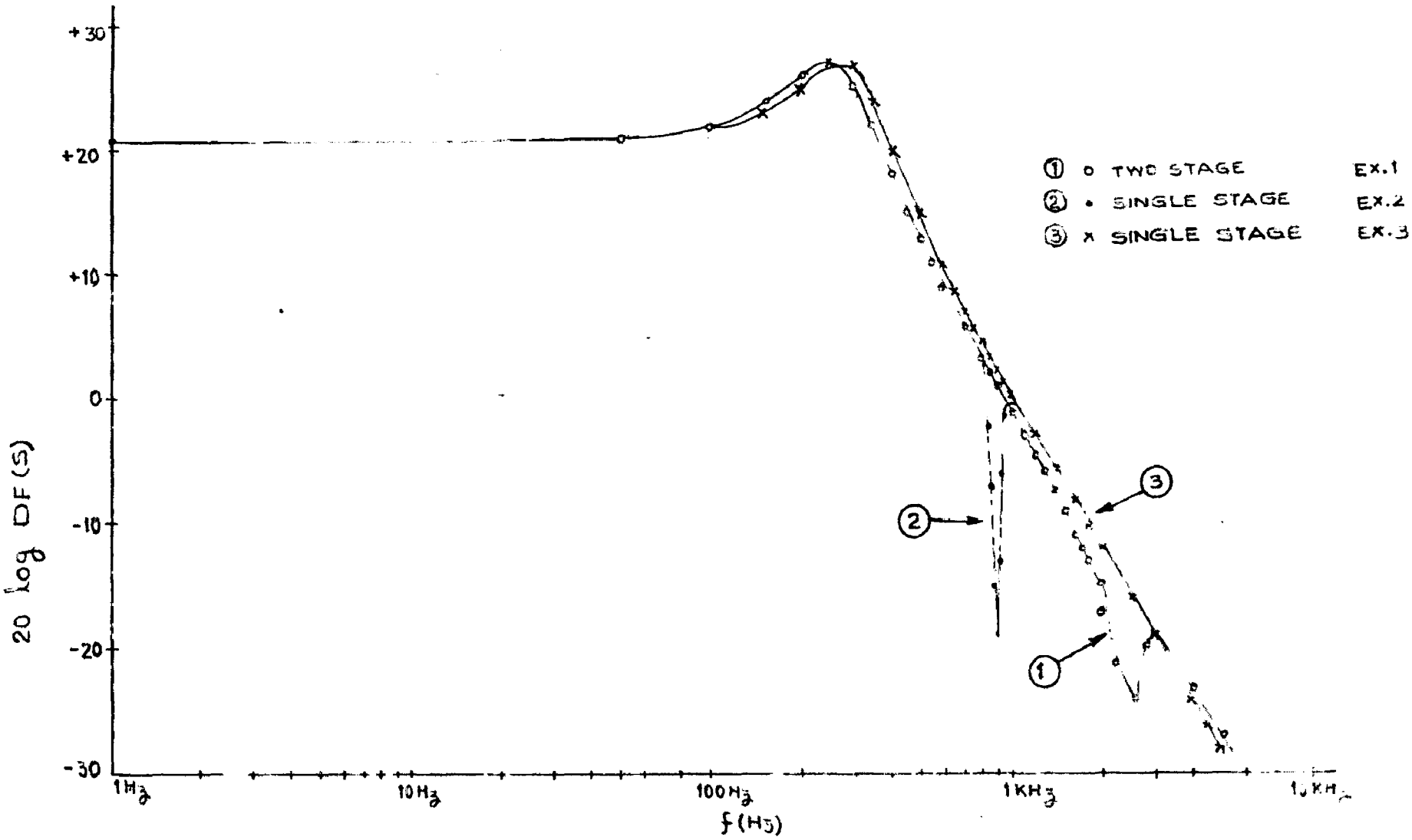


FIG 4-2 SWITCHING MODE CONVERTER OF R & D DIVISION
I.T.I. LTD., NAINI

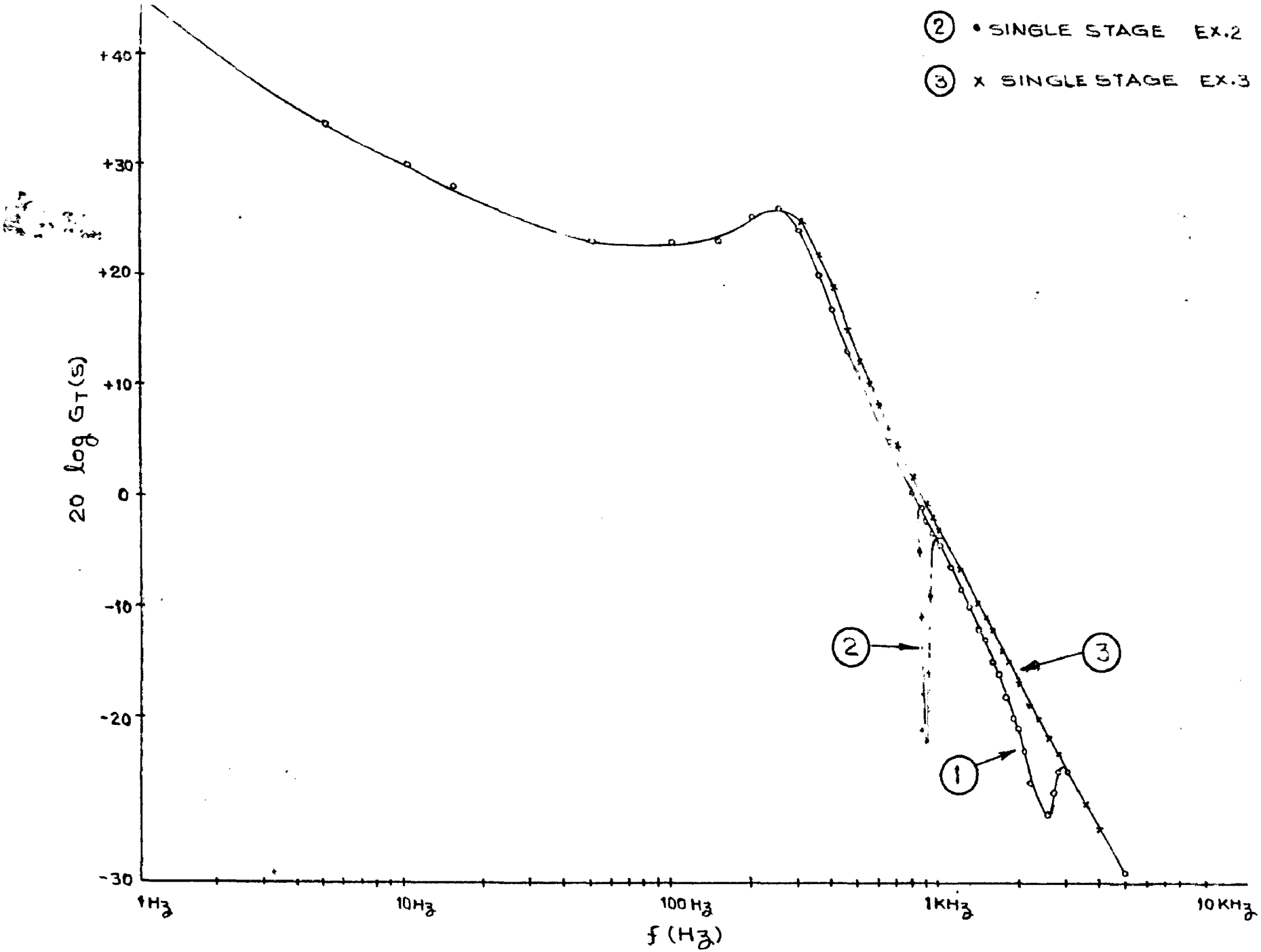

B_{F_1} = 2·0
B_{F_2} = 0·33
o EXACT ATTENUATION
x APPROXIMATE ATTENUATION
+30
+20
+10
0
-10
-20
W_1
W_2
100H3
1000H3
3KH3
5KH3
f (H3)



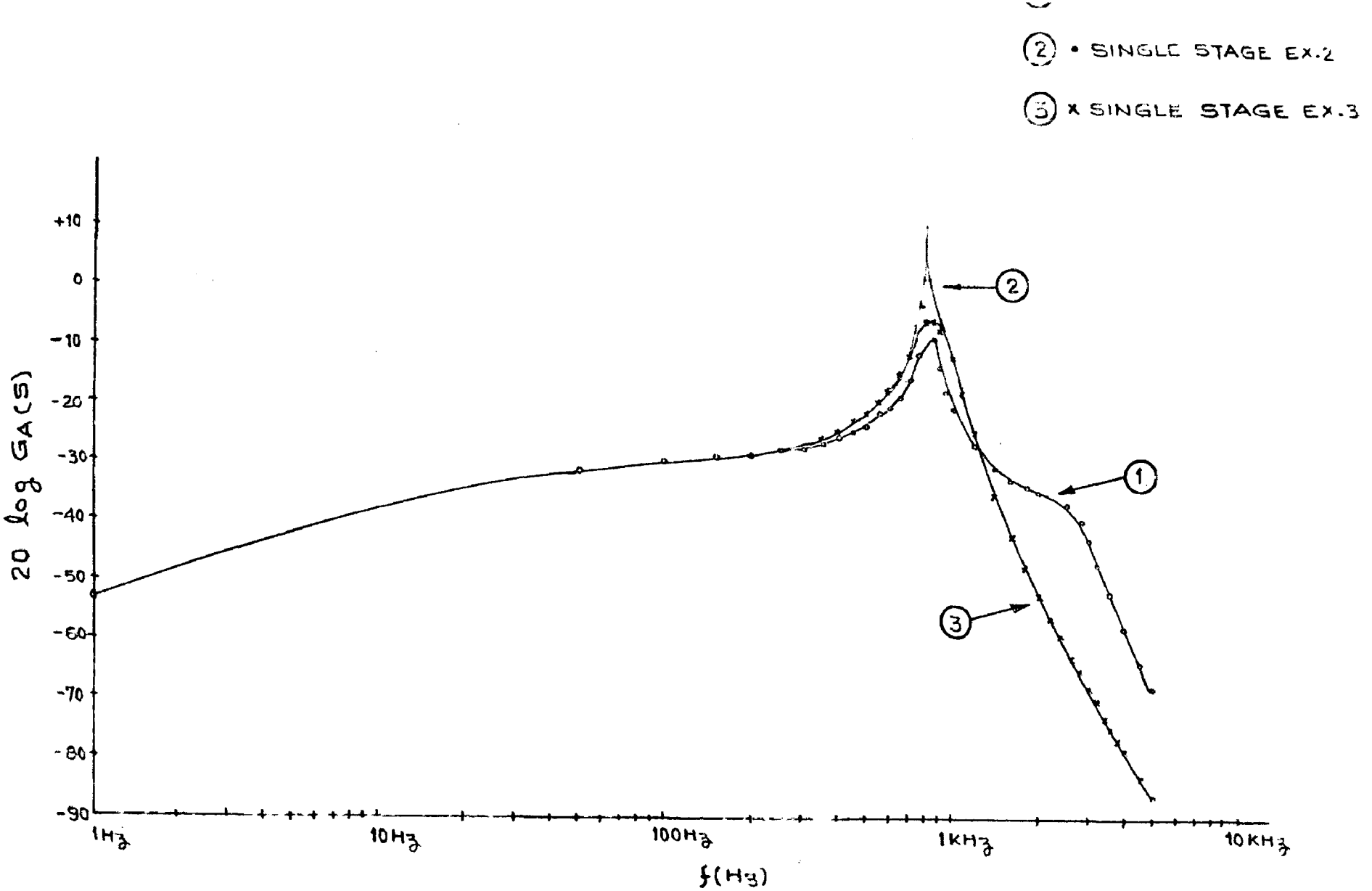
GRAPH 2: APPROXIMATE & EXACT OUTPUT IMPEDANCE OF TWO STAGE INPUT



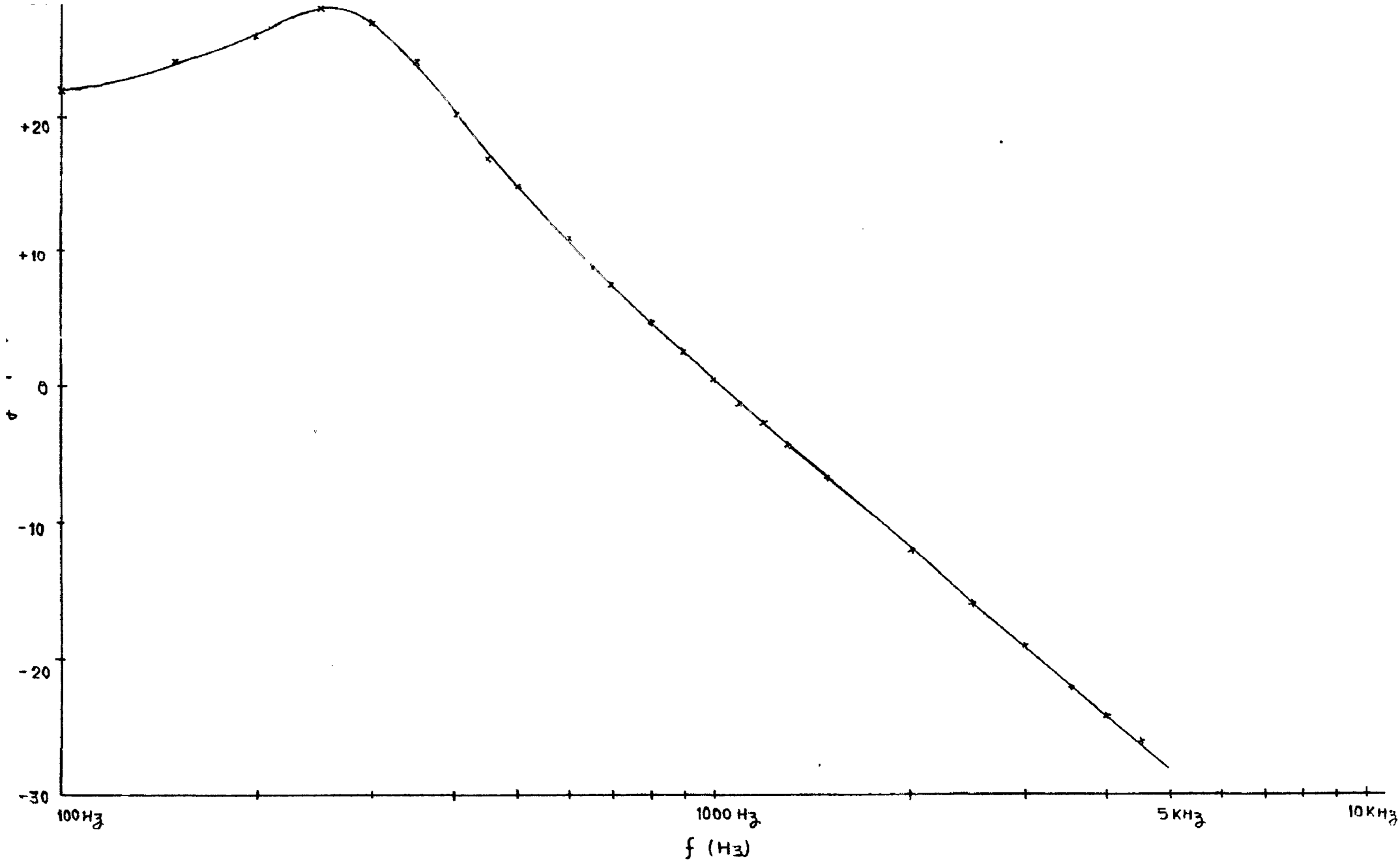
GRAPH 3: DUTY CYCLE TO OUTPUT VOLTAGE TRANSFER CHARACTERISTIC



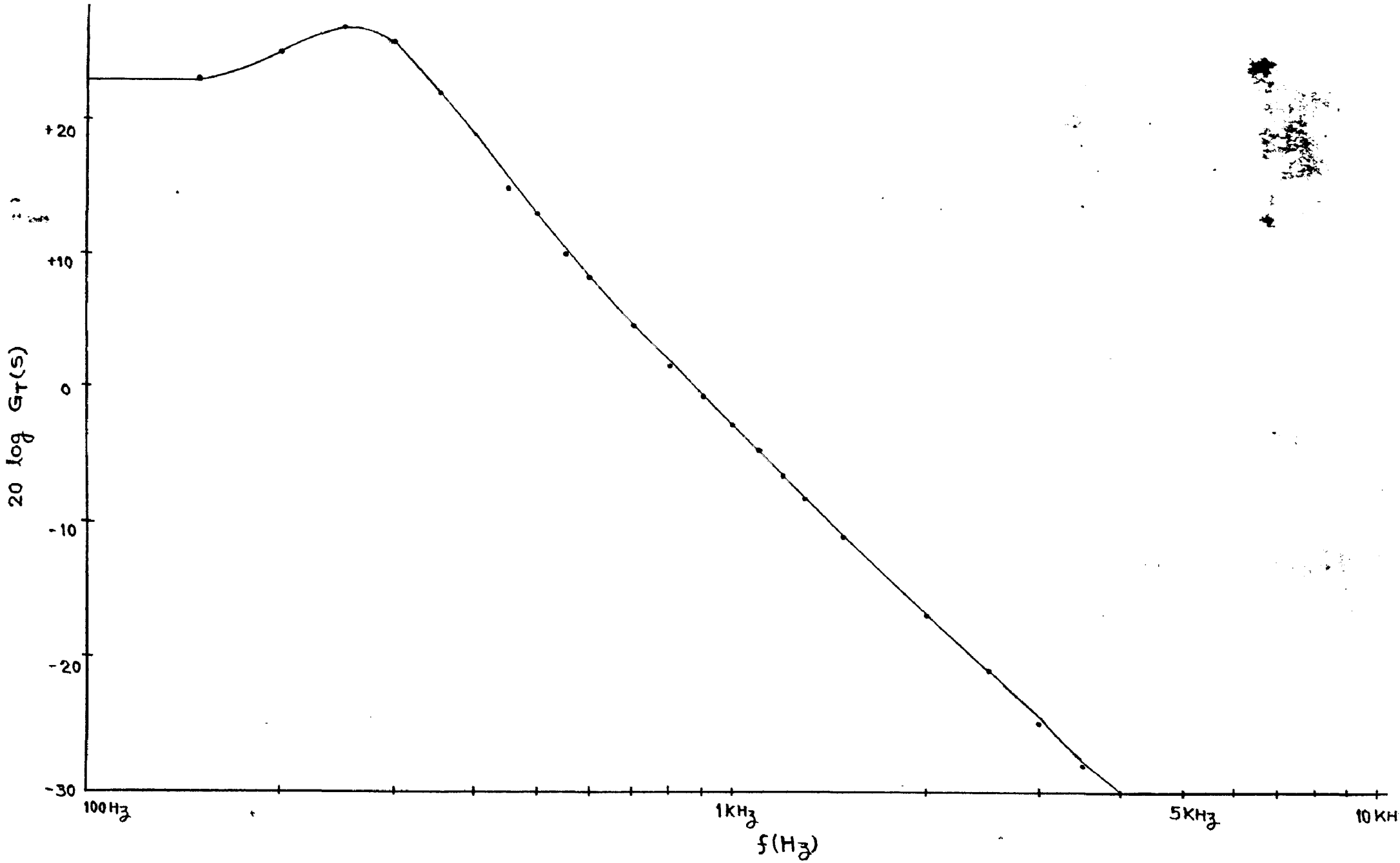
GRAPH 4 : OPEN LOOP TRANSFER CHARACTERISTIC



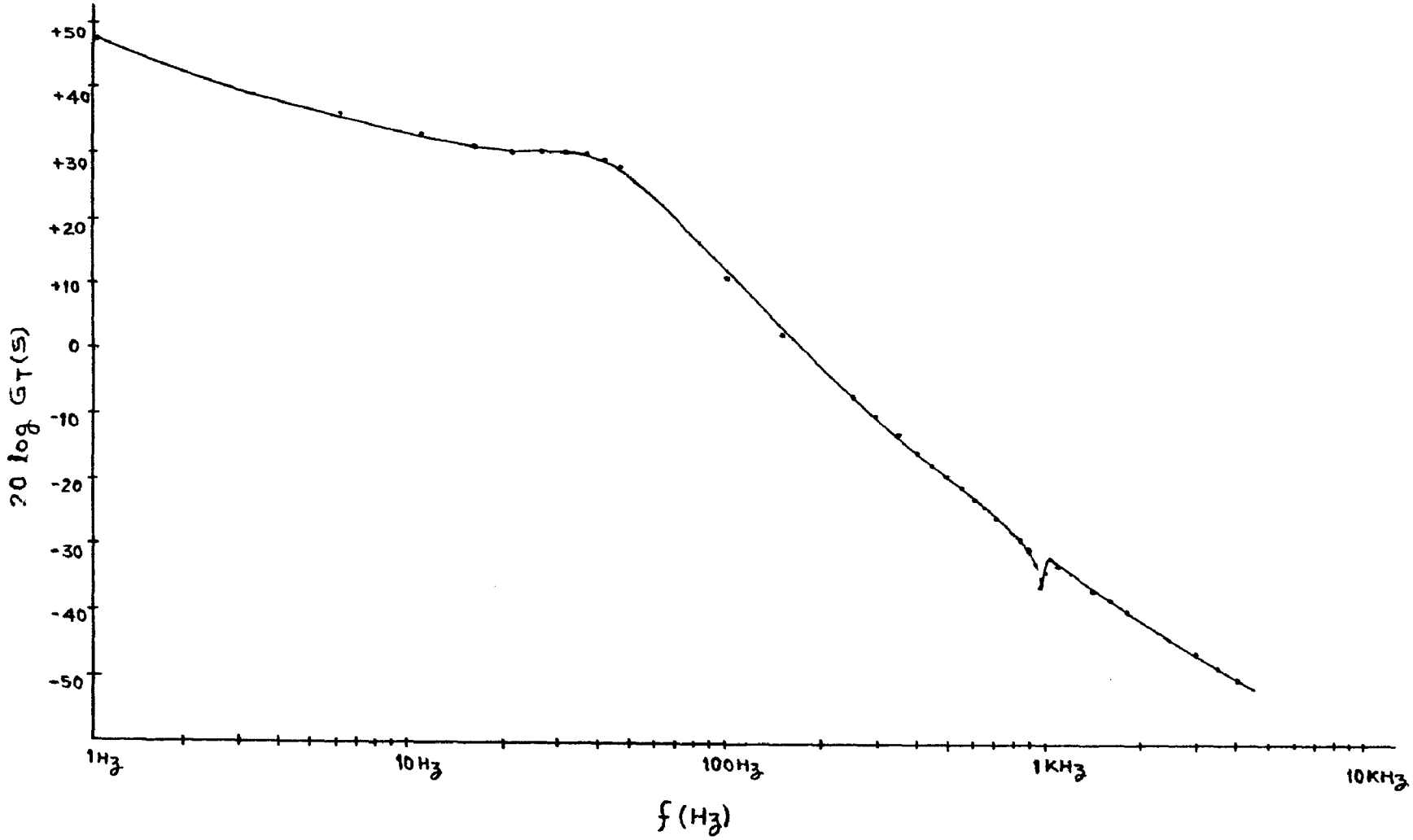
GRAPH 5 : AUDIOSUSCEPTIBILITY



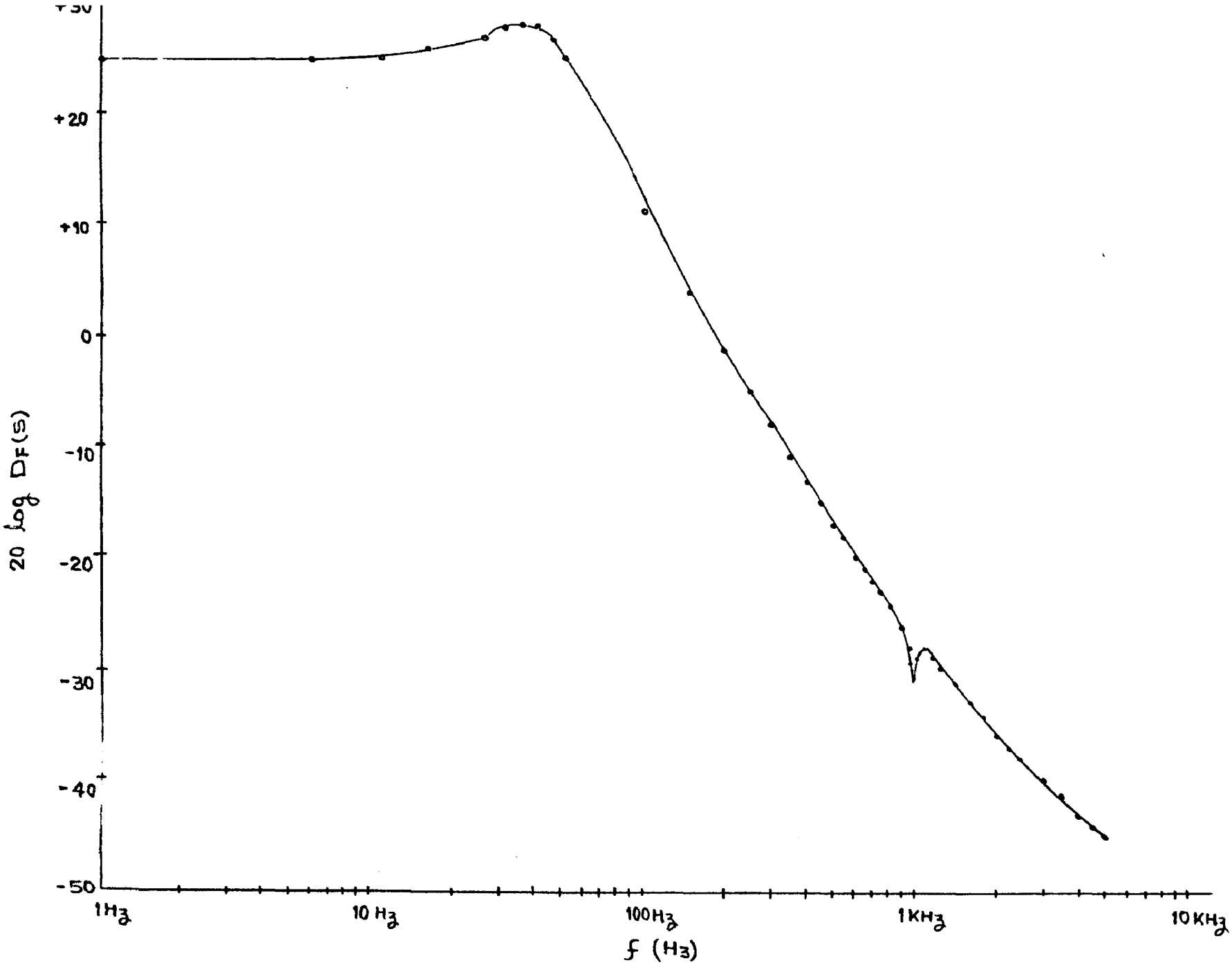
GRAPH 6 : DUTY CYCLE TO OUTPUT TRANSFER FUNCTION WITHOUT INPUT FILTER



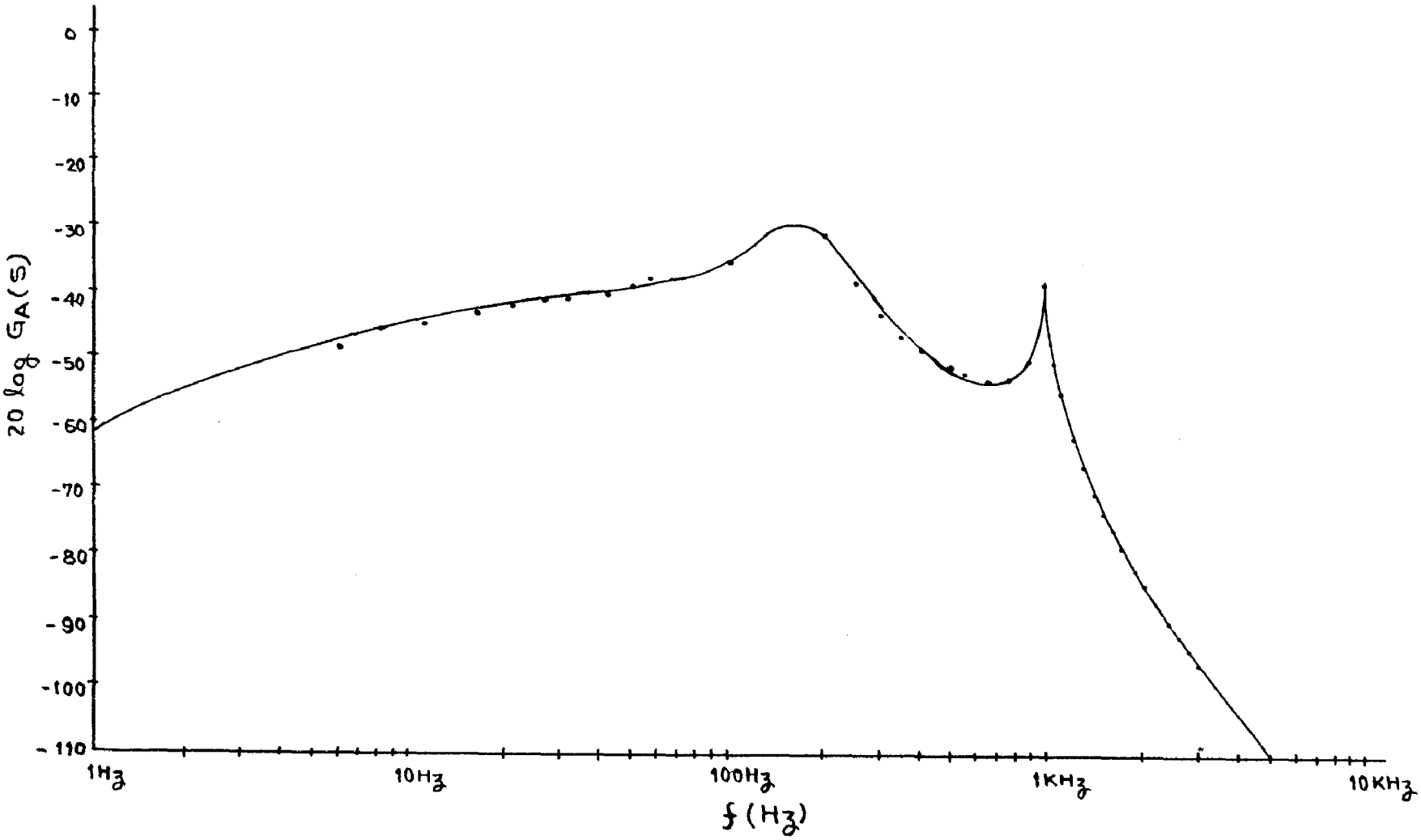
RAPH 7 : OPEN LOOP TRANSFER CHARACTERISTIC WITHOUT INPUT FILTER



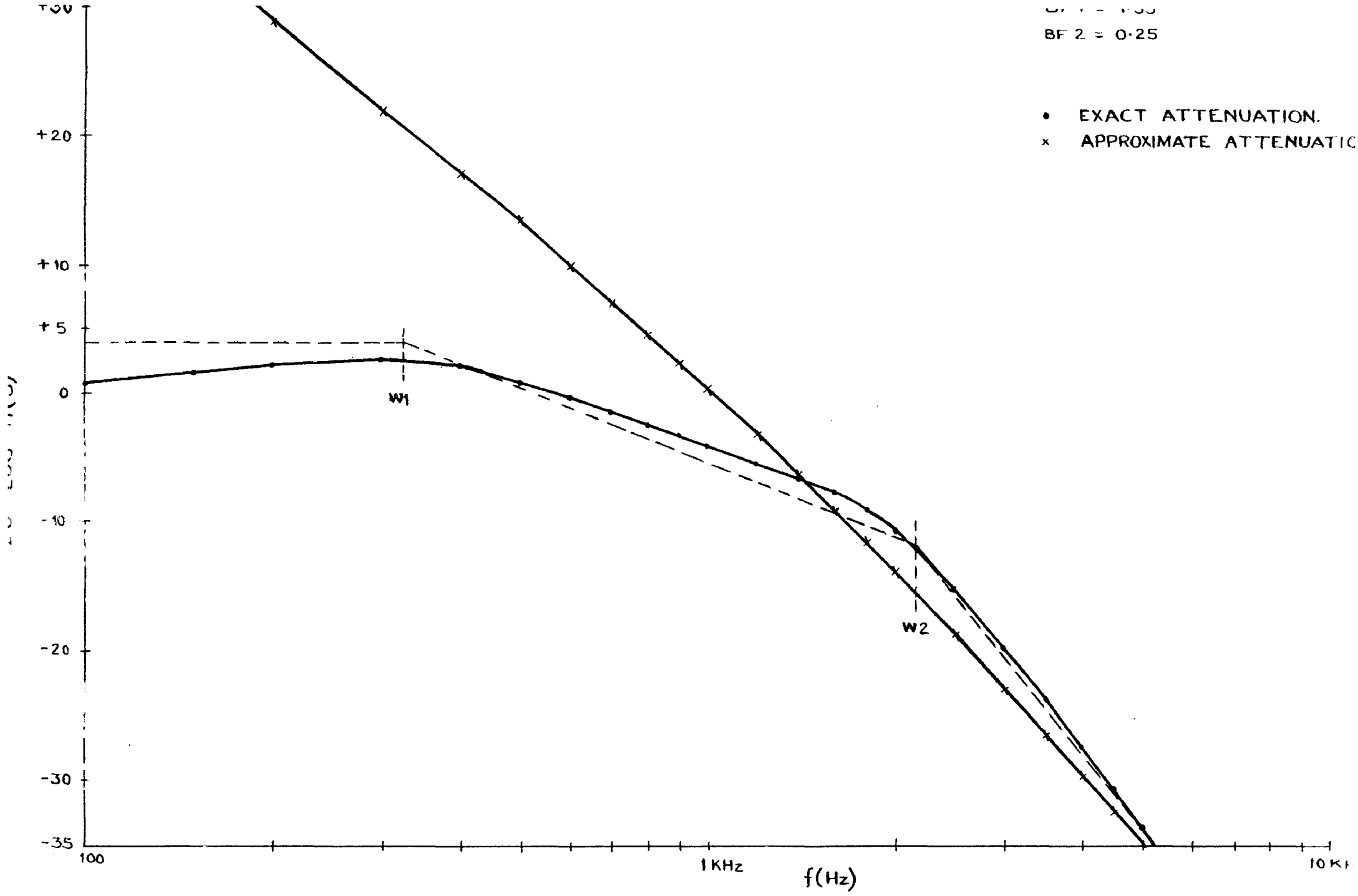
GRAPH 8 : OPEN LOOP TRANSFER CHARACTERISTIC



GRAPH 9 : DUTY CYCLE TO OUTPUT TRANSFER FUNCTION



GRAPH 10 : AUDIOSUSCEPTIBILITY



GRAPH 11 : EXACT & APPROXIMATE ATTENUATION

C H A P T E R-V

DISCUSSION AND CONCLUSION

A general method for modelling power stages of any switching dc-to-dc converter has been developed through the state space approach. The fundamental step is in replacement of the state space descriptions of the two switched networks by their average over the single switching period T, which results in a single continuous state space equation description designated the basic averaged state space model.

The subsequent perturbation and linearization step under the small signal assumption (2.3.12) leads to the final state space averaged model given by (2.3.13) and (2.3.14). These equations then serve as the basis for development of canonical circuit model. Different converters are represented simply by an appropriate set of formulas (2.3.27) and (2.3.28) for four elements in this general equivalent circuit. From the canonical circuit model, various perfomance characteristics of different switching converters can be compared in a quick and easy manner.

With the help of State Space Averaging technique, a small signal average model of switching mode regulator is derived to investigate analytically the complex interaction among input filter, output filter and control loop which often causes degradation of regulator performances. Analytically based design constraints are formulated. It is concluded that the minimization of the forward transfer characteristic H(s) and the output impedance Z(s) of input filter at filter resonance

are key to designing an input filter. But minimizing H(s) and Z(s) at resonance for a conventional single stage filter results weight and loss penalties. Therefore we conclude that :

Single stage filters are generally much heavier than two stage filters under identical design constraints and for the same filter weight design, a single stage filter has much higher filter resonant peakings B_F and B_R than those of a two stage filter. Therefore using a two stage input filter which is capable of reducing H(s) and Z(s) at resonance without significantly increasing weight and loss is more advantageous.

Some approximations were made in optimum design constraints. It was shown that these approximations do not affect the performance and optimum designing of switching mode converters and these equations can directly be used, thus saving a valuable computer time.

SCOPE FOR FURTHER WORK :

The insights that have emerged from the general state space modelling approach suggest that there is a whole field of new switching dc-to-dc converter power stages yet to be conceived. The state-space modelling approach discussed in this dissertation is for two state switching converters only. This method can be extended to multiple - state converters e.g. power stages operated in the discontinuous conduction mode, and dc-to-ac switching inverters in which a specific output waveform is 'assembled' from discrete segments. Some efforts have been made by Fred C.Y.Lee, Ralph P. Iwens, Yuan Yu, James E.Triner[3] &[4] for discontinuous conduction mode but they have not

considered the effect of Input filter in that case. Further work can be done by considering input filter also.

Further, component ratings of first and second order filter have not yet been determined. Multiple feedback systems and adaptive control system may also be considered. Feed-forward method of controlling audiosusceptibility can also be investigated.

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APPENDIX A

Consider Buck type switching converter with input filter as shown in Fig. 1.

If we define a state vector x(t) with components $x_1(t)=v_{c1}(t)$ $x_2(t) = v_{c2}(t)$, $x_3(t) = i_1(t)$ and $x_4(t) = i_2(t)$ i.e.

$$x(t) = \begin{bmatrix} v_{c1}(t) \\ v_{c2}(t) \\ i_1(t) \\ i_2(t) \end{bmatrix}$$

then the response of the network can be represented by

$$\dot{x} = Ax + b\,u(t)$$

During Ton

When switch is ON the above circuit becomes as shown in Fig.2.

$$E_{in} = R_1 i_1 + L_1 \frac{d_{i1}}{dt} + v_{c1} + R_3(i_1-i_2)$$

$$v_{c1} = \frac{1}{C_1}\int(i_1-i_2)dt$$

$$\dot{v}_{c1} = \frac{1}{C_1} i_1 - \frac{1}{C_1} i_2 \qquad \ldots.(a)$$

$$\dot{i}_1 = -\frac{1}{L_1} v_{c1} - \frac{R_1+R_3}{L_1} i_1 + \frac{R_3}{L_1} i_2 + \frac{1}{L_1} E_{in} \qquad ..(b)$$

$$v_{c2} = \frac{1}{C_2}\int\left(i_2 - \frac{V_o}{R_1} \right) dt$$

But $V_o = v_{c2} + R_4\left(i_2 - \frac{V_o}{R_1}\right)$

or $V_o\left(\frac{R_L+R_4}{R_2}\right) = v_{c2} + R_4 i_2$

or $\frac{V_o}{R_L} = \frac{1}{R_L + R_4}(v_{c2}+R_4 i_2)$

$\therefore \dot{v}_{c2} = \frac{1}{C_2}\left[i_2 - \frac{1}{R_L+R_4} (v_{c2}+R_4 i_2)\right]$

$= \frac{1}{C_2}\left[- \frac{1}{R_L+R_4} v_{c2} + \frac{R_L}{R_L+R_4} i_2\right]$

$$\dot{v}_{c2} = - \frac{1}{C_2(R_L+R_4)} v_{c2} + \frac{R_L}{C_2(R_L+R_4)} i_2 \qquad ...(c)$$

$$v_{c1}+R_3(i_1-i_2) - \frac{R_L}{R_L + R_4}(v_{c2}+R_4 i_2) = R_2 i_2 + L_2 \frac{di_2}{dt}$$

$$L_2 \frac{di_2}{dt} = v_{c1} - \frac{R_L}{R_L+R_4} v_{c2} + R_3 i_1 - (R_3 + \frac{R_L R_4}{R_L + R_4} + R_2) i_2$$

$$i_2 = \frac{1}{L_2} v_{c1} - \frac{R_L}{L_2(R_L+R_4)} v_{c2} + \frac{R_3}{L_2} i_1 - \left[\frac{R_2+R_3}{L_2} + \frac{R_L R_4}{L_2(R_L+R_4)}\right] i_2 \qquad ...(d)$$

If we put eqn (a) to (d) in matrix form :

$$\begin{bmatrix} \dot{v}_{c1}(t) \\ \dot{v}_{c2}(t) \\ \dot{i}_1(t) \\ \dot{i}_2(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{1}{C_1} & -\frac{1}{C_1} \\ 0 & \frac{1}{C_2(R_L+R_4)} & 0 & \frac{R_L}{C_2(R_L+R_4)} \\ -\frac{1}{L_1} & 0 & \frac{R_1+R_3}{L_1} & \frac{R_3}{L_1} \\ \frac{1}{L_2} & -\frac{R_L}{L_2(R_L+R_4)} & \frac{R_3}{L_2} & -\frac{R_2+R_3}{L_2} + \frac{R_L R_4}{L_2(R_L+R_4)} \end{bmatrix}$$

$$\begin{bmatrix} v_{c1}(t) \\ v_{c2}(t) \\ i_1(t) \\ i_2(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 1/4_1 \\ 0 \end{bmatrix} E_{in}$$

During TOFF :

When switch is OFF the Buck power stage becomes as shown in Fig.3

$$v_{c1} = \frac{1}{C_1}\int i_1 \, dt$$

$$\therefore \quad \dot{v}_{c1} = \frac{1}{C_1} \; i_1 \qquad \ldots(a')$$

$$E_{in} = R_1 i_1 + L_1 \frac{di_1}{dt} + v_{c1} \mp R_3 i_1$$

$$\therefore \quad \dot{i}_1 = -\frac{1}{L_1} \; v_{c1} - \frac{R_1+R_3}{L_1} \; i_1 + \frac{1}{L_1} \; E_{in} \qquad \ldots(b')$$

$$v_{c2} = \frac{1}{C_2}\int \left(i_2 - \frac{V_o}{R_L} \right) dt$$

But $$V_o = v_{c2} + R_4\left(i_2 - \frac{V_o}{R_L}\right)$$

From eqn (C)

$$\dot{v}_{c2} = -\frac{1}{C_2(R_L+R_4)} \; v_{c2} + \frac{R_L}{C_2(R_L+R_4)} \; i_2 \qquad \ldots\ldots(c')$$

$$R_2 i_2 + L_2 \frac{di_2}{dt} + V_o = 0$$

or $$R_2 i_2 + L_2 \frac{di_2}{dt} + \frac{R_L}{R_L+R_4} \; (v_{c2} + R_4 i_2) = 0$$

or $$\dot{i}_2 = -\frac{1}{L_2} \; \frac{R_L}{(R_L+R_4)} \; v_{c2} - \frac{1}{L_2}\left(R_2 + \frac{R_L R_4}{R_L+R_4}\right) i_2 \qquad \ldots(d')$$

Combining eqn (a) to (d)

$$\begin{bmatrix} \dot{v}_{c1} \\ \dot{v}_{c2} \\ \dot{i}_1 \\ \dot{i}_2 \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{1}{C_1} & 0 \\ 0 & -\frac{1}{C_2(R_L+R_4)} & 0 & \frac{R_L}{C_2(R_L+R_4)} \\ \frac{1}{L_1} & 0 & -\frac{R_1+R_3}{L_1} & 0 \\ 0 & -\frac{R_L}{L_2(R_L+R_4)} & 0 & -\frac{1}{L_2}\left(R_2+\frac{R_L R_4}{R_L+R_4}\right) \end{bmatrix} \begin{bmatrix} v_{c1}(t) \\ v_{c2}(t) \\ i_1(t) \\ i_2(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 1/ \\ 0 \end{bmatrix}$$

Therefore

$$A_1 = \begin{bmatrix} 0 & 0 & \frac{1}{C_1} & -\frac{1}{C_1} \\ 0 & -\frac{1}{C_2(R_L+R_4)} & 0 & \frac{R_L}{C_2(R_L+R_4)} \\ -\frac{1}{L_1} & 0 & -\frac{R_1+R_3}{L_1} & \frac{R_3}{L_1} \\ \frac{1}{L_2} & -\frac{R_L}{L_2(R_L+R_4)} & \frac{R_3}{L_2} & -\left\{\frac{R_2+R_3}{L_2}+\frac{R_L R_4}{L_2(R_L+R_4)}\right\} \end{bmatrix}$$

$$A_2 = \begin{bmatrix} 0 & 0 & \frac{1}{C_1} & 0 \\ 0 & -\frac{1}{C_1(R_L+R_4)} & 0 & \frac{R_L}{C_2(R_L+R_4)} \\ -\frac{1}{L_1} & 0 & -\frac{R_1+R_3}{L_1} & 0 \\ 0 & -\frac{R_L}{L_2(R_L+R_4)} & 0 & -\frac{1}{L_2}\left(R_2+\frac{R_L R_4}{R_L+R_4}\right) \end{bmatrix}$$

$$b_1 = b_2 = \begin{bmatrix} 0 \\ 0 \\ 1/L_1 \\ 0 \end{bmatrix}$$

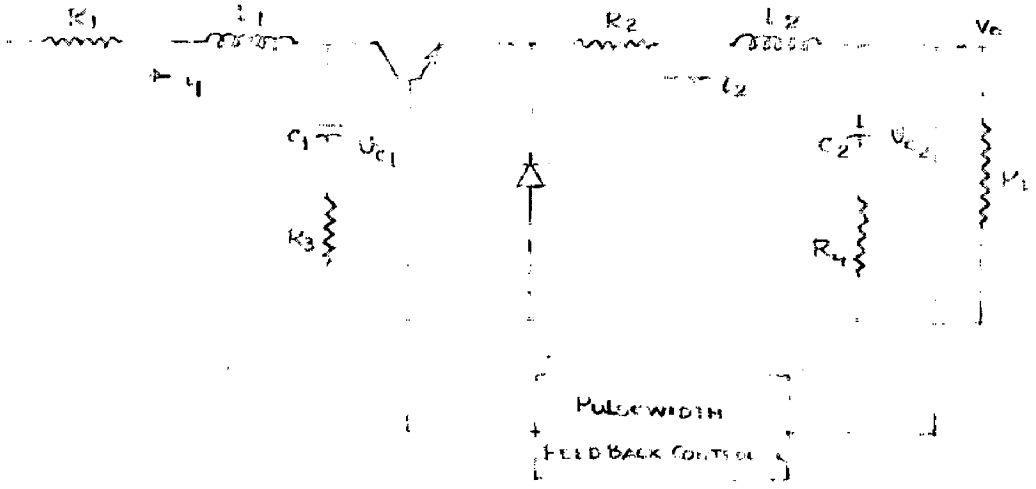

FIG. 1 BUCK TYPE SWITCHING CONVERTER WITH INPUT FILTER

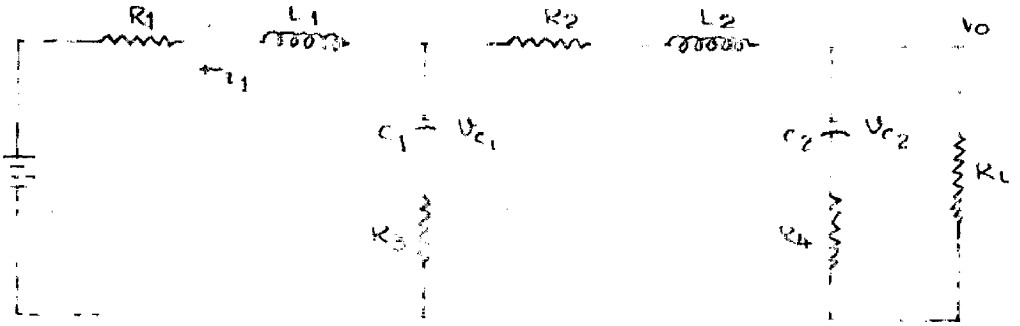

FIG 2. BUCK CONVERTER WHEN SWITCH IS ON

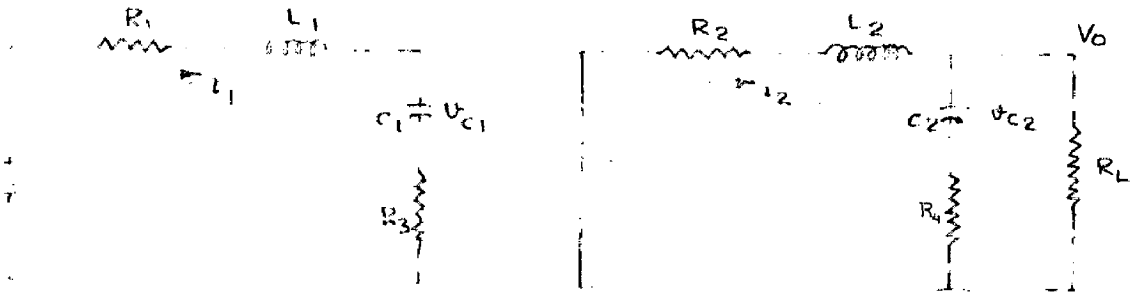

FIG 3 BUCK CONVERTER WHEN SWITCH IS OFF

APPENDIX B

The fundamental approximation in the state-space averaging approach :

Let the two linear system be described by

(i) interval Td ; $0 < t < t_o$ (ii) interval Td' . $t_o < t < T$

$$\dot{x} = A_1 x \qquad \dot{x} = A_2 x \qquad \ldots(a)$$

The exact solutions of these state space equations are :

$$x(t) = e^{A_1 t} x(o) \qquad t \in [0, t_o]$$

$$x(t) = e^{A_2 (t-t_o)} x(t_o) \qquad t \in [t_o, T] \qquad \ldots(b)$$

The state-variable vector x(t) is continuous across the switching instant t_o, and so :

$$x(T) = e^{A_2 (T-Td)} x(t_o)$$

$$= e^{d'A_2 T} e^{dA_1 T} x(o) \qquad \ldots(c)$$

Now if we introduce following approximation in above equation

$$e^{d'A_2 T} e^{dA_1 T} \simeq e^{(dA_1 + d'A_2) T} \qquad \ldots(d)$$

resulting in an approximate solution

$$x(T) \simeq e^{(dA_1 + d'A_2) T} x(o) \qquad \ldots(e)$$

However, this is the same as the solution of the following linear system equation for x(T) :

$$\dot{x} = (dA_1 + d'A_2)x \qquad \ldots(f)$$

The last model (f) is, therefore, the averaged model obtained from the two switched models given by (a) and is valid provided approximation (d) is well satisfied. This is so if the following linear approximations of the fundamental matrices hold :

$$e^{dA_1 T} \simeq I + dA_1 T$$

$$e^{d'A_2 T} \simeq I + d'A_2 T$$

In essence, (d) is the first approximation to the general series :

$$AT = (dA_1 + d'A_2)T + dd' (A_1A_2 - A_2A_1)T^2 + \ldots\ldots$$

where $e^{AT} = e^{d'A_2 T} \; e^{dA_1 T}$

Hence, when two matrices are commutative, that is $A_1A_2 = A_2A_1$, then $A = dA_1 + d'A_2$ and (d) becomes an exact result.

APPENDIX C

The Pulsewidth modulated signal was obtained by Dither method. In this method, the low frequency error signal $V_e(t)$ is compared with a high frequency dither signal, a fixed ramp A(t). As shown in fig. 4(a) the resulting signal e(t) is fed into a relay element. The output of the relay element is a pulse-train of magnitude V, described as

$$d(t) = \begin{cases} V & \text{if } A(t) \leq V_e(t) \\ 0 & \text{otherwise} \end{cases} \qquad \ldots \text{(i)}$$

Input and output waveforms of PWM are shown in Fig. 4(b) and 4(c) respectively. Since the dither frequency is significantly higher than the frequency of error signal $V_e(t)$, the error signal can be modelled as a bias over one dither cycle as shown in fig. 5(b). The Input-output relation for PWM is shown in Fig. 5(a).

Thus, the describing function of PWM be

$$K_m = \frac{d_{av}}{V_e} \qquad \ldots \text{(ii)}$$

From fig. 5(b) the average output is given by

$$d_{av} = \frac{1}{T_p} V.t_1$$

$$= \frac{V.\ V_e}{V_p} \qquad \ldots \text{(iii)}$$

```
INPUT FILTER DESIGN FOR SWITCHING REGULATORS
EVALUATION OF OPEN LOOP GAIN AND AUDIOSUSCEPTIBILITY
WITH TWO STAGE INPUT FILTER
PROGRAMMED BY P.K. GUPTA
REAL L,L1
READ I,AO,TP,TD,L,C,L1,C1,VI,VO,RL,RL1,RC,R1,AK,F1,F2,F3,F4
FORMAT(7E10.1,F9.4/F8.4,8F9.4/F9.4)
READ 50,R2,R3,AL2,C2
FORMAT(2F9.4,2E10.1)
AL1=L1
D=VO/VI
IO=VO/RL
DO 10I=1,5001,50
AI=I
W=2.0*22.0/7.0*AI
FE=AK*((1.+AI/F1)/(1.+AI/F2))/((1.+AI/F3)/(1.+AI/F4))
PI=22.0/7.0
FMRE=1./(AO*TP)*COS(W*TD*PI/180.)
FMIM=-1./(AO*TP)*SIN(W*TD*PI/180.)
ZIRE=(RL+W**2*C**2*RC*RL*(RC+RL))/(1.+W*W*C*C*(RC+RL)**2)
ZIIM=-W*C*RL**2/(1.+W*W*C*C*(RC+RL)**2)
ZISRE=RL1+ZIRE
ZISIM=W*L+ZIIM
APPROXIMATE CALCULATION BY CONSIDERING FIRST STAGE ONLY:
Z1SRE=((R1*R3+AL1/C1)*(R1+R3)+(W*AL1*R3-R1/(W*C1))*(W*AL1-1.0/(
1 1)))/((R1+R3)**2+(W*AL1-1.0/(W*C1))**2)
Z1SIM=((W*AL1*R3-R1/(W*C1))*(R1+R3)-(W*AL1-1.0/(W*C1))*(R1*R3+A
1C1))/((R1+R3)**2+(W*AL1-1.0/(W*C1))**2)
Z1S=SQRT(Z1SRE**2+Z1SIM**2)
Z2RE=R2+Z1SRE
Z2IM=W*AL2+Z1SIM
ZSRE=(Z2RE*(1.0-Z2IM*W*C2)+Z2IM*W*C2*Z2RE)/((1.0-Z2IM*W*C2)**2+
1C2*Z2RE)**2)
ZSIM=(Z2IM*(1.0-Z2IM*W*C2)-Z2RE*W*C2*Z2RE)/((1.0-Z2IM*W*C2)**2+
```

```
     1C2*Z2RE)**2)
      ZS=SQRT (ZSRE**2+ZSIM**2)
      A=(D*D*ZSRE+ZISRE)**2+(D*D*ZSIM+ZISIM)**2
      FPRE=(ZIRE*(D*D*ZSRE+ZISRE)+ZIIM*(D*D*ZSIM+ZISIM))/A
      FPIM=(ZIIM*(D*D*ZSRE+ZISRE)-ZIRE*(D*D*ZSIM+ZISIM))/A
      FCRE=VI-ZSRE*IO*D
      FCIM=-ZSIM*IO*D
C     DUF IS DUTY CYCLE TO OUTPUT DESCRIBING FUNCTION
      DUFRE=FPRE*FCRE-FPIM*FCIM
      DUFIM=FPIM*FCRE+FPRE*FCIM
      ADUF=SQRT(DUFRE**2+DUFIM**2)
      PDUF=ATAN(DUFIM/DUFRE)
      GTRE=FE*FMRE*DUFRE-FE*FMIM*DUFIM
      GTIM=FE*FMIM*DUFRE+FE*FMRE*DUFIM
      AGTS=SQRT(GTRE**2+GTIM**2)
      PGTS=ATAN(GTIM/GTRE)
      DGTS=180./PI*PGTS
      DDUF=180./PI*PDUF
C     EVALUATION OF ATTENUATION
      VOUT=1.0
      COUTIM=W*C2
      VXRE=1.0-W*W*AL2*C2
      VXIM=W*C2*R2
      VX=SQRT (VXRE**2+VXIM**2)
      CXRE=(W*W*C1*C1*R3*VXRE-W*C1*VXIM)/(1.0+(W*C1*R3)**2)
      CXIM=(W*C1*VXRE+(W*C1)**2*VXIM)/(1.0+(1.0+(W*C1*R3)**2)
      CIRE=CXRE
      CIIM=CXIM+COUTIM
      CI=SQRT (CIRE**2+CIIM**2)
      VIRE=R1*CIRE-W*AL1*CIIM+VXRE
      VIIM=AL1*CIRE+R1*CIIM+VXIM
      VII=SQRT(VIRE**2+VIIM**2)
      HS=1.0/VII
      FPS=SQRT(FPRE**2+FPIM**2)
      GAS=D*HS*FPS/SQRT((1.+GTRE)**2+GTIM**2)
```

Put eq. (iii) in (ii) we get

$$K_m = \frac{V}{V_p}$$

And if the magnitude of output pulses are unity i.e. for unity pulse train

$$V = 1.$$

$$\therefore \quad \boxed{K_m = \frac{1}{V_p}}$$

```
      FM= SQRT(FMRE**2+FMIM**2)
      FC= SQRT(FCRE**2+FCIM**2)
      ADUFL= 20.0*ALOG10(ADUF)
      AGTSL= 20.0*ALOG10(AGTS)
      GASL= 20.0*ALOG10(GAS)
      PRINT 2, AI, W, FE, FC, FM, FPS, ADUF, ADUFL, PDUF, DDUF
2     FORMAT(5X, 5HFREQ=, I6, 2HHZ, 2X, 2HOR, 2X, F8.1, 4HRAD./5X, 6HFE(S)=, E1
     1, 2X, 6HFC(S)=, E10.3, 2X, 6HFM(S)=, E10.3, 2X, 6HFP(S)=, E10.3/5X, 23HDES
     2IBING FUNCTION DF=, E9.2, 2X, 9H20LOG DF=, E9.2, 2X, 8HPHASEDF=, E9.2, 8
     3AD. OR , E9.2, 6HDEGREE)
      PRINT 3, AGTS, AGTSL, PGTS, DGTS, GAS, GASL
3     FORMAT(5X, 21HOPEN LOOP GAIN GT(S)=, E9.2, 2X, 12H20LOG GT(S)=, E9.2
     1, 6HPHASE=, E9.2, 8HRAD. OR , E9.2, 6HDEGREE/5X, 26HAUDIO SUSEPTIBILITY
     2GA(S)=, E9.2, 2X, 13H20 LOG GA(S)=, E9.2)
      PRINT 4, DUFRE, DUFIM, GTRE, GTIM
4     FORMAT(5X, 6HDUFRE=, E10.4, 5X, 6HDUFIM=, E10.4, 5X, 5HGTRE=, E10.4, 5X,
     1TIM=, E10.4)
10    CONTINUE
      STOP
      END
```

```
 1.          C  INPUT FILTER DESIGN FOR SWITCHING REGULATORS
 2.          C  EVALUATION OF ATTENUATION
 3.          C  PROGRAMMED BY P.K. GUPTA
 4.             READ1.R1.R2.R3.AL1.AL2.C1.C2
 5.  0036    1  FORMAT(7E10.1)
 6.  0036       DO 10 I=1,5001,50
 7.  0034       AI=I-1
 8.  0042    6  W=2.0*22.0/7.0*AI
 9.  0040       VOUT=1.0
10.  0050       COUTIM=W*C2
11.  0056        VXRE=1.0-W*W*AL2*C2
12.  0066       VXIM=W*C2*R2
13.  0065       VX=SQRT(VXRE**2+VXIM**2)
14.  0086       CXRE=(W*W*C1*C1 *R3*VXRE-W*C1*VXIM)/(1.0+(W*C1*R3)**2
15.  0086       CXIM=(W*C1*VXRE+(W*C1)**2*R3*VXIM)/(1.0+(W*C1*R3)**2)
16.  00DA       CIRE =CXRE
17.  00DF       CIIM=CXIM+COUTIM
18.  00E4       CI=SQRT (CIRE**2*CIIM**2)
19.  00F0       VIRE=R1*CIRE-W*AL1*CIIM*VXRE
20.  010F       VIIM=W*AL1*CIRE+R1*CIIM+VXRE
21.  0120       VI=SQRT(VIRE**2+VIIM**2)
22.  0138       ATTEN=1.0/VI
23.  013F       PRINT 20.AI,COUTIM,VX,CI,VI,ATTEN
2424.0168 20    FORMAT(5X,5HFREQ=I6,2HHZ/10X,15HOUTPUT CURRENT=.F8.3.
                                                        .3HVX=,F7
25.                1 .3/10x,14HINPUT CURRENT=F6,3,10X,13HINPUT VOLAGE=.
                                                        F7.3/10X.12HATT
26.                2ENUATION=F8.5)
27.  016C          F1=1.0/(2.0*22.0/7.0*SQRT(ALI*C1))
28.  0184       A=(C2/C1)*(AI/F1)**2
29.  0198       B=AL2*C2/(AL1*C1)*(AI/F1)**3*SQRT (AL1/C1)/R3
30.  01C0       APPATT=1.0/SQRT (A**2+B**2)
31.  01DF       PRINT 30,APPATT
32.  01EF    30 FORMAT (10X.24HAPPROIMATE ATTENTION=E8.5)
33.  01FE    10 CONTINUE
34.  01E6       STOP
35.  01F8       END
```