A SOLID STATE INVERTER FED INDUCTION MOTOR DRIVE

A DISSERTATION
Submitted in partial fulfilment of the requirements for the award of the degree
of
MASTER OF ENGINEERING
in
ELECTRICAL ENGINEERING
(Power Apparatus & Electric Drives)

by

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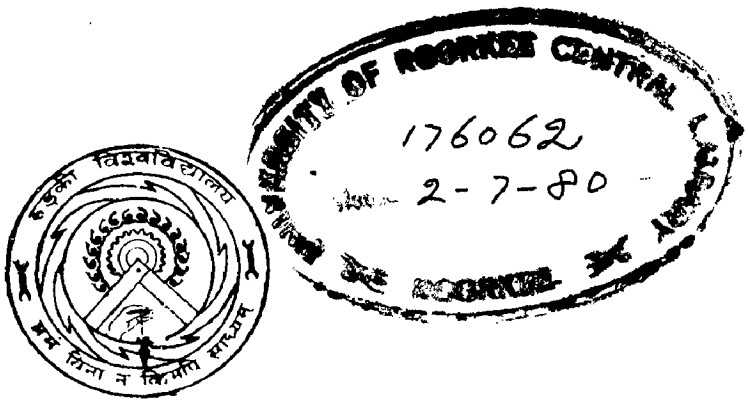

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C E R T I F I C A T E

Certified that the dissertation entitled"A Solid State Inverter Fed Induction Motor Drive" which is being submitted by Sri Yash Pal Singh in partial fulfilment for the award of the Degree of Master of Engineering in Power Apparatus and Electric Drives of the University of Roorkee is a record of students own work carried out by him under my supervision and guidance. The matter embodied in this dissertation has not been submitted for the award of any other Degree or Diploma.

This is further to certify that he has worked for a period of 11 months from Feb. 1979 to Dec. 1979 for preparing dissertation for Master of Engineering Degree at this university.

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A C K N O W L E D G E M E N T S

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(YASH PAL SINGH)

C O N T E N T S

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CHAPTER I

INTRODUCTION

1.1 Importance of Statically Controlled Induction Motor Drives

The field of static control and conversion of electric power has been revolutionized with the development of solid state semiconductor devices (such as silicon controlled rectifiers, power diodes and power transistors etc.). Also the fast developments in Power Electronics have opened up new vistas in the field of static control of electric drives that are gaining more and more popularly. An electric drive basically consists of an electric machine associated with a control equipment (that may include a frequency converter, rectifier etc.) to convert electrical energy into a mechanical energy and thereby to provide a versatile control of speed, torque etc. of the electric machine.

Normally, among the statically controlled electric drives, a d.c. motor operated as a variable speed drive by a static power controller is a popular choice. But the main draw backs of a d.c. motor are :-

(i) Increase in cost and decrease in power/weight ratio because elaborate mechanical commutator.

(ii) Accentuated sparking at high currents and speeds.

(iii) A limited armature voltage rating inherent in d.c. machines.

(iv) A limited armature current, because of commutation problem.

Because of the above drawbacks of a d.c. motor, a suggested alternative is to use a cage rotor induction motor, or a synchronous motor or a reluctance motor ; operating at variable frequency and supplied from a static frequency converter. The use of a cage rotor-induction motor has the advantage that :-

(i) The cost of induction motor is only about one sixth for the d.c. motor of the same speed and power rating.

(ii) The lower/weight ratio of the squirrel cage I.M. is twice that of a d.c. machine.

In general, a solid state inverter fed induction motor drive, is an efficient, and robust, drive system, having an application in fields where an extremely precise speed control or speed matching is required. Thus, the static frequency converters provide a wide range variable speed drive with control accuracies upto .001 % , since the solid state frequency converters/inverters provide output frequencies that are precise and stable. The initial capital cost of such drives is very high and discourages the application of such drives for general purpose application. However the fast decline in the cost of solid state devices and electronic components, and an added advantages obtainable in such drives these are bound to replace d.c. drives in time to come.

1.2 Variable Frequency Inverter Fed Induction Motor Drives

A cage-rotor induction motor fed with a variable frequency supply provides a versatile and wide range speed

controlled drive. The variable frequency supply that alters the synchronous speed of the induction motor, can be obtained through a static frequency converter. For optimum motor performance and effective utilization of core material, the air gap flux of the induction motor should be maintained constant. The air gap flux can be maintained approximately constant by keeping a constant volts/Hz ratio i.e. varying the supply voltage proportionately as the frequency is varied. However with constant v/f operation, the performance of the motor deteriorates at low frequencies because at low frequencies the influence of stator resistance is increased and consequently the air gap flux reduces to some extent. Hence, in order to improve the low frequency characteristic, the terminal voltage should be increased more than the proportionate value. The required boost actually depends upon the design and size of the machine. A constant volts/Hz operation gives the following characteristic features to a variable frequency drive:-

(i) The starting current,power factor and also the starting torque are improved.

(ii) The pull-out torque remains approximately constant.

(iii) Sufficiently high torque can be achieved through-out the entire range of speed control.

There are two mode of operation of a variable frequency induction motor drives, such as I-Constant Flux operation ; (II-Constant Current operation.

1.2.1 Constant Flux Operation:- In order to maintain a high torque throughout the entire speed range, it is essential to maintain the flux constant. This can be achieved if the air-gap e.m.f. E_1, instead of terminal voltage is varied linearly with the frequency and a proper boost in E_1 is given at low frequencies in order to compensate for the increased effect of stator winding resistance. Further it can be shown that [1] the electromagnetic torque is proportional to square of E_1/f_1 or air gap flux, at a given rotor frequency f_2. Consequently if E_1/f_1 or air gap flux is maintained constant, the torque is solely determined by the absolute rotor frequency " f_2 and is independent of supply frequency, f_1 ".

Thus a control scheme in which the rotor-slip frequency is directly controlled while maintaining the constant air gap flux or E_1/f_1, the drive can exhibit a precise control and adjustment of torque at any speed.

1.2.2 Constant Current Operation :- Practically, high torque under constant flux operation can be obtained only at the cost of increased stator current. Again it has been shown[1], that the stator current I_1, is independent of the supply frequency, f_1, when the air-gap flux is constant, but depends upon the rotor slip frequency, f_2. Thus the air gap flux of the motor can be indirectly determined by the stator current and rotor slip frequency f_2. Further, the torque can be expressed in terms of stator current and rotor frequency[1]. Therefore in

second mode of operation the stator current I_1, as well as rotor frequency f_2 are controlled in order to maintain the air gap flux constant and consequently the high torque through-out the entire range of speed control. The basic advantage of constant-current operation is that there is no necessity of large overcurrent capacity of the inverter since there are no current surges and thus the inverter design is economical.

Normally variable frequency drives are closed loop drives and the simplest scheme is the controlled, Slip drive, in which the slip frequency is contineously controlled so as to ensure that operation is always at small slip. This owes a high developed torque at high power factor with low losses. The overall characteristics of the drive can be adjusted so as to suit the particular application and two basic types of characteristics i.e. as 'constant torque' and 'constant horse power' characteristics can be achieved in the following way:-

1.2.3 Constant Torque Operation :- (Below and upto one per unit sped). It can be obtained by increasing the terminal voltage linearly with the supply frequency and to provide a suitable boost in terminal voltage at low frequencies in order to maintain a constant air gap flux. This gives a high torque through-out the speed range. However the speed range can be increased above the 1 p.u. speed by keeping the terminal voltage constant and increasing the fundamental frequency above the normal rated supply frequency. But in this case the torque goes on reducing as speed is increased above one per unit because of decrease in air gap flux.

1.2.4 Constant Horse Power Operation :- (Above and upto one per unit speed)

If the frequency f_2 is increased linearly with f_1 for a constant stator voltage then it can be shown that torque is inversly proportional to the supply frequency. Since $T = K''\phi^2 f_2$ or $\simeq K''(V_1/f_1)^2 \times f_2$.

This means that the torque varies inversly with the speed i.e. a constant horse power characteristic is obtained.

1.2.5 Constant Horse Power Operation :- (At low speeds in sub-synchronous region).

For a fixed value of 'f2', it can be obtained by varying $(V_1)^2$ proportional to f_1, In this case torque varies inversly proportional to f_1 and a constant hourse power output is obtained, since $T = K''\phi^2 f_2 \alpha \phi^2 \alpha(V_1^2/f_1^2)$.

Constant horse power operation over a wide speed range is required for Traction purpose and for that methods describe above under section 1.2.4 and 1.2.5 can be conveniently used.

1.3 Types of Inverters Used for Variable Frequency Induction Motor Drives

The variable frequency operation of an induction motor is obtained by the use of Frequency Converter. A frequency converter is a machine or equipment that can generate or convert the input supply to a supply of variable frequency and amplitude. The rotating type of frequency converters have been used in past but now a days are out-dated and are replaced by the solid state frequency converters. State frequency conversion hasethe following advantages:-

(i) Extremely high accuracy and stability are obtained.

(ii) High efficiency and absence of moving parts, reduces the operating cost.

(iii) Require smaller space, lesser maintenance, no machine alignment and have lower installation cost.

(iv) Fast response and control can be achieved easily.

The static frequency converters are divided into two categories- [A] D.C. Link Convertors & [B] Cycloconvertors. A d.c. link convertor is a two stage conversion device in which power from the a.c. network is first rectified to d.c. and then inverted to obtain a.c. voltage at variable frequency. This type of inverter can operate over a large frequency range and is suitable for wide-range speed control drives. However this type of inverter employing thyristors, require additional commutation circuits and therefore complicated control circuitry. Also for regeneration capability it requires additional circuits and hence the cost and complexity is increased.

A cyclo-convertor is a device to convert directly the supply frequency to a lower output frequency and does not require intermediate rectification. The output frequency range and is limited to about one third of the supply frequency and therefore the drives employing cyclo-convertors are suitable only for operation at low-frequency or speed range. However the basic advantage of a cyclo-convertor is its inherent capability of regenerative operation and a close approximation

of the output voltage to a sine wave, particularly at low frequencies, since the output wave is fabricated from the segments of the input supply waveforms.

In general for wide range speed control and where regeneration braking is not essential a d.c. link converter fed induction motor is the best choice. In actual practice for drive applications, a d.c. link converter is required to provide an output of variable frequency as well as variable voltage. Based upon the above requirements, the rectifier-inverters (frequency converters) are divided into the following two groups:-

(A) A.V.I. (Adjustable Voltage Input) inverter.

(B) P.W.M. (Pulse Width Modulated) inverter.

(C) Current Source Inverter.

1.3.1 Adjustable Voltage Input Inverter :- The A.V.I. inverter[2], basically consists of three major circuits: a phase controlled bridge or a chopper controller for voltage control, an inverter for frequency control and a fixed d.c. bus to provide constant commutating capability.

In phase controlled bridge rectifiers, a 'phase control' technique (in which delayed firing of thyristors normally connected in three phase bridge configuration) is employed in order to control the d.c. voltage input to the static-inverter. Basically, in phase controlled rectifiers, the displacement power factor varies linearly with the output voltage and at low output voltage, the power factor is low which is a disadvantage.

Also, some "beating" motor currents are caused by the difference of inverter output and rectified line frequency and in order to minimise them a smoothing L.C. filter is required. Further because of discontinuous conduction at low voltages, the filter capacitor required would be larger than that for a P.W.M. inverter where continuous conduction takes place. Again because of large filter time constant response is slow.

A.V.I. inverter with chopper controlled input has the advantage of good power factor at the a.c. input and possible faster voltage response due to smaller time constant on account of L.C. filter used on the output of a high-frequency chopper.

1.3.2 Pulse Width Modulated Inverter :- The P.W.M. inverter[2], can be considered as a refined version of the chopper-input A.V.I., since in this case voltage and frequency control are accomplished with only one power controller and some special control logic circuitry. The P.W.M. inverter basically generates an output voltage of constant amplitude and variable width blocks; which when supplied to an inductive load (or motor), produces a smoothed version of the voltage waveform i.e. of fundamental frequency. Pulse width modulated blocks are generated by the comparison of a reference sinusoidal signal (of fundamental frequency) with a carrier wave (that may be a triangular, rectangular, square or trapizoidal). Normally the ratio of the carrier wave to reference sinewave is kept high in order to reduce the lower order harmonics.

The pulse width modulated inverters have the following advantages:-

1. When the pulse width is sinusoidally modulated with high frequency triangular wave, the output voltage and current have small harmonic contents. This reduces the undesirable torque pulsation which are usually associated with low frequency static a.c. drives
2. A high pulsing frequency reduces the lower order harmonics content and eases the filter requirements.
3. Mains interference and distortion are also minimized because of an uncontrolled rectifier and high pulse repetition frequency in the inverter.
4. The P.W.M. system requires a minimum of auxiliary equipment, since the only apparatus required, in addition to inverter, is an inexpensive bridge rectifier.
5. Good power factor to a.c. line and excellent dynamic response.
6. Full load speed range of 20:1 is obtainable.

1.3.3 Current Source Inverter:- Most of the solid state inverters used in variable frequency a.c. drives are of variable voltage and frequency type. Recently, current source inverters[3] have been developed in which the magnitude of current at any point is always controlled by the regulated current source. The current source inverters are becoming more popular and ideally suited for a.c. drives requiring a constant torque output. In a current source inverter fed induction motor drive,

the average d.c. voltage at the input terminals of the inverter varies with the power demand of the motor. For example, if the motor is unloaded, the d.c. voltage will be near zero, while it will be at some maximum positive value when supplying rated H.P. If the motor load is overhauling, the d.c. voltage reverses in polarity and the power will be returned to a.c. through the controlled rectifiers i.e. regeneration takes place. However the circuit and induction motor parameters effect the performance of current source inverter[3]. The current source inverters have the following specific advantages over the voltage fed inverters:-

1. Simple configuration and non-inverter grade thyristors can be used.
2. Commulation capability is load current dependent.
3. Ability to ride through commulation failure and also to recover from momentary short circuit failure. Hence thyristors require minimal protection and full current handling capacity can be utilized.
4. Regeneration capability, makes these ideally suited for drives requiring frequent acceleration and deceleration.
5. Low cost.

1.4 Special Features of a Three Phase Solid State P.W.M. Inverter Using Power Transistors

Normally, P.W.M. inverters employ thyristors, having fast turn off time of the order of 20 micro-sec. but the commutation difficulties and commutation circuit time constant limit the switching frequency. In a sinusoidal P.W.M. with triangular wave a Modulation Ratio (Ratio of triangular carrier

frequency to the frequency of reference sine wave) upto 20 can be achieved and may give an inverter motor drive with substantially a good performance for normal application of speed control. But for some specialized applications, such synthetic fiber manufacturing, paper manufacturing and other continuous processing plants, a very precise, wide range, stable and coordinated speed control of multimotor drives system is the specific requirement and K.V.A. ratings are in the range of upto 20 K.V.A. For such applications, a solid state P.W.M. inverter (employing Power Transistors as a switching element) Fed Squirrel Cage Induction Motor Drive is the best choice because of the following reasons:-

(a) A Power Transistor employed as a solid state switching element requires only one signal to switch it ON and it turns OFF automatically, when the switching ON signal is absent. Hence the P.W.M. Inverter employing Power Transistors, do not require any commutation circuitry and the problems associated with commutation in the Thyristors are over. Further the control circuitry is much simplified.

(b) Power Transistor being a fast switching device, having a turn ON and turn OFF times of the order of 1 micro-second (approx) ~~or less~~, the inverter can be operated at high switching frequencies and thus high modulation ratios, (even upto 100) can be achieved. Therefore an output wave of low harmonic content can be generated, with all

the harmonics that effect the motor performance, being reduced to minimum.

The ready availability and fast reduction in the cost of high rating switching power transistors (e.g. 800V, 30 Amp) have resulted in a possible alternative to use power transistors in place of thyristors. With this view a Three Phase Solid State Inverter is designed and fabricated ; the practical feasibility of this alternative have been tried and the results are reported in this thesis. The P.W.M. inverter designed and fabricated have the following specifications:-

(a) Output K.V.A. Rating :- 0.5 KVA*(50V, 10 Amp, 3 Phase).

(b) Operating Frequency Range :- 5 Hz to 100 Hz.

(c) Faculty to control the voltage and frequency of the output with seperate control signals, in order to provide constant V/F operation.

(d) Modulation Ratio :- Two modes of operation are possible:-

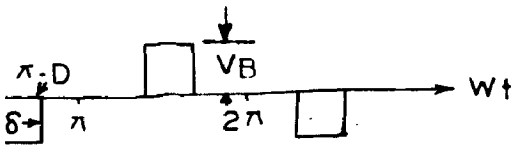
(i) Fixed Modulation Ratio (M.R. = 6, 12 or 24).

(ii) Variable Modulation Ratio (M.R. Varying 20 to 100 with the variation of fundamental frequency from 50 to 5 Hz)

(* The rating of the developed inverter is limited to 0.5 KVA because the only power transistors available were 2N3055 (60V , 15 Amp). The inverter rating can be extended upto 10 KVA by using the power transistors of rating 800V, 30A ; with the same control and power unit).

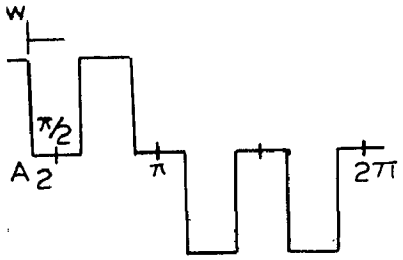
1.5 Brief Description of the Work Presented in This Thesis

In chapter 2, the review of various pulse width modulation techniques is presented and some P.W.M. inverter fed induction motor drives are discussed. The third chapter describes the control scheme for the Three Phase P.W.M. Inverter, designed and fabricated as a part of this dissertation. Design considerations that are of vital importance in design are fully discussed and design of various blocks is given. The design of Power Unit is also presented in the same fashion in fourth chapter. In the last chapter (Chapter V) the practical observations of P.W.M. inverter and conclusions are presented.



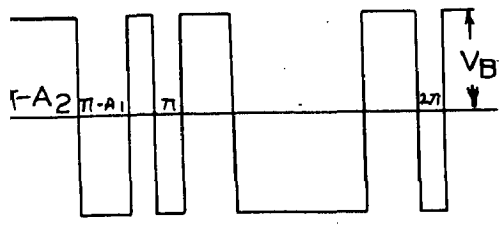
PULSE MODULATION

Fig 2.1



PULSE UNIDIRECTION WAVE

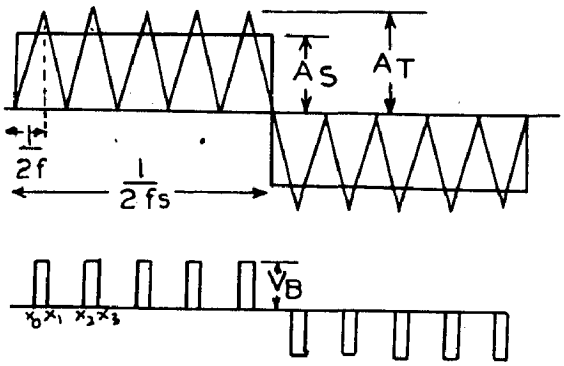
Fig-2.2



PULSE BIDIRECTIONAL WAVE

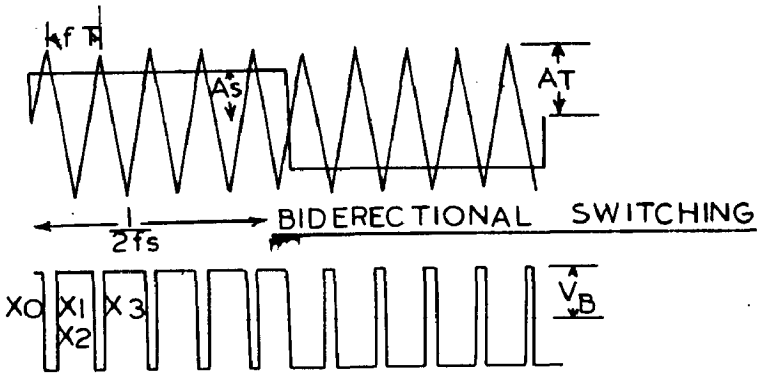
MODULATION

Fig 2.3a



UNIDIRECTIONAL P.W.M WITH SQUARE WAVE

Fig. 2.4



P.W.M WITH SQUARE WAVE

Fig. 2.5

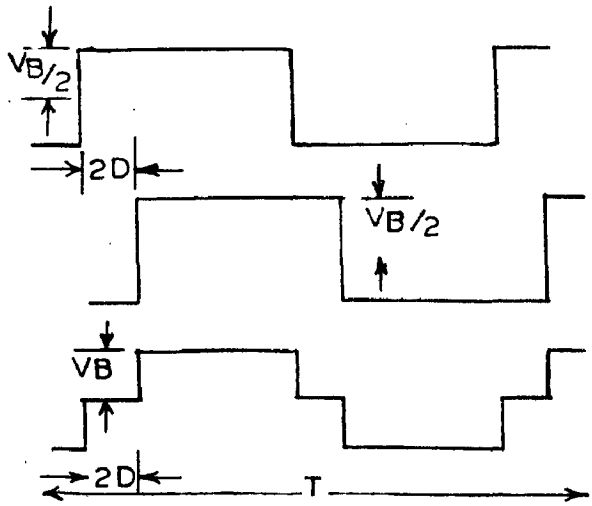


Fig. 2.3b

CHAPTER - II

REVIEW OF PULSE WIDTH MODULATION TECHNIQUES AND SOLID STATE INVERTER FED INDUCTION MOTOR DRIVES

2.0 Review of Pulse Width Modulation Techniques

It is evident from the discussion of section 1.3.2. that a P.W.M. inverter can inherently perform a dual function of varying the frequency as well as the magnitude of the output voltage. The voltage control is basically achieved by Pulse Width Modulation which may be defined as the control of average level of a quantity (Voltage, current, flux etc.) by applying or driving that quantity in discrete intervals or pulses. The most commonly used techniques of pulse width modulation are :-

1. Single Pulse Width Modulation or Quasi Square Modulation.
2. Multiple Pulse Width Modulation.
3. Sinusoidal Pulse Width Modulation.
4. P.W.M. in Six-Step Wave.

2.1 Single Pulse Modulation or Quasi Square Modulation

This type of modulation is characterized as one whose polarity reverses twice per cycle. This is the most simple type of modulation technique employed to control the amplitude of fundamental component of the wave by varying the ~~work~~ mark to space ratio as shown in Fig.2.1. The analysis of such a wave form gives the r.m.s. value of the n^{th} coefficient as

$$\frac{\% \text{ r.m.s } (n)}{V_B} = \left[\frac{2\sqrt{2}}{\pi} \cos n D\right] \times 100 \qquad (2.1)$$

and the total r.m.s voltage of the waveform, including all the harmonics, is given by

$$\frac{\% \text{ r.m.s (T)}}{V_B} = \left[1 - \frac{2D}{\pi}\right]^{1/2} \times 100 \qquad (2.2)$$

Equations (2.1) and (2.2) are derived in and numerical results are given in Ref.[4], table 9.1. The greatest disadvantage of the quasi-square or single pulse modulation is that the normal voltage control range is limited only 30 to 90 % because allow voltage various harmonics have amplitude almost equal to that of fundamental.

2.2 Multiple Pulse Modulation

In this type of modulation polarity reverses more than twice per cycle and harmonic content at lower output voltages can be significantly reduced by using several pulses in each half cycle. This type of modulation can be further sub-devided into following groups:-

I-(a) Two Pulse Uni-directional Wave Modulation.

I-(b) Two Pulse Bi-directional Wave Modulation.

II-(a) Uni-directional P.W.M. with Swuare Wave.

II-(b) Bi-directional P.W.M. with Square Wave.

2.2.1 Two Pulse Uni-directional Wave Modulation:- In two pulse uni-directional wave modulation, two pulses of either polarity + or - are generated in each half of the cycle as shown in Fig.2.2. The word unidirectional means that all the pulses in a given half cycle, have either a positive magnitude ~~positive~~ or a negative magnitude with respect to ground or zero level and the wave may assume zero level for some time. As shown in

Fig.2.2, if $B = \frac{A_1 + A_2}{2}$ and $w = \frac{A_2 - A_1}{2}$, then the n^{th} fourier coefficient is given by

$$b_n = \frac{8V_B}{\pi n} \text{ Sin } nB . \text{Sin } nW \qquad (2.3)$$

Here by proper selection of 'B' as shown in Fig.2.2, the Pth harmonic can be eliminated, if the following condition is satisfied i.e. Sin PB = 0 or $B = \pi/P$. Also by maintaining this value of 'B' and varying the width 'w', the effective voltage can be varied while the Pth harmonic still remains absent. From equation (2.3) the r.m.s values of the n^{th} harmonics and the total harmonic content is given by % r.m.s(n)

$$\frac{\% \text{ r.m.s (n)}}{V_B} = \left[\frac{4\sqrt{2}}{\pi} \text{ Sin } \frac{n\pi}{p} \cdot \text{Sin } n\, w\right] \times 100 \qquad (2.4)$$

and

$$\frac{\% \text{ r.m.s(T)}}{V_B} = 100 \left[\frac{2}{\pi}(A_2 - A_1)\right]^{1/2} = 200 \sqrt{w/\pi} \qquad (2.5)$$

Since the harmonics of the order P is absent from the output, this technique is also called " Selected harmonic elimination" technique. It can be observed in this case that even though lower harmonics are eliminated, the total harmonic content is large and the most serious disadvantage is that the fundamental (max), obtainable is 75.1 % , 62.2 % or 33.3 % , of the d.c. according to whether 3rd, 5th or 7th harmonic is eliminated.

2.2.2 Two Pulse Bi-directional Wave Modulation:- In two pulse bidirectional modulation the output voltage have dual polarity pulses, having a symmetry over a cycle, as shown in Fig.2.3(a). Here, again B and W can be selected to eliminate a particular harmonic

and to vary the fundamental voltage and are given by $B = (A_1 + A_2)/2$ and $W = (A_1 - A_2)/2$. The voltage components in this case are given by

$$\frac{\% \text{ r.m.s}(n)}{V_B} = \frac{2\sqrt{2}}{n\pi} [1-4 \sin nB \sin nw] \qquad (2.6)$$

Now it is possible to combine, two phase shifted bi-directional waveforms of Fig.3.2(a). This combination results in a quasi-square wave. For example, if two phase shifted bi-directional square waves are combined together, then they produce a quai-square waveform as shown in Fig.3.2(b).

The combination of two phase-shifted, two pulse bi-directional waveform would give a modified r.m.s. value of n^{th} harmonic as :-

$$\frac{\% \text{ r.m.s}(n)}{V_B} = \frac{2\sqrt{2}}{\pi} [1-4 \text{ Sin } nB \text{ Sin } nW] \text{ Cos } nD \qquad (2.7)$$

and total harmonic content as

$$\frac{\% \text{ r.m.s}(T)}{V_B} = 100\sqrt{1-2D/\pi} \qquad (2.8)$$

where 2D is the phase shift between the two waveforms.

Now, there are three control variables w,B, and D, out of that w and B can be used to eliminate any two harmonics, while D controls the magnitude of fundamental voltage. Therefore a selected harmonic elimination for any two harmonics (say P_1 and P_2) can be achieved, if the following condition is satisfied i.e. $1-4 \sin (P_1B).\sin (P_1W) = 0$ and $1-4 \sin (P_2B)$.

$$\sin(P_2W) = 0 \qquad (2.9)$$

From an analysis of these results it can be observed[4] that:-

(a) Fundamental output (max) voltage is more than that obtainable from unidirectional wave particularly when higher harmonics are eliminated.

(b) Total harmonic content is less than that obtained with uni-directional wave.

(c) The amplitude of harmonic increases with the harmonic number e.g. 9th is the largest when 3rd and 5th are eliminated, where as when 3rd and 7th are eliminated 11th predominates, while others also exist but with lesser amplitude.

(d) Only two chosen harmonics are eliminated while in the case of uni-directional wave, an odd multiple of the harmonic being eliminated are also absent from the output.

(e) Normally harmonic elimination causes the remaining harmonics to be of objectionably larger amplitudes.

2.2.3 Uni-directional P.W.M. With Square Wave:- In this type of modulation several equally spaced unidirectional pulses every half cycle, are generated, by feeding a high frequency carrier triangular wave and a low frequency reference square wave into a comparator. The resulting output waveform is shown in Fig.2.4, and swings between V_B and zero and the width of the pulses are determined by the ratio A_{sq}/A_T and the number of pulses per cycle, by the ratio of f_T/f_q. The harmonic voltages are given by:-

$$\frac{\% \text{ r.m.s}(n)}{V_B} = \sum_{n=0,2,4} \frac{2\sqrt{2}}{\pi} [\text{Cos } nx(M) - \text{Cos } nx(M+1)] \qquad (2.10)$$

and

$$\frac{\% \text{ r.m.s}(T)}{V_B} = 100\left[\frac{f_T}{2\pi f_q}\{x(0) - x(1)\}\right]^{1/2} \qquad (2.11)$$

where M = Modulation Ratio = A_{sq}/A_T

The analysis of equations (2.10) and (2.11) for various values of f_T/f_S indicate that :-

(a) Lower harmonics are considerably reduced, although total harmonic content increases with pulse number.

(b) The third harmonic at high pulse number varies almost linearly with the fundamental.

(c) The maximum fundamental r.m.s voltages is 90 % of d.c.

(d) All even harmonics are absent from the output.

2.2.4 Bi-directional P.W.M. with Square Wave :- Several equispaced bidirectional pulses can be generated as shown in Fig.2.5 by mixing a triangular and square wave through a comparator.This output waveform with this type of modulation contains odd and even harmonics. The n^{th} harmonic component is given by[4]

$$\frac{\% \text{ r.m.s}(n)}{V_B} = \frac{\sqrt{2}}{n\pi} \times 100\{1-\cos n x(0)+\Sigma[\cos n x(2M+1)-\cos nx(2M+2)] - \Sigma[\cos n x(2M)-\cos n x(2M+1)]\} \qquad (2.12)$$

where M is the Modulation Ratio = A_{sq}/A_T and x_0, x_1, x_2, x_3 are the points of intersection of triangular and squarewave.

This type of modulation gives the following characteristics:-

(a) Even harmonics except those of the order (f_T/f_S) and $3(f_T/f_S)$ are absent e.g. for $f_T/f_S = 4$ only 4th and 12th even harmonics are present.

(b) The harmonic with number equal to f_T/f_S has the largest amplitude.

(c) The content of lower order harmonics is less than that obtained with unidirectional switching.

(d) The odd harmonic content generally increases as the operating frequency is increased, while reverse is true in the case of unidirectional switching.

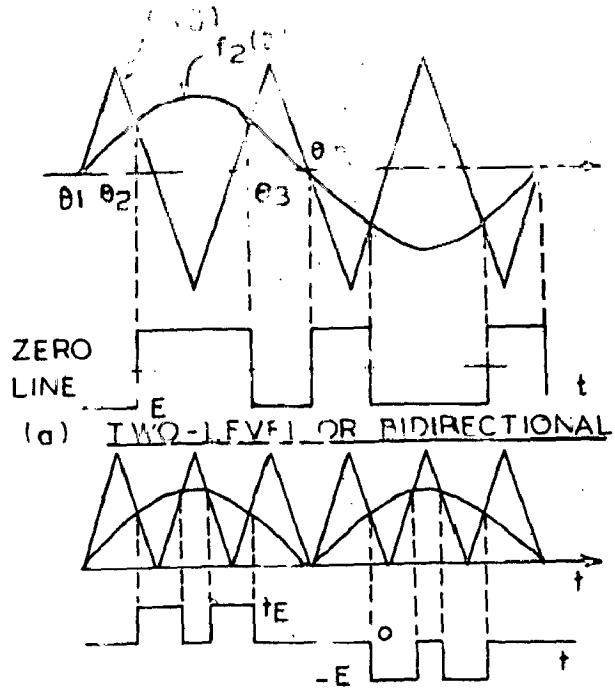
2.3 Sinusoidal Pulse Width Modulation

Sinusoidal pulse width modulation is obtained by modulating the reference sine wave with triangular wave. This type of modulation is also termed as subharmonic method of control, and offers the advantage of reducing the harmonics to a tolerable limit in the voltage and current and consequently in torque (in P.W.M. inverter fed drives). In speed control of induction motors using P.W.M. inverters (employing sinusoidal pulse width modulation), there is a production of sinusoidal mean voltage from a square alternating voltage with different positive and negative voltage-time areas. Also the flux varies according to the mean voltage of this alternating square voltage.

Basically, a voltage with sinusoidal mean value contains two types of harmonics e.g.

(i) Three-phase harmonics that forms a rotating field.

(ii) The harmonics that are in-phase and drive a current in the neutral. Practically, the in phase harmonics can be easily eliminated by omitting the neutral.

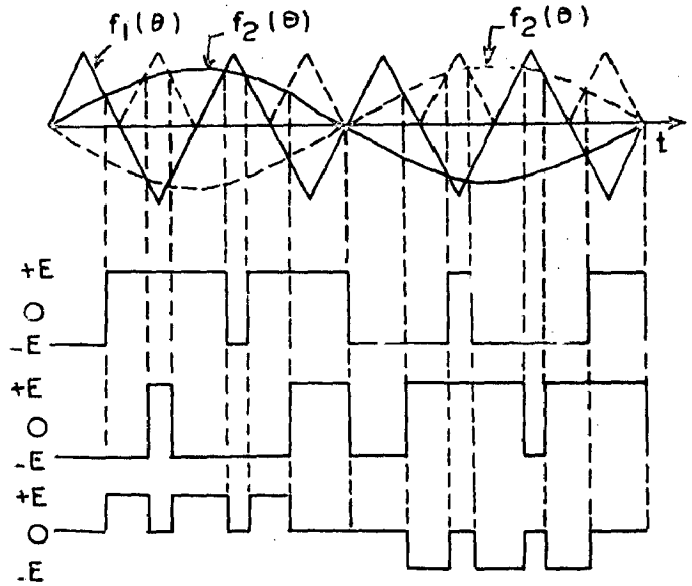


(a) TWO-LEVEL OR BIDIRECTIONAL

(b) THREE LEVEL OR UNIDIRECTIONAL

BASIC SINUSOIDAL P.W.M

Fig. 2.6



SYNTHESIS OF THREE-LEVEL P.W.M. WAVEFORM BY TWO DIFFERENT TWO LEVEL P.W.M. WAVES

Fig 2.7

There are two types of Sinusoidal Pulse Width Modulation[5] schemes: (1) Two Level or Bidirectional P.W.M. and (2) Three Level of unidirectional P.W.M.

2.3.1 Two Level or Bi-directional Sinusoidal P.W.M :- A two level or bidirection pulse modulation is shown in Fig.2.6, where $Q_1, Q_2, Q_3, \ldots\ldots \theta_m$ are the points of intersection of triangular carrier wave $f_1(\theta)$ and the modulating wave $f_2(\theta)$. where

$$f_1(\theta) = (\theta - j\,\frac{\pi}{N})\,\frac{(-1)^j}{\pi/2N} \qquad (2.13)$$

where $j = 0$; $0 \leq \theta \leq \pi/2N$

$j = 1$; $\pi/2N \leq \theta \leq 3\pi/2N$

$j = 2$; $3\pi/2N \leq \theta \leq 5\pi/2N$

$j = N$; $(2N - 1)\,\pi/N \leq \theta \leq (2N + 1)\pi/N$

and $f_2(\theta) = Y \sin \theta$; here N = Frequency Ratio = f_T/f_S and Y = Modulation Index (Ratio of amplitude of sine wave to that of triangular wave. From Fig.2.6(a) we get $m = (N + 1)$, $\theta_1 = 0$ and $\theta_m = \pi$ and also $|Y| \leq 1$.

The R.M.S. value of the n^{th} harmonic -Voltage of two level or Bi-directional P.W.M. waveform from unit D.C. link voltage is given by[5]

$$2^{V}n = \frac{\sqrt{2}}{n\pi}\,[-\cos n(\theta_1) + 2\{\cos n\,\theta_2 - \cos n\,\theta_3 + \ldots\ldots \ldots\ldots + (-1)^N.\cos n\,\theta_N\} - (-1)^m \cos n\,\theta_m] \qquad (2.14)$$

The solution of the equation (2.14) for four values of $N = f_T/f_S$ are given in Tables 9-20 to 9.23[4]. It is seen from these

tables that the harmonics with largest amplitude is that which occurs at the member given by f_T/f_S .

For example when operating at $f_T/f_S = 6$, the sixth harmonic; at $f_T/f_S = 10$, the 10th harmonics and at $f_T/f_S = 20$ the 20th harmonics, have the largest amplitude. For zero modulation index the output is a square wave at the frequency $N.f_S$ and the fundamental is zero. Also the amplitude of the $N.f_S$ harmonics has a value 90 % of the d.c. supply. As the Modulation Index increases the fundamental also increases in value and the $N.f_S$ harmonic reduces, where as adjacent even harmonics increase in value.

2.3.2 Three Level or Unidirectional Sinusoidal P.W.M.:-

A three level P.W.M. wave form as shown in Fig.2.6(b) can be synthesized by subtracting a two-level P.W.M. waveform with a Modulation Index of (+Y) from a similar two-level P.W.M. waveform with a Modulation Index of (-Y) as shown in Fig.2.7.

Let N'be the frequency ratio of three-level unidirectional P.W.M. waveform. The Fig.2.7 shows that $N' = 2N$, hence the r.m.s. value of the n^{th} harmonic voltage of a three level P.W.M. with a frequency ratio of N'is given by[5]

$$3V_n = \frac{1}{2} [2V_n(+Y,N) - 2V_n (-Y,N)]$$

where $2V_n$ (+Y,N) represents the r.m.s value of the n^{th} harmonic voltage of a two level P.W.M. waveform with a modulation (+Y) and frequency N.

This concept of synthesizing a three-level P.W.M. waveform simplifies computation of harmonic components, since the same algorithm can be used for computation, in both the cases. The Newton-Rahpson method can be used to compute the intersection points $\theta_1, \ldots\ldots \theta_m$ to an accuracy of 10^{-5} radians.

The maximum value of the modulation index (A_S/A_T) is limited to 0.98 rather than unity to prevent adjacent pulses from merging into each other.

In this type of modulation it can be noticed that:-

(i) The harmonic number having the largest amplitude occurs at $f_T/f_S \pm 1$: For example with $f_T/f_S = 10$; the harmonics are largest at the 9th and 11th. This is logical also since the 10th ha rmonic is the carrier wave itself and no attempt is made to eliminate it.

(ii) The higher the ratio of f_T/f_S the more effective this system becomes.

(iii) Because of symmetrical output wave all the even harmonics are eliminated.

However, there are following disadvantages in the schemes of sinusoidal P.W.M.:-

(a) The higher inverter frequency required to give effective lower-harmonic reduction leads to lower efficiencies.

(b) The maximum fundamental output is approx. 70 % of d.c. in case of two level or bidirectional and 78 % of d.c. for three-level or unidirectional P.W.M. for maximum

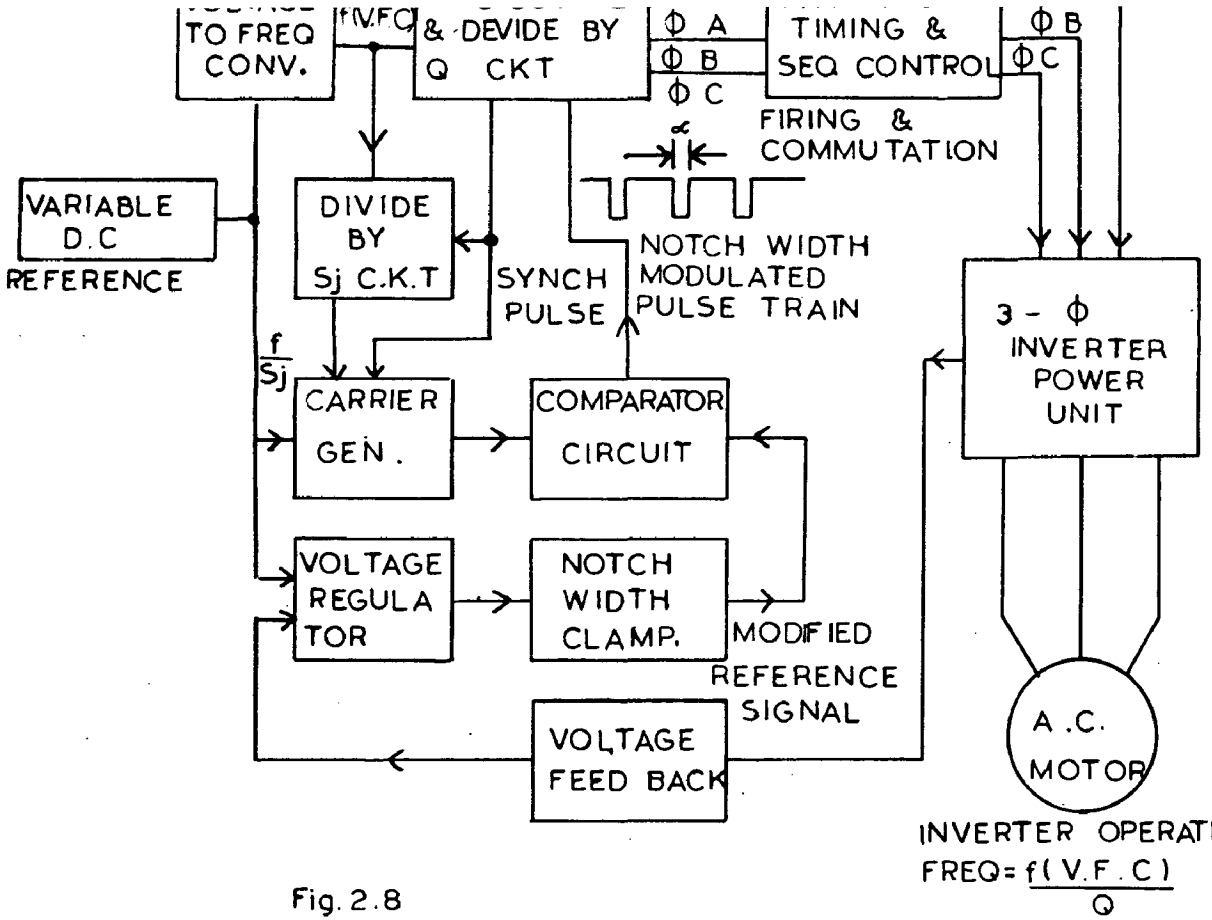


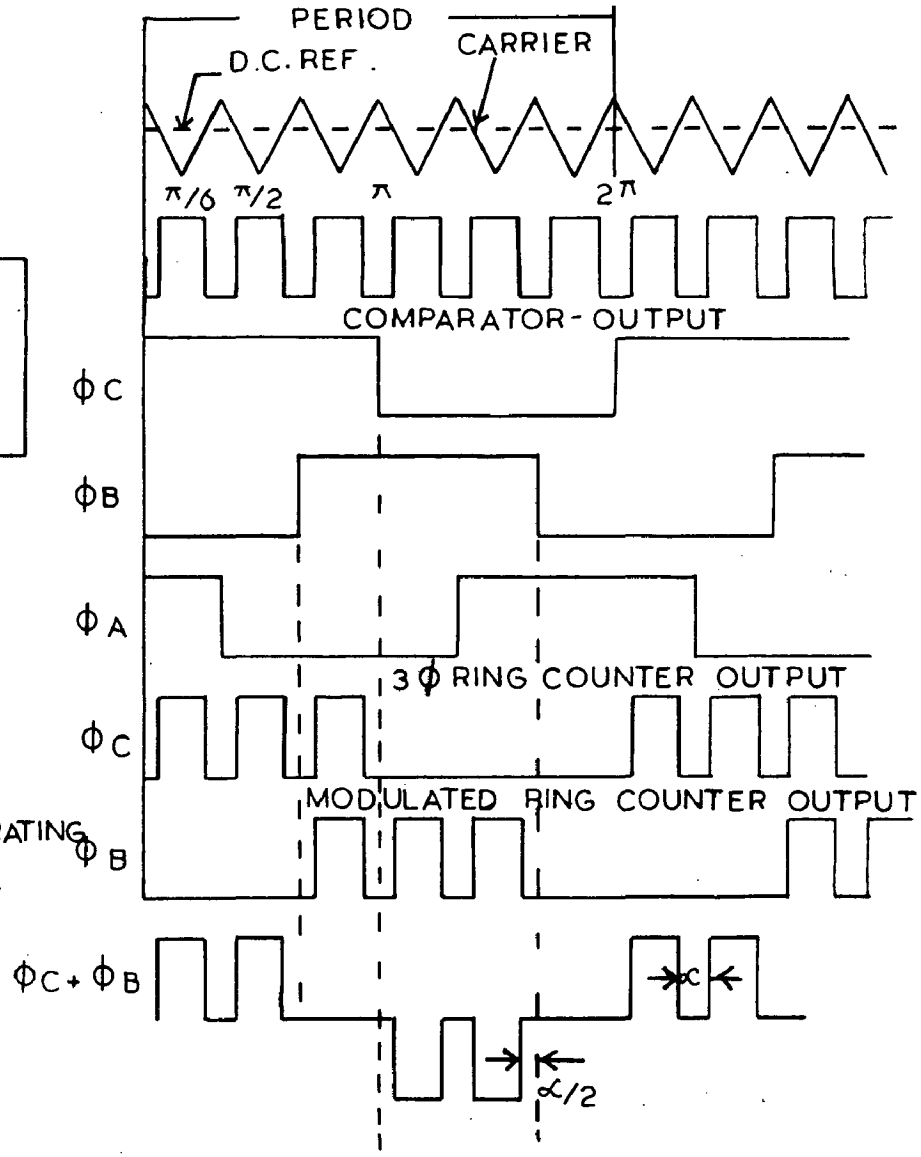
Fig. 2.8

NOTE :- Q IS A CONSTANT SELECTED SO THAT ALL REQUIRED VALUES OF R_c/f ARE INTEGER MULTIPLES OF THREE

R_c/f = CARRIER FREQUENCY / INVERTER OPERATING FREQ

$$\frac{f(V.F.C.)/Sj}{f(V.F.C)/Q} = \frac{Q}{Sj} = 3, 6, 9, 12, 15 \text{ etc.}$$

BLOCK-DIAGRAM OF SIX STEP MODULATED THREE PHASE INVERTER



LINE TO LINE LINE MODULATED OUTPUT

P.W.M. IN SIX STEP-WAVE

Fig. 2.9

value of Modulation Ratio (f_T/f_S = 20) and Modulation Index (A_g/A_T = 0.98). This max. value of fundamental output is well below that of a square wave modulation that is about 90 % of d.c.

(c) There is a characteristic increase in the total harmonics contents with higher operating frequencies. However this is not a serious drawback since the higher harmonics can be more easily filtered out than lower order harmonics.

Review of

2.4 Some Control Schemes For Solidstate ~~for~~ (P.W.M.) Inverter Fed Induction Motor Drives:

In this section some selected schemes for Induction Motor drives, employing P. W. M. Inverters are discussed. Their control schemes and special features are also reviewed and discussed in brief, so as to give a different control actions, type of protections and mode of operations possible with a P.W.M. Inverter-Motor Drive. These scheme are:-

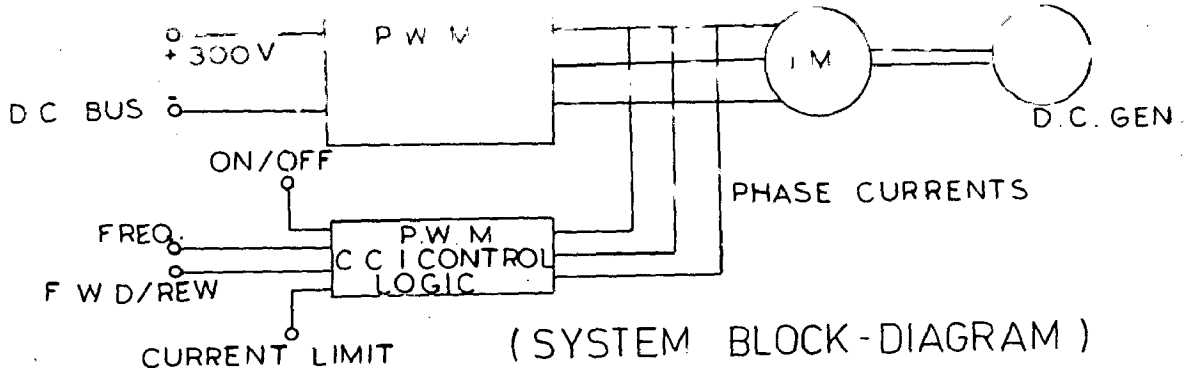
2.4.1 A Six-Step P.W.M. Inverter Fed I.M. Drive:- R.D.Adams and R.S. Fox[6], have discussed a basic pulse width modulated six-step inverter fed induction motor drive, where the following three modulation schemes are adopted:- (i) Fixed Ratio Modulation (ii) Variable Ratio Modulation (iii) Adaptive Ratio Modulation.

The basic 'Notch Width' or pulse width modulated. Six-step system is shown in Fig.2.8. In this system a variable d.c. reference signal is used for (1) a voltage to frequency converter (V.F.C), which in turn controls the inverter output frequency and also the carrier frequency.(2) Carrier frequency generator.(3) Output voltage level control through a voltage regulator.

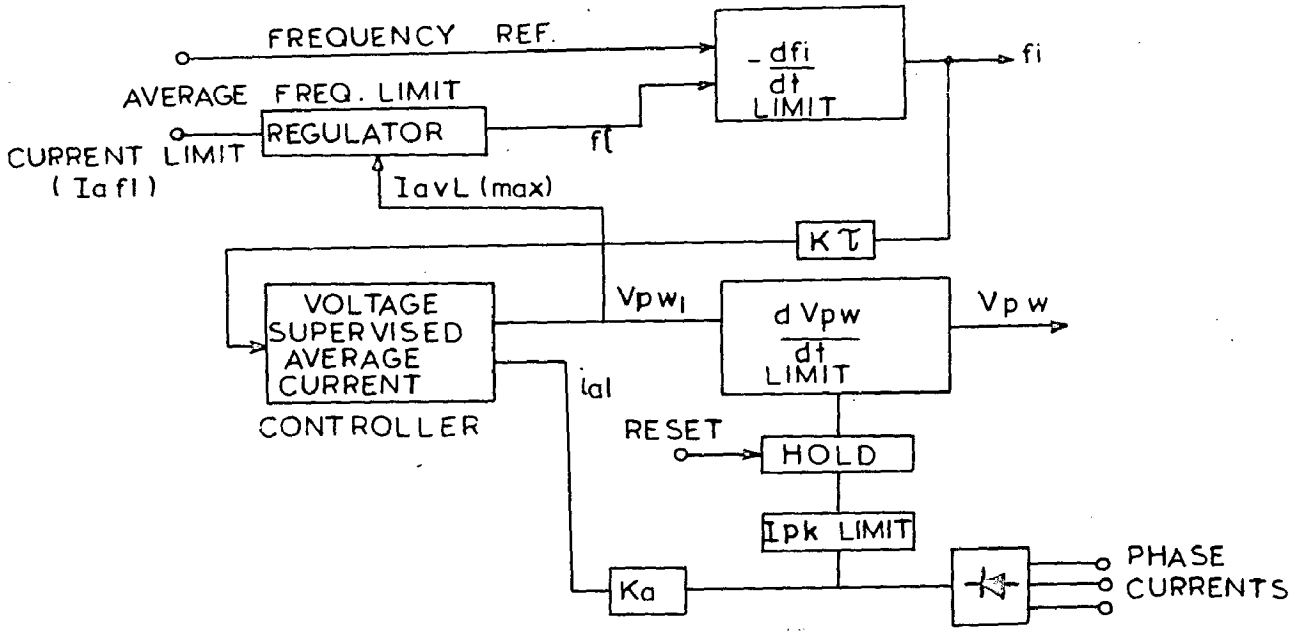
It can be observed in this scheme that the modified version of this reference voltage is compared with carrier wave through a comparator, the output of which is a "Notch width" modulated pulse Train. These pulses are used to modulate a 3-phase output of ring counter, through a modulation circuit and the three phase modulated ring counter output is obtained as shown in Fig.(2.9). This output is used to drive a Thyristor Firing Sequence Controller, that produces sequential pulses to turn-ON or turn OFF (through Commutation Circuit) the thyristors in a particular sequence, in order to produce a three-phase pulse width modulated wave at the output of Power Bridge and thus to control the speed of the induction motor.

Basically, in the fixed ratio system the ratio of carrier to fundamental frequency (denoted by R_c/f) remains constant over the operating range of the inverter. Where as in the variable ratio scheme the ratio R_c/f is varied along with the fundamental frequency in sequential steps, so as to produce only higher order harmonics in the output wave, that all easily filtered out. However, there is a limit in the increase of modulation ratio R_c/f or "the notch width" because of the switching capability of the power thyristors. The minimum value of 'Notch Width'(α) as well as minimum value of pulse width are limited by the combination of thyristor switching and recovery times. It can be observed that a typical 300 μ-sec operating time produces the following results:-

(a) The maximum voltage that can be obtained for a given R_c/f varies inversly with operating frequency.



(SYSTEM BLOCK-DIAGRAM)



(C.C.I. CURREN REGULATOR)

CURRENT REGULATED P.W.M. INVERTER MOTOR DRIVE

Fig. 2.10

(b) A minimum output voltage must be maintained for a particular R_c/f and operating frequency. This minimum output voltage increases with the inverter output frequency.

The basic problem with Fixed/Variable ratio modulation is that a provision is to be made for a 'Notch Width Clamp' that operates on d.c. reference level, which will not permit notch width (α) to become less than 300 micro-sec. In the adaptive ratio technique the carrier ratio R_c/f is automatically adjusted to take care of all possible limiting combinations of the pulse width, notch width and the carrier frequency and maintains constantly a high carrier frequency through out the entire operating range. Thus the adaptive ratio technique optimizes the operating characteristic of the modulated six-step inverter.

2.4.2 Output Current Regulation With P.W.M. Inverter in Inverter Motor Drive:

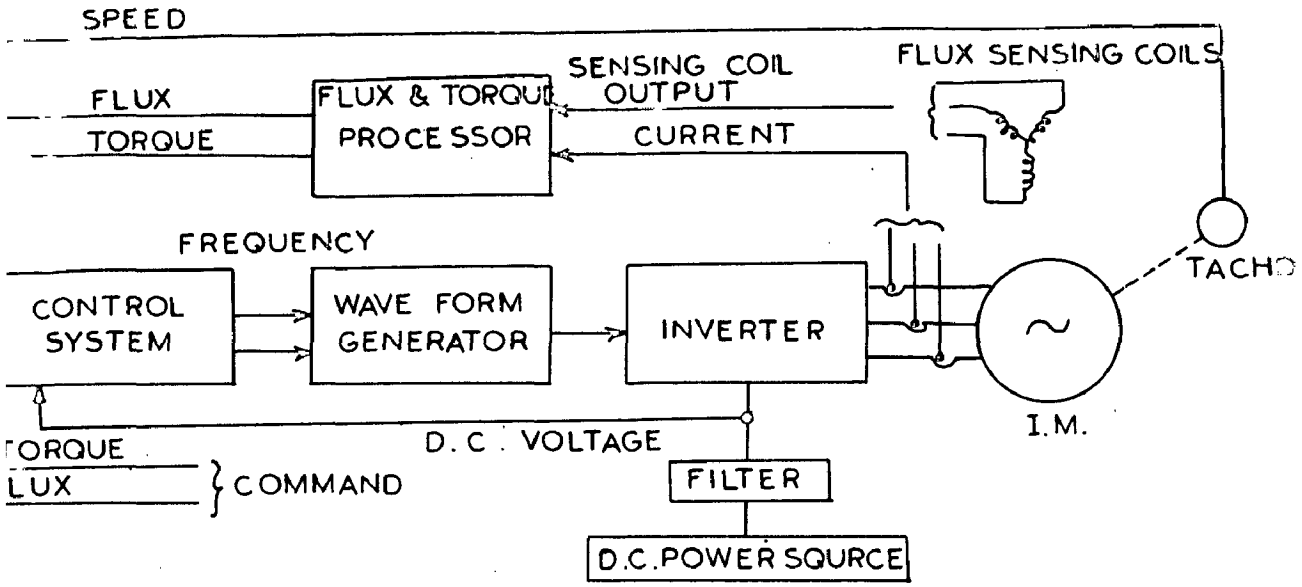
Basically current regulation plays an important role in the protection of solid state drives, operating from stiff voltage source[7]. The P.W.M. inverters, however are not suitable for peak or average current regulation with motor loading. For stable, average and peak current regulation, the control system must limit the rate of inverter output reduction. A variable frequency, non-regenerative reversible drive, with average current and overload protection is shown in Fig.2.10. Here the control provides a dual policy peak current limit and a frequency control loop is used to recover the rotor from pull-out i.e. the rotor frequency is not allowed to increase (or speed to decrease) more than rotor break down frequency at which break down torque

occurs. The dual policy substantially extends the range of induction motor over loads, that do not exceeds the inverter commutation capability. Thus the transient performance of the drive for rapidly applied motor overloads is substantially improved and practically a load step change of 3-p.u. and max. peak load current of 1-p.u. are easily achieved.

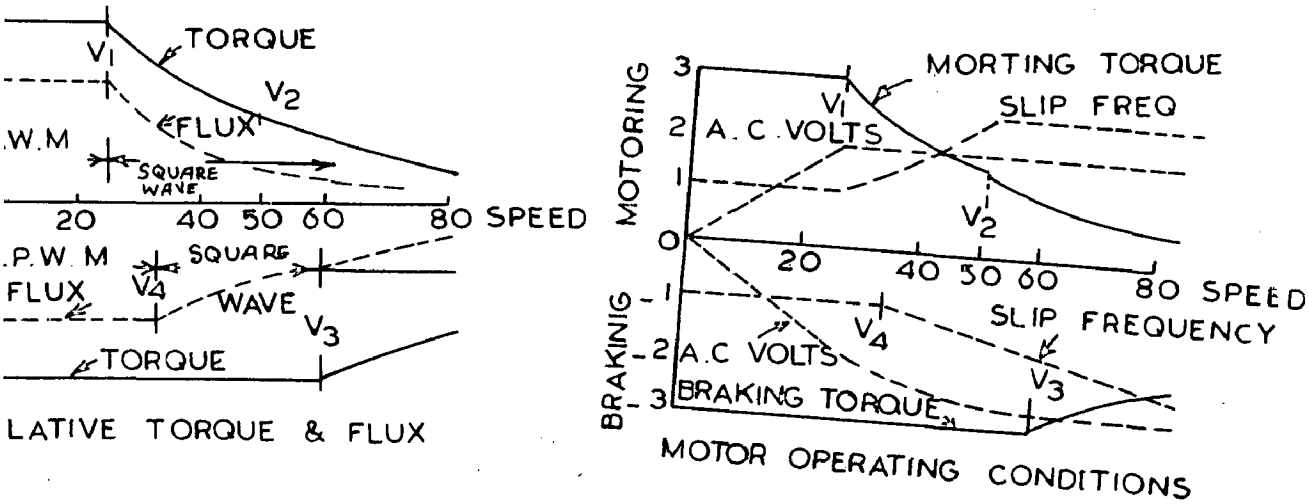
2.4.3 Direct-Flux and Torque Regulation in a P.W.M. Inverter-Induction Motor Drive[8]-

Almost all the methods of induction motors torque regulation assumed that the motor flux level is proportional to the applied voltage divided by the frequency and the torque is then proportional to the real component of stator current. In this technique inaccuracy in torque regulation occurs due to source voltage changes, load changes, and cable and motor internal voltage drops. An alternative method of torque regulation is sensing the slip frequency and real component of stator current to allow regulation of both flux and torque, if the rotor resistance is constant and known.

The method of torque and flux regulation described by[8] allows direct regulation of flux without depending upon the invariance of the motor parameters and also provides automatically and electrically isolated feedback signal. A simple calculation of motor torque that is not effected by time harmonics of stator voltage and current can be made using the flux signals and a measurement of stator current. A system is described in which inverter is sinusoidally pulse width modulated



SYSTEM - BLOCK DIAGRAM



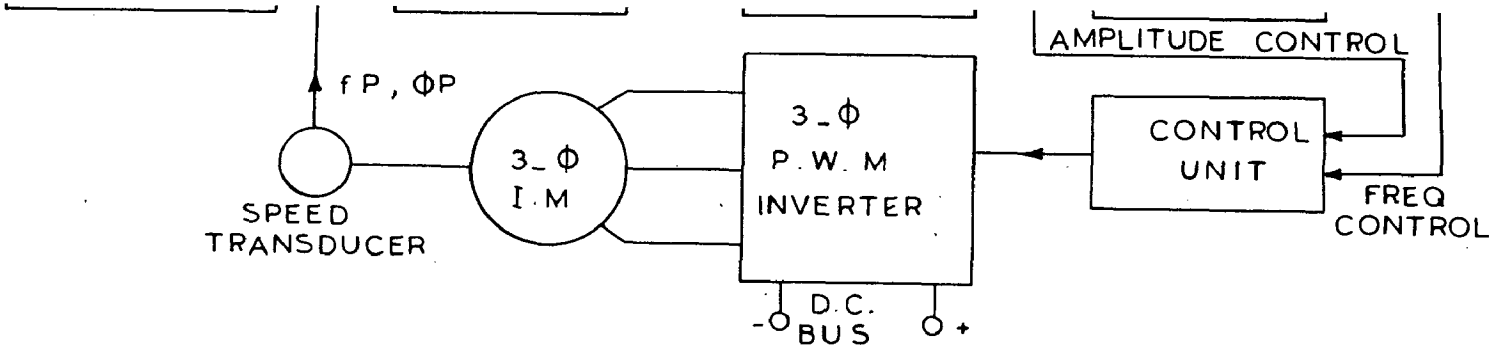
FLUX AND TORQUE REGULATION IN P.W.M INVERTER- INDUCTION MOTOR DRIVE.

Fig . 2.11

at low frequencies so as to shape the a.c. voltage waveform. At higher speed square wave operation is used for maximum efficiency. An intermediate transition mode of P.W.M that is not sinusoidal is used for smooth transition for P.W.M. mode to squarewave mode. The system in block diagram and desired motor operating conditions are shown in Fig.2.11. The flux and torque measurement is done by sensing the flux through flux sensing coils placed in the motor winding in which the voltage generated represents the flux. The level of the flux in the motor is always chosen to be regulated at the maximum in order to minimize the time for which the inverter is P.W.M. and maintaining the operation of the inverter at the minimum possible frequency. However, it should be noticed that this scheme does not require the use of tachometer.

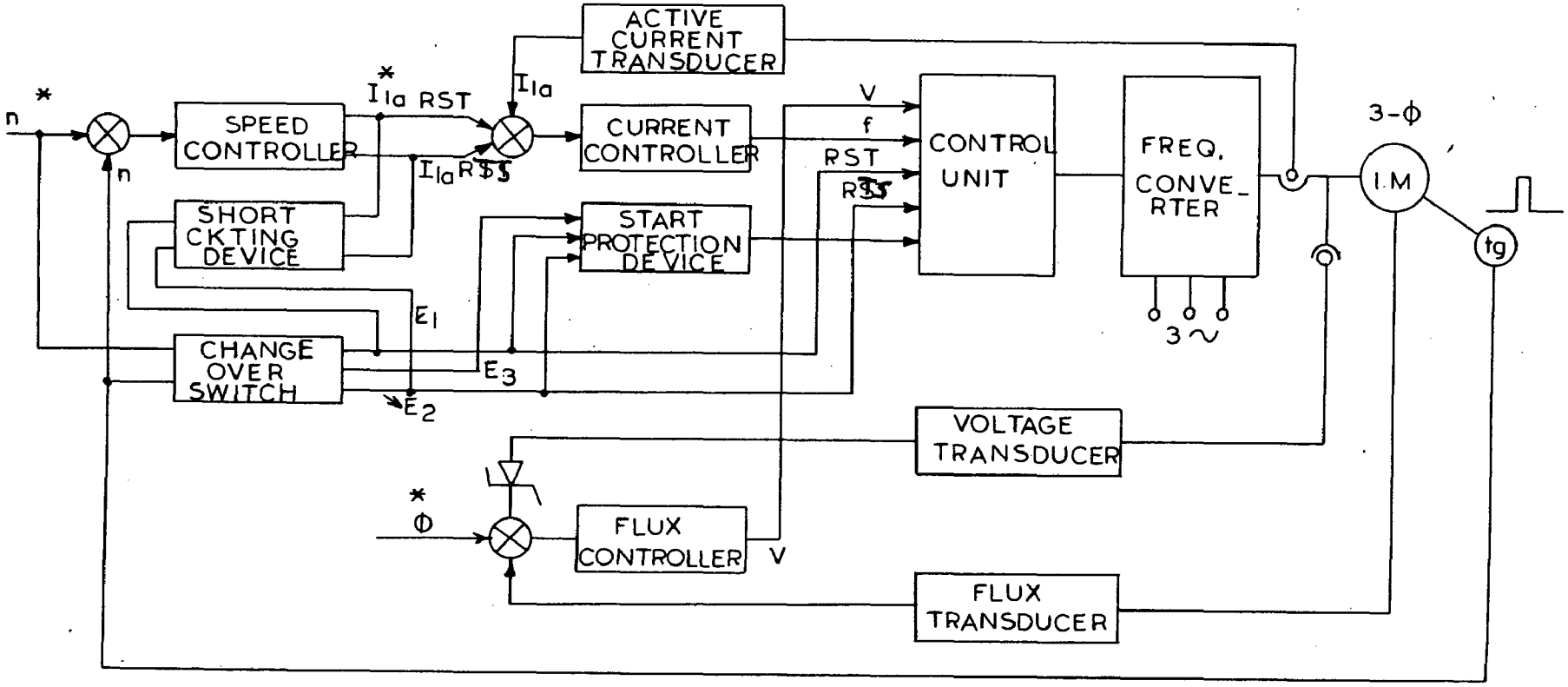
2.4.4 A Precision Speed Control of Induction Motor Using Phase Locked Loop:-

The particular application of an electric drive, basically determines the degree of speed control required. In some applications a simple open loop speed control of A.C. motor operating with solid state variable frequency inverter may be sufficient, while in some cases feedback control is essential in order to achieve better performance. In close-loop systems, conventionally an analog-servo feedback system is used in which any change in speed is sensed by a tachometer and is compared with a fixed reference voltage and gives a corrective signal. However in some applications, where an excellent speed regulation and fast



I.M. SPED CONTROL USING PHASE LOCKED LOOP

Fig. 2.12



SPEED REGULATING SYSTEM OF SQUIRREL CAGE I.M USING STATIC INVERTER

dynamic response are required, even analog-servo systems are not satisfactory. These feature can be achieved by using digital phase locked loop control system[9].

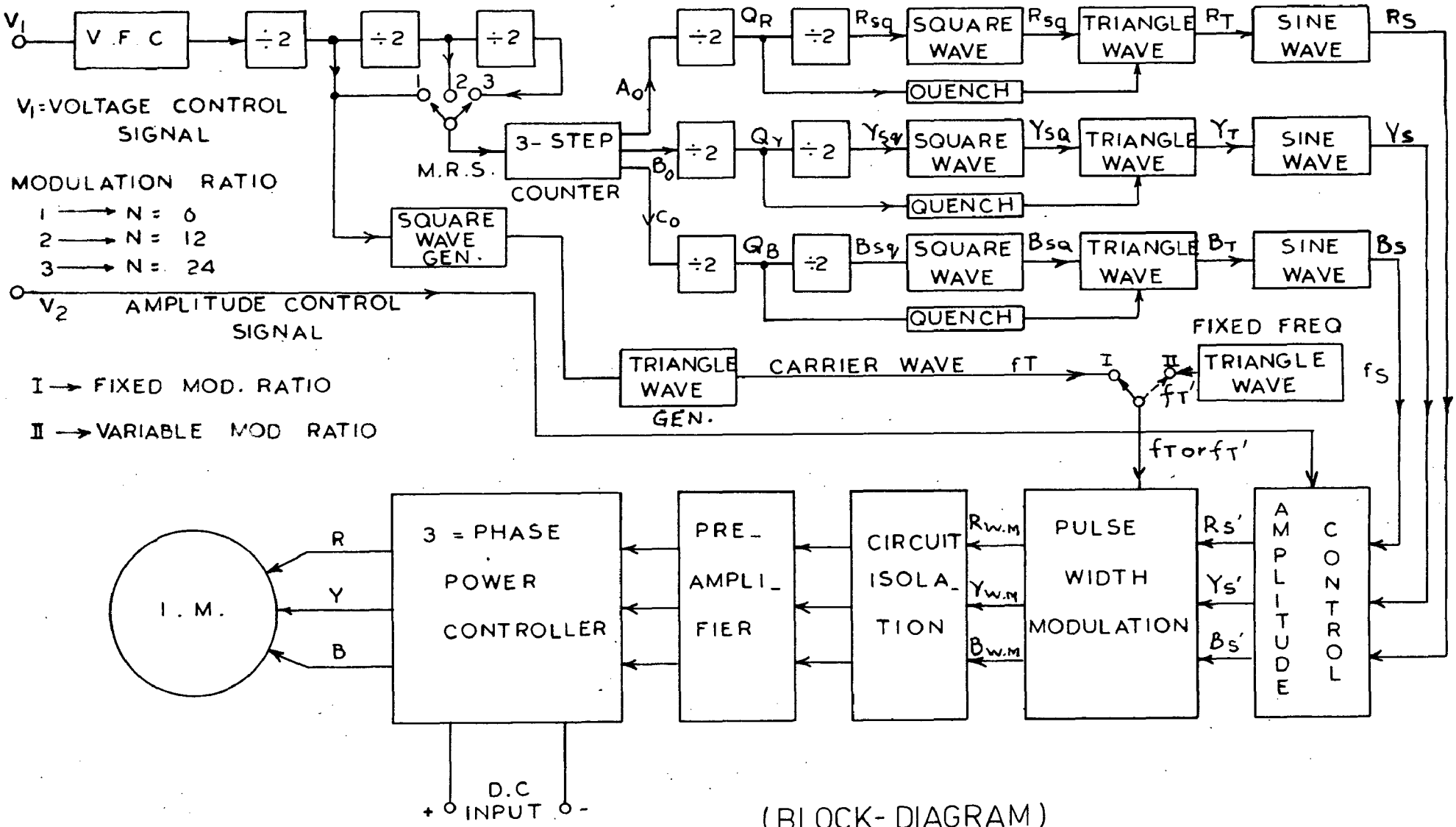
In a phase locked loop method; motor speed is converted to a digital pulse train which is synchronized with a reference digital pulse train. In this way by locking into the reference frequency, precise speed control of motor speed is achieved.The block diagram of an induction motor drive with phase-locked loop in the feedback network is shown in Fig.2.12, where a speed control accuracy upto 0.002 % can be achieved.

The phase locked loop control system is desired where motors must be synchronized to each other such as paper mill; textile mill drive or drives used for manufacturing of synthetic fiber.

2.4.5 A Completely Automatic Speed Regulating System:- I.D. LANDAU[10] has described a completely automatic control system for wide range speed control of three phase squirrel cage induction motor using static converter. The block diagram of the control system is shown in Fig.2.13. The speed and the active current of the motor (that is proportional to torque for a given value of flux) are controlled in a cascaded manner. This system also ensures an independent control of air gap flux by maintaining constant V/f operation in subsynchronous region and operation at constant rated voltage with in the frequency range above synchronous. The change over of from one control to other is accomplished by a gate circuit. The active current during overloads or transient

process is limited by the current control loop. Actually the limiting value of the active current is determined by the maximum value of the speed controller output voltage. A logical change over switch, which processes logically the preset speed and the measured speed value, provides a reverse operation. The logical change over switch actuates the control device of converter, a short circuiting device and the start and protection device.The short circuiting device always short circuits one of the speed controller output $I_{1a}R_{ST}$ or $I_{1a}R_{TS}$ (either in phase or anti-phase with respect to input) according to the motor direction of rotation so that sign I^*_{1a} = Sign ($|\hat{n}|-|n|$). The astrick (*) indicate the preset parameters and without astrick (*) as the measured one.

ELECTRONIC CONTROL SCHEME FOR THREE PHASE PULSE WIDTH MODULATED INVERTER



(BLOCK- DIAGRAM)

Fig- 31

CHAPTER - III

A SOLID STATE THREE-PHASE P.W.M. INVERTER - CONTROL UNIT

3.0 Description of the Control Scheme

A solid state three phase P.W.M. inverter, used for speed control of induction motor basically performs the following two functions:-

(a) It delivers a Three Phase Sinusoidal Pulse Width Modulated output voltage of variable amplitude.

(b) It controls the frequency of sinusoidal three phase output.

Based upon the above two basic requirements, ~~and this specific features of a~~ Solid State Three Phase P.W.M. Inverter employing Power Transistor as a switching element (as discussed under section 1.4), ~~which~~ is designed and fabricated in this thesis. For simplicity the design and fabrication of P.W.M. Inverter is devided into two parts:-

I - The design and fabrication of Control Unit, the design of which is presented in this chapter.

II - The design and fabrication of Power Unit, the design of which is presented the next chapter i.e. chapter IV.

The basic control scheme used for control unit is depicted in the form of block diagram in Fig.3.1. The design considerations and the basic design of each individual block is presented in the subsequent part of this chapter (i.e. from sections 3.1 to 3.4).

As shown in block-diagram (Fig.3.1), the control scheme employ two control signals V_1 and V_2. The d.c. signal V_1 controls the fundamental frequency of the output sinusoidal P.W.M. wave, while the signal V_2 controls the amplitude of this P.W.M. output wave. Further as shown in block-diagram (Fig.3.1) the signal V_1 is fed to a voltage to frequency converter (V.F.C.) that generates the pulses directly proportional to this signal. The pulses from V.F.C. are divided through a binary counter in order to maintain a fixed frequency ratio of the sinusoidal reference wave to the triangular carrier wave (that is required to be generated). A proper Modulation Ratio, denoted as $N = f_T/f_s$ where f_T = frequency of triangular wave and f_s = frequency of reference sine wave can be selected through a Modulation Ratio Selector Switch (M.R.S.); such as N = 6,12 or 24.

In the next stage a three-step ring counter to which the pulses are fed after a proper M.R. section; generate three seperate sequential square pulses, A_o, B_o, C_o, as shown in Fig.(3.1). These pulses on further division by a factor of four (actually divided by a factor of two in 2-stages) and with proper inversion generate three square pulses that are at 120 degree phase displacement (i.e. R_{sq}, Y_{sq}, and B_{sq}). These square pulses are unidirectional pulses and are converted to bi-directional square waves R_{SQ}, Y_{SQ} and B_{SQ} through uni-directional square pulse to Bi-directional square pulse converters.

These square waves are then converted to triangular waves (R_T, Y_T and B_T) through square wave to triangular wave converters or analog integrators.

In an analog-integrator any d.c. off set (either in the input square waves or because of operational amplifier used in integrator), causes a problem of saturation at the output. Hence inorder to overcome this problem, Quenching or Reset circuits are also added to the basic integrators, so as to provide the Reset or Quench pulses to the integrators and are discussed in detail later under section (3.1.4). Further in order to maintain the amplitude of the triangular waves constant with respect to the variation of the reference frequency (through V.F.C.), a d.c. signal V_1' proportional to V_1 is fed to square wave converters that vary the amplitudes of the square waves as the frequency is varied through V_1. Now the triangular waves are converted to sine waves of constant amplitude through the wave-shaping or triangular to sine-wave converters. Thus a set of three phase (120 degree phase displaced) constant amplitude reference sine wave (i.e. R_S, Y_S and B_S) is generated.

In order to maintain a constant V/Hz ratio, the amplitudes of R_S, Y_S and B_S are controlled through analog multipliers or some other amplitude control circuits with the help of a separate d.c. signal V_2(i.e. Amplitude Control Signal).

The amplitude controlled reference sine waves are Pulse Width Modulated through P.W.M. circuits where the

Sinusoidal Pulse Width Modulation is achieved through the comparator circuits. A P.W.M. circuit receives at its input, the amplitude controlled reference sine wave (R_S' or Y_S' or B_S') and a triangular carrier wave f_T or f_T', and generates a train of width-modulated pulses that are generated at the cross-over points of reference sine wave and the triangular carrier waves. Basically, there are two schemes of Pulse Width Modulation:-

(I) Fixed Modulation Ratio :- Here the ratio of triangular wave to sinusoidal wave is kept constant and is achieved by proper division of pulses after V.F.C. as shown in Fig.3.1.

(II) Variable Modulation Ratio :- Here the ratio of triangular wave to sinusoidal waves (f_T/f_S) varies inversely as the frequency of the reference sine waves is varied i.e. the M.R. (f_T/f_S) increases as the frequency of sine waves is reduced, and the value of M.R. is maximum when the frequency of sine wave is minimum.

The Pulse Width Modulated Waves (R_{WM}, Y_{WM} and B_{WM}) are now required to be transferred to the Power Control Unit, ensuring proper circuit isolation and retaining the pulse widths. The circuit isolation is normally achieved through optical isolators that employ Light Emitting Diodes and Photo-transistors. But there are two main problems in employing optical isolators :- (i) The output signal of Photo-transistor is very weak in strength and requires, large amplification.

(ii) Some spurious pulsesmay be generated because of ground noise or supply transients. In the scheme presented in this dissertation a new technique has been used for circuit isolation in which the width modulated pulses are first modulated with a high frequency (say 25 KHz or more). The high frequency modulated pulses are fed to the primary of pulse transformers. The pulse transformers transfer, The H.F. modulated pulse at their secondaries with proper circuit isolation. The high frequency superimposed width modulated pulses transferred at the secondaries of pulse transformers, are demodulated and produces an exact replica of pulse width modulated pulses i.e. R_{WM}, Y_{WM} and B_{WM}.

The width modulated pulses (after demodulation) are amplified in current strength through Preamplifier/Driver and then fed to Power Control Unit. The pulses after driver stage are sufficient in current strength to drive the Power Transistors in Power Control Unit at full rating. The three phase power control unit delivers at its output a three phase P. W. M. supply to control the speed of induction motor. With proper coordination of two control signals V_1 and V_2, it is possible to operate the inverted fed induction motor drive in constant Volt/Hz mode.

The design and development of the control scheme as described above is devided into the following groups :-

(i) Generation of Three Phase Variable Frequency, (constant amplitude) reference sine waves and Triangular carrier waves.

(ii) Amplitude Control of Three Phase Reference sine waves with a control signal V_2.

(iii) Pulse Width Modulation of amplitude controlled sine waves with the triangular wave.

(iv) Circuit Isolation.

3.1 Generation of Three Phase Reference Sine Waves and Triangular Carrier Waves

As described in section 3.1 ; the Three Phase sine wave is generated by converting the control signal to pulses of proportional frequency through VFC and then converting these pulses to three-sequential pulses through a 3-step Ring Counter. These pulses are then converted to three phase square, triangular and finally to sine waves through square wave, triangular wave and sine wave converters. Similarly triangular waves are generated either by suitable division and integration or by a seperate circuit. Hence the actual design can be further sub-devided into following sub-groups:-

(1) Design of voltage to frequency converter.

(2) Design of Three-Step Ring Counter.

(3) Design of Square-Pulse to Square Wave Converter.

(4) Design of Square Wave to Triangular Wave Converter.

(5) Design of Triangular Wave to Sine Wave Converter.

3.1.1 Design of Voltage to Frequency Converter:-

(a) Criterion for Selection of Proper Voltage to Freq. Converter:-

A voltage to frequency converter produces, Output frequencies that are proportional to an input. The selection

of a particular type of V.F.C depends upon the following factors:-

(a) Input requirements:-

(i) Input signal for full scale 'f' out (Voltage and Current Limits).

(ii) Whether input signal is single ended or differential.

(iii) Nominal input impedence of V.F.C.

(iv) Circuit input off set voltage and off set current.

(v) Input supply and power.

(b) Output available :-

(i) Output frequency range for full range of input signal.

(ii) Non-linearity in voltage to frequency conversion.

(iii) Output pulse width (Min/Max).

(iv) Full Scale-temp coefficient ($\pm$ p p m/0^{o}C max).

(v) Conversion time.

Out of the above factors, the accuracy and conversion time are the most important factors, that must be given due considerations for the selection of a particular V.F.C circuit current or Integrated circuit.

Presently, very precise (highly accurate and linear) and high frequency range, voltage to frequency converters are

available in integrated circuit chip form. We may have V.F.C with frequency range from 10 KHz to 5 MHz and linearity ranging from 1 % to .005%. But these V.F.C chips are very costly.

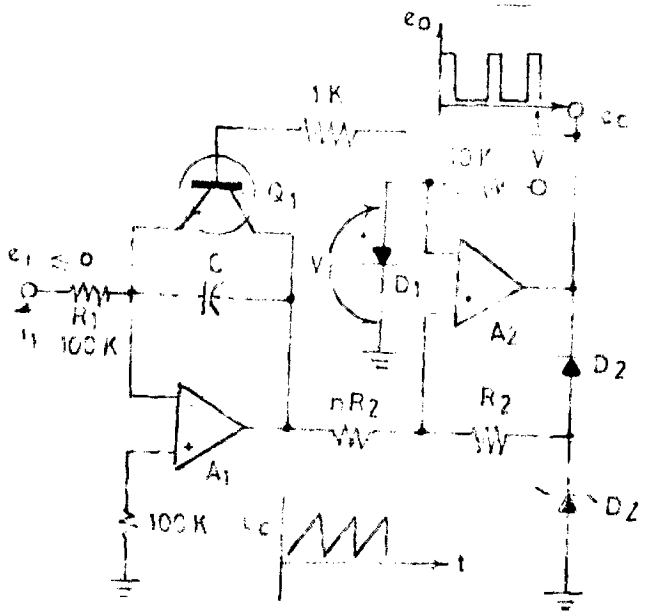
The precison V.F.C chips are not readily available in India. The only readily available chip is 566, that has frequency range of 10 KHz and linearity of only 1 % .

For our purpose where 10 KHz frequency is sufficient and 1 % linearity is tolerable, the 566 chip seems to be a good selection and we could have used it no doubt but in some more precise variable speed drives we may require a better linearity. In view of this fact we have selected a voltage to Frequency Converter circuit[11], that employ only two general purpose operational amplifiers and some discrete components. This circuit has low cost and a good linearity of the order of .05 % .

Basic Design of Voltage to Frequency Converter :-

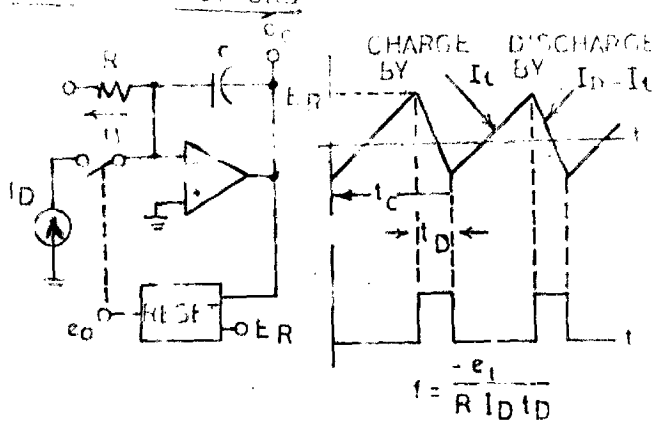
The basic circuit of a V.F.C is shown in Fig.3.2 and consists of an integrator and a comparator. When an input signal of constant amplitude is applied to the integrator, it charges the capacitor C_1 at the rate defined by the time constant set by R_1 C_1 combination and causes the output of the integrator to increase linearly with time. The comparator employs a zener diode to control the high threshold and has hysteresis to provide low threshold. In this circuit a negative input voltage causes the output of the integrator

VOLTAGE TO FREQUENCY CONVERTORS



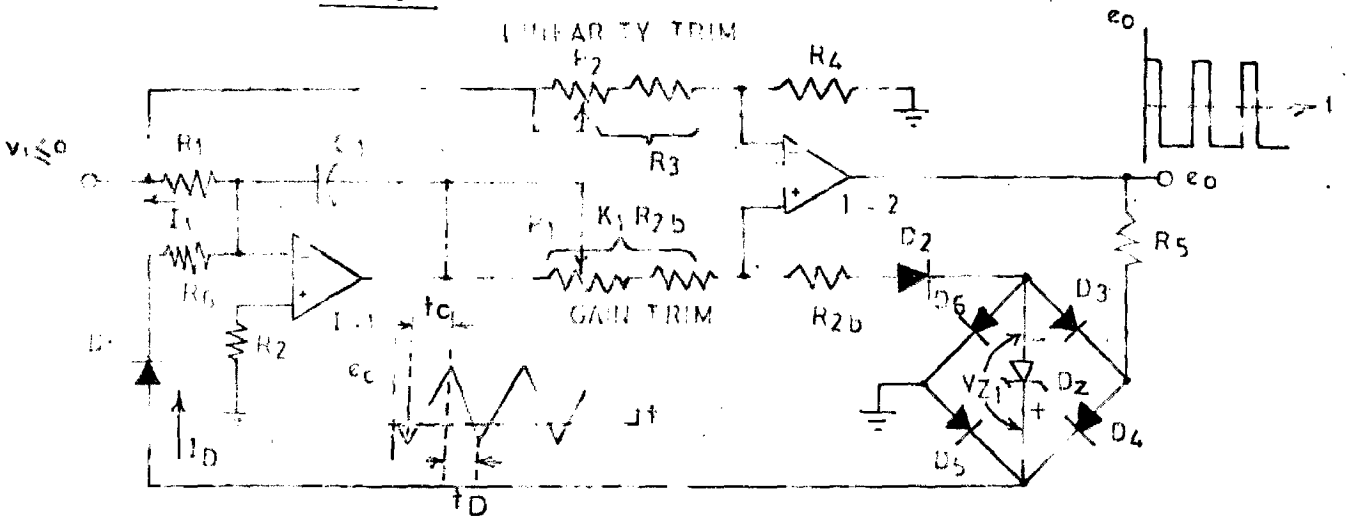
COMPARATOR CONTROLLED RESET CKT

FIG 3.2



CONTROLLED CHARGE RESET CKT

FIG 3.3



PRECISION VOLTAGE TO FREQUENCY CONVERTOR

(CONTROLLED CHARGE RESET TYPE)

FIG 3.4

ıncrease to $o_c = n V_Z + (n+1) V_f$. At this point the com-
ıtor output swings to positive and turns on the reset switch
The reset switch discharges the capacitor C and it conti-
; untill o_c reaches the low threshold of the comparator.
low threshold equals the forward voltage drop across the
le D_1, or the voltage level at the inverting (-) input of
comparator. It can be observed that R_2 supplies no positive
lback so long as the output is positive, because of diode
The diode D_1, always keeps the lower threshold about zero.
; is necessary since Q_1 can not discharge the capacitor C
ow the transistor saturation voltage. The change in capacit
tage during each cycle between two comparator switching poin
n($V_Z + V_f$) as shown in Fig.3.2. The operating frequency of
converter is determined by time required for this change in
ıcitor voltage (i.e. Δo_c). If we assume that if the input
rent i_1 remains constant during the charging cycle, then
charging time is given by $\Delta t = C.\Delta o_c/i_1$ and the frequency
$f = 1/\Delta t = -o_1/nCR_1(V_Z + V_f)$
performance of this V.F.C. depends upon the off set,
carity and gain. The error produced in output frequency
ause of offset produced by the operational amplifier A_1,
given by

$$= (V_{os1} + I_{os1}.R_1)/[nCR_1(V_Z + V_f)] \qquad (3.1)$$

re V_{os} is the off-set voltages and I_{os} is the off-set
rent of the operational amplifier A_1.

The Non-Linearity error is introduced by the discharge time t_D and the limited gain of A_1 and is given by

$$\Delta fN = f.[f.t_D + \frac{n(V_z + V_f)}{A_o\ e_1}] \qquad (3.2)$$

= Non-linearity.

The slow rate of the op-amp or the maximum current of the discharge switch Q_1, which ever have more limiting effect determines the reset time t_D. Normally the gain error is governed by the tolerance variation of R_1, C, R_2, nR_2, D_1 and D_2.

A technique to achieve better linearity with higher frequency :-

The operating frequency limits of a V.F.C. are governed by two factors:-

(a) The conversion time, that places a limit on the minimum operating frequency and for practical conversion times not exceeding 1-sec., the minimum usable converted frequency is 1 Hz.

(b) The resulting time of the integrator capacitor limits high frequency operation.

Also the non-linearity error is introduced by the reset time and to reduce this error to .01 %, the reset time must be no more than .01 % of the minimum signal period i.e. 10-n-sec for 10 KHz range. Practically it is very difficult to achieve such short reset intervals and even if achieved they produce sharp pulses of such a small pulse width that they are absorbed by the line capacitance itself. Hence a technique is employed to

supply to the integrating capacitor, a controlled amount of resetting charge, rather than a fixed reset voltage in order to extend dynamic range for improved precision.

The principle of operation of a V.F.C. employing controlled charge reset circuit is depicted in Fig.3.3. In this circuit the reset charge is supplied each time, the input signal charges the integrating capacitor to a reference level E_R, at a rate determined by the current i_1 from an input signal. At the reference level the discharge current I_D, discharges the capacitor for a period t_D. As the process repeats the charging and discharging voltages are equal and opposite since $Q_c = i_1 t_c = - Q_D = I_D t_D$.

Where I_D = Discharge current ; t_D is the discharge time ; i_1 is the input charging current and t_c is the charging time. Also Q_c and Q_D are the amount of charges that provide charging and discharging respectively.

The frequency of oscillation is given by $f = 1/t_C = 1/i_D \cdot t_D \cdot i_i$

$= -e_1/R.I_D.t_D.$

If I_D and t_D are constant we can clearly observe that $f \propto e_1$.

A Precision Voltage to Frequency Converter :-

The circuit of a precision VFC employing controlled reset charged reset technique is shown in Fig.3.4. Similar to comparator controlled reset circuit as shown in Fig.3.2, this circuit also contains an integrator and a comparator. But the

comparator in this precision circuit provides a controlled discharged current I_D and a fixed discharge time and thus ensures a constant reset charge of $Q_D = - I_D.t_D$. A fixed voltage across the zener diode feeds a controlled discharge current through a summing resistor R_6 . The input signal is coupled to the comparator in order to produce a fixed discharge time, rather than a fixed voltage.

If we apply a negative signal $V_1 \leq 0$, then the output of the comparator is positive. This positive output conducts a current through D_4 , D_5 and D_6 . Now a voltage of $V_z+V_{f6}-V_{f1}$ is established across the resistor R_6 and creates a discharge current of $I_D = V_z/R_6$ since $V_{f6} = V_{f1}$. Also the current $I_D > I_1$ and causes a negative going ramp at the output of the integrator I-1. This ramp continues to the 1st trip point of the comparator. The first trip point of the comparator is set only by e_1 because the diode D_1 disconnects the positive feedback for positive values of the comparator and is given by $e_c = V_1/K_2$ where $K_2 = R_4/(R_3 + R_4)$. When the negative going ramp voltage at the non-inverting pin of I-2 comparator reaches this trip point, the output of the comparator swings from positive to negative voltage. This negative voltage applies reverse bias at the diode D_1 and stops discharging. The current I_1 now starts charging the capacitor till the second trip point of the comparator is reached.

The second trip point of the comparator is decided by e_1 and the positive feedback of the comparator, since the diode

D_2 now conducts and completes the positive feedback path. The diode bridge in this case inverts the voltage presented by the zener. Thus the same zener diode D_2 establishes a second trip point as well as the discharge current (as indicated earlier). The zener diode thus play an important role in the operation of this VFC. The zener creates a voltage of $-V_B = V_{f5} + V_{f2}$ on the comparator feedback resistor R_2b. The second trip point is $e_0 = K_1(V_B + V_1/K_2) + V_1/K_2$, as $V_{f5} = V_{f2}$.

The total change in e_c is given by the difference of these two trip points i.e. $\Delta e_c = K_1 (V_B + V_1/K_2)$ we can note here that Δe_c is a function of V_1 and hence makes discharge time t_D a constant. The discharge time $t_D = \Delta e_c \cdot C/(I_D - I_1)$ $= \Delta e_c \cdot C/(V_B/R_6 + V_1/R_1)$ or $t_D = \dfrac{K_1(V_2 + V_1/K_2)C}{(V_B/R_6 + V_1/R_1)} = K_1 \cdot R_6 \cdot C$

since $R_1 = K_2 R_6$. With t_D a constant, the convertor response relates linearly to

$$e_2 \propto a_f = e_1/(R_1 K_1 V_2) \qquad (3.3)$$

As discussed already the linearity-error depends upon the reset or the discharge time, and therefore once the discharge time is made constant, the circuit becomes highly linear and error is minimised by reducing t_D to a minimum by supplying a maximum possible controlled reset charge that greatly depend upon V_B. The performance of this circuit basically depends upon the component selection, the off set in operational amplifiers and the linearity error.

Calculation and Selection of Values of the Components for Voltage to Frequency Converter:-

It is evident from the block diagram that the max.ratio between the frequency of voltage to frequency converter and the frequency of three phase reference sine waves ($f(V.F.C.)/f_s$) is 96. Hence when the reference sine waves have a maximum frequency of 100 Hz, the V.F.C. output would have a maximum frequenc; of 9.6 KHz at a max. controlsignal of -10V. V.F.C. employ the operational amplifiers 741 for I_1 and I_2 as shown in Fig.3.4 and because of its gain band width limitation it can not give a good linearity above 5 KHz. It is therefore recommended to operate V.F.C. in two ranges (i) 5Hz to 50 Hz and (ii) 50 Hz to 100 Hz ; if the modulation ratio is to be selected as 24. For a modulation ratio of 12 or 6 the range (i) itself can be used for frequency range of 5Hz to 100 Hz, since V.F.C. would operate at a max. freq. of 5 KHz in these of cases.

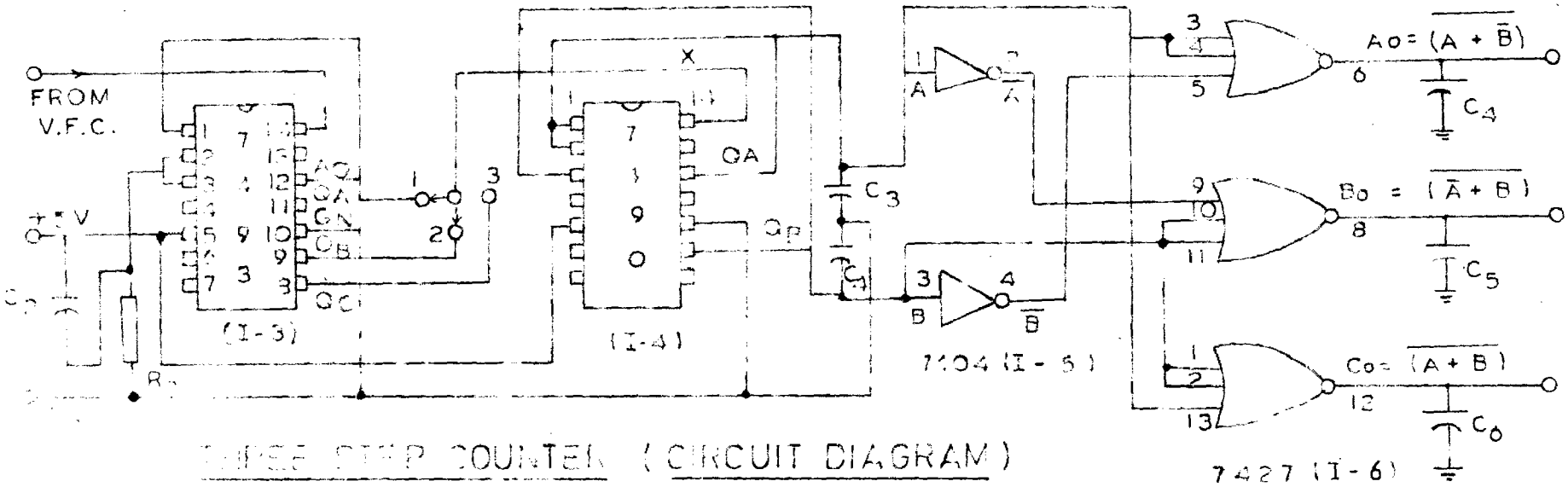
As shown in equation (3.3), the output frequency of the V.F.C. is given by $f = e_1/(R_1 C K_1 V_z)$. Now selecting R_1 = 100 K ; K_1 = 1 (such that $K_1 . R_2 b$ = 2.2 K-ohm + 1 K-ohm preset and $R_2 b$ = 3.3K-ohms) ; V_z = 9.1 Volts and operating frequency = 5 KHz for e_1 = -10V, we get the value of capacitor as

$$C = \frac{e_2}{f . R_1 . K_1 . V_z} = \frac{1}{5 \times 10^3 \times 10 \times 10^3 \times 1 \times 9.1}$$

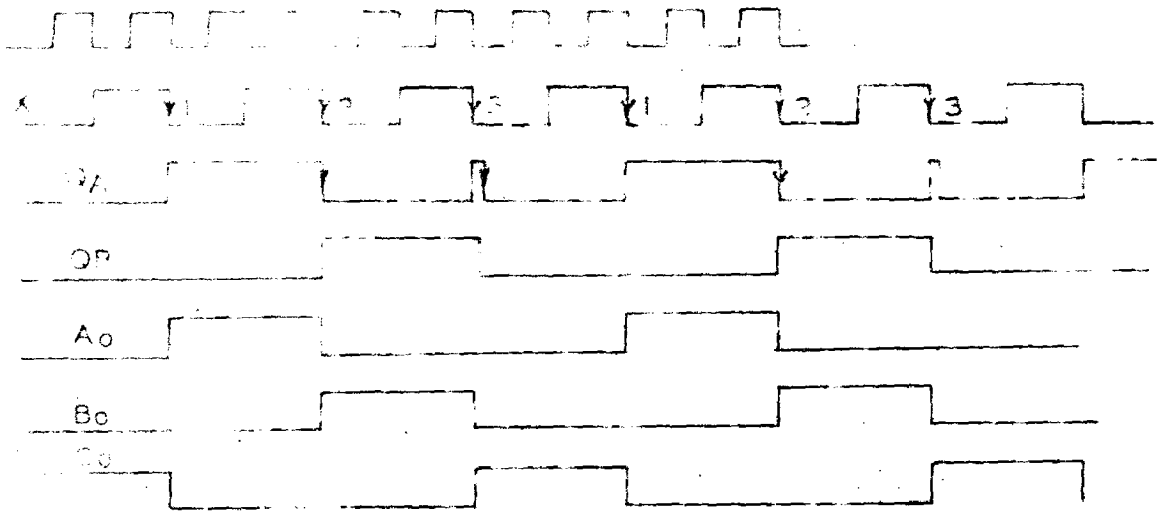
i.e. $C = \frac{1}{45.5} \times 10^{-6} = 0.022\ \mu F.$

The value of R_5 is selected to be 500 ohm, so that it gives a sufficient regulating current to zener D_z when e_0 is

positive. The discharge current I_D is fixed by V_{B1} and R_6 and for a zener value of 9.1V, the value of R_6 = 1K is justified since it shall feed a discharge current I_D = 9 mA (approx.) that is much larger (about 100 times) than the maximum input current which is .09 mA, that is the basic requirement. R_2 is economically selected as 10K while R_5 = 1K and P_2 + R_3 = 2.2K + 1K can serve as an accurate linearity trim. The diodes D_1 to D_6 should be of high speed type in order to have a good performance at high frequency upto 10 KHz.



THREE STEP COUNTER (CIRCUIT DIAGRAM)



(WAVE FORMS)

.1.2 Design of Three Step Counter :- The output from voltage to frequency converter is in the form of pulses. This is converted to square wave with the help of a binary counter 7493 by dividing by two. The square wave is further divided by the same factor in next two steps. As shown in Fig.3.5, this division can be obtained at the outputs Q_A , Q_B and Q_C of IC 7493 (I-3). These outputs are connected to a Modulation Ratio Selector Switch which can select any number 'N' = Frequency of Triangular Carrier/frequency of sine wave. The pole of the selector switch is connected to the 3-step ring counter.

The 3-step ring counter gives a pulse at each step of counting through a digital counter IC-7490 (I-4). The truth table for a counting sequence of 1 to 3 is given below:-

Counting Sequence	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1/0	1/0

The output Q_A , Q_B , Q_C or Q_D are at low level (= 0.8VI) for state 0 and at high level (≈ 3.5V) for state 1. Now if the output Q_A and Q_B are connected to 'Reset to Zero', inputs (R_{01} and R_{02}) of the 7490, then the counter will reset at every third pulse. In order to obtain a separate pulse at each step ;

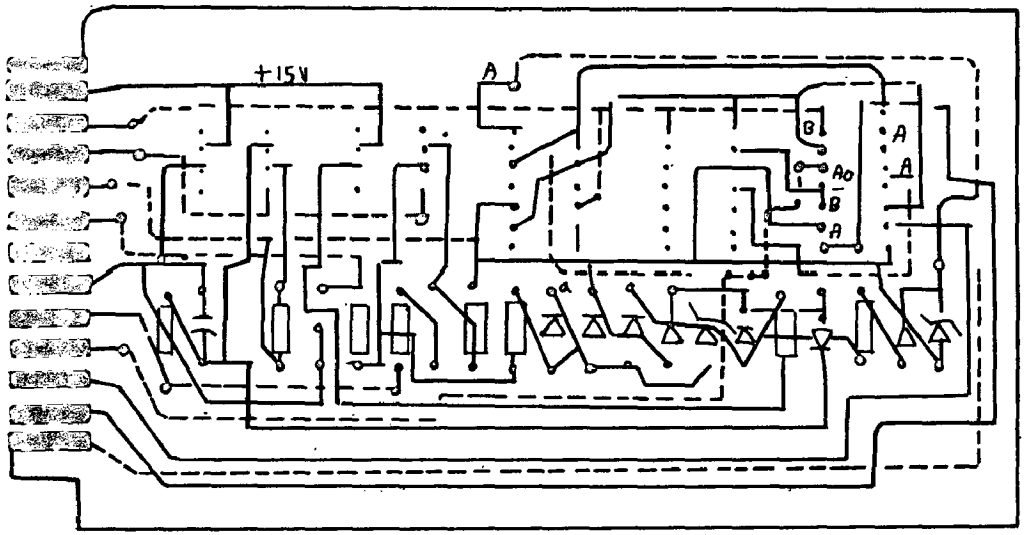


Fig. 3.6

COMPONENT LAYOUT OF V. F. C & 3 STEP COUNTER

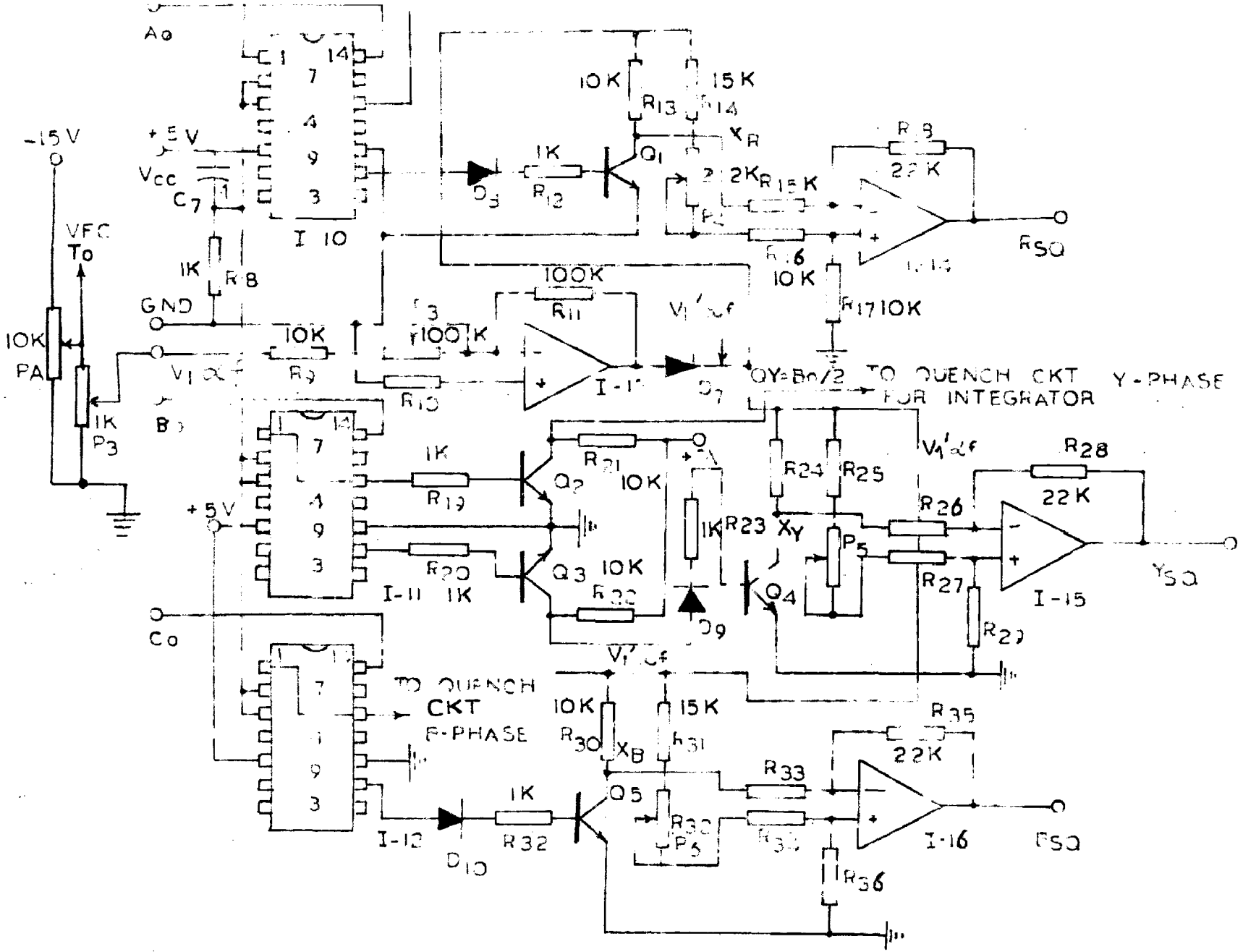
Q_A and $\overline{Q_B}$ are fed to a three input NOR gate to get a pulse at 1st step ; $\overline{Q_A}$ and Q_B to second NOR gate to get a pulse at 2nd step and Q_A and Q_B to third NOR gate to get a pulse at 3rd step. The signals $\overline{Q_A}$, $\overline{Q_B}$ are achieved by a flip-inverter 7404 (I-5) and NOR operations through a Triple 3-Input NOR gate 7427 (I-6). The output of a 3-step counter are three signals $A_0 = (\overline{A + B})$; $B_0 = (\overline{A + B})$ and $C_0 = (\overline{A + B})$. These three signals are used to generate three square pulses having a phase displacement of 120 degrees. This is achieved by dividing the signals by a factor of two in two steps through the 4-bit binary counters 7493 (I_7 , I_8 , I_9). The signal R_{sq} is obtained directly by division through I_7 , Y_{sq} is obtained by inversion after division through I_8 and B_{sq} is also obtained directly after division through I_9 , The divided output is taken from Q_B terminals of the respective I.C.

Fig.3.5 also, depicts the various wavefoms of a 3-step counter. Fig.3.6 depicts the component layout for V.F.C. and 3-step Ring Counter.

3.1.3 Design of Square Pulse to Square Wave Convertor:- The following

The following points should be taken into consideration:-

(a) The outputs after I_7 , I_8 , and I_9 as shown in Fig.3.5 are square pulses with their amplitudes as 0.8V at state '0' and about 3.5 volts at state '1'. These signals are converted to bidirectional symmetrical (with respect to ground) square waves, that can be further shaped to



CIRCUIT-DIAGRAM FOR THREE SEQUENTIAL SQUARE PULSES TO THREE PHASE SQUARE WAVE CONVERSION

Fig 3.7

triangular and sine waves. Symmetrical bidirectional shape of the square pulses is necessary for the generation of sine wave output having a symmetry with respect to ground.

(b) Since the signals R_{sq} , Y_{sq} and B_{sq} do not reach at zero voltage at low states. There is always a d.c. level carried over to the next stage that causes a d.c. off set in the output of next stage i.e. the bidirectional square wave. Hence the circuit should be designed properly to eliminate this source of error.

(c) The square wave can be shaped to a triangular wave by using an Integrator. But the main draw-back (discussed in detail in section 3.1.4) is that the amplitude of the trangular wave would be frequency dependent and would decrease with increase of frequency. Further, the frequency is to be varied over a wide range say 10 Hz to 100 Hz. Therefore it is required that the amplitude of triangular wave remain constant with respect to the variation of frequency in order to produce the sine waves of constant amplitude through triangular wave to sine wave converters.

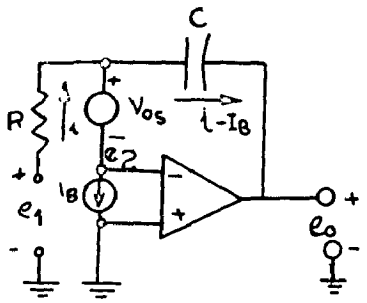
Therefore it is needed to design a circuit that would convert the square (unidirectional) pulses R_{sq} , Y_{sq} , B_{sq} , to bi-directional square waves R_{SQ} , Y_{SQ} and B_{SQ} , without any d.c. off set and with their amplitudes increasing proportional to the frequency. The circuit used to achieve the above performance is shown in Fig.3.7.

The supply voltage V_1' for transistors Q_1 , Q_4 , and Q_5 is proportional to the frequency control signal V_1 and therefore the amplitudes of the signals X_R , X_Y and X_B at the collectors of Q_1 , Q_4 , and Q_5 (as shown in Fig.3.7) are proportional to the frequency. The presets P_4 , P_5 and P_6 are used to adjust the symmetry of the square waves R_{SQ} , Y_{SQ} and B_{SQ} at the outputs of the operational amplifiers (I_{10} , I_{11} and I_{12}) respectively. The operational amplifier I_{13} provides a supply V_1' and V_1 (i.e. frequency control signal) for the transistors Q_1 , Q_4 and Q_5 after suitable amplification, adjustable through P_3 and R_{11} .

The signals $Q_R = A_{0/2}$; $Q_Y = B_{0/2}$ and $Q_B = C_{0/2}$ are used to generate Quenching or Reset pulses for the integrator every cycle, in order to remove any d.c. off-set existing either because of input square wave or because of the operational amplifier used in the integrator circuit. The square waves R_{SQ} , Y_{SQ} and B_{SQ} with their magnitude being proportional to V_1 (or the frequency) are converted to triangular waves by using an analog-integrators. The basic design and some design considerations for an analog-integrator is discussed in the next section (i.e. section 3.1.4). Selection of components values for square pulses to square wave conversion circuit is as follows :-

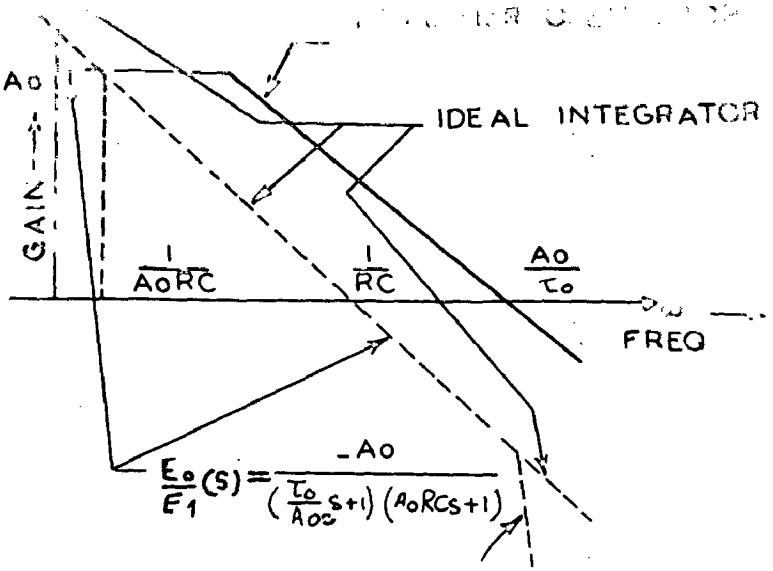
The supply voltage for the transistors Q_1 , Q_4 and Q_5 is precisely controlled through presets or potentiometers P_A , P_B and P_3 , as shown in Fig.3.7. The preset P_A gives a control signal V_1 for V.F.C. and presets P_B and P_3 through operational

amplifier I-13, give a precise proportional control of V_1 (i.e. produces V_1' and V_2) and modulates the amplitudes of the square waves. and The amplitude control ranges from 1.0 Volts to 10 Volts for a frequency variation from 5 c/s to 50 c/s. Thus the amplitude of triangular wave (generated by integration of the amplitude modulated square waves) remains constant by the variation of frequency. The proper choice of presets P_A , P_B and P_3 are 10 K, 1K and 100 K ohms respectively, while the feedback resistanced R_{11} is taken as 100 K. The resistance R_9 and R_{10} are taken as 10 K ohms, taking into consideration that sufficient bias current flows through (-) terminal of the operational amplifier I-13 (i.e. 0.1 mA at 1 Volt input across $R_9 + P_3$). Transistors Q_1 , Q_4 and Q_5 (BC 107/SG 104) act as switching transistors and therefore R_{12} , R_{23} , and R_{32} can be safely assumed equal to 1K ohms while R_{13} , R_{24} and R_{30} = 10 K. The collector voltages of these transistors are fed to the non-inverting terminals of I-14, I-15 and I-16, through R_{15} = R_{26} = R_{33} = 10 K ohms, taking into consideration that the proper bias-currents is available at the non inverting terminals, at the lowest possible voltages appearing at the collectors of the transistors. The feedback resistances R_{18} , R_{28} , R_{35} are suitably selected equal to 22 K-ohms, so as to give a unity gain after the operational amplifiers I_{14} , I_{15} and I_{16} , The resistances R_{14} , R_{16} , R_{17} and P_4 are used to remove the d.c. off set and to maintain symmetry with respect to ground for the output wave R_{SQ} , and have the value of 10 K-ohm each.



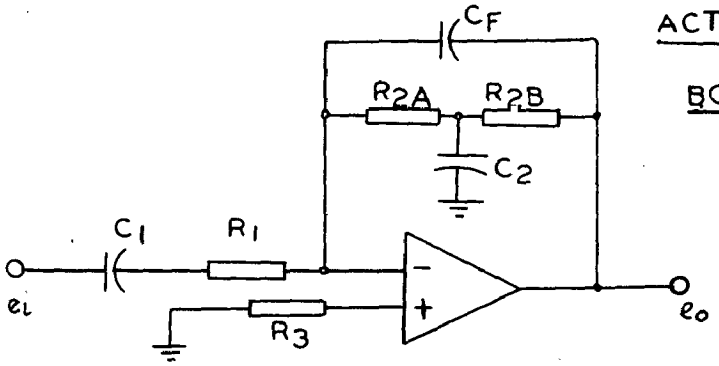
NTEGRATOR CIRCUIT

Fig. 3.8



BODE PLOTS (AMP.) INTEGRATOR

Fig. 3.9



BASIC INTEGRATOR CKT, (WIDE RANGE)

Fig. 3.10

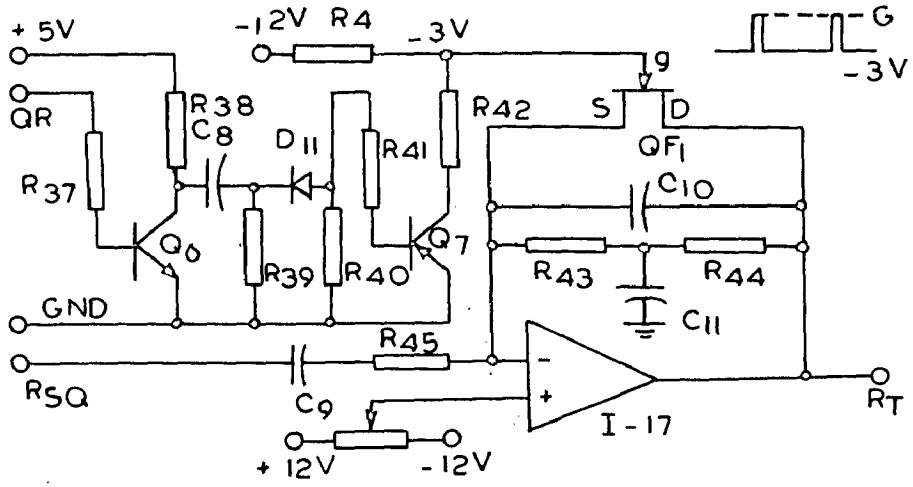


Fig. 3.11

AN INTEGRATOR
FOR
SQUARE WAVE TO TRIANGULAR WAVE CONVERSION

(CIRCUIT FOR PHASE-R)

:- IDENTICAL CIRCUITS ARE USED FOR PHASE-Y AND PHASE-B

Similar values are chosen for R_{25} , R_{27} , R_{29} , R_{31} , R_{34} , R_{36} , P_5 and P_6 , respectively for generation of Y_{SQ} and B_{SQ} . Transistors, Q_2 and Q_3 acts as inverters operating in switching mode, hence $R_{19} = R_{20} = 1K$ and $R_{21} = R_{22} = 10K$ can be chosen.

.1.4 Design of Square-wave to Trangular-wave Converter:

Basic Design Considerations:- The square wave can be converted into a triangular wave by using an analog-integrator[12]. As shown in Fig.3.8 an analog integrator integrates the signal e_1 at its input with respect to time, and employs an operational amplifier in inverting configuration. If the operational amplifier is assumed to be ideal having a gain 'A' then the equations for operation as an integrator can be derived as follows:-

$$\frac{e_1 - e_2}{R} = i \; ; \; e_2 - e_0 = \frac{1}{C}\int_0^t i\,dt = \frac{1}{RC}\int_0^t (e_1 - e_2)\,dt. \text{ and } e_2 = \frac{e_0}{A}$$

where e_1 = Input signal ; e_2 = Signal value at inverting (-) terminal of op. amp. e_0 = Output signal and R and C are the components deciding the time for integration.

since for an ideal integrator $A \to \infty$, therefore $e_2 \to 0$.

and $e_0 = -\frac{1}{RC}\cdot\int_0^t e_1\,dt$. Basically in an inverting amplifier the summing point (-) is held at a virtual ground level because of high gain of the amplifier and since no current can flow into the input terminals of the amplifier, all the current $i = e_1/R_1$ is forced to charge the capacitor and this charging voltage

appears at the output. Further the integrator circuit provides the low output impedance.

The following are the factors that must be given due consideration before designing an integrator

(I) Effect of off set voltage and bias current of the operational amplifier.

(II) Effect of voltage gain of the op. Amp.

(III) Effect of slew rate of the op. Amp.

(IV) Selection of proper components.

(I) <u>The effect of offset and bias current in an integrator</u>:-

Precisely, the output of an integrator consists of two components (the integrated signal term and the error term) and is given by

$$e_0 = \frac{1}{RC}\int e_i\,dt + \frac{1}{RC}\int V_{OS}\,dt + \frac{1}{C}\int I_B\,dt + V_{OS}$$

where V_{OS} is the offset voltage and I_B is the bias current of the operational amplifier used in the integrator circuit. Here it can be observed that :-

(i) There is a linearly increasing term which represents a ramp voltage due to the integral of the d.c. offset voltage. The polarity of this ramp voltage is determined by the polarity of input offset.

(ii) There is a d.c. component in the output termed as output offset voltage that is equal to input offset value.

(iii) The bias current that also charges the capacitor

in a ramp fashion, produces a ramp voltage at the output, similar to that produced by off-set voltage.

The overall effect of the off-set voltage and input bias current is to produce a ramp voltage that continue to increase untill the amplifier reaches a Saturation Voltage or may produce a d.c. off-set in integrated output signal. The continuous charging effect of these errors (i.e. V_{OS} and I_B) actually sets a limit on the maximum time of integration or the lowest frequency of operation. Normally a large input off-set causes saturation at the output of integrator and fails it to operate. Hence the reduction of the effect of input off-set and bias current to a minimum is most essential for satisfactory and reliable operation of an integrator, especially at low frequency.

The adverse effect due to bias current can be minimized by :-

(i) Increasing the value of capacitance and decreasing the value of resistance for a particular value of time constant RC. The lower value of R being set by current limit and loading of the input signal

(ii) The insertion of a compensating resistance between the Non-inverting input of the amplifier and the ground, equalizes the resistance of the two inputs i.e. at inverting and non-inverting inputs and thus reduces the effect of input bias current to that an off-set (differen current.

The effect of off-set that is determined by the off-set voltage of the operational amplifier employed and also on the time constant can be minimized by :-

(a) By selecting an operational amplifier having the minimum off-set voltage and temperature drift.

(b) By providing an off-set ~~vdd~~ at non-inverting input.

(c) By quenching (discharging or resetting) the capacitor every time the output crosses the ground (zero level). This technique provides a perfect and linear integration of the input signal at the lowest operating frequency. The quenching, removes any off-set present either at starting or at the time of zero level crossing and thus starts a fresh integration every cycle.

(II) Effect of Voltage Gain in an integrator:

In the design of an integrator the most important factors are the finite (closed loop) gain and the band width of the operational amplifier being used in integrator. Both of these factors make the voltage gain of the amplifier and consequently the integrator as frequency dependent, that is the gain goes on reducing as the operating frequency increases. When a constant amplitude of the integrated signal is required over the entire operating range of frequency. This problem becomes serious and require some modifications in the basic integrator circuit in order to counter act the above problem. One of the technique, that we have employed is to increase the amplitude of the input signal (i.e. square wave) proportionately as the

frequency is increased so as to maintain the amplitude of the integrated output (triangular wave) constant, irrespective of the frequency change.

The effect of voltage gain in integrator is depicted in Fig.3.9. We can observe the open loop frequency response of the amplifier is approximated by a single pole located at $1/\tau_0$ and low frequency gain A_0 . It can also be noted that the response of real integrator departs from that of ideal one, at low frequencies due to finite gain of the amplifier and at high frequencies due to finite band width of the amplifier.

(III) The Effect of Slew Rate in an Integrator:

The slew rate of an operational amplifier that is defined as the maximum rate of rise of output voltage at a step input, normally leads to a distortion of output at high frequencies. The time required for the amplifier to RESET to initial condition or starting zero voltage levels, is limited by R.C. time constant of the RESET/QUENCHING network and by the slew rate available in the closed loop circuit.

(IV) Selection of Proper Component:

In order to realise the best performance out of an integrator, the choice and selection of proper component is most important and for that following considerations are useful:-

(i) The integration time and the accuracy generally specifies the particular type of the operational amplifier to be used. For long term integration or very low frequency

(below 1 Hz to 10 KHz) chopper stabilized amplifier is the best choice, since it has a superior long term stability. For medium-length integration (say 1 KHz to 100 KHz), FET amplifiers are used because of their low bias current.

(ii) The best performance of an integrator can also be achieved by selecting a feedback capacitor with its dielectric leakage current less than the bias current of an operational amplifier. Normally, for the ultimate long term integrating accuracy Teflon or Polystyrene capacitors are used and for high speed integration Mylar or Silver-mica capacitors are used.

Design of Wide-Range Integrator:

The basic circuit of a wide frequency range analog integrator[13], that can be employed to convert square wave to a trangular wave, is shown in Fig.3.10. The design of this basic circuit is as follows:-

The value of R_1 is chosen on the basis of input bias current, the voltage drop across R_1 and to produce realistic values for C_F and C_1 . For safety let us assume R_1 = 10K.

The time constant R_2 C_F combination must be substantially larger than the R_1 C_F combination. For this reason the values of R_{2A} and R_{2B} are approximately 10 time the values of R_1= 100K.

With values of R_2 set, the value of C_2 is determined by the low frequency limit of the integrator (Freq A) as given by the equation

$$C_2 \approx (2/6.28 \times \text{Freq A})/R_{2A} \qquad (3.4)$$

Now assuming the lower frequency as

$$1 \text{ Hz}, \; C_2 = \frac{2}{6.28 \times 1} \times \frac{1}{100{,}000} = 30 \; \mu F$$

With the values of R_1 set, the value of C_F is determined by the high frequency limit of integrator (Freq C) and the gain desired at this frequency. Assuming the Freq C = 100 Hz and gain to be unity, the value of

$$C_F = \left(\frac{1}{\text{Gain} \times \text{Freq C} \times 6.28}\right) \times \frac{1}{R_1}$$

$$= \frac{1}{1 \times 100 \times 6.28} \times \frac{1}{10 \times 1000} = 0.2 \; \mu F. \qquad (3.5)$$

Again with the value of R_1 set, the value of C_1 is determined by the intermediate frequency of integrator (Freq B). Normally the frequency B is approximately one decade above Freq A. Let us assume Freq B = 10 c/s, then the value of C_1 is approximately

$$C_1 = \left(\frac{1}{6.28 \times \text{Freq B}}\right) \times \frac{1}{R_1} = \frac{1}{6.28 \times 10 \times 10{,}000} = 2 \; \mu F \qquad (3.6$$

The effect of off-set voltage and bias current discussed in section (3.14/I) can be reduced by associating with the integrator the following two additional features :-

(a) The off-set Null balance, providing a suitable nulling voltage at the non-inverting terminal of the operational amplifier, through a preset arrangement as shown in Fig.3.11.

(b) A quenching or reset circuit that quenches or reset or discharge the capacitor to ground, every cycle at the moment the output crosses the ground level. Thus any residual charge contained in the capacitor is discharged or removed every cycle. The design of a quenching circuit is described below.

The design of quenching circuit :- For this a square pulse of half the frequency of the square wave is tapped out from the dividing integrated circuit (I-10, I-11 and I-12) as shown in Fig.3.7. These square pulses Q_R , Q_Y and Q_B are inverted through transistors Q_6 , Q_6' and Q_6'' to give Q_R', Q_Y' and Q_B' that after differentiation gives the positive and negative sharp pulses at the rising and lowering edge of each wave. The positive pulses are clipped through the diodes D_{11} , D_{11}' and D_{11}'' and retains only the negative pulses. These negative pulses switches the transistors Q_7 , Q_7' and Q_7'' to generate -3 Volts to ground pulses at their collectors. Since these pulses are generated through the square pulses of half the frequency of the square waves R_{SQ} , Y_{SQ} and B_{SQ} (required to be integrated), therefore the negative to ground going pulses of very small notch width are generated exactly at the middle of the square wave input to the integrators.

These reset or quenching pulses are used to switch on the FET's Q_{F1} , Q_{F2} and Q_{F3} (2N 4393). These transistor are placed across the integrating capacitors (C_{10} , C_{10}', C_{10}'') and provides the very high impedance (≈ 1M ohm) across them, for

the complete cycle except at the point of crossing the ground level, when a sharp negative to ground going pulses are generated. These sharp pulses are applied to the gates of the field effect transistors and makes them ON (i.e. in the conduction mode) and thus discharges the capacitors momentarily. The FET's are used either in pinch off or cut-off region or in normal conduction mode. As shown in Fig.3.11, source and drain terminals are connected across the integrating capacitors, such that source is connected to the inverting point and drain at the output terminals of operational amplifiers. Since the inverting points are always maintained at ground level, hence the voltage level at the gate terminals of the FET's should be about -3V to pinch off the FET's and zero to put them in conduction mode. In pinch off condition FET's provide a high resistance across the integrating capacitors and allows the normal charging of the capacitors as per the square wave inputs.

Selection of the values of components for Quenching Circuit:-

As shown in Fig.3.11, the quenching pulse Q_R is applied to the base of Q_6 (a n-p-n transistor say DC 107) through R_{37}. This transistor acts an inverter while operating in switching mode. The resistors R_{37} and R_{38} can be conviniently choosen as 1K-ohms and 10K-ohms, respectively. The capacitor C_8 and resistance R_{39} form a differentiating circuit that produces sharp positive and negative pulses at the rising and falling edge of square wave Q_R. The inversion of Q_R through Q_6 produces negative going sharp pulse exactly at the middle of square wave

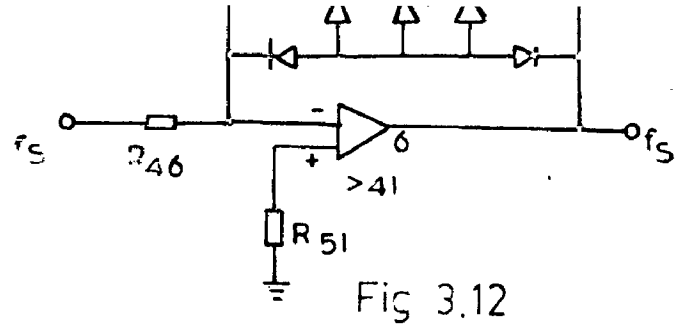
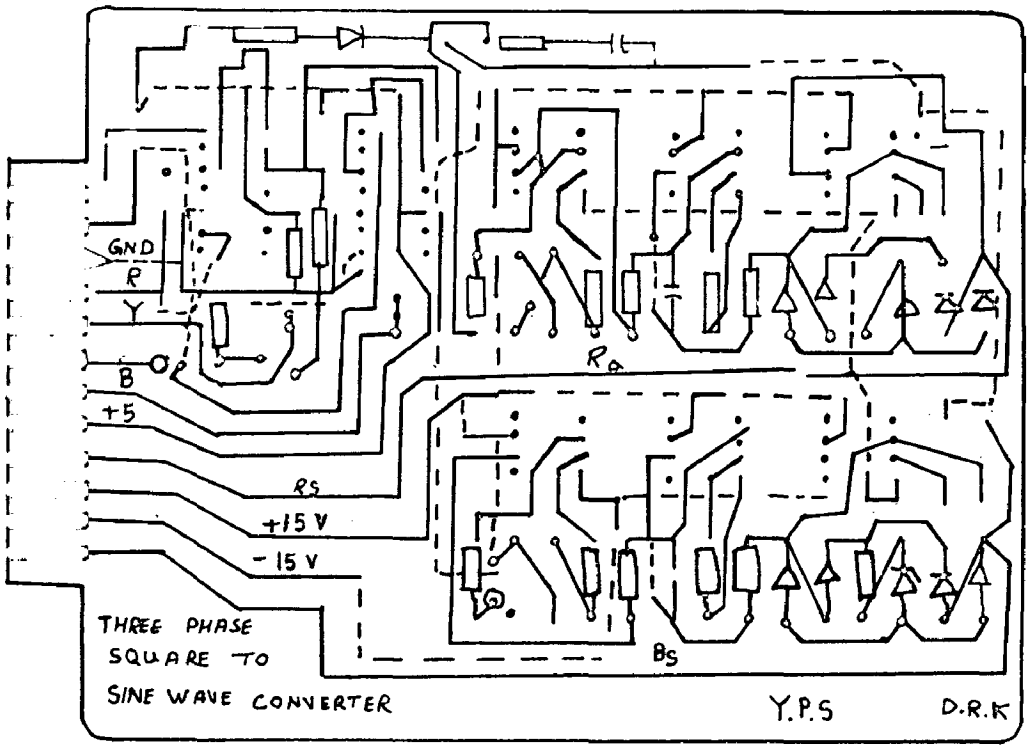


Fig 3.12



COMPONENT LAYOUT
OF
SQUARE TO TRIANGULAR TO SINE WAVE
CONVERTER CIRCUITS
Fig. 3 13

R_{SQ}. The time constant of differentiating circuit is given by $t = 0.7\ R_C$. If R_{39} = 1K and C = 1000 pf then t = 7 micro seconds. The positive going sharp pulse is clamped through D_{11} while only negative going pulse switches the p-n-p transistor Q_7(say BC 178 or SF 104). The resistances R_{42} and R_{43} are selected in such a way that a negative pulse of amplitude -3V and pulse width of about 5 micro-sec is applied at the gate of field effect transistor QF_1. The values of R_{42} and R_{43} are selected as 10K and 3.3K ohms respectively and the value of R_{41} as 1.5K-ohms that gives a proper switching of the transistor Q_7.

3.1.5 Design of Triangular to Sine Wave Converter:-

The triangular waves are converted to sine waves[14] via the circuit shown in Fig.3.12. Circuits of this type are capable of producing functions such as sine functions whose slope decreases as the input increases. The circuit relies on the values of zener voltages of the zener diodes ZD_1 , ZD_2 and ZD_3. By arranging the diodes D_1, D_2, D_3, and D_4 to form a full wave bridge rectifier a shown, the circuit will shape bipolar input voltages. The detailed operation of the circuit is as follows:-

When V_{in}(R_T, Y_T or B_T) is low, all zener diodes will be cut-off. The gain of the amplifier is therefore R_{50}/R_{46}. When the voltage across R_{50} tries to increase above VZ_1 plus 2 V_F (for two diodes), it will be clamped by ZD_1. The amplifier incremental gain will then be

$$\frac{(R_{50} \times R_{47})/(R_{50} + R_{47})}{R_{46}} \qquad (3.7)$$

As V_{in} increases further the voltage will be clamped successively by ZD_2 and finally ZD_3. The final incremental gain is

$$\frac{1}{R_{46}} \times \frac{\left(\frac{R_{47} \cdot R_{48} \cdot R_{49}}{R_{47}R_{48} + R_{48}R_{49} + R_{49}R_{47}}\right) \times R_{50}}{\frac{R_{47}R_{48}R_{49}}{R_{47}R_{48} + R_{48}R_{49} + R_{49}R_{47}}} \qquad (3.8)$$

It is stated above in this section that initially when non of the zener diode conducts the gain is given by R_{50}/R_{46}. Practically the amplitude of triangular wave was found to be constant at 2.5 Volts peak to peak. Now in order to have the maximum amplitude of output to be limited to 24 Volts peak to peak, so that the zener of maximum voltage 8.2V could be regulated, a gain of approximately 10 is required. Thus if we select the input resistance R_{46} = 10K-ohms, the value of R_{50} comes out to be 100K approximately. Further, the value of R_{47} = 150K-ohms, R_{48} = 68K ohms and R_{49} = 33K-ohms are chosen to regulate the zeners ZD_1 = 3.2 Volts, ZD_2 = 6.8 Volts and ZD_3 = 9.2 Volts.

The voltage across R_{50} rises with a slope determined by the gain R_{50}/R_{46} = 10. When this voltage rises to such a level that zener ZD_1 is clamped then the slope is given by the

$$\text{gain} = \frac{(R_{50} \times R_{47})/(R_{50} + R_{47})}{R_{46}} = \frac{100 \times 150}{250} \times \frac{1}{10} = 6$$

Again when ZD_2 conducts the slope is determined by the gain given by:-

$$G_3 = \frac{1}{R_{36}}\left[\frac{R_{50} \times (R_{37} \times R_{38})}{(R_{37} \times R_{38}) + R_{50} \times (R_{37} + R_{38})}\right]$$

$$= \frac{1}{10}\left[\frac{100 \times \frac{150 \times 68}{218}}{100 + \frac{150 \times 68}{218}}\right] \approx \frac{1}{10}\left[\frac{150 \times 50}{150}\right] = 3.5 \text{ (Approx.)}$$

And finally when ZD_3 conducts, the slope is determined by the gain given by equation

(3.3) as $G_4 = \frac{1}{10}\left[\frac{100 \times 150 \times 68 \times 33}{150 \times 68 \times 68 \times 33 + 33 \times 150 \times 68}\right]$

$$100 + \frac{150 \times 68 \times 33}{150 \times 68 + 68 \times 33 + 33 \times 150}$$

$$= \frac{1}{10}\left[\frac{100 \times 15}{100 + 15}\right] = 1.5 \text{ (Approx.)}$$

This circuit is very simple but requires a constant amplitude triangular wave, however it can accept any frequency. The sine wave out put contains a maximum of 5 % total harmonics and have the amplitude of 10 Volts peak to peak.

Three such identical circuits are used to generate three phase reference sine waves R_3, Y_3 and B_3. Fig.3.13 shows the component layout for square wave to triangular wave and triangular wave to sine wave for Phase R and Phase Y. Fig.3.14 depicts the wave diagrams for 3-step sequential pulses to square wave; square wave to triangular wave and triangular wave to sine wave conversion.

3.3 Amplitude Control of 3-Phase Reference Sine wave With a d.c. Control Signal

(a) Design Aspects for Amplitude Control of Three Phase Reference Sine Waves-

As described in sections 3.1.1 to 3.1.5, a set of three phase reference sine waves are generated with their amplitude maintained constant and frequency varying linearly with a d.c. control signal V_1. Now, it is required to control their amplitude with another d.c. signal V_2. Any circuitry or device used for amplitude control must satisfy the following requirement

(a) The amplitude control should be linear with respect to control signal.

(b) It should not provide any waveform distortion or asymmetry in the controlled output waveform.

(c) It should not provide any off-set in the output.

(d) Input loading should be minimum.

(e) Amplitude should be controllable from 0 to 20 volts peak to peak.

(f) Amplitude control action should be frequency independent.

The amplitude control of the reference sine wave with the help of a d.c. signal can be obtained by the following two techniques-

[A] Use of Field Effect Transistor as a Variable resistor.

[B] Use of Analog Multipliers.

3.3.1 Amplitude Control of Sine Wave employing F.E.T as a Variable Resistor

The field effect transistor can be used as a voltage controlled resistor[19]. This fact is utilized in this technique

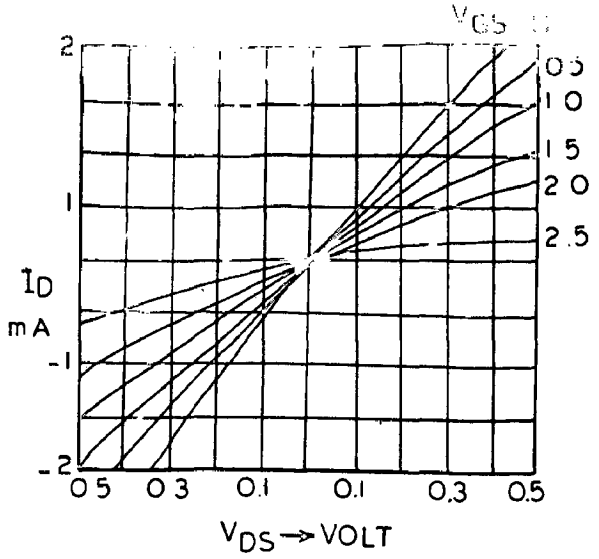


Fig. 3.15

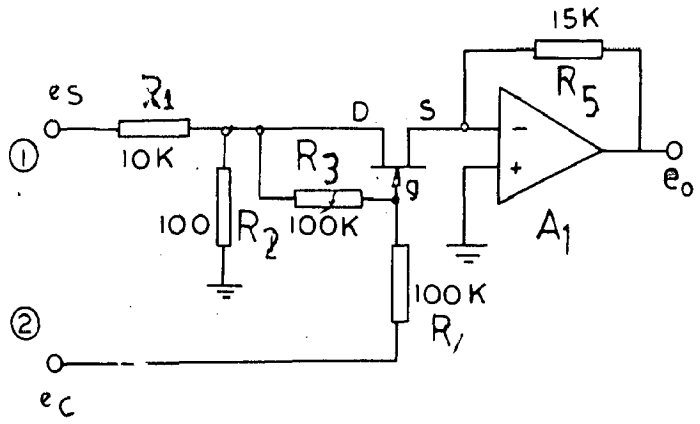


Fig. 3.17

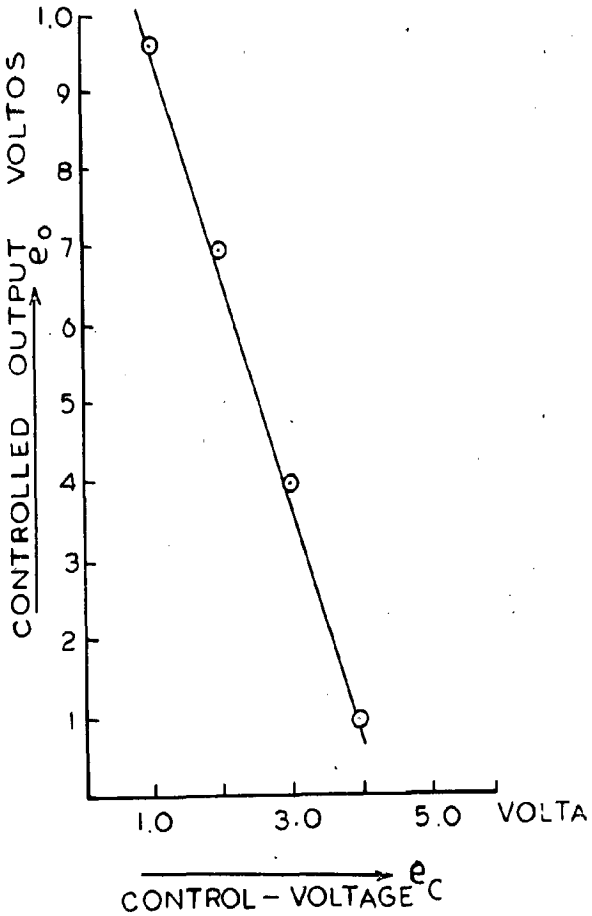
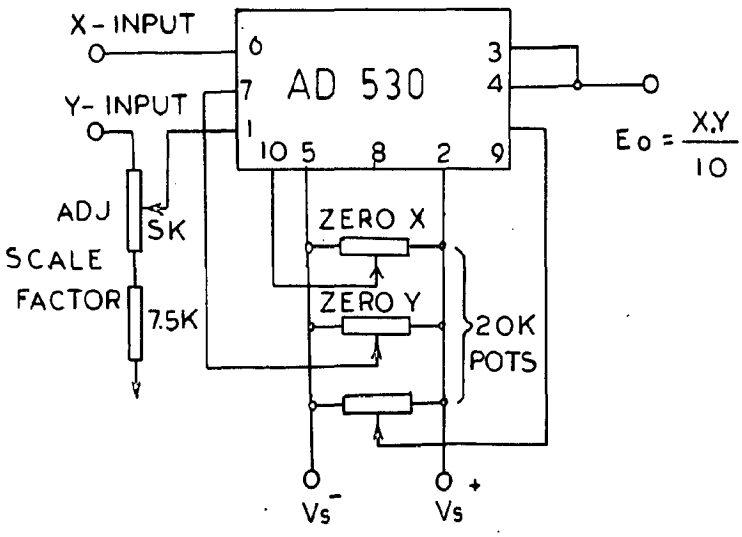


Fig. 3.18



ANALOG - MULTIPLIER

Fig. 3.19

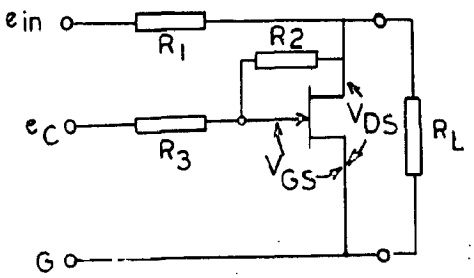


Fig. 3.13

If a very small voltage V_{DS} of the order of 0.5 Volts is applied across the Drain to Source terminals of the FET, then the channel resistance (i.e. R_{DS}) can be controlled by a control signal V_{GS} applied across the Gate to source terminals. Since the F.E.T act as a voltage controlled resistance only for very small values (approaching to origin) of V_{DS} and V_{GS}, hence this operation is also termed as operation in ohmic region or region of origin. Fig.3.15 depicts the characteristic of a F.E.T in the ohmic (near zero) region. Here it can be observedthat :-

(i) There is a zero off-set voltage i.e. $I_D = 0$ for $V_{DS} = 0$

(ii) For small values of V_{DS}, as well as V_{GS}; the characteristics are reasonably linear.

(iii) The resistance of channel ($R_{DS} = V_{DS}/I_D$) can be controlled by the variation of V_{GS}.

Actually the value of R_{DS} for $V_{GS} = 0$ and $V_{DS} = 0$ is called the $R_{DS}(ON)$ and sets a minimum value of resistance that FET can offer. The practical values may range from 1 to 10 ohms or at the most 100 ohm for certain typical FET's.

The FET used as a variable resistor should have symmetrical geometry (i.e. interchangable source and drain) in order to have operation in I and III quadrants as shown in Fig.3.15, since we have to apply an alternating voltage across the drain to source terminals and d.c. control signal V_2 across gate to source in order to control the amplitude of the sine wave, it is therefore essential for the F.E.T. to be used, to have a geometrical symmetrical geometry.

Theoretically, the drain current I_D, in the ohmic region is given by

$$I_D = I_{DSS}\left[\left(1 - \frac{V_{DS}}{V_p}\right)^2 - \left(1 - \frac{V_{GS} - V_{DS}}{V_p}\right)^2\right]$$

$$= \frac{2I_{DSS}V_{DS}}{V_p^2}\left[V_{GS} - V_p - \frac{V_{DS}}{2}\right] \qquad (3.9)$$

where V_p = pinch off voltage (V_{GS} at which channel opens and offers the maximum possible resistance across the drain to source terminal).

Because of the presence of $\frac{V_{DS}}{2}$ term the relation between I_D and V_{DS} is not linear unless V_{DS} is small as compared with $V_{GS} - V_p = V_{DSO}$.

The channel conductance G_{DS} is given by

$$G_{DS} = \frac{1}{R_{DS}} = \frac{I_D}{V_{DS}} = \frac{2I_{DSS}}{V_p^2}\left[V_{GS} - V_p - \frac{V_{DS}}{2}\right] \qquad (3.10)$$

and $R_{DS}(On) = -V_p/2\ I_{DSS}$ (for $V_{GS} = V_{DS} = 0$).

It should be noted that however R_{DS} can be varied over a wide range by changing V_{GS}, but as V_{GS} approaches V_p, the rate of change of R_{DS} is very rapid and control is difficult. The satisfactory and reasonable range of control is 10:1. The variation of r_{DS} is linear with V_{GS}, from $R_{DS}(On)$ to about 4 times of this value.

Further, the variation of R_{DS} could be achieved by the variation of V_{DS} but large variation of V_{DS} causes distortion

of the signal. A reasonable linearity for a large variation of V_{DS}, requires larger V_p, that usually means higher I_{DSS} and lower $R_{DS}(on)$.

The reduction in non-linearity and signal distortion can be best accomplished by a negative feedback arrangement. From the equation(3.8) it can be seen that if a signal of amplitude $V_{ds}/2$ is fed-back to the gate then the $V_{ds}/2$ term is cancelled and $I_D \propto V_{DS}$; G_{DS} = constant.

The Fig.3.16 above an arrangement in which a negative feedback is employed to obtain a voltage controlled attenuator. attenuator It should be noted here that R_2 and R_3 are large compared with the other resistors R_1, R_2 or $R_{DS}(on)$. Further if $R_2 = R_3$, a signal $V_{ds}/2$ is fed-back in series with control voltage V_c, such that $V_{GS} = e_0 + V_{ds}/2$ and thus we can get from equations (3.9) and (3.10) ;

$$I_D = \frac{2 I_{DSS}}{V_p^2} V_{DS}(e_0 - V_p) \text{ and } G_{DS} = \frac{2 I_{DSS}}{V_p^2} (e_0 - V_p) .$$

Based up on the above discussion, a circuit as shown Fig.3.17, was developed for the control of the amplitude of the sine wave with a control signal e_0, applied at terminal (2) i.e. the gate of the F.E.T, Q_{FT}. In order to have a linear control over a wide range of amplitude of the output signal the following points should be given due consideration prior to design the circuit:-

(a) V_{DS} should be small, approx = $0.5V_p$ so that field effect transistor operates near zero (in ohmic) region.

(b) V_{GS} should also be small ≃ 20 % of V_{GS} (pinch off voltage).

(c) Transistor should be of large pinch off voltage (e.g. -37 for DN - 11).

(d) For the identical circuits that are required for the control of magnitudes of three phase sine waves, the field effect transistors must have the matched characteristics.

(e) Negative feedback as explained above must be provided in order to improve linearity and reduce signal distortion

As shown in Fig.3.17 ; the resistances R_1 and R_2 provide a voltage of about 0.7V p.p. with an input signal of 10V peak to peak. Since drain to source terminals can sustain bi-directional signals, the sine wave input is applied to the terminal(1). Resistances R_3 and R_4 provides the necessary negative feedback in order to achieve a linear control and a suitable gain is obtained by the use of operational amplifier A_1.

The circuit as described above was found to be sufficient linear as shown in figure 3.18. But, when three such identical circuits were used to control the amplitudes of three phase reference sine waves, employing a common control signal (e_c), it was observed practically that the amplitudes of the controlled sine waves were different for a given control signal and thus there was an error in the simultaneous control of amplitude with a common control signal. The reason might be the difference the characteristics of the F.E.T's employed and the tolerances of the

components used in the circuit. Hence the above circuit as shown in Fig.3.10 can not recommended for the simultaneous amplitude control of three-phase sine wave. However if the amplitude of each phase is to be controlled independently, this scheme, is still most suitable, simple and economical.

3.2.2 Analog Multipliers for Amplitude Control of Three Phase Reference Sine Waves:-

A precise and accurate amplitude control of three phase reference sine waves (R_0, Y_0 and B_0) with a control signal (V_2); can be obtained by employing three analog multipliers, one, for each phase. The analog-multipliers (upto 0.5 % accuracy) are available in integrated circuit chip form. The following are the analog-multiplier chips, recommended for amplitude control:-

Make	Type No.	Function	Description (Accuracy Full Scale)
Motorola	MC 1594	4 Quadrant	0.5 % ; 50 MHz
-do-	MC 1595	4 Quadrant	1.0 %
Analog-Devices	AD 530	4 Quadrant	0.5 % ; 750 MHz
-do-	AD 531	4 Quadrant	1.0 % ; 750 MHz
-do-	AD 532	4 Quadrant	0.3 % ; Fully trimmed
Fairchild	uA 795	Low Cost Fairchild multiplier.	
N.S.C.	CA 3060/3080.	Variable Trans-conductance multiplier (N.S.C.)	
Solitron Philbrick	4494	4 Quadrant	± 0.5 % , 100 MHz
	4495	-do-	± 0.25 % , 100 MHz
	4450 (General Purpose)	-do-	± 1 % ; 100 MHz
	4452 (Accuracy)	-do-	± 2 % ; 50 MHz

The most commonly used chips are AD 530 and Motorola MC1496, since they are very simple to operate and cheap. The Fig.3.12 shows a testing circuit for AD 530.

3.3 Pulse Width Modulation of Sine Wave with a Triangular Wave

The pulse width modulation technique (PWM) is based on the production of an output voltage consisting of constant amplitude, variable width pulses, which when supplied to an inductive load, produce a current corresponding to a modified version of the voltage waveform. The method used to vary the pulse width is based on the comparision of the signal with a high frequency triangular wave. The cross-over points of the sine wave and the triangular wave are used to generate the pulses required to switch the transistors. The ratio of triangular wave (carrier wave) to sine wave (reference) is termed as Modulation Ratio. The modulation ratio is required to be as high as possible so that the sine wave may be reproduced at the output with less distortion and low harmonic contents. However the maximum Modulation Ratio depends upon the following factors:-

(1) The maximum switching frequency at which the switching device can operate safely and reliably.

(2) The accuracy and the frequency limit of the comparator.

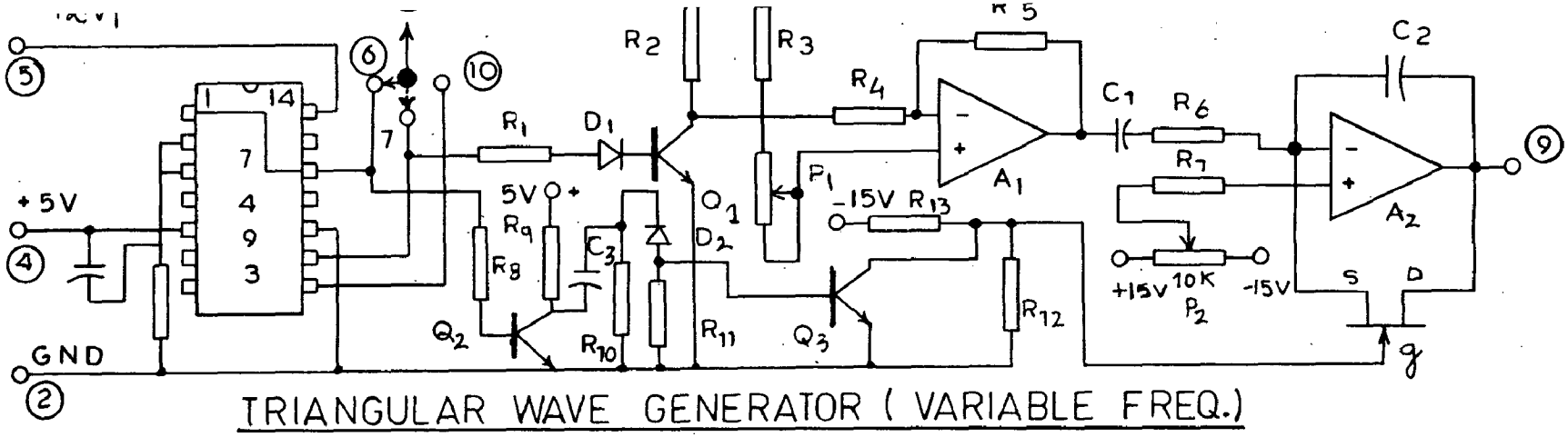
(3) The performance of pulse isolation circuit, that determine the minimum notch width of the pulse that can be isolated faithfully without any distortion.

3.3.1 For pulse width modulation, two basic schemes are possible ; such as :- (1) The fixed Modulation Ratio (2) Variable Modulation Ratio.

(i) Fixed Modulation Ratio :- In this case the frequency ratio of triangular wave to sine wave is maintained fixed by taking the square pulses from the output of VFC after a suitable division as shown in Block Diagram Fig.3.1. The possible ratios are $f_T/f_s = 6$; 12 and 24. This ratio remains fixed as the frequency of reference sine wave is changed with a control signal V_1. Here the frequency of the triangular wave varies proportionately with the frequency of sine wave.

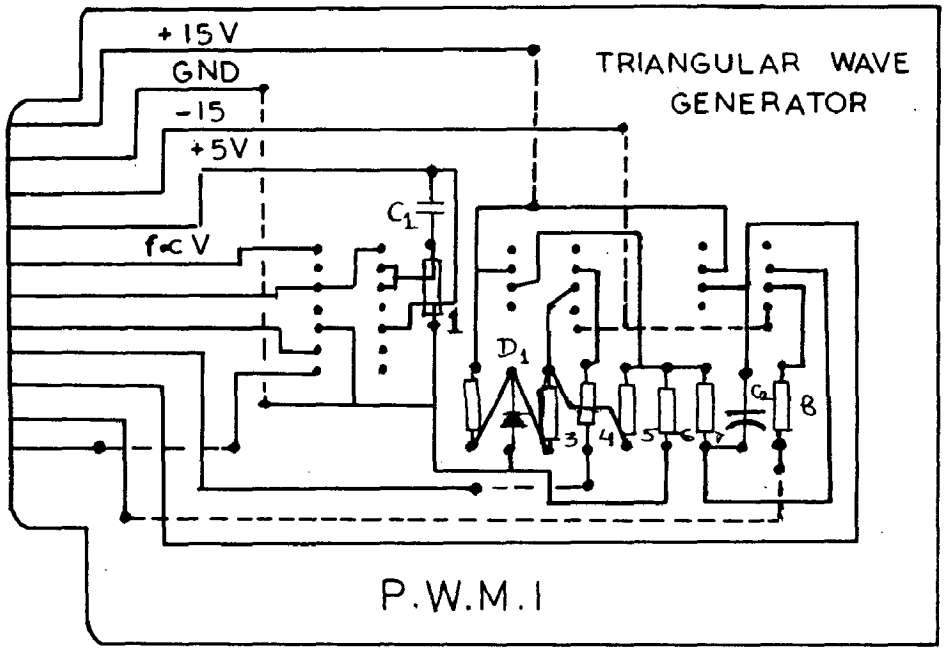
(ii) Variable Modulation Ratio :- In this case the frequency of the triangular wave remains constant, while the sine wave reference wave frequency varies. Thus the modulation ratio vary with the variation of the fundamental frequency sine wave. For example if we keep the triangular wave at 1 KHz and vary the sine wave frequency from 50 Hz to 5 Hz the modulation ratio will vary from 20 to 200. The basic advantage of this scheme is that the low order harmonics even upto 20 or more are drastically reduced and the performance of the P.W.M. inverter (employing this technique) feed induction motor is sufficiently improved, specially at low speeds.

3.3.2 Design of Triangular Wave Generators :- As explained in 3.3.1(1), for a fixed modulation ratio scheme, a variable frequency triangular wave of constant amplitude is required to be generated in such a way that the frequency of this triangular wave bears a constant ratio with the frequency of sine wave generated as shown in block diagram Fig.3.1. The triangular wave can be



TRIANGULAR WAVE GENERATOR (VARIABLE FREQ.)

(CIRCUIT DIAGRAM)



COMPONENT LAYOUT

Fig - 3.20

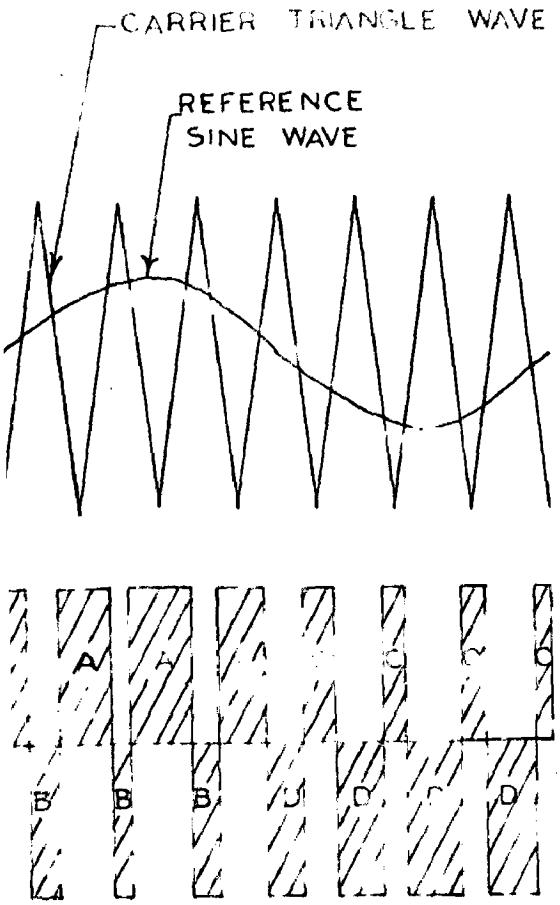
PIN	DETAILS
1	+15V
2	GND
3	-15V
4	+5V
5	f∝V
6	f_T/f_S = 6
7	f_T/f_S =12
8	Freo Ratio Selector
9	Triangle Wave
10	f_T/f_S= 24

generated by a square wave to triangular wave converter (an analog integrator). The square pulses (that are converted to square wave through a square pulse to square wave generator) are derived from pin number 12 of divider I-3. The divider I_3 divide, by two, the V.F.C. output at its pin No.12, as shown in Fig.3.20.

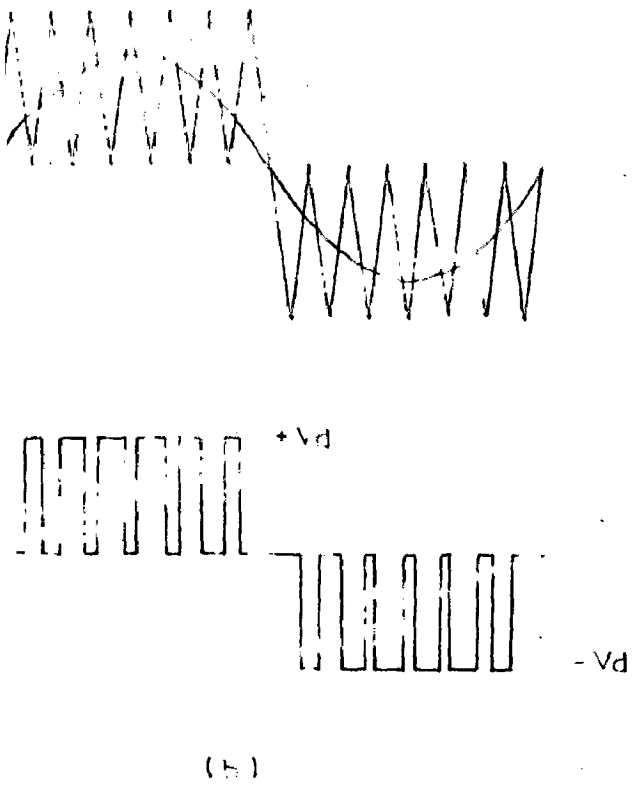
The design of square pulse to square wave converter and square wave to triangular wave converter is already discussed in sections 3.1.3 and 3.1.4 respectively and the same values components are used for these two converters as shown in Fig.3.20 except for the analog-integrator time constant i.e. R_6 and R_2.

.3.3 Basic Pulse Width Modulation Circuit:- There are two main methods for pulse width modulation using triangular carrier waveforms[16]. The principal features of these two methods and the associated load terminal voltages are illustrated in Fig.3.21. In the 1st method the load terminal voltage is switched between $+V_d$ and $-V_d$. In the second method this voltage is switched either between $+V_d$ to zero or between $-V_d$ to zero, according to current directio Periods of zero load voltages are achieved by short circuiting the load through one diode and one transistor. The second method is more complex but the switching frequency harmonics appearing in the output are much reduced.

Mode of operation:- The first method described above is employed in our scheme not only to minimize control circuit complexity but also to avoid circulating currents induced by triansformer action in the three-phase machine load. Further, with the

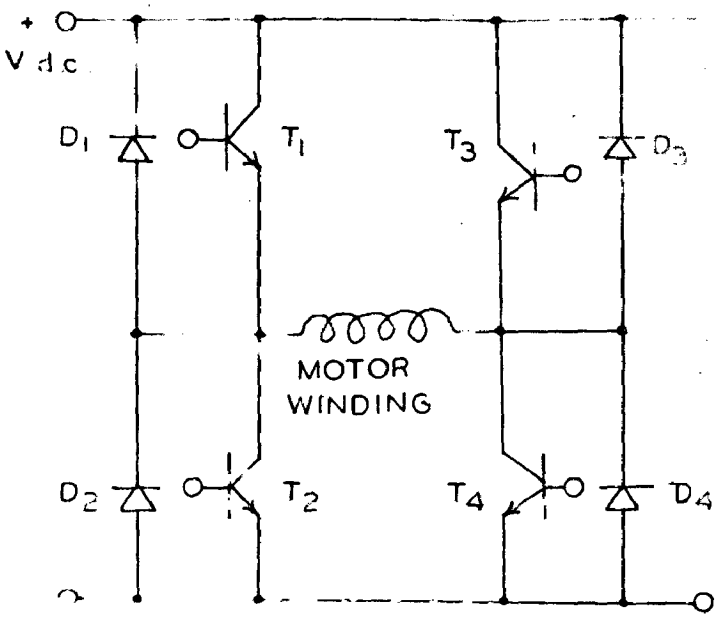


(a)



(b)

Fig 3.21



BASIC CIRCUIT OF SINGLE PHAS BRIDGE INVERTER

Fig 3.22

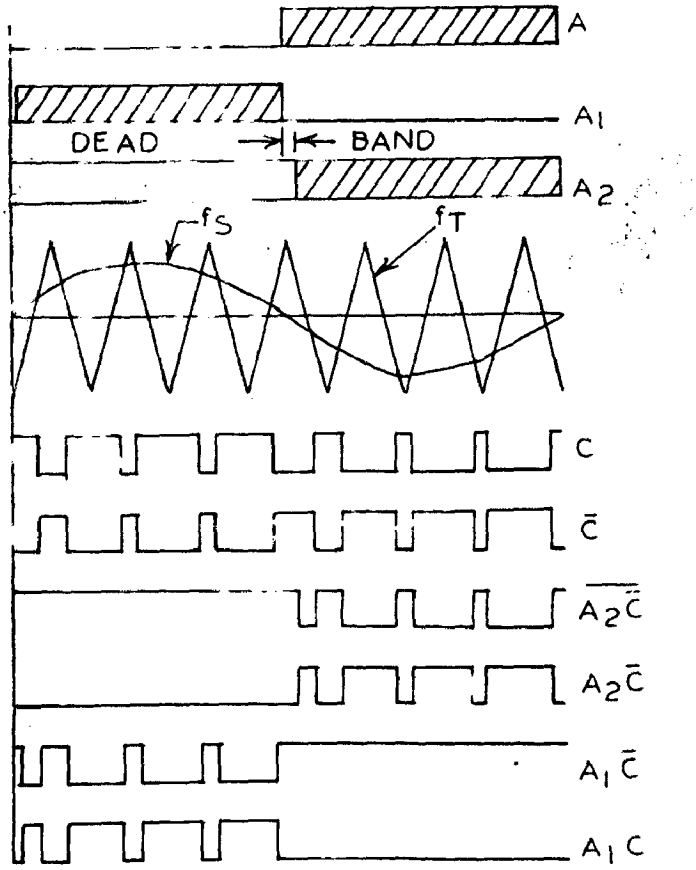
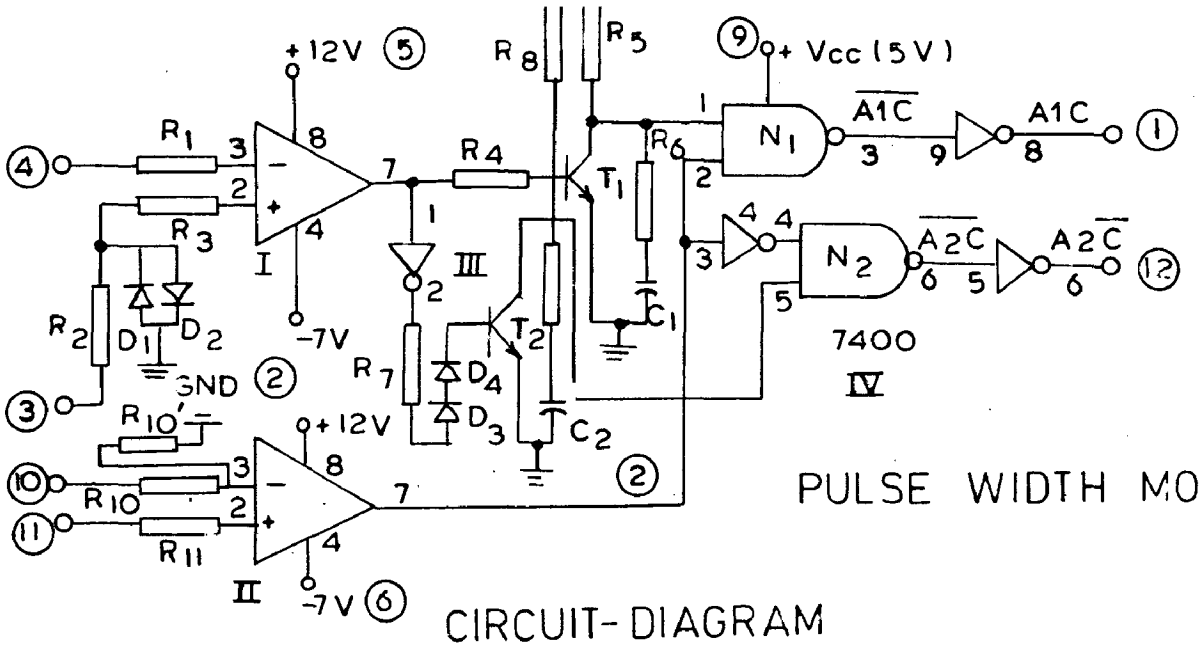


Fig 3.24

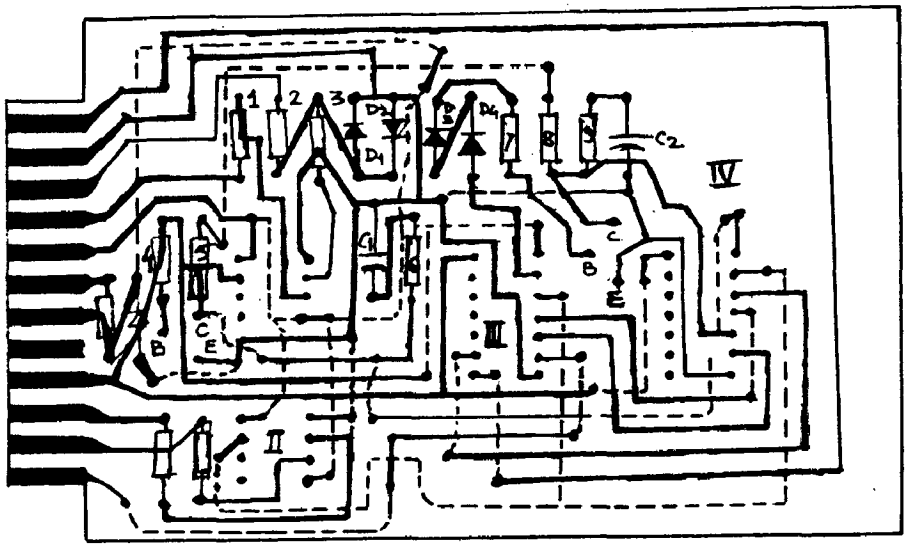
carrier frequency employed the output components at carrier frequency and above are negligible so that there is no real advantage using the more complex system. The operation of the modulation circuit may be described in general form as follows:- Referring to Fig. 3.21-a and 3.22, transistor T_1 and T_4 are driven during periods B and C, the current is carried by T_1 and T_4 during A periods, by diodes D_2 and D_3 during B periods, by D_1 and D_4 during C periods and by T_3 and T_2 during D periods. although there is no need to drive any transistor during the B and C periods, if this is done it enables simpler switching logic to be employed and allows current reversal to occur without deformation of the current waveforms.

In thyristor inverters it is often permissible to trigger a switch before the other switch in the same arm is completely commutated. This is unacceptable in transistor inverters. To avoid short circuiting the supply it is necessary to provide a dead band during which neither transistor in any given arm conducts. The duration of this dead band must exceed the sum of the transistor storage and fall times (≈ 4 μ.S) and must be included in each period (≈ 50 μ.S) of the switching frequency. During these safety intervals the current flows through the diodes and the voltage of reverse polarity is applied across the load. It obvious that short pulses would be more effected than the longer pulses and some waveform distortion would occur. To minimize this distortion the shortest possible dead band-period must be employed.



PULSE WIDTH MODULATION CIRCUIT

CIRCUIT-DIAGRAM



COMPOUENT LAYOUT

Fig. 3.23

PIN	CODE
1	A1C
2	GND
3	REF. VOLTAGE
4	CURRENT SIGNAL
5	+12 V
6	-12V
7	- 7 V
8	-
9	+5 V
10	CARRIER
11	REF_SINE WAVE
12	$A_2\bar{C}$

To overcome the difficulties mentioned above, a modified switching mode is adopted[16]. In this mode during period A, transistors T_1 and T_4 are driven as before. During periods B and C, all transistors are in "off" state and during D period transistors T_3 and T_2 are driven. With this system it is essential to provide logical signals allowing either T_1 and T_4 or T_3 and T_2 to be driven. These signals depends on the direction of load current flow, rather than upon the signal voltage. If the voltage signal is used in high power factor loads, a reasonable current waveform will be obtained. For low power factor load a noticeable deformation occurs when the voltage and current direction are opposed. Assume T_1 and T_4 have been conducting and drive is now transferred to T_3 and T_2. For correct operation T_3 and T_2 should conduct during MARK and D_2 and D_1 during SPACE. With a lagging power factor, the current will flow via D_2, D_3, just after cross-over and the output waveform is therefore not controlled. The modulator circuit that we have used overcome this difficulty by employing a combination of voltage and output current current control. The circuit diagram of the Pulse Width Modulator circuit is shown in Fig.3.23 and the waveform at the different points in the circuit are shown in Fig.3.24.

The operation of the modulator circuit may be explained as follows. The voltage reference signal is compared with the carrier triangular wave by the comparator IC (710)-I- , providing a logic output signal C. A second signal A is derived from the combination of reference voltage the load current signal. A delayed inverted version of signal A is formed by means of

(1) High speed-optical isolators.

(2) Pulse Transformers employing high frequency Modulation/ Demodulation Technique.

Optical Isolator:- This is the most commonly used technique in which a light emitting source and photo sensing device is coupled together to form an opto-isolation. The signals produce corresponding currents in the light emitting device and the intensity of light is sensed through a photo transistor which deliver the current as an exact replica of input signal. Normally optical-isolator is available as a composite device and are cheaply available.

The basic advantage of optical isolator are:-

(a) A high speed isolation (upto 10 K c/s or more) is possible.

(b) Isolation is perfect (of the order of several hundred Mega-ohms).

However there are few limitation of using these devices:-

(1) The isolators are quite sensitive spurious noises of high frequency. Hence require the noise free signals. Also the supply transients gives spurious switching pulses.

(2) The output signal generated are very weak in strength and require sufficient current amplification.

Pulse Transformer Type Isolators:- In this case the pulse transformers capable of operating at high frequencies say upto 100 K c/s or more employing ferrite cores are used to transmitt the width modulated pulses and to provide proper circuit isolatio

Q_1, Q_3 and C_1. A delayed uninverted version A_2 is produced by means of Q_2, R_4 and C_2. These signals and the signal C are combined in gates N_1 and N_2 to produce the required drive signals A_1C and $A_2\overline{C}$ which ultimately control the power units T_1, T_4 and T_3, T_2 respectively. This circuit thus allows control by the current feedback signal when the magnitude of current exceeds threshold (0.4A) and control by the voltage signal at all lower current levels.

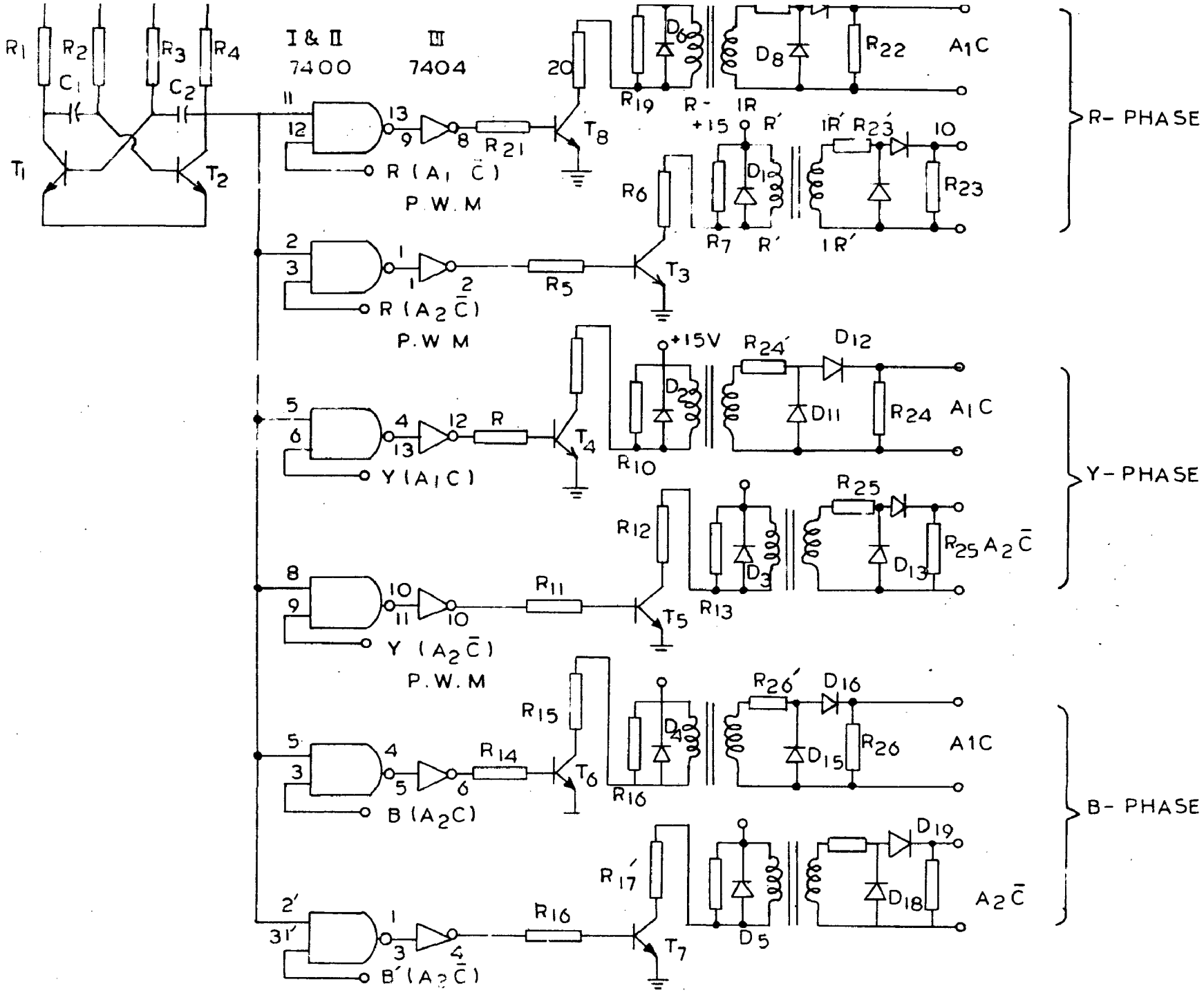
3.4.0 Circuit Isolation:- In pulse width modulation, as discussed in section (3.3.3), the width modulated pulses A_1C and $A_2\overline{C}$ (Fig.3.24) are generated to switch the power transistors in Power Control Unit. These pulses can not be fed directly to switch the transistors because of the following two reasons :-

(a) The pulses are generated through a low voltage ($\pm$ 15V and 5VDC) system, while the power control unit is operating at high voltage, hence circuit isolation is necessary.

(b) The pulses to the transistors are to be fed with a correct polarity. Also as per circuit configuration it is most essential to isolate the pulses fed to individual transistors.

Hence it is quite evident, that the pulse width modulated signals must be fed to a high speed isolator which provides the necessary control isolation between logic circuits and power inverter, with a faithful reproduction of exact wave shape (with minimum distortion).

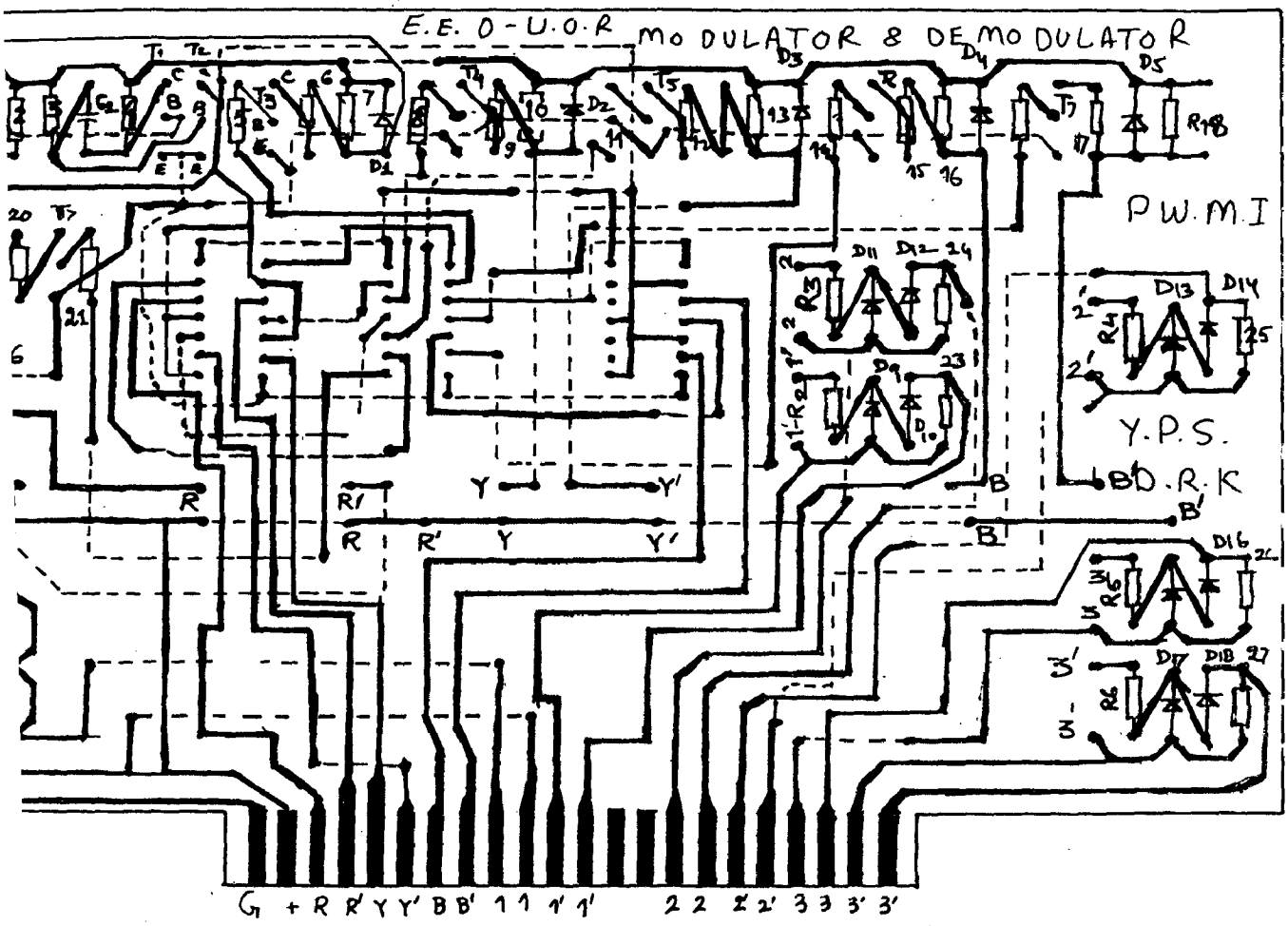
There are two alternative choice for pulse isolators:-


R1
R2
R3
R4
C1
C2
T1
T2
I & II
7400
III
7404
11
12
13
9
8
R21
T8
20
R19
D6
D8
R22
A1C
R- IR
+15
R'
1R'
R23'
10
R23
R6
D10
R7
R'
1R'
R (A1 C̄)
P.W.M
2
3
1
1
2
R5
T3
R (A2 C̄)
P.W M
+15V
R24'
D12
5
6
4
13
12
R
T4
D9
R10
D11
R24
A1C
Y (A1C)
R25
R12
D3
R25 A2 C̄
D13
R13
8
9
10
11
10
R11
T5
Y (A2 C̄)
P.W.M
R15
R26'
D16
D4
5
3
4
5
6
R14
T6
R16
D15
R26
A1C
B (A2C)
R17'
D19
D18
A2 C̄
2'
31'
1
3
4
R16
T7
D5
B' (A2 C̄)
R- PHASE
Y- PHASE
B- PHASE

Here the width modulated pulse required to be transferred are modulated by a high frequency say 40 K c/s. These high frequency modulated pulses are fed to pulse transformers that transfer the signals at the secondary, at which these signals are demodulated i.e. the high frequency component being filtered out, giving there by the exact replica of input width modulated pulses. In this case the output is of sufficient strength and require less current amplification as compared to optoisolator but the speed of operation is limited because of demodulator circuit. However the speed of operation can be increased by using a higher carrier modulating frequency say of the order of 100 K c/s or more and also improving the demodulator circuit.

The basic circuit diagram employing pulse-transformer type isolation is depicted in Fig.3.25. There are six pulse transformers are used to transfer the width modulated pulse of each half cycle of the three phases. The simple free running multivibrator is used to generate a 40 K c/s carrier square wave. The width modulated pulses are gated with high frequency carrier through NAND gates and inverters. These h.f. modulated pulses are fed to pulse transformers through switching transistors. Each pulse-transformer is having two windings in order to provide isolated driving pulses to individual transistors operating at a time. The values of resistance and capacitance in the demodulating circuit are so chosen to avoid any waveform deformation and to provide complete demodulation. The pulse transformers are designed at maximum operating (modulating) frequency that is

COMPONENTS	LIST
I C S	I & II = 7400, III = 7404
TRANSISTORS	T_1, T_2 = 66104 T_3 To T_8 = SL100
DIODES	D_1 to D_{18} OE 1001
CAPACITOR	$C_1 = C_2$ = 1500 bf C_3 to C_5 = 0·1 MF
RESISTANCES	$R_1 = R_4$ = 1K ; $R_2 = R_3$ = 33K $R_5 = R_8 = R_{11} = R_{14} = R_{16}$ = 1K $R_6 =$ $R_9 = R_{12} = R_{15} = R_{17} = R_{20}$ = 82Ω (1W) $R_7 = R_{10} = R_{13} = R_{16} = R_{18} = R_{19}$ = 15Ω R_{22} to R_{27} = 500Ω



PONENT LAYOUT OF CIRCUIT ISOLATION SCHEME

Fig 3 26

choosen to be 40 K Hz and the voltage levels of the signals appearing across the primary windings of the pulse transformers that is 12 Volts, magnitude.

It is clear from the waveforms of modulating circuit Fig.3.24 that the outputs A_1C and $A_2\bar{C}$ represent the width modulated pulses for each half of a cycle and for proper operation of the interfer are to be supplied in a isolated way. Hence for each phase two pulse transformers are required and thus in all six-pulse transformers are needed. Further since each transistor in a phase (T_1 to T_4) need pulses of positive polarity with respect to the emitter to base and also to be applied in an isolated way, the pulse transformers should have two secondary windings for a particular output train of pulses A_1C or $A_2\bar{C}$.

The complete circuit diagram and the component layout are shown in Fig.3.25 and Fig.3.26 respectively.

3.4.1 Design of Pulse Transformer:- Pulse transformer is basically used to interface between low power, sensitive control circuits and high voltage, high power circuits and usually need a high interwinding dielectric strength. The primary requirement of a pulse transformer is the efficiency and reliable and faithful transmission of pulses applied to it.

Factors Effecting the Pulse Transformer Design :-

(1) Primary magnetizing inductance should be high enough so that the magnetizing current is low in comparision with pulse current during pulse time. This can be achieved by using high permeability material for core.

(2) Core saturation must be avoided.

(3) Coupling between the primary and secondary circuit should be tight. And the insulation between the windings should be adequate for the application.

(4) Usually interwinding capacitance is in significant but it may be a path of undesirable stray signals at high frequencies.

Selection of Core Material : In principle, when an electric current flows through a conductor a magnetic potential is established and the magnetomotive force that have their source in electric currents and links with the magnetic circuit in the form of a coil is given by $F_m = N.I$, where N = NO of turns and I = flow of current and magnetic potential $H = F_m/l$ (Amp.turns/meter). This magnetizing force causes a magnetic field to surround the current and the magnetic flux density B is given by $B = \mu H$. where μ = permeability of the magnetic material.

1st Criterion for the selection of μ :- The value of μ of the magnetic material is of importance in pulse transformer design and normal values are (i) 5000 for ferrites (ii) 10,000 - 20,000 for silicon-steels.

The permeability may however vary with the flux density 'B', that may vary some times linearly or some times inversly with the flux density. The effect of this non-linearity can be reduced by inclusion of an air gap in the magnetic circuit.

2nd Criterion is the Selection of 'B' : It is given as

Ferrites Saturates at 0.3 to 0.5 web / Sq. meter.

Nickel Iron at 0.6 to 0.8 web / Sq. meter.

Silicon Steel at 1.2 to 1.4 web / Sq. meter.

3rd Criterion is the Magnetic Material Loss : This is also an important consideration in the choice of material for a transformer core. Core loss consists of in the form of core heating. This heating in addition to the winding copper losses determines the temperature rise of T_X and this is a determining factor in the life of transformer.

In pulse transformers SOFT ferrites are used, which retains its magnetism so long the influencing field exists and does not retain it as it is removed. Central Electronic Limited (C E L), India, is manufacturing a. variety of grades of ferrites for various applications. Out of these we have selected Toroid Cores of size ($\overset{I.D. \times O.D. \times thickness}{17.5 \times 35 \times 10}$) m.m. and material grade HP_4. Since the saturation flux density is 0.35 web/m^2. Let us assume an operating flux density to be 0.1 web/m^2. Now, depending upon this flux density the number of turns can be calculated from the relation

$$E = 4.44\ fN.\phi = 4.44.fN\ B.A.$$

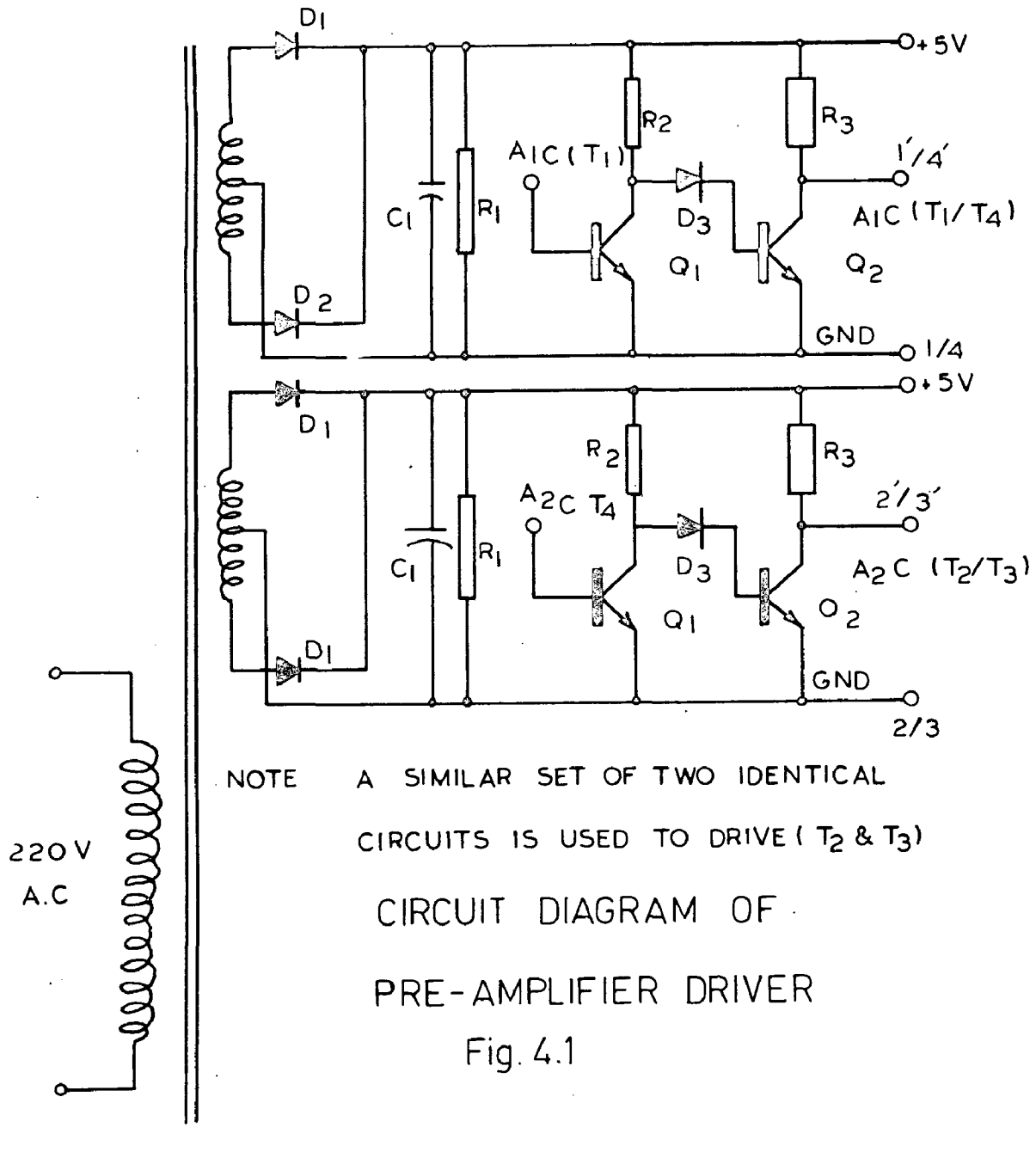
The operating frequency $\overset{40}{25}$ K Hz and voltage is 12 V hence

$12 = 4.4 \times 25 \times 10^3 \times N \times 8.5 \times 10 \times 10^{-6}$ or $N = 25$ turns.

For the maintenance of above flux density the value of H may be taken as 2.0 Oersted. The value of required current can be calculated from $H = \frac{N.I}{l}$ = A.T/meter.

Here $l = \pi \times 30 \times 10^{-3} = 0.1$ meter

$\therefore\ I = \frac{2 \times 0.1}{25} = 8$ m.A. For this current we may choose wire size of 30 SW.G, safely.

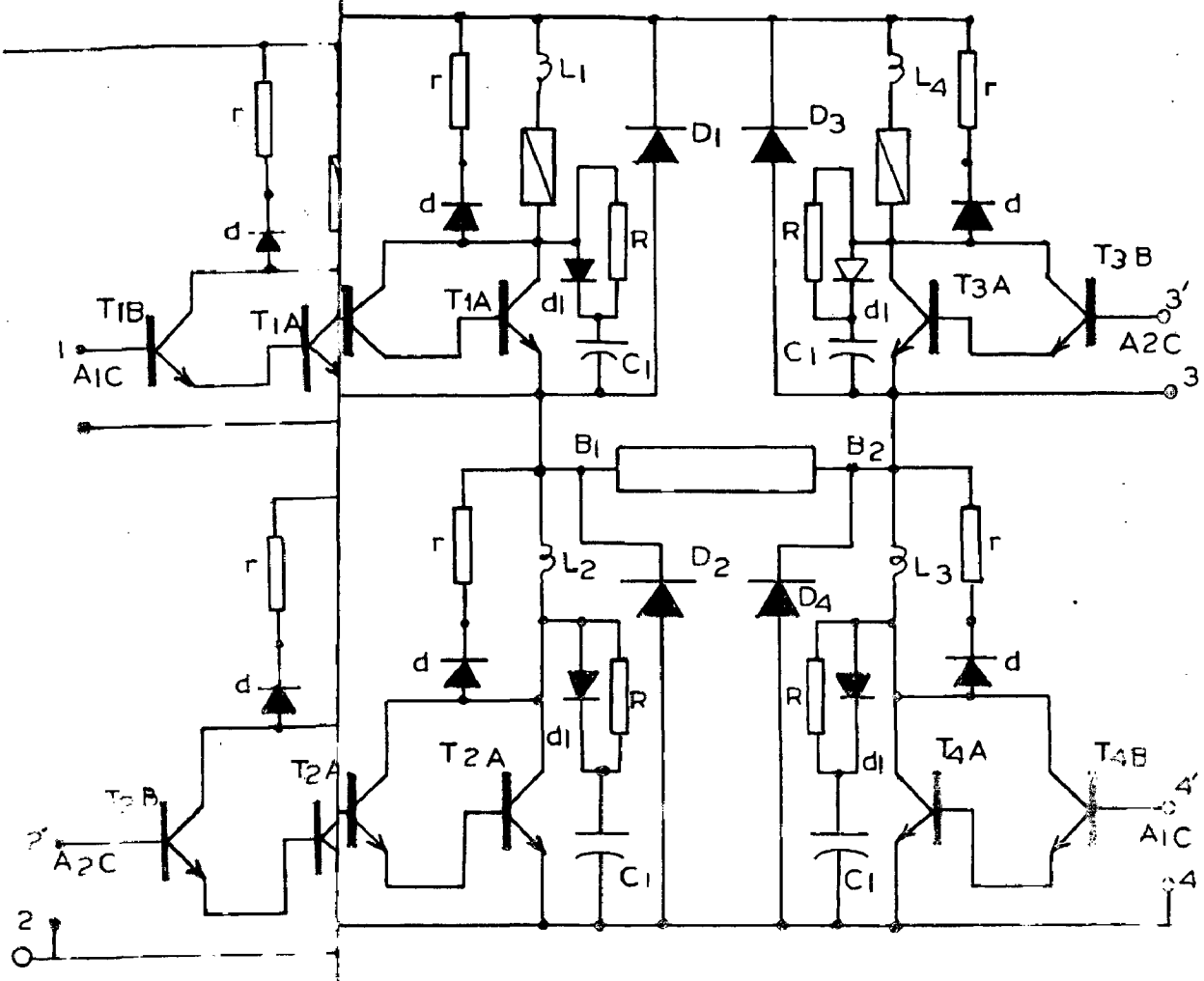


NOTE A SIMILAR SET OF TWO IDENTICAL CIRCUITS IS USED TO DRIVE (T_2 & T_3)

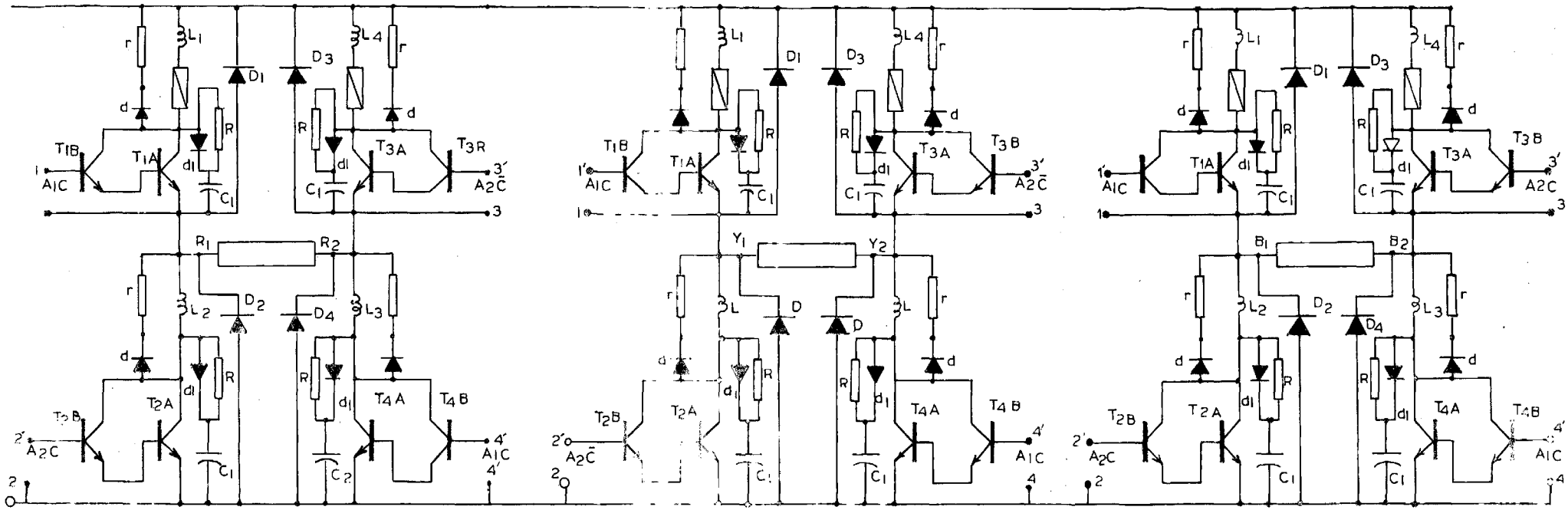
CIRCUIT DIAGRAM OF

PRE-AMPLIFIER DRIVER

Fig. 4.1


r
L1
D1
D3
L4
r
d
R
T3B
T1B
T1A
T3A
3'
A1C
A2C
C1
B1
B2
L2
D2
D4
L3
T2A
T4A
T4B
4'
2
3
4

CIRCUIT



CIRCUIT DIAGRAM OF SOLID STATE THREE-PHASE P W M. INVERTER-POWER UNIT

Fig 4.7

CHAPTER - IV

A THREE PHASE SOLID STATE P.W.M. INVERTER - POWER UNIT

4.1 Description of Power Unit for A Three Phase Solid State P.W.M. Inverters

The basic function of Power Unit is to generate a Three Phase Pulse Width Modulated supply of variable voltage and frequency, both being controlled through control unit. The power unit developed and fabricated in this thesis employ power transistors as switching elements instead of thyristors because of the reasons discussed in Chapter - I, section 1.4.

The power unit receives a three-phase P.W.M. signal that is a set of three phase width modulated square pulses. These pulses are generated in and derived from the control unit after proper circuit isolation and demodulation (as discussed in sections 3.3.3 and 3.4). But pulses, before driving the power transistors in power unit, are to be amplified in current strength through Preamplifier or Driver. The preamplifier or driver stage is used to supply the sufficient base current to the power transistor in order to provide the perfect switching at maximum load current, and forms an integral part of the power unit. The power unit therefore can be divided into two parts: (i) Pulse amplifier/preamplifier or Driver Stage and (ii) Power Control Unit.

The basic circuit diagrams of Pre-amplifier and the Power Control Unit, are shown in Figs. (4.1) and (4.2) respectively.

4.1.1 Description of Preamplifier/Driver Stage:- The preamplifier as shown in Fig.4.1 basically produce a set of four isolated width modulated pulses for each power transistors (T_1 to T_4) used in a phase that is $A_1C[(1 - 1')/(4 - 4')]$ for transistors T_1 and T_4 and $A_2\bar{C}$ $[(2 - 2')/(3 - 3')]$ for transistors (T_2 and T_3). The pulses A_1C and $A_2\bar{C}$ are generated in electronic control unit as discussed in section (3.3.3) through a pulse width modulator circuit as shown in Figs.3.23 and 3.24 and are received in the pre-amplifier after proper circuit isolation and demodulation as discussed in section 3.4 through a puls-isolation scheme as shown in Figs.3.25 and 3.26. The pulse from A_1C or $A_2\bar{C}$ is applied to the base of the transistor Q_1, that generate an inverted pulse train at its collector. Since, the strength of the pulse train A_1C or $A_2\bar{C}$ (derived after demodulation) is not sufficient to drive or switch on the power transistors (i.e. only 5 m-A approx.), these signals at the collector of Q_1 are amplified in current strength, decided by the current gain of the transistor Q_1. Practically the current gain obtainable at the first stage, again, is not sufficient to supply the proper base current to the power transistor, due to limitations of current gain and current carrying capacity of Q_1. Further, the pulses areinverted also, hence a second stage is provided by the use of transistor Q_2 that again inverts the pulses and produce the same pulse train A_1C or $A_2\bar{C}$ at its collector. Also the second transistor Q_2 provide a sufficient current gain, because the gains of Q_1 and Q_2 are multiplied. For example if a nominal gain of 20 is assumed

for each transistor (Q_1 and Q_2) that actual current gain of 400 can be easily achieved. Thus a two-stage pre-amplifier can easily provide the width modulated pulse train (A_1C or $A_2\overline{C}$) of driving capacity upto 2 Amps and can provide an efficient switching of the power transistors employed in power control unit, since the inverter developed in this thesis have the reate current capacity of 10 amp only.

Further, all the four switching pulse trains are to be isolated from each other for the proper switching of transistors T_1, T_2, T_3 and T_4 for a phase-R as shown in Fig.4.2. This is also essential since ; any transistor can be switched on only when the pulse train applied at its base is positive going with respect to the emitter terminal and hence as per circuit configuration of the power control unit, the same pulse train (e.g. A_1C [(1-1')] can not be simultaneously applied across the Transistors T_1 and T_4. The transistors T_1 and T_4 come in series with the load (i.e. the winding of R-phase of the motor), and therefore are required to be switched on simultaneously and with the same shape of pulses i.e. A_1C. The pulses A_1C are applied for a period of half cycle as shown in Fig.3.24. For the next half cycle the pulse train $A_2\overline{C}$ drives the transistors T_2 and T_3, but in a isolated way.

For proper isolation of switching pulses, the insulated d.c. supply voltages of 5 volts are provided in the pre-amplifier by the employing a mains transformer and rectifier-filter circuits as shown in Fig.4.1. In all 12 Nos. of such d.c. supplies are provided for providing isolated switching pulses for all the three phases.

4.1.2 Description of Power Control Unit:- The complete circuit diagram of a three phase power control unit is shown in Fig.4.2. All the three-phases have similar circuitary and identical components. In this section the description of the power unit is confined to one phase (i.e. R-phase) only and for others follows similarly. The power unit employ power transistors T_1 to T_4 as switching elements. Since the power transistors have low value of current gain, the transistors T_1 to T_4 are basically darlington pair of two transistors in order to have a sufficient gain (e.g. T_1 consists of two transistors T_{1A} and T_{1B} connected in darlington pair configuration). The darlington pair configuration of power transistors provide a high gain that in turn reduces the current capacity requirement of the pre-amplifier or driver.

As described in the previous section (4.1.1), the a train of width modulated pulses A_1C or A_2C is applied to the Transistors T_1 and T_4 or T_2 and T_3 simultaneously, for a period of half cycle of fundamental frequency. The pulses provides the switching of power transistors. For one half of the cycle with the application of pulse train A_1C to T_1 and T_4 the motor winding (R_1 - R_2) or load is connected across the d.c. supply to the inverter-power unit, connecting terminal R_1 to + and R_2 to - terminal of d.c. supply. The wave shape of voltage appearing across the load depends upon the waveform of the switching pulses. For second half, when $A_2\overline{C}$ is applied to T_2 and T_3, the motor winding terminal R_2 is connected to positive and R_1 to negative terminal of the d.c. supply and thus the load pulses polarity is reversed.

Thus for a symmetrical pulse width modulation in both half of the fundamental cycles (i.e. when A_1C and $A_2\bar{C}$ are symmetrical), the power control unit employing a circuit configuration as shown in Fig.4.2 ; have the following basic advantages :-

(i) The reversal of polarity across the load in each cycle, produces an output having maximum possible peak or r.m.s. values depending upon the modulation ratio.

(ii) Since for every switching there are two transistors (such as T_1 and T_4 or T_2 and T_3) that come in series with the load, hence the d.c. supply voltage rating can be increased or for a give supply voltage, the transistors of lower voltage ratings can be employed. However for series operation of two power transistors the following factors are of great importance and should be given due consideration before employing them:- (1) The switching pulses must be perfectly identical. (ii) There should be no phase shift in switching pulses. (iii) Protection against be voltage transients should be provided.

~~(iii) Protection against be voltage transients should be provided.~~

(iii) No d.c. component in the output wave, hence the possibility of saturation in the a.c. motor is avoided. This is due to the symmetry of the output wave with respect to zero-level. Further when the modulation ratio is zero, the out is a train of square pulses alternating in polarity after every half cycle and thus the amplitude of sinusoidal output wave in the motor is also zero.

(iv) Identical circuit for each phase, gives a simple circuit configuration and gives a flexibility to use the three phase inverter as three-different single phase inverters. With this flexibility the same unit can be used to control the speed of three different single phase a.c. motors, which is an added advantage.

Further with the identical circuitry employed in electronic control unit, the speed control of three different single phase motors can be obtained either in-dependently and simultaneous, with slight adjustment in control circuitry.

The diodes D_1, D_2, D_3 and D_4, as shown in Fig.4.2, serve the purpose of free wheeling diode. If we consider the switching of Transistors T_1 and T_4 through A_{1C} , the transistors conducts for the intervals, the pulses of modulated pulse train A_{1C} are present and for the intervals these pulses are absent, and the transistors are switched off. The induced e.m.f. (of the inductive load i.e. motor winding of reverse polarity circulate the current through D_1 and D_4 and therefore a free-wheeling action takes place during the period the pulses are absent. The current through transistors T_1, T_2, T_3 and T_4 during reverse recovery time of D_1, D_2, D_3 and D_4 is limited by the inclusion of 1 micro-henery inductors L_1, L_2, L_3 and L_4. The snubber circuit $d_1 R C_1$ or [illegible] etc. provide protection again voltage transients. The Snubber circuits consisting of capacitors C_1 to [illegible] and diodes d_1 to ϕ_4 (with resistance R in parallel) are also provided for protection against secondary break down that occurs when the reverse collector-to-emitter voltage exceeds the primary break

down voltage of the transistor. The reverse collector-to-emitter voltage is applied during the reverse recovery time of the free-wheeling diodes and in inductive loads this reverse voltage applied across collector-to-emitter junction may be sufficiently high. The secondary-break down or a current-avallanche that is most likely to occur in inductive loads, forms a hot spot and ultimately destroys the power-transistor.

During switching-off operation, current is diverted from the transistor to the associated capacitor. When the transistor is turned off, the capacitor is charged, the load current will flow through the associated free-wheel diode.

4.2 Design of Pre-amplifier/Driver

As discussed under section 4.1.1. The pre-amplifier has to provide a set of four isolated pulse trains for each phase and thus is required to provide the pre-amplifier a set of 12 isolated +5V supplies, a part of which is depicted in Fig.4.2. The design of transformer and the rectifier filter part is not taken into consideration in this section because it is quite elementry. Only the design of actual pre-amplifier is dealt with, in this section. The pulses A_1C or $A_2\bar{C}$ are applied at the base of Q_1, that after amplification at its collector are applied to the base of Q_2. The transistor Q_2 is selected to be SL 100 with current capacity of 1 Amp and for that a current gain of 20 can be safely assumed. Since in the power unit two transistors 2N 3055 and ECN055 are used in darlington pair configuration, for them a

normal gain of 10 each i.e. a combined gain of 100 can be assumed. Thus for a max. load current of 10 Amp the base drive or current required to switch the darlington pair is 100 mA. In order tosupply 100 mA base current to power transistors R_3 is chosen to be 50 ohm, 2W. Now for the transistors Q_2 SL 100 a gain of 20 is assumed, therefore the collector drain of Q_1 would be only 5 mA. The collector resistance of Q_1 is therefore selected as 1K in order to supply sufficient current of 5 mA to the base of Q_2. The transistor Q_1 would required at its base approximately 0.2 mA only, that can be easily supplied through the demodulating circuit.

4.3 Design of Power Control Unit

In the design of power control unit that employ power transistors as switching device, it is quite evident that the selection of proper switching device (its characteristic, specification and rating) plays an importance role in order to have a good performance and reliability of the overall unit. Before selecting the particular transistor, it is very essential for a design engineer to have a basic under standing of transistor acting as a switch, its time constants and switching times and also that of the practical design considerations and design trade off, to be safe rather than be sorry when used practically.

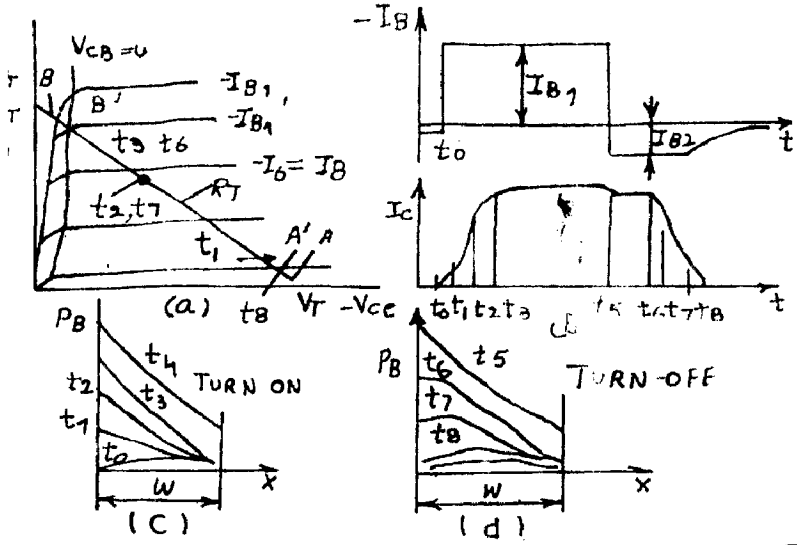
In design of power unit, next follows the design and selection of components for the protection of transistors and also the design or selection of proper heat sink in order to

obtain the most efficient and reliable operation of the power unit. The design of power-unit is therefore divided into the following sub-section:-

4.3.1 Basic Operation & Switching Time Constants of Power Transistor Switch.

The transistor acting as a switch assume two stable state e.g. one in cutoff and other in saturation region and is most often used in a common-emitter configuration, since power gain is highest in this configuration. The basic switching characteristic of a transistor is shown in Fig.4.3. When there is no signal applied to the base-to-emitter, the transistor is in OFF state and offer a high resistance (in M-ohm range) but by the application of step voltage or signal of suitable amplitude ~~is applied~~, the operating point switch over from t_1 to t_4 as shown in Fig.4.3 and reaches in saturation region. In saturation region the transistor is termed as turned-ON and offers a low resistance (less than one ohm). The operation retrace back to OFF state when signal is removed.

Basically, the switching characteristic of a transistor depends upon the switching time constant (τ) that characterizes the variation of collector current and may be calculated using transistor parameters. Normally, the build up time of collector current (that reduces with increase of base current) is given by Over Drive Factor '0' = I_{B1}/I_{B1}' ; where I_B is the controlling base current and I_B' is the base current belonging to saturation limit (point B'. The base and collector current and the hole

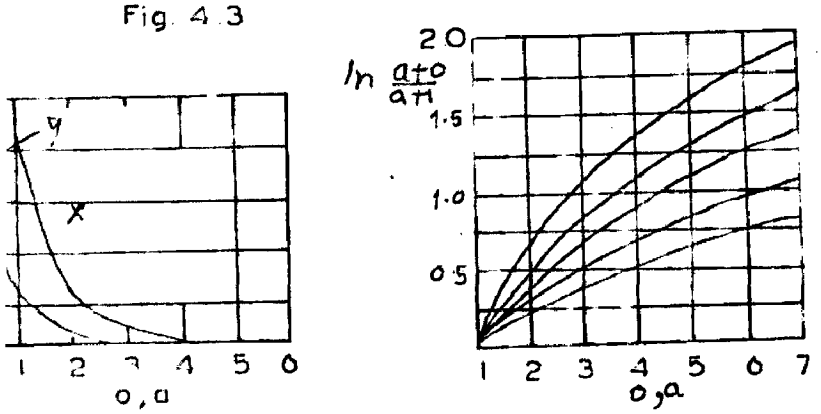


SWITCHING CHARTERSTICS OF TRANSISTOR

Operating Point (b) Base & Collector Current

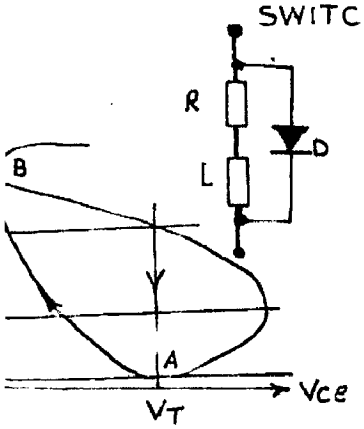
Hole density in base region

Fig. 4.3



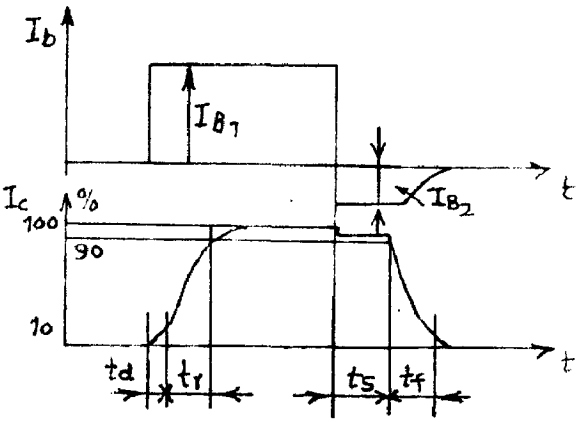
LOGARITHMIC GRAPH FOR COMPUTATION OF SWITCHING TIMES

Fig. 4.5



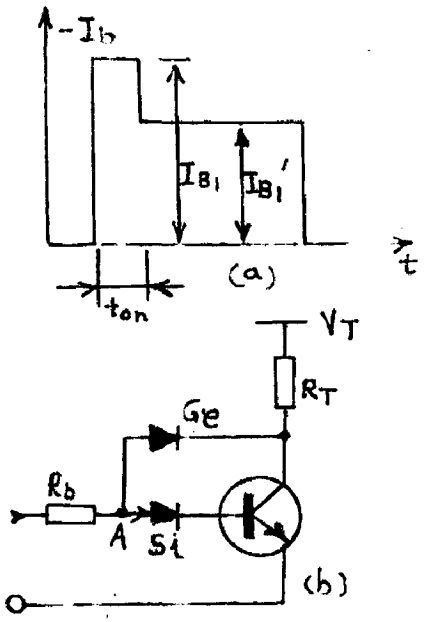
ACEMENT OF OPERATING POINT

Fig. 4.6



SWITCHING TIMES

Fig 4.4



PULSE SHAPE & CKT TO REDUCE t_{on} & t_{off}

Fig. 4.7

density in base region are shown in Fig.4.2-b and 4.2-c respectively. Similarly the fall of collector current depends upon the storage time constant τ_s ; which is proportional to the duration of saturation state. Also the rate of decay of collector current as well as storage time are governed by the reverse bias current I_{B2}. Hence a factor called Depletion Factor is defined as 'a' = I_{B2}/I_{B1}' where I_{B2} is the actual depletion or reverse bias current and I_{B1}' is the base current at saturation limit.

Switching Time of the Transistor:

It is very essential to provide switching times data for a transistor switch as shown in Fig.4.4, which is most helpful in estimating the switching losses and design of power controller employing power transistors in switching mode. As shown in Fig.4.4 ; t_r = rise time, t_s = storage time and t_f = fall time while switch ON and OFF times are given by $t_{ON} = t_d + t_r$ and $t_{OFF} = t_s + t_f$.

In general transistor catalog normally provide the switching time constants τ and τ_s (the storage time constant). The switching times may be expressed in terms of over drive and depletion factor[17] as follows:- Rise Time :

$t_r = \tau \ln \frac{'0' - 0.1}{'0' - 0.9}$; Storge Time : $t_s = \tau_s \ln \frac{'a' + '0'}{'a' + 1}$ and

Fall time $t_f = \tau \ln \frac{'a' + 1}{'a' + 0.1}$ (4.1)

Fig.4.5 represents the logrithmic functions occuring in the expressions of the switching times vs the over drive '0' and

depletion factor 'Q'.

4.3.2 Design Trade Off and Practical Considerations for Using Power Transistor As a Switching Device:

Normally data sheet of a power transistor provides a data curve, that gives a 'Safe Operation Area (S.O.A.) curve. But one should be careful, since the curve is usually drawn for a case temperature of 25°C and must be derated to get the practical values. Although 25°C is the most universal standard, it is completely unrealistic temperature for the power semiconductors. In a typical power assembly, ambient temperature can easily run to 80°C ; consequently the case temperature is quite high.

" One of the most common mis-understanding of design engineers is to believe that maximum ratings are practical normal operating values "[18]. For example if a transistor specification sheet claims 115 Watts dessipation (such as 2N3055) at 25°C case temperature ; it should not be concluded immediately that transistor can really be used to dissipate the total 115 watts. Hence it is essential to derate the 25°C rating to get a practical value, that depends upon the ambient temperature. Further, it should be noticed that the derating factor (given by derating curve) as 10 % of 25°C rating still do not provide a good safety factor. For example if case to ambient thermal resistance for the unit rated at 115W is 10°C/W and junction to case is 1.5°C/W. Then for only 10 W dissipation in an ambient of 80°C, the case temperature rises to 180°. Also the transistor junction temperature rises

to 195°C, which is perilously close to the limit of 200°C for silicon semiconductor devices in metal can.

The maximum allowable rating of a transistor[17] must not exceed maximum prescribed for a given ambient temp and given connection, either in steady state or transient operation. The analysis of the electric and thermal loads on a switching transistor required the knowledge of the current and voltage waveforms in the transistor during switching process. Actually the supply voltage and the nature of load (pure resistance, inductance or capacitance determine the range of operating displacement of the transistor with in safe operation area, provided the dissipation in the transistors do not heat the crystal above maximum allowable temperature. The displacement of operating point in a switching transistor under series R-L load is shown in Fig.4.6, which indicates that the switching off of an inductive load generate over-voltages that may exceed the supply voltage several time and may attain the break down voltage of the transistor and ultimately destroy it. The over-voltage protection of the transistor may be provided by putting a diode in parallel with the load, the switch off then takes place along the straight vertical line as shown in Fig.4.6. The other rating parameters, which many design engineers feel to appreciate are:-

(i) The maximum value of V_{ceo} defined with I_c between 10 and 200 mA. Design trade off are that for high currents and particularly in inductive switching applications, one

should choose a device based upon lower V_{ceo} rating.

(ii) Reverse bias secondary break down rating that is a measure of the energy (in joules) that can be safely absorbed when collector current avalanches or reduced to zero value under reverse bias condition and secondary break down occurs as explained in section 4.1.2.

(iii) Effect of Turn off time (t_f):- In switching applications a major portion of power transistor losses occurs during t_f, the collector voltage is 90 % of the supply voltage or higher and the collector current falls from 90 % of its maximum to 10 % . Consequently a substantial power is dissipated during turn-off. Some times the losses in tail that extends 10 % to 2 % of the collector current are also comparable.

(iv) Effect of base-drive on fall time of power transistor:- The fall time is normally reduced by apply a reverse biase current I_{B2}. Although high turn off-drive current (I_{B2}) shorten t_f , an excessive turn-on base drive (I_{B1}) lengthens it. Further to reduce turn-on time I_{B1} must be large. Therefore in switching applications, the base drive should be just enought to drive the transistor into saturation even at maximum value of collector current. However the over drive reduces the current gain and fall times, hence a suitable circuit as shown in Fig.4.7 can be employed to prevent the transistor from operating in saturation region despite of the over drive i.e. large base currents used to switch on the transistor.

4.3.3 <u>Criterion and Justification for the Selection of Proper Power Transistor</u> :-

The following are the criterion for the Selection of a

particular power transistor to be employed as a switching device:

(a) The transistor should have maximum safe operation area i.e. optimum collector to emitter sustaining voltage V_{CED} and continuous collector current I_C.

(b) Should have low-saturation voltages.

(c) High dissipation rating.

(d) High current gain at maximum operating frequency or minimum switching time.

(e) Highly resistant to secondary break down over a wide range of operating conditions.

In view of the above requirement, the power transistor 2N 3055 (BEL-Make) is chosen, since this transistor was readily available. It is a silicon-n-p-n transistor for a wide variety of high power-application one of which is the power switching circuits. The data-sheet of 2N 3055 gives the following maximum rating of this power transistors (that are of practical importance)[19] :-

(1) Collector to emitter sustaining voltage (V_{CEO}) = 60V.

(2) Continuous collector current (I_C) = 15 Amp.

(3) Transistor dissipation (Case temp of 25°C) = 115 Watts. (At case temperatures above 25°C Fig.1,2 and 4 can be referred).

(4) Maximum safe operation area shown in Fig.2.

(5) D.C. forward current transfer ratio (h_{FE}) given for V_{CE} = 4V and pulse duration (300 μ-sec), duty factor = 1.8 % as 5 for I_C = 10 Amp and 20 to 70 for I_C = 5 Amp.

(6) The construction of this device render it highly resistant to secondary break down over a wide range of operating conditions.

The transistor 2N 3055 is used in power unit in order to provide the switching of D.C. supply to inverter according to the pulse train A_{1C} or A_{2C} and to provide pulse width modulated wave across the load (motor winding) as shown in Fig.(4.1). The d.c. supply to the inverter-power unit can assume a maximum voltage of 100 Volts since two transistor are connected in series, every time the switching takes place. Now from maximum operating area for these transistors (Fig.2)[19], it is evident that the transistors can safely handle 15 Amp current, since in switching 'ON' condition V_{CE} is only about 1.0 Volts. It should be noted that these ratings are given at 25°C case temperature and the derating depending upon the ambient temperature as described in section 4.3.2. Now from current derating curve of 2N3055 i.e. Fig.1[19], it is clear that for current capacity of 10 Amp i.e. about 66 % of rated value, the case temperature should be limited to about 75°C. Assuming an ambient temperature of 30°C (max) and a thermal resistance of about 10°C/W for the heat sink (of 1.5 m.m. blackened aluminium with area of 25 Sq.cm approx.) then the transistor would be able dissipate only 4.5 W while operating at about 50V and delivering a P.W.M. load current of 10 Amp.

Hence it should be varified that total losses in the switching device do not increase more than 4 W. This is

verified by the following calculations:-

The power loss in the transistor while operating in switching mode can be estimating by the heat generated during a half of fundamental cycle. The heat generated can be determined by average power VxI handled during half of the operating cycle i.e. a period of 10 m-sec while operating at 50 Hz and 0.1 sec while operating at 5 Hz. The power losses can be estimated in the following two steps:-

(a) The losses occuring in the function while fully conducting for a period of 10-m sec to 0.1 sec for an optimum condition when in the pulse width modulation the amplitude of sine wave and carrier triangular wave are equal and a square wave is generated. During this period the voltage drop across collector-emitter junction (i.e. Vsat = 1.1V) and current is 10 Amp. The losses are therefore $W_{1(min)} = 1.1 \times 10 \times 10^{-3} = 0.11$ watts to $W_{1(max)} = 1.1 \times 10 \times 0.1 = 1.1$ watts.

(b) The losses in transistor during switching off (the losses during switching ON being neglected since turn on time of the transistor is normally very small ≈ 2 u.sec). These losses actually depends upon (i) turn off time that governed by inductive load and be safely assumed as 100 u-sec for an inductive load of 200 mH and (ii) number of switchings taking place during the cycle under consideration that is 12 for a maximum modulation ratio of 24. Further during turn off the voltage and durrent can be assumed as 50V and 10A. Now the losses

are $W_2(\text{min}) = 50 \times 10 \times 12 \times 100 \times 10^{-6} = 0.6$ watts = W(max) for a fixed modulation ratio (i.e. $f_T/f_s = 24$). But for a variable modulation ratio scheme where maximum value of modulation ratio is 100 that is there are 50 switchings per half cycle, the losses are $W_2(\text{min}) = 50 \times 10 \times 50 \times 100 \times 10^{-6} = 2.5$ watts.

From the above calculation it can be observed that total losses for (i) Fixed Mod. Ratio are W(min) = 0.11 + 0.6 = 0.7 W to W(max) = 1.1 + 0.6 = 1.7 Watts and for (ii) variable Modulation Ratio are W(min) = 0.11 + 2.5 = 2.61 W to W(max) = 1.1 + 2.5 = 3.6 W. Thus it can be varified that the transistor switching losses in P.W.M. are will within the permissible range of 4.5 W. as estimated above, assuming an ambient temperature of 30°C and thermal resistance from case to ambient (Rth C-a = 10°C/W).

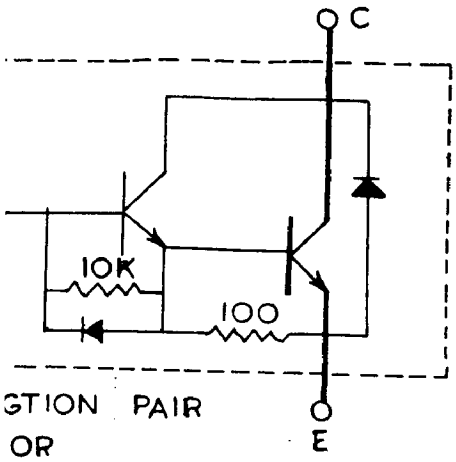
For the selection of power transistor next parameter of consideration is the current gain. This parameter of great practical importance, since the Preamplifier or Drive Stage capacity is determined with this parameter. The Forward Current Transfer Ratio or Current gain basically depends upon two factors (i) the switching frequency (ii) case temp. For the power transistor operating in P.W.M. switching mode with modulation of 20 at 50 c/s, the minimum notch width may be of 0.05 m-sec duration i.e. corresponding to 20 KHz frequency. From gain-band width product curve, Fig.9[19], it can be seen that for V_{CE} = 4V and IC = 10 Amp the operating frequency may be upto 100 KHz or 0.1 MHz. Again from Fig.10 i.e. typical beta-

characteristic (a curve between h_{FE} and I_C for a given V_{CE} = 4V and case temp of 25°C to 125°C) it is can be observed that for I_C-10 Amp at V_{CE} = 4V at 75°C case temp, a typical h_{FE} or current gain is 10 approx. Thus the nominal gain of 10 for 2N 3055, as assumed earlier in section 4.2 is justified. Again in section 4.2 is clear that for power switching at high gain two transistors 2N 3055 and ECN 055 (50V, 5 Amp) are used in darlington pair configuration. For ECN 055, an assumed nominal gain 10 can also be justified as discussed above for 2N 3055 because the two transistors have almost similar characteristics. Thus an overall gain of 100 can be conveniently assumed for a darlington pair of 2N 3055 and ECN 055.

4.3.4 Power Monolithic Circuit/Darlington Pair/High Gain Triple Darlington Configuration of Power Transistors:-

When constructing the power section of a static power controller, normally the following two basic building block principles are incorporated:-

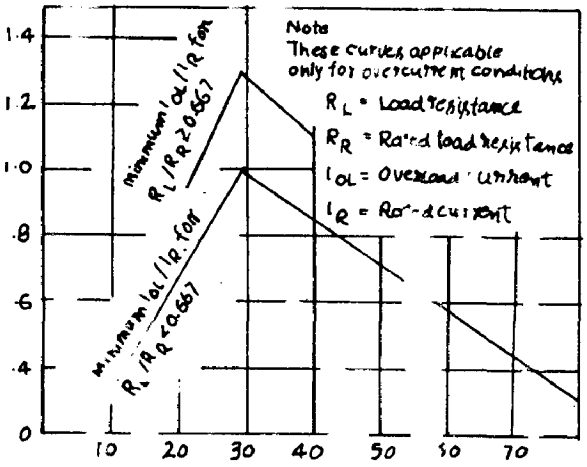
(a) Package Transistor Chips: Mounted on the common strips in direct proximity to each other, is the common production method[20]. The chips are inter-connected as a power darlington with a common drive stage. Practically this technique has already been tried for automatic ignition systems in which transistor chips for 500V integrated power switching were used and mass production of these devices in quantities of millions every year made it possible to dramatically improve transistor



GTION PAIR
OR

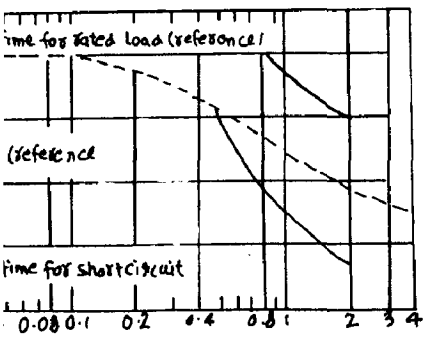
MONOLITNC CIRCUIT

FIG. 4.8



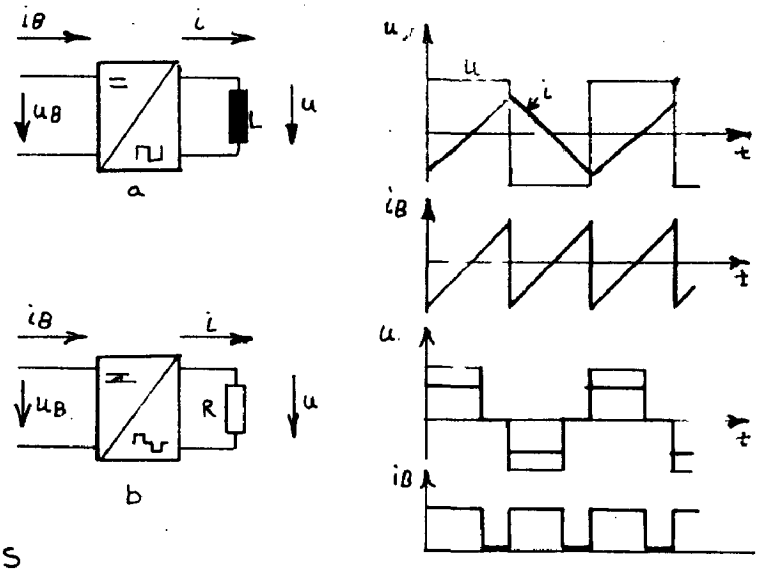
OVERALL CURRENT LIMITING CHARACTERISTIC
dc POWER CONTROLLERS

Fig 4 9



ACTERISTIC FOR SHORT CIRCUIT
RVOLTAGE FOR dc POWER CONTROLLERS

Fig. 4.10



INPUT CURRENTS OF CONVERTERS
(a) WITH INDUCTANCE LOAD (b) OF VARIABLE VOLTAGE

Fig. 4.11

performance and a high reliability of these packaged transistor chips on a scale never before achieved by high-voltage transistors.

(b) Advanced power monolithic circuit (PMC) chips: have been developed recently with a circuit configuration as shown in Fig.4.8. PMC basically is a composite chip comprising the entire darlington power circuit. The integral base steering network as shown in Fig.4.8, increases the base to emitter voltage when the wafer temperature increases at high collector current. When the device is turned ON, the equivalent input network of PMC can be represented by a resistance rb with two forward biased diodes in series. Now heating of P.M.C. at high current density, results in a positive temperature coefficient of the series resistance. This phenomenon assures an absolute corrective feedback mechanism, against over-loading of single chip and this a thermal run away is eliminated by enforcing current sharing for each device in parallel configuration.

Further, the basic advantage of the darlington configuration is that positive base current requirement for the power-stage, is sufficiently reduced to less than 1A for power transistor ratings upto 100 Amps. During turn-off, the fast removal of the stored base charge of the output transistor, is provided by a diode D_1 across the base-emitter junction of the input transistor. The diode D_2 across the emitter-collector junction provides protection against secondary break down (as explained in section 4.1.2) that is most likely to occur in inductive loads. The complete circuitry as shown in Fig.4.8 is fabricated

on a single chip and such power monolithic circuit chips are presently employed in all the present day static power control equipments, employing these devices as switching elements.

Although a darlington configuration of power transistors gives a significantly improve current gain as a compared to a single power transistor (such as a gain of 100 can be achieved) and thus require a lesser base drive but as compared to thyristor this gain is quite low. For example a thyristor (Type-261, Westighous Make) can switch forward current of 200 Amps with a gate trigger current of 150 mA only and thus have a gain of about 1300 is achieved. The thyristor, however have a great problem of turning-off i.e. commutation is required that is a great problem in most of the applications. → To next page (102)

In this thesis a novel (alternative) idea is suggested to employ switching power transistors in 'High Gain Triple Darlington' configuration. This idea was first of all suggested by 'Eric Burwen'[21] and have the specific advantage that a very high current gain and a saturation voltage equal to that of two transistors can be achieved. Practically this configuration is tried[21], for switching resistive load current of 2A at 20 Volts and a gain of 250,000 is achieved. It is not however tried for high voltage, large current switching application and is a new field of research in efficient power switching. It is therefore suggested to try this idea in power switching and it is expected that if perfect switching (at large currents) is possible in this configuration a nominal current gain of about 1000 or more can be easily obtained. Thus employing a successful, High gain triple darlington power transistor switch, a perfect switching can be obtained with base drives approaching to that of trigger current in a thyristor and the field of efficient solid state switching using power transistors can be revolutionized.

~~A high gain triple darlington circuit is shown and described in detail in Appendix~~ .

4.4 Design and Selection of Protection Circuits and Components

In the power unit along with power transistors some circuits and components are also provided in order to provide a proper operation of the inverter and to provide the protection of power transistors (the main component) used in the inverter. The design and selection of these circuits and components is presented in the following sub-sections:-

4.4.1 Selection of Proper Rating for Free Wheeling Diodes:- As explained in section 4.1.2 and shown in Fig.4.2, the free wheeling diodes carry the load currents during off intervals of the switching pulses. The value of applied induced e.m.f. and the load current determine the rating of Free-Wheeling diodes. Conventionally, the rating of these diodes is selected to be equal to the rating of switching elements i.e. Power Transistors. The power unit fabricated in this thesis is designed so as to deliver an output of 400V and 10 Amp, in case the high voltage and current (e.g. 800V,10A) rating power transistors are available, as discussed in section 1.4 of chapter I. Hence the free wheeling diodes are selected having 800 volts P.I.V. and 10 Amp current rating.

4.4.2 Design of Air Core Inductors (L_1 to L_4):- The currents through transistors T_1 to T_4 during reverse recovery times of free wheeling diodes D_1 to D_4 are limited by the inclusion of inductors L_1 to L_4 of 1 uH. The inductor of such a small value can be easily fabricated by few turns of copper wire that form an air core inductor. However the choice of number of turns require the understanding of designing an air core. The inductor inductance of a air-choke or inductor is a function of the coil geometry (i.e. shape and size)[22], and can be calculated from the empirical formula $L = N^2 D_K \phi \times 10^{-9}$. Henery; where D_K = Mean diameter of coil in Cm; ϕ = form factor and N = Number of turns.

In table at Fig.6.8[22], we can read off the factor ϕ, where the coil geometry parameters are $\beta = b/D_K$ and $F = r/D_K$.

Here b is the height of coil and r is the radial thickness. If we form a coil of single layer using conductor of diameter 0.2 cm (that can easily carry the load current of 10 Amp), the coil diameter D_K = 2 Cm and height or length of 5 cm ; then β = 2.5 and ρ = 0.04. For these value of β and ρ from table as referenced above, the value of ϕ = 3.2, Now we can calculate the number of turns from the emperical formula ; as $1 \times 10^{-6} = N^2 \times 2 \times 3.25 \times 10^{-9}$ or N = 14 turns (approx).

4.4.3 Design of Circuit For Protection Against Voltage Transients:-

Voltage transients are considered to be those voltage levels which exceed the normal repetitive peak voltage applied to the power transistor. Any switched energy storage system (such as inductive load or motor winding) is a potential source of over-voltage. Because of profound influence of voltage transients on successful operation of the transistor circuits; an understanding of sources of transient voltages and the means of reducing them is essential.

For voltage transient suppression three basic approaches can be employed such as: (i) Series suppression (ii) Shunt suppression (iii) Combination of (i) and (ii). Functionally the series transient suppressors acts as a series impedance which varies from low resistance under normal operation to high resistance when a transient appears. Where as a shunt transient suppressor appears as an open circuit under normal conditions and becomes a low impedance shunt path during transients. The shunt type suppressor that basically consists of a series resistor and a capacitor is called a 'Snubber Circuit'. The

basic snubber circuits consisting of capacitors C_1 to C_4, resistor R and diodes d_1 to d_4 are shown in Fig.4.2 and are connected across the switching power transistors (T_1 to T_4). The basic function of this snubber circuit is to protect the power transistors from secondary break down that is most likely to occur because of excessive reverse voltage applied across the collector to emitter function during off-period of switching pulse. This reverse-bias voltage is basically the induced voltage (e.m.f.) generated in motor winding that depends upon the inductance of the motor winding and the operating frequency. Since the switching transistors connects the winding to one polarity for a half cycle, the maximum frequency at which e.m.f. (reverse bias) will be applied would be 50 Hz when the inverter is operating at 100 Hz and switching wave is a square wave (under worst case i.e. M.I$\geq$1). Hence the following design factors can be assumed[23]; for the design of snubber circuit that will by pass the current from the transistor to the capacitor C_1 when transistor is off and a transient of reverse bias voltage is applied:-

1. Peak switching voltage (d.c. voltage) = 230V (max).
2. Operating frequency = 50 Hz.
3. Rate of rise of voltage across collector-emitter is to be limited to 100V/μ sec.
4. Choose ϵ = 0.65 for a controlled voltage overshoot of approximately 20 %.

Now refer the nomograph (such as shown in Fig.16.16 through 16.18[23] to determine:-

(a) The required time constant of the snubber, referring Fig.16.17 and is by connecting two point specified by point 'A' = $(dv/dt)/E_S$ = 100/230 = 0.44 and point 'B' = θ = 0.65. Thus R-C time constant is evaluated as 3.5 u-sec.

(b) The value of R, refer Fig.16.16 and locate $(I_p.R)/E_S$= 0.63. If I_p = 25 Amp then R = (230 x .63)/25 = 50 ohms.

(c) From $R_C = 3.5 \times 10^{-6}$ we have C = $(3.5/50) \times 10^{-6}$ = 0.07 uF or 0.1 uF (approx).

Thus we have R = 50 ohms and C = 0.1 uF as designed values for snubber circuit. For proper dissipation the rating of R is taken as 5W.

4.4.4 Over Current Protection and Overall-Current Limiting Characteristics of Static Power Controllers:-

Because of relatively low thermal capacity of semiconductor devices such as Transistors or SCR,S, protection against overcurrents is often more critical than for other type of electrical components. Since the transistor do not have any overload capacity, the selection of proper current limit and circuit protection scheme plays an important role for the efficient and reliable operation of the device. There are two basic reasons for incorporating the proper current limit and circuit protection : (1) To protect the unit itself and (2) to protect the circuit or system it is controlling.

During normal operation, the power dissipated in the switching transistor is held to a minimum, by providing a proper base drive current to cause, the transistor to saturate and thus incur a small voltage drop. While, during over-load, short circuit or voltage transient, there is a tendency for

the load current to increase, that causes the transistor to fall out of saturation and increased its power dissipation. Since the input voltage can not be controlled by this device, current limiting must be provided to hold power dissipation within limits and prevent the semiconductor junction from rising above the rated value when the maximum voltage is applied on the input and the output is shorted to ground. A current limiting characteristic specified for the d.c. power controllers[24], is shown in Fig.4.8. From this figure it can be observed that for a rated voltage (29V d.c.) and normal loading conditions (R load/ R rated $\leq$ 0.667), the current is permitted to be limited to 100 % for short circuit at the output while for (R load/R rated $\geq$ 0.667 the current limit is set at 130 % for an overload. These limit characteristics are called as "fold back" and are incorporated to provide current values greater than rated for starting surges and also allow current reduction to protect the switching transistor during the action of circuit protection (i.e. current limit and trip out).

However, it would be impractical to design the power controller to dissipate such a large amount of power on a continuous basis, hence a trip out circuit is incorporated to turn-off the power switch if the overload or short circuit conditions prevails for a long time. Also an indication should also be provided for this tripping. A trip characteristic for short circuit and/or overvoltage for the d.c. power controllers is shown in Fig.4.9. It should be noted from this figure that a minimum to max. trip time of 1 to 3 secs is provided at 29 V

for short circuit or overload which is practically justified because this time must be long enough to prevent nuisance tripping caused by transients of very very small durations.

4.4.5 Filtering of Harmonics at the Input of P.W.M. Inverter :-

Normally the direct current absorbed by the inverter from its supply source is not quite smooth. Further if the voltage regulation is incorporated within the inverter itself and the load is inductive ; the current in the supply source is either alternating or clipped[22] as shown in Fig.4.10. Basically the power absorbed by the inverter from the supply source is equal to the product of the mean current and the supply voltage. But the r.m.s. value of the supply current is more than mean value and the losses occuring in the internal resistance depends upon the r.m.s. value. Hence to reduce these losses filtering at the input of the inverter is essential. The filtering at the input of inverter is provided normally by a L-C filter. The capacitor absorb the a.c. component of the input current. While across the inductance, the a.c. voltage is only because of a.c. component of current being absorbed by the capacitor, which is substantially small. However, if the voltage control is achieved by pulse width modulation, the value of capacitor reduces. But, for an inductive load the energy of the inductance is to be absorbed by the capacitor in any case which is sufficiently large. Hence if a L-C filter is incorporated with a P.W.M. inverter feeding an inductive load such as motor, the energy required to be stored in the capacitor

would be significantly large and consequently a larger a.c. voltage will appear across the inductor that would lower the regulation and also reduce the efficiency of P.W.M. inverter fed induction motor drive. Hence for a P.W.M. inverter operating on stiff d.c. supply, only capacitor is used for filtering and regulation of energy stored in the inductive load.

Further for the P.W.M. inverters fed with rectifier, a capacitor at the input side is indispensable, since rectifier permits no current reversal.

PHOTO-[1] OUTPUT OF THREE STEP COUNTER (A_0/B_0)

A_0 — LOWER TRACE.
B_0 — UPPER TRACE.
FREQ. = 50 Hz

PHOTO-[2] SQUARE PULSES (R_{SQ}/Y_{SQ})

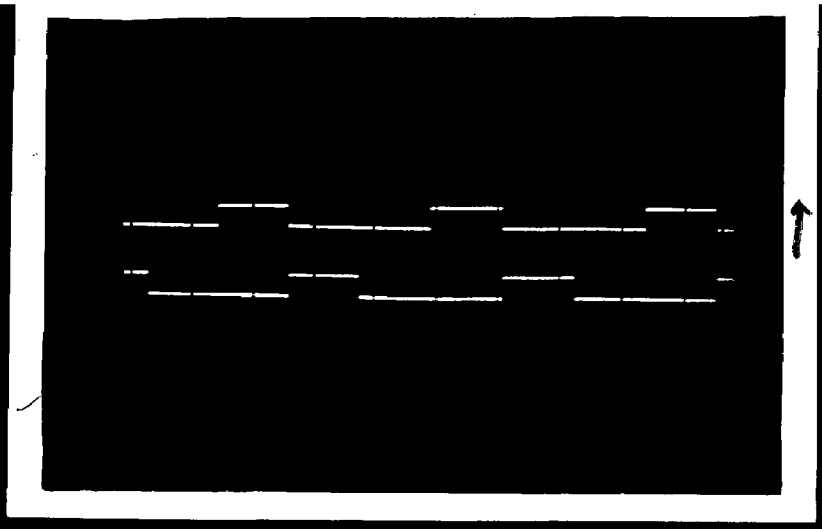
R_{SQ} → UPPER TRACE.
Y_{SQ} → LOWER TRACE.

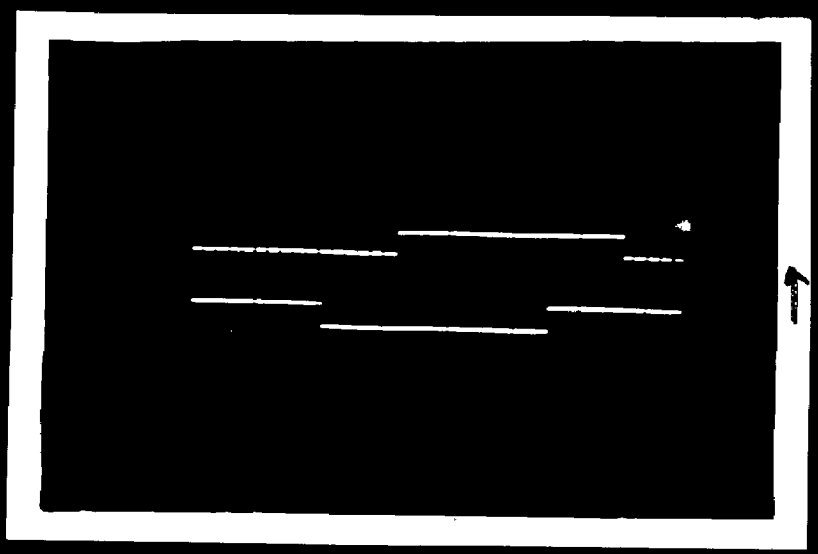
PHOTO-[3] REFERENCE SINE WAVES (R_S/Y_S)

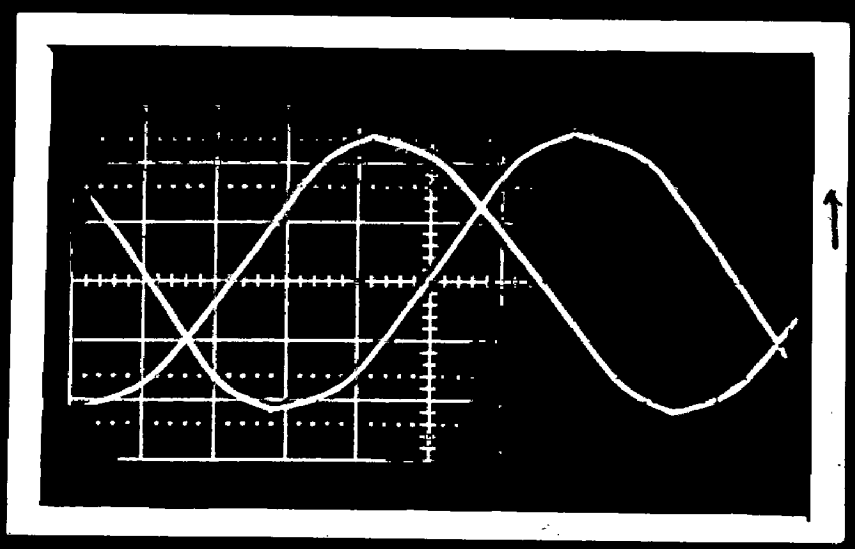
R_S → Sine Wave Starting From a Point Below Zero Line.
Y_S → Sine Wave Starting From a Point Above Zero Line.
FREQ. = 250Hz.

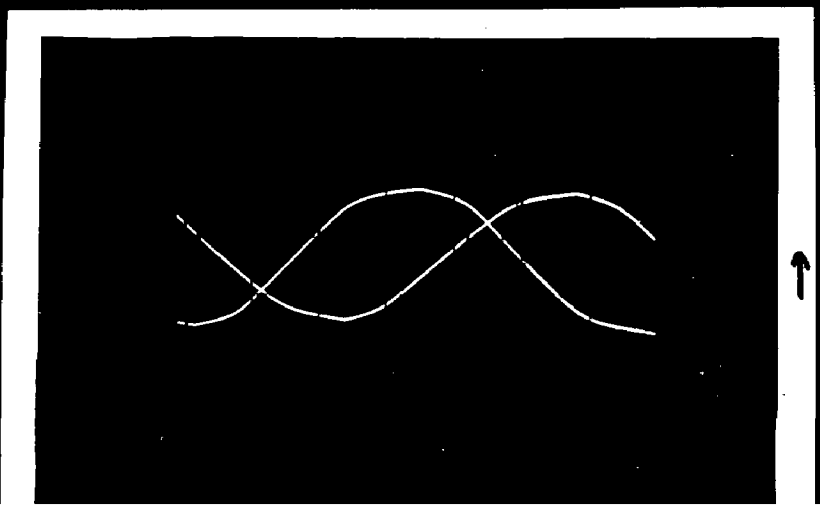
PHOTO-[4] REFERENCE SINE WAVES (R_S/B_S)

R_S → Sine Wave Starting From a Point Above Zero Line.
B_S → Wine Wave Starting From a Point Below Zero Line.
FREQ. = 15 Hz.









CHAPTER - V

PRACTICAL OBSERVATIONS AND TEST RESULTS

5.1 Waveforms Observed at Various Points In Control-Unit

In this section, the various waveformes observed practically at different points in the circuits blocks of the control unit ; are shown in Fig.3.14. (Chapter III) and through photographs [1] to [7]. The block-diagram of the control unit is depicted in Fig.3.1, (Chapter-I). The description and comments of the waveforms and photographs are as follows:-

The waveform at the output of voltage to frequency converter is depicted in Fig.3.4 Chapter-I (as e_0 vs t) and the tringular charging and discharging of the integrator I-1 is shown as (e_0 vs t). As observed in waveform e_0 vs t, the discharge time two t_D is small as compared to charging time t_0 , hence the output is not a square wave, but train of sharp pulses.

These sharp pulses are converted to square pulses and then to a set of three sequential pulses A_0,B_0,C_0, through a three-step counter (as shown in block-diagram Fig.3.1). The pulses A_0 to B_0 to C_0 appear in succession one after another and are shown at (1), (1') and (1") in Fig.3.14. Also a set of two such pulses observed practically, is shown photographed in Photo [1]. It is clear from this photo that B_0 (lower trace) follows in succession with A_0 (upper trace). Now Fig.3.14 shows the wave forms QR = $A_0/2$ and R_{sq} at (2) and (3) respectively that are the square pulses and generate a square wave R_{SQ} for

phase R at ④. Again these square pulses for phase Y, $Q_Y = B_0/2$ and Y_{sq} are shown at ②' and ③' and square wave Y_{SQ} at ④' respectively. The square pulses R_{sq} and Y_{sq} that generate square waves for phase - R and phase - Y, are shown in Photo [2], as photographed practically. From this photo it can be clearly observed that these sequare pulses have a phase - displacement of 120°. These pulses are used to generate square pulses R_{SQ} and Y_{SQ} having again a phase displacement of 120°.

The waveforms at ⑤ and ⑥ Fig.3.14 show the generation of sharp quenching pulses as required for an analog integrator (Fig.3.11) employed to convert the square wave R_{SQ} to a triangular wave R_T shown at ⑦. The similar type of quenching pulses, generated for an integrator required for phase-Y, are shown at ⑤' and ⑥' in Fig.3.14. Further the triangular waves R_T and Y_T are converted to sine waves R_S and Y_S through triangular to sine wave to sine wave converter (Fig.3.13) and shown at ⑧ and ⑧' in Fig.3.14. Fig.3.14 also deputs the various waveforms for the generation sine wave for Phase-B. Photograph-[3], shows sine waves generated for R-Phase and Y-Phase respectively at 50 Hz. This photograph shows clearly that there is a phase shift of 120° between R_S (the wave starting from point below the zero line in the photograph) and Y_S(the wave starting from a point above the zero line). Similarly Photo-[4] depicts the sine waves R_S and B_S at about 15 c/s. Again this photo-shows that there is a phase shift of 240° between R_S and B_S where R_S is the wave starting from a point above the

PHOTO-[5] WIDTH MODULATED PULSE TRAIN (A_1C)

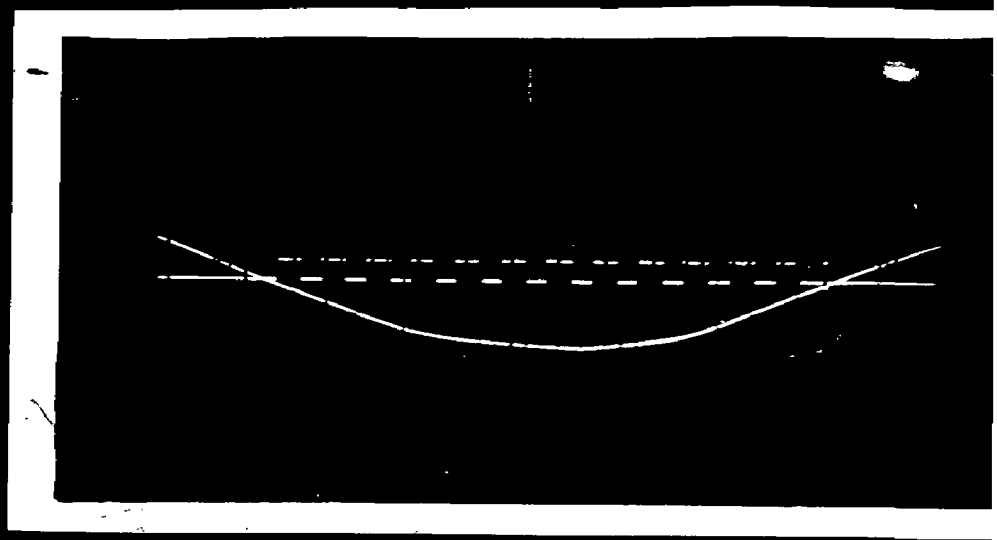
M.I. = 0.6 (Approx.)
M.R. = 24
f_s = 50 Hz.

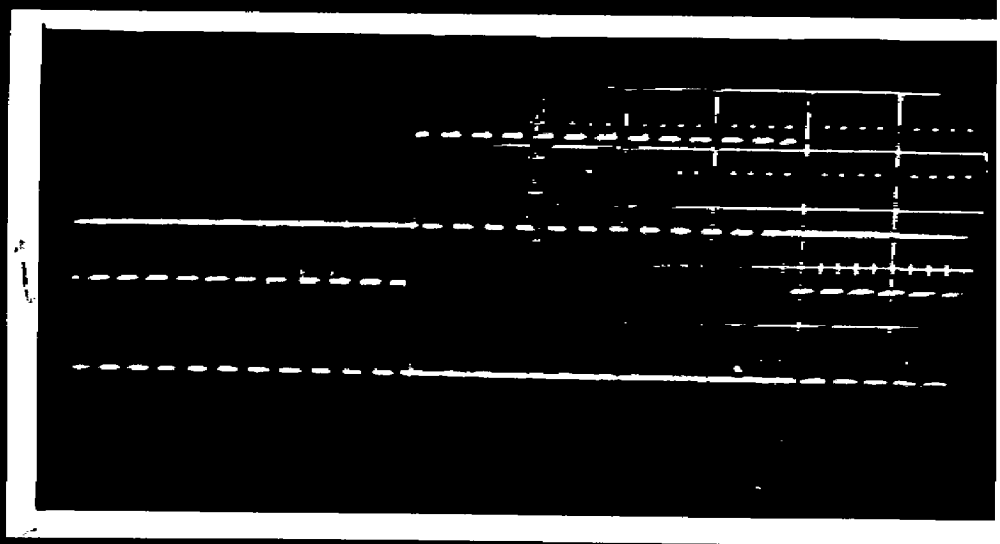
PHOTO-[6] WIDTH MODULATED PULSE TRAINS (A_1C/A_2C)

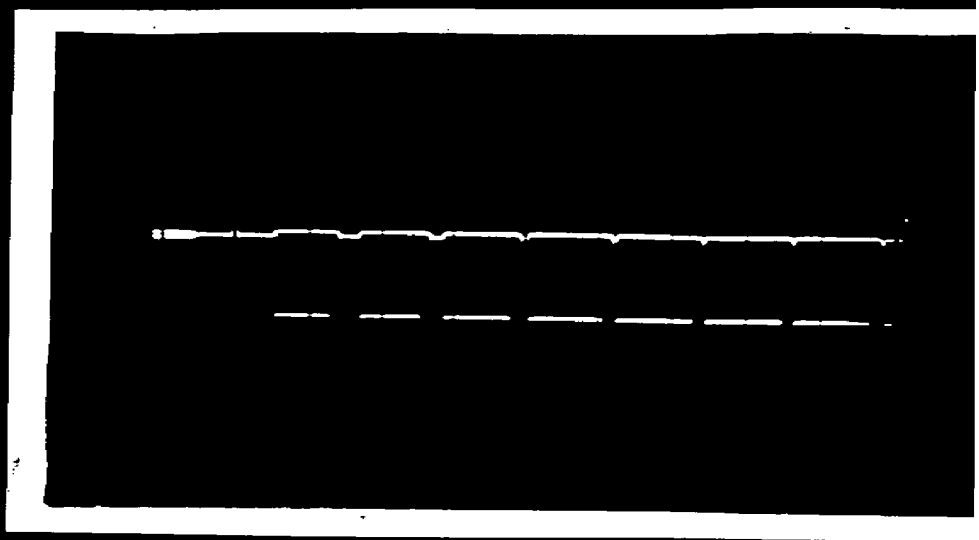
M.I. = 0.2 (Approx.)
M.R. = 24
f_s = 25 Hz

PHOTO-[7] HIGH FREQ. SUPPERIMPOSED WIDTH MODULATED PULSE TRAIN

M.I. = 0.8 (Approx)
M.R. = 24
f_s = 50 Hz







zero line and B_S is the wave starting from a point below the zero line.

The there phase sine wave is modulated with a triangular wave with a frequency ratio or Modulation Ratio (MR = f_T/f_S= 24 or 12 or 6). The pulse width modulation is achieved by a circuit as shown in Fig.3.23. The Fig.3.24 shows that A_1C or $A_2\bar{C}$ are the width modulated pulse trains for each half of a cycle. Actually, A_1C is a width modulated,pulse train for positive half of a cycle of reference sine wave. This pulse train A_1C with a Modulation Index (M.I = A_S/A_T ; where A_S = Amplitude of reference sine wave and A_T = Amplitude of triangular carrier wave) of 0.6 (approximately) and M.R. = 24 is shown photographed in Photo-[5] at reference sine-wave frequency of 50 Hz. Also Photo-[6] depicts the both of width modulated pulse trains (A_1C and $A_2\bar{C}$; Fig.3.24) for a M.I = 0.2 and M.R= 24 at reference sine wave frequency of 25 Hz (approx.)

These width modulated pulses are transferred from electronic control unit discussed in Chapter III to Power Unit (Chapter-IV), through a Pulse Isolation Scheme, shown in Fig. 3.25. As described in section 3.40, that a very high frequency carrier (as compared to width modulated pulses) is super imposed on the width modulated pulses A_1C or $A_2\bar{C}$. These high frequency width modulated pulses are transferred from control unit to power unit through pulse transformers. Photo-VII, shows a high frequency (about 40/25 KHz) superimposed width modulated pulse train (A_1C), R-Phase appearing at the collector of Q_8.

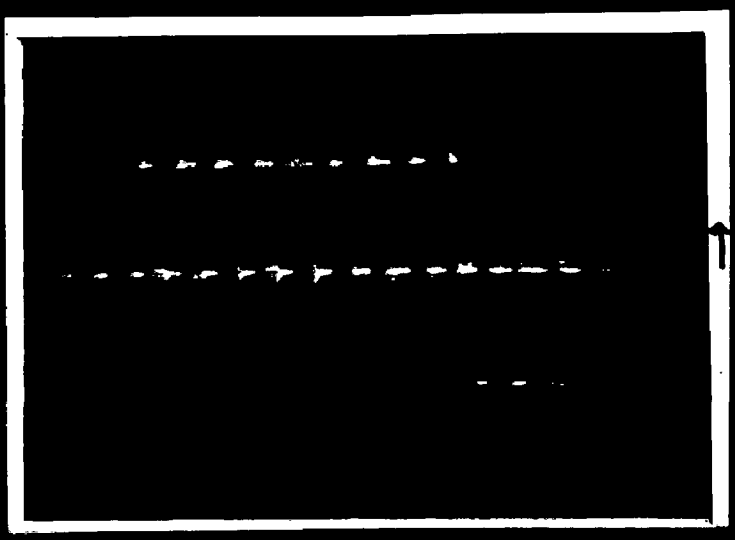


PHOTO-[8] INVERTER OUTPUT ACROSS RESISTIVE LOAD
R = 10 ohms
M.I. = 0.4 (Approx.)
M.R. = 24
f_s = 25 Hz

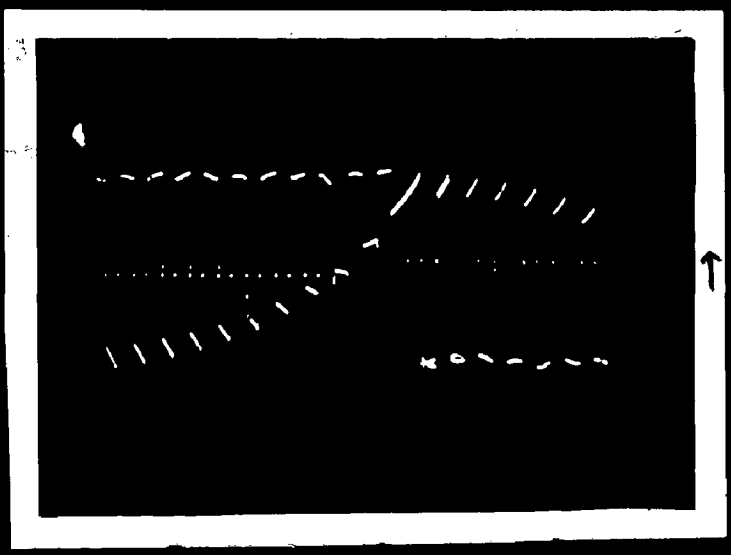


PHOTO-[9] INVERTER OUTPUT ACROS INDUCTIVE LOAD
R = 10 ohms ; L = 50 mH.
M.I. = 0.5; M.R. = 24
f_s = 50 Hz.

In this case sine wave of 50 Hz is modulated with M.R = 24 and M.I = 0.8. Since the width modulated pulses are filled with a high frequency of about 25 KHz the superimposed pulse train shown in Photo-[7] where the high frequency carrier is not clearly visible but the pulse width modulation is clearly visible.

5.2 Waveforms and Test Results of Power Unit/P.W.M. Inverter:

As described in Chapter-IV, the power unit delivers a three phase pulse width modulated supply of variable fundamental operating frequency and variable amplitude. A simusoidal mean voltage is produced when this supply is fed to an inductive load such as induction motor. Basically the power unit employ power transistors that are switched on or off as per the waveform (A_1C or $A_1\overline{C}$) driving the transistors T_1 to T_4 for a phase-R. The output across the load (or motor winding) is a pulse width modulated wave alternating in polarity every cycle (because of the power circuit configuration and driving pulse train as shown in Fig.4.1 and Fig.3.24).

Photograph-[8], show the inverter output waveform across a pure resistance load of about 10 ohms in a phase-R i.e. across R_1-R_2. The D.C. input to the power control unit/inverter is 20V and is obtained after a rectification through a three-phase bridge rectifier and a L.C filter consisting of an inductor of about 0.15 mH and a capacitor of 5000 µF and are calculated from the emperical formula [25], as % ripple = (1.33)/LC for a three phase 50 c/s supply fed bridge rectifier, where, L is in

Henery, C in μF. Then L for 2 % ripple is given by 2 = (1.33)/ L x 5000 = 0.133 mH or 15 mH).

[Power supplies for Electronics Equipments by J.R.Nowicki.] This rectifier/filter supply gives a correct value of 2 % ripple when loaded upto 5 Amp with a resistive load.

Photo [8], depicts an inverter output voltage across a resistive load for a M.R. of 24 and M I = 0.4 (approx). From this photo it is clear that the output waveform is similar to the waveform of switching pulses ile. a width modulated pulse train A_{1C} or $A_2\overline{C}$. The amplitude of output pulse trains (width modulated as per A_1C or $A_1\overline{C}$ appearing for each half cycle ; alternates ih polarity every cycle and have a value of about + 19 V to zero and zero to - 19 V respectively. Further it can be observed that :- (i) The top level (+ve peak or -ve peak) widths and zero level widths of the pulses, are straight lines, because of the filter circuit being provided at the input of the power control unit. (ii) There is a reduction in peak value of amplitudes of the pulses. The peak values are ± 19 V and thus, a drop of about 1V occurs on each polarity that is due to the pulsating voltage of about 1 Volt appearing continuously (during inverter operation) across the inductor used in L_C filter. The pulsating voltage of 1V.p-p appearing across the inductor is because of the pulsating current drawn by the resistive load connected across the inverter output (i.e. R_1-R_2) and is also justified from the calculation that is as follows:- Let us assume the pulse train of average frequency

of 1 KHz (i.e. 24 times to 50 Hz which is the fundamental operating frequency of the inverter). Then for a current with a total r.m.s value of approx.1.0 amp and total r.m.s voltage of about 10 Volts (as observed through dynamometer type ammeter and voltmeter); the voltage appearing across the inductor L (0.25 mH) is V_L = WL.I(r.m.s) = $2\pi.1000 \times 0.15 \times 10^{-3} \times 1$ = 1.0V(approx). The value of total r.m.s a.c voltage appearing across the load of M.I = 0.5 and with M.R = 24 as read by a dynamometer type voltmeter is 10 volts. Now it can be varified from the table 9.12 pp.219[4],(that gives the harmonic content of a sine modulated uni-directional wave) that for a M.I = 0.4 and M.R = 20, total harmonic content is 50.2 % of the d.c supply. Since a dynamometer type of instruments read a total r.m.s value of an electrical quantity (i.e. current, voltage or watts), hence the inverter output voltage read by a dynamometer type voltmeter, in this case (where a M.R = 24 and M.I. = 0.4 is selected) is a measure of total harmonic content. This voltage is read as 10V which is 50 % of the d.c input and is almost equal to the value given by the total harmonic content in the case of a sine modulated.(Uni-directional wave f_T/f_S = 20 or MR =20 and A_S/A_T = 0.4 = M.I. This equivalency leads to an important conclusion that the sine modulated wave appearing across the load in the P.W.M. Inverter developed and fabricated in this thesis produces an output wave that shall have a harmonic pattern equivalent to that of a sine modulated uni-directional wave. This conclusion is further supported by the following discussion:-

It should be observed from Fig. 3.21(a) of puls width modulator in electronic control unit, that the pulse width modulation of bi-directional or two level type(in every half cycle of a fundamental operating frequency) is achieved by modulating a reference sine wave with a bidirectional triangular carrier wave as described in section 3.33Chapter III. These width modulated pulses A_1C or A_2C two level-bidirectional P.W.M. nature are used to drive the power transistor T_1 to T_4 in such a way that the pulse width modulated output of inverter alternates in the polarity every cycle. Thus even though the pulses in every half cycle have their widths modulated as per two-level/bi-directional modulation but because of the alternating (+ve to zero or zero to -ve) nature of the output wave, the output shall have a harmonic pattern equivalent to that of a uni-directional or three-level type of P.W.M. Again it can be observed from the Table 9.12[4] that gives (harmonic content of sine modulated unidirectional wave with $f_T/f_S=20$) and table 9.23 (that also gives the harmonic content of a sine modulated bi-directional wave with $f_T/f_S=20$); that:-

(i) The harmonics 1 to 20th are present in output in the case of bidirectional or two level modulation while in case of uni-directional P.W.M. all the even harmonics are absent and others are present.

(ii) The amplitude of all the harmonics 1 to 15 (as shown in table 9.23 for bidirectional P.W.M. wave) are smaller then the amplitudes of the corresponding harmonics in

case of unidirectional P.W.M.(as shown in table 9.12).

Hence it is concluded from the above discussion and comparision that the output wave of the P.W.M. inverter (developed and fabricated in this thesis) have utilized both the advantages of a undirectional and bidirectional P.W.M. and are:-

(1) that all the even harmonics are eliminated from the output wave. The elimination of even harmonics is mainly due the unidirectional nature of the output wave.

(2) that all the harmonic present in the output (except even harmonics that are eliminated as stated above) have the smallest possible amplitudes. This is due to the bi-directional type of pulse width modulation being adopted to generate the width modulated pulses such as A_1C or $A_1\bar{C}$ as shown in Fig. .

Photo [9] depicts the output waveform when the inverter is feeding a R-L load. The load consists of an inductor of the value of 50 m.H and a parallel resistance of 25 ohms. The waveform shows that:-

(1) The top or bottom widths of the pulse train in a half of the cycle are almost at the same voltage level as in the case of resistive load, (as shown in Photo-(8)), but are wary in nature instead of straight line,as in the case of resistive load. This is because of the reason that only condenser is connected across the out-put of rectified supply and the wary nature is because

of the ripple presented in the supply when inverter is feeding the load.

(2) The zero line width are shown shifted downward in one half and upward in the other half. This shift in zero-line widths is due to inductive nature of the load.The magnitude of this shift actually depends upon the value of inductance of the load. Larger the inductance, more would be the shift in zero line width.

(3) The shift in zero-line widths, basically indicate the fly-back action or the application a reverse voltage appearing across the load because of stored energy in the inductor or the any other inductive load such as winding of a.c. motor. The fly-back action actually takes place during off-period of switching pulses that is when non of the transistor is in conduction and the load is removed from the supply. The stored energy in the inductor or the em.f of a motor winding then circulate the current through free-wheeling diodes during this period (i.e. the period in which Transistors T_1 and T_4 or T_2 and T_3 are not conducting) and thus apply a reverse-voltage across the load.

5.2.1 Inverter Operation on Load:- In this section the performance of Three-Phase P.W.M. Inverter developed and fabricated (in this thesis), is observed by operating the inverter with a variable resistance. An experiment was performed with the observations as follow:-

(a) Inverter operating conditions:-

(i) Modulation Ratio = f_T/f_S = 24. (ii) Operating frequency of inverter = 50 Hz (iii) Modulation Index (A_S/A_T) = 0.8 (iv) Input Supply Inverter = 20 V.D.C. (Input supply is filtered through Ø L-C Filter ; with L = 0.15 mH and C = 5000 µF) (v) Resistive load = 50 ohm, 5A (Variable).

(b) Observations on Resistance Load:-

The inverter was found to operate satisfactorily on resistive loads with a loading current upto 5 Amp(max.) in all the three phases. A load test performed on phase -R is tabulated below in Table-'A'.

TABLE - A

Sl.No.	D.C. Input				A.C. Output *		
	VOLTS		AMPS		VOLTS		AMPS
	V_{dc}	V_{dc}'	I_{dc}	I_{dc}'	V_{ac}	V_{ac}'	I_{ac}
1.	20	-	0	-	15	-	0
2.	20	-	1.3	-	13.5	-	0.5
3.	20	-	1.4	-	13.5	-	1.0
4.	19.5	21.0	1.85	1.8	12.8	14.0	2.0
5.	20.5	21.0	2.75	2.6	12.5	13.0	3.0
6.	20	22.5	3.2	3.15	10.5	13.25	4.0
7.	22	23.5	4.3	4.0	10.5	12.5	5.0

The following inferences can be drawn from the table'A':-

(i) It is possible to load the inverter upto 5 Amp giving proper operation.

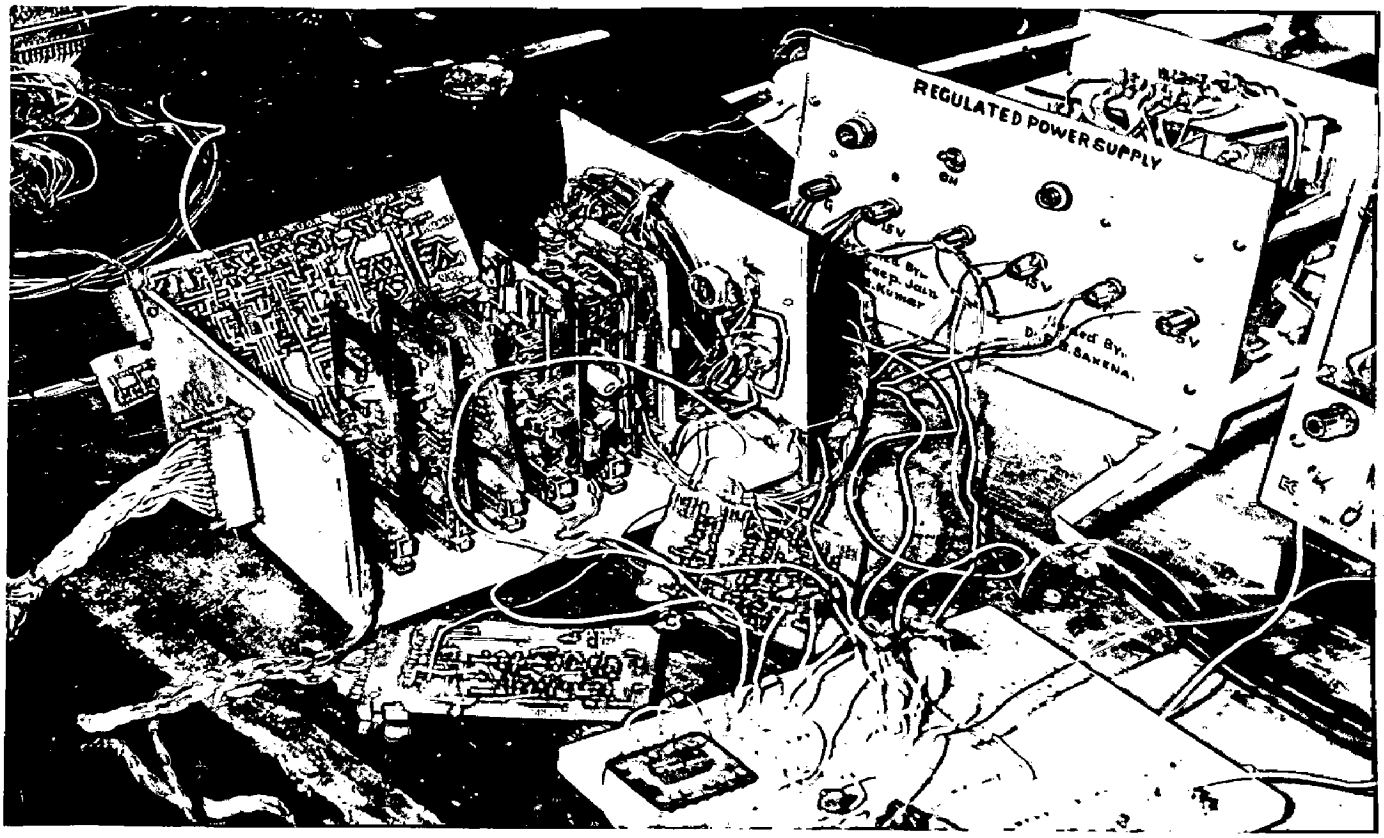


PHOTO-[10] PICTORIAL VIEW OF ELECTRONIC CONTROL UNIT

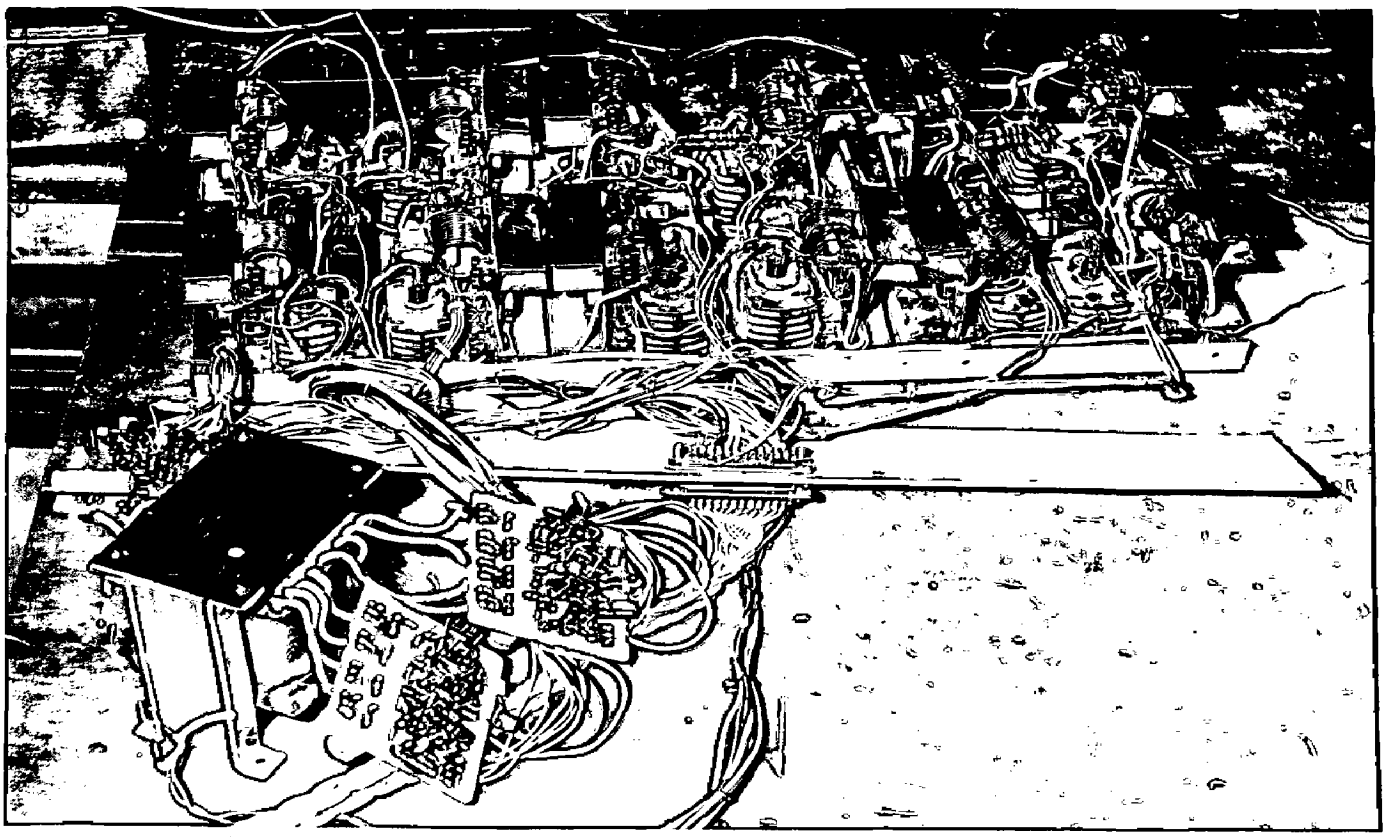


PHOTO-[11] PICTORIAL VIEW OF POWER CONTROL UNIT

(ii) The observation of V_{dc} reveals that voltage falls on loading after 2 Amp. The reason for this is that the current drawn from D.C. supply is pulsating at about 1200 Hz at which drop across the inductor in filter circuit goes on increasing with the load. If we observe the input supply D.C voltage on C.R.O. it can be seen that on no load or loads upto about 1 Amp the supply remains pure d.c but after 1 amp say 2 Amp to 5 Amp there is a modulated wave super imposed the D.C supply. This super imposed wave have the waveshape as that of the switching pulses and there is a dip in the d.c voltage during the period the load current flows. This dip causes the average d.c value to be decreases as shown for V_{dc} at g. No.4 in the table "A". Hence in order to compensate a slight boost in d.c voltage is required so as to maintain average d.c. supply voltage constant. Actually the values V_{dc}' are obtained after compensating for such dips by increasing the d.c. supply slightly and observing on C.R.O. the wave shape of d.c. supply. The d.c. supply is adjusted in such a way that average d.c. remains substantially constant.

(iii) On observation of V_{ac} and V_{ac}' it is evident that the voltage across the load remains substantially constant and there is only 1 Volts difference between V_{ac} = 13.5 and V_{ac}' = 12.5 at 5 Amp. Thus the regulation of the inverter is quite good that is about 8 % from a load of 0.5 Amp to 5 Amps.

5.2.2 Pictorial Views of Electronic Control Unit and Power Control Unit:

Photo [10] and [11] give the pictorial views of Electronic control unit (described in Chapter III and and Power Control

Unit (described in Chapter IV) Photo[10] clearly depicts the printed circuits cards are fabricated and mounted on plug-in printed card connectors for better reliability, easyness in testing, repair and interconnection of different cards. The card No.1 from front panel, contains the circuitary for VFC and 3-step ring counter, card No.2 and No.3 for square pulse to square wave to sine wave converters. The 4th, 5th and 6th cards contain the circuitary for Pulse Width modulation, while card 7th (last from rear panel) contains a divider (to obtain proper) modulation ratio and a triangular carrier generator and is shown lying flat and connected to its connector in the cabinet through a card connecting chord. The big printed circuit card No.8, in the rear of camera eye, contains the total circuitary for circuit Isolation and there are 6 pulse transformers mounted on the bottom of this card.

Photo.11 gives the complete view of power control unit employing power transistors with a set of two power transistors connected in darlington pair and mounted on the same heat sink. The heat sinks for power transistors are mounted with flat face (vertical) and four horizontal fins to give sufficient area for cooling the power transistors which are the main source of heat generation while switching ON and OFF. On the flat face of these heat sinks, the power transistor are mounted with proper thermal contact with the sink. Finned type heat sinks are used for free wheeling diodes The snubber citcuits and fuses are provided in the space left between the mountings of power transistors.

The air core choke coil made of spiral shape coil of copper wire with a resistance and a diode connected across it, is also visible.

The preamplifier or driver is also clearly visible that consists of a transformer as shown in Photo and a set of three equivalent cards used for providing sufficient base drive to the power transistors.

CHAPTER - VI

CONCLUSIONS AND SUGGESTIONS

From the test results it is clear that practically it is possible to run a ;110V, 0.5 KVA, 3 Ø, Induction motor with the Three Phase solid state P.W.M. Inverter (employing power transistors as switching device). It is also possible to vary the speed ; of the induction motor by supplying a 50 V.D.C. to the inverter and maintaining a M.R = 24 (f_T/f_S) and M.I = 0.8, simply by varying the fundamental frequency of operation i.e. f_S through the variation of a d.c. control signal V_1. The variation of d.c. control signal basically varies the frequency ofV.F.C. and consequently the fundamental frequency. Since the speed of an induction motor can be varied by the variation of frequency of the 3Ø supply, hence it is possible to vary the speed of the induction motor, from 10 % to 100 % of the rated no-load speed by variation of P.W.M. supply frequency from 5 Hz to 50 Hz. The speed variation is observed to be quite smooth through out this speed range.

However it could not be possible to operate the inverter motor-drive at P.W.M. supply voltage of more than 40 Volts because of the lower voltage ratings of the power transistors but the motor could be loaded upto 4 Amp. The loading of motor at a fixed frequency and proportional fixed voltage of inverter output,(i.e. 35V at 25 Hz) however could not be performed because of the large impedance of the motor winding and consequently a substantial voltage drop occuring in the

winding impedance and therefore reducing the available air-gap power or torque on the rotor. Hence the load test on the inverter motor drive, operating in open loop configuration but fed with constant V/f condition could not be performed and thus motor-characteristics while operating on the P.W.M. inverter could not be evaluated. With the availability of the high voltage, large current rating power transistors (such as 800V, 30 Amp); it would be practically feasible to control the speed of conventional 400V, 3Ø. Squirrel cage induction motor upto 10 KVA or more, by employing the same power unit simply by replacing the existing power transistors (2N 3055) by high voltage and current rating power transistors and also the same electronic control unit to control the speed of the induction motor from 10 % to 100 % of the rated speed.

In order to obtain a constant V/f operating of the induction motor drive employing a solid state P.W. M. inverter developed in thhs thesis, some modifications in the electronics control scheme are required such as:-

(1) The amplitude control of the reference sine wave R_S, Y_S or B_S, that in the present case is achieved through three potentiometers (one in each phase), should be replaced by amplitude control employing Analog Multipliers (chip recommended in section 3.2.2). The employment of analog multipliers for amplitude control of three phase reference sine waves if recommended because of the main reasons:- that it would provide a precise, a linear smooth amplitude control of constant amplitude, 3Ø sine wave, simultaneously with a common control signal V_2, that is the basic requirement for

obtaining the constant V/f operation of an inverter and practically could not be achieved in this thesis mainly because of non-availability of Analog Multipliers having a good linearly (of the order of 0.5 %). A good linearity as the basic requirement to have a precise control of amplitude through a control signal V_2 i.e. 0 to 10V signal for the amplitude control from zero to max. of 10V.

(2) Some control circuits are required to be disigned and developed for the following purposes:-

(a) A circuitary to provide an overload/short circuit protection employing a current feedback. A voltage proportional to the current can be used to provide this protection as well as to reduce the deformation in the current wave[3.3] as shown in Fig.3.23, that normally occur at low p.f. loads.

(b) A phase-reversal circuitary to provide a counter current braking (plugging) condition.

(c) A circuitry to maintain a definite ratio between the two control signals V_1 and V_2, such that the frequency varies with a direct proportion to the amplitude i.e. a constant V/f condition.

(3) If a completely automatic speed regulating system (as shown in Fig.2.13) required. The following circuits are required to be developed:-

(a) (i) speed controller (ii) Active current controller. (iii) Start Protection Device (iv) Flux controller, that compares voltage and flux sensed through voltage and flux transducers.

(b) A processing unit that continuously observed the the above parameters (V, f, R_{ST} and R_{TS}) and process them to give the control action and the switching pulses to the power unit or inverter.

Thus in this thesis the practical feasibility of employing the power transistors in place of thyristor (as switching device), in Solid State inverters is observed. The employment of power transistors results in relatively simple control scheme to obtain a constant V/f operation, as compared to thyristor which reqäires comparatively more complicated control scheme because commutation is to be provided for every switching. Thyristors also require the bulky.energy storage circuits for commutation purposes and thus increases the bulk, xaka weight and complexity of the statically controlled equipment.

B I B L I O G R A P H Y

1. 'Thyristor Control of A.C. Motors'; J.M.D. MURPHY

2. IEEE Transaction on Ind.& Appl. Vol. IA-8, pp -584- 592, Sept./Oct. 1972.

3. 'Current Source Converter for A.C. Motor Drives'; K.P. Phillips, IEEE Trans. Ind. and Appl., IA,- 8, pp 667-683, Nov./Dec. 1972.

4. 'Thyristor Control'; MAZDA, 1973 Chapter 9, pp 208-230.

5. 'Volt-Amp. Rating of Components of P.W.M. Inverter System', , IEEE Trans. on Industrial Electronics & Control Instrumentation, IECI -25, No.8, Aug. 1978, pp - 278.

6. 'Several Modulation Techniques For a Pulse Width Modulated Inverte R.D. ADAMS & R.S. FOX, I.E.E.E. Trans. on Ind. Appl. Vol IA -8, No. 5, Sept./Oct. 1972, pp 626.

7. 'Output Current Regulation with P.W.M. Inverter - Inverter Motor Drive'; J.B. Forey the & S.B. Dewan, IEEE. Trans. on Ind. Appl., Vol IA -11, No 5, Sept./Oct. 1975, pp 517.

8. 'Direct Flux & Torque Regulation in a P.W.M. Inverter, Induction Motor Drive'; Allan. B. PLUNKETT., IEEE Trans. on Ind. & Appl, Vol IA - 13, No. 2, March/Spril 1977 pp 139.

9. 'Digital Phase Locked Loop for Induction Motor Speed Control'; P.C. SEN & R. MOFFAT, IEEE Trans. on Ind. Apl., Vol IA -15, No -2, March/April 1979.

10. 'Speed Regulating System of Squirrel Cage Induction Motor by Frequency Converter'; IOAN. D. LANDAU, IEEE Trans. on Ind. Appl., Vol IA -5, Jan./Feb. 1969, pp 53.

11. 'Use V/f Converters for analog data transmission', JERALD GREAME, Electronics Design 7, April 1, 1975.

12. 'Operational Amplifiers (Design & Application)'; JERALD. G. GREAME & GENE. E. TOBEY, pp 213.

13. 'Manual for Operational Amplifier Users'; John, D.Lenk, pp. 203.

14. 'A Solid State, Variable Frequenoy, 3-phase Power Source with Individual Harmonic Control'; D.A.G. PEDDER, A.M. ISHAW & H.R. BOLTON, IEEE Trans. on Industrial Electronics & Control Instrumentation, Vol IECI -24, No.1, Feb., 1977 pp. 102.

15. 'Hand Book of Linear Integrated Circuits'; HAMILTON pp. 349.

16. Same as (14); pp. 104-105.

17. 'Power Electronics'; F. Csaki, K. Ganskey, pp.495.

18. 'A Focus on Power Transistors' Electronic Design-23, Nov. 8, 1977, pp -55.

19. B.E.L. Semiconductor Data Manual.

20. 'Practical Desing Problems in Transistor DC/DC Converter & dc/ac Inverter' Proc. IEE (Lond). Vol. 106.Pt B Suppl. 18, pp. 1373 April 1960.

21. 'High Gain Triple Darlington has low Saturation Voltage'; I Eric Burwen, G&S. Systems Inc., Burlington, Mass.

22. 'Desing of Power Inductor step by step' Electronic Design - 26, Dec 20, 1977.

23. 'S.C.R. Manual' General Electric, 5th Edition; 1972 pp. 482.

24. 'Solid State Switching for Air Craft Electric System'; L.D. Dickey & C.M. Jones ; IEEE Spectrum, Nov. 1970.

25. "Power Supplies for Electronic Equipment"; J.R. NOWIKI.