SPEED CONTROL AND SYNCHRONIZING OF ALTERNATORS USING PHASE LOCKED LOOPS

A DISSERTATION

Submitted in partial fulfilment of the requirements for the award of the degree of

MASTER OF ENGINEERING

in

ELECTRICAL ENGINEERING

(System Engineering & Operation Research)

By

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C O N T E N T S

D E D I C A T I O N

This work is dedicated to the memory of Khutu Mian who spent more than fifty years of his active life as a Synchronizing operator in the "Salawa" Power station of Meerut District. Khutu personofied in himself the genius of Indias technological skill - a mind innovative and uncontaminated with borrowed and half -bakede ideas, a hand gifted with creative craftsmanship and applied disinterestedly with consummate passion, and an attitude fiercely independent, dominating and primordially, blunt in action. From Khutu more than from any one else has the authors imbibed and inherited some of the finest tradition of the 'Indian Technological Spirit' and he is indeed grateful to him.

C E R T I F I C A T E

CERTIFIED THAT the Dissertation entitled "SPEED CONTROL AND SYNCHRONISING OF ALTERNATORS USING PHASE LOCKED LOOPS" which is being submitted by PRAVIN PRADHAN in partial fulfilment for the award of the Degree of Master of Engineering in Systems Engineering add Operations Research - Electrical Engineering of the University of Roorkee, Roorkee is a record of the student's own work carried out by him under my supervision and guidance. The matter embodied in this dissertation has not been submitted for the award of any other degree or diploma.

This is to further certify that he has worked for a period of 9 months from FEB ,1978 to OCTOBER 1978 for preparing this dissertation at this University.

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November 10,1978.

A C K N O W L E D G E M E N T

The author expresses his sincerest gratefulness to Shri M.K. Vasantha, Reader, Department of Electrical Engineering, University of Roorkee, Roorkee and his guide and Supervisor for the present work, for all the help and guidance that he has received so spontaneously from him throughout the period of this work. It was indeed a privilege to have worked under him.

The author would be singularly ungrateful if he does not record his indebtedness for the help rendered by M/S Amber, P.K. Srivastava, Ashish Saxena, R.S. Dheer all presently students of the University. To M/S Kishan Lal, Tiwari, Chaman Lal, C.P. Ganguli, Shoogan Giri, Phool Singh, Rishi Pal all members of that vital force the technician Cadre brigade- without which no technological project worth the salt can be implemented in real flesh and blood, the author cannot but be grateful.

To that symbol of "dynamic dangerous living" "The UST9803 "the author offers his salutations for the many tasks it has

accomplished with speed and efficiency.

ROORKEE

Dated: November 10,1978.

(PRAVIN PRADHAN)

A_B_S_T_R_A_C_T_

In the present work, an integrated and fully automatic speed control scheme, has been conceived and implemented, based on the concepts of both frequency and phase locking. Perhaps for the first time, an attempt has been made to develop, a fully automated Synchronizer for power station applications utilizing the techniques of both frequency and phase locking. In the area of implementation new types of hib precision frequency difference and phase difference detectors have been developed and fully tested. The incorporation of dual locked loops in the control scheme is primarily dictated, from considerations of improving significantly the system stability. Endowed with orders of accuracy within .002 percent and considerably improved levels of repeatability and stability, the developed control scheme promises to be extremely versatile with applications ranging from high precision regulation of large capacity motors to automated Synchronizing of multi motor systems in addition to thatof fully automated alternator Synchronizers. A unit feature of the dissertation is the development of an experimental version of the PLDS for research investigations and educational purposes.

I N T R O D U C T I O N

The impetus for the present work has come from the realization that the real potential of the Phase Locked Loop and its associated techniques still remain to be exploited in the fascinating and versatile area of precision electrical machine control system. And this becomes evident, even from a cursory survey of the literature pertaining to this area. For how else is it explainable that as yet, the phase Locked Loop and its associated techniques has not been applied to the problem of fully automated Synchronizing of power station alternators. The other major shortcomings which becomes strikingly evident from a survey of the Existing literatureof Phase-Locked Loop Drive Systems (P.L.D.S.) are:-

1. This technique has still to make in roads into the commercially important area of 'precision Industrial Electric Drives' involving the use of large DC and AC motors.

2. The problem of instability of PLDS's particularly in the lower speed range has still to be over come even in the case of sub-fractional horsepower servo systems.

It was primarily to fill up these important Lacunas in the application of Locked Loop Control Techniques in general and of the Phase Locked Loop in particular the present work was initiated.

With these ends in view the first chapter of the present work deals essentially with the evolution pattern which has taken place or is exp ected to take place in the allied areas of Locked Loop Drive System and fully, automated Synchronizers. It also presents, the salient details of the significant literature available in this area of development. Chapter 2 deals with the fundamentals and detailed description of the developed schemes and Systems. In particular a detailed description is given of the integrated and fully automated Synchronizers for power stations based on the application of the Locked Loop Techniques. Details circuit action are also spelt out in respect of the phase difference and frequency difference detectors, developed specifically for this scheme . In the third chapter the Emphasis is on design considerations and performance features based on actual experimental investigations and test results.

The concluding chapter summarizes the important conclusions of the present work discusses critically the scope and potential for further work and spells out the specific areas in which such precision drives can find applications. In particular, it predicts radically new areas of application of such systems which are relevent for the "region" development programmes of the developing countries.

CHAPTER-I

EVOLUTION AND SURVEY OF RECENT DEVELOPMENTS (LOCKED LOOP DRIVE SYSTEMS AND AUTOMATED SYNCHRONIZERS)

1.1 Perspective And The Evolution Pattern

The evolution and development pattern of solid state "Locked Loop Contrd Systems" and in particular of the "Phase Locked-Loop Drive Systems" (P.L.D.S.) has followed the familiar trend of technological advancements that have taken place in recent years, in the area of precision and automated Electrical machine controls in general and of Drive Systems in particular. The initiating impetus for the advancement originates essentially either from major break-throughs achieved in material and component hardware developments or from heavy reductions in the per unit cost of components developed primarily for applications in conventional areas. This is closely followed by application and adaptation of already existing techniques in the allied areas of signal processing and logic implementation. This in turn leads to new developments in the above techniques with the primary aim, of eleminating those new performance shortcomings that are invariably associated with the advanced systems undergoing development. With performance optimized by an order of

nagnitude now-where approachable by the existing conventional systems the emphasis is next placed on achieving a high level of "in built " system reliability. Side by side new testing procedures are evolved and standardized for effecting critical performance evolution of developed systems. The next major step in the evolution pattern stems from the new levels of performance and geometry that are attained with the advanced systems. These levels of performance and geometry ultimately lead to the opening up of radically new areas of applications not inthe least possible by the conventional systems. This inturn, brings forth developments oriented towards specific applications in specialized areas.

On the basis of the technical survey carried out in the broader area of precision and automated electrical machine control systems and of Locked Loop control systeme in particular, the following salient points emerge in respect of the evolution pattern of automated Locked Loop control systems. This study includes in addition to the conventional research literature scrutiny acritical survey of both the manufacturers and the users literature in respect of hardware advancements testing techniques and technical specifications of specified application areas really inneed of automated

and high precisi n facilities:-

(1) The initiating impetus for the development of Locked Loop electrical machine control systems came from the availability of in expensive phase Locked Loop in monolithic IC form for the first time in 1971.

(2) The reported developments are confined to the area of "Phase Locked-Loop Drive Systems " using monolithic PLL IC's.

(3) The P.L.D.'s's developed fill yet are essentially servo systems with the associated motors being by and large DC sub-fractional horsepower motors.

(4) The development pro achieve till yet is still confined to the second stage-namely, the development of PLDS's with only the already existing techniques of signal processing and logic implementation.

(5) The Locked Loop Control Systems have as yet, not made in roads into the field of Automated Synchronizers for power stations which goes without saying is an area that is not only of the greatest practically importance but is also at the same time an application in which the need for total reliable automation is a very genuine one.

(6) The existing state of the art of automated Synchronizers is still at the experimental stage and that too is confined to the application of conventional techniques like those of Electromagnetic slip frequency measrment and frequency come face difference comperators using conventional analog methods.

(7) The development trend of Automated Synchronizers reported till yet is towards all "Solid State Equipment".

1.2 Survey-Recent Developments

The first recorded reference in which mention is made regarding the possibility of using phase Locked Loops for electric machine control applications is on article by R.A. Miller (2). This paper established for the first time the unique potential of PLLS's as comparators in digital control schemes for shaft speed and position parameters. However the major emphasizes in this work is towards bringing out the distinct superiority of digital control schemes for rotating electrical machines. In 1970 Volpe(3) established the view points for the first time, that a hysteresis Synchronous motor operates similar to a phase-locked loop as encountered till then in communication applications. From this view point a model adequately describing the motorsmotion

with respect to Synchronism and specifically the well known hunting characteristic phenomenon is presented, analysed and interpreted. It is also mentioned that a fair degree of experimental success was achieved in stabilizing a hysteresis synchronous motor using the PLL typeof control system. However, no details of this are spell out in the above work.

As already emphasized earlier it was not till the advent of in expensive digital PLL'S in monolithic I.C. form that real interest was aroused in the application of PLL's for electrical machine control. To Moore(4) goes the credit of having taken a pioneering step of suggesting a practical PLL control Scheme for a reel to reel tape drive using a MC4044 phase frequency detector IC for controlling a permanent magnet DC Motor. His other significant contributions in this work were as follows:-

(1) His estimated prediction to the effect that P.L.D.S.'s through the experience of locking on to a reference frequency can achieve speed accuracies of the order of .002% representing almost a hundred fold improvement over earlier methods of speed regulation.

(2) His prediction that Motors of any size can be controlled with this technique .

(3) His specific estimation that the digital PLL approach would be more economical as compared to conventional servo systems and particularly for high precession drive systems.

(4) His identification of specific and specialized PLDS application areas such as conveyor systems for materials handling, a computer peripheral drive or in general application where motors have to be Synchronized to each other or to an existing clocking signal.

(5) His performance comparison and evaluation of different types of digital phase detectors with particular reference to their important performance parameters.

(6) His suggestion of a specific practical schemwhich includes component details.

However Moores work does not contain any experimental details of the suggested scheme. His work was followed by Smithgalls' paper (5) in which an attempt was made to fill up the lacuna in Moores' work. The significant aspects of these work are as under :-

(1) It describes a practical circuit of a PLDS implemented with an RCA CD4046 AD phase frequency detector . capable of effecting a 40:1 speed range.

(2) It presents a non linear model developed to describe the dynamic response of the control loop.

(3) It compares the response characteristics of the developed model with the measured response of the implemented system and reports th findings that the two "agree quite well".

(4) The developed and tested PLDS has a speed range from 120 RPM to 2520 RPM and speed regulation of less than.1 percent at the lower end of the range and less than .02 percent over the majority of the range.

The next importantdevelopment in this area was reported by Sinha ad Baily (6) and the emphasis herein too was on the implementation side. The major points to emerge from this work are as under:

(1) It is reported that Moores'(4) suggested circuit using an MC4004 digital phase detector could not be made to operate with the speed encoder or in fact with any pulse train.

(2) On the basis of the above findings a modified scheme was tested using an analog phase detector a NE(SE) 565 PLL deep on a 1/50 H.P. DC Servo-motor.

(3) On the basis of the test results it is reported that the regulation accuracy is within .075% at a base speed of 2500 RPM. It is further predicted that accuracies of the order of about .002% would be achievable particularly at higher speeds.

(4) The performance of the loop has been further evaluated. On the basis of two performance parameters namely fl and f_c for both modes of motor control i.e. both Armature andfield control modes.

(5) It is predicted that still higher orders of accuracy are attainable with a digital PLL using a more sophisticated design.

(6) It is further recommended that improved performance can be obtained by increasing the accuracy of the speed encodor and by eliminating the gitter in its output wave form.

Kenley and Boses' work reported in 1976(8) is perhaps the first and only attempt till yet in the application of phase Locked-Loop Techniques for effecting autatic speed regulation of relatively large sized

motors other unique features of this work are in respect of application of triacs as the controlled rectifier elements and of control of three phase Induction Motors same of the salient details reported in this work are as follows:-

(1) Experimental results of a 5 h.p., phase Locked Loop Induction motor drive system have been reported. The drive is based on the stator voltage control method using triac as the controlled rectifier elements.

The next significant work • which appeared in 1977(20) is perhaps the first theoretical work on the problem of PLDS instability at low speeds. The paper describes the operation of phase locked servo systems with the aid of a linear discrete model developed specifically for this purpose. Also discussed are the design problems speed variations and the extension of lock range, by Lag-lead net-works. In the area of stability analysis the condition under which the system remains stable has been quantitatively established. (For details please refer appendix B) on this basis an analytic expression has been derived for the lower speed limit. Also discussed are the design requirements and the main problems encountered in the design. These includes the

system bandwidth, the lock range and the speed variation of the motor.

A year later (1978) (9) Bose and Jentzen have reported a digital speed ontrol method of a rectifier fed seperately excited dc motor incorporating phase locked loop technique. The salient features of this significant experimental work are as follows:-

1. A digital speed control method based on the phase-Locked Loop technique has been described which provides the advantages of freedom from drift and offset errors, immunity of the control circuit from transients and distorsion of supply voltage andpermits integration of the control circuit.

2. The essentially digital control action is effected by comparing the reference and the feed back frequencies in the phase frequency Detector and generating therefrom an analog error signal proportional to the phase difference of the input waves at the output of the loop filter.

3. The convertor uses cosine wave crossing method, the digital version of which is generated by programming a set of Read-only Memories (ROM).

4. A complete speedcontrol system employing a DC seperately excited 3/4 hp Motor has been designedand tested

in the lab and the system gives satisfactory performance.

The principle can be extended to three phase system with higher horse-power drives or to other phase controlled convertor circuits.

OF AUTOMATED SYNCHRONIZERS

The impetus for the development of automatic synchronising equipment came from the development of static Relays. Adamson and Moslands' Work (22). was perhaps the first work in the development of Synchronizing equipment using solid state devices. However his work along with those of Humpage & Co. (23), Malik & Co. (24) and Raj Kumar and Associates (25) suffer from the following shortcomings.

1. They are all at best, only automatic check equipments for ensuring closure of circuit breaker by sensing the instant at which synchronizing is achieved within preset limits. These equipment are essentially used in conjuction with already existing manual or semi-automatic Synchronizing equipment.

2. Testing only under Laboratory conditions.

3. The comparator elements are all conventional and implemented by back dated components and techniques.

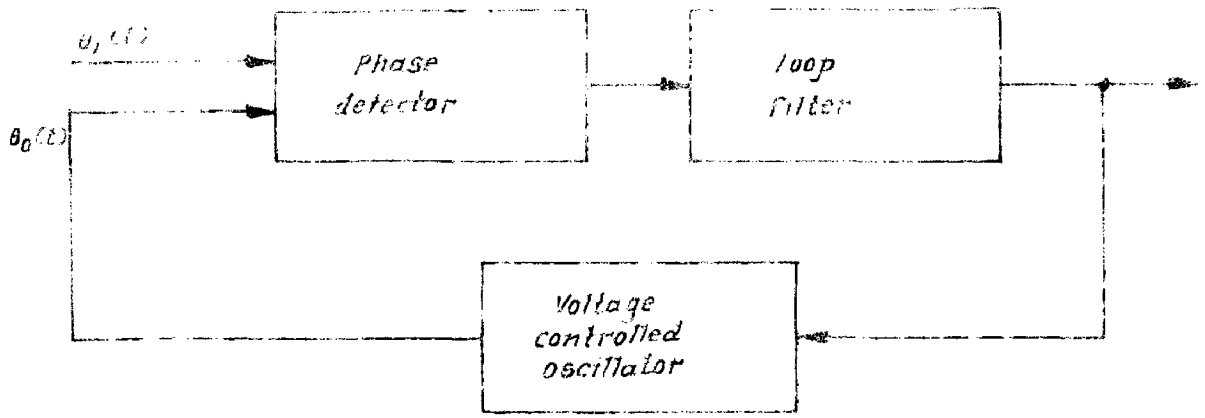


Fig. 3 Schematic diagram of the basic phase-locked loop.

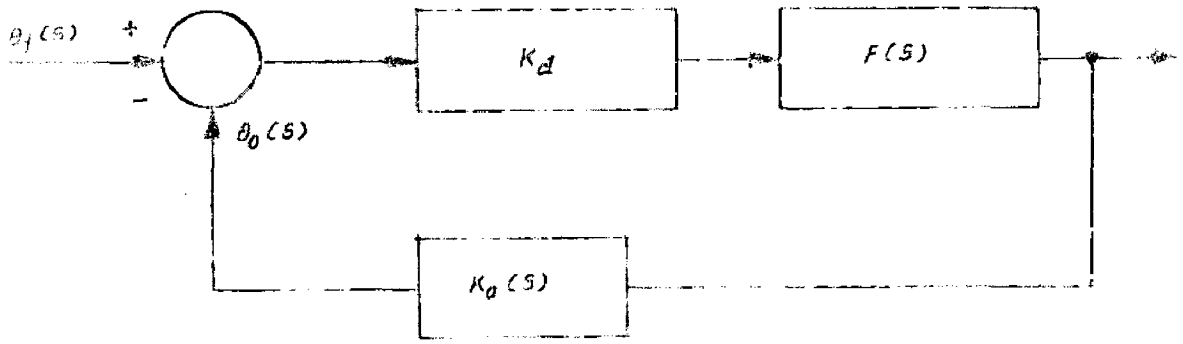


Fig. 4 Block diagram of the phase-locked loop.

CHAPTER-II

THE DEVELOPED SYSTEMS-FUNDAMENTAL CONSIDERATIONS AND DESCRIPTIONS

2.1 Introduction

PLL's havebeen used quite successfully in FM receivers, culour television, missile tracking loops space telemetry and AM demodelution. Gardner has described much of the history and potential applications of PLL's. Some of these application date back to 1930's when the systems were designed with descrete componants. These were thereforelimited to such cases where better performance would justify cost of Sophisticated Electronic circuitary for the PLL. The situation has changed considerably since then and currently PLL's are available in the form of a single IC chip at a very low cost. This has led Engineers to find areas of applications of PLL's other than in communications.

2.2 Theory of P.L.L.

Consider the schematic diagram shown in Fig.(3) The phase detector measures the phas e difference between an input voltage $v_i(t)$ and an output voltage $v_o(t)$ to give an output.

$$V_d(t) = kd\ (\theta_i - \theta_o) \qquad (1)$$

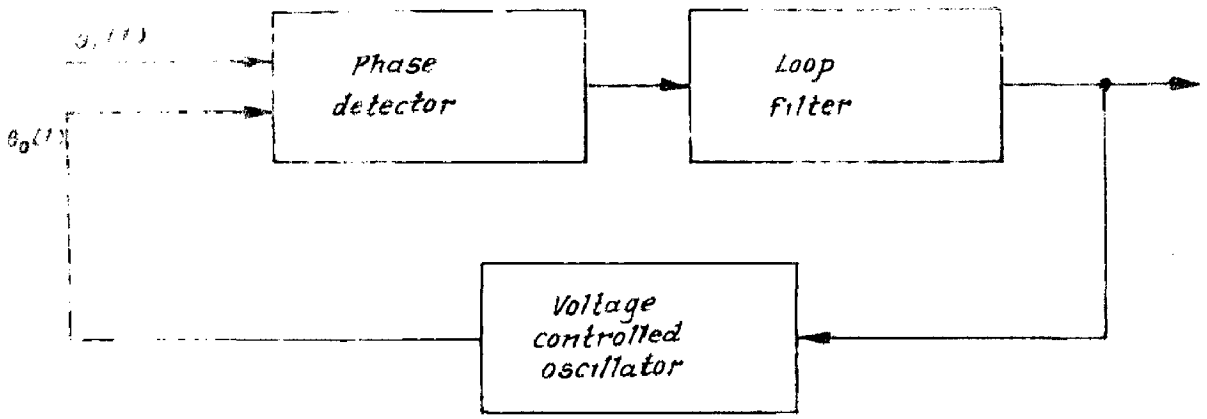


Fig. 3 Schematic diagram of the basic phase-locked loop.

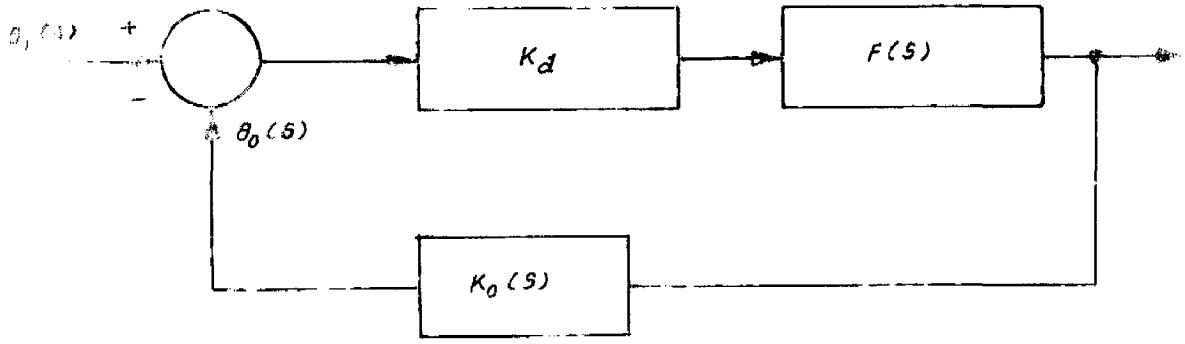


Fig 4 Block diagram of the phase-locked loop.

Where $\theta_o(t)$ is the instantaneous phase of $V_i(t)$ and $\theta_o(t)$ is the instantenous phase of $V_o(t)$.

This Error voltage is passed through a low pass filter to reduce Noise and Extraneous high frequency. components. The filtered voltage $V_f(t)$ drives a voltage controlled oscillator (VCO) and alters its frequency in such a direction as will minimize the phase error. Thechange in the frequency of the VCO output may be related to the input $V_f(t)$ through the linear equation $\Delta W_o(t) = K_v V_f(t)$ ..(2)

Since f isthe derivative of phase equation (2) may be integrated to obtain $\theta_o(t) = \theta_o(0) + \int_0^t K_o V_f(t)\, dt$.

The Loop is said to be locked when the error voltage remains steady and the frequency of $V_c(t)$ is exactly equal to that of $V_i(t)$. The block diagram of the basic loop is shown in Fig.(4). It may be pointed out that the PLL is basically a non-linear feed back control system. But by assuming that thephase detector is linear and that the loop is locked, the response of the loop can be analyzed using laplace transforms and linear system theory. These assumptions are both justified and qualified by gardner(1). The block diagram of motor speed control is shown in Fig.(2) where for the sake of simplicity the motor isassumed to have a first order transfer function. It may be noted that the VCO

has been replaced by ashaft encoder the output of which is the integral of the speed and therefore analogous to the phase. The reference input may be a periodic wave form with frequency proportional to the desired speed.

The T.F. of theloop is given by

$$\frac{W_m(s)}{\theta_i(s)} = \frac{sKF(s)}{s(1+sT_m) + KK_oF(s)}$$

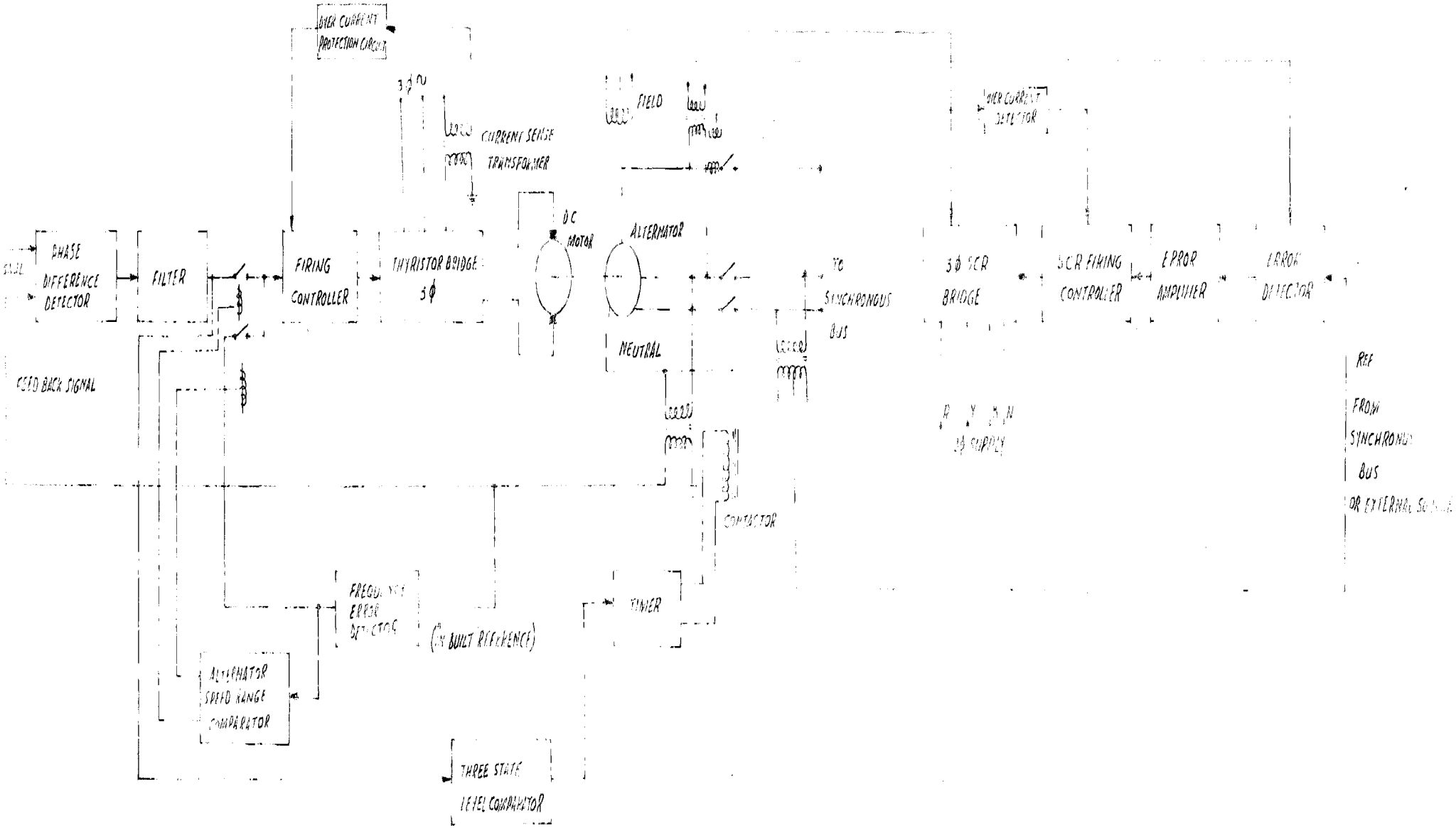
Where K: Kd KA KM = gain of forward path.

It is evident the performance of the Loop will depend considerably on the transfer function of the filter F(s). One may therefore use various methods of control system design like root locus, Bode plots, Nichols chart or other linear control system techniques to ensure that the loop will be stable as well as sensitive.

2.2 The Locked Loop Alternator Synchronizing System:

Thesystem conceived and developed in the present work has the following salient features in respect of its control action:-

1. Two independent and distinct comparators are incorporated in the developed scheme- namely the Phase difference detector and the frequency error detector for the specific purpose of achieving fully automated high precision add rapid synchronizing and having an order



IG. 5 THE PHASE LOCKED ALTERNATOR SYNCHRONISING SYSTEM - BLOCK DIAGRAM OF DEVELOPED SCHEME.

of stability considerably better than that achieved by the conventional types of phasecomparators which have been used in earlier schemes.

2. As is clear from Fig.5, these two comparators are part of two distinct loops kbe of which could be appropriately termed as the phase Locked Loop (PLL) and the other as the frequency Locked Loop (FLL).

3. This scheme is being implemented in the present work on a 5 kw alternator set driven bya DC Motor but is applicable withthe same order of precision topower station generators driven by all types of prime-movers by suitable modification in their existing speed control schemes.

4. In the present scheme as detailed in Fig.(5) the basic control action is initiated and implemented as follows:-

4.1 The DC Motor Alternator set is brought up to near about its synchronous speed by the action of the frequency Locked Loop which includes in addition to the frequency error detector,the firing controller and the three phase SCR bridge type conventor. The alternator output at reduced voltage level is used directly as the output frequency feed back signal.

4.2 With the 3 phase SCR convertor energized and firing controller supply switched on the in built' soft starting arrangement of the firing controller ensures controlled acceleration of the DC Motor through a limiting action.

4.3 The alternator set is brought up to a speed near about the synchronous speed under the exclusive influence of the frequency locked control loop.

4.4 At a preset value of speed (which is adjustable) near about the Synchronous speed (within ± 3 to 5%) which is sensed by the speed range comparator the frequency error detector is disconnected the frequency locked loop (FLL) goes out of action and is replaced automatically by the PLL whose comparator is a phase difference detector. The need for incorporation of the PLL, is justified on the following grounds.

4.3.1 It ensures perfect frequency control with an order of accuracy not at all possible by any other method or through the exclusive use of the FLL.

4.3.2 In addition it ensures perfect phase synchronizing as the PLL in herently compares the instantaneous phases and produces a proportional error signal .

4.4 The reference signal of the PLL is derived directly from the 50 Hz supply and the feed back signal is obtained from the alternator output.

5. The DC Motor controlled convertor has a built in over current protection arrangement.

6. A unique feature of the developed scheme is in respect of the arrangement provided for automatic closure of the circuit breaker conteacts connecting the incoming machine to the station bus bars. The arrangement comprises a state level comparator acting in conjunction with a timer. This arrangements operates on the premise that the contacts are closed only after it is ensured that the phase difference is within the set limits and that it is free of oscillations. The is a achieved by an automatic check arrangement which brings about the above check for a period of 4 to 5 seconds and only there after produces the energizing signal for the contractor.

7. The envisaged scheme also incorporates a closed loop static excitation system using a three phase SCR Bridge convertor and associated control circuits. The reference for this automatic voltage regulator is derived from the station bus and exercised the control is exercised by the error signal varying the SCR firing angle.

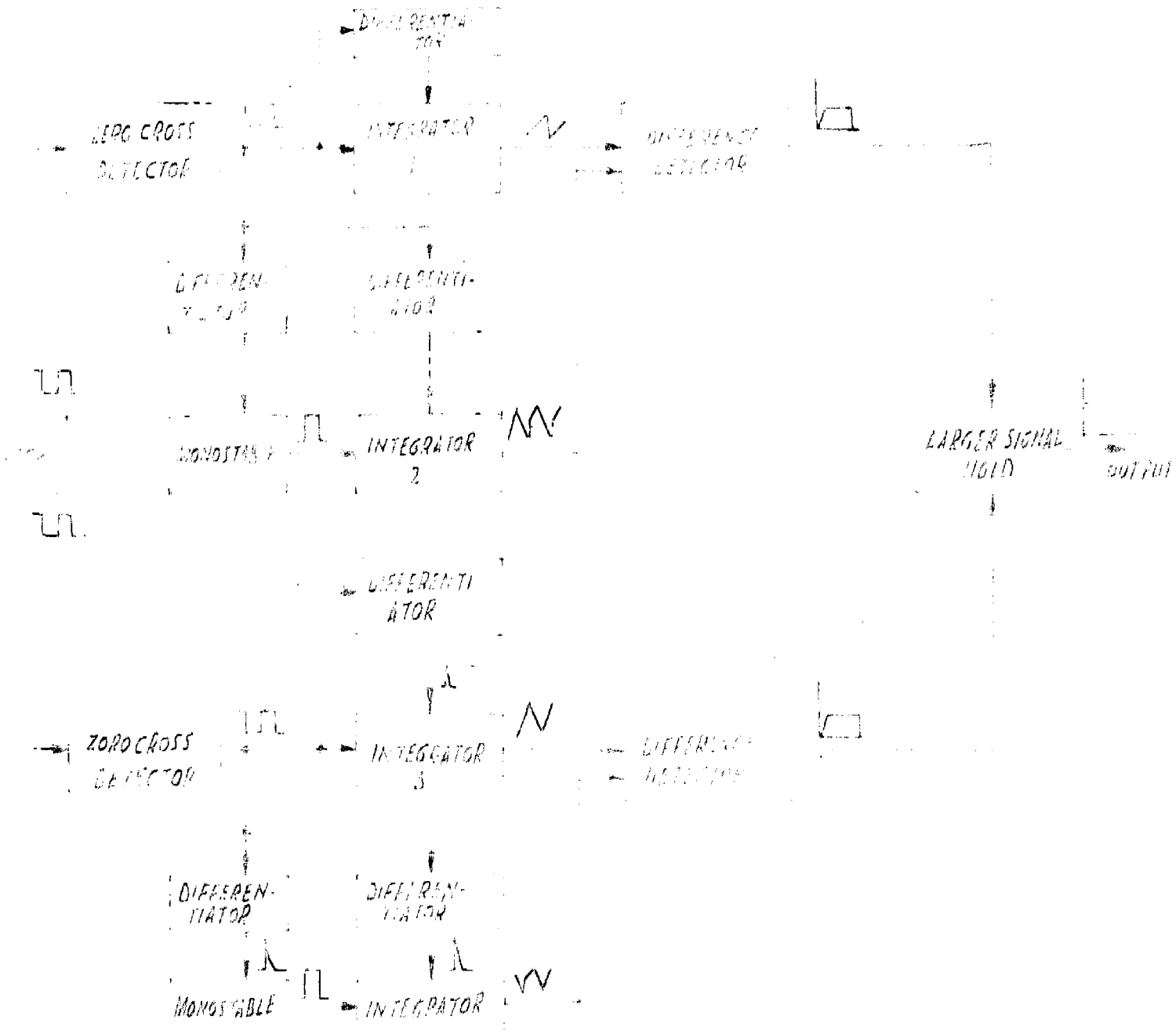


FIG. 6 BLOCK SCHEMATIC OF THE DEVELOPED FAST FREQUENCY ERROR DETECTOR.

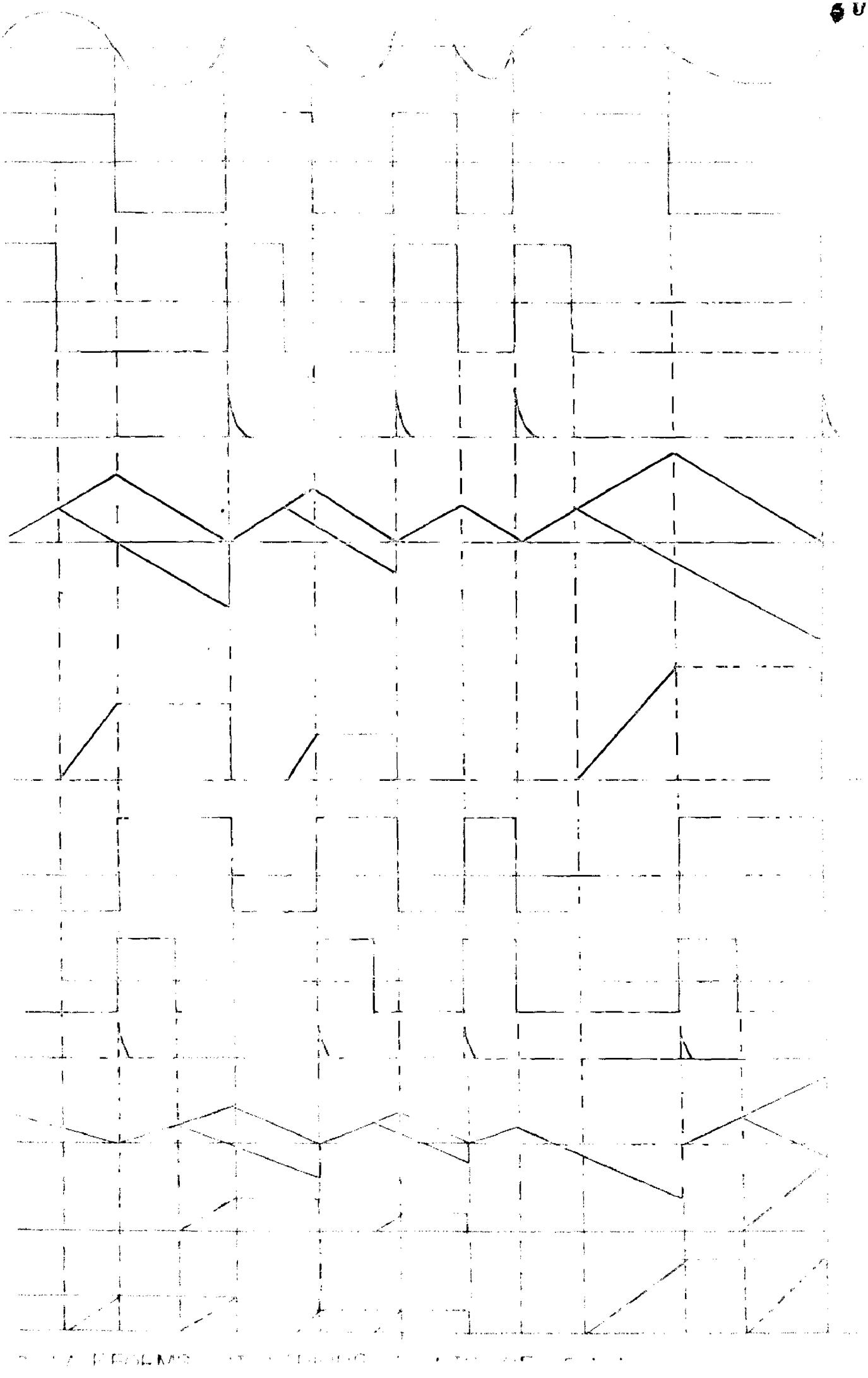
2.2.1 The Fast Frequency Error Detector:

This constitutes the main functional block of the frequency Locked Loop of the developed scheme. Its block representation is as given in Fig.(6) . It generates a DC output voltage whose magnitude is a function of the instantaneous frequency difference, of the input signals. The complete scheme could be symmetrically split into two identical portions with each part consisting of a zero-cross detector, a pair of integrators a monostable and a difference detector. The action of this complete circuit is on the following basis:-

1. The feed back signal whose frequency is to be controlled is applid at the terminal marked "Signal input in Fig.(6).

2. The instantaneous frequency difference is measured by comparing instantaneously the half cycle period of the input feed back signal and the pulse duration of the monostable output signal which acts also as the reference timeperiod and therefore as the reference frequency signal.

3. The upper half of the circuitoperates for the positive half cycle of the input signal and is responsible for generating the DC output level which is a function of the instantaneous time difference of the two

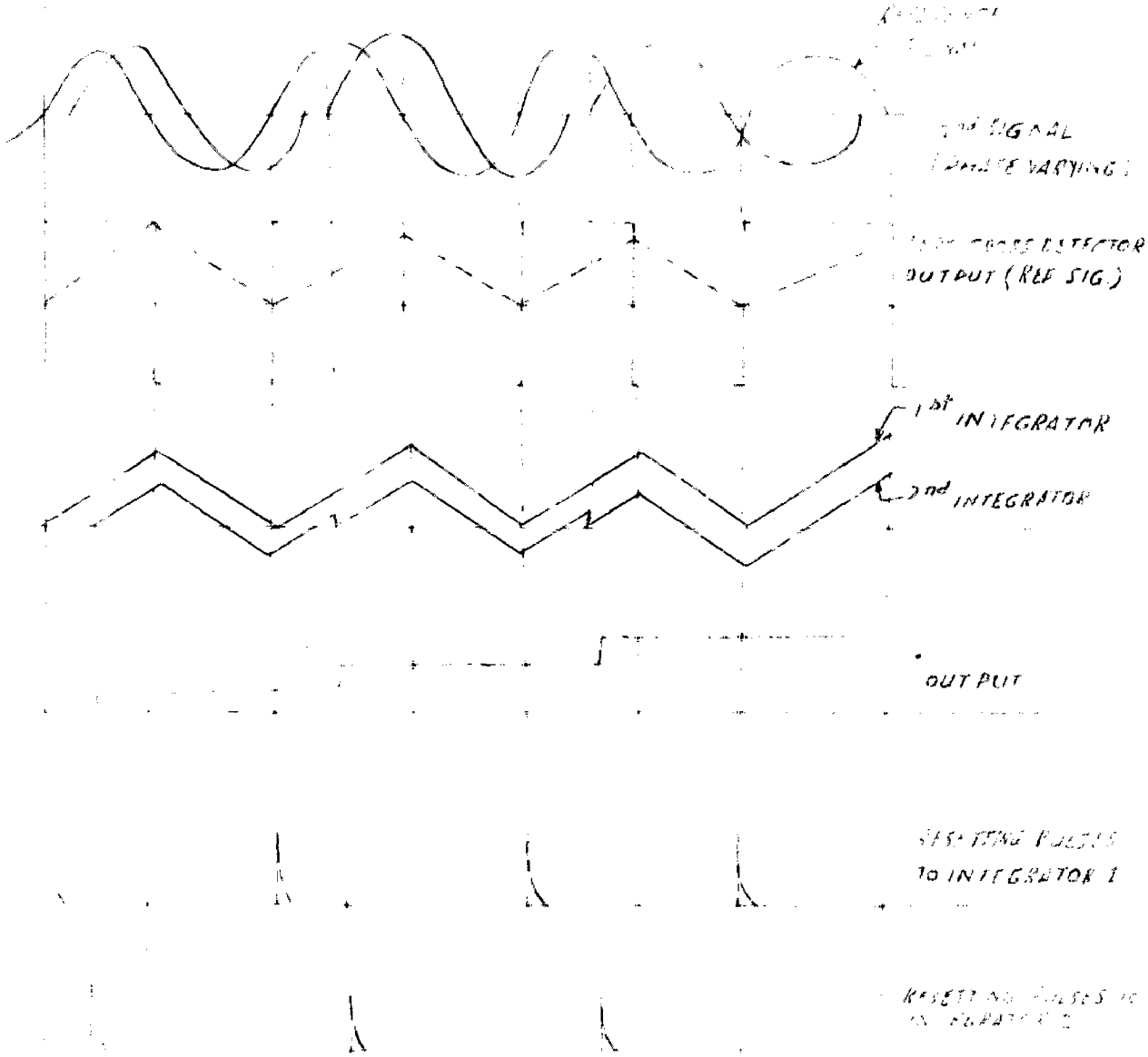


signals for one half of the input cycle. The lower half of tb the circuit operates during the negative half cycle of the Input Signal.

4. The difference detectors used are essentially differential amplifier.

5. Each half of the input signal is converted into a squarewave (refer B & G Fig.7), by the Zero Cross detector which in turn is linearly integrated (refer E and J of Fig.7) by integrator 1. At the instant of commencement of integration by Integrator 1, the monostable is triggered by pulses (refer D and I of Fig.7) and its output is as shown in C and H of Fig.(7). The monostable output inturn is integrated by Integrat 2. The outputs of each of the two integrators are fed simultaneously to the difference detector(ref. E and J of Fig.7). The output of the difference detector is a DC Voltage which is proportional function of the instantaneou difference of the two frequencies of(refer F & K of Fig.7).

6. The outputs of the two difference detectors are simultaneously fed to the larger signal hold block. At every instant the larger of the two inputs to the hold circuit appears at its output terminal(refer L of Fig.7).



WAVE FORMS AT VARIOUS POINTS OF THE PHASE COMPARATOR.

2.2.2 The Fast Phase Error Detector:

Representing the main functional block of the PLL in the developed scheme the fast phase error detector has been specifically developed to generate a linear DC output voltage Fig.3 represents the waveform diagram of the developed detector and Fig.10 the complete circuit diagram. With reference to Fig.

The reference signal and the feedback signal are given to OP AMPs Z_1 and Z_2, respectively, which act as zero crossing detectors producing square-wave outputs. Later these are converted to sharp pulses and applied at the gates of the field effect transistors. The integrators I_1 and I_2 are quenched by these respective pulses. The integrator I_2 will be quenched depending upon the relative phase position of the feed back signal (Fig.9) . The net difference of the two integrated outputs are available at the output as a dc voltage (Fig.9). Since integrator I_1 will always be quenched by its own pulse, the output voltage is proportional to the phase difference.

Salient Features:

1. The phase error detector, generates a dc output voltage directly proportional to the phase difference.

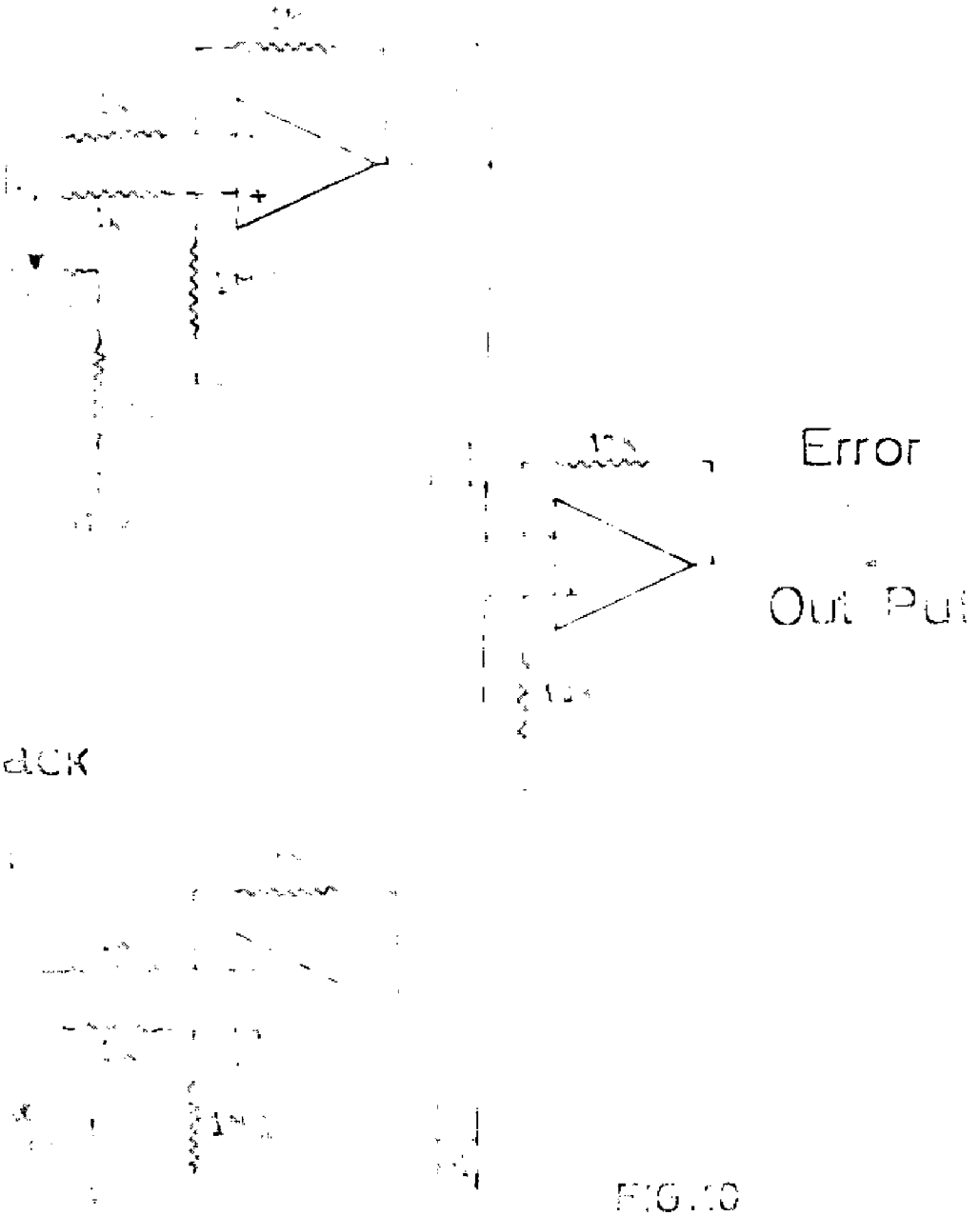


FIG.10

ASE ERROR DETECTOR

2. Since the use of a filter becomes unnecessary the response time of the PLL using this type of phase detector in a PLDS will be much less than the existing PLDS's.

CHAPTER-III

THE DEVELOPED SYSTEMS DESIGN CONSIDERATIONS AND EXPERIMENTAL RESULTS

3.1 Design Considerations:

The major design considerations which have been taken into account in the design of the various functional blocks of the developed integrated scheme are as under.

3.1.2 Of The Fast Frequency Error Dectector:

The circuit diagram of this developed detector is given in Fig.11. The frequency error detector has been designed to meet the following specifications:-

1. The response time should be the minimum possible from stability considerations.
2. The input frequency range should be of the order of 0 to 50 Hz.
3. The output voltage should be a pure DC signal whose magnitude must be a function of the instantaneous frequency difference of the input signals.

The developed frequency difference detector has been primarily evolved with a view to achieve the minimum possible response time so as to improve the overall stability of the control system. With this end in view the developed scheme samples over a half cycle period of the input frequency and is thereby an inherently more superior technique than the conventional detectors of the counter types in which response times are limited from accuracy considerations.

SALIENT DESIGN FEATURES

1. The integrators designed have been provided with "in built" Synchronized resetting facilities to ensure good repeatability.

2. The monostables havebeen designed using IC 555 timer with a view to impart to them higher stability. Higher accuracy is ensured by the use of tantalum (Low Leakage) capacitors in their timing circuits.

3.1.3 Of The Fast Phase Error Detector:

The present phase error detector was primarily designed to eliminate the basic drawbacks of large response times arising from the necessity of providing low pass filters with other types of phase detectors including all types of PLL's available in Monolithic IC form.

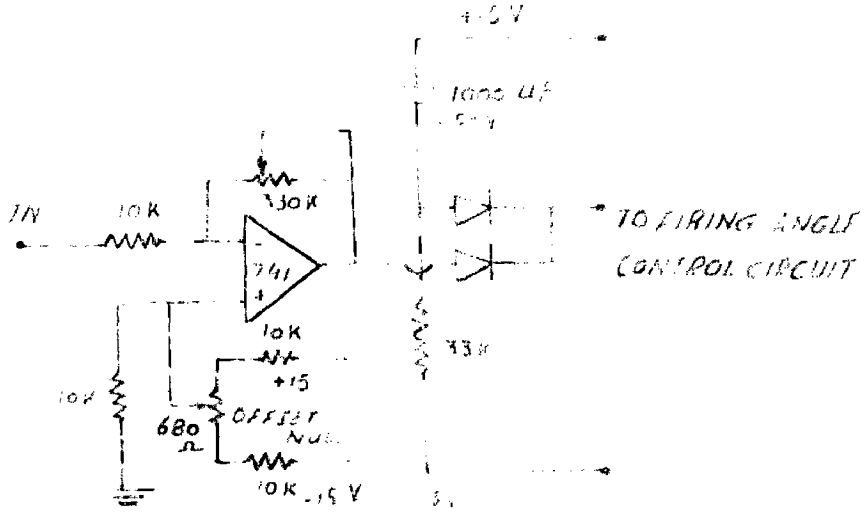


FIG. 12 STARTING AND FEED BACK AMPLIFIER CIRCUIT.

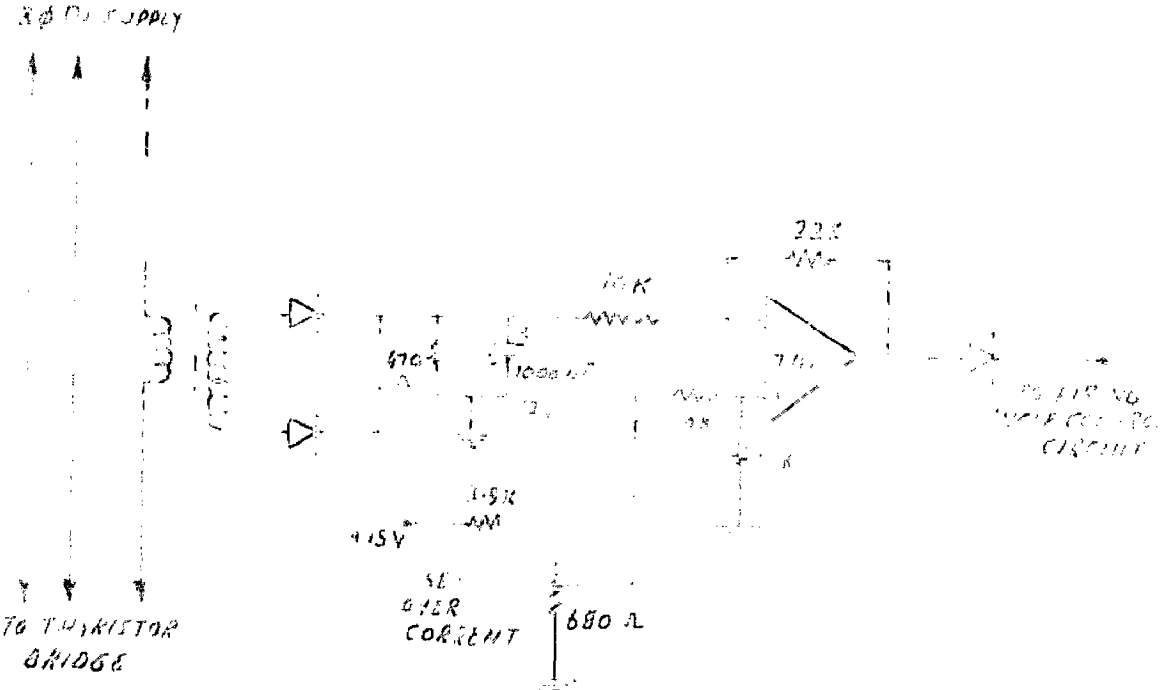


FIG. 13 CIRCUIT DIAGRAM, OVER CURRENT PROTECTION.

In all phase detetor being used till yet the necessis ty for usinglow pass filtrs basically arose from the fact that the output signals wave form was of the pulse type. The technique of phase detection developed in the present work was so altered as to ensure an output signal which was essentially a pure DC signal whose magnitude was proportional to the instantaneous phase difference, of input signal. Some of the major design consideraionof this improved type of phase detectors are as follows:-

1. The phase detection was conceivedsuch that the instantaneous phase difference was converted into the level difference of the integrators in contrast to the other types of existing comparators based on gating techniques.

2. The resetting switch for the integrators are designed with FETS from considerations of improving the switching characteristics and simultaneously maintaining the linearity of integration.

3. The integrator timing capacitors are of the tantalum (Low Leakage) types in order to improve the linearity of integraion. This is not possible withelectrolytic typeof capacitors.

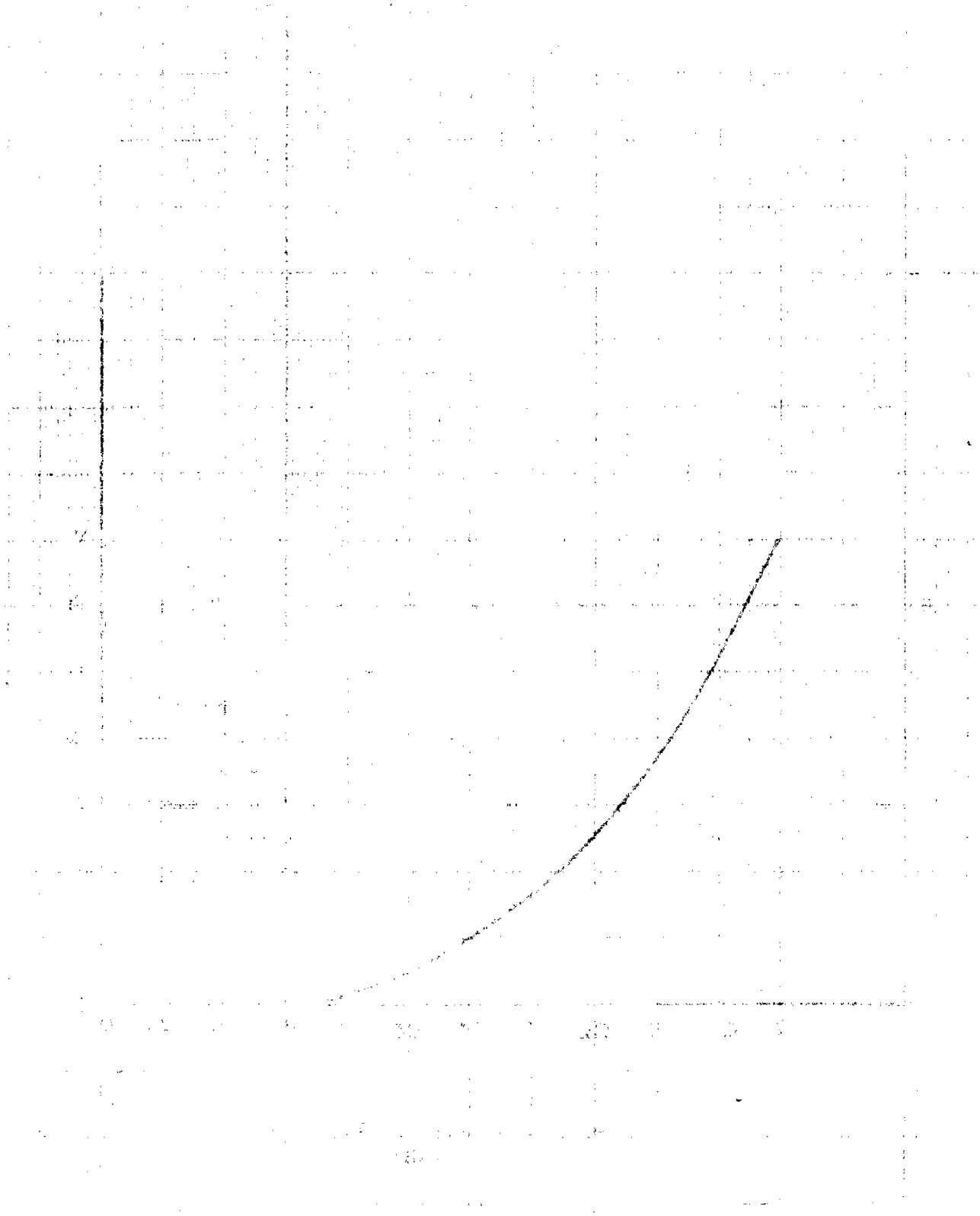


Fig 17. OUTPUT VOLTAGE VERSUS INPUT FREQUENCY

/

3.2 Experimental Results:

Frequency Error Detector

The developed frequency detector has been fully tested under Laboratory conditions. The salient aspects of the test results are as under.

1. The output response curve is as shown in Fig.17 for reference time of 10 m/seconds. This was tested by applying both Sinusoidal and square wave signals.

2. Performance Parameters Details:

Input impedance one M Ohm .

Output impedance 75 Ohm.

Frequency range 5 Hz to 45 Hz

Output voltage range 7 to 0 volts.

Supply voltage ± 15 Volts.

Phase Error Detector

The circuit was tested by using 2 sinusoidal signals. The relative phase difference was varied upto 180°. A good linear relationship was observed between the output DC voltage and the phase difference (refer Fig.18). Even when the signal contained random noises the circuit was found to be stable in operation.

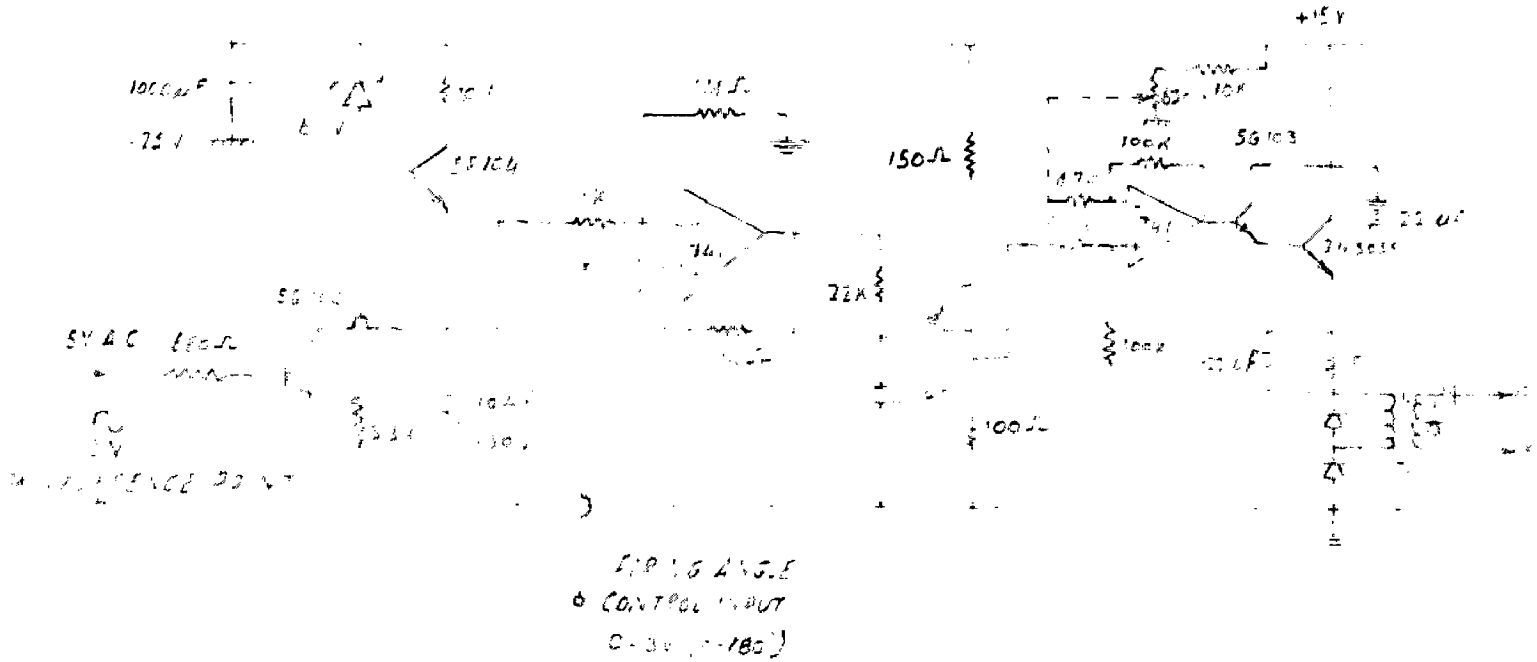


FIG 4 PULSE TRAIN TYPE OF S.C.R. FIRING CIRCUIT .

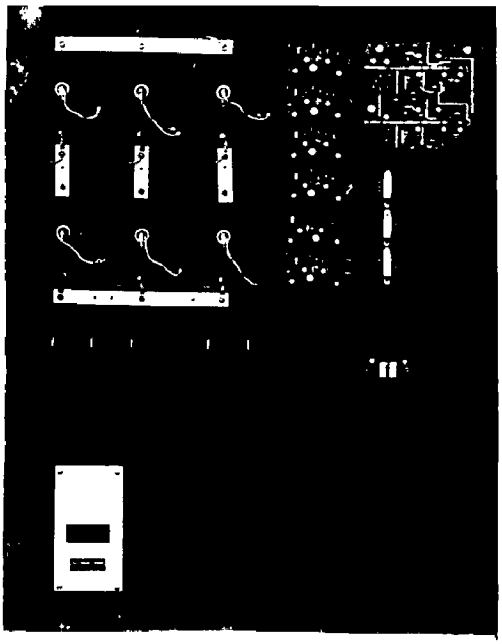


Plate 31: A view of the front panel of the "Experimental Generalized Locked Loop Drive System cum Automated Synchronizer developed at Roorkee.

Plate 32: SCR heat sinks used with the three phase fully controlled convertor of the developed ELLDS.

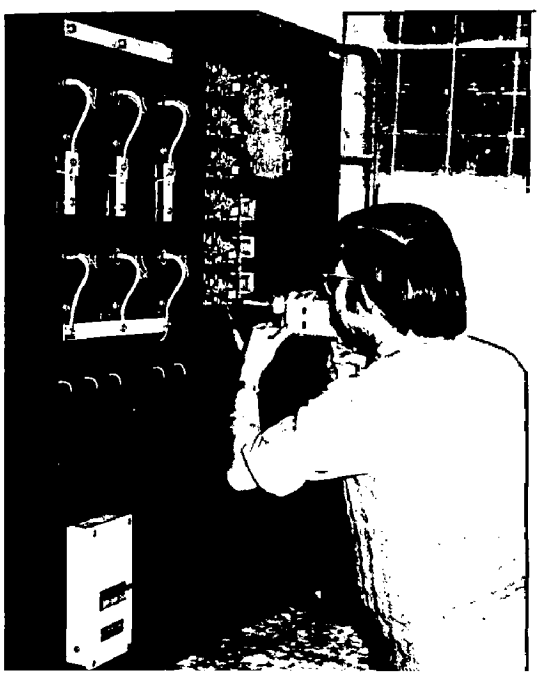
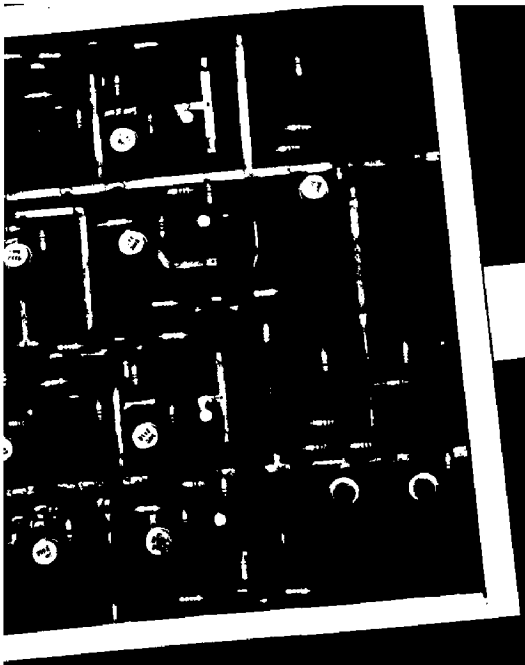
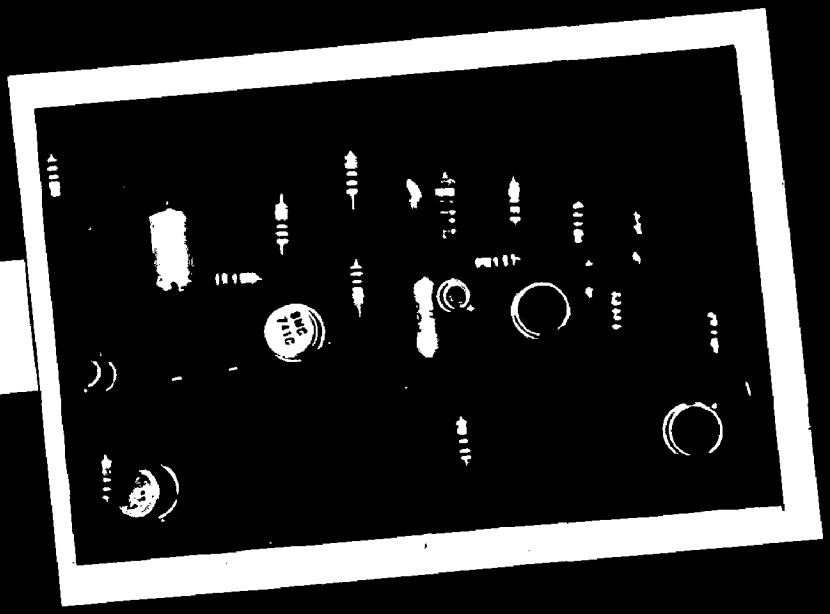


Plate:
The author at work on the control panel of the ELLDS.



Close up view of fast frequency error detector.



Close up view of s.c.r. firing circuit

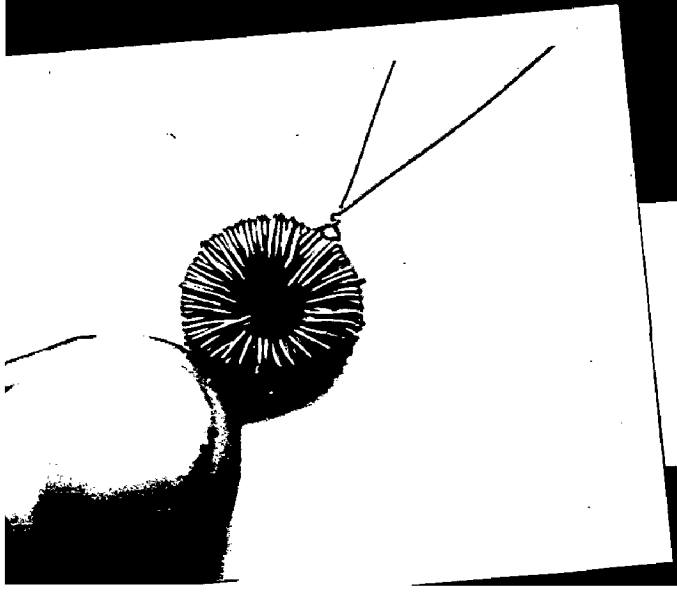


Plate 33: A close up view of the miniature pulse transformer developed for firing 40 A SCR's of ELDS.

2. Performance Parameter Details:

Input impedance 1 M- Ohm.

Output impedance 65 Ohms.

Supply voltage ± 15 volts.

Phase difference 0 to 180°.

Output voltage 0 to 3 volts.

3. Wave Form Results:

The wave forms of the various circuits and systems tested under laboratory conditions are as shown in plate Nos.19 to 30. These are in close agreement with the theoretically predicted wave forms as detailed in Chapter II.

3.3 Details Of "Experimental Generalized Locked Loop Drive Systems Cum Automated Synchronizer"

The development of the above unit was taken up in the present work with a view to create facilities for advanced experimentation in the field of precision locked loop drive systems and fully automated Synchronizers. Some of its unique features are as follows:

1. Sufficient flexibility has been "in built" into the unit so as to facilitate detailed experimental investigations on the effect of comparators on the stability of locked loop drive systems".

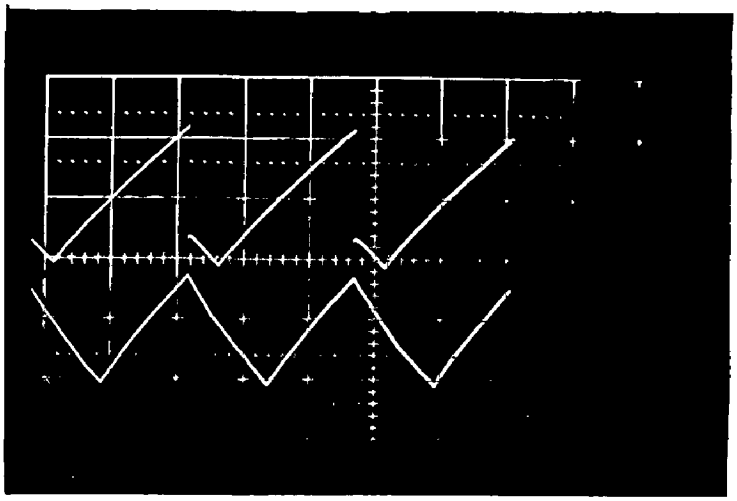
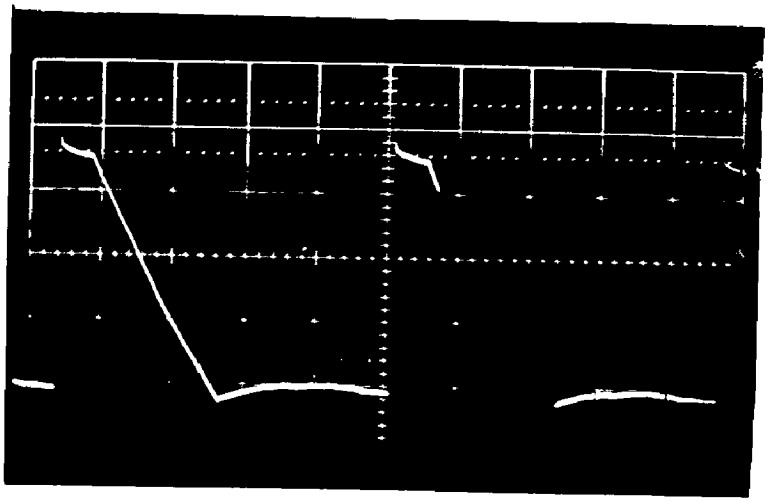


Plate 19.:Output of fast frequency error detector,integrators (upper trace of Integrator 2 & Lower of integrator 1 Horizontal scale: 10 m sec/cm vertical Scale:2V/cm per both.

Plate 20: Output of difference detector of fast frequency error detector. Horizontal scale:20 m sec/cm vertical scale 2V/cm.



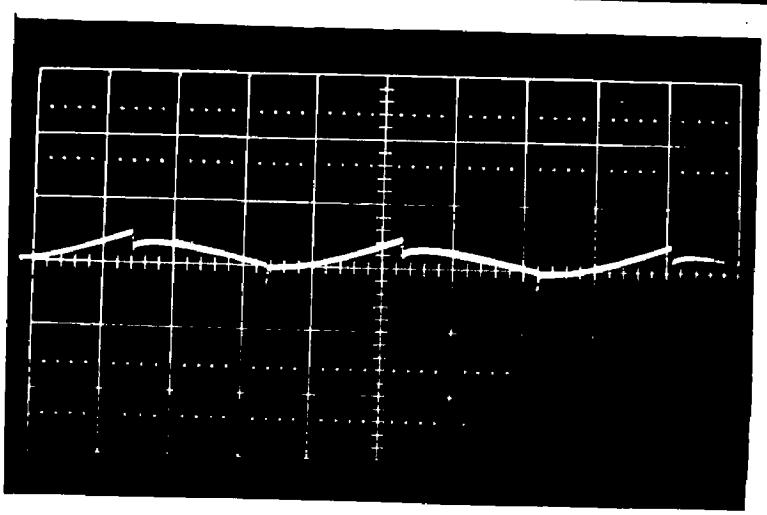
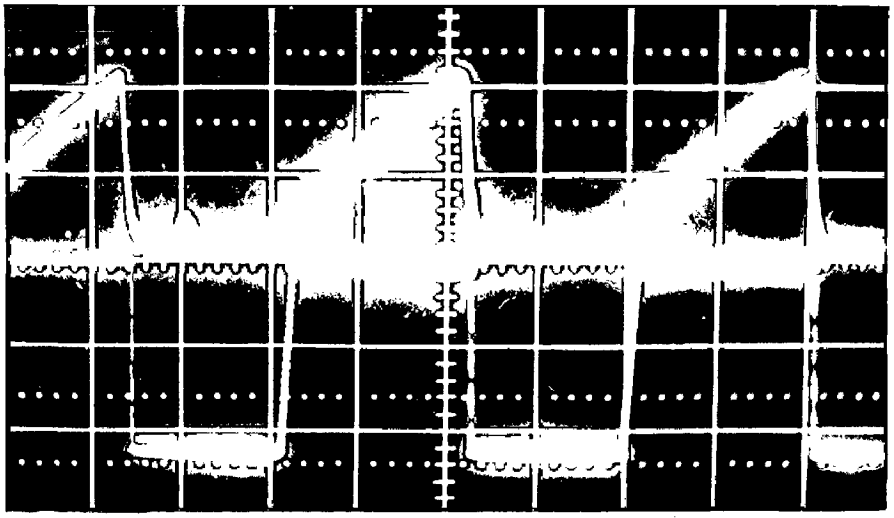


Plate 21: Final output waveform of the fast frequency error detector. Horizontal scale:20 m sec/cm vertical scale 50 mV/Cm.

Upper
Sawtooth
comparator
ce(2).Out-
mparator
l scale
.
scale



E FORMS ASSOCIATED WITH PULSE TRAIN TYPE OF SCR FIRING CIRCUIT (REFER
CUIT DIAGRAM IN FIGURE 14).

Plate 23: Upper trace
(1) Output of
comparator
Lower Trace(2)Pulse
train type of firing
pulses.
Horizontal Scale
5 msec/cm.
Vertical Scale
5V.

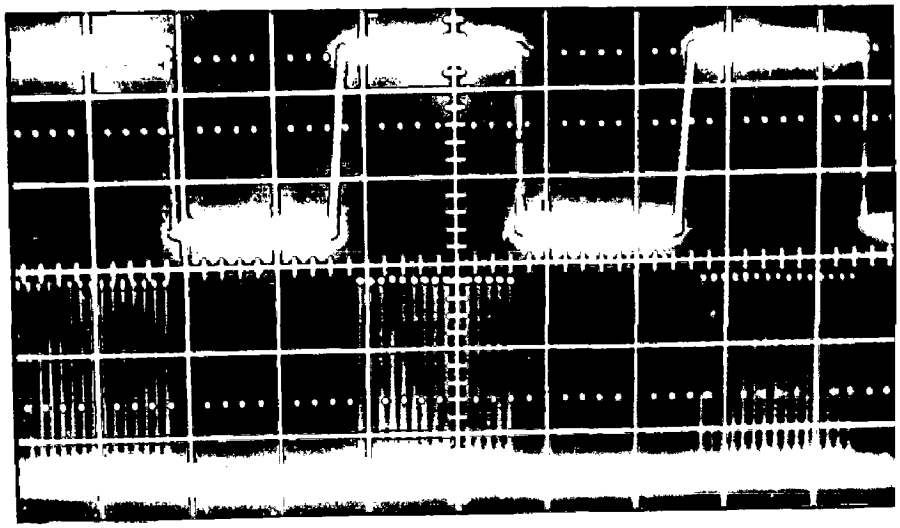
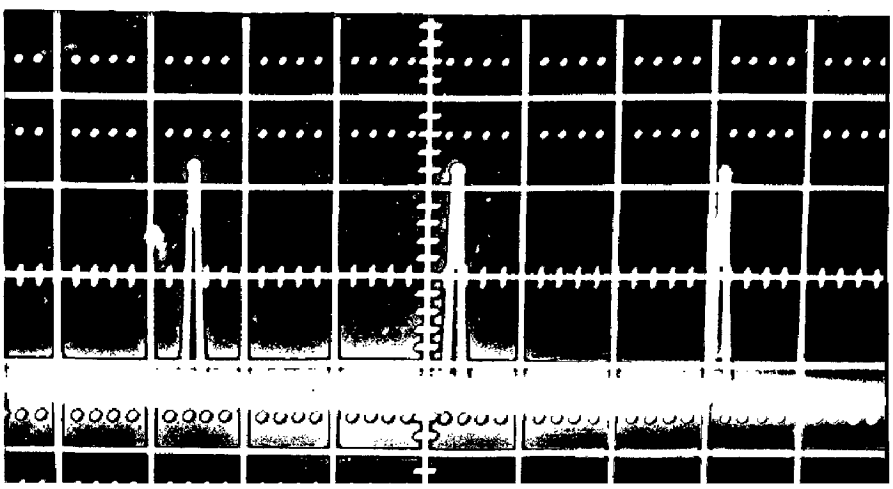


Plate 24:Expended
wave shape of firing
pulse



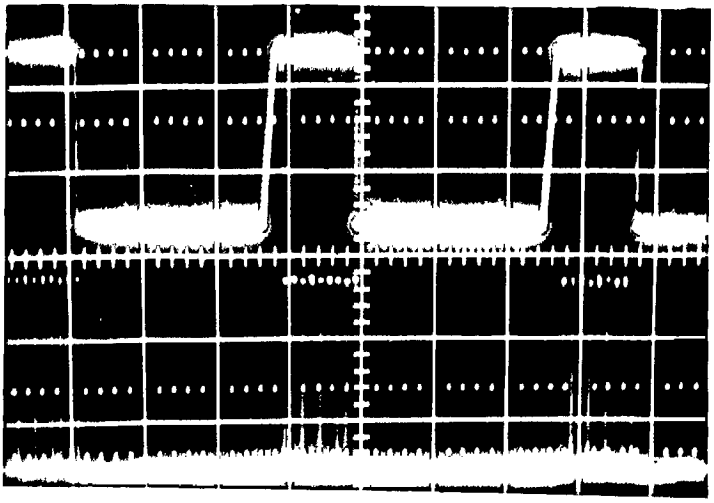


Plate 25:Upper Trace (1)Output of Comparator Lower Trace: (2)Final firing pulses at delay angle = 90° Horizontal scale 5 m sec/cm. vertical scale (1.. & .2) 5V/Cm.

WAVE FORMS FOR VARYING FIRING DELAY ANGLES OF THE PULSE TRAIN TYPE OF FIRING CIRCUIT

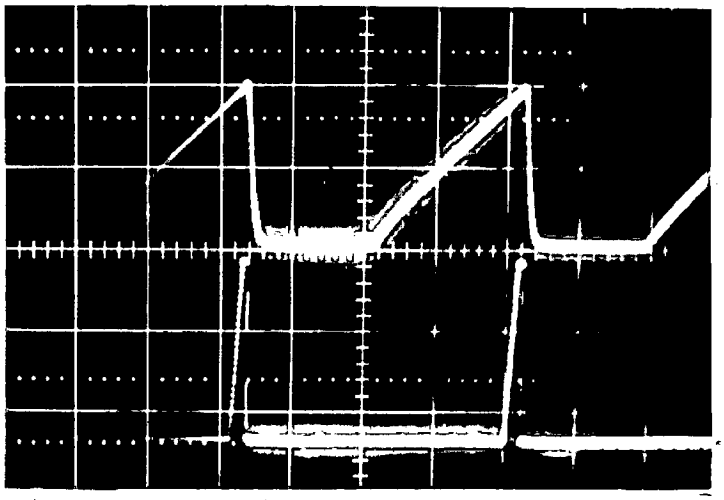


Plate 26: Upper trace (1) Sawtooth input to comparator Lower trace (2):Final firing pulses at delay angle equal to 176°(Approx.) Horizontal Scale 5msec/cm. vertical scale(1)2V/cm (2) 5V/Cm.

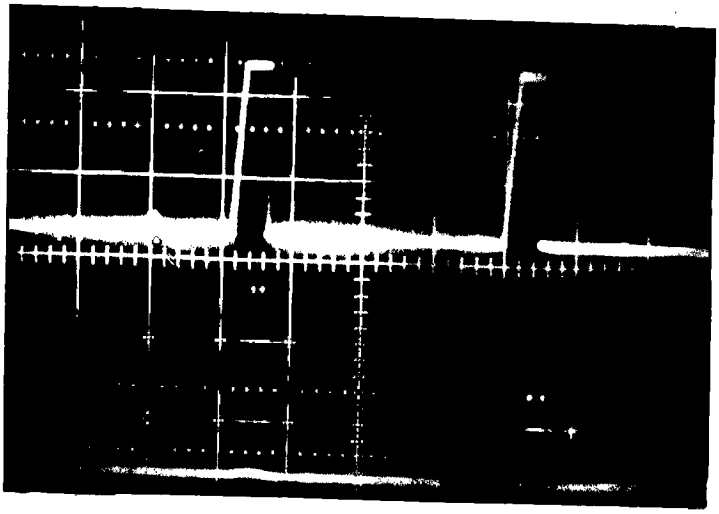


Plate 27: Upper trace (1) output of comparator Lower trace (2) final firing pulses at delay angle = 45° Horizontal scale :5 msec/cm. Vertical scale 5V/Cm.

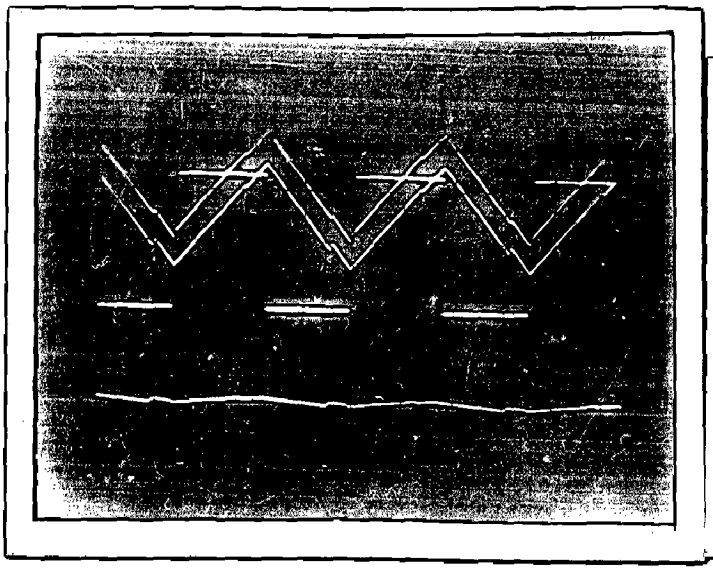


Plate 29: Output waveforms-horizontal scale 5 ms/cm.(1) output of phase detector with zero reference shown below-scale 5 V/cm.(2) Square wave inputs to I_1 and I_2- scale 10v/cm.(3)Output of I_2 and (4) output of I_1 - scale 2 V/cm.

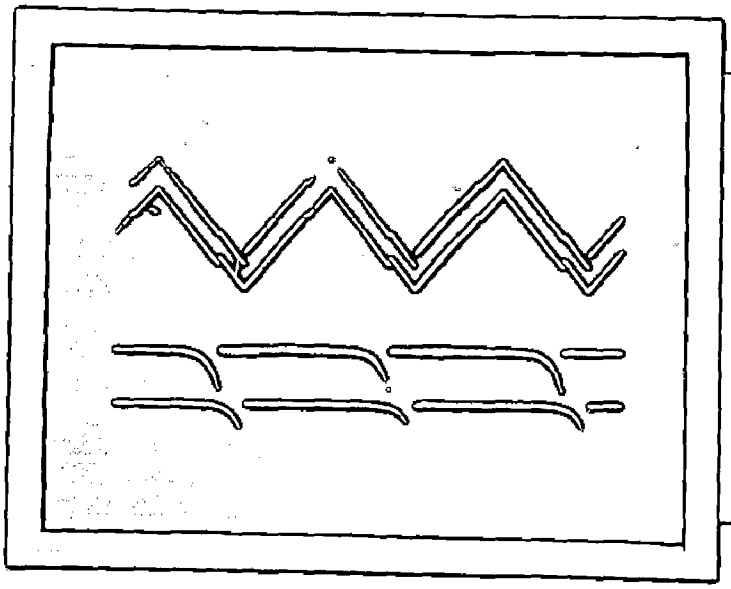
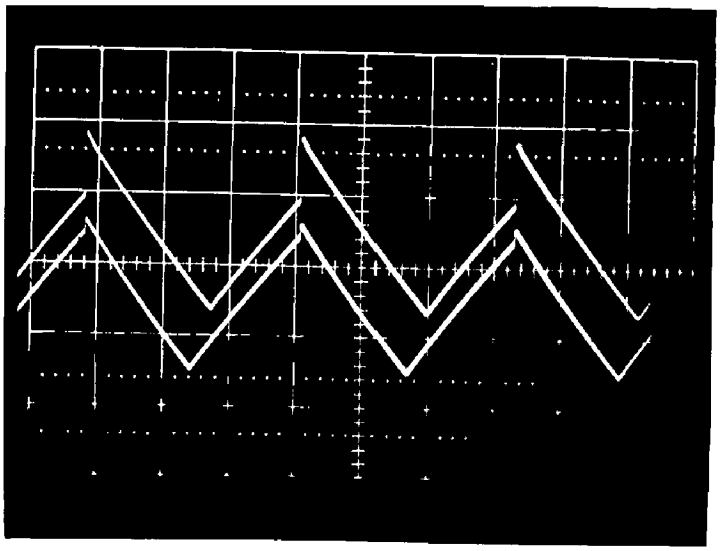


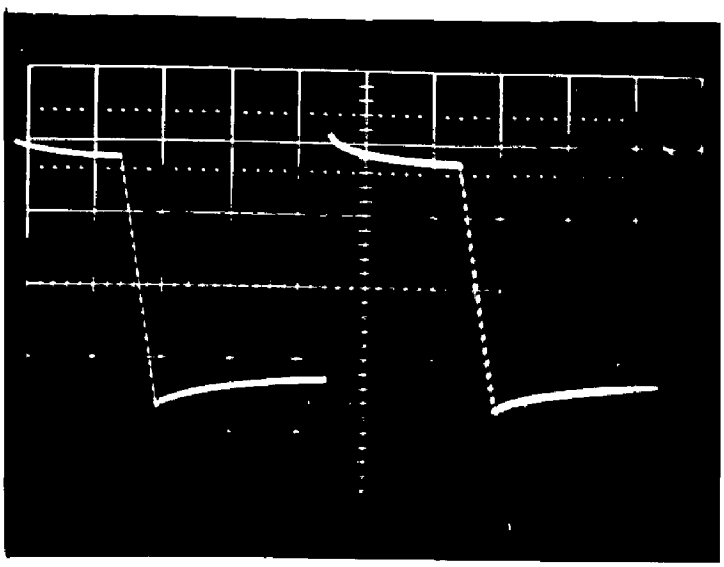
Plate No.28:

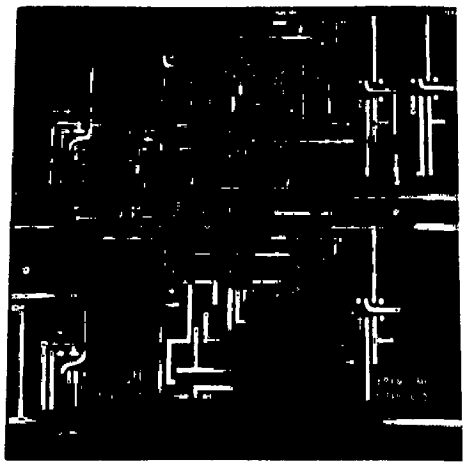
Ouputs of integrators and the quenching pulse, Horizontal scale 5 ms/cm.(1)Pulses on I_1 and (2) pulses on I_2-scale 20V/cm. (3)Outputs of I_2 and (4) output of I_1-scale 2V/cm.



Output wave shapes of the two ingegrators of the fast frequency error detector at 60Hz

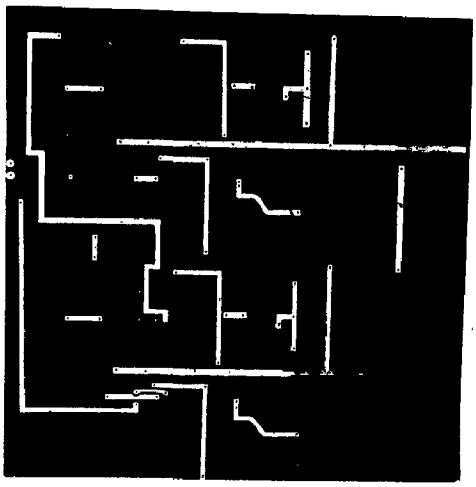
Output of Difference Detector, of Fast Frequency Error Detector. At 40Hz.





FAST FREQUENCY ERROR DETCTOR

PRINTED CIRCUIT BOARD.



2. It would permit experimental performance studies of different types of closed loop solid state drives.

3. It would open up the challenging area of detailed experimentation and development of fully automated synchronizers for power station applications.

CHAPTER-IV

C O N C L U S I O N S

4.1 Major Assetts Of the Fully Automated Dual Locked-Loop Type of Alternators Synchronizer:

With the incorporation of two independent and distinct Locked - Loops the fully automated synchronizer in-herits the following significant merits:-

1. Theelimination of PLL and its replacement by the FLL at speeds other than near about the synchronous speeds eleminates the problem of harmonic locking.

2. It improves the systems stability by minimizing the transient circulating currents.

3. It would bring out heavy reductionof the turbine foundation transient stress levels. It is of interest to note that the basic cause of these high stresses is attributable to the draw backs inherent in manual and semi-automatic synchronizing methods which are in use currently.

4. It would bring about considerable reduction of the transient during the synchronizing operation these in turn would ensure the following improvements and advantages.

4.1 It would eleminate considerably the possibility of grid failures arising from imperfected synchronizing operation.

4.2 It would lead to a definite increase of the power capacity of the existing power systems by increasing the transient stability limit.

4.3 By in-corporating such Synchronizers there would considerable economy in the design of the transmission system.

4.2 Specific Recommended Application:

With overall system stability considerably improved the high precision Locked Loop Drive Systems are admirably suited for the following applications:-

1. As fully automated Synchronizers in Power stations.

2. For all drive applications demanding extremely high precision specifications- .2% to less than .002% regulation.

3. For all drive applications requiring automatic Synchronizing of Large Number of Motors with respect to each other.

4. For all drive applications requiring automatic Synchronizing of a motor to an existing clocking pulse train.

4.3 Some Specific Application Areas:

1. Computer peripheral drive such as a disc unit.

2. As a conveyore drive for materials handling

3. A reel to reel tape drive.

4. In fully automated high precession and high pressure misting systems for controlled enviornment ecological systems.

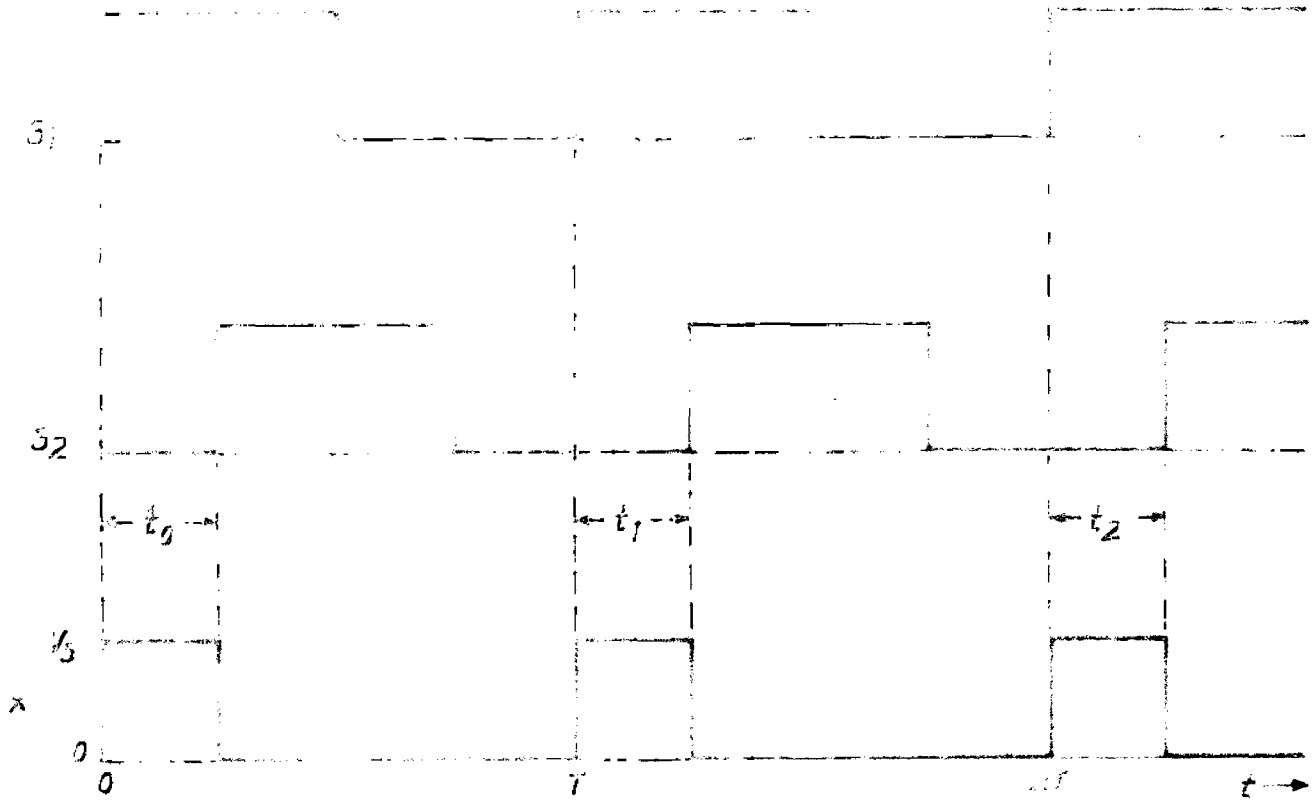


Fig. A1. The inputs S_1 and S_2 of PFD and the output x.

APPENDIX A

LINEARIZED MODEL FOR PFD

The objective of this section is to derive a linearized model for the PFD under locked condition and constant reference frequency.

Assume, with no loss of generality, that the reference signal, S_1 , leads the feedback, S_2. The output x of the PFD will be V_s during the time interval between the leading edges of S_1 and S_2 as illustrated in Fig.A1.

The phases θ_1 and θ_2 of S_1 and S_2, respectively, are:

$$\theta_1 (kT) = 2 \pi k \qquad (A1)$$

$$\theta_2 (kT + t_k) \; 2 \pi k \qquad (A2)$$

Denote

$$\theta = \theta_1 - \theta_2 \qquad (A3)$$

The PFD output is

$$x = \begin{cases} V_s & KT < t \leq kT + t_k \\ 0 & \text{elsewhere} \end{cases} \qquad (A4)$$

Now suppose that the system operates around a nominal value of $\theta + \Omega + \delta\theta$ (A5)

Since the reference frequency is constant, (A5) can occur only if a change occurred in θ_2:

$$\theta \rightarrow \theta_2 - \delta\theta \qquad (A6)$$

This will result in a change in the duration of the output pulses,

$$t_k \rightarrow t_k + \delta t_k \qquad (A7)$$

and a change in the output,

$$x \rightarrow x + \delta x \qquad (A8)$$

The method to be used here is to determine the relationship between δx and $\delta\theta$. The relationship constitutes the linearized model of the system. Note that the new pulsedurations are such that (A2) must hold. Thus,

$$\theta_2(kT + t_k + \delta t_k) - \delta\theta(kT + t_k + \delta t_k) = 2\pi k \qquad (A9)$$

Since $\delta\theta$ and δt are very small, we can expand (A9) by Taylor series and retain the first order terms.

$$\theta_2(kT+t_k) + \frac{d\theta_2}{dt}(kT+t_k)\delta t_k - \delta\theta(kT+t_k) = 2\pi k \qquad (A10)$$

Simplify according to (A2), and note that

$$\frac{d\theta_2}{dt} = w \qquad (A11)$$

Equation (A10) becomes

$$w(kT+t_k)\delta t_k - \delta\theta(kT + t_k) = 0 \qquad (A12)$$

or

$$\delta t_k = \frac{\delta\theta(kT+t_k)}{w(kT + t_k)} \qquad (A13)$$

Since the frequency is nearly constant, we can write

$$\delta t_k = \frac{1}{w}\,\delta\theta(kT+t_k) \qquad (A14)$$

Then the resulting change in x is a pulse of duration δt_k.

$$\delta x = \begin{cases} V_s & kT + t_k < t \leq kT + t_k + \delta t_k \\ 0 & \text{elsewhere} \end{cases} \qquad (A15)$$

Since δt_k is very small, we can approximate the series ofpulses of (A15) by a series of impulses of the same area. Note that the area, A, of each pulse is:

$$A = V_s\,\delta t_k = \frac{V_s}{w}\,\delta\theta\,(kT + t_k) \qquad (A16)$$

$$\delta x = \frac{V_s}{w} \sum_{k=0}^{\infty} \delta\theta(kT + t_k) \, \delta(t - kT - t_k) \qquad (A17)$$

Note that if the frequency is constant, t_k is constant, and we an can shift t to eliminate t_k in (A17). Also mote that $w = 2\Pi / T$. Therefore,

$$\delta x = \frac{V_s T}{2\Pi} \sum_{k=0}^{\infty} \delta\theta(kT) \, \delta(t-kT) \qquad (A18)$$

Thus, the linearized model of the PFD is the sampling of θ by a train of impulses of weight $V_s T/2\Pi$.

APPENDIX - B

STABILITY OF THE PLS

Given the characteristic equation (13).

$$z^2 + z\,(-1\,B - BC + C) + B = 0 \qquad \text{(B1)}$$

In order to determine the stability, use the transformation.

$$z = \frac{\lambda + 1}{\lambda - 1} \qquad \text{(B2)}$$

This transforms the inside of the unit circle, $|z| < 1$,

$$C(1 - B)\,\lambda^2 + 2\,(1-B)\,\lambda + 2(2 + 2B + BC - C) = 0 \qquad \text{(B3)}$$

In order for the roots of (B3) to be in the LHP, all the coefficients in (B3) must have the same sign. Furthermore, as $(1 - B)$ is always positive, we require the last term to be positive, too.

$$2 + 2B + BC - C > 0 \qquad \text{(B4)}$$

This can be written as

$$C(1-B) < 2(1 + B) \qquad \text{(B5)}$$

or

$$C < \frac{2(1 + B)}{1 - B} \qquad \text{(B6)}$$

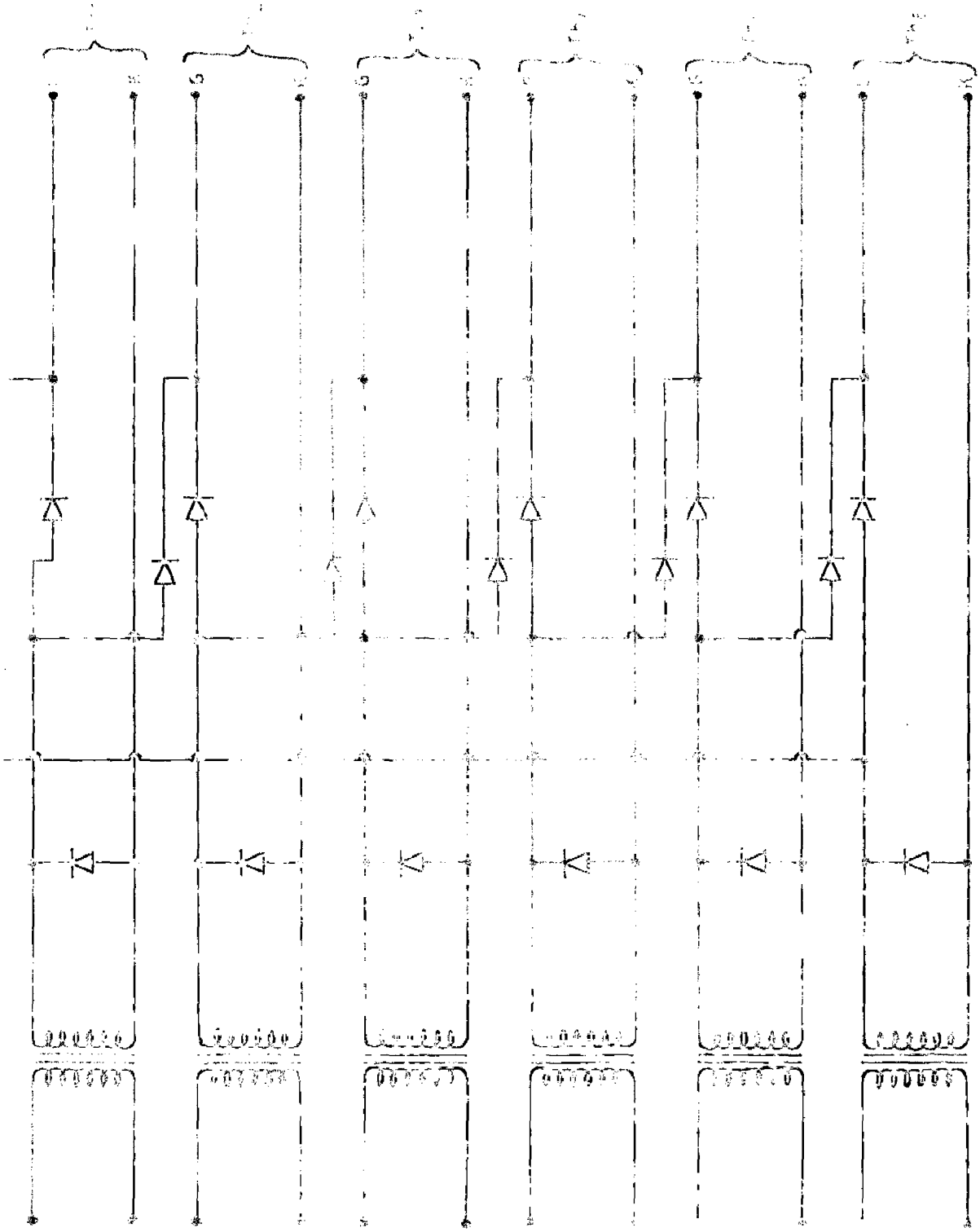


FIG. 15 PULSE TRANSFORMER OUTPUT CONNECTIONS.

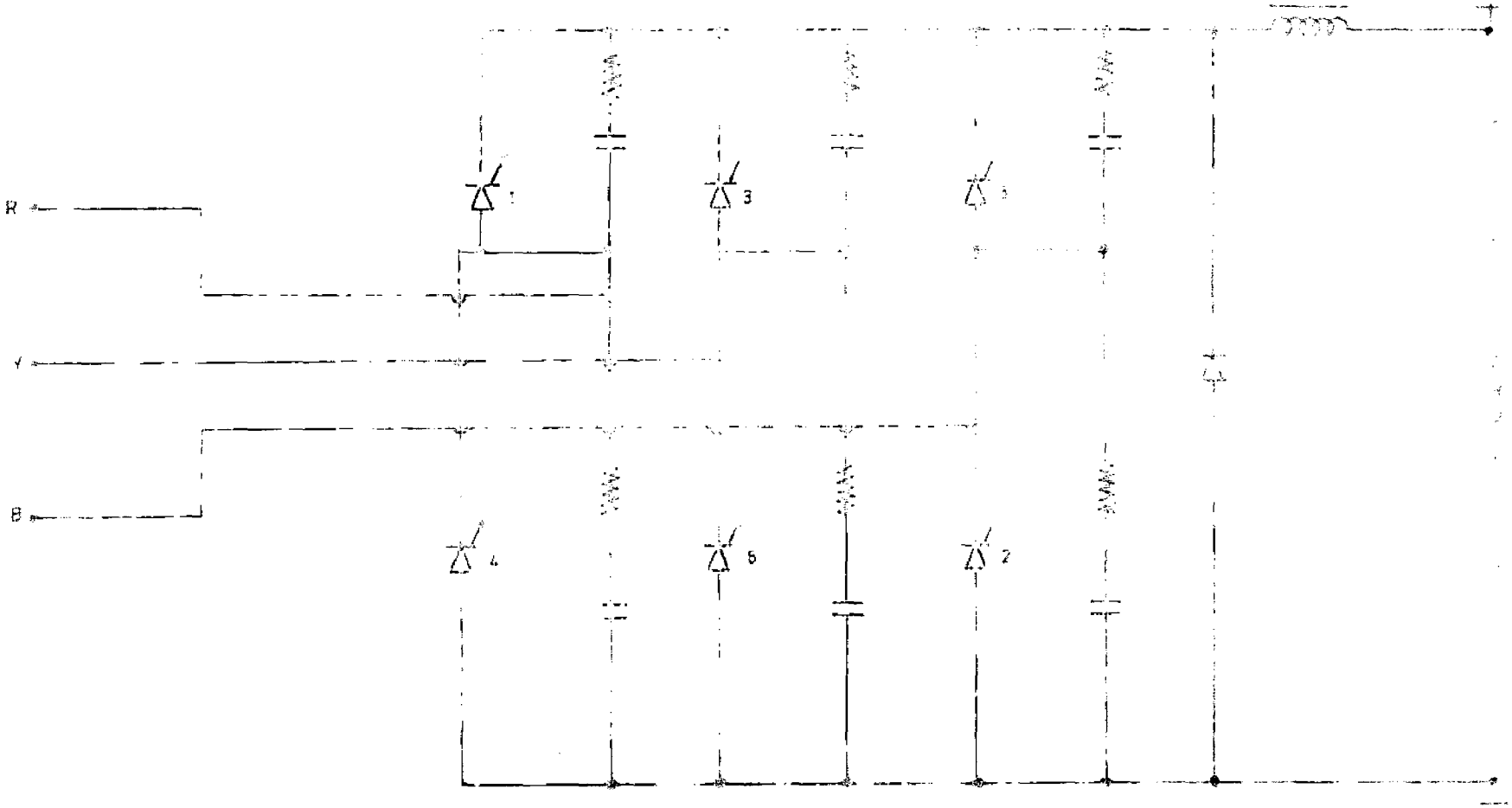


Fig. 16 THREE PHASE THYRISTOR BRIDGE FIRING SEQUENCE 1,2,3,4,5,6 .

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