DESIGN AND FABRICATION OF HIGH FREQUENCY CARRIER MULTIPARAMETER TELECONTROL

A DISSERTATION

Submitted in partial fulfilment of the requirements

for the award of the degree

of

MASTER OF ENGINEERING

in

ELECTRICAL ENGINEERING

by

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C E R T I F I C A T E

Certified that the dissertation entitled " DESIGN AND FABRICATION OF HIGH FREQUENCY CARRIER MULTIPARAMETER TELECONTROL " which is being submitted by Terlochan Singh Bhatti in partial fulfillment for the award of Degree of Master of Engineering in Electrical Engineering (System Engineering and Operation Research) of the University of Roorkee, is a record of the student's own work carried out by him under my supervision and guidance. The matter embodied in this dissertation has not been submitted for the award of any other degree or diploma.

This is further certified that he has worked for a period of 8 months from January 1978 to August 1978 for preparing this dissertation for the Master of Engineering Degree, at this University.

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SYNOPSIS

In a communication system or a remote control system sometimes it is impossible to connect the two systems by wire links, may be due to some environmental conditions or other reasons. For example, communication between stationary and mobile object such as ship to shore, from ground to aircraft, from ship to ship or from aircraft to aireraft or between satellites (known as space communication), the control of mining machinery from outside and there are other numerous examples where the communication between the two systems by wire links is impossible. In all such cases the radio communication by wireless is the only alternative.

A digital multiplexing technique for four channels has been designed fabricated and tested for transmitting four parameters of a d.c. shunt motor on a 1 W, 1 MHz A.M. transmitter. Similarly a digital demultiplexer has been designed fabricated and tested for displaying the four signals, the exact replica of the input signals, on a digital display. The whole system is designed and fabricated by using the third generation technique i.e. integrated circuit technology. Lastly for transmitting a large number of signals over a certain distance it will be definitely cheaper than the other systems and also more reliable.

A C K N O W L E D G E M E N T

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Terlochan Singh Bhatti

TERLOCHAN SINGH BHATTI

C O N T E N T S

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CHAPTER - 1

INTRODUCTION

Transmission of intelligence by radio is based on modulation. Modulation is a process by which the message to be transmitted is superimposed at the sending end of a radio link as a modulating signal (or simply, the signal) on a strong carrier wave, thereby changing the latter's amplitude, frequency or phase. The modulated carrier is radiated by a transmitting aerial as a wave of electromagnetic energy which propagates through space at the velocity of light.

At the point of reception the modulated wave is picked up by a receiving aerial and is fed to the receiver input. In the receiver, the signal is separated from the radio-frequency carrier and drives the receiver load, which may be a speaker, a recorder, a cathode-ray tube etc.

As an electro-magnetic wave travels away from the transmitter it is weakened or attenuated. This is why radio receivers should be capable of picking up relatively weak signals.

At present, radio serves a variety of purposes, such as communication, broadcasting, navigation, radar, and telecontrol.

Radio communication is the transmission and reception of messages without wires or wave guides. It includes communication by radio telegraph, radio telephone, radio teletype writer and television. It is the only method of communication between stationary and mobile objects (such as from ship to shore, from ground to aircraft, from ship to ship or from aircraft to aircraft and more recently from ground to satellites or from satellites to ground, and between satellites, known as space communication).

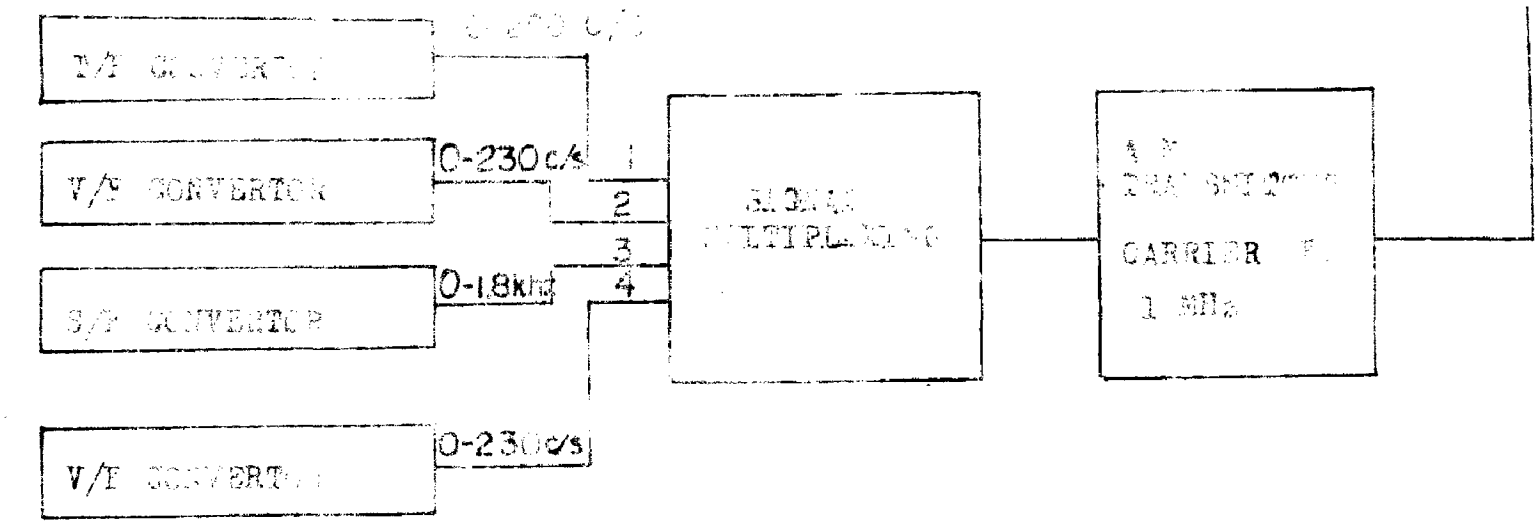
Radio broadcasting is radio transmission for general reception, including speech, music and commercial television.

Radio navigation is the use of radio facilities for determining the position or direction or both of ships or planes.

Radar (which is an acronym for Radio Detection and Ranging) is a technique for determining the range and bearings of objects (usually called targets) by the transmission of beamed high power signals against reflective targets, the reception of the reflected signals, and the presentation of the resultant data on a dial or a cathode ray display. Radar may be used for marine navigation, gun (fire) control, earth surveillance from the air etc.

Telecontrol is a technique for control of machinery by radio. It is the process by which a measurement of a quantity is transferred to a remote location to be recorded, to be displayed, or to actuate a process. Radio-frequency telemetry utilizes a radio wave type of carrier to transmit information from one location to another. The wireless telemetry uses a transmitter which transmitts the measured data or signal and displayed, recorded or controlled from the receiving end. It eliminates all cable connections as with the case of remote control, since, in some cases we are restricted to use cables for transmitting data from one place to the other place e.g. flight test of aircraft and missiles etc.

We can transmit only one signal at a time on the transmitter. What if a number of signals has to be transmitted, there must be some arrangement such that at the receiving end we can again get the same signals separately from one receiver. A multiplexer solve this problem. Multiplexing is a technique in which data from several signal sources (or channels) are combined in a prescribed orderly fashion onto a single line. A digital multiplexer has been designed which is a circuit that serially switches a number of different digital signals onto a single line or channel. Similarly a De-multiplexer is needed at the receiving end to convert the output of the receiver into the different signals that has been transmitted.


0-230c/s
0-230c/s
0-18kHz
0-230c/s
1
2
3
4
CARRIER
1 MHz

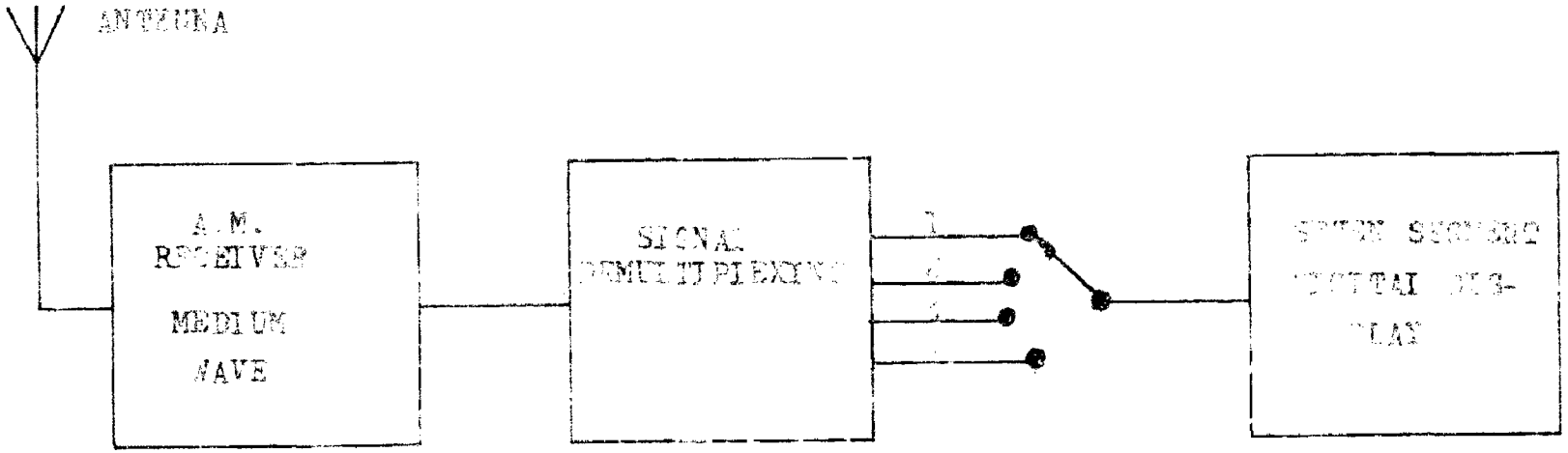

ANTENNA
A.M.
RECEIVER
MEDIUM
WAVE

FIGURE - 1

The Multiplexer and the De-multiplexer employ gates viz. OR, AND, inverter and shift registers, Astable multivibrators, monostables and a comparator. The output of an OR assumes the 1 state if one or more inputs assume the 1 state. The output of an AND assumes the 1 state if and only if all the inputs assume the 1 state. The output of an inverter circuit takes on the 1 state if and only if the input does not take on the 1 state. A group of cascaded flip flops used to store related bits of information is known as a register. A register that is used to assemble and store information arriving from a serial source is called a shift register. The schematic block diagram is shown in the figure 1. The t/f converter transducer is a temperature to frequency converter which senses the temperature of the motor and gives a corresponding digital signal. The sensor employs six silicon diodes. The v/f converter transducer converts voltage across the armature of across the shunt field into a corresponding digital electrical signal. The s/f converter transducer is a speed to frequency converter. It employs a photo-transistor with a rotating disc containing hole as a sensor.

The four signals are then fed to a multiplexer. The output of the multiplexer is transmitted by a 1 W, 1 MHz. A.M. transmitter. This whole comprises a one unit called a multichannel signal transmitting system.

The signal transmitted is received by a medium wave superheterodyne receiver tuned maximum at 1 MHz. The receiver output is fed into a De-multiplexer. The De-multiplexers output are the same signals which are fed to the multiplexing system. The output is connected through a band switch to a 4-digit digital display. This whole is called a multi channel signal reception and display system.

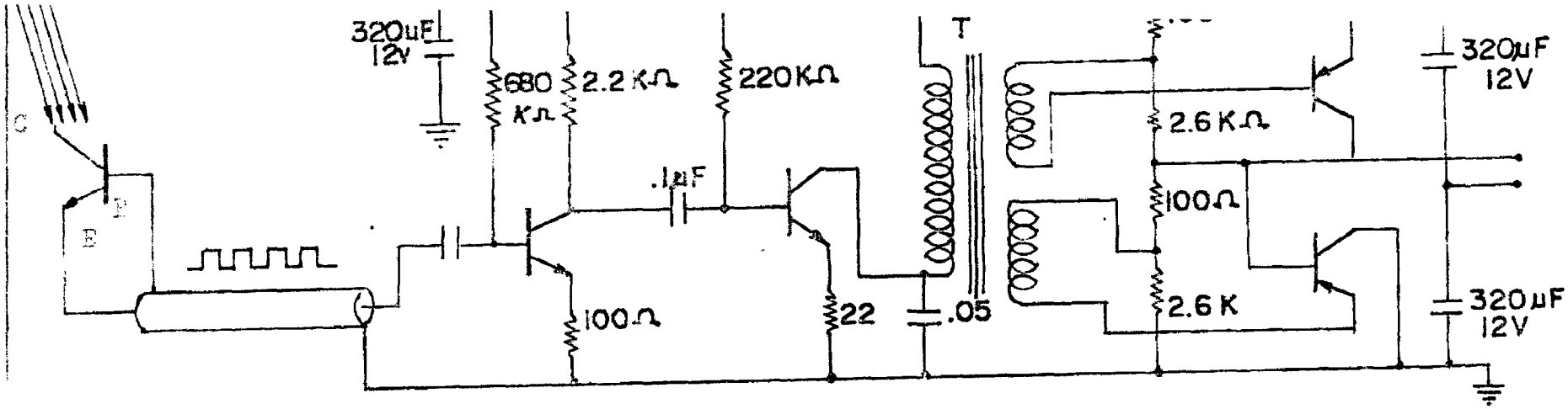
CHAPTER - 2

MULTICHANNEL SIGNAL TRANSMITTING SYSTEM

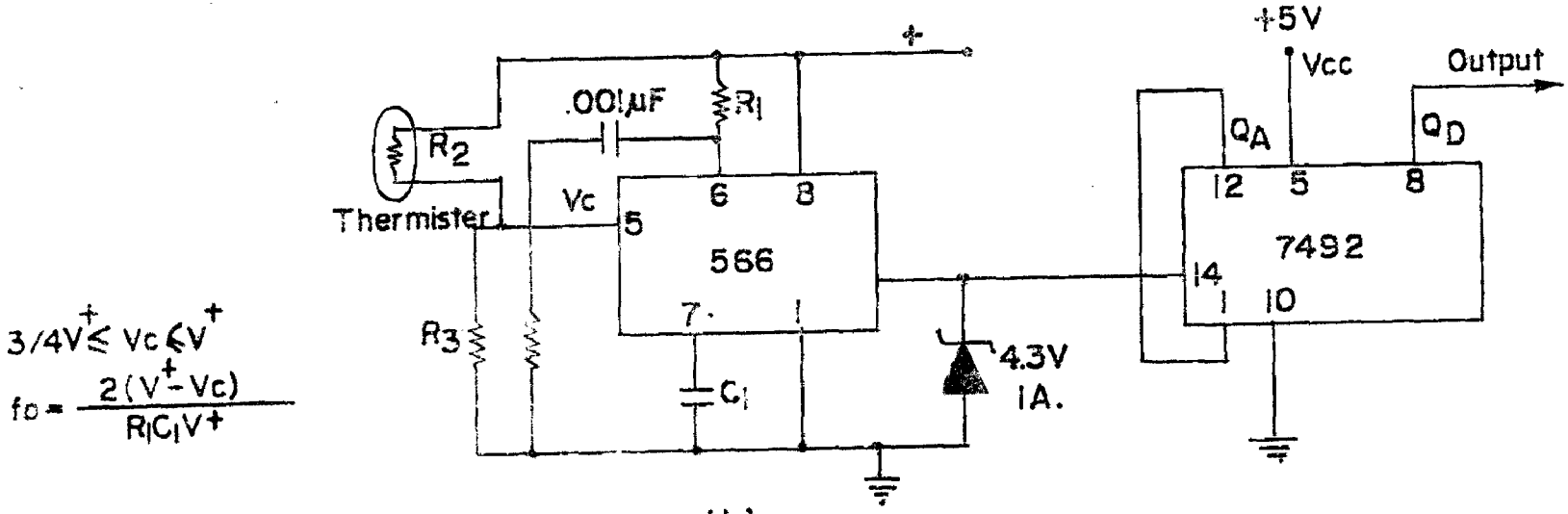
The four parameters of a d.c. shunt motor, namely, the speed, the temperature, the voltage across the field winding and voltage across the armature are converted to digital signals by the transducers, s/f, convertor, t/f convertor, and v/f convertor. Followed by a four channel multiplexing system. The output of the multiplexing system is applied to a 1 W, 1 MHz A.M. transmitter. The design of these individual systems is described below.

(i) Speed to Frequency Convertor (s/f) Transducer Amplifier

The Figure 2(a) shows the complete circuit of the speed to frequency convertor. A photo-transistor speed transducer is fabricated to convert the speed of the motor into a frequency signal. It consists of disc of 7.5" diameter. 60 holes each of 1/8" dia. are made on a circle of radius 3.5" with equal spacing on the disc. This disc. is mounted on the shaft of the motor. A photo transistor SIT 200 is mounted at one side of the disc and a bulb on the other side. They are aligned in such a wave that whenever the hole from the disc comes in ~~feet~~ front of the bulb, the light crosses the hole and falls on the junction of the photo transistor. The output of the photo-transistor is a series of pulse train, the pulse width of which is dependent upon the speed of the motor. Since the amplitude of the signal from the photo-transistor is very low, and to convert it to a level



(a)



$$3/4V^{+} \leq Vc \leq V^{+}$$

$$fo = \frac{2(V^{+} - Vc)}{R_1 C_1 V^{+}}$$

(b)

FIGURE 2 (SPEED TO FREQUENCY CONVERTOR (S/F) TRANSDUCER AMPLIFIER
(a) TEMPERATURE TO FREQUENCY CONVERTOR TRANSDUCER (T/F)

compatible with TTL logic levels, it is followed by an audio amplifier.

(ii) Temperature to Frequency Convertor(t/f) Transducer

Figure 2(b) shows the complete circuit of a temperature to frequency convertor. A thermistor or a series bank of six silicon diodes are mounted on the motor, so that whenever the temperature of the motor changes the sensors resistance will change. IC 566, a voltage controlled oscillator, is used to convert the temperature to frequency. The sensors i.e. either the thermistor or the diodes forms one arm of the potential divider. The supply voltage V_{cc} is 15 volts. The control terminal voltage should be in the range $3/4\ V^+ \leq V_c \leq V^+$. It means the voltage across sensor varies from 11.5 V to 15 volt. The frequency is given by

$$f_o = \frac{2\,(V^+ - V_c)}{R_1\ C_1\ V^+}$$

The output of the IC 566 is grounded through a 4.3 V. Zener diode to eliminate and to maintain level suitable for TTL devices for further application.

(iii) Voltage to Frequency Convertor (v/f) Transducer

The voltage across the armature is reduced to a maximum of 4 volt signal by a potential divider as shown in figure 3. The signal is then applied to the inverting input of the difference amplifier. The operational amplifier gives an output ranging from 11.5 V to 15 volt as the voltage varies from

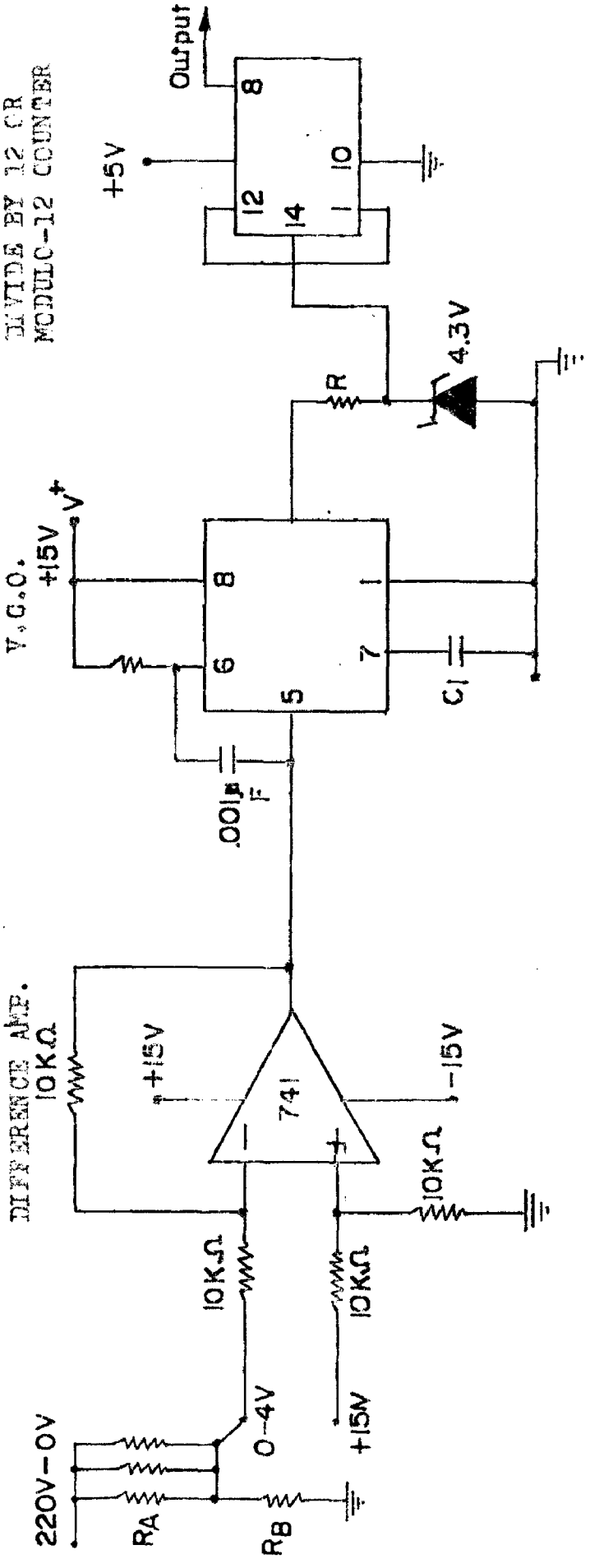


FIGURE - 3 VOLTAGE TO FREQUENCY CONVERTOR TRANSDUCER (V/F)

3.5 volts to 0 volts. This signal is suitable to apply to the control terminal of IC 566, V.C.O., whose supply voltage is 15 volts. Since the control voltage should follow the relation

$$3/4\ V^+ \leq V_c \leq V^+$$

The frequency of the output signal is given by

$$f_o = \frac{2\,(V^+ - V_c)}{R_1 C_1 V^+}$$

The output signal is first of all passed through a zener diode to make it suitable for further application to digital circuits.

(iv) Digital Signal Multiplexer

Multiplexing is a popular technique in which data from several signal sources (or channels) are combined in a prescribed orderly fashion into a single transmitting line. The digital signal multiplexing can be simply pictured as a rotating commutator that momentarily and sequentially connects each of the several digital input signals to the single common output. A digital signal multiplexer, then, is a circuit that serially switches a number of different digital input signals onto a single channel.

Figure No.4 shows a functional block diagram of a four channel digital multiplexer. The one input of each of the four AND gates is connected to the four input digital signals

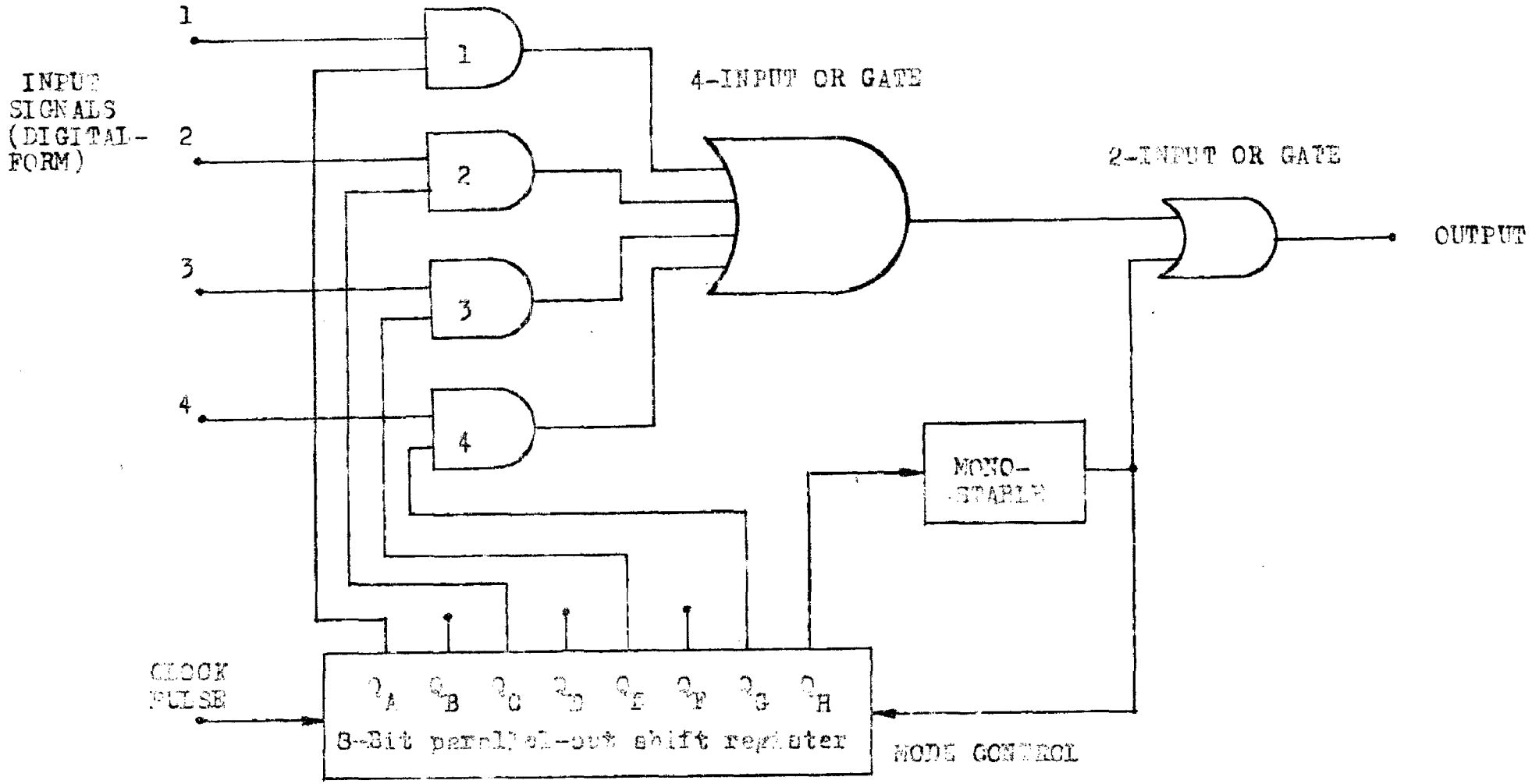


FIGURE - 4 FOUR CHANNEL SIGNAL MULTIPLEXING

to be multiplexed. All the four digital inputs are compatible with TTL logic levels. The other corresponding four inputs to the AND gates are the four outputs Q_A, Q_C, Q_E and Q_G of a 8-bit parallel out shift register. All the four outputs of the AND gates are applied to a 4-input OR gate. The last output of the 8-bit parallel out shift register, Q_H, triggers the monostable, the output of which is applied to the mode control of the shift register. And also this output, with the output of the 4-input OR gate forms the input for a 2-input OR gate.

The functioning of the multiplexer can be described with the help of the figure No.5. A clock pulse from an astable multivibrator of pulse width 25 μsec as shown in figure 5(a), is applied as the clock input of the shift register. As shown in the figure 5(a), at the trailing edge, a, of the clock pulse the output Q_A goes high. The AND gate 1, will pass all the signals which appears at the input of channel No.1, until the trailing edge, b, reaches. At this point Q_A goes low, and Q_B goes high so from the t. edge, b, to c, no signal will be transferred. At the trailing edge, c, Q_C goes high and the outputs, Q_A, Q_B, Q_D, Q_E, Q_F, Q_G and Q_H remains low. It will transfer the signal untill the next trailing edge appears. This procedure continues upto the trailing edge, h, at which the channel-4 has been just exhibited

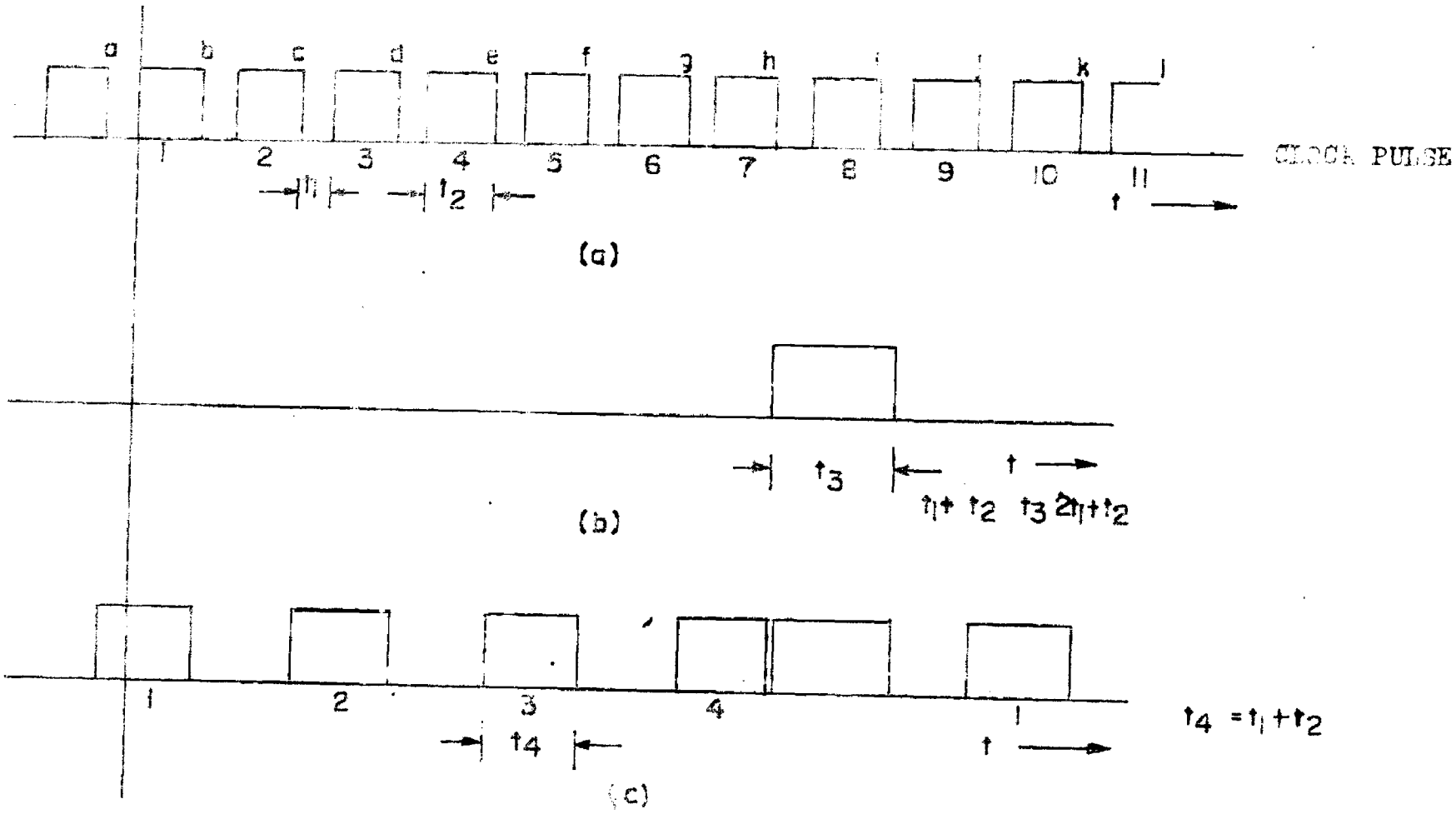


FIGURE - 5 WAVE FORMS AT THE OUTPUT OF VARIOUS IC's IN THE SIGNAL MULTIPLEXING SYSTEM

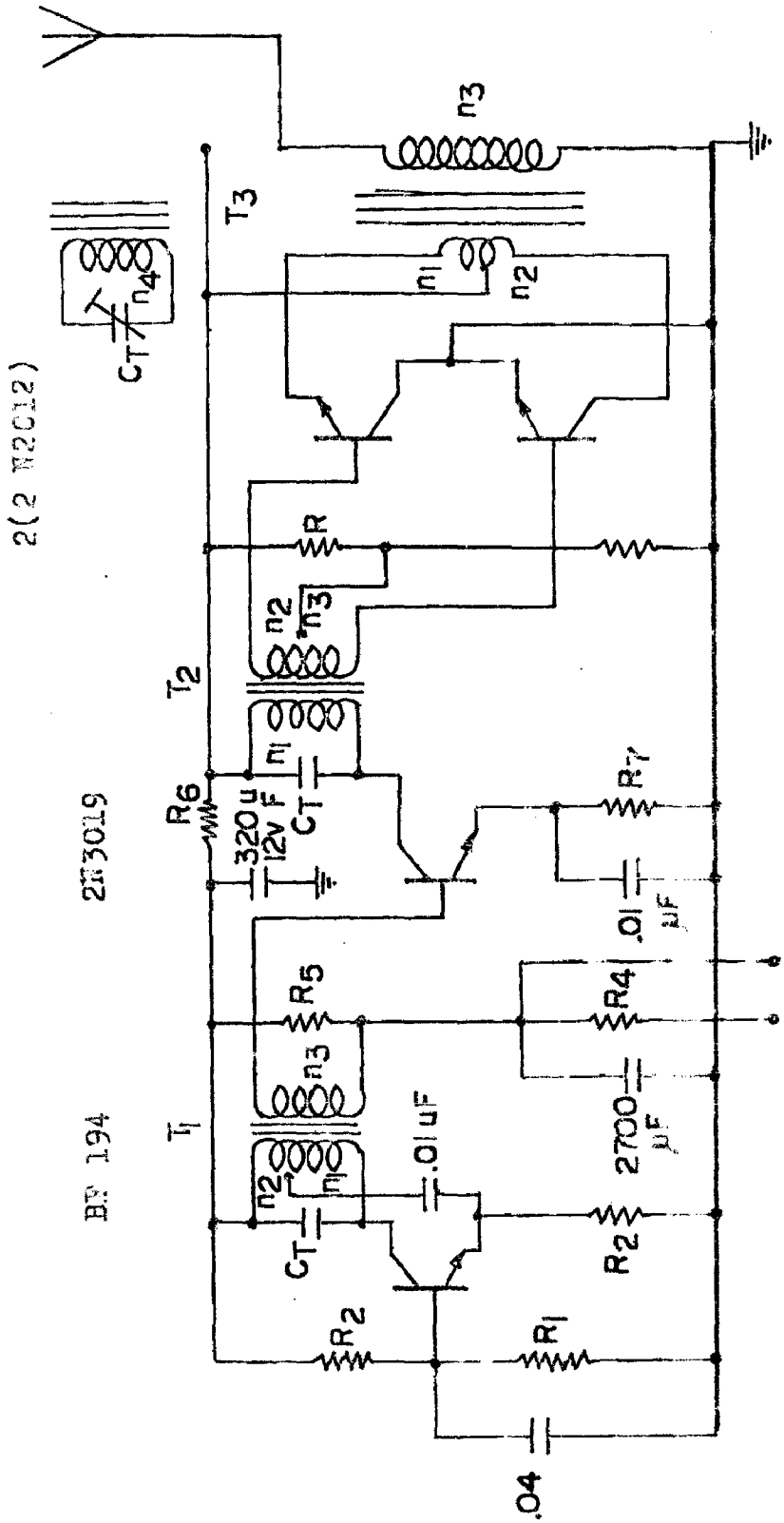
to transfers the signal. At this trailing edge Q_H goes high which triggers the monostable. Now the outputs of the AND gates sequentially goes to high depending upon the signal pulses appearing at the input of each channel for a period 25 μ sec. maximum. These outputs are applied to a 4-input OR gate. The output of this OR gate transfers the information for 25 μ sec of the first signal (or channel) then after the elapse of 25 μ sec again it transfers the second signal for 25 μ sec and so on. The output of this 4-input OR gate is applied to the 2-input OR gate as shown in figure 4. This 2-input OR gate passes all the information of the previous OR gate. In addition it also transfers an output pulse from the monostable of pulse width $T = t_1 + t_2 < t_3 < 2t_1 + t_2$, which appears just the fourth signal has been stopped from transferring.

The output of the monostable is also applied to the Mode Control of the shift register. The triggered pulse of the monostable resets the 8-bit parallel out shift registers. At the trailing edge of the 9th pulse, i. Q_A goes high and thus the cycle starts again till the monostable again resets the shift-register.

The output of the OR gate or the multiplexer contains samples of information of each signal for 25 u sec, one at a time, and a reset pulse from the monostable.

(v) 1 W, 1 MH_z AM Transmitter

The circuit diagram of a 1 W, 1 MH_z, A.M. transmitter



MODULATING
INPUT SIGNAL

FIGURE - 6 [illegible], 1WATT, [illegible], TRANSMITTER

is shown in the figure 6. It comprises of an oscillator, modulator, R-F. pre-amplifier, R.F. power amplifier and antenna. The design of these stages is given below.

Antenna -

For the full wave anteena the length of the anteena wire

$$= \frac{3 \times 10^{10}}{1 \times 10^{6}} = 3 \times 10^{4} \text{ cms}$$

$$= 300 \text{ metres}$$

Push-pull R.F. Transformer T_3

The push-pull transformer which is driven by two transistors 2 N 2012, NPN, consists U/23/32/7 ferrite U-core assembly as the core of the transformer. The ferrite core set have

Effective length $l_e = 74$ mm

Effective area $A_e = 61 \text{ mm}^2$

For calculating the inductance for the above core any one of the formulae given below can be used.

$$L = \frac{\mu_0 \mu_e N^2}{l_e / A_e} \quad \text{(all units in M.K.S.)}$$

$$= 1520 - 2800 \quad \text{(E.C.L F) Manual}$$

or $N = 92 \sqrt{L}$ (1)

where L in m H.

In the class-B push pull stage, the mean a.c. power output P_{out} is given by

$$P_{out} = \frac{(V_{r.m.s.})^2}{R_{Ce}}$$

Since the supply voltage is 10 volts we can take

$$V_{r.m.s.} = \frac{10 - 2}{\sqrt{2}} = 5.66 \text{ volts}$$

$$P_{out} = 1 \text{ Watt}$$

$$\therefore \quad R_c = \frac{(V_{r.m.s.})^2}{P_{out}} = 32 \ \Omega$$

For the U-core assembly the working Q (i.e. Q_w) can be taken between 10 and 20. Let we take $Q_w = 12$. The unloaded Q_0 is of the order of 230. Because $Q_0 \gg Q_w$, the dynamic impedance of the circuit at resonance is effectively equal to R_c, the collector load. Thus

$$R_c = \omega L \, Q_w$$

$$\therefore \quad L = \frac{R_c}{\omega Q_w} = \frac{4 \times 10^{-6}}{3\pi} \text{ H}$$

$$n_1 = 92\sqrt{L} \qquad \text{where L in mH}$$

$$n_1 = 1.9 = 2 \text{ turns}$$

$$\therefore \quad L = \frac{1}{2.12} \times 10^{-6} \text{ H}$$

$$n_2 = n_1 = 2 \text{ turns}$$

The output voltage across the secondary of the transformer, let be 60 volts peak to peak

$$\therefore \quad \frac{2\,n_1}{n_3} = \frac{V_1 \text{ r.m.s.}}{V_3 \text{ r.m.s.}}$$

$$\therefore \quad n_3 = 30 \text{ turns}$$

To find the mutual inductance, the inductance of sec. winding is

$$L = \left(\frac{n}{92}\right)^2 = 1.21 \times 10^{-4} \text{ H.}$$

$$\therefore \quad M = K\sqrt{L_1 L_2}$$

$$= 0.5\sqrt{L_1 L_2} = 3.8 \times 10^{-6} \text{ H}$$

$\therefore$ Total primary winding inductance

$$L' = L + M = 4.27 \times 10^{-6} \text{ H}$$

$$C = \frac{1}{(2\pi f)^2 L'} = 5.92 \times 10^{-9} \text{ F}$$

$$C_T = \left(\frac{n_1}{n_4}\right)^2 C = 27 \text{ p.f.}$$

R.F. Transformer T_2

The transistors used in the push pull stage has $h_{fe\ min} = 50$.

We have chosen $V_{p-p} = 8$ volt

and $P_{out} = 1$ watt

now $V_{r.m.s.}$ $i_{c\ r.m.s.} = P_{out}$

i_c the collector current

$\therefore\ i_{c\ r.m.s.} = 1/8/\sqrt{2}$

$\therefore\ i_{c\ p-p} = \dfrac{\sqrt{2}}{8/\sqrt{2}} = 250$ mA

$\therefore$ base current

$$i_{b.\ p-p} = \frac{250}{50} = 5 \text{ mA}$$

$$i_{b\ r.m.s.} = 5/\sqrt{2} \text{ mA}$$

$$V_{b\ p-p} = 1 \text{ volt}$$

$$V_{b\ r.m.s.} = 707 \text{ volt}$$

Base power input

$$P_{b\ in} = 5/\sqrt{2}\quad 1/\sqrt{2} = 2.5 \text{ mW}$$

Now $$\frac{(V_{b\ r.m.s.})^2}{Z_{in}} = 2.5 \times 10^{-3}$$

$$Z_{in} = 200\ \Omega$$

Now $$L = \frac{Z_{in}}{\omega . Q_\omega} = \frac{1}{35\pi} \times 10^{-4} \text{ H}$$

$$(\ 50 \geq Q_\omega \geq 25\ )$$

$\therefore$ $n_2 = 135 \sqrt{L}$ where L in mH

$= 4.1$ turns

$= 5$ turns

$\therefore$ $L = (\frac{n_2}{135})^2 \times 10^{-3} = 1.37 \times 10^{-6}$ H

$n_2 = n_3 = 5$ turns

$n_2 + n_3 = 10$ turns

Total inductance $L = (\frac{10}{135})^2 \times 10^{-3}$ H

$= 5.50 \times 10^{-6}$ H

We have taken the turning capacitance

C = 820 p.f.

$\therefore$ Total primary inductance

$$L' = \frac{1}{(2\pi f)^2 C} = 3.08 \times 10^{-5} \text{ H}$$

$L' = L_1 + M$

Now $M = K \frac{L_1 + L_2}{2}$

$= \frac{L_1 + L_2}{2}$

$= .45 L_1 + 2.475 \times 10^{-6}$

$\therefore$ $L' = L_1 + .45 L_1 + 2.475 \times 10^{-6}$

$3.08 \times 10^{-5} = L' = 1.45 L_1 + 2.475 \times 10^{-6}$

We can calculate L_1

$$n_1 = \sqrt{\frac{L.l}{\mu_o \mu_r A}} = 28 \text{ turns}$$

Oscillator Transformer T_1

$$f = 1 \text{ MH}_s$$

Let we take $C_T = 2000$ p.f.

$$\therefore L = \frac{1}{(2\pi f)^2 C} = 1.27 \times 10^{-5} \text{ H}$$

$$\therefore n_1 = \sqrt{\frac{L.l}{\mu_o \mu_r A}} = 40 \text{ turns}$$

Now

$L = 1.27 \times 10^{-5}$ H

$n_2 = 135 \sqrt{L}$ where L in mH

$= 15.2 = 16$ turns

mutual inductance

$$M = K \sqrt{L_1 L_2}$$

$$= .5 \sqrt{L_1 L_2} = .635 \times 10^{-5} \text{ H}$$

$$\therefore L' = 1.905 \times 10^{-5} \text{ H}$$

$$C_T = \frac{1}{(2\pi f)^2 L'} = 1333.33 \text{ p.f.}$$

CHAPTER - 3

MULTICHANNEL SIGNAL RECEPTION AND DISPLAY

Multiplexed signals are received by the receiver and the demultiplexing system separates out the four signals again into the same form as they are, when applied at the input of the multiplexing system. The output of the demultiplexer is applied to a 4-digit LED display through band switch. The individual circuits are described below.

(i) Recdver

In a superhetrodyne receiver, the incoming r.f. signal is amplified and converted to what is called the intermediate frequency. The i.f. signal is then amplified and detected. Frequency conversion is effected in such a way that the envelope of the modulated wave is preserved. Since for any signal frequency there is one and the same intermediate frequency, it is easy to build the i.f. circuits of the requisite band width and high selectivity.

The aerial input circuit and radio-frequency amplifier have but little effect on receiver selectivity on short and ultra short waves, and only improves the receiver sensitivity.

The frequency changer consists of a mixer and a local oscillator. The latter is a low power self excited radio-frequency oscillator which generates a signal at a slightly different frequency from the r.f. signal, f_o.

Frequency conversion is obtained in the mixer which accepts two signals, the incoming r.f. signal f_s picked up by the aerial, and the local oscillator signal fo. The intermediate signal at the output of frequency changer usually is a difference frequency

$$f_o - f_s = f_i$$

The intermediate frequency amplifier operates at a constant frequency and amplifies the i.f. signal to the value required for the normal operation of the detector. I.f. amplifiers are usually band-pass amplifiers whose resonance characteristics is nearly rectangular. In this way high selectivity can be obtained at uniform amplification within the bandwidth.

The audio-frequency amplifier builds up the audio-frequency signal to deliver the power output or output voltage necessary for the operation of the terminal equipment (load).

In addition to high selectivity and sensitivity, superheterodyne receivers show better overall performance.

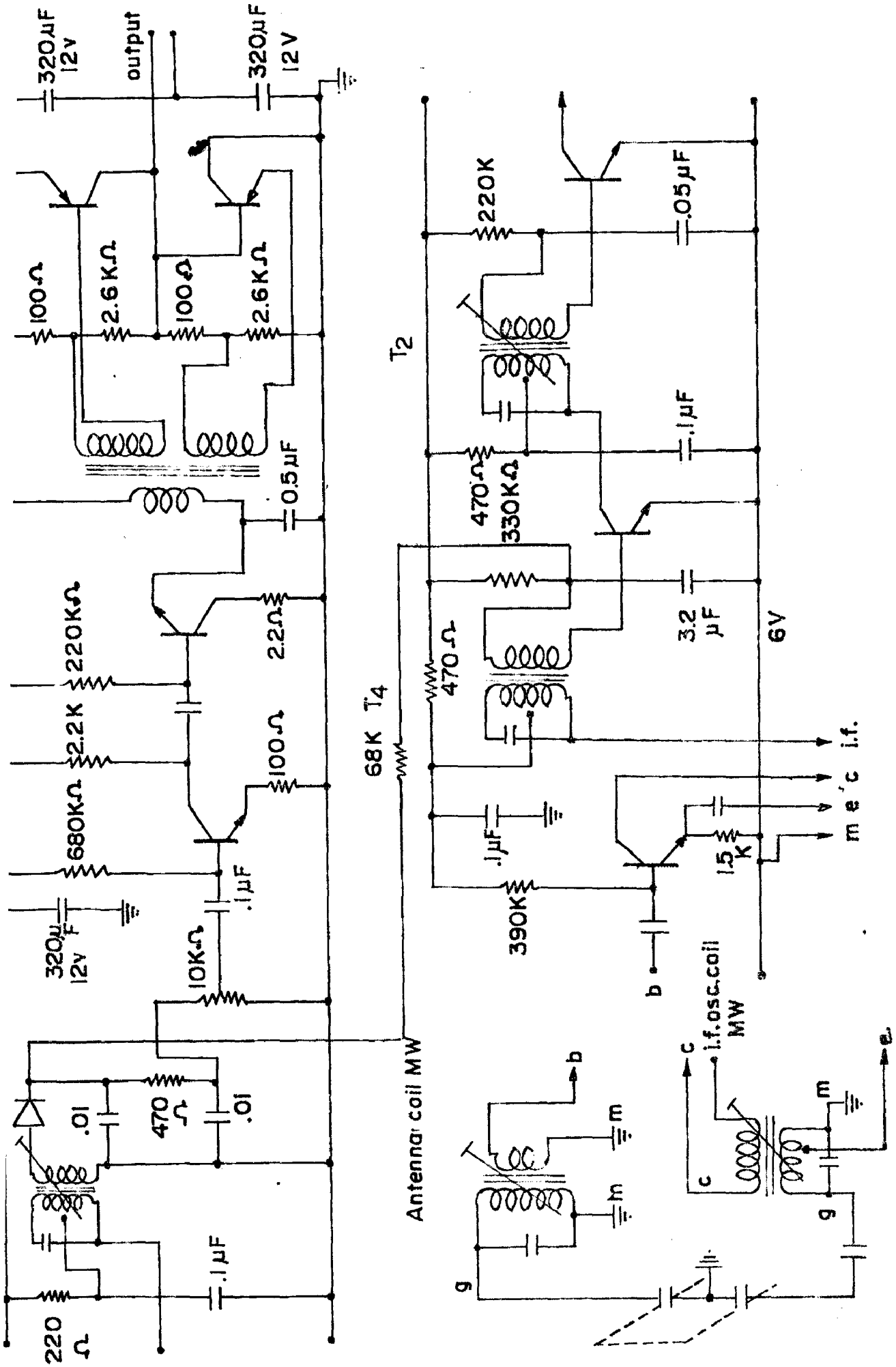


FIGURE - 7 MODERN MATE A.M. ROUTER

The complete circuit diagram of the receiver is shown in Fig.7. Seven transistors and one germanium diode are used in the basic form of the receiver. The BF 194B is the frequency changer and the two BF 195 form the i.f. amplifier. The detector is the OA 70 germanium diode. Four transistors made the audio stages, BC 148 is used as an audio frequency pre-amplifier, the next BC 148 silicon transistor is being used to drive a matched pair of AC 128 (the 2- AC 128) in the transformers push-pull output stage. The aerial is a ferrite rod which gives the required selectivity and sensitivity and can be coupled conveniently to the frequency changer. The oscillator and antenna coil connections made as under.

Coils colour code

(OSE Coils)

White	-	Collector c
red	-	i.f. +
green	-	gang g
yellow	-	emitter e
black	-	ground m

(antenna coil)

green	-	gang g
blue	-	base b
black	-	ground m
red	-	loop aerial l

The loop antenna is a rectangular of size 11'' x 6'' of SWG 18 wire. Instead of gang two trimmers of 0-50 p.f. are used to tune the circuit at our required 1 MHz frequency. The standard i.f. of 465 kc/s is used and the local oscillator frequency is above the signal frequency in accordance with normal practice. The BF 194 B operates as a self-oscillating mixer. The r.f. signals from the aerial coupling coils are fed into the base of the BF 194, which produces its own local oscillation by means of feedback from the collector to the emitter. The i.f. is selected at the collector of the BF 194 by the first i.f. transformer T_1.

The i.f. amplifier consists of two BF 195 operating in unilateralised grounded emitter circuits. Singly tuned i.f. transformers are used here. We can also use double tuned i.f. transformers to improve either or both, the frequency response ~~xit~~ and adjacent channel rejection.

The third i.f. transformer T_3 is connected to an OA 70 detector diode which provides an audio output and a d.c. output. The d.c. output is fed back to control the operating current of the first i.f. transistor so providing automatic gain control. The audio amplifier is the same as is the transducer amplifier except the transistors used in output stage i.e. in the push pull transformerless stage are a matched pairs of AC 128 instead 2N 359.

A battery voltage of 10 V is selected and this voltage is allocated in the following way -

(a) the h.f. transistors work at the collector emitter voltage of 6.5 volt which gives a maximum gain.

(b) a voltage drop of about 1 V is allowed across the emitter resistors of h.f. transistors for stabilization of the working point.

(c) a drop of 3.5 volt is allowed across the decoupling resistor from the audio output stage, so that the decoupling resistance can be high enough to make a very high decoupling capacitance unnecessary.

(ii) Signal Demultiplexer

A group of cascaded flip flops used to store related bits of information is known as a register. A register that is used to assemble and store information arriving from a serial source is called a shift register. Each flip-flop output of a shift register is connected to the input of the following flip flop, and a common clock pulse is applied to all flip flops, clocking them synchronously. Hence the shift register is a synchronous sequential circuits. Registers are data storage devices that are most sophisticated than latches. They use edge triggered flipflops, Shift registers can be classified into five classes -

1. Serial-in, serial-out shift registers
2. Parallel-in, serial-out shift registers
3. serial-in, parallel-out shift registers
4. Parallel-in, parallel-out shift registers
5. Parallel-in, parallel-out bidirectional shift registers

Shift registers are used in a digital system for temporary information storage and data manipulation and transferring.

A voltage comparator (VC) senses the relative polarity of the differential voltage applied to the comparator's two inputs. The output of an ideal VC will be at a voltage level corresponding to a logic 1 whenever the difference voltage existing between the non-inverting and inverting inputs is positive, or

$$V_{out} = \text{logic 1} \quad \text{when } (V_+ - V_-) > 0$$

when this difference voltage is negative, the VC output is a logic, 0, or

$$V_{out} = \text{logic 0 when } (V_+ - V_-) < 0$$

The output of an ideal comparator changes state when $V_+ = V_-$.

An important application of a VC is a level detection. A reference voltage and an input signal are separately applied to VC inputs. The VC output is at a low voltage level (logic 0) whenever the input is more negative than the reference voltage, it is at a high level (logic 1) whenever the input is more positive than the reference.

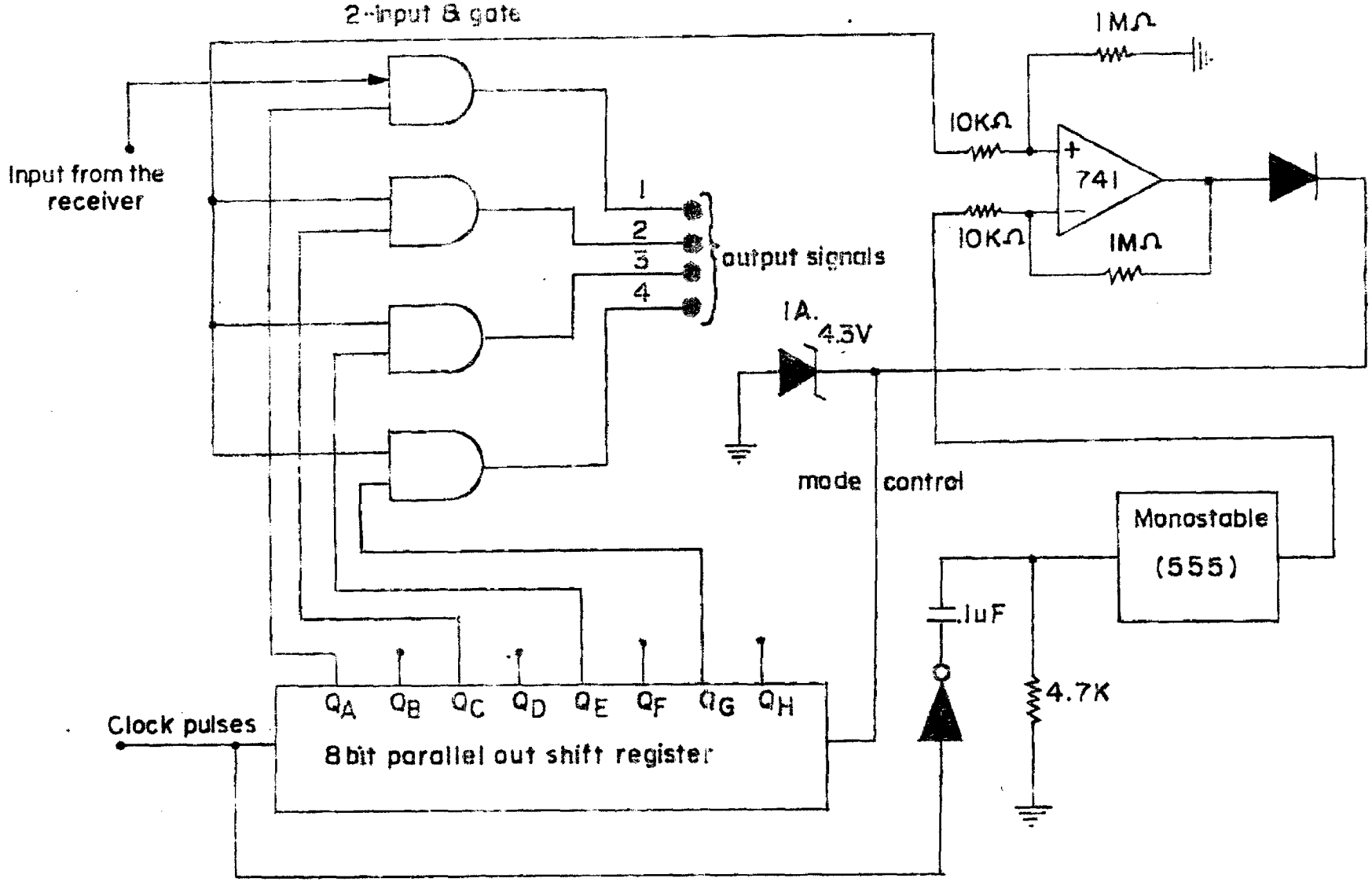


FIGURE - 8 SIGNAL TO-MULTIPLEXING

The VC is equally functional if the input- and reference voltage terminals are interchanged. This reversal of terminals will simply invert the output voltage wave shape.

Figure 8 shows the functional diagram of the De-multiplexer. The output of the receivers is connected to one input of each of the four AND gates. The other four inputs are connected to the outputs Q_A, Q_C, Q_E, Q_G of the 8-bit parallel-out shift register. A clock pulse of pulse width 25 μ sec is applied to the shift register from an astable multivibrator. The clock pulse is also applied to an inverter and then after differentiating it is applied to a monostable. The output triggered pulse of the monostable goes to inverting input of the operational amplifier used as a comparator. The non-inverting input the operational amp. is connected to the output of the receiver. The comparator output is applied to the mode control terminal of the shift register.

The working of the demultiplexer is explained below. At the negative edge of the clock pulse the monostable gets triggered and it gives an output pulse, the pulse width of which is less than the width of the pulse generated by the monostable in the multiplexer. The pulse of the monostable of the multiplexer has been transmitted along with the intelligence. These pulse after receiving applied to the non-inverting input of comparator alone with the intelligence.

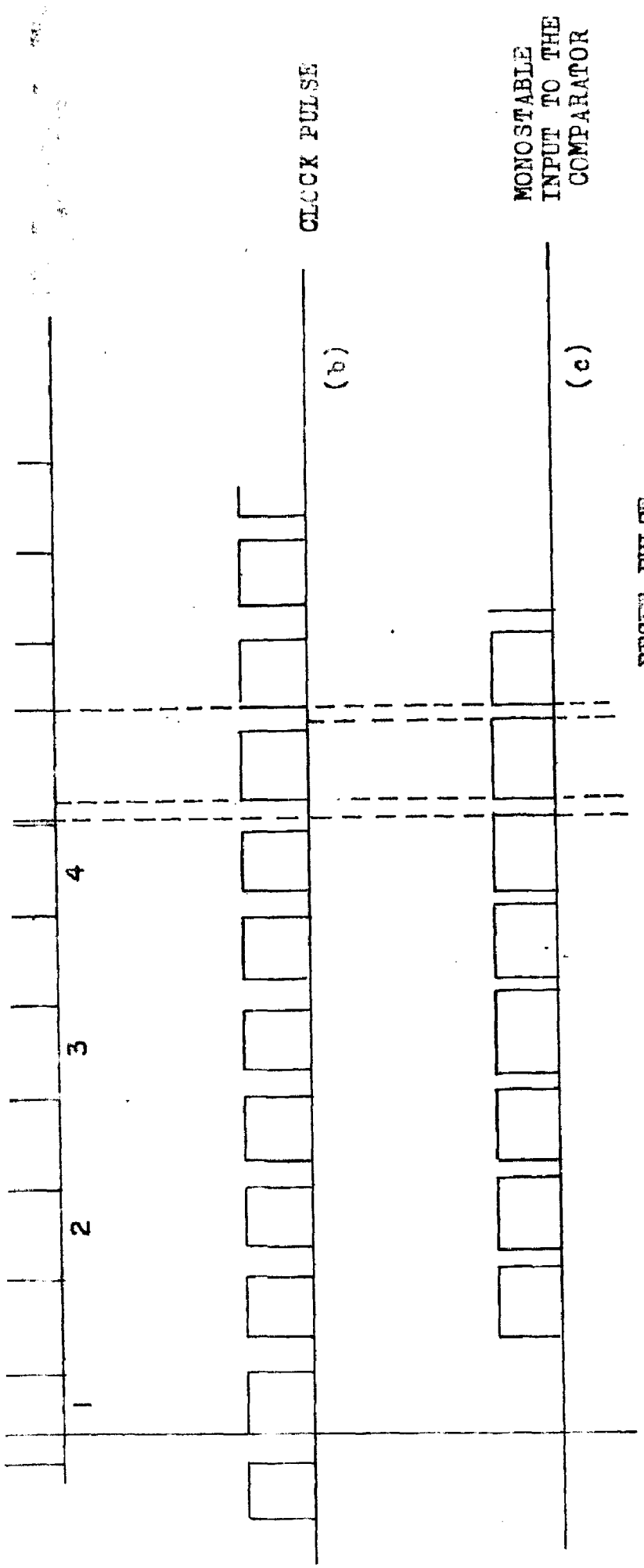


FIGURE - 9 WAVEFORMS TO SHOW THE SYNCHRONIZATION OF THE SIGNAL MULTIPLEXING AND THE SIGNAL-DEMULTIPLEXING

The comparator compares the two inputs and generally gives a negative output which the diode connected at the output, blocks at here. As shown in the figure-9 for the period d'e' a positive pulse appears at the non-inverting input and there is no input at the inverting input. This gives a) pulse which reset the 8-bit parallel out shift register. At the negative edge of the clock-pulse Q_A goes high for 25 μ sec Whatever be the signal at the input of gate 1 will be transmitted. For the next 25 μ sec Q_B goes high and all others remains low. Therefore no intelligence will be transmitted. For the next 25 μ sec Q_C goes high and the signal at gate 2 will be transmitted. When the last intelligence has been transmitted, the monostable generates their pulses, wh ch again the comparator, compares and resets the monostables. The four signals are obtained at the output of the four gates in the same serial order as they are at the input of the multiplexing system.

(iii) <u>4-digit seven segment Digital Display</u>

Flip-flops programmed as counters are used in a wide variety of counting application in ascientific instruments, industrial controls, computers and communication equipments, as well as in many other areas. The basic function of a counter is to ' remember ' how many clock pulses have been applied to the input, hence in the most basic sense, counters are memory systems. They are used for counting pulses, equipment operation sequencing, frequency division and mathematical manipulation.

Because of wide range of applications for counters they are differing in complexity, functional versatility, speed, power and cost depending upon the specific need.

Counters are classified into two types, the ripple or asynchronous counter and the synchronous counter. A ripple counter is an asynchronous sequential circuit, hence the name asynchronous counter. A synchronous counter is a synchronous sequential circuit. All flip-flops in a synchronous counter are under the control of the same clock pulse, whereas those in an asynchronous counter are not. All counters are made from a set of flip-flops in series. Although each individual flip-flop in a counter may be edge triggered or master-slave, the clock to the counter is of the edge trigger type.

Figure shows the functional diagram of a 4-digit seven segment digital display. It consists of 4 seven segment, common cathode L.E. D's. These are driven by 4 IC's 7448, a BCD to 7-segment decoder/driver. The input to 7448 is applied from a 4-bit latch 7475. These latches are used as temporary storage for binary information between processing units and input/output or indicator units. The 7490 used is a decade counter.

The functioning of the counter is explained below. The signal is applied at one input of the AND gate. The other input is a clock pulse, the pulse width of which is adjusted such that it remains high for a period 1 sec in every cycle.

7 Segment, common cathod L.E.Ddisplay
7448
7475
7490
Ro
2input
8 gate
Input
1 sec.timing pulse
4.7K
Monostable
555
Control waveform
counter reset
gate on
1 sec.

The output of the AND is applied at the input of the decade counter 7490. There are four decade counters which are connected in series. The gate will remain on for 1 sec when the clock pulse goes high. The input is transmitted for second to the counter and it counts the number of pulses for that period. After one sec at the negative going edge of the clock pulse a differented pulse which is generated by the circuit shown in the figure is applied to the clock input of each latch. The latches then enabled to update the data which is stored for 1 second to the display. The differential pulse is applied to the monostable for triggering. The triggered pulse again get inverted and differented. This pulse is applied to the reset terminals of the decade counters. The decade counters then again get ready for counting of the next information. Thus the 7475 will update the data after every one second and whatever we the numbers on the LED's will remain constant for one second untill the new data comes in.

If the input pulses are equal to or less than 9 the first counter 7490 will count it. When the pulses exceeded than 9 and less than or equal to 99 per second the first and the second counter will count. The second counte. will pass only one pulse to the third after every hundred pulse per second. Similarly the third decade counter will pass one pulse to fourth decade counter after every 1000th pulse per second. The whole counter will count input pulse upto 9999 per second.

CHAPTER - 4

LIST OF IMPORTANT COMPONENTS

The following is the list of the main components used in the fabrication work.

1.	566	Function Generator	2 No.
2.	7492	divide by twelve counter	2 No.
3.	741	op. amp.	2 No.
4.	7408	quad 2-input AND gate	3 No.
5.	7402	quad 2-input NOR gate	1 No.
6.	7400	quad 2-input NAND gate	2 No.
7.	7404	hex inverter	2 No.
8.	7495	4-bit right shift, left shift register	4 No,
9.	555	Timer	5 No.
10.	7490	decade counter	7 No.
11.	7475	4-bit Batch	4 No.
12.	7448	bcd to 7-segment decoder/driver	4 No.
13.	Seven segment common cathode L.E.D's		4 No.
14.	2N 359		4 No.
15.	2N 3019		1 No.
16.	2N 2012		2 No.
17.	BF 194		2 No.
18.	BC 148		4 No.
19.	BF 195 D		1 No.

20.	BF 195C	1 No.
21.	4.3 V zeners	4 No.
22.	OA79 diode	1 No.
23.	I.F.T.'s sets, P104	2 No.
24.	SIT 200 photo-transistor	1 No.
25.	4- pole band switch	1 No.

In addition it consists other minor elements like resistance capacitance etc.

CHAPTER - 5

OPERATION AND TESTING

The photo transistor gives a signal of 2 μA r.m.s. when the motor is operating. The signal is fed to the transducer amplifier by a shielded wire. All wire connection in the transducer amplifier should be made by using a shielded wire. Otherwise it will catch noise and which will cause some modulation even if the light bulb which is illuminating the photo-transisto is off and also even the motor is not operating. There is a direct conversion of the speed of the motor from r.p.m. to cycles per second as the disc contains 60 holes. A 6 volt d.c. supply is applied to the amplifier and the output has a signal level of 4.1. volt as tested on the C.R.O. which is compatible with TTL logic levels for application to digital circuits.

As shown in the circuit of figure 2(b), a 15 volt d.c. supply is applied to the circuit. In place of the thermister six diodes are used as the temperature sensing element. At room temperature the voltage drop across R_2 is 3.6 volts and the remaining voltage drops across the resistor R_3. The controlled voltage V_c at room temperature is 15-3.6 = 11.4 volts. As the temperature increases the voltage across the diodes decreases thereby increasing the control voltage. The frequency is given by

$$f_o = \frac{2 (V^+ - V_c)}{R_1 C_1 V^+}$$

have a some linear relationship with the control voltage V_c. or i.e. with the temperature. As the circuit is tested the output of the V.C.O. 566 has a considerable d.c. level of about 3.5 volts and above it the signal level is about 8.5 volts. The d.c. level is filtered by connecting a capacitor of $\cdot 1\,\mu F$ in series with the output. A 4.3 volt zener is connected at the output to make it suitable for further use with digital circuits

Figure 3 shows the circuit diagram of the voltage to frequency converter transducers (V/f). The voltage across the armature is fed to a potential divider such that across one resistance the voltage varies upto 4 volts with respect to ground as the armature voltage goes to 220 volts. The output voltage of one end of the R_B resistance which is a 0-4 volts signal is applied to the inverting input of the difference amplifier. The other end of R_B is grounded. The non-inverting input is supplied a constant 15 volts supply. The output of the difference amplifier varies from 11 volts to 15 volts as the voltage across R_B varies from 4 volts to 0 volts. This output voltage is fed to the modulation input terminal of V.C.O. 566. The other testing and results are the same as described in the previous paragraph. The three signals are available from the thr transducers with sufficient levels to apply further to any digital circuits.

Before feeding these three signals to the multiplexer, the multiplexer is tested individually. The figure 4 shows the circuit diagram of the four channel multiplexer. The 8-bit parallel out shift register is formed by cascading two parallel in parallel out shift registers , the

7495's. A ring counter is formed by connecting Q_E to the serial input i.e. by connecting the pin 10 of the second cascaded IC 7495 to pin 1 of the first IC 7495. A clock pulse of pulse width 25 μsec, is applied to the shift register, which is generated separately by an astable multivrator using Timer 555. To start the shift register a pulse is applied at the mode control manually through a switch. Each of the AND gates and OR gates are tested that without giving any input, the input terminals should not be high. If they show high, then must be grounded, individually through 1 K resistance. First of all check on the C.R.O. that the monostable gives a pulse after every eighth pulse of the clock pulse. Now adjust the pulse width as shown in figure 5. Check the output of the 2-input OR gate. It only gives the pulse ~~only~~ which is generated by the monostable. Now connect the input 1 to V_{cc}, see the output. The output now contains one pulse of equal width that of the clock pulse and followed by a monostable triggered pulse after seven clock pulse. Similarly connect the input terminal 2 to V_{cc} and see the output. As shown in figure 5 (c) the output will now contains pulses 1, 2 and 5 only. Similarly applying V_{cc} to various input combinations. The whole circuit can be tested. Now the circuit is ready for taking input digital signals to be multiplexed.

The output signal from the multiplexer is now reduced by a potential divider to a low level and is feed to the modulating input terminals of the transmitter through a capacitor of 0.1 μF. The transmitter circuit diagram is shown in the figure 6. The value of the modulating signal is so adjusted that only 60% modulation will be obtained. If the modulation increases distortion will be more. The testing of the transmitter is done as : Disconnect the transformer T_1 from the following stages by removing the connection from the base of the transistor 2 N 3019. Now adjust the i.f.t. T_1 so that the oscillator in the common base configuration will give maximum output signal at 1 MH_z. Now connect the base of 2 N 3019 again. To test the next stage, disconnect the bases of the transistors in the push-pull and tune the i.f.t. T_2 to have maximum output at MH_z. Then connect the transistors 2 (2 N 3019). Tune the capacitor C_T to have a maximum output at the antenna. The transmitter fabricated gives an output signal of 40 volts when the applied voltage is 10 volts. The circuit of a superheerodyne, Medium wave A.M. receiver is shown in figure-7. The problems that comes in the operation and testing are described below.

The term ' squeal' ' oscillations', and 'motorboating' are often used interchangeably, depending on the frequency of the oscillations. High frequency oscillations are usually referred to as sequeals, and low frequency ones as motorboating.

The two most common causes of oscillations are open and leaky by-pass capacitors, usually electrolytics. Take a 20 F 15 volt capacitor and tied one end of it to the ground and move the free end to each connection on the printed board. When you reach the defecting capacitor, the radio will start playing.

If by-passing capacitors does't stop oscillations, then you need to isolate the offending stage or stages even further. This can be done by lowering the gain of the suspected stage. If the oscillations stops, the trouble is close to it. The simplest method of lowering the gain in RF mixer and IF stages is to load the stage with a resistor. For example, if it is suspected that an i.f. stage of oscillating place a 10 K across the i.f. transformer. If the oscillations stops, it is a good bet that the trouble is in either that stage or the one following. It should be remembered that a resistor across the transformer is not a cure, even, if it stops the trouble.

If turning the volume does not stop the oscillations the trouble must be in the audio circuits. As in other stages it can be caused by open electrolytes, especially those on the battery supply line. Oscillations may also be caused by incorrect phasing of a replacement transformer, where inverse feedback is used.

Before applying the signal from the receiver to the demultiplexer, the demultiplexing system should be operated and tested individually. As discussed in the case multiplexer the shift register is connected in such a wave to form the ring counter. In this case the manual starting is not necessary. Apply a pulse at the input instead from the receiver from the output of the multiplexer when there is no input signal is applied to the multiplexer. Now check that the monostable generates pulses at equal time period. The pulse width of the pulses generated by the monostable in the multiplexer must be greater than the pulse width of the pulse generated by monostable in the multiplexer. As shown in Figure-9 a'b' is greater than c'd'. For a period of d'e' a positive pulse appears at the non-inverting input of the comparator. The output of the comparator will go high causing the diode forward biased. The amplitude of the output pulse from the operational amplifier is clipped to 4.3 V by a zener diode, so that it becomes suitable to apply to the mode control of the shift register. If after every 8th clock pulse a reset pulse occurs at the mode control it means that both the multiplexer and the demultiplexers are tuned. Now apply the output of the receiver to the input of the demultiplexer. Before applying, check the output of the receiver. It should not be more than 5 volts, otherwise it is not suitable to apply to the digital circuit.

From the band switch, whosoever signal is to be displayed is connected to the 4-digit seven segment display. The display should be adjusted by applying input signal from a function generator at different frequencies. The 1 sec timing pulse or gate pulse should be adjusted until difference between the input frequency to the AND gate and the frequency shown by the L.E.D's display is eliminated.

CHAPTER - 6

CONCLUDING REMARKS APPLICATIONS

The system found practically to be quite immune to electrical disturbances, may be atmospheric or man-made interference. The reason being simple that be have actually transmitted frequency signals on an A.M. transmitter. The disturbances cause the amplitude of the signal to vary. At the end of the receiver we are mainly concerned with the frequency of the signal transmitted and not with the amplitude The circuit following the receiver is again a digital circuit where we are mainly concerned with the frequency. The appendix at the end compares AM versus FM with respect to Interference and other related topics. The total cost of the four channel transmitting system comes upto Rs.1325 at the presents rates of the components, used. The cost have very little effect with the increase in the number of channels.

The multiparameter wireless telemetry found wide acceptance in air borne systems, where weight is always critical in obtaining peak flight performance. The multiplexing and demultiplexing scheme can be helpful to reduce system costs by greatly lessening the number of point to point cable runs as well as the number of individual

components. The wireless telemetry has been and is being used in communication between stationary and mobile objects (such as from ship to shore, from ground to aircraft, from ship to ship or from aircraft to aircraft, and more recently from ground to satellite or from satellite to ground, and between satellites, known as space communication). I t can be used in oil drilling wells in seas to control the drilling machinery from the sea-shore. It can be used to transmit, display and control different parameters of interests like torque, vibrations, speed etc. of rotating machines.

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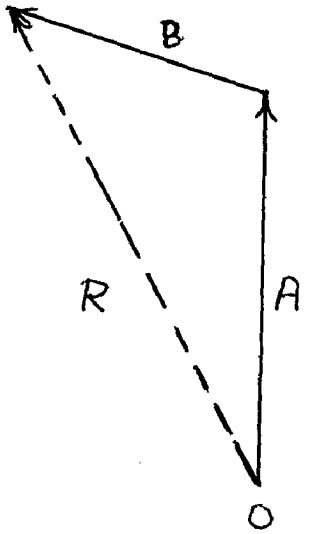
APPENDIX

AM VERSUS FM WITH RESPECT TO INTERFERENCE

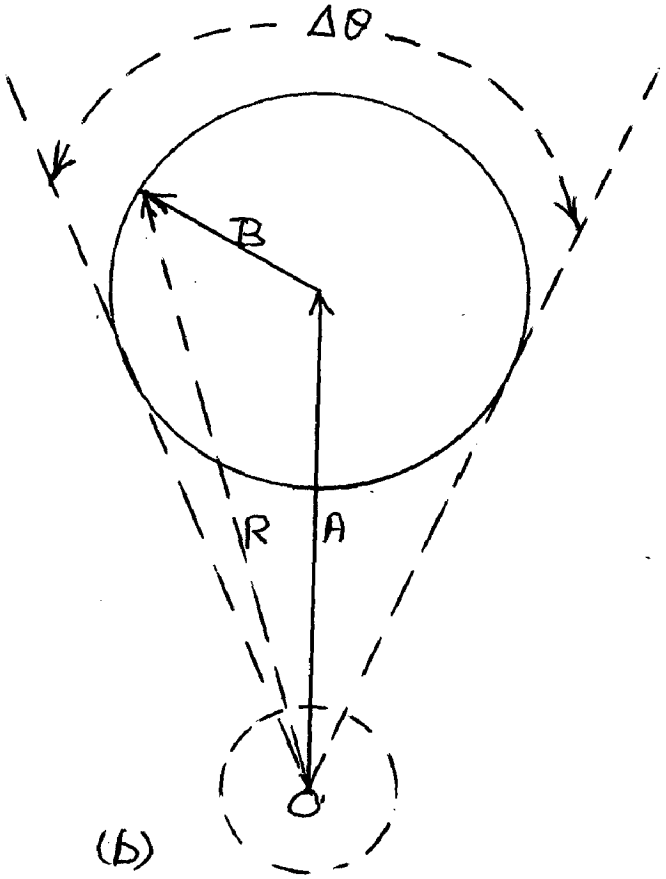
Noise signals caused by atmospheric static or man-made electrical discharges create reception problems for radio signals. If a receiver is designed for reception of FM signals with wide frequency bandwidth and is made insensitive to amplitude variations of the signal, such random interference can be largely eliminated. Thus FM has a major advantage over AM for noisy channel use, particularly in the mobile service.

Interference between two simultaneously received signals on the same or adjacent channels is a major difficulty in radio reception. In this respect FM also has advantages over AM. In the accompanying figure(a) one signal as represented by phasor A rotates about point 0. A second signal of amplitude B is received simultaneously, so that the sum voltage applied to the receiver input is R. As phasor B rotates through its cycle, the amplitude of R will change greatly, thus the input to the receiver is varied in amplitude ef by signal B, and in an AM receiver the B signal may cause appreciable amplitude interference with A even though B is quite small.

If signal A is frequency modulated as in accompanying fig.(b) and an intefering FM signal B is added, the resultant input to the receiver will be R. Phasor B will rotate about



(a)



(b)

Fig:(a)&(b) Effect of Interference between two FM signals.

the end of A_s and the resultant R will vary in amplitude and also in relative phase-angle. For the amplitudes shown, the variation θ approximates 1 radian, as indicated by the circle locus. Even if the two signals are equal in amplitude, the phase-angle variation cannot be much greater, although the amplitude variation would then be so severe that AM reception would be impossible.

An FM receiver can be made insensitive to amplitude variations by clipping all signals to a common low level, this effect is indicated by reducing the signals to an amplitude fixed by the small circle with center at O. Amplitude variations, due either to amplitude modulation on the signal or to amplitude variation of R caused by the interfering FM signal, can be removed. The voltage effective on the receiver would then be fixed by this dashed circle but varying $\pm$ 1/2 radian in phase with respect to phase A_s. If the original frequency modulation causes the phase angle to vary through 2 f/f_m radians per cycle, or 10 radians for f = 75,000 cycles and f_m = 15,000 cycles, it can be seen that the phase variation of $\pm$ 1/2 radian due to interference is quite small. If f_m = 150 cycles for the same value of f, then the desired signal phase variation would be 500 radians, further reducing the effect of the interference.

The effect of the interfering signal can be reduced by widening the frequency band of the signal by increasing f, sufficiently strong signals being assured. This is contrary to

is credited with demonstrating that increased bandwidth of signal does reduce interference when the signal is definitely above the noise level.

AMPLIFICATION OF MODULATED SIGNALS

It would appear that amplitude modulation at a low level, followed by amplification to raise the power level, would provide a saving in power and cost over the high level AM methods discussed. If such amplification is undertaken with a class C amplifier, operating into saturation, variations in input voltage will have only small effect on the output, or the modulation would be stripped off the carrier.

However, the output voltage of the Class B radio-frequency amplifier is a direct function of input voltage, so that such a circuit will properly amplify an AM signal. Such linear class B circuits are widely used, particularly to raise the power level of SSB signals originally generated at low level.

There is no such problem in amplification of FM signals, since the amplitude is constant. Class C amplifiers with their high efficiency, are used to raise the power level of FM signals.