DEVELOPMENT OF FAULT TREE SIMULATOR

A DISSERTATION
submitted in partial fulfilment of
the requirements for the award of the degree
of
MASTER OF ENGINEERING
in
ELECTRICAL ENGINEERIG
(System Engineering and Operations Research)

By

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THE DISSERTATION

ON

DEVELOPMENT OF FAULT TREE SIMULATOR

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C E R T I F I C A T E

Certified that the dissertation on 'DEVELOPMENT OF FAULT TREE SIMULATOR', which is being submitted by SHRI AVINASH SHRIDHAR GAVANE, in partial fulfilment for the award of the degree of MASTER OF ENGINEERING in Systems Engineering and Operations Research of the University of Roorkee, Roorkee (U.P.), is a record of student's own work carried out by him under my supervision and guidance. The work embodied in this dissertation has not been submitted for the award of any other degree or diploma.

This is further to certify that he has worked for a period of 6 months from February 1977 for preparing dissertation for Master of Engineering Degree of this University.

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A C K N O W L E D G E M E N T

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C O N T E N T S

A B S T R A C T

Here the equipment 'FAULT TREE SIMULATOR' is developed. The priliminary informations like

1. Various Path Sets
2. Minimal Path Sets
3. Various Cut Sets
4. Minimal Cut Sets

which are necessary in the Fault Tree Analysis of system can be obtained from the equipment.

LIST OF COMPONENTS USED

PARTICULARS			Nos.
1. 7493	FOUR BIT BINARY COUNTER	...	3
2. 7483	FOUR BIT FULL ADDER	...	3
3. 7408	QUAD TWO INPUT AND GATE	...	4
4. 7404	HEX INVERTER	...	2
5. 7400	QUAD TWO INPUT NAND GATE	...	1
6. 7430	SINGLE EIGHT INPUT NAND GATE	...	1
7.	L.E.D. INDICATING BULBS	...	14
8.	BANANA SOCKETS	...	111
9.	SINGLE SIDED CU-CLADED PLATE 3' x 2'	...	3
	8' x 2'	...	1
10.	DOUBLE SIDED CU-CLADED PLATE 3' x 2'	...	2
11.	PUSH BUTTON SWITCHES ON -	...	2
	ON - OF SWITCH	...	1
12. SG-103	TRANSISTORS	...	2
13.	FLEXIBLE AND HOOK-UP WIRE	...	40 Meters
14.	RESISTANCES 440	...	13
	330	...	3
	1 K	...	2
	6.8 K	...	1
15.	CAPACITORS. 100 MFD	...	1
16.	I.C. BASES 14 PIN TYPE	...	11
	16 PIN TYPE	...	3
17.	METAL CASE FOR EQUIPMENT		

C H A P T E R - 1

INTRODUCTION

There has been a mushroom groth of electronic industries manufacturing lot of entertainment and power electronic equipment. However, reliability of these equipment manufactured currently in India is doubtfull. primarily on account of disregard of these industries in properly carrying out of reliability analysis of the design. These industries can not afford to have an exclusive group for such analysis.

It is therefore the main purpose of the proposed 'FAULT TREE SIMULATOR' to provide these industries with an anologue equipment which will help them in physically carrying out the studies mainly in identifying the various causes of components failure of the equipment through functional simulation of these components failures on fault tree simulation. Fault tree simulator is basically an anologue equipment which will provde an inside to the designer on the critically of the components used in an equipment with regard to the equipment performance.

The idea of fault tree simulation has not yet been exploited any where and is likely to revolunise thinking in

equipment failure analysis methodology, basides its potentiality for bringing out patent.

The preliminary imformations like Path-sets, cut-sets Minimal Path-sets and Minimal cut-sets can be obtained from the equipment.

The given system is first represented by its functional interconnection. Each element of the network element is represented by a 2-input AND gate. One terminal of each AND gate is used to form the given system configuration,. while the other terminals are supplied from the out put binary generation.

The input state vector to the AND gated system network for which the out put indication is obtained represents the various Path sets. And those input state rector which do not give the out put indication represents the various cut-sets.

To obtain Minimal Path-sets, first the path sets of various sizes are obtained by compairing the state vector at the input of AND gated network and state vector at the out put of AND gated network in a binary full adder. The out put of full adder and state of out put node condition are then feed to a final AND gate, which gives the out put indication, for paths of various sizes. Out of these paths of various sizes all paths of size up to and including

(n-1) represents minimal paths sets. Here n are number of nodes present in the network.

Minimal cut sets are nothing but the minimal path sets of DUAL system network.

In the chapter for circuit modification, design of switch operating a monostable multivibrator is given. The out put of this multivibrator is used to drive the input of binary generator.

CHAPTER 2

FAULT TREE ANALYSIS

2.1 WHAT IS FAULT TREE

Fault tree analysis is a technique used for reliability analysis and is generally applicable to complex systems. The predictions from this type of analysis are important considerations in the design of many systems such as space vehicles, air crafts, ships and their electronic systems, missiles and nuclear reactor systems.

Fault tree analysis is considered to be the most simple and most sophisticated analytical technique for reliability analysis.

2.2 ADVANTAGES OF FAULT TREE ANALYSIS:

Technqie of 'Fault Tree Analysis' is of major valve in the following respect.

1. Analyst can concentrate on one particular system at a time.
2. Analysis can be performed with different degrees of detail.
3. Analyst can know the internal behaviour of the system.

4. Points out the aspects of system which are important with respect to the failure of interest.
5. Provides the option for qualitative or quantitative system reliability analysis.
6. Makes easy translation of graphical symbols for methamatical simplification.
7. Allows an easy modification of the number and the characteristics of input random quantities and allowing different out put quantities to be related.
8. Provides a graphical aid giving visibility to those in system management and planning about the final results of the examinations in a syntific way.
9. External influences are just another input to the fault tree (environmental and operational etc.).
10. Analysis can easily be computerised.

2.3 DISADVANTAGES OF FAULT TREE ANALYSIS:

Fault tree analysis has certain disadvantages as listed below:

1. High cost of development
2. Limitations of skilled persons in this techniques.
3. Non-availability of efficient mathematical techniques for analysis.

2.4 DEFINATIONS OF CERTAIN TERM USED IN FAULT TREE ANALYSIS

1. COMPONENT:

A component is a functional unit. These functional

units are arranged and interconnected so as to form a system.

2. SYSTEM:

Intercoupling of several components leads to a system. The system is designed to fulfil its function throughout a specified period of time.

3. RELIABILITY:

The characteristic of an item expressed by the probability with which it will perform a required function under stated condition for a stated period of time. The term reliability is widely used in connection with non-maintained system. (where repair is not possible), such as air craft systems, equipments used in military and medical side etc.

4. TOP EVENT:

It is an undesired event for the system and is obtained by the combinations of primary failures.

5. PRIMARY FAILURE:

It is a failure for a system component

6. FAILURE MODES:

Failure mode is the type of failure in which a

component or system fails to fulfil its function within a a specified period of time.

7. COMMON MODE FAILURE:

Certain single failure that can result in several component failure simultaneously is called common mode failure.

8. FAULT EVENT

It is a failure situation resulting from the logical interaction of primary failure.

9. BRANCH:

Development of any fault event results in a branch of a fault tree.

10. BASE EVENT:

Event being developed is called the base event of the branch.

11. TRANSFER EVENT:

Transfer of any base event from one part of the tree to the other is a transfer event.

12. REPEAT EVENT:

Transfer of one primary event to the other branch of the tree is a repeat event.

13. PATH SET (OR TIE SET)

Set of elements whose functionning will ensure system success.

14. MINIMAL PATH SET:

It is a path set consisting of minimum number elements whose operation is necessary for the system success. Minimal path set is nothing but the forward path from input node to output node.

15. CUT SET

Set of elements whose failure will ensure system to fail.

16. MINIMAL CUT SET:

It is a cut-set consisting of minimum number of elements whose failure ensures the system failure.

Cut sets are nothing but the path sets of the 'DUAL' system of original system. Similarly minimal cut sets are the minimal path sets of this DUAL system.

2.5 GRAPHICAL SYMBOLS USED IN FAULTREE ANALYSIS

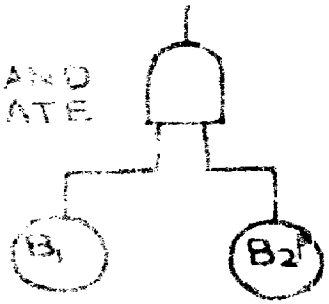
Fault tree construction is a logical development of top event. A fault tree consist of events, branches and gates which define some undesired event the gates acts as mathematical operators which determine the probabilities of events preceding them. There are several operator theories for obtaining probabilities, three of the them which are commonly used in fault tree analysis being (a) Probabilistic set theory (b) Logic theory and (c) Boolean Algebra.

Of the three theories for fault tree analysis set theory is generally considered the best known and easiest to understand. Set operators can be calegorized as 'Union' operators, 'Intersection' operators or combination of these two. Fault tree gates basically fall into these three calegories.

1. 'Union' operator
   - (a) OR gates
   - (b) Exclusive OR gates

2. 'Intersection' Operator
   - (a) AND gates
   - (b) Priority AND gates
   - (c) Inhibit AND gates

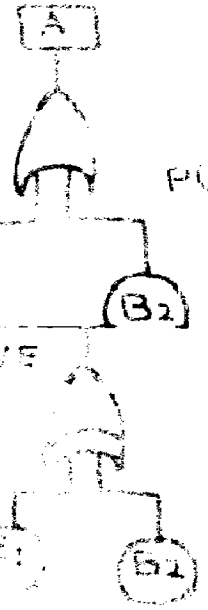
AND GATE



$A = B_1 \cap B_2$

$P(A) = P(B_1) \cdot P(B_2)$

Fig. 1A



OR GATE

$A = B_1 \cup B_2$

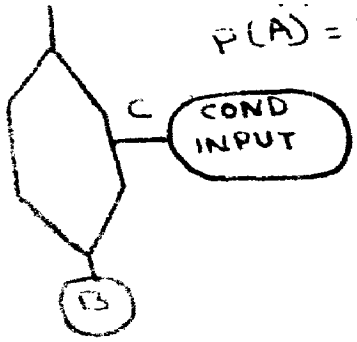
$P(A) =$

EXCLUSIVE OR GATE

$P(A) = P(B_1) + P(B_2)$

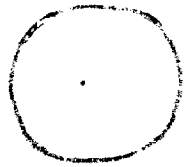
Fig. 1.D.

INHIBIT AND GATE



$P(A) = P(B) \cdot P(C)$

Fig. 1.E



CIRCLE : A PRIMARY EVENT

Fig. 1F

Fig. 1H

GRAPHICAL SYMBOLS USED IN FAULT TREE ANALYSIS

Fig. 1

A. S. GANAPATHY
M. E. [illegible]
[illegible]

3. Combinations

The graphical symbols used in a fault tree basically fall in to two categories.

(a) Logic symbol [fig....1....page 10]

(b) Event symbol [fig....1....page 10]

The most commonly used Logic symbols are described below:

THE AND GATE [fig..1A... page.19.....]

The set notation for event A is

$$A = B_1 \sqcap B_2$$

In other words event A will occure if both events B_1 and B_2 occure. The probability of A when B_1 and B_2 are independent is

$$P(A) = P(B_1).\ P(B_2)$$

In general formula for the AND gate containing K independent events is

$$P(A) = P(B_1)\ P(B_2)\ P(B_3)\ \ldots\ldots\ldots P(B_k)$$

THE OR GATE [fig..1B... Page.19...]

The set notation for event A is

$$A = B_1 \cup B_2$$

Event A will occure if either event B_1 or event B_2 occurs. The probability of A when B_1 and B_2 are independent is

$$P(A) = 1-(1-P(B_1)).\ (1-P(B_2))$$

In general formula for OR gate containing k independent events is

$$P(A) = 1-(1-P(B_1)).\ (1-P(B_2)).\ (1-P(B_3)).....(1-P(B_k))$$

<u>THE PRIORITY AND GATE</u> [fig..1C..page.19...]

Priority AND gate is used when the occurance of events is important. As shown event A occurs only if event B_1 occurs first B_2 occurs next. Both events B_1 and B_2 can occurs in two different ways (B_1 first B_2 next or vice-versa), but the event A will occur only when B_1 occurs first and B_2 next. If both B_1 and B_2 have uniform probability distribution over the interval in question, the probability of A can be given by

$$P(A) = \frac{1}{2}\ P(B_1).\ P(B_2)$$

General formula is

$$P(A) = \frac{1}{K} P(B_1)\ P\ (B_2).\ P\ (B_3) \qquad \ldots P(B_k)$$

where k is the number of ways the B_s can occurs, following permulation selection without replacement.

THE EXCLUSIVE OR GATE [fig..1D..page.10....]

Events immediately following the exclusive or gate are mutually exclusive, that is the occurance of B_1 implies that B_2 can not occur (i.e. $P(B_1 \quad B_2) = 0$) or vice-versa. The general formula for exclusive OR gate containing k events (mutually exclusive and independent)

$$P(A) = P(B_1) + P(B_2) + P(B_3) + \ldots\ldots + P(B_k)$$

THE INHIBIT AND GATE [fig..1:E....page.10....]

It requires the occurence of some out side event for flow thrugh. In order that B flow through the gate event C must occur. The set notation for the gate is

$$A = B_1 \cap B_2$$

and $P(A) = P(B_1).\ P(B_2)$

The most commonly used 'Event Symbols' are described below

RECTANGLE]fig.1F..page.10...]

This represents a fault event resulting from the combination of more basic faults acting through the logical gates.

CIRCLE [fig.1G....page.10...]

This denotes primary events or failure inputs that are independent of all other events.

TRIANGLE: [fig.1H..page.10...]

It is not strictly an event symbol but a transfer from one part of the fault tree to another. A line from the side of the triangle denotes an event transfer out from the associated logic gate. A line from the 9pex of the triangle makes an event transfer in to the associated logic gate from the transfer out triangle with the same identifications number.

2.6 DEVELOPMENT OF FAULT TREE:

The following four steps generally can be present

in a fault tree analysis.

1. To define system
2. Fault tree development
3. Qualitative analysis
4. Quantitative analysis

1. To Define System:

System defination is often the most difficult task associated with fault tree analysis. Of primary importance is a functional lay out diagram of the system showing all functional inter connections and identifying each system component.

The next step in the system description is to establish the system boundary conditions, System boundary condition is defined as the situation for which the fault tree is to be drawn. A most important system boundary condition is the top event. System boundary conditions also include any fault event declared to exist or to be not-allowed for the duration of the fault tree construction. These events are called existing system boundary conditions and 'not allowed system boundary condition. An existing system boundary condition is treated as certain to occure and not allowed system boundary conditions is treated as an event with no possibility of occuring. Neither existing non not-allowed

system boundary conditions appear as event in the final fault tree.

2. FAULT TREE CONSTRUCTION

Here we will illustrate by an example that how a fault tree can be constructed.

Let us consider the example of D.C. motor set up shown in [fig.2A...page.17...]

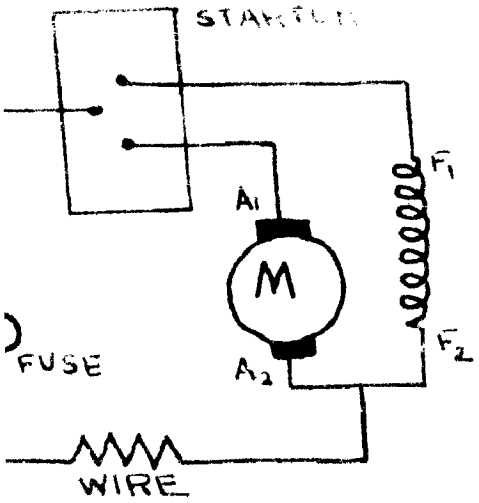
Top event: Motor overheats

The other boundary conditions are switch is closed and failure due to external system is not allowed event. The motor overheats if an electrical over load is supplied to the motor or a primary failure within the motor causes the overheating e.g. if the bearing lose their lubrication or a wiring failure occure withing the motor.

Fault tree is constructed as shown in [fig.....pag..] Excessive current to motor occurs if excessive current is present in the circuit and fuse fails to open. It also occurs if the wire fails shorted or the power supply surfes.

3. QUALITATIVE ANALYSIS:

For the fault tree shown in [fig.2B.page.17...] it is



JP FOR D.C. MOTOR

Fig. 2A

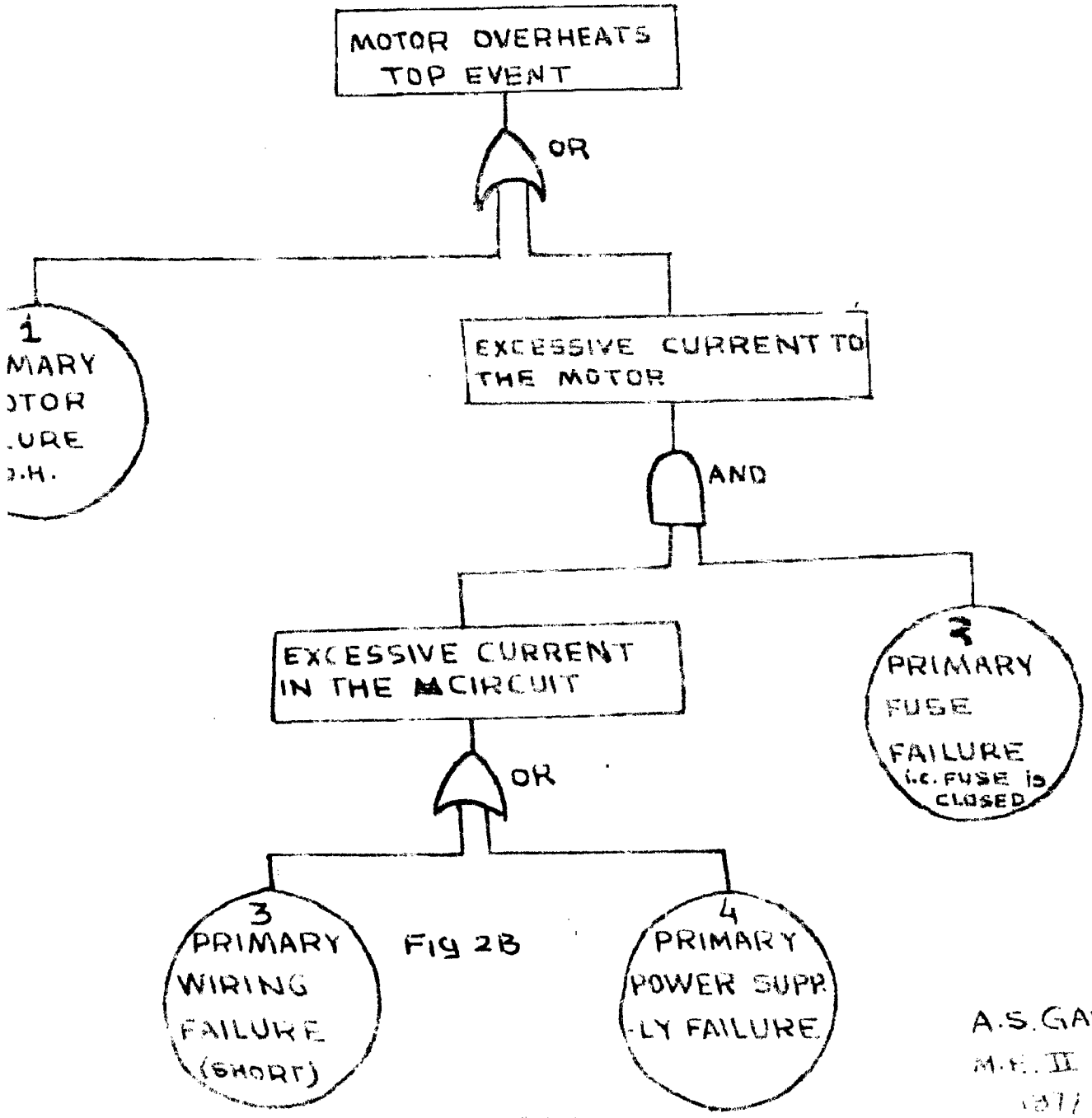


Fig 2B

FAULT TREE Fig 2

A.S. GAVANE
M.E. II SEM
(87)

possible to find the minimal cut-sets by inspection but an exhaustive method is required to be found out for larger tree configuration. The primary events are numbered from 1 to 4 which leads to top event. The minimal cut sets are (by inspection)

(1) (2,3), (2,4)

The top event is given by the boolean equation.

$$Top = 1 \cup 2 \cap 3 \cup 2 \cap 4$$

and the top event probability is given by

$$P(TOP) = P(1 \cup 2 \cap 3 \cup 2 \cap 4)$$

$$= 1-(1-P(1)).(1-P(2)).P(3).(1-P(2)).P(4)$$

'Vesely and Narvm' has suggested a computerized approach for determining the minimal cut-sets. The boolean equation implied by the fault tree is constructed by the computer. The primary events are thin turned-on one at a time and the equation is checked each time to determine wheather it is true. Next all possible combination of two primary events are turned on and again the equation is checked wheather it is true. Each time the equation is true, the collection of primary events that were turned on show cut set. After these cut sets are determined, all cut sets that are sub sets

of other cut sets are discarded to obtain minimal cut sets.

Vesely and Narum have suggested a Mole carlo approach where by appropriate weighing of primary events is used to accelerate the process of determining minimal cut sets. However, doubt that all minimal cut sets have been found is always present when Monte Carlo approach is used.

In practice both of these methods requires excessive computer time to obtain cut sets containing more than three primary events.

4. QUANTITATIVE ANALYSIS:

There are three methods for solutions to fault trees

(a) Direct simulation Apporoach
(b) Monte Carlo Methods
(c) Direct analytical solutions

The direct simulation approach uses boolean logic hard ware similar to those used in digital computor. Obviously this method is costly for implimentation.

Monte Carlo methods are perhaps the most simple in principle but in practice it is very complex. The Monte Carlo methods is not practical without the use of digital computer In this method probability data are provided as input and simula-

tion programme represents the fault tree on a computer to provide quantitative results.

Out ofthe various analytical techniques suggested, the technique of 'Kinetic tree theory' can be used for solving complex fault tree containing primary failures which are a complex function of time and repair possibilities. The solution of fault tree is obtained through the application of probability theory and differential calculus. The use of AND , OR and INHIBIT gate is allowed, Since the information is obtained as a function of time hence with regard to reliability.

C H A P T E R 3

COMPONENT DESCRIPTION

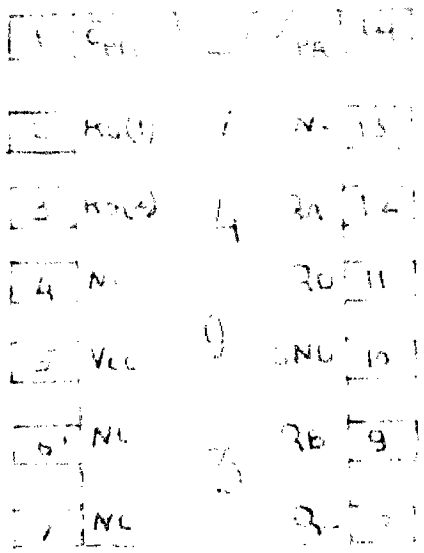
3.1 4-BIT BINARY COUNTER (TTL/MSI 9393/5493/7493):

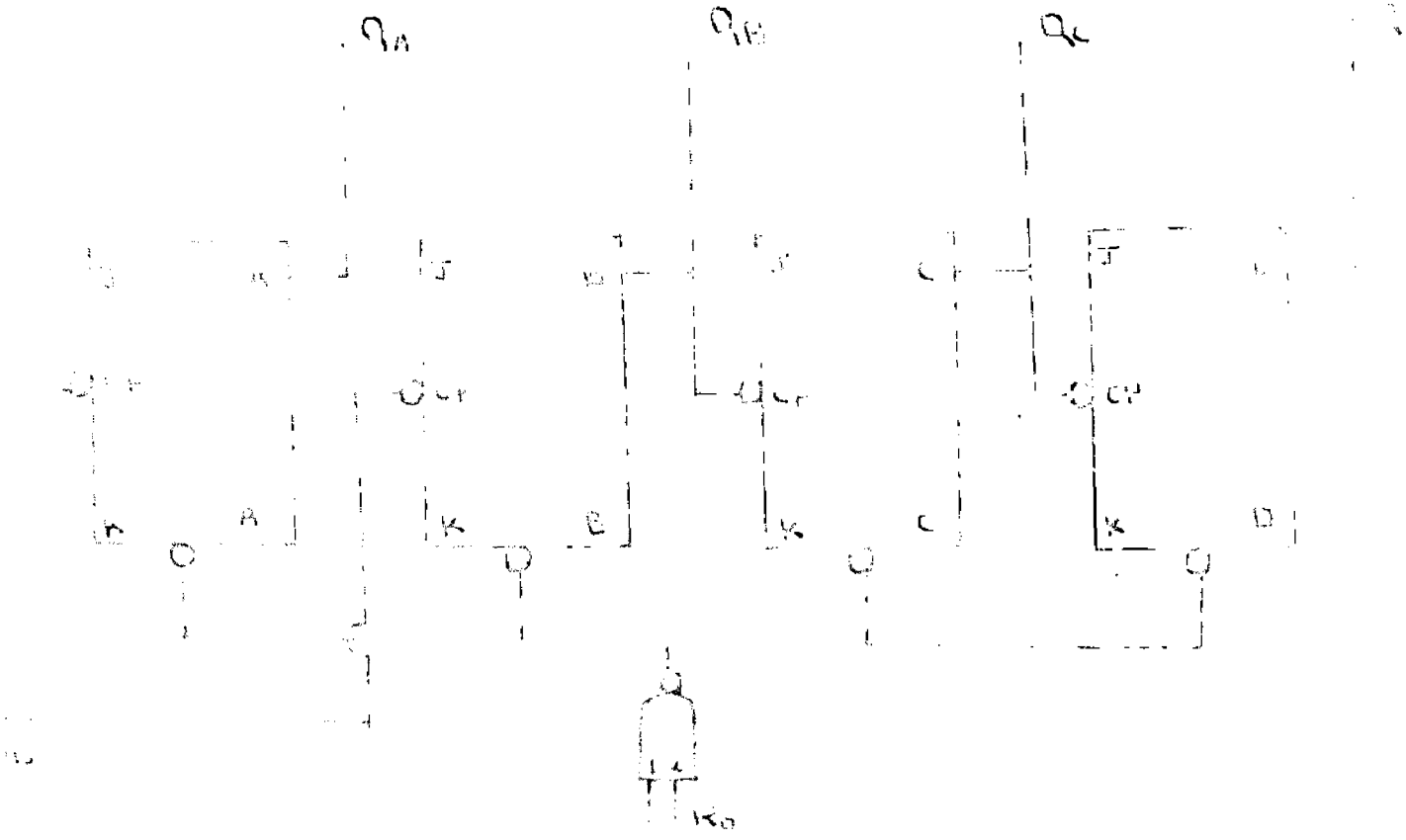
DESCRIPTION:

The TTL/MSI 9393/5493/7493 is a 4-bit binary counter consisting of four master slave flip flops which are internally interconnected to provide a divide by two counter and a divide by eight counter. A gated direct reset line is provided which inhibts the count inputs and simulteneously returns the four flip flop outputs to a LOW level. As the out put from flip flop A is not internally connected to the succeeding flip flops the counter may be operated in two independent models:

(A) When used as a 4-bit ripple through counter, out put Q_A must be externally connected to input C_{PB}. The input count pulses are applied to C_{PA}. Simulteneously division of 2,4,8 and 16 are performed at Q_A, Q_B, Q_C and Q_D out puts as shown in truth table.

(B) When used as a 3-bit ripple through counter, the input count pulses are applied to input C_{PB}. Simulteneously





FOUR BIT BINARY COUNTER

frequency division of 2,4 and 8 are available at Q_B, Q_C and Q_D output. Independent use of flip flop A is available if the reset function conside with the reset of the 3 bit ripple through counter.

PIN NAMES:

		Loading
R_o	Reset Zero input	1 U.L.
C_{PA}	Clock (Active low going edge) input	2 U.L.
C_{PB}	Clock (Active low going edge) input	2 U.L.
Q_A, Q_B, Q_C and Q_D	out puts	10 U.L.

1 U.L. = 40 μA HIGH/1.6 mA LOW

CONNECTION DIGRAM AND LOGIC DIGRAMS:

These digrams are shown in fig.3. Page 22

TRUTH TABLE

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L

table contnue

table contd....

Count	Out puts			
	Q_D	Q_C	Q_B	Q_A
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

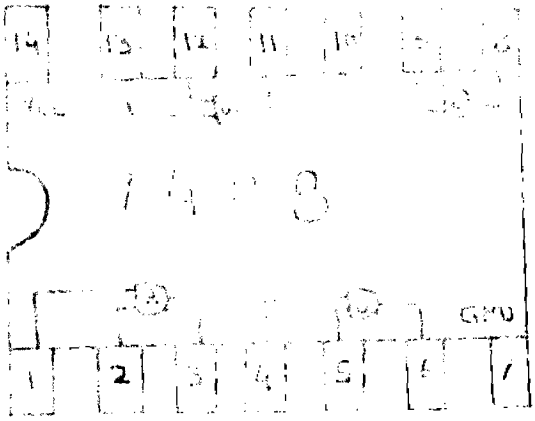
Note:

1. Out put Q_A connected to input C_{PB}.
2. To reset all out puts to LOW level both $R_o(1)$ and $R_o(2)$ input must be at HIGH Level.
3. Either (or both) resent inputs Ro(1) and Ro(2) must be at low level to count.

3.2 QUAD TWO INPUT AND GATE (TTL/SSI 9408/5408,7408):

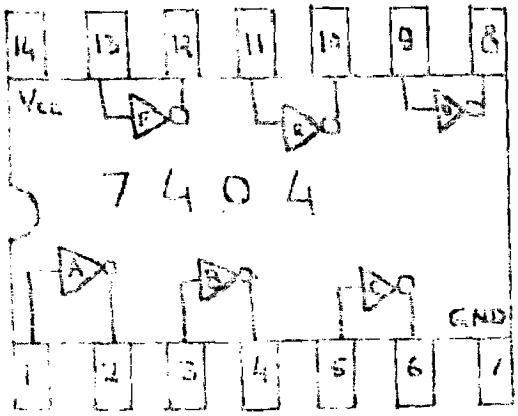
DESCRIPTION

The 7408 I.C. consist of four kndependent 2-input



7408 QUAD TWO INPUT AND GATE

FIG. 4



7404 HEX INVERTER

FIG - 5

A.S.GAVANE
M.E. II S.E.O.H.
1971

AND gates as shown in fig. 4 Page 25

1,2	Input to AND gate A
3	Output of AND gate A
4,5	Input to AND gate B
6	Output of AND gate B
7	Ground terminal
9,10	Input to AND gate C
8	Output to AND gate C
12,13	Input to AND gate D
11	OUT put of AND gate D
14	Vcc supply terminal = 5.0V

If P and Q are (say) input to a AND gate then the out put (Y) of AND gate is given by the logic

$$Y = PQ$$

3.3 HEX INVERTER [TTL/SSI 9N04/5404/7404]

DESCRIPTION

The 7404 I.C. consist of six independent inverters as given shown in fig. 5 Page 25

1. Input to inverter A
2. Output of inverter A
3. Input inverter B
4. Output of inverter B
5. Input to inverter C
6. Output of inverter C
7. Ground terminal
8. Output of inverter D
9. Input to inverter D
10. Output of inverter E
11. Input to inverter E
12. Output of inverter F
13. Input to inverter F
14. Vcc supply terminal = 5.0V

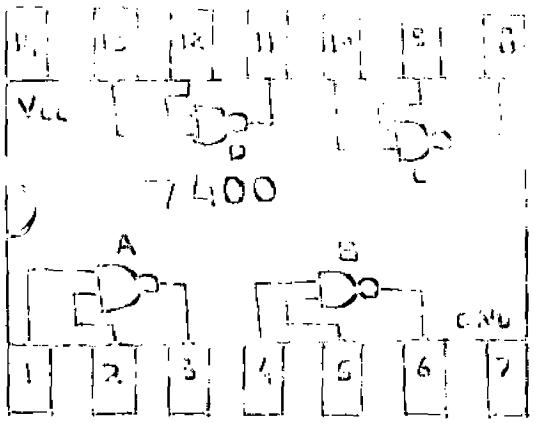
If P is the input to a inverter, the out put (Y) of inverter is given by logic

$$Y = \bar{P}$$

3.4 QUAD TWO INPUT NAND GATE [TTL/SSI 9N00/5400,7400]

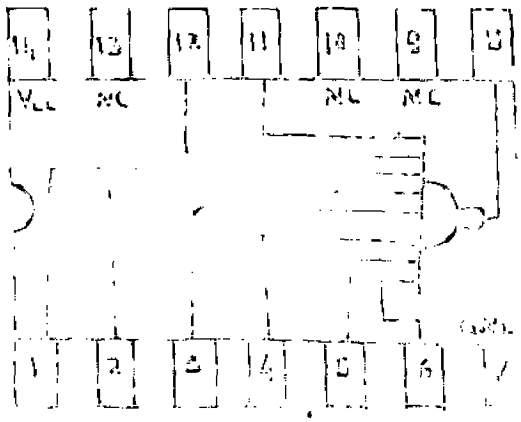
DESCRIPTION:

The 7400 I.C. consist of four independent two input NAND gates as shown in fig.6. Page 28



7400 QUAD TWO INPUT NAND GATE

FIG 6



7430 SINGLE 8-INPUT NAND GATE

FIG - 7

1,2	Input to NAND gate A
3	Output of NAND gate A
4,5	Input to NAND gate B
6	OUT put of NAND gate B
7	Ground terminal
9,10	Input to NAND gate C
8	Output of NAND gate C
12,13	Input to NAND gate D
11	Output of NAND gate D
14	Vcc supply terminal = 5.0V

If P and Q are the inputs to a NAND gate then the out put (Y) of the NAND gate is given by the logic

$$Y = \overline{PQ}$$

3.5 SINGLE EIGHT INPUT NAND GATE[TTL/SSI 9N30/5430,7430]

DESCRIPTION: Fig.7 Page 28

The 7430 I.C. consist of only one 8-input NAND gate as shown in fig.

1,2,3,4,5,6,11,12	input to NAND gate
8	out put of NAND gate
7	Ground terminal
14	Vcc supply terminal = 5.0V
9,10,13	N.C. terminals.

If P,Q,R,S,T,U,V,W forms input to NAND gate then the out put (Y) of NAND gate is given by logic

$$Y = \overline{PQRSTUVW}$$

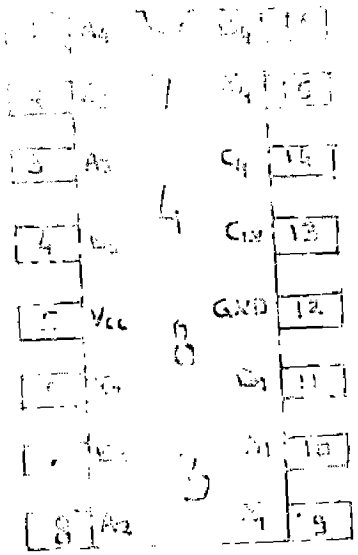
3.6 FOUR BIT BINARY FULL ADDER: [TTL/MSI 9383/5483,7483]

DESCRIPTION:

The TTL/MSI 9383/5483,7483 is a FULL ADDER which performs the addition of two 4 bit binary numbers. The sum ( ) outputs are provided for each bit andthe resultant carry (C_4) is obtained from 4th bit. Designed for medium to high speed, multiple bit, parallel add/serial-carry applications, the circuit utilized high speed high fan out TTL The implimentation of a single inversion, high speed, darlington-connected serial-carry circuit within each bit minimizes the necessaty for extensive 'look ahed and carry cascading circuits.

PIN NAMES

		Loading
A_1, B_1, A_3, B_3	Data Inputs	4 U.L.
A_2, B_2, A_4, B_4	Data Inputs	1 U.L.
C_{IN}	Carry Inpute	4 U.L.
1' 2' 3, 4	Sum Out puts	10 U.L.
C_4	Carry Out bit 4	5 U.L.



7483 4-BIT BINARY FULL ADDER

FIG - 8

	A_4	A_3	A_2	A_1
+	B_4	B_3	B_2	B_1
C_4	Σ_4	Σ_3	Σ_2	Σ_1

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CONNECTION DIGRAM:

Connection digram is shown in fig. 8. Page 31

TRUTH TABLE

Inputs				Outputs					
				WHEN $C_{IN}=0$ / WHEN $C_2=0$			WHEN $C_{IN}=1$ /WHEN $C_2=1$		
A_1/A_3	B_1/B_3	A_2/A_4	B_2/B_4	$1/3$	$2/4$	C_2/C_4	$1/3$	$2/4$	C_2/C_4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

Note: Input conditions at A_1, A_2, B_1, B_2 and C_{IN} are used to determine outputs 1 and 2 and the value of internal carry C_2. The valves at C_2, A_3, B_3, A_4 and B_4 are then used to determine outputs 3 4 and C_4

CHAPTER 4

THE EQUIPMENT AND ITS DESIGN

4.1 DESIGN PHILOSOPHY: (RELIABILITY EVALUATION THROUGH PATH SETS AND CUT SETS).

Design approach is well explained by the following illustrative examples.

Consider the system given in [fig 9A. page 34.] and the Table shown in [fig....page 37...] Let state [1] represents that a path is conducting and state [0] represents that a path is non-conducting.

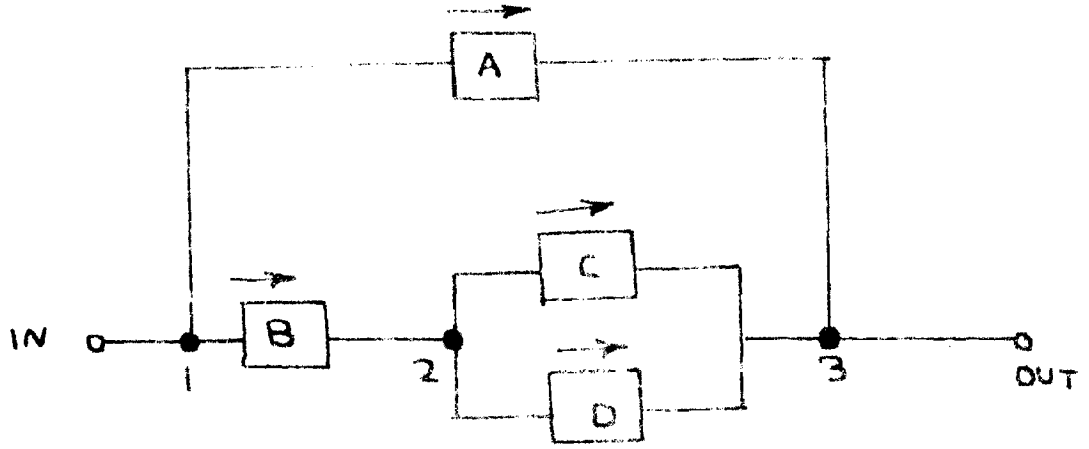
Each element in the network has two states (a) conducting (b) non-conducting. There are four such elements in the system under consideration. Therefore, the maximum possible states in which the system can exists are 2^4 i.e. 16. Those 16 states are shown in [table 1..page. 37. column..2.....] Those states can be generated by binary generator.

Further a signal can flow from node 'X' to node 'Y' when

(a) There is a path between X and Y and

(b) Signal is present at node X

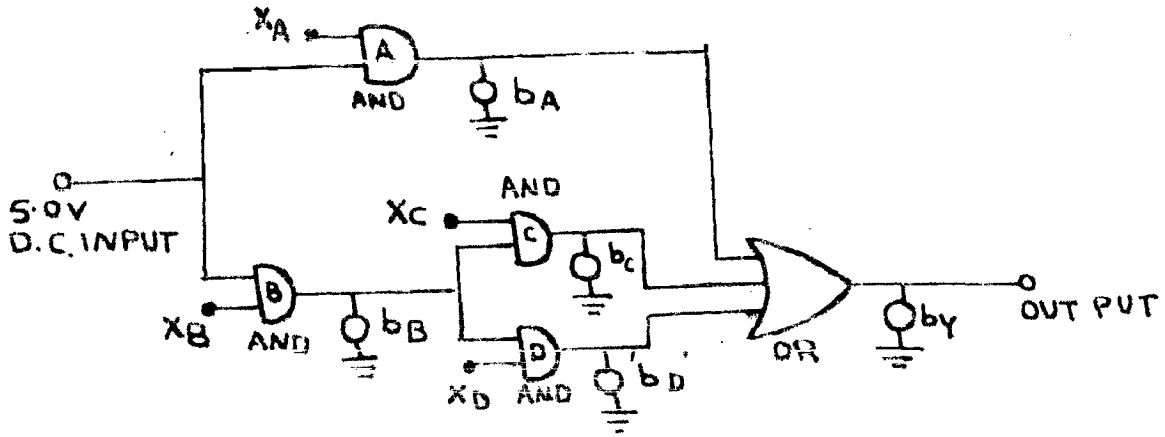
In other words it can be said that signal flows from



SYSTEM UNDER CONSIDERATION

Fig. 9A

ARROW INDICATES DIRECTION OF SIGNAL FLOW



LOGICAL SYSTEM RERRESENTATION

Fig. 9B

Fig. 9

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node X to node Y only when conditions (a) AND (b) both exists. This is equivalent of having a 2-input AND gate between X and Y.

Therefore we represent each element of the given system by a 2-input AND gate which transmits the signal in a direction in which the original element transmitts one terminal of each AND gate is used to form the given system network configuration and other terminal of each AND gate is supplied from the out put of binary generation.

If the 'Signal Inputs' (Excluding the binary input to AND gated network) +0 a AND gate (which is representing a particular element in thenetwork) are more than one, then these inputs are applied to the AND gate through an OR gate e.g. in the system of [fig.9A.page.34..] a OR gate is needed at node 3. The input to this OR gate is from the out put of, AND gate -A, AND gate-C, and AND gate D to obtain the out put indication. Similarly for the system of [fig.10A page.39...], OR gates are necessary at node 2,3 and 4 as shown

Now the state vectors for which the given system gives through and through passage to the input signal are noted [i.e. state vectors corresponding to '1' out put in column-3 of table..1..page37] These state vectors are the various 'PATH SETS' of the system and their sum gives the reliability of the given system.

Let p_A, p_B, p_C and p_D represents the reliabilities of the network elements A,B,C and D. Then reliability of whole network can be written as

$$R = p_A \cdot q_B \cdot q_C + p_A \cdot p_B \cdot q_C \cdot q_D + p_A \cdot q_B \cdot p_C \cdot q_D + q_A \cdot p_B \cdot p_C \cdot q_D$$
$$+ p_A \cdot p_B \cdot p_C \cdot q_D + p_A \cdot q_B \cdot q_C \cdot p_D + q_A \cdot p_B \cdot q_C \cdot p_D + p_A \cdot p_B \cdot q_C \cdot p_D$$
$$+ p_A \cdot q_B \cdot p_C \cdot p_D + q_A \cdot p_B \cdot p_C \cdot p_D + p_A \cdot p_B \cdot p_C \cdot p_D$$

equation..(1)

The state vectors which do not give passage to the input signal (i.e. the state vectors corresponding to '0' of the column-3 table....page.....] are known as CUT-SETS and their sum gives the expression the un-reliability (Q)

$$Q = [q_A \cdot q_B \cdot q_C \cdot q_D + q_A \cdot p_B \cdot q_C \cdot q_D + q_A \cdot q_B \cdot p_C \cdot q_D$$
$$+ q_A \cdot q_B \cdot q_C \cdot p_D + q_A \cdot q_B \cdot p_C \cdot p_D]$$

..... (2)

The reliability of the given sytem is then found by the relation

$$R = [1-Q] \qquad \text{.....} \quad (3)$$

TABLE -1

umn 1 ce ber	Column-2 Binary state at the input of AND gated network				Column-3 State of output node	Set	Column-4 Binary state at the output of AND gated network				Column 5 Output from final and gate	Column 6 Paths
	X_D	X_C	X_B	X_A			b_D	b_C	b_B	b_A		
	0	0	0	0	0	CUT	0	0	0	0	0	
	0	0	0	1	1	PATH	0	0	0	1	1	A
	0	0	1	0	0	CUT	0	0	1	0	0	
	0	0	1	1	1	PATH	0	0	1	1	1	AD*
	0	1	0	0	0	CUT	0	0	0	0	0	
	0	1	0	1	1	PATH	1	0	0	1	0	
	0	1	1	0	1	PATH	0	1	1	0	1	BC
	0	1	1	1	1	PATH	0	1	1	1	1	ABC
	1	0	0	0	0	CUT	0	0	0	0	0	
	1	0	0	1	1	PATH	0	0	0	1	0	
)	1	0	1	0	1	PATH	1	0	1	0	1	BD
)	1	0	1	1	1	PATH	1	0	1	1	1	ABD
	1	1	0	0	0	CUT	0	0	0	0	0	
	1	1	0	1	1	PATH	0	0	0	1	0	
)	1	1	1	0	1	PATH	1	1	1	0	1	BCD
)	1	1	1	1	1	PATH	1	1	1	1	1	ABCD

Notes:

1. (φ) marked pulse numbers are the desired pulse number to which the equipment should respond.

2. (*) marked pulse number are the pulses which gives the undesired out put signal.

Thus in general the various path-sets and cut-sets of the any given system can be found by the following procedure.

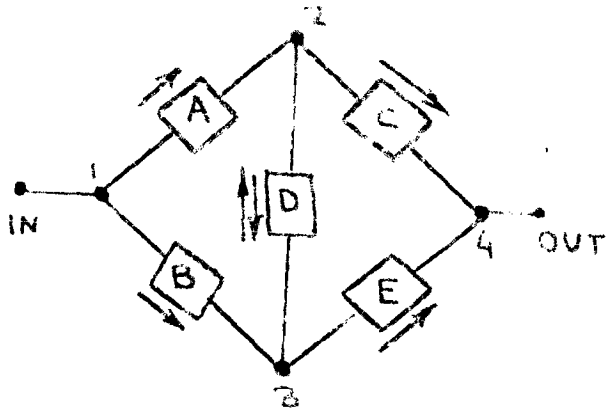
'Represent each element of the given system network by a 2-input AND gate. One terminal of each AND gate is used to form the given network configuration. The other terminal of each AND gate is supplied from the out put of binary generator. Use OR gate of signal input to the AND gate is more than one. Also use OR gate at out put node if out put is obtained from more than one source. Each input state vector which gives the out put indication represents a path set. Each input satate vector which does not give out put indication represents cut-sets. The reliability of the network between input and output node is then evaluated as explained by the above example'

This is the simplest way of evaluating reliability through path-sets and cut-sets. When the network grows complex and complex, the expression for reliability contains a large numbers of terms. This in turn needs large memory and increased mathematical operations if the equipment is to be made automatic and reliability of given system is desired in digital form.

4.2 DESIGN PHILOSOPHY:

RELIABILITY EVALUATION THROUGH MINIMAL PATH SETS AND MINIMAL CUT SETS (DESIGN APPROACH)

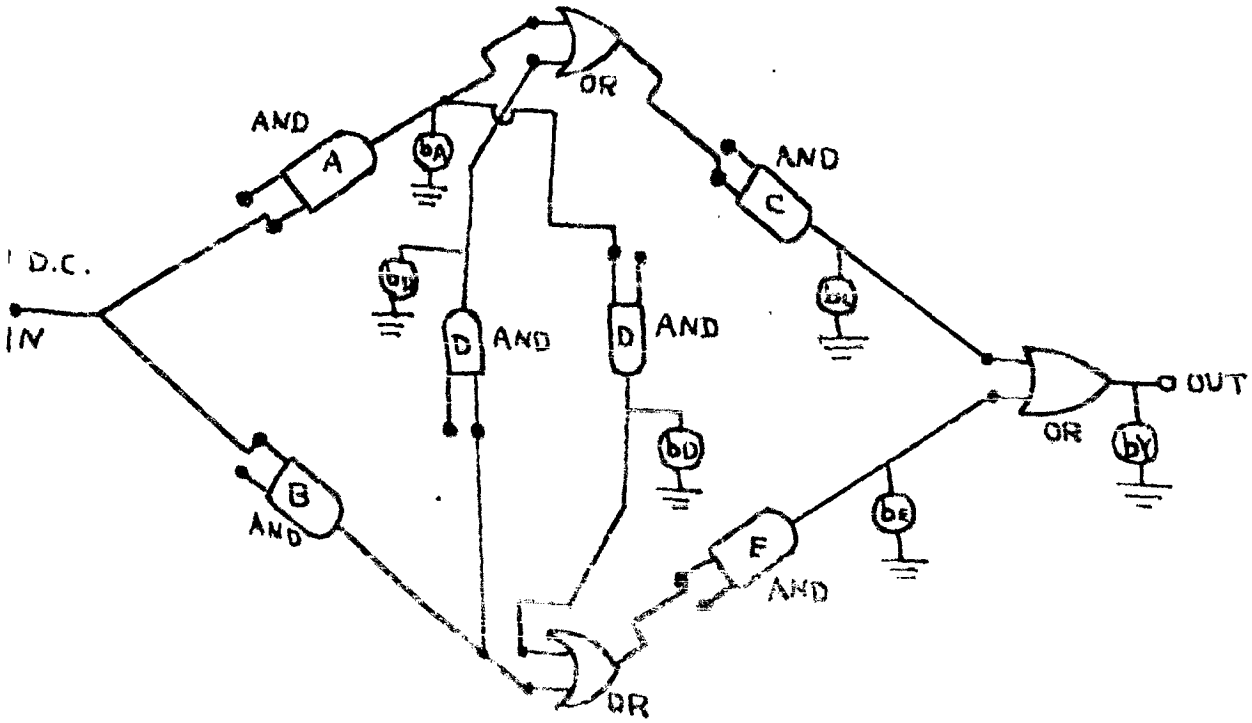
The reliability expression can also be determined if



BRIDGE NETWORK

Fig.10A

ARROWS INDICATE DIRECTION OF SIGNAL FLOW



LOGICAL REPRESENTATION OF THE SYSTEM

Fig. 10B

Fig. 10

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one can find out the paths of various sizes existing in the system network under consideration.

Consider the system of [fig.10.A page.39..]. This system is a case of non-series parallel network. Since the network is of practical size, therefore paths of various sizes can be found out by inspection.

Paths of size 1	:	None
Paths of size 2	:	(A,C), (B.E.)
Paths of size 3	:	(A,D.E), (B,D,C,)
Paths of size 4	:	(A,B,D,C), (A,B,D,E,), (A,D,C,E,), (B,D,C,E,) (A,C,B,E,)
Paths of size 5	:	(A,B,C,D,E,), (A,B,C,D,E,

Here (A,C,), (B,E), (A,D,E,), (B,D,C,) are the forward paths are minimal paths. The remaining (A,B,D,C,), (A,B,D,E,), (A,D,C,E,), (B,D,C,E,), (A,C,B,E,), (A,B,C,D,E,) and (A,B,C,D,E,) are various 'forward paths with lopp'

Reliability expression is then given by

$$R = [A.C. + B.E. + A.D.E. + B.D.C. - ABDC - ADBE - ADCE - BDCE - ACBE + 2\ ABCDE \quad .....(4)$$

If p_A, p_B, p_C, p_D and p_E are the reliabilities of elements

TABLE-2

lumn 1	Column-2					Column-3		Column-4					Column-5	Column-6
loc nbor	Binary state at the input of AND gated network					State of output node	Set	Binary state at the out put of AND gated net work					Output from final and gate	Paths
	X_E	X_D	X_C	X_B	X_A			b_E	b_D	b_C	b_B	b_A		
	0	0	0	0	0	0	CUT	0	0	0	0	0	0	
	0	0	0	0	1	0	CUT	0	0	0	0	1	0	
	0	0	0	1	0	0	CUT	0	0	0	1	0	0	
	0	0	0	1	1	0	CUT	0	0	0	1	1	0	
	0	0	1	0	0	0	CUT	0	0	0	0	0	0	
	0	0	1	0	1	1	PATH	0	0	1	0	1	1	AC
	0	0	1	1	0	0	CUT	0	0	0	1	0	0	
	0	0	1	1	1	1	PATH	0	0	1	1	1	1	ACB*
	0	1	0	0	0	0	CUT	0	0	0	0	0	0	
	0	1	0	0	1	0	CUT	0	1	0	0	1	0	
	0	1	0	1	0	0	Cut	0	1	0	1	0	0	
	0	1	0	1	1	0	CUT	0	1	0	1	1	0	
	0	1	1	0	0	0	CUT	0	0	0	0	0	0	
*	0	1	1	0	1	1	PATH	0	1	1	0	1	1	ACD*
?	0	1	1	1	0	1	PATH	0	1	1	1	0	1	BCD
	0	1	1	1	1	1	PATH	0	1	1	1	1	1	ABDC
	1	0	0	0	0	0	CUT	0	0	0	0	0	0	
	1	0	0	0	1	0	CUT	0	0	0	0	1	0	
?	1	0	0	1	1	1	PATH	1	0	0	1	0	1	BE
*	1	0	0	1	1	1	PATH	1	0	0	1	1	1	BEA*
	1	0	1	0	0	0	CUT	0	0	0	0	0	0	
	1	0	1	0	1	1	PATH	0	0	1	0	1	0	
	1	0	1	1	0	1	PATH	1	0	0	1	0	0	

1	0	1	1	1	1	PATH	1	0	1	1	1	1	ABCE
1	1	0	0	0	0	OUT	0	0	0	0	0	0	
1	1	0	0	1	1	PATH	1	1	0	0	1	1	ADE
1	1	0	1	0	1	PATH	1	1	0	1	0	1	BED*
1	1	0	1	1	1	PATH	1	1	0	1	1	1	ABDE
1	1	1	0	0	0	CUT	0	0	0	0	0	0	
1	1	1	0	1	1	PATH	1	1	1	0	1	1	ADCE
1	1	1	1	0	1	PATH	1	1	1	1	0	1	BDCE
1	1	1	1	1	1	PATH	1	1	1	1	1	1	ABCDE

Note:

1. (φ) marked pulse numbers are the desired pulse number to which the equipment should respond.
2. (*) marked pulse numbers are the pulses which gives the undesired output signal.

A,B,C, D and E then the equation (4) becomes

$$R = [p_A \cdot p_C + p_B \cdot p_E + p_A \cdot p_D \cdot p_E + p_B \cdot p_D p_C - p_A p_B \cdot p_D \cdot p_C$$

$$-p_A p_D p_B p_E - p_A p_D p_C p_E - p_B p_D p_C p_E - p_A p_C p_B p_E$$

$$+ 2p_A p_B p_C p_D p_E] \qquad .....(5)$$

As a check, wheather the relability expression given by equation (4) is correct on not, one should get R = + 1 for

$$p_A = p_B = p_c = p_D = p_E = 1 \qquad ..... (6)$$

Substituting equation (6) in equation (4)

$R = [\ 1 + 1 + 1 + 1 - 1 - 1 - 1 - 1 + 2(1)] = +1$ checked.

HOW TO ALLOCATE POSITIVE AND NEGATIVE SIGNS IN RELIABILITY EXPRESSION

1. All forward paths are give positive sign. Thus in equation (4) AC, BE, ADE and BDC are given positive sign. The forward path of maximum size is 3.

2. Then all forward paths with loops of next higher size than the forward paths of maximum size are given negative sign. Thus in equation 4 all forward paths

with loop of maximum size 4 i.e. ABDC, ADBE, ADCE, BDCE, ACBE are given negative sign.

3. Then all forward paths with loops of next higher order (than those which are alloted negative signs) are give positive sign. Thus in equation 4 all paths ABCDE and ABCDE of size 5 are given positive sign.

In summary we can say that all forward paths are alloted positive sign and forward paths with loop which are arranged is increasing order of 'size' are given alternately negative and positive sign.

As an another example consider the system of [fig.9A.. page.34..]. Here the reliability expression is given by

$$R = \underset{\text{forward path}}{A+BC+BD} - \underset{\text{forward paths with loop}}{ABC - ABD - BCD + ABCD}$$

$$= p_A + p_B \cdot p_C + p_B p_D - p_A p_B p_C - p_A \cdot p_B \cdot p_D - p_B \cdot p_C \cdot p_D$$

$$+ p_A p_B p_C \cdot p_D$$

If $p_A = p_B = p_C = p_D = 1$ then

$R = +1$ checked.

Note that all forward paths A,BC, and BD are given positive sign. The forward path of maximum size is 2. Thesefore,

forward paths with loops of size 3 (i.e. ABC, ABD and BCD) are given negative sign. All forward paths with loop of size 4 (i.e. ABCD) are given positive sign.

TO FIND MINIMAL PATH SETS

As explained earlier minimal path sets are nothing but the forward paths from input node to out put node off a network consist of 'n' nodes then the forward paths will have the maximum size of (n-1). For example consider the bridge network there are 4 nodes. Therefore maximum size of the forward path will be (4-1) i.e. 3.

Thus a equipment is fabricated, the purpose ofwhich is to filter out 'paths of various sizes' out of these all paths of size upto and including (n-1) will give forward paths (where n are the number of nodes present in the system under consideration).

To explain the design used consider the system of (fig.9A....page.34...) and (Table..1...page..37...). For this system the reliability expression consisting of paths of various sizes is

$$R = A + BC + BD - ABC - ABD - BCD + ABCD \qquad \ldots.(7)$$

The logical approach is that the equipment should respond

to the terms involving in the expression for reliability (equation (7) i.e. corresponding to the pulse number 1,6,7,10, 11, 14 and 15 only. Out of the 16 possible states in which the given system can exists.

The design approach again consist in representing each element of the network by a 2 input AND gate. One terminal of e each AND gate is used to form the given system configuration and other terminals of the AND gates are supplied from the output of binary generator. These binary state at the input of AND gated network is shown in column-2. Also the binary state at the out put of AND gated network is listed in column-4. (Corresponding to each input state vector). Corresponding to the input state vector which provide through and through pussage the input signal, the output node condition is represent by '1' otherwise by '0' as shown in column 3.

Thus we are making use of following 3 things in the design approach

1.	Input state vectors	(column - 2)
2.	Output state vectors	(column - 2)
3.	Output node condition	(Column - 3)

When we compair input state vectors of column-2 and out put state vector of column-4 it is found that corresponding to the desired terms of reliability expression (marked pulse

numbers).

(a) Out put node condition is '1' and

(b) Input state vector and out put state vector are Exactly similar.

Such exactly similar state vectors when subtracted one from another give a state vector consisting of ALL-ZEROS. This all zero vector can be inverted to give the a resultant state vector consisting of ALL-ONES. This all one state vector can be found in another way also when we add complementary binary input state vector and out put state vector. The desired pulse number gives the output indication when the resultant all one state vector together with out put node condition drives a final AND gate e.g. Take the case of desired pulse number 6th for which following information is obtained

1.	Input state vector	0 1 1 0
2.	Output state vector	0 1 1 0
3.	Out put node condition	1
	The complimentary input state vector	1 0 0 1
	Compliimentary input state vector	0 1 1 0
	✧ Out put state vector	
	Resultant = state vector	1 1 1 1

This all one state vector together with the out put node condition (which is always '1' for desired pulse number) '

'enables' the final AND gate to give the output indication.

For the undesired pulse numbers following information is obtained when column-2 and column-4 are compaired

(a) Output node condition is either '0' or '1'

(b) Input and out put state vectors are either similar or dis-similar.

The similar input and output state vectors (for undesired pulse number) on comparision gives a all-one resultant state vector. But this all-one state vector together with out put node condition which is always zero, 'DISABLES' the final AND gate to give the out put indication. The dissimilar input and out put state vector (for the undesired pulse numbers) gives a resultant state vector consisting of combination of '0' and '1' such state vector together with out put node condition again disables the final AND gate to give out put indication.

However when this design approach is used, out put indication is obtained for certain undesired pulse number. For example for system under consideration undesired out put signal is obtained corresponding to pulse no.3. Such undesired output.

The reason for indication is due to forward paths on forward paths with loop connecting the input and output nodes. The undesired out put indication due to pulse no.3 is on account

the forward path A. For the case of bridge network undesired output indication is obtained corresponding to the pulse number 7, 13, 19 and 26. For pulse no.7, the out put is due to forward path .

For pulse no.7, the output is due to forward path			AC
'	13	'	AC
'	19	'	BE
'	26	'	BE

INTERPRETATION OF RESULT:

The final information obtained from the equipment consist for desired and certain undesired terms. These undesired terms can be discarded as explained below:

The expression for reliability (like equation 7) cons: of

(a) Either foreard paths or
(b) Forward paths with loops

The undesired path sets does not fall in any of these two categorize. Thus in the system under consideration path AB does not fall in any of the two categorize mentioned above.

After discarding undesired terms, the remaining terms are either forward paths or forward paths with loop. Out of these terms of also upto and including (n-1) will give forward paths are minimal path sets (where n is the number of nodes present in the system).

TO FIND MINIMAL (CUT - SET)

When the system fed to the equipment is 'DUAL' of the original system, the path sets and minimal path sets (obtained in the manner as explained above) for the DUAL SYSTEM are nothing but cut sets and minimal cut sets for the original system.

4.3 RELIABILITY EVALUATION USING MINIMAL PATH SETS AND CUT SETS (ANALYTICALLY)

The minimal paths for the system of [fig. 9A ..page 34..] are A, BC and BD. If any how these paths can be found experimentally then the reliability can be found as explained below:

Minimal paths A, BC and BD

Combine A and BC to give

[A + BC - ABC]

Finally combine this [A+ BC - ABC]

With BD to give the reliability of the system i.e.

$R = [A + BC - ABC] + BD - ABD - BCD + ABCD$

or $R = A + BC + BD - ABC - ABD - BCD + ABCD$

This isthe desired reliability expression for the given system.

As an another example consider the system of [fig.10A. page..39...] which has AC, BE, ADE and BDC as minima/paths combine AC and BE to give

$[AC + BE - ABCE]$

Combine this with ADE to give

$[AC + BE - ABCE + ADE - ACDE - ABDE + ABCDE]$

Finally combine this with BDC to give the reliability expression for the system

$R = AC + BE - ABCE + ADE - ACDE - ABDE + ABCDE + BDC - ABCD$

$- BCDE + ABCDE$

$R = AC + BE + ADE + BDC - ABDC - ABDE$

$- ACDE - BCDE - ACBE + 2\ ABCDE$

Now we will see how reliability can be found using

minimal cut set

Consider system of [fig.....page.....]

Minimal cut sets are

AB, CE, ADE and BDC

Combine AB and CE to give

[AB+ CE - ABCE]

Combine this with ADE to give

[AB+CE - ABCE + ADE - ABDE - ACDE + ABCDE]

Combine this with BDC to give the final expression for unreliability (Q)

$$Q = AB + CE - ABCE + ADE - ABDE - ACDE + ABCDE + BDC - ABCD - BCDE + ABCDE - ABCDE + ABCDE + ABCDE - ABCDE$$

or $$Q = AB + CE + ADE + BDC - ABCE - ABDE - ACDE - ABCD - BCDE + 2ABCDE$$

Suppose the unreliabilities of A,B,C,D, and E are give as q_A, q_B, q_C, q_D and q_E then

$$Q = q_A \cdot q_B + q_C \cdot q_E + q_A \cdot q_D q_E + q_B \cdot q_D \cdot q_C - q_A \cdot q_B \cdot q_C \cdot q_E - q_A \cdot q_B \cdot q_D \cdot q_E - q_A \cdot q_C \cdot q_D \cdot q_E - q_A \cdot q_B \cdot q_C \cdot q_D - q_B \cdot q_C \cdot q_D \cdot q_E + 2\, q_A \cdot q_B \cdot q_C \cdot q_D \cdot q_E$$

The reliability is then given of expression

$$R = [1-Q]$$

4.4 THE EQUIPMENT

1. SPECIFICATIONS OF THE EQUIPMENT:

(a) The equipment is fabricated to simulate a network consisting of maximum 12 elements.

(b) Pulses (0 to 5 V magnitude) are applied manually. Actually these pulses are used to operate binary generator. The input terminal of given network system is connected to +5V D.C. while output is obtained through an OR gate.

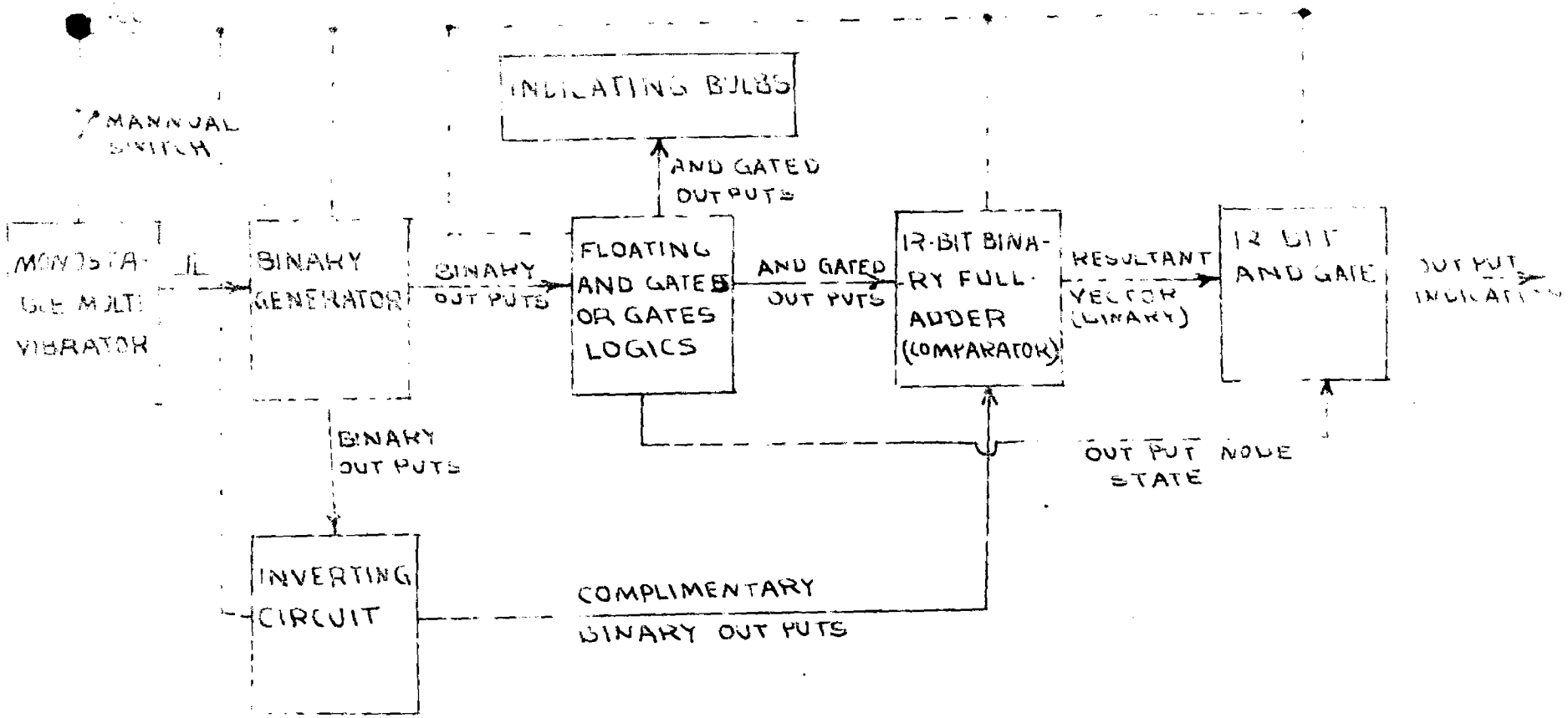
(c) The supply input to the equipment should be +5V D.C. strictly.

(d) The following information is obtained from the equipment.

(i) Path-sets
(ii) Cut sets.
(iii) Minimal path sets
(iv) Minimal cut sets of the given system

2. ORGANIZATION OF THE EQUIPMENT

The Block diagram showing the basic scheme of the



BLOCK DIGRAM OF THE EQUIPMENT

FIG - 11

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M.E. II SEM
1971

INDICATING BULBS
12 INPUT AND GATE
12-BIT BINARY FULL ADDER
FLOATING AND GATES. OR GATES LOGIC
MANNUAL PULSER
SWITCH AND INDICATION BULB

FIG 12

equipment is shown in [fig.11.page 54.] Keeping the above design philosophy in mind, the equipment is constructed in following independent unit. The equipment is designed for a network using maximum of 12 elements.

(1) 12-Bit Binary Generator

(2) Floating AND Gated Network

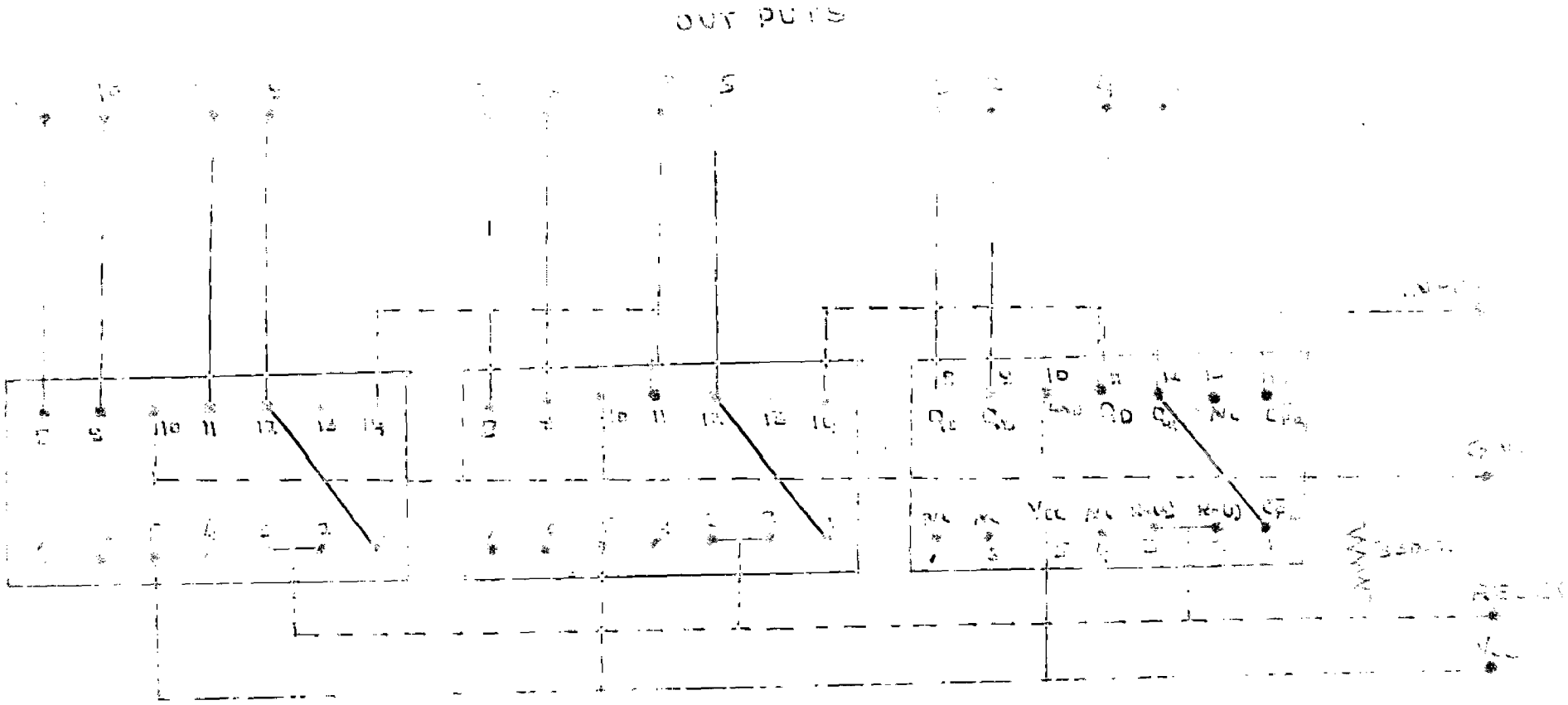
(3) 12-Bin Binary Full Adder

(4) 12-Input AND Gate

12 BIT BINARY GENERATOR: [fig.13.page 57...]

The 7493 I.C. is used for this purpose. To obtain 12 bit generator three such ICS are used in cascade by connecting pin-11 of a chip to pin-14 of the next chip in cascade. Input pulses are applied to the pin-14 of the first chip. A 330 resistance is used to ground the reset terminal. Thus divide by 2,4,8,16.....(requencies are available at out puts 1,2,3,4,5.....).

Since binary complementary out put are not available from ~~the~~ the 7493 itself. Therefore a inverter circuit is used to inv rt the binary out puts. The 7404 (the Hex Inverter) I.C. Chip is used for inverting the binary outputs. Thus if the binary out put is A,B,C,D.... then the complementary binary out puts from the inverting ckt. are $\bar{A}$, $\bar{B}$, $\bar{C}$, $\bar{D}$.....



IR BIT – BINARY GENERATOR

FIG. 13

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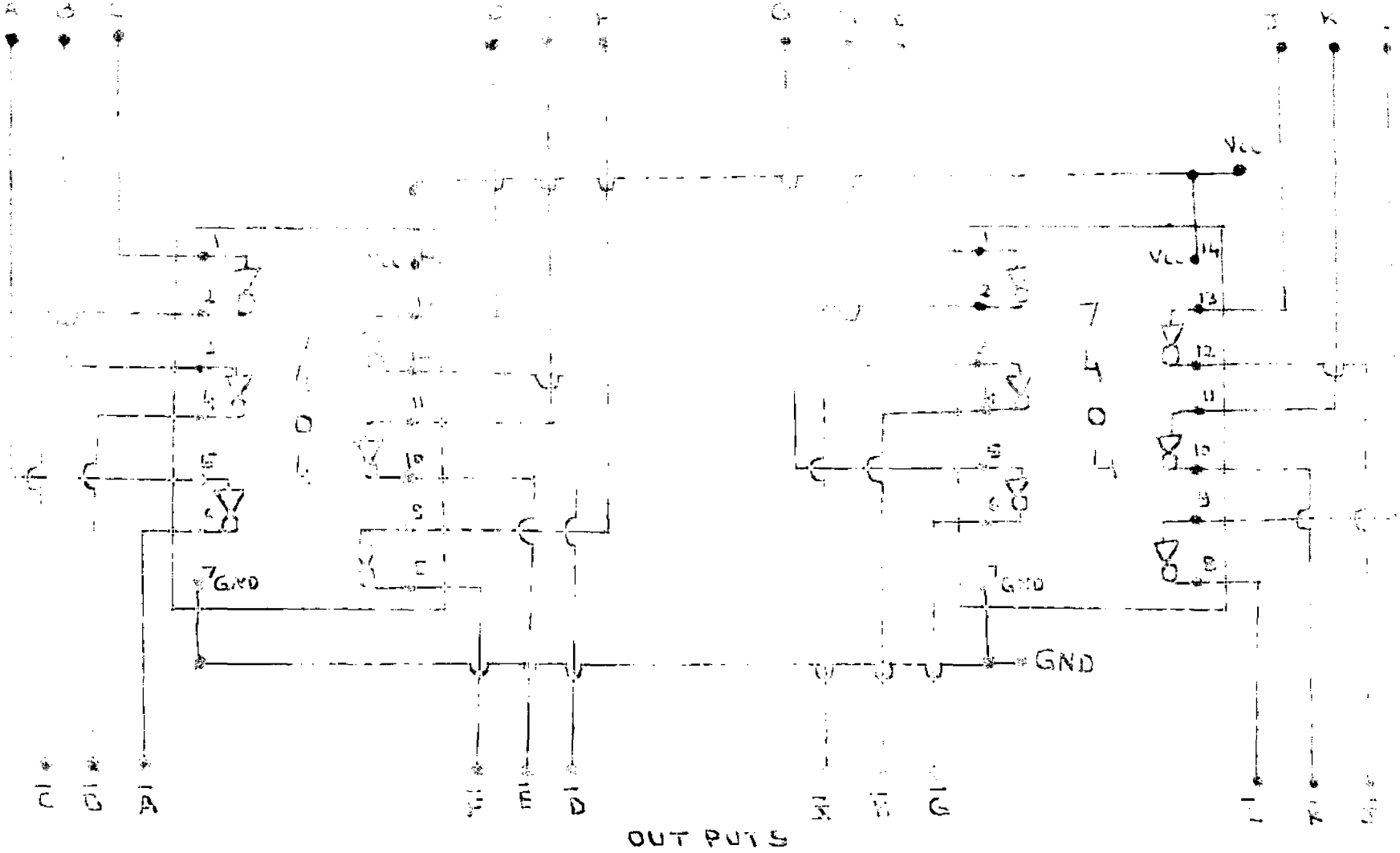

CIRCUIT FOR COMPLIMENTRY BINARY OUTPUTS

FIG-14

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ME IC E.C.P.
1977

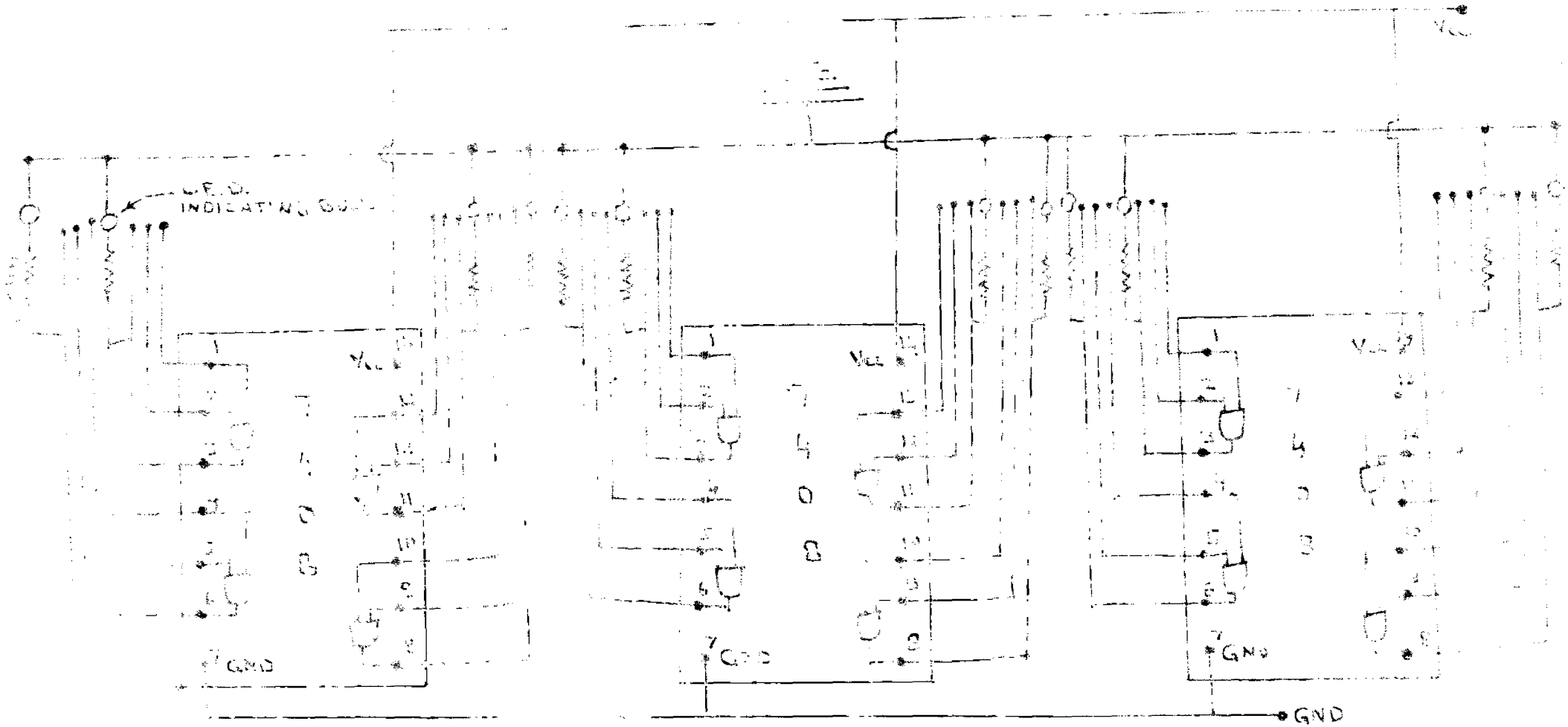
Supply voltage Vcc should be strictly 5V. Pulses are applied to the binary generation through a monostable multivibrator operated by a mannual switch. Pulses are of 0 to 5V magnetude.

FLOATING AND GATED NETWORK [fig.15..page..60....]

For this purpose 7408 I.C. Chip is used. Each 7408 chip consist of 4 independent AND gates. Total of 3 such chips are used. In this way input and out put connections of these 12 AND gates are brought to punnel board. The out put of each AND gate is provided with a indicating bulbs b_1, b_2....b_{12}, between out put of a AND gate and ground.

12-BIT BINARY FULL ADDER [Fig.16.page.61.]

The 7483 is a 4 Bit binary full addor. i.e. it per forms the addition of two 4 bit binary numbers. To obtain 12 bit binary full adder, to perform the addition of two 12 bit binary number, 3 such 7483 are used in cascade by connecting pin 14 of one chip to pin 13 of next chip in cascade i.e. by connecting carry input of one chip to C_{IN} of next chip in cascade. Pin-13 i.e. carry input pin of first I.C. in cascade is grounded. The carry-out put of addition of 12 bit number is obtained from the pin-14 of last I.C.



FLOATING AND GATES

RESISTANCE 440Ω EACH

FIG - 15

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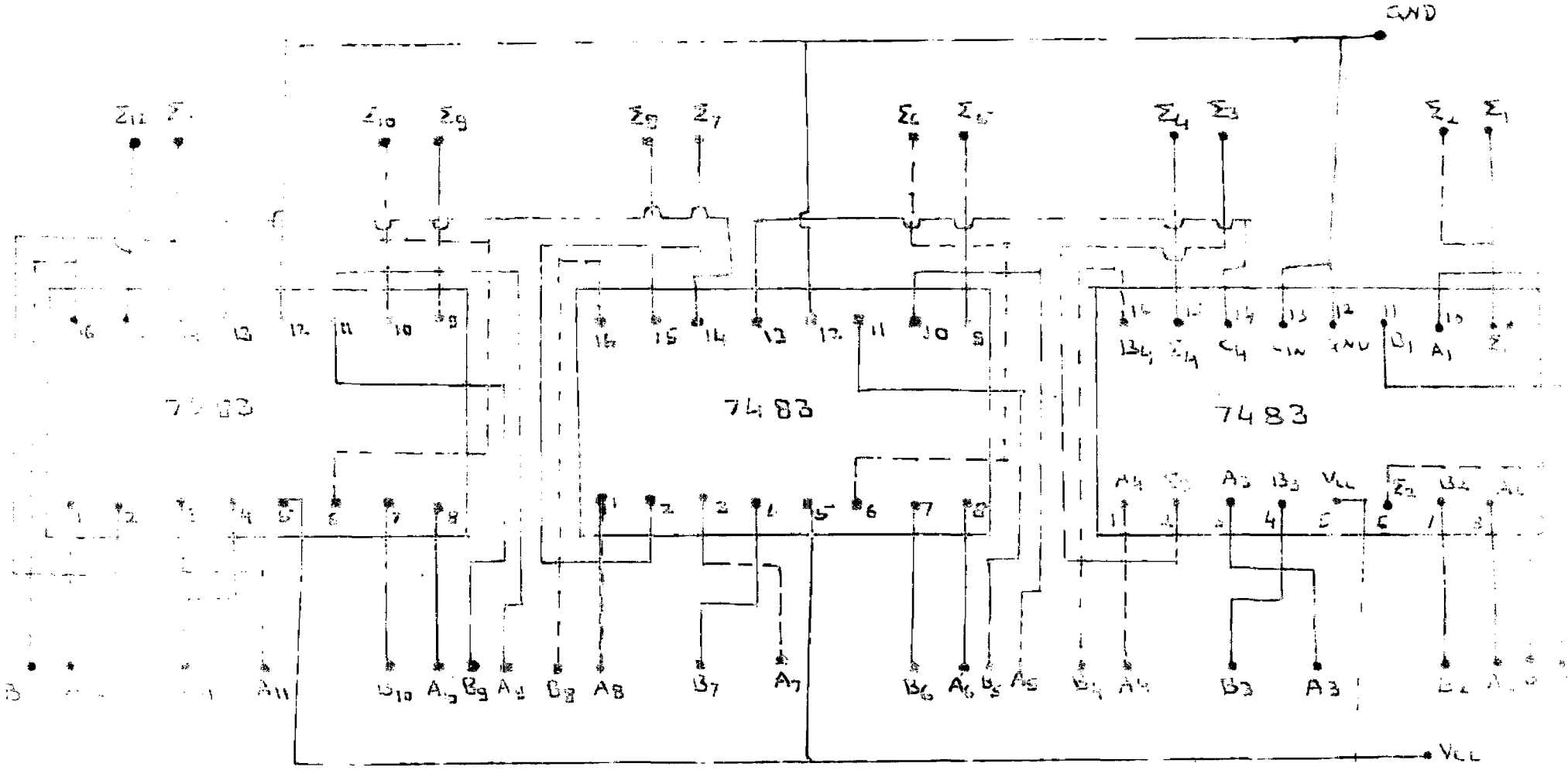


BINARY FULL ADDER

FIGURE 16

A.S. GAVANI

M.E. II [illegible]

19

in cascade. The sum is obtained in the following manner

A_{12}.....A_4 A_3 A_2 A_1

\+

B_{12}.....B_4 B_3 B_2 B_1

Carry output from pin 14 Σ_{12} Σ_4 Σ_3 Σ_2 Σ_1

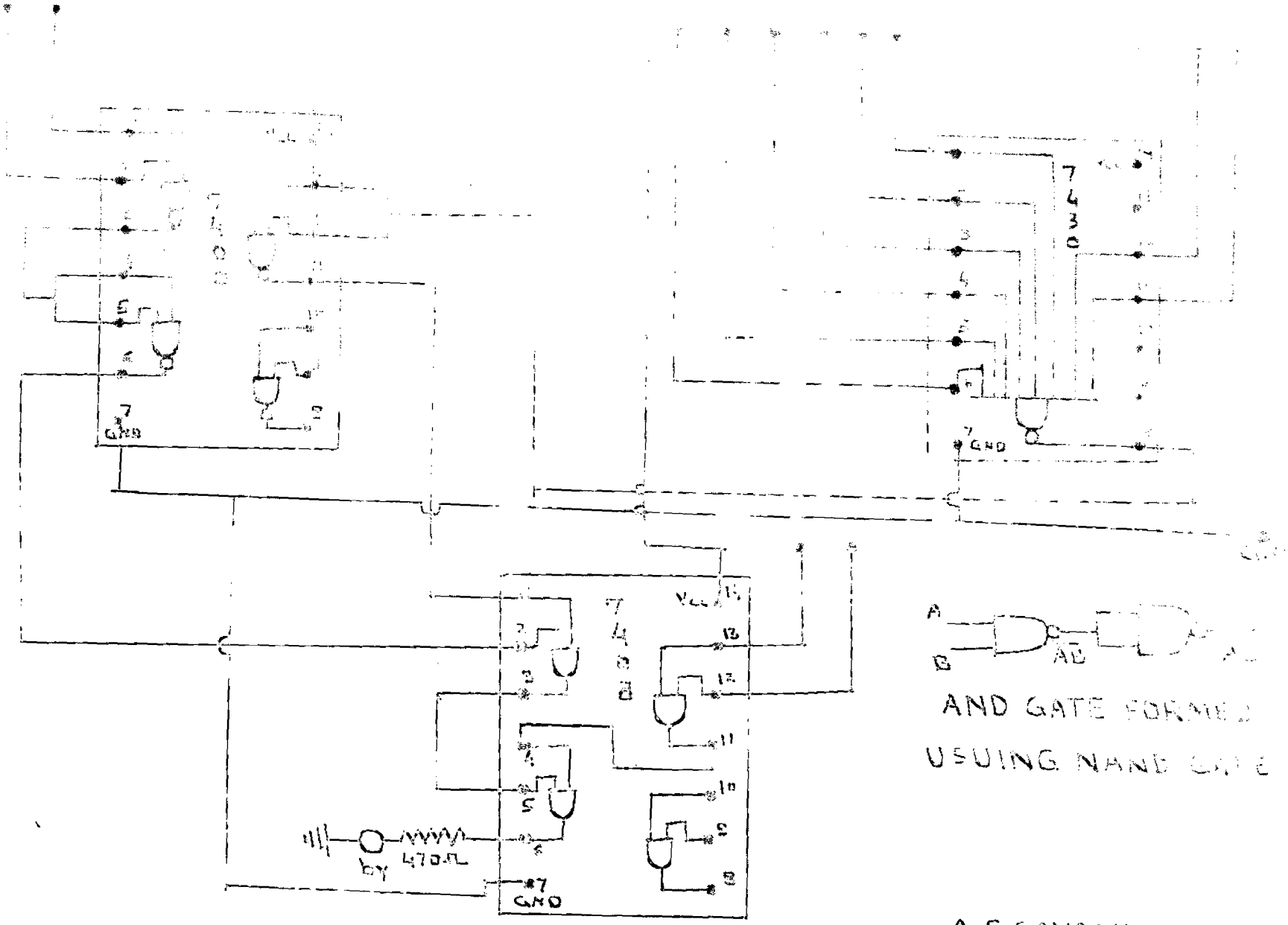
All inputs A_1, A_2, A_3.....A_{12}, B_1, B_2, B_3.....B_{12} and all out puts Σ_1 Σ_2 Σ_3 Σ_{12} are brough to pannel board. This 12 bit binary full adder can be used to porform the addition of say 5 bit binary number. Actually we are not interested in getting actual sum, but the resultant vector.

12-BIT AND GATE [Fig..17...page.63.]

This is the final AND gate in the equipment to which resultant state vector (from output of 12 bit binary full adder) and the out put node condition are fed. This gate works only when all the inputs are at state '1', otherwise not. To construct a 12 bit AND gate. following types of I.C. are used.

7400 Quad two input NAND gate

7430 single eight input NAND gate



2 INPUT AND GATE

AND GATE FORMED USUING NAND GATE

FIG-17

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ME II SEM
19

7408 Quad two inputAND gate.

A AND gate can be formed using 2 NAND gate.by using the following logic

4.5 EXPERIMENTAL PROCEDURE

1. Represent each element of the given system by 2-input AND gate one terminal of each AND gate is used to form the given system configuration while other terminals are supplied from the out put of binary generator. Use the OR gates if the 'signal in put to a AND gate is more than one. Also use the OR gate at the out put if out put is obtained.

2. If in a element the signal can flow in either direction (e.g. the bridge arm ofthe bridge network system), then represent such paths by two back to back AND gate. Such two back to back AND gates are supplied from the same binary out put e.g. the two AND gates representing the bridge are supplied from the same binary out put. X_D.

3. Keep the terminals open which are not in use.

4. In order to find the path sets and cut sets of the given system observe the state of out put node (shown by the indicating bulb by). All input state vectors (shown by the

indicating bulbs) which gives the conducting state '1' of the out ut node represents the various path sets. State vectors which gives the non-conducting state of out put bulb are the various cut sets.

5. To find the minimal path sets. Supply one set of terminals A_1, A_2, A_3.....of 12 bit binary full adder from the out put $\bar{A}$, $\bar{B}$, $\bar{C}$, $\bar{D}$.... of the complimentary binary out put. The other set B_1, B_2, B_3 .....of the full addor are supplied from the out put of corresponding AND gates used to form the given system configuration.

6. The sum out puts Σ_1, Σ_2, Σ_3..... and state of out put node is fed to the final 12 input AND gate keep all the terminals of 12 input AND gate which are not in use. The terminals which are left open are at high state.

7. Note the state shown by the indicating bulbs whenever the output indication is obtained.

8. Discard the undesired terms from the final information. as explained earlier. Out of the remaining terms select terms upto and including the size of (n-1) where n are the number of nodes in the given system. Those selected terms will give minimal path sets.

9. To find the cut set feed the dual of given system on the pannel board and apply the procedure for find finding

minimal path sets. The minimal path sets of the dual network are minimal cut sets of the original network.

CHAPTER 5

CIRCUIT MODIFICATIONS

A difficulty arises when the input of binary generator is driven from a mechanical switch directly. Contact Bounce in mechanical switch causes the generation of a twin of pulses at each operation. To avoid such difficulties following alternatives can be used.

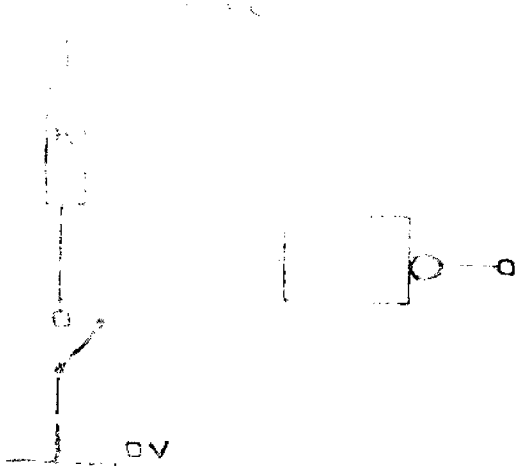
1. In the simple arrangement shown in [fig.18..page..69] the use of resistor R reduces the possibility of noise pick-up when the switch is open.

2. Alternatively if a change over switch is available then a pair of cross coupled gate may be used as shown in [fig..19..page..68...].

3. Other alternative (which is used in the equipment being fabricated) consist in triggering a one shot monostable multivibrator by a switch and the out put of monostable multivibrator is used to drive the input of binary generator. This method is designed and discussed in detail in the following paragraphs.

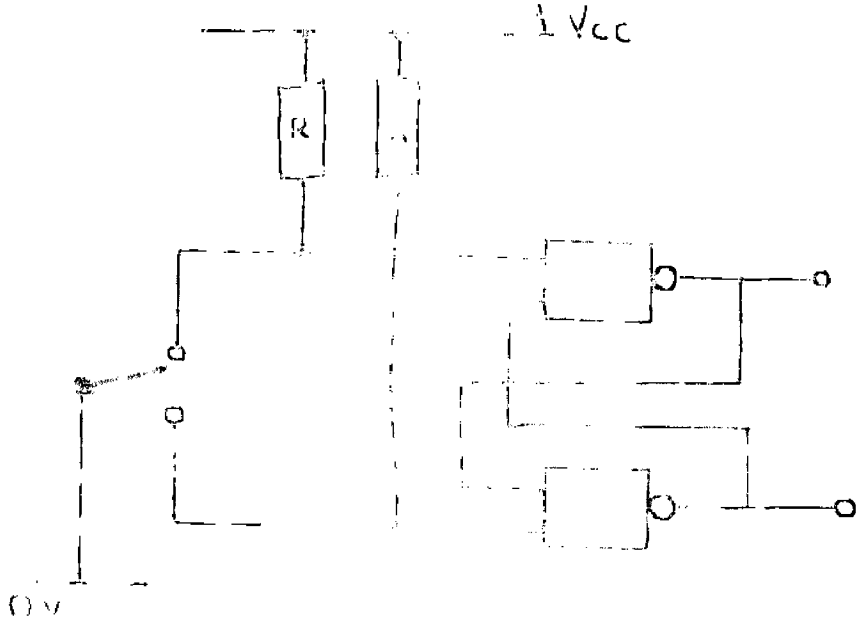
OPERATION OF MONOSTABLE MULTIVIBRETOR:

Refer [fig.20...page..69...] which shows the schemo used



TTL GATE DRIVEN BY MECHANICAL CONTACT

FIG 18



TTL GATE DRIVEN BY MECHANICAL CONTACT

A CROSS COUPLED SWITCH

A value of R should be

$(V_{IH\,MIN} - V_{OL\,MAX}) / I_{IH}$

i.e. $V_{IH\,MIN} = 2V$, $V_{OL\,MAX} = 0V$

$(2 - 0) / 40\,\mu A$

$50\,k\Omega$

FIG 19

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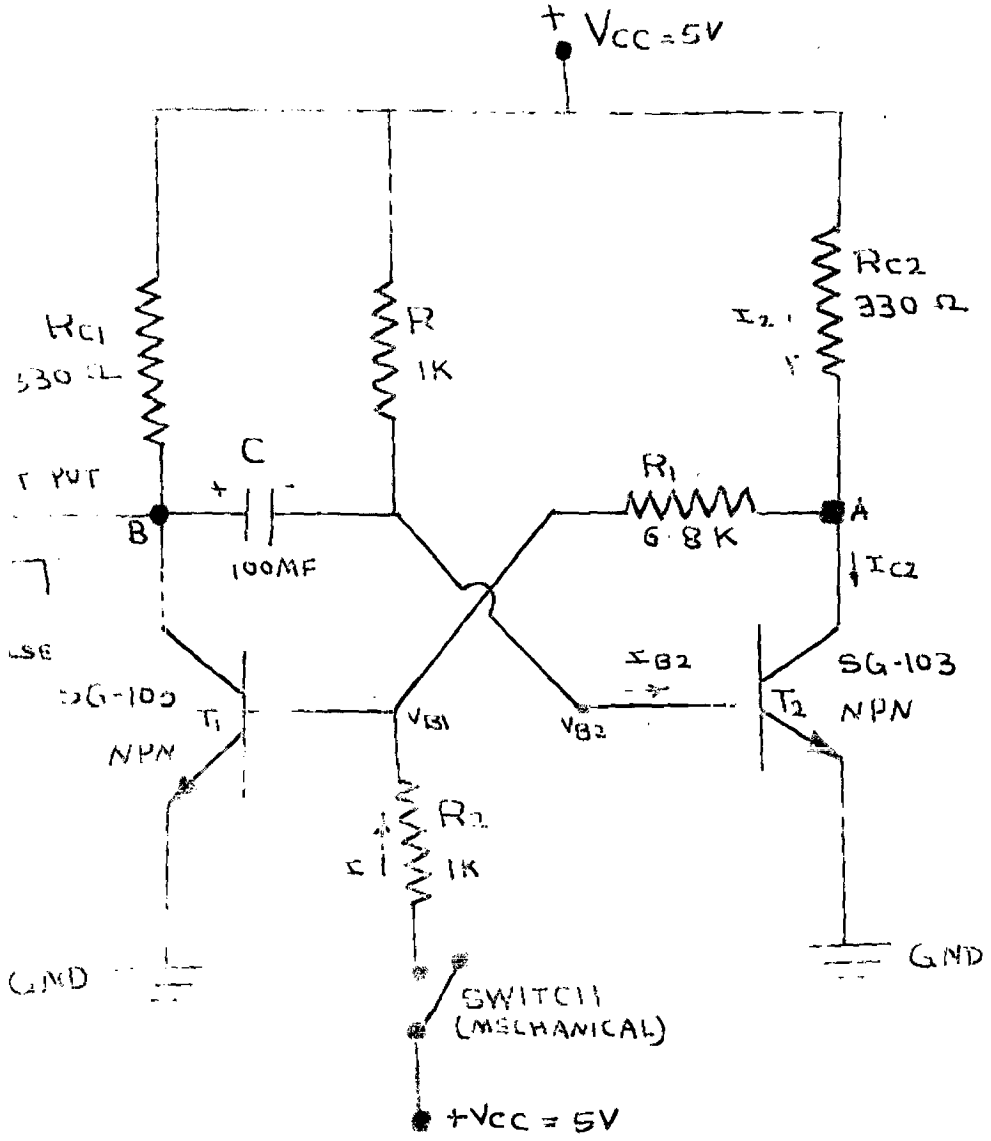

MONOSTABLE MULTIVIBRATOR ARRANGEMENT TO REPLACE MECHANICAL SWITCHING

FIG—20

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MIT SLOAN

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to drive the input of binary generator.

A monostable multivibretor has only one stable state. Let in this stable state transistor T_2 is ON and T_1 is OFF. When a short the pulse is applied the base of T_1, through the mechanical switch, T_1 is brought to ON condition with T_2 OFF. thecapacitor c which was charged to a voltage of Vcc with the polarity shown during the stable state of the multivibrator, causes a -Vcc volts at the base of T_1. Thus T_2 is brought to OFF. The capacitor now discharges through R and hence the voltage at the base of T_2 rises in potential and as soon as this potential rises above zero volts, the T_2 is brought to ON with T_1 OFF.

Thus when a short positive pulse is applied through a switch, the stable state (T_2 ON, T_1 OFF) is changed to un-stable state (T_2 OFF, T_1 ON) temporarily. The circuit regains its stable state after a time.

$$T = 0.7\ RC$$

DESIGN CONSIDERATIONS:

Select SG-103 NPN Transistor. This has following specifications.

$BV_{CBO} = 30V$ $\quad\quad$ $I_c = 0.25A$

$BV_{CER} = 24V$ $\quad\quad$ h_{FE} = Min/Max = 40/300

BV_{EBO} = 5.0V at V_{CE} = 5V and I_C = 150 mA

For a transistor to be in saturation following conditions must be satisfied

1. Base current $\frac{\text{Collector Current}}{\beta_{min}}$

2. Base-Emitter junction must be forward biased.

Consider stable state (with switch open) we have T_2 ON and T_1 OFF

$$I_{Cmax} = 0.25A$$

$$I_{B2max} = \frac{I_{Cmax}}{\beta_{min}} = \frac{0.25}{40} = 6mA$$

This means base of T_2 can carry a max. of 6mA for T_2 to be ON

Let I_{B2} = 5 mA (assumed) which the base can take safely

$$R = \frac{V_{cc}}{I_{B2}} = \frac{5V}{5mA} = 1K$$

Assume a 330 resistance in the collector of T_2

then $I_{C2} = \frac{5.0}{330} = 15$ mA

Base current corresponding to I_{C2} = 15 mA required to bring T_2 in ON condition

$$I_B = \frac{15mA}{40} = 0.4 \text{ mA}$$

Actual base current is 5 mA.

Also V_{B2} is positive 5V this make base emitter junction of T_2 forward biased.

Therefore, both conditions for the transistor to be in saturation are full-filled

T_2 becomes ON with V_{C2} = OV

Since switch is open voltage at the two ends of the voltage divider (formed by R1 and R2) are zero V_{B1} is zero volts

Hence T_1 is cut-off with V_{C1} = + 5V

Now consider that switch is closed and a short pulse is applied to thebase of T_1. The transistor T_1 is forward biased with a voltage given by

$$V_{B1} = Vcc - \frac{V_{cc} R_2}{R_1+R_2} = 5 - \frac{5x\ 1000}{6800 + 1000}$$

$$= + 4.36 \text{ V}$$

Thus T_1 is now ON with V_{C1} = 0 Volts

Thus when switch is open, out put voltage at B is + 5 V and when switch is closed the out put voltage at B is applied OV. This out put from B is applied to input (pin 14) of binary generator. Out put from A can also be used to drive the input of binary geneator. In the equipment out put from B is connected to the pin 14 of binary generator.

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