NANOSCALE FINFETS: DEVICE AND CIRCUIT DESIGN METHODOLOGY

A DISSERTATION

Submitted in partial fulfillment of the
requirements for the award of the degree
of
MASTER OF TECHNOLOGY
in
ELECTRONICS AND COMMUNICATION ENGINEERING
(With Specialization in Semiconductor Devices and VLSI Technology)

By

SAURABH KUMAR NEMA

DEPARTMENT OF ELECTRONICS AND COMPUTER ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY ROORKEE
ROORKEE-247 667 (INDIA)

JUNE, 2010

CANDIDATE'S DECLARATION

I hereby declare that the work which is being presented in this dissertation report, entitled **"Nanoscale FinFET: Device and Circuit Design Methodology"**, and is being submitted in partial fulfillment of the requirements for the award of the degree of **Master of Technology** in **Semiconductor Devices and VLSI Technology**, in the Department of Electronics and Computer Engineering, Indian Institute of Technology Roorkee, is an authentic record of my own work, carried out from June 2009 to June 2010, under the guidance and supervision of **Dr. Anand Bulusu**, Assistant Professor and **Dr. A. K. Saxena**, Professor, Department of Electronics and Computer Engineering, Indian Institute of Technology Roorkee.

The results embodied in this dissertation have not been submitted for the award of any other Degree or Diploma.

Date: 24/06/2010

Place: Roorkee

Saurabh Kumar Nema

CERTIFICATE

This is to certify that the statement made by the candidate is correct to best of my knowledge and belief.

Date: 24/6/10

Place: Roorkee

B. Anand

Dr. Anand Bulusu, Assistant Professor,
Department of Electronics & Computer,
Indian Institute of Technology, Roorkee

Date: 24/6/10

Place: Roorkee

Dr. A. K. Saxena, Professor,
Department of Electronics & Computer,
Indian Institute of Technology, Roorkee

ACKNOWLEDGEMENT

I would like to express my deep and sincere gratitude to my supervisor, Dr. Anand Bulusu, Assistant Professor, Department of Electronics and Computer Engineering at Indian Institute of Technology Roorkee. His supervision, advice, and guidance from the very early stage of this research as well as giving me extraordinary experiences throughout the work have been of great value for me not only for this work but also for my life. Above all he provided me steady encouragement, care and support in various ways throughout my work. Working under him will always be a pleasant experience in my memory.

I gratefully acknowledge to Dr. A. K. Saxena, Professor, Department of Electronics and Computer Engineering at Indian Institute of Technology Roorkee for his advice, guidance and support as my supervisor. I am indebted to him for his lectures on physical electronics and semiconductor materials, which immensely helped me in understanding concepts of Nano-scale FinFET, which made him a backbone of this research and so to this thesis. He gave me freedom to explore ideas on my own and guided whenever I was in need for help. Again I gratefully thank him for his valuable comments on this thesis.

I am very grateful to Dr. Sanjeev Manhas and Dr. Sudeb Dasgupta for their comments and guidance on my work time to time.

I am very grateful to Angnada B. Sachid and Mayank Srivastava research scholar, IIT Bombay, for guiding me the fundamentals of tool, and device design which we used in this work. They are my role models for hard work.

I would like to convey my sincere gratitude to my senior and friend Tapas Dutta, who helped and guided me throughout my work in all matters regarding Sentaurus simulations and device designing concepts.

My hearty thanks to all my friends and research scholars of Microelectronics and VLSI lab their help and support during my dissertation work. I extend my sincere thanks to rest of the faculty in the Department of Electronics and Computer Engineering at Indian Institute of Technology Roorkee, from whom I learned a lot.

My parents deserve special mention for their inseparable support, love and prayers. They are source of my motivation and cause of my being at this position, also lots of thanks for my loving and caring siblings.

Saurabh Kumar Nema,

M. Tech. (SDVT),

IIT Roorkee.

ABSTRACT

Double gate FinFET has emerged as one of the most promising device that can replace bulk MOSFET as we approach sub-45 nm technologies. In these devices, the short channel effects are reduced because of better gate control and the use of a thin and lightly doped channel. In this dissertation report, a detailed analysis of the various scaling issues pertaining to DG FinFETs has been carried out through 2D simulations using a state of the art device simulator. Underlap FinFET device is used in this work because of it's superior subthreshold leakage immunity than overlap FinFET devices.

For analyzing circuit aspects of FinFET device, a Standard Cell consisting Inverter, NAND, NOR and SR Latch were simulated using mixed mode simulation with and without external parasitics. We observed that in combinational cells, impact of internal parasitics of the device is much more than that of interconnect parasitics.

We propose an optimized FinFET device design, such that circuit performance is improved. The Source/Drain extension parameters that we consider are pad doping concentration, extension spacer dielectric constant, gate oxide thickness (t_{ox}), asymmetric doping profile and asymmetric spacer dielectric constants on source-drain side ($K_{S\ Ext}$). We observed that by optimizing t_{ox}, $K_{S\ Ext}$ device performance can be further improved. The value of t_{ox} much more than its ITRS projected value can be used. We show using simulation that applying asymmetric device design with source spacer of a high dielectric constant improves device performance significantly.

List of Figures

List of Tables

List of Abbreviations

Abbreviation	Expansion
CMOS	Complementary Metal-Oxide Semiconductor
DG	Double Gate
FinFET	Fin structure Field Effect Transistor
SOI	Silicon on Insulator
BTBT	Band to Band Tunneling
I_{on}	ON state Current
I_{off}	OFF state Current
TCAD	Technology Computer-Aided Design
SRH	Shockley–Read–Hall
DIBL	Drain Induced Barrier Lowering
GIDL	Gate Induced Drain Leakages
SCE	Short Channel Effect
PTM	Predictive Technology Model
TEM	Transmission Electron Microscope
SEM	Scanning Electron Microscope
GUI	Graphical User Interface
T_{fin}	Fin Thickness
L_g	Gate Length
L_{ext}	Extension Region Length
T_{gate}	Gate Thickness
t_{ox}	Gate Oxide Thickness
V_t	Threshold Voltage
L_{eff}	Effective gate length
L_{phy}	Physical gate length
$L_{underlap}$	Gate Underlap length
L_{over}	Gate overlap length
SS	Subthreshold slope

SDE	Source/Drain Extension
W_{fin}	Fin Width
L_{SD}	S/D Pad Length
N_{fin}	Channel Doping
N_{SD}	Pad Doping
T_{pHL}	Logic High To Logic Low Delay
T_{pLH}	Logic Low To Logic High Delay
DRAM	Dynamic Random Access Memory
ITRS	International Technology Roadmap for Semiconductors
NTRS	National Technology Roadmap for Semiconductors
C_{inv}	Input Capacitance of Inverter
C_p	Parasitic Capacitance at Drain Terminal
$K_{S\ Ext}$	Spacer Dielectric Constant on Source Side
$K_{SD\ Ext}$	Spacer Dielectric Constant on Drain Side
S_{Ext}	Extension Region on Source Side
FO4	Fan-Out 4
t_{rise}	Rise Time
t_{fall}	Fall Time
$T_{o/p\ rise}$	Output Rise Time
$T_{o/p\ fall}$	Output Fall Time
$R_{D\ Ext}$	Drain Extension Region Resistance
$R_{S\ Ext}$	Source Extension Region Resistance
$R_{S/D\ pad}$	Source / Drain Pad Resistance

Table of Contents

CHAPTER 1

INTRODUCTION

1.1 Background

The evolution and growth of the semiconductor industry is governed by downscaling of device dimensions. CMOS technology played a major role in downsizing the device and so circuit dimensions because of its high compact density. International Technology Roadmap for Semiconductors (ITRS) guides and predicts the growth of semiconductor industry [1], it predicts to achieve gate length down to 20nm by 2014.

With scaling to this extent several malfunctions in the device operation start occurring, some major issues [2] are the non-linear scaling of the threshold voltage, the control of the short channel effects and the hot carrier reliability. Along with this some technology limitations are there such as the selection of the thin gate dielectric and lithography limitations. Answers to these problems will decide the scaling trends for future.

Hisamoto et al. [3] reported the first successful operation of FinFET for NMOS-devices in 2000 and Huang et al. [4] reported it for PMOS-device in 2001. The multi-gate device has some attracting features which motivated to continue scaling trends with them, these are resemblance of it's structure with that of conventional MOSFET and it's enhanced control over channel which reduce the subthreshold leakages to a great extend without increasing the substrate doping [5]. FinFET is a member of multi-gate devices having two gates so it is called as Double Gate FinFET or just DG-FinFET. Multi-gate devices can be achieved by changing device geometry in such a way that the body is kept thin enough, low doped and wrapped around by the gate. . Thus the whole body is under the gate control. Devices with gate length of 18nm and gate oxide thickness of 2.5nm have been experimentally demonstrated with acceptable short-channel characteristics [4].

With shrinking device dimensions narrow dimension, effects start dominating and worsen the proper device operations. FinFET has reduced narrow dimension effects than bulk MOSFET. Thus it has lower subthreshold leakages, improved I_{on}/I_{off} and sharp subthreshold slopes which allows for better switching-off in the device. In FinFET structures threshold voltage is increased by increasing gate control and reducing I_{off} without the use of heavy channel doping, so it

reduces the problem of random doping fluctuations, mobility degradation in channel by carrier scattering, drain induced barrier lowering (DIBL) and drain to body BTBT leakage currents [6].

1.2 Thesis Contribution

In this work, various scaling issues in FinFET with channel length of 16 nm are investigated in detail through device simulations using a numerical device simulator. The efforts of scaling gate insulator thickness, extension region doping profile, source/ drain pad doping and spacer dielectric constants are analyzed.

FinFET device with 16nm gate length is used to create different standard circuits such as Inverter, NAND, NOR, SR NAND latch without considering effects of the parasitic resistance and capacitance and with including their effect which dominate in deciding circuit performance.

Impact of these parameter variations on the circuit performance is analyzed and leads towards developing a device scaling methodology so as to maintain the optimized performance with respect to delay and power which also ensures simplicity in device fabrication. Ring oscillator with 3-stages and Inverter with fan out 4 load is simulated with the proposed methodology and the effect is analyzed.

1.3 Thesis Organization

Rest of this report is organized as follows:

Chapter 2 gives the details of the semiconductor structures which are used prior to design and development of FinFETs and issues in those devices that lead to need research and development of new devices for continuing scaling trends called nonconventional structures. Then it introduces some of the nonconventional structures. It also gives brief details of roadmap proposed for growth of semiconductor industry.

Chapter 3 begins with description of the FinFET device structure, followed by some details of the device structure used in this work. Then it presents some brief of FinFET fabrication methods. It describes the simulation methodology used in this work. It uses Sentaurus TCAD from Synopsys. This further explains the tool flow in Syntaurus and different physical models used in simulations and details of methods used for parameter extraction.

Chapter 4 begins with the types of FinFET structures i.e. underlap and overlap and justification of the use of underlapped structure in this work. Multiple fin FinFET structures and their

parameters are described. Then impact of parasitic resistance and capacitance in a FinFET standard cell is analyzed. This work analyses FinFET based Inverter, NAND, NOR and SR latch circuits.

Chapter 5 efforts for proposing a novel scaling methodology for underlap FinFET devices by variation of some of the device design parameters keeping the optimum circuit performance and ease of device fabrication issues. It also leads to propose a three transistor analogy for underlap FinFETs which is able to describe the behavior of device properly. Finally the performance parameters I_{on} and input capacitance of an inverter C_{inv} are modeled with design parameters to achieve the maximum performance.

In chapter 6, conclusions are drawn on the basis of this work.

CHAPTER 2

CURRENT LITERATURE OF MULTIPLE GATE STRUCTURES

2.1 History of Devices – Necessity for CMOS Scaling

Semiconductor industry has experienced tremendous growth over the last 3 decades. Integrated Circuit (IC) design and computing technologies passed some great miles in progress journey from Small-Scale Integration (SSI), at less than 30 devices per chip, to Medium-Scale Integration (MSI), with 30 to 10^3 devices per chip, to Large-Scale Integration (LSI) with 10^3 to 10^5 devices per chip, to VLSI with 10^5 to 10^7 devices per chip, and now it's going to achieve Ultra-Large Scale Integration (ULSI) with 10^7 to 10^9 devices per chip. All this progress can be possible because of continued scaling device dimensions. Figure 2.1 shows the numbers of transistors in million, that can be purchased in $1[7]. Development of silicon integrated circuits in the 1950's [8-9] has contributed the most significant role in the growth shown in figure 2.1. With CMOS transistor technologies [10], high-density, low-power computing became available.

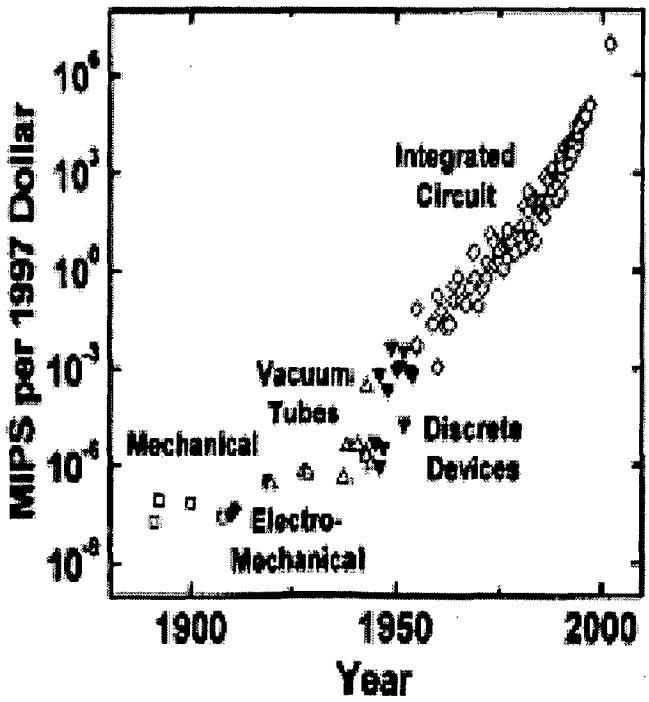

Figure 2.1: The millions of instructions per second that can be purchased with $1, showing growth path of semiconductor industry

With scaling transistor dimensions, peak operating oxide electric field, channel mobility, and subthreshold swing all should remain relatively constant, so Constant Field Scaling (CFS) scheme has been used as guidance to predict future device designs [11]. In constant field scaling supply voltage and device dimension are scaled equally so as to maintain the electric field constant to allow speed improvements for circuits without sacrificing reliability.

Gordon Moore predicted in the year 1975 that the number of transistors on a chip would be approximately doubled in every 18 months, [12] and this trend is still valid [13]. The industry has followed this Moore's law and achieved a continuous increase in transistor speed and density and a continuous decrease in power dissipation per transistor and cost per transistor.

For the circuits, the technology scaling enhances the performance and simultaneously reduces the layout area requirement resulting in enormous reduction in manufacturing costs.

2.2 Scaling Issues in Bulk MOSFET Scaling

Conventional planar MOSFET device has been used to follow scaling trend in order to achieve the higher and higher speed and density and allowed semiconductor industry to follow Moore's law, till recently [14]. Figure 2.2 shows the leakage currents in planar bulk MOSFET.

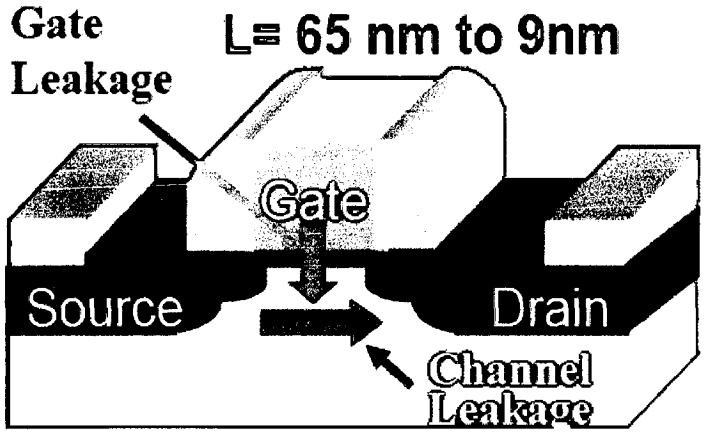

Figure 2.2: Schematic cross-section of planar bulk MOSFET

However, as the planar devices scaled at gate lengths around 50nm and below, scaling of these devices becomes increasingly difficult and requires innovations to overcome the problems due to fundamental physics that constrains the conventional MOSFET. The major limiting physical, technological and electrical phenomena are [15-23] -

- V_t roll-off
- Drain Induced Barrier Lowering (DIBL)
- Increasing leakage currents such as subthreshold S/D leakage
- Gate Induced Drain Leakages (GIDL)
- Gate direct tunneling and hot carrier effect.
- Random Dopant fluctuation
- Controlling junction and depletion depths.
- Quantum-mechanical tunneling of carriers from source to drain, and from drain to the body of the MOSFET.
- Control of the density and location of dopant atoms in the MOSFET channel and source/drain region to provide a high on-off current ratio and halo implants.
- Interconnect Resistance and Capacitance.
- Minimum Supply voltage.
- Lithography at nanoscale regime and its 3D integration.

Reducing the power supply V_{dd} helps to reduce power requirement and hot carrier effects, but worsens performance. Performance can be improved back by lowering V_t but at the cost of worsening S/D leakage. To reduce DIBL and increase adequate channel control by the gate, the oxide thickness can be reduced, but that increases gate leakage [6]. Solving one problem leads to another. Efforts are on to find a suitable high-k gate dielectric so that a thicker physical oxide can be used to help reduce gate leakage and yet have adequate channel control, but this search has not been successful to the point of being usable [6]. There are problems with band alignment (with respect to Si) and/or thermal instability problems and/or interface states problems (with Si). Polysilicon gate electrode suffers from thermal instability problem because insufficient activation leads to poly depletion effects. For reduction of SCE high channel doping is used. At small dimensions it leads to random dopant fluctuation as well as increased impurity scattering and therefore reduced mobility. [6]

In technology roadmap [13], at the end of near term of ITRS2003, nearly all of the thirty or so transistor characteristics expected between 2005 and 2008 required for high performance IC devices to meet the expectations of Moore's law are listed as "no known solutions" (Table 2.1). This is a clear indication that IC transistor technology requires fundamental changes in the next half decade.

Year of production	2003	2004	2005	2006	2007	2008	2009	Driver
Technology Node		hp90			hp65			
DRAM 1/2 pitch (nm)	100	90	80	70	65	57	50	DRAM
MPU/ASIC 1/2 pitch (nm)	107	90	80	70	65	57	50	MPU
MPU Printed Gate Length (nm)	65	53	45	40	35	32	28	MPU
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20	MPU
Equiv. physical oxide thickness for MPU/ASIC T_{ox} (nm)	1.3	1.2	1.1	1.0	0.9	0.8	0.8	MPU
Gate dielectric leakage at 100C (nA/um) High Performance	100	170	170	170	230	230	230	MPU
Physical gate length low operating power (LOP) (nm)	65	53	45	37	32	28	25	Low Power
Physical gate length low standby power (LSTP) (nm)	75	65	53	45	37	32	28	LSTP
Equiv. physical oxide thickness for low operating power T_{ox} (nm)	1.6	1.5	1.4	1.3	1.2	1.1	1.0	LOP
Gate dielectric leakage (nA/um) LOP	0.33	1.0	1.0	1.0	1.67	1.67	1.67	LOP
Equiv. physical oxide thickness for low standby power T_{ox} (nm)	2.2	2.1	2.1	1.9	1.8	1.6	1.4	LSTP
Gate dielectric leakage (nA/um) LSTP	3	3	5	7	8	10	13	LSTP
Thickness control EOT (% 3σ)	<±4	<±4	<±4	<±4	<±4	<±4	<±4	MPU/ASIC
Gate etch bias (nm) [D]	20	16	14	12	10	10	8	MPU/ASIC
I_{gate} 3σ variation (nm) [E]	4.46	3.75	3.15	2.81	2.5	2.2	2	MPU/ASIC
Total max allowable lithography 3σ (nm)	3.99	3.35	2.82	2.51	2.26	1.97	1.79	MPU/ASIC
Total max allowable etch 3σ (nm)including photoresist trim and gate etch [F]	1.99	1.68	1.40	1.26	1.02	0.98	0.89	MPU/ASIC
Resist trim max allowable 3σ (nm)	1.16	0.97	0.82	0.78	0.65	0.57	0.52	MPU/ASIC
Gate etch max allowable 3σ (nm)	1.82	1.37	1.15	1.02	0.91	0.80	0.73	MPU/ASIC
CD bias bet. dense and isolated lines	<±15	<±15	<±15	<±15	<±15	<±15	<±15	MPU/ASIC

Table 2.1: ITRS Roadmap 2003 showing the physical limits of scaling

Due to all above problems it was the best promising and practical solution felt for further scaling, to adopt some new alternative MOSFET structures, which are discussed now.

2.3 Non-Conventional CMOS structures

Following device structures have shown considerable potential and attracted the researches as alternatives of planar MOSFETs and also have been identified by *International Technology Roadmap for Semiconductors* [13] as the emerging research and/or commercial devices for continuing scaling trends at very small dimensions with improved performance.

2.3.1. Planar Devices: Silicon-On-Insulator (SOI) and Depleted Substrate Transistors (DST)

As fundamental limit of the planar CMOS structure is approaching rapidly, to allow continued device scaling, some new structures and materials has to be searched. This section discusses the various improvements in planar structures for continuing scaling.

One of the major problems with planar MOSFET scaling is extensive subthreshold leakages and increased junction capacitance. Both of these problems can be addressed by using silicon on insulator (SOI) method for planar devices [24]. It minimizes substrate leakages, reduce junction capacitance substantially, and power dissipation simultaneously.

Ultra-thin body (UTB) SOI devices [25] have additional advantage of improved electrostatic integrity. UTB-SOI devices are built on a very thin silicon body typically less than 20nm (< 20nm) with buried oxide beneath. This is also known as fully depleted condition in which channel is depleted of mobile carries under all operating bias conditions.

One of the solutions is to fabricate the device on a SOI substrate [24]. It is well known that SOI devices provide advantages of substantially reduced junction capacitance that facilitates high speed operation. At the same time, power dissipation is minimized. Ultra-thin body (UTB) SOI devices [25] have the added benefit of improved electrostatic integrity. The transistor is built on a very thin silicon body typically <20nm with buried oxide beneath. This is known as the fully depleted condition in which the thin silicon channel is depleted of mobile carriers under all operating bias conditions, thus scaling to a shorter length as compared to bulk planar devices is possible. It leads to the subthreshold slope to the theoretical value of 60mV/dec [26]. Typically in bulk transistors with scaling, channel doping is increased to reduce subthreshold leakages and thus subthreshold slope degrades because of increased depletion capacitance. The expression for sunthreshold slope (SS) is as follows:

$$SS = (kT/q)\ 1n_{10}.(1+C_D/C_{ox})$$

Where T is the temperature

q is the electronic charge

C_D is the capacitance of the depletion region

C_{ox} is the gate-oxide capacitance

In fully depleted structures depletion capacitance is greatly reduced, so subthreshold slope is improved.

However fully depleted transistors present a manufacturing challenge. The transistor is placed on an ultrathin layer of silicon having thickness approximately one third of the gate length. It is very difficult to achieve the precise thickness due to process variations like uneven oxidation rate across the wafer [26]. So the threshold voltage may vary widely if silicon layer thickness is not precisely controlled.

2.3.2 Tri-Gate MOSFET

Triple-gate MOSFETs allow more flexibility and tolerance of silicon with acceptable control of short channel effects. Triple gate structure (as the name suggests) has three gates, one horizontal and two vertical side gates over the box like channel as a connected gate. The silicon channel is covered from three sides by gate insulator followed by gate. Inversion takes place on two vertical faces and one top surface of box like channel. A TEM cross-section of a tri-gate FinFET is shown in Figure 2.3. The fin width and height are comparable to the gate length and this "relaxes" the body dimensions in terms of the lithography challenges.

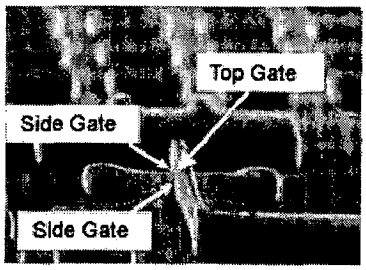

Figure 2.3: Cross-section of a tri-gate FinFET [27]

Tri-gates posses a major fabrication problem, as here thickness of all three gate insulators are same. But gate oxide (the most common gate insulator) is thermally grown. At different planes

of silicon surface rate of thermal oxidation is different. So it is very hard to get all three oxide of same thickness.

Apart from the tri-gate proposed by INTEL, there are many different gate configurations for SOI devices, namely Pi-Gate FET [29], Omega FET [30] and Surround-Gate FET [31] for number of gates greater or equal to 3. But these all has some manufacturing problem, so these are not commonly pursued by researchers.

2.3.3 Gate-All-Around MOSFET (GAA)

Gate-All-Around MOSFETs (GAA) or Silicon Nanowire attract significant interest as potential replacements or complements for traditional CMOS transistors around, or beyond the end of the current edition of the International Technology Roadmap for Semiconductors (ITRSs). In GAA, gate covers the wire like channel from all directions. So in GAA, the gate control over the lightly or undopped channel is very much improved. The thin channel is completely inverted. This improves immunity for short channel effect and transconductance performance, since volume inversion presents lesser scattering than surface inversion [32]. From simulation results it has found that the the drive current and transconductance of a gate-allaround is approximately four times that of the single gate device. Also it is more effective in suppressing short channel effects than other multiple gate structures [33].

However fabricating gate-all-around MOSFETs poses a technological challenge as it is not compatible with standard planar CMOS processing. Though it has the best scalability, it involves the most process complexity among all the multiple gate structures. The fabrication cost will be higher [34].

2.3.4 FinFET

The double-gate MOSFET is considered the most attractive device to succeed the planar MOSFET [35]. With two gates controlling the channel, short channel effects can be greatly suppressed. Out of the many double gate structures, FinFET is considered the most promising. It consists of a channel formed in a vertical Si fin controlled by a self-aligned double-gate. The top gate dielectric thickness is made larger as compared to the side vertical gate dielectric layers so that effectively only two vertical channels induced when a gate voltage is applied. Fact from fabrication point of view is that Si has different oxide growth rates in different planes, so it is

very difficult to match thickness of top and side gate dielectric (oxide) thickness. The fin is made thin enough when viewed from above such that the two gates control the entire fully-depleted channel film. The features include:

1. An ultra-thin silicon fin for suppression of short-channel effects

2. Two gates which are self-aligned to each other and to the source/drain regions

3. Raised source/drain to reduce parasitic resistance

4. Gate-last process compatible with low temperature, high-k gate dielectrics.

N-channel FinFETs showed good short channel performance down to 17 nm gate lengths [3] whereby boron doped SiGe is used as a gate material. Promising results were obtained for PMOS structure [4].

But in FinFETs, the width of the fin is smaller than the gate length. In FinFET fabrication, the width of the fin becomes the critical dimension. Lithography would have to be extended to finer line-widths in order to pattern the fin and that accelerates the lithography roadmap.

Chapter 3

FinFET Basics and Simulation Methodology

Among the various types of multi - gate structures, FinFETs have been shown to be the most attractive alternative to the bulk MOSFETs as it's fabrication is compatible with the current CMOS fabrication technology.

3.1 FinFET Structure

In a FinFET device, the channel is in the form of a thin vertical silicon structure referred to as the fin (as it resembles the tail fin of a fish). It is called a quasi-planar device because of this vertical fin, even though the current conduction is parallel to the plane of the silicon wafer [3]. FinFETs come in two flavors: double gate and triple gate. In triple gate FinFETs, the gate wraps around the fin from the top as well as from the side walls and the gate insulator thickness on the three sides are similar. In the double gate FinFETs, either the top insulator layer is made much thicker than the vertical insulator layers or a top gate is avoided altogether. In this work, only double gate FinFETs has been considered. Figure 3.1 shows 3^D structure and cross sectional view of a FinFET device.

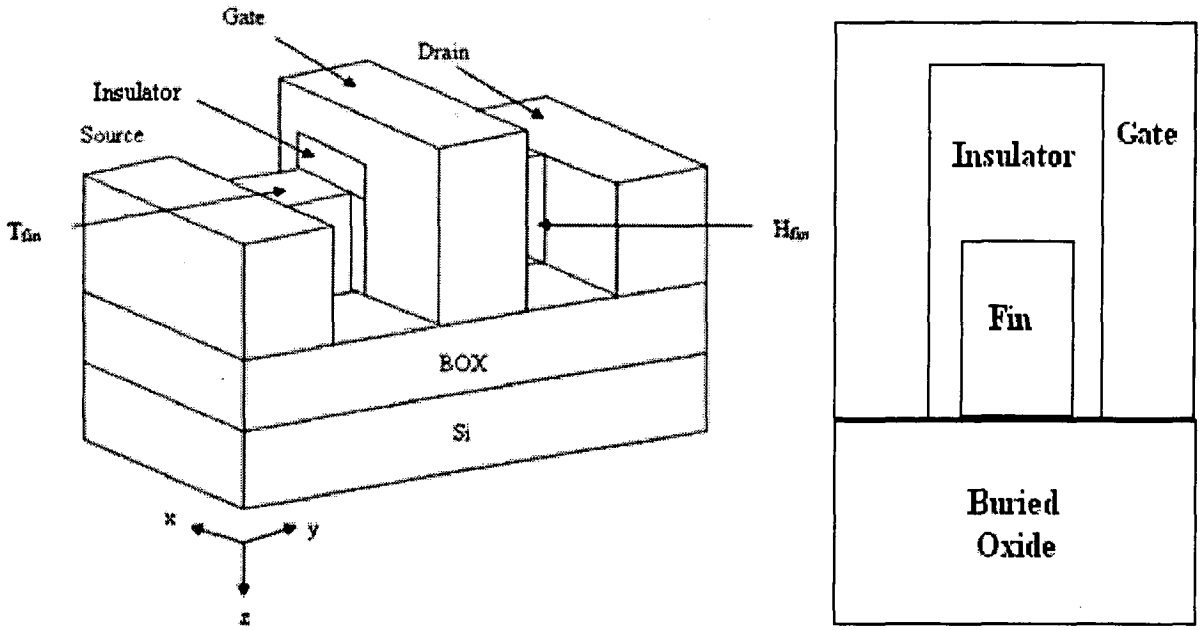

Figure 3.1: (a) 3D structure of a FinFET (b) Cross-sectional view of the gate region

The three dimensional structure and the 2-D cut-plane (y–z plane) view of the gate region of a typical double gate FinFET have been shown in figure 3.1 The fin height and fin thickness have been denoted by H_{fin} and T_{fin} respectively. The oxide thickness between the side gates and the fin is t_{ox}. Fin engineering (balancing fin height, fin thickness, oxide thickness, and channel length) is crucial in minimizing the leakage currents I_{off}, and maximizing the on current Ion [34].

For a double gate FinFET, the effective channel width is dependent on the fin height, given as

$W_{fin} = 2H_{fin}$. For FinFET, the top gate oxide layer is made sufficient thick so that its effect is negligible, as gate oxide is thermally grown for FinFETs and due to different oxide growth rates in different plans, it is difficult to make all three oxide layers equithick. Hence the gate controls the channel from two sides each having width H_{fin} (Note: For a triple gate FinFET, the expression becomes $W_{fin} = 2H_{fin} + T_{fin}$ since now we have additional gate control from the top).

3.2 Doping Densities

The fin is generally lightly doped (or even undoped). Source/Drain regions are heavily doped, while the Source/Drain extension regions have been subjected to different doping levels by different researchers – from undoped to constantly doped to Gaussian doped. Figures 3.2 & 3.3 show the structure and Gaussian doping profile in extension regions N-channel underlap FinFET respectively.

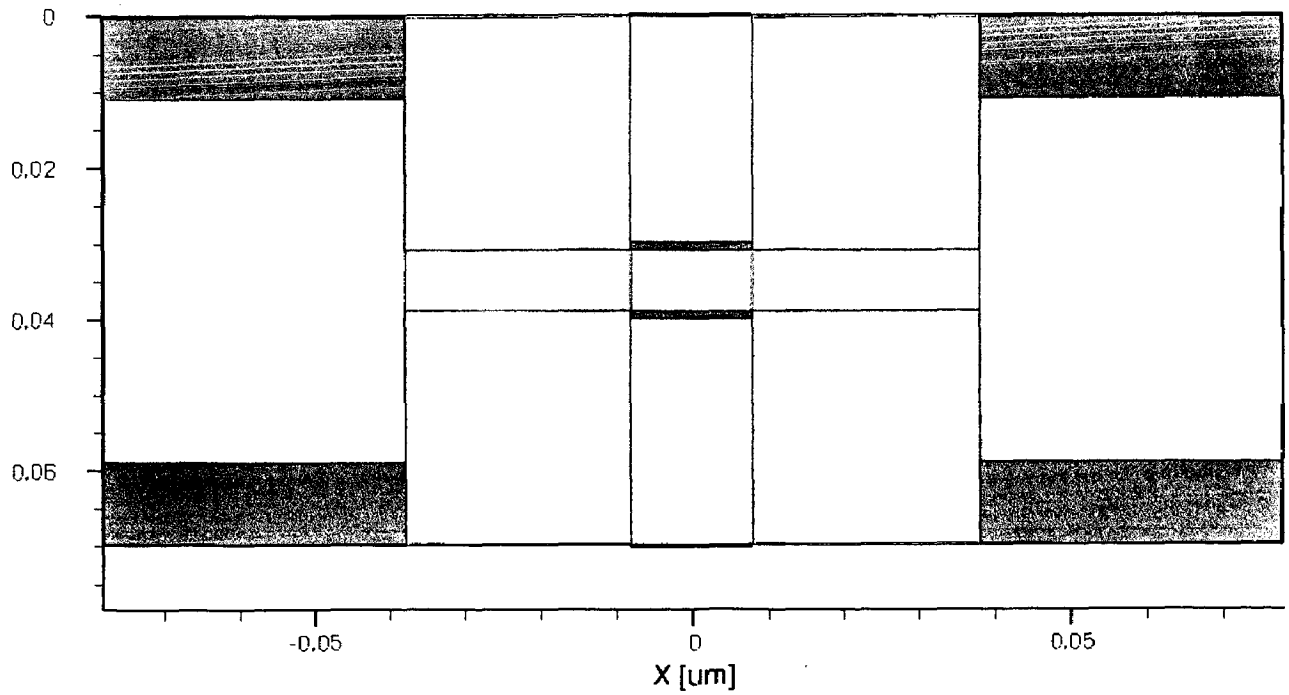

Figure 3.2: N-channel underlap FinFET structure with Gaussian doping profile in extension regions

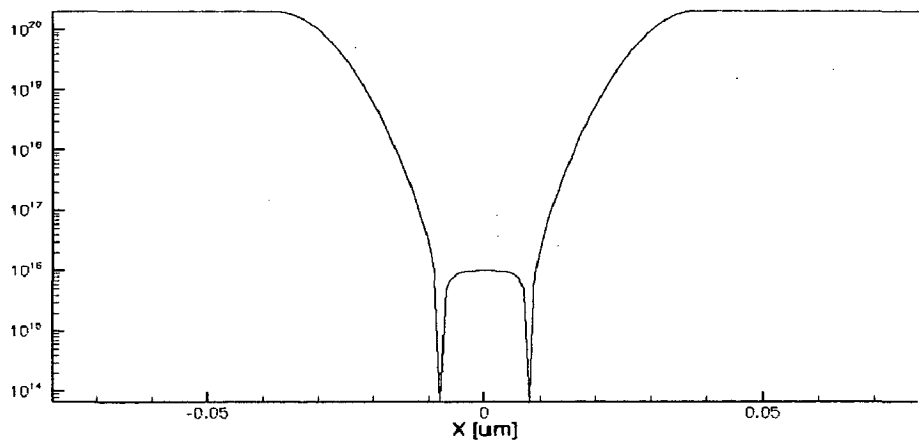

Figure 3.3: N-channel underlap FinFET structure doping profile

3.3 FinFET Fabrication Methods

FinFETs have been fabricated by mainly two different techniques:

Gate-First Approach: In this process, the source and drain regions are created after the formation (patterning) of the gate stack [36].

Gate-Last Approach: Here, the source and drain regions are formed before the formation of the gate stack [37, 3].

The fabrication of the FinFET begins with the patterning and etching of a thin fin on an SOI substrate using a hard mask which is retained throughout the fabrication process. The fin thickness is smaller than the gate length, and hence either electron-beam lithography or optical lithography with extensive linewidth trimming is used to pattern the thin fin. Figure 3.4 shows fabrication sequence of a Gate -First process and SEM & TEM images across the device width.

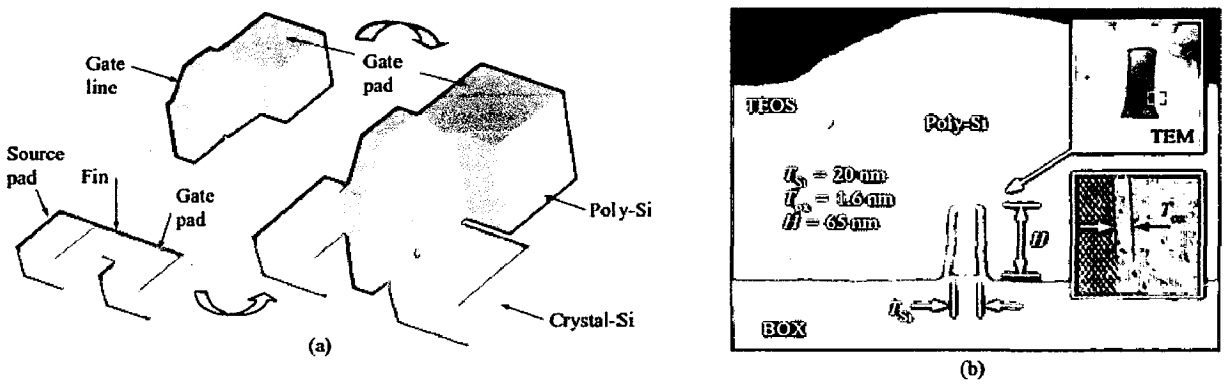

Figure 3.4: (a) Gate-First Process (b) Cross-sectional SEM and TEM images across the device width, llustrating the fin cross-sectional dimensions and the thin (1.6-nm) gate oxide grown on the sidewall of the fin. [6]

For the gate-first process, the fabrication steps after the fin formation are similar to the fabrication steps of the conventional bulk MOSFET. After the gate oxide is grown, the gate polysilicon is deposited, patterned and etched. A sidewall spacer is formed next to the gate.

Source/drain and extension implants can be performed before and/or after the gate spacer, using angled implants.

For the gate-last process, the source and drain regions are formed immediately after patterning. Doped polysilicon or polycrystalline SiGe is deposited on the fin, followed by lithographic patterning of the source/drain pads with a thin slot between the source and drain. This distance between the source and drain determines the gate length. The slot length is further reduced by a dielectric sidewall spacer. Then the gate oxide is grown, and the gate material is deposited and patterned [6]. Figure 3.5 shows fabrication sequence of a Gate-Last double gate FinFET process.

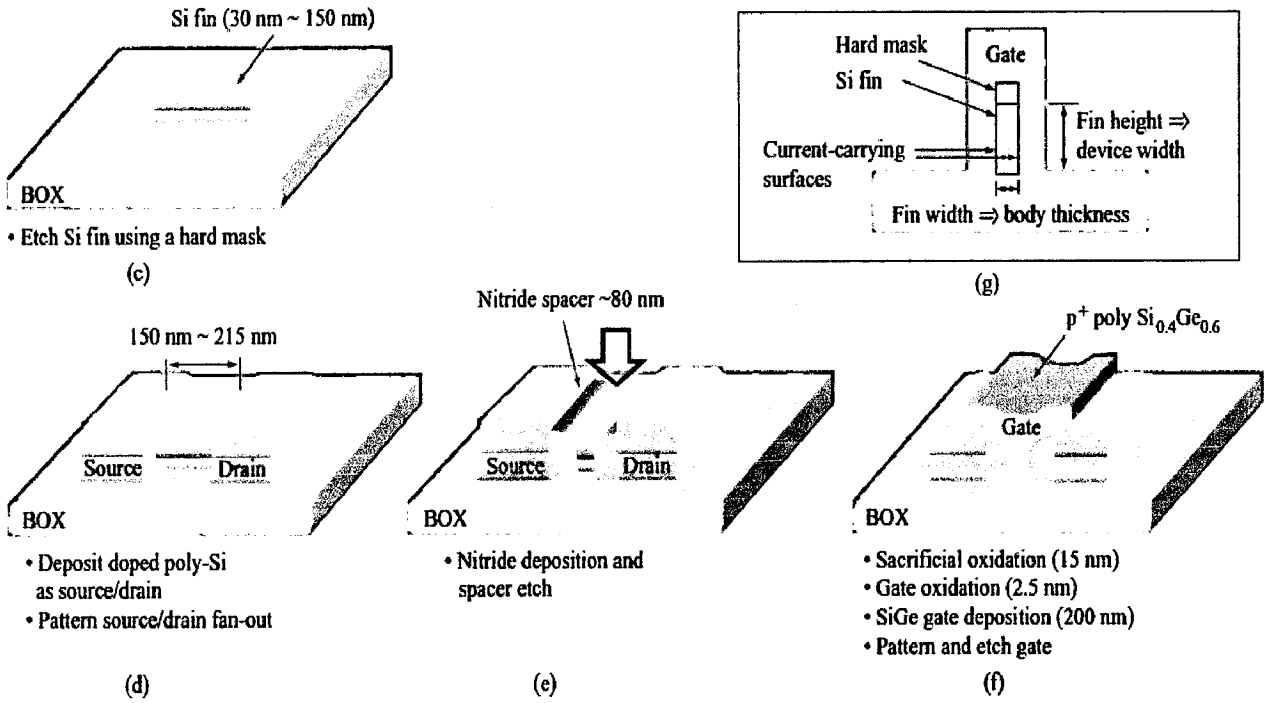

Figure 3.5: (a) –(d) Fabrication sequence of a Gate-Last double gate FinFET process. (e) Cross section of the silicon fin showing the current-carrying plane. Direction of current flow is into the plane of the diagram [7]

The gate-last process enables more flexibility in cases where metal-gate and high – κ dielectrics are used.

3. 4 Simulation Methodology

3.4.1 TCAD Device Simulations

Technology CAD (TCAD) refers to using computer simulations to develop and optimize semiconductor devices and processing technologies. TCAD simulation tools solve fundamental physical partial differential equations, such as transport equations for discretized geometries representing the silicon wafer or the layer system in a semiconductor device.

This deep physical approach gives TCAD simulation predictive accuracy. It is, therefore, possible to substitute TCAD computer simulations for costly and time-consuming test wafer runs when developing and characterizing a new semiconductor device or technology.

Device simulations can be thought of as virtual measurements of the electrical behavior of a semiconductor device. The device is represented as a meshed finite-element structure. Each node of the device has properties associated with it, such as material type and doping concentration. For each node, the carrier concentration, current densities, electric field, generation and recombination rates, etc. can be computed.

Electrodes are represented as areas on which boundary conditions, such as applied voltages, are imposed. The device simulator solves the Poisson equation and the carrier continuity equation (and other suitable equations). After solving these equations, the resulting electrical currents at the contacts can be extracted.

3.4.2 Sentaurus TCAD Package from Synopsys

The following tools from the Sentaurus package from Synopsys were used in this work:

Sentaurus Structure Editor: The device structures were created using this editor. The doping levels can be set and the meshing of the structure can also be done. It has a GUI as well as a command line interface.

The input files for this editor are written in the scheme programming language.

Sentaurus Device: Sentaurus Device can simulate the electrical, thermal, and optical characteristics of semiconductor devices. It contains a comprehensive set of physical models that can be applied to all relevant semiconductor devices and operating conditions. A real semiconductor device, such as a transistor, is represented in the simulator as a 'virtual' device

whose physical properties are discretized onto a non-uniform 'grid' (or 'mesh') of nodes. Continuous properties such as doping profiles are represented on a sparse mesh and, therefore, are only defined at a finite number of discrete points in space. The doping at any point between nodes (or any physical quantity calculated by Sentaurus Device) can be obtained by interpolation.

Each virtual device structure is described in the Synopsys TCAD tool suite by a *tdr* file containing the following information:

- The grid (or geometry) of the device contains a description of the various regions, that is, boundaries, material types and the locations of any electrical contacts. It also contains the locations of all the discrete nodes and their connectivity.
- The data fields contain the properties of the device, such as the doping profiles, in the form of data associated with the discrete nodes. By default, a device simulated in 2D is assumed to have a 'thickness' in the third dimension of 1 μm.

For maximum efficiency of a simulation, a mesh must be created with a minimum number of vertices to achieve the required level of accuracy. For any given device structure, the optimal mesh varies depending on the type of simulation.

Tool Flow: In a typical device simulation tool flow, the Sentaurus Structure Editor generates a *tdr* file, which is then used in the Sentaurus Device along with other input files viz. command file (*.cmd*) and a parameter file to simulate the electrical characteristics of the device. The parameter file(*.par*) is used for changing the default values. The *tdr* file can be generated using the Sentaurus Structure Editor alone or it can also be created in an alternate manner: the generation of a device structure by process simulation (using Sentaurus Process) followed by re-meshing using Sentaurus Structure Editor. In this scheme, control of mesh refinement is handled automatically through the command file.

The log files contain step-by-step information of the commands executed.

Tecplot: This tool is used for visualization purposes. It can plot solutions and derives variables like potential, carrier density, mobility, electrical field, etc.

Figure 3.6 shows the typical tool flow for device simulation using Sentaurus Device [38]

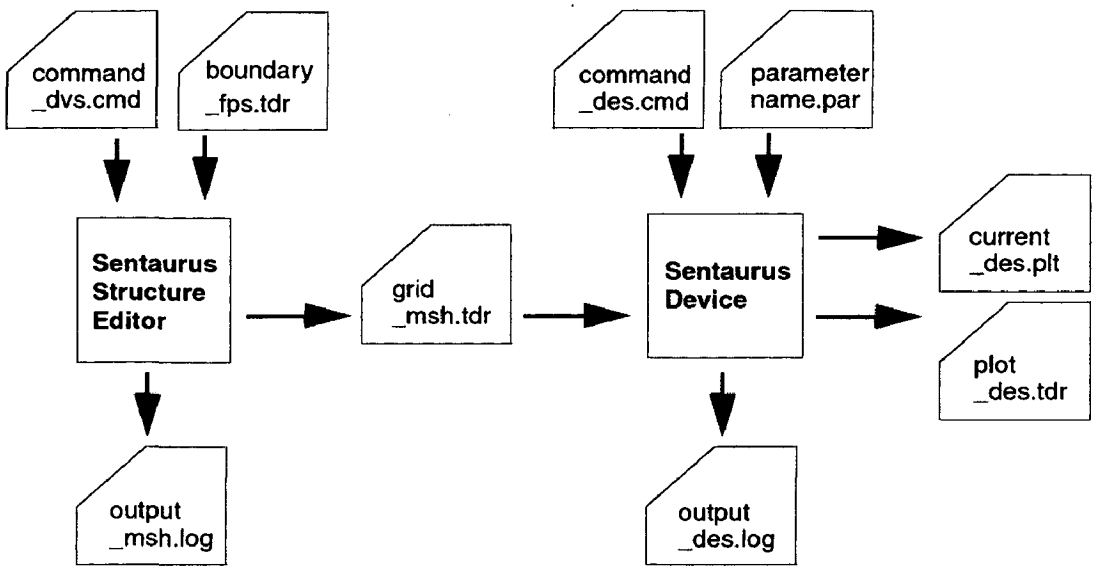

Figure 3.6: Typical tool flow for device simulation using Sentaurus Device [38]

3.4.3 A typical FinFET device used in the simulations

Two dimensional simulations were performed on the FinFET device, a typical one being shown in Figure 3.7. This diagram depicts a view from the top of the device. The various regions and geometrical parameters have been marked on the figure. T_{fin} is the fin thickness, L_g is the gate length, L_{spacer} and L_{ext} are the width of the spacer along the channel and total underlap length (including the spacer) respectively, while T_{gate} is the gate thickness.

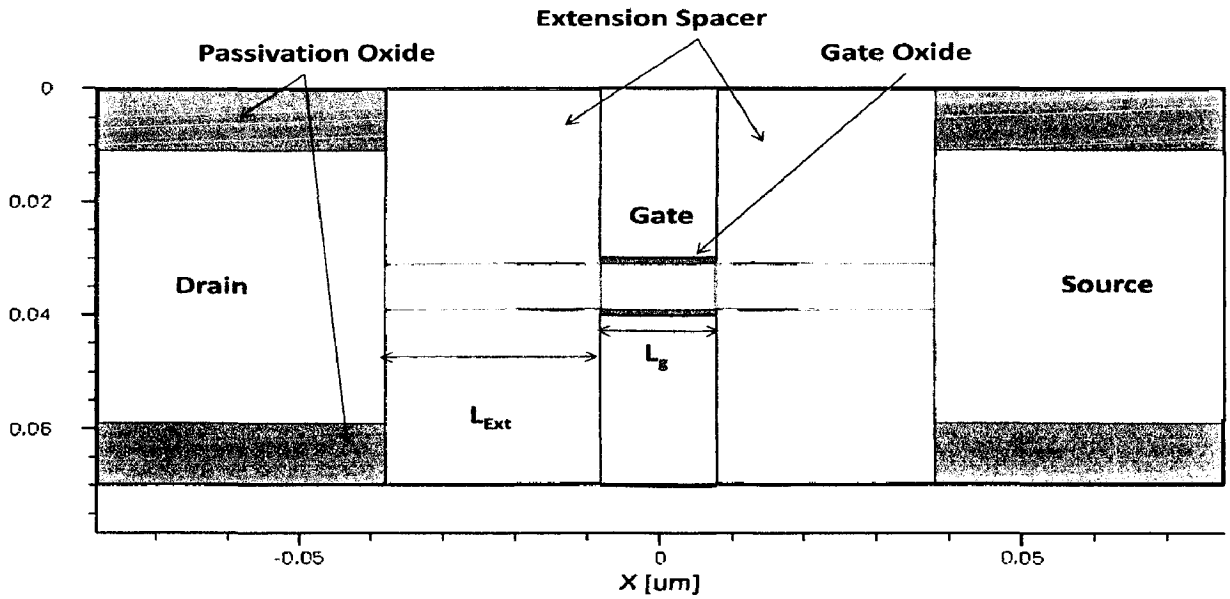

Figure 3.7: A typical 2D FinFET structure used in the Sentaurus simulations

3.5 Details of physical models used

This section describes the various physical models used in the simulations.

3.5.1 Band Gap Narrowing Model

The energy bandgap and the intrinsic carrier concentration are very important characteristics of a semiconductor material. At high impurity concentrations, the density of energy states no longer has a parabolic energy distribution and becomes dependent on the impurity concentration and it has been found experimentally that the bandgap is effectively reduced with increasing doping densities [39] as

$$E_{g,eff}(T) = E_g(T) - E_{bgn}$$

where E_{bgn} is the amount of band gap narrowing.

The Old Slotboom model [39] was used, which gives the amount of band –gap narrowing as:

$$E_{bgn} = E_{ref}\left[ln\left(\frac{N}{N_{ref}}\right) + \sqrt{\left(ln\left(\frac{N}{N_{ref}}\right)^2 + 0.5\right)}\right]$$

with E_{ref} = 9x10^{-3} and N_{ref} = 1x10^{17}.

As a result of band-gap narrowing, the effective intrinsic carrier concentration also changes as

$$n_i^2(N,T) = n_{i0}^2(T)exp\left(E_{g,eff}(N,T)/kT\right)$$

3.5.2 Mobility Models

The following mobility models were included in the simulation:

(a) The constant mobility model: It is the default model in Sentaurus Device. It accounts only for phonon scattering and, therefore, it is dependent only on the lattice temperature:

$$\mu_{const} = \mu_L\left(\frac{T}{300K}\right)^{-\zeta}$$

The following table lists the values of the coefficients μ_L and ζ:

Table 3.1: Constant Mobility Model: Default coefficients for Si

Parameter	Electron	Holes
μ_L	1417 cm^2/Vs	470.5 cm^2/Vs
ζ	2.5	2.2

(b) Doping Dependent Mobility Model: In doped semiconductors, the charged impurity ions cause scattering of the carriers, leading to degradation of the carrier mobility. In this work, the Masetti model [40] was used where

$$\mu_{dop} = \mu_{min1}\, exp\left(-\frac{P_c}{N}\right) + \frac{\mu_{const} - \mu_{min2}}{1 + (N_{tot}/C_r)^{\alpha}} - \frac{\mu_1}{1 + (C_s/N_{tot})^{\beta}}$$

The reference motilities μ_{min1}, μ_{min2} , μ_1 and μ_{const} the reference doping concentrations C_r, C_s, P_c and the exponents α and β are available in [38]

(c) High Field Saturation Mobility model

Since the FinFET dimensions are sub –100nm, the electric fields in the channel can be pretty high. In high electric fields, the carrier drift velocity gets saturated. The Extended Canali model [41] was used for accounting for this effect in the device simulations as

$$\mu(F) = \frac{(\alpha + 1)\mu_{low}}{\alpha + \left[\left(\frac{(\alpha + 1)\mu_{low} F_{hfs}}{v_{sat}}\right)^{\beta}\right]^{\frac{1}{\beta}}}$$

where μ_{low} denotes the low-field mobility, v_{sat} the saturation velocity and β is a temperature dependent exponent given by $\beta = \beta_0 \left(\frac{T}{300K}\right)^{\beta_{exp}}$ and $F_{hfs} = |\nabla\phi|$, is the electric field strength.

(d) Mobility degradation at interfaces

High perpendicular electric field in the channel region causes strong interaction of carriers at the silicon–insulator interface. Carriers are subjected to scattering by acoustic surface phonons and surface roughness. The Lombardi model [42] was used to include the degradation of carrier mobility at the interfaces.

The surface contribution due to acoustic phonon scattering has the form:

$$\mu_{ac} = \frac{B}{F_\perp} + \frac{C(N_{tot}/N_0)^\lambda}{F_\perp^{1/3}(T/300K)^k}$$

and the contribution attributed to surface roughness scattering is given by:

$$\mu_{sr} = \left(\frac{(F_\perp/F_{ref})^{A*}}{\delta} + \frac{F_\perp^3}{\eta} \right)^{-1}$$

The values for the various coefficients are available in [38]

The net mobility is given by the combination of the mobility models described above, according to the well known Mathiessen's rule: $\mu^{-1} = \mu_1^{-1} + \mu_2^{-1} + \mu_3^{-1}$.....

3.5.3 Recombination Model

(a) Shockley–Read–Hall (SRH)

Electron-hole recombination is an important mechanism by which carrier concentrations tend to approach their equilibrium values. Phonon emission can occur during this recombination process in the presence of a trap (or defect) within the forbidden gap of the semiconductor. The doping dependent model of Shockley–Read–Hall (SRH) recombination was used to consider recombinations through deep defect levels in the band gap. In Sentaurus Device, the following form is implemented [38]:

$$R_{net}^{SRH} = \frac{np - n_{i,eff}^2}{\tau_p(n + n_1) + \tau_n(p + p_1)}$$

where, n and p are the electron and hole concentrations at the site, and

$$n_1 = n_{i,eff}\, exp(E_{trap}/kT)$$

$$p_1 = p_{i,eff}\, exp(-E_{trap}/kT)$$

where is E_{trap} the difference between the defect level and intrinsic level. The variable is accessible in the parameter file (.par file). It's default value for silicon is 0. $n_{i,eff}$, is the effective intrinsic electron concentration. τ_p and τ_n are the minority carrier lifetimes and are dependent on the doping, electric field and temperature. The doping dependence of the SRH lifetime τ_{dop} is modeled in Sentaurus Device with the Scharfetter relation, written below [38].

$$\tau_{dop}(N_{A,0} + N_{D,0}) = \tau_{min} + \frac{\tau_{max} - \tau_{min}}{\left(1 + \frac{N_{A,0} + N_{D,0}}{N_{ref}}\right)^{\Upsilon}}$$

Table 3.2 lists the default parameters.

Table 3.2: Default parameters for the doping dependent SRH lifetimes [38]

Parameter	Electron	Holes	Unit
τ_{min}	0	0	s
τ_{max}	$1x10^{-5}$	$3x10^{-6}$	s
N_{ref}	$1x10^{16}$	$1x10^{16}$	cm^{-3}
Υ	1	1	1
E_{trap}	0	0	eV

Since the simulations performed included quantum transport models to account for the quantum mechanical effects, the expression for R_{net}^{SRH} needs to be modified as follows

$$R_{net}^{SRH} = \frac{np - \Upsilon_n \Upsilon_p n_{i,eff}^2}{\tau_p(n + \Upsilon_n n_1) + \tau_n(p + \Upsilon_p p_1)}$$

where

$$\Upsilon_n = \frac{n}{N_c} exp(-\eta_n), \quad \Upsilon_p = \frac{p}{N_c} exp(-\eta_p)$$

$$\eta_n = \frac{E_{F,n} - E_c}{kT}, \quad \eta_p = \frac{E_V - E_{F,p}}{kT}$$

(b) Auger recombination

In Auger recombination an electron from conduction band to valence band and the energy of transition is given to a third particle, it may be another electron or hole. Auger recombination is typically important at high carrier densities. Therefore, this injection dependence will only be seen in devices where extrinsic recombination effects are extremely low. The rate of band-to-band Auger recombination R_{net}^{A} is given by:

$$R_{net}^{A} = (C_n\, n + C_p\, p)\,(n\, p - n_{i,eff}^2)$$

with temperature-dependent Auger coefficients (Sentaurus manual device[43][44][45]

$$C_n(T) = \left(A_{A,n} + B_{A,n}\left(\frac{T}{T_0}\right) + C_{A,n}\left(\frac{T}{T_0}\right)^2\right)\left[1 + H_n\, exp\left(\frac{n}{N_{0,n}}\right)\right]$$

$$C_p(T) = \left(A_{A,p} + B_{A,p}\left(\frac{T}{T_0}\right) + C_{A,p}\left(\frac{T}{T_0}\right)^2\right)\left[1 + H_p\, exp\left(\frac{p}{N_{0,p}}\right)\right]$$

Where T_0 =300 K.

Default values of the parameters for silicon are listed in Table 3.3

Table 3.3: Default parameters for parameters for silicon [38]

Symbol	A_A ($cm^6 s^{-1}$)	B_A ($cm^6 s^{-1}$)	C_A ($cm^6 s^{-1}$)	H	N_0 (cm^{-3})
Parameter name	A	B	C	H	N0
Electrons	6.7×10^{-32}	2.45×10^{-31}	-2.2×10^{-32}	3.46667	1×10^{18}
Holes	7.2×10^{-32}	4.5×10^{-33}	2.63×10^{-32}	8.25688	1×10^{18}

3.5.4 Quantization models

For FinFETs (oxide thickness, fin width etc.) have reached quantum-mechanical length scales. Therefore, the wave nature of electrons and holes can no longer be neglected. The most basic quantization effects in MOSFETs are the shift of the threshold voltage and the reduction of the gate capacity.

To include quantization effects in a classical device simulation, Sentaurus Device introduces a potential-like quantity in the classical density formula:

$$n = N_C\, F_{1/2}\left(\frac{E_{F,n} - E_C - \Lambda_n}{k\, T_n}\right)$$

An analogous quantity Λ_p is introduced for holes.

We used van Dort model in simulation physics. It computes Λ_n as a function of $|\hat{n}\,.\,\vec{F}|$, the electric field normal to the semiconductor–insulator interface:

$$\Lambda_n = \frac{13}{9} \cdot k_{fit} \cdot G(\vec{r}) \cdot \left(\frac{\epsilon\,\epsilon_0}{4\,k\,T}\right)^{1/3} \cdot \left|\left|\hat{n} \cdot \vec{F}\right| - E_{crit}\right|^{2/3}$$

and likewise for Λ_p, k_{fit} and E_{crit} are fitting parameters.

The function $G(\vec{r})$ is defined by:

$$G(\vec{r}) = \frac{2 \cdot exp\left(-a^2(\vec{r})\right)}{1 + \exp\left(-2a^2(\vec{r})\right)}$$

where $a(\vec{r}) = l(\vec{r})/\lambda_{ref}$ and $l(\vec{r})$ is a distance from the point $\vec{r}$ to the interface. The parameter λ_{ref} determines the distance to the interface up to which the quantum correction is relevant.

3.5.5. Transport Model

The Density Gradient transport model was used for the device simulations. This model advanced by Ancona [48] and his coworkers is an approximate approach to the quantum mechanical correction of the macroscopic electron transport equation. In this approach, an extra term is introduced in the carrier flux by making the equation of state for the electron gas density gradient dependent.

DG equation for electrons: $\frac{\partial n}{\partial t} = \frac{\nabla . J_n}{q} = \nabla . (-n\,\mu_n \nabla \Psi_n + D_n \nabla n)$

Correction: $\Psi_n \rightarrow \Psi_n + \Psi_{qn}$, $\Psi_{qn} = 2b_n \left(\frac{\nabla^2 \sqrt{n}}{\sqrt{n}}\right)$; $b_n = \frac{\hbar^2}{4 r_n m_n q}$

Here r_n is a fitting parameter generally taken to be equal to 3.

Quantum-corrected current density: $J_n = -qn\mu_n \nabla \Psi_n + qD_n \nabla_n - qn\mu_n \nabla \left(2b_n \frac{\nabla^2 \sqrt{n}}{\sqrt{n}}\right)$

3.6 Parameter Extraction

The various device parameters were extracted from the simulated FinFET characteristics using the "Inspect" tool. Here is a description of the extraction methodologies and parameter definitions used.

3.6.1 Ion Extraction: The on-current is defined as I_{DS} (V_{DS}=V_{GS}=V_{DD}).

3.6.2 Ioff Extraction: The off current i.e. the subthreshold leakage current ($I_{DS,\,sat}$) is defined as I_{DS} (V_{DS} = V_{DD}, V_{GS}=0).

3.6.3 Threshold Voltage Extraction: The threshold voltage (V_t) is a fundamental parameter in MOSFET design and modeling. Many different definitions and extraction methodologies exist in literature and are in use [49]. In essence, it is interpreted as the gate voltage value at which the transition between weak and strong inversion takes place in the channel of the device. The theoretical definition of V_t for conventional MOS devices is based on the "strong-inversion" condition at which the surface potential is twice of the bulk Fermi potential ($\phi_S = 2\phi_F$). However, most practical FinFETs have undoped or lightly doped channels. In such cases, $\phi_F \approx 0$ and hence this definition of threshold voltage doesn't have any relevance.

In this work, the threshold voltages have been calculated from the simulated drain current versus gate voltage transfer characteristics by constant current method.

Constant-current (CC) method: In the CC method, the threshold voltage is evaluated as the value of the gate voltage, V_g, corresponding to a given arbitrary constant drain current, I_d with V_{ds} < 100 mV. The threshold voltage can be determined easily with only one voltage measurement. In this work, the CC threshold voltage of the FinFET has been taken as the value of V_G for which the drain current is given by $I_{D0} = (300nA \times W/L_g$, where W is the effective width of the FinFET, which is given by $W = 2Tfin$, at low drain bias of 0.05V for extracting the linear threshold voltage [50]. Since the drain current in the 2D simulations is available in units of A/μm, the constant current value is modified as $I_{D0} = (300\ nA \times W/L_g) \times W = 300\ nA/\ L_g$, the L_g value being in units of μm. For p-finFETs, the current was taken to be $0.4I_{D0}$.

3.6.4 Subthreshold Slope Extraction

First the drain current I_{crit}, corresponding to the gate voltage equal to V_t-g_m is found. If the current level at V_G=0 is less than $I_{crit}/10$, we proceed to find the subthreshold slope, else it implies that there is no well defined subthreshold region.

$$S = \frac{dV_{GS}}{d\ log I_D}$$

Chapter 4

Results & Impacts of Parasitics on FinFET Standard Cell

4.1 Overlap & Underlap Device Structures

Researchers have proposed FinFETs with both gate overlap and underlap drain/source extension regions [51, 52]. In overlap, gate region overlaps source and drain regions, Figure 4.1 shows gate overlap and underlap FinFET schematics.

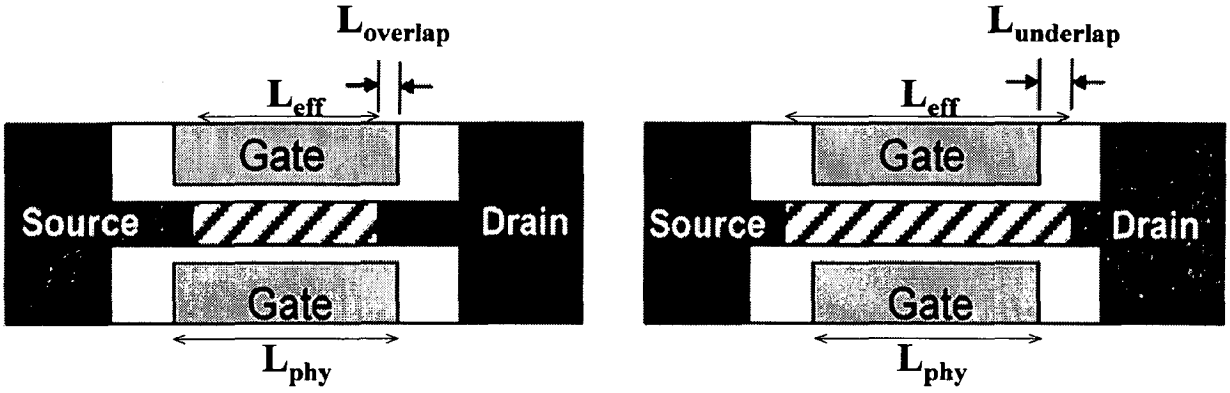

Figure 4.1: Cross sectional top view of a FinFET, (a) With gate to drain/source overlap. (b) With gate to drain/source underlap [53].

A cross-sectional schematic showing various terms of length is depicted in Figure 4.1. L_{eff} is defined as $L_{eff} = L_{phy} - 2L_{over}$ (in case of overlapped structure) and $L_{eff} = L_{phy} + 2L_{over}$ (in case of underlapped structure). A basic concept for determining L_{over} and $L_{underlap\ is}$ based on the short channel characteristics of the device. As the gate length decreases, short channel characteristics such as drain induced barrier lowering (DIBL), subthreshold swing (SS) and on/off current ratio (I_{on}/I_{off}) are degraded. As L_{phy} reduces, source and drain gets closer then gate field effect becomes weakened. As a result, DIBL and SS are increased, and I_{on}/I_{off} is decreased. In turn, the transistor acts as a resistor when metallurgical junctions of S/D are contacted [55].

FinFETs with gate overlap have a higher value of ON current I_{on} at the cost of a much higher OFF current I_{off}. The value of I_{on}/I_{off} reduces greatly with scaling of FinFET device dimensions. Therefore, there is need to design drain/source extension regions (SDE) carefully. Underlap FinFETs have been proposed to address this issue. The SDE regions in underlap FinFETs have a

DEPARTMENT OF ELECTRONICS AND COMPUTER ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NO.ECE/ 1375 /M-20 DATED: 20 JUL 2010

Dean, Academic Studies

Subject: **M. Tech/IDD Dissertation Examination**

Enclosed please find a copy of the panel of examiners regarding the dissertation examination of SAURABH KUMAR NEMA student of M. Tech/IDD (SDVT).

The above Viva-Voce for the above examination has been scheduled at 3.00 p.m.

on 30/7/10 in Seminar Room No. 1

B. Anand
Supervisor

Chairperson, DAC

S N Singh 20/7
Head of the Department

Accepted 19/7/10
Copy to:

1. Supervisor to please arrange to send copies of dissertation to the members of Viva-Voce Board.

2. All members of the board : 1. External Examiner Dr. Indra Gupta
2. HOD/DAC Nominee Dr. B.K. Kaushik
3. Internal Examiner: (i) Dr. A. Bakshi
(ii) Dr. A.K. Saxena

3. File.

Chairperson, DAC

S N Singh 20/7
Head of the Department

Head, E. & C.E. Deptt.

The notice did not reach the External examiner Dr. Gupta from E and CE office. The exam needs to be rescheduled to Mo 11 AM due to the above negligence.

Accepted 30/7

B. Anand
30/7/10

graded doping profile from source/drain pads to channel region. Due to this, the SDE doping values are very low near the channel regions. When the device is ON, carrier concentration is high in the SDE regions and vice-versa. This results in a higher value of I_{on}/I_{off}. Due to this reason, underlap FinFETs with an optimized graded doping profile has received considerable interest recently [55, 56]. Table 4.1 shows the values of device parameters used.

Table 4.1: Parameters of the device considered in this work

Gate oxide	SiO_2
Gate material	Metal
Gate work function	4.4 (for nFinFET), 4.9 (for pFinFET)
Gate length L_g	16 nm
Fin pitch	70 nm
Fin width W_{fin}	8 nm
Oxide thickness	1.1 nm
Extension length L_{ext}	30 nm
Spacer length L_{spacer}	30 nm
S/D pad length L_{SD}	40 nm
Channel doping N_{fin}	1e16 cm^{-3} (Boron)
Pad Doping N_{SD}	2e20 cm^{-3}

4.2 Current characteristics of Overlap & Underlap Devices

For increasing the current driving capability of the device, FinFET with multiple fin are simulated and their parameters are analyzed. This section first describes the multiple fin structures which are used and then current driving capability of FinFET with increasing number of fins for both overlapped and underlapped structures.

Figures 4.2-4.5 show single fin and multiple fins (three fins) overlapped N-channel FinFET and P-channel FinFET with overlapped length L_{over} = 1nm.

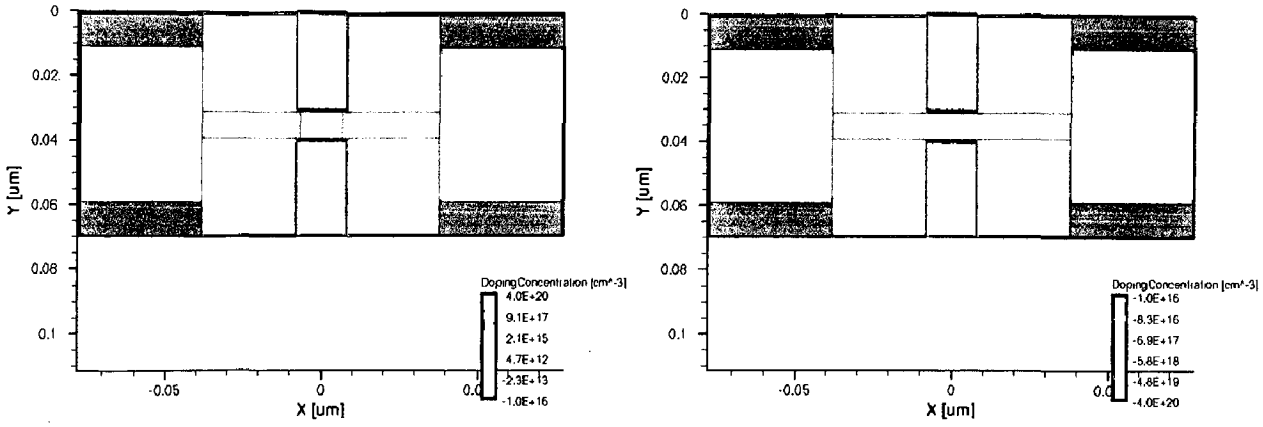

Figure 4.2: Overlap device structure of single fin N-channel FinFET and P-channel FinFET

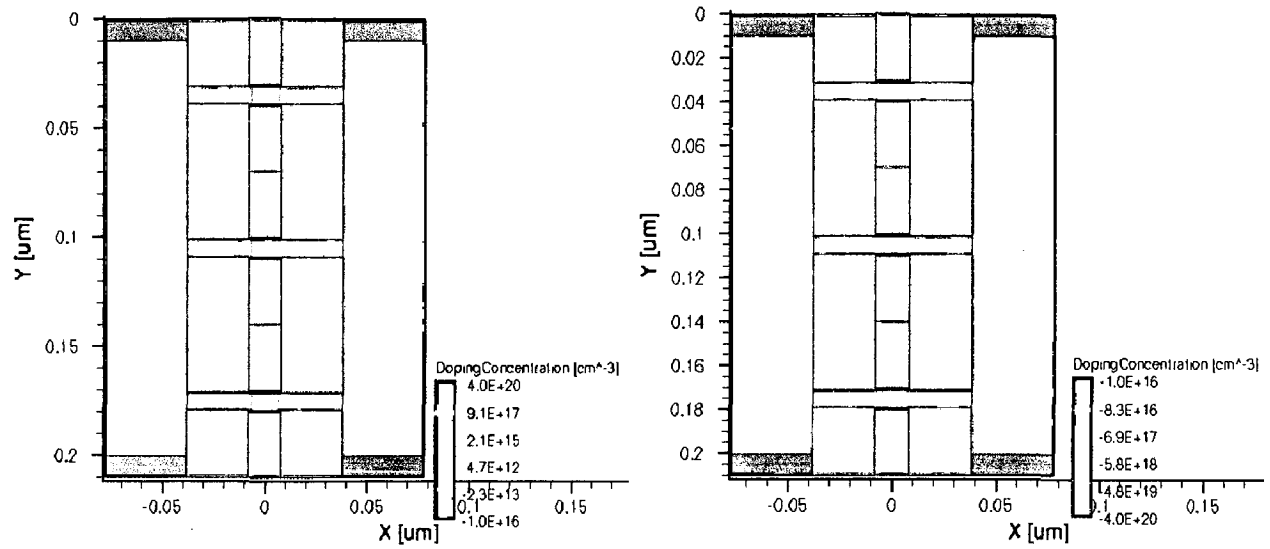

Figure 4.3: Overlap device structure of three fins N-channel FinFET and P-channel FinFET

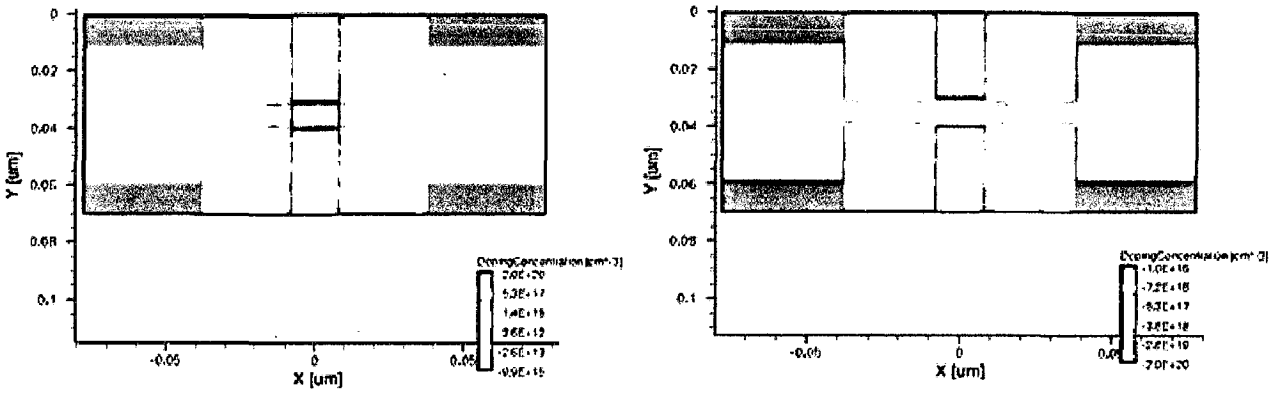

Figure 4.4: Underlap device structure of single fin N-channel FinFET and P-channel FinFET

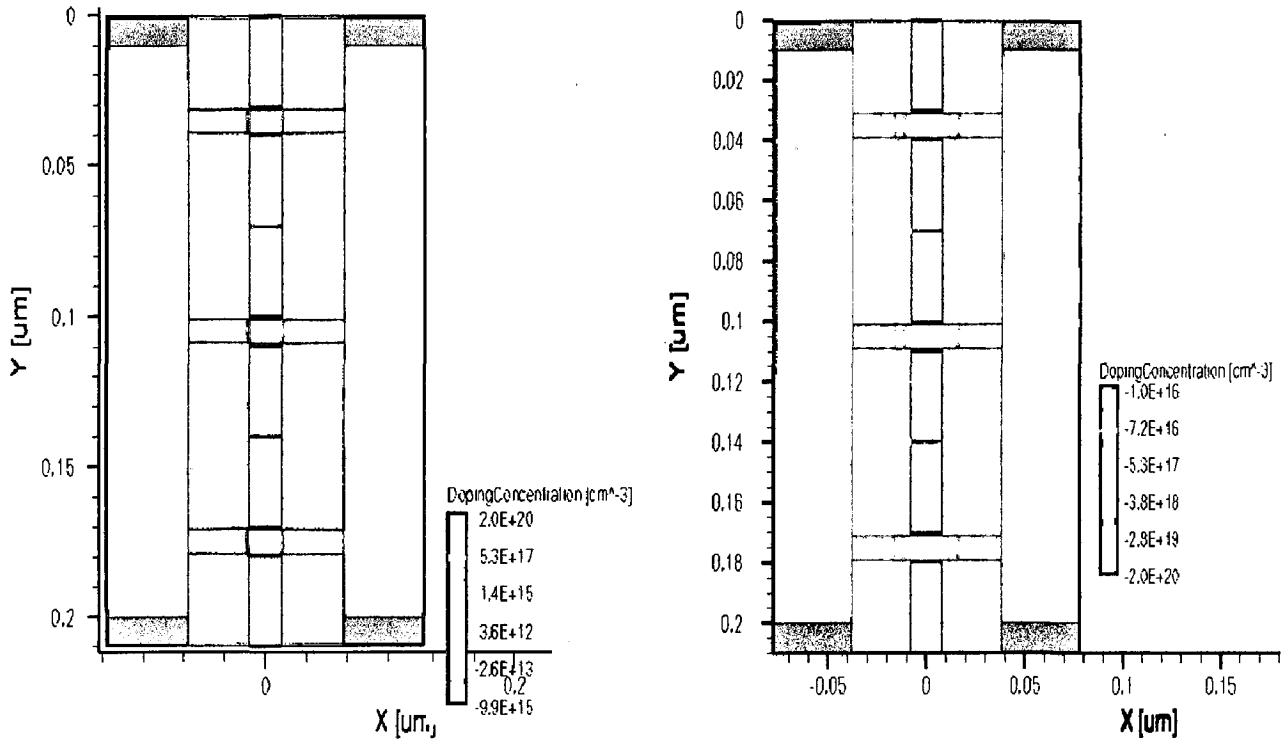

Figure 4.5: Device structure of multiple fins (three fins) N-channel FinFET and P-channel FinFET

Figure 4.6-4.11 shows ON and OFF current characteristics of overlap and underlap devices with multiple number of fins.

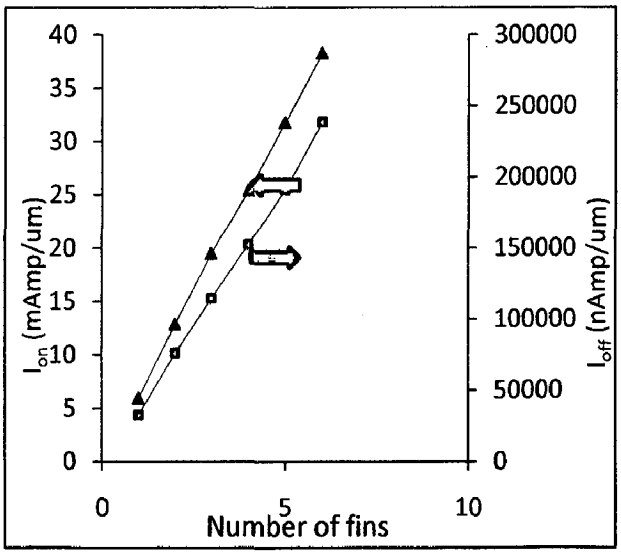

Figure 4.6: I_{on} and I_{off} of overlap n-channel FinFET vs. number of fins

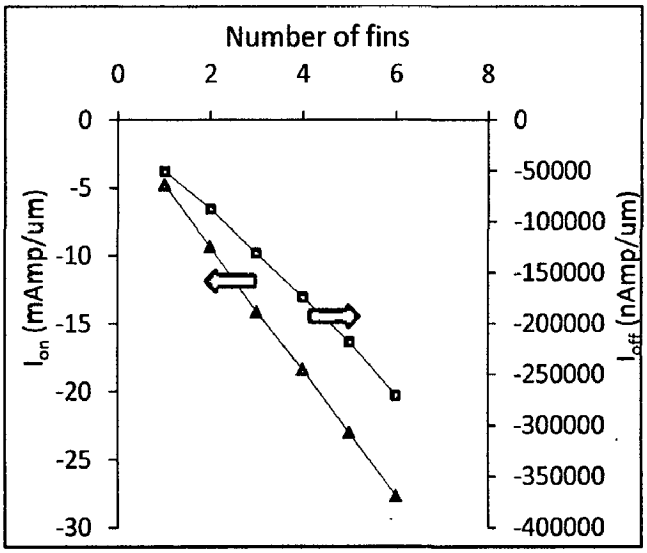

Figure 4.7: and I_{off} of underlap p-channel FinFET vs. number of fins

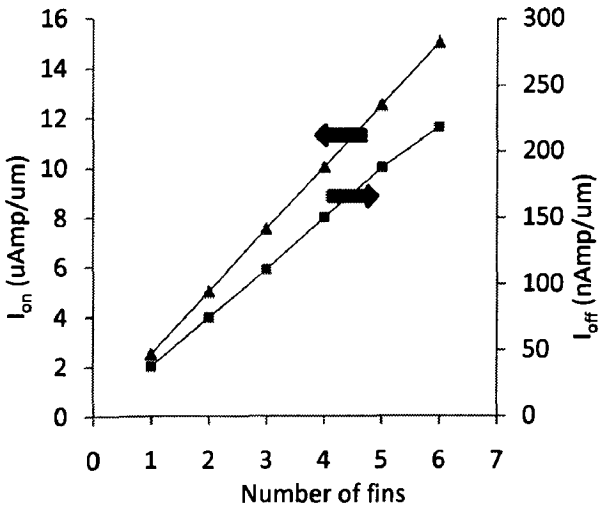

Figure 4.8: I_{on} and I_{off} of underlap n-channel FinFET vs. number of fins

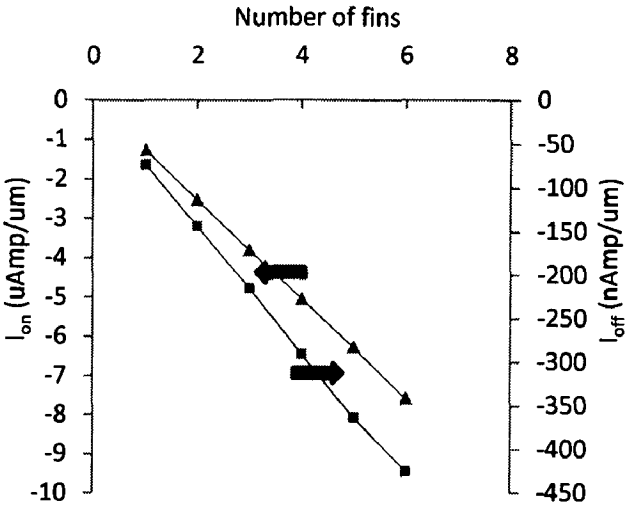

Figure 4.9: I_{on} and I_{off} of underlap p-channel FinFET vs. number of fins

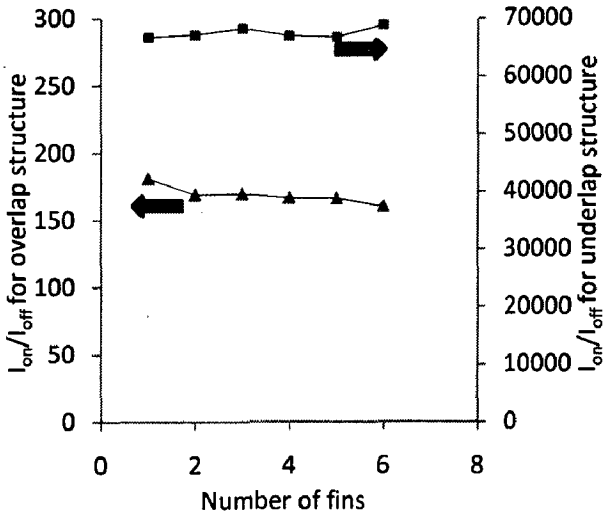

Figure 4.10: I_{on}/I_{off} for overlap & underlap n-channel FinFET vs. number of fins

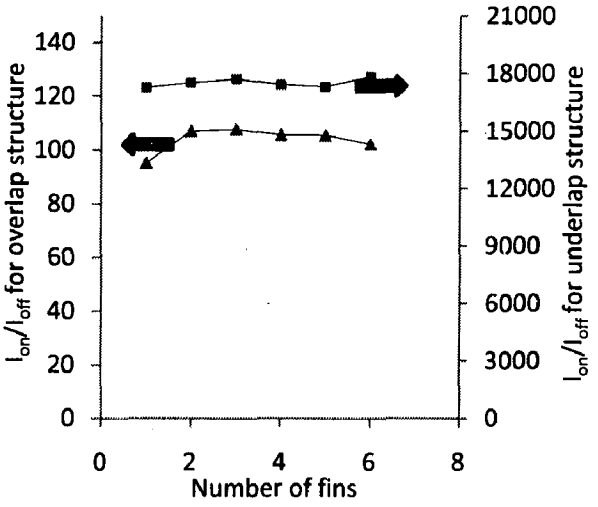

Figure 4.11: I_{on}/I_{off} for overlap & underlap p-channel FinFET vs. number of fins

Discussion

With overlapped structure, very high I_{on} can be achieved (Figure 4.6-4.7) but subthreshold leakages are also very high causing degradation in I_{on}/I_{off} (Figure 4.10). Whereas in case of underlapped structure, somewhat lesser value of I_{on} gained but subthreshold leakages i.e. I_{off} is very low compared to overlapped structure (Figure 4.8-4.9), so I_{on}/I_{off} is typically very large compared to overlapped structure (Figure 4.11).

4.3 Standard circuit by FinFET Device with different number of fins

Standard circuits as Inverter, 2-input NAND gate, 2-input NOR gate and SR latch are simulated without considering the effect of parasitic capacitance and resistance included by interconnects. For getting a realistic result, effect of parasitic capacitance and resistance because of interconnects, are included as lumped elements in mixed mode simulation of TCAD. Predictive technology model (PTM) which is evolution of previous Berkeley Predictive Technology Model (BPTM) is used for calculating parasitic capacitance and resistance.PTM provide the novel features for robust design exploration toward the 10nm regime [57].

For achieving NAND, NOR and SR latch circuits, series and parallel combination of n-channel FinFET and p-channel FinFET are simulated by Sentaurus-Device and these composite devices are used for making NAND, NOR and SR latch circuits by Sentaurus-mixed mode simulation.

Figures 4.12 and 4.13 respectively show parallel and series combination of two n-channel and p-channel FinFET devices with single fin structure.

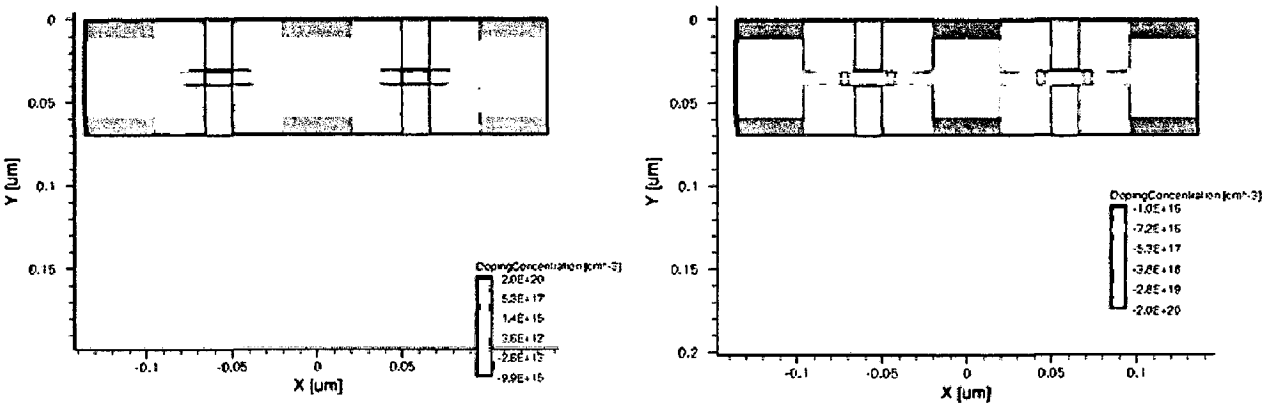

Figure 4.12: Parallel combinations of two n-channel and p-channel single fin FinFET devices

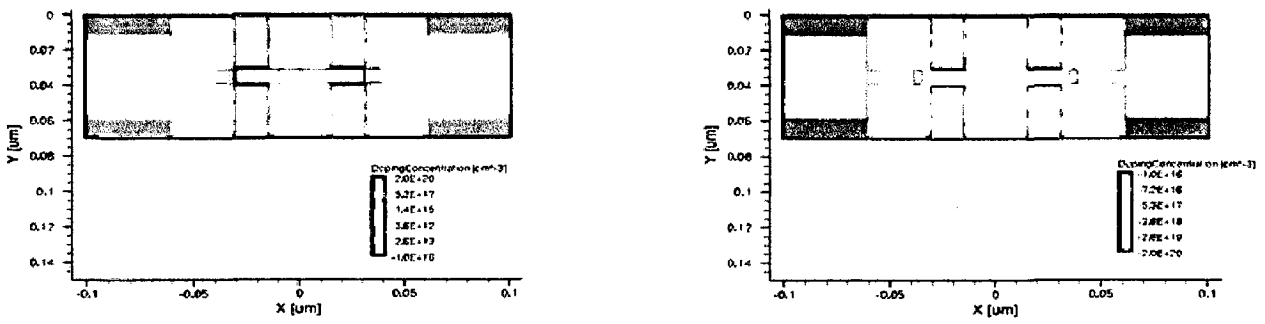

Figure 4.13: Series combinations of two n-channel and p-channel single fin FinFET devices

Figures 4.14-4.17 show current characteristics of series and parallel combinations of N-channel and P-channel FinFET structures used in mixed mode simulation of FinFET based standard cell.

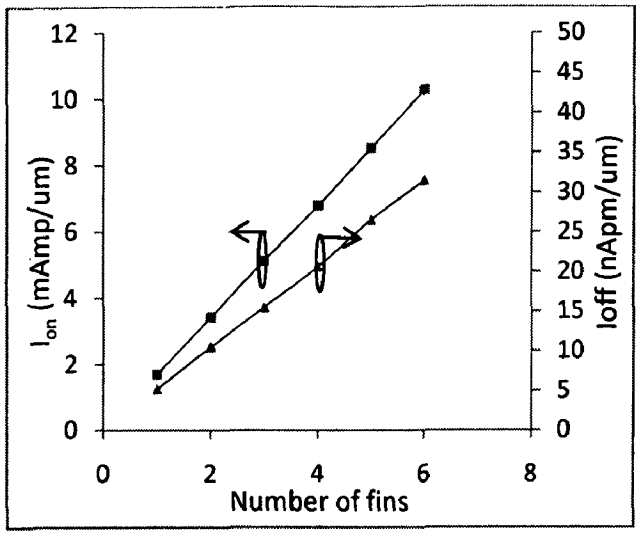

Figure 4.14: I_{on} and I_{off} of series combination of two n-channels FinFET with multiple fins

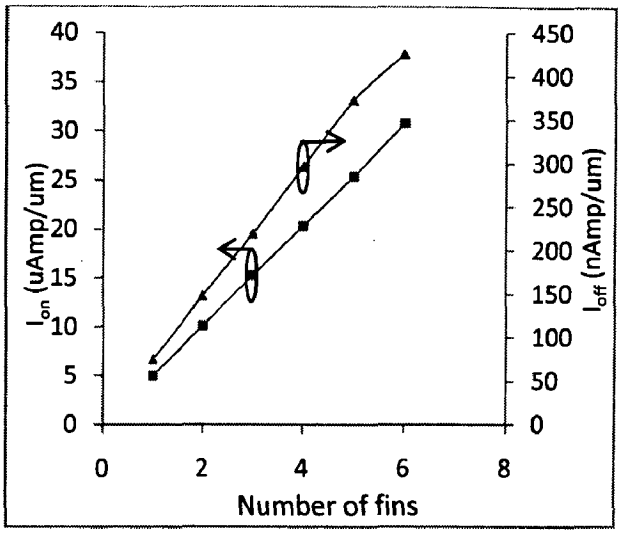

Figure 4.15: I_{on} and I_{off} of parallel combination of two n-channels FinFET with multiple fins

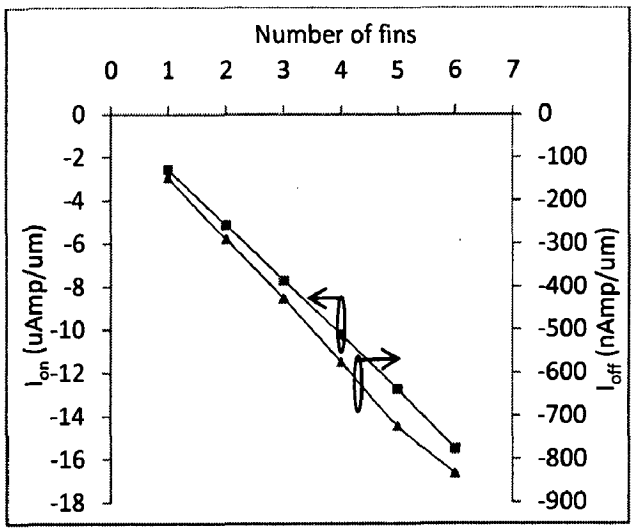

Figure 4.16: I_{on} and I_{off} of series combination of two p-channels FinFET with multiple fins

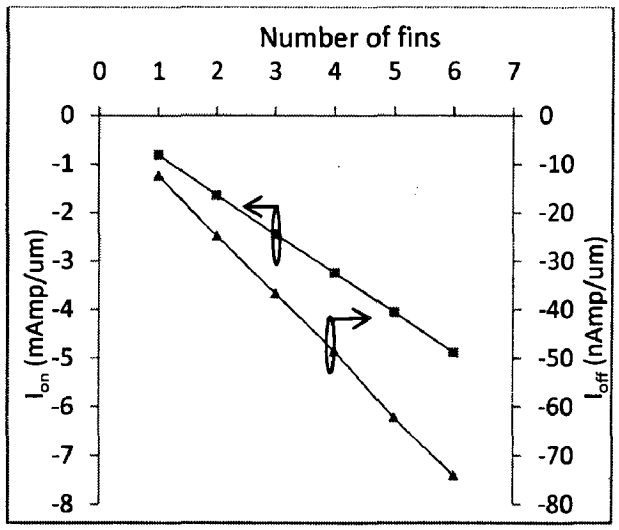

Figure 4.17: I_{on} and I_{off} of parallel combination of two p-channels FinFET with multiple fins

Figure 4.18-4.29 shows layout schemes used for simulating Inverter, 2-input NAND gate, 2-input NOR gate and SR latch and their corresponding logic delays.

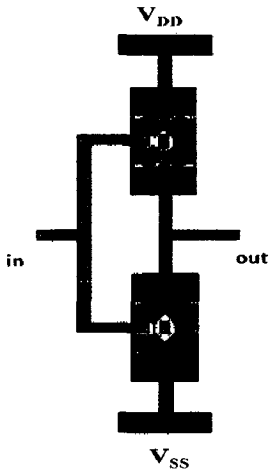

Figure 4.18: Layout used for Inverter
(not to scale)

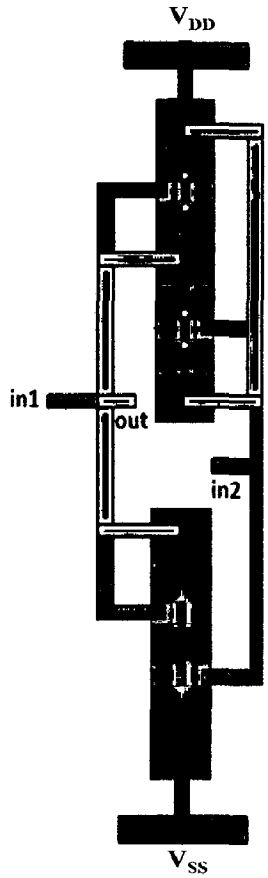

Figure 4.19: Layout used for NAND-2
(not to scale)

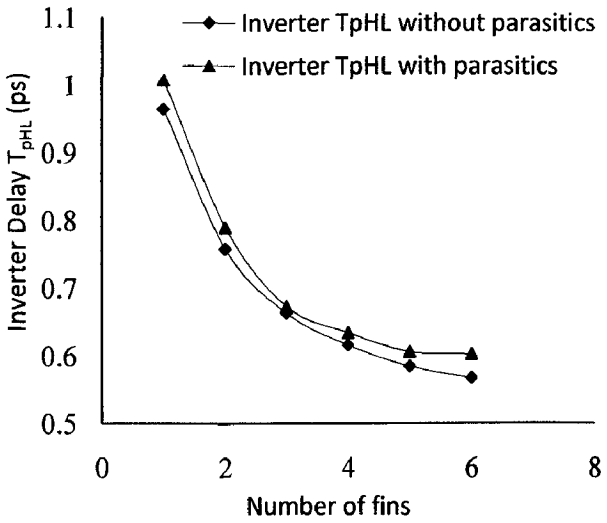

Figure 4.20: Logic high to logic low delay of inverter with and without parasitics

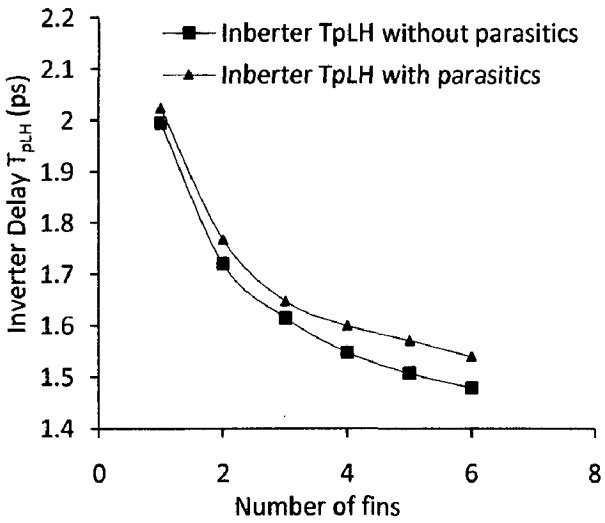

Figure 4.21: Logic low to logic high delay of Inverter with and without parasitics

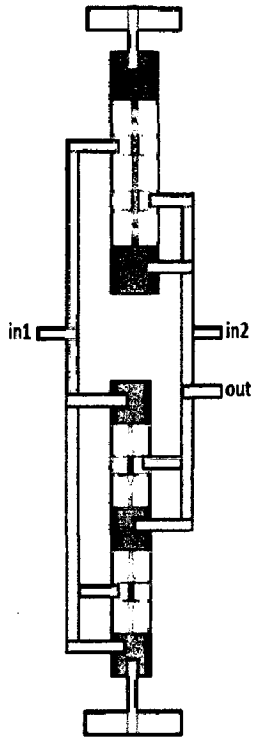

Figure 4.22: Layout used for NOR-2 (not to scale)

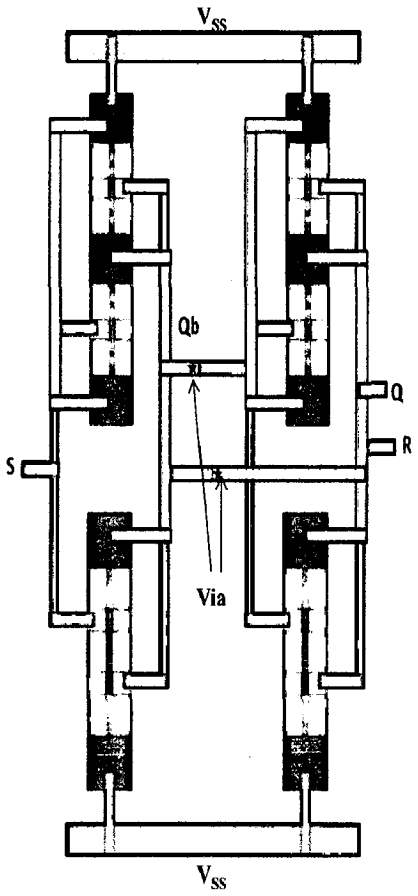

Figure 4.23: Layout used for SR NAND latch (not to scale)

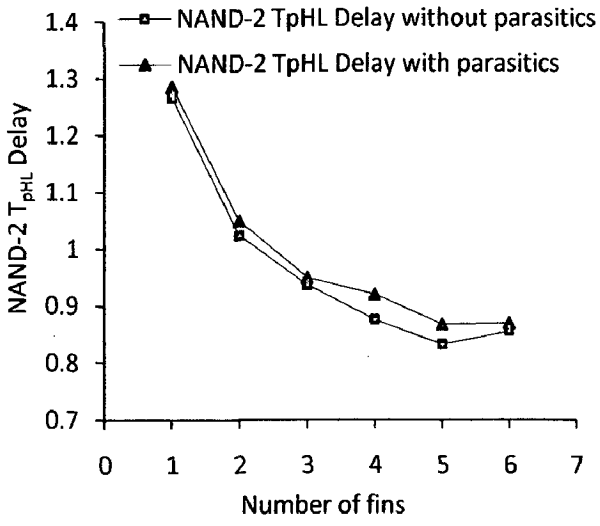

Figure 4.24: Logic high to logic low delay of 2-input NAND gate with and without parasitics

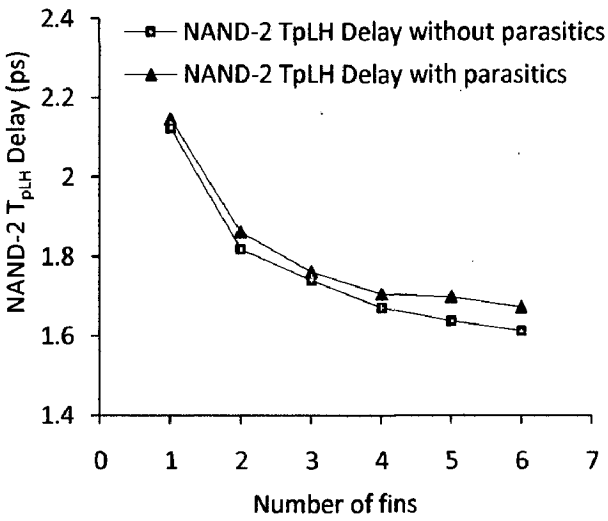

Figure 4.25: Logic low to logic high delay of 2-input NAND gate with and without parasitics

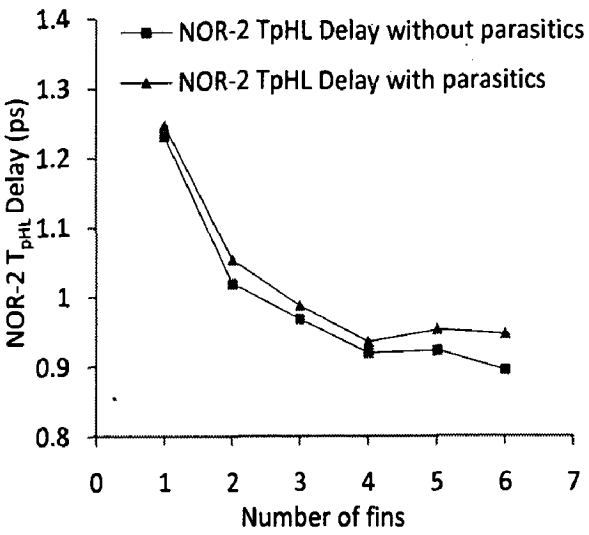

Figure 4.26: Logic high to logic low delay of 2-input NOR gate with and without parasitics

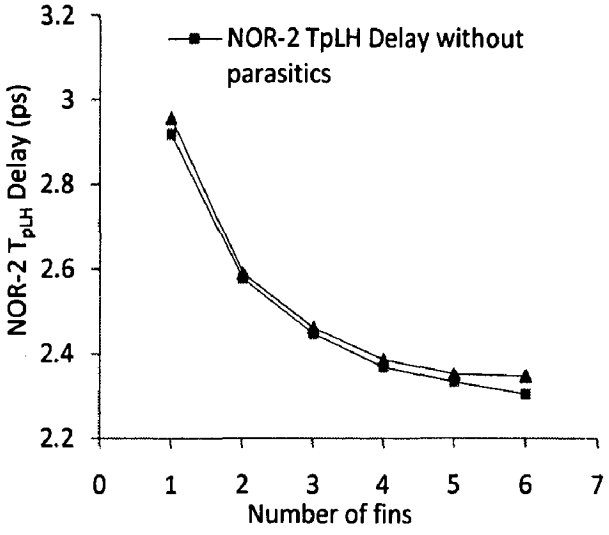

Figure 4.27: Logic low to logic high delay of 2-input NOR gate with and without parasitics

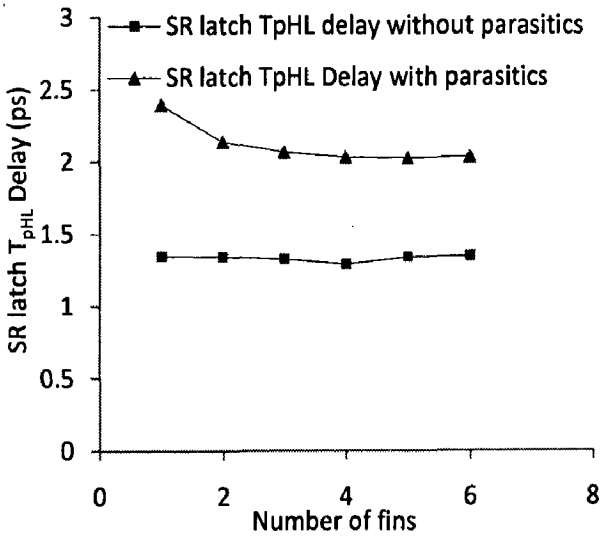

Figure 4.28: Logic high to logic low delay of SR latch by NAND gate with and without parasitics

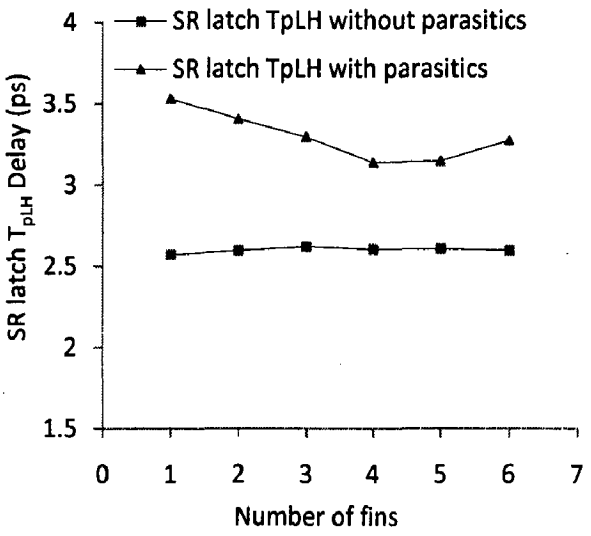

Figure 4.29: Logic low to logic high delay of SR latch by NAND gate with and without parasitics

Discussion

It was observed that the I_{on} and I_{off} currents are reduced in case of the series combination of two FinFET devices (Figures 4.14 & 4.15) and currents are increased in case of parallel combination of two FinFET devices (Figures 4.16 & 4.17), used for accounting internal parasitics in simulation of standard cell, which is quite realistic.

External parasitics are added with standard cell layouts and accounted by mixed mode simulation with external parasitics. Logic delays of the two versions of standard cell i.e. without inclusion of external parasitics and with including external parasitics reveals that there is not very significant difference between two. It concludes that in case of FinFET based circuits internal parasitics of device dominates the external parasitics such as interconnect parasitics.

Chapter 5

Optimization of FinFET Device based on circuit performance

The final goal of all device scaling and optimizations is to achieve the maximum compact density of the components along with some specific device and circuit performance parameters such as ON current (I_{on}), OFF current (I_{off}), subthreshold slope (SS), basic inverter delay, power consumption etc. In this chapter, some device design parameters are varied in order to achieve the best device and circuit performance. This chapter leads to get optimized device parameters corresponding to circuit performance and also develop a methodology for scaling FinFET device for 16 nm technology.

5.1 Meaning of "16 nm" Technology

Since 2005, ITRS has stopped using the term "technology node" for describing the status of technology with respect to the scaled dimensions. Instead, each distinct scaling feature is specifically referenced as such. Until recently the gate length corresponding to a technology "node" of say "xx nm" was quite smaller than "xx nm" (in fact approximately equal to xx/2). This "xx nm" actually referred to the metal half pitch in DRAM. The reduction from generation to generation of the DRAM half-pitch of metal by 30 % (0.7×the previous technology generation) identified a "technology node".

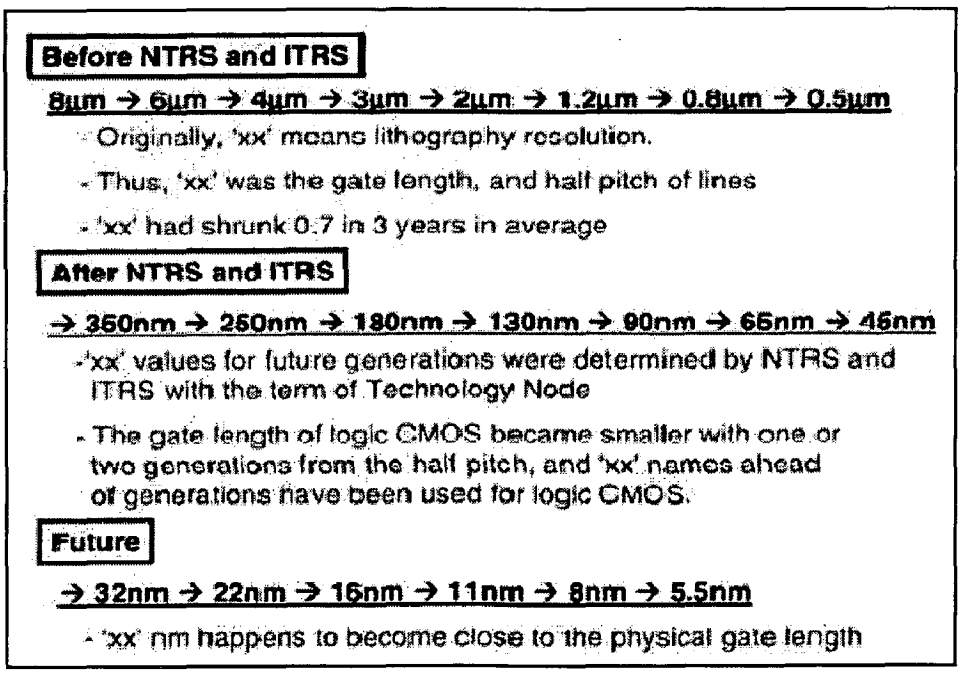

Figure 5.1: Meaning of "xx nm" Technology [58]

But around the 22nm node and beyond, when we talk of "xx nm" technology, the gate length is close to "xx nm" [58], so 16 nm technology corresponds to a physical gate length of 16 nm. Figure 5.1 puts these ideas in proper perspective. Here NTRS stands for "National Technology Roadmap for Semiconductors" – the precursor to the ITRS.

Device design parameters which are varied for this exercise are pad doping concentration, lateral diffusion standard deviation σ of source and drain extension doping, gate oxide thickness t_{ox}, source and drain extension spacer dielectric constants $K_{S\,ext}$ and $K_{D\,ext}$.

5.2 Source/Drain Pad Doping Engineering

Source/Drain pad doping is an important aspect for increasing device performance. Pads are doped with very high doping so as to decrease the resistance offered by pads. Thus generally high pad doping are used in FinFET, but with increasing pad doping concentration carries scattering in pad region increases and carrier mobility suffers a lot. So it may lead to increase pad resistance. The device parameters used in this simulation were as follows: L_g =16 nm, T_{fin}=8 nm, T_{ox} = 1.1 nm, spacer dielectric constant $K_{S\,ext}$= $K_{D\,ext}$ = 7.5, extension region σ = 2 nm. Figures 5.2- 5.9 show various device parameters extracted with varying pad doping concentration.

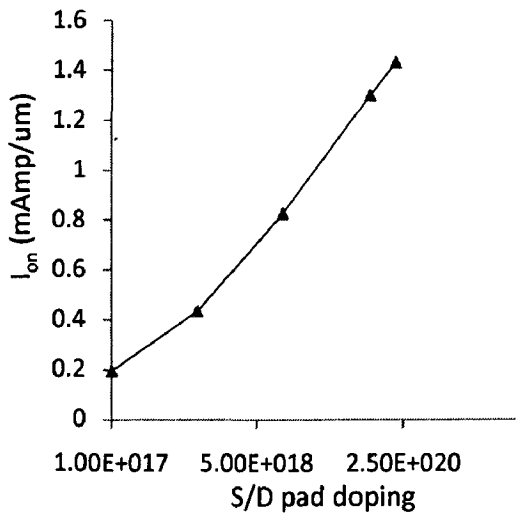

Figure 5.2: I_{on} with varying pad S/D doping

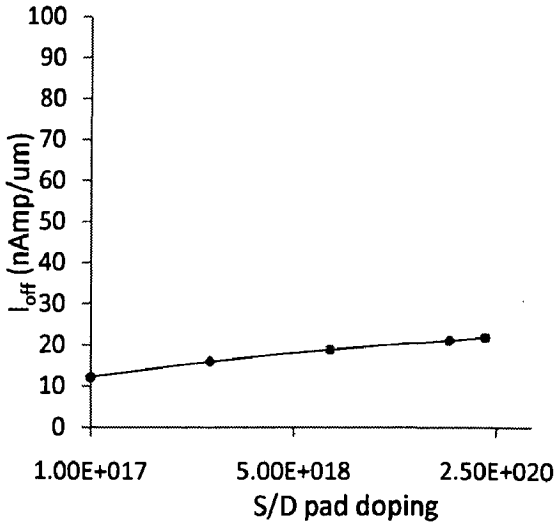

Figure 5.3: I_{off} with varying pad S/D doping

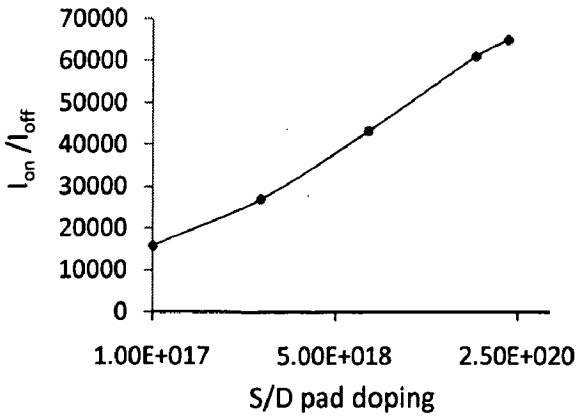

Figure 5.4: I_{on}/I_{off} with varying pad S/D pad doping

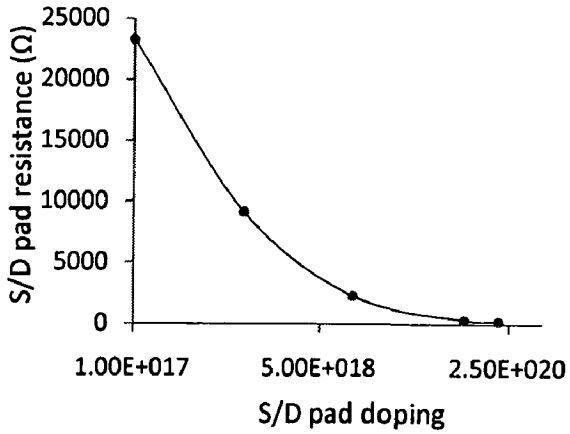

Figure 5.5: S/D pad resistance with varying S/D pad doping

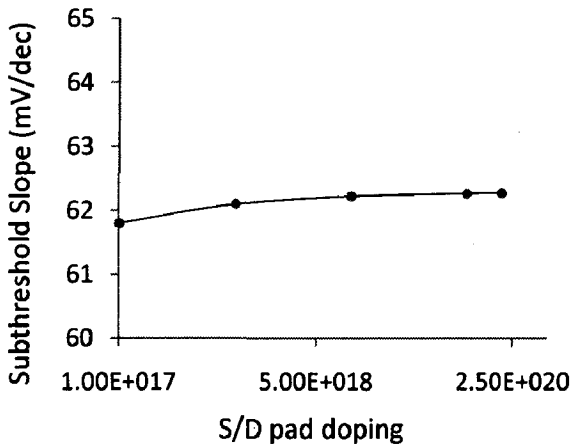

Figure 5.6: Variation of SS with S/D pad doping at V_d=0.05V

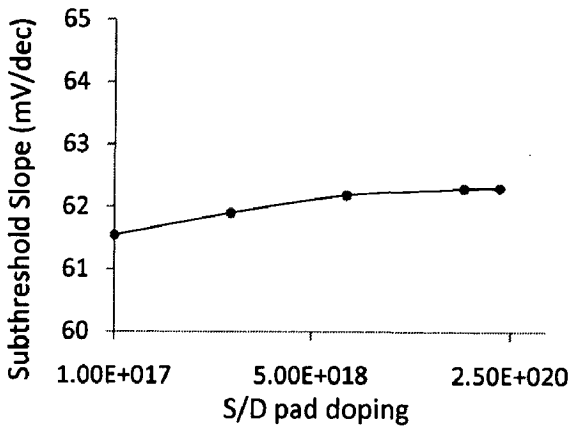

Figure 5.7: Variation of SS with S/D pad doping at V_d=1V

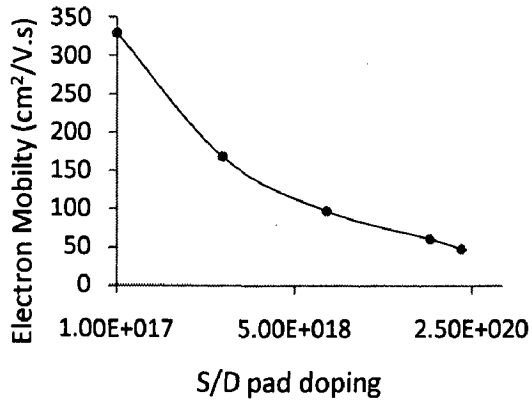

Figure 5.8: Electron mobility (cm^2/V.s) with varying S/D pad doping

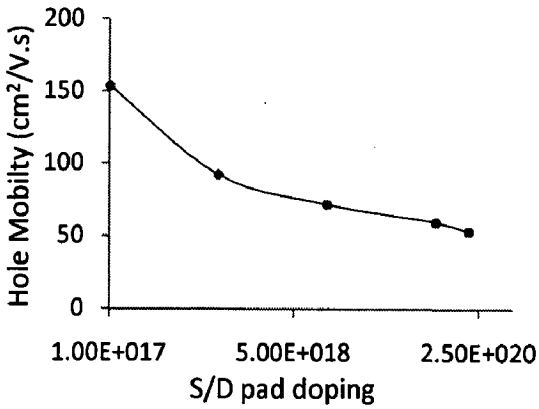

Figure 5.9: Hole mobility (cm^2/V.s) with varying S/D pad doping

For checking circuit performance by changing S/D pad doping concentration, an inverter with a Fan-Out 4 (FO4) stage is made and simulated by mixed mode simulation. A pulse input voltage with rise time t_{rise} =10 ps and fall time t_{fall} =10 ps is applied. Now with this arrangement, output logical high to low T_{pHL} (time taken for o/p to come from high level to 50% of maximum value), low to high T_{pLH} (time taken for o/p to come from low level to 50% of maximum value), output rise time $t_{o/p\ rise}$ (time taken for o/p to come from 20% to 80% of maximum value), output fall time $t_{o/p\ fall}$ (time taken for o/p to come from 80% to 20% of maximum value) are extracted. Figures 5.10-5.13 show the logic delays extracted for inverter with FO4 load:

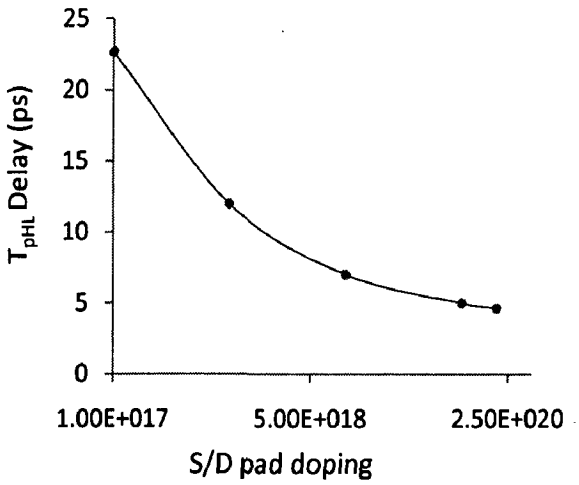

Figure 5.10: Variation of inverter T_{pHL} with S/D pad doping

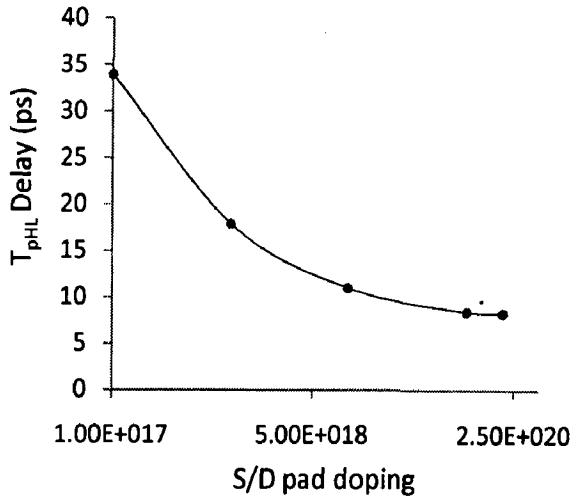

Figure 5.11: Variation of inverter T_{pHL} with S/D pad doping

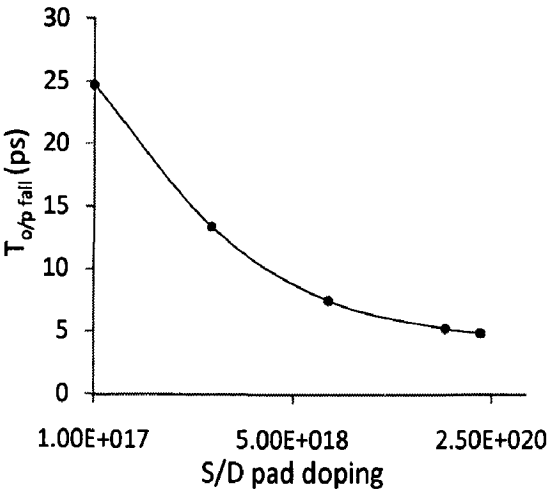

Figure 5.12: Variation of $T_{o/p\ fall}$ with S/D pad doping

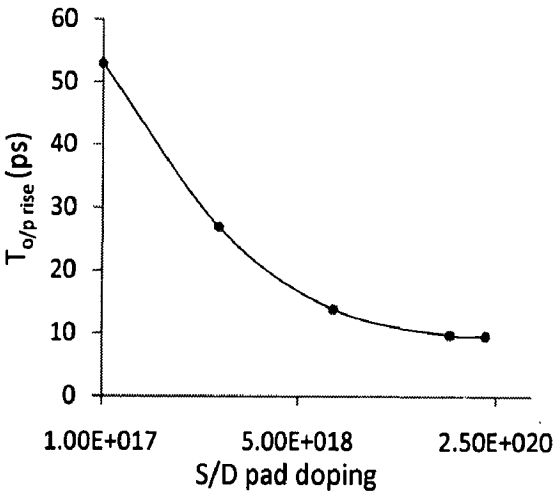

Figure 5.13: Variation of $T_{o/p\ fall}$ with S/D pad doping

Discussion

Although with increasing pad doping concentration, mobility of carriers decreased because of increased scattering but the pad resistance is decreased. Decrease in $R_{S/D\ pad}$ dominates and thus I_{on} increases very significantly with increasing S/D pad doping (Figure 5.2). Increased pad doping increases carrier concentration in fin region due to which subthreshold leakages also increase but this is negligible (Figure 5.3). With increasing pad doping concentration, pad resistance decreases very significantly also subthreshold slope increased because of increase in leakage current (Figures 5.6 & 5.7). Due to increased carrier scattering carrier mobility decreased significantly (Figures 5.8 & 5.9). T_{pHL}, T_{pLH}, $T_{o/p\ rise}$, $T_{o/p\ fall}$ of inverter with fan out 4 load decreases because of increased I_{on}.

5.3 Gate Oxide thickness and Spacer Dielectric Constant Engineering

Gate oxide thickness (t_{ox}) is one of the most important parameter of device design, with scaling gate length; the gate oxide thickness also needs to be reduced. In this section device parameters such as I_{on}, I_{off}, subthreshold slope, channel resistance etc. and circuit performance parameters of inverter with FO4 load as delays, large signal input capacitance (C_{inv}) and parasitic capacitance at drain terminal (C_p) and extension resistance are analyzed.

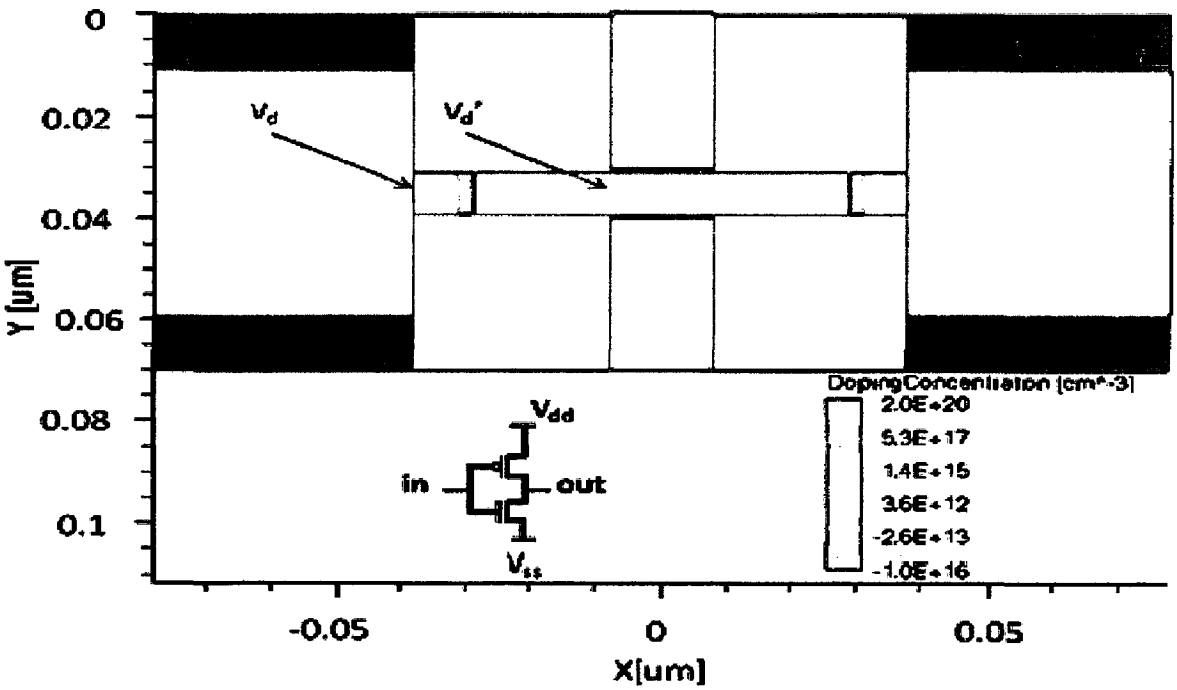

Figure 5.14: N-channel FinFET device structure and scheme used in this work

Source Drain Extension (SDE) resistance $R_{S/D}$ is extracted from the values of drain voltage V_d and voltage at the "edge" of drain/source extension and channel regions V_d' for a given current for different spacer dielectric constants K (Figure 5.14).

The device parameters used in this simulation were as follows: L_g =16 nm, T_{fin}=8 nm, spacer dielectric constant $K_{S\ Ext} = K_{D\ Ext}$ = 3.9, 7.5 and 15, pad doping concentration = 2e20 cm^{-3}. Figures 5.15-5.23 show various device parameters extracted with varying t_{ox} and $K_{S/D\ Ext}$.

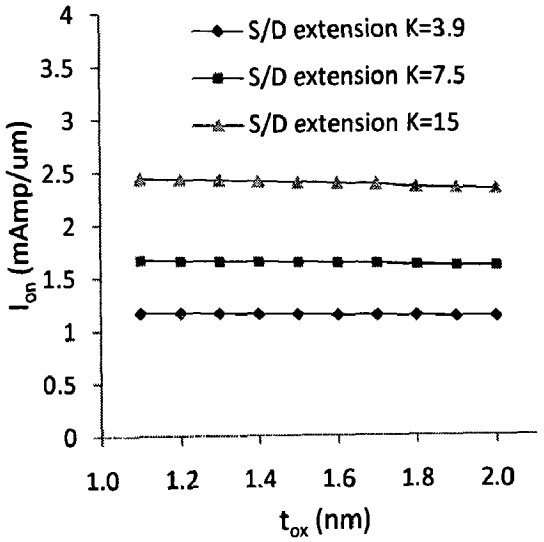

Figure 5.15: Variation of I_{on} with t_{ox} and $K_{S/D\ Ext}$

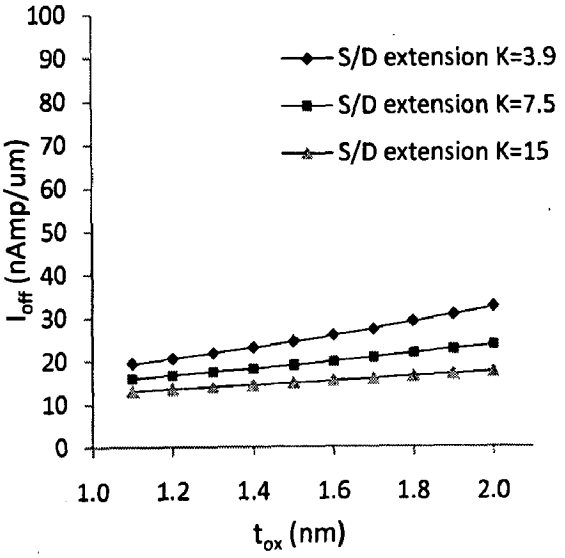

Figure 5.16: Variation of I_{off} with t_{ox} and $K_{S/D\ Ext}$

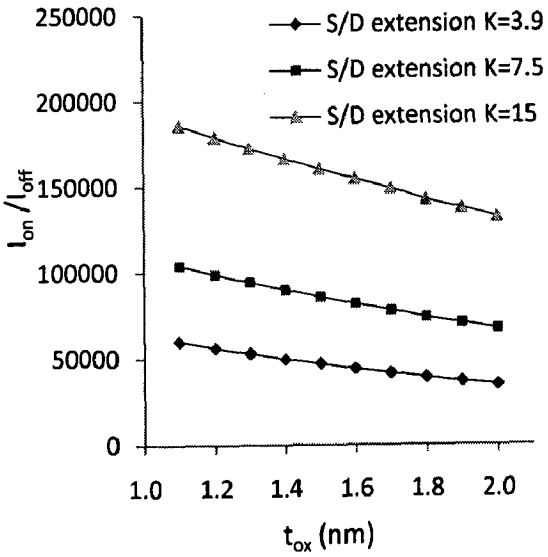

Figure 5.17: Variation of I_{on}/I_{off} with t_{ox} and $K_{S/D\ Ext}$

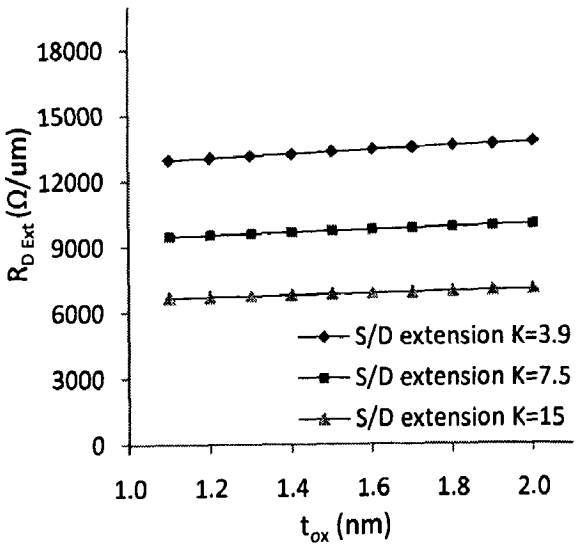

Figure 5.18: Variation of Drain extension region resistance with t_{ox} and $K_{S/D\ Ext}$

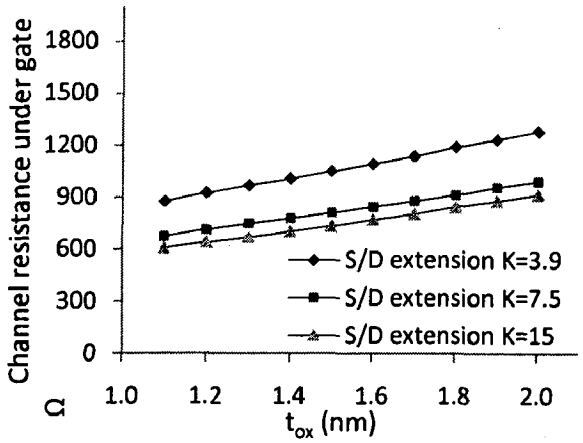

Figure 5.19: Variation of channel resistance under gate region with t_{ox} and $K_{S/D\ Ext}$

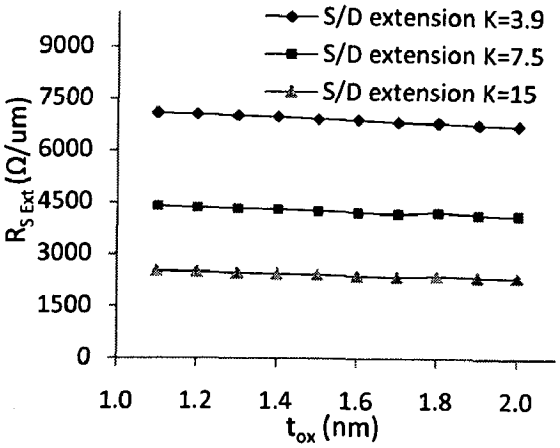

Figure 5.20: Variation of Source extension resistance with t_{ox} and $K_{S/D\ Ext}$

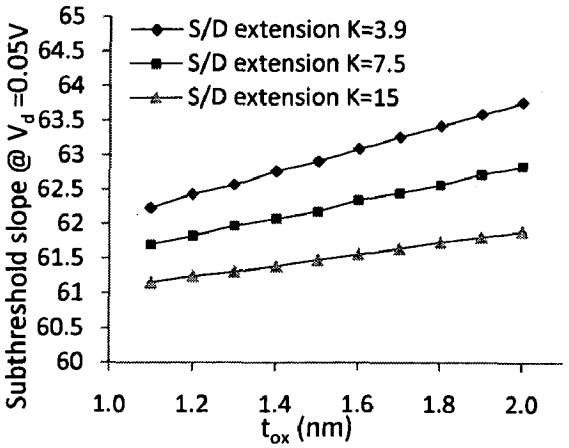

Figure 5.21: Variation of Subthreshold slope at V_d = 0.05 V with t_{ox} and $K_{S/D\ Ext}$

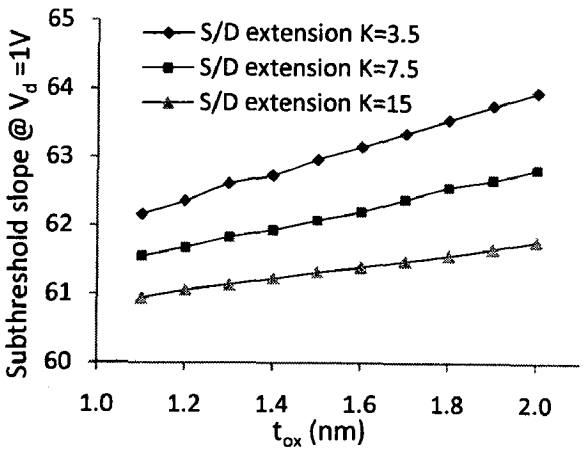

Figure 5.22: Variation of Subthreshold slope at V_d = 1 V with t_{ox} and $K_{S/D\ Ext}$

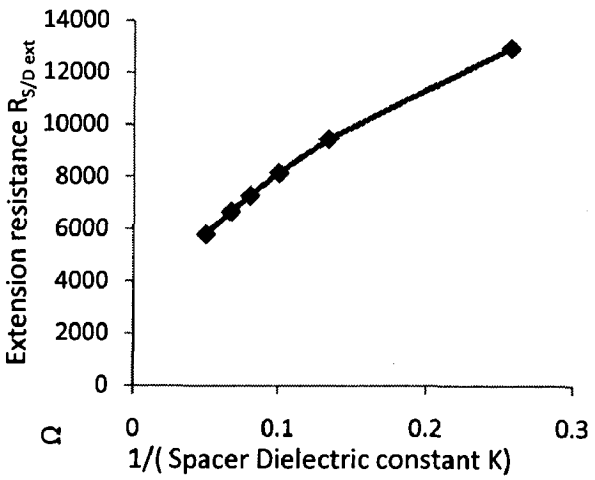

Figure 5.23: Variation of Extension resistance with 1 / (spacer dielectric constant)

For checking circuit performance by varying gate oxide thickness along with S/D spacer dielectric constant (K), an inverter with a Fan-Out 4 (FO4) stage is made and simulated by mixed mode simulation. A pulse input voltage with rise time t_{rise} =10 ps and fall time t_{fall} =10 ps is applied. Now with this arrangement, output logical high to low T_{pHL} (time taken for o/p to come from high level to 50% of maximum value), low to high T_{pLH} (time taken for o/p to come from low level to 50% of maximum value), output rise time $t_{o/p\ rise}$ (time taken for o/p to come from 20% to 80% of maximum value), output fall time $t_{o/p\ fall}$ (time taken for o/p to come from 80% to 20% of maximum value) are extracted. Following are results of inverter with FO4 load. Figures 5.24 & 5.25 show logic delays of Inverter with Fan Out 4 load with a height of 40 nm with varying t_{ox}.

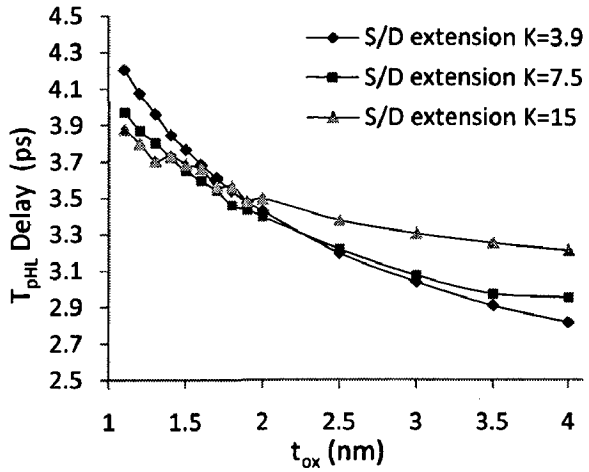

Figure 5.24: Variation of logic high to low delay (T_{pHL}) with t_{ox} and $K_{S/D\ Ext}$

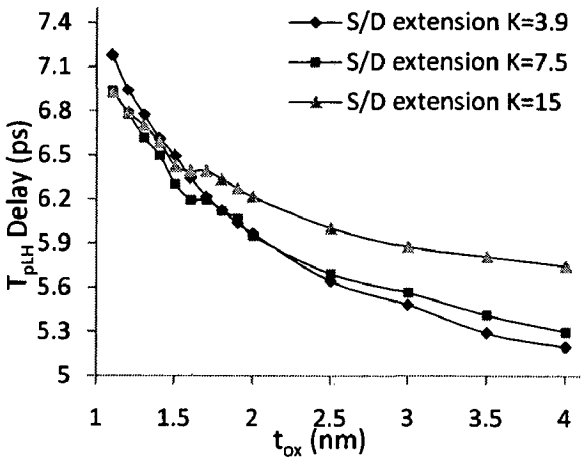

Figure 5.25: Variation of logic low to high delay (T_{pLH}) with t_{ox} and $K_{S/D\ Ext}$

Inverter's input capacitance (C_{inv}) is extracted from the gate terminal charge obtained from mixed-mode simulations (Figure 2.26). The inverter's input voltage is increased from 0 to V_{dd} and the corresponding gate current is integrated to obtain change in gate charge ΔQ_g. The ratio of ΔQ_g and V_{dd} is the large signal input capacitance C_{inv}. We extract the inverter's parasitic capacitance C_p by integrating the difference in currents entering from the supply node I_{Vdd} and that leaving from the ground node I_{Vss}. While doing this, no external load capacitance is applied ($C_l = 0$).

The integration of (I_{Vdd}-I_{Vss}) is performed over the time period Δt when the output node voltage transits from 0 to V_{dd} (or V_{dd} to 0). The value of C_p includes the effective contributions at the

output node due to all overlap and fringe effects in the device. In extracting the value of C_p, we took care to keep input and output transition times Δt equal so that Miller effect is considered (Figure 2.27). Figure 2.28 shows the oscillation period and operating frequency of a ring oscillator with stage, using device height of 40 nm with varying t_{ox}. Figure 2.29 shows the power drawn by each stage of 3 stage ring oscillator with varying t_{ox}.

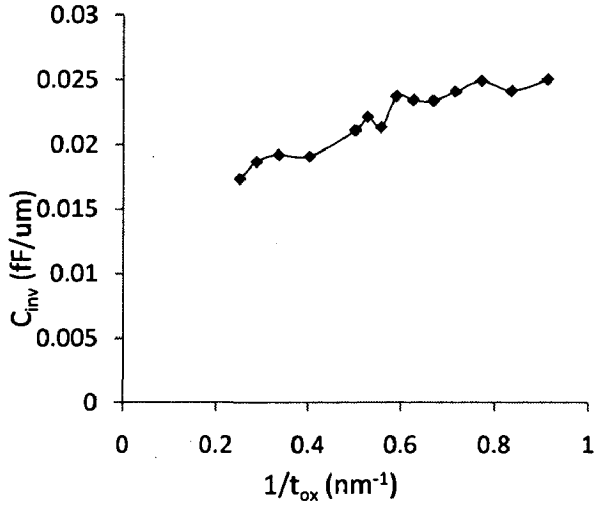

Figure 5.26: Variation of input capacitance of inverter C_{inv} with t_{ox} and $K_{S/D\ Ext}$

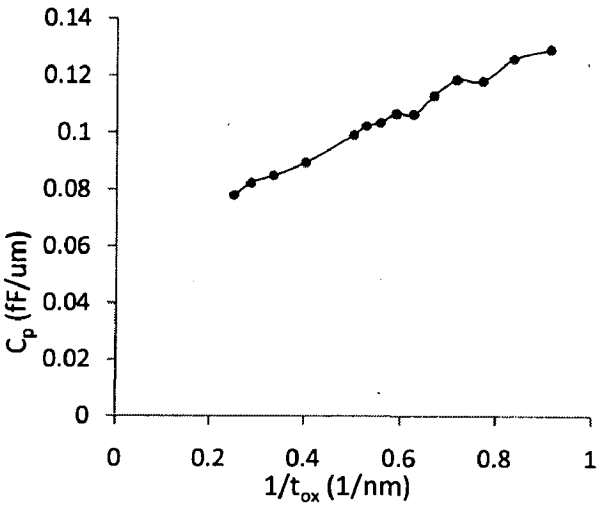

Figure 5.27: Variation of parasitic capacitance of inverter C_p with and $K_{S/D\ Ext}$

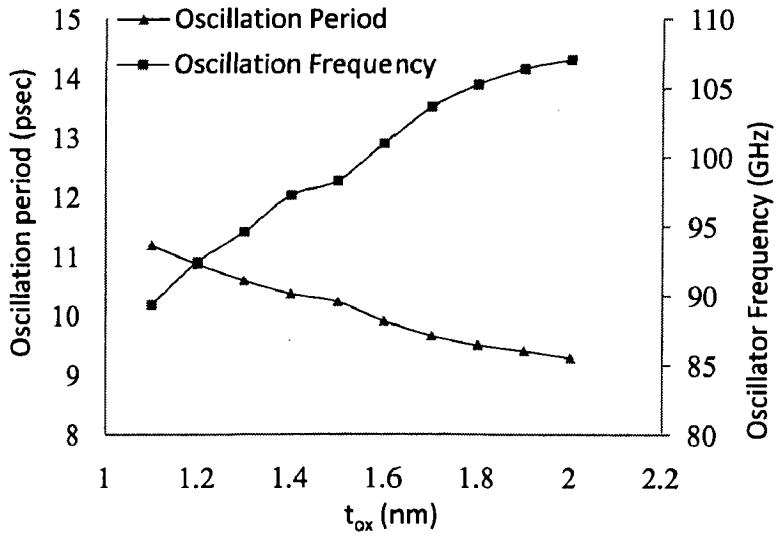

Figure 5.28: Variation Oscillation period and oscillation frequency of 3-stage ring oscillator with t_{ox}

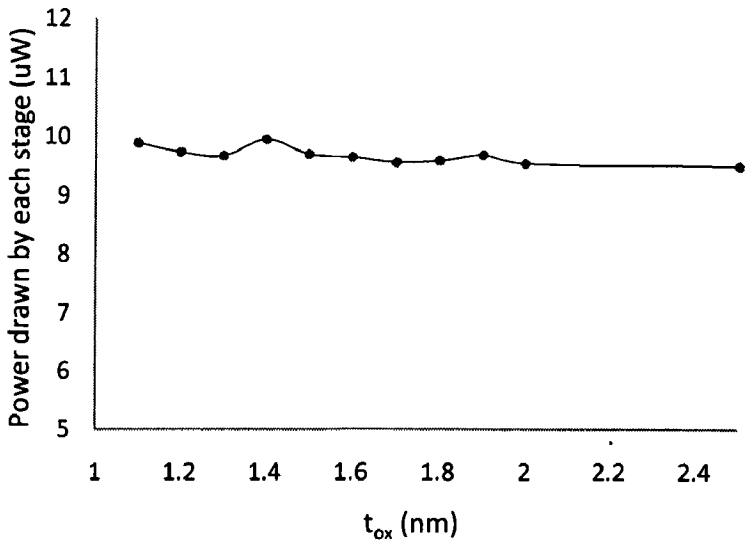

Figure 5.29: Power drawn by each stage of 3-stage ring oscillator vs. t_{ox}, K=7.5

5.3.1. Three transistor analogy and Novel Scaling Methodology

We observe in Figure 5.23 that the resistance of SDE region is inversely proportional to spacer K when all other device parameters are kept unchanged. On the other hand, we observe in Figure 5.26 that the capacitance at gate terminal (which includes gate to channel, outer and inner fringe capacitances) is directly proportional to $1/t_{ox}$. Therefore, an underlap FinFET device is made of three transistors: one being the "main" transistor which is formed by the channel and the gate oxide and others being *two* SDE transistors, schematic diagram of a FinFET by 3 transistor equivalent circuit is shown in figure 5.30.

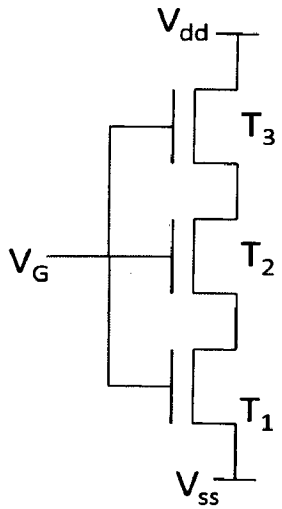

Figure 5.30: Schematic diagram of a FinFET by 3 transistor equivalent circuit

These two are the two "side" transistors formed by SDE region as channel and spacer dielectric as gate dielectric.

Since the underlap FinFET device consists of three transistors stacked in series, ON and OFF currents of the underlap device are not inversely proportional to the gate oxide thickness t_{ox} alone. I_{ON} and I_{OFF} have a weaker dependence on t_{ox} in the underlap device when compared with the corresponding parameters in the overlap device. This is contrary to conventional transistors and can be used in device design. In Figure 5.15 and 5.16, we observe that simulated values of I_{on} and I_{off} are weaker functions of t_{ox}.

Results from mixed-mode simulations show that circuit delays and dynamic power consumption reduce with an increase in t_{ox}. The corresponding increase in I_{off} is not significant even for an increase in t_{ox} from 1.1nm to 2nm. In Figures 5.24 and 5.25, we observe that inverter delay with fan-out 4 (FO4) load reduces by about 16% for an increase in t_{ox} from 1.1nm to 2nm and a spacer K of 7.5. In Figure 5.28 we observe that the frequency of operation of a 3-stage ring-oscillator increases by about 16% for an equal increase in t_{ox} and K=7.5. This increase in performance comes without any penalty in terms of the ring-oscillator power consumption, as we observe in Figure 5.29.

5.4 Asymmetric Source/Drain Extension Doping Profile Engineering

The underlap FinFET device can be assumed to be made by series connection of 3 transistors. The middle transistor is the strongest among all is made by gate oxide as insulator, fin below the gate as channel; the two side transistors are made by S/D extension as gate insulator and underlap extension region as channel are weaker than the middle transistor.

Asymmetrical structure is made by making drain side 0 nm overlaped and source side underlap as the source side underlap can make I_{off} low and drain side overlap can make larger V_{ds} across main transistor to increase I_{on}.

The device parameters used in this simulation were as follows: L_g =16 nm, T_{fin}=8 nm, t_{ox} = 1.1 nm, spacer dielectric constant $K_{S\ Ext}$ = $K_{D\ Ext}$ = 7.5, pad doping concentration = 2e20 cm^{-3}. Figures 5.31-5.33 show the current characteristics of N-channel FinFET device with varying σ on S_{Ext}.

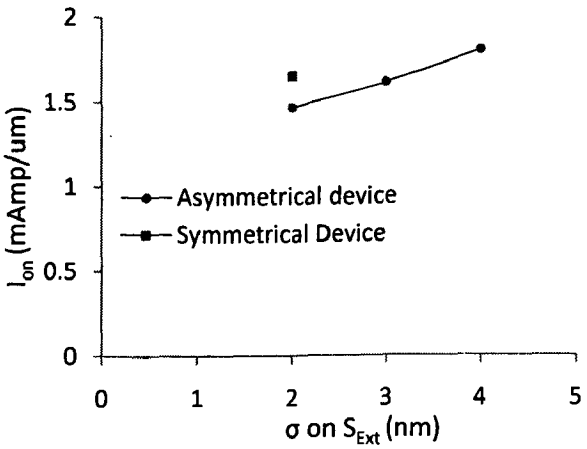

Figure 5.31: Variation of I_{on} for Symmetric and Asymmetric extension profile with σ on S_{Ext}

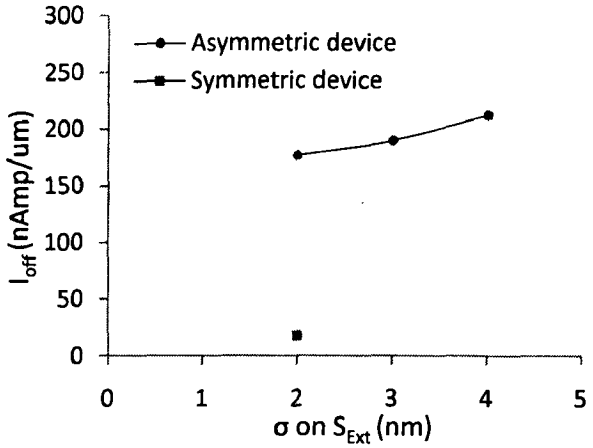

Figure 5.32: Variation of I_{off} for Symmetric and Asymmetric extension profile with σ on S_{Ext}

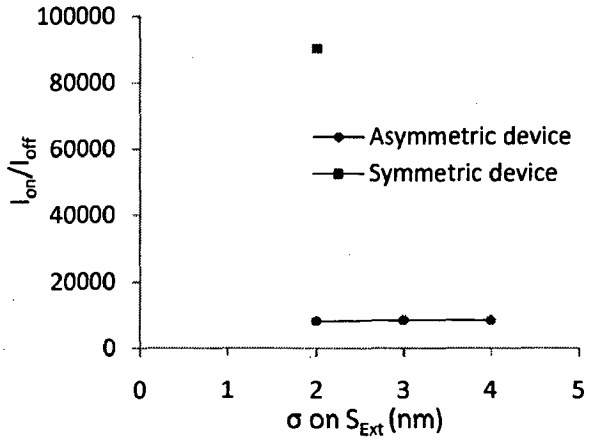

Figure 5.33: Variation of I_{on}/I_{off} for Symmetric and Asymmetric extension profile with σ on S_{Ext}

For checking circuit performance by changing lateral diffusion standard deviation (σ) on Source extension region (S_{Ext}) when Drain extension is 0 nm overlapped an inverter with device height of 40 nm, a Fan-Out 4 (FO4) stage is made and simulated by mixed mode simulation. A pulse input voltage with rise time t_{rise} =10 ps and fall time t_{fall} =10 ps is applied. Now with this arrangement output logical high to low T_{pHL} (time taken for o/p to come from high level to 50% of maximum value), low to high T_{pLH} (time taken for o/p to come from low level to 50% of maximum value), output rise time $T_{o/p\ rise}$ (time taken for o/p to come from 20% to 80% of maximum value), output fall time $T_{o/p\ fall}$ (time taken for o/p to come from 80% to 20% of maximum value) are extracted. Figures 5.34-5.37 show logic delays extracted of inverter with FO4 load with varying σ on S_{Ext}.

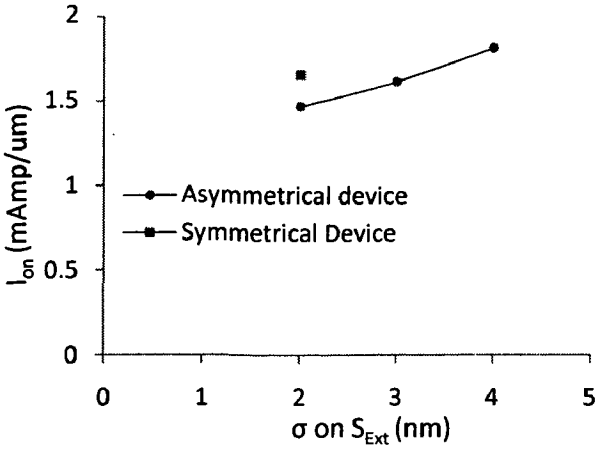

Figure 5.31: Variation of I_{on} for Symmetric and Asymmetric extension profile with σ on S_{Ext}

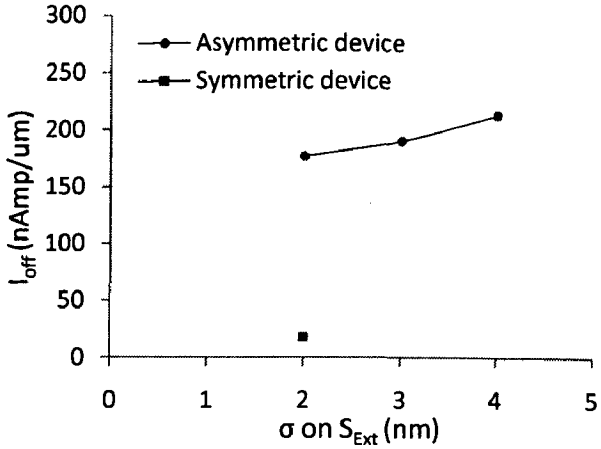

Figure 5.32: Variation of I_{off} for Symmetric and Asymmetric extension profile with σ on S_{Ext}

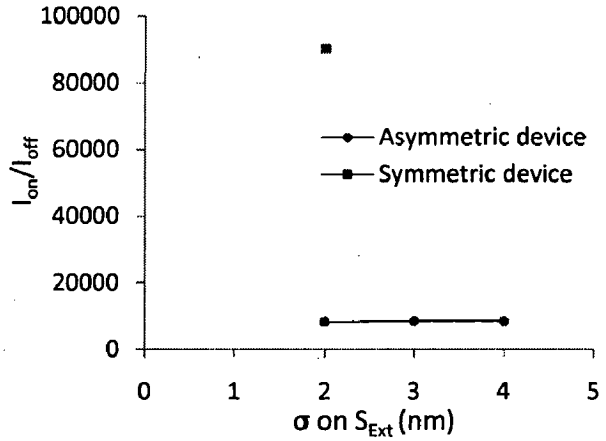

Figure 5.33: Variation of I_{on}/I_{off} for Symmetric and Asymmetric extension profile with σ on S_{Ext}

For checking circuit performance by changing lateral diffusion standard deviation (σ) on Source extension region (S_{Ext}) when Drain extension is 0 nm overlapped an inverter with device height of 40 nm, a Fan-Out 4 (FO4) stage is made and simulated by mixed mode simulation. A pulse input voltage with rise time t_{rise} =10 ps and fall time t_{fall} =10 ps is applied. Now with this arrangement output logical high to low T_{pHL} (time taken for o/p to come from high level to 50% of maximum value), low to high T_{pLH} (time taken for o/p to come from low level to 50% of maximum value), output rise time $T_{o/p\ rise}$ (time taken for o/p to come from 20% to 80% of maximum value), output fall time $T_{o/p\ fall}$ (time taken for o/p to come from 80% to 20% of maximum value) are extracted. Figures 5.34-5.37 show logic delays extracted of inverter with FO4 load with varying σ on S_{Ext}.

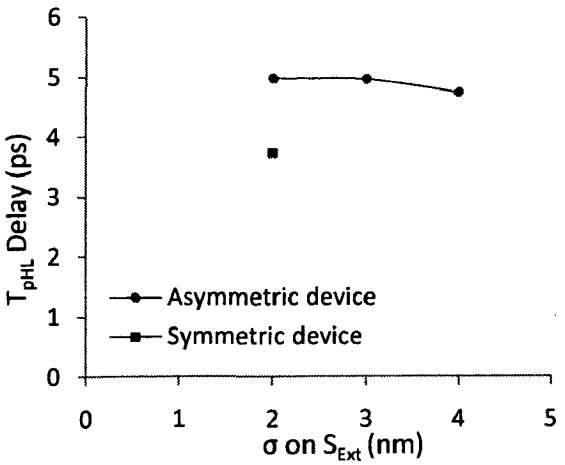

Figure 5.34: Variation of T_{pHL} Delay for Symmetric and Asymmetric extension profile with σ on S_{Ext}

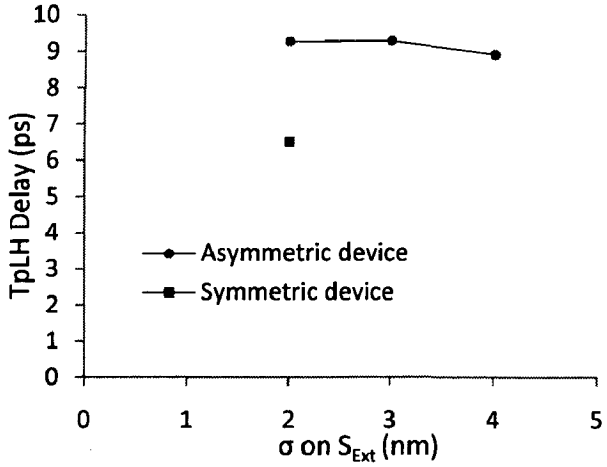

Figure 5.35: Variation of T_{pLH} Delay for Symmetric and Asymmetric extension profile with σ on S_{Ext}

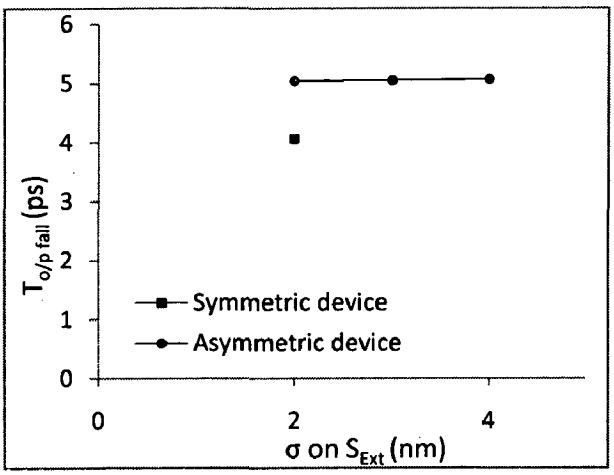

Figure 5.36: Variation of $T_{o/p\ fall}$ for Symmetric and Asymmetric extension profile with σ on S_{Ext}

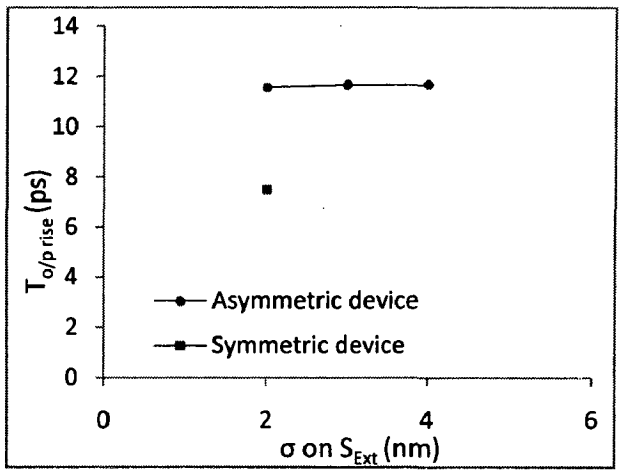

Figure 5.37: Variation of $T_{o/p\ rise}$ for Symmetric and Asymmetric extension profile with σ on S_{Ext}

Discussion

With using asymmetrical structure which is made 0nm overlapped on drain side and underlapped on source side and comparing its parameters with a symmetrical device which is underlapped on both side symmetrically we find that the symmetrical device is better than an asymmetrical device in all respects. We find that symmetrical device has improved I_{on} than drain side overlapped device (Figure 5.31). It can be explained by using three transistor analogy of FinFET device. With using overlap structure on drain side reduces the voltage drop in the drain extension region and V_{ds} of the top transistor reduces and V_{gs} of any transistor does not improve, so the

current through composite structure get reduced as the two side transistors form the bottleneck for FinFET current.

For case of I_{off} as the gate voltage is low enough, not able to create inversion in fin, the side transistors can be considered as resistances. The drain overlap reduces the resistance of drain extension so subthreshold leakages are increased in this case (Fig. 5.32), it reduces I_{on}/I_{off} of asymmetrical device drastically.

Figures 5.34 & 5.35 show that logic high to low and low to high delays of an inverter with fan out 4 load made by asymmetrical device are larger than that of made by a symmetrical device, because of smaller I_{on}. The same is true for rise time and fall time of FO4 inverter.

5.5. Asymmetric Spacer Dielectric constant scheme

As we have seen that the middle transistor of FinFET is strongest and the side transistors are weaker. With increasing extension spacer dielectric constant (K) more fringe lines terminate on the extension region fin and thus resistance of extension region decreases.

In this section, we go through asymmetric spacer dielectric constants. In first case, dielectric constant on source extension ($K_{S\ Ext}$) kept constant at 7.5 and dielectric constant on drain extension ($K_{D\ Ext}$) is varied. In second case $K_{D\ Ext}$ is kept constant at 7.5 and $K_{S\ Ext}$ is varied. In both cases all device and circuit parameters are extracted and analyzed. Figures 5.38-5.45 show various device parameters extracted with varying spacer dielectric constant.

The device parameters used in this simulation were as follows: L_g =16 nm, T_{fin}=8 nm, t_{ox} =1.1 nm, pad doping concentration = 2e20 cm^{-3}.

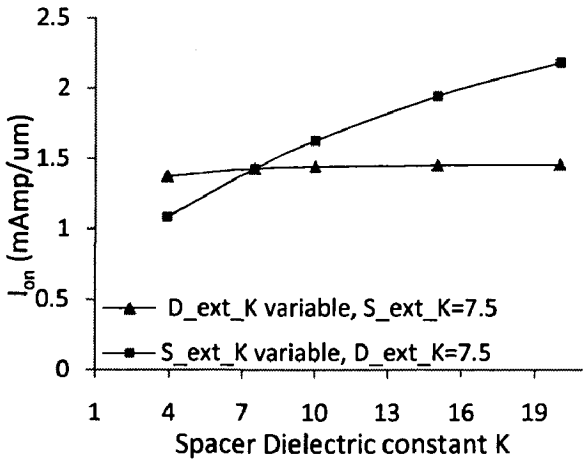

Figure 5.38: Variation I_{on} with K

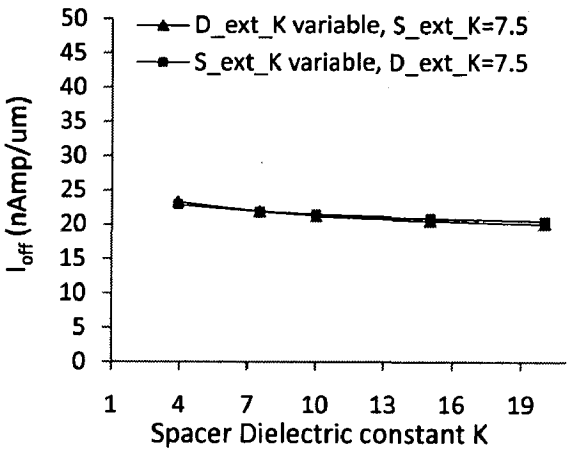

Figure 5.39: Variation I_{off} with K

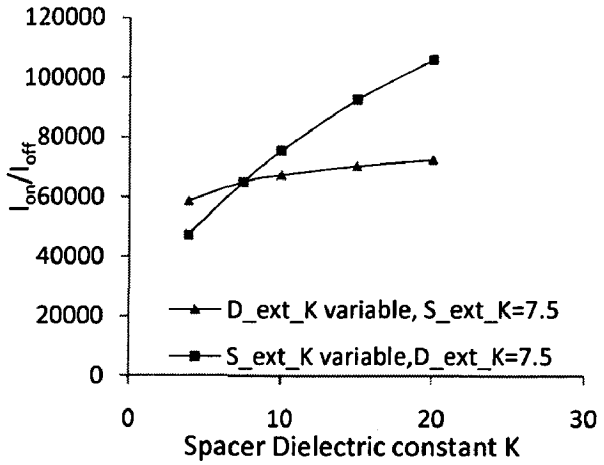

Figure 5.40: Variation I_{on}/I_{off} with K

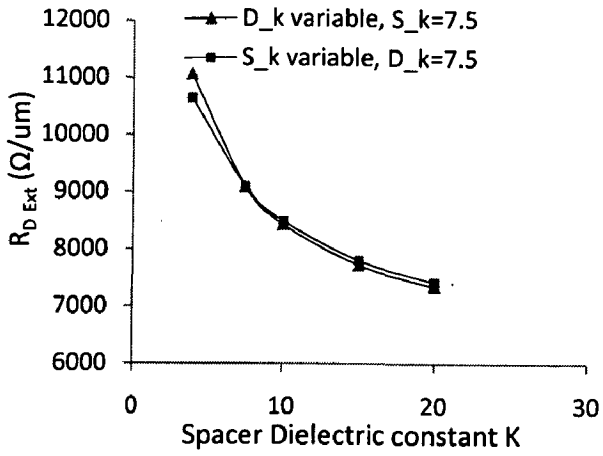

Figure 5.41: Variation Drain extension resistance with K

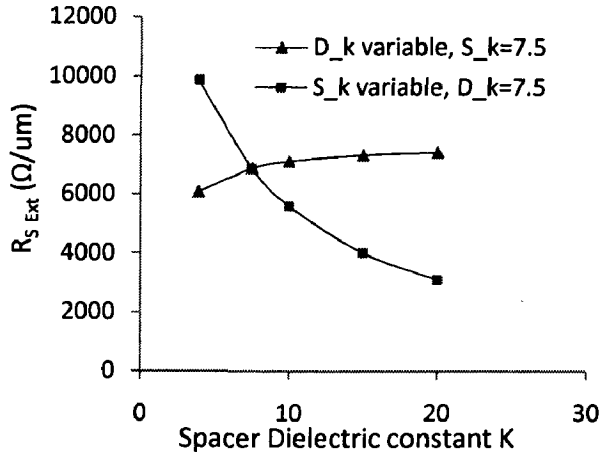

Figure 5.42: Variation Source extension resistance with K

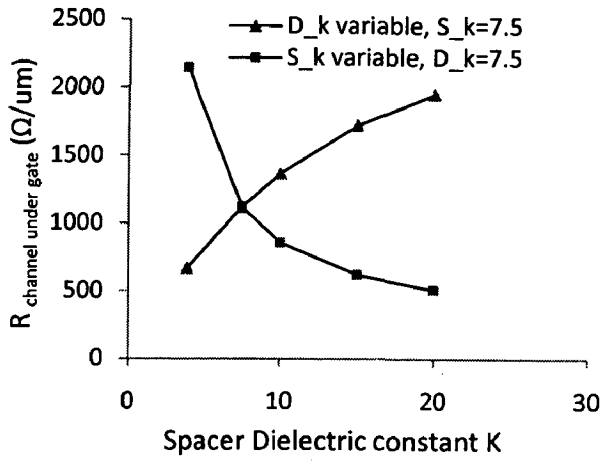

Figure 5.43: Variation resistance under gate with K

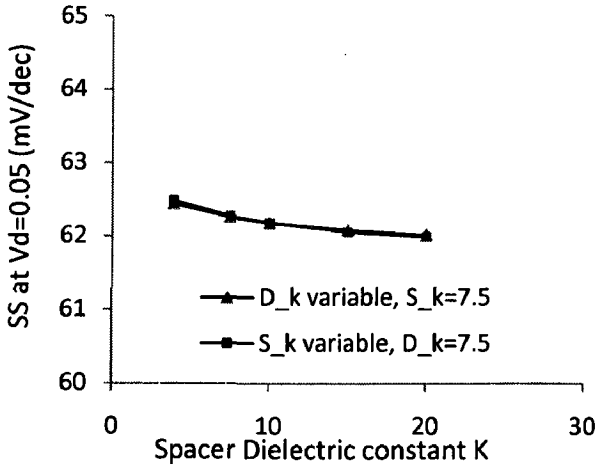

Figure 5.44: Variation Subthreshold slope at V_d=0.05 with K

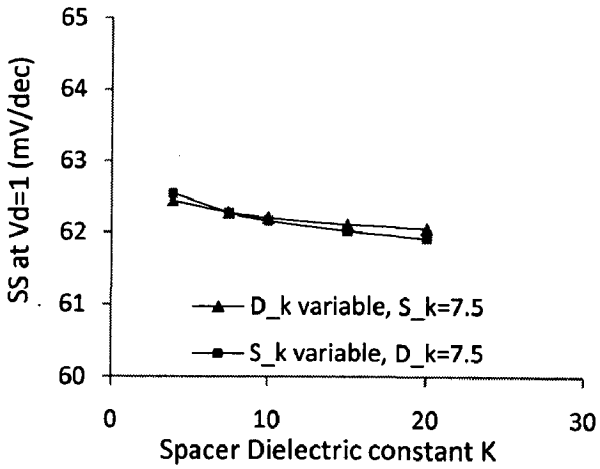

Figure 5.45: Variation Subthreshold slope at V_d=1 with K

For analyzing the effect of changing the extension dielectric constant asymmetrically an inverter is simulated in mixed mode simulation.

Inverter's input capacitance C_{inv} ($C_{inv} = C_{gate+sext+dext}$) is extracted from the gate terminal charge obtained from mixed-mode simulations. The inverter's input voltage is increased from 0 to V_{dd} and the corresponding gate current is integrated to obtain change in gate charge ΔQ_g. The ratio of ΔQ_g and V_{dd} is the large signal input capacitance C_{inv}, which includes the gate input capacitance as well as S/D extension capacitances due to fringe effect. In extracting the value of C_{inv}, we took care to keep input and output transition times Δt equal so that Miller effect is considered. Figures 5.46 & 5.47 show the schematic diagram of inverter circuit used and schematic diagram of underlap FinFET device by 3 transistors equivalent circuit.

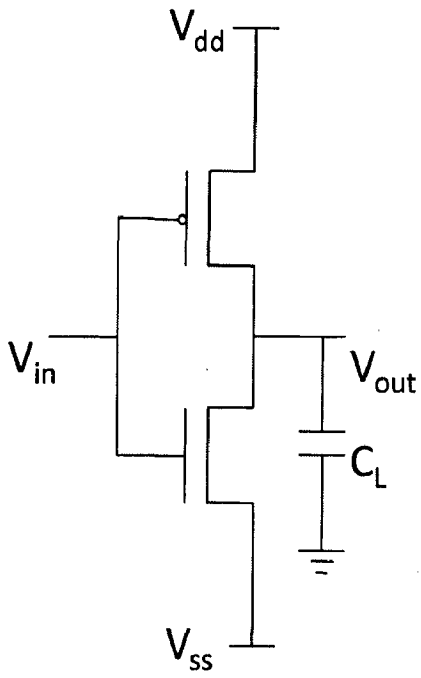

Figure 5.46: Schematic diagram of inverter circuit

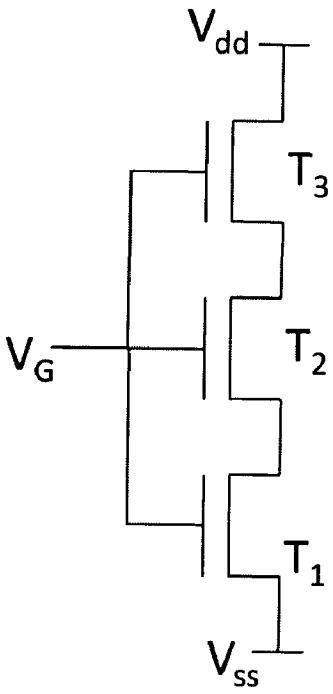

Figure 5.47: Schematic diagram of FinFET by 3T equivalent circuit

Figure 5.48 shows input capacitance of inverter (C_{inv}) with devices of height 40 nm, with varying spacer dielectric constant K.

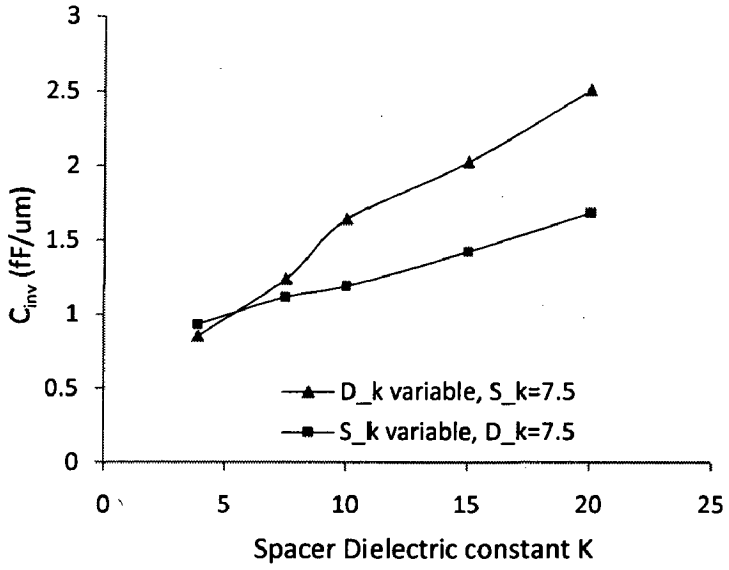

Figure 5.48: Input capacitance of inverter C_{inv} with K

Discussion

Increasing $K_{S\ Ext}$, resistance in S extension region decreased and it improves the V_{gs} for all three transistors (T_1, T_2 and T_3) and V_{ds} for T_1 is increased. It improves I_{on} of composite circuit. Whereas with increase in $K_{D\ Ext}$, resistance in D extension region decreased so V_s of T_3 increase causing reduction in V_{gs} of T_3 but V_{ds} of T_2 and T_3 increase and V_{gs} of T_2 and T_3 are unaffected. The overall result of these effects causes approximately no change in I_{on} of composite device (Figure 5.38). I_{off} is effectively constant with $K_{S/D\ Ext}$ variation (Figure 5.39).

With increasing $K_{S\ Ext}$, extension resistances $R_{S\ ext}$ and $R_{D\ Ext}$ decreased because improving $K_{S\ Ext}$ reduces $R_{S\ Ext}$ because of increasing inversion under source region and increasing $K_{S\ Ext}$, increases V_s of T_3 which reduces V_{ds} of T_3 leading it away from saturation region, so $R_{D\ Ext}$ reduces. With increasing $K_{D\ Ext}$, $R_{D\ Ext}$ decreases because of increasing inversion under drain region, but improved $K_{D\ Ext}$ increase V_{ds} of T_1 leading it towards saturation region so it increases $R_{S\ Ext}$ (Figure 5.42). Resistance of the region under gate follows the same trend as $R_{S\ Ext}$. Subthreshold slope decreases with increasing $K_{S/D\ Ext}$ as now gate control is increased (Figure 5.44, 5.45).

With increasing $K_{S/D\ Ext}$, C_{inv} increases. But with increasing $K_{D\ Ext}$, C_{inv} increases rapidly because it allows more charge to change in channel because of Millar Effect (Figure 5.48). So it is beneficial to increase $K_{S\ Ext}$ while $K_{D\ Ext}$ can be kept at lower value.

5.6. Modeling the Circuit Performance based on Device Parameters

Up to this point device parameters such as Ion, I_{off}, channel resistances, subthreshold slope etc and circuit performance parameters such as logic delays of inverter with fan out 4 load, rise/fall times, input capacitance C_{inv} and output node capacitance C_p are analyzed with some device design parameters i.e. S/D pad doping concentration, asymmetric S/D extension doping profile, gate oxide thickness and spacer dielectric constant and asymmetric spacer dielectric constant individually.

In this section, the dominant device parameters such as I_{on} and C_{inv} are analyzed and modeled with design parameters. In Chapter 5, it is proved that I_{on} and C_{inv} are very strongly dependent on $K_{S\,Ext}$, $K_{D\,Ext}$ and t_{ox}.

Thus

$$I_{on} = f(K_{S\,Ext}, K_{D\,Ext}, t_{ox})$$

and

$$C_{inv} = g(K_{S\,Ext}, K_{D\,Ext}, t_{ox})$$

By plotting the relations of I_{on} and C_{inv} as function of $K_{S\,Ext}$, $K_{D\,Ext}$ and t_{ox} in the previous chapter following relations are found-

$$I_{on}(K_{S\,Ext}) = 0.067\,K_{S\,Ext} + 0.893$$

$$I_{on}(K_{D\,Ext}) = -0.00056\,K_{D\,Ext}^2 + 0.01829\,K_{D\,Ext} + 1.31411$$

$$I_{on}(t_{ox}) = -0.115\,t_{ox} + 1.554$$

$$C_{inv}(K_{S\,Ext}) = 0.045\,K_{S\,Ext} + 0.874$$

$$C_{inv}(K_{D\,Ext}) = 0.101\,K_{D\,Ext} + 0.505$$

$$C_{inv}(t_{ox}) = -0.002\,t_{ox} + 1.239$$

Here t_{ox} is in units of nm.

According to Taylor series for several variables, a function f depending on $(x_1, x_2 \ldots . x_d)$ can be expressed around a point $(a_1, a_2 \ldots . . a_d)$ by following expression –

$$f(x_1, x_2 \ldots . x_d)$$
$$= \sum_{n_1=0}^{\infty} \ldots . . \sum_{n_d=0}^{\infty} \frac{(x_1 - a_1)^{n_1} \ldots (x_d - a_d)^{n_d}}{n_1! \ldots n_d!} \left(\frac{\partial^{n_1 + n_2 + \ldots n_d} f}{\partial {x_1}^{n_1} \, \partial {x_2}^{n_2} \ldots \partial {x_d}^{n_d}} \right) (a_1, a_2 \ldots . a_d)$$

Thus $I_{on}(K_{S\,Ext}, K_{D\,Ext}, t_{ox})$ and $C_{inv}(K_{S\,Ext}, K_{D\,Ext}, t_{ox})$ can be expressed in this way as

$$I_{on}(K_{S\,Ext}, K_{D\,Ext}, t_{ox})$$
$$= I_{on}(7.5, 7.5, 1.1) + (K_{S\,Ext} - 7.5) \frac{\partial I_{on}(7.5, 7.5, 1.1)}{\partial K_{S\,Ext}}$$
$$+ (K_{D\,Ext} - 7.5) \frac{\partial I_{on}(7.5, 7.5, 1.1)}{\partial K_{D\,Ext}} + (t_{ox} - 1.1) \frac{\partial I_{on}(7.5, 7.5, 1.1)}{t_{ox}}$$

$$I_{on}(K_{S\,Ext}, K_{D\,Ext}, t_{ox})$$
$$= 0.945825 - 0.0315\, K_{D\,Ext}^2 - 0.00149\, K_{D\,Ext} + 0.067\, K_{S\,Ext} - 0.115\, t_{ox}$$

And

$$C_{inv}(K_{S\,Ext}, K_{D\,Ext}, t_{ox}) = 0.144 + 0.101\, K_{D\,Ext} + 0.045\, K_{S\,Ext} - 0.002 t_{ox}$$

As we found that the performance of the FinFET based circuit is very much improved as $K_{S\,Ext}$ is improved. For analyzing the performance, we took typical value of $K_{D\,Ext} = 7.5$ and for easiness and reduced gate leakages we took $t_{ox} = 2$nm. With these values, the expression for I_{on} and C_{inv} as a function of $K_{S\,Ext}$ is given by following expressions –

$$I_{on}(K_{S\,Ext}) = -1.067225 + 0.067\, K_{S\,Ext}$$

and

$$C_{inv}(K_{S\,Ext}) = 0.8975 + 0.045\, K_{S\,Ext}$$

Performance (Delays) of a circuit basically depends on the value of I_{on}/C_{inv}, larger factor gives improved performance of the circuit. Graph of I_{on}/C_{inv} is plotted with K_s to find out the maximum value of I_{on}/C_{inv}, at which maximum performance in terms of circuit speed is achieved (Figure 5.49).

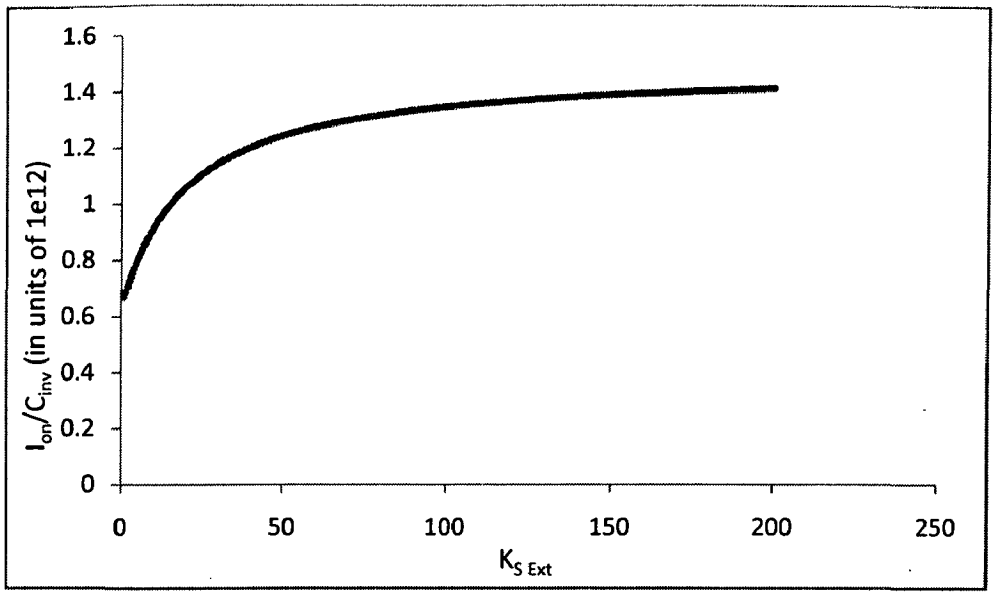

Figure 5.49: I_{on}/C_{inv} with $K_{S\ Ext}$.

Discussion

With Figure 5.49 it is apparent that with a fixed value of t_{ox} and $K_{D\ Ext}$ (here it is 2nm and 7.5 respectively) the ratio I_{on}/C_{inv} increases, which is proportional to the performance (speed) of circuit. Thus with increasing $K_{S\ Ext}$ with fixed t_{ox} and $K_{D\ Ext}$ the circuit performance given by underlap FinFET device increase.

Figure 5.49 shows that initially performance increases linearly with increasing $K_{S\ Ext}$, after $K_{S\ Ext}$ around 30 it start saturating and the slope of curve start decreasing.

Chapter 6

Conclusions and Future Work

A thorough analysis of the scaling issues in Nano Scale FinFET devices was carried out and some new device scaling designs are proposed in this dissertation work using the Sentaurus simulation package. It was found that although the overlapped FinFET structure increases ON current (I_{on}) extensively but it also increases the subthreshold leakages I_{off} and the overall effect has made the I_{on}/I_{off} worsen. Other option for this is to use underlapped structure for further scaling FinFET devices which provides much improved I_{on}/I_{off}. Underlap and overlapped device structures were analyzed with multiple numbers of fins leading to a larger total drain current and thus can be used where a higher ON current is required, replacing the planar devices.

A FinFET based standard cell, consisting some basic circuits such as Inverter, NOR-2, NAND-2 and SR latch by NAND gate, is simulated for analyzing roles of FinFET device parameters in circuit point of view. Standard cell is simulated with & without considering, the effect of the parasitic external to FinFET device which are basically interconnect parasitic resistance and capacitance. Predictive technology model (PTM) was used for calculating values of parasitic. By mixed mode simulation of these composite external parasitics, it was observed that the external parasitics don't cause very significant change in the logic delays of the standard cell. It was the internal parasitics which dominates in case of FinFET devices. So the FinFET device is more suitable to replace the planar MOSFET devices in scenario where the external parasitics dominates, such as memory designing.

For improving the FinFET device performance, Source/Drain pad doping variation experiment was carried out. With increasing pad doping concentration, carrier mobility decreased due to increased scattering and the pad resistance reduced. It was observed that the effect of reducing pad resistance dominates while modulating pad doping causing improved I_{on}, I_{on}/I_{off}, $R_{S/D\ pad}$. It causes negligible increase in I_{off} and subthreshold slope. Circuit performance aspect of pad doping engineering is to reduce logic delays of inverter with a Fan Out 4 load.

Spacers in case of underlap FinFET device help in inverting the extension regions in ON conditions. With improving spacer dielectric constant I_{on}, I_{on}/I_{off}, inverter's input capacitance

C_{inv}, output capacitance C_p and logic delays are increased. Whereas I_{off}, extension resistances, channel resistance and subthreshold slope are decreased.

Increasing gate oxide thickness causes reduced gate control and significant decreased I_{on} in case of planar MOSFET devices. But in case of underlap FinFET, I_{on} does not decrease very significantly. Lesser decrease in I_{on} of underlap FinFET with t_{ox} increment can be understood by three transistor analogy of underlap FinFET device. Because of increased gate oxide thickness, gate capacitance decreases. Decrease in gate capacitance dominates to decrease I_{on} causing significant improvement in the circuit performance at higher dielectric constants. It was observed that by this scheme, inverter delay with fan-out 4 (FO4) load reduces by about 16% for an increase in t_{ox} from 1.1nm to 2nm and a spacer K of 7.5. We also observe that the frequency of operation of a 3-stage ring-oscillator increases by about 16% for an equal increase in t_{ox} and K=7.5 without any penalty in terms of the ring-oscillator power consumption.

Asymmetric structure design of the FinFET device with drain side 0nm overlap and source side underlap cause decrease in I_{on}, I_{on}/I_{off}; whereas I_{off} and logic delays of inverter with Fan Out 4 load is decresed. So it is not preferred to make drain side overlapped or lesser underlap to increase the circuit performance, but it is preferred on source side.

Continuing developing the asymmetric structure for FinFET, spacer dielectric constants were varied independently which shows that with increasing $K_{D\,Ext}$, parameters I_{on} and I_{off} are changed negligibly; $R_{S\,Ext}$, $R_{channel\ under\ gate}$ and C_{inv} increases; whereas $R_{D\,Ext}$ decreases and subthreshold slope decreases negligiblly. With increasing $K_{S\,Ext}$, parameters I_{on}, I_{on}/I_{off} and C_{inv} are increased; $R_{D\,Ext}$, $R_{S\,Ext}$, $R_{channel\ under\ gate}$ decrease and subthreshold slope decreases negligibly.

In this section, the dominant device parameters such as I_{on} and C_{inv} are analyzed and modeled with design parameters. In Chapter 5 it is proved that I_{on} and C_{inv} are very strongly dependent on $K_{S\,Ext}$, $K_{D\,Ext}$ and t_{ox}.

For obtaining a model for the proposed device designs for scaling underlap FinFET devices, a mathematical model was developed by using expressions for ON current and input capacitance of inverter individually with different parameters $K_{S\,Ext}$, $K_{D\,Ext}$ and t_{ox}. Then by using Taylor series for three variables, these individual expressions are combined to get the composite expression for I_{on} and C_{inv} as a composite function of $K_{S\,Ext}$, $K_{D\,Ext}$ and t_{ox}. The speed of a circuit is directly proportional to input capacitance of load device and inversely proportional to drive

current. So the performance of underlap FinFET can be considered to be directly proportional to the ratio I_{on}/C_{inv}.

With this relation, we prove our proposed device scaling methods and also get a model to get the values of device design parameters corresponding to the point of maximum circuit performance.

This work will be further extended to propose a scaling methodology using this new proposed device design for scaling underlap FinFET device.

REFERENCES

1. International Technology Roadmap for Semiconductors, Semiconductor Industry Association (SIA) 2003.
2. S. Thompson, P.Packan, and M.Bohr, "MOS scaling: Transistor challenges for the 21st century," *Intel Tech. J.*, vol.Q3, pp. 1-19, 1998.
3. D.Hisamoto, W.-C. Lee, J.Kedzierski, H.Takeuchi, K.Asano, C.Kuo, E.Anderson, T.-J. King, J. Bokor, C. Hu, "FinFET- A Self-Aligned Double- Gate MOSFET Scalable to 20nm," *IEEE Transactions on Electron Devices*, vol.47, pp. 2320-2325, Dec.2000.
4. X.Huang, W.-C. Lee, C.Kuo, D.Hisatomo, L.Chang, J.Kedzierski, E.Anderson, H.Takeuchi, Y.-K.Choi, K.Asano, V.Subramanian, T.-J. King, J.Bokor, and C.Hu, "Sub-50nm FinFET: PMOS," in *IEDM Tech. Digest*, pp. 67-70, 1999.
5. S.H. Tang, L.Chang, N.Lindert, Y-K. Choi, W-C. Lee, X. Huang, V. Subramanian, T-J. King, J Bokor and C. Hu, "FinFet-a quasi-planar double-gate MOSFET" in Proc. *Int. Solid-State Circuits Conf. (ISSCC)*, pp. 118- 119, 2001.
6. H.-S. P. Wong, "Beyond the conventional transistor," *IBM J. Res. Dev.*, vol. 46, no. 2/3, pp. 133-168, 2002.
7. H. Moravec, "Robot: Mere Machine to Transcendent Mind", Oxford Univ. Press, Inc., 1998.
8. R. N. Noyce, "Semiconductor device-and-lead structure." U.S. Patent #2,981,877, issued Apr. 25, 1961.
9. J.S Kilby, "Miniaturized electronic circuits," U.S. Patent #3,138,743, issued June 23, 1964.
10. F. M. Wanlass and C. T. Sah, "Nanowatt logic using field-effect metal-oxide semiconductor triodes," *IEEE Int'l Solid-State Circuits Conf.*, pp.32-33, 1963.
11. P. Chatterjee, "ULSI-Market Opportunities and Manufacturing Challenges," *IEDM Tech. Digest*, pp. 11-17, 1991.
12. G.E Moore, "Progress in digital integrated electronics," *IEDM Tech. Digest*, vol. 21, pp. 11-13, Dec. 1975.
13. International Technology Roadmap for Semiconductors, 2001. Available online: http://public.itrs.net/.

14. A. James Hutchby, Victor Zhirnov, Ralph Cavin, George Bourianoff, "CMOS Devices and Beyond – A Process Integration Perspective," *International Conference on Characterization and Metrology for ULSI Technology*, vol. 683, pp. 74-80 2003.
15. P. Packan, "Pushing the Limits," *Science*, vol. 285, pp. 2079, 1999.
16. B. Hoeneisen and C. A. Mead, "Fundamental Limitations in Microelectronics-I MOS Technology," *Solid State Electronics*, vol. 15, pp. 819-829, 1972.
17. J. Meindl, "Low Power Microelectronics-Retrospect and Prospect," *Proc. IEEE*, vol. 83, no. 4, pp. 619-635, 1995.
18. S. Asai and Y. Wada, "Technology Challenges for Integration Near and Below 0.1 micrometer," *Proc. IEEE*, vol. 85, pp. 505-520, 1997.
19. Y. Taur, D. Buchanan, W. Chen, D. Frank, K. Ismail, S. H. Lo, G. Sai-Halasz, R. Viswanathan, H.-J. C. Wann, S. Wind, H.-S. Wong, "CMOS Scalinginto the nanometer regime," *Proc. IEEE*, vol. 85, pp. 486-504, 1997.
20. H.-S. P. Wong, D. Frank, P. M. Solomon, H.-J. Wann, and J. Welser, "Nanoscale CMOS," *Proc. IEEE*, vol. 87, pp. 537-570, 1999.
21. D. Frank, R. Dennard, E. Nowak, P. Solomin, Y. Taur, and H.-S. Wong, "Device Scaling Limits of Si MOSFETs and Their Application Dependencies," *Proc. IEEE*, vol. 89, pp. 259-288, 2001.
22. R. W. Keyes, "Fundamental Limits of Silicon Technology," *Proc. IEEE*, vol. 89, pp. 227-239, 2001.
23. J. Plummer and P. Griffin, "Material and Process Limits in Silicon VLSI Technology," *Proc. IEEE*, vol. 89, pp. 240-258, 2001.
24. James B.Kuo, S.C. Lin, "Low-Voltage SOI CMOS VLSI Devices and Circuits" *JOHN WILEY & SONS, INC*, 2001.
25. T. Drake, Z.Cheng, J.L.Hoyt, E.Fitzgerald and D.A. Antoniadis, "Ultra-thin Strained Silicon on Insulator MOSFET", SRC and MARCO, 2003.
26. R.Chau, J.Kavalieros, B.Roberds, A.Murthy, B.Doyle, D.Barlage, M.Doczy, and R.Arghavani, "A 50nm depleted-substrate CMOS transistor (DTS)," *IEDM Tech. Digest*, pp. 621-623, 2001.

27. B.Doyle, B.Boyanov, S.Datta, M.Doczy, S.Hareland, B.Jin, J.Kavalieros, T.Linton, R.Rios and R.Chau, "Tri-Gate Fully-Depleted CMOS Transistors: Fabrication, Design and Layout," *Symp.VLSI Tech. Dig.*, pp. 133- 134, June 2003.
28. J.G. Fossum, J.-W. Yang and V.P. Trivedi, "Suppression of Corner Effects in Triple-Gate MOSFETs," *IEEE Electron Device Letters*, vol. 24, no.12, pp. 745-747, Dec. 2003.
29. J.T. Park, J.P. Colinge, and C.H. Diaz, "Pi-gate SOI MOSFET," *IEEE Electron Device Lett.*, vol.22, pp. 405-406, Aug.2001.
30. F.-L. Yang, H.-Y. Chen, F.-C.Chen, C.-C. Huang. C.-Y Chang, H.-K Chiu, C.-C. Lee, C.-C Chen, H.-T. Huang, C.-J. Chen, H.-J Tao, Y.-C. Yeo, M.S. Liang and C. Hu, "25 nm CMOS Omega FETs," *IEDM Tech. Digest*, pp. 255, 2002.
31. 18 H. Takato et. al., "Impact of surrounding gate transistor (SGT) for ultra-high density LSI's", *IEEE Trans. Electron Devices,* vol. 38, no. 3, pp. 573-578, Mar. 1991.
32. J.P. Colinge, M.H. Gao, A. Romano-Rodriguez, H.Maes, and C.Claeys, "Silicon-on-Insulator gate-all-around device," *IEDM Tech. Digest*, pp. 595-598, 1990.
33. J.T. Park and J.P.Colinge, "Multiple-Gate SOI MOSFETs: Device Design Guidelines," *IEEE Transactions Electron Devices*, vol.49, no.12, pp. 2222-2229, Dec.2002.
34. Oliver Hayden, Ritesh Agarwal and Wei Lu, "Semiconductor nanowire devices," *Nanotoday*, vol. 3, no. 5-6, pp. 12-22, Oct-Dec 2008.
35. C.H. Wann, K.Noda, T.Tanaka, M.Yoshida, and C.Hu, "A comparative study of advanced MOSFET concepts," *IEEE Trans. Electron Devices*, vol. 43, no.10, pp. 1742-1753, Oct. 1996.
36. N. Lindert, L. Chang. Yang-Kyu Choi E.H. Anderson, Wen-Chin Lee, Tsu-Jae King, J. Bokor and Chenming Hu , "Sub-60-nm Quasi-Planar FinFETs Fabricated Using a Simplified Process," *IEEE Electron Device Letters*, vol. 22, pp. 487–489, 2001.
37. Xuejue Huang, Wen-Chin Lee, Charles Kuo, D. Hisamoto, Leland Chang, J Kedzierski, E. Anderson, H. Takeuchi, Yang-Kyu Choi, K.Asano, V. Subramanian, Tsu- Jae King, J. Bokor and Chenming Hu "Sub 50-nm FinFET: PMOS," *IEDM Tech. Digest*, pp. 67, 1999.
38. Sentaurus Device User Guide, Version: A-2007.12, Synopsys Inc.
39. J. W. Slotboom and H. C. de Graaff, "Measurements of Bandgap Narrowing in Si Bipolar Transistors," *Solid-State Electronics*, vol. 19, no. 10, pp. 857–862, 1976.

40. G. Masetti, M. Severi, and S. Solmi, "Modeling of Carrier Mobility Against Carrier Concentration in Arsenic-, Phosphorus-, and Boron-Doped Silicon," *IEEE Transactions on Electron Devices*, vol. ED-30, no. 7, pp. 764–769, 1983.
41. C. Canali, G. Majni, R. Minder and G. Ottaviani, "Electron and Hole Drift Velocity Measurements in Silicon and Their Empirical Relation to Electric Field and Temperature," *IEEE Transactions on Electron Devices*, vol. ED-22, no. 11, pp. 1045–1047, 1975.
42. C. Lombardi, S. Manzini, A. Saporito, and M. Vanzi, "A Physically Based Mobility Model for Numerical Simulation of Nonplanar Devices," *IEEE Transactions on Computer-Aided Design*, vol. 7, no. 11, pp. 1164–1171, 1988. *ESPRIT-6075 Project (DESSIS), Period 1, May 27 – November 26, 1992*, Six-Month Report, University of Bologna, Bologna, Italy, 1992.
43. A. Bringer and G. Schön, "Extended moment equations for electron transport in semiconducting submicron structures," *Journal of Applied Physics*, vol. 64, no. 5, pp. 2447–2455, 1988.
44. M. A. Stettler, M. A. Alam, and M. S. Lundstrom, "A Critical Examination of the Assumptions Underlying Macroscopic Transport Equations for Silicon Devices," *IEEE Transactions on Electron Devices*, vol. 40, no. 4, pp. 733–740, 1993.
45. K. M. Cao, W. C. Lee, W. Liu, X. Jin, P. Su, S. K. H. Fung, J. X. An, B. Yu, and C. Hu, "BSIM4 gate leakage model including source-drain partition," *IEDM Tech. Digest*, pp. 815–818, Dec. 2000.
46. Schenk and G. Heiser, "Modeling and simulation of tunneling through ultra-thin gate dielectrics," *Journal of Applied Physics*, vol. 81, no. 12, pp. 7900–7908, 1997.
47. M.G. Ancona, H.F. Tiersten, "Macroscopic physics of the silicon inversion layer", *Phys. Rev. B*, vol. 35, pp. 7959, 1987.
48. A. Ortiz-Conde, F. J. Garcia Sanchez, J. J. Liou, A. Cerdeira, M. Estrada, Y. Yue, "A review of recent MOSFET threshold voltage extraction methods", *Microelectronics Reliability*, vol. 42, no. 4-5, pp. 583-596, April-May 2002.
49. D. S. Havaldar, G. Katti, N. DasGupta and A. DasGupta, "Subthreshold current model of FinFETs based on analytical solution of 3-D Poisson's equation," *IEEE Transactions on Electron Devices*, vol. 53, no. 4, pp. 737-742, April 2006.

50. H.-S. P. Wong, K. K. Chan, and Y. Taur, "Self-aligned (top and bottom) double-gate MOSFET with a 25 nm thick silicon channel," *IEDM Tech. Digest*, pp. 427- 430, Dec. 1997.

51. X. Huang, W.-C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y.-K. Choi, K. Asano, V. Subramanian, T.-J. King, J. Bokor, and C. Hu, "Sub-50 nm p-channel FinFET," *IEEE Trans. Electron Devices*, vol. 48, no. 5, pp. 880–886, May 2001.

52. S. A. Tawfik, V. Kursun, "Multi-Threshold Voltage FinFET Sequential Circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. PP, issues 99, pp. 1, Sept. 2009.

53. Jin-Woo Han, Choong-Ho Lee, Donggun Park, and Yang-Kyu Choi, "Extraction Method of Source and Drain to Gate Overlap Length in Thin-Body FinFETs", *The 14th Korean Conference on Semiconductors (KCS)*, pp. 619-620, Jeju, Korea, Feb. 8-9, 2007.

54. V. Trivedi, J. G. Fossum, and M. M. Chowdhury, "Nanoscale FinFETs with gate–source/drain underlaps," *IEEE Trans. Electron Devices*, vol. 52, no. 1, pp. 56–62, Jan. 2005.

55. J. Kedzierski, M. Ieong, E. Nowak, T. S. Kanarsky, Y. Zhang, R. Roy, D. Boyd, D. Fried, and H.-S. P.Wong, "Extension and source/drain design for high-performance FinFET devices," *IEEE Trans. Electron Devices*, vol. 50, no. 4, pp. 952–958, Apr. 2003.

56. Predictive technology model (PTM) Available online: http://ptm.asu.edu/

57. H. Iwai, "Roadmap for 22 nm and beyond (Invited Paper)", *Microelectronic Engineering*, vol.86, no. 7-9, pp. 1520-1528, July-September 2009.

List of Publications

Based on this dissertation work two papers are submitted. Details of these are as follows:

Paper Title	**Journal / Conference**
1. A Novel Scaling Strategy for Underlap FinFETs	International Conference on Communications, Computers & Devices, IIT Kharagpur, Dec. 10 - 12, 2010.
2.An Optimized Device Design for Underlap FinFETs	IEEE Electron Device Letters