VERTICAL SILICON NANOWIRE GATE ALL AROUND FIELD EFFECT TRANSISTOR BASED NANOSCALE CMOS

A DISSERTATION

Submitted in partial fulfillment of the requirements for the award of the degree of

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ELECTRONICS AND COMMUNICATION ENGINEERING

(With Specialization in Semiconductor Devices & VLSI Technology)

By

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CANDIDATE'S DECLARATION

I hereby declare that the work, which is being reported in this dissertation report, entitled **"Vertical Silicon Nanowire Gate All Around Field Effect Transistor Based Nanoscale CMOS"**, is being submitted in partial fulfillment of the requirements for the award of the degree of **Master of Technology** in **Semiconductor Devices and VLSI Technology**, in the Department of Electronics and Computer Engineering, Indian Institute of Technology, Roorkee is an authentic record of my own work, carried out from June 2009 to June 2010, under guidance and supervision of **Dr. Sanjeev Manhas**, Assistant Professor, Department of Electronics and Computer Engineering, Indian Institute of Technology, Roorkee.

The results embodied in this dissertation have not submitted for the award of any other Degree or Diploma.

Date : 29/06/10
Place : Roorkee

Satish
Maheshwaram Satish

CERTIFICATE

This is to certify that the statement made by the candidate is correct to best of my knowledge and belief.

Date : 29/6/10
Place : Roorkee

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Maheshwaram Satish

M. Tech. (SDVT)

List of Abbreviations

Abbreviation	Meaning
NW	Nanowire
GAA	Gate All Around
FET	Metal Oxide Semiconductor Field Effect Transistor
CMOS	Complementary MOS
TCAD	Technology Computer Aided Design
SS	Subthreshold-slope
DIBL	Drain Induced Barrier Lowering
SWVI	Single Wire Vertical CMOS Inverter
TWVI	Two Wire Vertical CMOS Inverter
GUI	Graphical User Interface
SPR	Simple process representation
SPROCESS	Sentaurus Process simulator
SDE	Sentaurus Structure Editor
SDEVICE	Sentaurus Device Simulator
SOI	Silicon On Insulator
DGSOI	Double gate SOI
HDP	High density Plasma
SEM	Scanning Electron Microscope
S/D	Source/Drain
SWTG	Single Wire Transmission Gate
TWTG	Two Wire Transmission Gate
FPGA	Field Programmable Gate Array

ABSTRACT

The nanowire (NW) gate-all-around (GAA) Metal Oxide Semiconductor Field Effect Transistor (MOSFET) have potential to enable the Complementary MOS (CMOS) downscaling beyond the roadmap that is, for deca-nanometer channel lengths. It has minimum short channel effects and eliminated the requirement to scale gate dielectric thickness with channel length scaling thereby reducing the leakage currents in the device. The nanowire devices, which are obtained by the top-down approach, are preferred over the bottom-up approach for being CMOS compatible and allowing precise control over the location of devices on substrate and circuit fabrication. Further, these devices have an added advantage of occupying least Silicon area on wafer because of its vertical pillar structure.

In order to reduce the costs and speed up the research and development of new devices and circuits, the Technology Computer Aided Design (TCAD) software packages are proving to be very useful. Hence these tools have been used to carry out an extensive scaling study on Vertical Silicon NW GAAFET 3D device structures.

The simulation results show that that these devices have best gate control over the channel electrostatics owing to near ideal subthreshold-swing (SS) of 60mV/decade at room temperature, Drain Induced Barrier Lowering (DIBL) < 50mV/V and a high I_{on}/I_{off} ratio ($\sim 10^6$). In this work, a Two Wire Vertical CMOS Inverter (TWVI) obtained by combination of matched n and p NW GAAFET is proposed and simulated. Along with TWVI, we also propose a Single Wire Vertical CMOS Inverter (SWVI) structure as an enhancement to TWVI. The device matching principle used for TWVI led to implementation of dual diameter SVI. However, dual diameter SWVI approach shows severe impact of source pad and nanowire resistance. Thus, a single diameter SWVI is implemented to address source/drain resistance issue. The benchmarking of vertical CMOS with FinFET based inverter shows that the single diameter SWVI offers up to 80 % reduction in layout area and nearly 70 % reduction in power at the cost of 40% increase in delay.

The results show that these vertical devices have very high potential for use in ultra-low power applications and offers best overall performance for deca-nanoscale CMOS. As further extension of the work a transmission gate can be implemented by modifying the layout of SWVI structure. This will be of greater advantage as reconfigurable interconnects, where logic gates can be build in interconnects chain (pass transistor, inverter and transmission gate).

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CHAPTER 1

Motivation of the thesis

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1.1 Introduction

The scaling of the device dimension has continued to follow the Moore's law [1] for more than 40 years. The CMOS device architecture has induced new ideologies such as lighly doped drain implantation, lateral non-uniformity in channel doping, reduction in junction-depth, halo implants etc, in addition to these stressors have been introduced to better mobility [2]. These improvements are good enough to keep the technology in pace with the roadmap. For deca-nanometer and beyond technology nodes the novel devices with 3D structures (Double Gate FET, Fin-FET, Nanowire (NW) Gate-all-around (GAA) FET) are being researched for future replacement of planar MOSFET devices.

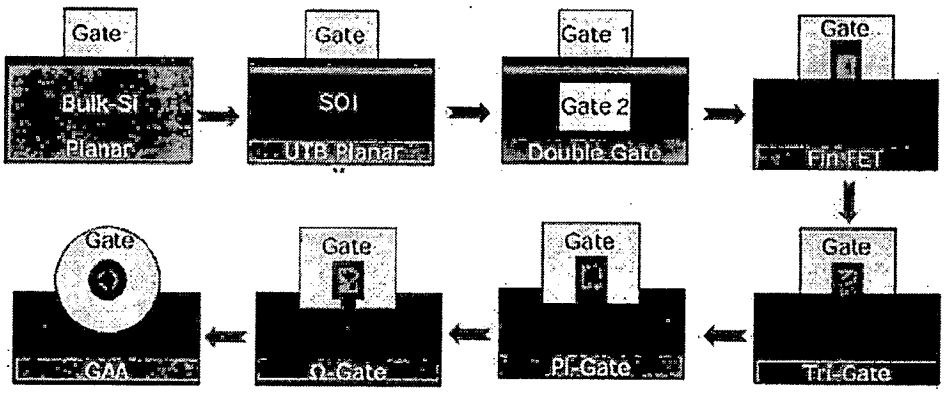

Figure 1.1 Progression of device structure from single-gated planar to fully GAA NWFET

Figure 1.1 shows that these novel devices have evolved as multiple-gate structures with better electrostatic control [4]. Consider the Double Gate FET which has the following salient features 1) control of short-channel effects by device geometry, as compared to bulk FET because of presence of two gates; 2) a thin silicon channel leading to tight coupling of the gate potential with the channel potential. These features provide the advantage of 1) reduced short-channel effects leading to a shorter allowable channel length compared to bulk FET; 2) a sharper subthreshold slope (60 mV/dec compared to 80 mV/dec for bulk FET) which allows for a larger gate overdrive for the same power supply and the same off- current and 3) better carrier transport as the channel doping is reduced [2].

FinFET is considered to be the first member of vertical structures family. It is called so, since the silicon channel protrudes from the silicon wafer surface like a fin. Two types of FinFET are reported 1) a gate-first process in which the source and drain are formed after the formation (patterning) of the gate stack and 2) a gate-last (or replacement-gate) process in

which the source and drain are formed before the formation of the gate stack. The fabrication of the FinFET begins with the patterning and etching of a thin fin on an SOI substrate using a hard mask which is retained throughout the fabrication process. The drive current of FinFET devices rival those of best conventional bulk devices. Despite the unconventional device structure and topology, the minimum gate length achieved is among the shortest [2].

However, the GAA structure with its multiple gate control is the most effective for better electrostatic control of the channel charge and is resistant to short-channel effects [5]. One of the important problems of planar CMOS is the shrinking gate oxide thickness which causes increase in tunneling leakage whereas in NW GAAFET the gate length can be scaled with wire diameter without reducing the gate dielectric thickness [6]. Based on the fabrication approach the nanowire structure can be classified into two types 1) the bottom–up approach and 2) the top–down approach [5].

The bottom up approach is basically a non-lithographic method. Vapor-liquid-solid mechanism using suitable catalyst and molecular beam epitaxy can produce very thin nanowires. However, nanowires thus produced are randomly distributed and additional processing steps are required to assemble them into functional devices. The top-down approach which is a CMOS compatible process can be further classified into 2 types of structures based upon the nanowire orientation 1) vertical pillar type and 2) lateral nanowire type [5].

Of the two types based on nanowire orientation, the lateral nanowire type follows process steps similar to FinFET with an additional step after the Si fin formation. This step is mainly to convert the rectangular fin structure to a cylindrical wire structure. It is achieved by first etching away a part of the buried oxide then oxidizing the fin. Then finally the oxide is etched to reveal the nanowire supported at its ends by the source/drain pads.

The vertical nanowire structure follows different process steps than used for lateral nanowire device. The foremost step involves vertical pillar structure formation by selective deep etching of Silicon against hard mask resist dots. The substrate acts as source, the top part of nanowire acts as drain and channel in between them. The gate around the nanowire channel is obtained by special processing step. In this thesis work vertical silicon nanowire gate all around FET (NW GAAFET) has been studied whose structure and process steps are proposed by Yang et al., [7].

1.2 Motivation

Of all the 3D device structures discussed in previous section the Vertical NW GAAFET occupies the least Silicon wafer area. Thus these devices can be used to obtain ultra dense integrated circuits.

There is also possibility of introducing logic functions in the interconnect layers; in principle allowing fabrication of vertical transistors in vias, a step towards reconfigurable interconnect. There is also the promise of adding functionality on top layer beyond ICs, such as chemical or bio sensors, mechanical nano-actuators and embedded solar cells to provide power directly to the circuits [8].

These advantages of vertical nanowire devices have motivated us in carrying out channel length scaling study and CMOS inverter implementation. The work has been extensively carried out on Sentaurus TCAD (version 2009.10) a virtual fabrication and characterization software package supplied by Synopsys Inc.

1.3 Objectives

The following objectives have been successfully achieved in this thesis:

- Channel length scaling study of n/p Vertical Si NW GAAFET
- Effect of nanowire diameter on device characteristics
- n/p device matching for CMOS inverter implementation.
- Implement two different configurations of CMOS inverter: two wire vertical CMOS inverter (TWVI) and single wire vertical CMOS inverter (SWVI).
- Benchmarking study of NW GAAFET with bulk MOSFET, FinFET.

1.4 Thesis Organization

Chapter 2 deals with basic understanding on different tools available in Sentaurus TCAD software package which are used in the thesis implementation.
Chapter 3 presents a brief overview of scaling theory for Silicon MOSFET's: Bulk to GAA.
In chapter 4, the 3D structural details of NW GAAFET are presented along with the simulation results of channel length scaling and varying the nanowire diameter, matched n and p FET devices for CMOS inverter.

Chapter 5 presents the two wire vertical CMOS inverter (TWVI) configuration and its comparison with the proposed single wire vertical CMOS inverter (SWVI) configuration with single diameter and dual diameter wire.

Finally, conclusions and recommendations for future work are outlined in chapter 6.

CHAPTER 2

Sentaurus TCAD

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2.1 Technology Computer Aided Design

The semiconductor industry needs to run costly and time-consuming wafer tests when developing and characterizing a new semiconductor device or technology. As the technologies become more complex, the semiconductor industry has developed virtual fabrication tools to run computer simulations in order to cut costs and speed up the research and development process. These computer applications are known as Technology CAD (TCAD) tools.

TCAD simulation tools solve fundamental, physical partial differential equations, such as diffusion and transport equations for discretized geometries, representing the silicon wafer or the layer system in a semiconductor device. This deep physical approach gives TCAD simulation predictive accuracy. In addition, semiconductor manufacturers use TCAD for yield analysis that is, monitoring, analyzing, and optimizing their IC process flows, as well as analyzing the impact of IC process variation.

Sentaurus TCAD a Synopsys Inc. product is extensively used in this dissertation work. TCAD consists of two main branches: process simulation and device simulation [9].

2.2 Process Simulation

In process simulation, processing steps such as etching, deposition, ion implantation, thermal annealing and oxidation are simulated based on physical equations, which govern the respective processing steps. The simulated part of the silicon wafer is discretized (meshed) and represented as a finite-element structure as shown in Figure 2.1.

For example, in the simulation of thermal annealing, complex diffusion equations for each dopant species are solved on this mesh. For oxidation simulations, the growth of the silicon di oxide is simulated taking into account the oxygen diffusion, the mechanical stresses at corners, and so on.

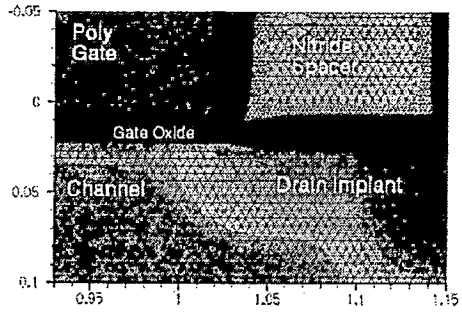

Figure 2.1 Magnification of gate-drain corner of an NMOSFET with finite-element grid.

The different tools required for process simulation are:

2.2.1 Ligament

The Ligament software package provides a convenient graphical user interface (GUI) for process simulation. The input to Ligament includes process flows, process libraries, layouts, and other TCAD-related information. The output is process command files to be used by the target process simulator. The tools included in the package are: Ligament Flow Editor, Ligament Layout Editor, and Ligament Translator.

The **Ligament Flow Editor** is used to create and edit process flows. It allows users to assemble a process flow from macros. It uses the simple process representation (SPR) language, which is independent of the language requirement of any particular process simulator. The **Ligament Layout Editor** is used to create and edit layouts. Its main purpose is to serve as an interface between EDA layout tools and TCAD, such as defining 1, 2 or 3D simulation domains. The **Ligament Translator** translates the language native to the Ligament tools, that is, the SPR language, to the language that can be recognized by the target simulator (SProcess, Dios, TSUPREM-4).

2.2.2 Sentaurus Process

Sentaurus Process (SProcess) is a complete and highly flexible, multidimensional, process modeling environment. With its modern software architecture, it constitutes a new tool generation and a solid base for process simulation. Calibrated to a wide range of the latest experimental data using proven calibration methodology, Sentaurus Process offers unique predictive capabilities for modern silicon and nonsilicon technologies.

2.2.3 Sentaurus Structure Editor

An alternate tool is available in Sentaurus TCAD known as Sentaurus Structure Editor (SDE) which is a structure editor for 2D/ 3D device structures. It has three distinct operational modes: 2D structure editing, 3D structure editing, and 3D process emulation.

From the GUI, 2D and 3D device models are created geometrically, using 2D or 3D primitives, such as rectangles, polygons, cuboids, cylinders, and spheres. Rounded edges are generated by filleting, 3D edge blending, and chamfering. Complex shapes are generated by simply intersecting primitive elements. Along with this, it has provision to define doping profiles, mesh strategy and contacts.

In process emulation mode (Procem), SDE translates processing steps, such as etching and deposition, patterning, fill and polish, into geometric operations.

In this thesis work the 3D structure editing operation mode in SDE has been used extensively to create 3D structures of NWFET devices. The details of which are discussed in chapter 3 and 4.

2.3 Device Simulation

Device simulations can be thought of as virtual measurements of the electrical behavior (I-V, C-V, static and dynamic), thermal and optical characteristics of semiconductor devices or circuits. The device is represented as a meshed finite-element structure. Each node of the device has properties associated with it, such as material type and doping concentration. For each node, the carrier concentration, current densities, electric field, generation and recombination rates, and so on are computed (as shown in Figure 2.2).

Electrodes are represented as areas on which boundary conditions, such as applied voltages, are imposed. The device simulator solves the Poisson equation and the carrier continuity equation (and possibly other equations). After solving these equations, the resulting electrical currents at the contacts are extracted (as shown in Figure 2.3).

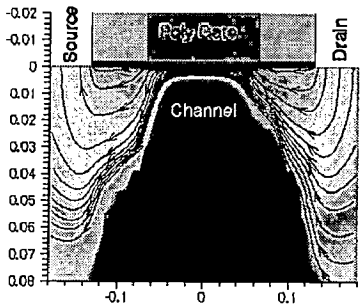

Figure 2.2 Current flow lines in a 0.13 μm NMOSFET at V_{gs} = 1.5 V and V_{ds} = 3.0 V; shading represents current density.

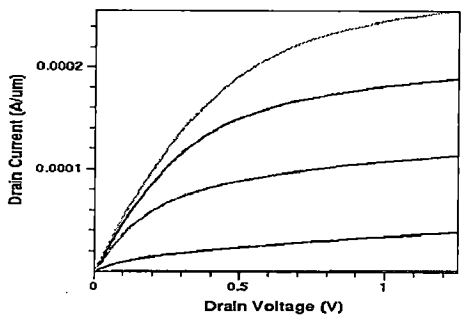

Figure 2.3 Drain current as function of drain voltage for a 130 nm NMOSFET at different V_{gs}.

2.3.1 Sentaurus Device

Sentaurus Device (SDevice) is a comprehensive semiconductor, device simulator framework capable of simulating the electrical, thermal, and optical characteristics of silicon-based and compound semiconductors. Figure 2.4 shows a typical flow diagram of the input and output files for SDevice.

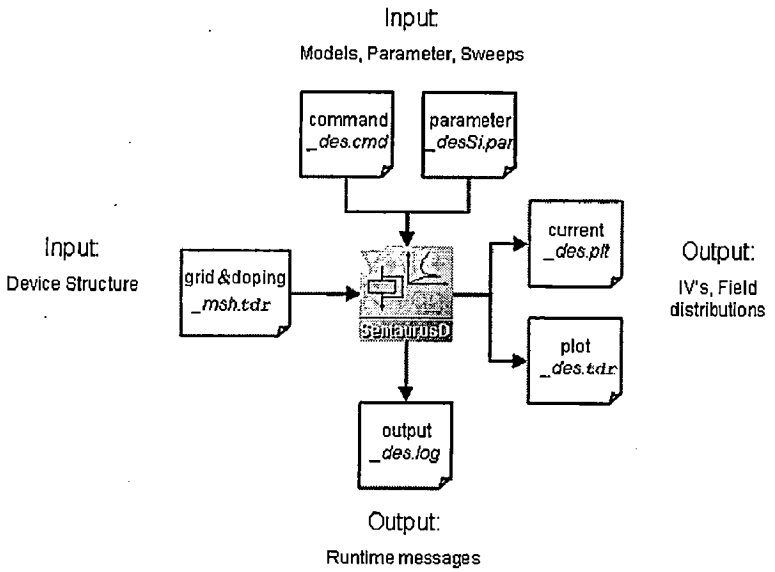

Figure 2.4 Flow of input and output files in Sentaurus Device.

The following sections are to be included in the input command file (with extension _des.cmd) which is used for running the simulation:

File Section

This consists of the input files, the grd file (_msh.grd) is the device geometry, including the regions and materials of the device, the locations of the contacts, and the mesh points, including the location of all the discrete points, also called nodes or vertices. The doping profile file (_msh.dat) obtained after meshing the structure with mesh engine and an optional Parameter file (.par) with user-defined model parameters which supersede the SDevice built-in defaults.

The SDevice simulation produces many output files: the Current file (_des.plt) contains the electrical output data, such as currents, voltages, and charges at each of the contacts. The Output file (_des.log) contains all the informative texts that Sentaurus Device has downloaded during a run, including the physical models that have been activated and the parameter values that have been used. This file also contains error messages. The Plot file

(_des.tdr) contains the final spatial solution for all variables of the structure, for example, the electron distribution at the final bias point.

Electrode Section

The electrical (or thermal) contacts of the device, together with their initial bias conditions, are defined in the Electrode section. If there is a special boundary condition for a contact, it can be defined here. Each electrode defined here must match exactly (case sensitive) an existing contact name in the structure file and only the contacts that are named in the Electrode block are included in the simulation.

Physics Section

In this section, physical models to be used in the simulation are declared. Example models include the carrier mobility model, the band-gap narrowing model, the carrier generation and recombination model, the impact ionization model, and the gate leakage model. For the simulations I have considered the classical device model (QCvanDort) to be applied for device. For carrier mobility the high field saturation model, enormal model and PhuMob models are applied. It also includes the SRH generation-recombination and Band2Band tunneling models in recombination part. And for Silicon - Oxide interface Fowler Nordheim and Direct tunneling are included in gate current calculations.

Plot Section

This includes the different device parametric values which are to be saved at the end of simulation such as density, mobility, velocity, current (e or h) etc.

Math Section

It includes the different mathematical algorithms which are to be used to control the numeric solver in the simulation. For example include AvalDerivatives algorithm when considering AvalancheGeneration in physics section.

Solve Section

It consists of statements for solving the coupled Poisson, coupled Poisson electron hole and the quasi-stationary blocks. These quasi-stationary blocks are used to bias a terminal with voltage or current value and also to sweep voltage or current at a terminal. At each simulation point, the Poisson equation and carrier continuity equations are solved self-consistently in a single Newton solver.

2.4 Plotting and Analysis Tools

The device structures shown in Figure 2.1 and 2.2 are visualized using the **Tecplot SV** tool. In addition, it can extract slices of data along the coordinate axes or user-defined lines of a 2D device, obtain 2D cross sections of 3D devices, and perform mathematical operations on the extracted data. Either the .tdr file or the .dat and .grd files together are required to be loaded to view the device.

The device characteristics (_des.plt) obtained after device simulation shown in Figure 2.3 can be viewed in Tecplot SV (XY mode) or using **Inspect** a plotting and analysis tool for XY data such as 1D doping profiles and terminal characteristics. In inspect one can obtain some of the parametric values such as V_{th}, G_m max, Ron, Vecvalx, Vecvaly etc which are available as predefined macros or use the scripting language and library of mathematical functions to compute using curve data, and to manipulate and extract data from simulations. Using the inspector option one can manually find the difference between 2 data points and also the slope (inverse slope) between points. This is useful for subthreshold-swing extraction.

CHAPTER 3

Scaling Theory of Si MOSFET Bulk to Gate-All-Around

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3.1 Scaling of Si Bulk MOSFET [10]

With the scaling of the Si MOSFET the requirements on subthreshold leakage control force conventional scaling to use high doping as the device dimension penetrates into the deep-submicrometer regime, leading to undesirable large junction capacitance (Region I in Figure 3.1) and degraded mobility. At the same time, reliability constraints have led to reductions in the power supply voltage. The combination of high channel doping and capacitance, increased threshold voltage, and reduced supply voltage, imposes severe tradeoffs between standby power and circuit speed. According to Brew's formula, the effective channel length L_{eff} of the device must be larger than L_{min} in order to achieve good subthreshold behavior

$$L_{min} = A\ [\ t_j\, t_{OX}\, (w_s + w_d)^2\ ]^{1/3} \tag{3.1}$$

where the constant $A = 0.41A^{o-1/3}$.

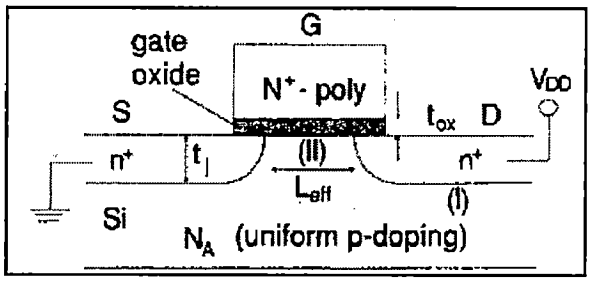


Figure 3.1 The device structure for a conventional NMOSFET. A uniform doping of N_A is assumed. Region (I) indicates the junction region, Region (II) the inversion layer.

Thus it is important to solve the problems caused by direct scaling – higher leakages, high capacitance and surface mobility degradation for deep submicron devices to work properly.

3.2 Scaling in Silicon on Insulator (SOI) devices [10]

The fully depleted SOI (FDSOI) devices eliminate the junction capacitance with the presence of buried oxide layer. Furthermore, the high channel doping can be reduced because of the additional advantage introduced by using a thin Si layer in the structure.

The electrical field profile undergoes a rapid change in the vertical (*y*) direction, and induces a large potential curvature in the lateral direction (Figure. 3.2 (c)) helping to build up the potential barrier (Figure. 3.2 (b)) needed to prevent electrons flow from the source. Therefore, one could control horizontal leakage through vertical structures.

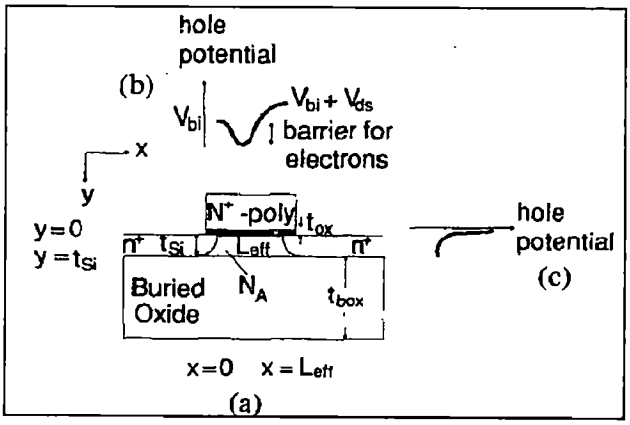


Figure 3.2 A fully-depleted SOI MOSFET in the subthreshold regime of operation. (a) Cross-section view of the structure. (b) Lateral potential distribution from source to drain. (c) Vertical potential distribution from the front gate oxide to the bottom buried oxide.

The 2D potential distribution in the Si film $\Phi(x, y)$ is governed by Poisson's equation

$$\frac{d^2\Phi}{dx^2} + \frac{d^2\Phi}{dx^2} = \frac{qN_A}{\varepsilon_{Si}} \tag{3.2}$$

where $0 \le x \le L_{eff}$ and $0 \le y \le t_{Si}$. To describe the potential distribution in the vertical direction a simple parabolic function is used

$$\Phi(x, y) \approx c_1(x) + c_2(x)\, y + c_3(x)\, y^2 \tag{3.3}$$

The boundary conditions used to obtain a nontrivial solution for (3.3) are

1) $\Phi(x, 0) = \Phi_f(x) = c_0(x)$.

2) The electric field at y = 0 is determined by the gate voltage and the oxide thickness

$$\left.\frac{d\Phi(x,y)}{dy}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{\Phi_f(x) - \Phi_{gs}}{t_{ox}} = c_1(x) \tag{3.4}$$

3) The electric field at $y = t_{si}$ is approximately zero

$$\left.\frac{d\Phi(x,y)}{dy}\right|_{y=t_{Si}} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{\Phi_{bs} - \Phi_b(x)}{t_{box}} = c_1(x) + 2t_{Si}c_2(x) \approx 0 \tag{3.5}$$

Using these boundary conditions, we transform $\Phi(x, y)$ to the following expression in which the function $\Phi_f(x)$ is to be solved:

$$\Phi(x,y) = \Phi_f(x) + \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{\Phi_f(x) - \Phi_{gs}}{t_{ox}} y - \frac{1}{2t_{Si}} \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{\Phi_f(x) - \Phi_{gs}}{t_{ox}} y^2 \tag{3.6}$$

A simpler equation is obtained by substituting (3.5) into (3.2) and setting y = 0

$$\frac{d^2\Phi_f(x)}{dx^2} - \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{\Phi_f(x) - \Phi_{gs}}{t_{ox}t_{Si}} = \frac{qN_A}{\varepsilon_{Si}} \tag{3.7}$$

Once $\Phi_f(x)$ is determined, the whole $\Phi(x, y)$ can be obtained by using (3.3). The following transformations are made

$$\lambda = \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{Si}\, t_{ox}} \tag{3.8}$$

and

$$\Phi(x) = \Phi_f(x) - \Phi_{gs} + \frac{qN_A}{\varepsilon_{Si}}\lambda^2 \tag{3.9}$$

which further simplifies (3.7)

$$\frac{d^2\Phi(x)}{dx^2} - \frac{\Phi(x)}{\lambda^2} = 0 \tag{3.10}$$

For these SOI devices the scaling parameter λ (natural length scale) is introduced to describe the potential distribution $\Phi(x)$ of whole structure. Note that $\Phi(x)$ differs from $\Phi_f(x)$ only by a position-independent term. Since punchthrough control-depends on the potential difference between the minimum potential in the channel and that of the source, this position-independent term does not affect this difference directly through the potential distribution, but rather indirectly through the boundary conditions as discussed below. And its effect is not as strong as λ.

Equation (3.10) is simply a second order 1D differential equation, and can be uniquely solved by specifying two boundary conditions which in our case are the potentials at the source ($x = 0$) and the drain ($x = L_{eff}$).

$$\Phi(0) = V_{bi} - \Phi_{gs} + \frac{qN_A}{\varepsilon_{Si}}\lambda^2 = \Phi_s \tag{3.11}$$

$$\Phi(L_{eff}) = V_{ds} + V_{bi} - \Phi_{gs} + \frac{qN_A}{\varepsilon_{Si}}\lambda^2 = \Phi_d \tag{3.12}$$

Solving (3.10) using (3.11) and (3.12), we have

$$\Phi(x) = \frac{\Phi_s[e^{(L_{eff}-x)/\lambda} - e^{(x-L_{eff})/\lambda}] + \Phi_d[e^{x/\lambda} - e^{-x/\lambda}]}{e^{L_{eff}/\lambda} - e^{-L_{eff}/\lambda}} \tag{3.13}$$

Although the requirements on the ratio between L_{eff} (L_G) and λ would depend on the specific application, $\alpha = L_{eff} / \lambda \approx 5\text{-}10$ is generally enough to produce reasonable subthreshold behavior. For a given λ, an increase of doping (within the range of full depletion) decreases the potential at source and drain ends, helping to reduce the minimum potential at the channel centre. However, the effect is more or less linear, and it would be more efficient to decrease λ directly. Thus, thin Si films and thin gate oxides are desirable for SOI devices in the deep-

submicrometer regime, while the doping would be mainly used to adjust the threshold voltage.

The threshold voltage of these devices is given by [10]

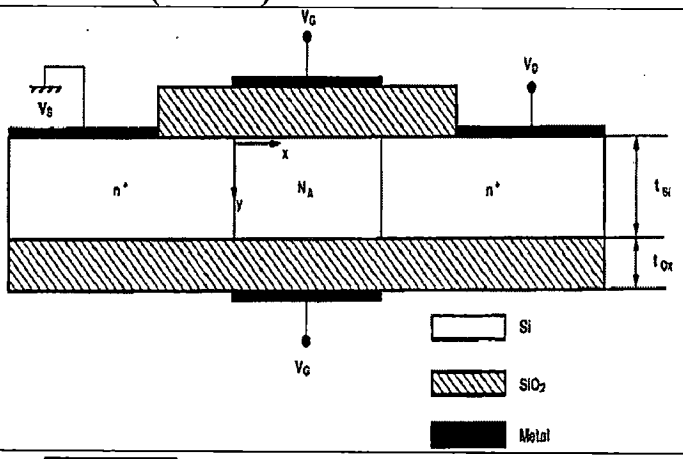
$$V_{th} \approx \frac{qN_A}{\varepsilon_{Si}}\lambda^2 + \Phi_{ms} = \frac{qN_A t_{Si} t_{ox}}{\varepsilon_{ox}} + \Phi_{ms} \qquad (3.14)$$

3.3 Scaling of Double Gate SOI (DGSOI) device [11]

In SOI structures the boundary conditions play a vital role in determining the natural scale length. If we change the structure in Figure 3.2 to the double gate structures shown in Table 3.1, the boundary conditions change, thus the natural scale length λ will also vary.

The DGSOI structure has been proposed as a way to improve the drive capability of SOI devices. Basically, the buried oxide is replaced by a gate oxide, and the same gate voltage is applied to both the top and bottom gates. The natural scale length λ is reduced through such a structure change. The threshold voltage given by Eqn 3.3 can be used for DGSOI devices by substituting the corresponding λ.

TABLE 3.1 DGSOI STRUCTURE WITH NATURAL SCALE LENGTH EXPRESSION

Structure	**Double Gate (DGSOI)**
Schematic	
Scaling parameter (λ)	$\lambda = \sqrt{\frac{\varepsilon_{Si}}{2\varepsilon_{ox}} t_{Si} t_{ox}}$

As a case study let us consider a device with a gate oxide thickness of 2 nm and Si film thickness of 10 nm, λ decreases from 7.81 nm to 5.52 nm for SOI and DGSOI respectively. Thus the DGSOI gives a 30 % improvement in λ over conventional SOI.

But it is proved by Suzuki [11] that DGSOI devices suffer from short channel effects more than expected by the Yan's model [10] given in Table 3.1. Thus the modified scale length is given by

$$\lambda = \sqrt{\frac{\varepsilon_{Si}}{2\varepsilon_{ox}}\left(1+\frac{\varepsilon_{ox}t_{Si}}{4\varepsilon_{Si}t_{ox}}\right)t_{Si}\,t_{ox}} \tag{3.15}$$

The relation between effective gate length and natural scale length of DGSOI is governed by the parameter α as

$$\alpha = \frac{L_G}{2\lambda} \tag{3.16}$$

Thus, the natural scale length, λ of DGSOI with Eqn 3.15 results in 6.55 nm. With this the minimum gate length achieved is 40 nm for the limiting case α = 3.

3.4 Scaling of Vertical Gate All Around device [12]

As mentioned in the chapter 1, the necessity to have ultra dense memories and logic chips led to the introduction of devices with novel structure. Of these the most promising one is the Gate-All-Around (Vertical Surround gate Figure 3.3) structure. It is fabricated on a cylindrical pillar of silicon, and has the benefits of both reducing the short channel effects and improving the subthreshold slope, device leakages, as well as potentially higher packing densities.

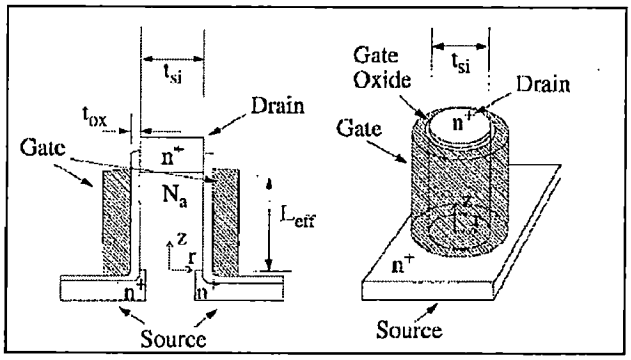


Figure 3.3 Schematic of Vertical Surround Gate MOSFET

Auth [12] has followed the same scaling principle for GAA as presented by Suzuki [11] and Yan [10] in modeling of DGSOI and FDSOI respectively.

The natural scale length of cylindrical GAA is given by the expression:

$$\lambda = \sqrt{\frac{2\varepsilon_{Si}t_{Si}^2\ln\left(1+2\frac{t_{ox}}{t_{si}}\right)+\varepsilon_{ox}t_{Si}^2}{16\varepsilon_{ox}}} \tag{3.17}$$

For the same case study with t_{ox} of 2 nm and t_{si} of 10 nm the natural scale length of GAA is obtained as 4.36 nm. This results in achieving a minimum gate length of 20 nm for $\alpha = 2.3$ the limiting case.

A plot of the minimum gate length versus the silicon thickness, t_{si}, illustrates the advantage of a cylindrical device when compared to a double gate device (Figure 3.4) with stringent conditions on SS < 70mV/dec and DIBL < 50mV/dec.

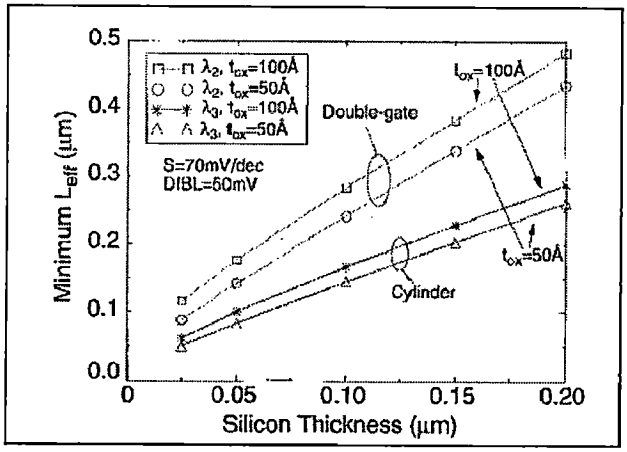


Figure 3.4 Minimum gate length versus Silicon thickness for DG and GAA MOSFET's

Thus, we can achieve desired minimum gate length device with modifications to device geometry and structure which are limited by fabrication process. This theory motivates one to consider GAAFET as replacement to address the present downscaling issue faced by Bulk MOSFET's.

CHAPTER 4

Scaling Study of Vertical NW GAAFET

Table of Contents

4.1 Introduction

Vertical Silicon Nanowire GAAFET proposed by Yang [7] is show in Figure 4.1 (a) - (f) step by step. A brief description of fabrication steps is as follows: circular resist dots of different diameters (from 160 to 600 nm) were patterned on the bulk Si wafer followed by 1-μm deep Si etch under hard mask. Pillars are then oxidized at 1150°C to convert into nanowires. The grown oxide is then stripped after vertical nanowire formation a 250-nm-thick layer of high-density plasma (HDP) oxide is deposited, followed by wet chemical etch-back. The HDP deposition resulted in thicker oxide on the bottom surface and thinner oxide along the nanowire sidewalls due to the nonconformal deposition. After wet etch-back 150-nm-thick oxide remains to cover the footing of the vertical standing wire as shown in Figure 4.1 (a). This technique separates the gate electrode from the source extension pad and, thus, reduces the gate to source fringing capacitance.

Gate oxide of 5 nm is then thermally grown on the exposed wire surface, followed by deposition of 30-nm poly-Si, which serves as the gate electrode. Gate pad is then patterned and etched under resist mask which covers the nanowire and provide a polyextension for gate contact as shown in Figure 4.1 (b). After gate pad etching, the process of HDP oxide deposition followed by wet etch back is repeated to access the polysilicon on top of nanowire while protecting the gate pad defined earlier as shown in Figure 4.1 (c). From Figure 4.1 (d) it can be observed that the exposed poly-Si is etched isotropically.

The oxide on the wafer is then completely removed in wet etching process and Arsenic is implanted. Due to thickness of the gate, a shadowing effect is anticipated at the bottom of the pillar. It is found, however that a rapid thermal annealing at 1000°C for 10 s is enough for dopants to diffuse across the shadowed region, effectively eliminating the offset in the shadowed region. Thus the structure as shown in Figure 4.1 (e) is obtained before contact formation and metallization. A standard metallization then follows to complete the fabrication process resulting in the device as shown in Figure 4.1 (f). The SEM image of the device can be seen in Figure 4.2.

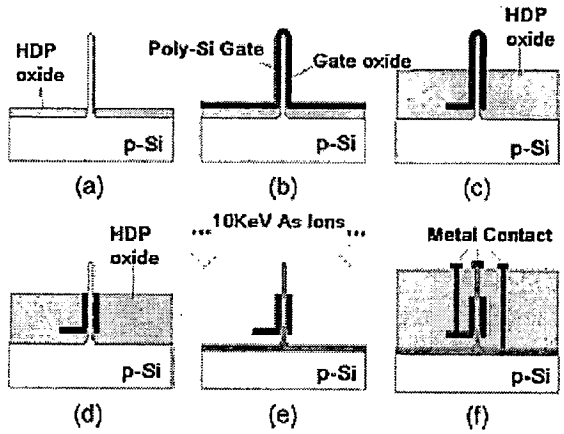


Figure 4.1 Process flow for pillar and transistor formation

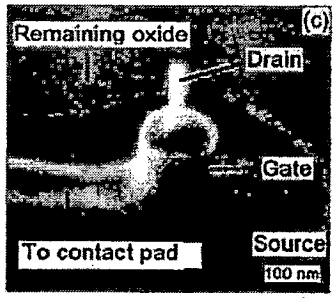


Figure 4.2 SEM image of vertical NWFET

In this thesis work the 3D structure of NW GAAFET as proposed by Yang is obtained by using the Sentaurus Structure Editor tool and is presented in the following section.

4.2 3D Structure Details of NW GAAFET

The device can be divided into 4 regions namely substrate, Si nanowire, gate (gate dielectric and gate electrode) and Aluminum metal (via's and contacts) as shown in Figure 4.3. The structure is created using the 3D shapes (cuboid, cylinder, cubical windows for selective doping and meshing), 3D edit tools for tapering, analytical doping placement, and refinement placement tool box available in SDE.

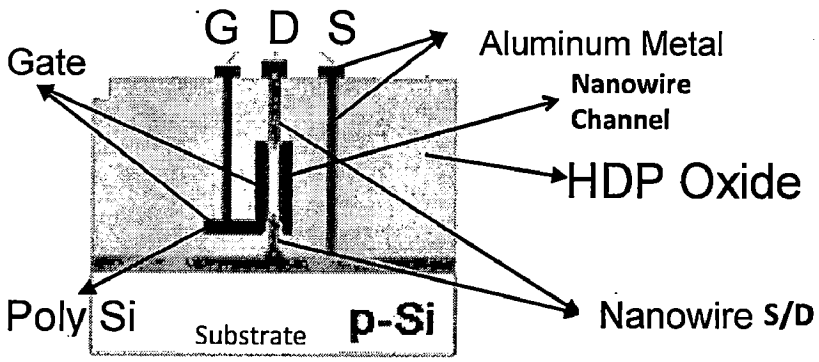


Figure 4.3 2D cut of NWFET showing the 4 regions

The n/p FET device is built on a p-doped Si substrate (10^{17} cm^{-3}) with a highly doped (n/p) thin source region (10^{20} cm^{-3}) below the nanowire and substrate interface. The nanowire is divided into 3 regions source, channel and the drain region. The source and drain region are of same lengths (30 nm or 25 nm) with a gaussian doping (n/p) profile varying from highly doped source in substrate to channel. The channel region is p/n doped (10^{17} cm^{-3}) and devices are created with different channel lengths of 180 nm, 90 nm, 45 nm, 22 nm. The diameter of

the nanowire region is 10 nm (15 nm) uniform along the length. The gate region consists of SiO_2 as the gate dielectric with constant thickness of 2 nm around the wire for all devices with gate overlap of source/ drain as 5 nm. It has a workfunction specified gate (4.4 eV for n and 4:85 eV for p devices in order to tune the threshold voltage) of thickness 10 nm around the gate oxide with a pad structure on which the gate metal via will be formed. The metal via for source, gate and the metal contacts for gate, drain and source are of Aluminum metal. The 3-D device structures thus obtained is shown in Figure 4.4.

As discussed in section 3.4, the minimum gate length achieved with t_{ox} of 2 nm and t_{si} of 10 nm is 20 nm. Hence the device scaling has been done with minimum gate length of 22 nm.

After the structure creation and contact definition we have to mesh it in order to generate the necessary files needed for device simulation. This is accomplished with the help of Sentaurus meshing tools. We define coarse meshing in substrate region, fine meshing for source region in substrate and finest meshing for nanowire region, gate region and electrode regions as shown in Figure 4.5.

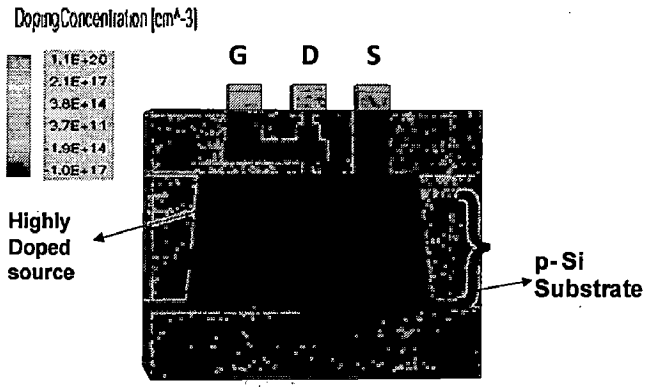


Figure 4.4 (a) NMOS device with channel length of 45nm

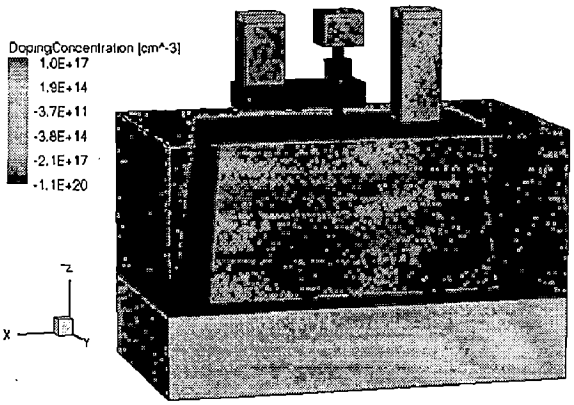


Figure 4.4 (b. PMOS device with channel length of 45nm

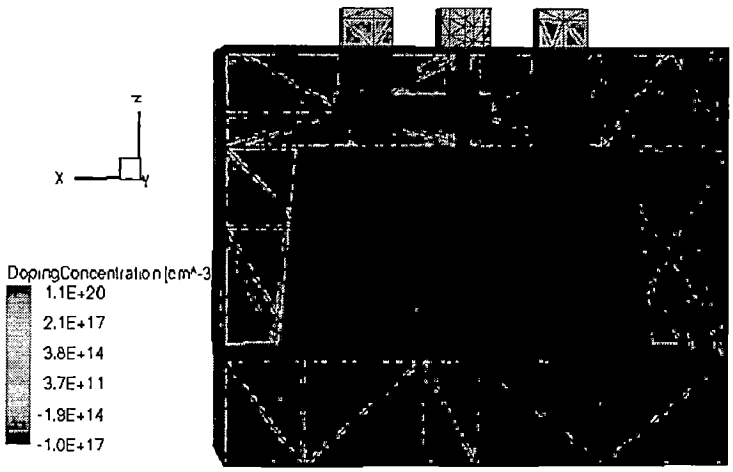


Figure 4.5 Device structure after meshing.

As mentioned in the structure details channel length scaling and nanowire diameter scaling are studied for 2 different S/D lengths.

4.2 Channel length and nanowire diameter scaling study

In this work, both the n and p NW GAAFET devices are simulated for different channel lengths and for 2 different S/D lengths. A typical I_d-V_{gs} characteristic of n/p NW GAAFET for different drain bias is shown in Figure 4.6.

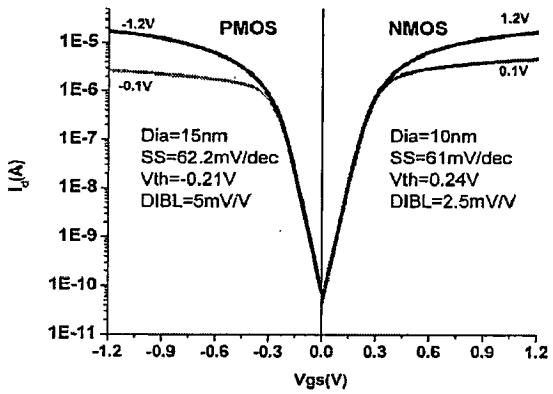


Figure 4.6 I_d-V_{gs} of NMOS and PMOS of L=45nm

The subthreshold slope (SS) indicates how effectively the transistor can be turned off when V_{gs} is decreased below V_{th} [12]. The SS is measured in millivolts per decade of drain current. For the limiting case of $t_{ox} \rightarrow 0$ and at room temperature, SS $\approx$ 60 mV/ decade. From the Figure 4.7 we can observe that the SS of NW GAAFET is nearly 60mV/ decade which prove the better gate control over channel electrostatics even for small channel lengths. Also the

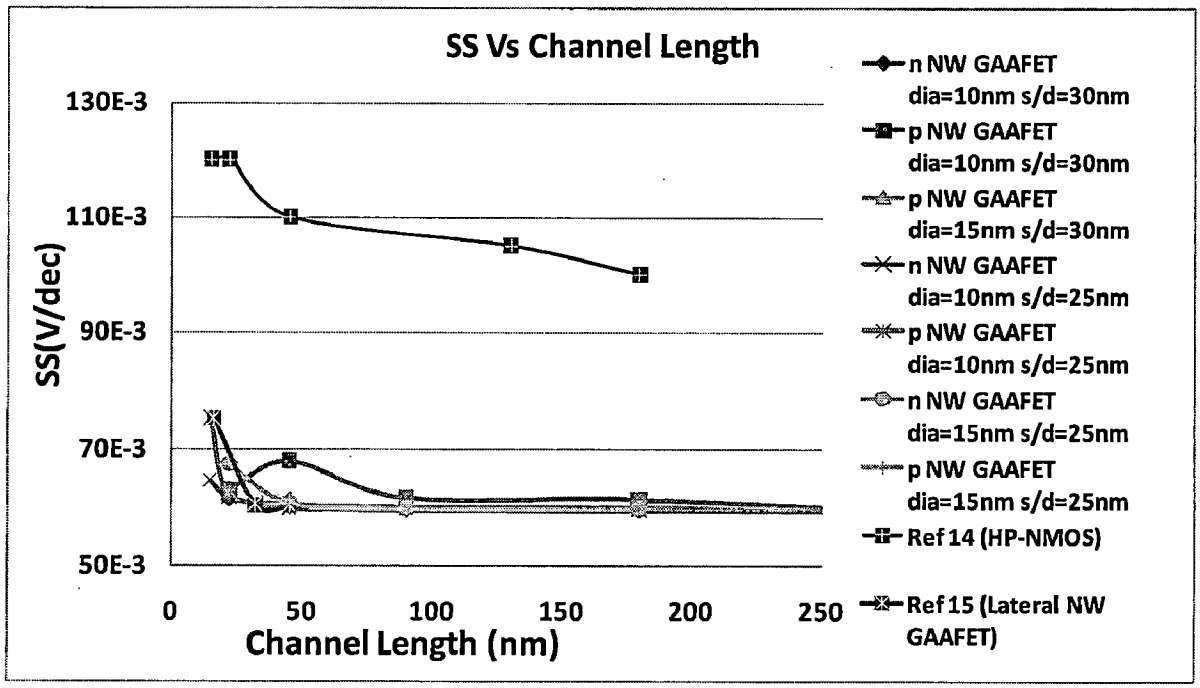


Figure 4.7 Subthreshold slope Vs Channel Length

lateral NW GAAFET is observed to have SS ≈ 60 mV/dec when compared to bulk MOSFET with SS > 100mv/dec. Thus the multiple gate devices are better than the planar or 2D bulk devices. It can also be observed the effect of S/D length on SS of device is not significant. But beyond the scalable limit for this device i.e., 20 nm it is observed that for 15 nm channel length the device is affected by short channel effects.

The threshold voltage (V_{th}) for long channel devices is simply the gate voltage when the surface potential or band bending reaches $2\psi_B$ and the silicon charge is equal to the bulk depletion charge for that potential [13]. For the extraction purpose we consider the V_{gs} value where the I_d = 300 nA (n device) and -150 nA (p device) from the I_d-V_{gs} characteristic. From the Figure 4.8 it can be observed that with decreasing channel length the threshold voltage of device also decreases. And there is negligible effect of varying S/D length on threshold voltage of the device.

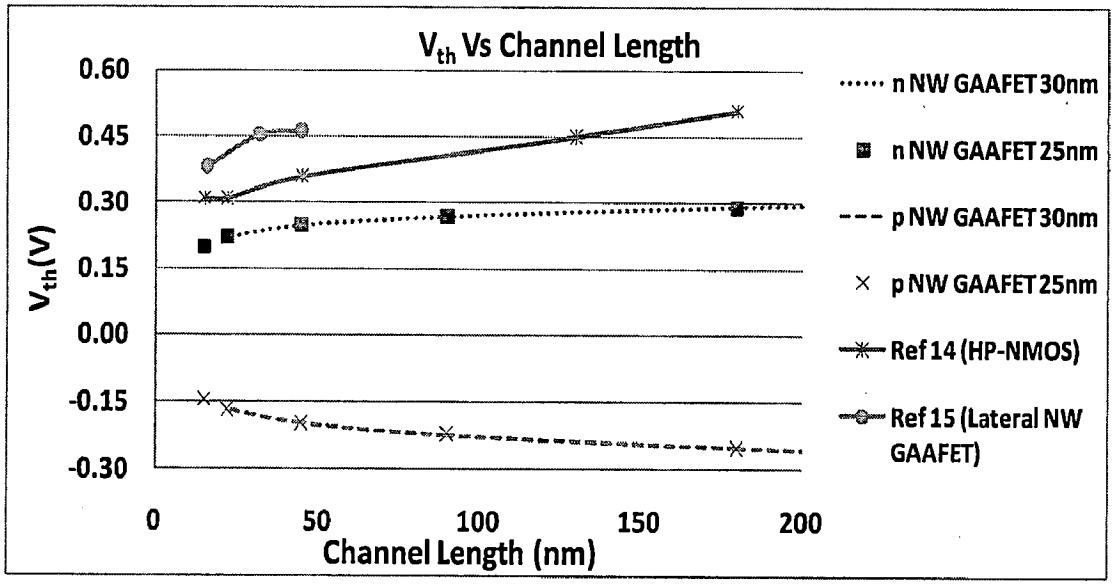


Figure 4.8 V_{th} Vs Channel Length

As the drain voltage increases, the drain to channel depletion region widens, resulting in a significant increase in the drain current. This increase in I_{off} is typically due to channel surface current caused by drain-induced barrier lowering (DIBL) [13]. Or it can also be understood as, when a high drain voltage is applied to a short-channel device, the barrier height is lowered even more, resulting in further decrease of the threshold voltage [13]. Thus DIBL is calculated as ratio of change in V_{th} to change in V_{ds} in units of mV/V. It can be observed from Figure 4.9 that the n-NW GAAFET devices have negligible DIBL thus implies that the increase in off current or decrease in barrier is not significant. For bulk MOSFET with DIBL > 100 mV/V indicates the presence of severe short channel effects.

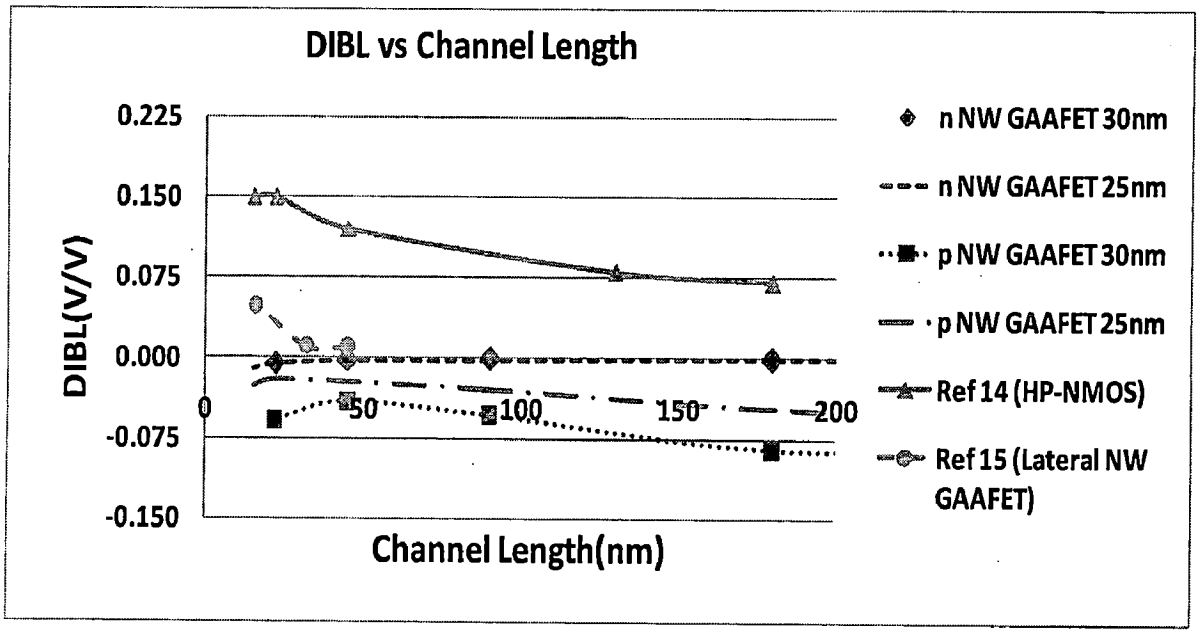


Figure 4.9 DIBL Vs Channel Length

Transistor on-state current (I_{ON}) is the drain current when $V_g = V_d = V_{dd}$, and transistor off-state current (I_{OFF}) is the drain current when the gate voltage is zero.

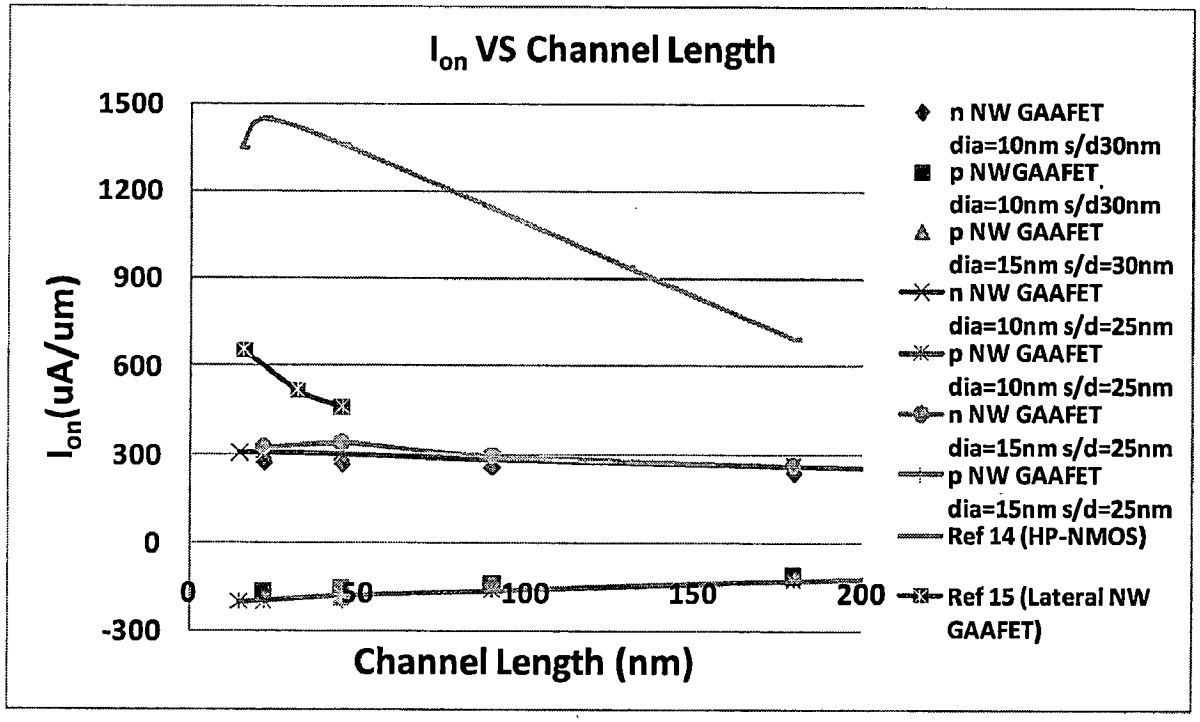


Figure 4.10 I_{on} Vs Channel Length

From Figure 4.10 it is observed that the on current of vertical NW GAAFET is around 200-300 μA/μm which is small when compared with bulk and lateral NW GAAFET. The higher on current in case of lateral NW GAAFET is due to the presence of large S/D pads which are absent in vertical pillar type. The on current can be increased by using multiple wires between S/D. Or an alternative way to achieve higher drive currents is by increasing the nanowire diameter.

The main effect of S/D length can be seen on I_{on} of the devices, it can be observed that a 12% increase is obtained with 5 nm reduction in S/D length indicating strong dependence of drive current on S/D series resistance as shown in Figure 4.11.

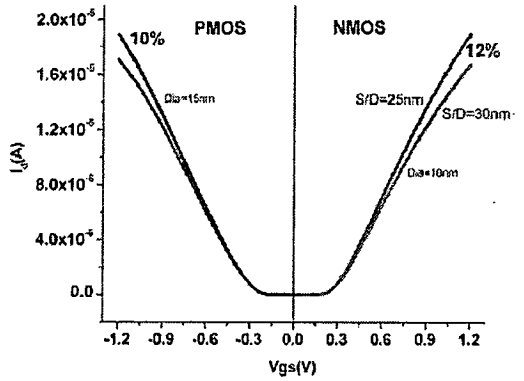


Figure 4.11 I_d-V_{gs} for different S/D lengths for channel length of 45nm

Similar trends can be observed for I_{on}/I_{off} ratio shown in Figure 4.12. The lateral NW GAAFET has ratio of ~10^7 to 10^9 whereas vertical devices have lower ratio of 10^6. For the bulk devices though the I_{on} is very high, the off state leakages is so high that effectively I_{on}/I_{off} ratio decreases and is comparable with vertical NW GAAFET. Also the effect of S/D length can be clearly observed, for shorter S/D lengths the ratio is higher. With increase in nanowire diameter it is observed that for n devices there is increase in I_{on} of the device but the corresponding increase in I_{off} is much higher thus resulting in lower I_{on}/I_{off} ratio where as for p devices the increase in I_{on} is much higher than increase in I_{off} thus it has a higher I_{on}/I_{off} ratio. It can be stated that increasing nanowire diameter will not only give higher drive currents but it also increases the off state leakages.

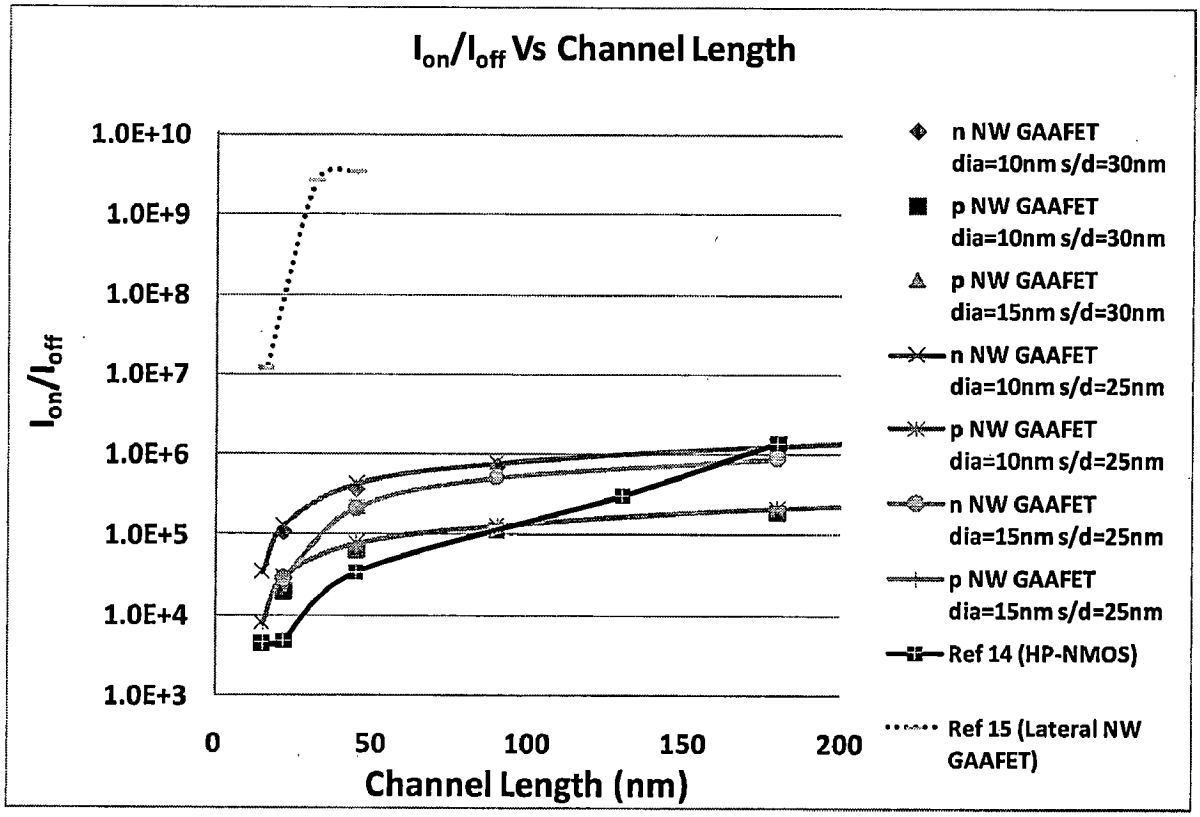


Figure 4.12 I_{on}/I_{off} Vs Channel Length

4.3 Device matching for CMOS Inverter

For inverter to have symmetric static and transient characteristics it is important to have matched n and p NW GAAFET device characteristics. The mismatch between similar n and p devices arise due to difference in carrier mobility. The device matching is to be achieved with respect to threshold voltage and on state current. In order to match the drive current of n and p devices it is observed that the p device nanowire diameter should be increased by 1.5 times with respect to n device nanowire diameter. We consider matched devices with channel

length of 45 nm and for 2 different S/D lengths as tabulated in Table 4.1, which will be used for inverter simulation in next chapter.

TABLE 4.1 MATCHED n, p NW GAAFET DEVICE PARAMETERS

	n NW GAAFET	p NW GAAFET	n NW GAAFET	p NW GAAFET
L	45 nm	45 nm	45 nm	45 nm
Diameter	10 nm	15 nm	10 nm	15 nm
S/D length	25 nm	25 nm	30 nm	30 nm
V_{th} (V)	0.249	-0.215	0.249	-0.213
I_{on} (A)	$1.90X10^{-5}$	$-1.89\ X10^{-5}$	$1.67\ X10^{-5}$	$-1.71\ X10^{-5}$

CHAPTER 5

Vertical NW CMOS Inverter Configurations

Table of Contents

5.1 Introduction

CMOS inverter is implemented for two different types of configurations based upon the number of nanowires present in the inverter circuit. The first type, the two wire vertical CMOS inverter (TWVI) is implemented with interconnected n and p matched devices. It is called as TWVI as its structure contains 2 wires, 1 in each n and p device. The matched devices of Table 3.1 in section 3.4 are used to simulate the static and dynamic characteristics of inverter. The second type, the single wire vertical CMOS inverter (SWVI), it is called so because the structure consists of single nanowire. The structure is such that both n and p device can be obtained from this single nanowire.

5.2 Two Wire Vertical CMOS Inverter (TWVI)

This configuration is obtained by interconnecting matched n and p devices as shown in Figure 5.1 with a capacitive load at output node. As this configuration has 2 nanowires (1 in each device), hence the name TWVI. The devices used in this configuration are with channel length of 45 nm, n device nanowire diameter as 10 nm and p device nanowire diameter as 15 nm the other device parameters are mentioned in Table 3.1. The TWVI is simulated for 2 different S/D lengths.

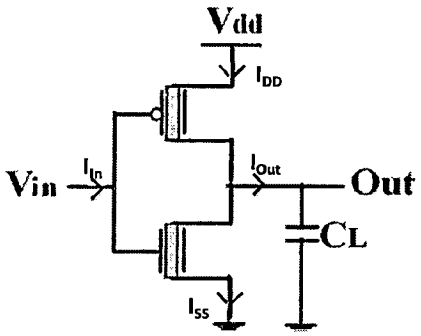


Figure 5.1 TWVI circuit schematic

Figure 5.2 shows layout of TWVI configuration with λ (= 45 nm) based design rules i.e., the channel length of devices is λ, minimum spacing between features in device is λ (S/D/Gate contact to STI edge, S to D and D to gate contact spacing) and device to device spacing as 2λ. Thus, the TWVI configuration consumes Si area of $42\lambda^2$. This configuration is mainly affected by internal device parasitics rather than the inter-device parasitic and is also affected by inter connect parasitics. The parasitic components in a NW GAAFET have been identified and shown in Figure 5.3.

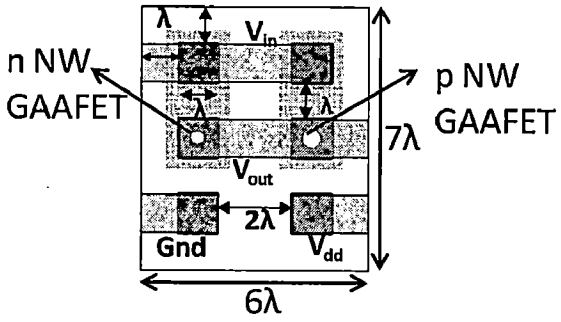


Figure 5.2 Layout of TWVI with n-dia=10nm and p-dia=15nm and L=45nm

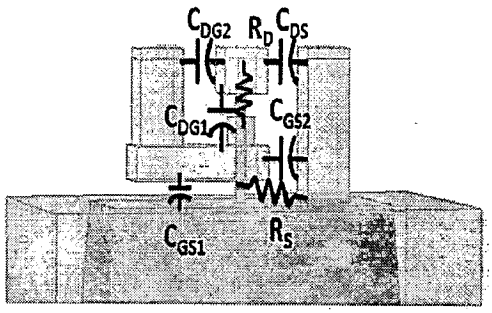


Figure 5.3 Parasitic components in an NW GAAFET

5.3 Single Wire Vertical CMOS Inverter (SWVI)

The single wire vertical inverter structure is as shown in Figure 5.4 with bottom half functioning as the p device and n device stacked on top of it. It has common drain contact and common gate contact with via connecting both n and p gate pad extensions. This configuration has been implemented for 2 different cases based on wire diameter in n and p halves as dual diameter SWVI and single diameter SWVI.

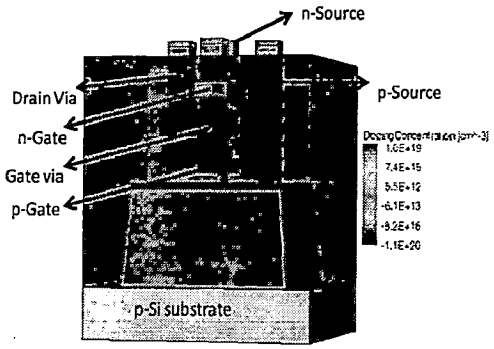


Figure 5.4 3D view of SWVI device with channel length of 45 nm

5.3.1 Dual Diameter SWVI

As discussed in section 3.4, that for inverter to have symmetric characteristics we have to match n and p devices, this lead to the implementation of SWVI with different diameter of wire for n and p halves.

The layout of dual diameter SWVI CMOS following the λ based design rules is shown in Figure 5.5 and it occupies Si area of $24\lambda^2$ which is nearly 45 % lower than TWVI configuration layout. The dual diameter SWVI shown schematically in Figure 5.6 and 2D device cuts shown in Figure 5.7 can be obtained by the following proposed processing steps on a single vertical nanowire for both n and p devices. First, nanowire with required diameter for use as p device, i.e., 15 nm is obtained. Then the process steps of p device fabrication as

given in section 4.1 are carried out on the bottom half of nanowire and filled with isolation oxide. Next the top half of nanowire is oxidized to obtain the required diameter for use as n device, i.e., 10 nm. The n device process steps are then performed on this half and filled with oxide. Finally oxide is etched to make vias for p source, common drain and common gate. These vias are then filled with aluminum and the four contacts are obtained on the top. The dual diameter SWVI is implemented using the structure editor tool of Sentaurus.

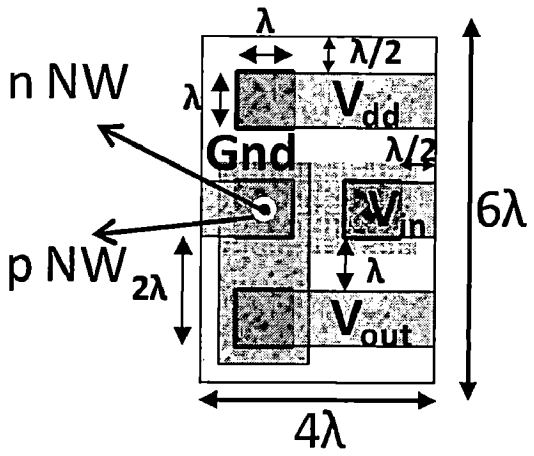


Figure 5.5 Layout of dual diameter SWVI with n -dia=10 nm, p-dia=15 nm and L= 45 nm

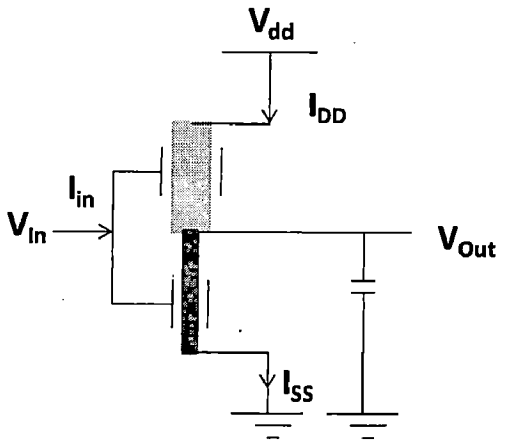


Figure 5.6 Dual diameter SWVI circuit schematic thick p-wire and thin n-wire

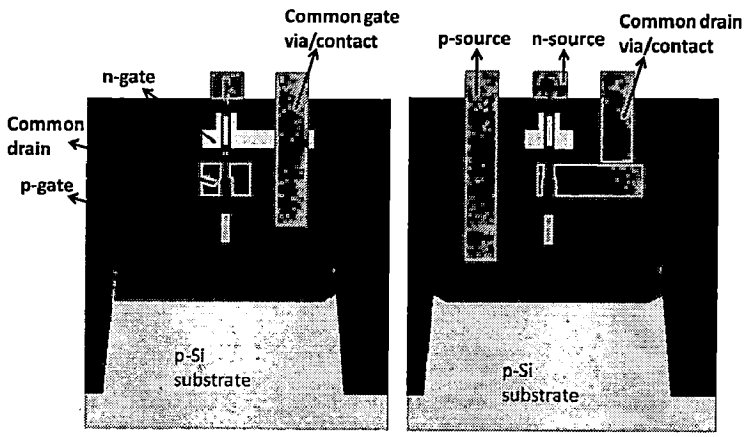


Figure 5.7 2D cuts of dual diameter SWVI showing common gate and common drain via/contacts with bottom p-NW dia = 15nm and top n-NW dia = 10 nm with L=45nm

It is observed that the dual diameter SWVI has asymmetric characteristics, which will be presented in the section 5.5. This asymmetric behavior is attributed to the absence of large source pad in the n device (top half) and the increase in S/D resistance due to decreased contact area. Thus a SWVI is implemented with a thicker n wire diameter to reduce the series resistance and also account for the absence of source pad; it is presented in detail in the next section.

5.3.2 Single Diameter SWVI

The layout of single diameter SWVI CMOS is shown in Figure 5.8 and its schematic in Figure 5.9. The single diameter SWVI can be obtained by processing on a single vertical nanowire. First nanowire with required diameter i.e., 15nm is obtained. Then the process steps of p device fabrication are carried out on the bottom half of nanowire and filled with isolation oxide. The n device process steps are then performed on the top half and filled with oxide. Finally oxide is etched to make vias for p source, common drain and common gate. These vias are then filled with aluminum and the four contacts are obtained on the top. And the 2D cut shown in Figure 5.10 shows the single diameter nanowire.

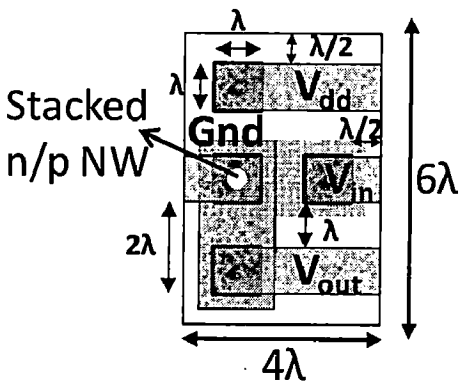


Figure 5.8 Layout of Single diameter SWVI, L=45 nm n/p dia = 15 nm

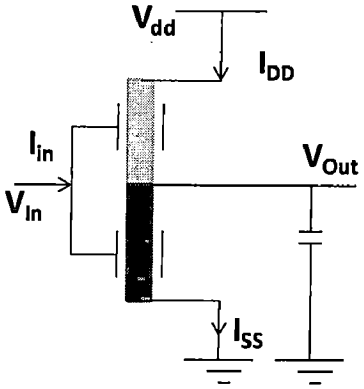


Figure 5.9 Single diameter SWVI circuit schematic

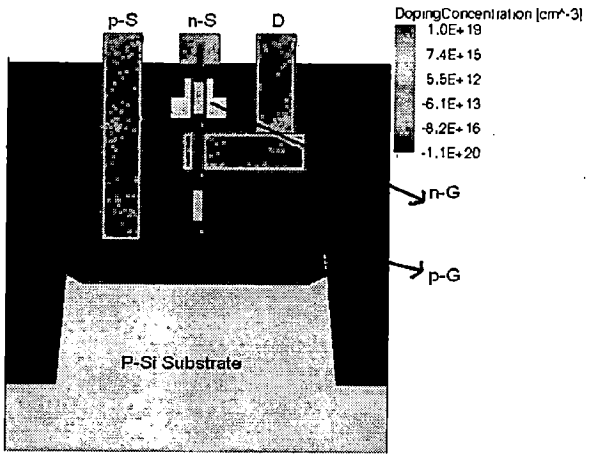


Figure 5.10 2D cut of Single diameter SWVI with L= 45 nm and n/p dia = 15 nm

It can be observed from Figure 5.11 that SWVI configuration has no additional interconnect parasitic, but there is increase in inter-device parasitic between the n and p halves. Due to vertical stacking of the devices there is reduced contact area of n source and reduced contact area of drain pad with drain region. Thus, SWVI is expected to have large delay when compared to TWVI.

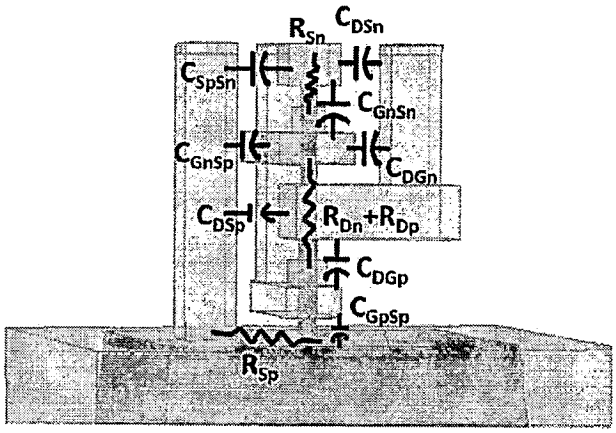


Figure 5.11 Parasitic components in a SWVI

5.4 Voltage Transfer Characteristics (VTC) of TWVI and SWVI

The voltage transfer characteristics describe V_{out} as a function of V_{in} under DC conditions. The main parameters obtained from this are noise margins (NM) levels and inverter threshold voltages as indicated in Figure 5.12.

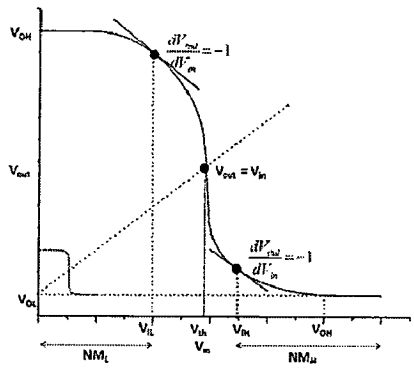


Figure 5.12 Typical VTC of CMOS inverter

A detailed description of voltage transfer characteristics has been presented in Appendix A along with the mathematical expressions for noise margins and inverter threshold [16]. These are used as a first order approximation to model the inverter static characteristics. The values of parameters K_n and K_p are obtained from G_m versus V_{GS} curves (derivative of $I_D - V_{GS}$ curve) by considering the average value of G_m beyond V_{GS} (G_{mMax}) and up to V_{DD}.

A typical voltage transfer characteristics of dual diameter SWVI for S/D = 25 nm is shown in Figure 5.13. It is observed that nanowire based devices can be operated at very low supply voltages (0.2V). The gain of inverter defined as dV_{out}/dV_{in} [4] is calculated for different V_{DD} and a typical gain Vs V_{DD} plot for dual diameter SWVI for S/D = 25 nm is shown in Figure 5.14 with a maximum gain of 70. The noise margins and gain are comparable with the fabricated lateral device characteristics reported in [4], [5]. The maximum gain Vs S/D length for different inverter configurations is shown in Figure 5.15.

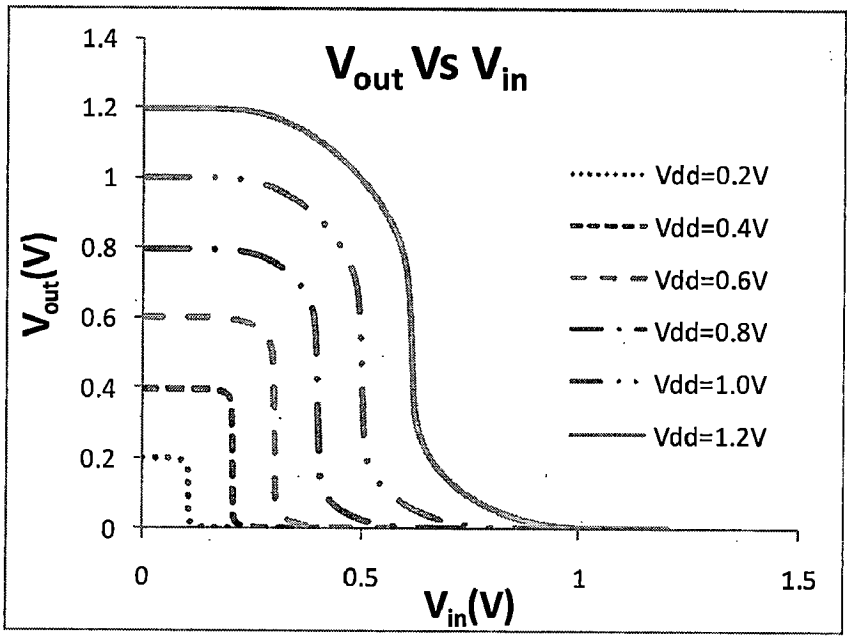


Figure 5.13 Typical Voltage transfer characteristics of dual diameter SWVI with S/D =25 nm for different V_{DD}

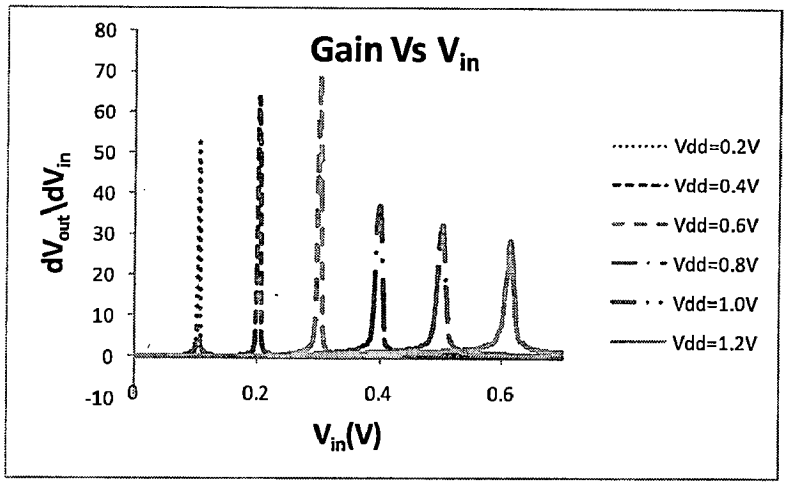


Figure 5.14 Typical Gain Vs V_{DD} plot of dual diameter SWVI with S/D = 25 nm

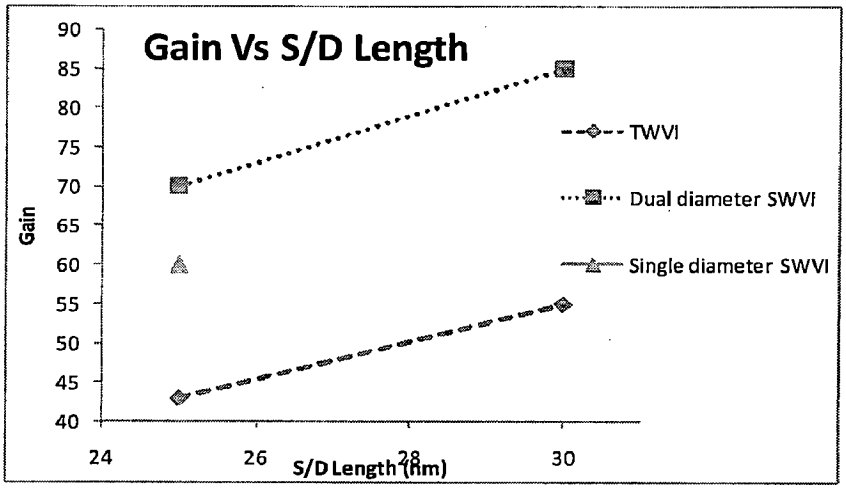


Figure 5.15 Maximum Gain Vs S/D lengths for TWVI and SWVI configurations.

The simulated and calculated static noise margins, inverter threshold for different configurations are tabulated in Table 5.1. It is observed that there is negligible effect of S/D length on noise margin levels and inverter threshold voltage. But the single diameter SWVI threshold decreases comparably with respect to dual diameter SWVI due to thicker n wire. Thus, indicating the difference in drive currents of n and p halves.

TABLE 5.1 SIMULATED AND CALCULATED STATIC NOISE MARGINS, INVERTER THRESHOLD FOR DIFFERENT CONFIGURATIONS AT V_{DD}=1.2V

			SWVI		
	TWVI		**Dual diameter**		**Single diameter**
S/D Length	25nm	30nm	25nm	30nm	25 nm
NM_H (V)	0.514	0.500	0.482	0.457	0.482
NM_L (V)	0.392	0.383	0.423	0.412	0.423
V_{th} (V)	0.584	0.584	0.610	0.614	0.52
NM_H Calc (V)	0.483	0.494	0.483	0.494	0.56
NM_L Calc (V)	0.507	0.5	0.507	0.5	0.43
V_{th} Calc (V)	0.61	0.6	0.61	0.6	0.55

Figure 5.16 shows a typical plot of simulated and calculated noise margins for TWVI configuration with S/D = 30 nm, using Eqn. (A.4) – (A.6). A good matching between simulated and calculated value is observed except for NM_L at high V_{DD}. This is attributed to V_{th} variation due to DIBL effects which are not modeled in equations used.

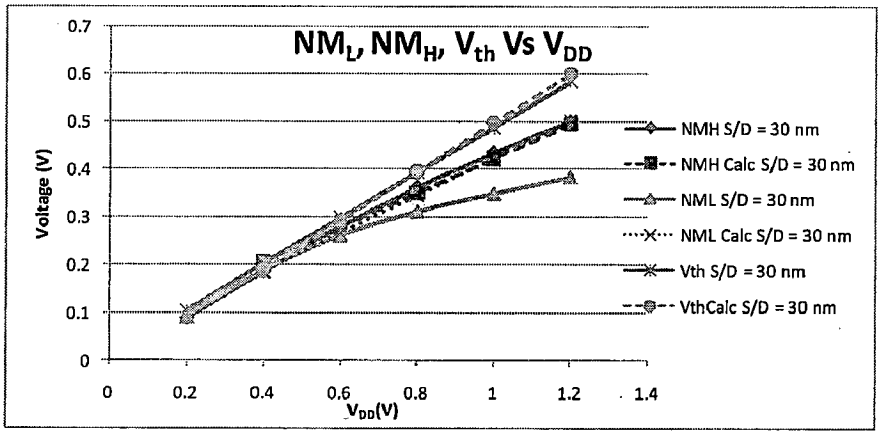


Figure 5.16 Typical plot of simulated and calculated noise margins, inverter threshold for TWVI with S/D=30nm

5.5 Dynamic Characteristics of TWVI and SWVI

The dynamic characteristics (explained in detail in Appendix A) of TWVI and SWVI (dual and single diameter) having different S/D lengths for standard fanout of four is summarized in Table 5.2. In Figure 5.17 detailed transient characteristics are shown for different inverter configurations with S/D = 25 nm. For both dual diameter and single diameter SWVI the delay

is large when compared to TWVI this is due to extra capacitances between the n and p halves and the increase in source/drain resistance due to lower contact area overlap. It is observed that the high to low propagation delay (T_{pHL}) in dual diameter SWVI is very high; this is because of the absence of source pad in n half. The delay of dual diameter SWVI is improved by using single diameter SWVI which has a thicker n wire accounting for the absence of source pad. This will affect the inverter characteristics during the output rising transition by increasing the leakages thereby reducing the load capacitance charging rate. Thus, T_{pLH} of single diameter SWVI is higher than the dual diameter SWVI. It is observed from Table 5.2 that S/D length plays a significant role in delay values, decreasing the S/D length by 5 nm decreases the delay by 8-12%.

TABLE 5.2 DYNAMIC CHARACTERISTICS OF TWVI and SWVI for L=45 nm

			SWVI		
	TWVI		Dual Diameter		Single Diameter
S/D length (nm)	25nm	30nm	25nm	30nm	25 nm
T_{pHL} (ps)	10.6	11.8	20.9	22.0	12.0
T_{pLH} (ps)	11.1	12.6	14.2	15.9	16.0
T_d (ps)	10.8	12.2	17.6	19.0	14.0

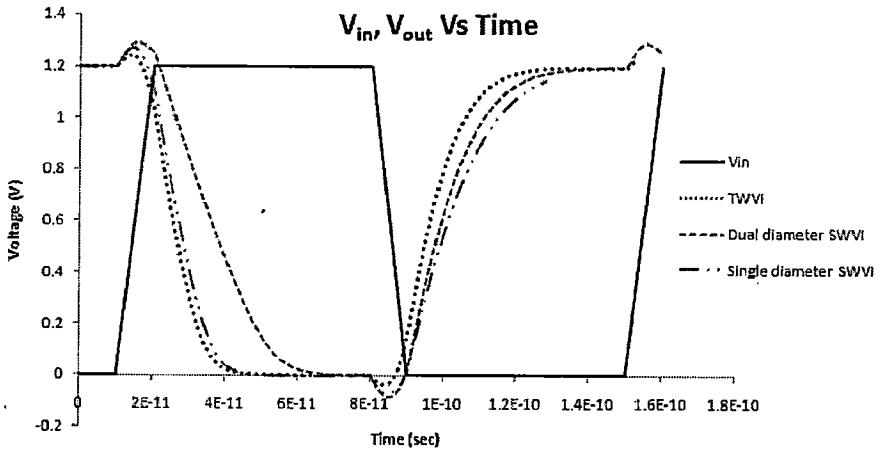


Figure 5.17 Typical Dynamic characteristics of TWVI and SWVI with S/D = 25 nm

The dynamic characteristic parameters T_{pHL}, T_{pLH} and T_p are calculated for TWVI and SWVI using the Eqn. (A.8) – (A.12) given in Appendix A. The load capacitance (C_{load}) is extracted by obtaining total charge stored or discharged at output node during voltage rise ($0.1V_{DD}$ to $0.9V_{DD}$) or fall ($0.9V_{DD}$ to $0.1V_{DD}$). This charge is obtained by integrating the difference in I_{DD}, I_{SS} (supply currents indicated on inverter schematic in Figures 5.1, 5.6, 5.9) during the rise or fall time.

Thus, the expression for C_{Load} is given by:

$$C_{Load} = \frac{\Delta Q}{0.8V_{DD}} = \frac{\int_{t_{0.1V_{DD}}}^{t_{0.9V_{DD}}} [I_{DD} - I_{SS}]dt}{0.8V_{DD}} \quad (5.1)$$

The total output node capacitance while charging and discharging a 200aF load, extracted from this method for different configurations is given in Table 5.3. It can be observed that the SWVI structure has more internal capacitances than the TWVI structure which proves the structure parasitic components discussion given in section 5.2 and 5.3. The increase in $C_{Load\ Fall}$ capacitance value in single diameter SWVI is the reason for the increase in delay during rise time.

TABLE 5.3 C_{Load} EXTRACTED DURING OUTPUT RISE AND FALL TRANSITIONS FOR DIFFERENT CONFIGURATIONS

			SWVI		
	TWVI		Dual diameter		Single diameter
S/D length	25nm	30nm	25nm	30nm	25 nm
$C_{Load\ Fall}$ (aF)	250	250	300	300	310
$C_{Load\ Rise}$ (aF)	270	265	340	335	340

Using the output node capacitances given in above table, the dynamic characteristic delay parameters are calculated using the equations (A.8)-(A.12) given in Appendix A and tabulated in Table 5.4. A typical plot of calculated and simulated inverter delay parameters for dual diameter SWVI is shown in Figure 5.18. The calculated values show good fit to within 10% of the simulated values.

TABLE 5.4 CALCULATED VALUES OF T_{pLH}, T_{pHL}, T_p FOR DIFFERENT CONFIGURATIONS

			SWVI		
	TWVI		Dual diameter		Single diameter
S/D length	25nm	30nm	25nm	30nm	25 nm
T_{pHL} calc (ps)	17.5	19.3	21.3	25.6	11.1
T_{pLH} calc (ps)	13.0	15.6	16.6	19.6	16.7
T_p calc (ps)	15.2	17.4	19.0	22.6	13.9

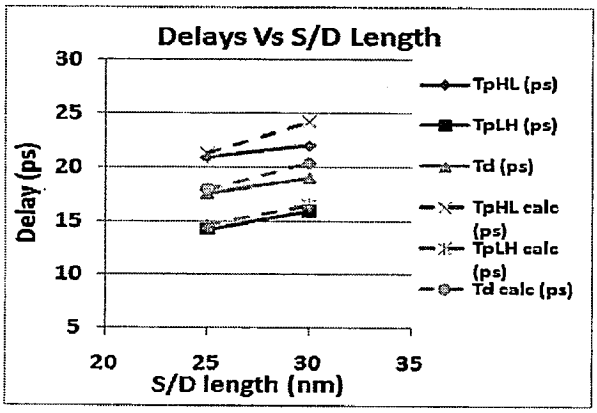


Figure 5.18 Typical plot of simulated and calculated inverter delay parameters for dual diameter SWVI

One of the most important parameter to benchmark devices is the power dissipation (a detail study of inverter power dissipation is given in Appendix A). As stated the power dissipation is independent of transistor characteristics and transistor sizing [16], it depends on the load, supply voltage and the frequency of operation. The load is quantified in terms of fanout (number of equivalent inverters the ouput can drive). Thus the SWVI and TWVI inverter configurations are benchmarked with FinFET based CMOS [17] for area consumption, power dissipation ($C_L f V_{DD}^2$) and inverter delay with load equivalent to fanout of 4. From Table 5.5 it is observed that SWVI has the least area consumption with 80 % saving, power saving of up to 70 % and with increase in delay by 40 - 80 % for single diameter and dual diameter respectively. The TWVI has 65 % area gain with 77 % lower power and 15 % increase in delay. From this analysis it can be stated that the single diameter SWVI has better overall performance.

TABLE 5.5 PERFORMANCE COMPARISONS OF TWVI, SWVI, FINFET

Device	FinFET	TWVI	SWVI	
			Dual diameter	Single Diameter
Area	120 λ^2	42 λ^2	24 λ^2	24 λ^2
Area (µm2)	0.243	0.08505	0.0486	0.0486
% Area saving	0	65	80	80
Delay (FO 4) (ps)	10	11.5	18.3	14.1
Power (pW/gate/MHz)	430	100	130	144
% increase in Delay	0	15	83	40
% decrease in Power	0	77	70	67

CHAPTER 6

Conclusions and Future scope

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6.1 Conclusions

Vertical Si Nanowire GAAFET's are simulated at different channel lengths and nanowire diameter with minimum Si area consumption. As per the scaling theory of GAA devices it is found that device with gate length of up to 22 nm can be achieved with reasonable subthreshold behavior. It is observed that these devices have subthreshold swing ≈ 60mV/dec at room temperature thus proving best electrostatic control over the channel potential when compared to > 80mV/dec for other devices. The DIBL of these devices is less than 50 mV/V, which is very less than the stringent condition imposed by Gnani et.al. [6] i.e.,100 mV/V. With increasing nanowire diameter the drive current of device increases, this technique is applied to obtain matched devices for CMOS inverter with symmetric characteristics.

In this work two different inverter configurations TWVI and SWVI have been discussed in detail. The static and dynamic characteristics show excellent performance with lower area and power consumption. Of all CMOS inverter the SWVI configuration with single diameter wire has the best overall performance. It is observed that single diameter SWVI has area gain of 80 % and around 70 % decrease in power consumption when compared with FinFET. With the first order approximated modeling of inverter characteristics, the error of 10 % is a good start towards the modeling of novel gate all around devices.

6.2 Future Scope

This work can be continued by implementation of the basic gates (NAND, NOR, XOR, XNOR) and their performance analysis for two configurations. A detailed device modeling considering the effect of effective channel length, S/D length, t_{ox} and nanowire diameter can be carried out. The SWVI structure encourages to implement a single wire transmission gate (SWTG) and carrying out a comparative study with two wire transmission gate (TWTG). The main application of SWTG is as programmable interconnects in field programmable gate array (FPGA) circuits.

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Appendix - A

Voltage Transfer Characteristics (VTC) of CMOS Inverter [16]

For very low input voltage levels, the output voltage is equal to the high value of V_{OH}. In this case, the driver nMOS transistor is in cut-off and hence, does not conduct any current and pMOS is in saturation. As the input voltage increases, the nMOS transistor starts conducting a certain drain current, and the output voltage eventually starts to decrease. This drop in output voltage is rather gradual and with a finite slope. Two critical voltage points on this curve are identified, where the slope of $V_{out}(V_{in})$ characteristics become equal to -1.

$$\frac{dV_{out}}{dV_{in}} = -1 \tag{A.1}$$

The smaller input voltage value satisfying this condition is called the input low value V_{IL}, and the larger input voltage satisfying this condition is called the input high value V_{IH}. Both of these voltages play significant roles in determining the noise margins of the inverter circuit.

As the input voltage is further increased, the output voltage continues to drop and reaches a value of V_{OL} (output low voltage) when the input voltage is equal to V_{OH}. This happens because of pMOS transition from saturation to cutoff state. The inverter threshold V_{th}, which is considered ad the transition voltage, is defined as the point where $V_{in} = V_{out}$ on the VTC. All these are shown in a typical VTC curve in Figure A.1.

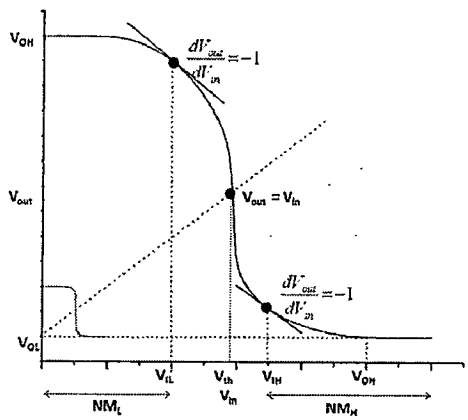

Figure A.1 Typical VTC of a CMOS Inverter

Thus any input voltage level between the lowest available voltage in the system and V_{IL} is interpreted as logic "0" input, while any input voltage level between the highest available voltage in the system and V_{IH} is interpreted as logic "1" input. These are used to define noise tolerances for digital circuits, called noise margin (NM) and are calculated as shown in

Eqn. (A.2) and (A.3). Figure A.2 shows a graphical illustration of the noise margins. Here, the shaded areas indicate the valid regions of input and output voltages.

$$NM_L = V_{IL} - V_{OL} \tag{A.2}$$

$$NM_H = V_{OH} - V_{IH} \tag{A.3}$$

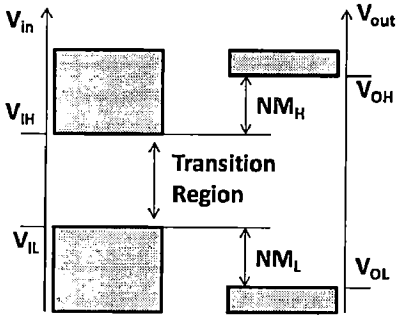

Figure A.2 Definition of noise margin diagramatically.

For a CMOS inverter $V_{OH} = V_{DD}$ and $V_{OL} = 0$. From $I_{D,n} = I_{D,p}$, for different transition regions the mathematical expressions for V_{IL}, V_{IH} and V_{th} can be obtained as

$$V_{IH} = \frac{V_{DD} + V_{T0,p} + K_R.(2V_{out} + V_{T0,n})}{1 + K_R} \tag{A.4}$$

$$V_{IL} = \frac{2V_{out} + V_{T0,p} - V_{DD} + K_R V_{T0,n})}{1 + K_R} \tag{A.5}$$

$$V_{th} = \frac{V_{T0,n} + \sqrt{1/K_R}.(V_{DD} + V_{T0,p})}{(1 + \sqrt{1/K_R})} \tag{A.6}$$

$$\text{where } K_R = \frac{K_n}{K_p} \tag{A.7}$$

Dynamic Characteristics of CMOS Inverter [16]

The dynamic characteristic (transient analysis) of the inverter is obtained for a pulse input with a finite rise and fall time as shown in Figure A.3. The propagation delays T_{pHL} and T_{pLH} determine the input-to-output signal delay during the high-to-low and low-to-high transitions of the output, respectively. These delays are measured at $V_{50\%}$ transition voltage level. The average propagation delay T_p of the inverter characterizes the average time required for the input signal to propagate through the inverter.

For a CMOS inverter with step input these delay parameters are mathematically expressed as Eqn. A.8–A.10.

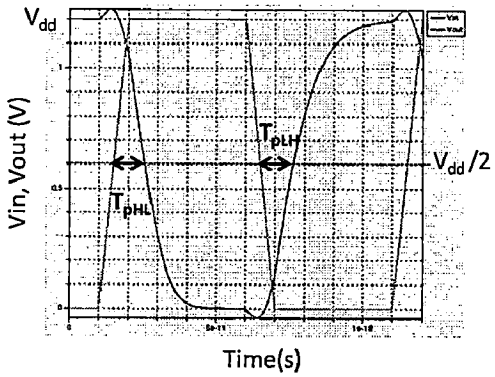

Figure A.3 Dynamic characteristics of a CMOS Inverter

$$\tau_{PHL}\,(step\ input) = \frac{C_{load}}{K_n(V_{DD} - V_{T,n})}\left[\frac{2V_{T,n}}{V_{DD} - V_{T,n}} + \ln\left(\frac{4(V_{DD} - V_{T,n})}{V_{DD}} - 1\right)\right] \tag{A.8}$$

$$\tau_{PLH}\,(step\ input) = \frac{C_{load}}{K_p(V_{DD} - |V_{T,p}|)}\left[\frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + \ln\left(\frac{4(V_{DD} - |V_{T,p}|)}{V_{DD}} - 1\right)\right] \tag{A.9}$$

$$\tau_p = \frac{\tau_{PHL} + \tau_{PLH}}{2} \tag{A.10}$$

Now, we consider the case where the input voltage waveform is not an ideal (step) pulse waveform, but has finite rise and fall times, τ_r and τ_f. Thus, the actual propagation delays are calculated using the following empirical expressions:

$$\tau_{PHL}\,(actual) = \sqrt{\tau_{PHL}^2\,(step\ input) + \left(\frac{\tau_r}{2}\right)^2} \tag{A.11}$$

$$\tau_{PLH}\,(actual) = \sqrt{\tau_{PLH}^2\,(step\ input) + \left(\frac{\tau_f}{2}\right)^2} \tag{A.12}$$

Switching Power Dissipation of CMOS inverter [16]

During switching events where the output load capacitance is alternatingly charged up and charged down, on the other hand, the CMOS inverter inevitably dissipates power. When the input voltage switches from low to high the pMOS transistor in the circuit is turned off, and the nMOS transistor starts conducting and discharges the output load capacitance C_{load}. When the input voltage switches from high to low, the nMOS transistor in the circuit is turned off, and the pMOS transistor starts conducting and charges the output load capacitance C_{load}. Therefore, the capacitor current equals the instantaneous drain current of the pMOS transistor.

Assuming periodic input and ouput waveforms, the average power dissipated by any device over one period can be found as follows:

$$P_{avg} = \frac{1}{T}\int_0^T v(t).i(t)\,dt \tag{A.13}$$

Since during switching, the nMOS transistor and the pMOS transistor in a CMOS inverter conduct current for one-half period each, the average power dissipation of the CMOS inverter can be calcualted as the power required to charge up and charge down the ouptu load capacitance.

$$P_{avg} = \frac{1}{T}\left[\int_0^{T/2} V_{out}(-C_{load}\frac{dV_{out}}{dt})dt + \int_{T/2}^{T}(V_{DD}-V_{out})(C_{load}\frac{dV_{out}}{dt})\,dt\right] \tag{A.14}$$

$$P_{avg} = \frac{1}{T}C_{load}V_{DD}^2 = C_{load}V_{DD}^2 f \tag{A.15}$$

The average power is independent of transistor characteristics and transistor sizes.

Note that under realistic conditions, when the input voltage deviates from ideal step input and has non zero rise and fall times, for example, both the nMOS and pMOS transistor will simultaneously conduct a certain amount of current during the switching event. This is called as the short circuit current, since in this case, the two transistors temporarily form a conducting path between the V_{DD} and the ground. Thus, additional power dissipation is seen in the circuit. This short circuit dissipation becomes negligable in comparison to the power dissipation which is due to charging/discharging of capacitances.