FINFET BASED ROBUST SENSE AMPLIFIER DESIGN FOR PROCESS VARIATIONS

A DISSERTATION

Submitted in partial fulfillment of the requirements for the award of the degree

of

MASTER OF TECHNOLOGY

in

ELECTRONICS AND COMMUNICATION ENGINEERING

(With Specialization in Semiconductor Devices & VLSI Technology (SDVT))

By

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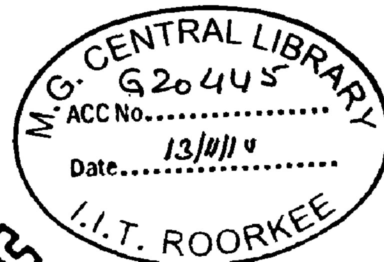

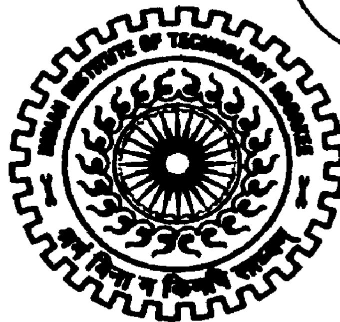

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CANDIDATE'S DECLARATION

I hereby declare that the work presented in this dissertation report entitled, "**FinFET based robust sense amplifiers design for process variations**," towards the partial fulfilment of the requirements for the award of degree of **Master of Technology** in **Electronics and Computer Engineering** with specialization in **Semiconductor Devices and VLSI Technology**, in the Department of Electronics and Computer Engineering, Indian Institute of Technology Roorkee, is an authentic record of my own work, carried out during the period from June 2009 to June 2010, under the guidance of **Dr. Sanjeev Manhas**, Assistant Professor, and **Dr. A.K. Saxena**, Professor, Department of Electronics and Computer Engineering, Indian Institute of Technology Roorkee.

The results embodied in this dissertation have not submitted for the award of any other degree or diploma.

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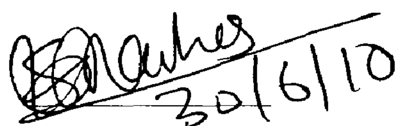
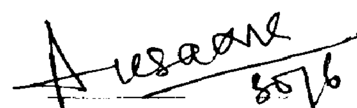
CERTIFICATE

This is to certify that the above statement made by the candidate is correct to the best of our knowledge and belief.





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ABSTRACT

Process variations inducing transistor characteristics mismatch have emerged as major challenge to nano-scale circuit design leading to failure and yield loss of circuits such as sense amplifiers. In this work, these issues have been addressed and compensated sense amplifier circuits having high tolerance to process variations have been designed. The circuit designed with double gate FinFET technology, utilizes an improved self-compensation technique to overcome variations in transistor characteristics. It exploits the backgate of FinFET device for dynamic compensation against process variations.

The simulations of threshold voltage (V_t) mismatch using Monte-Carlo technique on CCLSA circuit show that the proposed circuit functions correctly even for worst case V_t mismatch of 50mV. The results are benchmarked with corresponding circuits reported in literature for area, speed and yield gain. This sense amplifier design shows excellent tolerance and offers up to 30% higher yield compared to uncompensated circuit reported in literature. The CCLSA design have minimal penalty for circuit complexity, speed, and is easily implementable at 45nm and 32nm technology nodes.

Further two more circuit styles namely IGSA (Independent Gate Sense Amplifier) and LBSA (Latch Based Sense Amplifier) using independent gate control in double gate FinFET have been designed. The dynamic compensation introduced earlier has been applied to these circuits. The compensated IGSA offers 25% higher yield and proves to be more insensitive to mismatch than uncompensated IGSA reported in literature. Also compensated LBSA circuit shows 15-20% more tolerance and can withstands 20mV more mismatch than LBSA circuit. This robustness is attributed to the compensation scheme designed. Performance comparisons of CCLSA, CIGSA, CLBSA show that CIGSA has the best over performance in terms of yield, power, delay and area.

This work can be extended by implementing these circuits in a device simulator where fine tuning of FinFET device parameters can be done. Layouts of the circuits can also be drawn and parasitic can be measured. Multi-fin structures which are not utilized in this work can be a possible option for reducing the delay.

CONTENTS

CANDIDATE'S DECLARATION i
ACKNOWLEDGMENTS ii
ABSTRACT iii
LIST OF FIGURES vi
ABBREVIATIONS viii

CHAPTER 1: **INTRODUCTION** 1
1.1 Background 1
1.2 Thesis Contribution 2
1.3 Thesis Organization 3

CHAPTER 2: **BASICS OF DRAM CELL** 4
2.1 DRAM Structure and Operation 4
2.1.1 Memory Array 6
2.1.2 Dynamic Random Access Memory Cell Storage 6
2.1.3 Storage to Bit Line Capacitance 9
2.1.4 Static Data Retention 9
2.1.5 Data Sensing 12
2.1.6 Positive-Feedback Differential Voltage Sense Amplifier 13
2.1.7 Positive-Feedback Current Sense Amplifier 15
2.2 FinFET SOI Technology 16
2.2.1 SOI Technology in general 17
2.2.2 FinFET in SOI Technology 17
2.2.3 Advantages of SOI for DRAM 18

CHAPTER 3: **VARIATIONS STUDY AND RESULTS OF FINFET BASED SENSE AMPLIFIERS** 20
3.1 Abstract 20
3.2 Introduction 20
3.3 FinFET Based Latch Sense Amplifier 21

3.3.1 Impact of Process Variations in CLSA and VLSA 23
3.3.2 Monte-Carlo Analysis 24
3.3.3 Effect of V_t Mismatch on sensing of CLSA and VLSA 24
3.4 Compensated current latch sense amplifier (CCLSA) 25
3.4.1 Operation of Compensated Circuit of CLSA 26
3.4.2 Impact of Process Variations on the Compensated Circuit 27
3.5 Results 28
3.5.1 Yield v/s V_t Mismatch 28
3.5.2 Sense Delay v/s Bit-Line Differential Voltage 30

CHAPTER 4: **NOVEL FINFET BASED SENSE AMPLIFIERS AND RESULTS** 32
4.1 Abstract 32
4.2 Independent Gate Sense Amplifier 32
4.2.1 Operation of IGSA 33
4.2.2 Advantages of the IGSA Over Directly Translated CLSA 34
4.2.3 Compensated Circuit for IGSA (CIGSA) 36
4.2.4 Operation of Compensated Circuit of IGSA 37
4.2.5 Results 38
4.3 Latch-based sense amplifier 40
4.3.1 Impact of Process Variations in LBSA 42
4.3.2 Compensated Circuit for LBSA (CLBSA) 42
4.3.3 Results 43

CHAPTER 5: **CONCLUSION** 46
REFERENCES 49
PUBLICATIONS 51

LIST OF FIGURES

Figure No.	Caption	pp.
2.1	Architectural block diagram of a DRAM critical path	5
2.2	Signal timing diagram in DRAMs	5
2.3	Bit line configurations in DRAMs	7
2.4	Various DRAM cell structures	8
2.5	Leakage mechanisms for bulk-Si DRAM cell	12
2.6	Full-complementary positive-feedback sense amplifier circuit	13
2.7	Simple positive feedback current sense amplifier	15
2.8	Bisection of SOI MOSFET	18
2.9	Multiple-fin FinFET structure	18
3.1	FinFET based Latch Sense Amplifier circuits, a) CLSA b) VLSA	22
3.2	Correct sensing operation of CLSA	23
3.3	Wrong sensing in CLSA due to V_t mismatch	24
3.4	Yield vs. V_t mismatch for CLSA and VLSA	25
3.5	New schematic for compensation technique	26
3.6	Correct sensing in CCLSA circuit	27
3.7	Charging of back-gate of X7	28
3.8	Yield comparisons for different sense amplifiers	29
3.9	Yield comparisons of IGSSA and CCLSA	30
3.10	Comparison of yield at 32nm node	30
3.11	Sense delays for compensated CLSA	30
4.1	Schematic for independent gate sense amplifier (IGSA)	33
4.2	Schematic of directly translated CLSA	34
4.3	Correct sensing operation of IGSA	34
4.4	Delay comparisons of CLSA and IGSA	35
4.5	Average power dissipation of CLSA and IGSA	36
4.6	Yield comparisons of CLSA and IGSA	36
4.7	New schematic for compensation technique for IGSA	37
4.8	Correct sensing in CCLSA circuit	38
4.9	Yield comparisons for different sense amplifiers	39
4.10	Sense delays for IGSA and CIGSA	39

4.11	Sense delays for CCLSA and CIGSA	40
4.12	Schematic of Latch Based Sense Amplifier (LBSA)	41
4.13	Sensing in Latch Based Sense Amplifier (LBSA)	41
4.14	Yield vs. V_t mismatch for CLSA, IGSA and LBSA	42
4.15	New schematic for compensation technique for LBSA	43
4.16	Yield comparisons for LBSA and CLBSA	44
4.17	Sense delays for IGSA and CIGSA	44
4.18	Average power dissipation of LBSA and CLBSA	45
5.1	Yield graphs for compensated and uncompensated designs	47
5.2	Delay variations for compensated and uncompensated designs	47
5.3	Power dissipations for compensated and uncompensated designs	47

ABBREVIATIONS

BL	Bit-Line
CAS	Column Address Strobe
CCLSA	Compensated Current Latch Sense Amplifier
CIGSA	Compensated Independent Gate Sense Amplifier
CLBSA	Compensated Latch Based Sense Amplifier
CLSA	Current Latch Sense Amplifier
CMOS	Complementary Metal Oxide Semiconductor
DRAM	Dynamic Random Access Memory
GIDL	Gate Induced Drain Leakage
IGSA	Independent Gate Sense Amplifier
IGSSA	Independent Gate Self-compensated Sense Amplifier
I/O	Input/output
ITRS	International Technology Roadmap for Semiconductor
JEDEC	Joint Electron Device Engineering Council
LBSA	Latch Based Sense Amplifier
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
OUT	Output
PTM	Predictive Technology Model
RAM	Random Access Memory
RAS	Row Access Strobe
SDVT	Semiconductor Devices and VLSI Technology
SEN	Sensing Enable
SIA	Semiconductor Industry Association
SN	Sense NMOS
SOI	Silicon On Insulator
SP	Sense PMOS
SRAM	Random Access Memory
VLSA	Voltage Latch Sense Amplifier
VLSI	Very Large Scale Integration

CHAPTER 1 INTRODUCTION

1.1 Background

DRAMs have the huge production volume in VLSI semiconductor products, and the DRAM market is one of the most competitive in the semiconductor industry. Maximizing the number of chips per wafer, improving the process yield, and simultaneously minimizing the process complexity and cost are mandatory for DRAM manufacturers. Traditionally, this demand for low-cost processes has caused DRAM transistor performance to lag that of high performance logic. Manufacturers try to meet the recent demand for higher DRAM performance mainly by DRAM architecture changes, but in future also an improved transistor performance may be needed. Emerging embedded applications require compatibility with complex logic processes in general. [1]

Variations in transistor characteristics and particularly in threshold voltage (V_t) have emerged as a major challenge for circuit design in scaled technologies. Process variations result in increased mismatch among neighbouring transistors which can affect the correct functionality of circuits such as sense amplifiers. In this work, the impact of process variations on sense amplifier circuits has been simulated and studied in detail. A double gate FinFET device in 45nm/32nm technology is used as a device of choice in implementing the desired approach.

With the emerging nanoscale devices, SIA roadmap identifies FinFET as a candidate for post-planar end-of-roadmap CMOS device. Lithography related critical dimension variations, fluctuations in dopant density, oxide thickness and parametric variations of devices are identified as a major challenge to the classical bulk type MOSFET in ITRS. The device and process variations cause failures in circuits which result in critical yield loss. Due to growth in size of embedded DRAMs as well as usage of sense amplifier based signalling techniques, process variations in sense amplifiers lead to significant loss of yield. In this work, FinFETs based sense amplifier design has been carried out, that exploits the backgate of FinFET devices for dynamic compensation against process variation. Results from statistical simulation show that the proposed dynamic

compensation is highly effective in restoring yield at a level comparable to that of sense amplifiers without significant process variations. [2]

By scaling down of CMOS technology, transistor parameters such as channel length (L), width (W), oxide thickness (t_{ox}) and threshold voltage (V_t) scale down. However, variability in process parameters increases with technology scaling, resulting in unpredictability of circuit responses such as delay and power dissipation. Random dopant fluctuation is emerging as a major cause of intra-die random variations in threshold voltage of transistors in scaled technologies. Under random dopant fluctuations, even two adjacent transistors can have different threshold voltages which lead to functional failures in circuits that rely on matched transistors such as DRAM cells and sense amplifiers. [3]

The FinFET technology is the most promising among the alternatives to conventional bulk CMOS. FinFETs increase drive current through larger gate area while they reduce sub-threshold leakage through reduced channel doping. FinFETs have been successfully fabricated by multiple laboratories. A FinFET is a vertical double gate device that is promising below 45nm technology. Motivated by these considerations, FinFET is chosen as a device of choice to solve the yield problem.

Several FinFET structures have been proposed. For this work a dual-gate FinFET structure with independent gate controls has been considered. In a dual-gate FinFET, the second gate may be biased in a way that changes the threshold voltage for the first gate, similar to the effect of body in bulk CMOS. Advantage of this property has been taken for compensating against process variations.

1.2 Thesis Contribution

The aim of this thesis is to design FinFET based sense amplifiers intended to work under FinFET based DRAM cell. The designed sense amplifier should be tolerant to threshold voltage (V_t) variation in critical devices. This is primarily attributed to parametric variations of devices i.e. length and width, oxide thickness, random dopant fluctuations etc. This design of sense amplifier has been compared with the benchmark circuits and compared based on metrics such as yield gain and sense delay. These are the two

primary metrics for any good sense amplifier design. The objectives of thesis are following:

- Study the basic operation of the DRAM cell along with its architecture and peripheral circuitry.
- Advantages of the double gate FinFET technology over the conventional CMOS bulk technology.
- Understanding of the working of different types of sense amplifier circuits which are being used in the embedded memories.
- Simulation of process variations in Synopsys' HSPICE for sense amplifiers' circuits.
- Design of CLSA (Current-latched sense amplifier) circuit for 45nm double gate FinFET technology node using PTM (Predictive Technology Model) files.
- Design of IGSA (Independent gate sense amplifier) circuit for 45nm double gate FinFET technology node in PTM (Predictive Technology Model) files.
- Finally yield gain and delay of the designed circuits are calculated and compared with the benchmark circuits based on the defined metrics.

1.3 Thesis Organization

The thesis is organized as follows:

In Chapter 2 basic operation of the DRAM cell is explained along with its architecture and peripheral circuitry. Various leakage mechanisms are explained and the limitations of the current bulk technology are summarized. FinFET technology is explained in the perspective of the DRAM and sense amplifiers along with its advantages over the current bulk technology.

Chapter 3 presents the design of process variation tolerant sense amplifier. Simulation results of process variation in sense amplifier circuit are presented.

In Chapter 4 IGSA (Independent Gate Sense Amplifier) design is presented. Results from Monte-Carlo simulations are reported and compared with the benchmark circuit.

Finally Chapter 5 concludes the thesis and discusses future scope of work.

CHAPTER 2 BASICS OF DRAM CELL

2.1 DRAM Structure and Operation

Figure 2.1 shows the architecture of a DRAM chip, with data and control signal paths. DRAM signal timing during read operation is shown in Figure 2.2. Row and column addresses decoded from the input determine the X and Y co-ordinates of the memory cell to be addressed. These addresses are time multiplexed to minimize the number of address pins. The RAS (Row address strobe) and CAS (Column address strobe) are typically active low signals. The row address is input first, and is latched by the falling edge of the $\overline{RAS}$, then the column address is latched by the falling edge of $\overline{CAS}$. The $\overline{CAS}$ signal also enables the output buffer. Row address selects a word line, which connects a memory cell to the bit line, establishing a signal on the bit line. The sense amplifier detects the signal and the column decoder connects it to an I/O line. The amplified signal from the sense amplifier is transferred to the data output buffer and subsequently data appears at the output at the falling edge of $\overline{CAS}$. Time from the falling edge of $\overline{CAS}$ to data out is called CAS access time and the time from the falling edge of $\overline{RAS}$ to data out is called the RAS access time. During the write operation, the data paths of the I/O lines are reversed. The row path, which selects the word lines are the same as for the read operation. [4]

Both read and write operations use the same path. However, the write operation bypasses the sense amplifier. Data to be written to the memory cell passes through the input buffers and onto the data bus. Signals are transferred to the bit-lines through a write select pass gate and are written to the memory cell by activating the word lines. The write operation is signalled by $\overline{WE}$ low and is high for 'READ'.

Once a word line is activated, all sense amplifiers associated with the memory cells connected to that word line are activated regardless of the data line connected to the I/O line. Depending on the memory density and division of blocks in the array, the number of sense amplifiers activated simultaneously varies depending on the number of banks and sub-blocks within a bank. Data is available on the sense amplifier outputs and transferred to the I/O lines with a select signal. Different architectures may be used to minimize the number of active sense amplifiers and cells in a sub-block. [4]

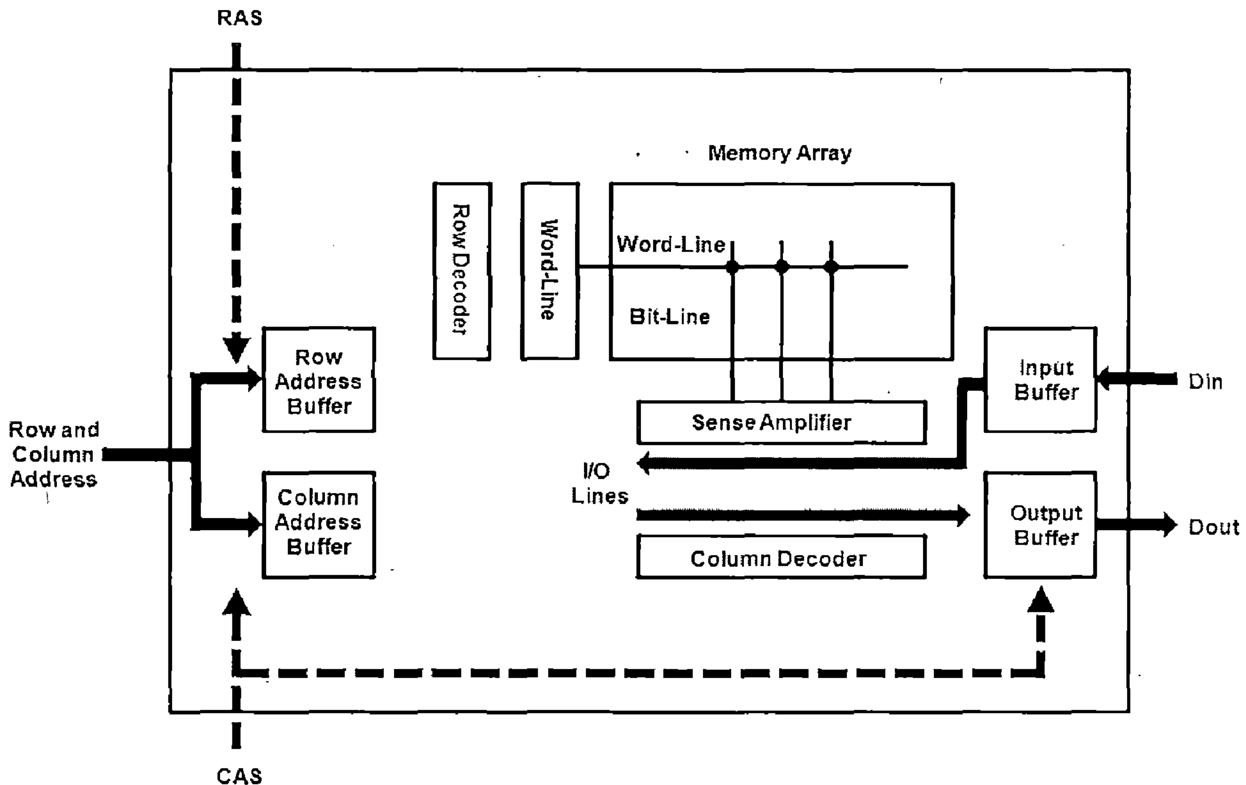


Figure 2.1 Architectural block diagram of a DRAM critical path.

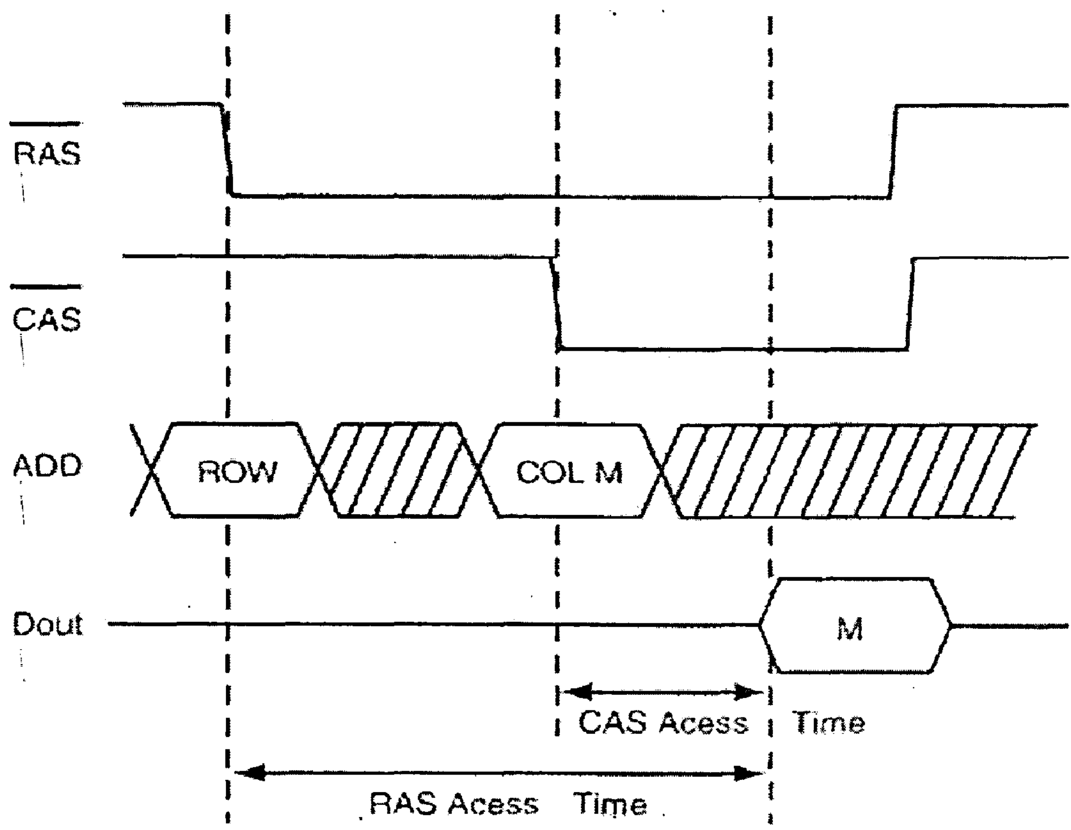


Figure 2.2 Signal timing diagram in DRAMs.

2.1.1 Memory Array

The simplest array architecture forms a memory cell wherever a word line and bit line cross each other. Since a pair of bit lines must be connected to a sense amplifier for data comparison, this architecture results in an open bit line configuration as shown in Figure 2.3 (a). When one of the word lines on the right side is selected, none of the word lines on the left side is selected. The left-side bit line with no connected memory cell serves as a reference for the right side bit line. There are disadvantages with the open bit line configuration. The sense amplifier circuit layout must fit into the narrow pitch of a cell bit line (sum of line width and spacing). This is difficult, because memory cell size and cell pitch decrease with successive generations of DRAM. A solution is to use a relaxed sense amplifier pitch open bit line architecture as shown in Figure 2.3 (b). Open bit line architecture also exhibits poor noise immunity. Localized noise in the array couples onto one side of the bit line pairs and degrades the sense amplifier differential input signal.

Localized noise coupling in the array may be avoided by the use of a folded bit line approach as shown in Figure 2.3 (c). BL and $\overline{BL}$ extend parallel from the sense amplifier. Localized noise couples onto both bit lines and is cancelled by the differential operation of the sense amplifier. Thus, the sense amplifier can detect a smaller differential signal from the memory cell in a folded bit line configuration [4].

2.1.2 Dynamic Random Access Memory Cell Storage

A variety of dynamic RAM cells are shown in Figure 2.4. Most of these use a capacitor as the storage element, although gate/source capacitance is used to store charge in the circuits shown in Figures 2.4 (a) and (d). Stored charge tends to leak away with time. As a result, data must be refreshed periodically with the original '0' or '1' level stored in the cell. [5]

The evolution of these cells began with the four-transistor dynamic memory cell shown in Figure 2.4(a). This cell is derived from the six-transistor static memory cell by removing the load devices. Since current is no longer supplied to the storage nodes to replace that lost to leakage, the cell must be periodically refreshed. This cell is activated using a clock pulse to the two access transistors. Since the charge eventually leaks off, the cell must be reactivated to refresh the data.

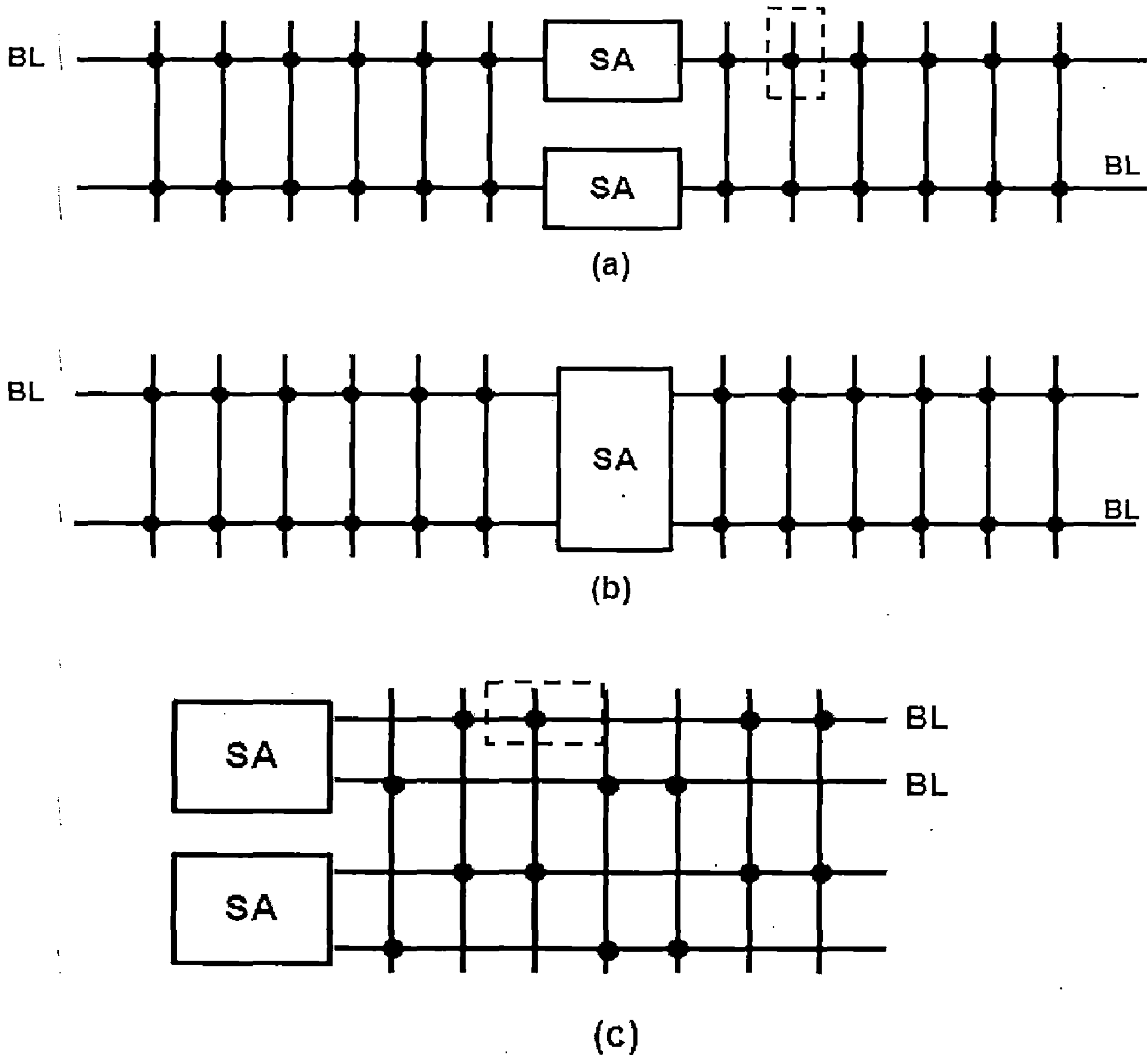


Figure 2.3 Bit line configurations in DRAMs a) open bit line b) relaxed sense amplifier pitch open bit line c) Folded bit line. The dotted regions represent the memory cell.

Figure 2.4(e) shows the conventional one transistor dynamic memory cell, which consists of a transistor and storage capacitor [6]. The biggest advantage of 1T DRAM cell is dramatic reduction in cell complexity as compared to the 3T and 4T DRAM cells and hence saving of chip area. Also unlike the 3T cell that relies on charge storage on a gate capacitance, the 1T cell requires the presence of an extra capacitance that must be explicitly included in the design. The gate of the transistor is controlled by a word-line. When the word line is enabled the select transistor turns 'on' and the charge stored is transferred onto the bit lines and then to a sense amplifier.

The sense amplifier compares it with a reference cell and determines if the DRAM cell contains a stored '1' or '0'. The read out from the cell discharges the capacitor so that

the data is no longer stored in the cell. Before the read operation is complete, the sense amplifier circuit must restore the original charge to the cell.

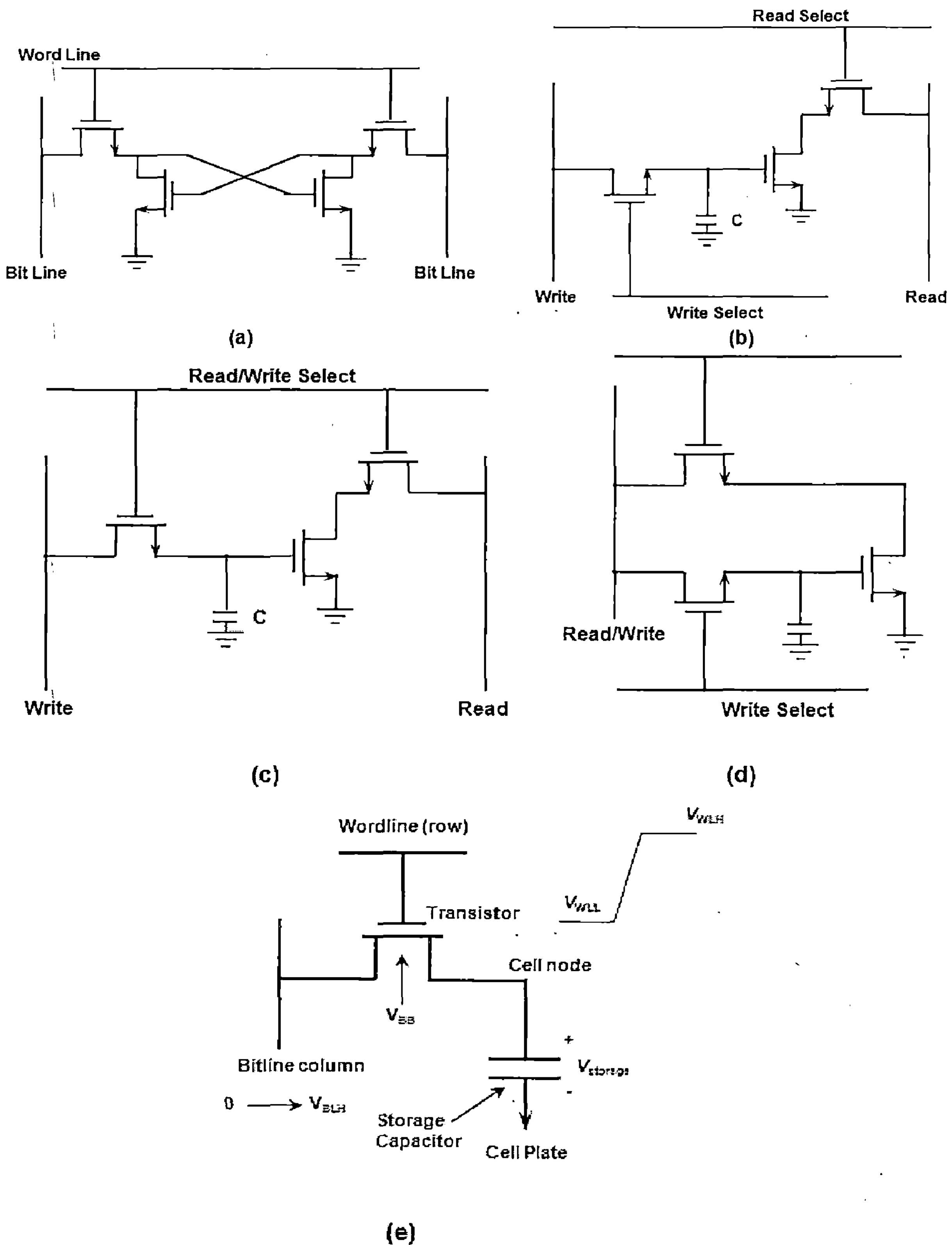


Figure 2.4 (a)-(e) Various DRAM cell structures

Although area efficient, the major problems of the 1T DRAM cell have been to ensure sufficient charge storage in the cell and designing small sense amplifiers to fit into the area between the bit-lines.

2.1.3 Storage to Bit Line Capacitance

The storage capacitance to bit line capacitance ratio is one of the most important characteristics of the 1T DRAM. Sufficient charge must be stored on the capacitor to provide a readable signal to the sense amplifier.

The parasitic bit line capacitance (C_b) is typically larger than the capacitance of the storage cell (C_s) due to a large number of cells present on a single bit-line. When the cell is selected and the signal stored in the cell capacitor (V_s) is read out onto the bit line, it is reduced by the ratio of the storage capacitance to the bit line parasitic capacitance. The signal magnitude on the bit lines (V_b) is, therefore, frequently described by the ratio, i.e., $C_s/C_b = V_b/V_s$ or $V_b = V_s\ (C_s/C_b)$. The bit line capacitance includes the junction and the source/drain capacitance of all the inactive cells on the same column.

The bit line capacitance C_b/C_s is determined by technology. The total value of C_b is strongly influenced by the number of storage cells on a bit line. C_b degrades the storage cell signal and hence the bit line signal has to be amplified by a sense amplifier, which must also be able to refresh the information of the selected cell. The more sensitive the amplifier is, the smaller the storage capacitance. If the bit line capacitance is large relative to the capacitance of the memory cell then, the signal across the bit lines and the signal available to the sense amplifier will be too small to be read. For example, if the C_b to C_s ratio is 10, and the voltage stored on the storage capacitor has decayed to 2V at the time the cell is read, the signal which is read out onto the bit line will be reduced by 1/10 to 200mV. The sense amplifier design is critical to DRAMs and must be sensitive enough to read this signal. Mismatches in the devices have to be taken into consideration to obtain efficient, fast and reliable sense amplifiers.

2.1.4 Static Data Retention

Some common leakage mechanisms that affect charge storage in static data retention schemes or circuits are [9]:

- Junction Leakage
- Pass transistor sub-threshold leakage
- Leakage through capacitor dielectric
- Other parasitic leakage paths

Junction Leakage

The p-n junction that makes the storage capacitor in the DRAM memory cell is always reverse biased or biased at ground. Leakage current through a reverse biased P-N junction can be expressed by the sum of the diffusion and the generation-recombination current as:

$$J_R = \frac{qD_P p_{n0}}{L_p} + \frac{qD_N n_{p0}}{L_N} + \frac{qn_i W}{\tau_e} \qquad \ldots(2.1)$$

The first two components are the diffusion current, and the third term is the generation-recombination current. Here, D_P and D_N are the diffusion coefficients of holes and electrons, respectively; L_p, L_n are the diffusion length of holes and electrons respectively; p_{n0} and n_{p0} are the equilibrium hole density on the 'n' side and electron density on the 'p' side; n_i is the intrinsic carrier concentration. W is the depletion width and τ_e is the effective carrier lifetime in the depletion region. The generation-recombination current is dominant in most cases; however, at zero bias conditions and high temperatures, diffusion current is higher. Diffusion current typically has activation energy of E_g, the band-gap energy of silicon, whereas the generation-recombination current has activation energy of about $E_g/2$.

Pass transistor subthreshold leakage

Even when the word line voltage is low (at ground) and the pass transistor is in OFF mode, a small amount of current flows through the pass transistor below its threshold voltage. This is called a subthreshold current, and is given as:

$$I_S = I_T \exp\frac{-qV_{th}}{mkT} \qquad \ldots(2.2)$$

where I_T is the drain current at the threshold voltage, V_{th} is the threshold voltage, and m is a measure of the subthreshold slope parameter, S (mV/decade) by

$$m = \frac{0.001 \times qS}{kT \ln 10} \qquad \ldots(2.3)$$

The transistor subthreshold current can be significant if the threshold voltage of the pass transistor is designed at too low a value.

Leakage through the Capacitor Dielectric

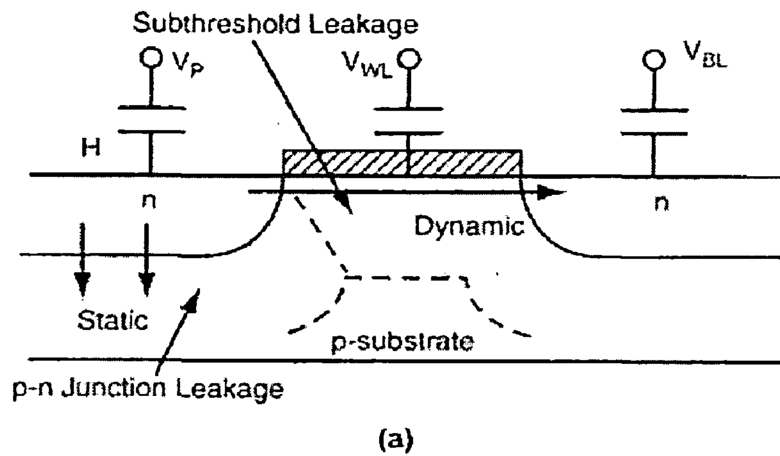
Although a capacitor dielectric is normally considered an insulating film, it conducts some current especially at high bias voltage or when very thin. When the bias voltage exceeds the breakdown voltage of the dielectric film, the film becomes conductive and leakage current increases significantly. Below the breakdown voltage, leakage is either Frenkel-Poole or Fowler-Nordheim. Frenkel-Poole leakage is due to field enhanced thermal excitation of trapped electrons in the conduction band, whereas, the Fowler-Nordheim current is caused by electron tunnelling.

Other parasitic leakage paths

In addition to these three mechanisms, there are some other parasitic leakage mechanisms some of which may be specific to the cell structure. One is a vertical parasitic MOS transistor that can leak the stored charge if the well doping concentration is not sufficiently high. Another is a trench-gated-diode leakage between the n-well and p^+ substrate.

In DRAMs the highest electric field in the drain–body junction occurs at the edge overlapped by the gate, where the full drain–gate voltage appears across the insulator and a depleted portion of the drain. GIDL is another leakage mechanism in which this high field can cause band-to-band tunnelling in regions where the bandgap voltage is dropped across a sufficiently small distance. For either direct or trap-assisted band-to-band tunnelling to be a significant contributor to leakage, the high field must occur over a distance of less than about 10 nm.

The static data retention limit occurs during refresh when the bit line of the unselected cell is precharged to $V_{DD}/2$ and is primarily due to junction leakage. Leakage mechanisms are shown in Figure 2.5 for bulk DRAM cell. [9]



(a)

Figure 2.5 Leakage mechanisms for bulk-Si DRAM cell.

2.1.5 Data Sensing

In an integrated memory circuit "sensing" means the detection and determination of the data content of a selected memory cell. The sensing may be "nondestructive," when the data content of the selected memory cell is unchanged (e.g., in SRAMs, ROMs, PROMS, etc.), and "destructive," when the data content of the selected memory cell may be altered (e.g., in DRAMS, etc.) by the sense operation.

Sensing is performed in a sense circuit. Typical sense circuits are mirror-symmetrical in structure and may comprise (1) a sense amplifier, (2) circuits which support the sense operation such as precharge, reference and load circuits, (3) an accessed memory cell, and (4) parasitic elements including the distributed capacitances of memory cells connected to the bit line.

Because the effective bitline capacitances and the cell-access resistances are large, and because a memory cell's energy output is small at read operations, an accessed memory cell can generate only small current and voltage signals. These signals have long switching and propagation times and insufficient amplitudes to provide the logic '0' and logic '1' levels which are required to drive the peripheral logic circuits of the memory.

To improve the speed performance of a memory, and to provide signals which conform to the requirements of driving peripheral circuits within the memory, sense amplifiers are applied.

2.1.6 Positive-Feedback Differential Voltage Sense Amplifier

The full-complementary positive feedback sense amplifier uses an active load circuit constructed of devices MP4, MP5 and MP6 in positive feedback configuration as shown in Figure 2.6. [23]

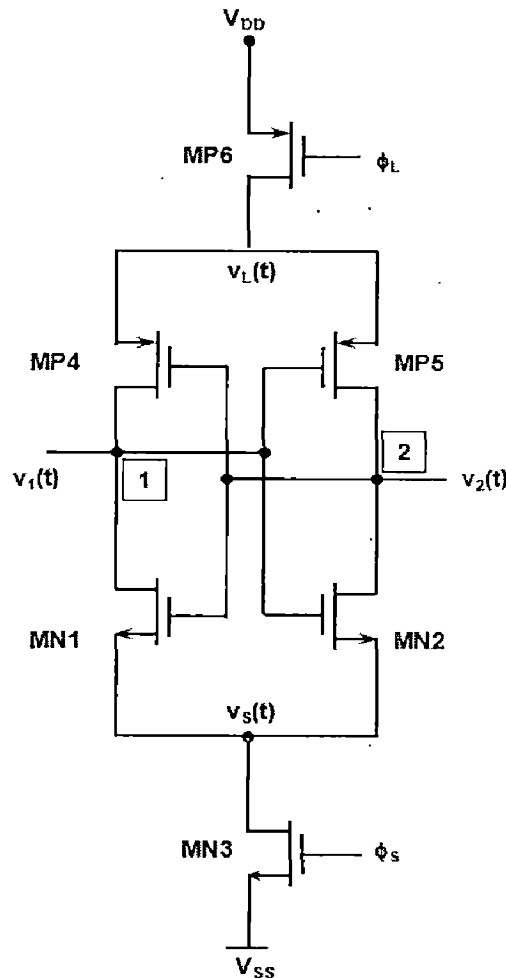


Figure 2.6 Full-complementary positive-feedback sense amplifier circuit.

In practice, device pairs MP4-MP5 and MN1-MN2 in Figure 2.6 cannot be matched completely despite carefully symmetrical design. Usually the mismatch between the p-channel MP4 and MP5 is more substantial than that between the n-channel MN1 and MN2, because most of the CMOS processes optimize n-channel device characteristics. To avoid a large initial offset resulting from the added effects of imbalances in the n-channel and p-channel device pair, source devices MN3 and MP6 are not turned on simultaneously, but first the n-channel device and later the p-channel is activated by control signals ϕ_S and ϕ_L respectively.

In the transient analysis, the differential signal development time t_d during the presence of impulse ϕ_S until the appearance of clock ϕ_L is determined by the switching time t_{dN} of the n-channel triad (MN3, MN2, MN1), and thereafter t_d is dominated by the transient time t_{dP} of the p-channel triad (MP4, MP5, MP6).

The sense-signal development time in full-complementary positive feedback differential voltage sense amplifier t_d may be approached as [23]:

$$t_d = t_{dN} + t_{dP} = \tau_{dN} \ln \frac{V_{DSAT}}{2\Delta V_0} + \tau_{dP} \ln \frac{0.9(V_{DD} - V_{PR})}{V_{DSAT}} \quad \ldots(2.4)$$

$$\tau_{dN} \approx \frac{C_B + C_{GSN} + 4C_{GDN}}{\beta_N [V_{PR} - v_s(0) - V_{TN}(V_{BG})]} \quad \tau_{dP} \approx \frac{C_B + C_{GSP} + 4C_{GDP}}{\beta_P [v_L(0) - V_{PR} - |V_{TP}(V_{BG})|]} \quad \ldots(2.5)$$

The indices N and P designate n-channel and p-channel devices, V_{DSAT} is the saturation voltage, ΔV_o is the amplitude of the initial voltage difference generated by the accessed memory cell on nodes 1 and 2 , V_{PR} is the precharge voltage, C_B is the bitline capacitance, C_{GS} and C_{GD} are the gate-source and gate-drain capacitances, and β is the individual gain factor for devices MN1, MN2, MP4 and MP5, $v_S(0)$ and $v_L(0)$ are the initial potentials on the drains of device MN3 and MP6, V_T is the threshold voltage and V_{BG} is the backgate bias.

The equation (2.4) for t_d demonstrate that in full-complementary positive feedback differential sense amplifier quicker operation can be obtained by increasing the gain factors β_N and β_P, by decreasing the parasitic gate-source capacitance C_{GS} and gate-drain capacitance C_{GD} of the n-channel and p-channel latch devices MN1, MN2, MP4 and MP5, and by decreasing the bitline capacitance C_{BL}. Additionally, reductions in the fall time of v_S (t) and in the rise time of $v_r(t)$ also shorten t_d.

The sensitivity of sense amplifier is defined as the minimum voltage difference on the bitlines which can be faithfully amplified to the full voltage swing. It depends on the rate at which the enable signal ϕ_S is fired. The slower the ϕ_S, the smaller signal sense amplifier can detect. The relationship between time for signal ϕ_S to go low, or the latch time T, and the sensitivity v of the sense amplifier, is given by [4]:

$$T = \frac{2C_B(V_{TN} - fv)}{\beta . f^2 V_{TN} v} \quad \ldots(2.6)$$

Here C_B is total bit line capacitance, V_{TN} is threshold voltage of n-channel device and $f = C_B/(C_B+C_G)$, where C_G is the gate oxide capacitance of transistor MN1 and β is the gain of MN1. Hence sensitivity v is inversely proportional to the latch time T.

2.1.7 Positive Feedback Current Sense Amplifier

The fundamental reason for applying current-mode sense amplifiers in sense circuits is their small input impedances and, in cross-coupled feedback configuration, their small common input/output impedances. Benefits of small input and input/output impedances, which are coupled to a bitline, include significant reductions in sense circuit delays, voltage swings, cross-talks, substrate currents and substrate voltage modulations.

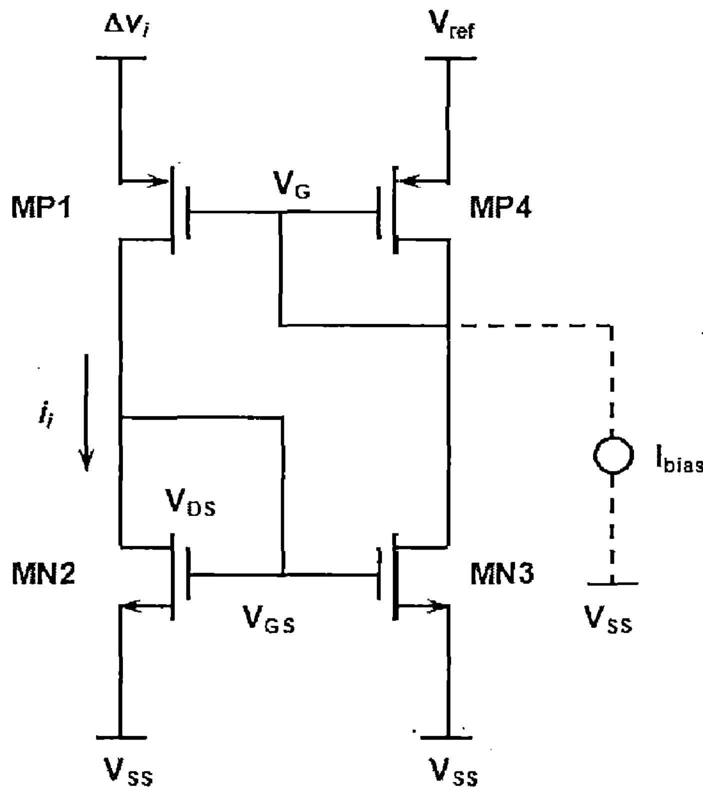


Figure 2.7 Simple positive feedback current sense amplifier

Very small input resistance and some built-in compensation of offsets can be provided by connecting two identical primitive current mirror amplifiers in positive feedback configuration as shown in Figure 2.7 [23] in which the closed loop gain is unity or less. In this configuration when an input voltage Δv_i increases, then the input current i_i rises

and the drain-source voltage V_{DS} becomes greater. Since $V_{DS} = V_{GS}$ in MN2, the increased V_{GS} tends to increase the current drive capability of MN2 and, thereby, to decrease V_{DS} of MN2. The current of MN2 is mirrored to MN3, and the effective gate voltage $|V_G - V_{ref}|$ of MP4 grows. Here, V_G is the gate voltage of MP1 and MP4, and V_{ref} is the reference voltage. Nonetheless, a larger $|V_G - V_{ref}|$ lowers the drain-source resistances r_{ds} of MP4 and MP1, and thus the gain in both $|V_G - V_{ref}|$ and Δv_i get attenuated while a considerable current change occurs. Since the closed loop gain is designed to be less than unity, the circuit is stable. To provide near unity gain and minimum offsets all four devices MP1, MN2, MN3 and MP4 have same gain factor β.

The positive feedback in MP1, MN2, MN3 and MN4 results also in an offset compensation effect. Namely, the feedback mechanism keeps not only the memory cell generated input voltage swing Δv_i at very small amplitude, but compensates also the circuit imbalance induced offset voltage V_{off}. Here, V_{off} is the offset voltage without the positive feedback. To demonstrate the effect of positive feedback on V_{off} the total of the parameter imbalances may arbitrarily be combined in a single term ΔV_T, and the offset voltage with positive feedback $V_{off}^{(+)}$ can be approximated by [23]

$$V_{off}^{\ +} \approx V_{off} + \left(1 + \frac{g_{m2}}{g_{m1}}.A - \frac{g_{m3}}{g_{m1}}.\frac{1-A}{1-\frac{g_{m3}}{g_{m2}}}\right)\Delta V_T \qquad \ldots(2.1)$$

The reduced offset voltage $V_{off}^{(+)} << V_{off}$ allows for sensing of smaller input signals imbalances, the sensing can start earlier, and the total sense time becomes shorter.

2.2 FinFET SOI Technology

Conventional bulk CMOS scaling beyond 45nm is severely constrained by short channel effects and gate insulator tunnelling. FinFET technology has been proposed as a promising alternative for deep sub-micron bulk CMOS technology, because of its better scalability. Double-gate FinFET technology is a very promising candidate to circumvent the conventional bulk CMOS scaling constraint, by changing the device structure in such a way that MOSFET gate length can be scaled further even with thicker oxide, so that we can continue scaling beyond the limit of conventional bulk CMOS.

One of the promising technologies that are capable of facilitating current DRAM trends is the SOI (Silicon On Insulator) technology. The SOI technology offers many potential benefits in terms of both power and performance over the traditional bulk CMOS technology. The benefits in power are especially attractive in light of the numerous emerging applications for low power electronics. FinFETs based on SOI technology may be promising candidate for the future DRAM trends.

2.2.1 SOI Technology in General

SOI is fabricated by implanting a thin layer of oxide beneath the silicon surface. (see Figure 2.8 [9]) When the silicon thickness is smaller than the depletion depth under the inversion channel, the SOI MOSFETs are said to be fully depleted (FD); otherwise, partially depleted (PD). FD SOI is much more difficult to manufacture because very thin (< 35nm) silicon layers are required to achieve optimized sub 0.18 mm FD devices, while only a 100 nm layer of silicon is needed for PD devices.

There are several advantages of SOI CMOS technology over conventional bulk CMOS technology:

1) Due to the elimination of the source/drain-substrate junction in bulk CMOS, the junction capacitance is significantly reduced.

2) Hence a reduction of dynamic power spent charging capacitors.

3) Because of their electrical isolation, they do not exhibit the conventional body-effect that decreases current drive in stacked devices.

4) When their body floats, it couples to the gate potential resulting in a higher on/off current ratio, and therefore they are more suitable for reduced V_{DD} operation at given performance.

2.2.2 FinFET in SOI Technology

Figure 2.9 shows the structure of multi-fin double-gate FinFET devices [11]. Double gate FinFET consists of two SOI gates connected together. The thickness (T_{si}) of a single fin equals to silicon channel thickness. The current flows from the source to drain along the wafer plane. Each fin provides 2H of device width, where H is the height of the each fin. For the FinFET devices, widths are quantized into units of the fins. Large width of device is obtained by using multiple fins.

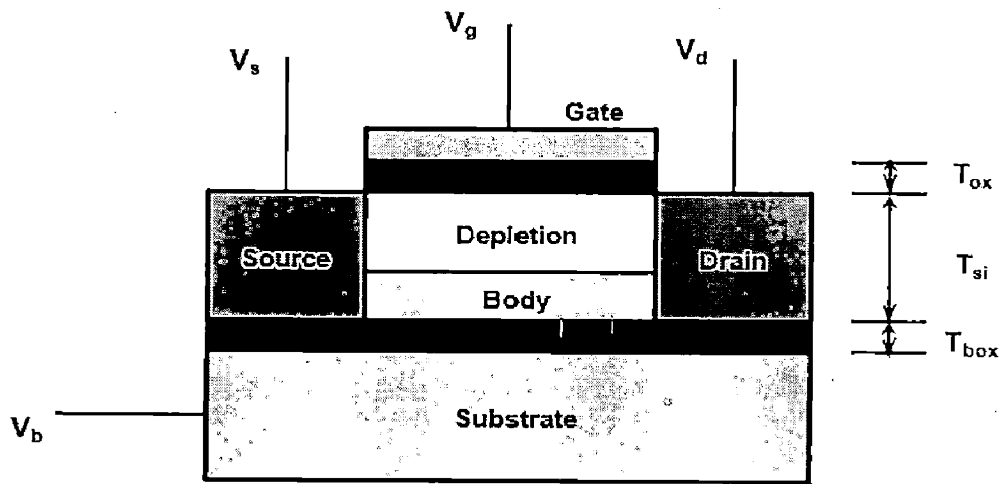


Figure 2.8 Bisection of SOI MOSFET

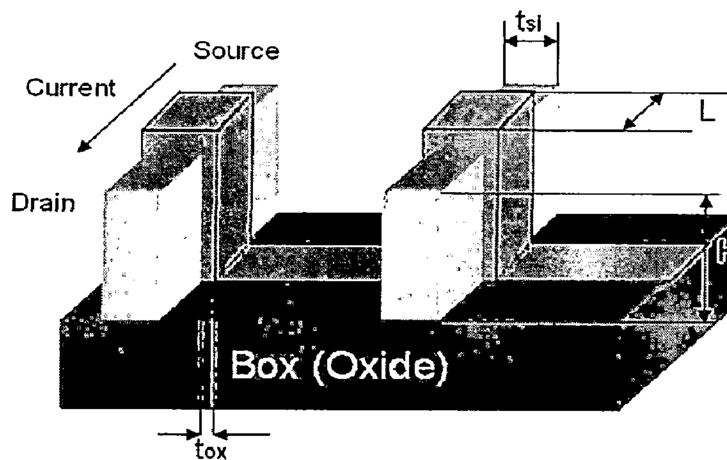


Figure 2.9 Multiple-fin FinFET structure

2.2.3 Advantages of SOI for DRAM

Here the related SOI features that benefit the DRAM design for both low voltage and low leakage power are listed:

- Small junction capacitance/area
- Small substrate bias effect
- Complete body isolation
- Small body capacitance

SOI DRAMs have several advantages over bulk DRAMs:

a) Reduction of the bit-line capacitance (by 25% compared to bulk)
b) Reduction of the access transistor leakage current

c) Reduction of soft error sensitivity.

Storage capacitance in SOI is around 55% lower than in bulk. Reduction of bit line capacitance is a natural convergence of the transfer to SOI, while increase in storage capacitance is achieved through cell design. Thin-film SOI MOSFET's have much lower leakage than bulk or thicker SOI devices. The off-state leakage current lower than 1fA/μm has been observed in fully depleted SOI. This is important as retention time is a function of storage capacitance and leakage. The lower the leakage is, the longer the retention time.

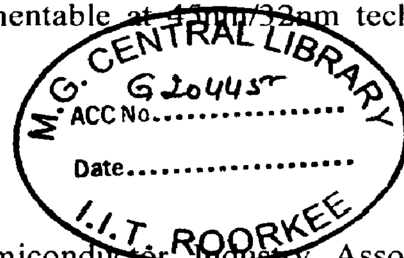
The progress in DRAM technology has thus far covered a long distance. Over the past decade, advancements in DRAM cell technologies have enabled denser, larger memories structures without sacrificing much in power and performance. Starting from the four-transistor dynamic memory cell, it has reached present day's 1T DRAM memory cell. As compared to the bulk technology which was extensively used in the earlier DRAM generations, now the paradigm is shifting towards the FinFET technology. This trend gives immense scope for one to work on DRAM cell design based on SOI-FinFET technology. [1] [9]

Above advantages summed up together poses FinFET a better option for future DRAM generation. FinFET built on SOI technology is a potential candidate for future DRAM cell. It will prove useful for the future DRAM cell design.

CHAPTER 3 VARIATIONS STUDY AND RESULTS OF FINFET BASED SENSE AMPLIFIERS

3.1 Abstract

Process variations inducing transistor characteristics mismatch have emerged as major challenge to nanoscale circuit design leading to failure of circuits, such as sense amplifiers. In this chapter, a modified current latch sense amplifier having high tolerance to process variations has been presented. The circuit designed with double gate FinFET technology, utilizes an improved self compensation technique to overcome variations in transistor characteristics. The simulations of transistor mismatch (threshold voltage, V_t) using Monte-Carlo simulation technique show that, the proposed circuit performs correct circuit functionality for worst case V_t mismatch of 50mV. This design offers up to 30% higher yield compared to uncompensated circuit. The design has a minimal penalty for circuit complexity and speed, and is easily implementable at 45nm/32nm technology node.



3.2 Introduction

With the emerging nanoscale devices, SIA (Semiconductor Industry Association) roadmap identifies FinFET as a candidate for post-planar end-of-roadmap CMOS device. As the device dimension scales below 100nm, process variations emerge as a significant design concern [12]. Embedded memories use sense amplifier for fast sensing. Typically, sense amplifiers use a pair of matched transistors in a positive feedback environment. A small difference in voltage level of applied input signals to these matched transistors is amplified and the resulting logic signals are latched.

Intra-die variations due to lithography related critical dimension variations, fluctuations in dopant density, oxide thickness and parametric variations of devices are the main causes of mismatch in scaled technology. They causes mismatch in the threshold voltages between the sense transistors that should ideally be identical structures. If this difference is sufficient to overcome differential voltage developed on the bit-lines of the sense amplifier then sense amplifier may latch incorrect signal, and hence functionality of the circuit is affected. Since a typical chip may contain hundreds of thousands of

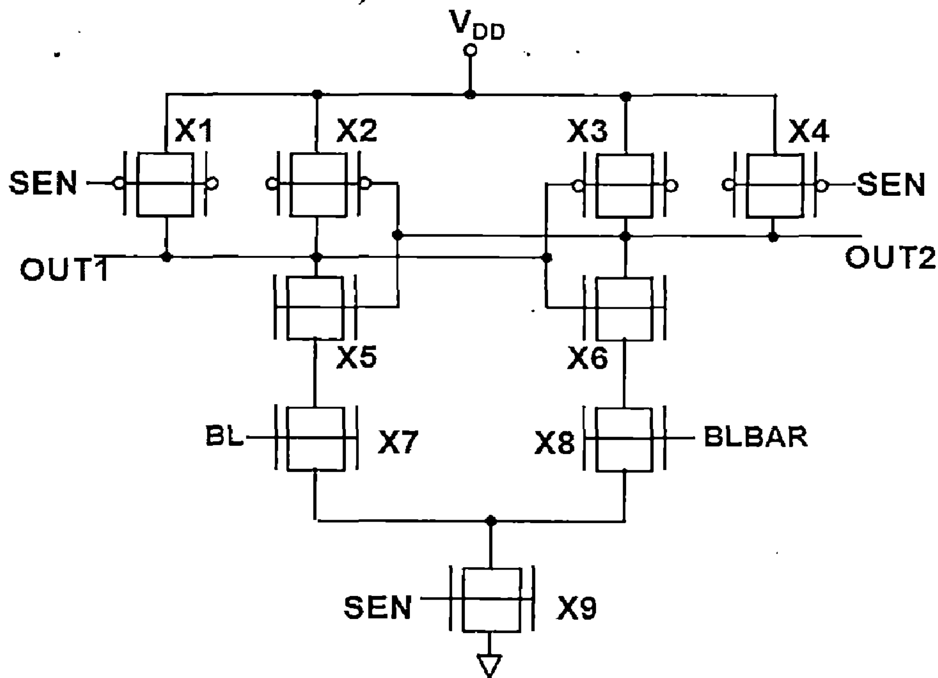
sense amplifiers, and if some sense amplifier results in malfunctioning then it causes loss of yield. This necessitates design of robust sense amplifiers that have lower failure probability against process variations.

The FinFET technology is the most promising among the alternatives to conventional bulk CMOS. FinFET increases drive current through larger gate area while it reduces sub-threshold leakage through reduced channel doping. A FinFET is a vertical double gate device that is promising below 45nm technology [13] [14]. Motivated by these considerations, FinFET is thought of as a device of choice to solve the scaling and process variation challenges present in current bulk MOSFET.

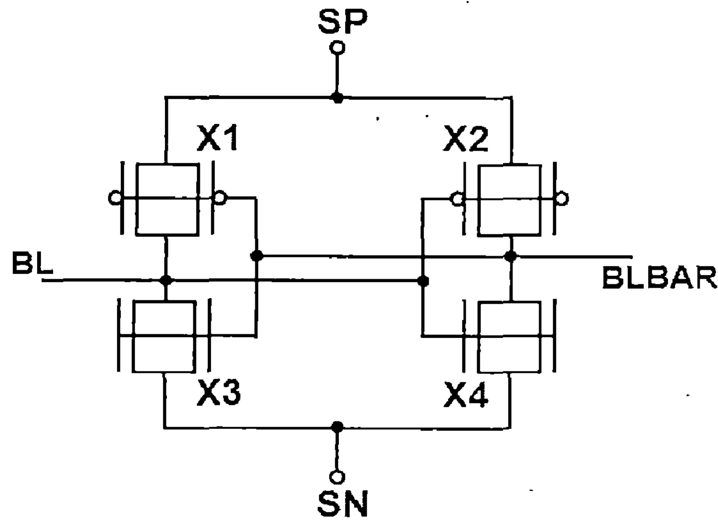
For the sense amplifier and other support circuits to work properly at reduced voltage requires the scaling of the V_t of those devices. This causes the same types of off-current problems faced today in scaled logic devices, where techniques are being developed to minimize the impact on standby power. Such low-V_t devices are very achievable for DRAM embedded in a high-performance logic technology base, but until now they have not been considered affordable for industry-standard DRAM. Alternatively, different sensing circuits may be developed for lower-voltage operation [15] [16]. Ultimately, current-sensing techniques would be ideal at very low voltages to obtain the full charge from the capacitor by holding the bitline voltage nearly constant during sensing [6]. With this goal in mind a process variation tolerant robust current-latch sense amplifier (CLSA) design is presented. In this study, Predictive Technology Models (PTM) [17] for 45nm/32nm FinFET devices is used to demonstrate the effectiveness of the proposed approach.

3.3 FinFET Based Latch Sense Amplifier

The circuit diagram of a FinFET-based CLSA is shown in Figure 3.1(a) [3]. All transistors in this design refer to nominal 45nm technology node devices. Due to process variations like random dopant fluctuations, V_t of transistors have random variations which cause mismatch among transistors. This mismatch can induce trip point mismatch among the cross-coupled inverters of sense amplifiers and current mismatch in the evaluation branches of the sense amplifier circuit, resulting in its operational failure. Trip point is the point on inverter characteristic where input voltage equals the output voltage i.e. $V_{out}=V_{in}$.



(a) CLSA



(b) VLSA

Figure 3.1 FinFET based Latch Sense Amplifier circuits, a) CLSA b) VLSA.

Referring to the circuit of CLSA in Figure 3.1(a), ideally, without parametric variations, the circuit is symmetrical. During precharge phase, output nodes are precharged to V_{DD} by the two precharging transistors X1 and X4, BL and BLBAR are applied to the circuit (e.g. $V_{BL} = V_{DD}/2$ and $V_{BLBAR} = V_{DD}/2 - \Delta V$). Upon arrival of the sensing enable signal (SEN), the circuit conducts and outputs start discharging. A stronger current is developed in X7 than X8 due to the higher gate input voltage ($V_{BL} > V_{BLBAR}$), thus making OUT1 discharge faster than OUT2. The rapid drop of OUT1 turns on the strong positive feedback of the cross-coupled inverters and turns on the FinFET X3 of OUT2, thus charges OUT2 back to V_{DD}. With OUT1 continuing to discharge, a full swing signal

is obtained between the output nodes resulting in correct sensing operation as shown in Figure 3.2. [3]

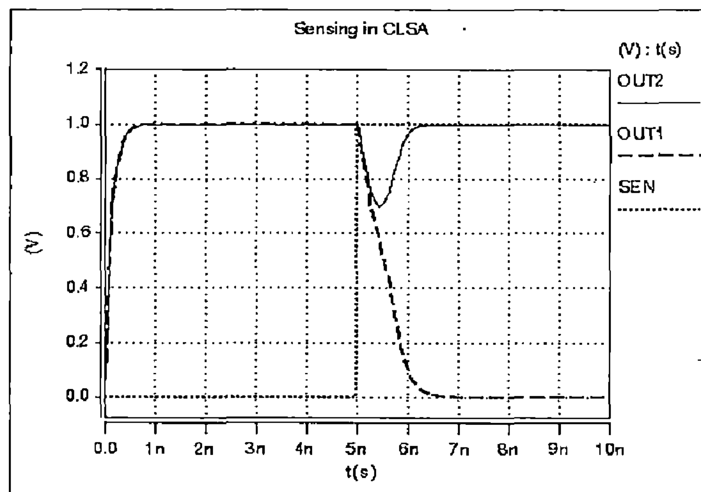


Figure 3.2 Correct sensing operation of CLSA.

3.3.1 Impact of Process Variations in CLSA and VLSA

Due to random threshold variations, transistor X7 in Figure 3.1(a) might develop a higher V_t than X8. In this case, even if the gate input of X7 is higher than that of X8, the current induced in X8 could still be larger than that in X7. In this case, OUT2 discharges faster than OUT1 and the circuit flips in the wrong direction and hence resulting in an operational failure.

The other failure mechanism induced by V_t mismatch is activated by trip-point mismatch among the cross-coupled inverters of the sense amplifier circuit which can happen in both CLSA and VLSA. Under threshold variation, different trip point voltages are developed for the two inverters in the circuit. If there is sufficient trip point voltage mismatch between cross-coupled inverter pair, it can overcome the initial differential voltage at the output nodes created by either current difference (in the case of CLSA) or directly by bitline voltage difference (in the case of VLSA). This can result in the flipping of the cross-coupled inverters in the wrong direction causing stored high to be read as zero and vice versa.

3.3.2 Monte-Carlo Analysis

Monte-Carlo analysis is a generic tool for simulating the effects of variations in device characteristics on circuit performance [18]. The variations in device characteristics are expressed as distributions on underlying model parameters. For each sample of the Monte-Carlo analysis, random values are assigned to these parameters and a complete simulation is executed, producing one or more measurement results. The series of results from a particular measurement represent a distribution, which can be characterized by statistical terms; for example, mean value and standard deviation (σ). With increasing number of samples, the shape of the distribution gets better defined with the effect that the two quantities converge to their final values.

3.3.3 Effect of V_t Mismatch on sensing of CLSA and VLSA

Under random dopant fluctuation, threshold voltages of transistors (V_t) have independent random variations (δV_t) which follows a Gaussian distribution with mean of zero [19]. To estimate yield of sense amplifier, Monte-Carlo simulations are performed in HSPICE, where V_t mismatch of every transistor in CLSA of Figure 3.1(a) is represented as Gaussian distribution [18]. Therefore, random threshold variation can be generated for each transistor independently in each simulation. The yield of the sense amplifier is estimated as [3]:

$$\text{Yield} = \frac{\text{number of correct decisions}}{\text{total number of simulations}} \times 100\%$$

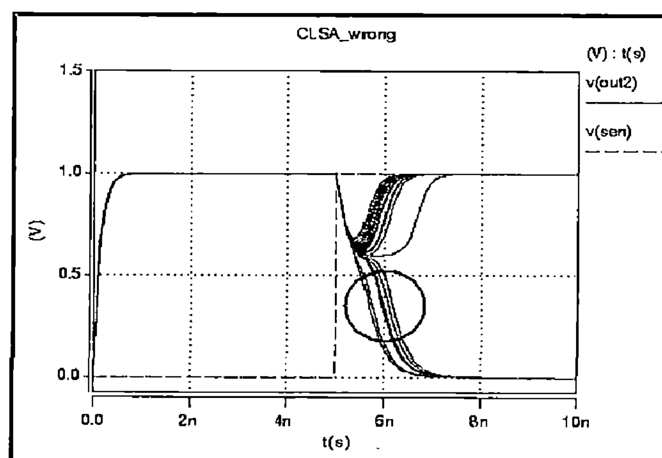


Figure 3.3 Wrong sensing in CLSA due to V_t mismatch.

Yield strongly depends on V_t mismatch. With larger V_t mismatch σ_{V_t}, failure probabilities of sense amplifiers increase drastically and yield goes down as seen in Figure 3.4. CLSA shows more failure probability and hence less yield as compare to VLSA because it is susceptible to both current mismatch and trip-point mismatch.

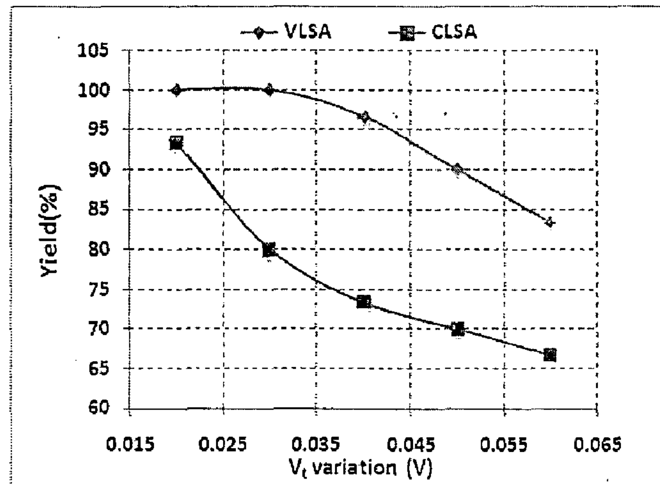


Figure 3.4 Yield vs. V_t mismatch for CLSA and VLSA.

3.4 Compensated current latch sense amplifier (CCLSA)

The proposed design of the sense amplifier has added compensation circuitry as shown in the Figure 3.5. All devices used in the circuit are nominal devices with W=90nm and L=45nm. In the modified circuit two transistors X7 and X8 which are most crucial in terms of process variations are now independently biased. Rest of the FinFET transistors has both of their gates tied together. Under this operation, threshold voltage is controlled by the input signal. The front gate of the X7 and X8 transistor still acts as inputs to BL and BLBAR. The back gate of the critical transistor has the compensation circuit, which includes capacitances C1 and C2 for storing the reference voltage for compensation. The capacitances, C1 and C2 are charged by the 'TRAIN' control signal.

The CCLSA has compared with the IGSSA (Independent Gate Self Compensation Sense Amplifier) circuit reported in [2]. There are two P-FinFETs X16 and X17 added to the new circuit to speed-up the charging of the capacitors C1 and C2. When 'TRAIN' signal is raised high, they provide a high impedance path for the current flowing through the transistors X7 and X8. Hence the current is not divided in the branch consisting X16 or X17 and full current is available for charging the capacitors. So for a fixed duration of

TRAIN signal the voltages developed across capacitors C1 and C2 will be more than the voltages developed in IGSSA circuit for the same values of capacitances used. Hence it can withstands larger mismatch in V_t and therefore more robust than the latter.

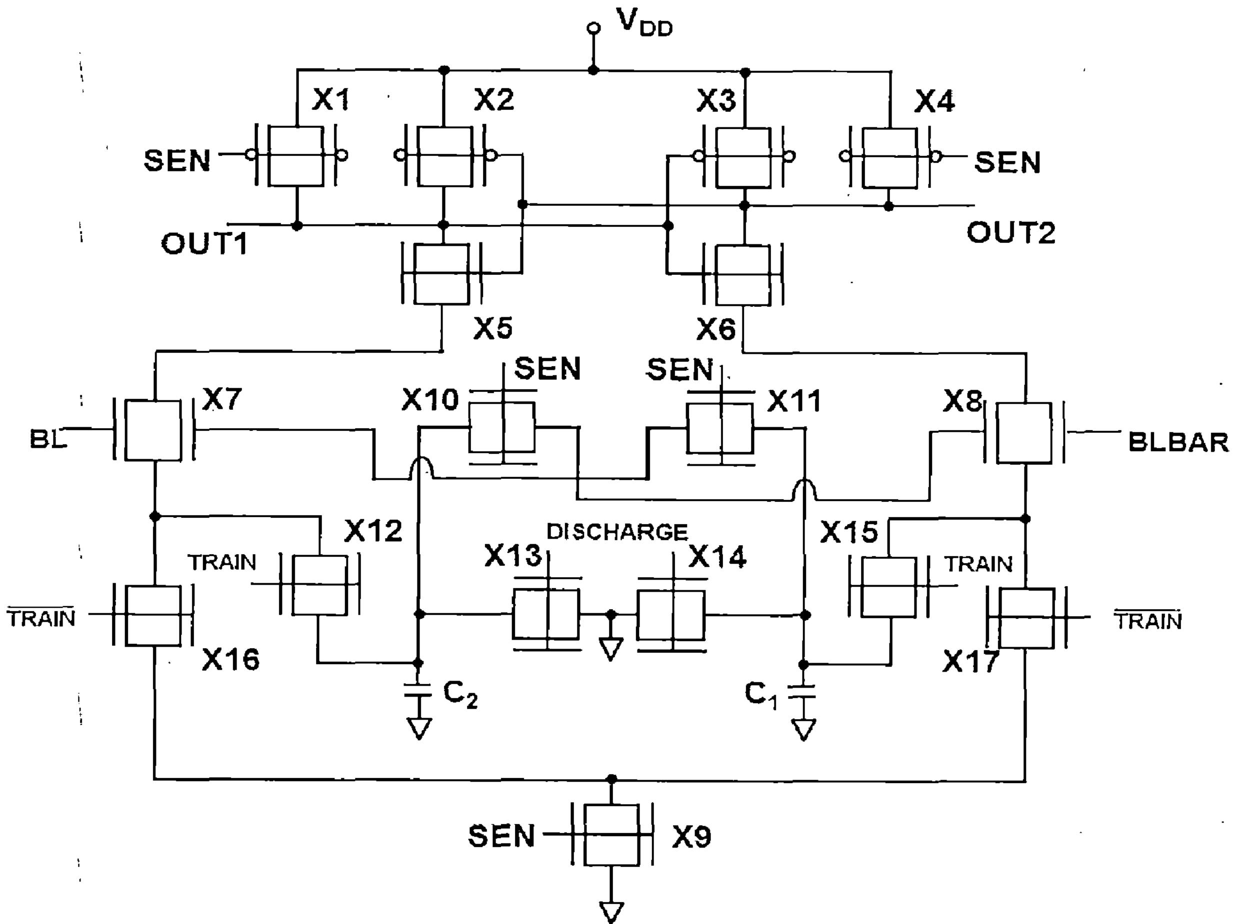


Figure 3.5 New schematic for compensation technique.

3.4.1 Operation of Compensated Circuit of CLSA

The proposed sense amplifier has four phases of operation, (i) Pre-charge phase, (ii) Capacitance discharge phase (iii) Training phase, and (iv) Sensing phase. Second phase is for discharging the capacitors, where the capacitors are fully discharged by raising the DISCHARGE signal. The SEN signal decides the phase of the sense amplifier. When SEN is low, sense amplifier is in precharge phase and the outputs are precharged high in this phase. In the sensing phase, SEN is turned-on for sensing the bit lines. The TRAIN and DISCHARGE control signal can be directly generated from the sense signal by using the self timing circuits [20].

In between second and fourth phase there is a charging phase for the capacitors C1 and C2. The TRAIN signal is turned on, SEN and DISCHARGE are off while $V_{BL} > V_{BLBAR}$. Assuming X7 has developed a higher V_t than X8 due to process variation, then X8 conducts greater current that charges C1, while X7 has smaller current that charges C2, C1 will develop a higher voltage than C2. This higher voltage of C1 is applied to the back gate of X7 which increases its current drive and compensates for threshold voltage variations. The voltage difference which develops across the capacitances is sufficient to overcome the V_t mismatch. Similar operation can be explained for the case when X7 develops a lower V_t than X8 and $V_{BL} < V_{BLBAR}$.

3.4.2 Impact of Process Variations on the Compensated Circuit

It is understood that all devices will have normal process variations. Therefore the result can only be verified by statistical simulation. In Monte-Carlo simulations, all transistors are subjected to process variations. However, since, X7 and X8 are most sensitive transistors for sense operation; compensation for X7 and X8 provides the greatest benefit. This has also been borne out by the results of Monte-Carlo simulation.

Once the TRAIN phase is turned-on, C2 and C1 enable the compensation due to mismatch through the back gate biasing of the FinFET. Even when there is V_t mismatch of 40mV between X7 and X8, the sense amplifier performs correct sensing as shown in Figure 3.6.

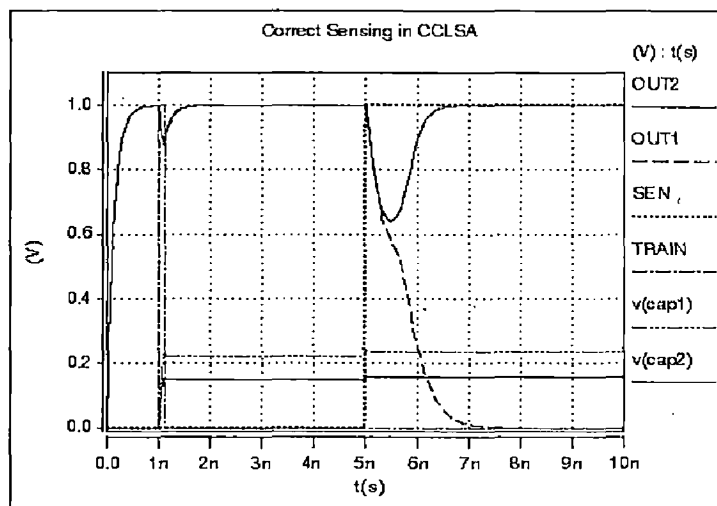


Figure 3.6 Correct sensing in CCLSA circuit.

3.5 Results

The values of C1, C2 in the compensation circuit is chosen such that it minimizes the RC time delay to charge the back-gate of X7, and also applying sufficient feedback voltages to X7 and X8. As shown in Figure 3.7, the gate of X7 charges rapidly as the sense signal arrives. The RC delay-time associated with this charging is less than 1% of sense delay.

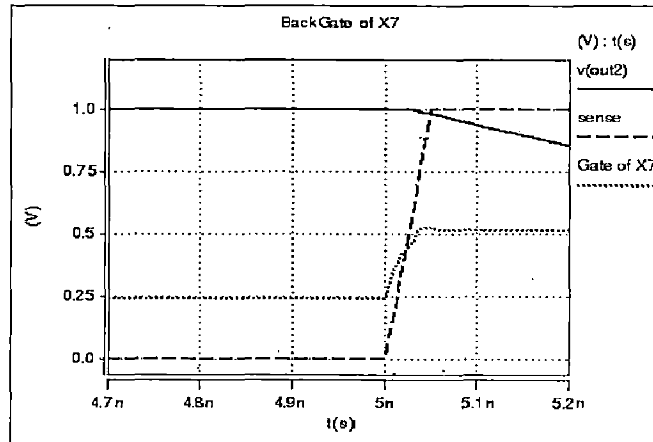


Figure 3.7 Charging of back-gate of X7.

The impact of process variation induced V_t mismatch on yield, bitline differential voltage and sense delay are studied for CLSA, VLSA and CCLSA and performance comparisons are obtained.

As seen in Figure 3.7, the gate of X7 is held fixed at a constant voltage developed during precharge phase (due to Miller capacitance) until the sense signal arrives. After that it follows the voltage across C1. Similar reasoning applies for the backgate of X8.

3.5.1 Yield v/s V_t Mismatch

The yield comparison of the CCLSA, CLSA and VLSA circuits is shown in Figure 3.8. As can be seen, CCLSA has highest yield. We see from Figure 3.8 that for a V_t mismatch of 50mV, which is typically worst case in manufactured devices, CLSA yield has dropped to almost 70% as compared to still 100% yield of CCLSA. Conversely for the same V_t mismatch yield gain of CCLSA over CLSA is almost 30% which is a significant improvement.

The comparison between the yield of IGSSA and CCLSA is shown in Figure 3.9. As seen in the Figure 3.9 CCLSA shows a yield improvement of 15% for the V_t mismatch

of as high as 60mV over IGSSA. Conversely for the same yield of 90% CCLSA can withstand V_t mismatch of as large as 25mV compared to the latter. Thus CCLSA circuit has high yield and more robustness than IGSSA, and it maintains a normal functioning of sense amplifier for worst case V_t variations.

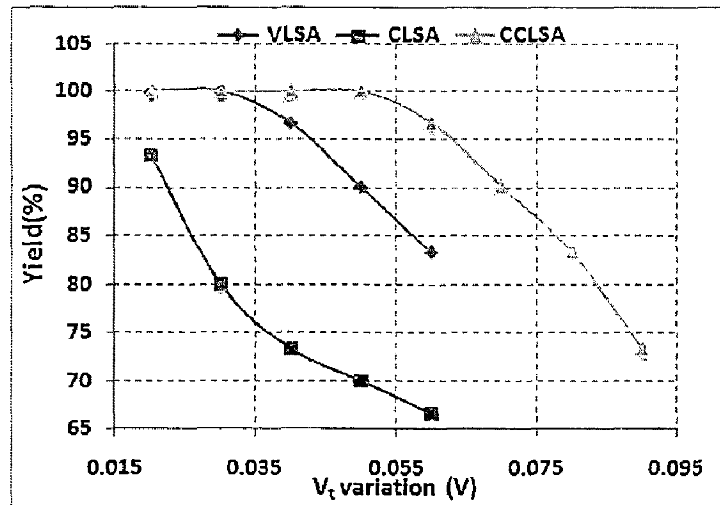


Figure 3.8 Yield comparisons for different sense amplifiers.

Further both IGSAA and CCLSA have been implemented in 32nm node. The comparison between the two circuits at 32nm is shown in Figure 3.10. As can be seen from Figure 3.10, this circuit is easily scalable to 32nm node. We note, however, that the magnitude of the yield for both CCLSA and IGSSA is lower in comparison to yield at 45nm node. But the yield difference between the two designs is consistently higher for CCLSA. This lower yield at 32nm is attributed to lower threshold voltage (V_t) and hence more susceptibility to process variations.

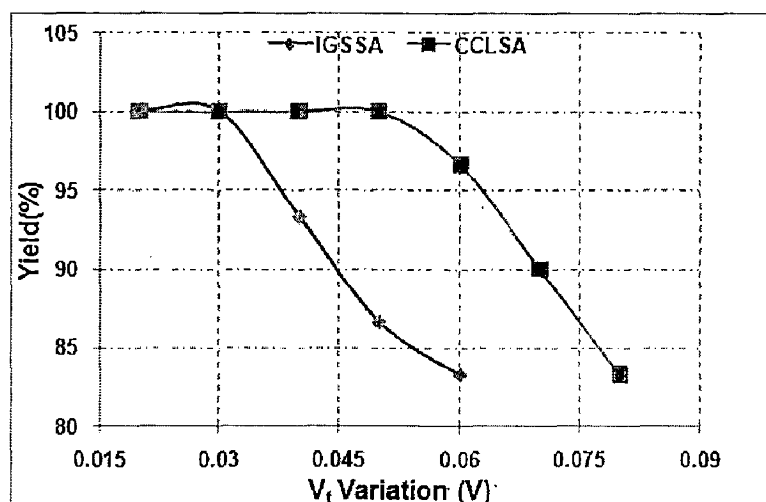


Figure 3.9 Yield comparisons of IGSSA and CCLSA.

3.5.2 Sense Delay v/s Bit-Line Differential Voltage

The sense delay versus bit-line differential voltage for the proposed CCLSA and IGSSA is shown in Figure 3.11. Sense delay is measured as the time duration when the sensing starts, up to the time when the output reaches 90% of its final value. As the applied differential voltage is increased gradually the sense delay decreases since a stronger current is developed in the circuit which speeds up sensing. The proposed circuit shows approximately 9% more sense delay than IGSSA due to current diversion in nFINFETs X16 and X17 in the discharge path. This delay penalty is a trade-off between the two designs which can be improved by making transistor X16 and X17 wider by using multi-fin structure.

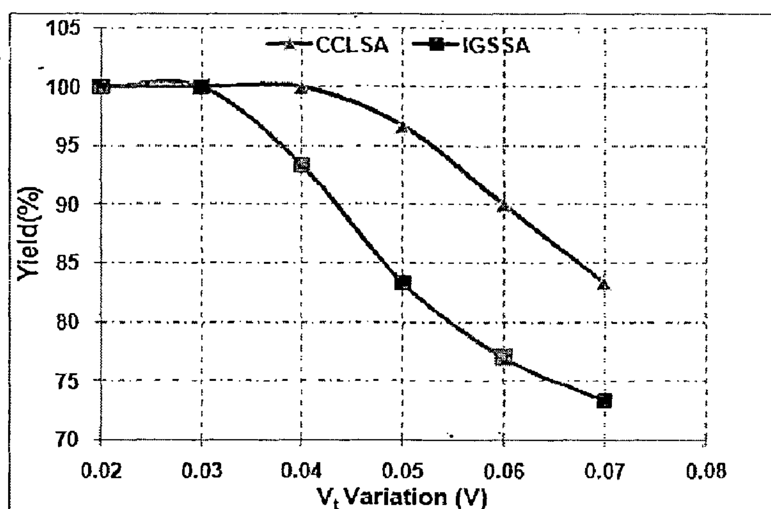


Figure 3.10 Comparison of yield at 32nm node

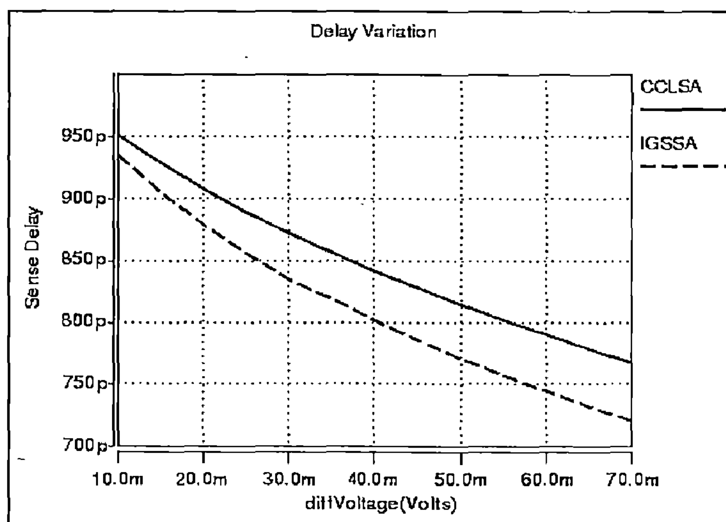


Figure 3.11 Sense delays for compensated CLSA.

In this chapter process variation tolerant self-compensating FinFET based current latch sense amplifier (CCLSA) design is presented. The proposed design withstands large mismatches (up to 50mV) in the primary sense transistors and reduces the failure probability to near zero compared to other designs. This ensures reliable circuit performance for large range of V_t mismatch. Further the statistical simulations show robustness of the design for variations in all transistors, and not just the primary transistors. The results further show that for given performance, the proposed CCLSA circuit improves yield than IGSSA. The marginally higher delay penalty introduced by CCLSA can be improved by speeding up transistors in the discharge path. The proposed design is easily implementable in 45nm FINFET technology and below to 32nm.

CHAPTER 4 NOVEL FINFET BASED SENSE AMPLIFIERS AND RESULTS

4.1 Abstract

Due to better control of short-channel effect, lower leakage current, and higher "ON" current, double-gate (DG) FinFETs have emerged as a very promising candidate for circuit design in the sub-50nm regime. FinFET can have front and back gates connected (tied-gate operation) or independent control of the front and the back gates (independent-gate operation). The tied-gate FinFET can directly translate the circuits designed in single-gate technology (e.g., bulk-CMOS) to DG-FinFET technology. In previous chapter directly translated circuit design styles were presented. However, directly translated circuit style does not utilize the possibility of independent control of front and back gates. The independent gate control is a unique property of FinFET device which is absent in standard CMOS circuits, and is very attractive for circuit design. Independent gate control has already been used in chapter 3 for dynamic compensation against process variations, where one gate is used for reference voltage and another is used for cross-coupled inverter connection. Application of independent input signals to the two gates can also improve the power and performance of logic/memory circuits. This chapter presents such type of circuit design. [21]

The importance of high-performance and robust sense amplifiers design have already been stated and explained in previous chapters. In this chapter an independent gate sense amplifier (IGSA) circuit design is introduced, where separate control of the front and the back gate is used to improve the performance and robustness of the current mode sense-amplifiers. Further dynamic compensation scheme introduced in the previous chapter is used to make the circuit design robust to process variations.

4.2 Independent Gate Sense Amplifier

In this section, the proposed IGSA design is presented and explained. FinFETs at 45nm technology node are used to implement and simulate the proposed circuit. The IGSA circuit demonstrates the advantages of using independent gate control in DG devices for circuit design in sub-50nm regime.

4.2.1 Operation of IGSA

Figure 4.1 shows the proposed IGSA circuit using FinFET at 45nm technology node. This schematic has been derived from the circuit schematic reported in [21]. Here the bit-line differential voltages are applied to one gate of the pFinFETs X2 and X3, while the other gate is used to form the cross-coupled inverters connections. Directly translated CLSA circuit from chapter 3 is shown in Figure 4.2 for easy reference.

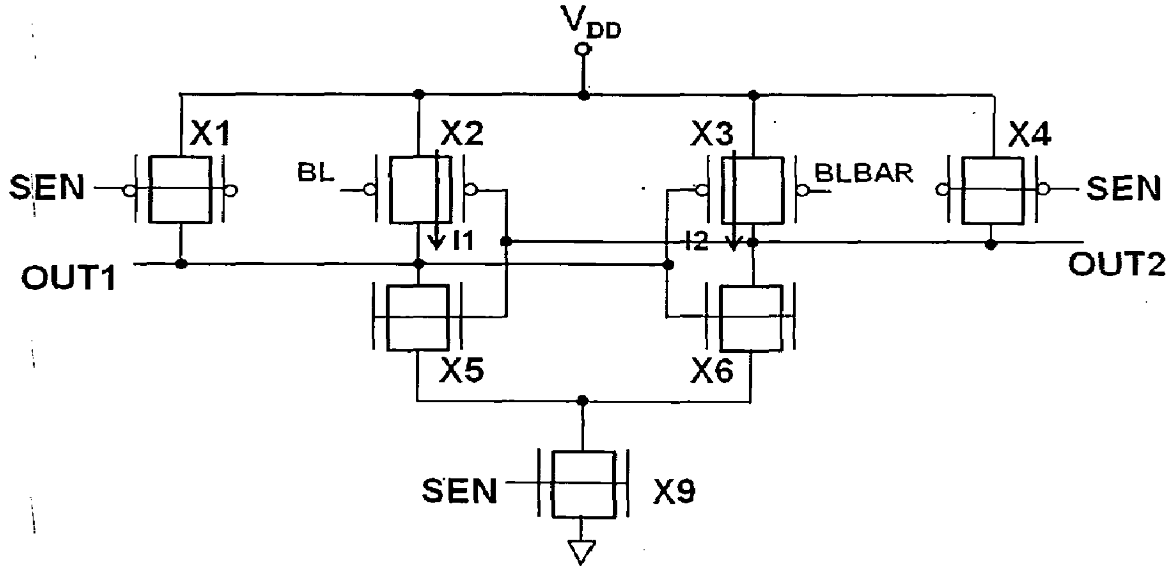


Figure 4.1 Schematic for independent gate sense amplifier (IGSA).

Using the independent gate operation of FinFET, the current difference in the two pull-down paths is achieved by using a single FinFET in each path. The front gates of X2 and X3 are connected in the cross-coupled inverter configuration; whereas BL and BLBAR are connected to the back gates (cf. Figure 4.2). When SEN is turned-on front gates of X2 and X3 are at V_{DD} but the back gates are at different voltages (V_{BL} and V_{BLBAR}). The currents difference between two paths i.e. through X2 and X3 is proportional to voltage differential,

$$\Delta I = I_1 - I_2 \propto \Delta MIN$$

where ΔI represents the current difference between X2 and X3 in Figure 4.1. Hence, it can be observed that, the voltage difference ΔMIN results in a current difference between the two paths ($V_{BL} > V_{BLBAR} \Rightarrow \Delta MIN > 0 \Rightarrow I_1 > I_2$ i.e., correct sensing), thereby ensuring the sensing operation. Figure 4.3 shows the waveform of sensing

operation of IGSA circuit. As seen in Figure 4.3 this circuit correctly senses the bit line voltages, as is done by the CLSA circuit.

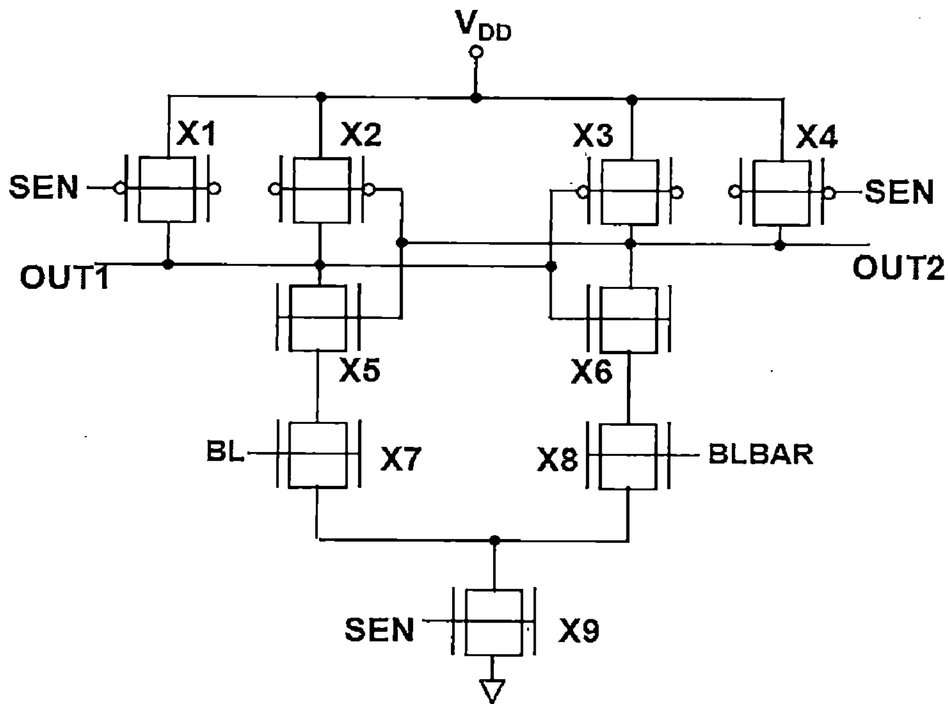


Figure 4.2 Schematic of directly translated CLSA.

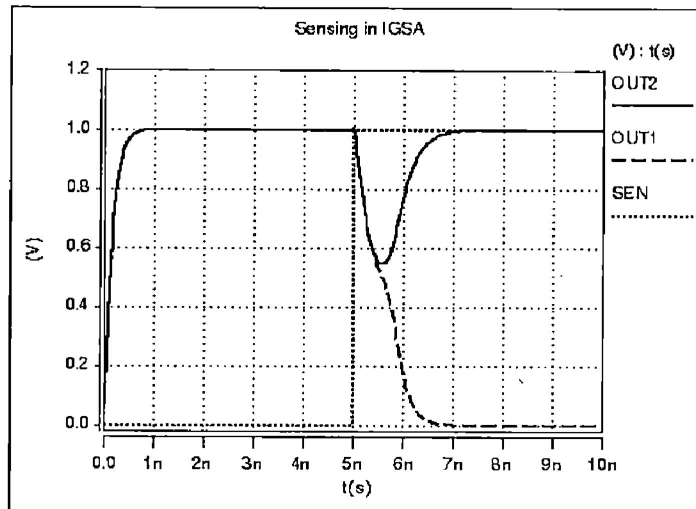


Figure 4.3 Correct sensing operation of IGSA.

4.2.2 Advantages of the IGSA Over Directly Translated CLSA

In the IGSA circuit of Figure 4.1, OUT1 and OUT2 are discharged through 2-transistor stack (instead of 3-transistor stack as in CLSA circuit). Reducing the number of transistors in the stack reduces the sensing delay. Also, in the IGSA, nodes OUT1 and

OUT2 drive only front gates of X2 and X3 instead of the front and back gates of X2 and X3 as in Figure 4.2. This reduces the capacitive load on OUT1 and OUT2, thereby increasing the speed and reducing the switching power [21]. Also elimination of X7 and X8 reduces complexity, hence saving of chip area.

Figure 4.4 shows the delay variation of CLSA and IGSA circuit. As predicted IGSA circuit shows significant improvement of 19% over CLSA circuit. It is also evident that the proposed IGSA has less number of transistors (X7 and X8 are eliminated). This factor also contributes to delay reduction.

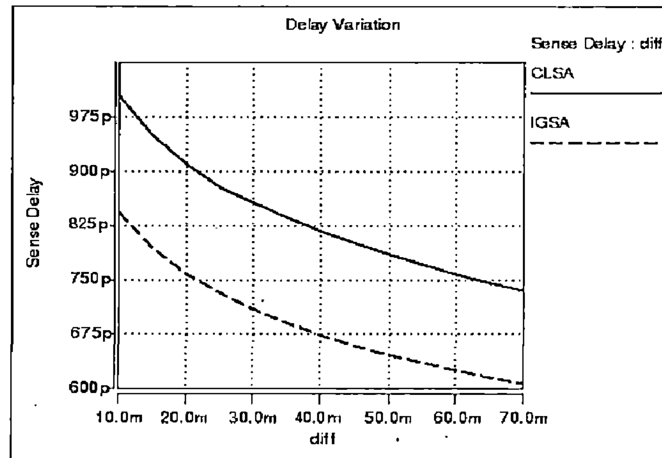


Figure 4.4 Delay comparisons of CLSA and IGSA.

In Figure 4.5 average power dissipation of CLSA and IGSA circuit for one sensing cycle has plotted for various bit-differential voltages. Elimination of transistor X7 and X8 from CLSA results in 7% reduction in power. Power reduces as differential voltage increases since stronger current forces output nodes to reach their final values quickly.

The yield comparison of two circuits is shown in Figure 4.6 for different V_t mismatch. The IGSA circuit shows better robustness compared to directly translated CLSA circuit. This happens because removal of X7 and X8 eliminates the input offset due to mismatch in these transistors, thereby reducing the input offset voltage. This has also been borne out by the Monte-Carlo simulations and as shown in graphs of Figure 4.6. Yield of sense amplifier strongly depends on V_t mismatch. With larger V_t mismatch, failure probabilities of sense amplifiers increase drastically and yield goes down to 70% as seen in Figure 4.6 for the V_t mismatch of 25mV and higher.

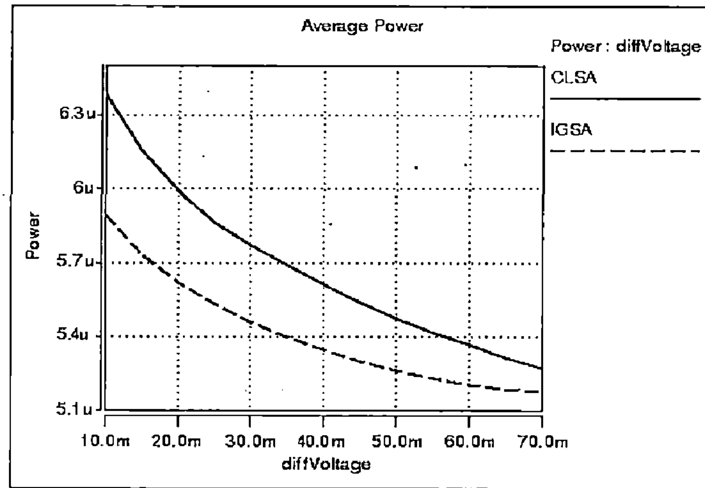


Figure 4.5 Average power dissipations of CLSA and IGSA.

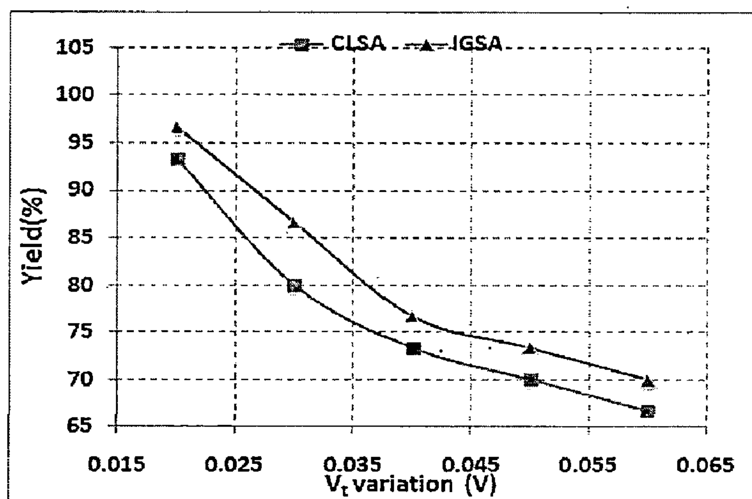


Figure 4.6 Yield comparisons of CLSA and IGSA.

Though IGSA has slightly better yield (almost 5%) than CLSA, still this is not sufficient yield improvement. To further improve the yield, compensation scheme introduced in previous chapter has been applied to IGSA circuit.

4.2.3 Compensated Circuit for IGSA (CIGSA)

The compensation scheme proposed in chapter 3 is applied to IGSA circuit to make it tolerant against process variation. The proposed sense amplifier has added compensation circuitry as shown in the Figure 4.7. In the modified circuit the reference voltages developed across two capacitors C1 and C2 is applied to one gate of transistors X5 and X6 which form the cross coupled inverters. While the bit line voltages are applied to transistors X2 and X3. In this way the compensation scheme is employed using the back

gate of FinFET. Remaining FinFET transistors have both of their gates tied together. The front gate of the X2 and X3 transistor still acts as inputs to BL and BLBAR. The back gate of the transistors X5 and X6 has the compensation circuit, which includes capacitance C1 and C2 for storing the reference voltages for compensation. C1 and C2 are charged by the 'TRAIN' control signal.

4.2.4 Operation of Compensated Circuit of IGSA

As already explained in chapter 3 for the case of CCLSA, there are four phases of operation for CIGSA circuit too, (i) Pre-charge phase, (ii) Capacitance discharge phase (iii) Training phase, and (iv) Sensing phase. Second phase is for discharging the capacitors, where the capacitors are fully discharged by raising the DISCHARGE signal. The SEN signal decides the phase of the sense amplifier. When SEN is low, sense amplifier is in precharge phase and the outputs are precharged high in this phase. In the sensing phase, SEN is turned-on for sensing the bit lines. The TRAIN and DISCHARGE signal can be directly generated from the SEN signal by using the self timing circuits [20].

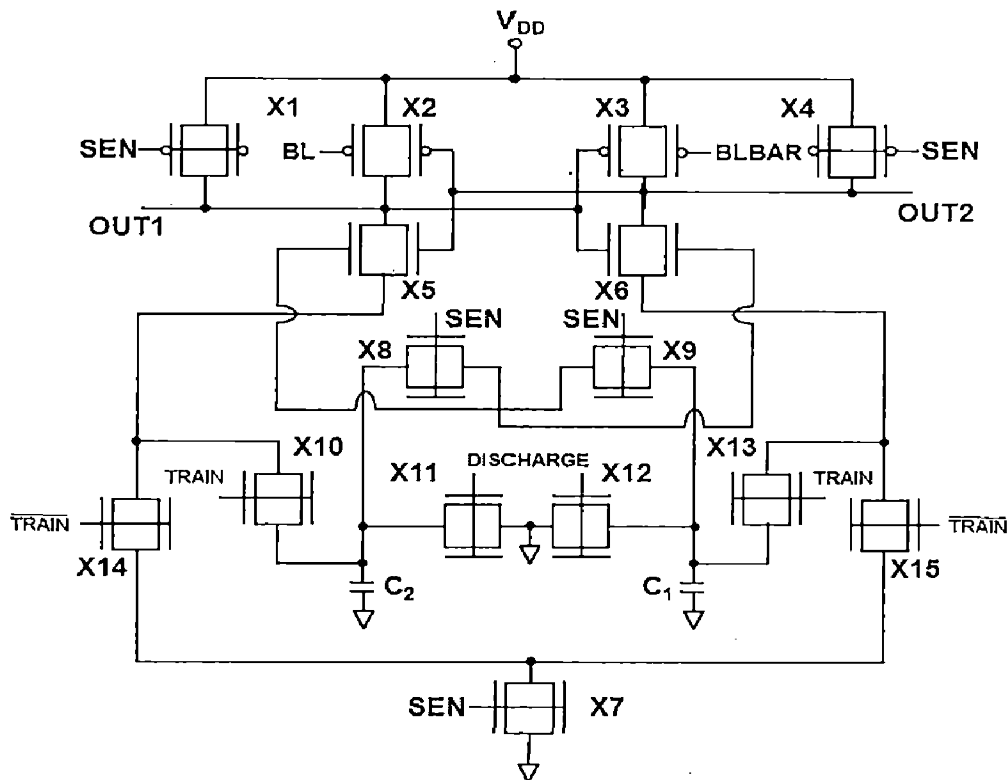


Figure 4.7 New schematic for compensation technique for IGSA.

During the TRAIN phase, SEN and DISCHARGE are off while $V_{BL} > V_{BLBAR}$. Assuming X2 has developed a higher V_t than X3 due to process variations, then X3 conducts greater current that charges C1, while X2 has smaller current that charges C2. Hence C1 will develop a higher voltage than C2. This higher voltage of C1 is applied to the back gate of X5 which increases current drive for its branch and compensates for threshold voltage variations. The voltage difference developed across the capacitances is sufficient to overcome the V_t mismatch. Similarly, operation for the case when X3 has developed a higher V_t than X2 and $V_{BL} < V_{BLBAR}$ can be explained.

Once the TRAIN phase is turned-on, C2 and C1 enable the compensation due to mismatch through the back gate biasing of the FinFET. Even when there is V_t mismatch of 50mV between X7 and X8, the sense amplifier performs correct sensing as shown in Figure 4.8.

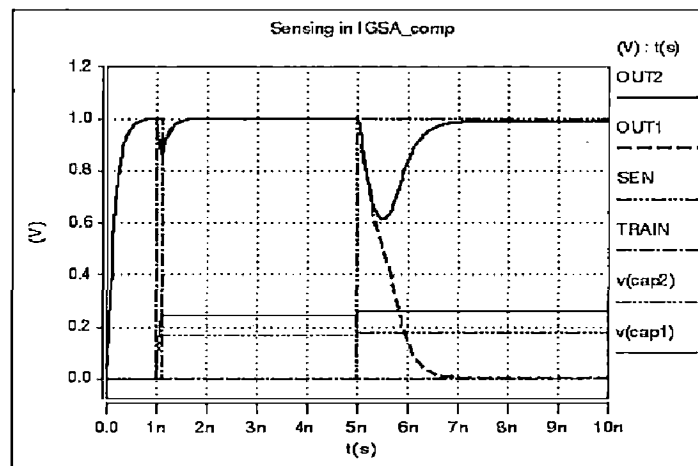


Figure 4.8 Correct sensing in CIGSA circuit.

4.2.6 Results

The impact of process induced V_t mismatch on yield, bitline differential voltage and sense delay are studied for CLSA, CCLSA, IGSA and CIGSA circuits and performance comparisons are obtained.

The yield comparisons of the IGSA and CIGSA circuits are shown in Figure 4.9. As can be seen, CIGSA has higher yield. As is seen from Figure 4.9 that for a V_t mismatch of 50mV, which is typically worst case in manufactured devices, IGSA yield has dropped to almost 70% as compared to still 95% yield of CIGSA. Hence for the same V_t

mismatch yield gain of CIGSA over CLSA and IGSA is almost 25-30% which is a significant improvement. As seen in the Figure 4.9 CCLSA has highest yield among all the circuits, followed by CIGSA circuit. The CCLSA has 7-9% more yield than CIGSA circuit for the V_t mismatch of as high as 60mV.

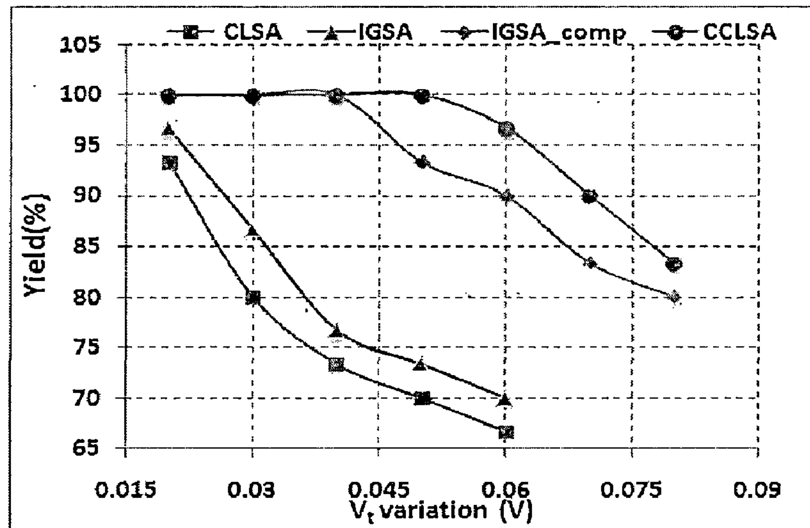


Figure 4.9 Yield comparisons for different sense amplifiers.

The sense delay versus bit-line differential voltage for IGSA and CIGSA is shown in Figure 4.10. Sense delay is measured as the time duration when the sensing starts, up to the time when the output reaches 90% of its final value [21]. As the applied differential voltage is increased gradually the sense delay decreases since a stronger current is developed in the circuit which speeds up sensing.

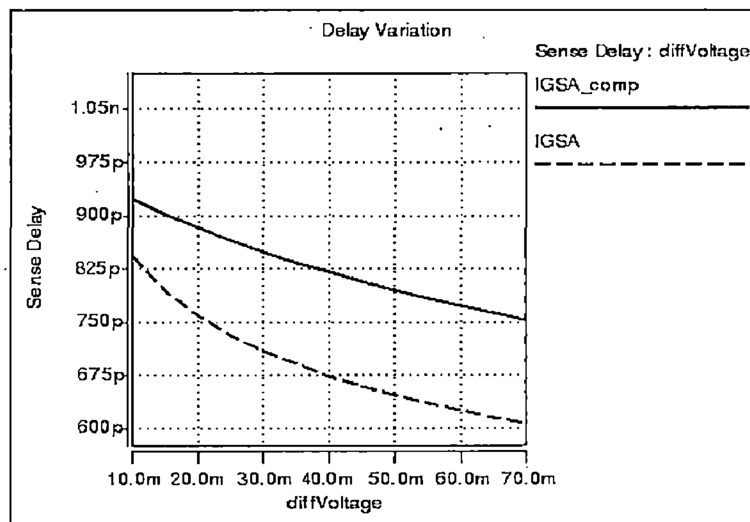


Figure 4.10 Sense delays for IGSA and CIGSA.

As is observed in Figure 4.10 that compensated IGSA (CIGSA) has 15-20% more sense delay than IGSA. This is attributed to incresed complexity of CIGSA circuit i.e. more number of devices. This delay penalty is trade-off between choice of two designs, which calls for selecting a design style depending on robustness and circuit complexity.

Further the sense delays for CIGSA and CCLSA circuit (presented in chapter 3) have been compared and are shown in Figure 4.11 against the varying differential voltages. The CCLSA circuit has marginally higher delay (3%) than CIGSA, because elimination of two transistors in CIGSA circuit.

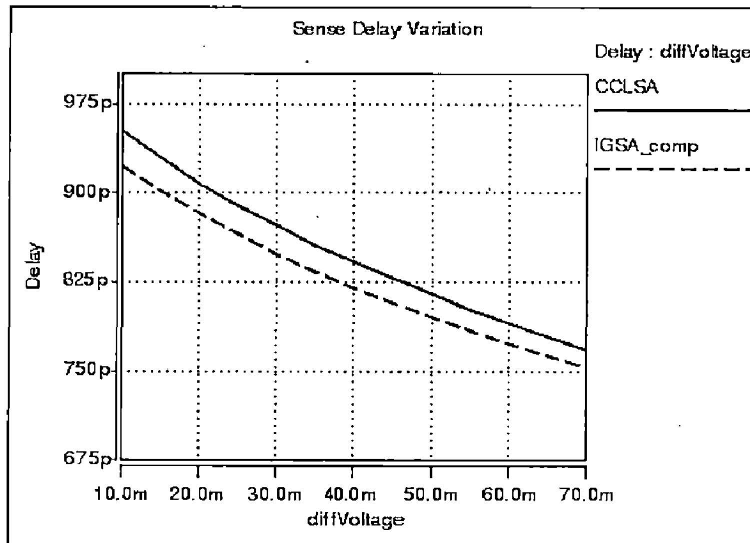


Figure 4.11 Sense delays for CCLSA and CIGSA.

The work has thus far shown the robustness of designed compensation circuitry. One more circuit is presented in the next section which will further prove the robustness.

4.3 Latch-based sense amplifier

Figure 4.12 presents the Latch Based Sense Amplifier (LBSA) derived from the circuit reported in [22]. This circuit consists of the cross-coupled inverter latch formed by X2, X4 and X3, X5 and hence the name. OUT1 and OUT2 nodes are precharged to 0V before sensing. At the beginning of operation, both X2 and X3 transistor start to pull-up OUT1 and OUT2 to V_{DD}. The imbalance in current flow caused by voltage difference on the front-gates (FG) of X2 and X3 slows down the pull-up of one of the output nodes. Due to cross-feedback connections in the structure in Figure 4.12, increasing voltage of one of the output nodes causes cutting-off of the opposite pFinFET thus reducing its

pull-up strength. The same feedback connection on the back-gate of nFinFET causes increase in conductivity and better pull-down of relevant output voltage. Introduction of the DG technology allowed an additional back-gate connection, resulting in feedback strength and speed improvement [22]. The disadvantage of this schematic is that during sensing, there is always an open path from V_{DD} to ground, due to the fact that X4 and X5 front-gates are always connected to the bitlines which are precharged to V_{DD}.

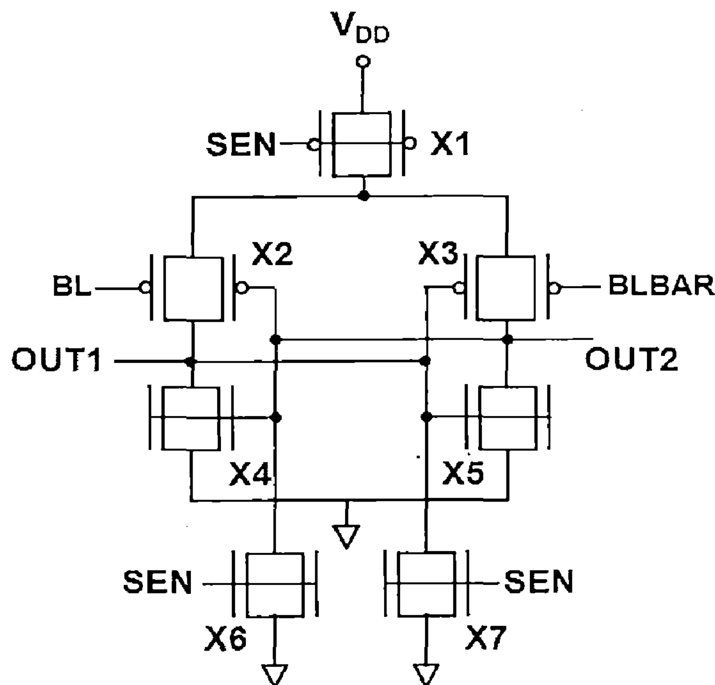


Figure 4.12 Schematic of Latch Based Sense Amplifier (LBSA).

The sensing operation of LBSA is shown in Figure 4.13. In the Figure 4.13 OUT2 is latched to V_{DD} while OUT1 is latched to ground.

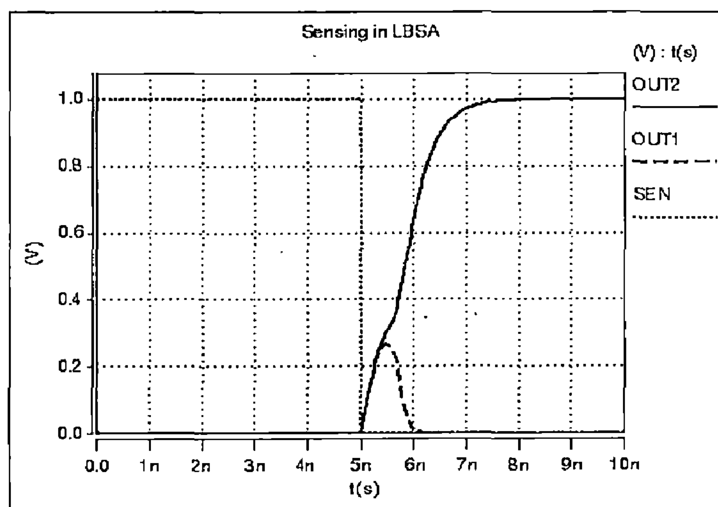


Figure 4.13 Sensing in Latch Based Sense Amplifier (LBSA).

4.3.1 Impact of Process Variations in LBSA

In Monte-Carlo simulations, V_t mismatch of every transistor in LBSA of Figure 4.12 is represented as a Gaussian function [19]. Therefore, random threshold variation can be generated for each transistor independently in each simulation. The yield of the sense amplifier is estimated as [3]:

$$Yield = \frac{number\ of\ correct\ decisions}{total\ number\ of\ simulations} \times 100\%$$

Yield strongly depends on V_t mismatch. With larger V_t mismatch, failure probability of LBSA increases, hence yield goes down as seen in Figure 4.14.

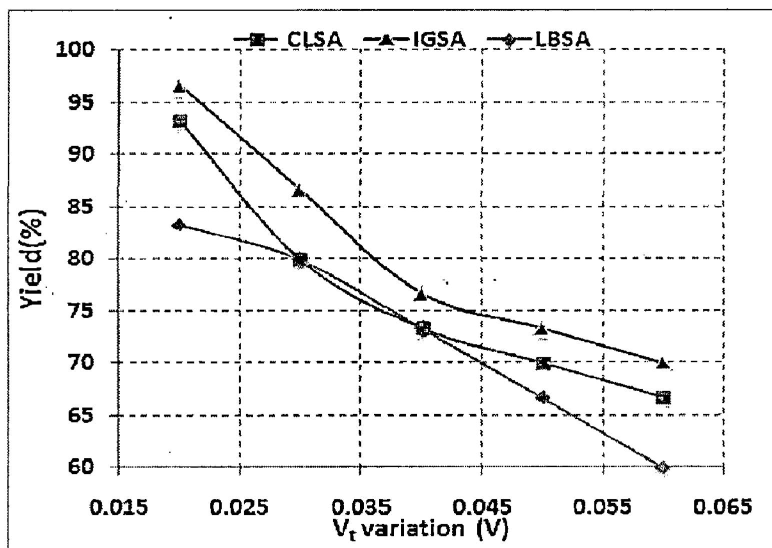


Figure 4.14 Yield vs. V_t mismatch for CLSA, IGSA and LBSA.

It is clear from the above figure that yield of LBSA decreases drastically as compare to CLSA and IGSA circuit. To improve the yield, compensation scheme introduced in previous chapter has been applied to LBSA circuit.

4.3.2 Compensated Circuit for LBSA (CLBSA)

The compensation scheme proposed in chapter 3 and applied to IGSA circuit, has also been applied to LBSA to make it process variation tolerant. The proposed sense amplifier has added compensation circuitry as shown in the Figure 4.15. In the modified circuit the reference voltages developed across two capacitors C1 and C2 is applied to one gate of transistors X4 and X5 which form the cross coupled inverters. While the bit

line voltages are applied to transistors X2 and X3. In this way the compensation scheme is employed using the back gate of FinFET. Remaining of the FinFET transistors have both of their gates tied together. The front gates of the X2 and X3 transistor still act as inputs to BL and BLBAR. The back gate of the transistors X4 and X5 has the compensation circuit, which includes capacitances C1 and C2 for storing the reference voltages for compensation. These capacitances are charged by the 'TRAIN' control signal.

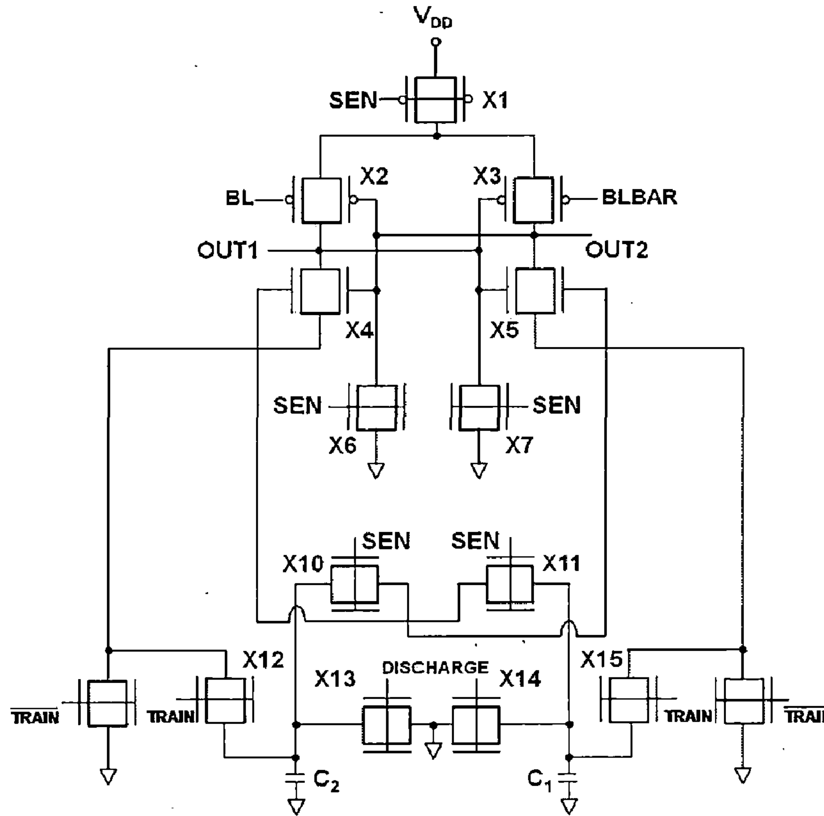


Figure 4.15 New schematic for compensation technique for LBSA.

4.3.3 Results

The impact of process induced V_t mismatch on yield, bitline differential voltage and sense delay are studied for LBSA and compensated LBSA (CLBSA) and performance comparisons are obtained.

The yield comparisons of the LBSA and CLBSA circuits are shown in Figure 4.16. As can be seen, CLBSA has higher yield. This proves the effectiveness of the devised compensation scheme. As is observed from Figure 4.16 that for a V_t mismatch of 40mV, LBSA yield has dropped to almost 70%. At this mismatch CLBSA shows 85% yield

which is a result of compensation scheme. This yield improvement is significant at higher mismatches. Conversely for the same yield of 85% CLBSA can withstands 20mV more mismatch than LBSA circuit. This robustness is attributed to the compensation scheme.

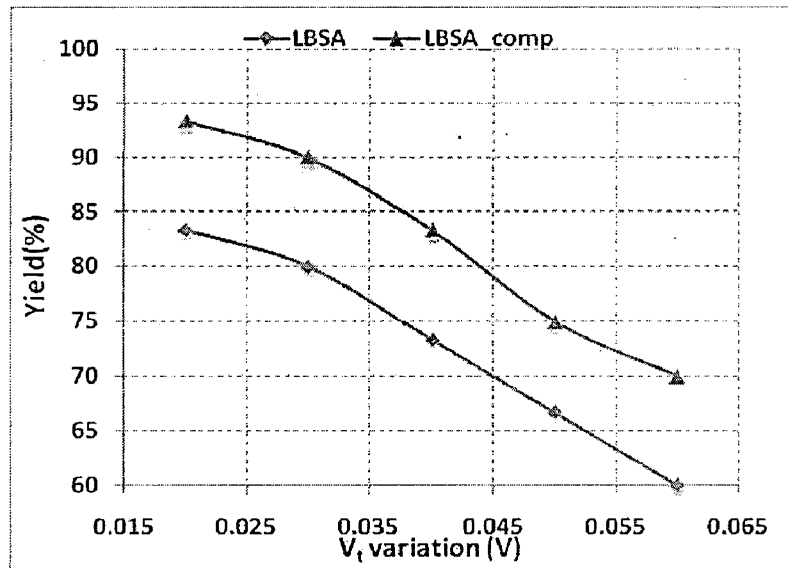


Figure 4.16 Yield comparisons for LBSA and CLBSA.

The sense delay versus bit-line differential voltage for LBSA and CLBSA is shown in Figure 4.17. Sense delay is measured as the time duration when the sensing starts, up to the time when the output reaches 90% of its final value.

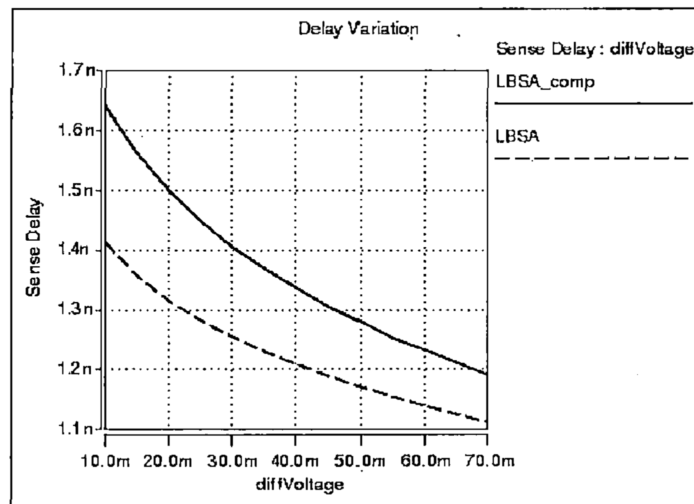


Figure 4.17 Sense delays for IGSA and CIGSA.

As is observed from Figure 4.17 that compensated LBSA (CLBSA) has 10-12% more sense delay than LBSA. This is caused by the incresed complexity of CLBSA circuit i.e.

more number of devices. This delay penalty is a trade-off between choice of two designs, which calls for selecting a design style depending on robustness and performance criteria.

In Figure 4.18 average power dissipations of LBSA and CLBSA circuit for one full sense cycle has plotted for various bit-differential voltages. It is seen from Figure 4.18 that CLBSA shows 5-6% more power dissipation than LBSA. This is due to the added complexity introduced by compensation scheme, hence an increase in number of devices. Power reduces as differential voltage increases since stronger current forces output nodes to reach their final values quickly.

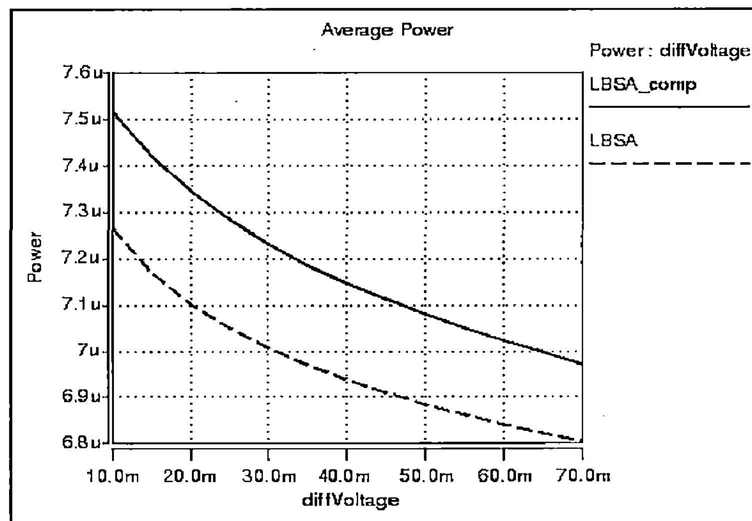


Figure 4.18 Average power dissipations of LBSA and CLBSA.

In this chapter process variation tolerant self-compensating FinFET based independent gate sense amplifier (IGSA) design is presented. This design withstands large mismatches (up to 50mV) in primary sense transistors and increases yield. This ensures reliable circuit performance for large range of V_t mismatch. Further the statistical simulations show robustness of the design for variations in all transistors, and not just the primary transistors. The results further show that for given performance, the proposed IGSA and CIGSA scheme improves yield than CLSA. The marginally higher delay penalty introduced by CIGSA can be traded-off with yield. This scheme is easily implementable in 45nm.

CHAPTER 5 CONCLUSION

In this work different types of robust sense amplifier circuits are designed. Their yield, sense delay and power dissipations are measured and compared. The compensation scheme introduced has been shown to be effective in restoring yield at worst-case process variation conditions. Moreover, the designed circuits do not suffer from any significant delay penalty. The proposed designs are easily implementable at FinFET 45nm technology.

Three sense amplifiers with their compensation circuitry are designed and presented in this report. These are namely CLSA, IGSA, LBSA circuits and their compensated variants are namely CCLSA, CIGSA, and CLBSA. A summary of results for these circuits are given below in Table 1 and Table 2.

Table 1 Compensated circuits

Metrics ↓ Circuits →	CCLSA	CIGSA	CLBSA
Yield at mismatch of 40mV	100%	95%	85%
Delay at 40mV bit-line diff-voltage	840ps	825ps	1350ps
Power dissipation at 40mV diff-voltage	5.7 μW	5.67 μW	7.15 μW
Area factor	$9\times120\lambda^2$	$8\times120\lambda^2$	$8\times120\lambda^2$

Table 2 Uncompensated circuits

Metrics ↓ Circuits →	CLSA	IGSA	LBSA
Yield at mismatch of 40mV	72%	77%	70%
Delay at 40mV bit-line diff-voltage	825ps	675ps	1200ps
Power dissipation at 40mV diff-voltage	5.6 μW	5.35 μW	6.95 μW
Area factor	$4.5\times120\lambda^2$	$3.5\times120\lambda^2$	$3.5\times120\lambda^2$

Above tables show meaningful comparisons between compensated and uncompensated circuits, along with the design metrics. The relevant graphs are also given for easy reference in Figure 5.1, Figure 5.2, and Figure 5.3. As shown in Figure 5.1 the yield for uncompensated CLSA, IGSA, LBSA are shown along with the yield of compensated circuits. The sense delay variations for these two classes are shown in Figure 5.2, whereas Figure 5.3 shows the power dissipations graph.

From above discussion it is clear that to choose a particular design style strongly depends upon the requirements. If the circuit has to operate under severe process variation conditions, then CCLSA is the best choice. It has highest yield among all the circuits with less delay penalty. Yield gain of CCLSA over CLSA circuit is almost 30% for a V_t mismatch as high as 40mV. This high yield is due to introduction of compensation circuitry. But chip area occupied by CCLSA is almost double than CLSA.

If at the same time we also want less delay penalization, then CIGSA circuit schematic can be opted. This design maintains the yield close to CCLSA and delay does not suffer much. The CIGSA circuit has merely 5% less yield than CCLSA, while the elimination of two transistors results in an area factor of $8\times120\lambda^2$ which is less than CCLSA. Sensing delays of CCLSA and CIGSA are comparable. CCLSA has just 3% excess delay as compared to CIGSA.

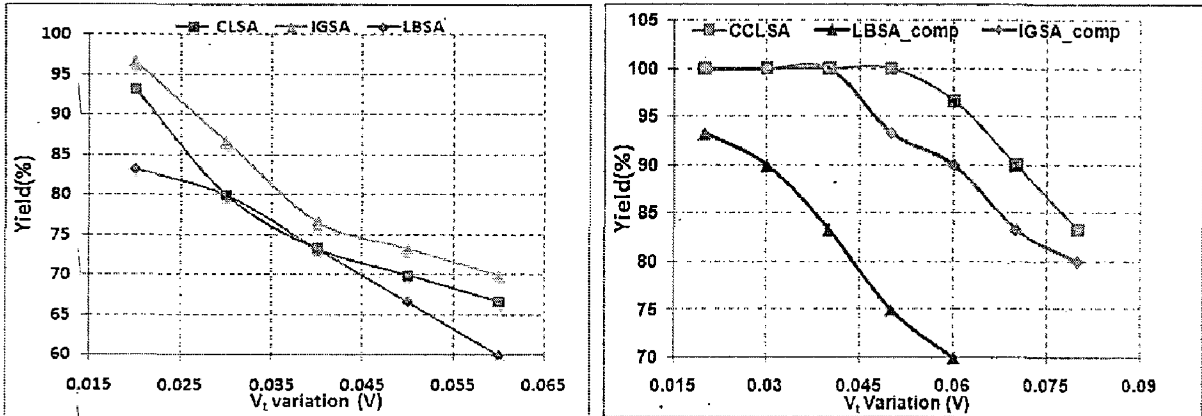


Figure 5.1 Yield graphs for compensated and uncompensated designs.

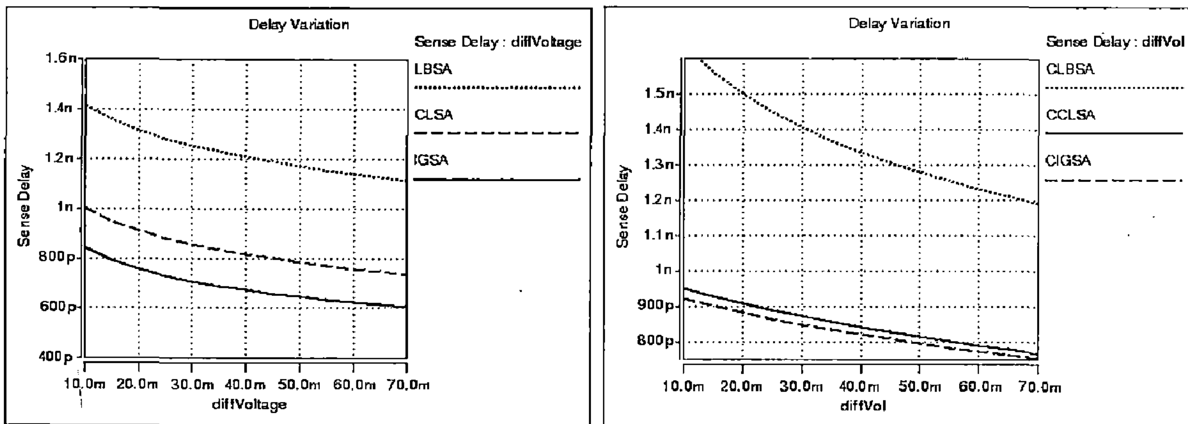


Figure 5.2 Sense delay variations for compensated and uncompensated designs.

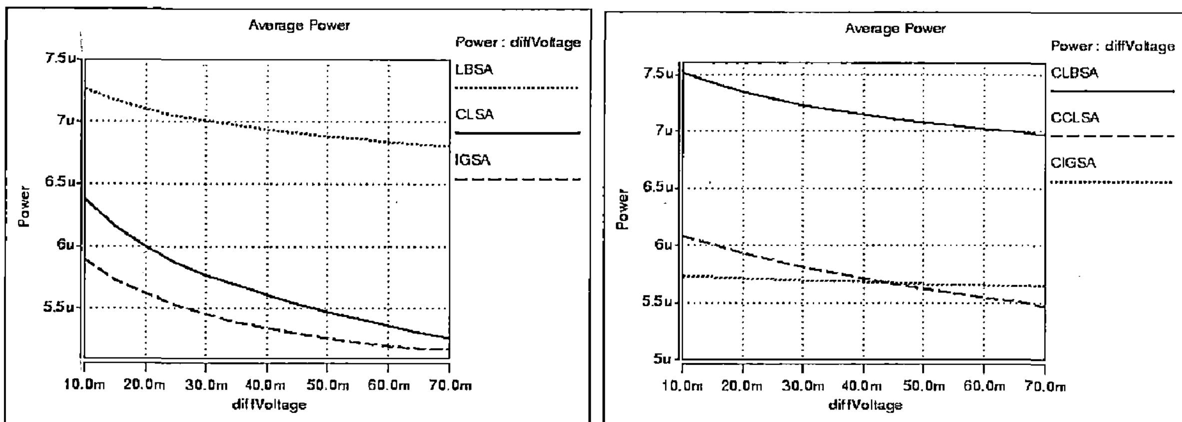


Figure 5.3 Average power dissipations for compensated and uncompensated designs.

On the other hand if reduced circuit complexity is desired and hence less chip area is prime requirement, then IGSA circuit can be picked out. It offers optimum design for yield, speed and area. The chip area occupied by the circuit depends upon the width and length of the transistors. It can be approximately calculated by using the layout of FinFET inverter proposed in [24]. The cell layout area has expressed in terms of λ, which is the minimum spacing requirements for the particular technology.

As seen in above table the speed of IGSA is higher than the other two uncompensated circuits. Moreover it offers less area along with reduced power dissipation. So among the uncompensated circuits IGSA is a natural choice for sensing operation for high V_t variation.

Therefore even if the area is slightly greater for compensated circuits they show substantial yield gain for worst case V_t variations over the uncompensated designs. However among compensated circuits, CCLSA has the largest area than other schemes, but also offers the highest yield. Hence the increased area can be traded-off with the yield gain. The LBSA has the least area but its yield deteriorates as variation increases. However CLBSA improves the yield, but its delay and power dissipation is higher.

Future Scope for work

In this work the designs of different configuration of sense amplifier circuits has been investigated. However there is immense scope for one to further extend the work. In this work PTM model is used to simulate FinFET based circuit schematics in HSPICE. These models give fairly accurate results in less simulation time, while avoiding going into rigor of the device simulation.

The possible future path might consist of implementing these circuits in a device simulator where fine tuning of individual transistor parameters i.e. (oxide thickness t_{ox}, channel doping N_{ch}, etc.) can be done. Also Monte-Carlo simulation can be performed on each individual parameter to find its effect on yield and delay. At the same time accurate area can be calculated by drawing layouts of these circuits. Multi-fin structures which are not utilized in this work can be a possible option for reducing the delay.

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