LOW POWER 12-BIT SAR ADC DESIGN

A DISSERTATION

Submitted in partial fulfillment of the requirements for the award of the degree of

MASTER OF TECHNOLOGY

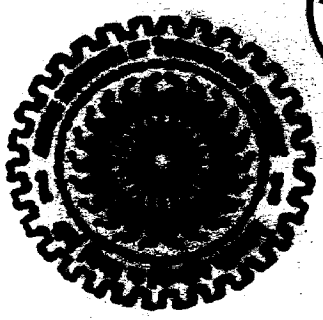
in

ELECTRONICS AND COMMUNICATION ENGINEERING

(With Specialization in Semiconductor Devices & VLSI Technology)

By

VENKATA SS KUMAR NITTALA



DEPARTMENT OF ELECTRONICS AND COMPUTER ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY ROORKEE
ROORKEE -247 667 (INDIA)

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CANDIDATE'S DECLARATION

I hereby declare that the work presented in this dissertation report entitled, **"LOW POWER 12 BIT SAR ADC DESIGN"** towards the partial fulfillment of the requirements for the award of **Master of Technology in Electronics and Communication Engineering** with specialization in **Semiconductor Devices and VLSI Technology (SDVT)**, submitted in the Department of Electronics and Computer Engineering, Indian Institute of Technology Roorkee, is an authentic record of my own work carried out during the period from July 2009 to July 2010, under the guidance of **Dr. Sudeb Dasgupta and Dr. A.K. Saxena, Department of Electronics and Computer Engineering, Indian Institute of Technology Roorkee.**

The content of this dissertation has not been previously submitted for examination as part of any academic qualifications.

Date: 26-07-10

Place: ROORKEE

VENKATA SS KUMAR NITTALA

CERTIFICATE

This is to certify that the above statement made by the candidate is correct to the best of my knowledge and belief.

Date: 26/07/10

Place: Roorkee

Dr. A. K. Saxena
Professor, E&C Department,
Indian Institute of Technology, Roorkee
Roorkee-247667 (India).

Dr. S. Das Gupta 26/07/10
Assistant Professor, E&C Department,
Indian Institute of Technology, Roorkee
Roorkee-247667 (India).

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Kumar N.V.S.S
M.Tech SDVT

ABSTRACT

This thesis presents a new scheme of designing a low power 12-bit split capacitor array analog to digital converter (ADC). The proposed design involves a novel way so as to achieve low power and low area requirements. The design is targeted to cater the needs of micro sensor wireless applications. Low Power consumption is reported with moderate accuracy.

In this thesis the design strategies for power effective medium/high resolution successive-approximation ADC are analyzed. The study considers reducing the power of the capacitive array with suitable capacitive attenuators that do not need non-unity capacitors. The design of minimum power comparators is analyzed and a novel comparator scheme, named time-domain comparator, is described. The input referred offset voltage of the time domain comparator reported is 700μv. The increase of resolution with reduced sampling is also analyzed and implemented. The different architectures of the Boot strapping were implemented to reduce the distortion of the sampling switch. The proposed methodologies, verified with a test design, are capable to provide 12-bit with 50-kHz signal band and 1-V supply.

All the circuits in this work are implemented using Intel's 32 nm CMOS process.

List of Figures

Contents

CHAPTER 1

1. INTRODUCTION

In order to interface digital processors with the analog world, data acquisition and reconstruction circuits must be used such as Analog to digital converters (ADCs) to acquire and digitize the signal at the front end, and Digital to analog converters (DACs) to reproduce the signal at back end.

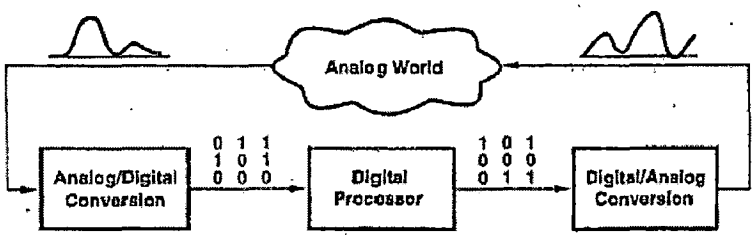

Figure 1.1 Interface between analog world and a digital processor.

Since the data conversion deals with both analog and digital signals, their design becomes extermely difficult if they are to maintain comparable performance with their corresponding digital systems i.e is not appear as bottle neck in the signal path. This is because the primary trade off in digital cicuits is between speed and power ,where as in analog cicuits it is between speed, power and precision (including resolution, dynamic range and linearity) [1].

With moore's law driving the cost of a square millimeter of silicon steadily down,the economic potential for electronics to become ubiquitous has appeared. In the last ten years,portable devices such as cell phones,laptops have first made their apperance in the market, to continously support increased functionality and intelligence.

While the current spread of such devices is of order of one or two persons, it is natural to think that the ongoing decrease of cost will enable electronic devices to be present in the environment with densities of tens, or may be hundreds per person. Such devices would not necessarily be allocated substantial computation power individuality, However when allowed to communicate, they could perform useful tasks such as online monitoring, response and distributed computation.

To minimize deployment cost and effort and minimize network adaptability and life time, the interconnection amongst nodes should happen over the air, without requiring any wiring. The electronic system dscribed above is a Wireless Sensor Network (WSN). The major obstacle to the massive deployment of Wireless Sensor Network (WSN) has to do with power [2].

For different reasons these energy limited applications, however addresses the design of A/D converters.The specifications for these above Wireless Sensor Network (WSN) are medium resolution (~10-12 bit) and low speed (~500-700 Ks/s). Therefore, these specifications are not difficult but the necessary low power level required is a challenge [3].
The successive approximation ADC has been the mainstay of data acquisition systems for many years. Recent design improvements have extended the sampling frequency of these ADCs into the megahertz region with 18-bit resolution.

This report is divided into six sections: Section II compares SAR ADC with other architectures and defines the specifications of ADC. Section III various sampling and hold circuits employed in Analog to Digital Converters have been discused. Section IV explains working principle of V2T comparator for low power applications. Section V decribes the implementation of the split capacitor array digital to annalog converter. Section VI shows the Successive Approximation Register(SAR) block diagram. Section VI concludes the report.

1.1 SUCCESSIVE APPROXIMATION CONVERTER:

The successive approximation algorithm performs the A/D conversion over multiple clock periods by exploiting the knowledge of previously determined bits to determine the next significant bit. The method aims to reduce the circuit complexity and power consumption using a low conversion rate by allowing one clock period per bit (plus one for the input sampling).

For a given dynamic range $0-V_{FS}$ the MSB distinguishes between input signals that are below or above the limit $V_{FS/2}$. Therefore, comparing the sampled input with $V_{FS/2}$ obtains the first bit as illustrated by the timing scheme. The knowledge of the MSB restricts the search for the next bit to either the upper or lower half of the $0-V_{FS}$ interval. Consequently, the threshold for determining the second bit is either $V_{FS/4}$ or (as it is for the case of the Figure 1.2) $3_{VFS/4}$. After

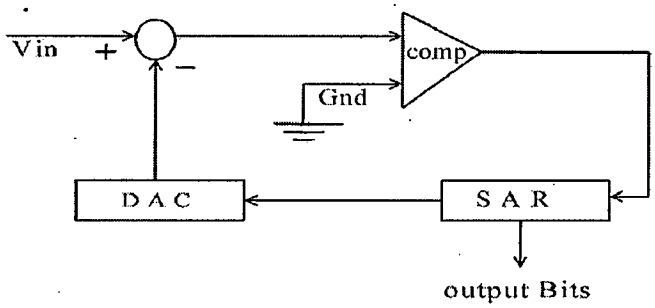

Figure 1.2 : Block diagram of SAR ADC.

this, a new threshold is chosen and the next bit can be estimated. The timing diagram of SAR ADC shown in Figure 1.2 describes the operation for three bits but, obviously, the search can continue for additional clock cycles to determine more bits [4]. The voltages used for the comparisons are generated by a DAC under the control of a logic system known as the successive approximation register (SAR) as shown in Figure 1.3. Notice that the input common mode range of the comparator must equal the dynamic range of the converter. The method uses one clock period for the S&H and one clock period for the determination of every bit thus requiring (n+1)clock intervals for an n-bit conversion. Sometimes, if the S&H settling period is significantly longer than the time required for each

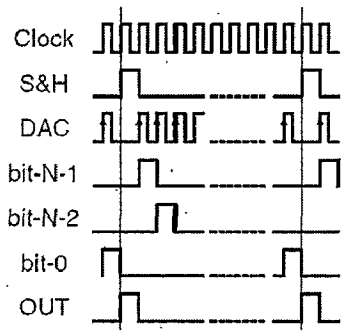

Figure 1.3: Timing diagram of SAR ADC.

comparison, then it can be convenient to use two clock periods for the sampling and one per every bit totaling (n +2) clock intervals for an n-bit conversion.Figure1.2. shows a typical block diagram of a successive approximation converter. The S&H samples the input during the first clock period and holds it for N successive clock intervals. The digital logic controls the DAC according to the successive approximation algorithm whose flow diagram is shown in Figure 1.3.

Initially the SAR sets the MSB to 1 as a prediction of the MSB value. If the comparator confirms the predicted value then the value is retained, otherwise the MSB is set to zero. On the next clock period the SAR makes another prediction by setting the value of the next bit to 1. Again the comparator confirms if this assumption was correct and, after confirmation, the algorithm proceeds in the same way predicting each successive bit until all n-bits have been determined.

At the start of the next conversion, while the S&H is sampling the next input, the SAR provides the n-bit output and resets the registers. Figure 1.3.shows the timing sequence for this conversion: the voltage V_{DAC} changes at the rising edge of Φ_{DAC} and remains available for the entire clock period. Note that the SAR's control is such that V_{DAC} tracks $V_{S\&H}$ thus establishing a search path. The name of the algorithm comes from the fact that the voltage V_{DAC} is an improving approximation of $V_{S\&H}$ every step the error can be occasionally larger than the previous one but surely is not larger than successive divisions of two of the full scale amplitude.

1.2 Charge redistribution successive approximation converter:

An effective circuit implementation of the successive approximation algorithm is the so called charge redistribution scheme. The name of the method comes from the fact that the charge sampled at the beginning of the conversion cycle is properly redistributed on the sampling array to obtain a top plate voltage close to zero at the end of the conversion cycle. A possible implementation of the charge redistribution method, shown in Figure 1.4, uses an array of binary weighted capacitances and just one comparator as an active element. The sampling phase, Φs, pre-charges the entire array to the input signal by connecting the bottom plates of the array to the input and the top plates to ground [3]. The charge on the entire array is

$$C_{Tot} = 2^n C_u V_{in} \qquad 1.0$$

After the sampling phase the SAR begins the conversion (clock period 1) by first connecting the bottom plate of the biggest capacitance ($2^n{-}1C_u$) to V_{ref} and the remaining part of the array to ground. The superposition principle determines the voltage on the top plate, applied to the comparator, to be equal to

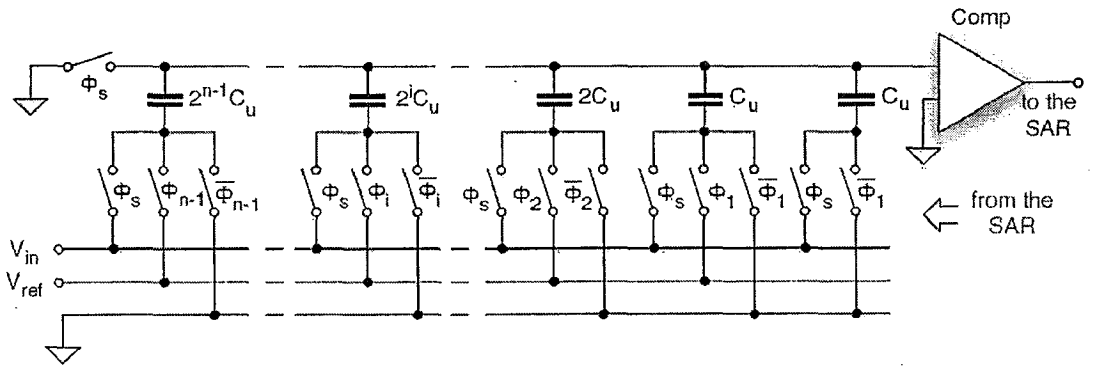

Figure 1.4: Charge redistribution implementation.

$$V_{comp}(1) = \frac{V_{ref}}{2} - V_{in} \quad 1.1$$

Since this voltage is the difference between the MSB voltage and the input, it is only necessary to compare it to ground. The comparator result determines the MSB and enables the SAR to establish the conditions for the next bit calculation. If the MSB is 1 the connection of $(2^n - 1)C_u$ to V_{ref} is confirmed and the capacitance $(2^n - 1)C_u$ is tentatively connected to Vref during the 2^{nd} period. Depending on the value of the already determined MSB the new top plate voltage becomes

$$V_{comp}(2) = \frac{3V_{ref}}{4} - V_{in} \quad 1.2$$

(or)

$$V_{comp}(2) = \frac{V_{ref}}{4} - V_{in} \quad 1.3$$

for MSB =1 or MSB = 0 respectively. This voltage is then used to determine the next bit and the algorithm continues until all the n-bit are generated. Observe that parasitic capacitances affect the top plate voltage. Actually, the total parasitic Cp attenuates the generated voltages by a factor of α.

$$\alpha = \frac{C_u 2^n}{C_u 2^n + C_p} \quad 1.4$$

However, the attenuation factor is not a significant limit as it only reduces the comparator input but does not changes its sign, which is the relevant. For determining the bit, this feature is a

consequence of the pre-charging to zero of the top plate during the sampling phase. That voltage is zero during the sampling and is almost zero at the end of the conversion cycle.

The advantage of the charge redistribution method is that the input common mode range of the comparator is brought to zero without using op-amps or OTAs. Furthermore, only the comparator and the dynamic charging and discharging of the capacitive array determine the power consumption of the scheme [4].

Variations of the scheme of Figure 1.4 can use the auto-zero of the comparator to compensate for offset errors. In this case the gain stage is connected in the unity gain configuration and used to pre-charge the top plate of the array to the offset during the sampling phase. Another modification is the use of capacitive attenuation for limiting the capacitive spread in the binary weighted array. For this, one or more series capacitors are used to divide the array into sections that are all connected to ground during the sampling phase.

1.3 SAR ADC VERSUS OTHER ARCHIETECTURES

1.3.1 Versus pipelined ADC:

A pipelined ADC employs a parallel structure in which each stage works on one to a few bits (of successive samples) concurrently. The inherent parallelism increases throughput, but at the expense of power consumption and latency. However each stage uses active gain element whose power equals the one of many comparators. Latency in this case is defined as the difference between the time an analog sample is acquired by the ADC and the time when the digital data is available at the output.

For instance, a five-stage pipelined ADC will have at least five clock cycles of latency, whereas a SAR has only one clock cycle of latency. Note that the latency definition applies only to the throughput of the ADC, not the internal clock of a SAR, which runs at many times the frequency of the throughput. Pipelined ADCs frequently have digital error correction logic to reduce the accuracy requirement of the flash ADCs (that is, comparators) in each pipeline stage.On the other hand, a SAR ADC requires the comparator to be as accurate as the overall system. A pipelined ADC generally takes up significantly more silicon area than an equivalent SAR. Like a

SAR, a pipelined ADC with more than 12 bits of accuracy usually requires some form of trimming or calibration. Therefore the pipeline Archietecture is not good approch for ultra low power.

1.3.2 Versus flash:

Among the data converter Archietectures, the flash is a first generic option:it uses (2^{N-1}) comparators. However, the high number of comparators makes the archietecture too power hungry even for low resolutions. In a SAR ADC, however, the increased resolution requires more accurate components, yet the complexity does not increase exponentially. Of course, SAR ADCs are not capable of speeds anywhere close to those of flash ADCs.

1.3.3 Versus sigma delta and time interleaved:

Other Archietectures, like sigma delta and the time interleaved have similar limits because

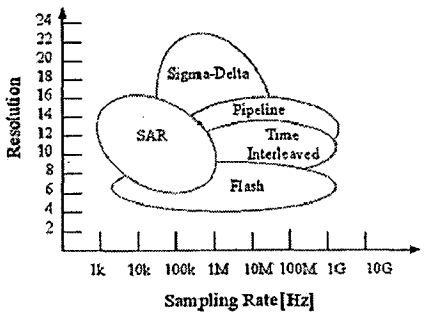

Figure 1.5 :Typical converter topologies as a function of the sampling rate and obtained resolution.

despite their use of speed or mulitple paths to increase resolution or throughput, they use active power hungry elements. However for the average speed the most suitable algorithm is the Successive approximation that uses a Successive Approximation Register(SAR) to control a DAC in a feedback loop with a single comparator. The cost is that it requires n+1 comparison cycles to achieve n-bit resolution.

The above considerations are summarized in Figure 1.5 that shows the best converter topologies as a function desired sampling rate and the required output bit resolution. The diagram depends

on the technology and the used supply voltage however SAR algorithm is preferable for signal bands up to one, two hundred of KHz.

1.4 Specifications of ADC:

A large set of specifications describe the performance of data converters. Specifications are used to interpret and understand the material in catalogues and to facilitate the use and characterization of products. Some specifications describe the features of either an ADC or a DAC, while others refer to the operation of both ADC and DAC. The specifications are divided into the following classes.

The specifications are divides as

1. Static specifications.
2. Dynamic specifications.

1.5. Static specifications:

The input-output transfer characteristic depicts the static behavior of a data converter. For an ideal case the input-output characteristic is a staircase with uniform steps over the entire dynamic range. If the first and last steps are $\Delta/2$ then the full-scale range is divided by ($2^n - 1$)instead of 2^n to give Δ. Figure outlines that a quantization interval can be encoded using both digital code or mid step point. As known, the quantization error ranges between $\pm\Delta/2$ and is equal to zero at the mid step. Deviations from the ideal transfer characteristic produce results like the ones shown in Figure 1.6. The curve of Figure 1.6(a) shows an almost random variation of the quantization intervals. There is no correlation between successive errors. The figure also shows the interpolating curve as a straight line running from the origin to the full scale. The characteristics of Figure 1.6(b) display small quantization intervals at the beginning and large quantization intervals at the end of the curve. As a result, the interpolating curve moves away from the straight line leading to a distorted response. These features are quantified by the INL and DNL, two of the static specifications defined below

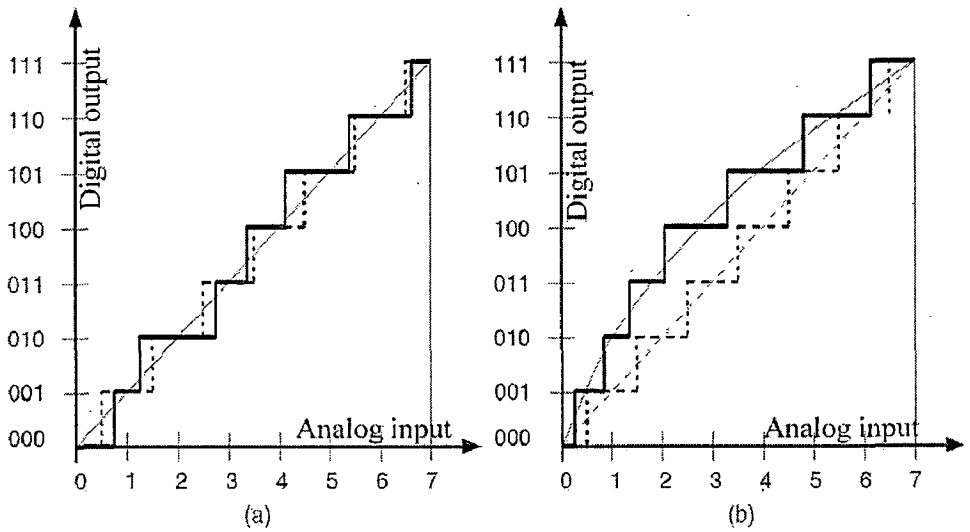

Figure1.6: Input-output transfer characteristic of a real data converter.

1.5.1 Analog Resolution: is the smallest analog increment corresponding to a 1 LSB code change. For example, the resolution of a 16 bit converter with X_{FS}=1 is $15.26.10^{-6}$=15.26μs.

1.5.2 Analog Input Range: is the single ended or differential peak-to-peak signal (voltage or current) that must be applied to the A/D converter to generate a full-scale response. A peak differential signal is the difference between the two 180^0 out of phase signal terminals. Peak-to-peak differential is computed by rotating the inputs phase 180^0, taking the peak measurement again and subtracting it from the initial peak measurement [5].

1.5.3 Offset: the offset describes a shift for zero input. Offset is an error that can affect both an ADC and a DAC. Figure 1.6 (a) compares the input-output transfer characteristics of a real and an ideal ADC. The offset changes the transfer characteristics so that all the quantization steps are shifted by the ADC offset. The offset of a DAC is defined by using the real response of Figure 1.6(b). The analog signal generated by the digital code $0 \cdots 0000$ is the DAC offset. The offset can be measured in LSB, absolute value (volts or amperes), or as % or ppm of the full scale.

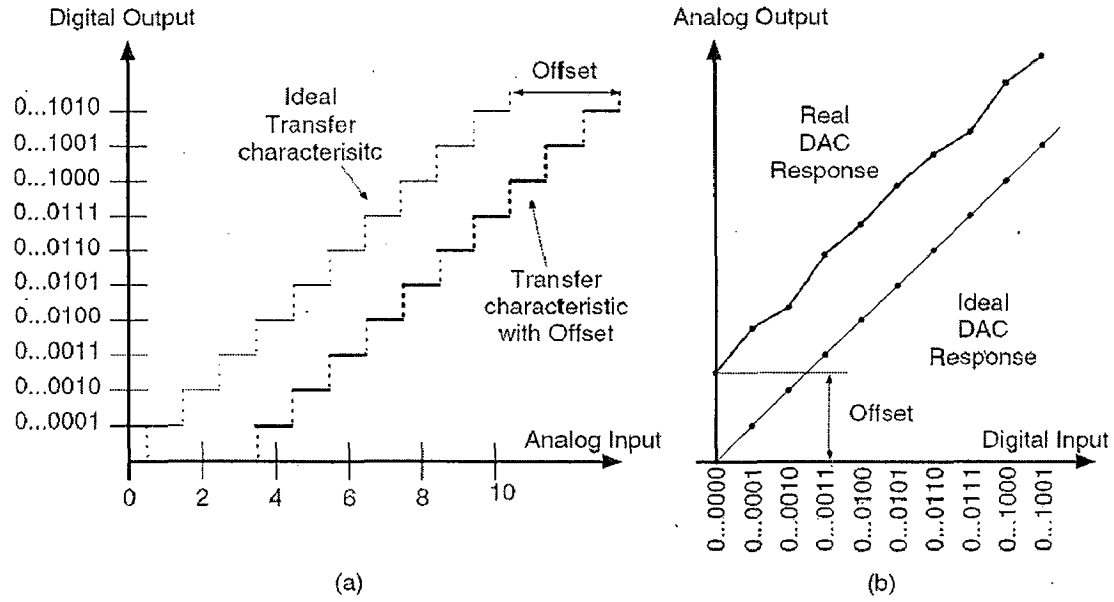

Figure 1.7: Gain error for an analog-to-digital (a) and a digital-to-analog (b) converter.

1.5.4 Zero Scale Offset: some ADC data sheets provide this parameter. It is the difference between the ideal input voltage (1/2 LSB) and the actual input voltage that just causes a transition from an output code of all zeros to an output code of one.

1.5.5 Common-mode Error: this specification applies to ADCs with differential inputs. It describes the change in the output code that occurs when the common-mode analog voltage changes by a given amount. The equal change of the two analog inputs that cause one LSB code transition is usually measured in LSBs.

1.5.6 Full-scale Error: is a measure of how far the last code transition of an ADC is from the ideal top transition immediately below V_{ref+}.It is normally measured in LSB.

1.5.7 Gain error: is the error on the slope of the straight line interpolating the transfer curve. For an ideal converter the slope is D_{FS}/X_{FS}, where D_{FS} and X_{FS} are the full-scale digital code and full-scale analog range respectively. Since D_{FS} represents X_{FS}, we normally say that the ideal slope is one. The gain error defines the deviation of the slope of a data converter from the expected value.

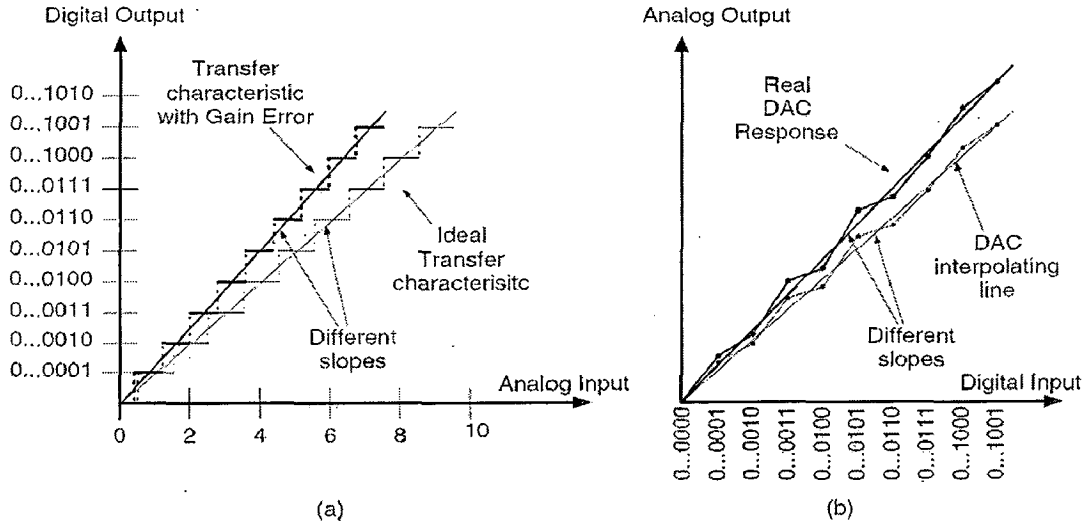

Figure 1.8: Input-output diagrams for a real and an ideal ADC (a) and DAC (b).

Another measure of the gain error is given by the difference between the input voltage causing a transition to the full scale and the reference (minus half LSB). When using this definition the gain error is known as the full scale error.

1.5.8 Differential non-linearity error (DNL): is the deviation of the step size of a real data converter from the ideal width of the bins Δ. Assuming that X_k is the transition point between successive codes k−1 and k, then the width of the bin k is $\Delta_r(k) = (X_{k+1} - X_k)$ the differential non-linearity is

$$\mathrm{DNL(k)} = \frac{\Delta_r(k)-\Delta}{\Delta} \qquad 1.5$$

This function is also known as the differential linearity error (DLE). Fig. 2.6 shows an example of DNL for a 12-bit ADC. The diagram shows the error to be within a ±0.5 LSB interval over the entire dynamic range. Fig. 2.6 measures the DNL in LSB. The DNL can be also measured in Volts (or amperes when the input is a current) or as % or ppm of the full scale. The maximum differential nonlinearity is the maximum of |DNL(k)| for all k.

$$DNL_{\mathrm{RMS}} = \left\{\frac{1}{2^{N-2}} \sum_1^{2^N-2} \mathrm{DNL}\,(k)^2\right\}^{1/2} \qquad 1.6$$

Often the maximum differential nonlinearity is simply referred to as DNL. An additional specification given by some data sheets is the root mean square (RMS) of the DNL.

1.5.9 Monotonicity:

Is the ADC feature that produces output codes that are consistently increasing with increasing input signal and consistently decreasing with decreasing input signal. Therefore, the output code will always either remain constant or change in the same direction as the input.

1.5.10 Integral non-linearity (INL): is a measure of the deviation of the transfer function from the ideal interpolating line. Another definition of the integral non-linearity measures the deviation from the endpoint-fit line[5]. The use of the endpoint-fit line corrects the gain and offset error. The second definition is chosen as standard since it is more informative for estimating harmonic distortion. Figure 2.0 shows an example of an INL plot drawn using

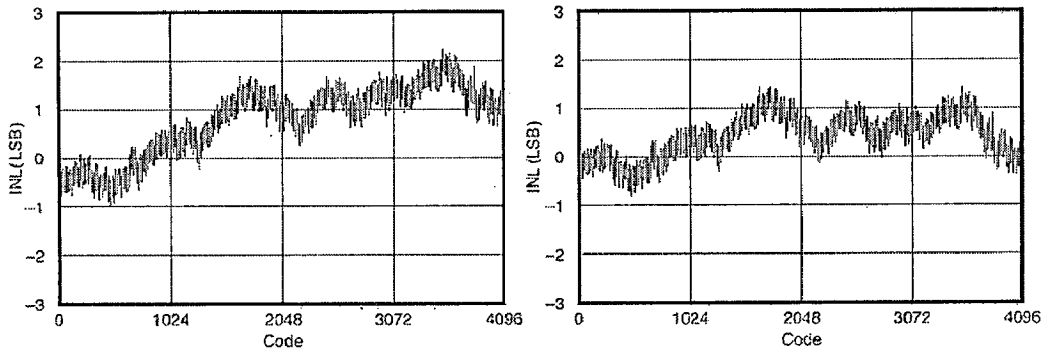

Figure 1.9: INL obtained with the ideal interpolation line (left), or the endpoint-fit line (right).

1.6 Dynamic specifications:

The frequency response and speed of the analog components of a data converter determine its dynamic performance. Obviously, the performance becomes critical when the input bandwidth and the conversion-rate are high. Therefore, the specifications either correspond to defined dynamic conditions or are given as a function of frequency, time, or conversion data-rate. A quality factor of a dynamic feature is its capability to remain unchanged within the entire range of dynamic operation.

1.6.1 Analog Input Bandwidth: specifies the frequency at which a full-scale input of an ADC leads to a reconstructed output 3dB below its low frequency value. This definition differs from what is used for amplifiers which usually use a small signal input.

1.6.2 Input Impedance: is the impedance between the input terminals of the ADC. At low frequency the input impedance is a resistance: ideally, it is infinite for voltage inputs and zero for current inputs (thus leading to an ideal measure of voltage or current.) At high frequency the input impedance is dominated by its capacitive component. Often, a switched capacitance structure performs the input sampling. In this case the specification provides the equivalent load at the input pin. At very high frequency the input impedance of the ADC must be the matched termination of the input connection.

1.6.3 Settling-time: is the time at which the step response of a DAC enters and subsequently remains within a specified error band around its final value. The input is a step signal applied at time t=0. The final value is defined to occur a long time after the beginning of the step.

1.6.4 Aperture uncertainty (Clock Jitter): is the standard deviation of the sampling time. It is also called aperture jitter or timing phase noise. It is normally assumed that clock jitter is like a noise with a white spectrum.

1.6.5 Signal-to-Noise Ratio (SNR): is the ratio between the power of the signal (normally a sine wave) and the total noise produced by quantization and the noise of the circuit. The SNR accounts for the noise in the entire nyquist interval. The SNR can depend on the frequency of the input signal and it decreases proportional to the input amplitude.

1.6.6 Signal-to-Noise-and-Distortion Ratio (SINAD or SNDR): is similar in definition to the SNR except that non linear distortion terms, generated by the input sine wave, are also accounted for. The SINAD is the ratio between the root-mean-square of the signal and the root-sum-square of the harmonic components plus noise (excluding dc). Since static and dynamic limitations cause a non-linear response the SINAD is dependent on both the amplitude and frequency of the input sine wave.

1.6.7 Dynamic Range: is the value of the input signal at which the SNR (or the SINAD) is 0 dB. The parameter is useful for some types of data converters that do not obtain their maximum SNR (or SINAD) at 0 dBFS input. The peak of the SNR is at 74 dB while the dynamic range is 80dB. Therefore, the peak of the SNR occurs approximately at −6dBFS.

1.6.8 Effective-Number-of-Bits (ENOB): measures the signal-to-noise and distortion ratio using bits. SINAD in dB and ENOB are linked by

$$\text{ENOB} = \frac{\text{SINAD}_{\text{dB}} - 1.76}{6.02} \tag{1.7}$$

1.6.9 Harmonic Distortion (HD): is the ratio between the root-mean-square of the signal and the root-mean-square of harmonic components including aliased terms. Unless otherwise specified the HD accounts for the second through tenth harmonics.

CHAPTER 2

2.1 SAMPLE AND HOLD CIRCUIT

The function of sample and hold circuit is to sample an analog input signal and hold this value over a certain length of time for subsequent processing. The main important building block of sample and hold circuits are switches. Generally transistors are used as switches for every sampled data system.

The main limitations of such a building block have been recognized in the following pages such as finite (and input dependent) on resistance and charge injection. These limitations should be re-examined in the context of very low voltage operation.

Taking the advantage of the excellent properties of MOS capacitors and switches, traditional switched capaciotr techniques can be used to realize different sample and hold circuits[6].

2.2 Basic sample and hold circuit:

The simplest S/H circuit in MOS technology is shown below, where V_{in} is the input signal, M_1 is an MOS transistor operating as the sampling switch, C_h is the hold capacitor, ck is the clock signal, and V_{out} is the resulting sample and hold output siganl.

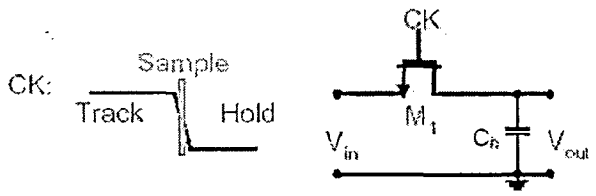

Figure 2.1 : Simplest sample and hold circuit in MOS technology.

As depicted by the figure in the simplest sense, a S/H circuit can be achieved using only one MOS transistor and one capacitor. The operation of this circuit is very straight forward, whenever ck is high, the MOS switch is on, which in turn allows V_{out} to track V_{in}. On the other

hand, when ck is low, the MOS Switch is off. During this time, C_h will keep V_{out} equal to the value of V_{in} at the instance when ck goes low.

Unfortunately ,in reality,the performance of this S/H circuit is not as ideal as described above. The major two types of errors in this circuit are

1.charge injection.

2.clock feedthrough.

2.3 Charge injection:

When a MOS switch is on, it operates in the triode region and its drain to source voltage, V_{ds} is approximatley zero. During this time transistor is on, it holds mobile charges in its channel. Once the transistor is turned off, these mobile charges must flow out from the channel region and into the drain and the source junction as depicted in the follwing figure

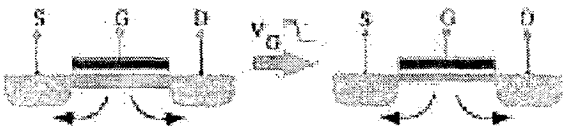

Figure 2.2: Channel charge when MOS transistor is in triode region.

For the S/H circuit in fig, if the MOS switch M_1 is implemented using an NMOS transistor, the amount of channel charge ,Q_{ch} this transistor can hold while it is on is given equation by

$$Q_{ch} = -WLC_{ox}\,(V_{DD} - V_{th} - V_{in}) \qquad 2.0$$

where W and L are the channel width and channel length of the MOS transistor, C_{ox} is the gate oxide capacitance, and V_{th} is the threshold voltage of the NMOS device. When the switch is turned off, some portion of the channel charge is released to hold capacitor C_h while the rest of the charge is transferred back to the input, V_{in}.The fraction k of the channel charge is injected onto C_h is given by the Equation 2.2

$$\Delta Q_{ch} = kQ_{ch} = -kWLC_{ox}(V_{DD} - V_{th} - V_{in}) \qquad 2.1$$

As a result the voltage change at V_{out} due to this charge injection is given by equation below

$$\Delta V_{out} = \left(\frac{\Delta Q_{ch}}{C_h}\right) = -\frac{kWLC_{ox}(V_{DD}-V_{th}-V_{in})}{C_h} \quad 2.2$$

Note that V_{out} is linearly related to V_{in} and V_{th}. However , V_{th} is nonlinearly related to V_{in}. Therefore charge injection introduces nonlinear signal dependent error into the S/H circuit.

2.4 Clock feedthrough:

Clock feed through is due to the gate-to-source overlap capacitance of the MOS switch. For the S/H circuit of Figure 3.1 the voltage change at V_{out} due to the clock feed through is given by Eqn.

$$\Delta V_{out} = \frac{-C_{out}(V_{DD}-V_{ss})}{C_{para}+C_h} \quad 2.3$$

Where C_{para} is the parasitic capacitance. The error introduced by clock feed through is usually very small compare to charge injection. Also, notice that clock feed through is signal-independent which means it can be treated as signal offsets that can be removed by most systems. Thus, clock feed through error is typically less important than charge injection.

Charge injection and clock feed through are due to the intrinsic limitations of MOS transistor switches. These two errors limit the maximum usable resolution of any particular S/H circuit, and in turn, limit the performance of the whole system. New S/H techniques must be developed to reduce these errors.

The main drawback for circuit shown in the Figure 2.2 is as the input signal varies the resistance of the switch varies and varies the bandwidth of the sampling circuit. This can be solved by using the following technique called Boot strapped sample and hold circuit.

2.5 Boot strapped sample and hold circuit:

Charge pumps provide higher voltages than their supply voltages. However, the use of charge pumps for generating a control that is a multiplied version of V_{DD} is not suitable for clocking

MOS switches. The reason is that the driving can be adequate when the input signal is close to the supply voltage, but the gate-to-source difference can become too high when the input signal is close to zero. As a matter of fact, high gate-to-source voltages cause failures due to various mechanisms. When short channel lengths are used in deep sub-micron technologies the so-called "hot electrons" or "hot holes" effect degrades the transistor threshold over time. Moreover, high electric fields degrade the oxide breakdown voltage, increasing the local tunneling current that is responsible for oxide lifetime reduction [10].

The above arguments motivate the switch bootstrapping method which ensures that the stress on the gate is always below its technologic limit. The method is conceptually based on the scheme of Fig. that uses a charged capacitor to sustain the gate-to-source voltage of M_S during the on-phase. The switch S_{OFF} grounds the gate of the switch M_S during Φ_{OFF} and, at the same time, switches S_1 and S_2 charge the boosting capacitance C_B to the supply voltage. The switches S_3 and S_4 connect C_B between the source and drain of M_S during Φ_{ON} to obtain gate boosting.
Actually, the voltage at the gate of M_S does not increase by $V_{in}+V_{DD}$ but, due to the initially discharged parasitic capacitance C_p, goes to

$$V_{GS} = (V_{in} + V_{DD})\frac{C_B}{C_B+C_P} \qquad 2.4$$

leading to a gate-to-source voltage which will be lower than V_{DD} and also dependent on the input voltage.

$$V_{GS,MS} = V_{DD}\frac{C_B}{C_B+C_P} \qquad 2.5$$

This limit is reduced by using relatively large boosting capacitances and small gate areas for all transistors connected to G_S. The on-conductance of M_S becomes describing the mentioned reduced boosting effectiveness and a slight on-resistance dependence on the input voltage.

$$G_{on} = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[V_{DD}\frac{C_B}{C_B+C_P} - V_{in}\frac{C_p}{C_B+C_p} - V_{Th,n}\right] \qquad 2.6$$

The circuit implementation illustrating the boot strapping concept is shown in Figure 2.3. Should ensure the proper driving of the switch transistors, thus avoiding any direct biasing of the

channel-substrate diodes, and providing suitable protection for the drains that undergo large voltage swings

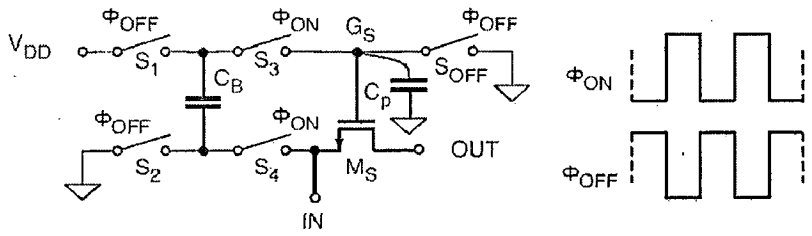

Figure 2.3: Boosting concept

Accordingly, it is necessary to satisfy the following conditions:

1) S_1 must be able to switch on and off V_{DD}.

2) The switch S_3 must sustain the boosted voltage during the on phase.

3) The switch S4 must operate under the same conditions as the main switch.

4) S_{OFF} must be able to swing from the boosted voltage to zero.

A possible switch boosting scheme is the one shown in Figure 2.3 .which highlights the transistors used to realize the five switches. Since switch S_1 is an n-channel transistor, control of its gate requires a voltage higher than V_{DD} and, for this, the scheme uses a voltage doublers made by the cross pair Md_1 and Md_2, and the charge pumping capacitances C_1 and C_2 driven by Φ_{OFF} and its inverse. Since the charge pump biases the gate of M_1 to V_{DD} during Φ_{ON} and up to $2V_{DD}$ during Φ_{OFF}, the boosting capacitance C_B charges to V_{DD} (because S_2 is also on) Switch S_3 is realized by the p-channel transistor M_3. The inverter Mi_1 and Mi_2 whose output during Φ_{ON} goes to the voltage of the bottom plate of C_B drives the gate of M_3. Sometimes the transistor Mi_3 takes the control if switch S_4 pushes the source of Mi_1 above the control of the inverter [11].

The boosted voltage of node G_S has two effects: it switches both S_4 and M_S on, and it gives rise to a high voltage at the drain of Mo,(the transistor realizing S_{OFF}).The high-voltage drain protection of M_o is ensured by Mp_o that, during Φ_{ON}, distributes the boosted voltage between Mp_o and M_o. Observe that the source-to-well connection of M_3 avoids any possible latch up. Moreover, the use of an n-channel transistor for S_1 requires voltage doublers but is less problematic than using a p-channel switch, as the proper biasing of a p-channel device would

have required switching between V_{DD} during one phase and the boosted voltage during the other phase. The input voltage of the scheme of Figure 2.4 cannot exceed V_{DD} as the switching on of Mi_3 applies the input voltage to the drain of Mi_2. Since the well of Mi_2 is at V_{DD} a higher drain voltage would forward bias the well drain diode. Therefore, input voltages higher than V_{DD} require more complex boosting schemes.

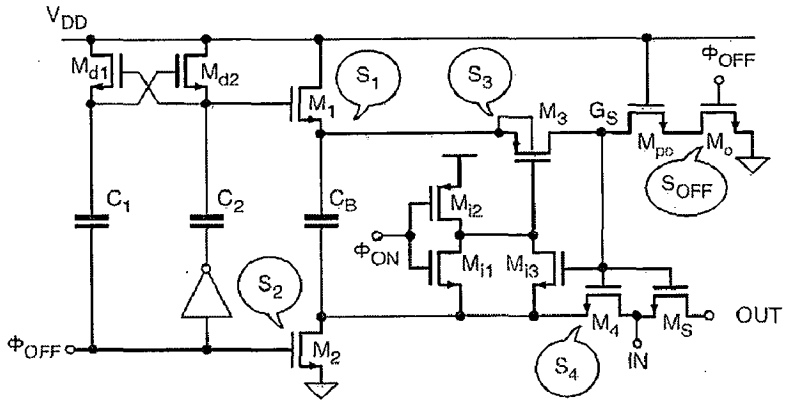

Figure 2.4: Boot strapped sample and hold circuit.

The drawback of the above circuit is that nmos S_1 device is used for charging the capacitor, so it requires additional circuit of the clock doublers scheme for the operation. Fig below shows the circuit which uses pmos device to charge the capacitor.

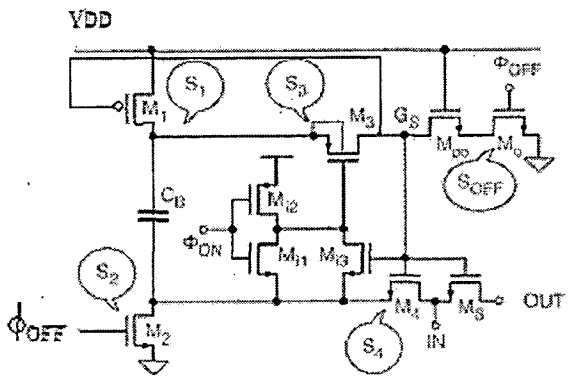

Figure 2.5: Circuit uses pmos device for charging the capacitor.

The sample and hold output waveforms of the above circuits is as follows in Figure 2.6.

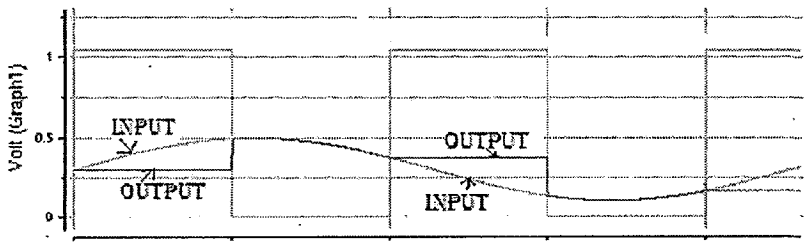

Figure 2.6: Input and output waveforms of sample and hold circuit.

If we observe carefully the above waveforms the input signal once is greater than the output and once it is less than output. This shows that for nmos the drain and source are exchanging for every T/4 cycle of input. This causes great harmonics in the output of the circuit and reduces the SNDR of the circuit.

The mathematical equations for the above circuit is as follows,

$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS}-V_{th})} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{DD}-V_{th}-V_{in})} \quad 2.7$$

If we fix V_{GS} to V_{DD} then the R_{ON} can be fixed in one quarter of the cycle where output is greater than input.

Another way of doing the same operation is the nmos device for the sampling switch can be replaced by the pmos device. As for a particular CMOS technology the bulk of the pmos can be accessed. Now the source and bulk of the switch needs to be connected to V_{DD} to avoid the second order effects of the distortion. This can be done by identifying the source and drain terminal during the entire operation and need to be connected to V_{DD}.

This can be done by comparing the source and drain by means of comparator and then connecting it into the bulk. The Figure 2.6 shows the schematic of the circuit. Through the above discussion, a key point is that a "source follower" is needed to track the "real source" connecting the charged capacitor and maintaining the gate overdrive to be a constant voltage "V_{DD}". Figure2.6 shows the proposed circuit. The sampling switch is composed of a comparator and several switches. Besides some necessary switches of a typical bootstrapped sampling switch, additional switches S_{W6} and S_{W7} are added. To ensure rail to rail swing, S_{W6} and S_{W7} are made of

complementary switches. The comparator is used to trigger S_{W6} and S_{W7} to make the bulk connect to the real source terminal. The bulk is guaranteed to connect to only one terminal, the source terminal, during the "on" state. We adopt the structure of direct connection between source and bulk because it has less nonlinearity and large input swing than using a replica. In the standard CMOS technology, the sampling switch should be p-type. Two cases are discussed in the following where V_{in} represents input signal and V_{out} represents the voltage sampled in the "on" state [11].

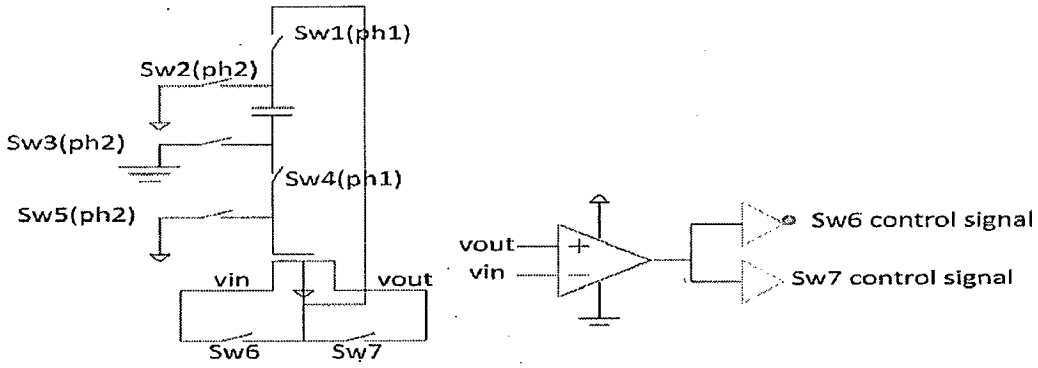

Figure 2.7: The proposed circuit.

Case 1: When $V_{in} > V_{out}$, the real source is the input terminal. During "off" state (S_{W2}, S_{W3}, and S_{W5} on), the capacitor would be charged to V_{DD}. During the "on" state (S_{W1} and S_{W4} on), the comparator output will be low to turn on S_{W6} to make a connection between the input and bulk because input voltage is higher than V_{out}. And the gate voltage of switch equals V_{IN}-V_{DD}. Then the gate overdrive V_{SG} and V_{SB} exactly equals V_{DD} and zero respectively, during the "on" state.
Case 2: When $V_{in} < V_{out}$, the real source terminal should be the output terminal. It is certainly the reverse of case1.The S_{W7} would be turn on by the comparator to connect the output and bulk. The gate voltage would become V_{OUT} -V_{DD} and the source voltage is also V_{out}. The gate overdrive (V_{SG}) still maintains exact V_{DD}. And threshold voltage is also held constant.

$$V_{source} = V_{out}, V_{gate} = V_{out} - V_{DD}, V_{tp} = V_{to}, V_{sg} = V_{DD} \quad 2.8$$

$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{DD} - |V_{to}|)} \quad 2.9$$

During "on" state, when the difference between input and output becomes "zero", the comparator would be low and SW6 would be turn on again. At this time, we do not care which terminal is source because V_{in} already equals the sampled signal.

CHAPTER 3

3.1 Voltage to Time domain comparator:

The second element that consumes power in SAR ADC is the comparator. Since the input differential signal of a latch should be at least 20 mV to avoid latching errors, it is necessary to use a preamplifier. The LSB of a 10-12-bit ADC is a fraction of mV, therefore, the differential dynamic gain of the preamplifier should be in the 30-60 dB range. The trans-conductance of the input pair used in the preamplifier with input voltage V_{in} determines a signal current, $g_m V_{in}$, that charges a parasitic capacitance, C_p, for the pre amplification time, T_p. The output voltage at the latch time becomes

$$V_{out} = V_{in}\frac{g_m T_p}{C_p} = V_{in}\frac{I_B T_p}{mV_T C_p} \qquad 3.0$$

where I_B is the bias current of the input pair. Moreover, it is assumed that the MOS transistors of the input pair are in weak inversion (m=2.2). Above Equation 3.0 determines the minimum current for a given clock frequency, dynamic gain, V_{LSB} and parasitic capacitance loading the preamplifier output. Cp is given by the parasitic of the preamplifier output and the input parasitic of the latch. Assuming a preamplifier made by a cascode structure, C_p for 32nm CMOS technology is estimated to be 40fF.

With V_{LSB} = 0.2mV, T_p=380ns, and V_{out}=20 mV, the bias current I_B equals 0.76µA.Even if this current consumption is already very low, the figure can be improved by using a new proposed time-domain comparator structure that, instead of operating in the voltage domain, transforms the input voltage into a pulse whose duration is compared with half period of the master clock.

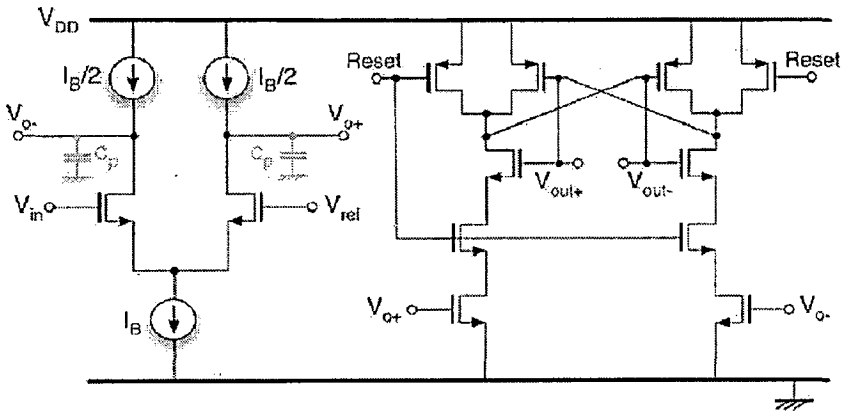

Figure 3.0: Preamplifier followed by latch.

Figure 3.0 shows the circuit schematic of the voltage-to-time (V2T) cell, used to generate the pulse. The input voltage V_{in} establishes a current through R_D that charges capacitor C_L. When the clock signal is low, transistors M_1 charges the capacitor C_L [1]. In the meantime, transistor M4 discharges the parasitic capacitor C_P to cancel out any memory of the previous conversion. When clock rises, transistors M_2 turns on and the current generator made by M_3 and R_D discharge C_L at constant rate. If the input voltage is constant and produces VR across R_D, then

$$I_D = \frac{V_R}{R_D} \qquad 3.1$$

When, after a given time Td, the voltage across C_L, V_C, crosses the threshold of M_5, OutV2T rises up, driven by the tapered inverter chain. OutV2T drives also the logic which turns off M_2 for saving power, as the operation avoids to complete discharge C_L. Fig conceptually shows the V2T cell operation.

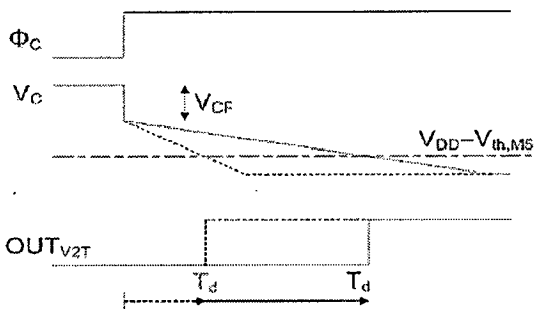

Figure 3.1: Voltages across the C_L.

For the used configuration Td increases when the input voltage is reduced and vice-versa. Moreover, since the parasitic capacitor C_P is discharged by M_4, its series connection with C_L gives an initial charging of C_L itself. Therefore, voltage V_C immediately falls to

$$V_{CF} = V_{DD} \frac{C_p}{C_L + C_p} \quad 3.2$$

Then the constant rate discharge of C_L starts. The initial drop of V_C has positive effects because it reduces Td without increasing the discharge current. Splitting C_L in two parts, C_{L1} and C_{L2}, enhances the drop. where C_{L1} is connected to ground as in the scheme, C_{L2} is connected between ground and the source of M2 and pre-discharged to ground by a switch that ties the source of M_2 to ground during clk bar. Neglecting C_P, the drop of V_C becomes

$$V_{DD}\left(\frac{C_{L2}}{C_{L1} + C_{L2}}\right) \quad 3.3$$

Figure 3.0.shows the block diagram of the comparator together with its timing. It consists of a V2T cell and a flip-flop delay (FFD). The time-domain comparator output voltage, Output of the comp, is then used as input of the SAR. Slightly after the crossing of the threshold, the logic opens M_2 and stops the flow of current through R_D. Therefore, if V_C is the drop of the voltage VC giving rise to the bit detection, the energy per clock period consumed by C_L is$C_L = \Delta V_c^2$.

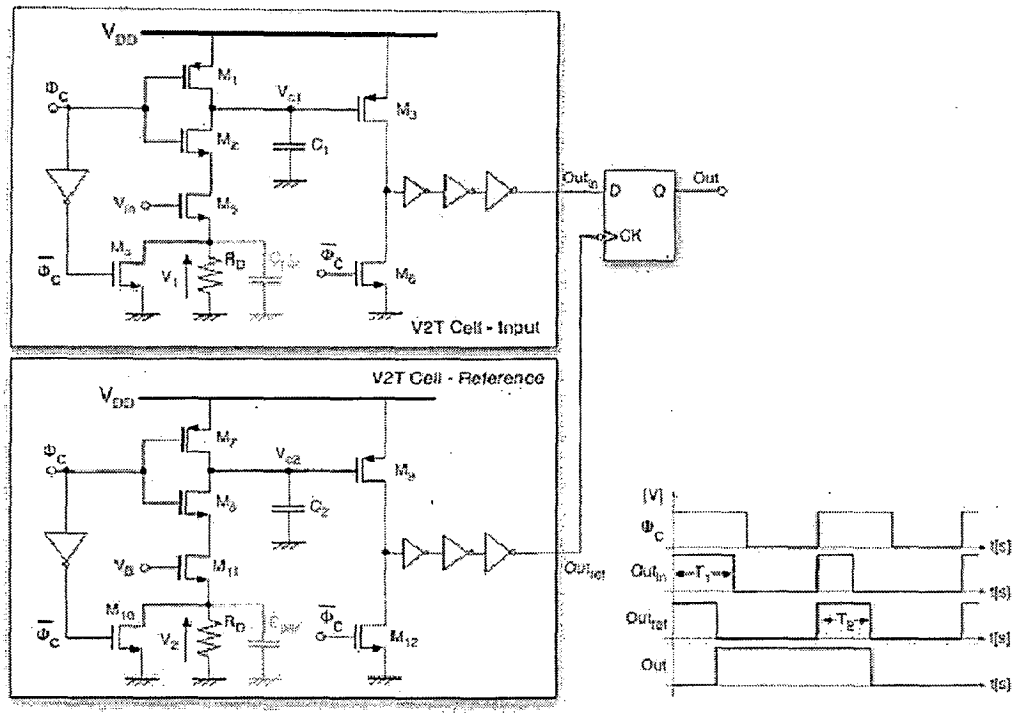

Figure 3.2: Two V2T cells determine the core of the comparator.

The components size of the Voltage to time domain cells depends on the period of time available for comparison and the accuracy. Two factors influence the time accuracy: the kT/C noise voltage across C_1 and C_2, and the latch plus jitter time error ΔT [4].

The design parameters of the V2T are determined by the required accuracy that, by turn, is controlled by three main factors: the kT/C noise, the input referred noise of M_5, vn,5, and the minimum distance between clock and D input in the FFD. Since the time for discharging C_L by ΔV_C is $T_0 = ¾\ T_{CIK}$, the bias value of V_A must produce across R_L a drop voltage ΔV_R such that $\Delta V_C/\Delta V_R = T_0/R_LC_L$. Therefore, an LSB added to the bias of V_A determine a $\Delta V_C = LSB \cdot T_0 /RLCL = LSB \cdot \Delta V_C/\Delta V_R$ variation at $t=T_0$.

Therefore, the amplification of the LSB by $A_0= \Delta V_C/\Delta V_R$ must be lower than the equivalent noise across C_L, i.e. the quadratic superposition of sqrt(2kT/CL) with vn,5. If $C_L = 0.8$ pF, vn,5 = 130μV and $A_0 = 2$, the LSB, that equals the noise, is as low as 83μV. The nominal slope of the discharge of V_{CL} is $\Delta VC/T_0$, accordingly, a time uncertainty δt in the operation of the FFD corresponds to an input referred noise $\delta V_A=\delta t^* \Delta V_C/T_0/A_0$. With $\Delta V_C = 0.2$ V, $T_0= 0.5\mu s$ and δt

= 250ps, δV_A=43μV. The value of R_L is 150kΩ and the average consumed power per comparison is 0.5pW.

The main cause of the offset in this comparator is mismatch in the lengths of the two critical transistors. The paper presented will take care for one time offset calibration but the technique implemented in this work will reduce the offset to great extent.

The offset of the comparator can be reduced with switching the inputs and outputs of the comparator during one conversion time and performing the normal operation during the another time and averaging the both the output bits by means of a adder and performing the right shifting the averaged bits will results the reduced offset and increases the resolution and ENOB with increase in the power consumption and reduced sampling frequency. The simulations are performed with both the conditions and manually added them and right shifted to verify whether the offset effect is removed or not.

For a particular process technology the length variation after chip fabrication will be of 5% error Considering that into account and calculating the offset in terms of time domain will be 507ps, and the amount of input voltage required to make the offset zero is 700μv less for the reference input, so that the correct comparison can be done.

The power supply rejection ratio for the comparator at zero frequency is -60dB. The waveform below shows the PSRR at zero frequency i.e. dc gain with 100 kHz noise on the supply lines.

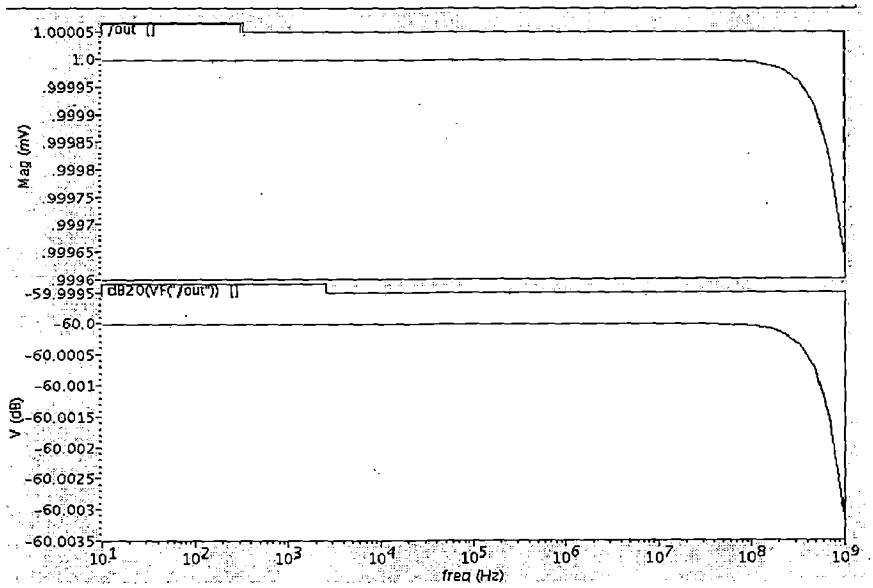

Figure 3.3: PSRR for the comparator.

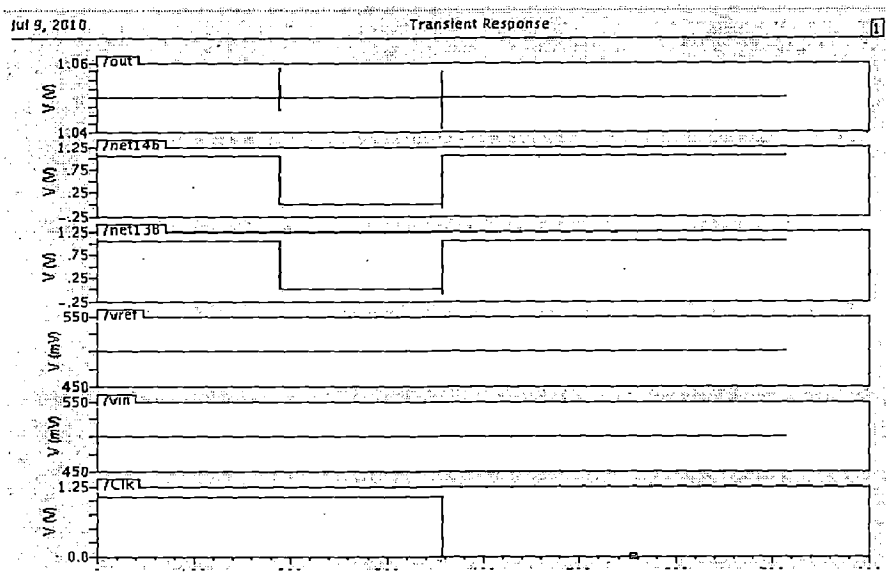

Figure 3.4: Bit comparison in TTTT corner.

simulation results of the comparator in different process corners giving the desired results are shown below.

Process corners	supply voltage	Temperature	Bit-comparison
TTTT	1.05	50^0C	correct
FFFF	1.155	-3^0C	correct
SSSS	0.945	110^0C	correct

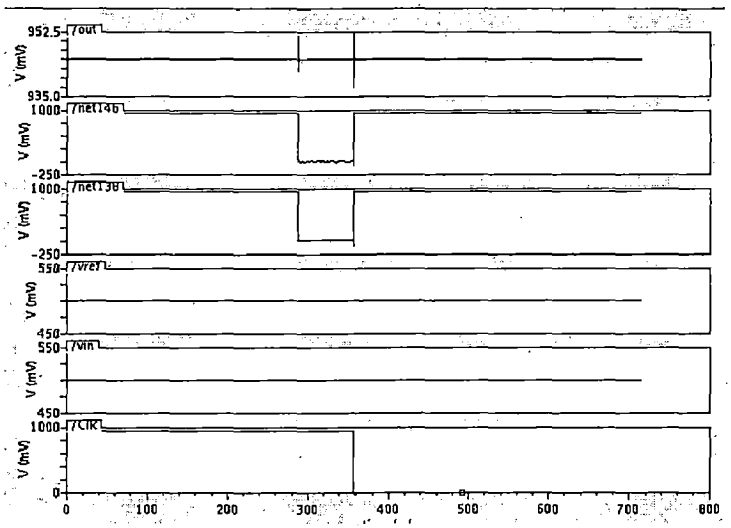

Figure 3.5: Bit comparison in SSSS corner.

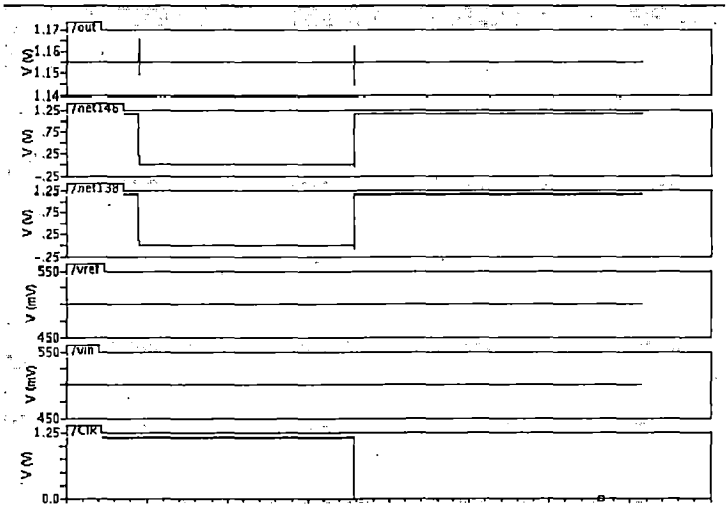

Figure 3.6: Bit comparison in FFFF corner.

3.2 D Flip-flop design:

Synchronous pipelined structures have been extensively used in digital systems to achieve high-speed operation. These are composed of registers and several stages of combinational logic circuits between the registers. The registers can be D flip-flops (DFFs). The data flow in such structures is synchronized using a system clock. The speed of the system clock is constrained by the setup time of the DFFs (t_{setup}) the propagation delay time of the DFFs (t_{pFF}) and the propagation delay time of the combinational circuits (t_{pcomb}) following relation must hold for the circuit to operate correctly.

$$T > t_{setup} + t_{pFF} + t_{pcomb} \qquad 3.4$$

Where T is the time period of the system clock. To increase the speed of the system, it is necessary to minimize each of the three time parameters ($t_{setup} + t_{pFF} + t_{pcomb}$), our aim in this design is to reduce the setup time of DFFs.

There are two commonly used DFFs: static and dynamic DFFs. Dynamic DFFs usually have a shorter setup time than static DFFs. A system can run at a higher speed if dynamic DFFs are used. Dynamic DFFs store signal values as a charge on parasitic capacitors. However, because the charge on capacitors tends to leak away with time, dynamic DFFs can only be used when the system clock is continuously running. By contrast, static DFFs use positive feedback to implement the memory function and can store a signal value indefinitely without regular refreshing. The ability to store a signal value without regular refreshing is extremely important in low power design, where circuits might be partially or completely idled. In this design, we have implemented a method to reduce the setup time of static DFFs to a level equivalent to that of dynamic DFFs, thus making it possible for a system utilizing the proposed static DFF to achieve high-speed operation and power efficiency at the same time.

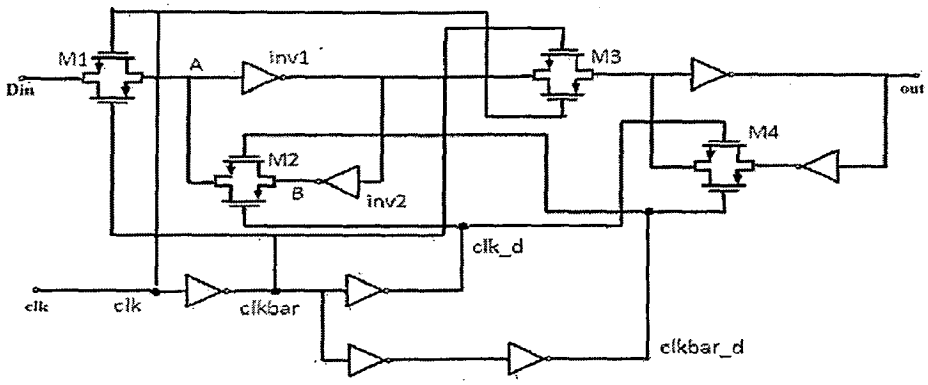

Figure 3.7: D Flip flop with reduced setup time and hold times.

3.3 Reduced setup time static DFF:

The proposed DFF uses two sets of clocks, as shown in Figure 3.5. The clocks applied on transmission gates M_1 and M_3 are denoted as clk , and clkbar, and the clocks applied on gates M_2 and M_4 are denoted as clk_d and clkbar_d. Clocks clk_d and clkbar_d are generated by delaying clocks (clk & clkbar) respectively, with two stages of inverters. The proposed static DFF has a reduced setup time compared to that of a conventional static DFF. The conventional static DFF shown in Figure 3.5 is a positive edge-triggered static DFF. When the clock φ is low, the data D is loaded to node A and stored in the first memory unit composed of inverters INV_1, and INV_2.

When the clock clk, goes high, the data stored in the first memory unit is propagated to the output terminal. In order for the DFF to function correctly, a sufficiently large setup time is required to allow the new data to be propagated to node B, through the path of node A, INV_1, and INV_2 .If the clock is too fast, the DFF will not have sufficient setup time and the following scenario might cause the DFF to not function correctly. Assume that the clock is low and the input data changes from low to high, then the signal at node A will change from low to high. At this moment, due to the delay of inverters, INV_1 and INV_2 node B is still in the previous state. If the clock goes high before node B changes to the present state, the transmission gate M_2 will be closed, causing the data previously stored at node B to be propagated to node A. If the previous data is different from the new data, they will 'fight' with each other. Since the transmission gate M_I is now open, the final state of node A is uncertain and the DFF may function incorrectly.

From the above analysis, the worst-case setup time of conventional static DFFs can be estimated by the following equation:

$$t_{setup\_conv} = t_{dm1} + t_{dinv1} + t_{dinv2} + t_{dm2} + t_{fight} \quad 3.5$$

Where tdm1, t_{dinv1}, t_{dinv2} & t_{dm2} are the delay times of transmission gate M_1, inverter INV_1, inverter INV_2, and transmission gate M_2 and is the 'fighting' time when the new data is different from the previous data stored in the DFF. The proposed design uses two sets of clocks on gates M_1, and M_2. When clock clk, is low, the new data is propagated to node A through M_1. Then, as soon as the new data is propagated to the output of INV1, the clock can go high and the new data can be propagated to the output of the DFF. Since clock clk_d is the delayed version of clock φ, when clock clk goes high, clock clk_d is still low. Thus, gate M_2 is still open and the previous data stored at node B cannot be propagated to node A through M_2.The 'fighting' condition between the new data and the previous data is then avoided. As a result, the setup time of the proposed DFF t_{setup_prop} reduced. Comparing the operation of the proposed static DFF with the dynamic DFF shown in Fig. we find that their setup times are the same and can be estimated from the following equation.

$$t_{setup\_prop} = t_{setup\_dynamic} = t_{dm1} + t_{dm2} \quad 3.6$$

Where $t_{setup\_dynamic}$ setup time of the dynamic DFF shown in figure above.
The setup time of the D flip flop designed above is 50ps.

CHAPTER 4

4.1 Split capacitor array Digital to analog convertor:

For the realization of a fast, successive-approximation A/D converter in MOS technology, conventional voltage driven R-2R techniques are cumbersome since diffused resistors of proper sheet resistance are not available in the standard single channel technology. A complex thin-film process must be used. Furthermore, these approaches require careful control of the "ON" resistance ratios in the MOS switches over a wide range of values. In contrast to its utilization as a current switch, the MOS device, used as a charge switch, has inherently zero offset voltage and as an amplifier has very high input resistance. In addition, capacitors are easily fabricated in metal gate technology. Therefore, one is led to use capacitors rather than resistors as the precision components, and to use charge rather than current as the working medium. This technique, referred to as charge-redistribution, has been used in some discrete component A/D converters for many years.

Nevertheless better matching can be obtained by means of capacitors rather than with transistors. If a resolution of 10 bit can be easily obtained with a resistor bank, then 12 bit can be obtained with a matched capacitor bank.

Digital to analog converter is an essential building block of mixed signal systems. As with the requirement of accuracy of digital to analog converters for micro sensors wireless system is increasing, demanding of high resolution digital to analog converters. As the resolution of digital to analog converters is increasing the number of bits of the DAC is also increasing in linear fashion. But the implementation of digital to analog converter involves a MSB (Most Significant Bit) capacitor whose size increases in an exponential fashion with increasing in the number of bits there by increasing the area, power consumption and delay. To solve this problem a Novel architecture is proposed to solve the above problems.

4.2 Circuit description:

The idea is to divide the number of bits into two halves and each half is implemented with capacitor array and joins the two arrays by means of an attenuation capacitor C_{atten}.The Figure 4.0 consists of two identical 6-bits sub array binary weighted with unary attenuation capacitor.

The use of two sub arrays is to reduce the capacitor spread, and consequently the power due to the charging and discharging of capacitors during the conversion cycles. The value of unity capacitor is 50fF as per the KT/C noise limitation. This can be explained in detail as follows: the binary weighted capacitor array can be made by 2^N unity elements Figure 4.0 or by two sub-arrays with an attenuation capacitance between the arrays Figure 4.0. Typically, the two sub-arrays serve for the conversion of an equal number of elements. Therefore, for 12-bit, each sub-array uses 64 unity elements. A further segmentation of the resolution with three sub-arrays is not practical because of the difficulties in realizing the attenuating capacitors. The size of MSB capacitor in proposed architecture is 1.6pF which is very less compared to the size of actual MSB capacitor 102.4pF in original DAC. The switches for connecting the capacitors to V_{ref} and ground is implemented by means of a inverter with supply voltageV_{ref}.The figure 4.1 shows the output of digital to analog converter of 12 different number of input combinations.

The value of the unity capacitor is determined by two conditions: the kT/C noise and the matching accuracy. The sampling of the input signal over the array or the sub-arrays gives rise $\left(\frac{N}{2}+\frac{N}{2}\right)$ to a noise power equal

$$V_n^2 = \frac{kT}{2^N C_u} \qquad 4.0$$

Or

$$V_n^2 = \frac{kT}{2^{N/2} C_u} \qquad 4.1$$

The noise must be lower than the quantization noise $\Delta^2/12$. Therefore, the value of C_U must satisfy

$$C_u > \frac{12kT}{V_R^2} 2^{2N-12} \qquad 4.2$$

Remind that the binary weighted capacitive DAC is not intrinsically monotonic. The worst situation is at the midpoint of the dynamic range where the DNL caused by the random mismatch between capacitors

$$\frac{C_u}{\sqrt{C_u}} = (1 + \epsilon_c) \text{ is DNL} = \epsilon_c \, 2^{3N/4} \qquad 4.3$$

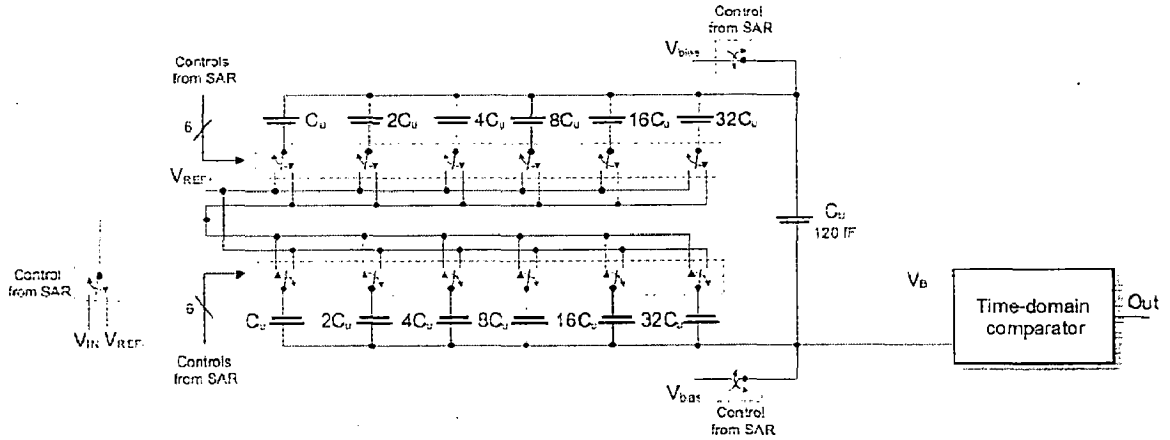

Figure 4.0: Proposed split capacitor array Digital to analog convertor.

The above equation accounts for the switching of two arrays of $32C_u$ and (31+63/64) C_u whose error is assumed $\epsilon_c \sqrt{32}$, being errors quadratic ally combined. Equation 4.3 determines the minimum area of the unity capacitance.

As known, the attenuation capacitor C_x used between the two sub-arrays of Figure 4.0.is not unity:

$$C_x = \frac{2^{N/2}}{2^{N/2}-1} C_u \qquad 4.4$$

The way used here to avoid the limit is to remove a capacitor from the LSB sub-array and to use a unity capacitor as an attenuating element. The result is shown in Figure 4.0. By inspection of the circuit, assuming and that k1 and k2 elements of the LSB and MSB sub-arrays, respectively, are connected to V_{REF}, the voltage generated by the DAC (N = 12) turns out to be equal to

$$V_{DAC} = (V_{REF-} + V_{REF-}) \frac{K_1 + 64K_2}{63.64+63} \qquad 4.5$$

The full scale ($k_1 = k_2 = 63$) is $V_R = V_{REF+} - V_{REF-}$ instead of$V_R \frac{2^N}{2^N-1}$. Equation 4.5 verifies that the error is equally distributed between the quantization intervals of the DAC and, instead of causing INL, the error leads to a 1-LSB gain error, negligible with respect to the error on the reference voltages. This result is an improvement of the technique proposed in [8].

The figure shows the output voltages of the DAC for different input combinations.

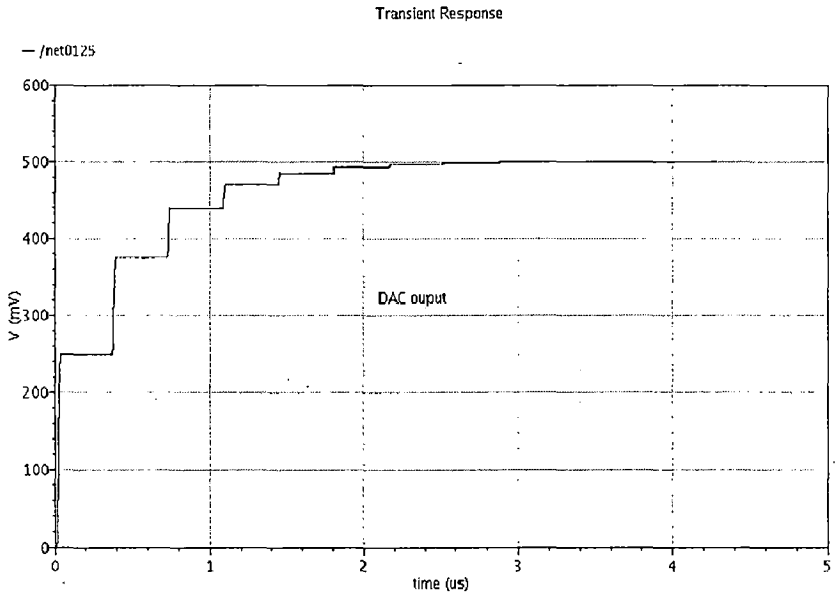

Figure 4.1: DAC output for 12 different input combinations.

CHAPTER 5

5.1 SUCCESSIVE APPROXMATION REGISTER DESIGN:

The digital logic was implemented using standard cell library gates. The architecture of the digital section is the same used in and displayed in Figure 5.0; it makes use of two shift registers to implement the successive approximation routine. The lower shift register is clocked synchronously by the fast clock and is used a sequencer, while the upper register is used to store the conversion value. When the clock signal arrives, the sequencer is reset in the 10000000000 condition. At every subsequent fast clock rising edge, the one value propagates along the sequencer, so that i clock cycles after the reset edge, it passes from the i-th position to the i+1-th. The main function performed by the SAR register is the following

1. To perform binary search algorithm.

2. Storing the comparator output.

3. Register finishing storing 12 bit and give output signal and trigger another sample signal.

4. To give input to DAC.

The SAR is built with standard CMOS logic gates. It is well known that the power consumption of such a CMOS logic circuit is approximately

$$P_D = f_{clk} V_{DD}^2 C_{ckt} \alpha(V_{in}) \qquad 5.0$$

where f_{clk} represents the clock frequency, C_{ckt} denotes the total capacitance of the circuit nodes, and α is the switching activity factor depending on the analog input. In order to save the digital power, all MOSFETs of the digital gates were designed to be as small as possible to minimize. Figure 5.0 shows the successive approximation logic.

5.2 Circuit operation:

Initially the clock signal sets the sequencer as 10000000000. The comparator output is made and the bit is stored depending upon the R signal given to the first upper register.

The R is activated if the, $V_{in} < V_{ref}$ the R is deactivated if $V_{in} > V_{ref}$ and the cycles go til the 12^{th} bit is decided. After the 12^{th} cycle the thirteenth flip flop in the sequences will activate the Output bits and the analog to digital output is done. In the fourteenth cycle the successive approximation register is reset to start the next conversion.

This architecture relies on the ring structure to achieve a low-switching activity, and therefore low active power dissipation. However, the large number of registers used increases leakage current, which is a concern at low speed. Due to the low operating voltage and frequency, power dissipation of the digital logic was assumed to be negligible at design time. Therefore, no effort was done to reduce this contribution. In fact, the power dissipation of the digital section resulted significant in final system simulations and in measurements.

Furthermore, a large fraction of this power is due to leakage, which is known to be poorly modeled and highly process dependent. This fraction of power could be lowered in several ways: first, logic could be restructured, and number of registers reduced to minimize leakage; second, custom, minimum sized logic gates could be used to decrease switching power. Finally, high-threshold devices could be employed instead of standard-Vt ones to further reduce standby power.

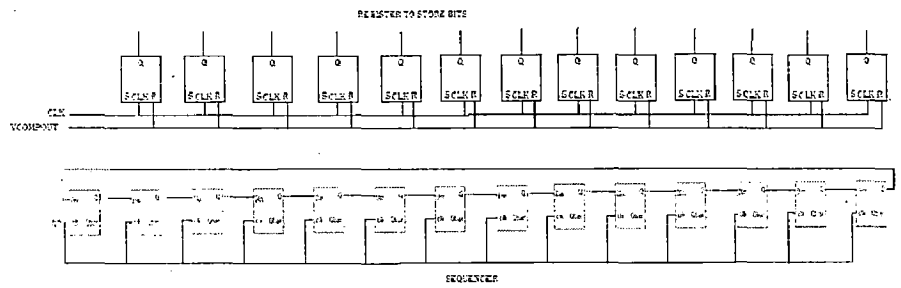

Figure 5.0: Successive approximation registers logic

5.3 Clock generating circuit for the capacitor Digital to analog converter:

The non overlapping clocks required to connect the V_{ref} and ground for the capacitor bottom plates is designed as per the requirements. We connect the capacitor bottom plates with the inverter with supply voltage equal to the V_{ref}. Then that inverter will switch the capacitor bottom plate to required voltages. For this when the capacitor bottom plate needs to be connected to the V_{ref}, we need to give the pmos input as zero, while giving the input zero to pmos device the nmos is shut off before the pmos is on to avoid the leakage or loss of data (charge) in the capacitive DAC.

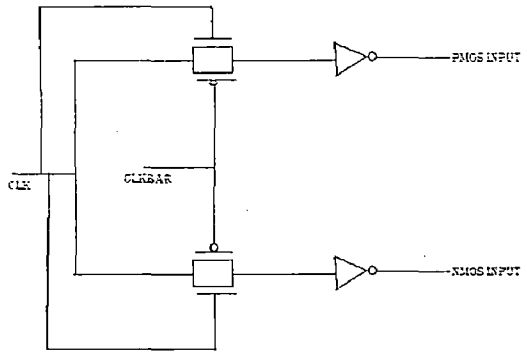

Figure 5.1: Clock generating circuit for capacitive DAC.

And while connecting the capacitive bottom plates to ground the pmos is shut off first and the nmos is turned on later to avoid the charge or loss of data. These requirements results the following waveforms for the inverter inputs.

Figure 5.2: Clock generating circuit waveforms for the capacitive DAC.

This is being implemented by the following simple circuit. The widths and lengths are adjusted to get the desired waveforms.

CHAPTER 6

6.1 Conclusion:

In summary, this work mainly focused on the design of SAR ADC targeted at low power consumption, medium resolution and moderate accuracy. The input referred offset voltage of the novel voltage to time domain comparator is $700\mu V$. The power consumption of the comparator is minimized by using a logic that shuts the comparator once the conversion is done. The resolution of the comparator is improved at the cost of the decreasing sampling frequency.

SAR ADC specifications:

Technology node	: 32nm
Sampling rate	: 100Ksps
Input signal range	: 0 -1V
Power consumption	: $5\mu W$
Supply voltage	: 1.05V

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