TCAD SIMULATION STUDY OF CRYSTALLINE SILICON SOLAR CELL AND RELIABILITY OF NANOWIRE FET

A DISSERTATION

Submitted in partial fulfillment of the
requirements for the award of the degree
of
MASTER OF TECHNOLOGY
in
ELECTRONICS AND COMMUNICATION ENGINEERING
(With Specialization in Semiconductor Devices and VLSI Technology)

By

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CANDIDATE'S DECLARATION

I hereby declare that the work, which is presented in this dissertation report, titled " **TCAD Simulation Study of Crystalline Silicon Solar Cell and Reliability of Nanowire FET** ", being submitted in partial fulfillment of the requirements for the award of the degree of **Master of Technology** with specialization in **Semiconductor Devices and VLSI Technology**, in the Department of Electronics and Computer Engineering, Indian Institute of Technology, Roorkee is an authentic record of my own work carried out from July 2009 to June 2010, under guidance and supervision of **Dr. A.K.Saxena** and **Dr. S.K.Manhas**, Department of Electronics and Computer Engineering, Indian Institute of Technology, Roorkee.

The results embodied in this dissertation have not been submitted for the award of any other Degree or Diploma.

Date: 29|06|2010

Place: Roorkee

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CERTIFICATE

This is to certify that the statement made by the candidate is correct to the best of our knowledge and belief.

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LIST OF ABBREVIATIONS

AM	Air mass
GAA	Gate All Around
EHP	Electron Hole Pairs
QE	Quantum Efficiency
TCAD	Technology Computer Aided Design
TMM	Transfer Matrix Method
IQE	Internal Quantum Efficiency
EQE	External Quantum Efficiency
OG	Optical Generation
FF	Fill Factor
ARC	Anti Reflective Coatings
SRH	Shockley Read Hall
BSF	Back Surface Field
MOSFET	Metal Oxide Semiconductor Field Effect transistor
DIBL	Drain Induced Barrier Lowering
SS	Subthreshold Slope
LDD	Lightly Doped Drain
SMU	Source Measure Unit
FN	Fowler Nordhiem
NW	NanoWire
CMOS	Complementary Metal Oxide Semiconductor

ABSTRACT

Photovoltaics' has gained importance with the failure of conventional energy resources to meet the energy requirements of various sectors. Crystalline silicon dominates the photovoltaic market today primarily due to its low cost. This work demonstrates a comprehensive study of a single junction two dimensional crystalline silicon solar cell through simulations carried out in Synopsys TCAD Sentaurus version 2007.12. Using the Transfer Matrix Method of the Sentaurus device simulator, the optical and electrical characteristics of the solar cell are simulated. Reflectance and quantum efficiency spectra, as well as dark and light current density-voltage (J-V) curves are calculated. A planar two dimensional silicon structure was used in the setup. The performance of the cell is studied considering various solar cell design parameters like cell thickness, doping of base and emitter, emitter thickness, front contact grid pattern and the design trade-offs are clearly defined.

Silicon nanowire based MOS devices are putting a strong claim as the solution to the scaling constraints on planar MOSFETS due to their strong gate electrostatic control over the channel. A study on the gate oxide reliability of these nanowires is carried out to determine the lifetime of these devices. A quantitative study supported with experimental data is shown to determine the hot carrier degradation on these nanowires.

1 INTRODUCTION

One of the largest challenges mankind will face in the twenty-first century and beyond is how to supply our increasing need for energy. With the rapid consumption rate of fossil fuels, we need to consider renewable energy sources such as photovoltaics. Photovoltaic's is a promising technology that directly takes advantage of our planet's ultimate source of power, the sun. When exposed to light, solar cells are capable of producing electricity without any harmful effect to the environment or device, which means they can generate power for many years while requiring only minimal maintenance and operational costs. Currently, the wide-spread use of photovoltaics over other energy sources is limited by the relatively high cost and low efficiency of solar cells.

The enormous gap between the potential of solar energy and our currently low conversion of it is due to low conversion efficiencies of silicon photovoltaic's, its fixed bandgap and cost of materials currently required. The cost effective raising of conversion efficiency is primarily a scientific challenge. A history of photovoltaic's goes back to 1839, when Edmund Becquerel observed a photovoltaic effect in liquid electrolytes [www.wikipedia.org]. However it was not until 1954 that the first solar cell was developed at Bell Laboratories [1]. Modern research in the area of photovoltaic technologies has lead to creation of a huge spectrum of solar cells, these are commonly classified into three generations which differ from one another based on the material and the processing technology used to fabricate the solar cells. The material used to make the solar cell determines the basic properties of the solar cell, including the typical range of efficiencies. The first generation of solar cells, also known as silicon wafer-based photovoltaic's, is the dominant technology for terrestrial applications today, accounting for more than 85 % of the solar cell market [www.solarbuzz.com].Single-crystalline and multi-crystalline wafers used in commercial production allow power conversion efficiencies up to 25 %, although the fabrication technologies at present limit them to about 15 to 20 % [2].

1.1 Objectives

This study aims to determine the performance in terms of electrical and optical characteristics of crystalline silicon solar cells operating under the Air Mass Index 1.5 (AM1.5) sun radiation. To achieve this, the cell is simulated in the Sentaurus version

2007.12 device simulator provided by Synopsys. Simulations include an electrical characterization (current-voltage curve) and an optical characterization (Transmission and Reflectance spectra). The data obtained from the simulations is used to determine performance parameters like conversion efficiencies, internal and external quantum efficiencies, fill factors, series resistance and temperature sensitivities. The choice of structure and dimensions used are meant to simplify the characterization and understanding of the cell.

In order to understand the results in detail this document presents a complete overview of the basic concepts related to solar energy and solar cell operation. Chapter 2 describes a general technical background required for solar cells and also describes the technical definitions commonly-used for solar cell characterization. Chapter 3 elaborates on the solar cell structure and the device specific setup used in the simulator. The effect of varying the various design parameters on the performance of the cell is discussed in the fourth chapter. Finally, the observations and conclusions are presented.

Chapter 7 describes how the GAA silicon nanowire structure seems to have possible novel solutions in the "more-than-moore" regime. It talks about the fabrication techniques of these nanowire FETs and discusses the current available performance of these devices by comparing critical FET parameters. A section within this chapter is devoted to the basic physics of hot carrier degradation mechanisms and the experimental setup used to assess the oxide reliability by observing the breakdown time during stress measuring.

2 FUNDAMENTAL SOLAR CELL CONCEPTS

Before reviewing the technical aspects of solar cells we take a look at solar radiation and its characteristics.

2.1 Solar Energy

Solar energy in one form or another is the source of nearly all energy on the earth. Photovoltaics' (often abbreviated as PV) is a simple and elegant method of harnessing the sun's energy. PV devices (solar cells) are unique in that they directly convert the incident solar radiation into electricity with no noise, pollution or moving parts making them robust, reliable and long lasting. Solar cells are semiconductor devices that are designed to generate electric power when exposed to electromagnetic radiation. Light may be viewed as consisting of "packets" or particles of energy, called photons. A photon is characterized by either a wavelength denoted by λ or equivalently an energy denoted by E. There is an inverse relationship between the energy of a photon (E) and the wavelength of the light (λ) given by the equation

$$E=\frac{hc}{\lambda} \tag{2.1.1}$$

where h is Planck's constant (6.626×10^{-34} Joule-s) and c is the speed of light(3×10^{8} m/s). The photon flux is defined as the number of photons per second per unit area.

$$\phi=\frac{No.of\ photons}{\sec m^2} \tag{2.1.2}$$

Since the photon flux gives the number of photons striking a surface in a given time, multiplying by the energy of the photons comprising the photon flux gives the energy striking a surface per unit time, which is equivalent to a power density. To determine the power density H in units of W/m^2, the energy of the photons must be in Joules. The equation is

$$H(\frac{W}{m^2})=\phi\frac{hc}{\lambda}(J)=q\phi\frac{1.24}{\lambda(\mu m)} \tag{2.1.3}$$

The spectral irradiance as a function of photon wavelength denoted by F is the most common way of characterizing a light source. It gives the power density at a particular wavelength. The units of spectral irradiance are in $Wm^{-2}\mu m^{-1}$. The Wm^{-2} term is the power density at the wavelength λ (μm). Hence, the m^{-2} refers to the surface area and the μm^{-1} refers to the wavelength of interest.

$$F=(\frac{W}{m^2\mu m})=q\phi\frac{1.24}{\lambda^2(\mu m)}=q\phi\frac{E^2(eV)}{1.24} \quad (2.1.4)$$

where F is the spectral irradiance in $Wm^{-2}\mu m^{-1}$,Φ is the photon flux in number of photons $m^{-2}sec^{-1}$,E and λ are the energy and wavelength of the photon in eV and μm respectively and q, h and c are constants.

The solar irradiance is the power density incident on a surface due to illumination from the sun. A comparison of solar radiation outside the Earth's atmosphere with the amount of solar radiation reaching the Earth itself is shown in Figure 2.1.1. While the solar radiation incident on the Earth's atmosphere is relatively constant, the radiation at the Earth's surface varies widely due to atmospheric effects, including absorption and scattering, local variations in the atmosphere such as water vapour, clouds, and pollution, latitude of the location and the season of the year and the time of day. For this reason, the typical distribution of light on the surface of the earth shown in Figure 2.1.1 is different than the distribution of light in space. Engineers must consider the spectrum of incident light when designing solar cells.

From Table 2.1, we see that almost 90 % of the sun's energy is concentrated in the visible and infrared part of the electromagnetic spectrum. Hence ideally we should choose a material with a cut-off wavelength close to 4 μm so that the entire spectrum is utilized. Silicon with a bandgap of 1.12 eV has a cut-off wavelength of 1.1μm and as a result is not an ideal material for solar cells. However this disadvantage is offset by its low cost of manufacturing. The Air Mass Index is the path length which light takes through the atmosphere normalized to the shortest possible path length (that is, when the sun is directly overhead).

Radiation	Range of wavelengths(μm)	% of energy carried
UV	0.15 to 0.38	7.6
Visible	0.38 to 0.72	48.4
IR	0.72 to 4	43
Other	> 4	1

Table 2.1 Division of sun's energy into various EM regions

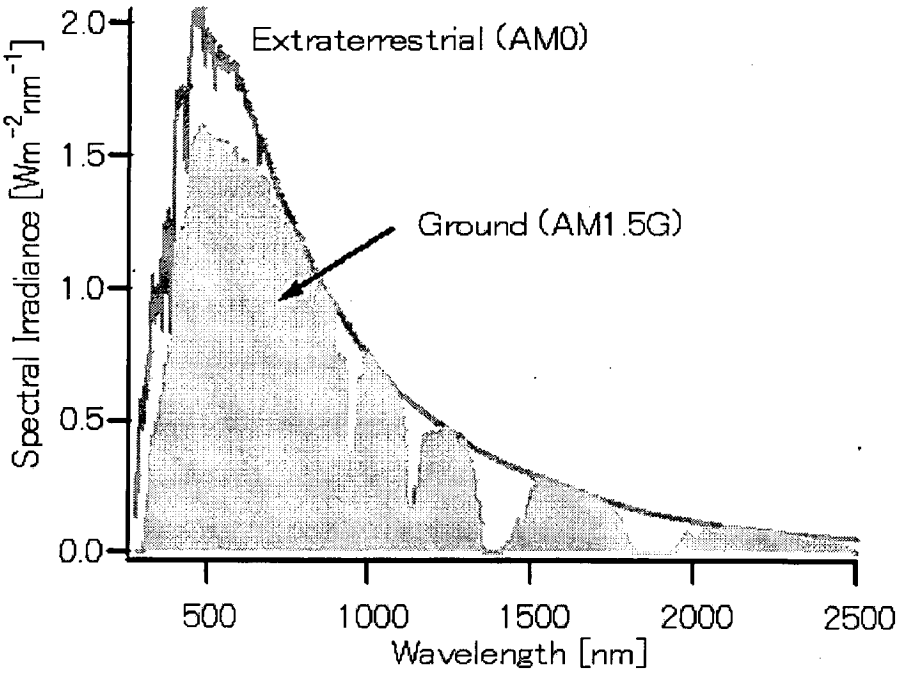


Figure 2.1.1 Spectral Irradiance of the sun [3]

The Air Mass Index quantifies the reduction in the power of light as it passes through the atmosphere and is absorbed by air and dust. The Air Mass Index is defined as

$$AM = \frac{1}{\cos\theta} \tag{2.1.5}$$

where θ is the angle shown in Fig 2.1.2.

The Air Mass Index represents the proportion of atmosphere that the light must pass through before striking the Earth relative to its overhead path length, and is equal to Y/X.

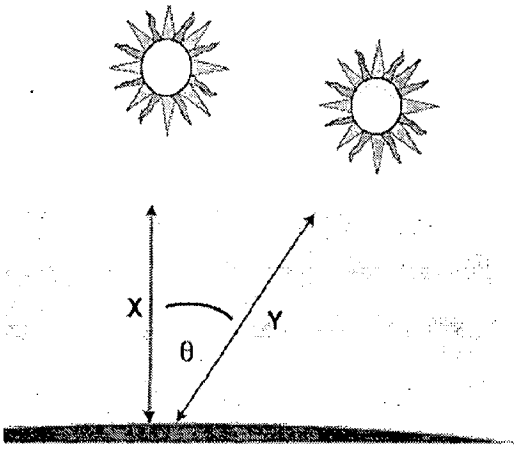


Figure 2.1.2 Path of sunlight to earth at different times [4].

The standard spectrum at the Earth's surface is called AM1.5G, (G stands for global and includes both direct and diffuse radiation). The standard AM1.5G spectrum has been normalized to give 1 kW/m^2 due to the convenience of the round number and the fact that there are inherent variations in incident solar radiation. The standard spectrum is listed in the Appendix page.

2.2 Technical Background

Before describing the technical terms commonly used for solar cell characterization, the basic operation of a single junction cell will be discussed.

2.2.1 Photovoltaic cell operation

A single-junction photocell is just a p-n junction with metallic rear and front contacts that allow electron conduction to an external load. The front contacts cover only partially the semiconductor to allow the light to enter. In Figure 2.2.1, a schematic cross-section diagram of a single-junction solar cell is displayed. Light enters the semiconductor material through the n region and generates electron-hole pairs (EHP) in the material due to the photoelectric effect.

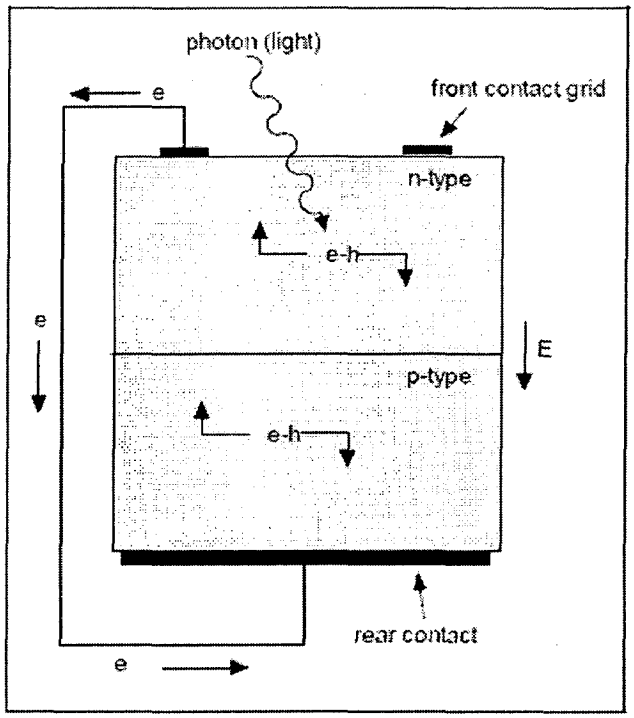


Figure 2.2.1 Schematic cross-section diagram of a single-junction solar cell [5]

In order to promote an electron into the conduction band, an incoming photon must have energy at least equal to the band gap (assuming all the electrons in the donor levels have already been thermally promoted). Therefore, photons of wavelength greater than the cut-off wavelength will make no contributions to generate electricity in the cell. However, photons with sufficient energy will promote electrons. The n region is designed to be thin while the depletion region is thick. If the EHP is generated in the depletion region, the built-in electric field drifts the electron and hole apart and they will, in the presence of an external load, produce a current through the cell. This current is called the photocurrent. If the EHP is generated in the n or p regions, the electrons and holes drift in random directions and may or may not become part of the photocurrent.

In the case when there is no load, the photons promote electrons into the conduction band on the n-type side, leaving holes in the valance band that can see the junction field and be swept across to the p-type side. Once they reach the p-type side, however, they cannot re-cross the junction; to do so would be to oppose the field. In the p-type material too, electrons become promoted to the conduction band and roll easily down the "hill" into the n-type side, but once they are there, they cannot re-climb the hill. This is analogous to an increase of the thermal current.

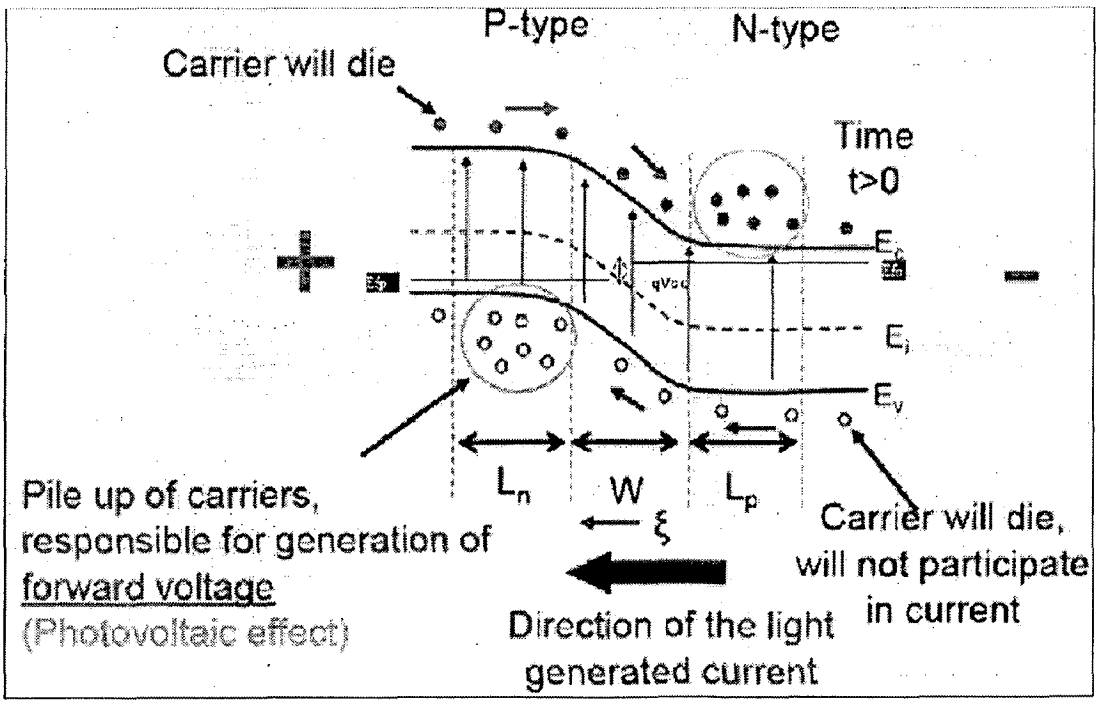


Figure 2.2.2 band diagram of a solar cell under illumination

Separation of charge begins to build up, because an excess of electrons become trapped on the n-type side while an excess of holes are trapped on the p-type side. This separation of charge contributes a voltage between the two contacts. This phenomenon is called the photovoltaic effect. The build up of carriers and the band positions are shown in figure 2.2.2. This newly created field competes with and eventually overcomes the junction field and forms a forward biased junction. If this continues, the forward bias will not last. However, the net current must be zero so the recombination current must somehow compensate. The sum of the total junction current and the newly created photocurrent must be zero, so that,

$$I_J = | I_P | = I_S(e^{\frac{qV_{oc}}{kT}} - 1) \qquad (2.2.1)$$

where I_P flows from the n-type side to the p-type side, while I_J flows from the p-type material to the n-type material. In the above equation, the potential V_{oc} is the potential difference set up by the photocurrent. It is the voltage created by the photons, and is called the open circuit voltage. Physically, the majority carriers cross the junction until a situation has been reached in which the difference in potential between the p-type side and the n-type side has "unbent" the bands exactly. In such a situation, the system reaches equilibrium. Then the open circuit voltage must be exactly equal to the contact potential in the junction. Experimentally, this is exactly the case. The open circuit voltage of silicon photovoltaic cells is between 0.5 V and 0.7 V, which is the range of "turn-on potential" in silicon diodes. From this realization, the current equation (2.2.1) can be solved to find the open circuit voltage.

If the junction is uniformly illuminated by photons with energy greater than E_g an added generation rate g_{op} (EHP/cm^{-3}- s) participates in the diode current. The number of holes created per second within a diffusion length on the n side is $AL_p g_{op}$. Similarly $AL_n g_{op}$ electrons are generated per second within L_n and AWg_{op} carriers are generated within W. The resulting current due to collection of these optically generated carriers by the junction is

$$I_p = qAg_{op}(L_p + L_n + W)$$

The thermally generated current adds to the photocurrent and the diode current equation now becomes

$$I_J = I_S(e^{\frac{qV_{oc}}{kT}} - 1) - I_p$$

$$I_j = qA(\frac{L_P}{\tau_P} p_n + \frac{L_n}{\tau_n} n_p)(e^{\frac{qV}{kT}} - 1) - (qAg_{op}(L_n + L_p + W)) \qquad (2.2.2)$$

Thus the I-V curve is lowered by an amount proportional to the generation rate as seen in figure 2.2.3. For higher generation rates the graph moves further in the fourth quadrant, signifying an increase in the photocurrent obtained from the cell.

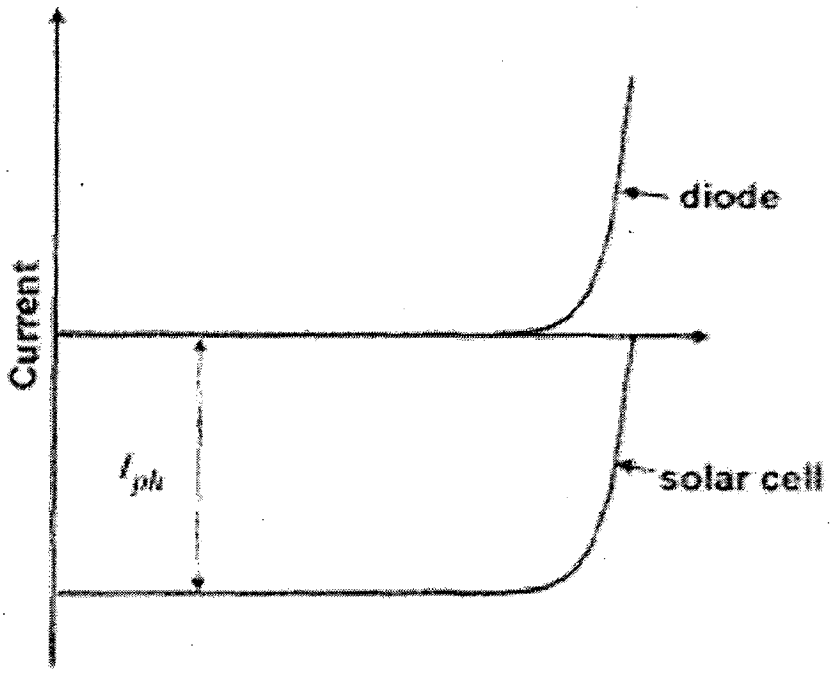


Figure 2.2.3 I-V characteristics of an illuminated junction [5].

When there is an open circuit across the device I_j is zero and the voltage is obtained by setting the current as zero in equation 2.2.2.

$$V_{OC} = \frac{kT}{q}(\ln(\frac{I_P}{I_S} + 1)). \qquad (2.2.3)$$

The condition V= 0 gives the following expression for I_p

$$I_P = -q A g_{op} (L_n + L_p + W)$$

Thus, it is a combination of the photoelectric and photovoltaic effects that produces current and voltage from the cell needed to generate power. The photocurrent is negative with respect to the junction current and hence the net power is negative, which translates to generation of power.

2.2.2 Definitions for characterization of photovoltaic devices

The following photovoltaic definitions are extensively used in this document. These are the basic concepts required to understand and characterize the performance of solar cells. As shown in figure 2.2.3 the solar cell I-V shifts down with illumination. Higher the optical generation, greater is the shift in magnitude. As a result, in the fourth quadrant we have positive voltage and negative current meaning a net gain in power. For ease in understanding we shift the characteristics to the 1st quadrant by reversing the current and identify the various points on a photovoltaic device I-V curve.

Current-Voltage curves (I-V): On an I-V plot, the ordinate refers to current, and the abscissa to voltage. This curve passes through two significant points, the *short-circuit current* (I_{sc}) and the *open-circuit voltage* (V_{oc}) as seen in Figure 2.2.4. The I_{sc} refers to the current when the output terminals of the cell are short-circuited. In the plot, this point is the intercept of the curve with vertical axis. The V_{oc} is the voltage measured at open circuit conditions and is represented as the intercept of the curve with the horizontal axis in the plot.

Maximum Power point: The Maximum Power (P_{mp}) point occurs when the product of the current and voltage is maximum. The current and voltage at the maximum power point are denoted by I_{mp} and V_{mp}, respectively. This is the point that encloses the most amount of area in the fourth quadrant when vertical and horizontal lines are drawn from the point. The power point is shown in Figure 2.2.4.

Fill factor, FF: A percentage given by Equation (2.2.3) that describes how close the I-V curve of a solar cell resembles a perfect rectangle, which represents the ideal solar cell.

$$Fill\ Factor\ (FF) = \frac{I_{mp} V_{mp}}{I_{sc} V_{sc}} [\%] \qquad (2.2.4)$$

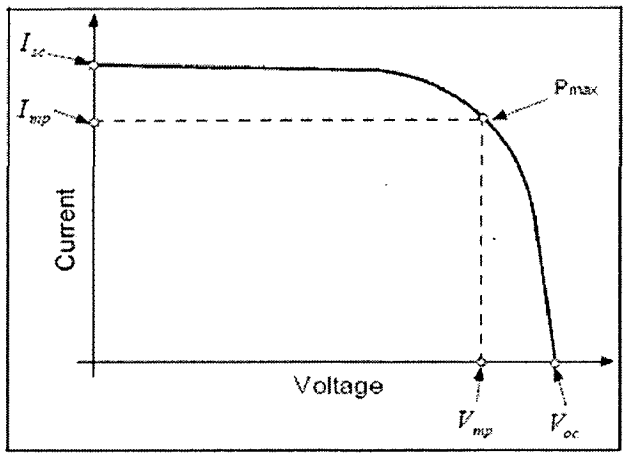


Figure 2.2.4 Current versus Voltage curve (I-V) for a typical solar cell [6].

Quantum efficiency: Quantum efficiency (QE) is the ratio of the number of charge carriers collected by the solar cell to the number of photons of a given energy incident on the PV device. QE therefore is related to the response of a solar cell to the various wavelengths in the spectrum of incident light on the cell. The QE is given as a function of either wavelength or energy.

Conversion efficiency: The conversion efficiency of a solar cell is the percentage of the total incident solar energy on a photovoltaic device that is converted into electrical energy. This relation is given by

$$Conversion\ Efficiency = \frac{P_{mp}}{Incident\ Solar\ Energy}[\%] \qquad (2.2.5)$$

3 GENERAL SIMULATION SETUP

In the past decade, the capabilities of optoelectronic device simulation have advanced tremendously. Faster and more powerful computers enable the numeric simulation of microscopic physical phenomena to investigate and optimize complex state of- the-art optoelectronic devices. Currently, Technology Computer Aided Design (TCAD) is widely used for the development and optimization of new generations of silicon devices. As a powerful, general, semiconductor processing and device simulation suite, TCAD Sentaurus can simulate various optoelectronic devices. A comprehensive set of carrier transport models, combined with an extensive set of optical models implemented in Sentaurus Device, addresses the needs of the optoelectronic community to simulate various devices. In this work we have used TCAD Sentaurus to perform a 2D device simulation of a solar cell. The simulation is organized as a Sentaurus Work Bench (SWB) project. The tool flow of the project is discussed here. It consists of Sentaurus Structure Editor which creates the solar cell structure, Sentaurus Device which calculates the optical device characteristics and the visualization tool Inspect.

3.1 Device Structure in Sentaurus Structure Editor:

Sentaurus Structure Editor defines the two-dimensional solar cell made of silicon. The structure is made of a n-type layer on a p-type silicon substrate, an antireflective coating of silicon nitride, and silver metal contacts. The geometric parameters of the solar cell are defined by setting the following global SWB parameters (The 3rd dimension is assumed to be 1 μm.)

- *dfront*, top contact depth, 1 μm
- *wfront*, top contact width, 5μm
- *wback*, bottom contact width, 600 μm
- *wtot*, the total width of the structure, 600 μm
- *darcfront*, depth of the antireflective film on top of the structure, 0.075 μm
- *dsub*, thickness of the cell, 15μm

The solar cell structure is created with analytic doping profiles for the p and n regions and appropriate mesh refinements are added.

After the structure is created, the generated mesh and doping information is stored in a file, which is then passed to Sentaurus Device. The solar cell device obtained with Sentaurus Structure Editor is shown in Figure 3.1.1. From the structure, we observe that the junction is formed at a depth of 0.48 μm from the top of the device. The n-type doping near the top surface is gaussian with peak concentration of $6e^{19}cm^{-3}$ and the p-type doping near the back surface is also gaussian with peak concentration of $1e^{19}cm^{-3}$. The substrate is a p-type silicon substrate with constant doping of $2e^{16}$ cm^{-3}. N-type silicon has a better surface quality than p-type, so it is placed at the front of the cell where most of the light is absorbed. A large fraction of the light is absorbed close to the surface, hence by making the front layer very thin; most of the carriers generated by the incoming light are created within a diffusion length of the p-n junction.

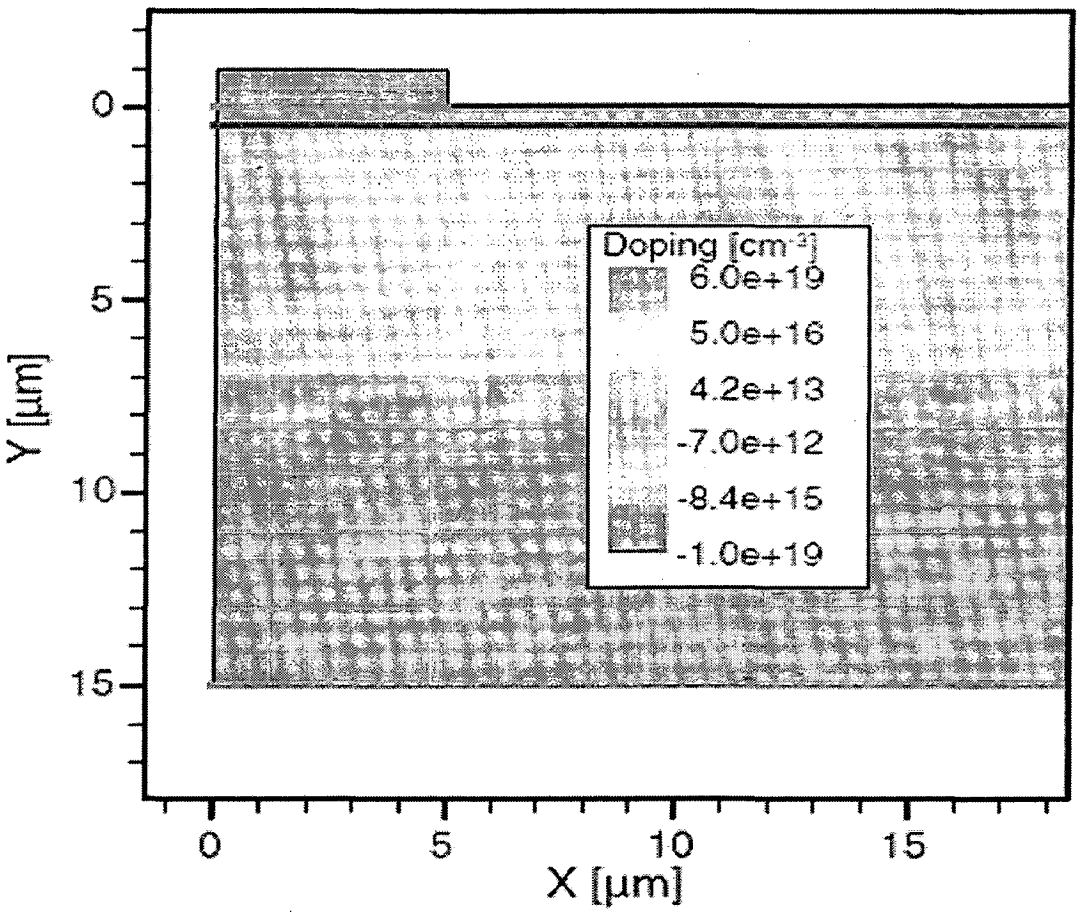


Figure3.1.1 Part of the solar cell generated by the Sentaurus Structure Editor

3.2 Device Simulation using Sentaurus Device:

After the structure is created, the generated mesh and doping information is passed to Sentaurus Device. Figure 3.2.1 shows the flow of input and output files in Sentaurus Device. The input files consist of the structure, doping and meshing files passed from Sentaurus Structure Editor. The other input files are the parameter files for

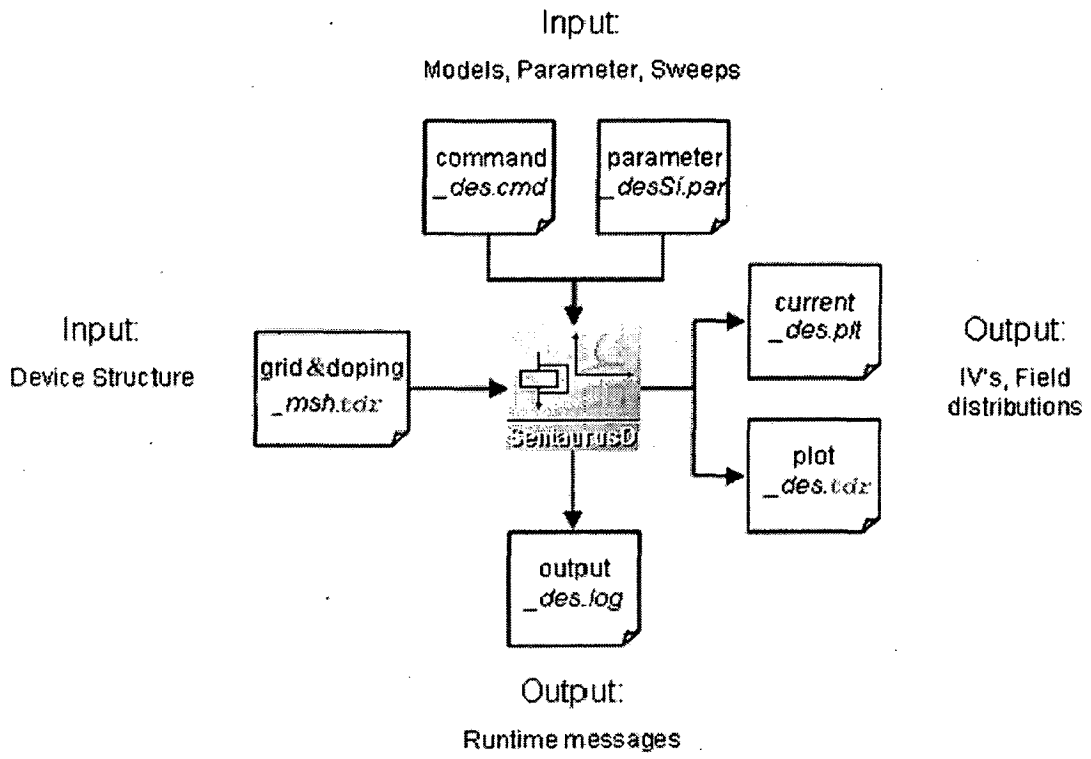


Figure 3.2.1 Flow of input and output files in Sentaurus Device

silicon and silicon nitride. To analyze the performance of solar cells, numerical simulation of the device is done by solving the three governing semiconductor equations, Poisons equations and the electron and hole continuity equations, together with the drift-diffusion model. In simulation, the impurity scattering and carrier-carrier scattering were also considered. The band to band Auger recombination model was included and Shockley-Read-Hall recombination was also modeled. Sentaurus Device calculates the optical generation rate in the solar cell and couples it with the electrical simulation. In this setup, the rate of optical carrier generation for different wavelengths of the incident radiation is calculated using the Transfer Matrix Method (TMM) [7], which is subsequently used in Inspect to calculate the photo generated current. The incident light spectrum i.e. the sunlight AM1.5 spectrum is given as input

in an external file. Three types of calculation are performed in this step, the illuminated I-V, dark I-V and the reflectance and transmittance spectra. The reflectance/transmittance spectra are calculated for a discrete set of wavelengths controlled by the following SWB parameters:

- *wstart* [nm]: Set to 300.
- *wend* [nm]: Set to 1100.
- *wsteps*: Set to 12.

These parameters correspond to the initial wavelength, final wavelength, and the number of steps between the initial and final wavelengths used to calculate the spectra, respectively. The range of wavelengths is set from 0.38 to 1.1 μm which is the range to which silicon responds. The light intensity is defined by the parameter:

- *intensity* [W m–2]: Set to 1000.

The number of electron hole pairs generated per photon is normalized to 1. The incident light spectrum i.e. the sunlight AM1.5 spectrum is given as input in an external file. Figure 3.2.2 demonstrates the I–V and power curves of the illuminated diode. The photocurrent is opposite to the dark current of the forward-biased diode. For low applied voltage, the photocurrent is independent of the voltage and dominates the I–V curve of the illuminated device. In this regime, the solar cell power grows linearly. When the voltage is increased after the maximum power point is reached, the contribution of the photocurrent to the total current through the diode becomes less important, and the total current changes sign.

The maximum current density and maximum power density are extracted and have the following values, respectively, $6.932e^{-8}$ A/μm and $3.664e^{-8}$ W/μm. The value for V_{oc} is 0.634 V. The maximum power point is found out to be (0.548 V, $6.68e^{-8}$A/μm). The fill factor is then calculated from equation (2.2.3) to be 83.3 %.

For the dark characteristics, the optical generation model is not activated and the diode I-V curve is obtained with the same voltage ramping as for the case of illumination. From the dark current plot in Figure 3.2.3, we can see a characteristic I–V curve of a forward-biased diode in this plot.

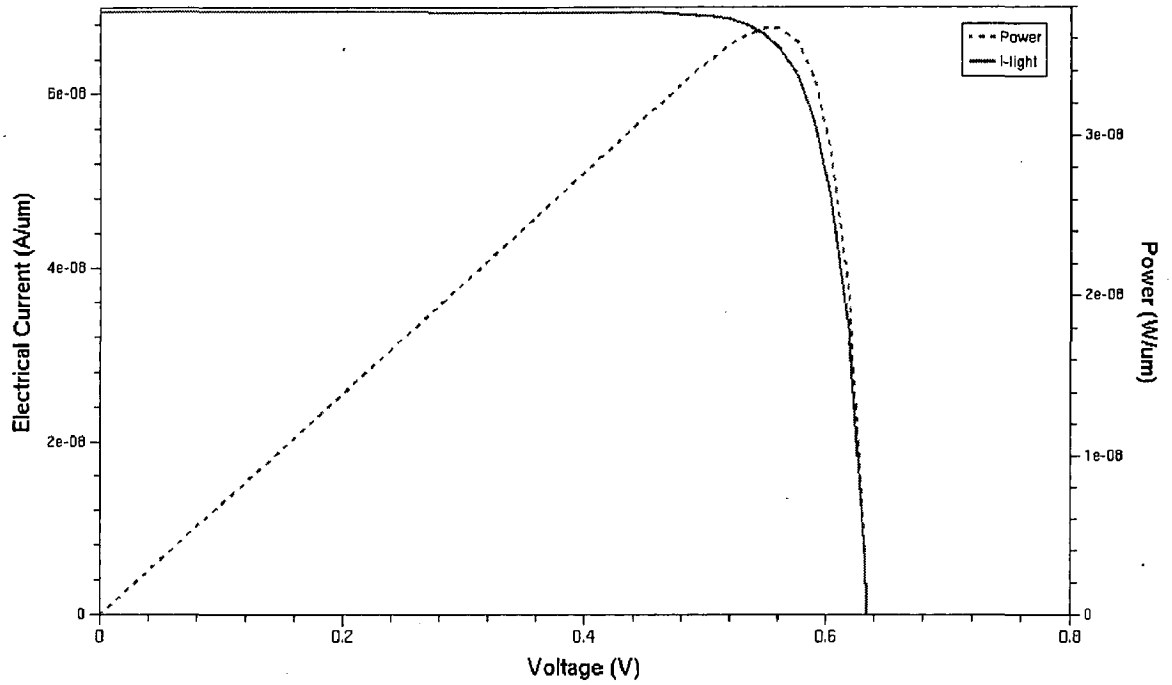


Figure 3.2.2 Current and power versus voltage for the illuminated device.

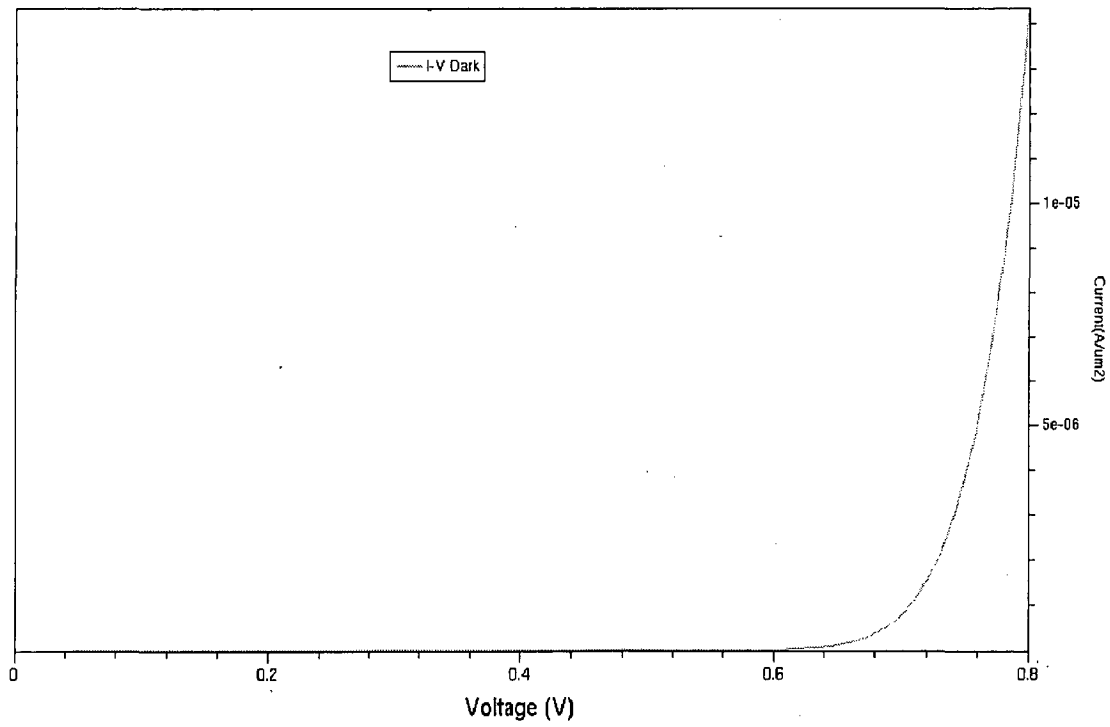


Figure 3.2.3 I-V curve of the diode without illumination.

3.3 Device Reflectance and Transmittance Calculation in INSPECT:

To obtain the reflectance/transmittance and quantum efficiency spectra, the wavelength is ramped. At higher wavelengths, interference effects lead to fast oscillations in the optical and electrical characteristics. The transmittance and reflectance coefficients of the cell are also stored in the plot file and are presented in Figure 3.3.1 and Figure 3.3.2 respectively. These coefficients are calculated using the depths of the material layers and the complex refractive coefficients as set in the parameter file given as input. For the structure under consideration, the optical radiation is not transmitted for wavelengths below 600 nm. Above this wavelength, transmission grows and multiple reflections become important. Consequently, an occurrence of interference is visible in the fast oscillations of the reflectance/transmittance spectra. The reflectance and transmittance spectra have been normalized by the total incident light hence its maximum value is 1and minimum 0.

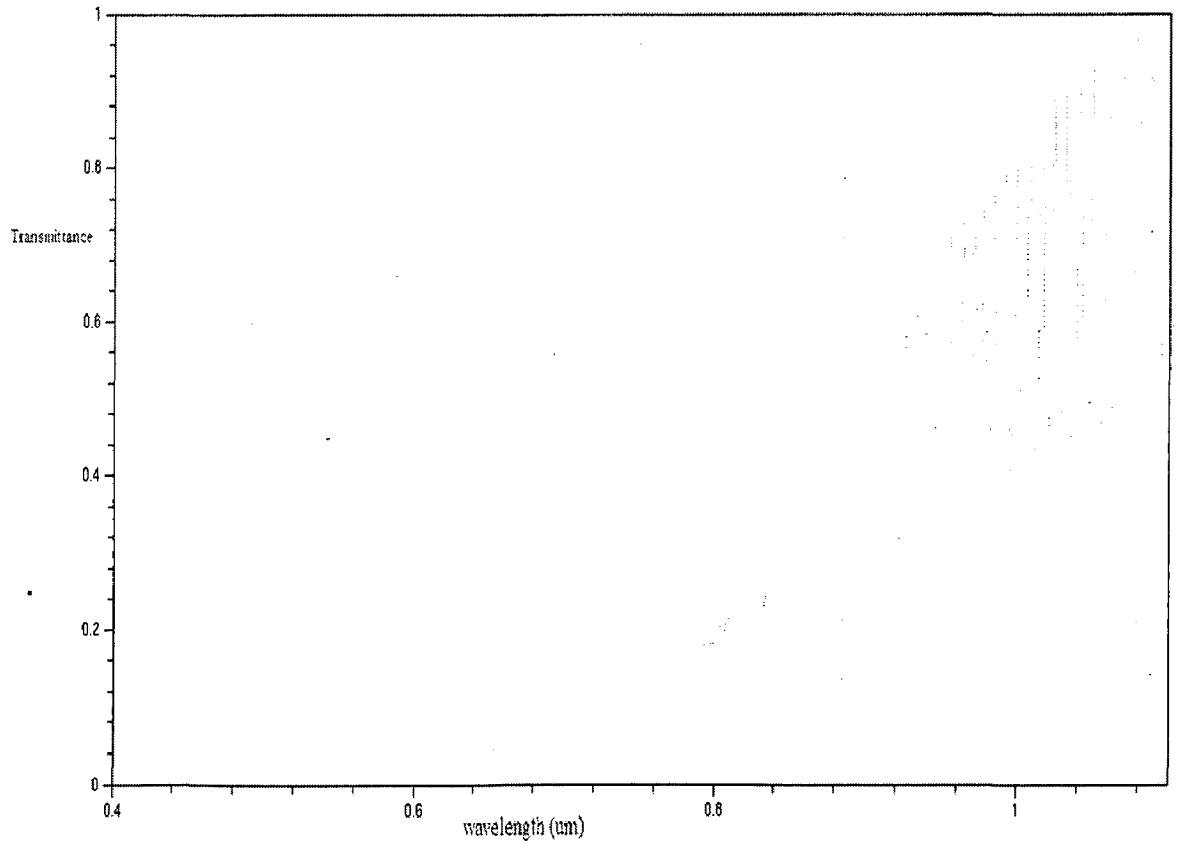


Figure 3.3.1 Transmittance spectra versus wavelength

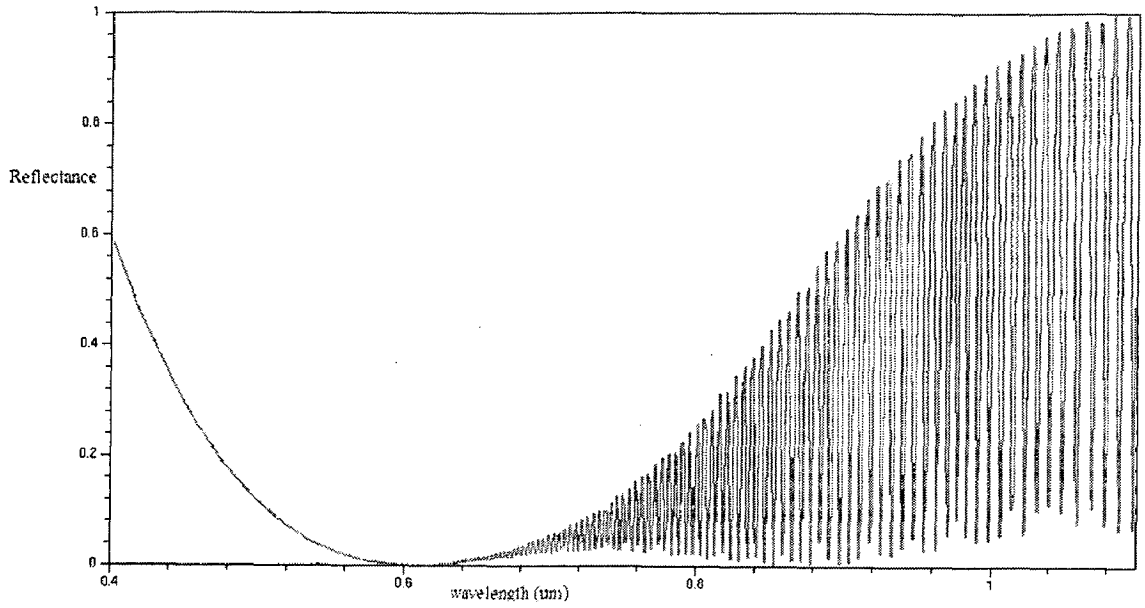


Figure 3.3.2 Reflectance spectra versus wavelength.

The number of carriers optically generated within the silicon substrate is shown in Figure 3.3.3. It is evident that high energy blue photons create more number of EHPs than low energy red photons. Beyond 1.1 μm the carrier generation is almost zero because the photon energy is less than the bandgap of silicon. Near 0.4 μm the optical absorption coefficient is very large which means that the absorption depth is very small (Refer Appendix for optical properties of silicon). Due to very small absorption depth, all of the generated carriers are lost in surface recombination at the Si/SiO_2 interface. Hence the UV part of the electromagnetic spectrum does not generate many EHPs in the substrate.

The internal quantum efficiency (IQE) is defined as the ratio of the number of carriers contributing to the electrical current to the total number of photogenerated carriers. The latter can be found through the carrier generation rate integrated over the substrate volume. The IQE is given as [5]

$$IQE=\frac{I}{Gq} \tag{3.3.1}$$

where I is the electrical current, q is the charge, and G is the optical generation rate. The external quantum efficiency (EQE) is defined as the ratio of the number of electrons in the current to the number of incident photons. The EQE is given as [5]

$$EQE = \frac{Ihc}{q\lambda I_o S} \tag{3.3.2}$$

where h is Plank's constant, c is the speed of light, λ is the wavelength, Io is the incident light intensity, and S is the incidence surface area.

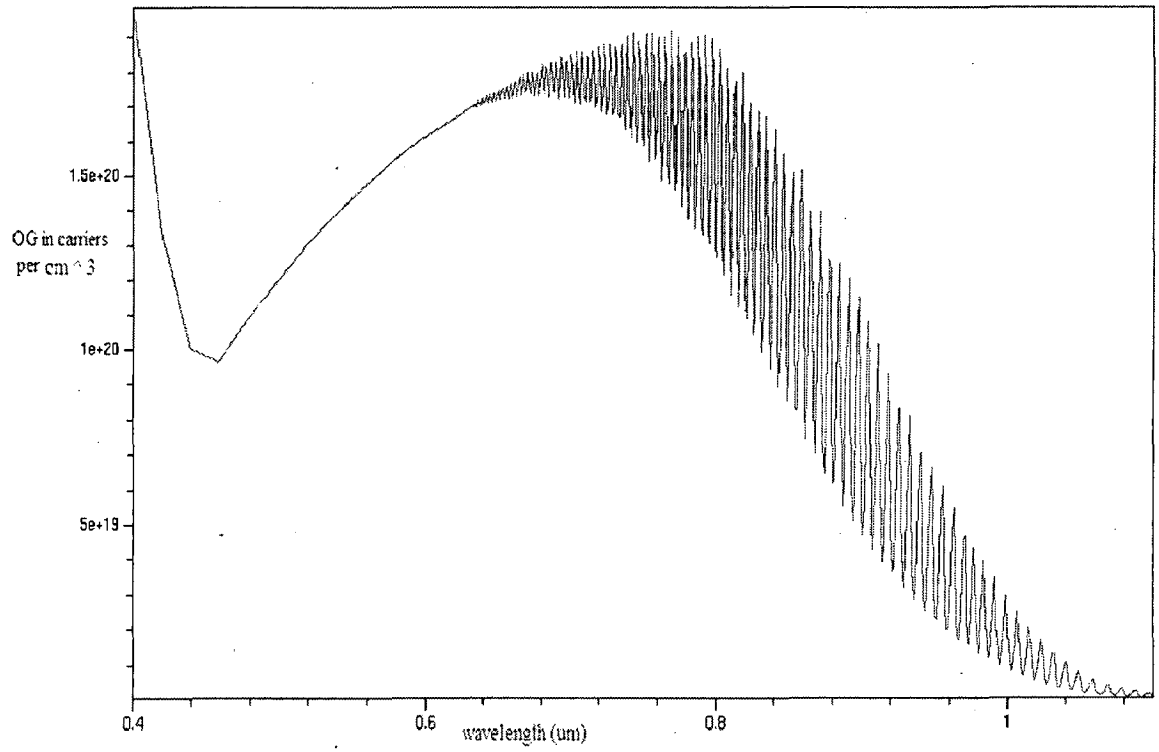


Figure 3.3.3 Optical Generation versus wavelength

Figure 3.3.4 shows a plot of the Internal and External quantum efficiencies versus wavelength. The efficiencies are defined as a percentage and hence have a range from 0 to 1. As one can see, the quantum efficiencies initially grow with the wavelength. Comparing this to the reflectivity and transmittivity graphs, it is seen that this regime corresponds to the decreasing reflection and increasing absorption. As the wavelength increases, more radiation is transmitted through the structure or reflected from the surface. Consequently, less of the incident light is absorbed and the EQE decreases to almost zero at higher wavelengths. The optically created carriers are still effective in contributing to the electrical current as follows from the IQE curve that stays above 80 %.

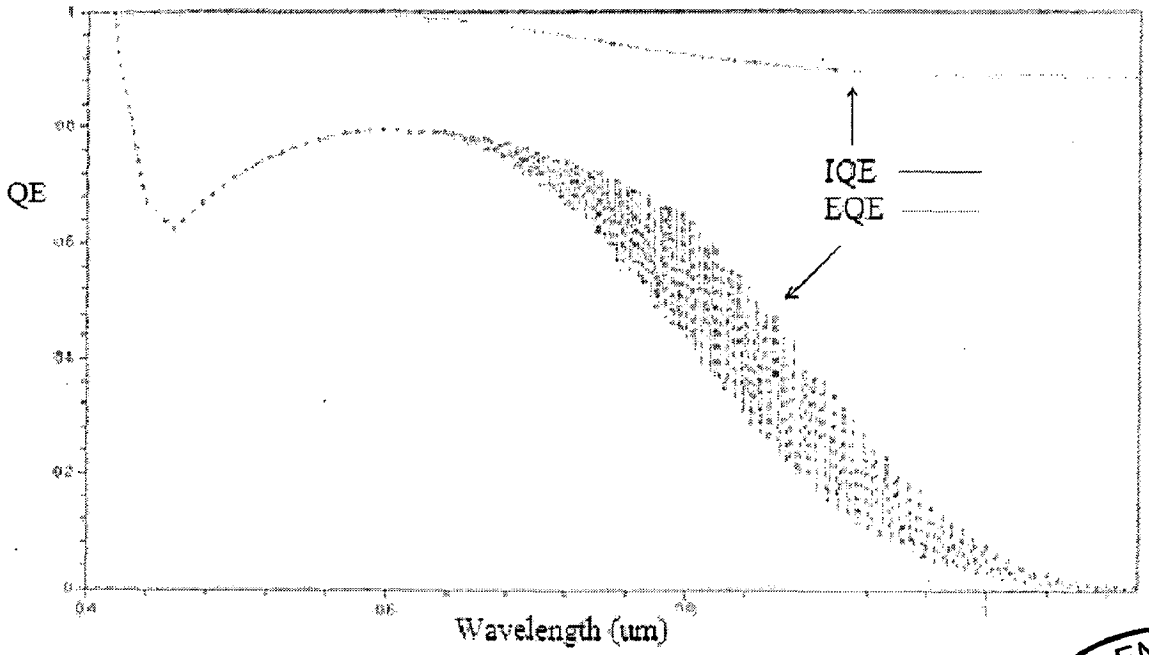


Figure 3.3.4 Internal and External Quantum Efficiencies versus wavelength

3.4 Comparison of Simulated and Quantitative Results

The cell current and open circuit voltage values are quantitative calculated using equation 2.2.2. The calculations are done in MatLab and the tabulated results are shown below. The simulated values are obtained from the graphs discussed earlier. The current, voltage and power have units Ampere, Volt and Watt respectively.

	Simulated						Calculated	
Wavelength(um)	OG	IQE	Isc	Voc	Pmax	Cellcurrent	CellCurrent	Voc
0.3	1.24E+18	0.988	1.80E-11	0.418	5.89E-12	5.41E-09	3.58E-06	0.527
0.35	1.06E+18	0.988	7.97E-09	0.576	3.78E-09	2.39E-06	3.06E-06	0.523
0.4	1.95E+17	0.988	2.83E-09	0.549	1.27E-09	8.48E-07	5.64E-07	0.479
0.5	1.19E+17	0.944	2.64E-09	0.547	1.18E-09	3.53E-07	3.44E-07	0.466
0.6	1.59E+17	0.991	3.27E-09	0.553	1.48E-09	9.80E-07	4.59E-07	0.474
0.7	1.79E+17	0.963	3.03E-09	0.551	1.37E-09	9.10E-07	5.17E-07	0.477
0.8	1.22E+17	0.992	1.76E-09	0.537	7.71E-10	5.28E-07	3.53E-07	0.467
0.9	4.98E+16	0.896	5.05E-10	0.504	2.06E-10	1.52E-07	1.44E-07	0.444
1	1.72E+16	0.886	1.63E-10	0.476	6.19E-11	4.90E-08	5.00E-08	0.416
1.1	7.41E+14	0.884	3.90E-12	0.379	1.13E-12	1.17E-09	2.00E-09	0.334
1.2	1.01E+13	0.885	5.49E-14	0.269	1.04E-14	1.65E-11	6.30E-12	0.182

Table 3.4.1 Comparison of simulated and calculated results

The difference in cell current and open circuit values as compared with the simulated values is due to the fact that that equation 2.2.2 assumes constant doping profile across the junction while the simulator has a gaussian doping profile for the emitter.

4 DESIGN OF SOLAR CELLS & RESULTS

Solar cell design involves specifying the parameters of a solar cell structure in order to maximize efficiency, given a certain set of constraints. These constraints will be defined by the working environment in which solar cells are produced. For example, in a commercial environment where the objective is to produce a competitively priced solar cell, the cost of fabricating a particular solar cell structure must be taken into consideration. However, in a research environment where the objective is to produce a highly efficient laboratory-type cell, maximizing efficiency rather than cost is the main consideration.

The theoretical efficiency for photovoltaic conversion is in excess of 86.8 % [9]. However, the 86.8 % figure uses detailed balance calculations and does not describe device implementation. For silicon solar cells, a more realistic efficiency under one sun operation is about 29 % [10]. The maximum efficiency measured for a silicon solar cell is currently 24.7 % under AM1.5G. The difference between the high theoretical efficiencies and the efficiencies measured from terrestrial solar cells is due mainly to two factors. The first is that the theoretical maximum efficiency predictions assume that energy from each photon is optimally used, that there are no unabsorbed photons and that each photon is absorbed in a material which has a band gap equal to the photon energy. This is achieved in theory by modeling an infinite stack of solar cells of different band gap materials, each absorbing only the photons which correspond exactly to its band gap. The second factor is that the high theoretical efficiency predictions assume a high concentration ratio. Assuming that temperature and resistive effects do not dominate in a concentrator solar cell, increasing the light intensity proportionally increases the short-circuit current. Since the open-circuit voltage (V_{oc}) also depends on the short circuit current, V_{oc} increases logarithmically with light level. Furthermore, since the maximum fill factor (FF) increases with V_{oc}, the maximum possible FF also increases with concentration. The V_{oc} and FF increase with concentration, which allows concentrators to achieve higher efficiencies. This advantage of concentrator photovoltaics' has led to its wide use.

In designing such single junction solar cells, the principles for maximizing cell efficiency are:

- increasing the amount of light collected by the cell that is turned into carriers;
- increasing the collection of light-generated carriers by the *p-n* junction;

- minimising the forward bias dark current;
- extracting the current from the cell without resistive losses.

4.1 Optical Losses

Optical losses chiefly effect the power from a solar cell by lowering the short-circuit current. Optical losses consist of light which could have generated an electron-hole pair, but does not, because the light is reflected from the front surface or because it is not absorbed in the solar cell. For the most common semiconductor solar cells, the entire visible spectrum has enough energy to create electron-hole pairs and, therefore, all visible light would ideally be absorbed.

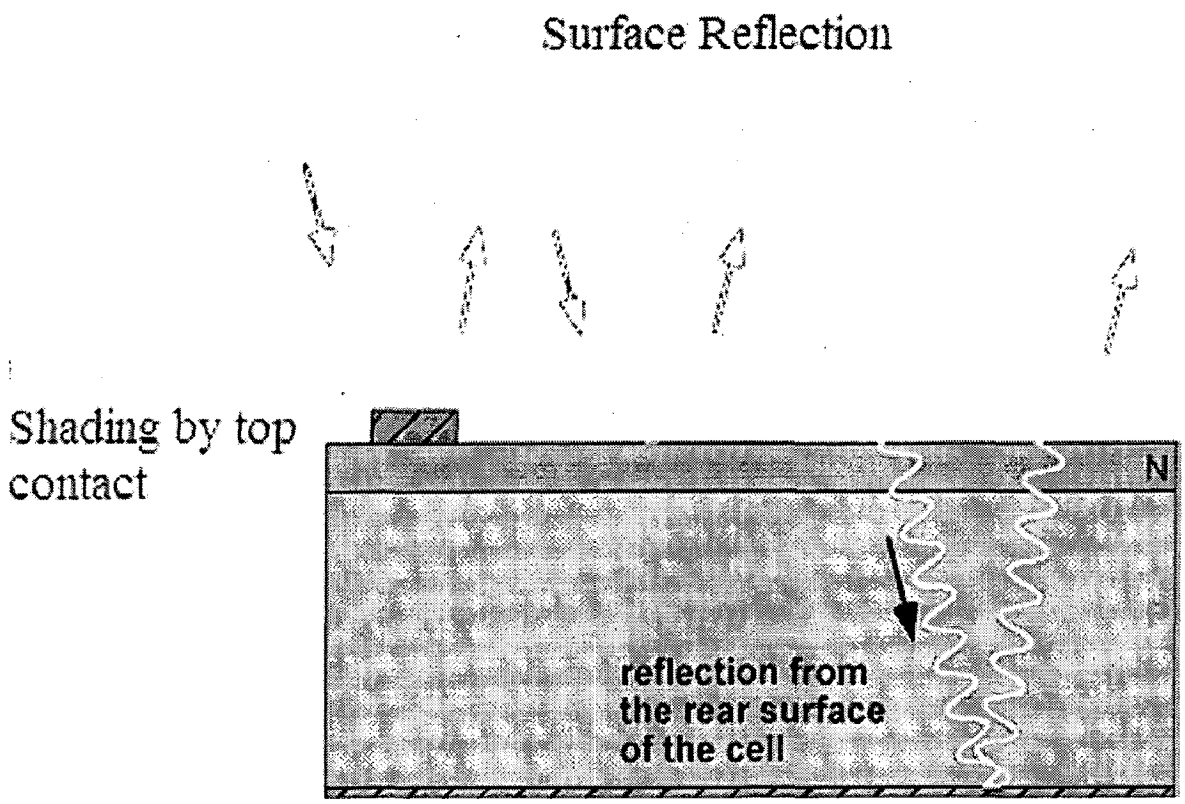


Figure 4.1.1 Sources of optical loss in a solar cell.

There are a number of ways to reduce the optical losses:

- Top contact coverage of the cell surface can be minimised (although this may result in increased series resistance).
- Anti-reflection coatings can be used on the top surface of the cell.
- Reflection can be reduced by surface texturing.

- The solar cell can be made thicker to increase absorption (although any light which is absorbed more than a diffusion length away from the junction will not typically contribute to short-circuit current since the carriers recombine).
- The optical path length in the solar cell may be increased by a combination of surface texturing and light trapping.

4.2 Anti-Reflection Coatings

Anti-reflection coatings on solar cells are similar to those used on other optical equipment such as camera lenses. They consist of a thin layer of dielectric material, with a specially chosen thickness so that interference effects in the coating cause the wave reflected from the anti-reflection coating top surface to be out of phase with the wave reflected from the semiconductor surfaces. These out-of-phase reflected waves destructively interfere with one another, resulting in zero net reflected energy. The thickness of the anti-reflection coating is chosen so that the wavelength in the dielectric material is one quarter the wavelength of the incoming wave. For a quarter wavelength anti-reflection coating of a transparent material with a refractive index n_1 and light incident on the coating with a free-space wavelength λ_0, the thickness d_1 which causes minimum reflection is calculated by[5]

$$d_1 = \frac{\lambda_0}{4n_1}$$

Reflection is further minimised if the refractive index of the anti-reflection coating is the geometric mean of that of the materials on either side; that is, glass or air and the semiconductor. Referring to Figure 4.2.1 the refractive index is expressed by[5]

$$n_1 = \sqrt{n_0 n_2}$$

Figure 4.2.3 shows how the reflectivity varies with changing ARC thickness. As we increase the ARC thickness from 0.05 to 0.125 μm, the zero reflectivity wavelength increases from 0.4 to 0.8 μm. The ARC thickness with 0.0625 μm gives zero reflectance around 0.6 μm wavelength and is generally preferred as the ARC thickness as it maximizes the cell output.

Figure 4.2.2 shows a comparison of surface reflection from a silicon solar cell, with and without a typical anti-reflection coating. For simplicity, this simulation assumes a constant refractive index for silicon at 3.5. In reality, the refractive index of silicon and the coating is a function of wavelength.

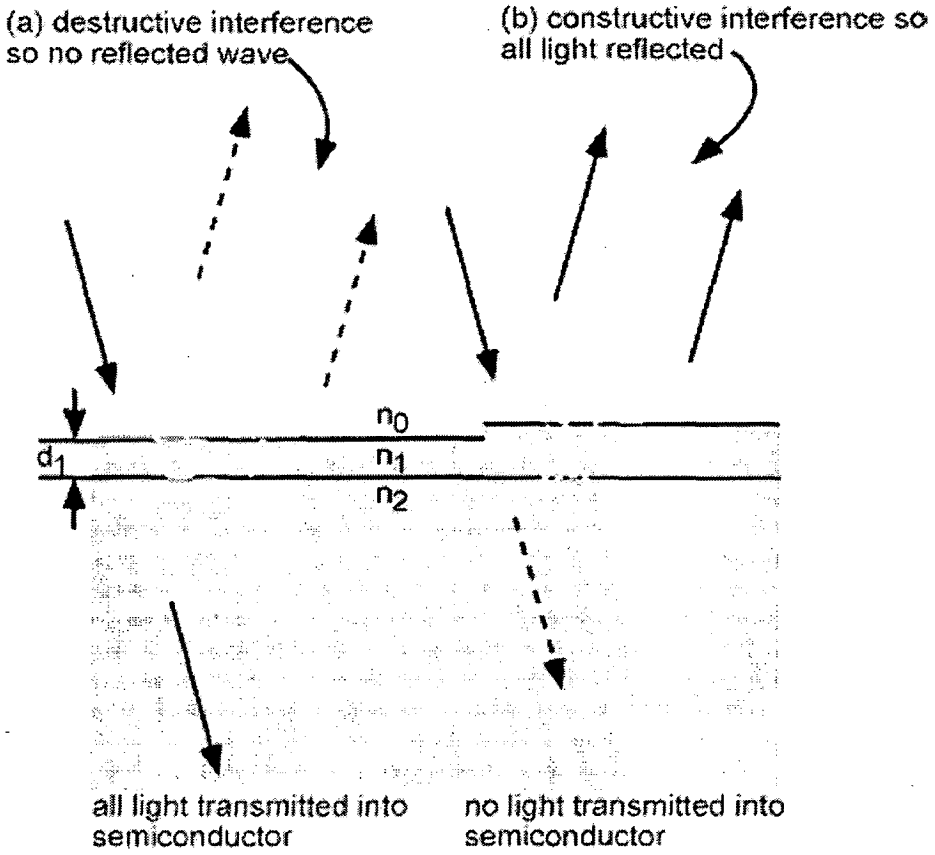


Figure 4.2.1 Use of a quarter wavelength anti-reflection coating to counter surface reflection [4].

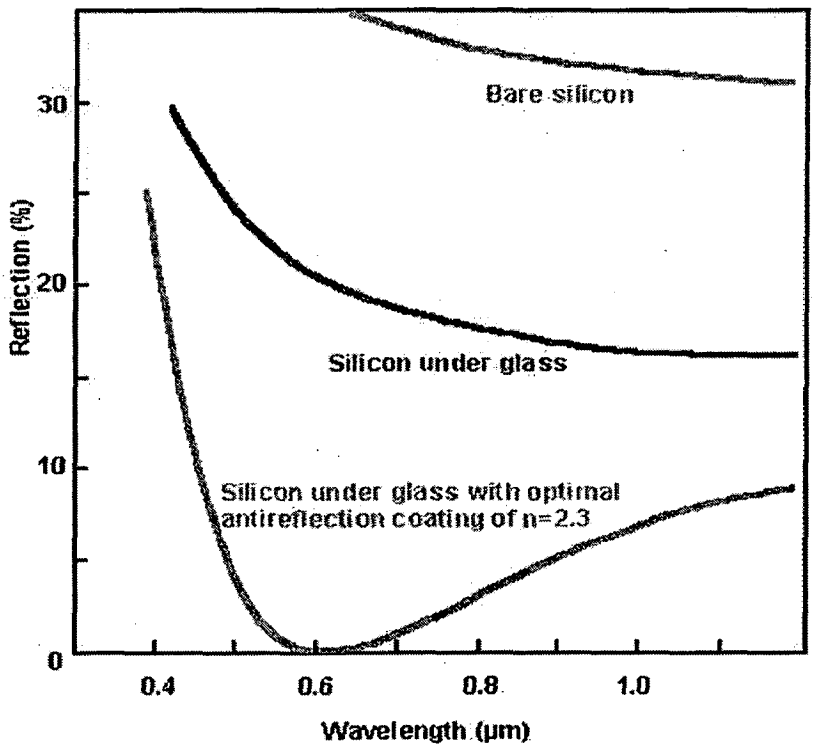


Figure 4.2.2 Effect of ARC [11]

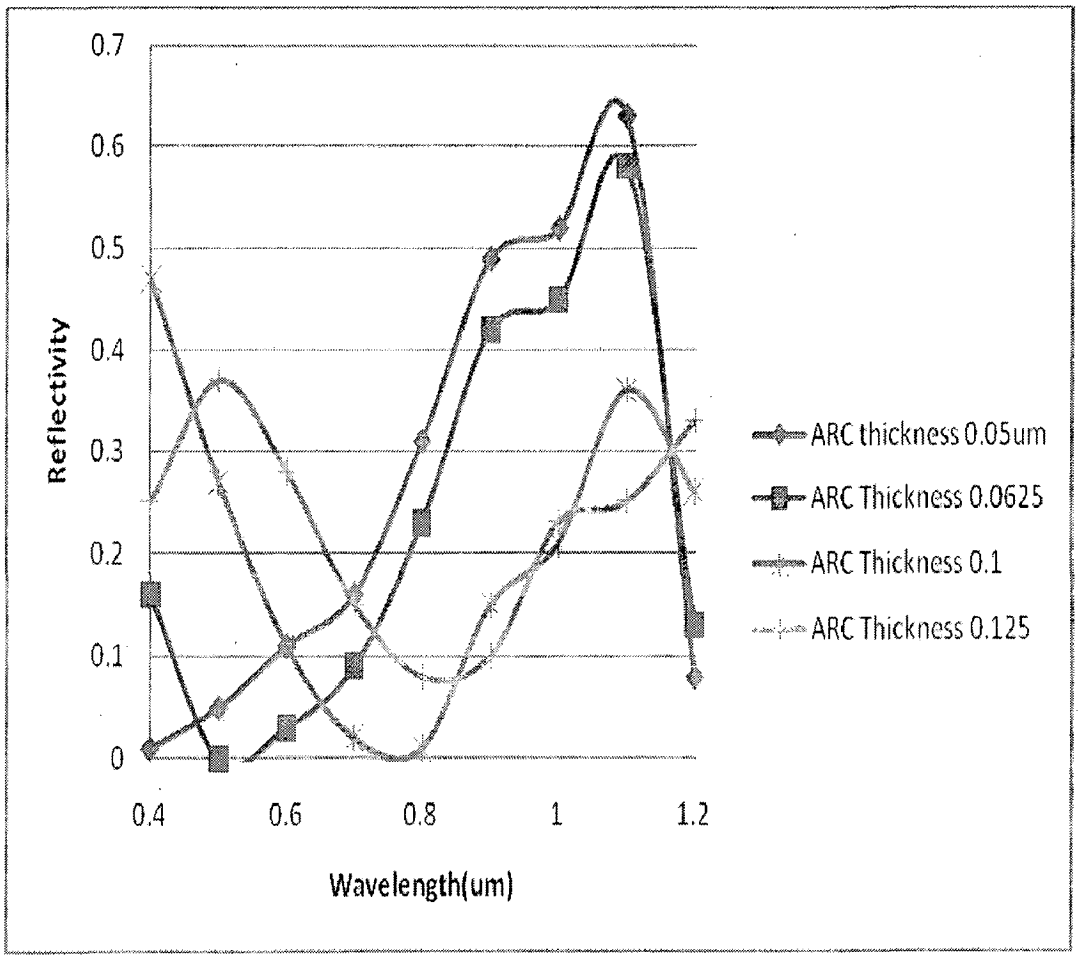


Figure 4.2.3 Reflectivity with changing ARC thicknesses.

4.3 Material Thickness

While the reduction of reflection is an essential part of achieving a high efficiency solar cell, it is also essential to absorb all the light in the silicon solar cell. The amount of light absorbed depends on the optical path length and the absorption coefficient. For silicon material in excess of 10 mm thick, essentially all the light with energy above the band gap is absorbed. The 100% of the total current refers to the fact that at 10 mm, all the light which can be absorbed in silicon is absorbed. In material of 10 microns thick, only 30% of the total available current is absorbed. The photons which are lost are the orange and red photons. Figure 4.3.1 shows that with increasing cell thickness more light is absorbed in the cell which translates to an increase in Voc and Jsc.

The optimum device thickness is not controlled solely by the need to absorb all the light. For example, if the light is not absorbed within a diffusion length of the junction, then the light-generated carriers are lost to recombination. As discussed in the "voltage losses due to recombination" section, a thinner solar cell which retains the absorption of the thicker device may have a higher voltage. Consequently, an optimum solar cell structure will typically have "light trapping" in which the optical path length is several times the actual device thickness, where the optical path length of a device refers to the distance that an unabsorbed photon may travel within the device before it escapes out of the device. This is usually defined in terms of device thickness. For example, a solar cell with no light trapping features may have an optical path length of one device thickness, while a solar cell with good light trapping may have an optical path length of 50 times the device thickness, indicating that light bounces back and forth within the cell many times.

4.4 Recombination Losses

Photons incident on the solar cell generate electron hole pairs; these generated pairs are called as excess carriers. The generated carriers need to be separated before they recombine, with emission of energy. Recombination causes loss of carriers and affects the performance of the cell. Open circuit voltage V_{oc} of the cell is affected by recombination of carriers. As recombination increases V_{oc} reduces. Various techniques are used to reduce the recombination in the solar cells and improve V_{oc}. Generation of carriers is in the entire volume of the solar cell material. The carriers

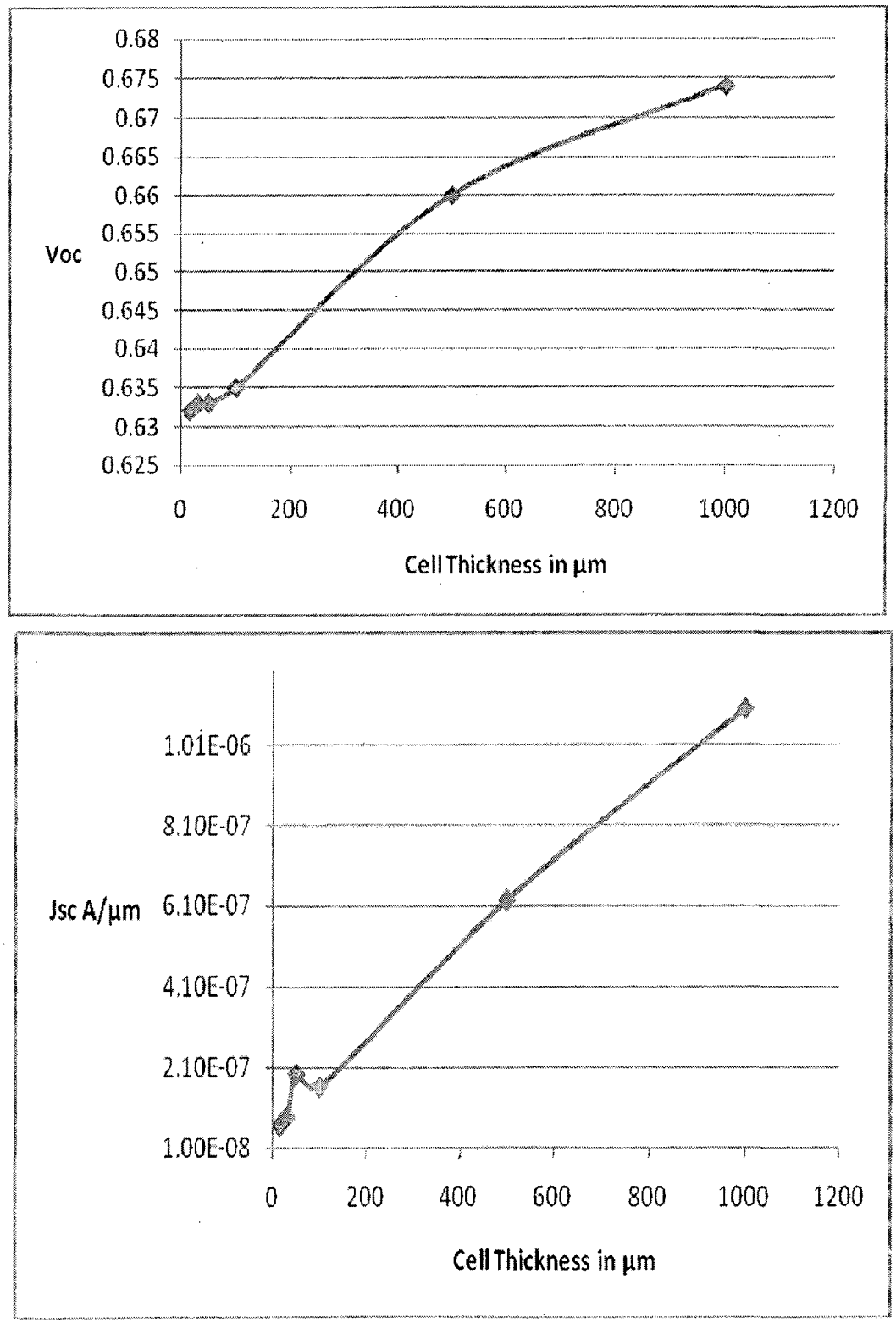


Figure 4.3.1 Change in Voc and Jsc with increasing cell thickness

generated near depletion region are separated out very quickly as they get swept away by the electric field present in the depletion region. Whereas the carriers which are

generated away from the depletion region that is in the bulk region, on the surface, or at the back surface have less probability of getting separated. These carriers will be lost and would not contribute to the current flow if they recombine. Recombination of carriers generated in the Solar cells due to photo excitation is one of the most dominating loss mechanisms occurring in the solar cell. Various mechanisms which contribute to the recombination phenomenon are included and are shown in Figure 4.4.1. These and described below

1. *Band to band recombination*: It is a radiative form of recombination in which an electron from conduction band combines with the hole in the valence band with emission of energy (light). Band to band recombination most efficiently occurs in direct band gap semiconductors. The emitted photon has an energy similar to the band gap and is therefore only weakly absorbed such that it can exit the piece of semiconductor.

2. *Trap assisted recombination*: It is the dominant form of recombination mechanism in most of the solar cells. Recombination through defects, also called Shockley-Read-Hall or SRH recombination, does not occur in perfectly pure, defect free materials. Due to the impurities present in the semiconductor an additional energy level E_t is introduced within the forbidden energy gap. This energy level acts as a trap and captures electrons and holes, leading to recombination. Trap assisted recombination is a two step process in which electrons and holes recombine in traps and then fall back into the valence band, completing the recombination process. The rate at which carriers move into the energy level in the forbidden gap depends on the energy difference distance of the introduced energy level from either of the band edges. Therefore, if an energy level is introduced close to either band edge, recombination is less likely as the electron is likely to be re-emitted to the conduction band edge rather than recombine with a hole which moves into the same energy state from the valence band. For this reason, energy levels near mid-gap are very effective for recombination.

3. *Surface recombination*: Surface of the solar cell has a large number of dangling bonds due to abrupt termination of crystal structure. These dangling bond acts as recombination centres. Carriers generated at the surface fall in to the dangling bonds and recombine with holes.

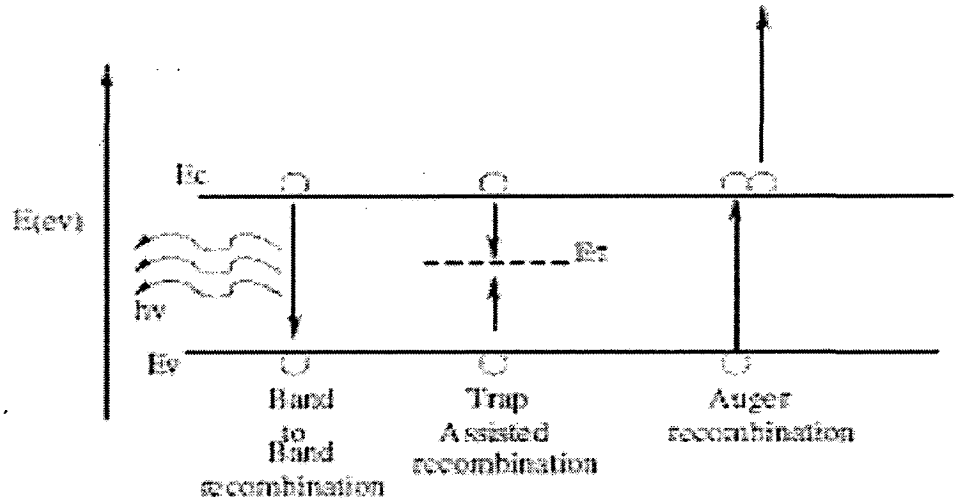


Figure 4.4.1 various recombination losses

4. *Auger recombination*: Solar cells when exposed to high intensity of photons, exhibit the phenomenon of Auger recombination. It involves three particle electron-electron-hole or hole-hole-electron. When hole from the valence band recombines with the electron in the conduction band, the excess energy released during recombination is absorbed by the neighbouring electron in the conduction band which then goes to some higher energy level and then again falls back to the conduction band with release of energy. Auger recombination is most important in heavily doped or heavily excited materials.

Recombination losses affect both the current collection (and therefore the short-circuit current) as well as the forward bias injection current (and therefore the open-circuit voltage). Recombination is frequently classified according to the region of the cell in which it occurs. Typically, recombination at the surface (surface recombination) or in the bulk of the solar cell (bulk recombination) are the main areas of recombination. The depletion region is another area in which recombination can occur (depletion region recombination). Surface recombination can have a major impact both on the short-circuit current and on the open-circuit voltage. High recombination rates at the top surface have particularly detrimental impact on the short-circuit current since top surface also corresponds to the highest generation region of carriers in the solar cell. Lowering the high top surface recombination is

typically accomplished by reducing the number of dangling silicon bonds at the top surface by growing a "passivating" layer (usually silicon dioxide) on the top surface. Since the passivating layer for silicon solar cells is usually an insulator, any region which has an ohmic metal contact cannot be passivated using silicon dioxide. Instead under the top contacts, the effect of the surface recombination can be minimised by increasing the doping. While typically such a high doping severely degrades the diffusion length, the contact regions do not participate in carrier generation and hence the impact on carrier collection is unimportant.

A similar effect is employed at the rear surface to minimize the impact of rear surface recombination velocity on voltage and current if the rear surface is closer than diffusion length to the junction. A "Back Surface Field" (BSF) consists of a higher doped region at the rear surface of the solar cell. The interface between the high and low doped region behaves like a *p-n* junction and an electric field forms at the interface which introduces a barrier to minority carrier flow to the rear surface. The minority carrier concentration is, thus, maintained at higher levels in the undoped region and the BSF has a net effect of passivating the rear surface.

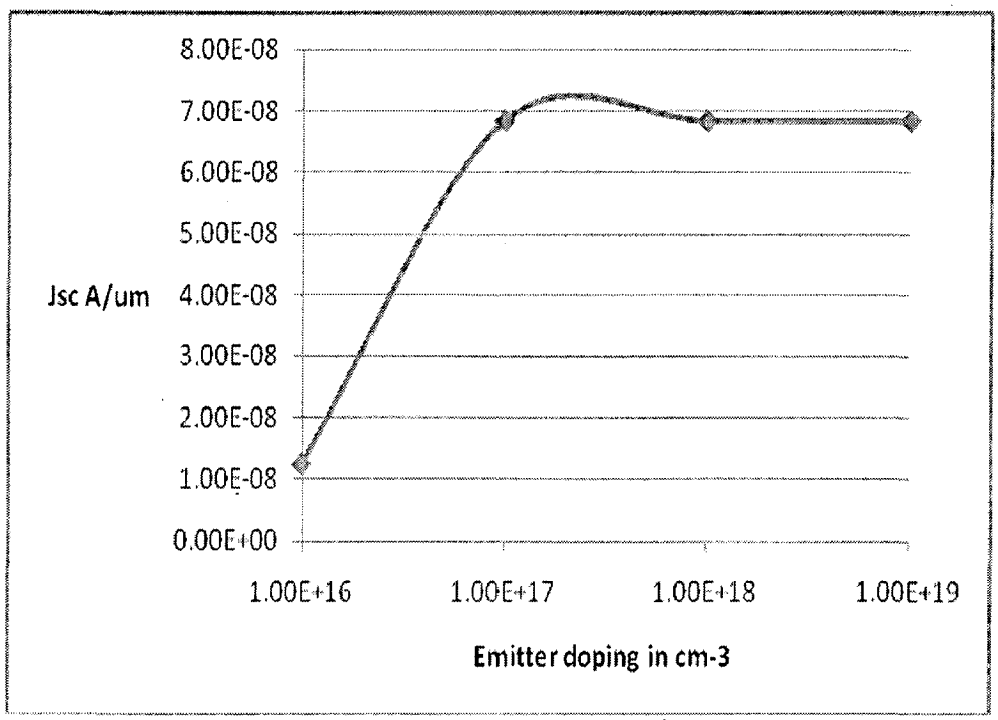
4.5 Current Losses Due to Recombination

In order for the *p-n* junction to be able to collect all of the light-generated carriers, both surface and bulk recombination must be minimised. In silicon solar cells, the two conditions commonly required for such current collection are:

- The carrier must be generated within a diffusion length of the junction, so that it will be able to diffuse to the junction before recombining and
- In the case of a localised high recombination site (such as at an unpassivated surface or at a grain boundary in multicrystalline devices), the carriers must be generated closer to the junction than to the recombination site. For less severe localised recombination sites, (such as a passivated surface), carriers can be generated closer to the recombination site while still being able to diffuse to the junction and be collected without recombining.

Figure 4.5.1 shows how the cell short circuit current reduces with increasing doping for the base and emitter. Increasing the doping takes the junction deeper into the cell and hence should increase the number of carriers collected by the contacts. However, bulk recombination dominates due to reduced material quality. This reduces

the current. The presence of localised recombination sites at both the front and the rear surfaces of the silicon solar cell means that photons of different energy will have different collection probabilities.



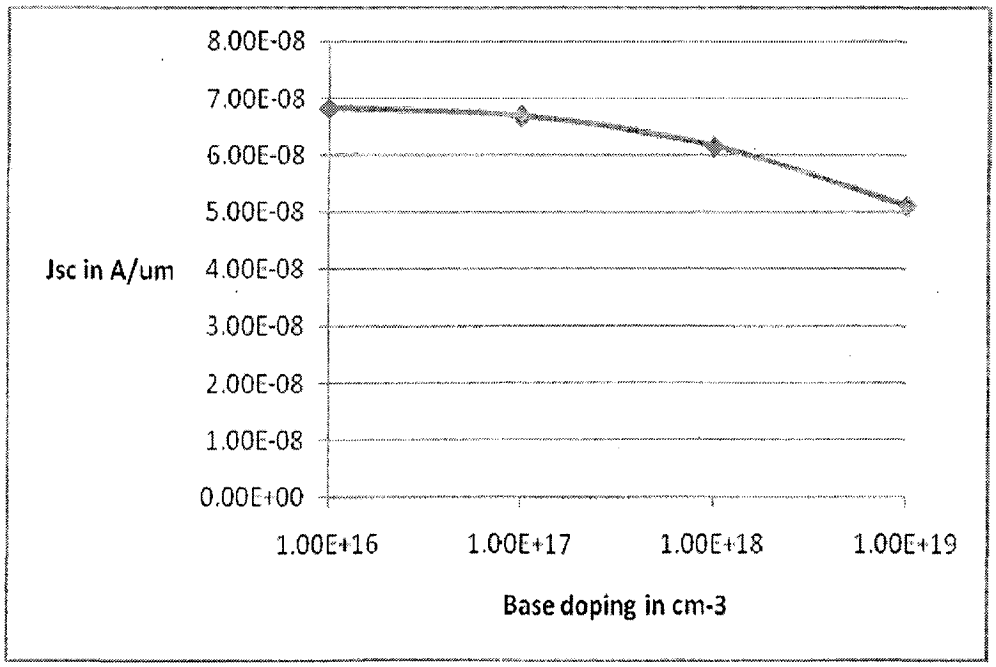


Figure 4.5.1 Change in short circuit current density with varying emitter and base doping

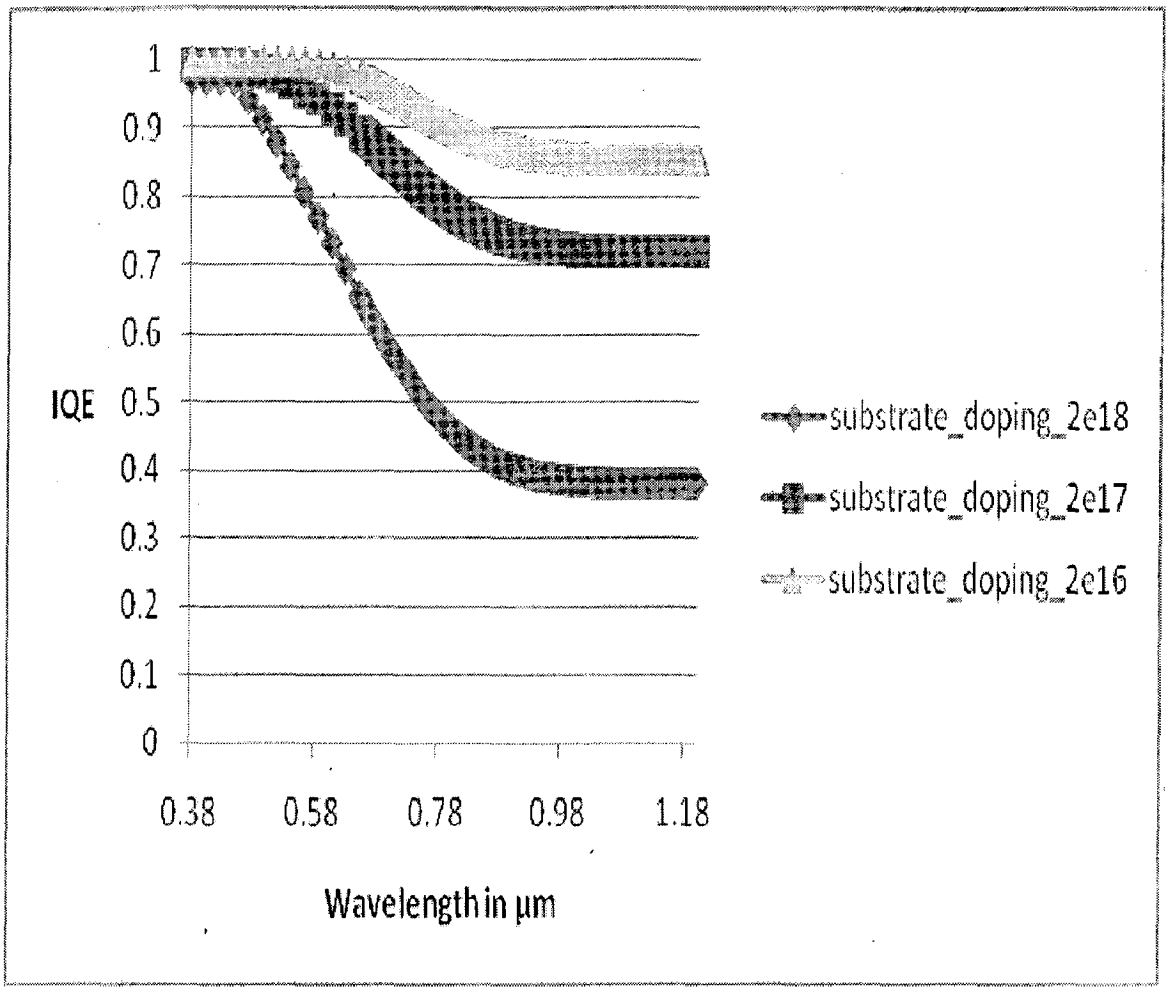


Figure 4.5.2 Change in IQE with increasing substrate doping

The quantum efficiency of a solar cell quantifies the effect of recombination on the light generation current. Figure 4.5.2 shows how the IQE reduces with increasing substrate doping. This translates to a reduction in current obtained from the cell. Since blue light has a high absorption coefficient and is absorbed very close to the front surface, it is not likely to generate minority carriers that can be collected by the junction if the front surface is a site of high recombination. Similarly, a high rear surface recombination will primarily affect carriers generated by infrared light, which can generate carriers deep in the device.

4.6 Voltage Losses Due to Recombination

The open-circuit voltage is the voltage at which the forward bias diffusion current is exactly equal to the short circuit current. The forward bias diffusion current is

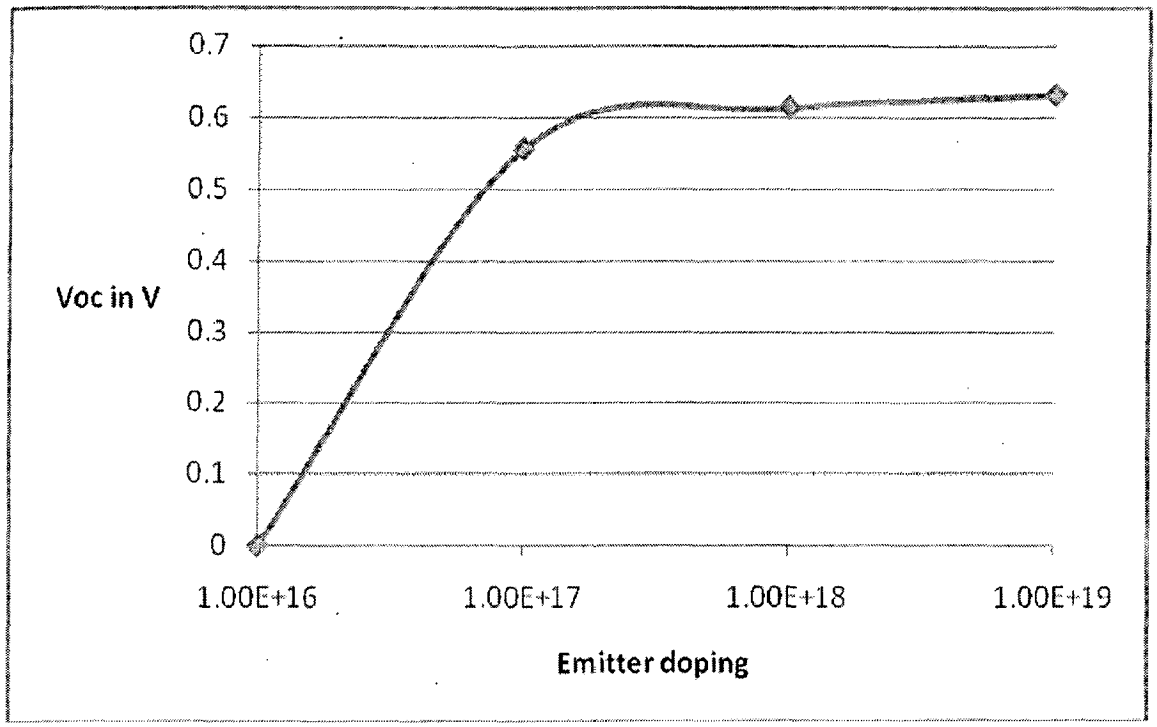
dependent on the amount of recombination in a *p-n* junction and increasing the recombination increases the forward bias current. Consequently, high recombination increases the forward bias diffusion current, which in turn reduces the open-circuit voltage. The material parameter which gives the recombination in forward bias is the diode saturation current. The recombination is controlled by the number of minority carriers at the junction edge and depends as to how fast they move away from the junction and how quickly they recombine. Consequently, the dark forward bias current, and hence the open-circuit voltage is affected by the following parameters:

- The number of minority carriers at the junction edge. The number of minority carriers injected from the other side is simply the number of minority carriers in equilibrium multiplied by an exponential factor which depends on the voltage and the temperature. Therefore, minimising the equilibrium minority carrier concentration reduces recombination. Minimising the equilibrium carrier concentration is achieved by **increasing the doping**;

- The diffusion length in the material. A low diffusion length means that minority carriers disappear from the junction edge quickly due to recombination, thus, allowing more carriers to cross and increasing the forward bias current. Consequently, to minimise recombination and achieve a high voltage, a **high diffusion length is required.** The diffusion length depends on the type of material, the processing history of the wafer and the doping in the wafer. High doping reduces the diffusion length, thus introducing a trade-off between maintaining a high diffusion length (which affects both the current and voltage) and achieving a high voltage;

- The presence of localised recombination sources within a diffusion length of the junction. A high recombination source close to the junction (usually a surface or a grain boundary) will allow carriers to move to this recombination source very quickly and recombine, thus dramatically increasing the recombination current. The impact of surface recombination is reduced by **passivating the surface**.

The net effect of previous trade-offs is shown in the graphs below.



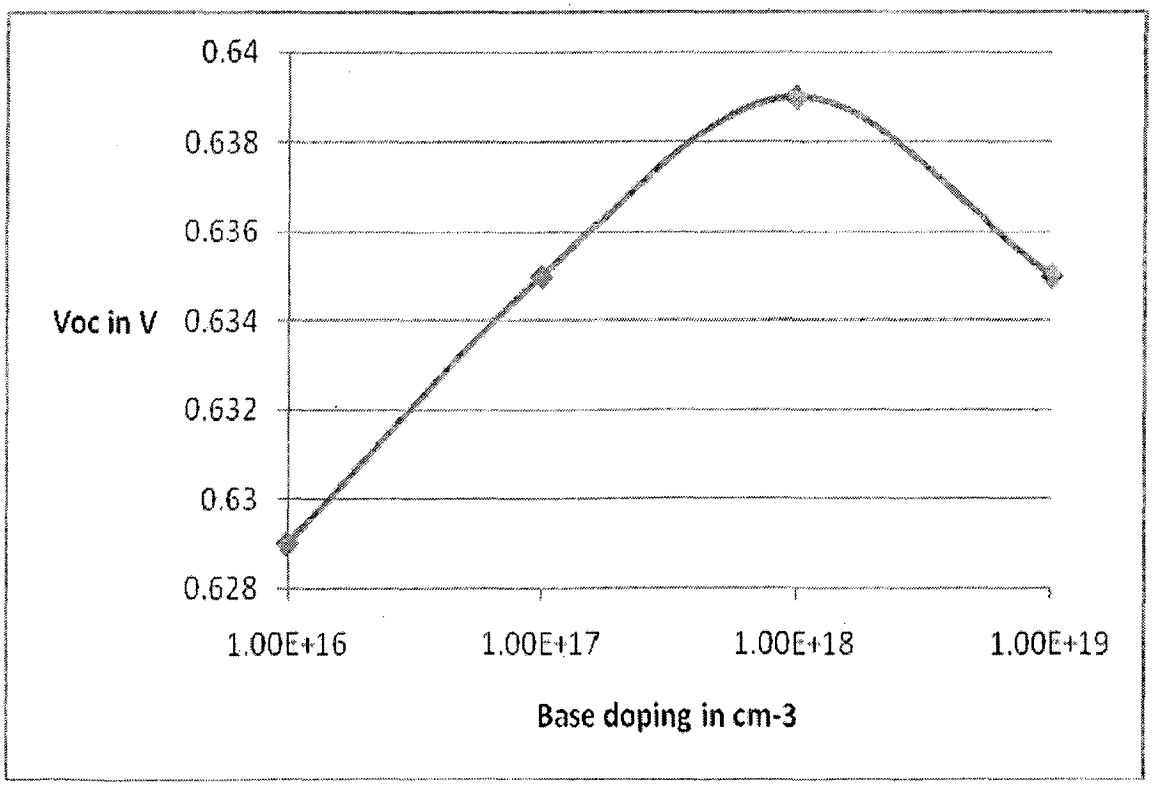


Figure 4.6.1Effect of variation in emitter and base doping on Voc

4.7 Emitter Resistance

Based on the sheet resistivity, the power loss due to the emitter resistance can be calculated as a function of finger spacing in the top contact. Refer to Appendix for the derivation of total power lost due to emitter resistance. Using equation (B.4) the power lost due to emitter resistance is shown in Figure 4.7.1.

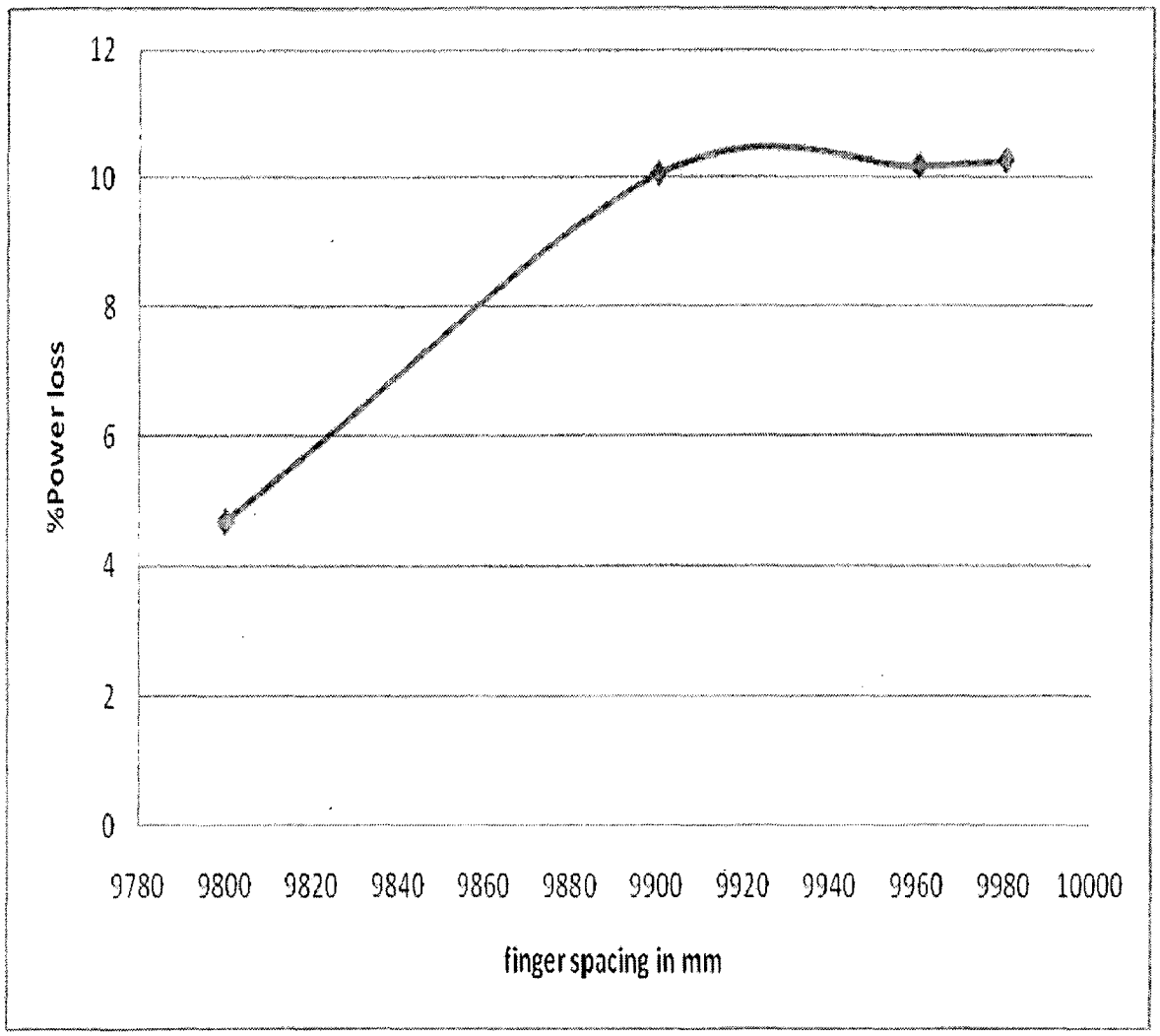


Figure 4.7.1 Power loss due to emitter reisitance with variation in finger spacing for a (10X10) mm structure.

4.8 Finger Resistance

To provide higher conductivity, the top of the cell has a series of regularly spaced fingers. The resistive loss in a finger is calculated and given in the Appendix. The structure has been altered to have two contacts, one each at either ends of the top surface. The spacing between the fingers is varied and using equation (B.6), the power loss due to finger resistance is plotted below.

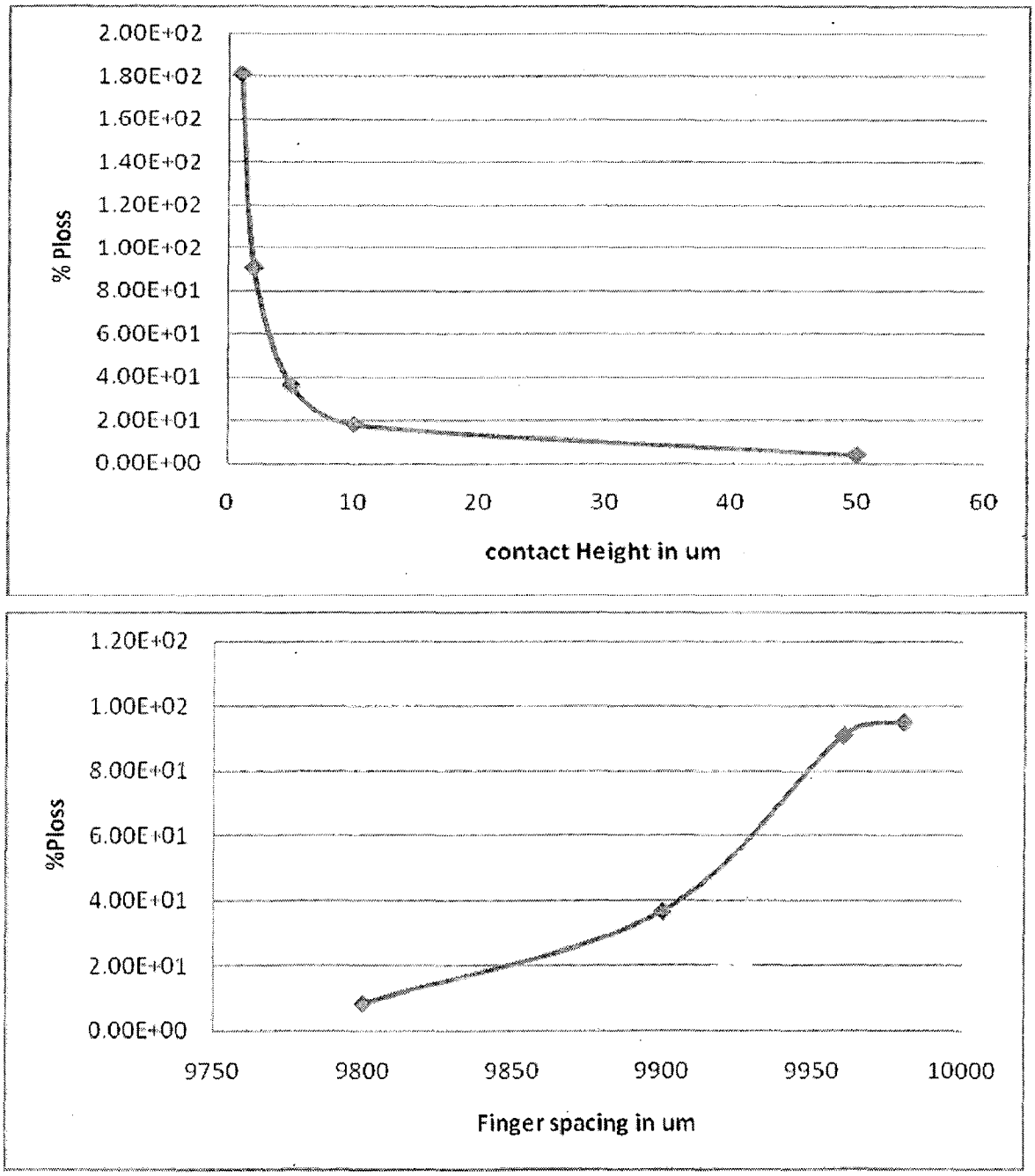


Figure 4.8.1 Power loss in finger due to varying finger height and finger width

It is seen that as the finger width is increased or the finger spacing is reduced, the power loss is reduced. However this occurs at the expense of shading losses which increase due to increased contact area. Similarly, varying the contact height reduces the contact resistance significantly but increasing the height can increase the shadow losses since light is not always perpendicular to the cell.

4.9 Effect of Intrinsic Electric Field

It is well known that the presence of electric field can improve solar cell performance [18], although an electric field is not an essential requirement for photovoltaic conversion. Doping gradients can induce built-in fields in solar cells [8]. The effect of electric fields created by doping gradients is quantitatively analyzed and clear boundaries are found as to when built-in fields are beneficial or deleterious. In the case of a doping gradient $N_A(x)$ in the p-type material, approximate balance between majority carrier hole drift and diffusion generates a field E ideally given by

$$E_p = \frac{kT}{qN_A}\frac{dN_A}{dx} \tag{4.9.1}$$

where kT/q is the thermal voltage (25.852mV at 300K). This field acts in the opposite direction on electrons as compared to holes and can aid the collection of the minority carrier electrons [12].

Under low injection – a regime of particular importance for solar cell operation the majority carrier concentration can be assumed excitation independent, and the effect of recombination can be discussed in terms of minority- carrier lifetime. In p-type material, for example the recombination rate can be written as

$$U = \frac{1}{\tau_n}(n - n_0) \tag{4.9.2}$$

where τ_n is the minority-carrier (electron) lifetime and $(n - n_o)$ is the excess electron concentration. The inverse of the lifetime – the rate constant – is a sum of the different contributions to the lifetime.

$$\frac{1}{\tau} = \frac{1}{\tau_{rad}} + \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{SRH}} \tag{4.9.3}$$

Radiative recombination is very less for an indirect bandgap semiconductor like silicon. SRH recombination dominates for doping levels below 10^{18} cm^{-3}. However, there is no general agreement about the dominant mechanism that limits the minority carrier lifetime in heavily doped silicon (in the range of 10^{18}-10^{20} cm^{-3}). There is a common observation that lifetime decreases with increasing dopant concentration. Phonon assisted band to band Auger recombination appears to explain the measured lifetimes satisfactorily in p-type silicon [13,14]. The effect of lifetime on transport properties by carrier diffusion can be discussed in terms of diffusion length defined by .

$$L_n=\sqrt{D_n\tau} \tag{4.9.4}$$

where D_n is the diffusion constant for the minority carriers in question. The contribution to lifetime due to defects has been empirically observed to follow the equations [5]

$$\frac{1}{\tau_{SRH}}=(\frac{1}{2.5*10^{-3}}+11.76*10^{-13}N_A)(\frac{300}{T})^{0.57} \tag{4.9.5}$$

Similarly the contribution by band to band Auger recombination can be described by the expression [5]

$$\frac{1}{\tau_{AUGER}}=1.83*10^{-31}N_A^{\ 2}(\frac{T}{300})^{1.18} \tag{4.9.6}$$

Electric fields created by nonhomogeneously doped silicon can be analyzed by present day device simulators [15]. A Gaussian transition with varying standard deviation creates an electric field which reaches its maximum at the middle of its gradient range and scales with the absolute value of the variation of the doping concentration. Depending on the smoothness of the doping profile, the maximum value of the field varies. In our 2D solar cell structure, by varying the standard deviation of the Gaussian back surface field, we observed an electric field in the substrate whose peak varies depending on the doping gradient. Figure 4.9.1 shows the doping gradient in the substrate generated by varying the back doping depth.

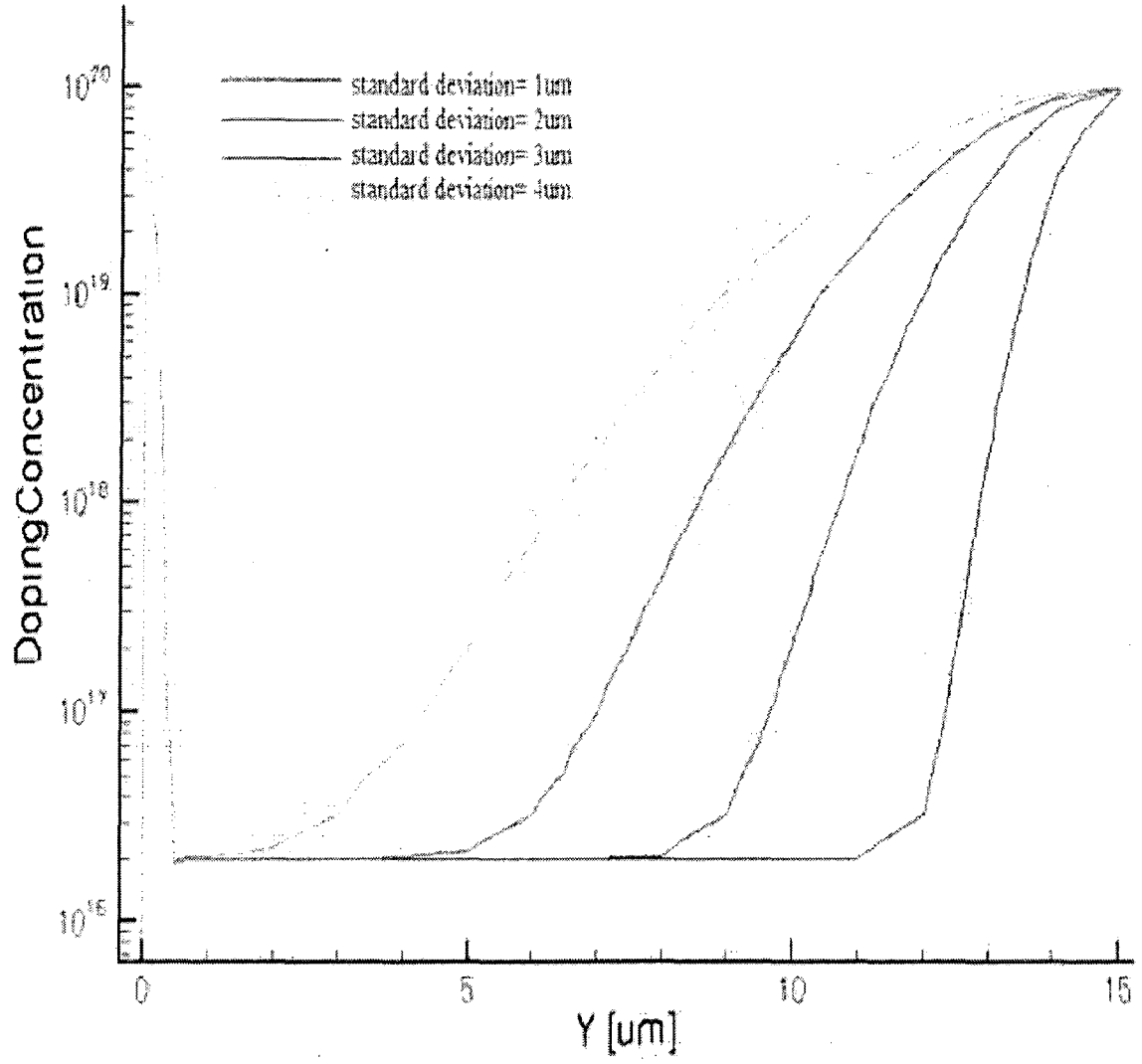


Figure 4.9.1 Variation in the doping concentration in the substrate with different back doping depths

According to equation (4.9.1), this doping gradient generates an electric field in the substrate as shown in Figure 4.9.2. The highest field (840 V/cm) is seen for the least doping depth while the least (207 V/cm) is seen for the largest spread in the Gaussian profile. The average field in the substrate due a Gaussian spread of 4μm is more than 100V/cm. This field should help in the collection of minority carriers i.e. electrons which were optically generated in the substrate. Consequently we should see an increase in the collected current. However the effect of the heavy doping ($>10^{18}$ cm^{-3}) on the minority carrier lifetime affects the device characteristics adversely as we shall see in the next section. The reference structure used in comparison has zero

electric field over most of the substrate as seen by the graph corresponding to the doping depth of 1μm.

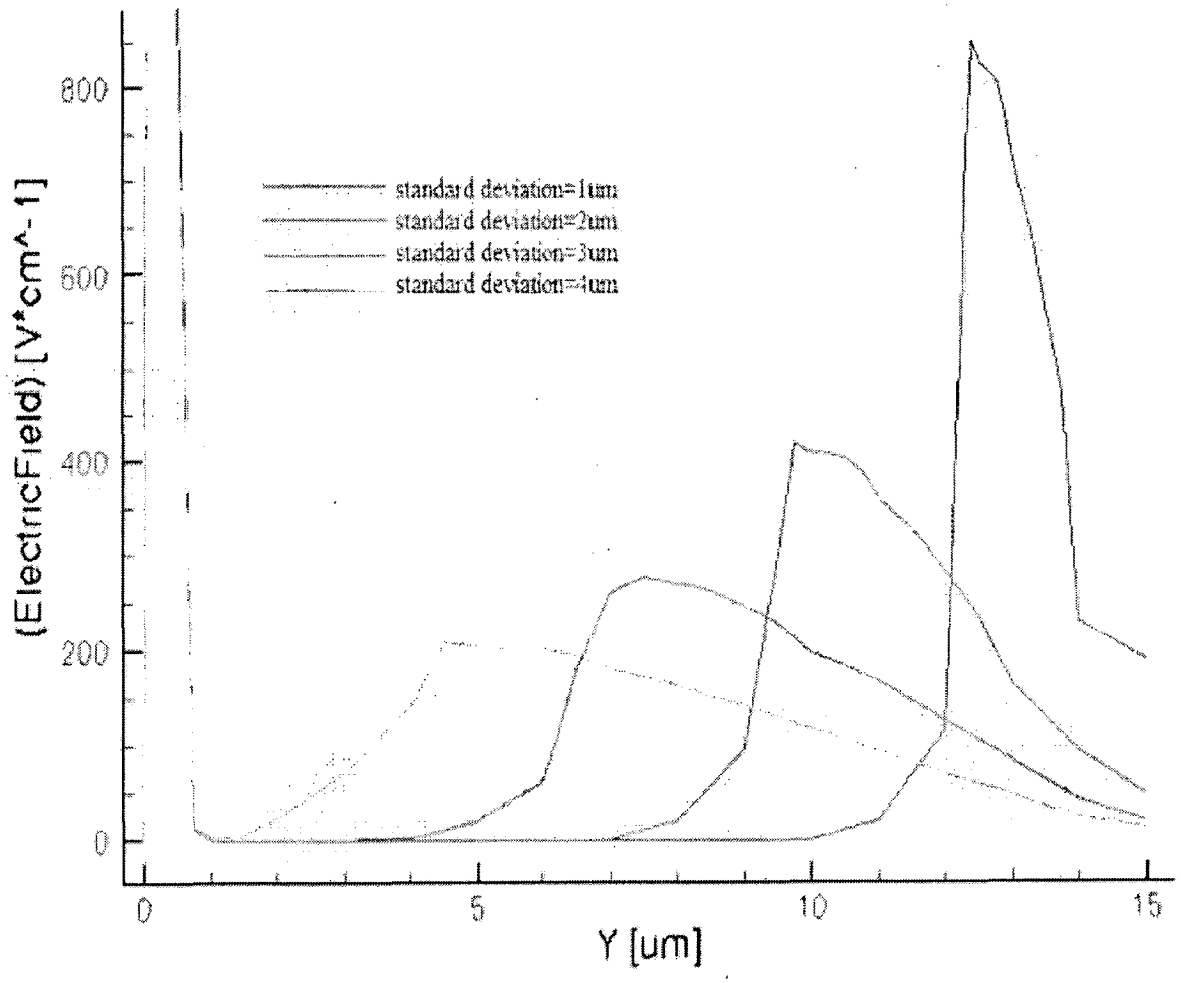


Figure 4.9.2. Electric field in the substrate due to different Gaussian doping profiles.

Consider the case when the back doping depth is 4μm. The doping concentration varies from $1e^{20}cm^{-3}$ at the rear contact to $2e^{16}cm^{-3}$ in the substrate near the junction line. This doping gradient causes an electric field throughout the substrate with average value exceeding 100V/cm.

From equation (4.9.6), we see that this decreases the lifetime proportional to the square of doping. The overall effect of this is that the total minority carrier lifetime reduces significantly than for the case with no electric field in the substrate.

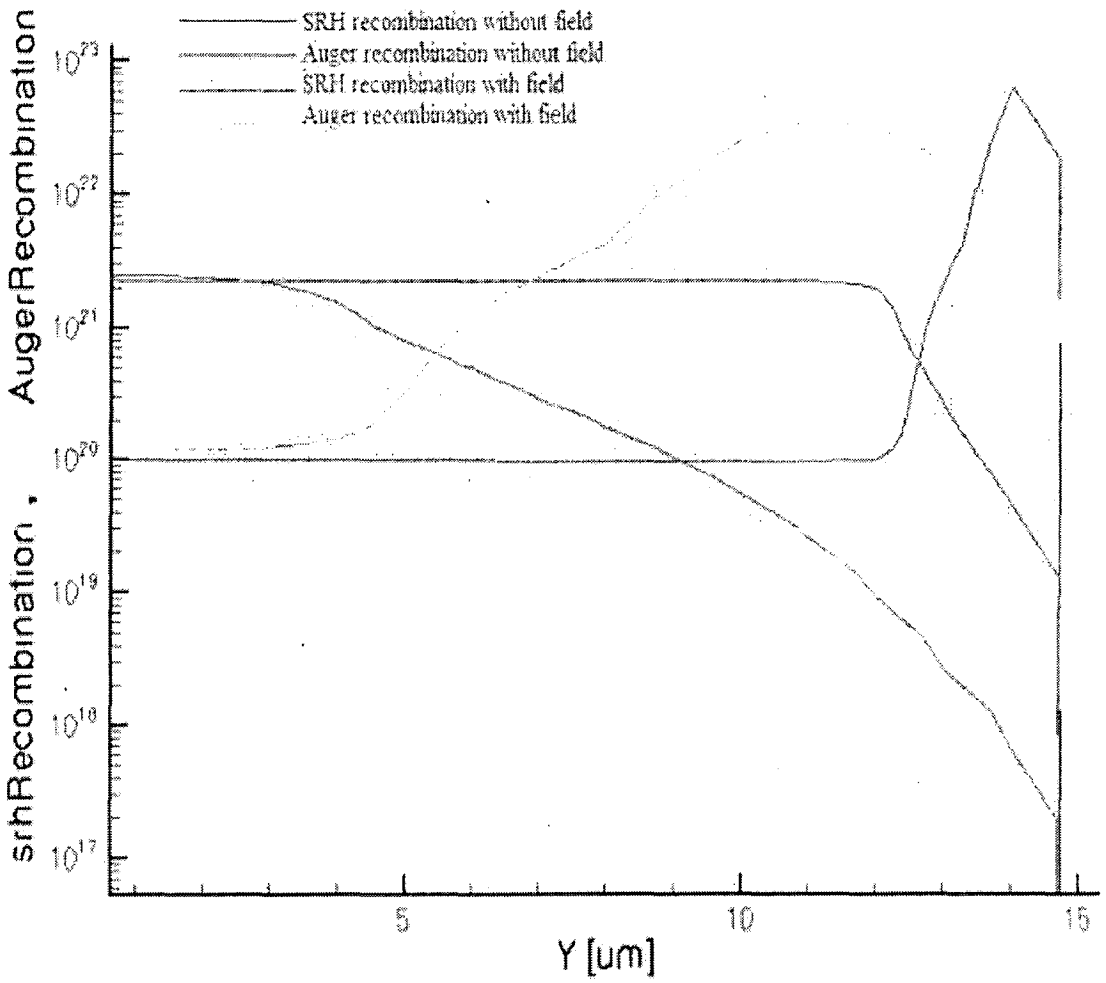


Figure 4.9.3 Variation in Auger and SRH recombination with and without electric field.

The length of substrate for which the doping exceeds $10^{18}cm^{-3}$ sees a dominance of band to band Auger recombination as seen in Figure 4.9.3

From equation (4.9.4), this has an adverse effect on the diffusion length and we see a net increase in the total recombination in the substrate. This is seen in Figure 4.9.4. The effect of increased recombination and reduced lifetime is seen in the electrical characteristics of the cell. The maximum short circuit current reduces by 8% to $6.437e^{-8}$ A/μm. The open circuit voltage increases by 1.5 % to 0.641 V. The maximum power reduces by 5.7 % to $3.451e^{-8}$ W/um. The marginal increase in the V_{OC} is because the substrate field aids the junction field in separation of carriers. However, the lifetime is dominated by the recombination in the substrate. A plot of the maximum power obtained from the cell for different back doping depths is shown

in Figure 4.9.5. We see that increasing the back doping depth increases the average field in the substrate and reduces the cell performance.

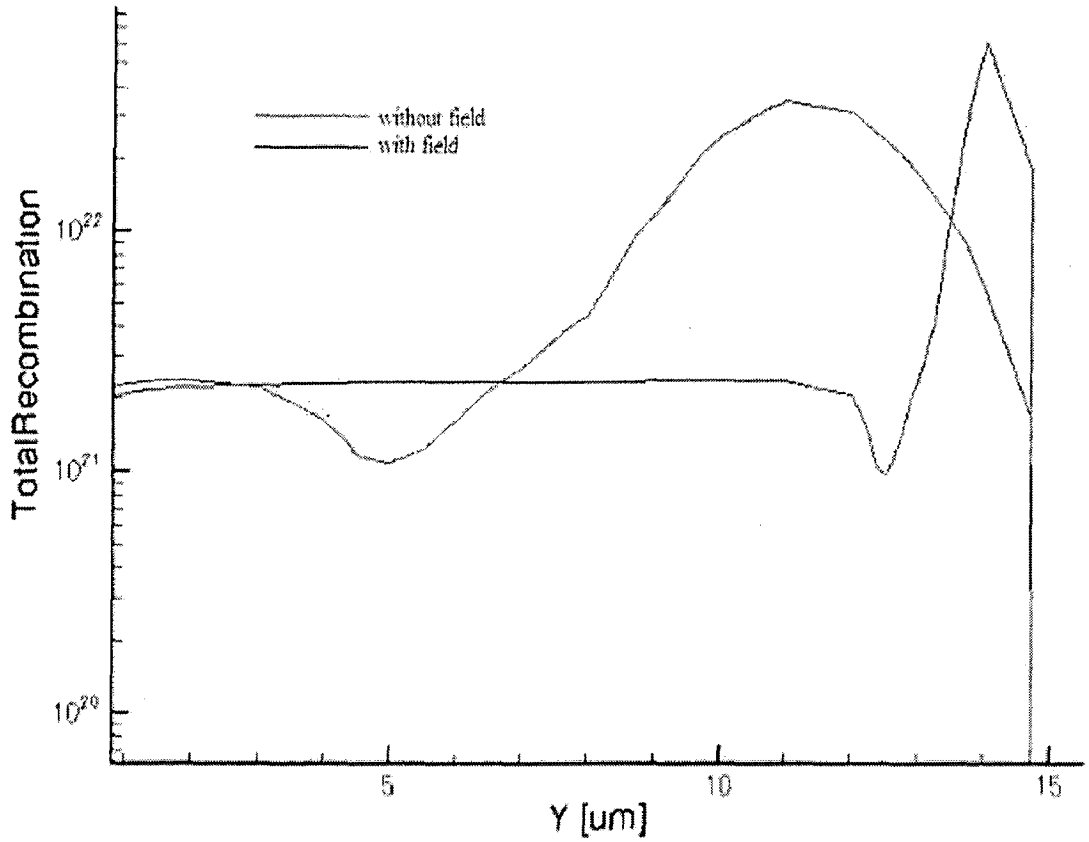


Figure 4.9.4. Variation in total recombination with and without electric field.

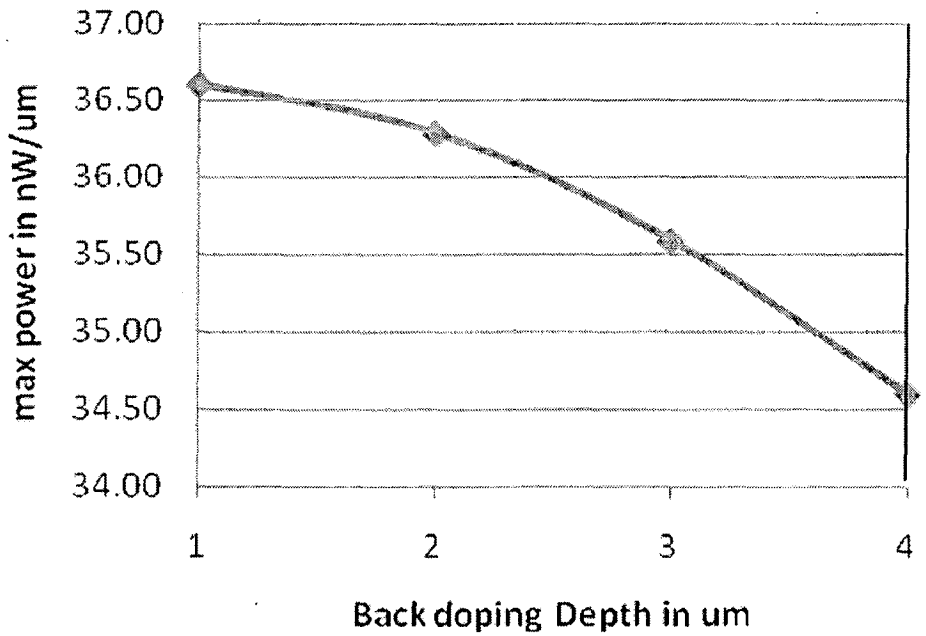


Figure 4.9.5 Maximum power points versus back doping depths

4.10 Effect of Temperature

Like all other semiconductor devices, solar cells are sensitive to temperature. Increase in temperature reduces the band gap of a semiconductor, thereby effecting most of the semiconductor material parameters. The decrease in the band gap of a semiconductor with increasing temperature can be viewed as increasing the energy of the electrons in the material. Lower energy is, therefore, needed to break the bond. In the bond model of a semiconductor band gap, reduction in the bond energy also reduces the band gap. Therefore increasing the temperature reduces the band gap.

In a solar cell, the parameter most affected by an increase in temperature is the open-circuit voltage. The impact of increasing temperature is shown in figure 4.10.1. The open-circuit voltage decreases with temperature because of the temperature dependence of I_S. The equation for I_S from one side of a *p-n* junction is [5];

$$I_S = q A \frac{D_n n_i^2}{L_n N_D}$$

where:

q is the electronic charge;

D is the diffusivity of the minority carrier given for silicon as a function of doping;

L is the diffusion length of the minority carrier;

N_D is the doping; and n_i is the intrinsic carrier concentration given for silicon

In the above equation, many of the parameters have some temperature dependence, but the most significant effect is due to the intrinsic carrier concentration, n_i. The intrinsic carrier concentration depends on the band gap energy (with lower band gaps giving a higher intrinsic carrier concentration) and on the energy which the carriers have (with higher temperatures giving higher intrinsic carrier concentrations). Figure 4.10.1 shows the effect of temperature on open circuit voltage.

4.11 Effect of Diode Ideality Factor

The ideality factor of a diode is a measure of how closely the diode follows the ideal diode equation. The derivation of the simple diode equation uses certain assumption about the cell. In practice, there are second order effects so that the diode does not follow the simple diode equation and the ideality factor provides a way of describing them. The ideal diode equation assumes that all the recombination occurs

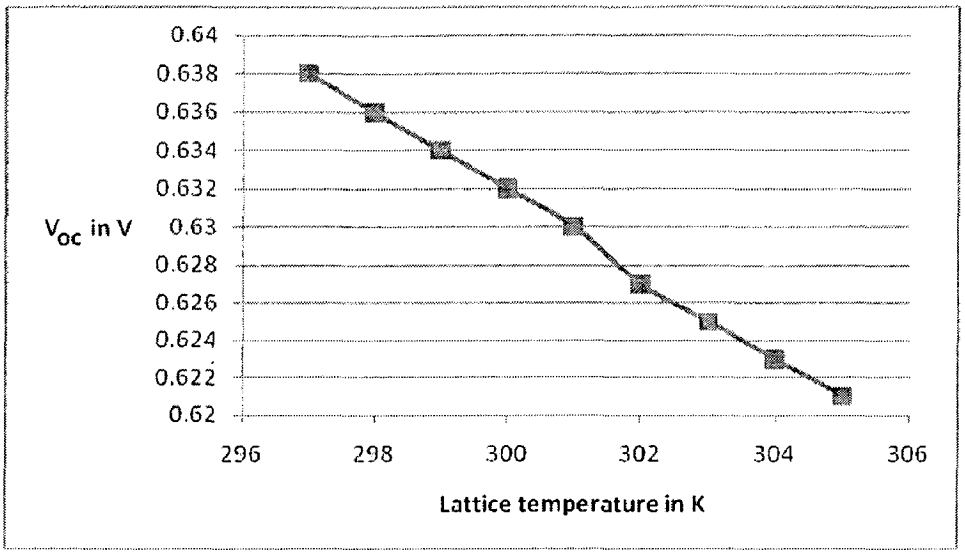


Figure 4.10.1 Effect of temperature on Voc

via band to band or recombination via traps in the bulk areas from the device (i.e. not in the junction). From the derivation showed earlier and from equation 2.2.2 the ideal diode current equation is produced here again for convenience

$$I = I_L - I_0[(\exp\frac{qV}{\eta KT})-1]$$

However recombination does occur in other ways and in other areas of the device. These recombinations produce ideality factors that deviate from the ideal value. Deriving the ideal diode equation by considering the number of carriers that need to come together during the process produces the results given in Table 4.11 below.

Recombination type	Ideality factor	Description
SRH, band to band(low level injection)	1	Recombination limited by minority carrier
SRH, band to band(high level injection)	2	Recombination limited by both carrier types
Auger	2/3	Two majority and one minority carriers required for recombination
Depletion region (junction)	2	two carriers limit recombination

Table 4.11 Dependence of ideality factor on recombination type [8]

The ideality factor is derived from the slope of the dark-IV and the optical-IV curve. The basic cell equation in the dark is:

$$I = I_0[(\exp\frac{qV}{\eta KT})-1]$$

where I is the current through the diode, V is the voltage across the diode, I_0 is the dark saturation current, η is the ideality factor and T is the temperature in Kelvin. q and k are both constants. For V > 50 - 100 mV, the negative unity term can be ignored and so the above equation reduces to:

$$I = I_0(\exp\frac{qV}{\eta KT})$$

taking the log of both sides of the equation gives

$$\ln(I) = \ln(I_o) + (\frac{q}{\eta KT})V$$

When plotting the natural log of the current against the voltage, the slope gives $q/\eta kT$ and the intercept gives $ln(I_o)$. In real cells, the ideality factor depends on the voltage across the cell. The ideality factor can either be plotted as a function of voltage or it can be given as a single value. Since the ideality factor varies with voltage, the voltage also needs to be given. Deviations in the ideality factor from unity indicate that either there are unusual recombination mechanisms taking place or that the recombination is changing in magnitude. Thus the ideality factor is a powerful tool for examining the recombination in a device. There are several problems when measuring ideality factors:

- At low voltages, the shunt resistance (R_{shunt}) dominates the device performance and causes a large peak. It is usually not possible in practice to correct for the effects of R_{shunt}.
- In a dark-IV curve, at high voltages the series resistance dominates and this causes a large peak in the ideality factor curve at high voltages. The ideality factor graph is shown in figure 4.11.1. The single diode equation assumes a constant value for the ideality factor η. In reality, the ideality factor is a function of voltage across the device as noted in the previous discussion.

At high voltage, when the recombination in the device is dominated by the surface and the bulk regions, the ideality factor is close to unity. However at lower voltages,

recombination in the junction dominates and the ideality factor approaches a value close to 2. The junction recombination is modeled by adding a second diode in parallel with the first and setting the ideality factor typically to 2 as shown in Figure 4.11.2.

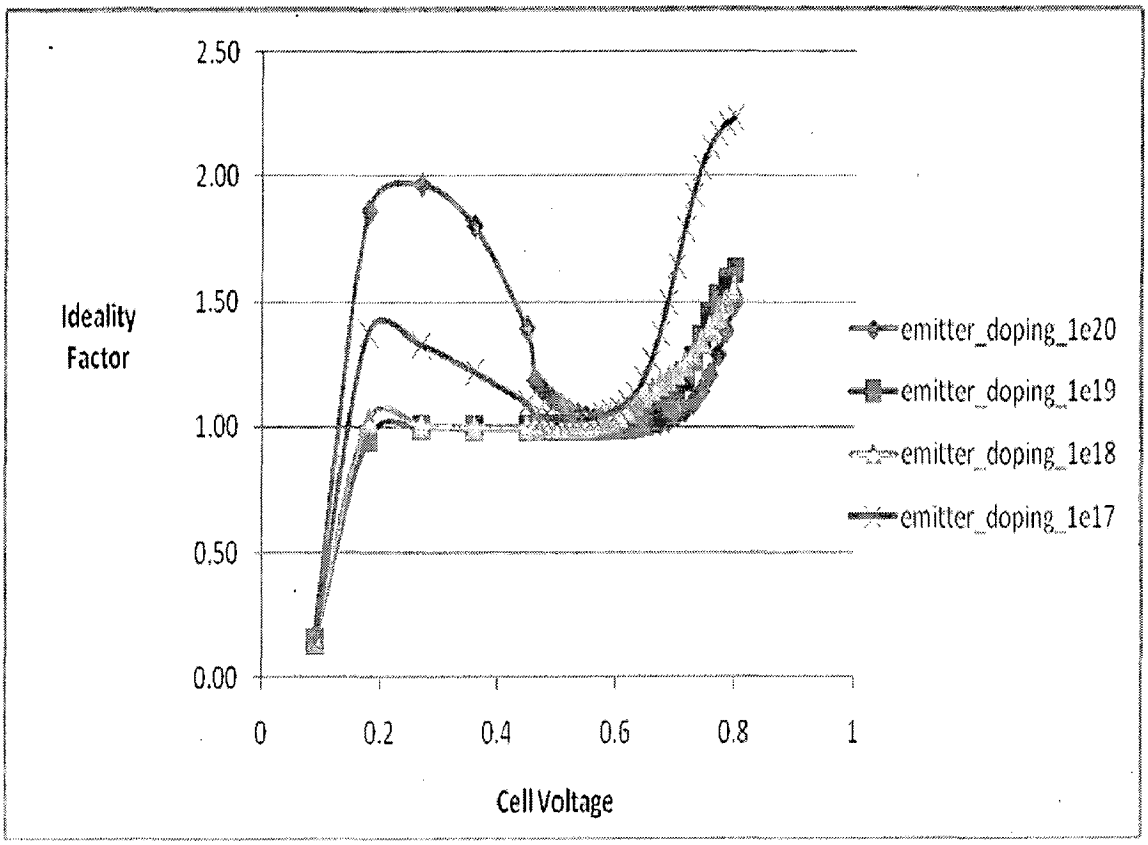


Figure 4.11.1 Effect of emitter doping on diode Ideality factor

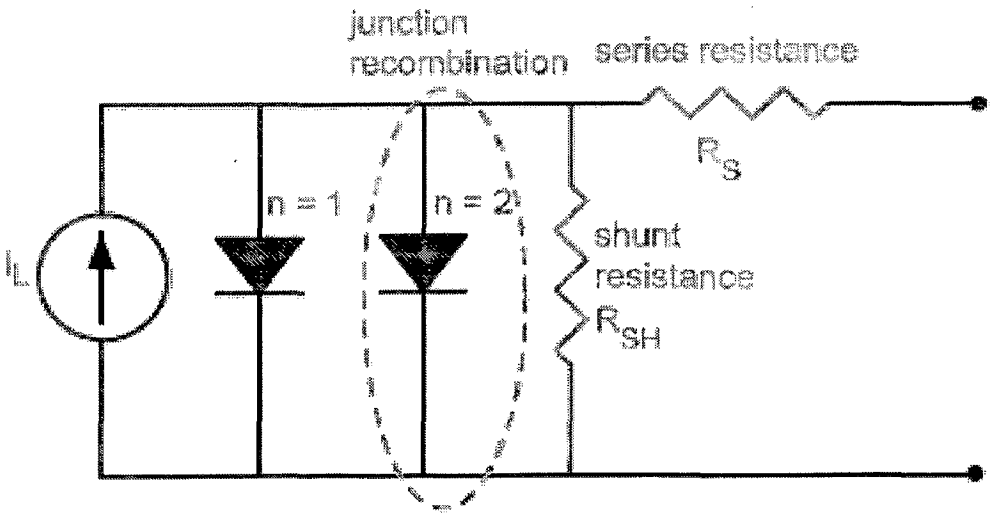


Figure 4.11.2 Circuit of the double diode model including the parasitic series and shunt resistances [4]

5 OBSERVATIONS AND DISCUSSION

The silicon solar cell was studied in chapter 4 by taking into account its various design parameters, effects of physical processes like electric field and recombination as well as external factors like temperature. Here we discuss the results from an engineering design point of view and design trade-offs.

- Substrate Material: Bulk crystalline silicon dominates the current photovoltaic market, in part due to the prominence of silicon in the integrated circuit market. As is also the case for transistors, silicon does not have optimum material parameters. In particular, silicon's band gap is slightly too low for an optimum solar cell. Also since silicon is an indirect material, it has a low absorption co-efficient. While the low absorption co-efficient can be overcome by light trapping, silicon is also difficult to grow into thin sheets. However, silicon's abundance and its domination of the semiconductor manufacturing industry has made it difficult for other materials to compete.

- Cell Thickness: An optimum silicon solar cell with light trapping and very good surface passivation is about 100 μm thick. However, thickness between 200 and 500 μm are typically used, partly for practical issues such as making and handling thin wafers and partly for surface passivation reasons.

- Doping of Base: A higher base doping leads to a higher V_{oc} and lower resistance, but higher levels of doping result in damage to the crystal.

- Emitter Dopant: *N*-type silicon has a higher surface quality than *p*-type silicon so it is placed at the front of the cell where most of the light is absorbed. Thus the top of the cell is the negative terminal and the rear of the cell is the positive terminal.

- Emitter Thickness: A large fraction of light is absorbed close to the front surface. By making the front layer very thin, a large fraction of the carriers generated by the incoming light are created within a diffusion length of the *p-n* junction.

- Emitter Doping: The front junction is doped to a level sufficient to conduct away the generated electricity without resistive loses. However, an excessive level of doping reduces the material quality to the extent that carriers recombine before reaching the junction.

- Grid Pattern: The resistivity of silicon is too high to conduct away all the current generated, so a lower resistivity metal grid is placed on the surface to conduct away the current. The metal grid shades the cell from the incoming light so there is a compromise between light collection and resistance of the metal grid.

- Substrate Electric Field: Increasing the BSF doping depth reduces the maximum power and hence cell performance due to increased average doping and therefore field in the substrate.

- Parasitic Resistances: Resistive effects in solar cells reduce the efficiency by dissipating power in the resistances. Series resistance in a solar cell has three causes: firstly, the movement of current through the emitter and base of the solar cell; secondly, the contact resistance between the metal contact and the silicon; and finally the resistance of the top and rear metal contacts. The main impact of series resistance is to reduce the fill factor. Significant power losses caused by the presence of a shunt resistance, R_{SH}, are typically due to manufacturing defects, rather than poor solar cell design. Low shunt resistance causes power losses in solar cells by providing an alternate current path for the light-generated current. Such a diversion reduces the amount of current flowing through the solar cell junction and reduces the voltage.

- Anti-Reflecting Coatings: While the reflection for a given thickness, index of refraction, and wavelength can be reduced to zero using the equations described, the index of refraction is dependent on wavelength and so zero reflection occurs only at a single wavelength. For photovoltaic applications, the refractive index and thickness are chosen in order to minimize reflection for a wavelength of 0.6 μm. This wavelength is chosen since it is close to the peak power of the solar spectrum. Surface texturing, either in combination with an anti-reflection coating or by itself can also be used to minimize reflection. Any "roughening" of the surface reduces reflection by

increasing the chances of reflected light bouncing back onto the surface rather than out to the surrounding air.

For silicon solar cells, the basic design constraints on surface reflection, carrier collection, recombination and parasitic resistances result in an optimum device of about 25 % theoretical efficiency. However, this is true only under laboratory conditions with state-of-the-art technology. Commercially mass produced cells are typically only 13-14 % efficient. Figure D.1 in Appendix gives a picture on how silicon solar cell efficiencies have improved over the last decade. The overriding reason for this difference in efficiency is that the research techniques used in the laboratory are not suitable for commercial production within the photovoltaic industry and therefore lower cost techniques, which result in lower efficiency, are used.

6 CONCLUSIONS

This dissertation has addressed the performance of single junction crystalline silicon solar cells through Technology CAD simulations. The electrical and optical characteristics of a silicon solar cell were plotted using Sentaurus TCAD software. Silicon mainly responds to wavelengths above 450 nm and up to 1100 nm which is in accordance to its bandgap limitation of 1.12 eV. Silicon being an indirect type of semiconductor is less efficient in absorbing the incident radiation.

A number of factors are involved in the design of solar cells. These factors are mainly concentrated towards maximizing the cell efficiency. It has been shown that device dimensions play a major role in determining the cell output current and voltage. Having an emitter of less than 1μm ensures that most of the carriers are generated within the depletion region or within a diffusion length from the junction. To ensure good amount of light trapping, the cell should be at least 100 μm thick. Doping levels for the emitter should be higher than the substrate since it has to conduct away the current to the contacts. Doping gradients vary the electric field in the device, which affects the device characteristics adversely. Hence higher doping levels (beyond $10^{18}cm^{-3}$) should be avoided for the back surface field. Similarly, emitter doping levels upto $10^{19}cm^{-3}$ give good power output from the cell. Anti-reflective coating thickness is selected such that light in the visible spectrum is not reflected at all. It is found that with increasing lattice temperature, the performance of the cell degrades significantly. Hence a cold and sunny environment is best suited for optimum output. The pattern for the front contact grid can affect the output power significantly and hence a compromise has to be made between shading losses and finger resistance.

7 RELIABILITY ANALYSIS OF SILICON NANOWIRE MOSFETS

The phenomenal progress signified by Moore's law has been achieved through scaling of the Metal-Oxide–Semiconductor Field-Effect Transistor (MOSFET) from larger to smaller physical dimensions, thereby gaining speed and density. Shrinking the conventional MOSFET beyond 50-nm-technology node requires innovations to circumvent barriers due to the fundamental physics that constrains the conventional MOSFET. A greater electrostatic control over the channel is the need of the hour. Gate All Around (GAA) structures are the most resilient to short-channel effects among all the emerging device structures for a given silicon body thickness.

7.1 Introduction

The microelectronics industry owes a great deal of its success to the existence of the thermal oxide of silicon, i.e., silicon dioxide (SiO_2). A thin layer of SiO_2 forms the insulating layer between the control gate and the conducting channel of the transistors used in most modern integrated circuits. As circuits are made denser, all of the dimensions of the transistors are reduced ("scaled") correspondingly, so that nowadays the SiO_2 layer thickness (t_{ox}) is 2 nm or less. Aggressive scaling of the thickness of the gate insulator in CMOS transistors has caused the quality and reliability of ultrathin dielectrics to assume greater importance. Estimating reliability requires an extrapolation from the measurement conditions (e.g., higher voltage) to normal operation conditions. Hot-carrier induced phenomena are of great interest due to their important role in device reliability. High energy carriers (also known as hot carriers) are generated in MOSFETs by high electric field near the drain region. Hot carriers transfer energy to the lattice through phonon emission and break bonds at the Si/SiO_2 interface. The trapping or bond breaking creates oxide charge and interface traps that affect the channel carrier mobility and the effective channel potential. Interface traps and oxide charge also affect the transistor parameters, such as, threshold voltage and drive currents. The current flowing through an ultrathin gate oxide is not merely a nuisance parasitic, but also causes reliability problems by leading to long-term parameter shifts (wear out) and eventually to oxide breakdown. The stress induced parameter shifts are gradual and the degradation is predictable on the basis of experimental data and physical models. The impact on device design, therefore, involves an engineering tradeoff between short-term and long-term

performance. Breakdown is generally understood to be the result of a gradual and predictable buildup of defects such as electron traps in the oxide, but the precise point at which breakdown occurs is statistically distributed so that only statistical averages can be predicted.

The influence of the hot carriers on the threshold voltage and drive currents needs to be examined in detail for Si nanowire FETS. Present research is aimed at better understanding the nature of the electrical conduction during breakdown and the effect of the oxide breakdown on device performance. This chapter is divided into three sections with section one describing how the GAA Silicon nanowire structure seems to have possible novel solutions in the "more-than-moore" regime. Section two talks about the fabrication techniques of these nanowire FETs and section three discusses the current available performance of these devices by comparing critical FET parameters. The last two sections are devoted to the basic physics of hot carrier degradation mechanisms and the experimental setup used to assess the oxide reliability by observing the breakdown time during stress measuring.

7.2 Progression of Device Structure

The semiconductor industry has been so successful in providing continued system performance improvement year after year that the Semiconductor Industry Association (SIA) has been publishing roadmaps for semiconductor technology since 1992. These roadmaps represent a consensus outlook of industry trends, taking history as a guide. Feature-size scaling in CMOS technology has continued to follow the diktat of Moore's law for more than 40 years. The device scaling, however, appears to be reaching the end-of-the-technology roadmap. The limits most often cited are 1) quantum-mechanical tunneling of carriers through the thin gate oxide; 2) quantum-mechanical tunneling of carriers from source to drain and from drain to the body of the MOSFET; 3) control of the density and location of dopant atoms in the MOSFET channel and source/drain region to provide a high on-off current ratio and 4) the finite subthreshold slope.

Although the structure remains planar, the CMOS device architecture has undergone many a mutation to sustain the scaling pace. Implementation of LDD, lateral nonuniformity in channel doping, reduction in junction depth, and vertical

nonuniformity in well doping including pocket and halo implants are a few examples. In addition, the performance of scaled devices has been further improved by introducing stressors in the structure to improve mobility [25].

The increased doping in the channel which is needed to help the control of the gate over the channel vis-à-vis that of source and drain terminals leads to degraded performance. The electrostatics gets improved in multiple-gate structures as the gate influences the channel potential from more than one side and thus relaxes the demand on the doping. Figure 7.2.1 shows the evolution of multiple-gate transistors schematically in the order of increasing gate electrostatic control. Apparently, the Gate-All-Around (GAA) structure with its multiple gate control is the most effective for electrostatic control of the channel charge and is resistant to short-channel effects. The cylindrical geometry gives inverse logarithmic dependence of the gate capacitance on the channel diameter and thus, the gate length in these devices can be scaled with wire diameter without reducing the gate dielectric thickness. The nanowire technology has blossomed in the last 5-6 years and has many potential applications in nonvolatile memories, biochemical sensors and other circuits like ring oscillators [26]. Thus, the nanowire technology indicates feasibility of opening up newer application opportunities for Si technology.

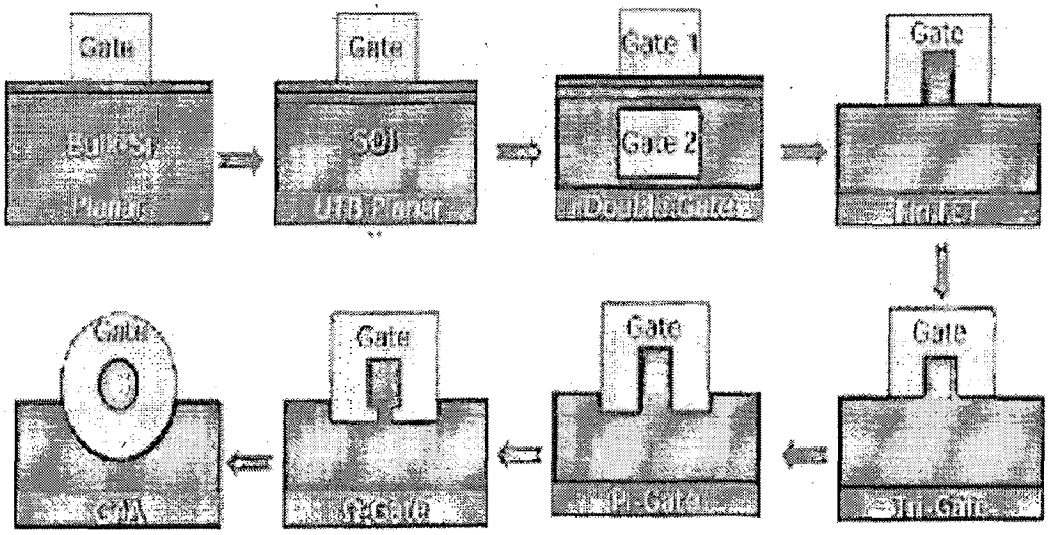


Fig7.2.1 Progression of device structure from single-gated planar to fully GAA NW MOSFETs.

7.3 GAA Nanowire Fabrication

The fabrication technology of NW channels can be broadly categorized into two groups, namely 1) the bottom–up approach and 2) the top–down approach. The bottom up approach is basically a non-lithographic method. Vapor-liquid-solid mechanism and molecular beam epitaxy can produce very thin nanowires. However, nanowires thus produced are randomly distributed and complicated processes are required to assemble them into functional devices [22]. In the top–down approach, the NWs are prepared in place utilizing lithography and etch processes, followed by trimming or stress-limited oxidation techniques. Integration of top–down-fabricated NWs in circuit functionality is straightforward, while the bottom–up approach faces a daunting challenge of assembling the wires into circuit functions. The silicon nanowires characterized by us were fabricated using the CMOS compatible top-down approach.

All approaches start with the silicon wafers as the substrate and involve lithography and etching processes for starting pattern definition. Different process steps such as hard mask trimming, etching in H_2 ambient, and/or stress limited oxidation processes follow to convert the silicon structures defined in the earlier step into NWs. The stress limited oxidation is usually carried out at low temperature to keep the grown oxide in stress to progressively slow down the oxidation rate, thus leaving a nanometer-scale silicon core embedded in the oxide. The self-limiting oxidation process is for Si-NW fabrication in lateral as well as vertical architectures. The wires have been carefully released by etching away the grown oxide in dilute HF. Fig 7.3.1 shows the SEM images of NWs fabricated using the lithographic pattern transfer and self-limiting oxidation processes.

The device and circuit fabrication is straightforward—very similar to the process steps used in standard CMOS flow. The gate oxide is grown or deposited on the NWs, followed by gate electrode deposition and definition. S/D implantation, metallization, followed by alloying completes the fabrication process similar to the planar FETs. The NW channel remains undoped, i.e., no intentional doping to adjust the threshold voltage V_{TH} or to control short-channel effects is introduced. After NW formation, the key process is gate definition in which the dry etching process requires a high selectivity to gate dielectric.

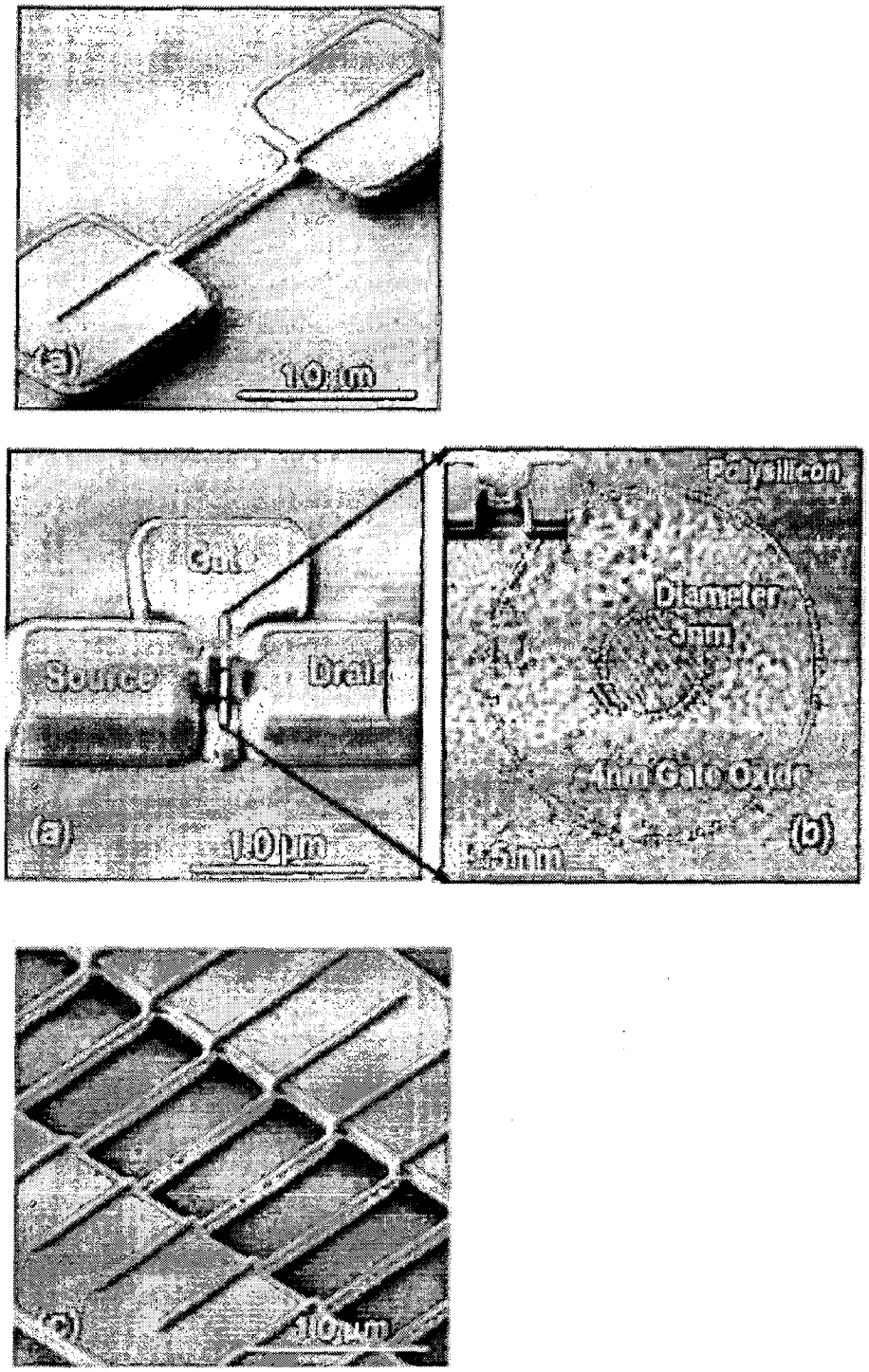


Fig.7.3.1 a) Single nanowire b) GAA NW transistor with gate length of 350 nm after gate patterning and (b) its TEM cross section in which ~3-nm-thick Si-NW surrounded by 4-nm SiO2 followed by poly-silicon is clearly seen. The inset shows the NW channel before poly-gate deposition.(c)multi fin mosfet. [1].

The device nomenclature used is as follows:

L_p- length of nanowire in μm

W_p-width of silicon before trimming down to a nanowire in μm

F_n-n is the number of fins between source and drain.

So for example, a typical device with a nomenclature Lp.4Wp15F1 meaning it has a length of 400nm, a width of 150μm and is a single wire GAA FET. The Electrical characterization and carrier transport results of these nanowires are well known [21] and will be discussed in the next section.

7.4 Current GAA Nanowire Performance

Most of the reported data on the I–V characteristics of GAA NW FETs show excellent gate control, near-ideal subthreshold behavior, high I_{ON}/I_{OFF} ratio, and high drive current. For instance, researchers have obtained I_{ON} values of 2.4 and 1.3 mA/μm, DIBL values of 8 and 13 mV/V, and SS of 60 and 65 mV/dec for NMOS and PMOS, respectively [21]. These results suggest a major advantage of these devices in relaxing the demands on gate oxide thickness for CMOS scaling. I_d-V_d curves show large linear region conductance and high output resistance in saturation region for these devices.

The I–V characteristics of these GAA Si-NW devices with 3-nm diameter are shown in Figure 7.4.1, where the current is normalized to diameter. Although it is a matter of debate, it is worth mentioning here that the typical trend in the contemporary NW literature is the normalization to diameter, which may be appropriate only with fully volume-inverted channels existing in the case of ultra narrow undoped wire channels.

Table 7.1 gives the comparative list of device electrical and structural parameters reported in the literature, along with the best reported FinFET performance [21].

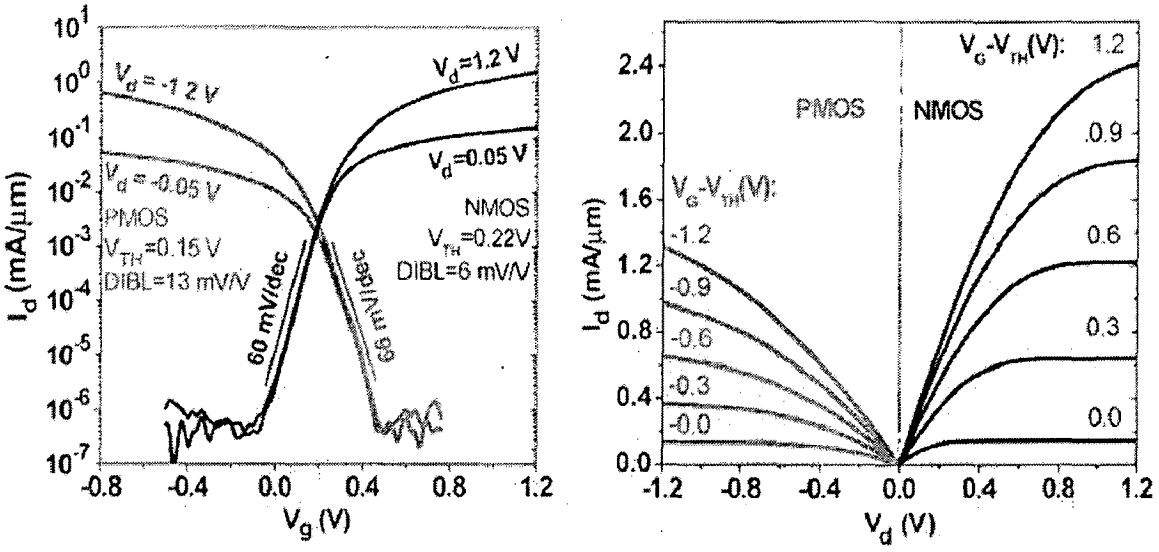


Fig.7.4.1 (a) Transfer characteristics of GAA n- and p-FETs (LG = 350 nm and TOX = 4 nm) showing near-ideal subthreshold swing indicating the excellent electrostatic control. (b) Drain current characteristics showing that high drive currents are possible in GAA FETs [21].

TABLE I
NW AND FINFET TRANSISTOR PERFORMANCE DATA

Device Type	Grown Nanowire		Top-Down Nanowire		Fin-FETs	
	N* [37]	P [38]	N [36]	P [27]	N [39]	P [39]
NW dia./Fin Width	20	15	10	8	25	25
Channel length (nm)	2000	40	8	15	40	40
Normalization method	diameter	diameter	diameter	diameter	W_{FIN}+2*H_{FIN}	W_{FIN}+2*H_{FIN}
I_{ON} (uA/um)	80	2100	3670	1940	1395	1140
I_{ON}/I_{OFF}	~10^4	~10^3	>10^6	>10^5	>10^4	>10^4
DIBL(mV/V)	-	-	28	43	89	101
SS(mV/dec)	300	140	73	71	76	82
V_{DD} (V)	5	-0.5	1	-1	1.1	-1.1

*I_{ON} data [37] is at V_{GS}=5V and V_{DS}=1V. W_{FIN} and H_{FIN} are is fin width and height respectively.

Table 7.1 Nanowire and FinFET transistor performance data

7.5 Basic Concept of Hot Electron Degradation

The reliability of SiO_2 in microelectronics, i.e., the ability of a thin film of this material to retain its insulating properties while subjected to high electric fields for many years has always been a concern and has been the subject of numerous publications over the last 35– 40 years since the realization that SiO_2 could be used as an insulating and passivating layer in silicon-based transistors. At least three defect generation mechanisms have been identified: The first two, impact ionization and anode hole injection occur at higher voltages and lead to hole trapping and hole-related defect generation. The lowest-energy process so far identified, which dominates at the voltages at which present MOSFETs operate, is the so-called "trap-creation" process attributed to hydrogen release from the anode [29].

As it is well known, there is a transition zone of a few tens of angstrom in the Si-SiO_2 interface. In the zone of non-chemical partition ratio of Si and O, some impurities and defects cause a large number of electron and hole traps as well as interface states. The reaction of the oxidation of silicon is expressed as follows:

$$Si\text{-}Si + 1/2O_2 = Si^* + [O\text{-}Si]^+ = Si\text{-}O\text{-}Si.$$

During the process of fabricating MOS structures, there are Si-OH, Si-O-Si and Si-Si bonds in the SiO_2-Si system, whether using the annealing process in H_2 or not, growing SiO_2 in the HCl gas, or using a dry-wet-dry process. Therefore, after hot carriers are injected into the SiO_2-Si system, the following reactions will be generated:

$Si_s\text{-}H + \text{hot e} = Si_s^* + H$

$Si_s\text{-}OH + \text{hot e} = (Si_sO)^* + H$

$Si_s\text{-}H + Si_o\text{-}O\text{-}Si_o + \text{hot e} = Si_s^* + Si_o^+ + \text{Si-OH}$

where the subscript in Sis means an interface, the one in the Si_o means inside the oxide.

So the interface states Si_s * and $(Si_sO)^*$ as well as the positively charged Si_o^+ in the SiO_2 have been formed. Hot electrons can break Si_s - Si_s and Si_o-O- Si_o bonds, and neutral positive charge traps Si_20, SiO and Si_2O_3 , as well as neutral negative charge traps Si_3-Si-O* and O_3-Si-O* are built up. These neutral traps can capture electrons and holes and therefore form negative charge centers and positive ones. The process described above is called charge trapping.

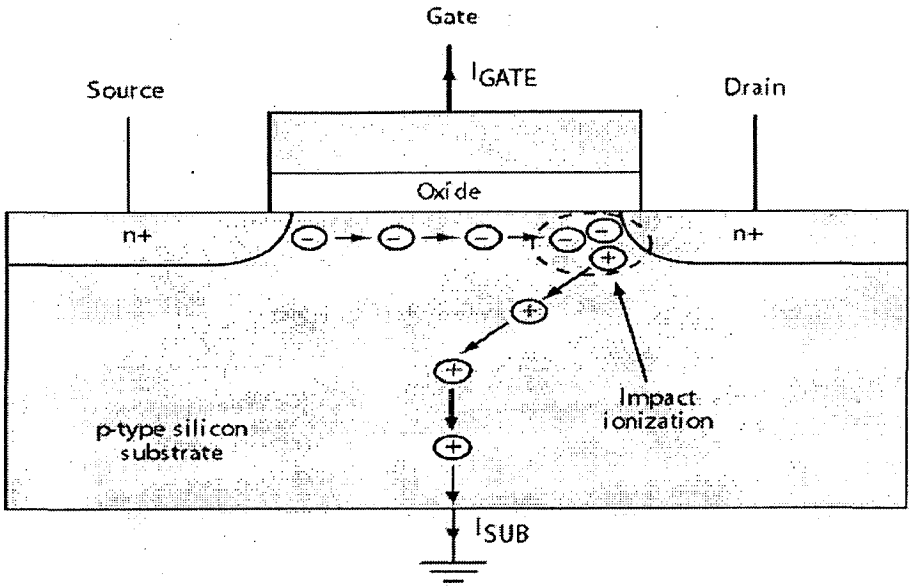


Fig 7.5.1 With reducing channel lengths the likelihood of impact ionization and the creation of hot carriers increase. These carriers have been proven to degrade transistor performance over time.

Although the generation of interface states and charge trapping in the oxide are caused by hot carriers, they are generated by two different processes. Interface states are considered to be generated by hot carriers at the surface that are energetic enough to jump over an interface potential barrier and to break an Si-O, Si-Si, Si-H or an Si-OH bond. In the case of charge trapping, hot carriers need to acquire enough kinetic energy to overcome the interface barrier (instead of breaking a bond), and be trapped in the SiO_2 by already existing traps (no trap generation). Therefore, the hot carrier energy generating interface state is bigger than that trapped into traps. In summary, after hot carriers are injected into SiO_2, the Si-SiO_2 system will undergo the following changes [23]:

Interface and interface defects + h or e = interface states,

Neutral traps in oxides + h or e = oxide charges $^{+/-}$

As the lateral electric field near the drain increases due to stress on the device, electron-hole pairs are generated by impact ionization. These generated electrons have energies far greater than the thermal-equilibrium value and are the hot holes. The hot holes are injected into the gate oxide via hot-carrier injection (HCI), resulting in the formation of dangling silicon bonds due to the breaking of silicon-hydrogen bonds and lead to the interface traps generation . The charge trapping in interface states

causes a shift in threshold voltage and the decrease of transconductance, which degrades the device properties over a period of time.

The procedure to characterize the device is by applying an electrical stress of 5V on the drain and grounding the source and body. This stress is applied at every multiple of 2 secs and after each stress the drain current is measured by sweeping the gate voltage from -1 to 3V. The stress time is as high as 90 minutes which comes to an effective stress time of 3 hrs. The experimental setup used to characterize the device is explained below.

7.6 Experiment Setup

This is a fully shielded setup with triax chuck and full Kelvin probes, designed to have very low noise floor and very high measurement sensitivity (<10fA) at room temperature [8]. Several routines have also been programmed to incorporate transistor-level and capacitor-level measurements like CV, IV, FN stress, Charge Pumping, NAND and NOR Flash memory reliability related measurements.

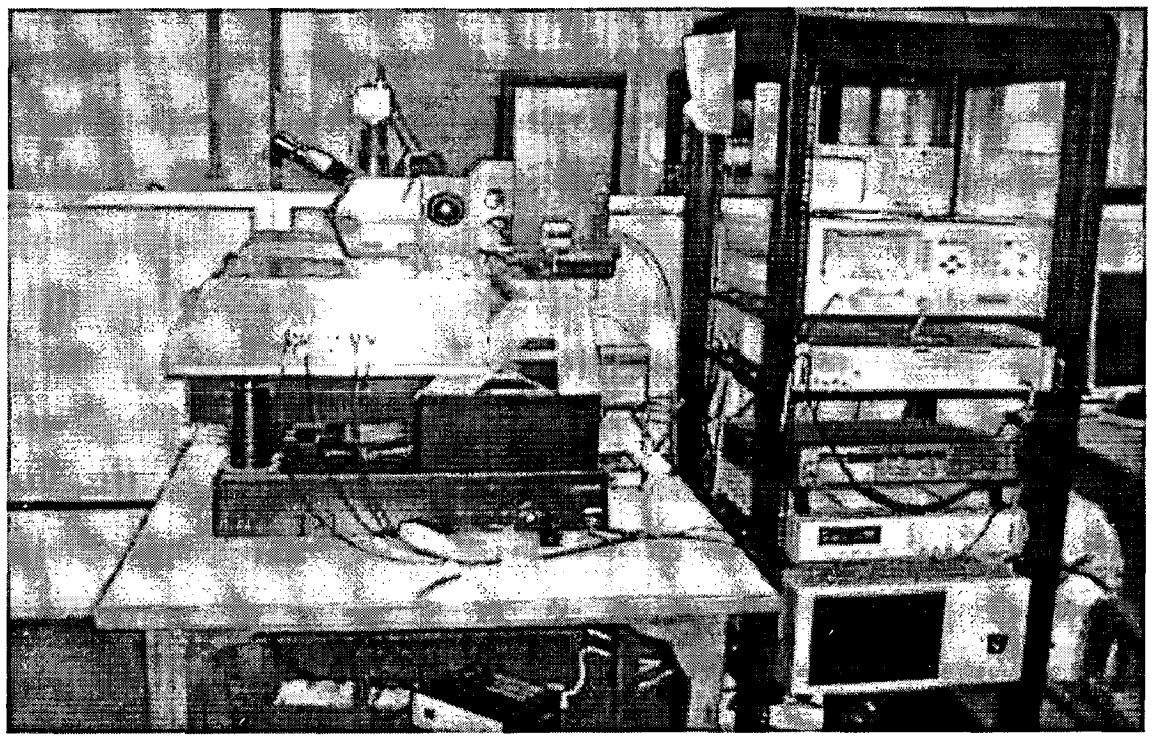


Fig 7.6.1 Entire experimental setup for reliability measurements

The instruments which are used in this setup are as follows:

Keithley 4200 SCS and KITE Software

This is a Semiconductor Characterization System with improved low current measurements on Nanoelectronic and Molecular Electronic devices. It has introduced Pulsing into Reliability Tests for Advanced CMOS Technologies and it enables to probe transistors at the contact level in Integrated Circuits. This is supported by Keithley Interactive Test Environment (KITE) software which is used to configure the SMU's that is to source or/and measure the voltage or/and current of a device terminal. It has the ability to sweep, bias, step or customized sourcing options.

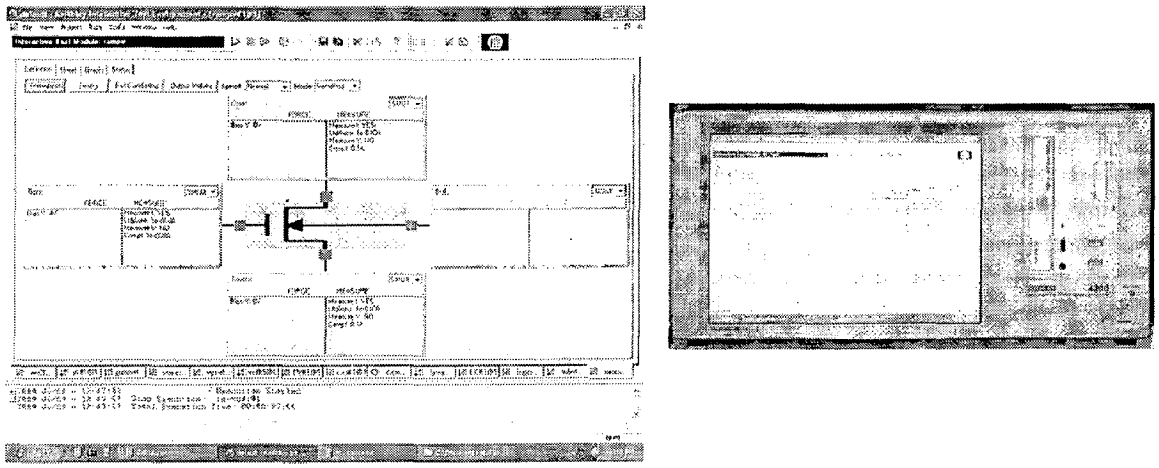


Fig 7.6.2 Keithley 4200 SCS and KITE software

Agilent 4284a LCR Meter

The 4284A precision LCR meter is a cost-effective solution for component and material measurement. The wide 20 Hz to 1 MHz test frequency range and superior test-signal performance allow this to test components to the most commonly-used test standards, such as IEC/MIL standards, and under conditions that simulate the intended application. Whether in research and development, production, quality assurance, or incoming inspection, the 4284A will meet all of your LCR meter test and measurement requirements.

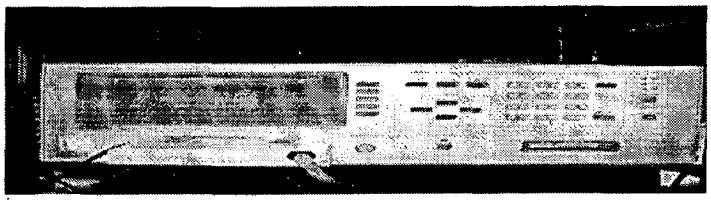


Fig 7.6.3 AGILENT 4284A LCR METER

Keithley 708a Switching Matrix

This setup consists of Model 708A Switching Matrix Card accessible from either front or rear panel. The Front panel has the relay status display and ""One touch"" programming- Control for up to 96 channels of 2-pole switching (expandable to 480).

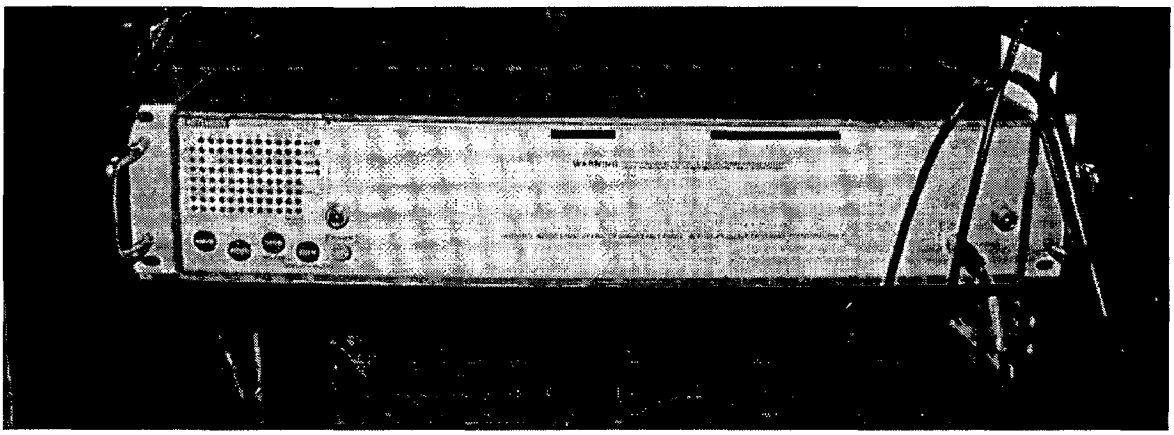


Fig7.6.4 (8 X 11) Programmable FPGA cross points array

Keithley 237 SMU

The Model 237 Source-Measure Unit (SMU) is a fully programmable instrument, capable of sourcing and measuring voltage or current simultaneously. This system is really four instruments in one: voltage source, current source, voltage measure, and current measure. As this is used for characterization of semiconductor devices, it is desirable to have the high measurement sensitivity of 10fA, 10μV. It can source and measure up to 1100V with standard and custom sweep capability including pulse. It has the ability to make 1000 source/measurements per second.

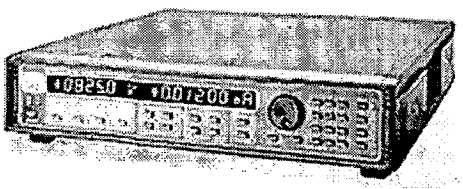


Fig7.6.5 KEITHLEY 237 SMU

SUSS MICROTEC Probe Station

This setup is used to physically connect the SMU's to the semiconductor device terminal contacts on wafer with specially designed probe tips made out of Tungsten. These probe tips are manually controlled using the probe manipulators, contacts are made by viewing the probe tips and the wafer placed on the chuck from the microscope provided under 2x or 10x optical zoom.

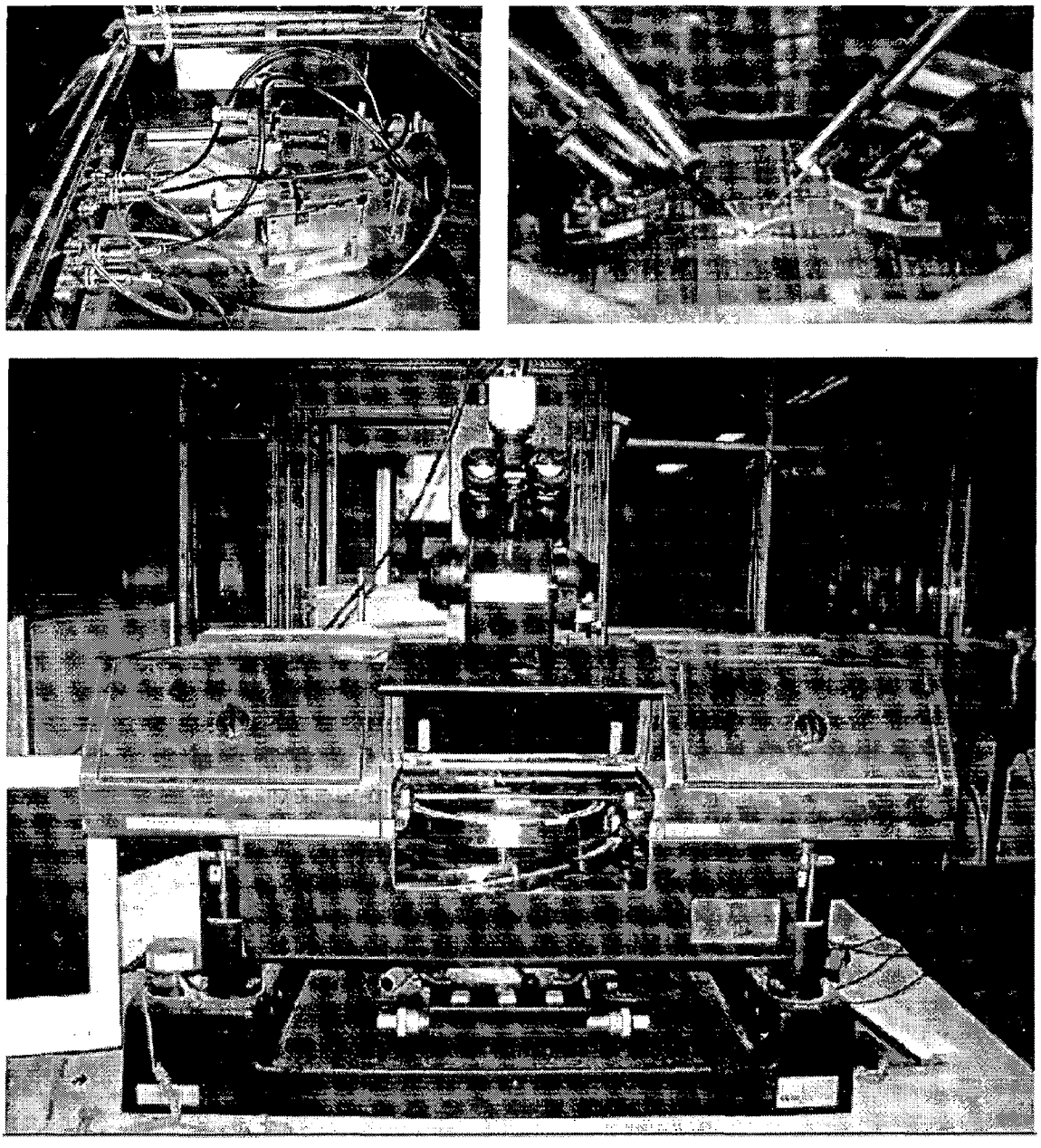


Fig7.6.6 SUSS Microtec Probe station manipulators and contact probes

7.7 Results

Figure 7.7.1shows the degradation of nMOSFET linear region characteristics due to hot carrier injection before and after stress [30]. The oxide thickness of the device was 40nm and the stress was applied for 90mins. The voltage values were V_{GS} = 6V and V_{DS} = 7.5V. We see that due to injection of hot carriers the threshold voltage of the device increases.

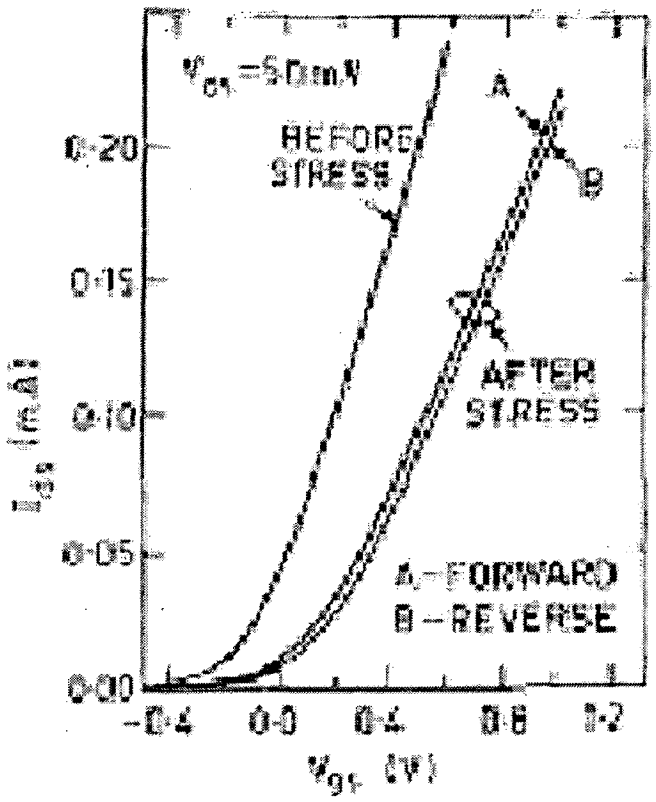


Fig 7.7.1 Curves showing the degradation of nMOSFET characteristics due to applied stress on the gate terminal [30].

The experimental results obtained on lateral silicon nanowires are shown below.The device dimensions are LP4 WP15 F1. It is a common practice to characterize device degradation by measuring shifts in V_{th} , change in transconductance $\Delta gm/gm$ or by measuring the drain current $\Delta I_D / I_D$ after the device is stressed.

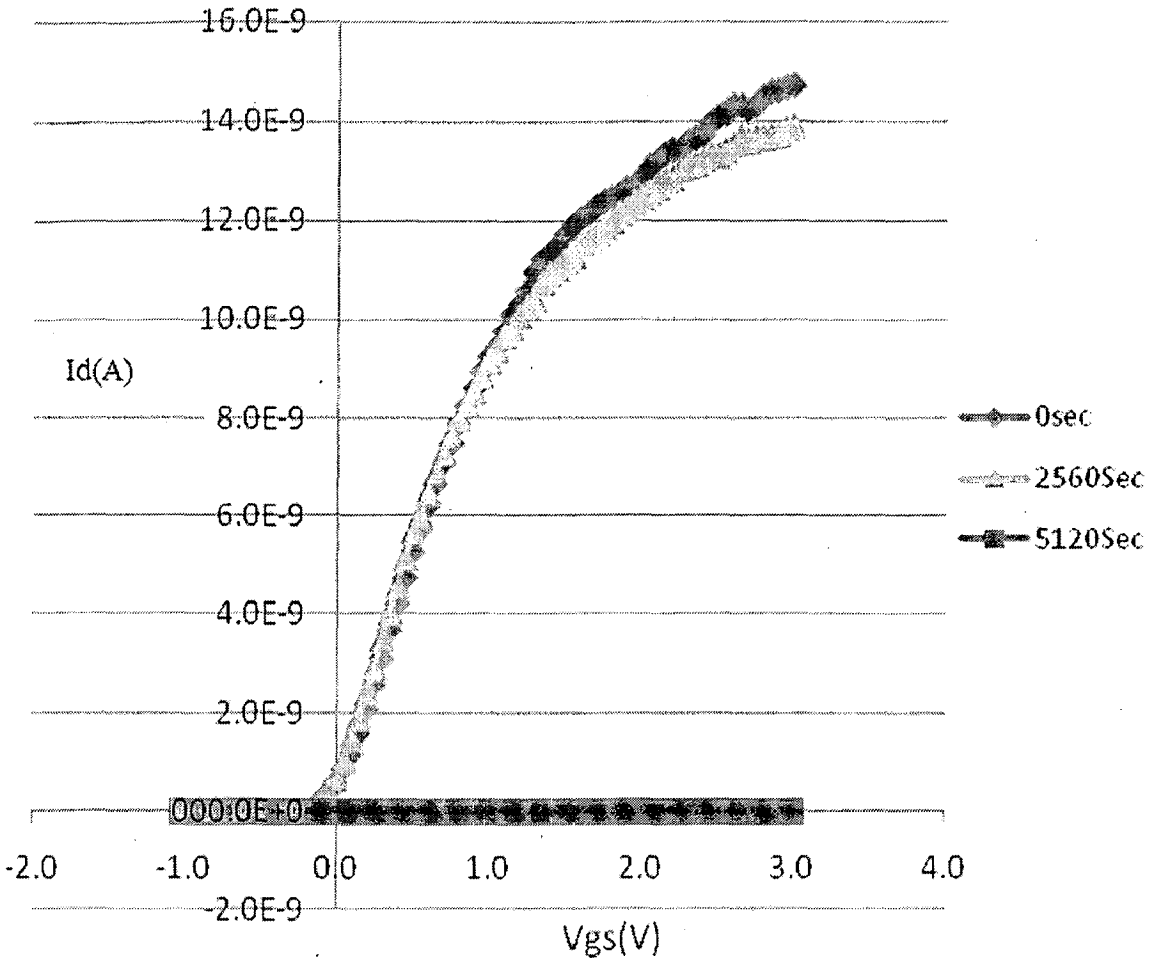


Fig 7.7.2 Experimental results obtained for lateral GAA silicon nanowire nMOSFETs.

7.8 Conclusions

A study on the silicon GAA nanowire MOSFETS is presented through their evolution, effective performance and CMOS compatible top-down fabrication method. With reducing dimensions the need to study the hot carrier degradation of these devices is brought to surface. The physics of hot injection mechanism is explained and their effect on device reliability measurements is pointed out. The initial results show a shift in threshold voltage and a complete breakdown of the device is seen after 90 minutes.

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APPENDIX A: OPTICAL PROPERTIES OF SILICON

The optical properties of silicon are measured at 300 K [16]. While a wide range of wavelengths is given here, silicon solar cells typical only operate from 400 to 1100 nm. Silicon is an indirect bandgap semiconductor so there is a long tail in absorption out to long wavelengths. The data is graphed on a log scale. Absorption coefficient determines how far of a particular wavelength can penetrate before it is absorbed. Typically we need high absorption coefficient so that most of the light is absorbed very close to the surface and within the depletion region width.

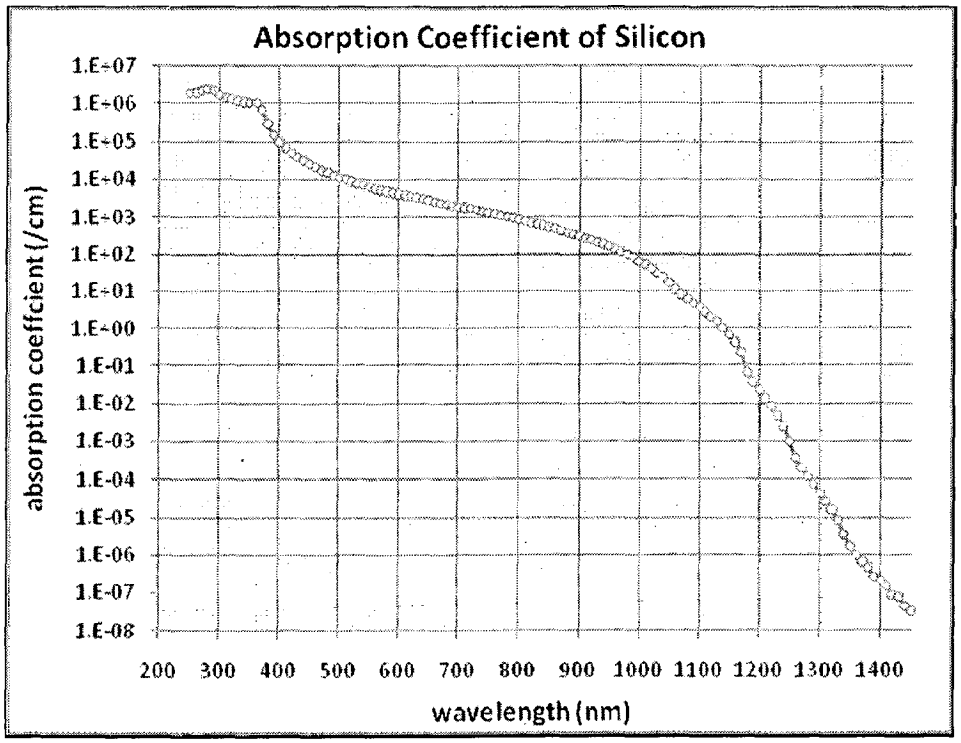

Figure A1 Absorption coefficient of silicon in cm^{-1} as a function of the wavelength

The absorption depth is the inverse of the absorption coefficient. An absorption depth of, for example, 1 μm means that the light intensity has fallen to 36 % (1/e) of its original value at 1μm. Figure A2 shows absorption depth versus wavelength in centimeters and meters. Figure A3 shows the real and imaginary components of the refractive index of silicon at 300K. The complex refractive index of silicon is given as,

Refractive index = n – ik, where n is the real component of refractive index and ḱ is the extinction coefficient.

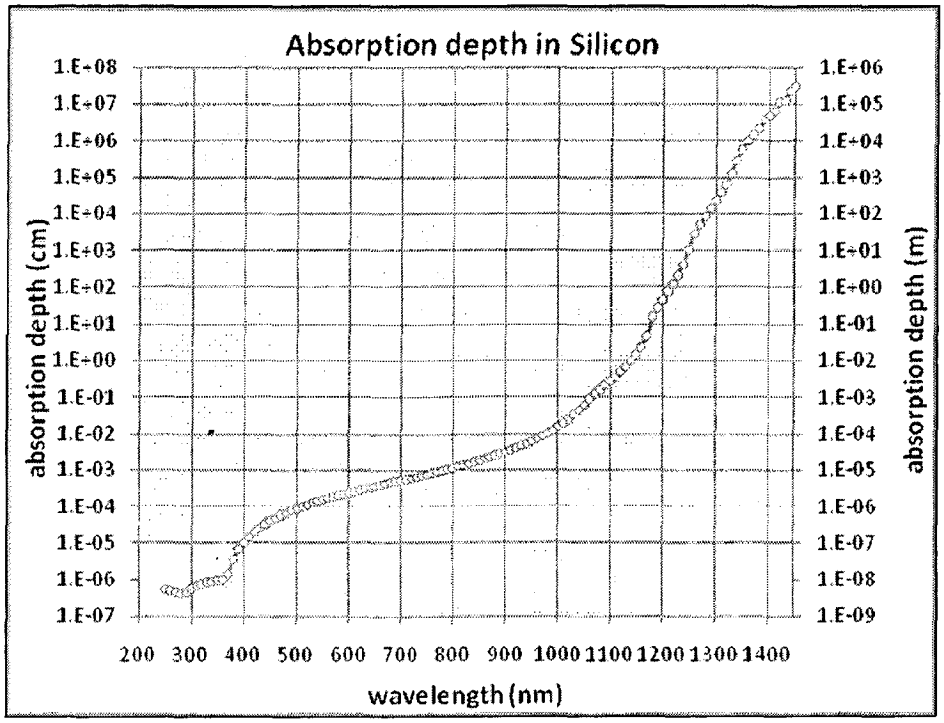

Figure A2 Absorption depth of silicon as a function of the wavelength

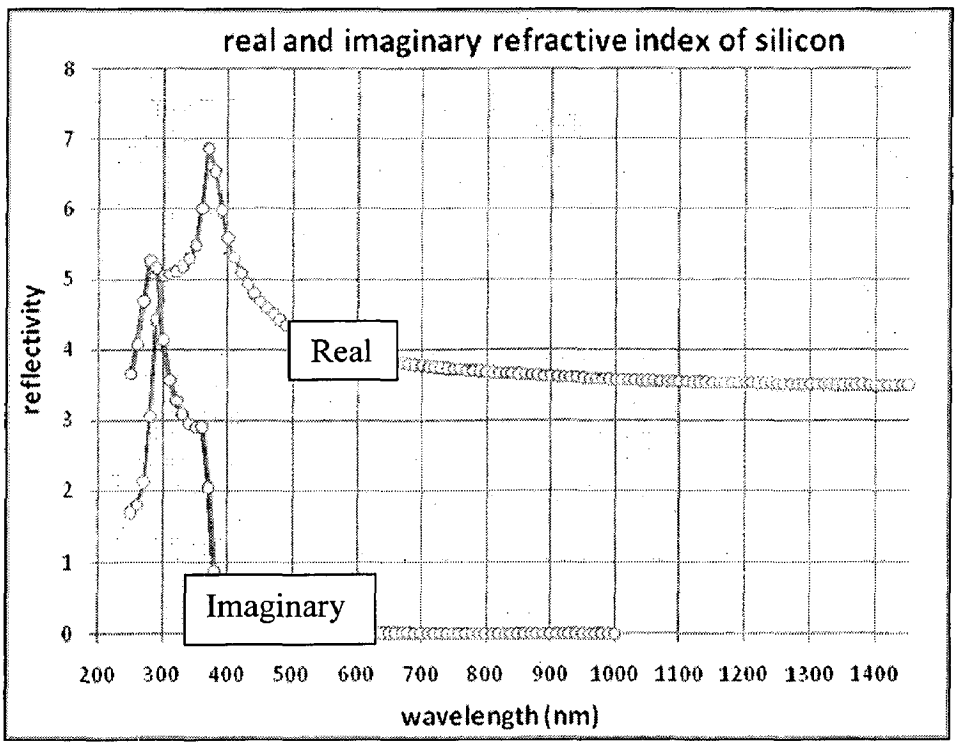

Figure A3 Real and (negative) imaginary components of the refractive index for silicon

APPENDIX B: DERIVATION FOR BASE, EMITTER AND FINGER RESISTANCE

The metallic top contacts are necessary to collect the current generated by a solar cell. "Busbars" are connected directly to the external leads, while "fingers" are finer areas of metallization which collect current for delivery to the busbars. The busbars connect the fingers together and pass the generated current to the external electrical contacts. The key design trade-off in top contact design is the balance between the increased resistive losses associated with a widely spaced grid and the increased reflection caused by a high fraction of metal coverage of the top surface. Figure B1 shows the various resistive components in the cell and also the directions of idealized current flows.

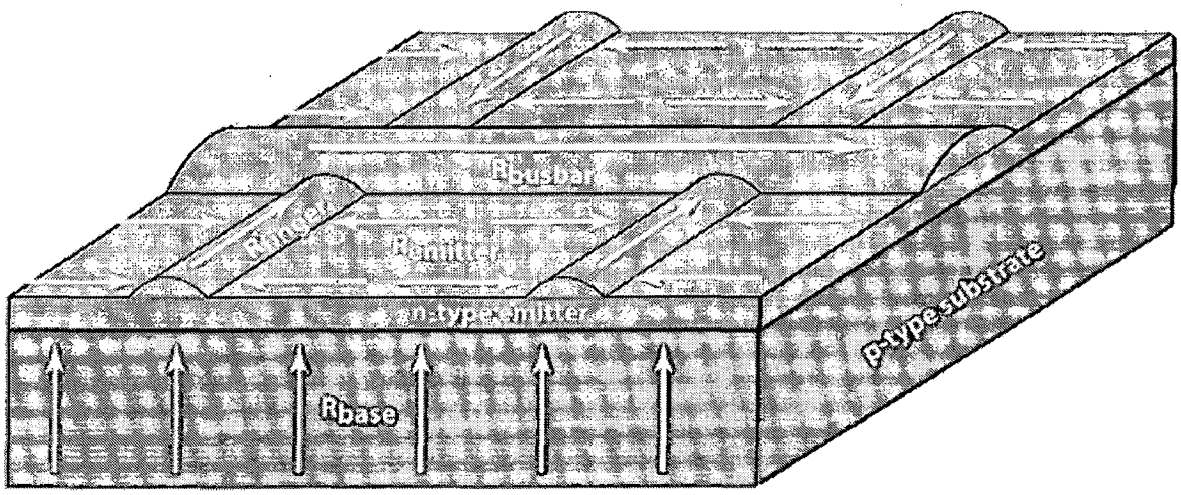

Figure B1. Resistive components and current flows in a solar cell. [4]

Base Resistance:

The optically generated current typically flows perpendicular to the cell surface from the bulk of the cell and then laterally through the top doped layer until it is collected at a top surface contact. The resistance and current of the base is assumed to be constant. The resistance to the current of the bulk component of the cell, or the "bulk resistance", R_b is defined as:

$$R_b = \frac{\rho l}{A} = \frac{\rho_b W}{A} \qquad (B.1)$$

taking into account the thickness of the material. Where:

l = length of conducting (resistive) path

ρ_b = "bulk resistivity" (inverse of conductivity) of the bulk cell material (0.5 - 5.0 Ω cm for a typical silicon solar cell)

A = cell area, and

w = width of bulk region of cell.

Emitter Resistance:

Based on the sheet resistivity (ρ_Δ), the power loss due to the emitter resistance can be calculated as a function of finger spacing in the top contact. However, the distance that current flows in the emitter is not constant. Current can be collected from the base close to the finger and, therefore, has only a short distance to flow to the finger. Alternatively, if the current enters the emitter between the fingers, then the length of the resistive path seen by such a carrier is half the grid spacing.

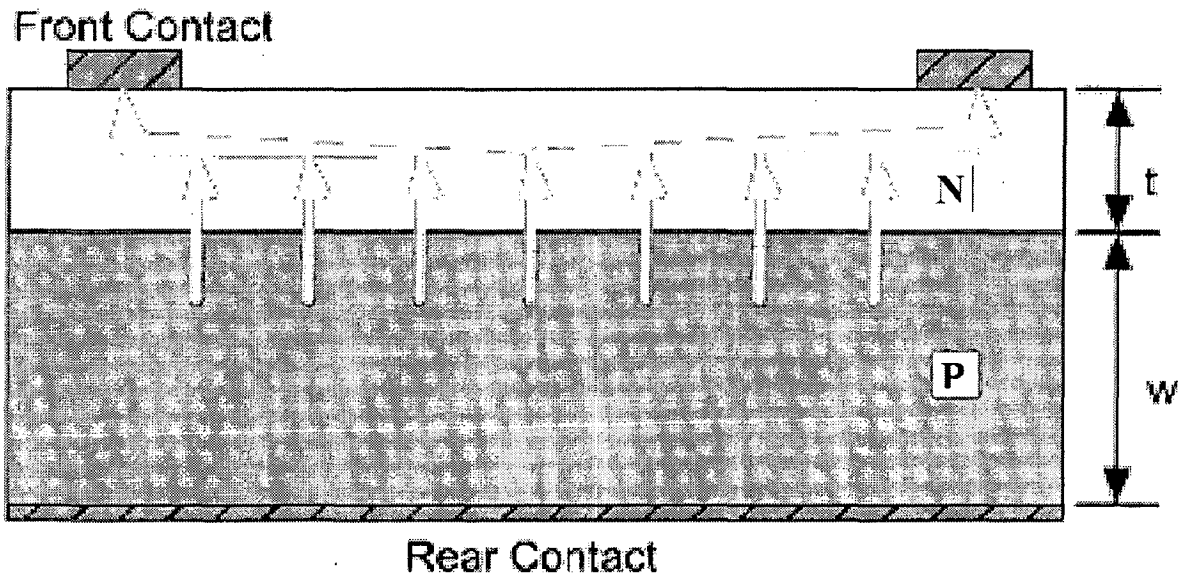

Figure B2. Idealized current flow from point of generation to external contact in a solar cell. The emitter is typically much thinner than shown in the diagram.

The incremental power loss in the section dy is given by:

$$dP_{loss} = I^2 \, dR \qquad (B.2)$$

The differential resistance is given by

$$dR = \frac{\rho}{b} dy$$

where

ρ is the sheet resistivity in Ω/Δ

b is the distance along the finger; and

y the distance between two grid fingers as shown below in Figure B3.

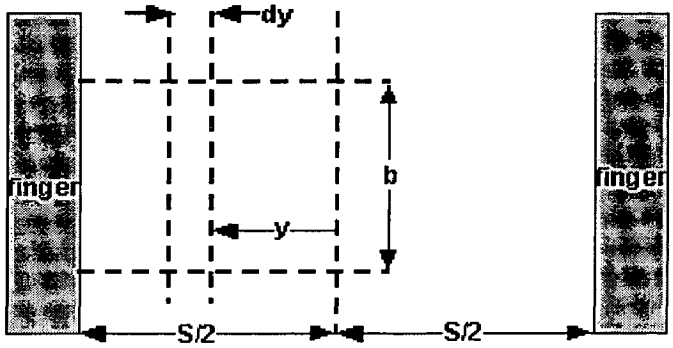

Figure B3. Dimensions needed for calculating power loss due to the lateral resistance of the top layer.

The current also depends on y and $I(y)$ is the lateral current flow, which is zero at the midpoint between grating lines and increases linearly to its maximum at the grating line, under uniform illumination. The equation for the current is:

$$I(y)=Jby$$

where

J is the current density;

b is the distance along the finger; and

y the distance between two grid fingers as shown above.

The total power loss is therefore:

$$P_{loss}=\int I(y)^2\,dR=\int_0^{\frac{S}{2}}\frac{J^2b^2y^2\rho_\Delta}{b}dy=\frac{J^2b\rho_\Delta S^3}{24} \qquad (B.3)$$

where S is the spacing between grid lines.

At the maximum power point, the generated power is:

$$P_{gen}=J_{MP}\,b\frac{S}{2}V_{MP}$$

The fractional power loss is given by:

$$P_{\%\,lost}=\frac{P_{loss}}{P_{gen}}=\frac{\rho_\Delta S^2 J_{MP}}{12V_{MP}} \qquad (B.4)$$

Hence, the minimum spacing for the top contact grid can be calculated. For example, for a typical silicon solar cell where ρ= 40 Ω/Δ, J_{MP} = 30 mA/cm^2, V_{MP} = 450 mV, to have a power loss in the emitter of less than 4 %, the finger spacing should be less than 4 mm.

Finger Resistance:

To provide higher conductivity the top of a cell has a series of regularly spaced fingers. While tapered fingers theoretically provide lower losses technology limitations mean that fingers are usually uniform in width. The resistive loss in a finger is calculated as below.

Refer to Figure B4 to derive an expression for the power loss due to finger resistance. Consider an element dx at a distance x from the end of the finger. The current through the element dx is given as $x J_{MP} S_f$, where J_{MP} is the current at maximum power point and S_f is the finger spacing.

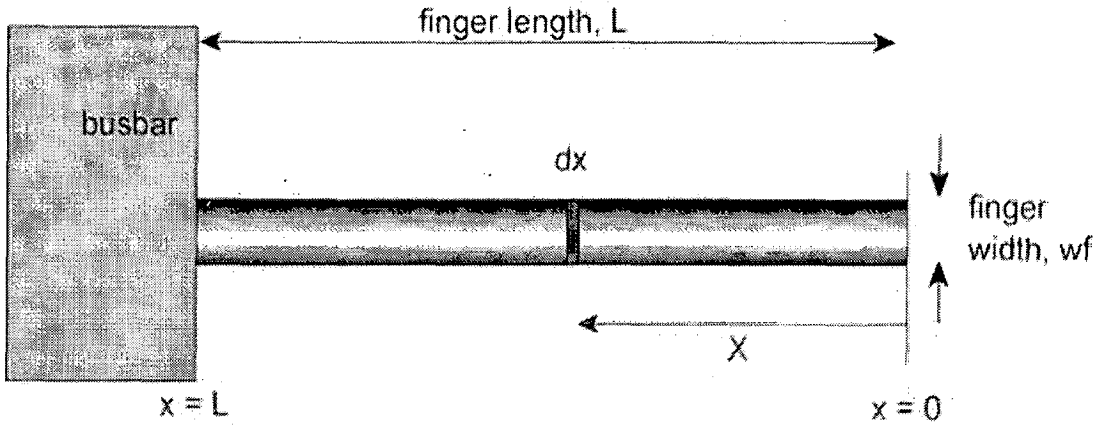

Figure B4 Calculation of the power loss in a single finger. The width is assumed constant and it is assumed that the current is uniformly generated and that it flows perpendicularly into the finger, i.e., no current flow directly into the busbar.

The resistance of the element dx is given as

$\frac{dx \rho_f}{w_f d_f}$, where w_f is the finger width, d_f is the finger depth (or height) and ρ_f is the effective resistivity of the metal.

The power loss in the element dx is

$$I^2 R = \frac{d\,x\,\rho_f}{w_f\,d_f}(x J_{MP} S_f)^2 \qquad (B.5)$$

Integrating x from 0 to L gives the power loss in the finger:

$$\int_0^L \frac{(x J_{MP} S_f)^2 \rho_f}{w_f\,d_f} dx = \frac{1}{3} L^3 J_{MP}^2 S_f^2 \frac{\rho_f}{w_f\,d_f} \qquad (B.6)$$

APPENDIX C: STANDARD AM1.5G SUNLIGHT SPECTRA

Wavelength (nm)	AM1.5G Spectrum $W*m^{-2}*nm^{-1}$
0.38	7.125
0.39	7.207
0.4	10.131
0.41	11.582
0.42	11.84
0.43	10.719
0.44	13.02
0.45	15.26
0.46	15.996
0.47	15.81
0.48	16.283
0.49	15.392
0.5	15.487
0.51	15.865
0.52	14.849
0.53	15.724
0.54	15.507
0.55	15.615
0.56	15.315
0.57	15.015
0.58	14.485
0.59	13.955
0.6	14.404
0.61	14.853
0.62	14.597
0.63	14.341
0.64	14.27
0.65	14.199
0.66	14.061
0.67	13.923
0.68	12.612
0.69	11.3
0.7	12.234
0.71	13.167
0.72	10.206
0.73	11.035
0.74	12.112
0.75	11.974
0.76	9.093
0.77	10.508
0.78	11.311
0.79	11.064
0.8	10.816
0.81	9.364
0.82	8.158
0.83	8.911
0.84	9.599
0.85	9.694
0.86	9.789
0.87	9.561
0.88	9.332
0.89	8.593
0.9	7.854
0.91	7.08
0.92	6.789
0.93	4.036
0.94	2.734
0.95	3.387
0.96	4.641
0.97	5.667
0.98	6.464
0.99	7.208
1	7.389
1.01	7.268
1.02	7.147
1.03	7.026
1.04	6.905
1.05	6.728
1.06	6.552
1.07	6.375
1.08	5.625
1.09	4.876
1.1	4.126
1.11	2.608
1.12	2.306
1.13	1.891
1.14	1.581
1.15	2.442
1.16	3.304
1.17	3.963
1.18	4.6
1.19	4.418
1.2	4.236

Source: http://rredc.nrel.gov/solar/

APPENDIX D: BEST RESEARCH-CELL EFFICIENCIES

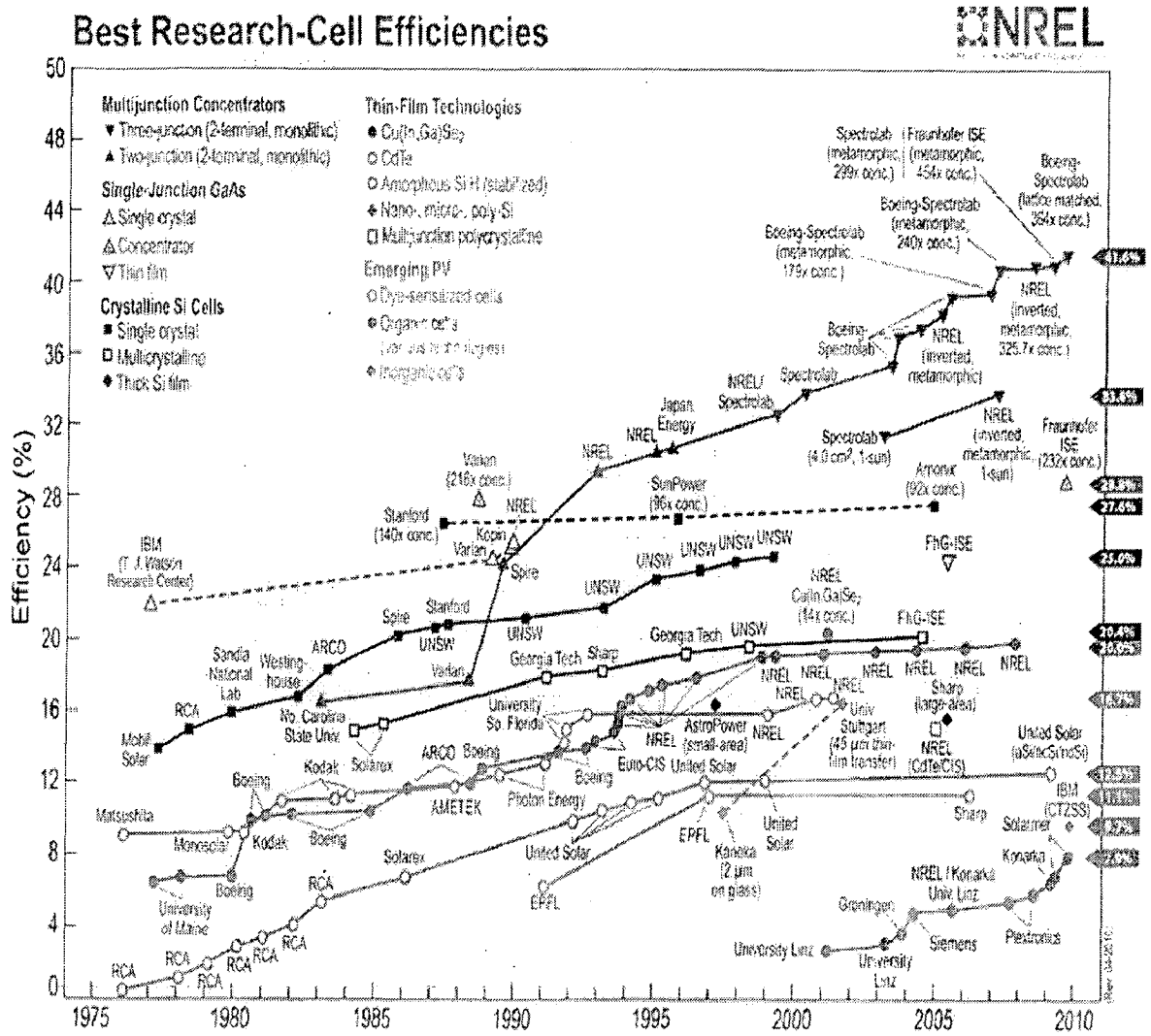

Figure D1 Best Research-cell efficiencies

PUBLICATIONS

[1] Communicated a paper entitled "**TCAD study on the influence of intrinsic electric fields on the performance of a crystalline silicon solar cell**" to International Conference on Optoelectronics and Photonics 2010 to be held at IIT Guwahati from 11^{th}-13^{th} December, 2010.