ROBUST ANALOG VLSI CIRCUIT DESIGN

A DISSERTATION

Submitted in partial fulfillment of the requirements for the award of the degree of

MASTER OF TECHNOLOGY

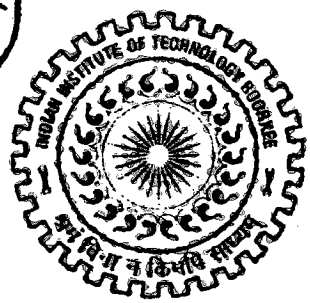
in

ELECTRONICS AND COMMUNICATION ENGINEERING

(With Specialization in Semiconductor Devices & VLSI Technology (SDVT))

By

ATUL KUMAR



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JUNE, 2010

CANDIDATE'S DECLARATION

hereby declare that the work presented in this dissertation report entitled, **"ROBUST ANALOG VLSI CIRCUIT DESIGN"** towards the partial fulfillment of the requirements for the award of **Master of Technology in Electronics and Communication Engineering** with specialization in **Semiconductor Devices & VLSI Technology,** submitted in the Department of Electronics and Computer Engineering, Indian Institute of Technology Roorkee, is an authentic record of my own work carried out during the period from July 2009 to June 2010, under the guidance of **Dr. Anand Bulusu** and **Dr. Sudeb Dasgupta,** Department of Electronics and Computer Engineering, Indian Institute of Technology Roorkee.

The content of this dissertation has not been previously submitted for examination as part of any academic qualifications.

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I hereby declare that the work presented in this dissertation titled ***"ROBUST ANALOG VLSI CIRCUIT DESIGN"*** in partial fulfillment of the requirements for the award of the degree of **Master of Technology in Electronics and Communication Engineering** with specialization in **VLSI**, submitted in the Department of Electronics and Computer Engineering , Indian Institute of Technology Roorkee, is an authentic record of my own work carried out during the period from *January,2010* to *June,2010* under the guidance of ***Mr. Shivraj G. Dharne****, Intel Technology India*

The matter embodied in this dissertation has not been submitted by me for award of any other degree or diploma.

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ABSTRACT

Variation in transistor characteristics is increasing as CMOS transistors are scaled to nanometer feature sizes. In analog integrated circuits, the variability of identically designed devices plays an important role since it directly affects the attainable precision.

An operational amplifier is one of the most basic components in analog integrated circuit design. Random device mismatch creates input referred offset voltage in the op amp which limits the overall performance of the system in many cases. In this work, chopper stabilization is applied to the amplifier to reduce the input referred offset voltage. The chopper stabilized op amp is used to build a bandgap reference voltage. In simulations, chopper stabilization improved the accuracy of the bandgap reference voltage from +/- 11.62% (3σ variation due to random mismatch only) to less than +/- 0.02%.

All the circuits in this work are implemented using Intel's 32 nm CMOS process.

CONTENTS

Chapter 1

Introduction and Process Variation Overview

1.1 Introduction

The impact of Process, Voltage and Temperature variations have been sharply increasing as CMOS transistors are scaled to nanometer feature size. As the silicon geometries are shrinking

- The IC manufacturing process has more variations in it.
- The power supply voltage is reduced, decreasing the margin available to the designer, making voltage variations a significant part of the overall design.
- The operating frequency is increasing, which results in high junction temperature and within-die temperature variations.

A lot of research effort is currently going on to characterize the various sources of variation and to study its impact on circuit behavior. To develop layout and circuit design techniques to reduce the impact of variability, a designer needs to understand the various sources of variation to be able to anticipate the amount of variation and then design the circuit to make it variation aware.

A design technique used to mitigate the impact of random variations is chopping. In chopping, the inputs to a differential amplifier are swapped, or chopped, under the control of a clock signal. The same clock signal is used to swap the outputs, and then the results are low pass filtered.

1.2 Organization of Thesis

The remainder of this chapter gives an overview of the process variation. Chapter two describes the theory of chopping and gain boosting. Chapter three describes the design of chopper stabilized op amp. It contains the design of amplifier, biasing, chopping blocks, non overlapping clock generator as well as the simulated results. Chapter four describes the design of bandgap voltage reference using the chopper stabilized op amp. The bandgap reference voltage is

simulated with chopping on and off, to see the effect of chopping on random variations. Conclusions are drawn in chapter five.

1.3 Process Variations

Process variations can be divided into two main categories: systematic variations and random variations. Systematic variations can be characterized with a suitable quantitative model, relating the variations to the design parameters. Examples include the impact of gate poly pitch on gate length due to optical proximity effects, stress effects, orientation effects, etc. Random variations cannot be described using deterministic models. Therefore, statistical design approaches are needed for them. Examples include Line Edge Roughness, Random Dopant Fluctuation, etc.

1.3.1 Systematic Variations

Systematic variation is the difference in the electrical characteristics of two transistors with identical width and length (*W/L*), where there is a clearly identifiable difference in either the device layout or the layout neighborhood. Examples include Well Proximity Effect, STI Stress Effect, etc. The systematic variations can be characterized using suitable quantitative model relating the variation to design practice. Because we are able to describe these phenomena, we treat them as systematic in nature, and we will refer to them as systematic variability.

1.3.1.1 Well Proximity Effect

In modern CMOS technology, ion implantation is used to form deep retro gate well profiles that are needed for latch-up protection and suppression of lateral punch-through. During ion-implantation, high energetic ions can scatter laterally from the edge of the photo resist (which is used to mark the well boundary). These laterally scattered ions become embodied in the silicon surface, as a result of which the surface concentration varies with the distance from the well edge over a range of about 1 um or more. Because of the variation in the surface concentration of the well, threshold voltage and other electrical characteristics of the MOSFET transistor vary with the distance from the well edge. This phenomenon is known as the Well Proximity Effect (WPE).

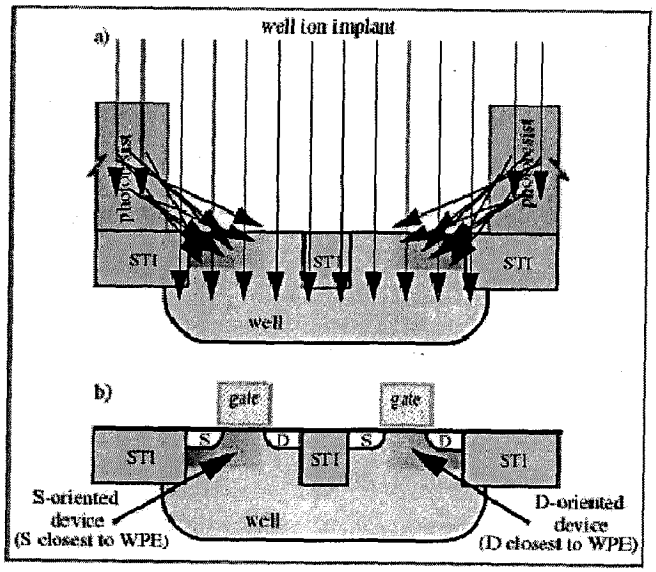


Figure 1.1: A depiction of the WPE [1]

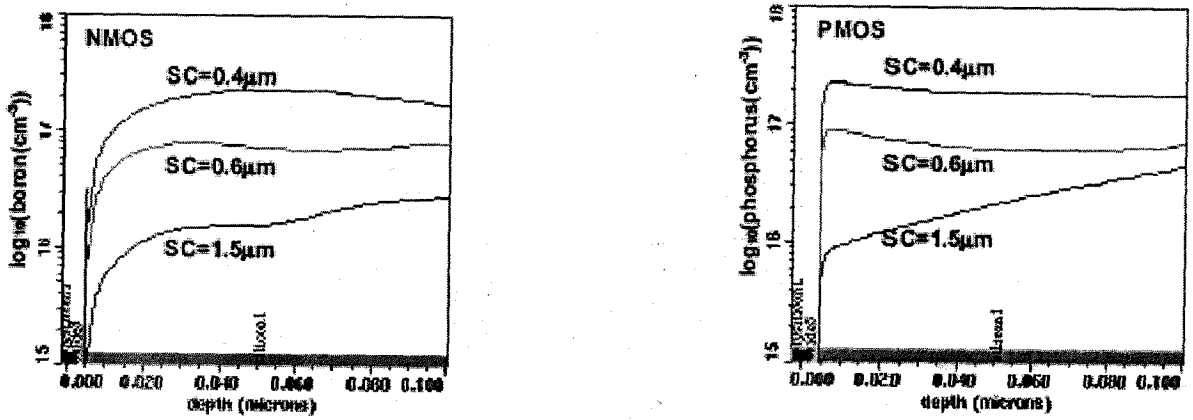


Figure 1.2: TCAD simulated vertical channel dopant profile versus well gate edge distance, SC [2]

Figure 1.2 shows the TCAD simulation results, as the gate edge is moving closer to well edge the concentration of dopants is increasing confirming Well Proximity Effect.

The impact of Well Proximity Effect (WPE) on current mirror has been considered in [1].

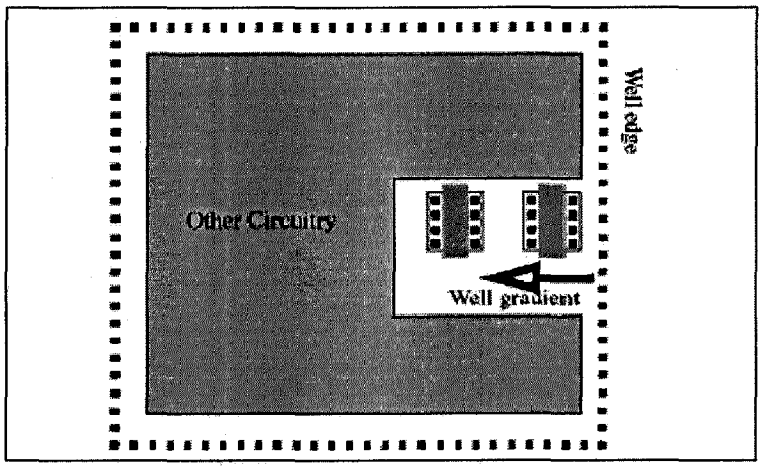


Figure 1.3: An example layout for a matched device application near a single well edge. [1]

The output current of a current mirror located near the well edge is compared with the output current of a current mirror which far from the edge.

The output of the current mirror is shown in figure 1.4 with varying well edge distances. The curve cross the 0% when the drain bias of reference and output transistor is equal. It is clear from the curves that the current offset is strongly dependent on the location of the output transistor with respect to the well edge. As the output transistor moves closer to well edge, the offset current also increases.

A simple solution to Well Proximity Effect could be to increase the active to well spacing but it will consume more chip area. The problem cannon be solved by simulation also because the effect comes into picture after the layout stage and it needs to be accounted for in the schematic entry stage. Cost, yield and competitive pressure push designers to deal with WPE in some capacity and without the understanding of the effect, the designer is completely blind to this potential source of circuit failure.

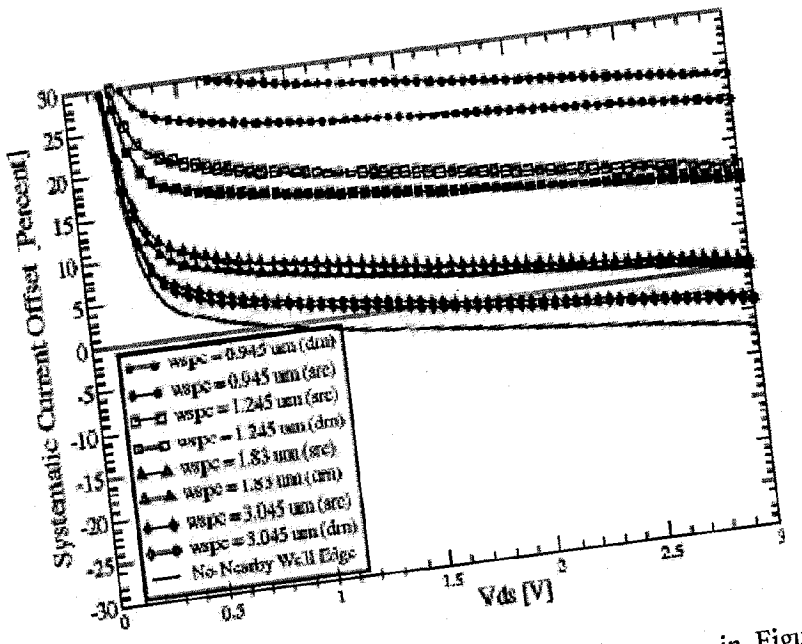


Figure 1.4: Current mirror output offset for a layout configuration as in Figure 1.3 and a reference device with negligible well-proximity shift. [1]

1.3.1.2 STI Stress

Shallow Trench Isolation (STI) is the most dominant isolation technique for deep submicron technologies, favored for its excellent latch-up immunity, low junction capacitance and sharp vertical edges. The key steps of the STI process involve etching a pattern of trenches in the silicon, depositing one or more dielectric (such as SiO_2) to fill the trenches and removing the excess dielectric using a technique such as chemical mechanical planarization.

A large amount of compressive mechanical stress is produced at the STI edge. This compressive stress results from the mismatch in the thermal expansion coefficients of different materials and the volume expansion of silicon dioxide. Mechanical stress in the device affects many device characteristics for example- carrier mobility and dopant diffusion.

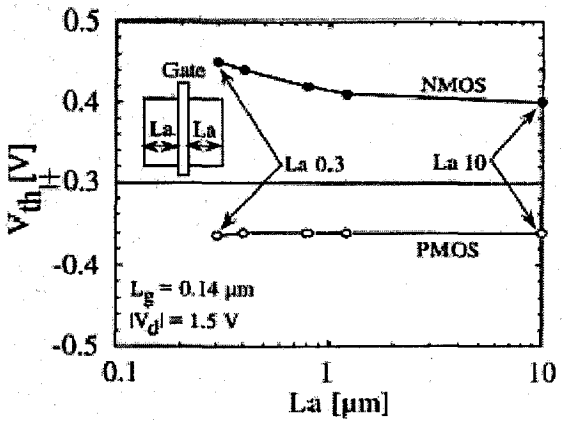


Figure 1.5: Dependence of threshold voltage on active-area length (L_a) in 0.18-μm CMOS technology. Here, L and W are constant (Lg = 0.14 μm and Wg = 15 μm) with $L_a$variation.[3]

The effect of STI induced stress on the device characteristics is highly layout dependent and it is different for NMOS and PMOS. Variation of the threshold voltage with active area layout is shown in figure 1.5. The STI induced stress reduces the diffusion of boron while it has no effect on the diffusion of phosphorus. As a result of the reduced boron diffusion, its concentration increases at the channel edges, because of which the threshold voltage of NMOS increases as the gate edge is moving closer to the trench edge. The threshold voltage of PMOS is not effected because the diffusion of phosphorus is not effected by the STI induced stress.

Plots of device transconductane(gm) with respect to gate voltage for NMOS and PMOS are shown in figure 1.6 . For NMOS, the transconductance is higher for the device which is away from the trench egde (i.e La = 10um) whereas for PMOS, the transconductance is higher for the device which is closer to the trench egde (i.e La = 0.3um). This result is consistent with the fact that bi-axial compressive stress enhances hole mobility and degrades electron mobility.

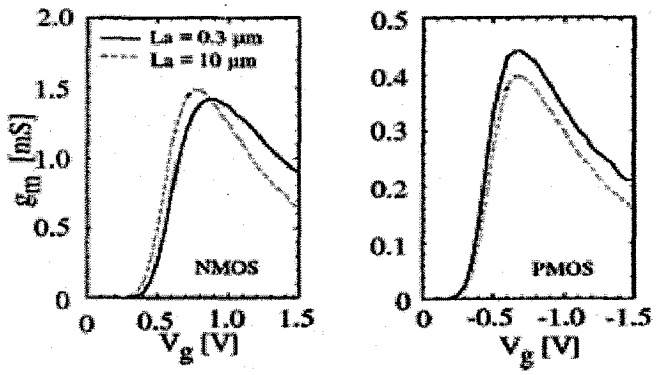
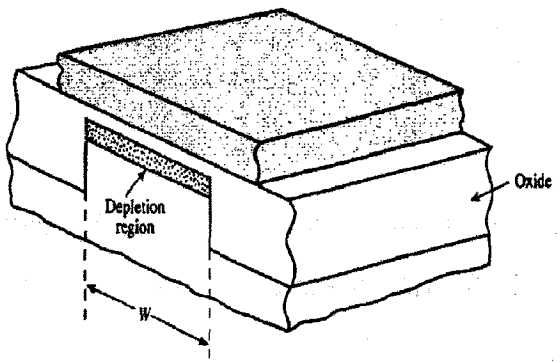


Figure 1.6: g_m-V_g curve of transistors with L_a = 0.3 μm and L_a = 10 μm in linear region. Here, L_g= 0.14 μm, W_g= 15 μm, and $|V_d|$ = 0.05 V. [3]

1.3.1.3 Inverse Narrow Width Effect

In the LOCOS (local oxidation of silicon) isolation scheme, the depletion region is not limited to under the oxide only because of the fringing field emanating from the gate charge. So effectively the gate is responsible for depleting more area than required and thus the threshold voltage increases for device with narrow width (i.e. when the extra part of depletion region becomes a large percentage of the total).



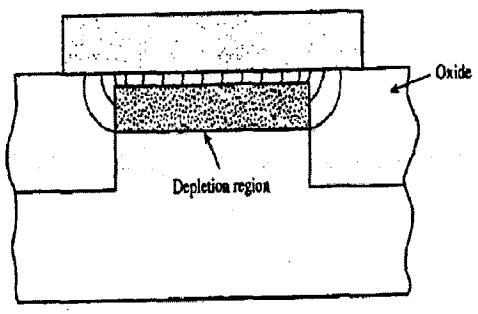


Figure 1.7(left): Cross section along the width of a STI MOSFET device [4]

Figure 1.8(right): Schematic cross sections along the width of MOSFET transistors depicting the effect of gate fringing electrical lines on the extent of depletion region of a STI MOSFET. [4]

In the STI (Shallow Trench Isolation), the depletion region is limited to under the thin oxide only. So the fringing field is useful here and thus the threshold voltage decreases for device with narrow width. This decrease in the threshold voltage of the narrow width device which is opposite to the traditional trend is known as the Inverse Narrow Width Effect.

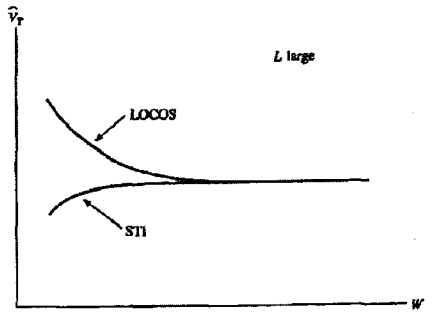


Figure 1.9: Effective threshold voltage Vs width for identically processed MOSFETs except for the isolation process. [4]

1.3.1.4 Optical Proximity Effect

Proximity effect refers to the dependence of the printed CD (critical dimension) on its surroundings. The rapid progress made in developing new high contrast resists and the introduction of new imaging techniques such as phase shifting mask allows the features in the resist to be printed closer and closer to the resolution limit of the exposure tool. As a result of this, optical proximity effects start to become very pronounced.

Poly silicon feature can be classified as isolated or dense depending on the nearest neighbor. Because of the proximity effect there exist a CD offset between dense and isolated line, isolated lines expose the resist with higher light intensity, resulting in shorter channel lengths. Other proximity effects include deformations of the printed features, such as corner rounding and line shortening.

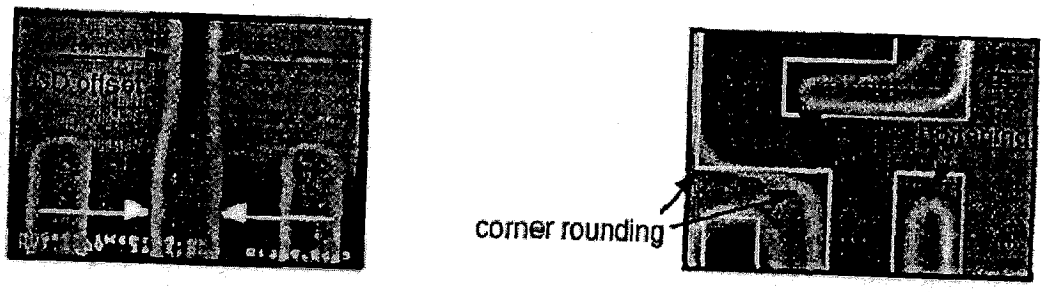


Figure 1.10: Optical proximity phenomena [5]

1.3.2 Random Variations

Random variation is the difference in the electrical characteristics of devices with identical geometry (W/L), layout, and neighborhood within the interaction distance of the known sources of variation. For random variability the only information available is typically the statistical distribution of that variability. So the designer is required to build enough design margin to accommodate that variability. The large margins are usually wasteful in design resources and end up impacting the overall cost and performance. We will refer to these types of phenomena as random variability.

1.3.2.1 Line Edge Roughness

Line Edge Roughness (LER) is the local roughness of the edge of the poly silicon gate along its width. The reason for the increase in the LER in future processes include the random variation in the incoming photon count during exposure and the contrast of aerial image, as well as the absorption rate, chemical reactivity, and the molecular composition of resist.

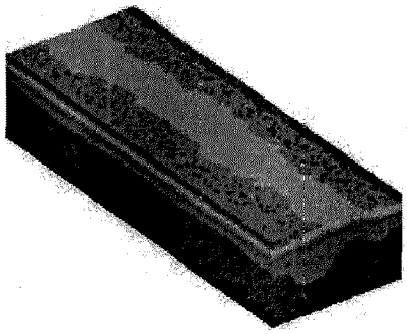


Figure 1.11: Description of Line Edge Roughness

Line edge roughness has impact on all the main electrical device characteristics: the drive current, off-current, and the threshold voltage. The effect of LER is random and cannot be corrected by optical proximity corrections. The easiest way to characterize the line edge roughness is to compute its variance. For example, in a 193nm process, the total variation due to LER has the standard deviation of 3σLER = 6.6 − 9nm, measured on a poly silicon line with Lgate=110nm. [6]

Experimental results have shown that LER does not significantly contribute to the parameter fluctuations of a 90nm technology but it may become dominant for 32nm channel length transistors.

1.3.2.2 Random Dopant Fluctuations

Threshold voltage of a MOS transistor depends on the concentration of the dopant atoms in the channel area. Placement of dopant atoms into the channel is achieved via ion implantation. Implantation and the subsequent anneal is such that the number and placement of atoms implanted in the channel of each transistor is effectively random. Therefore threshold voltage exhibits a significant variation in devices with small area/length.

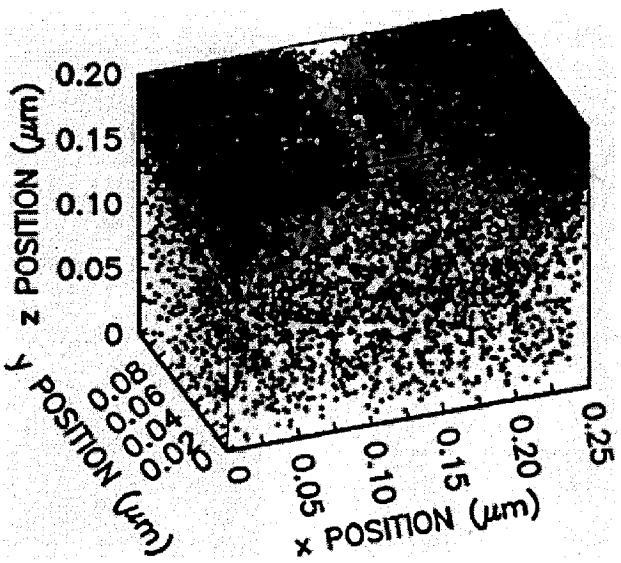


Figure 1.12: 3-D perspective plot of the dopant atoms in a 25-nm MOSFET. Darker dots are donors and lighter dots are accepters. [7]

As the number of the dopant atoms is getting smaller, the variation of the number of dopants around a certain mean value is increasing.

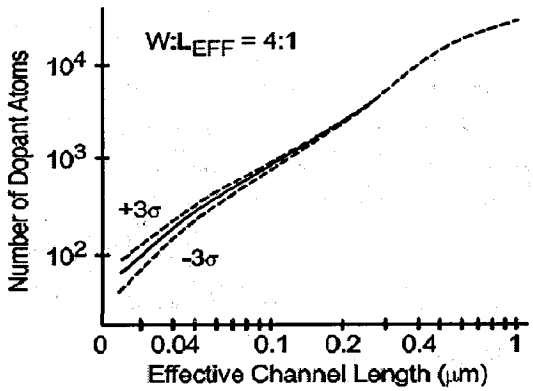


Figure 1.13: The number of dopant atoms in the channel is getting smaller, increasing the relative uncertainty in the actual number. [7]

Based on numerical simulations of dopant concentration variation, an empirical model has been developed for threshold voltage variation due to RDF. [8]

$$\sigma V_{th} = 3.19 \times 10^{-8} \frac{T_{ox} N_A^{0.4}}{\sqrt{L_{eff} W_{eff}}}$$

where $T_{ox}$is the oxide thickness, N_A is the doping density, L_{eff} and W_{eff} are the effective channel length and width.

From a designer's point of view, the important information that this model provides is the inverse dependence of the $V_{th}\sigma$ on the area of the transistor. This dependence tells the designer that uncertainty in large width devices will be much smaller than that of minimal width devices.

1.3.2.3 Oxide Film Thickness

The thickness of the dielectric film that isolates the gate from the silicon channel greatly influences the transistor's electrical properties, including current drive, threshold voltage, and leakage current. The scaling of the oxide thickness has continued with every technology node and is currently approaching 10-12 A. The 3σ variation of oxide thickness is of the order of 2A. The thickness of oxide film of 10A corresponds to approximately 5 atomic layers of SiO_2 while the thickness variation is 1-2 atomic layers.

Since the threshold voltage depends on the thickness of the oxide, therefore it also varies. It is found that for a device with an average T_{ox} = 10.5A, σV_{th}= 4mV. For devices below 30nm, the uncertainty in threshold voltage due to oxide thickness variation becomes comparable to the uncertainty produced by random dopant fluctuations.

Chapter 2

Chopper Stabilization and Gain Boosting Technique

2.1 Theory of Chopping

Chopper Stabilization (CHS) is a continuous time modulation technique that can be employed to reduce the effects of op-amp imperfections including noise (mainly 1/f and thermal noise) and the input referred dc offset voltage. CHS technique applies modulation to transpose the signal to higher frequency where there is no 1/f noise and offset, and then demodulates it back to the baseband after amplification.

The principle of chopper stabilization is shown in figure 2.1. It is assumed that the input signal has a spectrum limited to half of the chopper frequency so no aliasing occurs. The input signal is multiplied by the square wave carrier signal $m_1(t)$ with period $(= \frac{1}{f_{chop}})$. Chopper stabilization eliminates low frequency noise and dc offset by first shifting the input signal to a high frequency. This modulation is accomplished by switching the input signal between the two terminals of the amplifier. After this modulation, the signal is transposed to the odd multiples of the chopping frequency. Low frequency 1/f noise (V_N) and dc offset (V_{OS}) are added to the signal. It is then amplified and demodulated back to the original band. This simultaneously moves the signal back to the baseband frequencies and modulates the 1/f noise and dc offset to odd multiples of chopping frequency.

Since the input signal sees two modulating blocks, one before the amplifier and one after, the desired signal is at the baseband at V_{out}. However, the dc offset and 1/f noise only goes through one modulation block and is transposed to the odd multiples of the chopping frequency. The dc offset and 1/f noise now appears at much higher frequencies than the signal bandwidth and can be easily filtered, leaving the amplifier ideally without any offset and low frequency noise.

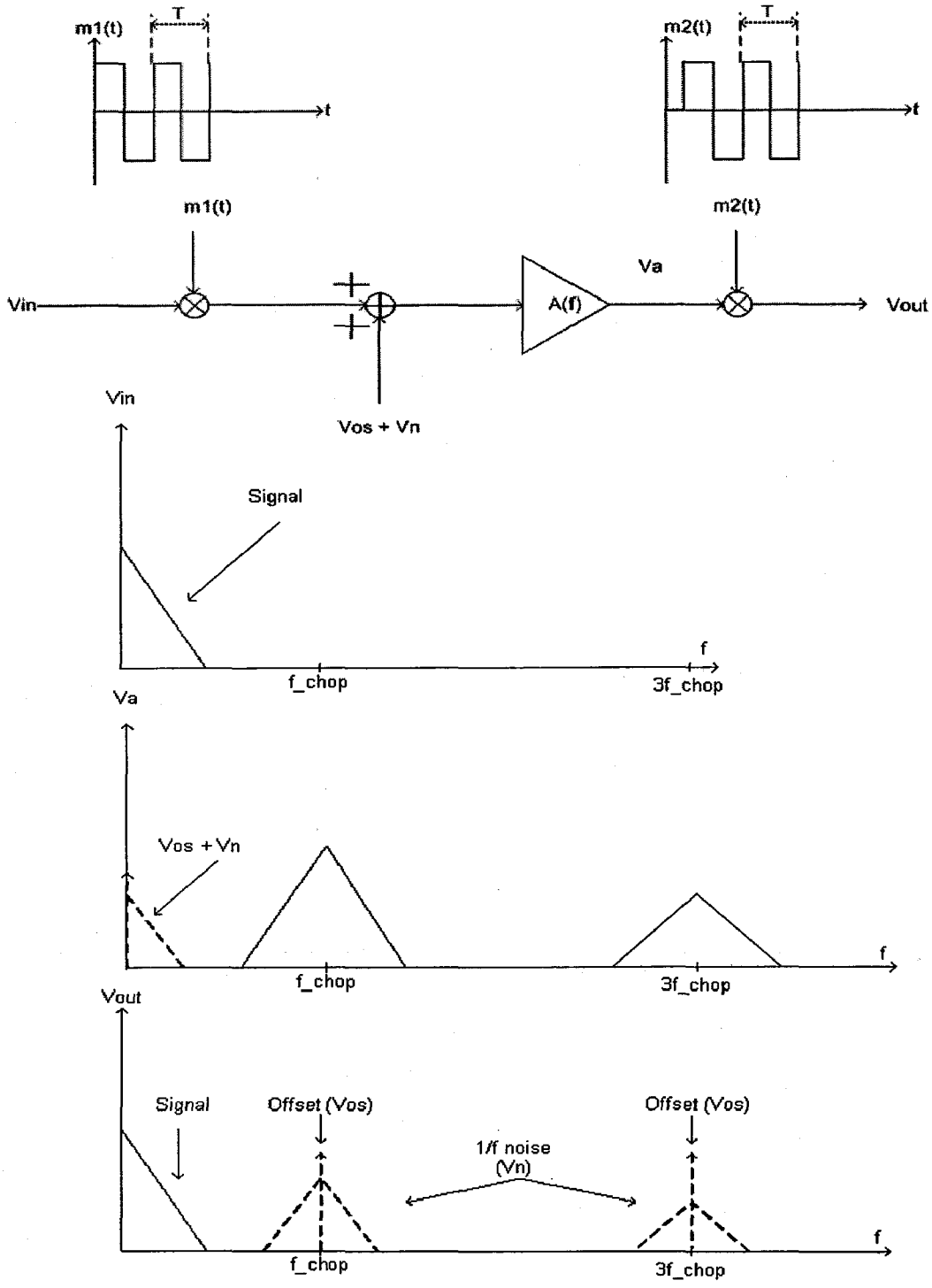


Figure 2.1: Principle of chopping

2.1.1 Chopping Principle in Time Domain

To demonstrate the principle of chopping in time domain, an amplifier with offset (V_{OS}) is connected in unity feedback configuration with chopper blocks at input and output. During the first phase of the clock cycle, both signals are passed straight through the chopping blocks. And the signals switch outputs for the second stage.

Figure 2.2(b) shows the circuit during phase 1. It is simply connected in unity feedback configuration. In this configuration, the op amp (with high gain) will output whatever voltage and current it takes to make voltage difference between its 2 input terminals to be zero, or equivalently for voltage at negative terminal ($V\_$) to be equal to voltage at positive terminal(V_+). So,

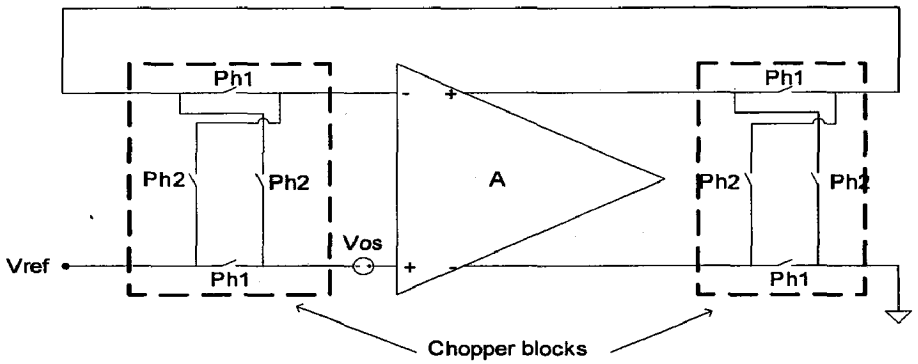
$V_{out} = V_{ref} + V_{OS}$

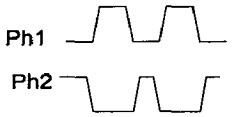
Figure 2.2(c) shows the circuit during phase 2. Now the chopper block switches the output but still the op amp is connected in negative feedback. In this configuration, the op amp will try to force voltage at positive terminal (V_+) to be equal to voltage at negative terminal ($V\_$). (if V_+ is more (or less) than $V\_$, then the output will go down (or up), which will result in V_+ going down (or up)).

$V_{out} + V_{OS} = V_{ref}$

$V_{out} = V_{ref} - V_{OS}$

So, offset (V_{OS}) appears as $+V_{OS}$ for half of the clock period and $-V_{OS}$ for the other half of the clock period. The average offset becomes zero.





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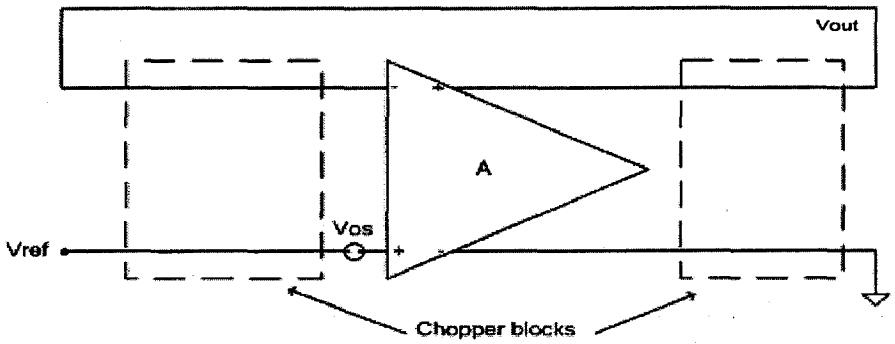

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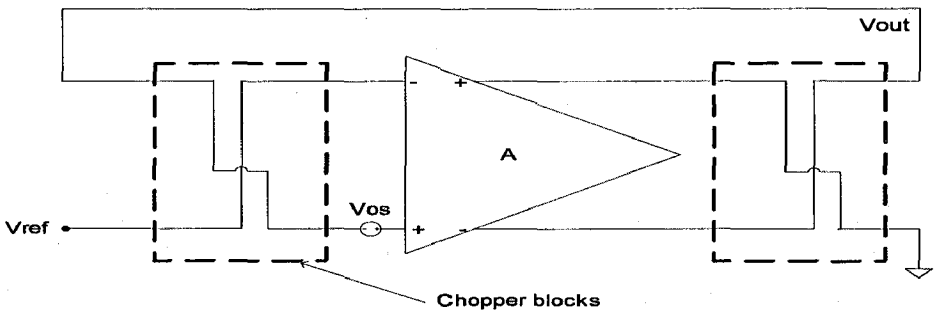

(c)

Figure 2.2: (a) Chopper Stabilized op amp (b) & (c) during phase1 and phase2 respectively

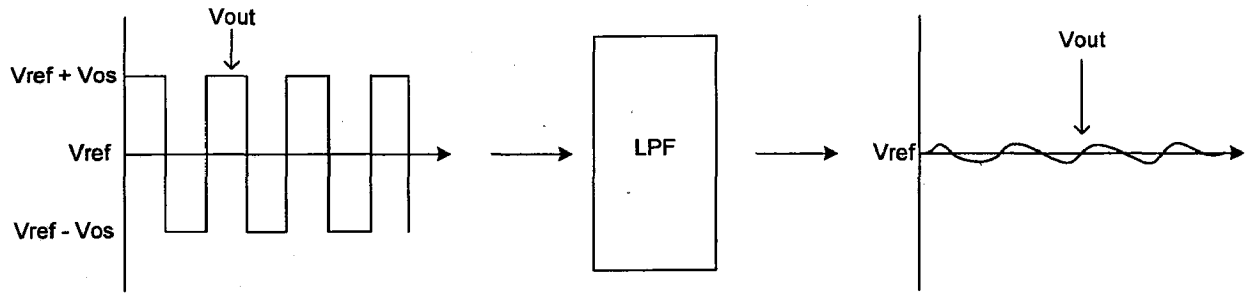

Figure 2.3: Effect of chopping on offset

2.1.2 Chopping Blocks

Four switches are used for each modulator block seen in figure 2.4. This is the basic chopping block that has two inputs and two outputs. During the first phase of the clock cycle, both signals are passed straight through the modulator. And the signals switch outputs for the second stage. Special attention must be paid to the timing of the two phases. In general, they should be driven with a non-overlapping clock to prevent noise leakage. This (non-overlapping) clock contains a short period of time where neither signal is propagated through the chopping block to prevent noise leakage during switching. The phases should also be close to a 50% duty cycle for proper modulation.

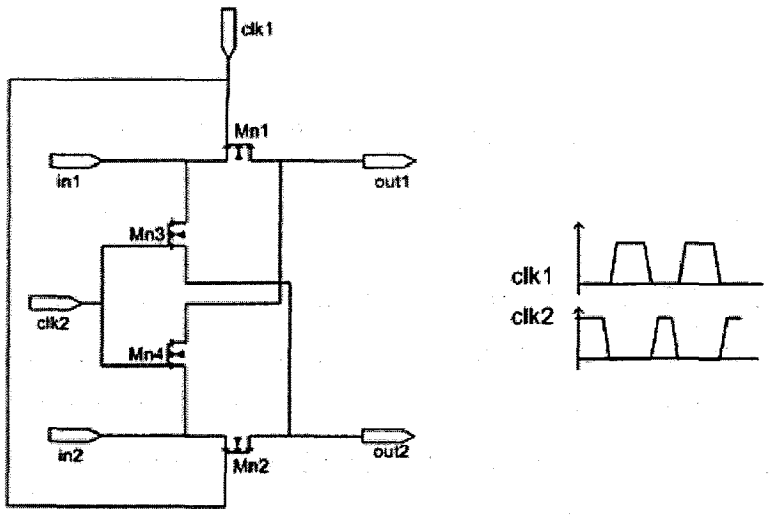

Figure 2.4: Chopping block with non-overlapping phase clock

2.2 The Gain Boosting Technique

In modern processes with sub-nanometer channel length devices, the intrinsic MOS transistor gain $g_m * r_o$ is about 20-25dB, resulting in a DC-gain of the cascoded version of about 40-50dB. This is however in many cases not sufficient.

The Gain Boosting Technique increases the DC-gain of the cascoded CMOS amplifier without affecting its bandwidth. This is achieved by increasing the effect of the cascode transistor by means of an additional gain-stage, thus increasing the output impedance of the sub-circuit.

2.2.1 Gain Boosting Principle

The idea behind gain boosting is to further increase the output impedance without adding more cascode devices. A feedback amplifier is used to increase the output resistance of the cascode as shown in figure 2.5.

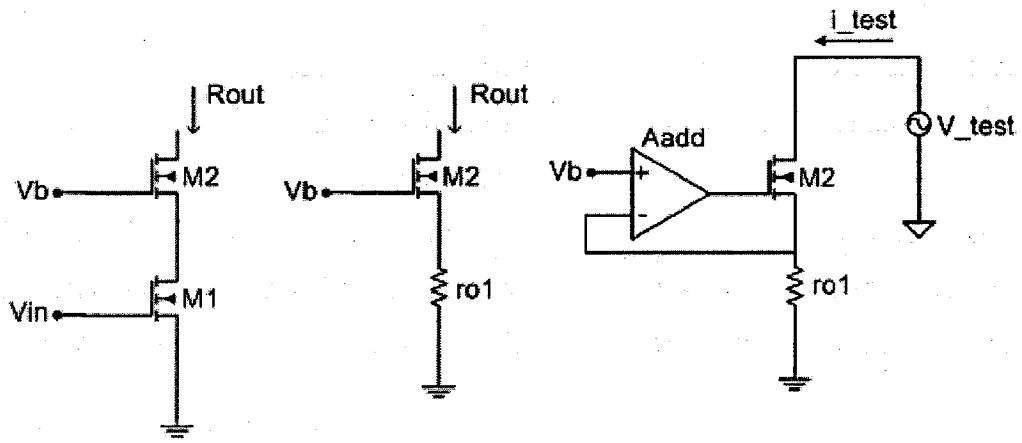

Figure 2.5: Increasing the output impedance by feedback

The output voltage of the amplifier is given as,

$$V_{out} = A_{add} \cdot (V_+ - V_-)$$

To calculate the output resistance, a small signal test voltage v_T is connected at the output and input is short circuited.

$$v_{gs2} = -A_{add} i_T r_{01} - i_T r_{01}$$

$$= -i_T r_{01}(A_{add} + 1)$$

$$i_T = g_{m2} * v_{gs2} + \frac{v_T - i_T * r_{01}}{r_{02}}$$

$$i_T = -g_{m2} i_T r_{01}(A_{add} + 1) + \frac{v_T - i_T r_{01}}{r_{02}}$$

$$R_{out} = \frac{v_T}{i_T} = (r_{02} + r_{01}) + g_{m2} r_{02} r_{01}(A_{add} + 1)$$

$$\approx g_{m2} r_{02} r_{01} A_{add}$$

The output resistance of the cascode ($\approx g_{m2} r_{02} r_{01}$) is increased by the gain of the added amplifier.

The amplifier holds the drain voltage of M_1 equal to V_b. If the drain voltage of M_1 increases, then the output of the amplifier decreases, thereby attempting to shut off M_2 , as a result of which the drain (source) voltage of $M_1(M_2)$ reduces to maintain the current. Thus, the amplifier holds the drain voltage of M_1 at a constant voltage and makes the output resistance very high.

In the gain boosted amplifier, the feedback amplifier is implemented as a simple common source amplifier as shown in figure 2.6 and is used on the load side also.

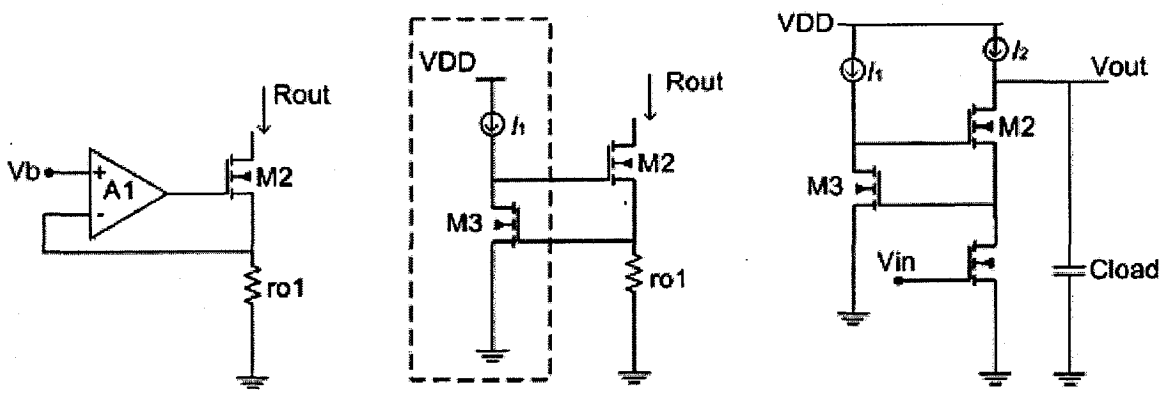

Figure 2.6: Implementation of the gain boosting amplifier

2.2.2 High Frequency Behavior

In figure 2.7, a gain Bode-plot is shown for the original cascoded gain-stage (A_{orig}), the additional gain-stage (A_{add}) and the improved cascoded gain-stage (A_{tot}). At DC, the gain enhancement $\frac{A_{tot}}{A_{orig}}$ equals approximately $[1 + A_{add}\ (0)]$.

For $f > f_1$, the output impedance is mainly determined by C_{load}. This results in a first-order roll-off of A_{tot} (f). Moreover, this implies that A_{add} (f) may have a first order roll-off for $f > f_2$as long as $f_2 > f_1$. This is equivalent to the condition that the unity-gain frequency (f_4) of the additional gain-stage has to be larger than the 3-dB bandwidth (f_3) of the original stage, but it can be much lower than the unity-gain frequency (f_5) of the original stage. The unity-gain frequencies of the improved gain-stage and the original gain-stage are the same.

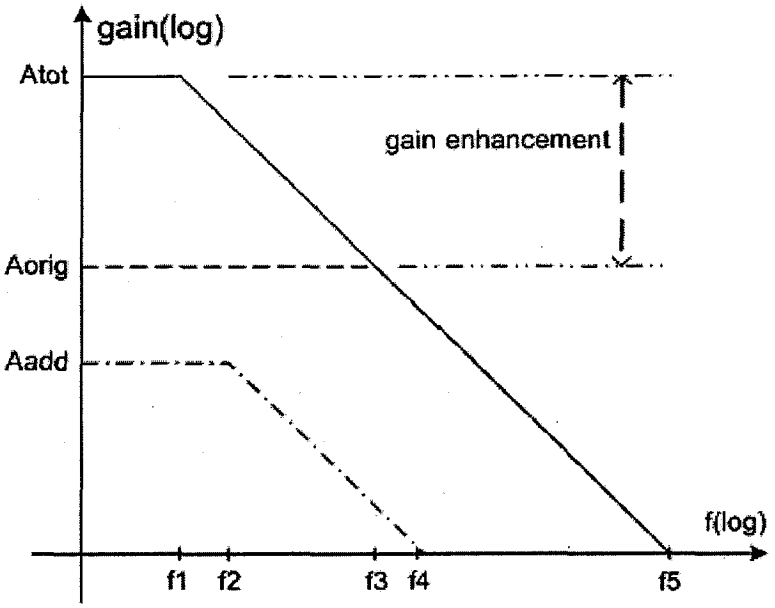

Figure 2.7: Gain Bode-plots of the original cascode gain stage (A_{orig}), the additional gain stage (A_{add}), & the improved cascoded gain stage (A_{tot}) [12]

From the above, to obtain a first-order roll-off of the total transfer function, the additional gain-stage does not have to be a fast stage. Moreover, as the additional stage forms a closed loop with M_2, stability problems may occur if this stage is too fast. There are two important poles in this loop. One is the dominant pole of the additional stage and the other is the pole at the source of M_2. For stability reasons, we set the unity-gain frequency of the additional stage lower than the second pole frequency (f_6) of the added amplifier. A safe range for the location of the unity-gain frequency f_4 of the additional stage is given by

$$f_3 < f_4 < f_6$$

2.2.3 Settling Behavior

The Gain-Boosting Technique increases the output impedance, Z_{out}, by a factor approximately equal to (A_{add} + 1). The gain of the additional stage, A_{add}, decreases for frequencies above f_2 (figure 2.7) with a slope of -20 dB/decade. For frequencies above f_4, A_{add} is less than one, and the normal output impedance Z_{orig} of a cascode stage without gain enhancement remains. The figure 2.9 also shows the load impedance (Z_{load}) and the total impedance at the output node (Z_{out}).

The total impedance at the output of the amplifier is the parallel connection of the load capacitance and the output impedance of the circuit. At f_2, the output impedance of the circuit begins to decrease as a function of frequency due to the roll-off of the additional stage. This can be modeled as a small capacitor in parallel with the output resistor. This small capacitor is simply parallel connected to the (large) output capacitance and gives a small shift of the total impedance at the output. At f_4 however, the effect of this small capacitor disappears because the gain of the additional stage goes below one. At this frequency, a small shift in the total output impedance occurs, back to the original line (in figure 2.9) determined by the load capacitor only. A closer look at the plot reveals that a doublet is present in the plot of the total output impedance near f_4.

Non complete doublet cancelation can seriously degrade the settling behavior of an op amp [refer bult]. If a doublet is present in an op amp open-loop transfer function at f_{pz} , a slow settling component is present with time constant $1/f_{pz}$.

If the time constant of the doublet $1/f_{pz}$ is smaller than the main time constant $1/\beta f_{unity}$, the settling time will not be increased by the doublet. This is achieved when the unity gain frequency of the additional stage is higher than the -3 dB bandwidth of the closed-loop circuit. On the other hand, for reasons concerning stability, the unity-gain frequency must be lower than f_6. This results in the "safe" area for the unity-gain frequency of the additional stage

$$\beta f_5 < f_4 < f_6$$

as shown in figure 2.8. Note that this safe area is smaller than given by (equation).

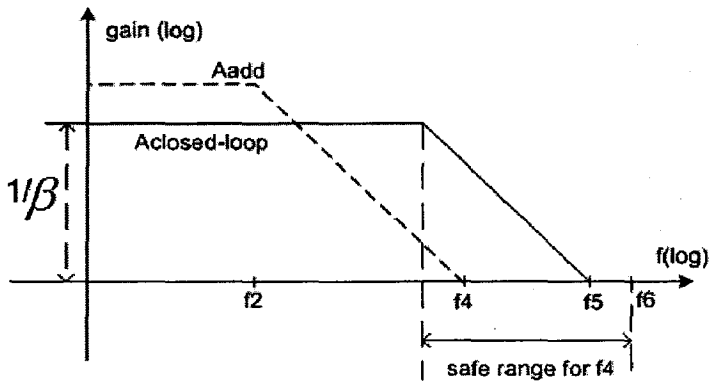

Figure 2.8: The "safe" range for the unity-gain frequency of the additional stage [12]

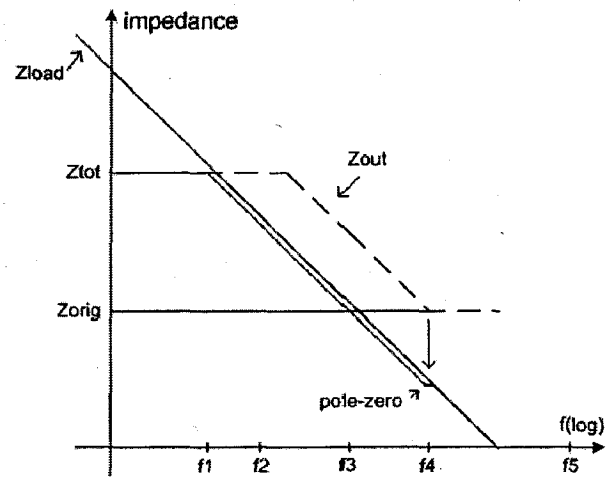

Figure 2.9: The output impedance as a function of frequency [12]

Chapter 3

Chopper Stabilized Op Amp

Operational Amplifiers (Op Amps) are an integral part of many analog and mixed signal systems. Op Amp is a key building block for many applications like bandgap reference circuit, sensor application, etc. In many cases, the overall performance of the system is limited by the input referred offset of the op amp.

In this chapter, we discuss the design of a robust chopper stabilized op amp, which can overcome the limitations imposed by offset. The core of the design is the well known folded cascode op amp. Gain boosting is used to increase the DC gain of the op amp and chopper stabilized technique is used to reduce the op amp's input referred offset voltage.

3.1 Circuit Details

The detailed schematic of the proposed chopper-stabilized amplifier is shown in figure 3.1. M_{p1}-M_{p7} , $M_{n1} - M_{n4}$ forms the core PMOS input folded cascode amplifier. Common Source stage is used to implement the gain boosting. M_{n5}, M_{p10} & M_{n6}, M_{p11} forms the gain boosting stage at the folded cascode node. M_{p8}, M_{n7} & M_{p9}, M_{n8} forms the gain boosting stage at the load current source of the folded cascode op amp. M_{n9}, M_{n10} acts as capacitor to stabilize the gain boosting stage at the folded cascode node.

$M_{p1}(= M_{p2})$ is sized relatively large (to increase their area) to minimize the threshold voltage (ΔV_t) mismatch and size ($\Delta(W/L)$) mismatch between the input transistors. The DC bias current (I_{bias}) in the tail current source is kept to 194.4 μA to get the required UGB (Unity Gain Bandwidth). The DC current in the folded branch is kept to around 233.6 μA(1.2 times the I_{bias}), so that DC current in the cascode mirror never goes to zero. $M_{p7}, M_{n1}(= M_{n2})$ are sized to provide the required bias current. $M_{p5}(= M_{p6})$ is sized to keep the voltage at drain of M_{p3} (= gate voltage of M_{p5}) to be around V_{out} to minimize the systematic offset. The output voltage (=gate voltage of M_{p5}) is around 1.3 volts. $M_{p3}(= M_{p4})$ are sized large to keep its overdrive

voltage small, $M_{p8}(= M_{p9})$ are sized to provide M_{p3} & M_{p4} the required drain to source voltage to keep them well within saturation.

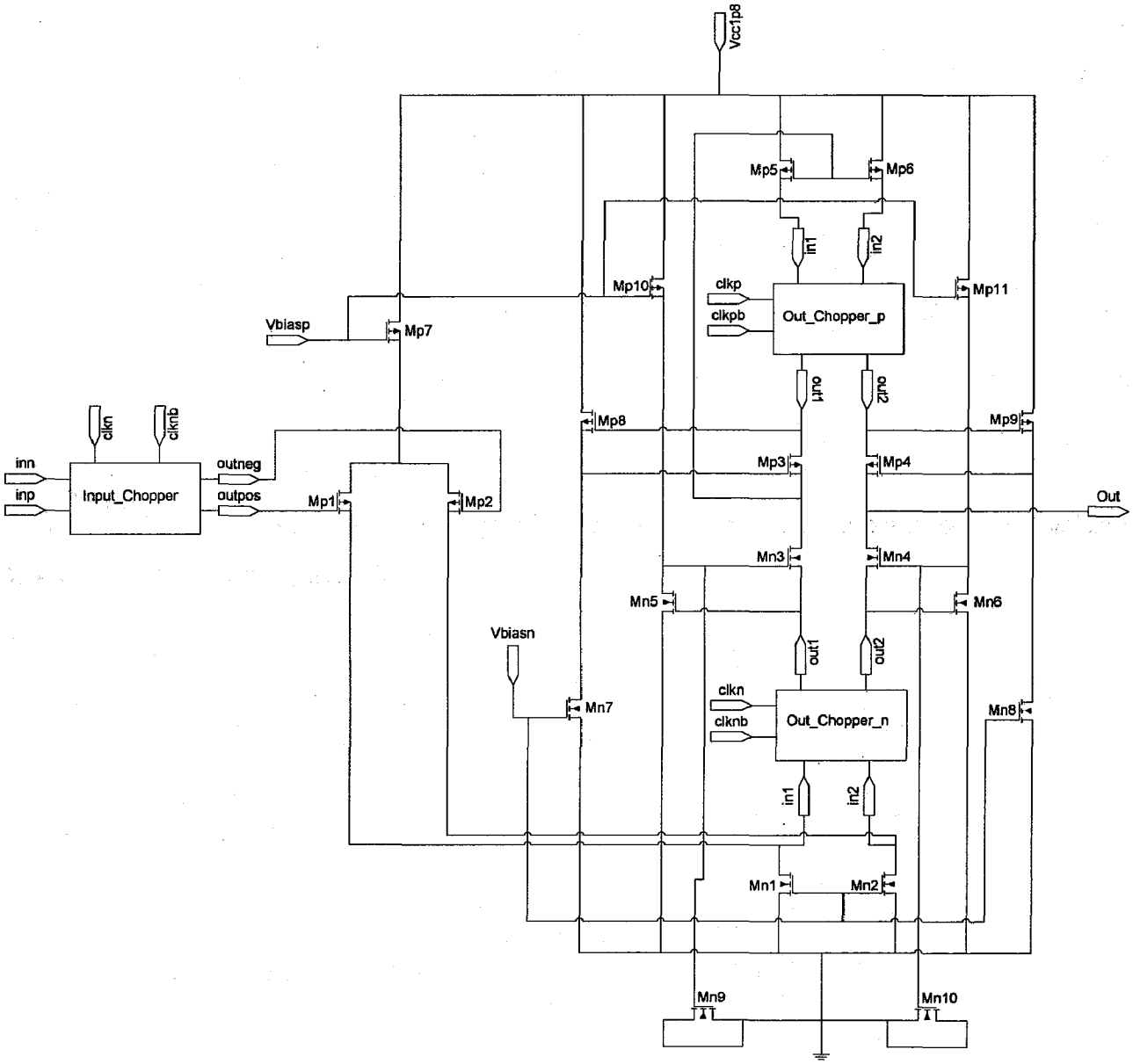

Figure 3.1: Chopper Stabilized Op Amp circuit

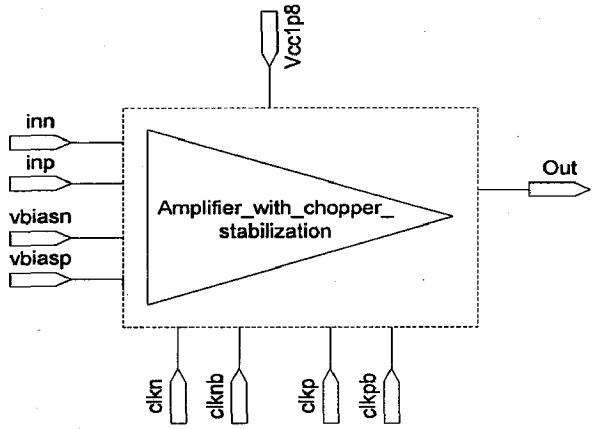

Figure 3.2: Chopper Stabilized Op Amp symbol

Table 3.1: Component size in Chopper Stabilized Op Amp

Transistor	W/L * $Mult_i$	Transistor	W/L * $Mult_i$
M_{p1}	256	M_{n1}	18
M_{p2}	256	M_{n2}	18
M_{p3}	64	M_{n3}	16
M_{p4}	64	M_{n4}	16
M_{p5}	6	M_{n5}	2
M_{p6}	6	M_{n6}	2
M_{p7}	20	M_{n7}	2
M_{p8}	8	M_{n8}	2
M_{p9}	8	M_{n9}	50
M_{p10}	2	M_{n10}	50
M_{p11}	2		

Note: All the transistors in the chopper stabilized op amp have the same W/L for good matching. Table gives the relative sizes of all the transistors.

3.1.1 Biasing

Constant g_m circuit is used to generate the bias voltage (V_{biasn} & V_{biasp}) for the amplifier. The resistor (which defines the current) is placed on the PMOS side to reduce the body effect. The current in the constant g_m circuit is highly sensitive to changes in supply voltage (V_{CC}) due to the finite MOSFET output resistance (r_o) at short channel lengths. To reduce the sensitivity, a differential amplifier ($M_{p3}, M_{p4}, M_{n3}, M_{n4}$) is added to the circuit. The idea is to use the differential amplifier to compare the drain voltages of $M_{p2}(V_{biasp})$ with the drain voltage of M_{p1} and regulate them to be equal. The result is an effective increase in M_{p1} output resistance. To make the circuit stable, capacitor (M_{n7}) is added.

A "start-up circuit" is also added to make sure that the circuit doesn't settle to degenerate bias point when the supply is turned on. In the degenerate bias state gates of M_{n1}/M_{n2} are at ground while the gates of M_{p1}/M_{p2} are at V_{CC}. When in this state, the gate of M_{p5} is at V_{CC} and so it is off. The gate of M_{n5}/M_{n6} is somewhere between V_{thn}(threshold voltage of NMOS transistor) and ground. M_{p6}, which behaves like a PMOS switch, turns on and leaks current into the gate of M_{n1}/M_{n2} from the gates of M_{p2}. This causes the current to snap to the desired state and M_{p6} to turn off.

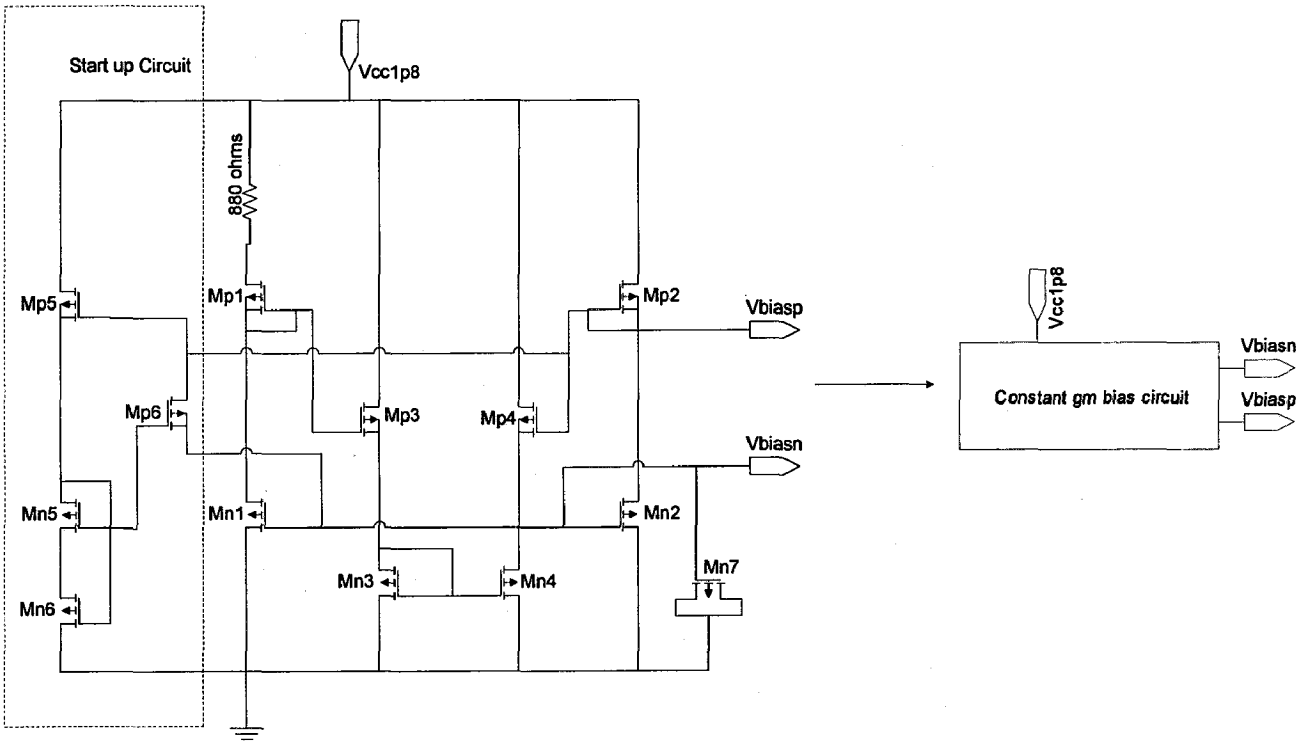

Figure 3.3: Constant g_m bias circuit and its symbol

Table3.2: Component size in bias circuit

Transistor	W/L * $Mult_i$	Transistor	W/L * $Mult_i$
M_{p1}	48	M_{n1}	6
M_{p2}	12	M_{n2}	6
M_{p3}	12	M_{n3}	6
M_{p4}	12	M_{n4}	6
M_{p5}	12	M_{n5}	2
M_6	4	M_{n6}	2
		M_{n7}	400

Note: All the transistors in the chopper stabilized op amp have the same W/L for good matching. Table gives the relative sizes of all the transistors.

For a current of around 100 μA in the bias circuit, the transistors $M_{p1}, M_{p2}, M_{n1}, M_{n2}$ are sized to generate, V_{biasn}=0.4576 V & V_{biasp}=1.3234 V.

3.2 Chopping Locations

Now let's look at the chopper switches. The circuit has three chopper switches, one is at the input and the other two are at the low-impedance nodes between the active loads and the cascoded devices. Since the input signal to the amplifier will be around 0.6 to 0.7 volts, the input chopper (see figure 3.4) uses NMOS transistors. The PMOS chopper for the top output device uses PMOS transistors while NMOS transistors are used in the lower NMOS chopper. This design choice comes from the ability to turn the switches on and off quickly and the bias points of the two nodes. The upper and lower gate voltages are biased at 1.3234V and 0.4576V, respectively. The supply voltage is only 1.8V. Even with a low threshold voltage for an NMOS device, it may not be able to turn on completely if placed at the top node. Thus PMOS transistor is used and clocked with the opposite phase of the NMOS device. NMOS transistors can be used at the lower node.

Devices for the chopper switches are sized to keep the ON resistance to minimum. The main concern when choosing the switch sizes was to minimize the voltage drop across the switches, when bias current flows through it. Since no current flows through the input chopper, so width of the transistors in input chopper is less.

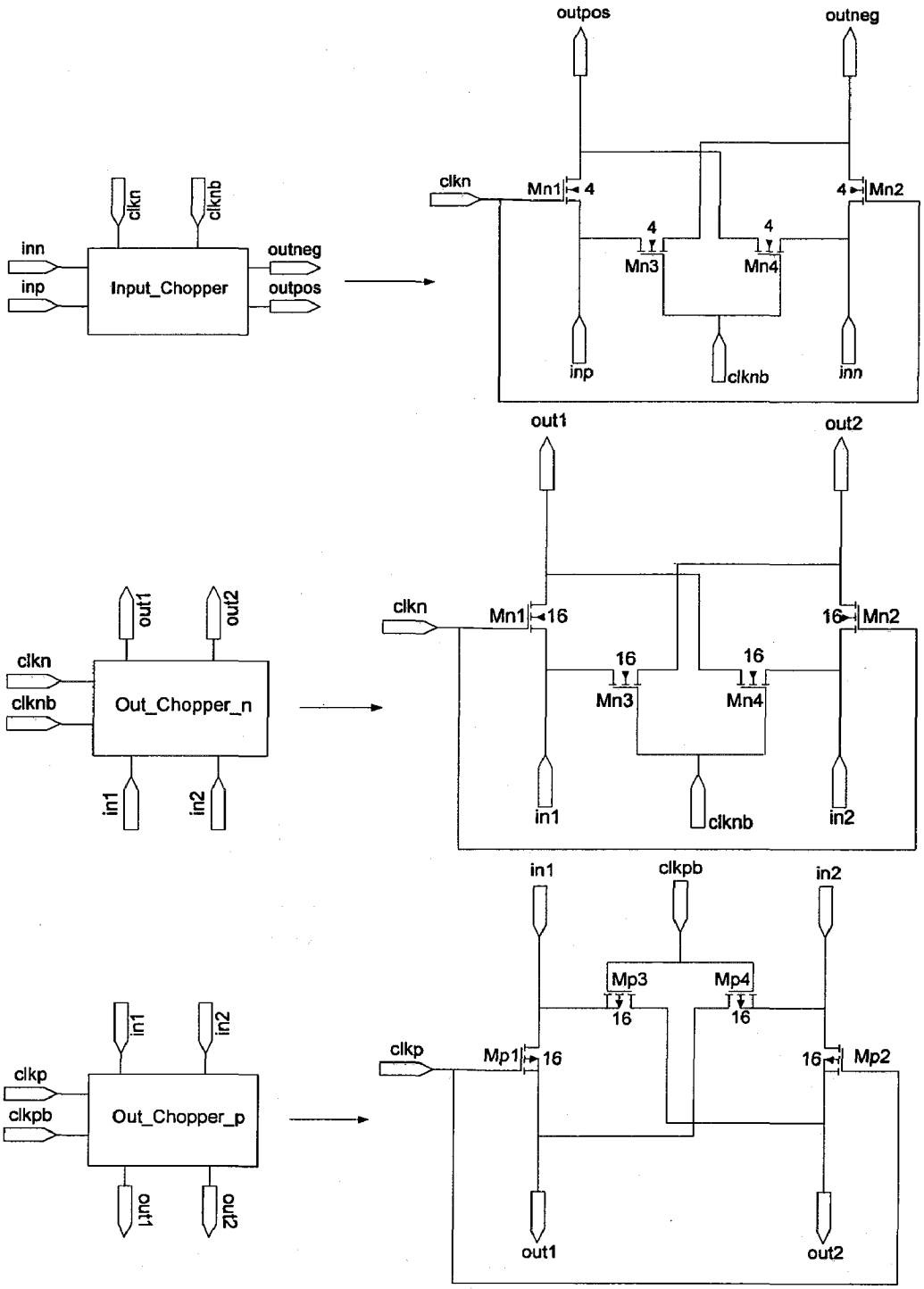

Figure 3.4: Chopper blocks with their symbols

3.3 Timing

A two-phase non-overlapping clock with a fifty-percent duty cycle is used to drive the four devices in each chopper block. Since both PMOS and NMOS switches are used, complements of both phases are required for simultaneous switching. The chopping frequency is 4 Mhz, and the non overlap period is around 70ps. In order to create the non-overlapping clock, the 4 MHz input clock is passed to the clock generator shown in figure 3.5 which creates both phases and their complements. All four signals must be generated at the same time to ensure that the clock edges line up properly and the PMOS and NMOS switches should turn on or off simultaneously.

The output inverter in the non-overlapping clock generator circuit is sized large to avoid the loading. The switches in the lower and upper chopper have size of 16*W/L, so if the inverter with small transistor size is used to drive the switches, it may get loaded.

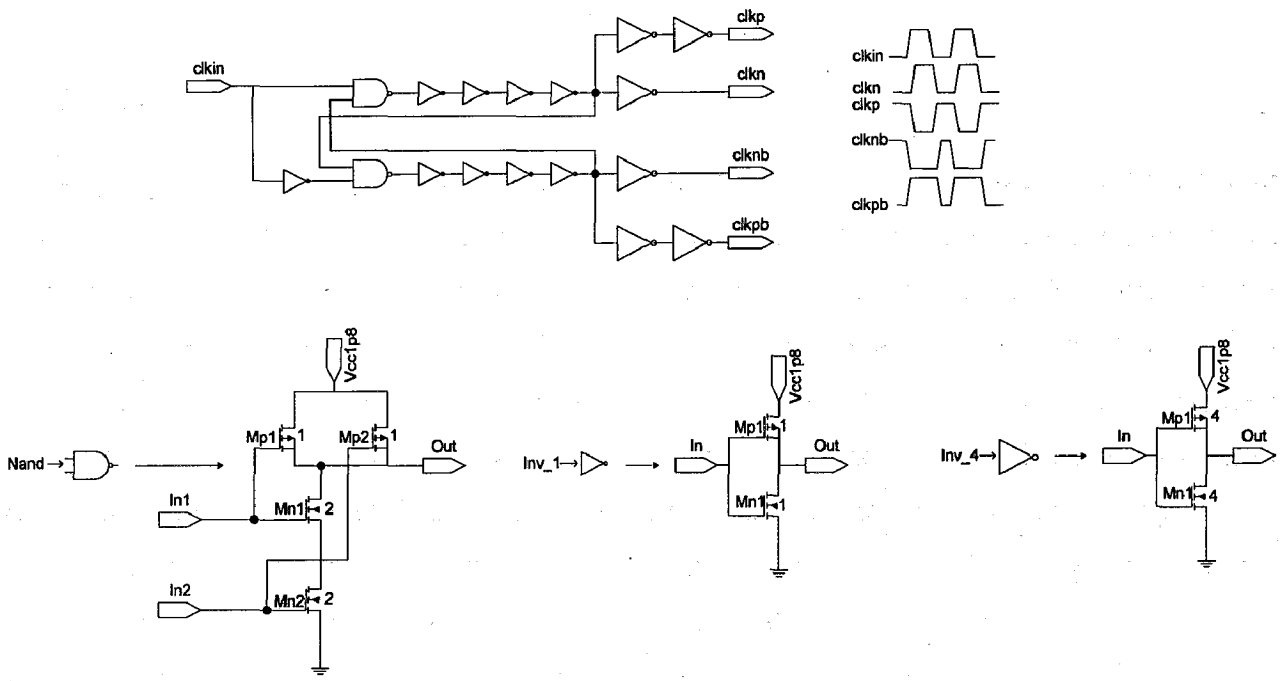

Figure 3.5: Non-overlapping clock generator circuit

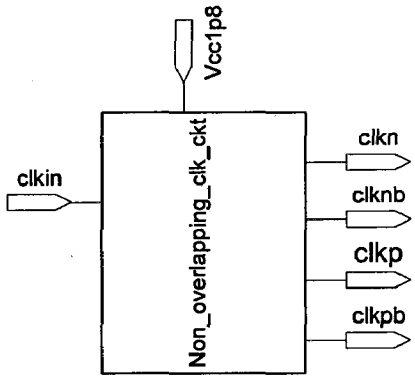

Figure 3.6: Non overlapping clock generator symbol

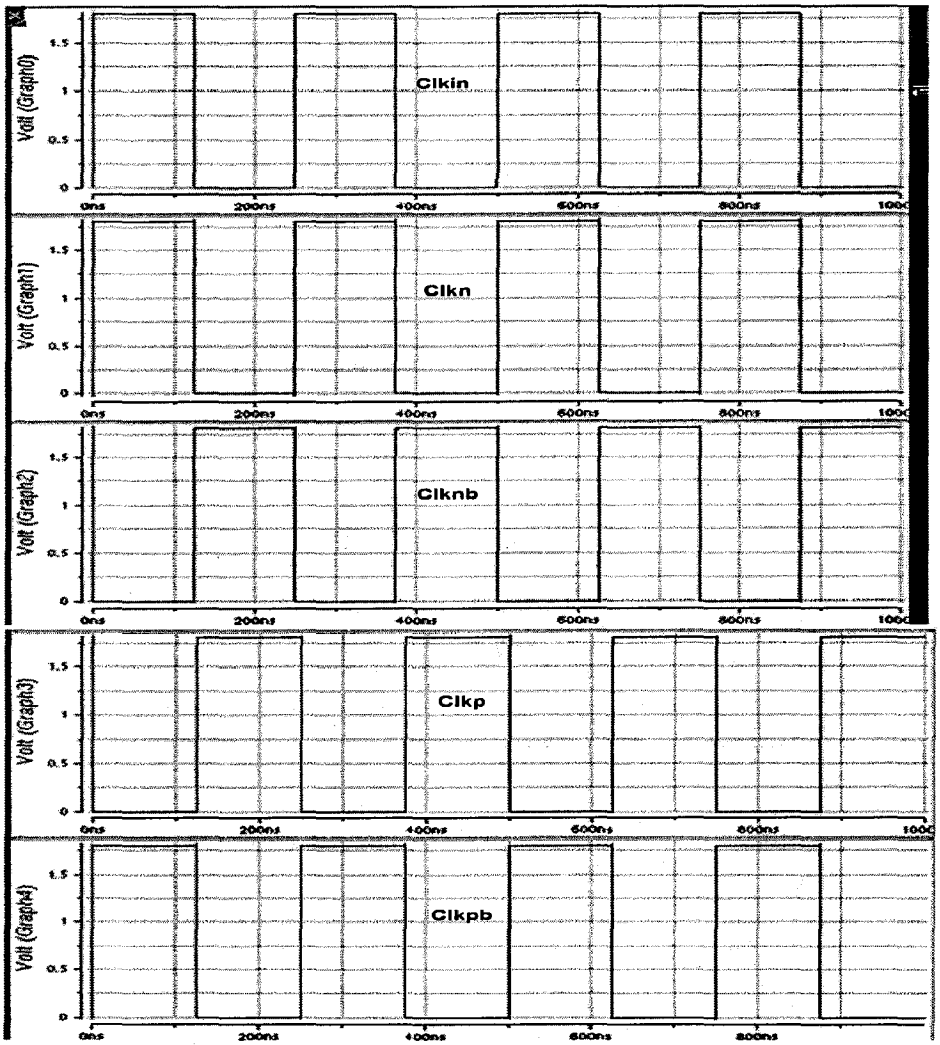

Figure 3.7: Simulated clock signals

3.4 AC Response

3.4.1 Chopper Stabilized Op Amp

The open loop frequency response of the chopper stabilized op amp is measured by connecting it in the configuration shown in figure 3.8. RC network in the feedback establishes the correct DC operating point but act as open circuit (because of large time constant) for AC. The simulated magnitude and phase response at the output is shown in figure 3.9.

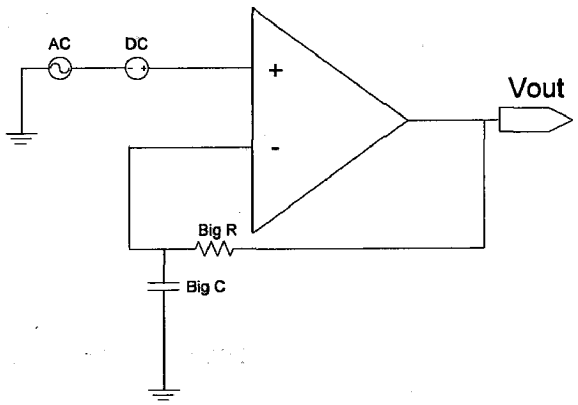

Figure 3.8: Open loop frequency response of Chopper Stabilized Op Amp

Table 3.3: Chopper Stabilized Op Amp's frequency response

Unity Gain Bandwidth (UGBW)	98 Mhz
DC Gain	78 dB
Phase Margin (PM)	88 Degrees
Power	2 mW

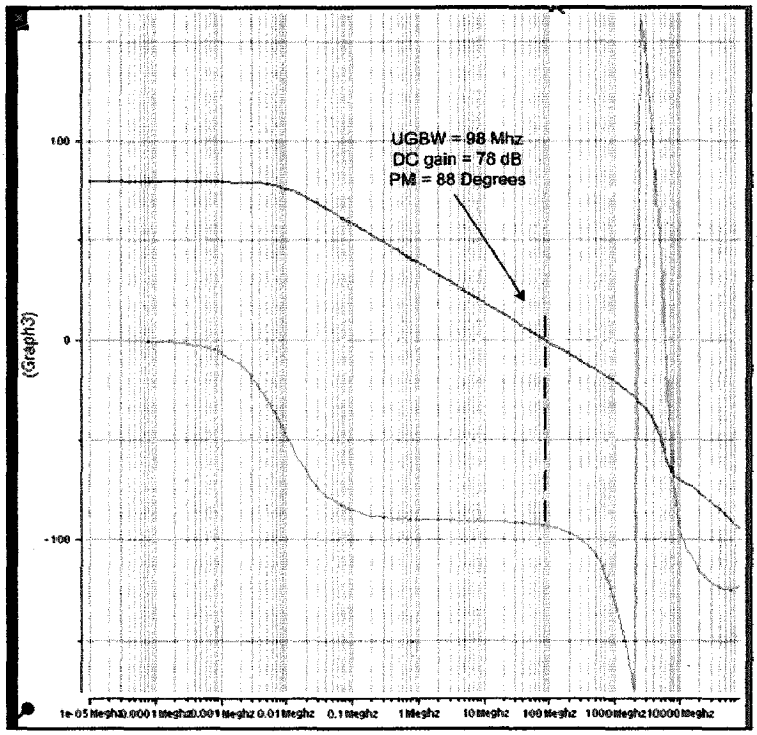

Figure 3.9: Chopper Stabilized Op Amp's Magnitude and Phase Response Vs Frequency

3.4.2 Gain Boosting Amplifier

The open loop frequency response of the gain boosting stage at the folded cascode node is measured by breaking the loop as shown in figure 3.10. Magnitude and Phase response is plotted at source of M_{n3}. Figure 3.11 shows that the Unity Gain Bandwidth of the gain boosting stage is 847 Mhz (> Unity Gain Bandwidth (98 Mhz) of the main amplifier) as required from the discussion in chapter 2.

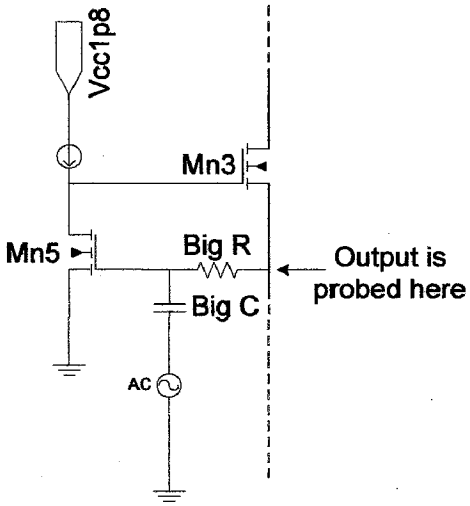

Figure 3.10: Open loop frequency analysis of gain boosting stage at folded cascode node

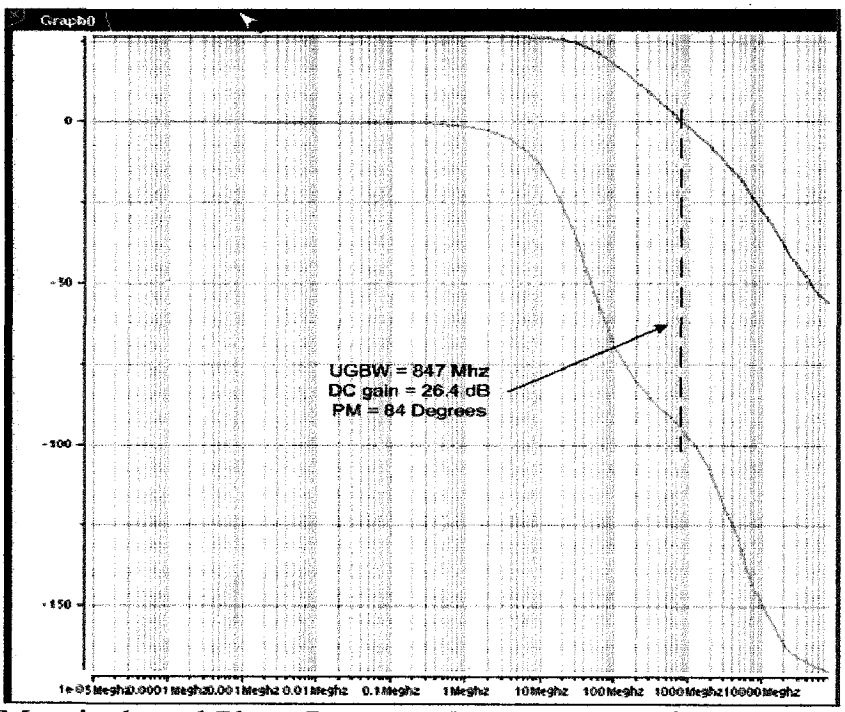

Figure 3.11: Magnitude and Phase Response Vs Frequency of gain boosting amplifier at folded cascode node

Table 3.4: Gain Boosting Stage's (at the folded cascode node) frequency response

Unity Gain Bandwidth (UGBW)	847 Mhz
DC Gain	26.4 dB
Phase Margin (PM)	84 Degrees
Power	0.036 mW

Similarly the open loop frequency at the load cascode node is calculated. Here also the Unity Gain Bandwidth (4900 Mhz) of the gain boosting stage is more than the Unity Gain Bandwidth (98 Mhz) of the main amplifier.

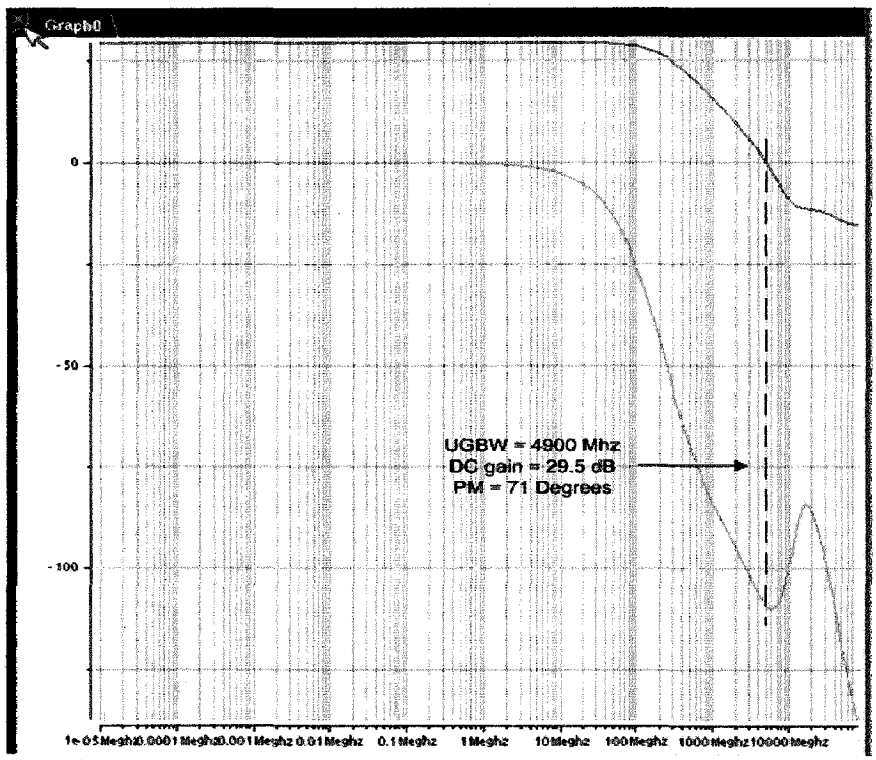

Figure 3.12: Magnitude and Phase Response Vs Frequency of gain boosting amplifier at load cascode node

Table 3.5: Gain Boosting Stage's (at the load cascode node) frequency response

Unity Gain Bandwidth (UGBW)	4900 Mhz
DC Gain	29.5 dB
Phase Margin (PM)	71 Degrees
Power	0.058 mW

3.5 Effect of Chopping on Op Amp Offset

The input-referred offset of the Op Amp is a critical performance parameter for most applications. There are three main sources that contribute to the overall offset,

1: threshold voltage mismatch ΔV_t between the input transistors,
2: size mismatch $\Delta(W/L)$ between the input transistors, and
3: current mismatch ΔI between the active load transistors.
The input-referred offset can be expressed as:

$$V_{OS} = |\Delta V_t| + \left|\frac{\Delta\left(\frac{W}{L}\right) I_b}{g_{m1}}\right| + \left|\frac{\Delta I}{g_{m1}}\right|$$

where g_{m1} is the transconductance of the input stage and I_b is its bias current.

The input referred offset of the proposed chopper stabilized op amp is obtained through Monte Carlo simulation (with chopping off). The input referred offset has a sigma(σ) of 9.1 mV. To analyze how chopping eliminates the input referred offset of the op amp, it is connected as shown in figure 3.13. To model the offset in circuit analysis, a battery of 27.3 mV (3σ) is used. When the chopping is off, offset of 27.3 mV is observed at the output. When the chopping is enabled ($F_{chop} = 4Mhz$), the offset appears as 27.3 mV for half of the clock period and -27.3 mV for the other half of the period. The average offset becomes zero. A low pass filter is placed at the output to filter out the high frequency components and obtain the average value of the output.

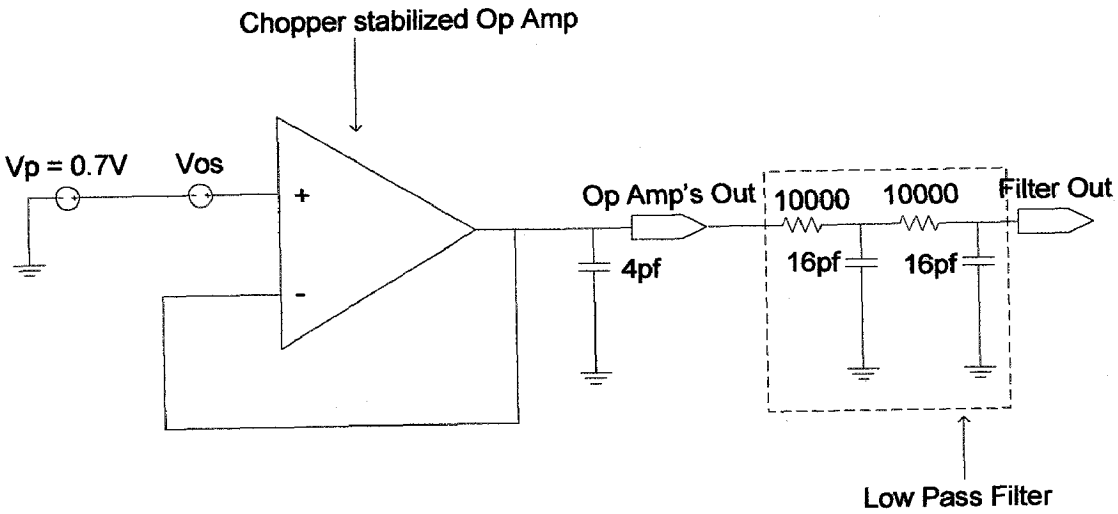

Figure 3.13: Effect of chopping on op amp

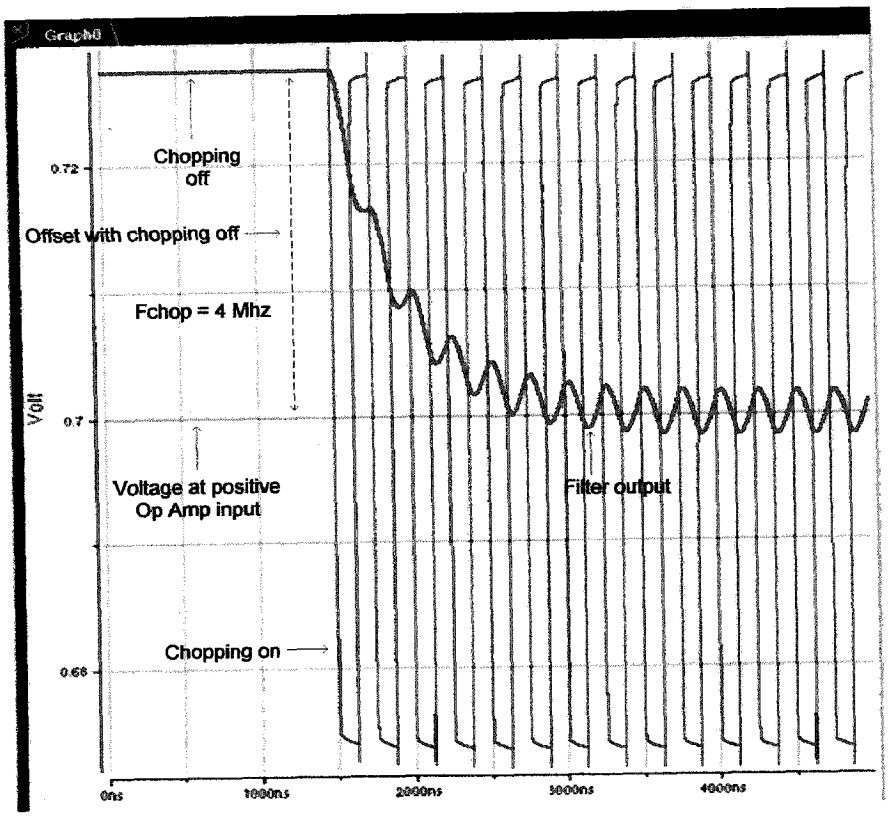

Figure 3.14: Effect of chopping on offset of Op Amp

CHAPTER 4

Bandgap Reference

Reference voltage generators with low sensitivity to the temperature and supply voltage are commonly required in mixed-signal circuits such as ADC or DAC. Bandgap reference circuits play a vital role in most of today's high performance portable systems. The input referred offset voltage of the op amp introduces error in the output voltage of the bandgap. The proposed chopper stabilized op amp is used in the bandgap reference circuit to decrease the effect of offset.

A bandgap reference is a circuit that adds two voltages having opposite temperature coefficient with proper weighting to get a reference voltage having zero temperature coefficient. The base-emitter voltage of bipolar transistors exhibits a negative temperature coefficient.

For a bipolar device, $I_C = I_S \exp(V_{BE}/V_T)$, where $V_T = kT/q$. The saturation current I_S is proportional to $\mu kT n_i^2$, where μ denotes the mobility of minority carriers and n_i is the intrinsic minority carrier concentration of silicon. The temperature dependence of these quantities is represented as $\mu \propto \mu_o T^m$, where $m \approx -3/2$, and $n_i^2 \propto T^3 \exp(-\frac{E_g}{kT})$, where $E_g \approx 1.12\ eV$ is the bandgap energy of silicon.

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_T}{T} ln \frac{I_C}{I_S} - (4+m)\frac{V_T}{T} - \frac{E_g}{kT^2} V_T$$

The positive temperature coefficient comes from the voltage difference between two pn junctions having unequal current densities.

$$V_{BE1} - V_{BE2} = \Delta V_{BE} = V_T ln \frac{I_C}{I_S} - V_T ln \frac{I_C}{nI_S} = V_T \ln(n),$$

where n equals to the current density ration of two junctions.

4.1 Circuit Details

Figure 4.1 shows the bandgap circuit. Because of high gain of the chopper stabilized op amp, the voltage at node X and Y is forced to be equal.

$V_X = V_Y = V_{BE1} = V_{BE2} + I_2R_3$, where $V_{BE} = V_T ln\frac{I_C}{I_S}$

Therefore,

$$V_{BE1} - V_{BE2} = V_T \ln(n) = I_2R_3, \qquad (\text{where } n = \frac{BJT_2(Area)}{BJT_1(Area)}) \tag{1}$$

The voltage difference between two pn junctions is the positive temperature coefficient voltage. Adding a positive temperature coefficient voltage I_2R_3 to a base emitter voltage, the negative temperature coefficient voltage, can achieve a temperature independent voltage.

$$V_{bgout} = V_{BE2} + \frac{V_T \ln(n)}{R_3}(R_2 + R_3)$$

$$= V_{BE2} + (1 + \frac{R_2}{R_3})V_T \ln(n) \tag{2}$$

For zero temperature coefficient,

$$\frac{\partial V_{bgout}}{\partial T} = \frac{\partial V_{BE2}}{\partial T} + \left(1 + \frac{R_2}{R_3}\right)\ln(n)\frac{\partial V_T}{\partial T} = 0 \tag{3}$$

$$\frac{\partial V_T}{\partial T} \approx +0.087\, mV/K \tag{4}$$

From simulations,

$$\frac{\partial V_{BE2}}{\partial T} \approx -1.85\, mV/K \qquad (\text{for } I_2 = 100\mu A \text{ and at } T = 60C(333K)) \tag{5}$$

To satisfy equation 3, $(1 + \frac{R_2}{R_3})\ln(n) = 21.26$

We have chosen $n = 35$, so $\frac{R_2}{R_3} \approx 5$ (6)

To set $I_2 = 100\mu A$, $R_3(= R_4) = 1066\ ohms$ is selected from equation $1(\Delta V_{BE} = 0.1066\ V$ from simulation), which gives $R_2(= R_1) \approx 5000\ ohms$.

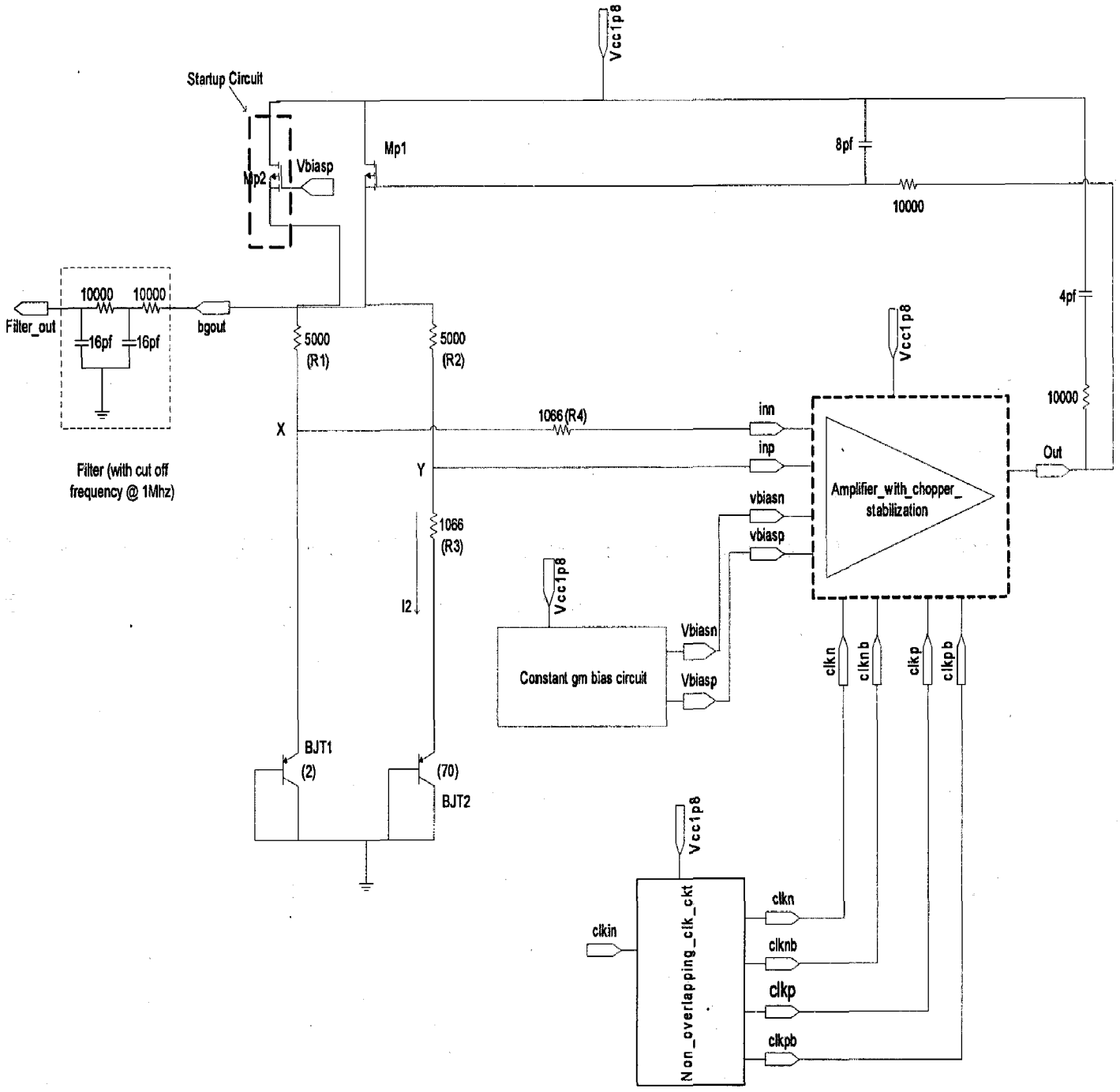

Figure 4.1: Bandgap reference circuit diagram

A start-up circuit has been added to the design to ensure correct operation of the circuit. The start-up circuit consists of transistor M_{p2}, which will leak some current into nodes X and Y to make sure that the loop starts and snap to the right voltage even if the output of the amplifier is close to V_{CC} when the supply is turned on.

4.2 Effect of Op Amp Offset on the Bandgap Output Voltage

The op amp suffers from input referred offset because of random mismatch. The input referred offset of the op amp introduces error in the output voltage of the bandgap. The offset (V_{OS}) is included in the figure 4.2.

$V_{BE1} - V_{OS} \approx V_{BE2} + R_3 I_2$ (if DC gain of amplifier is large)

$$V_{bgout} = V_{BE2} + (R_2 + R_3)\frac{V_{BE1} - V_{BE2} - V_{OS}}{R_3}$$

$$= V_{BE2} + \left(1 + \frac{R_2}{R_3}\right)(V_T \ln(n) - V_{OS})$$

Input referred offset of the op amp (V_{OS}) is amplified by $\left(1 + \frac{R_2}{R_3}\right)$ and introduces error in the output voltage of the bandgap. To lower the effect of offset, chopper stabilized op amp is used in the bandgap circuit.

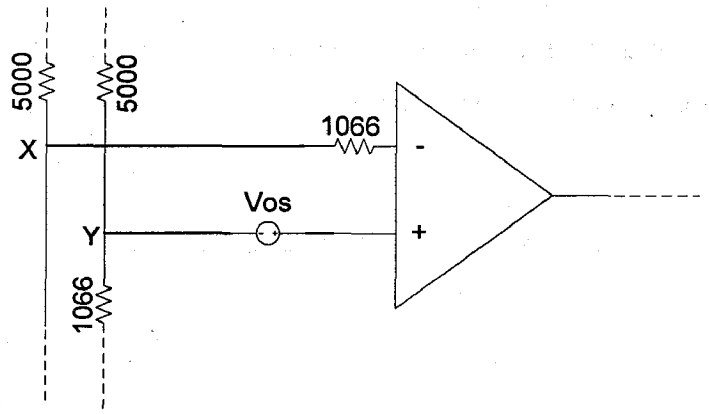

Figure 4.2: Effect of op amp offset on the reference voltage

4.3 Bandgap Stability Analysis

The open loop frequency response of the Bandgap reference circuit is measured by breaking the feedback loop as shown in figure 4.3. The DC value at the positive terminal of the op amp is set to the voltage obtained from the transient simulation (with loop closed). The measured Magnitude and Phase response is shown in figure 4.4.

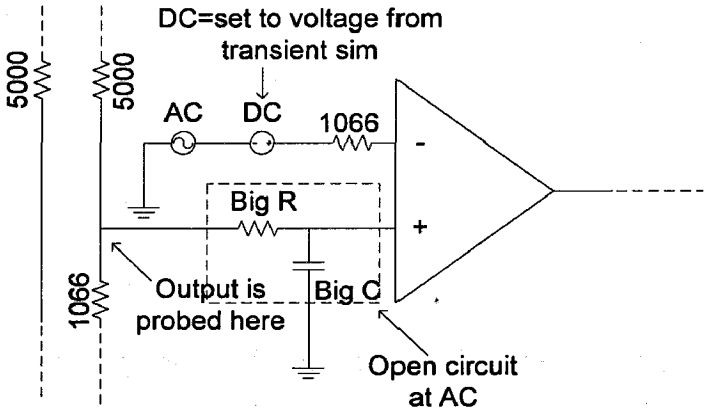

Figure 4.3: Open loop frequency analysis of Bandgap

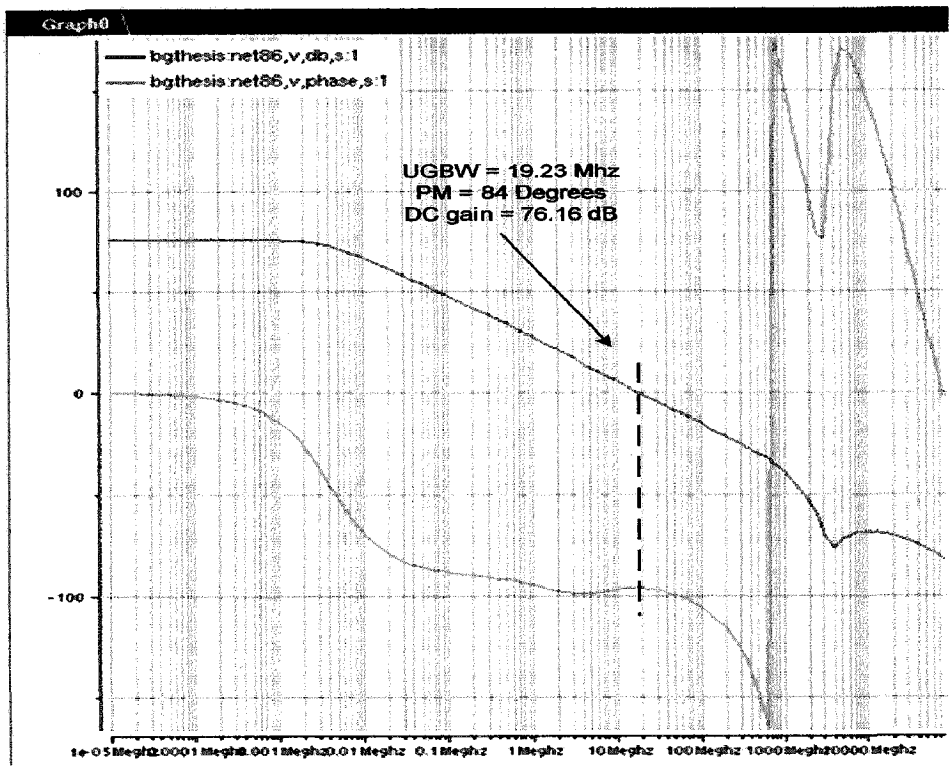

Figure 4.4: Bandgap Magnitude and Phase Response Vs Frequency

Table 4.1: Bandgap's open loop frequency response

Unity Gain Bandwidth (UGBW)	19.23 Mhz
DC Gain	76.16 dB
Phase Margin (PM)	84 Degrees
Power	2.4 mW

4.4 Bandgap Output Voltage Variation Analysis

4.4.1 Supply Voltage Variation of the Bandgap Output Voltage

Figure 4.5 shows the variation of the Bandgap output voltage with variation in the supply voltage. The Bandgap output voltage varies only 0.3 mV (~ 0.02 %) for 10% variation in the supply voltage.

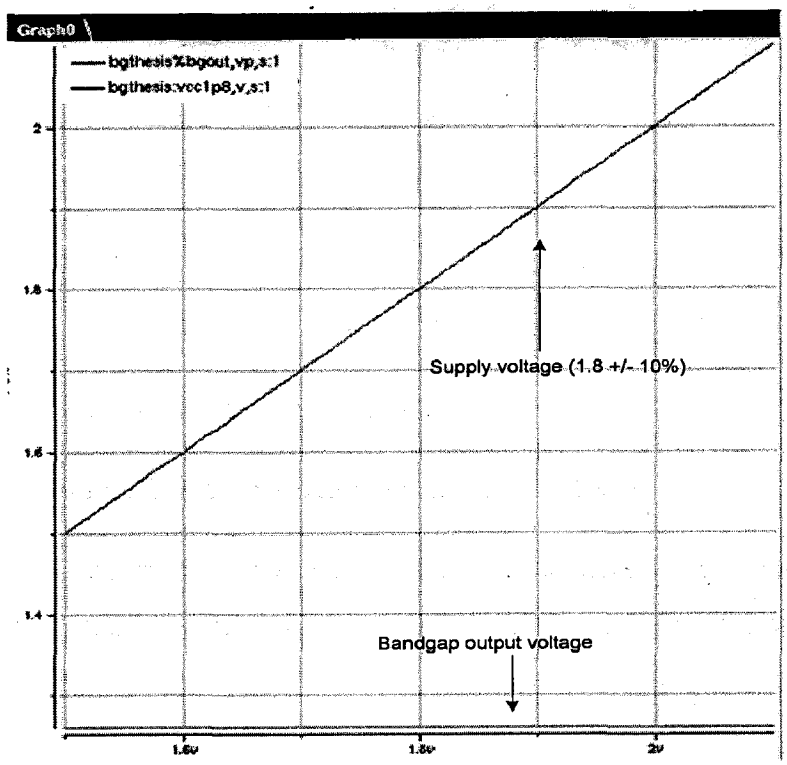

Figure 4.5: Bandgap output voltage variation with supply voltage

Table4.2: Bandgap output voltage accuracy Vs supply voltage variation

Supply voltage	Bandgap Output Voltage
V_{CC} (1.8 V)	1.2277 V
V_{CC} + 10% (1.98 V)	1.22772 V
V_{CC} − 10% (1.62 V)	1.22769 V

4.4.2 Temperature Variation of the Bandgap Output Voltage

The temperature variation of the Bandgap output voltage is shown in figure 4.6. The temperature coefficient of Bandgap output voltage is +41.63 ppm/C in the range -40C to 50C and -26.76 ppm/C for 50-120C .

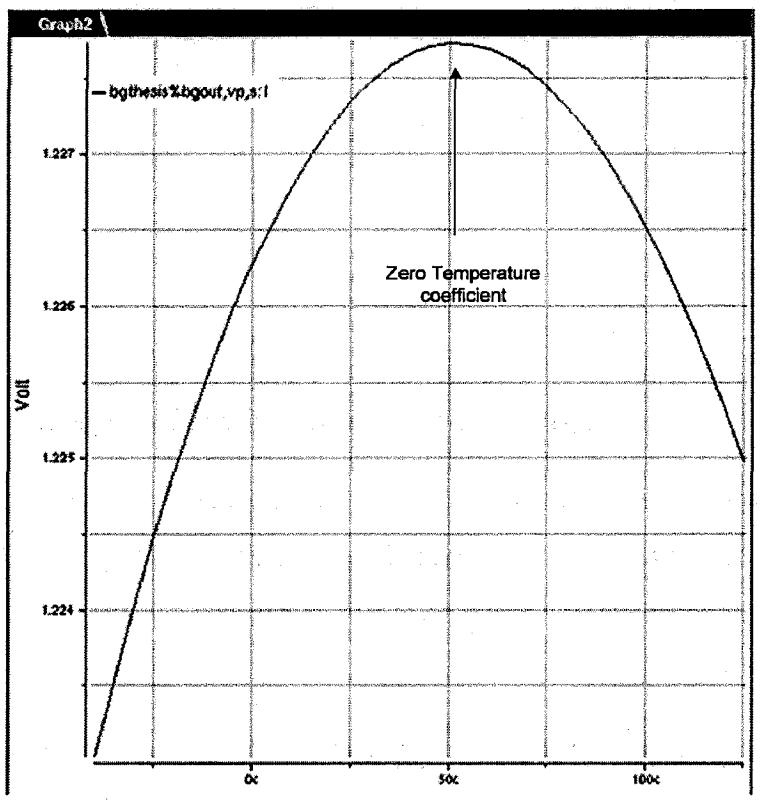

Figure 4.6: Temperature variation of the Bandgap output voltage

4.4.3 Bandgap Output Voltage Variation due to Random Mismatch

The op amp offset voltage due to random variations (V_t and length mismatch) of input transistors, NMOS current mirror and PMOS current mirror is measured by connecting the op amp in unity gain configuration using Monte Carlo simulation. The offset has Gaussian distribution with sigma (σ) = 9.1 mV.

The effect of random mismatch (of op amp) on the bandgap output voltage is shown in figure 4.7 obtained through Monte Carlo simulation. The op amp mismatch causes the output voltage of bandgap to vary by +/- 11.62%. This variation is caused by random mismatch and does not include any PVT variation.

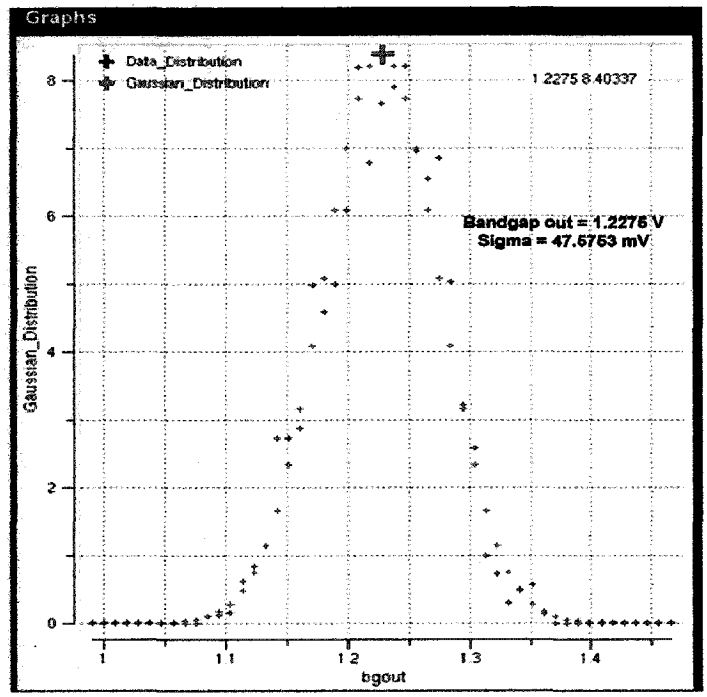

Figure 4.7: Bandgap output voltage due to op amp offset (with chopping off)

Table 4.3: Bandgap output voltage variation due to op amp mismatch

Bandgap output voltage accuracy	Δ_{bgout} (with chopping off)
3σ	142.71 mV (+/- 11.62 %)

The random mismatch is modeled in the circuit analysis with battery. If no random mismatch is modeled with the battery, the bandgap output voltage is 1.2277 V. When random mismatch is modeled using battery of 27.3 mV (-27.3 mV) [3σ value of op amp offset] for positive (negative) polarity of offset, then bandgap output shifts to 1.0471 V (1.3997 V). When chopping is enabled, the average bandgap output voltage becomes 1.2276 V (1.2275 V). Chopping corrects the error of 180 mV (172 mV) in bandgap output voltage due to random mismatch to within 1 mV of the ideal value (without any mismatch). Chopping almost completely eliminates the effect of random mismatch on bandgap output voltage. A second order RC low pass filter with cut off frequency of 1 Mhz is placed at the bandgap output to filter out the high frequency components (generated because of chopping).

Table 4.4: Bandgap output voltage variation due to op amp mismatch

Bandgap output voltage accuracy	Δ_{bgout} (with chopping off)	Δ_{bgout} (with chopping on)
3σ	142.71 mV (+/- 11.62 %)	~ 0.2 mV (+/- 0.08%)

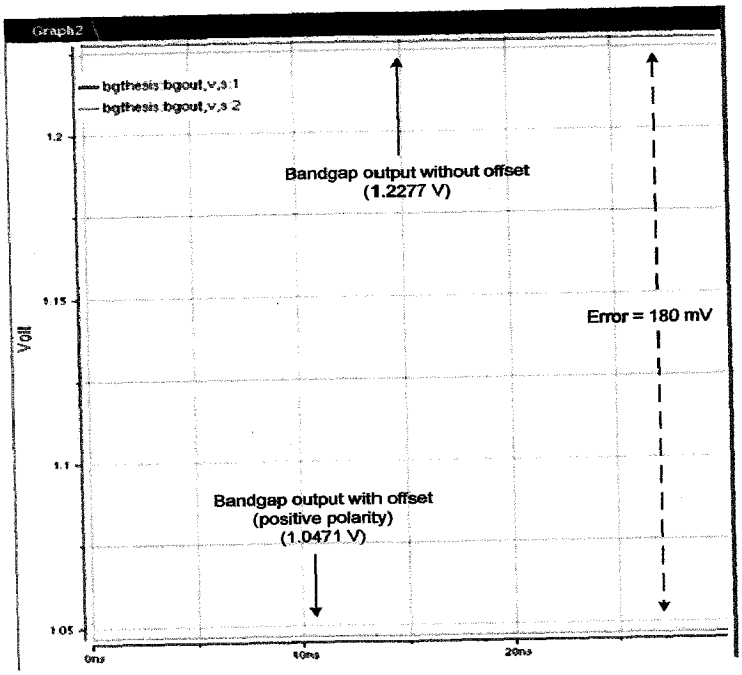

Figure 4.8: Bandgap output voltage with positive offset (chopping off)

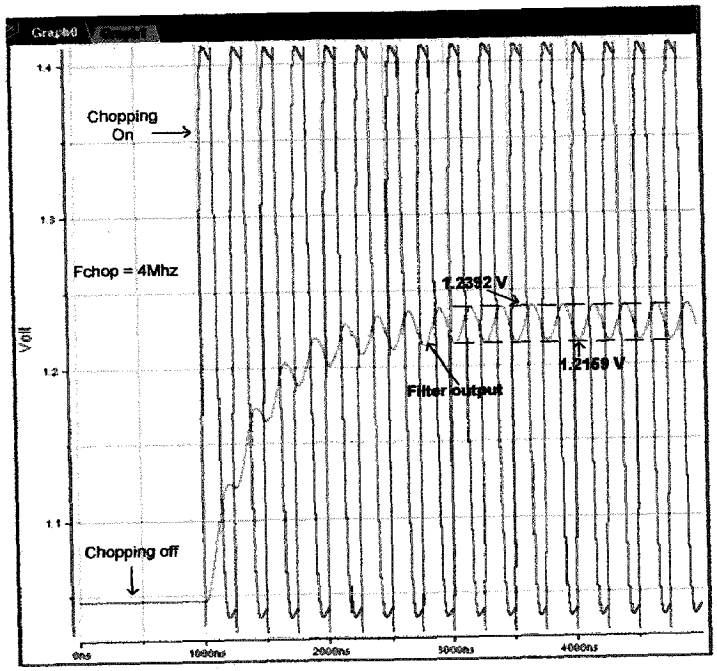

Figure 4.9: Bandgap output voltage with positive offset (chopping on)

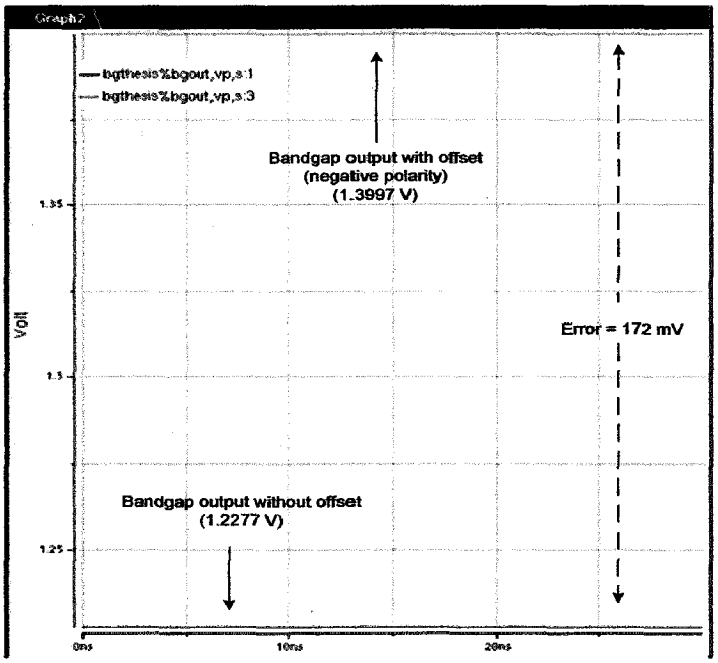

Figure 4.10: Bandgap output voltage with negative offset (chopping off)

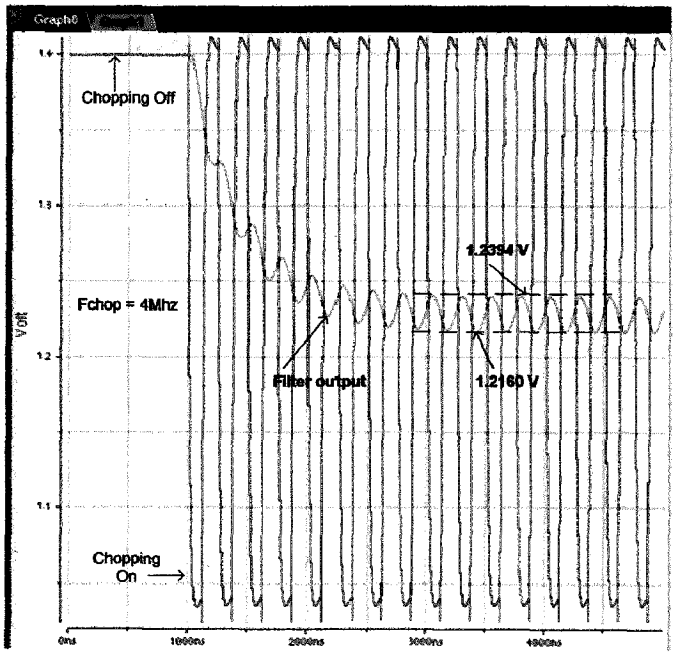

Figure 4.11: Bandgap output voltage with negative offset (chopping on)

CHAPTER 5

5.1 Conclusion

To mitigate the impact of random variations on op-amps, a design technique – chopper stabilization is used in this work. In chopper stabilization, the inputs to a differential amplifier are swapped, or chopped, under the control of a clock signal. The same clock signal is used to swap the outputs, and then the results are low pass filtered.

This work presents the design of a chopper stabilized operational amplifier. The operational amplifier is built upon a folded-cascode amplifier core. Gain boosting technique is used to increase the gain of the operational amplifier. Constant g_m circuit is used to generate the bias voltages for the operational amplifier. The input referred offset of the proposed chopper stabilized op amp is obtained through Monte Carlo simulation (with chopping off). The input referred offset has a sigma (σ) of 9.1 mV.

The proposed amplifier is designed in Intel's 32 nm CMOS process technology and is used to design a bandgap reference circuit. The effect of random mismatch (of op-amp) on the bandgap reference voltage is obtained through Monte Carlo simulations. The bandgap reference voltage shows a 3σ variation of 142.71 mV (+/- 11.62%) (with chopping off). Chopper stabilization improved the accuracy of the bandgap reference voltage from +/- 11.62% (3σ variation due to random mismatch only) to less than +/- 0.02%.

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