A RECONFIGURATION TECHNIQUE FOR MULTILEVEL INVERTER INCORPORATING A DIAGNOSTIC SYSTEM BASED ON ANFIS

A DISSERTATION

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CANDIDATE'S DECLARATION

I hereby declare that the work presented in this dissertation report entitled **"A Reconfiguration Technique for Multilevel Inverter Incorporating a Diagnostic System Based on ANFIS"** submitted for the award of the degree of **Master of Technology** with specialization in **Control & Guidance** in the department of Electronics & Computer Engineering, **Indian Institute of Technology Roorkee,** is an authentic record of my own work carried out from June 2009 to June 2010, under the guidance of **Dr. Vijay kumar,** Department of Electronics & Computer Engineering, Indian Institute of Technology Roorkee.

I have not submitted the mater embodied in this dissertation for the award of any other degree.

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CERTIFICATE

This is to certify that the above statement made by the candidate is true to the best of my knowledge and belief.

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ABSTRACT

Multilevel Inverter have become a research hotspot in high voltage and high power applications because of their many advantages, such as their low voltage stress on power switches, low harmonic and EMI output. However, the increasing of the power devices improves the system's fault rate. How to ensure stable operation of the system has become an important research question.

In this thesis work, a fault diagnostic system in a multilevel-inverter using Fuzzy inference System and an Adaptive Neuro Fuzzy Inference System are developed. These techniques are applied to the fault diagnosis of a Multi Level Inverter (MLI) system to avoid the difficulties in using mathematical models. This thesis work presents a fault detection method for open-circuit and short circuit faults of a switching device in diode-clamped inverter systems, which is based on the inherent characteristic of continuous pulse width modulation and its reconfiguration method to avoid feeding faulted output to load.

The phase-to-phase and phase-to-Neutral voltages include information of switching states in the inverter system corresponding to their respected legs but not affected by the load. Therefore, a fault condition of the inverter system itself can be diagnosed through analysis of any of these voltages. Compared to conventional fault detection methods, the present fault detection method has faster detection capability that is within 1 cycle period it can detect the fault and is much simpler to implement. Therefore, the use of the method presented could minimize harmful effects such as imbalance of dc-link voltage and overstress on other switching devices.

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INTRODUCTION

In recent years, industry has begun to demand higher power ratings, and multilevel inverter drive (MLID) systems have become a solution for high-power applications. The results of a patent search show that multilevel inverter circuits have been around for more than 25 years. An early traceable patent appeared in 1975, in which the cascade inverter was first defined with a format that connects separately dc-sourced full-bridge cells in series to synthesize a staircase ac output voltage. Through manipulation of the cascade inverter, with diodes blocking the sources, the diode-clamped multilevel inverter was then derived. The diode-clamped inverter was also called the neutral-point clamped (NPC) inverter when it was first used in a three-level inverter in which the mid-voltage level was defined as the neutral point. Because the NPC inverter effectively doubles the device voltage level without requiring precise voltage matching, the circuit topology prevailed in the 1980s. The cascade MLID is a general fit for large automotive all-electric drives because of the high Volt-Ampere (VA) rating possible and because it uses several level dc voltage sources which would be available from batteries or fuel cells. Mainly three-phase Pulse Width Modulated (PWM) inverters have been utilized in variety of industrial applications like Uninterrupted Power supply (UPS), electric motor drives and active power filters and so on. Due to environmental pollution and exhaustion of fossil fuel, inverters are being used for renewable energy conversion systems and hybrid vehicles. Various control techniques have been implemented to reduce the harmonics. A multilevel inverter not only achieves high power ratings, but also enables the use of renewable sources [1].

However, different types of unexpected faults are frequent in industrial fields. These inverter faults may influence the operation of whole system. In order to avoid these harmful effects and to improve the reliability the fault detection and diagnosis are very important.

Different faults in 3-phase inverters are classified in to

- Single-line-to ground faults of input supply
- Short-circuit faults of diode rectifier
- Earth faults of input supply
- Earth faults on dc-bus
- Short-circuit faults of dc-link capacitors
- Switching device faults
- Line-to-line short circuits at machine terminals
- Single line-to-ground faults at machine terminals, etc.

Our main concentration is on switching device faults which occurs inside the inverters. Switching device faults results in harmonics in the output voltage and currents. In this research, we will attempt to diagnose the fault location in a Multi Level Inverter (MLI) system from its output voltage waveform because the output voltages are normally independent from the load and correspond with fault types and locations. MLI open and short circuit faults at each switch are considered. The proposed Fault diagnostic system utilizes output voltage signals of the MLI systems to detect the fault location in the inverter. The unbalanced voltage and current may result in vital damage because of overheating in the ac load if the ac load is supplied with unbalanced voltages for a long time. The unbalanced condition from fault can be corrected if the fault location is identified.

A voltage-fed inverter system, as shown in Fig.1.1, can develop various types of switching device faults that can be classified as follows:

1) Open-circuit fault of semiconductor device
2) Short-circuit fault of semiconductor device
3) Two semiconductor device of one leg open-circuit fault

In order to maintain continuous operation for a multilevel inverter system, knowledge of fault behaviors, fault prediction, and fault diagnosis are necessary. So the

most important factor, however, is how the system could operate continuously while there is an abnormal condition.

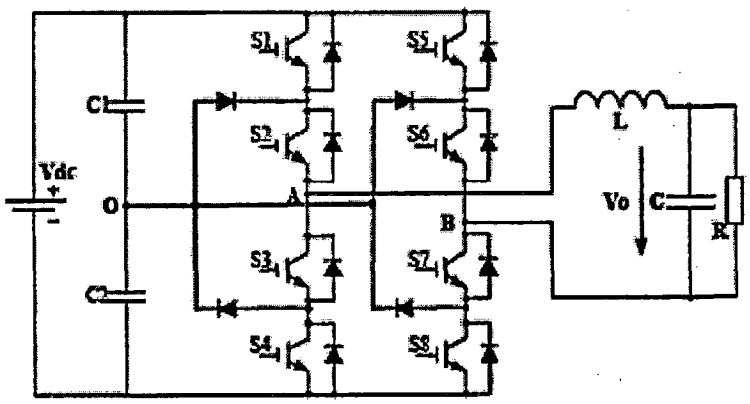

Fig.1.1. Single-phase multilevel-inverter system.

Faults should be detected and corrected and the faulted part should be isolated as soon as possible after they occur, because if a motor drive runs continuously under abnormal conditions, the drive or motor may quickly fail. Many engineers and researchers have focused on incipient fault detection and preventive maintenance to avert inverter and motor faults [4]-[6].

Research on fault diagnostic techniques initially focused on conventional pulse width modulation (PWM) voltage source inverters (VSI). This integrated system introduced remedial control strategies soon after failure occurrences; therefore system reliability and fault tolerant capability are improved.

Three different methods which are mainly used for in fault detection and diagnosis are model-based techniques, expert systems, and artificial intelligence methods. Model-based techniques are very outstanding if an accurate model of the process can be obtained. But accurate model of the whole Inverter system is difficult to obtain. The inverter model (including Snubber capacitance and power electronic switches) is not only hard to obtain but also inaccurate due to component values, parasitic components, and unavoidable assumptions and limitations. Therefore, methods that do not require model knowledge are of great interest. Expert systems usually

dedicated to big systems are useful if minor modifications are made in the process and above all assume the existence of an expert to build the rules and the reasoning tree. The introduction of artificial intelligence methods (fuzzy logic and artificial neural network) will have more flexibility, as there is no need for a model. The accuracy of these methods depends upon the initial training data in healthy and faulty conditions. Nevertheless, this is not a major drawback in this case because reliable simulation tools exist that can furnish appropriate data. A general review of recent developments in the field of AI-based diagnostic systems in machine drives has been proposed in [9].

Thus far, limited research has focused on MLI systems fault diagnosis. Therefore, an MLI fault diagnostic system is discussed in this thesis work that only requires measurement of the MLI's voltage waveforms.

1.1 Problem Description

Because multilevel inverter systems are utilized in high power applications, the reliability of the power electronics is very important. For example industrial applications such as industrial manufacturing are dependent upon induction motors and their inverter systems for process control. Generally, the conventional protection systems are passive device such as fuses, overload relays, and circuit breakers to protect the inverter systems and the induction motors. The protection devices will disconnect the power sources from the multilevel inverter system whenever a fault occurs, stopping the operated process. Downtime of manufacturing equipment can add up to be thousands or hundreds of thousands of dollars per hour, therefore fault detection and diagnosis is vital to a company's bottom line.

The inverter switching devices are normally controlled by isolated base drive amplifiers. Malfunctioning of one of these units can result in a missing base drive, and so device open-circuit fault occurred in the inverter. It may also occur by several reasons such as lifting of bonding wires due to thermal cycling, drive failures, and IGBT breakage due to short-circuit faults, etc. Open-circuit faults might cause the system shut-down depending on the state of system, however the system can also keep operating under the fault since it doesn't always result in the incapability of system operation. But

it may lead to the secondary faults such as thermal defects of the other switches, winding and bearing faults of the motor and so on, by continuous operation without any recovery. Usually, a diagnosis of open-circuit faults of the switching devices is based on the current signal.

The device short-circuit fault is due to reverse breakdown of the device, or may due to insulation breakdown of the leg, or sucking circuit paralleling with the device is short. This type of fault is a serious fault and it may be resulting in fault of other device. Unfortunately it is also a commonly occurring fault. For such a fault, base drive to the healthy IGBT of the same leg should be immediately suppressed in order to prevent a shoot through fault [7]-[24].

A 3-phase MLI system (3-level) using diode-clamped technique is represented in Fig.1.2 is able to generate 3-level staircase form of voltage which is nearly sinusoidal which are displaced by 120° apart. By increasing the number of levels we can reduce the harmonic content present in the output. Due to the great demand of medium-voltage high-power inverters, the inverter has drawn tremendous interest ever since. The field applications include use in laminators, mills, conveyors, pumps, fans, blowers, compressors, and so on [3]-[8].

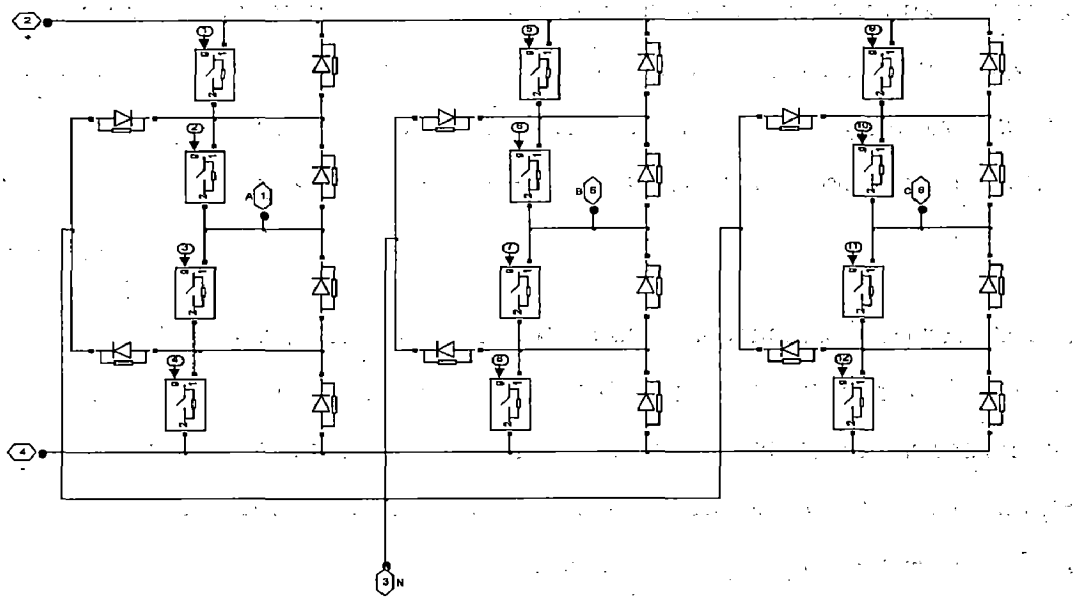

Fig.1.2. 3-phase multilevel-inverter system.

However, the use of inverters has some drawbacks. The introduction of power electronic converters came with an increased possibility of component failures. It is the power electronic stage of the drive, including its dc link and control circuitry, which becomes the system's weakest part in the sense of operational reliability. High costs due to standstill and repair, as well as the general need to improve reliability have led to research in fault detection in inverters. Short circuit detection has become a standard feature of driver ICs. However, much fewer research results have been published on open circuit faults. An open switch fault can lead to over stresses on the healthy switches as well as to pulsating current. In turn this can lead to failures in other components, for example by causing a torque ripple in a drive fed by such inverter [25].

1.2 Organization of the Thesis

Chapter 1 introduces to the prominence of the inverters and major changes that have been undergone over past 50 years and different causes for faults in inverters. Chapter 2 gives the literature survey I have done on different topologies, inverter applications and controlling techniques from various IEEE papers which I studied for the work. In chapter 3 it gives the general discussion about 3-level inverter and its operation using Sinusoidal Pulse Width Modulation (SPWM) control techniques in order to control the output voltage of the 3-level inverter, the Simulink models designed for three-level inverters with SPWM technique and the results obtained from the simulation of the block models in MATLAB/SIMULINK 7.1 version. Chapter 5 deals with different fault detection methods and its importance and proposed two techniques for detection of fault location. They are Adaptive Neuro Fuzzy Inference Systems which uses Fast Fourier Transform (FFT) analysis and Fuzzy Inference System which uses 3rd harmonic content present in the output voltages. Chapter 5 deals with different reconfiguration techniques. In Chapter 6 concludes the thesis work and scope for future work drawn is drawn.

A SURVEY OF TOPOLOGIES, CONTROL METHODS, APPLICATIONS AND THEIR SIMULINK MODELS

As the demand for higher power equipment has been increasing rapidly, this may be up to the megawatt level. Controlled ac drives in the megawatt range are usually connected to the medium-voltage network. Today, it is difficult to connect a single power semiconductor switch directly to medium voltage grids (2.3, 3.3, 4.16, or 6.9 kV). Due to these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels [1].

Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages. Fig.2.1 shows a schematic diagram of one phase leg of inverters with different numbers of levels, for which the action of the power semiconductors is represented by an ideal switch with several positions. A two-level inverter generates an output voltage with two values (levels) with respect to the negative terminal of the capacitor [see Fig. 2.1(a)], while the three-level inverter generates three voltages, and so on. Considering that m is the number of steps of the phase voltage with respect to the negative terminal of the inverter, then the number of steps in the voltage between two phases of the load k is

$$k=2m+1$$

And the number of steps in the phase voltage of a three-phase load in Y connection is

$$p=2k-1$$

By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveform, which has a reduced harmonic distortion. However, a high number of levels increases the control complexity and introduces

voltage imbalance problems [1]. Three different topologies for multilevel inverters are diode-clamped (neutral-clamped), capacitor- clamped (flying capacitors) and cascaded Multicell with separate dc sources [16].

The most attractive features of multilevel inverters are as follows.

- They can generate output voltages with extremely low distortion and lower dv/dt.
- They draw input current with very low distortion.
- They generate smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods, CM voltages can be eliminated.
- They can operate with a lower switching frequency.

This dissertation work presents state of the art multilevel technology, considering well-established and emerging topologies as well as their modulation and control techniques. Special attention is dedicated to the latest and more relevant industrial applications of these converters.

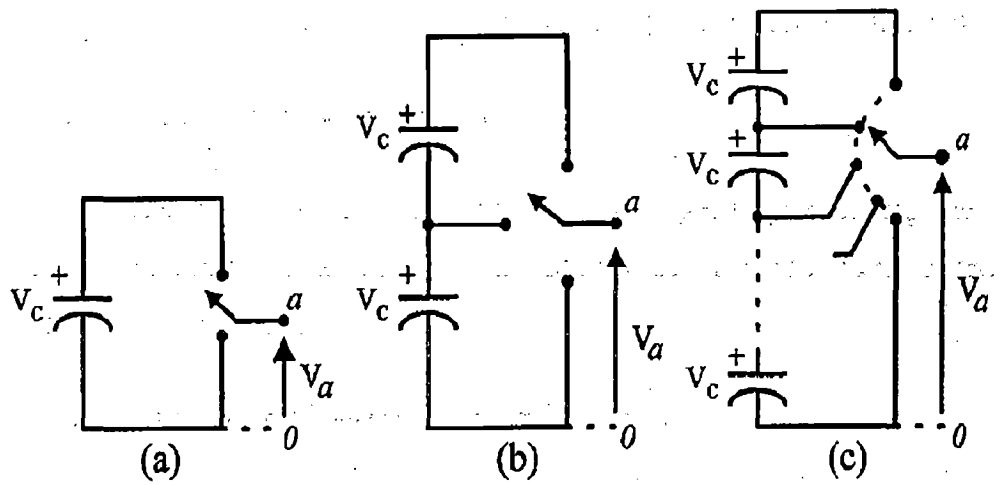

Fig.2.1. One phase leg of an inverter with (a) two levels, (b) three levels, and (c) n levels.

From Fig. 2.1(a) as there is only one charging capacitor which acts as dc source, the output will be a single level. As the number of charging capacitors increases there

will be a proportionate increment in switches this in turn produce a multi level output. If there are 'n' numbers of switches, the output stages will be of 2n+1[1].

2.1 Inverter Topologies

2.1.1 Diode-Clamped Inverter

A three-level diode-clamped inverter is shown in Fig. 2(a). In this circuit, the dc-bus voltage is split into three levels by two series-connected bulk capacitors, C_1 and C_2. The middle point of the two capacitors 'n' can be defined as the neutral point. The output voltage V_{an} has three states: $V_{dc}/2$, 0, $-V_{dc}/2$. For voltage level $V_{dc}/2$, switches $S_1$and S_2 need to be turned on; for $-V_{dc}/2$, switches S_1' and S_2' need to be turned on; and for the 0 level, S_2 and S_1' need to be turned on.

The key components that distinguish this circuit from a conventional two-level inverter are D_1 and D_1'. These two diodes clamp the switch voltage to half the level of the dc-bus voltage. When both $S_1$and S_2 turned on, the voltage across 'a' and '0' is V_{dc} i.e., in this case, D_1' balances out

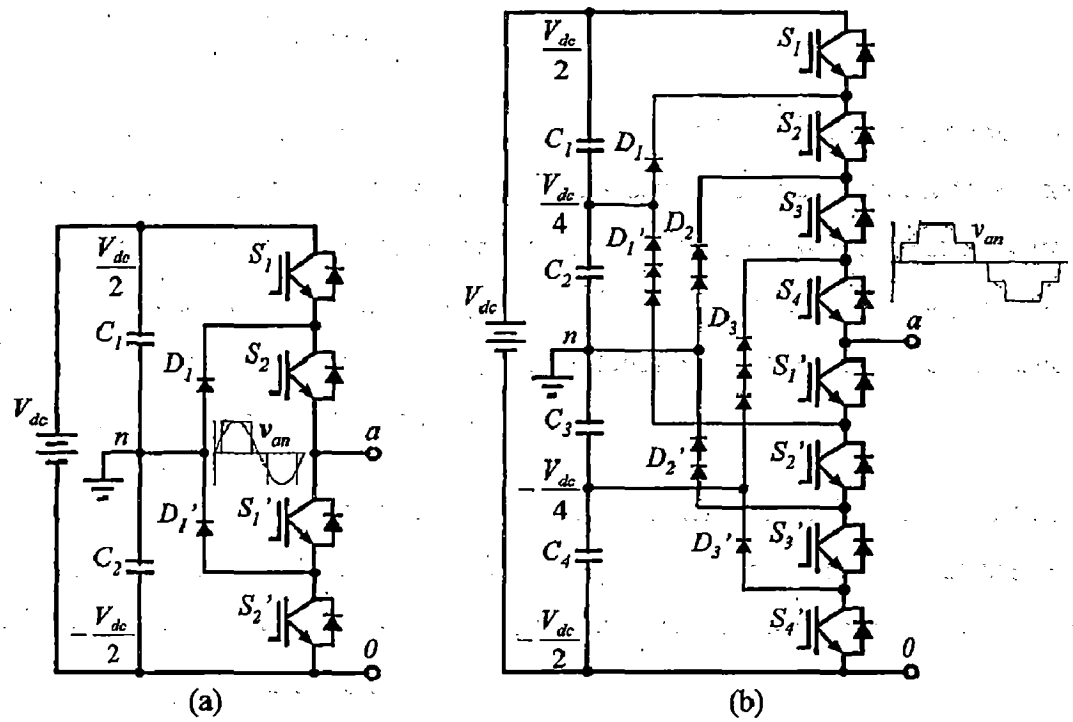

Fig.2.2. Diode-clamped multilevel inverter circuit topologies. (a) Three-level. (b) Five-level.

The voltage sharing between S_1'and S_2'with S_1'blocking the voltage across $C_1$and S_2' blocking the voltage across C_2. Notice that output voltage V_{an} is ac, and $V_{a0}$is dc. The difference between V_{an} and V_{a0} is the voltage across C_2, which is $V_{dc}/2$. If the output is removed out between 'a' and '0', then the circuit becomes a dc/dc converter, which has three output voltage levels: V_{dc}, $V_{dc}/2$, and 0.

Fig.2.2(b) shows a five-level diode-clamped converter in which the dc bus consists of four capacitors, C_1, C_2, C_3, and C_4. For dc-bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/4$, and each device voltage stress will be limited to one capacitor voltage level $V_{dc}/4$ through clamping diodes. To explain how the staircase voltage is synthesized, the neutral point n is considered as the output phase voltage reference point. There are five switch combinations to synthesize five level voltages across a and n.

For voltage level $V_{an}=V_{dc}/2$, turn on all upper switches S_1–S_4.

For voltage level $V_{an}=V_{dc}/4$, turn on three upper switches S_2–S_4, one lower switch S_1'.

For voltage level $V_{an}=0$, turn on two upper switches S_3–S_4, two lower switches S_1'– S_2'.

For voltage level $V_{an}=-V_{dc}/4$, turn on one upper switch S_4, three lower switches S_1 –S_3'.

For voltage level $V_{an}=-V_{dc}/2$, turn on all lower switches S_1'–S_4'.

Four complementary switch pairs exist in each phase. The complementary switch pair is defined such that turning on one of the switches will exclude the other from being turned on. In this example, the four complementary pairs are (S_1, S_1'), (S_2, S_2'), (S_3, S_3'), and (S_4, S_4') although each active switching device is only required to block a voltage level of $V_{dc}/(m-1)$, the clamping diodes must have different voltage ratings for reverse voltage blocking. Using D_1'of Fig.2.2(b) as an example, when lower devices S_2'-S_4' are turned on, D_1'needs to block three capacitor voltages, or $3V_{dc}/4$. Similarly, D_2 and D_2' need to block $2V_{dc}/4$, and D3 needs to block $3V_{dc}/4$. Assuming that each blocking diode voltage rating is the same as the active device voltage rating, the number of diodes required for each phase will be (m-1)*(m-2).

This number represents a quadratic increase in m. When m is sufficiently high, the number of diodes required will make the system impractical to implement. If the inverter runs under PWM, the diode reverse recovery of these clamping diodes becomes the major design challenge in high-voltage high-power applications [1]-[2].

2.1.2. Capacitor-Clamped Inverter

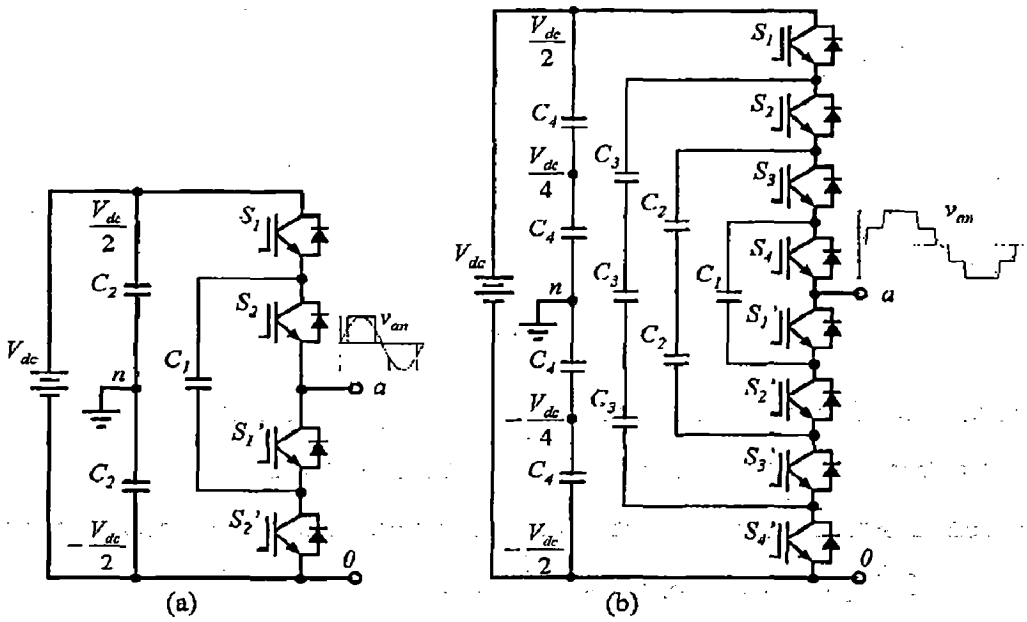

Fig.2.3. Capacitor-clamped multilevel inverter circuit topologies. (a)Three-level (b) Five-level

Fig. 2.3 illustrates the fundamental building block of a phase-leg capacitor-clamped inverter. The circuit has been called the flying capacitor inverter with independent capacitors clamping the device voltage to one capacitor voltage level. The inverter in Fig.2.3(a) provides a three-level output across 'a' and 'n', i.e., $V_{an}=V_{dc}/2$, 0, or $-V_{dc}/2$. For voltage level $V_{dc}/2$, switches $S_1$and S_2 need to be turned on; for $-V_{dc}/2$, switches S_1'and S_2' need to be turned on; and for the 0 level, either pair (S_1, S_1') or (S_2, S_2') needs to be turned on. Clamping capacitor C_1 is charged when S_1 and S_1'are turned on, and is discharged when S_2 and S_2' are turned on. The charge of C_1 can be balanced by proper selection of the 0-level switch combination.

The voltage synthesis in a five-level capacitor-clamped converter has more flexibility than a diode-clamped converter. Using Fig. 2.3(b) as the example, the voltage

of the five-level phase-leg output with respect to the neutral point n, V_{an}, can be synthesized by the following switch combinations [1]-[2].

1) For voltage level Van=V_{dc}/2, turn on all upper switches S_1 –S_4.

2) For voltage level V_{an}=V_{dc}/4, there are three combinations:

S_1, S_2, S_3, S_1' (V_{an}=V_{dc}/2 of upper C_4's –V_{dc}/4 of C_1);

S_2, S_3, S_4, S_4' (V_{an}=3V_{dc}/4 of C_3's –V_{dc}/2 of lower C_4's); and

S_1, S_3, S_4, S_3' (V_{an}=V_{dc}/2 of upper C_4's -3V_{dc}/4 of C_3's +V_{dc}/2 of C_2's).

3) For voltage level V_{an}=0, there are six combinations:

S_1, S_2, S_1', S_2' (V_{an}=V_{dc}/2 of upper C_4's –V_{dc}/2 of C_2's);

S_3, S_4, S_3', S_4' (V_{an}=V_{dc}/2 of C_2 –V_{dc}/2of lower C_4);

S_1, S_3, S_1', S_3' (V_{an}=V_{dc}/2 of upper C_4's -3V_{dc}/4 of C_3's V_{dc}/2 of C_2's –V_{dc}/4 of C_1);

S_1, S_4, S_2', S_3' (V_{an}=V_{dc}/2 of upper C_4's -3V_{dc}/4 of C_3's +V_{dc}/4 of C_1);

S_2, S_4, S_2', S_4'(V_{an}=3V_{dc}/4 of C_3's –V_{dc}/2 of C_2's +V_{dc}/4 of C_1 –V_{dc}/2 of lower C_4's);
S_2, S_3, S_1', S_4'(V_{an}=3V_{dc}/4 of C_3's of –V_{dc}/4 of C_1 –V_{dc}/2 of lower C_4's).

4) For voltage level V_{an}= -V_{dc}/4, there are three combinations:

S_1, S_1', S_2', S_3'(V_{an}= V_{dc}/2 of upper C_4's -3V_{dc}/4 of C_3's);

S_4, S_2', S_3', S_4'(V_{an}= V_{dc}/4 of C_1 –V_{dc}/2 of lower C_4's); and

S_3, S_1', S_3', S_4'(V_{an}=V_{dc}/2 of C_2's –V_{dc}/4 of C_1 –V_{dc}/2 of lower C_4's).

5) For voltage level V_{an}= -V_{dc}/2, turn on all lower switches, S_1'– S_4'.

In the preceding description, the capacitors with positive signs are in discharging mode, while those with negative sign are in charging mode. By proper selection of

capacitor combinations, it is possible to balance the capacitor charge. Similar to diode clamping, the capacitor clamping requires a large number of bulk capacitors to clamp the voltage. Provided that the voltage rating of each capacitor used is the same as that of the main power switch, an m-level converter will require a total of (m-1)*(m-2)/2 clamping capacitors per phase leg in addition to (m-1) main dc-bus capacitors.

2.1.3. Cascaded Multilevel Inverters

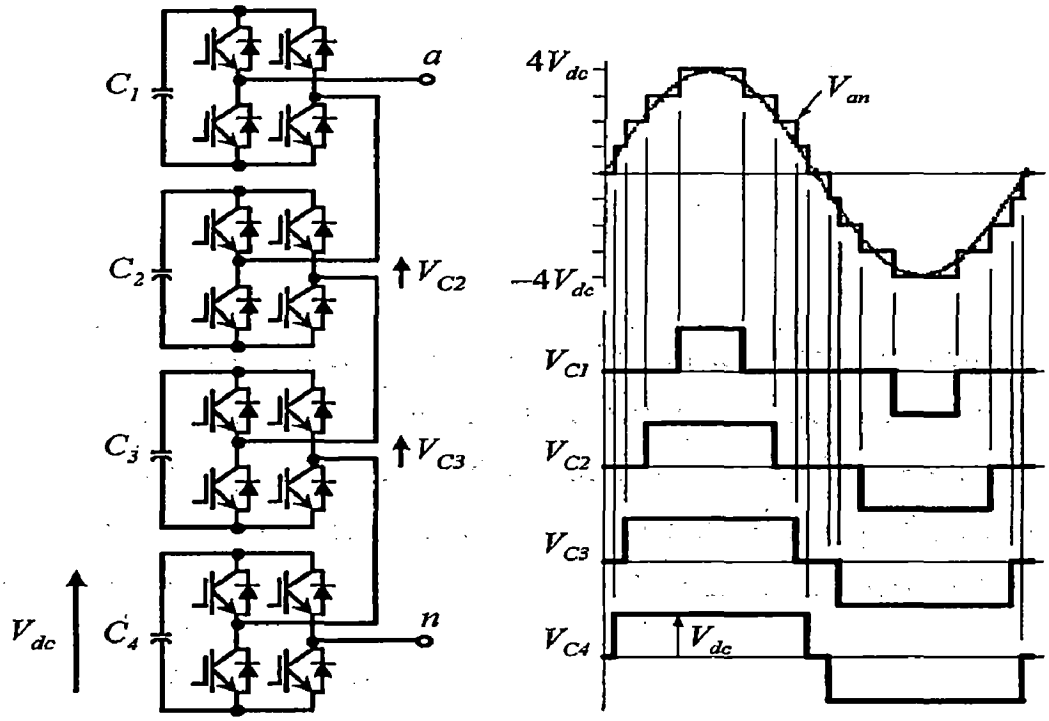

Fig.2.4. Cascaded inverter circuit topology and its associated waveform

A different converter topology is introduced here, which is based on the series connection of single-phase inverters with separate dc sources. Fig.2.4 shows the power circuit for one phase leg of a nine-level inverter with four cells in each phase. The resulting phase voltage is synthesized by the addition of the voltages generated by the different cells. Each single-phase full-bridge inverter generates three voltages at the output: $+V_{dc}$, 0, and $-V_{dc}$. This is made possible by connecting the capacitors sequentially to the ac side via the four power switches. The resulting output ac voltage swings from-$4V_{dc}$ to -$4V_{dc}$ with nine levels, and the staircase waveform is nearly sinusoidal, even without filtering [1]-[2]-[3].

2.2 Control Methods for Inverter

Different modulation methods used in multilevel inverters can be classified according to switching frequency is shown in Fig.2.5. Methods that work with high switching frequencies have many commutations for the power semiconductors in one period of the fundamental output voltage.

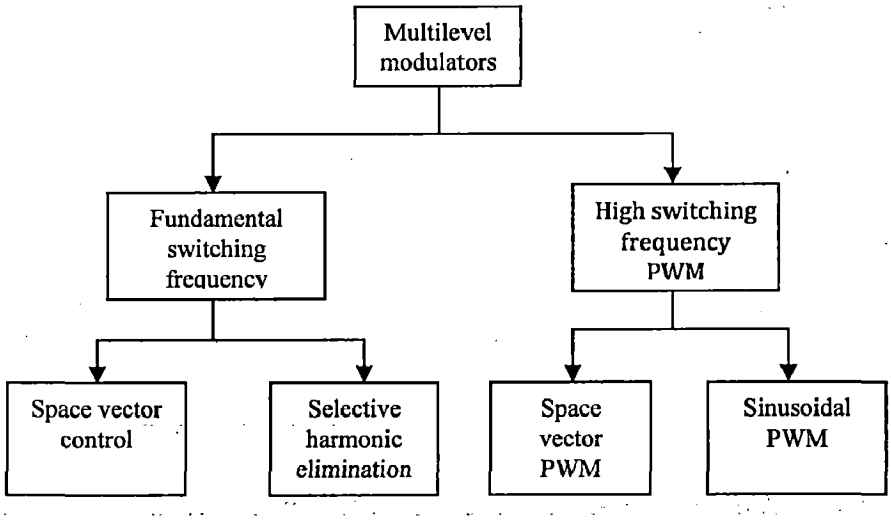

Fig.2.5. Classification of multilevel modulation methods.

A very popular method in industrial applications is the classic carrier-based Sinusoidal Pulse Width Modulation (SPWM) that uses the phase shifting technique to reduce the harmonics in the load voltage. Another interesting alternative is the Space Vector Pulse Width Modulation (SVM) strategy, which has been used in three-level inverters. Methods that work with low switching frequencies generally perform one or two commutations of the power semiconductors during one cycle of the output voltages, generating a staircase waveform. Selective harmonic elimination and the space-vector control (SVC) are the different modulation techniques in this family [1].

2.2.1 Need for the Control of the Inverter

In many industrial applications, it is often required to vary the output voltage of the inverter due to the following reasons:

- To compensate for the variations in the input voltage.

- To compensate for the regulation of the inverters.
- To supply some special loads which need variation of voltage with frequency, such as an induction motor.

The inverter output voltage can be controlled by various techniques. Here we use SINE-PWM technique for control of the inverter.

2.2.2 Sinusoidal Pulse Width Modulation

Pulse width modulation (PWM) techniques are effective means to control the output voltage frequency and magnitude. It has been the subject of intensive research during the last few decades. Here we mainly consider the carrier based PWM approaches that are often applied to the single phase applications [15].

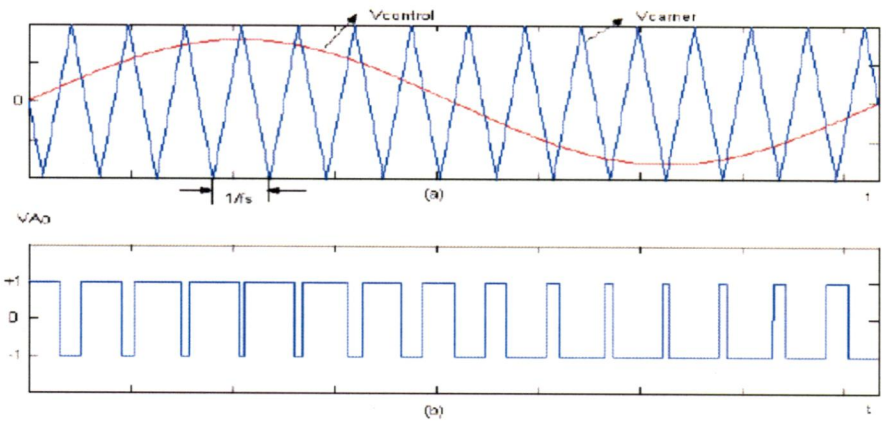

Fig.2.6. a Reference and carrier wave b .Pulses generated on comparison

Fig.2.6 is a general scheme of PWM modulation. In order to produce a sinusoidal voltage at desired frequency, say f_1, a sinusoidal control signal $V_{control}$ at the desired frequency (f_1) is compared with a triangular waveform $V_{carrier}$ as shown in Fig.2.7, at each compare match point, a transition in PWM waveform is generated as shown in Fig.2.7. When $V_{control}$ is greater than $V_{carrier}$, the PWM output is positive and When $V_{control}$ is smaller than $V_{carrier}$, the PWM waveform is negative. The frequency of triangle waveform $V_{carrier}$ establishes the inverter's switching frequency f_s. We define the modulation index m_i as follows:

$$m_i = V_{control} / V_{tri}$$

Where $V_{control}$ is the peak amplitude of the control signal, while V_{tri} is the peak amplitude of the triangle signal (carrier), the frequency modulation ratio is defined as

$$m_f = f_s / f_1$$

m_f is the ratio between the carrier and control frequency. The fundamental component $(V_{out})_1$ of the H bridge output voltage $(V_{out})_1$ has the property as depicted in equation below in a linear modulation region:

$$(V_{out})_1 = m_i * V_d$$

$$m_i < 1.0$$

This equation shows an interesting result that the amplitude of the fundamental component of the output voltage varies linearly with the modulation index. The m_i value from zero to one is defined as the linear control range of sinusoidal carrier PWM.

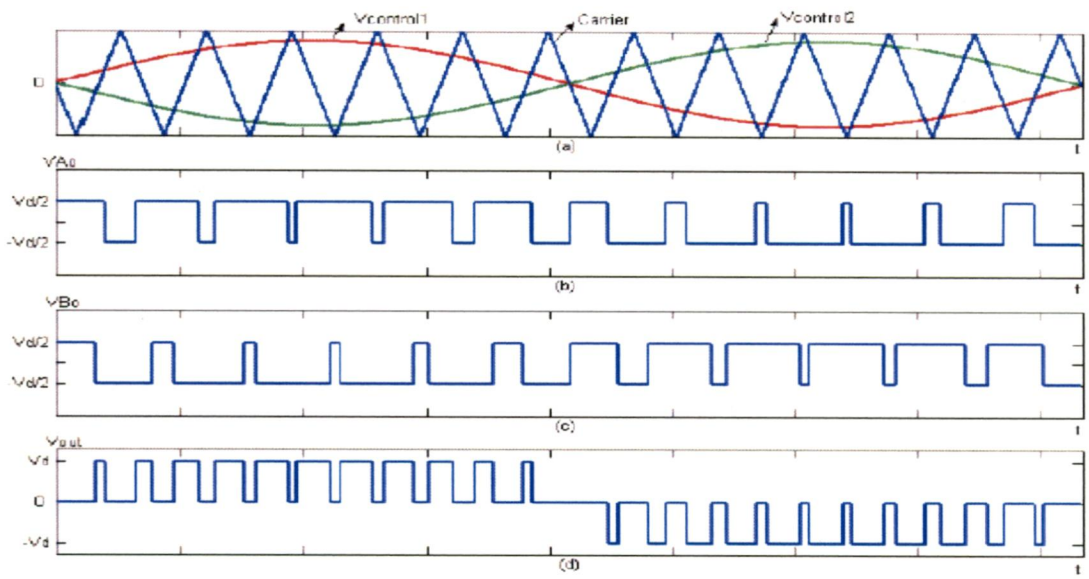

Fig.2.7. a. shows the comparison of carrier with sine wave b. shows pulses generated for positive device c. pulses for negative device d. obtained output wave for one-cycle

CHAPTER-3

THREE LEVEL INVERTERS

3.1 General Discussion

As we know that the output obtained from a two-level inverter is not a pure sinusoidal waveform. It is due to the presence of harmonics in the inverter output voltage which may cause heavy losses and may lead to low efficiency of the induction motors or any other applications which may take the supply from the inverter. So, there is a need for us to reduce these harmonics [8]-[13].

The harmonics in a two level inverter is reduced by increasing the switching frequency. But the switching frequency is restricted by the switching losses in high power applications. In such applications multilevel inverters have been widely used in recent years for the advantage of low harmonic output at low switching frequency. At the same time low blocking in the switching devices can be achieved. The more the number of levels of the output voltage the lesser will be the harmonic content. Multi level inverters have advantages of good power quality, good electromagnetic compatibility, low switching losses, high voltage capability. Because of these reasons the multi level inverters are used in the active rectifiers and the FACTS applications [2].

The multi level inverters synthesize several voltage levels from the various levels of the DC input. A near sinusoidal voltage waveform can be generated from the various levels of the DC input. They have become attractive in the high power and high voltage applications. By using the multilevel inverters the stress on each device is reduced proportional to the number of the output levels present [2]. With several levels in the output waveform the switching dv/dt stresses are reduced, and hence the lifetime of motor and cables are increased. By using a multilevel inverter the power rating of the equipment can be enhanced without any dangerous consequences [18].

3.2 Three-Level Inverter

The three-level implementation is based on the digital implementation of the diode-clamped three-phase three-level SPWM control based inverter. It is well known that multilevel inverter have been receiving more and more attention for high-voltage and high power applications. Numbers of topologies and modulation strategies have been investigated for utility and drive applications recent years.

Multi-level inverters are suitable in high-voltage and high power applications due to their ability to synthesize waveforms with better harmonic spectrum and attain higher voltages with a limited maximum device rating. Based on the analysis of the diode-clamped three-level inverter topology, this chapter presents SPWM modulation strategy to reduce switching loss.

3.2.1 Operation of Three-Phase 3-Level Inverter

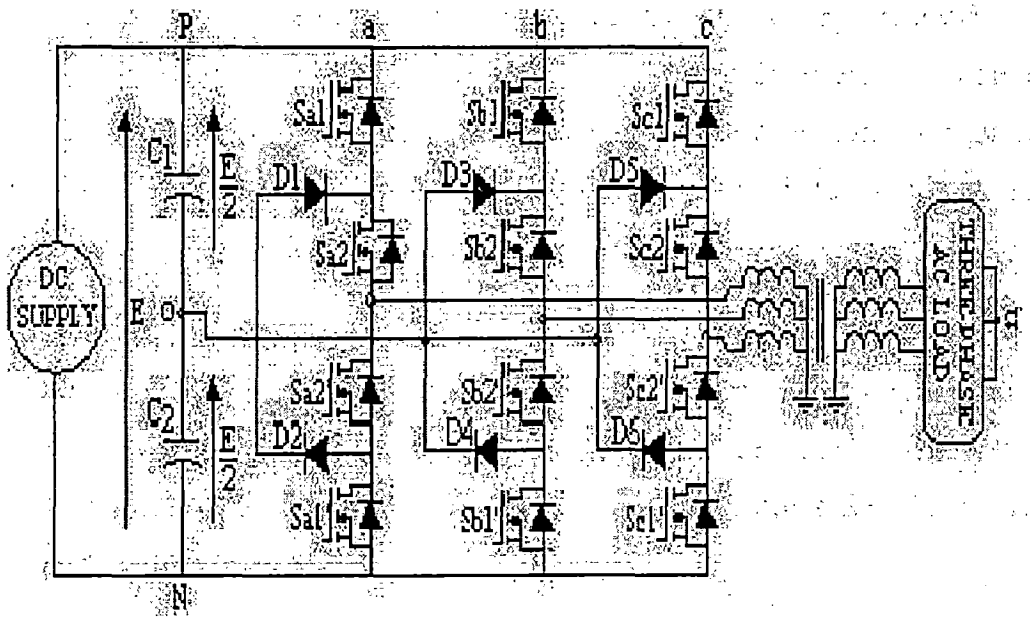

Fig.3.1. Power Circuit for Three-Phase Three-Level Inverter

The Fig.3.1 shown above gives the basic circuit for the 3-phase three-level diode clamped inverter. The circuit employs 12 power switching devices (S_{a1}-S_{a4}) and 6 clamped diodes (D_1-D_6). And the dc-bus voltage is split into three-level by two series-connected bulk capacitors can be defined as the neutral point 0. as the result of the

diode-clamped the dc-bus voltage $V_{dc}/2$. Thus, the voltage stress of the switching device is greatly reduced. The output voltage V_{a0} has three different states: $+V_{dc}/2$, 0, $-V_{dc}/2$.

Here take phase-A as an example for voltage. For voltage $-V_{dc}/2$, S_{a3} and S_{a4} need to be turned on. We can define these states as 2, 1, and 0, respectively. Then, the switching variable S_a is shown in table 3.1. be similar to three-phase two-level inverter, the switching states of each bridge leg of three-phase three-level inverter is described by using switching variables S_a, S_b and S_c. Whereas the difference is that, in three-level inverter, each bridge leg has three different switching states [4]- [11].

Table 3.1 Switching Variable of Phase A

V_{ao}	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_a
$+V_{dc}/2$	ON	ON	OFF	OFF	2
0	OFF	ON	ON	OFF	1
$-V_{dc}/2$	OFF	OFF	ON	ON	0

Using switching variable S_a and dc-bus voltage Vdc, the output phase voltage V_{ao} is obtained as follows:

$$V_{an} = (S_a-1)*V_{dc}/2$$

And the output line voltage of phase A and B can be expressed as follows:

$$V_{ab} = V_{ao}- V_{bo} = 1/2*V_{dc} (S_a-S_b)$$

3.3 Sinusoidal PWM for A Three-Level Inverter

If the fundamental output voltage and corresponding power level of the PWM inverter are to be increased to a high value, the dc link voltage V_{dc} must be increased and the devices must be connected in series. By using matched devices in series, static voltage sharing may be somewhat easy, but dynamic voltage sharing during switching is always difficult. The problem may be solved by using a multi-level inverter or neutral point clamped (NPC), inverter. In this thesis work we mainly confined to the three-level inverter.

As shown in Fig.3.1 three-level, three-phase inverter using MOSFET devices. In the Fig.3.1, the dc link capacitor C has been split to create the neutral point '0'. Since the operation of all the phase groups is essentially identical, consider only the operation of the half-bridge for phase A. A pair of devices with bypass diodes is connected in series with an additional diode connected between the neutral point and the center of the pair as shown. The devices S_{a1} and S_{a2} function as main devices(like a two-level inverter), the S_{a2} and S_{a3} function as auxiliary devices which help to clamp the output potential to the neutral point with the help of clamping diodes D_1 and D_2.

All the PWM techniques can be applied to this inverter. The main devices (S_{a1} and S_{a4}) generate the V_{a0} wave, whereas the auxiliary devices (S_{a3} and S_{a2}) are driven complementary to the respective main devices. With such control, each output potential is clamped to the neutral potential in the off periods of the PWM control. Evidently, the positive phase current $+i_a$ will be carried by devices D_1 and S_{a2} at the neutral clamping condition. On the other hand, negative phase current $-i_a$ will be carried by D_1 and D_2 when V_{a0} is positive, by S_{a3} and Sa4 when V_{a0} is negative, and by S_{a3} and diode at the neutral clamping condition. This operation mode gives three voltage levels ($+0.5V_{dc}$, 0, and $-0.5V_{dc}$) at the V_{a0} wave as shown in the Fig.3.2 of phase voltage below. Likewise the wave forms for all the other phases are generated and the resultant Phase-to-Phase voltages are obtained.

Sinusoidal PWM:

The implementation of a three-level inverter by sine-PWM is carried out using two carrier waves. They are compared with the single sinusoidal wave and corresponding pulses are generated which are to be supplied to the inverter gate devices. And for the other phases the sinusoidal wave is displaced by an angle 2Π/3 and 4Π/3. Let us see an example for a single leg of a three-level inverter bridge.

The sinusoidal with frequency f_o is taken and two carrier waves, i.e., a carrier wave which is starting at 0 time period and the other carrier wave is a negative going one and is the negative going carrier wave with frequency f_s i.e., switching frequency. The magnitude of the carrier wave is always greater than the reference wave. The positive going carrier wave generates the pulses for the devices by which the inverter phase generate a positive voltage. The negative going carrier wave generates the pulses for the inverter which in turn give the negative phase voltage in a particular leg. The above procedure can be shown for a single phase of one leg in the Fig.3.2. From the above procedure we can obtain the pulses for the two devices of a single leg but totally we want four set of pulses for a single leg in order to generate the required output wave form. The other two set of pulses are generated by taking the negation of the above obtained two set of pulses as shown in Fig.3.3 [1]-[15].

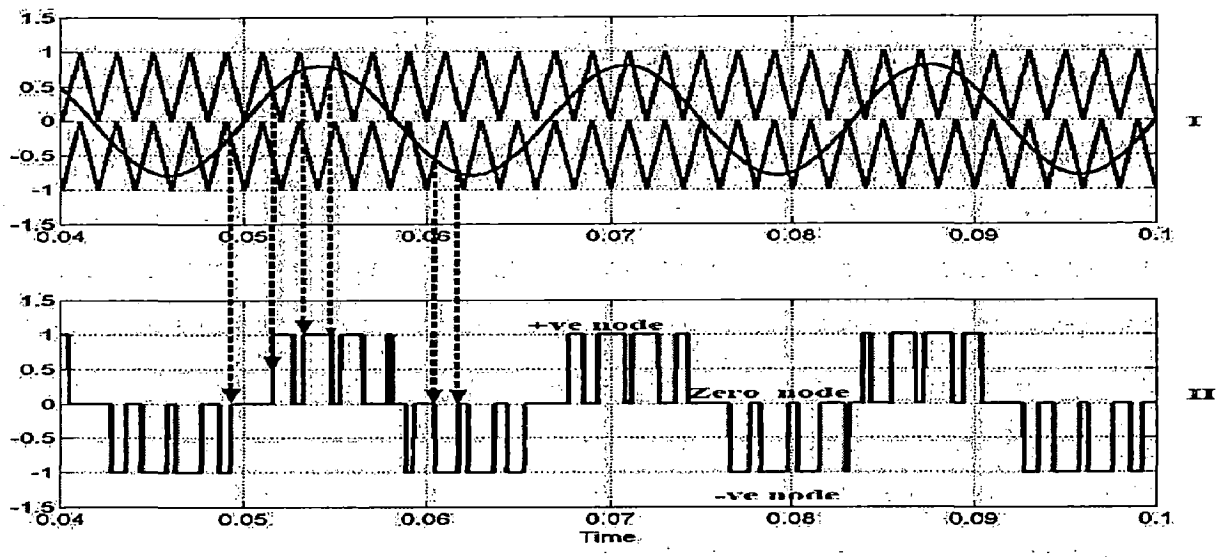

Fig 3.2 Sine-PWM switching patterns for single-phase of three-level inverter

Following conditions are fulfilled in order to generate the pulses for the inverter legs:

Sinusoidal > carrier 1 then the pulse will be1 else 0

Sinusoidal < carrier 2 then the pulse will be 1 else 0

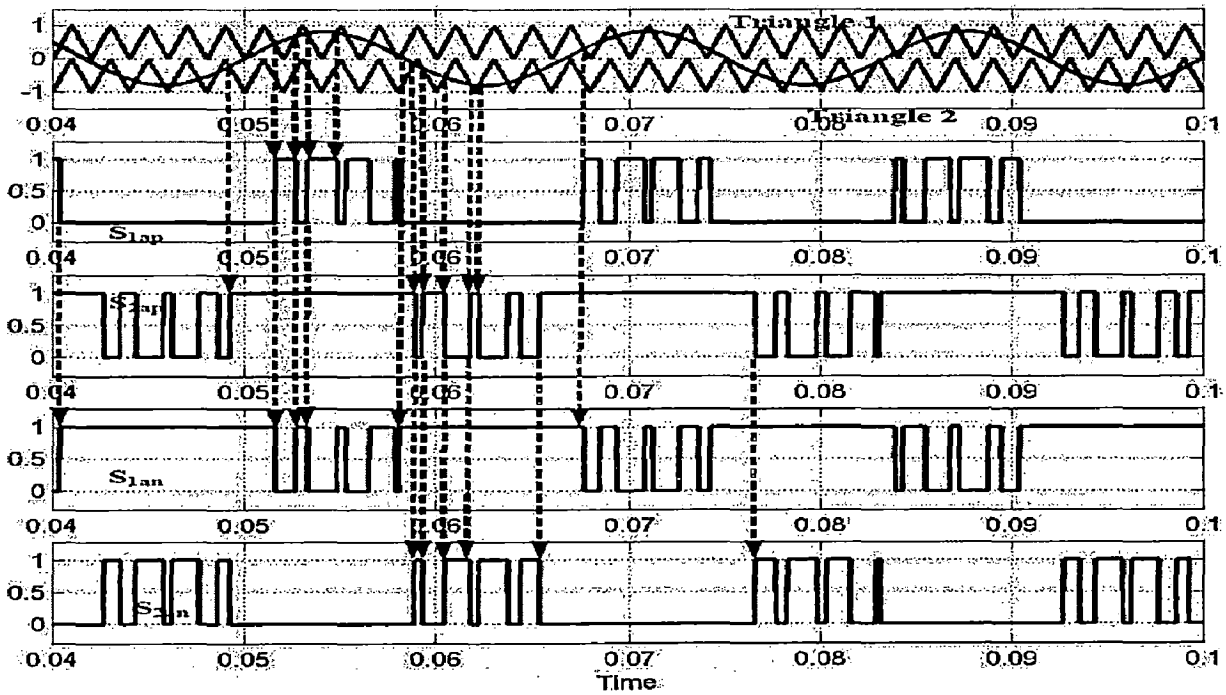

Fig.3.3. Sine-PWM switching pattern for three-level inverter

Similarly the same logic is employed to the other two legs but with a phase displacements of 2Π/3 and 4Π/3 for sinusoidal reference wave for other two legs for the two-phase B and C respectively.

3.4 Simulation and Analysis

3.4.1 Simulink block for Three Level Inverter with sinusoidal PWM

The model given in Fig.3.4 gives the three-level inverter with the sinusoidal PWM as the control technique. The input DC voltage is split into two halves and given to a three-level bridge which is built by three-arms and 12 power devices in total. Each leg has four power devices and diodes are connected in parallel with these power devices. IGBTs are taken as the power devices. The block properties of the three-level bridge can be modified by double clicking on the block. The ABC is taken as the output

terminals. The output is measured across a three-phase load whose specifications are given below. The load current and the load voltage are taken as the output in a scope.

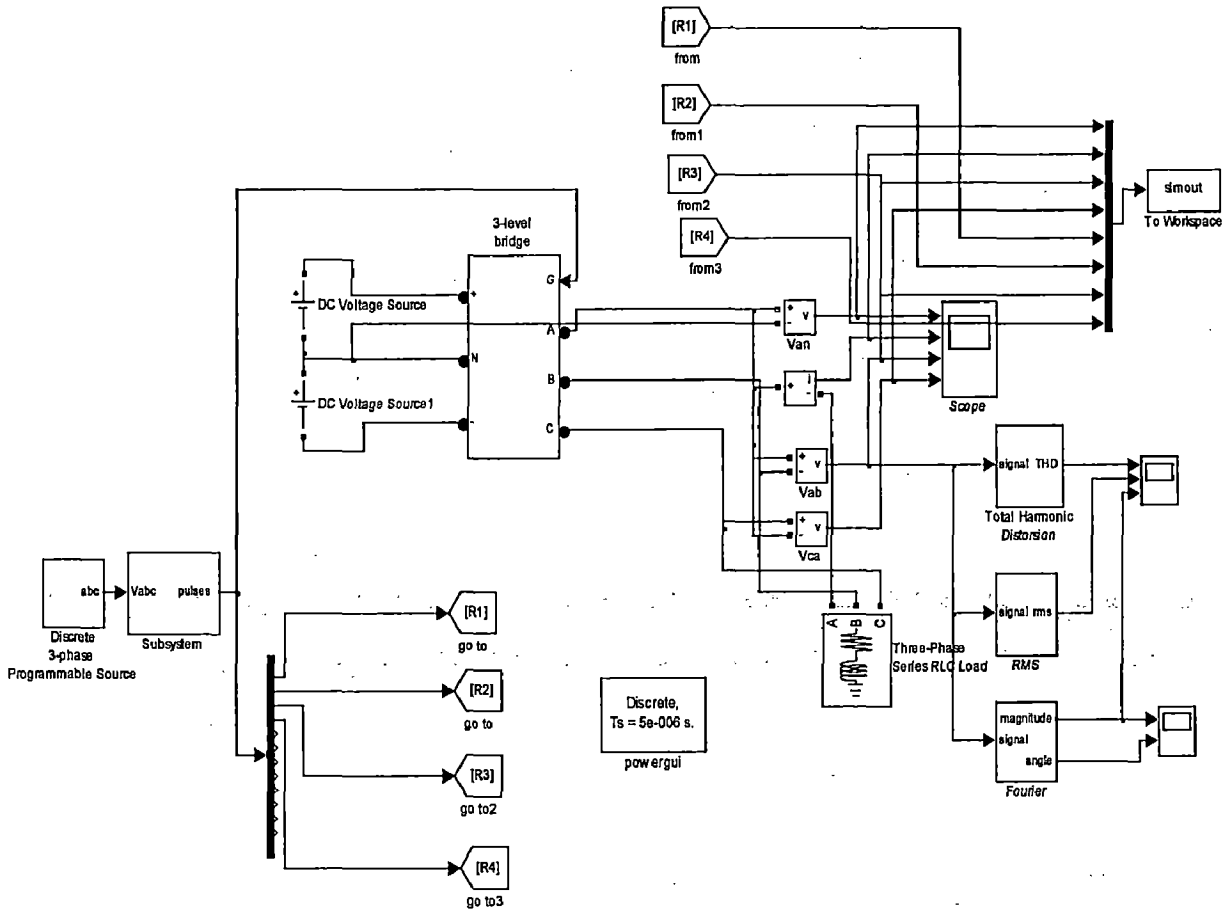

Fig.3.4. Simulink Model for Three-Phase Three-Level Inverter

MODEL PARAMETERS:

Input DC voltage : 200V

Load : resistance= 1ohm; Inductance= 0.001H

Output frequency : 50Hz

Output peak voltage : 400V

3.4.2 Sinusoidal PWM Control Block

The Fig.3.5 shown below gives the control block of the sine-PWM for the three-level inverter. A positive going carrier-1 and a negative going carrier-2 are generated and are compared with the sinusoidal wave form and the pulses are obtained. The sinusoidal and the carrier waves are generated by the repeating signal block in the SIMULINK browser.

The repeating signal is found in the **SIMULINK/SOURCES/REPEATING SEQUENCE**. The sine wave form can be obtained from the **SIMULINK/SOURCES/SINE-WAVE** block. The properties of the blocks can be changed by double clicking on the block.

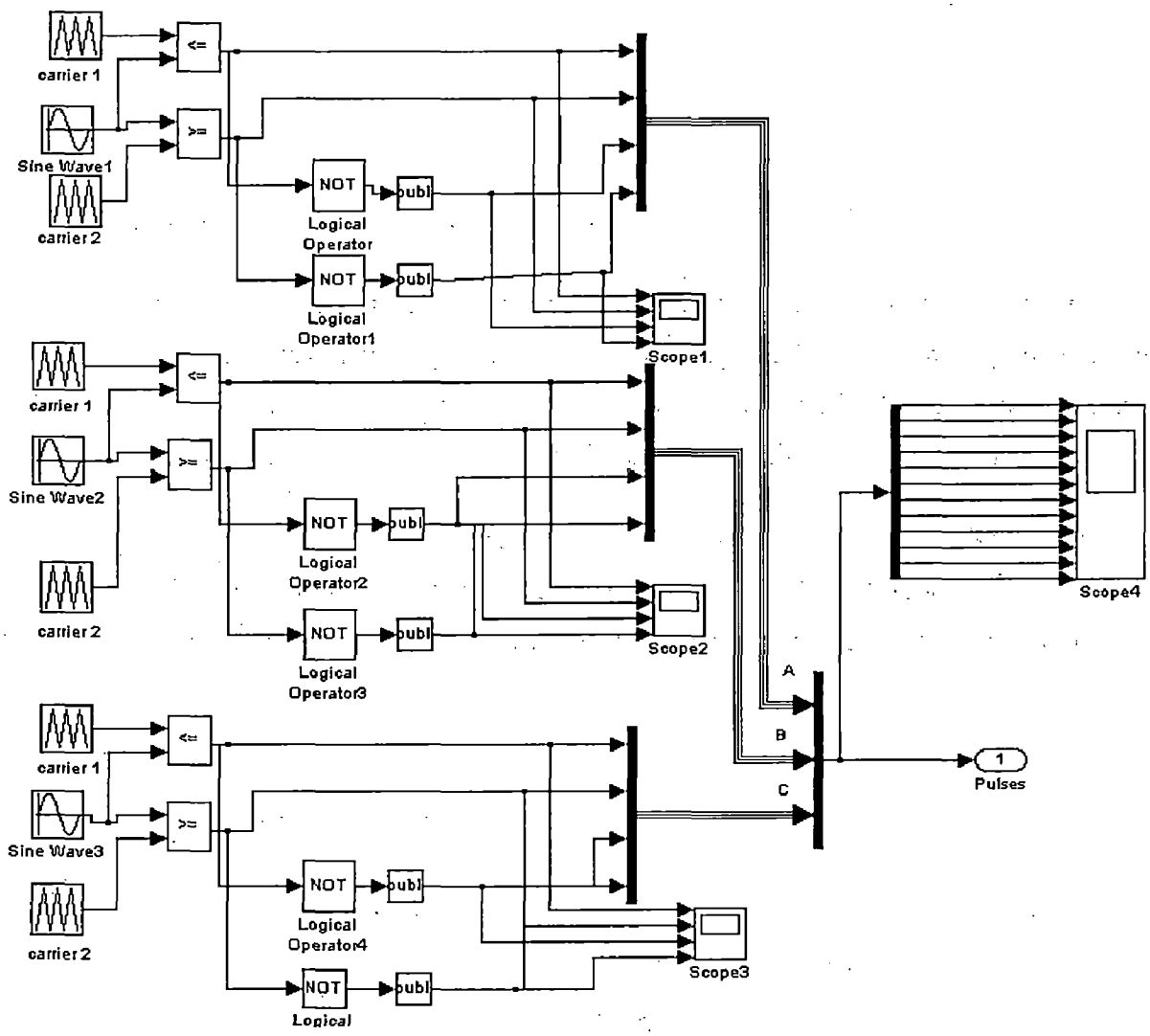

Fig.3.5. Sinusoidal PWM Control Block

Table 3.2 PARAMETERS:

Carrier 1: Frequency : 1000Hz initial value→ 0 Magnitude : 1V		**Carrier 2:** Frequency : 1000Hz initial value→ -1 Magnitude : 1V
Sine 1 : Frequency = 50Hz, Magnitude = 0.9V Phase = 0	**Sine 2 :** Frequency = 50Hz, Magnitude = 0.9V Phase = $2\pi/3$	**Sine 3 :** Frequency = 50Hz, Magnitude = 0.9V Phase = $4\pi/3$

3.4.3 3-Level Bridge Using Diode Clamped Topology

Fig.3.6 shows the Simulink model for three phase inverter using diode clamped configuration for generating the multilevel output.

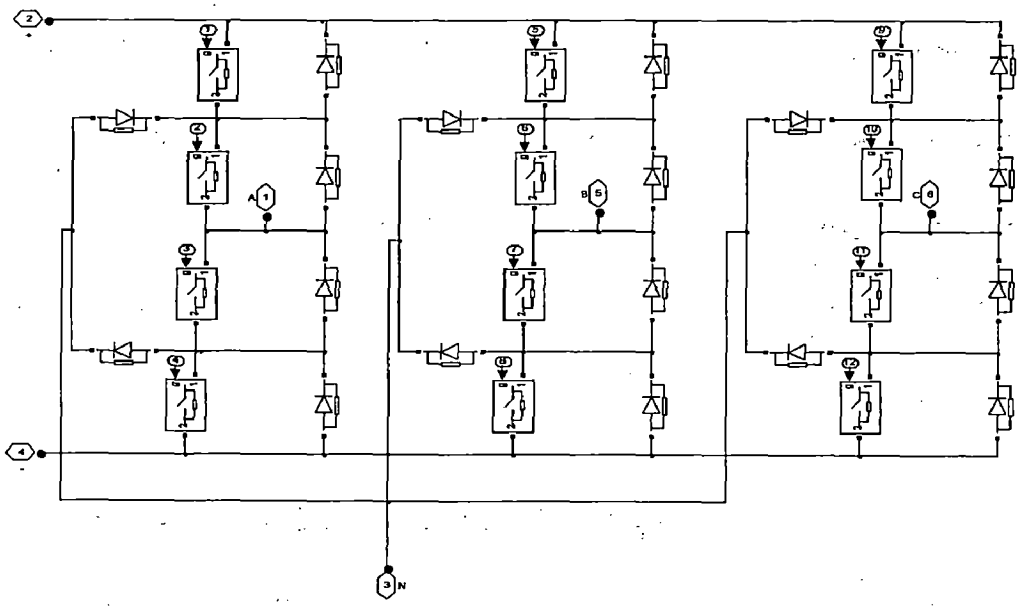

Fig.3.6. Subsystem for the 3-Level Bridge

CHAPTER -4

FAULT DETECTION IN MULTI LEVEL INVERTER USING FUZZY INFERENCE SYSTEM AND ANFIS

Introduction to Fuzzy and ANFIS:

The term expert system (ES), Fuzzy logic (FL), artificial neural network (ANN), and genetic algorithm (GA) belong to an area called ARTIFICIAL INTELLIGENCE (AI). Recently, the area of AI has penetrated deeply into electrical engineering, and their applications in power electronics and motion control appears very promising. The goal of AI is to plant human or natural intelligence in a computer so that a computer can think intelligently like a human being.

A system with embedded computational intelligence is often defined as an "intelligent system" that has "learning," "self-organizing," or "self-adapting" capability. However, there is no denying the fact that computers can have adequate intelligence to help solving our problems that are difficult to solve by traditional methods. Therefore, it is true that AI techniques are now being extensively used in industrial process control, image processing, diagnostics, medicine, space technology, and information management system, just to name a few.

System modeling based on conventional mathematical tools like differential equations is not perfectly suited for dealing with uncertain systems. By contrast a Fuzzy inference system employing Fuzzy IF-THEN rules can model the qualitative aspects of human knowledge and reasoning process without employing precise quantitative analyses. This Fuzzy modelling or Fuzzy identification, first explored systematically by Takagi and Sugeno, has found numerous practical applications in control, prediction and inference. However, there are some basic aspects of this approach which are in need of better understanding.

More specifically:

1) No standard methods exist for transforming human knowledge or experience into the rule base and database of a Fuzzy inference system.
2) There is a need for effective methods for tuning the membership functions (MF's) so as to minimize the output error measure or maximize performance index.

An Adaptive-Neuro Fuzzy Inference System, or simply ANFIS, which can serve as a basis for constructing a set of Fuzzy if-then rules with appropriate membership functions to generate the stipulated input-output pairs.

The basic structure of the type of Fuzzy inference system is a model that maps input characteristics to input membership functions, input membership function to rules, rules to a set of output characteristics, output characteristics to output membership functions, and the output membership function to a single-valued output or a decision associated with the output. We have only considered membership functions that have been fixed, and somewhat arbitrarily chosen. Also, we've only applied Fuzzy inference to modeling systems whose rule structure is essentially predetermined by the user's interpretation of the characteristics of the variables in the model.

4.1 Fuzzy Inference Systems and ANFIS

A. Fuzzy If-Then Rules

Fuzzy if-then rules are expressions of the form IF A THEN B, where A and B are labels of Fuzzy sets characterized by appropriate membership functions. Due to their concise form, Fuzzy if-then rules are often employed to capture the imprecise modes of reasoning that play an essential role in the human ability to make decisions in an environment of uncertainty and imprecision [10]-[26].

An example that describes a simple fact is

"If pressure is high, then volume is small"

Where pressure and volume are linguistic variables, high and small are linguistic values or labels that are characterized by membership functions.

Another form of Fuzzy if-then rule, proposed by Takagi and Sugeno, has Fuzzy sets involved only in the premise part. By using Takagi and Sugeno's Fuzzy if-then rule, we can describe the resistant force on a moving object as follows:

"If velocity is high, then force = k*(velocity)^2"

Where, again, high in the premise part is a linguistic label characterized by an appropriate membership function. However, the consequent part is described by a non-Fuzzy equation of the input variable, velocity. Both types of Fuzzy if-then rules have been used extensively in both modelling and control. Through the use of linguistic labels and membership functions, a Fuzzy if-then rule can easily capture the spirit of a "rule of thumb" used by humans. From another angle, due to the qualifiers on the premise parts, each Fuzzy if-then rule can be viewed as a local description of the system under consideration [25]. Fuzzy if-then rules form a core part of the Fuzzy inference system to be introduced below.

A Modeling Scenario

Suppose we want to apply Fuzzy inference to a system for which we already have a collection of input/output data that we would like to use for modeling, model-following, or some similar scenario. We don't necessarily have a predetermined model structure based on characteristics of variables in our system.

There will be some modeling situations in which we can't just look at the data and discern what the membership functions should look like. Rather than choosing the parameters associated with a given membership function arbitrarily, these parameters could be chosen so as to tailor the membership functions to the input/output data in order to account for these types of variations in the data values. This is where the so-called Neuro-Adaptive learning techniques incorporated into ANFIS in the Fuzzy Logic can help [10].

The basic idea behind these Neuro-Adaptive learning techniques is very simple. These techniques provide a method for the Fuzzy modeling procedure to learn information about a data set, in order to compute the membership function parameters that best allow the associated Fuzzy inference system to track the given input/output data. This learning method works similarly to that of neural networks [5]-[9].

What Is ANFIS?

The acronym ANFIS derives its name from Adaptive Neuro-Fuzzy Inference System. Using a given input/output data set, ANFIS constructs a Fuzzy inference system (FIS) whose membership function parameters are tuned (adjusted) using either a Back propagation algorithm alone, or in combination with a least squares type of method. This allows our Fuzzy systems to learn from the data they are modeling [27].

Simply we can say that it's a network-type structure similar to that of a neural network, which maps inputs through input membership functions and associated parameters, and then through output membership functions and associated parameters to outputs, can be used to interpret the input/output map. The parameters associated with the membership functions will change through the learning process. The computation of these parameters (or their adjustment) is facilitated by a gradient vector, which provides a measure of how well the Fuzzy inference system is modeling the input/output data for a given set of parameters. Once the gradient vector is obtained, any of several optimization routines could be applied in order to adjust the parameters so as to reduce some error measure (usually defined by the sum of the squared difference between actual and desired outputs). ANFIS uses either back propagation or a combination of least squares estimation and back propagation for membership function parameter estimation [5]-[9].

Familiarity Breeds Validation: Know Your Data

The modeling approach used by ANFIS is similar to many system identification techniques. First, we hypothesize a parameterized model structure (relating inputs to membership functions to rules to outputs to membership functions, and so on). Next,

you collect input/output data in a form that will be usable by ANFIS for training. You can then use ANFIS to train the FIS model to emulate the training data presented to it by modifying the membership function parameters according to a chosen error criterion.

In general, this type of modeling works well if the training data presented to ANFIS for training (estimating) membership function parameters is fully representative of the features of the data that the trained FIS is intended to model. This is not always the case, however. In some cases, data is collected using noisy measurements, and the training data cannot be representative of all the features of the data that will be presented to the model. This is where model validation comes into play [9].

Model Validation Using Checking and Testing Data Sets

One problem with model validation for models constructed using adaptive techniques is selecting a data set that is both representative of the data the trained model is intended to emulate, yet sufficiently distinct from the training data set so as not to render the validation process trivial. If we have collected a large amount of data, hopefully this data contains all the necessary representative features, so the process of selecting a data set for checking or testing purposes is made easier. However, if we expect to be presenting noisy measurements to our model, it is possible the training data set does not include all of the representative features we want to model.

Constraints of ANFIS:

ANFIS is much more complex than the Fuzzy inference systems, and is not available for all of the Fuzzy inference system options. Specifically, ANFIS only supports Sugeno-type systems, and these must have the following properties:

- Be first or Zeroth order Sugeno-type systems.
- Have a single output, obtained using weighted average Defuzzification. All output membership functions must be the same type and either linear or constant.

- Have no rule sharing. Different rules cannot share the same output membership function, namely the number of output membership functions must be equal to the number of rules.
- Have unity weight for each rule.
- An error occurs if our FIS structure does not comply with these constraints.
- Moreover, ANFIS cannot accept all the customization options that basic Fuzzy inference allows. That is, we cannot make our own membership functions and Defuzzification functions; we must use the ones provided.

Architecture of ANFIS:

The ANFIS is a Fuzzy Sugeno model put in the framework of adaptive systems to facilitate learning and adaptation. Such framework makes the ANFIS modelling more systematic and less reliant on expert knowledge. To present the ANFIS architecture, two fuzzy if-then rules based on a first order Sugeno model are considered:

Rule 1: If (x is A_1) and (y is B_1) then ($f_1 = p_1x + q_1y + r_1$)

Rule 2: If (x is A_2) and (y is B_2) then ($f_2 = p_2x + q_2y + r_2$)

Where x and y are the inputs, A_i and B_i are the fuzzy sets, f_i are the outputs within the Fuzzy region specified by the Fuzzy rule, p_i, q_i and r_i are the design parameters that are determined during the training process. The ANFIS architecture to implement these two rules is shown in Fig.4.1, in which a circle indicates a fixed node, whereas a square indicates an adaptive node.

In the first layer, all the nodes are adaptive nodes. The outputs of layer 1 are the fuzzy membership grade of the inputs, which are given by:

$$O_i^l = \mu A_i(x) \quad i = 1, 2; \tag{4.1.1}$$

$$O_i^l = \mu B_{i-2}(y) \quad i=3,4; \tag{4.1.2}$$

Where $\mu A_i(x)$, $\mu B_{i-2}(y)$ can adopt any Fuzzy membership function. For example, if the bell shaped membership function is employed and is given by

$$\mu A_i(x) = \frac{1}{1+\left\{\left(\frac{x-c_i}{a_i}\right)^2\right\}^{b_i}} \tag{4.1.3}$$

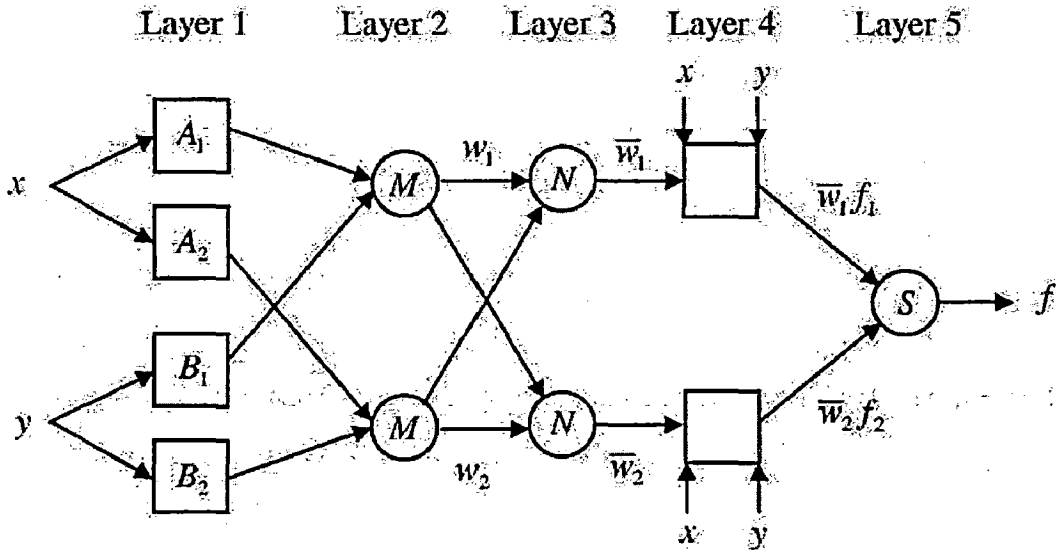

Fig 4.1 ANFIS architecture.

Where a_i, b_i and c_i are the parameters of the membership function, governing the bell shaped functions accordingly. In the second layer, the nodes are fixed nodes. They are labelled with *M*, indicating that they perform as a simple multiplier. The outputs of this layer can be represented as:

$$O_i^2 = w_i = \mu A_i(x)\mu B_i(y) \quad \text{i=1,2} \tag{4.1.4}$$

Which are the so-called firing strengths of the rules. In the third layer, the nodes are also fixed nodes. They are labelled with *N*, indicating that they play a normalization role to the firing strengths from the previous layer. The outputs of this layer can be represented as

$$O_i^3 = \overline{w_i} = \frac{w_i}{w_1 + w_2} \quad \text{i=1,2} \tag{4.1.5}$$

which are the so-called normalized firing strengths. In the fourth layer, the nodes are adaptive nodes. The output of each node in this layer is simply the product of the normalized firing strength and a first order polynomial (for a first order Sugeno model). Thus, the outputs of this layer are given by:

$$O_i^4 = \overline{w_i} f_i = \overline{w_i}\left(p_i x + q_i y + r_i\right) \quad \text{i=1,2} \tag{4.1.6}$$

In the fifth layer, there is only one single fixed node labelled with *S*. This node performs the summation of all incoming signals. Hence, the overall output of the model is given by:

$$O_i^5 = \sum_{i=1}^{2} \overline{w_i} f_i = \frac{\sum_{i=1}^{2} w_i f_i}{w_1 + w_2} \tag{4.1.7}$$

It can be observed that there are two adaptive layers in this ANFIS architecture, namely the first layer and the fourth layer. In the first layer, there are three modifiable parameters $\{a_i, b_i, c_i\}$, which are related to the input membership functions. These parameters are the so-called premise parameters. In the fourth layer, there are also three modifiable parameters $\{p_i, q_i, r_i\}$, pertaining to the first order polynomial. These parameters are so-called consequent parameters [27].

Learning algorithm of ANFIS:

The task of the learning algorithm for this architecture is to tune all the modifiable parameters, namely $\{a_i, b_i, c_i\}$ and $\{p_i, q_i, r_i\}$, to make the ANFIS output match the training data. When the premise parameters a_i, b_i and c_i of the membership function are fixed, the output of the ANFIS model can be written as:

$$f = \frac{w_1}{w_1 + w_2} f_1 + \frac{w_2}{w_1 + w_2} f_2 \tag{4.1.8}$$

Substituting Eq. (4.1.5) into Eq. (4.1.8) yields:

$$f = \overline{w_1} f_1 + \overline{w_2} f_2 \tag{4.1.9}$$

Substituting the fuzzy if-then rules into Eq. (4.1.9), it becomes:

$$f = \overline{w_1}(p_1 x + q_1 y + r_1) + \overline{w_2}(p_2 + q_2 y + r_2) \tag{4.1.10}$$

After rearrangement, the output can be expressed as:

$$f = (\overline{w_1} x) p_1 + (\overline{w_1} y) q_1 + (\overline{w_1}) r_1 + (\overline{w_2} x) p_2 + (\overline{w_2} y) q_2 + (\overline{w_2}) r_2 \tag{4.1.11}$$

This is a linear combination of the modifiable consequent parameters p_1, q_1, r_1, p_2, q_2 and r_2. The least squares method can be used to identify the optimal values of these parameters easily. When the premise parameters are not fixed, the search space becomes larger and the convergence of the training becomes slower. A hybrid algorithm combining the least squares method and the gradient descent method is adopted to solve this problem. The hybrid algorithm is composed of a forward pass and a backward pass. The least squares method (forward pass) is used to optimize the consequent parameters with the premise parameters fixed. Once the optimal consequent parameters are found, the backward pass starts immediately. The gradient descent method (backward pass) is used to adjust optimally the premise parameters corresponding to the Fuzzy sets in the input domain. The output of the ANFIS is calculated by employing the consequent parameters found in the forward pass. The output error is used to adapt the premise parameters by means of a standard Back-propagation algorithm. It has been proven that this hybrid algorithm is highly efficient in training the ANFIS.

There are number of intelligent systems approaches that have been investigated in signal fault diagnosis. Decision trees and Rule-based expert systems are two normally used diagnostic techniques, but they have serious limitations. A rule-based system often has difficulties in dealing with novel faults and acquiring a complete knowledge to build a reliable rule base. A decision tree can be very large for a complex system, and it is also system dependent such that even small engineering changes can mean significant updates. More recently model based approaches, Fuzzy logic, Artificial Neural Networks (ANN), case-based reasoning (CBR) are popular techniques used in various fault diagnostics problems in electrical systems [23].

The diagnostic system has the capability of accurately detecting whether a fault has occurred, and show the faulty location in the electric drive within 20 ms or less. The contribution of this work is important because in many applications it is extremely important to detect a fault immediately after it occurs and pin-point to the cause of fault. As soon as a fault is detected and located, for example switch S_1 short or S_5 open and so on, it should be isolated and the damaged part should be shut down immediately to minimise the damage to other parts of the system. Identifying the location and type of the fault fast enough can also allow smooth transition to a gracefully degradable mode, which enhances the overall system availability [30]-[14].

It is to point out that generating short circuit faults is in an inverter can cause significant damage (if not total destruction) to the closed-loop controlled electrical system. To prevent such a situation, an electrical system in a lab setting needs various protective mechanisms built in it to shut down the system before any signals in a faulty condition can be sampled. Regarding the possibility of setting up hardware-based experiment where catastrophic failure will not occur during a short circuit fault, it should be noted that this catastrophic failure pertains initially to the solid state power electronic switches, which will try to short circuit the source. Hence, to save the system (both the source and the power electronics switch) we must have to trip it off. If not the source it self, in addition to the switch, may suffer damage. The issue, therefore, is more related to be able to diagnose the fault before it is tripped off. Otherwise the power electronics circuit can soon become unbalanced. At that point, if the motor still has mechanical load connected to it, the situation can lead to both electrical and mechanical damage to the motor because of unbalanced operation.

All the above items point to the difficulty of designing a physical experiment under the above circumstances. Therefore the simulated systems are important means to study fault diagnostic problems in closed-loop situation. Due to these difficulties, the results generated in this thesis work are primarily from the data produced by a simulation model. The simulation model has been validated on the single open switch faults and short-circuits faults in inverter [4].

4.2 General Structure of the fault diagnostic system:

The fault diagnostic system is composed of four major states: feature extraction, Artificial Intelligent systems, fault diagnosis, and switching pattern calculation with gate signal output. The Feature extraction, Intelligent system, and Fault diagnosis are the focus of this research. The Feature extraction performs the voltage input signal transformation, with rated signal values as important features, and the output of the transformed signal is transferred to the Intelligent system. The Intelligent system is designed to give output as 1 for abnormal conditions and 0 for normal conditions. By decoding this binary code the fault location can be detected. After decoding the switching pattern is calculated.

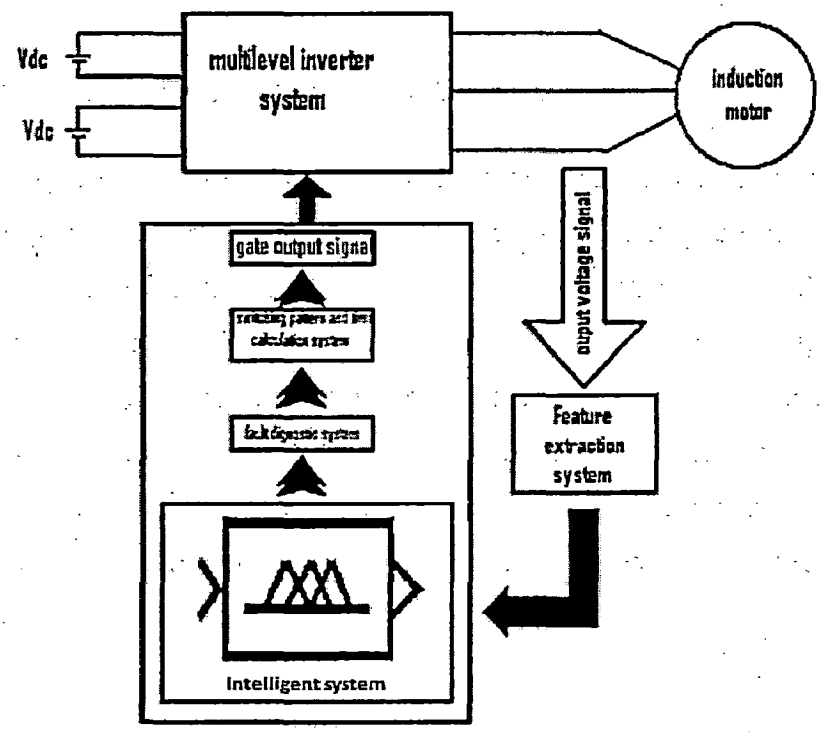

Fig 4.2 Structure of Fault diagnosis system

Since the output of the multilevel inverter is a staircase form, we can't give this output voltages directly to any fault detection system for detection of fault. So we extract the fault features from the output of the multilevel inverter using Feature

Extraction system; these features are given as input for Intelligent system to detect fault location. For Fuzzy inference system we have used the 3rd harmonic magnitude to represent the fault features, for ANFIS we have used the FFT samples to represent the fault features of the system.

4.3 Fault detection using Fuzzy Inference System

The Fuzzy inference system is of Sugeno type. The magnitudes of third harmonic content present in the Phase-to-neutral voltages are taken as input for Fuzzy to detect the type of fault. The number of inputs for Fuzzy inference system is 3, they are 3rd harmonic magnitudes of Phase-to-neutral voltages and the number of outputs of Fuzzy is 12. These 12 outputs are suitably modified to generate the triggering pulses for the extra added leg(s) which is used for reconfiguration and to isolate the faulted inverter leg(s). The variation in magnitudes 3rd harmonic present in each phase-to-neutral output voltage is shown in the last row of the Table 4.1. The range of 3rd harmonic content present in the phase-to-neutral voltages is shown at the end of the Table 4.1. And the structure of the Fuzzy Inference system is shown in Fig.4.3.

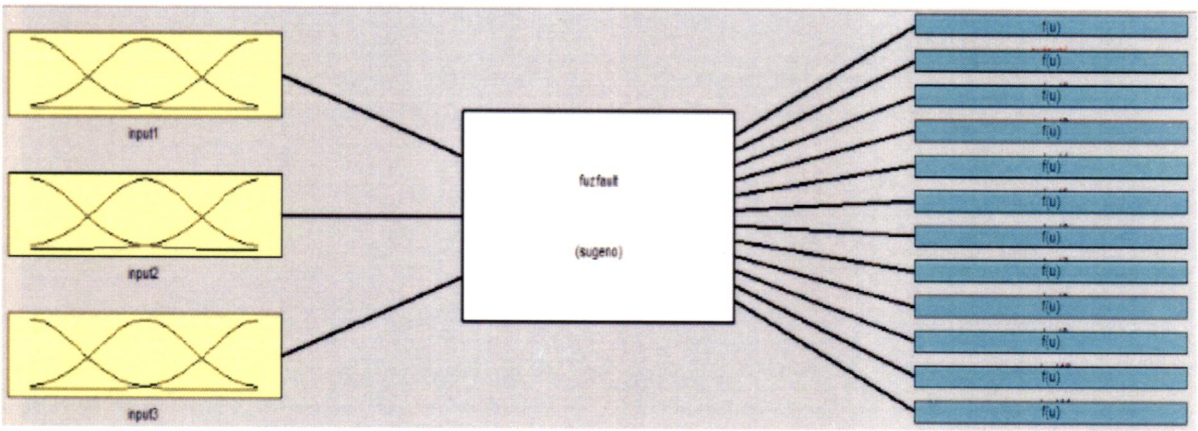

Fig.4.3. Structure of the fuzzy inference system

The member ship functions are of type triangular. In the first step we create membership functions based on the variation of the magnitude of 3rd harmonic. The range of values is given in the table below.

Table 4.1: Variation 3rd Harmonic in the phase-to-Neutral Voltages

Type of fault	Magnitude ranges of 3rd harmonic in V_{an}	Magnitude ranges of 3rd harmonic in V_{bn}	Magnitude ranges of 3rd harmonic in V_{cn}
Open S_1	2.53-2.57	.28-.34	.194-.206
Short S_1	.276-.277	.29-.34	.237-.242
Open S_2	4.1-4.25	.22-.28	.161-.1615
Short S_2	.21-.26	.315-.3	.204-.207
Open S_3	4.1-4.7	.205-.26	.1325-.1335
Short S_3	.27-.31	.29-.36	.215-.22
Open S_4	.27-.285	.29-.35	.184-.188
Short S_4	.097-.098	.31-.365	.22-.24
Open S_5	.17-.24	3.1-3.33	.24-.26
Short S_5	.24-.3	.015-.022	.233-.238
Open S6	.11-.18	4.3-4.7	.224-.245
Short S_6	.25-.32	.31-.37	.235-.245
Open S_7	.2-.27	3.75-3.95	.14-.2
Short S_7	.17-.23	.29-.32	.25-.265
Open S_8	.2-.32	2.3-2.4	.205-.23
Short S_8	.21-.26	.09-.13	.212-.22
Open S_9	.215-.245	.27-.32	2.33-2.35
Short S_9	.24-.31	.3-.36	.015-.038
Open S_{10}	.15-.2	.24-.3	3.75-3.9
Short S_{10}	.25-.31	.3-.345	.224-.226
Open S_{11}	.19-.285	.245-.29	3.8-4.6
Short S_{11}	.22-.27	.3-.36	.275-.28
Open S_{12}	.22-.305	.29-.34	2.4-3.2
Short S_{12}	.21-.255	.31-.36	.12-.16
Range	.097-4.25	.015-4.7	.015-4.6

Here the number of membership functions is 24 corresponding to 24 different types of faults. These are shown in Fig.4.4.

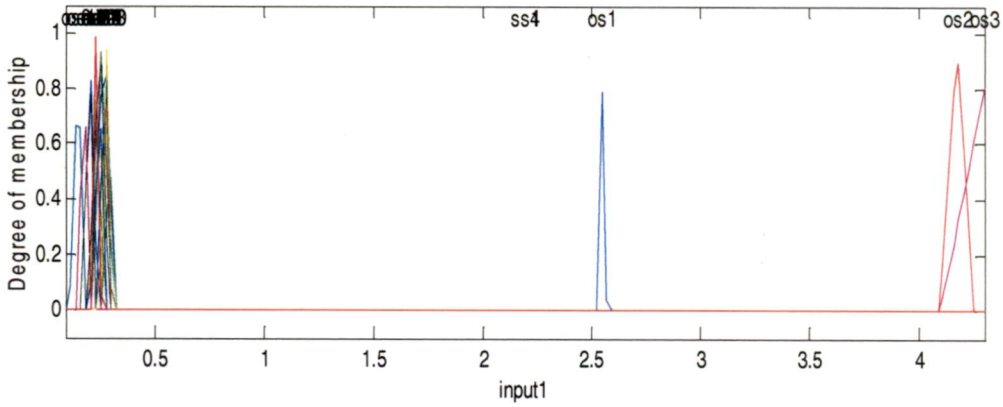

Fig.4.4. Member Ship functions corresponding to V_{an}

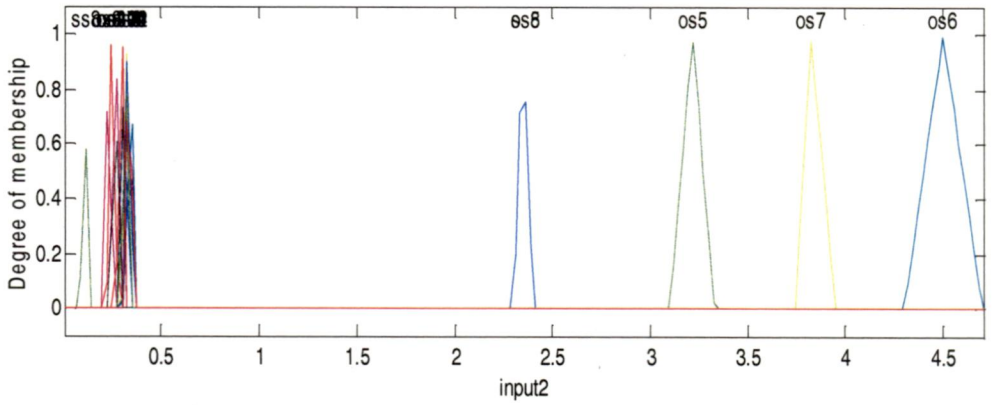

Fig.4.5. Member Ship functions corresponding to V_{bn}

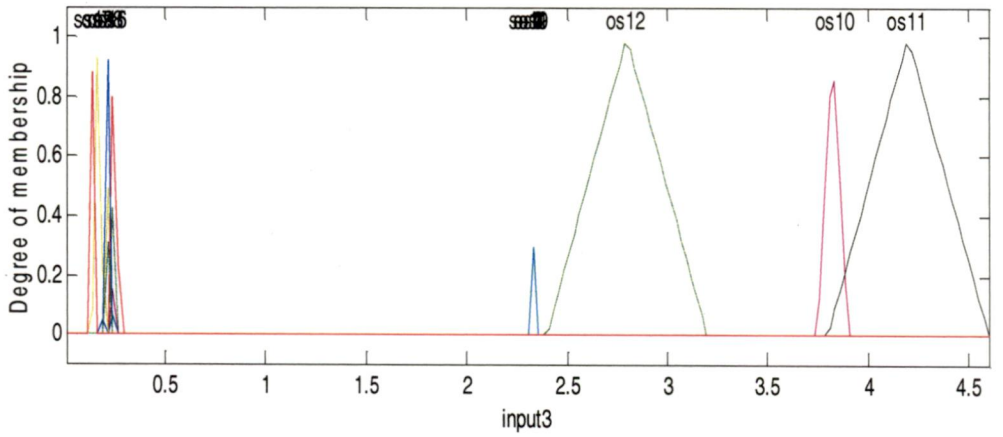

Fig.4.6. Member Ship functions corresponding to V_{cn}

4.4 Fault detection using Adaptive Neuro Fuzzy Inference System

In this type of fault detection system we use FFT samples as the fault features of the inverter. The FFT used here is going to generate 20 FFT samples of the Phase-to-Phase output voltage of the inverter. Among them we have used 5 samples for training purpose. And these 5 samples are given as input to ANFIS. An appropriate selection of feature extractor is to provide the ANFIS with adequate significant details in the pattern set so that the highest degree of accuracy in the ANFIS performance can be obtained.

To improve on the accuracy of the ANFIS a suitable feature extractor be employed for the task of providing the best patterns to the ANFIS for training and consultation. In addition to the time domain feature extractor, other candidates include the Fast Fourier Transform (FFT), the Hartley Transform and the Wavelet Transform. Here we use FFT samples to train the ANFIS.

Fourier developed several mathematical tools and published these findings in 1882 in "Analytical Theory of Heat" which described the propagation of heats in solids. One of these tools, the Fourier Transform is used to easily analyze the frequency components of phenomena in the time domain.

The Hartley transform was originally developed in 1942 to investigate the steady-state and transient analysis transmission problems, and researchers like Bracewell have embraced it for signal processing especially because of its real nature.

Wavelet transforms are based on a set of signals derived from a basic mother wavelet by adjusting the time-shifting and time-dilation parameters. In this way, the wavelet transform isolates and magnifies a specific portion of the input time domain sequence under investigation.

The simpower MATLAB tool box in simulink is used to simulate data fault features. Just by seeing and with some analysis we can determine the fault features in both open circuit and short circuit cases can be visually distinguished; however, the computation unit cannot directly visualize as like a human being. Normally the output signals corresponding to different faults will have high correlation that is why they can't

be distinguished easily. Therefore a signal transformation technique is required. An appropriate selection of the feature extractor is to provide the ANFIS with adequate significant details in the pattern set so that the highest degree of accuracy in the ANFIS performance can be obtained. One possible technique for implementation with a digital signal processing microchip is Fast Fourier Transform (FFT) [17].

Theoretical Background:

The two-sided Fourier transform is represented by Equation 4.4.1, and was widely used to investigate spectral phenomenon of time domain sequences:

$$F(\gamma)=\frac{1}{\sqrt{2\pi}}\int_{-\infty}^{\infty} f(t)e^{-j\omega t}dt \tag{4.4.1}$$

As advances were made in digital computers, research towards an algorithm that can more quickly perform the Fourier and its inverse transform was brought forth by Cooley and Tuckey in 1965. Starting with the discrete Fourier Transform in Equation (4.4.2), the FFT using the decimation in time decomposition algorithm is shown in Equation (4.4.3).

$$F_k=\sum_{n=0}^{N-1} f_n W_N^{nk} \quad \text{for k=0,.....,N-1} \tag{4.4.2}$$

Where $W_N = e^{-j2\pi/N}$

$$F_k = G_k + W_N^k H_k \qquad \text{for k=0,.....,} \frac{N}{2}-1$$

$$F_{k+\frac{N}{2}} = G_k - W_N^k H_k \qquad \text{for k=0,.....,} \frac{N}{2}-1 \tag{4.4.3}$$

The components G_k and H_k are computed in (4.4.4, 4.4.5), where:

$$G_k=\sum_{n=0}^{(N/2)-1} f_{2n} W_{N/2}^{nk} \tag{4.4.4}$$

$$H_k = \sum_{n=0}^{(N/2)-1} f_{2n+1} W_{N/2}^{nk} \qquad (4.4.5)$$

is for the odd-numbered elements of fn. Together, the computational savings of the FFT becomes $N \log x^N$ compared to N^2 for the DFT.

For detection purpose we will train the ANFIS so that it gives output 1 abnormal 0 for normal operation of the inverter. For example to train ANFIS corresponding to any one IGBT fault detection we will train that ANFIS with FFT samples corresponding to all cases i.e.,

i. FFT samples of single open IGBT fault when the extra leg is not included,
ii. FFT samples of single short IGBT fault when the extra leg is not included,
iii. FFT samples of single open IGBT fault when the extra leg is included and
iv. FFT samples of single open IGBT fault when the extra leg is included.

Each case will have 12 different situations corresponding to 12 IGBTs. We are also training the ANFIS with FFT samples corresponding to fault of IGBT when extra leg is included. It is because if we train the ANFIS with only 1st two situations the corresponding ANFIS structure is going to give the output as 1, using this output the isolation is going to isolate the faulted leg output to load. But in circuit configuration it is always present in the inverter circuits which will effects the FFT samples after reconfiguration. So if we don't train the ANFIS with these samples that structure is not going to detect the fault. Hence it is mandatory to train the ANFIS with the FFT samples corresponding to fault of IGBT when reconfiguration technique is included.

The main advantage with Adaptive Neuro Fuzzy Inference system is that we don't need expert knowledge for designing the system. Just by giving the input training data and target data we can design the system. And Accuracy of the system will be very high.

For training the ANFIS we have used Gaussian member ship functions for input and by default it's a Sugeno type so its output values will be crisp in nature whose value is linear function of input.

4.4.1 Normal Operation

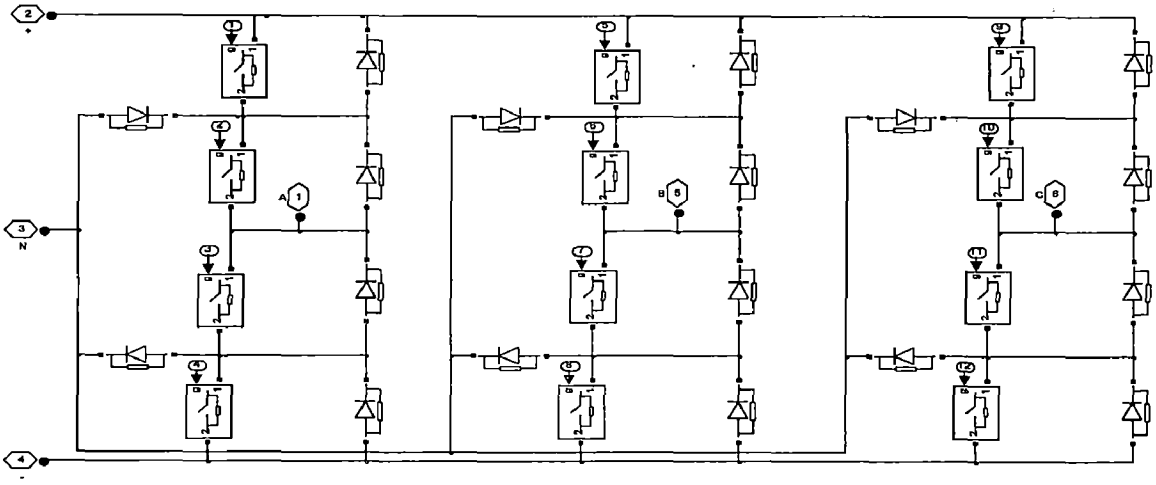

Fig.4.7 a. 3-Level inverter circuit

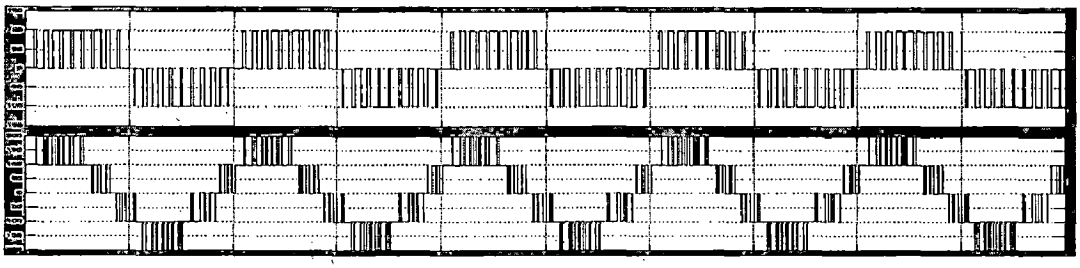

Fig.4.7 b. Phase-to-neutral voltage of Phase A and Phase-to-Phase voltage of Phase A and B

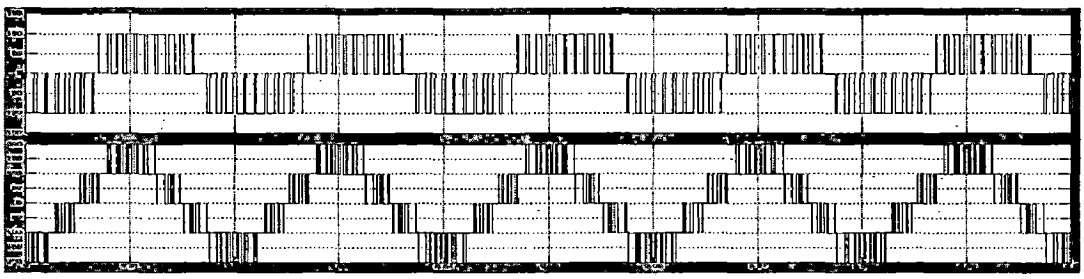

Fig.4.7 c. Phase-to-neutral voltage of Phase B and Phase-to-Phase voltage of Phase B and C

Fig.4.7 d. Phase-to-neutral voltage of Phase C and Phase-to-Phase voltage of Phase C and A

As can be seen from the Fig.4.7 that output voltages will not get affected because every switch is working properly.

4.4.2 Fault On Switch 1

i) Open fault

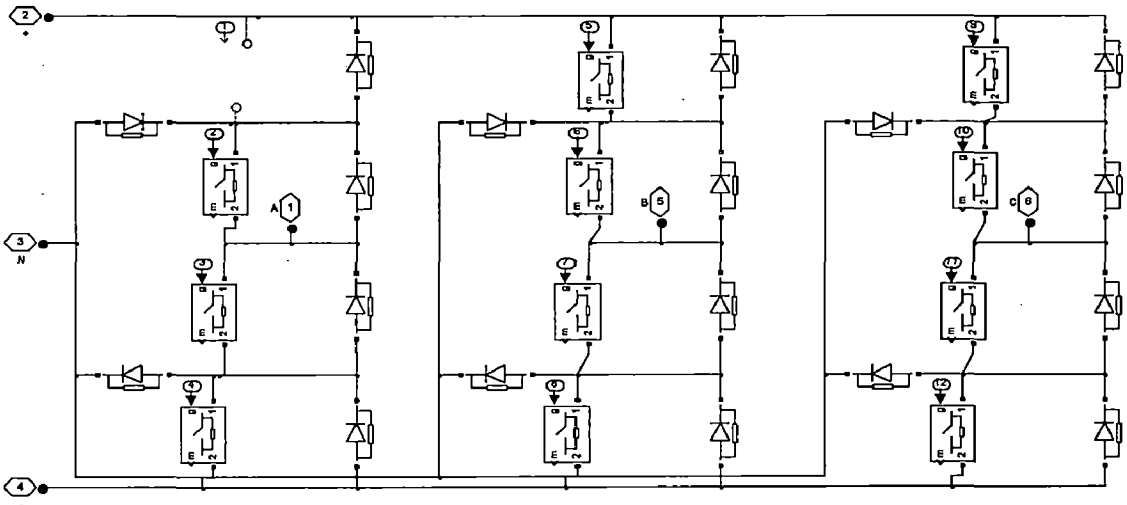

Fig.4.8 a. 3-level inverter circuit with open IGBT fault on switch 1

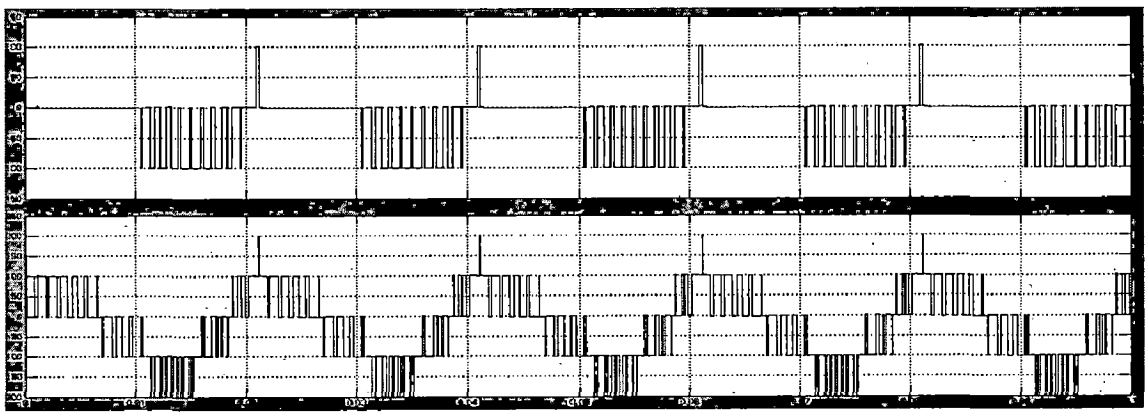

Fig.4.8 b. Phase-to-neutral voltage of Phase-A and Phase-to-Phase voltage of Phase A and B

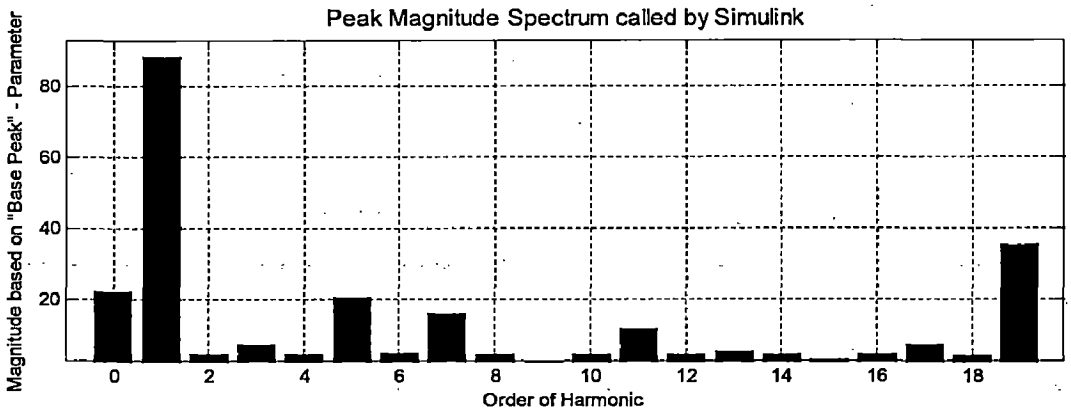

Fig.4.8 c. V_{AB} spectrum

ii) Short IGBT fault

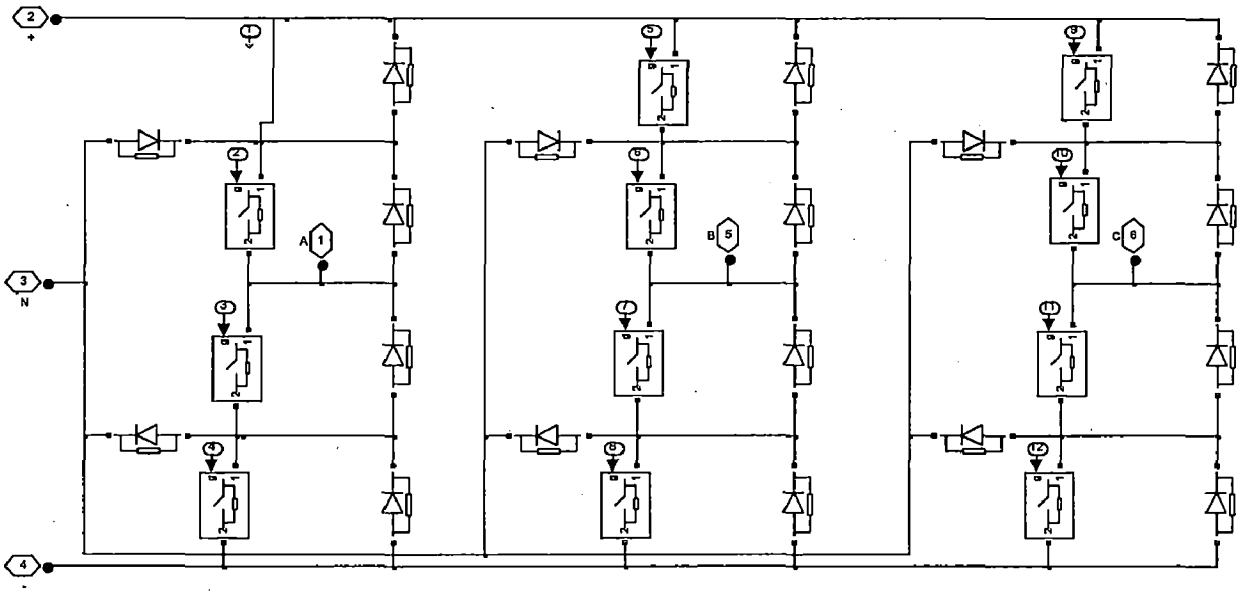

Fig.4.8 d. 3-level inverter circuit with short IGBT fault on switch 1

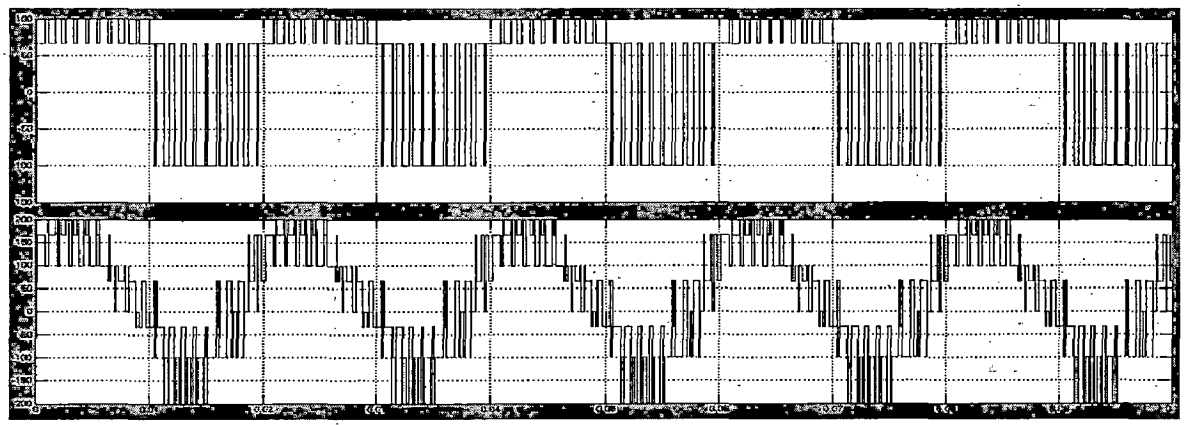

Fig.4.8 e. Phase-to-neutral voltage of Phase A and Line-to-Line voltage of Phase A and B

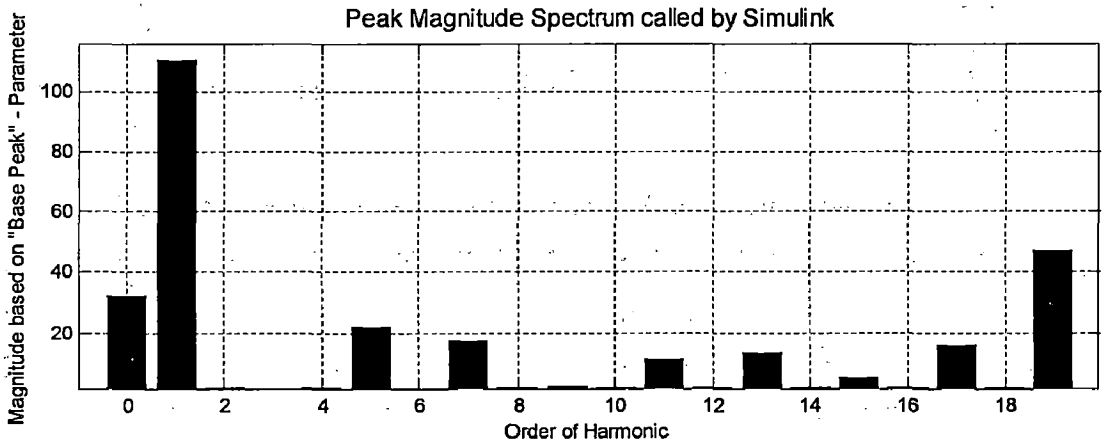

Fig.4.8 f. V_{AB} spectrum

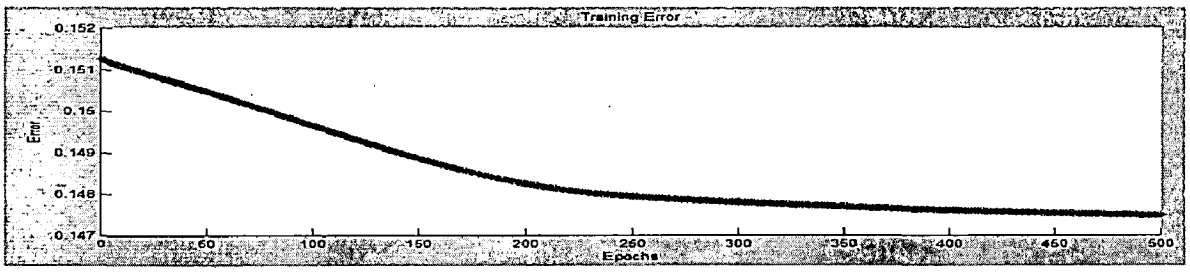

Fig.4.8 g. Anfis Training

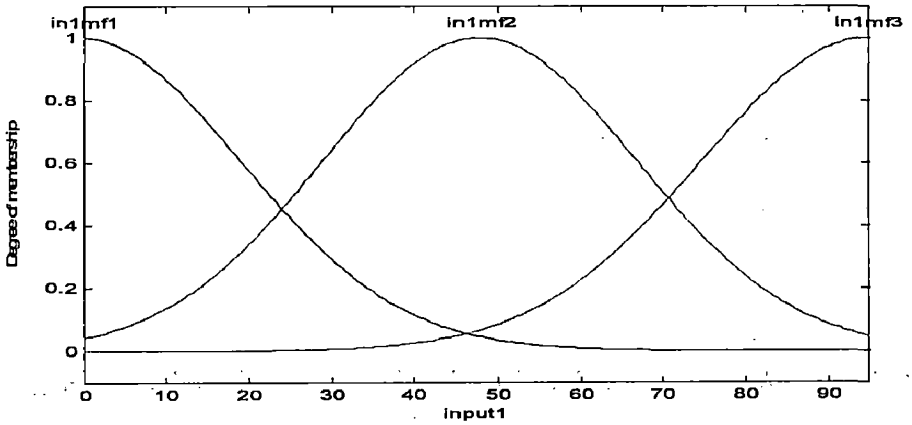

Fig.4.8 h. Input member ship function

Table 4.2 The member ship function ranges and Parameters for inputs:

Harmonic order	Range	parameters
1	0 to 95.02	[19.33 -0.3024]
2	0 to 112.5	[23.87 0.0002536]
3	0 to 24.91	[5.305 0.1201]
4	0 to 19.4	[4.035 0.2361]
5	0 to 12.83	[1.415 -1.419]

The Effect of these faults will be in V_{AB}, V_{BC} and V_{AN}, so only these output voltages will change. From Fig.4.8b and Fig.4.8e, the positive peaks are getting clipped it is because the switch S_1 is triggered for generating the $+V_{dc}/4$ and $+V_{dc}/2$ voltage levels.

4.4.3 Fault on Switch 2

i) Open fault

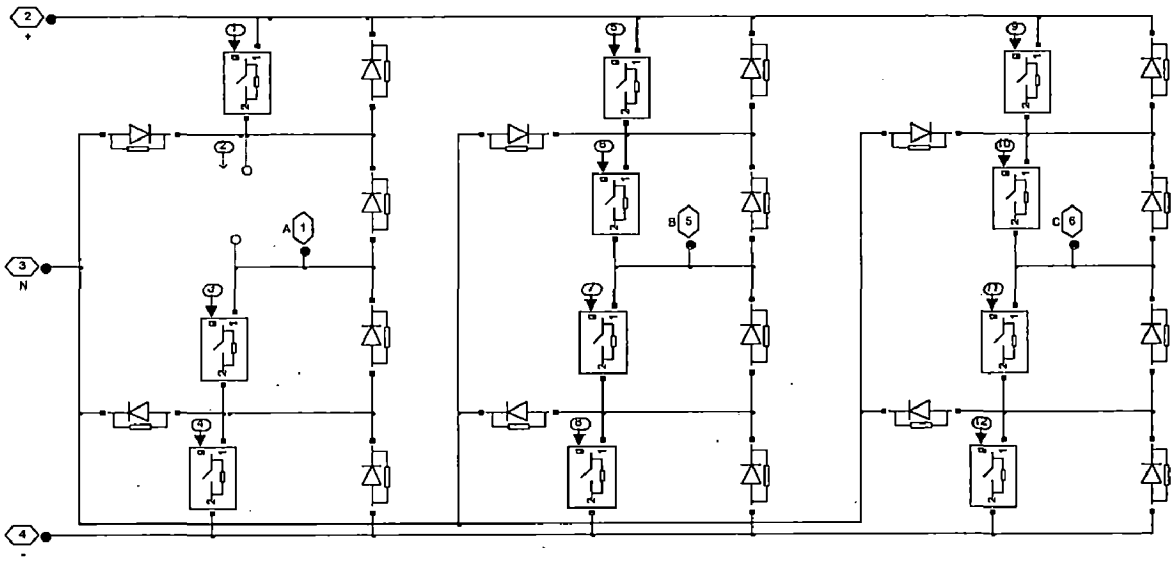

Fig.4.9 a. 3-level inverter circuit with open IGBT fault on switch 2

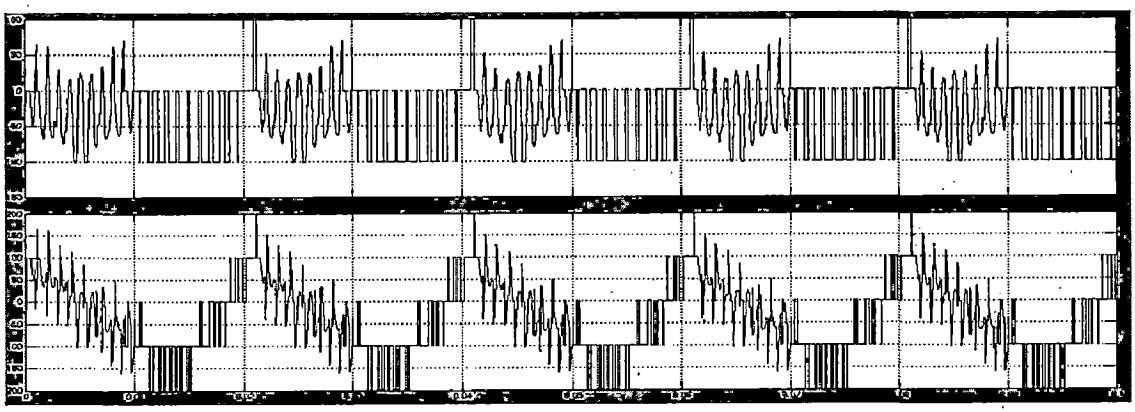

Fig 4.9 b. Phase-to-neutral voltage of Phase A and Phase-to-Phase voltage of Phase A and B

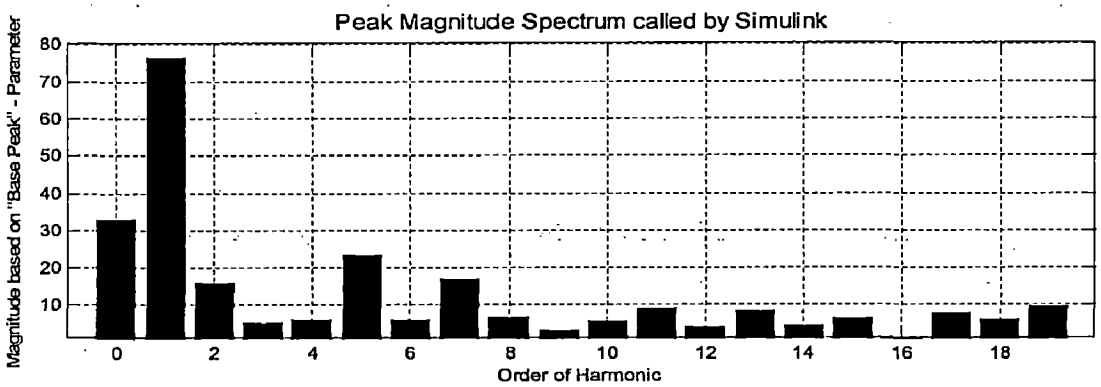

Fig.4.9 c. V_{AB} spectrum

ii) Short IGBT fault

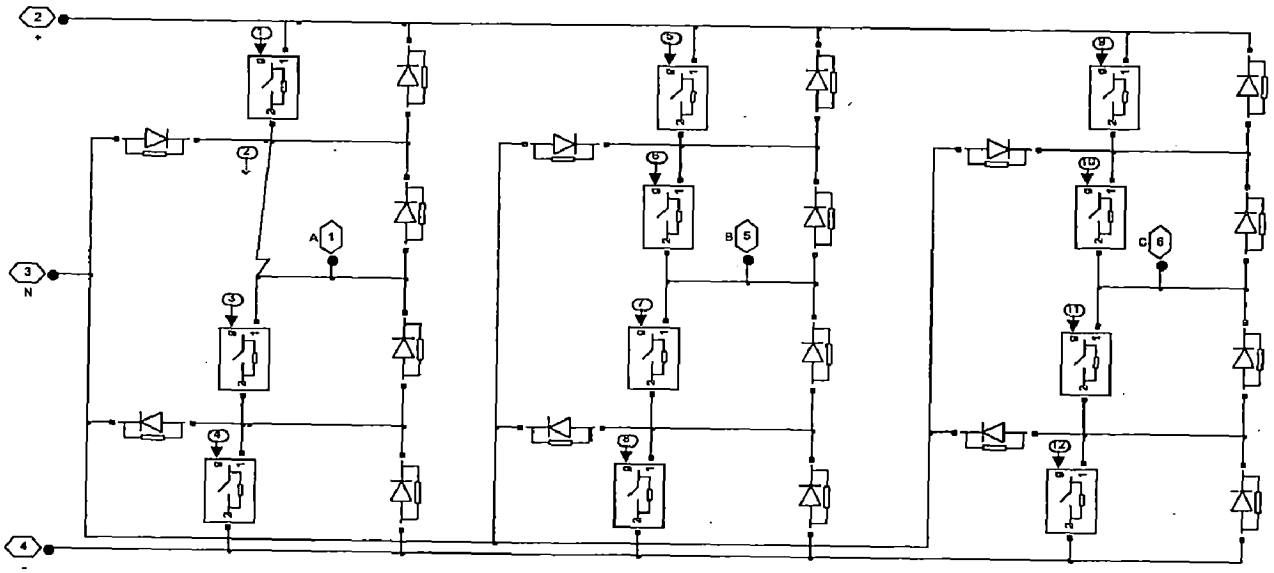

Fig.4.9 d. 3-level inverter circuit with short IGBT fault on switch 2

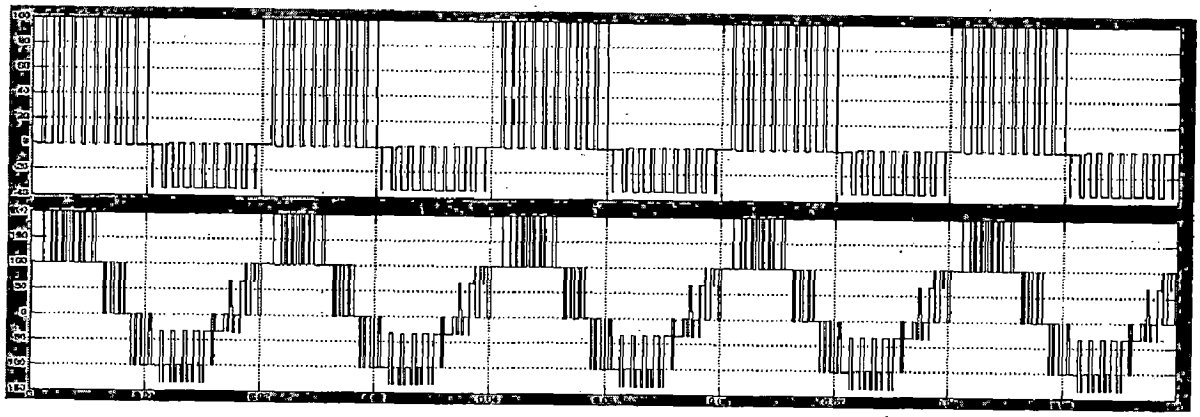

Fig.4.9 e. Phas-to-neutral voltage of Phase A and Line-to-Line voltage of Phase A and B

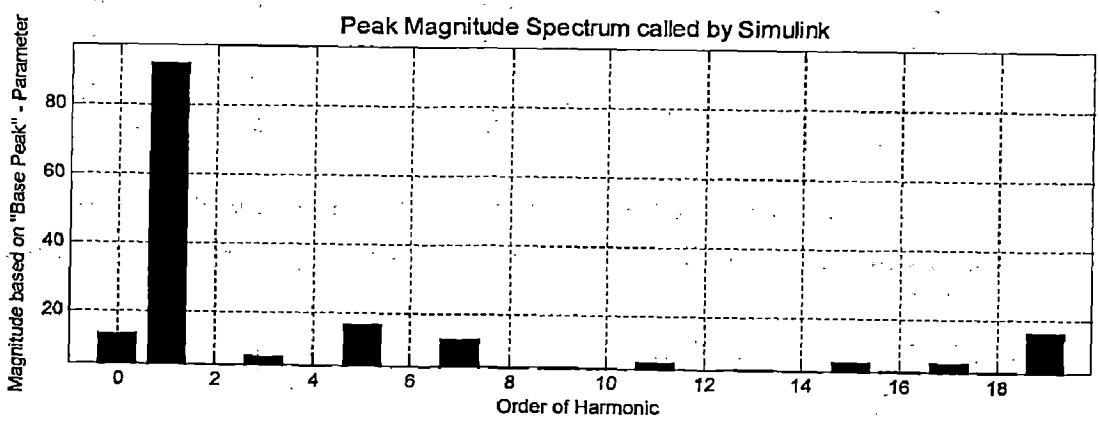

Fig.4.9 f. V_{AB} spectrum

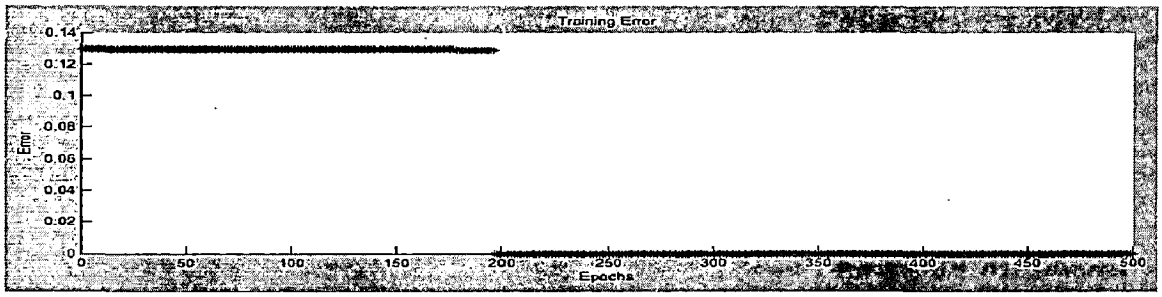

Fig.4.9 g. Anfis Training

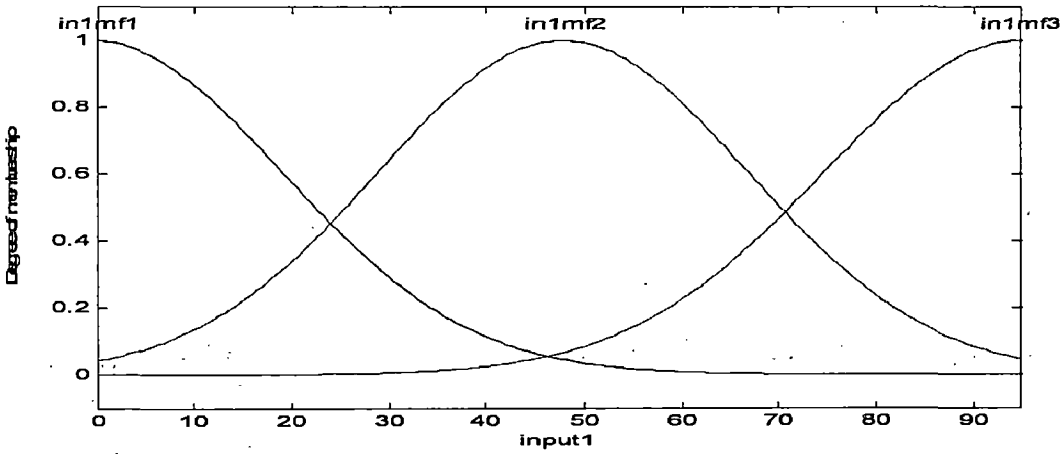

Fig.4.9 h. Input member ship function

Table 4.3 The member ship function ranges and Parameters for inputs:

Harmonic order	Range	parameters
1	0 to95.69	[18.82 -1.096]
2	0 to 112.5	[23.86 0.005173]
3	0 to 24.91	[4.805 -0.3154]
4	0 to 19.54	[2.562 0.777]
5	0 to 12.83	[1.992 0.1845

The Effect of these faults will be in V_{AB}, V_{BC} and V_{AN}, so only these output voltages will change for this type of fault. From the Fig.4.9b, Fig.4.9e it is shown that the positive values of output voltages are getting effected, because the switch S_2 is triggered to generate the $+V_{dc}/2$ and $+V_{dc}/4$ voltage levels.

4.4.4 Fault on Switch 3

i) Open fault

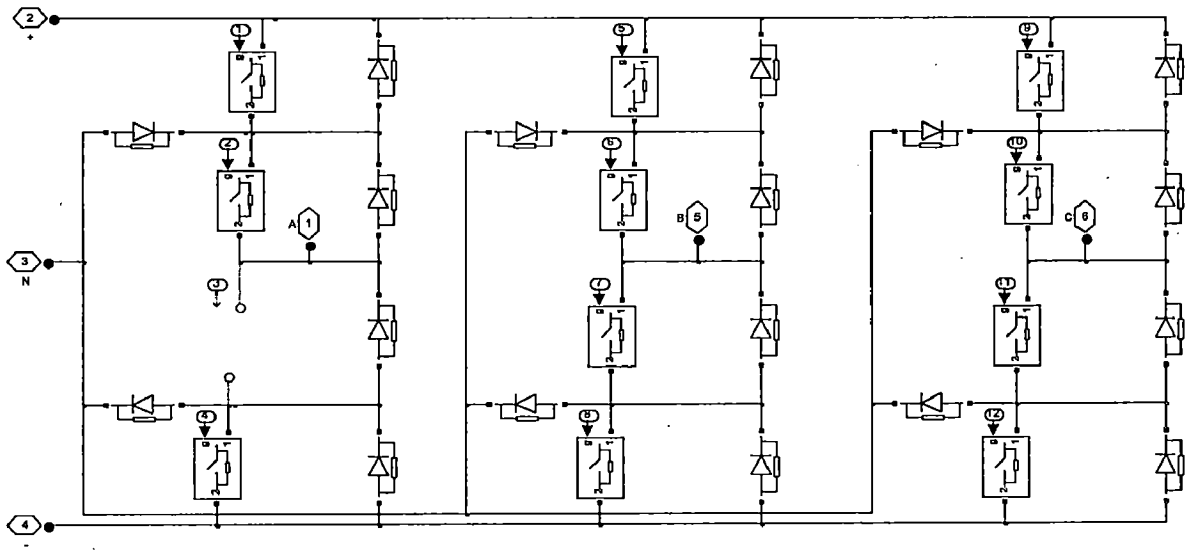

Fig.4.10 a. 3-level inverter circuit with open IGBT fault on switch 3

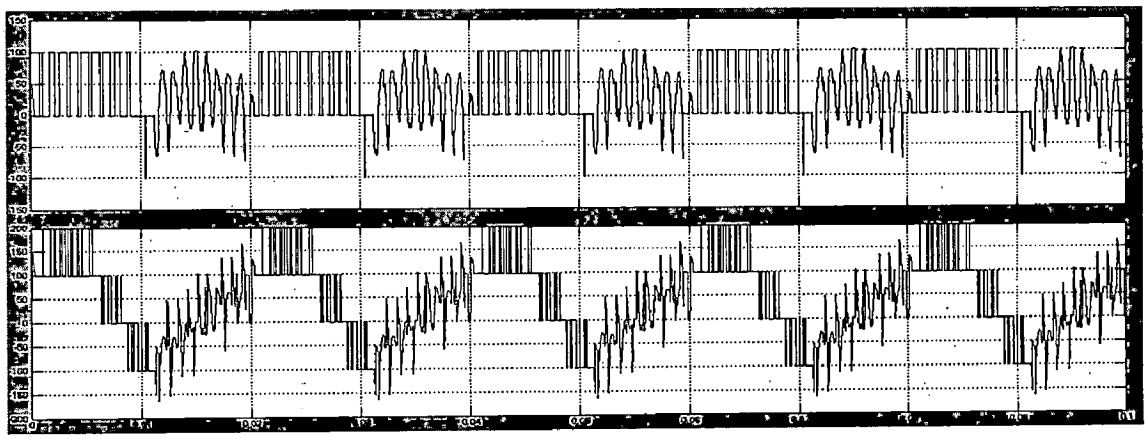

Fig 4.10 b. Phase-to-neutral voltage of Phase A and Phase-to-Phase voltage of Phase A and B

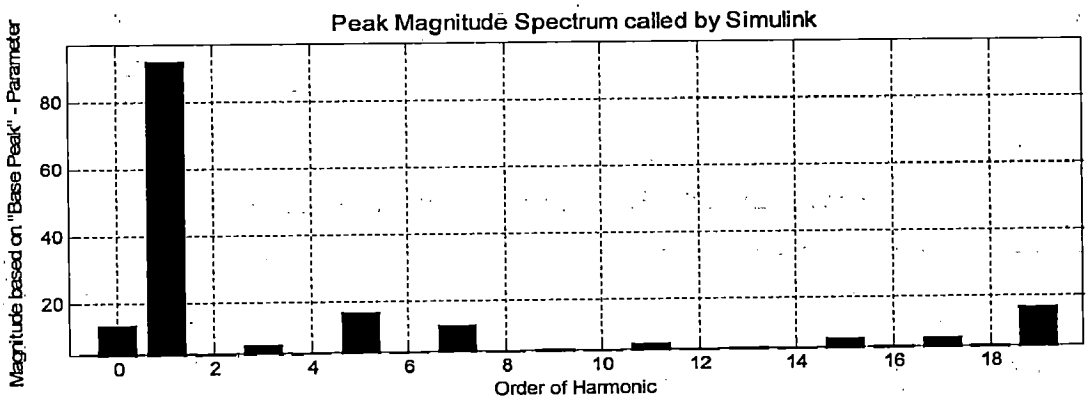

Fig 4.10 c. V_{AB} spectrum

ii) Short IGBT fault

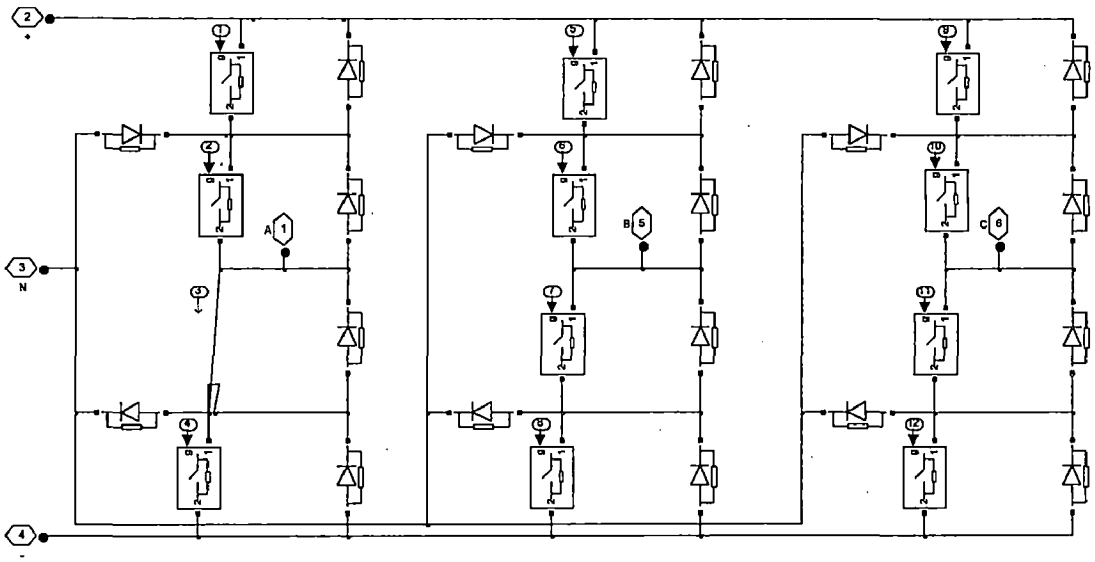

Fig.4.10 d. 3-level inverter circuit with short IGBT fault on switch 3

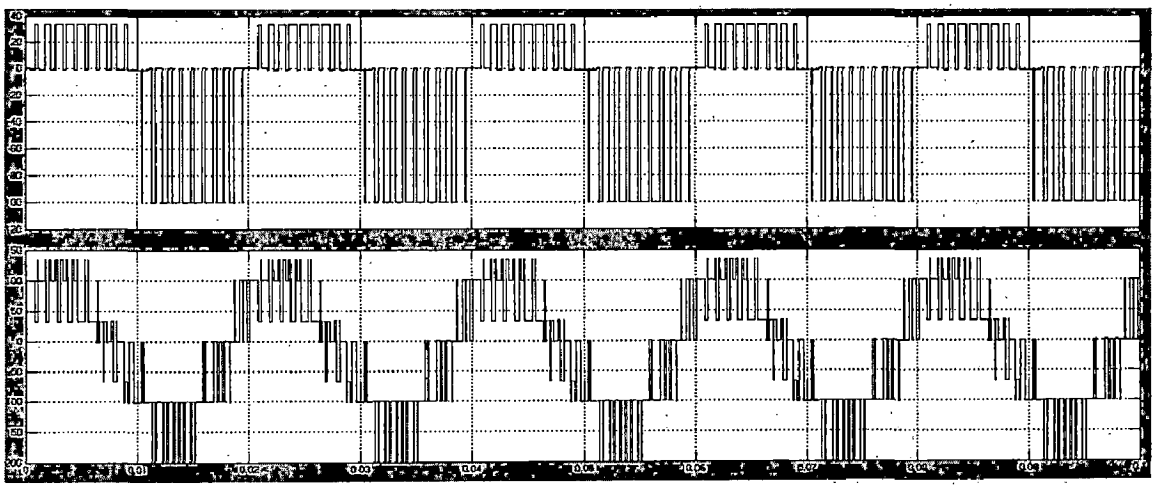

Fig.4.10 e. Phase-to-neutral voltage of Phase A and Phase-to-Phase voltage of Phase A and B

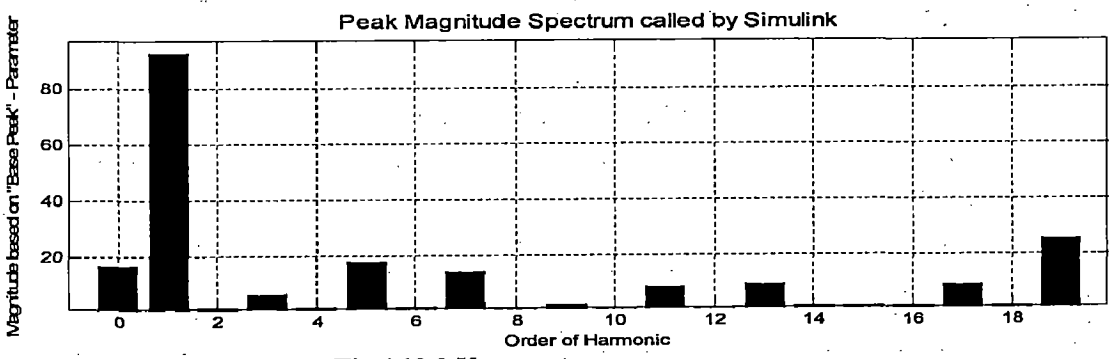

Fig.4.10 f. V_{AB} spectrum

Fig.4.10 g. Anfis Training

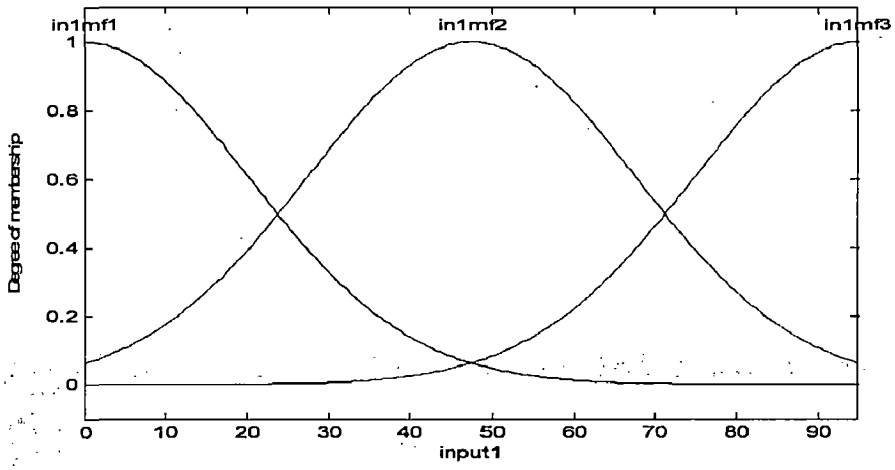

Fig.4.10 h. Input member ship function

Table 4.4 The member ship function ranges and Parameters for inputs:

Harmonic order	Range	parameters
1	0 to 95.02	[20.17 -0.003716]
2	0 to 112.5	[23.88 -0.0001804]
3	0 to 24.91	[5.256 -0.03845]
4	0 to 19.54	[3.896 -0.2499]
5	0 to 12.83	[1.839 -1.108]

The Effect of these faults will be in V_{AB}, V_{BC} and V_{AN}, so these output voltages will change for the fault on switch S_3. The Switch S_3 is triggered for generating the $-V_{dc}/2$ and $-V_{dc}/4$ levels. So these output voltages are getting affected which is obvious from the Fig.4.10b and Fig.4.10e.

4.4.5 Fault on Switch 4

i) Open fault

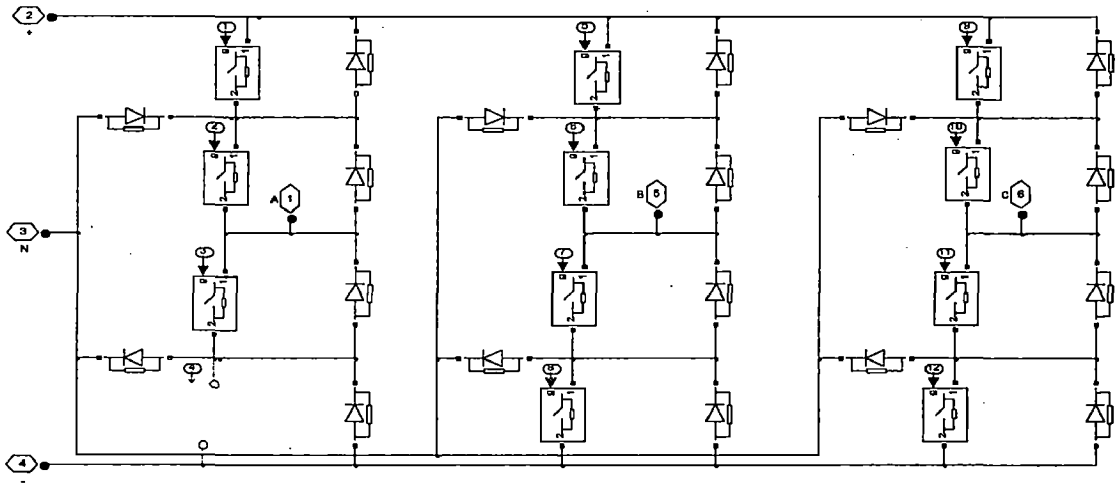

Fig.4.11 a. 3-level inverter circuit with open IGBT fault on switch 4

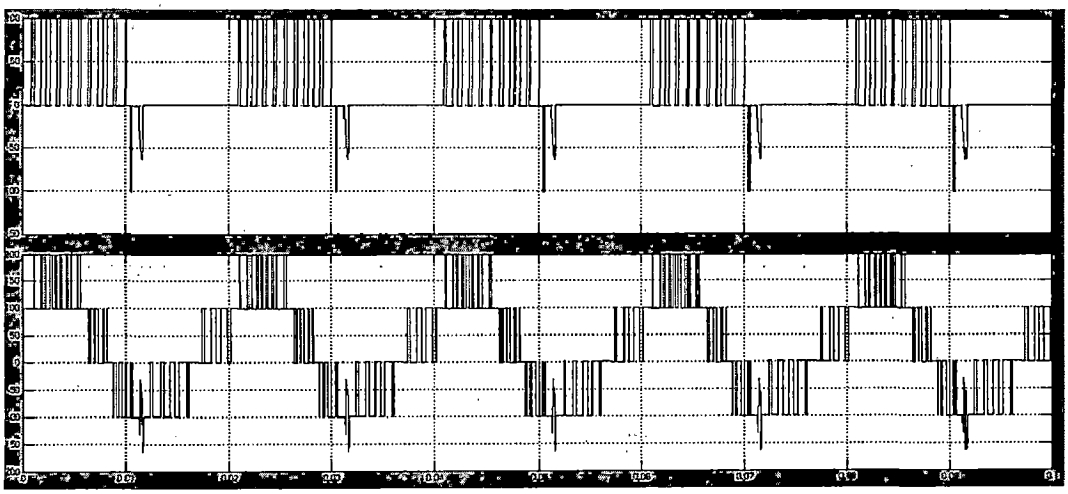

Fig.4.11 b. Phase-to-neutral voltage of Phase A and Phase-to-Phase voltage of Phase A and B

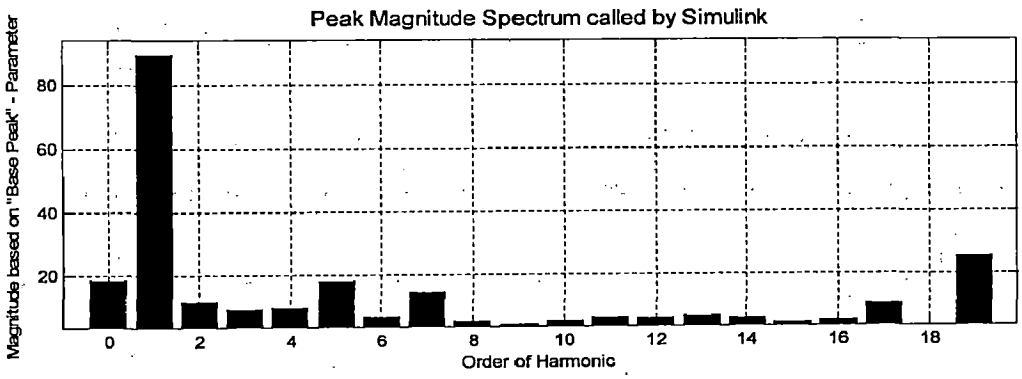

Fig.4.11 c. V_{AB} spectrum

ii) Short IGBT fault

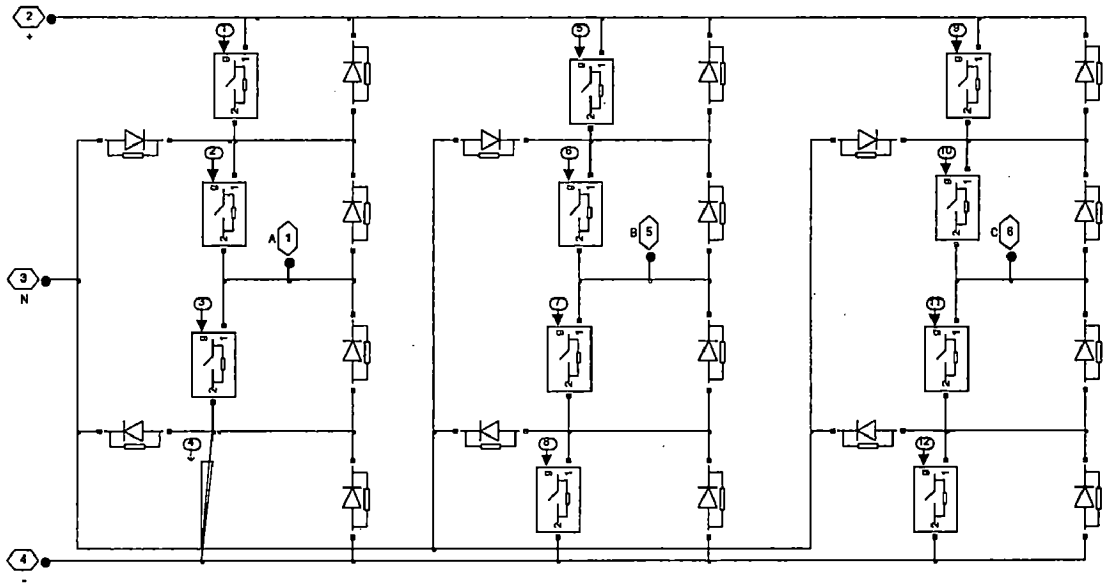

Fig.4.11 d. 3-level inverter circuit with short IGBT fault on switch 4

Fig.4.11 e. Phase-to-neutral voltage of Phase A and Phase-to-Phase voltage of Phase A and B

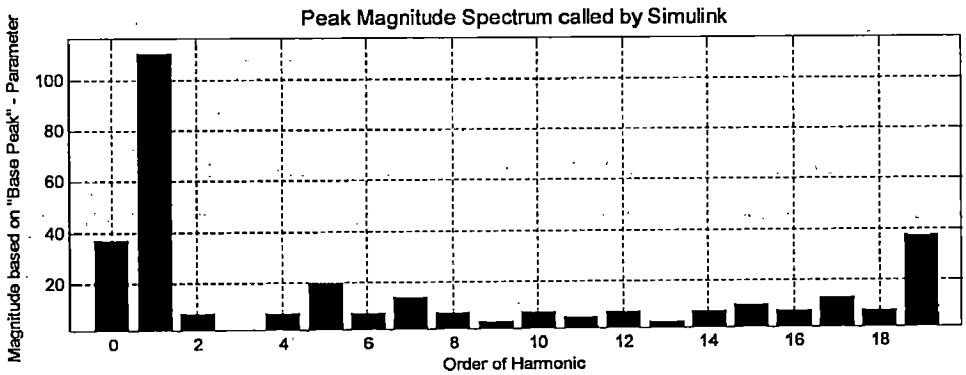

Fig.4.11 f. V_{AB} spectrum

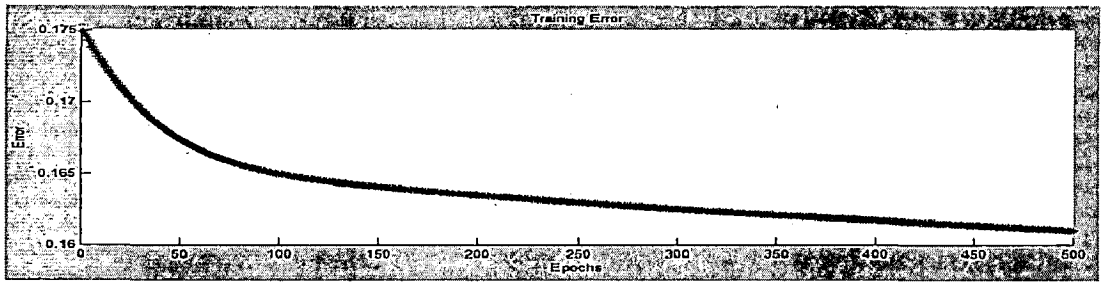

Fig.4.11 g. Anfis Training

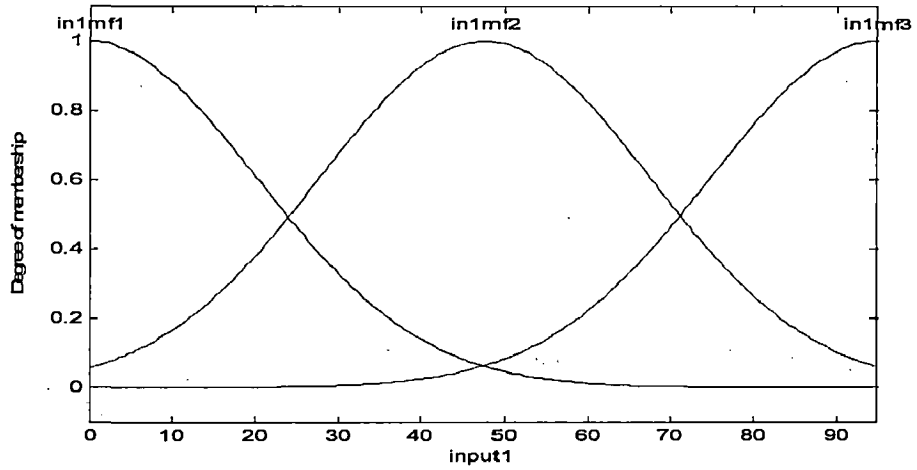

Fig.4.11 h. Input member ship function

Table 4.5 The member ship function ranges and Parameters for inputs:

Harmonic order	Range	parameters
1	0 to 95.02	[20.17 0.05624]
2	0 to 112.5	[23.88 0.001691]
3	0 to 24.91	[5.296 0.03987]
4	0 to 19.54	[4.079 -0.09206]
5	0 to 12.83	[0.8321 -1.382]

The Effect of these faults will be in V_{AB}, V_{BC} and V_{AN} so these output voltages will change for the fault on switch s_4. . The Switch S_4 is triggered for generating the $-V_{dc}/2$ and $-V_{dc}/4$ levels. So these output voltages are getting affected which is obvious from the Fig.4.11b and Fig.4.11e.

4.4.6 Fault on Switch 5

i) Open fault

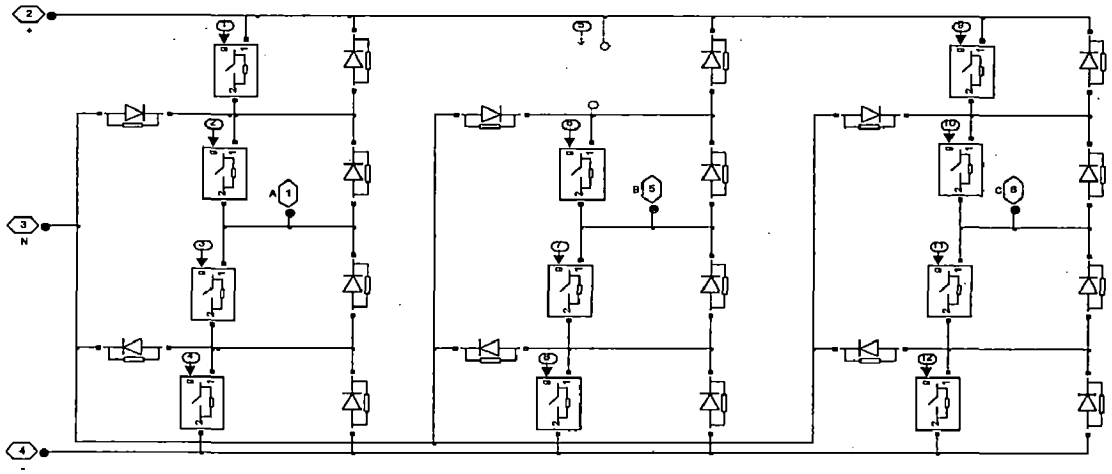

Fig.4.12 a. 3-level inverter circuit with open IGBT fault on switch 5

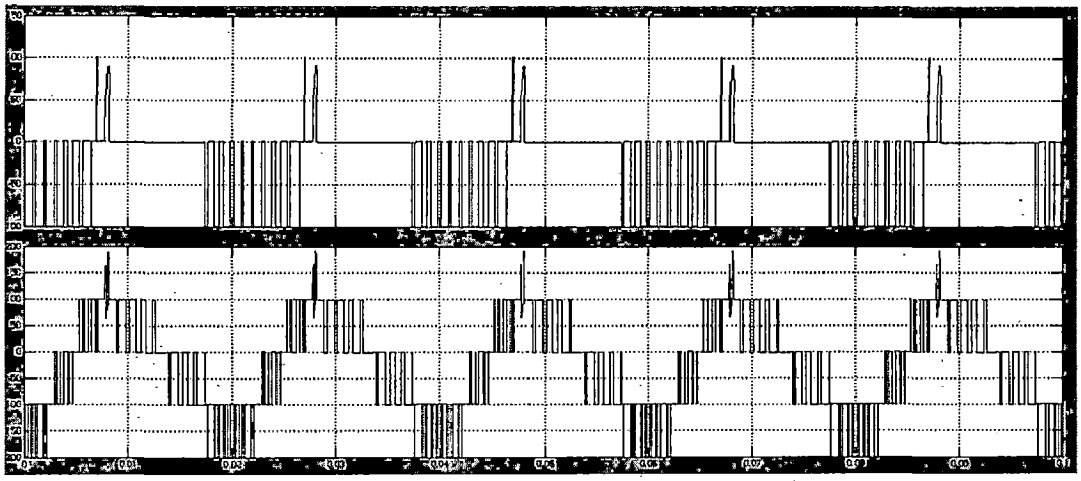

Fig.4.12 b. Phase-to-neutral voltage of Phase B and Phase-to-Phase voltage of Phase B and C

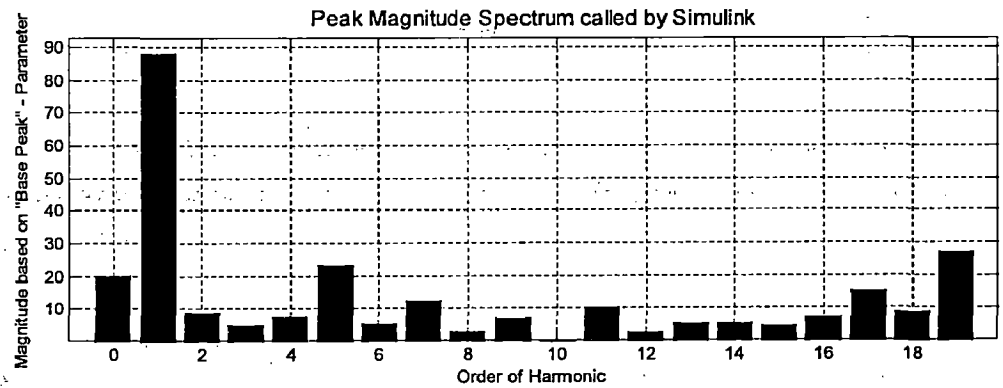

Fig.4.12 c. 3 V_{BC} spectrum

ii) Short IGBT fault

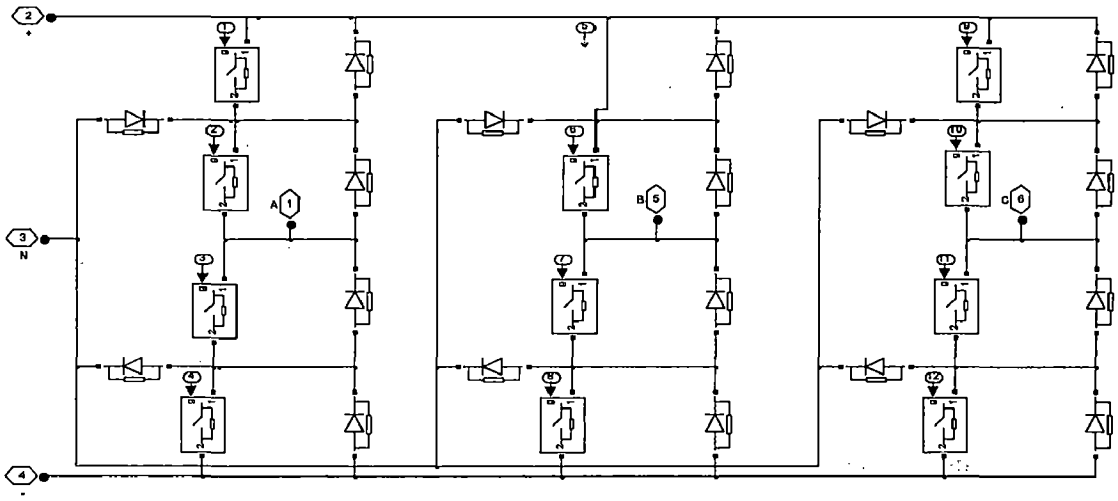

Fig.4.12 d. 3-level inverter circuit with short IGBT fault on switch 5

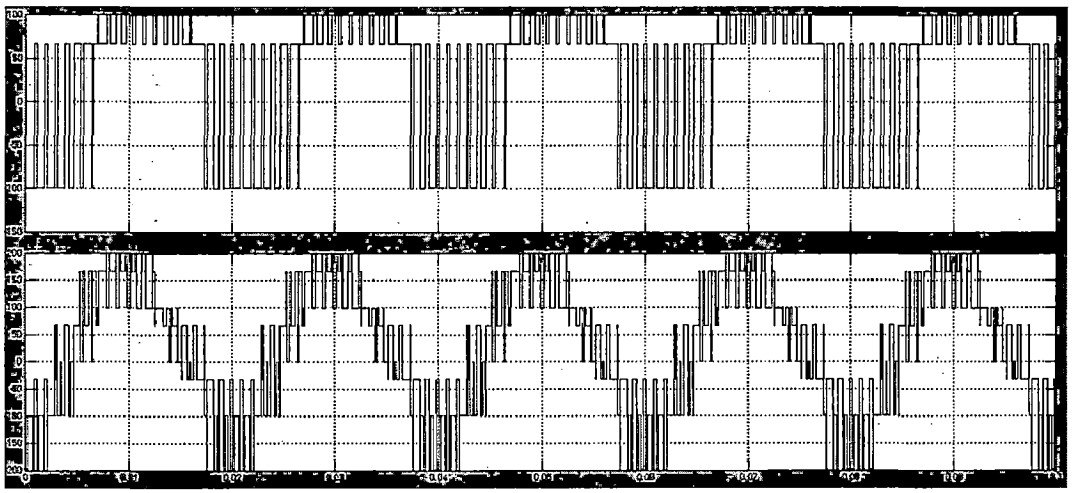

Fig.4.12 e. Phase-to-neutral voltage of Phase B and Phase-to-Phase voltage of Phase B and C

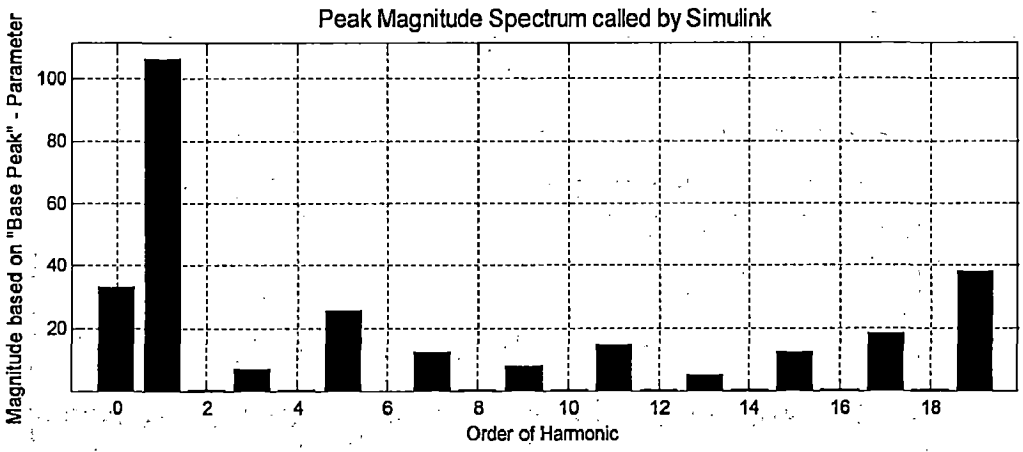

Fig.4.12 f. V_{BC} spectrum

Fig.4.12 g. Anfis Training

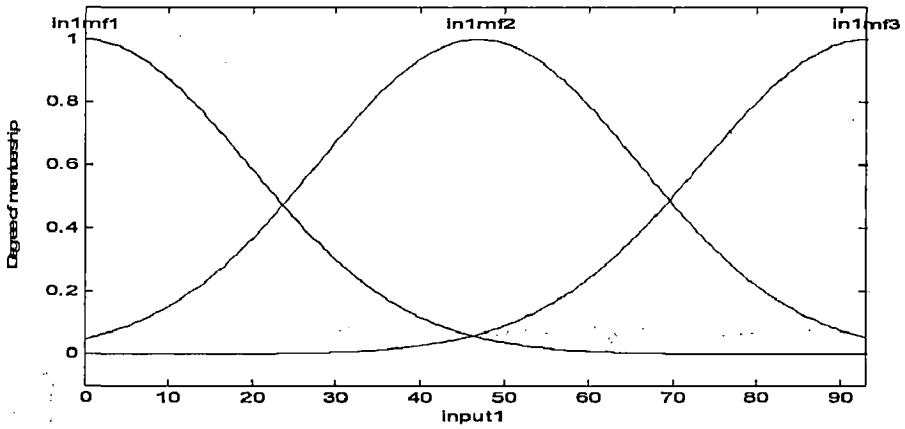

Fig.4.12 h. Input member ship function

Table 4.6 The member ship function ranges and Parameters for inputs:

Harmonic order	Range	parameters
1	0 to 93.17	[19.36 -0.005055]
2	0 to 110.2	[23.39 0.003772]
3	0 to 20.74	[0.3035 -0.7907]
4	0 to 20.06	[2.603 -0.6402]
5	0 to 8.99	[1.126 -0.8069]

The Effect of these faults will be in V_{AB}, V_{BC} and V_{BN}, so these output voltages will change for the fault on switch s_5. From the Fig.4.12b, Fig.4.12e it is obvious that the positive values of output voltages are getting effected, because the switch S_5 is helpful for generating $+V_{dc}/2$ and $+V_{dc}/4$ levels.

4.4.7 Fault on Switch 6

i) Open fault

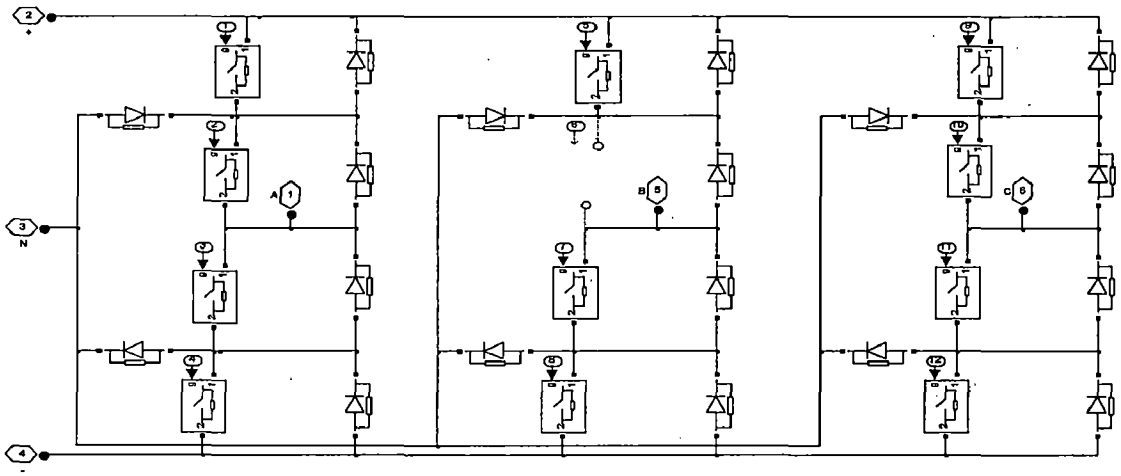

Fig.4.13 a. 3-level inverter circuit with open IGBT fault on switch 6

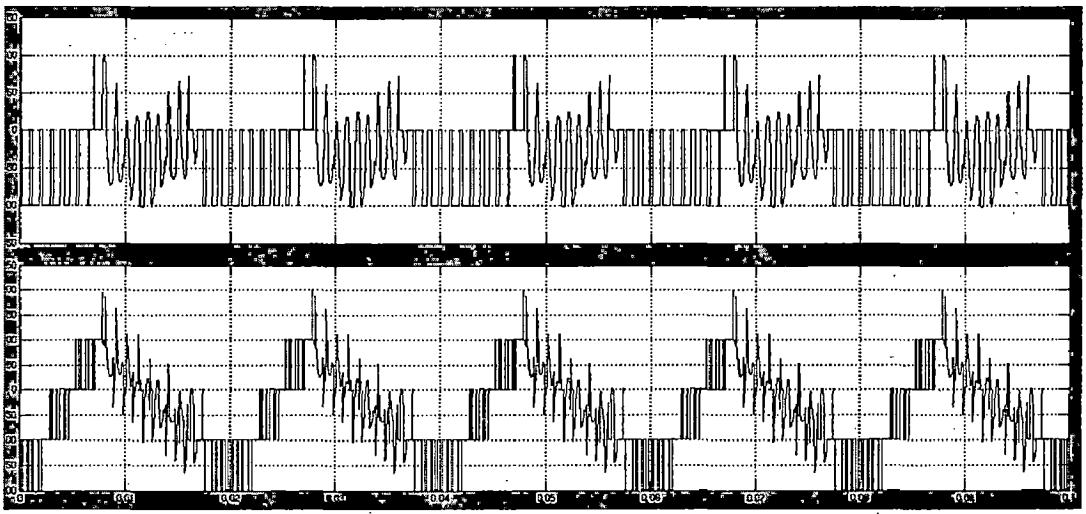

Fig 4.13.b. Phase-to-neutral voltage of Phase B and Phase-to-Phase voltage of Phase B and C

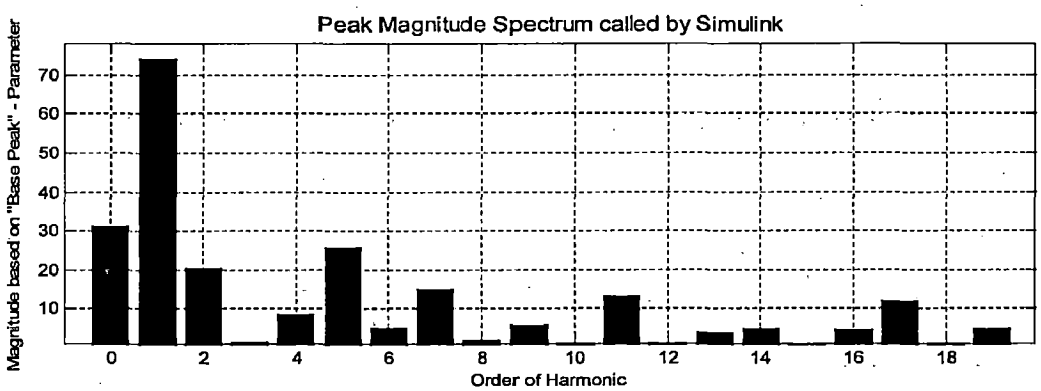

Fig.4.13 c. 3 V_{BC} spectrum

ii) Short IGBT fault

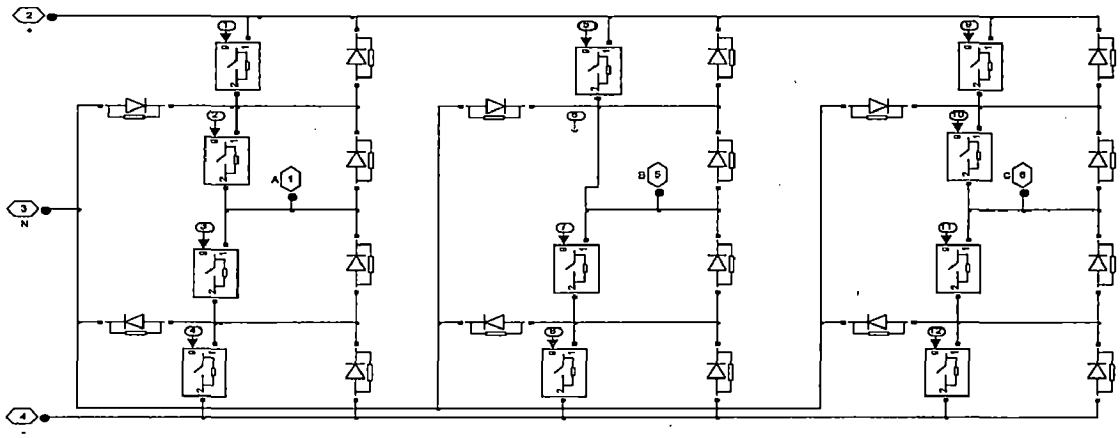

Fig.4.13 d. 3-level inverter circuit with short IGBT fault on switch 6

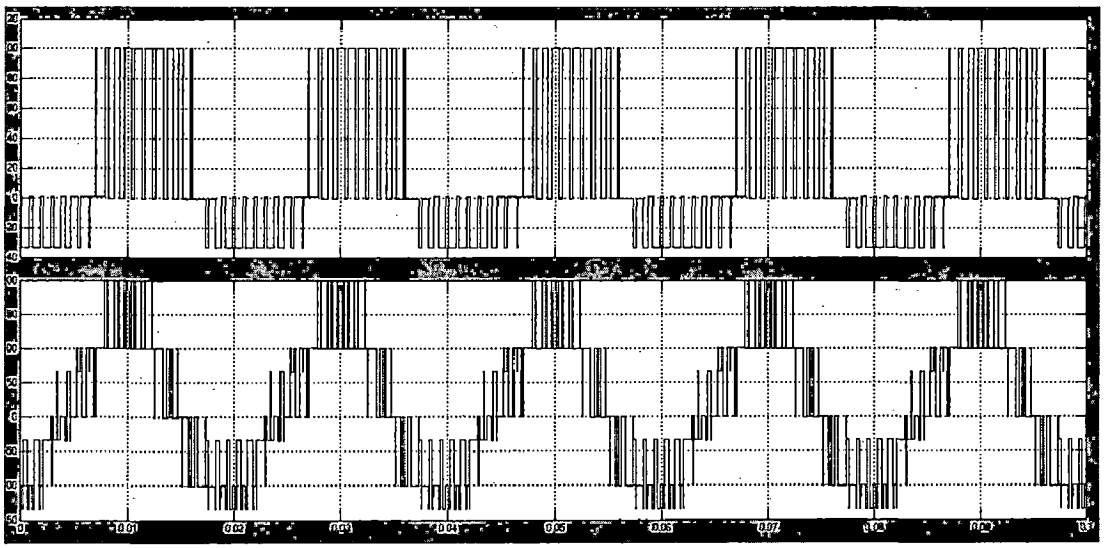

Fig.4.13 e. Phase-to-neutral voltage of Phase B and Phase-to-Phase voltage of Phase B and C

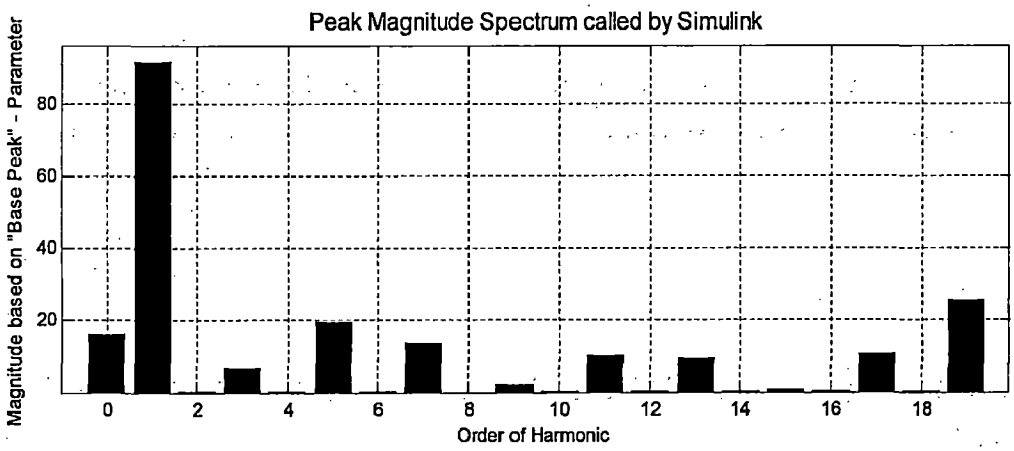

Fig.4.13 f. V_{BC} spectrum

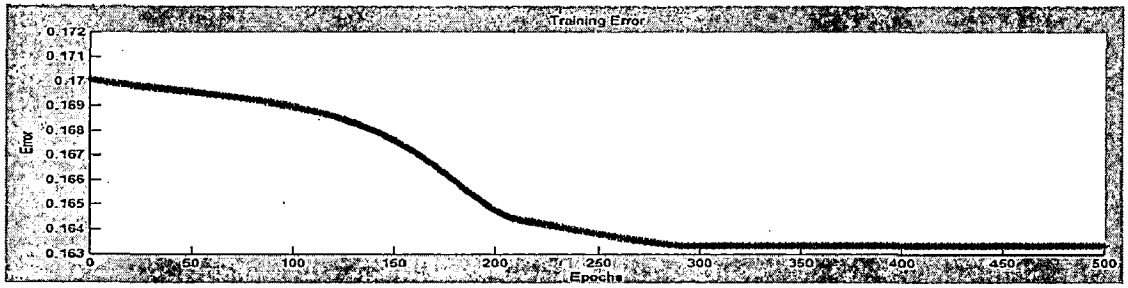

Fig.4.13 g. Anfis Training

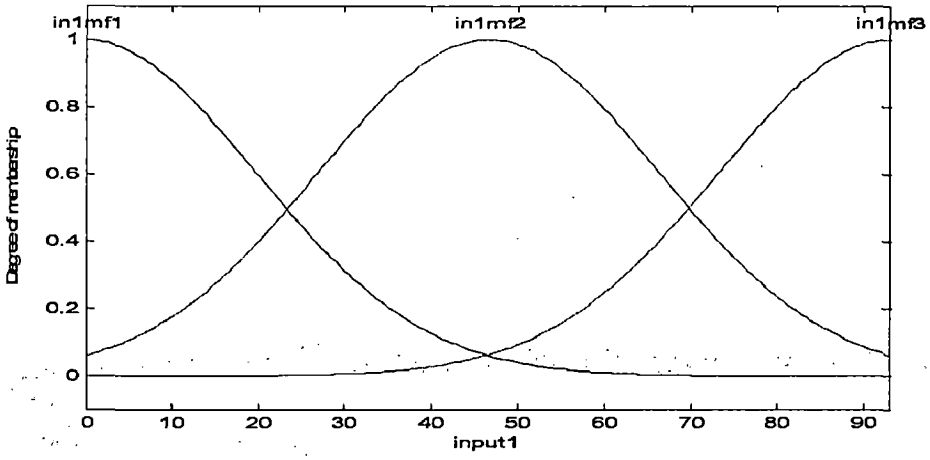

Fig.4.13 h. Input member ship function

Table 4.7 The member ship function ranges and Parameters for inputs:

Harmonic order	Range	parameters
1	0 to 93.17]	[19.72 -0.02075]
2	0 to 110.2]	[23.39 -0.001256]
3	0 to 20.74]	[4.092 -0.3092]
4	0 to 20.06]	[3.68 -0.2331]
5	0 to 8.99]	[0.6991 -1.156]

The Effect of these faults will be in V_{AB}, V_{BC} and V_{BN}, so these output voltages will change for the fault on switch s_6. From the Fig.4.13b, Fig.4.13e it is obvious that the positive values of output voltages are getting effected, because the switch S_6 is helpful for generating $+V_{dc}/2$ and $+V_{dc}/4$ levels.

4.4.8 Fault on Switch 7

i) Open fault

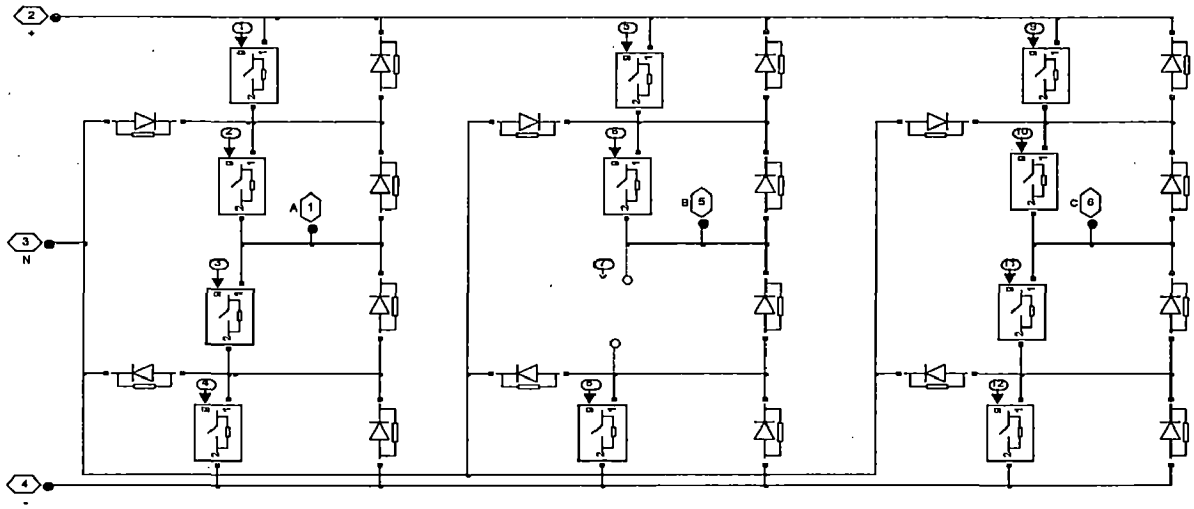

Fig.4.14 a. 3-level inverter circuit with open IGBT fault on switch 7

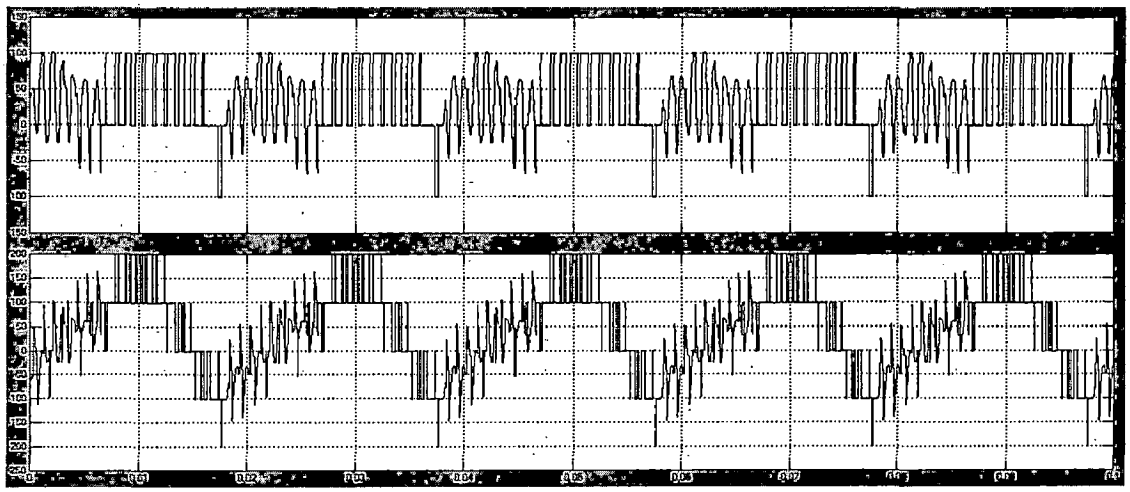

Fig.4.14 b. Phase-to-neutral voltage of Phase B and Phase-to-Phase voltage of Phase B and C

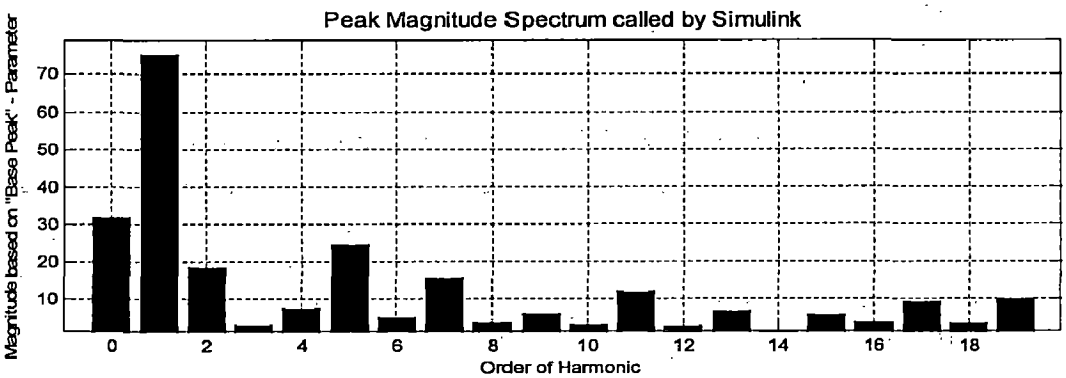

Fig.4.14 c. 3 V_{BC} spectrum

ii) Short IGBT fault

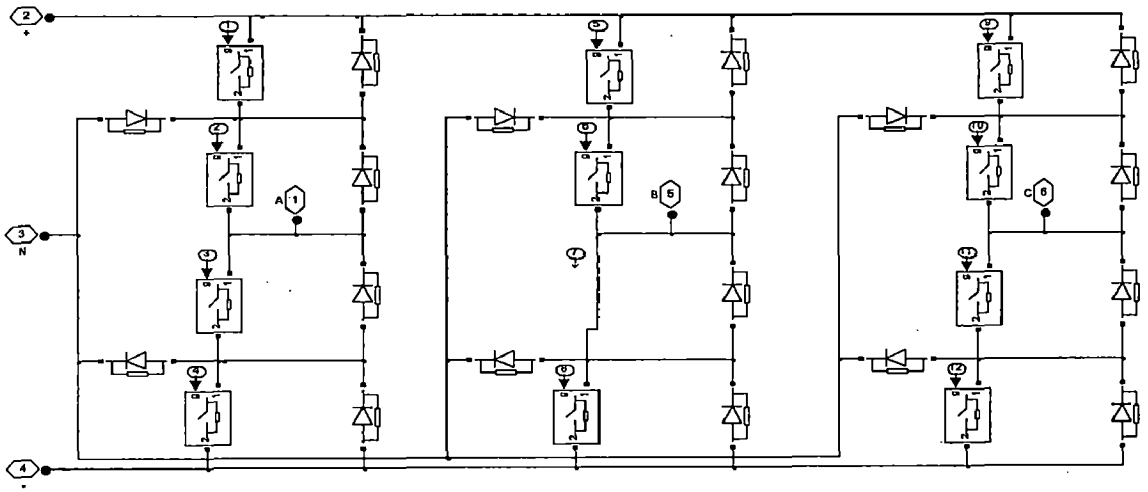

Fig.4.14 d. 3-level inverter circuit with short IGBT fault on switch 7

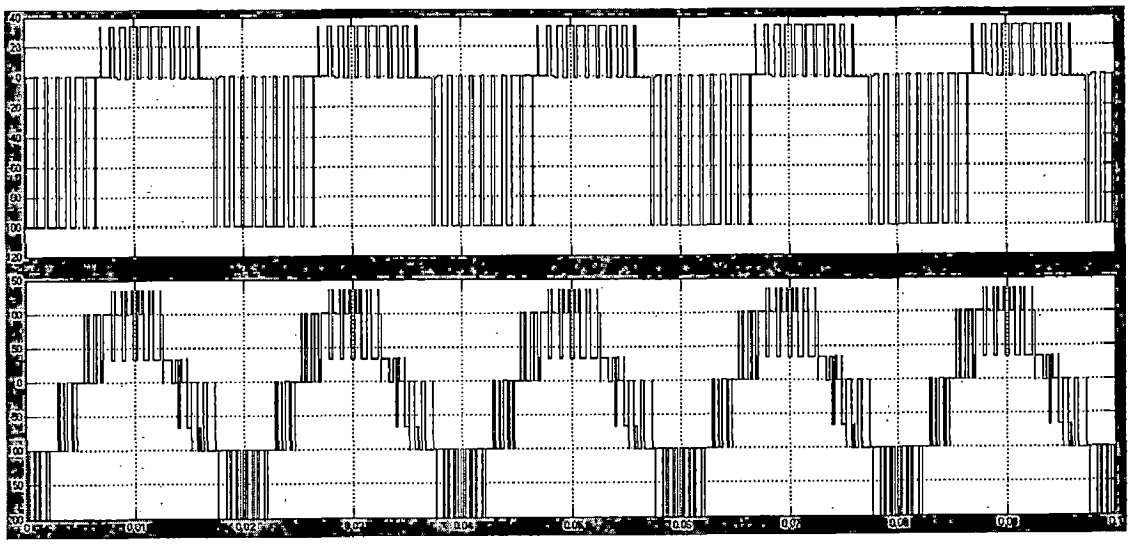

Fig.4.14 e. Phase-to-neutral voltage of Phase B and Phase-to-Phase voltage of Phase B and C

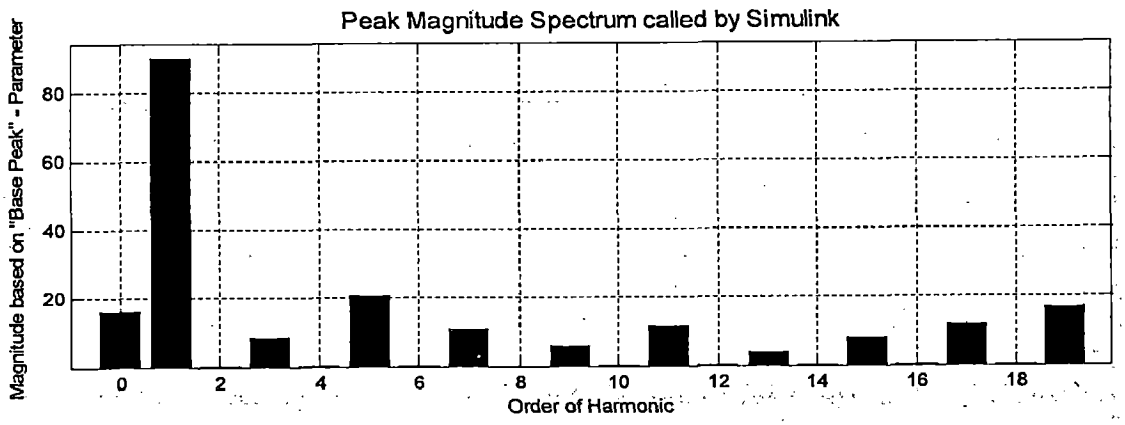

Fig.4.14 f. V_{BC} spectrum

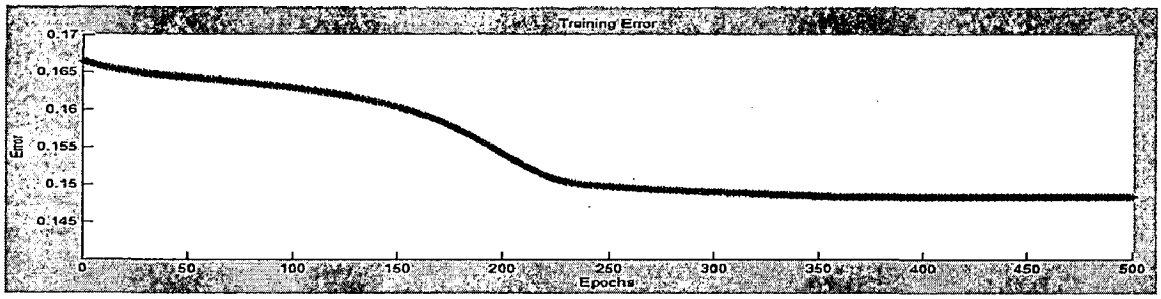

Fig.4.14 g. Anfis Training

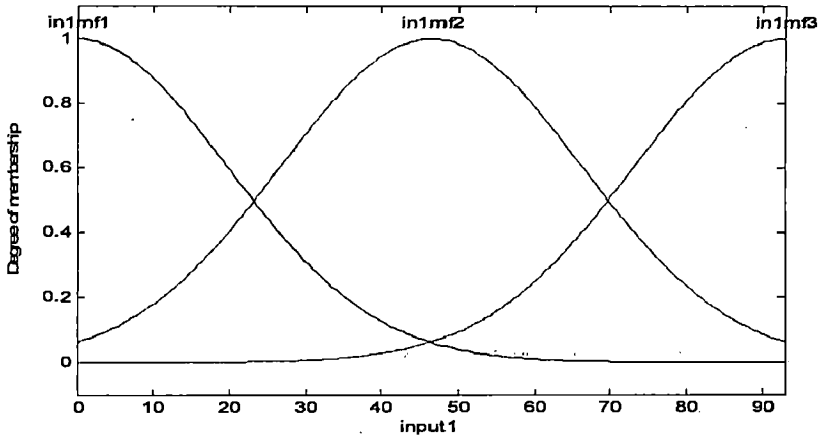

Fig.4.14 h. Input member ship function

Table 4.8 The member ship function ranges and Parameters for inputs:

Harmonic order	Range	parameters
1	0 to 92.96	[19.69 -0.02272]
2	0 to 110.2	[23.39 0.0005347]
3	0 to 20.71	[4.31 -0.1742]
4	0 to 20.06	[4.515 0.4262]
5	0 to 8.99	[0.2881 -0.6988]

The Effect of these faults will be in V_{AB}, V_{BC} and V_{BN}, so these output voltages will change for the fault on switch S_7. The Switch S_7 is triggered for generating the $-V_{dc}/2$ and $-V_{dc}/4$ levels. So these output voltages are getting affected which is obvious from the Fig.4.14b and Fig.4.14e.

4.4.9 Fault on Switch 8

i) Open fault

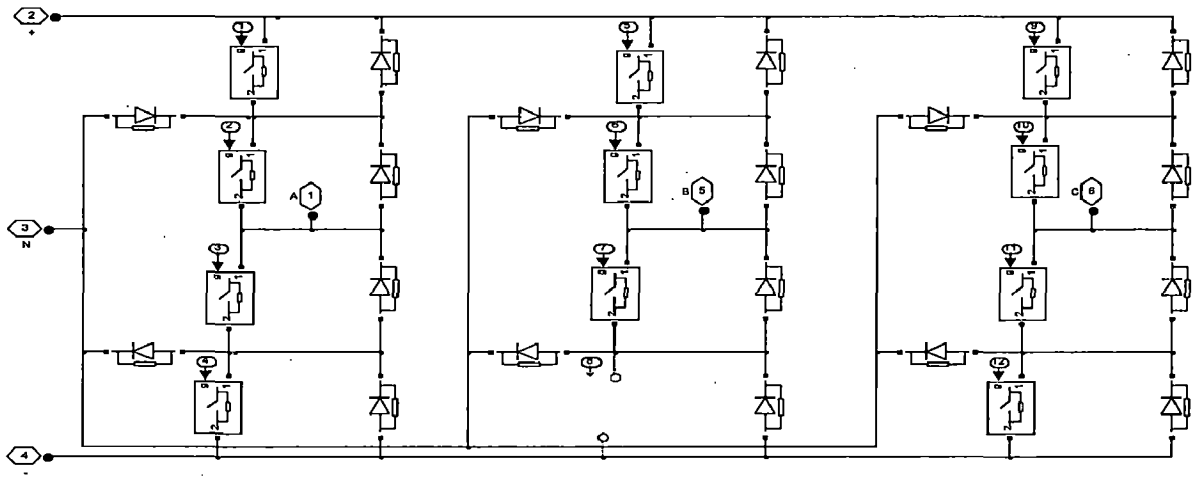

Fig.4.15 a. 3-level inverter circuit with open IGBT fault on switch 8

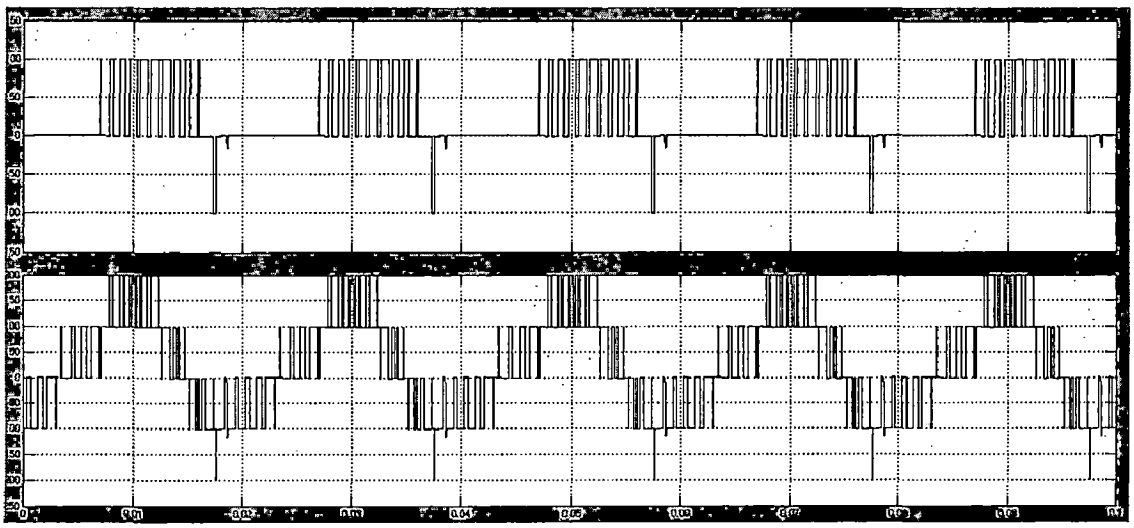

Fig.4.15 b. Phase-to-neutral voltage of Phase B and Phase-to-Phase voltage of B and C

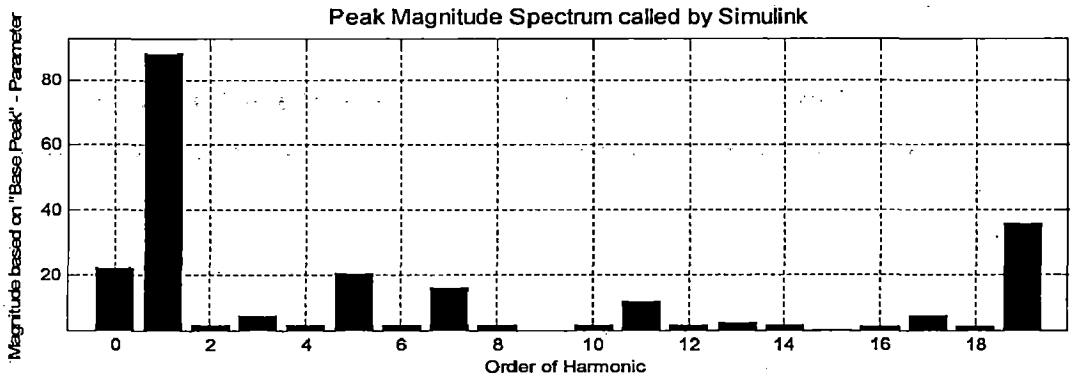

Fig.4.15 c. V_{BC} spectrum

ii) Short IGBT fault

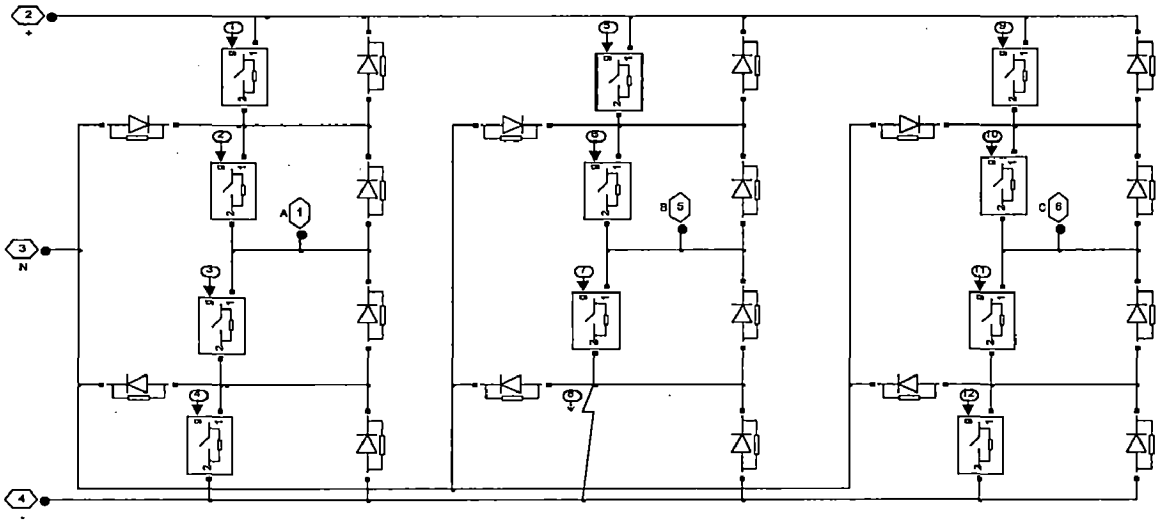

Fig.4.15 d. 3-level inverter circuit with short IGBT fault on switch 8

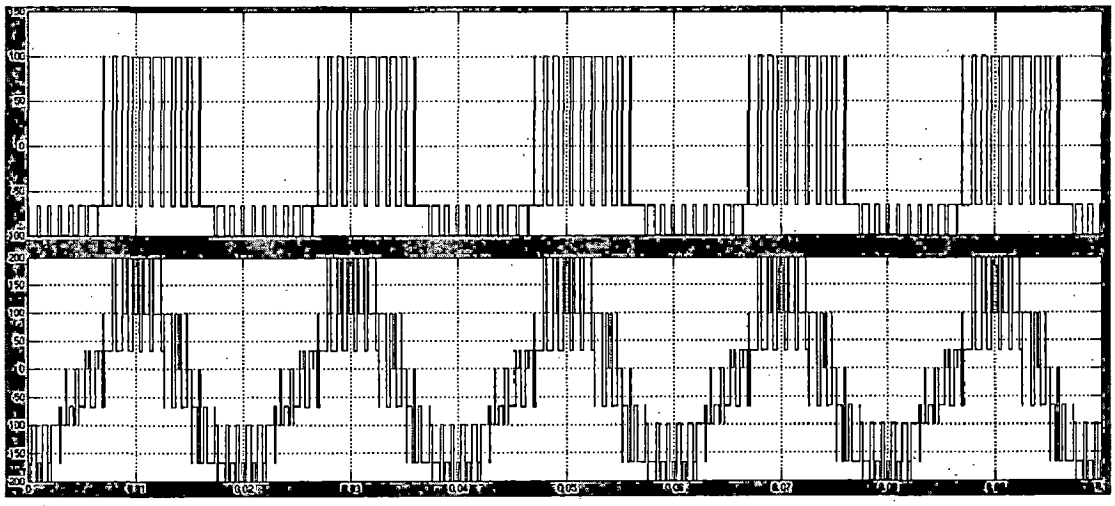

Fig.4.15 e. Phase-to-neutral voltage of Phase B and Phase-to-Phase voltage of B and C

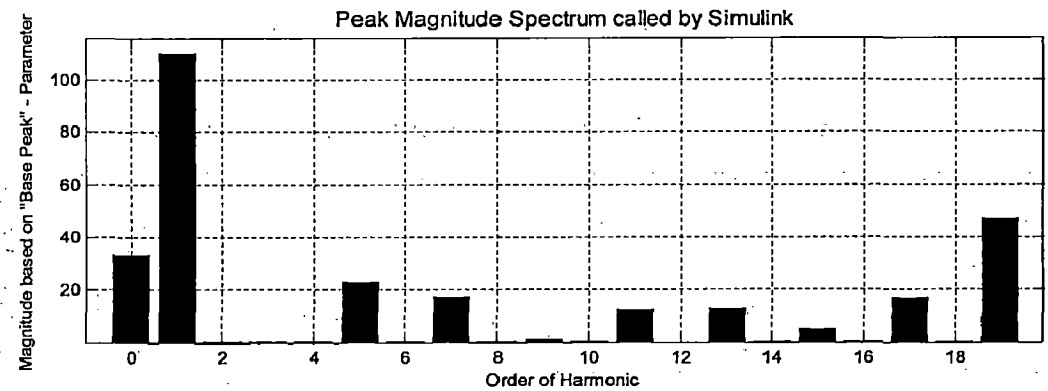

Fig.4.15 f. V_{BC} spectrum

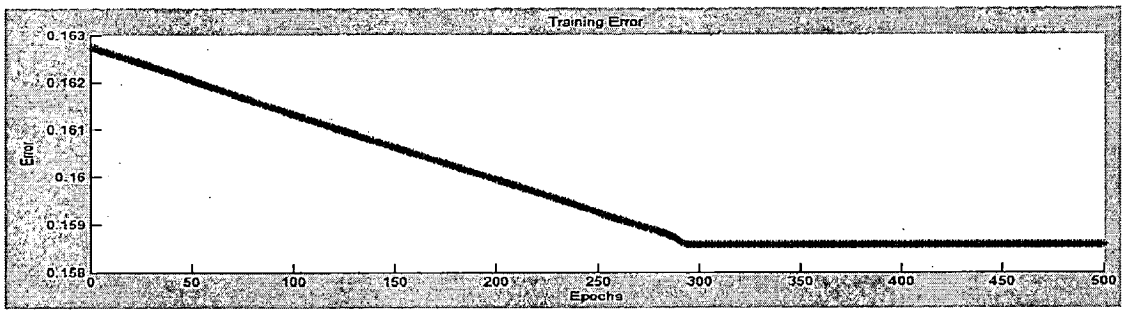

Fig.4.15 g. Anfis Training

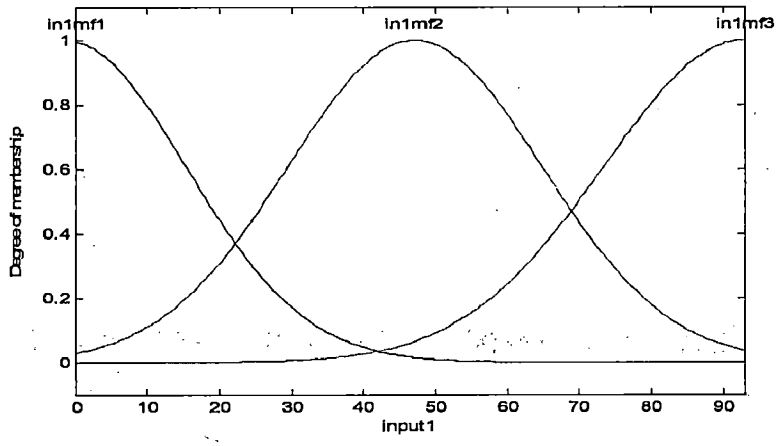

Fig.4.15 h. Input member ship function

Table 4.9 The member ship function ranges and Parameters for inputs:

Harmonic order	Range	parameters
1	0 to 92.96	[16.67 -1.246]
2	0 to 110.2	[23.38 0.002117]
3	0 to 20.71	[2.897 -2.375]
4	0 to 20.06	[5.123 0.41]
5	0 to 8.99	[0.3111 -1.163]

The Effect of these faults will be in V_{AB}, V_{BC} and V_{BN}, so these output voltages will change for the fault on switch S_8. The Switch S_8 is triggered for generating the $-V_{dc}/2$ and $-V_{dc}/4$ levels. So these output voltages are getting affected which is obvious from the Fig.4.15b and Fig.4.15e.

4.4.10 Fault on Switch 9

i) Open fault

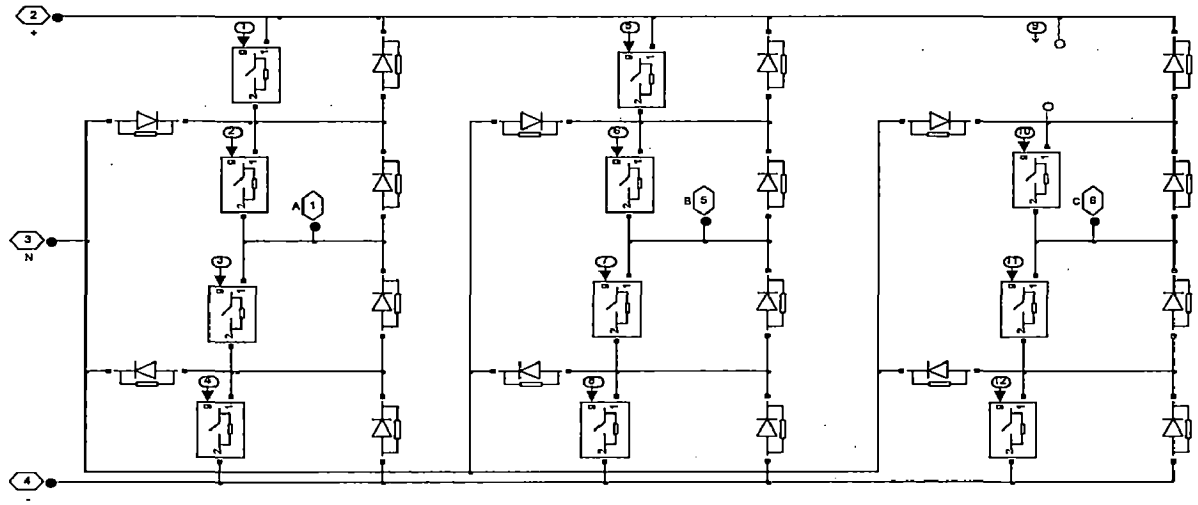

Fig.4.16 a. 3-level inverter circuit with open IGBT fault on switch 9

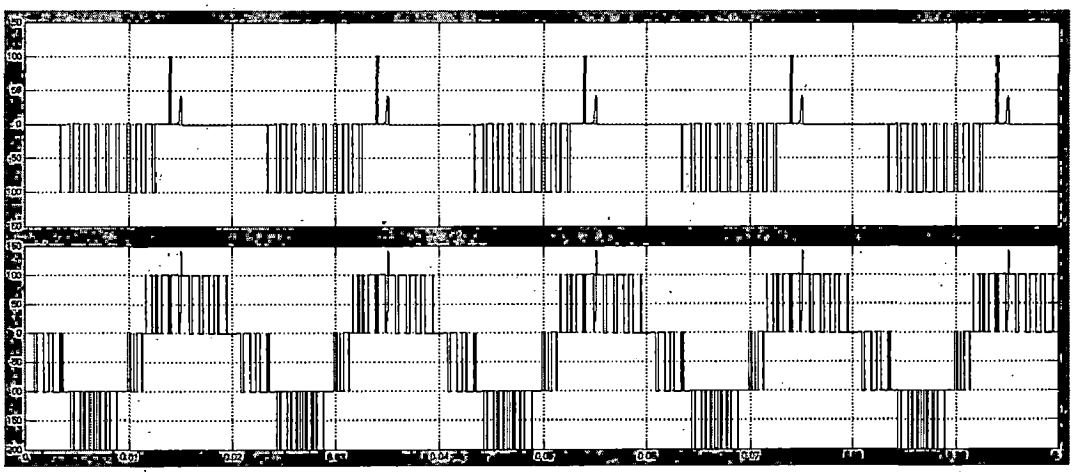

Fig.4.16 b. Phase-to-neutral voltage of Phase C and Phase-to-Phase voltage of C and A

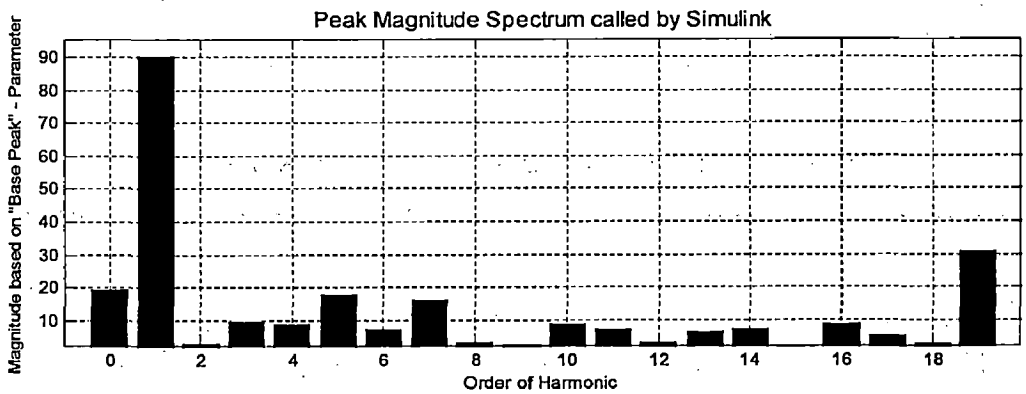

Fig.4.16 c. V_{CA} spectrum

ii) Short IGBT fault

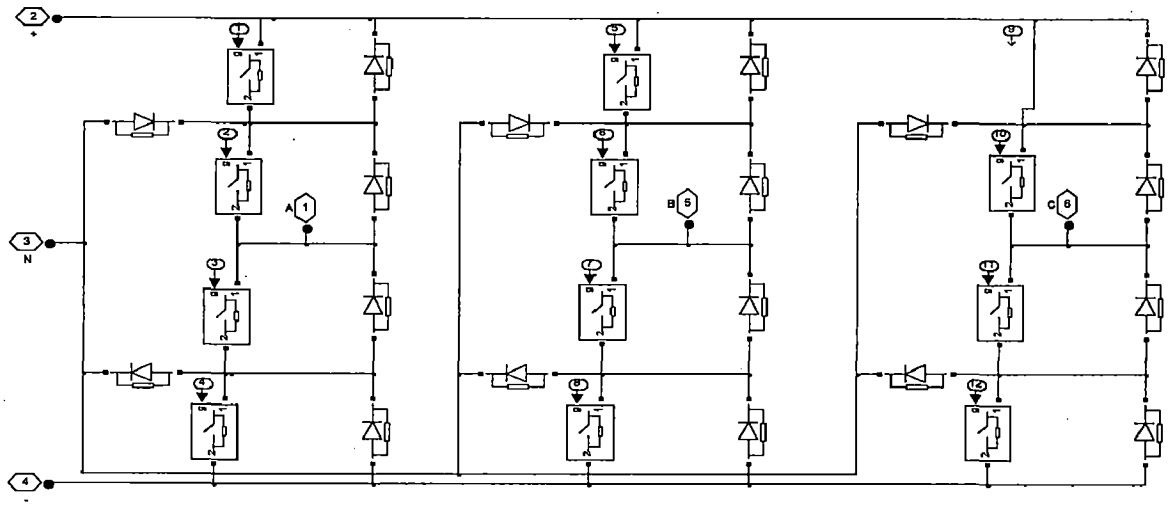

Fig.4.16 d. 3-level inverter circuit with short IGBT fault on switch 9

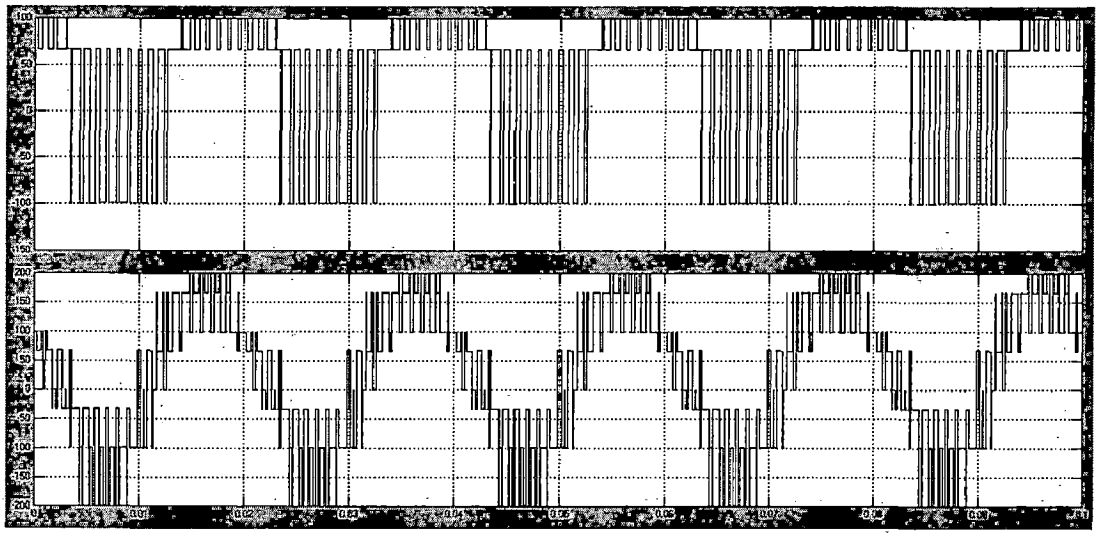

Fig.4.16 e. Phase-to-neutral voltage of Phase C and Phase-to-Phase voltage of Phase C and A

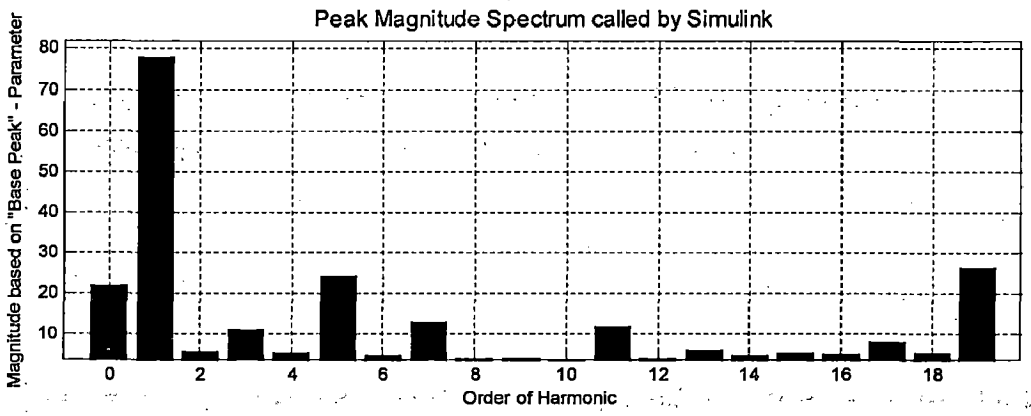

Fig.4.16 f. V_{CA} spectrum

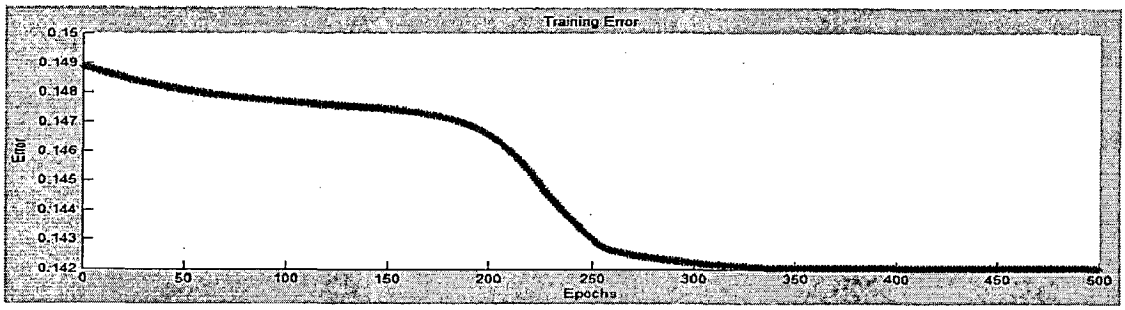

Fig.4.16 g. Anfis Training

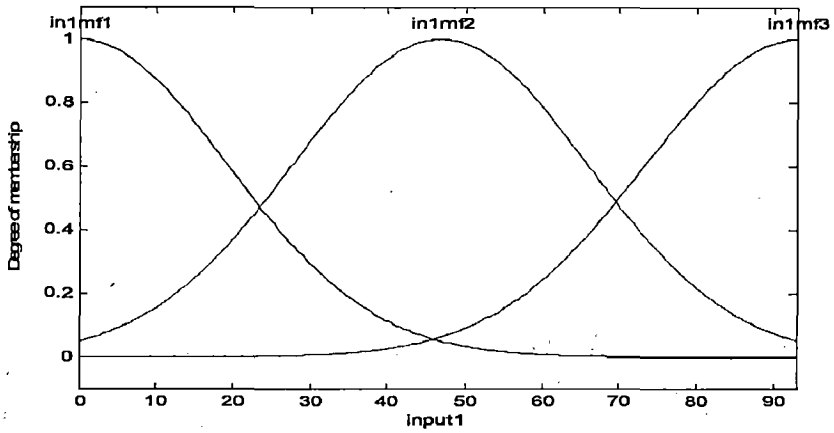

Fig.4.16 h. Input member ship function

Table 4.10 The member ship function ranges and Parameters for inputs:

Harmonic order	Range	parameters
1	0 to 92.96	[19.25 -0.07193]
2	0 to 110.2	[0 110.2]
3	0 to 20.71	[0.2906 -0.7833]
4	0 to 20.06	[2.237 -0.8114]
5	0 to 8.99	[0.3778 -0.8589]

The Effect of these faults will be in V_{BC}, V_{CA} and V_{CN}, so these output voltages will change for the fault on switch S_9. From the Fig.4.16b, Fig.4.16e it is shown that the positive values of output voltages are getting effected, because the switch S_9 is helpful for generating $+V_{dc}/2$ and $+V_{dc}/4$.

4.4.11 Fault on Switch 10

i) Open fault

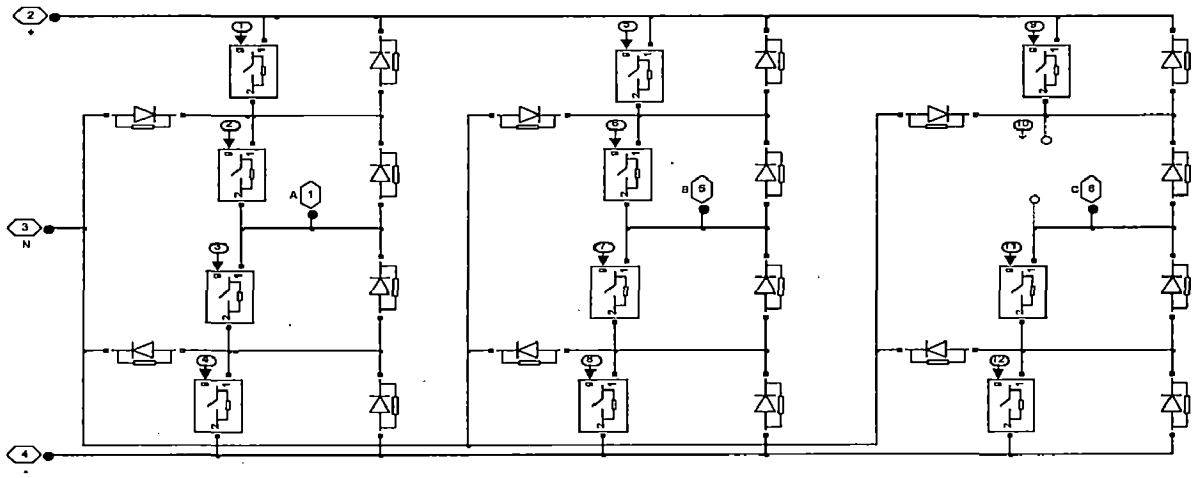

Fig.4.17 a. 3-level inverter circuit with open IGBT fault on switch 10

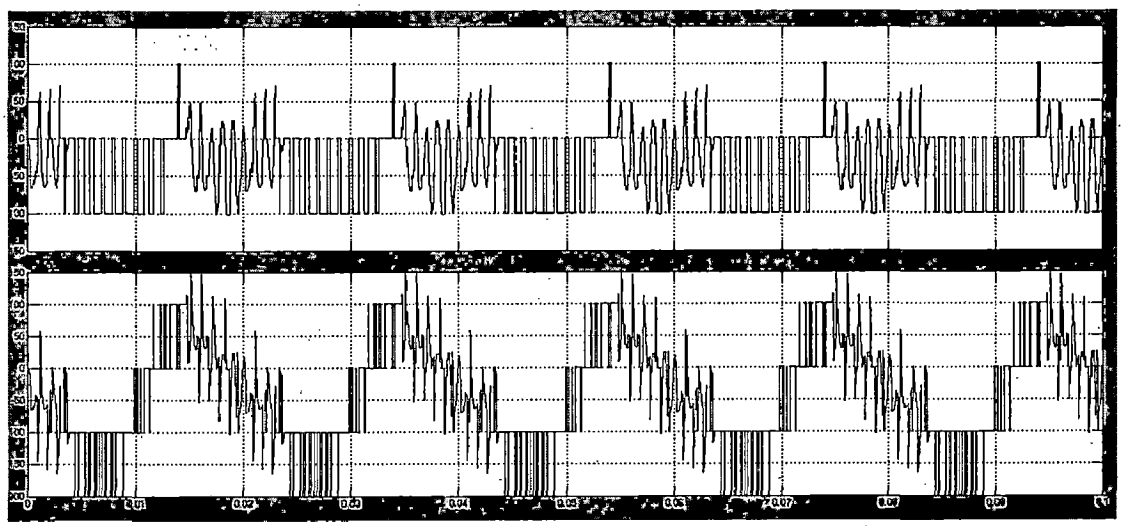

Fig.4.17 b. Phase-to-neutral voltage of Phase C and Phase-to-Phase voltage of C and A

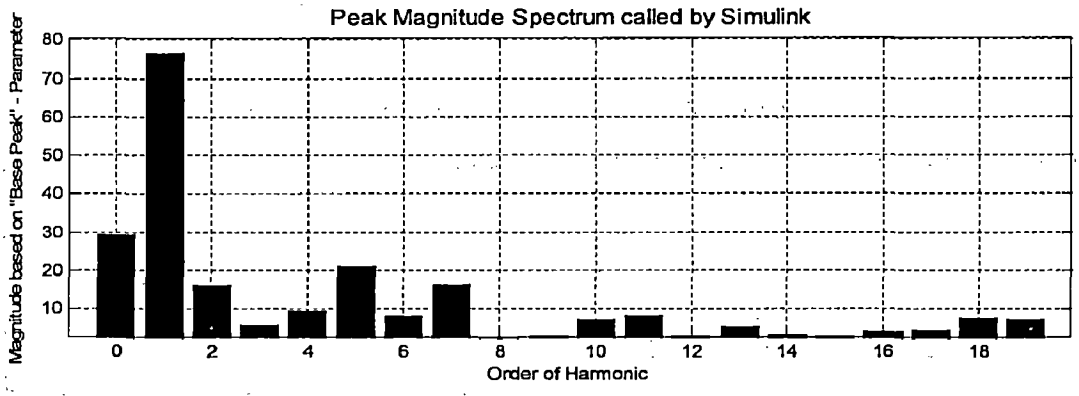

Fig.4.17 c. V_{CA} spectrum

ii) Short IGBT fault

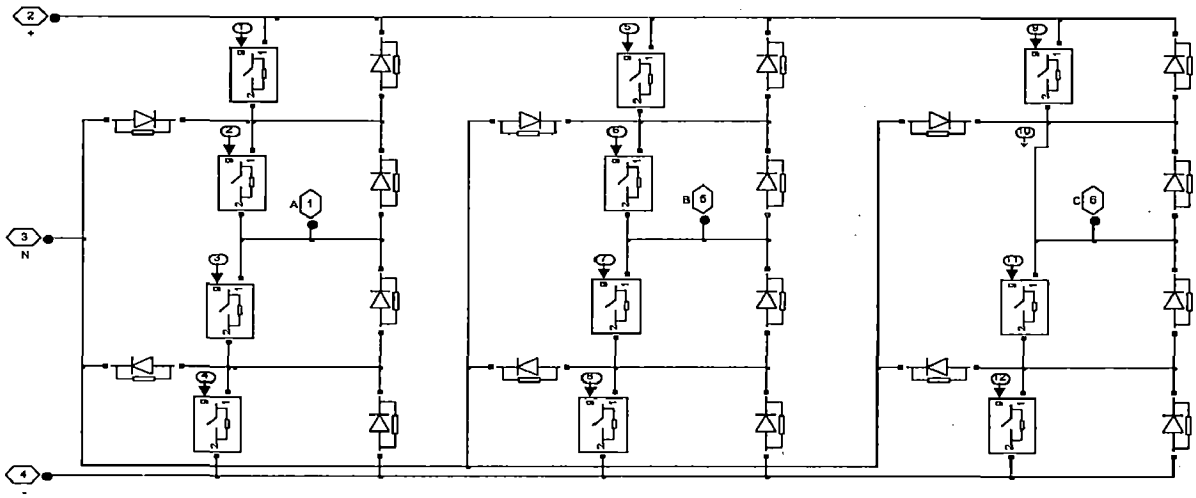

Fig.4.17 d. 3-level inverter circuit with short IGBT fault on switch 10

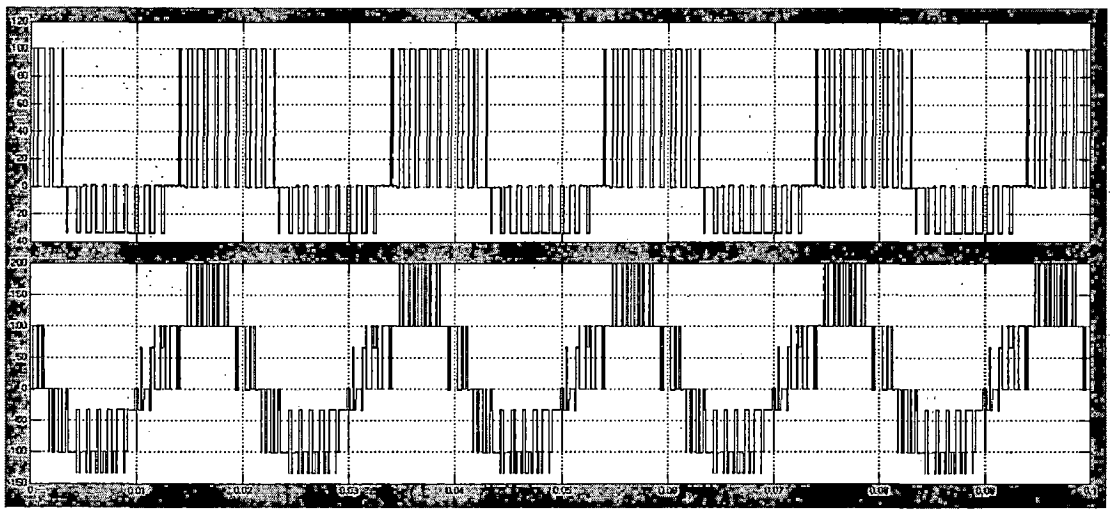

Fig.4.17 e. Phase-to-neutral voltage of Phase C and Phase-to-Phase voltage of Phase C and A

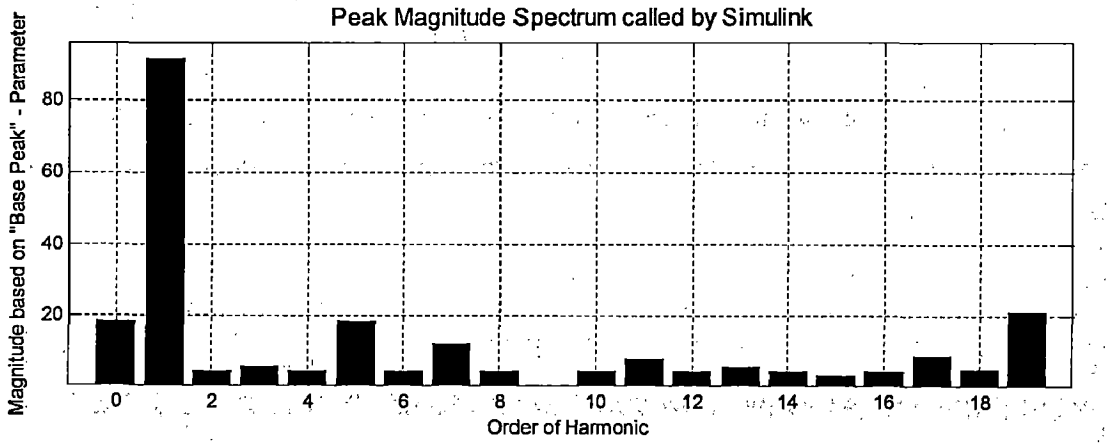

Fig.4.17 f. V_{CA} spectrum

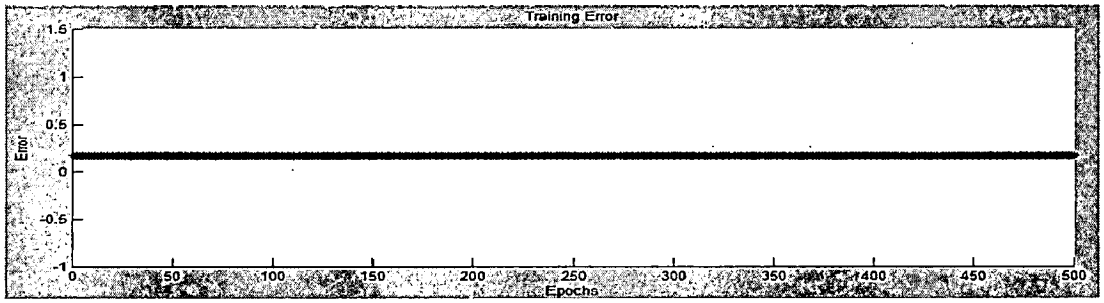

Fig.4.17 g. Anfis Training

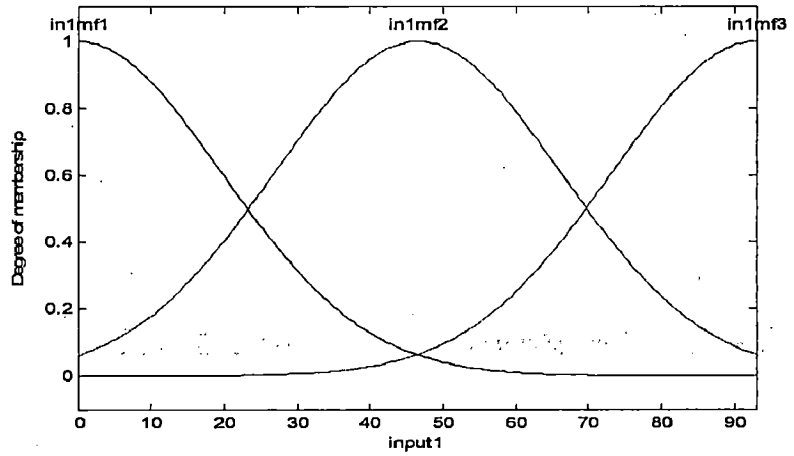

Fig.4.17 h. Input member ship function

Table 4.11 The member ship function ranges and Parameters for inputs:

Harmonic order	Range	parameters
1	0 to 92.96	[19.71 -0.009953]
2	0 to 110.2	[23.4 0.003733]
3	0 to 20.71	[4.121 -0.2672]
4	0 to 20.06	[3.274 -0.406]
5	0 to 8.99	[0.613 -1.05]

The Effect of these faults will be in V_{BC}, V_{CA} and V_{CN}, so these output voltages will change for the fault on switch S_{10}. From the Fig.4.17b, Fig.4.17e it is shown that the positive values of output voltages are getting effected, because the switch S_{10} is triggered for generating $+V_{dc}/2$ and $+V_{dc}/4$.

4.4.12 Fault on Switch 11

i) Open fault

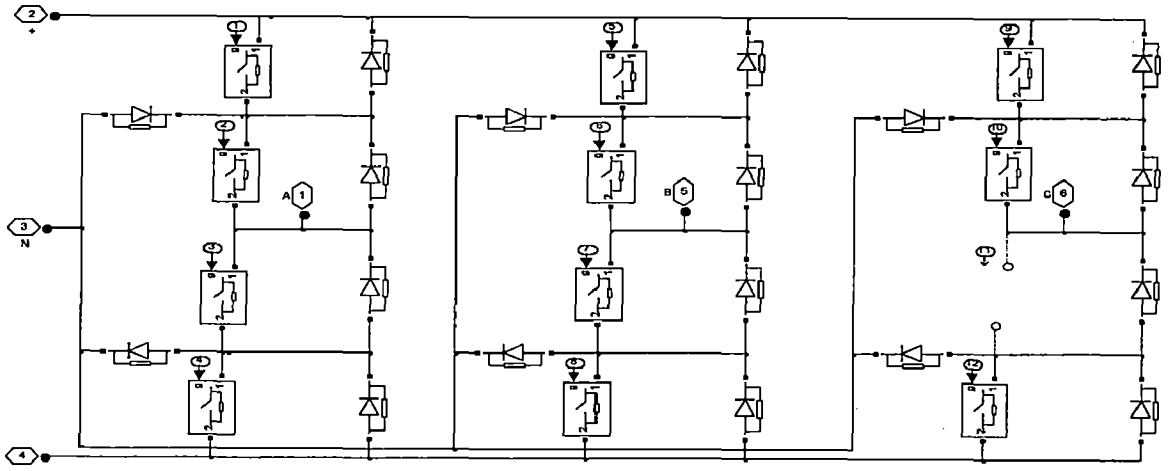

Fig.4.18 a. 3-level inverter circuit with open IGBT fault on switch 11

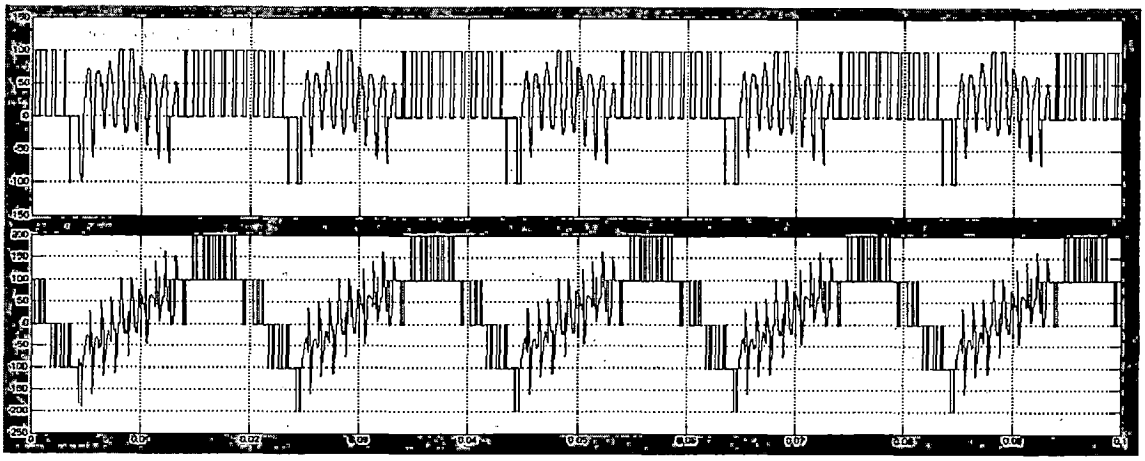

Fig.4.18 b. Phase-to-neutral voltage of Phase C and Phase-to-Phase voltage of C and A

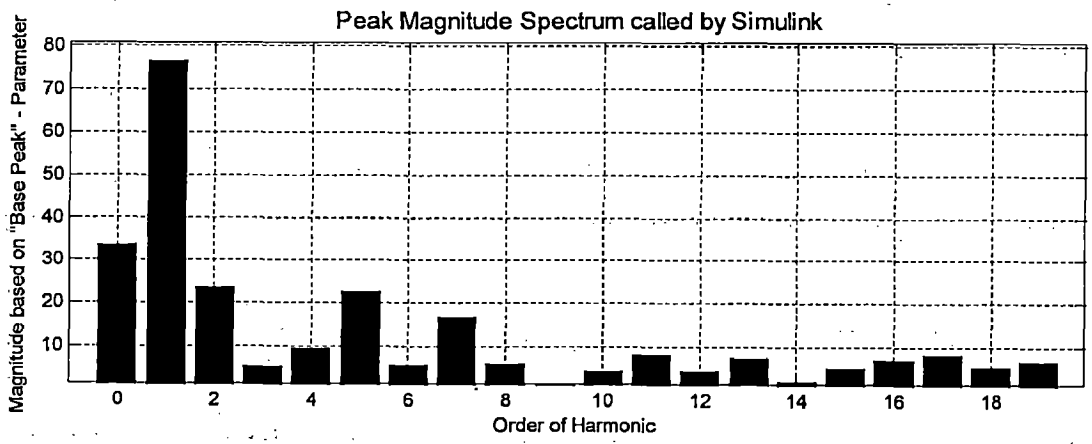

Fig.4.18 c. V_{CA} spectrum

ii) Short IGBT fault

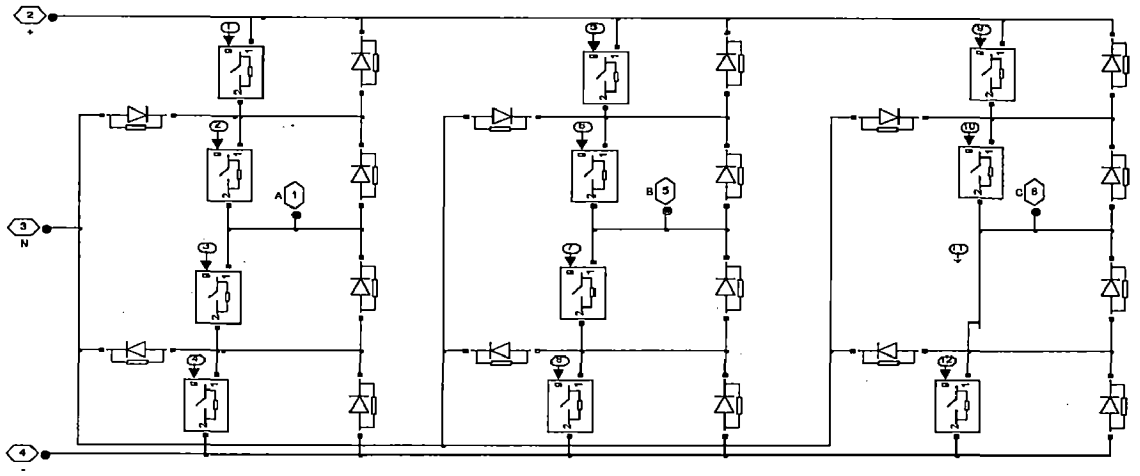

Fig.4.18 d. 3-level inverter circuit with short IGBT fault on switch 11

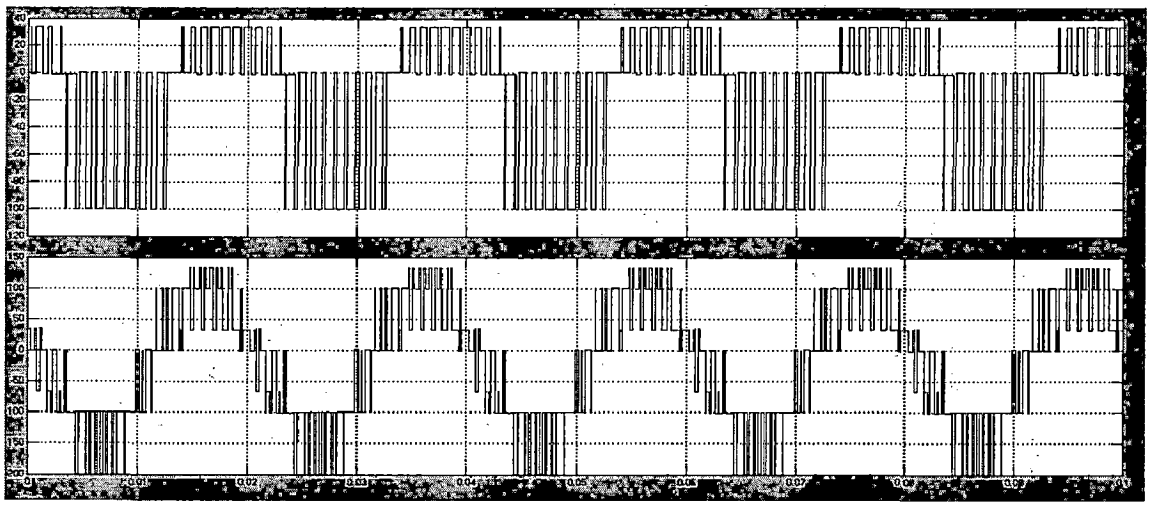

Fig.4.18 e. Phase-to-neutral voltage of Phase C and Phase-to-Phase voltage of Phase C and A

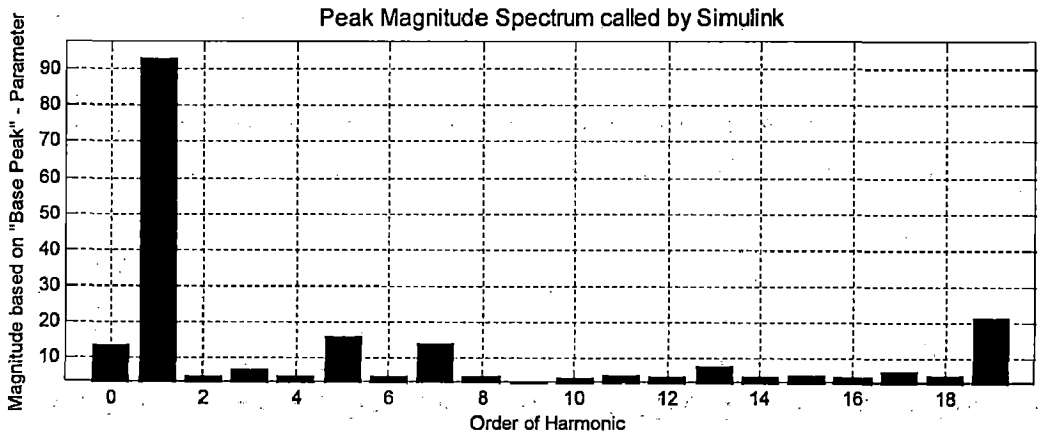

Fig.4.18 f. V_{CA} spectrum

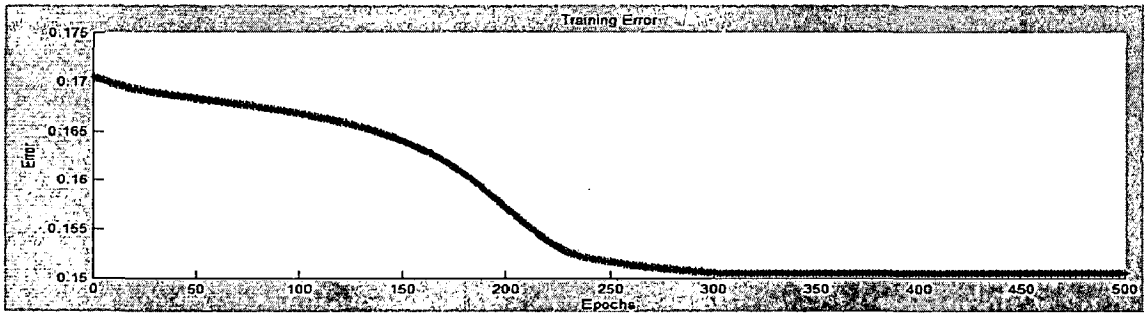

Fig.4.18 g. Anfis Training

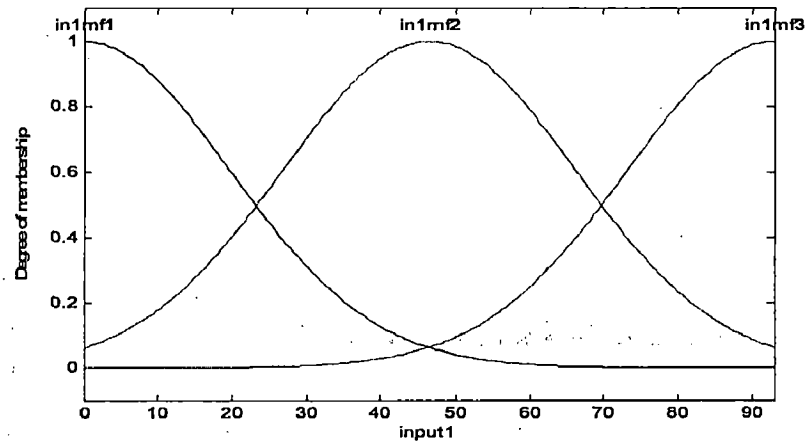

Fig.4.18 h. Input member ship function

Table 4.12 The member ship function ranges and Parameters for inputs:

Harmonic order	Range	parameters
1	0 to 92.96	[19.7 -0.0138]
2	0 to 110.2	[23.4 0.001918]
3	0 to 20.71	[4.351 -0.1077]
4	0 to 20.06	[4.475 0.4342]
5	0 to 8.99	[0.6164 -1.094]

The Effect of these faults will be in V_{BC}, V_{CA} and V_{CN}, so these output voltages will change for the fault on switch S_{11}. The Switch S_{11} is triggered for generating the $-V_{dc}/2$ and $-V_{dc}/4$ levels. So these output voltages are getting affected which is obvious from the Fig.4.18b and Fig.4.18e.

4.4.13 Fault on Switch 12

i) Open fault

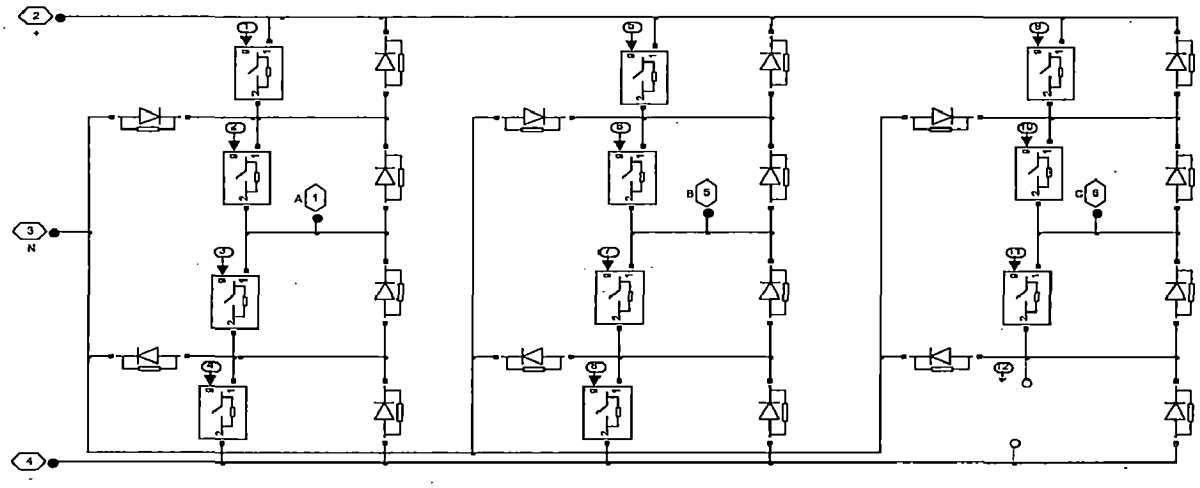

Fig.4.19 a. 3-level inverter circuit with open IGBT fault on switch 12

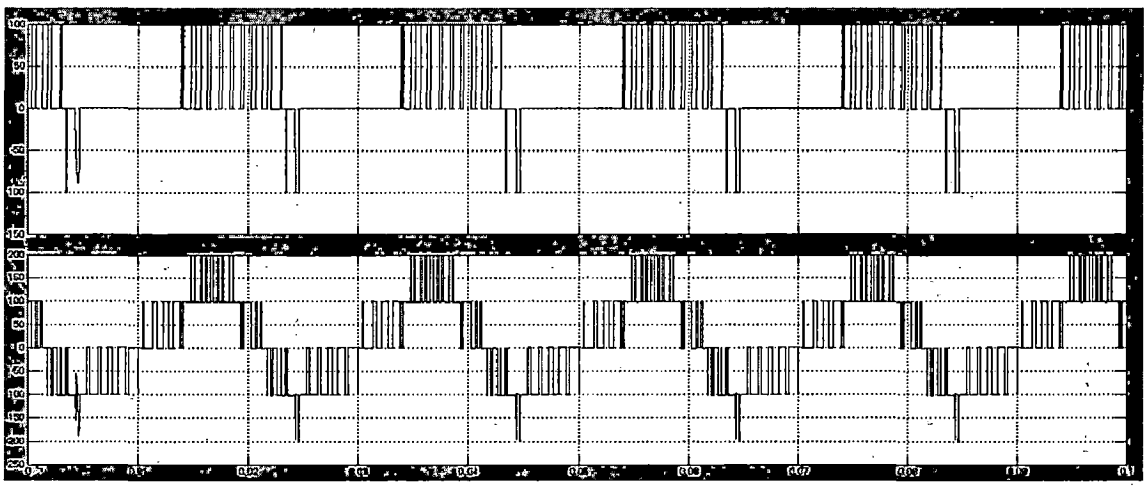

Fig.4.19 b. Phase-to-neutral voltage of Phase C and Phase-to-Phase voltage of C and A

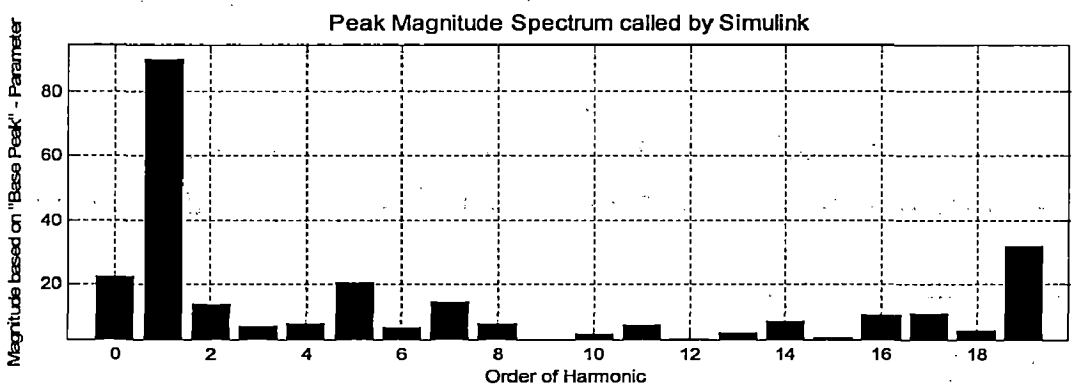

Fig.4.19 c. V_{CA} spectrum

ii) Short IGBT fault

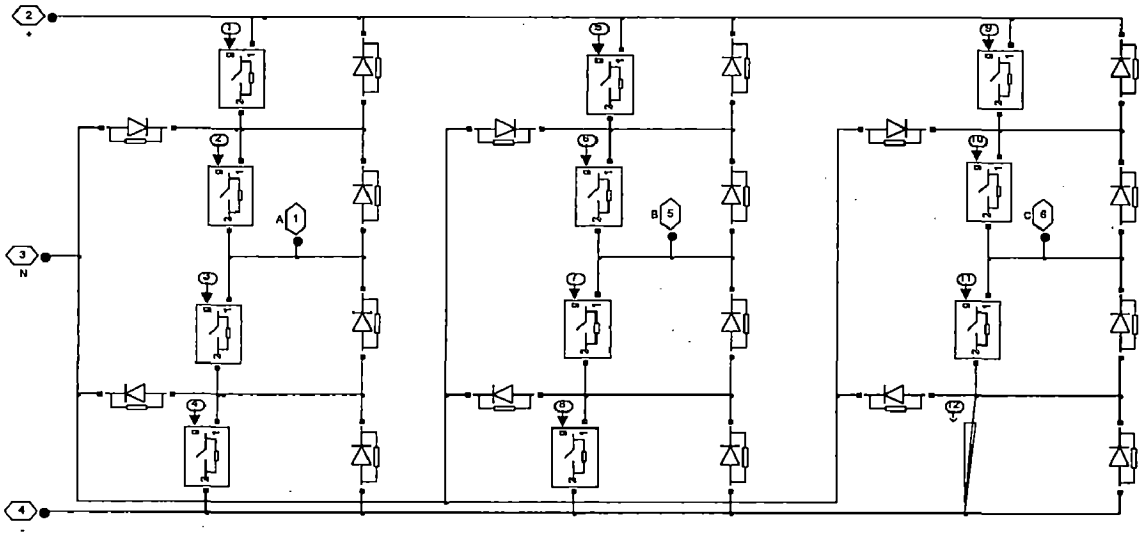

Fig.4.19 d. 3-level inverter circuit with short IGBT fault on switch 12

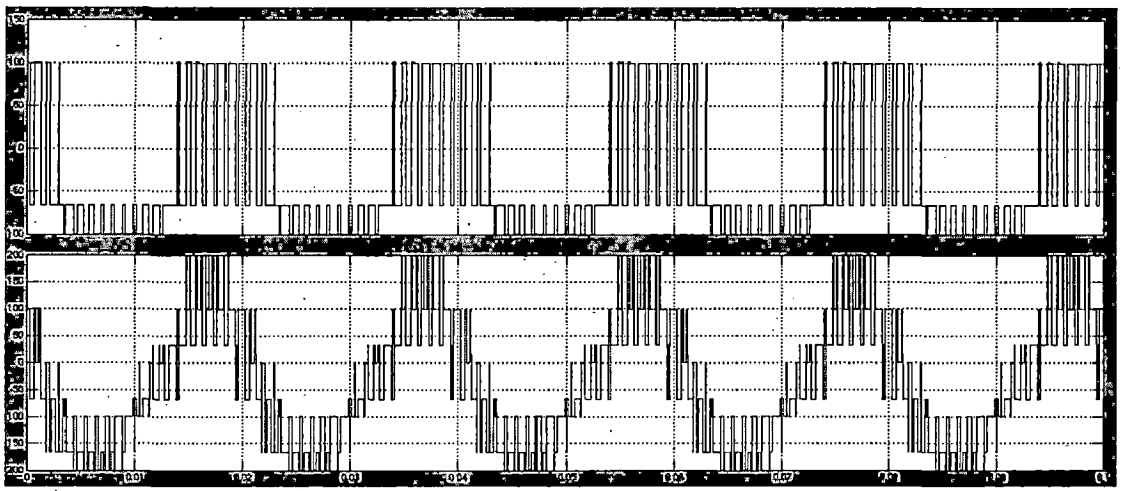

Fig.4.19 e. Phase-to-neutral voltage of Phase C and Phase-to-Phase voltage of Phase C and A

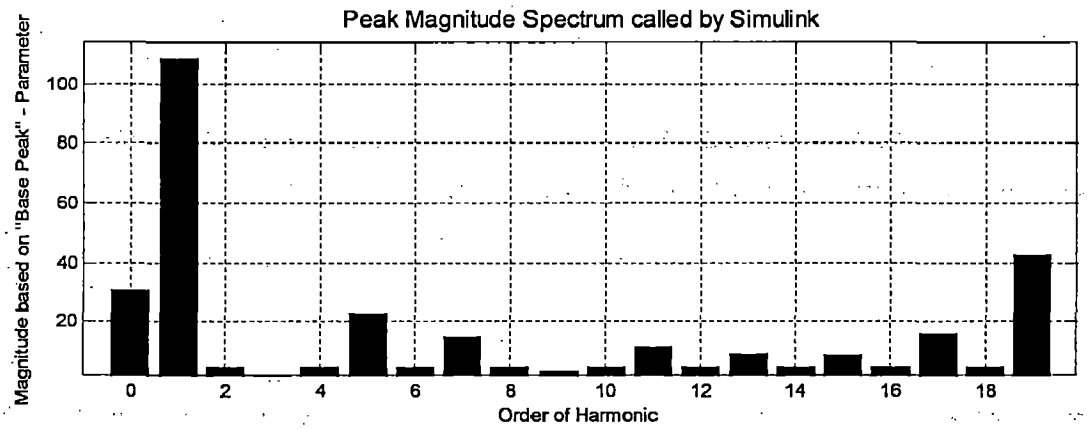

Fig.4.19 f. V_{CA} spectrum

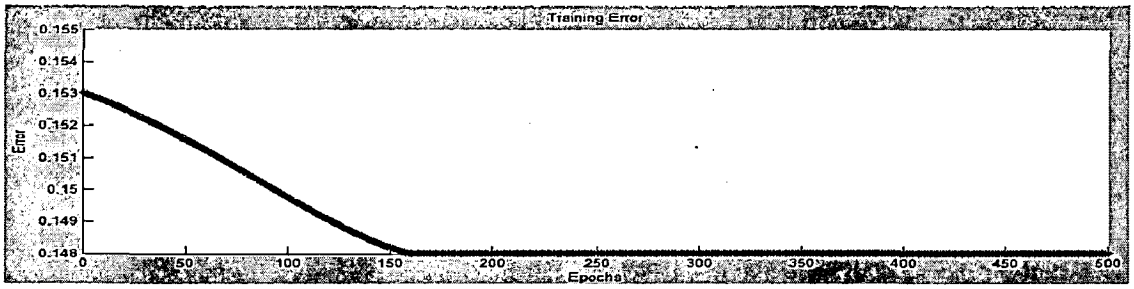

Fig.4.19 g. Anfis Training

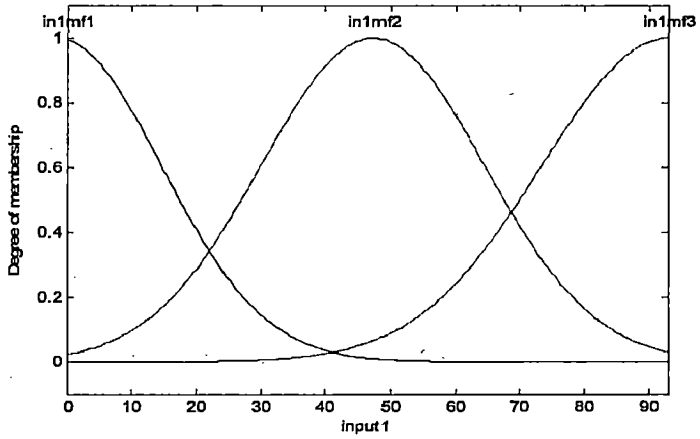

Fig.4.19 h. Input member ship function

Table 4.13 The member ship function ranges and Parameters for inputs:

Harmonic order	Range	parameters
1	0 to 92.96	[16.08 -1.429]
2	0 to 110.2	[23.38 -0.006731]
3	0 to 20.71	[0.9249 -2.588]
4	0 to 20.06	[4.401 -0.06488]
5	0 to 8.99	[0.3958 -1.102]

The Effect of these faults will be in V_{BC}, V_{CA} and V_{CN}, so these output voltages will change for the fault on switch S_{12}. The Switch S_{12} is triggered for generating the $-V_{dc}/2$ and $-V_{dc}/4$ levels. So these output voltages in corresponding phases are getting affected which is obvious from the Fig.4.19b and Fig.4.19e.

CHAPTER -5

RECONFIGURATION TECHNIQUES

In recent years the applications of powerelectronic devices are getting increased, in the same way the rate of faults occuring in industry fields also icreasing and these faults especially may influence the system operation. Mainly the Asynchronous machines are fed by voltage inverters in most of industrial applications. This type of AC drive system is sensitive to different kinds of faults occurring at the front end rectifier, or at the power inverter or at the control subsystem. Whenever fault occurs, the system operation has to be stopped for a non-programmed maintenance schedule. Because the Switching device failure is one of the important reasons for circuit dysfunction. The cost of the stops can be high and justifies the development of a fault tolerant supply system. Therefore inorder to preclude these harmful influence as well as to enhance the reliability of the system, the fault detection and diagnosis are compulsory [12]-[28].

It is apparent that whenever short IGBT failure occurs the source or clamp capacitor will discharge through a conducted pole switch if there is no protective action for such faults. Inorder to avoid series damages and system commapse due to current surges the conducted switch must be turned off quickly and properly. In case of open type IGBT faults the main switching device fail open, some switching states and the corresponding desired voltage levels would be lost. When clamping switching devices fail open, the clamping ability and some switching states would be lost. From the above analysis, one knows that device's failure impacts the circuit operation fatally. To keep the converter working at switching device fails, it is effective to have the circuit be redundant [21].

With the help of those characteristics, multilevel inverter topologies have been widely studied by many researchers. They are classified into Diode Clamped Multilevel Inverters (DCMIs), Clamping Capacitor Multilevel Inverters (CCMIs), and Isolates H-bridge Multilevel Inverters (IHMIs). Among them, the 3-level diode clamped inverter has been regarded as the most popular inverter. It is also known as the neutral-point

clamped (NPC) inverter and does not have clamping capacitors and isolation transformers, resulting in the possibility of hardware simplification. Due to these advantages, it has been widely used in high power industrial applications, such as voltage source converter based HVDC transmissions, static VAR compensators, high-power adjustable-frequency motor drives and so on [19].

Here we have presented two reconfiguration techniques for NPC inverter to correct open and short type of IGBT faults in inverters. As this inverter configuration does not need the additional transformer for isolation of power and extra capacitance except the dc-link capacitance. In this reason the NPC inverter has used more than before. The specific application among widely industrial utilities, the NPC inverter is needed to operate continuously. Thus, it's necessary to develop a fault tolerant in NPC inverter for improvement of reliability [31].

Whenever one switching device gets faulted at one leg in the NPC inverter, it increase the voltage stress of the other switching device as result of the unbalancing voltage between upper and lower dc-link capacitor structurally. If it hasn't protection circuit, this unbalance voltage cause to breakdown from one switching device to the others sequentially. Until now, the development of the PWM strategies has been treated as the main research area in order to solve the inherent problems, such as dc link unbalancing and output harmonics. Also, parallel redundancy is often employed for continuous operation under fault condition, although at a high system cost [20]-[22].

Here 2-different reconfiguration techniques are presented to diagnose the faults in the inverter. They are

i) Using addition of 1-extra leg

ii) Using addition of 3-extra legs

The advantage using addition of 3-extra legs is that, this reconfiguration technique can be applied if faults occur in two or more switch faults in any leg.

5.1 Reconfiguration using addition of 1-extra leg

In this technique we will place an additional leg in parallel with DC-Supply which is connected to pre-installed NPC inverter. Whenever fault occurs this extra added leg will serve the purpose by isolating the faulted leg. This configuration is useful for open and short IGBT faults in inverter. But it is limited to single IGBT faults. As the presented method of fault detection is able to detect the fault with in one sample period of time so the effect faulted IGBT will not be there on other IGBTs which are in inverter. And one more advantage is this configuration is applicable to both open and short IGBT faults of inverter. One of the main advantages of this circuit is this reconfiguration technique can be applied to preinstalled inverter without opening it. The additional leg configuration is shown in Fig.5.1.

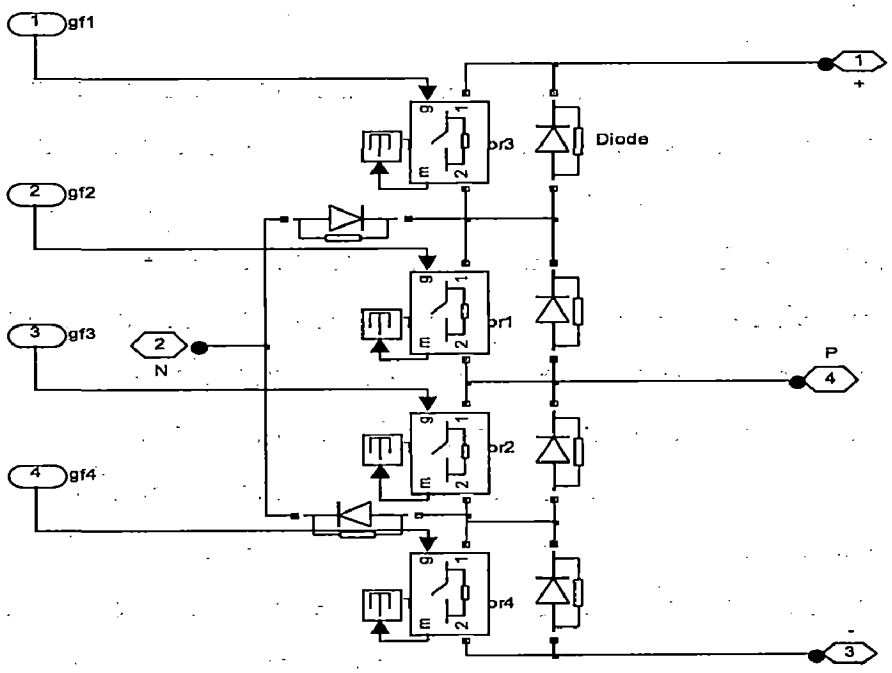

Fig.5.1 Additional leg for reconfiguration

If the fault occurs on switch S_1 the fault detection system is going detect the fault location. The isolation of the faulted leg can be done by giving '0' pulses to the switches corresponding to faulted leg. This can be done with the help of a logical circuit shown in Fig.5.2.

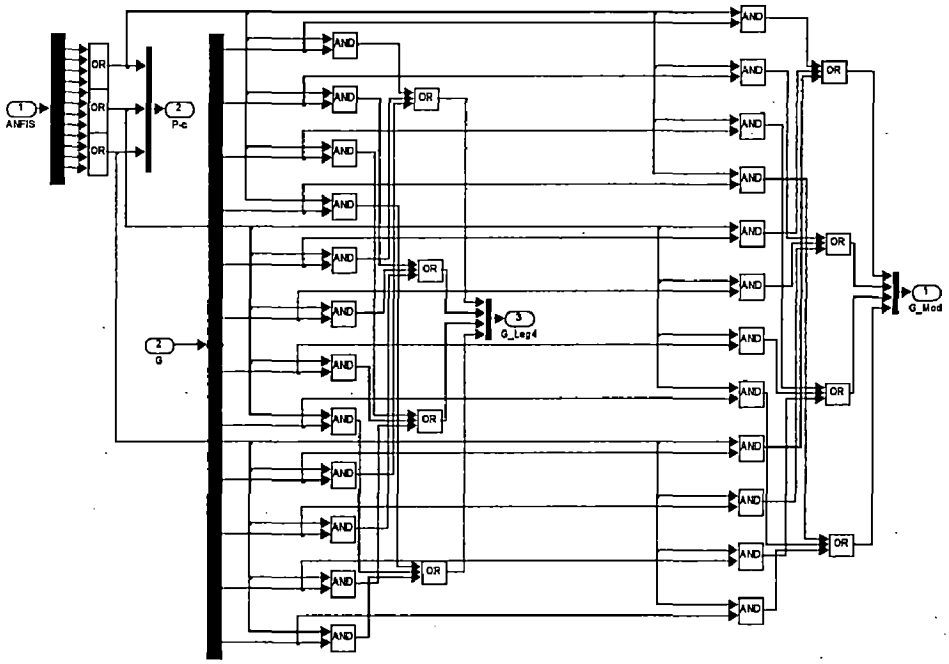

Fig.5.2 Logical circuit for Gate pulse modification

Because of that the faulted IGBTS acts like open circuits irrespective of the control circuit. As we are taking the measurement at faulted legs, the measurement system is going to show the output corresponding to open circuit faults of 4 IGBTS, because of that the outputs of fault detection system also differ. In order to avoid this situation we should have logical mechanism that keeps the outputs as 1 until the switch is replaced. The corresponding logical system is shown in Fig.5.3.

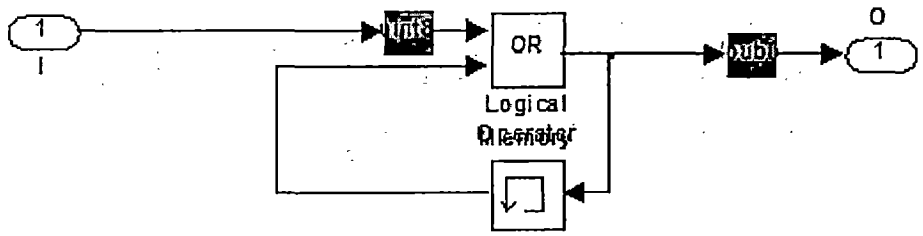

Fig.5.3 Logical systems.

Ones the Fault detection system detects the fault in inverter the reconfiguration scheme is going to correct the fault by adding an extra leg, but the load always

connected to faulted leg only. So we need to interchange the extra added leg with faulted leg in order to supply corrected output to load. To make this we use 2-way switch configuration as shown in Fig.5.4.

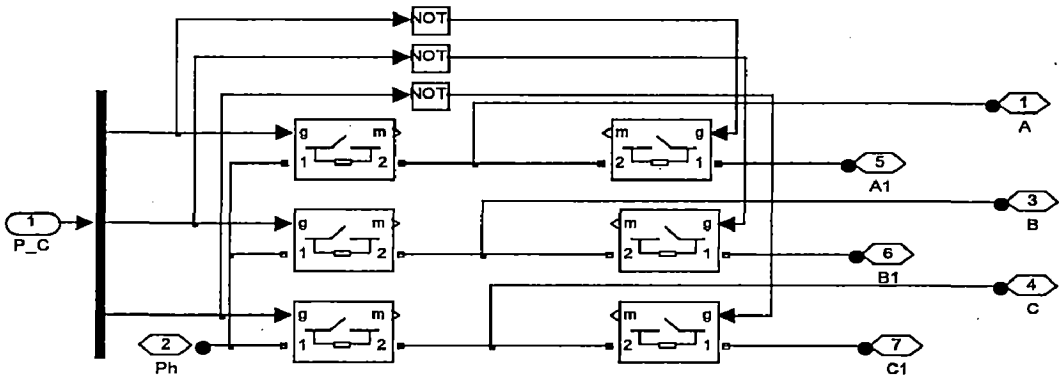

Fig.5.4 Phase connection isolation circuit

5.1.1 Fault diagnosis using Fuzzy Inference System

Fault detection system using Adaptive Neuro Fuzzy Inference System is shown in Fig.5.5 which uses phase-to-Neutral voltages of the inverter at faulted leg

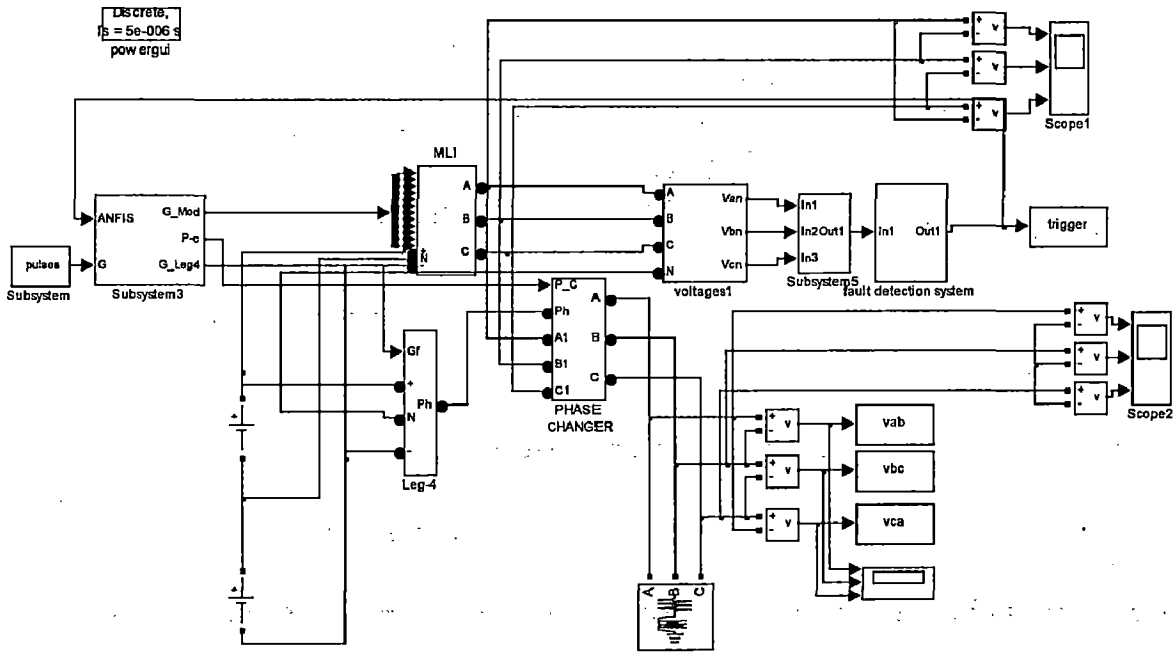

Fig.5.5 Fault diagnosis and reconfiguration system using Fuzzy Inference System

5.1.2 Fault diagnosis using ANFIS

Fault detection system using Adaptive Neuro Fuzzy Inference System is shown in Fig.5.5 which uses phase-to-phase voltages of the inverter at faulted leg

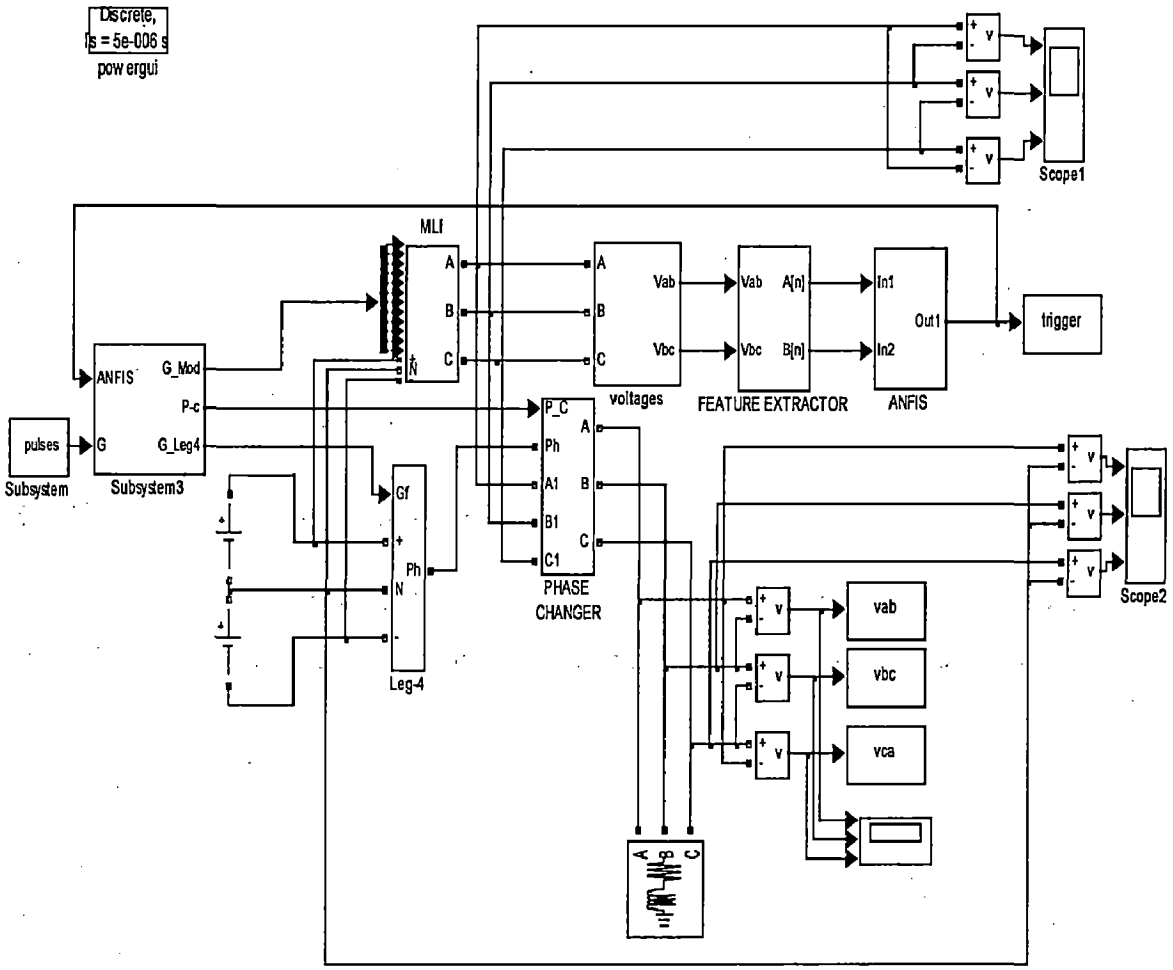

Fig.5.6 Fault diagnosis and reconfiguration system using ANFIS

5.2 Reconfiguration using addition of 3-extra legs

This reconfiguration method is same as reconfiguration using addition of 1-extra leg but it uses three legs to replace the faulted legs. This reconfiguration method has the advantage that it can operate even if the fault occurs in two or more switches of the inverter.

5.2.1 Fault diagnosis using Fuzzy Inference System

Fault detection system using Fuzzy Inference System is shown in Fig.5.7 which uses phase-to-Neutral voltages of the inverter at faulted leg

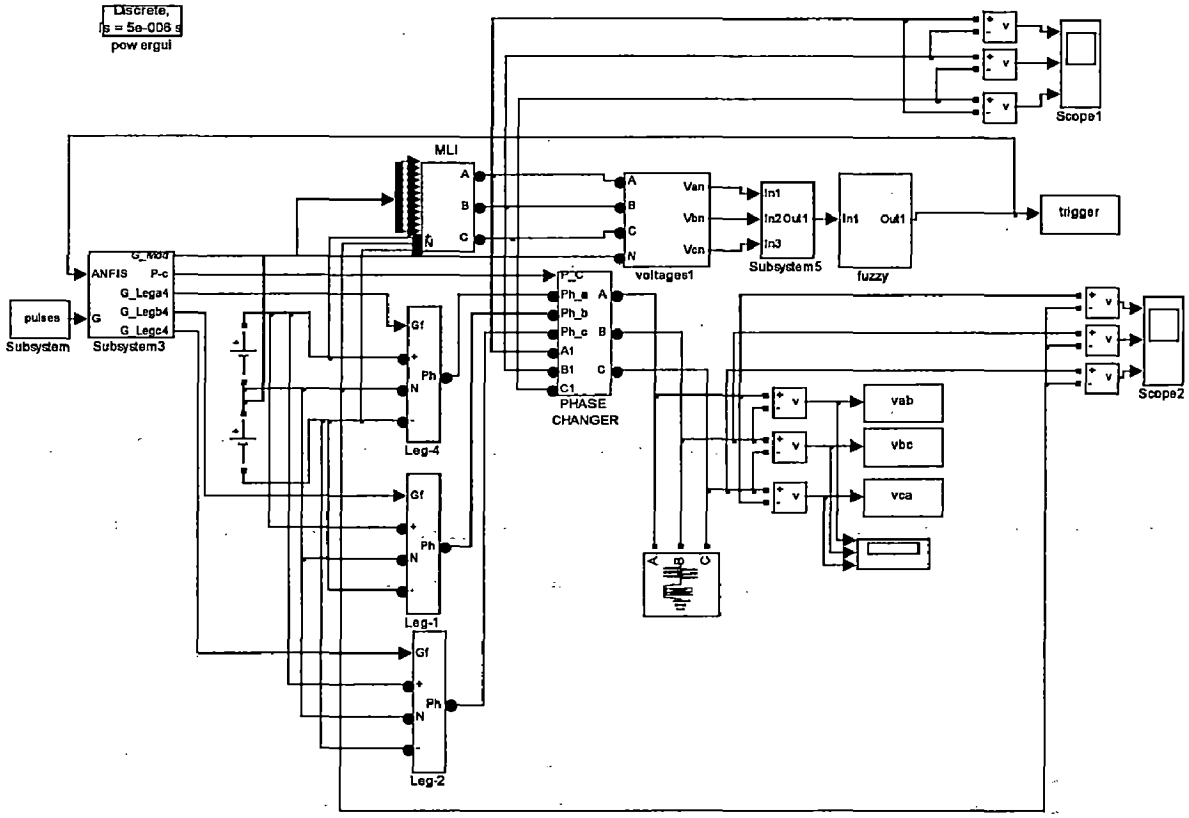

Fig.5.7 Fault diagnosis and reconfiguration system using Fuzzy Inference System

Phase connection isolator circuit used in this circuit shown in Fig.5.8

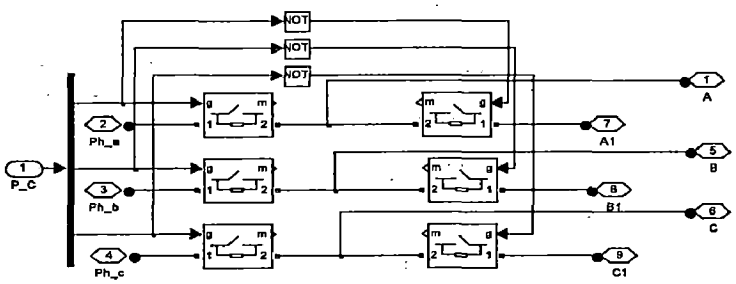

Fig.5.8 Phase connection isolation circuit

The three phases of the three extra added legs are connected to ph_a, ph_b, ph_c and the three phases of the inverter are connected to the A1, B1, C1. If the fault occurs in the 1st leg of the inverter outputs of the P_C will be [1 0 0]. Due to that A1 will be isolated and ph_a will be connected to the load. As this leg is operating healthy the output to the load will be a 3-level stair case form.

5.2.2 Fault diagnosis using ANFIS

Fault detection system using Adaptive Neuro Fuzzy Inference System is shown in Fig.5.9 which uses phase-to-phase voltages of the inverter at faulted leg

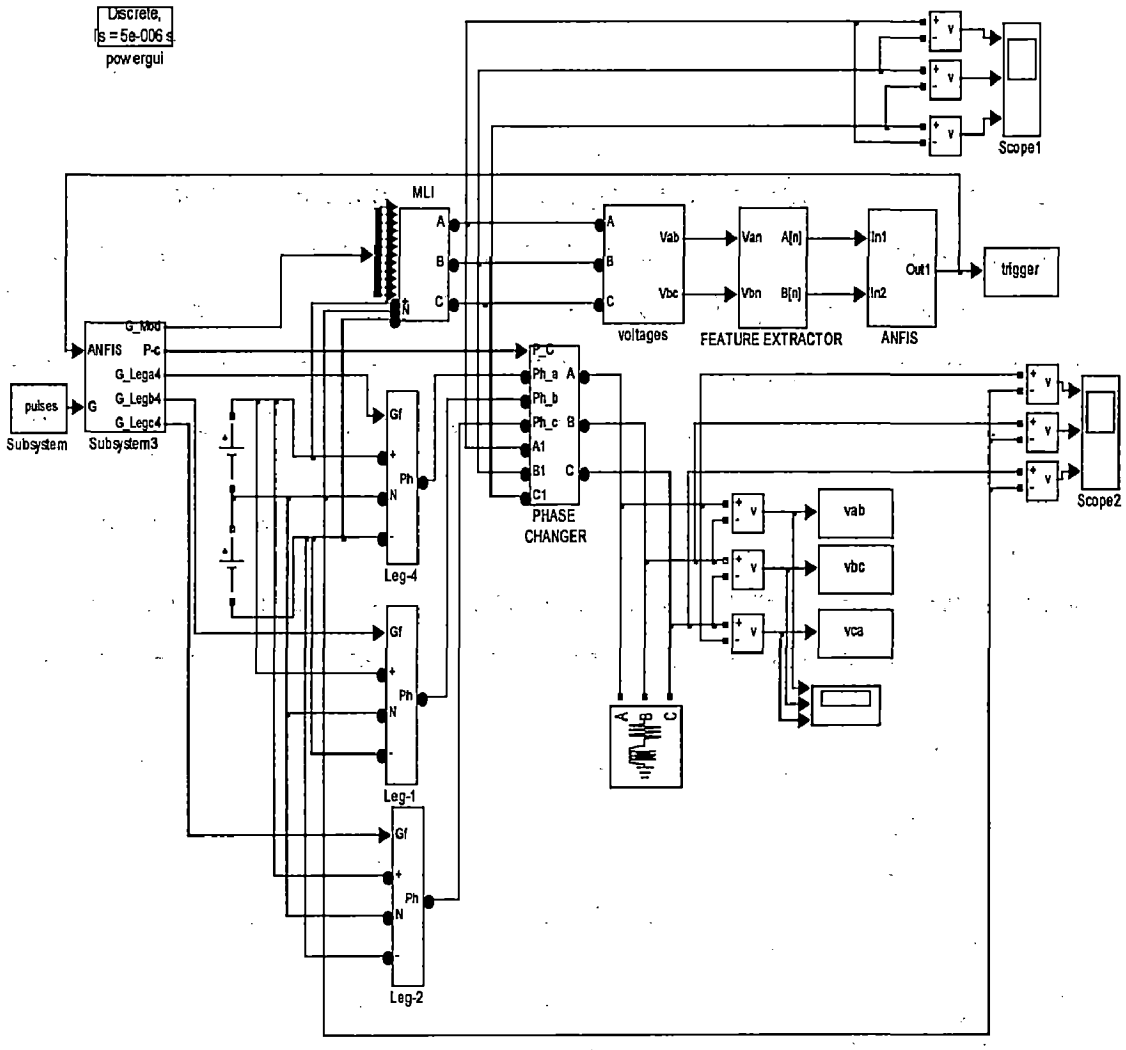

Fig.5.9 Fault diagnosis and reconfiguration system using ANFIS

5.3 Wave Forms Corresponding To Reconfiguration Using an Additional Leg(s)

Here the output wave forms shown in the following figures can be obtained from the any of the reconfiguration techniques which are proposed earlier. Here for illustrative purpose the results corresponding to fault on switch (IGBT) 1 are only shown

5.3.1 Open IGBT fault of switch-1:

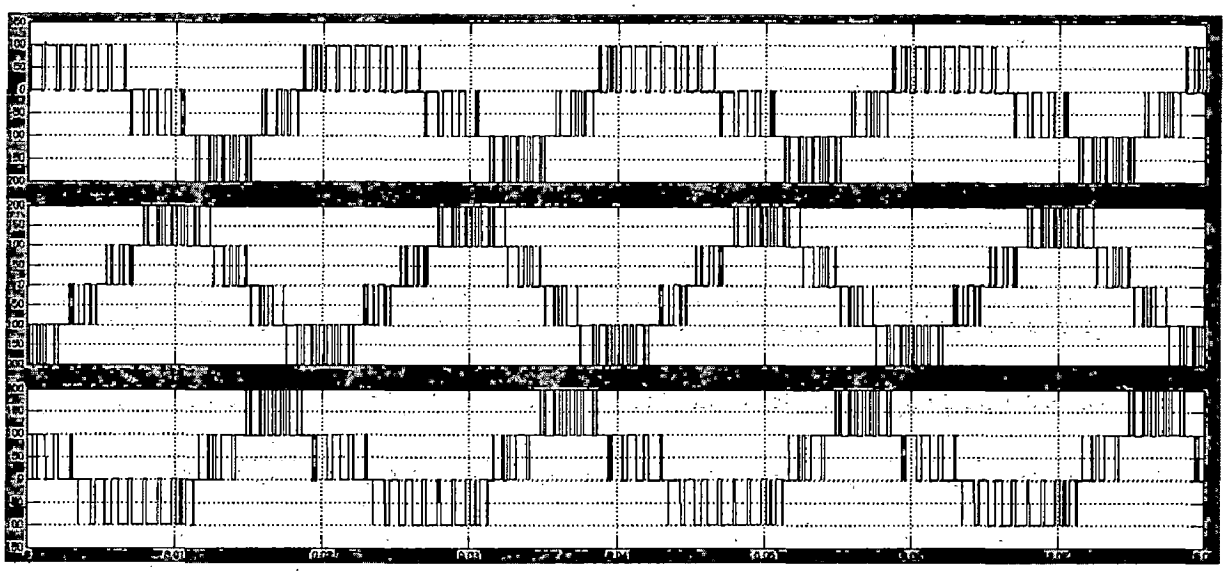

Fig 5.10 Phase-to-Phase voltage wave form without fault diagnosis system i)V_{AB} ii)V_{BC} iii)V_{CA}

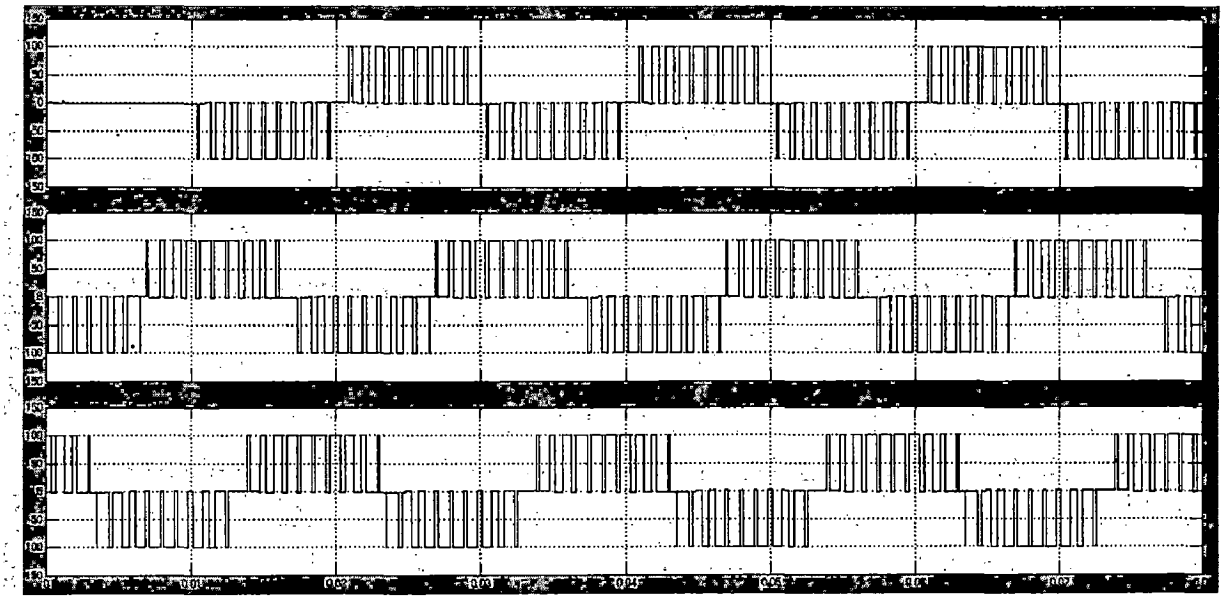

Fig.5.11 Phase-to-neutral voltage wave form without fault diagnosis system i)V_{An} ii)V_{Bn} iii)V_{Cn}

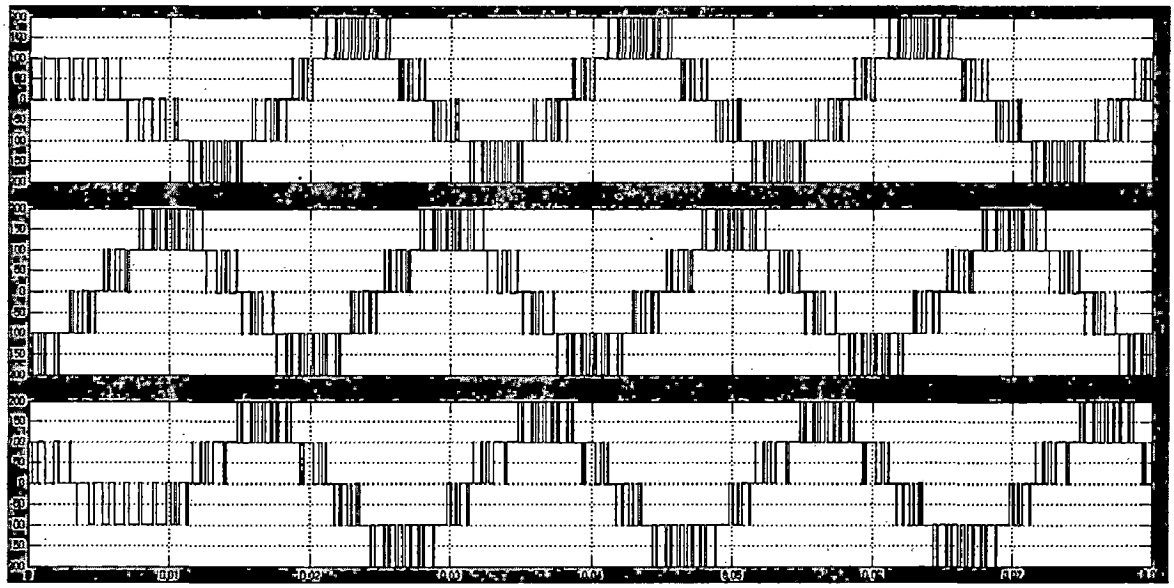

Fig.5.12 Phase-toPhase voltage wave form with fault diagnostic system i)V_{AB} ii)V_{BC} iii)V_{CA}

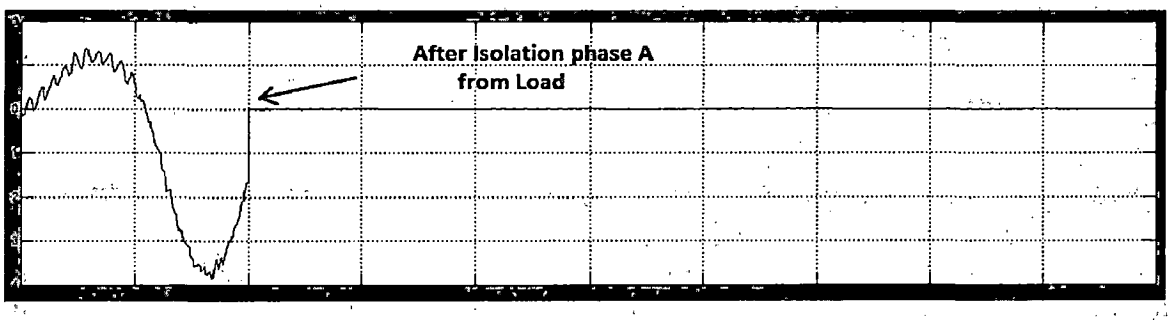

Fig.5.13 Faulted Phase currents without fault diagnostic system

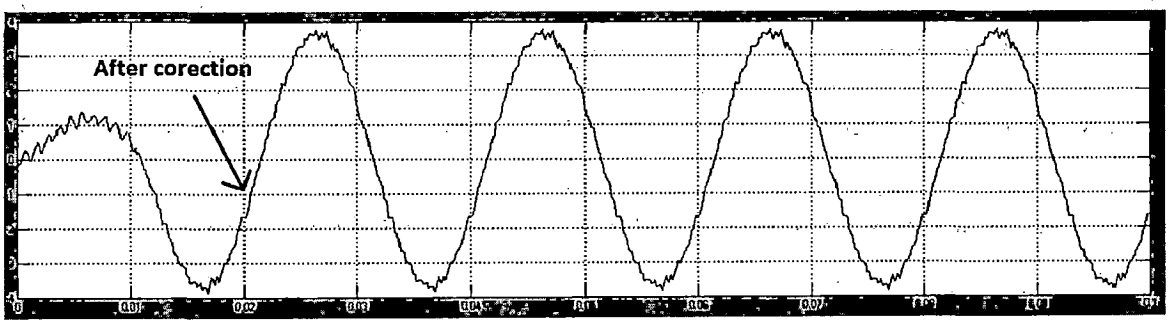

Fig.5.14 Phase currents after incorporating the fault diagnostic system

From the Fig.5.13 the output after correction is 0. It is because the faulted phase is isolated.

5.3.2 Short IGBT Fault of Switch-1

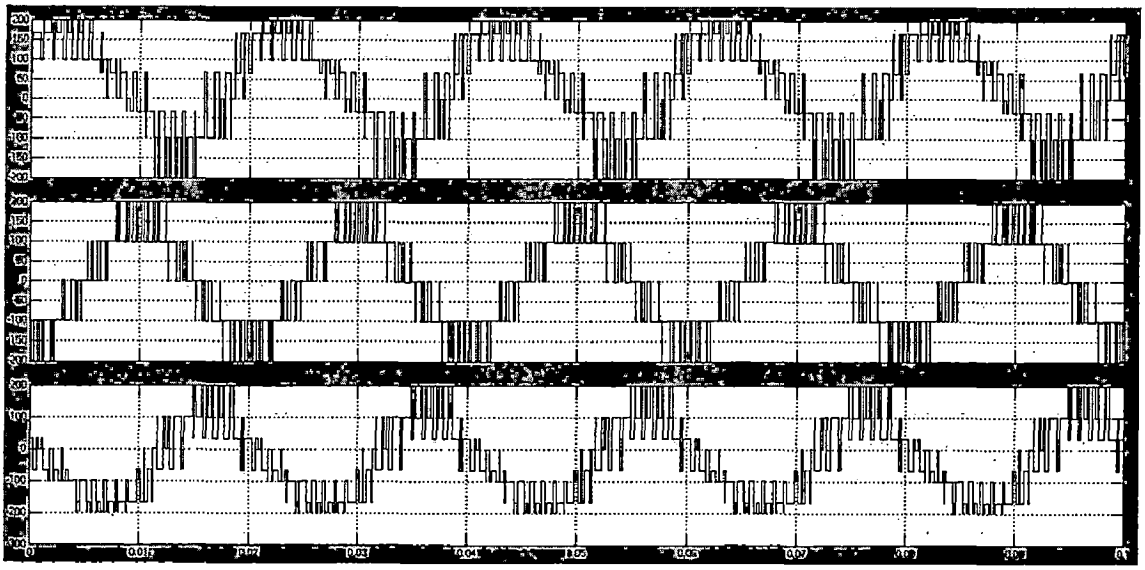

Fig.5.15 Phase-toPhase voltage of faulted wave form i)V_{AB} ii)V_{BC} iii)V_{CA}

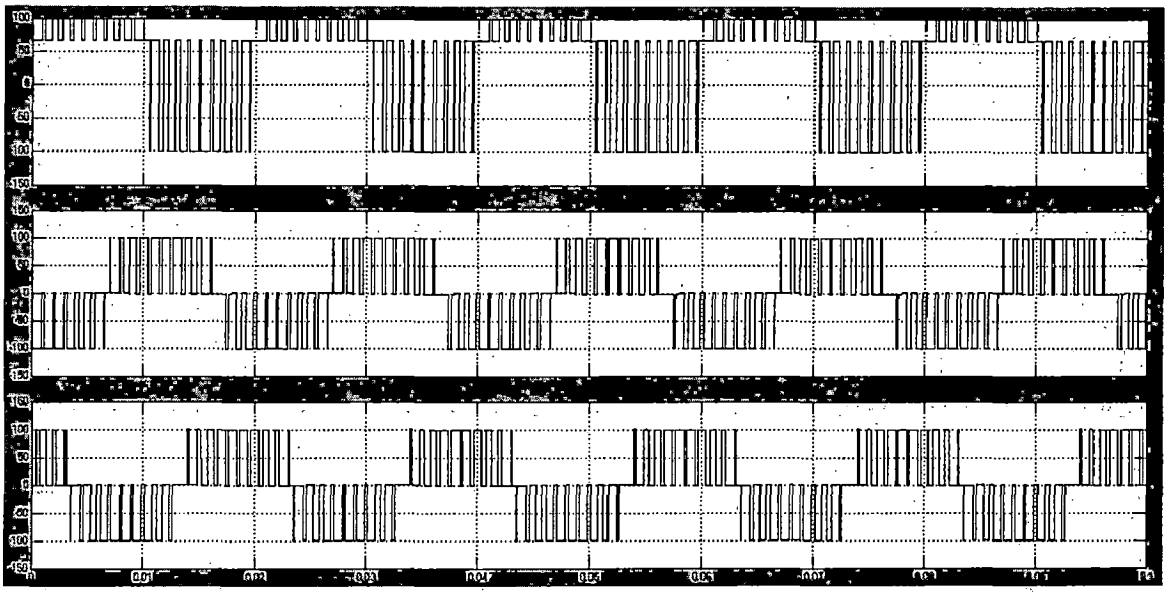

Fig.5.16 Phase-to- neutral voltage waveforms of after the occurrence of fault i)V_{An} ii)V_{Bn} iii)V_{Cn}

As can be seen from the wave form corresponding to sitch S_1 fault, the output voltage of the V_{AN}, V_{AB}, V_{CA} are getting affected. Hance the fault in the inverter can be detected with the help of these voltages only.

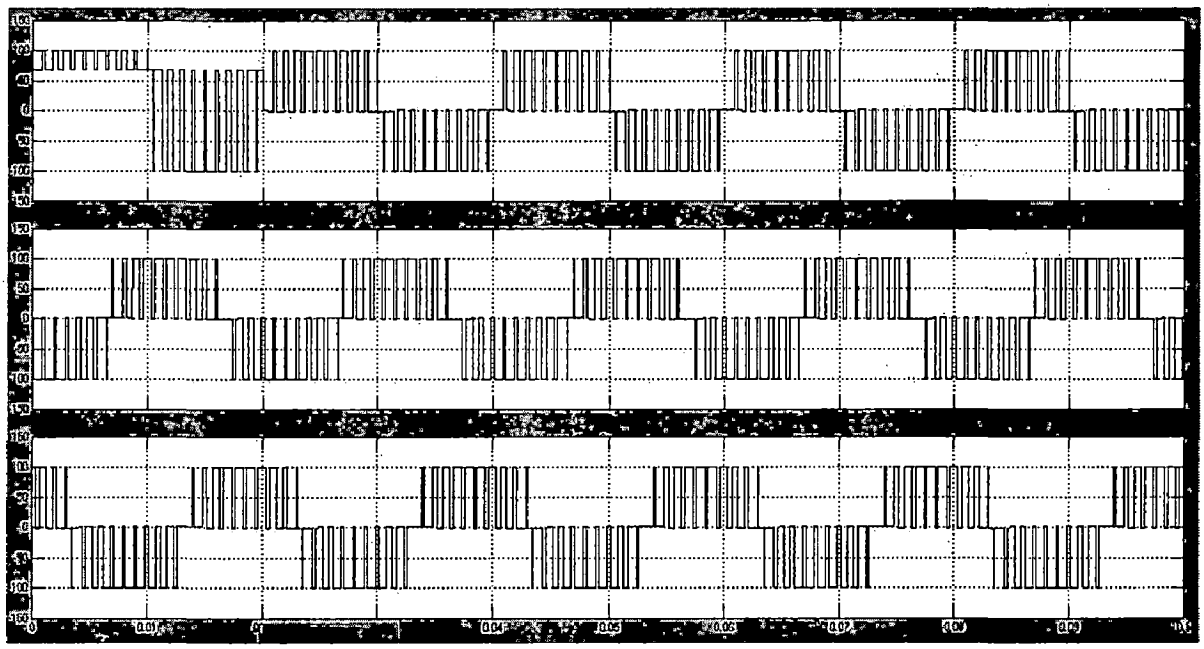

Fig.5.17 Phase-to- neutral voltage of after incorporating the reconfiguration technique

i)V_{An} ii)V_{Bn} iii)V_{Cn}

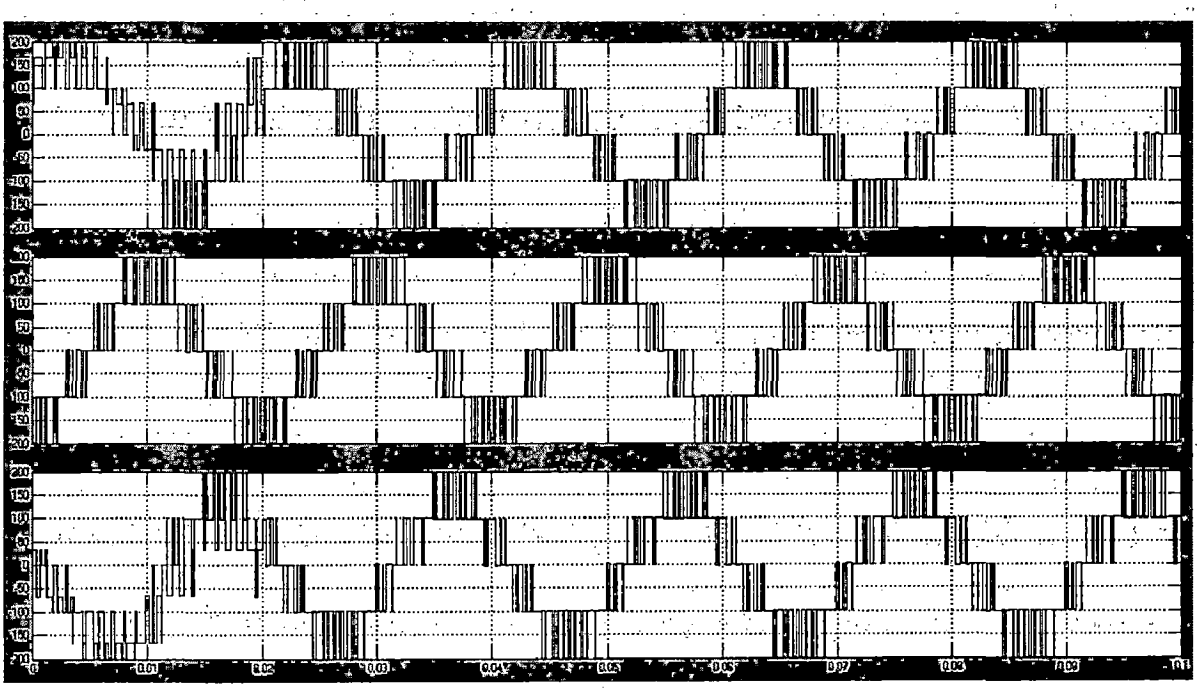

Fig.5.18 Phase-to-Phase voltage after incorporating the reconfiguration technique

i)V_{AB} ii)V_{BC} iii)V_{CA}

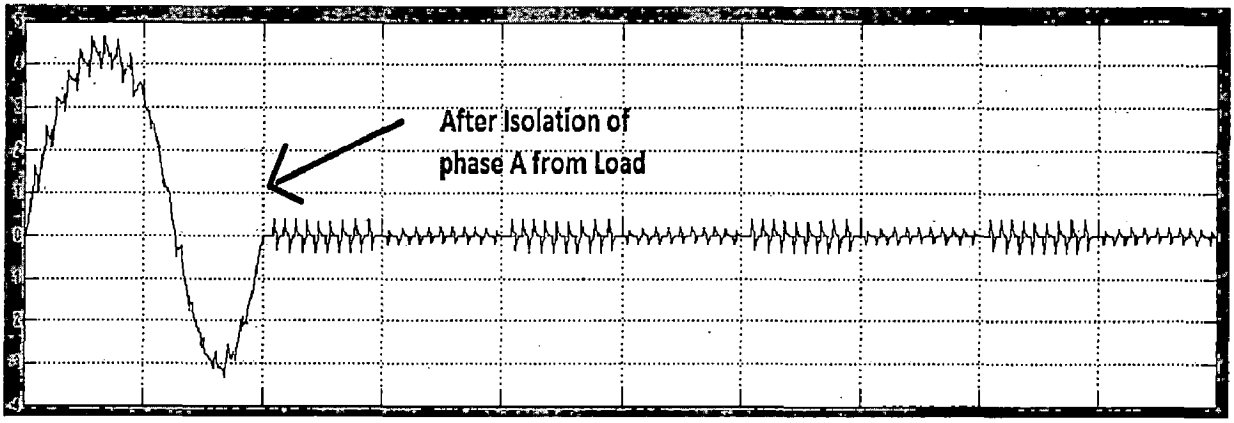

Fig.5.19 Faulted Phase currents without fault diagnostic system

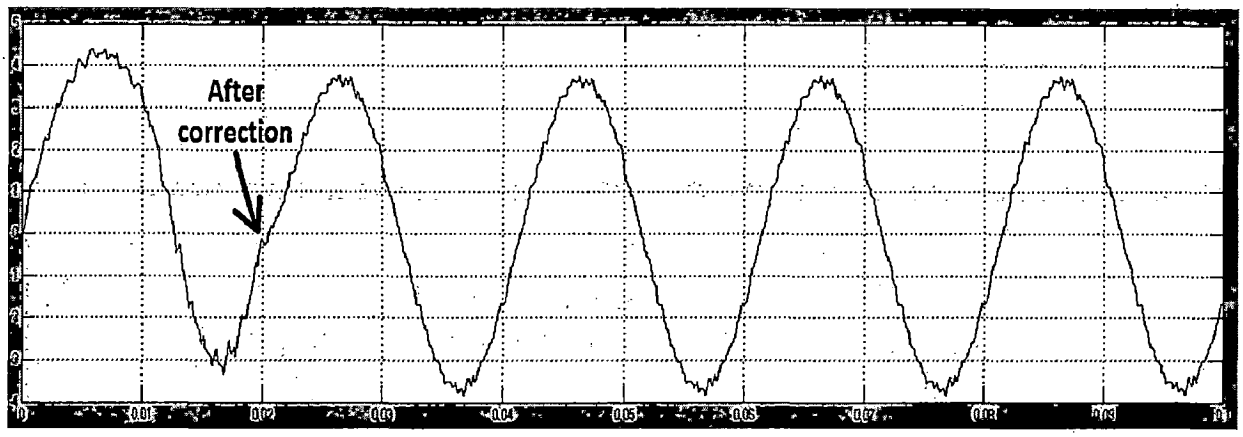

Fig.5.20 Faulted Phase currents with fault diagnostic system

As can be seen from the Fig. 5.20 that the fault diagnostic system is taking 0.02sec to detect the fault type.

CONCLUSION

The fault detection method which is designed using Fuzzy Inference system is able to detect the fault location. But this type of detection doesn't work properly if 3rd harmonic content varies in a wider range. And it needs proper judgment in designing the membership functions. These problems can be eliminated with ANFIS. It doesn't require the modeling of membership functions. ANFIS does this thing itself. Just by giving the training data and target data we can design the ANFIS structure for detection of fault

The Adaptive Neuro Fuzzy Inference system which has been designed, and developed and trained to detect the most common types of fault locations like single switch open circuit faults, short circuit faults. Various simulation experiments were conducted to test the system, and the results show that the Adaptive Neuro Fuzzy Inference system which was trained with FFT samples of the output voltages approach gives high accuracy about (98%) in detecting the fault location in inverter.

The reconfiguration technique based on the addition of 1- extra leg has the advantage that it requires only 4 extra switching devices for reconfiguration purpose, but it is useful if fault occurs only on one switching device. This problem can be eliminated by properly designing the fault detection system so that it detects the fault in less than one fundamental period of the output voltage. If the fault detection system is unable to detect the fault location within that time, we can go for reconfiguration technique using addition of 3-legs. But it needs 12 extra switching devices which increase the cost for the reconfiguration system. The use of 3-legs is useful even if the fault occurs on 2 or more switching devices at a time.

The reconfiguration techniques which are proposed here can isolate the faulted leg without interrupting the supply to load through inverter. And it can detect the fault location within one fundamental period (here it is 20ms) of the output voltage.

SCOPE OF THE FUTURE WORK

- Comparing the presented method with any of the conventional methods.
- Development of the hardware model for the multilevel inverter.
- Extinction of fault detection method for multi switch faults.
- We can extend this work for different multi level inverter topologies and for different faults which occurs outside the inverter using the same method of fault detection.
- We can extend this work to decrease the time for fault detection.

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