SPEED CONTROL OF INDUCTION MOTOR WITH SILICON CONTROLLED RECTIFIER

A Dissertation
submitted in partial fulfilment
of the requirements for the degree
of
MASTER OF ENGINEERING
in
ELECTRICAL ENGINEERING
(Advanced Electrical Machines)

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C E R T I F I C A T E

CERTIFIED that the dissertation entitled "SPEED CONTROL OF INDUCTION MOTOR WITH SILICON CONTROLLED RECTIFIERS", which is being submitted by Sri Jugal Kishore Mendiratta, in partial fulfilment for the award of Degree of Master of Engineering in Advanced Electrical Machines, of the University of Roorkee, is a record of student's own work carried out by him under my supervision and guidance. The matter embodied in this dissertation has not been submitted for the award of any other Degree or Diploma.

This is further to certify that he has worked for a period of 8 (eight) months from January to August for preparing dissertation for Master of Engineering Degree at this University.

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CONTENTS

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NOTATIONS

N_0 : Synchronous speed in r.p.m.

f_1, f : Supply frequency in c/s.

p : Number of poles.

L : Length of rotor in metres.

k_{p1} : Winding pitch factor.

k_{d1} : Winding distribution factor.

B_0 : Maximum flux density in Web/m^2.

τ : Pole pitch.

I_d : D.C. current in amperes.

I_{s1} : Saturation current for junction one, in amperes.

I_G : Gate current.

α_1 : Normal alpha with junction one emitting and junction two collecting.

t_c : Commutating time.

L_d : D.C. inductor.

( ) : Bracketed numerals are references listed in Bibliography.

SYNOPSIS

Different types of schemes for speed control of induction motor with silicon controlled rectifier has been reviewed. Principle of different types of inverters enumerated. A three phase static inverter with frequency range from 1 c/s to 100 c/s has been designed and fabricated. Generally the inverters have output wave form rich in harmonics. The speed control of a ½ H.P., 3 phase, squirrel cage induction motor has been attempted by varying the supply frequency from 1 c/s to 100 c/s from the output of the inverter.

CHAPTER I.

INTRODUCTION

It is long since it was felt necessary to devise satisfactory variable speed drives embodying the robustness and simplicity associated with commutatorless a.c. motors. The d.c. commutator motors are used for wide range of speed control by either controlling the field current or armature voltage. In many applications, commutator of a d.c. motor is a source of trouble; it requires periodic maintenance, which may be inconvenient due to interruption in service or access to commutator may be difficult or when motor is submerged in some liquid. On the contrary a.c. motors and particularly induction motors need little maintenance service. But the main difficulty with these motors is that they are generally constant speed, because speed is linearly related to supply frequency which is generally constant. The variable speed a.c. motors can be made in various forms, but in most cases, either they are inefficient or they afford only a limited control of speed or they incorporate commutator and thus have no advantage over the d.c. motor apart from working directly from an a.c. supply.

The possibility of producing a d.c. motor in which commutator has been replaced by static switches or gas filled thyratrons has been recognised. There is no need to have separate switch for each commutator segment, but it is only necessary to arrange the switching circuits in such a way that they maintain in the armature an m.m.f. pattern which is stationary with respect to the field system. With static switching system it is more inconvenient to have the armature stationary and the field system rotating, in which case the armature m.m.f. wave rotates at synchronous speed relative to motor frame. Thus function of static switches is to produce a synchronous rotating field in the stator of the machine, so, the switches must be arranged in such a way as to achieve a sufficiently good m.m.f. waveform. It is equivalent to using a synchronous a.c. motor supplied from a static polyphase invertor. The advantage of synchronous motor is that its speed can be regulated as accurately as may be desired, by stabilising the supply frequency. The power factor can also be controlled by controlling the field excitation.

But in most cases where a marginal speed variation with load is allowed squirrel cage motor may be preferred, because it can compensate the cost of invertor, particularly in case of single motors drive.

Speed control of small induction motor can be done by controlling the stator voltage supply but at low speeds the efficiency is reduced with reduction of torque.

Speed control is also limited to subsynchronous range. Alternative method of speed control by transfer of slip energy to supply is also limited to subsynchronous range generally. On the contrary speed control of induction motor by variable frequency supply offers a continuous control of speed over a wide range. Of course to achieve a viable scheme of speed control magnitude of supply voltage should also be amenable to control.

The systems in which the frequency, other than supply frequency have been used for some times, in connection with railway traction and mill drives etc. But these variable frequency systems have generally been based either on rotary frequency changers or on thyratron invertors, in which the advantage of variable frequency is realised to a limited degree.

The other method for variation of frequency uses cycloconvertor which converts the fixed frequency a.c. supply to variable frequency output without intermediate rectification. But in this case output frequency is limited only from one third to supply frequency, one cannot have the speed control from zero upto maximum. Where a wide range of speed control is required, the most practical system is one that comprises a rectifier followed by a variable frequency invertor. Due to superior switching characteristics of thyristors, considerable progress has been made in supplying variable frequency to induction motor for wide range of speed control.

In the present work, a variable frequency inverter has been designed and fabricated to have the speed control over a wide range.

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CHAPTER II.

C_H_A_P_T_E_R _II.

SPEED CONTROL, INDUCTION MOTOR USING S.C.R. MOTOR.

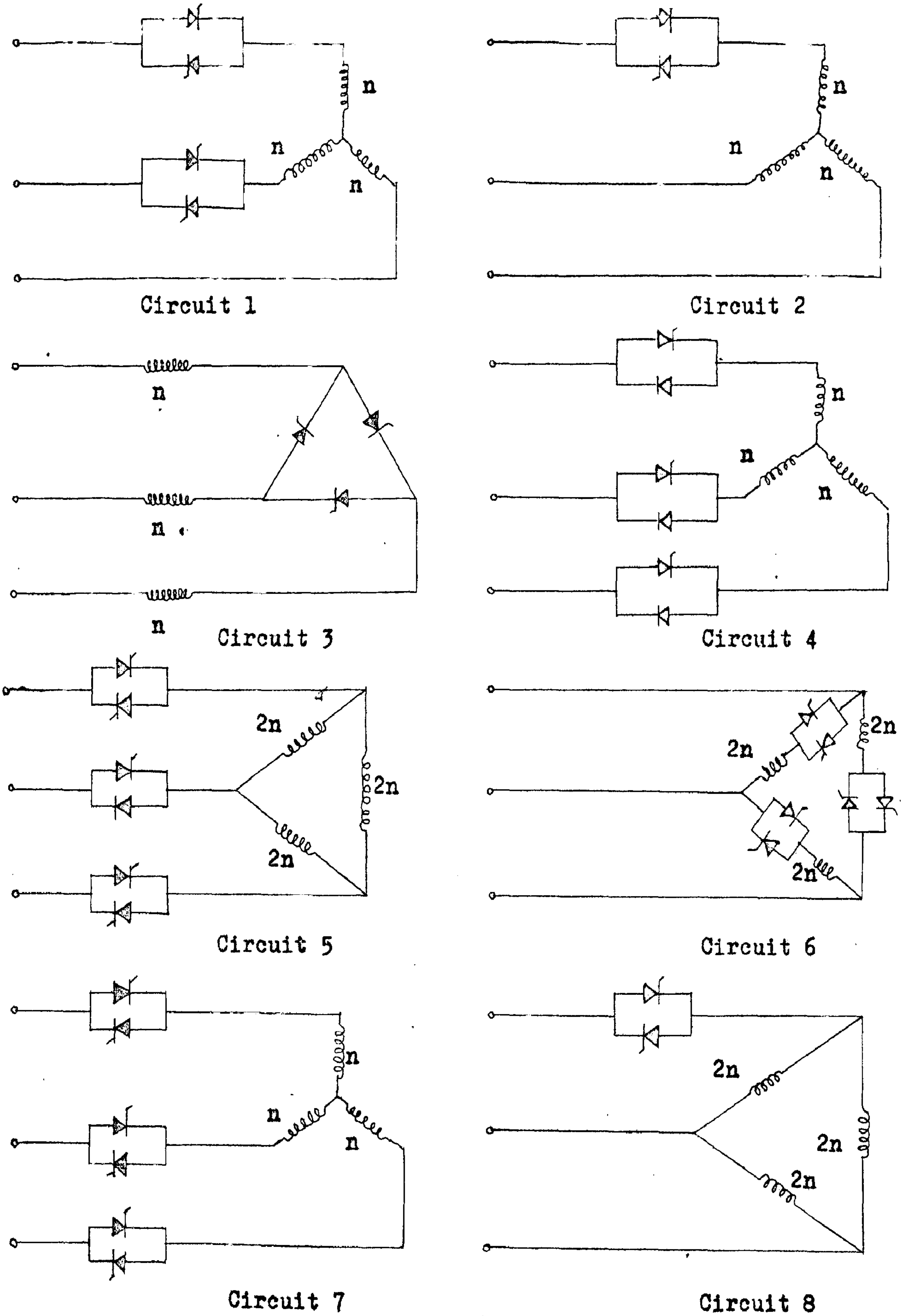
Review: - In the last few years, different methods have been developed to control the speed of Induction motor for different applications. As has been pointed out that there are different methods to control the speed of induction motor. With the development of thyristors these methods have become more suited.

2.1. Speed control by stator voltage control:

It is the well established technique for speed control. Variation of voltage, symmetrically or unsymmetrically, on open loop gives a wide range of useful torque-speed curves. Many schemes have been given by different authors, by means of saturable reactor or saturable transformer connections. With thyristor the voltage control can be done very easily. D. A. Paice(5) has discussed various circuit arrangements for voltage control by use of thyristors (Fig. 2.1)

Power considerations: The speed of an induction motor is given by: $N_s = \frac{120f}{p}$. For sinusoidally varying quantities average torque T_m is proportionate to $\frac{I^2R}{s}$,

R = rotor resistance I = rotor circuit, s slip.



Circuit 1

Circuit 2

Circuit 3

Circuit 4

Circuit 5

Circuit 6

Circuit 7

Circuit 8

Fig.2.1
Thyristor Power Circuits.

For fan loads, load torque is related to square of motor speed i.e. $T_L \propto (\text{rotor speed})^2 \propto (1 - s)^2$ where T_L = load torque.

$$\text{so,} \quad I = (1 - s)\,(s)^{\frac{1}{2}} / R^{\frac{1}{2}}$$

so input current will be maximum when $s = \frac{1}{3}$.

If torque is constant $I \propto (s / R)^{\frac{1}{2}}$, so heating will occur, as the speed is reduced. With chopped waveforms, as is with thyristors outputs motor will give more losses. Mr. Paice has given different power control circuits with their relative merits and demerits (Fig. 2.1).

Circuit 1 : In this circuit excessive current is required through two lines.

Circuit 2 : It is extremely simple, and as the motor stalls when operated on single phase, speed can be controlled down to zero. Excessive currents are required through two unregulated lines.

Circuit 3 : It requires only three thyristors and represent the best possibility of simple circuits.

Circuit 4 : Performance is similar to circuit 3.

Circuit 5 : It represents a conventional balanced three-phase control approach and gives a good performance. At 33 per cent slip, input current is 14 per cent greater than for sine wave control.

Circuit 6 : It is also conventional approach, but performance is not as good as Circuit 5.

Circuit 7 : It gives very good performance. At 33 per cent slip the input current is only 8 per cent greater than for sine wave control.

Circuit 8 : It is similar to circuit 2 and causes excessive large currents in motor windings.

So, circuit 7 is the best of all above circuits. As input current is not significantly increased over the stator losses.

If solid iron rotor is used instead of squirrel cage rotor, for speed control by changing the stator voltage V, the induced air gap voltage E is also (5) reduced and thus a reduction of rotor iron flux penetration, i.e. a decrease of the depth of rotor penetration belt, or in other words, parameter $\frac{b.fl}{E}$, which corresponds to R^2 of conventional motor acquires larger values, then E is decreased and so ratio $\frac{\text{stator loss}}{\text{rotor loss}}$ becomes smaller as slip increases, without deteriorating performance in range of high speeds i.e. high applied stator voltage. The favourable influence of the rotor characteristics of solid rotor machine is shown in curve of Fig.2.2, which shows that it is most suited for speed control by voltage control. For solid rotor machine, the torque increases linearly with slip except for the influence of stator drops with constant load torque, so it is stable.

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where b is defined as :

$$b = \frac{57.2\, mL^2\, (k_{p1} \cdot k_{d1} z N)^2\, D_s}{p\, V}$$

depth of penetration :
depth in which the wave has been attenuated approximately 37 per cent of its original value.

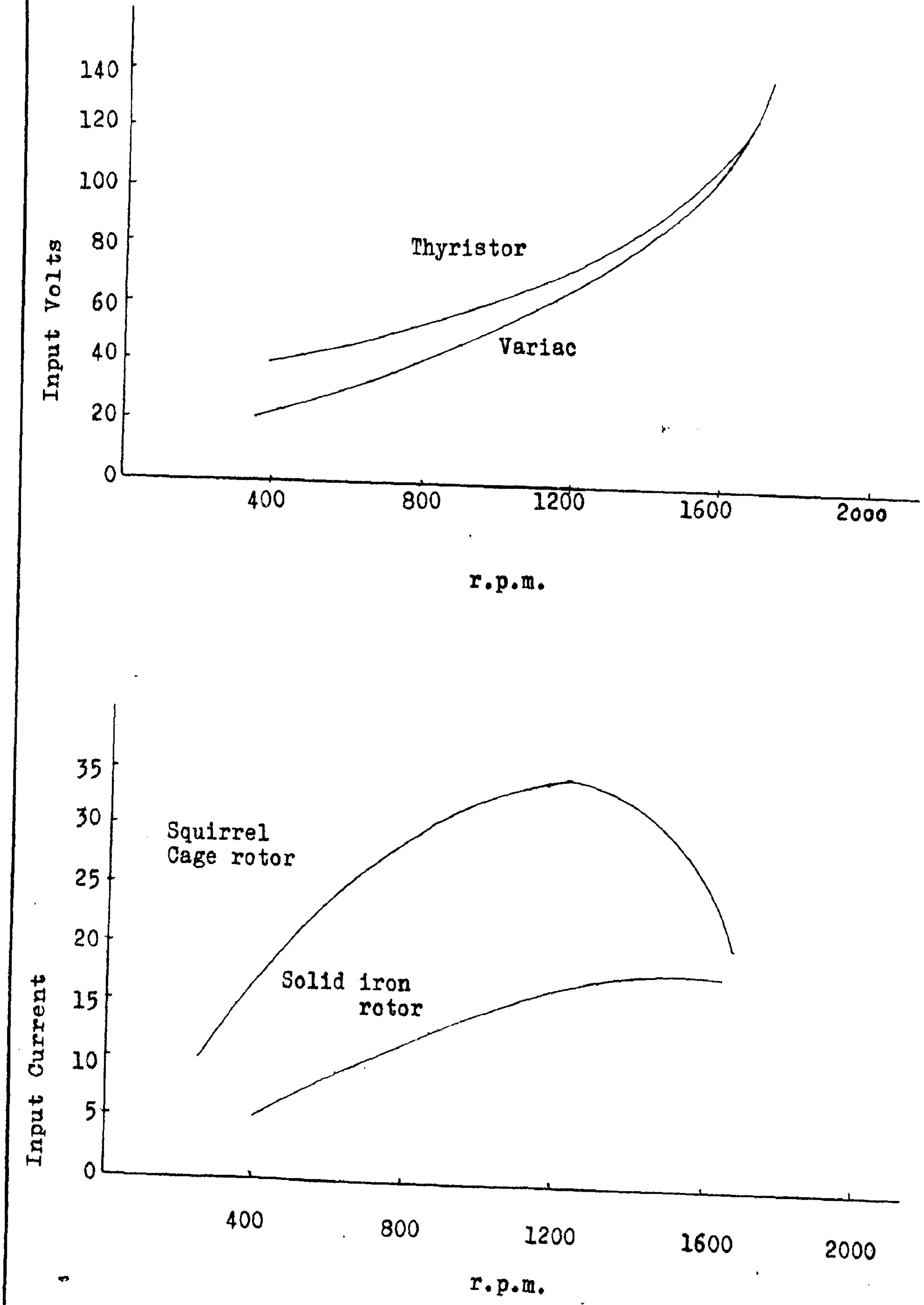

Input Volts
140
120
100
80
60
40
20
0
Thyristor
Variac
400
800
1200
1600
2000
r.p.m.
Input Current
35
30
25
20
15
10
5
0
Squirrel
Cage rotor
Solid iron
rotor
400
800
1200
1600
2000
r.p.m.

Fig. 2.2

For the speed control of a hoist or elevator the d.c. shunt motor type of steady state torque-speed characteristic is necessary. When speed is to be kept constant with change of load, closed loop system is required. W.Shepherd(1) and J. Stanway have analysed the problem with voltage control in a closed loop, of motor for speed control of motor (Fig. 2.3).

The signal proportional to speed is fed to the thyristors to control the firing point and so the applied voltage to motor. The change in speed is fed back to the signal as error, to adjust the firing angle. The transfer function of induction motor is assumed. The transfer function of power modulator should match the induction motor, for linear variation of speed and error signal. In the experiment, six thyristors have been used in pairs in all the three phases. The speed and error was found to be linear variation in steady state. The transient response was similar to slightly over damped second order system. The drive was found to have the disadvantage that controlled speed reduction was not possible. A sudden reduction of reference signal caused the error signal to go negative due to positive only response of thyristor triggering, control was lost until the load had decelerated the motor speed to the point where the feedback signal was once more slightly smaller than reference signal.

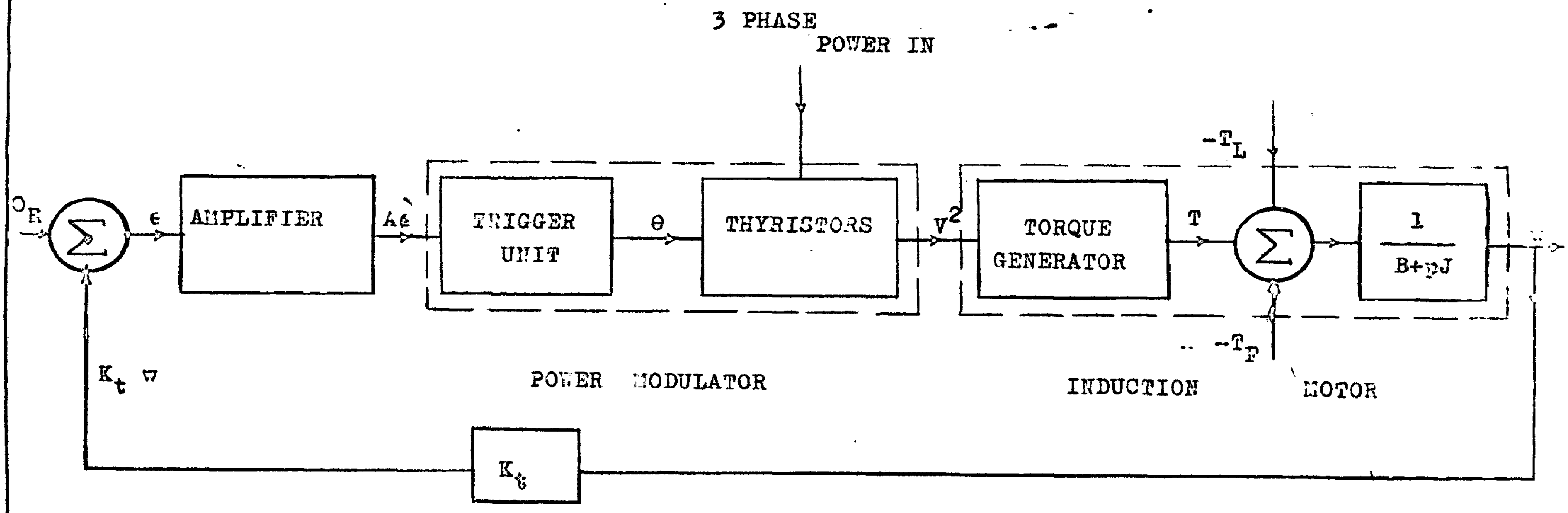


Fig. 2.3 Block Diagram of a closed-loop drive incorporating a thyristor driven induction motor.

2.2. Speed control by slip power recovery:

At low speeds the efficiency of Induction motor can be improved by feeding the rotor energy to a.c. supply by rectifying and inverting at line frequency so, the torque speed characteristics will be similar to a variable speed drive. Many methods have been developed to extract the slip frequency power from rotor, rectified and actively used, than dissipated in resistors. It can be used in two methods:

(i) By connection to the armature of a d.c. motor mechanically coupled to the induction motor shaft.

(ii) By inversion to line frequency, and injecting it to a.c. supply. Erlicki has described a rectifier-inverter scheme for feeding the rotor with slip frequency e.m.f's. using the principle of stator fed, shunt commutator motor.

W.Shepherd and J.Stanway(2) have used the line commutated inverter to feedback the rotor power to lines. When the equal firing angles of six inverter thyristors are greater than 90°, and when the applied rectified voltage is high enough to overcome the opposing e.m.f. of inverter, inversion occurs and power is recycled from rotor back to supply. But in these scheme, the power factor is very poor.

Peter N. Miljanic(3) has described a through pass artificially commutated inverter. Its basic characteristic is the two mode operation:

(i) Inverter is short circuited so that d.c. energy is stored in choke and a.c. line is disconnected from d.c. circuit.

(ii) The direct current is forced to flow into the a.c. line against the line e.m.f. and energy recovery occurs. Time ratio of two modes which occurs every half cycle, determine the voltage ratio between d.c. and a.c. line voltage. The operation is similar to time ratio control.

This type of inverter may be of two types:

(i) <u>Line commutated</u>: Fig.(2.5) shows the line commutated through pass inverter for single phase. During $t_1 - t_2$ inverter is short circuited through T_2 and T_4. At t_3, T_3 is turned on and still positive voltage turns T_4 off. When line voltage changes its polarity, power is delivered to a.c. lines. At t_3, T_1 is turned on which interrupts the inversion, turns T2 off and establishes the short circuit mode. In the next half cycle, the process is repeated. Firing angle of t_2 and t_4 is fixed and inverter is controlled by shifting only the firing pulse at t_1 and t_3. Fig.(2.5) (b) shows the line voltage, current and power delivered at three values of firing angle αo. Average d.c. voltage will be:

$$E_d = \frac{2}{T}\int_{t_2}^{t_3} E_m \sin \omega t \, dt = \frac{\sqrt{2}\, E_1}{\pi} (\cos \alpha_1 - \cos \alpha_0)$$

E_1 = r.m.s. voltage, E_m = maximum line voltage.

α_1 = fixed firing angle.

When $\alpha_0 \longrightarrow 0$, d.c. voltage becomes slightly - , slip-rings are short circuited, machine is running near synchronous speed and invertor is disconnected. Power factor is improved considerably, but invertor still consumes reactive power, especially at half rated motor speed.

(ii) Artificial commutation: Fig.(2.6) capacitor C and diodes D_5, D_6 are used for artificial commutation. In Fig.(2.9)(c), during $t_1 - t_3$ invertor is shorted through T2, D5, and T4. At t2, thyristor T1 turns on and voltage on capacitor turns off T2, Id flows through T1,C,D5 and T4. Capacitor voltage charges from its maximum negative value to a positive value equal to line voltage at t 2 causing current to flow through T1, D5, C and T4. For some time a fraction of current Id flows through C and D5, charging the capacitor to the maximum value of the line voltage Em. When e starts to decrease, D5 clamps the charge on C. At t3, T3 is turned on and line voltage turns off T4. Short circuit is now through T1, D5, T3. Average d.c. voltage:

$$E_d = \frac{2}{T}\int_{t_2'}^{t_3} E_m \sin \omega t \, dt = \frac{\sqrt{2}\, E_1}{\pi}(\cos \alpha_1 - \cos \alpha_0) - \frac{8 f E_1^2 C}{I_d}$$

Now α_1 is controllable and α_0 is fixed.

Second term represent voltage drop due to line delay between firing of T1 and T2. This delay is due to time necessary for reversal of voltage of C and so is inversely proportional to current and is given by:

$$\Delta t = \frac{2\, E_m . C}{I_d}$$

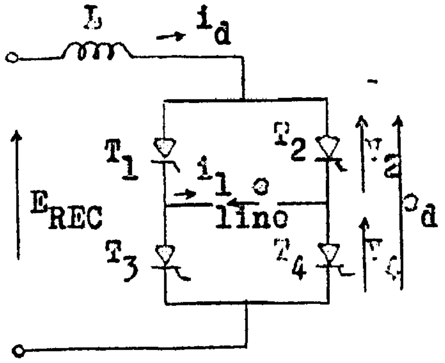


Fig.2.4 Line Commutated Single-phase through pass inverter

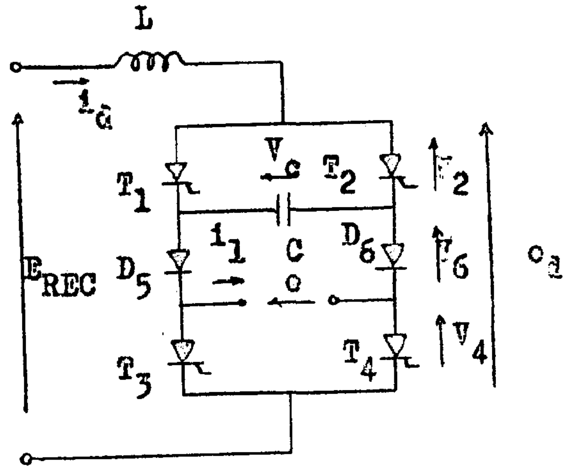


Fig.2.5 Artificially Commutated Single-phase through pass inverter ,

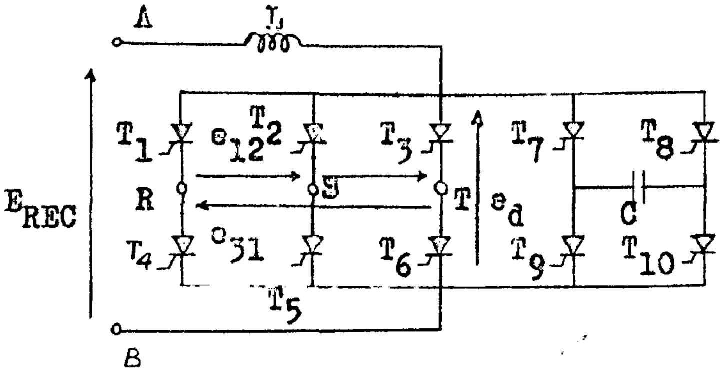
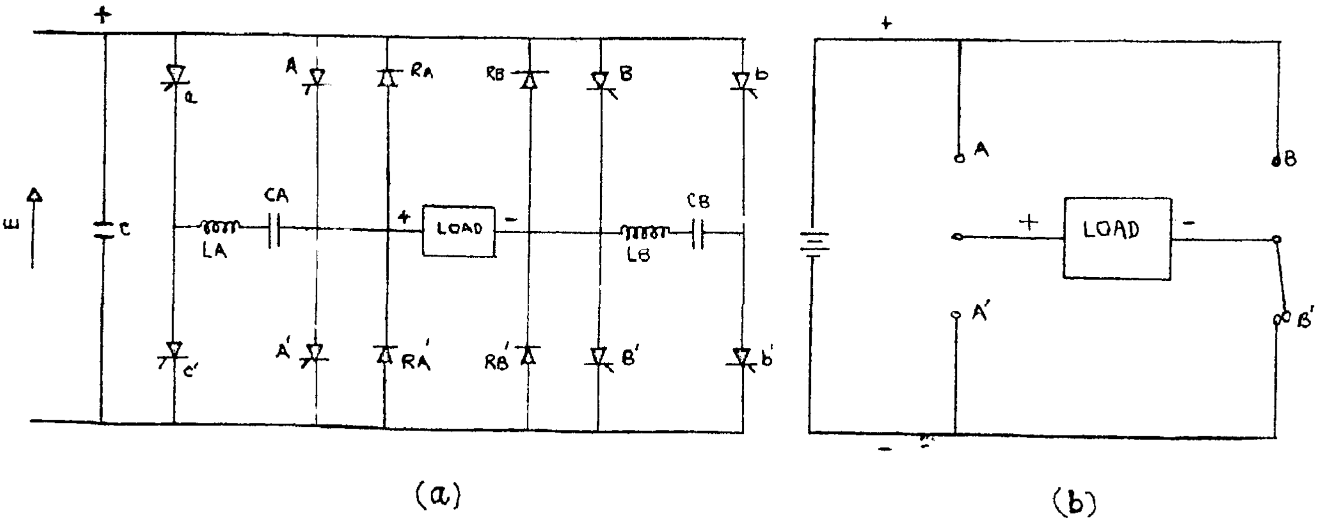


Fig.2.6 Three-phase Bridge inverter with artificial commutation.



(a)

(b)

Fig.2.7 Thyristor inverter. (a) Thyristor inverter

(b) Switch analog.

For three phase operation Fig.(2.7) the three single phase units are connected in three phases. For equal voltage and current distribution, generally a.c. sides are connected to a multiphase transformer and d.c. sides in series. This scheme gives characteristic similar to Ward Leonard drive. For various invertor settings speeds from $s = 0$ to $s = 1$, can be achieved, as well as braking operation for $s < 0$ and $s > 1$.

2.3. Speed control by change of supply frequency:

As has been discussed, the speed control of Induction motor with stator voltage control and slip power recovery has its many disadvantages:

(i) maximum torque which the machine can generate is proportional to the square of the stator voltage.

(ii) The slip at maximum torque is independent of input voltage, so stator voltage control allows only small changes in rotor speed. At low slip the torque-speed characteristic is not affected by stator impedance, so change of slip power has also some disadvantage.

So, when speed control over wide range is required only change of synchronous speed is useful method. Two methods can be used for by change of frequency of applied voltage:

(i) Cycloconvertor: the disadvantage is that speed control is limited only upto one third of supply frequency.

(ii) Variable frequency inverter: In the last few years, inverter technology has become a separate branch of Electrical Engineering. Detailed description and principles of inverters has been described in next chapter. A few inverters used by different workers has been described below:

Pulse width modulated inverter: (6)

Pulse width may be defined as the control of the average level of a quantity by applying or driving the quantities in discrete intervals or pulses. The circuit Fig.(2.8) can be divided into two portions A and B Upper case character denote main thyristors and lower case, denote auxiliary thyristors, which help to turn off the main thyristors. If thyristor A is conducting, to commutate it off thyristor a is fired which connects the charged capacitor CA, so diverting the current from thyristor A. Similarly A′, B, B′ are turned off by the action of auxiliary thyristors a′, b, b′ respectively.

Boris Mokrytzki has used McMurray-Bedford inverter. Four thyristors are grouped in two phases, A phase and B phase. Pulse width operation is as discussed above. If thyristor A is on, A′ off, capacitor C A′ charged to E, CA to zero volts. Reactor X1 is assumed to incorporate an inductance L associated with each winding and perfect coupling between each winding.

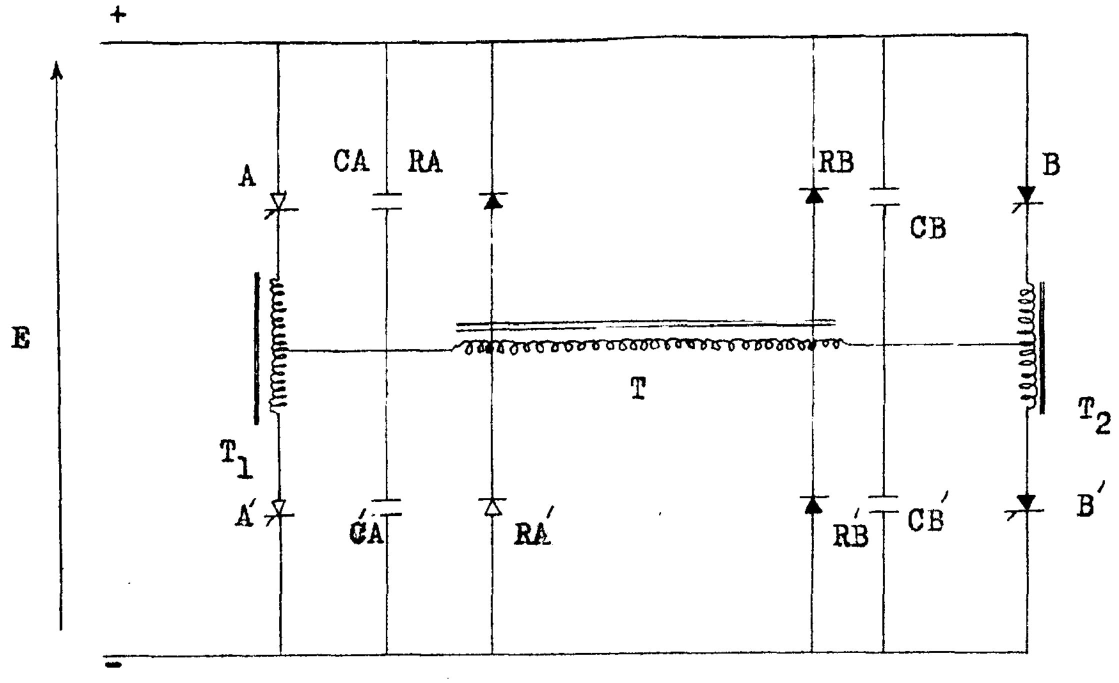


Fig. 2.8 Improved McMurray-Bedford circuit.

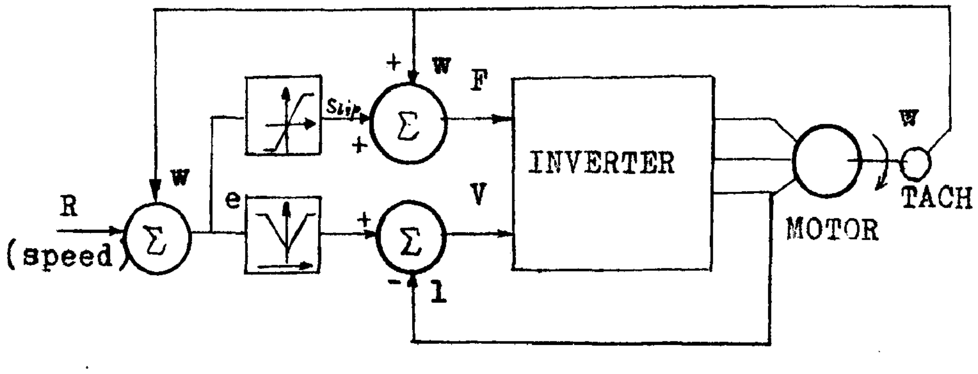


Fig. 2.9 Controlled slip drive system.

Triggering A places the voltage of CA′(E) across lower portion of T1, via transformer action, across the upper portion, placing the cathode of A at + 2E volts, so reverse biasing it by a net voltage of E volts and achieving turn off as the charge originally on C A′ transfer to CA. T1 must be capable of sustaining a direct current because both the load current and pulsation of commutation are polarised with respect to reactor.

To utilise the trapped energy (i.e. energy transmitted to the reactor during [illegible] commutation) actively auxiliary transformer T is used. A portion of the transformer n is clamped to the supply voltage E by the rectifier bridge, introducing a voltage E / n in a portion of the transformer, associated with the trapped energy current loop. It has two effects:

(a) Due to increased discharged voltage, a rapid decrease of trapped current.

(b) Transformation of trapped energy via the clamped portion of T. The disadvantage is that blocking voltage of each thyristor is raised by $E[1+(1/n)]$ volts.

With change of frequency, the supply voltage must also be controlled simultaneously, to keep the flux in the air gap of motor to be constant. So, for voltage control either variable transformer, or variable d.c. bus is used generally for higher powers, harmonic cancellation and switched inverters can be used. The best method can be the three phase bridge rectifier with three thyristors and three rectifiers, with filter. For thyristor firing some signal can be applied, to control the voltage, which is used to control frequency. The disadvantage of inverters is their nonsinusoidal output. To reduce the harmonics , various methods have been used such as subharmonic method, pulse width modulation or filters can be used at output of inverter.

Pulse Width Modulated inverter has the advantage of frequency and voltage control in one circuit. The inverter voltage is controlled by average width of pulses and harmonics are controlled by modulating to a sinusoidal envelope. Modulating frequency harmonics can be made so high so that rotor may reject them. It can be assumed as 'black box' with two control inputs: one for frequency and other for voltage. As the speed of response, is high, so it can be used in any close loop system for constant torque operation. As the rotor flux is formed with the product of stator flux and slip. It can be varied to set the torque by adjusting slip or excitation just as the armature flux is controlled by adjusting current in a d.c. machine. To have the maximum value of rotor flux at same level, slip must be increased as the stator flux is weakened in the constant horse-power mode. The arrangement is shown in Fig.(2.10) which includes a slip control loop(7) and a stator flux regulator brought about by a shaped current reference that produces indirect stator flux control. Operating above base speed in the constant horsepower range is limited by the maximum

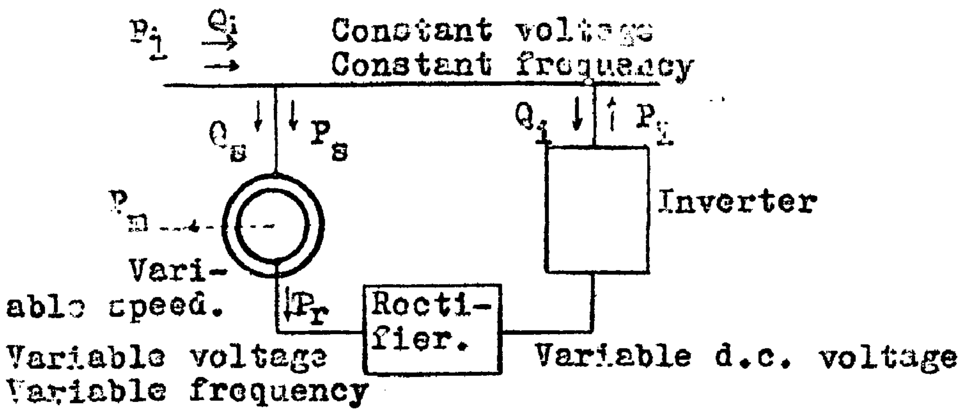


Fig. 2.10 Slip power recovery system.

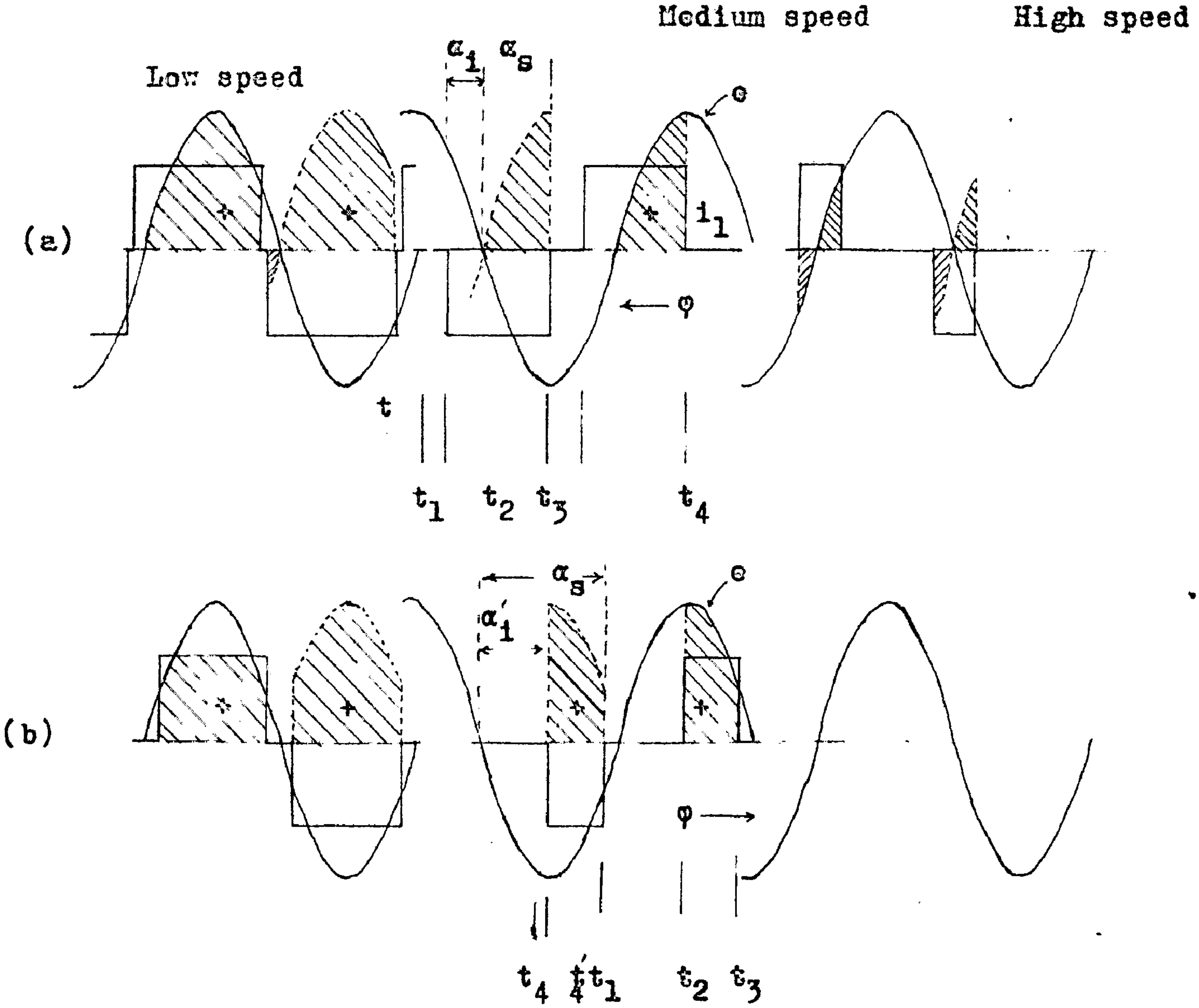


Fig. 2.11 Wave forms of inverter output current at various motor-speeds

(a) Line commutated through pass inverter

(b) Artificial commutated through pass inverter.

practical slip obtainable from the motor. This is about twice rated slip, hence the constant horsepower range for a motor extends to about twice the base speed.

-::-

C_H_A_P_T_E_R III.

C H A P T E R III.

COMMUTATION IN INVERTERS.

The Silicon controlled rectifier:(11)

For better application of inverter operation, the operation of S.C.R. under different conditions should be detailed. In the following different stages of S.C.R. operation has been described.

It is a three junction, four layer semiconductor device. In this device the end p region is called the anode and the end n region is called the cathode, p region in the centre is called the gate. It is a bistable switching device. It normally has no linear region of operation as for the transistors. Thus S.C.R. operates either in the saturated region or in the cut off region. With a reverse voltage applied to its anode to cathode terminals, the device will not conduct any appreciable current. When the anode is made positive with respect to the cathode again no appreciable current flows. But when anode is positive and cathode is negative, and a small positive voltage is applied across, gate to cathode terminals, the device switches 'on'. The current flow from anode to cathode is limited only by external load impedance. When the appreciable forward current flow from anode to cathode the gate to cathode signal is no longer required to maintain the device in its 'on' condition. When the device has switched to its 'on' condition, the forward current can be extinguished by increasing the circuit impedance to reduce the current below a specified value, making the cathode terminal positive with respect to the anode terminal or in relatively low current controlled rectifiers, by applying a negative current pulse to the gate terminals. The voltage current characteristics of S.C.R. can be considered in three regions: Fig.(3.1).

Region A: It occurs when cathode is positive to anode. It reverse biases junction two, so S.C.R. allows only a small leakage current to flow from cathode to anode. Anode current can be expressed by

I_a (Region A) = $-[I_{o1} + I_g\ (\alpha 2\ \alpha 1)]$

The increasing of the reverse leakage current by the additon of gate current can increase the junction heating and can cause thermal runaway. If the junction temperature is raised the saturation current will increase and so will further increase junction temperature. As with increase of reverse voltage of anode to cathode increases the depletion of junctions one and three, so to make high voltage units, width of center n region is made large so that depletion layer is not punched through.

Region B: In this region anode is positive and cathode is negative and the device is in blocking condition, junctions one and three are forward biased and junctionnnn two is reversed biased, so anode current is very small. Anode current will be:

I_a (Region B) = $I_{o2} + I_g\ \alpha 2$

where I_{o2} is saturation current for junction two in ampere.

As anode current is positive so increase of gate current will increase the anode current.

Leakage current is in micro to milli amperes.

Region C: There are four methods for switching the thyristor from region D to region C. If the anode to cathode voltage is increased, depletion layer at junction two is increased, so is the accelerating voltage for minority carriers crossing junctiontwo. When these carriers are accelerated across junction two, they collide with the fixed atoms of the crystal structure and dislodge additional minority carriers. With increase of voltage, minority carriers dislodge many additional carriers during their transient across junction two, resulting in an avalanche breakdown of the junction, and so junction two also becomes forward biased. As all the junctions are now forward biased, so anode current is limited only by external load impedance. The anode to cathode voltage at which device switched from Region D to Region C is called forward breakover voltage.

If the gate to cathode is made positive, which injects additional minority carriers into second junction, is the second method of switching the device from Region D to Region C. Switching takes place at less anode to cathode forward voltage, than forward break over voltage. So, this is the method generally used to switch from Region D to Region C.

The third method is to illuminate the gate to cathode region.

The fourth method is by rapidly increasing the anode to cathode voltage. This dv / dt turn on is believed to be caused by anode to gate and gate to cathode capacitances.

3.2. Silicom controlled rectifier turn off:

There are three methods to turn an S.C.R. off.

(i) Anode current is reduced to minimum, called hold on current. In this case anode is maintained at positive potential. Anode current can be reduced by opening a line switch, increasing the load resistance or by shunting, part of load current.

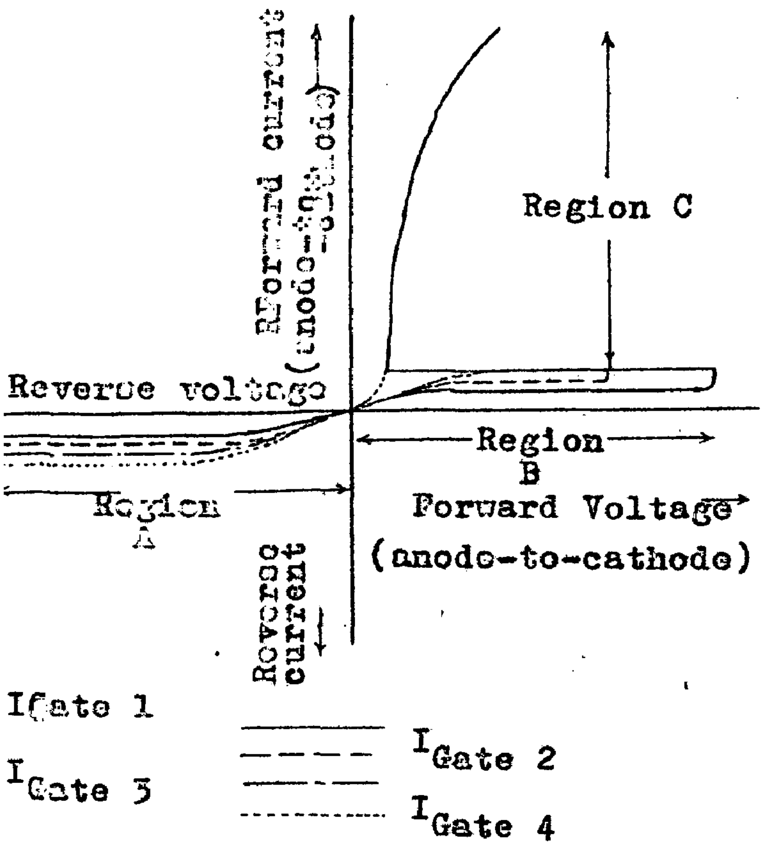
(ii) Anode current is interrupted by reversing the anode to cathode voltage. The device switches to region A by reversing the polarity of A anode.

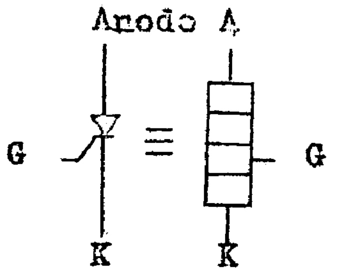
(iii) By supplying a negative gate current, but this is used in low current rating devices.

For second method, the thyristor is usually reversed biased for an appreciable portion of negative half cycle of supply voltage.

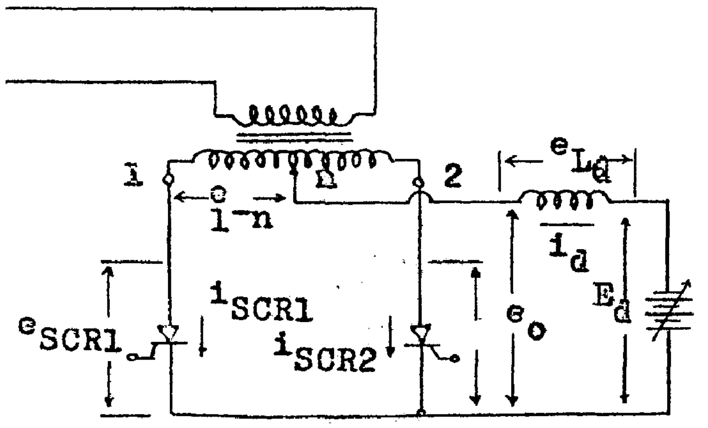
3.3. Type of Inverters:(11)

While the transfer of current from one value to another occurs automatically due to periodic variation of anode voltage level in a rectifier circuit, the reliable accomplishment of this current transfer is one of the basic problems of the inversion process. The commutation is the process of current transfer from one electric valve to another in rectifier and inverter circuits. The commu-

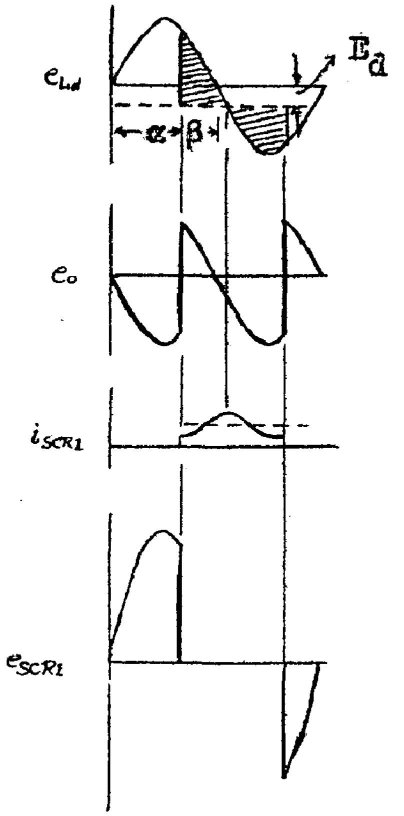




. 3.1 p-n-p-n Controlled rectifier, volt-ampere characteristic.



(a)



(b)

Fig. 3.2

ll-wave, single-way, phase-controlled rectifier and a-c line
mmutated invertor.

veforms with $\alpha = 120^{\circ}$.

-tation may involve different events:

(i) reduction of forward current to zero in one valve

(ii) the delay of reapplication of forward voltage to this valve till it has regained its forward blocking capability

(iii) build up of forward current in second valve. In case of low frequency operation the circuit constants generally determine the time interval required for complete commutation. For higher frequency inverters, characteristics of SCR are required for complete commutation process. The difference in inverters is mainly due to the particular technique which is used to reduce the current to zero in a conducting valve and delay the reapplication of forward voltage to this valve until it has regained its forward blocking capability. Inverter circuits can be self excited, where the circuit is self oscillatory or separately excited where a signal oscillator is used as a driver for the power inverter. Self excited type inverter will often require some separately applied transient to start. In separately driven inverters, starting transient will occur, depending upon the position in the driving oscillator cycle when d.c. power is applied to the inverter. Separately excited inverter must be designed to accommodate the starting transient currents which may flow due to inductive loads and transform magnetising current. Inverters can be classified as:

1. A.C. Line voltage commutated Inverter
2. Parallel capacitor commutated Inverter

3. Series capacitor commutated Inverter

4. Impulse commutated Inverter.

1. A.C. line voltage commutated Inverter Fig.(3.2):

To charge a given rectifier to an inverter, two of the most basic modifications that are required

(i) the two terminal rectifying elements must be replaced with thyristors,

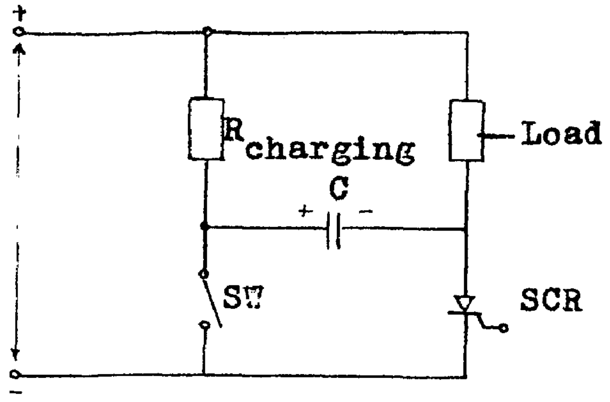
(ii) a relaib~~a~~le means of commutation must be incorporated into the circuit. The line voltage commutated inverter is nothing but phase controlled rectifier. When firing angle α is less than 90°, the rectifier will give positive voltage with reference to zero axis. When α is 90°, the output voltage will be zero and for α greater than 90°, the output voltage is negative, so the rectifier will deliver negative power or it will act as inverter. The average output voltage is given as :

$$E_o = \frac{1}{\pi} \int_{\alpha}^{\pi+\alpha} E_{l-n,m} \sin \omega t . d(\omega t)$$

$$\Rightarrow \frac{E_{l-n,m}}{\pi} \left[-\cos \omega t \right]_{\alpha}^{\pi+\alpha}$$

$$= \frac{2E_{l-n,m}}{\pi} \cos \alpha .$$

so, output voltage will follow a cosine curve, with zero at $\alpha = \frac{\pi}{2}$. For maximum phase control angle of retard for inverter operation, the angle β must be at least great enough to produce complete commutation $(\beta = 180 - \alpha)$. The time interval of negative voltage at S.C.R^{o}, must be



3 Principle of Parallel inverter.

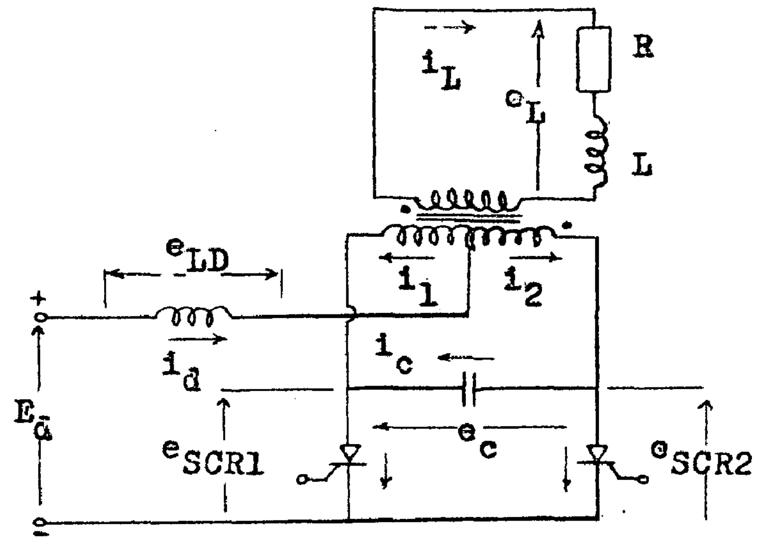
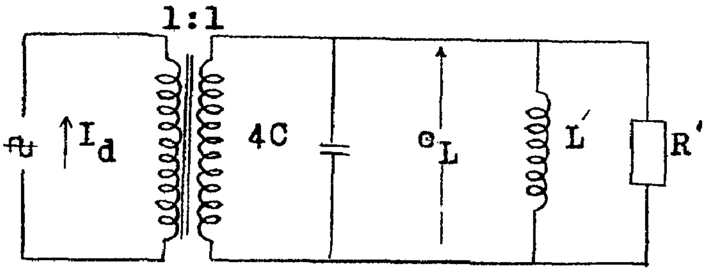


Fig.3.4 Parallel capacitor-commutated inverter.



.5 Equivalent circuit of Fig.3.4 with a large d-c reactor.

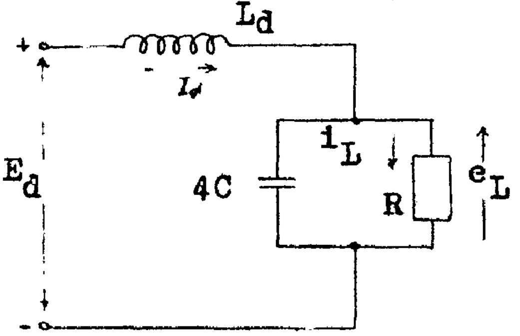


Fig. 3.6 Equivalent circuit of Fig.3.4 during each half-cycle.

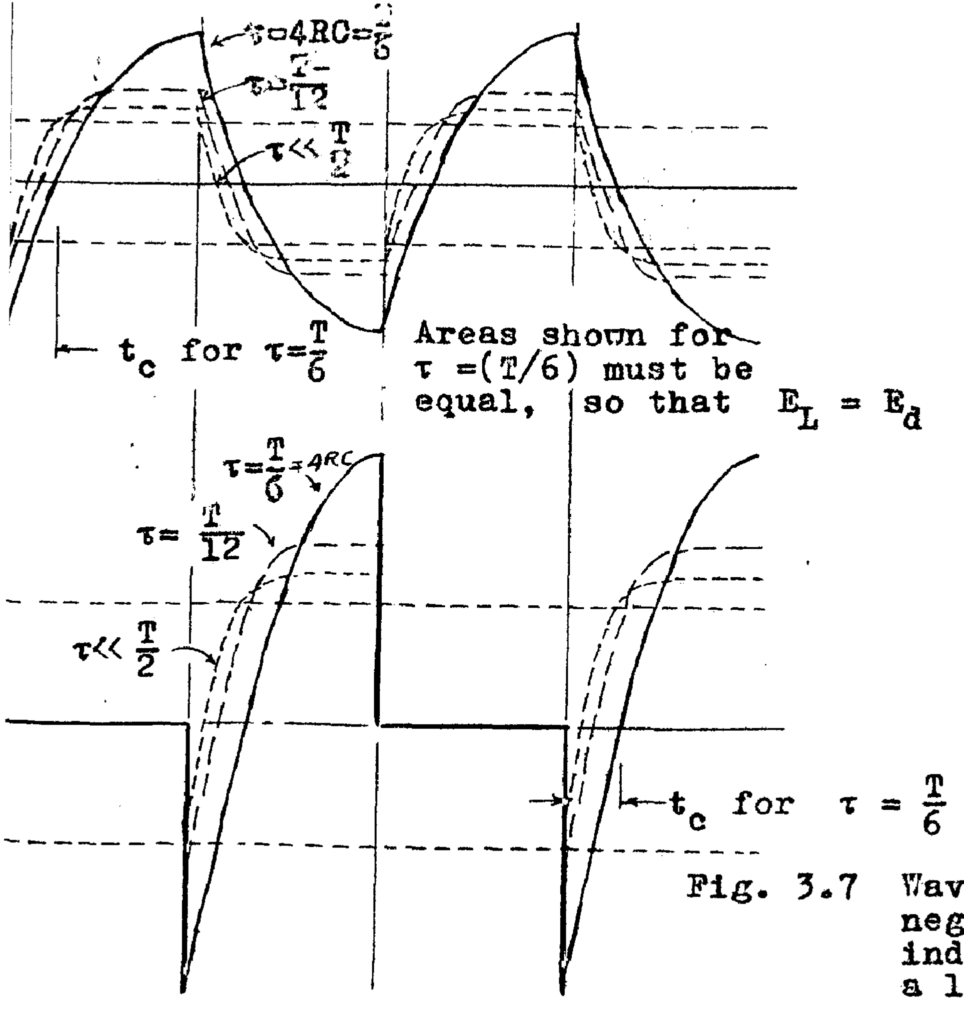


Fig. 3.7 Waveforms of Fig.3.4 neglecting load inductance and assuming a large d-c reactor.

sufficient to accomplish the principal events of commutation, otherwise the circuit will operate as rectifier, circulating excessive currents both in a.c. and d.c. circuits. Due to the reactance present in the circuit, the firing angle will be more delayed, so interval for negative voltage on thyristor is reduced which may cause failure of commutation.

2. Parallel capacitor commutated Inverters:

Commutating Principle: In this the commutating is done by capacitor connected in parallel with load. Consider the Fig.(3.3) when S.C.R. is gated on, the capacitor will be charged exponentially with polarity shown. Now, if S.W. is closed, capacitor will be connected across S.C.R. in a direction to provide a negative anode-cathode voltage diverting the load current through the capacitor turning off the S.C.R. Size of the capacitor depends upon the amount of load current and time interval required to put the S.C.R. off.

Single phase Inverter: The circuit is shown in Fig.(3.4). It is similar to the above circuit with commutating thyristor (instead of S.W.) and d.c. reactor. The commutation takes place when next S.C.R. is gated on. The d.c. reactor limits the inrush of current flowing in capacitor. The D.C. source alternately supplies D.C. to the two halves of the transformer primary producing m.m.f. of opposite polarity, which is equivalent to a square wave alternating current in a single primary winding and thus the transformer secondary delivers an a.c. to the load. The capa-

-citor can be placed on the secondary side giving a simplified equivalent circuit as shown in Fig.(3.5). A net capacitive reactance is generally required for satisfactory operation. The square wave current source input can be solved into Fourier components and would give active and reactive components of current corresponding to the equivalent parallel load.

<u>Circuit Analysis:</u> A detailed analysis of Fig.(3.5) can be done by solving differential equations with the assumption that load inductance and ripple in d.c. current is negligible.

So, the equations will give:(11)

$$e_L = \frac{Ed(1 + \epsilon^{-T/2\tau} - 2\epsilon^{-t/\tau})}{1 + \epsilon^{-T/2\tau} - \frac{4\tau}{T}(1 - \epsilon^{-T/2\tau})} \quad --- \quad (1)$$

$$i_2 = \frac{Ed}{R} \cdot \frac{\epsilon^{-t/\tau}}{1 + \epsilon^{-T/2\tau} - \frac{4\tau}{T}(1 - \epsilon^{-T/2\tau})} \quad --- \quad (2)$$

$$i_L = \frac{Ed}{R} \cdot \frac{1 + \epsilon^{-T/2\tau} - 2\epsilon^{-t/\tau}}{1 + \epsilon^{-T/2\tau} - \frac{4\tau}{T}(1 - \epsilon^{-T/2\tau})} \quad --- \quad (3)$$

$$i_1 = \frac{Ed}{R} \cdot \frac{1 + \epsilon^{-T/2\tau} - \epsilon^{-t/\tau}}{1 + \epsilon^{-T/2\tau} - \frac{4\tau}{T}(1 - \epsilon^{-T/2\tau})} \quad --- \quad (4)$$

where $\tau = 4RC$.

The effect of change of load voltage and load resistance or commutating capacitance can be determined, as shown in Fig.(3.6). It shows that waveshape and peak magnitude of load voltage changes appreciably with change of parameters. The magnitude of the load voltage must increase as 4.R.C. is increased in order to maintain the areas equal.

The time interval in which the anode-cathode voltage is negative immediately after conduction of a given S.C.R. is important for commutation. When the inductance is negligible the negative anode-cathode voltage interval is essentially the complete commutating period, which must be sufficient to allow the S.C.R. to regain its forward blocking capability. As shown in Fig.(3.7), this time interval increases with increasing load resistance or commutating capacitance. So, for a given load, the capacitance must be sufficient to provide the necessary commutating time.

The commutating time can be calculated for a constant d.c. current and pure resistive load by equating equation (1) equal to zero as:

$$e_L /t = to = 0 = \frac{RI(1+\epsilon^{-T/2\tau} - 2\,\epsilon^{-to/\tau}}{1+\epsilon^{-T/2\tau} - \frac{4\tau}{T}(1-\epsilon^{-T/2\tau})} \quad --(5)$$

$$2\epsilon^{-to/\tau} = 1 + \epsilon^{-T/2\tau}$$

$$-\frac{tc}{\tau} = \ln\frac{\epsilon^{-T/2\tau}+1}{2}$$

$$tc = \tau\ln\frac{2}{\epsilon^{-T/2\tau}+1}$$

The commutating time expressed in radians

$$\mu = \frac{2\pi}{T}\,tc = \frac{2\pi\tau}{T}\ln\frac{2}{\epsilon^{-T/2\tau}+1} \qquad \text{----- (6)}$$

It can be shown that commutating angle is approximately equal to power factor angle of the circuit. When the load inductance is present, the analysis becomes quite complicated. When inductance is quite large, the output waveform is nearly sinusoidal for many practical cases, so the analysis can be done:

$$I_{d,o1}\cdot E_{L,o}\sin\theta = \frac{E^2_{L,o}}{X_L'} \qquad \text{- - - (7)}$$

$$I_{d,o1}\cdot E_{L,o}\cos\theta = \frac{E^2_{L,o}}{R'} \qquad \text{- - - (8)}$$

where R' and X_L' are equivalent parallel load resistance and inductance

$$\left.\begin{aligned} \text{As}\quad \frac{1}{X_e'} &= \frac{1}{X_c} - \frac{1}{X_L} \\ \frac{E^2_{L,o}}{R'} &= E_d\, I_d \end{aligned}\right\} \qquad \text{- - - (9)}$$

For a square wave current:

$$I_{d,o1} = \frac{4}{\sqrt{2}\,T} \int_{0}^{T/2} I_d \cdot \sin wt \, dt$$

$$= \frac{2\sqrt{2}\,I_d}{T} \left[- \frac{\cos wt}{w} \right]_{0}^{T/2} = \frac{2\sqrt{2}}{\pi} \cdot I_d \quad \text{- - -} \quad (10)$$

combining (7) and (8):

$$E^2_{L,o} = \frac{I^2_{d,o1}\, R'^2\, X_c'^2}{R'^2 + X_c'^2} \quad \text{- - -} \quad (11)$$

combining (9) and (10):

$$I_d = \frac{\pi^2}{8} \, \frac{E_d}{R'} \, \frac{R'^2 + X_c'^2}{X_c'^2} \quad \text{- - -} \quad (12)$$

from (9): $E_{L,o} = \sqrt{E_d\, I_d \cdot R'} = \frac{\pi}{\sqrt{8}} \sqrt{\frac{R'^2 + X_c'^2}{X_c'}}$

For more generalised study of effect of change of different parameters on the performance of inverter can be done by simulating the circuit on analogue computer. The results can be summarised as:

(i) For pure resistive load, commutating angle increases with increase of resistance and peak amplitude of the load voltage is also increased, so resulting in greater voltage on the SCRs.

(ii) Commutating angle increases with increase of commutating capacitor with all other circuit parameter being constant.

(iii) When inductive load is added with other parameters constant, commutating angle is reduced and load voltage can become quite oscillatory.

(iv) When L_d is reduced, the load voltage becomes quite oscillatory for high resistive loads and this may cause the high peak voltages on controlled rectifiers.

Starting troubles:

1. Initial charge on the capacitor is necessary.
2. Residual flux in the core may cause saturation of the transformer, lower flux densities are used and air-gap may be provided.
3. Inverter should be tuned off by disconnecting the power rather than turning off the gate.

In order to improve performance with inductive loads additional feedback paths are provided for feedback of inductive energy into the supply.

3. Series Capacitor Commutated Inverters Fig.(3.8):

Generally it involves a series L-C resonant circuit to provide commutation. Resonant frequency of the circuit determines the duration of the damped sinusoidal pulse of current through the controlled rectifying element in series with the resonant circuit and the load. Series inverter can produce sinusoidal output if load is fixed. When load current is increased, the voltage on the capacitor increases. To reduce this problem feedback diodes can be used which will increase V operating load range also. Commutation is not so severe problem as in parallel capacitor inverter, so power switching is not needed. When SCR_1 is gated on, with SCR_2 off, a series resonant circuit is connected to d.c. supply. If the resistance in the load is zero, the capacitor voltage be $2E_d$ after first half cycle of oscillation and then conduction stops, as current drops below the SCR holding current. On second half cycle, when SCR_2 is closed, again it is series resonant circuit, with voltage $2E_d$ on capacitor as source. The current is again a sinusoidal pulse and capacitor charges to negative $2E_d$. Again, when SCR_1 is gated on, the capacitor voltage will be $-2E_d$ rather than zero. At the end of the third half cycle capacitor voltage is positive $4E_d$, assuming negligible losses. This voltage will go on increasing, but as the resistance is present in the practical circuits, so it will be limited by circuit parameters. The a.c. voltage across the load R may be determined by calculating the fraction of the fundamental and each harmonic in the applied square wave that appears across R. The effective value of fundamental component of the voltage across R can be given by:

$$E_{R1}\,c_1 = \frac{\sqrt{2}}{\pi}\,E_d \cdot \frac{R}{\sqrt{R^2 + (wL - \frac{1}{wC})^2}}$$

$$= \frac{\sqrt{2}\,E_d}{\pi}\;\frac{1}{\sqrt{1 + \left(\frac{wL - \frac{1}{wC}}{R}\right)^2}}$$

For practical cases, X_L and X_C are taken equal and many times of R. So, operating frequency will be [illegible] $1 / \sqrt{LC}$

at this resonance and current wave shape is also sinusoidal.

In practice the circuit given in Fig.(3.8) can not be used successfully over a wide range of load. For this, some modification is shown in Fig.(3.9). The reactor has been split into two parts, the centre tap going to load and outer terminals are connected to SCR^s, and supply. The condenser is also divided into two parts. The important advantage of this circuit is that one SCR may be turned on before the current in the other SCR oscillates to zero. When an SCR is turned on, a voltage is induced in the coupled winding of the reactor, which reverses the voltage on the other SCR, causing it to stop conduction. So, operating frequency can be somewhat higher than resonant frequency of series R-L-C circuit. The peak voltage on each SCR is also increased. The advantage of two capacitors is that on each half cycle, one half of the load current is obtained from d.c. source and one half is obtained by from capacitor. If $C_1=C_2=C$ and $L_1=L_2=L_1$ and E_d and R are equal as previous circuit, so average current for each half cycle will be half, so reduction in d.c. source ripple current. The large negative voltage on the SCR is obtained by action of the centre tapped reactor, which gives improved commutation.

4. Impulse Commutated Inverters:

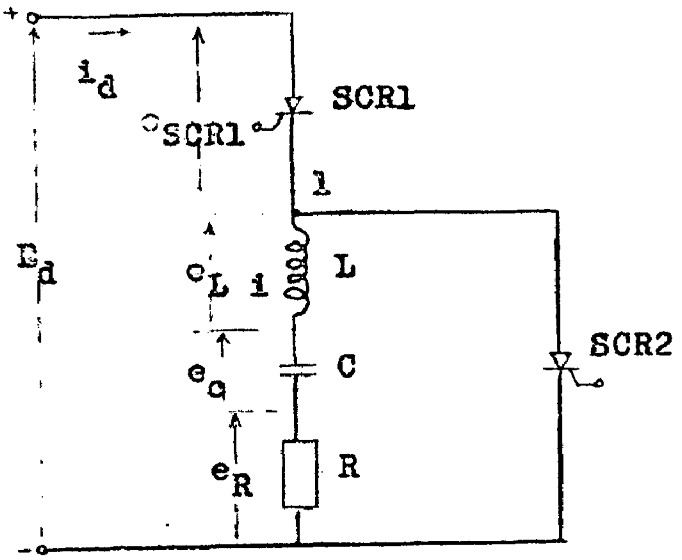
An impulse is used to briefly reverse the voltage on the conducting thyristor,allowing it to turn off.

The magnitude of the pulse must be sufficient to extinguish the current in the SCR and duration should be long enough to provide the necessary turn off time. Generally pulse is formed by means of an oscillatory L-C circuit, in which natural period is directly related to the turn off time of the controlled rectifier and characteristic impedance of the network is related to d.c. supply voltage and maximum value of load current which must be commutated. If the period of the a.c. output of the inverter is long compared with the turn off time of the controlled rectifiers, the size of the commutating components is relatively small.

The impulse can be generated either from some auxiliary commutating circuit or it may be generated by turning on the SCR that is complementry to the controlled rectifier being turned off. The feedback diodes generally used in the impulse commutated inverter contribute to the good regulation and ability to handle wide variation of load magnitude, power factor and frequency. They have small size with high efficiency. The voltage control can also be done by minor changes.

Auxiliary Impulse-Commutated Inverter Fig.(3.10):

In this centre tapped d.c. is used, the main SCR^s are gated on to conduct the current to the load during alternate half cycles of the a.c. output. When the load is reactive the diodes D_1 and D_2 conduct during part of



3.8 Basic series capacitor-commutated inverter.

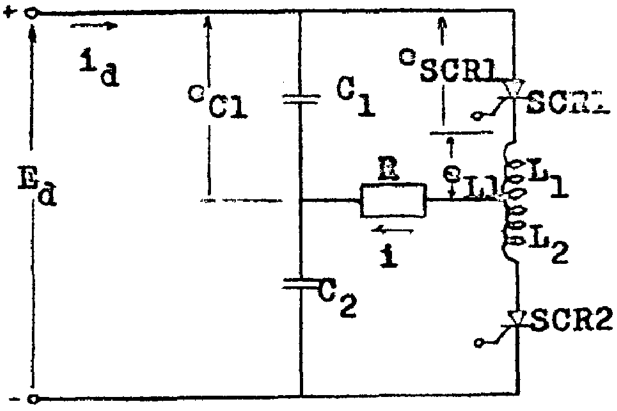
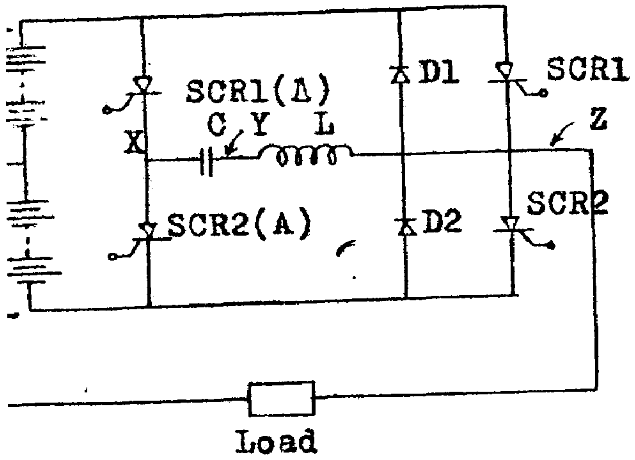


Fig. 3.9 Modifications to basic series capacitor-commutated inverter.



3.10 Auxiliary impulse--commutated inverter.

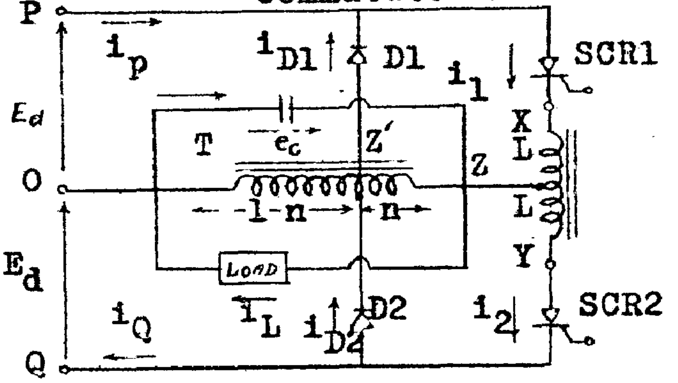
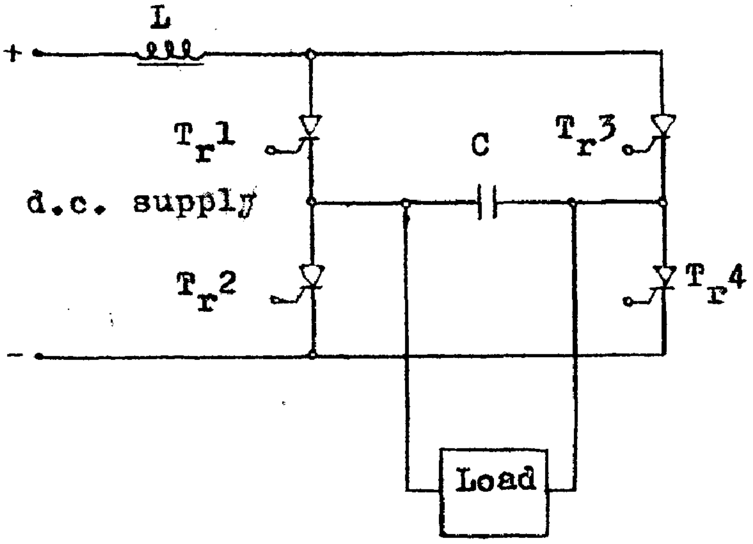


Fig. 3.11 Complementary impulse-commutated inverter.



4.1 Single-phase Bridge inverter.

each half cycle to return power from the load to d.c. supply. Commutation of the main controlled rectifiers is accomplished by means of the auxiliary controlled rectifiers $SCR_1(A)$ and $SCR_2(A)$ in conjunction with the capacitor C and the inductance L, which generate the impulse. The circuit can be operated upto a range of frequency, with period 10 times longer than the turn off time of thyristors.

<u>Operation:</u> Let SCR_1 is conducting current to the load from upper half supply, capacitor C is charged with Y point positive with respect to X. To commutate SCR_1, $SCR_1(A)$ is fired. The discharge current pulse through $SCR_1(A)$, C and L builds up to exceed the load current I_L, so current through SCR_1 is zero. The excess current flows through diode D_1. After reaching a peak, commutating current i_c starts to decay and c is charged with reversed polarity. During the time, D_1 is conducting, forward drop of D_1 appears as inverse voltage across SCR_1 and turns it off.

When i_c is zero, which occurs at $\pi\sqrt{LC}$ interval, SCR_2 is fired. Forward voltage is applied on SCR_1. A second and much smaller pulse of current i_c will flow from d.c. supply through $SCR_1(A)$, C, L_1, and SCR_2 to make up the losses incurred during the first pulse and complete the charge of capacitor to initial magnitude, but with opposite polarity. After second pulse $SCR_1(A)$ stop conducting. Now, when $SCR_2(A)$ is fired at the end of conducting half cycle of SCR_2 , capacitor is ready to commutate. With inductive load D_2 will conduct before SCR_2 is fired, then commutating current i_c falls below load current I_L. Energy stored in the commutating inductance L_1 at this time will cause the capacitor c to charge to a higher voltage, so it will produce large commutating current pulse. Thus the circuit has the advantage that commutating pulse varies with the load automatically. If commuting elements have higher Q. factor, commutating losses will be small and inverter efficiency high. The commutating pulse is minimum at no load, so losses will be less. The load voltage is a square wave under all conditions of loading. It is assumed that main controlled rectifier SCR_2 is gated exactly $\pi\sqrt{LC}$ seconds after auxiliary $SCR_1(A)$ is gated, and SCR_1 is gated $\pi\sqrt{LC}$ seconds after $SCR_2(A)$ is gated.

The time to available for recovery of main thyristor is the time during which the feedback rectifier carries the excess commutating pulse. Optimum commutating pulse is that which achieves the required turn off time with the least amount of energy $\frac{1}{2} CE^2_c$, where E_c is the voltage across the condenser. The optimum occurs when $I_m = 1.5\ I_L$, where I_m is peak commutating. The capacitor voltage and the commutating current pulse can build upto their maximum values even under no load conditions, simply by advancing the gating of main thyristor. The time delay t_1 between the gating of the auxiliary controlled rectifiers and the main thyristors is reduced to less than

$\pi \sqrt{LC}$. The optimum pulse conditon is achieved by :

$t_1 = 0.767 \pi \sqrt{LC}$ or $2.41 \sqrt{LC}$ seconds.

When the load has leading power factor, commutation is similar to no load condition.

McMurray and Bedford Inverter (11) Fig.(3.11):

It is similar to parallel inverters except feed-back diodes. D.C. power supply requires a center tap or a neutral point established by a pair of large capacitors. This is useful when small amount of a.c. power is required The feedback rectifiers are connected to taps on the primary winding of the output transformer, rather than to the ends of the windings in order to enable the feed-back of energy stored and otherwise trapped in inductor L just after commutation. The variation of power factor of load and output voltage is less as compared to parallel inverter.

Optimum values of L_1 and C of the above circuit are:

$$C = \frac{t_c \, I_{com}}{1.7 \, E_d} , \quad L = \frac{t_c \cdot E_d}{0.425 \, I_{com}}$$

where I_{com} = maximum value of load current at commutation

t_c = minimum turn off time for the SCR.

CHAPTER IV.

C_H_A_P_T_E_R _IV.

DESIGN OF INVERTER AND ITS CONTROL SCHEME: (10)

Inverter used for speed control:

Principle: In the Fig.(4.1) a single-phase arrangement is shown. For commutation, capacitor C has been connected in parallel with the load.

The thyristors are fired cyclically in the diagonal pairs. Suppose that at the end of a particular half cycle thyristors Tr_1 and Tr_4 are conducting, the capacitor C is charged so that its left hand plate is positive, Tr_2 and Tr_3 are now fired, the voltage on C is applied in reverse to Tr_1 and Tr_4. The current flowing in the input inductor L , together with the n current ~~flowing~~ in the ~~input inductor~~ load, discharges C and charges it agin in the opposite direction. Thyristors Tr_1 and Tr_4 are thus turned off provided that the discharge time of C is at least equal to their forward recovery time, so the output waveform is square in shape.

The above inverter is suited only for resistive loads. But if the load is inductive, the reactive energy causes the load voltage to rise relative to the d.c. input voltage and so may cause failure to commutate owing to the high forward voltages which appear across the thyristors. To avoid this, it is usual to provide an additional set of diodes as shown in Fig.(41.2)whereby reactive energy is returned to the d.c. supply at the

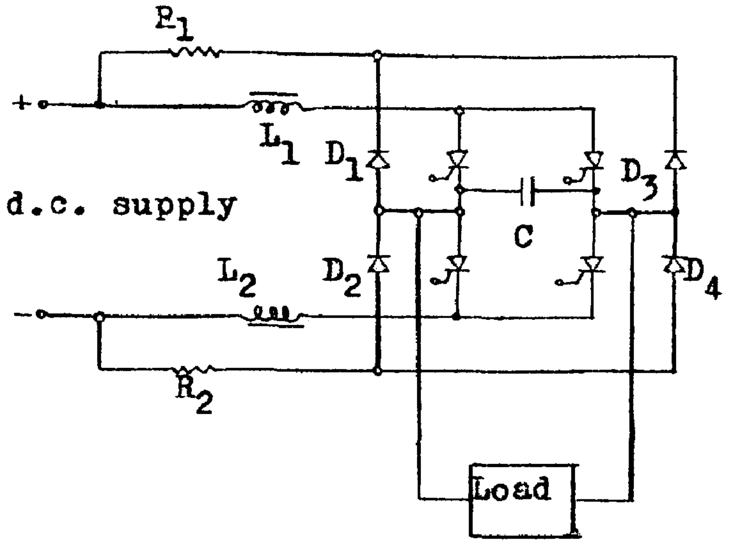


Fig.4.2 Single-phase Bridge Inverter with Diodes for reactive current feedback.

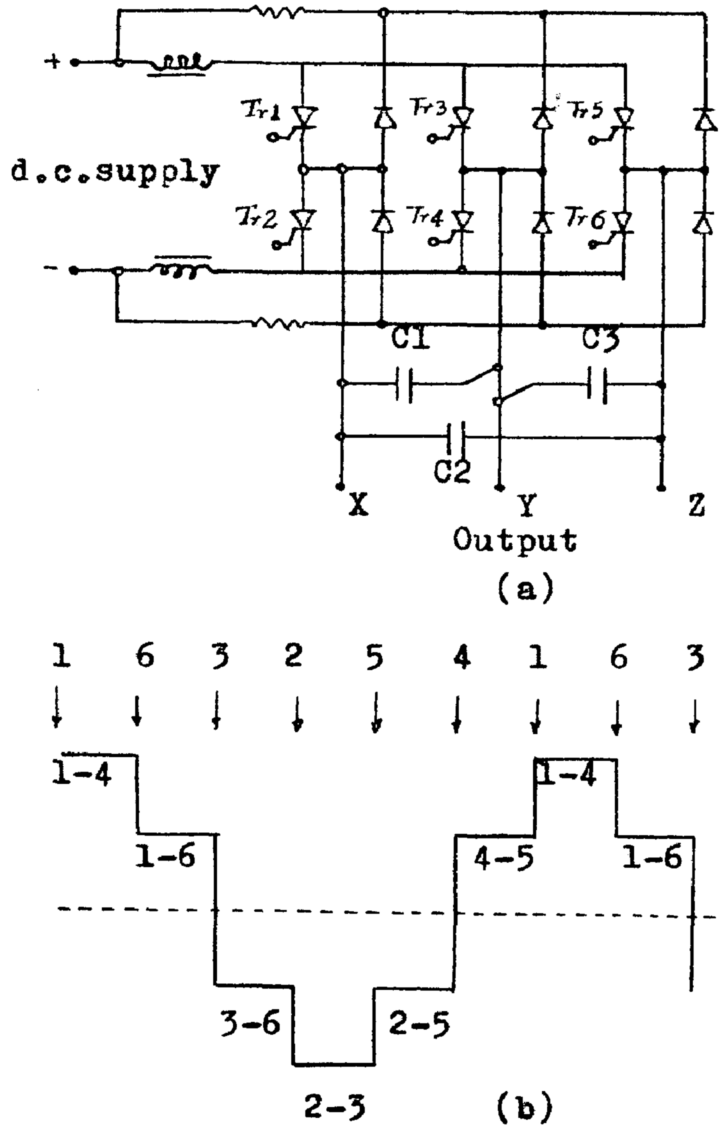
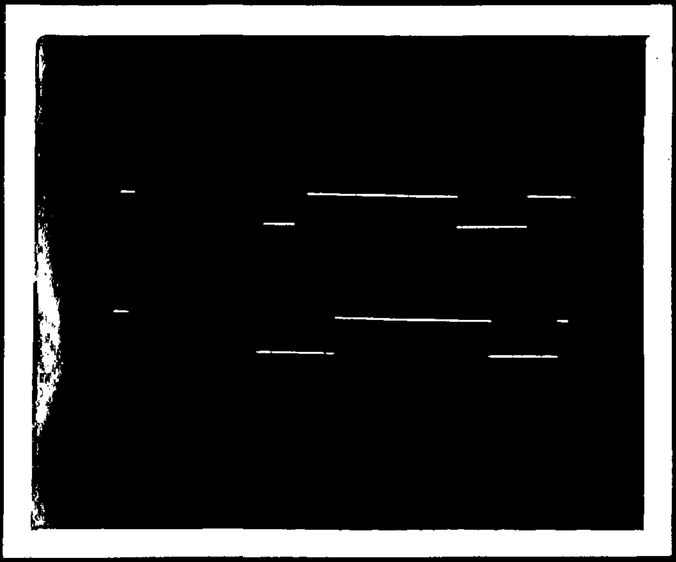
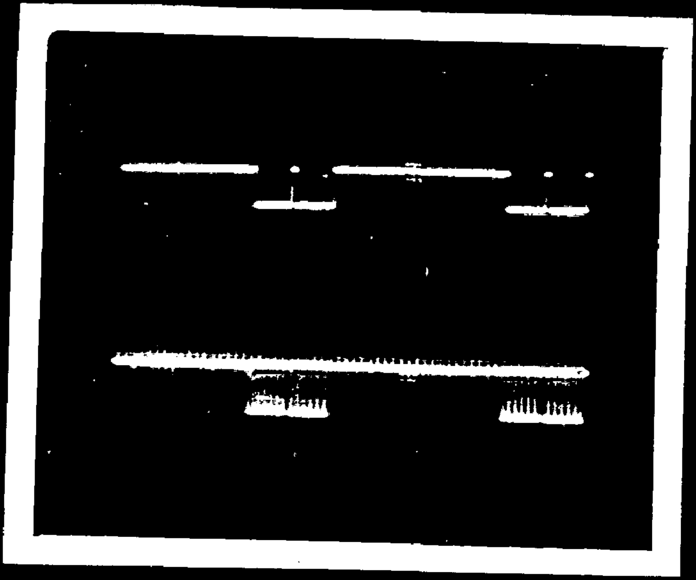


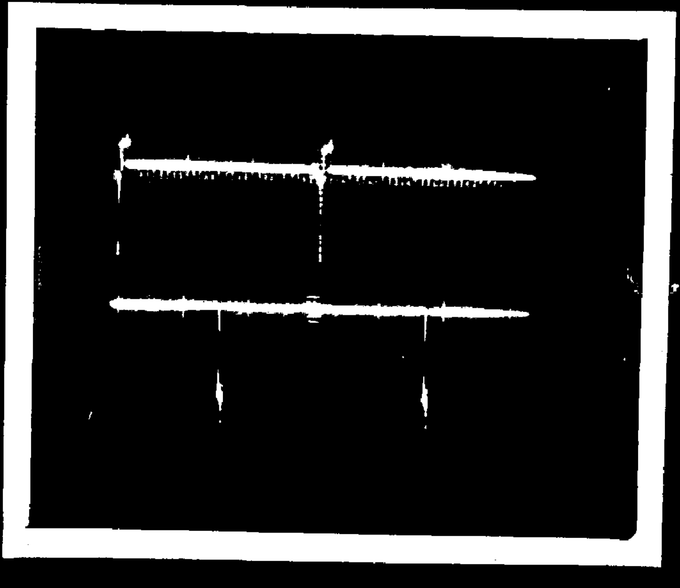
Fig.4.3 Three-phase Bridge-inverter
(a) Circuit;
(b) Idealised waveform of V_{XY} with resistive load.



Out-put of two adjacent stages of shift Register.



ut of shift Register
ate (showing carreir frequency).



Time delay in gate signals of Tr_8 and Tr_7(1000 c/s).

beginning of each half cycle and the voltage to which the thyristors are subjected are limited to little more than supply voltage.

To get three phase output similar units are connected to form a three phase bridge and three capacitors are provided to commutation of each phase, such an arrangement is shown in Fig.(4.3). The thyristors are fired according to a pattern in which there are six firing pulses per cycle, each thristor conducts, with a resistive load, for two sixth of the cycle. The conduction is shifted from one thyristor to the next in the upper and lower rows, alternately. For a resistive load, let Tr_1 and Tr_6 are conducting, so the supply voltage will appear at XZ and will be divided in XY and YZ terminals. If now Tr_3 is fired, voltage on C is applied in reverse across Tr_1 and so it will be turned off. Tr_3 and Tr_6 are now conducting and output voltages are modified. So output waveform will be stepped, which contain all odd harmonics except third and its multiples, giving fifth harmonic 20 per cent, seventh harmonic 14 per cent eleventh harmonic 9 percent etc, with fundamental 95 per cent of total.

4.1. Design of Invertor for Motor Control:

For normal loads, the above invertor described is suitable for a range of frequency. But if induction motor load is connected, to vary the speed over a wide range, there are following disadvantages:

(i) In ideal operating conditions, the commutation voltage which appear across the condensers is just half the supply voltage, and only half the total capacitor is effective.

(ii) At standstill and at very low speeds motor may require the full load or even higher current, while the voltage required is quite low. As commutating charge on capacitors is proportional to the load current, so at low voltages, greatest charge is needed, when voltage on capacitors is lowest.

(iii) When the motor is running, the e.m.f. generated within the motor distorts the inverter output waveform in such a way that voltage on the capacitors at the instants of commutation is lower even than would be expected.

The effect of these factors is to make the total capacitance required impracticably large. So, the commutating system required should be free from all the above defects. For this reason two additional thyristors are required Fig.(4.4). Tr_8 is fired at each desired commutating instant, i.e. six times per cycle. If condenser C is initially charged with its upper plate negative, when Tr_8 is fired, the voltage at the input to the bridge is reversed for a brief period. C is now charged positively from the main supply and due to stored energy in L_1 and L_2 acquires a voltage somewhat higher than the supply, so producing a reverse voltage on Tr_8 and turning it off by natural commutation. Tr_7 is fired before the next commutation, C now charges negatively through the small inductor L_3 so that after a half cycle of oscillation its voltage

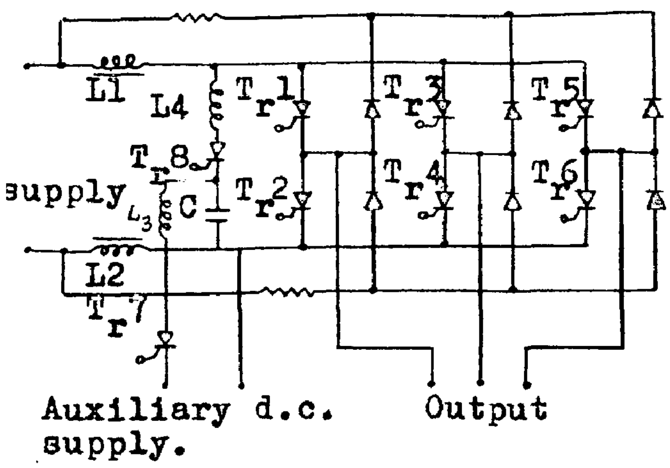


Fig.4.4 Practical Three-phase Bridge inverter with D.C.Commutation and Reactive feedback Diodes.

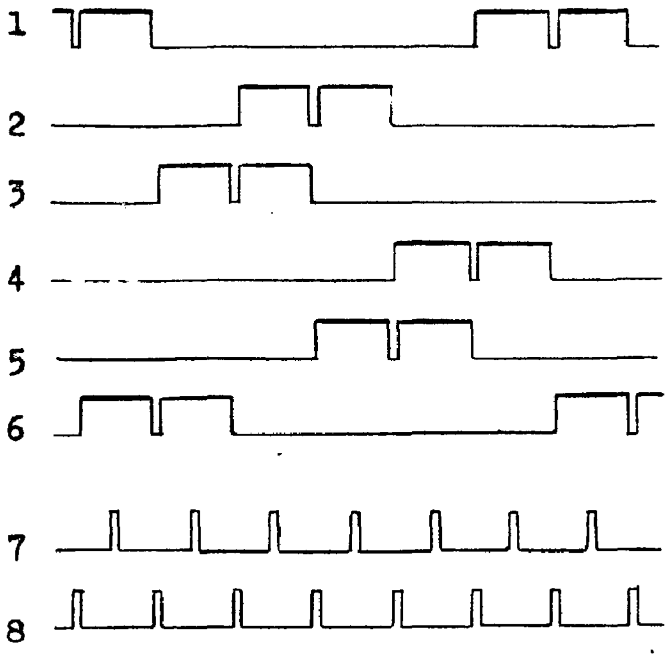


Fig.4.5 Pattern of Firing Pulses required by the inverter of Fig.4.4.

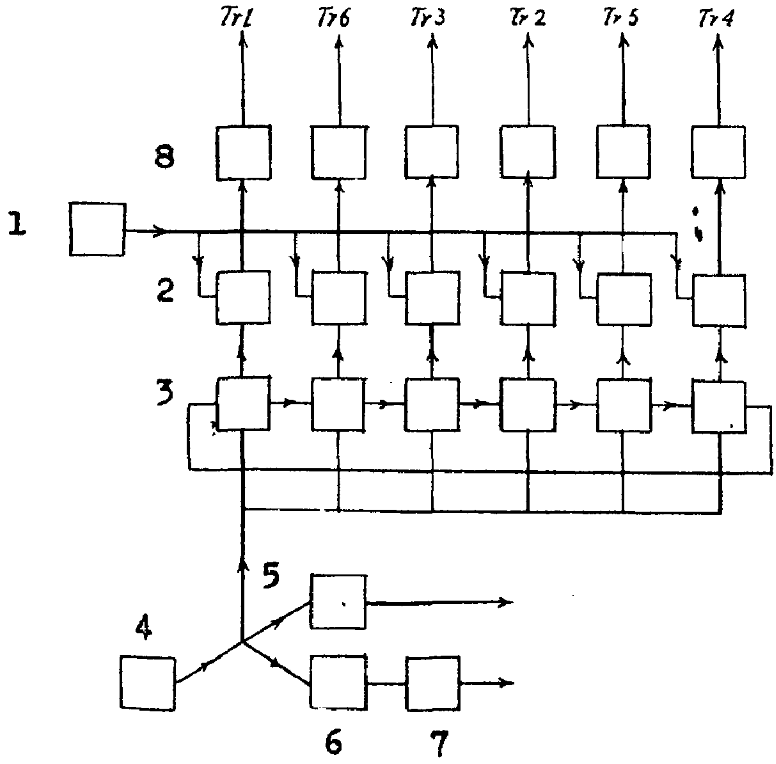


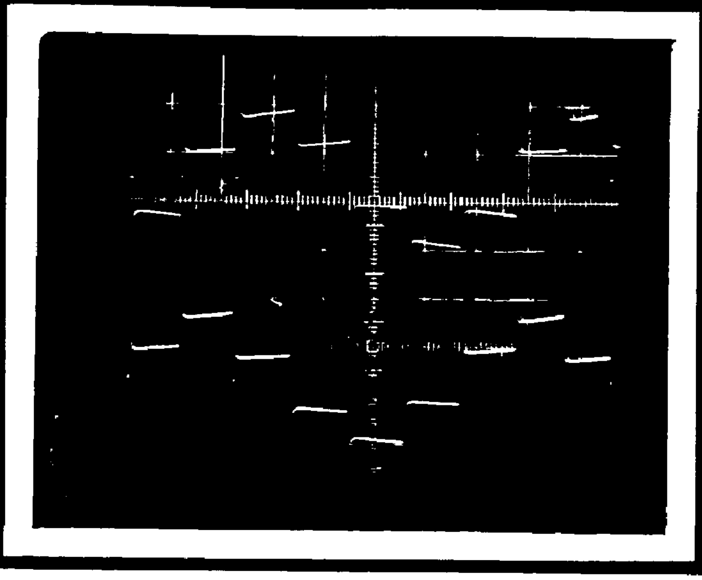
Fig.4.6 Control System for the inverter of Fig.4.4.

1. High-frequency carrier input
2. Gating circuits
3. Shift-register
4. Variable-frequency pulse-generator
5. Pulse amplifier
6. Delay circuit
7. Pulse amplifier
8. Pulse amplifier.

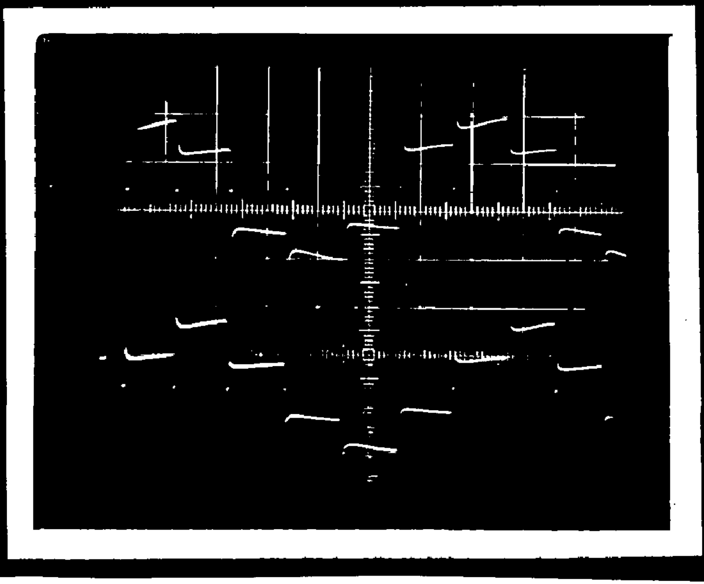
reaches a level which approaches twice the auxiliary supply voltage plus value of positive voltage after commutation.

So, in this case, the charge available is partially dependent on the main supply voltage and partially on auxiliary supply. When the main supply voltage is low, that is, when motor is at standstill, the commutating charge is entirely dependent upon the auxiliary supply, which must be adequate to ensure proper commutation of the highest motor current required. But when the main supply voltage is high, the commutating charge may be adequate without the effect of auxiliary supply, so, the d.c. commutating system provides complete flexibility to meet virtually any operating condition.

For the speed control, one half horse-power, three phase, 50 cycles G.E.C. Educational Kit motor has been used. Rated voltage at 50 cycles is 110 volts. As has been discussed in chapter III, the design of inverter components, with inductive load is quite difficult. But to have the approximate value of different inductors and capacitors, the circuit can be solved by Kirchhoff's Laws. The inductors L_3 and L_4 used are of about 10 μH. value. The commutating capacitor is 8μF. So time of half cycle of this L-c circuit is $\pi\sqrt{LC}$, which is approximately 30 μ sec. It was found that if size of L_3 and L_4 is increased, commutation failed at about one ampere load. For L_1 and L_2 inductors, two autotransformers have been used. If the value of L_1 and L_2 is increased, the waveshape of the inverter output is distorted, as the L-c



Out-put voltage of 3-φ Inverter, at 12 c/s with resistive load (XY, YZ phases).



Out-put voltage of 3-φ Inverter at 16 c/s with resistive load (XY, YZ phases).

components will act as oscillators, and so the shape of output voltage wave form will contain charging and discharging waveforms, superimposed. It was found that small values of inductors L_1 and L_2 gave quite satisfactory results. The value of L_1 and L_2 used is approximately in the range of a few hundred millihenries. If the condensers are put in parallel with induction motor load, the performance and stability improves i.e. the commutation improves with braking capability. The auxiliary voltage used for commutation was 100 volts. If it is decreased, the load carrying capacity of invertor reduces. It shows that auxiliary voltage and commutating condensers are important parameters for satisfactory performance. The feedback resistances should be of low values, other-wise there will be voltage on the diodes which may cause failure in satisfactory commutation. So carbon resistances of 15 ohms , 5 watts rating have been used.

4.2. Motor drive Invertor Ratings: (9)

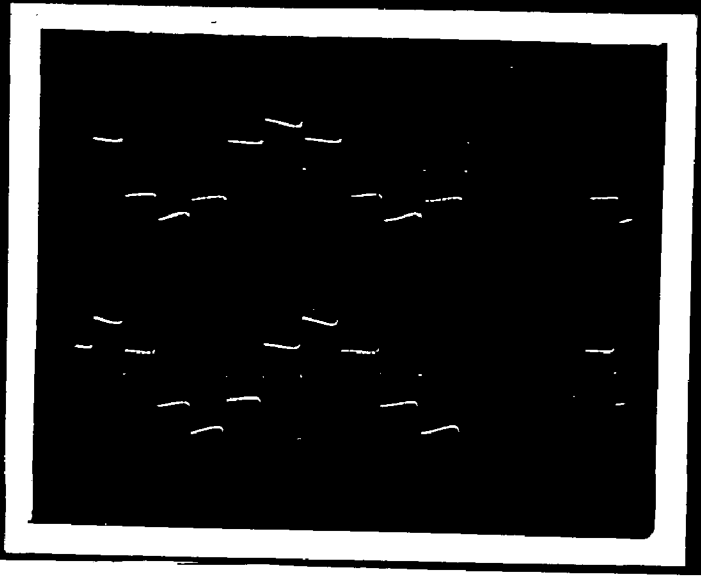
When designing the invertor, the different ratings of the SCR should be cared of. The static invertor equipment may have continuous and a short time over load rating. For a application the above ratings with commutatable load ampere rating should also be considered.

The continuous and momentary ratings depend upon the internal dissipation of the invertor. They determine the sizing of heat sink, cables, breakers etc. If the commutating rating is high, the overloads can be tolerated, if the overload time is reduced. The commutation rating depends upon the size of energy storage elements, minimum d.c. bus voltage and turn off time requirements of SCR^{s}.

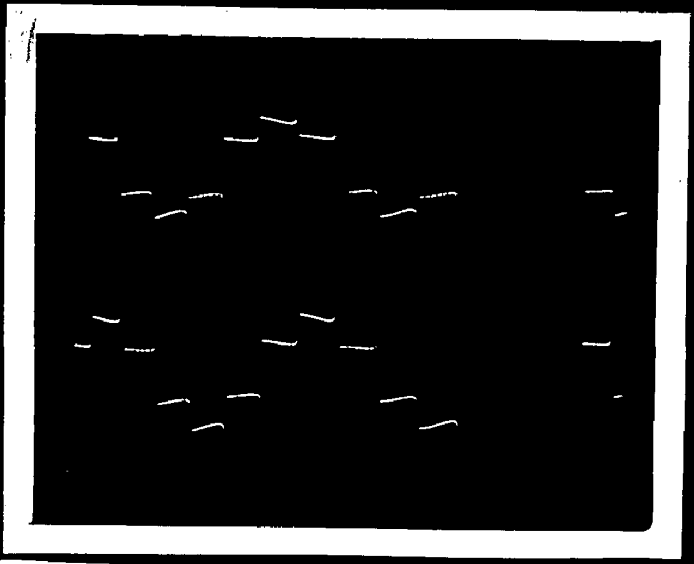
M/s. Charles D. Beck and Edgar P. Chandler has discussed the procedure for calculating the commutation ratings, in their paper. The commutating capacity should be sufficient to commutate the most possible combination of peak current, load transients, transients accompanying frequency change, operation out of synchronism, d.c. offsets, during motor starting, low d.c. bus voltage and motor manufacturing tolerances.

Due to peak circulating currents, the commutation burden increases. M/s Charles and Chandler have given the harmonic factors to calculate the maximum commutatable current, which heat the motor is: full load sine wave in amperes. $(\bar{H}_f - 1)$ + actual running load in sine wave, amperes.

The thyristors used are 10RC60, with average current rating of 10 amperes, so, for the present load, there is high factor of safety. Even then, cooling fins have been used with 3 amperes rating glass fuses, to protect the thyristors from excessive heat and current, which may flow in case of failure of commutation.



Out-put voltage of 3-φ Inverter at 50 c/s with resistive load (XY, YZ phases).



Out-put voltage of 3-φ Inverter at 80 c/s with resistive load (XY, YZ phases).

4.3. Control Circuits:(10)

Fig.(4.5) shows the pattern of firing pulses required by the various thyristors. As the load is inductive, and the load current therefore flow sometimes in the thyristors and sometimes in diodes, it is necessary for thyristors in bridge, to be supplied with extended gate signals rather than short pulses, and as the gate circuits of the three arms of the bridge are not at a fixed potential, some form of control circuit that permits continuous direct current to be switched and at the same time provides the required isolation must be used. For this purpose, high frequency carrier is switched, on the input side of an isolating transformer, with the extended gate signal, by an 'AND' gate in each thyristor. The output of gate is fed to amplifier and transformer. The output of the transformer is rectified to get the isolated signal. The photographs show the signals to be fed to 'AND' gate and output of 'AND' gate also.

The control signals for the thyristors are obtained from a counting circuit such as a shift register, in the manner shown in Fig.(4.7). The shift register comprises six binary stages connected in a ring in such a way that a pattern once set up in the circuit is shifted one stage round the ring on the receipt of a shift pulse, provision is made initially to set up a pattern giving outputs from two adjacent stages, and shift pulses are provided by a pulse generator which runs at six times the desired inverter frequency. The pattern of outputs from the oscillator is thus shifted according to the required firing sequence. Firing pulses for commutating thyristor Tr_8 are derived directly at the correct frequency from the pulse generator, and those for capacitor charging thyristor, Tr_7 from the same source but via a short delay Fig.(4.6). So, the correct sequence of pulses is provided, with perfect regularity, under the control of a single pulse generator, which can be fairly controlled.

4.4.1. Design of Control Circuits:

Shift Register Fig.(4.7): It is cascade connection of binaries, in which two inputs are fed to each binary. The binaries are connected to each other with delay circuits. The shift pulses are fed by the pulse generator, which is controlling the output frequency of inverter. The delay sections have a delay much smaller than the time interval between pulses and are required to ensure that an individual binary shall not receive a triggering signal simultaneously from the shift line and from a preceding flip flop. The shift pulses always drive the binaries to state zero. The coupling between the binaries is such that a succeeding flip flop will respond only if the preceding binary goes from state 1 to state 0.

Out-put voltage of 3-φ Inverter at 16 c/s with induction motor load(A phase).

The pulse which results from t is transition will drive the succeeding flip flop to state 1.

For the present application, six binaries are connected in series with delay circuits. The last stage output is fed to input of first binary with delay circuit. So the shift register is connected in ring. Monostable binary is used for delay purpose. Though Rc network can be used for delay but the performance was found not satisfactory. For starting, two first stages are set in 1 position and rest in 0 position. When a shift pulse is applied, it will change 1 to zero. So first two stages with rest of four stages will be in 0 position in transition stage. But when first two stages changes from 1 to 0, these give negative pulses, which put second and third stages to 1 and rest stages remain in zero. Now second and third stages are in 1 position and first with fourth to sixth stages are at 0. When next shift pulse is applied, above operation is shifted by one stage. At the end of sixth shift pulse, the original set up is obtained.

Design:(23)

1. Bistable Multivibrator: The self biased binary has been used, to avoid negative power supply for biasing. Assume that Q_1 is cut off and Q_2 is in saturation. Connections between the base of Q_1 and the collector of Q_2 are indicated in Fig.(4.8), the connections from the base of Q_2 to the collector of Q_1 are in Fig.(4.9). The The transistors used are 2SB75, p.n.p. germanium type.

Since $V_{EE} = (I_{B2} + I_{C2}) R_e$. To calculate saturation currents, the equivalent circuit for Q_2 is given in Fig.(4.9)(b). The collector circuit of Q_2 is replaced by Thevenin's voltage:

$$-\frac{V_{CC}(R_1 + R_2)}{R_1 + R_2 + R_C} = \frac{(-16)(22 + 10)}{22 + 10 + 4.7} = -13.95 \text{ V.} \qquad \text{-- --} \quad (1)$$

and its Thevenin's resistance $= \dfrac{R_C(R_1 + R_2)}{R_1 + R_2 + R_C}$

$$= 4.1\ K\Omega \qquad \text{-- --} \quad (2)$$

Similarly, the Thevenin's equivalent of base circuit of Q_2 is obtained from Fig. (4.9) as a voltage:

$$-\frac{V_{CC} \cdot R_2}{R_1 + R_2 + R_C} = \frac{(-16) \times (10)}{36.7} = -4.35 \text{ V.} \qquad \text{-- --} \quad (3)$$

in series with a resistance $= \dfrac{R_2(R_1 + R_C)}{R_1 + R_2 + R_C} = \dfrac{(10)(26.7)}{36.7}$

$$= 7.28\ K\Omega \qquad \text{-- --} \quad (4)$$

Hence the equivalent circuit of Q_2 is as shown in Fig. (4.9). Since a germanium transistor is under consideration, we assume, $V_{BE(sat)} \approx -0.3$ V and $V_{CE(sat)} \approx -0.1$ V.

The Kirchhoff's voltage equations are:

$4.35 - 03 + I_{B2}\,(7.28 + .47) + I_{C2}(.47) = 0$

and $13.95 - 0.1 + I_{B2}(.47) + I_{C2}(\,4.1 + .47) = 0.$

Solving, we find $I_{B2} = -0.342$ mA and $I_{C2} = -14.3$ mA

Hence $h_{FE(min)} = \frac{I_{C2}}{I_{B2}} = +\frac{14.3}{.342} = 41.9.$

The voltages in the circuit can be found:

$$V_{EN} = (I_{B2} + I_{C2})\,R_e = (-14.3 - .342).47$$

$$= -6{\cdot}89\ \text{V.}$$

$$V_{CN2} = V_{CE2} + V_{EN} = -0{\cdot}1 - 6{\cdot}89 = -6{\cdot}99\ \text{V.}$$

$$V_{BN2} = V_{BE2} + V_{EN} = -.3 - 6{\cdot}89 = -7{\cdot}19\ \text{V.}$$

$$V_{BN1} = V_{CN2}\cdot\frac{R_2}{R_1 + R_2} = -7{\cdot}19\cdot\frac{10}{32}$$

$$= -2{\cdot}245\ \text{V.}$$

$$V_{BE1} = V_{BN1} - V_{EN} = -2{\cdot}245 + 6{\cdot}89$$

$$= 4.645\ \text{V.}$$

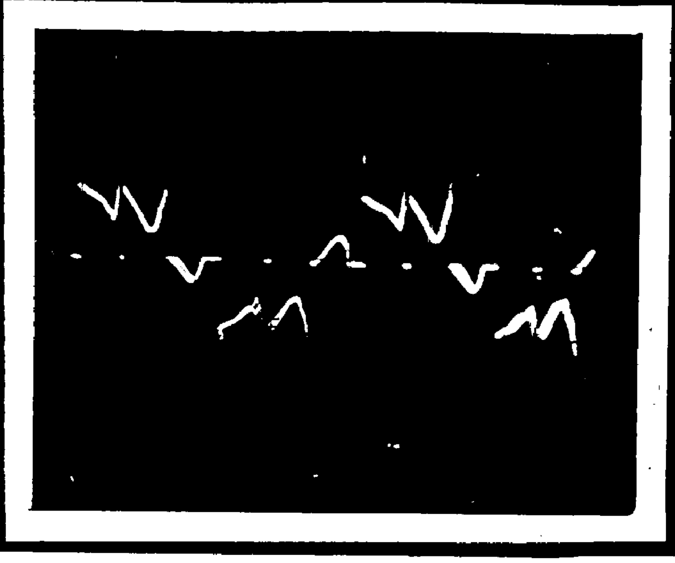
A positive value of V_{BE} of only about 0.1 V is required to cut-off a p.-n-p transistor. Hence Q_1 is certainly off.

From Fig. 4.9:

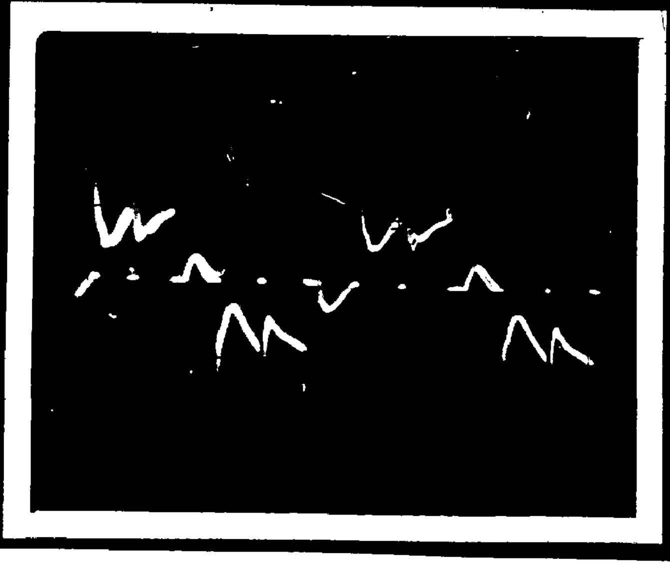
$$V_{CN1} = -\frac{V_{CC}\cdot R_1}{R_1 + R_C} + \frac{V_{BN2}\cdot R_C}{R_C + R_1}$$

$$= \frac{(-16)\cdot 22}{22 + 4.7} + \frac{-7{\cdot}19 \times 4{\cdot}7}{26.7}$$

$$= -13{\cdot}2 - 1{\cdot}265 = -14{\cdot}46\ \text{V.}$$



Out-put current of 3-φ Inverter at 30 c/s with induction motor load.



Out-put current of 3-φ Inverter at 50 c/s with induction motor load.

Output swing $= V_W = V_{CN2} - V_{CN1}$

$= -6{\cdot}99 + 14{\cdot}46$

$= 7{\cdot}47$ V.

As the very precisely values of voltages and currents are not required for flip flop circuits, so, assumption made for $V_{BE(sat)}$ and $V_{CE(sat.)}$ are valid.

Commutating Capacitors:

To reduce the transition time, small capacitors are introduced in parallel with coupling resistors of the binary. As these capacitors are used for making abrupt transitions between states, they are known as commutating or speed up capacitors. A compromise is made in transition and settling times, for fixing the values of these capacitors. So a 33pF capacitor has been assumed.

Maximum frequency of operation for which commutating condenser will increase the switching speed for above flip flop:

$$f_{max} = \frac{10 + 22}{2 \times 33 \times 10^{-12} \times 10 \times 22} = \frac{32 \times 10^{12}}{2 \times 33 \times 10 \times 22}$$

$$= 2{\cdot}27 \times 10^{9} \text{ c/s.}$$

Delay Circuit: For delay, monostable multivibrator has been used. The delay can be adjusted by varying the values of resistor and capacitors. The bistable circuit designed above is used for monostable circuit, with minor changes. For coupling resistor of first transistor one condenser is used, with resistor, which is connected to negative supply point. The delay time will depend upon the product of RC. For the present case, the time delay used is:

$$T = 0\ 69 \times 0{\cdot}02 \times 10^{-6} \times 22 \times 10^{3}$$

$$= {\cdot}304 \times 10^{-3} = {\cdot}304 \text{ millisecond.}$$

Triggering: Triggering signal which is usually employed to indicate a transition from one state to the other is usually a pulse of short duration, which is used to trigger either symmetrically or unsymmetrically. In unsymmetrical triggering the triggering signal is effective in inducing a transition in only one direction. A second triggering signal from a separate source must be introduced in a different manner to achieve the reverse transition. So, for the shift register, unsymmetrical triggering is used. Second pulse is derived from ~~[illegible]~~ previousstage. An excellent method of triggering a binary unsymmetrically on the leading edge of a pulse is to apply the pulse from a high impedance source to the output of the nonconducting device.

So, for the present scheme, the square wave is fed to the monostable circuit, which gives sharp pulses, which are used for triggering the binaries.

Output swing $= V_w = V_{CN2} - V_{CN1}$

$= - 6{\cdot}99 + 14{\cdot}46$

$= 7{\cdot}47$ V.

As the very precisely values of voltages and currents are not required for flip flop circuits, so, assumption made for $V_{BE(sat)}$ and $V_{CE(sat.)}$ are valid.

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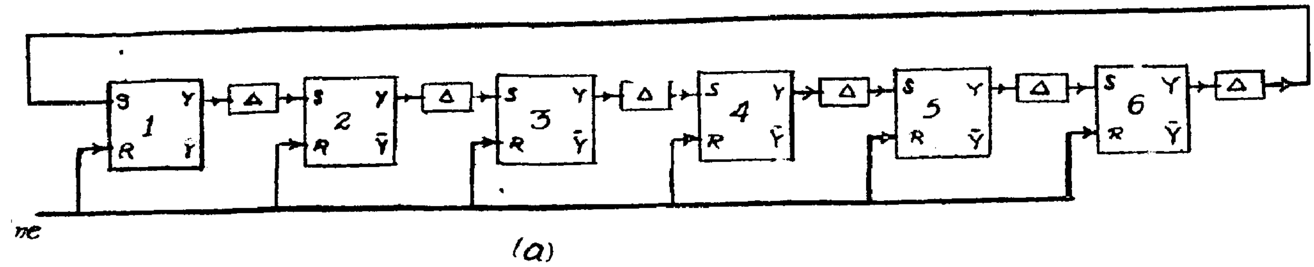
To reduce the transition time, small capacitors are introduced in parallel with coupling resistors of the binary. As these capacitors are used for making abrupt transitions between states, they are known as commutating or speed up capacitors. A compromise is made in transition and settling times, for fixing the values of these capacitors. So a 33pF capacitor has been assumed.

Maximum frequency of operation for which commutating condenser will increase the switching speed for above flip flop:

$$f_{max} = \frac{10 + 22}{2 \times 33 \times 10^{-12} \times 10 \times 22} = \frac{32 \times 10^{12}}{2 \times 33 \times 10 \times 22}$$

$= 2{\cdot}27 \times 10^9$ c/s.

Delay Circuit: For delay, monostable multivibrator has been used. The delay can be adjusted by varying the values of resistor and capacitors. The bistable circuit designed



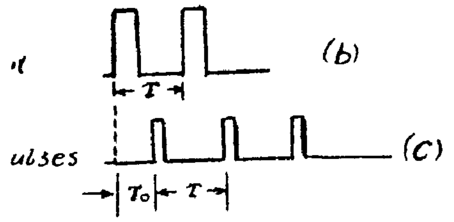
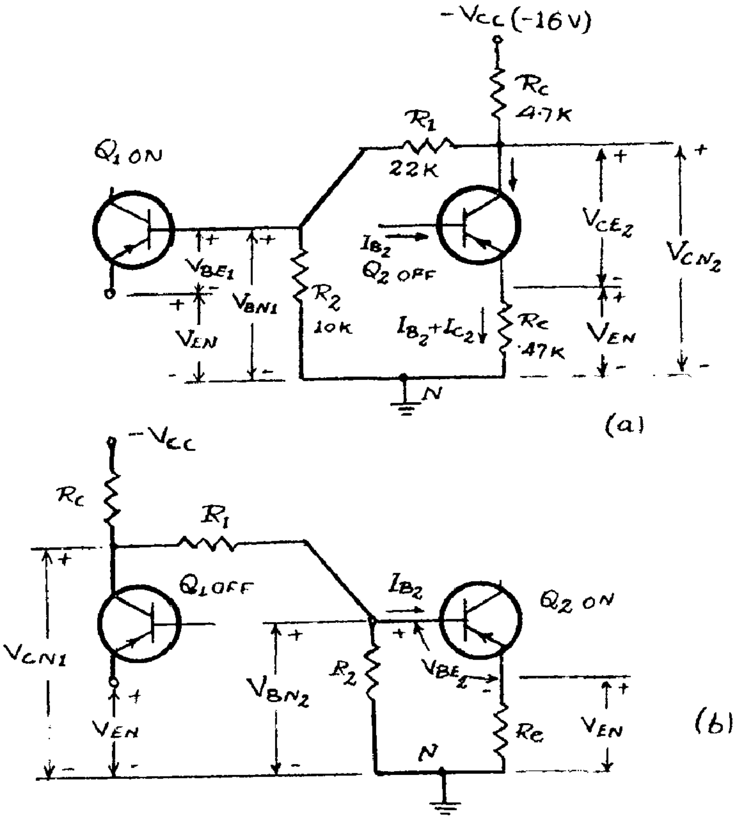
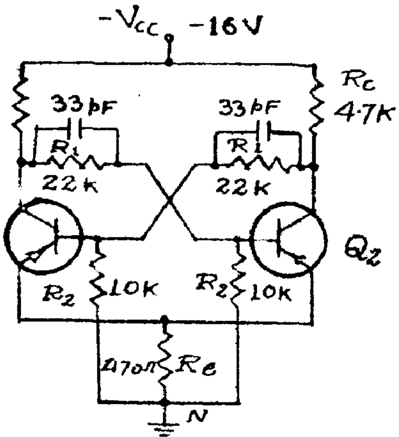


FIG. 4.7 (a) Shift Register, Δ is time delay.





·4·8 A self-biased p-n-p transistor binary.

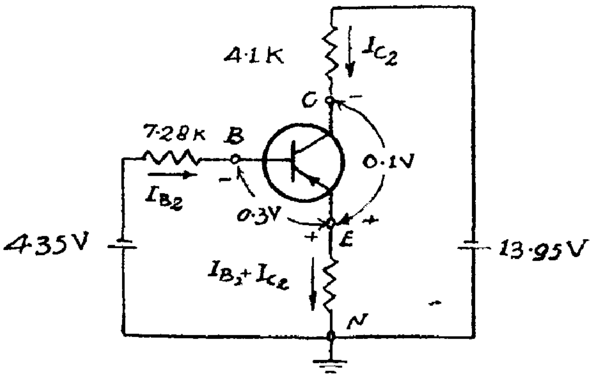
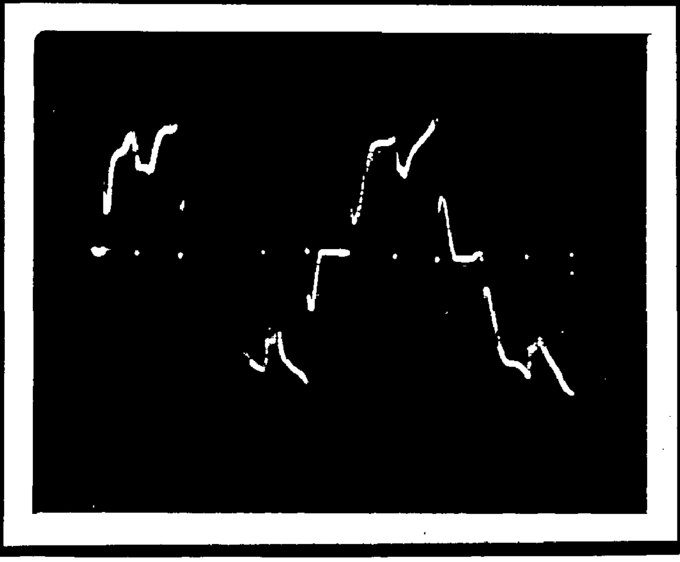


FIG. 4.9 The equivalent Circuit when Q_2 is in Saturation.



Out-put voltage of 3-φ Inverter at 50 c/s with induction motor load(RY phase).

The base of first transistor of each binary is fed by a diode and 10 K Ω resistance which are connected to the output of monostable, used as pulse generator. The design of monostable is similar to the design of bistable. As the second transistor is loaded by the six binaries through 10 K Ω resistances in parallel, the resistance at the collector of second transistor is taken only 500 Ω s. Emitter biasing is done with 47 Ω resistance. The time constant of pulses, is:

$$T = 0.69 \times .002 \times 10^{-6} \times 51 \times 10^{3}$$

$$= .07 \text{ milli seconds.}$$

The monostable is triggered through one condenser, to provide isolation and differentiation of square wave, obtained from square wave generator.

The output of binary stages are amplified before feeding them to the 'AND' gates. The amplifiers are of single stage. To avoid loading on the binaries, the base of amplifiers is fed by 15 K Ω resistances.

As the amplifiers should give quite large output, to saturate gates, so collector resistance should be low, which is taken 470 Ω s.

For high frequency, which is used as carrier frequency to feed the 'AND' gate, astable multi-vibrator is used.

Design of Astable Multi-vibrator:

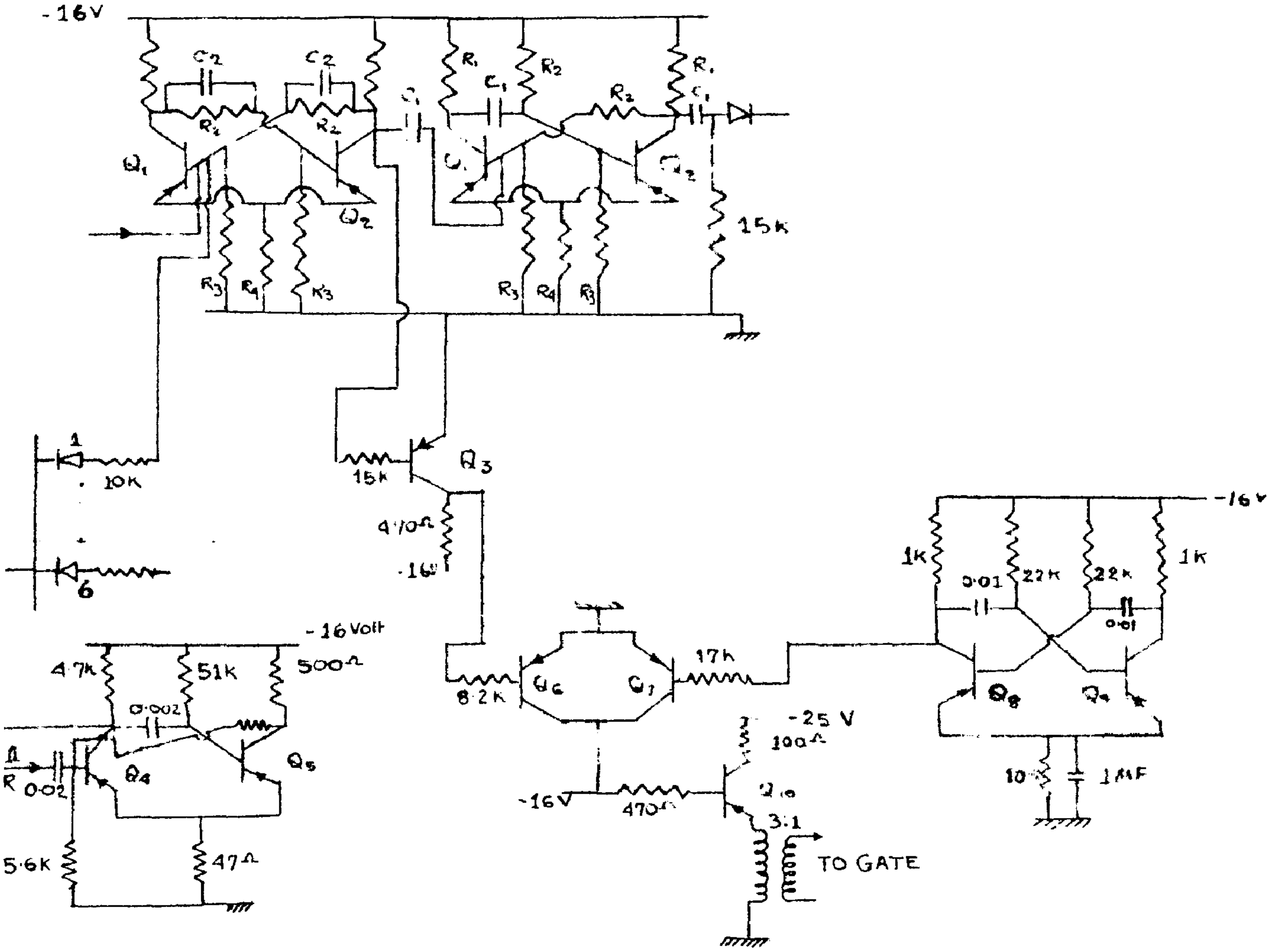
It is similar to bistable circuit, where capacitor coupling is used instead of resistor coupling, so neither transistor can remain permanently cut-off. The waveforms at the bases and collectors for the multi. are shown in Fig.(4.11). Before $t = 0$, Q2 is in saturation, carrying current I, while Q1 is below cut-off. Hence, for $t < 0$, V_{B1} is positive. $v_{C1} = -V_{CC}$, $v_{B2} = V_{BE(sat.)}$ and $v_{C2} = V_{CE(sat.)}$. Capacitor C_1 charges through R_1 and v_{B1} falls exponentially toward $-V_{CC}$. At $t = 0$, base B_1 reaches the cutin voltage V_γ and Q1 conducts. As Q1 goes to saturation, v_{C1} rises by I_{RC} to $V_{CE(sat.)}$, as indicated. The rise in v_{C1} causes an equal rise of $I.R_C$ in v_{B2} cuts off Q2, and its collector falls towards $-V_{CC}$. This fall in v_{C2} is coupled through capacitor C1 to the base of Q1, causing the undershoot δ in v_{B1} and abrupt drop by the same amount δ in v_{C2}. The waveforms at the base of Q1 and the collector of Q2 change exponentially with the time constant $\tau = (R_C + r_{bb'})\, C_1$ to the levels V_σ and $-V_{CC}$ respectively.

The voltage v_{B2} is $I.R_C + V_\sigma$ at $t = 0+$ and decreases exponentially with time constant $\tau_2 = R_2 C_2$ toward $-V_{CC}$. At $t = T_2$, B_2 reaches the cutin level V_γ and a reverse transition takes place. The waveforms in the first stage during the interval T_1 are the same as the waveforms in the second stage during the interval T_2 and are shown in Fig. 4.11.

Time Considerations:

The period T is given by:

For symmetrical circuit $R_1 = R_2 = R = 22K\Omega$, and $C_1 = C_2 = C = .01\ \mu F$.



DIODES ------ IN66

Q_1, Q_2 ------ 2SB75

Q_3 ------- AC126

Q_4, Q_5, Q_6, Q_7, Q_8, Q_9 } --- AC126

Q_{10} ---- AC128

$R_1 = 4.7K$, $C_2 = 33pF$

$R_2 = 22K$

$R_3 = 10K$

$R_4 = 470\Omega$

$C_1 = 0.02\mu F$

FIG. 4.10 One stage of shift-register with amplifier, gate, and transformer.

$\therefore \quad T = 22 \times 10^{3} \times .01 \times 10^{-3} \times 1.38$

$= .3$ milli second.

R_s is taken 1 KΩ. R_e is taken 10 Ω °. During the course of a transition, the emitter current I_E will vary by ΔI_E. To keep the emitter voltage V_{EE} almost constant during the transition time T_R, capacitor C_s is used to by-pass R_e. Value of C_s is decided by :

$$(\Delta I_E) \frac{T_R}{C_s} \ll V_{EE}$$

Fig. 4.10 shows the one stage of shift register, amplifier, gate and isolating transformer. The six stages feed the thyristors from Tr_1 to Tr_6. For Tr_7 and Tr_8, two more amplifiers are used. Tr_7 is fired with some delay so monostable binary, with required time constant is used, with the amplifier of Tr_7. Isolating transformers are used for these thyristors also.

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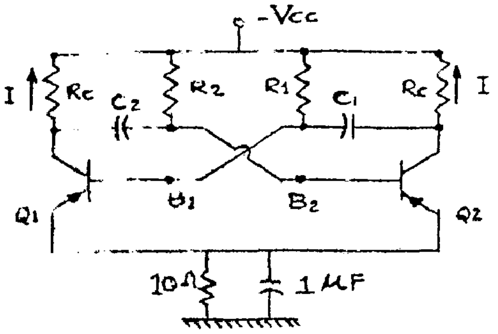


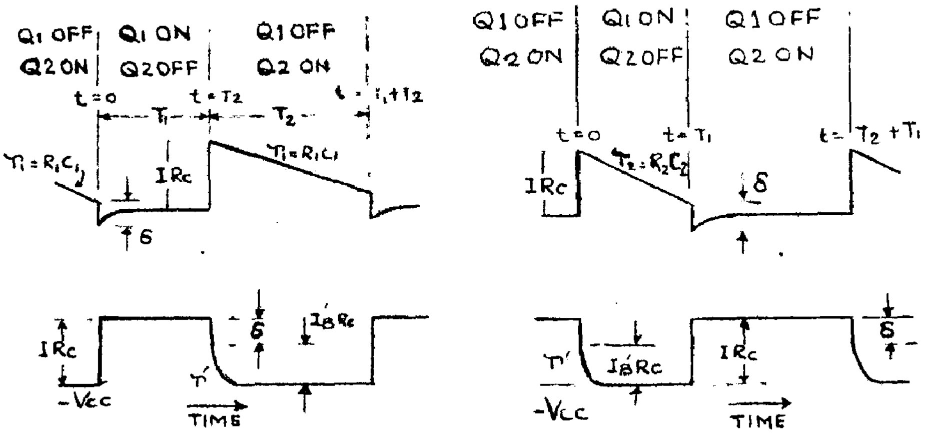
$C_1 = C_2 = 0.01\ \mu F$

$R_1 = R_2 = 22\ K$

$V_{cc} = 16V$

$R_c = 1K$

FIG 4.11(a) COLLECTOR COUPLED ASTABLE MULTIVIBRATOR



G 4.11(b) WAVEFORMS OF THE COLLECTOR COUPLED MULTIVIBRATOR (FREE RUNNING)

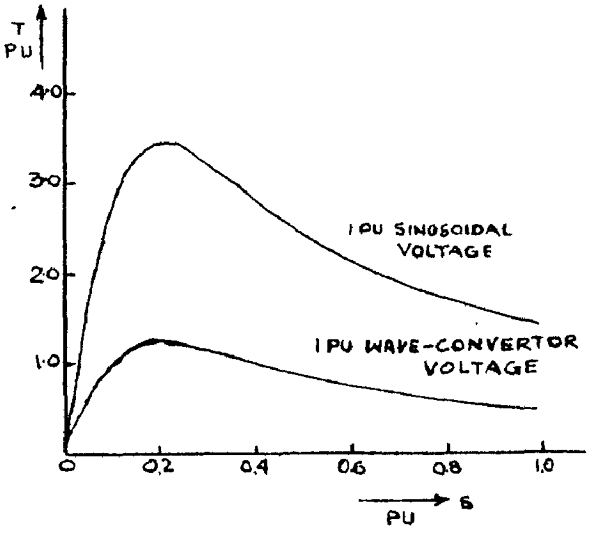


FIG.5.1 TORQUE SLIP CURVE OF AN INDUCTION MOTOR

CHAPTER V.

C_H_A_P_T_E_R_ V.

THE PERFORMANCE OF SYSTEM:

9.1. The complete variable frequency drive:

With varying the supply frequency, the voltage applied must also be varied, to keep the conditions in electric and magnetic circuits, normal. If the frequency is raised and voltage is kept constant, the magnetic field will rotate at faster rate and the increased back e.m.f. will be produced. If the supply voltage is not raised and motor does not require any increased back e.m.f. the magnetic field will be decreasedto such a point that a new field rotating at a new speed will generate the same back e.m.f. as the old field rotating at the old speed. This e.m.f. will be nearly the same as the applied voltage. Result will be decrease in magnetic field and so decrease in torque. The inverter used does not embody any facility for voltage control. For voltage control, an autotransformer is used, with a rectifier. So the variable d.c. voltage is fed to the inverter, whihh will give variable a.c. voltage on output side. The other method of voltage control can be, a three phase SCR rectifier, in which voltage can be controlled by feeding the same signal, which is used for inverter operation. But the drawback of this method is that voltage to frequency ratio can not be changed as needed for various applications.

If the motor is started at high voltage and frequency, there will be inrush of current corresponding to direct on line starting on a normal supply. The starting torque will be poor with starting current many times thefull load current, which is very undesirable from the point of view of both inverter rating and commutating capacity that must be provided. So motor is started by increasing frequency and voltage gradually from low initial values. For reversing the direction of rotation of the drive, the direction of operation of shift register is reversed.

5.2. Performance of practical variable frequency system:

The output waveforms of the inverter used, are shown with resistive and induction motor loads. The output waveform for resistive load is identical to the stepped waveform shown in Fig.(4.). But for induction motor load, voltage waveform is considerable distorted due to inductance of the load, but the harmonic content is not very different.

The inverter designed can give a frequency range from 2 c/s upto 100 c/s. At 2 c/s the thyristors will have to be derated, as only two arms of the inverter bridge will be carrying current for a long period.
At low frequencies, if the voltage to frequency ratio is increased, high starting torque can be achieved. At low frequency, there is quite a pulsation of torque, so lowest frequency is decided by the particular type of application.

Mr. G.C. Jain(28) has shown Fig.(5.1) that torque is reduced in the squared ratio of the fundamental component of input voltage wave in p.u. So, when harmonics are present, the machine will operate as if the applied sinusoidal voltage were reduced. The voltage reduction factor being the fundamental component of voltage wave shape, is expressed in p.u. For the better utilisation of the motor, the fundamental component in the voltage wave shape to the motor should be kept high. It has been found that if d.c. voltage to frequency ratio is kept constant, the torque reduces with increase of frequency, so it agrees with the Fig. 5.1.

In their paper Eugene A. Klingshirn and Howard E. Jordan,(29) have found the losses and performance of induction motor, when fed from nonsinusoidal source. The wave form, which is obtained from static invertors, can be analysed with Fourier Analysis:

$$v(t) = \sqrt{2}\,[\, V_1 \sin \omega t + V_5 \sin 5\omega t + V_7 \sin 7\omega t + \dots + V_k \sin k\omega t \,] \qquad --- \quad (1)$$

For analysis the motor may be assumed to be connected to different independent generators, all connected in series. Each generator represents one of the term in equation (1). So machine will have different equivalent circuits for different harmonics. Table I in Appendix shows that magnetising current for non-sinusoidal supply is more than for sinusoidal supply. The major contributing factor in reduction of inductances is due to the increased leakage flux produced by harmonic current with higher saturation of portions of magnetic circuit.

Klingshirn and Jordan have given method to calculate the magnetising inductance, wheren motor is supplied from non sinusoidal source. The losses in the motor are increased due to harmonics. Rotor harmonic losses are the main losses which are increased due to deep bar effect. For kth harmonic, the losses will be:

$m\,(I_k^r)^2\, r_k^r$, I_k^r and r_k^r are the rotor current and resistance respectively, for kth harmonic. m being the number of phases.

9.2. Stability analysis :

Rectifier-inverter drive systems are used in varied applications, for controlling the speed of a.c. machines by changing the frequency of applied voltage. At low frequency operation, the system becomes unstable, which is one of the main problems in the design of rectifier-inverter drive.

The complete generalised transient equations of a squirrel cage induction motor are non-linear and hence are extremely difficult to solve analytically. Rogers (16) has analysed the system by small oscillations about a steady state condition. The non-linear differential equations have been linearised and by Kron's transformation, these equations are converted into ordinary differential equations. He has shown that speed disturbances of an induction motor may be highly damped during operation at low frequencies.

Many workers(19,20,21,22) have simulated the system on analogue computer by assuming a linear magnetic circuit, uniform air gap and ideal stator winding distribution. Thomas A. Lipo and Paul C. Krause(19) have used the small displacement method to find the system stability by Nyquist stability criterion. The harmonics in the terminal voltages are neglected and machine is analysed in the synchronously rotating reference frame. The influence on system stability due to changes in several machine parameters, filter parameters and rectifier commutating reactance has been studied. The results have been compared with the results obtained on digital and analogue computer.

If the system load is switched from critical point of stability to unstable region the sustained oscillations occurs. But if load is switched to stable region the positive damping of oscillations brings a stable operating point. When the system is in unstable region the positive damping in oscillations will occur due to rectifiers and in that parts of oscillations which include operating points outside the region of instability. As the system oscillations increase, the rectifier current assumes an intermittent zero mode of operation due to the unidirectional current constraint. So, sustained oscillations will occur, when equivalent damping over a complete cycle is zero. It can be concluded that unless region of instability is sufficiently large machine will have sustained oscillations rather than breakdown.

If the inertia of the system is increased the region of instability is reduced. But at one particular intermediate value the system has maximum area of instability.

To enhance the inverter commutation, it may be desirable to make the magnetising reactance large so reducing the magnetising current. It was found that the system becomes unstable, for a given load, at a particular value of reactance. Mr. Lipo has also shown the effect by Nyquist plot. With increase of amplitude of fundamental of applied stator voltage, region of instability increases. Hence an increase of breakdown torque is accompanied by a larger region of instability. It shows that if V / f ratio is increased the region of instability increases.

If the value of condenser is reduced the instability region increases. In the practical set up it was found that if the condenser is reduced to a minimum, any change of load, caused the inverter to stop working. If the filter inductance is increased the region of instability increases. On the contrary, the increase of filter resistance causes the system stability to increase. If the commutating capacitor is increased the system becomes more stable. Hence, according to the load fluctuations, one can have the required region of instability. It can be concluded that at higher values of inductance of the system the region of instability increases, while increase of system capacitance the system becomes more stable.

Step Response:(14) P. J. Lawrenson and J.M. Stephenson have shown by analogue computer results that as the frequency of operation is reduced the damping of oscillations about synchronous speed changes. There is a particular frequency when damping of oscillations is minimum. This frequency can be found experimentally for a given system. With reduction in supply frequency, the frequency of oscillations falls, resulting in very long setting times. At the higher supply frequency, natural frequency is approximately independent of supply frequency and is inversely proportional to square root of inertia.

Rapid speed changing: If the voltage to frequency ratio is kept constant, the rapidly change of speed have less severe starting transients than with machine operated from a fixed frequency system. Also the ~~mum~~ run up time is also very much reduced.

Speed Reversal: The average useful torque in plugging is higher in variable frequency system than in fixed frequency system. The kinetic energy of the machine is fedback to the supply, so heating problem is also reduced in case of braking and speed reversal. The rate of change of supply frequency depends upon the system parameters. If the system is operating in high stability region, the machine braking can be done in reduced time.

CHAPTER VI.

CHAPTER VI

CONCLUSION:

6.1. Discussion:

As mentioned previously, the inverter designed has the advantage that a sudden change in load will not cause the failure of commutation. The price of this is an auxiliary d.c. voltage. But the additional advantages justify this provision of auxiliary d.c. voltage. The auxiliary d.c. voltage has been fed from a separate d.c. bus. Alternatively it can be taken either from a set of d.c. batteries or from rectifier. In case of railway traction where speed control is required by such a drive the auxiliary d.c. supply is not a problem. In selecting the auxiliary source, one must see that source impedance be small, so as to charge the commutating condenser in shortest possible time. The auxiliary voltage should be so limited that the sum of main d.c. voltage and twice auxiliary voltage should be less than the forward break over voltage of thyristor, otherwise the commutating thyristors may be damaged. The value of condenser depend on the maximum load current to be commutated.(11) It has been found that the performance of system improves, if condensers are connected at the a.c. side of inverter.

The drawback with the inverters is their nonsinusoidal output. As discussed in chapter V, the machine will operate as if operation for a source of reduced voltage,(28) because the torque for a machine operating from nonsinusoidal voltage supply is less than that of a machine operating from a source of sinusoidal voltage of equal r.m.s. value. A filter can be used at the output of inverter to improve the performance. For inverter, under discussion the waveshape has six steps, so its fundamental component is about 95 per cent of total. If more smooth sinusoidal wave is required, the control circuit of the system will be more complicated. One can have approximately sinusoidal wave by sub-harmonic method(18).

Within a last few years, sizeable amount of work has been done on stability of rectifier-inverter drives. These will provide a guide line for system design with an eye on optimum parameters for given conditions. Compared to induction load effect of large induction motor load, this system of speed control will have a favourable loading effect. It has been discussed in chapter V, that starting current is low with variable frequency system, when voltage and frequency are increased from load to rated values. Thus larger induction motors can be directly started from the lines without too large fluctuations of supply voltage.

6.2. Field of Application:

With robustness and simplicity, the induction motor has the drawback that its speed can not be controlled. Desired load characteristic can be obtained from variable frequency inverter driven induction motor. So, the field of application for an induction motor driven by static frequency inverter has increased tremendously. General Motors(25 , 26) is trying to develop the electric car driven by static inverter fed induction motor. With development of cheap batteries to supply the inverter, electric cars supersede the automobiles in near future.

6.3. Scope of Future Work:

In this dissertation the induction motor speed control has been attempted by feeding variable frequency supply to the stator. On the other hand if the variable frequency voltage is fed to rotor of wound rotor induction motor, there is possibility of wider range of speed control, with excellent braking characteristics. It has been shown by Prescott and Raju(27) that such a system is inherently unstable, with line frequency fed to stator and rotor. Further investigation on stability of this type of control with variable frequency supply on both stator and rotor may lead to useful results.

<u>Comments</u>: The reliability of the system can be enhanced by the use of printed circuits. In case of any fault replacement of faulty circuits becomes easier. This type of speed control with thyristors will be commercially feasible when thyristors are available at a reasonable price, which is expected in not too distant future.

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APPENDIX

TABLE I.

NO-LOAD TEST

Non-sinusoidal supply		Sinusoidal supply	
Current	Volts.	Current	Volts.
.6	27	.45	27
.62	28.7	.46	28
.62	30	.47	30
.63	32.5	.47	32
.64	34	.47	34
.69	39	.50	39
.71	41	.58	41.5
.73	43	.54	44
.78	47	.56	47

Note:- Instruments used for current and voltage measurements were of rectifier- type.

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